



# HARRIS

## RF COMMUNICATIONS

# RF-590 RECEIVER

# INSTRUCTION MANUAL





**LIMITED ONE YEAR WARRANTY  
HARRIS CORPORATION (RF COMMUNICATIONS GROUP)**

**FROM HARRIS TO YOU** – This warranty is extended to the original buyer and applies to all Harris Corporation, RF Communications Group equipment purchased and employed for the service normally intended, except those products specifically excluded.

**WHAT WE WILL DO** – If your Harris Corporation, RF Communications Group equipment purchased from us for use outside the United States fails in normal use because of a defect in workmanship or materials within one year from the date of shipment, we will repair or replace (at our option) the equipment or part without charge to you, at our factory. If the product was purchased for use in the United States, we will repair or replace (at our option) the equipment or part without charge to you at our Authorized Repair Center or factory.

**WHAT YOU MUST DO** – You must notify us promptly of a defect within one year from date of shipment. Assuming that Harris concurs that the complaint is valid and is unable to correct the problem without having the equipment shipped to Harris:

- Customers with equipment purchased for use outside the United States will be supplied with information for the return of the defective equipment or part to our factory in Rochester, NY, U.S.A., for repair or replacement. You must prepay all transportation, insurance, duty and customs charges. We will pay for return to you of the repaired/replaced equipment or part, C.I.F. destination; you must pay any duty, taxes or customs charges.
- Customers with equipment purchased for use in the United States must obtain a Return Authorization Number, properly pack, insure, prepay the shipping charges and ship the defective equipment or part to our factory or to the Authorized Warranty Repair Center indicated by us.

Harris Corporation  
RF Communications Group  
Customer Service  
1680 University Avenue  
Rochester, NY 14610, U.S.A.

Telephone: (716) 244-5830  
Telex: 240313  
Cable: RFCOM UR

Harris will repair or replace the defective equipment or part and pay for its return to you, provided the repair or replacement is due to a cause covered by this warranty.

**WHAT IS NOT COVERED** – We regret that we cannot be responsible for:

- Defects or failures caused by buyer or user abuse or misuse.
- Defects or failures caused by unauthorized attempts to repair or alter the equipment in any way.
- Consequential damages incurred by a buyer or user from any cause whatsoever, including, but not limited to transportation, non-Harris repair or service costs, downtime costs, costs for substituting equipment or loss of anticipated profits or revenue.
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**IMPORTANT** – Customers who purchased equipment for use in the United States must obtain a Return Authorization Number before shipping the defective equipment to us. Failure to obtain a Return Authorization Number before shipment may result in a delay in the repair/replacement and return of your equipment.

**IF YOU HAVE ANY QUESTIONS** – Concerning this warranty or equipment sales or services, please contact our Customer Service Department.



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# RF-590 RECEIVER

## INSTRUCTION MANUAL

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**HARRIS CORPORATION** RF COMMUNICATIONS GROUP  
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Equipment manufactured by Harris Corporation, RF Communications Division meets stringent quality and safety standards. However, high voltages are present in many radio products, and only a skilled technician should attempt to remove outer covers and make adjustments or repairs. All personnel who operate and maintain the equipment should be familiar with this page as a safety preparedness measure. Although this procedure is reproduced as a service to the personnel involved with this equipment, Harris Corporation assumes no liability regarding any injuries incurred during the operation and repair of such equipment, or the administration of this suggested procedure.

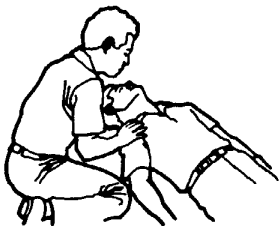
**ELECTRICAL SHOCK: EMERGENCY PROCEDURE**

The victim will appear unconscious and may not be breathing. If the victim is still in contact with the voltage source, disconnect the power source in a manner safe to you, or remove the victim from the source with an insulated aid (wooden pole or rope). Next, determine if the victim is breathing and has a pulse. If there is a pulse but no breathing, administer artificial respiration. If there is no pulse and no breathing, perform CPR (if you have been trained to do so). If you have not been trained to perform CPR, administer artificial respiration anyway. Never give fluids to an unconscious person.

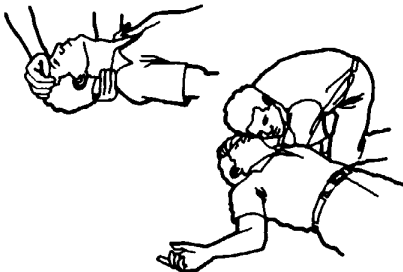
**WHEN BREATHING STOPS**

**FIRST**, send someone to get a **DOCTOR**.  
**THEN**, administer first aid to restore breathing (artificial respiration):

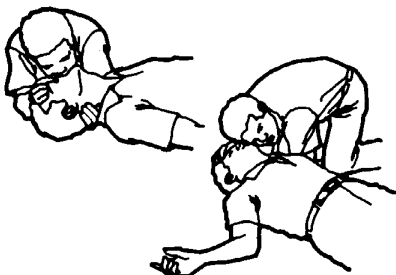
**1 IF A VICTIM APPEARS TO BE UNCONSCIOUS**  
TAP VICTIM ON THE SHOULDER AND SHOUT, "ARE YOU OKAY?"



**2 IF THERE IS NO RESPONSE**  
TILT THE VICTIM'S HEAD, CHIN POINTING UP. Place one hand under the victim's neck and gently lift. At the same time, push with the other hand on the victim's forehead. This will move the tongue away from the back of the throat to open the airway.  
**IMMEDIATELY LOOK, LISTEN, AND FEEL FOR AIR.**  
While maintaining the backward head tilt position, place your cheek and ear close to the victim's mouth and nose. Look for the chest to rise and fall while you listen and feel for the return of air. Check for about five seconds.



**3 IF THE VICTIM IS NOT BREATHING**  
GIVE FOUR QUICK BREATHS.  
Maintain the backward head tilt, pinch the victim's nose with the hand that is on the victim's forehead to prevent leakage of air, open your mouth wide, take a deep breath, seal your mouth around the victim's mouth, and blow into the victim's mouth with four quick but full breaths just as fast as you can. When blowing, use only enough time between breaths to lift your head slightly for better inhalation.  
If you do not get an air exchange when you blow, it may help to reposition the head and try again.  
**AGAIN, LOOK, LISTEN, AND FEEL FOR AIR EXCHANGE.**



**4 IF THERE IS STILL NO BREATHING**  
CHANGE RATE TO ONE BREATH EVERY FIVE SECONDS.



For more information about these and other life-saving techniques, contact your Red Cross chapter for training.  
"When Breathing Stops" reproduced with permission from an American Red Cross Poster.

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**RF-590 HF-SSB SYNTHESIZED RECEIVER  
SPECIFICATIONS**

<b>Frequency Range</b>	10 kHz to 29.999999 MHz
<b>Frequency Resolution</b>	1 Hz increments standard
<b>Tuning</b>	Continuous with seven selectable tuning rates and keypad entry.
<b>Tuning Time</b>	Tuning time between any two frequencies is less than 20 milliseconds.
<b>Frequency Stability—Internal</b>	± 1 part in 10 <sup>6</sup> per day — Standard TCXO ± 1 part in 10 <sup>8</sup> per day — Optional OVEN
<b>Frequency Standard I/O</b>	Input: 1, 5, or 10 MHz; 1 Vrms Output: 1, 5, or 10 MHz (depends on internal frequency standard chosen); 1 Vrms
<b>Channel Memory</b>	100-channel capacity capable of being loaded locally or remotely with complete receiver parameters. Battery backup provides retention of operational parameters without power for one month minimum.
<b>Scanning</b>	Scan any set of consecutive channel numbers (channel scan) or one of ten pre-programmed sets of random channel numbers (group scan).
<b>Readout/Display</b>	Receiver frequency, BFO frequency, channel assignment, mode, IF BW/filters, AGC, BITE, dwell, and scan group.
<b>BFO</b>	10 Hz synthesized tuning, ± 9.99 kHz
<b>Internal Preselector</b>	Low Pass Filter — standard Suboctave Filters — optional (internal module) Digital Preselector — optional (internal module)
<b>Maximum Signal Input</b>	Receiver protected to 100 watts (72 Vrms) available power input.
<b>Modes of Operation</b>	CW, 2-ISB (optional) 4-ISB (optional), AM, FM, LSB, USB, FSK (with external demodulator), Special Data Modes (Link 11, etc.)
<b>Squelch</b>	Syllabic Rate Squelch (CW, SSB, AM) and Noise Squelch (FM), both operated from a common front panel adjustable control.
<b>Sensitivity</b>	100 kHz-30 MHz — for 10 dB $\frac{S+N}{N}$ ratio CW: 0.15 uV (300 Hz bandwidth) AM: 1.5 uV (6 kHz bandwidth) SSB: 0.35 uV NOTE: Below 100 kHz, sensitivity degrades 20 dB/decade.
<b>IF Bandwidths</b>	Up to six IF bandwidths plus LSB and USB.

IF Filter	-3 dB BW (kHz)	IF Filter	-3 dB BW (kHz)
CW	0.3	FM Wide Band	16
CW	1.0	USB	2.8
AM	3.2	LSB	2.8
AM	6.0		
AM	16		

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<b>Intermodulation</b>	In Band: -50 dB or better for two 100 mv (-7 dBm) signals within the IF passband. Out of Band: -50 dB or better for two 0 dBm signals separated 30 kHz or more.
<b>Cross Modulation</b>	-20 dB or better for 500 mV 30% modulated interfering signals removed 20 kHz or greater from the desired signal of 10 uV.
<b>Reciprocal Mixing</b>	The apparent noise appearing at the receiver input when in a 3 kHz bandwidth, caused by a 0 dBm signal 100 kHz off tune, is less than 1.0 uV (-107 dBm).
<b>Quieting</b>	Ultimate (S + N)/N: 50 dB
<b>Spurious Responses</b>	Image and IF: -100 dB Spurious: Internal -123 dBm equivalent or less; external -80 dB.
<b>AGC Range</b>	Less than 3 dB audio output variation for 1 uVrms to 1 Vrms RF signal range. (Threshold internally adjustable from .5uVrms to 5uVrms.)
<b>AGC Time Constants</b>	Attack time < 20 milliseconds. Decay time: Front panel selectable as follows: Slow, 4 ± 1 second Medium, 200 ± 50 milliseconds Fast, less than 30 milliseconds
<b>Manual RF Gain</b>	Front panel control, 125 dB range.
<b>AGC I/O</b>	Separate AGC inputs/outputs are provided on the rear panel.
<b>Audio Outputs</b>	Phone: +10 dBm/600 ohms/1% distortion Line Output: -16 to +10 dBm/600 ohms/1% distortion Speaker Internal: 2.0 W/8 ohms/5% distortion Speaker External: 2.0 W/8 ohms/5% distortion Hum and Noise: Less than -50 dB Pass Band Ripple: 3 dB maximum
<b>IF Outputs</b>	Filtered or unfiltered 455 kHz second IF.
<b>Built-In Test Diagnostics</b>	Fault isolation to replaceable module level, with front panel alphanumeric indication.
<b>Power Requirements</b>	100, 120, 220, or 240 Vac selectable; 47-420 Hz, 75 watts typically.
<b>Temperature</b>	Operating: -10 to +55° C Nonoperating: -62° C to +71° C
<b>Humidity</b>	0 to 95%
<b>Size</b>	Rackmount and desk mount capability. 5.25H x 19W x 20.5D inches maximum (13.3H x 48.3W x 52.1D, cm)
<b>Weight</b>	40 pounds (18.1 kg)
<b>Remote Control (Optional, Internal Module)</b>	A microprocessor based system capable of accepting asynchronous serial data in accordance with any one of the following formats: MIL-STD-188C, EIA Standard RS-232-C, or RS-422. Remote Control Functions: Frequency, Channel Select, IF BW, Mode, AGC-TC, BFO, Fault-BITE Status, Scan Select, RF/IF Gain, and Channel Load.

### **ABOUT THIS MANUAL**

This manual is divided into five major sections indicated by blue tabs with section 5 further divided into sub-sections indicated by white tabs. The blue tabs indicate the introduction, installation, operation, technical description, and maintenance sections, while the white tabs indicate the detailed repair information for each assembly.

# **RF-590 RECEIVER**

## **INSTRUCTION MANUAL**

**HARRIS**  
RF COMMUNICATIONS



RF-590 Receiver

## SECTION 1

### INTRODUCTION

#### 1.1 INTRODUCTION

This manual contains information necessary to install, operate, maintain, and repair the RF-590 HF-SSB Synthesized Receiver. This manual is subdivided into the five following sections.

- Section 1: Introduction. Contains an introduction to the RF-590. Includes RF-590 basic description, feature highlights, optional auxiliary equipment, etc.
- Section 2: Installation. Includes site selection, power requirements, mechanical installation, interconnect requirements, initial setup and power on, and a functional checkout.
- Section 3: Operation. Includes general operating instructions, control, and indicator descriptions.
- Section 4: Technical Description. Contains general receiver characteristics, receiver block diagram, AGC-gain distribution chart, and signal path and synthesizer functional descriptions.
- Section 5: Maintenance. Contains general repair techniques, component handling techniques, self-test (BITE) descriptions and error code listings, receiver performance test procedures, and component data sheets.

Also included, as subsections, are all subassembly and main chassis descriptions, schematics, parts lists, component location details, and subassembly test procedures.

#### 1.2 GENERAL DESCRIPTION

The RF-590 is a high performance synthesized communications receiver designed to tune AM, CW, FM, USB, LSB, and ISB (optional) signals from 10 kHz to 30 MHz (in 1 Hz increments) utilizing digital tuning techniques. Up to 100 channels of frequency, detection mode, filter bandwidth, AGC mode, and BFO offset can be stored in memory, and recalled individually, or scanned sequentially or in groups. The receiver contains a comprehensive built-in test equipment (BITE) network which allows extensive microprocessor controlled self-testing to isolate faults at the modular level.

Manual tuning and channel selection is activated via a front panel touch pad or tuning knob. Operating parameters such as detection mode and filter bandwidth (typically: CW - .3 kHz, 1 kHz; AM - 3 kHz, 6 kHz, 16 kHz; USB/LSB - 3 kHz; FM-16 kHz.) and AGC mode (slow, medium, fast, off) are push-button selectable. Receiver operating parameters and self-testing results are displayed on two front panel



numeric and alphanumeric displays. Full remote control capability is accomplished with an optional remote control system compatible with MIL-STD-188C, EIA Standard RS-232-C, or RS-422 formats.

The rear panel contains BNC 50 ohm connectors for the following inputs/outputs: RF antenna input, filtered 455 kHz IF output, unfiltered 455 kHz DSB output, ISB output, 1, 5 or 10 MHz frequency standard input, and frequency standard output. Additionally, other connectors allow access to 600 ohm line audio outputs, AGC input or output, speaker mute, local control lines, and other functions (see table 2-2 and 2-3).

The receiver is entirely modular in design to facilitate maintenance. The unit may be rack mounted with the following considerations.

- Dimension — 5.25H x 19.0W x 20.5D inches maximum (13.3H x 48.3W x 52.1D, cm)
- Weight — 40 pounds (18.1 kg)
- Power requirements — 115/230 Vac, 47-420 Hz, 75 watts typically, 85 watts maximum (with all options)

Note that a complete listing of all RF-590 specifications may be found at the beginning of this manual.

### 1.3 RF-590 RECEIVER FEATURES

The RF-590 is a modern high performance HF-SSB receiver utilizing the latest device technology and circuit techniques. The use of a microprocessor as the central control unit allows a cost effective design offering many versatile features. These features include:

- Synthesized digital tuning and readout in 1 Hz steps from 10 kHz to 30 MHz.
- Keyboard control
- Continuous single knob tuning
- Full remote control by digital asynchronous commands with a wide variety of standards and rates.
- Built-in test equipment (BITE) fault isolation to replaceable module level.
- Preset channel memory — Up to 100 front panel programmable channels can be stored in a nonvolatile memory. Frequency and mode are stored in memory for instant recall.
- Channel scanning — Automatically searches preprogrammed channels, with a selectable dwell time.

- Synthesized variable BFO –  $\pm 9.99$  kHz in 10 Hz steps.
- Diversity capability – With external RF-575 Diversity Combiner.
- Multimode operation – Including USB, LSB, CW, AM, and FM. (ISB and FSK optional).
- Squelch – Syllabic rate (AM, SSB, CW) or noise operated (FM), operated from a common front panel control.
- Plug in subassemblies – All subassemblies can be replaced using common hand tools.

#### 1.4 COMPATIBILITY

The RF-590 HF Receiver is compatible with the following RF products.

- RF-551A Preselector (requires a RF-553-01 option)
- RF-575 Quad Diversity Combiner
- RF-130, RF-1130, and RF-745 Transmitters

#### 1.5 CUSTOMER OPTIONS

Table 1-1 is a list of RF-590 optional equipment.

**Table 1-1. RF-590 Optional Equipment**

Number	Name	Part No.	Description	Publication No.
RF-518	Earphones	724-0075	For reduction of ambient noise levels or to utilize private listening.	None
RF-553-01	Remote Control Interface	10073-6910	Permits the RF-590 to remotely control the RF-551A Preselector.	SU-10073-6911 (supplement)
RF-567	High Impedance RF Input Transformer	1920-1450	Improves reception when untuned antennas are used.	1920-1452 (Instruction Sheet)
RF-575	Diversity Combiner	7634-0000	Selects audio from the receiver with the strongest signal.	7634-1030
RF-592	Remote Control	10073-6210	Provides complete remote control of Frequency, Mode IF/BW,	SU-10073-0017 (supplement)

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**Table 1-1. RF-590 Optional Equipment (Cont.)**

Number	Name	Part No.	Description	Publication No.
RF-592 (Cont.)			AGC Speed, BFO, BITE/Fault Status, Scan, RF/IF Gain Control, Channel Select and Channel Load.	
RF-593	High Stability Frequency Option	759-3906	1 MHz frequency standard with proportional temperature control. 1 part in 10 <sup>8</sup> stability.	10073-0020 A12/A21 section
RF-594-01	Rack Mount	10073-0055	Includes slides and related hardware for rack mounting applications.	10073-0020 (installation section)
RF-594-02	Desk Top Case	10073-0045	Enclosed case for desk top installation.	10073-0020 (installation section)
RF-594-03	Stack Mount	10073-0035	Includes hardware for standard stack mounting applications.	10073-0020 (installation section)
RF-595-01	ISB Option	10073-6310	Allows simultaneous operation in USB and LSB modes.	SU-10073-0018 (supplement)
RF-595-02	Delay Compensated ISB Option	10073-6360	Delay compensated filtering for critical data communications. Provides less than 500 u/sec. differential time delay from 400 Hz to 2900 Hz. Offers less than 2 dB ripple in the 300 Hz to 3 kHz passband.	SU-10073-0022 (supplement)
RF-596-01	Half Octave Filter	10073-6410	Offers filtering protection from 2 to 30 MHz in 8 half-octave band filters. Also, for frequencies below 2 MHz, Low Pass filtering is provided.	SU-10073-0019-1 (supplement)
RF-596-02	Digital Tuned Bandpass Filter	10073-6510	Provides over 20 dB of selectivity at ±10% of tuned frequency. Reduces interference from close transmitters.	SU-10073-0019-2 (supplement)

**Table 1-1. RF-590 Optional Equipment (Cont.)**

<b>Number</b>	<b>Name</b>	<b>Part No.</b>	<b>Description</b>	<b>Publication No.</b>
RF-597	Noise Blanker	10073-6800	The Noise Blanker removes impulse type noise from received signals. Adjusts automatically to received signal level changes.	10073-6808 (supplement)
RF-598	4ISB Option	10141-5010	Provides simultaneous operation on four independent sidebands.	10141-5020
RF-651-02	Receiver Multicoupler (2 port)	RF-651-002	Permits operation of two receivers from a common antenna. At the same time, it provides isolation between receivers.	7733-000
RF-651-04	Receiver Multicoupler (4 port)	RF-651-004	Same as RF-651-002, but with 4 ports.	7733-000
RF-651-08	Receiver Multicoupler (8 port)	RF-651-008	Same as RF-651-002, but with 8 ports.	7733-000

## 1.6 SPECIALIZED REQUIREMENTS

Harris/RF Communications Group Systems Division specializes in translating exacting customer needs into complete systems packages. No job is too small or too large. Contact the following for specialized requirements.

Harris Corporation/RF Communications Group  
 1680 University Avenue  
 Rochester, New York 14610 U.S.A.  
 Phone: (716) 244-5830  
 Cable: RFCOM; Rochester, New York  
 Telex: 978464

**SECTION 2**

**INSTALLATION**

**2.1 INTRODUCTION**

The following paragraphs provide unpacking and inspection information, equipment installation and mounting instructions, site selection, interconnection data, and receiver functional test procedures.

**2.2 UNPACKING AND INSPECTION**

Carefully open the shipping carton and check the contents against the packing list secured to the outside of the container. Inspect all items for signs of damage. Immediately notify the carrier if any damage is discovered. Save all packing material for possible reshipment.

**2.3 ANCILLARY KIT**

Items that are supplied in the RF-590 Ancillary Kit, (part no. 10073-0021) are listed in table 2-1.

**Table 2-1. Ancillary Kit (P/N 10073-0021)**

Quantity	Part No.	Description
5	F03-0002-019	Fuse, 1 amp, slow blow
5	F03-0002-022	Fuse, 1-1/2 amp, slow blow
1	W-0023	Cord, Line, 6 feet
1	Z80-0001-000	Tool, Tuning

The following connectors are available to mate to the rear panel connectors (J7, J8, and J9).

J22-0001-001	Connector, Type D, 25 pin
J22-0010-000	Connector, Type D, 37 pin
J55-0015-825	Shell, D Connector*
J55-0015-837	Shell, D Connector*

\*Note: The two D connector shells are provided with various sized grommets to accommodate different sized cables.

## 2.4 SITE SELECTION

The RF-590 provides specified performance in any environment within the temperature range of -10°C to +55°C and up to 95 percent humidity. Consider the following factors when determining the operating location for the RF-590.

- Avoid sites which will subject the receiver to conditions exceeding those mentioned above. If this is not possible, provide an environmentally controlled site (adequate ventilation, temperature control, etc.) to maintain the stated operating limits.
- Avoid nearby obstructions such as hills, trees, buildings, and power lines which absorb and reflect radio signals. In particular, avoid obstructions that are in a direct line with the desired directions of reception.
- Some antennas, especially the doublet, are directional and should be oriented for maximum signal gain. Therefore allow enough land area around the site to orient the antenna as necessary.
- Reception is generally best at the top of a hill, over level ground, or over water.

Once the operating site has been chosen, consider the following factors when positioning the RF-590 at the site.

- Ease of operation and visibility of controls
- Relation to other units
- Power, control, and output interfaces
- Environmental considerations for unit and operator (temperature control, adequate ventilation, etc.).

**WARNING**

Always operate the RF-590 with a heavy gauge ground strap connected from a solid earth ground to the RF-590 rear panel ground lug (provided for this purpose). Failure to do so could result in serious injury or death to the operator if the receiver should ever fail in such a manner as to make the chassis electrically hot.

### 2.4.1 Antennas

Maximum receiver sensitivity is achieved when the antenna input impedance presented at antenna input connector, J1, is 50 ohms. The use of coaxial cables, such as type RG-58/U terminated with a BNC connector, prevents feed-line noise pickup and provides the proper impedance match.

Doublet antenna kits, such as the RF-334 and SB-AD, are available from Harris Corporation/RF Communications. Three basic types of antennas, the horizontal doublet, the inverted V, and the slant wire can be constructed with these kits. Figure 2-1 shows these three antenna types used in typical installations. Each type of doublet antenna has two legs of equal length, one connected to the center conductor of the coaxial cable and the other connected to the shield. The two legs have a combined electrical length of one-half wavelength (one-quarter wavelength for each leg).

The inverted V and slant wire doublets are useful if the antenna site prohibits the use of the two supports required for a horizontal doublet, or if the supports cannot be located so that the doublet is perpendicular to the direction of the desired transmitted signal. All doublet antennas are directional and provide best response to signals received from directions perpendicular to their lengths. The length of each element of a doublet can be determined from one of the formulas given in table 2-2.

**Table 2-2. Calculation of Doublet Antenna Element Lengths**

Antenna Type	Length of Each Element (Feet)	Length of Each Element (Meters)
Doublet, horizontal, or slanted	$\frac{234}{f(\text{MHz})}$	$\frac{71.3}{f(\text{MHz})}$
Inverted V doublet	$\frac{245}{f(\text{MHz})}$	$\frac{74.5}{f(\text{MHz})}$

## 2.5 INITIAL SETUP AND ADJUSTMENTS

The advanced design of the RF-590 Receiver minimizes initial setup and adjustment procedures. The initial setup and adjustment should include:

- Connecting memory backup battery
- Adjusting front panel display brightness
- Adjusting LSB and USB audio output levels

### CAUTION

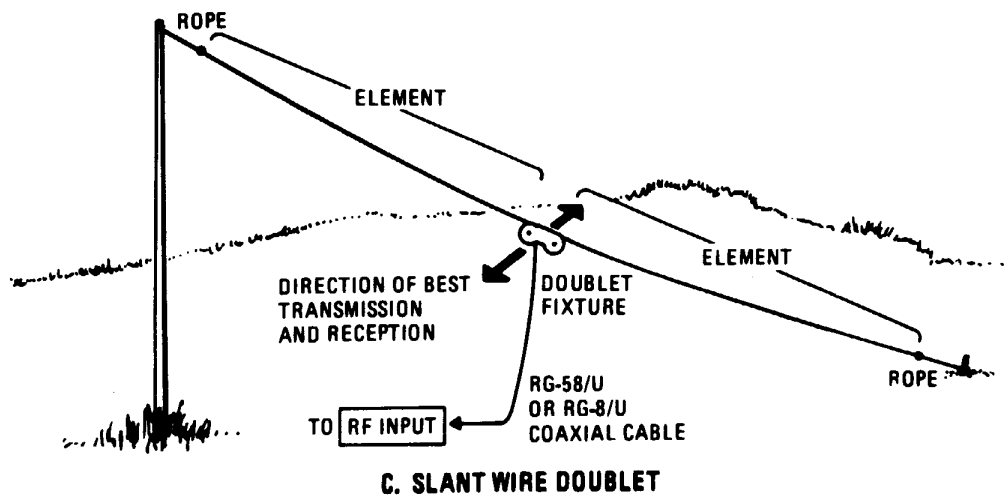
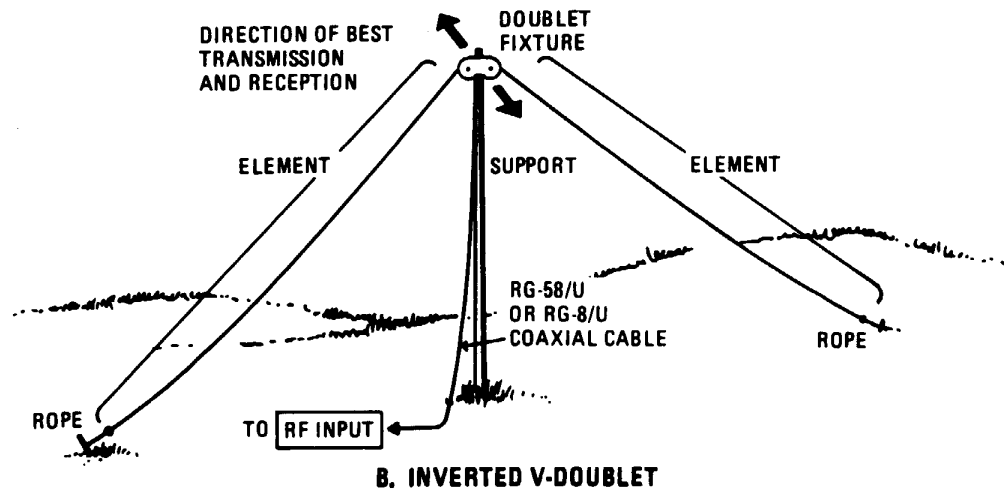
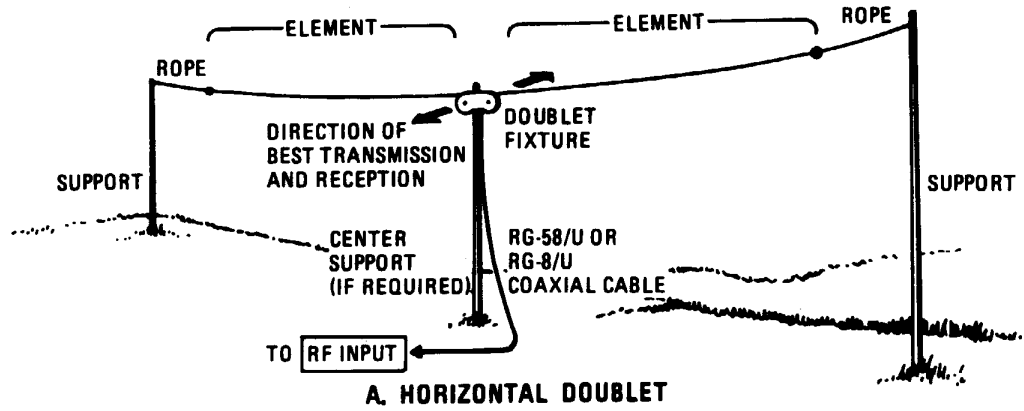
Do not short out the memory backup battery terminals. This could result in severe circuit damage.

#### 2.5.1 Connecting Memory Backup Battery

A ni-cad battery is used to keep the RAM memory alive when power is removed from the receiver. The backup battery is located on the A14 Control Board assembly. The backup battery jumper must be



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Figure 2-1. Typical Doublet Antenna Installation

inserted between E1 and E2 on the A14 Control Board assembly to activate the keep alive circuit. See subsection A14 for location of the assembly and the jumper.

### **2.5.2 Adjusting Front Panel Display Brightness**

Potentiometer R29 on Front Panel Driver Board assembly A13A2 is used to adjust the brightness of the vacuum fluorescent displays. R29 can be accessed by removing the top chassis cover or tilting the front panel assembly forward. R29 can be adjusted with a small screwdriver and is identified in subsection A13.

### **2.5.3 USB, LSB and Optional ISB Line Audio Output Level Adjust**

USB and LSB line audio output levels are adjustable from the front panel. Adjustment potentiometers are accessed through holes located next to the USB and LSB meter select pushbutton switches on the front panel.

Line audio output range is -16 to +10 dBm into 600 ohms.

## **2.6 POWER REQUIREMENTS**

The RF-590 requires 100, 120, 220, or 240 Vac, 47 to 420 Hz single phase power at 75 watts, nominally. Ac power selection is normally factory set to 120 Vac. To select a different range, first turn the front panel power switch off, then remove the ac power cord at the rear panel. Slide the plastic cover out of the way to expose the fuseholder and remove the fuse by pulling on the lever labeled FUSE PULL. Grasp the small PC card (located to the left of the fuseholder) with needlenose pliers and pull the card straight out. This card will be labeled with the numbers 100, 120, 220, and 240 Vac. For 220 V or 240 V operation, the fuse must be replaced with a 1.0 amp fuse (P/N F03-0002-019). Orient this card so that the desired range faces the fuseholder, and is the only number visible once the card has been reinserted. Reinsert the fuse and reconnect the power cord to the radio and the ac source. Turn the power on.

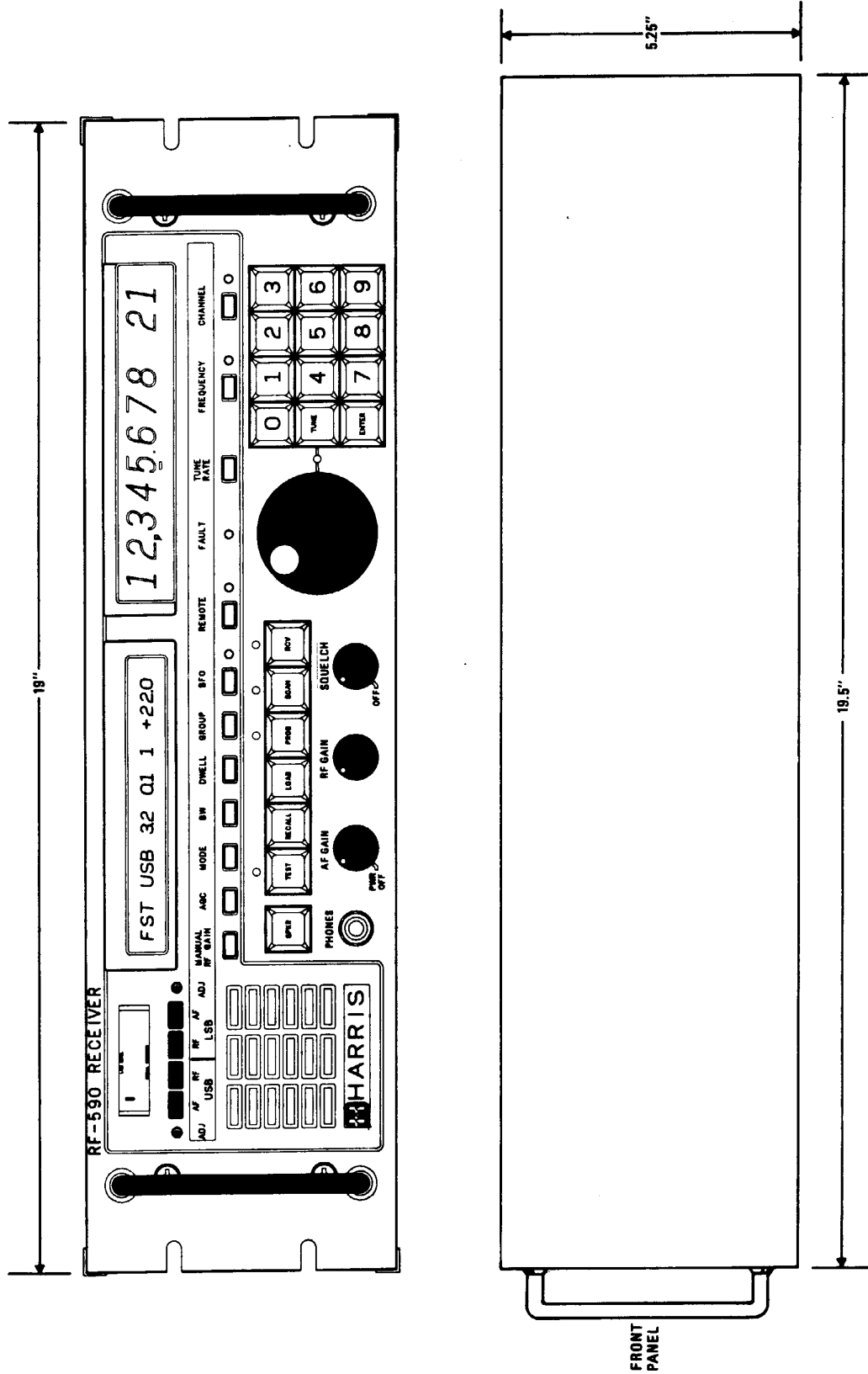
## **2.7 MECHANICAL INSTALLATION**

The RF-590 may be desk mounted (RF-594-02 option), see figure 2-2, stack mounted (RF-594-03 option) or rack mounted (RF-594-01 option) into a standard 19-inch equipment rack. See figure 2-3 for rack mounting information. Note that two different mounting brackets are supplied for rack mounting. PN 10073-1010 fits the left side of the RF-590 and PN 10073-1014 fits the right side. The detail drawing in figure 2-3 shows the left side bracket.

## **2.8 INPUT/OUTPUT CONNECTIONS**

The RF-590 is a complete receiver independent of all other equipment. It requires only the appropriate power and antenna connections. All other input/output connectors are used to expand and integrate features of the receiver or the system. RF-590 input and output connectors are shown and their uses explained in figure 2-4.

All RF type connectors are standard BNC, 50 ohm connections. Table 2-3 details the RF-590 local control functions available at TB1. Table 2-4 details the RF-590 local control functions available at J7. (Note that all of the TB1 inputs/outputs also appear at J7). Table 2-5 details the RF-590 remote control connectors J8 (RS-232) and J9 (RS-422).



590-2

Figure 2-2. RF-590 Desk Mount Dimensions

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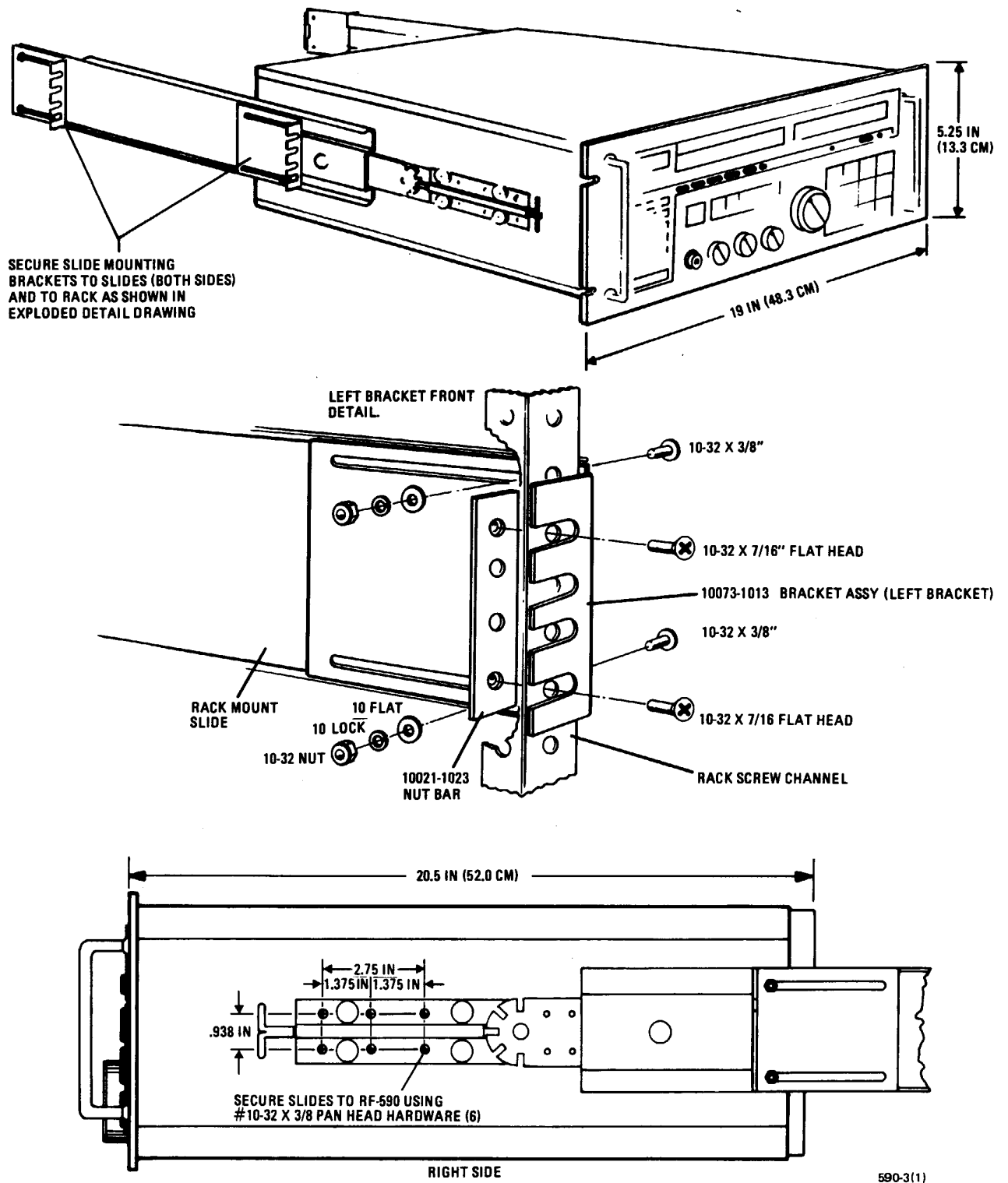


Figure 2-3. RF-590 Rack Mounting Details

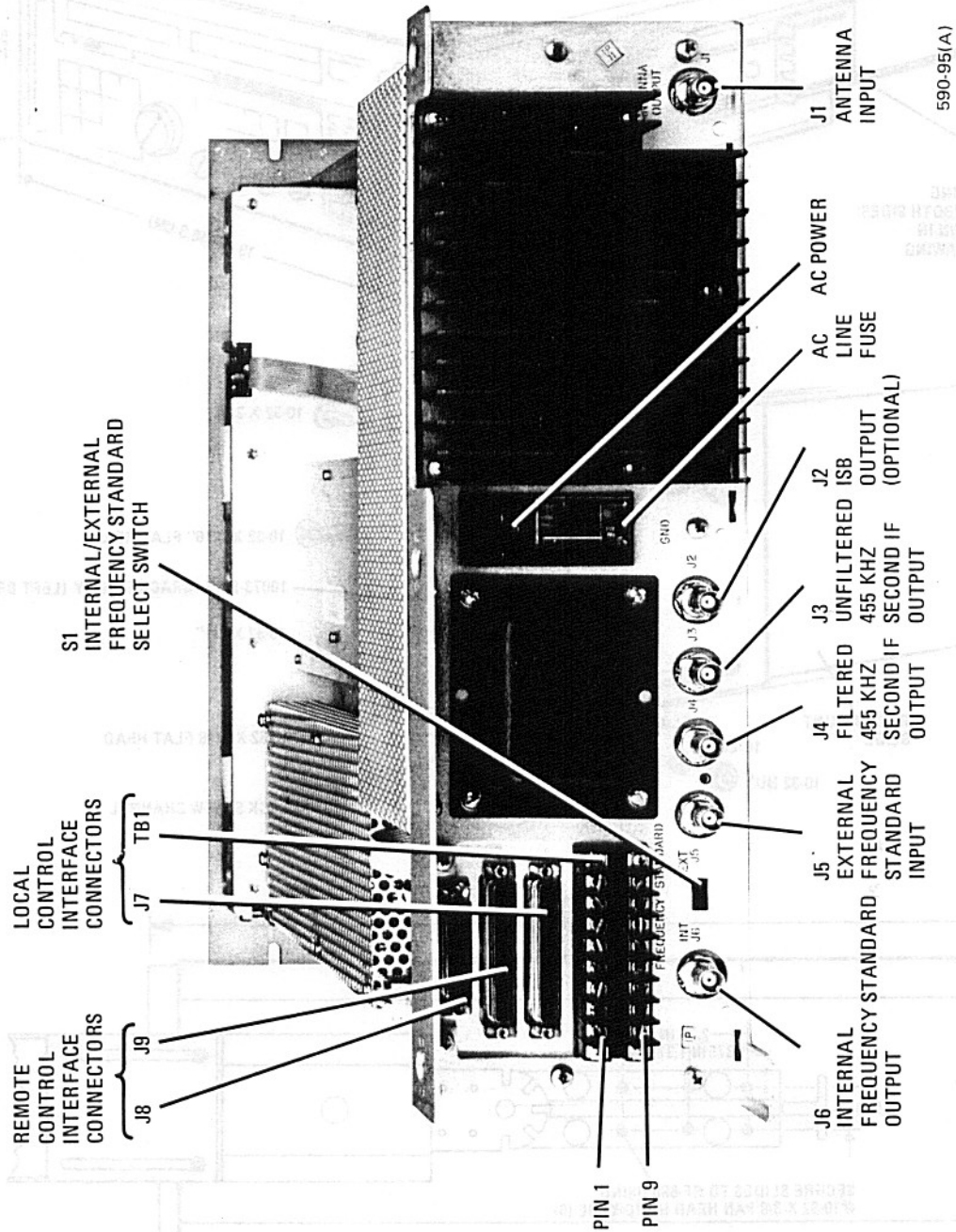


Figure 2-4. RF-590 Rear Panel

**Table 2-3. RF-590 Local Interface Terminal Board TB1**

Pin	Function
TB-1	GND
TB-2	USB AGC Dump
TB-3	USB AGC In
TB-4	Combined AGC
TB-5	ISB AGC Out
TB-6	ISB AGC Dump
TB-7	ISB AGC In
TB-8	Fault
TB-9	USB Line Audio
TB-10	USB Line Audio CT
TB-11	USB Line Audio
TB-12	USB AGC Out
TB-13	ISB Line Audio
TB-14	ISB Line Audio CT
TB-15	ISB Line Audio
TB-16	EXT Mute

**Table 2-4. RF-590 Local Control Interface Connector J7**

Connector and Pin	Function
J7-1	Remote Out 1
J7-2	GND
J7-3	Scan Step
J7-4	Remote Out 0
J7-5	Stop Scan
J7-6	Spare (To Control Board)
J7-7	Ext. Mute

**Table 2-4. RF-590 Local Control Interface Connector J7 (Cont.)**

Connector and Pin	Function
J7-8	ISB Line Audio
J7-9	ISB Line Audio CT
J7-10	ISB Line Audio
J7-11	USB AGC Out
J7-12	USB Line Audio
J7-13	USB Line Audio CT
J7-14	USB Line Audio
J7-15	Ext. Audio In
J7-16	Ext. Speaker GND
J7-17	Ext. Speaker Out
J7-18	Ext. Speaker Out
J7-19	Ext. Speaker GND
J7-20	Strobe 2
J7-21	Spare (To Control Board)
J7-22	Remote Out 2
J7-23	Strobe 1
J7-24	Clock
J7-25	Data
J7-26	Fault
J7-27	ISB AGC In
J7-28	ISB AGC Dump
J7-29	ISB AGC Out
J7-30	Combined AGC
J7-31	USB AGC In
J7-32	USB AGC Dump
J7-33	GND



**Table 2-4. RF-590 Local Control Interface Connector J7 (Cont.)**

Connector and Pin	Function
J7-34	Ext. Speaker GND
J7-35	Ext. Speaker Out
J7-36	Ext. Speaker Out
J7-37	Ext. Speaker GND

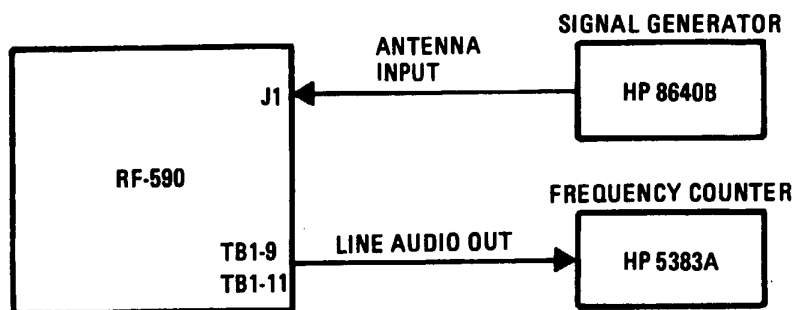
**Table 2-5. RF-590 Remote Control Interface Connectors J8 and J9**

Connector and Pin	Function
J8-1	Shield
J8-2	Tx Data 232/188C
J8-3	Rx Data 232/188C
J8-4	FSK Data Out -
J8-5	FSK Data In +
J8-6	ID0
J8-7	RS-232 Sig. GND
J8-8	ID1
J8-9	ID4
J8-10	Baud Rate 1
J8-11	Baud Rate 2
J8-12	N/C
J8-13	N/C
J8-14	Spare
J8-15	ID3
J8-16	ID2
J8-17	ID5
J8-18	ID6
J8-19	GND

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Table 2-5. RF-590 Remote Control Interface Connectors J8 and J9 (Cont.)

Connector and Pin	Function
J8-20	Spare
J8-21	Spare
J8-22	Baud Rate 3
J8-23	Baud Rate 0
J8-24	N/C
J8-25	N/C
J9-3	Bus Req.
J9-4	RS-422 Out +
J9-6	RS-422 In +
J9-19	GND
J9-20	RS-422 In -
J9-21	Bus Available
J9-37	RS-422 Out -
<b>NOTE</b>	
All other J9 pins are spares with no internal connections.	



590-5

Figure 2-5. RF-590 Functional Test Setup

## **2.9 RF-590 FUNCTIONAL CHECKOUT PROCEDURE**

The following is a local control functional test to determine the satisfactory operation of the RF-590. The following equipment (or equivalent) is required.

- HP-8640B Signal Generator
- HP-5383A Frequency Counter

The following paragraphs briefly describe RF-590 operation. The operator may find it useful to read section 3, Operation, prior to or concurrently with this procedure. Connect the above equipment as shown in figure 2-5.

### **2.9.1 Receive Mode Test**

Apply the ac power and check that the receiver (under test) powers up with RCV (Receive), FREQUENCY, and TUNE LEDs lit.

Set the receiver to the following initial conditions:

- Mode: USB
- RF Gain: Fully clockwise (cw)
- AGC: MED
- Speaker: On

Connect the signal generator to the receiver's antenna input and set the generator for a level of -24 dBm (14.1 mVrms).

#### **2.9.1.1 Frequency Entry**

Press the FREQUENCY button and enter a frequency of 12.345678 MHz via the keypad. Press ENTER. Set the signal generator to a frequency 1 kHz above the receiver tuned frequency (12.346678) and note the 1 kHz audible output tone. Connect the frequency counter to the line audio output and verify the audio frequency is 1 kHz.

#### **2.9.1.2 Tune Rate**

Press TUNE RATE successively until the cursor is beneath the 1 kHz digit. Rotate the Tuning knob and use the signal generator to verify a tune range of 100 kHz  $\pm$ 20 percent per revolution.

Press TUNE RATE to place the cursor beneath the 100 Hz digit and use the signal generator to verify a 10 kHz per revolution  $\pm$ 20 percent tune range.

Press TUNE RATE to place the cursor beneath the 10 Hz digit and use the signal generator to verify a 1 kHz per revolution  $\pm 20$  percent tune range.

### 2.9.1.3 Mode Selection

Press the MODE button under the alphanumeric display and check that USB, LSB, CW, AM, and FM are selectable as modes. Keeping the button pressed causes the display to scroll through the valid modes. Release the button and the receiver is placed into the selected mode.

### 2.9.1.4 Bandwidth Selection

Press the BW button under the alphanumeric display and check that the bandwidth display scrolls through the filter selections that are valid for the selected mode. (Note that filter bandwidths are customer specified, and will vary depending on the requirements. A typical filter complement for different modes is shown in table 2-6).

**Table 2-6. Typical Filter Complement**

Mode	Bandwidth
USB	2.8 kHz
LSB	2.8 kHz
CW	0.3 kHz
CW	1.0 kHz
AM	3.0 kHz
AM	6.8 kHz
AM	16.0 kHz
FM	16.0 kHz

### 2.9.1.5 AGC Selection

Press the AGC button beneath the alphanumeric display and check that the AGC speed selection scrolls from SLOW, MEDIUM, FAST, or DATA.

### 2.9.1.6 BFO Selection

Select the USB mode, and press the BFO button to enable BFO entries. Check that the BFO LED lights and that keypad selections (followed by pressing ENTER) cause the BFO offset frequency to appear in the BFO display field.

Check that the Tuning knob varies the BFO selection when the TUNE LED is lit.

With the signal generator set for a frequency of 12.346678 and the receiver set at 12.345678, USB mode, tune the BFO via the Tuning knob to -1 kHz and check that a zero beat is obtained.

Return the BFO frequency to 0.00 kHz.

**2.9.1.7 RF Gain**

Press the AGC ON/OFF button under the alphanumeric display to select AGC OFF. Check that the AGC display changes to OFF and that the RF GAIN knob adjusts the gain. Push RF meter button to ensure that reading increases.

**2.9.1.8 AF Gain**

Rotate the AF GAIN knob and check that the volume is adjustable.

**2.9.1.9 Channelized Reception**

**NOTE**

Proceed to paragraph 2.9.2.1, Load Memory Function, and perform the steps listed there. Return to 2.9.1.9 after the four channels have been programmed.

With the receiver in the Receive mode (RCV LED lit), press the CHANNEL button. (CHANNEL LED should light.) Select each channel number (followed by ENTER) listed in table 2-7. Check that the receiver front panel updates to number listed. Using the signal generator, check that the receiver has in fact tuned to the frequency listed.

**Table 2-7. Programmed Channels**

Channel	Frequency MHz	AGC	Mode	Bandwidth kHz
01	01.111111	SLO	USB	2.8
02	02.222222	MED	LSB	2.8
03	03.333333	FST	CW	1.0
04	04.444444	MED	CW	1.0

With the TUNE and CHANNEL LEDs lit, rotate the Tuning knob. Check that channels 1-4 are selected.

**2.9.1.10 Speaker On/Off**

Check that the SPKR (SPEAKER ON/OFF) button alternately enables and disables the speaker.

### 2.9.1.11 Local/Remote Switch

The following test applies only if the remote option is installed in the receiver. If not, the REMOTE button will have no effect. With the receiver under local control, press the REMOTE button and check that the REMOTE LED lights and that it is no longer possible to change receiver parameters via the front panel. Make sure that by pressing the REMOTE button a second time, the receiver is placed back under local control.

### 2.9.1.12 Meter Switch

Set the receiver in the following conditions:

Frequency:	12.345678 MHz
Mode:	USB
AGC:	MED
RF Gain:	Fully clockwise (cw)
AF Gain:	As desired

Set the signal generator to a frequency of 12.346678 MHz and a level of -24 dBm (14.1 mVrms).

Press the USB/RF pushbutton under the meter. The meter indication should be approximately 14 mVrms.

Press the USB/AF pushbutton under the meter. The meter indication should be approximately 0 dBm.

Note that in the standard receiver, LSB and USB signals will be routed through the USB switch positions, and the ISB-LSB switch position will be inactive. If the ISB option has been installed, the USB positions select USB information and the ISB-LSB positions select LSB information.

### 2.9.1.13 Squelch Control

Set receiver as in paragraph 2.9.1.12. Verify receiver squelch action as the squelch control is varied. A reduction in speaker audio output should be noted.

## 2.9.2 Program Mode

### 2.9.2.1 Load Memory Function

The channel programming memory allows up to 100 channels to be stored. Press the PROGRAM button to place the receiver in the Program mode, and check that the PROGRAM and CHANNEL LEDs light. Perform the following steps:

- a. Enter 01 via the keyboard.

- b. Press FREQUENCY and enter 01.111111 MHz via the keyboard. Press ENTER.
- c. Select AGC-SLO, MODE-USB.
- d. Press LOAD.
- e. Press CHANNEL and enter 02 via the keyboard.
- f. Press FREQUENCY and enter 02.222222 MHz via the keyboard. Press ENTER.
- g. Select AGC-MED, MODE-LSB.
- h. Press LOAD.
- i. Press CHANNEL and enter 03.
- j. Push FREQUENCY and enter 03.333333 MHz. Press ENTER.
- k. Select AGC-FAST, MODE-CW, BW-1.0 kHz.
- l. Press LOAD.
- m. Press CHANNEL and enter 04.
- n. Press FREQUENCY and enter 04.444444 MHz. Press ENTER.
- o. Select AGC-MED, MODE-CW, BW-1.0 kHz.
- p. Press LOAD.
- q. Press RECEIVE to leave the Program mode.

Perform the steps in paragraph 2.9.1.9, Channelized Reception, to check that the channels were in fact programmed.

### **2.9.2.2** Recall Memory Function

Place the receiver in the Program mode. Enter 02 via the keyboard and press RECALL. The display should update to 02.222222 MHz, CHANNEL-02, AGC-MED, MODE-LSB.

### **2.9.2.3** Program Group Function

Group programming of channels allows the preprogramming of up to 10 channel groups (20 channels per group maximum). Channels may be programmed in any order and any channel can appear in more than one group.

To program a group, place the receiver in the Program mode and perform the following steps:

- a. Press GROUP.
- b. Enter 1 digit via the keyboard in response to the prompt GROUP NUMBER?. Press ENTER.
- c. Enter 03 via the keyboard in response to the prompt CHANNEL NUMBER?, and press ENTER and LOAD. The display will respond with 03 OK.
- d. Enter 02, followed by ENTER and LOAD.
- e. Enter 01, followed by ENTER and LOAD.
- f. Exit programming by pushing RECEIVE.
- g. Proceed to 2.9.3. Verification of Group programming will be done during the Group scan test.

### 2.9.3 Scan Mode Test

The following two scan modes are available on the RF-590.

- Channel scan
- Group scan

Channel scan allows the automatic sequential scanning of up to 100 preprogrammed channels. Group scan allows scanning of up to ten groups (20 channels per group, maximum). Follow the steps in paragraph 2.9.3.1 to perform a Channel scan and the steps in 2.9.3.2 to perform a Group scan.

#### 2.9.3.1 Channel Scan

- a. With the receiver in RECEIVE MODE, press SCAN. SCAN LED should light.
- b. Press CHANNEL in response to GROUP or CHANNEL SCAN?.
- c. Enter 01 followed by ENTER in response to FIRST CHANNEL?.
- d. Enter 04 followed by ENTER in response to LAST CHANNEL?. The receiver should commence to automatically scan channels 1-4. Press SCAN; verify that the scanning stops. Verify that pressing SCAN again restarts scanning. Verify that pushing the DWELL button affects the dwell speed accordingly.



**2.9.3.2** Group Scan

- a. Push the RECEIVE button, then SCAN.
- b. Press GROUP in response to the GROUP or CHANNEL SCAN? prompt.
- c. Enter 1 digit via the keyboard, then ENTER. The receiver should now scan channels 3, 2, 1 in that order.

**2.9.4** Self-Test (BITE)

Press the TEST button to begin the receiver's self-diagnostics. The receiver will perform an automatic self-test, approximately 5 seconds in length. During this time, all front panel display segments and LEDs should light, and stay lit until the message — — — TEST PASSED — — — appears in the left hand display.

In the event of a failure, a receiver fault code will be displayed. If this occurs, consult the maintenance section of this manual, table 5-1, which lists the fault codes by assembly number.

## SECTION 3

### OPERATION

#### 3.1 INTRODUCTION

This section completely covers all operational aspects of the RF-590. All operational controls and procedures are detailed and explained. Section 2 (Installation) and 5 (Maintenance) are referenced in this section regarding I/O connections and BITE TEST failure codes.

#### 3.2 OPERATIONAL CONTROLS AND I/O CONNECTIONS

All operating controls are located on the RF-590 front panel, as shown and described in figure 3-1. Detailed operational procedures for front panel control are given in paragraphs 3.6 through 3.9.

All interfacing connections are located on the RF-590 rear panel (except for headphones). Rear panel connector locations are shown in figure 2-4, and connector pinouts are listed in tables 2-3, 2-4, and 2-5.

#### 3.3 POWER UP DEFAULT CONDITIONS

Radio power up always places the receiver in the Receive mode of operation that existed at power off, either Local or Remote. (If no Remote option has been installed, the receiver will always power up in the Local Receive mode.) The display will show the last frequency, AGC, bandwidth, etc. that was in use by the receiver at power off.

#### 3.4 LOCAL/REMOTE SELECTION

Local/Remote selection is accomplished with a single alternate action pushbutton. If the LED indicator is off, depressing the Remote button will place the receiver in the Remote mode, assuming that the Remote option is installed.

#### 3.5 TEST FUNCTION

The Test function is entered by pressing the TEST button on the receiver front panel. The receiver immediately enters a self-test mode and performs the following checks.

- Processor EPROM validity
- Processor RAM memory validity
- Synthesizer lock tests
- RF signal path checks

- IF signal path checks
- Remote option tests (if installed)

When the tests are complete the alphanumeric display is used to inform the operator of test results by displaying the failed module code number or the message TEST PASSED.

A complete table of failed module code numbers, as well as a comprehensive description of this Built In Test Equipment (BITE) may be found in the maintenance section of this manual.

### **3.6 OPERATIONAL MODES**

The RF-590 Receiver can be selected to function in four basic ways:

- Receive
- Scan
- Program
- Test

#### **3.6.1 Receive Function**

The Receive function is entered by pressing the RECEIVE button on the receiver front panel. The receiver will tune to the parameters that were used in the previous Receive function, and will show those parameters on the front panel display. The Receive LED will also light. The radio is now under manual control and the following conditions apply.

##### **3.6.1.1 Frequency Entry**

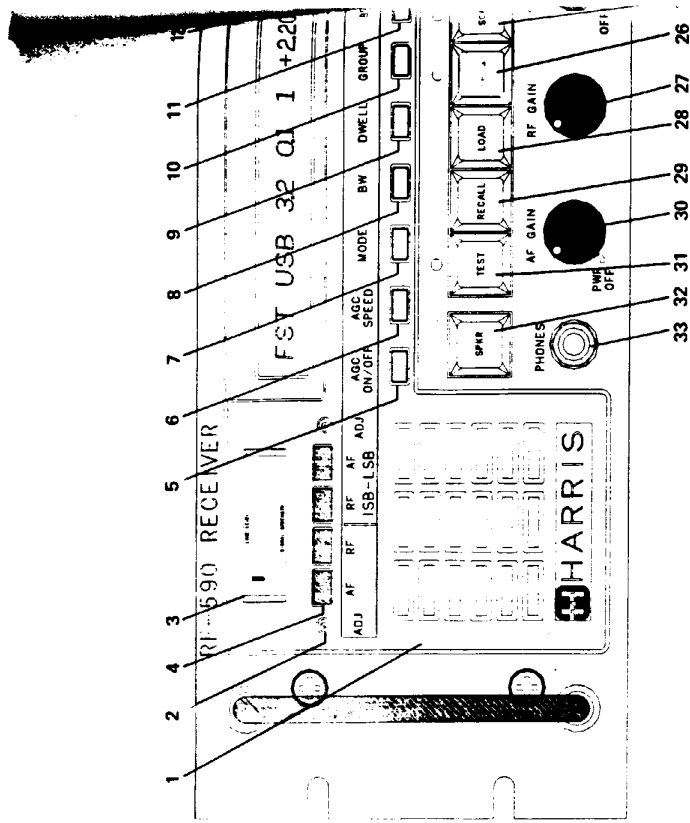
###### **3.6.1.1.1 Entering a Complete Frequency**

Pressing the FREQUENCY button causes subsequent digit entries to begin at the 10 MHz position and proceed to the right as the frequency is entered. All changed digits are dimmed to half brilliance. Pressing the ENTER button causes the receiver to tune to the new frequency and the digits are returned to full brilliance. In general, if the FREQUENCY button is pressed before keypad entries, the digits start in the 10 MHz position. If the FREQUENCY button is not pressed before keypad entries, then the digits are entered starting at the position of the cursor (underline).

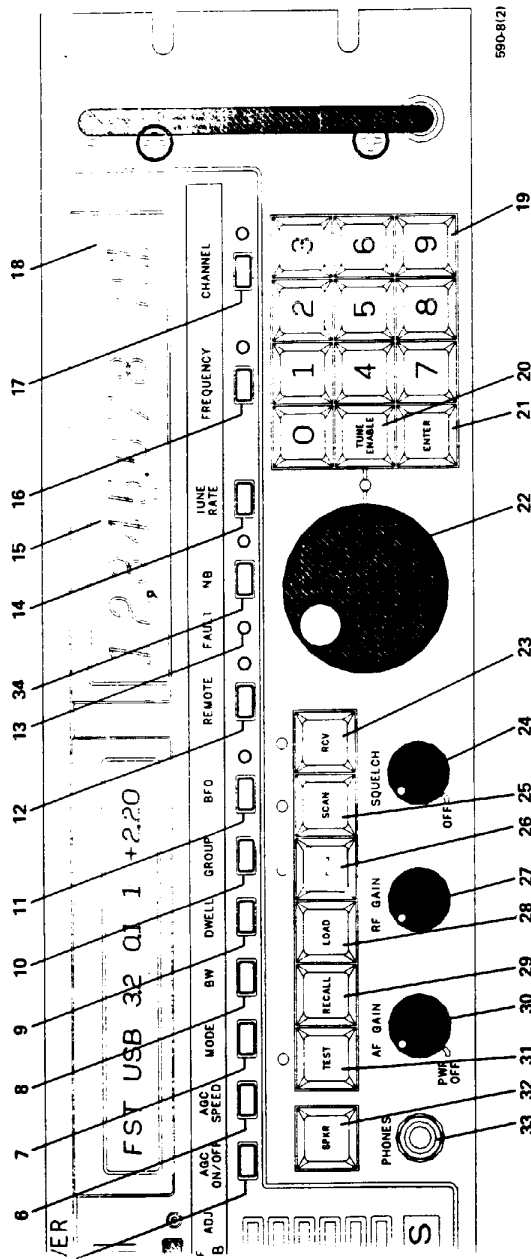
METER PUSHBUTTON FUNCTION TABLE

	SPEAKER OUTPUT	METER FUNCTION
AF	MONITORS: AF IN ALL MODES EXCEPT 2-ISB (USB, WHEN IN 2-ISB MODE)	INDICATES: USB LINE AUDIO LEVEL
RF	MONITORS: AF IN ALL MODES EXCEPT 2-ISB (USB, WHEN IN 2-ISB MODE)	INDICATES: RF LEVEL (OF USB ONLY WHEN IN 2-ISB MODE)
ISB-LSB RF	MONITORS: LSB AF WHEN IN 2-ISB MODE	INDICATES: RF LEVEL OF LSB CHANNEL (WHEN IN 2-ISB)
ISB-LSB AF	MONITORS: LSB AF WHEN IN 2-ISB MODE	INDICATES: LSB LINE AUDIO LEVEL (WHEN IN 2-ISB)

NOTE: THE ISB-LSB RF AND ISB-LSB AF BUTTONS FUNCTION ONLY WHEN RF-590 IS IN 2-ISB MODE. (OPTIONAL)



1. LOUSPEAKER
2. LINE LEVEL ADJUST  
SEPARATE SCREWDRIVER ADJUSTMENTS ALLOW ADJUSTMENT OF USB AND LSB LINE LEVELS.
3. METER  
DISPLAYS RF SIGNAL STRENGTH (MICROVOLTS OR MILLIVOLTS RMS) OR LINE AUDIO OUTPUT LEVEL (DBM/600 OHMS).
4. METER SELECT SWITCHES  
SELECTS AF-USB, RF-USB, AF-LSB, OR RF-LSB FOR METER DISPLAY. ALSO SELECTS USB OR LSB AUDIO (WHEN USB OPERATION IS USED) TO SPEAKER AND HEADPHONES. (SEE ABOVE: METER PUSHBUTTON FUNCTION TABLE.)
5. MANUAL RF GAIN PUSHBUTTON  
SELECTS AGC ON OR OFF.
6. AGC PUSHBUTTON AND DISPLAY  
SWITCHES THROUGH AGC TIME CONSTANTS SINGLE STEP, OR SCROLLS WHEN HELD DOWN.
7. MODE PUSHBUTTON AND DISPLAY  
SWITCHES THROUGH AVAILABLE MODES (AM, FM, CW, LSB, OR USB) SINGLE STEP, OR SCROLLS THEM WHEN HELD DOWN. ALSO CAUSES AUTOMATIC RESELECTION OF IF BANDWIDTH WHEN NECESSARY.
8. BANDWIDTH PUSHBUTTON AND DISPLAY  
SINGLE STEP OR SCROLLS THROUGH IF FILTER BANDWIDTHS AVAILABLE IN THE SELECTED MODE. THE DISPLAY SHOWS BANDWIDTH IN KHZ.
9. DWELL PUSHBUTTON AND DISPLAY  
SINGLE STEP OR SCROLLS THROUGH DWELL TIMES AVAILABLE IN SCAN MODE. DISPLAY SHOWS DWELL TIME IN SECONDS.
10. GROUP PUSHBUTTON AND DISPLAY  
PUSHBUTTON IS USED TO SELECT OR PROGRAM ONE OF TEN GROUPS OF CHANNELS WHILE SCANNING. DISPLAY SHOWS GROUP NUMBER.
11. BFO PUSHBUTTON, DISPLAY, AND INDICATOR  
PUSHBUTTON ALLOWS ENTRY OF BFO FREQUENCY IN 10 HZ STEPS WITH EITHER THE MAIN TUNING KNOB OR KEY PAD. BFO SIGN IS CHANGED BY RE-PRESSING BFO BUTTON. LED TO THE RIGHT OF THE PUSHBUTTON INDICATES WHEN BFO ADJUSTMENTS ARE ENABLED.
12. REMOTE PUSHBUTTON AND INDICATOR  
ALLOWS SELECTION OF REMOTE OR LOCAL CONTROL. LED ILLUMINATES IN REMOTE MODE.
13. FAULT INDICATOR  
INDICATES SYNTHESIZER OUT OF LOCK, POWER SUPPLY FAULT, RF INPUT OVERLOAD OR BITE TEST FAILURE.
14. TUNE RATE PUSHBUTTON  
SINGLE STEP OR SCROLLS THE CURSOR (UNDERLINE) POSITION FOR FREQUENCY TUNING.
15. FREQUENCY DISPLAY  
DISPLAYS FREQUENCY BEING USED, PROGRAMMED, OR SCANNED.
16. FREQUENCY PUSHBUTTON AND INDICATOR  
PLACES RECEIVER IN FREQUENCY MODE. FREQUENCY AND OTHER OPERATING PARAMETERS ARE ENTERED DIRECTLY, USING EITHER THE KEY PAD OR TUNING KNOB. LED INDICATES WHEN IN FREQUENCY MODE.
17. CHANNEL PUSHBUTTON AND INDICATOR  
PLACES RECEIVER IN CHANNEL MODE. FREQUENCY AND OPERATING PARAMETERS MAY BE PREPROGRAMMED FOR 100 CHANNELS. CHANNEL IS SELECTED EITHER BY KEY PAD OR TUNING KNOB. LED INDICATES WHEN IN CHANNEL MODE.
18. CHANNEL  
DISPLAYS CHANNEL PROGRAMMED, OR CHANNEL NUMBER.
19. NUMERIC  
USED FOR NUMERIC SET, OR CHANNEL SET, OR CHANNEL.
20. TUNE PUS  
ENABLES TUNING FREQUENCY OF TUNING KNOB IS ENABLED.
21. ENTER PUS  
INITIATES EXECUTE BFO OFFSET.
22. TUNING K  
WHEN ENABLED, INDICATES CHANNEL QUENCY, CHANNEL.



- 32. **RATE PUSHDOWN**  
OR SCROLLS THE CURSOR UNDER-  
ON FOR FREQUENCY TUNING.
- 33. **PHONES**  
USE OF HEADPHONES AUTOMATICALLY DISABLES  
LOUDSPEAKER.
- 34. **NOISE BLANKER (NB) (OPTIONAL)**  
SELECTS NOISE BLANKER OPERATION.
- 31. **ENTER PUSHDOWN**  
INITIATES EXECUTION OF FREQUENCY, CHANNEL, OR  
BFO OFFSET.
- 30. **AF GAIN**  
ADJUSTS THRESHOLD FOR VOICE ACTIVATED SQUELCH  
(CW, SB, OR AM) OR CARRIER ACTIVATED SQUELCH  
(FM).
- 29. **RECALL PUSHDOWN**  
ALLOWS INSTANT RECALL OF PARAMETERS IN  
THE AUXILIARY (MOST-USED) CHANNEL.
- 28. **RF GAIN**  
ADJUSTS THRESHOLD FOR VOICE ACTIVATED SQUELCH  
(CW, SB, OR AM) OR CARRIER ACTIVATED SQUELCH  
(FM).
- 27. **RF GAIN CONTROL**  
ALLOWS MANUAL CONTROL OF RF GAIN.
- 26. **PROGRAM (PROG) PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN TEST MODE IN WHICH  
RECEIVER COMPLETES A COMPREHENSIVE SERIES  
OF TESTS. RESULTS APPEAR ON ALPHANUMERIC  
DISPLAY. INDICATOR ILLUMINATES DURING TEST.
- 25. **SCAN PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN SCAN MODE IN WHICH CHANNELS  
ARE SCANNED IN EITHER CHANNEL OR GROUP MODE.  
DWELL TIME IS ADJUSTABLE.
- 24. **SQUELCH CONTROL**  
ADJUSTS THRESHOLD FOR VOICE ACTIVATED SQUELCH  
(CW, SB, OR AM) OR CARRIER ACTIVATED SQUELCH  
(FM).
- 23. **RECEIVE (RCV) PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN THE RECEIVE MODE. ALL  
FUNCTIONS ARE CONTROLLED EITHER DIRECTLY OR BY  
INFORMATION PREPROGRAMMED FOR CHANNELS.  
INDICATOR ILLUMINATES WHEN IN THE RECEIVE MODE.
- 22. **TUNE PUSHDOWN AND INDICATOR**  
ENABLES TUNING KNOB FOR SELECTION OF CHANNEL,  
FREQUENCY, OR BFO OFFSET. LED INDICATES WHEN  
KNOB IS ENABLED.
- 21. **ENTER PUSHDOWN**  
INITIATES EXECUTION OF FREQUENCY, CHANNEL, OR  
BFO OFFSET.
- 20. **TUNE PUSHDOWN AND INDICATOR**  
ENABLES TUNING KNOB FOR SELECTION OF CHANNEL,  
FREQUENCY, OR BFO OFFSET. LED INDICATES WHEN  
KNOB IS ENABLED.
- 19. **NUMERIC KEY PAD**  
USED FOR NUMERIC ENTRY OF FREQUENCY, BFO OFF-  
SET, OR CHANNEL.
- 18. **CHANNEL DISPLAY**  
DISPLAYS CHANNEL NUMBER BEING USED, PRO-  
GRAMMED, OR SCANNED.
- 17. **RECEIVE (RCV) PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN THE RECEIVE MODE. ALL  
FUNCTIONS ARE CONTROLLED EITHER DIRECTLY OR BY  
INFORMATION PREPROGRAMMED FOR CHANNELS.  
INDICATOR ILLUMINATES WHEN IN THE RECEIVE MODE.
- 16. **SQUELCH CONTROL**  
ADJUSTS THRESHOLD FOR VOICE ACTIVATED SQUELCH  
(CW, SB, OR AM) OR CARRIER ACTIVATED SQUELCH  
(FM).
- 15. **SCAN PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN SCAN MODE IN WHICH CHANNELS  
ARE SCANNED IN EITHER CHANNEL OR GROUP MODE.  
DWELL TIME IS ADJUSTABLE.
- 14. **PROGRAM (PROG) PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN TEST MODE IN WHICH  
RECEIVER COMPLETES A COMPREHENSIVE SERIES  
OF TESTS. RESULTS APPEAR ON ALPHANUMERIC  
DISPLAY. INDICATOR ILLUMINATES DURING TEST.
- 13. **ENTER PUSHDOWN**  
INITIATES EXECUTION OF FREQUENCY, CHANNEL, OR  
BFO OFFSET.
- 12. **TUNE PUSHDOWN AND INDICATOR**  
ENABLES TUNING KNOB FOR SELECTION OF CHANNEL,  
FREQUENCY, OR BFO OFFSET. LED INDICATES WHEN  
KNOB IS ENABLED.
- 11. **NUMERIC KEY PAD**  
USED FOR NUMERIC ENTRY OF FREQUENCY, BFO OFF-  
SET, OR CHANNEL.
- 10. **CHANNEL DISPLAY**  
DISPLAYS CHANNEL NUMBER BEING USED, PRO-  
GRAMMED, OR SCANNED.
- 9. **RECEIVE (RCV) PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN THE RECEIVE MODE. ALL  
FUNCTIONS ARE CONTROLLED EITHER DIRECTLY OR BY  
INFORMATION PREPROGRAMMED FOR CHANNELS.  
INDICATOR ILLUMINATES WHEN IN THE RECEIVE MODE.
- 8. **SQUELCH CONTROL**  
ADJUSTS THRESHOLD FOR VOICE ACTIVATED SQUELCH  
(CW, SB, OR AM) OR CARRIER ACTIVATED SQUELCH  
(FM).
- 7. **SCAN PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN SCAN MODE IN WHICH CHANNELS  
ARE SCANNED IN EITHER CHANNEL OR GROUP MODE.  
DWELL TIME IS ADJUSTABLE.
- 6. **PROGRAM (PROG) PUSHDOWN AND INDICATOR**  
PLACES RECEIVER IN TEST MODE IN WHICH  
RECEIVER COMPLETES A COMPREHENSIVE SERIES  
OF TESTS. RESULTS APPEAR ON ALPHANUMERIC  
DISPLAY. INDICATOR ILLUMINATES DURING TEST.
- 5. **ENTER PUSHDOWN**  
INITIATES EXECUTION OF FREQUENCY, CHANNEL, OR  
BFO OFFSET.
- 4. **TUNE PUSHDOWN AND INDICATOR**  
ENABLES TUNING KNOB FOR SELECTION OF CHANNEL,  
FREQUENCY, OR BFO OFFSET. LED INDICATES WHEN  
KNOB IS ENABLED.
- 3. **NUMERIC KEY PAD**  
USED FOR NUMERIC ENTRY OF FREQUENCY, BFO OFF-  
SET, OR CHANNEL.
- 2. **CHANNEL DISPLAY**  
DISPLAYS CHANNEL NUMBER BEING USED, PRO-  
GRAMMED, OR SCANNED.
- 1. **RATE PUSHDOWN**  
OR SCROLLS THE CURSOR UNDER-  
ON FOR FREQUENCY TUNING.
- 0. **PHONES**  
USE OF HEADPHONES AUTOMATICALLY DISABLES  
LOUDSPEAKER.
- 32. **SPEAKER (SPKR) PUSHDOWN**  
ALTERNATE ACTION ENABLES AND DISABLES  
LOUDSPEAKER.
- 33. **HEADPHONE (PHONES) JACK**  
USE OF HEADPHONES AUTOMATICALLY DISABLES  
LOUDSPEAKER.
- 34. **NOISE BLANKER (NB) (OPTIONAL)**  
SELECTS NOISE BLANKER OPERATION.

Figure 3-1. RF-590 Front Panel Control

### **3.6.1.1.2** Tune Rate Cursor Movements

Pressing the TUNE RATE button causes the cursor to move one place to the right. When held down, the cursor moves to the right at one step each half second. Release the button and the movement stops. If the cursor goes off the end it reappears in the most significant position. Note that the cursor does not move with digit entries. Only the TUNE RATE button changes the cursor position. The cursor may be considered as a starting point for frequency entries.

### **3.6.1.1.3** TUNE Knob Operation

If the LED adjacent to the TUNE knob is not lit, press TUNE, which will enable the TUNE knob and light the LED. The knob is now used to select the digits at and to the left of the cursor. The frequency tuning stops at minimum and maximum frequencies and will not roll around to the opposite end of the range (e.g., it stays at 29.999999 despite efforts to increase it). Press TUNE a second time and the tune LED goes off and further rotation has no effect (Tune knob disabled).

#### **NOTE**

The tune knob rate is fixed at 100 changes per revolution for frequency and 25 per revolution for channels.  
The knob cannot be used in the 10 MHz position.

### **3.6.1.1.4** Partial Frequency Entry

Partial frequency entries simply start at the cursor position and enter to the right when keyed entry is used. Selected digits are dimmed to half brilliance until the ENTER button is pressed. Note again that the cursor position does not move, so multiple entries can be made from the same starting point. It is therefore easy to change from 17.2053 to 17.2018 and back to 17.2053 again.

Pressing the FREQUENCY button will clear any pending (dimmed) digits entered in error, and restore the cursor to the 10 MHz position.

## **3.6.1.2** Channel Entry

### **3.6.1.2.1** Entering a New Channel

Pressing the CHANNEL button causes the CHANNEL LED to light indicating channelized operation. Digits are entered first in the tens position, then in the ones position. Digits selected are dimmed to half brilliance until the ENTER button is pushed, at which time the receiver tunes to the new channel and the digits return to full brilliance.

### **3.6.1.2.2** Tune Knob Operation in Channel Entry

To operate the TUNE knob in the channel field, press CHANNEL and then activate the TUNE knob. (CHANNEL and TUNE LEDs will light.) Rotation of the TUNE knob will cause the receiver to automatically select a new operating channel.

### **3.6.1.3** BFO Entry

The BFO offset range is -9.99 kHz to +9.99 kHz. Pressing the BFO button causes subsequent keypad or tune knob entries to be made in the BFO section of the alphanumeric display. Keypad BFO entries are still terminated by the ENTER button. Enable the TUNE knob to allow BFO change by knob rotation. The knob selects up to +9.99 and stops or down to -9.99 and stops. There is no roll around in the tune knob function. The cursor is not relevant in BFO operation. The plus (+) or minus (-) sign is changed by alternate presses of the BFO button when BFO operation has been selected.

### **3.6.1.4** Automatic Gain Control (AGC) and RF GAIN Control

Two basic modes of RF gain control are possible:

- Automatic Gain Control (AGC) – with selectable time constants.
- Manual RF Gain – variable using the front panel RF GAIN Control.

Additionally, there are four choices for AGC speed.

#### **3.6.1.4.1** AGC Time Constant Selection

The AGC ON/OFF pushbutton turns the AGC ON or OFF. When turned on, the last used AGC speed is enabled until changed.

Automatic Gain Control (AGC) time constant selection is accomplished by the AGC button. Pressing this button will scroll the AGC portion of the alphanumeric display through the possible AGC speeds: slow, medium, fast, and data. Releasing the button causes the receiver to operate using the selected AGC speed.

#### **3.6.1.4.2** Manual GAIN Control

The RF GAIN control is always active and may override the AGC if so desired. It provides up to approximately 125 dB of gain reduction.

### **3.6.1.5** Demodulation Mode Selection

Pressing and holding down the MODE button causes the receiver to scroll through the available modes (AM, CW, LSB, USB, or FM) in the alphanumeric display. While the modes are scrolling they are displayed

at half brilliance. Release of the button causes the receiver to operate in the selected mode and the display returns to full brilliance. When the mode change has been completed the BW display changes to the bandwidth that was last used for that mode.

#### **3.6.1.6 Bandwidth Selection**

Pressing and holding the BW button causes the receiver to scroll through the bandwidth selections that are available and valid for the selected mode. Release of the button causes the receiver to switch to the selected bandwidth. Bandwidths used are normally customer specified, and usually only CW or AM will have more than one filter.

#### **NOTE**

After any Receive function parameter (MODE, BW, AGC, BFO, or FREQUENCY) is changed by release of a scrolling button, depression of ENTER or rotation of the TUNE knob, the new RECEIVE set up is stored and would be reused upon later entry into the Receive function from some other function, such as SCAN. Note that such a parameter change will also cause the previously displayed CHANNEL number to be blanked, since the new setups no longer correspond to that channel's setup parameters.

#### **3.6.1.7 Meter Monitoring Selection**

A meter on the front panel of the RF-590 monitors the RF and AF signal levels. Pushbutton switches allow the operator to monitor the LSB (in the ISB mode) RF signal strength, USB RF signal strength, USB line audio output level, and LSB (in the ISB mode) line audio output level. The meter scale is calibrated in  $\mu\text{Vrms}$  or  $\text{mVrms}$  for RF signals (1  $\mu\text{V}$  to 100  $\text{mV}$ ) and  $\text{dBm}$  for AF signals (-15  $\text{dBm}$  to +10  $\text{dBm}$ , +4  $\text{dBm}$  center scale). In ISB mode, the meter switches also select USB or LSB input to loudspeaker and headphones.

#### **3.6.1.8 Audio Output Selection and Control**

The RF-590 provides the four following audio output sources:

- Internal Speaker
- Headphone
- External Speaker
- Line Audio



#### **3.6.1.8.1 Internal Speaker and Headphone Output**

A front panel speaker capable of delivering 2.0 watts of audio power is provided in the RF-590. A front panel 600 ohm Headphone Output jack compatible with a PL-55 type connector is also provided.

The AF GAIN Control adjusts the speaker and headphone volume level. This control has no effect upon the Line Audio Output.

Use of the headphone jack automatically disables the speaker. Speaker disabling is also provided by the speaker ON/OFF switch.

#### **3.6.1.8.2 External Speaker Output**

A rear panel output (listed in table 2-3) allows connection of an external 8 ohm speaker. This external speaker is controlled in the same manner as the internal speaker (paragraph 3.6.1.8.1), and will deliver 2.0 watts of audio power.

#### **3.6.1.8.3 Line Audio Outputs**

The 600 ohm line audio outputs for USB and ISB (LSB) audio signals are provided on the RF-590 rear panel (listed in tables 2-3 and 2-4). All outputs are balanced, with an ungrounded center tap.

Line audio output levels are continuously variable via front panel screwdriver adjustments. Either output (USB or ISB) is independently adjustable from -16 dBm to +10 dBm (600 ohm). Line audio level monitoring is provided by a front panel meter and meter select switches (see paragraph 3.6.1.7 and figure 3-1).

#### **3.6.1.9 Squelch Control**

Front panel SQUELCH control adjusts a threshold for carrier activated squelch (FM mode) or voice activated squelch (all other modes). The SQUELCH control is continuously variable.

### **3.7 PROGRAM FUNCTION**

The RF-590 program function allows an operator to store up to 100 channels of frequency, modulation mode, filter bandwidth, AGC mode, and BFO offset.

#### **3.7.1 Programming Channels**

The program function is entered by pushing the PROGRAM button on the receiver front panel. The CHANNEL LED will light, indicating that the receiver is set up to accept channel programming. To program channels in the RF-590, proceed with the following steps.

- a. Select the desired two digit channel number.
- b. Press the FREQUENCY pushbutton, and enter the desired frequency. (Note that for both steps a and b, the digits will dim to half brilliance once entered.)
- c. Press ENTER. (Digits will return to full brilliance.)
- d. Select desired AGC speed, modulation mode, filter bandwidth, and/or BFO offset. (Only BFO offset entry must be terminated by ENTER button.)
- e. Press LOAD button once all parameters (steps a through d) have been selected.
- f. Push CHANNEL button and repeat steps a through e to program the next channel.
- g. Press RECEIVE or any other function button to get out of the program function.

Programmed channels are stored in battery back-up CMOS RAM. At power up, the microprocessor checks the validity of the RAM. If the RAM fails the validity check the channels are defaulted to 10.000000 MHz, AGC-fast, Mode-USB, and BFO-0.00 kHz.

### **3.7.2 Programming Groups**

In addition to incremental channel scan, the receiver has the capability of scanning predefined subsets of channels organized as groups (zero to nine). Each of these ten groups may have between zero and twenty channels in it. Any channel may be assigned to any group and the same channel can be assigned to several groups if desired.

To program these groups the operator should:

- a. Press PROGRAM and then GROUP. The receiver responds by prompting GROUP NUMBER?.
- b. Select the single digit group number via the keypad. Press ENTER. The receiver responds by clearing the group of previous channels and prompts CHANNEL NUMBER?.
- c. Select a two digit channel number. Press ENTER and LOAD. (Channel numbers will appear at half brilliance until the ENTER button is pushed. The receiver responds with the channel number followed by OK when the LOAD button is pushed.)
- d. Select the next two digit channel number. Press ENTER and LOAD. Channels are entered in this fashion, until all the desired channels in this group (up to 20) have been entered.
- e. Press GROUP to select another Group to program. The receiver responds again with the prompt GROUP NUMBER?.

- f. Repeat steps b through e for up to nine more groups.
- g. Press RECEIVE or any other function button to get out of the Program function.

Since the operator can manually scan through a group in the Scan function using the Tune knob, no special provision has been provided for reviewing the groups in the Program function. Also, the RECALL button has no effect in Group programming.

### **3.7.3 Program Function – Effect on Receiver Operation**

In general, the receiver operating frequency is changed only in Receive or Scan. Entries made in Program function do not change the frequency of operation. Because Program function does affect the front panel display, return to the Receive function from the Program function will restore the display to the true parameters that are presently in use.

## **3.8 SCAN FUNCTION**

The Scan function of the receiver is entered by pressing the SCAN button. The message prompt GROUP OR CHANNEL SCAN?, then appears in the alphanumeric display field. The operator responds by pressing either the GROUP button for group scan or the CHANNEL button for sequential channel scan.

### **3.8.1 Dwell Selection in Scan Function**

Dwell time per channel is a front panel scroll function that is selected for scan operation. It is not preprogrammed with channels or groups. There are ten internal dwell selections. They are 0.1, 0.2, 0.4, 0.5, 0.8, 1.0, 2.0, 4.0, 5.0, and 8.0 seconds. Additionally, the scroll includes the selection of EXT for external channel change timing. Note that the dwell times scroll is from minimum to maximum and back down to minimum without rolling around.

### **3.8.2 Channel Scan**

If the operator presses the CHANNEL button after entering the Scan function, the receiver prompts FIRST CHANNEL?. The operator responds by selecting 2 digit channel number at the keypad followed by ENTER. The receiver responds by prompting LAST CHANNEL? and the operator selects another channel at the keypad and presses ENTER. The keypad selections are the lower and upper limits on an incremental Channel Scan. If the last limits used (displayed with the prompt) are desired, the number need not be reentered. Pressing ENTER alone will reuse the previous SCAN channels.

### **3.8.3 Group Scan**

If the operator pressed GROUP after entering Scan mode, the receiver responds by prompting GROUP NUMBER?. The operator selects a group by pressing a digit followed by ENTER. (The number of the last group scanned or programmed will appear with the prompt. To reuse this group number, press ENTER alone.) The receiver automatically scans the channels in the indicated group in the same order that they were entered using the dwell selected at the front panel. If the group has not been programmed, the receiver responds by displaying ANOTHER GROUP? and the operator should select an alternate group.

### **3.8.4 Additional Scan Details**

The scan may be stopped by:

- Pressing the SCAN button while scanning (a second push will restart it).
- Pressing TUNE to stop automatic Scan and press CHANNEL to allow Manual scan via the TUNE knob (CHANNEL and TUNE LEDs will be on).
- Providing an external Stop Scan signal (see table 2-4).

### **3.9 AUXILIARY CHANNEL**

Operators will frequently have a preferred (most widely used) frequency or channel. The receiver provides a method to instantly call up this favorite setting while tuned to some other frequency in the Receive function. To program this auxiliary channel, update the display to the desired frequency, modulation mode, etc (while in the Receive function) and press LOAD. To use the auxiliary channel, simply press RECALL at any time while in the Receive function. The receiver will tune to the auxiliary channel and will update the displays accordingly.

The auxiliary channel information is also stored in the battery backup RAM, so the favorite channel data is stored during power off.

## SECTION 4

### TECHNICAL DESCRIPTION

#### 4.1 INTRODUCTION

The information in this section is in the following two broad categories:

- A general overview of RF-590 Receiver operation
- Specific electronic theory about circuits and/or concepts utilized in the RF-590

Included in the general receiver overview are the following items:

- Receiver signal path simplified block diagrams
- Receiver gain distribution chart
- Frequency synthesizer simplified block diagram
- Synthesizer operation example using a desired radio tune frequency

Included in the electronic theory section are the following items:

- Conversion between dBm and volts rms chart
- Discussion about the "heart" of the RF-590 frequency synthesizer, the phase-locked loop, and its many variations
- VCO frequency resolution reduction techniques

Many of these items appear in other sections of this manual and are discussed as necessary. For example, there are more extensive block diagrams provided with circuit descriptions, schematics, parts lists, and test procedures in each subassembly section describing a particular RF-590 assembly. However, items such as the dBm to V<sub>rms</sub> conversion chart appear nowhere else in the text.

#### 4.2 RECEIVER OPERATION

##### 4.2.1 Receiver Signal Path

The information presented in this section details the signal processing in the receiver signal path from antenna RF input to audio output. The RF input range is from 10 kHz to 30 MHz. A dual conversion type receiver is employed, with the first intermediate frequency (IF) of 40.455 MHz and a second intermediate frequency (IF) of 455 kHz.

A variable first local oscillator (LO No. 1) of 40.465 to 70.455 MHz is employed for the first conversion to 40.455 MHz while a fixed second local oscillator (LO No. 2) at 40.000 MHz is employed for the second conversion to 455 kHz.

The RF signal path contains the following assemblies:

- Input Filter Assembly A1
- First Converter Assembly A2
- Second Converter Assembly A3
- IF Filter Assembly A4
- IF/Audio Assembly A5A1 and AGC Assembly A5A2
- Audio Amplifier Assembly A23

Additionally, Meter Board Assembly A13A3 provides monitoring capabilities, and ISB IF/Audio Assembly A18 provides ISB operation capabilities. Note that the A18 assembly is optional.

The following brief circuit descriptions follow figure 4-1, Simplified Receiver Block Diagram. A Receiver Gain Distribution Chart, figure 4-2, has also been included.

#### 4.2.1.1 Input Filter Assembly A1

The antenna input to the receiver is applied to Input Filter Assembly A1. This assembly contains low pass filtering to provide more than 100 dB of rejection to undesired signals at input frequencies greater than 30 MHz.

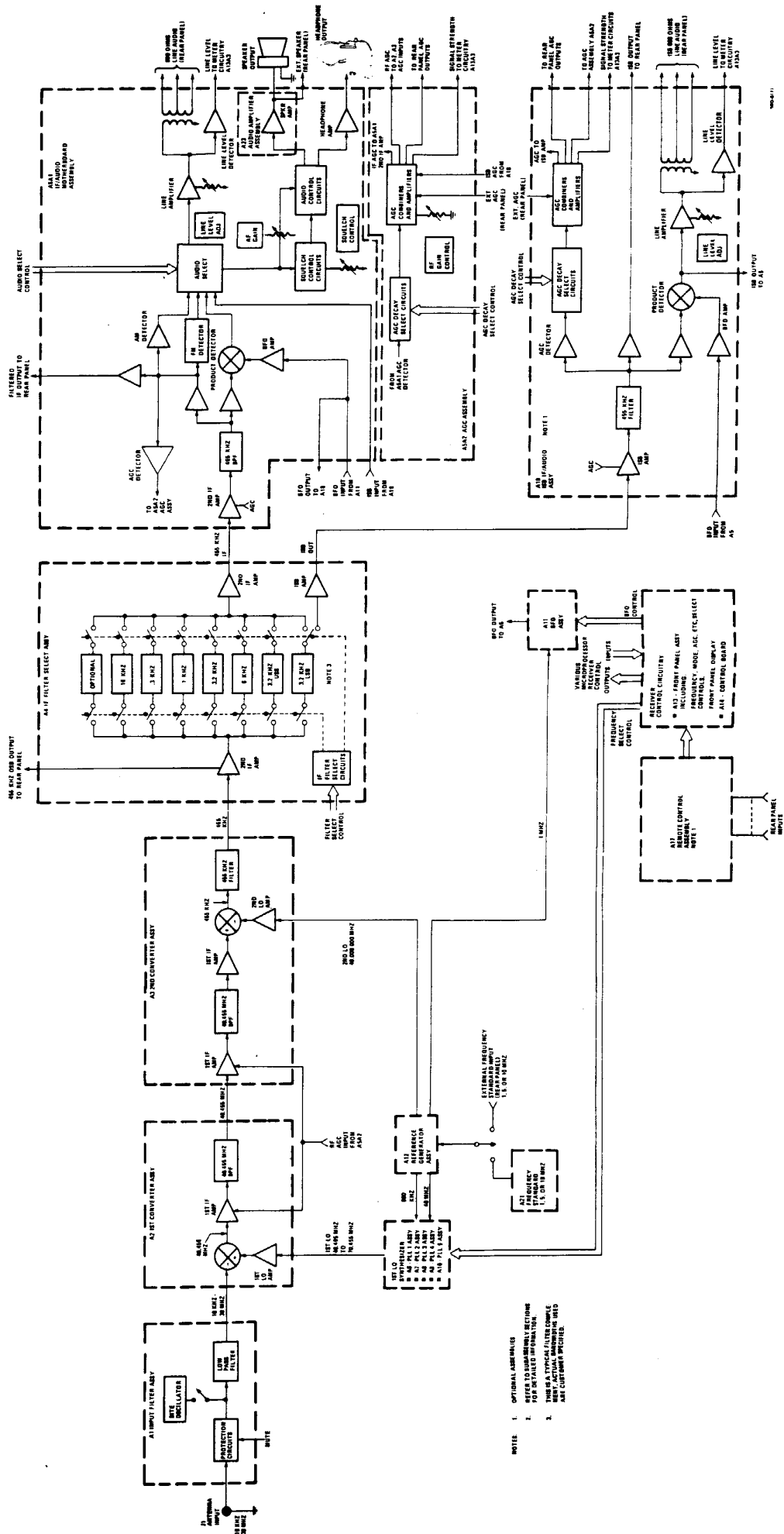
Insertion loss is less than 1/2 dB, with a VSWR less than 2:1. Receiver input overload protection circuitry (up to 70 Vrms overload), muting, Built-In Test Equipment (BITE) detection, and BITE signal generation functions are also included.

#### 4.2.1.2 First Converter Assembly A2

First Converter Assembly A2 accepts the 10 kHz to 30 MHz output from the A1 assembly and subtractively mixes with the first LO (40.465 to 70.455 MHz) to produce a first IF of 40.455 MHz. (Note that sideband inversion occurs during the mixing process.) Extensive filtering is utilized at 40.455 MHz before the first IF is directed to second Converter Assembly A3. Input signal levels of typically -120 to +10 dBm are gain controlled by an AGC signal which provides up to 20 dB of gain reduction. Typical conversion loss through the assembly is 0 dB.

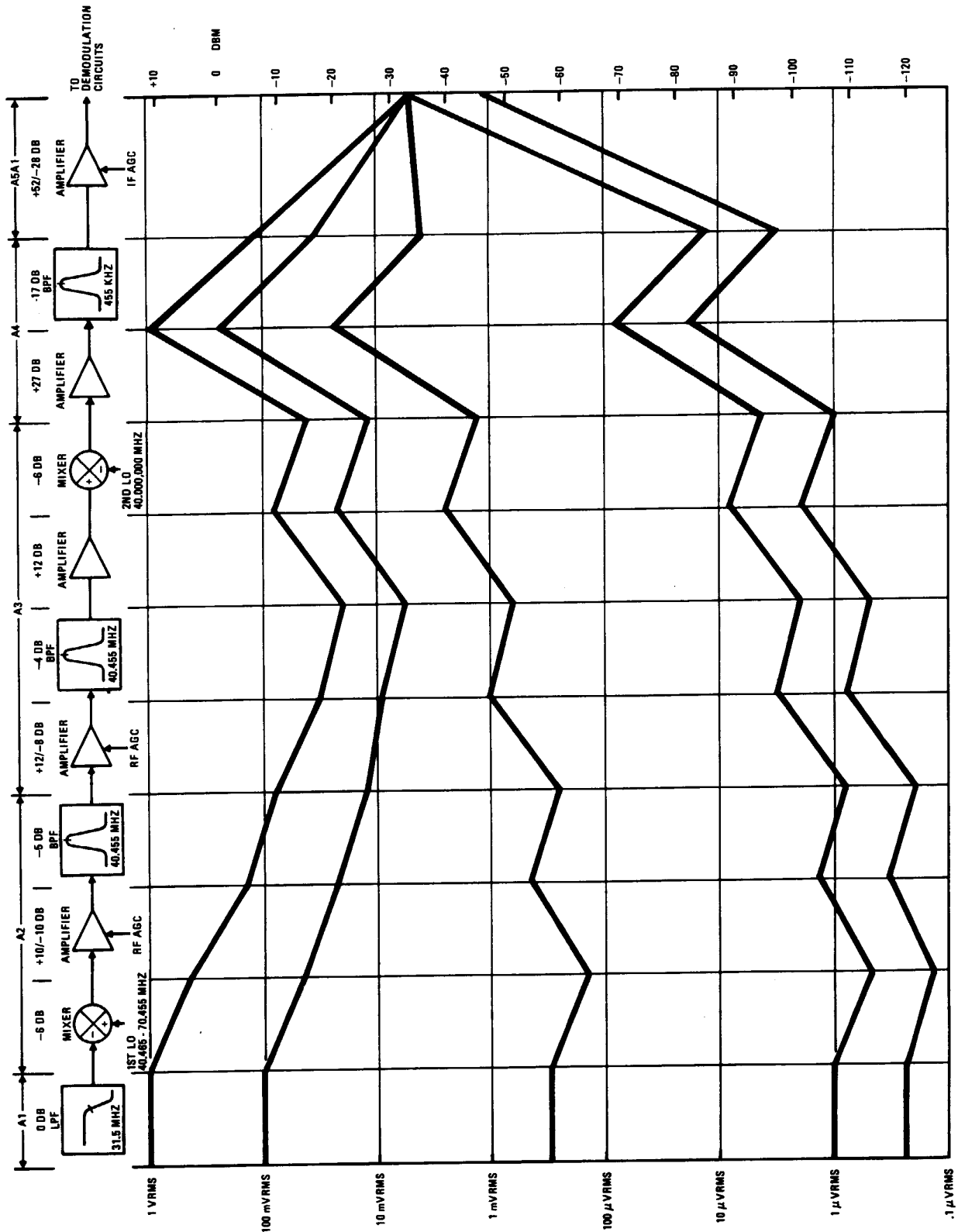
A BITE detector operating at 40.455 MHz monitors the operation of the assembly.

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- NOTE: 1. OPTIONAL ASSEMBLIES  
2. REFER TO TABLES FOR PARTS LIST  
3. THESE ARE TYPICAL ALTERNATE COMPONENTS  
4. REFER TO THE DRAWING FOR THE ACTUAL COMPONENTS  
5. REFER TO THE DRAWING FOR THE ACTUAL COMPONENTS

Figure 4-1. RF-590 Receiver Signal Path Block Diagram



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Figure 4-2. RF-590 Receiver Gain Distribution



#### 4.2.1.3 Second Converter Assembly A3

Second Converter Assembly A3 converts the first IF of 40.455 MHz to a second IF of 455 kHz through subtractive mixing with the second LO frequency of 40.000000 MHz.

Filtering occurs at both IF frequencies. Overall module gain is approximately 16 dB and gain reduction of up to 20 dB is controlled by an AGC voltage.

A BITE detector operating at 455 kHz monitors the operation of the assembly.

#### 4.2.1.4 IF Filter Assembly A4

IF Filter Assembly A4 accepts the second IF from the A3 assembly and provides the selection of one of eight filters for signal processing. (ISB operation requires selection of two filters.) The main signal frequency selectivity is determined by these filters. Module gain is +10 dB. An unfiltered 455 kHz signal output is tapped off and applied to a rear panel RF-590 connector for external demodulation or monitoring purposes. Two main signal outputs are fed off this board. The two signal outputs are:

- The normal 455 kHz second IF to the A5A1 IF/Audio assembly, (for AM, CW, FM, USB, or LSB operation).
- ISB output to the optional A18 ISB IF/Audio assembly (for ISB operation).

#### 4.2.1.5 IF/Audio Assembly A5

IF/Audio Assembly A5 consists of the following two subassemblies:

- IF/Audio Motherboard A5A1
- AGC Board A5A2

##### 4.2.1.5.1 IF/Audio Motherboard A5A1

The IF/Audio Motherboard A5A1 provides most of the receiver gain utilizing a cascaded 455 kHz second IF AGC controlled amplifier chain with a maximum gain of 80 dB. This amplifier works in conjunction with AGC controlled amplifiers on the A2 and A3 assemblies to provide a constant -34 dBm second IF output to the signal demodulators over an RF input range of -120 dBm to +10 dBm.

Additionally, the assembly contains circuits for the following functions:

- Signal demodulation (AM, FM, and Product Detection for USB, LSB, or CW signals)
- Audio amplification and control

- Squelch control
- BITE detection

Signal outputs include:

- Speaker audio output (to speaker Audio Amplifier Assembly A23)
- Headphones (+10 dBm (maximum)/600 ohms)
- Line output (-16 dBm to +10 dBm/600 ohms, rear panel)
- Filtered 455 kHz IF output (50 ohm, rear panel)

Note that audio outputs (speaker and headphone) and line output are independently adjustable.

#### 4.2.1.5.2 AGC Board A5A2

AGC Board A5A2 contains AGC (Automatic Gain Control) voltage generation and shaping circuitry for slow, medium, or fast AGC decay speeds. BITE detection circuitry is also provided. Outputs include AGC control voltages to A2, A3, and A5A1 assemblies and a rear panel AGC output. Figure 4-2 (receiver gain distribution) shows the effectiveness of the AGC circuits in providing a constant -34 dBm input to the A5A1 signal demodulators.

#### 4.2.1.6 Audio Amplifier A23

Audio Amplifier Assembly A23 receives demodulated audio from the A5A1 assembly. Amplifiers on this assembly provide enough power gain to drive the 8 ohm front panel speaker or an external 8 ohm speaker to a minimum of 2.5 watts at full audio.

#### 4.2.1.7 ISB IF/Audio Assembly A18

ISB IF/Audio Assembly A18 is an option purchased when independent sideband operation (simultaneous LSB and USB) is required. A18 operation is virtually identical to A5 operation, except that the A18 assembly contains only one demodulator circuit (the ISB product detector). A 455 kHz ISB IF output, an ISB line audio output, and an ISB AGC voltage output are provided on the RF-590 rear panel.

#### 4.2.1.8 Meter Board A13A3

Meter Board A13A3 contains the circuitry and switches required to monitor selected RF and AF signals. The following signals may be monitored on the front panel meter via front panel switch controls:

- USB-RF
- USB-AF

- LSB-RF
- LSB-AF

(Note that in ISB operation, the ISB channel is monitored in the LSB switch mode.)

Meter drive signals originate on IF/Audio Assembly A5. (ISB signals originate on ISB IF/Audio Assembly A18.) The meter itself is calibrated in microvolts rms or mVrms for RF signal strength and dBm/600 ohms for AF line level.

#### 4.2.2 Frequency Synthesizer

The information presented in this section shows the signal processing required to cause the receiver to tune anywhere in the RF input range of 10 kHz to 30 MHz with a 1 Hz resolution.

The main function of the entire synthesizer is to provide a variable output frequency that functions as the first Local Oscillator injection for the first Converter A2 mixer. This first LO must have the following characteristics:

- a. Tune exactly 40.455000 MHz higher in frequency than the desired RF input signal. This requires a range of 40.465 MHz to 70.455 MHz.
- b. Respond to changes in the receiver's tuning controls to allow a 1 Hz resolution over the approximately 30,000,000 Hz tuning range.
- c. Perform a. and b. within a tuning time of less than 20 milliseconds.

The Frequency Synthesizer consists of the following assemblies:

- PLL I Assembly A6
- PLL II Assembly A7
- PLL III Assembly A8
- PLL IV Assembly A9
- PLL V Assembly A10
- Reference Generator Assembly A12
- Frequency Standard Assembly A21

Reference Generator Assembly A12 also provides the 40.000000 MHz second LO injection for the A3 assembly's signal conversion of the 40.455 MHz first IF to a 455 kHz second IF.

BFO Assembly A11 is also a frequency synthesizer covering a much smaller frequency range (445 kHz to 465 kHz). The BFO assembly is required to accomplish product detection.

Note that figure 4-3 shows a complete frequency synthesizer simplified block diagram and figure 4-4 shows how to compute the intermediate frequencies produced by the synthesizer assemblies for any given receiver tune frequency. Other information which may be helpful (towards the end of this section) is the discussion of programmable divide by N phase locked loops and frequency resolution reduction techniques. Also, all these assemblies are discussed in detail in their respective subsections.

#### 4.2.2.1 Frequency Synthesizer - Basic Operation

The frequency synthesizer must be able to tune 40.465000 MHz to 70.455000 MHz with 1 Hz resolution. In order to do this, three main phase locked loop voltage controlled oscillators with programmable divide by N counters are utilized.

The frequency of each of these VCOs is a function of their associated programmable counter factor, N. N is a function of the values of the receiver's tuning positions (10 MHz, 1 MHz, . . . 1 Hz). Each of the programmable counters are wired to accept only a segment of the receiver's tuning positions. For example, the A7 assembly receives tune data relating to the 10 MHz, 1 MHz, and 100 kHz position's value. The A8 assembly receives tune data relating to the 10 kHz and 1 kHz values, and the A10 assembly receives tune data relating to the 100 Hz, 10 Hz, and 1 Hz values. (Note that this data is in the form of a serial data code generated by the receiver's Control Board Assembly A14).

If the values of the input tune data change (for any of these three assemblies), the programmable counter's divide by N factor changes. Since the programmable counter is in the VCO feedback path to a phase comparator, the phase comparator issues an error command to force the VCO to tune in the direction required to make the feedback signal equal to the reference signal at the phase comparator's inputs. The net result (for each of the three assemblies) is that the VCO output frequency is a unique frequency corresponding to exactly one value of the tune data at the input to the programmable counter, and hence to the receiver tune frequency.

The outputs of the A7, A8, and A10 assemblies undergo further processing in the synthesizer chain before they are combined in the A6 assembly. The result of the combination of these three unique frequencies is a single unique frequency directly relating to the settings of all the receiver's tune positions. Furthermore, it is controllable to 1 Hz resolution, and is used as the first LO injection for the First Converter Assembly A2 mixer to tune the radio.

#### 4.2.2.2 Reference Generator Assembly A12 and Frequency Standard Assembly A21

Frequency Standard Assembly A21 is the key to the RF-590 frequency stability and accuracy. Three stability options are available:  $1 \times 10^{-6}$ ,  $1 \times 10^{-7}$ , and  $1 \times 10^{-8}$  per day at either 1 MHz, 5 MHz, or 10 MHz.

The standard output phase locks a 40 MHz VCXO on the A12 assembly. Phase lock loop (PLL) references on all other assemblies are derived from this A12 VCXO. The A12 also provides 40 MHz to the A3 assembly for signal path conversion to the second IF of 455 kHz.

#### 4.2.2.3 PLL V Assembly A10

The A10 assembly is a programmable divide by N PLL that provides the 1 Hz, 10 Hz, and 100 Hz tuning increments in the LO 1 output signal. The A10 output is from 50 to 60 kHz in 10 Hz controllable steps. The output frequency is  $10 (6000 - X_3X_2X_1)$  Hz, where  $X_3X_2X_1$  is the value of the 100 Hz, 10 Hz, and 1 Hz receiver tune positions, respectively.

#### 4.2.2.4 PLL IV Assembly A9

The A9 assembly is a translational type phase locked loop which converts the low frequency A10 output of 50 to 60 kHz in 10 Hz increments into 40.05 to 40.06 MHz in 10 Hz increments. The A9 assembly provides the intermediate signal processing required before the A10 output can be combined with the PLL III A8 10 kHz and 1 kHz tuning increments. The A9 output may be computed from the formula  $40,000,000 + 10 (6000 - X_3X_2X_1)$  Hz, where  $X_3X_2X_1$  is the value of the 100 Hz, 10 Hz, and 1 Hz receiver tune positions, respectively.

#### 4.2.2.5 PLL III Assembly A8

The A8 assembly is a programmable divide by N and translation PLL which performs the following two functions:

- Generation of the 10 kHz and 1 kHz tuning increments for LO 1 output
- Combination of these increments with the 100 Hz, 10 Hz, and 1 Hz tuning increments provided by the A9 assembly

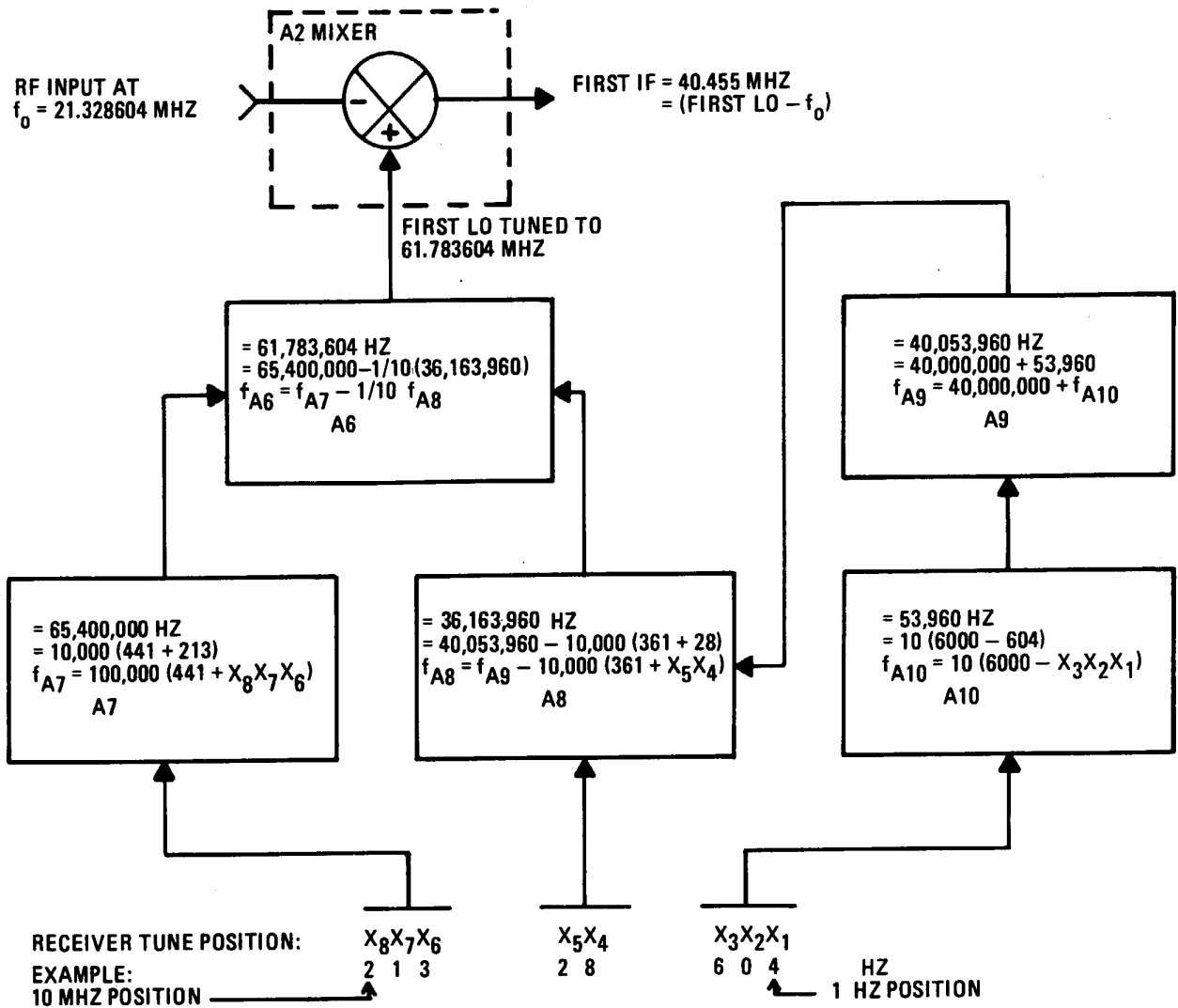
The A8 output frequency can be determined by the following formula. Given that  $X_3X_2X_1$  are the values of the receiver's 100 Hz, 10 Hz, and 1 Hz tuning positions and that  $X_5X_4$  are the values of the 10 kHz and 1 kHz tuning positions, A8 frequency =  $[40,000,000 + 10 (6000 - X_3X_2X_1)] - [10,000 (361 + X_5X_4)]$  Hz. Note that the A8 output frequency range is 35.45 MHz to 36.45 MHz.

#### 4.2.2.6 PLL II Assembly A7

The A7 assembly is a programmable divide by N PLL which provides the 10 MHz, 1 MHz, and 100 kHz tuning increments in the LO 1 output. The A10 output is from 44.1 MHz to 74.0 MHz in 100 kHz controllable steps.

The A7 output frequency is  $100,000 (441 + X_8X_7X_6)$ , where  $X_8X_7X_6$  is the value of the 10 MHz, 1 MHz, and 100 kHz receiver tuning positions, respectively.





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Figure 4-4. Frequency Synthesizer Tuning Example

#### 4.2.2.7 PLL I Assembly A6

The A6 assembly is a translation type PLL which combines the 10 MHz through 1 Hz tuning increments for the LO 1 output from assemblies A7, A8, A9, and A10. The output signal will be the first LO injection signal. It will be variable from 40.465 kHz to 70.455 MHz in 1 Hz controllable steps. Given a receive tune frequency of  $X_8X_7X_6X_5X_4X_3X_2X_1$  Hz where  $X_8$  to  $X_1$  are the values of the 10 MHz to 1 Hz receiver tuning positions, the A6 (and LO 1) output frequency is:

$$FA6 = FA7 - \frac{1}{10} FA8 \text{ Hz,}$$

where

$$FA7 = (441 + X_8X_7X_6) 100,000 \text{ Hz}$$

$$FA8 = [40,000,000 + 10 (6000 - X_3X_2X_1)] - [10,000 (361 + X_5X_4)] \text{ Hz}$$

This signal will always be tuned exactly 40.455 MHz above the receiver tune frequency.

#### 4.2.2.8 BFO Assembly A11

The A11 assembly is a programmable divide by N PLL which provides the BFO offset injection signal required on IF/Audio Motherboard Assembly A5A1 for proper CW or SB reception. The BFO output at 455 kHz  $\pm$  10 kHz mixes with the 455 kHz second IF signal at the product detector and provides an audio offset of up to 10 kHz. The A11 output frequency may be determined from the following formula where  $X_A X_B X_C$  is the  $\pm$  value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tuning positions:

$$FA11 = 10 (45,500 - X_A X_B X_C) \text{ Hz}$$

#### 4.2.2.9 Frequency Synthesizer Tuning Example

The output frequencies of the A10, A9, A8, A7, and A6 assemblies at any given receiver tune frequency can be determined from the example shown in figure 4-4. Assume a receiver frequency  $f_o = 21,328,604$  Hz and that  $X_8X_7X_6X_5X_4X_3X_2X_1$  represent the values of the 10 MHz through 1 Hz positions.

Start at the A10 assembly, then move on to the A9, A8, A7, and A6 in that order.

The answer can always be checked since the following formula must always be true.

$$F_{LO 1} = f_o + 40.455 \text{ MHz}$$

Here,

$$f_o = 21.328,604 \text{ MHz}$$

therefore,

$$\begin{aligned} F_{LO 1} &= 21.328,604 \text{ MHz} + 40.455 \text{ MHz} \\ &= 61.783,604 \text{ MHz (which agrees with the result of figure 4-4)} \end{aligned}$$



### 4.3 ADDITIONAL THEORY

#### 4.3.1 Conversion Between dBm and Vrms

Power levels in this manual are stated in dBm, or decibels with respect to 1 milliwatt. For example, +6 dBm means 6 dB more than (above) 1 mW, or 4 mW. Similarly, -6 dBm is 6 dB less than (below) 1 mW, or 0.25 mW (250 uW). Notice that every value of dBm corresponds to a particular amount of power. If the impedance in which this power is dissipated is known, the corresponding voltage and current can be determined. Table 4-1 lists 50 ohm voltage equivalents for many dBm power levels. Note that for negative values of dBm, voltages are read in either of the two left-hand columns. For positive values of dBm, voltages are read in the right-hand column. For instance, -6 dBm is 0.112 V (112 mV), across 50 ohms, while +6 dBm is 0.446 V. Similarly, -20 dBm equals 22.4 mV, while +20 dBm equals 2.24 volts (across 50 ohms).

**Table 4-1. Conversion of dBm to Vrms across 50 ohms  
(0 dBm = 1 mWatt)**

(Negative dBm)		dBm	(Positive dBm)
Volts	Millivolts		Volts
.224	224	0	.224
.199	199	1	.251
.178	178	2	.282
.158	158	3	.316
.141	141	4	.354
.126	126	5	.398
.112	112	6	.446
	99.9	7	.501
	89.0	8	.562
	79.3	9	.630
	70.7	10	.707
	63.0	11	.793
	56.2	12	.890
	50.1	13	.999
	44.6	14	1.12
	39.8	15	1.26

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**Table 4-1. Conversion of dBm to Vrms across 50 ohms (Cont.)**  
(0 dBm = 1 mWatt)

(Negative dBm)		dBm	(Positive dBm)
Volts	Millivolts		Volts
	35.4	16	1.41
	31.6	17	1.58
	28.2	18	1.78
	25.1	19	1.99
	22.4	20	2.24
	19.9	21	2.51
	17.8	22	2.82
	15.8	23	3.16
	14.1	24	3.54
	12.6	25	3.98
	12.0	25.41	4.17
	11.2	26	4.46
	10.0	27	5.01
	8.90	28	5.62
	7.93	29	6.30
	7.07	30	7.07
	3.98	35	12.6
	2.24	40	22.4
	1.26	45	39.8
	0.707	50	70.7

#### 4.3.2 PLL Frequency Resolution Reduction Techniques

Use of a single frequency source to provide the variable first local oscillator signal in a radio such as the RF-590 would be virtually impossible (given the resolution requirements desired). This would require that the LO tune over the entire range (40.465000 MHz to 70.455000 MHz) with a resolution of 1 Hz or a total of 30,000,000 discrete 1 Hz steps. By using three sources, each with a much lower resolution requirement and combining their outputs, the net one part per 30,000,000 resolution can still be obtained.

Assume that a total of 30,000,000 1 Hz increments must be tuned. Allow each of the three sources to produce an output response proportional to only a segment of the 30,000,000 necessary frequencies. The following three examples show how the three sources produce an output response.

- Let source no. 1 respond to changes in the 10 MHz, 1 MHz, and/or .1 MHz positions. Since these would be a maximum of 300.1 MHz possible changes between 00.0 MHz and 29.9 MHz, the resolution of source no. 1 would be one part per 300.
- Let source no. 2 respond to changes in the 10 kHz and/or 1 kHz position. There would be a maximum of 100 1 kHz changes between 00 kHz and 99 kHz (for a resolution of 1 part per 100).
- Let source no. 3 respond to changes in the 100 Hz, 10 Hz, and/or 1 Hz positions. There would be a maximum of 1000 1 Hz changes between 000 Hz and 999 Hz (for a resolution of one part per 1000).

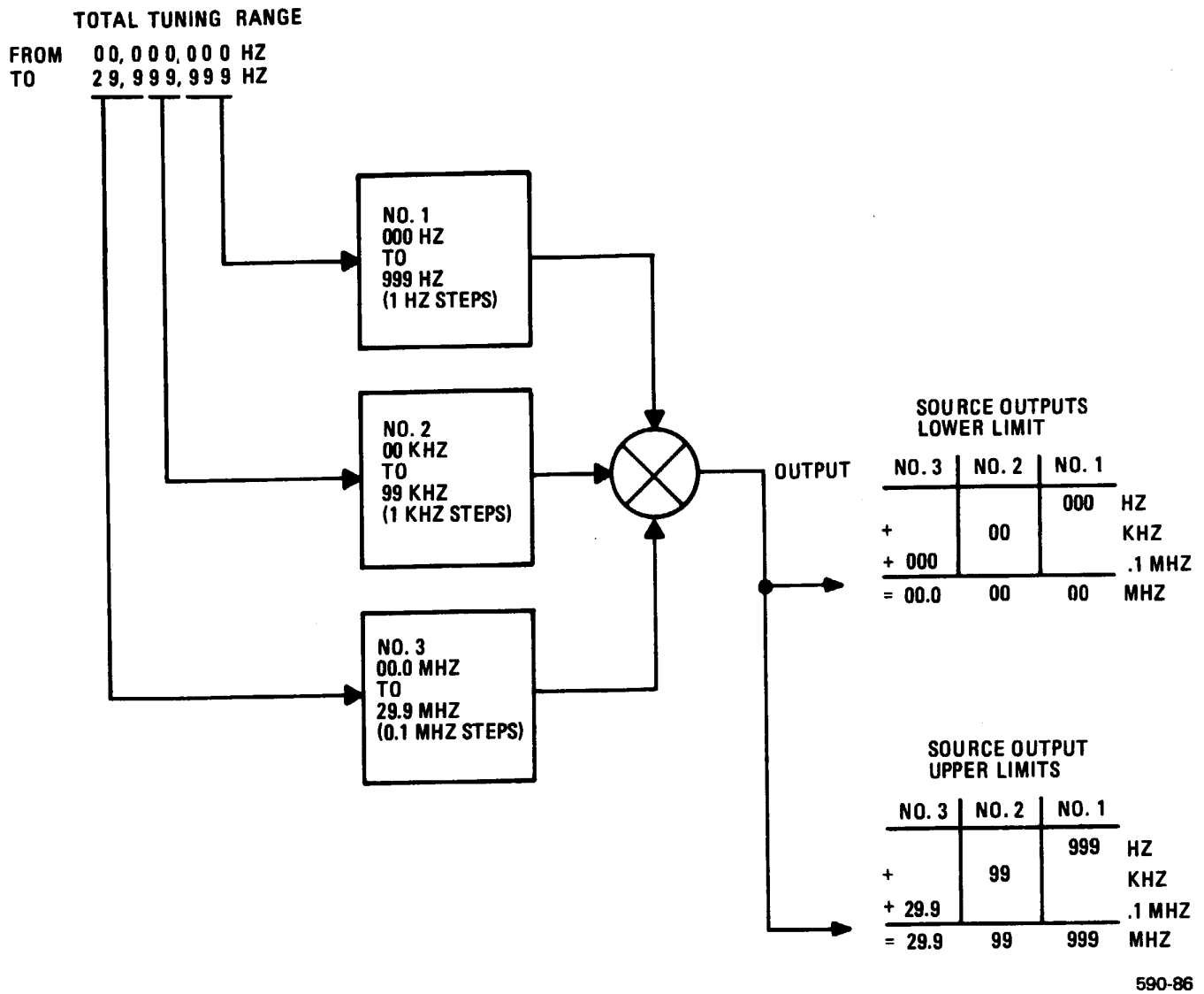
Combining the three source outputs in a nonlinear device such as a mixer would yield the desired frequency range and 1 Hz resolution required. Figure 4-5 illustrates this.

Note that the sources used in this example would actually be voltage controlled oscillators (VCO) whose actual output frequency would be controlled by a programmable divide by N counter.

The RF-590 essentially uses this concept, except that the source frequencies run at a much higher frequency than those shown. There are three VCOs which respond to the tuning segments shown. (10 MHz, 1 MHz, and 100 kHz increment changes occur on the A7 assembly, the 10 kHz and 1 kHz increment changes occur on the A8 assembly, and the 100 Hz, 10 Hz, and 1 Hz increment changes occur on the A10 assembly.)

#### 4.3.3 Phase Locked Loops (PLL)

The basic phase locked loop (PLL) consists of four components: a phase detector (or comparator), a low pass filter, a voltage controlled oscillator (VCO), and a divider (counter). The counter component may be either a fixed divisor or programmable. The RF-590 utilizes both types.

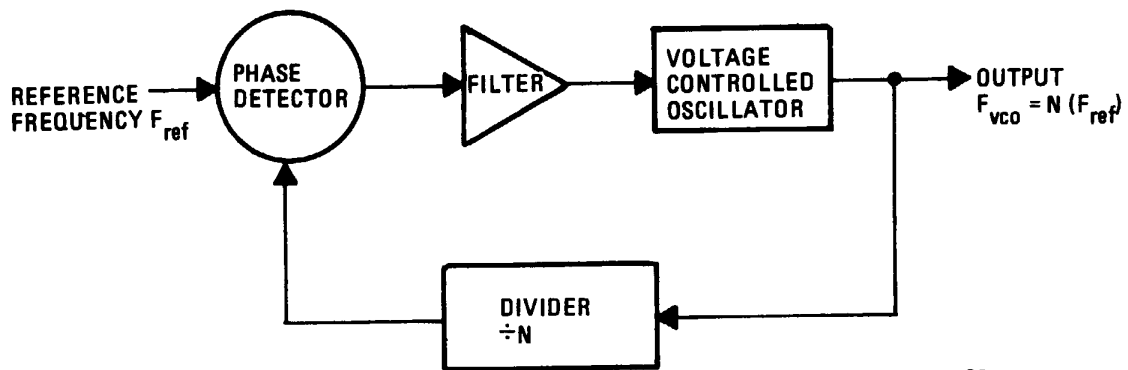


590-86

Figure 4-5. Resolution Reduction Example

#### 4.3.3.1 Basic Phase Locked Loop

Figure 4-6 shows the four basic components of a phase locked loop. PLL operation involves comparing the frequency and phase of an incoming reference signal to the output of the voltage controlled oscillator (VCO). If the two signals differ in frequency and/or phase, an error voltage is generated by the phase detector and applied to the VCO. This causes it to correct in the direction required for decreasing the frequency/phase difference. The correction procedure continues until lock is achieved, after which the VCO will track the incoming reference signal.



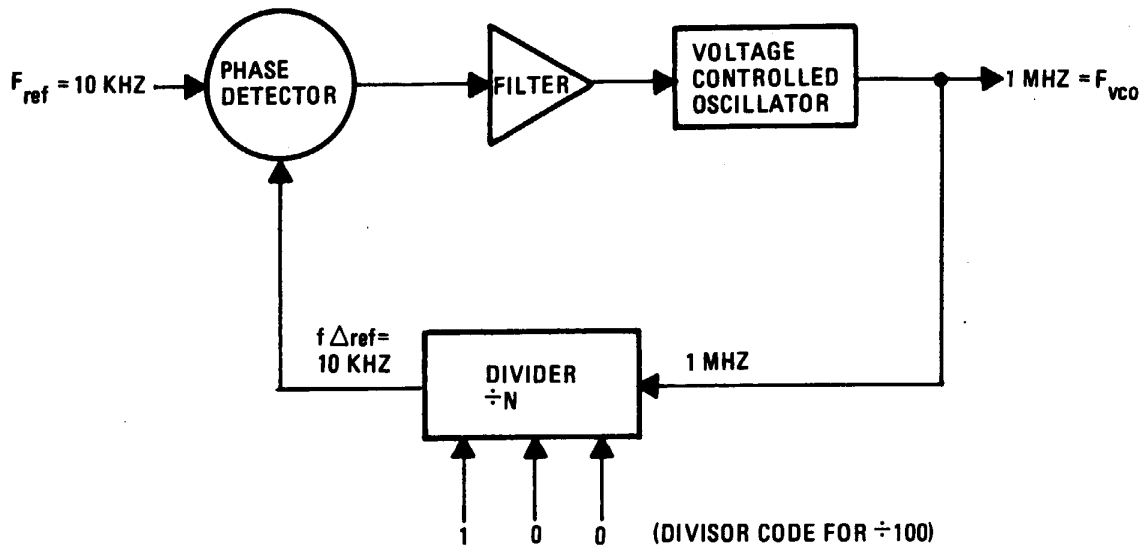
590-38

Figure 4-6. Basic Phase Locked Loop

#### 4.3.3.2 PLL Programmable Counters

Dividing a VCO output by two before applying it to the phase detector results in an error voltage that drives the VCO to twice the reference frequency. A divide-by-three action results in an error voltage that drives the VCO to three times the reference frequency. From this, the following relationship can be given,  $f_{VCO} = N (F_{REF})$ .

An example of the basic phase lock loop technique, using numbers, will provide an understanding of its actual operation. Referring to figure 4-7, the desired frequency is obtained by programming the variable divider through selectable inputs. Assuming the VCO is locked at the desired frequency of 1 MHz, this signal enters the input of the (in this case) divide-by-100 counter (divider). The counter emits a pulse at its output each time 100 pulses enter its input. Therefore, dividing the 1 MHz input by 100 results in an output of 10 kHz. This 10 kHz signal is compared to the reference frequency of 10 kHz indicating a locked situation. If the divider's output had been less than 10 kHz, the phase detector would have produced pulses to drive the VCO to a higher frequency. Similarly, if the divider's output had been greater than 10 kHz, the VCO would have been driven to a lower frequency. Note that the phase lock loop's output is dependent upon the selectable inputs of the variable divider. The RF-590 provides this input to the  $\div N$  counter in the form of a serial data command word. The coding of this word determines the divisor ratio of the counter, and is supplied (under microprocessor control) from the information supplied by the RF-590 frequency select controls.

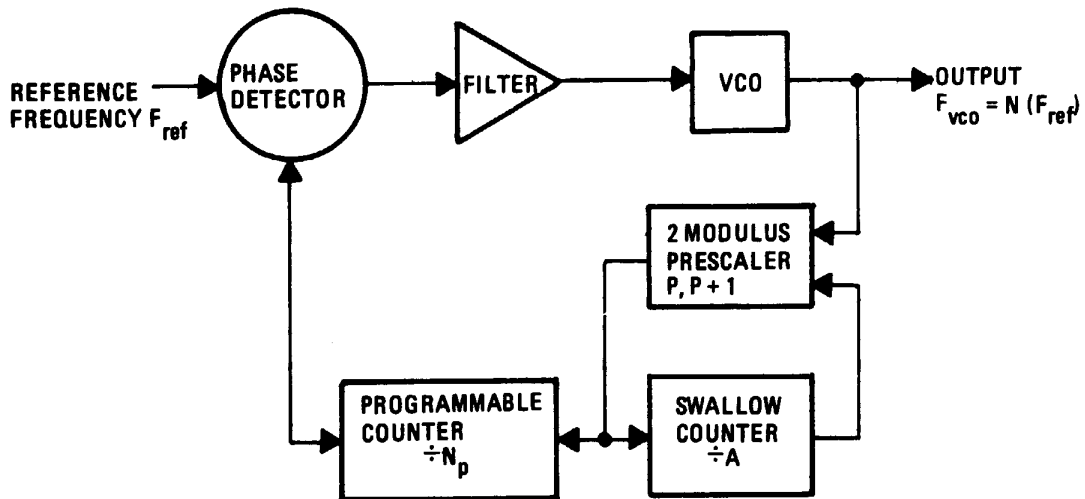


590-39(1)

Figure 4-7. Programmable Phase Lock Loop

#### 4.3.3.3 PLL Prescaling Operation

A variation of the basic PLL which involves division of the feedback VCO signal prior to application to the  $\div N$  counter is shown in figure 4-8. The total divider portion of the PLL now consists of two programmable counters and a two modulus prescaler.



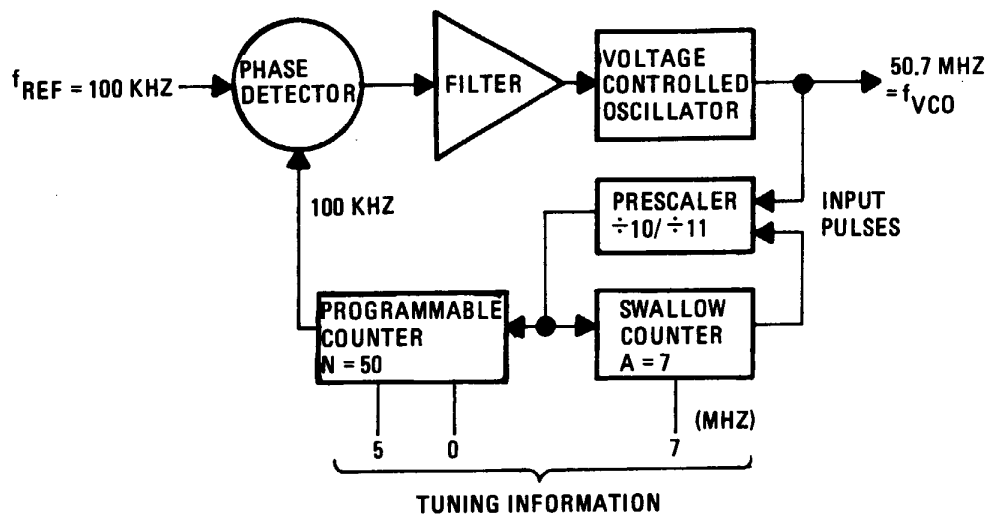
590-40

Figure 4-8. Phase Lock Loop Prescaling Technique

The two modulus prescaler begins operation by dividing the VCO output by the higher of its two possible divisors,  $P + 1$ . The programmable  $\div N$  counter counts the number of pulses from the prescaler. The swallow counter controls the number of times that the prescaler will be allowed to divide by  $(P + 1)$ . (To be precise,  $A$  times.) After the swallow counter reaches  $A$  counts, it instructs the prescaler to change its division ratio to  $P$ . (Note that the RF-590 uses this scheme on the A7 and A10 assemblies, where the prescaler is a  $\div 10/\div 11$  counter, and the swallow counter is a counter internal to the  $\div N$  IC.)

In operation, the prescaler divides by  $P + 1$ ,  $A$  times. For every  $P + 1$  pulse from the prescaler, both the  $A$  counter and  $N_p$  counter are decreased by 1. The prescaler divides by  $P + 1$  until counter  $A$  reaches its zero state. At this point, the modulus of the prescaler changes to  $P$ . The prescaler then divides by  $P$  until the remaining count,  $(N_p - A)$  in the  $N_p$  counter, decreases to zero. At this time, the  $N_p$  output emits a pulse while the  $A$  and  $N_p$  counters reset. The cycle then repeats.

An example of the two modulus prescaling technique is given in figure 4-9 and table 4-2. For illustrative purposes, a VCO output of 50.7 MHz is desired.



590-59

Figure 4-9. Prescaling Technique Example

Table 4-2. Prescaling Technique Example

Input Pulses	Prescaler Counts	Swallow Counter	Programmable Counter
0	0	7	50
11	11	6	49
22	11	5	48
33	11	4	47

**Table 4-2. Prescaling Technique Example (Cont.)**

Input Pulses	Prescaler Counts	Swallow Counter	Programmable Counter
44	11	3	46
55	11	2	45
66	11	1	44
77	11	0	43
87	10	0	42
97	10	0	41
107	10	0	40
477	10	0	3
487	10	0	2
497	10	0	1
507	10	0	0

507 input pulses = 1 output pulse

Selected into the programmable counter are the two most significant digits, 5 and 0. Selected into the swallow counter is the least significant digit, 7. Under locked conditions, the divider has an input (fVCO) of 50.7 MHz, and an output of 100 kHz.

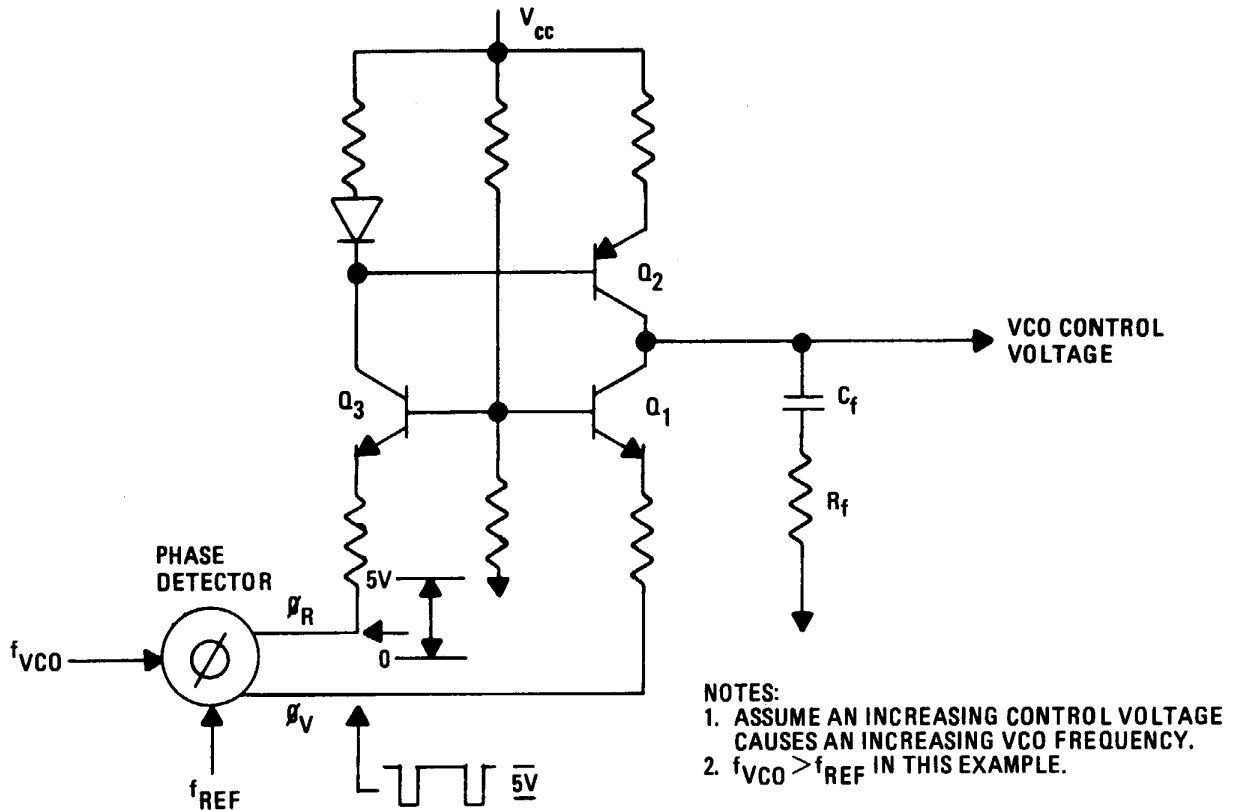
To produce a 100 kHz signal from the 50.7 MHz fVCO signal, a divisor ratio of  $(50.7 \div 100)$  or 507 is required. Table 4-2 shows a count sequence of 507 input pulses resulting in 1 output pulse. Similarly, a 50.7 MHz input results in a 100 kHz output.

The programmable  $\div N$  counter emits a pulse every time it counts 50 input pulses. With the swallow counter set to seven, the prescaler divides by 11, seven times, and then switches to dividing by 10. At this point, the  $\div N$  counter needs 43 input pulses before emitting an output pulse. The prescaler will now divide by 10, 43 times, to finish the count sequence. With seven counts of 11 ( $7 \times 11 = 77$ ) and 43 counts of 10 ( $43 \times 10 = 430$ ), one pulse emits from the programmable counter every  $(77 + 430)$  or 507 input pulses.



#### 4.3.4 Charge Pumps

The basic circuit employed in the RF-590 which converts the PLL phase comparator complementary pulse output error signals into an analog dc VCO control voltage is the charge pump. The three basic components of a charge pump circuit are a current source, a current sink, and an output filter. Figure 4-10 shows a typical charge pump circuit.



590-60(1)

Figure 4-10. Basic Charge Pump Circuit

##### 4.3.4.1 Phase Detector Outputs

The phase detector compares the phase and/or frequency of two inputs ( $f_{VCO}$  and  $f_{REF}$ ) and issues an output error signal at one of its two outputs ( $D_V$  or  $D_R$ ) whenever the inputs are not equal. The pulse widths of these output signals are directly proportional to the phase error of the two input signals.

If the frequency  $f_{VCO}$  is greater than  $f_{REF}$  or if the phase of  $f_{VCO}$  is leading, then error information is provided by  $D_V$  pulsing low.  $D_R$  remains essentially high (this is the situation shown in figure 4-10).

If the frequency  $f_{VCO}$  is less than  $f_{REF}$  or if the phase of  $f_{VCO}$  is lagging, then error information is provided by  $D_R$  pulsing low.  $D_V$  remains essentially high.

If the frequency of  $f_{VCO} = f_{REF}$  and both are in phase, then both  $\phi_V$  and  $\phi_R$  remain high, except for a small minimum time period when both pulse low in phase. (This time period is too small to affect the charge pump's lead-lag filter network Cf-Rf however, and is ignored.)

#### 4.3.4.2 Charge Pump Operation

The charge pump circuit functions as a current source/current sink network to lead-lag filter network Cf-Rf. Q2-Q3 function as a current source to dump charge into the filter network, while Q1 functions as a current sink to pull charge out of the network. The net result is that the output voltage across the network rises when Cf charges and falls when Cf discharges.

Assume that  $f_{VCO} > f_{REF}$  as shown in figure 4-10. Output  $\phi_R$  remains high, holding Q3 off. Output  $\phi_V$  pulses low, turning Q1 on. This provides a low impedance discharge path to ground for Cf. As Cf discharges, the charge pump output voltage (VCO control voltage) decreases, causing  $f_{VCO}$  to decrease.

Now assume that  $f_{VCO} < f_{REF}$ .  $\phi_V$  remains high, holding Q1 off.  $\phi_R$  pulses low, turning on Q3, and allowing Q2 to turn on and dump charge into Cf. This causes the VCO control voltage to increase, causing  $f_{VCO}$  to increase.

## SECTION 5

### MAINTENANCE

#### 5.1 INTRODUCTION

Section 5 contains information concerning general RF-590 repair, Built-In Test Equipment (BITE) description and fault code chart, overall receiver performance tests, and component data.

#### 5.2 PWB REPAIRS

The following general rules and techniques are useful in servicing RF-590 printed circuit boards.

- When replacing components on printed wiring boards (PWB), clip the mounting leads with a suitable pair of diagonal cutters and remove the component. This is especially helpful on multilead components such as the dual inline and circular type integrated circuits. The individual leads are then removed from the PWB with a low wattage iron.
- Before removing an integrated circuit from a PWB, note orientation of the pin locating tab and make sure the replacement component is reinstalled in exactly the same way.
- Because of the double sided construction used on many of the PWBs in the RF-590, a component lead may be soldered to printed circuit areas on the top and bottom of the PWB. Consequently, when a component lead is removed, the replacement component should be resoldered top and bottom as applicable.
- Overheating a printed circuit conductor may cause it to pull loose from the board material. Apply only the minimum amount of heat necessary for component removal or replacement. The use of a soldering iron in the 25 to 35 watt range is recommended.
- A desoldering tool (solder-sucker) is very convenient (and minimizes board damage) when removing multilead components which cannot be cut loose with diagonal cutters. Components of this type include special PWB transformers mounted on solderable leads and double balanced mixers, both used extensively in the various assemblies.
- A convenient device to use in place of a solder-sucker is a roll of Solder-Wick, manufactured by Solder Removal Co., Covina, California. This flux-saturated copper braid is often more effective than a solder-sucker for removing solder from PWBs.

#### 5.3 MOSFET REPLACEMENT

When handling and replacing Metal-Oxide Substrate Field-Effect Transistor (MOSFET) devices, the following three (3) steps should be performed.

- a. Remove new MOSFET from package. The four leads will be connected together with a small ferrule or wire to prevent static voltage differences from developing between the gate and substrate terminals. If the ferrule is present, wrap several turns of small solid wire around the leads and then remove the ferrule.
- b. Position the four leads and carefully install the MOSFET on the PWB.
- c. Remove the jumper(s) only after the leads have been soldered.

#### **5.4 CMOS HANDLING AND REPLACEMENT**

All Complementary Offset Symmetry Metal-Oxide Semiconductor (CMOS) devices have diode input protection against adverse electrical environments such as static electricity.

Although the devices contain circuitry to protect inputs against damage due to high voltages or electrical fields, precautions should be taken to avoid application of any voltage higher than maximum rated voltages.

Unfortunately, severe electrical conditions can develop during the process of handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range. This depends to a great extent upon the humidity, surface conditions, friction, and other factors. These static voltages are potentially disastrous when discharged into a CMOS input, considering the energy stored in the human body at these voltage levels.

Present CMOS gate protection structures can generally protect against overvoltages. However, these same structures will break down under severe conditions such as described above. The following are some suggested handling procedures for CMOS devices, many of which apply to most semiconductors.

- All CMOS devices should be stored or transported in materials that are conductive. CMOS devices must never be inserted into conventional plastic packing material or plastic trays.
- Avoid contact with the leads of the device. The component should always be handled very carefully by the ends or the side opposite the leads.
- Avoid contact between printed wiring board circuits or component leads and synthetic clothing while handling static sensitive devices or assemblies containing them.
- Do not insert or remove CMOS devices when power is applied. Check all power supplies to be used for testing CMOS devices to be certain that the voltage and polarity are correct, and that no transients are present.

- Use only soldering irons and tools that are properly grounded. Ungrounded soldering tips will destroy these devices. Never use soldering guns.

**NOTE**

When replacing CMOS devices in a PWB, it is recommended that the same procedures for replacing MOSFET devices be followed.

**5.5 BUILT-IN TEST EQUIPMENT (BITE) SELF DIAGNOSTICS**

The RF-590 has the capability of extensive self-testing in the event of a failure. The general types of tests and the assemblies affected are as follows:

- a. Control circuits tests
  - Control Board A14
  - Driver Board A13A2
  - Display Boards A13A4 and A13A5
  - Remote Control Board A17
  
- b. Frequency Synthesizer tests
  - Reference Generator A12 and Frequency Standard A21
  - BFO Assembly A11
  - PLL V Assembly A10
  - PLL IV Assembly A9
  - PLL III Assembly A8
  - PLL II Assembly A7
  - PLL I Assembly A6

c. Signal Path tests

- Input Filter Assembly A1
- First Converter Assembly A2
- Second Converter Assembly A3
- IF Filter Assembly A4
- IF/Audio Assembly A5A1
- AGC Assembly A5A2

d. Power Supply tests

- Power Supply Assembly A15

Most of these tests can be automatically performed by momentarily pressing the TEST button located on the receiver's front panel. Once the TEST button has been pressed, all receiver front panel controls (except AF GAIN, SPEAKER, and AUDIO LINE LEVEL) become inoperative, and the signal overload relay located on the A1 assembly deenergizes to prevent any possible spurious radiation of test signals during BITE diagnostics.

The normal length of the self-test is approximately 5 seconds. All tests are performed sequentially in their order of importance.

If it is determined that a fault exists in a particular assembly, that assembly number and the corresponding fault code number defining the type of failure will be displayed on the receiver's front panel alphanumeric display. (See table 5-1 for a listing of assembly numbers and fault codes). For example, if the reception of LSB signals became difficult (due to unknown reasons), initiate self-test by pressing TEST. The display, Assy 04 FAULT "02", would probably be shown. Table 5-1 indicates that this would be a fault due to IF Filter Assembly A4 LSB Filter.

If no faults were found during the self testing, the front panel will display ---TEST PASSED---

**NOTE**

A fault indication may be displayed at initial turn on and will remain on until the frequency standard stabilizes.

When interpreting Built-In Test (BIT) fault indications, do not overlook the possibility that the fault condition at the indicated module may be caused by a failure or marginal condition in an associated module.

**Table 5-1. Fault Code Listing**

Assembly Number	Fault Code	Description
A1	1	Antenna Overload
	2	Relay Fault (Closed)
	3	BITE Oscillator or A1 RF Det.
	4	Front End Filter
	5	Relay (Open) or dc Det. (TP5)
A2	1	A2 Detector
A3	1	A3 Detector
A4	1	Bypass Signal Path Fault (WBP Pad)
	2	LSB Filter
	3	USB Filter
	4	CW Filter
	5	CW Filter
	6	Special Filter - Slot 5
	7	Special Filter - Slot 6
	8	Special Filter - Slot 7
	9	A5 IF Input Peak Detector or A4 IF Amplifier and Output Circuitry
A5	1	A5 Gain
	2	AM Detector
	3	Line Audio

**Table 5-1. Fault Code Listing (Cont.)**

Assembly Number	Fault Code	Description
A5 (Cont.)	4	Product Detector
	5	FM Detector
A6	1	PLL I Out-of-Lock
A7	1	Serial Data
	2	PLL II Out-of-Lock
A8	1	Serial Data
	2	PLL III Out-of-Lock
A9	1	PLL IV Out-of-Lock
A10	1	Serial Data
	2	PLL V Out-of-Lock
A11	1	Serial Data
	2	BFO PLL Out-of-Lock
A12	1	1 MHz Reference
	2	800 kHz Reference
	3	40 MHz PLL Out-of-Lock
A13	No Fault Codes (Converter Module)	
A14	1	PROM Failure
	2	8155 RAM Failure
	3	CMOS RAM Failure
	4	Serial Data
	5	8155 Output Port Failure



**Table 5-1. Fault Code Listing (Cont.)**

Assembly Number	Fault Code	Description
A14 (Cont.)	6	8255 Output Port Failure
	7	A/D Conversion Timing Test
	8,9	A/D Converter Result Test
A15	No Fault Codes (Linear Power Supply)	
A17	1	LCU PROM
	2	LCU Communication
	3	LCU Interface
A18	1	A18 Peak Detector or A4 Output Failure
	2	A18 AGC Level Test
	3	A18 Line Audio Detector

### 5.5.1 Continuous Self-Test Monitoring

Certain critical circuits which may adversely affect receiver operation or even cause physical damage if they malfunction, are continuously monitored by the self diagnostics. These circuits are as follows:

- a. Power Supply A15. All power lines distributed to the receiver are continuously monitored for acceptable voltage limits.
- b. RF Input or Antenna Overload. The signal presented to the receiver from the antenna is constantly monitored so that signal path shut down circuits will protect the receiver from an input signal greater than approximately 1.5 Vrms.
- c. All Synthesizer Phase Lock Loops (PLL). These PLLs are continually monitored for a locked condition, indicating that the receive frequency stability is assured.

Any of the above mentioned items will cause a front panel FAULT LED to illuminate. Additionally, the RF signal overload would result in a front panel display of ANTENNA OVERLOAD.

## 5.5.2 Self Diagnostic Operation

The RF-590 self diagnostic tests are a series of sequential tests and measurements used to verify the proper operation of the RF-590. They are described in the following paragraphs. It may be necessary to consult the specific circuit schematics under discussion. These schematics are in the assembly subsections.

### 5.5.2.1 Lamp Test

The first test performed is a lamp test. All LEDs and segments of the 10 character and 20 character displays located on the front panel are lit. This condition is maintained for approximately 4 seconds for the operator to examine all front panel indicators and while the remainder of the receiver testing is being accomplished.

### 5.5.2.2 ROM Test (Assembly A14)

ROM test of Control Board Assembly A14 is the next test performed. U5, U6, and U19 contain all the firmware used to control the main receiver functions and are tested to determine that the information they contain is correct. If any of these are found to have a problem, the corresponding fault message will be displayed on the front panel. If at any time this fault is displayed, factory replacements should be obtained. These devices are factory programmed and cannot be repaired in the field.

### 5.5.2.3 RAM Test (Assembly A14)

The next test to be performed is the RAM test. This test will determine the read/write capability of the 2K CMOS RAM (U8) and 256 byte RAM of the 8155 (U7) located on Control Board Assembly A14. If it is determined that a fault exists, then the appropriate fault message will be displayed on the front panel.

### 5.5.2.4 I/O Port Tests

Parallel output ports of the A14 assembly are tested next. Output bit patterns are written to U7 and U9 ports, and then read back by the microprocessor to check the data bus path to these devices. If the bit pattern read back is not the same as written, a fault is noted.

### 5.5.2.5 Serial Data Test

The operation of the parallel-in/serial-out shift registers (U17, U18) on the Control Board and the capability of all synthesizers to accept serial data from the Control Board will now be tested. If a synthesizer fails to receive data correctly, then that assembly will be identified as having failed. If all synthesizers fail then it will be assumed that the Control Board is the faulty assembly.

The synthesizer PLLs are first loaded with all zeros and tested. They are then loaded with 00000000 00000000 001 binary. The one (1) bit will set the serial check line (SW1) of the PLLs to logic 1. This bit is then tested for all PLLs. If a fault occurs, the appropriate fault message will be displayed on the front panel.

### 5.5.2.6 Reference Generator Test (Assembly A12)

Reference Generator Assembly A12 will be tested next. The 40 MHz lock bit is read and tested for a lock condition (0 = lock). If detected as being out of lock, the proper fault code and assembly number will be displayed on the front panel.

The 1 MHz and 800 kHz detect lines are now read and if a logic 1 is read (indicating a fault), the appropriate fault code and the appropriate assembly number are displayed on the front panel.

### 5.5.2.7 A/D Converter Tests

The analog-to-digital converter used in the remaining BITE tests is now tested. A conversion is made to confirm that a result is available in approximately 100 microseconds (as indicated by the end-of-conversion output line). Readings are also obtained from two A/D channels tied to the +5 V and ground reference points, respectively. The conversion result bounds are checked. Failure of any of these three tests causes an A14 fault to be indicated.

### 5.5.2.8 Phase Locked Loop (PLL) Tests

The BFO PLL, PLL I, PLL II, PLL III, PLL IV, and PLL V are now tested to ensure that they can be tuned over their entire range. This testing is done in three steps. These three steps are shown in table 5-2.

**Table 5-2. BFO Tuning Range**

Range	Receiver Frequency	BFO Frequency
LOW	00,000.000 kHz	9.99 kHz
MID	15,050.500 kHz	0.00 kHz
HIGH	29,999.999 kHz	-9.99 kHz

At each frequency, all PLLs are tested to determine the status of their respective lock lines. They are tested in order starting with PLL V and finishing with BFO PLL. If a fault occurs as a result of these tests, the appropriate fault code and assembly number are displayed on the front panel.

### 5.5.2.9 Input Filter Test (Assembly A1)

Input Filter Assembly A1 will be tested next. This is done by testing the relay, the BITE oscillator, and front end filter.

First the input is tested for an overload condition. If an overload exists, then the test is terminated and an antenna overload message is displayed. If no overload exists, testing is continued.

The antenna relay is tested by energizing the relay, passing dc through it, and sampling the A1 dc detector to ensure that the signal path is complete. Sampling the A1 detector output (as well as the A2, A3, and A5 detector outputs) is done by an analog to digital converter (A/D) located on Control Board Assembly A14.

If this test fails, there will not be an immediate fault. The result is saved for future use during this test. The relay is then turned off using the relay control line and the BITE detector level is again tested. If a signal is still present, then the problem is in the relay or its associated control circuitry. If this is the case, a fault is reported indicating a relay failure.

If a fault condition is not detected, an RF test of the A1 assembly is performed by removing the dc relay test signal and activating the 100 kHz BITE oscillator. The BITE oscillator signal level at the output of the A1 assembly is -20 dBm. The A1 RF detector level is measured. If it is found that the output level is too low then the results of the relay test are checked. If the relay test also failed, then the fault is in the front end filter or the detector line to the A14 assembly. If the relay test passed, then the fault is in either the BITE oscillator or the RF detector. If the RF test is passed and the relay test failed, then the fault is either the relay or the dc detector.

#### 5.5.2.10 First Converter Test (Assembly A2)

After the A1 assembly has been found to be operating correctly, First Converter Assembly A2 is tested. It should be pointed out that the BITE oscillator was left activated from the previous test and will be used as a signal source during the testing of this assembly. The AGC is set to OFF, the RF GAIN is set to maximum and the receiver is tuned to 100 kHz. The A2 DET line is now read by the A/D converter and the results tested to ensure the level is correct. If a fault occurs as a result of this test, the A2 assembly will be flagged as the faulty module and the appropriate fault code will be displayed.

#### 5.5.2.11 Second Converter Test (Assembly A3)

If the First Converter is operating correctly then the Second Converter module is tested. AGC, RF GAIN, and BITE oscillator are in the same state as used in the testing of the First Converter. Since all conditions are set up, it is only necessary to measure the A3 detector level using the A/D converter and to verify the correct level. If the level is incorrect, the appropriate fault information will be displayed.

#### 5.5.2.12 IF Filter Test (Assembly A4)

After it has been determined that the Second Converter is operating satisfactorily, IF Filter Assembly A4 can be tested. FSK filters will not be tested because of the wide variety of center frequencies and shifts available. The BITE test oscillator located on the A1 assembly will be disabled at this time. A signal generated by the first LO (via signal leakage through the First Converter A2 mixer) will be used. (The first LO signal is used to obtain better frequency accuracy for some of the narrow bandwidth filters that may be present in IF Filter Assembly A4.)

First the 16 kHz bypass path is tested to verify that a signal can be passed through the filter assembly amplifiers to the peak detector located on the input of IF/Audio Assembly A5. The 16 kHz bypass is selected and the level of the peak detector is read by the A/D converter. The results of this test are stored until after the USB filter is tested since, at this time, there could be a problem in either the A4 bypass circuitry or a problem in the A5 input peak detector.

To pinpoint any possible problem, the receiver will now be tuned to set the first LO to 40.454 MHz. This will generate a 1 kHz USB tone. USB filter (BW2) will be selected and the peak detector output read using the A/D converter. If a fault exists, then the results of the 16 kHz bypass test will be examined to pinpoint the fault. If the USB filter test passed but the bypass test indicated a fault, then the bypass path is flagged as the faulty circuit. If the USB filter test failed and the bypass path test passed, then the USB filter is identified as the faulty circuit. If both of these tests failed, then the fault is identified as being either the A5 peak detector or the A4 filter amplifiers and their associated circuitry. If the test results indicate that both are operating correctly, then testing the remaining filters installed in the A4 assembly continues.

The LSB filter (BW1) is tested by tuning the first LO to a frequency of 40.456 MHz and enabling the A4 LSB filter slot. A 1 kHz LSB tone is generated, detected by the A5 input peak detector, and measured by the A14 A/D converter. If a fault exists, the LSB filter is identified as the faulty circuit.

Next the CW filter slot (BW3) is tested. The first LO is tuned to 40.455 MHz and the CW filter slot is enabled. The level of the peak detector is read by the A/D converter. If the level monitored indicates that a problem exists, then the CW filter (BW3) is identified as being the faulty circuit.

The CW filter slot (BW4) is now tested. The same procedure is used to test this filter as was used to test BW3 CW filter. If a problem exists, then this CW filter (BW4) is identified as being the faulty circuit.

Filter slots 5, 6, and 7 may have a variety of filters installed. The only types of filters allowed in these slots are AM, FM, CW, or FSK. Since FSK filters will not be tested and AM, FM, and CW can all be tested at the same frequency, we only need to determine if a filter is present and whether or not it is an FSK type. Testing is identical to that of the CW filters, BW3, and BW4. If a problem exists in any of these filters, the appropriate fault message is displayed.

#### NOTE

The eight pole dip switch (S2) located on the A14 assembly must be set correctly for the above test to be performed correctly. This switch is set at the factory (based on the filter configuration of the A4 assembly) and should not be altered.

#### 5.5.2.13 IF Audio Test (Assembly A5)

IF/Audio Assembly A5 is now tested to determine that the SSB, AM, and FM detectors are operating correctly. The A4 filter is set to select the 16 kHz bypass path. The AGC speed is set to MEDIUM, the mode is set to USB, and the A1 assembly BITE test oscillator is enabled.

The receiver is first tuned to 104.000 kHz. Since the BITE oscillator has a frequency of 100 kHz, a 4 kHz USB tone will result. The second IF AMP GAIN is tested by measuring the AGC voltage through the A/D converter. If the level is incorrect, an AGC fault is displayed on the front panel of the receiver. If this level is satisfactory, then the product detector is tested. The BITE test oscillator is disabled and the receiver is tuned to 4 kHz. The results of this test are stored since there could be a problem in either the line audio circuits or the USB product detector (if a fault indication is detected).

The AM test is now performed. With the receiver tuned to 4 kHz, the receiver mode is set to AM. The 16 kHz bypass is again used for this test. To simulate an AM signal, the receiver will be tuned repetitively from 4 kHz to 100 kHz using LO No. 2 leakage as a signal source. The line audio level is measured to verify that the AM detector is operational. The results of this test and those of the SSB test are compared to determine where possible faults may have occurred. Table 5-3 shows the results of this test and that of the SSB test.

**Table 5-3. AM and SSB Test Results and Fault Locations**

AM and SSB Test Results	Fault Location
If AM passed and SSB passed	no fault
If AM passed and SSB failed	product detector fault
If AM failed and SSB passed	AM detector fault
If AM failed and SSB failed	line audio fault

The next test concerned with the A5 assembly is the FM detector test. The receiver is set to FM mode and tuned to a frequency of 5 kHz. The receiver will then be tuned from +5 kHz to -5 kHz repetitively to simulate a FM signal using LO No. 1 leakage as a signal source. The line audio will be read through the A/D converter. If a problem exists, the appropriate fault message is displayed on the front panel of the receiver.

#### 5.5.2.14 ISB Test (Assembly A18, If Installed)

ISB option assembly A18 (if installed) is now tested to determine that the IF Peak Detector, ISB AGC, and ISB Line Audio Detector are operating correctly.

Filter Assembly A4 is first set to select the LSB filter. Next, the receiver mode is set to ISB and the RF GAIN is set to maximum. The 100 kHz bite oscillator located on Input Filter Assembly A1 is now activated and the receiver is tuned to 95 kHz (resulting in a LSB frequency of 5 kHz).

Now the ISB Peak Detector level is sampled to determine whether an inband ISB signal has been found (level greater than 1 volt dc). If this level is not found, the frequency of the receiver is increased 200 Hz and the detector level is checked again. This process is repeated until the correct level is found or until the receiver frequency is greater than 115 kHz.

If the frequency is greater than 115 kHz, the no inband tone was found so it is assumed that the input peak detector has failed or the signal path between Filter Assembly A4 and the A18 ISB Assembly has been interrupted. If this is true, the fault code for the A18 Peak Detector will be displayed on the receiver front panel and no further testing of the assembly will take place.

If the inband tone was found, the frequency is increased by 1.5 kHz, placing the tone in the center of the LSB filter.

Once the receiver is tuned, the peak detector, AGC detector, and line audio detector levels are measured to verify their operation. If any of these are found to be at an improper level, the appropriate fault code will be displayed on the receiver front panel and all further receiver testing is aborted.

If the three levels are found to be correct, then the assembly is considered to be functioning correctly.

#### 5.5.2.15 LCU Test (Assembly A17)

The last thing to be tested during self-test is Remote Control Assembly A17. The information used to control these tests is contained within the remote control assembly firmware. If it is determined that the remote control assembly is installed, the remote control assembly will test the UART, the LCU ROM (U7), and the RS-422 interface. If any of these are found to be at fault, then the corresponding fault information is displayed on the front panel. The LCU also reports, to the remote site, any self-test pass/fail conditions that may occur as a result of the TEST function being performed.

Upon completion of the self-test, if no fault has occurred, a — — — TEST PASSED — — — message is displayed indicating to the operator that the radio is operating satisfactorily.

#### 5.5.3 Self Diagnostics Sequence Summary

The RF-590 self diagnostics are done in the order of assembly importance. If a fault is discovered during testing, this failure must be corrected before the remaining tests are attempted.

The order of testing from the first to last test is shown in table 5-4.

**Table 5-4. Self Diagnostics Sequence Summary**

1. ROM Test — Assembly A14
2. RAM Test — Assembly A14
3. Output Port Test — Assembly A14
3.1 8155 Ports B, C
3.2 8255 Port A

**Table 5-4. Self Diagnostics Sequence Summary (Cont.)**

<p>4. Serial Data Tests</p> <p>4.1 Assembly A14</p> <p>4.2 Assembly A11</p> <p>4.3 Assembly A7</p> <p>4.4 Assembly A10</p> <p>4.5 Assembly A8</p>
<p>5. Reference Generator Tests – Assembly A12</p> <p>5.1 40 MHz Phase locked loop</p> <p>5.2 1 MHz Reference</p> <p>5.3 800 kHz Reference</p>
<p>6. Phase Locked Loops</p> <p>6.1 Assembly A10 - PLL V</p> <p>6.2 Assembly A9 - PLL IV</p> <p>6.3 Assembly A8 - PLL III</p> <p>6.4 Assembly A7 - PLL II</p> <p>6.5 Assembly A6 - PLL I</p> <p>6.6 Assembly A11 - BFO PLL</p>
<p>7. A/D Converter Test – Assembly A14</p> <p>7.1 Conversion Timing Test</p> <p>7.2 +5 Reference Measurement</p> <p>7.3 Gnd Reference Measurement</p>
<p>8. Input Filter Test – Assembly A1</p> <p>8.1 Antenna overload test</p> <p>8.2 Dc signal test</p> <p style="padding-left: 20px;">8.2.1 Relay closed</p> <p style="padding-left: 20px;">8.2.2 Relay open</p>



**Table 5-4. Self Diagnostics Sequence Summary (Cont.)**

<p>8.3 RF signal test</p> <p style="text-align: center;"><b>NOTE</b></p> <p>If both tests 8.2.1 and 8.3 fail then it is assumed that the filter is faulty.</p>
<p>9. First Converter Test – Assembly A2</p>
<p>10. Second Converter Test – Assembly A3</p>
<p>11. IF Filter Tests – Assembly A4</p> <p>11.1 16 kHz Bypass Test</p> <p>11.2 USB Filter Test</p> <p style="text-align: center;"><b>NOTE</b></p> <p>If both tests 11.1 and 11.2 fail then it is assumed that either the IF amplifier or the A5 assembly peak detector is faulty.</p> <p>11.3 LSB Filter Test</p> <p>11.4 CW Filter Test</p> <p>11.5 CW Filter Test</p> <p>11.6 Special Filter 5 Test</p> <p>11.7 Special Filter 6 Test</p> <p>11.8 Special Filter 7 Test</p> <p style="text-align: center;"><b>NOTE</b></p> <p>Tests 11.6, 11.7, and 11.8 are done only if filters are installed and if they are not FSK filters.</p>
<p>12. IF/Audio Test – Assembly A5</p> <p>12.1 AGC Test</p> <p>12.2 SSB Noise Test</p> <p>12.3 SSB Signal Test</p>

**Table 5-4. Self Diagnostics Sequence Summary (Cont.)**

<p>12.4 AM Noise Test</p> <p>12.5 AM Signal Test</p> <p style="text-align: center;"><b>NOTE</b></p> <p>If both test 12.3 and 12.5 fail then it is assumed that the line audio detector is faulty.</p> <p>12.6 FM Noise Test</p> <p>12.7 FM Signal Test</p>
<p>13. ISB Test – Assembly A18 (If Installed)</p> <p>13.1 Peak Detector</p> <p>13.2 AGC Test</p> <p>13.3 Line Audio Detector</p>
<p>14. Remote (LCU) Test – Assembly A17 (If Installed)</p> <p>14.1 PROM Test</p> <p>14.2 Communications Test</p> <p>14.3 Interface Test</p>

## 5.6 RECEIVER PERFORMANCE TEST PROCEDURES

Table 5-5 shows tests used to verify RF-590 operation.

**Table 5-5. RF-590 Test Procedures**

Test	Paragraph
Local Control Function Test	2.7
Sensitivity	5.6.1

**Table 5-5. RF-590 Test Procedures (Cont.)**

Test	Paragraph
Audio Output Level and Distortion	5.6.2
AGC Range	5.6.3
Ultimate Quieting	5.6.4
IF Filter Selectivity	5.6.5

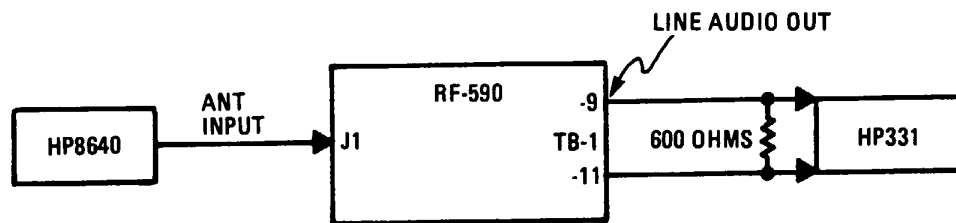
**5.6.1 Sensitivity Test**

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Audio Distortion Analyzer
- 600 Ohm Feedthrough Termination

The following steps describe the sensitivity test procedure.

- a. Connect equipment as shown in figure 5-1.



590-44(1)

**Figure 5-1. Sensitivity Test Setup**

- b. Initially set receiver's AGC to OFF and RF GAIN to maximum.
- c. Perform steps d through f for each of the modes and bandwidths listed in table 5-6.
- d. Set generator for a minimum RF output.
- e. Adjust audio distortion analyzer sensitivity for a convenient reference indication.

**HARRIS**  
**RF COMMUNICATIONS**

- f. Adjust generator output until the audio output rises 10 dB above the reference noted in step e. Record the signal generator output level in table 5-6. Note that this value must be no greater than the maximum allowable 10 dB  $\frac{S + N}{N}$  sensitivity listed.

N

**NOTE**

Generator frequencies may be varied within the passband range to obtain a peak audio output in the channel being tested.

**NOTE**

In AM mode, it will be necessary to set the signal generator for 50 percent modulation at the modulation frequency indicated. Increase carrier power until a 10 dB difference above the reference level is obtained between modulation OFF and modulation ON.

**NOTE**

In FM mode, set the generator for 4.7 kHz deviation at the modulation frequency indicated. Increase carrier power until a 17 dB difference is obtained on the audio voltmeter between modulation OFF and modulation ON.

**Table 5-6. Sensitivity Test Reports**

Mode	BW kHz	Radio Frequency MHz	Generator Frequency MHz	Modulation Frequency kHz	*Maximum 10 dB $\frac{S + N}{N}$ Sensitivity $\mu$ Vrms	Measured 10 dB $\frac{S + N}{N}$ Sensitivity $\mu$ Vrms
LSB	3.2	2.000000	1.999000	—	.35	_____
		16.000000	15.999000	—	.35	_____
		29.999999	29.999000	—	.35	_____
USB	3.2	2.000000	2.001000	—	.35	_____
		16.000000	16.001000	—	.35	_____
		29.999999	30.001000	—	.35	_____
CW	.3	2.000000	2.000150	—	.15	_____
		16.000000	16.000150	—	.15	_____
		29.999999	30.000150	—	.15	_____
CW	1.0	2.000000	2.000500	—	.25	_____
		16.000000	16.000500	—	.25	_____
		29.999999	30.000500	—	.25	_____

**Table 5-6. Sensitivity Test Reports (Cont.)**

Mode	BW kHz	Radio Frequency MHz	Generator Frequency MHz	Modulation Frequency kHz	*Maximum 10 dB $\frac{S+N}{N}$ Sensitivity uVrms	Measured 10 dB $\frac{S+N}{N}$ Sensitivity uVrms
AM	3.2	2.000000	2.000000	1.0	1.25	_____
		16.000000	16.000000	1.0	1.25	_____
		29.999999	29.999999	1.0	1.25	_____
AM	6.0	2.000000	2.000000	1.0	1.5	_____
		16.000000	16.000000	1.0	1.5	_____
		29.999999	29.999999	1.0	1.5	_____
FM	16.0	2.000000	2.000000	1.0	2.0	_____
		16.000000	16.000000	1.0	2.0	_____
		29.999999	29.999999	1.0	2.0	_____

\* = These numbers double when the RF-596-02 Preselector option is installed.

### 5.6.2 Audio Output Level and Distortion Test

The following test equipment is required to perform this test.

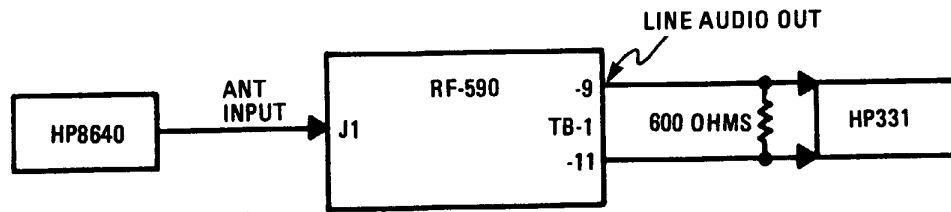
- HP-8640B Signal Generator
- HP-331A Distortion Analyzer
- 600 Ohm Feedthrough Termination
- 8 Ohm 5 Watt Termination

Use the following procedures to check line output, headphone output, and speaker output.

#### 5.6.2.1 Line Output Check

To check the line input proceed as follows:

- a. Set signal generator to -20 dBm, 2.001500 MHz. Set receiver to 2.000000 MHz, AGC to MEDIUM, Mode to USB, and RF GAIN to maximum.
- b. Connect equipment as shown in figure 5-2.



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Figure 5-2. Line Audio Test Setup

- c. Measure line audio output level. Level must be adjustable from -16 dBm (.123 Vrms) to +10 dBm (2.45 Vrms) (.1 mW to 10 mW). Record range in table 5-7.

Table 5-7. Audio Output Level and Distortion Test Report

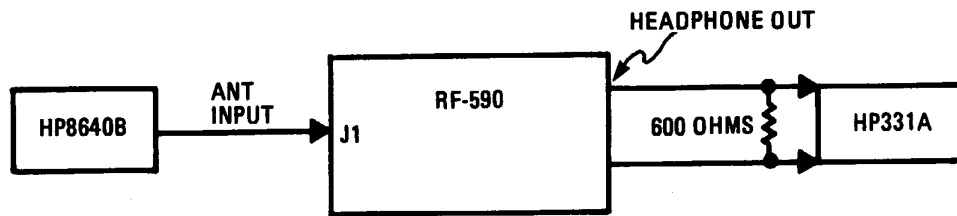
Test	Output Level Measured Vrms	Output Level Limits Vrms	Distortion Measured dBc	Distortion Limits dBc
Line Audio		.123 to 2.45 Minimum		-40
Headphone Audio		2.45 Minimum		-40
Speaker Audio		4.0 Minimum		-26

- d. Set line audio level to 2.45 Vrms. Measure total harmonic distortion (THD). THD must be at least -40 dBc (1% maximum). Record in table 5-7.
- e. Reset line audio level to .775 Vrms (0 dBm). Check that the RF-590 front panel meter indicates 0 dBm  $\pm$  2 dB.

### 5.6.2.2 Headphone Output Check

To check the headphone output proceed as follows:

- a. Set signal generator to -20 dBm, 2.001500 MHz. Set receiver to 2.000000 MHz, AGC to MEDIUM, Mode to USB, and RF GAIN to maximum.
- b. Connect equipment as shown in figure 5-3.



590-43(2)

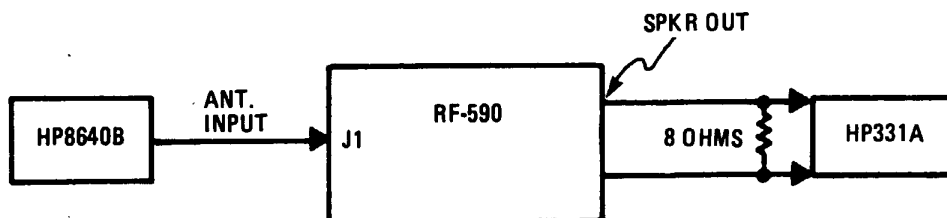
**Figure 5-3. Phone Audio Test Setup**

- c. Set speaker to OFF. Adjust AF GAIN control for maximum output. Headphone output level must be 2.45 Vrms (10 mV) minimum. Record in table 5-7.
- d. Measure Total Harmonic Distortion at 2.45 Vrms output. THD must be at least -40 dBc (1% maximum). Record in table 5-7.
- e. Readjust AF GAIN to minimum.

### 5.6.2.3 Speaker Output Check

To check speaker output proceed as follows:

- a. Set signal generator to -20 dBm, 2.00150 MHz. Set receiver to 2.000000 MHz, AGC to MEDIUM, Mode to USB, and RF GAIN to maximum.
- b. Connect equipment as shown in figure 5-4.



590-50(2)

**Figure 5-4. Speaker Audio Test Setup**

**NOTE**

It will be necessary to disconnect the audio lines to the speaker and connect them to the 8 ohm load to perform this test.

- c. Set speaker to ON, and adjust AF GAIN to maximum. Speaker audio output level must be 4.0 Vrms (2.0 W) minimum. Record in table 5-7.
- d. Measure total harmonic distortion (THD) at 4.0 Vrms output. THD must be at least -26 dBc (5% maximum). Record in table 5-7.
- e. Set speaker to OFF, AF GAIN to minimum. Disconnect 8 ohm load and reconnect speaker.

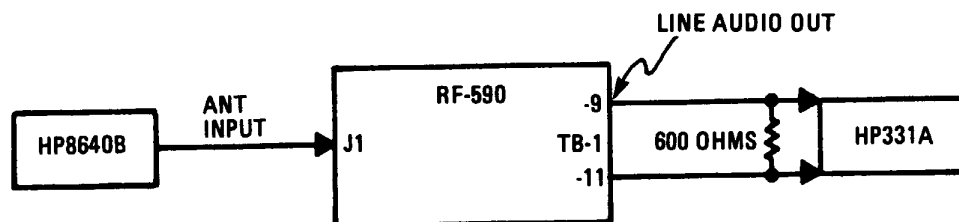
### 5.6.3 AGC Range

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Audio Distortion Meter
- 600 Ohm Feedthrough Termination

Use the following procedures to perform the AGC range test.

- a. Connect equipment as shown in figure 5-5.



590-44(2)

Figure 5-5. AGC Range Test Setup

- b. Set signal generator to 10.001500 MHz and RF output level at 2 uVrms.
- c. Set AGC to MEDIUM, RF GAIN to maximum, Mode to USB, Receive Frequency to 10.000000 MHz, BFO to 0.00 kHz, and Line Audio Output to 0 dBm.
- d. Set a convenient reference level on the distortion analyzer, and then increase signal generator output to 1 Vrms. The audio output level should not increase by more than 3 dB. Record level change below.

Total Audio Output Level Change: \_\_\_\_\_ dB (3 dB maximum)  
(RF input level 2 uVrms to 1 Vrms)



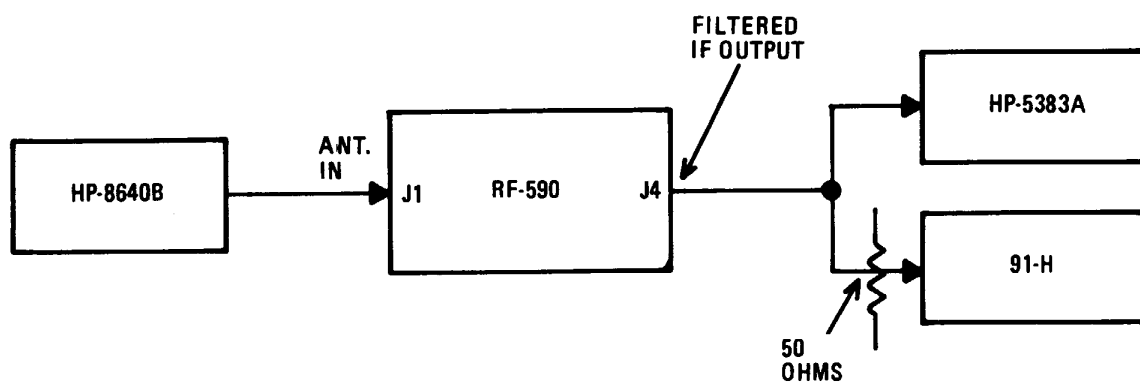
### 5.6.4 IF Filter Selectivity

The following test equipment is required for this test:

- HP-8640B Signal Generator
- Boonton Model 91-H RF Millivoltmeter with 50 ohm adapter.
- HP-5383A Frequency Counter

Use the following procedures to verify filter IF response.

- a. Initially set receiver to 10.000,000 MHz, AGC to OFF, BFO to 0.00 kHz, and MODE to USB. Connect equipment as shown in figure 5-6.



590-80

**Figure 5-6. IF Filter Selectivity Test Setup**

- b. Set signal generator frequency  $f_o$  to 10.0015 MHz. Adjust generator output to set a convenient millivoltmeter reference level in the generator's -110 dB range (i.e., below the receiver's AGC threshold).
- c. Vary the generator frequency  $\pm 10$  kHz and note the IF output -3 dB roll-off frequencies. (Note that only one major, distinct peaked response should occur for any selected filter. However there may be some passband ripple.) Calculate the -3 dB bandwidth as the difference between these frequencies. Record in table 5-8.
- d. Note the passband ripple as the difference in IF output maxima and minima values between the -3 dB frequencies. Check (✓) table 5-9 if ripple  $\leq 3$  dB.
- e. Repeat steps b through d for the generator frequencies ( $f_o$ ), IF filter modes, and BWs listed in table 5-8.

**Table 5-8. IF Filter Response Test Report**

Generator Reference Level Frequency $f_0$ MHz	Mode	Filter Bandwidth, kHz		Passband Ripple	
		(Minimum)	Measured	Maximum dB	Measured dB
10.00150	USB	2.8		3	
9.99850	LSB	2.8		3	
10.0000	CW	.30		3	
10.0000	CW	1.0		3	
10.0000	AM	3.2		3	
10.0000	AM	6.8		3	
10.0000	AM	16		3	

**5.7 COMPONENT DATA SHEETS**

This section contains any applicable data sheets for the RF-590. They can be used for reference purposes and are listed alphabetically.



# Am26LS31

## Quad High Speed Differential Line Driver

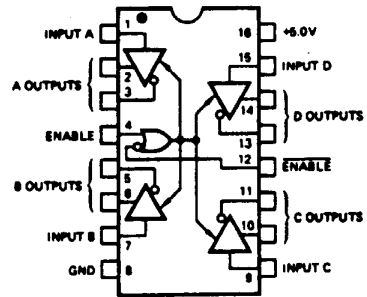
### FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

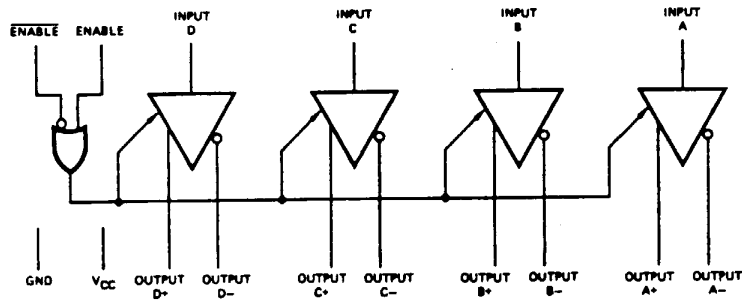
The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

**CONNECTION DIAGRAM  
(Top View)**



**LOGIC DIAGRAM**



# Am26LS33

## FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

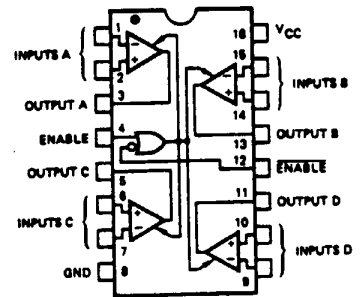
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of  $\pm 7V$ .

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of  $\pm 15V$ .

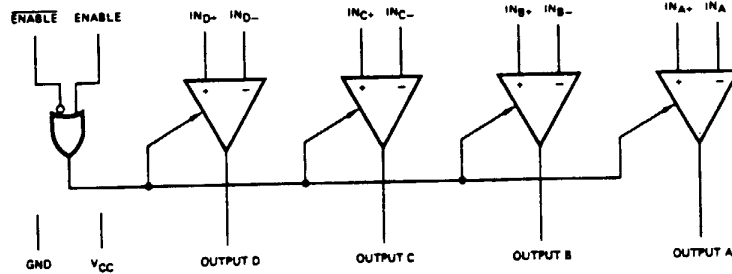
The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

**CONNECTION DIAGRAM**  
Top View



**LOGIC DIAGRAM**



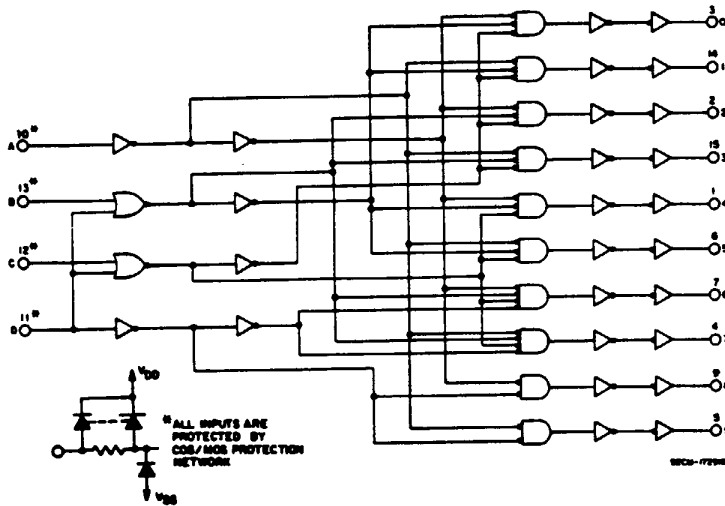
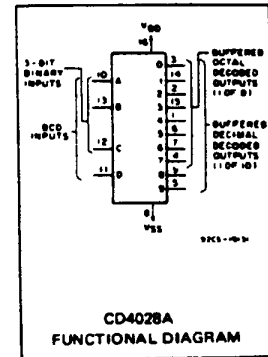


## CD4028A Types COS/MOS BCD-to-Decimal Decoder

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs

0 through 7 to go low. If unused, the D input must be connected to VSS. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



**TABLE I - TRUTH TABLE**

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	1	0
1	1	0	1	0	0	0	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	0	0	0	0	0	0	1

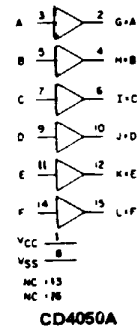
\* WHERE 1 = HIGH LEVEL  
0 = LOW LEVEL

\*\* EXTRAORDINARY STATES

## CD4050A

### COS/MOS Hex Buffer/Converters

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage ( $V_{CC}$ ). The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{CC}$  supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. ( $V_{CC}=5V$ ,  $V_{OL} \geq 0.4V$ , and  $I_{DN} \geq 3.2mA$ .)



## CD4053B

### COS/MOS Analog Multiplexers/Demultiplexers

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if  $V_{DD}-V_{SS} = 3$  V, a  $V_{DD}-V_{EE}$  of up to 13 V can be controlled; for  $V_{DD}-V_{EE}$  level differences above 13 V, a  $V_{DD}-V_{SS}$  of at least 4.5 V is required). For example, if  $V_{DD} = +5$  V,  $V_{SS} = 0$ , and  $V_{EE} = -13.5$  V, analog signals from  $-13.5$  V to  $+4.5$  V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full  $V_{DD}-V_{SS}$  and  $V_{DD}-V_{EE}$  supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

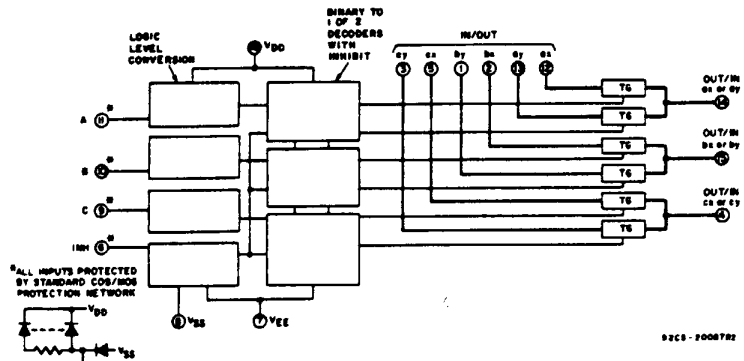
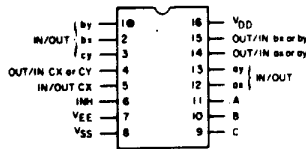


Fig. 3 - Functional diagram of CD4053B.

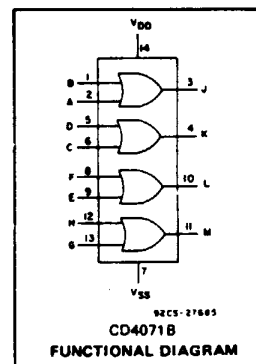


CD4053B  
Terminal Assignment

## CD4071B

### COS/MOS QUAD 2-INPUT OR GATE

The RCA-CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates. The CD4071, CD4072, and CD4075 types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).



CD4071B  
FUNCTIONAL DIAGRAM



## CD4094B

### COS/MOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the  $Q_5$  serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the  $Q_5$  terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

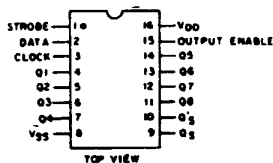
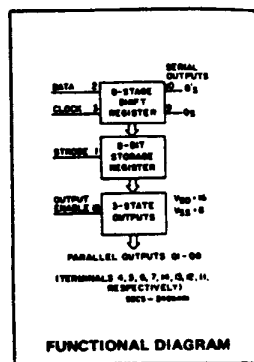


Fig. 1 - Terminal assignment.

TRUTH TABLE

CL <sup>a</sup>	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q2	Q5*	Q6
Level Change	0	X	X	OC	OC	Q7	NC
Level Change	0	X	X	OC	OC	NC	Q7
Level Change	1	0	X	NC	NC	Q7	NC
Level Change	1	1	0	0	Q <sub>N-1</sub>	Q7	NC
Level Change	1	1	1	1	Q <sub>N-1</sub>	Q7	NC
Level Change	1	1	1	NC	NC	NC	Q7

<sup>a</sup> - Level Change  
X - Don't Care  
NC - No Change  
OC - Open Circuit

Logic 1 = High  
Logic 0 = Low

\* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the  $Q_5$  output

## CD4098B Types

### COS/MOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

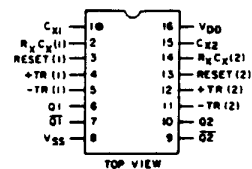
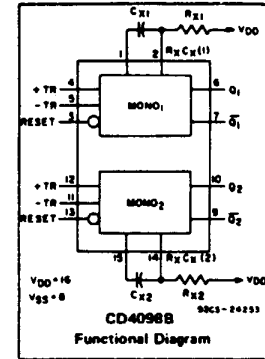
The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor ( $R_X$ ) and an external capacitor ( $C_X$ ) control the timing for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of  $R_X$  and  $C_X$ .

Leading-edge-triggering (+TR) and trailing edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode,  $\bar{Q}$  is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used.

The time period (T) for this multivibrator can be approximated by:  $T_X \approx \frac{1}{2} R_X C_X$  for  $C_X \geq 0.01 \mu F$ .



TERMINALS 1, 8, 15 ARE  
ELECTRICALLY CONNECTED  
INTERNALLY

92CS-24048R1  
**TERMINAL ASSIGNMENT**

## CD4514B

### COS/MOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)  
CD4514B Output "High" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0 (CD4514B) or 1 (CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are similar to industry types MC14514 and MC14515.

The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

**DECODE TRUTH TABLE (Strobe = 1)**

INHIBIT	DECODER INPUTS				SELECTED OUTPUT
	D	C	B	A	CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low

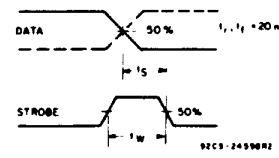
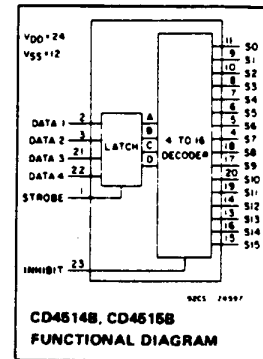
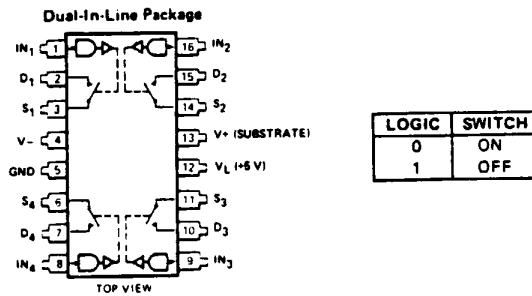


Fig. 14 - Waveforms for setup time and strobe pulse width.

# DG211 Quad Monolithic SPST CMOS Analog Switch

The DG211 is a 4-channel single pole single throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

## PIN CONFIGURATION



SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

# HM-6516

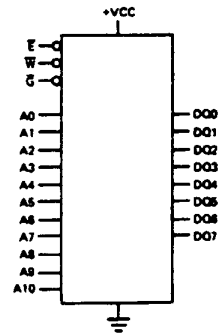
## 2K x 8 CMOS RAM

### Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times.

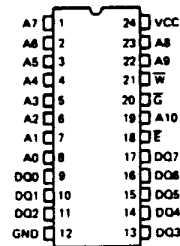
The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus, such as the 8085. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

### Logic Symbol



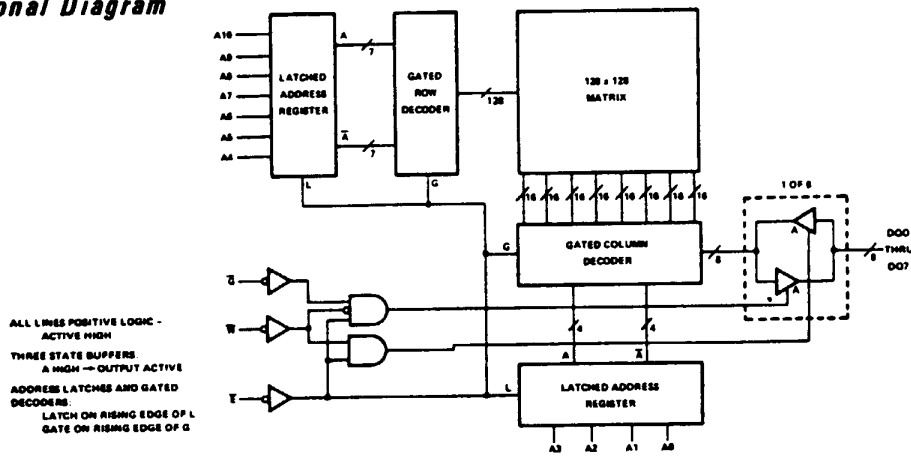
### Pinout

TOP VIEW



- A Address Input
- DQ Data Input/Output
- E Chip Enable
- G Output Enable
- W Write Enable

### Functional Diagram



## LM211 Voltage Comparator

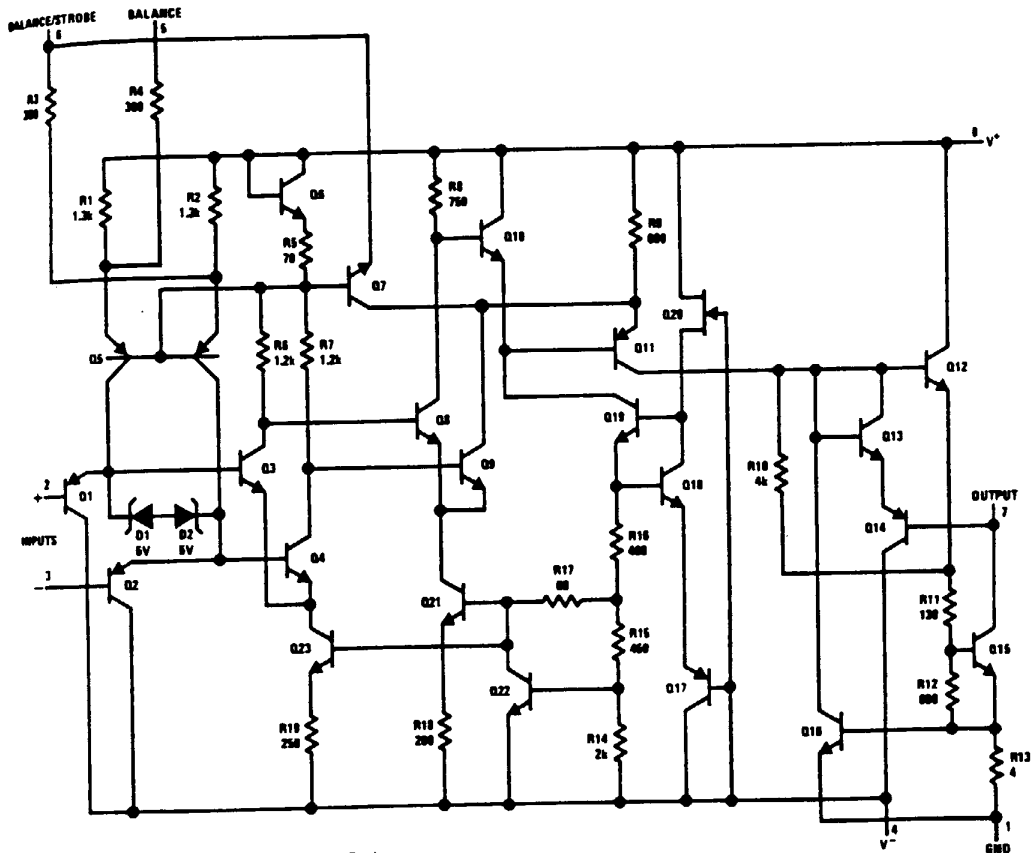
### General Description

The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard  $\pm 15V$  op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA. Outstanding characteristics include:

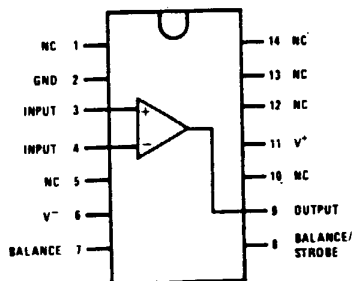
- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature

- Differential input voltage range:  $\pm 30V$
- Power consumption: 135 mW at  $\pm 15V$

Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed.



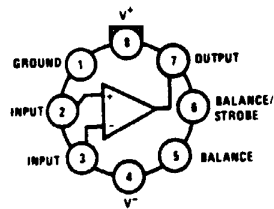
Dual-In-Line Package



Note: Pin 6 connected to bottom of package.

TOP VIEW

Metal Can Package



NOTE: Pin 4 connected to case.

TOP VIEW

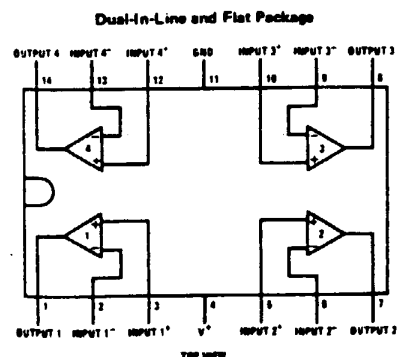
## LM324 Low Power Quad Operational Amplifiers

### General Description

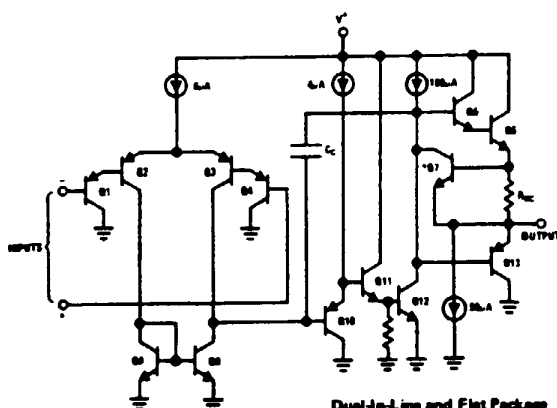
The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V<sub>DC</sub> power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V<sub>DC</sub> power supplies.

### Connection Diagram



### Schematic Diagram (Each Amplifier)

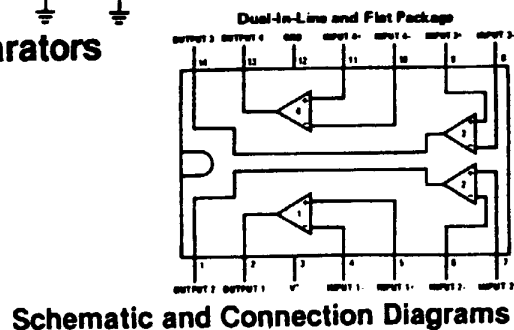


## LM339 Low Power Low Offset Voltage Quad Comparators

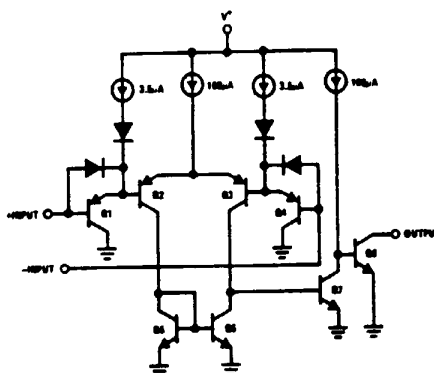
### General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic—where the low power drain of the LM339 is a distinct advantage over standard comparators.



### Schematic and Connection Diagrams

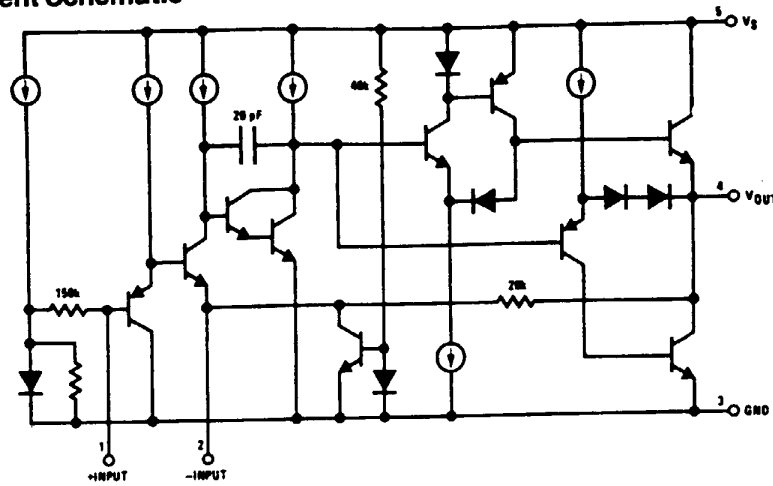


## LM383/LM383A 8 Watt Audio Power Amplifier

### General Description

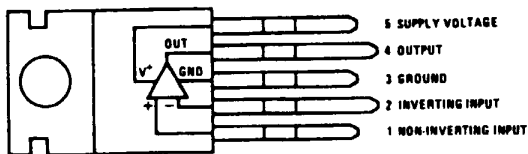
The LM383 is a high power amplifier. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM383 is current limited and thermally protected. High voltage protection is available (LM383A) which enables the amplifier to withstand 40V transients on its supply. The LM383 comes in a 5-pin TO-220 package.

### Equivalent Schematic



### Connection Diagram

TO-220 Plastic Package



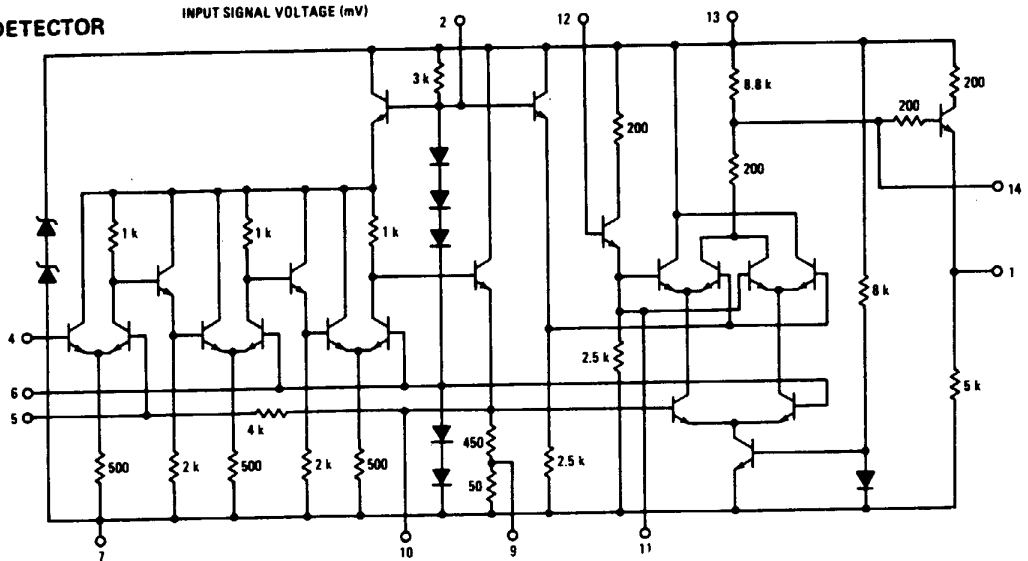




# MC1357

FIGURE 1 - CIRCUIT SCHEMATIC

## QUADRATURE DETECTOR



• A Direct Replacement for the ULN2111A

• Greatly Simplified FM Demodulator Alignment

Typical Performance:  
2 Watts Output  
2% Distortion  
250  $\mu$ V Sensitivity (3 dB Lim.)

C1 = 120 pF  
L1 = 14  $\mu$ H  
R1 = 20 k $\Omega$   
Q = 30

# MC1458

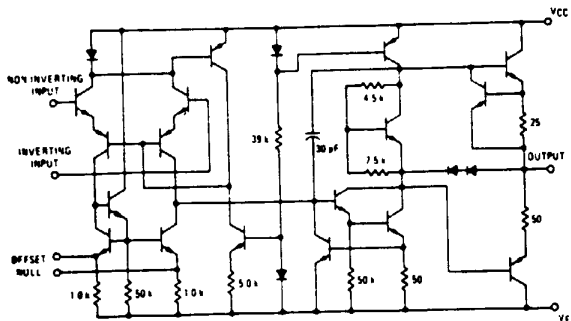
• Excellent Performance at  $V_{CC} = 8.0$  Vdc

## DUAL OPERATIONAL AMPLIFIERS

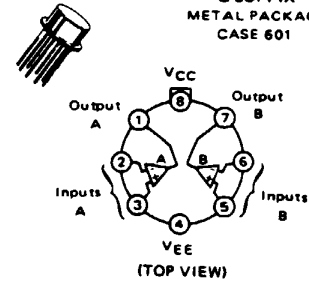
... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered - N Suffix

### EQUIVALENT CIRCUIT SCHEMATIC



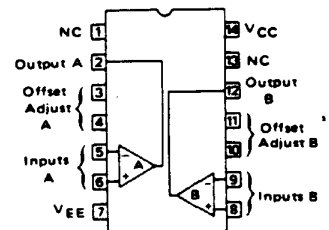
**G SUFFIX**  
METAL PACKAGE  
CASE 601



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 632  
TO-116



**P2 SUFFIX**  
PLASTIC PACKAGE  
CASE 646  
(MC1458, MC1458C, MC1458N)



# MC1488

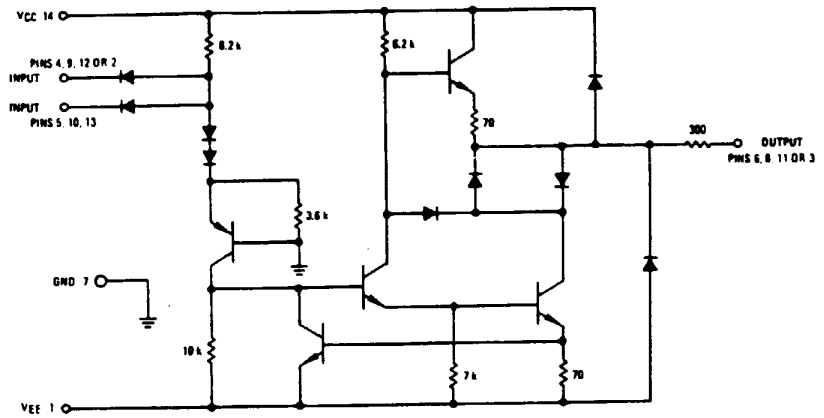
## QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

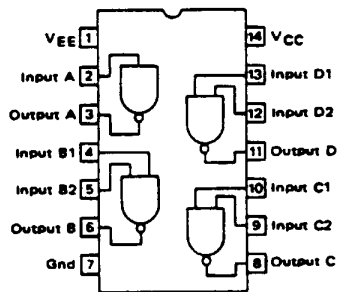
**Features:**

- Current Limited Output  
±10 mA typ
- Power-Off Source Impedance  
300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

**CIRCUIT SCHEMATIC**  
(1/4 OF CIRCUIT SHOWN)



**PIN CONNECTIONS**

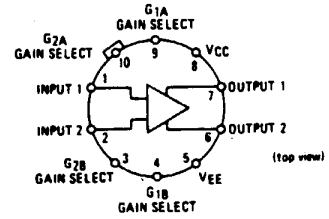


# MC1733

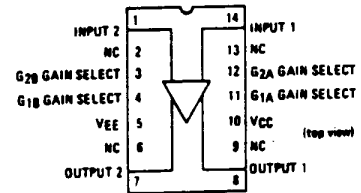
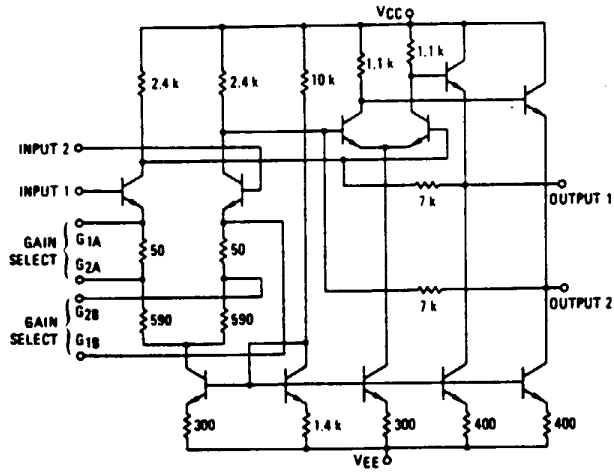
## DIFFERENTIAL VIDEO AMPLIFIER

... a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth – 120 MHz typical @  $A_{vd} = 10$
- Rise Time – 2.5 ns typical @  $A_{vd} = 10$
- Propagation Delay Time – 3.6 ns typical @  $A_{vd} = 10$



**EQUIVALENT CIRCUIT SCHEMATIC**

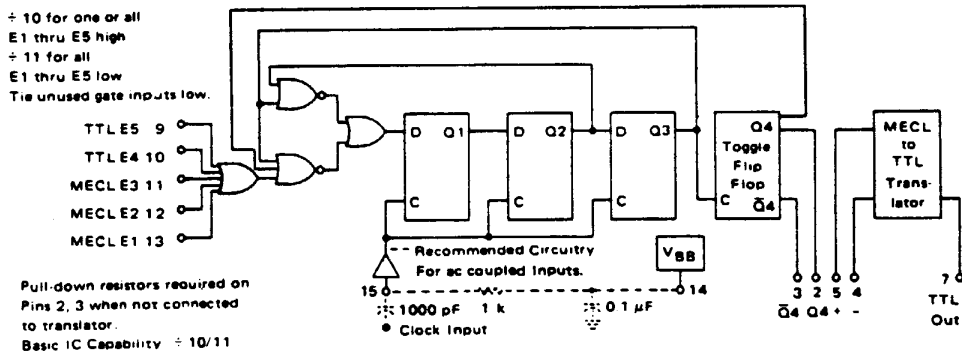
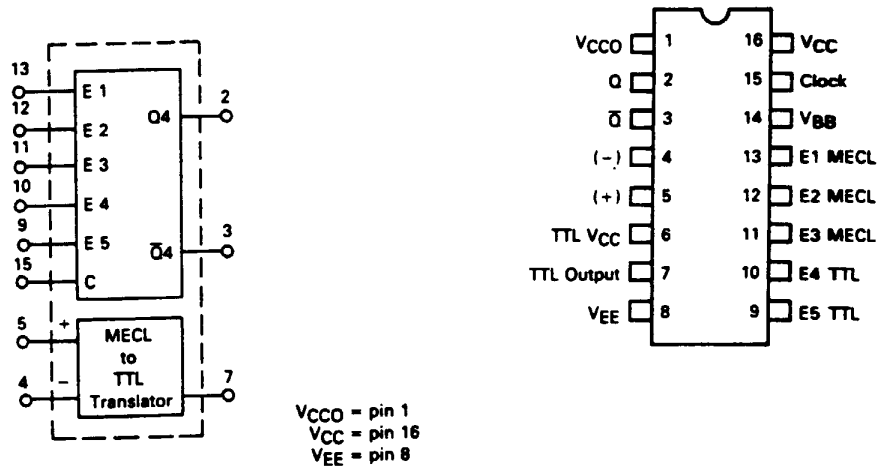


## MC12013

### TWO-MODULUS PRESCALER

These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-TTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

#### LOGIC DIAGRAM



## MC14094B

### 8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS

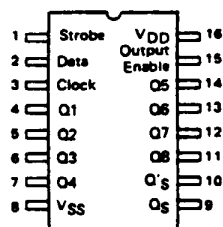
The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The  $Q_5$  output data is for use in high-speed cascaded systems. The  $Q'_5$  output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTTL Loads Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Three-State Bus Compatible
- Pin-for-Pin Compatible with CD4094B



Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q <sub>N</sub>	Q <sub>5</sub> <sup>*</sup>	Q' <sub>5</sub>
	0	X	X	3S	3S	Q7	No Chg.
	0	X	X	3S	3S	No Chg.	Q7
	1	0	X	No Chg.	No Chg.	Q7	No Chg.
	1	1	0	0	Q <sub>N</sub> -1	Q7	No Chg.
	1	1	1	1	Q <sub>N</sub> -1	Q7	No Chg.
	1	1	1	No Chg.	No Chg.	No Chg.	Q7

3S = Three-State  
X = Don't Care  
<sup>\*</sup>At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q<sub>5</sub>.



# MC145156

## SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

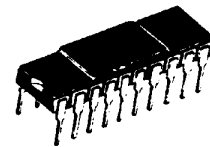
The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable +A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156.

- General Purpose Applications –
  - CATV                      TV Tuning
  - AM/FM Radios          Scanning Receivers
  - Two-Way Radios        Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values – 8, 64, 128, 256, 640, 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- +N Range = 3 to 1023
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options –
  - Single Ended (Three-State)
  - Double Ended

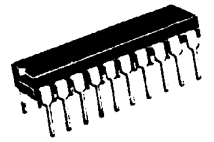
## CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

## SERIAL INPUT PLL FREQUENCY SYNTHESIZER

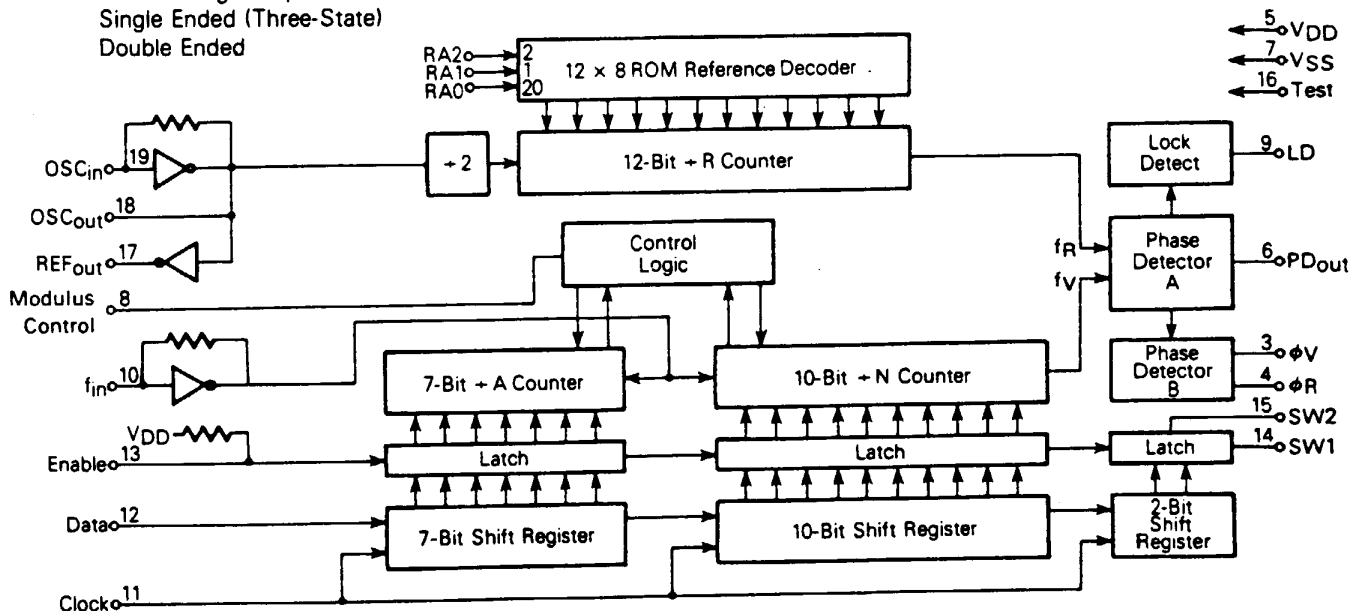
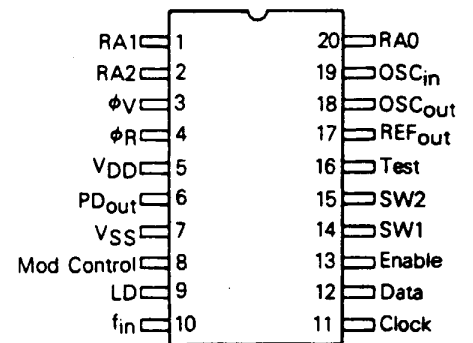


**L SUFFIX**  
CERAMIC PACKAGE  
CASE 729-01



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 738-02

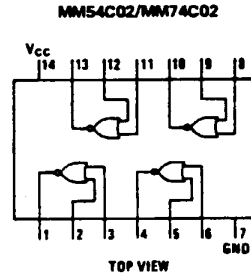
### PIN ASSIGNMENT



## MM74C02 Quad 2-Input NOR Gate

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems.

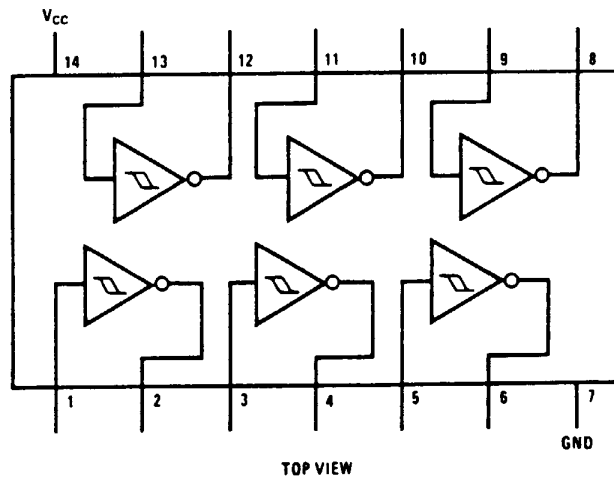
All inputs are protected from damage due to static discharge by diode clamps to  $V_{CC}$  and GND.



## MM74C14 Hex Schmitt Trigger

The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages,  $V_{T+}$  and  $V_{T-}$ , show low variation with respect to temperature (typ.  $0.0005 V/^{\circ}C$  at  $V_{CC} = 10V$ ), and hysteresis,  $V_{T+} - V_{T-} > 0.2V_{CC}$  is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to  $V_{CC}$  and GND.





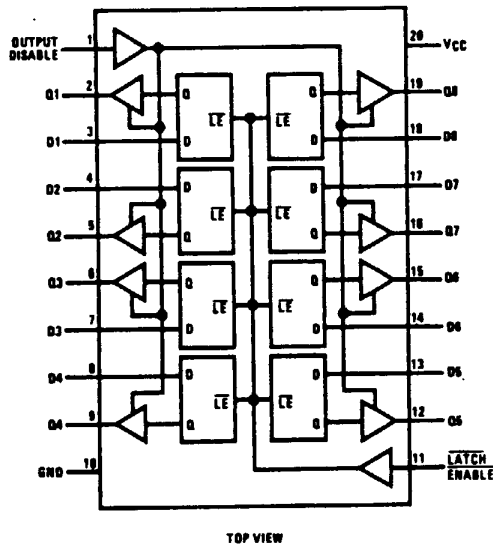
## MM74C373 Octal Latch

### General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When  $\overline{\text{LATCH ENABLE}}$  is high, the Q outputs will follow the D inputs. When  $\overline{\text{LATCH ENABLE}}$  goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until  $\overline{\text{LATCH ENABLE}}$  returns high again.

**Connection Diagram**





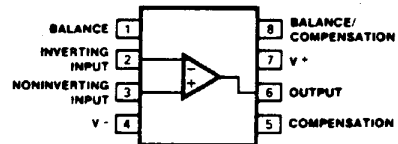
## NE-5534 SINGLE AND DUAL LOW NOISE OPERATIONAL AMPLIFIER

### DESCRIPTION

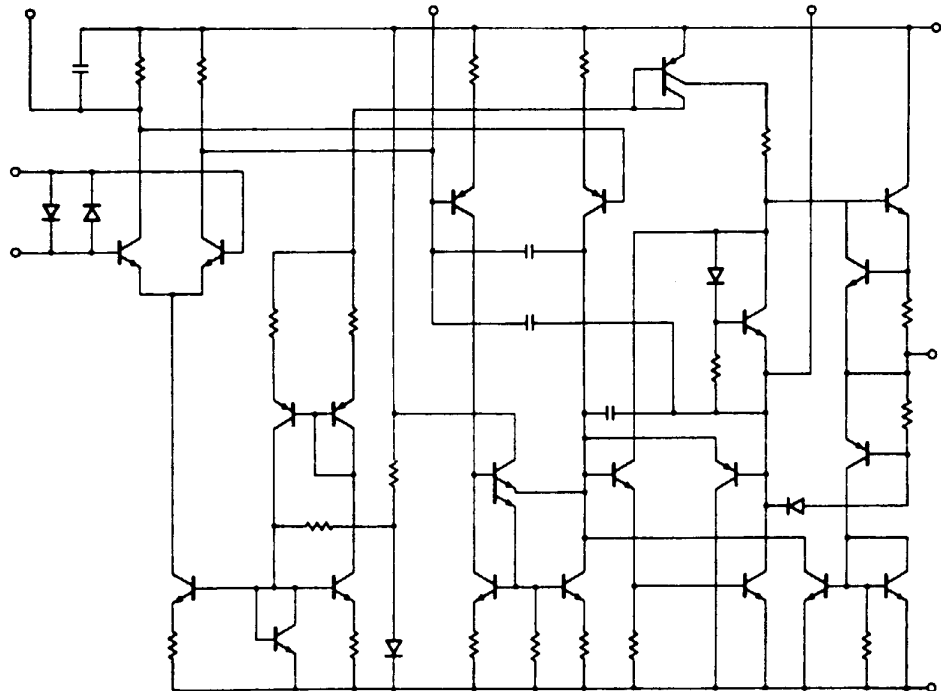
The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.)

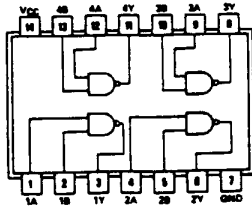
**D,N,FE PACKAGE**



### EQUIVALENT SCHEMATIC

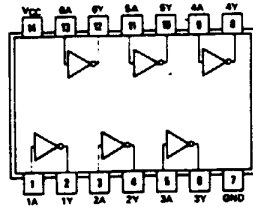


**SN74LS00**



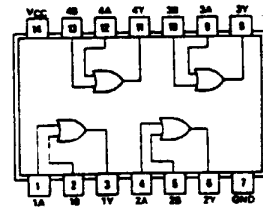
**QUADRUPLE 2-INPUT  
POSITIVE-NAND BUFFERS**  
 $Y = \overline{AB}$

**SN74LS04**



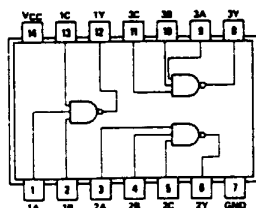
**HEX INVERTERS**  
 $Y = \overline{A}$

**SN74LS08**



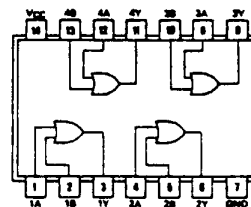
**QUADRUPLE 2-INPUT  
POSITIVE-AND GATES**  
 $Y = \overline{AB}$

**SN74LS27**



**TRIPLE 3-INPUT  
POSITIVE-NOR GATES**  
 $Y = \overline{A+B+C}$

**SN74LS32**



**QUADRUPLE 2-INPUT  
POSITIVE-OR GATES**  
 $Y = A+B$

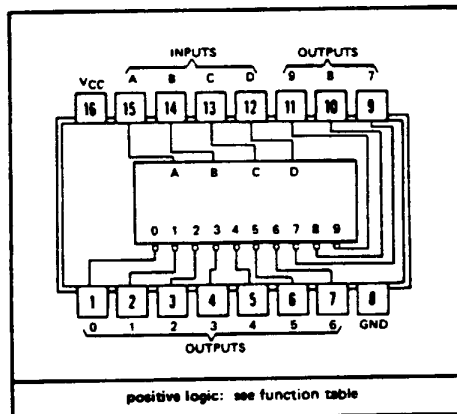
**SN74LS42**

**4-LINE-TO-10-LINE DECODERS (1-OF-10)**

**description**

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. D-c noise margins are typically one volt.

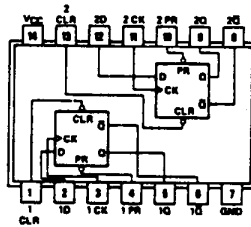


ALL TYPES DECIMAL OUTPUT									
0	1	2	3	4	5	6	7	8	9
L	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H
H	H	H	H	L	H	H	H	H	H
H	H	H	H	H	L	H	H	H	H
H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	L	H	H
H	H	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	L
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H

## SN74LS74N

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$



## SN74L90

### DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTER

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the  $Q_A$  output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the  $Q_D$  output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output  $Q_A$ .

'90A, 'L90, 'LS90  
BCD COUNT SEQUENCE  
(See Note A)

COUNT	OUTPUT			
	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

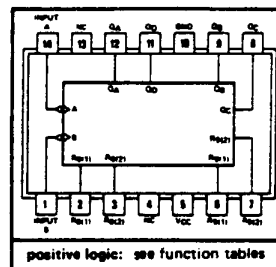
'90A, 'L90, 'LS90  
BI-QUINARY (5-2)  
(See Note B)

COUNT	OUTPUT			
	$Q_A$	$Q_D$	$Q_C$	$Q_B$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90, 'LS90  
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_0(1)$	$R_0(2)$	$R_9(1)$	$R_9(2)$	$Q_D$	$Q_C$	$Q_B$	$Q_A$
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

- NOTES: A. Output  $Q_A$  is connected to input B for BCD count.  
 B. Output  $Q_D$  is connected to input A for bi-quinary count.  
 C. Output  $Q_A$  is connected to input B.  
 D. H = high level, L = low level, X = irrelevant

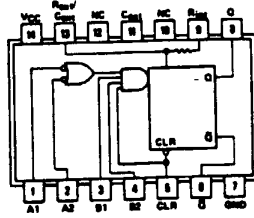


## SN74LS122

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

**FUNCTION TABLE**

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	↓	↑
H	L	X	H	↑	↓	↑
H	X	L	↑	H	↓	↑
H	X	L	H	↑	↓	↑
H	H	↓	H	H	↓	↑
H	H	↓	↓	H	↓	↑
H	↓	H	H	H	↓	↑
H	↓	↓	H	H	↓	↑
↑	L	X	H	H	↓	↑
↑	X	L	H	H	↓	↑



SN84122 (J, W) SN74122 (J, N)  
 SN84L122 (J, T) SN74L122 (J, N)  
 SN84LS122 (J, W) SN74LS122 (J, N)  
 \*122 ...  $R_{int} = 10 \text{ k}\Omega \text{ NOM}$   
 \*L122 ...  $R_{int} = 20 \text{ k}\Omega \text{ NOM}$   
 \*LS122 ...  $R_{int} = 10 \text{ k}\Omega \text{ NOM}$

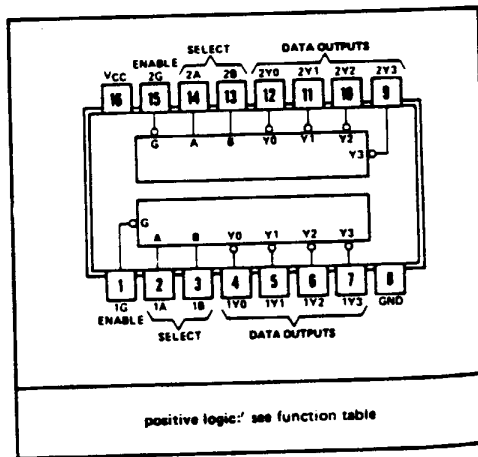
- NOTES: 1. An external timing capacitor may be connected between  $C_{ext}$  and  $R_{ext}/C_{ext}$  (positive).  
 2. For accurate repeatable pulse widths, connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.

## SN74LS138 DECODER/DEMULIPLEXER

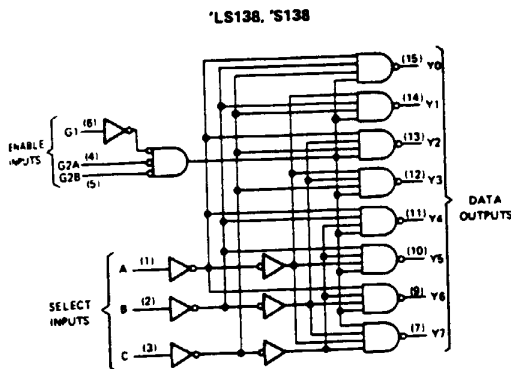
description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.



'LS138, 'S138  
FUNCTION TABLE



INPUTS		OUTPUTS										
ENABLE	SELECT											
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H
H	L	H	L	H	H	H	H	H	H	H	L	H
H	L	H	H	L	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	L

\*G2 = G2A + G2B  
 H = high level, L = low level, X = irrelevant

## SN74165 PARALLEL-LOAD 8-BIT SHIFT REGISTERS

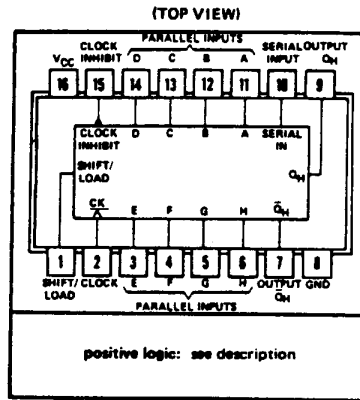
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165	35 MHz	105 mW

### description

The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of  $Q_A$  toward  $Q_H$  when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

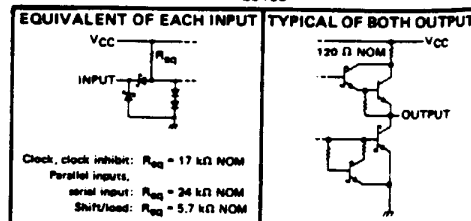
Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.



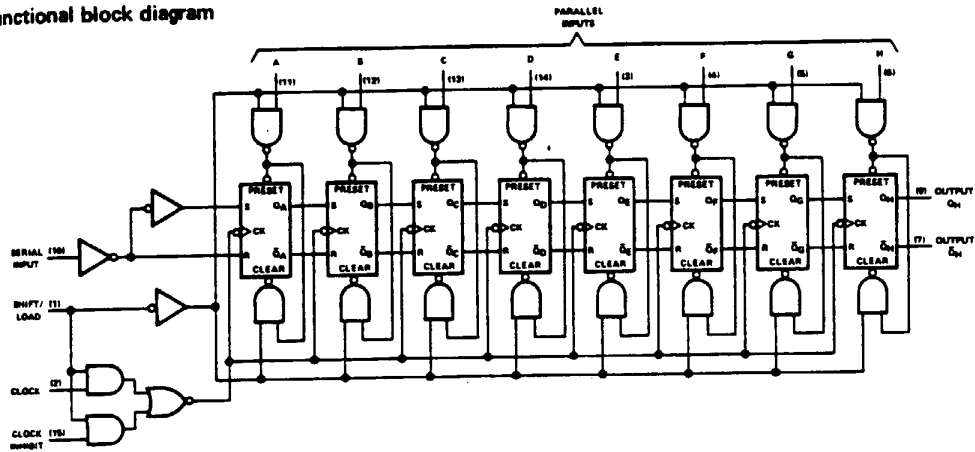
FUNCTION TABLE

INPUTS				INTERNAL PARALLEL A...H	INTERNAL OUTPUTS		OUTPUT QH
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL		QA	QB	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	QA0	QB0	QH0
H	L	↑	H	X	H	QAn	QGn
H	L	↑	L	X	L	QAn	QGn
H	H	X	X	X	QA0	QB0	QH0

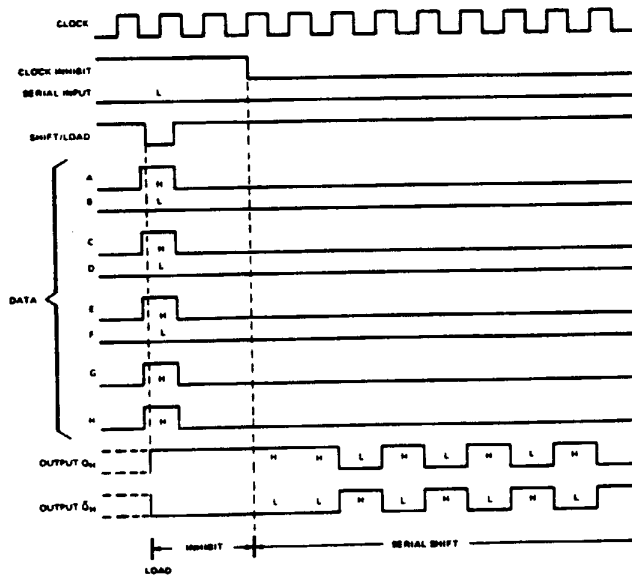
'LS165



functional block diagram



typical shift, load, and inhibit sequences



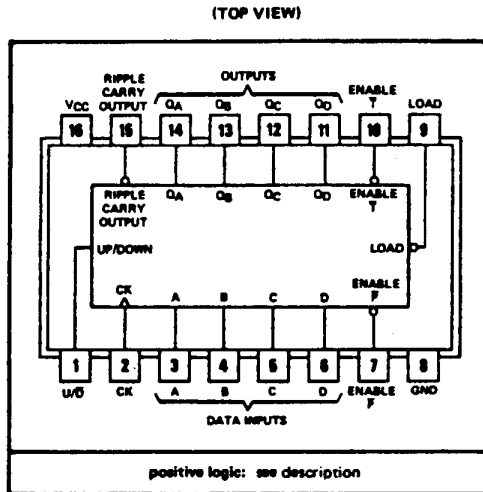


## SN74LS168A SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Programmable Look-Ahead Up/Down  
Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS168A, 'LS169A	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW



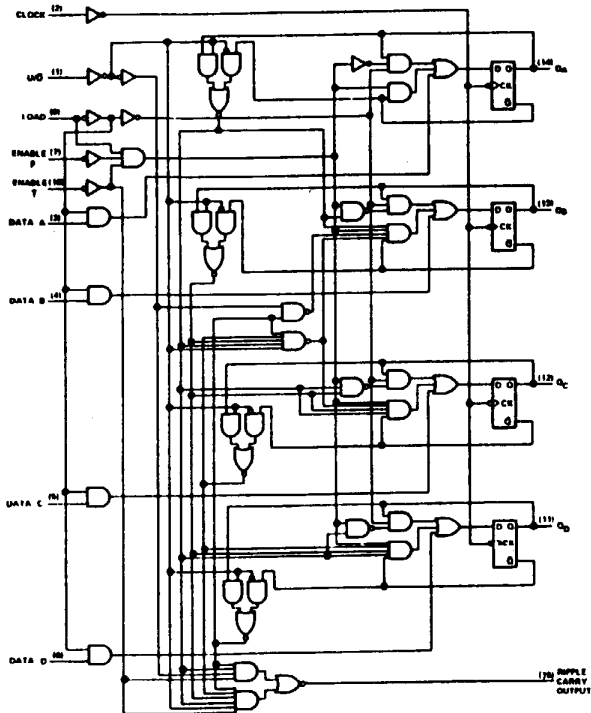
description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS168A and 'S168 are decade counters and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

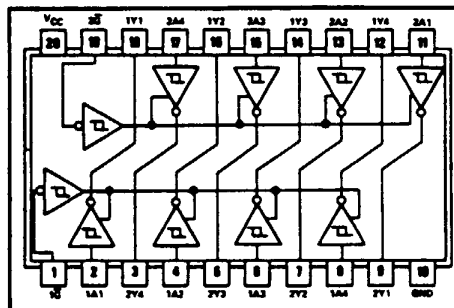
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ( $\bar{P}$  and  $\bar{T}$ ) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input  $\bar{T}$  is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the  $Q_A$  output when counting up and approximately equal to the low portion of the  $Q_A$  output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable  $\bar{P}$  or  $\bar{T}$  inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

These counters feature a fully independent clock circuit. Changes at control inputs (enable  $\bar{P}$ , enable  $\bar{T}$ , load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.



## SN74LS244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical  $\bar{G}$  (active-low output control) inputs, and complementary  $G$  and  $\bar{G}$  inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

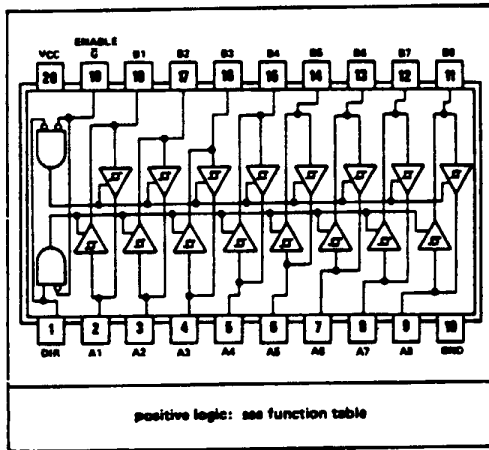


## SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

### description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ( $\bar{G}$ ) can be used to disable the device so that the buses are effectively isolated.

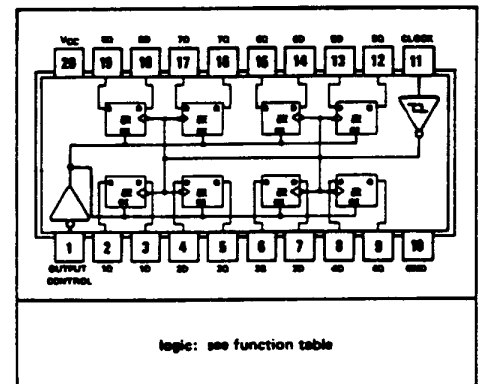
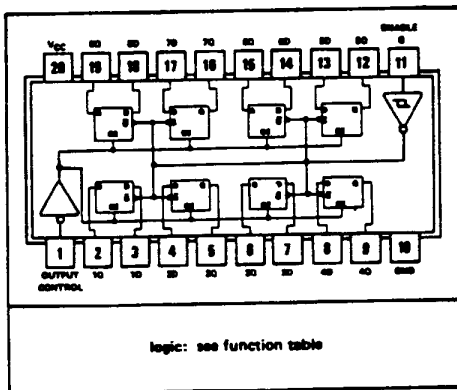


FUNCTION TABLE

ENABLE $\bar{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

## SN74LS373, SN74LS374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS



'LS373, 'S373  
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

'LS374, 'S374  
FUNCTION TABLE

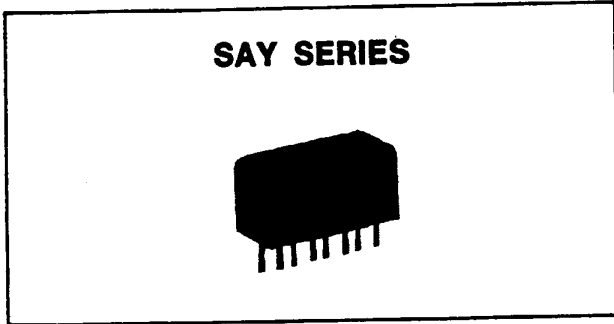
OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

**SAY-1**

**Super High Level (+23 dBm LO)  
DOUBLE-BALANCED MIXERS**



**DESCRIPTION** — High-level RF input capability coupled with ultra-low distortion, octaves of bandwidth, and reasonably good conversion loss make the SAY series obvious choices for applications in ECM receivers, spectrum analyzers, and field radios.

Housed in a miniature RFI shielded metal enclosure, these tiny units occupy a volume of only 0.128 cubic inches. The SAY series mixers are constructed to meet the requirements of MIL-M-28837/1A. Internally every unit is encapsulated with silicone rubber in order to withstand high shock, vibration, and acceleration environments.

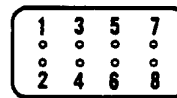
These mixers offer two-tone, third order intermodulation products that are typically 70 dB below the desired IF level (each tone is set at 0 dBm and the LO drive is at +23 dBm). The 1 dB conversion compression point occurs at an RF level of +20 dBm.

**CONNECTIONS**

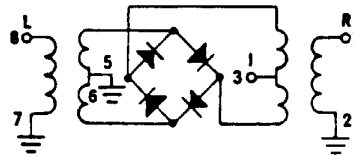
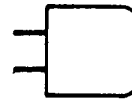
TOP VIEW



Letter M over pin 2  
Blue bead pin 1



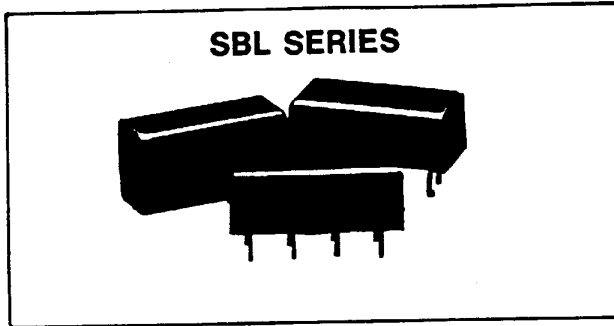
BOTTOM VIEW



Model No.	-1 -2 -11
LO	8
RF	1
IF	3
Ground	2,5,6,7
Case Ground	2,5,6,7

**SBL-1**

# Standard Level (+7 dBm LO) DOUBLE-BALANCED MIXERS

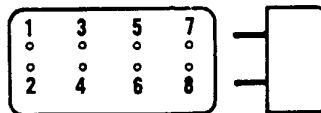


### CONNECTIONS

LETTER M OVER PIN 2  
(BLUE BEAD PIN 1 SBL-1X ONLY)

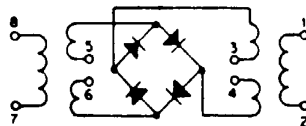


TOP VIEW



BOTTOM VIEW

### PIN LAYOUT

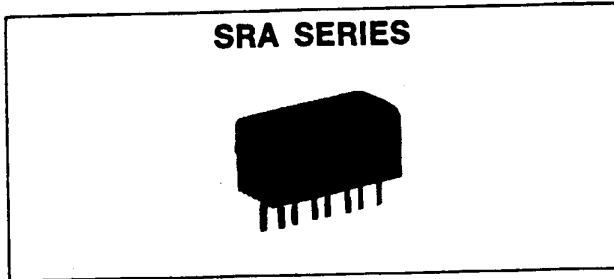


Model No.	Fig. 1	Fig. 2
	-1'	-1X
LO	8	8
RF	1	3,4
IF	3,4	1
Ground	2,5,6,7	2,5,6,7
Case Ground	—	2,5,6,7

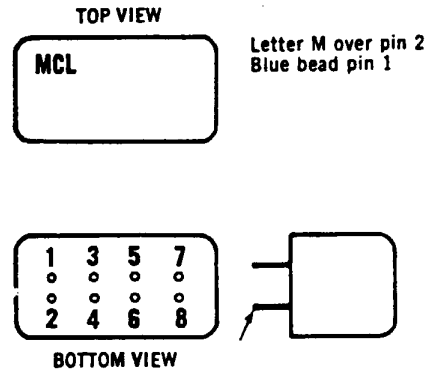
NOTE: PINS 3 AND 4 MUST BE CONNECTED TOGETHER

**SRA-1**

# Standard Level (+7 dBm LO) DOUBLE-BALANCED MIXERS



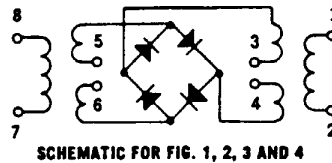
**CONNECTIONS**



**DESCRIPTION** — Having a volume of only .128 cu. inches, the SRA series covers a very broad frequency range from 500 Hz to 2000 MHz. These rugged units provide low conversion loss, 6 dB, high isolation, 40 dB, and exceptional unit to unit matched performance.

Packaged within an RFI shielded metal enclosure and hermetically sealed header, these high performance units have their pins oriented on a 0.2 inch grid.

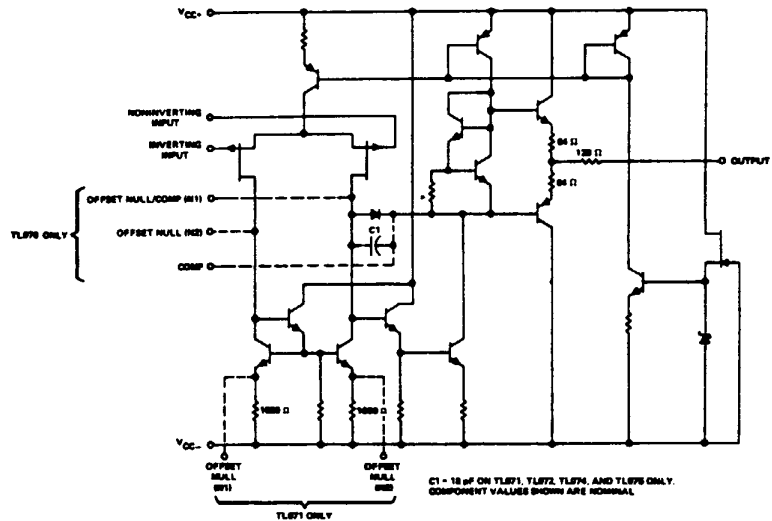
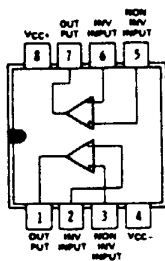
Only well matched hot-carrier diodes and ruggedly constructed transmission line transformers are used. Internally, every component is bonded to the header and case with silicone rubber to provide super reliable protection against shock, vibration and acceleration.



**PIN LAYOUT**

Fig. 1	
Model No.	-1 -1-1 -3 -1TX
LC	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

## TL072 LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS



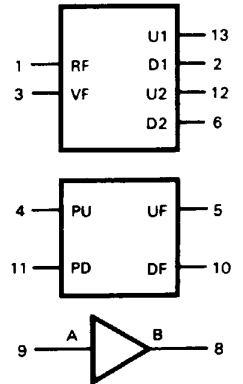
**description**

The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

**11C44**  
**Phase/Frequency Detector**

**GENERAL DESCRIPTION** — The 11C44 contains a Phase/Frequency Detector, a Phase Detector, a Charge Pump, and an Amplifier. The Phase/Frequency Detector accepts TTL signals representing a Reference Frequency (RF) and a Variable Frequency (VF), compares the relative timing of their negative going transitions, and generates either an UP (U1) or a DOWN (D1) signal whose duration is equal to the RF-VF timing difference. When the RF and VF signals have the same frequency, the Phase Detector outputs U2 and D2 provide binary signals whose duty cycles are proportional to the phase angle between RF and VF. The Charge Pump can be driven from U1 and D1 or U2 and D2, and has three possible output states representing CHARGE, DISCHARGE, and HOLD instructions when applied to an integrator. The Amplifier is a Darlington transistor with grounded emitter and uncommitted collector and base. The 11C44 thus contains several of the functional elements used in phase-locked loop applications.

**LOGIC SYMBOL**



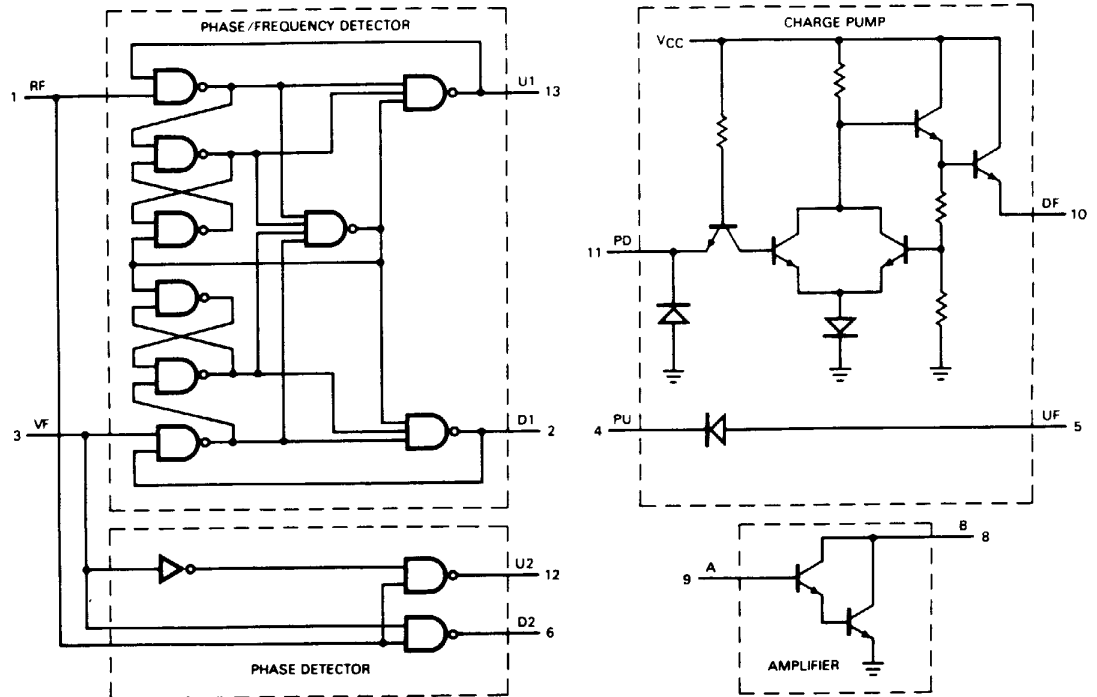
**FUNCTIONS**

RF — Reference Frequency Input  
VF — Variable Frequency Input  
U1, D1 — Phase/Frequency Detector Outputs  
U2, D2 — Phase Detector Outputs

PU, PD — Charge Pump Inputs  
UF, DF — Charge Pump Outputs  
A — Amplifier Input  
B — Amplifier Output

V<sub>CC</sub> = Pin 14  
GND = Pin 7

**LOGIC DIAGRAM AND SCHEMATIC**



## ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE (EPCI)

2661

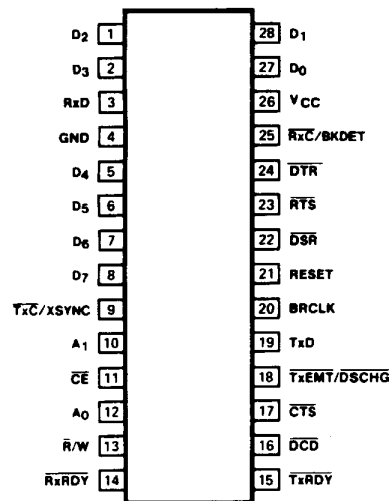
### DESCRIPTION

The Signetics 2661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced pin compatible version of the 2651. It interfaces directly to most 8-bit microprocessors and may be used in a polled or interrupt driven system environment. The 2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines—synchronous and asynchronous—in the full or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

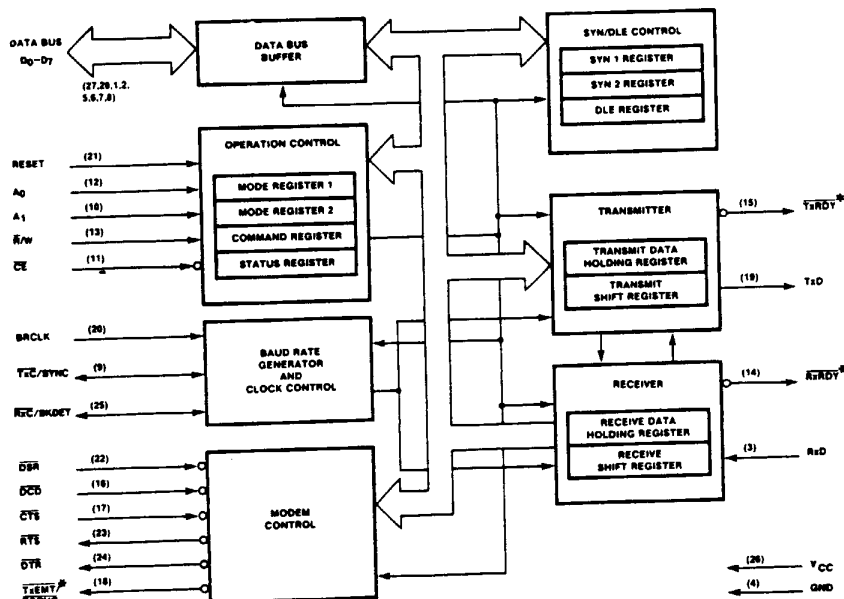
The 2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (-1, -2, -3) has a different set of baud rates.

The EPCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.



### PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27,28,1, 2,5-8	D <sub>0</sub> -D <sub>7</sub>	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A <sub>0</sub> -A <sub>1</sub>	Internal register select lines	I
13	R/W	Read or write command	I
11	CE	Chip enable input	I
22	DSR	Data set ready	I
24	DTR	Data terminal ready	O
23	RTS	Request to send	O
17	CTS	Clear to send	I
16	DCD	Data carrier detected	I
18	TxEMT/DSCHG	Transmitter empty or data set change	O
9	TxC/XSYNC	Transmitter clock/external SYNC	I/O
25	RxC/BKDET	Receiver clock/break detect	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	TxRDY	Transmitter ready	O
14	RxDY	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	VCC	+5V supply	I
4	GND	Ground	I





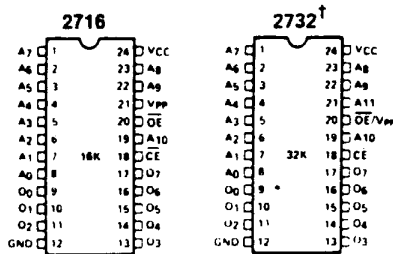
## 2716 16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - 350 ns Max. 2716-1
  - 390 ns Max. 2716-2
  - 450 ns Max. 2716
  - 650 ns Max. 2716-6
- **Pin Compatible to Intel® 2732 EPROM**
- **Simple Programming Requirements**
  - Single Location Programming
  - Programs with One 50 ms Pulse
- **Single +5V Power Supply**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Low Power Dissipation**
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

### PIN CONFIGURATION



† Refer to 2732 data sheet for specifications

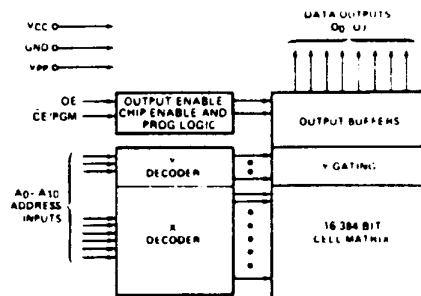
### PIN NAMES

A <sub>0</sub> - A <sub>10</sub>	ADDRESSES
CE/PGM	CHIP ENABLE/PROGRAM
OE	OUTPUT ENABLE
O <sub>0</sub> - O <sub>7</sub>	OUTPUTS

### MODE SELECTION

MODE \ PINS	CE/PGM (18)	OE (20)	V <sub>pp</sub> (21)	V <sub>CC</sub> (24)	OUTPUTS (9-11, 13-17)
Read	V <sub>IL</sub>	V <sub>IL</sub>	+5	+5	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	Don't Care	+5	+5	High Z
Program	Pulsed V <sub>IL</sub> to V <sub>IH</sub>	V <sub>IH</sub>	+25	+5	D <sub>IN</sub>
Program Verify	V <sub>IL</sub>	V <sub>IL</sub>	+25	+5	D <sub>OUT</sub>
Program Inhibit	V <sub>IL</sub>	V <sub>IH</sub>	+25	+5	High Z

### BLOCK DIAGRAM



## 2732 32K (4K x 8) UV ERASABLE PROM

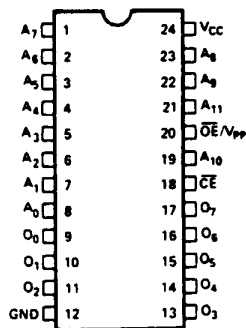
- **Fast Access Time:**
  - 450 ns Max. 2732
  - 550 ns Max. 2732-6
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  - 150mA Max. Active Current
  - 30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - Single Location Programming
  - Programs with One 50ms Pulse
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory EPROM. The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control.

An important 2732 feature is the separate output control, Output Enable  $\overline{OE}$ , from the Chip Enable control  $\overline{CE}$ . The  $\overline{OE}$  control eliminates bus contention in multiple bus microprocessor systems.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the  $\overline{CE}$  input.

### PIN CONFIGURATION



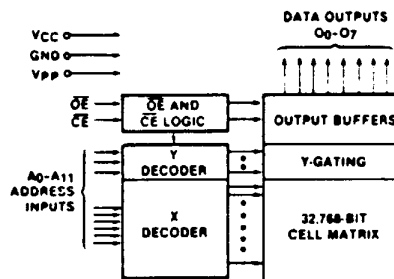
### PIN NAMES

A <sub>0</sub> -A <sub>11</sub>	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O <sub>0</sub> -O <sub>7</sub>	OUTPUTS

### MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{pp}$ (20)	V <sub>CC</sub> (24)	OUTPUTS (9-11,13-17)
Read	V <sub>IL</sub>	V <sub>IL</sub>	+5	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	Don't Care	+5	High Z
Program	V <sub>IL</sub>	V <sub>pp</sub>	+5	D <sub>IN</sub>
Program Verify	V <sub>IL</sub>	V <sub>IL</sub>	+5	D <sub>OUT</sub>
Program Inhibit	V <sub>IH</sub>	V <sub>pp</sub>	+5	High Z

### BLOCK DIAGRAM



## 8035

# SINGLE COMPONENT 8-BIT MICROCOMPUTER

- \*8048 Mask Programmable ROM
- \*8748 User Programmable/Erasable EPROM
- \*8035 External ROM or EPROM

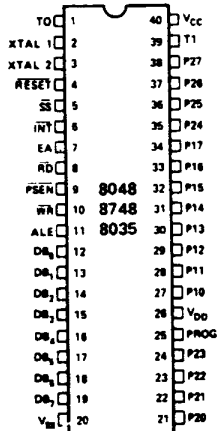
- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5  $\mu$ sec and 5.0  $\mu$ sec Cycle Versions  
All Instructions 1 or 2 Cycles.
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM
- 64 x 8 RAM
- 27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

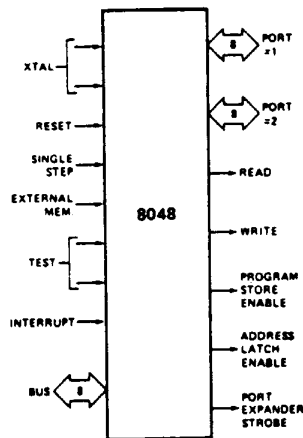
The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and 8000 series peripherals. The 8035 is the equivalent of an 8048 without program memory.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

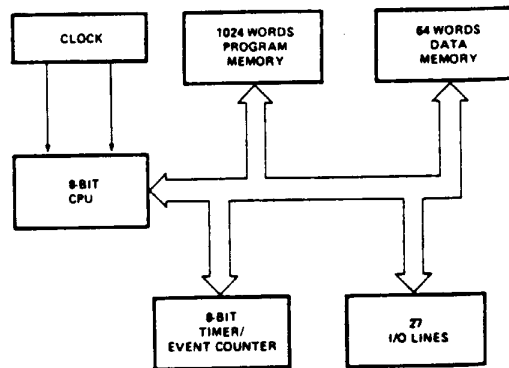
### PIN CONFIGURATION



### LOGIC SYMBOL



### BLOCK DIAGRAM



 **HARRIS**  
**RF COMMUNICATIONS**

**PIN DESCRIPTION**

Designation	Pin #	Function	Designation	Pin #	Function
V <sub>SS</sub>	20	Circuit GND potential	$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.  Used as a Read Strobe to External Data Memory. (Active low)
V <sub>DD</sub>	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.	$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
V <sub>CC</sub>	40	Main power supply; +5V during operation and programming.	$\overline{WR}$	10	Output strobe during a BUS write. (Active low) (Non TTL V <sub>IH</sub> )  Used as write strobe to External Data Memory.
PROG	25	Program pulse (+25V) input pin during 8748 programming.  Output strobe for 8243 I/O expander.	ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.  The negative edge of ALE strobes address into external data and program memory.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.	$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243	$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
DB <sub>0</sub> -DB <sub>7</sub> BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$ , $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$ . Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ , and $\overline{WR}$ .	EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.	XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.	XTAL2	3	Other side of crystal input.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)			

## 8085A/8085A-2 SINGLE CHIP 8-BIT N-CANNEL MICROPROCESSORS

- Single +5V Power Supply
- 100% Software Compatible with 8080A
- 1.3  $\mu$ s Instruction Cycle (8085A);  
0.8  $\mu$ s (8085A-2)
- On-Chip Clock Generator (with External  
Crystal, LC or RC Network)
- On-Chip System Controller; Advanced  
Cycle Status Information Available for  
Large System Control
- Four Vectored Interrupt Inputs (One is  
non-Maskable) Plus an 8080A-  
compatible interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision  
Arithmetic
- Direct Addressing Capability to 64k  
Bytes of Memory

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's (8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)) while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

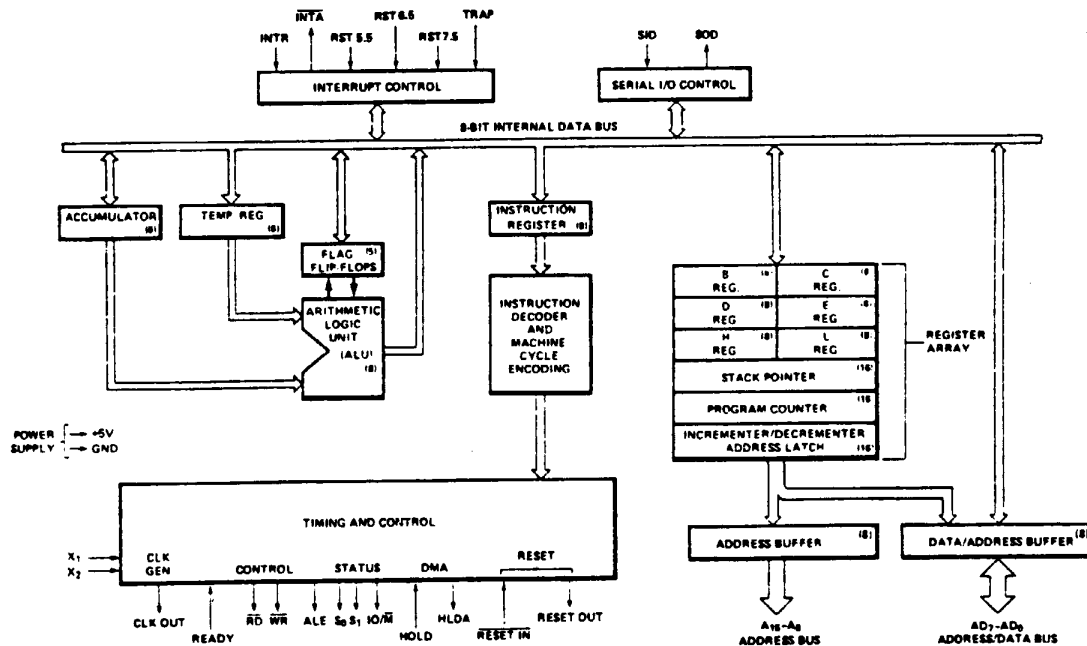


Figure 1. 8085A CPU Functional Block Diagram

## 8155/8156/8155-2/8156-2 2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

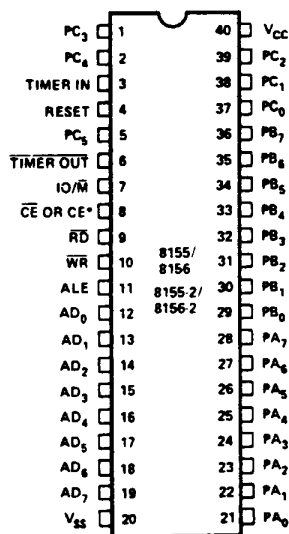
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 89156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

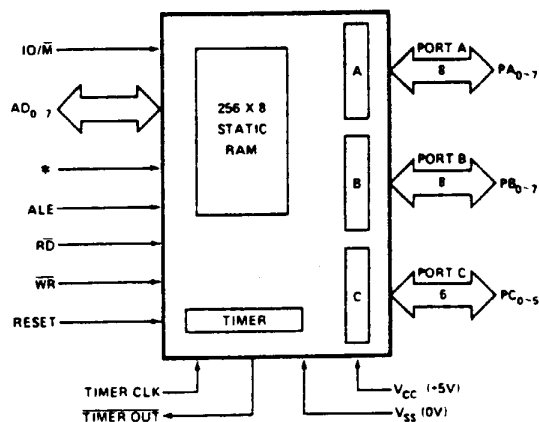
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

### PIN CONFIGURATION



### BLOCK DIAGRAM



8155/8155-2 =  $\overline{CE}$ , 8156/8156-2 = CE

**8155/8156 PIN FUNCTIONS**

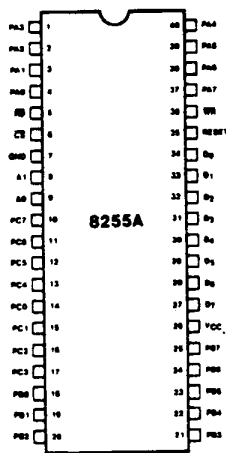
<u>Symbol</u>	<u>Function</u>	<u>Symbol</u>	<u>Function</u>
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.	ALE input	Address Latch Enable: This control signal latches both the address on the AD <sub>0-7</sub> lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
AD <sub>0-7</sub> (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/56 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/M input. The 8-bit data is either written into the chip or read from the chip, depending on the WR or RD input signal.	IO/M (input)	Selects memory if low and I/O and command/status registers if high.
CE or $\overline{CE}$ (input)	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.	PA <sub>0-7</sub> (8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD <sub>0-7</sub> buffers. If IO/M pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.	PB <sub>0-7</sub> (8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/M.	PC <sub>0-5</sub> (6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC <sub>0-5</sub> are used as control signals, they will provide the following: PC <sub>0</sub> — A INTR (Port A Interrupt) PC <sub>1</sub> — ABF (Port A Buffer Full) PC <sub>2</sub> — A STB (Port A Strobe) PC <sub>3</sub> — B INTR (Port B Interrupt) PC <sub>4</sub> — B BF (Port B Buffer Full) PC <sub>5</sub> — B STB (Port B Strobe)
		TIMER IN (input)	Input to the counter-timer.
		$\overline{TIMER OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
		V <sub>cc</sub>	+5 volt supply.
		V <sub>ss</sub>	Ground Reference.

## 8255A/8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Micro-processor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

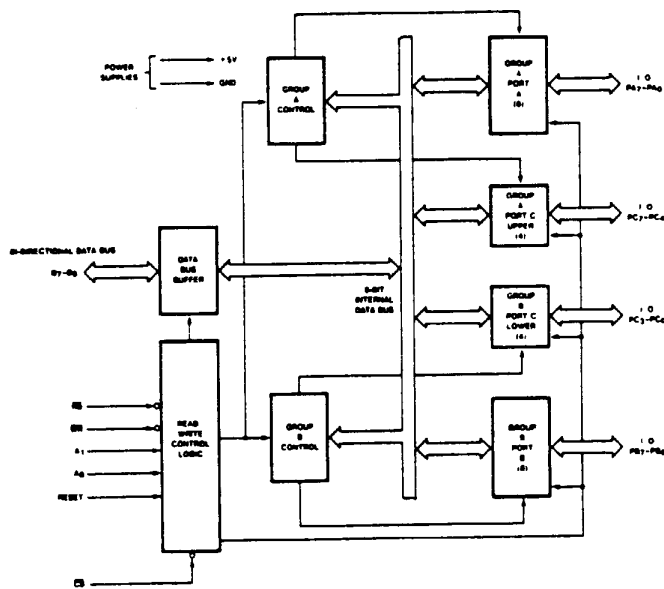
**PIN CONFIGURATION**



**PIN NAMES**

D <sub>7</sub> -D <sub>0</sub>	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A <sub>8</sub> , A <sub>1</sub>	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V <sub>CC</sub>	+5 VOLTS
GND	0 VOLTS

**8255A BLOCK DIAGRAM**





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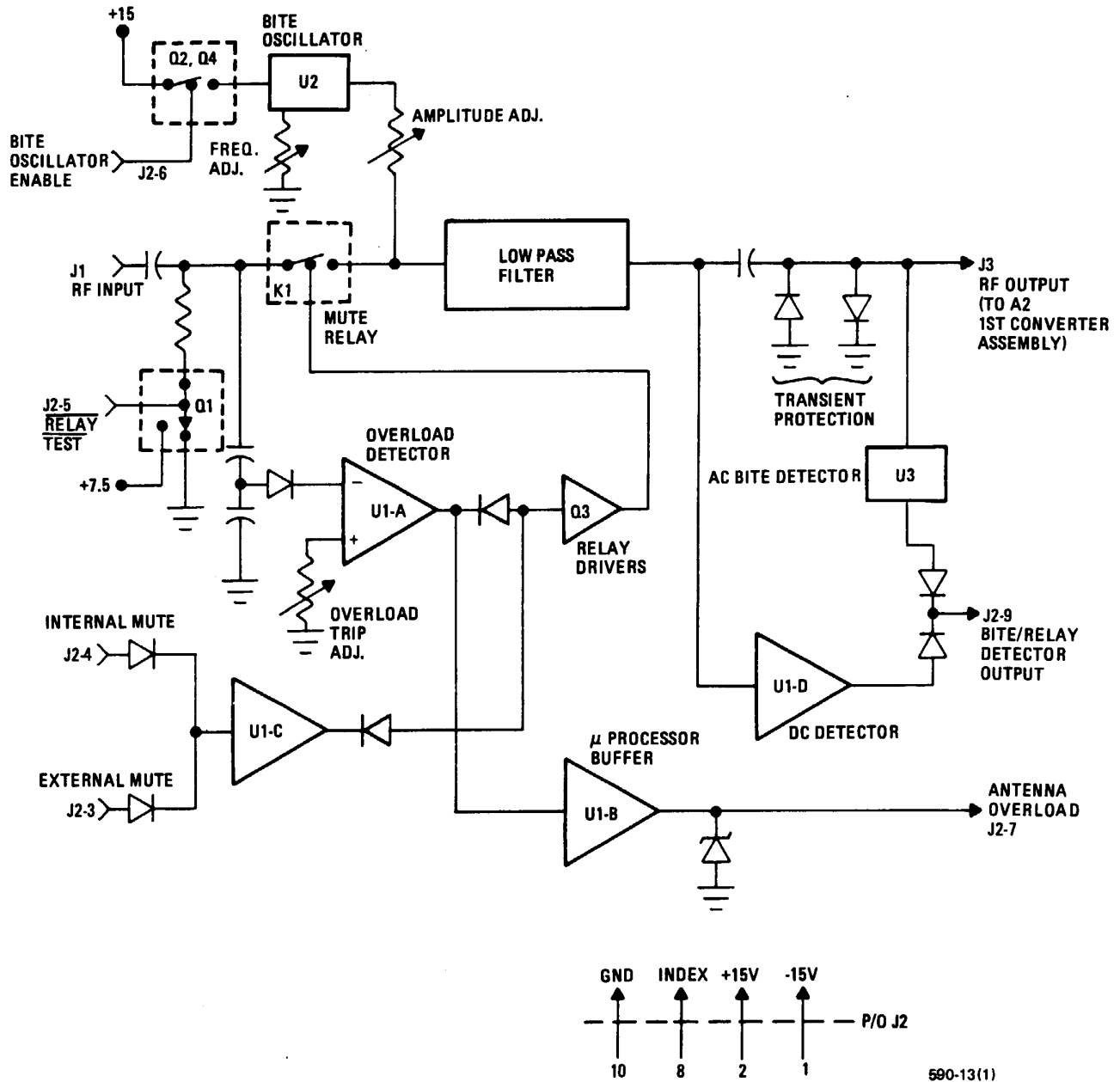
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**HARRIS**  
RF COMMUNICATIONS



Input Filter Assembly A1 Functional Block Diagram

## 1. GENERAL DESCRIPTION

Input Filter Assembly A1 performs two primary functions:

- a. RF signal filtering above the desired receiver input range of 10 kHz to 30 MHz. Specifically, the first IF signal at 40.455 MHz, and the image band at 80.920 to 110.910 MHz.
- b. Protection from high level input signals (1.5 to 70 Vrms) which could damage receiver front end circuits.

Additionally, BITE signal generation, A1 BITE detection, and receiver muting also occur on the A1 Assembly.

RF input signals arrive at J1 from rear panel connector J1, Antenna Input. RF output signals feed from J3 to First Converter Assembly A2. Total module gain from input to output is nominally 0 dB.

## 2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and any relevant data.

**Table 1. A1 Input Filter Assembly Interface Connections**

Connector	Function	Characteristics
J1	RF INPUT	10 kHz - 30 MHz, $Z_o = 50$ ohms
J2-1	Power	-15 Vdc at 20 mA
J2-2	Power	+15 Vdc at 200 mA
J2-3	External Mute	Same as Internal Mute
J2-4	Internal Mute	+5 Vdc = relay contacts open, 0 Vdc = relay contacts closed
J2-5	Relay Test	Relay Test Line, 0 Vdc = +7.5 Vdc applied to K1 contacts +5 Vdc = 0 Vdc applied to K1 contacts
J2-6	Bite Oscillator Enable	Bite Oscillator Enable Line, +5 Vdc = oscillator on 0 Vdc = oscillator off
J2-7	Antenna Overload Output	3.5 Vdc output for 1.5 - 70 Vrms input
J2-8	Index	
J2-9	BITE Detector Output	BITE signal test: 2.5 Vdc nominally for ac or dc BITE tests
J2-10	GND	
J3	RF Output	10 kHz - 30 MHz, $Z_o = 50$ ohms

### 3. CIRCUIT DESCRIPTION

#### 3.1 Low Pass Filter (LPF) Circuit

The LPF was designed for a passband of 10 kHz to 30 MHz, a total insertion loss of less than 1/2 dB (nominally), and an SWR of 1.1:1.

The LPF image rejection desired of > 100 dB is required since the RF-590 image band of 80.920 MHz to 110.910 MHz encompasses U.S. TV channels 5, 6, and the FM band. To accomplish this, a ninth order Elliptic function filter is cascaded with a fifth order Chebishev function filter. The first null of the Elliptic filter was chosen at the first IF (40.455 MHz), and the Chebishev filter is used to flatten out the stop band characteristics of the Elliptic filter. See figure 1 for a typical A1 LPF characteristic. The -3 dB cutoff frequency is approximately 31.5 MHz.

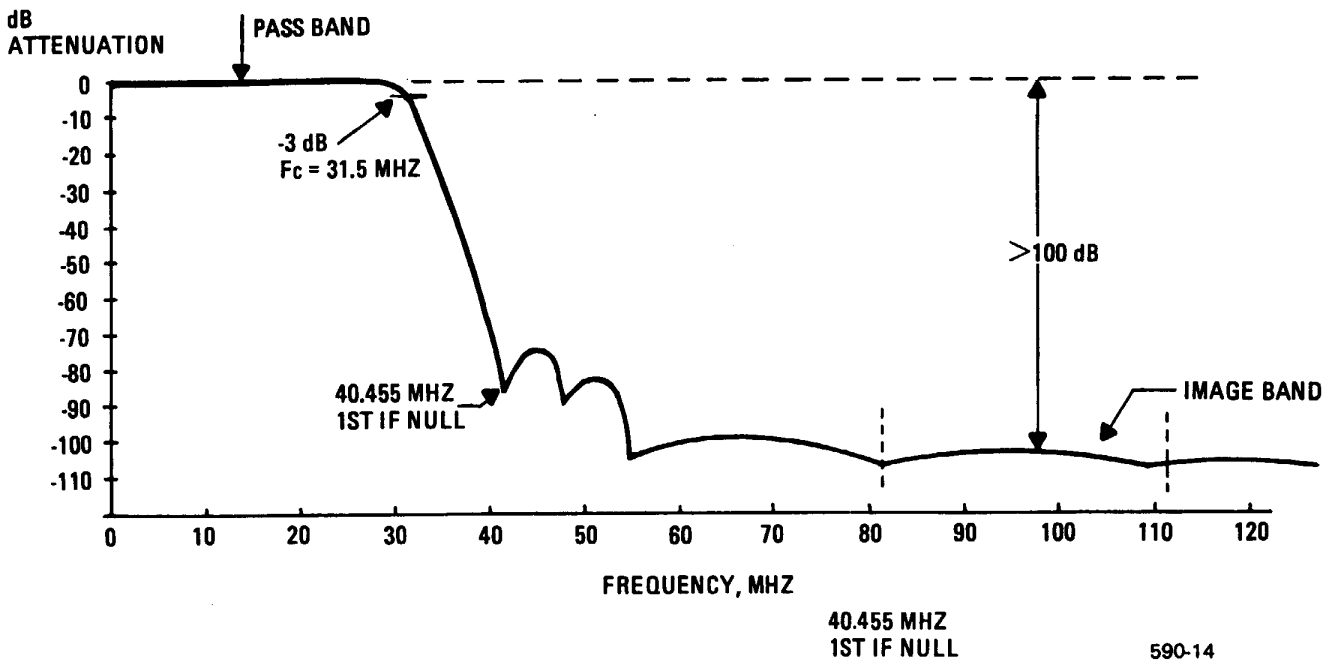


Figure 1. Typical A1 LPF Characteristic

#### 3.2 Protection Circuits

Two protection circuits are employed on the A1 assembly and respond to the two possible types of overload conditions: transient and steady state.

##### 3.2.1 Transient Protection

Upon initial application of an overload condition, a transient signal may pass through the LPF before relay K1 can deenergize. This transient is clamped at a maximum level of 8 Vpp by CR1-CR4 and CR24-CR27 before leaving the assembly. This allows temporary protection until the relay control circuits can activate

in the presence of a steady state signal. Also, certain types of overloads are basically transient in nature, and it may not be desirable to disturb the signal path by deenergizing K1.

### 3.2.2 Steady State Protection

Under no RF input conditions at J1, CR5-CR8, R40, and CR9-CR12, R5 bias U1A (-) input to nominally 0 Vdc. This value is less than the positive potential set by R7, Overload Adjust, at U1A (+), so U1A output at pin 8 will be high (+15 Vdc). Consequently, CR14 is reverse biased, and R10 supplies base current to Q3, turning Q3 and relay K1 on.

When an RF signal is received at J1, a portion is tapped off by voltage divider network C3-C9 and detected by the diode string CR5-CR12. This raises the potential at U1A (-). When this level exceeds the trip point set by R7 (corresponding to approximately 1.5 Vrms ac at J1), U1A output swings low (-15 Vdc) and forward biases CR14. This removes base drive to Q3. Q3 turns off and the relay deenergizes, breaking the RF signal path into the receiver. Hysteresis around U1A holds the relay deenergized until the RF input drops at least 10 dB.

Under overload conditions, the low output at U1A causes U1B output to swing high (+15 Vdc). This forward biases CR29. Voltage divider/clamp network R18, R21, R37, and CR22 provide a TTL logic high signal ( $\approx 4$  Vdc) to detection circuitry on Control Board A14. This in turn causes the RF-590 front panel display to read out the message ANTENNA OVERLOAD. This disables all front panel controls until the overload condition is removed, at which time the overload message is removed and normal operation is resumed.

### 3.3 Mute Circuitry

Two receiver mute inputs are provided on the A1 board; Internal Mute and External Mute. Both cause RF signal path muting when a high TTL level ( $\approx 5$  Vdc) signal is present at their inputs. This causes U1C output to swing low (-15 Vdc), which forward biases CR20 and removes base drive to Q3. Q3 turns off, deenergizing K1 and disrupting the RF signal path into the receiver. This +5 Vdc is generated on the control board (A14) whenever the external Mute line on J7-7 (rear panel) is grounded.

Internal Muting occurs as part of the receiver BITE routine. External Muting is accessed via the rear panel terminal strip TB1, pin 16, and/or connector J7, pin 7. External Muting is an option to be exercised by the operator, depending upon system requirements.

### 3.4 BITE Circuitry

Bite test signal generation occurs on the A1 assembly. This test signal is adjusted to -20 dBm, 100 kHz at J3. It is fed through the A1 assembly and on to assemblies A2-A5 for testing purposes. Various amplitude sample and detection circuits throughout the signal path monitor critical signal stages to check for proper operation. BITE testing is completely under software control and is initiated by pressing the RF-590 front panel TEST switch (see the Maintenance section of this manual).

### 3.4.1 BITE Signal Generation

The BITE test signal is generated by 100 kHz oscillator U2 and its associated components. U2 output is applied to the LPF side of relay K1 only when K1 is deenergized via software control. This prevents U2 output signals from reaching the antenna. The 100 kHz injection at U2, pin 3, is a 15 Vpp square wave. The BITE test signal is set while monitoring J3. R25 sets the operating frequency to 100 kHz and R28 sets the output amplitude to -18 dBm.

Oscillator U2 is enabled by Q2 and Q4, which in turn are controlled via system software. A +5 Vdc level at J2-6 enables U2.

### 3.4.2 BITE Detection

Two BITE tests are enacted on the A1 assembly.

- K1 relay check
- A1 signal path level check

Both tests are under BITE software control and commence upon initiating RF-590 front panel TEST control. The tests are done sequentially, and the resulting output signal at J2-9 is ultimately applied to Control Board Assembly A14. An error code will be displayed on the RF-590 front panel display if either test fails.

#### 3.4.2.1 Relay K1 Test Circuits

During normal operating conditions, K1 will be energized, Internal Mute line will be low, and Relay Test line will be high (consequently, holding Q1 on, and applying 0 Vdc to TP1 and relay K1). When the BITE routine begins, Relay Test goes low, turning off Q1 and applying  $\approx 7.5$  Vdc to TP1 and the relay contacts. This signal is passed through the relay and the low pass filter (LPF), and is detected by Dc BITE Detector U1D. U1D output, which had previously been low (-15 Vdc) will now swing high (+15 Vdc) and forward bias CR21. This provides a nominal 2.5 Vdc level at J2, pin 9, BITE/Relay Out. This signal is fed to an A/D converter on the A14 Control Board, which then feeds other A14 circuits that determine if this signal has sufficient amplitude to ensure that no dc losses are present in relay K1 or the LPF.

Next, Internal Mute goes high, which turns Q3 and K1 off. Since the 7.5 Vdc signal at TP1 can no longer pass through the relay, U1D output will swing low and present  $\approx 0$  Vdc at BITE/Relay Out. Control Board A14 circuitry will interpret this as an indication that the relay did deenergize, and will proceed to the next test, A1 Signal Path.

#### 3.4.2.2 A1 Signal Path Test Circuits

Upon successful completion of relay K1 testing, the A1 signal path is checked using a 100 kHz test signal generated by BITE Oscillator U2. The oscillator is enabled when the BITE Oscillator Enable line is pulled high (under software control) turning on Q4 and Q2. This applies +15 Vdc to oscillator U2. U2 output is

applied to the input of the LPF (relay K1 is deenergized during this test) and is detected by Ac BITE Detector U3. If no faults occur in the signal path, U3 will produce a nominal output voltage of 2.5 Vdc at J2, pin 9, BITE/RELAY OUT. This is sampled by the A/D Converter on Control Board A14, and if the level is sufficient (indicating no ac losses on the A1 assembly), BITE testing would continue throughout the RF chain of the receiver. (Note that it is this same 100 kHz signal which is used to test circuits on the A2-A5 assemblies.)

#### 4. MAINTENANCE

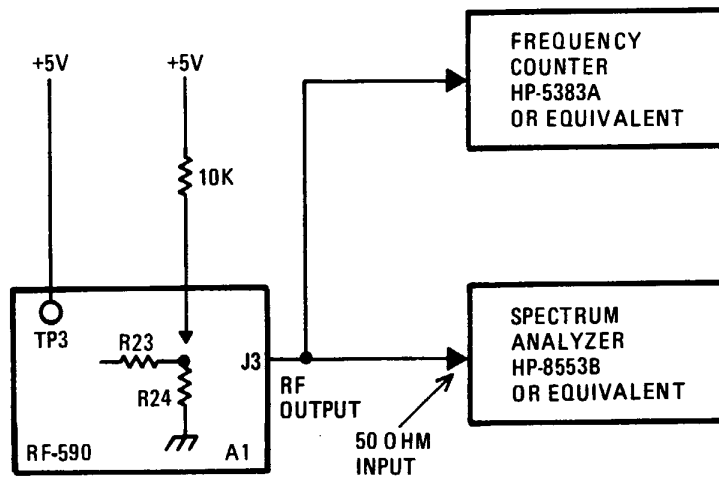
The following adjustments should not be performed as routine maintenance procedures, but should be used only when a failure indicates a definite requirement. All tests should be performed with all assembly connections in normal contact, unless otherwise specified.

#### NOTE

J3 plugs directly into the A2 assembly through the chassis.  
Therefore it will be necessary to remove the A1 assembly  
from the chassis to gain access to J3.

#### 4.1 BITE Oscillator Adjustments/Test

- a. Connect equipment as shown in figure 2.



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**Figure 2. A1 BITE Oscillator Test Setup**

- b. Adjust R25 for 100.0 kHz and R28 for -18 dBm at J3 RF output.
- c. Disconnect all equipment and fully reconnect the A1 module to RF-590. Initiate RF-590 BITE Test. The receiver must pass O1 testing.

## 4.2 Overload Adjustments/Test

- a. Connect equipment as shown in figure 3.



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**Figure 3. A1 Overload Adjustment Test Setup**

- b. Set RF-590 controls as follows:

Frequency: 10.000000 MHz  
Mode: USB  
AGC: Medium  
RF Gain: Fully clockwise (cw)

- c. Set signal generator to 10.000 MHz, 1.5 Vrms.  
d. Adjust R7 until J2-7 Antenna Overload switches to approximately 5 Vdc.  
e. Disconnect all equipment.

## 5. PARTS LIST

Table 2 is a comprehensive parts list of all replaceable components in Input Filter Assembly A1. When ordering parts from the factory, include a full description of the part. Use figure 4, the Input Filter Assembly A1 Component location diagram to identify parts.

## 6. SCHEMATIC DIAGRAM

Figure 5 is the Input Filter Assembly A1 schematic diagram.



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Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100)

Ref. Desig.	Part Number	Description
	10073-5100	PWB, INPUT FILTER
C1	M39014/02-1320	CAP .47UF 10% 50V CER-R
C2	M39014/02-1320	CAP .47UF 10% 50V CER-R
C3	CM04ED300J03	CAP 30PF 5% 500V MICA
C4	CM04ED300J03	CAP 30PF 5% 500V MICA
C5	CM04ED300J03	CAP 30PF 5% 500V MICA
C6	CM04ED300J03	CAP 30PF 5% 500V MICA
C7	CM04ED750J03	CAP 75PF 5% 500V MICA
C8	CM04ED750J03	CAP 75PF 5% 500V MICA
C9	CM04ED750J03	CAP 75PF 5% 500V MICA
C10	CM04CD120J03	CAP 12PF 5% 500V MICA
C11	CM04CD050D03	CAP 5PF + -.5PF 500V MICA
C12	CM04FD151J03	CAP 150PF 5% 500V MICA
C13	CM04ED430J03	CAP 43PF 5% 500V MICA
C14	CM04ED510J03	CAP 51PF 5% 500V MICA
C15	CM04ED750J03	CAP 75PF 5% 500V MICA
C16	CM04ED470J03	CAP 47PF 5% 500V MICA
C17	CM04FD131J03	CAP 130PF 5% 500V MICA
C18	CM04ED300J03	CAP 30PF 5% 500V MICA
C19	CM04ED620J03	CAP 62PF 5% 500V MICA
C20	CM04ED680J03	CAP 68PF 5% 500V MICA
C21	CM04FD151J03	CAP 150PF 5% 500V MICA
C22	CM04ED680J03	CAP 68PF 5% 500V MICA
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1320	CAP .47UF 10% 50V CER-R
C26	M39014/02-1320	CAP .47UF 10% 50V CER-R
C27	CK05BX472M	CAP 4700PF 20% 100V CER
C28	CM04FD151J03	CAP 150PF 5% 500V MICA
C29	M39014/02-1320	CAP .47UF 10% 50V CER-R
C30	M39014/02-1320	CAP .47UF 10% 50V CER-R
C31	M39014/02-1320	CAP .47UF 10% 50V CER-R
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	CM06FD122J03	CAP 1200PF 5% 500V MICA
C35	M39014/02-1320	CAP .47UF 10% 50V CER-R
C36	M39014/01-1535	CAP .01UF 20% 100V CER
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	C26-0025-339	CAP 3.3UF 20% 25V TANT
C45	C26-0025-339	CAP 3.3UF 20% 25V TANT
C46	M39014/01-1535	CAP .01UF 20% 100V CER
C47	M39014/01-1535	CAP .01UF 20% 100V CER

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Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100) (Cont.)

Ref. Desig.	Part Number	Description
C48	M39014/02-1310	CAP .1UF 10% 100V CER-R
C50	CM04FD151J03	CAP 150PF 5% 500V MICA
CR1	D02-0003-001	DIODE 2.5A 50V RECT FR
CR2	D02-0003-001	DIODE 2.5A 50V RECT FR
CR3	D02-0003-001	DIODE 2.5A 50V RECT FR
CR4	D02-0003-001	DIODE 2.5A 50V RECT FR
CR5	1N4454	DIODE 200mA 75V SW
CR6	1N4454	DIODE 200mA 75V SW
CR7	1N4454	DIODE 200mA 75V SW
CR8	1N4454	DIODE 200mA 75V SW
CR9	1N4454	DIODE 200mA 75V SW
CR10	1N4454	DIODE 200mA 75V SW
CR11	1N4454	DIODE 200mA 75V SW
CR12	1N4454	DIODE 200mA 75V SW
CR13	1N5245B	DIODE 15V 5% .5W ZENER
CR14	1N4454	DIODE 200mA 75V SW
CR15	1N4007	DIODE 1A 1000V RECT GP
CR16	1N4454	DIODE 200mA 75V SW
CR17	1N4454	DIODE 200mA 75V SW
CR18	1N4454	DIODE 200mA 75V SW
CR19	1N4454	DIODE 200mA 75V SW
CR20	1N4454	DIODE 200mA 75V SW
CR21	1N4454	DIODE 200mA 75V SW
CR22	1N5230A	DIODE 4.7V 10% .5W ZENER
CR23	1N5230A	DIODE 4.7V 10% .5W ZENER
CR24	D02-0003-001	DIODE 2.5A 50V RECT FR
CR25	D02-0003-001	DIODE 2.5A 50V RECT FR
CR26	D02-0003-001	DIODE 2.5A 50V RECT FR
CR27	D02-0003-001	DIODE 2.5A 50V RECT FR
CR28	1N4454	DIODE 200mA 75V SW
CR29	1N4454	DIODE 200mA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J46-0032-010	HDR 10 PIN 0.100" SR
J3	J90-0014-001	CONN SMB VERT PCB MT M
K1	K-0118	RLY,12VDC,DPDT,ENC,PC MNT
L1	10073-5111	INDUCTOR
L2	10073-5112	INDUCTOR
L3	10073-5113	INDUCTOR
L4	10073-5114	INDUCTOR
L5	10073-5114	INDUCTOR
L6	10073-5114	INDUCTOR
L7	10073-7029	INDUCTOR, FILTER CHOKE
L9	MS75085-13	COIL 330UH 10% FXD RF
L10	MS75085-13	COIL 330UH 10% FXD RF
L11	MS75085-13	COIL 330UH 10% FXD RF

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Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100) (Cont.)

Ref. Desig.	Part Number	Description
L12	MS75085-13	COIL 330UH 10% FXD RF
L13	MS75085-13	COIL 330UH 10% FXD RF
L14	MS75085-13	COIL 330UH 10% FXD RF
Q1	2N2222	XSTR SS/GP NPN TO-18
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	2N2222	XSTR SS/GP NPN TO-18
Q4	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R2	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R3	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R4	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R5	RN55D1053F	RES,105K 1% 1/8W MET FLM
R6	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R7	R30-0008-501	RES,VAR,PCB 500 20%
R8	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R9	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R10	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R11	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R12	R65-0003-330	RES 33 5% 1/4W CAR FILM
R13	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R14	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R15	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R16	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R17	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R19	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R20	R65-0003-122	RES 1.2K 5% 1/4W CAR FILM
R21	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R22	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R23	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R24	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R25	R-2228	RES,VAR,PCB 10K .5 20%
R26	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R27	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R28	R-2229	RES,VAR,PCB 20K .5 20%
R29	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R30	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R31	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R32	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R33	RN55D1740F	RES,174.0 1% 1/8W MET FLM
R34	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R35	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R36	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R37	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R38	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

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Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100) (Cont.)

Ref. Desig.	Part Number	Description
R39	R65-0003-394	RES 390K 5% 1/4W CAR FILM
R40	RN55D8062F	RES,80.6K 1% 1/8W MET FLM
R41	R65-0004-472	RES 4.7K 5% 1/2W CAR FILM
R42	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R43	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R44	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R45	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R46	RN55D1003F	RES,100K 1% 1/8W MET FLM
R47	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R50	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R51	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R52	R65-0003-124	RES 120K 5% 1/4W CAR FILM
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	130-0003-000	IC 324 OP AMP PLASTIC
U2	120-0005-000	IC LM111H COMPARATOR
U3	120-0005-000	IC LM111H COMPARATOR

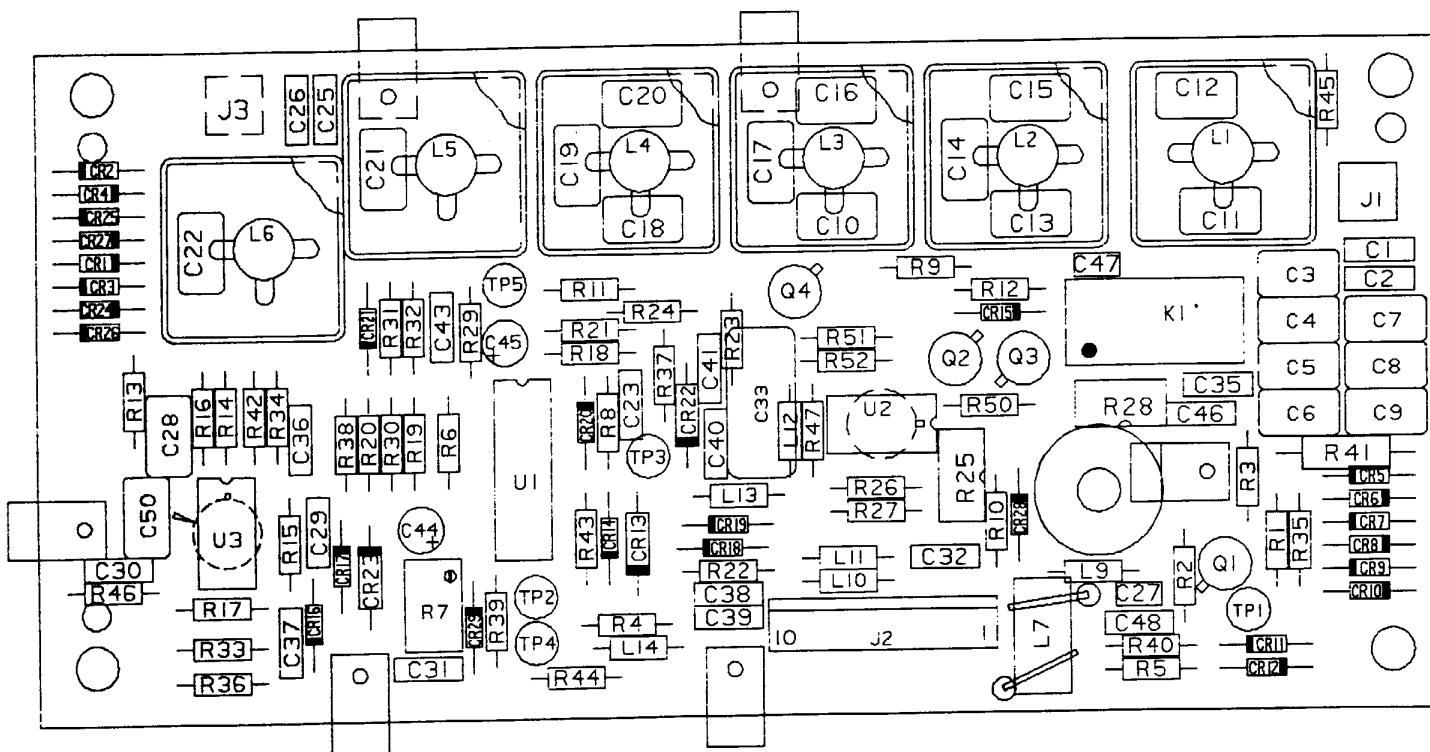


Figure 4. Input Filter Assembly A1 Component Location Diagram (10073-5100, Rev. J)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
2. COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO., DESIGNATION.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%;
4. ALL CAPACITOR VALUES ARE IN MICROFARADS.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
6. VENDOR PART NO. CALCULATIONS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
7. RELAY K1 IS SHOWN ENERGIZED.
8. VOLTAGE LEVEL SPECIFIED FOR NO RF INPUT.
9. VOLTAGE LEVEL SPECIFIED DURING A1 BITE TEST.

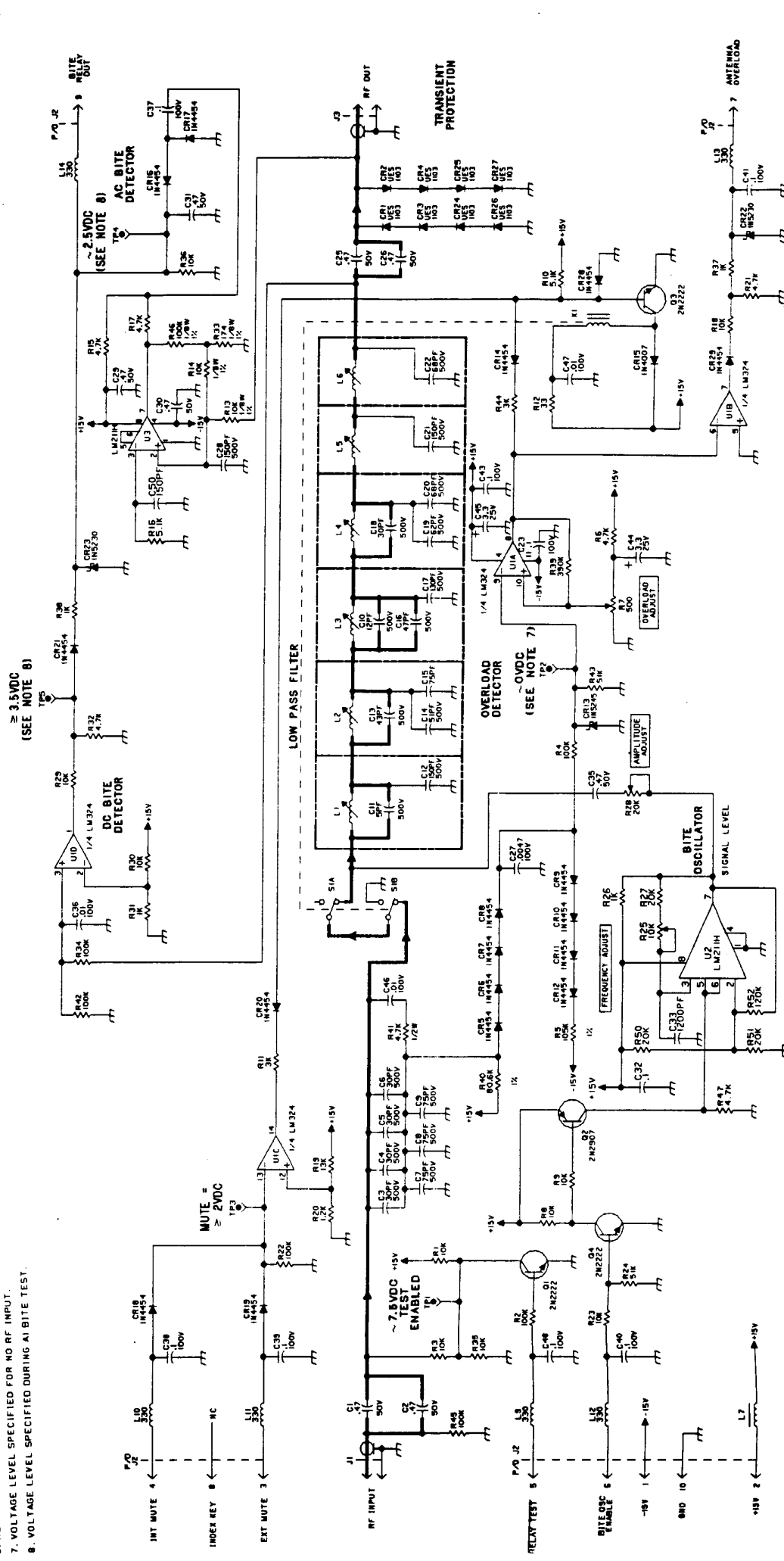


Figure 5. Input Filter Assembly A1 Schematic Diagram (10073-5101, Rev. F)

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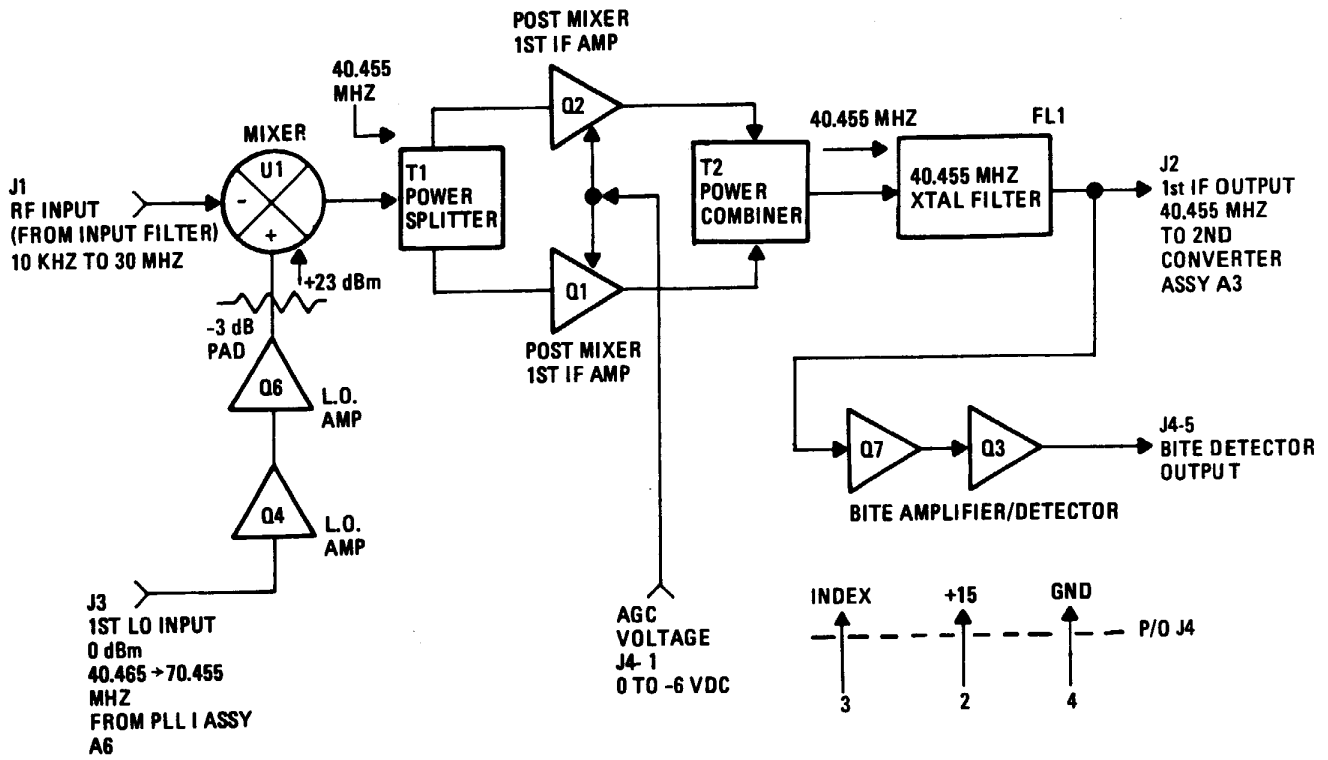
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**First Converter Assembly A2 Functional Block Diagram**

## 1. GENERAL DESCRIPTION

First Converter Assembly A2 converts the Input Radio Frequency (RF) range of 10 kHz to 30 MHz to an Intermediate Frequency (IF) of 40.455 MHz at mixer U1. (Sideband inversion occurs during the mixing process.) This IF signal is then split in power and fed to two identical automatic gain controlled (AGC) First IF Amplifier (postmixer) stages. After the amplified signals are recombined, they are filtered through a 16 kHz wide, 40.455 MHz crystal filter and directed to Second Converter Assembly A3. Typical RF input to IF output gain is 0 dB. The IF signal is also monitored by the Built In Test Equipment (BITE) detection circuit which monitors the operation of the First Converter Assembly.

## 2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

**Table 1. First Converter A2 Interface Connections**

Connector	Function	Characteristics
J1	RF INPUT	10 kHz - 30 MHz, -120/+10 dBm Zo = 50 ohms
J2	IF Output	40.455 MHz $\pm$ 8 kHz, -120/9 dBm (under AGC control), Zo = 50 ohms
J3	LO No. 1 Injection	40.465 - 70.455 MHz, 0 dBm
J4-1	AGC Input	0 Vdc $\rightarrow$ -6 Vdc produces 0 $\rightarrow$ -20 dB gain reduction
J4-2	Power	+15 Vdc at 400 mA
J4-3	Index Pin	
J4-4	Ground	
J4-5	Bite Output	Approximately .75 Vdc for -20 dBm J1 input at 100 kHz

## 3. CIRCUIT DESCRIPTION

### 3.1 Mixer/Postmixer IF Amplifiers

RF input signals from 10 kHz to 30 MHz are applied to doubly balanced, diode - ring type mixer U2 at pin 1, through a 2 dB pad. U1 is a very high level mixer requiring +23 dBm at its LO port, pin 8, from the LO No. 1 Amplifier (paragraph 3.3). Conversion loss is typically 6 dB.

IF output from U1 (pins 3, 4) is applied to a broadband 50 ohm power splitter comprised of T1, C1, C2, C45, and R4.



Q1 and Q2 are identically grounded gate FET amplifier stages, so only one stage (Q1) shall be discussed. Q1 is biased by R5 to typically 1-2 volts at its source. The drain load impedance is set at 1400 ohms by C46, C16, and L6 (L6 is adjusted for resonance at 40.455 MHz). Nominal stage power gain is +12 dB.

CR1 provides gain reduction by reducing the drain load on Q1 upon application of a negative AGC voltage at R7. Typically, -20 dB of gain reduction is possible.

Q1 and Q2 outputs are recombined in a broadband 50 ohm combiner consisting of T2, C19, C20, and R9. The 40.455 MHz IF output is then filtered in crystal filter FL-1, whose -3 dB bandwidth is  $\pm 8$  kHz and whose loss is approximately -5 dB.

The filtered IF output is directed to Second Converter Assembly A3 via J2, and to the BITE detection circuit (paragraph 3.2).

### 3.2 BITE Detection Circuit

The 40.455 MHz IF output is applied to buffer stage Q7, a source follower. Q7 output feeds tuned amplifier Q3, which amplifies the signal to the required detection level. This signal is then rectified and filtered by CR3, CR4, and C25. CR6 limits the detection voltage to approximately 5 Vdc to protect the following A/D converter inputs. An RF input level of -20 dBm at J1 results in approximately .5 Vdc at BITE Output, J4, pin 5.

### 3.3 LO No. 1 Amplifier

LO No. 1 injection of 0 dBm (nominally) is supplied by PLL1 Assembly A6 to LO No. 1 input, J3, and then to common base amplifier driver Q4. The LO frequency range is 40.465 - 70.455 MHz. Q4 is biased to approximately 50 mA of emitter current via R14 - R16, and provides approximately 10 dB of voltage gain from TP3 to TP4.

T3 and T4 provide an impedance stepdown to the base of power amplifier Q6. R29 - C40 - R26 stabilize Q6 and provide a flat output ( $\pm 1$  dB) from Q6 over the LO frequency range. T5 supplies nominally +26 dBm and impedance matching to a 50 ohm, -3 dB pad consisting of R1, R2, and R3. This pad then supplies a solid 50 ohm termination and +23 dBm level to the LO port of mixer U1.

Q5 and associated circuitry provides base current to Q6, resulting in a Q6 collector current of approximately 300 mA. Diode CR5 provides thermal stabilization to Q5 base current. Resistor pair R23 and R24 form a sense circuit for Q6 collector current. As Q6 collector current increases, the voltage at the emitter of Q5 decreases, thereby reducing the base-emitter voltage of Q5. This in turn reduces Q5 base and emitter current, and also Q6 base and collector current.

## 4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests are performed with all assembly connections in normal contact except those specified.

**NOTE**

J1 plugs directly into the A1 assembly through the chassis.  
Therefore it will be necessary to remove the A1 assembly  
from the chassis to gain access to J1. Leave all other  
connections to A2 connected unless otherwise specified.

**4.1 LO No. 1 Amplifier Test**

- a. Set RF-590 controls as follows:

Frequency: 10.000000 MHz  
Mode: USB  
AGC: OFF  
RF Gain: Fully clockwise (cw)

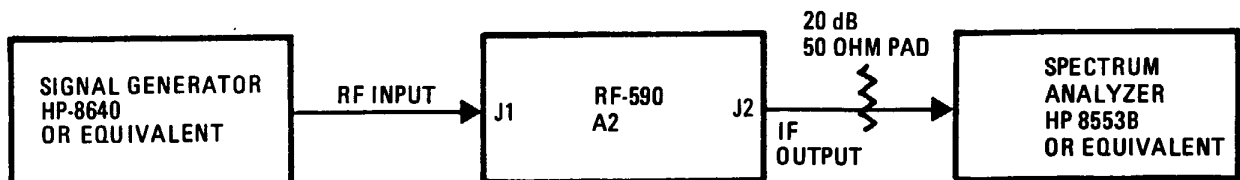
- b. Monitor A2 TP1 with an oscilloscope and frequency counter (each capable of measuring signals to 100 MHz). Signal at TP1 should be approximately 7.5 Vpp at 50.455000 MHz.

**4.2 Postmixer IF Amplifier Adjustments/Test**

- a. Set RF-590 controls as follows:

Frequency: 10.000000 MHz  
Mode: USB  
AGC: OFF  
RF Gain: Fully clockwise (cw)

- b. Connect equipment as shown in figure 1.



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**Figure 1. A2 Postmixer IF Amplifier Test Setup**

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- c. Apply a 0 dBm, 10.000000 MHz test signal to RF input J1. Monitoring IF output J2 with a spectrum analyzer at 40.455 MHz, adjust L6 and L7 for maximum output. Output must be 0 dBm  $\pm$  2 dB, indicating an overall module gain of 0 dB.

**4.3 AGC Test**

- a. Set RF-590 controls as follows:

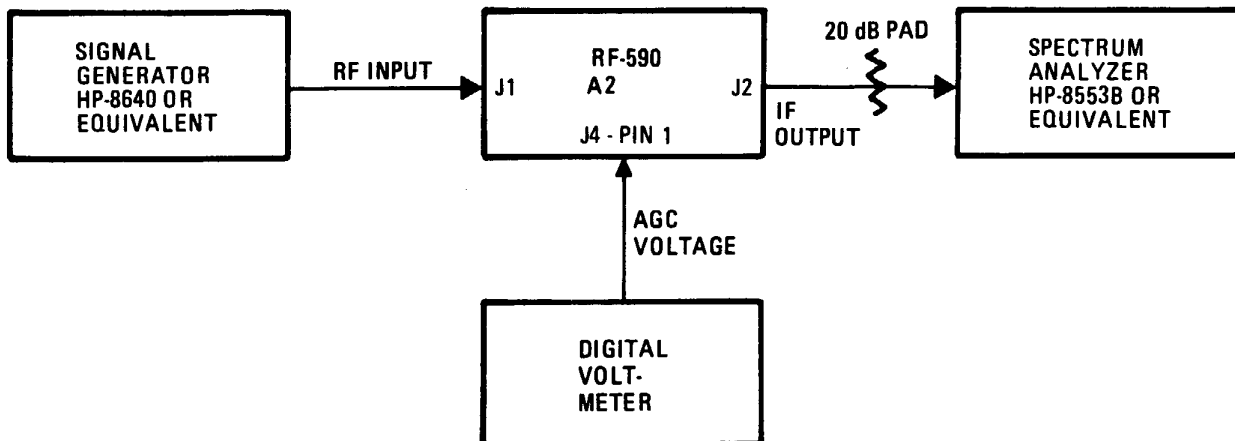
Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

- b. Connect equipment as shown in figure 2.



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Figure 2. A2 AGC Test Setup

- c. Adjust signal generator to approximately 0 dBm at 10.000000 MHz. Monitor IF output J2 on spectrum analyzer. IF output must be 0 dBm  $\pm$  2 dB.
- d. Slowly turn RF-590 RF Gain Control counterclockwise (ccw). An AGC voltage range of 0 to -10 Vdc should result in an IF output gain reduction range of approximately 0 to -30 dB. Intermediate levels are given in table 2.

Table 2. A2 AGC - Gain Reduction Data

AGC Voltage, Volts	Gain Reduction, - dB
0	0
-1	9
-2	17
-3	21
-4	23
-5	25
-6	27
-7	28
-8	29
-9	30
-10	31

**4.4 BITE Test/Alignment**

- a. Set RF-590 controls as follows:

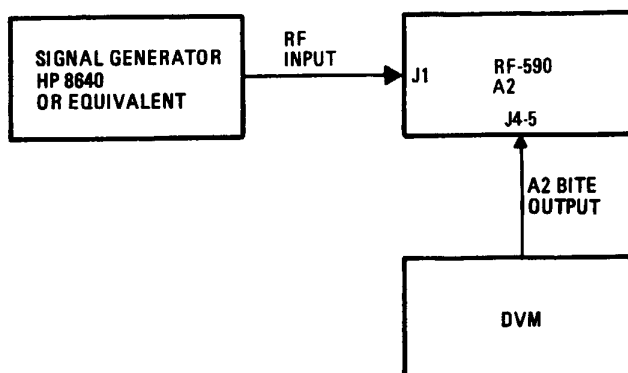
Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

- b. Connect equipment as shown in figure 3.



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Figure 3. A2 BITE Test Setup

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- c. Set signal generator to 10.000000 MHz, -20 dBm. Adjust L8 for a peak indication on the DVM. DVM should indicate approximately .75 Vdc.
- d. Disconnect all equipment and reconnect A2 to RF-590. Initiate RF-590 BITE test. The receiver must pass 02 testing.

**5. PARTS LIST**

Table 3 is a comprehensive parts list of all replaceable components in First Converter Assembly A2. When ordering parts from the factory, include a full description of the part. Use figure 4, First Converter Assembly A2 Component Location diagram to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 5 is the First Converter Assembly A2 Schematic Diagram

**Table 3. First Converter Assembly A2 Parts List (PL 10073-5200)**

Ref. Desig.	Part Number	Description
	10073-5200	PWB, FIRST CONVERTER
	E70-0002-002	PAD MNT XSTR TO-5
	E70-0001-007	INSL BEO TO-5 X.015 THK
	E70-0011-001	INSL XSTR UNIVERSAL HOLE
C1	CM04ED330J03	CAP 33PF 5% 500V MICA
C2	CM04ED330J03	CAP 33PF 5% 500V MICA
C3	M39014/01-1535	CAP .01UF 20% 100V CER
C4	M39014/01-1535	CAP .01UF 20% 100V CER
C5	M39014/01-1535	CAP .01UF 20% 100V CER
C6	M39014/01-1535	CAP .01UF 20% 100V CER
C7	C26-0025-100	CAP 10UF 20% 25V TANT
C8	C26-0025-100	CAP 10UF 20% 25V TANT
C9	M39014/01-1535	CAP .01UF 20% 100V CER
C10	M39014/01-1535	CAP .01UF 20% 100V CER
C11	M39014/01-1535	CAP .01UF 20% 100V CER
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	M39014/01-1535	CAP .01UF 20% 100V CER
C14	M39014/01-1535	CAP .01UF 20% 100V CER
C15	M39014/01-1535	CAP .01UF 20% 100V CER
C16	CM04CD150J03	CAP 15PF 5% 500V MICA
C17	CM04CD150J03	CAP 15PF 5% 500V MICA
C18	M39014/01-1535	CAP .01UF 20% 100V CER
C19	CM04ED330J03	CAP 33PF 5% 500V MICA
C20	CM04ED330J03	CAP 33PF 5% 500V MICA
C21	M39014/01-1535	CAP .01UF 20% 100V CER
C22	M39014/01-1535	CAP .01UF 20% 100V CER
C23	M39014/01-1535	CAP .01UF 20% 100V CER
C24	M39014/01-1535	CAP .01UF 20% 100V CER

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Table 3. First Converter Assembly A2 Parts List (PL 10073-5200) (Cont.)

Ref. Desig.	Part Number	Description
C25	M39014/01-1535	CAP .01UF 20% 100V CER
C26	CM04CD050D03	CAP 5PF +- .5PF 500V MICA
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	C26-0025-339	CAP 3.3UF 20% 25V TANT
C29	M39014/01-1535	CAP .01UF 20% 100V CER
C30	M39014/01-1535	CAP .01UF 20% 100V CER
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	M39014/01-1535	CAP .01UF 20% 100V CER
C33	CM04ED390J03	CAP 39PF 5% 500V MICA
C34	M39014/01-1535	CAP .01UF 20% 100V CER
C35	M39014/01-1535	CAP .01UF 20% 100V CER
C36	M39014/01-1535	CAP .01UF 20% 100V CER
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/01-1535	CAP .01UF 20% 100V CER
C39	C26-0025-339	CAP 3.3UF 20% 25V TANT
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/01-1535	CAP .01UF 20% 100V CER
C42	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	C26-0025-339	CAP 3.3UF 20% 25V TANT
C44	M39014/01-1535	CAP .01UF 20% 100V CER
C45	CM04CD050D03	CAP 5PF +- .5PF 500V MICA
C46	CM04ED510J03	CAP 51PF 5% 500V MICA
C47	CM04ED510J03	CAP 51PF 5% 500V MICA
C48	C26-0025-339	CAP 3.3UF 20% 25V TANT
C49	M39014/01-1535	CAP .01UF 20% 100V CER
C50	M39014/01-1535	CAP .01UF 20% 100V CER
C51	M39014/01-1535	CAP .01UF 20% 100V CER
C52	M39014/01-1535	CAP .01UF 20% 100V CER
CR1	D12-0007-001	DIODE 1W 75V PIN SW
CR2	D12-0007-001	DIODE 1W 75V PIN SW
CR3	1N4454	DIODE 200mA 75V SW
CR4	1N4454	DIODE 200mA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N5231B	DIODE 5.1V 5% .5W ZENER
FL1	10073-7000	FILTER,40.455 MHZ
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0032-005	HDR 5 PIN 0.100" SR
L1	MS14046-4	COIL 10UH 10% FXD RF
L2	MS14046-4	COIL 10UH 10% FXD RF
L3	MS14046-4	COIL 10UH 10% FXD RF
L4	MS14046-4	COIL 10UH 10% FXD RF
L5	L08-0001-001	CHOKE W B 50 MHZ
L6	L11-0004-005	INDUCT SH VAR .198-.242UH

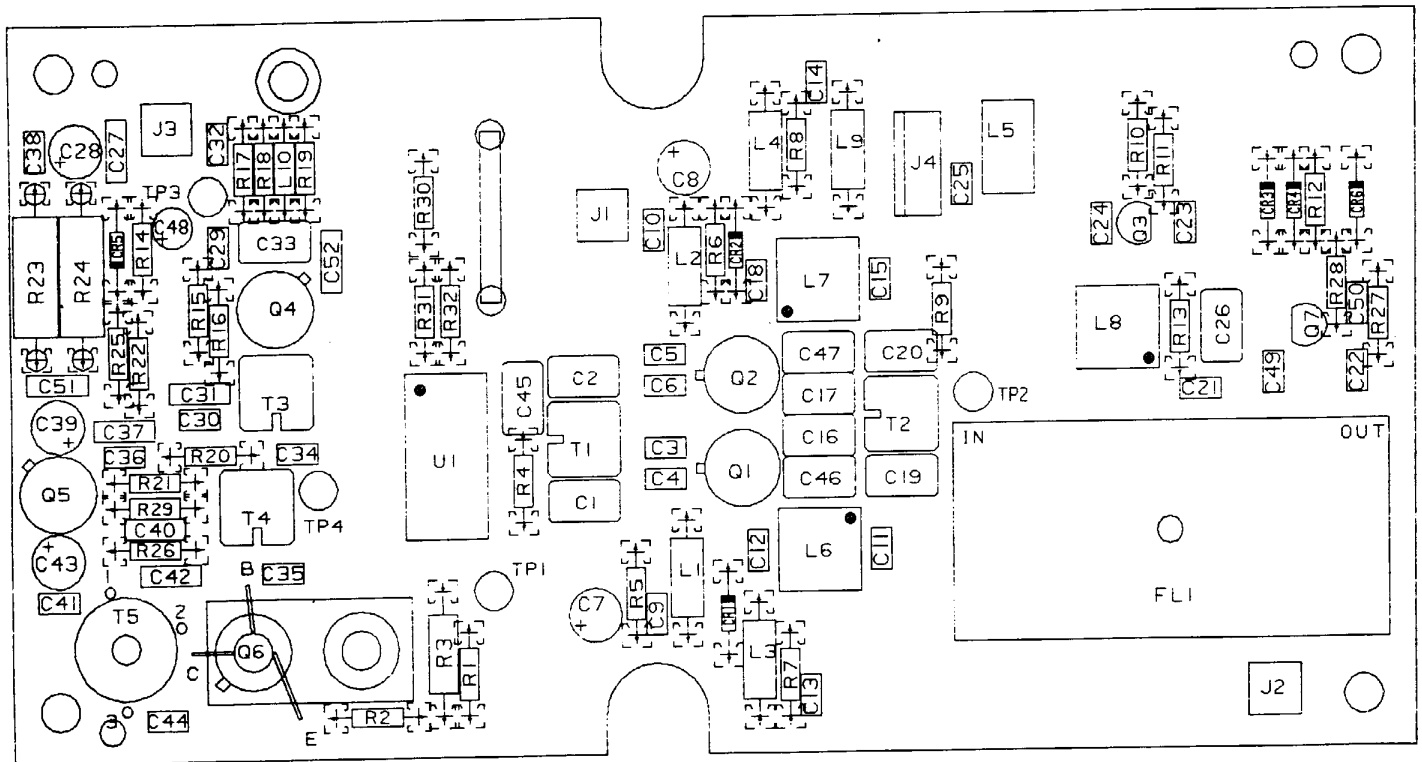
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**Table 3. First Converter Assembly A2 Parts List (PL 10073-5200) (Cont.)**

Ref. Desig.	Part Number	Description
L7	L11-0004-005	INDUCT SH VAR .198-.242UH
L8	L11-0004-013	INDUCT SH VAR .900-1.1 UH
L9	MS90538-12	COIL 100UH 5% FXD RF
L10	MS75084-12	COIL 10UH 10% FXD RF
Q1	Q35-0004-001	XSTR JFET U431
Q2	Q35-0004-001	XSTR JFET U431
Q3	Q35-0001-001	XSTR JFET J310
Q4	2N3866	XSTR SS/RF NPN TO-39
Q5	2N4037	XSTR SS/RF NPN TO-39
Q6	Q25-0014-000	XSTR RFPWR
Q7	Q35-0001-001	XSTR JFET J310
R1	R65-0003-301	RES 300 5% 1/4W CAR FILM
R2	R65-0003-301	RES 300 5% 1/4W CAR FILM
R3	RCR20G180JM	RES,18 5% 1/2W CAR COMP
R4	R65-0003-510	RES 51 5% 1/4W CAR FILM
R5	R65-0003-910	RES 91 5% 1/4W CAR FILM
R6	R65-0003-910	RES 91 5% 1/4W CAR FILM
R7	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R8	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R9	R65-0003-510	RES 51 5% 1/4W CAR FILM
R10	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R11	R65-0003-181	RES 180 5% 1/4W CAR FILM
R12	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R13	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R14	R65-0003-100	RES 10 5% 1/4W CAR FILM
R15	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R16	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R17	R65-0003-270	RES 27 5% 1/4W CAR FILM
R18	R65-0003-221	RES 220 5% 1/4W CAR FILM
R19	R65-0003-680	RES 68 5% 1/4W CAR FILM
R20	R65-0003-101	RES 100 5% 1/4W CAR FILM
R21	R65-0003-681	RES 680 5% 1/4W CAR FILM
R22	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R23	RCR32G100JM	RES,10 5% 1W CAR COMP
R24	RCR32G100JM	RES,10 5% 1W CAR COMP
R25	R65-0003-301	RES 300 5% 1/4W CAR FILM
R26	R65-0003-101	RES 100 5% 1/4W CAR FILM
R27	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R28	R65-0003-181	RES 180 5% 1/4W CAR FILM
R29	R65-0003-101	RES 100 5% 1/4W CAR FILM
R30	R65-0003-431	RES 430 5% 1/4W CAR FILM
R31	R65-0003-120	RES 12 5% 1/4W CAR FILM
R32	R65-0003-431	RES 430 5% 1/4W CAR FILM
T1	10073-7013	TRANSFORMER ASSY
T2	10073-7013	TRANSFORMER ASSY

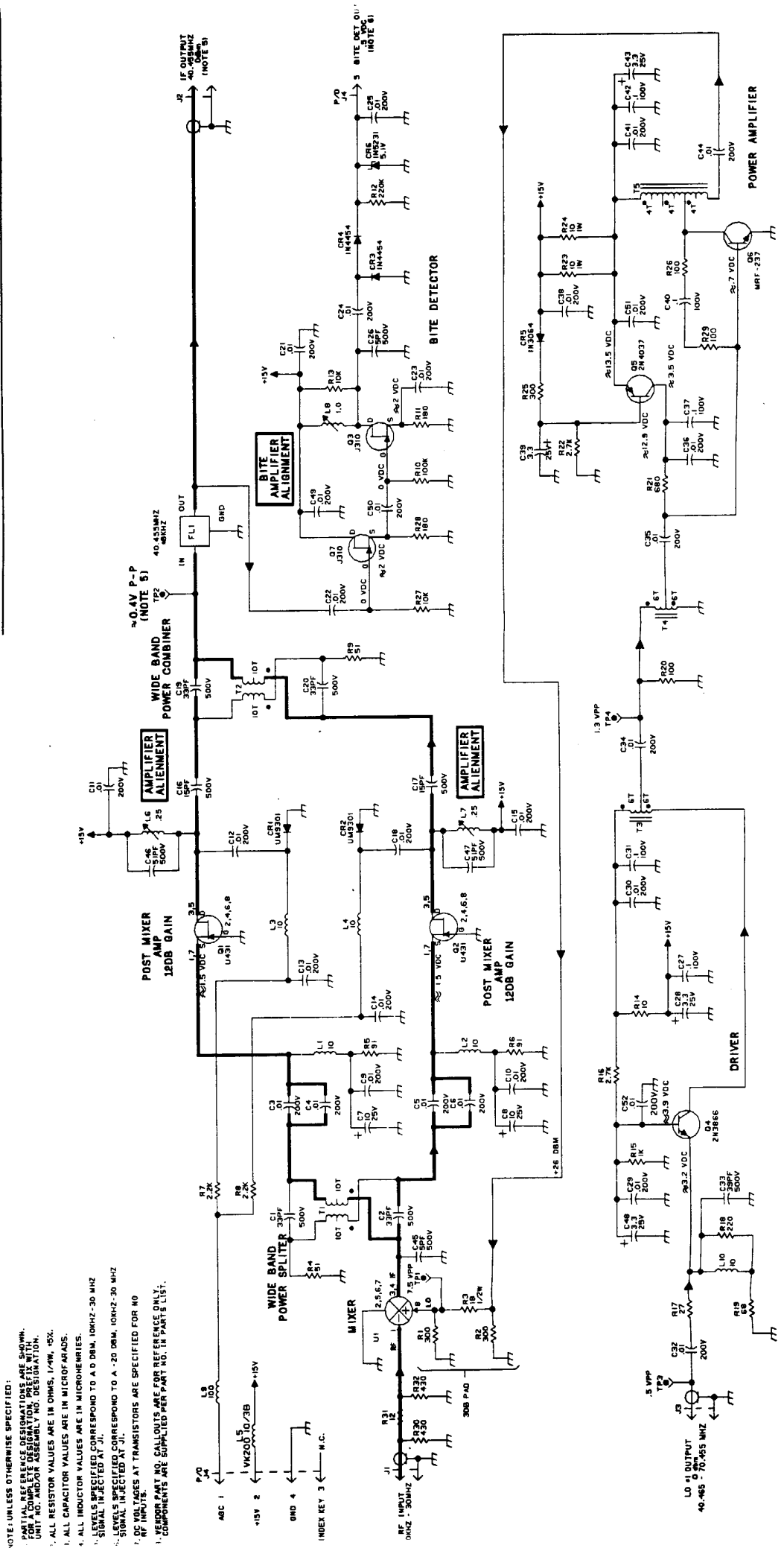
**Table 3. First Converter Assembly A2 Parts List (PL 10073-5200)**

Ref. Desig.	Part Number	Description
T3	10073-7005	TRANSFORMER, RF, FIXED
T4	10073-7005	TRANSFORMER, RF, FIXED
T5	10073-7010	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
U1	151-0003-002	MIXER DB 500MW 500MHZ



**Figure 4. First Converter Assembly A2 Component Location Diagram (10073-5200, Rev. F)**





NOTE: UNLESS OTHERWISE SPECIFIED:  
 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.  
 ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.  
 ALL CAPACITOR VALUES ARE IN MICROFARADS.  
 ALL INDUCTOR VALUES ARE IN MICROHENRIES.  
 LEVELS SPECIFIED CORRESPOND TO A -20 DBM, 10KHZ-30 MHZ  
 SIGNAL INJECTED AT J1.  
 LEVELS INJECTED AT J2 CORRESPOND TO A -20 DBM, 10KHZ-30 MHZ  
 SIGNAL INJECTED AT J1.  
 DC VOLTAGES AT TRANSISTORS ARE SPECIFIED FOR NO  
 RF INPUTS.  
 VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY.  
 COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

Figure 5. First Converter Assembly A2 Schematic Diagram (10073-5201, Rev. G)

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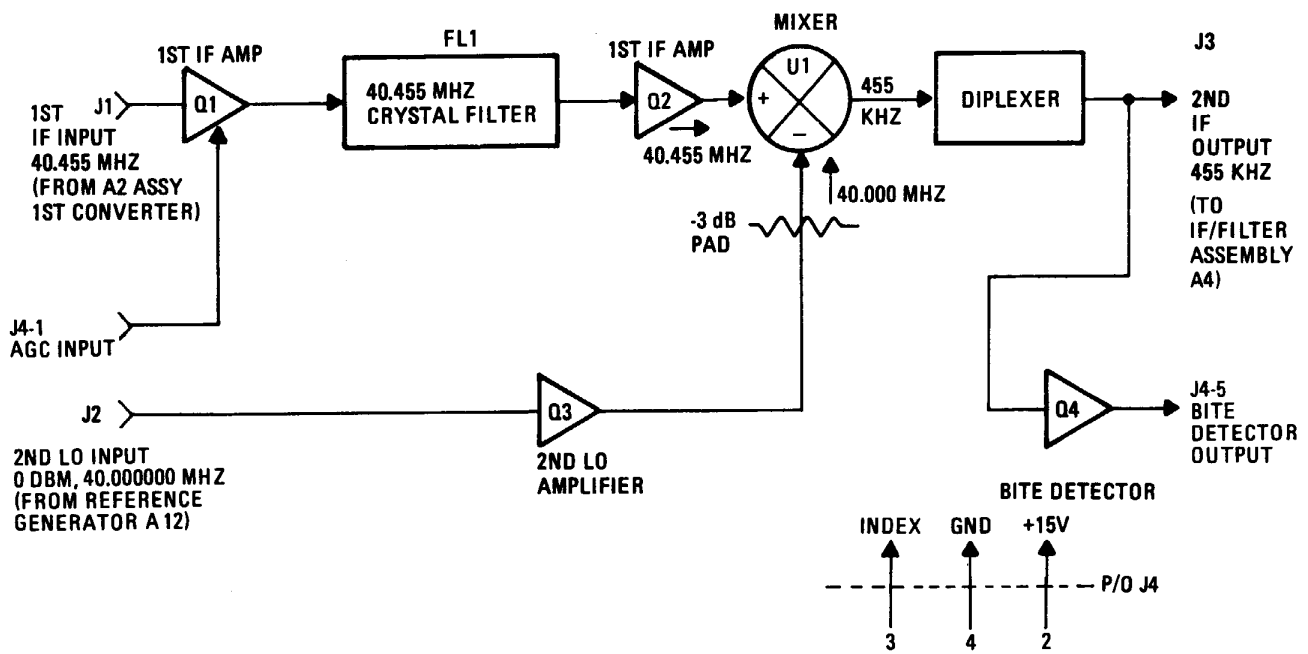
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Second Converter Assembly A3 Functional Block Diagram

**1. GENERAL DESCRIPTION**

Second Converter Assembly A3 converts the first IF of 40.455 (from First Converter Assembly A2) to a second IF of 455 kHz. Overall module gain from J1 to J3 is approximately  $14 \pm 2$  dB.

Input 40.455 MHz first IF signals are applied through an automatic gain controlled amplifier, a 40.455 MHz, 16 kHz wide crystal filter, and on to a fixed gain stage. At this point the signal is down converted to 455 kHz, filtered, and fed out to IF Filter Assembly A4. The second IF signal is also monitored by the BITE detection circuit which monitors the operation of the Second Converter Assembly.

**2. INTERFACE CONNECTIONS**

Table 1 details the various input/output connections and any relevant data.

**Table 1. Second Converter A3 Interface Connections**

Connector	Function	Characteristics
J1	First IF Input	40.455 MHz, -120/-9 dBm (under AGC control), $Z_o = 50$ ohms
J2	Second LO Input	40.000 MHz, 0 dBm, $Z_o = 50$ ohms
J3	Second IF Output	455 kHz, -107/-15 dBm (under AGC control), $Z_o = 50$ ohms
J4-1	AGC Input	0 to -6 Vdc produces a 0 to -20 dB gain reduction
J4-2	Power	+15 Vdc at 60 mA
J4-3	Index pin	
J4-4	Ground	
J4-5	BITE Output	2.25 - 3 Vdc for -20 dBm input at J1

**3. CIRCUIT DESCRIPTION**

**3.1 IF Amplifiers and Mixer**

First IF input signals from First Converter Assembly A2 are received at J1 and fed to grounded gate FET amplifier Q1. C1 and L4 perform an impedance transformation of 50 ohms to Q1's source impedance for optimum power gain. C2 and R1 form a bypassed bias resistor network. L1, C25, and C5 provide impedance transformation for Q1's drain load of 2200 ohms to FL-1's input impedance of 50 ohms. This yields an overall stage gain of 13 dB.

CR1 provides gain reduction by reducing Q1's drain load upon application of a negative AGC voltage at R2 (AGC input). Typically -20 dB of gain reduction is possible.

Filtering is applied at FL-1, a 40.455 MHz crystal filter whose -3 dB bandwidth is  $\pm 8$  kHz. Typical insertion loss is -3.5 dB. FL-1 output is applied to grounded gate FET amplifier Q2. Q2 and its associated components perform identically to amplifier Q1, except that no AGC is applied. This fixed gain stage also has an overall gain of 13 dB.

U1 is a low LO level diode ring mixer that converts the 40.455 MHz first IF to the 455 kHz second IF. A LO drive level of +7 dBm (50 ohm) at 40.000000 MHz is supplied by Q3 (paragraph 3.3). U1 typically has 6 dB of conversion loss.

Components C10 - C12, L6 - L8, and R5 form a diplexer with a cutoff frequency of 4 MHz to terminate all undesired mixer products (especially LO leakage) into 50 ohms. This allows only 455 kHz to pass out of J3 to IF Filter Assembly A4 and ultimately to the high gain second IF amplifiers on IF/Audio Assembly A5.

### 3.2 BITE Detection Circuit

The 455 kHz second IF signal is also applied to common emitter amplifier Q4. Bias circuitry R7, R8, and R11 bias Q4 to 10 mA of collector current. R9, R10, and C16 set the voltage gain to allow BITE to operate when the signal at J1 is at -20 dBm. The dc detection voltage produced by detector network CR2, CR4, and C17 under these conditions is approximately 2.25 to 3 Vdc at J4-5, BITE Detector output.

### 3.3 LO No. 1 Amplifier

Common emitter amplifier Q3 receives a 40.000000 MHz, 0 dBm drive signal from Reference Generator Assembly A12 at J2. R14, R15, CR3, and R17 bias Q3 to 23 mA of collector current. R16-C21 and R18 comprise emitter and collector to base feedback networks. These networks simultaneously set the stage gain to +10 dB and the input and output impedances to 50 ohms. A +10 dBm signal is fed to -3 dB, 50 ohm pad R19-R21. This applies a +7 dBm LO level to mixer U1.

## 4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests should be performed with all assembly connections in normal contact unless otherwise specified.

### 4.1 LO No. 1 Amplifier Test

- a. Set RF-590 controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

- b. Monitor TP4 with an oscilloscope and frequency counter. Signal at TP4 would be 40.000000 MHz at approximately 1.3 Vpp.

#### 4.2 IF Amplifiers and Mixer Adjustments/Test

- a. Remove the ribbon cable connecting the AGC assembly to the IF/Audio Amp Assembly A5A1.

- b. Set RF-590 controls as follows:

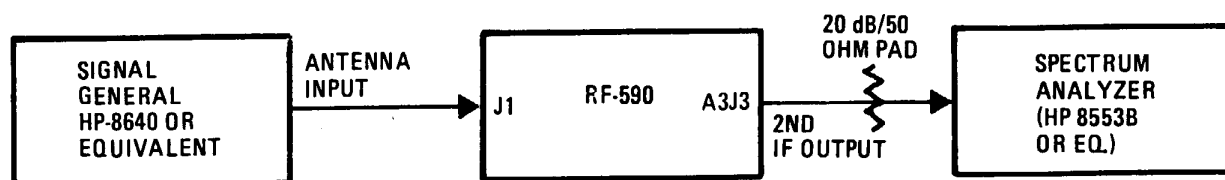
Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

- c. Connect equipment as shown in figure 1.



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Figure 1. A3 IF Amplifier Test Setup

- d. Apply a -70 dBm, 10.0015 MHz signal at J1. Monitor second IF output J3 at 455 kHz on the spectrum analyzer. Adjust L1 and L2 for maximum output. Output must be -55 dBm  $\pm$  2 dB, indicating approximately 15 dB of module gain.

#### 4.3 AGC Test

- a. Set RF-590 controls as follows:

Frequency: 10.000000 MHz

Mode: USB

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AGC: OFF  
RF Gain: Fully clockwise (cw)

b. Connect equipment as shown in figure 2.

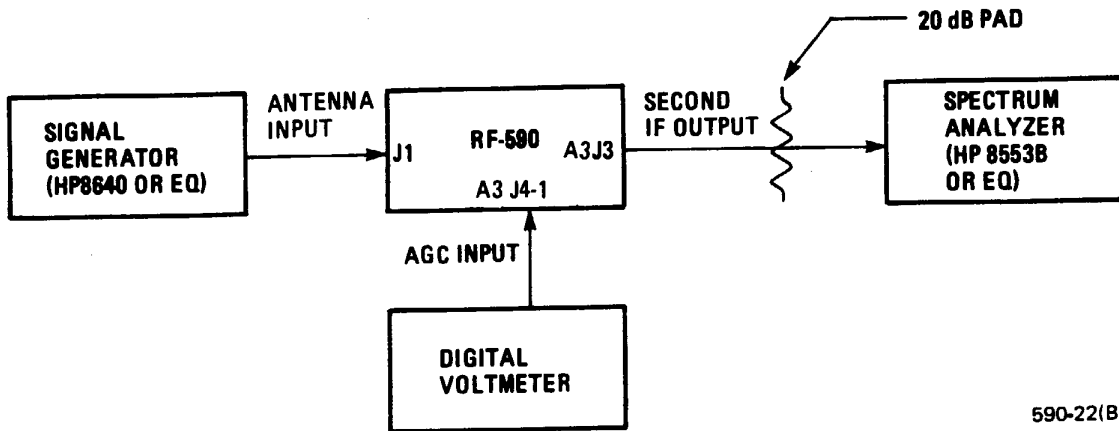


Figure 2. A3 AGC Test Setup

- c. Adjust Signal Generator to -30 dBm, 10.0015 MHz. Monitor second IF output J3 on spectrum analyzer. IF output must be -15 dBm  $\pm$  3 dB.
- d. Slowly adjust RF-590 RF gain control counterclockwise (ccw). An AGC voltage range of 0 to -6 Vdc should result in an IF output gain reduction of approximately 0 to -20 dB. Intermediate levels are given in table 2. Reset RF gain control fully clockwise (cw).

Table 2. A3 AGC - Gain Reduction Data

AGC Voltage, Volts	Gain Reduction, - dB
0	0
-1	18
-2	32
-3	40
-4	45
-5	49
-6	52
-7	54
-8	56
-9	58

#### 4.4 BITE Test

- a. Set RF-590 controls as follows:

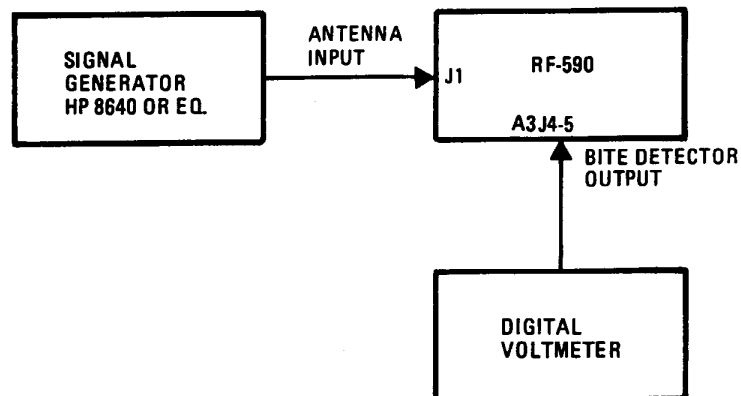
Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

- b. Connect equipment as shown in figure 3.



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Figure 3. A3 BITE Test Setup

- c. Set signal generator to -20 dBm at 40.455 MHz. BITE output voltage must be approximately 2.25 -3 Vdc.
- d. Disconnect all equipment and reconnect A3 to RF-590. Initiate RF-590 BITE test. The receiver must pass 03 testing.

#### 5. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in Second Converter Assembly A3. When ordering parts from the factory, include a full description of the part. Use figure 4, the Second Converter Assembly component location diagram to identify parts.

#### 6. SCHEMATIC DIAGRAM

Figure 5 is the Second Converter Assembly schematic diagram.



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**Table 3. Second Converter Assembly A3 Parts List (PL 10073-5300)**

Ref. Desig.	Part Number	Description
	10073-5300	PWB, 2ND CONVERTER
	E70-0002-002	PAD MNT XSTR TO-5
C1	CM04FD111J03	CAP 110PF 5% 500V MICA
C2	CK05BX103M	CAP .01UF 20% 100V CER
C3	CK05BX103M	CAP .01UF 20% 100V CER
C4	CK05BX103M	CAP .01UF 20% 100V CER
C5	CM04CD120J03	CAP 12PF 5% 500V MICA
C6	CM04FD111J03	CAP 110PF 5% 500V MICA
C7	CK05BX103M	CAP .01UF 20% 100V CER
C8	CK05BX103M	CAP .01UF 20% 100V CER
C9	CM04CD120J03	CAP 12PF 5% 500V MICA
C10	CM04FA391J03	CAP 390PF 5% 100V MICA
C11	CM04FA391J03	CAP 390PF 5% 100V MICA
C12	CM06FD182J03	CAP 1800PF 5% 500V MICA
C13	M39014/02-1320	CAP .47UF 10% 50V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1320	CAP .47UF 10% 50V CER-R
C16	M39014/02-1320	CAP .47UF 10% 50V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	CK05BX103M	CAP .01UF 20% 100V CER
C19	CK05BX103M	CAP .01UF 20% 100V CER
C20	CK05BX103M	CAP .01UF 20% 100V CER
C21	CK05BX103M	CAP .01UF 20% 100V CER
C22	CK05BX103M	CAP .01UF 20% 100V CER
C23	M39014/02-1320	CAP .47UF 10% 50V CER-R
C24	CM04CD070D03	CAP 7PF +-.5PF 500V MICA
C25	CM04CD070D03	CAP 7PF +-.5PF 500V MICA
C26	CK05BX103M	CAP .01UF 20% 100V CER
CR1	D12-0007-001	DIODE 1W 75V PIN SW
CR2	1N4454	DIODE 200mA 75V SW
CR3	1N4454	DIODE 200mA 75V SW
CR4	1N4454	DIODE 200mA 75V SW
FL1	10073-7001	FILTER
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0032-005	HDR 5 PIN 0.100" SR
L1	L11-0004-011	INDUCT SH VAR .612-.748UH
L2	L11-0004-011	INDUCT SH VAR .612-.748UH
L3	MS14046-6	COIL 15UH 10% FXD RF
L4	MS18130-3	COIL .33UH 10% FXD RF
L5	MS18130-3	COIL .33UH 10% FXD RF
L6	MS18130-8	COIL 1.0UH 10% FXD RF
L7	MS18130-15	COIL 3.9UH 10% FXD RF
L8	MS18130-15	COIL 3.9UH 10% FXD RF

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**Table 3. Second Converter Assembly A3 Parts List (PL 10073-5300) (Cont.)**

Ref. Desig.	Part Number	Description
L9	MS14046-6	COIL 15UH 10% FXD RF
L10	MS90539-15	COIL 1000UH 5% FXD RF
Q1	Q35-0001-001	XSTR JFET J310
Q2	Q35-0001-001	XSTR JFET J310
Q3	2N5109	XSTR RFPWR NPN TO-39
Q4	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-181	RES 180 5% 1/4W CAR FILM
R2	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R3	R65-0003-181	RES 180 5% 1/4W CAR FILM
R4	R65-0003-101	RES 100 5% 1/4W CAR FILM
R5	R65-0003-510	RES 51 5% 1/4W CAR FILM
R6	R65-0003-101	RES 100 5% 1/4W CAR FILM
R7	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R8	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R9	R65-0003-561	RES 560 5% 1/4W CAR FILM
R10	R65-0003-270	RES 27 5% 1/4W CAR FILM
R11	R65-0003-431	RES 430 5% 1/4W CAR FILM
R12	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R13	R65-0003-101	RES 100 5% 1/4W CAR FILM
R14	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R15	R65-0003-471	RES 470 5% 1/4W CAR FILM
R16	R65-0003-399	RES 3.9 5% 1/4W CAR FILM
R17	R65-0003-101	RES 100 5% 1/4W CAR FILM
R18	R65-0003-681	RES 680 5% 1/4W CAR FILM
R19	R65-0003-301	RES 300 5% 1/4W CAR FILM
R20	R65-0003-180	RES 18 5% 1/4W CAR FILM
R21	R65-0003-301	RES 300 5% 1/4W CAR FILM
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	I51-0003-001	MIXER DB 50mW 500MHZ



NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS, 200VDC.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. LEVELS SPECIFIED ARE FOR A -30 DBM, 40.455 MHZ SIGNAL INJECTION AT J1.
6. LEVELS SPECIFIED ARE FOR A -20 DBM, 40.455 MHZ SIGNAL INJECTION AT J1.
7. DC VOLTAGES AT TRANSISTORS ARE SPECIFIED FOR NO RF INPUT.

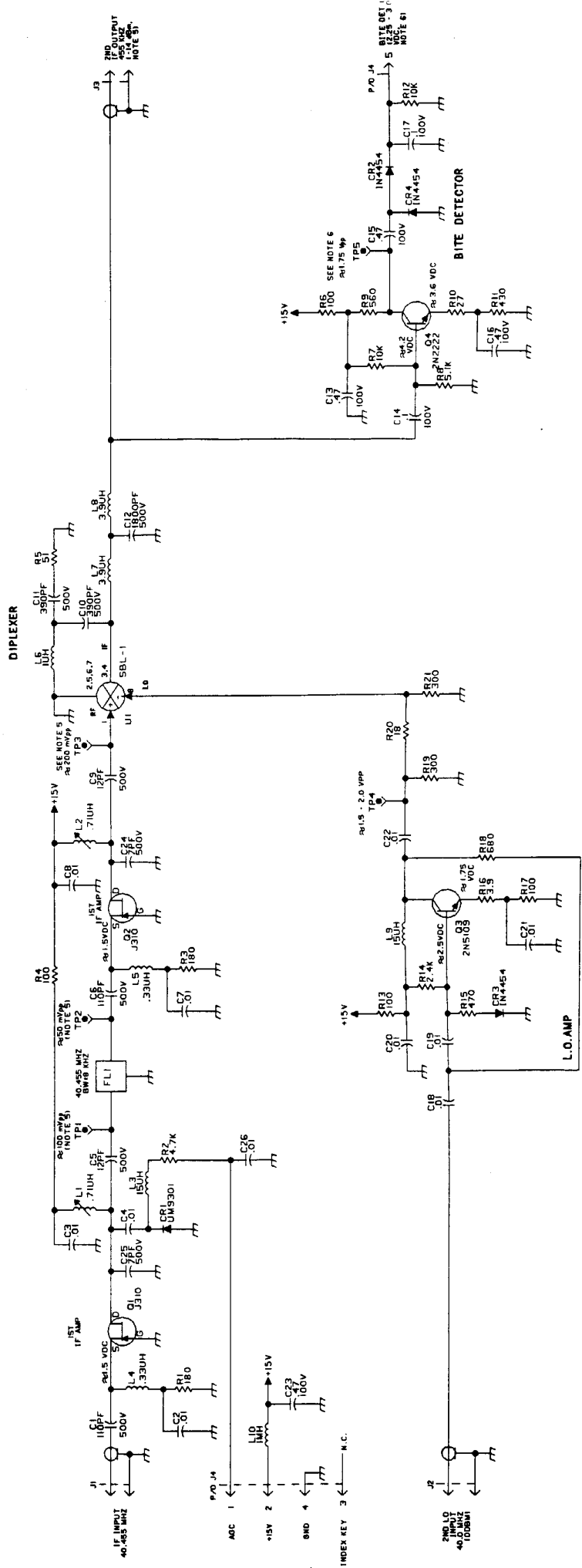


Figure 5. Second Converter Assembly A3 Schematic Diagram (10073-5301, Rev.

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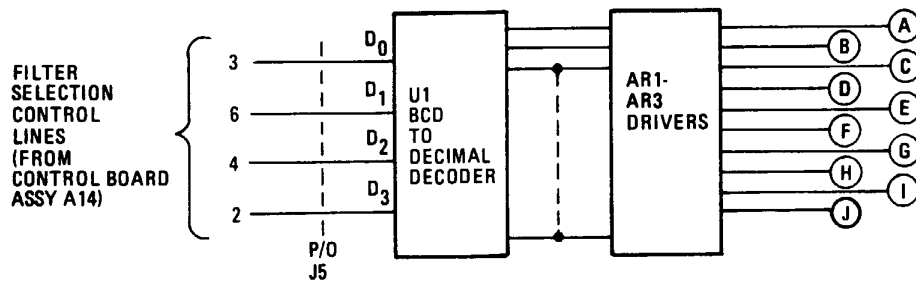
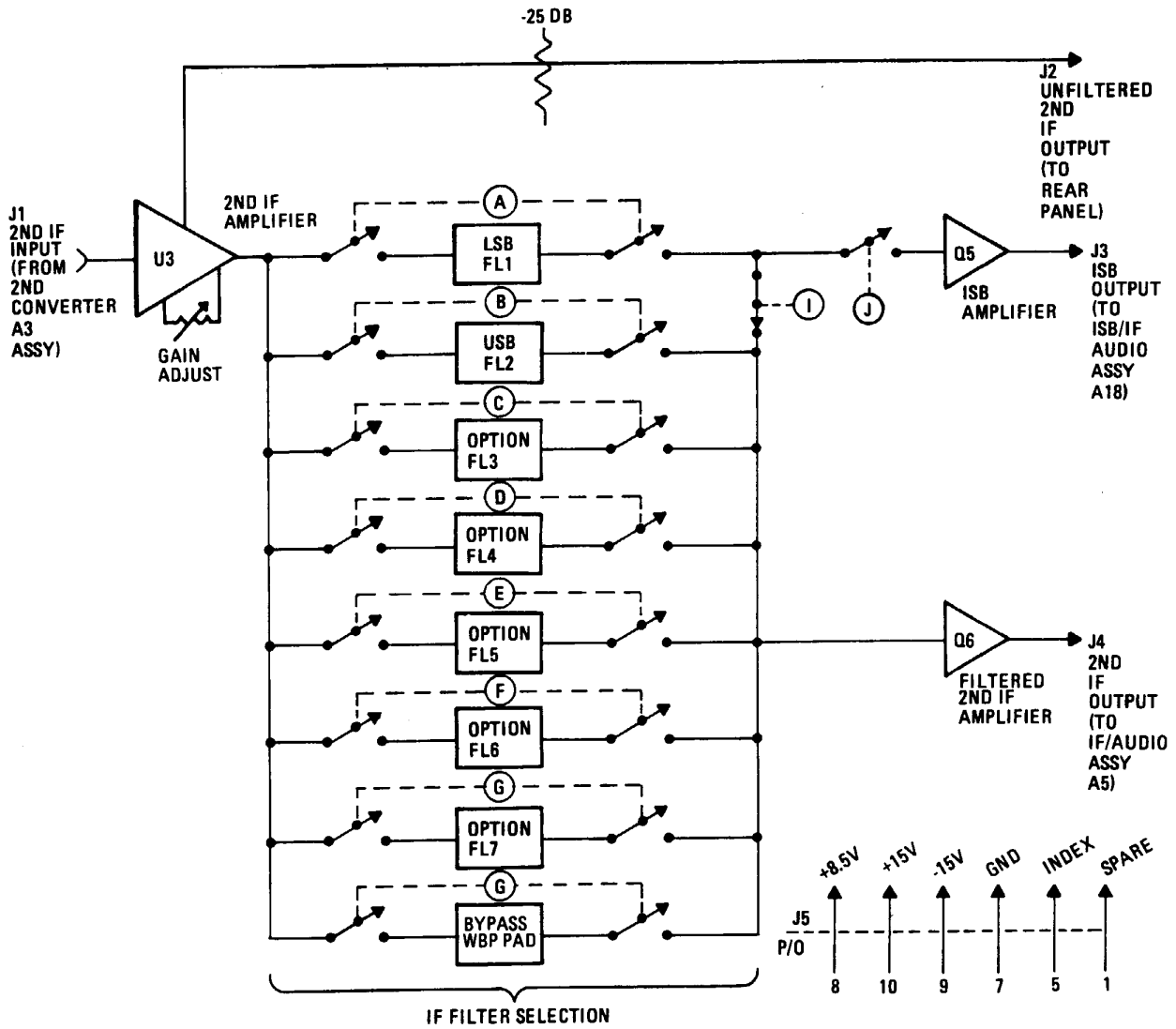
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**IF Filter Assembly A4 Functional Block Diagram**

**1. GENERAL DESCRIPTION**

IF Filter Assembly A4 contains provisions for automatically selecting one of seven bandpass filters or one filter bypass function, which is a resistive pad. The main signal frequency selectivity is determined by these filters. Actual filter bandwidths which may be employed are customer specified and depend upon operational modes desired (see note below). Table 1 shows a typical filter complement in the RF-590. Automatic filter selection is accomplished via flexible programmable logic circuitry on Control Board Assembly A14.

**NOTE**

Filter positions FL1 and FL2 must be reserved for LSB and USB (respectively) if ISB operation is desired. (ISB operation requires the simultaneous selection of two filters). WBP Pad is an R.C. filter pad network and is used for standard AM 16 kHz bandwidth and FM 16 kHz bandwidth operation.

**Table 1. Typical RF-590 Filter Complement**

Mode of Operation	Filter Selected	Specified Bandwidth
LSB	FL1	2.8 kHz
USB	FL2	2.8 kHz
CW	FL3	.3 kHz
CW	FL4	1.0 kHz
AM	FL5	3.2 kHz
AM	FL6	6.8 kHz
Optional	FL7	--
FM or AM	WBP Pad	16 kHz (Bypass)

Input signals at 455 kHz (nominally) arrive at J2 from Second Converter Assembly A3. Three A4 signal outputs are derived.

- Filtered Second IF output at J4. This output is fed to IF/Audio Assembly A5, and is chosen whenever SSB, AM, or FM detection is required.

- ISB output at J3. This output is fed to ISB IF/Audio Assembly A18 and is used whenever Independent Sideband (ISB) reception of LSB and USB signals is simultaneously required. Under these conditions, J3 carries the LSB signal to the A18 Assembly while J4 routes the USB signal to the A5 Assembly. Note that ISB IF/Audio Assembly A18 is an optional assembly, and ISB operation is not possible unless the RF-590 is equipped with it.
- Unfiltered second IF output at J2. This output is fed to RF-590 rear panel connector J3, and is provided as a convenience whenever external signal processing of the wideband signal (present at J1) is required.

Overall assembly gain is set by R10 to nominally be 10 dB at J4 in the USB mode of operation. This also sets the ISB output (when used) to 10 dB, and the unfiltered second IF output to approximately 4 dB.

## 2. INTERFACE CONNECTIONS

Table 2 details the various input/output connections and other relevant data.

**Table 2. IF Filter Assembly A4 Interface Connections**

Connector	Function	Characteristics
J1	Unfiltered second IF input	455 kHz, -107/-15 dBm, $Z_o = 50$ ohms
J2	Unfiltered second IF output	455 kHz, -103/-11 dBm, $Z_o = 50$ ohms
J3	ISB output	455 kHz, -97/-5 dBm, $Z_o = 50$ ohms
J4	Filtered second IF output	455 kHz, -97/-5 dBm, $Z_o = 50$ ohms
J5-1	Spare	
J5-2	D3	*
J5-3	D0	*
J5-4	D2	*
J5-5	Index pin	
J5-6	D1	*
J5-7	Ground	
J5-8	Power	+8.5 V at 8 mA
J5-9	Power	-15 V at 30 mA
J5-10	Power	+15 V at 100 mA

\* Filter select line: 0 = ground, 1 = +5 V



### 3. CIRCUIT DESCRIPTION

#### 3.1 Input/Output Amplifiers

Unfiltered second IF signals at J1 are applied to second IF amplifier U3. U3 provides +27 dB (nominal) of gain at each of two outputs, adjustable by R10. The output at pin 8 drives the selected filter input, and is adjusted by R10 for a nominal assembly gain of 10 dB with the USB filter selected.

The second U3 output at pin 7 is applied through 50 ohm matching network R75 and R77 to J2. This unfiltered 455 kHz IF output is then routed to RF-590 rear panel connector J2. Output level under AGC action at this port is typically -103/-11 dBm into 50 ohms.

Output source follower FET amplifier Q6 matches the high impedance filter outputs (5 K ohms) to the low impedance IF/Audio Assembly A5 input (50 ohms). Q6 may normally receive signals from any of the filters, depending upon the filter selected. However, when the ISB option is used, diode logic steers only USB information to Q6, while LSB information is steered to Q5 (see paragraph 3.2).

Output amplifier Q5 is essentially identical to Q6, except that it is used only when the ISB option is used, and then will only carry ISB (LSB) information. ISB signals would then pass through J3 ISB output to ISB IF/Audio Assembly A18. Q5 is turned off by Q4 when the radio is not in the ISB mode (see paragraph 3.2).

#### 3.2 Filter Selection

Automatic filter selection control originates on Control Assembly A14 in response to operator entries via the front panel controls. Control line inputs D0-D3 carry BCD control signals to BCD to decimal decoder U1. U1 outputs (as a function of control line inputs) are shown in table 3. U1 outputs are normally low (0 volts) until they are selected, and then switch high (5 volts).

U1 outputs, in turn, selectively drive switches AR1-AR3. These switches then select the appropriate filter by putting -15 Vdc on the associated filter control line, while holding all other lines at +15 Vdc.

As an example, consider the selection of FL3. U1 filter select control lines would be D0 = 1, D1 = 1, D2 = 0, and D3 = 0. This would cause only U1, pin 15, to switch high (+5 Vdc); all other outputs would remain low. This 5 volt level causes switch AR1-A, pin 13, (-) input to exceed the 2 volt level at AR1-A, pin 12 (+), which forces the output, pin 14, to swing to -15 Vdc. Note that at this time, all other switch outputs would be at +15 Vdc.

The -15 Vdc potential at AR1-A, pin 14, now forward biases CR12 and CR15, while reverse biasing CR13 and CR14. Any signal present at amplifier U3 output would now be allowed to only pass through FL3 to buffer amplifier Q6. Diodes associated with all other filters would prevent any signal from passing through these filters.

Table 3. A4 Filter Selection

Filter Position Chosen	Mode	Control Line Inputs				Selected Output Pin No.	Output Amplifier Used
		U1-10 D0	U1-13 D1	U1-12 D2	U1-11 D3		
FL1	LSB	0	1	0	0	2	Q6
FL2	USB	0	0	0	0	3	Q6
*FL1, FL2	ISB	1	0	0	0	14	Q5 and Q6
*FL1, FL2	ISB/LSB	1	0	0	1	5	Q5 and Q6
FL3	CW	1	1	0	0	15	Q6
FL4	CW	0	0	1	0	1	Q6
FL5	AM	1	0	1	0	6	Q6
FL6	AM	0	1	1	0	7	Q6
FL7	Optional	1	1	1	0	4	Q6
WBP Pad	Bypass	0	0	0	1	9	Q6

\*Software Dependent

If some other filter is selected, U1, pin 15, would now switch low (0 Vdc). This triggers AR1-A, pin 14, to swing to +15 Vdc. This level reverse biases CR12 and CR15 (preventing any signal from passing through FL3), while forward biasing CR13 and CR14 (which would short out any signal that did appear there).

### 3.2.1 ISB Operation

During ISB operation, U1, pin 14, is selected, allowing AR2-A and AR3-A to switch to -15 Vdc via OR Gates P/O U2. Control lines for FL1 and FL2 are then -15 Vdc, enabling FL1 and FL2. This places both USB and LSB filters in the circuit. The control line to R59 and R60 goes to +15 Vdc, which reverse biases CR5 and CR7, effectively steering FL1 (LSB) signals to Q5 (ISB output) and FL2 (USB) signals to Q6. Also, Q4 is selected via AR1-D which activates Q5 by applying +15 Vdc on Q5's drain.

Note that under normal LSB operation, the control line to R59 and R60 would be at -15 V. CR5 and CR7 would be forward biased and LSB signals would flow to Q6. All other operating modes except ISB would cause Q4 to turn Q5 off.

## 4. MAINTENANCE

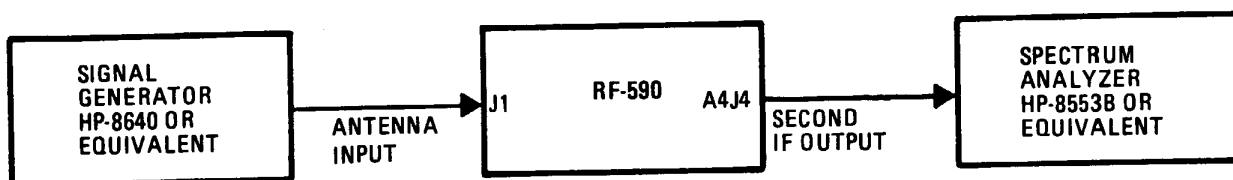
The following adjustment should not be performed as a routine maintenance procedure. It should be performed under the following two conditions:

- A failure indicating a definite problem
- Installation of new or different sideband filters. If the new filters have a loss which is different than the loss of the filters supplied with the RF-590, then R10 should be readjusted according to paragraph 4.1.

All tests are performed with all assembly connections in normal contact unless otherwise specified.

#### 4.1 Input/Output Amplifier Test/Adjustment

- a. Verify that the proper filters are installed in the A4 Assembly.
- b. Remove the ribbon cable connecting the AGC Assembly A5A2 to the IF/Audio Amp assembly A5A1.
- c. Set RF-590 controls as follows:  
  
Frequency: 10.000000 MHz  
  
Mode: USB  
  
AGC: OFF  
  
RF Gain: Fully clockwise (cw)
- d. Connect equipment as shown in figure 1.



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Figure 1. A4 I/O Amplifiers Test Setup

- e. Apply a -70 dBm, 10.0015 signal to J1, Antenna Input. Monitoring A4J4, adjust R10 for -44 dBm signal level.
- f. Monitor J2 (unfiltered IF output) with a spectrum analyzer. Signal level should be approximately -50 dBm.
- g. Place RF-590 to ISB mode of operation (if option is installed). Change signal generator frequency to 9.9985 MHz. Monitor A4J3 (ISB output) with spectrum analyzer. Signal level should be the same as step e.
- h. Disconnect test equipment and reconnect A4 to RF-590.

**4.2 Filter Selection Test**

- a. Selection of filters via the front panel consists of verifying that only the proper filter control line goes to -15 Vdc when the desired filter is selected. All other lines must stay at +15 Vdc (except in the case of ISB mode, where both control lines FL1 and FL2 go to -15 Vdc).
- b. Initiate RF-590 BITE test. The receiver must pass 04 testing.

**5. PARTS LIST**

Table 4 is a comprehensive parts list of all replaceable components in IF Filter Assembly A4. When ordering parts from the factory, include a full description of the part. Use figure 2, the IF Filter Assembly component location diagram to identify parts.

**6. SCHEMATIC DIAGRAMS**

Figure 3 is the IF Filter Assembly schematic diagram.

**Table 4. IF Filter Assembly A4 Parts List (PL 10073-5570)**

Ref. Desig.	Part Number	Description
AR1 - AR3	10073-5570	PWB, IF FILTER
C6	I30-0003-000	IC 324 OP AMP PLASTIC
C9	M39014/02-1320	CAP .47UF 10% 50V CER-R
C10	M39014/02-1320	CAP .47UF 10% 50V CER-R
C11	M39014/01-1535	CAP .01UF 20% 100V CER
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	M39014/02-1320	CAP .47UF 10% 50V CER-R
C14	CM04FC271J03	CAP 270PF 5% 300V MICA
C15	CM04FC271J03	CAP 270PF 5% 300V MICA
C16	M39014/02-1320	CAP .47UF 10% 50V CER-R
C17	M39014/01-1535	CAP .01UF 20% 100V CER
C18	M39014/01-1535	CAP .01UF 20% 100V CER
C19	CM04FC271J03	CAP 270PF 5% 300V MICA
C20	CM04FC271J03	CAP 270PF 5% 300V MICA
C21	M39014/02-1320	CAP .47UF 10% 50V CER-R
C22	M39014/01-1535	CAP .01UF 20% 100V CER
C23	M39014/01-1535	CAP .01UF 20% 100V CER
C24	CM04FD181J03	CAP 180PF 5% 500V MICA
C25	CM04FD181J03	CAP 180PF 5% 500V MICA
C26	M39014/02-1320	CAP .47UF 10% 50V CER-R
C27	M39014/01-1535	CAP .01UF 20% 100V CER
C28	M39014/01-1535	CAP .01UF 20% 100V CER
C29	CM04FD111J03	CAP 110PF 5% 500V MICA
C30	CM04FD111J03	CAP 110PF 5% 500V MICA
C31, C32	M39014/02-1320	CAP .47UF 10% 50V CER-R
C33	M39014/01-1535	CAP .01UF 20% 100V CER
	CM04FA361J03	CAP 360PF 5% 100V MICA

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Table 4. IF Filter Assembly A4 Parts List (PL 10073-5570) (Cont.)

Ref. Desig.	Part Number	Description
C34	CM04FA361J03	CAP 360PF 5% 100V MICA
C35	M39014/02-1320	CAP .47UF 10% 50V CER-R
C36	M39014/01-1535	CAP .01UF 20% 100V CER
C37	M39014/01-1535	CAP .01UF 20% 100V CER
C38	CM06FD751J03	CAP 750PF 5% 500V MICA
C39	CM06FD751J03	CAP 750PF 5% 500V MICA
C40	M39014/02-1320	CAP .47UF 10% 50V CER-R
C41	M39014/01-1535	CAP .01UF 20% 100V CER
C42	M39014/01-1535	CAP .01UF 20% 100V CER
C43	CM06FD122J03	CAP 1200PF 5% 500V MICA
C44	CM06FD122J03	CAP 1200PF 5% 500V MICA
C45	M39014/02-1320	CAP .47UF 10% 50V CER-R
C46	M39014/01-1535	CAP .01UF 20% 100V CER
C47	M39014/01-1535	CAP .01UF 20% 100V CER
C48	M39014/01-1535	CAP .01UF 20% 100V CER
C49	M39014/01-1535	CAP .01UF 20% 100V CER
C50	M39014/01-1535	CAP .01UF 20% 100V CER
C51	M39014/02-1310	CAP .1UF 10% 100V CER-R
C52	M39014/02-1310	CAP .1UF 10% 100V CER-R
C53	M39014/02-1310	CAP .1UF 10% 100V CER-R
C54	M39014/02-1310	CAP .1UF 10% 100V CER-R
C55	C26-0016-330	CAP 33UF 20% 16V TANT
C56	M39014/02-1320	CAP .47UF 10% 50V CER-R
C57	M39014/02-1320	CAP .47UF 10% 50V CER-R
C58	M39014/02-1320	CAP .47UF 10% 50V CER-R
C59	M39014/02-1320	CAP .47UF 10% 50V CER-R
C60	M39014/02-1320	CAP .47UF 10% 50V CER-R
C61	M39014/02-1320	CAP .47UF 10% 50V CER-R
C62	C26-0025-470	CAP 47UF 20% 25V TANT
C63	C26-0025-470	CAP 47UF 20% 25V TANT
CR1	1N4454	DIODE 200mA 75V SW
CR2	1N4454	DIODE 200mA 75V SW
CR3	1N4454	DIODE 200mA 75V SW
CR4	1N4454	DIODE 200mA 75V SW
CR5	1N4454	DIODE 200mA 75V SW
CR6	1N4454	DIODE 200mA 75V SW
CR7	1N4454	DIODE 200mA 75V SW
CR8	1N4454	DIODE 200mA 75V SW
CR9	1N4454	DIODE 200mA 75V SW
CR10	1N4454	DIODE 200mA 75V SW
CR11	1N4454	DIODE 200mA 75V SW
CR12	1N4454	DIODE 200mA 75V SW
CR13	1N4454	DIODE 200mA 75V SW
CR14	1N4454	DIODE 200mA 75V SW
CR15	1N4454	DIODE 200mA 75V SW

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**Table 4. IF Filter Assembly A4 Parts List (PL 10073-5570) (Cont.)**

Ref. Desig.	Part Number	Description
CR16	1N4454	DIODE 200mA 75V SW
CR17	1N4454	DIODE 200mA 75V SW
CR18	1N4454	DIODE 200mA 75V SW
CR19	1N4454	DIODE 200mA 75V SW
CR20	1N4454	DIODE 200mA 75V SW
CR21	1N4454	DIODE 200mA 75V SW
CR22	1N4454	DIODE 200mA 75V SW
CR23	1N4454	DIODE 200mA 75V SW
CR24	1N4454	DIODE 200mA 75V SW
CR25	1N4454	DIODE 200mA 75V SW
CR26	1N4454	DIODE 200mA 75V SW
CR27	1N4454	DIODE 200mA 75V SW
CR28	1N4454	DIODE 200mA 75V SW
CR29	1N4454	DIODE 200mA 75V SW
CR30	1N4454	DIODE 200mA 75V SW
CR31	1N4454	DIODE 200mA 75V SW
CR32	1N4454	DIODE 200mA 75V SW
CR33	1N4454	DIODE 200mA 75V SW
CR34	1N4454	DIODE 200mA 75V SW
CR35	1N4454	DIODE 200mA 75V SW
CR39	1N4454	DIODE 200mA 75V SW
FL1	10073-7301	FILTER,MECH,455 KHZ USB
FL2	10073-7300	FILTER,MECH 455 KHZ LSB
FL3	10073-7302	FILTER
FL4	10073-7303	FILTER
FL5	10073-7304	FILTER
FL6	10073-7305	FILTER
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J46-0032-010	HDR 10 PIN 0.100" SR
L4	MS75085-13	COIL 330UH 10% FXD RF
L5	MS75085-13	COIL 330UH 10% FXD RF
L6	10073-7033	INDUCTOR, 10MH
L7	10073-7033	INDUCTOR, 10MH
L8	MS75085-13	COIL 330UH 10% FXD RF
L9	MS75085-13	COIL 330UH 10% FXD RF
Q4	2N2222	XSTR 5S/GP NPN TO-18
Q5	Q35-0001-001	XSTR JFET J310
Q6	Q35-0001-001	XSTR JFET J310
R1	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R2	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R3	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R4	R65-0003-103	RES 10K 5% 1/4W CAR FILM

 **HARRIS**  
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**Table 4. IF Filter Assembly A4 Parts List (PL 10073-5570) (Cont.)**

Ref. Desig.	Part Number	Description
R5	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R6	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R7	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R8	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R10	R-2205	RES,VAR,PCB 500 .5 20%
R17	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R21	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R22	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R23	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R24	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R25	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R26	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R27	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R28	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R29	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R30	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R31	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R32	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R33	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R34	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R35	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R36	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R37	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R38	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R39	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R40	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R41	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R42	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R43	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R44	RNC55H5111FM	RES,5110 1% 0.1W MET FLM
R45	R65-0003-822	RES 8.2K 5% 1/4W CAR FILM
R46	R65-0003-822	RES 8.2K 5% 1/4W CAR FILM
R47	R65-0003-912	RES 9.1K 5% 1/4W CAR FILM
R48	R65-0003-101	RES 100 5% 1/4W CAR FILM
R49	R65-0003-101	RES 100 5% 1/4W CAR FILM
R50	R65-0003-101	RES 100 5% 1/4W CAR FILM
R51	R65-0003-101	RES 100 5% 1/4W CAR FILM
R52	R65-0003-101	RES 100 5% 1/4W CAR FILM
R53	R65-0003-101	RES 100 5% 1/4W CAR FILM
R54	R65-0003-101	RES 100 5% 1/4W CAR FILM
R55	R65-0003-101	RES 100 5% 1/4W CAR FILM
R56	R65-0003-101	RES 100 5% 1/4W CAR FILM
R57	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R58	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R59	R65-0003-333	RES 33K 5% 1/4W CAR FILM

 **HARRIS**  
**RF COMMUNICATIONS**

**Table 4. IF Filter Assembly A4 Parts List (PL 10073-5570) (Cont.)**

Ref. Desig.	Part Number	Description
R60	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R61	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R62	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R63	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R64	R65-0003-101	RES 100 5% 1/4W CAR FILM
R65	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R66	R65-0003-101	RES 100 5% 1/4W CAR FILM
R67	R65-0003-101	RES 100 5% 1/4W CAR FILM
R68	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R69	R65-0003-101	RES 100 5% 1/4W CAR FILM
R70	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R71	R65-0003-510	RES 51 5% 1/4W CAR FILM
R72	R65-0003-510	RES 51 5% 1/4W CAR FILM
R73	R65-0003-511	RES 510 5% 1/4W CAR FILM
R74	R65-0003-511	RES 510 5% 1/4W CAR FILM
R75	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R76	R65-0003-681	RES 680 5% 1/4W CAR FILM
R77	R65-0003-510	RES 51 5% 1/4W CAR FILM
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP6	J-0072	TP PWB BLU TOP ACCS .080"
TP7	J-0073	TP PWB VIO TOP ACCS .080"
TP8	J-0074	TP PWB GRA TOP ACCS .080"
U1	I01-0000-200	IC 4028B PLASTIC CMOS
U2	I01-0000-023	IC 4071B PLASTIC CMOS
U3	I50-0002-000	IC 733 VIDEO AMP PLASTIC
VR1	1N5231B	DIODE 5.1V 5% .5W ZENER



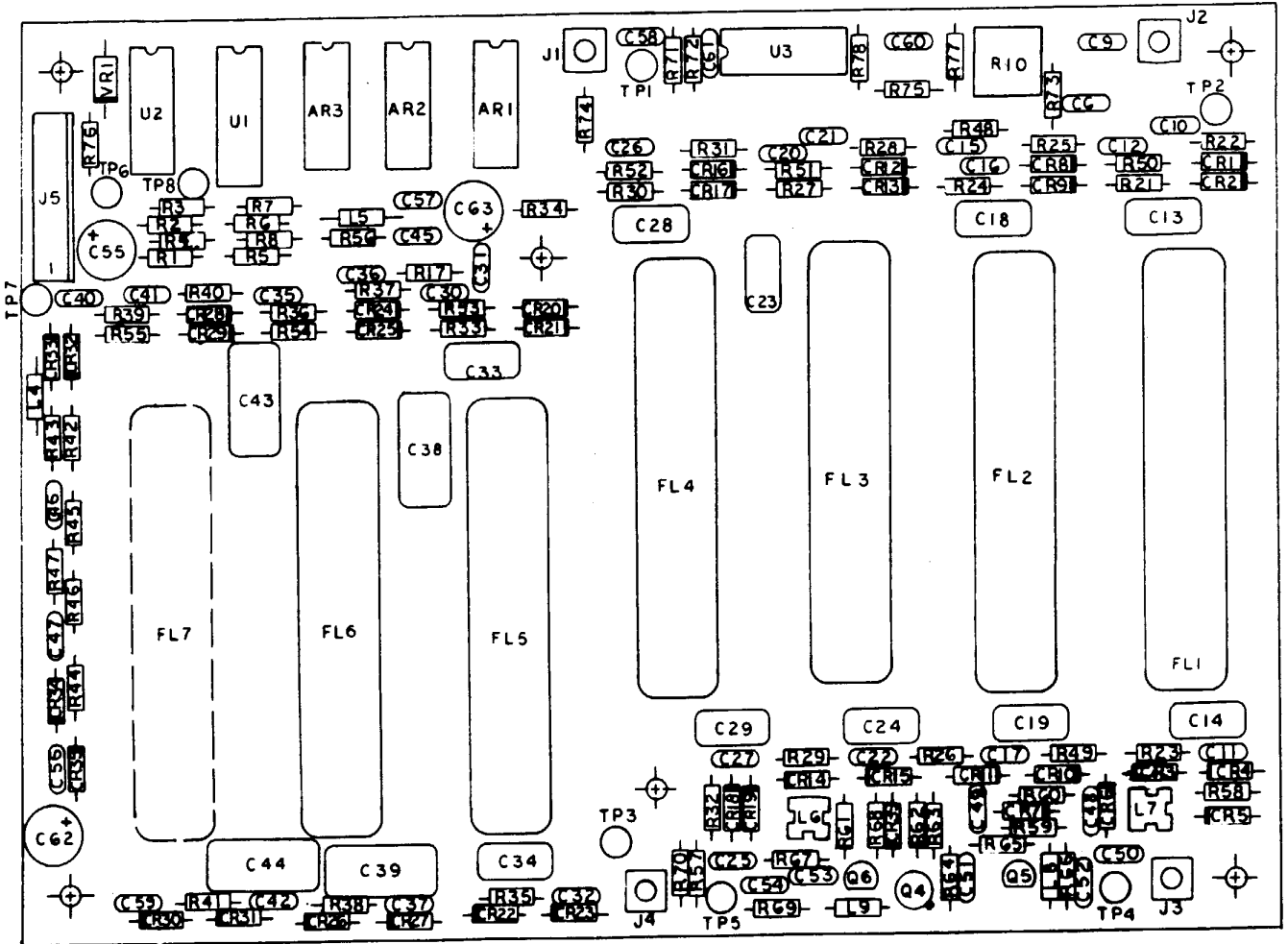


Figure 2. IF Filter Assembly A4 Component Location Diagram (10073-5570, Rev. D)

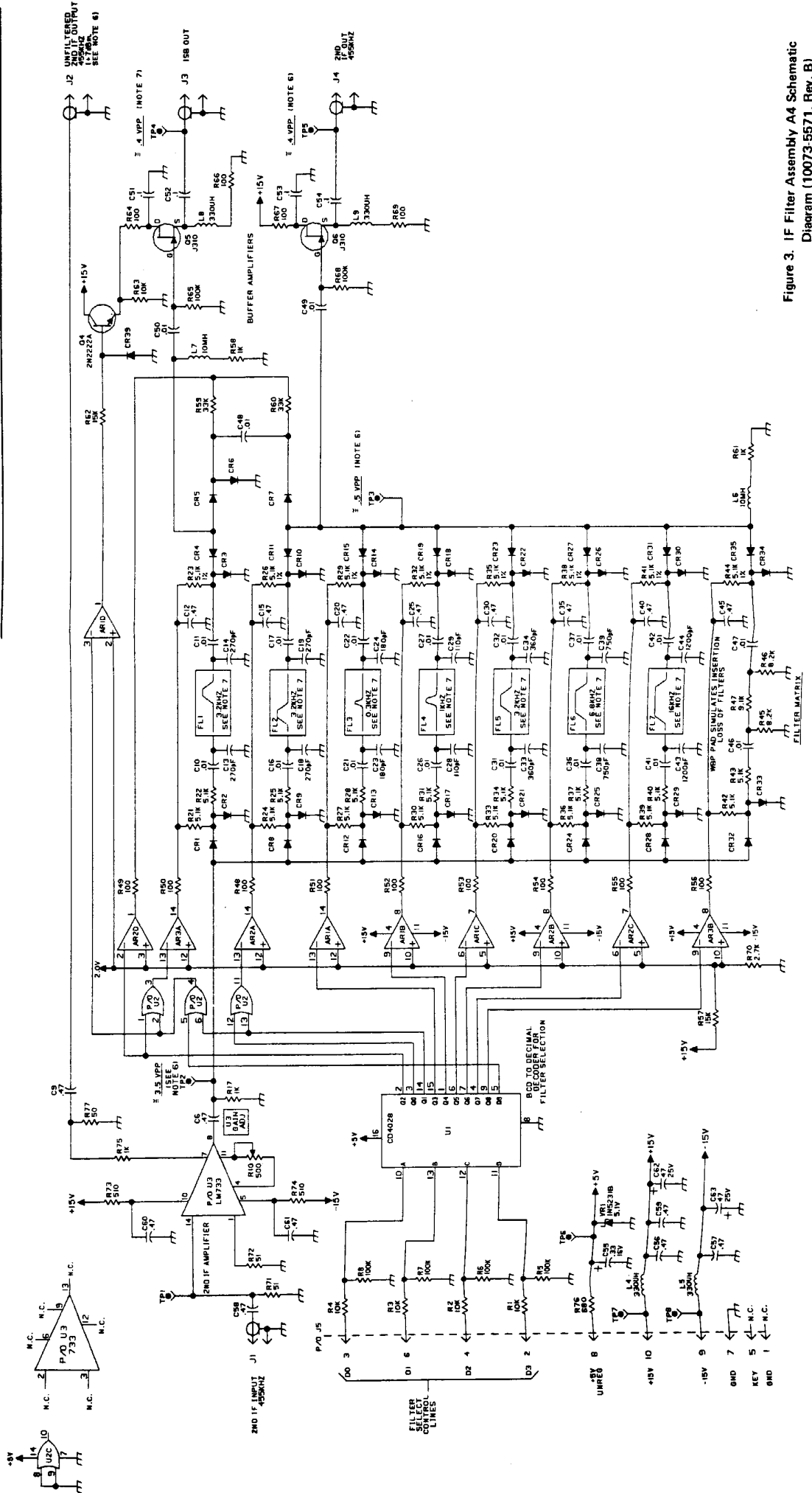
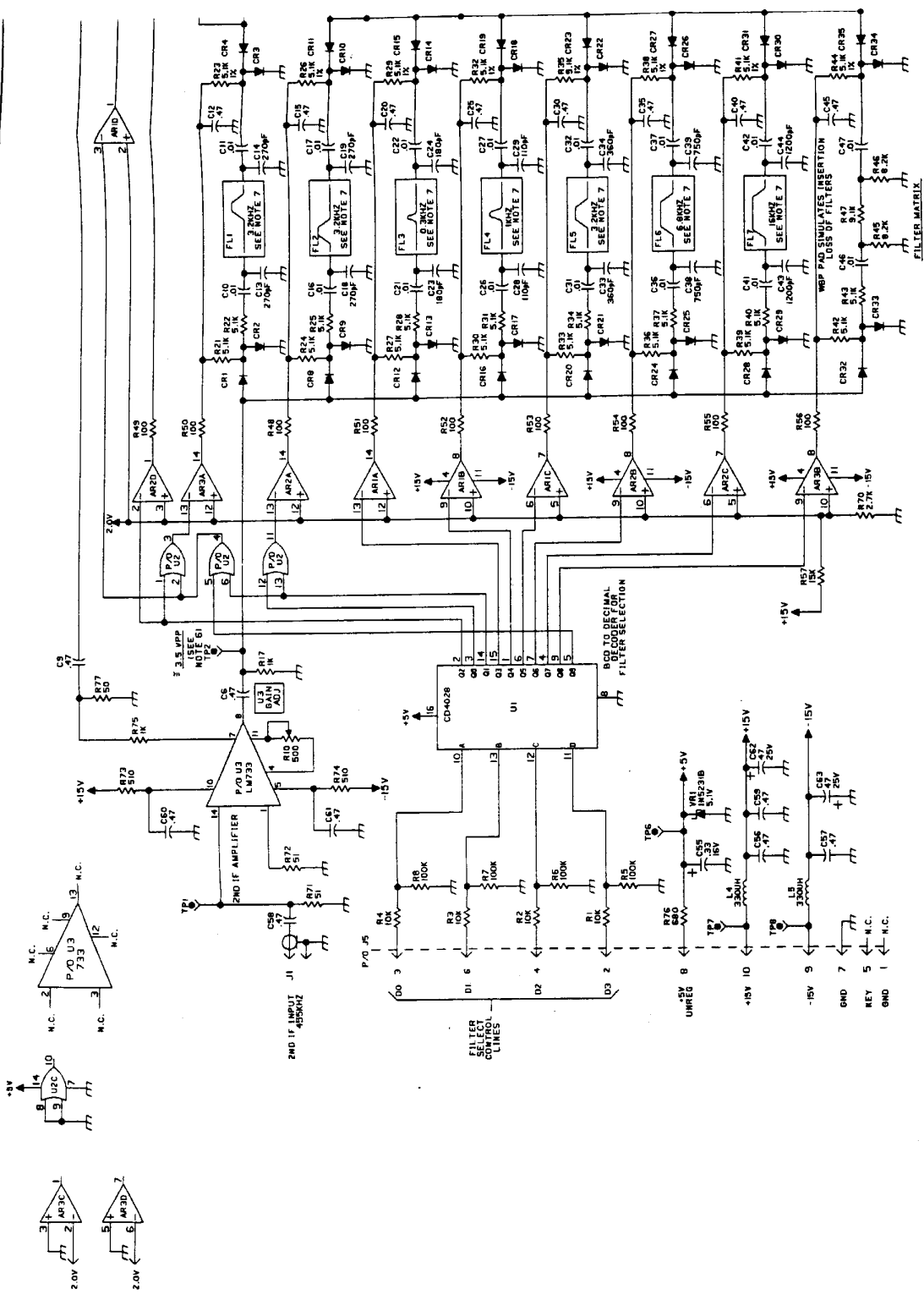


Figure 3. IF Filter Assembly A4 Schematic Diagram (10073-5571, Rev. B)



- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. ALL UNLABELED DIODES ARE DID 4454-000.
  5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  6. CURRENTS ARE IN MILLIAMPERES UNLESS OTHERWISE SPECIFIED.
  7. FILTERS FL1 THROUGH FL5 ARE AND TYPE. OPTIONAL AND MAY VARY IN USE AND TYPE.

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## 1. INTRODUCTION

IF/Audio Assembly A5 (10073-5400) consists of the following two PWBs:

- IF/Audio Motherboard A5A1 (10073-5410)
- AGC Board A5A2 (10073-5450)

## 2. A5A1 MOTHERBOARD ASSEMBLY – GENERAL DESCRIPTION

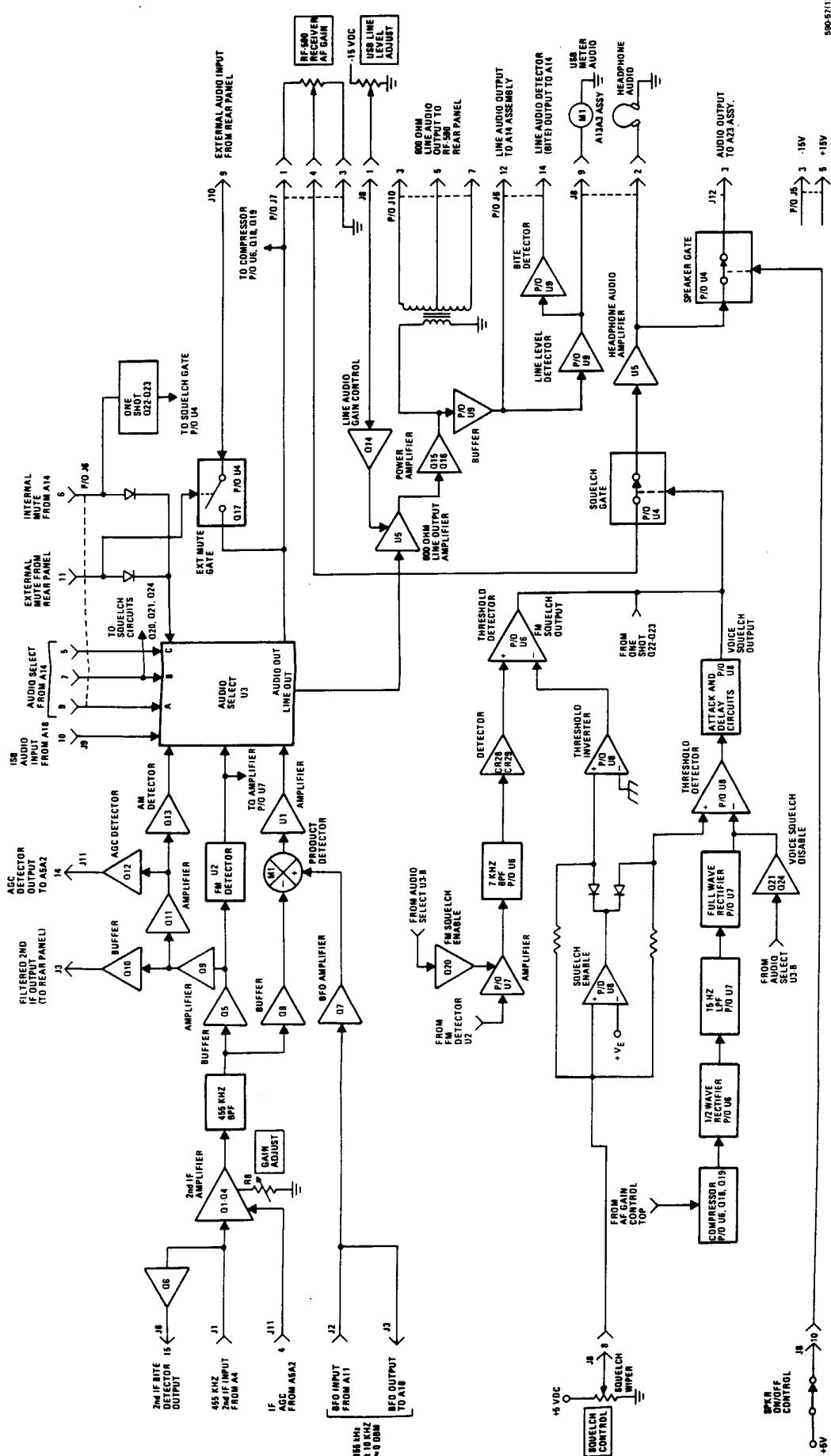
The A5A1 assembly provides most of the receiver gain utilizing a cascaded 455 kHz, second IF AGC controlled amplifier chain. The total gain range of this stage is 80 dB. This stage works in conjunction with amplifiers on the A2, A3, and A4 assemblies to provide a nominal -7 dBm output over an RF input level range of -120 to +10 dBm. Additionally, the assembly contains circuits for the following functions.

- a. Signal demodulation selection:
  - AM
  - FM
  - Product detection (for CW, USB, and LSB)
- b. Audio amplification and control, including the following audio outputs:
  - Headphone (+10 dBm/600 ohms)
  - Line (-16 dBm to +10 dBm, 600 ohms)
- c. Squelch control:
  - Voice operated (CW, AM, SB)
  - Carrier operated (FM)
- d. Signal monitoring:
  - Line level (via RF-590 front panel metering)
  - BITE detection (line audio level and second IF input level)

Table 1 details the various input/output connections and other relevant data.

**Table 1. A5A1 IF/Audio Assembly Interface Connections**

Connector	Function	Characteristics
J1	IF Input	455 kHz, -97/-5 dBm, 50 ohms
J2	BFO Input	455 kHz $\pm$ 10 kHz, 0 dBm, 50 ohms
J3	BFO Output	455 kHz $\pm$ 10 kHz, 0 dBm, 50 ohms
J4	Filtered IF Output	455 kHz, -7 dBm (under AGC control), 50 ohms
J5-1	Spare	
J5-2	Spare	
J5-3	Power	-15 Vdc, $\approx$ 50 mA
J5-4	Index Key	
J5-5	Power	+15 Vdc, $\approx$ 130 mA
J5-6	RF AGC	See A5A2
J6-1	Ground	
J6-2	RF Gain	See A5A2
J6-3	Special Data	See A5A2
J6-4	AGC Off	See A5A2
J6-5	Audio Select C	See table 2
J6-6	Internal Mute	+5 Vdc = Mute
J6-7	Audio Select B	see table 2
J6-8	AGC Fast	See A5A2
J6-9	Audio Select A	see table 2
J6-10	AGC Medium	see A5A2
J6-11	External Mute	+5 Vdc = Mute
J6-12	Line Audio Out	-16/+10 dBm, 600 ohms
J6-13	Line Audio Ground	
J6-14	Line Audio Det. BITE	
J6-15	BITE IF DET	
J6-16	AGC BITE	



98-5711

IF/Audio Motherboard Assembly A5A1  
Functional Block Diagram



Table 1. A5A1 IF/Audio Assembly Interface Connections (Cont.)

Connector	Function	Characteristics
J7-1	Volume Potentiometer - Top	
J7-2	Index Key	
J7-3	Volume Potentiometer - Ground	
J7-4	Volume Potentiometer - Wiper	
J8-1	USB Line Level Adj.	0 to -15 Vdc
J8-2	Headphones Audio	+10 dBm/600 ohms, maximum
J8-3	USB Meter - RF	See A5A2
J8-4	Spare	
J8-5	Spare	
J8-6	Spare	
J8-7	Index Key	
J8-8	Squelch Wiper	0 to +5 Vdc
J8-9	USB Meter Audio	
J8-10	Speaker on/off	+5 Vdc = speaker on
J9-1	Special Data	See A5A2
J9-2	Power, +15 V	See A5A2
J9-3	Power, -15 V	See A5A2
J9-4	Index Key	
J9-5	RF Gain	See A5A2
J9-6	AGC Off	See A5A2
J9-7	AGC Fast	See A5A2
J9-8	AGC Med	See A5A2
J9-9	ISB AGC	See A5A2
J9-10	ISB Audio In	See A5A2

Table 1. A5A1 IF/Audio Assembly Interface Connections (Cont.)

Connector	Function	Characteristics
J10-1	AGC Out	See A5A2
J10-2	Comb. AGC Out	See A5A2
J10-3	600 ohm Line Audio	-16/+10 dBm
J10-4	AGC In	See A5A2
J10-5	600 ohm Line Audio	Center Tap
J10-6	AGC Dump	See A5A2
J10-7	600 ohm Line Audio	-16/+10 dBm
J10-8	Ground	
J10-9	External Audio In	Typically 50 mVrms
J10-10	Spare	
J11-1	ISB AGC	See A5A2
J11-2	AGC Med	See A5A2
J11-3	AGC BITE	See A5A2
J11-4	IF AGC In	0 to -3 Vdc
J11-5	Spare	
J11-6	AGC Fast	See A5A2
J11-7	Special Data	See A5A2
J11-8	AGC Off	See A5A2
J11-9	Spare	
J11-10	Spare	
J11-11	Power, +15 V	
J11-12	RF Gain	
J11-13	USB Meter RF	See A5A2
J11-14	AGC Det. Out	Typically -1 Vdc

Table 1. A5A1 IF/Audio Assembly Interface Connections (Cont.)

Connector	Function	Characteristics
J11-15	RF AGC	See A5A2
J11-16	AGC Dump	See A5A2
J11-17	Spare	
J11-18	AGC In	See A5A2
J11-19	AGC Out	See A5A2
J11-20	Comb AGC	See A5A2
J12-1	Index Key	
J12-2	Audio Ground	
J12-3	Audio Output	

### 3. A5A1 CIRCUIT DESCRIPTIONS

#### 3.1 455 kHz Second IF Amplifier Chain

Low level signals at 455 kHz from IF Filter Assembly A4 enter the A5A1 assembly at coax connector J1. At this point, it goes to both the input of the IF amplifier and the input BITE detector. The BITE detector consists of Q6 and its associated components. Q6 is an amplifier with 26 dB of gain that feeds a diode detector consisting of CR4, CR5, R32, and C27. CR6 is a 4.7 volt Zener diode that protects the BITE circuitry against overvoltage. This detector serves to check the output of the IF Filter board and the input to the IF/AF board.

Q1 is a grounded gate FET amplifier that is the input stage to the IF strip amplifier, and has approximately 20 dB of gain. Q2, Q3, and Q4 are common emitter amplifiers with an overall gain of 46 dB  $\pm$  6 dB. This 12 dB gain adjustment is available at R8, and allows the user to trim the overall gain of the IF strip to its desired value.

Receiver Automatic Gain Control (AGC) of the IF strip is accomplished through the use of PIN diodes CR1, CR2, and CR3. A negative voltage applied to the IF AGC IN line, J11-4, forward biases the PIN diodes and decreases the gain of the IF strip by decreasing the load impedance of each stage. Normal receiver operation requires 80 dB of available gain reduction in the strip, which is accomplished with approximately -3.0 volts on the IF AGC line.

L3, L4, C17, C18, and C19 form a bandpass filter which is adjusted during alignment to be centered at 455 kHz. This filter has approximately 9 dB of insertion loss for an overall gain to TP1 of 56 dB. The output of this filter drives Q5, (an emitter follower that buffers the rest of the IF strip) and Q8 (a dual gate MOSFET that is the input to the product detector).

Q5 serves as a buffer to provide inputs to U12 (FM demodulator) and Q9 (IF output gain stage). Q9 is a common emitter amplifier that has 30 dB of gain to provide the high level IF output, and drive amplifier Q11. Q10 is an emitter follower that buffers the high level IF output, nominally -7 dBm. Resistor R60 serves to set the IF output impedance at 50 ohms to J4. This output is then routed to rear panel connector J4 and is referred to as the filtered IF output. Overall IF strip gain to the IF output is nominally 80 dB. Q11 is a common emitter amplifier with 11 dB of gain that drives Q12 (the AGC detector) and Q13 (AM detector).

### 3.2 Demodulator Circuits

The A5A1 assembly contains four detector circuits whose inputs are derived from the 455 kHz IF chain. The AM, FM, and product detectors all feed audio select circuit U3. The AGC detector output is routed to AGC Assembly A5A2, where it is used as part of the feedback loop that controls the gain characteristics of the receiver.

#### 3.2.1 AM and AGC Detectors

Q12 and Q13 serve as the AGC detector and AM detector, respectively. Both of these detectors are temperature compensated and provide envelope detection to their respective outputs. The output of the AM detector is ac coupled and attenuated by R85, C65, and R86. The AGC detector output is dc coupled and goes to the A5A2 AGC PWB by way of J11-14.

#### 3.2.2 Product Detector

Sideband signals are demodulated using a mixer as a product detector. The 455 kHz input to the mixer RF port is buffered through dual gate MOSFET Q8. LO input is 455 kHz,  $\pm 10$  kHz, 0 dBm, and is supplied by BFO Assembly A11 at J2. Q7 provides 10 dB of gain to 50 ohm matching network R39, R40, R41, which in turn provides 7 dBm of LO drive to M1. LO leakage back into the IF chain is prevented by the 40 dB LO to RF isolation of M1 as well as the high reverse isolation of buffer Q8. Sideband inversion occurs in the mixing process. This produces an audio signal whose bandwidth is determined by the particular A4 filter selected, but may be translated in frequency by  $\pm 10$  kHz. Typical audio output level of 2.5 mVrms at the M1 IF port is boosted to approximately 150 mV4ms by amplifier U1.

#### 3.2.3 FM Detector

FM demodulation is accomplished by quadrature detector U2. IF input from Q5 is fed to pin 4, and maximum recovered audio occurs at pin 1 when tuned circuit L7-C55 is peaked for resonance at 455 kHz, the second IF center frequency.

### 3.3 Audio Selection

U3 is a CMOS analog switch that provides audio selection and muting functions. The IC is configured as three SPDT switches. In the receiver, these switches are connected in series to allow selection between the three demodulator outputs along with the audio output of the ISB board. Actual signal selection is con-

trolled by the receiver microprocessor on Control Board Assembly A14. Table 2 lists the control logic required at the audio select inputs (pins 9, 10, and 11) which allow the desired demodulator output to pass to the audio select outputs (pins 5, 15, and 4).

**Table 2. Audio Select Data**

Function Selected	Input Lines		
	A	B	C
AM	0	0	0
ISB	1	0	1
FM	0	1	0
SB (Product Detector)	1	0	0

+5 Vdc = 1  
0 Vdc = 0

There is also an inhibit input that allows complete muting of the inputs. This function is controlled by the internal mute and external mute lines at U3, pin 6. A logic 1 causes muting. The CD4053 IC has a limited supply voltage range. To provide true bipolar signal operation, it was provided with regulated  $\pm 5$  volt supplies (VR1, VR2). This also makes the logic levels compatible with the TTL control logic from the receiver control processor.

### 3.4 Audio Output Circuitry

There are two different audio paths in the receiver, both derived from different switched outputs of audio select U3. U3 pins, 5 and 15, provide audio for the 600 ohm line audio output, while U3, pin 4, provides audio for the speaker and headphone outputs.

#### 3.4.1 600 Ohm Line Audio

The 600 ohm line audio output at J10 (pins 3, 5, and 7) is driving long lines. This output is the secondary of transformer T2 and along with the center tap it is available at both the rear panel terminal strip TB1 and D connector J7.

The input to the 600 ohm line out amplifier is from the audio selection IC, U3 (pins 5 and 15). Any of the three demodulators (AM, FM, and Product Detector) is capable of being output. The gain of the output amplifier is adjusted by a 20 turn trim potentiometer at the front panel meter. The output level in dBm 600 ohms may be read from the meter to ease adjustment.

The output amplifier is a FET input, low noise, wideband op amp (U5A) with a complementary current buffer Q15 and Q16. Gain control is accomplished by varying the gate bias on FET Q14. Q14 is configured as a voltage variable resistor and acts as the shunt leg in the amplifier feedback network. Total gain control range is 30 dB from -20 dBm to +10 dBm. The two endpoints can be set independently. The minimum gain is controlled by resistor R90 which is in parallel with Q14. The maximum gain is set by the minimum on resistance of Q14.

The current buffer output stage of this amplifier is formed by Q15 and Q16, a class AB complementary amplifier. The 600 ohm output impedance is set by resistor R96 whose 180 ohm value is transformed to 600 ohms by the 1.82:1 ratio of T2.

The line level is monitored at the top of R96, and a buffered single ended line output to the processor is available at J6-12. The output of this buffer (U9A) also drives the precision half-wave detector (U9C) that provides the USB AF meter and line audio detector BITE outputs. This circuit is a precision wideband, temperature compensated detector that provides meter drive through R101. The value of R101 is chosen so that the meter reads calibrated line output level in dBm 600 ohms. R169 provides a discharge path for C68 when the meter is not in circuit. There is also a buffered version of the peak detector output available for the line audio detector BITE line to the processor. A 4.7 volt Zener diode (CR17) provides overvoltage protection for the BITE circuitry.

### 3.4.2 Speaker and Headphone Audio

The second audio signal path in the receiver involves the local audio. It consists of the front panel, external speaker, and the headphones. The local audio output of audio select IC, U3 (pin 4) provides the signal input for the top of the volume potentiometer and the squelch circuitry. This point is also where the external audio is injected during an external mute. An external mute signal at U3, pin 6, inhibits the audio select chip and closes an analog switch that is connected to the external audio input.

The signal connection to the front panel volume potentiometer is through a shielded cable to protect the low level signal from external interference. The wiper of the volume potentiometer is returned to the A5A1 assembly through this same cable and is routed to an analog switch (U4B) that functions as a squelch gate. This gate is paralleled with resistor R107 that sets the depth of squelch by forming an attenuator with R110. Depth of squelch is 25 dB.

The output of the squelch gate is fed into the input of U5B, a low noise, wideband op amp that serves as the headphone amplifier. This stage has 50 dB of gain and is ac coupled into the headphone output. A series resistor R113 sets the 600 ohm output impedance. The output of this amplifier is also attenuated through R111 and R112 and fed into an analog gate (U4C) that provides a speaker on/off function. The output of this gate is then routed through J12, pin 3, to the speaker audio amplifier located on Audio Assembly A23.

### 3.5 Squelch Circuitry

The receiver has two separate mutually exclusive squelch circuits. The first is a noise squelch that operates only when the FM mode is chosen. The other type is a syllabic rate voice squelch which operates in all

other modes of operation. Both types use the variable squelch signal provided by the front panel Squelch control to establish a squelch threshold. Both control the squelch gate analog switch, (U4B), which mutes audio to headphone audio and speaker audio amplifier circuits. Note that the 600 ohm line audio is not squelch controlled, and that squelch action may also be accomplished at the squelch gate by signals provided automatically during receiver self-test (BITE).

### 3.5.1 Squelch Enabling

Two enabling schemes are used to allow the squelch circuits to function. The first selectively activates either the FM noise squelch or the voice squelch, but not both. The second allows the actual variable threshold signal from the front panel Squelch control to reach the squelch circuits.

#### 3.5.1.1 Squelch Selection

The logic signal from the B input of audio select circuit U3 is a logic 1 (5 volts) only when the FM mode is chosen. This signal may be used to selectively activate FM squelch/deactivate voice squelch, or vice versa.

FM squelch selection occurs when U3, pin 10, is a logic 1. This turns Q20 on, providing a low impedance to ground for R144. This allows the audio at U7, pin 12 (derived from FM detector U2) to pass through amplifier U7 and be processed by the rest of the FM squelch circuitry. Simultaneously, the same logic signal from U3 turns Q21 and then Q24 on. This shorts out the voice squelch signal (derived from audio supplied by the other detectors) at U8, pin 6. This action disables the voice squelch.

Voice squelch selection occurs when U3, pin 10, is a logic 0. Q21 and Q24 turn off, and the voice squelch derived signal at U8, pin 6, is no longer shorted out. Simultaneously, Q20 turns off removing the ground return at R144, and FM squelch derived signals are prevented from passing through U7.

#### 3.5.1.2 Squelch Threshold Enabling

A variable dc voltage provided by the front panel Squelch control wiper arm functions as the squelch threshold signal to both squelch circuits. This level must first exceed the potential  $V_e$  at U8 (pin 2, 27 mV) before it is applied to the squelch circuits. This action is the electronic equivalent of a hardwired mechanical switch that would provide a squelch off function. This causes no squelching action to occur for the first few degrees of the squelch control rotation.

Once  $V_e$  is exceeded, U8, pin 1, switches from -15 Vdc to +15 Vdc, reverse biases CR31 and CR34, and allows the squelch control wiper voltage to feed through R153 (to the FM squelch circuits) and R156 (to the voice squelch circuits). When the threshold is below  $V_e$ , U8 (pin 1) is at -15 Vdc. This forward biases the diodes and shorts out the squelch threshold inputs to the two squelch circuits. Note that despite this threshold value being applied to both squelch circuits simultaneously, only the squelch circuit enabled at the time will process it to cause squelch gating.

### 3.5.2 Voice Squelch Operation

The voice squelch in the receiver operates on the principle that the human voice has characteristic modulation in the 5 Hz to 15 Hz range.

The local audio is tapped off at the top of the volume potentiometer and run into a compressor comprising U6A, Q18, and Q19. The action of the compressor enables the squelch to operate on low level signals below the AGC threshold of the receiver. It also cancels any difference there may be in the level of recovered audio between the various detectors in the signal path.

The output of the compressor is fed into a precision temperature compensated, half-wave detector, U6B. This detector contains a limiting circuit that reduces its slew rate, and correspondingly reduces its ability to reproduce transient peaks greater than the nominal level of the highest frequency of interest. The output of this detector is run into a 15 Hz low pass filter (U7B) to separate out the syllabic rate component of the signal envelope. The output of the low pass filter is ac coupled to provide some highpass characteristic and reject frequencies below 5 Hz. The ac coupled low pass output is then fed into a precision temperature compensated, full-wave rectifier/integrator (U7C). The output of this detector is integrated to provide a desirable transient response, and offer additional rejection of higher frequency information. This integrated output is then compared against the variable threshold from the squelch control at U8C, pins 5 and 6. The output of this comparator charges and discharges an RC network that controls the squelch open and close timing.

The time constants chosen (determined by R140, R141, and C82) will cause U8, pin 14, to switch within 50m seconds of detected voice. This applies +15 Vdc at squelch gate U4, pin 9, which allows audio at pin 11 to pass through the gate headphone amplifier U5B. Similarly, the time constants will allow U8, pin 14, to remain at +15 Vdc for three seconds after voice activity stops. This allows the squelch gate to stay open, and allows normal interruptions of the human speech pattern to occur without annoying squelching activity between words, sentences, etc.

### 3.5.3 FM Squelch Operation

When the receiver is set to FM mode the voice squelch is disabled, and the FM noise squelch enabled. The input to the FM squelch is the attenuated output of the FM detector U2. This input goes into an amplifier (U7, pin 12) that also provides the enable function (at pin 13). After being amplified, the FM audio is fed into a bandpass filter (U6C) that is centered at 7 kHz. This filter was designed to reject signal information while amplifying any accompanying noise. The noise output of this filter is then detected by CR28 and CR29 and compared against the variable threshold at U6 pins 9 and 10 to make the squelch decision. Once the detected squelch signal exceeds the squelch threshold, U6, pin 8, swings to +15 Vdc and closes the squelch gate at U4, pin 9. Audio will now pass through to succeeding audio stages.

The threshold that the detected noise level is compared against is not the same threshold that the voice squelch uses, although it is generated from the same control. The operation of the two squelches is opposite in the sense that the voice squelch operates from the increasing presence of a signal (voice), and the FM squelch operates from the decreasing presence of a signal (as the signal strength increases, the



signal to noise ratio increases and the detected noise level will decrease). Both of these thresholds must operate from the same control potentiometer with a logical increase in squelch threshold with CW rotation. This necessitates inverting the sense and offsetting the level of the FM squelch threshold voltage. It is this altered threshold that is used to open and close the squelch gate in FM squelch.

### 3.5.4 Miscellaneous Squelch Circuits

There is one additional circuit on the A5A1 board that is capable of squelching the audio. A discrete one shot with a duration of approximately 500 mseconds is triggered off the falling edge of the internal mute line. This serves to mute the receiver audio during the BITE sequence so that the operator does not hear the various signals that are injected into the signal path by the processor controlled BITE operation. This one shot consists of Q22 and Q23 and their associated components.

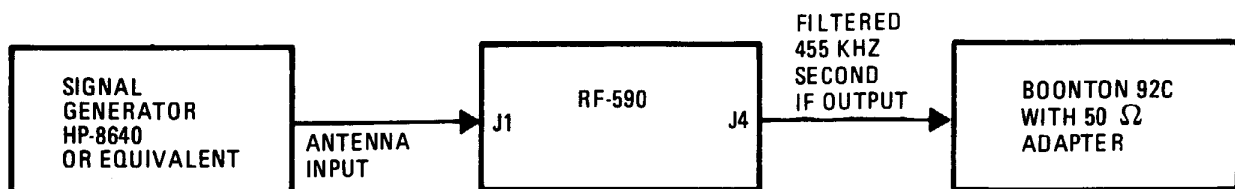
## 4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests are performed with all assembly connections in normal contact, unless otherwise specified.

### 4.1 Second IF Chain Alignment

Perform the following procedure to align the second IF chain.

- a. Disconnect the ribbon cable connecting the AGC Assembly A5A2 to the IF/Audio Assembly A5A1 at A5A1J11.
- b. Connect equipment as shown in figure 1.



590-81(B)

Figure 1. Second IF Chain Alignment

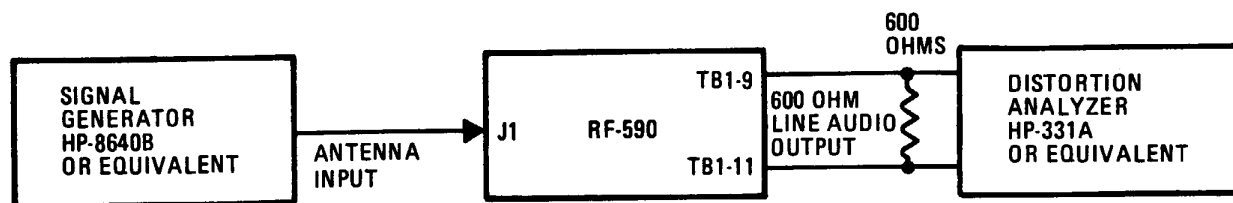
- c. Set RF-590 controls as follows:
  - Frequency to 10.000000 MHz.
  - Mode to USB
  - USB meter button to USB/RF
  - AGC to OFF
  - RF Gain to fully clockwise (cw)

- d. Set signal generator to 10.0015 MHz, -70 dBm RF output.
- e. Disconnect the coax from A4J4 on the IF/Filter Assembly A4. Connect the RF millivoltmeter, with 50 ohm adapter, to A4J4 and verify that the level is -44 dBm. (If the level at A4J4 is not -44 dBm, alignment is required ahead of IF/Audio Assembly A5.) Disconnect RF millivoltmeter and reconnect coax to A4J4.
- f. Connect RF millivoltmeter with 50 ohm adapter to RF-590 rear panel connector J4, Filtered IF output.
- g. Set signal generator RF output to 0.5 uVrms.
- h. Monitoring the Boonton 92C, adjust A5A1L3 and A5A1L4 for maximum output indication on an RF millivoltmeter. (Adjustments may be some what interactive, so repeat as necessary.)
- i. Adjust A5A1R8 for -7 dBm (100 mVrms) output indication on the RF millivoltmeter.
- j. Turn RF-590 power off. Reconnect ribbon cable to A5A1. Test is complete.

#### 4.2 FM Detector Alignment

Perform the following procedure to align the FM detector.

- a. Connect equipment as shown in figure 2. Set signal generator to 10.000000 MHz, 10 uV, 4.7 kHz FM deviation, and 1 kHz modulation.



590-82(A)

Figure 2. FM Detector Alignment

- b. Set RF-590 controls as follows:
  - Frequency to 10.000000 MHz
  - Mode to FM
  - AGC to MEDIUM
  - RF Gain to fully clockwise (cw)
  - Meter to USB Audio
- c. Adjust L7 for maximum audio output at TB1. (More than one setting may produce a peaked response choose the setting which gives the most response.)

The audio output level should be 0 dBm,  $\pm 4$  dB. (This assumes that the USB audio control located to the left of the meter had been previously set to 0 dBm for USB operation).

- d. Activate receiver BITE self-test. Receiver must pass all tests associated with the A5A1 assembly. Test is complete.

**5. PARTS LIST**

Table 3 is a comprehensive parts list of all replaceable components in IF/Audio Motherboard Assembly A5A1. When ordering parts from the factory, include a full description of the part. Use figure 3, IF/Audio Motherboard Assembly A5A1 Component Location Diagram to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 4 is the IF/Audio Motherboard A5A1 schematic diagram.

**Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410)**

Ref. Desig.	Part Number	Description
	10073-5410	PWB ASSEMBLY
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2 - C4	M39014/02-1320	CAP .47UF 10% 50V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6 - C8	M39014/02-1320	CAP .47UF 10% 50V CER-R
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1320	CAP .47UF 10% 50V CER-R
C11	M39014/02-1320	CAP .47UF 10% 50V CER-R
C12	C26-0025-220	CAP 22UF 20% 25V TANT
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1320	CAP .47UF 10% 50V CER-R
C15	M39014/02-1320	CAP .47UF 10% 50V CER-R
C16	CM04FD181J03	CAP 180PF 5% 500V MICA
C17	CM06FD112J03	CAP 1100PF 5% 500V MICA
C18	CM04ED680J03	CAP 68PF 5% 500V MICA
C19	CM06FD122J03	CAP 1200PF 5% 500V MICA
C20	M39014/02-1310	CAP .1UF 10% 100V CER-R
C21	M39014/02-1320	CAP .47UF 10% 50V CER-R
C22	M39014/02-1320	CAP .47UF 10% 50V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1320	CAP .47UF 10% 50V CER-R
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	M39014/02-1320	CAP .47UF 10% 50V CER-R
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	M39014/02-1320	CAP .47UF 10% 50V CER-R
C33	CK05BX102M	CAP 1000PF 20% 200V CER

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Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410) (Cont.)

Ref. Desig.	Part Number	Description
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	M39014/02-1320	CAP .47UF 10% 50V CER-R
C36	CK05BX102M	CAP 1000PF 20% 200V CER
C37	M39014/02-1320	CAP .47UF 10% 50V CER-R
C38	M39014/02-1320	CAP .47UF 10% 50V CER-R
C39	M39014/02-1320	CAP .47UF 10% 50V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/02-1320	CAP .47UF 10% 50V CER-R
C42	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	C26-0025-339	CAP 3.3UF 20% 25V TANT
C45	CK05BX472M	CAP 4700PF 20% 100V CER
C46	M39014/02-1310	CAP .1UF 10% 100V CER-R
C47	M39014/02-1320	CAP .47UF 10% 50V CER-R
C48	M39014/02-1310	CAP .1UF 10% 100V CER-R
C49	M39014/02-1310	CAP .1UF 10% 100V CER-R
C50	M39014/02-1310	CAP .1UF 10% 100V CER-R
C51	C26-0025-339	CAP 3.3UF 20% 25V TANT
C52	CK05BX102M	CAP 1000PF 20% 200V CER
C53	C26-0025-339	CAP 3.3UF 20% 25V TANT
C54	M39014/02-1310	CAP .1UF 10% 100V CER-R
C55	CM06FD362J03	CAP 3600PF 5% 500V MICA
C56	CM04ED750J03	CAP 75PF 5% 500V MICA
C57	M39014/02-1320	CAP .47UF 10% 50V CER-R
C58	C26-0025-339	CAP 3.3UF 20% 25V TANT
C59	M39014/02-1310	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310	CAP .1UF 10% 100V CER-R
C61	M39014/02-1310	CAP .1UF 10% 100V CER-R
C62	M39014/02-1310	CAP .1UF 10% 100V CER-R
C63	C26-0025-339	CAP 3.3UF 20% 25V TANT
C64	M39014/01-1535	CAP .01UF 20% 100V CER
C65	C26-0025-339	CAP 3.3UF 20% 25V TANT
C66	CK05BX332M	CAP 3300PF 20% 100V CER
C67	C26-0025-339	CAP 3.3UF 20% 25V TANT
C68	C26-0025-339	CAP 3.3UF 20% 25V TANT
C69	M39014/02-1320	CAP .47UF 10% 50V CER-R
C70	M39014/02-1320	CAP .47UF 10% 50V CER-R
C71	C26-0025-339	CAP 3.3UF 20% 25V TANT
C72	C26-0035-100	CAP 10UF 20% 35V TANT
C73	C26-0025-339	CAP 3.3UF 20% 25V TANT
C74	M39014/02-1310	CAP .1UF 10% 100V CER-R
C75	M39014/02-1302	CAP .022UF 20% 100V CER
C76	M39014/02-1320	CAP .47UF 10% 50V CER-R
C77	C26-0025-339	CAP 3.3UF 20% 25V TANT
C79	M39014/02-1316	CAP .22UF 20% 50V CER

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Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410) (Cont.)

Ref. Desig.	Part Number	Description
C80	M39014/02-1316	CAP .22UF 20% 50V CER
C81	C26-0025-479	CAP 4.7UF 20% 25V TANT
C82	C26-0035-100	CAP 10UF 20% 35V TANT
C83	M39014/02-1310	CAP .1UF 10% 100V CER-R
C84	CK05BX821K	CAP 820PF 10% 200V CER
C85	CK05BX821K	CAP 820PF 10% 200V CER
C86	M39014/02-1310	CAP .1UF 10% 100V CER-R
C87	C26-0025-339	CAP 3.3UF 20% 25V TANT
C88	M39014/02-1320	CAP .47UF 10% 50V CER-R
C89	C26-0025-339	CAP 3.3UF 20% 25V TANT
C90	C26-0035-159	CAP 1.5UF 20% 35V TANT
C91	C26-0025-470	CAP 47UF 20% 25V TANT
C92	C26-0025-470	CAP 47UF 20% 25V TANT
C93	M39014/02-1310	CAP .1UF 10% 100V CER-R
C94	CK05BX221M	CAP 220PF 20% 200V CER
C95	M39014/02-1320	CAP .47UF 10% 50V CER-R
C96	M39014/02-1310	CAP .1UF 10% 100V CER-R
C97	M39014/02-1320	CAP .47UF 10% 50V CER-R
C98	M39014/02-1310	CAP .1UF 10% 100V CER-R
CR1	10073-5412	DIODE PIN
CR2	10073-5412	DIODE PIN
CR3	10073-5412	DIODE PIN
CR4	1N4454	DIODE 200mA 75V SW
CR5	1N4454	DIODE 200mA 75V SW
CR6	1N4732	DIODE 4.7V 10% 1W ZENER
CR7	1N4454	DIODE 200mA 75V SW
CR8	1N4454	DIODE 200mA 75V SW
CR9	1N4454	DIODE 200mA 75V SW
CR10	1N4454	DIODE 200mA 75V SW
CR11	1N4454	DIODE 200mA 75V SW
CR12	1N4454	DIODE 200mA 75V SW
CR13	1N4454	DIODE 200mA 75V SW
CR14	1N4454	DIODE 200mA 75V SW
CR15	1N4454	DIODE 200mA 75V SW
CR16	1N4454	DIODE 200mA 75V SW
CR17	1N4732	DIODE 4.7V 10% 1W ZENER
CR18	1N4454	DIODE 200mA 75V SW
CR19	1N4454	DIODE 200mA 75V SW
CR21	1N4454	DIODE 200mA 75V SW
CR22	1N4454	DIODE 200mA 75V SW
CR23	1N4454	DIODE 200mA 75V SW
CR24	1N4454	DIODE 200mA 75V SW
CR25	1N4454	DIODE 200mA 75V SW
CR26	1N4454	DIODE 200mA 75V SW
CR27	1N4454	DIODE 200mA 75V SW

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Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410) (Cont.)

Ref. Desig.	Part Number	Description
CR28	1N4454	DIODE 200mA 75V SW
CR29	1N4454	DIODE 200mA 75V SW
CR30	1N4454	DIODE 200mA 75V SW
CR31	1N4454	DIODE 200mA 75V SW
CR32	1N4454	DIODE 200mA 75V SW
CR33	1N4454	DIODE 200mA 75V SW
CR34	1N4454	DIODE 200mA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J90-0014-001	CONN SMB VERT PCB MT M
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J46-0022-006	HDR 6 PIN 0.100" SR LKG
J6	J46-0013-016	HDR 16 PIN 0.100" DR SHRD
J7	J46-0022-004	HDR 4 PIN 0.100" SR LKG
J8	J46-0032-010	HDR 10 PIN 0.100" SR
J9	J46-0032-010	HDR 10 PIN 0.100" SR
J10	J-0870	CONN, 10 PIN
J11	J46-0013-020	HDR 20 PIN 0.100" DR SHRD
J12	J46-0022-003	HDR 3 PIN 0.100" SR LKG
JMP1	MP-1142	CIRCUIT JUMPER
L1	MS75085-19	COIL 1000UH 10% FXD RF
L2	MS75085-19	COIL 1000UH 10% FXD RF
L3	L11-0004-037	INDUCT SH VAR 90.0-110 UH
L4	L11-0004-037	INDUCT SH VAR 90.0-110 UH
L5	MS75085-19	COIL 1000UH 10% FXD RF
L6	MS75085-11	COIL 220UH 10% FXD RF
L7	L11-0004-031	INDUCT SH VAR 29.7-36.3UH
L8	MS75085-19	COIL 1000UH 10% FXD RF
L9	MS75085-19	COIL 1000UH 10% FXD RF
L10	MS75085-19	COIL 1000UH 10% FXD RF
M1	I51-0003-001	MIXER DB 50mW 500MHZ
Q1	Q35-0001-001	XSTR JFET J310
Q2	2N2222A	XSTR SS/GP NPN TO-18
Q3	2N2222A	XSTR SS/GP NPN TO-18
Q4	2N2222A	XSTR SS/GP NPN TO-18
Q5	2N2222A	XSTR SS/GP NPN TO-18
Q6	2N2222A	XSTR SS/GP NPN TO-18
Q7	2N2222A	XSTR SS/GP NPN TO-18
Q8	Q03-0187-000	XSTR MOSFET
Q9	2N2222A	XSTR SS/GP NPN TO-18
Q10	2N2222A	XSTR SS/GP NPN TO-18
Q11	2N2222A	XSTR SS/GP NPN TO-18
Q12	2N2907A	XSTR SS/GP PNP TO-18
Q13	2N2222A	XSTR SS/GP NPN TO-18
Q14	2N4091	XSTR JFET N-CH TO-18

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**Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410)  
(Cont.)**

Ref. Desig.	Part Number	Description
Q15	2N2222A	XSTR 5S/GP NPN TO-18
Q16	2N2907A	XSTR 5S/GP PNP TO-18
Q17	2N2222A	XSTR 5S/GP NPN TO-18
Q18	Q05-0002-000	XSTR JFET
Q19	2N2907A	XSTR 5S/GP PNP TO-18
Q20	2N2222A	XSTR 5S/GP NPN TO-18
Q21	2N2222A	XSTR 5S/GP NPN TO-18
Q22	2N2222A	XSTR 5S/GP NPN TO-18
Q23	2N2907A	XSTR 5S/GP PNP TO-18
Q24	2N2907A	XSTR 5S/GP PNP TO-18
R1	R65-0003-181	RES 180 5% 1/4W CAR FILM
R2	R65-0003-561	RES 560 5% 1/4W CAR FILM
R3	R65-0003-101	RES 100 5% 1/4W CAR FILM
R4	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R5	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R6	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R7	R65-0003-200	RES 20 5% 1/4W CAR FILM
R8	R40-0008-101	RES,VAR , 100
R9	R65-0003-431	RES 430 5% 1/4W CAR FILM
R10	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R11	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R12	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R13	R65-0003-221	RES 220 5% 1/4W CAR FILM
R14	R65-0003-390	RES 39 5% 1/4W CAR FILM
R15	R65-0003-431	RES 430 5% 1/4W CAR FILM
R16	R65-0003-101	RES 100 5% 1/4W CAR FILM
R17	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R19	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R20	R65-0003-561	RES 560 5% 1/4W CAR FILM
R21	R65-0003-101	RES 100 5% 1/4W CAR FILM
R22	R65-0003-361	RES 360 5% 1/4W CAR FILM
R23	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R24	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R25	R65-0003-271	RES 270 5% 1/4W CAR FILM
R26	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R27	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-561	RES 560 5% 1/4W CAR FILM
R30	R65-0003-270	RES 27 5% 1/4W CAR FILM
R31	R65-0003-431	RES 430 5% 1/4W CAR FILM
R32	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R33	R65-0003-221	RES 220 5% 1/4W CAR FILM
R34	R65-0003-431	RES 430 5% 1/4W CAR FILM
R35	R65-0003-101	RES 100 5% 1/4W CAR FILM

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**RF COMMUNICATIONS**

**Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410)  
(Cont.)**

Ref. Desig.	Part Number	Description
R36	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R37	R65-0003-120	RES 12 5% 1/4W CAR FILM
R38	R65-0003-101	RES 100 5% 1/4W CAR FILM
R39	R65-0003-301	RES 300 5% 1/4W CAR FILM
R40	R65-0003-180	RES 18 5% 1/4W CAR FILM
R41	R65-0003-301	RES 300 5% 1/4W CAR FILM
R42	R65-0003-510	RES 51 5% 1/4W CAR FILM
R43	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R44	R65-0003-183	RES 18K 5% 1/4W CAR FILM
R45	R65-0003-201	RES 200 5% 1/4W CAR FILM
R46	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R47	R65-0003-201	RES 200 5% 1/4W CAR FILM
R48	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R49	R65-0003-221	RES 220 5% 1/4W CAR FILM
R50	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R51	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R52	R65-0003-201	RES 200 5% 1/4W CAR FILM
R53	R65-0003-561	RES 560 5% 1/4W CAR FILM
R54	R65-0003-100	RES 10 5% 1/4W CAR FILM
R55	R65-0003-431	RES 430 5% 1/4W CAR FILM
R56	R65-0003-433	RES 43K 5% 1/4W CAR FILM
R57	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R58	R65-0003-100	RES 10 5% 1/4W CAR FILM
R59	R65-0003-331	RES 330 5% 1/4W CAR FILM
R60	R65-0003-510	RES 51 5% 1/4W CAR FILM
R70	R65-0003-271	RES 270 5% 1/4W CAR FILM
R71	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R72	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R73	R65-0003-751	RES 750 5% 1/4W CAR FILM
R74	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R75	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R76	R65-0003-561	RES 560 5% 1/4W CAR FILM
R77	R65-0003-161	RES 160 5% 1/4W CAR FILM
R78	R65-0003-561	RES 560 5% 1/4W CAR FILM
R79	R65-0003-122	RES 1.2K 5% 1/4W CAR FILM
R80	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R81	R65-0003-101	RES 100 5% 1/4W CAR FILM
R82	R65-0003-101	RES 100 5% 1/4W CAR FILM
R83	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R84	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R85	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R86	R65-0003-681	RES 680 5% 1/4W CAR FILM
R87	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R88	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R89	R65-0003-104	RES 100K 5% 1/4W CAR FILM



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**Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410)  
(Cont.)**

Ref. Desig.	Part Number	Description
R90	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R92	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R93	R65-0003-910	RES 91 5% 1/4W CAR FILM
R94	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R95	R65-0003-910	RES 91 5% 1/4W CAR FILM
R96	R65-0003-181	RES 180 5% 1/4W CAR FILM
R97	R65-0003-621	RES 620 5% 1/4W CAR FILM
R98	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R99	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R100	R65-0003-244	RES 240K 5% 1/4W CAR FILM
R101	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R102	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R103	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R104	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R105	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R106	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R107	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R108	R65-0003-470	RES 47 5% 1/4W CAR FILM
R109	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R110	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R111	R65-0003-303	RES 30K 5% 1/4W CAR FILM
R112	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R113	R65-0003-561	RES 560 5% 1/4W CAR FILM
R114	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R115	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R116	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R117	R65-0003-334	RES 330K 5% 1/4W CAR FILM
R118	R65-0003-124	RES 120K 5% 1/4W CAR FILM
R119	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R120	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R121	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R122	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R123	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R125	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R126	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R127	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R128	R65-0003-511	RES 510 5% 1/4W CAR FILM
R129 - R131	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R132 - R135	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R136	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R137	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R138	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R140	R65-0003-132	RES 1.3K 5% 1/4W CAR FILM
R141	R65-0003-244	RES 240K 5% 1/4W CAR FILM
R142, R143	R65-0003-473	RES 47K 5% 1/4W CAR FILM

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**Table 3. IF/Audio Motherboard Assembly A5A1 Maintenance Parts List (PL 10073-5410)  
(Cont.)**

Ref. Desig.	Part Number	Description
R144	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R145	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R146	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R147	R65-0003-244	RES 240K 5% 1/4W CAR FILM
R148	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R149	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R150	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R151	R65-0003-623	RES 62K 5% 1/4W CAR FILM
R152	R65-0003-754	RES 750K 5% 1/4W CAR FILM
R153	R65-0003-563	RES 56K 5% 1/4W CAR FILM
R154	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R155	R65-0003-270	RES 27 5% 1/4W CAR FILM
R156	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R157 R158	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R159	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R161	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R162	R65-0003-471	RES 470 5% 1/4W CAR FILM
R163	R65-0003-101	RES 100 5% 1/4W CAR FILM
R164	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R165	R65-0003-511	RES 510 5% 1/4W CAR FILM
R166 - R168	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R169	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R170	D40-0004-004	THERM, 2K, 5%
R171	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R172	R65-0003-511	RES 510 5% 1/4W CAR FILM
T1	10073-7026	TRANSFORMER, RF, FIXED
T2	T60-0004-001	TRANSFORMER
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP7	J-0073	TP PWB VIO TOP ACCS .080"
TP8	J-0074	TP PWB GRA TOP ACCS .080"
TP9	J-0065	TP PWB WHT TOP ACCS .080"
TP10	J-0067	TP PWB BLK TOP ACCS .080"
TP11	J-0071	TP PWB BRN TOP ACCS .080"
TP12	J-0066	TP PWB RED TOP ACCS .080"
U1	I30-0036-001	IC 5534 OP AMP PLASTIC
U2	I60-0003-001	IC FM IF AMP
U3	I01-0000-252	IC 4053B PLASTIC CMOS
U4	I06-0002-001	IC DG211 PLASTIC CMOS
U5	I30-0035-000	IC 072 OP AMP PLASTIC
U6 - U9	I30-0003-000	IC 324 OP AMP PLASTIC
VR1	I12-0010-005	IC VR 79L05A -5V .10A 4%
VR2	I12-0005-005	IC VR 78L05 +5V .10A 10

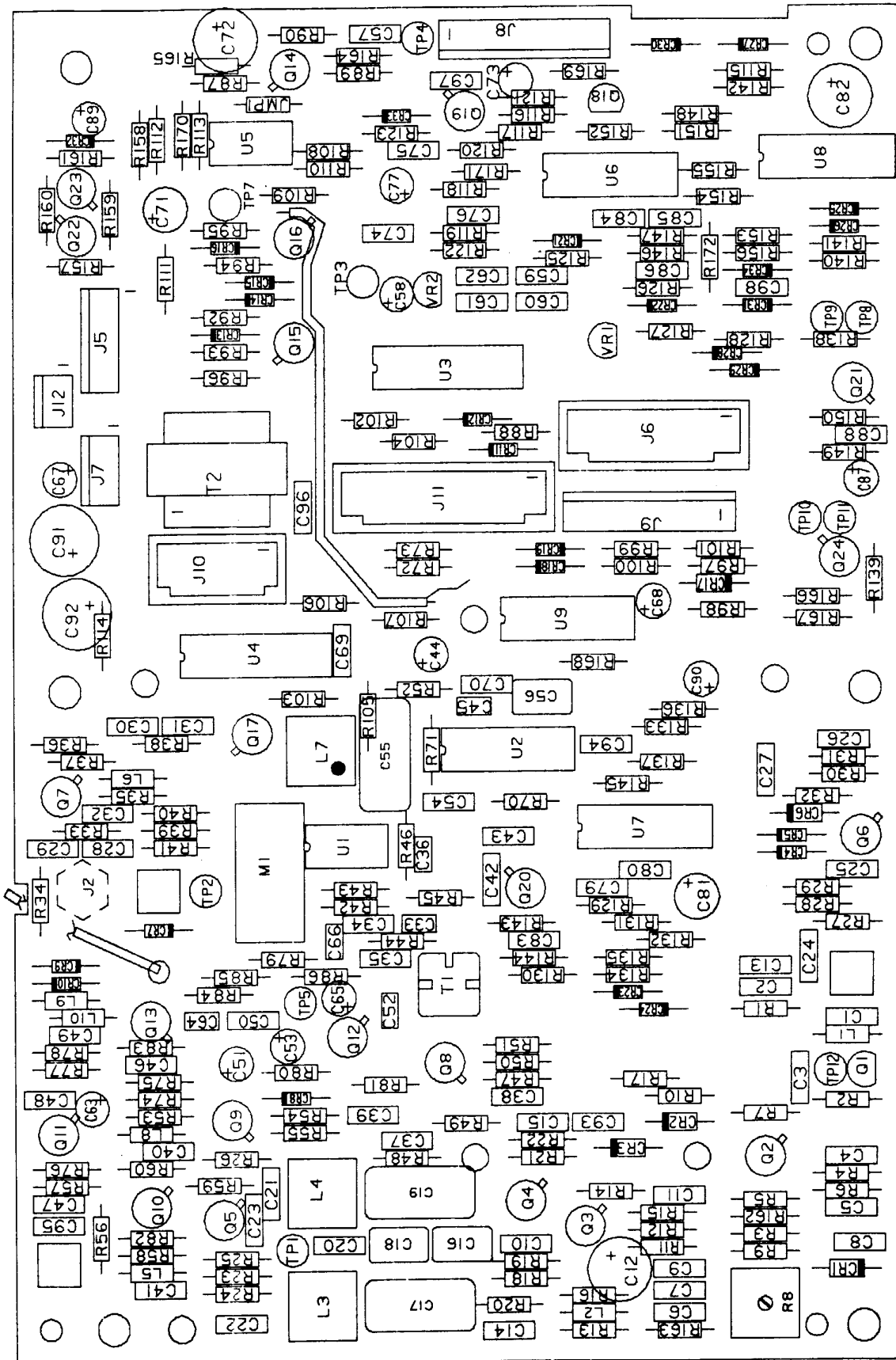


Figure 3. IF/Audio Motherboard Assembly A5A1 Component Location Diagram (10073-5410, Rev. E)

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- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. COMPLETE DESIGNATION, PREFIX, UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 15%.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS, 200VDC.
  4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  5. ▽ INDICATES SINGLE POINT GROUND.

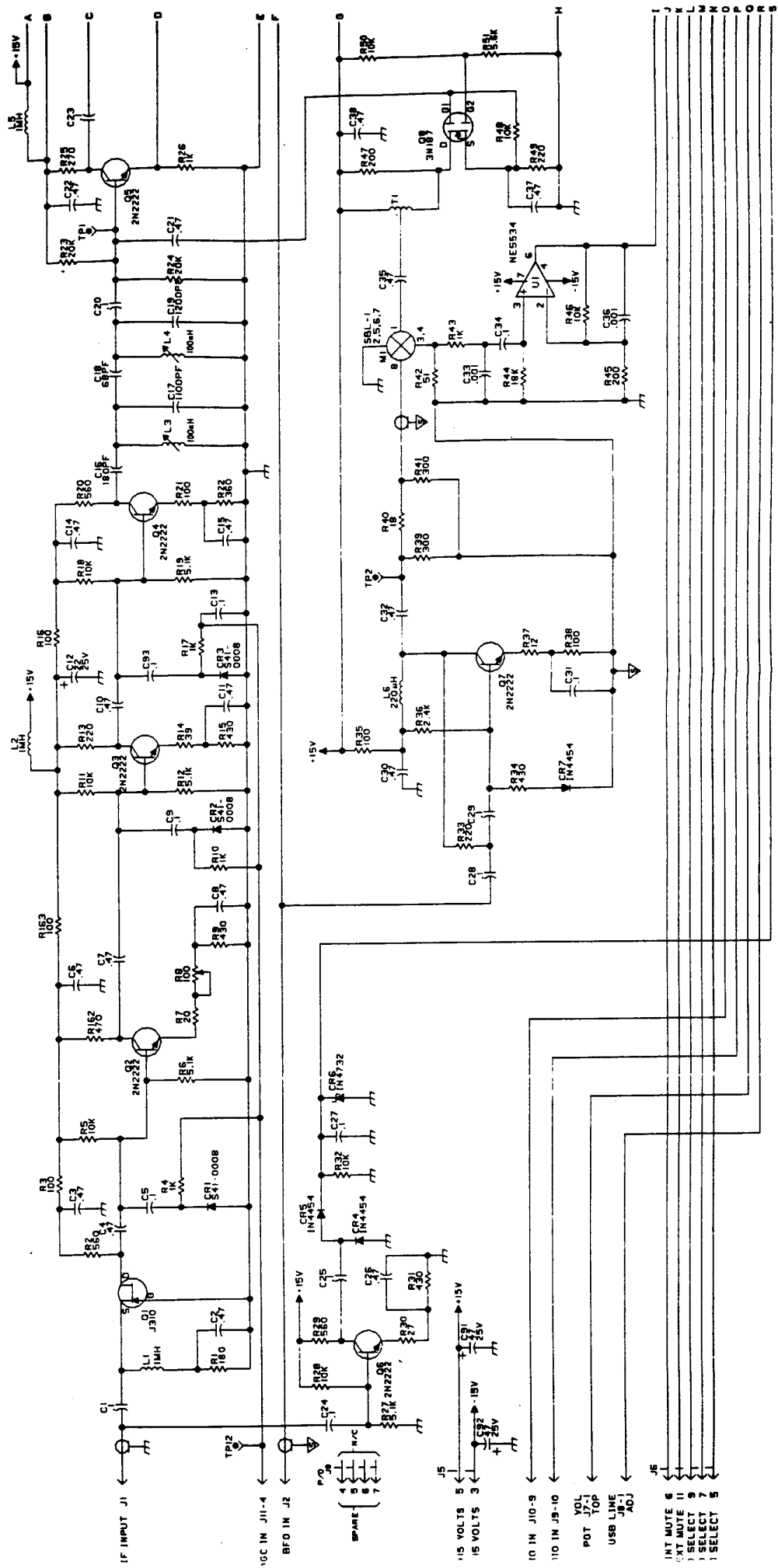


Figure 4. IF/Audio Motherboard ASB1 Schematic  
Diagram (10073-5411, Rev. J)  
(Sheet 1 of 4)



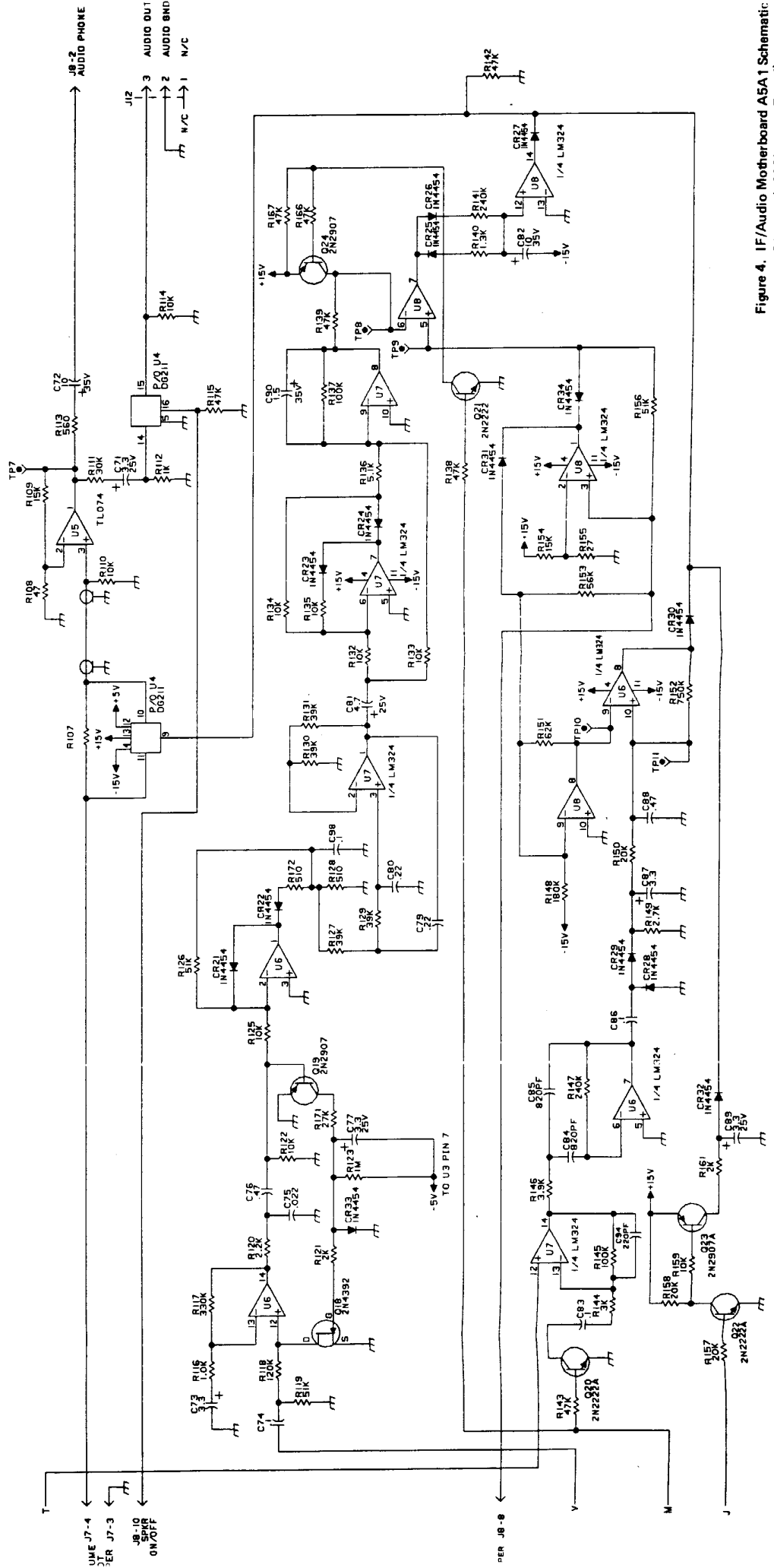


Figure 4. IF/Audio Motherboard A5A1 Schematic Diagram (10073-5411, Rev. J) (Sheet 3 of 4)

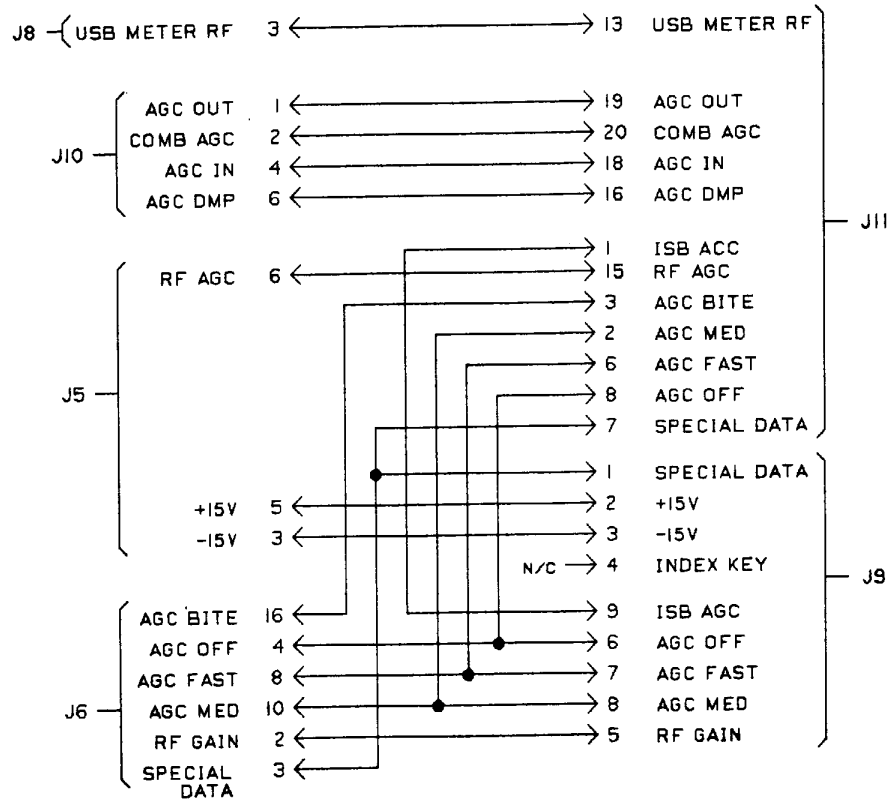
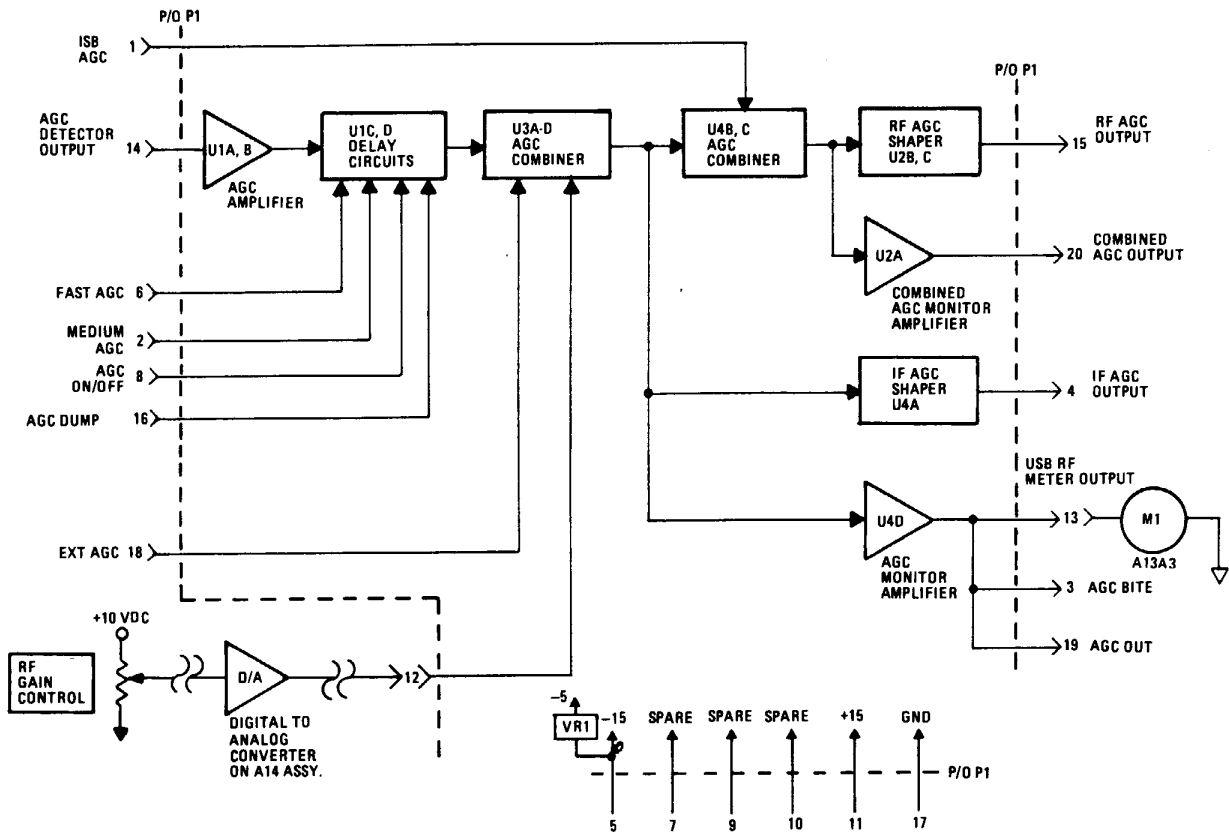


Figure 4. IF/Audio Motherboard A5A1 Schematic Diagram (10073-5411, Rev. J) (Sheet 4 of 4)



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**IF/Audio AGC Assembly A5A2 Functional Block Diagram**



## 7. A5A2 AGC ASSEMBLY GENERAL DESCRIPTION

AGC Assembly A5A2 contains circuits that automatically control receiver gain over a 120 dB dynamic range. RF input levels at the antenna input from 1 uVrms to 1 Vrms will produce no more than a 3 dB change in audio output level.

Shaping circuitry on the A5A2 assembly provides the following automatic gain control characteristics:

- Attack time – fixed: less than 20 mseconds
- Decay time – selectable: fast, less than 30 mseconds; medium,  $200 \pm 50$  mseconds; slow,  $4 \pm 1$  second

Signal monitoring circuits include the following:

- RF signal strength via RF-590 front panel metering
- BITE detection of the AGC output level

Receiver gain control may also be accomplished when any of the following signals are present:

- RF Gain (Local manual control from the RF-590 front panel.)
- External AGC (A rear panel input for remote control of the gain controlling circuits.)
- ISB AGC (Used when the ISB option is installed in the receiver. In this case, the stronger of the two received sideband signals will control receiver gain.)

Additionally, AGC output and combined AGC output (when ISB operation is utilized) signals are available at the receiver rear panel.

The A5A2 assembly is mounted to the A5A1 assembly, and signals flow from A5A2P1 to A5A1J9 and J11. Once these signals arrive at the A5A1 assembly, they are directed to various other connectors on the A5A1 assembly and then routed to other assemblies in the radio. Table 4 details the input/output connections and any relevant data.

**Table 4. AGC Assembly A5A2 Interface Connections**

Connector	Function	Characteristics
P1-1	ISB AGC	+5 Vdc = Selected  Typically 1.5 Vdc during BITE Test
P1-2	MED AGC	
P1-3	AGC BITE	

Table 4. AGC Assembly A5A2 Interface Connections (Cont.)

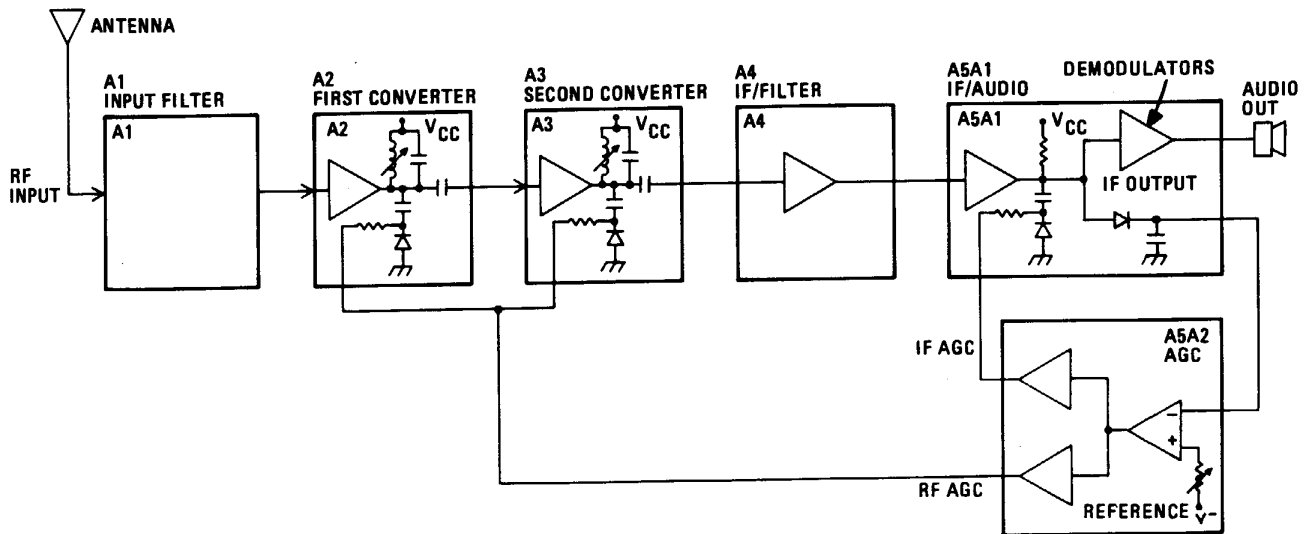
Connector	Function	Characteristics
P1-4	IF AGC	0 to -3 Vdc
P1-5	Power	-15 Vdc
P1-6	FAST AGC	+5 Vdc = Selected
P1-7	Spare	
P1-8	AGC ON/OFF	+5 Vdc = AGC OFF
P1-9	Spare	
P1-10	Spare	
P1-11	Power	+15 Vdc
P1-12	RF Gain	0 to +12 Vdc
P1-13	USB RF Meter Output	
P1-14	AGC Detector	Typically -1 Vdc
P1-15	RF AGC Output	Typically 0 to -6 Vdc
P1-16	AGC Dump	+5 Vdc = AGC off
P1-17	Ground	
P1-18	External AGC	Typically 0 to +6 Vdc
P1-19	AGC Output	Typically 0 to -6 Vdc
P1-20	Combined AGC Output	

## 8. CIRCUIT DESCRIPTIONS

### 8.1 AGC Operation

Figure 5 is a simplified block diagram which shows the relationship of the AGC assembly to the rest of the radio.

The AGC circuitry in the receiver maintains a constant peak level at the A5A1 IF output. The strength of the IF output is a function of the received RF signal strength at the antenna as well as the gain of all the stages preceding the IF output. If the gain of the receiver could be decreased in proportion to the increasing strength of a received signal (and vice versa), then a constant IF output and audio output will be maintained.



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Figure 5. AGC Operation

The RF-590 AGC circuits accomplish this by sampling the IF output signal, converting it into a dc signal whose amplitude is a function of signal strength and comparing it to a reference signal. Any difference in amplitude between these two signals will cause an error signal to develop. This error signal is fed back to PIN diode attenuator circuits throughout the radio, and causes the diodes to alter the impedance of the output stages of selected amplifier stages. In so doing, they have modified the stage gain. Therefore, for large RF input signals (and IF output signals) there will be a large error voltage generated, a large change in amplifier output impedance, and a large decrease in receiver gain. The converse is true for small RF input signals, although there is an AGC threshold limit at which low level RF signals will not cause gain reduction.

## 8.2 AGC Amplifiers

The circuits which produce the actual AGC voltage consist of the four sections of U1. U1A is a noninverting buffer which amplifies the detected AGC signal provided by the A5A1 assembly. Section U1B is the AGC loop error amplifier which generates the AGC error voltage that controls the receiver gain. This differential amplifier has a gain of 10 for inputs greater than the error reference, and a gain of 0 for inputs below the error reference. The error reference signal is set by potentiometer R5 at the noninverting input of the amplifier.

The decay time of the AGC voltage is set by the discharge time constant of C3. The discharge rate is a function of the shunt resistance of C3, and is altered by adding or removing resistance via Q1 and Q2. When Q1 and Q2 are off, only R11 is the discharge path (corresponding to slow AGC speed). Turning Q2 on, shunts R11 with R10 (decreasing the total shunt resistance, etc). These decay speeds are front panel selectable.

Shorting C3 out via a low resistance to ground through Q3 disables the AGC entirely. This will happen in response to the AGC off command from the front panel (so that manual gain control may be used) or to the rear panel AGC dump signal.

U1D is strictly a noninverting buffer stage which presents C3 with a high impedance input so that charge will not leak off and alter the AGC time constants.

### **8.3 AGC Combination and Control Circuits**

The receiver is designed to have a great deal of flexibility in controlling the receiver gain. The first method, as discussed above, is the receiver Automatic Gain Control (AGC). Also available from the front panel is an RF GAIN control, and from the rear panel connector there is an external AGC control.

The different gain controls are combined together using quad op amp U3. The combination is implemented using an analog OR gate that passes the largest of the four inputs on the gain control bus (TP5). The fourth input is an internal adjustment, potentiometer R19, that can be used to reduce the receiver gain, and thereby increase the AGC threshold.

None of these four inputs are ever disabled, so take care when using the receiver so that the gain control bus is not overridden by an undesired input. The best example of this is the front panel RF GAIN control. The RF GAIN control is supplied by the processor and is selected either from the front panel or the remote controller. It is the output of a digital to analog converter and is under direct processor control. (The converter output has a low pass filter to remove processor noise and to eliminate any ripple on the gain control voltage that would produce undesired modulation in the signal path.)

For proper operation of the AGC circuitry, the RF GAIN control should be at its maximum position to ensure full receiver sensitivity.

The output of the IF gain combiner U3 provides the input to the IF AGC shaping circuitry. It is also compared to the ISB AGC input for control of the RF AGC. The larger of the two AGC levels will then be the input to the RF AGC shaping circuitry. This will ensure that the gain of the input RF amplifiers will be at the correct level to avoid overload by the greater of the two sidebands when ISB operation is used. The IF strip AGC circuits will then control their own gain as required.

### **8.4 AGC Outputs**

#### **8.4.1 Shaping Circuitry**

As previously mentioned, the AGC action maintains a constant level at the IF output. This is accomplished by supplying an increasing linear AGC voltage to the PIN diode attenuators in the signal path (in response

to a logarithmic increase in RF signal strength). The RF AGC and IF AGC shaping circuitry provides a means to control the response of the PIN diodes to accomplish this.

Temperature compensation for the PIN diodes is provided by summing a temperature dependent offset voltage into the input of each shaping network. The temperature coefficient of gain of each gain controlled stage can be maintained at an acceptable minimum.

Note that two AGC shaping networks are required, since it is desirable to have RF AGC reduction (A2, A3 assemblies) begin at a higher RF input level than IF AGC reduction (A5A1 assembly). IF AGC reduction typically begins at RF signal levels on the order of .5  $\mu\text{Vrms}$ , while RF AGC reduction begins approximately 50 dB above this threshold.

#### 8.4.1.1 IF AGC Shaping

The shaping and compensation circuitry for the IF strip on the A5A2 assembly consists of op amp U4A and its associated circuitry. Q4 serves as a current buffer and is included within the circuit's feedback network. R30 acts to limit the maximum output current and protect Q4. Potentiometer R28 provides an adjustment in the shaping circuitry to compensate for variations between individual PIN diodes so that the meter indication of signal strength is calibrated in each receiver. The input to this circuit at TP5 is the AGC voltage which increases from 0 to 6 volts as the receiver gain decreases by 120 dB. The IF strip provides 80 dB of the necessary attenuation, and this requires approximately -2 volts on the IF AGC output. There is one gain breakpoint caused by CR10, and this occurs at the point when the AGC in the RF amplifiers begins (approximately 50 dB above AGC threshold). Temperature compensation is provided by CR11, R25, and R24. R24 sets the diode offset and R25 sets the offset temperature coefficient.

#### 8.4.1.2 RF AGC Shaping

The shaping circuitry for the RF AGC consists of op amp sections U2B, U2C, and their associated components. U2B is used to implement the necessary temperature compensation, along with the RF AGC threshold. The RF AGC threshold is set so that AGC action to the RF amplifiers in the receiver does not begin until 50 dB above AGC threshold. This was done to ensure that the S/N ratio of the receiver would increase linearly to at least 50 dB before the noise figure of the receiver input was degraded by RF AGC action. The RF threshold circuit subtracts 2.5 volts from the AGC input voltage to shaping circuit U2C. Temperature compensation for the RF AGC is provided by CR17 and R37. R37 sets the diode offset and temperature coefficient gain. The operation of U2B is noninverting.

U2C performs the shaping for the RF AGC. There are two breakpoints in the nonlinear approximation set by CR18 and CR19. These diodes are reverse biased by resistor pairs R42 and R43, and R40 and R41 respectively. When the diodes become forward biased by the increasing input, they conduct and increase the circuit gain by lowering the input impedance of the inverting amplifier. Potentiometer R45 provides adjustment of the shaping circuit gain to compensate for individual PIN diode variations. Q5 acts as a current buffer and is included in the amplifier feedback network. R47 provides current limiting protection for Q5.

The input to the shaping circuit is the receiver AGC voltage minus 2.5 volts. The input can be found at TP4. (The receiver AGC voltage is available at TP5). The output of the shaping circuit is a negative voltage that increases to approximately -8 volts (maximum) at full gain reduction, and is available at TP6. RF AGC action provides typically 40 dB of attenuation at maximum AGC voltages, with 20 dB occurring in the A2 assembly and 20 dB occurring in the A3 assembly.

#### 8.4.2 AGC Output Monitor Lines

There are four output monitor lines from the AGC assembly; the AGC OUT line, the AGC BITE line, the USB Meter RF line, and the Comb AGC OUT line. The first is the buffered AGC voltage which goes to the rear panel. The second is the AGC voltage divided by three which goes to the processor BITE circuitry. It has a 4.7 volt Zener diode on its output to protect the BITE circuitry against overvoltage. The USB Meter RF line goes to the front panel meter to provide signal strength information. The AGC voltage is calibrated to provide a linear 6.0 volt rise for an increase of 120 dB of signal strength above AGC threshold. The meter itself is a 100  $\mu$ A meter, so R49 (a 62 K resistor) provides the proper meter drive.

The Comb AGC OUT line is the output of the IF AGC and ISB AGC combiner. This line monitors the AGC control voltage going to the RF AGC shaping circuitry.

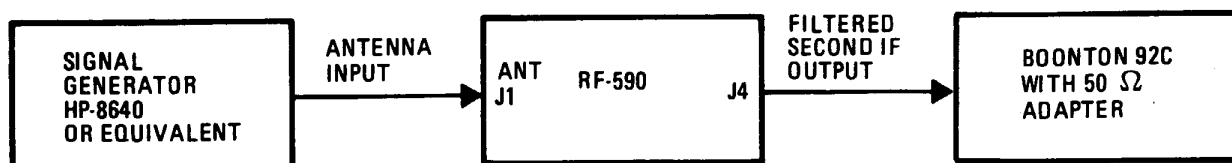
### 9. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests are performed with all assembly connections in normal contact, unless otherwise specified. It is further assumed that all other circuits in the RF path are operational and properly aligned.

#### 9.1 AGC Alignment

Perform the following procedure to align the AGC assembly.

- a. Remove the ribbon cable connecting the AGC Assembly A5A2 to the IF/Audio Amp Assembly A5A1.
- b. Connect equipment as shown in figure 6. Set generator to 10.0015 MHz and RF output to OFF. Set spectrum analyzer to the second IF frequency (455 kHz).



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Figure 6. AGC Assembly Alignment

- c. Turn on the receiver and set controls as follows:
  - Frequency to 10.000000 MHz
  - Mode to USB
  - USB meter button to USB/RF
  - RF GAIN to fully clockwise (cw)
  - AGC to OFF
- d. Rotate R19 fully counterclockwise (ccw) and measure TP5 (should be 0 Vdc).
- e. Turn the receiver off and reconnect the ribbon cable between the AGC Assembly A5A2 and the IF/Audio Amp Assembly A5A1.
- f. Turn on the receiver and set AGC to MED and generator output to -60 dBm. Adjust A5A2R5 for -7 dBm at second IF output.
- g. Decrease signal generator to 10  $\mu$ Vrms. Adjust A5A2R28 for a 10  $\mu$ Vrms reading on the RF-590 front panel meter.
- h. Increase signal generator to 10 mVrms. Adjust A5A2R45 for a 10 mVrms reading on the front panel meter.
- i. Note that the second IF output remains at a constant -7 dBm level between the two RF input extremes in steps g. and h.
- j. Initiate the receiver BITE self-test. The receiver must not fail at 05-01, the AGC test. Test is complete.

## 10. PARTS LIST

Table 5 is a comprehensive parts list of all replaceable components in IF/Audio AGC Assembly A5A2. When ordering parts from the factory, include a full description of the part. Use figure 7, IF/Audio AGC Assembly A5A2 Component Location Diagram to identify parts.

## 11. SCHEMATIC DIAGRAM

Figure 8 is the IF/Audio AGC Assembly A5A2 schematic diagram.

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**Table 5. IF/Audio AGC Assembly A5A2 Maintenance Parts List (PL 10073-5450)**

Ref. Desig.	Part Number	Description
	10073-5450	PWB, IF/AUDIO AGC
C1	C26-0025-100	CAP 10UF 20% 25V TANT
C2	C26-0025-100	CAP 10UF 20% 25V TANT
C3	C25-0003-209	CAP 22UF 10% 25V TANT
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
CR1	1N4454	DIODE 200mA 75V SW
CR2	1N4454	DIODE 200mA 75V SW
CR3	1N4454	DIODE 200mA 75V SW
CR4	1N4454	DIODE 200mA 75V SW
CR5	1N4454	DIODE 200mA 75V SW
CR6	1N4454	DIODE 200mA 75V SW
CR7	1N4454	DIODE 200mA 75V SW
CR8	1N4454	DIODE 200mA 75V SW
CR9	1N4454	DIODE 200mA 75V SW
CR10	1N4454	DIODE 200mA 75V SW
CR11	1N4454	DIODE 200mA 75V SW
CR12	1N4454	DIODE 200mA 75V SW
CR13	1N4454	DIODE 200mA 75V SW
CR14	1N4454	DIODE 200mA 75V SW
CR15	1N4454	DIODE 200mA 75V SW
CR16	1N4454	DIODE 200mA 75V SW
CR17	1N4454	DIODE 200mA 75V SW
CR18	1N4454	DIODE 200mA 75V SW
CR19	1N4454	DIODE 200mA 75V SW
CR20	1N4454	DIODE 200mA 75V SW
CR21	1N4732	DIODE 4.7V 10% 1W ZENER
P1	10073-7072	RIBBON CABLE, 20 COND
Q1	2N2222A	XSTR SS/GP NPN TO-18
Q2	2N2222A	XSTR SS/GP NPN TO-18
Q3	2N2222A	XSTR SS/GP NPN TO-18
Q4	2N2907A	XSTR SS/GP PNP TO-18
Q5	2N2907A	XSTR SS/GP PNP TO-18
R1	R65-0003-432	RES 4.3K 5% 1/4W CAR FILM
R2	R65-0003-432	RES 4.3K 5% 1/4W CAR FILM
R3	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R4	R65-0003-432	RES 4.3K 5% 1/4W CAR FILM
R5	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
R6	R65-0003-433	RES 43K 5% 1/4W CAR FILM
R7	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R8	R65-0003-431	RES 430 5% 1/4W CAR FILM
R9	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R10	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R11	R65-0003-474	RES 470K 5% 1/4W CAR FILM



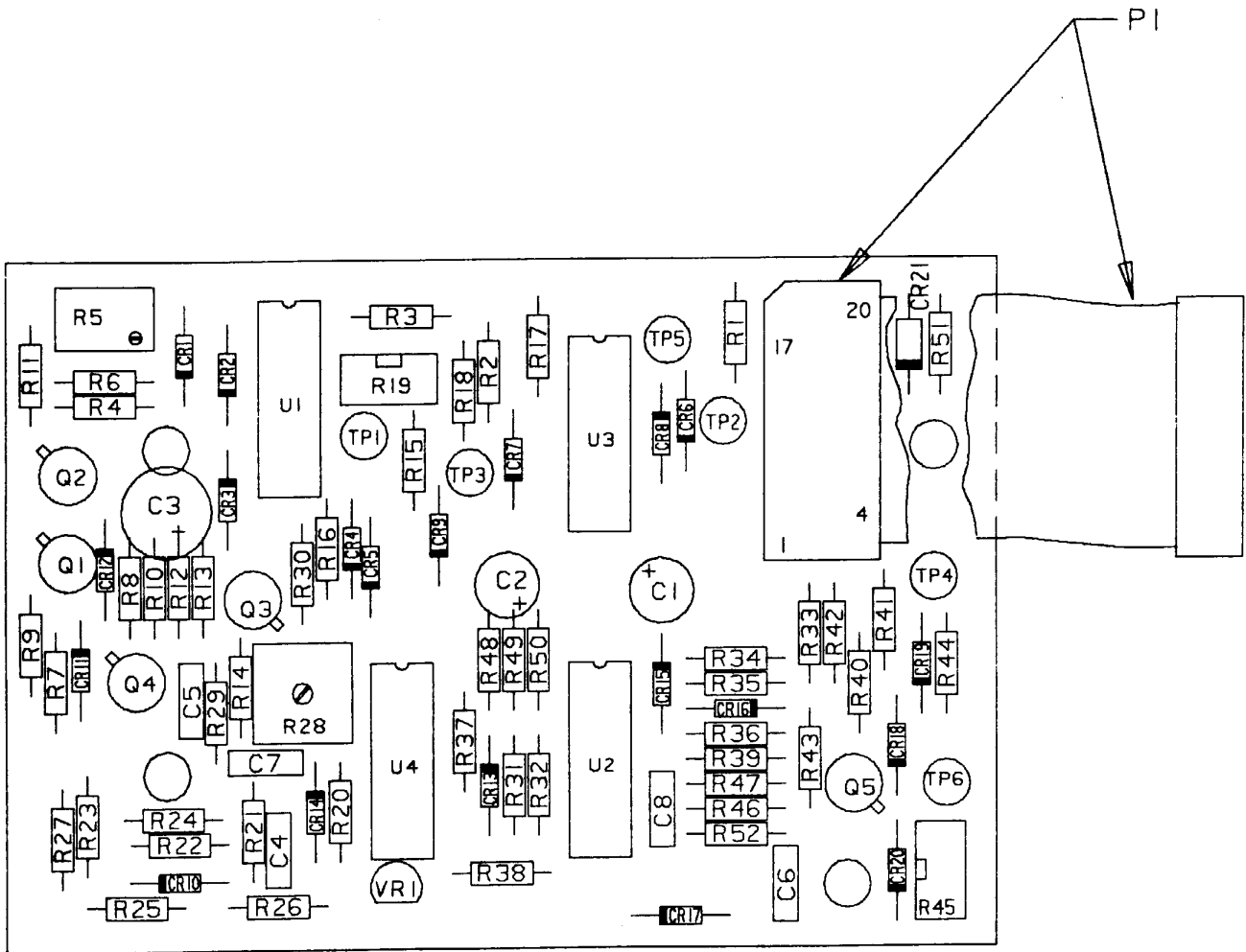
**Table 5. IF/Audio AGC Assembly A5A2 Maintenance Parts List (PL 10073-5450) (Cont.)**

Ref. Desig.	Part Number	Description
R12	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R13	R65-0003-100	RES 10 5% 1/4W CAR FILM
R14	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R15	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R16	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R19	R-2226	RES,VAR,PCB 2K .5 20%
R20	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R21	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R22	R65-0003-683	RES 68K 5% 1/4W CAR FILM
R23	R65-0003-822	RES 8.2K 5% 1/4W CAR FILM
R24	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R25	R65-0003-751	RES 750 5% 1/4W CAR FILM
R26	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R27	R65-0003-681	RES 680 5% 1/4W CAR FILM
R28	R-2205	RES,VAR,PCB 500 .5 20%
R29	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R30	R65-0003-301	RES 300 5% 1/4W CAR FILM
R31	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R32	R65-0003-243	RES 24K 5% 1/4W CAR FILM
R33	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R34	R65-0003-751	RES 750 5% 1/4W CAR FILM
R35	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R36	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R37	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R38	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R39	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R40	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R41	R65-0003-363	RES 36K 5% 1/4W CAR FILM
R42	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R43	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R44	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R45	R-2228	RES,VAR,PCB 10K .5 20%
R46	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R47	R65-0003-301	RES 300 5% 1/4W CAR FILM
R48	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R49	R65-0003-623	RES 62K 5% 1/4W CAR FILM
R50	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R51	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R52	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"

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**Table 5. IF/Audio AGC Assembly A5A2 Maintenance Parts List (PL 10073-5450) (Cont.)**

Ref. Desig.	Part Number	Description
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP6	J-0072	TP PWB BLU TOP ACCS .080"
U1	130-0003-000	IC 324 OP AMP PLASTIC
U2	130-0003-000	IC 324 OP AMP PLASTIC
U3	130-0003-000	IC 324 OP AMP PLASTIC
U4	130-0003-000	IC 324 OP AMP PLASTIC
VR1	112-0010-005	IC VR 79L05A -5V .10A 4%



**Figure 7. IF/Audio AGC Assembly A5A2 Component Location Diagram (10073-5450, Rev. D)**

- NOTE: UNLESS OTHERWISE SPECIFIED:  
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.  
 2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.  
 3. ALL CAPACITOR VALUES ARE IN MICROFARADS.  
 4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

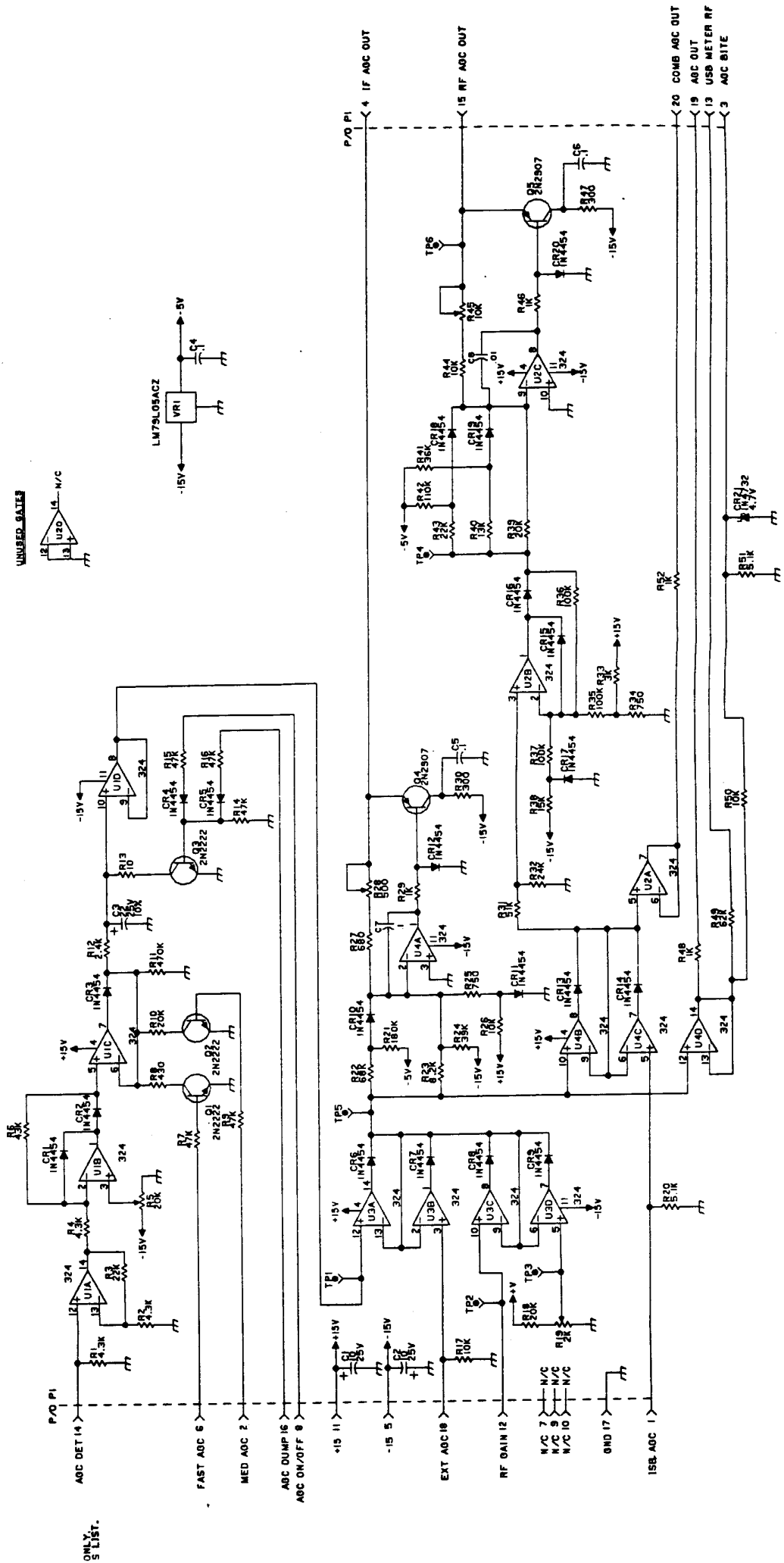


Figure 8. IF/Audio AGC Assembly A5A2  
Schematic Diagram (10073-6451, Rev. D)

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## 1. GENERAL DESCRIPTION

PLL I Assembly A6 is a translation type phase lock loop which performs the following primary functions.

- Combination of the 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, and 10 MHz tuning increments information
- Frequency translation of these increments to the required Local Oscillator (LO) no. 1 range of 40.465 to 70.455 MHz

Coarse tuning increments (100 kHz, 1 MHz, and 10 MHz) arrive from the A7 assembly are combined with the fine tuning increments (1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz) from the A8 assembly. Occurring simultaneously with this combination function is frequency translation to the Local Oscillator no. 1 range. This signal is then applied to First Converter Assembly A2, where it functions as the first local oscillator injection for A2 Mixer M1. This signal which is continuously variable in 1 Hz steps allows the RF-590 to tune from 10 kHz to 30 MHz, constantly maintaining a first intermediate frequency (IF) of 40.455 MHz (IF no. 1 = LO no. 1 - Radio tune frequency).

PLL I Assembly A6 consists of the following four separate subassemblies.

- Motherboard Assembly A6A1
- VCO Assembly A6A2
- Mixer Assembly A6A3
- Phase Comparator Assembly A6A4

The A6A2, A6A3, and A6A4 subassemblies are separate printed circuit boards which are mounted to the A6A1 motherboard. All three subassemblies are independently shielded from each other and other circuitry on the motherboard by separate shield cans which completely surround each subassembly.

Plug-in mating connectors connect each subassembly to the others. Signals which originate or terminate off the A6 assembly are connected via coax cables and connectors or through the one main plug-in type control connector, J1.

## 2. INTERFACE CONNECTIONS

Table 1 details the input/output connections and other relevant data for all signals which originate or terminate off the A6 assembly. (A6 subassembly interconnections are not shown.)

**Table 1. PLL I Assembly A6 Interface Connections**

Connector	Function	Characteristic
A6A1J1-1	+24 Volts	Approximately 20 mA
-2	Index	
-3	Ground	
-4	+5 Volts Unregulated	Approximately 200 mA
-5	Lock Detector Output	0 V = PLL locked, +5 V = PLL unlocked
-6	+15 Volts	Approximately 25 mA
A6A1P2	PLL II Tracking Reference	+3.5 to +19 Vdc
A6A2P1	LO no. 1	0 dBm, 40.465 to 70.455 MHz (PLL I Output)
A6A3P1	PLL II Output	+4 dBm, 44.1 to 74.0 MHz
A6A4P1	PLL III Output	-2 dBm, 35.45 to 36.45 MHz
A6A1P1	Switch	+4 V at tune frequency < 2 MHz 0 V at tune frequency ≥ 2 MHz

### 3. A6 FREQUENCY GENERATION SCHEME

A PLL intermediate frequency (IF) signal in the range of 3.545 MHz to 3.645 MHz is produced at the output of mixer A6A3U1. This IF signal is a result of the subtractive mixing of the 44.1 to 74.0 MHz PLL II output with a VCO signal from VCO Assembly A6A2 in the range of 40.465 MHz to 70.455 MHz.

This IF signal is converted to TTL levels and divided down to a 354.5 kHz to 365.4 kHz range, and applied to one port of Phase Comparator A6A4U2. The second port of A6A4U2 is the reference signal, a variable 354.5 kHz to 365.4 kHz signal derived from PLL III Assembly A8. Any difference in frequency or phase between these two signals produces an error output from the phase comparator which forces the VCO to change its operating frequency. As the VCO frequency changes, the IF output at mixer A6A3U1 must also change. Eventually the IF derived signal will equal the reference frequency at the Phase Comparator inputs and the Phase Comparator will stop the VCO at the frequency which produced the correct IF.

Since the instantaneous frequencies of the PLL II output and the PLL III output represent the values of the 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, 10 Hz, and 1 Hz receiver tuning positions respectively, the instantaneous frequency of the VCO will be a unique frequency representing all these values. The VCO output is applied to a mixer in the receiver's front end at the A2 assembly and functions as that mixer's LO signal. A change in any of the 10 MHz to 1 Hz tuning positions will cause the LO to change to the frequency required to tune the receiver, producing a constant receiver first intermediate frequency of 40.455 MHz.

Given the receiver tune frequency  $f_o = X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1$  Hz where  $X_8$  through  $X_1$  represent the values of the 10 MHz through 1 Hz tuning positions, the A6 output frequency can be determined by the following formula:

$$FA6 = FA7 - \frac{1}{10} FA8, \text{ Hz}$$

where

$$FA7 = (441 + X_8 X_7 X_6) (100,000), \text{ Hz}$$

$$FA8 = [40,000,000 + 10 (6000 - X_3 X_2 X_1)] - [10,000 (361 + X_5 X_4)], \text{ Hz}$$

Example:  $f_o = 14,682,156$  Hz

$$FA7 = (441 + 146) (100,000) = 58,700,000 \text{ Hz}$$

$$FA8 = [40,000,000 + 10 (6000 - 156)] - [10,000 (361 + 82)] = 40,058,440 - 4,430,000 = 35,628,440 \text{ Hz}$$

$$FA6 = 58,700,000 - \frac{1}{10} (35,628,440) = 55,137,156 \text{ Hz}$$

Note that  $FA6 - f_o = 40,455,000$  Hz. This relationship will be true for all receiver tune frequencies, since 40.455 MHz was chosen as the receiver's first IF.

#### 4. CIRCUIT DESCRIPTIONS

##### 4.1 Mixer Assembly A6A3 Operation

A variable 44.1 to 74.0 MHz, +4 dBm signal containing 100 kHz, 1 MHz, and 10 MHz tuning information from PLL II Assembly A7 enters the A6A3 assembly at P1 and is applied to pin 8 of mixer U1. A VCO derived signal from the A6A2 assembly is fed through -10 dB attenuator network R1-R3 to pin 1 of the mixer. The resultant IF output is a signal in the range of 3.545 to 3.645 MHz at U1, pins 3 and 4.

This signal is attenuated by -6 dB network R4-R6 and then applied to a low pass filter network to remove all undesirable mixer products. Amplifier stage Q1 boosts this signal to approximately 300 mVrms for application to Phase Comparator Assembly A6A4.

##### 4.2 Phase Detector Assembly A6A4 Operation

The IF signal from A6A3 assembly is converted to TTL levels by high gain limiter stage Q5 and Q6 and divided down to the 354.5 kHz to 364.5 kHz range by divide by 10 counter U3. This signal is then applied to the IF port of phase comparator U2.

The reference port of U2 is derived from the PLL III output, and is also in the 354.5 kHz to 364.5 kHz range after division by divide by 10 counters U1 and U4.



When these two signals are equal in frequency and phase, the phase comparator outputs at U2, pins 2 and 13, are at +5 Vdc. All transistors in charge pump network Q1, Q2, and Q3 are biased off. The voltage across C21 is constant, and this will bias transistor A6A2Q2 on the VCO assembly to produce a constant voltage drop across A6A2R9, at A6A2TP1. Consequently, the VCO on the A6A2 assembly is held at a constant frequency.

Assume that the A8 PLL III output increases in frequency due to decreasing the values of any of the 10 kHz through 1 Hz receiver tuning positions. Since the reference signal at the reference port of the Phase Comparator (pin 1) will suddenly be higher in frequency than the IF derived signal at the IF port, U1 produces an error command to lower the VCO frequency and thereby increase the IF feedback signal. This command is in the form of negative pulses at U2, pin 13. The pulse width of this signal is proportional to the difference in frequency and/or phase between the two Phase Comparator inputs. When these negative pulses occur, Q2 is forced on and a charge is drawn out of C21. This causes A6A2Q2 to conduct less, and the level of the VCO control voltage at A6A2TP1 will fall. As it decreases, the VCO frequency decreases, causing a corresponding increase in IF frequency at mixer A6A3U1's output. As the IF feedback signal at the Phase Comparator's input approaches the reference frequency, the output pulses at U2, pin 13, get narrower until they are essentially at a 5 Vdc level again. At this point, the two Phase Comparator inputs are equal in frequency, Q2 is turned off, and the voltage across C21 is constant (but at a new lower value). Consequently, the VCO control voltage is also constant, but at a new lower value, as is the VCO output frequency.

Note that the same sequence of events would have occurred if the A7 PLL II output frequency had decreased due to a decrease in the 10 MHz to 100 kHz receiver tuning positions.

Assume that the A7 PLL II output frequency increases due to increasing the 10 MHz to 100 kHz receiver tuning values. The instantaneous frequency at mixer A6A3U1's output will increase, causing a corresponding increase at the IF input port of the Phase Comparator. This signal will be greater in frequency than the reference signal and consequently U1 issues an error command to raise the VCO frequency in order to lower the mixer's output frequency. This time the negative pulses appear at pin 2 of the Phase Comparator. Q1 is forced on, and in so doing, turns Q3 on. Q3 begins pumping a charge into C21, raising its voltage. This turns A6A2Q1 on harder and a rising voltage occurs at A6A2TP1, the VCO control voltage. This voltage forces the VCO frequency to increase. Mixer A6A3U1's output (IF) frequency therefore decreases and continues to do so until the two signals at the Phase Comparator inputs are again equal. At that time, the output pulses at U2, pin 2, are essentially at 5 Vdc, Q1 and Q2 turn off, and the VCO control voltage stops at a new higher value (as does the VCO frequency).

Note that the same sequence of events would have occurred if the A8 PLL III output decreased in frequency due to increasing any of the values of the receiver's 10 kHz through 1 kHz tuning positions.

#### **4.3 VCO/Loop Filter A6A2 Operation**

A charge pump circuit on the A6A4 assembly converts the Phase Comparator's pulse outputs into an analog dc voltage and applies it to terminal E2 of VCO/Loop Filter Assembly A6A2. Q2 generates the actual VCO control voltage across R9 at TP1, and applies the signal through a low pass filter (LPF) network to the varactor diode string in the VCO. The LPF removes any noise transients on the VCO control voltage

line which could shift the VCO frequency. The VCO is a JFET Hartley Oscillator stage (Q1) whose frequency shifts as the varactor diodes capacitance changes in response to changes in VCO control voltage. A VCO control voltage range at TP1 of approximately 3.5 Vdc to 19.0 Vdc shifts the VCO frequency from 40.455 MHz to 70.455 MHz.

The VCO output is fed to two separate amplifier stages. The first, Q4, boosts the signal to 0 dBm and routes the signal through P1 to First Converter Assembly A2, where it functions as the first LO injection for mixer A2U1. The second stage is on the A6A1 motherboard and consists of transistors A6A1Q3 and A6A1Q4. This signal is simply referred to as the VCO output, and is boosted to approximately -6 dBm prior to application to mixer A6A3U1 on the mixer assembly; the VCO feedback loop is therefore completed.

#### 4.3.1 Other VCO Control Circuits

There are two other circuits which can cause the VCO control voltage to change. They are the PLL II Tracking Reference/Clamp circuit (motherboard transistors A6A1Q1 and A6A1Q2) and the 2 MHz switch circuit (VCO/Loop Filter transistor A6A2Q3).

##### 4.3.1.1 PLL II Tracking Reference/Clamp Circuit

The PLL II tracking reference/clamp circuit forces the PLL I VCO to track the PLL II VCO. In so doing, it shortens the receiver tuning time. It also prevents the PLL II VCO from running to the wrong side of the frequency conversion in the mixing process, which could cause failure or the loop to falsely lock up.

For example, assume that the PLL II output is at 74 MHz and the VCO output is at 70.455 MHz (the highest frequency it would normally operate at). The IF frequency produced at the A6A3U1 mixer output would then be  $(74 - 70.455) \text{ MHz} = 3.545 \text{ MHz}$ , which is in the normal PLL IF range.

Assume that the VCO exceeds its upper frequency bound, and is now at 77.545 MHz. The IF output at A6A3U1 would again be 3.545 MHz ( $77.545 \text{ MHz} - 74 \text{ MHz} = 3.545 \text{ MHz}$ ), and the Phase Comparator would lock, holding the VCO at the wrong frequency.

The potential problem is eliminated by forcing the A6A2 VCO to track the A7 PLL II VCO. The PLL II VCO does not have a mixer in its feedback path, and therefore does not have this problem. It does, however, contain a VCO circuit which is almost identical to the A6A2 VCO (with respect to control voltage levels and operational frequency). When the PLL I VCO control voltage changes from 3.5 to 19.0 Vdc, its frequency changes from 40.455 MHz to 70.455 MHz. When the PLL II VCO control voltage changes from 3.5 to 19.0 Vdc, its frequency changes from 44.1 to 74 MHz. Furthermore, whenever the PLL II control voltage and VCO frequency change, the PLL I control voltage and VCO frequency will always change by almost the same amount.

Knowing that the VCO control voltage levels of both VCOs should always be approximately the same, we could monitor both and know if the PLL I VCO frequency is incorrect, since if it is it would have a different control voltage level than the PLL II VCO.

The A6A1 Tracking Reference/Clamp circuit does this monitoring function, as well as forcing the PLL I VCO back to the correct control voltage range, if necessary. The PLL II tracking reference signal at A6A1P2 is the actual value of the instantaneous A7 control voltage and is applied to the input of the circuit. The clamp's output is PLL I VCO control voltage at the PLL I VCO input. So long as the two control voltages remain within approximately  $\pm 1.5$  Vdc of each other (due to the diode drops of CR1, CR2, and Q1 or CR3, CR4, and Q2), Q1 and Q2 are nonconducting, and the PLL I control voltage is in an acceptable range of  $\pm 1.5$  Vdc from the PLL II control voltage.

Assume that the PLL I control voltage took off, driving the VCO higher in frequency. As soon as the control voltage level exceeded the PLL II control voltage plus 1.5 Vdc, Q2 turns on, forcing the PLL I control voltage to stop. Simultaneously, the PLL I Phase Comparator would be reacting to this sudden increase in frequency and eventually would pull the control voltage back down to the correct level, at which time Q2 would turn off.

The Tracking Reference/Clamp circuit will act as a "quick reaction" method of holding the PLL I VCO to approximately the correct value until the Phase Comparator can react in the event of a VCO "run away" condition. (Note that Q1 would perform the controlling function if the PLL I control voltage dropped 1.5 Vdc below the PLL II control voltage.)

#### 4.3.1.2 2 MHz Switch Circuit

At receiver tune frequencies less than approximately 2 MHz, the VCO control voltage required to drive the VCO is so low that the charge pump circuit on Phase Comparator Assembly A6A4 enters a nonlinear region of operation in an attempt to produce it. In order to correct this (at frequencies less than 2 MHz), the PLL Frequency Synthesizer A7U2 on the PLL II assembly outputs a 5 Vdc level to A6A1P1. This level occurs at A6A2E3 and turns Q3 on. Q3, which is connected across the control voltage input at Q2's base reduces the control voltage level by switching R7 into the circuit. The net result is that the charge pump on the A6A4 assembly must now force its output to increase the dc level at E2 in order to produce the proper VCO control voltage level at TP1. In so doing, the charge pump pulls itself out of its nonlinear region. At tune frequencies greater than 2 MHz, Q3 is off, and the charge pump functions normally. Note that this same scheme is used on the A7 assembly.

#### 4.4 BITE Circuits

Lock detector A6A4Q4 on Phase Detector Assembly A6A4 monitors the status of the Phase Comparators outputs, A6A4U2 pins 2 and 13. If either output pulses low and remains low for a period exceeding the time constants of A6A4R10 and A6A4C4, A6A4Q4 turns on and outputs a 5 Vdc signal at (ultimately) connector A6A1J1, pin 5, Lock Detector Output. This immediately flags BITE monitoring circuits on Control Assembly A14 and a front panel fault light indicator will light.

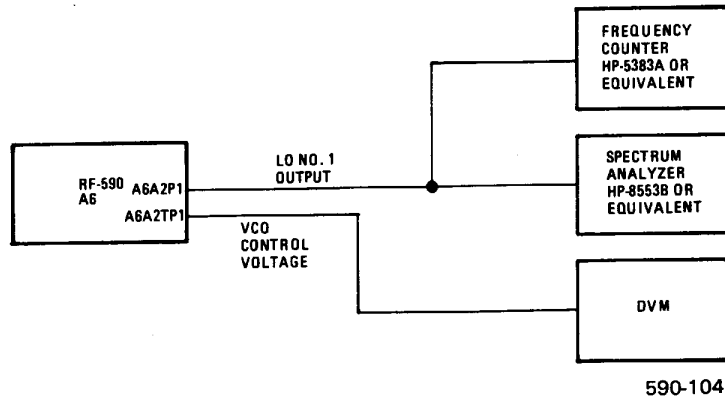
### 5. MAINTENANCE

The following adjustments should not be made as part of a routine maintenance procedure but rather only when a failure indicates a definite need. All tests are performed with all connections in normal contact, unless otherwise specified.

### 5.1 VCO Tracking Adjustment

Perform the following procedures to adjust the VCO.

- a. Connect equipment as shown in figure 1.



**Figure 1. VCO Adjustment**

- b. Set the RF-590 to 29.900000 MHz. Note the VCO control voltage level at A6A2TP1 (should be approximately 16 - 19.0 Vdc).
- c. Monitor the PLL II tracking reference from A7 to A6A1E2 with the DVM. The level should be the same as that noted in step b. If not, adjust PLL II Assembly A7C15 until the PLL II tracking reference is equal to the PLL I VCO control voltage at A6A2TP1.
- d. Tune the radio to each of the frequencies listed in table 2. At each frequency, the PLL II tracking reference and the PLL I VCO control voltage should agree within  $\pm 0.5$  Vdc. The LO no. 1 output should be 0 dBm  $\pm 3$  dB at the frequencies indicated.
- e. Check that the switch input at A6A1E1 does change to approximately  $4 \pm 0.5$  Vdc when the receiver is tuned below 2 MHz.

**Table 2. VCO Frequency Range**

Receiver Tune Frequency (MHz)	LO No. 1 Output Frequency (MHz)	Approximate PLL I VCO Control Voltage (Vdc)
29.900000	70.355000	17.75 $\pm$ 1.25
20.000000	60.455000	12.5 $\pm$ 1.0
10.000000	50.455000	7.5 $\pm$ 1.0
0.000000	40.455000	3.0 $\pm$ 1.0

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- f. Fully reconnect the A6 assembly to the RF-590 and initiate BITE self-test. The Receiver should not fail at any test concerning the A6 assembly. The test is now complete.

Tables 3 through 7 and figures 2 through 9 are the A6 assembly parts lists, component location drawings, and schematics.

**Table 3. PLL I Assembly Maintenance Parts List (PL 10073-4100-01)**

Ref. Desig.	Part Number	Description
A6	10073-7089	CABLE, COAX ASSY
A6A1	10073-4100-01	PLL1 ASSEMBLY
A6A2	10073-4110	PWB ASSY, PLL 1 MOTHER BD
A6A3	10073-4120-01	PWB ASSY, VCO
A6A4	10073-4130	PWB ASSY, MIXER
	10073-4160-01	PWB ASSY, PHASE DETECTOR

**Table 4. PLL I Assembly A6A1 Maintenance Parts List (PL 10073-4110)**

Ref. Desig.	Part Number	Description
	10073-4110	PWB, PLL 1 MOTHER BD
	J46-0003-001	HEADER, 1 PIN
	10073-7088	CABLE, COAX ASSY
	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	C26-0025-100	CAP 10UF 20% 25V TANT
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/01-1535	CAP .01UF 20% 100V CER
C8	M39014/01-1535	CAP .01UF 20% 100V CER
C9	M39014/01-1535	CAP .01UF 20% 100V CER
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/01-1535	CAP .01UF 20% 100V CER
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/01-1535	CAP .01UF 20% 100V CER
C15	CM04ED390J03	CAP 39PF 5% 500V MICA
C16	M39014/01-1535	CAP .01UF 20% 100V CER
C17	M39014/01-1535	CAP .01UF 20% 100V CER
C20	M39014/02-1310	CAP .1UF 10% 100V CER-R
C21	C26-0025-100	CAP 10UF 20% 25V TANT
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	C26-0016-151	CAP 150UF 20% 16V TANT
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R

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Table 4. PLL I Assembly A6A1 Maintenance Parts List (PL 10073-4110) (Cont.)

Ref. Desig.	Part Number	Description
C27	C26-0035-100	CAP 10UF 20% 35V TANT
C28	10073-7035	CAP,FEED-THRU 100
C29	10073-7035	CAP,FEED-THRU 100
C30	10073-7035	CAP,FEED-THRU 100
C31	10073-7035	CAP,FEED-THRU 100
CR1	1N3064	DIODE 75mA 75V SW
CR2	1N3064	DIODE 75mA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
J1	J46-0032-006	HDR 6 PIN 0.100" SR
L1	L08-0001-001	CHOKE W B 50 MHZ
L2	L08-0001-001	CHOKE W B 50 MHZ
L3	MS14046-9	COIL 27UH 10% FXD RF
Q1	2N2222	XSTR SS/GP NPN TO-18
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	Q35-0003-000	XSTR U310 JFET HIGH GM
Q4	2N5109	XSTR RFPWR NPN TO-39
R1	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R2	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R3	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R4	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R5	R65-0003-221	RES 220 5% 1/4W CAR FILM
R6	R65-0003-221	RES 220 5% 1/4W CAR FILM
R7	R65-0003-101	RES 100 5% 1/4W CAR FILM
R8	R65-0003-101	RES 100 5% 1/4W CAR FILM
R9	R65-0003-151	RES 150 5% 1/4W CAR FILM
R10	R65-0003-470	RES 47 5% 1/4W CAR FILM
R11	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R12	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R13	R65-0003-101	RES 100 5% 1/4W CAR FILM
R14	R65-0003-121	RES 120 5% 1/4W CAR FILM
R15	R65-0003-100	RES 10 5% 1/4W CAR FILM
R16	R65-0003-471	RES 470 5% 1/4W CAR FILM
T1	10073-7014	TRANSFORMER, RF, FIXED
T2	10073-7014	TRANSFORMER, RF, FIXED
VR1	I11-0001-001	IC VR 7805 + 5V 1.5A 4%
VR2	1N4737	DIODE 7.5V 10% 1W ZENER

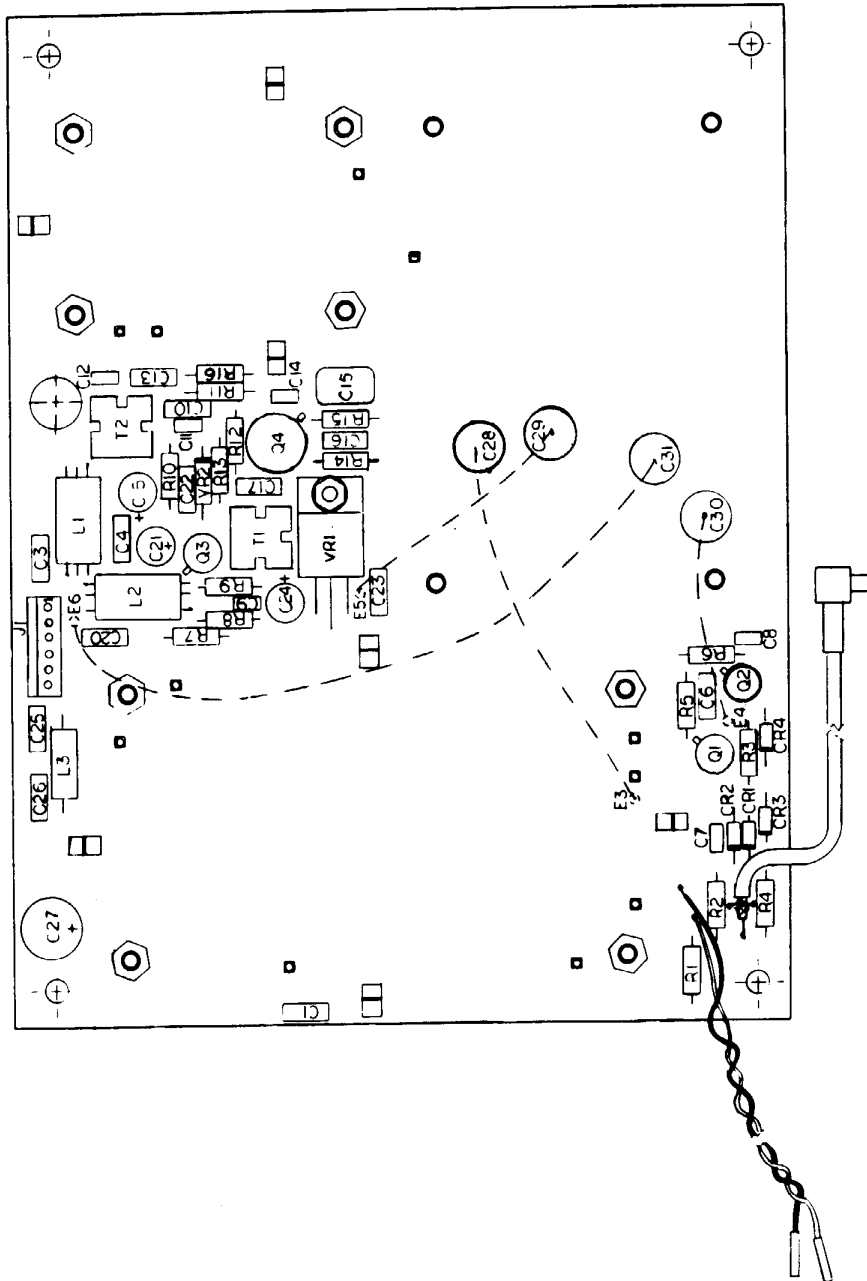


Figure 2. PLL I Assembly A6 and PLL I Motherboard Assembly A6A1  
Component Location Diagram (PL 10073-4110, Rev. C)

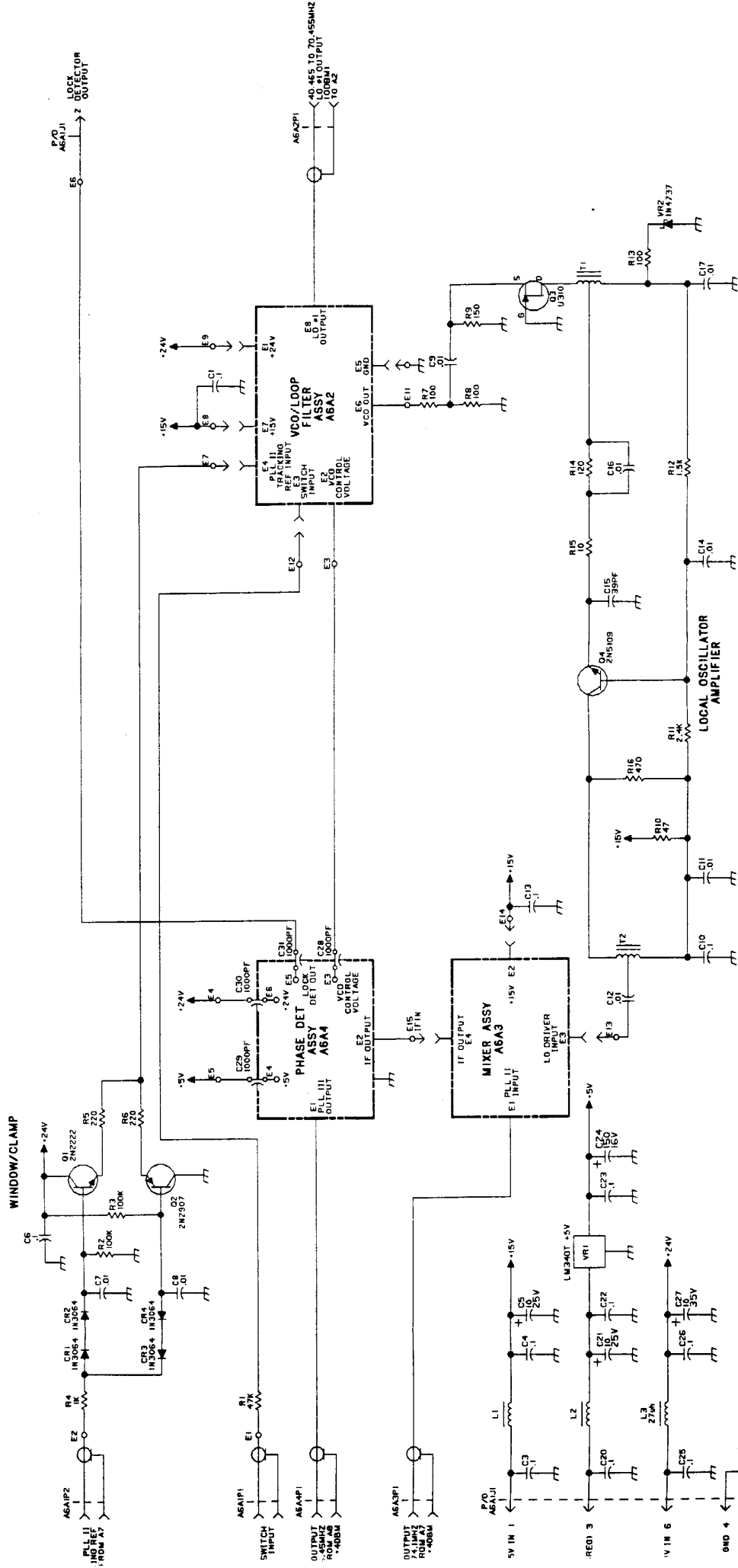
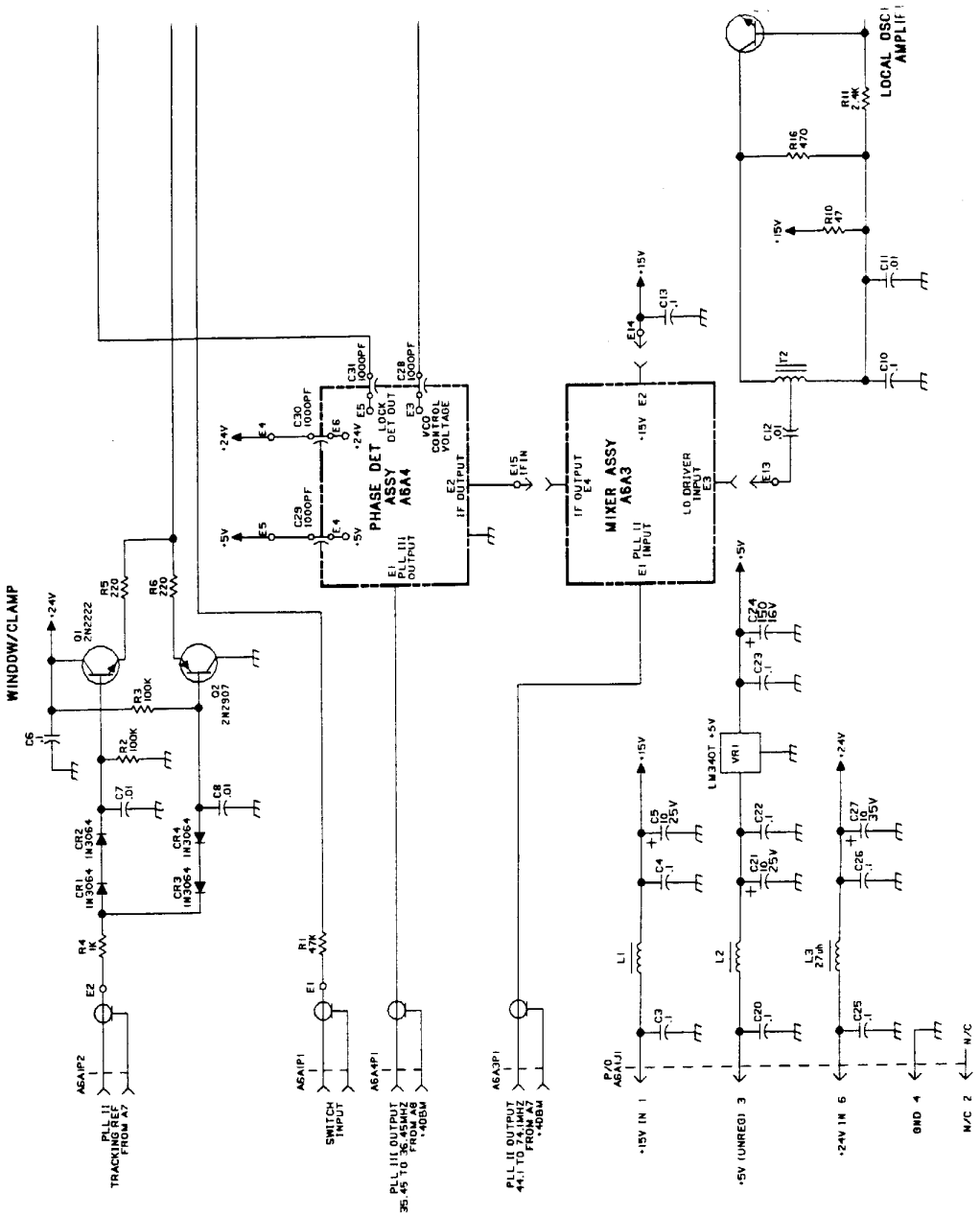


Figure 3. PLL I Assembly A6 and PLL I Mother Board Assembly A6A1 Schematic Diagram (10073-4111, Rev. E)



NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.



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**Table 5. VCO Board A6A2 Parts List (PL 10073-4120-01)**

Ref. Desig.	Part Number	Description
	10073-4120-01	PWB, VCO
	10073-7089	CABLE, COAX ASSY
C1	C26-0025-100	CAP 10UF 20% 25V TANT
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	C26-0025-100	CAP 10UF 20% 25V TANT
C6	CK05BX102M	CAP 1000PF 20% 200V CER
C7	C26-0025-339	CAP 3.3UF 20% 25V TANT
C8	CK05BX103M	CAP .01UF 20% 100V CER
C9	C66-0050-102	CAP 1000PF 5% 50V FILM
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	C26-0035-100	CAP 10UF 20% 35V TANT
C13	CK05BX102M	CAP 1000PF 20% 200V CER
C14	C26-0035-229	CAP 2.2UF 20% 35V TANT
C15	C-2496	CAP 470PF 2% 500V MICA
C16	C-2495	CAP 430PF 2% 500V MICA
C17	C-2501	CAP 680PF 2% 300V MICA
C18	C66-0050-152	CAP 1500PF 5% 50V FILM
C19	C66-0050-122	CAP 1200PF 5% 50V FILM
C20	C66-0050-182	CAP 1800PF 5% 50V FILM
C21	C66-0050-122	CAP 1200PF 5% 50V FILM
C22	C66-0050-102	CAP 1000PF 5% 50V FILM
C23	C-2501	CAP 680PF 2% 300V MICA
C24	C-2503	CAP 820PF 2% 300V MICA
C25	C66-0050-102	CAP 1000PF 5% 50V FILM
C26	CK05BX103M	CAP .01UF 20% 100V CER
C27	CK05BX103M	CAP .01UF 20% 100V CER
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	CK05BX102M	CAP 1000PF 20% 200V CER
CR1	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR2	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR3	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR4	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR5	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR6	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR7	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR8	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR9	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR10	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR11	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR12	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR13	D25-0002-001	VARACTOR 26.0 - 32.0pF
CR14	D25-0002-001	VARACTOR 26.0 - 32.0pF

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**Table 5. VCO Board A6A2 Parts List (PL 10073-4120-01) (Cont.)**

Ref. Desig.	Part Number	Description
CR15	1N6263	DIODE .40W 60V HOT CARR
E1	J42-0008-001	CONTACT, SOCKET
E2	J42-0008-001	CONTACT, SOCKET
E3	J42-0008-001	CONTACT, SOCKET
E4	J42-0008-001	CONTACT, SOCKET
E5	J42-0008-001	CONTACT, SOCKET
E6	J42-0008-001	CONTACT, SOCKET
E7	J42-0008-001	CONTACT, SOCKET
E8	E36-0026-001	TERM TUR BRS .178L
E9	E36-0026-001	TERM TUR BRS .178L
E10	E36-0026-001	TERM TUR BRS .178L
E11	E36-0026-001	TERM TUR BRS .178L
JMP1	MP-1142	CIRCUIT JUMPER
L1	MS75084-11	COIL 8.2UH 10% FXD RF
L2	10073-7042	INDUCTOR, 2.4MH
L3	10073-7042	INDUCTOR, 2.4MH
L4	10073-7042	INDUCTOR, 2.4MH
Q1	Q35-0003-000	XSTR U310 JFET HIGH GM
Q2	2N5088	XSTR SS/GP
Q3	2N2222	XSTR SS/GP NPN TO-18
Q4	Q35-0003-000	XSTR U310 JFET HIGH GM
R1	R65-0003-101	RES 100 5% 1/4W CAR FILM
R2	R65-0003-470	RES 47 5% 1/4W CAR FILM
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R5	R65-0003-101	RES 100 5% 1/4W CAR FILM
R6	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R7	R65-0003-683	RES 68K 5% 1/4W CAR FILM
R8	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R9	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R10	RN55D4641F	RES,4640 1% 1/8W MET FLM
R11	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R12	RN55D4750F	RES,475.0 1% 1/8W MET FLM
R13	R65-0003-270	RES 27 5% 1/4W CAR FILM
R14	R65-0003-151	RES 150 5% 1/4W CAR FILM
R15	R65-0003-101	RES 100 5% 1/4W CAR FILM
T1	10073-7002	TRANSFORMER, RF, FIXED
T2	10073-7014	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
VR1	I12-0006-012	IC VR 78L12A + 12V .10A 4%

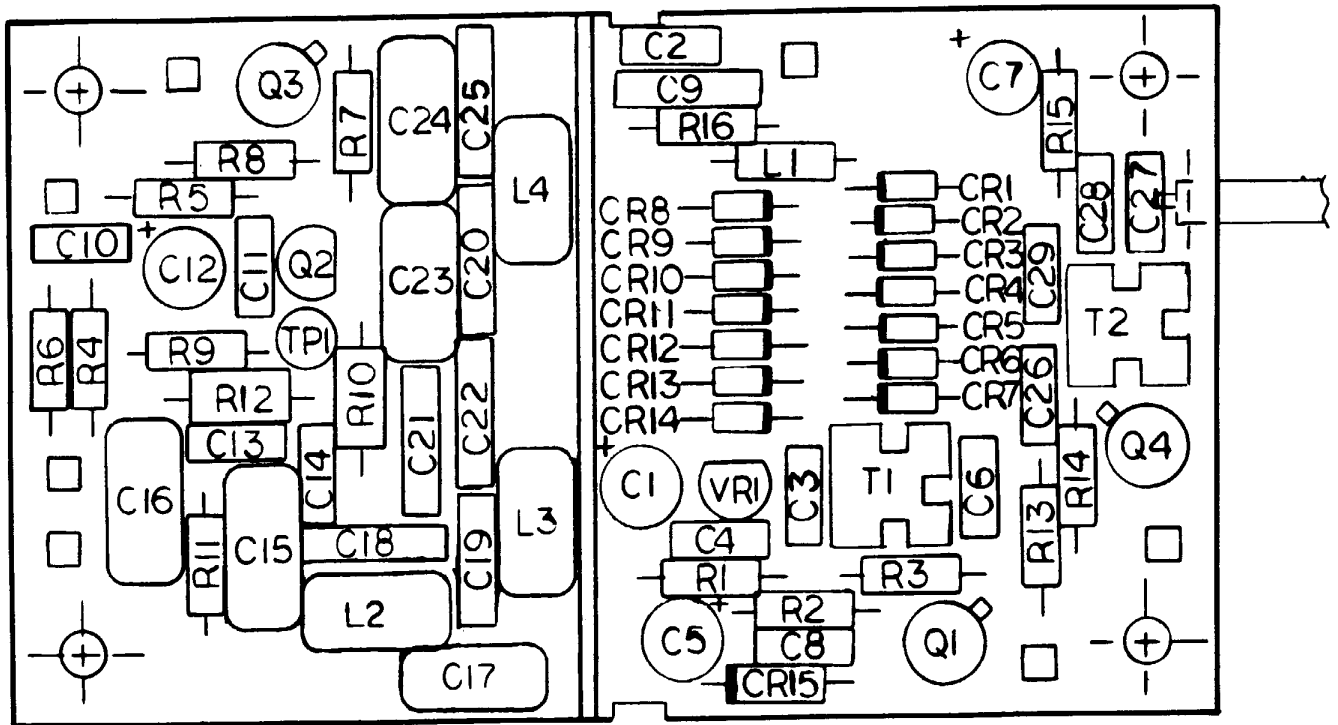


Figure 4. VCO Board A6A2 Component Location Diagram (10073-4120-01, Rev. G)

- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR A COMPLETE DESIGNATION, PRECEDED WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. CR1-CR14 ARE KV3901.
  5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  6. ON 10073-4120-02 ASSYS: R12 = RN5508250F, C14 = CK08BX474M
  7. L5 MAY BE REQUIRED ON SOME ASSYS TO OBTAIN THE DESIRED CONTROL VOLTAGE RANGE AND TRACKING.

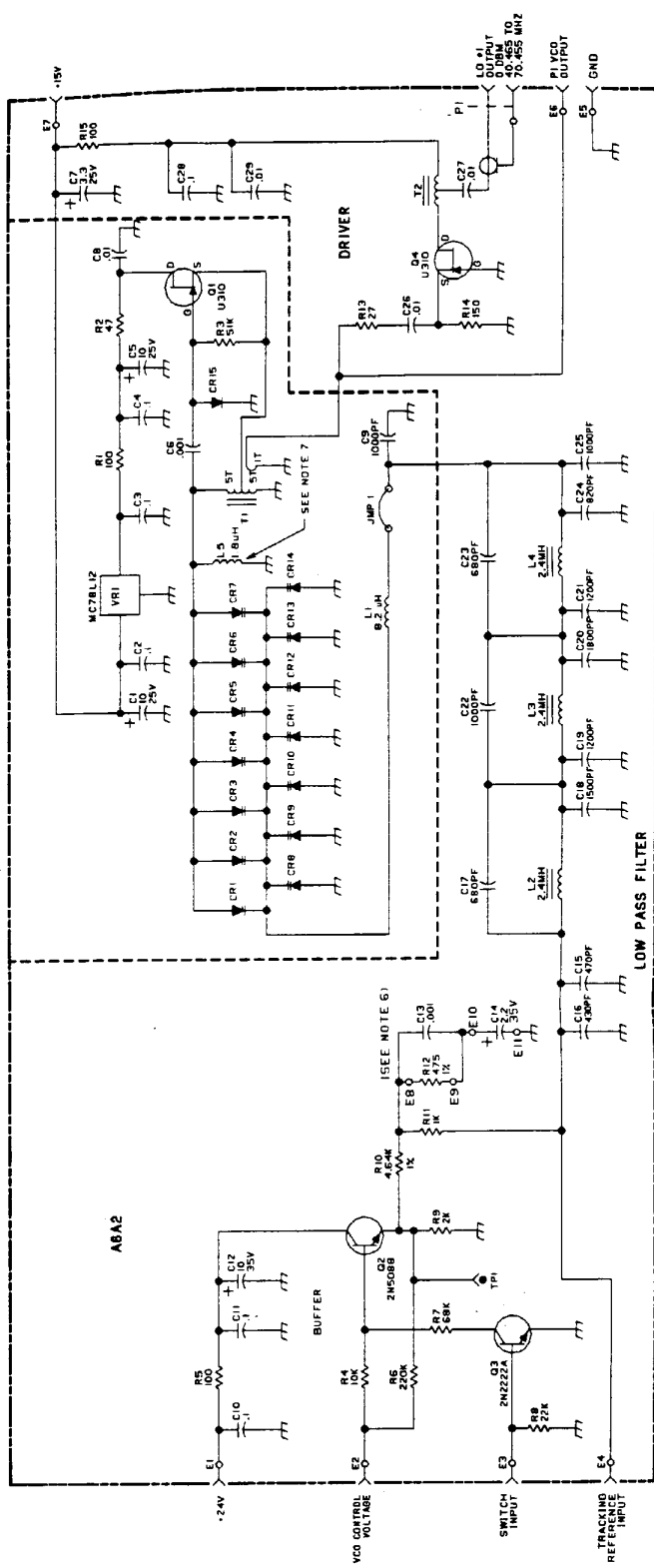


Figure 5. VCO Board A6A2 Schematic Diagram (10073-4121, Rev. H)

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**Table 6. Mixer Board A6A3 Maintenance Parts List (PL 10073-4130)**

Ref. Desig.	Part Number	Description
	10073-4130	PWB, MIXER
	10073-7087	CABLE, COAX ASSY
	E70-0002-005	PAD MNT XSTR TO-18
C1	CM04FD151J03	CAP 150PF 5% 500V MICA
C2	CM04FD151J03	CAP 150PF 5% 500V MICA
C3	CM04ED330J03	CAP 33PF 5% 500V MICA
C4	CM04FC271J03	CAP 270PF 5% 300V MICA
C5	CM04FC301J03	CAP 300PF 5% 300V MICA
C6	CM04FD151J03	CAP 150PF 5% 500V MICA
C7	CM04FC271J03	CAP 270PF 5% 300V MICA
C8	CM04FC271J03	CAP 270PF 5% 300V MICA
C9	CM04FD121J03	CAP 120PF 5% 500V MICA
C10	CM04FD111J03	CAP 110PF 5% 500V MICA
C11	CM04FD121J03	CAP 120PF 5% 500V MICA
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
L1	MS18130-9	COIL 1.2UH 10% FXD RF
L2	MS18130-9	COIL 1.2UH 10% FXD RF
L3	MS18130-8	COIL 1.0UH 10% FXD RF
L4	MS75085-7	COIL 100UH 10% FXD RF
Q1	2N2369	XSTR 5S/RF NPN
R1	R65-0002-101	RES 100 5% 1/8W CAR FILM
R2	R65-0002-750	RES 75 5% 1/8W CAR FILM
R3	R65-0002-101	RES 100 5% 1/8W CAR FILM
R4	R65-0002-151	RES 150 5% 1/8W CAR FILM
R5	R65-0002-390	RES 39 5% 1/8W CAR FILM
R6	R65-0002-151	RES 150 5% 1/8W CAR FILM
R7	R65-0002-560	RES 56 5% 1/8W CAR FILM
R8	R65-0002-103	RES 10K 5% 1/8W CAR FILM
R9	R65-0002-201	RES 200 5% 1/8W CAR FILM
R10	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R11	R65-0002-100	RES 10 5% 1/8W CAR FILM
R12	R65-0002-471	RES 470 5% 1/8W CAR FILM
U1	I51-0003-003	MIXER DB 50mW 500MHZ

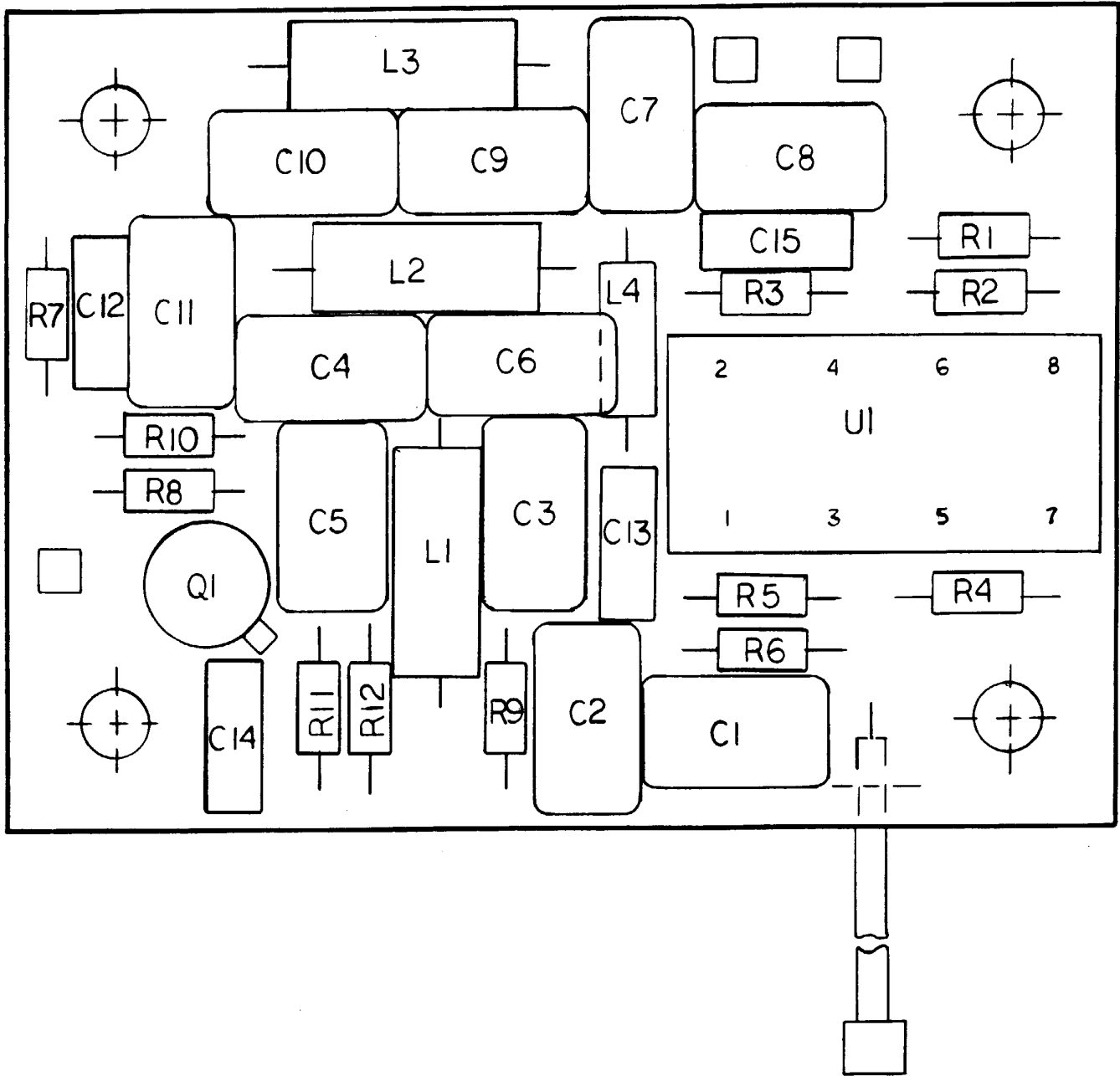


Figure 6. Mixer Board A6A3 Component Location Diagram (10073-4130, Rev. B)

Table 7. Phase Detector Board Maintenance Parts List (PL 10073-4160)

Ref. Desig.	Part Number	Description
	10073-4160-01	PWB, PHASE DETECTOR
	E70-0002-002	PAD MNT XSTR TO-5
C1	CM04ED330J03	CAP 33PF 5% 500V MICA
C2	CM04ED270J03	CAP 27PF 5% 500V MICA
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	C26-0035-109	CAP 1.0UF 20% 35V TANT
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/01-1535	CAP .01UF 20% 100V CER
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	C25-0003-411	CAP 150UF 10% 15V TANT
C16	C26-0025-100	CAP 10UF 20% 25V TANT
C17	C26-0035-100	CAP 10UF 20% 35V TANT
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	C26-0035-220	CAP 22UF 20% 35V TANT
C20	M39014/02-1310	CAP .1UF 10% 100V CER-R
C21	C26-0035-229	CAP 2.2UF 20% 35V TANT
C22	CM04ED200J03	CAP 20 PF 5% 500 V MICA
CR1	1N3064	DIODE 75mA 75V SW
CR2	1N3064	DIODE 75mA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
L1	L08-0001-001	CHOKE W B 50 MHZ
L2	MS75084-14	COIL 15.0UH 10% FXD RF
Q1	2N3866	XSTR SS/RF NPN TO-39
Q2	2N3866	XSTR SS/RF NPN TO-39
Q3	2N5160	XSTR RFPWR PNP
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	Q-0153	XSTR SS/RF PNP
Q6	2N2369	XSTR SS/RF NPN
R1	R65-0003-680	RES 68 5% 1/4W CAR FILM
R2	RN55D4990F	RES,499.0 1% 1/8W MET FLM
R3	RN55D2002F	RES,20.0K 1% 1/8W MET FLM
R4	RN55D4990F	RES,499.0 1% 1/8W MET FLM
R5	R65-0002-332	RES 3.3K 5% 1/8W CAR FILM
R6	RN55D1821F	RES,1820 1% 1/8W MET FLM



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**Table 7. Phase Detector Board Maintenance Parts List (PL 10073-4160-01) (Cont.)**

Ref. Desig.	Part Number	Description
R7	R65-0002-332	RES 3.3K 5% 1/8W CAR FILM
R8	RN55D4990F	RES,499.0 1% 1/8W MET FLM
R9	R65-0002-221	RES 220 5% 1/8W CAR FILM
R10	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R11	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R12	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R13	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R14	R65-0002-391	RES 390 5% 1/8W CAR FILM
R15	R65-0003-241	RES 240 5% 1/4W CAR FILM
R16	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R17	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R18	R65-0002-270	RES 27 5% 1/8W CAR FILM
R19	R65-0003-331	RES 330 5% 1/4W CAR FILM
R20	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R21	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R22	R65-0002-101	RES 100 5% 1/8W CAR FILM
R23	RN55D4990F	RES,499.0 1% 1/8W MET FLM
U1	I65-0004-001	IC 12013 PLASTIC ECL
U2	IC-0430	IC MC4044 CERAMIC CMOS
U3	I05-0000-090	IC 74LS90 PLASTIC TTL
U4	I05-0000-090	IC 74LS90 PLASTIC TTL



NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/BW, 15%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

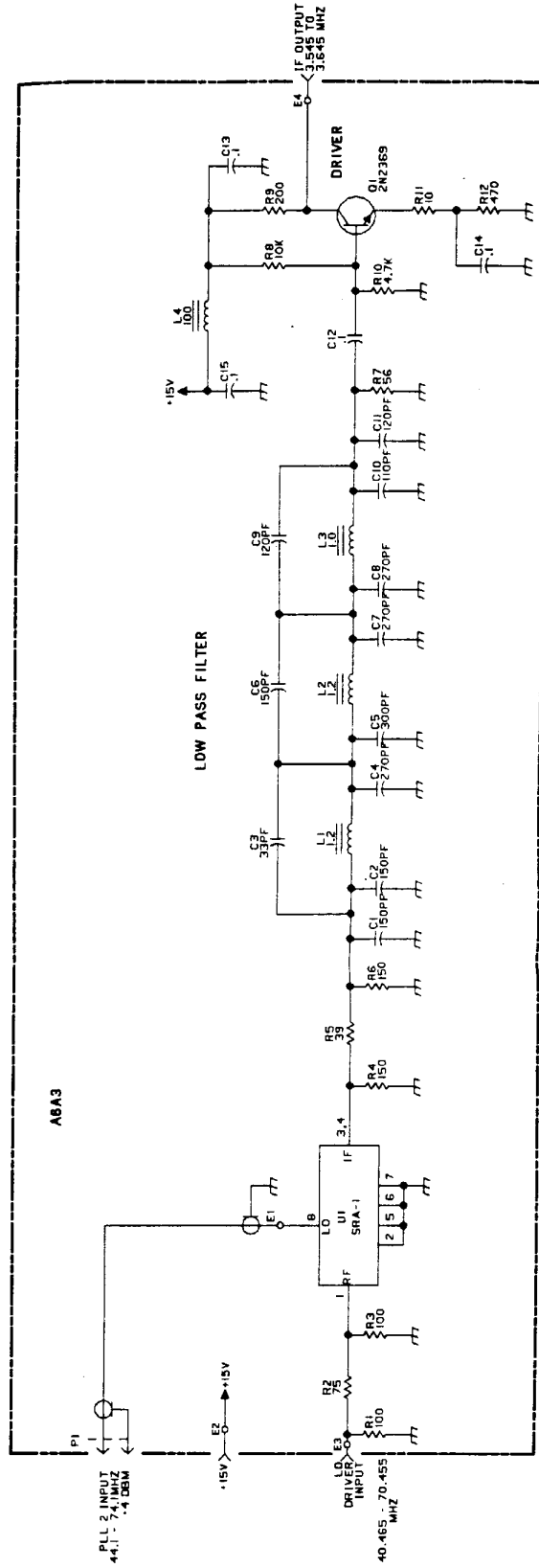
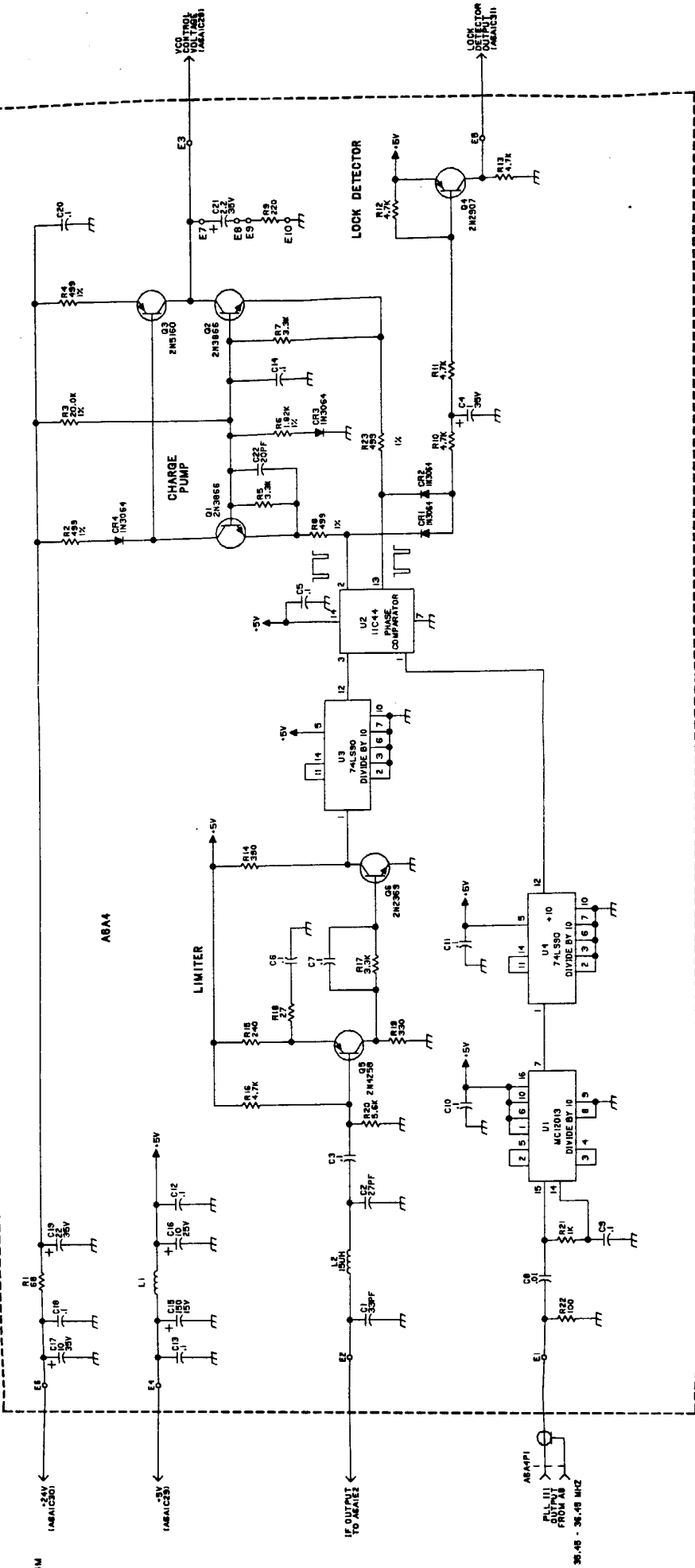


Figure 7. Mixer Board A6A3 Schematic Diagram (10073-4131, Rev. C)



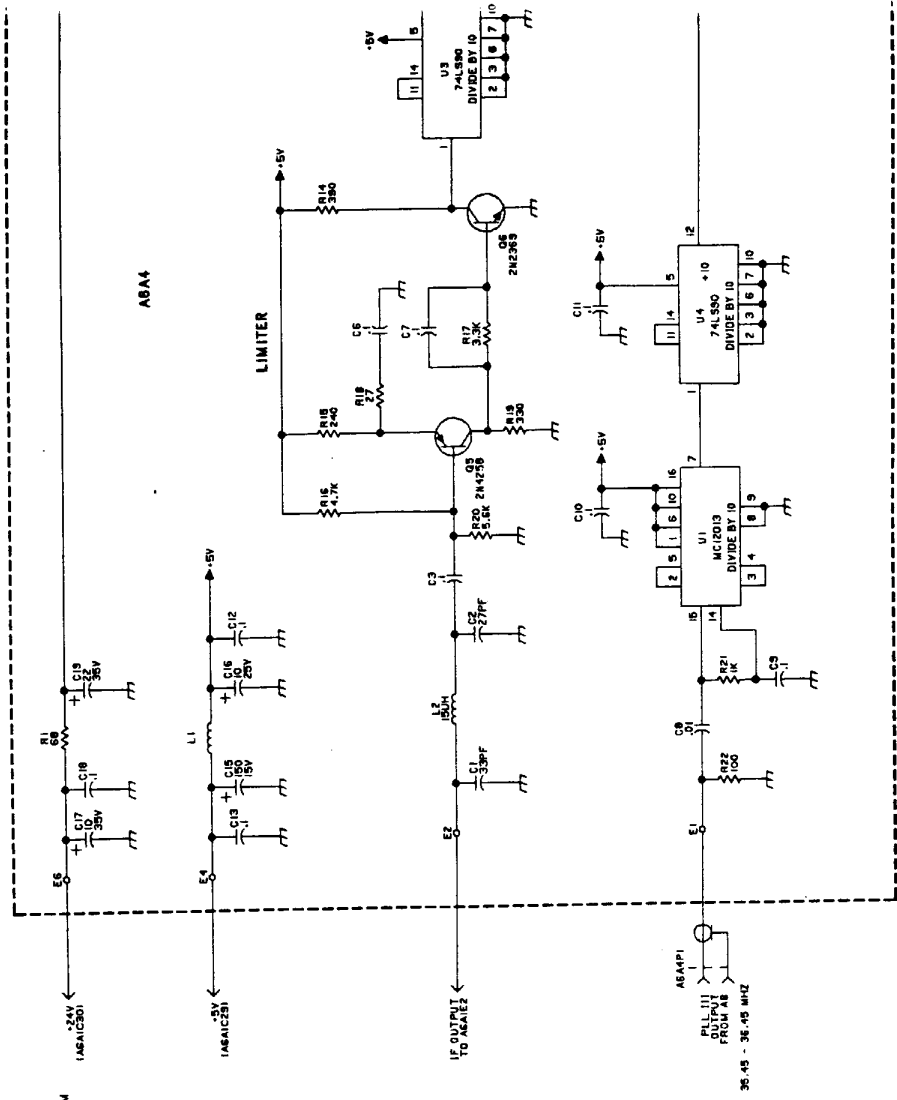
ONLY  
ITS LIST.  
= CK068X74M

IF OUTPUT  
TO AMATEZ

ASAPFI  
OUTPUT  
FROM A6  
36.49 - 36.49 MHz

Figure 9. Phase Detector Board A6A4 Schematic  
Diagram (10073.4161, Rev. E)

- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 5%.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  5. ON 10073-4160-02 ASSYS: R9 = R65-0002-511; C21 = CK06B474M



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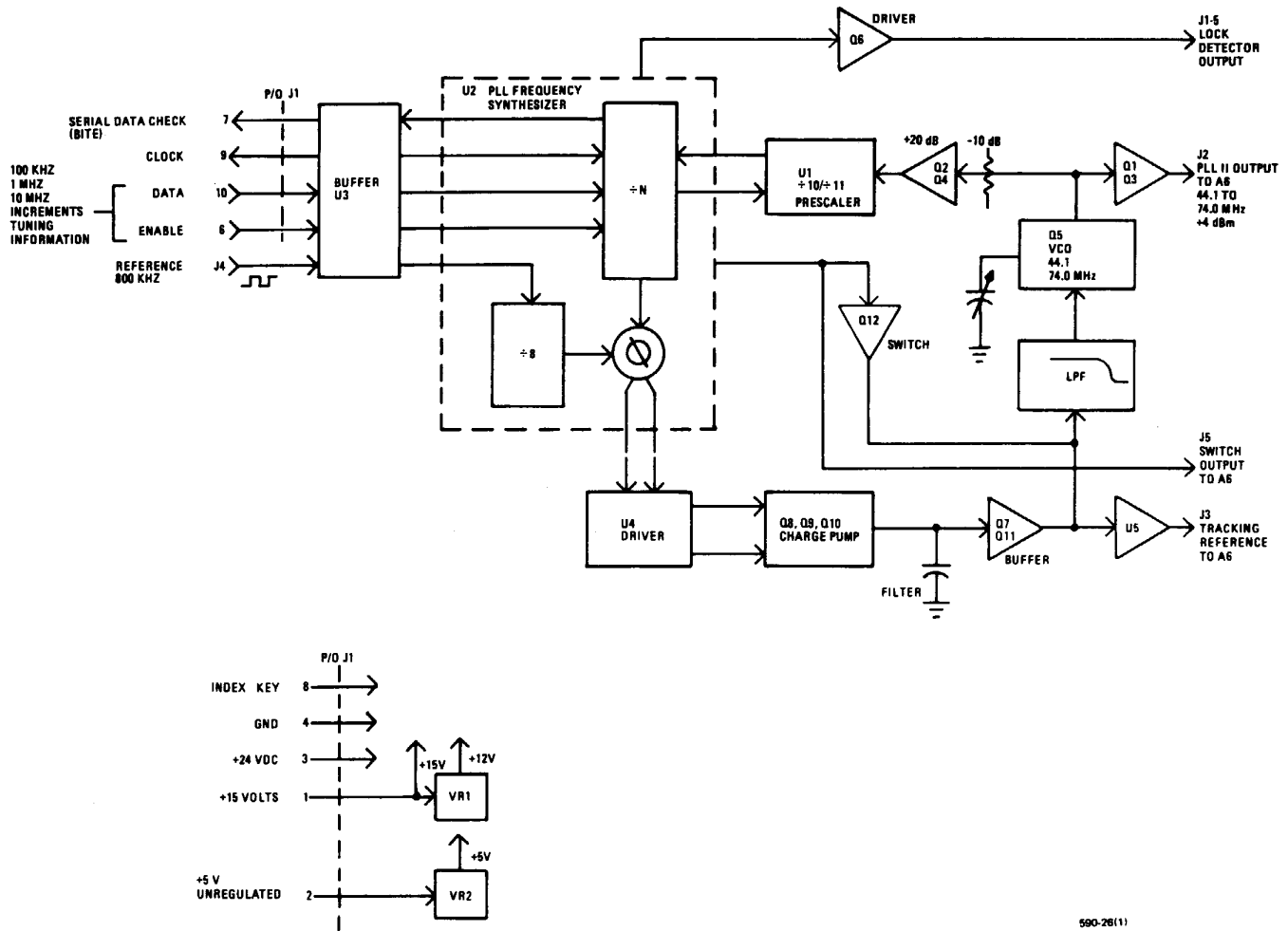
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590-26(11)

**PLL II Assembly A7 Functional Block Diagram**

## 1. GENERAL DESCRIPTION

PLL II Assembly A7 is a single phase locked loop synthesizer that ultimately provides the 100 kHz, 1 MHz, and 10 MHz tuning increments selected at the RF-590 front panel frequency selection controls.

Frequency select input data is applied to the assembly in serial data form under Control Board Assembly A14 microprocessor control. The A7 output to PLL I Assembly A6 is a variable 44.1 to 74.0 MHz signal in 100 kHz controllable steps. The net results of A7 operation (after further translation in the synthesizer chain) provide the course tuning increments (100 kHz, 1 MHz, and 10 MHz) for LO No. 1 output.

## 2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

**Table 1. PLL II Assembly Interface Connections**

Connector	Function	Characteristics
J1-1	+15 Volts	Approximately 25 mA
J1-2	5 Volts Unregulated	Approximately 240 mA
J1-3	+24 Volts	Approximately 20 mA
J1-4	Ground	
J1-5	Lock Detector Output	5 Vdc = unlocked; 0 Vdc = locked
J1-6	Enable	+ going pulse = Enabled
J1-7	Serial Data Check	P/O BITE Test, +5 Vdc = ok
J1-8	Key	
J1-9	Clock	TTL, 750 kHz
J1-10	Data	Serial TTL
J2	PLL II (A7) Output	+4 dBm/50 ohms, 44.1 to 74.0 MHz
J3	PLL II Tracking Reference	3.5 to 19 Vdc
J4	800 kHz Reference Input	TTL
J5	Switch Output	+4 V for < 2 MHz tune frequency 0 V for ≥ 2 MHz tune frequency



### 3. CIRCUIT DESCRIPTION

#### NOTE

A7 operation is similar (in operation) to that of the general  $\div N$  PLL and charge pump circuits described in section 4. A review of section 4 at this point would aid in the understanding of A7 operation.

#### 3.1 Reference Generation

The 800 kHz from Reference Generator Assembly A12 enters PLL II Assembly A7 at J4. This signal is applied via buffer U3 to a divide by 8 counter internal to U2 to produce a 100 kHz reference signal. Since this has been derived ultimately from the RF-590 crystal frequency standard via the A12 assembly, stable and accurate A7 operation is assured.

#### 3.2 Divide By N Counter

Since the A7 assembly requires a variable 44.1 to 74.0 MHz output frequency, a programmable counter has been designed into the VCO feedback path to the phase comparator. This counter consists of dual modulus  $\div 10$  prescaler U1 and a programmable counter internal to U2. Together U1 and the programmable portion of U2 create a total division range of  $N = 441$  to  $N = 740$ , where  $N$  is a function of the values of the receiver 10 MHz, 1 MHz, and 100 kHz tuning positions.

The output of the divide by  $N$  counter will always attempt to equal the 100 kHz reference frequency at the Phase Comparator inputs, despite changes in the divide by  $N$  factor due to changing the 10 MHz, 1 MHz, and/or 100 kHz receiver tuning increments. The VCO frequency will change to accomplish this, in response to command signals generated by the Phase Comparator. The VCO frequency will always equal  $(N)$  (Reference frequency), or  $(N)$  (100 kHz) = 44.1 MHz to 74.0 MHz. The exact value of  $N$  is determined by the 10 MHz, 1 MHz, and/or 100 kHz receiver tuning positions. This front panel selection causes Control Assembly A14 to generate a serial data code containing information pertaining to the values of the increments chosen. This code is applied synchronously with the 750 kHz system clock to U2 whenever the U2 enable line is gated open by A14. In general,  $N = (441 + XXX)$ , where  $XXX$  is the value of the 10 MHz, 1 MHz, and 100 kHz positions chosen at the receiver front panel frequency controls.

For example, tuning the RF-590 to 15.789000 MHz would make  $N = (441 + 157) = 598$ . The VCO frequency will be  $(N)$  (Reference) =  $(598)$  (100 kHz) = 59.8 MHz.

Tuning the radio to 24.705000 MHz would result in a VCO output frequency of  $(441 + 247)$  (100 kHz) = 68.8 MHz. Note that increasing the receiver tune frequency caused an increase in the A7 output frequency. The opposite will also be true.

### 3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 100 kHz reference and the 100 kHz divide by N counter's VCO derived signal is accomplished by a phase comparator internal to U2. When these two signals are equal in frequency and phase, the buffered Phase Comparator outputs at TP2 and TP3 are essentially 5 Vdc. This 5 volt level holds the charge pump transistors Q9, Q10, and consequently, Q8 off. The voltage across C51 will be at some constant value forcing buffers Q7 and Q11 to develop a constant voltage at TP1. This VCO control voltage holds the VCO frequency constant (somewhere between 44.1 MHz and 74.0 MHz).

Assume that the VCO feedback signal at the divide by N counter output is suddenly less than the reference frequency, which is what happens at the instant the divide by N factor is increased. Since the two Phase Comparator inputs are no longer equal, the Phase Comparator will output a series of negative pulses at TP3. (The pulse width of these pulses is a function of the difference in phase/frequency between the two inputs.) Q10 turns on, and its decreasing collector voltage turns Q8 on. Q8 will start to pump charge into C51, raising its voltage. Buffer stage Q7 and Q11 will produce a corresponding increase at TP1 which forces the VCO to increase in frequency. The increasing VCO signal produces a corresponding frequency increase at the divide by N counter output, driving it towards the reference signal at 100 kHz. As the divide by N counter output approaches the reference frequency, the pulses at TP3 get narrower, until they are at an essentially constant +5 Vdc level. Q10 and Q8 turn off, the voltage rise across C51 stops at a new higher level producing a stabilization of the VCO control voltage and the VCO frequency at a new higher value.

Assume that the VCO feedback signal is suddenly greater than the reference frequency, which is what occurs at the instant the divide by N factor is decreased. The Phase Comparator outputs a series of negative pulses at TP2. Q9 turns on, and starts drawing charge out of C51, dropping its voltage. A corresponding decrease in the VCO control voltage occurs, producing a decreasing VCO frequency. This causes the fed back VCO divide by N counter output to decrease, driving it towards the 100 kHz reference. As the divide by N counter output approaches the reference, the negative pulses at TP2 become narrower, until they are essentially at a 5 Vdc level. Q9 turns off, and stops any further decrease in the C51 voltage, the VCO control voltage, and therefore the VCO frequency. The VCO now rests at a new, lower frequency.

Note that the VCO control voltage at Q7 and Q11 is sent to two places. They are the LPF and VCO on the A7 assembly, and the buffer stage, U5. This second output is referred to as the Tracking Reference, and is routed through J3 for use on PLL I Assembly A6. It allows the A6 VCO to properly track the A7 VCO.

### 3.4 VCO Operation and Control

A charge pump circuit consisting of Q8-Q10 and associated components converts the two Phase Comparator pulse outputs into an analog dc control voltage. Buffer stages Q7 and Q11 apply the VCO control voltage through a low pass filter (LPF) network to the varactor diode string in the VCO. The VCO itself is a JFET (Q5) Hartley oscillator stage whose frequency shifts as the capacitance of the varactor diodes change in response to changes in VCO control voltage. A VCO control voltage range of approximately 3.5 Vdc to 17.5 Vdc shifts the VCO from 44.1 MHz to 74.0 MHz.

The VCO output is fed to two separate amplifier stages. The first, Q4 and Q2, is a 20 dB amplifier which applies the VCO signal to the  $\div 10/\div 11$  prescaler, U1. It is this signal which completes the feedback loop to the phase comparator. The second amplifier stage, Q3 and Q1, boosts the level to approximately 4 dBm and is called the PLL II output. This signal contains the 10 MHz, 1 MHz, and 100 kHz tuning increments information, and is fed to PLL I Assembly A6 for further processing.

### 3.5 Noise Reduction Techniques

The noise characteristics of the VCO output are enhanced by the following two methods:

- Use of a sharp cut off LPF network to filter noise off the VCO control voltage. This stage is located between the charge pump buffer stage Q11 and the VCO input.
- Use of a circuit to linearize charge pump operation at receiver tune frequencies less than 2 MHz. Lower receiver tune frequencies require less VCO control voltage than higher receiver tune frequencies. At tune frequencies less than 2 MHz, the VCO control voltage required is so low that the charge pump enters a nonlinear mode of operation in an attempt to produce the output across C51 that is required. In order to correct this, at frequencies less than 2 MHz, U2 outputs a 5 Vdc level which turns Q12 on. Q12, which is connected across the LPF input, reduces the control voltage level. The net result is that the charge pump is now "tricked" into forcing its output to increase the voltage across C51 required to produce the required VCO control voltage. In so doing, it pulls itself out of its nonlinear region. At frequencies greater than 2 MHz, Q12 is off and the charge pump functions normally. Note that this switch output from U2 is routed through J5 to the A6 assembly for similar purposes.

### 3.6 BITE Circuits

The A7 assembly contains two circuits for self-test evaluation.

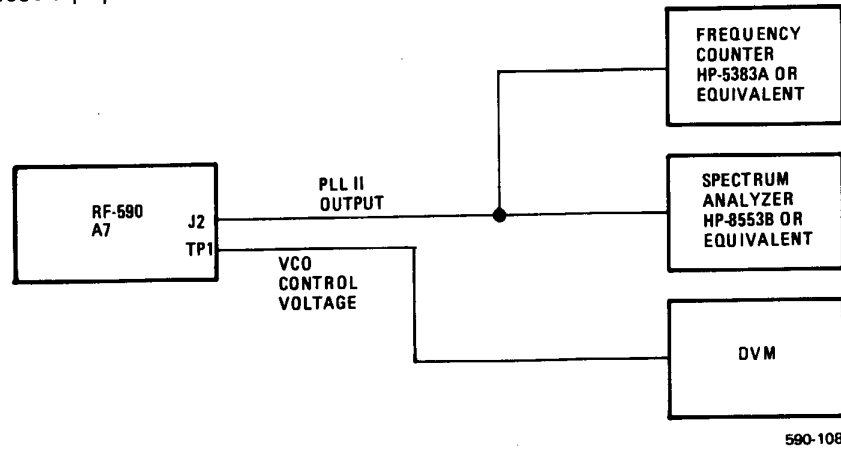
- Lock detector Q6 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by the A14 assembly. A front panel fault light will appear if the loop ever unlocks.
- Serial data check that verifies the tuning data from the A14 assembly has been received and properly translated into the correct divide by N factor. A serial data word is sent on the data line (J1 pin 10) and the U6 serial data check line is read back to the A14 assembly (J1 pin 7). If the word has been received and properly decoded, this line will pulse to +5 Vdc. The serial data check occurs automatically, but only when the receiver BITE self-test is actuated.

## 4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. All tests performed with all connections in normal contact, unless otherwise specified.

**4.1 VCO Frequency Adjustment**

- a. Connect equipment as shown in figure 1.



**Figure 1. VCO Adjustment**

- b. Set RF-590 frequency to 29.900000 MHz.
- c. Adjust C15 for 19.0 Vdc at TP1. PLL II output at J2 should be 74.0 MHz, 4 dBm  $\pm$ 3 dB. Check the receiver tune frequency against PLL II output frequencies listed in table 2. (Output should remain at +4 dBm  $\pm$ 3 dB).

**Table 2. VCO Frequency Range**

Receiver Tune Frequency, MHz	PLL II Output Frequency, MHz	Approximate TP1 Voltage, Vdc
29.900000	74.000000	19.0
15.000000	59.100000	10.0
00.000000	44.100000	3.5

- d. Check that the Tracking Reference Signal (J3) agrees within  $\pm .1$  Vdc to the control voltage at TP1 for the ranges listed in table 2.
- e. Check that the switch output (J5) changes to approximately 4 Vdc when the receiver is tuned below 2.000000 MHz.
- f. Fully reconnect the A7 assembly to the RF-590 and initiate BITE test. Receiver should not fail at any test concerning the A7 assembly. These tests have verified the proper operation of the A7 assembly. Proceed to paragraph 4.2, Tracking Adjustment.

**4.2 Tracking Adjustment**

- a. Perform VCO adjustment found in paragraph 4.1.
- b. Tune the RF-590 to 29.999999 MHz:
- c. Measure the VCO control voltage at TP1 on PLL I VCO Assembly A6A2. (Note that TP1 is located under the VCO assembly cover.) This voltage should be 16 to 19.0 Vdc on a properly aligned A6 assembly.
- d. Measure PLL II Assembly A7 VCO control voltage at TP1, and adjust C15 for a voltage equal to that of the A6 PLL I VCO control voltage (step c).
- e. Tune the receiver to 20 MHz, then 10 MHz, and then 0 MHz, measuring the VCO control voltages on both assemblies at each frequency. The two voltages should track each other at all times, and differ by no more than  $\pm .5$  Vdc. Test is complete.

**5. PARTS LIST**

Table 3 is a comprehensive parts list of all replaceable components in PLL II Assembly A7. When ordering parts from the factory, include a full description of the part. Use figure 2, PLL II Assembly A7 Component Location Diagram to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 3 is the PLL II Assembly A7 schematic diagram.

**Table 3. PLL II Assembly A7 Parts List (PL 10073-4200)**

Ref. Desig.	Part Number	Description
	10073-4200	PWB, PLL 2
	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/01-1535	CAP .01UF 20% 100V CER
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4 - C6	M39014/01-1535	CAP .01UF 20% 100V CER
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/01-1535	CAP .01UF 20% 100V CER
C9	C26-0025-100	CAP 10UF 20% 25V TANT
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	C26-0025-100	CAP 10UF 20% 25V TANT
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/01-1535	CAP .01UF 20% 100V CER
C15	C85-0001-002	CAP 1.0-10PF 250V
C16	CK05BX102M	CAP 1000PF 20% 200V CER

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Table 3. PLL II Assembly A7 Parts List (PL 10073-4200) (Cont.)

Ref. Desig.	Part Number	Description
C17	CK05BX102M	CAP 1000PF 20% 200V CER
C18	C26-0025-100	CAP 10UF 20% 25V TANT
C19	M39014/02-1310	CAP .1UF 10% 100V CER-R
C20	C26-0025-100	CAP 10UF 20% 25V TANT
C21	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	C26-0025-100	CAP 10UF 20% 25V TANT
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/01-1535	CAP .01UF 20% 100V CER
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/01-1535	CAP .01UF 20% 100V CER
C30	M39014/01-1535	CAP .01UF 20% 100V CER
C31	CK05BX102M	CAP 1000PF 20% 200V CER
C32	M39014/01-1535	CAP .01UF 20% 100V CER
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	M39014/01-1535	CAP .01UF 20% 100V CER
C35	M39014/02-1310	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	CM06FD472J03	CAP 4700PF 5% 500V MICA
C39	C-0912	CAPACITOR
C40	C-0912	CAPACITOR
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	CM06FD242J03	CAP 2400PF 5% 500V MICA
C45	CM06FD432J03	CAP 4300PF 5% 500V MICA
C46	C25-0001-301	CAP 1.0UF 20% 20V TANT
C51	M39014/02-1310	CAP .1UF 10% 100V CER-R
C52	6628-0660	CAP 5600PF 5% 300V MICA
C53	M39014/02-1310	CAP .1UF 10% 100V CER-R
C54	C26-0035-470	CAP 47UF 20% 35V TANT
C55	C-8212	CAP 470UF 50V ELEC
C56	M39014/02-1310	CAP .1UF 10% 100V CER-R
C57	M39014/02-1310	CAP .1UF 10% 100V CER-R
C58	M39014/02-1310	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310	CAP .1UF 10% 100V CER-R
C61	C26-0025-100	CAP 10UF 20% 25V TANT
C62	M39014/02-1310	CAP .1UF 10% 100V CER-R
C63	M39014/02-1310	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310	CAP .1UF 10% 100V CER-R
C82	CM04ED390J03	CAP 39PF 5% 500V MICA
C83	M39014/01-1535	CAP .01UF 20% 100V CER
CR1	10073-7118	DIODE, HYPERABRUPT
CR2	10073-7118	DIODE, HYPERABRUPT
CR3	10073-7118	DIODE, HYPERABRUPT
CR4	10073-7118	DIODE, HYPERABRUPT

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**RF COMMUNICATIONS**

Table 3. PLL II Assembly A7 Parts List (PL 10073-4200) (Cont.)

Ref. Desig.	Part Number	Description
CR5	10073-7118	DIODE, HYPERABRUPT
CR6	10073-7118	DIODE, HYPERABRUPT
CR7	10073-7118	DIODE, HYPERABRUPT
CR8	10073-7118	DIODE, HYPERABRUPT
CR9	10073-7118	DIODE, HYPERABRUPT
CR10	10073-7118	DIODE, HYPERABRUPT
CR11	10073-7118	DIODE, HYPERABRUPT
CR12	10073-7118	DIODE, HYPERABRUPT
CR13	1N6263	DIODE .40W 60V HOT CARR
CR14	1N3064	DIODE 75mA 75V SW
CR15	1N3064	DIODE 75mA 75V SW
J1	J46-0032-010	HDR 10 PIN 0.100" SR
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
L1	MS75084-3	COIL 1.8UH 10% FXD RF
L2	MS75084-11	COIL 8.2UH 10% FXD RF
L3	L08-0001-001	CHOKE W B 50 MHZ
L4	L08-0001-001	CHOKE W B 50 MHZ
L5	MS75089-21	COIL RF 680UF 5%
L6	MS75089-21	COIL RF 680UF 5%
L7	L08-0001-001	CHOKE W B 50 MHZ
Q1	2N5109	XSTR RFPWR NPN TO-39
Q2	Q35-0003-000	XSTR U310 JFET HIGH GM
Q3	Q35-0003-000	XSTR U310 JFET HIGH GM
Q4	2N3563	XSTR SS/RF
Q5	Q35-0003-000	XSTR U310 JFET HIGH GM
Q6	2N2907	XSTR SS/GP PNP TO-18
Q7	Q60-0003-000	XSTR MOSFET
Q8	2N2907	XSTR SS/GP PNP TO-18
Q9	2N2222	XSTR SS/GP NPN TO-18
Q10	2N2222	XSTR SS/GP NPN TO-18
Q11	2N5088	XSTR SS/GP
Q12	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-470	RES 47 5% 1/4W CAR FILM
R2	R65-0003-471	RES 470 5% 1/4W CAR FILM
R3	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R4	R65-0003-470	RES 47 5% 1/4W CAR FILM
R5	R65-0003-100	RES 10 5% 1/4W CAR FILM
R6	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R7	R65-0003-201	RES 200 5% 1/4W CAR FILM
R8	R65-0003-270	RES 27 5% 1/4W CAR FILM
R9	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R10	R65-0003-201	RES 200 5% 1/4W CAR FILM
R11	R65-0003-510	RES 51 5% 1/4W CAR FILM

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Table 3. PLL II Assembly A7 Parts List (PL 10073-4200) (Cont.)

Ref. Desig.	Part Number	Description
R12	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R13	R65-0003-151	RES 150 5% 1/4W CAR FILM
R14	R65-0003-680	RES 68 5% 1/4W CAR FILM
R15	R65-0003-101	RES 100 5% 1/4W CAR FILM
R16	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R17	R65-0003-100	RES 10 5% 1/4W CAR FILM
R18	R65-0003-151	RES 150 5% 1/4W CAR FILM
R19	R65-0003-470	RES 47 5% 1/4W CAR FILM
R20	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R21	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R22	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R23	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R24	R65-0003-201	RES 200 5% 1/4W CAR FILM
R25	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R28	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R29	R65-0003-479	RES 4.7 5% 1/4W CAR FILM
R31	R65-0003-279	RES 2.7 5% 1/4W CAR FILM
R32	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R33	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R34	RN55D1501F	RES,1500 1% 1/8W MET FLM
R35	RN55D2001F	RES,2000 1% 1/8W MET FLM
R36	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R37	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R38	RN55D1212F	RES,12.1K 1% 1/8W MET FLM
R39	R65-0003-121	RES 120 5% 1/4W CAR FILM
R40	R65-0003-101	RES 100 5% 1/4W CAR FILM
R41	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R42	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R43	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R44	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R45	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R46	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R47	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R48	R65-0003-103	RES 10K 5% 1/4W CAR FILM
T1	10073-7014	TRANSFORMER, RF, FIXED
T2	10073-7014	TRANSFORMER, RF, FIXED
T3	10073-7002	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	I65-0004-001	IC 12013 PLASTIC ECL



**Table 3. PLL II Assembly A7 Parts List (PL 10073-4200) (Cont.)**

Ref. Desig.	Part Number	Description
U2	I70-0002-001	IC MC145156 PLASTIC CMOS
U3	I01-0000-019	IC 4050B PLASTIC CMOS
U4	I05-0000-000	IC 74LS00 PLASTIC TTL
U5	I30-0018-000	IC 1458 OP AMP PLASTIC
VR1	I12-0006-012	IC VR 78L12A + 12V .10A 4%
VR2	I11-0001-001	IC VR 7805 + 5V 1.5A 4%
VR3	1N5236A	DIODE 7.5V 10% .5W ZENER

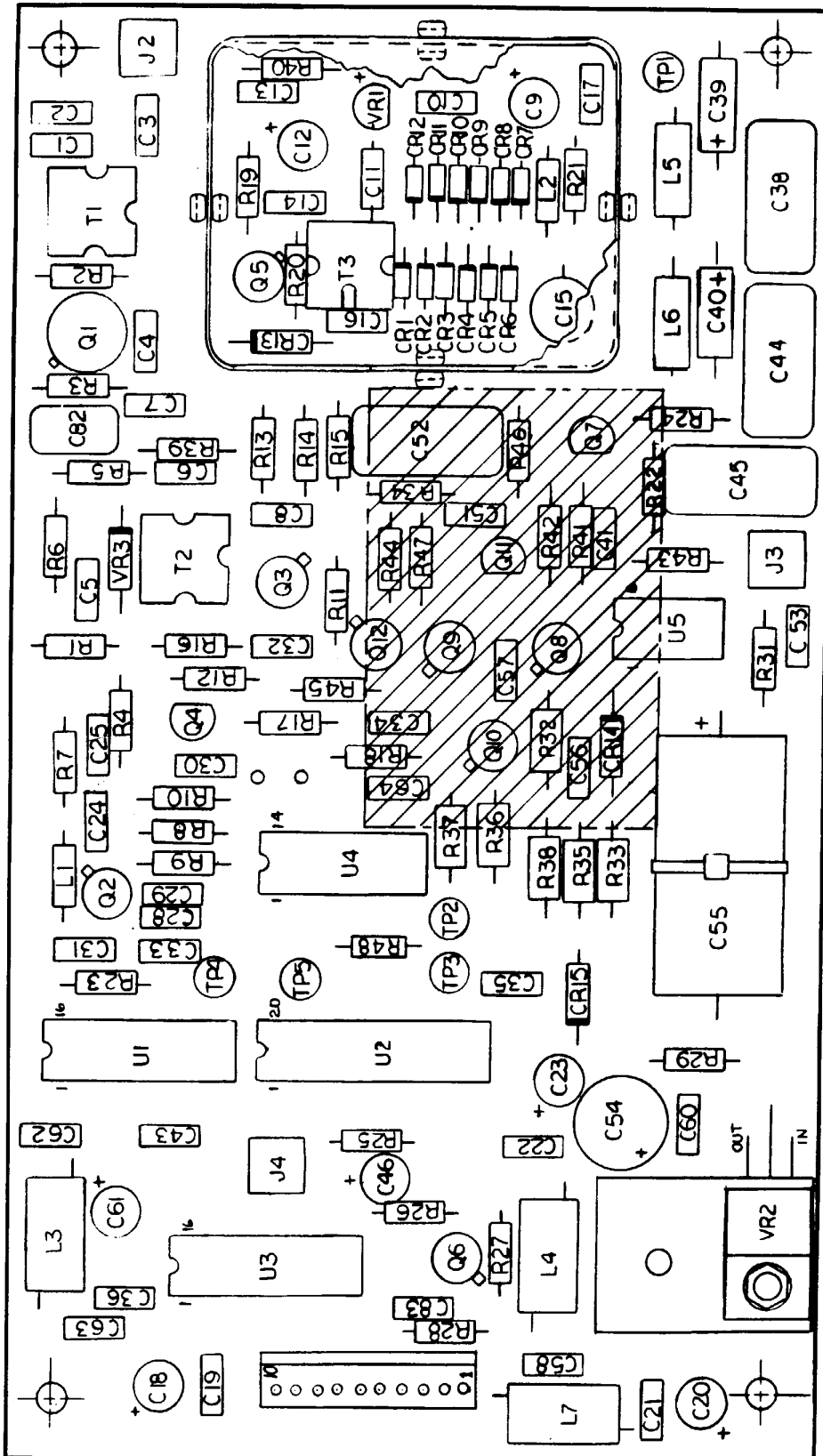


Figure 2. PLL II Assembly A7 Component Location Diagram (10073-4200, Rev. C)

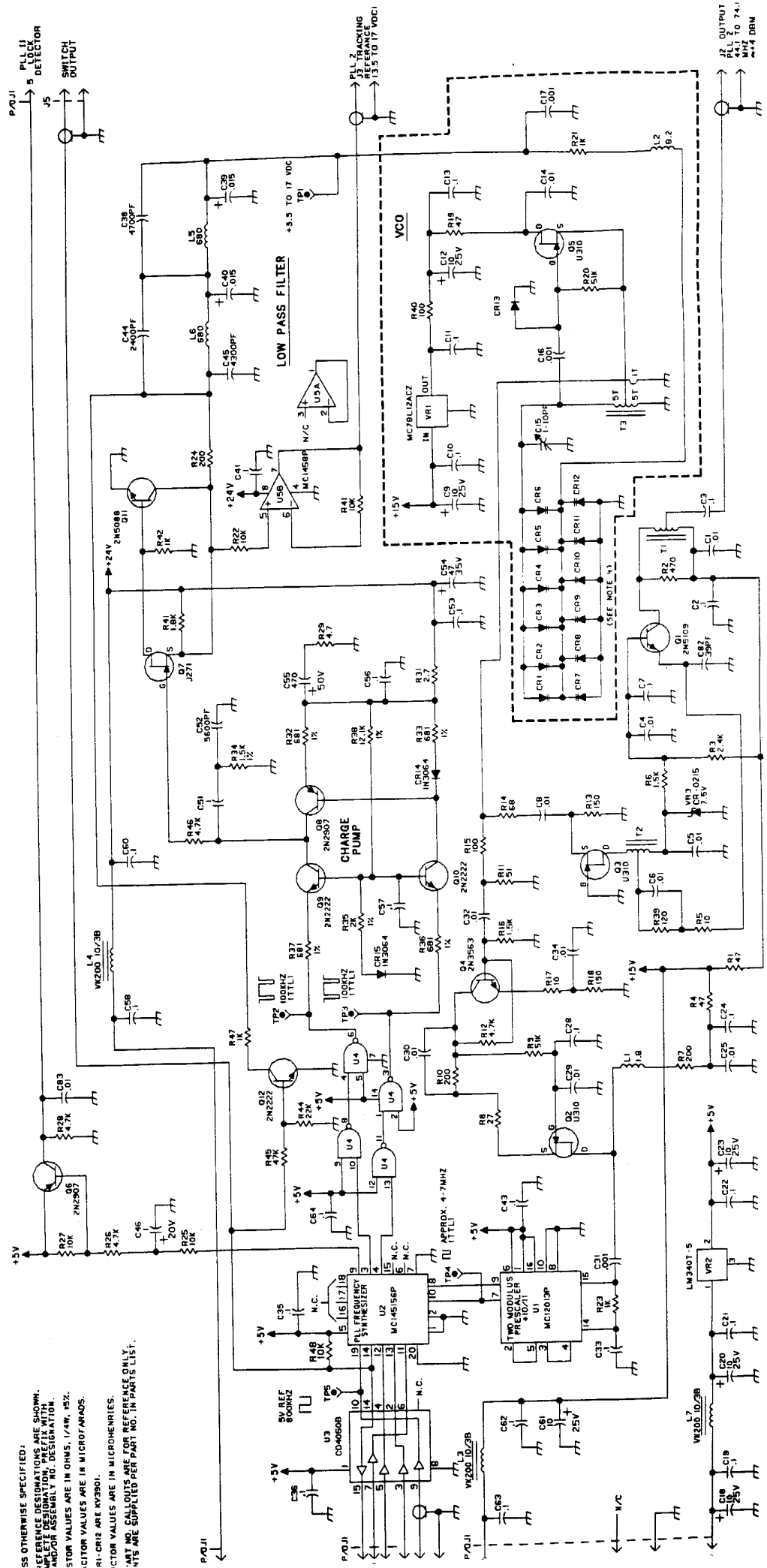


Figure 3. PLL II Assembly A7 Schematic Diagram (10073-4201, Rev. H)



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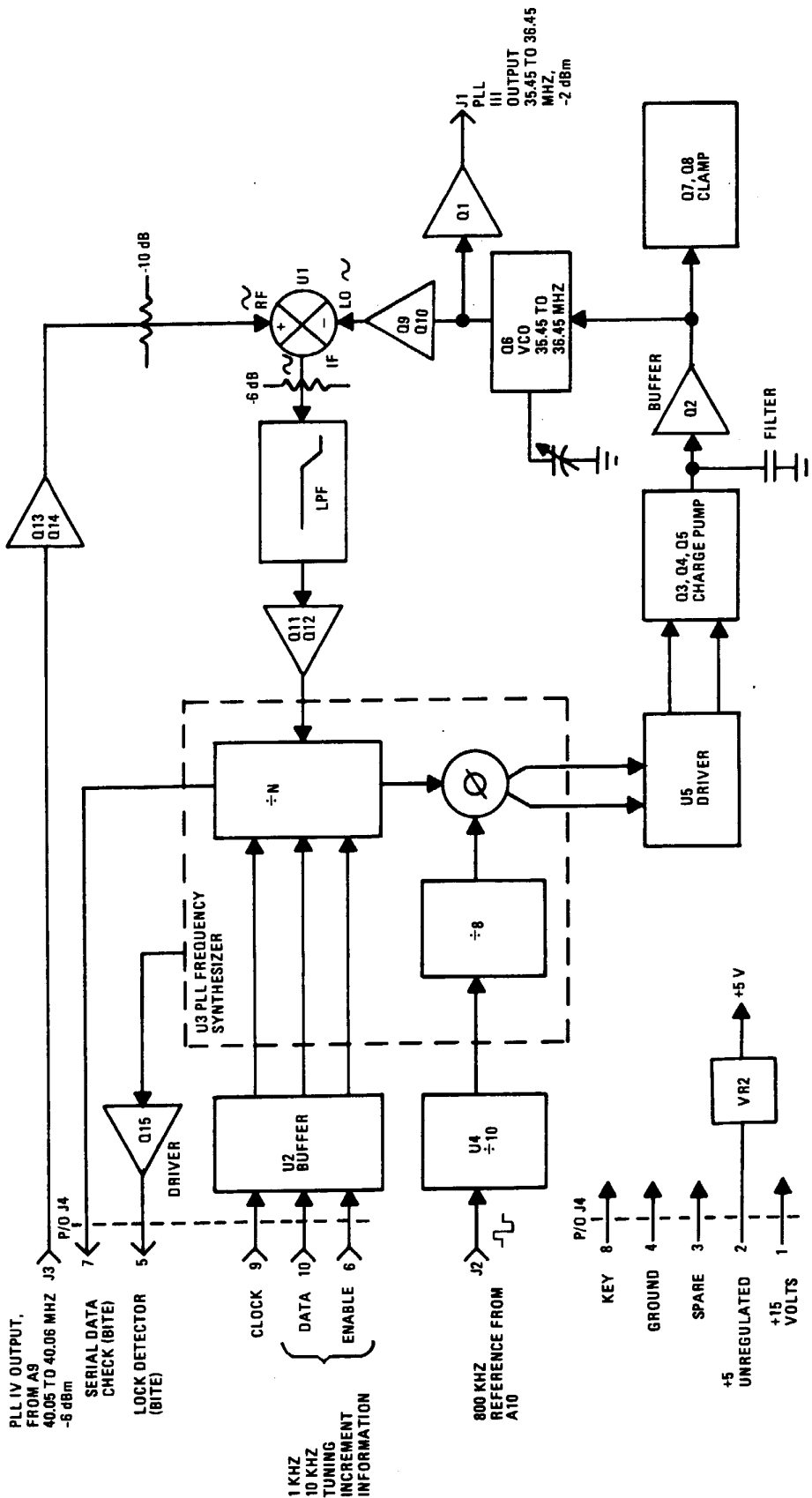
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PLL III  
ASSEMBLY  
A8



590-33(1)

PLL III Assembly A8 Functional Block Diagram

## 1. GENERAL DESCRIPTION

PLL III is a programmable translation loop which performs the following primary functions.

- Generation of 1 kHz and 10 kHz tuning increments as chosen by the RF-590 front panel controls
- Combination of these increments with information containing the 1 Hz, 10 Hz, and 100 Hz tuning increments

Frequency select input data for 1 kHz and 10 kHz tuning increments is applied to the A8 assembly in serial data format from the Control Board Assembly microprocessor. The 1 Hz, 10 Hz, and 100 Hz tuning increments information is supplied via PLL IV Assembly A9 in the frequency range of 40.06 to 40.05 MHz. A8 output to PLL I Assembly A6 contains 1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz tuning information in the frequency range of 35.45 to 36.45 MHz.

## 2. INTERFACE CONNECTIONS

Table 1 details the input/output connections and other relevant data.

**Table 1. PLL III Assembly Interface Connections**

Connector	Function	Characteristics
J1	PLL III Output	35.45 to 36.45 MHz, $\approx$ -2 dBm
J2	800 kHz Reference Input	TTL
J3	PLL IV Output	40.05 to 40.06 MHz, $\approx$ -6 dBm
J4-1	+15 Volts	$\approx$ 60 mA
J4-2	+5 Volts Unregulated	$\approx$ 30 mA
J4-3	Spare	
J4-4	Ground	
J4-5	Lock Detector Output	0 Vdc = PLL locked; +5 Vdc = PLL unlocked
J4-6	Enable	+ going pulse = enabled
J4-7	Serial Data Check	P/O BITE Test, +5 Vdc = ok
J4-8	Key	
J4-9	Clock	750 kHz, TTL
J4-10	Data	Serial TTL

### 3. A8 FREQUENCY GENERATION SCHEME

A PLL intermediate frequency (IF) range of 3.61 MHz to 4.61 MHz is produced at the IF output of mixer U1. The instantaneous IF frequency is a consequence of the subtractive mixing of the following two signals:

- 40.050 to 40.060 MHz PLL IV (RF port)
- 35.45 to 36.45 MHz VCO (LO port)

This IF signal will change in frequency to satisfy the requirement that the divide by N counter output will always try to equal the reference 10.000 kHz signal at the inputs to the Phase Comparator, P/O U3. When these two signals are not equal, the Phase Comparator produces an error command to drive the VCO frequency in the direction required to make them equal. If the divide by N output exceeds the reference 10.000 kHz, the VCO will rise in frequency. If the divide by N output is less than the reference, the VCO will decrease in frequency.

The VCO output frequency then is dependent upon the following two events:

- a. The division factor of the divide by N counter.  $N = (361 + XX)$ , where XX is the value of the 10 kHz and 1 kHz receiver tuning positions, respectively.
- b. The PLL IV output frequency. This is dependent upon the value of the 100 Hz, 10 Hz, and 1 Hz tuning positions (section A9, PLL IV Assembly).

To illustrate this, assume that the receiver is tuned to a frequency of  $X_8X_7X_6X_5X_4X_3X_2X_1$  Hz, where the Xs represent the values of the 1, 10, 100 Hz etc, tuning positions.

Example 1: Assume that the  $X_3X_2X_1$  value decreases.

- a. As  $X_3X_2X_1$  decreases the PLL IV output (RF) increases.
- b.  $RF - LO = IF$  increases.
- c. The divide by N output frequency ( $= IF \div N$ ) increases. Since this will now exceed the 10.000 kHz reference frequency, the Phase Comparator output forces the VCO frequency (LO) to increase.
- d. Now,  $RF - LO = IF$  decreases. The IF will decrease until the divide by N output again equals the reference.

Example 2: Assume that the  $X_5X_4$  value decreases.

- a. As  $X_5X_4$  decreases, the divide by N factor ( $N = 361 + X_5X_4$ ) decreases.



- b. The divide by N output frequency, equal to  $IF \div N$ , increases. Since this now exceeds the 10.000 kHz reference at the Phase Comparator inputs, the Phase Comparator output forces the VCO (LO) frequency to increase.
- c.  $RF - LO = IF$  decreases.
- d.  $IF \div N$  decreases, and continues to do so until equal to the reference.

The converse of both of these cases is true for  $X_3X_2X_1$  and/or  $X_5X_4$  increasing.

The A8 PLL III Output Frequency may be calculated from the following equation; given the receiver tune frequency is  $X_8X_7, X_6X_5X_4, X_3X_2X_1$  Hz:

$$FA8 = [40,000,000 + 10 (6000 - X_3X_2X_1)] - [10,000 (361 + X_5X_4)], \text{ Hz}$$

#### 4. CIRCUIT DESCRIPTIONS

##### NOTE

A8 operation is similar to the general PLL and charge pump circuits described in section 4. A review of section 4 at this time would help in understanding A8 operation.

##### 4.1 PLL IF Generation

PLL output at a -6 dBm level is applied to 10 dB gain stage Q13 and Q14. This output is attenuated by 50 ohm matching network R39, R40, and R44 and presents a -6 dBm signal ranging from 40.050 MHz to 40.060 MHz to the RF port of mixer U1.

U1 LO injection is supplied by the VCO via amplifier stage Q9 and Q10 at a +7 dBm level. This signal ranges from 35.45 to 36.45 MHz.

U1 IF output is approximately -12 dBm (in the 3.61 to 4.61 MHz range). The 6 dB attenuator network, R41-R43, feeds a low pass filter which removes all mixer products except the desired IF range. Amplifier stage Q11 and Q12 provide a TTL level signal to a divide by N counter internal to U3 at pin 10.

##### 4.2 Divide by N Counter

Since the A8 assembly requires a variable output frequency dependent upon the 1 kHz and 10 kHz tuning positions a divide by N programmable counter has been incorporated into the VCO feedback loop. The front panel selection of a tune frequency from 00 kHz to 99 kHz causes Control Assembly A14 to generate a serial data code containing information pertaining to the values chosen. This code is applied synchronously with the 750 kHz system clock to U3, whenever the U3 enable line is gated open by A14.

$N = (361 + XX)$  where  $XX$  is the value of the 10 kHz and 1 kHz tuning positions. The divide by  $N$  counter output will always attempt to equal the 10.000 kHz reference frequency at the Phase Comparator inputs.

#### 4.3 Phase Comparator and Charge Pump Operation

A 10.000 kHz Reference signal is applied to one port of the Phase Comparator. This signal has been divided down from the 800 kHz TTL reference supplied by the A10 assembly. Divide by 10 circuit U4 feeds 80 kHz to the divide by 8 circuit internal to U3.

The second input to the Phase Comparator is the divide by  $N$  counter output. When these two signals are equal in frequency and phase, the outputs at Buffer stage U5 (TP2 and TP3) is essentially a +5 Vdc level. This level holds Q4, Q5, and consequently Q3 off. The voltage across C8 is constant. Q2 is biased to produce a constant voltage across R12, and the dc level (VCO control) at TP1 is constant. This holds the VCO at a constant frequency.

Assuming that the divide by  $N$  output exceeds the reference 10.000 kHz, the Phase Comparator output at TP3 pulses low (the pulse width being a function of the amount of difference between the two signals). Q5 turns on, and its falling collector voltage turns Q3 on, allowing Q3 to pump charge into C8. C8 voltage increases, causing Q2 to conduct more current and develop a large voltage across R12. The VCO control voltage increases and forces the VCO to tune higher in frequency. This will lower the IF frequency, and divide by  $N$  counter output will decrease. As the divide by  $N$  counter output approaches the reference, the pulse widths will get narrower until a 5 Vdc level will again occur at TP3. At this point, Q5 turns off, Q3 stops pumping charge into C8, the VCO control voltage stops at a new higher level, and the VCO has been tuned to a higher frequency.

Assuming that the divide by  $N$  counter output is less than the reference. The Phase Comparator output at TP2 will pulse low. Q4 turns on and draws charge out of C8. Q2 conducts less current, and the VCO voltage drops, driving the VCO frequency down. The IF feedback signal frequency will increase, and consequently the divide by  $N$  counter output will increase. As this output approaches the reference frequency, TP2 pulses will get narrower until Q4 is turned off. The voltage across C8 halts at a lower value (as does the VCO control voltage level). This holds the VCO at a new lower frequency.

#### 4.4 VCO Operation and Control

A charge pump circuit consisting of Q3, Q4, Q5 (and associated components) in conjunction with filter network C8, C9, and R14 convert the two phase comparator pulse outputs into an analog dc control voltage. Buffer amplifier Q2 applies a VCO control voltage to the varactor diode string in the VCO. Changing diode capacitance fine tunes JFET Hartley oscillator stage Q6. The total VCO frequency range is 35.45 to 36.45 MHz. A control voltage range of approximately 6.5 to 7.5 Vdc will tune the oscillator from 35.45 MHz to 36.45 MHz.

Clamp circuit Q7, Q8 and CR2-CR5 monitors the VCO control voltage level, and will prevent the control voltage from exceeding the approximate range of 5.5 to 8.5 Vdc. This "window" is necessary to prevent the VCO from ever running to the wrong side of the frequency conversion during the mixing process. This could cause the receiver to falsely lock at the wrong frequency, or not lock at all. For example, as-

sume that the control voltage could rise high enough to force the VCO to 41 MHz. Combination of the 40.05 to 40.06 MHz signal at mixer U1 would produce a loop IF in the 1 MHz region instead of the required 3.61 to 4.61 MHz range. The clamp circuit would prevent this; however, since CR4, CR5, and Q8 would conduct to clamp the level at 8.5 volts and prevent the VCO from "running away".

The VCO output is fed through amplifier stage Q9 and Q10 to function as a +7 dBm LO injection for U1, and to Q1, where a -2 dBm signal is passed through J1 to PLL I Assembly A6.

#### 4.5 BITE Test Circuits

The A10 assembly contains two circuits for self-test evaluation. The circuits are:

- Lock detector Q15 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by the A14 assembly. A front panel fault light will appear if the loop ever unlocks.
- Serial data check that verifies that the tuning data from the A14 assembly has been received and properly translated into the correct divide by N factor. A serial data word is sent on the data line (J4 pin 10) and the U3 serial data check line is read back to the A14 assembly (J4 pin 7). If the word has been received and properly decoded, this line will pulse to +5 Vdc. The serial data check occurs automatically, but only when the receiver BITE self-test is actuated.

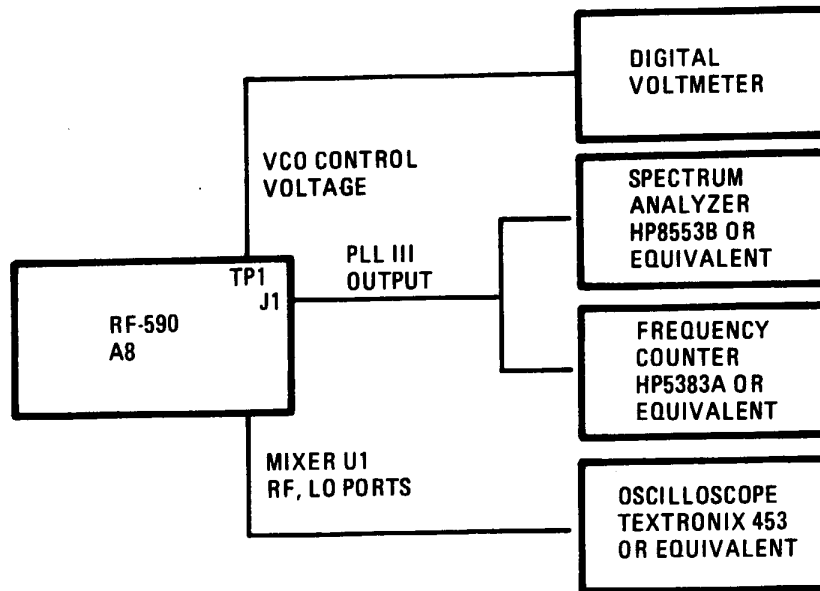
### 5. MAINTENANCE

The following adjustments should not be made as part of a routine maintenance procedure, but rather only when a failure indicates a definite need. All tests should be performed with all connections in normal contact, unless otherwise specified.

#### 5.1 VCO Alignment

Perform the following procedure to align the VCO:

- a. Connect equipment as shown in figure 1.
- b. Set receiver frequency to 00.050500 MHz.
- c. Monitor U1, pin 8, with an oscilloscope and adjust T3 for a maximum signal (should be approximately 1.2 Vpp).
- d. Monitor U1 RF input at R44 with oscilloscope and adjust T4 for a maximum signal (should be approximately 1 Vpp).
- e. Monitor J1 with spectrum analyzer at approximately 35 MHz. Adjust T2 for a maximum output (approximately -2 dBm).



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**Figure 1. A8 VCO Alignment**

- f. Monitor TP1 with DVM. Adjust C11 for 7.0 Vdc. PLL III output vs receiver tune frequency should agree with table 2.

**Table 2. PLL III Output Range**

Receiver Tune Frequency, MHz	PLL III Output Frequency, MHz	Approximate TP1 Voltage, Vdc
00.000000	36.450000	7.9
00.050500	35.944950	7.0
00.099999	35.450010	6.5

- g. Fully reconnect the A8 assembly to the RF-590 and initiate BITE self-test. No failures should occur indicating an A8 fault.

## 6. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in PLL III Assembly A8. When ordering parts from the factory, include a full description of the part. Use figure 2, PLL III Assembly A8 Component Location Diagram.

**7. SCHEMATIC DIAGRAM**

Figure 3 is the PLL III Assembly A8 schematic diagram.

**Table 3. PLL III Assembly A8 Parts List (PL 10073-4300)**

Ref. Desig.	Part Number	Description
	10073-4300	PWB, PLL 3
	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/01-1535	CAP .01UF 20% 100V CER
C3	M39014/01-1535	CAP .01UF 20% 100V CER
C4	CM04ED560J03	CAP 56PF 5% 500V MICA
C5	M39014/01-1535	CAP .01UF 20% 100V CER
C6	C26-0025-100	CAP 10UF 20% 25V TANT
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1318	CAP .33UF 10% 50V CER
C9	M39014/02-1543	CAP .027UF 10% 50V CER
C10	C26-0025-339	CAP 3.3UF 20% 25V TANT
C11	C84-0003-008	CAP 3-15PF 200V CER
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	CK05BX102M	CAP 1000PF 20% 200V CER
C15	M39014/01-1535	CAP .01UF 20% 100V CER
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	M39014/01-1535	CAP .01UF 20% 100V CER
C19	CK05BX102M	CAP 1000PF 20% 200V CER
C20	C26-0025-100	CAP 10UF 20% 25V TANT
C21	M39014/01-1535	CAP .01UF 20% 100V CER
C22	C26-0025-100	CAP 10UF 20% 25V TANT
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	CM04ED470J03	CAP 47PF 5% 500V MICA
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	M39014/01-1535	CAP .01UF 20% 100V CER
C28	M39014/01-1535	CAP .01UF 20% 100V CER
C29	C26-0016-151	CAP 150UF 20% 16V TANT
C30	M39014/01-1535	CAP .01UF 20% 100V CER
C31	M39014/01-1535	CAP .01UF 20% 100V CER
C32	C26-0025-339	CAP 3.3UF 20% 25V TANT
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	CM04ED470J03	CAP 47PF 5% 500V MICA
C35	M39014/01-1535	CAP .01UF 20% 100V CER
C36	C26-0025-100	CAP 10UF 20% 25V TANT
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R

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Table 3. PLL III Assembly A8 Parts List (PL 10073-4300) (Cont.)

Ref. Desig.	Part Number	Description
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C42	CM04FD151J03	CAP 150PF 5% 500V MICA
C43	CM04FD151J03	CAP 150PF 5% 500V MICA
C44	CM04FC271J03	CAP 270PF 5% 300V MICA
C45	CM04FC301J03	CAP 300PF 5% 300V MICA
C46	CM04FC271J03	CAP 270PF 5% 300V MICA
C47	CM04FC271J03	CAP 270PF 5% 300V MICA
C48	CM04FD111J03	CAP 110PF 5% 500V MICA
C49	CM04CD120J03	CAP 12PF 5% 500V MICA
C50	M39014/02-1310	CAP .1UF 10% 100V CER-R
C51	CM04ED330J03	CAP 33PF 5% 500V MICA
C52	CM04FD151J03	CAP 150PF 5% 500V MICA
C53	CM04CD120J03	CAP 12PF 5% 500V MICA
C54	M39014/01-1535	CAP .01UF 20% 100V CER
C55	M39014/01-1535	CAP .01UF 20% 100V CER
C56	CM04ED470J03	CAP 47PF 5% 500V MICA
C57	M39014/01-1535	CAP .01UF 20% 100V CER
C58	CM04ED390J03	CAP 39PF 5% 500V MICA
C59	M39014/01-1535	CAP .01UF 20% 100V CER
C60	M39014/01-1535	CAP .01UF 20% 100V CER
C61	M39014/02-1310	CAP .1UF 10% 100V CER-R
C62	C26-0025-470	CAP 47UF 20% 25V TANT
C63	C26-0025-470	CAP 47UF 20% 25V TANT
C64	M39014/02-1310	CAP .1UF 10% 100V CER-R
C65	M39014/02-1310	CAP .1UF 10% 100V CER-R
C66	M39014/02-1310	CAP .1UF 10% 100V CER-R
C67	M39014/02-1310	CAP .1UF 10% 100V CER-R
C68	M39014/02-1310	CAP .1UF 10% 100V CER-R
C69	C25-0001-301	CAP 1.0UF 20% 20V TANT
C70	M39014/01-1535	CAP .01UF 20% 100V CER
C71	M39014/01-1535	CAP .01UF 20% 100V CER
C72	M39014/01-1535	CAP .01UF 20% 100V CER
CR1	1N6263	DIODE, HOT CARRIER
CR2	1N3064	DIODE 75mA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N3064	DIODE 75mA 75V SW
CR7	10073-7118	DIODE, SILICON, HYPERABRUPT
CR8	10073-7118	DIODE, SILICON, HYPERABRUPT
CR9	10073-7118	DIODE, SILICON, HYPERABRUPT
CR10	10073-7118	DIODE, SILICON, HYPERABRUPT

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Table 3. PLL III Assembly A8 Parts List (PL 10073-4300) (Cont.)

Ref. Desig.	Part Number	Description
CR11	10073-7118	DIODE, SILICON, HYPERABRUPT
CR12	10073-7118	DIODE, SILICON, HYPERABRUPT
CR13	10073-7118	DIODE, SILICON, HYPERABRUPT
CR14	10073-7118	DIODE, SILICON, HYPERABRUPT
CR15	10073-7118	DIODE, SILICON, HYPERABRUPT
CR16	10073-7118	DIODE, SILICON, HYPERABRUPT
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0032-010	HDR 10 PIN 0.100" SR
L1	MS75084-13	COIL 12UH 10% FXD RF
L2	MS75083-6	COIL .27UH 10% FXD RF
L3	MS75084-6	COIL 3.3UH 10% FXD RF
L4	MS75083-6	COIL .27UH 10% FXD RF
L5	L08-0001-001	CHOKE W B 50 MHZ
L6	MS18130-9	COIL 1.2UH 10% FXD RF
L7	MS18130-9	COIL 1.2UH 10% FXD RF
L8	MS18130-8	COIL 1.0UH 10% FXD RF
L9	L08-0001-001	CHOKE W B 50 MHZ
Q1	Q35-0003-000	XSTR U310 JFET HIGH GM
Q2	Q05-0001-000	XSTR JFET N-CH
Q3	2N2907	XSTR SS/GP PNP TO-18
Q4	2N2222	XSTR SS/GP NPN TO-18
Q5	2N2222	XSTR SS/GP NPN TO-18
Q6	Q35-0003-000	XSTR U310 JFET HIGH GM
Q7	2N2222	XSTR SS/GP NPN TO-18
Q8	2N2907	XSTR SS/GP PNP TO-18
Q9	Q35-0003-000	XSTR U310 JFET HIGH GM
Q10	2N5109	XSTR RFPWR NPN TO-39
Q11	Q-0153	XSTR SS/RF PN4258
Q12	2N2369	XSTR SS/RF NPN
Q13	2N2369	XSTR SS/RF NPN
Q14	Q35-0003-000	XSTR U310 JFET HIGH GM
Q15	2N2907	XSTR SS/GP PNP TO-18
R1	R65-0003-101	RES 100 5% 1/4W CAR FILM
R2	R65-0003-470	RES 47 5% 1/4W CAR FILM
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-101	RES 100 5% 1/4W CAR FILM
R5	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R7	R65-0003-201	RES 200 5% 1/4W CAR FILM
R8	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R9	RN55D1501F	RES,1500 1% 1/8W MET FLM
R10	RN55D1501F	RES,1500 1% 1/8W MET FLM
R11	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R12	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM

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**Table 3. PLL III Assembly A8 Parts List (PL 10073-4300) (Cont.)**

Ref. Desig.	Part Number	Description
R13	RN55D3321F	RES,3320 1% 1/8W MET FLM
R14	RN55D1621F	RES,1620 1% 1/8W MET FLM
R15	RN55D2211F	RES,2210 1% 1/8W MET FLM
R16	RN55D2211F	RES,2210 1% 1/8W MET FLM
R17	R65-0003-330	RES 33 5% 1/4W CAR FILM
R18	R65-0003-121	RES 120 5% 1/4W CAR FILM
R19	R65-0003-360	RES 36 5% 1/4W CAR FILM
R20	R65-0003-201	RES 200 5% 1/4W CAR FILM
R21	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R22	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R23	R65-0003-470	RES 47 5% 1/4W CAR FILM
R24	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R25	R65-0003-681	RES 680 5% 1/4W CAR FILM
R26	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R27	R65-0003-471	RES 470 5% 1/4W CAR FILM
R28	R65-0003-330	RES 33 5% 1/4W CAR FILM
R29	R65-0003-101	RES 100 5% 1/4W CAR FILM
R30	R65-0003-271	RES 270 5% 1/4W CAR FILM
R31	R65-0003-820	RES 82 5% 1/4W CAR FILM
R32	R65-0003-391	RES 390 5% 1/4W CAR FILM
R33	R65-0003-561	RES 560 5% 1/4W CAR FILM
R34	R65-0003-330	RES 33 5% 1/4W CAR FILM
R35	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R36	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R37	R65-0003-471	RES 470 5% 1/4W CAR FILM
R39	R65-0003-750	RES 75 5% 1/4W CAR FILM
R40	R65-0003-101	RES 100 5% 1/4W CAR FILM
R41	R65-0003-101	RES 100 5% 1/4W CAR FILM
R42	R65-0003-101	RES 100 5% 1/4W CAR FILM
R43	R65-0003-750	RES 75 5% 1/4W CAR FILM
R44	R65-0003-101	RES 100 5% 1/4W CAR FILM
R45	R65-0003-101	RES 100 5% 1/4W CAR FILM
R46	R65-0003-111	RES 110 5% 1/4W CAR FILM
R47	R65-0003-471	RES 470 5% 1/4W CAR FILM
R48	R65-0003-470	RES 47 5% 1/4W CAR FILM
R49	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R50	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R51	R65-0003-681	RES 680 5% 1/4W CAR FILM
R52	R65-0003-201	RES 200 5% 1/4W CAR FILM
R53	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R54	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R55	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R56	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R58	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R59	R65-0003-101	RES 100 5% 1/4W CAR FILM



Table 3. PLL III Assembly A8 Parts List (PL 10073-4300) (Cont.)

Ref. Desig.	Part Number	Description
R60	R65-0003-560	RES 56 5% 1/4W CAR FILM
T1	10073-7004	TRANSFORMER, RF, FIXED
T2	10073-7011	TRANSFORMER, RF, VARIABLE
T3	10073-7011	TRANSFORMER, RF, VARIABLE
T4	10073-7011	TRANSFORMER, RF, VARIABLE
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP6	J-0072	TP PWB BLU TOP ACCS .080"
U1	I51-0003-003	MIXER DB 50mW 500MHZ
U2	I01-0000-019	IC 4050B PLASTIC CMOS
U3	I70-0002-001	IC MC145156 PLASTIC CMOS
U4	I05-0000-090	IC 74LS90 PLASTIC TTL
U5	I05-0000-000	IC 74LS00 PLASTIC TTL
VR1	I12-0005-012	IC VR 78L12 + 12V .10A 10
VR2	I11-0001-001	IC VR 7805 + 5V 1.5A 4%
VR3	1N5236A	DIODE 7.5V 10% .5W ZENER
VR4	1N5236A	DIODE 7.5V 10% .5W ZENER

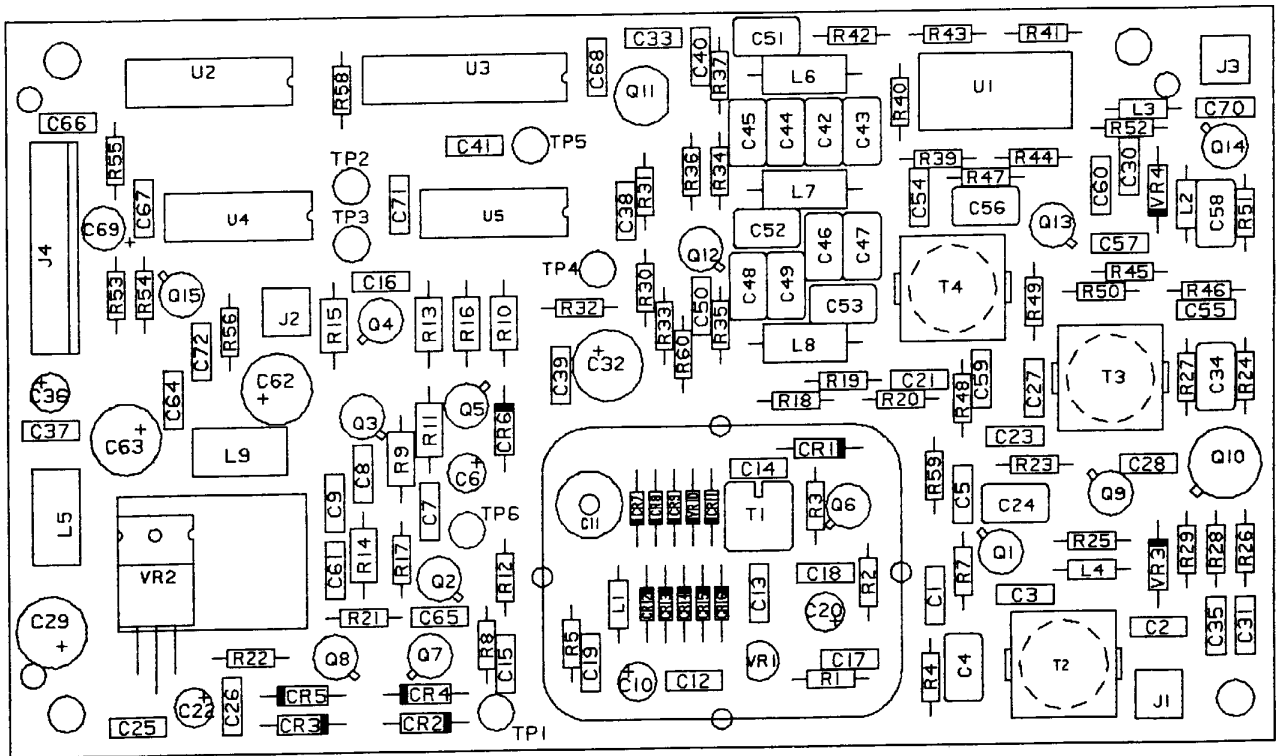
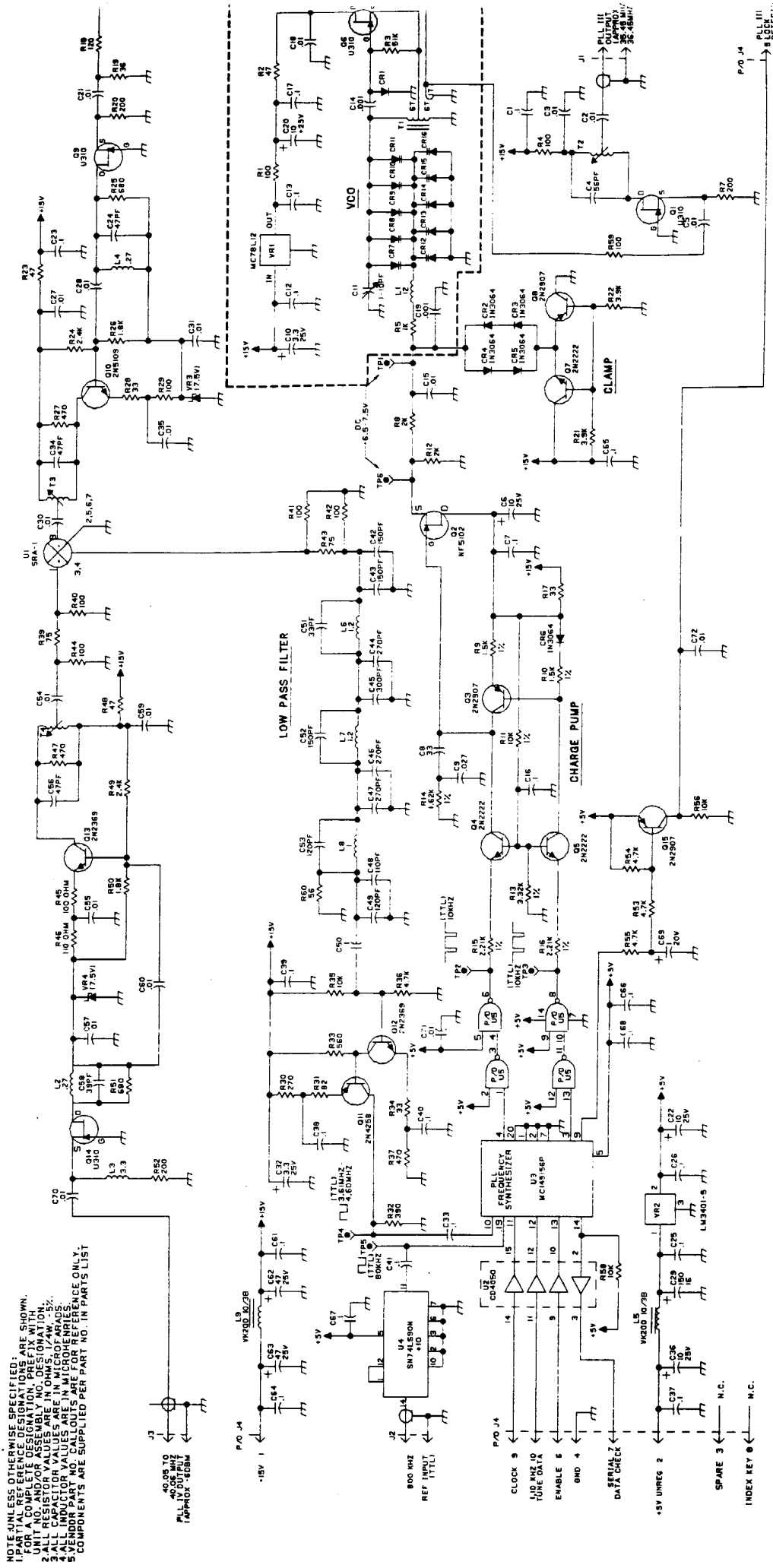


Figure 2. PLL III Assembly A8 Component Location Diagram (10073-4300, Rev. D)



NOTE UNLESS OTHERWISE SPECIFIED:  
 1. FOR A COMPLETE DESIGNATION, SHOW UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.  
 2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.  
 3. ALL CAPACITOR VALUES ARE IN MICROFARADS.  
 4. ALL INDUCTOR VALUES ARE IN MICROGRAMS.  
 5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

Figure 3. PLL III Assembly A8 Schematic Diagram (10073-4301, Rev. F)

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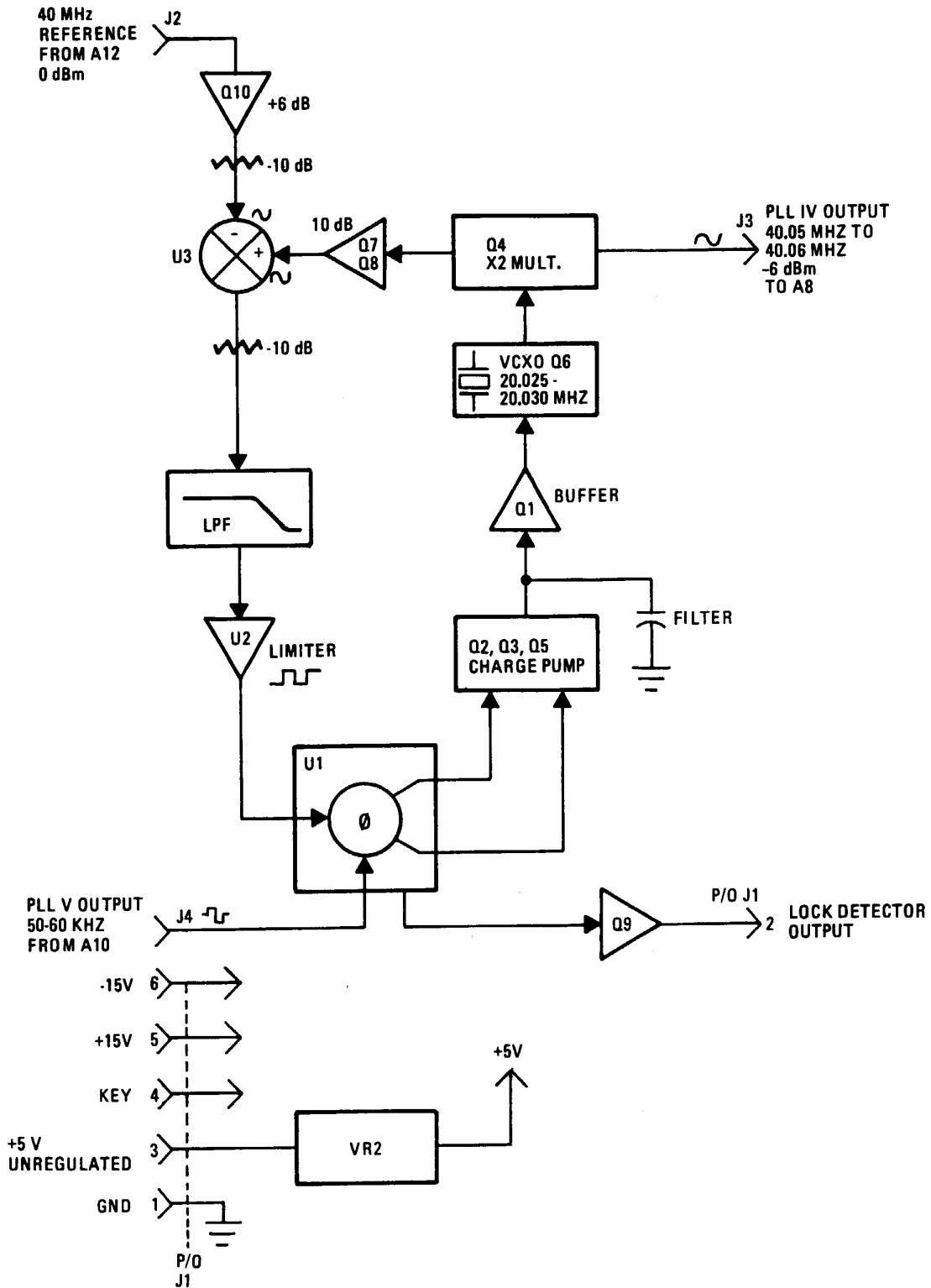
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PLL IV Assembly A9 Functional Block Diagram

## 1. GENERAL DESCRIPTION

PLL IV Assembly A9 is a translation type phase lock loop which converts the low frequency variable PLL V output at 50 to 60 kHz (in 10 Hz steps) into a higher frequency signal at 40.05 to 40.06 MHz. During translation, the 10 Hz step size is preserved. This conversion process is an intermediate step leading toward the 1 Hz, 10 Hz, and 100 Hz tuning increments in the RF-590 LO no. 1 frequency range of 40.465 to 70.455 MHz.

## 2. INTERFACE CONNECTIONS

Table 1 details the input/output connections and other relevant data.

**Table 1. PLL IV Assembly Interface Connections**

Connector	Function	Characteristics
J1-1	Gnd	
J1-2	Lock Detector Output	0 V = Locked, +5 V = Unlocked, P/O BITE Test
J1-3	+5 Volts Unregulated	Approximately 50 mA
J1-4	Key	
J1-5	+15 V	Approximately 60 mA
J1-6	-15 V	Approximately 6 mA
J2	40 MHz Reference	40.000000 MHz, 0 dBm
J3	PLL IV Output	40.050 to 40.060 MHz, -6 dBm
J4	PLL V Output	50.0 to 60.0 kHz, TTL

## 3. CIRCUIT DESCRIPTION

### 3.1 PLL IF Generation

A PLL intermediate frequency (IF) signal in the range of 50 kHz to 60 kHz is produced at the output of mixer U3. This IF signal is a result of the mixing of the 40.000000 MHz reference from A12 with a VCXO derived signal in the range of 40.050 to 40.060 MHz.

This IF signal is then compared against the PLL V output (a signal also in the range of 50 to 60 kHz) at Phase Comparator U1. If there is any difference in phase or frequency between the IF and the PLL V output signals, U1 produces an error output which forces the VCXO to shift in frequency. The new IF

produced will be equal to the A10 output frequency. The net result is that the VCXO derived frequency always equals the reference plus the A10 output frequency (even as the A10 output changes frequencies). As the A10 output changes from 50 to 60 kHz in 10 Hz increments, the A9 output will change from 40.050 MHz to 40.060 MHz (also in 10 Hz increments).

The actual value of the PLL IV output frequency can be determined by the following formula.  $F = [40.000,000 + 10 (6000 - XXX)]$  Hz, where XXX is the value of the 100 Hz, 10 Hz, and 1 Hz receiver tune positions, respectively.

The 40.000000 MHz reference signal from the A12 assembly enters A9 at J2 (0 dBm) and is applied to 6 dB gain amplifier stage Q10. The signal is attenuated to -4 dBm by 50 ohm matching network R28, R29, and R30, and applied to the RF port of mixer U3 at pin 1.

U3 LO injection at pin 8 is a 40.05 MHz to 40.06 MHz signal derived from the VCXO, and amplified to a +7 dBm level by LO amplifier stage Q7 and Q8.

U3 mixing action produces a 30 mVrms IF signal at pins 3 and 4 (in 50 to 60 kHz range). The -6 dB matching network R31, R32, and R34 couples this signal to a low pass filter network which removes all undesired mixer products except the IF signal. High gain amplifier U2 boosts this signal to a TTL level prior to application to one side of phase comparator U1.

### 3.2 Phase Comparator and Charge Pump Circuits

Phase Comparator U1 compares the IF signal with PLL V output signals in the range of 50 to 60 kHz. When these two signals are equal in frequency and phase, U1 outputs at TP2 and TP3 are essentially 5 Vdc. All transistors in the charge pump circuit (Q2, Q3, Q5) are turned off. The voltage across C19 is constant and Q1 is biased on producing a constant VCXO control voltage across R4. This holds the VCXO frequency constant.

Assume that PLL V output increases in frequency. The PLL V output frequency at U1, pin 1, will be higher than the IF signal frequency at pin 3. The U1 output at TP3 pulses low, turning Q5 on. Consequently, Q2 turns on as the Q5 collector voltage drops; Q2 pumps charge into C19, causing Q1 to conduct more current with a proportionate increase in voltage across R4. This rising control voltage forces the VCXO to increase in frequency, producing a corresponding increase in the IF frequency. As this new IF signal approaches the PLL V output frequency, the phase comparator output pulse width becomes narrower, until it is essentially a constant 5 Vdc. Q5 and Q2 turn off, the voltage rise in C19 stops at a new higher level, and the VCXO frequency stabilizes. The two phase comparator inputs are again equal.

Assume that the PLL V output decreases in frequency. This time the U1 output at TP2 will pulse low (the pulse width being a function of the difference in frequency at the inputs.) Q3 turns on and C19 now has a low impedance discharge path to ground. As the C19 voltage drops, Q1 conduction decreases, and the voltage across R4 decreases. This forces the VCXO to decrease in frequency which causes a corresponding decrease in the IF frequency. As the two U1 inputs become equal, the negative pulses at TP2 become narrower, until an essentially 5 Vdc level exists. Q3 turns off, holding the C19 voltage and consequently the R4 voltage at a new lower level. The VCXO stops decreasing and also rests at a new lower frequency.

### 3.3 VCO Operation and Control

A change pump circuit consisting of Q2, Q3, Q5, and associated components in conjunction with filter network C19-R6 convert the two phase comparator pulse outputs into an analog dc control voltage. Buffer amplifier Q1 applies this control voltage to varactor diodes CR1 and CR2 in the VCXO circuit. As the capacitance of these diodes changes due to control voltage fluctuations, JFET Hartley oscillator stage Q6 shifts in frequency. This oscillator stage is crystal controlled by Y1 and operates at 20.025 to 20.030 MHz, which is one-half the desired output frequency range. Therefore X2 multiplier stage Q4 is used to produce the desired VCXO range of 40.050 to 40.060 MHz. A control voltage of approximately 5 Vdc will tune the VCXO to produce 40.050 MHz at J3, while a control voltage of 10 Vdc will tune it to 40.060 MHz.

VCXO output is applied through an attenuator network to J3 at a level of -6 dBm and on to PLL III Assembly A8. It is also applied to 10 dB amplifier stage Q7 and Q8 which function as a local oscillator (LO) amplifier for U3. This stage provides a +7 dBm LO injection to U3, pin 8, to complete the feedback loop.

## 4. BITE TEST CIRCUITS

Lock detector Q9 monitors the status of phase comparator U1 outputs at TP2 and TP3. If either output pulses low and remains low for a period exceeding the time constants of C57 and R38, the appropriate diode will conduct. Q9 will turn on and the voltage across R41 will increase from 0 to +5 Vdc indicating an out of lock condition. This immediately flags BITE monitoring circuits on Control Assembly A14. A front panel fault light indicator will turn on.

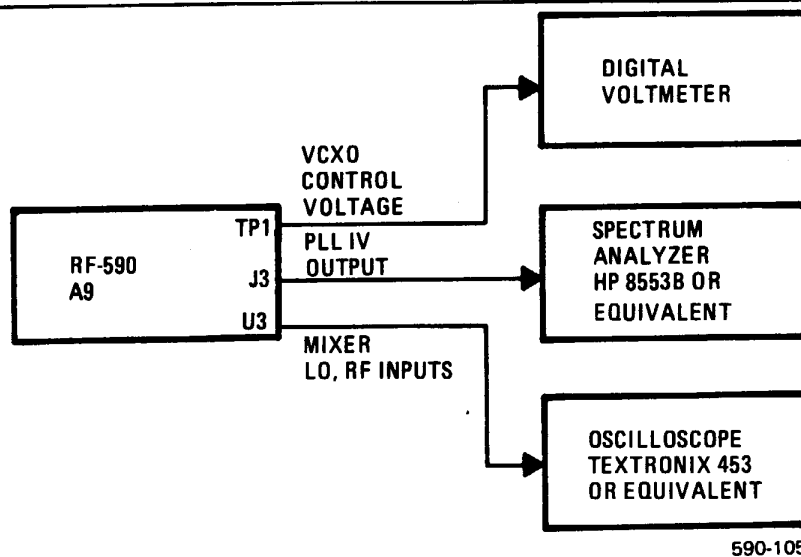
## 5. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. All tests should be performed with all connections in normal contact, unless otherwise specified.

### 5.1 X2 Multiplier, LO Amplifier, and RF Amplifier Alignment

Perform the following procedure to align the X2 Multiplier, LO, and RF amplifiers:

- a. Connect equipment as shown in figure 1.
- b. Set receiver to 00.000500 MHz.
- c. Monitoring TP1, adjust C23 for 7.5 Vdc.
- d. Monitoring J3, adjust T5 and T3 for maximum output level at approximately 40.055 MHz. Level should be -6 dBm  $\pm$  3 dB.
- e. Monitoring mixer U3 LO input at pin 8, adjust L10 and T4 for maximum level at approximately 40.455 MHz. Level should be approximately 1.25 Vpp  $\pm$  .5 volts.



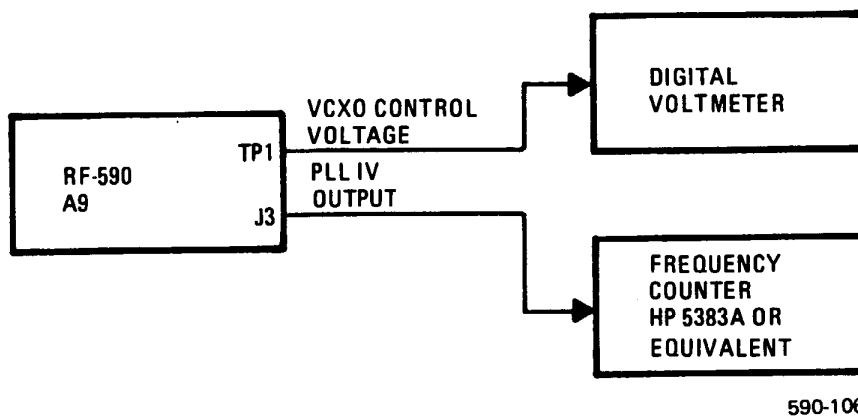
**Figure 1. X2 Multiplier, LO, and RF Amplifier Alignment**

- f. Monitoring mixer U3 RF input at R28, adjust T2 for a maximum level at 40.000 MHz. Level should be .75 Vpp ± .5 volts. Test is complete.

## 5.2 VCXO Alignment

Perform the following procedure to align the VCXO:

- a. Connect equipment as shown in figure 2.



**Figure 2. VCXO Alignment**

- b. Set receiver to 00.000500 MHz. Adjust C23 for 7.5 Vdc.
- c. Check that the PLL IV output frequency (as a function of the receiver tune frequency) agrees with table 2.



Table 2. VCXO Alignment

Receiver Tune Frequency, MHz	PLL IV Output Frequency, MHz	Approximate TP1 Voltage, Vdc
00.000000	40.060	10.0
00.000500	40.055	7.5
00.000999	40.050	5.0

- d. Fully reconnect the A9 assembly to the RF-590. Initiate BITE self-test. Receiver must pass all tests associated with A9 assembly. Test is complete.

## 6. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in PLL IV Assembly A9. When ordering parts from the factory, include a full description of the part. Use figure 3, PLL IV Assembly A9 Component Location Diagram to identify parts.

## 7. SCHEMATIC DIAGRAM

Figure 4 is the PLL IV Assembly A9 schematic diagram.

Table 3. PLL IV Assembly A9 Parts List (PL 10073-4400)

Ref. Desig.	Part Number	Description
	10073-4400	PWB, PLL 4
	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	C26-0025-100	CAP 10UF 20% 25V TANT
C6	CK05BX102M	CAP 1000PF 20% 200V CER
C7	CK05BX102M	CAP 1000PF 20% 200V CER
C8	CM06FD102J03	CAP 1000PF 5% 500V MICA
C9	C26-0025-100	CAP 10UF 20% 25V TANT
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	C26-0025-100	CAP 10UF 20% 25V TANT
C16	C26-0025-100	CAP 10UF 20% 25V TANT

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Table 3. PLL IV Assembly A9 Parts List (PL 10073-4400) (Cont.)

Ref. Desig.	Part Number	Description
C17	M39014/01-1535	CAP .01UF 20% 100V CER
C18	C26-0025-339	CAP 3.3UF 20% 25V TANT
C19	C25-0003-004	CAP 0.33UF 10% 50V TANT
C20	C26-0025-100	CAP 10UF 20% 25V TANT
C21	CM04ED680J03	CAP 68PF 5% 500V MICA
C22	M39014/01-1535	CAP .01UF 20% 100V CER
C23	C85-0001-002	CAP 1.0-10PF 250V
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/01-1535	CAP .01UF 20% 100V CER
C26	M39014/01-1535	CAP .01UF 20% 100V CER
C27	CM04ED470J03	CAP 47PF 5% 500V MICA
C28	M39014/01-1535	CAP .01UF 20% 100V CER
C29	M39014/02-1320	CAP .47UF 10% 50V CER-R
C30	CK05BX102M	CAP 1000PF 20% 200V CER
C31	M39014/01-1535	CAP .01UF 20% 100V CER
C32	CM04CD010D03	CAP 1PF +-.5PF 500V MICA
C33	CM04ED470J03	CAP 47PF 5% 500V MICA
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	CM04ED510J03	CAP 51PF 5% 500V MICA
C36	M39014/01-1535	CAP .01UF 20% 100V CER
C37	M39014/01-1535	CAP .01UF 20% 100V CER
C38	M39014/01-1535	CAP .01UF 20% 100V CER
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/01-1535	CAP .01UF 20% 100V CER
C41	M39014/01-1535	CAP .01UF 20% 100V CER
C42	C26-0025-100	CAP 10UF 20% 25V TANT
C43	CM04ED300J03	CAP 30PF 5% 500V MICA
C44	CM04ED330J03	CAP 33PF 5% 500V MICA
C45	M39014/01-1535	CAP .01UF 20% 100V CER
C46	M39014/01-1535	CAP .01UF 20% 100V CER
C47	M39014/02-1310	CAP .1UF 10% 100V CER-R
C48	M39014/02-1310	CAP .1UF 10% 100V CER-R
C49	M39014/01-1535	CAP .01UF 20% 100V CER
C50	C-0912	CAPACITOR
C51	C-0911	200V .01MFD TUBE
C52	CM06FD272J03	CAP 2700PF 5% 500V MICA
C53	CM06FD272J03	CAP 2700PF 5% 500V MICA
C54	CM06FD272J03	CAP 2700PF 5% 500V MICA
C55	C-0912	CAPACITOR
C56	C-0912	CAPACITOR
C57	C25-0001-301	CAP 1.0UF 20% 20V TANT
C59	CM04ED270J03	CAP 27PF 5% 500V MICA
C60	M39014/01-1535	CAP .01UF 20% 100V CER
C61	M39014/01-1535	CAP .01UF 20% 100V CER
CR1	10073-7118	DIODE, SILICON, HYPERABRUPT

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Table 3. PLL IV Assembly A9 Parts List (PL 10073-4400) (Cont.)

Ref. Desig.	Part Number	Description
CR2	10073-7118	DIODE, SILICON, HYPERABRUPT
CR4	1N3064	DIODE 75mA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N3064	DIODE 75mA 75V SW
J1	J46-0032-006	HDR 6 PIN 0.100" SR
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
L1	L08-0001-001	CHOKE W B 50 MHZ
L2	L08-0001-001	CHOKE W B 50 MHZ
L3	MS14046-9	COIL 27UH 10% FXD RF
L4	MS75084-17	COIL 27.0UH 10% FXD RF
L5	MS75084-3	COIL 1.8UH 10% FXD RF
L6	MS75084-17	COIL 27.0UH 10% FXD RF
L7	MS75084-6	COIL 3.3UH 10% FXD RF
L8	MS90538-8	COIL 68UH 5% FXD RF
L9	MS90538-8	COIL 68UH 5% FXD RF
L10	10073-7011	TRANSFORMER, RF, VARIABLE
Q1	Q05-0001-000	XSTR JFET N-CH
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	2N2222	XSTR SS/GP NPN TO-18
Q4	2N2369	XSTR SS/RF NPN
Q5	2N2222	XSTR SS/GP NPN TO-18
Q6	Q35-0003-000	XSTR U310 JFET HIGH GM
Q7	2N5109	XSTR RFPWR NPN TO-39
Q8	Q35-0003-000	XSTR U310 JFET HIGH GM
Q9	2N2907	XSTR SS/GP PNP TO-18
Q10	Q35-0003-000	XSTR U310 JFET HIGH GM
R1	R65-0003-201	RES 200 5% 1/4W CAR FILM
R2	R65-0003-201	RES 200 5% 1/4W CAR FILM
R3	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R4	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R5	R65-0003-201	RES 200 5% 1/4W CAR FILM
R6	RN55D1211F	RES,1210 1% 1/8W MET FLM
R7	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R8	R65-0003-121	RES 120 5% 1/4W CAR FILM
R9	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R10	RN55D3321F	RES,3320 1% 1/8W MET FLM
R11	R65-0003-201	RES 200 5% 1/4W CAR FILM
R12	R65-0003-101	RES 100 5% 1/4W CAR FILM
R13	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R14	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R15	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R16	R65-0003-911	RES 910 5% 1/4W CAR FILM
R17	R65-0003-101	RES 100 5% 1/4W CAR FILM

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Table 3. PLL IV Assembly A9 Parts List (PL 10073-4400) (Cont.)

Ref. Desig.	Part Number	Description
R18	R65-0003-101	RES 100 5% 1/4W CAR FILM
R19	R65-0003-470	RES 47 5% 1/4W CAR FILM
R20	R65-0003-470	RES 47 5% 1/4W CAR FILM
R21	R65-0003-201	RES 200 5% 1/4W CAR FILM
R22	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R23	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R24	R65-0003-511	RES 510 5% 1/4W CAR FILM
R25	R65-0003-471	RES 470 5% 1/4W CAR FILM
R26	R65-0003-390	RES 39 5% 1/4W CAR FILM
R27	R65-0003-121	RES 120 5% 1/4W CAR FILM
R28	R65-0003-101	RES 100 5% 1/4W CAR FILM
R29	R65-0003-750	RES 75 5% 1/4W CAR FILM
R30	R65-0003-101	RES 100 5% 1/4W CAR FILM
R31	R65-0003-101	RES 100 5% 1/4W CAR FILM
R32	R65-0003-101	RES 100 5% 1/4W CAR FILM
R33	R65-0003-510	RES 51 5% 1/4W CAR FILM
R34	R65-0003-750	RES 75 5% 1/4W CAR FILM
R35	RN55D1001F	RES,1000 1% 1/8W MET FLM
R36	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R37	R65-0003-470	RES 47 5% 1/4W CAR FILM
R38	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R39	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R40	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R41	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R42	R65-0003-471	RES 470 5% 1/4W CAR FILM
R43	R65-0003-101	RES 100 5% 1/4W CAR FILM
T1	10073-7008	TRANSFORMER, RF, FIXED
T2	10073-7012	TRANSFORMER, RF, VARIABLE
T3	10073-7015	TRANSFORMER, RF, VARIABLE
T4	10073-7011	TRANSFORMER, RF, VARIABLE
T5	10073-7011	TRANSFORMER, RF, VARIABLE
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	IC-0430	IC MC4044 CERAMIC CMOS
U2	I20-0005-001	IC LM211H COMPARATOR
U3	I51-0003-003	MIXER DB 50mW 500MHZ
VR1	1N5236	DIODE 7.5V 20% .5W ZENER
VR2	I11-0001-001	IC VR 7805 + 5V 1.5A 4%
Y1	10073-7039	CRYSTAL, 20.0275MHZ

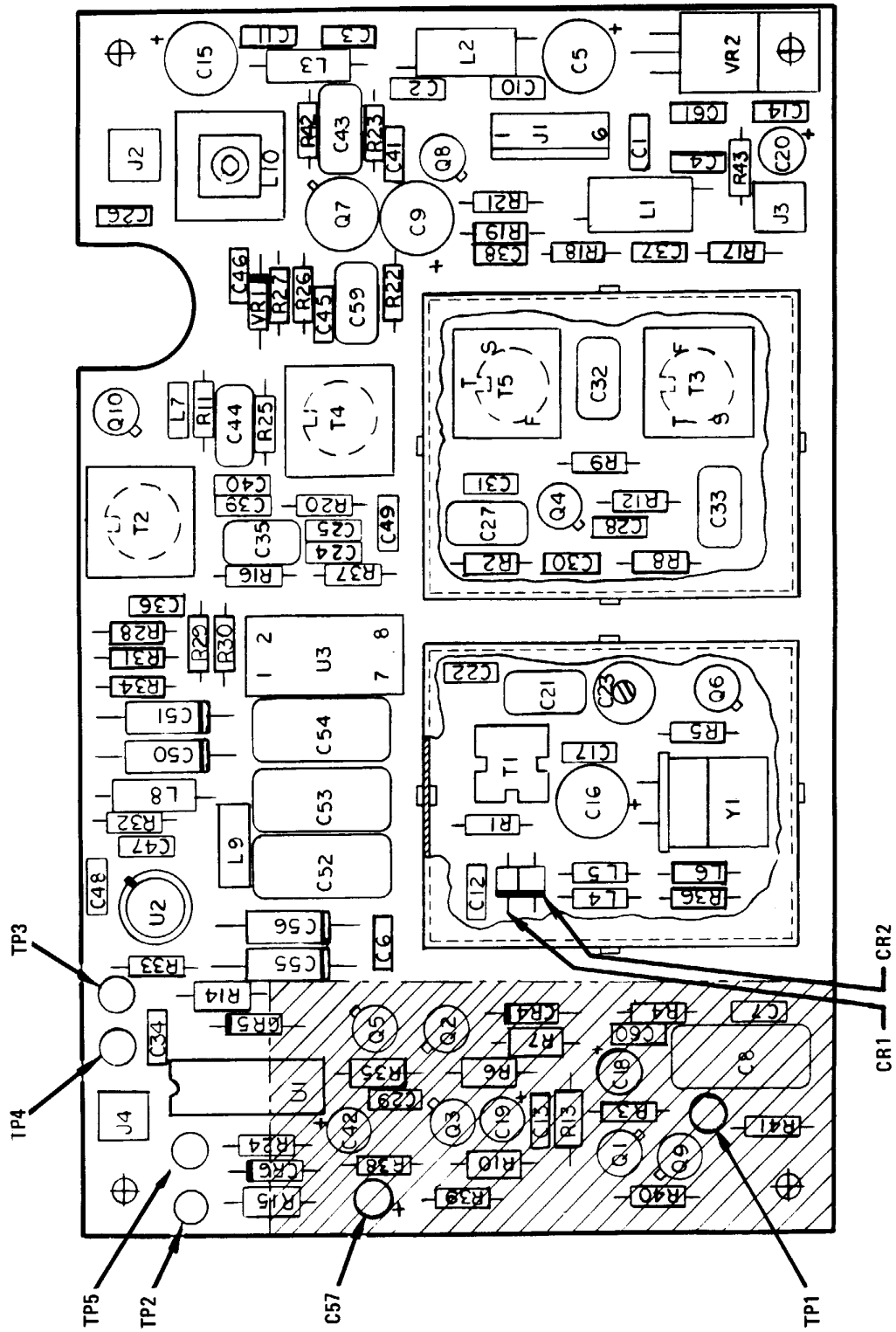


Figure 3. PLL IV Assembly A9 Component Location Diagram (10073-4400, Rev. E)

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NO. DESIGNATION.  
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S ARE REFERENCE ONLY.  
SEE PART NO. IN PARTS LIST.  
IN MICROMEHRES.

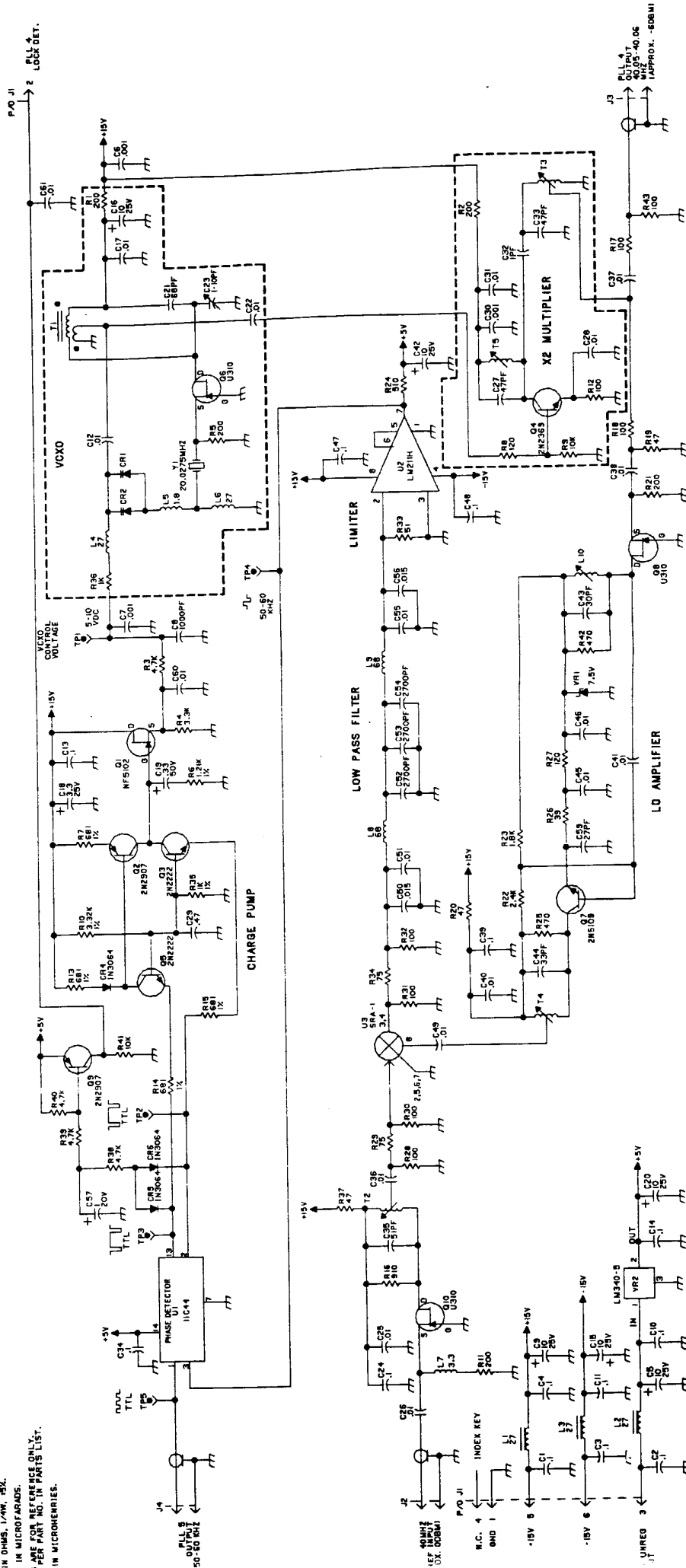
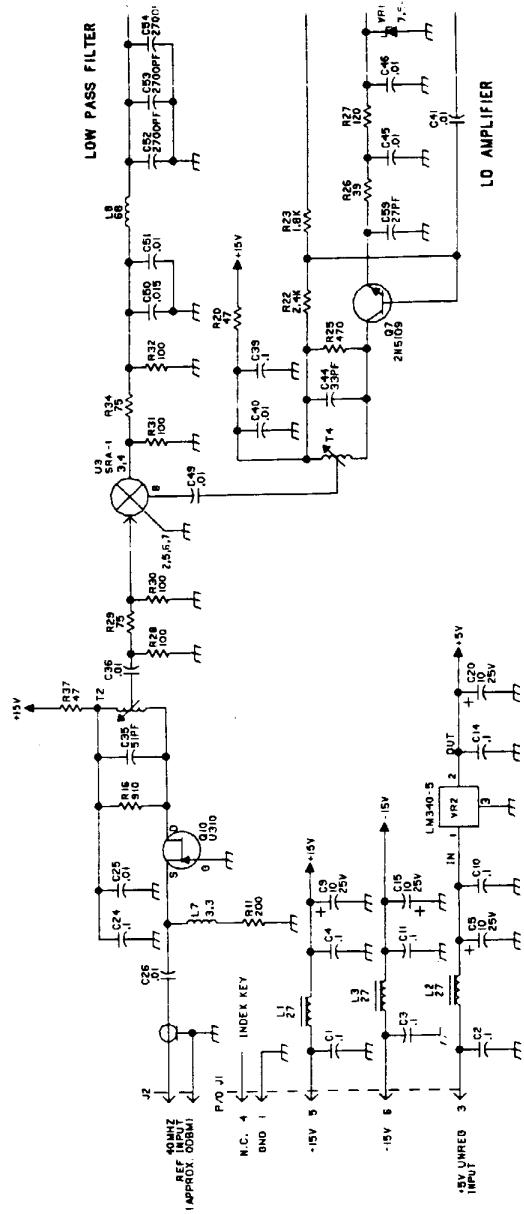
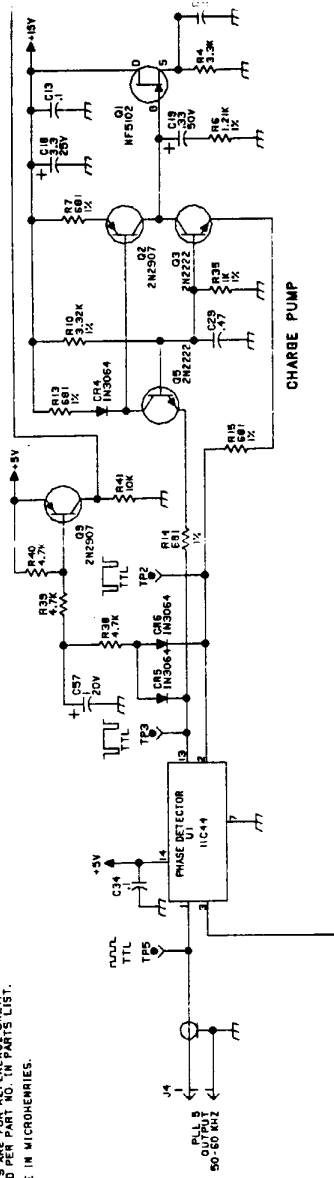


Figure 4. PLL IV Assembly A9 Schematic  
Diagram (10073-4401, Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/MW, -5%. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.



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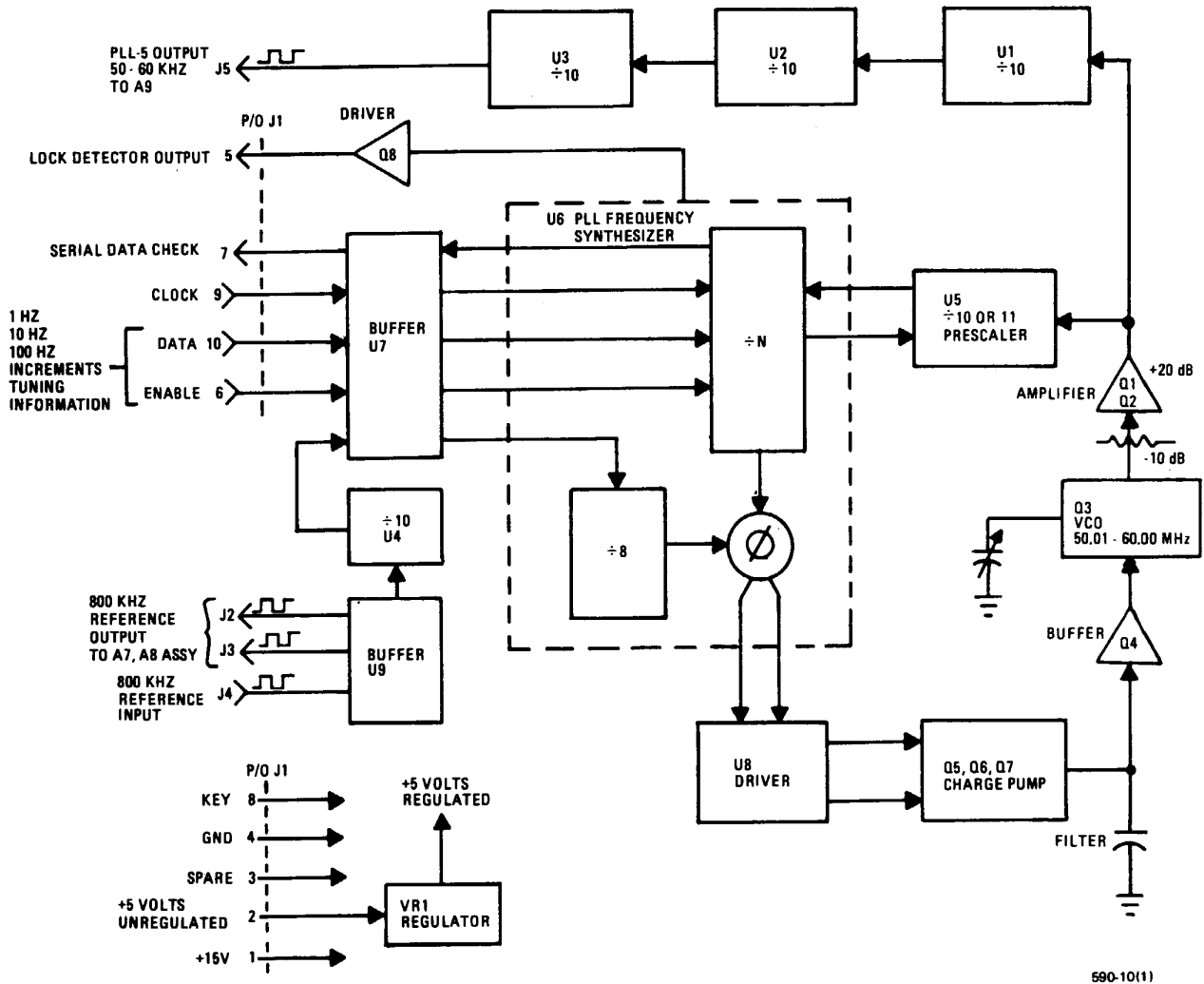
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590-10(1)

PLL V Assembly A10 Functional Block Diagram

**1. GENERAL DESCRIPTION**

PLL V Assembly A10 is a single phase locked loop synthesizer that ultimately provides the 1 Hz, 10 Hz, and 100 Hz tuning increments as chosen by the RF-590 front panel frequency selection controls.

Frequency select input data is applied to the assembly in serial data form under Control Board Assembly A14 microprocessor control. A10 output to PLL IV Assembly A9 is a variable 50 to 60 kHz signal in 10 Hz controllable steps. Since 1000 frequency steps are possible, the net results of A10 operation (after further translation to 1 Hz increments in the synthesizer chain) are 1 Hz, 10 Hz, and 100 Hz tuning increments in the LO no. 1 output.

**2. INTERFACE CONNECTIONS**

Table 1 details the various input/output connections and other relevant data.

**Table 1. PLL V Assembly Interface Connections**

Connector	Function	Characteristics
J1-1	+15 Volts	Approximately 25 mA
J1-2	+5 Volts unregulated	Approximately 240 mA
J1-3	Spare	
J1-4	Ground	
J1-5	Lock Detector Output	+5 Vdc = unlocked, 0 Vdc = locked, P/O BITE Test
J1-6	Enable	+ going pulse = Enabled
J1-7	Serial Data Check	P/O BITE Test, +5 Vdc = ok
J1-8	Key	
J1-9	Clock	TTL, 750 kHz
J1-10	Data	Serial TTL
J2	800 kHz Reference Output	TTL
J3	800 kHz Reference Output	TTL
J4	800 kHz Reference Input	TTL
J5	PLL-V Output	TTL, 50-60 kHz

### 3. CIRCUIT DESCRIPTION

#### NOTE

A10 operation is similar in operation to the general divide by N PLL and charge pump circuits described in section 4. A review of section 4 at this point would aid in the understanding of A10 operation.

#### 3.1 Reference Generation

800 kHz from Reference Generator Assembly A12 enters PLL V Assembly A10 at J4. This signal is buffered via TTL NAND GATES in U9 and directed through J2 and J3 to the A7 and A8 assemblies. It is also routed to divide by 10 counter U4 where it is divided down to 80 kHz. This 80 kHz signal is applied via buffer U7 to a divide by 8 counter internal to U6 to produce a 10 kHz reference signal. Since this has been derived ultimately from the RF-590 crystal frequency standard via the A12 assembly, stable and accurate A10 operation is assured.

#### 3.2 Divide by Counter

Since the A10 assembly requires a variable 50 to 60 kHz output frequency, a programmable counter has been designed into the VCO feedback path to the Phase Comparator. This counter consists of dual modulus  $\div 10/\div 11$  prescaler U5 and a programmable divide by N counter internal to U6. Together U5 and the programmable portion of U6 create a total division range of  $N = 5001$  to  $N = 6000$ , where N is a function of the setting of the receiver 1, 10, and 100 Hz tuning positions.

The output of the divide by N counter will always attempt to equal the 10.000 kHz reference frequency at the Phase Comparator inputs, despite changes in the divide by N factor due to changing the 1, 10, and/or 100 Hz receiver tuning increments. The VCO frequency will change to accomplish this (in response to command signals generated by the Phase Comparator). The VCO frequency will always equal (N) (reference frequency), or  $(N) (10.000 \text{ kHz}) = 50.01 \text{ MHz}$  to  $60.00 \text{ MHz}$ . Division of this range by 1000 will result in the required A10 output range of 50.01 kHz to 60.00 kHz.

The exact value of N is determined by the value of the 1, 10, and/or 100 Hz receiver tuning positions. This front panel selection causes control assembly A14 to generate a serial data code containing information pertaining to the values of the increments chosen. (This code is applied synchronously with the 750 kHz system clock to U6 whenever the U6 enable line is gated open by A14.) In general,  $N = (6000 - XXX)$ , where XXX is the value of the 100, 10, and 1 Hz positions chosen at the receiver front panel frequency controls.

For example, tuning the RF-590 to 10.401475 MHz would make  $N = (6000 - 475) = 5525$ . The VCO frequency will be  $(N) (\text{reference}) = (5525) (10.000 \text{ kHz}) = 55.25 \text{ MHz}$ . The VCO output is then divided by 1000 to produce the A10 output at 55.25 kHz.

The actual frequency of the A10 output may therefore be calculated from the following formula.  $F = 10 (6000 - XXX) \text{ Hz}$ , where XXX is the value of the receiver 100 Hz, 10 Hz, and 1 Hz tuning increments, respectively.

### 3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 10 kHz reference and the 10 kHz VCO derived signal at the divide by N counter output is accomplished by a Phase Comparator internal to U6. When these two signals are equal in frequency and phase, the Phase Comparator outputs at TP2 and TP3 are essentially 5 Vdc. U8 functions as a buffer for the Phase Comparator to the input of the charge pump circuit, consisting of Q5, Q6, and Q7. This 5 volt level holds Q6 and Q7 off. Consequently, Q5 is also off and the voltage across C24 is at some constant level. This biases Q4 to some specific source current, and the voltage across R16 at TP1 is constant. This VCO control voltage holds the VCO frequency constant, somewhere between 50 and 60 MHz.

Assume that the VCO derived feedback signal at the divide by N counter output is suddenly less than the reference frequency. This is what will happen at the instant the divide by N factor is increased. Since the two Phase Comparator inputs are no longer equal, the Phase Comparator will output a series of negative pulses at TP3. Q7 will turn on, forcing Q5 on. Q5 will start to pump charge into C24, causing Q4 to conduct more current as the voltage across C24 increases. This produces a higher dc level at TP1. The VCO frequency will increase in response to it until the signals at the Phase Comparator inputs are again equal. As the VCO derived signal is approaching the reference frequency, the output pulse width at TP3 will get smaller until the signal is essentially +5 Vdc again. Q7 and Q5 will turn off. The voltage at C24 will rest at this new higher dc value causing the VCO frequency to also rest at its new higher value.

Assume that the VCO feedback signal at the divide by N counter output is suddenly greater than the reference signal (meaning that the divide by N factor has just decreased). The two Phase Comparator inputs are again unequal, but now the Phase Comparator will output the negative pulses at TP2. Q6 will turn on, drawing charge out of C24, and causing the VCO control voltage to drop. Consequently, the VCO will shift lower in frequency, and the VCO derived signal at the Phase Comparator input will again approach the reference frequency. The output pulses will become very narrow, approaching 5 Vdc. Q6 will turn off, and equilibrium at the new lower VCO frequency will be obtained.

### 3.4 VCO Operation and Control

A charge pump circuit consisting of Q5, Q6, Q7, and associated components in conjunction with filters C24 and C25 convert the two Phase Comparator pulse outputs into an analog dc control voltage. Buffer amplifier Q4 applies this control voltage to the varactor diode string in the VCO. The VCO itself is a JFET (Q3) Hartley oscillator stage whose frequency shifts as the capacitance of the varactor diodes changes with changes in control voltage. A net control voltage change of 5 Vdc to 10 Vdc produces a net VCO frequency shift of 50 MHz to 60 MHz. Note also that the 10 volt limit corresponds to  $N = 6000$  while the 5 volt limit corresponds to  $N = 5001$ .

The VCO output is fed through 10 dB attenuator network R10-R11 to a +20 dB gain amplifier stage consisting of Q1, Q2, and associated components. This output is split and sent to divide by N circuit U5 and

U6 and to a divide by 1000 divider chain consisting of U1, U2, and U3. This divider output is therefore at a frequency range of 50.01 to 60 kHz (in 10 Hz increments) and is the PLL V output. This output is fed through J5 to PLL IV Assembly A9 where further signal processing occurs.

### 3.5 BITE Circuits

The A10 assembly contains two circuits for self-test evaluation.

- Lock detector Q8 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by the A14 assembly. It will cause a front panel fault light to appear if the loop ever unlocks.
- Serial Data check that verifies the tuning data from the A14 assembly has been received and properly translated into the correct divide by N factor. A serial data word is sent on the data line (J1 pin 10) and the U6 serial data check line is read back to the A14 assembly (J1 pin 7). If the word has been received and properly decoded, this line will pulse to +5 Vdc. The serial data check occurs automatically, but only when the receiver BITE self-test is actuated.

## 4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. All tests should be performed with all connections in normal contact, unless otherwise specified.

### 4.1 VCO Frequency Adjustment

- a. Connect equipment as shown in figure 1.

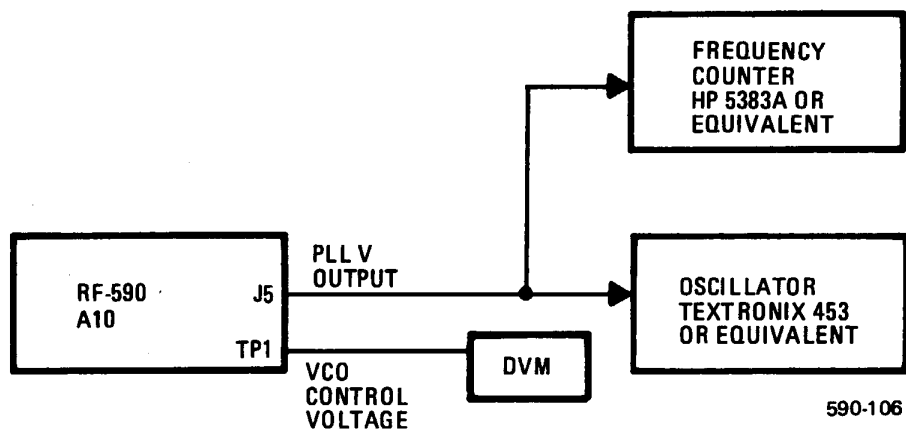


Figure 1. PLL V VCO Adjustment

- b. Set RF-590 frequency to 00.000500 MHz.
- c. Adjust C20 for 7.5 Vdc at TP1. PLL V output vs. receiver tune frequency should agree with table 2. The output waveform should always be a TTL signal.

**Table 2. VCO Frequency Range**

Receiver Tune Frequency, MHz	PLL V Output Frequency, kHz	Approximate TP1 Voltage, Vdc
00.000500	55.00	7.5
00.000000	60.00	10.0
00.000999	50.01	5.0

- d. Fully reconnect the A10 assembly to RF-590. Initiate BITE self-test. Receiver must pass all tests associated with assembly A10. Test is complete.

**5. PARTS LIST**

Table 3 is a comprehensive parts list of all replaceable components in PLL V Assembly A10. When ordering parts from the factory, include a full description of the part. Use figure 2, PLL V Assembly A10 Component Parts Location Diagram to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 3 is the PLL V Assembly A10 schematic diagram.

**Table 3. PLL V Assembly A10 Parts List (PL 10073-4500)**

Ref. Desig.	Part Number	Description
	10073-4500	PWB, PLL 5
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	C26-0025-470	CAP 47UF 20% 25V TANT
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/01-1535	CAP .01UF 20% 100V CER
C5	CK05BX102M	CAP 1000PF 20% 200V CER
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310	CAP .1UF 10% 100V CER-R
C9	M39014/01-1535	CAP .01UF 20% 100V CER
C10	M39014/01-1535	CAP .01UF 20% 100V CER
C11	M39014/01-1535	CAP .01UF 20% 100V CER
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	CK05BX102M	CAP 1000PF 20% 200V CER
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R

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Table 3. PLL V Assembly A10 Parts List (PL 10073-4500) (Cont.)

Ref. Desig.	Part Number	Description
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	C26-0025-680	CAP 68UF 20% 25V TANT
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/01-1535	CAP .01UF 20% 100V CER
C20	C84-0003-008	CAP 3-15PF 200V CER
C21	CK05BX102M	CAP 1000PF 20% 200V CER
C22	CK05BX102M	CAP 1000PF 20% 200V CER
C23	C26-0025-100	CAP 10UF 20% 25V TANT
C24	C25-0003-004	CAP 0.33UF 10% 50V TANT
C25	M39014/01-1546	CAP FXD CER 039UF
C26	C26-0025-470	CAP 47UF 20% 25V TANT
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	C26-0035-109	CAP 1.0UF 20% 35V TANT
C29	C26-0016-151	CAP 150UF 20% 16V TANT
C30	M39014/02-1310	CAP .1UF 10% 100V CER-R
C31	C26-0025-100	CAP 10UF 20% 25V TANT
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	C26-0035-109	CAP 1.0UF 20% 35V TANT
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	C26-0025-470	CAP 47UF 20% 25V TANT
CR1	10073-7118	DIODE, SILICON, HYPERABRUPT
CR2	10073-7118	DIODE, SILICON, HYPERABRUPT
CR3	10073-7118	DIODE, SILICON, HYPERABRUPT
CR4	10073-7118	DIODE, SILICON, HYPERABRUPT
CR5	10073-7118	DIODE, SILICON, HYPERABRUPT
CR6	10073-7118	DIODE, SILICON, HYPERABRUPT
CR7	10073-7118	DIODE, SILICON, HYPERABRUPT
CR8	10073-7118	DIODE, SILICON, HYPERABRUPT
CR9	1N6263	DIODE, HOT CARRIER
CR10	1N3064	DIODE 75mA 75V SW
CR11	10073-7118	DIODE, SILICON, HYPERABRUPT
CR12	10073-7118	DIODE, SILICON, HYPERABRUPT
J1	J46-0032-010	HDR 10 PIN 0.100" SR
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J-0031	CONN SMB VERT PCB F

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Table 3. PLL V Assembly A10 Parts List (PL 10073-4500) (Cont.)

Ref. Desig.	Part Number	Description
L1	MS14046-9	COIL 27UH 10% FXD RF
L2	MS75084-3	COIL 1.8UH 10% FXD RF
L3	MS75084-10	COIL 6.8UH 10% FXD RF
L4	L08-0001-001	CHOKE W B 50 MHZ
Q1	Q35-0003-000	XSTR U310 JFET HIGH GM
Q2	2N2369	XSTR SS/RF NPN
Q3	Q35-0003-000	XSTR U310 JFET HIGH GM
Q4	Q05-0001-000	XSTR JFET N-CH
Q5	2N2907	XSTR SS/GP PNP TO-18
Q6	2N2222	XSTR SS/GP NPN TO-18
Q7	2N2222	XSTR SS/GP NPN TO-18
Q8	2N2907	XSTR SS/GP PNP TO-18
R1	R65-0003-201	RES 200 5% 1/4W CAR FILM
R2	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-270	RES 27 5% 1/4W CAR FILM
R5	R65-0003-201	RES 200 5% 1/4W CAR FILM
R6	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R7	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R8	R65-0003-100	RES 10 5% 1/4W CAR FILM
R9	R65-0003-151	RES 150 5% 1/4W CAR FILM
R10	R65-0003-101	RES 100 5% 1/4W CAR FILM
R11	R65-0003-201	RES 200 5% 1/4W CAR FILM
R12	R65-0003-101	RES 100 5% 1/4W CAR FILM
R13	R65-0003-470	RES 47 5% 1/4W CAR FILM
R14	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R15	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R16	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R17	RN55D3651F	RES,3650 1% 1/8W MET FLM
R18	R65-0003-470	RES 47 5% 1/4W CAR FILM
R19	R65-0003-470	RES 47 5% 1/4W CAR FILM
R20	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R21	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R22	RN55D9091F	RES,9090 1% 1/8W MET FLM
R23	RN55D3321F	RES,3320 1% 1/8W MET FLM
R24	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R25	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R31	R65-0003-103	RES 10K 5% 1/4W CAR FILM
T1	10073-7002	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"



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Table 3. PLL V Assembly A10 Parts List (PL 10073-4500) (Cont.)

Ref. Desig.	Part Number	Description
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	165-0004-001	IC 12013 PLASTIC ECL
U2	105-0000-090	IC 74LS90 PLASTIC TTL
U3	105-0000-090	IC 74LS90 PLASTIC TTL
U4	105-0000-090	IC 74LS90 PLASTIC TTL
U5	165-0004-001	IC 12013 PLASTIC ECL
U6	170-0002-001	IC MC145156 PLASTIC CMOS
U7	101-0000-019	IC 4050B PLASTIC CMOS
U8	105-0000-000	IC 74LS00 PLASTIC TTL
U9	105-0000-000	IC 74LS00 PLASTIC TTL
VR1	111-0001-001	IC VR 7805 + 5V 1.5A 4%

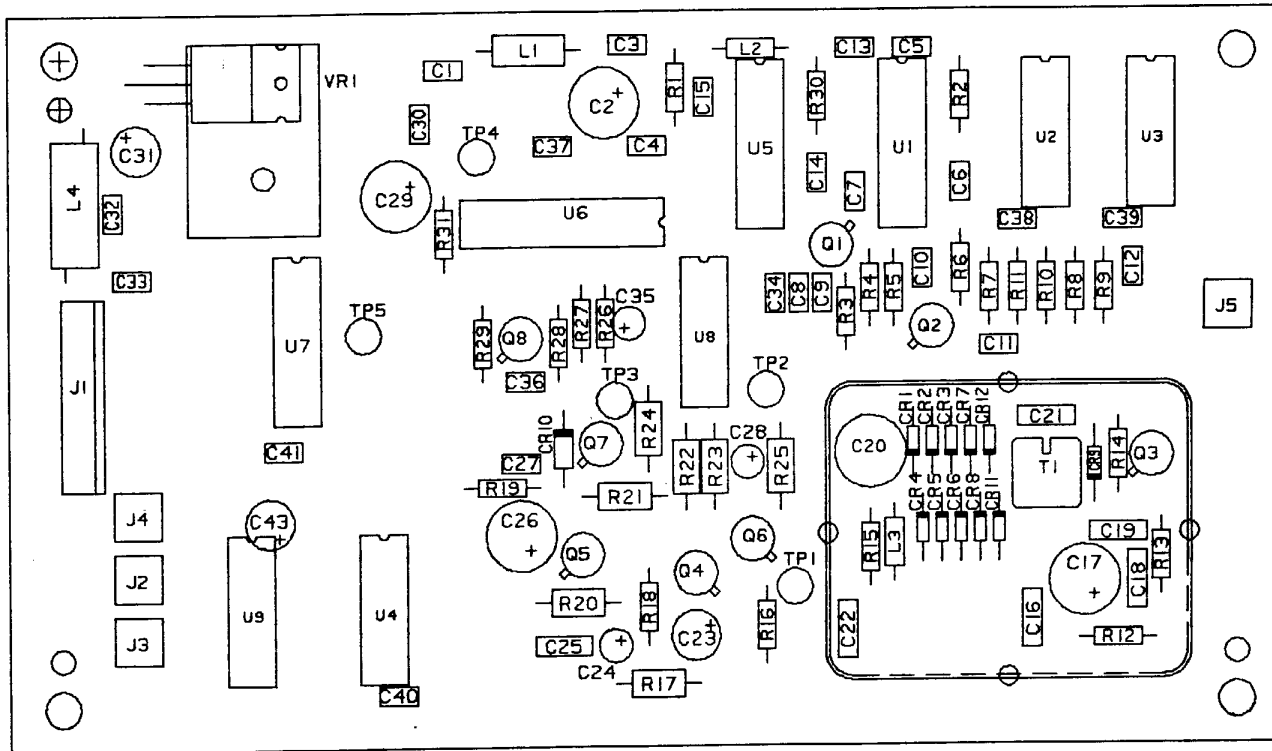
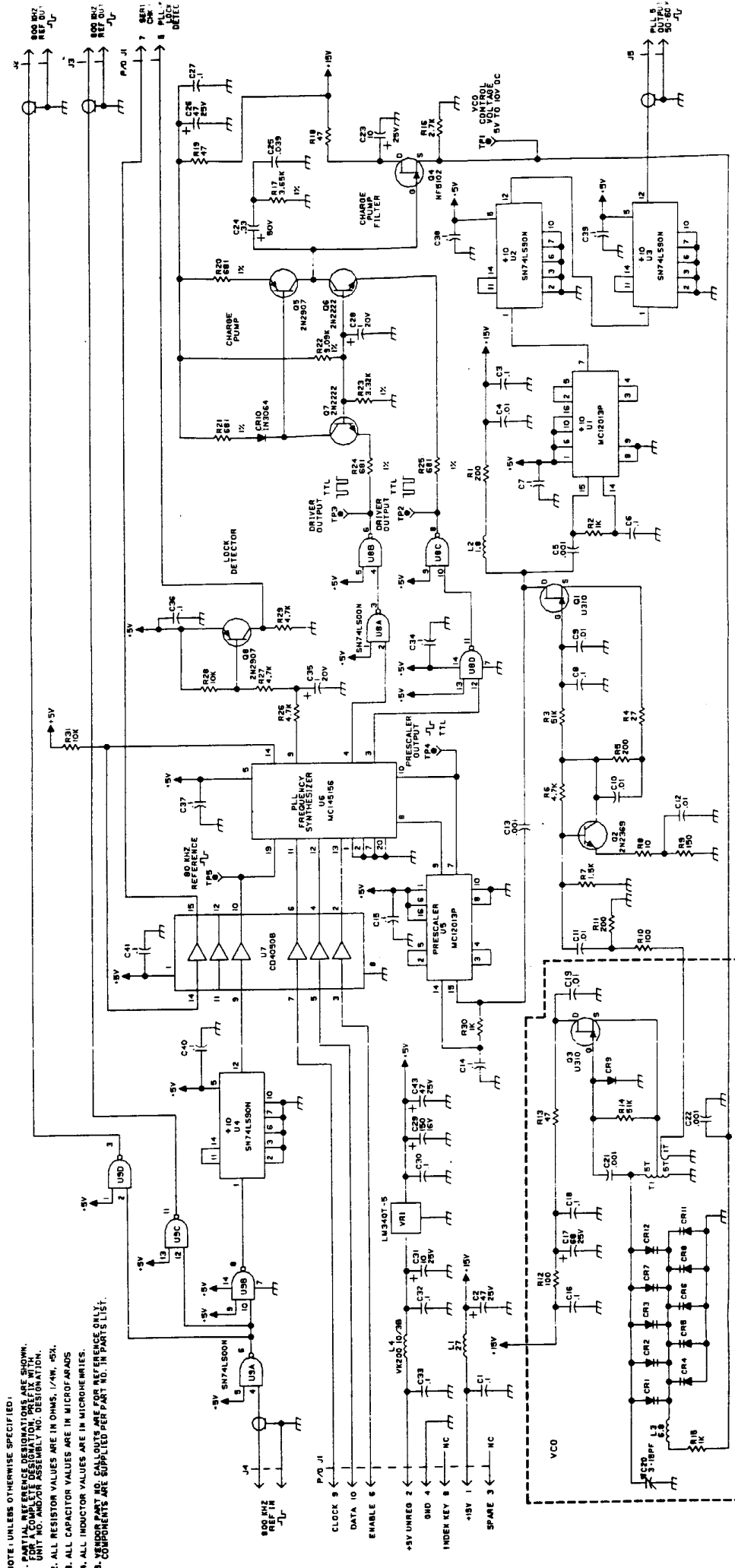


Figure 2. PLL V Assembly A10 Component Location Diagram (10073-4500, Rev. C)

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NOTE: UNLESS OTHERWISE SPECIFIED:  
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 PART NO. AND/OR ASSEMBLY NO. DESIGNATION.  
 2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, .5V.  
 3. ALL CAPACITOR VALUES ARE IN MICROFARADS.  
 4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.  
 5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY.  
 6. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

Figure 3. PLL V Assembly A10 Schematic Diagram (10073-4501, Rev. E)

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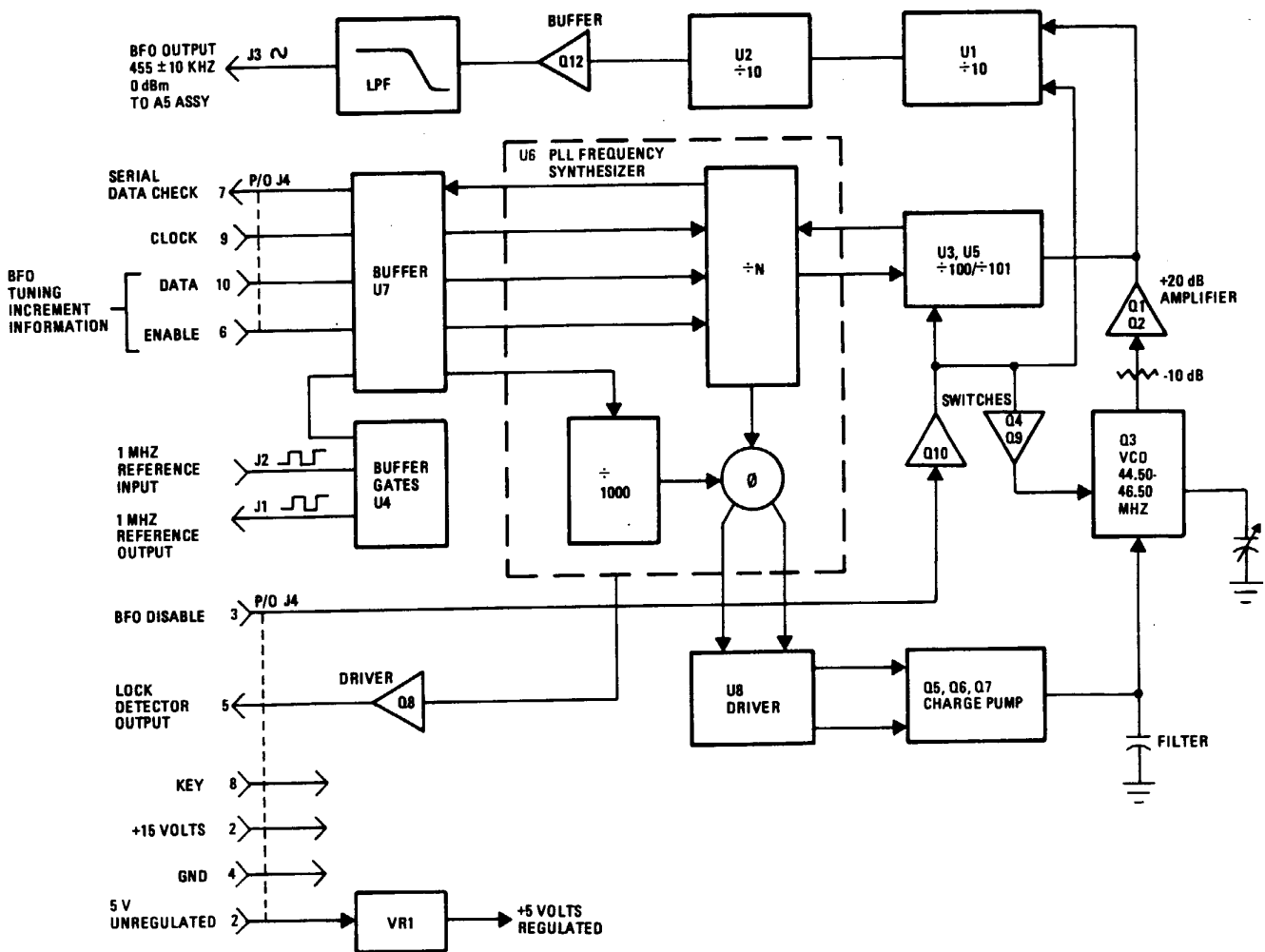
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**BFO Assembly A11 Functional Block Diagram**

## 1. GENERAL DESCRIPTION

The A11 BFO Synthesizer Assembly is a single phase locked loop synthesizer that provides the BFO offset injection required for proper CW or SB reception. The BFO range is  $\pm 10$  kHz around 455 kHz. It is selected via RF-590 BFO selection controls in 10 Hz increments.

Frequency select input data is applied to the A11 assembly in serial data form under Control Board Assembly A14 microprocessor control. A11 output is applied to IF/Audio Assembly A5 where it mixes with the second IF of 455 kHz to permit proper CW and SB demodulation.

## 2. INTERFACE CONNECTIONS

Table 1 lists the various input/output connections and other relevant data.

**Table 1. A11 BFO Synthesizer Interface Connections**

Connector	Function	Characteristics
J1	1 MHz Reference Output	TTL
J2	1 MHz Reference Input	TTL
J3	BFO Output	455 kHz $\pm$ 10 kHz, 0 dBm
J4-1	+15 V	Approximately 20 mA
J4-2	+5.0 V Unregulated	Approximately 200 mA
J4-3	BFO Disable	+5 V = BFO Disabled
J4-4	GND	
J4-5	Lock Detector Output	P/O BITE, +5 V = Unlocked, 0V = Locked
J4-6	Enable	+ going pulse = Enabled
J4-7	Serial Data Check	P/O BITE Testing, +5 Vdc = ok
J4-8	Key	
J4-9	Clock	TTL, 750 kHz
J4-10	Data	TTL

### 3. CIRCUIT DESCRIPTION

#### NOTE

A11 operation is similar to the general divide by N PLL and charge pump circuits described in section 4. Reviewing section 4 at this point would aid in understanding A11 operation.

#### 3.1 Reference Generation

A 1 MHz signal from Reference Generator Assembly A12 enters the A11 BFO synthesizer at J2. This signal is buffered by TTL NAND gates in U4 and directed to J1, a spare 1 MHz output. It is also routed to a divide by 1000 counter (internal to U6) via buffer stage U7 to produce a 1 kHz reference signal. Since this has been ultimately derived from the RF-590 crystal frequency standard via the A12 assembly, stable and accurate A11 operation is assured.

#### 3.2 Divide by N Counter

Since the A11 assembly requires a variable output frequency ( $455 \text{ kHz} \pm 10 \text{ kHz}$ ), a programmable counter has been incorporated into the VCO feedback path to the phase comparator. This counter consists of dual modulus  $\div 100/\div 101$  prescaler network U5 and U3 and a programmable counter internal to U6. Together this circuit creates a total division range of  $N = 44,500$  to  $N = 46,500$ , where N is a function of the receiver BFO offset tune positions.

The output of the divide by N counter will always attempt to equal the 1 kHz reference frequency at the phase comparator inputs (despite changes in the divide by N factor due to changing the 1 kHz, 100 Hz, and/or 10 Hz BFO offset tuning positions). To accomplish this, VCO frequency will change in response to command signals generated by the phase comparator output. The VCO frequency will always equal  $(N)$  (reference frequency) or  $(N) (1000 \text{ Hz}) = 44.50 \text{ MHz}$  to  $46.50 \text{ MHz}$ .

Selection of a BFO offset frequency from the front panel causes Control Assembly A14 to generate a serial data code containing information about the frequency chosen. This code is applied synchronously with the 750 kHz system clock to U6 whenever the U6 enable line is gated open by A14.

The value of N may be found from the formula,  $N = (45,500 - XXX)$ , where XXX is the  $\pm$  value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tuning positions. For example, tuning the BFO offset to +5.00 kHz would make  $N = 45,500 - (+500) = 45,000$ . The VCO frequency would be  $(N) (\text{reference}) = (45,000) (1000) = 45.00 \text{ MHz}$ . There is a divide by 100 counter at the VCO output, so the BFO output at J3 would be 450 kHz. Note that as the selected BFO offset frequency increases the BFO output frequency must decrease.

In summary, the BFO output frequency may be calculated from the following formula,  $F = 10 (45,500 - XXX) \text{ Hz}$ , where  $\pm XXX$  represents the value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tune frequency.

### 3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 1 kHz reference and the 1 kHz VCO derived signal at the divide by N counter output is accomplished by a phase comparator internal to U6.

When these two signals are equal in frequency and phase, the phase comparator outputs at TP4 and TP5 are essentially 5 Vdc. U8 buffers this level to the charge pump circuit where +5 Vdc on the Q6 and Q7 emitters holds both transistors off. Q5 is also off, and the voltage at TP1 (across C24) is constant. This level holds the VCO frequency constant between 44.5 MHz and 46.5 MHz.

Assume that the division ratio of U3, U5, and U6 is changed so that the VCO derived feedback signal is less than the 1 kHz reference. (This will happen if the divide by N factor increases.) The phase comparator will output a series of negative going pulses at TP4 whose pulse widths are a function of the difference in frequency. Q7 will turn on during these negative periods, and its collector voltage drops. This permits Q5 to turn on and pump charge into C24. This causes the C24 voltage to increase, which in turn causes an increase in the VCO frequency. The VCO frequency increases until the signals at the U6 phase comparator inputs are equal. At this time, the phase comparator output error pulse width will have decreased to an extremely small value. TP4 is essentially at 5 Vdc, Q5 and Q7 turn off, and no further increase in the voltage across C24 will occur. The VCO will therefore rest at a new higher frequency.

Assume that the division ratio changes so the VCO derived feedback signal is greater than the 1 kHz reference. U6 will pulse low at TP5, causing Q6 to turn on. C24 will start to discharge through Q6 to ground, and its voltage drops. This causes the VCO to decrease in frequency until the inputs at the phase comparator are equal. Again, the output error pulse width will have decreased to an extremely small value. TP5 will be at essentially 5 Vdc, Q6 will turn off, the C24 voltage will no longer decrease, and the VCO frequency will rest at this new lower value.

### 3.4 VCO Operation and Control

Buffer stage U8 applies the phase comparator outputs to a charge pump circuit consisting of Q5, Q6, Q7, and associated components followed by filters C24 and C25. This stage converts the two phase comparator pulse outputs into an analog dc control voltage. This control voltage is then applied to the varactor diode string in the VCO. It controls the operating frequency of JFET Hartley oscillator stage Q3. A net control voltage change of 6.5 Vdc to 8.5 Vdc produces a VCO frequency range of 44.500 MHz to 46.500 MHz.

The VCO output is fed through -10 dB attenuator network R10-R11 and to 20 dB gain amplifier stage, Q1 and Q2. The signal is then split and sent to the divide by N circuit U3, U5, and U6 (to complete the feedback loop) and to divide by 100 chain U1 and U2. U2 TLL output at 455 to 465 kHz is applied through buffer stage Q12 to a low pass filter (LPF) network. LPF output is a 455 kHz  $\pm$  10 kHz, 0 dBm sine wave and is fed through J3 to IF/Audio Assembly A5 to become the BFO injection frequency.

BFO disabling occurs whenever the receiver is in any mode other than LSB, USB, ISB, or CW modes. This occurs in response to a +5 Vdc command by the A14 assembly at J4, pin 3. This signal disables the VCO

by turning Q10 on. This turns Q4 on. Q4 then removes base drive to Q9. Q9 turns off and removes the supply voltage from oscillator stage Q3. Also, Q10's on state forward biases diodes CR14 and CR15, which shorts out the signals at the U1 and U5 inputs.

### 3.5 BITE Circuits

The A11 assembly contains two circuits for self-test evaluation.

- Lock detector Q8 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by Control Assembly A14. A front panel fault light will appear if the loop ever unlocks.
- Serial data check that verifies that the tuning data from the A14 assembly has been received and properly translated into the correct divide by N factor. A serial data word is sent by the A14 assembly on the BFO tuning data line (J4 pin 10) and the U6 SW1 output is read at J4, pin 7. If the word has been received and properly decoded, this line will pulse to +5 Vdc. The serial data check test occurs automatically, but only when the receiver BITE self-test is actuated.

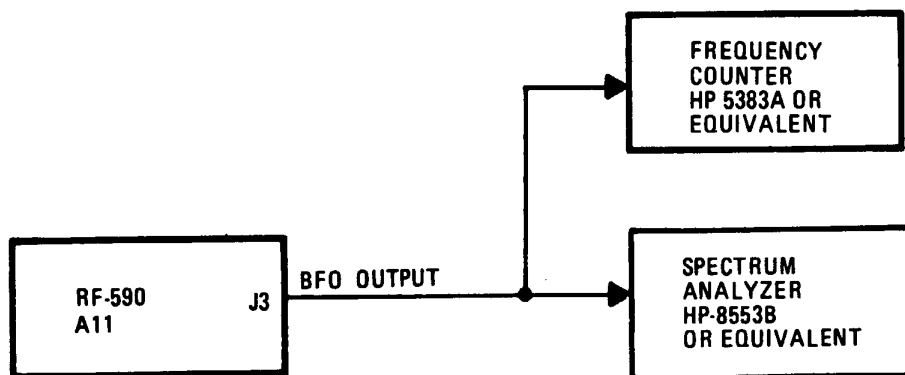
## 4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. A11 tests should be performed with all connections in normal contact, unless otherwise specified.

### 4.1 VCO Adjustment

Perform this procedure to align the VCO.

- a. Connect equipment as shown in figure 1.



590-107

Figure 1. BFO VCO Alignment



**NOTE**

A11J3 mates with A5A1J2 through a hole in the chassis.  
It will be necessary to remove the A5 assembly to gain access to A11J3.

- b. Set RF-590 controls as follows:
  - Frequency to 10.000000 MHz
  - MODE to USB
  - BFO to 0.00 kHz
- c. Monitor TP1 with a digital voltmeter. Adjust C20 for 7.0 Vdc.
- d. Check that the BFO output frequency (as a function of the front panel BFO settings) agree with table 2. (BFO output amplitude should always be 0 dBm  $\pm$  2 dB.)

**Table 2. BFO Frequency Offset**

BFO Offset Frequency Selected	BFO Output Frequency	Approximate Voltage at TP1
0.00 kHz	455.00 kHz	7.0
+9.99 kHz	445.01 kHz	6.0
-9.99 kHz	464.99 kHz	8.0

- e. Fully reconnect the A11 assembly to the RF-590. Initiate BITE self-test. Receiver must pass all tests associated with the A11 assembly. Test is complete.

**5. PARTS LIST**

Table 3 is a comprehensive parts list of all replaceable components in BFO Assembly A11. When ordering parts from the factory, include a full description of the part. Use figure 2, BFO Assembly A11 Component Location Diagram to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 3 is the BFO Assembly A11 schematic diagram.

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Table 3. BFO Assembly A11 Parts List (PL 10073-4600)

Ref. Desig.	Part Number	Description
	10073-4600	PWB
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	C26-0025-470	CAP 47UF 20% 25V TANT
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/01-1535	CAP .01UF 20% 100V CER
C5	CK05BX102M	CAP 1000PF 20% 200V CER
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310	CAP .1UF 10% 100V CER-R
C9	M39014/01-1535	CAP .01UF 20% 100V CER
C10	M39014/01-1535	CAP .01UF 20% 100V CER
C11	M39014/01-1535	CAP .01UF 20% 100V CER
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	CK05BX102M	CAP 1000PF 20% 200V CER
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	C26-0025-680	CAP 68UF 20% 25V TANT
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/01-1535	CAP .01UF 20% 100V CER
C20	C84-0003-004	CAP 9-35PF 200V CER
C21	CK05BX102M	CAP 1000PF 20% 200V CER
C22	CK05BX102M	CAP 1000PF 20% 200V CER
C23	C26-0025-680	CAP 68UF 20% 25V TANT
C24	C25-0003-107	CAP 1.0UF 10% 35V TANT
C25	C25-0003-004	CAP 0.33UF 10% 50V TANT
C26	C26-0025-100	CAP 10UF 20% 25V TANT
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	C25-0001-301	CAP 1.0UF 20% 20V TANT
C29	C26-0016-151	CAP 150UF 20% 16V TANT
C30	M39014/02-1310	CAP .1UF 10% 100V CER-R
C31	C26-0025-100	CAP 10UF 20% 25V TANT
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	C25-0001-301	CAP 1.0UF 20% 20V TANT
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C42	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	6628-0660	CAP 5600PF 5% 300V MICA

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Table 3. BFO Assembly A11 Parts List (PL 10073-4600) (Cont.)

Ref. Desig.	Part Number	Description
C45	CM06FD272J03	CAP 2700PF 5% 500V MICA
C46	CM06FD751J03	CAP 750PF 5% 500V MICA
C47	C-2503	CAP 820PF 2% 300V MICA
C48	6628-0660	CAP 5600PF 5% 300V MICA
C49	CM06FD272J03	CAP 2700PF 5% 500V MICA
C50	M39014/02-1310	CAP .1UF 10% 100V CER-R
C51	M39014/01-1535	CAP .01UF 20% 100V CER
C52	M39014/01-1535	CAP .01UF 20% 100V CER
CR1	10073-7118	DIODE, SILICON, HYPERABRUPT
CR2	10073-7118	DIODE, SILICON, HYPERABRUPT
CR3	10073-7118	DIODE, SILICON, HYPERABRUPT
CR4	10073-7118	DIODE, SILICON, HYPERABRUPT
CR5	10073-7118	DIODE, SILICON, HYPERABRUPT
CR6	10073-7118	DIODE, SILICON, HYPERABRUPT
CR7	10073-7118	DIODE, SILICON, HYPERABRUPT
CR8	10073-7118	DIODE, SILICON, HYPERABRUPT
CR9	10073-7118	DIODE, SILICON, HYPERABRUPT
CR10	10073-7118	DIODE, SILICON, HYPERABRUPT
CR11	1N6263	DIODE, HOT CARRIER
CR12	1N3064	DIODE 75mA 75V SW
CR13	1N3064	DIODE 75mA 75V SW
CR14	1N3064	DIODE 75mA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0032-010	HDR 10 PIN 0.100" SR
L1	MS14046-9	COIL 27UH 10% FXD RF
L2	MS75084-3	COIL 1.8UH 10% FXD RF
L3	MS75084-10	COIL 6.8UH 10% FXD RF
L4	L08-0001-001	CHOKE W B 50 MHZ
L5	MS14046-7	COIL 18UH 10% FXD RF
Q1	Q35-0003-000	XSTR U310 JFET HIGH GM
Q2	2N2369	XSTR SS/RF NPN
Q3	Q35-0003-000	XSTR U310 JFET HIGH GM
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	2N2907	XSTR SS/GP PNP TO-18
Q6	2N2222	XSTR SS/GP NPN TO-18
Q7	2N2222	XSTR SS/GP NPN TO-18
Q8	2N2907	XSTR SS/GP PNP TO-18
Q9	2N2907	XSTR SS/GP PNP TO-18
Q10	2N2222	XSTR SS/GP NPN TO-18
Q11	2N5088	XSTR SS/GP
Q12	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-201	RES 200 5% 1/4W CAR FILM
R2	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

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**Table 3. BFO Assembly A11 Parts List (PL 10073-4600) (Cont.)**

Ref. Desig.	Part Number	Description
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-270	RES 27 5% 1/4W CAR FILM
R5	R65-0003-201	RES 200 5% 1/4W CAR FILM
R6	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R7	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R8	R65-0003-100	RES 10 5% 1/4W CAR FILM
R9	R65-0003-151	RES 150 5% 1/4W CAR FILM
R10	R65-0003-101	RES 100 5% 1/4W CAR FILM
R11	R65-0003-201	RES 200 5% 1/4W CAR FILM
R12	R65-0003-101	RES 100 5% 1/4W CAR FILM
R13	R65-0003-270	RES 27 5% 1/4W CAR FILM
R14	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R15	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R16	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R17	RN55D5621F	RES,5620 1% 1/8W MET FLM
R18	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R19	R65-0003-561	RES 560 5% 1/4W CAR FILM
R20	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R21	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R22	RN55D9091F	RES,9090 1% 1/8W MET FLM
R23	RN55D3321F	RES,3320 1% 1/8W MET FLM
R24	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R25	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R31	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R32	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R33	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R34	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R35	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R36	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R37	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R38	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R39	R65-0003-151	RES 150 5% 1/4W CAR FILM
R40	R65-0003-750	RES 75 5% 1/4W CAR FILM
R41	R65-0003-103	RES 10K 5% 1/4W CAR FILM
T1	10073-7003	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"

Table 3. BFO Assembly A11 Parts List (PL 10073-4600) (Cont.)

Ref. Desig.	Part Number	Description
TP6	J-0072	TP PWB BLU TOP ACCS .080"
U1	165-0004-001	IC 12013 PLASTIC ECL
U2	105-0000-090	IC 74LS90 PLASTIC TTL
U3	105-0000-168	IC 74LS168 PLASTIC TTL
U4	105-0000-000	IC 74LS00 PLASTIC TTL
U5	165-0004-001	IC 12013 PLASTIC ECL
U6	170-0002-001	IC MC145156 PLASTIC CMOS
U7	101-0000-019	IC 4050B PLASTIC CMOS
U8	105-0000-000	IC 74LS00 PLASTIC TTL
VR1	111-0001-001	IC VR 7805 + 5V 1.5A 4%

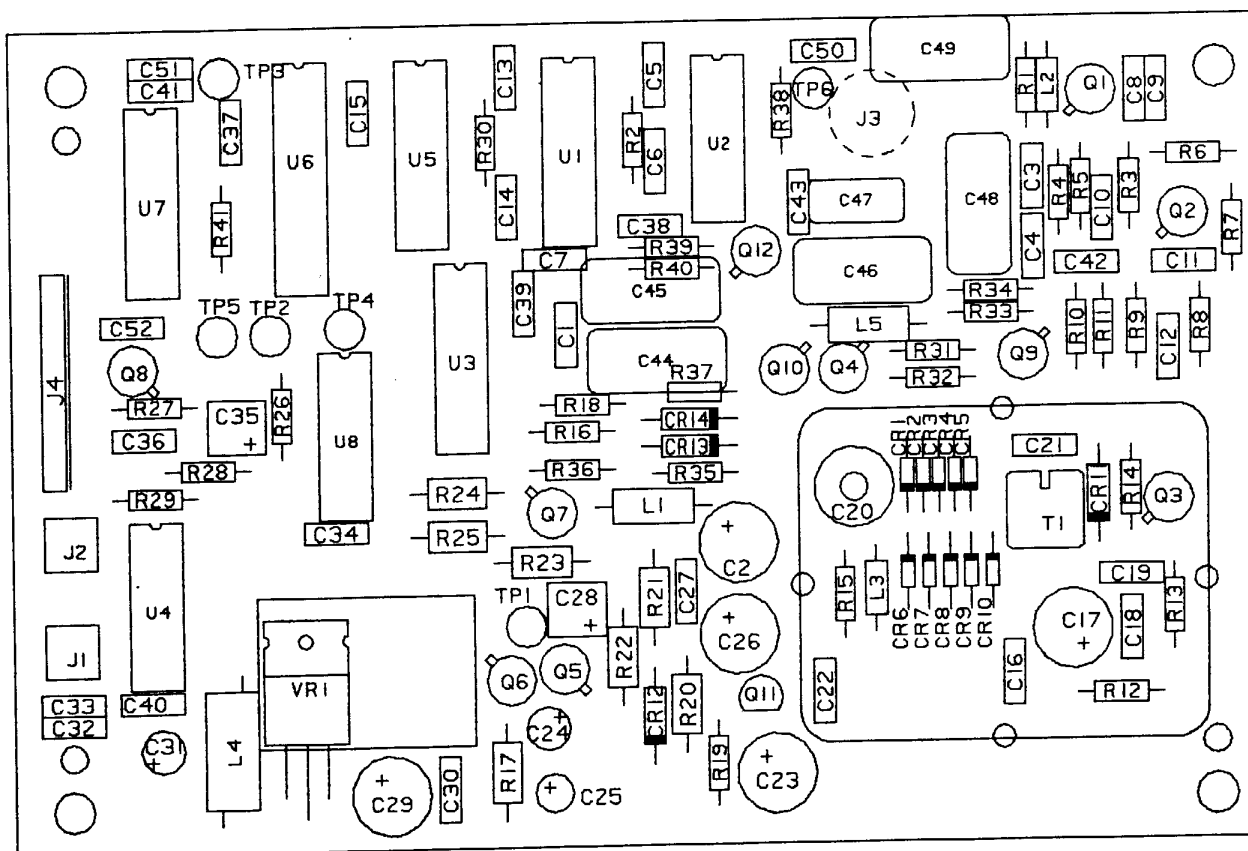


Figure 2. BFO Assembly A11 Component Location Diagram (10073-4600, Rev. C)

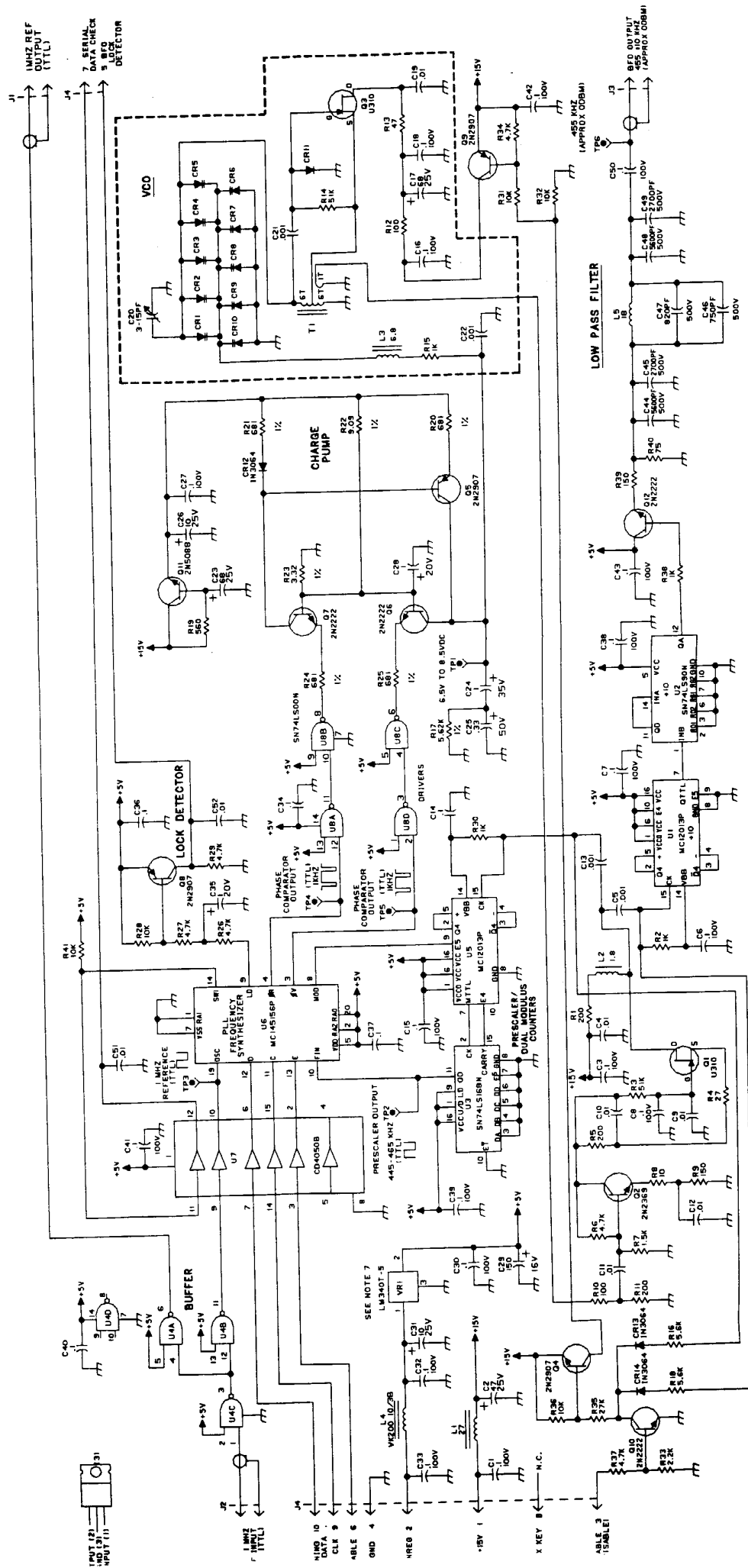


Figure 3. BFO Assembly A11 Schematic Diagram (10073-4601, Rev. F)



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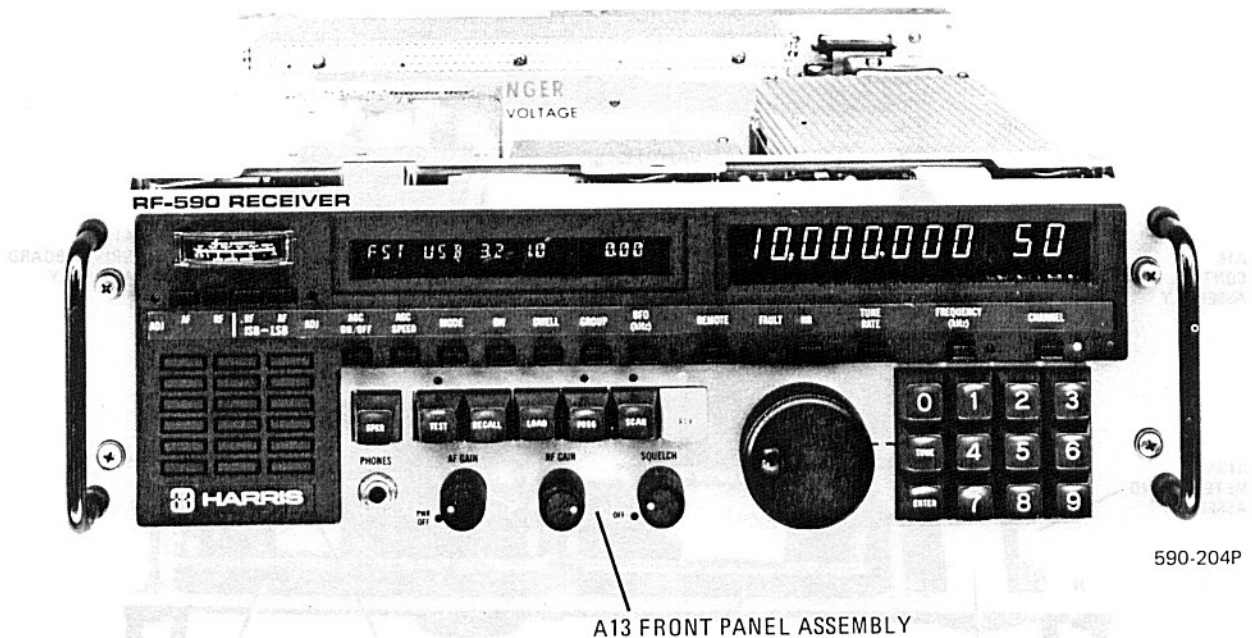
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**1. FRONT PANEL ASSEMBLY A13**

The RF-590 Front Panel Assembly A13 contains control circuits which permit all operator-receiver local interface functions such as tuning, channel selection, AF gain, system status indications, etc.

All operator controls (AF Gain, Squelch, Keypad, Tuning knob, etc) are accessed from the front of the assembly. Figure 3-1 of the Operations section details the location and functions of these controls, and figure 1 is a photograph of the front panel (included for reference).

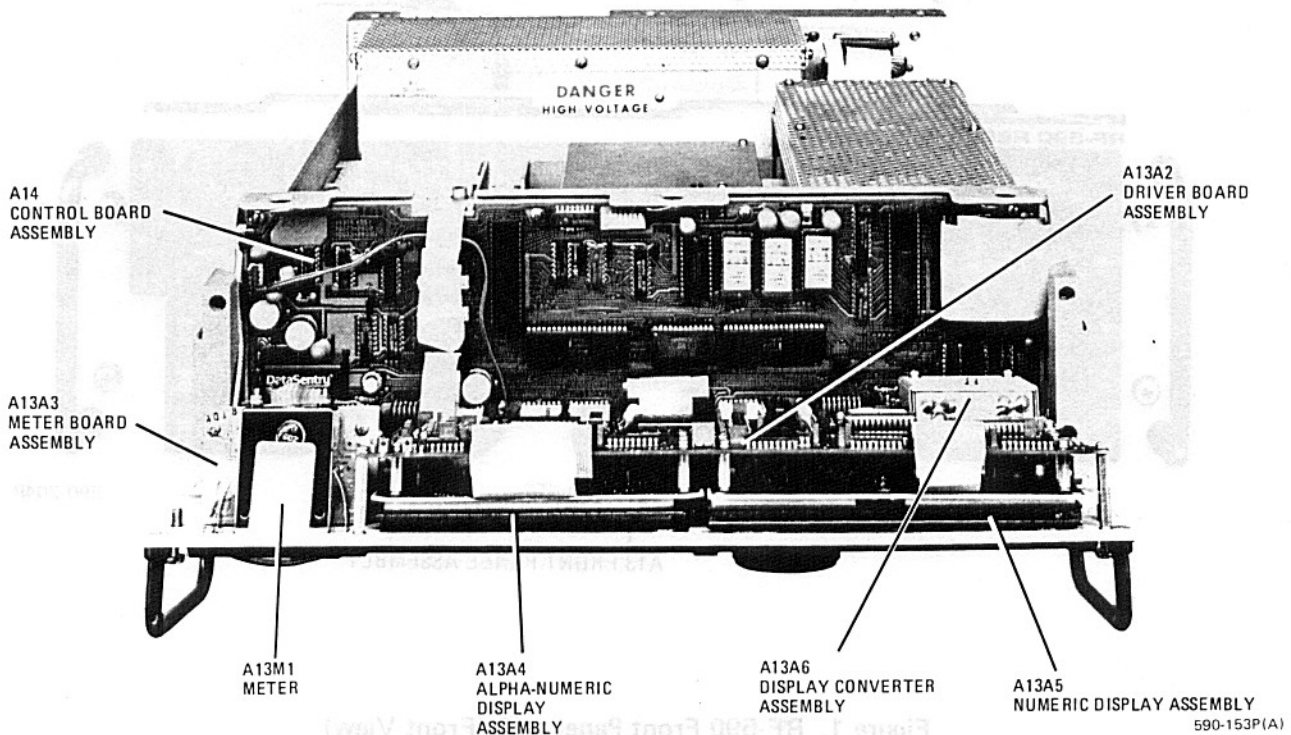


**Figure 1. RF-590 Front Panel A13 (Front View)**

Six major interface assemblies are mounted to the rear of the Front Panel Assembly. They are shown in figure 2. These assemblies are described in section 2 through 7 and listed below.

- Switch Board A13A1
- Driver Board A13A2
- Meter Board A13A3
- Display Board (Alphanumeric) A13A4

- Display Board (Numeric) A13A5
- Converter Assembly A13A6



**Figure 2. RF-590 Front Panel Assembly A13 (Rear View)**

The Front Panel Assembly is normally secured to the RF-590 chassis by four front panel captive screws. Loosening these screws allows the entire assembly to pivot down on hinges (located at two corners). This permits access to any of the items listed above as well as to Control Board Assembly A14 which is mounted behind the front panel.

Table 1 is the Front Panel Assembly A13 parts list.

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**Table 1. Front Panel Assembly A13 Parts List (PL 10073-2000)**

Ref. Desig.	Part Number	Description
	10073-2605	FRONT PANEL,RF-590
	10073-2021	FILTER, POLARIZED DISPLAY
	10073-2020	FILTER, POLARIZED DISPLAY
	10073-2018	BRACKET, PIVOT RIGHT
	10073-2019	BRACKET, PIVOT LEFT
	Z03-0001-004	HDL ALUM BLK 10-32X4.00IN
	Z03-0004-002	FER ALUM BLK .221 I.D.
	10073-2506	KNOB
	MP-1481	KNOB PLASTIC .713 DIA
A1	10073-2700	PWB ASSY,SWITCH&LED
A2	10073-2200	PWB ASSY, FRONT PANEL
A3	10073-2300	METER PWB ASSY
A4	10073-2400	PWB ASSY,DISPLAY
A5	10073-2500	PWB ASSY,DISPLAY
A6	10073-2250	CONVERTER MDL ASSY
G1	10073-2075	OPTICAL ENCODER PANEL MT
J1	J62-0001-007	JACK FONE CLOSED CKT
LS1	10073-2081	SPEAKER
M1	10073-2311	METER
P1	J46-0016-014	CONN HOUSING 14 POS 24AWG
P2	J40-0005-003	CONN,FEMALE,3CIR
P3	MP-0648	HOUSING, CONN, 5 CIRCUIT
P4	J40-0002-003	HOUSING, CONN, 3 CIRCUIT
P5	J40-0002-002	HOUSING, CONN, 2 PIN
P6	MP-0647	HOUSING, CONN, 6 CIRCUIT
R1	10073-2071	POT
R2	10073-2073	RES,VAR,5K,10%,LIN.TAPER
R3	10073-2072	RES,VAR,5K,10%,MOD.LOG

**2. FRONT PANEL SWITCHBOARD A13A1**

**2.1 General Description**

Front Panel Switchboard A13A1 consists of all RF-590 front panel pushbutton switches excluding the four-position meter select switch. It also includes all the discrete LED displays on the receiver front panel. Signals generated by switch closures are routed for processing to Control Board Assembly A14 via Front Panel Driver Board A13A2. The discrete LED displays are also driven from Front Panel Driver Board A13A2.

**2.2 Interface Connections**

Table 2 lists Front Panel Switchboard A13A1 interface connections.

**Table 2. A13A1 Switchboard Interface Connections**

Connector	Description
J1 to/from A13A2	
J1-1	Gnd
-2	Scan LED
-3	Test LED
-4	Program LED
-5	COL 7
-6	Receive LED
7	BFO LED
-8	Fault LED
-9	PB3
-10	Remote LED
-11	TWA
-12	TWB
-13	COL 2
-14	COL 0
-15	Tune Enable LED
-16	PB2
-17	COL 3
-18	N/C
-19	COL 5
-20	PB1
-21	N/C
-22	N/C
-23	COL 1
-24	Frequency LED
-25	N/C
-26	COL 6

**Table 2. A13A1 Switchboard Interface Connections (Cont.)**

Connector	Description
J1-27	PB0
-28	COL 4
-29	Channel LED
30	+5V
J2 to/from Panel coder	
J2-1	Gnd
-2	TWB
-3	Key
-4	TWA
-5	+5V
J3 to/from A13A3	
J3-1	N/C
-2	N/C
-3	Speaker on/off
-4	Speaker on/off

## 2.3 Functional Description

### 2.3.1 Switch Matrix

The pushbutton switches on the RF-590 Receiver front panel are arranged in a matrix of eight columns by four rows. The eight column signals (COL 0 through COL 7) are inputs from Front Panel Driver Board A13A2 while the four row signals are outputs to the Driver board. The microprocessor on the Control board detects switch activity by enabling all the column outputs while reading back the row inputs (PB0-PB3) looking for a connection between any row and any column. If a closure is detected, it enables the column lines selectively while reading back the row lines again to determine the exact location of the switch closure. The microprocessor then performs the activity indicated by the closure, including display update.

### 2.3.2 LED Circuits

The discrete LEDs on the Switchboard are driven directly from the front panel driver board. (See the description for Driver Board A13A2). Table 3 provides a listing of LED display by reference designator and function:

**Table 3. A13A1 Switchboard LED Indicators**

Indicator	Function	Description
DS1	Frequency	Indicates frequency display field will be modified by any tuning knob or keypad activity.
DS2	Fault	Indicates BITE, Power Supply, PLL Synthesizer faults, or Antenna Overhead faults.
DS3	Test	Indicates Test mode of operation.
DS4	Scan	Indicates receiver is in Scan mode of operation.
DS5	Receive	Indicates the RF-590 is in the standard Receive mode of operation.
DS6	BFO	Indicates BFO display field will be modified by any tuning knob or keypad activity.
DS8	Program	Indicates Receiver is in Channel or Group programming mode.
DS10	Remote	Indicates Receiver is under Remote control.
DS11	Tune	Indicates the tuning knob is enabled. If off, tuning knob rotation has no effect on the receiver.
DS12	Channel	Indicates the channel display field will be modified by any keypad or tuning knob activity.

## 2.4 Maintenance

The advanced design of the A13A1 assembly eliminates the need for regular maintenance. However, when replacing components on this assembly, observe the following caution.

**CAUTION**

Cleaning fluids normally used to remove flux will damage switches used on this assembly. Cleaning of the A13A1 assembly is not recommended.

Table 4 is the Front Panel Switchboard A13A1 parts list. Figures 3 and 4 are the Front Panel Switchboard A13A1 component location diagram and schematic diagram.

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Table 4. Front Panel Switchboard A13A1 Parts List (PL 10073-2700)

Ref. Desig.	Part Number	Description
	10073-2700	PWB, FRONT PANEL
	10073-2050	BUTTON,SW,0,CUSTOM MOLD
	10073-2051	BUTTON,SW,1,CUSTOM MOLD
	10073-2052	BUTTON,SW,2,CUSTOM MOLD
	10073-2053	BUTTON,SW,3,CUSTOM MOLD
	10073-2054	BUTTON,SW,4,CUSTOM MOLD
	10073-2055	BUTTON,SW,5,CUSTOM MOLD
	10073-2056	BUTTON,SW,6,CUSTOM MOLD
	10073-2057	BUTTON,SW,7,CUSTOM MOLD
	10073-2058	BUTTON,SW,8,CUSTOM MOLD
	10073-2059	BUTTON,SW,9,CUSTOM MOLD
	10073-2060	BUTTON,SW,TUNE,CUSTOM MLD
	10073-2061	SW BTN ENTR
	10073-2062	BUTTON,TEST
	10073-2063	BUTTON,SW,RECALL,CSTM MLD
	10073-2064	BUTTON,SW,LOAD,CSTM MOLD
	10073-2065	SW BTN PROG
	10073-2066	BUTTON,SCAN
	10073-2067	BUTTON SPK ON/OFF
	10073-2068	BUTTON RCV
	10073-2069	BUTTON,SW,CUSTOM MOLD
	10073-2022	SHIELD SWITCH
DS1	N21-0002-000	LED GRN T-1 2.0MCD
DS2	N21-0001-000	LED RED T-1 2.5MCD
DS3	N21-0002-000	LED GRN T-1 2.0MCD
DS4	N21-0002-000	LED GRN T-1 2.0MCD
DS5	N21-0002-000	LED GRN T-1 2.0MCD
DS6	N21-0002-000	LED GRN T-1 2.0MCD
DS8	N21-0002-000	LED GRN T-1 2.0MCD
DS10	N21-0002-000	LED GRN T-1 2.0MCD
DS11	N21-0002-000	LED GRN T-1 2.0MCD
DS12	N21-0002-000	LED GRN T-1 2.0MCD
DS14	N21-0002-000	LED GRN T-1 2.0MCD
J2	J46-0033-006	HDR 6 PIN 0.100" RT ANG
J3	J46-0033-005	HDR 5 PIN 0.100" RT ANG
S1 - S6	S05-0004-001	SWITCH
S9 - S16	S05-0004-001	SWITCH
S17, S18	S05-0004-002	SWITCH
S19	S05-0004-001	SWITCH
S20 - S29	S05-0004-002	SWITCH
S30	S05-0004-001	SWITCH
S31	S05-0004-001	SWITCH
S32	S05-0004-001	SWITCH
S33	S05-0005-001	SWITCH



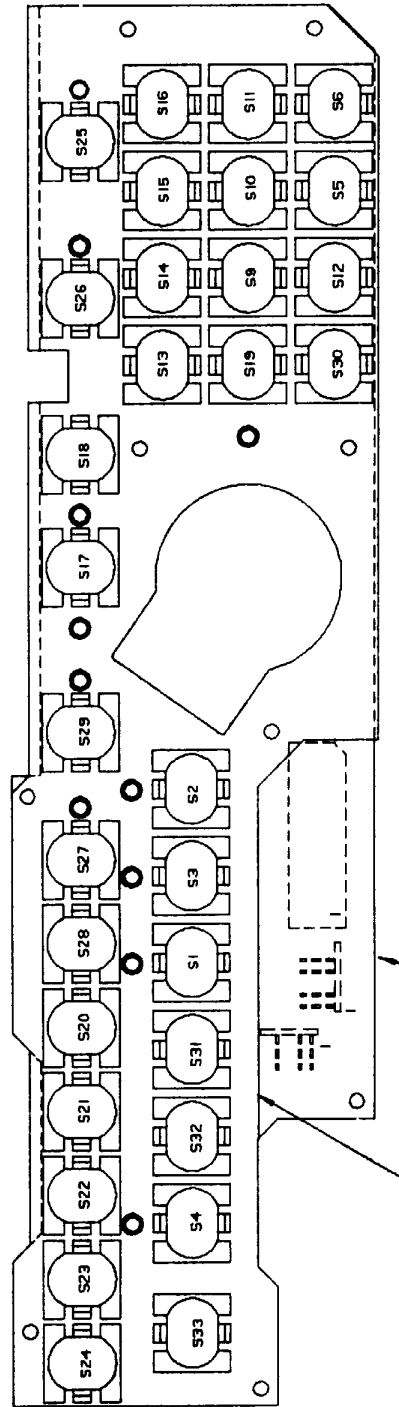
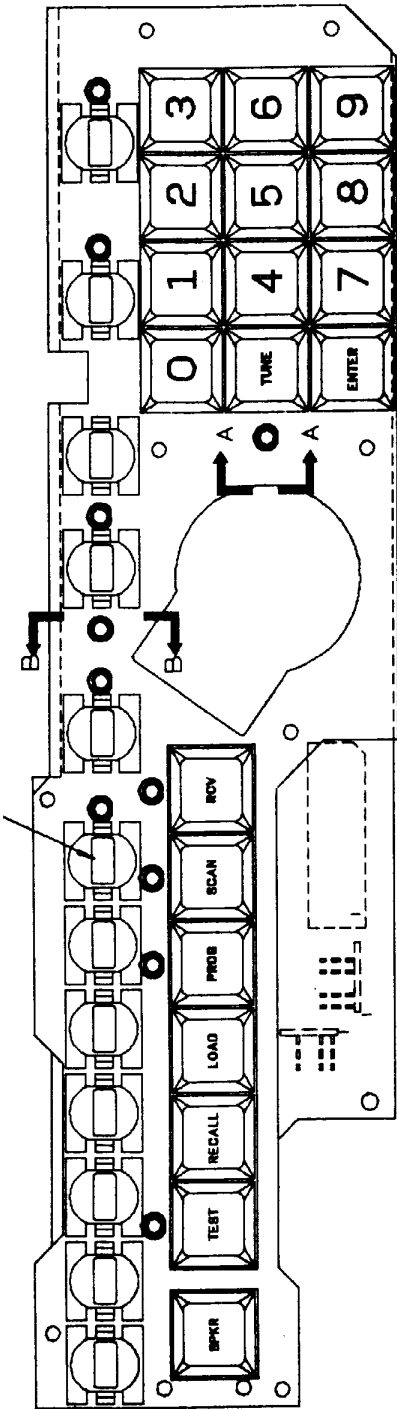
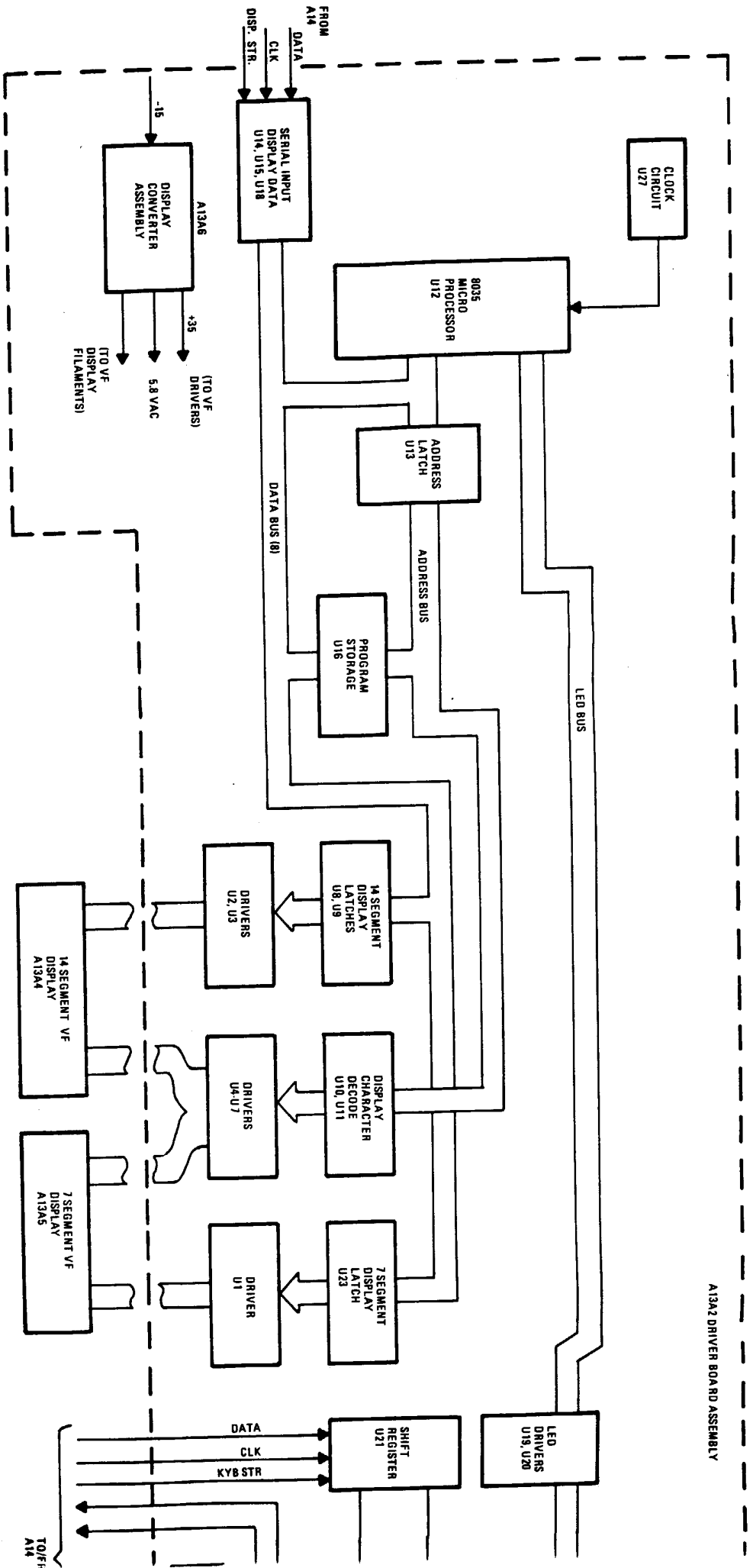


Figure 3. Front Panel Switchboard A13A1 Component Location Diagram (10073-2700, Rev. C)

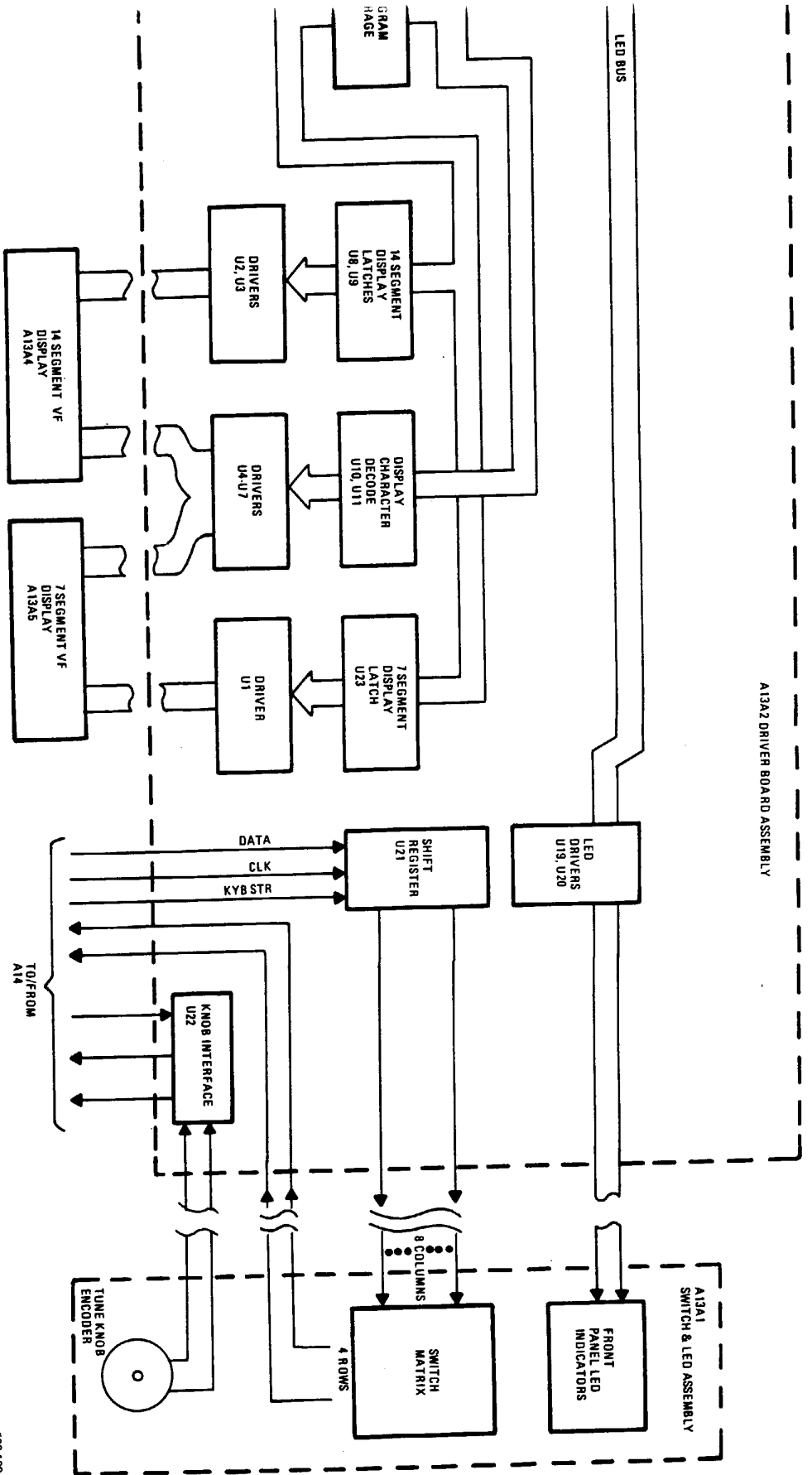




A13A2 DRIVER BOARD ASSEMBLY

Front Panel Driver Board A13A2  
Functional Block Diagram

A13A2 DRIVER BOARD ASSEMBLY



### 3. FRONT PANEL DRIVER BOARD A13A2

#### 3.1 General Description

The RF-590 Front Panel Driver Board serves four basic functions, all associated with controlling the front panel of the receiver. It generates the drive signals for the vacuum fluorescent displays, drives the discrete LED displays, generates signals indicating Tune Knob rotation and routes the signals to the Front Panel Switchboard associated with detecting pushbutton activity.

The Driver Board controls the vacuum fluorescent displays by providing filament voltages, display segment information, and digit select information to them. The filament voltages are generated in Display Converter Assembly A13A6 and routed to the display connectors. The Driver Board multiplexes the VF Displays by providing information for the segments to be lit within a character while enabling that character. This is done at a rapid rate to give the appearance of continuous illumination. (See sections 5 and 6 for drawings showing the display segment location.) The information to be displayed is provided to the Driver Board (A13A2) by the Control Board (A14) in serial fashion using the signals DATA, CLK, and DISP STR ON J1P1 pins 2, 4, and 14 respectively.

The discrete LED displays of the Front Panel are lit by the Driver Board using information provided by the Control Board.

Rotating the tune knob generates two pulsing signals which are squared up by the Driver Board, A13A2, and routed to the Control Board for service.

Driver Board A13A2 outputs eight column strobes to the switches in the front panel and inputs four row lines from the switches. The row lines are routed to the Control board where a switch closure is detected as a connection from a column to a row.

#### 3.2 Interface Connections

Table 5 summarizes the A13A2 interface connections.

**Table 5. A13A2 Driver Board Interface Connections**

Connector	Name	Description
J1 to/from A14		
J1-1	TWHL INT	Tune Knob Interrupt to Control Board
-2	Data	Serial Display Data from Control Board
-3	DIR	Tune Knob Direction to Control Board
-4	CLK	Clock for display Data from Control Board
-5	TWHL RESET	Interrupt Reset from Control Board
-6	-15V	
-7	+5V	
-8	BITE IN	Power Supply Fault Indicator

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**Table 5. A13A2 Driver Board Interface Connections (Cont.)**

Connector	Name	Description
J1-9	PB3	Switch row readback to Control Board
-10	KYBSTR	Keyboard Strobe from Control Board
-11	PB2	Switch Row readback to Control Board
-12	Fault	Output to Rear Panel (via Control Board)
-13	PB1	Switch Row readback to Control Board
-14	DISP STR	Display Strobe from Control Board
-15	PB0	Switch Row readback to Control Board
-16	N/C	
-17	N/C	
-18	GND	
-19	N/C	
-20	GND	
J2 to/from A13A1		
J2-1	GND	
-2	Scan LED	
-3	Test LED	
-4	Program LED	
-5	COL 7	
-6	Receive LED	
-7	BFO LED	
-8	Fault LED	
-9	PB3	
-10	Remote LED	
-11	TWA	Tuning knob encoder output
-12	TWB	Tuning knob encoder output
-13	COL 2	
-14	COL 0	
-15	Tune LED	
-16	PB2	
-17	COL 3	
-18	N/C	
-19	COL 5	
-20	PB1	
-21	N/C	
-22	N/C	
-23	COL 1	
-24	Frequency LED	
-25	N/C	
-26	COL 6	
-27	PB0	
-28	COL 4	

**Table 5. A13A2 Driver Board Interface Connections (Cont.)**

Connector	Name	Description
J2-29	Channel LED	
-30	+5V	
J3 to/from A13A4		
J3-1	a Segment	
-2	b Segment	
-3	c Segment	
-4	d Segment	
-5	m Segment	
-6	n Segment	
-7	e Segment	
-8	f Segment	
-9	J Segment	
-10	k Segment	
-11	g Segment	
-12	h Segment	
-13	Decimal Point	
-14	Comma	
-15	N/C	
-16	G1 Digit	
-17	p Segment	
-18	r Segment	
-19	G2 Digit	
-20	G3 Digit	
-21	G20 Digit	
-22	G4 Digit	
-23	G5 Digit	
-24	G6 Digit	
-25	G19 Digit	
-26	G7 Digit	
-27	G8 Digit	
-28	G9 Digit	
-29	G18 Digit	
-30	G10 Digit	
-31	G11 Digit	
-32	G12 Digit	
-33	G17 Digit	
-34	G13 Digit	
35	G14 Digit	
-36	N/C	
-37	G16 Digit	

**Table 5. A13A2 Driver Board Interface Connections (Cont.)**

Connector	Name	Description
J3-38	G15 Digit	
-39	Filament	
-40	Filament	
J4 to/from A13A5		
J4-1	G11 10 MHz Digit	
-2	G10 1 MHz Digit	
-3	G9 100 kHz Digit	
-4	G3 1/2 Segments	
-5	G7 1 kHz Digit	
-6	G8 10 kHz Digit	
-7	Filament	
-8	Decimal Point	
-9	G5 10 Hz Digit	
-10	G6 100 Hz Digit	
-11	N/C	
-12	Comma	
-13	G4 1 Hz Digit	
-14	c Segment	
-15	G2 CH10 Digit	
-16	G1 CH1 Digit	
-17	b Segment	
-18	a Segment	
-19	g Segment	
-20	Filament	
-21	Underline Segments	
-22	d Segment	
-23	e Segment	
-24	f Segment	

### 3.3 Circuit Description

#### 3.3.1 Microprocessor Operation

The heart of Front Panel Driver Board A13A2 operation is the 8035 microprocessor (U12). The execution of the software program stored in the 2716 type EPROM (U16) causes the microprocessor to perform the display update functions as described in paragraph 2. To execute the program, the microprocessor must continuously get instructions from U16 and process them. To accomplish this, the microprocessor (at the start of an instruction cycle) outputs the address of the instruction to be obtained into its address/data bus at pins U12-12 to U12-19. The address latch (U13) latches it to the EPROM. The EPROM (U16) outputs



the instruction to the data bus which is read by the microprocessor and executed. The microprocessor uses the Address Latch Enable, active high (ALE) signal to indicate the presence of a valid address on the bus. The Program Store Enable ( $\overline{\text{PSEN}}$ ) signal is used to enable the EPROM to output the obtained instruction while the  $\overline{\text{RD}}$  (read) and  $\overline{\text{WR}}$  (write) signals are used to read from and write to other external devices. The  $\overline{\text{RD}}$  signal is used to read display data sent by Control Board A14 from the shift registers U14 and U15 while the  $\overline{\text{WR}}$  signal is used to write the display information to the VF display segment latches U8, U9, and U23. These functions are explained in greater detail below.

### 3.3.2 Display Data Input

Front Panel Driver Board A13A2 at power up lights all LEDs and all segments of the vacuum fluorescent displays. After completion of the power on self-test, the display is updated to the last receive setting used before power off using display data provided by Control Board A14. The Control board provides the information for all display updates to the Driver board in serial fashion via J1-2. This information is clocked into serial shift registers U14 and U15 to be read in parallel by microprocessor U12. The clock signal is 750 kHz and is provided by the Control board at J1-4 and routed to the shift registers at pin 3. When the shift registers have been loaded with display data, the Control board generates an interrupt to the Driver board microprocessor (U12) using the signal display strobe at J1-14. The display strobe pulse serves to trigger monostable U24, which in turn generates the interrupt, causing the microprocessor to read the display data from the shift registers U14 and U15. U18 provides buffering of the display data onto the microprocessor data bus. The act of reading the shift registers causes resetting of the interrupt by the microprocessor read control line at U24-3 which is the reset in to the monostable.

### 3.3.3 Vacuum Fluorescent Display Drive

Display data read in from the Control board is converted by microprocessor U12 into formats required for driving the VF displays. The displays are driven in multiplexed fashion so that only one character is driven at a given instant. Each character in the VF displays has a unique address which is output by the microprocessor to the bus and latched into the address latch (U13) during a display character update. The address is decoded by U10 or U11 into a character enable pulse. During the output instruction, the segment information for the character to be lit is latched into U23 for seven segment characters or into U8 and U9 for 14 segment characters. Each character is enabled for approximately 640 microseconds after which, the microprocessor processes the next character in a similar manner.

### 3.3.4 LED Drive

The discrete LEDs on the front panel are driven from the parallel ports on microprocessor U12. These outputs are buffered by U19 and U20 and are routed to the switchboard via J2. An LED is lit by an active low output. The information to be written to the LEDs originates in Control Board A14 and is input to the Driver board in the manner described in paragraph 3.3.2.

### 3.3.5 Tuning Knob

Rotating the front panel tuning knob causes two pulsing signals to be generated which are 90 degrees out of phase. These are input to the Driver board at J2-11 and J2-12. The pulses are squared by Schmitt Trigger Inverters (U28) and used to generate an interrupt to the Control board via U22. The interrupt (active high) is output at J1-1 while J1-3 provides direction of rotation information to Control Board A14. When the Control board receives Tuning knob interrupts indicating rotation, it outputs new display information to the Driver board as described in paragraph 3.3.2, so that the indicated display field is increased or decreased.

### 3.3.6 Pushbutton Circuitry

The Driver board serves primarily to route the signals associated with detection of pushbutton activity to and from the Control and Switchboards. The switches are arranged in a matrix of eight columns by four rows. Switch activity is detected by sensing a closure between a column line to a row line. The column outputs are written serially from the Control board to the Driver board via P3-2, clocked via J1-4, and latched into shift register U21 by the signal KYB STR (keyboard strobe) at J1-10. The parallel outputs of the shift register are routed to the Switchboard via J2 signals COL 0 through COL 7. The rows are routed back to the Control board as signals PB 0 to PB 3 (see J1-9, 11, 13, and 15).

## 3.4 Maintenance

### 3.4.1 Adjustments

The only adjustment on the Front Panel Driver Board is the VF display brightness adjust potentiometer located at the top center of the PWB. Turn clockwise for brighter displays (single turn potentiometer).

### 3.4.2 Troubleshooting

To make a quick assessment of Driver Board functions, the four test points should be checked with an oscilloscope.

- TP1 – Microprocessor Write Line. Should be active low pulses repeated approximately every 600 to 700 microseconds.
- TP2 – Character Strobe to U10. Active high pulse every 600 to 700 microseconds indicates display is being updated.
- TP3 – Character Strobe to U11. Same as TP2. Also indicates display being updated. Both signals are required.
- TP5 – Interrupt to microprocessor from Control board. Active low approximately 50u seconds pulse every 1 second, (faster with Tuning Knob Rotating).

If the above signals are incorrect, more fundamental checks are indicated. Perform the checks in the following order.

- a. Verify +5V at J1-7 and -15V at J1-6.
- b. Verify display converter voltages at E7-E12 of Driver PWB and integrity of connections to converter module according to table 6.

**Table 6. Converter Voltages**

Driver	Converter	Function
E7	C1	-15 Vdc
E8	C5	5.8 Vac
E9	C3	+35 Vdc
E10	C4	Bias $\approx$ 6 Vdc
E11	C2	5.8 Vac
E12	E1	GND

- c. Verify integrity of connections E1 through E6. The 10073-2400 alphanumeric display module requires connections E1 to E2 and E5 to E4.
- d. Verify 6 MHz clock at U12-2 and U12-3.
- e. Verify approximately +5V at U12-4. (Microprocessor reset in).
- f. Verify ALE signal, approximately 60-40 duty cycle square wave at U12-11.
- g. Verify activity on bus AD0 - AD7 (zero to five volt random square waves).
- h. Verify that all socketed ICs are installed correctly with no pins bent underneath the IC.

### 3.5 Parts List and Schematic Diagram

Table 7 is the Driver Board A13A2 parts list. Figures 5 and 6 are the Driver Board A13A2 component location diagram and schematic diagram.

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Table 7. Driver Board A13A2 Parts List (PL 10073-2200)

Ref. Desig.	Part Number	Description
	10073-2200	PWB, FRONT PANEL
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/01-1535	CAP .01UF 20% 100V CER
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	CK05BX102M	CAP 1000PF 20% 200V CER
C37	C26-0025-470	CAP 47UF 20% 25V TANT
C38	C26-0050-479	CAP 4.7UF 20% 50V TANT
C39	CK05BX330M	CAP 33PF 20% 200V CER
C40	CK05BX330M	CAP 33PF 20% 200V CER
CR1	1N4454	DIODE 200mA 75V SW
CR2	1N4454	DIODE 200mA 75V SW
CR3	1N4454	DIODE 200mA 75V SW
CR4	1N4454	DIODE 200mA 75V SW
J2	J46-0013-030	HDR 30 PIN 0.100" DR SHRD
P1	10073-7050	RIBBON CABLE, 24 COND
P2	10073-7051	RIBBON CABLE, 40 COND
P3	10073-7053	RIBBON CABLE, 20 COND
R3	R50-0010-472	RES,10SIP,4.7K,2.0%, 9RES
R14	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R15 - R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R22	R51-0010-121	RES 10P SIP 120 2% 5RES
R23	R51-0010-121	RES 10P SIP 120 2% 5RES
R25	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R26	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R27	R65-0003-204	RES 200K 5% 1/4W CAR FILM
R28	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R29	R-2232	RES,VAR,PCB 100K .5 20%

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Table 7. Driver Board A13A2 Parts List (PL 10073-2200) (Cont.)

Ref. Desig.	Part Number	Description
R33	R65-0003-471	RES 470 5% 1/4W CAR FILM
R34	R65-0003-471	RES 470 5% 1/4W CAR FILM
R35	R65-0003-471	RES 470 5% 1/4W CAR FILM
R36	R65-0003-471	RES 470 5% 1/4W CAR FILM
R37	R65-0003-161	RES 160 5% 1/4W CAR FILM
R38	R50-0008-103	RES,8 SIP, 10K,2.0%, 7RES
R50	R65-0003-100	RES 10 5% 1/4W CAR FILM
R52	R65-0003-100	RES 10 5% 1/4W CAR FILM
R53	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS
TP2	J-0387	TP PWB RED RA SIDE ACCESS
TP3	J-0390	TP PWB ORN RA SIDE ACCESS
TP5	J-0389	TP PWB GRN RA SIDE ACCESS
U1	I75-0009-001	IC NE594 DISPLAY DRIVER
U2	I75-0009-001	IC NE594 DISPLAY DRIVER
U3	I75-0009-001	IC NE594 DISPLAY DRIVER
U4	I75-0009-001	IC NE594 DISPLAY DRIVER
U5	I75-0009-001	IC NE594 DISPLAY DRIVER
U6	I75-0009-001	IC NE594 DISPLAY DRIVER
U7	I75-0009-001	IC NE594 DISPLAY DRIVER
U8	I07-0013-001	IC 74C373 PLASTIC CMOS
U9	I07-0013-001	IC 74C373 PLASTIC CMOS
U10	I01-0000-202	IC 4514B PLASTIC CMOS
U11	I01-0000-202	IC 4514B PLASTIC CMOS
U12	IC-0347	IC 8035 MICRO 8-BIT
U13	I07-0013-001	IC 74C373 PLASTIC CMOS
U14	I01-0000-156	IC 4094B PLASTIC CMOS
U15	I01-0000-156	IC 4094B PLASTIC CMOS
U16	10073-8302	SOFTWARE KIT
U17	I05-0001-000	IC 4098B PLASTIC CMOS
U18	I05-0000-244	IC 74LS244 PLASTIC TTL
U19	I05-0000-244	IC 74LS244 PLASTIC TTL
U20	I05-0000-244	IC 74LS244 PLASTIC TTL
U21	I01-0000-156	IC 4094B PLASTIC CMOS
U22	I05-0000-074	IC 74LS74 PLASTIC TTL
U23	I07-0013-001	IC 74C373 PLASTIC CMOS
U24	I05-0001-000	IC 4098B PLASTIC CMOS
U25	I01-0056-001	IC 74C02 PLASTIC CMOS
U26	I05-0000-027	IC 74LS27 PLASTIC TTL
U27	I02-0015-000	IC 7404 PLASTIC TTL
U28	I18-0006-001	IC 74C14 PLASTIC CMOS
VR1	1N5234B	DIODE 6.2V 5% .5W ZENER
XU12	J77-0008-007	SKT IC MACH 40 PIN
XU16	J77-0008-005	SKT IC MACH 24 PIN
Y1	Y15-0004-060	CRYSTAL, 6MHZ

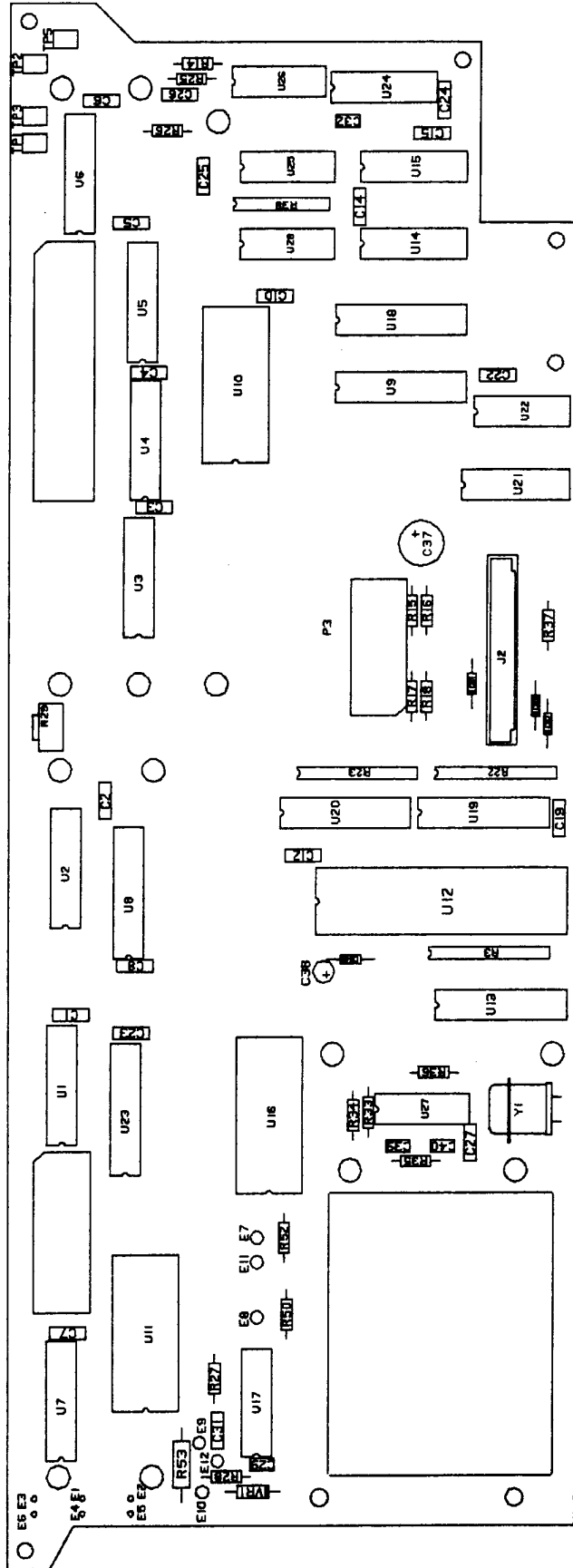
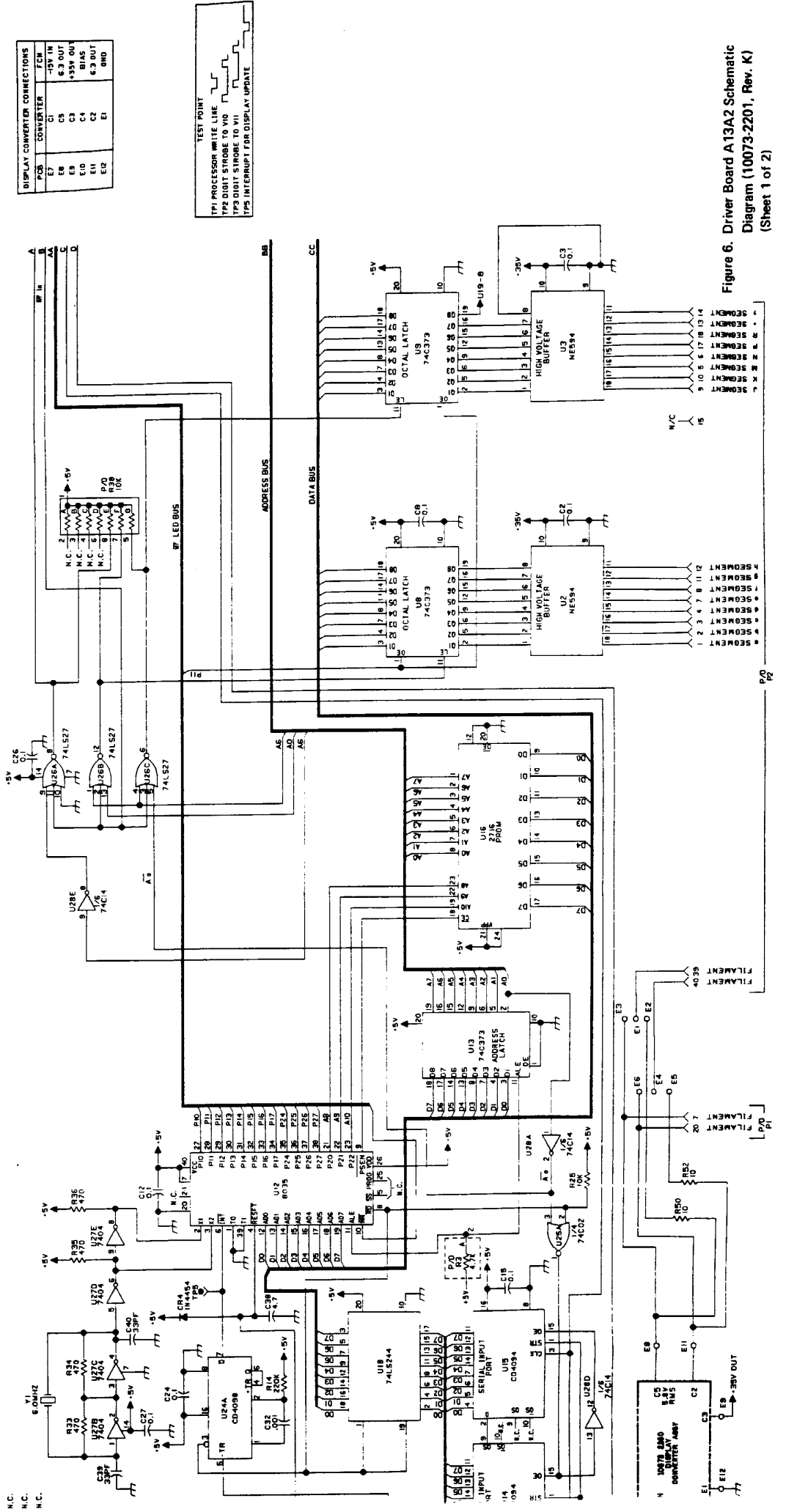


Figure 5. Driver Board A13A2 Component Location Diagram (10073-2200, Rev. G)



DISPLAY CONVERTER CONNECTIONS		FCW
PC5	C1	-15V IN
E7	C5	6.3 OUT
E8	C3	+35V OUT
E10	C4	BIAS
E11	C2	6.3 OUT
E12	E1	0ND

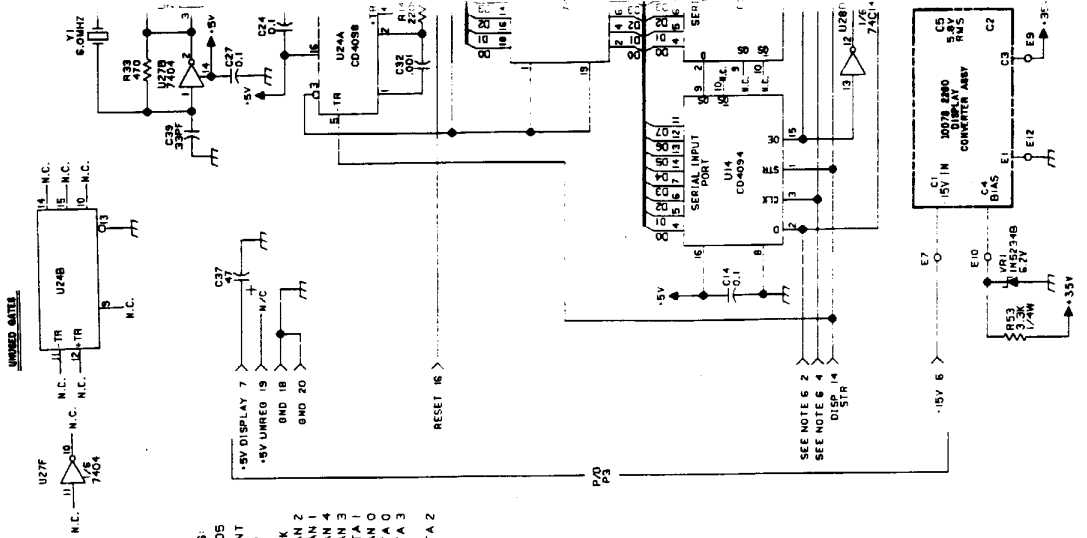
TEST POINT  
TPI PROCESSOR WRITE LINE  
TPE DIGIT STROBE TO V10  
TFS DIGIT STROBE TO V11  
TFS INTERRUPT FOR DISPLAY UPDATE

Figure 6. Driver Board A13A2 Schematic  
Diagram (10073-2201, Rev. K)  
(Sheet 1 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREcede WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
- ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%. ALL CAPACITOR VALUES ARE IN MICROFARADS.
- VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
- CONNECT E4 TO E5 AND E1 TO E2 FOR FABRIK MANU- NUMERIC DISPLAY (P/N 10075-2400).
- SIGNALS ARE PRODUCT SPECIFIC FOR THE FOLLOWING PINS:

PIN	RF-550	RF-1310	RF-7110	RF-7405
P3-1	TUNE WHL INT	N/C	N/C	TWHLINT
P3-2	DATA	N/C	N/C	DATA
P3-3	FR SER DATA	N/C	N/C	DIR
P3-4	CLK	FR SER CLK	DATA CLOCK	CLOCK
J2-2	SCAN	OPER	SOUELCH	LED SCAN 2
J2-3	TEST	AMP OFF	START LOA	LED SCAN 1
J2-4	PROG	STBY	SCAN	LED SCAN 4
J2-5	REC	POWER	CALL	LED SCAN 3
J2-6	REC	READY	SILENT	LED SCAN 0
J2-7	REC	CLIP	CALL AUTO	LED SCAN 1
J2-10	REMODE	N/C	N/C	LED DATA 3
J2-15	TUNE	N/C	N/C	LED DATA 2
J2-24	NOISEBLANK	N/C	N/C	LED DATA 1
J2-25	N/C	N/C	N/C	N/C
J2-28	N/C	N/C	N/C	N/C





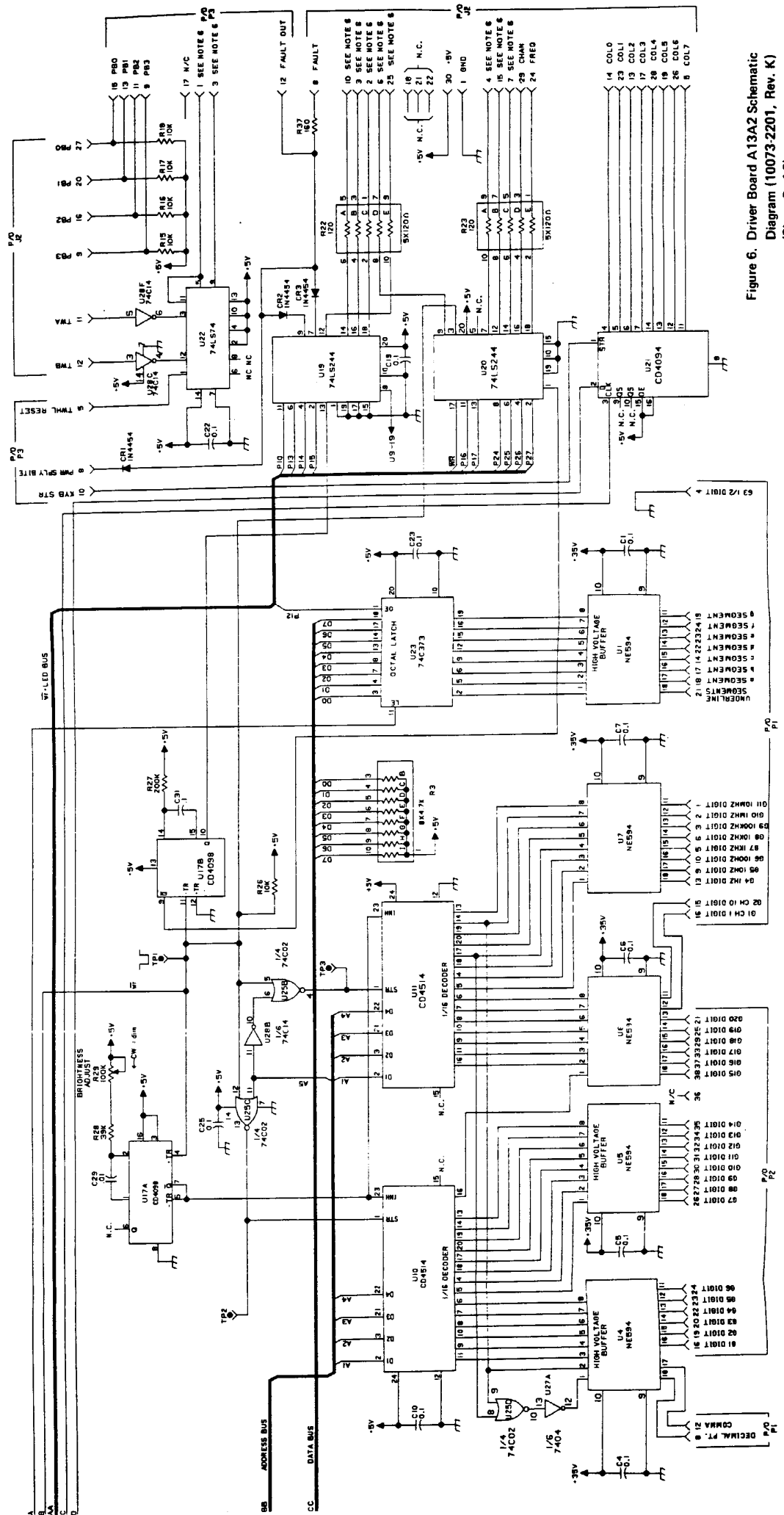
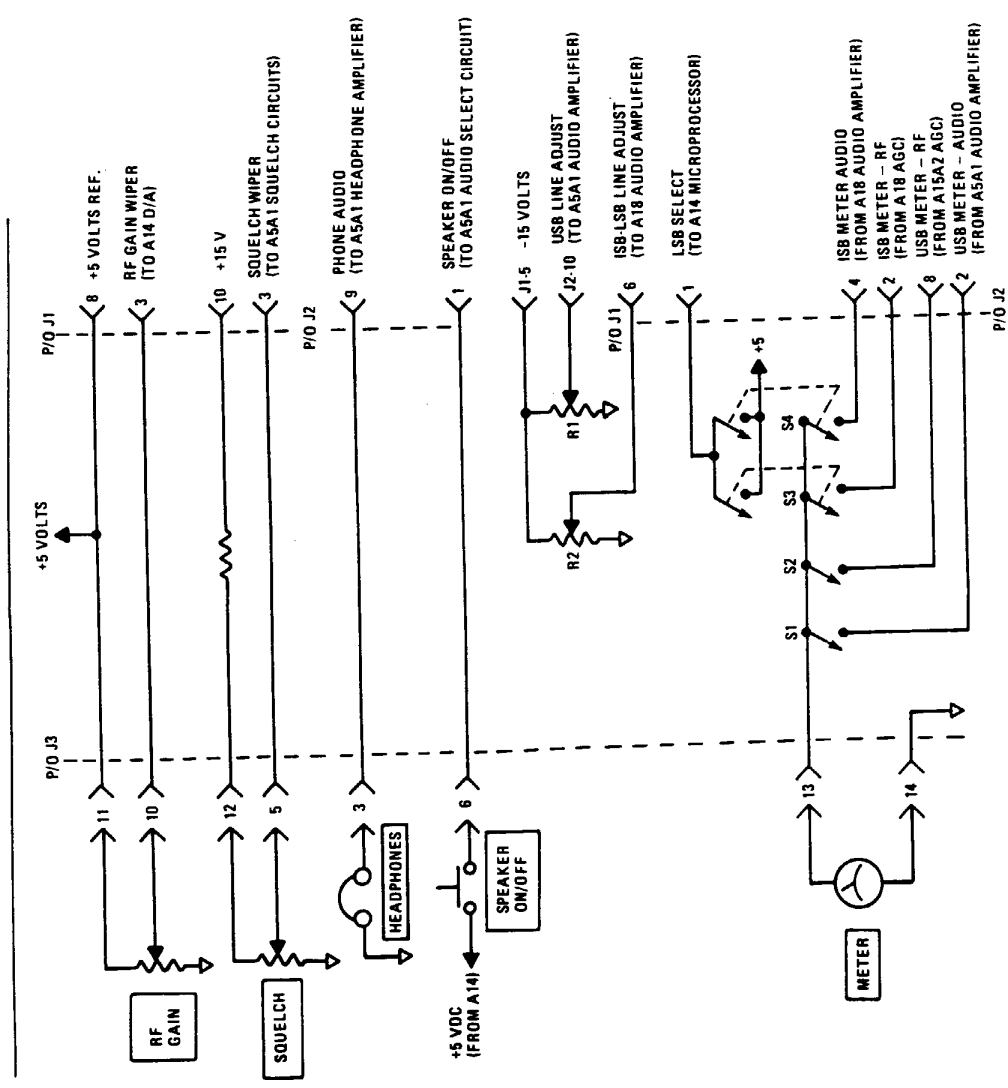


Figure 6. Driver Board A13A2 Schematic  
Diagram (10073-2201, Rev. K)  
(Sheet 2 of 2)



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Front Panel Meter Board A13A3  
Functional Block Diagram

#### 4. FRONT PANEL METER BOARD A13A3

##### 4.1 General Description

Meter Board A13A3 contains the circuitry required to monitor selected RF and AF signals on the RF-590 front panel meter (M1). The following signals may be monitored via pushbutton front panel control.

- RF Signal strength - All modes
- AF Line Audio level - All modes
- ISB - LSB RF Signal strength
- ISB - LSB Line Audio Level

The four switches controlling these functions are spring loaded so that only one of them may be active at any time.

Additionally, other signal data relating to the following functions flow through this board to the following RF-590 front panel controls.

- Headphone Audio
- RF Gain
- Squelch
- Speaker ON/OFF

##### 4.2 Interface Connections

Table 8 summarizes the A13A3 interface connections.

**Table 8. A13A3 Interface Connections**

Connector	Function
J1 to/from A14	
J1-1	LSB Select
-2	LSB Meter - AGC
-3	RF Gain
-4	LSB Meter - Audio
-5	-15V
-6	LSB Line Adjust
-7	Spare

**Table 8. A13A3 Interface Connections (Cont.)**

Connector	Function
J1-8	+5 Vdc
-9	Ground
-10	+15 Vdc
J2 to/from A5	
J2-1	Speaker ON/OFF
-2	USB Meter - Audio
-3	Squelch Wiper
-4	Key
-5	Spare
-6	Speaker Audio
-7	Audio Ground
-8	USB Meter - AGC
-9	Phone Audio
-10	USB Line Adjust
J3 to/from Front Panel	
J3-1	Spare
-2	Key
-3	Phone Audio
-4	Audio Ground
-5	Squelch Wiper
-6	Speaker ON/OFF
-7	Spare
-8	Speaker Audio
-9	Ground
-10	RF Gain
-11	+5 Vdc
-12	+15 Vdc
-13	Meter +
-14	Meter -

### 4.3 Circuit Description

#### 4.3.1 Meter Control

RF signal strength and line audio level signals are normally supplied by AGC assembly A15A2 and IF/ Audio Assembly A15A1 respectively. S2 connects the RF signal to the meter when pressed, and S1 connects the line audio signal. If optional ISB Assembly A18 has not been installed, there will be no ISB RF signal strength or ISB Line audio signals present to be selected. Consequently, pressing either S3 or S4 will result in a zero meter reading.

If the ISB option is installed; however, the RF (S1) and AF (S2) switches channel the USB components of the ISB signal to M1. The ISB LSB RF (S3) and ISB LSB AF (S4) switches route the LSB components of the ISB signal to the meter. Whenever an ISB switch (S3 or S4) is selected, +5 Vdc is switched on to the LSB select line (J1-1) which informs Control Board Assembly A14 that an ISB function has been selected.

#### 4.3.2 Line Level Control

Line audio output level adjustments are provided on the A13A3 assembly. They are accessed through small front panel holes to the left of the meter (USB line audio) and to the right of the meter (ISB-LSB line audio). R1 adjusts USB adjustments under normal receiver operation, while R2 will control the LSB audio portion of the ISB signal if the A18 ISB option is installed. Either control will vary the 600 ohm line audio outputs level (available at RF-590 rear panel connector TB1 and J7) from approximately -16 dBm to +10 dBm.

The adjustment of R1 controls line audio level by varying the bias and consequently the on resistance of an FET in the A5A1 line audio amplifier circuit. The FET therefore acts as an electronic attenuator for the line level. (See subsection A5A1). R2 functions identically for the optional ISB Assembly A18.

#### 4.3.3 Front Panel Control Signals

- **RF GAIN**

5 Vdc is applied to the top of the front panel RF GAIN control, and a portion is fed back via the wiper to Control Assembly A14 A/D converter. This signal is used to manually control the receiver gain.

- **SQUELCH**

+15 Vdc is fed through R4, which results in 5 Vdc at the top of the front panel SQUELCH CONTROL. The wiper arm returns a portion of this to act as a squelch threshold signal for squelch circuits on the A5A1 assembly.

- **HEADPHONES**

Headphone Audio from the A5A1 assembly is passed through the A13A3 assembly to a front panel HEADPHONE CONNECTOR. Headphone volume is adjustable via the AF GAIN control.

- **SPEAKER ON/OFF**

The Front Panel SPEAKER ON/OFF switch applies 5 Vdc to the audio select circuit on the A5A1 assembly whenever the switch is pushed in. This signal then gates audio to the speaker.

**4.3.4 Parts Lists and Schematic Diagram**

Table 9 is the Front Panel Meter Board A13A3 parts list. Figures 7 and 8 are the Front Panel Meter Board A13A3 component location diagram and schematic diagram.

**Table 9. Front Panel Meter Board A13A3 Parts List (PL 10073-2300)**

Ref. Desig.	Part Number	Description
J1	10073-2300	PWB, METER
	10073-2313	SW DPDT 4SEC INTLOCKING
	J-0870	CONN , 10 PIN
J2	J46-0032-010	HDR 10 PIN 0.100" SR
J3	J46-0032-014	HDR 14 PIN 0.100" SR
R1	R30-0001-103	RES,VAR,10K 3/4W 20%
R2	R30-0001-103	RES,VAR,10K 3/4W 20%
R3	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R4	R65-0003-103	RES 10K 5% 1/4W CAR FILM

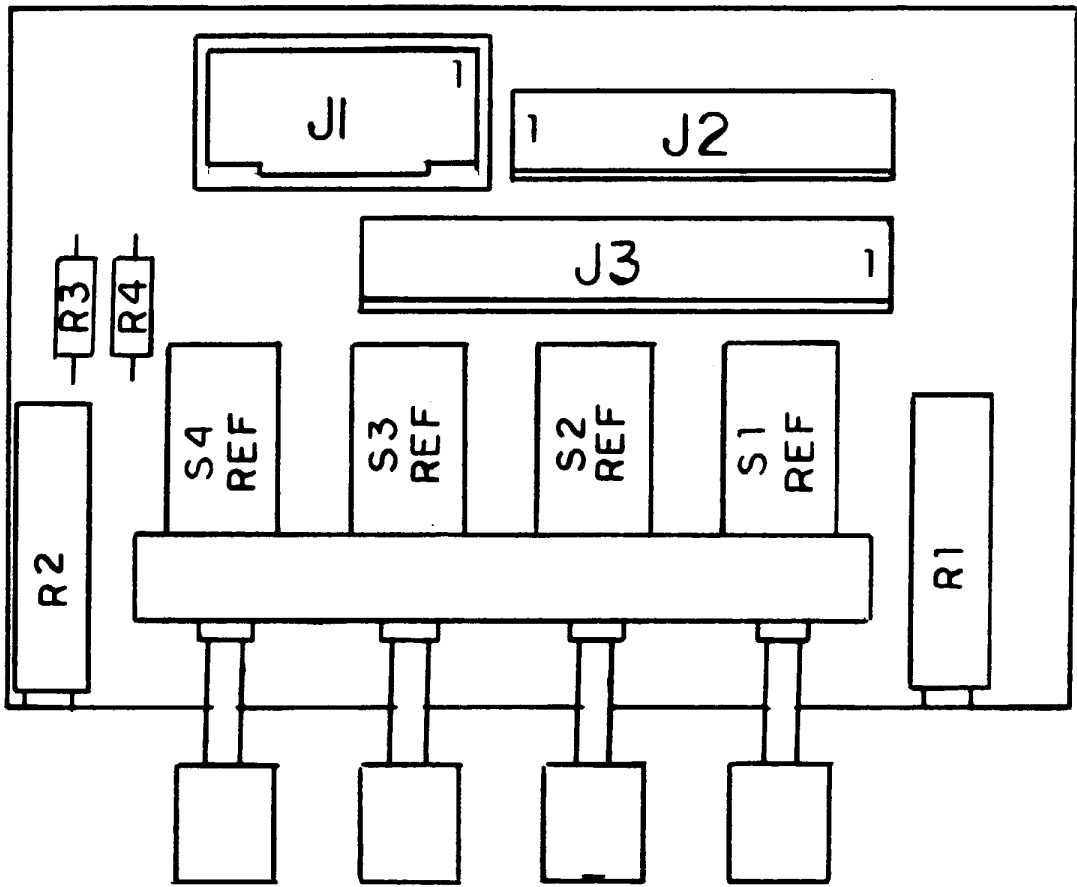


Figure 7. Front Panel Meter Board A13A3 Component Location Diagram (10073-2300, Rev. D)







**5. ALPHANUMERIC DISPLAY ASSEMBLY A13A4**

**5.1 General Description**

Alphanumeric Display Assembly A13A4 consists of a single vacuum fluorescent display which contains twenty four segment (British flag) characters. The alpha display is used to provide indications of AGC, Mode, Bandwidth, and Dwell time in Scan Mode, Scan Group and BFO frequency. Additionally the alphanumeric display is used to prompt the operator for programming and scan related function selections. It is also used to provide fault indications, if any, at the completion of the BITE test.

**5.2 Interface Connections**

Table 10 lists the A13A4 interface connections.

**Table 10. A13A4 Interface Connections**

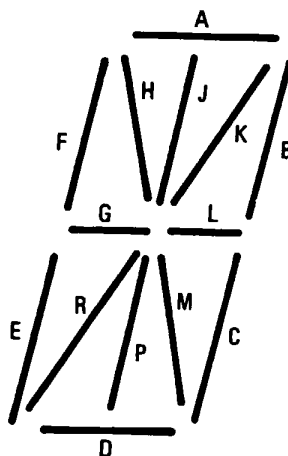
Connector	Description
J1 to/from A13A2	
J1-1	a Segment
-2	b Segment
-3	c Segment
-4	d Segment
-5	m Segment
-6	n Segment
-7	e Segment
-8	f Segment
-9	J Segment
-10	k Segment
-11	g Segment
-12	h Segment
-13	Decimal Point
-14	Comma
-15	N/C
-16	G1 Digit
-17	p Segment
-18	r Segment
-19	G2 Digit
-20	G3 Digit
-21	G20 Digit
-22	G4 Digit
-23	G5 Digit
-24	G6 Digit
-25	G19 Digit
-26	G7 Digit

**Table 10. A13A4 Interface Connections (Cont.)**

Connector	Description
J1-27	G8 Digit
-28	G9 Digit
-29	G18 Digit
-30	G10 Digit
-31	G11 Digit
-32	G12 Digit
-33	G17 Digit
-34	G13 Digit
-35	G14 Digit
-36	N/C
-37	G16 Digit
-38	G15 Digit
-39	Filament
-40	Filament

### 5.3 Functional Description

The alphanumeric vacuum fluorescent display is very similar in principle to the vacuum tube. Front Panel Driver Board A13A2 provides all required voltages and timing to properly drive the display. The 10073-2400 twenty character VF display requires a 4.7 Vac filament voltage and 35 Vdc grid and anode voltages. The grids (20 of them) are essentially character enable signals which are driven in multiplexed fashion, enabled one at a time as the segment data for that character is provided to the anode pins. The anode pins are inputs for the 14 segments plus dot and comma signals. Figure 9 shows the display's segment location. See paragraphs 3.1 and 3.3.3 for additional details.



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**Figure 9. Alphanumeric Display Segment Location**

**5.3.1 Parts List and Schematic Diagram**

Table 11 is the Alphanumeric Display A13A4 Assembly parts list. Figures 10 and 11 are the Alphanumeric Display A13A4 component location diagram and schematic diagram

**Table 11. Alphanumeric Display Assembly A13A4 Parts List (PL 10073-2400)**

Ref. Desig.	Part Number	Description
DS1 J1	10073-2400 N50-0006-001 J46-0031-040	PWB, DISPLAY DSPL FLR VAC 14SEG 20-DIG HDR 40 PIN 0.100" RT ANG

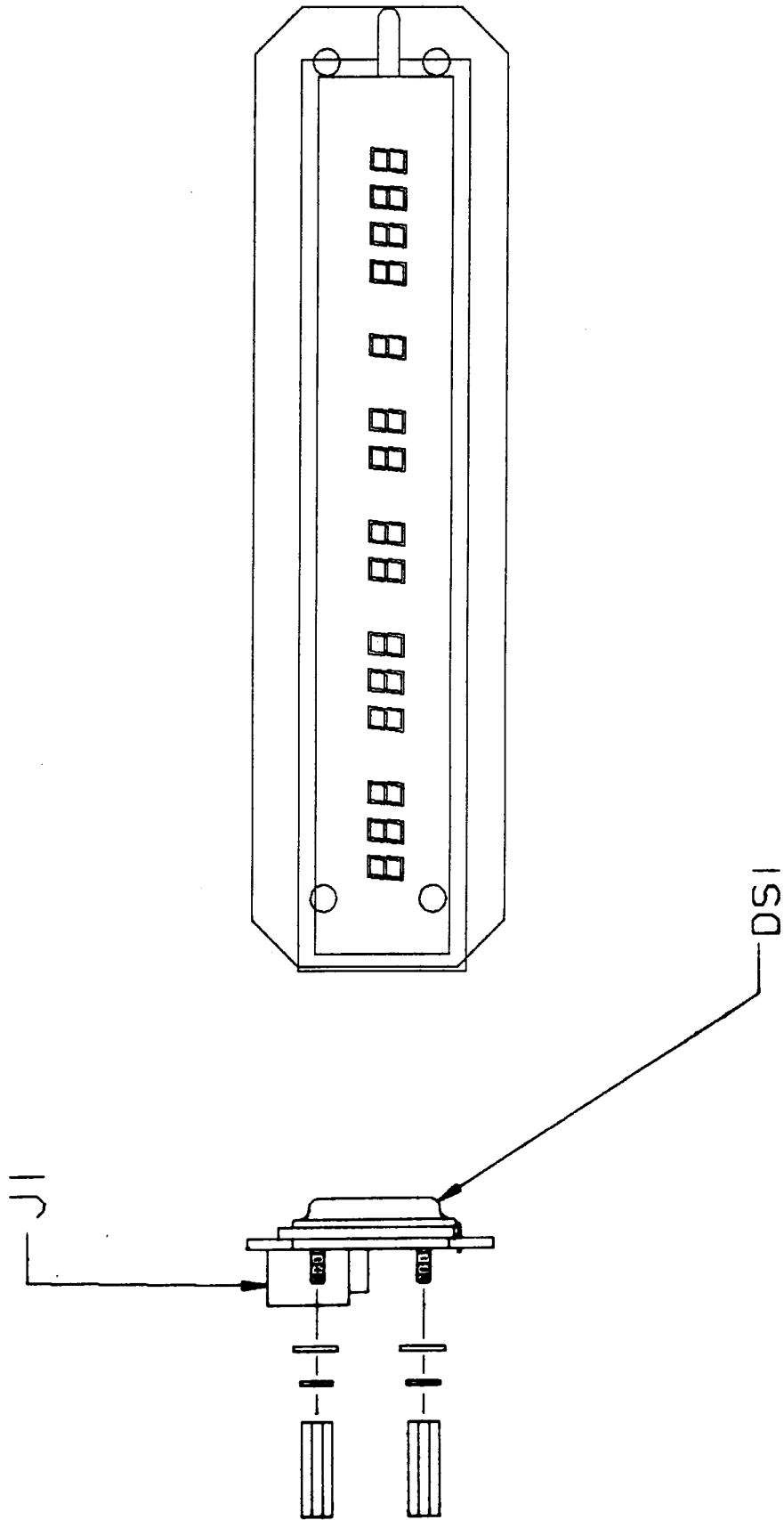


Figure 10. Alphanumeric Display Board A13A4 Component Location Diagram (10073-2400, Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

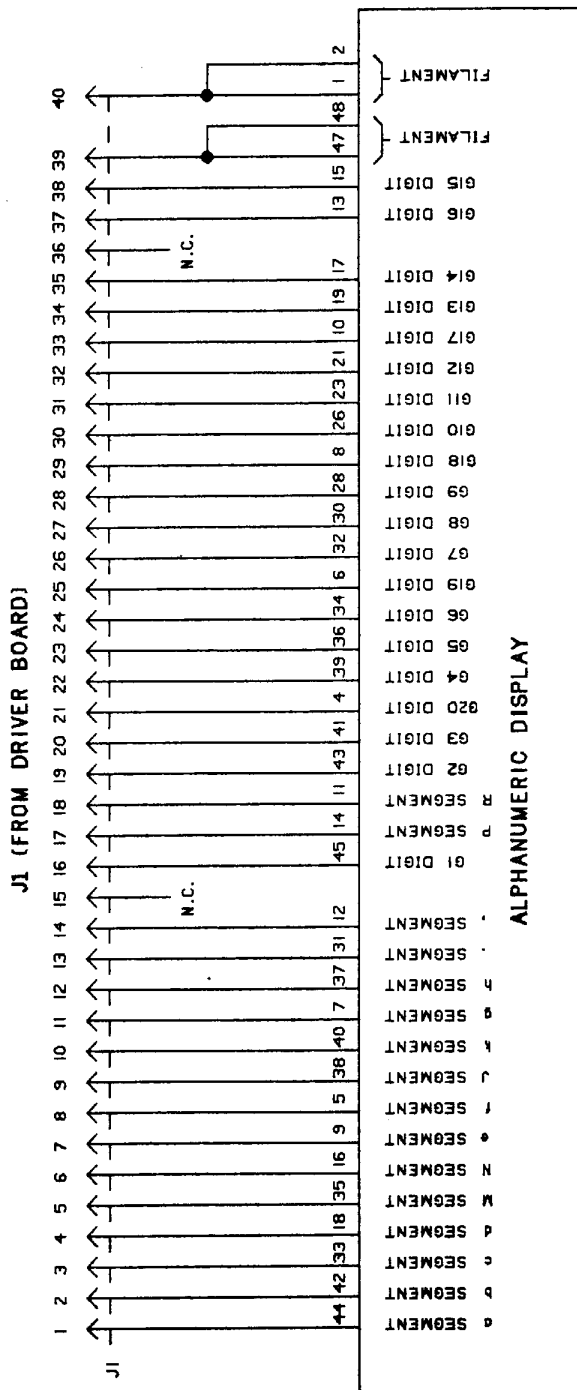


Figure 11. Alphanumeric Display Board A13A4 Schematic Diagram (10073-2401, Rev. B)

**6. NUMERIC DISPLAY ASSEMBLY A13A5**

**6.1 General Description**

Numeric Display Assembly A13A5 consists of a single vacuum fluorescent display which contains eight seven segment characters used for frequency display and two seven segment characters used for the channel display.

**6.2 Interface Connections**

Table 12 lists the A13A5 interface connections.

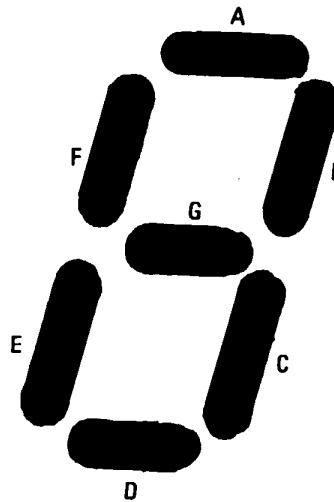
**Table 12. A13A5 Interface Connections**

Connector	Description
J1 to/from A13A2	
J1-1	G11 10 MHz Digit
-2	G10 1 MHz Digit
-3	G9 100 kHz Digit
-4	G3 1/2 Segments
-5	G7 1 kHz Digit
-6	G8 10 kHz Digit
-7	Filament
-8	Decimal Point
-9	G5 10 Hz Digit
-10	G6 100 Hz Digit
-11	N/C
-12	Comma
-13	G4 1 Hz Digit
-14	c Segment
-15	G2 CH10 Digit
-16	G1 CH1 Digit
-17	b Segment
-18	a Segment
-19	g Segment
-20	Filament
-21	Underline Segments
-22	d Segment
-23	e Segment
-24	f Segment



### 6.3 Functional Description

The numeric vacuum fluorescent display is very similar in principle to the vacuum tube. Front Panel Driver Board A13A2 provides all required voltages and timing signals to properly drive the display. The 10073-2500 VF display operates by using a 5.8 Vac filament voltage and 35 Vdc grid and anode voltages. The grids (ten of them) are character enable signals which are driven in a multiplexed fashion. The grids are enabled one at a time as the seven segment data plus underline, if required, are provided to the anode pins. Each digit is enabled for approximately 600 to 700u seconds. Figure 12 shows the displays segment's location.



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**Figure 12. Numeric Display Segment Location**

#### 6.3.1 Parts List and Schematic Diagram

Table 13 is the Numeric Display Assembly A13A5 parts list. Figures 13 and 14 are the Numeric Display Assembly A13A5 component location diagram and schematic diagram.

**Table 13. Numeric Display Assembly A13A5 Parts List (PL 10073-2500)**

Ref. Desig.	Part Number	Description
DS1 J1	10073-2500 N50-0005-001 J46-0031-024	PWB, DISPLAY DSPL FLR VAC 7SEG 11-DIG HDR 24 PIN 0.100" RT ANG

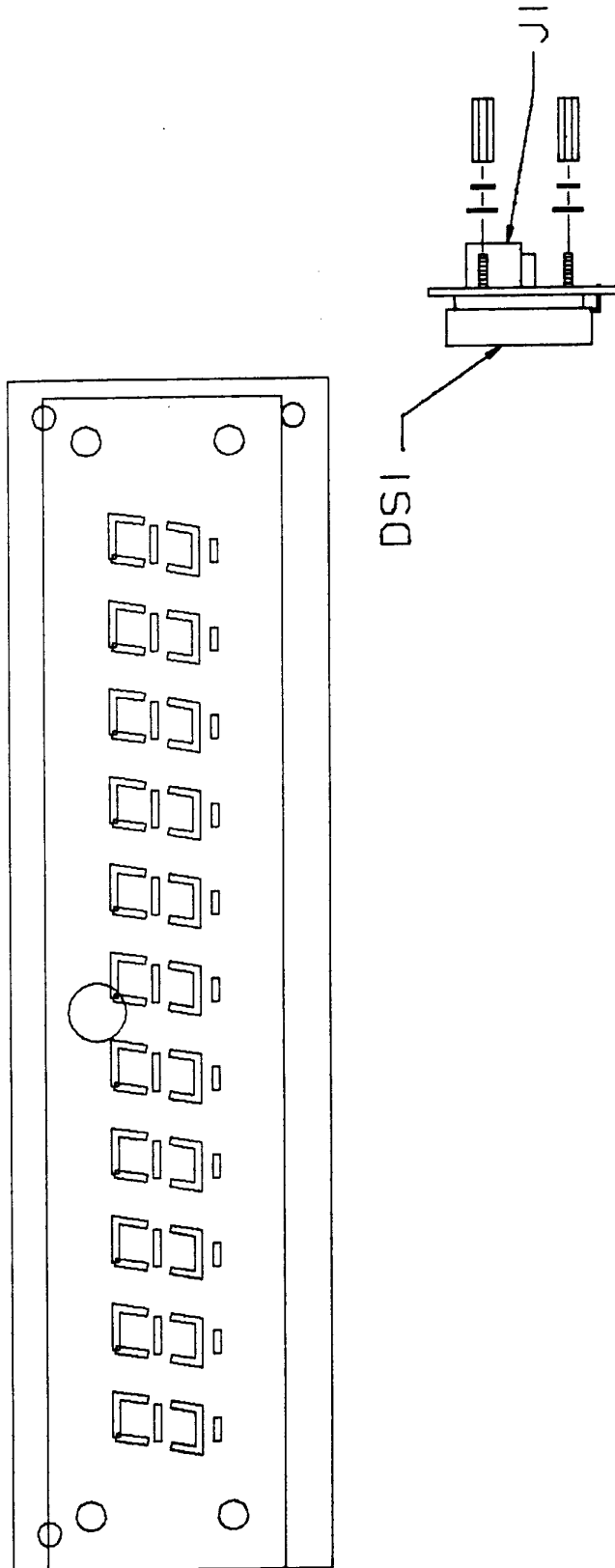


Figure 13. Numeric Display Board A13A5 Component Location Diagram (10073-2500, Rev. B)



**7. CONVERTER ASSEMBLY A13A6**

**7.1 General Description**

Converter Assembly A13A6 is a self contained dc to dc converter type power supply. It supplies anode and filament voltages to the A13A4 and A13A5 front panel vacuum fluorescent displays from the available -15 Vdc supply. Anode voltage output is 35 Vdc at 100 mA and filament output voltage is 5.8 Vac at 200 mA.

The A13A6 assembly itself is a sealed unit to provide EMI protection. Input/output connections to the internal A13A6A1 PWB is via feedthrough capacitors.

**7.2 Circuit Descriptions**

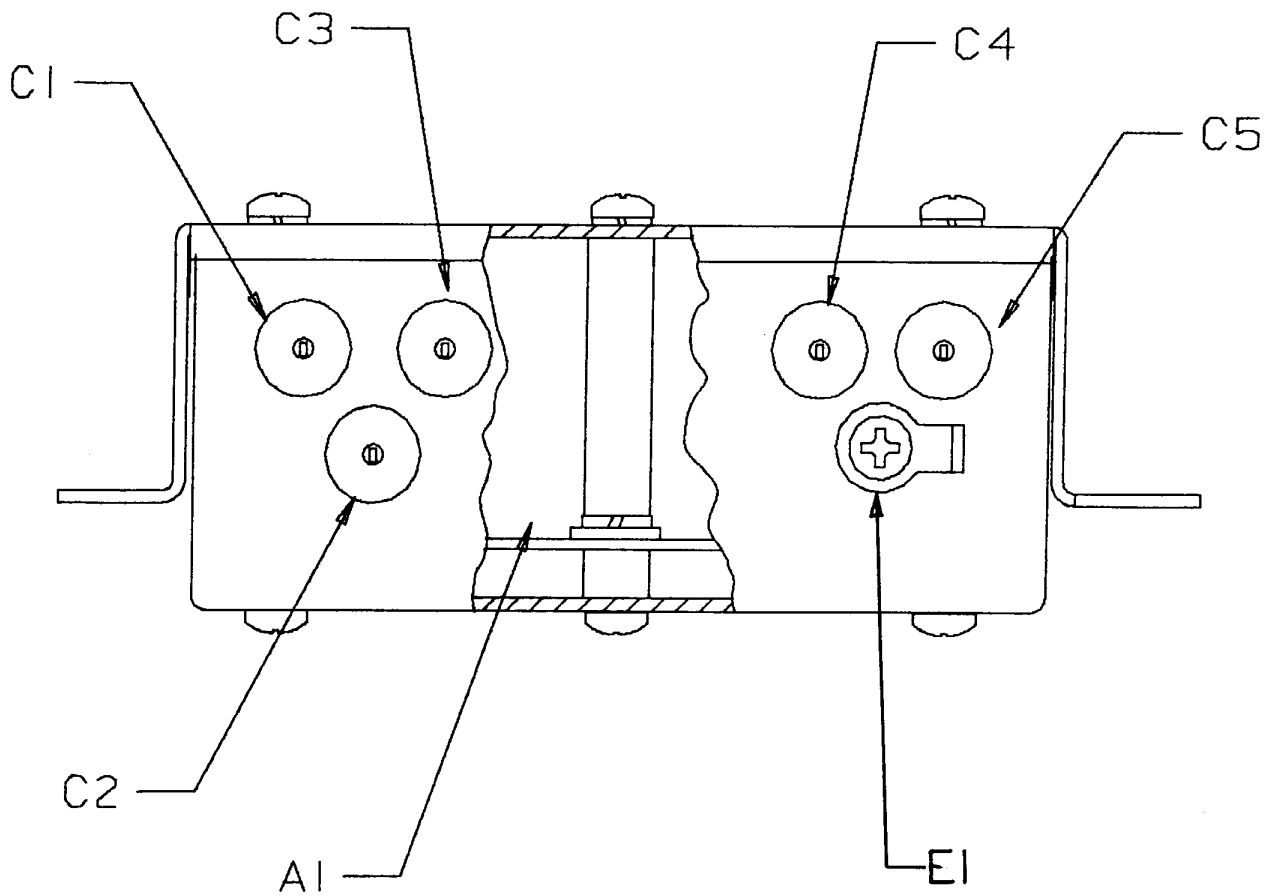
The -15 Vdc is applied to push/pull square wave oscillator Q1 and Q2 operating at approximately 15 kHz. T1 is a saturating transformer used to provide feedback and two output voltages. One output is rectified by fullwave bridge CR2-CR5 and filtered by pi-network C2-L1-C3 to provide 35 Vdc at 100 mA for display anode power. The second output is filtered by L2, C5, T2, and C6 to provide 5.8 Vac at 200 mA for display filament power. A bias voltage of approximately 6 Vdc is also supplied to the filaments. This bias voltage originates on the Driver Board Assembly A13A2 and is applied via a center tap at T2.

**7.2.1 Parts List and Schematic**

Table 14 is the Converter Assembly A13A6 parts list. Figure 15 is the Converter Assembly A13A6 component location diagram. Table 15 is the Converter Board Assembly A13A6A1 parts list. Figure 16 is the Converter Board Assembly A13A6A1 component location diagram and figure 17 is the A13A6 and A13A6A1 schematic diagram.

**Table 14. Converter Assembly A13A6 Parts List (PL 10073-2250)**

Ref. Desig.	Part Number	Description
A13A6	10073-2250	CONVERTER ASSY
A13A6A1	10073-2260	PWB ASSY, CONVERTER
C1	10073-7035	CAP,FEED-THRU 100
C2	10073-7035	CAP,FEED-THRU 100
C3	10073-7035	CAP,FEED-THRU 100
C4	10073-7035	CAP,FEED-THRU 100
C5	10073-7035	CAP,FEED-THRU 100
E1	E58-0004-000	LUG SLDR RIGHT ANGLE



**Figure 15. Converter Assembly A13A6 Component Location Diagram (10073-2250, Rev. E)**

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**Table 15. Converter Board Assembly A13A6A1 Parts List (PL 10073-2260)**

Ref. Desig.	Part Number	Description
	10073-2260	PWB, CONVERTER
C1	M39014/02-1305	CAP .047UF 10% 100V CER
C2	C26-0050-100	CAP 10UF 20% 50V TANT
C3	C26-0050-100	CAP 10UF 20% 50V TANT
C4	C18-0025-101	CAP 100UF 25V ELEC
C5	M39014/02-1318	CAP .33UF 10% 50V CER-R
C6	M39014/02-1318	CAP .33UF 10% 50V CER-R
C7	C26-0025-680	CAP 68UF 20% 25V TANT
CR1	1N4007	DIODE 1A 1000V RECT GP
CR2	D22-0007-002	DIODE 1A 100V RECT GP
CR3	D22-0007-002	DIODE 1A 100V RECT GP
CR4	D22-0007-002	DIODE 1A 100V RECT GP
CR5	D22-0007-002	DIODE 1A 100V RECT GP
CR6	D22-0007-002	DIODE 1A 100V RECT GP
CR7	D22-0007-002	DIODE 1A 100V RECT GP
L1	MS90538-12	COIL 100UH 5% FXD RF
L2	10073-7029	INDUCTOR, FILTER CHOKE
L3	10073-7029	INDUCTOR, FILTER CHOKE
Q1	2N5193	XSTR POWER PNP TO-205AA
Q2	2N5193	XSTR POWER PNP TO-205AA
R1	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R2	R65-0003-270	RES 27 5% 1/4W CAR FILM
R3	R65-0003-101	RES 100 5% 1/4W CAR FILM
R4	R65-0003-223	RES 22K 5% 1/4W CAR FILM
T1	10073-7027	TRANSFORMER, POWER
T2	10073-7028	TRANSFORMER, RF, FIXED

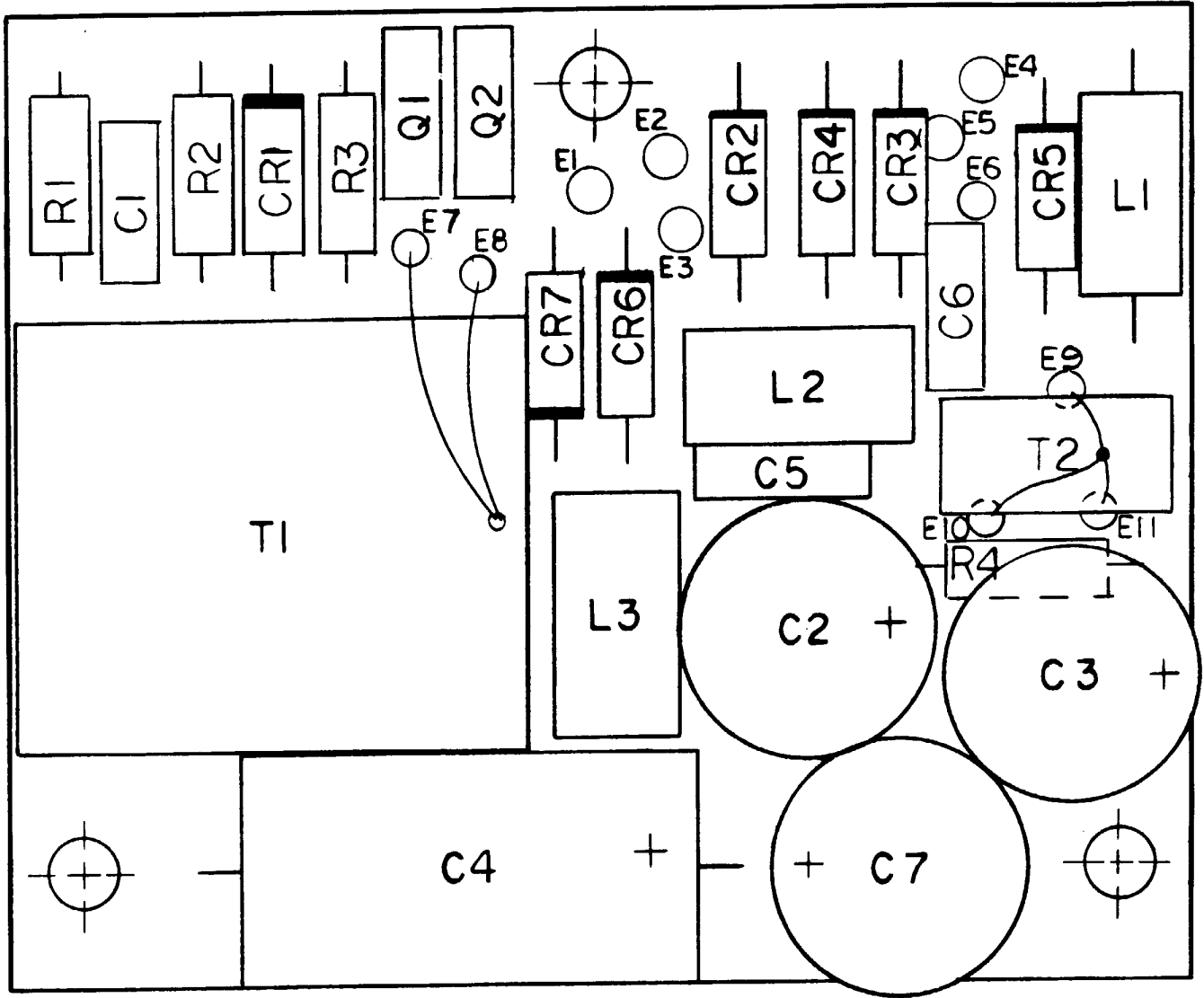


Figure 16. Converter Board Assembly A13A6A1 Component Location Diagram (10073-2260, Rev. D)





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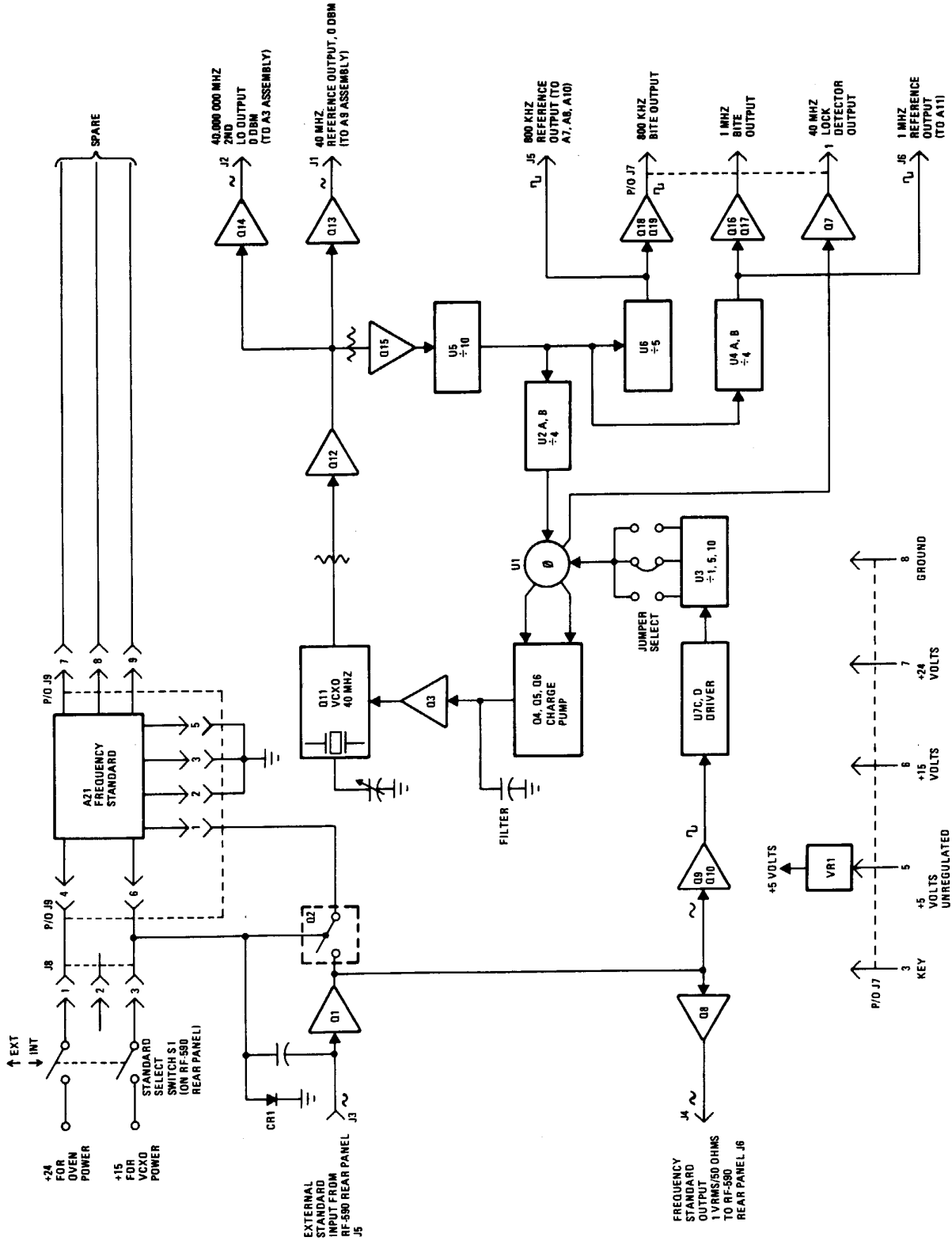
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Reference Generator Assembly A12/Frequency Standard Assembly A21 Functional Block Diagram

## 1. GENERAL DESCRIPTION

Reference Generator Assembly A12 is a single phased locked loop synthesizer which locks to a highly stable frequency standard and derives the various reference frequencies required to accurately control the RF-590.

The frequency standard employed may be either an internal or external standard and may be a 1, 5, or 10 MHz source. (A jumper connection on the A12 assembly must be configured to allow for the frequency of the standard chosen.)

Frequency Standard Assembly A21 supplied with the radio is a self contained, sealed unit which plugs directly into the A12 assembly via a nine pin connector. The following stability options are available.

- $\pm 1$  part in  $10^6$  per day, P/N 10073-6600, 5 MHz
- $\pm 1$  part in  $10^8$  per day, P/N 0759-3906, 1 MHz

Since the reference frequencies supplied by the A12 assembly are derived from the frequency standard used, they will have the same accuracy and stability as the standard. The following reference outputs are provided by the A12 assembly for RF-590 operation.

- 40 MHz - to Second Converter Assembly A3, 0 dBm
- 40 MHz - to PLL IV Assembly A9, 0 dBm
- 1 MHz - to BFO Synthesizer Assembly A11, TTL
- 800 kHz - to PLL II Assembly A7, TTL
- 800 kHz - to PLL III Assembly A8, TTL
- 800 kHz - to PLL V Assembly A10, TTL

Additionally, the RF-590 rear panel contains BNC type connector J6 allowing access to the buffered frequency standard output of 1 Vrms/50 ohms. BNC connector J5 provides a 50 ohm input for an external 1 Vrms frequency standard. Rear panel switch S1 (INT/EXT standard select) chooses the standard to be used.

## 2. INTERFACE CONNECTIONS

Table 1 details the A12 input/output connections and other relevant data.

Table 1. Reference Generator A12 Interface Connection

Connector	Function	Characteristics
J1	Second LO Output	40 MHz, 0 dBm, 50 ohms
J2	40 MHz Reference	40 MHz, 0 dBm, 50 ohms
J3	External Standard Input	1 Vrms, 50 ohms
J4	Standard Output	1 Vrms, 50 ohms
J5	800 kHz Reference Output	TTL
J6	1 MHz Reference Output	TTL
J7-1	40 MHz Lock Detector Output	0 Vdc = PLL Locked
J7-2	1 MHz BITE Output	0 Vdc = 1 MHz ok
J7-3	Key	
J7-4	800 kHz BITE Output	0 Vdc = 800 kHz ok
J7-5	+5 Volts Unregulated	200 mA
J7-6	+15 Volts	30 mA
J7-7	+24 Volts	10 mA
J7-8	Ground	
J8-1	A21 XTAL Oven Power	+24 (draws 100 mA only when $1 \times 10^{-8}$ ppm A21 option is chosen)
J8-2	Key	
J8-3	A21 TCXO Power	+15V, 100 mA
J9-1	Frequency Standard A21 Output	0.5 Vrms, 1, 5, or 10 MHz
J9-2	Gnd	
J9-3	Gnd	
J9-4	Same as J8-1	
J9-5	Gnd	

**Table 1. Reference Generator A12 Interface Connection (Cont.)**

Connector	Function	Characteristics
J9-6	Same as J8-3	
J9-7	Spare	
J9-8	Spare	
J9-9	Spare	

### 3. CIRCUIT DESCRIPTION

Voltage controlled crystal oscillator (VCXO) stage Q11 free runs at 40 MHz and provides all the outputs listed in section 1 after the required buffering and/or frequency division. The VCXO acquires its stability by providing a 1 MHz IF to one port of phase comparator U1 where phase comparison of the 1 MHz reference signal derived from the frequency standard occurs. Any difference in phase and/or frequency between these two signals produces an error signal by the phase comparator which causes the VCXO to tune in the direction which will reduce the error. In so doing, the VCXO frequency of 40 MHz acquires the stability and accuracy of the much lower frequency supplied by the frequency standard.

Note that many aspects of A12 operation are identical to the PLL description supplied in section 4 of this manual.

#### 3.1 Frequency Standard Assembly A21

The frequency standard supplied with the RF-590 is a self contained, sealed unit and plugs directly into A12 connector J9. The following stability options are available.

- $\pm 1$  part in  $10^6$  per day, P/N 10073-6600, 5 MHz
- $\pm 1$  part in  $10^8$  per day, P/N 0759-3906, 1 MHz

The  $1 \times 10^{-8}$  ppm option is referred to as the high stability option, and it uses a crystal oven for greater temperature stability.

#### 3.2 PLL Reference Generation

Phase comparator U1 obtains a 1.000000 MHz reference signal derived from either an internal or an external frequency standard whose frequency may be 1, 5, or 10 MHz. RF-590 rear panel INT/EXT standard select switch S1 chooses the desired source.

##### 3.2.1 Internal Standard Select

When the standard select switch is in the INT position, +24 volts and +15 volts are applied via J8 and J9 to Frequency Standard Assembly A21. (The +24 volt line draws no current unless the  $1 \times 10^{-8}$  ppm A21 option is employed. It feeds a spare pin on the  $1 \times 10^{-6}$  ppm.)

The +15 volts power the A21 TCXO, and causes a 0.5 Vrms signal at the A21 frequency to appear at J9 (pin 1) RF output. This signal is applied to switch Q2, which is biased on by the +15 volts. This allows the internal standard signal to pass. Simultaneously, the +15 volts biases PIN diode CR1 on, which provides a low impedance path to ground for any signals that might be at the J3 external standard input. The signal present at the Q1-Q2 output is applied via buffer Q8 through J4 to the RF-590 rear panel at a 1 Vrms/50 ohm level. It is also applied to limiter stage Q9-Q10 where it is converted to a TTL level to driver U7. U7 in turn drives divide by 1, 5, or 10 counter U3 which produces a constant 1 MHz reference output to U1. The actual divisor ratio depends upon the choice of frequency standard chosen, and is determined by the locations of a jumper wire on the A12 assembly at the U3 output. This jumper is normally factory set.

### 3.2.2 External Standard Select

When the standard select is in the EXT position, the +24 and +15 volts are removed from the A21 assembly turning it off. Simultaneously, +15 volts is removed from Q2 and CR1 turning them both off. Since the low impedance path to ground caused by CR1 is now a high impedance, signals at J3 from an external standard may pass unattenuated through Q1.

### 3.3 Phase Comparison Circuits

Phase comparator U1 compares the frequency standard derived 1 MHz reference signal to a VCO derived 1 MHz IF signal. When these two signals are equal in frequency and phase, U1 outputs at TP1 and TP2 are essentially 5 Vdc. This holds all transistors in the charge pump circuit (Q4, Q5, Q6) off. The dc voltage across C16 is constant, Q3 is conducting, and the control voltage developed across R13 at TP1 is constant. This holds the VCO frequency constant and equal to a multiple of the frequency standard.

Assume that the VCO frequency decreases due to temperature variations. This causes the 1 MHz IF frequency to decrease. Comparison at U1, pins 1 and 3, cause TP2 to pulse low, and in so doing, turn on Q6 since the Q6 base-emitter circuit is now forward biased. (Q5 remains off.) Q6 collector voltage drops and forward biases the Q4 base-emitter junction turning Q4 on. Q4 now starts driving charge into C16 raising the C16 potential. This in turn causes Q3 to conduct harder, and the control voltage developed across R13 at TP1 increases. As the control voltage increases, the VCO frequency increases until the IF frequency is again equal to the reference frequency at the U1 inputs. At this point, TP2 switches to +5 Vdc and equilibrium is obtained. C16 holds this higher dc level to maintain the new higher VCO frequency.

Assume that the VCO frequency increases. This causes the 1 MHz IF frequency to decrease. Comparison at U1, pins 1 and 3, cause TP3 to pulse low, and in so doing, bias Q5 into conduction. (Q6 and Q4 remain off.) C16 now has a low impedance discharge path and charge is drawn out. This drops its voltage. This causes Q3 to conduct less and less control voltage is developed across R13. As this voltage decreases, the VCO frequency decreases until the inputs at U1 are again equal in frequency/phase. At this point, TP3 switches to +5 Vdc and equilibrium is obtained. C16 holds this lower dc level to maintain the new lower VCO frequency.

### 3.4 VCXO Operation and Control

A charge pump circuit consisting of Q4, Q5, and Q6 in conjunction with filter network C16, C17, and R14 converts the two phase comparator outputs into an analog dc control voltage. Buffer amplifier Q3 applies this control voltage to varactor diodes CR7 and CR8 in the VCXO. As the capacitance of these diodes

change due to control voltage fluctuations, JFET oscillator stage Q11 shifts in frequency. This stage is crystal controlled by Y1 and operates at a nominal frequency of 40.000000 MHz. VCXO output passes through amplifier stages Q12, Q15, and onto divide by 10 counter U5. The 4 MHz from U5 is applied to divide by 4 counter U2 which applies a 1 MHz signal to the second port of phase comparator U1 to complete the feedback loop.

### **3.5 A12 Reference Generator Outputs**

The 40.000000 MHz from amplifier stage Q12 is amplified to 0 dBm by Q13 and applied through J1 to Second Converter Assembly A3 mixer U1 where it functions as a second local oscillator (LO) for the receiver.

Q12 also feeds amplifier stage Q14 which routes a 40.000000 MHz, 0 dBm signal to PLL IV Assembly A9 mixer U1 as an LO injection.

The 4 MHz from divider U5 is applied to divide by 5 counter U6. U6 TTL output at 800 kHz is fed through J5 to function as a reference signal for phase comparators on the A7, A8, and A10 assemblies. U5 also feeds 4 MHz to divide by 4 counter U4. U4 TTL output at 1 MHz is fed through U6 to function as a reference signal for beat frequency oscillator (BFO) Assembly A11.

### **3.6 BITE Circuits**

Q7 monitors the phase comparator (U1) outputs. If either output goes low and remains low for a period of time exceeding the time constant of R19-C19, one of the two diodes (CR5 or CR6) will conduct. This turns Q7 on and develops a +5 Vdc level indicating an out of lock condition. This immediately flags the BITE monitoring circuits on Control Assembly A14 to display a front panel fault light indicator.

The 800 kHz TTL signals from U6 feed detector stage Q18/Q19 and 1 MHz TTL signals from U4B feed detector stage Q16/Q17. Both these detectors will provide a 0 Vdc level when the 800 kHz and 1 MHz reference signals are present and a +5 Vdc level when they are not. These two signals are checked only when the receiver BITE self-test is actuated.

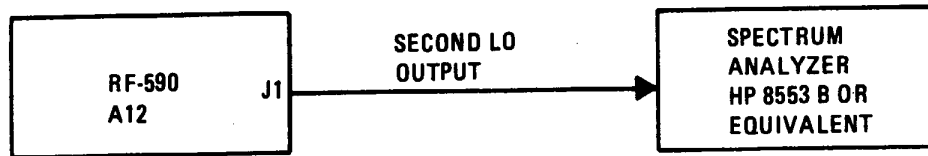
## **4. MAINTENANCE**

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. All tests are performed with all connections in normal contact unless otherwise specified.

### **4.1 40 MHz Outputs Adjustment**

Perform the following procedure to adjust the 40 MHz outputs.

- a. Connect equipment as shown in figure 1.



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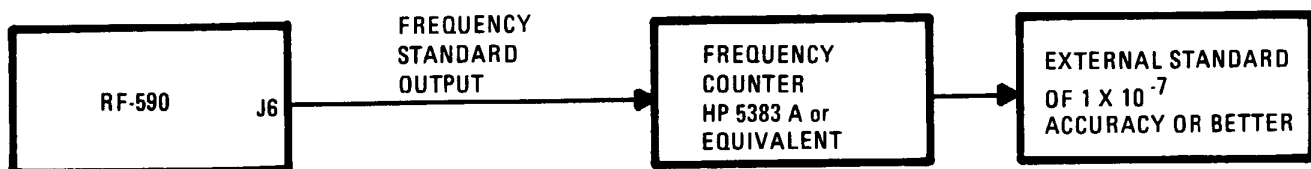
**Figure 1. 40 MHz Outputs Adjustment**

- b. Set receiver controls to the following:
- Frequency to 10.000000 MHz
  - Mode to USB
  - INT/EXT Standard to INT
- c. Monitoring J1, adjust T3 and then T4 for a peak indication at 40 MHz. (Approximately 0 dBm).
- d. Monitor J2 and adjust T5 for a peak indication at 40 MHz. (Approximately 0 dBm). Test is complete. Reconnect J1 and J2.

#### 4.2 A21 Frequency Standard Adjustment

Perform the following procedure to adjust the A21 frequency standard.

- a. Connect equipment as shown in figure 2. Set receiver INT/EXT Standard switch to INT.



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**Figure 2. A21 Frequency Standard Adjustment**



**NOTE**

The receiver should be on for at least 15 minutes prior to this alignment.

- b. Remove the screw on top of the A21 assembly to gain access to the frequency adjustment. Adjust this control (using a JFD-type nonmetallic alignment tool) to the frequency stamped on top of the assembly. (The accuracy of this setting is crucial to the VCO adjustment so perform this test carefully.)
- c. Test is complete. Replace screw in A21 assembly.

**4.3 VCO Adjustment**

Perform the following procedure to adjust the VCO.

- a. Make sure that the INT/EXT Standard switch is in the INT position and that the A21 frequency standard is properly adjusted on frequency.
- b. Monitor TP1 with a digital voltmeter. Adjust C36 for 7.4 Vdc. Test is complete.

**5. PARTS LIST**

Table 2 is a comprehensive parts list of all replaceable components in Reference Generator Assembly A12. When ordering parts from the factory, include a full description of the part. Use figure 3, Reference Generator Assembly A12 Component Location Diagram to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 4 is the Reference Generator Assembly A12 schematic diagram.

**Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700)**

Ref. Desig.	Part Number	Description
	10073-4700	PWB
	E70-0001-002	INSL BEO TO-5 X.030 THK
C1	M39014/02-1320	CAP .47UF 10% 50V CER-R
C2	M39014/02-1320	CAP .47UF 10% 50V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	C26-0025-339	CAP 3.3UF 20% 25V TANT
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	C26-0025-339	CAP 3.3UF 20% 25V TANT
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0025-339	CAP 3.3UF 20% 25V TANT
C9	M39014/01-1535	CAP .01UF 20% 100V CER
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R

**HARRIS**  
**RF COMMUNICATIONS**

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700) (Cont.)

Ref. Desig.	Part Number	Description
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	C26-0035-100	CAP 10UF 20% 35V TANT
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	C26-0025-470	CAP 47UF 20% 25V TANT
C16	C26-0025-339	CAP 3.3UF 20% 25V TANT
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	C25-0001-301	CAP 1.0UF 20% 20V TANT
C20	C26-0025-339	CAP 3.3UF 20% 25V TANT
C21	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	CK05BX102M	CAP 1000PF 20% 200V CER
C31	CK05BX102M	CAP 1000PF 20% 200V CER
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	C26-0025-680	CAP 68UF 20% 25V TANT
C34	M39014/01-1535	CAP .01UF 20% 100V CER
C35	CM04CD150J03	CAP 15PF 5% 500V MICA
C36	C85-0001-002	CAP 1.0-10PF 250V
C37	M39014/01-1535	CAP .01UF 20% 100V CER
C38	M39014/01-1535	CAP .01UF 20% 100V CER
C39	CM04ED470J03	CAP 47PF 5% 500V MICA
C40	M39014/01-1535	CAP .01UF 20% 100V CER
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C42	M39014/01-1535	CAP .01UF 20% 100V CER
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	M39014/01-1535	CAP .01UF 20% 100V CER
C45	CM04ED560J03	CAP 56PF 5% 500V MICA
C46	M39014/01-1535	CAP .01UF 20% 100V CER
C47	M39014/01-1535	CAP .01UF 20% 100V CER
C48	M39014/01-1535	CAP .01UF 20% 100V CER
C49	M39014/01-1535	CAP .01UF 20% 100V CER
C50	M39014/02-1310	CAP .1UF 10% 100V CER-R
C51	M39014/01-1535	CAP .01UF 20% 100V CER
C52	CM04ED560J03	CAP 56PF 5% 500V MICA
C53	M39014/01-1535	CAP .01UF 20% 100V CER
C54	M39014/01-1535	CAP .01UF 20% 100V CER
C55	M39014/02-1310	CAP .1UF 10% 100V CER-R



Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700) (Cont.)

Ref. Desig.	Part Number	Description
C56	M39014/01-1535	CAP .01UF 20% 100V CER
C57	M39014/01-1535	CAP .01UF 20% 100V CER
C58	M39014/01-1535	CAP .01UF 20% 100V CER
C59	M39014/02-1310	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310	CAP .1UF 10% 100V CER-R
C61	M39014/02-1310	CAP .1UF 10% 100V CER-R
C62	M39014/02-1310	CAP .1UF 10% 100V CER-R
C63	M39014/02-1310	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310	CAP .1UF 10% 100V CER-R
C65	C26-0016-151	CAP 150UF 20% 16V TANT
C66	M39014/02-1310	CAP .1UF 10% 100V CER-R
C67	M39014/02-1310	CAP .1UF 10% 100V CER-R
C68	C26-0025-100	CAP 10UF 20% 25V TANT
C69	M39014/02-1310	CAP .1UF 10% 100V CER-R
C70	M39014/02-1310	CAP .1UF 10% 100V CER-R
C71	C26-0050-100	CAP 10UF 20% 50V TANT
C72	M39014/02-1310	CAP .1UF 10% 100V CER-R
C73	M39014/02-1310	CAP .1UF 10% 100V CER-R
C74	C26-0025-470	CAP 47UF 20% 25V TANT
C75	M39014/02-1310	CAP .1UF 10% 100V CER-R
C76	CK05BX102M	CAP 1000PF 20% 200V CER
C77	M39014/01-1535	CAP .01UF 20% 100V CER
C78	M39014/02-1310	CAP .1UF 10% 100V CER-R
C79	CK05BX102M	CAP 1000PF 20% 200V CER
C80	M39014/01-1535	CAP .01UF 20% 100V CER
C81	M39014/01-1535	CAP .01UF 20% 100V CER
C82	M39014/02-1310	CAP .1UF 10% 100V CER-R
C83	M39014/02-1310	CAP .1UF 10% 100V CER-R
C84	M39014/01-1535	CAP .01UF 20% 100V CER
C85	M39014/01-1535	CAP .01UF 20% 100V CER
C86	M39014/01-1535	CAP .01UF 20% 100V CER
C87	10121-4720	CAP, TEMP COMP, 10
CR1	D12-0007-001	DIODE 1W 75V PIN SW
CR2	1N3064	DIODE 75mA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N3064	DIODE 75mA 75V SW
CR7	10073-7118	DIODE, SILICON, HYPERABRUPT
CR8	10073-7118	DIODE, SILICON, HYPERABRUPT
CR9	1N3064	DIODE 75mA 75V SW
CR10	1N3064	DIODE 75mA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F

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**RF COMMUNICATIONS**

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700) (Cont.)

Ref. Desig.	Part Number	Description
J4	J-0031	CONN SMB VERT PCB F
J5	J-0031	CONN SMB VERT PCB F
J6	J-0031	CONN SMB VERT PCB F
J7	J46-0032-008	HDR 8 PIN 0.100" SR
J8	J46-0022-003	HDR 3 PIN, SINGLE
J9	10073-7045	CONNECTOR, 9 PIN
J10	J-0031	CONNECTOR SMB VERT PCB F
L1	MS75085-7	COIL 100UH 10% FXD RF
L2	MS75085-7	COIL 100UH 10% FXD RF
L3	MS75084-12	COIL 10UH 10% FXD RF
L4	MS75083-9	COIL .56UH 10% FXD RF
L5	MS75084-12	COIL 10UH 10% FXD RF
L6	MS75084-5	COIL 2.7UH 10% FXD RF
L7	MS75084-12	COIL 10UH 10% FXD RF
L8	MS75084-12	COIL 10UH 10% FXD RF
L9	MS75085-7	COIL 100UH 10% FXD RF
L10	MS75084-12	COIL 10UH 10% FXD RF
L11	L08-0001-001	CHOKE W B 50 MHZ
L12	L08-0001-001	CHOKE W B 50 MHZ
L13	L08-0001-001	CHOKE W B 50 MHZ
L14	MS75084-3	COIL 1.8UH 10% FXD RF
Q1	2N3227	XSTR SS/GP NPN TO-18
Q2	2N3227	XSTR SS/GP NPN TO-18
Q3	Q05-0001-000	XSTR JFET N-CH
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	2N2222	XSTR SS/GP NPN TO-18
Q6	2N2222	XSTR SS/GP NPN TO-18
Q7	2N2907	XSTR SS/GP PNP TO-18
Q8	2N3866	XSTR SS/RF NPN TO-39
Q9	Q-0153	XSTR SS/RF PN4258
Q10	2N2369	XSTR SS/RF NPN
Q11	Q35-0003-000	XSTR U310 JFET HIGH GM
Q12	Q35-0003-000	XSTR U310 JFET HIGH GM
Q13	Q35-0003-000	XSTR U310 JFET HIGH GM
Q14	Q35-0003-000	XSTR U310 JFET HIGH GM
Q15	Q35-0003-000	XSTR U310 JFET HIGH GM
Q16	2N2907	XSTR SS/GP PNP TO-18
Q17	2N2222	XSTR SS/GP NPN TO-18
Q18	2N2907	XSTR SS/GP PNP TO-18
Q19	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-471	RES 470 5% 1/4W CAR FILM
R2	R65-0003-471	RES 470 5% 1/4W CAR FILM
R3	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R4	R65-0003-101	RES 100 5% 1/4W CAR FILM
R5	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R6	R65-0003-620	RES 62 5% 1/4W CAR FILM

 **HARRIS**  
**RF COMMUNICATIONS**

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700) (Cont.)

Ref. Desig.	Part Number	Description
R7	R65-0003-561	RES 560 5% 1/4W CAR FILM
R8	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R9	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R10	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R11	R65-0003-101	RES 100 5% 1/4W CAR FILM
R12	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R13	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R14	RN55D2211F	RES,2210 1% 1/8W MET FLM
R15	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R16	RN55D2002F	RES,20.0K 1% 1/8W MET FLM
R17	RN55D3321F	RES,3320 1% 1/8W MET FLM
R18	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R19	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R20	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R21	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R22	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R23	R65-0003-100	RES 10 5% 1/4W CAR FILM
R24	R65-0003-201	RES 200 5% 1/4W CAR FILM
R25	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R26	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R27	R65-0003-180	RES 18 5% 1/4W CAR FILM
R28	R65-0003-470	RES 47 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R31	R65-0003-241	RES 240 5% 1/4W CAR FILM
R32	R65-0003-270	RES 27 5% 1/4W CAR FILM
R33	R65-0003-331	RES 330 5% 1/4W CAR FILM
R34	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R35	R65-0003-391	RES 390 5% 1/4W CAR FILM
R36	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R37	R65-0003-201	RES 200 5% 1/4W CAR FILM
R38	R65-0003-201	RES 200 5% 1/4W CAR FILM
R39	R65-0003-101	RES 100 5% 1/4W CAR FILM
R40	R65-0003-201	RES 200 5% 1/4W CAR FILM
R42	R65-0003-101	RES 100 5% 1/4W CAR FILM
R44	R65-0003-201	RES 200 5% 1/4W CAR FILM
R45	R65-0003-751	RES 750 5% 1/4W CAR FILM
R46	R65-0003-751	RES 750 5% 1/4W CAR FILM
R47	R65-0003-201	RES 200 5% 1/4W CAR FILM
R49	R65-0003-101	RES 100 5% 1/4W CAR FILM
R50	R65-0003-201	RES 200 5% 1/4W CAR FILM
R51	R65-0003-101	RES 100 5% 1/4W CAR FILM
R52	R65-0003-101	RES 100 5% 1/4W CAR FILM
R53	R65-0003-201	RES 200 5% 1/4W CAR FILM
R54	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

 **HARRIS**  
**RF COMMUNICATIONS**

**Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700) (Cont.)**

Ref. Desig.	Part Number	Description
R55	R65-0003-510	RES 51 5% 1/4W CAR FILM
R56	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R57	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R58	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R59	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R60	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R61	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R62	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R63	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R64	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R65	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R66	R65-0003-224	RES 220K 5% 1/4W CAR FILM
T1	10073-7006	TRANSFORMER, RF, FIXED
T2	10073-7007	TRANSFORMER, RF, FIXED
T3	10073-7009	TRANSFORMER, RF, VARIABLE
T4	10073-7009	TRANSFORMER, RF, VARIABLE
T5	10073-7009	TRANSFORMER, RF, VARIABLE
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	IC-0430	IC MC4044 CERAMIC CMOS
U2	105-0000-074	IC 74LS74 PLASTIC TTL
U3	105-0000-090	IC 74LS90 PLASTIC TTL
U4	105-0000-074	IC 74LS74 PLASTIC TTL
U5	165-0004-001	IC 12013 PLASTIC ECL
U6	105-0000-090	IC 74LS90 PLASTIC TTL
U7	105-0000-000	IC 74LS00 PLASTIC TTL
VR1	111-0001-001	IC VR 7805 + 5V 1.5A 4%
Y1	10073-4720	CRYSTAL, 40 MHZ

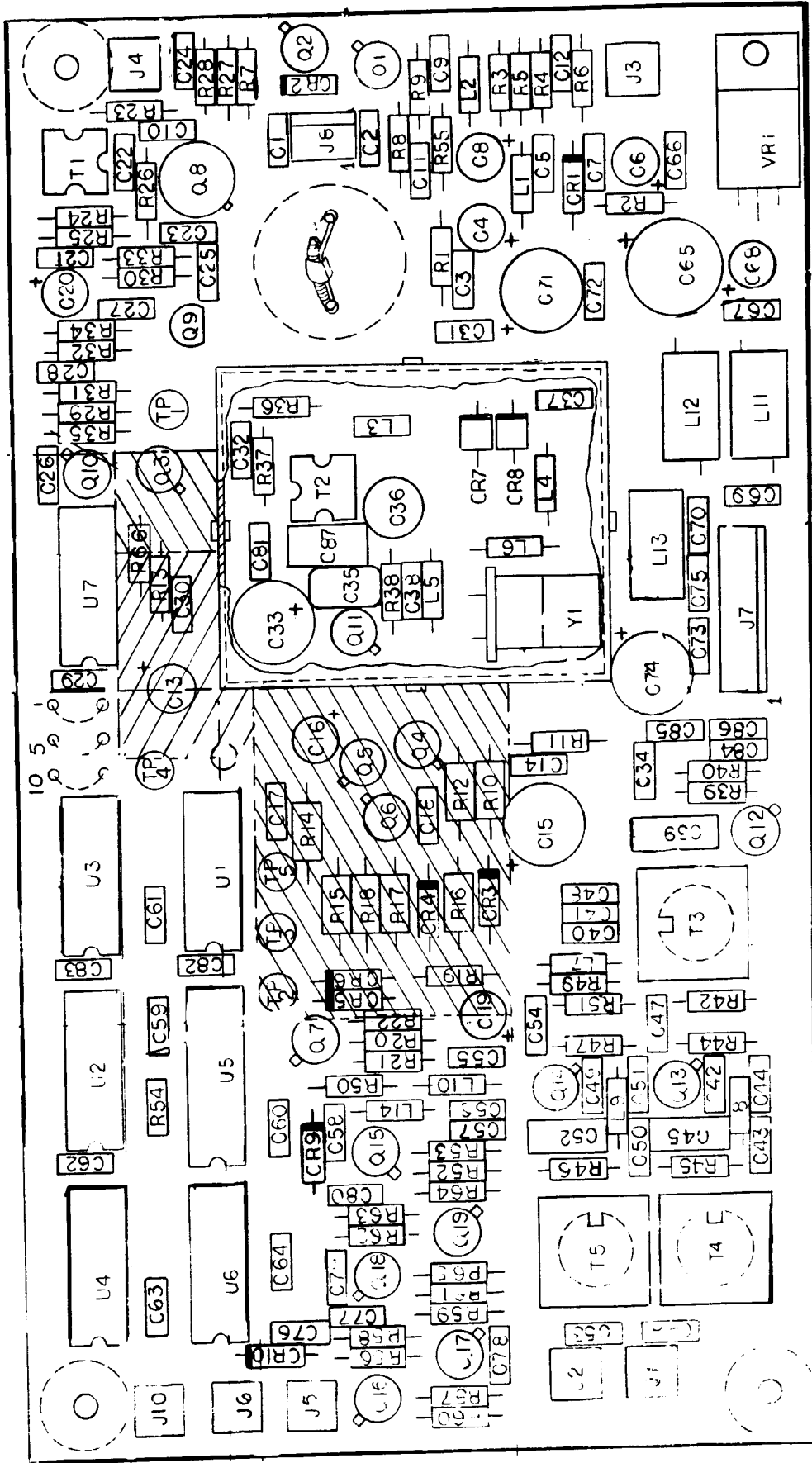
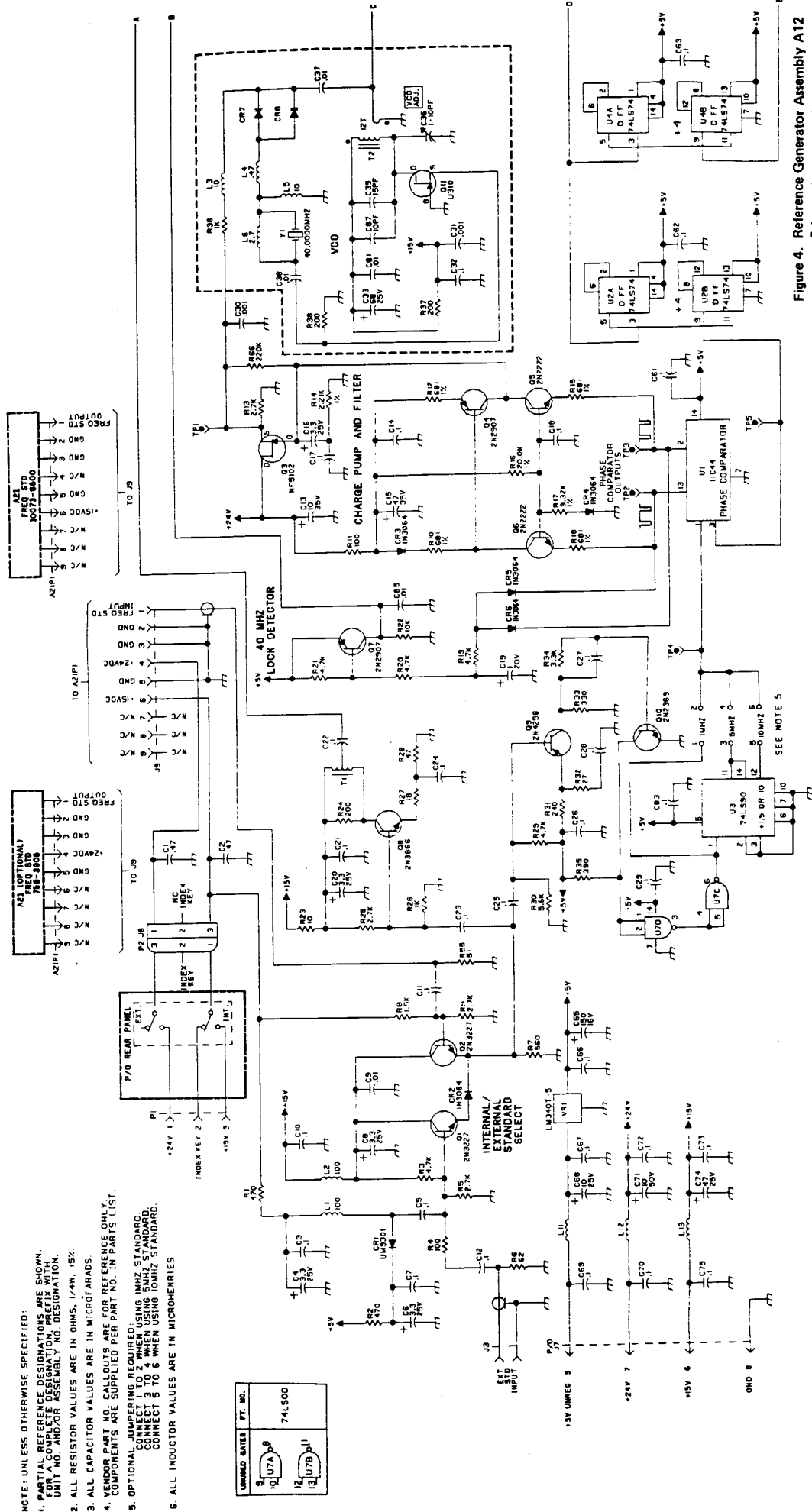


Figure 3. Reference Generator Assembly A12 Component Location Diagram (10073-4700, Rev. E)



- NOTE: UNLESS OTHERWISE SPECIFIED:
- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, SEE THE UNIT, NC, AND/OR ASSEMBLY NO. DESIGNATION.
  - ALL RESISTOR VALUES ARE IN OHMS, 1/K $\Omega$ , 1/M $\Omega$ , 15K.
  - ALL CAPACITOR VALUES ARE IN MICROFARADS.
  - VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  - OPTIONAL JUMPING REQUIRED:  
CONNECT 1 TO 2 WHEN USING 1MHZ STANDARD.  
CONNECT 1 TO 3 WHEN USING 10MHZ STANDARD.  
CONNECT 3 TO 6 WHEN USING 100MHZ STANDARD.
  - ALL INDUCTOR VALUES ARE IN MICROHENRIES.

Figure 4. Reference Generator Assembly A12  
Schematic Diagram (10073-4701, Rev. H)  
(Sheet 1 of 2)



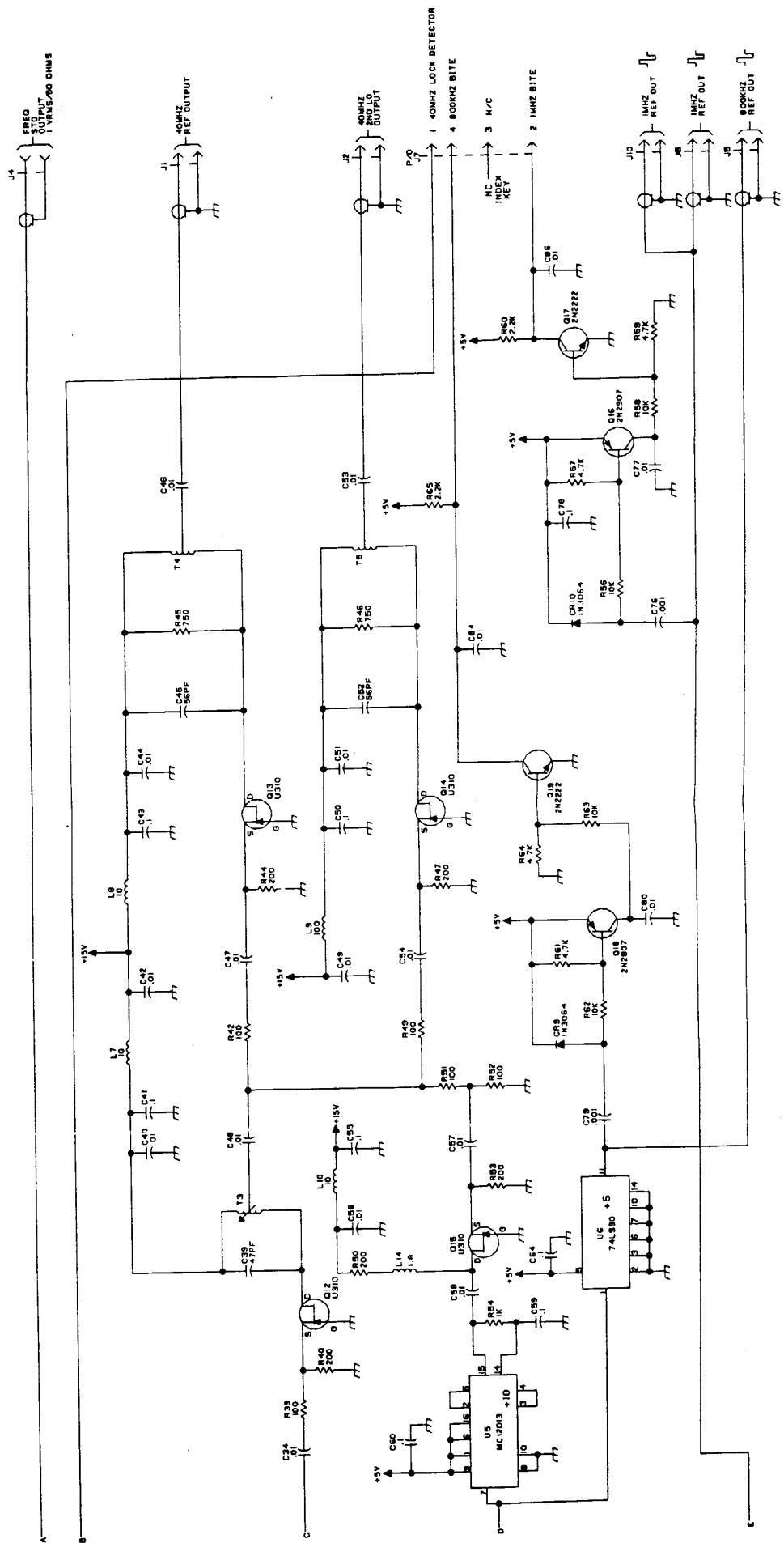
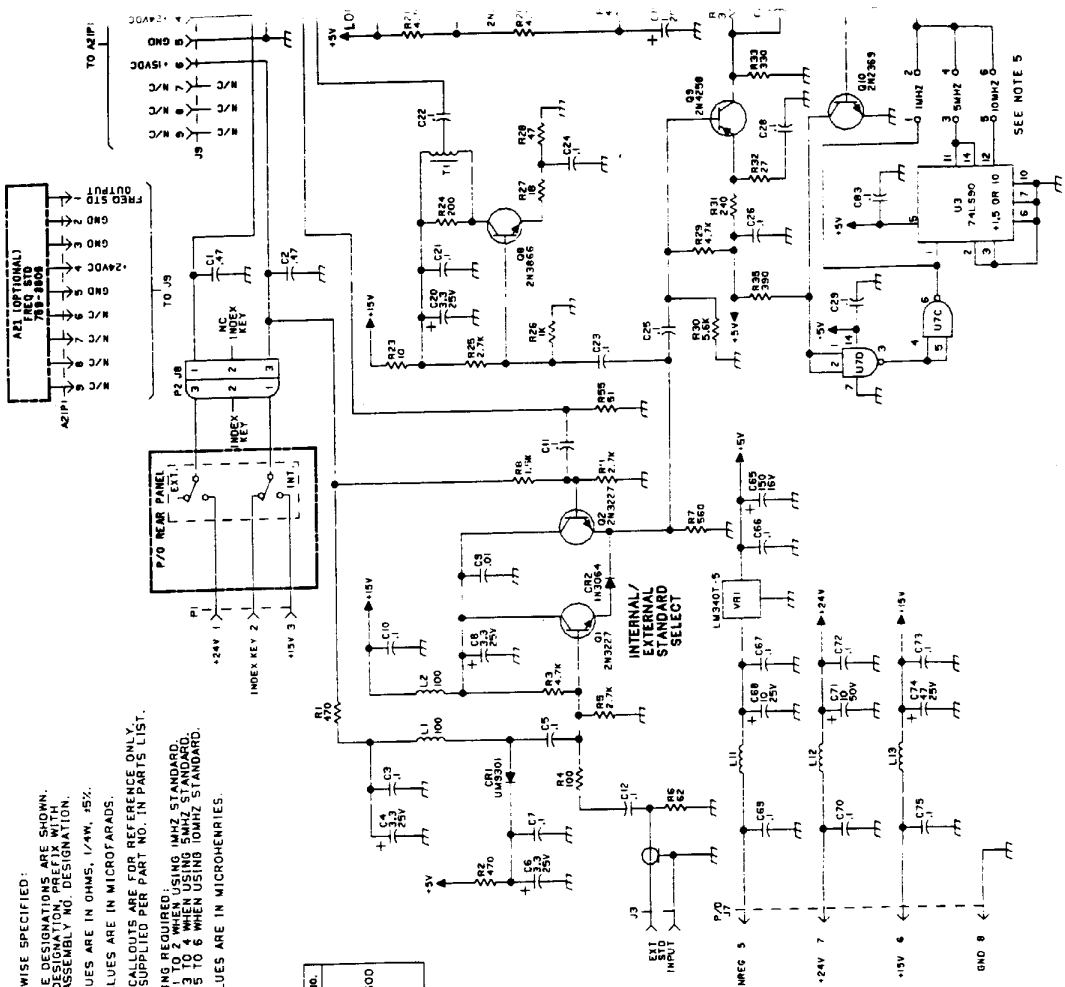


Figure 4. Reference Generator Assembly A12  
Schematic Diagram (10073-4701, Rev. H)  
(Sheet 2 of 2)



- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. VENDOR PART NO. CAPACITORS ARE OR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  5. OPTIONAL JUMPING REQUIRED. USING 1MHZ STANDARD. CONNECT 3 TO 4 WHEN USING 5MHZ STANDARD. CONNECT 5 TO 6 WHEN USING 10MHZ STANDARD.
  6. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

UNWID GATES	P.T. NO.
	74LS00

SEE NOTE 5

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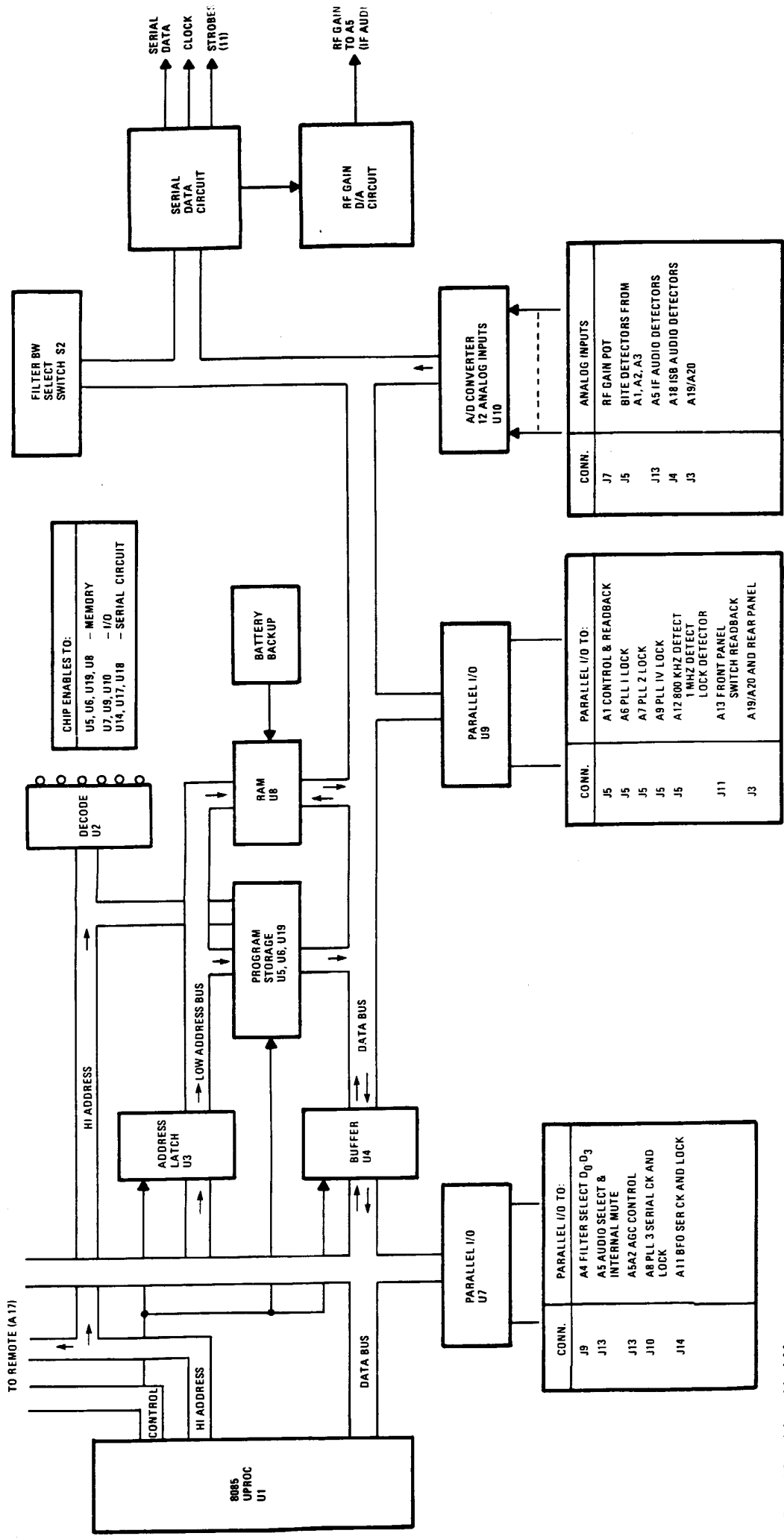
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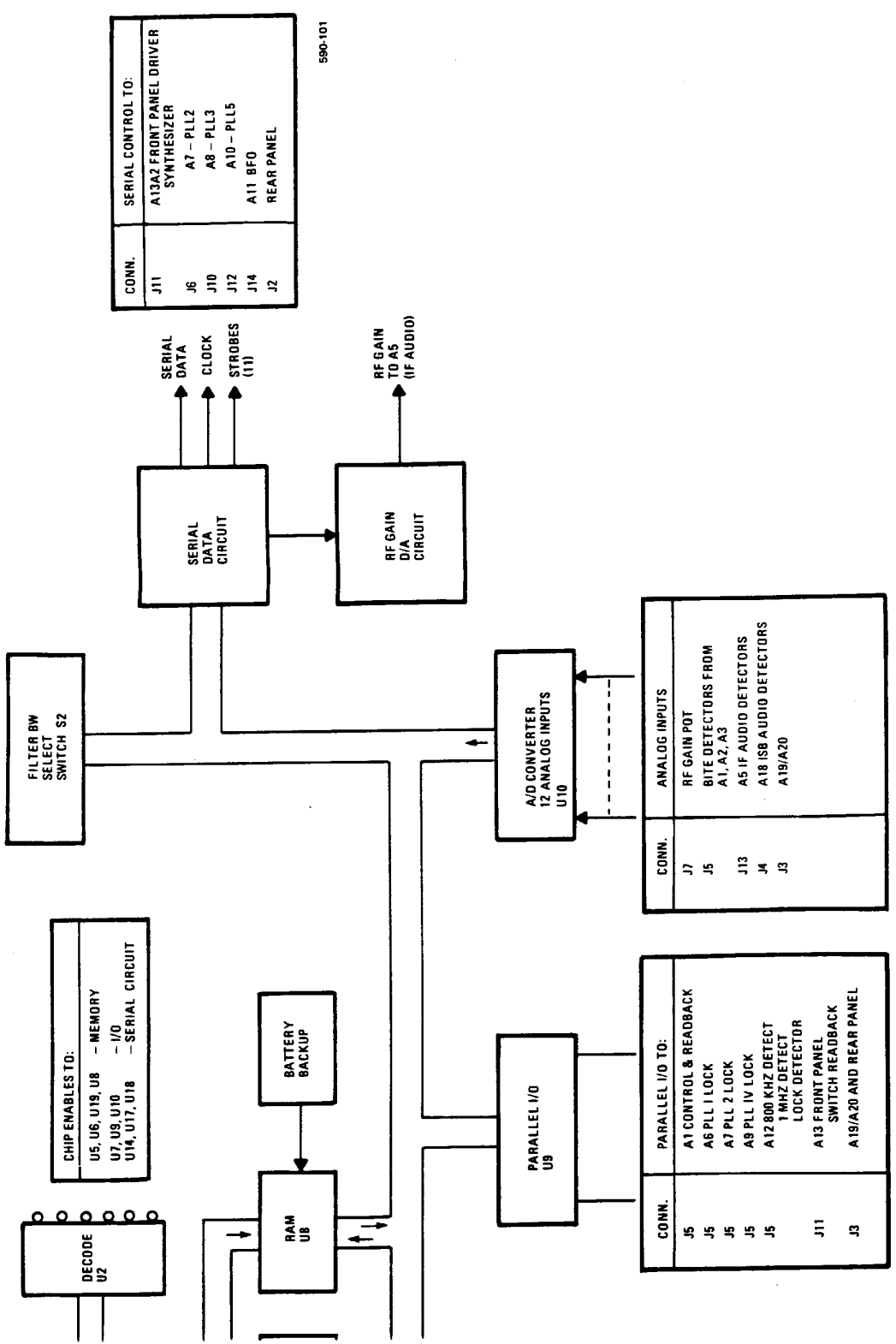
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Control Board Assembly A14  
Functional Block Diagram



590-101

CONN.	SERIAL CONTROL TO:
J11	A13A2 FRONT PANEL DRIVER
J6	SYNTHESIZER
J10	A7 - PLL2
J12	A8 - PLL3
J14	A10 - PLL5
J2	A11 BFO REAR PANEL

CONN.	ANALOG INPUTS
J7	RF GAIN POT
J5	BIT DETECTORS FROM A1, A2, A3
J13	A5 IF AUDIO DETECTORS
J4	A18 ISB AUDIO DETECTORS
J3	A19/A20

CONN.	PARALLEL I/O TO:
J5	A1 CONTROL & READBACK
J5	A6 PLL 1 LOCK
J5	A7 PLL 2 LOCK
J5	A9 PLL IV LOCK
J5	A12 800 KHZ DETECT 1 MHZ DETECT
J11	LOCK DETECTOR
J3	A13 FRONT PANEL SWITCH READBACK
	A19/A20 AND REAR PANEL

## 1. GENERAL DESCRIPTION

CPU PWB A14 contains the 8085A CPU and associated peripheral circuits, serial data transmission circuits, parallel I/O circuits, and analog-to-digital as well as digital-to-analog converter circuitry. Functioning as the control element of the RF-590, this assembly is responsible for accepting input from the front panel and receiver assemblies as well as generating the digital signals necessary to control the receiver. Software contained within the three, 4K byte EPROMs is executed to supervise, control, and in the BITE process, test the display, control, and radio circuitry. Random access read/write memory (RAM) is used for temporary storage by the software program and for battery backed storage of receiver setups, programmed channels, and channel groups.

## 2. INTERFACE CONNECTIONS

All Control PWB interface connections are shown in table 1 and schematic diagram.

**Table 1. Control Board Assembly A14 Interface Summary**

Connector	Function	To	From
A14J1-1	N/C	—	—
-2	Index Key	—	—
-3	+5V	—	A15J3-9
-4	+5V	—	A15J3-21
A14J2-1	Remote Out 1	J7-1	—
-2	Serial Strobe 2	J7-20	—
-3	Gnd	J7-2	—
-4	N/C	—	—
-5	Scan Step	—	J7-3
-6	Remote Out 2	J7-22	—
-7	Remote Out 0	J7-4	—
-8	Serial Strobe 1	J7-23	—
-9	Stop Scan	—	J7-5
-10	Serial Clock	J7-24	—
-11	N/C	—	—
-12	Serial Data	J7-25	—
-13	Ext. Mute	—	J7-7
-14	Fault	J7-16	—
A14J3-1	Noise Bank	—	A19J1-1
-2	Filter Id	—	A19J1-2
-3	Overload	—	A19J1-3
-4	Conv. Id	—	A19J1-4
-5	Osc. Enable	A19J1-5	—
-6	Index Key	—	—

**HARRIS**  
**RF COMMUNICATIONS**

**Table 1. Control Board Assembly A14 Interface Summary (Cont.)**

Connector	Function	To	From
A14J3-7 -8 -9 -10	Ext. Mute Enable Serial Data Serial Clock	A19J1-7 A19J1-8 A19J1-9 A19J1-10	— — — —
A14J4-1 -2 -3 -4 -5 -6 -7 -8 -9 -10	N/C Int. Mute Det. IF Input Det. Line Audio AGC Line Audio Adj. Ext. Mute Index Key ISB Audio Meter ISB AGC Meter	— A18J1-9 — — — A18J1-5 A18J1-4 — — —	— — A18J1-8 A18J1-7 A18J1-6 — — — A18J1-2 A18J1-1
A15J5-1 -2 -3 4 -5 -6 -7 -8 -9 -10 -11 -12 -13 -14	N/C A3 Det. A2 Det. A1 Ext. Mute A1 Relay Control A1 Relay Test A1 BITE Osc. Enab. A1 Ant. Overload A1 BITE Det. Out A6 PLL I Lock Det A9 PLL IV Lock Det A12 800 kHz Det A12 1 MHz Det A12 40 MHz PLL Lock Det	— — — A16A3J3-1 A16A3J3-4 A16A3J3-5 A16A3J3-6 — — — — — — —	— A16A2J2-3 A16A2J2-4 — — — — A16A3J3-7 A16A3J3-8 A16A3J1-1 A16A3J1-3 A16A3J1-4 A16A3J1-5 A16A3J1-6
A14J6-1 -2 -3 -4 -5 -6 -7 -8	Serial Data Serial Clock Index Key Serial Check Enable PLL II Lock Det Gnd N/C	A7J1-1 A7J1-2 — — A7J1-5 — A7J1-7 —	— — — A7J1-4 — A7J1-6 — —

**Table 1. Control Board Assembly A14 Interface Summary (Cont.)**

Connector	Function	To	From
A14J7-1	LSB Select	—	A13A3J1-1
-2	ISB AGC Meter	A13A3J1-2	—
-3	RF Gain	—	A13A3J1-3
-4	ISB Audio	A13A3J1-4	—
-5	-15V	A13A3J1-5	—
-6	LSB Audio Adj.	—	A13A3J1-6
-7	N/C	—	—
-8	+5V Ref.	A13A3J1-8	—
-9	Gnd	A13A3J1-9	—
-10	+15V	A13A3J1-10	—
A14J8-1	BITE P/S	—	A15J3-22
-2	N/C	—	—
-3	+15V	—	A15J3-23
-4	-15V	—	A15J3-11
-5	Index Key	—	—
-6	+8.5V	—	A15J3-12
-7	Gnd	—	A15J3-25
-8	Gnd	—	A15J3-13
A14J9-1	N/C	—	—
-2	N/C	—	—
-3	D3	A4J5-9	—
-4	D0	A4J5-8	—
-5	D2	A4J5-7	—
-6	Index Key	—	—
-7	D1	A4J5-5	—
-8	Gnd	A4J5-4	—
A14J10-1	Serial Data	A8J4-1	—
-2	Serial Clock	A8J4-2	—
-3	Index Key	—	—
-4	Serial Check	—	A8J4-4
-5	Enable	A8J4-5	—
-6	PLL III Lock Det	—	A8J4-6
-7	Gnd	A8J4-7	—
-8	N/C	—	—
A14J11-1	Twhl Int	—	A13A2J1-1
-2	Serial Data	A13A2J1-2	—
-3	Twhl Direction	—	A13A2J1-3



**HARRIS**  
**RF COMMUNICATIONS**

**Table 1. Control Board Assembly A14 Interface Summary (Cont.)**

Connector	Function	To	From
A14J11-4	Serial Clock	A13A2J1-4	—
-5	Twhl Reset	A13A2J1-5	—
-6	-15V	A13A2J1-6	—
-7	+5V	A13A2J1-7	—
-8	BITE P/S	A13A2J1-8	—
-9	PB3	A13A2J1-9	—
-10	Kybd Strobe	A13A2J1-10	—
-11	PB2	A13A2J1-11	—
-12	Fault	—	A13A2J1-12
-13	PB1	A13A2J1-13	—
-14	Display Strobe	A13A2J1-14	—
-15	PB0	A13A2J1-15	—
-16	Reset	A13A2J1-16	—
-17	N/C	—	—
-18	Gnd	A13A2J1-18	—
-19	+8.5V	A13A2J1-19	—
-20	Gnd	A13A2J1-20	—
A14J12-1	Serial Data	A10J1-1	—
-2	Serial Clock	A10J1-2	—
-3	Index Key	—	—
-4	Serial Check	—	A10J1-4
-5	Enable	A10J1-5	—
-6	PLL V Lock Det	—	A10J1-6
-7	Gnd	A10J1-7	—
-8	N/C	—	—
A14J13-1	Gnd	A5J6-1	—
-2	RF Gain 0-10V	A5J6-2	—
-3	Data AGC	—	—
-4	AGC Off	A5J6-4	—
-5	C Audio Select	A5J6-5	—
-6	Int. Mute	A5J6-6	—
-7	B Audio Select	A5J6-7	—
-8	AGC Fast	A5J6-8	—
-9	A Audio Select	A5J6-9	—
-10	AGC Medium	A5J6-10	—
-11	Ext. Mute	A5J6-11	—
-12	Line Audio	—	A5J6-12
-13	Line Audio Gnd	—	A5J6-13

 **HARRIS**  
**RF COMMUNICATIONS**

**Table 1. Control Board Assembly A14 Interface Summary (Cont.)**

Connector	Function	To	From
A14J13-14	Line Audio Det Out	—	A5J6-14
-15	IF Input Det	—	A5J6-15
-16	Second IF AGC	—	A5J6-16
A14J14-1	Serial Data	A11J4-1	—
-2	Serial Clock	A11J4-2	—
-3	Index Key	—	—
-4	Serial Check 1	—	A11J4-4
-5	Enable	A11J4-5	—
6	BFO Lock Detect	—	A11J4-6
-7	Gnd	A11J4-7	—
-8	BFO On/Off	A11J4-8	—
A14J15-1	+8.5V	A17J1-1	—
-2	+8.5V	A17J1-2	—
-3	Reset Out	A17J1-3	—
-4	HOLD	—	A17J1-4
-5	Line Audio	A17J1-5	—
-6	HLDA	A17J1-6	—
-7	Line Audio Gnd	A17J1-7	—
-8	CPU Clk Out	A17J1-8	—
-9	+15V	A17J1-9	—
-10	Gnd	A17J1-10	—
-11	Ready	—	A17J1-11
-12	-15V	A17J1-12	—
-13	RST 5.5	—	A17J1-13
-14	IO/M	A17J1-14	—
-15	INTR	—	A17J1-15
-16	S1	A17J1-16	—
-17	WR	A17J1-17	—
-18	RD	A17J1-18	—
-19	INTA	A17J1-19	—
-20	ALE	A17J1-20	—
-21	N/C	—	—
-22	N/C	—	—
-23	AD0	A17J2-3	Bi direc
-24	N/C	—	—
-25	AD1	A17J2-5	Bi direc
-26	A15	A17J2-6	—
-27	AD2	A17J2-7	Bi direc
-28	A14	A17J2-8	—

**Table 1. Control Board Assembly A14 Interface Summary (Cont.)**

Control	Function	To	From
A14J15-29	AD3	A17J2-9	Bi direc
-30	A13	A17J2-10	—
-31	AD4	A17J2-11	Bi direc
-32	A12	A17J2-12	—
-33	AD5	A17J2-13	Bi direc
-34	A11	A17J2-14	—
-35	AD6	A17J2-15	Bi direc
-36	A10	A17J2-16	—
-37	AD7	A17J2-17	Bi direc
-38	A9	A17J2-18	—
-39	Gnd	A17J2-19	—
-40	A8	A17J2-20	—

### 3. FUNCTIONAL DESCRIPTION

#### 3.1 CPU and Interface

The 8085A microprocessor (U1) executes the application program. The 6.0 MHz frequency of crystal Y1 is divided by two within U1 to yield the 3.0 MHz processor timing (333 nanosecond cycle time). The high order address bits of the CPU are inputs to address decoder U2, producing one of ten, active low chip selects to peripheral circuits. The multiplexed low address/data (AD) bus from U1 is input to low address latch U3 and bidirectional buffer U4. The control lines  $\overline{RD}$  and  $\overline{WR}$  are buffered by two gates of U23, with highest address line A15 and interrupt lines gated through U22 to control direction of U4. The  $\overline{RD}$  and  $\overline{WR}$  signals are combined with several of the enable outputs of U2 through U24 to produce chip selects for several devices. The major outputs of the microprocessor are also run to connector J15 for access to the installed remote; with R22, R23, R24, and R37 holding the lines at their proper logic levels. R26 and R36 act as pullup termination to the address and data busses, respectively. The high active interrupt lines of the CPU are dedicated as follows.

- RST 7.5 uses the real-time clock
- RST 6.5 handles the tune knob encoder interrupt
- RST 5.5 is used by the remote control option

#### 3.2 Reset and Trap

When the receiver power is turned on, the RC network (formed by R10 and C26) holds the processor RESET IN input low for about 100 milliseconds. This allows the power supplies time to stabilize before the

CPU starts running. Diode CR4 and Q2 detect a falling +5 V supply and pull the  $\overline{\text{RESET IN}}$  input low to avoid spurious operation on receiver power down or power loss. At such times, the chip select to CMOS RAM U8 is disabled by FET Q5, before the RAM enters its battery-backed condition.

During normal program execution, the microprocessor SOD output sends a low active pulse to the re-triggerable one-shot U20 every millisecond. If the CPU is so affected by noise on the busses or some other failure that it fails to do this, the one-shot will time out and restart the microprocessor through the 8085A TRAP input. Components C20 and R9 set this one-shot timeout to 50 milliseconds. The one-shot is also reset on powerup.

### 3.3 Memory

The firmware program is stored in the three 2732 4K byte EPROMS U5, U6, and U19. The program steps and data contained in these devices are accessed by the chip selects from U2 to each EPROM, gated onto the data bus with an output enable from the RD signal.

The information stored in the EPROMS is part of the RF-590 software and cannot be altered by the customer.

**CAUTION**

EPROMs are ultraviolet erasable over extended periods of exposure to fluorescent light or sunlight which can erase the memory information. Do not remove the opaque protective shield on these devices.

The 8155 circuit (U7) contains 256 bytes of RAM which are used for temporary storage by the software program. This device also contains a programmable timer which is conditioned to output a 1 kHz square wave to the RST 7.5 interrupt input of the CPU. This signal is the real time clock which is used to time and coordinate many RF-590 processes.

**CAUTION**

Do not short out the memory backup battery terminals. This could result in severe circuit damage.

The 6516 2K byte static CMOS RAM (U8) contains the channel storage. A fully charged battery BT1 in the backup power supply should maintain channel storage for one month. In normal receiver operation, the trickle charge circuit will recharge a dead battery in 24 hours. Terminals E1-E2 left unjumpered, isolate the battery from the board circuitry for prolonged storage without maintaining channel memory to prevent battery discharge. However, E1 and E2 must be connected prior to operating the receiver to provide the battery backup provision, and to avoid damage to U8.

### 3.4 Parallel Input/Output

The 8155 (U7) provides 22 lines of parallel I/O, one eight-bit output port, another six-bit output port, and the eight-bit input port. The 8255 I/O device (U9) provides another 24 lines, configured as two eight-bit input ports and one, eight-bit output port. Both of these circuits provide a means of monitoring as well as controlling signal lines from both the receiver and front panel sections of the RF-590.

The modules associated with these parallel ports are shown in table 2.

**Table 2. Control Board Port-to-Module Correlation**

Port	Associated Modules
U7 port A:	Rear panel, BFO, PLL III, PLL IV
U7 port B:	IF/Audio, BFO assemblies
U7 port C:	IF filter assembly
U9 port A:	Rear panel and input assemblies
U9 port B:	Reference generator and input assemblies, PLL I, PLL IV, preselector option
U9 port C:	Front panel, PLL II, Meter

Additionally, DIP switch S2 is read by the processor through buffer U21 to determine the filter types used in the particular receiver (see section 4.0).

### 3.5 Serial I/O

Control Board A14 sends most of its control signals out as serial data. The serial data transmission circuit consists of U16, U17, and U18. Dual flip-flop U16 divides the processor output clock by four and clocks U18 and U17, producing the synchronous 750 kHz serial clock signal sent throughout the receiver. Parallel data written to U17 is shifted out onto the serial data line (high order bit first), while U18 counts eight bits transmitted before clearing U16 and ending the serial transmission. The address then written to decoder U14 produces a 1-of-16, high-active strobe to the module which must use the newly transmitted serial data.

### 3.6 Analog I/O

A/D converter (U10) handles analog inputs. Most inputs come from BITE circuits. One input comes from the RF gain potentiometer on the front panel, which in local mode is sampled every 50 milliseconds. The result is sent serially to the D/A converter made up of U11, R28, and the low pass U13 buffer. This two step process is done to enable full control of RF gain through the optional remote control as well as the front panel control. The U13 output should track local rotation of the RF gain potentiometer over the range of 0 to 9 volts. A reference voltage of +5 volts is provided to the A/D and D/A components from regulator VR1. Dual flip-flop U15 divides the CPU 3 MHz clock by four for converter U10, whose end-of-conversion output is output to an input port of U9.

#### 4. BANDWIDTH SELECTION

The RF-590 Receiver can support a variety of IF filters (with several bandwidth and configuration options available). For CW, AM, and sideband modes, several bandwidths may be scrolled through from the front panel depending on customer ordered setup. In order to support the many combinations possible, the selected option is indicated to the microprocessor by switch S2 on Control PWB A14. Thirty-two combinations are presently supported, and the one used is indicated by the setting of the five switch sections S2-4 through S2-8. The last three IF filter board positions are used for filter combinations for AM, CW, or FSK modes and may be empty in a given application. Switch positions S2-1 through S2-3 on the A14 PWB are used to indicate such a condition. When the switch is OPEN, it indicates a filter present and when it is CLOSED, it shows the slot is empty.

Table 3 lists a typical filter complement for the RF-590.

**Table 3. Typical Filter Complement**

Mode	IF Bandwidths
LSB	2.8 kHz
USB	2.8 kHz
CW	0.3 kHz
CW	1.0 kHz
AM	3.2 kHz
AM	6.8 kHz
AM	16.0 kHz
FM	16.0 kHz

This setup uses configuration number 30, and leaves the last IF BW slot empty. The configuration number is expressed as a binary number with OPEN switch sections representing bit = 1. Therefore,

Configuration 30 = 11110 binary (S2-4 through 8)

Final filter slot empty, S2-1 CLOSED

Result:

S2-1	CLOSED
S2-2, S2-3	OPEN
S2-4 through S2-7	OPEN
S2-8	CLOSED

The configuration for a given receiver is factory set, and should not have to be altered by the customer. If S2 is to be replaced, its pattern should be recorded and the replacement set similarly after installation.

## 5. MAINTENANCE

### 5.1 Alignment

Control PWB Assembly A14 requires no adjustment for proper operation.

### 5.2 Troubleshooting

Although most of the circuitry on this assembly is controlled directly or indirectly by the microprocessor, a practice of standard digital troubleshooting methods will isolate most faults to the component level. A logic HIGH is the level between 3 and 5 volts, and a proper logic LOW typically is between 0 and 1 volt. The circuit area involved in minor faults can typically be determined by BITE fault codes, or by using paragraph 3, Functional Description in this section. More general or major failures are best handled by proceeding in order through the checks outlined below.

#### 5.2.1 CPU

If the microprocessor is running, it is capable of debugging several circuits on the A14 PWB by itself. However, it must first be determined if the 8085A is operating.

These inputs must be present in order for the device to run. Table 4 lists the operational inputs for the CPU.

**Table 4. Operational Inputs for CPU**

Pin	Signal
U1-1, 2	Crystal inputs - 6 MHz
U1-36	Reset input - HIGH
U1-6	Trap input - LOW
U1-35	Ready - HIGH
U1-39	Hold - LOW

A14 PWB +5 V supply should be between +4.75 and +5.1 volts. Table 5 lists the CPU outputs that should be present.

**Table 5. Operational Outputs for CPU**

Pin	Signal
U1-37	Clock out - 3 MHz square wave
U1-3	Reset out - LOW
U1-31	Write - active low pulses
U1-32	Read - active low pulses
U1-30	Address latch enable - active high pulses
U1-4	SOD - active low pulses at 1 millisecond intervals

When the CPU is running and executing the application software, its outputs will only be active a portion of each millisecond. The rest of the time it will be halted, waiting for a real time clock interrupt from U7.

#### 5.2.2 Trap and Reset Circuits

The trap circuit is provided to restart the CPU in the software if the device loses synchronization due to high noise levels on its busses. One-shot U20 is retriggered before timeout from U1, pin 4, the SOD output. The software will generate a low active pulse every millisecond if it is executing properly and if it gets the real time clock interrupt. Low voltage on the +5 supply to this board will cause a reset of the processor due to the reset circuit Q2-Q4.

#### 5.2.3 Device Selection

Address decoder U2 aids the access of devices through the data bus by outputting low active chip enable signals corresponding to the address on the high order bits of the CPU. During normal operation, the enables from U2 should be seen on pin 18 of U5, U6, U8, and U19, as well as U7-8. The select on U9-6 should be active immediately following changes in the frequency entered through keyboard or tune knob. Active high selection pulses on A/D converter U10 are visible at least every 50 milliseconds in local receiver operation.

#### 5.2.4 Memory Circuits

It can be very difficult to troubleshoot memory problems if the 8085A is not operating. If the CPU is running, it can find some problems itself. If the BITE routine indicates a PROM checksum fault, the fact that it is running indicates that the data bus buffers are operating and the PROMs are accessed. However, invalid data in these devices would require replacement of PROMs U5, U6, and U19.



If the BITE routine indicates a CMOS RAM fault, check that the enable pulse is getting to RAM U8 and check the voltage on U8-24. FET Q5 is driven by an enable from U2 as a switch to select U8. The chip enable should put Q5's gate at 8.5 Vdc to turn on the switch. The CMOS RAM is not connected directly to the +5 volt supply and E1-E2 must be jumpered to avoid damaging the RAM when the power is turned on.

### 5.2.5 Real Time Clock

As mentioned before, the 1 kHz square wave output from 8155 (U7) is used to interrupt the CPU to synchronize and time many RF-590 processes including the processor reset of the TRAP one-shot circuit U20. If this digital clock is not seen at U1-7, it should be checked at U7-6. The 3 MHz input to U7-3 from U1-37 should also be present. Any improper real time clock operation can be traced to U1, U7, or their interconnection.

### 5.2.6 Serial I/O

Control PWB A14 communicates with the display control board through its serial output circuit (U14, U16, U17, and U18). If this circuit fails the display will light up but will never change from its power up lamp test.

When the control board is operating normally, it will attempt to update the complete display once every second. Every second there will be a burst of 64 bytes to the display control board (two bytes of serial data sent every millisecond for a 32 millisecond total duration). There will be a strobe pulse (following every two bytes) to the display control board from U14-5.

The BITE routine tests the serial output circuit by sending a test pattern to four PLLs and reading back a test bit from each. If it can set (high) and reset (low) all four test bits, it assumes that the serial output circuit on the A14 PWB is operating. If any one test bit cannot be set and reset, it assumes a problem with that PLL.

Signals of interest in the serial data transmission circuit are listed in table 6.

**Table 6. Significant Serial Data Transmission Circuits**

Component	Function
U16-3	Clock in -3 MHz, square wave
U16-1, 13	Serial clock enable - High while data shifting out, 11 microseconds
U15-5, 11	1.5 MHz, square wave
U16-8, 9	750 kHz, square waves, opposite polarity
U17, 18 - 1	Serial port enable, narrow low active pulse
U17-9	Serial data

**Table 6. Significant Serial Data Transmission Circuits (Cont.)**

Component	Function
U16-8	Serial clock
U14-5	Display control board strobe, 30 narrow high active pulses every second

**5.3 Parallel I/O**

Parallel I/O is centralized through the ports on U7 and U9. If there is a BITE or operational problem concerning the modules (listed above) that are controlled by the lines from these parallel circuits, but the module in question is not at fault, port failure may be indicated. Improper operation of front panel scanned keypad, A/D converter output U10-13, or tune knob may be caused by defective U9.

**5.4 Analog I/O**

**5.4.1 Analog Inputs**

If not in remote or test, the control board tries to update the RF gain every 50 milliseconds, using A/D converter U10. Starting the conversion consists of two writes to U10, narrow high-active pulses on U10-16. Ten microseconds later the end of conversion (EOC) line will go low. It will stay low for 100 microseconds and after it goes high again there will be one narrow high active pulse on U10-21. The above is true for all the other analog inputs sampled during the execution of BITE. Signals of interest in the analog input circuit are listed in table 7.

**Table 7. Significant Analog Input Circuits**

Component	Function
U15-3	Clock in -3 MHz, square wave
U15-5, 11	1.5 MHz
U15-9	Clock out - 750 kHz, square wave
U10-22	Clock in - 750 kHz, square wave
U10-16, 32	Start conversion. Two narrow high going pulses, every 50 milliseconds
U10-13	End of conversion. 85 microseconds low, every 50 milliseconds
U10-21	Output enable narrow high going pulse, every 50 milliseconds
U10-15, 18	Multiplexer out, comparator in

### 5.4.2 Analog Outputs

During normal receiver operation, the D/A converter will track the RF gain potentiometer. U11 is a serial in/parallel out shift register. When the A/D finds a changed value for the RF gain, the digital value will be shifted into U11. The resulting bit pattern on the resistor network will cause R28, pin 16, output to track the RF gain potentiometer from 0-5 volts. U13 buffers and filters this voltage and its output will vary from 0-9 volts.

### 5.5 Faults Detected Through BITE

The four fault areas on A14 detectable through BITE are listed in table 8.

**Table 8. Fault Areas on Control Board A14**

Fault	Failure
Fault 01:	PROM failure - The binary checksum calculated from the contents of programmed U5, U6, and U19 do not match value programmed by the factory. Validity of firmware is doubtful, and all three devices should be replaced.
Fault 02:	8155 RAM failure - Errors are found in the ability to store and retrieve data in the 256 byte RAM of U7. Replace U7.
Fault 03:	CMOS RAM failure - Errors are found in the ability to store and retrieve data in U8. Replace U8. Check E1-E2 jumpering, BT1, Q5, and associated circuits.
Fault 04:	Serial data failure - Faulty serial transmission is detected. Check U14 and U16 through U18.

### 6. PARTS LIST

Table 9 is a comprehensive parts list of all replaceable components in Control Board Assembly A14. When ordering parts from the factory, include a full description of the part. Use figure 1, Control Board Assembly A14 Component Location Diagram to identify parts.

### 7. SCHEMATIC DIAGRAM

Figure 2 is the Control Board Assembly A14 schematic diagram.

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**Table 9. Control Board Assembly A14 Parts List (PL 10073-2800)**

Ref. Desig.	Part Number	Description
	10073-2800	PWB, CONTROL BOARD
BT1	B41-0009-004	BAT NICAD 3.6V -20/ + 70C
C1	M39014/01-1535	CAP .01UF 20% 100V CER
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	C26-0010-680	CAP 68UF 20% 10V TANT
C6	C26-0010-680	CAP 68UF 20% 10V TANT
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0010-680	CAP 68UF 20% 10V TANT
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	C26-0050-109	CAP 1.0UF 20% 50V TANT
C13	C26-0016-479	CAP 4.7UF 20% 16V TANT
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	C26-0010-680	CAP 68UF 20% 10V TANT
C20	C26-0050-109	CAP 1.0UF 20% 50V TANT
C21	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	C26-0016-150	CAP 15UF 20% 16V TANT
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	C26-0010-221	CAP 220UF 20% 10V TANT
C31	C26-0010-221	CAP 220UF 20% 10V TANT
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1318	CAP .33UF 10% 50V CER-R
C39	C25-0001-313	CAP 100UF 20% 20V TANT
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C42	C26-0010-221	CAP 220UF 20% 10V TANT
C43	C26-0010-221	CAP 220UF 20% 10V TANT
C44	C26-0016-479	CAP 4.7UF 20% 16V TANT
CR1	1N4454	DIODE 200mA 75V SW
CR2	1N4454	DIODE 200mA 75V SW
CR3	1N4454	DIODE 200mA 75V SW
CR4	1N4454	DIODE 200mA 75V SW

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Table 9. Control Board Assembly A14 Parts List (PL 10073-2800) (Cont.)

Ref. Desig.	Part Number	Description
CR5	1N4454	DIODE 200mA 75V SW
CR6	1N4454	DIODE 200mA 75V SW
E1	SE23XC02	TRM
E2	SE23XC02	TRM
J1	J46-0032-004	HDR 4 PIN 0.100" SR
J2	J46-0013-014	HDR 14 PIN 0.100" DR SHRD
J3	J46-0032-010	HDR 10 PIN 0.100" SR
J4	J46-0032-010	HDR 10 PIN 0.100" SR
J5	J46-0013-014	HDR 14 PIN 0.100" DR SHRD
J6	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J7	J46-0031-010	HDR 10 PIN 0.100" RT ANG
J8	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J9	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J10	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J11	J46-0031-020	HDR 20 PIN 0.100" RT ANG
J12	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J13	J46-0031-016	HDR 16 PIN 0.100" RT ANG
J14	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J15	J46-0013-040	HDR 40 PIN 0.100" DR SHRD
L1	10073-7034	INDUCTOR, 440UH
L2	L-0644	COIL 220UH 10% FXD RF
L3	10073-7034	INDUCTOR, 440UH
L4	MS75085-5	INDUCTOR
L5	10073-7029	INDUCTOR, FILTER CHOKE
L6	10073-7034	INDUCTOR, 440UH
Q1	2N2222	XSTR SS/GP NPN TO-18
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	2N2222	XSTR SS/GP NPN TO-18
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	3N170	XSTR MOSFET
Q8	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R2	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R9	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R10	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R11	R65-0003-122	RES 1.2K 5% 1/4W CAR FILM
R12	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R13	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R14	R65-0003-243	RES 24K 5% 1/4W CAR FILM
R15	R65-0003-204	RES 200K 5% 1/4W CAR FILM
R16	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R17	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R18	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R21	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R22	R65-0003-103	RES 10K 5% 1/4W CAR FILM

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**Table 9. Control Board Assembly A14 Parts List (PL 10073-2800) (Cont.)**

Ref. Desig.	Part Number	Description
R23	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R24	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R26	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R27	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R28	R53-0001-001	RES,DIP NETWORK R/2R
R29	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R30	R65-0003-363	RES 36K 5% 1/4W CAR FILM
R31	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R32	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R33	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R35	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R36	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R37	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R38	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R39	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R40	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R41	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R42	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R43	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R44	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R45	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R46	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R47	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R48	R65-0003-363	RES 36K 5% 1/4W CAR FILM
S1	S06-0002-100	SW PB SPST NO MOM BLK PCT
S2	S50-0001-008	SW SPST 8SEC .1A SLD DIP
U1	I27-0006-002	IC 8085A MICRO 8-BIT CER
U2	I05-0000-042	IC 74LS42 PLASTIC TTL
U3	I05-0000-373	IC 74LS373 PLASTIC TTL
U4	I05-0000-245	IC 74LS245 PLASTIC TTL
U5**	SEE NOTE	IC SOFTWARE PROM
U6**	SEE NOTE	IC SOFTWARE PROM
U7	I26-0003-001	IC 8155-2 STAT RAM 256X8
U8	I26-0010-001	IC STATIC RAM CMOS 2048X8
U9	I59-0008-001	IC 8255 PLASTIC
U10	I40-0010-001	IC ADC0817 PLASTIC CMOS
U11	I01-0000-156	IC 4094B PLASTIC CMOS
U13	I30-0018-000	IC 1458 OP AMP PLASTIC
U14	I01-0000-202	IC 4514B PLASTIC CMOS
U15	I05-0000-074	IC 74LS74 PLASTIC TTL
U16	I05-0000-074	IC 74LS74 PLASTIC TTL
U17	I05-0000-165	IC 74LS165 PLASTIC TTL
U18	I05-0000-165	IC 74LS165 PLASTIC TTL
U19**	SEE NOTE	IC SOFTWARE PROM
U20	I05-0000-122	IC 74LS122 PLASTIC TTL

\*\*NOTE: When ordering U5, U6, or U19, refer to the number located on the PROM label.

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**Table 9. Control Board Assembly A14 Parts List (PL 10073-2800) (Cont.)**

Ref. Desig.	Part Number	Description
U21	I05-0000-244	IC 74LS244 PLASTIC TTL
U22	I05-0000-000	IC 74LS00 PLASTIC TTL
U23	I01-0017-000	IC 7432 PLASTIC TTL
U24	I05-0000-032	IC 74LS32 PLASTIC TTL
U25	I05-0000-004	IC 74LS04 PLASTIC TTL
U27	I05-0000-004	IC 74LS04 PLASTIC TTL
VR1	I11-0008-005	IC VR 340 + 5V 0.1A 2%
XU1	J77-0008-007	SKT IC MACH 40 PIN
XU5	J77-0008-005	SKT IC MACH 24 PIN
XU6	J77-0008-005	SKT IC MACH 24 PIN
XU19	J77-0008-005	SKT IC MACH 24 PIN
Y1	Y15-0004-060	CRYSTAL, 6MHZ.

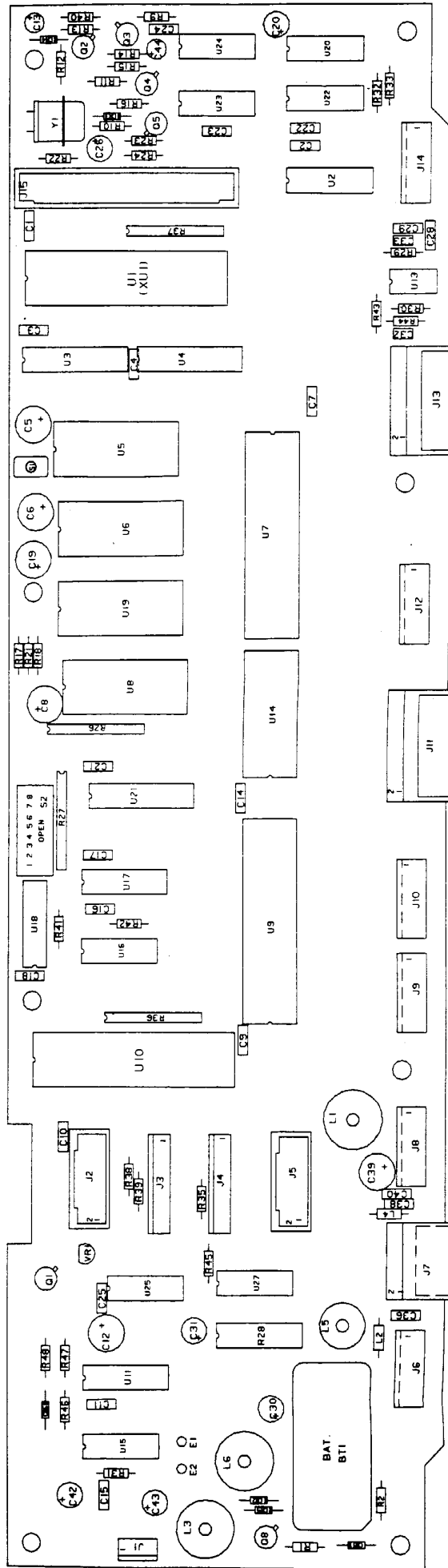
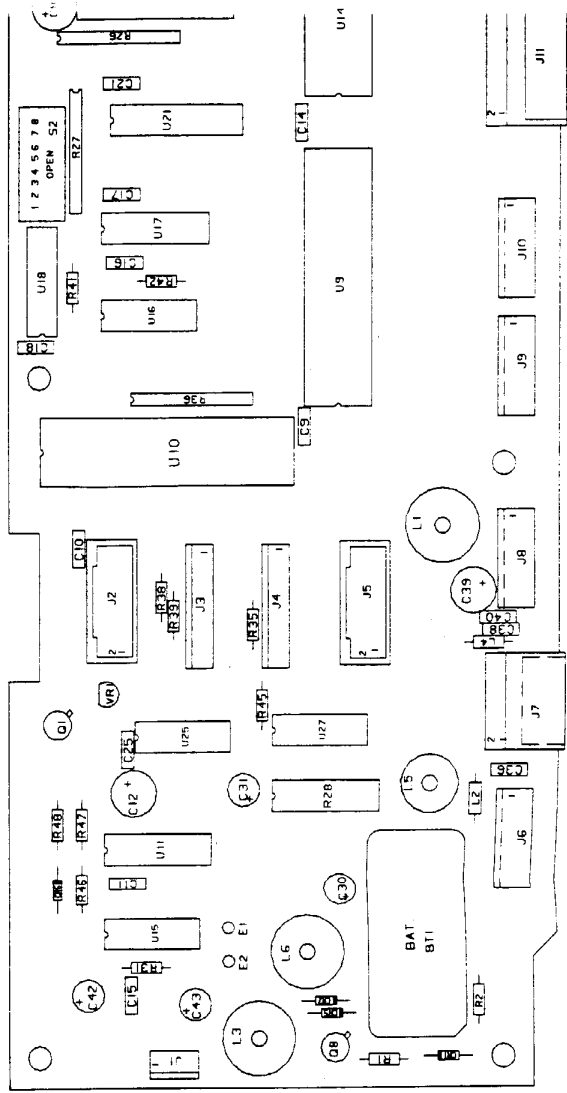


Figure 1. Control Board Assembly A14  
Component Location Diagram  
(10073-2800, Rev. G)





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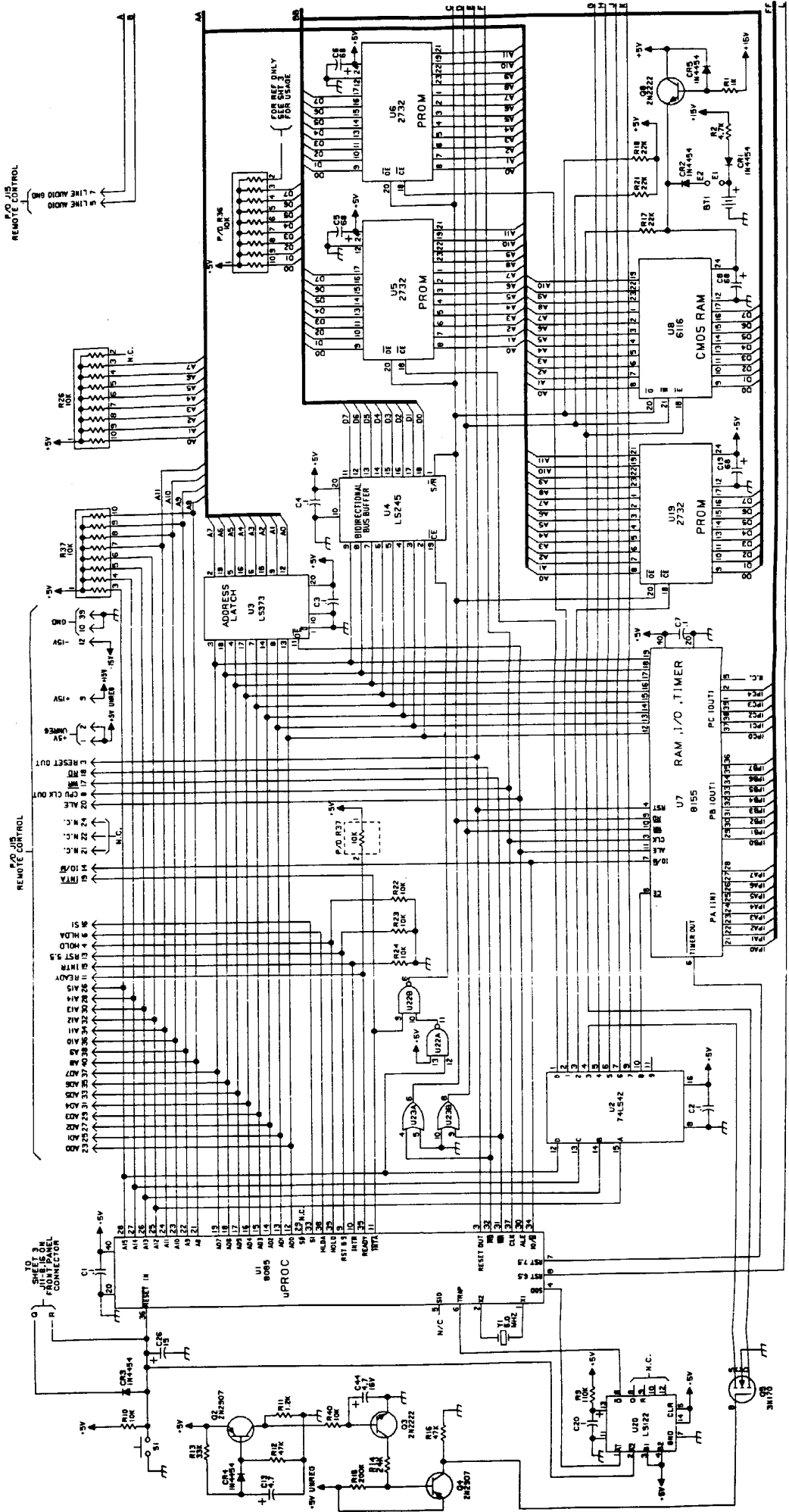


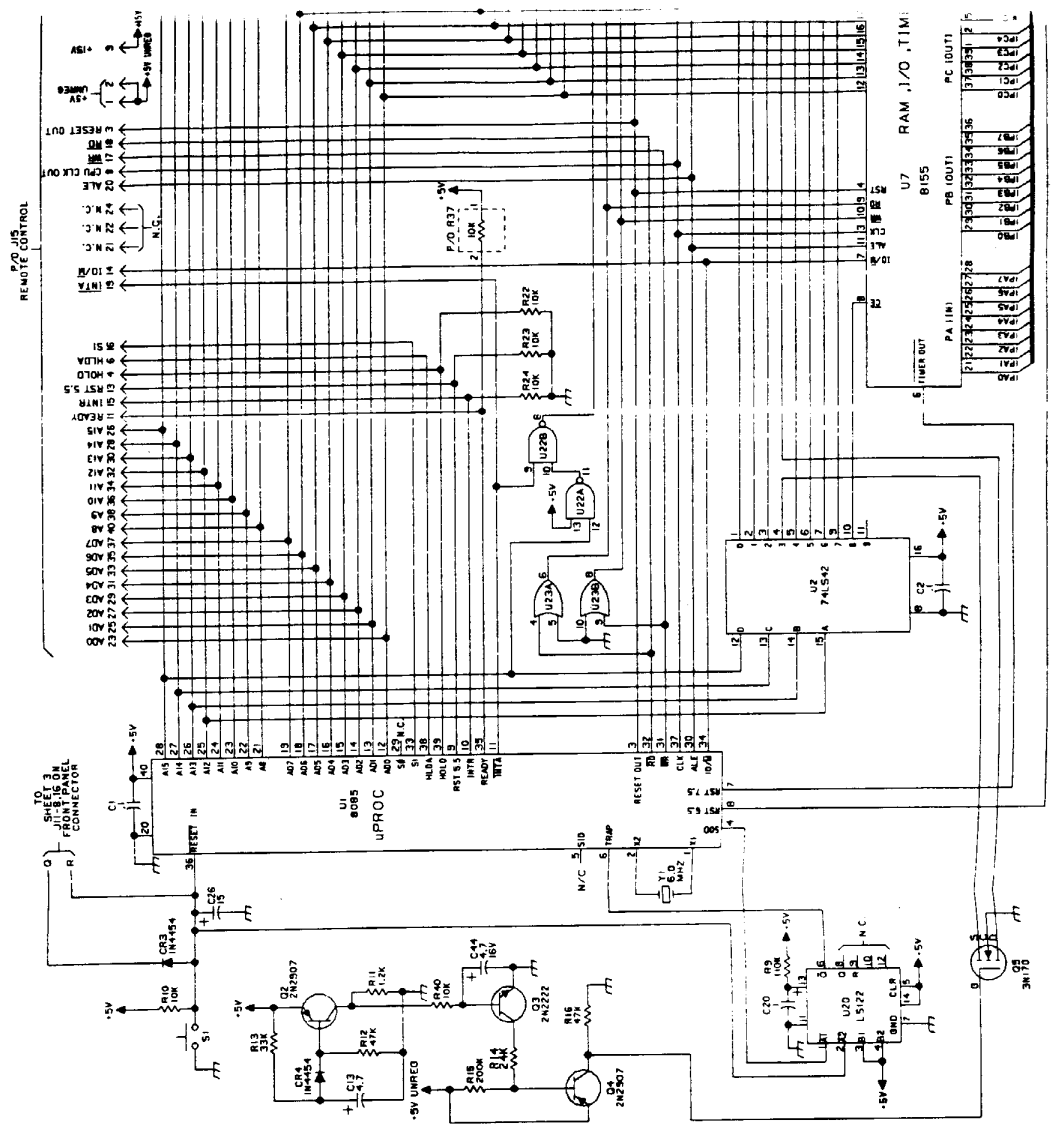
Figure 2. Control Board Assembly A14  
Schematic Diagram (10073-2801, Rev. L)  
(Sheet 1 of 3)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS.
5. COMPONENTS ARE SUPPLIED PER PART NO. IN PART'S LIST.
6. JUMPER E1-E2 MUST BE CONNECTED PRIOR TO USE, BUT REMOVED FOR EXTENDED STORAGE.

- U19 1N58  
 U16 74LS17  
 U25 74LS20  
 U23 74LS00  
 U22 74LS04  
 U27 74LS00

UNUSED GATES



P.O. J15  
 REMOTE CONTROL

RAM I/O (U7)

PA (I/O)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
PC (I/O)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50

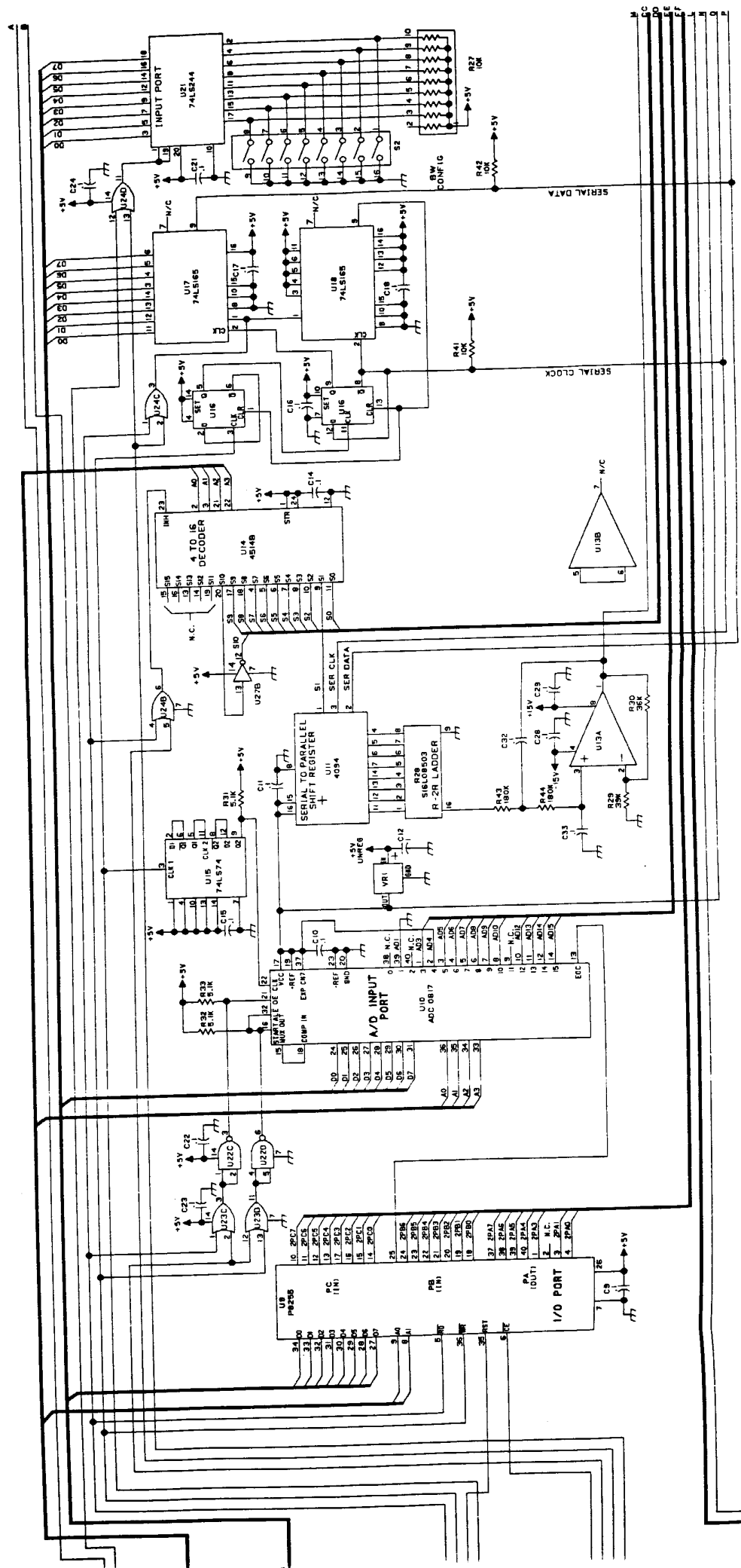
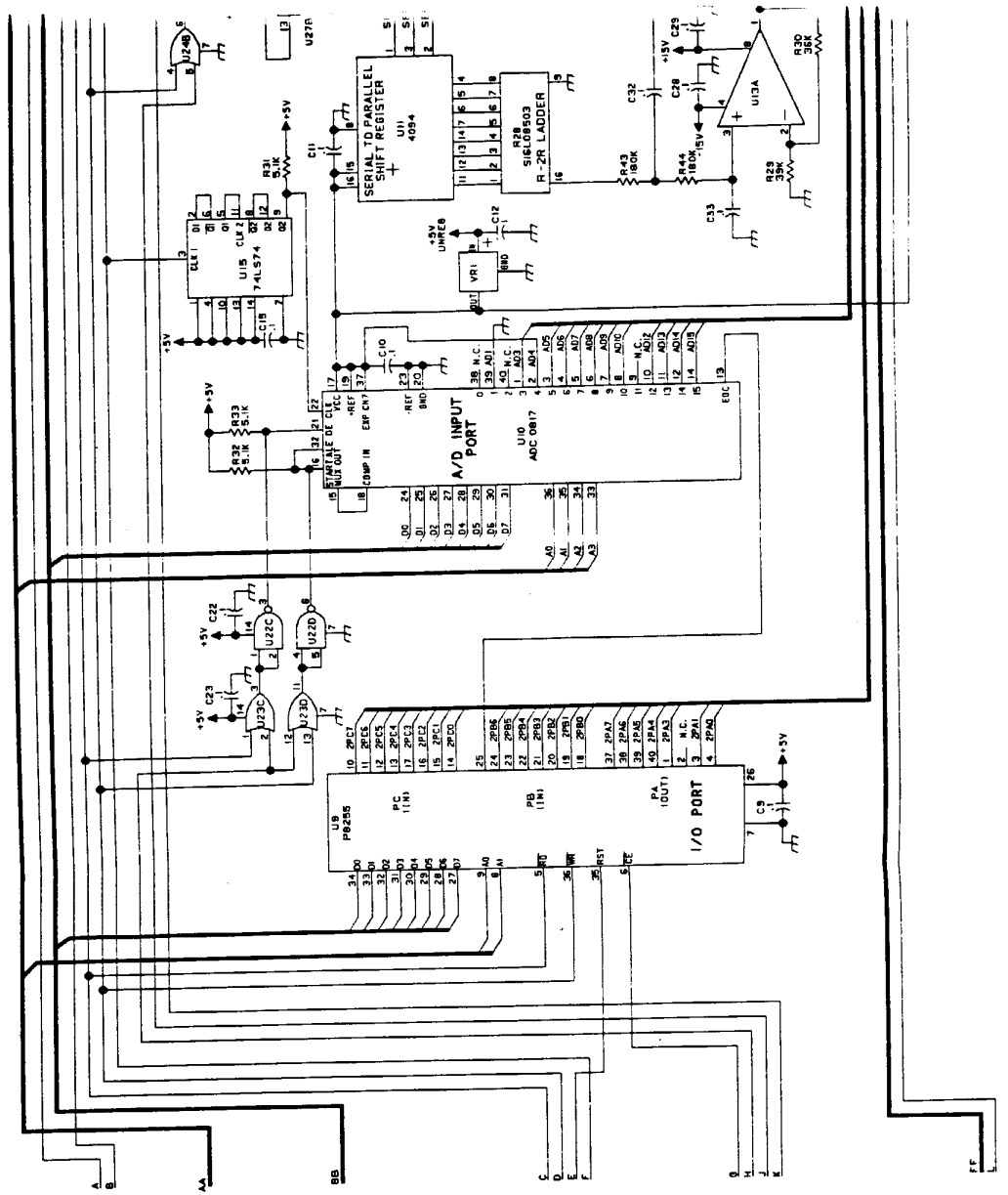


Figure 2. Control Board Assembly A14  
Schematic Diagram (10073-2801, Rev. L)  
(Sheet 2 of 3)



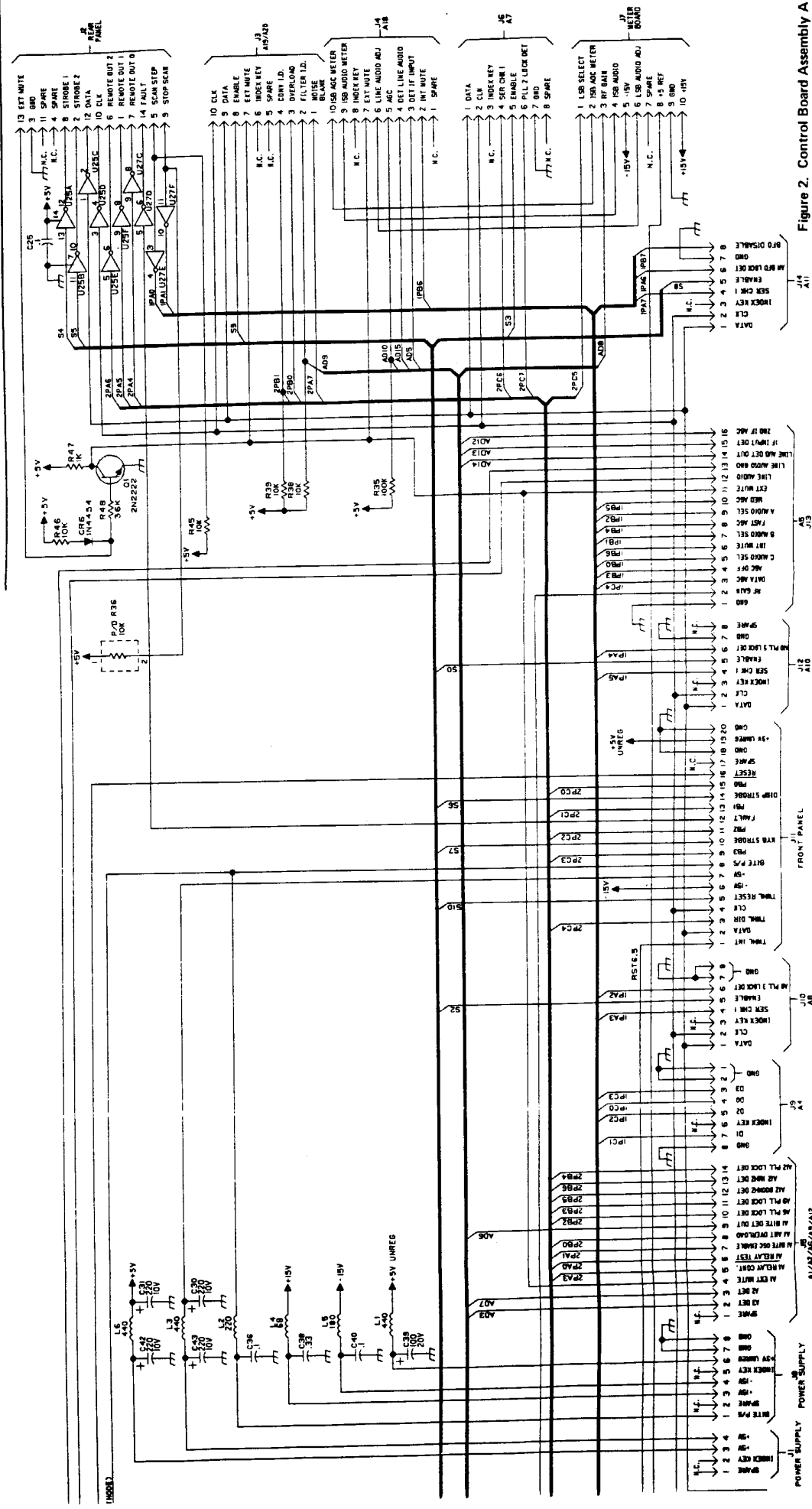
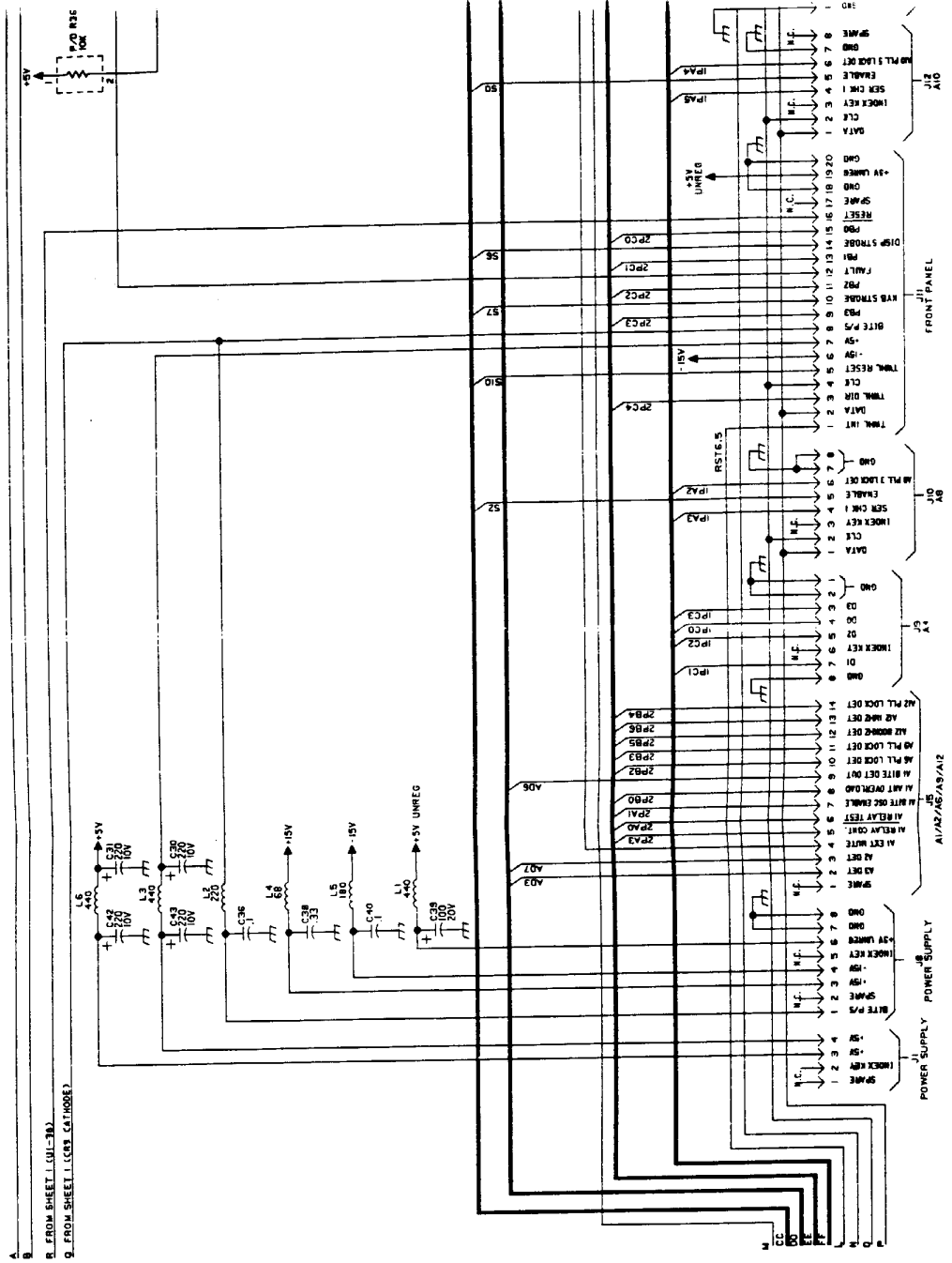


Figure 2. Control Board Assembly A14  
Schematic Diagram (10073-2801, Rev. L)  
(Sheet 3 of 3)



B. FROM SHEET 1 (01-78)

G. FROM SHEET 1 (08-CA-MODE)

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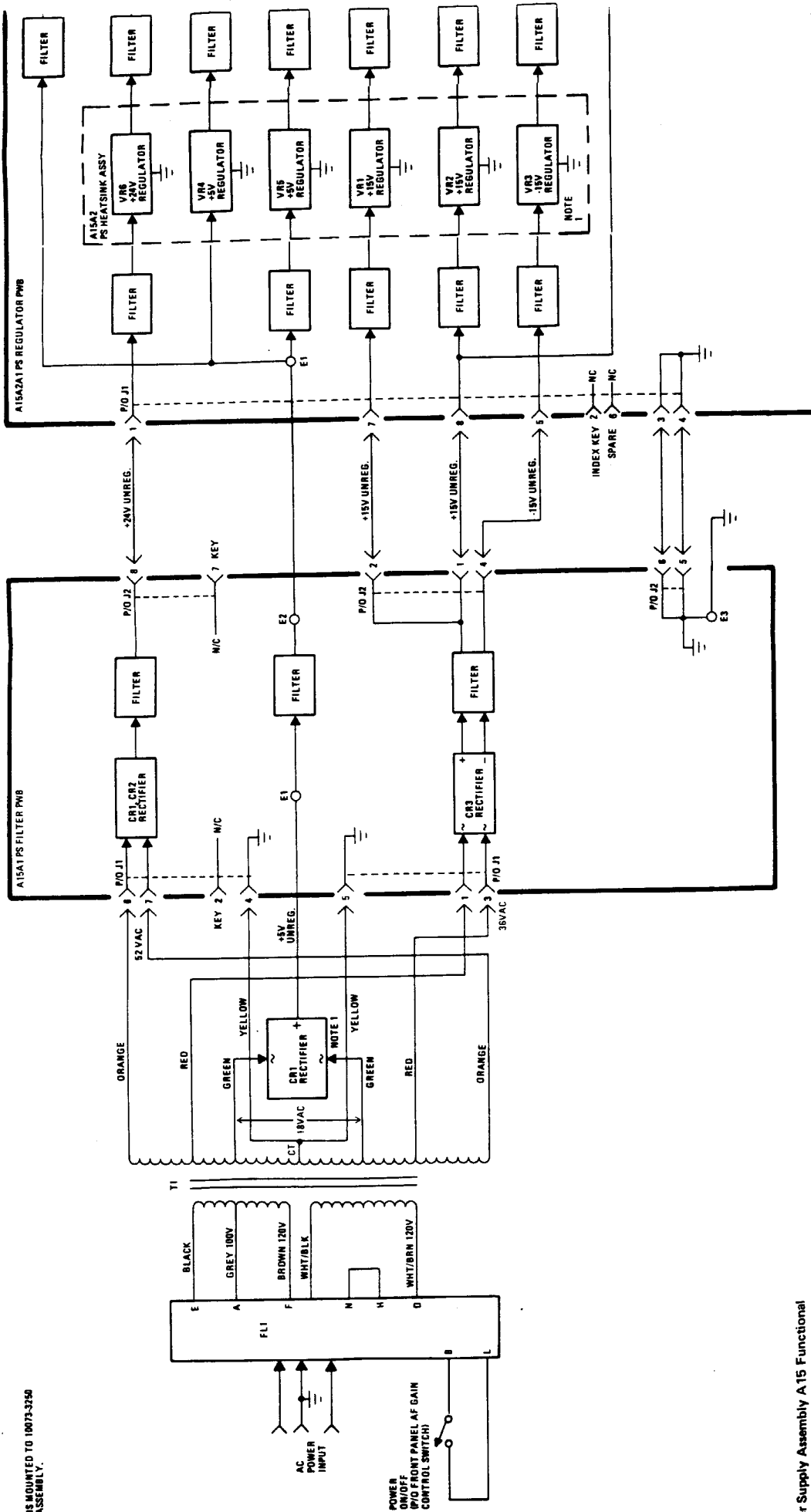
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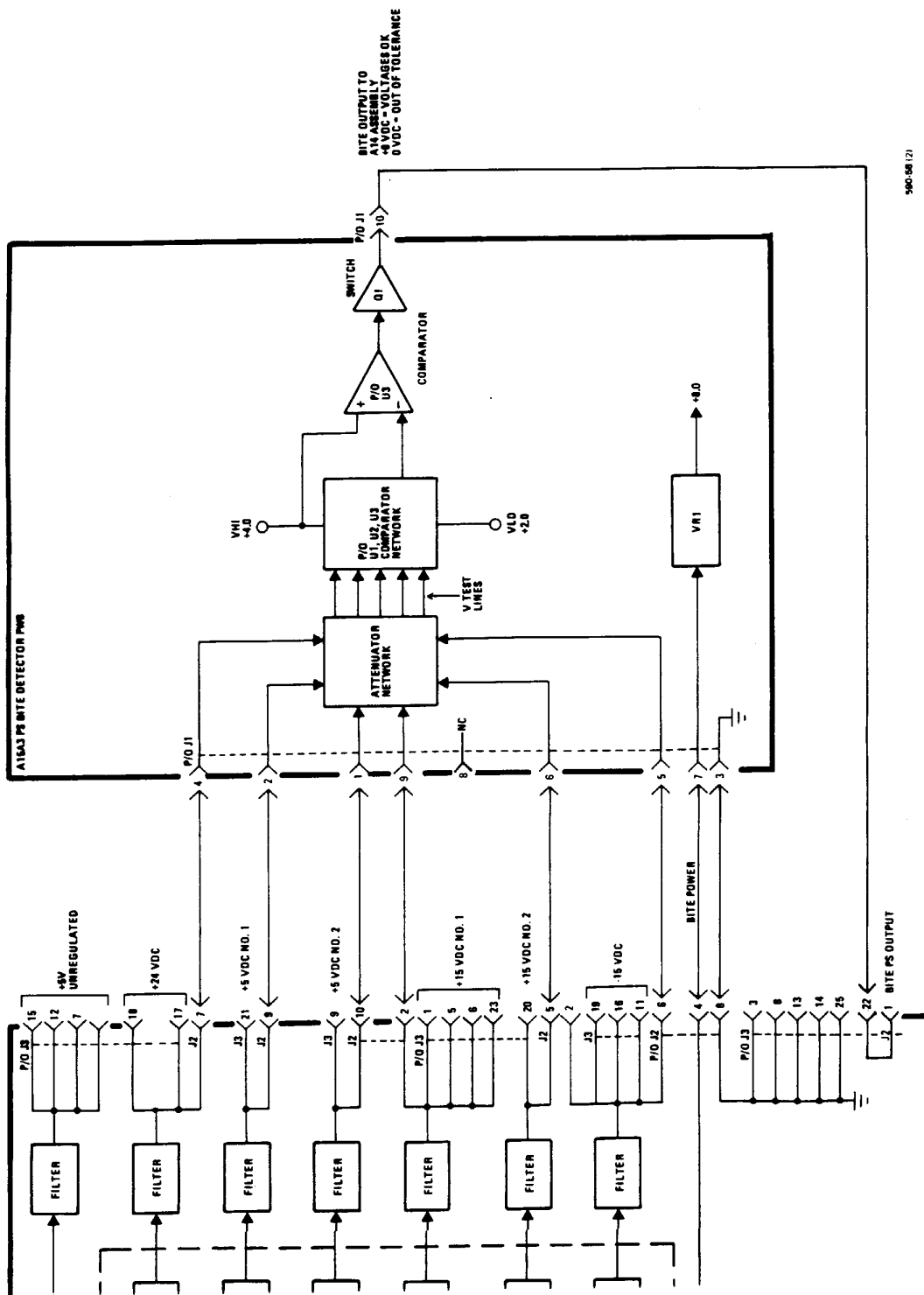
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NOTE:  
1) THESE ITEMS MOUNTED TO 10073-3250  
HEATSINK ASSEMBLY.



Power Supply Assembly A15 Functional Block Diagram



590-68 (2)

1. **A15 POWER SUPPLY ASSEMBLY**

**WARNING**

Potentially hazardous high voltages are present inside the A15 assembly whenever the receiver is connected to an ac line source. Do not attempt any repair to this assembly unless the line cord is disconnected. Do not operate the receiver without the protective cover over the assembly properly installed.

Power Supply Assembly A15 converts either 100, 120, 220, or 240 Vac (47 - 420 Hz) line input voltages into the voltage and current requirements of the RF-590. Input voltage selection is made via the positioning of a plug-in printed circuit card (P/O FL1) located next to the rear panel ac power fuse. The positioning of this card determines the tap selection of power transformer T1. (FL1 also contains the main ac power fuse and ac input power receptacle.)

All power supply components and assemblies are housed in a single metal housing with a perforated cover. This housing (and all the components it contains) may be removed from the RF-590 main frame chassis by removing the six screws at the rear panel and the two screws inside the housing which hold it to the chassis. A single plug-in connector (A15A2A1J3) carries output voltages to the RF-590 power distribution assemblies, and one other connector routes the ac input power to the front panel ON/OFF switch. Both of these must be disconnected in order to remove the housing completely.

EMI protection is provided via line filter FL1, as well as the shielding provided by the power supply housing and cover.

The main components and assemblies contained in Power Supply Assembly A15 are listed below.

- Input Line Filter FL1
- Power Transformer T1
- Filter PWB A15A1
- Heatsink Assembly A15A2 with Regulator PWB A15A2A1
- Power Supply BITE Detector PWB A15A3

FL1 provides both EMI protection and input voltage selection. T1 converts the ac line voltage into the required lower ac voltage levels needed to run the regulators. Filter PWB A15A1 converts the T1 ac outputs into unregulated dc voltage levels. The A15A2 assembly contains the three terminal voltage regulators which convert the unregulated dc levels into regulated dc output voltages. (Note that the voltage regulators VR1-VR6 are mounted to the Heatsink assembly, while the remainder of the necessary circuitry is on Regulator PWB Assembly A15A2A1. It is these A15A2A1 outputs which power the receiver.)

Power Supply BITE PWB A15A3 monitors the output of Regulator PWB A15A2A1 and signals the Control PWB A14 microprocessor if these levels exceed certain prescribed limits. This in turn, would cause a front panel fault light to light. All major components and assemblies in the A15 assembly are interconnected via ribbon cable with plug-in connectors.

The power supply output voltages and maximum design current capabilities provided to power the receiver at A15A2A1J3 are listed in table 1. Note that the current is the maximum allowable current, and that the actual amount drawn from each regulator would vary depending upon the options installed in the radio. (i.e., ISB, remote control, frequency standard, etc.)

**Table 1. A15 Power Supply Outputs**

A15A2A1J3 (Pin)	Voltage (Vdc)	Current (Maximum)
4, 7, 12, 15	+5 Unregulated	2.5 A
2, 17, 18	+24 Regulated	600 mA
21	+5 Regulated no. 1	750 mA
9	+5 Regulated no. 2	750 mA
1, 5, 6, 23	+15 Regulated no. 1	1.0 A
20	+15 Regulated no. 2	1.0 A
11, 16, 19	-15 Regulated	500 mA

## 2. A15 ASSEMBLY CIRCUIT DESCRIPTION

The RF-590 may be operated using either 100, 120, 220, or 240 Vac, 47 - 420 Hz as a primary source voltage. This voltage feeds through a standard three prong connector on the RF-590 rear panel (part of EMI Filter Assembly FL1). Input voltage selection is via a plug-in printed circuit board which is part of FL1 and accessible from the rear panel. FL1 also contains fuse F1 (replaceable from the rear panel) and initial line filtering. The receiver power switch is part of the front panel AF Gain control and is connected in series with one side of the ac line.

FL1 feeds power transformer T1 (mounted to the A15 assembly). T1 supplies 52 Vac and 36 Vac to Power Supply Filter PWB A15A1, and 18.5 Vac to rectifier CR1 mounted on the Heatsink assembly. CR1 in turn feeds an unregulated +5 volts to A15A1.

Table 2 is the A15 assembly parts list. Figures 1 and 2 show overall component location and schematic diagrams.

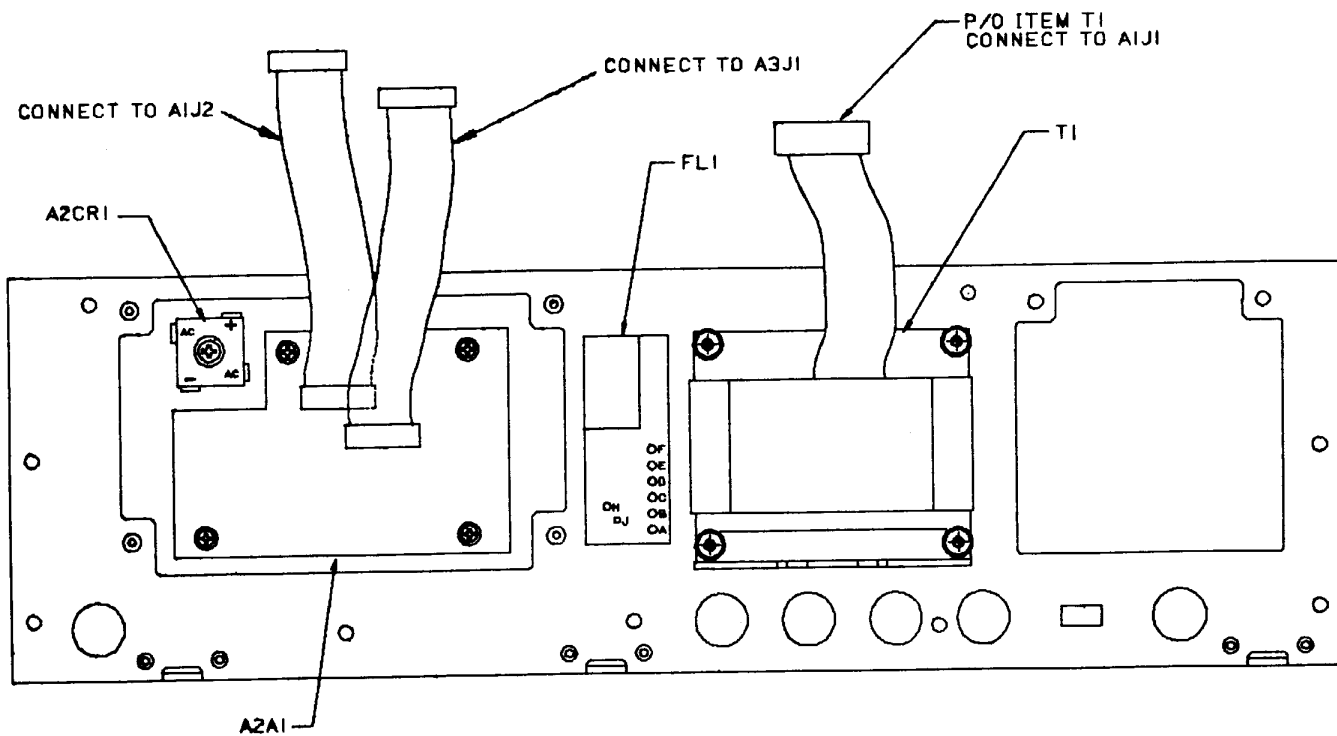
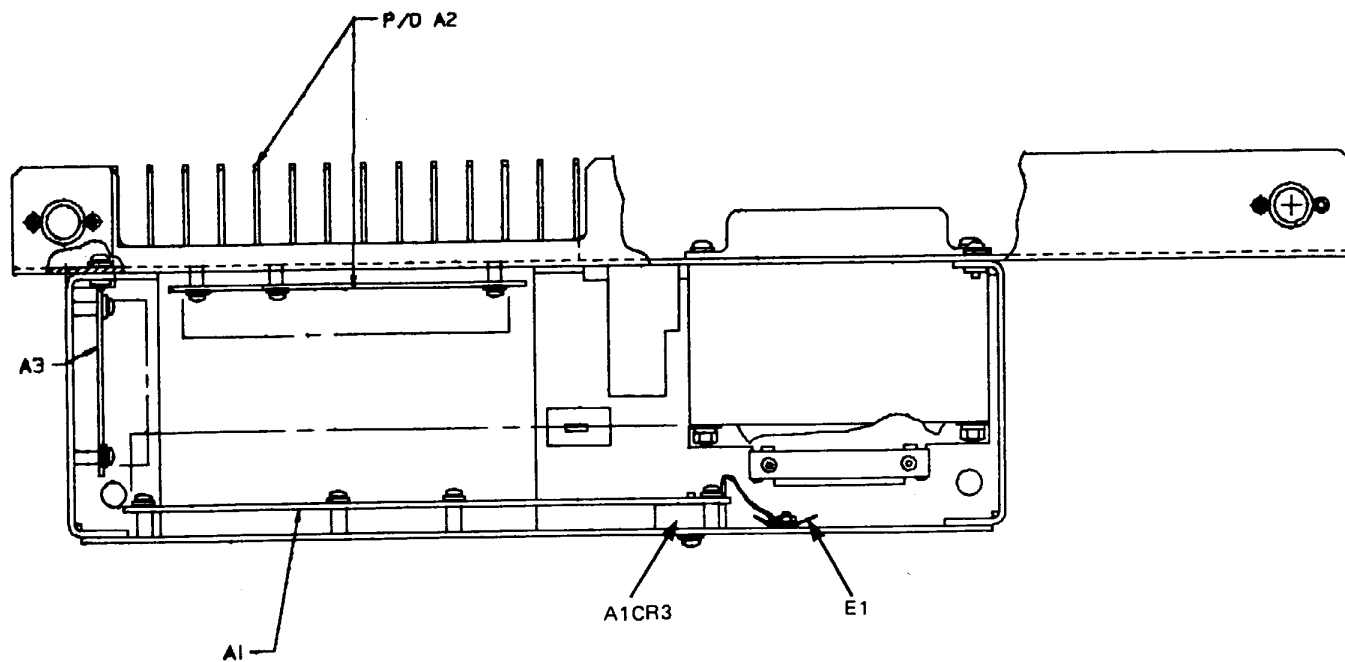


Figure 1. Power Supply Assembly A15 Component Location Diagram (10073-3000, Rev. G)

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NOTE: UNLESS OTHERWISE SPECIFIED:  
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR A COMPLETE DESIGNATION, PRESENTATION,  
UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

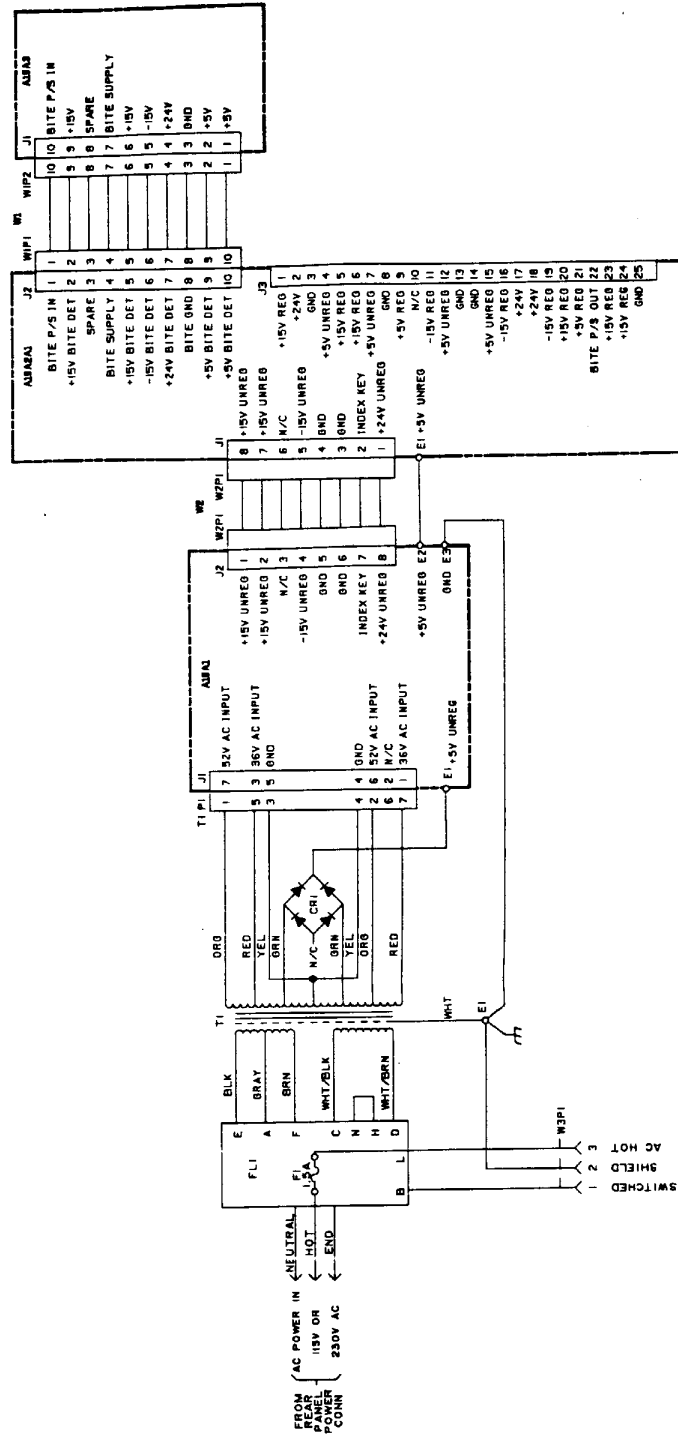


Figure 2. Power Supply Assembly A15 Schematic Diagram (10073-3001, Rev. E)

**Table 2. Power Supply Rear Panel Assembly A15 Parts List (PL 10073-3000)**

Ref. Desig.	Part Number	Description
A1	10073-3000	REAR PANEL ASSEMBLY
A2	10073-3006	CHASSIS, POWER SUPPLY
A3	10073-3100	PWB ASSY, FILTER
E1	10073-3250	HEATSINK ASSY
F1	10073-3300	PWB ASSY, BITE
FL1	MS77068-1	LUG SOLDER #4
T1	F03-0002-022	FUSE 1-1/2A QA
W1	6919-1400	LINE FILTER
W2	10073-3052	TRANSFORMER, POWER
W3	10073-7060	RIBBON CABLE, 10 COND
	10073-7059	RIBBON CABLE, 8 COND
	10073-7250	CABLE ASSY, 3 COND

### 2.1 A15A1 Power Supply Filter Assembly

The A15A1 assembly contains voltage rectifiers and the large filter capacitors required to filter the input voltages from T1. The 52 Vac at J1-6 and J1-7 is full-wave rectified by CR1 and CR2 and filtered by C1 to produce an unregulated +24 volts at J2-8.

The 36 Vac at J1-1 and J1-3 is full-wave rectified by CR3 and filtered by C2 and C3 to produce an unregulated +15 volts at J2-1 and J2-2 and -15 volts unregulated at J2-4. The 5 volts unregulated at E1 is heavily filtered by filter network C4-L1-C5 and made available at E2.

Table 3 is the A15A1 assembly parts list. Figures 3 and 4 are the A15A1 component location and schematic diagrams.

**Table 3. Power Supply Filter Board Assembly A15A1 Parts List (PL 10073-3100)**

Ref. Desig.	Part Number	Description
C1	10073-3100	PWB, FILTER
C2	C17-0050-282	CAP 2800UF 50V ELEC
C3	C17-0035-562	CAP 5600UF 35V ELEC
C15	C17-0035-212	CAP 2100UF 35V ELEC
C19	C17-0035-123	CAP 12000UF 35V ELEC
CR1	C17-0035-123	CAP 12000UF 35V ELEC
CR2	D22-0006-001	DIODE 3A 600V RECT GP
CR3	D22-0006-001	DIODE 3A 600V RECT GP
E3	D22-5011-200	DIODE 10A 200V RECT BR
J1	MP-0372	FAST-ON .125 PCB MOUNT
J2	J42-0004-007	CONN ,7 PIN
L1	J46-0032-008	HDR 8 PIN 0.100" SR
	10073-3051	INDUCTOR, 1MH 4 AMP

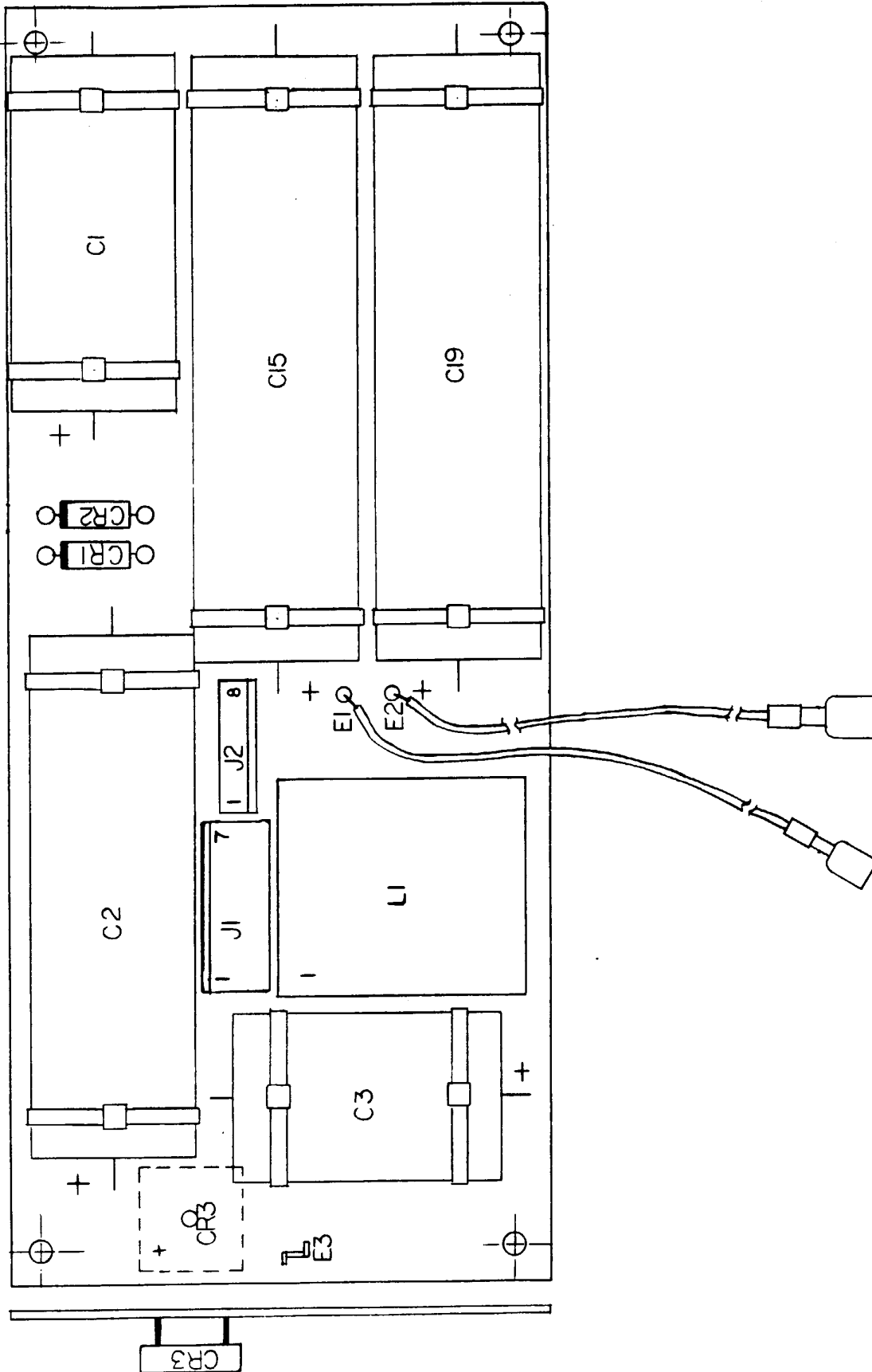


Figure 3. Power Supply Filter Board Assembly A15A1 Component Location Diagram (10073-3100, Rev. D)





## 2.2 Power Supply Regulator Assembly A15A2

Heatsink Assembly A15A2 consists of voltage regulators VR1-VR6, CR1, and Regulator PWB A15A2A1. They are all mounted to a large heatsink bolted to the rear of the A15 assembly. Heatsink Assembly A15A2 may be removed from Power Supply Assembly A15 by removing the five mounting screws on the rear of the A15 assembly.

Regulator PWB A15A2A1 receives the unregulated output voltages from A15A1, and uses linear regulators mounted to Heatsink Assembly A15A2 to produce the regulated output voltages required. Table 4 lists the input voltages, the associated voltage regulator, and the output voltages.

**Table 4. A15A2 Voltage Regulator Identification**

Input Voltage	A15A2 Voltage Regulator	Output Voltage
+15 Unregulated	VR1	15 Vdc no. 1
+15 Unregulated	VR2	15 Vdc no. 2
-15 Unregulated	VR3	-15 Vdc
+5 Unregulated	VR4	+5 Vdc no. 1
+5 Unregulated	VR5	+5 Vdc no. 2
+24 Unregulated	VR6	+24 Vdc

All these voltages are routed through connector A15A2A1J3 (located on the bottom of the A15A2A1 PWB) for power distribution throughout the radio.

Additionally, the A15A2A1 assembly provides additional filtering to these voltages, as well as to a +5 volt unregulated output which does not receive any regulation. (This output is used where local regulation to +5 Vdc will be accomplished on a particular assembly.)

Table 5 is the A15A2 assembly parts list and figure 5 is the A15A2 assembly component location drawing. Table 6 is the A15A2A1 parts list and figure 6 is the A15A2A1 assembly component location drawing. Figure 7 is the A15A2 assembly and A15A2A1 assembly schematic diagram.

**Table 5. Power Supply Heatsink Assembly A15A2 Parts List (PL 10073-3250)**

Ref. Desig.	Part Number	Description
A1	X-0814	INSULATOR, TRANSISTOR
CR1	10073-3200	PWB ASSY, REGULATOR
VR1, VR2	D22-5004-001	DIODE 15A 200V RECT BR
VR3	I11-0001-006	IC VR 7815 +15V 1.5A 4%
VR4, VR5	I12-0002-005	IC VR 7915C -15V 1.5A 4%
VR6	I11-0001-001	IC VR 7805 +5V 1.5A 4%
	IC-0358	IC VR 317 ADJ V 1.5A

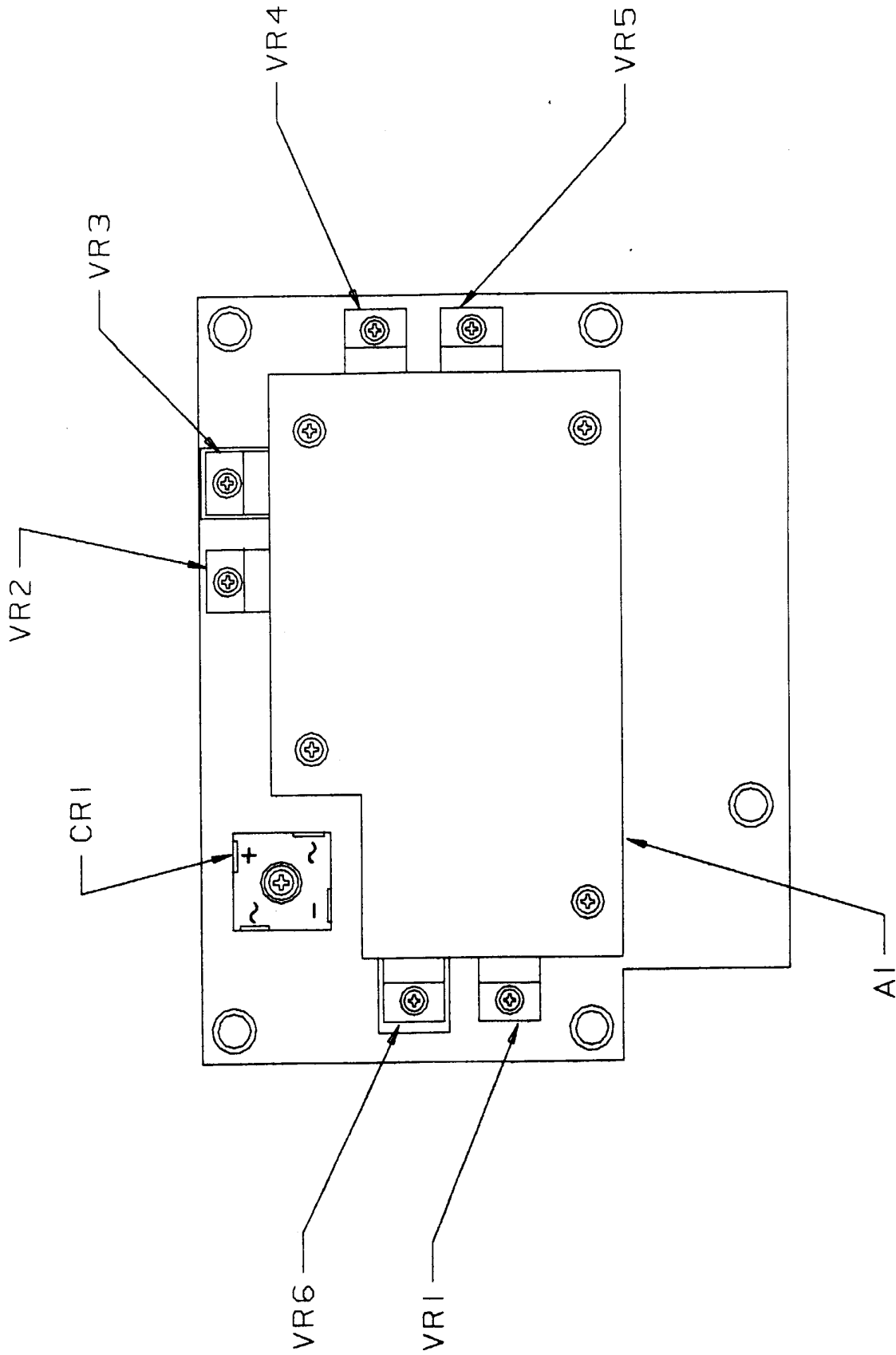
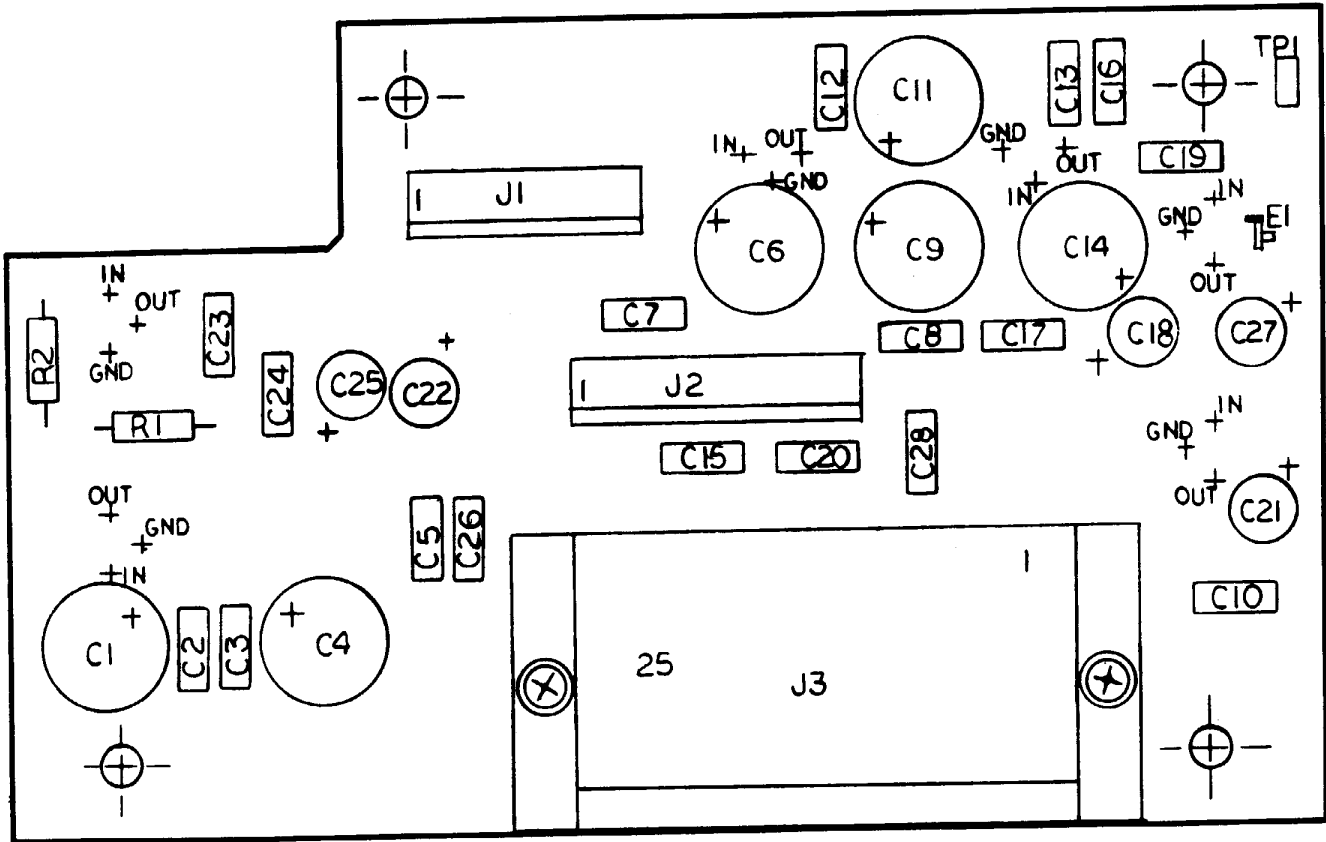


Figure 5. Power Supply Heatsink Assembly A15A2 Component Location Diagram (10073-3250, Rev. C)

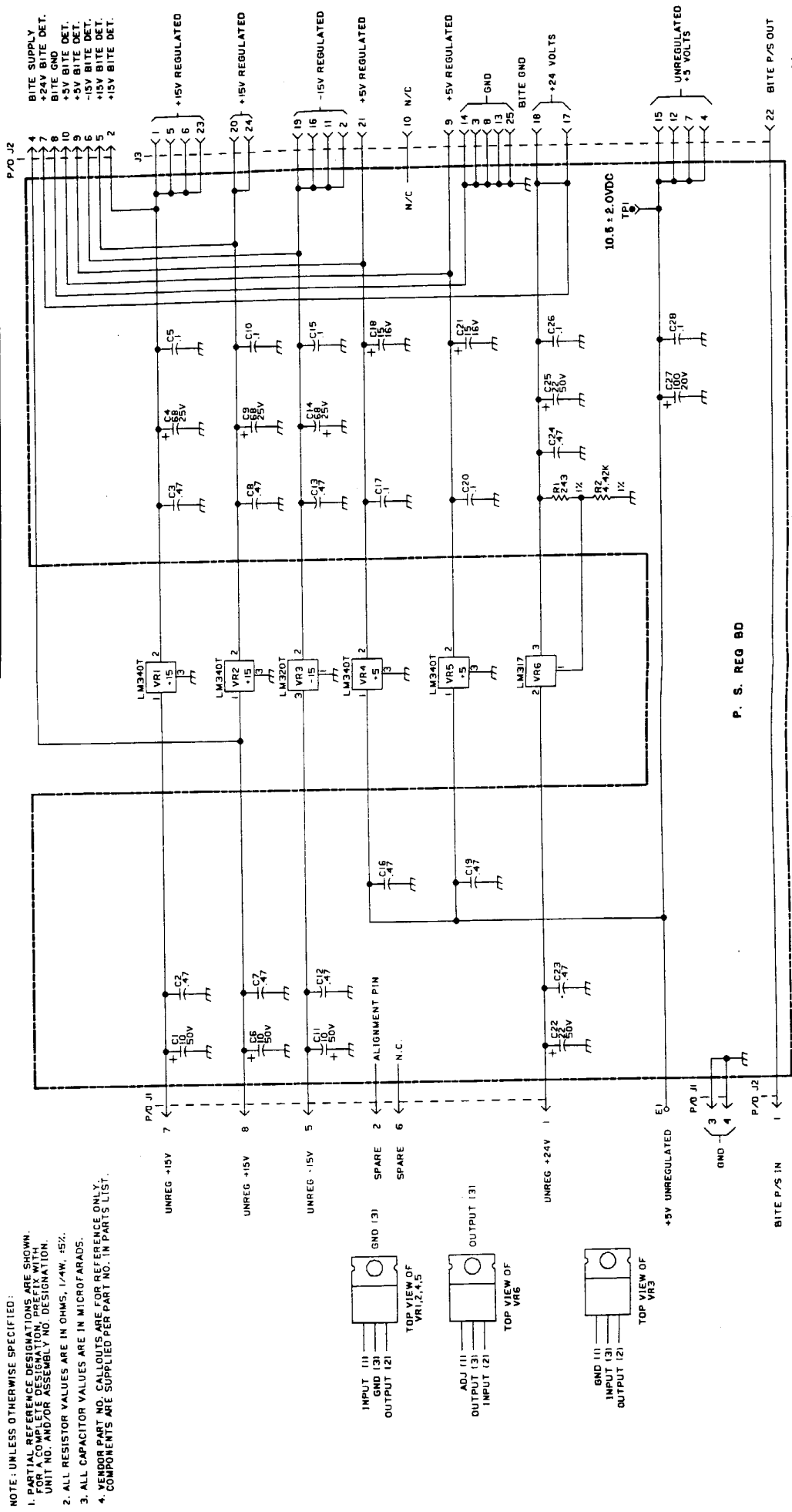
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**Table 6. Power Supply Regulator Board Assembly A15A2A1 Parts List (PL 10073-3200)**

Ref. Desig.	Part Number	Description
	10073-3200	PWB, REGULATOR
C1	C26-0050-100	CAP 10UF 20% 50V TANT
C2	M39014/02-1320	CAP .47UF 10% 50V CER-R
C3	M39014/02-1320	CAP .47UF 10% 50V CER-R
C4	C26-0025-680	CAP 68UF 20% 25V TANT
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	C26-0050-100	CAP 10UF 20% 50V TANT
C7	M39014/02-1320	CAP .47UF 10% 50V CER-R
C8	M39014/02-1320	CAP .47UF 10% 50V CER-R
C9	C26-0025-680	CAP 68UF 20% 25V TANT
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	C26-0050-100	CAP 10UF 20% 50V TANT
C12	M39014/02-1320	CAP .47UF 10% 50V CER-R
C13	M39014/02-1320	CAP .47UF 10% 50V CER-R
C14	C26-0025-680	CAP 68UF 20% 25V TANT
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1320	CAP .47UF 10% 50V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	C26-0016-150	CAP 15UF 20% 16V TANT
C19	M39014/02-1320	CAP .47UF 10% 50V CER-R
C20	M39014/02-1310	CAP .1UF 10% 100V CER-R
C21	C26-0016-150	CAP 15UF 20% 16V TANT
C22	C25-0003-015	CAP 22UF 10% 50V TANT
C23	M39014/02-1320	CAP .47UF 10% 50V CER-R
C24	M39014/02-1320	CAP .47UF 10% 50V CER-R
C25	C25-0003-015	CAP 22UF 10% 50V TANT
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	C25-0003-313	CAP 100UF 10% 20V TANT
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
E1	MP-0372	FAST-ON .125 PCB MOUNT
J1	J46-0032-008	HDR 8 PIN 0.100" SR
J2	J46-0032-010	HDR 10 PIN 0.100" SR
J3	J20-0009-025	CONN-D F 25 FXD RT A
R1	RN55D2430F	RES,243.0 1% 1/8W MET FLM
R2	RN55D4421F	RES,4420 1% 1/8W MET FLM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS



**Figure 6. Power Supply Regulator Board Assembly A15A2A1 Component Location Diagram  
(10073-3200, Rev. C)**



NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

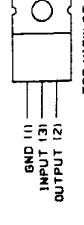
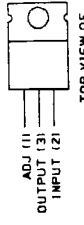
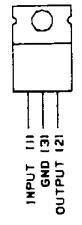


Figure 7. Power Supply Heatsink Assembly  
A15A2 and Power Supply Regulator  
Assembly A15A2A1 Schematic  
Diagram (10073-3201, Rev. E)

### 2.3 Power Supply BITE Detector Assembly A15A3

The A15A3 assembly monitors all the regulated output voltages listed in table 4 and will issue a fault signal to Control Board Assembly A14 if any of them exceed a defined upper or lower limit. The A14 assembly will then issue a fault command and turn on the RF-590 fault indicator on the front panel. This operation is performed continually while the receiver is operating.

The general operation scheme of the assembly is as follows, using the +5 Vdc from A15A2 at A15A3 J1-9 as an example.

The +5 Vdc at pin 2 is divided by resistor network R13-R14 to place nominally 3.1 Vdc at U2D-10 (-) and U2C-9 (+). (This level shall be referred to as  $V_{TEST}$ .) The +8 Vdc from VR1 is divided by R1 and R3 to place +4 Vdc at U2D-11 (+) and by R2 and R4 to place +2 Vdc at U2C-8 (-). (The +4 Vdc level shall be referred to as  $V_{HI}$ ; the +2 Vdc level as  $V_{LO}$ ). These two levels establish the "window" that  $V_{TEST}$  must not exceed.

Under conditions where  $V_{LO} < V_{TEST} < V_{HI}$ , U2C and U2D outputs are at +8 volts. This feeds to U3C-8 (-). Since U3C-9 (+) input is always held fixed at 4 Vdc ( $V_{HI}$ ), U3C output will be low (0 Vdc), Q1 will be biased off, and the BITE output signal will be at +8 Vdc. This notifies the BITE circuits that the +5 Vdc level is within its limits.

Assume that  $V_{TEST}$  exceeds  $V_{HI}$ . U2D output would switch 0 Vdc, causing U3C to switch to +8 Vdc, turning on Q1. Q1 output would drag the BITE output to 0 Vdc, and notify the BITE circuits of an error condition. The same events would occur if  $V_{TEST}$  fell below  $V_{LO}$ , except that now U2C output would affect the switching of U3C.

This concept of a comparator pair providing the lower and upper window limits is used to monitor the other regulated input voltages. Since all the comparator outputs are tied together, any one of them changing states would cause Q1 to issue an error signal.

Note that there are five comparator pairs, but six input voltages. The -15 Vdc input is used as a reference (instead of ground) for the two +15 Vdc and one +24 Vdc inputs, thereby eliminating the need for a separate comparator pair to monitor the -15 Vdc.

The approximate range of upper and lower input limits which will not trip the comparators is given in table 7.

**Table 7. A15A3 BITE Detector Trip Limits**

Input Voltage Vdc	Permissible Voltage Range
+5 Vdc no. 1	≈ 3.0 to 6.5
+5 Vdc no. 2	≈ 3.0 to 6.5

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**Table 7. A15A3 BITE Detector Trip Limits (Cont.)**

Input Voltage Vdc	Permissible Voltage Range
+15 Vdc no. 1	≈ 13.0 to 17.0
+15 Vdc no. 2	≈ 13.0 to 17.0
-15 Vdc	≈ -13.0 to -17.0
+24 Vdc	≈ 21 to 26

Table 8 is the A15A3 assembly parts list. Figures 8 and 9 are the A15A3 assembly component location and schematic diagrams.

**Table 8. Power Supply BITE Board A15A3 Parts List (PL 10073-3300)**

Ref. Desig.	Part Number	Description
	10073-3300	PWB, BITE
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	C26-0025-100	CAP 10UF 20% 25V TANT
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
J1	J46-0032-010	HDR 10 PIN 0.100" SR
Q1	2N2222	XSTR SS/GP NPN TO-18
R1	RN55D4021F	RES,4020 1% 1/8W MET FLM
R2	RN55D7501F	RES,7500 1% 1/8W MET FLM
R3	RN55D4021F	RES,4020 1% 1/8W MET FLM
R4	RN55D2491F	RES,2490 1% 1/8W MET FLM
R5	RN55D1212F	RES,12.1K 1% 1/8W MET FLM
R6	RN55D1822F	RES,18.2K 1% 1/8W MET FLM
R7	RN55D1212F	RES,12.1K 1% 1/8W MET FLM
R8	RN55D1822F	RES,18.2K 1% 1/8W MET FLM
R9	RN55D1822F	RES,18.2K 1% 1/8W MET FLM
R10	RN55D2102F	RES,21.0K 1% 1/8W MET FLM
R11	RN55D1821F	RES,1820 1% 1/8W MET FLM
R12	RN55D3011F	RES,3010 1% 1/8W MET FLM
R13	RN55D1821F	RES,1820 1% 1/8W MET FLM
R14	RN55D3011F	RES,3010 1% 1/8W MET FLM
R15	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R16	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R19	R65-0003-103	RES 10K 5% 1/4W CAR FILM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS
TP2	J-0387	TP PWB RED RA SIDE ACCESS



**Table 8. Power Supply BITE Board A15A3 Parts List (PL 10073-3300) (Cont.)**

Ref. Desig.	Part Number	Description
TP3	J-0390	TP PWB ORN RA SIDE ACCESS
TP4	J-0391	TP PWB YEL RA SIDE ACCESS
TP5	J-0389	TP PWB GRN RA SIDE ACCESS
TP6	J-0393	TP PWB BLU RA SIDE ACCESS
U1	I20-0006-000	IC LM339 COMPARATOR PL
U2	I20-0006-000	IC LM339 COMPARATOR PL
U3	I20-0006-000	IC LM339 COMPARATOR PL
VR1	I12-0006-008	IC VR 78L08A + 8V .10A 4%

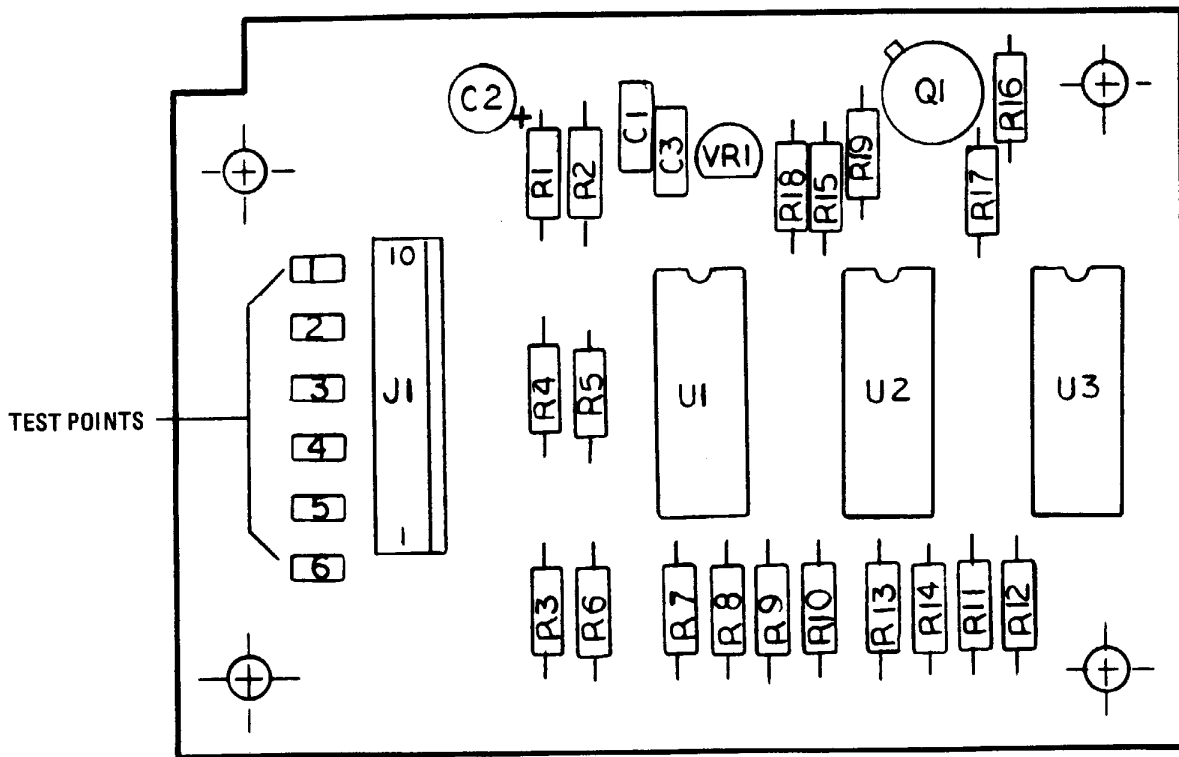


Figure 8. Power Supply BITE Board A15A3 Component Location Diagram (10073-3300, Rev. B)

- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE REFERENCE DESIGNATION, SEE THE PART NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL CAPACITOR VALUES ARE IN OHMS, 1/4W, 5%. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
  4. VENDOR PART NO. CALL OUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
  5. SEE GRAPHICS BELOW.

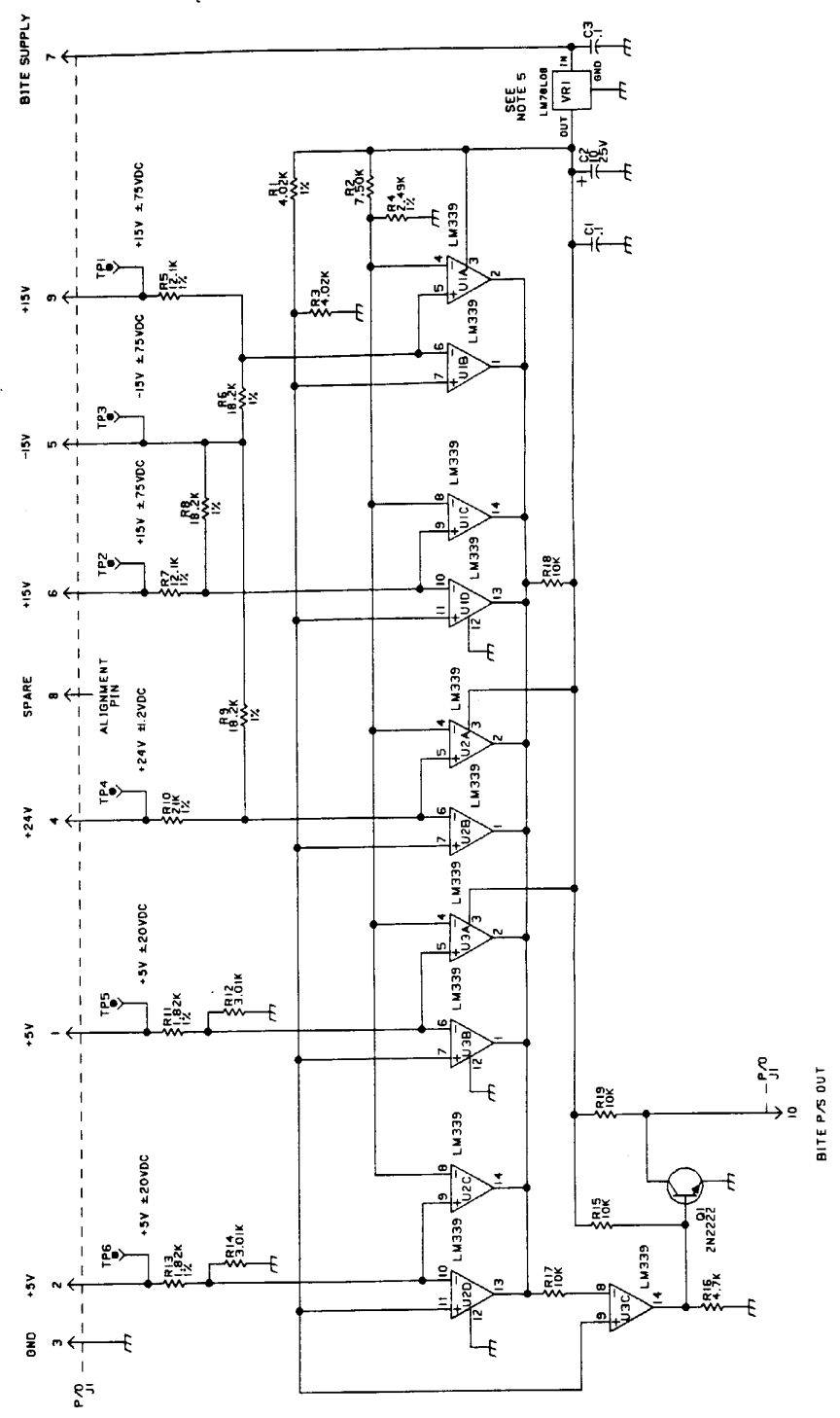
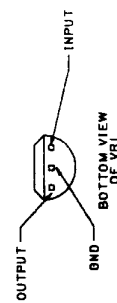


Figure 9. Power Supply BITE PWB A15A3  
Schematic Diagram (10073-3301,  
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## 1. MAIN CHASSIS

The RF-590 chassis is a rigid one piece sand casting. The main frame includes siderails, assembly mounting holes, and compartments used to mount and house most printed wiring board assemblies.

### 1.1 Top Side of Main Chassis

The top side of the chassis is shown in figure 1 and contains compartments that house the following assemblies.

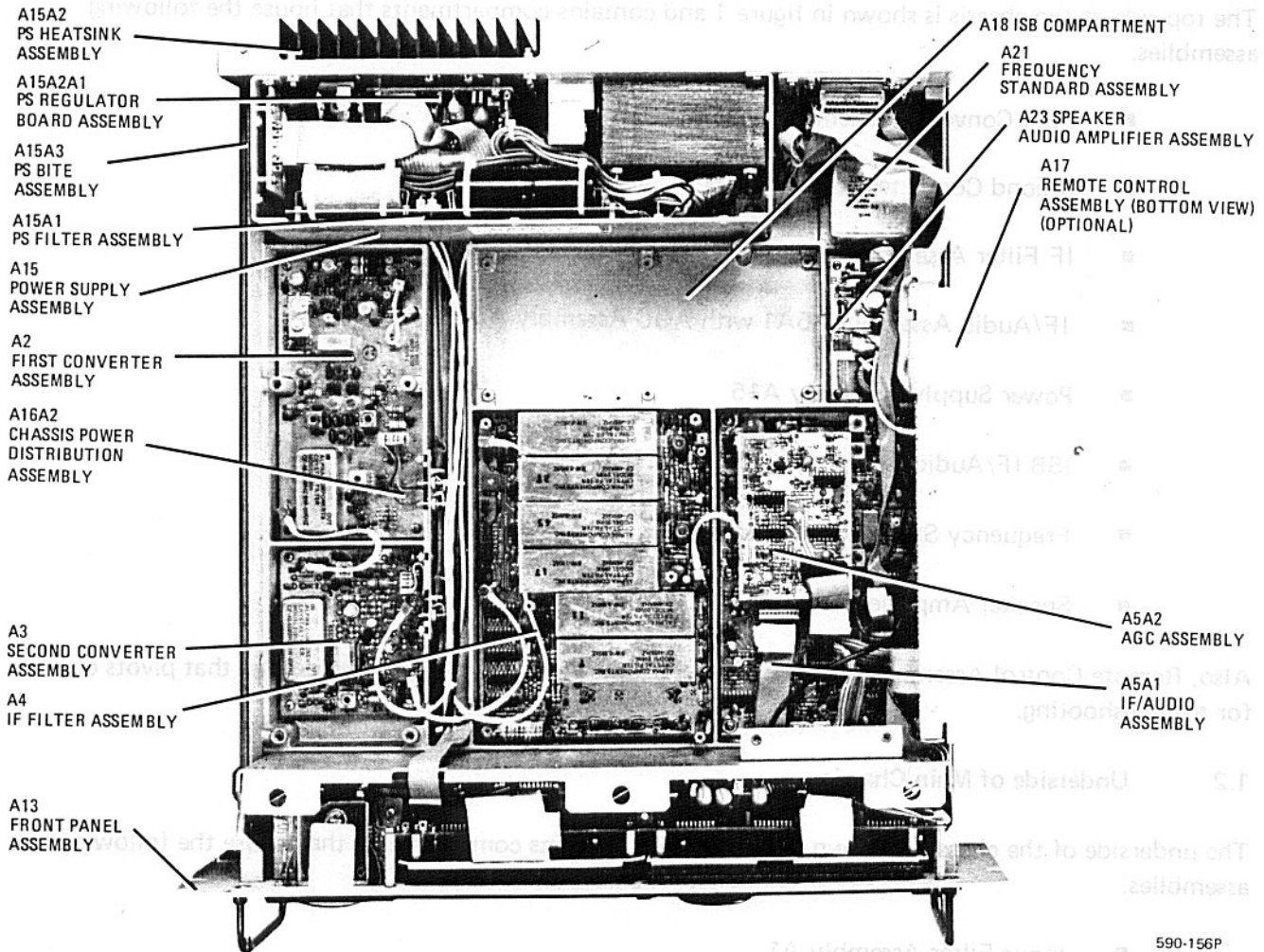
- First Converter Assembly A2
- Second Converter Assembly A3
- IF Filter Assembly A4
- IF/Audio Assembly A5A1 with AGC Assembly A5A2
- Power Supply Assembly A15
- ISB IF/Audio Assembly A18
- Frequency Standard Assembly A21
- Speaker Amplifier Assembly A23

Also, Remote Control Assembly A17 sets over IF/Audio Assembly A5 in a hinged pan that pivots out for troubleshooting.

### 1.2 Underside of Main Chassis

The underside of the chassis is shown in figure 2 and contains compartments that house the following assemblies.

- Input Filter Assembly A1
- PLL I Assembly A6
- PLL II Assembly A7
- PLL III Assembly A8
- PLL IV Assembly A9



**Figure 1. RF-590 Top View Without Covers**

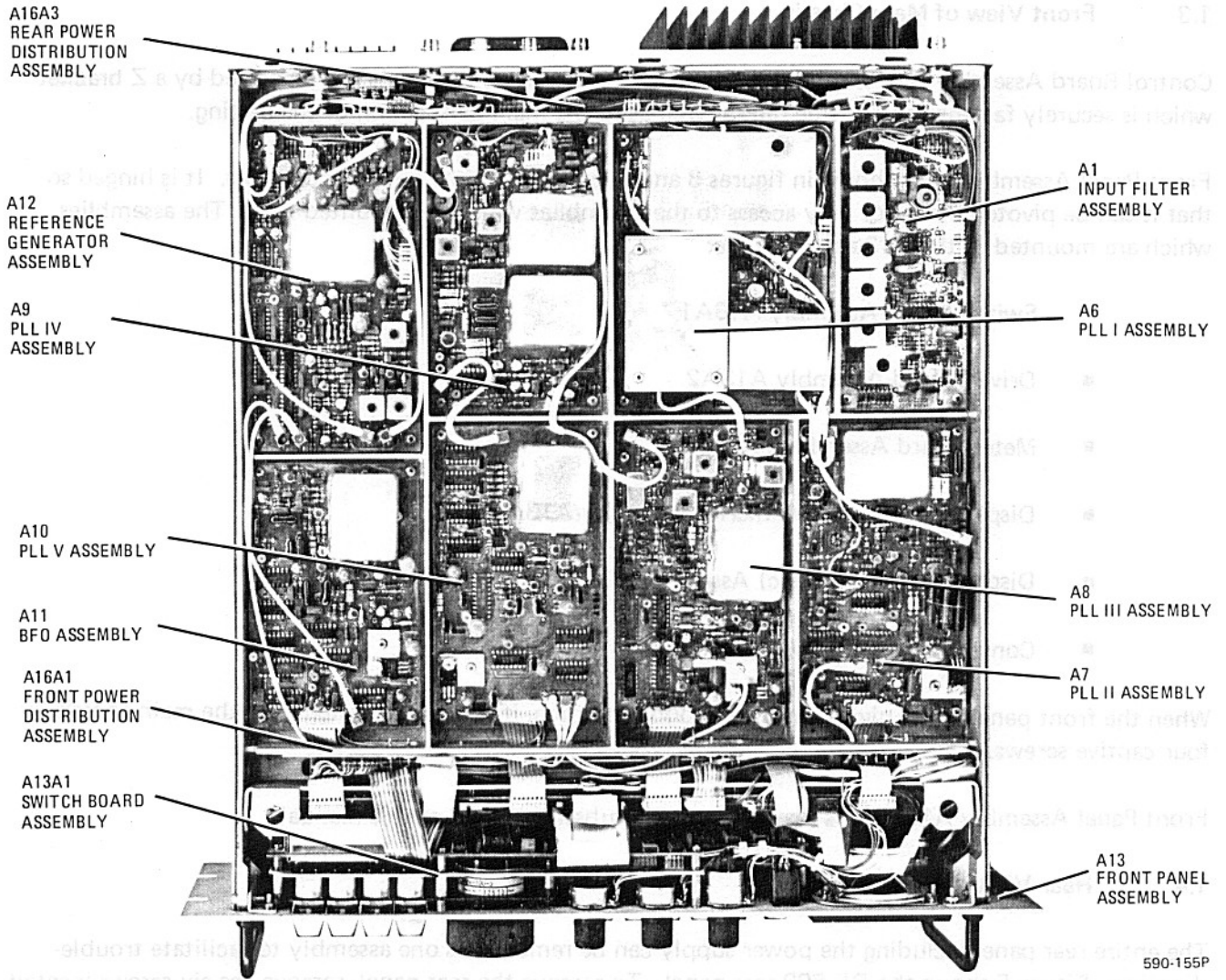


Figure 2. RF-590 Bottom View Without Covers

- PLL V Assembly A10
- BFO Assembly A11
- Reference Generator Assembly A12

### **1.3 Front View of Main Chassis**

Control Board Assembly A14 is mounted on the forward section of the chassis separated by a Z bracket which is securely fastened to the side rails as well as to the main pan section of the casting.

Front Panel Assembly A13, shown in figures 3 and 4, contains all the operator controls. It is hinged so that it can be pivoted down for easy access to the assemblies which are mounted to it. The assemblies which are mounted to the A13 assembly are:

- Switch Board Assembly A13A1
- Driver Board Assembly A13A2
- Meter Board Assembly A13A3
- Display Board (alphanumeric) Assembly A13A4
- Display Board (numeric) Assembly A13A5
- Converter Assembly A13A6

When the front panel is not pivoted out for troubleshooting, it is securely fastened to the main chassis by four captive screws.

Front Panel Assembly A13 details may be found in subsection A13 of this manual.

### **1.4 Rear View of Main Chassis**

The entire rear panel including the power supply can be removed as one assembly to facilitate troubleshooting. Figure 5 shows the RF-590 rear panel. To remove the rear panel, remove the six screws located on the panel and the two screws inside Power Supply Assembly A15. Disconnect the two connectors on the underside of the chassis.

Power Supply Assembly A15 contains the following assemblies housed in a wrap around chassis design.

- A15A1 Power Supply Filter Board
- A15A2 Power Supply Regulator Heatsink Assembly, with Regulator Board A15A2A1





590-205P

Figure 3. RF-590 Front View

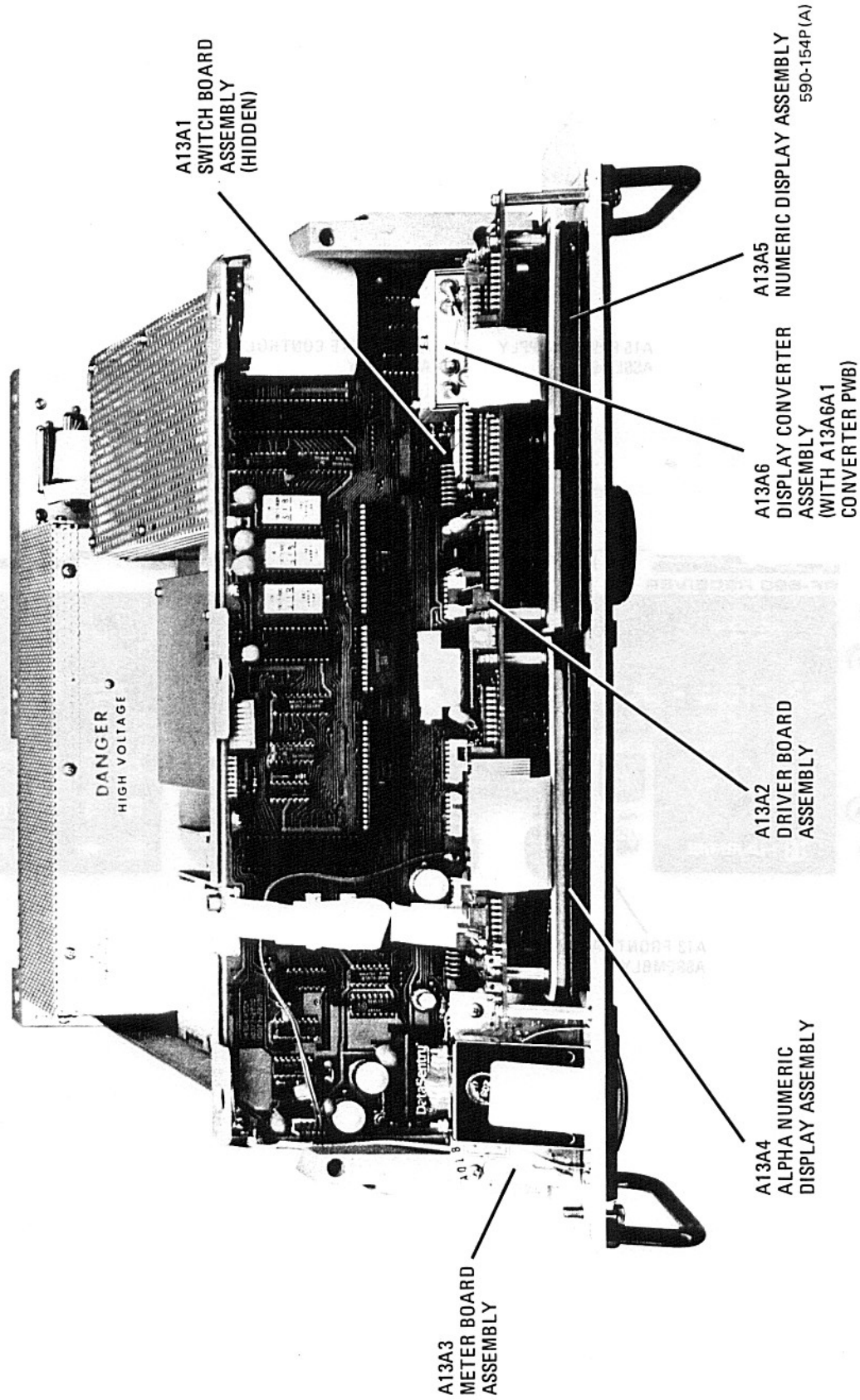


Figure 4. RF-590 Front View With Panel Down

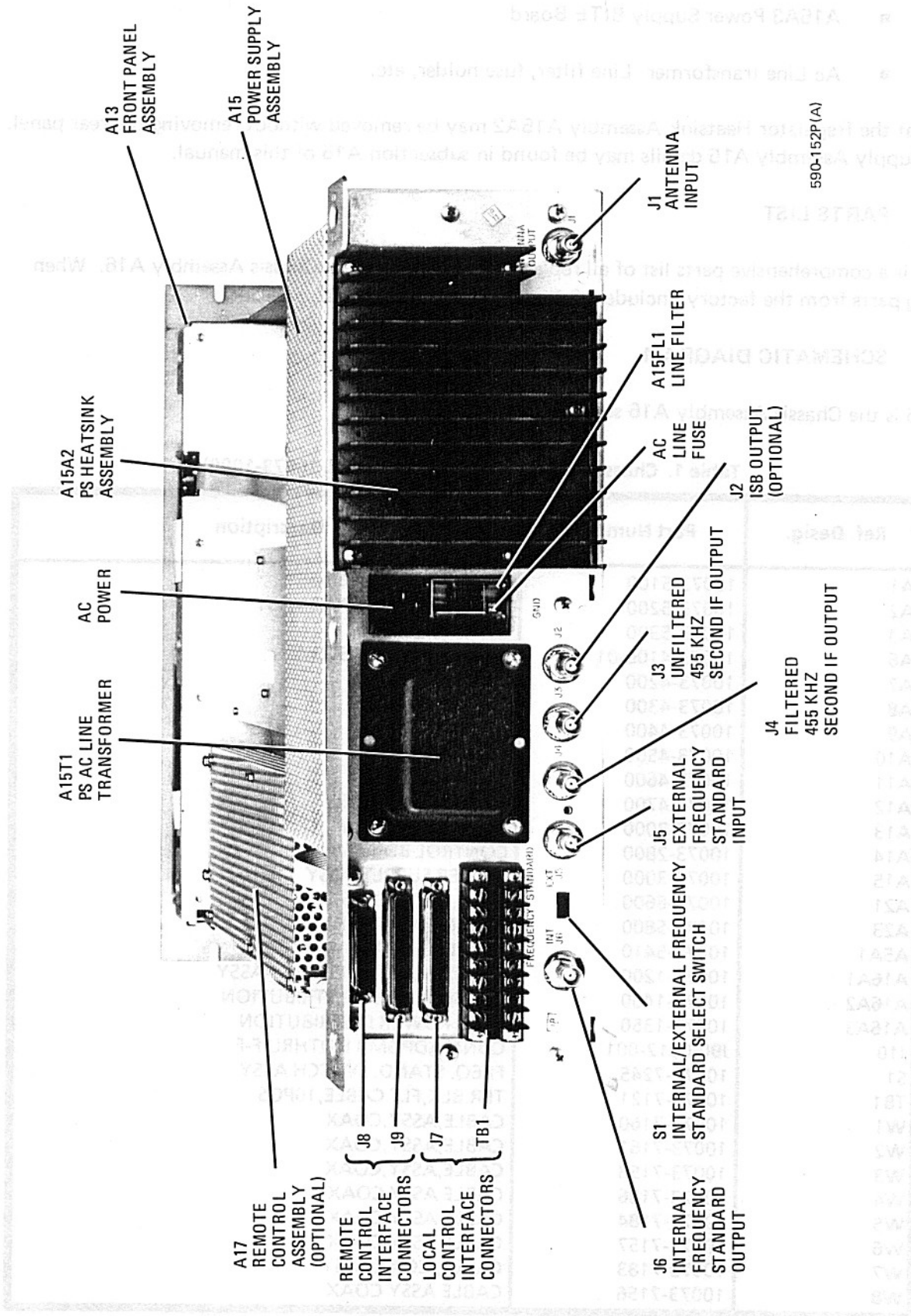


Figure 5. RF-590 Rear Panel

- A15A3 Power Supply BITE Board
- Ac Line transformer, Line filter, fuse holder, etc.

Note that the Regulator Heatsink Assembly A15A2 may be removed without removing the rear panel. Power Supply Assembly A15 details may be found in subsection A15 of this manual.

## 2. PARTS LIST

Table 1 is a comprehensive parts list of all replaceable components in Chassis Assembly A16. When ordering parts from the factory, include a full description of the part.

## 3. SCHEMATIC DIAGRAM

Figure 6 is the Chassis Assembly A16 schematic diagram.

**Table 1. Chassis Assembly A16 Parts List (PL 10073-1000)**

Ref. Desig.	Part Number	Description
A1	10073-5100	INPUT FILTER PWB ASSY
A2	10073-5200	1ST CONVERTER PWB ASSY
A3	10073-5300	2ND CONVERTER
A6	10073-4100-01	PWB ASSY, PLL 1 SLOW
A7	10073-4200	PWB ASSY, PLL 2
A8	10073-4300	PWB ASSY, PLL 3
A9	10073-4400	PWB ASSY, PLL 4
A10	10073-4500	PWB ASSY, PLL 5
A11	10073-4600	BFO PWB ASSY
A12	10073-4700	REF-GEN PWB ASSY
A13	10073-2000	PANEL ASSEMBLY
A14	10073-2800	CONTROL BD ASSY
A15	10073-3000	POWER SUPPLY ASSY
A21	10073-6600	FREQ. STD 1X10 6
A23	10073-5800	AUDIO AMPLIFIER
A5A1	10073-5410	IF AUDIO BOARD ASSY
A16A1	10073-1200	FRONT POWER DIST PWB ASSY
A16A2	10073-1400	CHASIS POWER DISTRIBUTION
A16A3	10073-1350	REAR POWER DISTRIBUTION
J10	J90-0012-001	CONN ADP SMB F'DTHRU F-F
S1	10073-7245	FREQ. STAND. SWITCH ASSY
TB1	10073-7121	TER.BLK,FLT CABLE,10POS
W1	10073-7160	CABLE,ASSY,COAX
W2	10073-7161	CABLE,ASSY,COAX
W3	10073-7158	CABLE,ASSY,COAX
W4	10073-7186	CABLE ASSY COAX
W5	10073-7184	CABLE ASSY COAX
W6	10073-7157	CABLE ASSY COAX
W7	10073-7183	CABLE, COAX ASSY
W8	10073-7156	CABLE ASSY COAX

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Table 1. Chassis Assembly A16 Parts List (PL 10073-1000) (Cont.)

Ref. Desig.	Part Number	Description
W9	10073-7054	CABLE,RIBBON
W10	10073-7182	CABLE, COAX ASSY
W11	10073-7246	CABLE, AC POWER
W12	10073-7155	CABLE, COAX ASSY
W13	10073-7154	CABLE, COAX ASSY
W14	10073-7159	CABLE, COAX ASSY
W15	10073-7153	CABLE, COAX ASSY
W16	10073-7150	CABLE, COAX ASSY
W17	10073-7069	RIBBON CABLE (CH PS)
W19	10073-7152	CABLE ASSY
W20	10073-7070	RIB CABLE CONT-PAN
W21	10073-7058	RIBBON (PAN IF/CONT)
W22	10073-7151	CABLE ASSY
W23	10073-7247	SPEAKER CABLE
W24	10073-7055	RIBBON CABLE (MTR CONT)
W26	10073-7056	CABLE,RIBBON
W28	10073-7078	IF AUDIO
W37	10073-7187	CABLE COAX
W38	10073-7248	CABLE ASSY

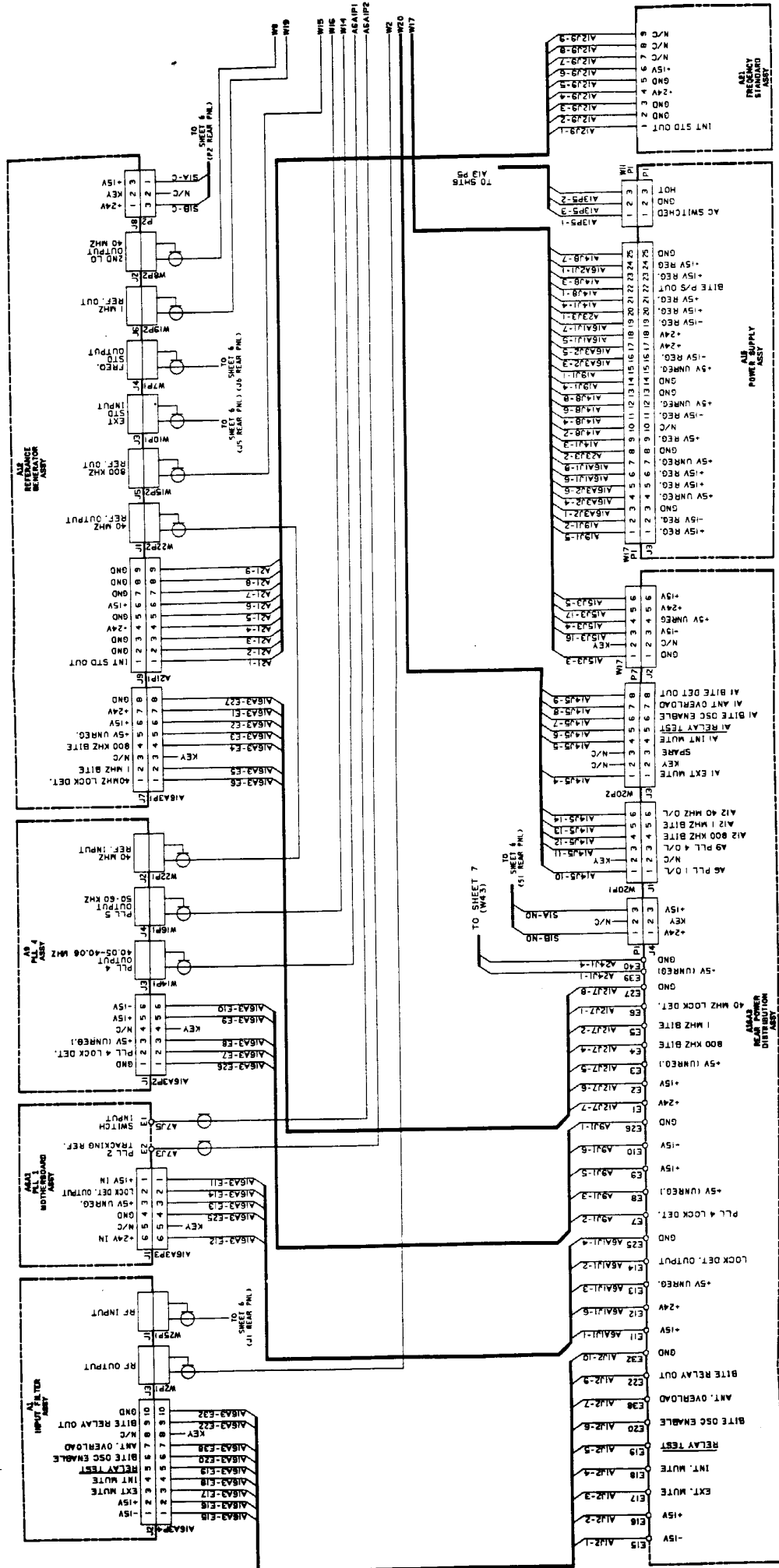
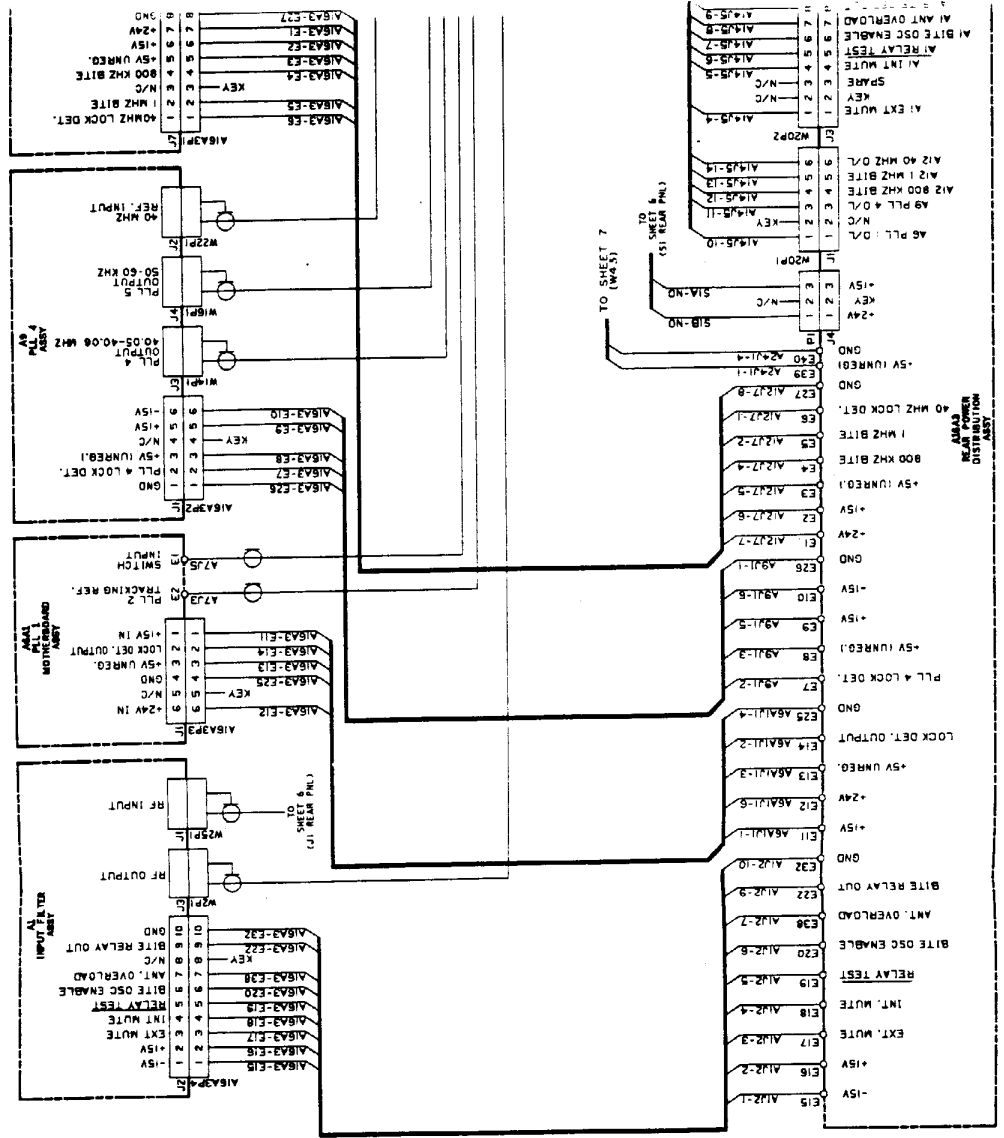


Figure 6. RF-590 Chassis Interconnect Schematic  
Diagram (10073-1001, Rev. J)  
(Sheet 1 of 7)







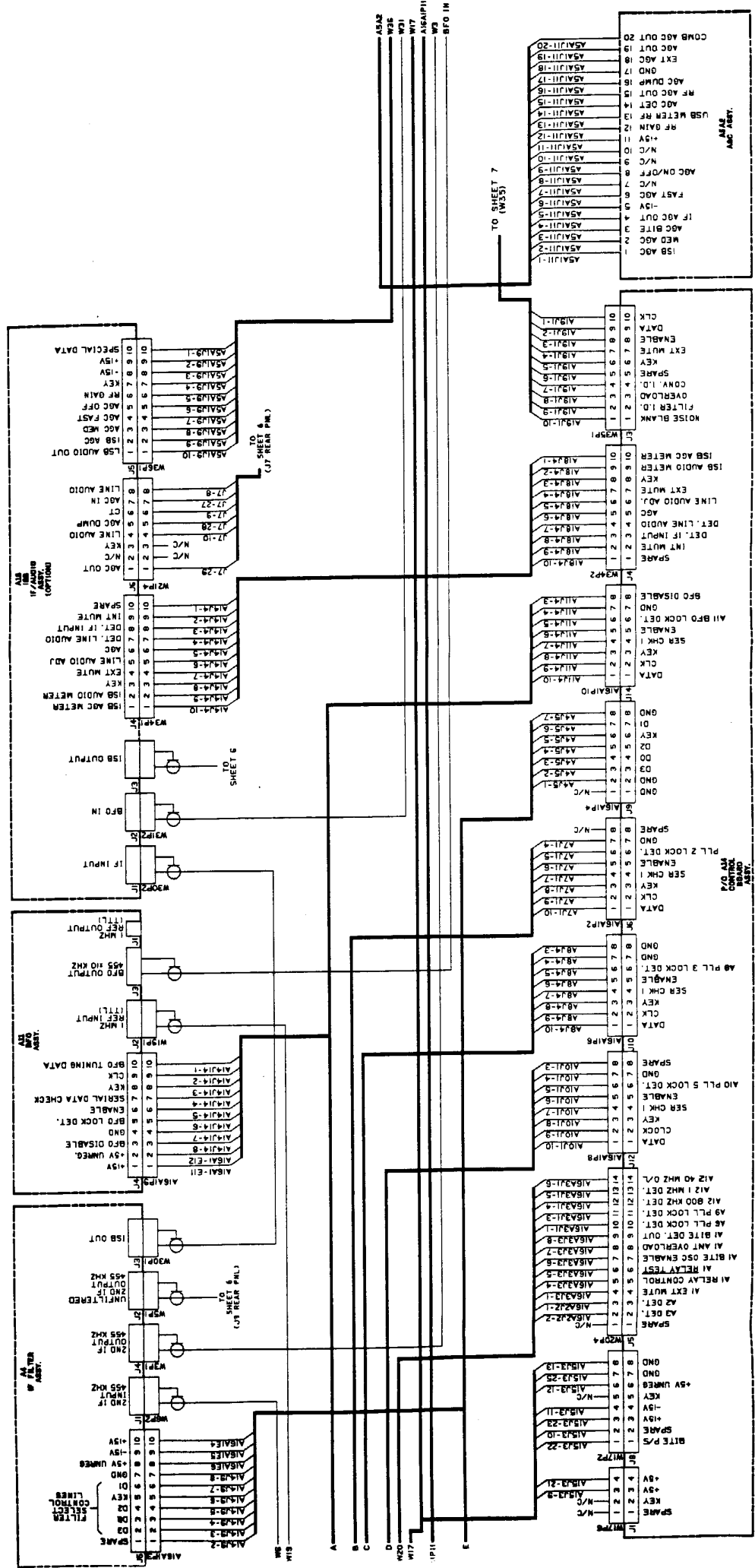


Figure 6. RF-590 Chassis Interconnect Schematic  
Diagram (10073-1001, Rev. J)  
(Sheet 3 of 7)



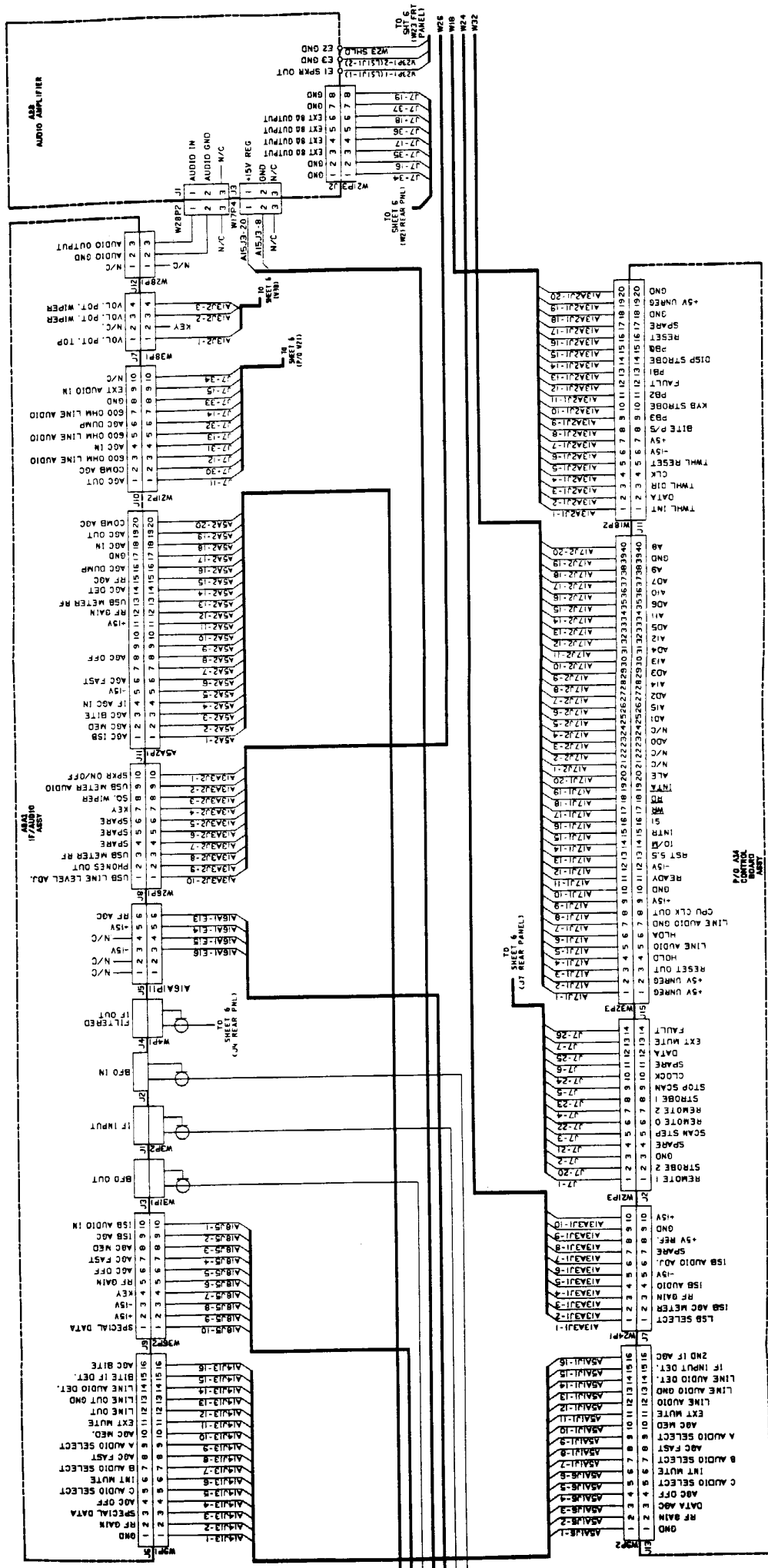


Figure 6. RF-590 Chassis Interconnect Schematic Diagram (10073-1001, Rev. J) (Sheet 4 of 7)



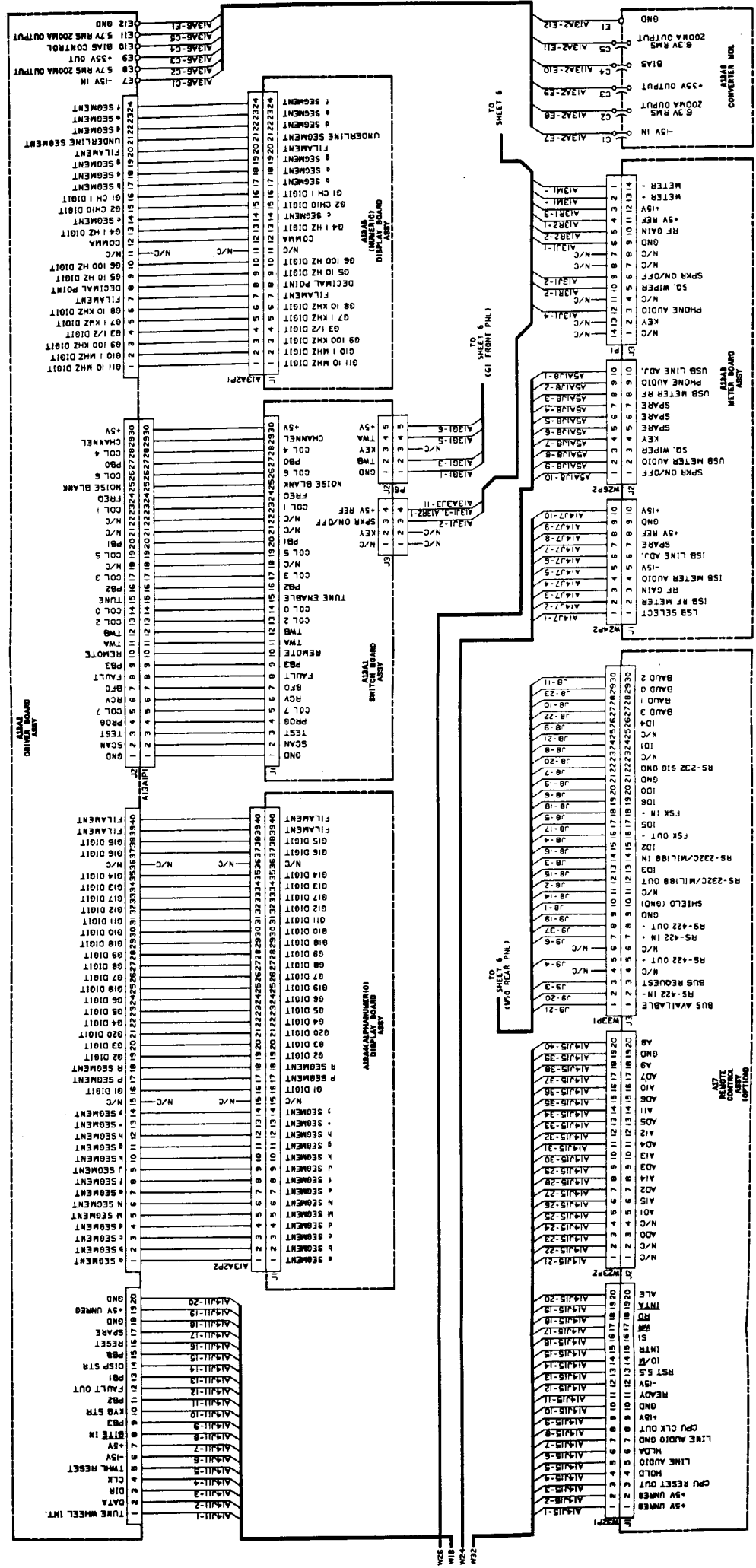


Figure 6. RF-590 Chassis Interconnect Schematic Diagram (10073-1001, Rev. J) (Sheet 5 of 7)

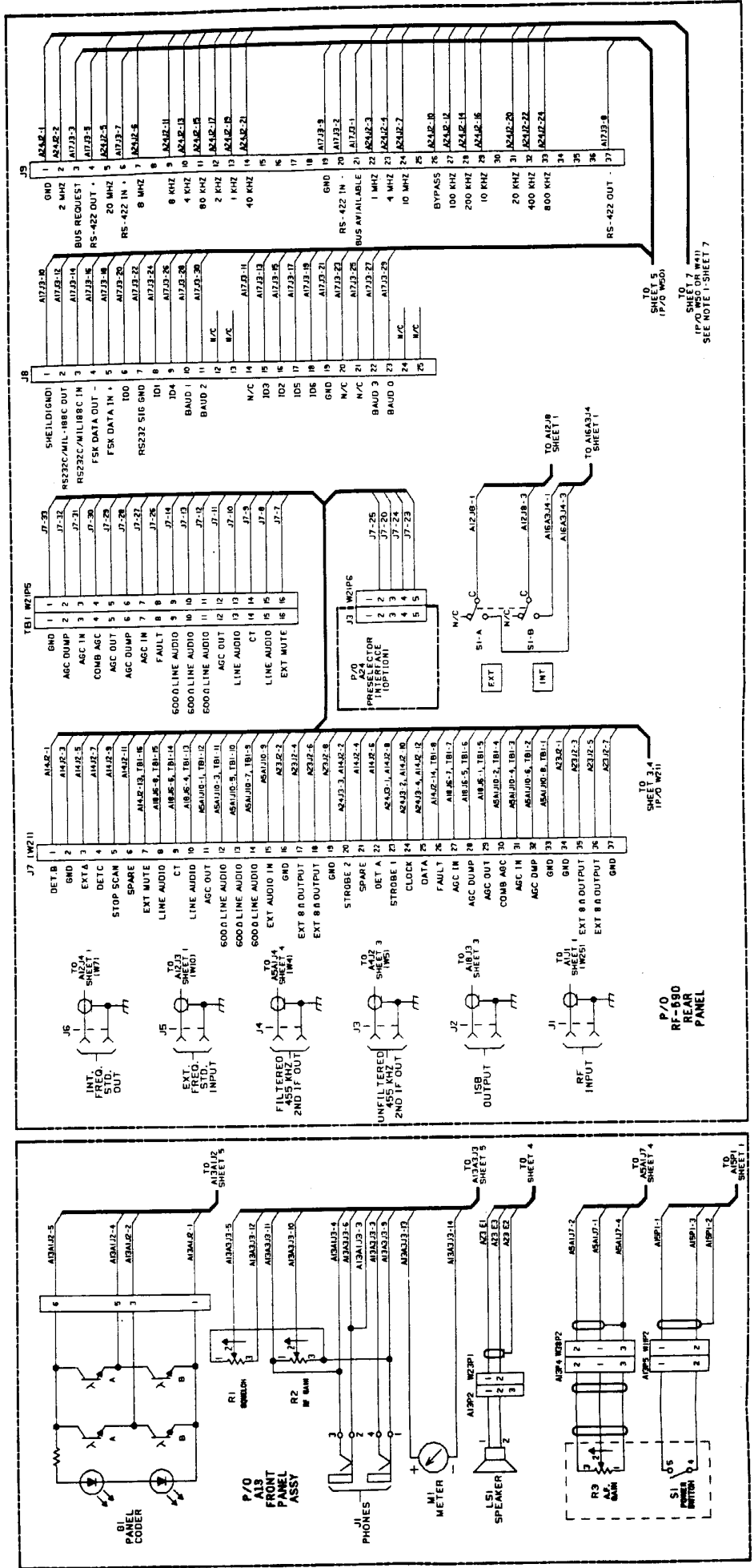
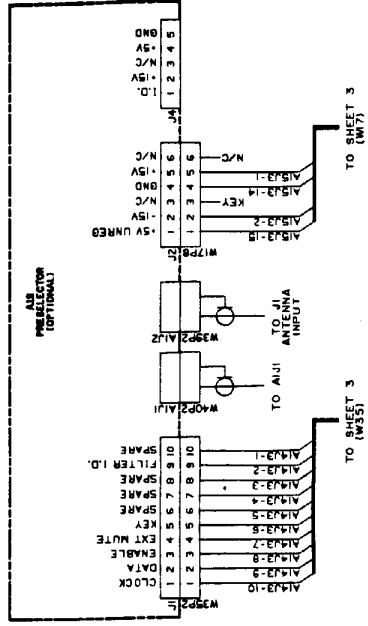
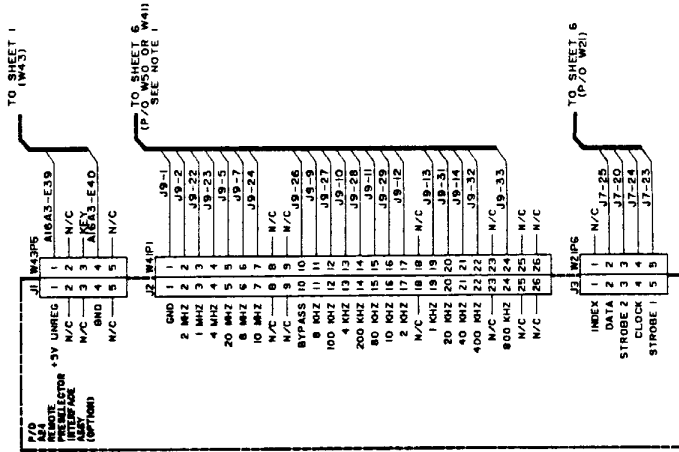


Figure 6. RF-590 Chassis Interconnect Schematic  
Diagram (10073-1001, Rev. J)  
(Sheet 6 of 7)

NOTES: THE A17 AND A24 OPTIONS ARE INSTALLED. THEN PART  
1. IF CABLE CONNECTS TO THE A24 ASSEMBLY AND CABLE  
ON 1 IS NOT USED.



#### 4. MAIN CHASSIS POWER DISTRIBUTION PWBS

Interconnections to PWBs are made by mass terminated ribbon cables and the following three power distribution PWBs.

- A16A1 Front Power Distribution (section 7)
- A16A2 Chassis Power Distribution (section 8)
- A16A3 Rear Power Distribution (section 9)

All cabling is keyed and polarized to prevent misalignment of plugs.

All PWB assemblies can be removed by removing the standard mounting hardware and connectors supplied. No unsoldering is required.

Internal covers providing Radio Frequency Interference (RFI) protection fit snugly over most of the assembly compartments listed in 1.1 and 1.2. Their snap in design makes removal easy. Top and bottom outer covers are fastened to the unit with quarter turn fasteners.

The RF-590 may be rack mounted into a standard 19-inch rack by securing rack slides to the chassis side rails in the mounting holes provided for this purpose.

##### 4.1 Front Power Distribution Board A16A1

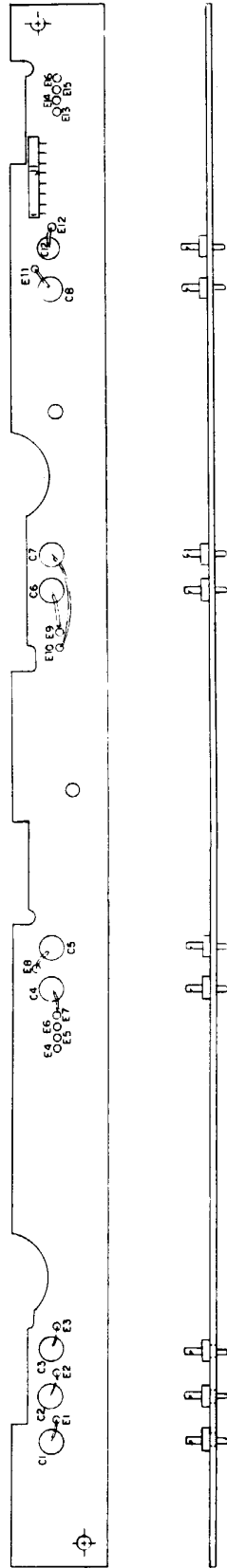
The A16A1 assembly is located on the underside of the main chassis and mounts through cutouts in the walls of the A7, A8, A10, and A11 compartments. The distribution board carries power to these assemblies via connector J1 from Power Supply Assembly A15. It also feeds power (through chassis cutouts) to the Chassis Distribution Board A16A2 mounted on the top side of the chassis, and power to the A4 and A5 assemblies.

Table 2 is the Front Power Distribution Board A16A1 parts list. Figures 7 and 8 are the Front Distribution Board A16A1 component location and schematic diagrams.

**Table 2. Front Power Distribution Board A16A1 Parts List (PL 10073-1200)**

Ref. Desig.	Part Number	Description
C1 - C9	10073-1200	PWB, FRONT PWR DIST
J1	CK05BX102M	CAP 1000PF 20% 200V CER
W1	J46-0033-008	HDR 8 PIN 0.100" RT ANG
W2	10073-7061	RIBBON CABLE, 7 COND
W3	10073-7057	RIBBON CABLE, 24 COND
W4	10073-7057	RIBBON CABLE, 24 COND
W5	10073-7057	RIBBON CABLE, 24 COND
W6	10073-7064	CABLE, RIBBON
	10073-7073	CABLE, RIBBON

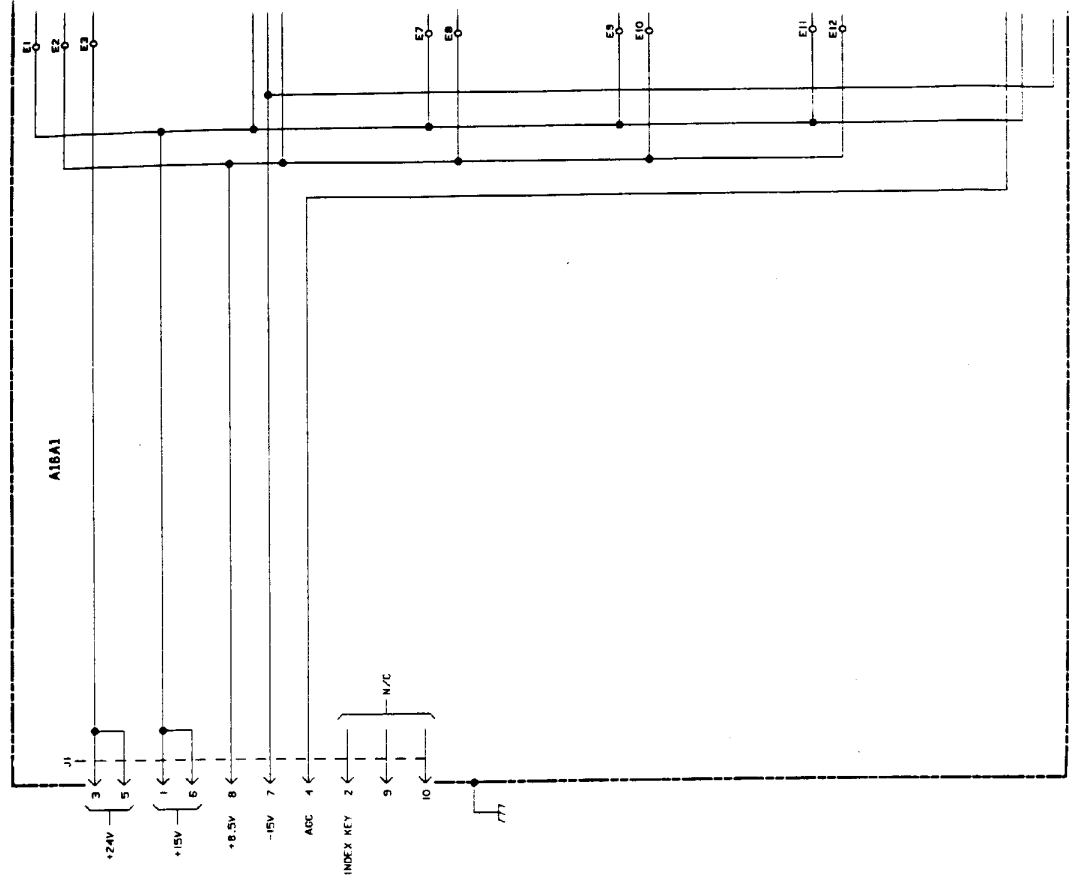




**Figure 7. Front Power Distribution Board A16A1 Component Location Diagram (10073-1200, Rev. E)**



NOTE: UNLESS OTHERWISE SPECIFIED:  
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 FOR A COMPLETE DESIGNATION, PREFIX WITH  
 UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.



#### 4.2 Chassis Power Distribution Board A16A2

The A16A2 assembly is located on the top side of the main chassis and mounts through cutouts in the walls of the A2 and A3 compartments. The assembly receives power and AGC signals via connector J1 from Front Power Distribution Board A16A1. It also carries A2 and A3 BITE information to Control Board Assembly A14 via connector J2.

Table 3 is the Chassis Power Distribution Board A16A2 parts list. Figures 9 and 10 are the Front Distribution Board A16A1 component location and schematic diagrams.

**Table 3. Chassis Power Distribution Board A16A2 Parts List (PL 10073-1400)**

Ref. Desig.	Part Number	Description
	10073-1400	PWB, CHASSIS PWR DIST
C1	C05-0003-102	CAP 1000PF GMV FEED-THRU
C2	C05-0003-102	CAP 1000PF GMV FEED-THRU
C3	C05-0003-102	CAP 1000PF GMV FEED-THRU
C4	C05-0003-102	CAP 1000PF GMV FEED-THRU
C5	C05-0003-102	CAP 1000PF GMV FEED-THRU
C6	C05-0003-102	CAP 1000PF GMV FEED-THRU
C7	C05-0003-102	CAP 1000PF GMV FEED-THRU
J1	J46-0033-004	HDR 4 PIN 0.100" RT ANG
J2	J46-0033-004	HDR 4 PIN 0.100" RT ANG
P1	J46-0016-005	CONN HOUSING 5 POS 24AWG
P2	J46-0016-005	CONN HOUSING 5 POS 24AWG

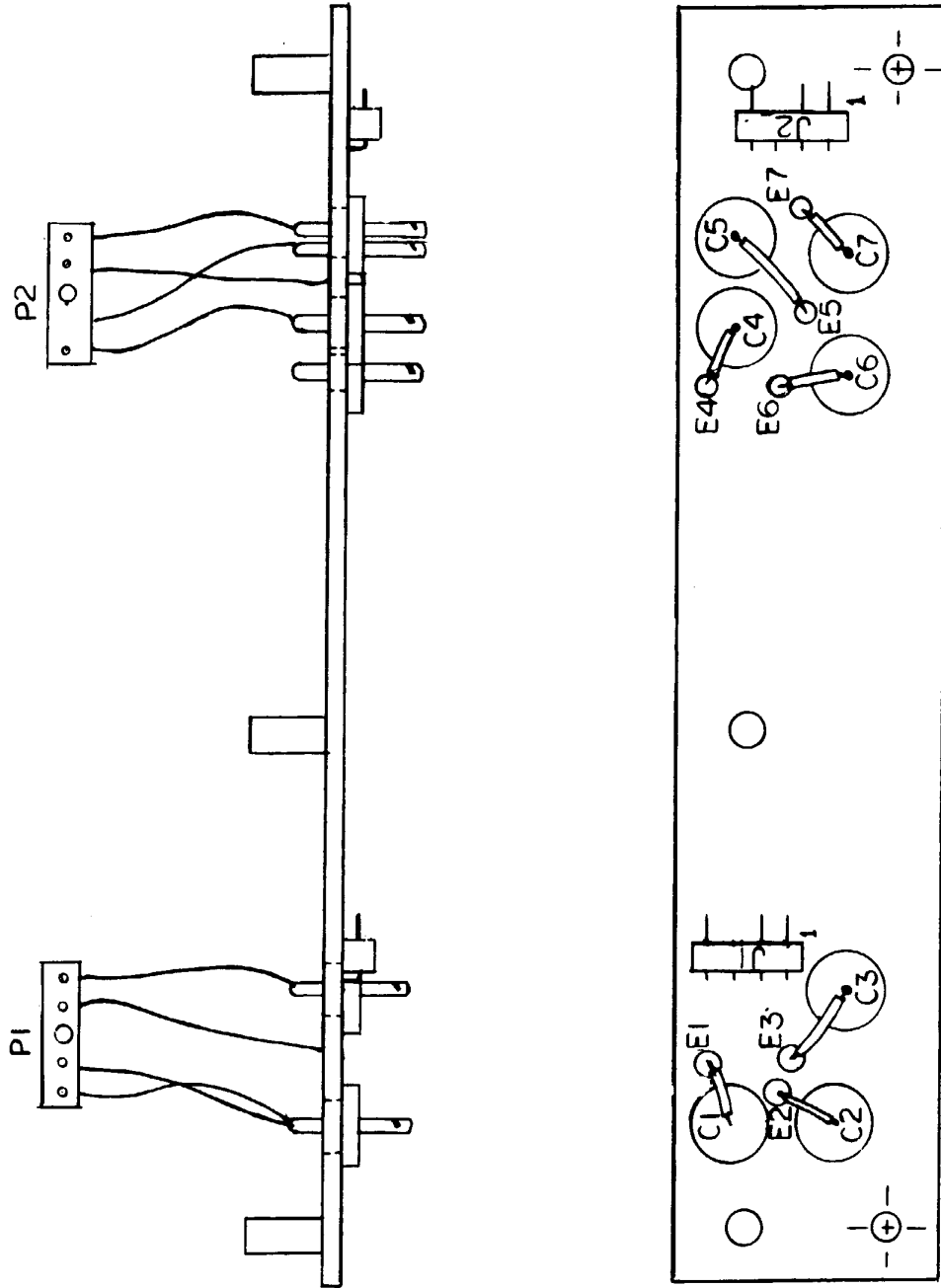


Figure 9. Chassis Power Distribution Board A16A2 Component Location Diagram (10073-1400, Rev. B)

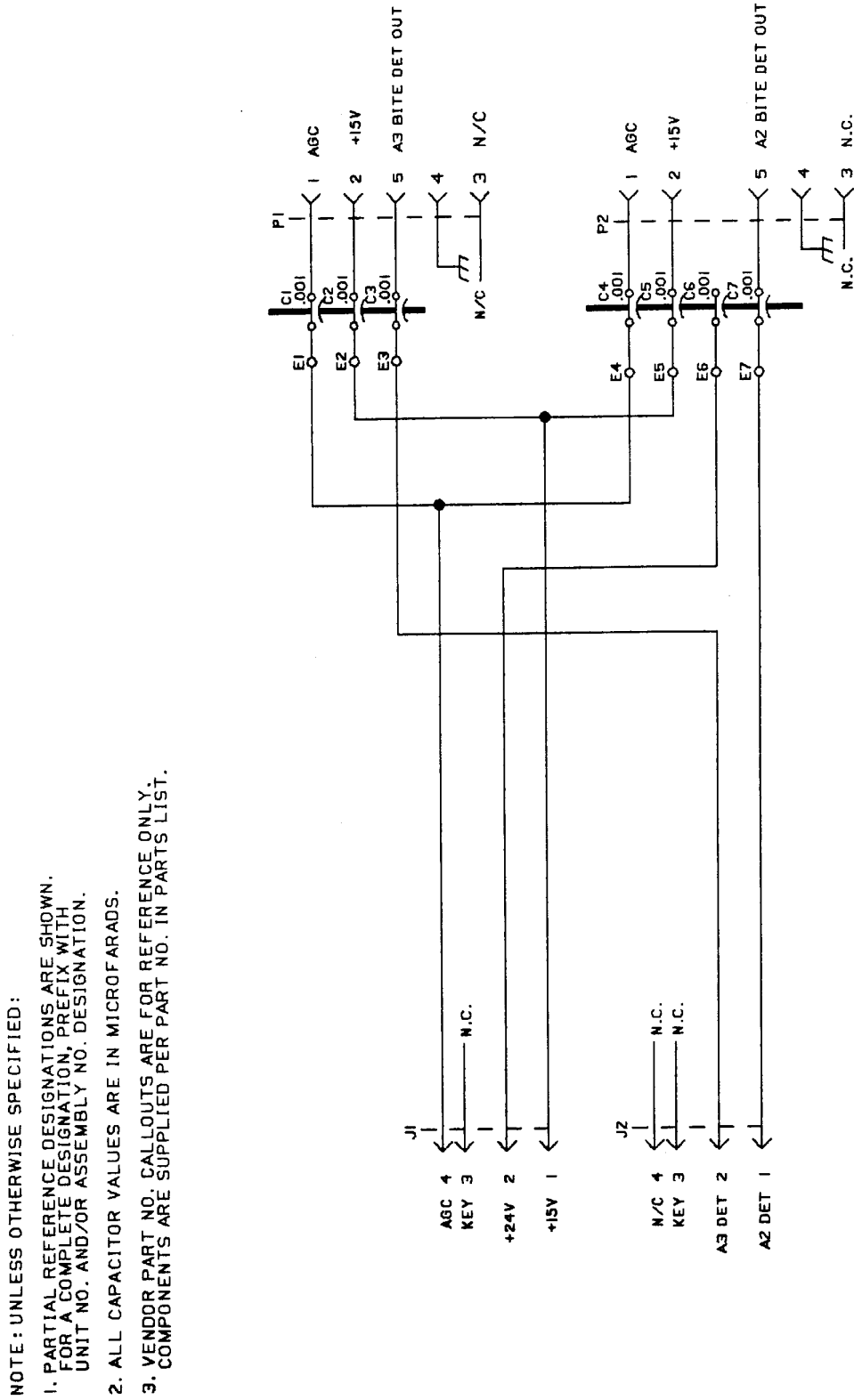


Figure 10. Chassis Power Distribution Board A16A2 Schematic Diagram (10073-1401, Rev. C)

### 4.3 Rear Power Distribution Board A16A3

The A16A3 assembly is located on the underside of the main chassis and mounts through cutouts in the walls of the A1, A6, A9, and A12 assemblies. It receives and distributes power from Power Supply Assembly A15 via connector J2. J4 connects to the RF-590 rear panel INT/EXT frequency standard switch. J1 carries BITE information to Control Board Assembly A14. J3 carries A1 control information to Control Board Assembly A14.

Table 4 is the Rear Power Distribution Board A16A3 parts list. Figures 11 and 12 are the Rear Power Distribution Board A16A3 component location and schematic diagrams.

**Table 4. Rear Power Distribution Board A16A3 Parts List (PL 10073-1350)**

Ref. Desig.	Part Number	Description
A16A3	10073-1350	PWB, REAR PWR DIST
C1	10073-7035	CAP,FEED-THRU 100
C2	10073-7035	CAP,FEED-THRU 100
C3	10073-7035	CAP,FEED-THRU 100
C4	10073-7035	CAP,FEED-THRU 100
C5	10073-7035	CAP,FEED-THRU 100
C6	10073-7035	CAP,FEED-THRU 100
C7	10073-7035	CAP,FEED-THRU 100
C8	10073-7035	CAP,FEED-THRU 100
C9	10073-7035	CAP,FEED-THRU 100
C10	10073-7035	CAP,FEED-THRU 100
C11	10073-7035	CAP,FEED-THRU 100
C12	10073-7035	CAP,FEED-THRU 100
C13	10073-7035	CAP,FEED-THRU 100
C14	10073-7035	CAP,FEED-THRU 100
C15	10073-7035	CAP,FEED-THRU 100
C16	10073-7035	CAP,FEED-THRU 100
C17	10073-7035	CAP,FEED-THRU 100
C18	10073-7035	CAP,FEED-THRU 100
C19	10073-7035	CAP,FEED-THRU 100
C20	10073-7035	CAP,FEED-THRU 100
C21	10073-7035	CAP,FEED-THRU 100
C22	10073-7035	CAP,FEED-THRU 100
C24	10073-7035	CAP,FEED-THRU 100
JMP1, JMP2	MP-1142	CIRCUIT JUMPER
J1, J2	J46-0033-006	HDR 6 PIN 0.100" RT ANG
J3	J46-0033-008	HDR 8 PIN 0.100" RT ANG
J4	J46-0033-003	HDR 3 PIN 0.100" RT ANG
P1	J46-0016-008	CONN HOUSING 8 POS 24AWG
P2, P3	J46-0016-006	CONN HOUSING 6 POS 24AWG
P4	J46-0016-010	CONN HOUSING 10 POS 24AWG
W43	10073-6915	CABLE ASSY

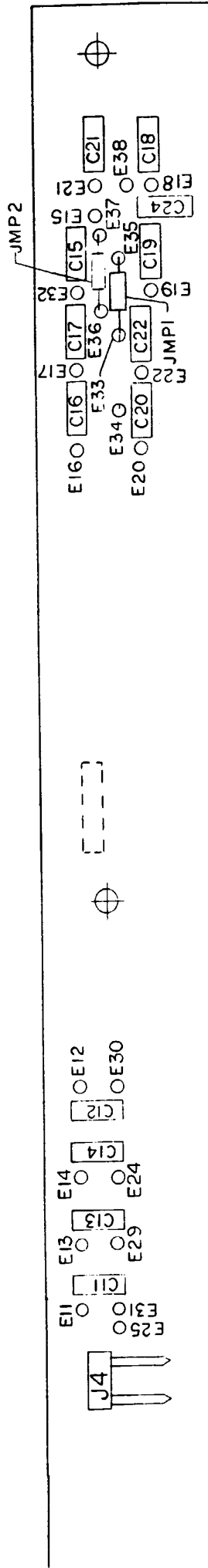
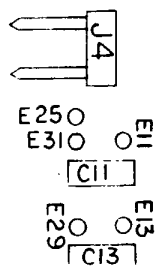
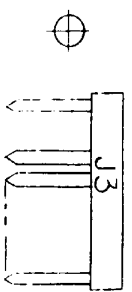
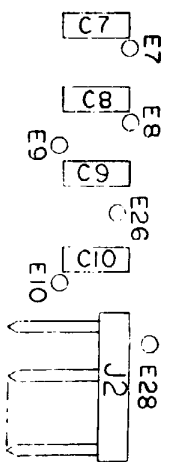
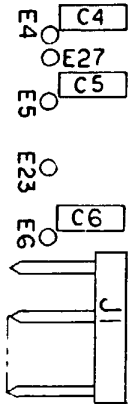
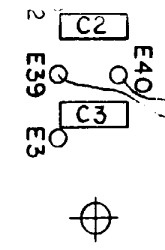
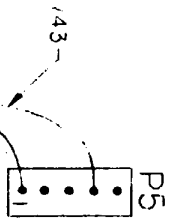
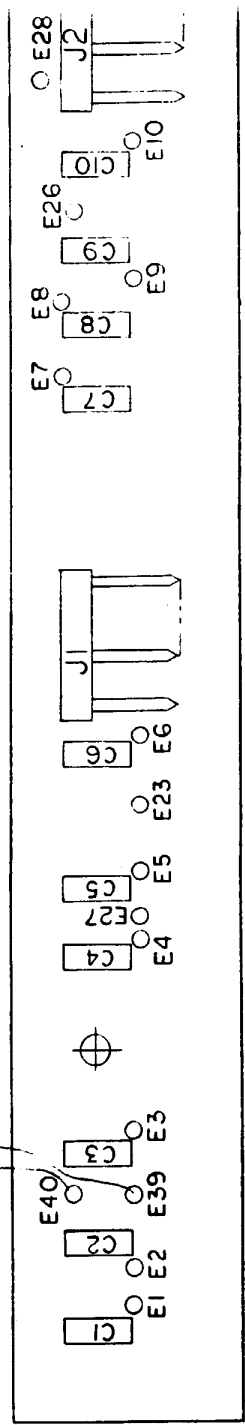
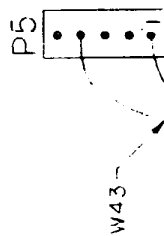
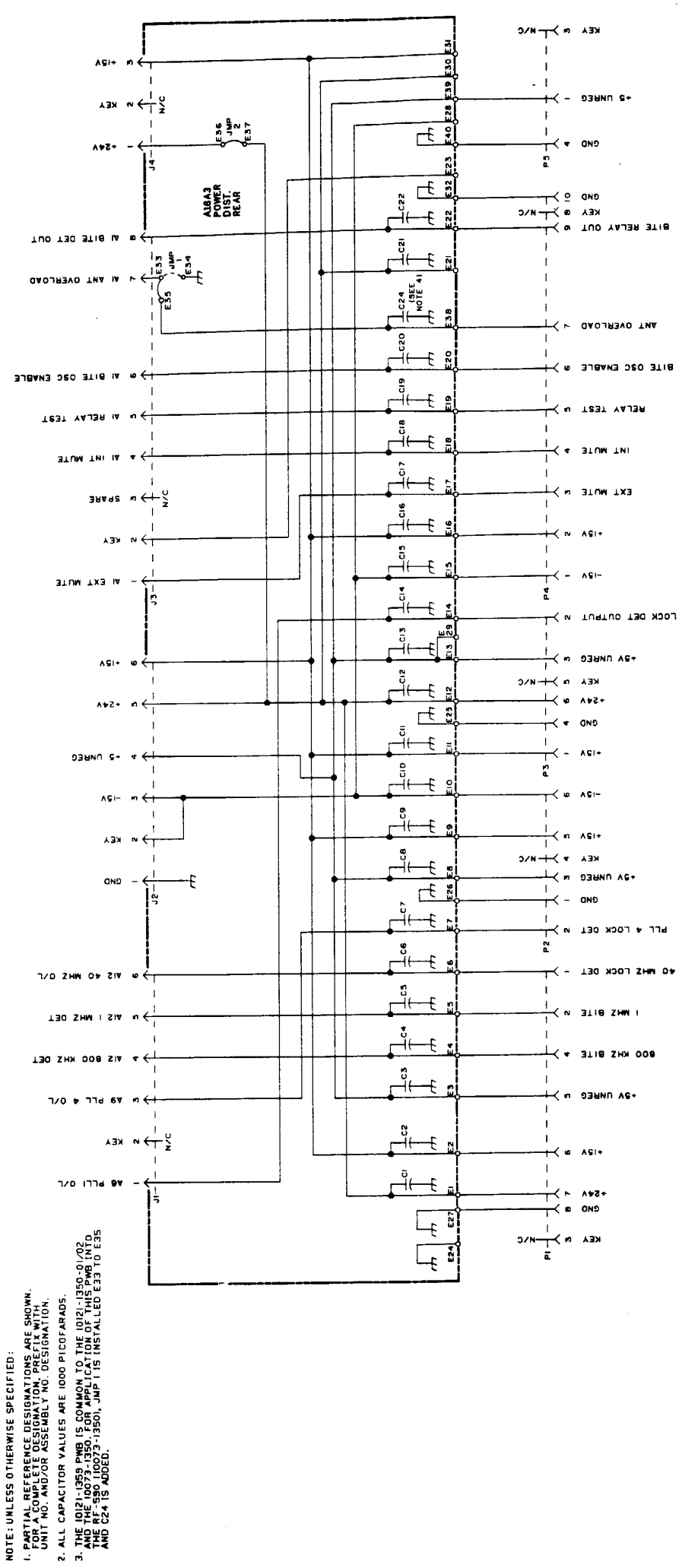


Figure 11. Rear Power Distribution Board  
A16A3 Component Location  
Diagram (10073-1350, Rev. B)







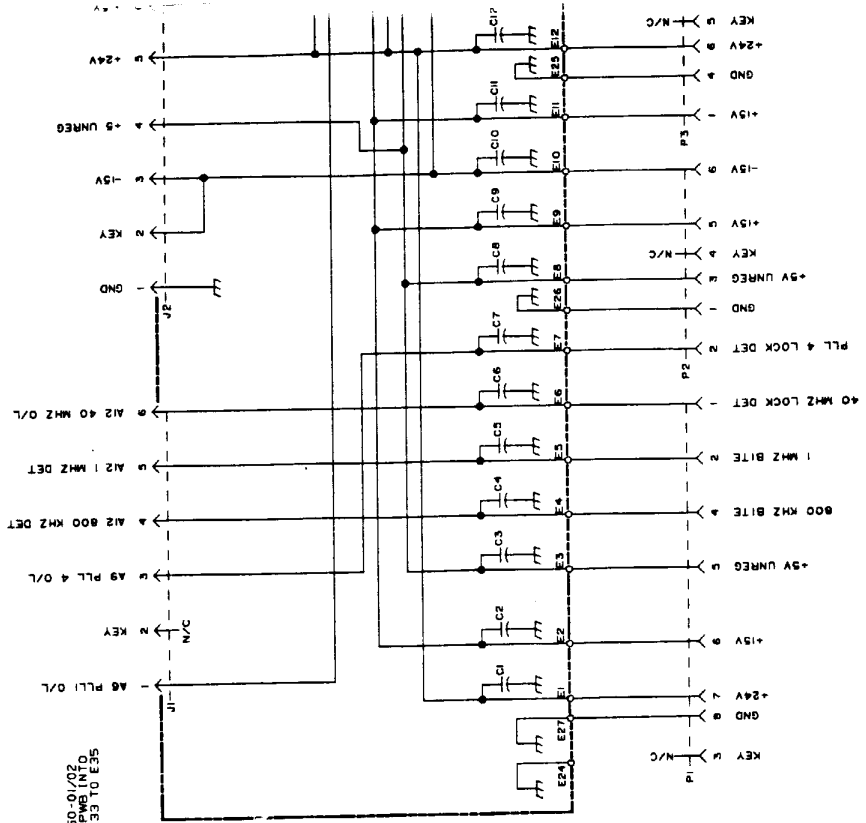


NOTE: UNLESS OTHERWISE SPECIFIED:  
 1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
 FOR A COMPLETE DESIGNATION, PREFIX WITH  
 UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.  
 2. ALL CAPACITOR VALUES ARE 1000 PICOFARADS.  
 3. THE 10121-1359 PWB IS COMMON TO THE 10121-1350-01/02  
 AND THE 10073-1350. FOR APPLICATION OF THIS PWB INTO  
 THE RF-550 (10073-1350), JMP 1 IS INSTALLED E33 TO E35  
 AND C24 IS ADDED.

Figure 12. Rear Power Distribution Board A16A3  
 Schematic Diagram (10073-1351,  
 Rev. A)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR IDENTIFICATION PURPOSES ONLY. UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL CAPACITOR VALUES ARE 1000 PICOFARADS.
3. THE 10121-1359 PWB IS COMMON TO THE 10121-1350-01/02 AND THE 6073-0350. FOR APPLICATION OF THIS PWB INTO THE 6073-0350, JMP-1 IS INSTALLED E33 TO E35 AND C24 IS ADDED.





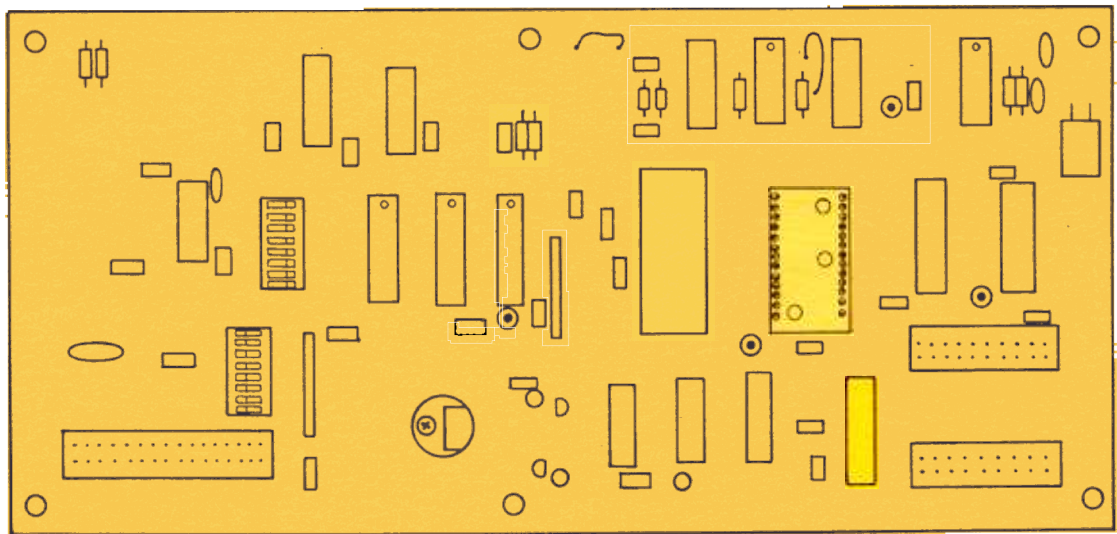
SUPPLEMENT NUMBER: SU-10073-0017A  
TO  
PUBLICATION NUMBER: 10073-0020A  
JULY 1983



RF COMMUNICATIONS

# REMOTE CONTROL ASSEMBLY

## (A17 ASSEMBLY)



# REMOTE CONTROL ASSEMBLY

(A17 ASSEMBLY)

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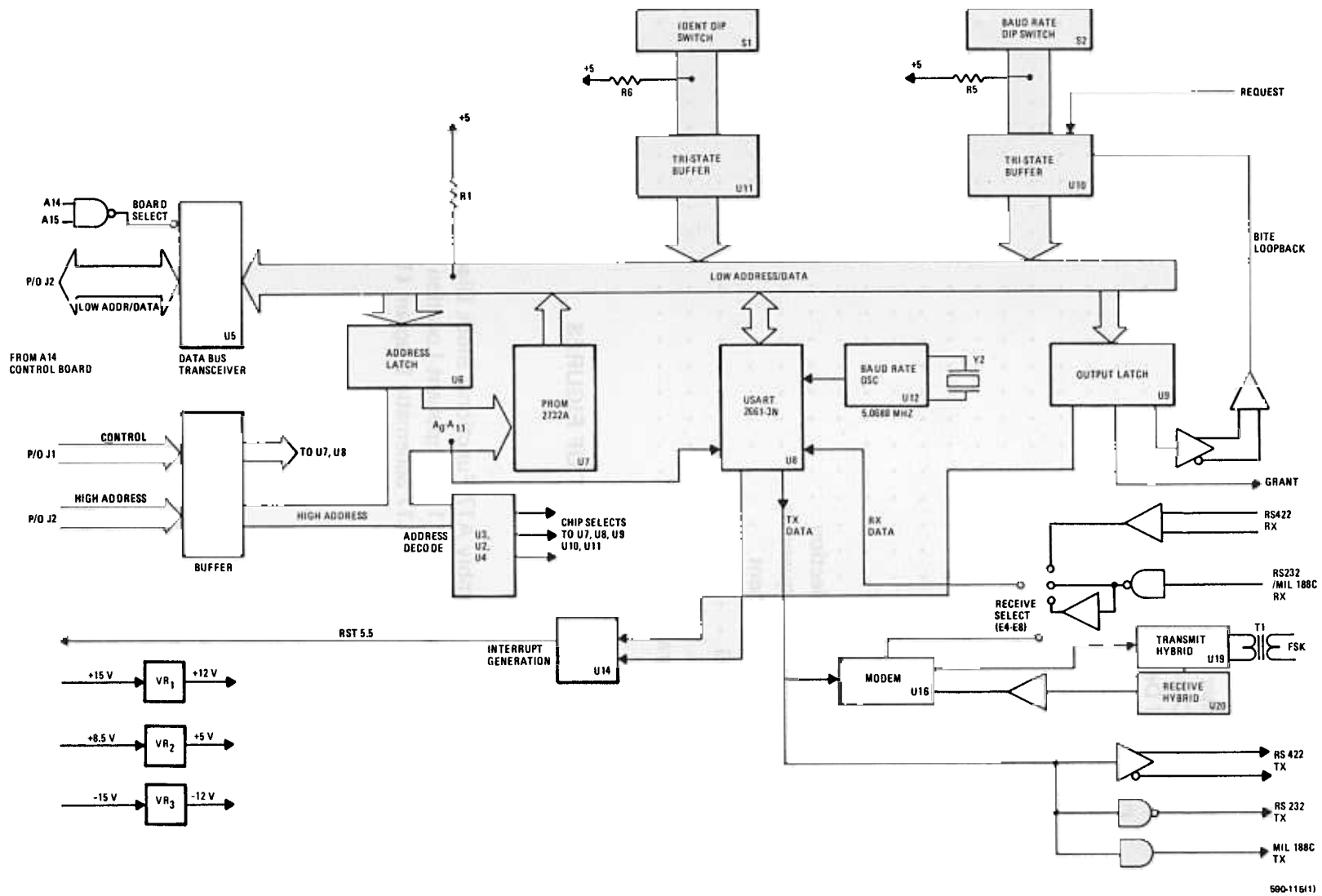
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590-116(1)

Remote Control Assembly A17 Functional Block Diagram



## 1. GENERAL DESCRIPTION

Remote Control Assembly (LCU) A17 provides facilities necessary to permit control of the RF-590 Receiver from a remote site. Connected to the microprocessor controlling the RF-590, this assembly contains interface buffering to Control Board A14, additional program memory, and circuits for parallel I/O, serial I/O controls, and modem. It functions as a local control unit (LCU) for the receiver providing RS-232C, MIL-STD-188C, RS-422, and FSK interface options to a distant remote control unit (RCU). The software programming using one 4K byte EPROM interfaces the A17 control and communication functions to the main control software on the A14 assembly. Electrical connection to the receiver from A17 is through ribbon cables to the control board and to interface connectors J8 and J9 on the RF-590 rear panel.

## 2. INTERFACE CONNECTIONS

LCU Assembly A17 interface connections are summarized in table 1

Table 1. LCU Assembly A17 Interface Summary

Connector	Function	To	From
A17J1-1	+8.5V	—	A14J15-1
-2	+8.5V	—	A14J15-2
-3	Reset Out	—	A15J15-3
-4	HOLD	A14J15-4	—
-5	Line Audio	—	A14J15-5
-6	HLDA	—	A14J15-6
-7	Line Audio Gnd	—	A14J15-7
-8	CPU Clk. Out	—	A14J15-8
-9	+15V	—	A14J15-9
-10	Gnd	—	A14J15-10
-11	Ready	A14J15-11	—
-12	-15V	—	A14J15-12
-13	RST 5.5	A14J15-13	—
-14	IO/M	—	A14J15-14
-15	INTR	A14J15-15	—
-16	S1	—	A14J15-16
-17	WR	—	A14J15-17
-18	RD	—	A14J15-18
19	INTA	—	A14J15-19
-20	ALE	—	A14J15-20

Table 1. LCU Assembly A17 Interface Summary (Cont.)

Connector	Function	To	From
A17J2-1	N/C	—	—
-2	N/C	—	—
-3	AD0	Bidirec	A14J15-23
-4	N/C	—	—
-5	AD1	Bidirec	A14J15-25
-6	A15	—	A14J15-26
-7	AD2	Bidirec	A14J15-27
-8	A14	—	A14J15-28
-9	AD3	Bidirec	A14J15-29
-10	A13	—	A14J15-30
-11	AD4	Bidirec	A14J15-31
-12	A12	—	A14J15-32
-13	AD5	Bidirec	A14J15-33
-14	A11	—	A14J15-34
-15	AD6	Bidirec	A14J15-35
-16	A10	—	A14J15-36
-17	AD7	Bidirec	A14J15-37
-18	A9	—	A14J15-38
-19	Gnd	—	A14J15-39
-20	A8	—	A14J15-40
A17J3-1	Bus Available	—	J9-21
-2	RS-422 IN —	—	J9-20
-3	Bus Request	J9-3	—
-4	N/C	—	—
-5	RS-422 OUT +	J9-4	—
6	N/C	—	—
-7	RS-422 IN +	—	J9-6
-8	RS-422 OUT —	J9-37	—
-9	Gnd	J9-19	—
-10	Shield (Gnd)	J8-1	—
-11	N/C	—	—
-12	RS-232 TX	J8-2	—
-13	ID3	—	J8-15
-14	RS-232 RX	—	J8-3
-15	ID2	—	J8-16
-16	RSK Data OUT —	J8-4	—
-17	ID5	—	J8-17
-18	FSK Data IN +	—	J8-5
-19	ID6	—	J8-18
-20	ID0	—	J8-6

Table 1 LCU Assembly A17 Interface Summary (Cont.)

Connector	Function	To	From
A17J3-21	Gnd	J8-19	—
-22	RS-232 Sig. Gnd	J8-7	—
-23	N/C	—	—
-24	ID1	—	J8-8
-25	N/C	—	—
-26	ID4	—	J8-9
-27	BR3	—	J8-22
-28	BR1	—	J8-10
-29	BR0	—	J8-23
-30	BR2	—	J8-11

### 3. FUNCTIONAL DESCRIPTION

#### 3.1 Control and Data Transfer

When installed in the RF-590, the A17 assembly appears as an electrical extension of the address/data bus of the microprocessor on the A14 assembly. This bus is buffered by tri-state bidirectional buffer U5 and high-order address and control inputs buffered by U1. Selection of IC devices on the LCU for data transfer to/from the CPU is done using three-to-eight decoder U3 with high-order address bits. Interface signals  $\overline{RD}$ ,  $\overline{WR}$ , and S1 from the A14 assembly determine the direction of data flow after addresses have been loaded into latch U6 by ALE, the address latch enable.

The information stored in the EPROM is part of the system software and is not customer alterable.

#### 3.2 Serial Data Transmission/Reception

Upon power up reset, the controlling CPU (A14U1) detects the presence of the LCU option, and initializes all IC devices on A17. Using the software in the LCU EPROM, the CPU conditions the USART U8 to receive incoming signals according to user-selected options. When response to a distant RCU is required by this RF-590 LCU, the transmit interface is enabled, and appropriate parallel data sent via address/data bus AD0-AD7 from the CPU is converted to serial data by USART U8. Completed reception/transmission of message characters by U8 is signaled to the CPU by interrupt line RST 5.5, generated by U8 and U14. The BRCLK input to the USART is from the 5.0688 MHz crystal oscillator circuit using Y2.

#### 3.3 Serial Interfaces

The A17 assembly provides all standard data communication interfaces (each is individually jumper selectable). For RS-232C/MIL-STD-188C interfaces, 1488 drivers in U15 and 1489A receiver U21 are used. The RS-422 interface utilizes tri-state drivers of U13 and receiver in U18.

## Parallel Data I/O

Parallel data I/O is accomplished by input buffers U10 and U11 reading user-selected options from DIP switches S1 and S2. Outputs from latch U9 select operating modes of modem U16 and the interface control functions. Data transfer to/from these parallel I/O elements, as well as USART U8, is managed by chip selects from U3 combined with appropriate  $\overline{RD}$  and  $\overline{WR}$  signals in U4.

### 3.5 Modem I/O

The TXD signal from USART U8 (2661) is presented in serial data format to the TXD input of universal low speed (0-600 bps) modem U16 (MC14412) for conversion to frequency shift keying (FSK) signals. The 1.0 MHz Y1 crystal is required to utilize the U16 on chip oscillator. The TXCND signal (transmit carrier), a digitally synthesized sine wave derived from the 1.0 MHz oscillator reference is applied to the filter input of transmit filter/line hybrid U19 (1262). With the MODE input from parallel data control U9 (74LS374) set to "1" and the TYPE input from switch S1 set to "1", the US standard originate frequencies are used. A MARK "1" is 1270 Hz while a SPACE "0" is 1070 Hz. The RX RATE input to U16 selects a receive data rate of 0-600 bits per second (bps).

Transmit filter/line hybrid U19 lowpass filters the oscillator output to attenuate those modulation components which would interfere with the adjacent channel. The CHAN SELECT signal input of U19 (1262), via part of dual op amp U22 allows the filter to pass the originate frequencies 1170 Hz  $\pm$  100 Hz when the CHAN SELECT signal is -12V and the answer frequencies 2125 Hz  $\pm$  100 Hz when the CHAN SELECT signal is +12V. U19 (1262) also contains an active line hybrid which couples the modem to the line. T1 provides a 600 ohm balanced audio output. LEVEL ADJ potentiometer R20 allows the operator to adjust the hybrid output level. The XMT FSK output signal is applied to the distant RCU via rear panel connector J8.

The RCV RSK input signal from the distant RCU via connector J8 is passed through U19 (1262) to receive filter U20 (1267) as the RCV FSK signal. Receive filter U20 (1267) attenuates signals outside the channel passband and also band limits noise energy from the line. The CHAN SELECT signal input to U20 (1267) allows the filter to pass the originate frequencies 1170 Hz  $\pm$  100 Hz when the CHAN SELECT signal is -12V and the answer frequencies 2125 Hz +100 Hz when the CHAN SELECT signal is +12V. U20 (1267) also contains a soft limiter amplifier which limits the RXCND signal to supply the demodulator in U16 (MC14412) with a square wave FSK signal. The RXCND signal is demodulated and routed to serial I/O (USART) U8 as the RXD signal via jumper A17E8 to A17E4.

### BITE (Self-Test)

When installed, the A17 LCU hardware is tested along with all other RF-590 functions during execution of the build-in-test (BITE) feature of the receiver. These tests are performed if the receiver is in Local or Remote operation. Specifically, three LCU tests are made: a test of USART U8 function, a checksum test to ensure correct EPROM function, and a test of parallel I/O and RS-422 receivers. The corresponding BITE fault codes are:

- Fault 01 – EPROM (U7) fault
- Fault 02 – Communications (USART U8) fault
- Fault 03 – Interface (U9, U10, U17, U18) fault

**Dc Distribution**

The A17 assembly receives three supply voltages from A14, each of which is converted by local regulators to provide voltages needed by the LCU circuits. The +8.5 volt input is regulated by VR2 to yield the +5V logic supply. The +15V and -15V inputs are converted by regulators VR1 and VR3 respectively to provide +12V and -12V levels for the modem and serial interface.

**4. MAINTENANCE**

**4.1 Setup**

**Identification Number**

For use in a remote control system consisting of many RF-590 or other compatible units, each LCU must be setup to have an individual unique identification number. This number, an eight-bit Binary code is set up on DIP switch S1 and allows 255 individual unit codes (1 to 255) according to table 2.

**Table 2. Identification Number Setup**

Switch	Binary Weight
S1-1	128 (highest order bit)
S1-2	64
S1-3	32
S1-4	16
S1-5	8
S1-6	4
S1-7	2
S1-8	1 (lowest order bit)

0 = switch closed  
1 = switch open

For example, leaving only S1-4 and S1-7 open and all other S1 switches closed, forms the binary identification number 00010010 which is 16 + 2 = 18 (in decimal format).

#### 4.1.2 Baud Rate Selection

The RF-590 LCU allows any of sixteen popular baud rates to be used in communication through the USART U8. The baud rate is selectable by setting switches on DIP switch S2 according to table 3.

**Table 3. Baud Rate Setup**

S2-1	S2-3	S2-4	S2-7	Baud Rate
C	C	C	C	50
C	O	C	C	75
C	C	C	O	110
C	O	C	O	134.5
C	C	O	C	150
C	O	O	C	300
C	C	O	O	600
C	O	O	O	1200
O	C	C	C	1800
O	O	C	C	2000
O	C	C	O	2400
O	O	C	O	3600
O	C	O	C	4800
O	O	O	C	7200
O	C	O	O	9600
O	O	O	O	19200

O = switch open  
C = switch closed

#### 4.1.3 Signaling Interface Selection

As mentioned before, the RF-590 LCU allows any one of four common signaling interfaces to be used. Typically, the desired interface will be set at the factory. If another interface is needed, configure jumpers as shown in table 4.

**Table 4. Jumper Selection of Interface**

Selected Interface	Jumper Configuration
RS-232C Interface	
RS-232C Tx	E27-E11 Jumpered E14-E16 Jumpered E15-E16 Open

Table 4. Jumper Selection of Interface (Cont.)

Selected Interface	Jumper Configuration
RS-232C Rx	E6-E4 Jumpered E5-E4 Open E7-E4 Open E8-E4 Open
MIL-188C Interface  MIL-188C Tx  MIL-188C Rx	E27-E11 Jumpered E15-E16 Jumpered E14-E16 Open  E7-E4 Jumpered E6-E4 Open E7-E4 Open E8-E4 Open
RS-422 Interface  RS-422 Rx and Tx	E5-E4 Jumpered E6-E4 Open E7-E4 Open E8-E4 Open
Modem (Refer to paragraph 4.1.4)  Modem Tx  Modem Rx	E27-E12 Jumpered  E8-E4 Jumpered E5-E4 Open E6-E4 Open E7-E4 Open

For normal operation, leave jumpers E1-E2 open.

#### 4.1.4 Modem Signalling Frequencies

The FSK modem may be operated using the US Answer or US Originate frequencies from the RF-590 remote control option. Typically, the RF-590 remote option is configured for US Originate operation and the distant controller then must be set for US Answer frequencies. Frequency pair selection is accomplished by the setup listed in table 5. Setup for FSK modem is listed in table 4.

Table 5. US Answer and US Originate Frequencies

RF-590 Option	Jumper Configuration
US Answer	E21-E22 Jumpered E26-E22 Open E26-E24 Jumpered E24-E21 Open
US Originate	E21-E22 Open E26-E22 Jumpered E26-E24 Open E24-E21 Jumpered

#### 4.2 Hybrid Level Adjustment

The following adjustment is for the FSK modem output level, and has been completed at the factory prior to shipment. In the event a board needs repair or realignment, the following procedure has been included.

Connect an HP-3400A Analog Voltmeter, or equivalent, between pins 16 and 18 of connector J8 on the RF-590 rear panel.

- b. Connect an ac power cord on the RF-590 rear panel.

Jumper A17E1 to A17E2.

- d. Set the voltmeter RANGE control to the 1 volt, 0 dBm position.
- e. Turn on the RF-590 power using Power ON/OFF VOLUME control switch/potentiometer located on the front panel.
- f. Adjust hybrid level adjustment A17R20 for a meter reading of 1 volt, 0 dBm.
- g. Turn off power and disconnect test equipment. Remove E1-E2 jumper.

#### 4.3 Troubleshooting

There are six test points located on LCU Assembly A17. Table 6 used together with the schematic diagram and component location drawing should help in locating most A17 problems.



**Table 6. Test Point Indications**

Test Point	Indicates
TP1	A17 address/data buffer enable A17U5
TP2	Chip enable for LCU EPROM A17U7
TP3	LCU activity signal from A17U9
TP4	RST 5.5 interrupt from A17U14
TP5	Modem Transmit carrier (MARK = 1270 Hz, SPACE = 1070 Hz)*
TP6	Modem Receive Carrier (MARK = 2225 Hz, SPACE = 2025 Hz)*
* Modem configured as U.S. Standard Originate.	

Data transfer to or from the microprocessor on Control Board A14 takes place when a logic LOW is seen at TP1. A simultaneous LOW at TP2 indicates the exchange is that of program steps from the EPROM containing software to manage the A17 assembly. When installed in a properly functioning receiver, logic HIGH pulses should be seen once per millisecond at TP3, even if the RF-590 is not in remote operation (with or without an attached, controlling unit). When a controlling unit is operating, its communication with the RF-590 will result in intermittent active high pulses on the interrupt line (TP4), again regardless of the local or remote operation of the receiver.

Absence of activity on points TP1-TP3 indicate a failure in the connection of A17 assembly to Control Board Assembly A14. If the Remote board is not properly installed, an operator pressing the REMOTE button on the RF-590 front panel will get no response. If activity is seen on TP1-TP3 and the receiver can be placed into remote operation (but no activity is seen at TP4), the fault lies in the setup of the A17 board (baud rate or interface jumpering) or in the controller or link between controller and RF-590.

If activity is seen on all four test points during operation with a controller, but the RF-590 cannot be remotely commanded, check that the LCU identification number is properly selected. Also check that this LCU is the one being commanded from the controller. As an aid to checking desired baud rate and identification number setups, apply power to the receiver after the corresponding DIP switches S1 and S2 have been set on A17. With the receiver selected to remote receive operation, depress and hold in the front panel ENTER button. Within ten seconds, the lefthand display of the RF-590 will show the identification number and baud rate selected on A17S1 and A17S2 in a format such as REMOTE # 04 2400 BPS. This is for LCU identification number 4 and a communication rate of 2400 bits per second (baud). Users should change the baud rate switches only when the RF-590 is off so that the A17 PWB will correctly be set up when power is again applied.

**5. PARTS LIST**

Table 7 is a comprehensive parts list of all replaceable components in Remote Control Assembly A17. When ordering parts from the factory, include a full description of the part. Use figure 1, Remote Control Assembly A17 Component Location Diagram to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 2 is the Remote Control Assembly A17 schematic diagram.

**Table 7. Remote Control Assembly A17 Parts List (PL 10073-6200)**

Ref. Desig.	Part No.	Description
	10073-6200	Remote Control Assembly
C1, C2	CK05BX103M	Capacitor, .01 uF
C3	C26-0050-109	Capacitor, 1 uF
C4	CK05BX103M	Capacitor, .01 uF
C5, C6	C26-0050-109	Capacitor, 1 uF
C7-C23	CK05BX103M	Capacitor, .01 uF
C24	CM04FD201J03	Capacitor, 200 pF, 500 V
C25-C27	CK05BX103M	Capacitor, .01 uF
C28	C11-0006-225	Capacitor, 2.2 uF, 50 V
C29	CK05BX103M	Capacitor, .01 uF
C30	CM05FD511J03	Capacitor, 510 pF, 500 V
C31	C22-0005-001	Capacitor, 2.7 uF, 50 V
C32, C33	CM04ED330J03	Capacitor, 33 pF
CR1, CR2	1N5234B	Diode, Zener, 6.2 V
E1, E2	J45-0041-001	Wire Wrap Post
E4-E8	J45-0041-001	Wire Wrap Post
E11, E12	J45-0041-001	Wire Wrap Post
E13-E22	J45-0041-001	Wire Wrap Post
E24, E26	J45-0041-001	Wire Wrap Post
E27	J45-0041-001	Wire Wrap Post
J1, J2	J45-0013-020	Connector, Jack, 20 pin
J3	J45-0013-030	Connector, Jack, 30 pin
R1	R50-0010-103	Resistor, SIP, 10 K
R2, R4	R65-0003-103	Resistor, Carbon Film, 10 K, 1/4 W, 5%
R5	R50-0010-103	Resistor, Network, 10 K
R6	R50-0010-103	Resistor, Network, 10 K
R7	R65-0003-362	Resistor, Carbon Film, 3.6 K
R8	R65-0003-103	Resistor, Carbon Film, 10 K
R9	R65-0003-203	Resistor, Carbon Film, 20 K
R11, R12	R65-0003-473	Resistor
R14	R65-0003-103	Resistor, Carbon Film, 10 K, 1/4 W, 5%
R16, R17	R65-0003-361	Resistor, Carbon Film, 360 ohms, 1/4 W, 5%

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Table 7. Remote Control Assembly A17 Parts List (PL 10073-6200) (Cont.)

Ref. Desig.	Part No.	Description
R18, R19	R65-0003-102	Resistor, Carbon Film, 1 K, 1/4 W, 5%
R20	R30-0002-204	Resistor, Variable, 200 K
R21, R22	R65-0003-471	Resistor, Carbon Film, 470 ohms, 1/4 W, 5%
S1, S2	S50-0001-008	Switch, DIP, 8 position
T1	T30-0001-004	Transformer
TP1	J-0071	Test Point, Brown
TP2	J-0066	Test Point, Red
TP3	J-0069	Test Point, Orange
TP4	J-0070	Test Point, Yellow
TP5	J-0068	Test Point, Yellow
TP6	J-0072	Test Point, Green
U1	I16-0002-000	Integrated Circuit, Octal Buffer
U2	I01-0042-000	Integrated Circuit, Quad AND Gate
U3	I37-0001-000	Integrated Circuit, Three-to-Eight Decoder
U4	I01-0045-000	Integrated Circuit, Quad OR Gate
U5	I58-0006-000	Integrated Circuit, Bus Transceiver
U6	I05-0000-373	Integrated Circuit, 8 Bit Latch
*U7	See Note	Integrated Circuit, 4KX8 EPROM
U8	I59-0005-000	Integrated Circuit, USART
U9	I50-0027-000	Integrated Circuit, 8 Bit Latch
U10	I16-0002-000	Integrated Circuit, Octal Buffer
U11	I16-0002-000	Integrated Circuit, Octal Buffer
U12	I01-0008-000	Integrated Circuit, Hex Inverter
U13	I16-0008-000	Integrated Circuit
U14	I01-0048-000	Integrated Circuit, Quad NAND Gate
U15	I16-0001-000	Integrated Circuit, RS-232 Driver
U17	I16-0008-000	Integrated Circuit, RS-422 Driver
U18	I17-0003-000	Integrated Circuit, RS-422 Receiver
U21	I17-0001-000	Integrated Circuit, RS-232 Receiver
XU7	J77-0008-005	Socket, 24 pin
VR1	I12-0006-012	Regulator, +12 V
VR2	IC-0441	Regulator, +5 V
VR3	I12-0010-012	Regulator, -12 V
Y1	Y15-0002-000	Crystal, 11000 MHz
Y2	Y15-0003-000	Crystal, 5.0688 MHz

\*When ordering this PROM, refer to the number on the sticker over the PROM

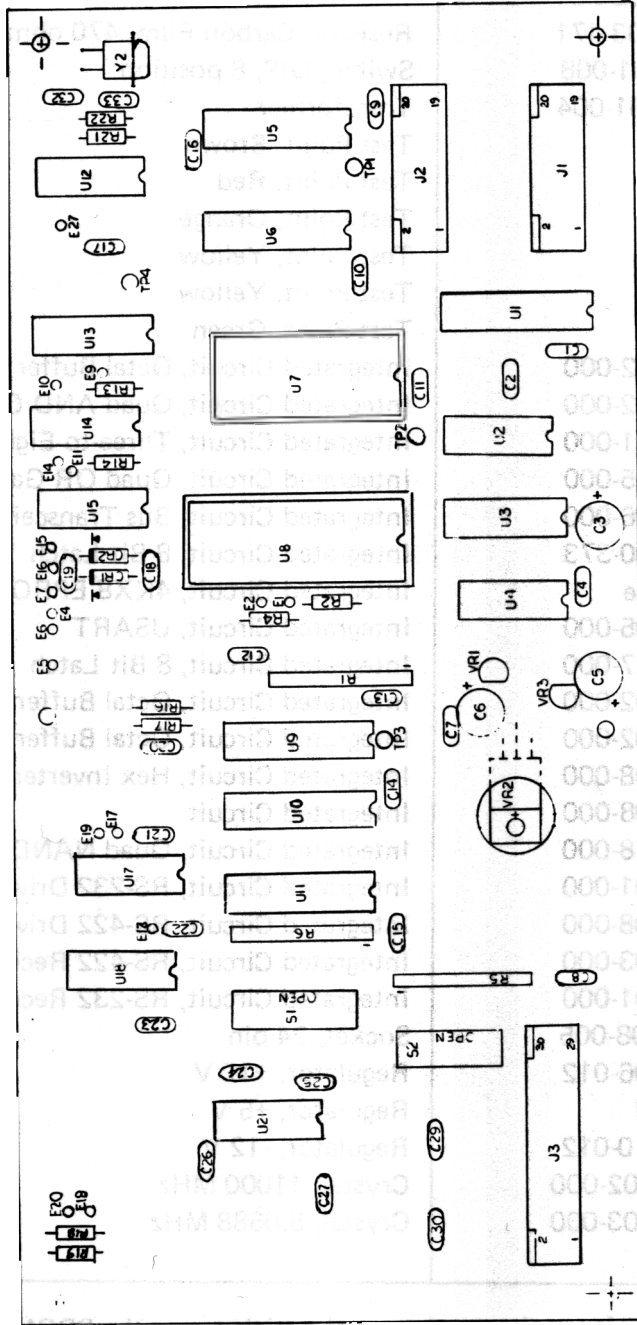
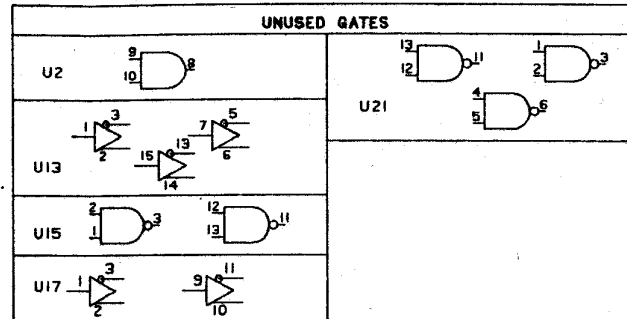


Figure 1. Remote Control Assembly A17 Component Location Diagram (10073-6200)

NOTE: UNLESS OTHERWISE SPECIFIED:

- PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
- ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
- ALL CAPACITOR VALUES ARE IN MICROFARADS.
- VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

U2 74LS08  
 U4 74LS32  
 U12 74LS04  
 U13 26LS31  
 U14 74LS00  
 U15 MC1489  
 U17 26LS31  
 U18 26LS33  
 U21 MC1489  
 U22 MC4558

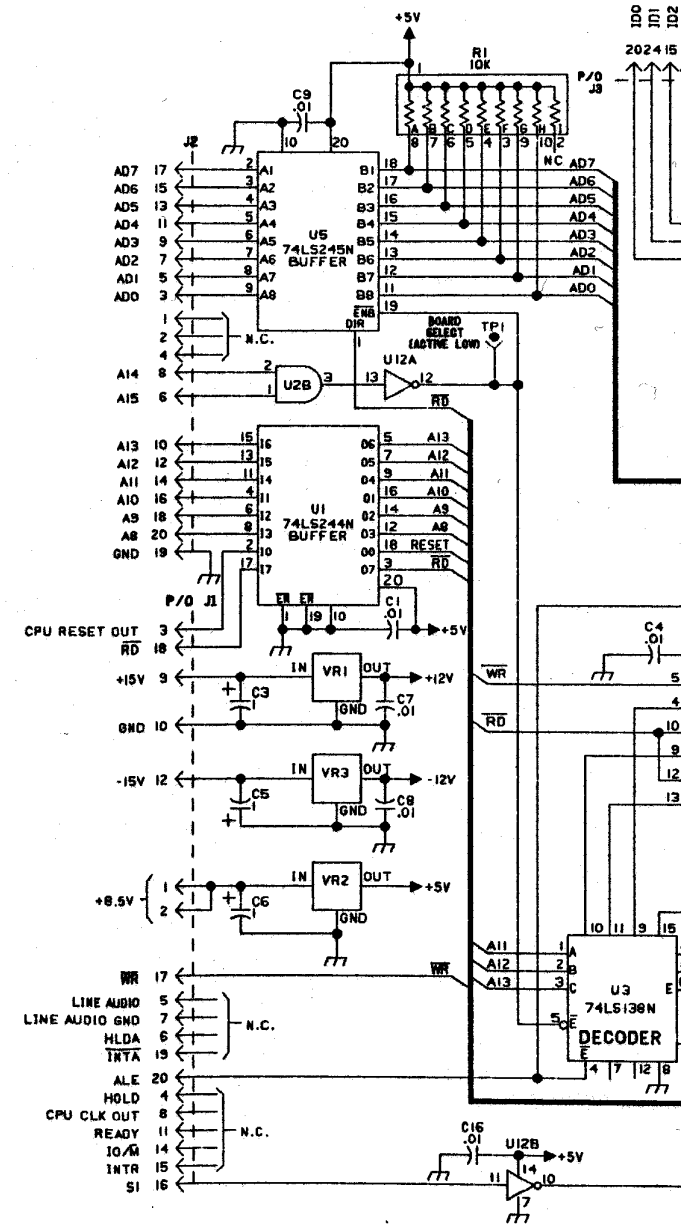


JUMPER SELECTION OF INTERFADE		
SELECTED INTERFACE	JUMPER CONFIGURATION	
RS-232-C INTERFACE	RS-232-C Tx	
	E27 TO E11	JUMPERED
	E14 TO E16 E16 TO E16	JUMPERED OPEN
RS-232-C Rx		
E6 TO E4	JUMPERED	
E5 TO E4	OPEN	
E7 TO E4	OPEN	
E8 TO E4	OPEN	
MIL-STD-188C INTERFACE	MIL-STD-188C Tx	
	E15 TO E16	JUMPERED
	E14 TO E16 E27 TO E11	OPEN JUMPERED
MIL-STD-188C Rx		
E7 TO E4	JUMPERED	
E5 TO E4	OPEN	
E6 TO E4	OPEN	
E8 TO E4	OPEN	

JUMPER SELECTION OF INTERFADE		
SELECTED INTERFACE	JUMPER CONFIGURATION	
RS-422 INTERFACE	RS-422 Tx	
	E5 TO E4	JUMPERED
	E6 TO E4 E7 TO E4	OPEN OPEN
RS-422 Rx		
E5 TO E4	JUMPERED	
E6 TO E4	OPEN	
E7 TO E4	OPEN	
FSK MODEM	MODEM Tx	
	E27 TO E12	JUMPERED
	E8 TO E4 E5 TO E4 E6 TO E4 E7 TO E4	JUMPERED OPEN OPEN OPEN
MODEM Rx		
E8 TO E4	JUMPERED	
E5 TO E4	OPEN	
E6 TO E4	OPEN	
E7 TO E4	OPEN	

NOTE:  
 FOR NORMAL OPERATION  
 E1 TO E2 LEFT OPEN.  
 CONNECT E1 TO E2 FOR  
 MODEM OUTPUT ADJUSTMENT.

JUMPER SELECTION OF INTERFACE		
MODEM HYBRID	JUMPER CONFIGURATION	
U.S. ANSWER	TRANSMIT HYBRID	
	E21 TO E22	JUMPERED
RECEIVE HYBRID		E26 TO E24 JUMPERED
U.S. ORIGINATE	TRANSMIT HYBRID	
	E26 TO E22	JUMPERED
RECEIVE HYBRID		E21 TO E24 JUMPERED



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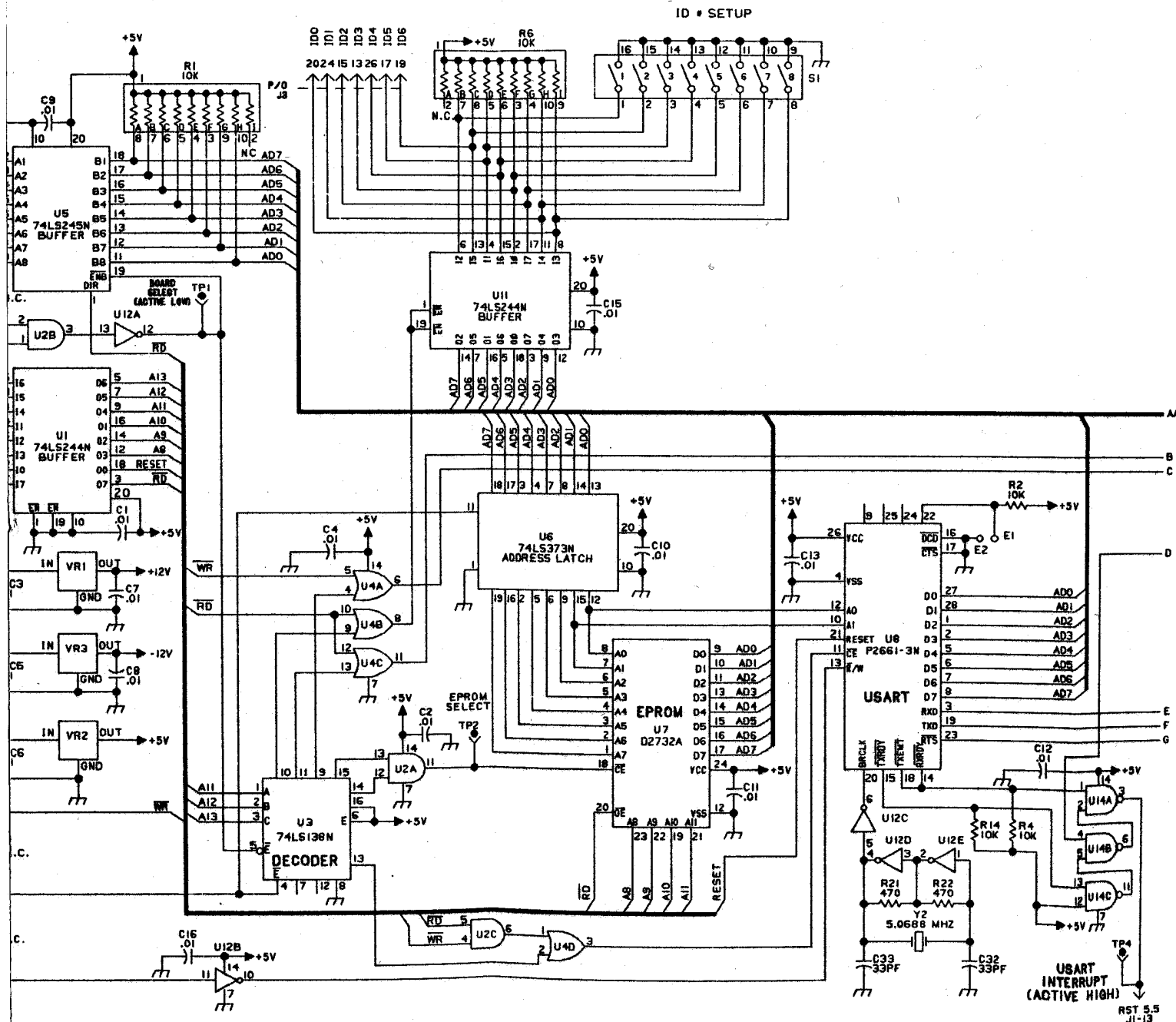


Figure 2. Remote Control Assembly A17  
Schematic Diagram (10073-6201)  
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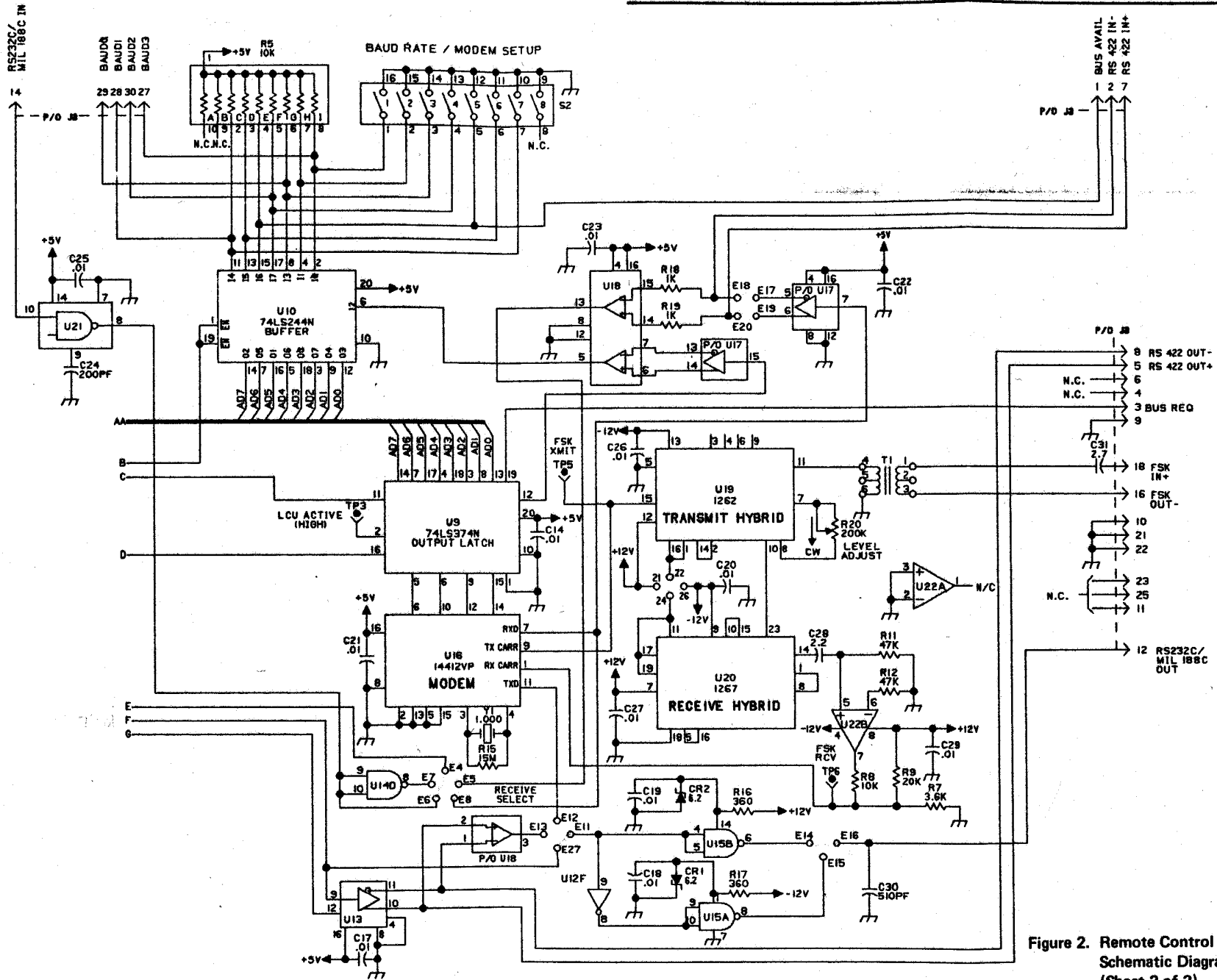


Figure 2. Remote Control Assembly A17  
Schematic Diagram (10073-6201)  
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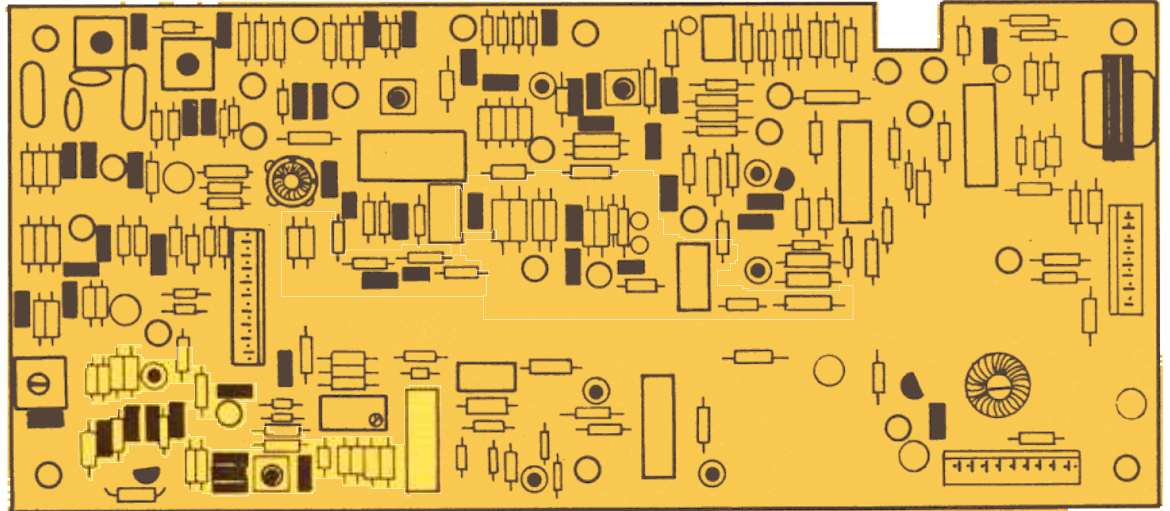
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**INDEPENDENT SIDEBAND  
(ISB) ASSEMBLY  
(A18 ASSEMBLY)**





# **INDEPENDENT SIDEBAND (ISB) ASSEMBLY (A18 ASSEMBLY)**

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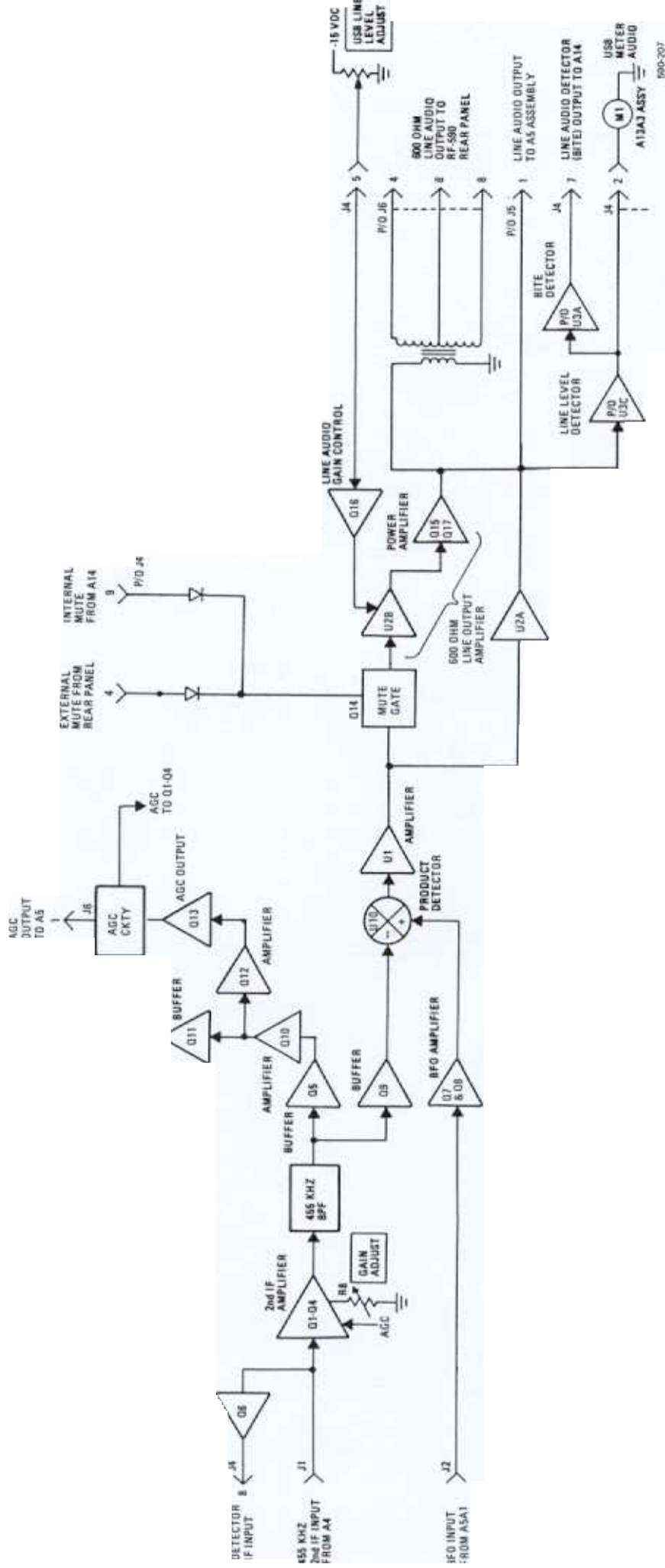
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SB Assembly A18 Functional Block Diagram

## 1 GENERAL DESCRIPTION

The ISB IF/Audio Assembly (10073-6350) duplicates the parts of the IF/Audio Assembly (10073-5410 and 10073-5450) required for independent sideband (ISB) operation. Specifically, it includes:

- 455 kHz IF Amplifier
- Product detector
- Line audio output
- Signal monitoring

## 2. INTERFACE CONNECTIONS

Table details the various input/output connections and other relevant data for:

- J4 – Interconnect with A14 Control Assembly
- J5 – Interconnect with A5 IF/Audio Assembly
- J6 – Interconnect with RF-590 Rear Panel

**Table 1 A18 ISB Assembly Interface Connections**

Connector	Function	Characteristics
J1	IF Input	455 kHz, -97/-5 dBm, 50 ohms
J2	BFO Input	455 kHz, 0 dBm, 50 ohms
J3	ISB Output	455 kHz, -7 dBm (under AGC control), 50 ohms
J4-1	ISB AGC Meter	ISB (LSB) signal strength
J4-2	ISB Audio Meter	ISB (LSB) line audio level
J4-3	Index key	
J4-4	External mute	+5 Vdc = mute
J4-5	ISB (LSB) Line Level Adjust	0 to -15 Vdc
J4-6	AGC BITE output	Typically 1.5 Vdc during BITE test
J4-7	Detected Line Audio	

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Table 1. A18 ISB Assembly Interface Connections (Cont.)

Connector	Function	Characteristics
J4-8	Detected IF Input (BITE)	
J4-9	Internal Mute	+5 Vdc = mute
J4-10	Spare	
J5-1	ISB (LSB) Audio Output	To volume potentiometer
J5-2	ISB (LSB) AGC Output	To IF/Audio AGC circuit
J5-3	Medium AGC	+5 Vdc = selected
J5-4	Fast AGC	+5 Vdc = selected
J5-5	AGC ON/OFF	+5 Vdc = AGC off
J5-6	RF gain	0 to +12 Vdc
J5-7	Index key	
J5-8	-15 Vdc	
J5-9	+15 Vdc	
J5-10	Spare	
J6-1	AGC output	0 to +6 Vdc
J6-2	Spare	
J6-3	Index key	
J6-4	Line audio	
J6-5	AGC dump	
J6-6	Line audio center tap	
J6-7	External AGC input	0 to +6 Vdc
J6-8	Line audio	

### 3. A18 CIRCUIT DESCRIPTIONS

#### 3.1 455 kHz Second IF Amplifier Chain

Low level signals at 455 kHz from IF Filter Assembly A4 enter the A18 assembly at coax connector J1. At this point it goes to both the input of the IF amplifier and the input BITE detector. The BITE detector consists of Q6 and its associated components. Q6 is an amplifier with 26 dB of gain that feeds a diode detector consisting of CR4, CR5, R32, and C27. CR6 is a 4.7 volt Zener diode that protects the BITE circuitry against overvoltage. This detector serves to check the output of the IF Filter board and the input to the IF/AF board.

Q1 is a grounded gate FET amplifier that is the input stage to the IF strip amplifier, and has approximately 20 dB of gain. Q2, Q3, and Q4 are common emitter amplifiers with an overall gain of 46 dB  $\pm$ 6 dB. This 12 dB gain adjustment is available at R8, and allows the user to trim the overall gain of the IF strip to its desired value.

Receiver Automatic Gain Control (AGC) of the IF strip is accomplished through the use of PIN diodes CR1, CR2, and CR3. A negative voltage applied to the IF AGC line (TP2) forward biases the PIN diodes and decreases the gain of the IF strip by decreasing the load impedance of each stage. Normal receiver operation requires 80 dB of available gain reduction in the strip, which is accomplished with approximately -3.0 volts on the IF AGC line.

L3, L4, C17, C18, and C19 form a bandpass filter which is adjusted during alignment to be centered at 455 kHz. This filter has approximately 9 dB of insertion loss for an overall gain to TP1 of 56 dB. The output of this filter drives Q5, (an emitter follower that buffers the rest of the IF strip) and Q9 (a dual gate MOSFET that is the input to the product detector).

Q5 serves as a buffer to provide inputs to Q10 (IF output gain stage). Q10 is a common emitter amplifier that has 30 dB of gain to provide the high level IF output, and drive amplifier Q12. Q11 is an emitter follower that buffers the high level IF output, nominally -7 dBm. Resistor R61 serves to set the IF output impedance at 50 ohms at J3. This output is then routed to rear panel connector J2 and is referred to as the ISB output. Overall IF strip gain to the IF output is nominally 80 dB. Q12 is a common emitter amplifier with 11 dB of gain that drives Q13 (the AGC detector).

#### 3.2 Product Detector

Sideband signals are demodulated using a mixer as a product detector. The 455 kHz input to the mixer RF port is buffered through dual gate MOSFET Q9. LO input is 455 kHz at 0 dBm. Q7 is a buffer that drives Q8. Q8 provides 10 dB of gain to 50 ohm matching network R42, R43, R44, which in turn provides 7 dBm of LO drive to U7. LO leakage back into the IF chain is prevented by the 40 dB LO to RF isolation of U7 as well as the high reverse isolation of buffer Q8. Sideband inversion occurs in the mixing process. Typically audio output level of 2.5 mVrms at the U7 IF port is boosted to approximately 150 mVrms by amplifier U1.

### 3.3 Audio Output Circuitry

The 600 ohm line audio output at J6 (pins 4, 6, and 8) is driving long lines. This output is the secondary of transformer T2 and along with the center tap it's available at both the rear panel terminal strip TB1 and D connector J7.

The gain of the output amplifier is adjusted by a 20 turn trim potentiometer at the front panel meter. The output level in dBm 600 ohms may be read from the meter to ease adjustment.

The output amplifier is a FET input, low noise, wideband op amp (U5A) with a complementary current buffer Q15 and Q17. Gain control is accomplished by varying the gate bias on FET Q16. Q16 is configured as a voltage variable resistor and acts as the shunt leg in the amplifier feedback network. Total gain control range is 30 dB from -20 dBm to +10 dBm. The two endpoints can be set independently. The minimum gain is controlled by resistor R82 which is in parallel with Q14. The maximum gain is set by the minimum on resistance of Q14.

The current buffer output stage of this amplifier is formed by Q15 and Q17, a class AB complementary amplifier. The 600 ohm output impedance is set by resistor R85 whose 180 ohm value is transformed to 600 ohms by the 1.82:1 ratio of T2.

A buffered single ended line output to the processor is available at J5-1. The output of Q15 and Q17 also drives the precision half-wave detector (U3C) that provides the ISB AF meter and line audio detector BITE outputs. This circuit is a precision wideband, temperature compensated detector that provides meter drive through R91. The value of R91 is chosen so that the meter reads calibrated line output level in dBm 600 ohms. R93 provides a discharge path for C60 when the meter is not in circuit. There is also a buffered version of the peak detector output available for the line audio detector BITE line to the processor. A 4.7 volt Zener diode (CR20) provides overvoltage protection for the BITE circuitry.

### 3.4 AGC Circuit Operation

Refer to paragraph 7 of the A5 (IF/Audio/AGC) section of the RF-590 manual for a discussion of AGC circuit operation. The circuitry is identical except for the portion that produces the RF AGC output.

## 4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests are performed with the assembly connections in normal contact, unless otherwise specified.

### 4.1 Second IF Chain Alignment

Perform the following procedure to align the second IF chain.

- a. Connect equipment as shown in figure 1. Set the signal generator to 456.5 kHz, 10 uV. Set spectrum analyzer to 455 kHz.



590-208

**Figure 1. Second IF Chain Alignment**

- b. Set RF-590 controls as follows:
  - Mode to ISB
  - AGC to OFF
  - RF Gain to fully clockwise (cw)
- c. Monitoring the spectrum analyzer at 455 kHz, adjust L3 and L4 for maximum output. (adjustments may be some what interactive, so repeat as necessary.)
- d. Adjust R8 for -7 dBm (100 mVrms) at J3. Test is complete.

**5. PARTS LIST**

Table 2 is a comprehensive parts lists of all replaceable components in ISB Assembly A18. When ordering parts from the factory, include a full description of the part. Use figure 2, ISB Assembly A18 Component Location Diagram, to identify parts.

**6. SCHEMATIC DIAGRAM**

Figure 3 is the ISB A18 schematic diagram.

**Table 2. ISB Assembly A18 Maintenance Parts List (PL 10073-6350)**

Ref. Desig.	Part No.	Description
C1	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C2	CK06BX474M	Capacitor
C3	CK06BX474M	Capacitor
C4	CK06BX474M	Capacitor
C5	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C6	CK06BX474M	Capacitor



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Table 2. ISB Assembly A18 Maintenance Parts List (PL 10073-6350) (Cont.)

Ref. Desig.	Part No.	Description
C7	CK06BX474M	Capacitor
C8	CK06BX474M	Capacitor
C9	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C10	CK06BX474M	Capacitor
C11	CK06BX474M	Capacitor
C12	C26-0025-220	Capacitor
C13	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C14	CK06BX474M	Capacitor
C15	CK06BX474M	Capacitor
C16	CM04FD181J03	Capacitor, Mica, 180 pF, 300
C17	CM06FD112J03	Capacitor
C18	CM04ED680J03	Capacitor
C19	CM06FD122J03	Capacitor
C20	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C21	CK06BX474M	Capacitor
C22	C26-0025-220	Capacitor
C23	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C24	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C25	CK06BX474M	Capacitor
C26	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C27	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C29	CK06BX474M	Capacitor
C30	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C31	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C32	CK06BX474M	Capacitor
C33	CK06BX474M	Capacitor
C34	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C35	CK05BX102M	Capacitor
C36	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C37	CK06BX474M	Capacitor
C38	CK06BX474M	Capacitor
C39	CK06BX474M	Capacitor
C40	CK06BX102M	Capacitor
C41	C26-0025-470	Capacitor
C42	C26-0025-470	Capacitor
C43	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C44	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C45	CK06BX474M	Capacitor
C46	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C47	CK06BX474M	Capacitor
C48	CK06BX474M	Capacitor

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Table 2. ISB Assembly A18 Maintenance Parts List (PL 10073-6350) (Cont.)

Ref. Desig.	Part No.	Description
C49	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C50	CK06BX474M	Capacitor
C51	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C52	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C53	CK05BX102M	Capacitor
C54	C26-0025-339	Capacitor
C55	C26-0025-339	Capacitor
C56	C26-0025-339	Capacitor
C57	CK06BX474M	Capacitor
C58	CK06BX474M	Capacitor
C59	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C60	C26-0025-339	Capacitor
C61	C25-0003-209	Capacitor
C62	CK06BX104M	Capacitor, .1 uF, 100 Vdc
C63	CK06BX104M	Capacitor, .1 uF, 100 Vdc
CR1	D12-0008-001	Diode
CR2	D12-0008-001	Diode
CR3	D12-0008-001	Diode
CR4	1N4454	Diode
CR5	1N4454	Diode
CR6	1N4732A	Diode, 1N4732A, 4.7 U, Zener
CR7	1N4454	Diode
CR8	1N4454	Diode
CR9	1N4454	Diode
CR10-CR19	1N4454	Diode
CR20	1N4732A	Diode, Zener, 1N4732A, 4.7 U
CR21	1N4454	Diode
CR22	1N4732A	Diode, Zener, 1N4732A, 4.7 U
CR23-CR30	1N4454	Diode
J1-J3	J-0031	Connector, Coax
J4,J5	J46-0032-010	Header, 10 pin
J6	J46-0032-008	Connector, Amp, 8 pin
L1,L2	MS75085-19	Inductor
L3,L4	L11-0004-037	Inductor
L5,L6	MS75085-19	Inductor
L7	MS75085-18	Inductor
L8	MS75085-11	Choke
L9-L11	MS75085-19	Inductor
L12	10073-7029	Inductor
Q1	Q35-0001-001	Transistor

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Table 2. ISB Assembly A18 Maintenance Parts List (PL 10073-6350) (Cont.)

Ref. Desig.	Part No.	Description
Q2	2N2222	Transistor, SI, NPN, GP
Q3	2N2222	Transistor, SI, NPN, GP
Q4	2N2222	Transistor, SI, NPN, GP
Q5	2N2222	Transistor, SI, NPN, GP
Q6	2N2222	Transistor, SI, NPN, GP
Q7	2N2222	Transistor, SI, NPN, GP
Q8	2N2222	Transistor, SI, NPN, GP
Q9	Q-0325	Transistor
Q10	2N2222	Transistor, SI, NPN, GP
Q11	2N2222	Transistor, SI, NPN, GP
Q12	2N2222	Transistor, SI, NPN, GP
Q13	2N2907	Transistor, PNP
Q14	2N2222	Transistor, SI, NPN, GP
Q15	2N2222	Transistor, SI, NPN, GP
Q16	2N4091	Transistor
Q17	2N2907	Transistor, PNP
Q18	2N2222	Transistor, SI, NPN, GP
Q19	2N2222	Transistor, SI, NPN, GP
Q20	2N2222	Transistor, SI, NPN, GP
Q21	2N2907	Transistor, PNP
R1	R65-0003-181	Resistor, Carbon Film
R2	R65-0003-561	Resistor, Film
R3	R65-0003-101	Resistor
R4	R65-0003-102	Resistor, Carbon Film
R5	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R6	R65-0003-512	Resistor, Carbon Film, 5.1 K, 1/4 W
R7	R65-0003-200	Resistor
R8	R40-0008-101	Resistor
R9	R65-0003-431	Resistor, Carbon Film
R10	R65-0003-102	Resistor, Carbon Film
R11	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R12	R65-0003-512	Resistor, Carbon Film, 5.1 K, 1/4 W
R13	R65-0003-221	Resistor
R14	R65-0003-390	Resistor, Film
R15	R65-0003-431	Resistor, Carbon Film
R16	R65-0003-101	Resistor
R17	R65-0003-102	Resistor, Carbon Film
R18	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R19	R65-0003-512	Resistor, Carbon Film, 5.1 K, 1/4 W
R20	R65-0003-561	Resistor, Film

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**RF COMMUNICATIONS**

Table 2. ISB Assembly A18 Maintenance Parts List (PL 10073-6350) (Cont.)

Ref. Desig.	Part No.	Description
R21	R65-0003-101	Resistor
R22	R65-0003-361	Resistor
R23	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R24	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R25	R65-0003-271	Resistor
R26	R65-0003-102	Resistor, Carbon Film
R27	R65-0003-512	Resistor, Carbon Film, 5.1 K, 1/4 W
R28	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R29	R65-0003-561	Resistor, Film
R30	R65-0003-270	Resistor
R31	R65-0003-431	Resistor, Carbon Film
R32	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R33	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R34	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R35	R65-0003-471	Resistor, Metal Film, 470, 1/4 W
R36	R65-0003-221	Resistor
R37	R65-0003-431	Resistor, Carbon Film
R38	R65-0003-101	Resistor
R39	R65-0003-242	Resistor, Carbon Film, 1/4 W, 5%
R40	R65-0003-120	Resistor, Carbon Film, 12, 1/4 W
R41	R65-0003-101	Resistor
R42	R65-0003-301	Resistor, Carbon Film
R43	R65-0003-180	Resistor
R44	R65-0003-301	Resistor, Carbon Film
R45	R65-0003-510	Resistor, Carbon Film, 1/4 W, 5%
R46	R65-0003-102	Resistor, Carbon Film
R47	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R48	R65-0003-201	Resistor, Film
R49	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R50	R65-0003-201	Resistor, Film
R51	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R52	R65-0003-221	Resistor
R53	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R54	R65-0003-562	Resistor
R55	R65-0003-561	Resistor, Film
R56	R65-0003-433	Resistor, Carbon Film, 43 K, 1/4 W, 5%
R57	R65-0003-100	Resistor, Carbon Film, 1/4 W, 5%
R58	R65-0003-100	Resistor, Carbon Film, 1/4 W, 5%
R59	R65-0003-431	Resistor, Carbon Film
R60	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R61	R65-0003-510	Resistor, Carbon Film, 1/4 W, 5%

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**RF COMMUNICATIONS**

Table 2. ISB Assembly A18 Maintenance Parts List (PL 10073-6350) (Cont.)

Ref. Desig.	Part No.	Description
R62	R65-0003-331	Resistor, Carbon Film, 330, 1/4 W
R63	R65-0003-432	Resistor, Carbon Film
R64	R65-0003-432	Resistor, Carbon Film
R65	R65-0003-223	Resistor, Carbon Film, 1/4 W, 5%
R66	R65-0003-432	Resistor, Carbon Film
R67	R65-0003-433	Resistor, Carbon Film, 43 K, 1/4 W, 5%
R68	R30-0008-203	Resistor, Variable, 20 K
R69	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R70	R65-0003-561	Resistor, Film
R71	R65-0003-512	Resistor, Carbon Film, 5.1 K, 1/4 W
R72	R65-0003-161	Resistor
R73	R65-0003-561	Resistor, Film
R74	R65-0003-473	Resistor, Carbon Film, 1/4 W, 5%
R75	R65-0003-101	Resistor
R76	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R77	R65-0003-513	Resistor, Carbon Film, 1/4 W, 5%
R78	R65-0003-512	Resistor, Carbon Film, 1/4 W, 5%
R79, R80	R65-0003-104	Resistor, Carbon Film, 100 K, 1/4 W, 5%
R81	R65-0003-511	Resistor, Carbon Film, 510, 1/4 W
R82	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R83	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R84	R65-0003-910	Resistor, Film, 910, 1/4 W, 5%
R85	R65-0003-181	Resistor, Carbon Film
R86	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R87	R65-0003-910	Resistor, Film, 910, 1/4 W, 5%
R88	R65-0003-473	Resistor, Carbon Film, 1/4 W, 5%
R89	R65-0003-152	Resistor, Film, 1.5 K, 1/4 W, 5%
R90	R65-0003-244	Resistor
R91	R65-0003-273	Resistor
R92	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R93	R65-0003-302	Resistor, Carbon Film, 3 K, 1/4 W, 5%
R95	R65-0003-512	Resistor, Carbon Film, 5.1 K, 1/4 W
R96	R65-0003-101	Resistor
R97	R65-0003-471	Resistor, Metal Film, 470, 1/4 W
R98	R65-0003-101	Resistor
R99	R75-0001-002	Resistor
R100	R65-0003-473	Resistor, Carbon Film, 1/4 W, 5%
R101	R65-0003-431	Resistor, Carbon Film
R102	R65-0003-473	Resistor, Carbon Film, 1/4 W, 5%
R103	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R104	R65-0003-242	Resistor, Carbon Film, 1/4 W, 5%

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Table 2. ISB Assembly A18 Maintenance Parts List (PL 10073-6350) (Cont.)

Ref. Desig.	Part No.	Description
R105	R65-0003-474	Resistor, Carbon Film, 1/4 W, 10%
R106	R65-0003-100	Resistor, Carbon Film, 1/4 W, 5%
R107	R65-0003-473	Resistor, Carbon Film, 1/4 W, 5%
R108	R65-0003-473	Resistor, Carbon Film, 1/4 W, 5%
R109	R65-0003-473	Resistor, Carbon Film, 1/4 W, 5%
R110	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R111	R65-0003-203	Resistor, Carbon Film, 1/4 W, 5%
R112	R30-0008-202	Resistor
R113	R65-0003-683	Resistor, Carbon Film, 68 K, 1/4 W
R114	R65-0003-184	Resistor, Carbon Film, 180 K, 1/4 W, 5%
R115	R65-0003-822	Resistor, Carbon Film, 8, 1/4 W, 5%
R116	R65-0003-393	Resistor, Carbon Film, 1/4 W, 5%
R117	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
R118	R65-0003-751	Resistor, Carbon Film
R119	R65-0003-681	Resistor, Carbon Film, 680, 1/4 W, 5%
R120	R30-0008-501	Resistor
R121	R65-0003-102	Resistor, Carbon Film
R122	R65-0003-301	Resistor, Carbon Film
R123	R65-0003-102	Resistor, Carbon Film
R124	R65-0003-623	Resistor, Carbon Film, 62 KR, 1/4 W, 5%
R125	R65-0003-103	Resistor, Carbon Film, 1/4 W, 5%
T1	10073-7026	Transformer
T2	T60-0004-001	Transformer
TP1	J-0071	Test Point
TP2	J-0066	Test Point
TP3	J-0069	Test Point
TP4	J-0070	Test Point, Yellow
TP5	J-0068	Test Point, Green
TP6	J-0072	Test Point, Blue
TP7	J-0073	Test Point
TP8	J-0074	Test Point, Grey
U1	I30-0036-001	Integrated Circuit
U2	I30-0035-000	Integrated Circuit
U3	I30-0003-000	Integrated Circuit, Quad Oper. Ampl.
U4	I30-0003-000	Integrated Circuit, Quad Oper. Ampl.
U5	I30-0003-000	Integrated Circuit, Quad Oper. Ampl.
U6	I30-0003-000	Integrated Circuit, Quad Oper. Ampl.
U7	I51-0003-001	Mixer
VR1	I12-0010-005	Voltage Regulator
VR2	I12-0006-005	Integrated Circuit



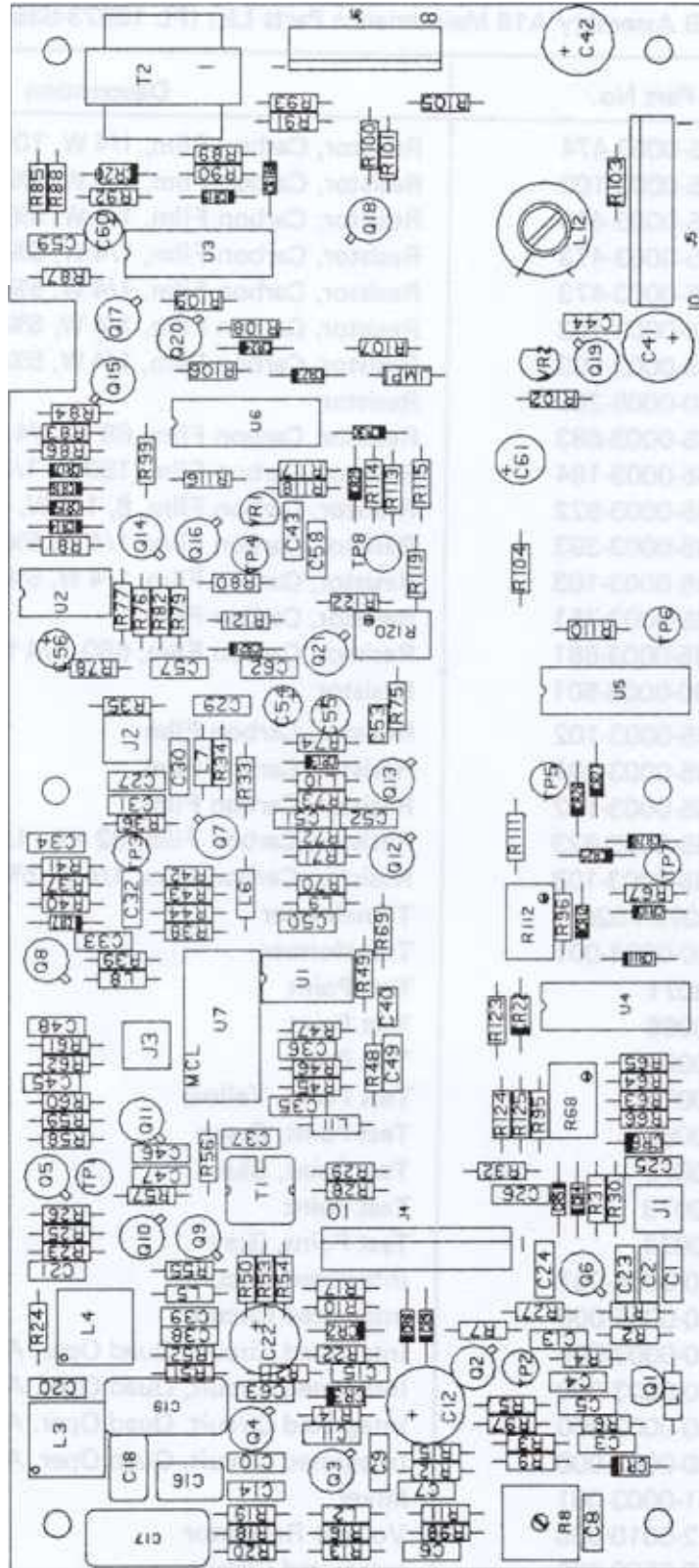


Figure 2. ISB Assembly A18 Component Location Diagram

NOTE: UNLESS OTHERWISE SPECIFIED:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.  
FOR A COMPLETE DESIGNATION, PREFIX WITH  
UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.

ALL CAPACITOR VALUES ARE IN MICROFARADS, 200V.

VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY.  
COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

⊕ = RF GND

⊕ = LOCAL GND

UNUSED GATES

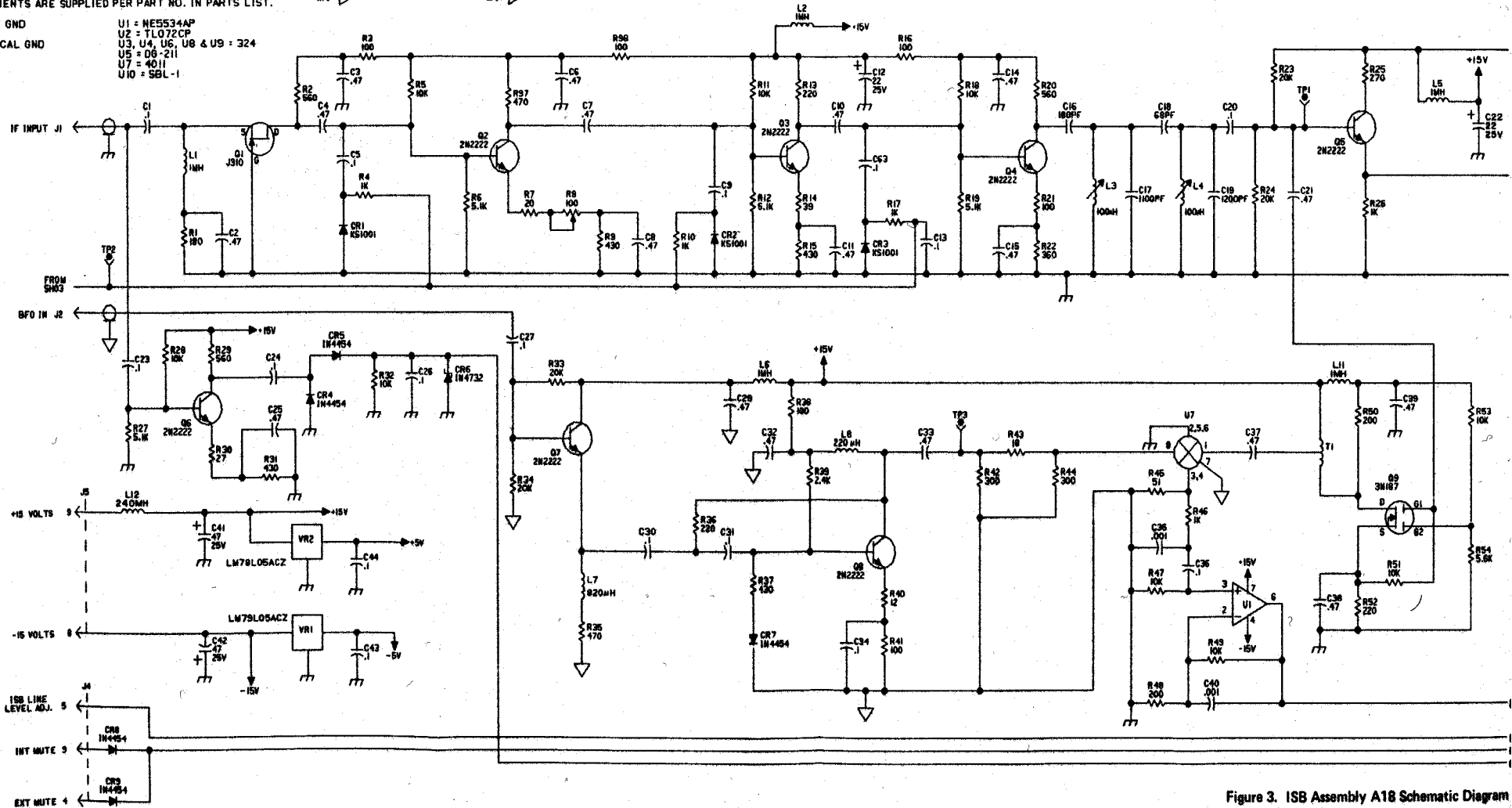
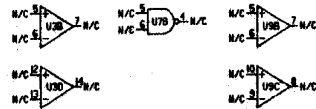


Figure 3. ISB Assembly A18 Schematic Diagram  
(Sheet 1 of 3)



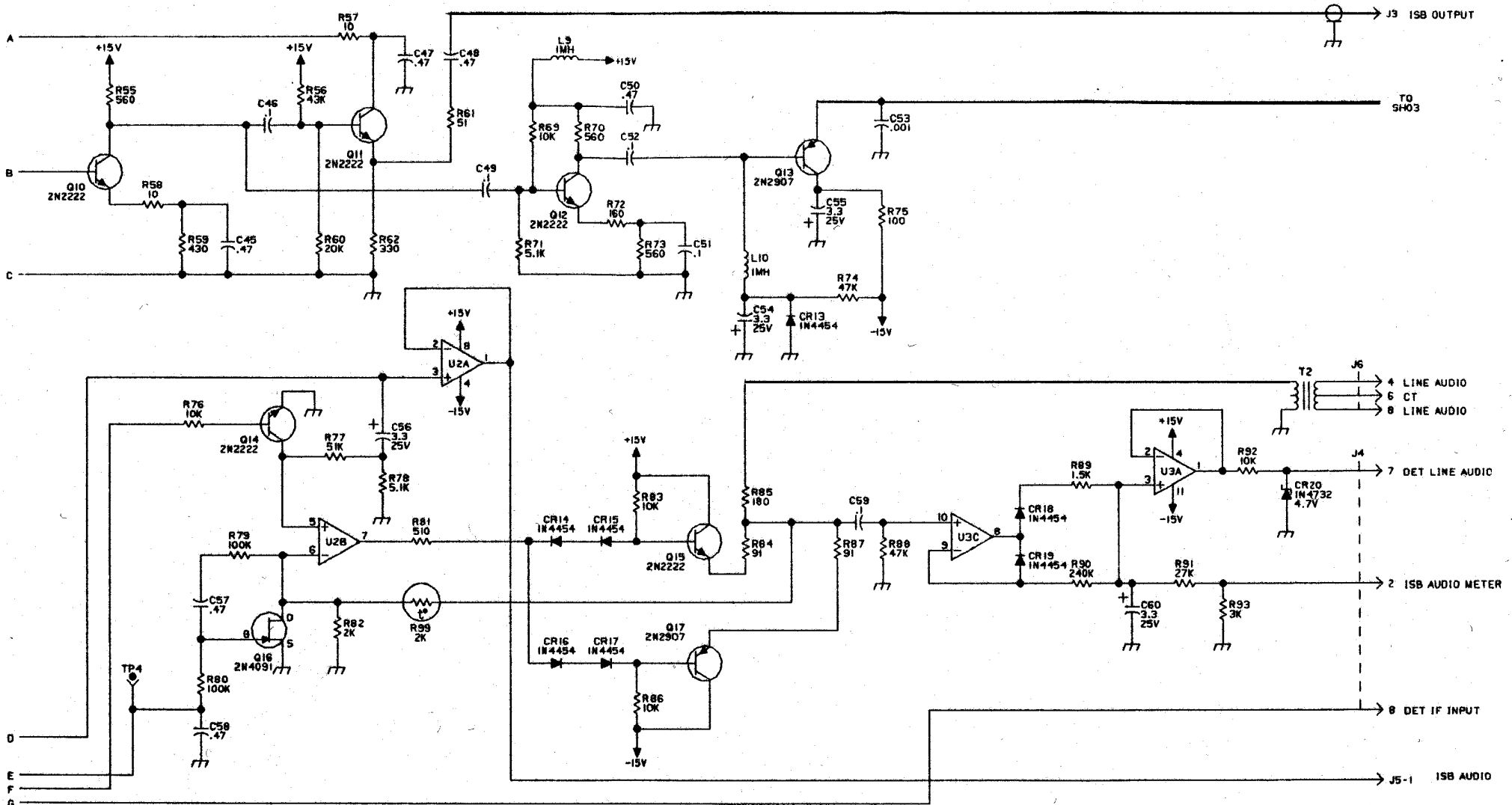
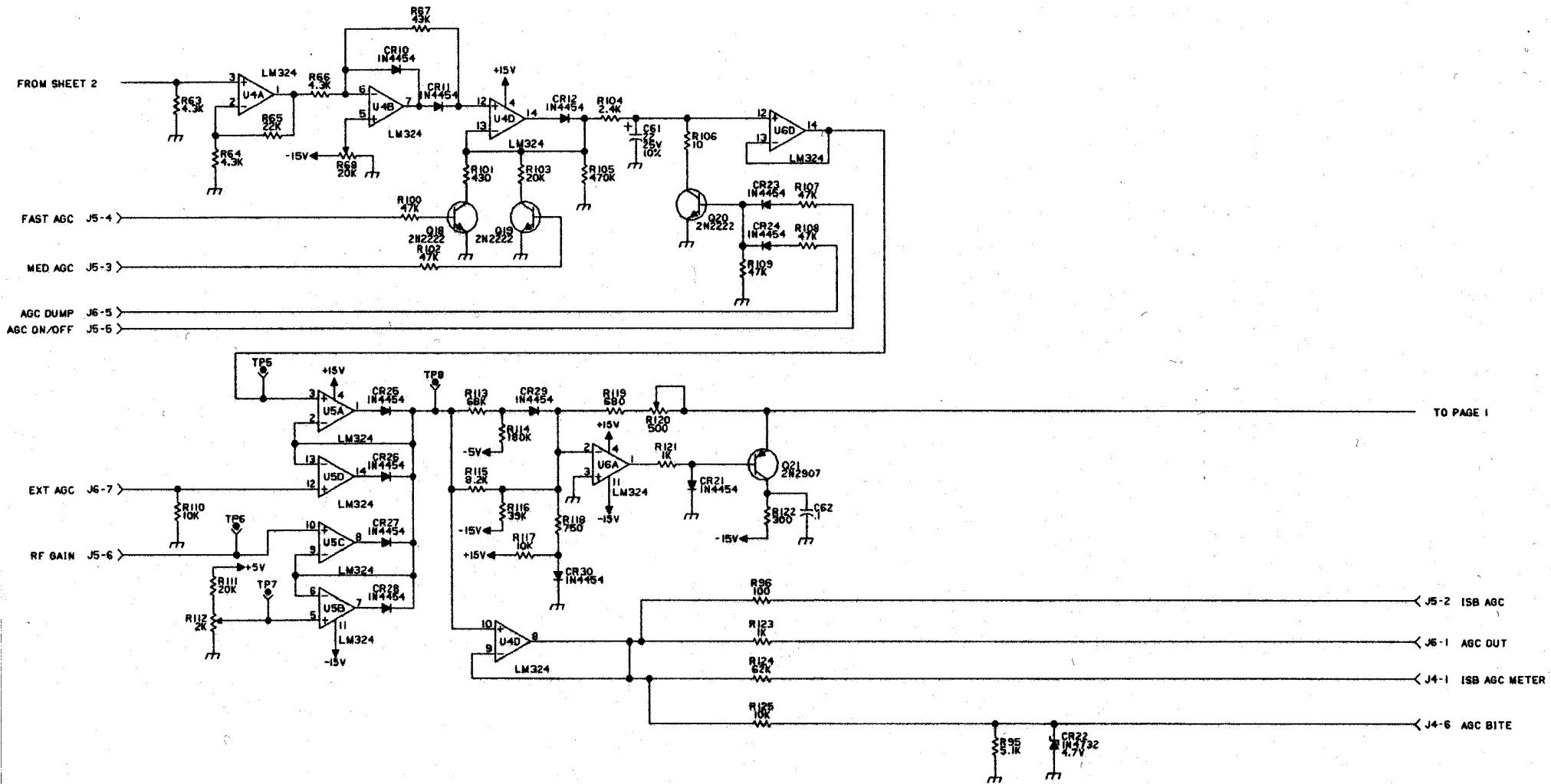


Figure 3. ISB Assembly A18 Schematic Diagram  
(Sheet 2 of 3)



TO PAGE 1

Figure 3. ISB Assembly A18 Schematic Diagram (Sheet 3 of 3)



SUPPLEMENT NUMBER: SU-10073-0019-2  
TO  
PUBLICATION NUMBER: 10073-0020A  
MARCH 1983



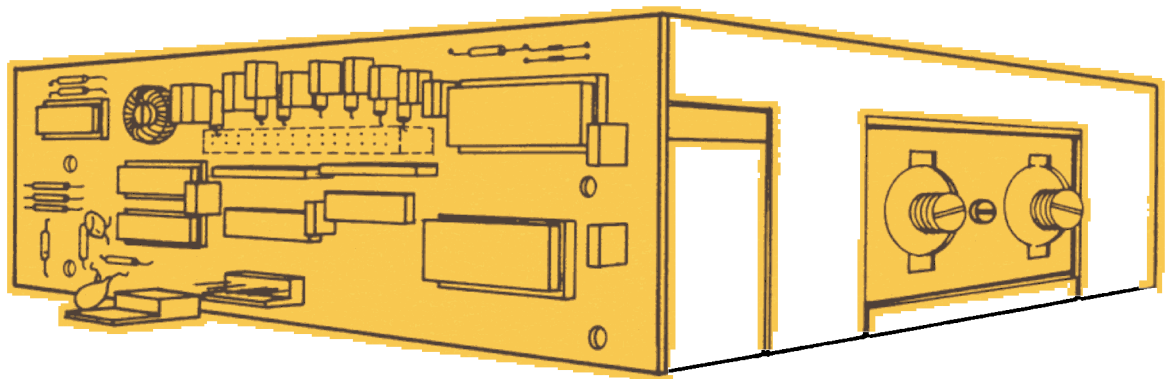
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**RF COMMUNICATIONS**

**RF-596-02**

**PRESELECTOR MODULE**

**( A19 ASSEMBLY )**



# **RF-596-02**

## **PRESELECTOR MODULE**

**( A19 ASSEMBLY )**

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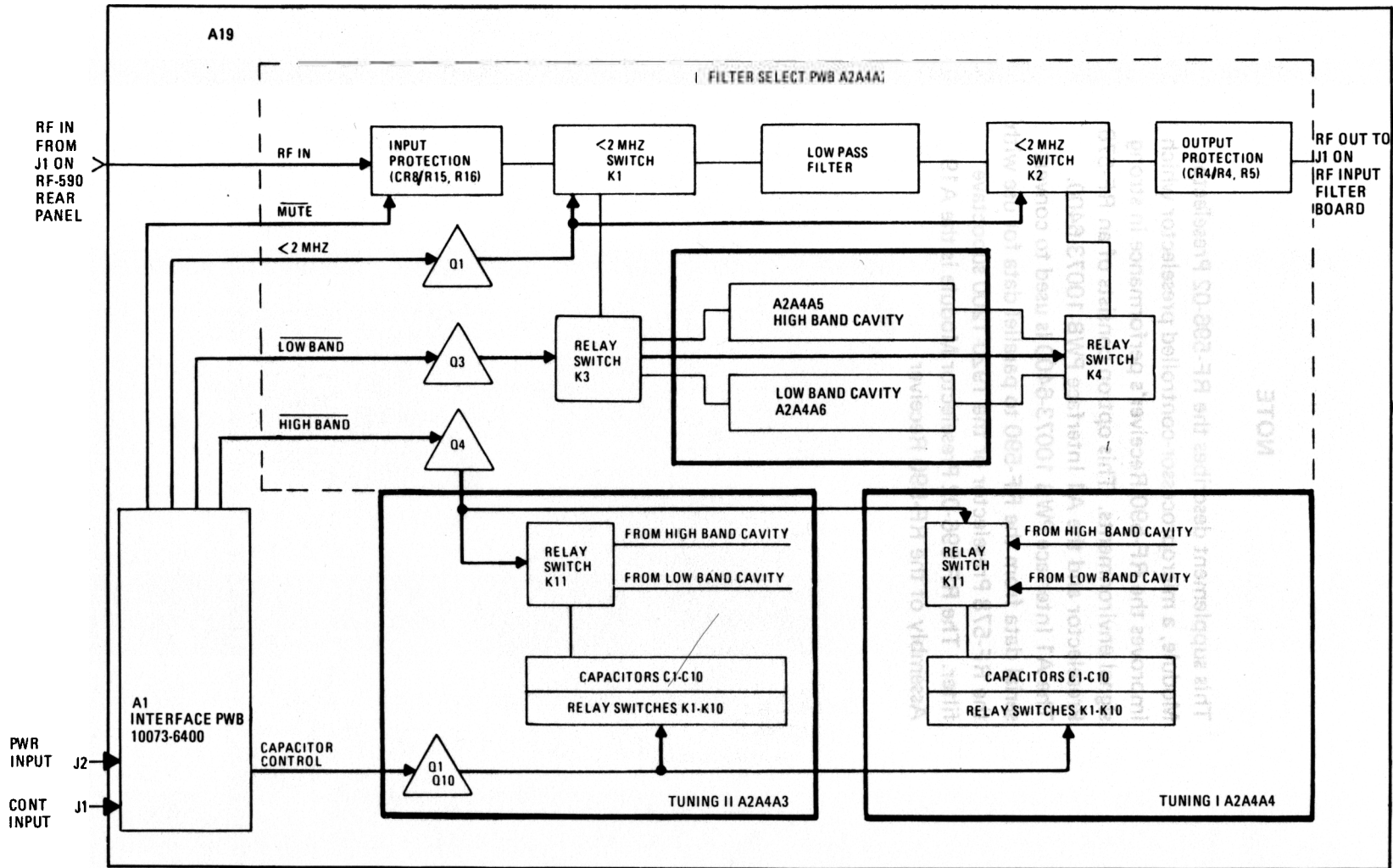
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**NOTE**

This supplement describes the RF-596-02 Preselector Module, a microprocessor-controlled preselector which improves the RF-590 Receiver's performance in strong signal environments. This option consists of an RF-578 Preselector and the A1 Interface PWB 10073-6400. The A1 Interface PWB 10073-6400 is used to convert serial data from the RF-590 to parallel data for use with the RF-578 Preselector or the 1920-1200 suboctave filter. The RF-596-02 Preselector Module is the A19 Assembly of the RF-590 Receiver.



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RF-596-02 Preselector Module (A19 Assembly) Functional Block Diagram



## 1. GENERAL DESCRIPTION

The RF-596-02 Preselector Module is a microprocessor-controlled preselector which improves the RF-590 Receiver's performance in strong signal environments. This option consists of an RF-578 Preselector and the A1 Interface PWB 10073-6400. The A1 Interface PWB 10073-6400 is used to convert serial data from the RF-590 to parallel data for use with the RF-578 Preselector or the 1920-1200 suboctave filter. Serial data is constantly clocked through shift registers U1 and U2 by the clock pulses. Only a frequency change on the RF-590 front panel causes a strobe pulse to be applied at the end of a serial word to U1 and U2. This strobe pulse causes the outputs of U1 and U2 to change to a parallel data format. The parallel output of shift registers U1 and U2 is the address that is used by EPROMS U3 and U4 to select capacitor control lines CO through C9 of the RF-578 or bands for the one-half octave filter. Figure 1 shows the location of the A1 Interface PWB on the RF-596-02 Preselector Module.

## 2. TECHNICAL CHARACTERISTICS

### Weight:

Preselector Module	2.6 pounds (1.8 kilograms)
Control PWB Assemblies	0.5 pounds (0.23 kilograms)

### Dimensions:

Preselector Module	5.31 (H) x 5.84 (W) x 2.09 (D) inches 13.49 (H) x 14.83 (W) x 5.31 (D) centimeters
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<u>Power Requirements:</u>	5 Vdc -15 Vdc
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<u>Frequency Range:</u>	0.1 to 30 MHz
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<u>Insertion Loss:</u>	4 to 6 dB
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<u>Selectivity:</u>	20 dB minimum at a frequency 10% from $f_o$
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<u>Overload Protection:</u>	On-channel - 10 Vrms nominal Off-channel - 30 Vrms nominal
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## 3. FUNCTIONAL DESCRIPTION

### 3.1 Filter Select Assembly A19A2

An RF input signal from the antenna enters the Filter Select PWB at J2, and is fed via the normally energized contacts of relay K6, to relay K1. Relays K1 and K2 are under the control of the < 2 MHz input from Interface PWB A19A1. If the receive frequency is less than 2 MHz, a low input would be present at E5. Q1 is now biased on energizing K1, K2; opening the signal path to the cavity filters; and coupling the

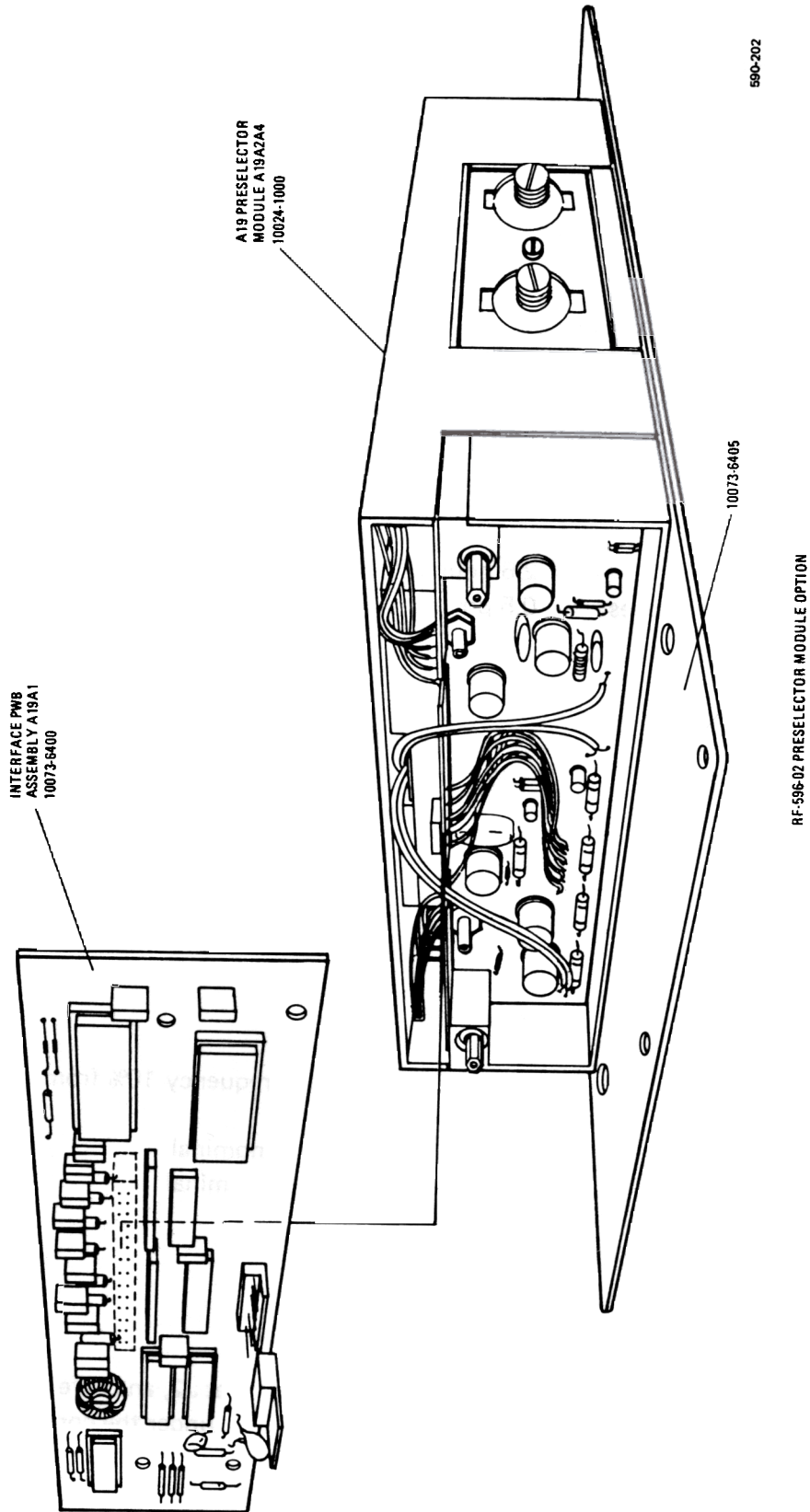


Figure 1. RF-596-02 Preselector Module Option (A19 Assembly)

RF signal via the low pass filter network C2, L3, C3, and C4, normally energized K5, to the input of Input Filter PWB A1 of the RF-590.

For a receive frequency greater than 2 MHz (as decoded by Interface PWB A19A1), Q1 is held at cut-off by R2. This keeps relays K1 and K2 deenergized. The RF signal (>2 MHz) is now passed, via the normally closed contacts of K1, to band select relay K3. Relays K3 and K4 operate in unison, under the control of A19A1. When Interface PWB A19A1 determines the receive frequency to be within the low band limits (2 MHz to 7.99 MHz), a low logic level is applied to Q3, via E1 and R10. Q3, now being forward biased, energizes relays K3 and K4, while C18, L8, and L9 serve to decouple any stray RF that may be present on the supply line. Energized relays K3 and K4 couple the RF signal to a high-Q, doubly-tuned bandpass filter, whose resonant frequency is determined by the tuning of the coils within the low band cavity assembly, and the capacitors (located on Tuning Assembly I and Tuning Assembly II) switched into the circuit by control data from A19A1. The individual filter shape is determined by several factors, which include filter tuning (capacitive and inductive) and the coil-to-coil coupling within the low band cavity. With the low band circuitry properly adjusted, each filter is designed to cover a specific frequency band with a one-half dB bandwidth of approximately 1/60 of an octave. From the low band cavity filter, the RF signal reenters the Filter Select PWB at E10, via low pass filter (C20, C21, L10, L11, and R14/L2), energized relay K4, normal K2 contacts, and energized relay K5, then is applied to the J1 RF output.

Similarly, if Interface PWB A19A1 determines the selected frequency to be 8 MHz or greater, a high logic level is applied to E1. This biases Q3 off, deenergizing relays K3 and K4. Deenergized relays K3 and K4 couple the RF signal to the high band cavity which functions in a manner similar to the low band cavity. The same groups of capacitors are used in both the high band and low band filters with any minor capacitive differences between high and low band cavities being compensated for by C21, C22 on Tuning Assembly I and C22, C23 on Tuning Assembly II. From the high band cavity, the RF signal reenters the Filter Select PWB at E12 via a low pass filter (C15, C16, L6, L7, and R11/L1), deenergized relays K4 and K2 and energized relay K5. The RF signal is then applied to the RF-590 A1 Input Filter (10073-5100). In addition, a low logic level is applied to the base of Q4, via E13 and R13, biasing Q4 on, which energizes relays K11 on Tuning Assemblies I and II of the RF-596-02 Preselector Module.

A high level, out-of-band input signal at J2 is coupled by C24 to the voltage divider network consisting of R15 and R16. This voltage, detected by CR8, is seen as a negative voltage at the base of Q5. This increases proportionally to the RF input level. At a level of 30 Vrms, the voltage developed across CR8 becomes sufficiently negative to bias Q6 off, deenergizing K6 and opening the antenna input path. Voltage divider network R4, R5, and detector CR4 develop a negative voltage proportional to the in-band signal level present at C7. At an in-band signal level of 10 Vrms or greater, the negative voltage at the base of Q2 becomes sufficient to bias Q2 off, deenergizing relay K5 and shorting the RF input to the receiver.

### 3.2 Tuning Assemblies I and II (A2A4A4, A2A4A3)

Tuning Assembly I (A2A4A4), and Tuning Assembly II (A2A4A3) are similar in design and function, with the exception that Tuning Assembly II contains the ten relay driver transistors (Q1 through Q10). Each PWB assembly is comprised of ten capacitor sections with their associated control relays (K1 through K10), and a high/low band select relay K11.

Refer to the Tuning Assemblies schematic diagram for the following discussion. Relay driver transistors Q1 through Q10, on Tuning Assembly II, are normally reversed biased by a 5 Vdc level supplied by Interface PWB A19A1. The Interface PWB A19A1 decodes the serial data stream from the RF-590 into a parallel word that is used to supply band information to C0 through C9. Active control signals appear at the inputs of Tuning Assembly II as low logic levels, while inactive control lines are identified by the presence of the 5 Vdc on the Tuning Assembly II inputs.

For the following discussion, assume that the receiver's front panel frequency select switches are set to 2.15 MHz. The frequency and band information for 2.15 MHz contained in the RF-590 frequency code is decoded by A19A1, which in turn presents a series of low (active) control inputs to Tuning Assembly II. In this example, all control inputs are low (active), with the exception of A3J1-2 (C8) which remains high (inactive). This low level at  $\overline{C0}$  through  $\overline{C7}$  and  $\overline{C9}$ , forward biases Q1 through Q7, Q9, and Q10, while the high level at A3J1-2 ( $\overline{C8}$ ) holds Q8 at cut-off. Transistors Q1 through Q7, Q9, and Q10 are now forward biased and energize their respective control relays (K1 through K10) on Tuning Assembly II, and via A3P1 and A3P2, control relays (K1 through K10) on Tuning Assembly I. Energized control relays K1 through K7, K9, and K10 switch their associated capacitors into the signal path from the cavity filter, in this case, the low band cavity.

In addition, since the frequency selected (2.15 MHz) is within the low band range, relays K11 on Tuning Assemblies I and II will be deenergized, connecting the capacitor network to the low band cavity.

**CAUTION**

The trimmer capacitors located on Tuning Assemblies I and II and adjustments on the cavity assemblies have been set for optimum response characteristics at the desired frequencies, and should not require any further adjustments under normal use. Severe degradation in receiver performance will result if attempts are made to adjust these capacitors without the use of proper test equipment (i.e., H.P. Spectrum Analyzer Model 8553B, equipped with Model 8444A Tracking Generator, or equivalent).

### 3.3 Interconnect Schematic

An interconnect schematic for the RF-596-02 Preselector Module is found at the end of this section.

## 4. MAINTENANCE

### 4.1 General

The RF-596-02 Preselector Module requires no periodic lubrication or adjustments of a mechanical nature. Under normal operation, no further adjustment to the high band cavities, low band cavities, or to the variable capacitors on the two Tuning Assemblies should be required.

## 4.2 Troubleshooting Procedure

After localizing the receiver's malfunction to the RF-596-02 Preselector Module, it must be further determined which assembly within the module itself is the cause of the problem. To localize faults within the RF-596-02 Preselector, seven different frequencies can be used to test the band selection relays and the tuning capacitors as shown in tables 1 and 2.

**Table 1. Filter Select Assemblies I and II Troubleshooting Aid**

Frequency MHz	Relays											
	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	A3P1-7	A4P2-2
	Terminals											
	E1	E11	E2	E8	E7	E4	E5	E6	E9	E10	A3K11	A4K11
2.150	L	L	L	L	L	L	L	H	L	L	H	H
2.90	X	X	X	X	X	X	X	L	H	X	X	X
7.890	H	H	H	H	H	H	H	H	H	H	X	X
8.0	X	X	X	X	X	X	X	X	X	X	L	L

**Notes:**

L = Low Logic Level/Relay Energized

H = High Logic Level/Relay Deenergized

X = Don't Care

Low Level to Activate Control Functions

**Table 2. Filter Select PWB A2A4A2 Frequency vs. Relay Operation**

Frequency MHz	Relays	
	K1, K2	K3, K4
1.5	Closed	Open
2.0	Open	Closed
8.0	Open	Open

When using tables 1 and 2, note that active control lines are indicated by low logic levels, while inactive control lines remain high (approximately 5 Vdc). The low levels on capacitor control lines C0 through C9 forward bias relay driver transistors Q1 through Q10, energizing their associated control relays. For example, assume that the front panel switches are set for 2,150 MHz. Table 1 indicates that for the frequency of 2.150 MHz, all capacitor control relays on Tuning Assemblies I and II (A2A4A4 and A2A4A3, respectively) should be energized with the exception of control relay K8. In addition, all terminals (E2 through E10)

on Control Input PWB A2A4A1 should indicate a low logic level, with the exception of E6 which should read a high level (approximately 5 Vdc). Should any control line(s) indicate other than what is shown in table 1, the fault is located before the module proper (i.e. Interface PWB A19A1). Similarly, if the status of the control lines reflect what is shown in the table, but the respective control relays remain de-energized, that fault is most likely within the module proper, (i.e., Tuning Assemblies I and II).

The frequencies in table 2 will check the following control lines; 2 MHz Control, Low Band Control, and High Band Control. The use of tables 1 and 2, together with the schematic drawings supplied, should ease fault location and repair.

## 5. ASSEMBLY A19 ALIGNMENT

### 5.1 General Information

The RF-596-02 Preselector Module, when used in conjunction with the RF-590 Receiver, will normally require no alignment. Read the following warning before attempting any alignment routine.

**WARNING**

Do not attempt any Preselector Module Alignment/ Adjustment procedure until all other possible causes for degraded performance have been checked and ruled out. As an example, if appropriate relays on the Tune I and Tune II boards are not switching in pairs, it could appear to be an alignment problem. Attempting to align the unit under these conditions would be futile and would probably require returning the unit to the factory to correct. Remember, realignment should never be required unless mechanical positioning of reactive elements are accidentally (or purposely) disturbed.

### 5.2 Prealignment Performance Check

The prealignment performance check should consist of measuring the insertion loss (in dB), the accuracy at which the "selectivity window" is centered on frequency, and ensuring that the selectivity is at least -20 dB at  $\pm 10$  percent removed from the center frequency ( $F_c$ ). This may be accomplished by setting the receiver frequency select switches to the frequencies specified in table 3 and observing the results with a spectrum analyzer and tracking generator tuned to the appropriate frequency (figure 2).

### 5.3 Assembly A19 Alignment Procedure

This alignment procedure is not intended to become a part of a periodic maintenance routine. Any attempt to adjust this assembly without the required test equipment (or equivalent) will cause severe

degradation in receiver performance. The RF-596-02 Preselector Module has been factory set for optimum response characteristics over the operating frequency range, and should not require further adjustment. If after a component replacement, measured performance indicates that a realignment is required; proceed as follows:

**NOTE**

Do not make the following adjustments without the use of a Hewlett-Packard Spectrum Analyzer Model HP-8553B, equipped with Model HP-8444A Tracking Generator (or equivalent). See figure 3 for alignment test setup.

**Table 3. Optimum Response Curve Characteristics**

Center Frequency $F_c$ (MHz)	-10% Below $F_c$ (MHz)	+10% Above $F_c$ (MHz)
2.015	1.813	2.216
2.500	2.250	2.750
5.000	4.500	5.500
7.945	7.150	8.739
8.050	7.245	8.855
10.000	9.000	11.000
15.000	13.500	16.500
20.000	18.000	22.000
25.000	22.500	27.500
29.999	27.000	33.000

**5.3.1 Low Band Adjustment (Initial Setup)**

- a. For the location of the aperture screw and link assembly mentioned in the following procedure, refer to figure 4.
- b. Turn aperture screw fully counterclockwise to the rear of the cavity, then rotate five turns clockwise.
- c. Turn low band link assemblies fully clockwise, then rotate two turns clockwise.
- d. Set cores fully clockwise.

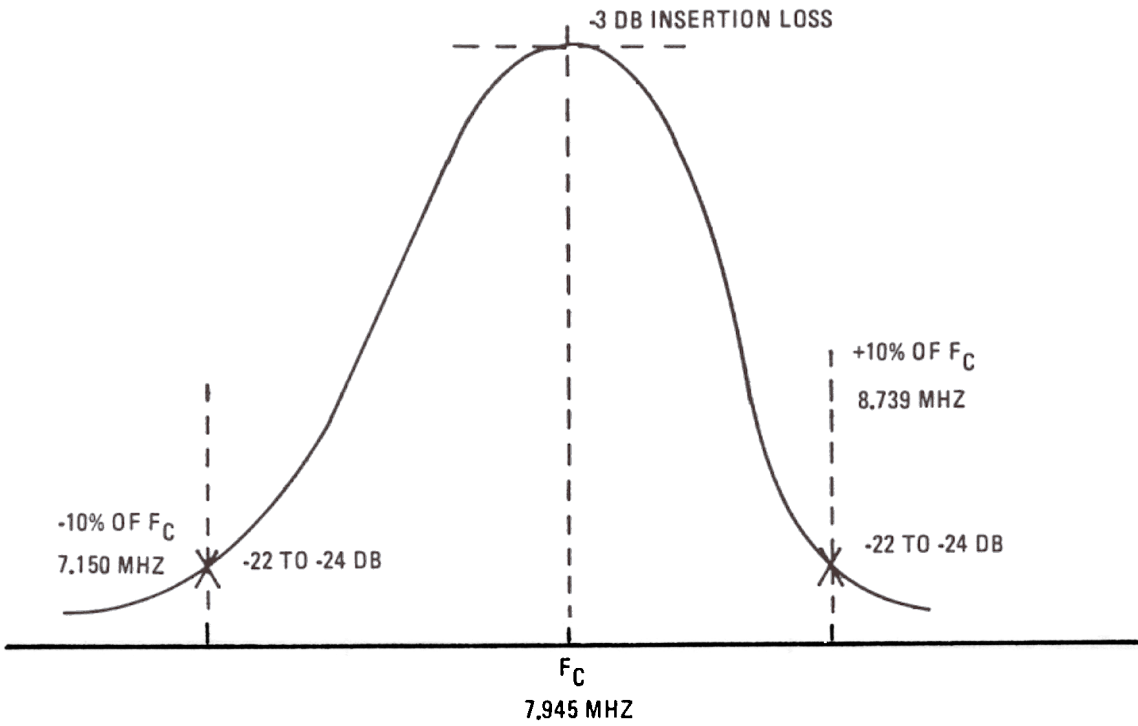
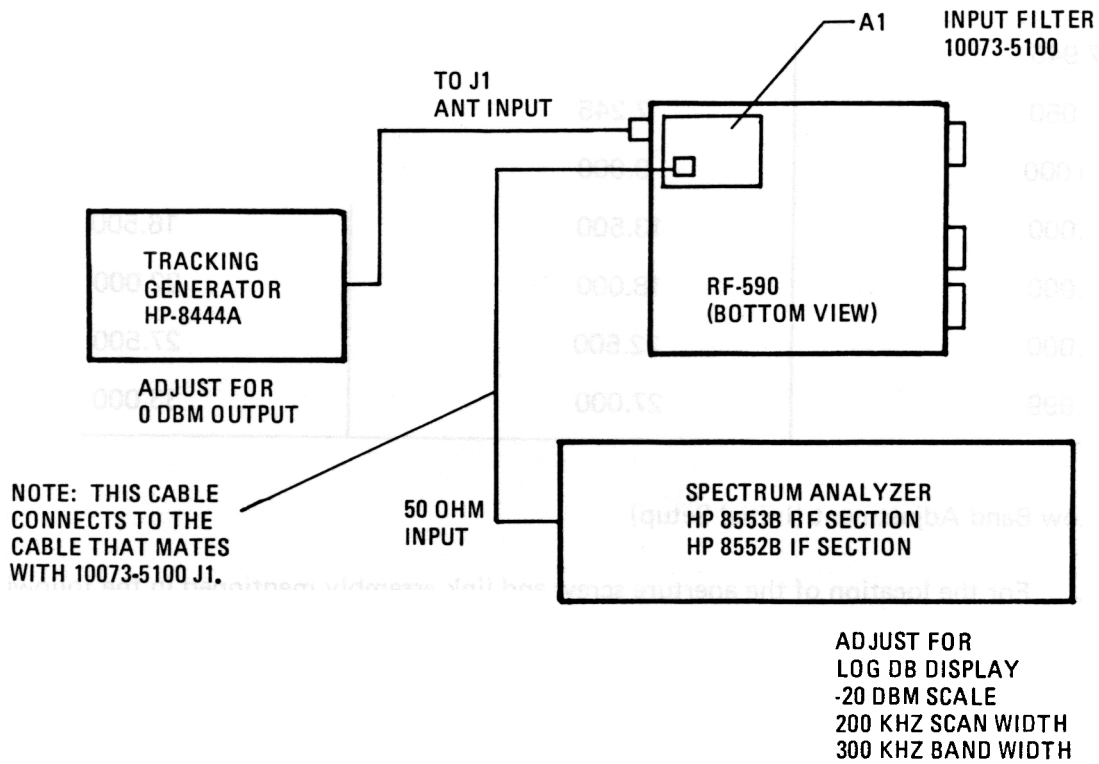


Figure 2. Typical Response Curve for Cavity Filter



590-204

Figure 3. Alignment Test Setup for Assembly A19



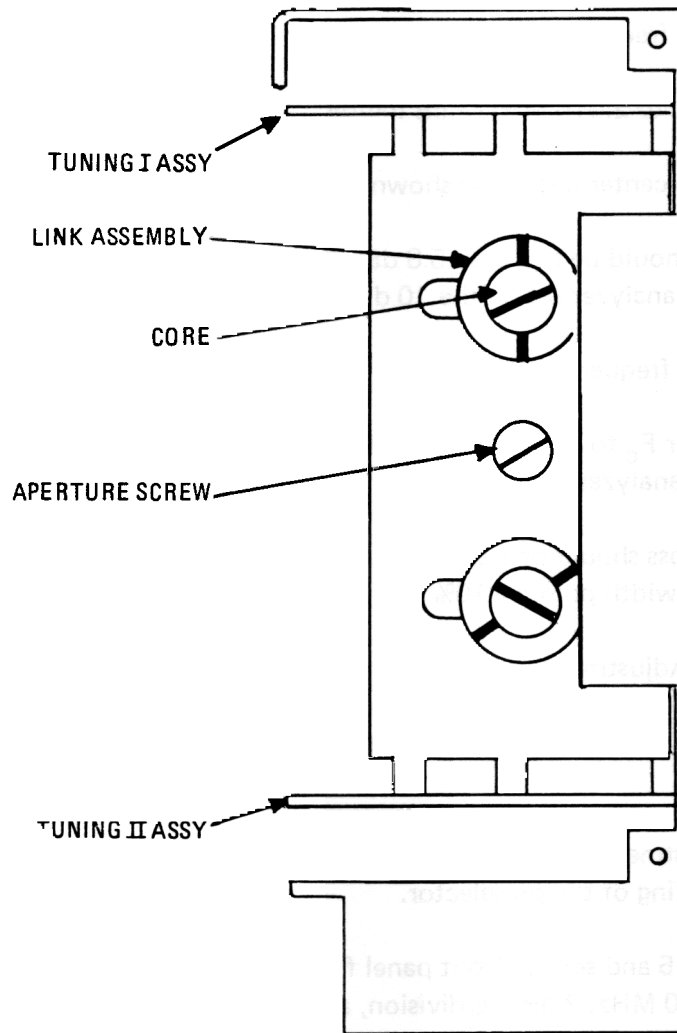


Figure 4. High/Low Band Cavity Coil Adjustment Locations

- e. Set front panel frequency switches to 7.9450 MHz.

Set analyzer to 7.945 MHz, bandwidth to 300 kHz, scan width to 0.2 MHz, 2 dB log/division. Set A3C21 and A4C22 for a centered display on the spectrum analyzer.

- g. Adjust link assemblies and aperture screw to obtain a 3 to 4 dB insertion loss. Set analyzer to 10 dB log/division. Check the points  $\pm 10\%$  of the center frequency (7.150 and 8.739 MHz) for a  $-22$  to  $-24$  dB level consistent with the 3 to 4 dB level at the center frequency ( $F_c$ ). Adjust link assemblies as necessary.

#### Low Band Adjustments (Tuning)

- a. Set front panel frequency switches to 2.015 MHz.
- b. Set analyzer  $F_c$  to 2.015 MHz, 2 dB log/division.
- c. Adjust cores to center display as shown in figure 4.
- d. Insertion loss should be less than 5.8 dB. Check the points at  $\pm 10\%$  of  $F_c$  (1.813 and 2.216 MHz) with the analyzer set on the 10 dB log/division. They should be a  $-22$  to  $-24$  dB.
- e. Set front panel frequency switches to 7.945 MHz.
- f. Set the analyzer  $F_c$  to 7.945 MHz, 2 dB log/division. Adjust A3C21 and C4C22 to center display on the analyzer.
- g. The insertion loss should be less than 4 dB. With the analyzer set to 10 dB log/division, check the bandwidth points  $\pm 10\%$  of  $F_c$  (7.150 and 8.739) for a  $-22$  to  $-24$  dB level.

#### Variable Capacitor Adjustment

##### NOTE

Use 2 dB log position on the spectrum analyzer. Precise adjustment of these trimmers is required for proper tracking of the preselector.

- a. Refer to figure 5 and set the front panel frequency switches to 7.840 MHz. Set the analyzer to a  $F_c$  of 7.840 MHz, 2 dB log/division, and bandwidth of 300 kHz. Adjust A3C10 and A4C10 to center and peak the response.
- b. Set front panel frequency switches to 7.760 MHz, and analyzer  $F_c$  at 7.760 MHz. Adjust A3C1 and A4C1 to center and peak response.
- c. Set front panel frequency switches to 7.565 MHz, and analyzer  $F_c$  to 7.565 MHz. Adjust A3C2 and A4C2 to center and peak display.
- d. Set front panel frequency switches to 7.260 MHz, and analyzer  $F_c$  to 7.260 MHz. Adjust A3C3 and A4C3 to center and peak display.
- e. Repeat steps 5.3.1e through g and 5.3.3a through d.

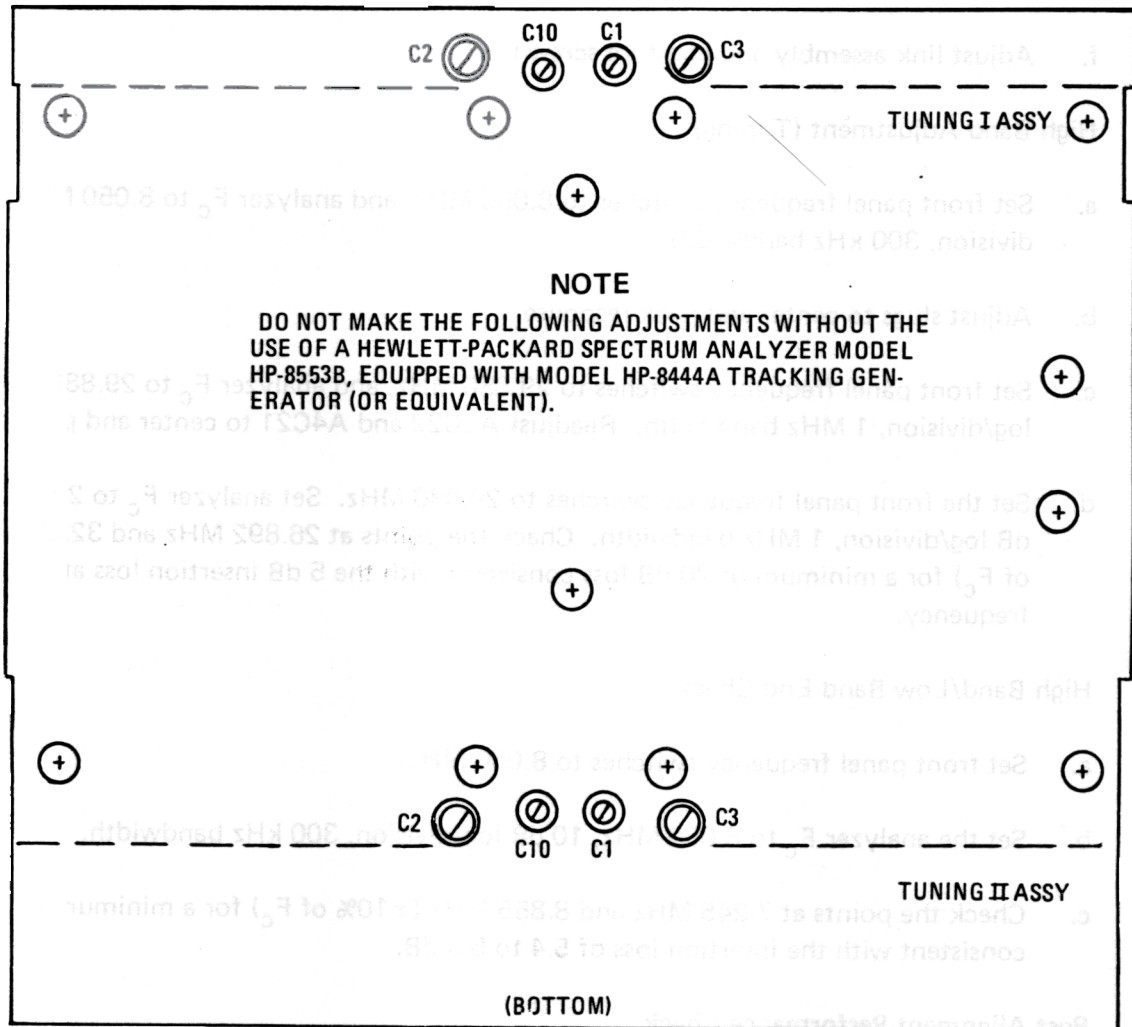


Figure 5. RF-596-02 Preselector Module Rear Panel Adjustments

**5.3.4 High Band Adjustment (Initial Setup)**

- a. Turn aperture screw (see figure 4) fully counterclockwise to rear of cavity, then rotate two turns clockwise.
- b. Turn link assemblies fully clockwise, then rotate four turns counterclockwise.
- c. Set cores fully clockwise.
- d. Set front panel frequency switches to 29.880.

- e. Set analyzer  $F_c$  to 29.880, 2 dB log/division, and bandwidth to 1 MHz. Adjust A3C22 and A4C21 to center and peak the response.
- f. Adjust link assembly and aperture screw to obtain a 5 dB insertion loss.

#### High Band Adjustment (Tuning)

- a. Set front panel frequency switches to 8.050 MHz, and analyzer  $F_c$  to 8.050 MHz, 2 dB log/division, 300 kHz bandwidth.
- b. Adjust slugs to center and peak response.
- c. Set front panel frequency switches to 29.880 MHz, and analyzer  $F_c$  to 29.880 MHz, 2 dB log/division, 1 MHz bandwidth. Readjust A3C22 and A4C21 to center and peak display.
- d. Set the front panel frequency switches to 29.880 MHz. Set analyzer  $F_c$  to 29.880 MHz, 10 dB log/division, 1 MHz bandwidth. Check the points at 26.892 MHz and 32.868 ( $\pm 10\%$  of  $F_c$ ) for a minimum of 20 dB loss consistent with the 5 dB insertion loss at the center frequency.

#### 5.3.6 High Band/Low Band End Check

- a. Set front panel frequency switches to 8.050 MHz.
- b. Set the analyzer  $F_c$  to 8.050 MHz, 10 dB log/division, 300 kHz bandwidth.
- c. Check the points at 7.245 MHz and 8.855 MHz ( $\pm 10\%$  of  $F_c$ ) for a minimum of 20 dB loss consistent with the insertion loss of 5.4 to 5.6 dB.

#### Post Alignment Performance Check

In addition to evaluating performance data (insertion loss and selectivity at  $\pm 10\%$  of  $F_c$ ) at the frequencies specified in the alignment procedure, spot checks should be made throughout the system frequency range to ensure proper tracking of the cavity filters. This may be accomplished by setting the receiver frequency select switches to the frequencies specified in table 4 and observing the results with a spectrum analyzer/tracking generator tuned to the appropriate frequency.

#### NOTE

A properly adjusted preselector will have the selectivity windows centered on frequency and meet published insertion loss and selectivity at  $\pm 10\%$  from the center frequency.

**Table 4. Post Alignment Test Frequencies**

Center Frequency ( $F_c$ )	-10% of $F_c$	+10% of $F_c$
2.500	2.250	2.750
5.000	4.500	5.500
10.000	9.000	11.000
15.000	13.500	16.500
20.000	18.000	22.000
25.000	22.500	27.500
29.999	27.000	33.000

**6. PARTS LISTS**

Tables 5 through 8 are comprehensive parts lists of all replaceable components for the RF-596-02 Pre-selector Module. When ordering parts from the factory, include a full description of the part. Manufacturers are referenced by a five digit code found in table 9. Figures 6 through 10 are component location diagrams for the RF-596-02 Preselector Module.

**7 SCHEMATIC DIAGRAMS**

Figures 11 through 14 are the RF-596-02 Preselector Module schematic diagrams.

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Table 5. Filter Select PWB Assembly Parts List

Ref. Desig.	Part No.	Description
A2	10024-2210	Filter Select PWB Assembly
C1	C11-0005-104	Capacitor, Ceramic, .1 uF
C2	CD15FA122J03	Capacitor, Mica, 1200 pF
C3	CMR04C750JODM	Capacitor, Mica, 75 pF
C4	CD15FA122J03	Capacitor, Mica, 1200 pF
C5, C6	C11-0005-104	Capacitor, Ceramic, .1 uF
C7	C320C103MIUICA	Capacitor, Ceramic, .01 uF; mfr 31433
C8	C330C104MIUICA	Capacitor, Ceramic, .1 uF; mfr 31433
C9-C14	C11-0005-104	Capacitor, Ceramic, .1 uF
C15		Not Used
C16		Not Used
C17-C19	C11-0005-104	Capacitor, Ceramic, .1 uF
C20	CMR04F361JODL	Capacitor, Mica, 360 pF
C21	CMR04F241JODL	Capacitor, Mica, 240 pF
C22, C23	C11-0005-104	Capacitor, Ceramic, .1 uF
C24	C320C103MIUICA	Capacitor, Ceramic, .01 uF; mfr 31433
CR1-CR2	1N4148	Diode, Silicon
CR4	HP5082-2800	Diode, Hot Carrier; mfr 28480
CR5-CR6	1N4148	Diode, Silicon
CR8	HP5028-2800	Diode, Hot Carrier; mfr 28480
CR9	1N4148	Diode, Silicon
K1-K4	712-5	Relay, DPDT
K5, K6	712-12	Relay, DPDT; mfr 11532
L1		Not Used
L2		See R14
L3	MS18130-14	Inductor, Fixed, 3.3 uH
L4, L5	MS181130-8	Inductor, Fixed, 1.0 uH
L6		Not Used
L7		Not Used
L8, L9	MS181130-8	Inductor, Fixed, 1.0 uH
L10	MS75083-11	Inductor, Fixed, .68 uH
L11	MS18130-9	Inductor, Fixed, 1.2 uH
L12, L13	MS181130-8	Inductor, Fixed, 1.0 uH
Q1	2N2907	Transistor, PNP
Q2	2N2222A	Transistor, NPN
Q3-Q4	2N2907	Transistor, PNP
Q5	2N2222A	Transistor, NPN
R1	RCR07G270J	Resistor, Fixed, Composition, 27 ohms, 1/4 W, 5%
R2	RCR07G103J	Resistor, Fixed, Composition, 10K ohms, 1/4 W, 5%
R3	RCR07G102J	Resistor, Fixed, Composition, 1000 ohms, 1/4 W, 5%
R4, R5	100NS2700-5	Resistor, 2,700 ohms, 1 W, 5%, mfr 00213
R6	RCR07G162J	Resistor, Fixed, Composition, 1.6K ohms, 1/4 W, 5%
R7	RCR07G822J	Resistor, Fixed, Composition, 8200 ohms, 1/4 W, 5%

Table 5. Filter Select PWB Assembly Parts List (Cont.)

Ref. Desig.	Part No.	Description
R8	RCR07G123J	Resistor, Fixed, Composition, 12K ohms, 1/4 W, 5%
R9	RCR07G103J	Resistor, Fixed, Composition, 10K ohms, 1/4 W, 5%
R10	RCR07G102J	Resistor, Fixed, Composition, 1000 ohms, 1/4 W, 5%
R11		Not Used
R12	RCR07G103J	Resistor, Fixed, Composition, 10K ohms, 1/4 W, 5%
R13	RCR07G102J	Resistor, Fixed, Composition, 1000 ohms, 1/4 W, 5%
R14/L2	6905-0610	Resistor/Inductor, Fixed
R15, R16	100NS2700-5	Resistor, High Power, 2700 ohms, 1 W, 5%; mfr 00213
R17	RCR07G183J	Resistor, Fixed, Composition, 18K ohms, 1/4 W, 5%
R18	RCR07G123J	Resistor, Fixed, Composition, 12K ohms, 1/4 W, 5%
R19	RCR07G822J	Resistor, Fixed, Composition, 8200 ohms, 1/4 W, 5%
R20	RCR07G273J	Resistor, Fixed, Composition, 27K ohms, 1/4 W, 5%
R21, R22	RCR07G750J	Resistor, Fixed, Composition, 75 ohms, 1/4 W, 5%
VR1, VR2	1N5242B	Diode, Zener .12 V, 5%
JMP1, 2	MP-1142	Jumper molded

Table 6. Tuning Assembly I Parts List

Ref. Desig.	Part No.	Description
A4	10024-2220	Tuning I PWB Assembly
C1	5801	Capacitor, Variable, .3 to 3.5 pF; mfr 91293
C2, C3	5201	Capacitor, Variable, .8 to 10 pF; mfr 91293
C4	6905-0606-1	Capacitor, Mica, 15 pF
C5	6905-0606-2	Capacitor, Mica, 30 pF
C6	6905-0606-3	Capacitor, Mica, 56 pF
C7	6905-0606-4	Capacitor, Mica, 110 pF
C8, C9	6905-0606-5	Capacitor, Mica, 220 pF
C10	5801	Capacitor, Variable, .3 to 3.5 pF; mfr 91293
C11-C20	C11-0005-104	Capacitor, Ceramic, .1 uF
C21, C22	5201	Capacitor, Variable, .8 to 10 pF; mfr 91293
C23	C11-0005-104	Capacitor, Ceramic, .1 uF
CR1 to CR11	1N3064	Diode, Silicon
K1 to K10	6905-0607	Reed, Relay
K11	6905-0608	Relay, DPDT
P1, P2	1100-1-107-02	Connector; mfr 26742

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Table 7. Tuning Assembly II Parts List

Ref. Desig.	Part No.	Description
A3	10024-2230	Tuning II PWB Assembly
C1	5801	Capacitor, Variable, .3 to 3.5 pF; mfr 91293
C2, C3	5201	Capacitor, Variable, .8 to 10 pF; mfr 91293
C4	6905-0606-1	Capacitor, Mica, 15 pF
C5	6905-0606-2	Capacitor, Mica, 30 pF
C6	6905-0606-3	Capacitor, Mica, 56 pF
C7	6905-0606-4	Capacitor, Mica, 110 pF
C8, C9	6905-0606-5	Capacitor, Mica, 220 pF
C10	5801	Capacitor, Variable, .3 to 3.5 pF; mfr 91293
C11-C20	C11-0005-104	Capacitor, Ceramic, .1 uF
C21, C22	5201	Capacitor, Variable, .8 to 10 pF; mfr 91293
C23	C11-0005-104	Capacitor, Ceramic, .1 uF
CR1-CR11	1N3064	Diode, Silicon
J1, J2	1300-007	Connector; mfr 26742
K1-K10	6905-0607	Reed, Relay
K11	6905-0608	Relay, DPDT
P1, P2	1100-1-107-02	Connector; mfr 26742
Q1-Q10	MPS-6562	Transistor, PNP; mfr 04713
R1	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R2	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R3	RCR05G103J	Resistor, Fixed Composition, 10K ohms, 1/8 W, 5%
R4	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R5	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R6	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R7	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R8	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R9	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R10	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R11	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R12	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R13	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R14	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R15	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R16	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R17	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%
R18, R19	RCR05G392J	Resistor, Fixed, Composition, 3900 ohms, 1/8 W, 5%
R20	RCR05G103J	Resistor, Fixed, Composition, 10K ohms, 1/8 W, 5%



**Table 8. Preselector Interface PWB Assembly Parts List**

Ref. Desig.	Part No.	Description
A19	10073-6400	Preselector Interface PWB Assembly
C1	CK06BX104M	Capacitor, Ceramic, 0.1 uF, 50 V
C2		Not Used
C3 – C6	CK06BX104M	Capacitor, Ceramic, 0.1 uF, 50 V
C7	C26-0025-100	Capacitor, Tantalum, 10 uF, 25 V
C8 – C21	CK06BX104M	Capacitor, Ceramic, 0.1 uF, 50 V
C22	C26-0025-339	Capacitor, Tantalum, 3.3 uF, 25 V
CR1 – CR5	1N4454	Diode
J1	J46-0032-010	Header, 10 Pin
J2	J46-0032-006	Header, 6 Pin
J3	J70-0007-010	Card Connector, 20 Pin
J4	J46-0032-005	Header, 5 Pin
JMP1	MP-1142	Molded Jumper
L1 – L12	L-0652	Inductor, Fixed, 1 uH
L13	10073-7029	Inductor, Toroid
L14	L-0652	Inductor, Fixed, 1 uH
R1	R65-0003-103	Resistor, Film, 1/4 W, 10K
R2	R65-0003-153	Resistor, Film, 1/4 W, 15K
R3, R4	R65-0003-103	Resistor, Film, 1/4 W, 10K
R5	R65-0003-153	Resistor, Film, 1/4 W, 15K
R6, R7	R65-0003-103	Resistor, Film, 1/4 W, 10K
R8	R65-0003-153	Resistor, Film, 1/4 W, 15K
R9, R10	R65-0003-103	Resistor, Film, 1/4 W, 10K
R11, R12	R50-0010-103	Resistor, SIP, 10K
U1, U2	I01-0000-156	CD4094
U3, U4	10073-8006-701	PROM
U5	I30-0003-000	LM324
U6, U7	I05-0000-005	SN74LS05
VR1	I11-0001-001	Regulator 5 V

**HARRIS**  
**RF COMMUNICATIONS**

Table 9. List of Manufacturer's Codes

Mfr. Code	Name & Address	Mfr. Code	Name & Address
00213	Nytronics Components Group Inc. Orange Street Darlington, SC 29532	26742	Method Electronics Inc. 7447 W. Wilson Avenue Chicago, IL 60656
01295	Texas Instruments Inc. Semiconductor Group P.O. Box 5012 13500 N. Central Expressway Dallas, TX 75222	27014	National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051
04713	Motorola Inc. Semiconductor Division 5005 E. McDowell Road Phoenix, AZ 85036	28480	Hewlett-Packard Company 1501 Page Mill Road Palo Alto, CA 94304
07263	Fairchild Semiconductor Div. 464 Ellis Street Mountain View, CA 94042	31433	Union Carbide Corporation Components Division Greenville, SC 29606
11532	Teledyne Relays 3155 W. EL Segundo Blvd. Hawthorne, CA 90250	53387	3M Company Electronic Products Division 3M Center St. Paul, MN 55101
13848	E.F. Johnson Company Comco/Communications Div. Coral Way Suite 106 Miami, FL 33155	91293	Johanson Manufacturing Company Box 329 Boonton, NJ 07005
18342	Amp Inc. Syscom Division 3711 Paxton Street Harrisburg, PA 17101		
21921	RCA Corporation Distributor and Special Products Clements Bridge Road P.O. Box 100 Deptford, NJ 08096		

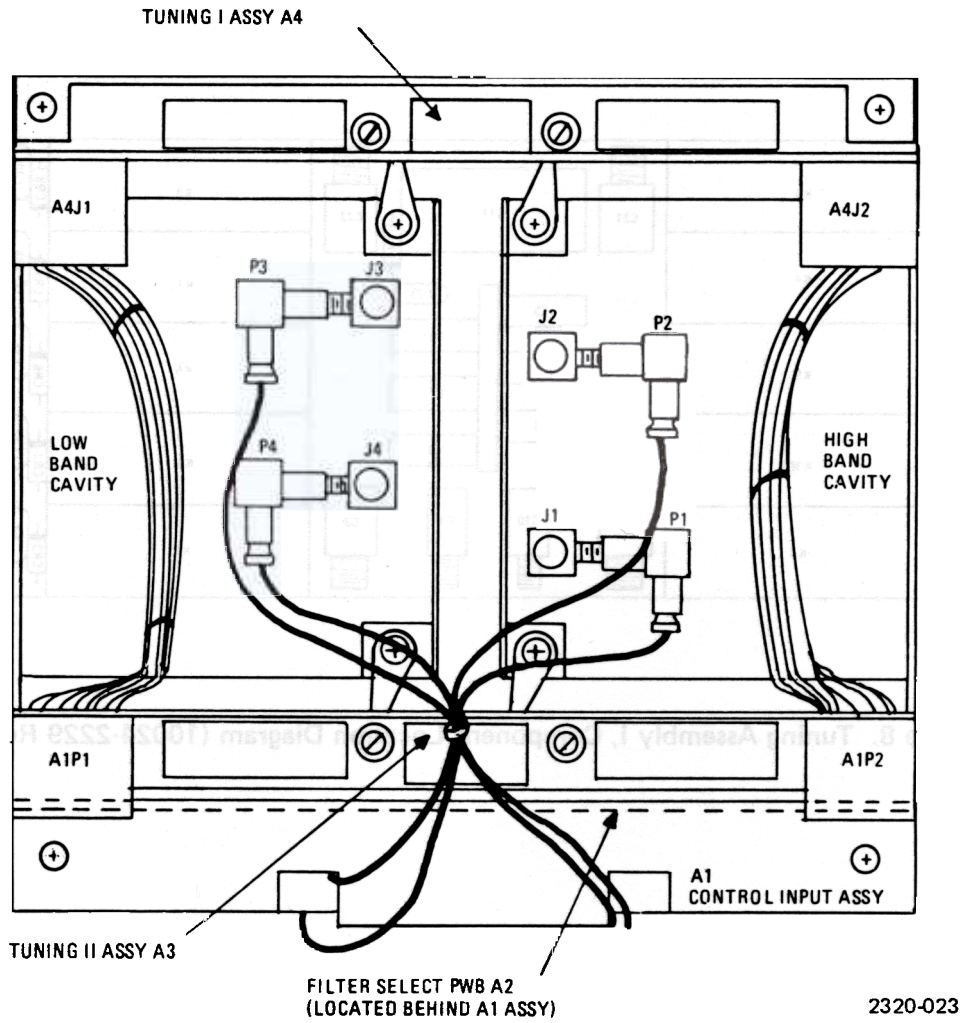


Figure 6. RF-596-02 Filter Assembly Module Locations

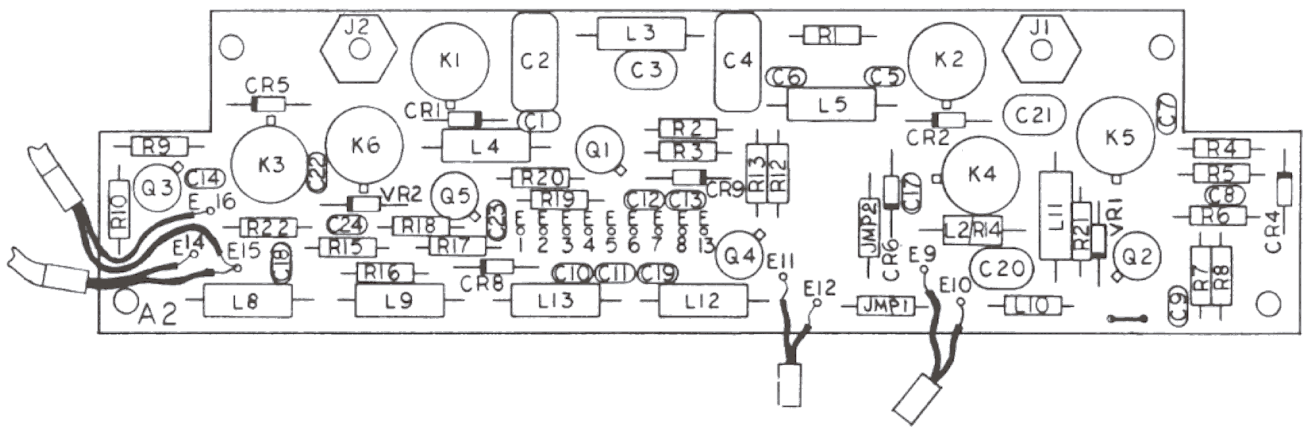


Figure 7. Filter Select PWB, Component Location Diagram (10024-2210)

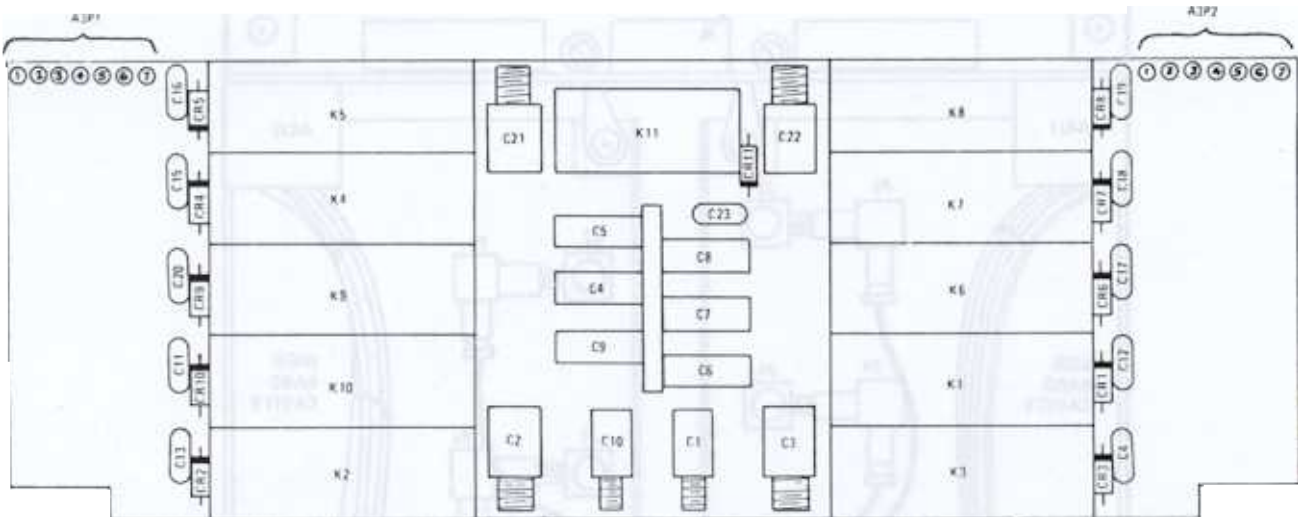


Figure 8. Tuning Assembly I, Component Location Diagram (10024-2229 Rev. A)

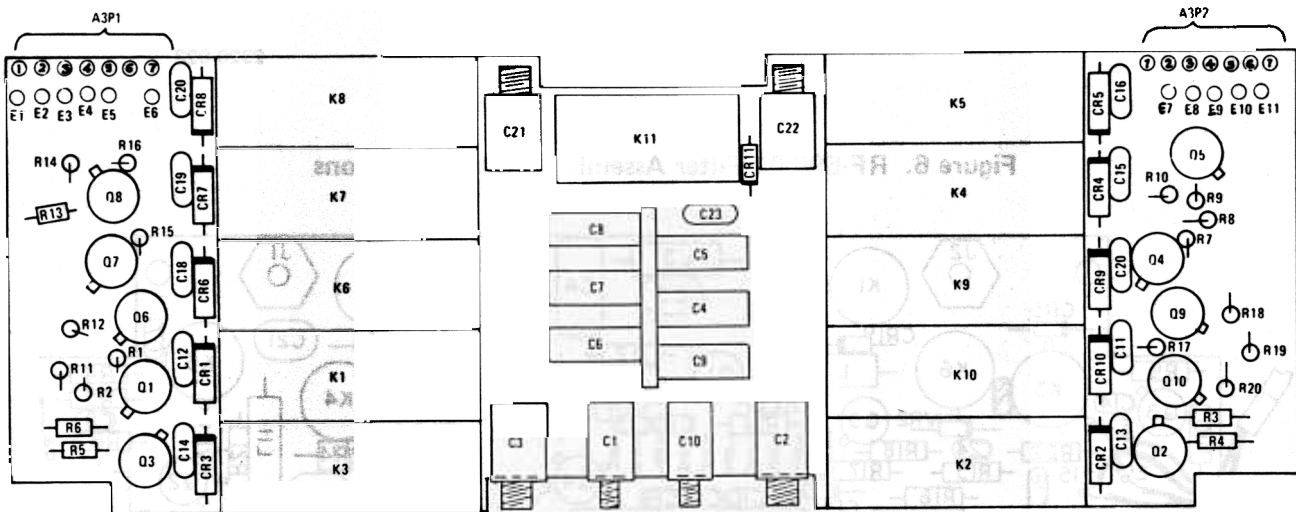


Figure 9. Tuning Assembly II, Component Location Diagram (10024-2339 Rev. A)

NOTES

1. COMPLETED ASSY SHALL BE IN ACCORDANCE WITH QC-3000.
2. MOUNT CONNECTOR J3 ON FAR SIDE
3. C21 MOUNTS ON FAR SIDE OF BOARD BETWEEN ITEM 10 AT E2 AND ITEM 9. SEE DETAIL "A".
4. REMOVE PIN 5 OF J1, PIN 3 OF J2 AND PIN 3 OF J4 FOR KEYING PURPOSES

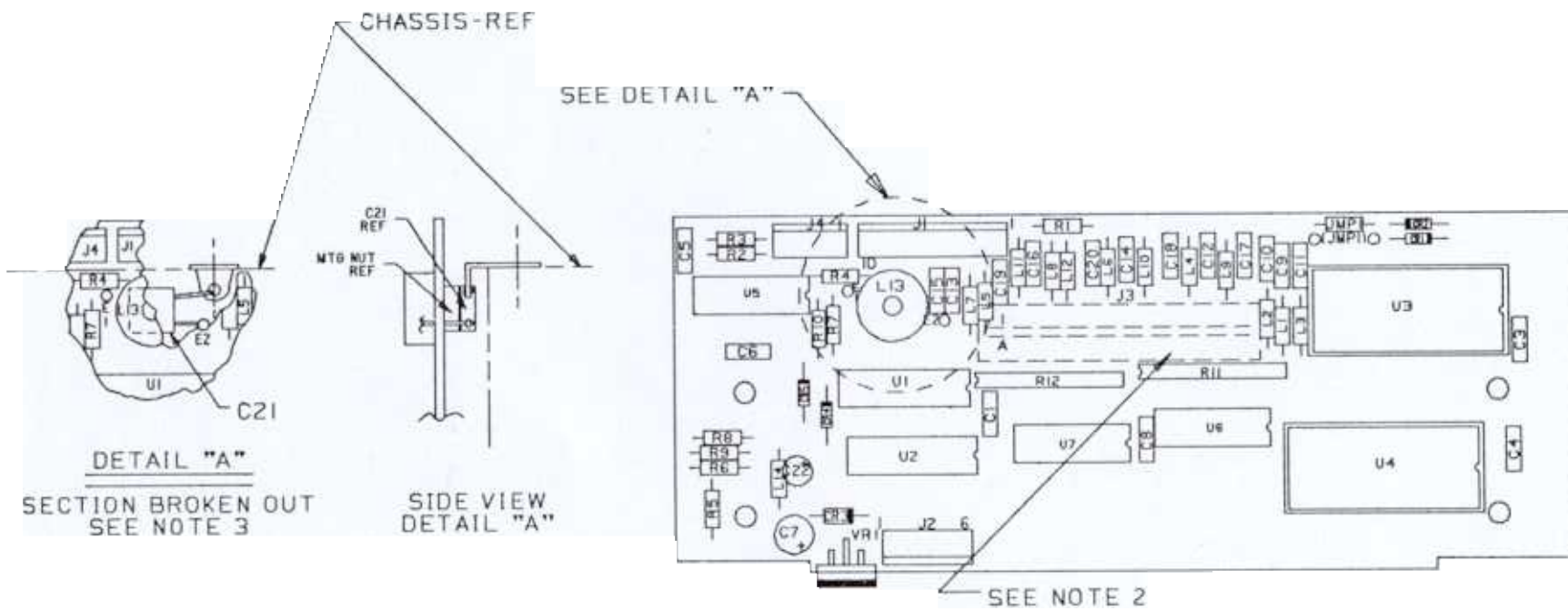


Figure 10. Interface PWB, Component Location Diagram

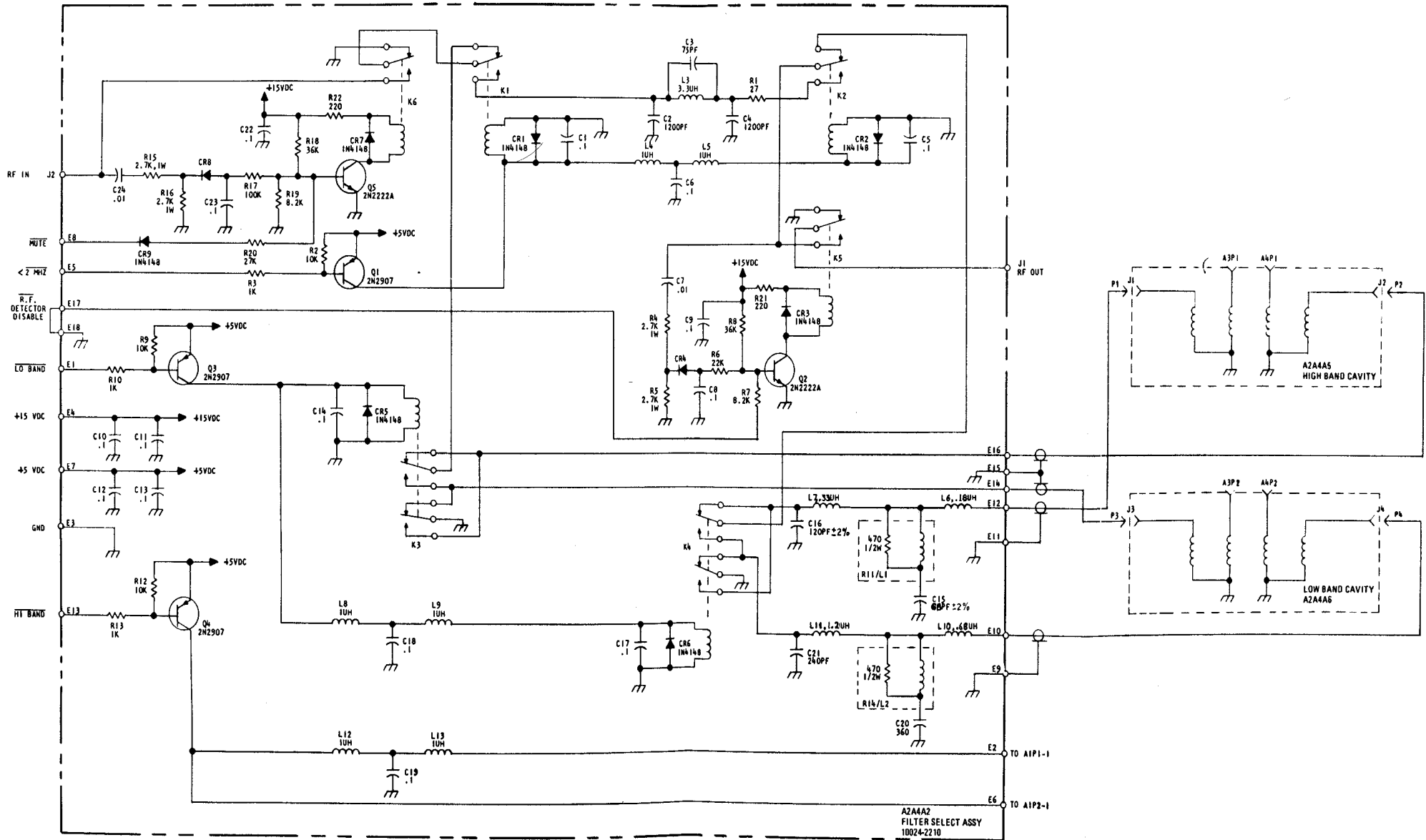


Figure 11. Filter Select PWB Schematic Diagram

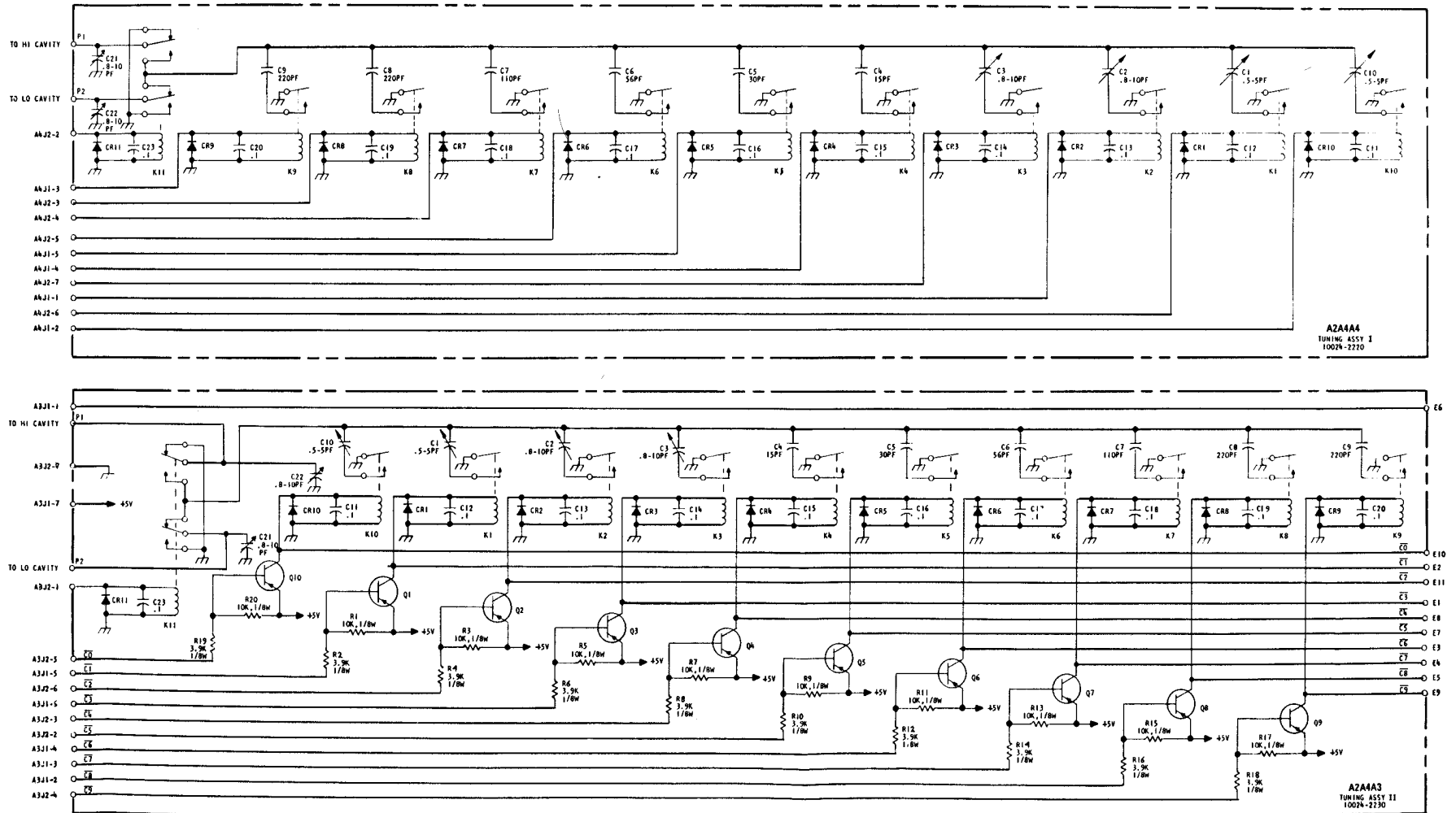
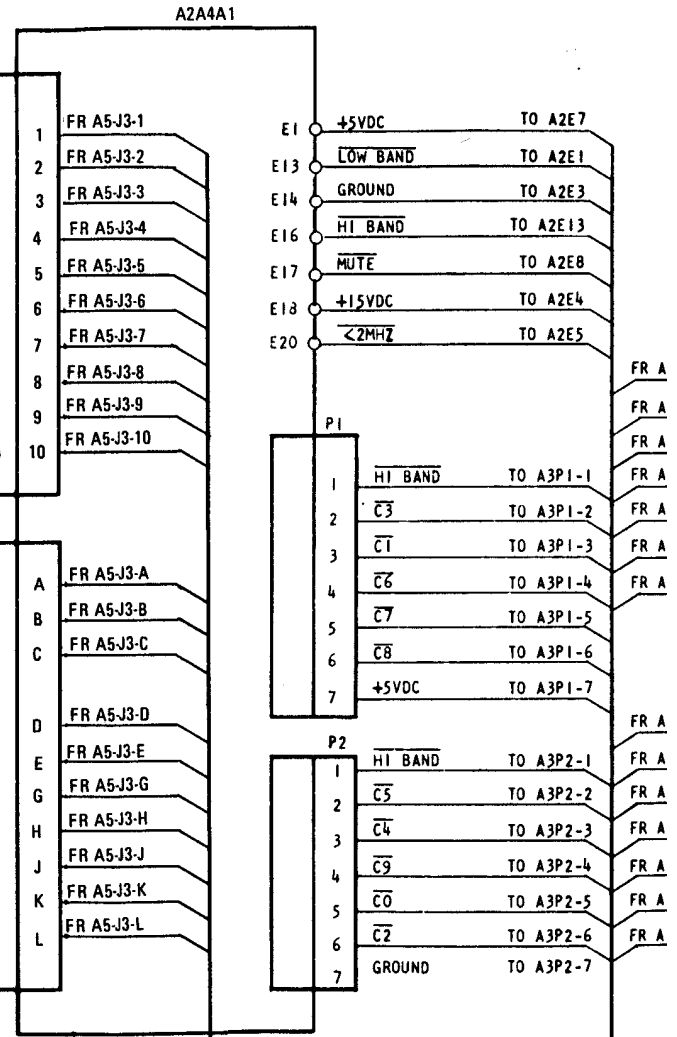
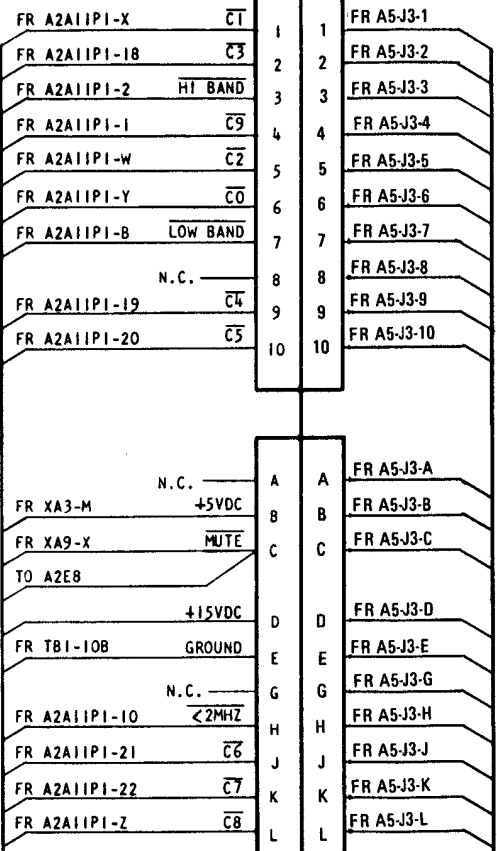
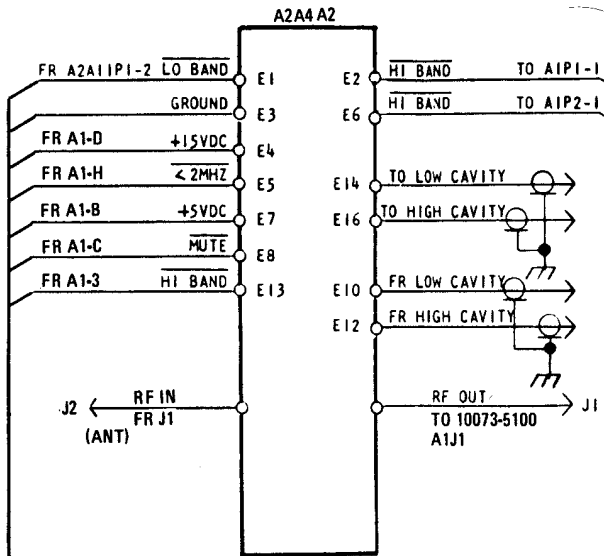
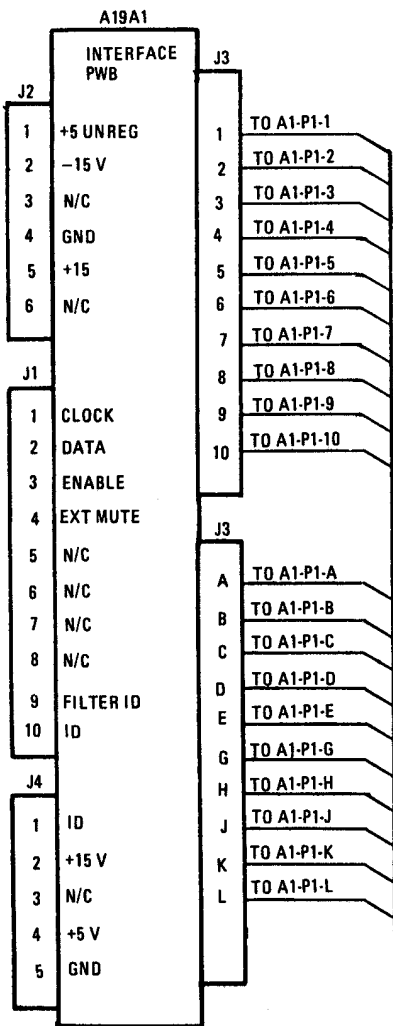


Figure 12. Tuning Assemblies I and II,  
Schematic Diagram





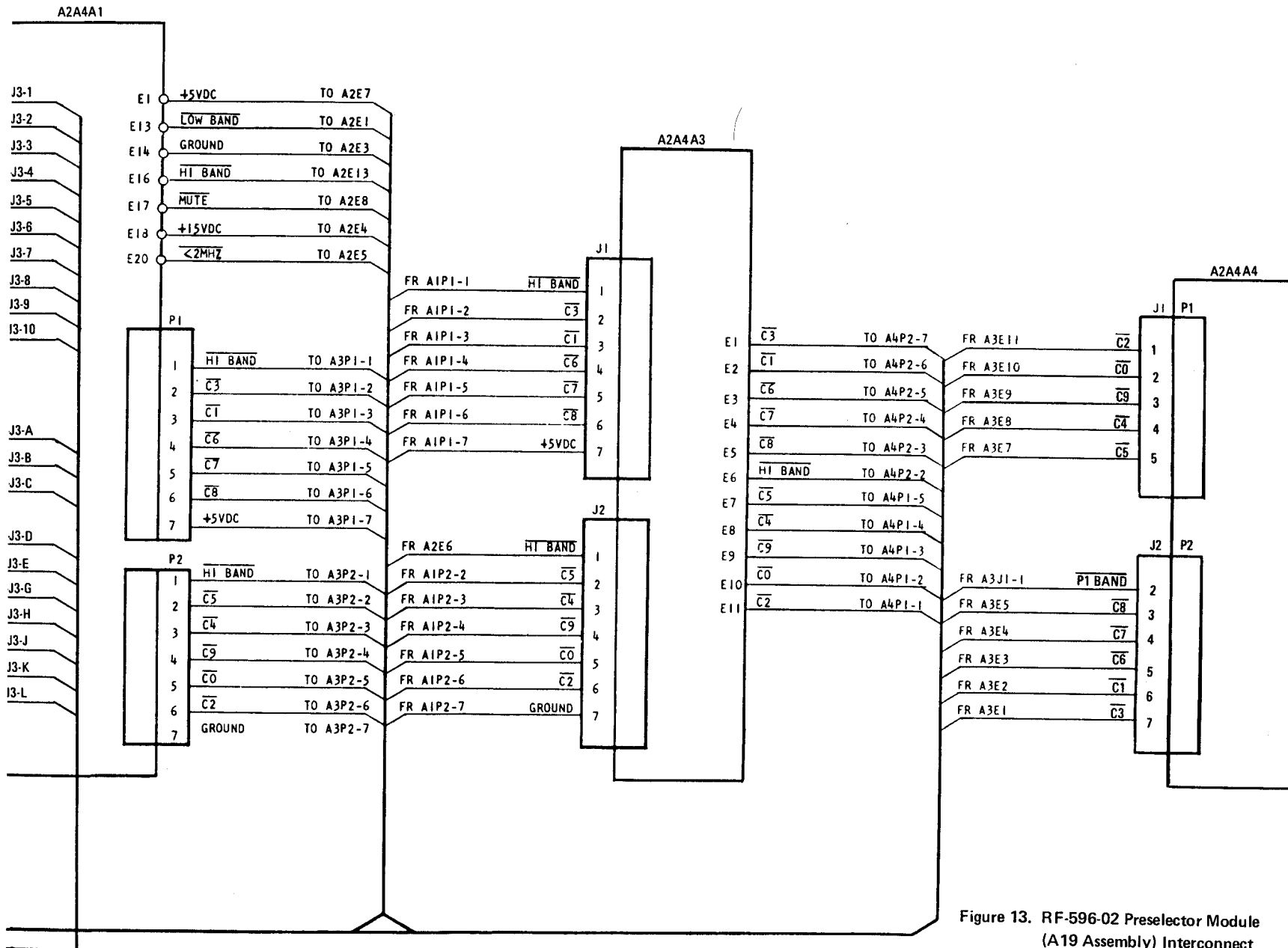


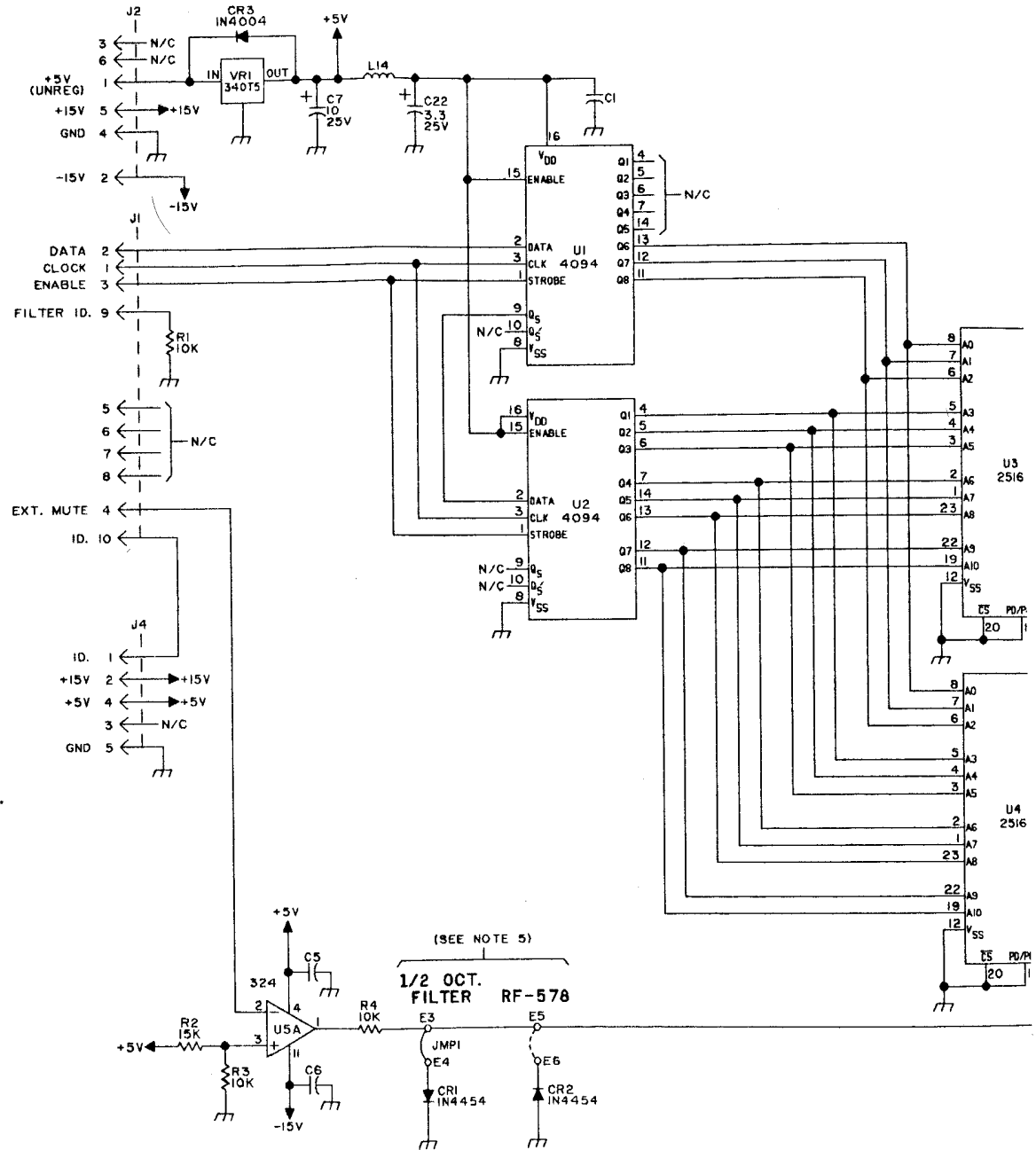
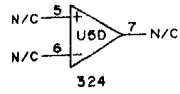
Figure 13. RF-596-02 Preselector Module (A19 Assembly) Interconnect Schematic Diagram

2

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1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE 0.1 MICROFARAD.
4. ALL INDUCTOR VALUES ARE 1000 MICROHENRYS.
5. STRAP BETWEEN E3 AND E4 (JMPI) FOR 1/2 OCT. FILTER. STRAP E5 TO E6 FOR RF-578.
6. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
7. C21 IS TO BE GROUNDED TO AN EXTERNAL CHASSIS THROUGH A TERMINAL LUG OFF THE PWB AS SHOWN.

UNUSED GATES



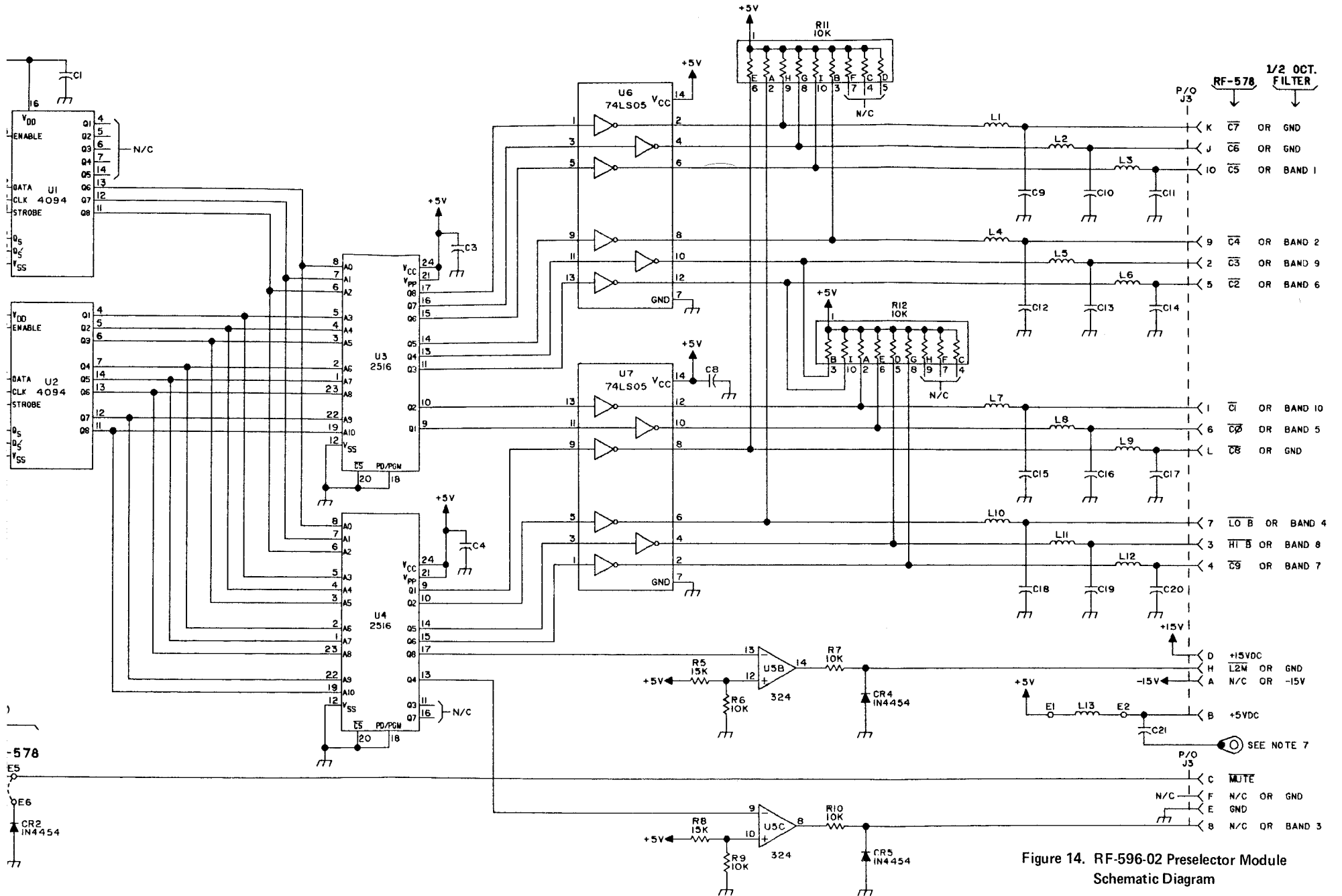


Figure 14. RF-596-02 Preselector Module Schematic Diagram

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**1. CIRCUIT DESCRIPTION**

Audio Amplifier Assembly A23 receives audio input from the A5 assembly and outputs a minimum of 2.5 watts of audio power at maximum AF gain control settings to the receiver front panel 8 ohm speaker. The total harmonic distortion at full output is 5 percent maximum and typically it's less than 1%.

Low level audio from the A5 Assembly is applied to voltage divider network R1 and R2. U1 provides 48 dB of fixed voltage gain to provide audio output power. U1 output drives the internal 8 ohm speaker through a shielded cable to prevent interference, and is also routed to rear panel connector J7 for use in driving an external 8 ohm speaker.

**2. AUDIO AMPLIFIER ASSEMBLY A23 INTERFACE CONNECTIONS**

Table 1 lists the Audio Amplifier A23 Interface.

**Table 1. Audio Amplifier A23 Interface**

Connector	Function	Characteristics
J1-1	Audio Input	From A5
J1-2	Audio Ground	From A5
J1-3	Spare	
J2-1	Ground	
J2-2	Ground	
J2-3	External Audio Output	To Rear Panel J7, 2.5 watts/8 ohms
J2-4	External Audio Output	To Rear Panel J7, 2.5 watts/8 ohms
J2-5	External Audio Output	To Rear Panel J7, 2.5 watts/8 ohms
J2-6	External Audio Output	To Rear Panel J7, 2.5 watts/8 ohms
J3-1	Power	+15 Vdc, 45 mA (quiescent)
J3-2	Ground	
J3-3	Spare	
E1	Speaker Audio Output	To Front Panel Speaker, 2.5 watts/8 ohms
E2	Speaker Audio Ground	To Front Panel Speaker
E3	Speaker Audio Shield	To Front Panel Speaker

**3. MAINTENANCE**

There are no adjustments or alignments on the A23 assembly.

**4. PARTS LIST**

Table 2 is a comprehensive parts list of all replaceable components in Audio Amplifier Assembly A23. When ordering parts from the factory, include a full description of the part. Use figure 1, Audio Amplifier Assembly A23 Component Location Diagram to identify parts.

**5. SCHEMATIC DIAGRAMS**

Figure 2 is the Audio Amplifier Assembly A23 schematic diagram.

**Table 2. Audio Amplifier Assembly A23 Parts List (PL 10073-5800)**

Ref. Desig.	Part Number	Description
	10073-5800	PWB, AUDIO AMPLIFIER
C1	1075-1039	CAPACITOR, ALUM, ELEC, 20 VDC, 680UF
C2	M39014/02-1320	CAP .47UF 10% 50V CER-R
C3	C26-0025-100	CAP 10UF 20% 25V TANT
C4	10073-7047	CAPACITOR
C5	M39014/02-1302	CAP .022UF 20% 100V CER
C6	10073-7048	CAPACITOR
C7	M39014/02-1320	CAP .47UF 10% 50V CER-R
E1	MP-0287	CONNECTOR PIN
E2	MP-0287	CONNECTOR PIN
E3	MP-0287	CONNECTOR PIN
J1	J46-0022-003	HDR 3 PIN SINGLE
J2	J-0870	CONN , 10 PIN
J3	J46-0022-003	HDR 3 PIN SINGLE
L1	10073-7043	INDUCTOR
R1	R65-0003-183	RES 18K 5% 1/4W CAR FILM
R2	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R3	R65-0003-279	RES 2.7 5% 1/4W CAR FILM
R4	R65-0003-681	RES 680 5% 1/4W CAR FILM
R5	R65-0003-510	RES 51 5% 1/4W CAR FILM
U1	10073-7119	IC AUDIO AMP

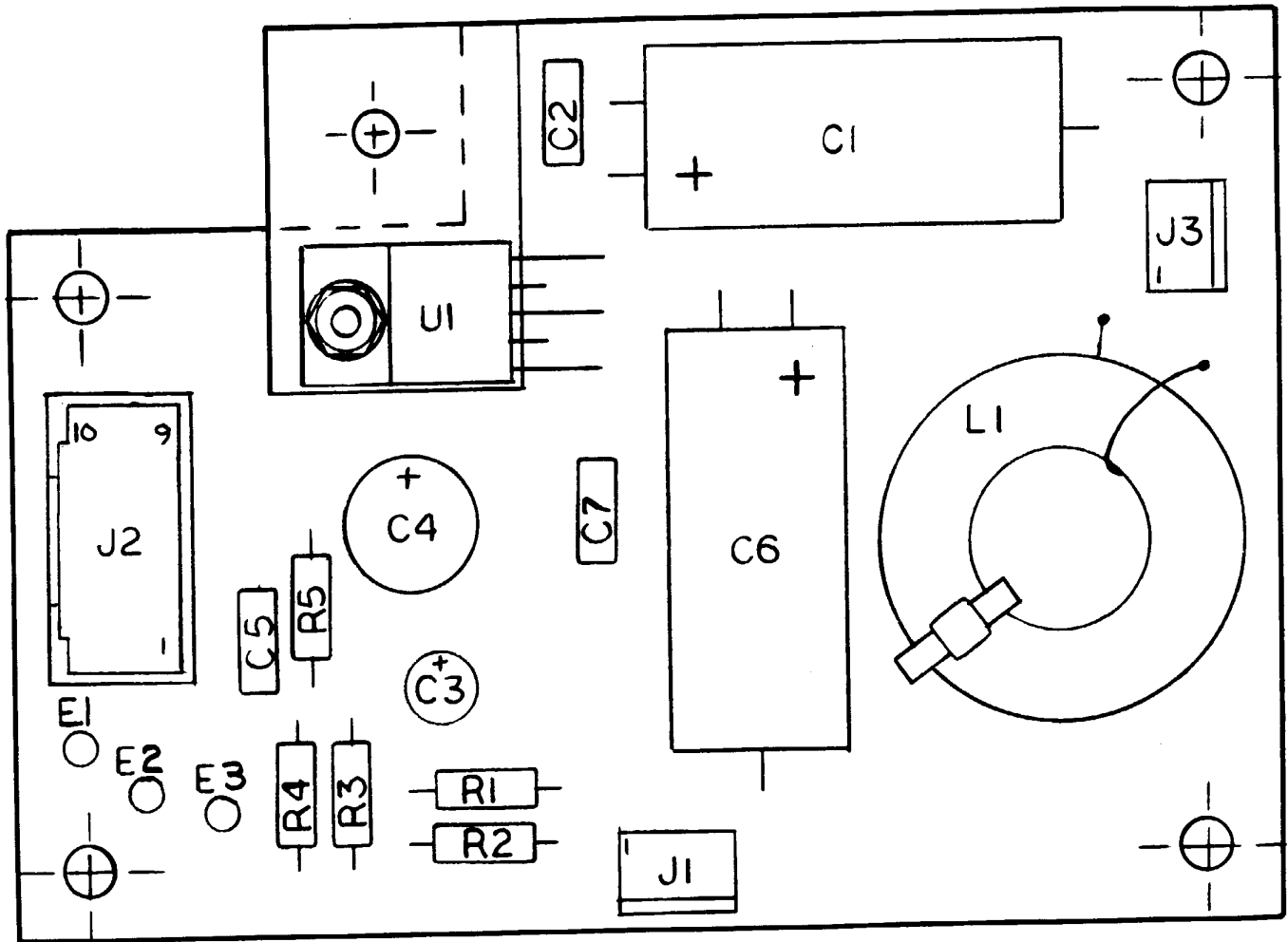


Figure 1. Audio Amplifier Assembly A23 Component Location Diagram (10073-5800, Rev. D)

- NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
  2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
  3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
  4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

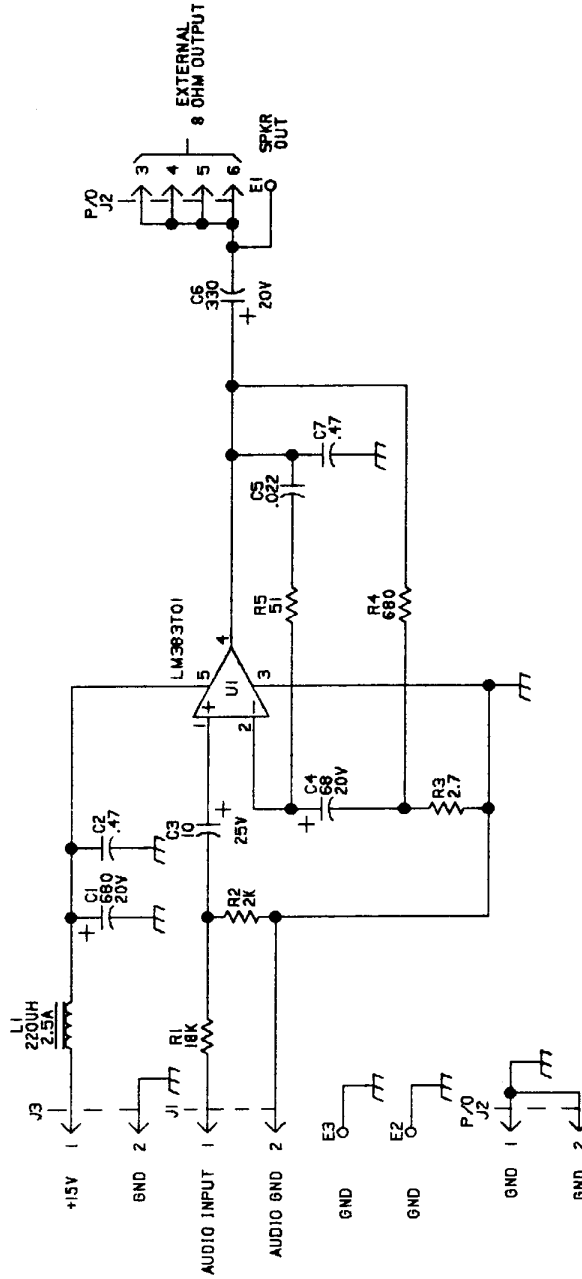


Figure 2. Audio Amplifier Assembly A23 Schematic Diagram (10073-5801, Rev. D)



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# **RF-553-01**

# **REMOTE PRESELECTOR**

# **INTERFACE**

# **(A24 ASSEMBLY)**

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## RF-553-01 REMOTE CONTROL ADAPTER GENERAL DESCRIPTION

The RF-553-01 Remote Control Adapter enables the RF-551A/552 Preselector to be remotely controlled by the RF-590 Receiver. This option consists of A24 Interface PWB (10073-6900) and necessary interconnecting cables and connectors.

The A24 Interface PWB (10073-6900) is used to convert serial data from the RF-590 to parallel data for use with either preselector. Serial data is supplied to J2 of A24 Interface PWB from A14 Control PWB through W21. Parallel data to the remote preselector is sent through Interconnect Cable W41 (10073-6917) from J9 on the rear panel of the RF-590 Receiver. Figure 1 shows the location of the A24 Interface PWB on the RF-590 Receiver Chassis.

### 2. FUNCTIONAL DESCRIPTION

Refer to the component location diagram, figure 2; schematic diagram, figure 3; Interface (A24) Interconnect diagram, figure 4; and Interconnect Cable diagram, figure 5 through this discussion.

Upon initial turn on of the RF-590, R10, C13 and inverter U7 produce the trailing-edge-triggering for U8. U8 enables the shift registers U1, U2, and U3 and gated buffers U4, U5, and U6 to load frequency information to the preselector.

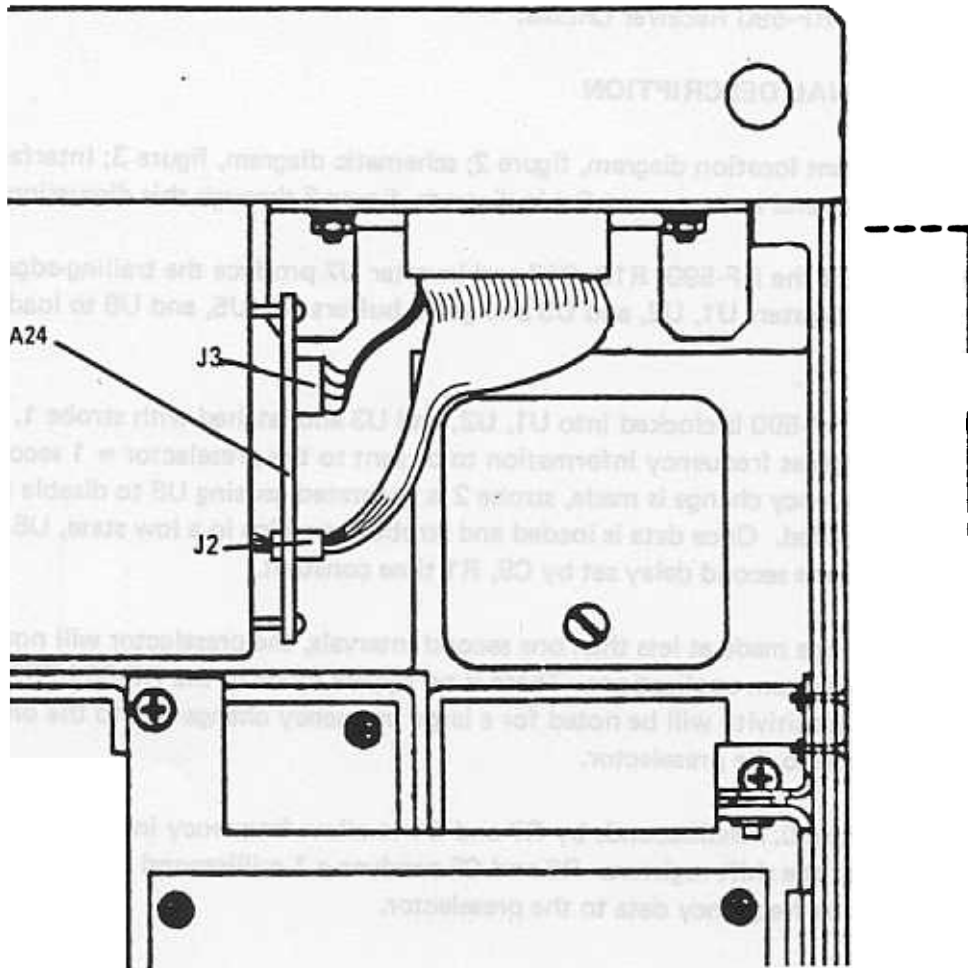
Serial data from the RF-590 is clocked into U1, U2, and U3 and latched with strobe 1. U8 is a retriggerable one shot that enables frequency information to be sent to the preselector  $\approx$  1 second after a frequency change. When a frequency change is made, strobe 2 is generated causing U8 to disable the shift registers while data is being loaded. Once data is loaded and strobe 2 remains in a low state, U8  $\overline{QA}$  enables the shift registers after a one second delay set by C9, R1 time constant.

If frequency changes are made at less than one second intervals, the preselector will not respond. A bypass signal is provided for system applications. There is no bypass mode in the RF-551/552 Preselector, a large degradation in sensitivity will be noted for a large frequency change due to the one second delay of frequency information to the preselector.

U8 QB signal is delayed 0.1 milliseconds by R7 and C4 to allow frequency information to be loaded into U4, U5, and U6 from the shift registers. R6 and C5 produce a 1 millisecond delay before U4, U5, and U6 are latched holding the frequency data to the preselector.

### 3. PARTS LIST

Table 1 is a comprehensive parts list for the A24 Interface PWB Assembly. Tables 2 and 3 are the parts lists for the cable assemblies used in this option.



**Figure 1. A24 Interface PWB Location**

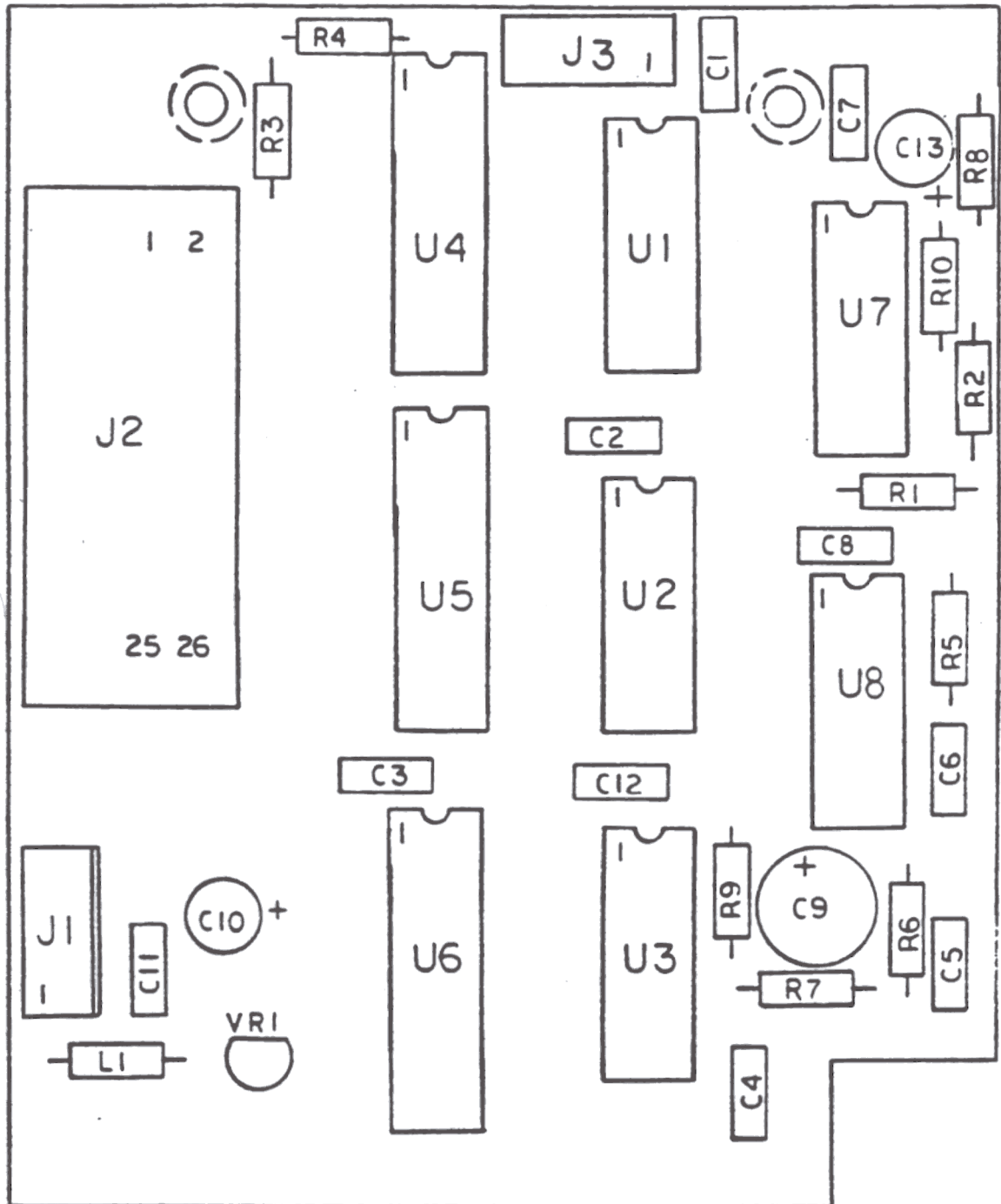


Figure 2. A24 Component Location (10073-6900)



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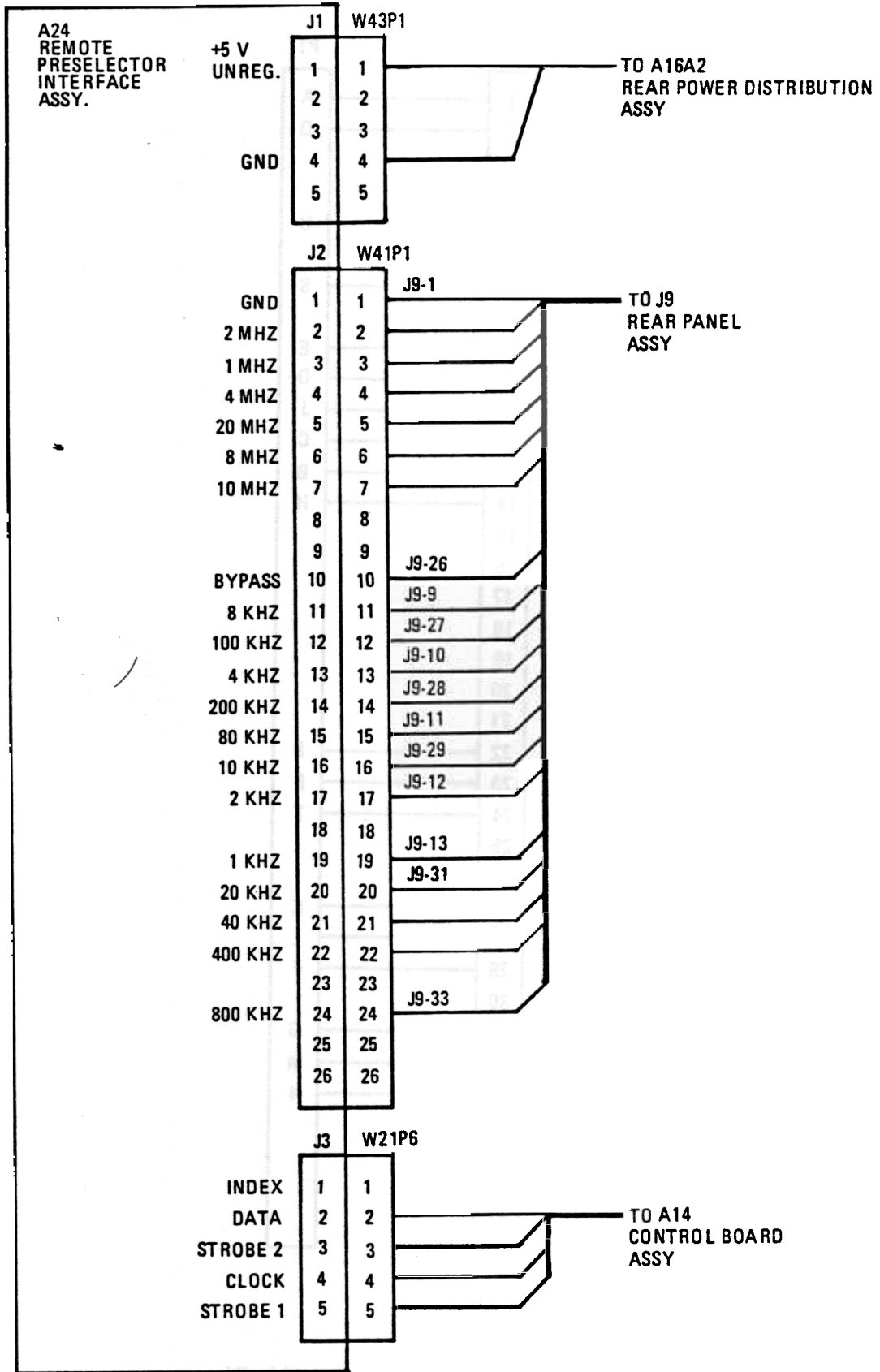


Figure 4. Interface (A24) Interconnect Diagram

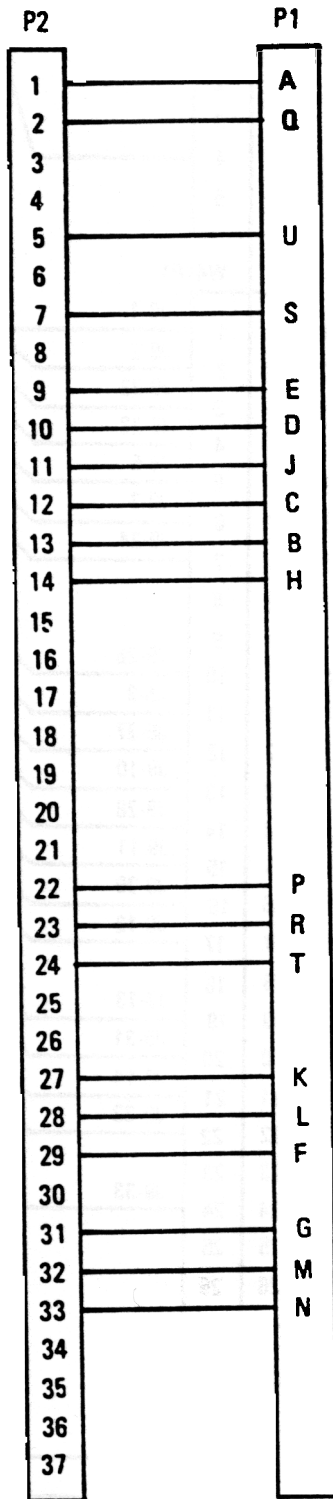


Figure 5. Interconnect Cable Assembly Diagram

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Table 1. A24 Interface PWB Parts List

Ref. Desig.	Part No.	Description
C1-C8	10073-6900	Interface PWB Assembly
C9	CK06BX104K	Capacitor, Ceramic, 1 uF, 100 V
C10	C26-0016-330	Capacitor, 33 uF
C11, C12	C26-0025-339	Capacitor, 3.3 uF
C13	CK06BX104K	Capacitor, Ceramic, 1 uF, 100 V
J1	C26-0016-330	Capacitor, 33 uF
J2	J46-0032-005	Connector, 5 Pin
J3	J46-0031-026	Connector, 26 Pin
L1	J46-0032-005	Connector, 5 Pin
R1	MS75085-13	Coil
R2-R4	R65-0003-303	Resistor, Carbon, Film, 30K, 1/4 W, 5%
R5, R6	R65-0003-473	Resistor, Carbon, Film, 47K, 1/4 W, 5%
R7	R65-0003-103	Resistor, Carbon, Film, 10K, 1/4 W, 5%
R8-R10	R65-0003-102	Resistor, Carbon, Film, 1K, 1/4 W, 5%
U1-U3	R65-0003-473	Resistor, Carbon, Film, 47K, 1/4 W, 5%
U4-U6	I01-0000-156	Integrated Circuit, CMOS, CD4094BE
U7	I05-0000-373	Integrated Circuit, 74LS373
U8	I01-0000-018	Hex Inverter - Buffer
	I01-0000-353	Dual Monostable, CD4538BEX

Table 2. In/Output Cable Assembly Parts List

Ref. Desig.	Part No.	Description
J1	10073-6916	In/Output Cable
1	J20-0004-104	Connector, 37
2	J45-0003-101	Sockets
3	MP-3633	Key
	10073-6918	Cable Assembly

Table 3. Interconnect Cable Parts List

Ref. Desig.	Part No.	Description
P1	10073-6917	Cable Interconnect
P2, P3	905-0042	Connector Kit
20	J20-0004-004	Connector, 37
	J45-0015-333	Contact Pins

- NOTES: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND/OR ASSEMBLY DESIGNATION.
  2. RESISTOR VALUES ARE IN OHMS, 1/K $\Omega$ , 5K.
  3. CAPACITOR VALUES ARE IN MICROFARADS.
  4. VENDOR AND/OR JEDEC PART NUMBER CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NUMBER IN PARTS LIST.

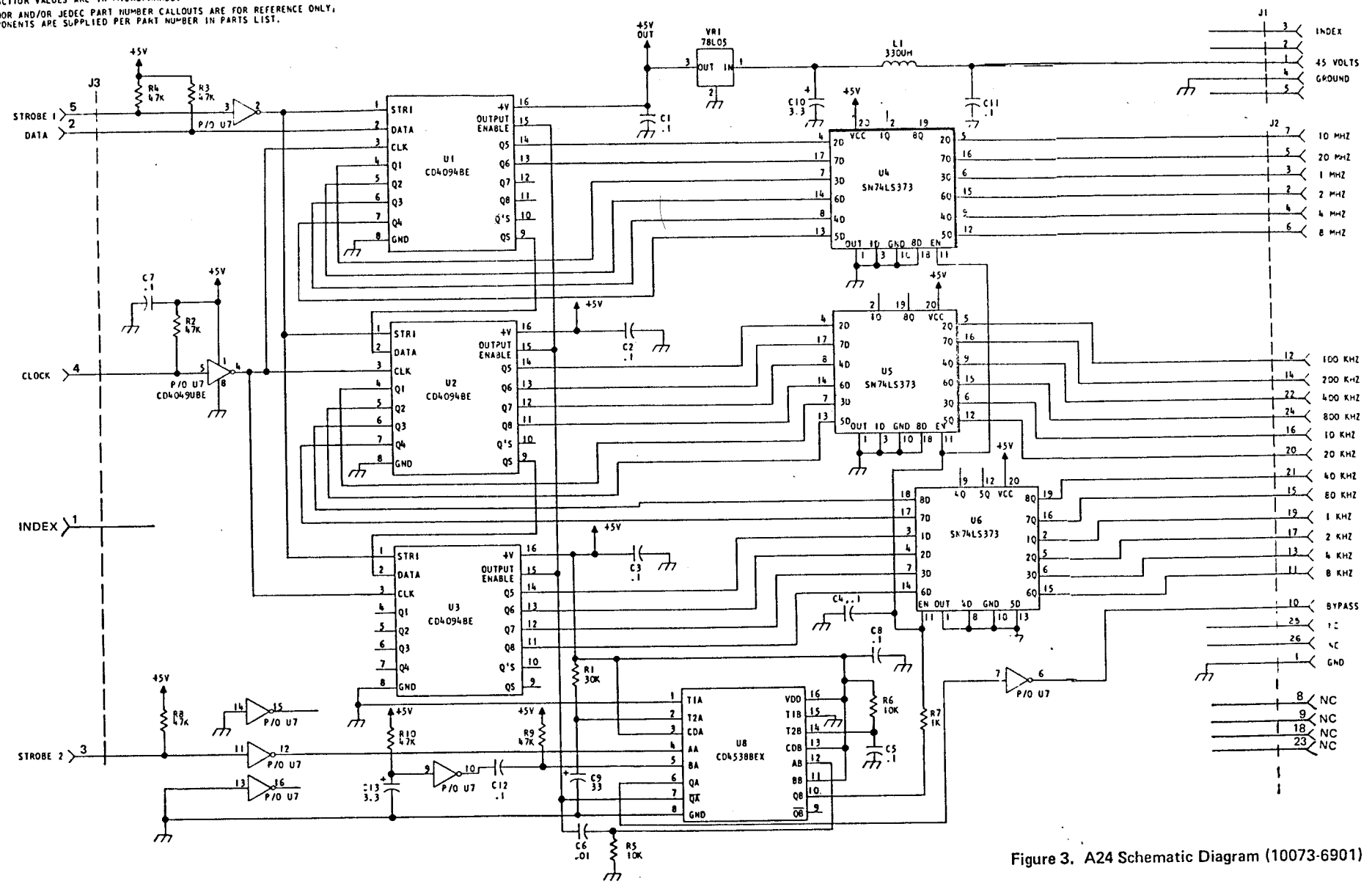


Figure 3. A24 Schematic Diagram (10073-6901)