Technical Manual

RA. 1792
HF Receiver

RACAL
The Electronics Group

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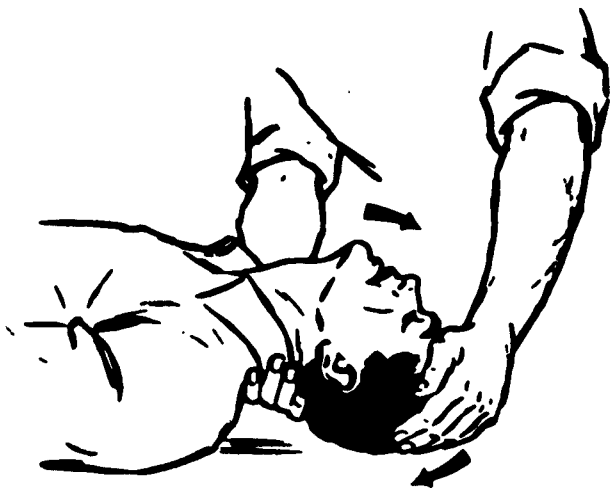
LETHAL WARNING

Voltages within this equipment are sufficiently high to endanger life.

Covers are NOT to be removed except by persons qualified and authorised to do so and these persons should always take extreme care once the covers have been removed.

Resuscitation instructions are given overleaf.

FIRST AID in case of Electric Shock



1. Lay victim on his back.
2. Clear victim's mouth and throat.
3. Tilt victim's head back as far as possible and raise his head.
4. Pinch victim's nostrils.
5. Take a deep breath.
6. Cover the victim's mouth with yours and blow, watching his chest rise.
   Note: Blow forcefully into adults, but gently into children.
7. Move your face away to allow victim to breathe out, watching his chest fall.
8. Repeat first five to ten breaths at a rapid rate; thereafter, take one breath every three to five seconds.
9. Keep victim's head back as far as possible all the time.

Have someone else send for a Doctor

Keep patient warm and loosen his clothing

DO NOT Give liquids
until patient is conscious

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

'POZIDRIV' SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trade mark of G.K.N. Screws and Fasteners Limited. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools Limited.

RA1792 - HF RECEIVER

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CHAPTER 1

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CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1 This manual contains detailed information on the installation, operation, and maintenance for the RA1792 Receiver. Chapter 1 contains general information and technical specifications. Chapter 2 contains installation data, and Chapter 3 contains detailed operating procedures. A detailed theory of operation is contained in Chapter 4, with Fault Finding and Maintenance data in Chapters 5 and 6. A complete parts list is contained in Chapter 7, with all circuit and wiring diagrams presented in Chapter 8.

2 The RA1792 receiver may be operated from a remote location through one of several different types of interfaces.

3 The RA1792 Receiver, shown in Figure 1-1, is a fully synthesized solid state receiver, suitable for all forms of reception and monitoring over the frequency range of 150 kHz to 30 MHz. Rapid and precise frequency selection in 10 Hz increments over the entire frequency range is achieved either through the use of a keypad or through the use of a single tuning control. The keypad permits instant selection of a new frequency regardless of the frequency the receiver is currently set to. The tuning control is an optically coupled device that provides a continuously variable tuning rate according to the speed at which it is turned. The receiver is also equipped with a 100 channel memory. Each channel may be preset to a particular frequency and operating mode through the front panel controls. When a particular channel is selected, the receiver will instantly tune to that frequency and mode. The receiver may also be set to a scan mode. In this mode the receiver will automatically scan 10 (or less) selected channels; stopping for a preset time interval (0.1 to 10 seconds) at each channel.

4 All receiver operating functions may be selected through the receiver front panel operating controls or through a remote device. Complete receiver status is shown through the liquid crystal display on the front panel.

5 The receiver provides reception capabilities for CW (A1), AM (A3), LSB/USB (A3J), FM (F3) and optionally ISB (A3B). Table 1-1 is an explanation of the international reception mode codes.

FUNCTIONAL DESCRIPTION

6 Figure 1-2 is an overall functional diagram of the RA1792 Receiver.

The input signal, in the range 150 kHz to 30 MHz, is fed through an RF amplifier stage and a 30 MHz low-pass filter to the first mixer. The amplifier stage may be bypassed if desired.

7 In the first mixer the received signal is combined with the output of the first local oscillator, a synthesizer covering the frequency range 40.605 MHz to 70.455 MHz in 10 Hz steps. This produces a first IF of 40.455 MHz which is fed through a crystal roofing filter of 16 kHz bandwidth and an AGC controlled amplifier to the second mixer. This roofing filter provides an additional selectivity option in the AM, CW, or FM modes.

TABLE 1-1. RECEPTION MODE CODES

Complete Designation Example:

2 A 2 H

Bandwidth in kHz

Type of Transmission
A = AM
F = FM
P = PCM

Purpose
0 = No modulation
1 = Telegraphy (on-off)
2 = Telegraphy (modulation)
3 = Telephony
4 = Facsimile
5 = Television
6 = Duplex Telegraphy
7 = Multichannel Telegraphy
9 = None of the above

Supplementary Characteristics
A = Single Sideband reduced carrier
B = Two independant sidebands
C = Single sideband vestigial
D = AM pulse
E = Pulse width modulation
H = Single sideband, full carrier
J = Single sideband, suppressed carrier
(None) = Double sideband, full carrier

Abbreviations:

AM = Amplitude Modulation
CW = Continuous Wave
FM = Frequency Modulation (or Phase)
FSK = Frequency Shift Keying
ISB = Independant Sideband
LSB = Lower Sideband
MCW = Modulated Continuous Wave
PCM = Pulse Coded Modulation
SSB = Single Sideband
USB = Upper Sideband
DSB = Double Sideband

8 The 40.455 MHz first IF is combined with the fixed 40 MHz output from the second oscillator synthesizer to produce a 455 kHz second IF. After amplification, this second IF is routed to a bank of six 455 kHz filters which provide the main receiver selectivity. These are selected through front panel controls; or automatically, when a sideband mode is selected.

9 A second AGC-controlled amplifier follows before demodulation takes place. In the SSB/CW/AM modes a product/synchronous detector is used. The BFO synthesizer generates a fixed 455 kHz reinserted carrier for SSB detection, but in the CW mode this signal is either variable + 8 kHz in 10 Hz steps or may be pre-programmed to provide a fixed offset BFO frequency. For AM reception the modulation is stripped off in the limiting amplifier and the resulting signal is applied to the carrier part of the product detector and mixed with the IF signal. For FM reception the 455 kHz second IF is brought through a limiting amplifier to a separate FM detector.

10 All three outputs from the synthesizers are referenced to an internal 5 MHz standard frequency source; or to external references of 1 MHz, 5 MHz, or 10 MHz.

11 The demodulated signal is fed through the audio crosspoint switch to separate AF amplifiers which provide outputs for a 600 ohm line, an internal loudspeaker and a headphone jack, and an external loudspeaker.

12 For ISB operation the optional ISB board provides the LSB signal path; while the receiver proper provides that for the USB. The LSB component of the 455 kHz second IF is processed through similar circuitry to that for the USB, with the common BFO synthesizer providing the reinserted carrier for demodulation. Two separate audio amplifiers provide 600 ohm line outputs for the two sidebands.

13 All command signals, whether from the front panel controls or from an extended remote operating position, are processed by the microprocessor assembly which is incorporated with non-volatile EAROMs located on the display assembly. These store pre-programmed frequency and mode information in each of 100 discrete channel locations for instant recall. Two separate buses carry control data and address information to/from the microprocessor/control assemblies. to the synthesizers for frequency selection, and to the appropriate switching circuits controlling the different operating modes.

MECHANICAL DESCRIPTION

14 A rigid, die-cast, full width chassis is used as the base for the main frame of the receiver. Mounted within compartments on the underside of this chassis are the mixer boards and the frequency generation system.

15 The input RF amplifier/low pass filter, main IF/AF, optional ISB IF/AF and power supply modules are located on the top surface of the cast chassis while the control and digital I/O modules are attached on the receiver main frame. All modules are accessible for maintenance and can be removed or replaced using simple hand tools without the use of a soldering iron.

REFERENCE DATA

16 Table 1-2 lists the different modules contained in the standard RA1792 receiver, the available optional modules, and the Racal part number for each module. The technical specification for the RA1792 is given in Table 1-3.

TABLE 1-2. RECEIVER MODULES

Designation	Module Name	Standard/Optional	Part No.
A1	Input RF Amplifier/Low Pass Filter	Standard	ST08233
A2	First Mixer	Standard	ST08184
A3	Second Mixer	Standard	ST08093
A4	Main IF/AF	Standard	ST08276
A6A2	Microprocessor	Standard	ST08203
*A7	First LO Synthesizer	Standard	ST80788
A8	Second LO/BFO Synthesizer	Standard	ST08283
A9A1	Front Panel Switch/Display	Standard	ST08198
A9A2	Front Panel Memory	Standard	ST08234
A5	ISB IF/AF	Optional	ST08109
A6A1	Remote Control SCORE Interface	Optional	ST08459
A10	AC Power Supply	Standard	ST80784
A10	DC Power Supply	Optional	ST80762
A11	Frequency Standard	Optional	ST08140

* Earlier Versions ST08545 (Appendix 4)

TABLE 1-3. TECHNICAL SPECIFICATION

Frequency Range	150 kHz to 30 MHz
Modes of Reception	USB/LSB (A3A, A3H, A3J, A2A, A2H, A2J) AM (A3) MCW (A2) CW (A1) ISB (A3B) optional FM (F3) Auxiliary - provides demodulated signal centred on optional fixed BFO offset frequency.
Tuning	Continuously tunable synthesizer in 10 Hz steps over the entire frequency range. Frequency setting either by numerical keypad or by single tuning knob with continuously variable tuning rate from 1 kHz per turn to approximately 20 kHz per turn, depending on the speed of rotation.
Pre-programmed Channels	EAROM memory unit may be programmed with up to 100 channel frequencies and mode which may be recalled by keypad or tuning control.
Channel Scanning	Automatic scanning of up to ten channels in any decade of the 100 stored channels. Dwell time on each channel variable in ten steps from 0.1 to 10 seconds; pre-selected by numeric keypad.
Frequency Stability	Dependant upon frequency standard used: 1. The following optional internal standard may be supplied: (a) Temperature Compensated Crystal Oscillator (TCXO): $\pm$ 2 in 10^6 from -10°C to +55°C. (b) Type 9442: (i) Temperature: ± 3 in 10^9/°C (ii) Long term: $\pm$ 3 in 10^9 per day after 3 months continuous operation. 2. External standard input: 1 MHz, 5 MHz, or 10 MHz level 0 dBm into 50 ohms.
Antenna Input	(a) Wideband, 50 ohms to 75 ohms nominal. (b) The receiver will withstand without damage input signals of 50 V EMF continuously. (c) Re-radiation: (i) 0 to 30 MHz; not greater than 10 µV PD (ii) 30 to 100 MHz: not greater than 200 pW
Sensitivity	(a) CW and SSB (A1, A2H, A3A, A3H, A3J): In a 3 kHz bandwidth, signal-plus-noise to noise ratio is better than: 150 kHz to 1 MHz: 10 dB with 3 µV (EMF) input, 1 MHz to 30 MHz: 10 dB with 1 µV (EMF) input.

TABLE 1-3. TECHNICAL SPECIFICATION (Cont'd)

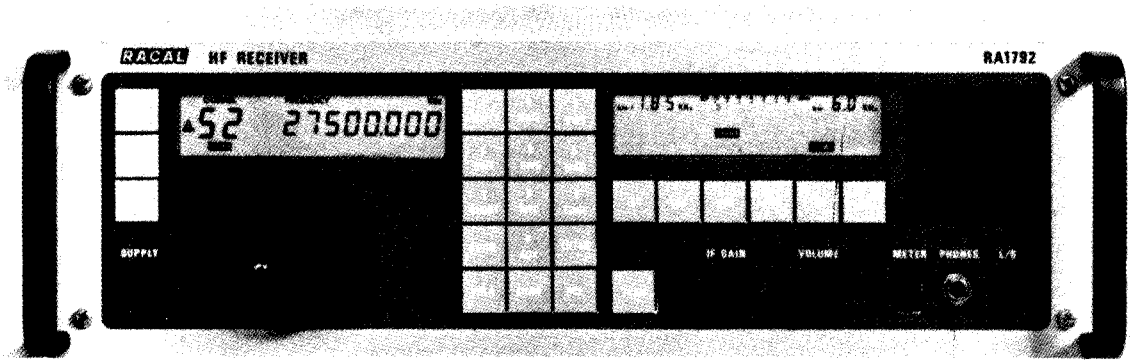
	(b) AM (A3): In a 6 kHz bandwidth, signal-to-noise to noise ratio is better than: 150 kHz to 1 MHz: 10 dB with 10 μV (EMF) input, 70% modulated at 1 kHz, 1 MHz to 30 MHz: 10 dB with 3 μV (EMF) input, 70% modulated at 1 kHz.
IF Selectivity	USB: +250 Hz to +3.2 kHz at -6 dB -400 Hz to +4.3 kHz at -60 dB LSB: -250 Hz to -3.2 kHz at -6 dB +400 Hz to -4.3 kHz at -60 dB CW1: >300 Hz at -6 dB <3 kHz at -60 dB CW2: >1 kHz at -6 dB <6 kHz at -60 dB AM1: > 3.2 kHz at -6 dB < 12 kHz at -60 dB AM2: > 6.0 kHz at -6 dB < 20 kHz at -60 dB AM3: > 16 kHz at -6 dB < 50 kHz at -60 dB Note: A maximum of six filters may be installed, in addition to a 16 kHz bypass.
Cross Modulation	With a wanted signal of 1 mV EMF in a 3 kHz bandwidth, an unwanted signal 30% modulated removed not less than 20 kHz, must be greater than 500 mV EMF to produce an output 20 dB below the output produced by the wanted signal.
Reciprocal Mixing	With a wanted signal of less than 100 μV EMF in a 3 kHz bandwidth, and unwanted signal more than 20 kHz removed is generally greater than 70 dB above the wanted signal level to give a noise level 20 dB below the output produced by the wanted signal.
Blocking	With a wanted signal of 1 mV EMF, an unwanted signal more than 20 kHz removed must be greater than 1 V EMF to reduce the output by 3 dB.
Intermodulation Products	(a) In band: Two 100 mV EMF signals within the IF passband will produce third order intermodulation products not greater than -50 dB at the IF output. (b) Out of band: With two 30 mV EMF signals, separated and removed from the wanted signal by not less than 25 kHz, the third order intermodulation products are not less than 90 dB below either of the interfering signals.
Spurious Responses	(a)External (including image and IF rejection): External signals, removed more than 20 kHz from the wanted frequency, must be greater than +80 dB relative to 1 μV EMF to produce an output equal to that produced by a 1 μV EMF signal at the wanted frequency.

TABLE 1-3. TECHNICAL SPECIFICATION (Cont'd)

	(b) Internal: The presence of an internally generated spurious response generally will not degrade the specified receiver sensitivity by more than 3 dB.
AGC	(a) Range: An increase in input of 110 dB above 2 μV EMF will produce an output change of less than 2 dB. (b) Time constants: Short, medium and long - preset to be automatically selected by mode switching, but can be set independantly by push-buttons. AGC lines are available at rear of receiver to permit remote control.
IF Gain Control	Control range 110 dB: Gain control may be switched either to manually set receiver gain or AGC threshold.
BFO	(a) Variable by main tuning control, ±8 kHz, synthesized in 10 Hz steps. (b) Pre-selected fixed offsets may be selected for use with external demodulator.
Pre-set Operating Conditions	Bandwidth, AGC time constant, and BFO offset may be pre-set for each mode so that they are automatically recalled when the mode is selected. 'Auxiliary' mode may be set up for any mode, bandwidth, AGC time constant and BFO offset. In the ISB mode, different AGC time constants may be stored for the two sidebands.
IF Output	455 kHz, nominal 100 mV into 50 ohms.
Muting	60 dB minimum by grounding rear panel connection.
AF Output	(a) Line output, 10 mW maximum into 600 ohms balanced, adjustable by internal preset level control. (b) Phone output, 1 mW maximum into 600 ohms unbalanced. (c) 200 mW maximum to internal loudspeaker which may be switched in or out of operation. (d) Connection for external loudspeaker, 200 mW into 16 ohms; 400 mW into 8 ohms.
Metering	Front panel display switched to indicate RF level or AF level output to line.
Power Supply	AC: Selections for 110, 120, 220, or 240V operation; +10% -15%. 45 to 65 Hz. DC: Receiver may also be operated from an 18 to 32 V dc source when receiver is equipped with optional dc power supply.

TABLE 1-3. TECHNICAL SPECIFICATION (Cont'd)

Power Consumption	Approximately 60 VA for ac operation; approximately 40 Watts for dc operation.
Enviromental Conditions	(a) The equipment is designed to operate under the following climatic conditions: Operating temperature -10°C to +55°C Storage temperature -40°C to +70°C Releative humidity 95% at +40°C (b) The equipment is suitable for mobile operation. (c) The equipment is suitable for air transportation in unpressurized conditions and for operation up to altitudes of 3500 meters above sea level.
Dimensions	Height - 133 mm (5.25 in.) Width - 483 mm (19 in.) Depth - 458 mm (18 in.)
Weight	14 kg (31 lbs).



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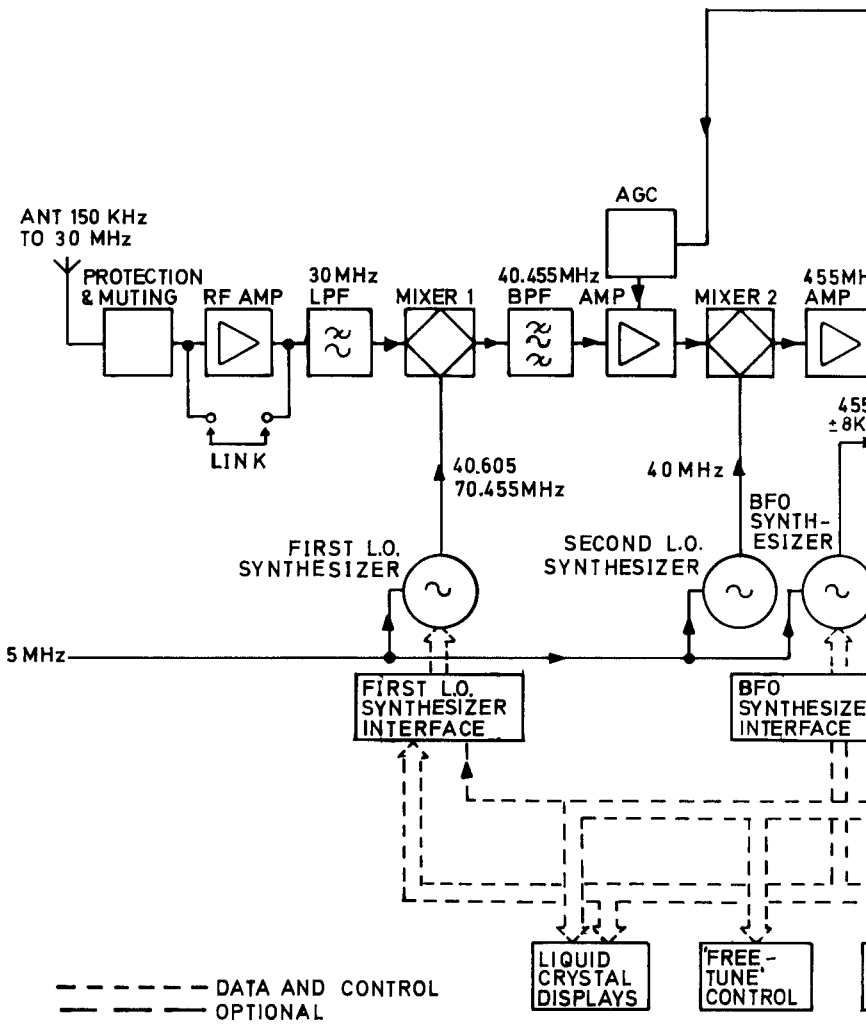
Overall View, RA 1792 Receiver

Fig.1-1


ANT 150 KHz
TO 30 MHz
PROTECTION
& MUTING
RF AMP
30MHz
LPF
MIXER 1
40.455MHz
BPF
AMP
AGC
MIXER 2
455MH
AMP
LINK
40.605
70.455MHz
40 MHz
BFO
SYNTH-
ESIZER
FIRST L.O.
SYNTHESIZER
SECOND L.O.
SYNTHESIZER
5 MHz
FIRST L.O.
SYNTHESIZER
INTERFACE
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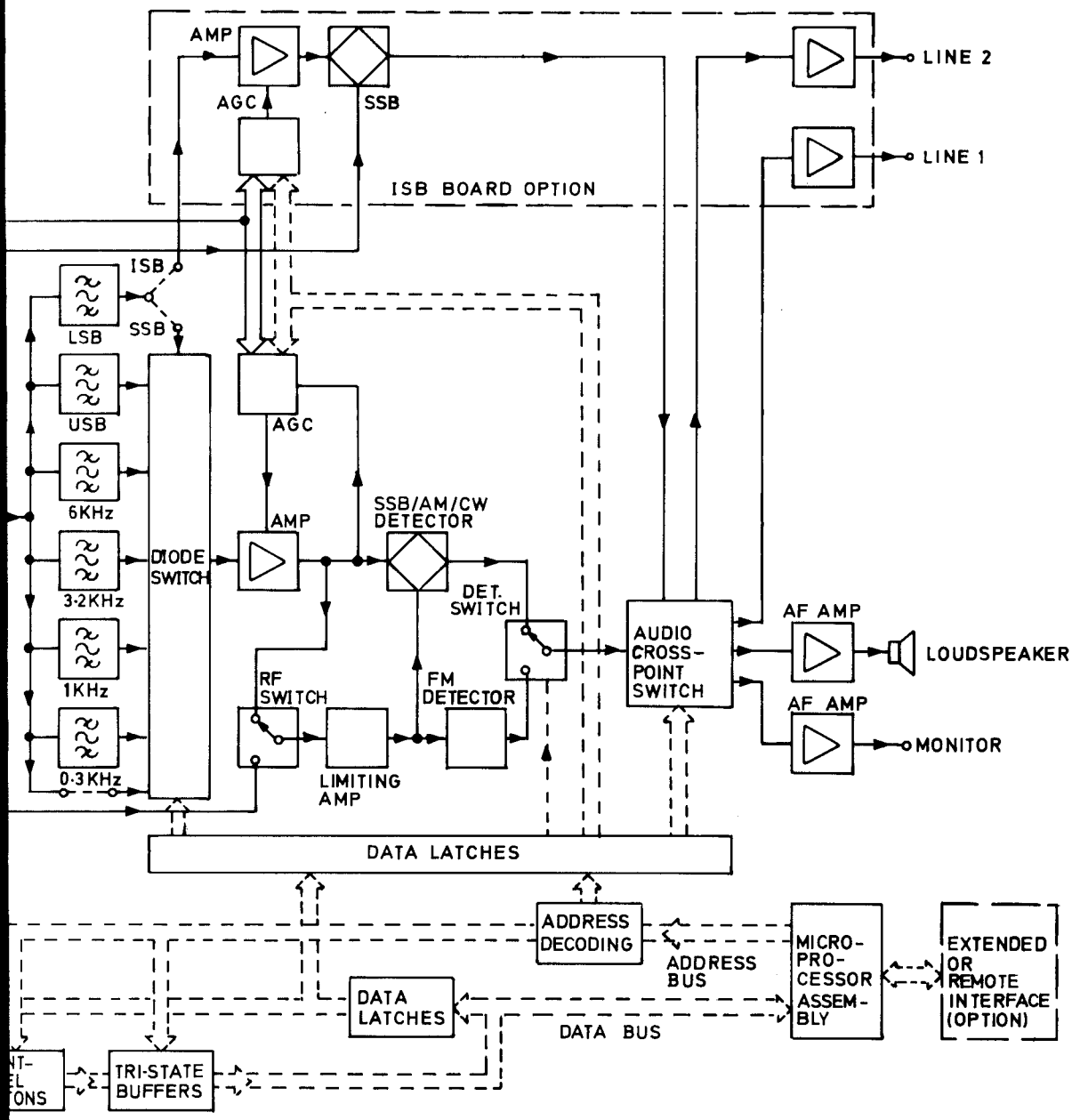
CRYSTAL
DISPLAYS
'FREE-
TUNE'
CONTROL
DATA AND CONTROL
OPTIONAL



Functional Block Diagram Fig.1.2

CHAPTER 2

INSTALLATION

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CHAPTER 2

INSTALLATION

INTRODUCTION

1 This chapter contains general installation data, detailed interface wiring requirements, and a brief initial checkout procedure. All interface connections are made to the rear panel of the receiver, as described in paragraphs 4 to 5. Figure 2-1 illustrates the rear panel connectors.

INSTALLATION DATA

2 The RA1792 Receiver is designed to be mounted in any standard 19 inch rack. Four mounting screws are required to secure the receiver to the rack. No special cooling consideration are required for the receiver; however, it should be positioned in the rack to permit convenient operation of the front panel controls.

3 The receiver is designed to operate with ac line voltages of 110, 120, 220, or 240 volts. The proper transformer wiring for the different voltages is accomplished with a 'programming card.' This card is located below the fuse on the rear panel. To change the receiver for operation with a different voltage simply disconnect the line cord from the receiver, slide the transparent cover to the left, then remove and reinsert the card so that the desired voltage is visible on the card. Refer to Figure 2-1 for the location of the programming card.

INTERFACE WIRING

4 All interface connections to the RA1792 receiver are made through the rear panel connectors. Figure 2-1 identifies the rear panel connectors and Tables 2-1 and 2-2 list the function and signal designations of the connectors.

5 After all interface wiring is complete, the initial check-out procedures described in paragraphs 6 to 16 should be performed to insure proper installation.

TABLE 2-1. REAR PANEL CONNECTORS

Reference Designation	Nomenclature	Function
J1	REF IN/OUT	Used in conjunction with switch S2 to accept an external reference source (S2 in EXT position) or to provide an output of the internally generated reference signal (S2 in INT position).
J2	MAIN IF OUTPUT	Receiver second IF output signal at 455 kHz.
J3	AF OUTPUT	25 pin 'D' type connector providing audio output signals. Refer to Table 2-2 for detailed listing of receiver connections.
J7	LO OUTPUT	When used, this connector provides an output of the receiver local oscillator frequency.
J9	ISB IF OUTPUT	When the receiver is equipped with the ISB option, this connector will provide an output of the ISB IF signal at 455 kHz.
A1J1	ANT INPUT	Receiver input from antenna.
A10J1	LINE	Connection for a.c. supply.
A6A1J1	-	Connector for external receiver control. Refer to the Appendix, located at the rear of the manual, for detailed wiring information.
-	GROUND	Grounding post used to connect receiver chassis ground to station ground.

TABLE 2-2. AF OUTPUT CONNECTOR WIRING

Pin	Signal Designation
1, 14	Line 1 Output, 600 ohm Balanced
2	Screen
3, 15	Line 2 Output, 600 ohm balanced
16	Screen
4, 17	Monitor Line Output
5	Monitor Line Output Ground
18	Loudspeaker Output
6	Loudspeaker Output Ground
19	Internal +12 Volt Output (200 mA maximum)
7	Internal +12 Volt Supply Ground
20	Mute Control Line Input
8	Mute Control Line Ground
21	DIV AGC Control Line Input
9	DIV AGC Control Line Ground
22	ISB DIV AGC Control Line Input
23	Scan Inhibit
10, 11, 12, 13, 24, 25	Not Used

INITIAL CHECK-OUT PROCEDURE

6 The following procedure may be used to insure that the receiver is operating properly and that the receiver has been properly installed. For detailed operating instructions, refer to the appropriate procedures contained in Chapter 3 of this manual.

CAUTION

Before attempting to operate the receiver, make certain that the programming card for voltage selection is properly inserted. (The selected voltage is visable on the top of the card). Refer to Figure 2-1.

7 Turn on the receiver by depressing the SUPPLY rocker switch. A random display may be present on both the frequency display and the mode display.

8 Depress the TUNE pushbutton. The TUNE indicator should be present in the frequency display and the tuning knob should be enabled. Use the tuning knob to select a known station. Spinning the knob at a fast rate will cause the frequency to change at a greater rate.

9 When the desired frequency is shown in the display, the TUNE pushbutton may be depressed a second time to disable the tuning knob.

10 Select the desired operating mode by depressing the AM, FM, CW, or sideband pushbuttons. In the AM, FM, and CW modes the desired bandwidth filter (BW1 to BW5) and the AGC (MAN, SHORT, MED, or LONG) operating mode may also be selected. The appropriate indicators will be displayed when the mode is selected.

11 In the CW mode, the BFO frequency may be changed by depressing the BFO pushbutton. The tuning knob may then be used to vary the BFO frequency as desired.

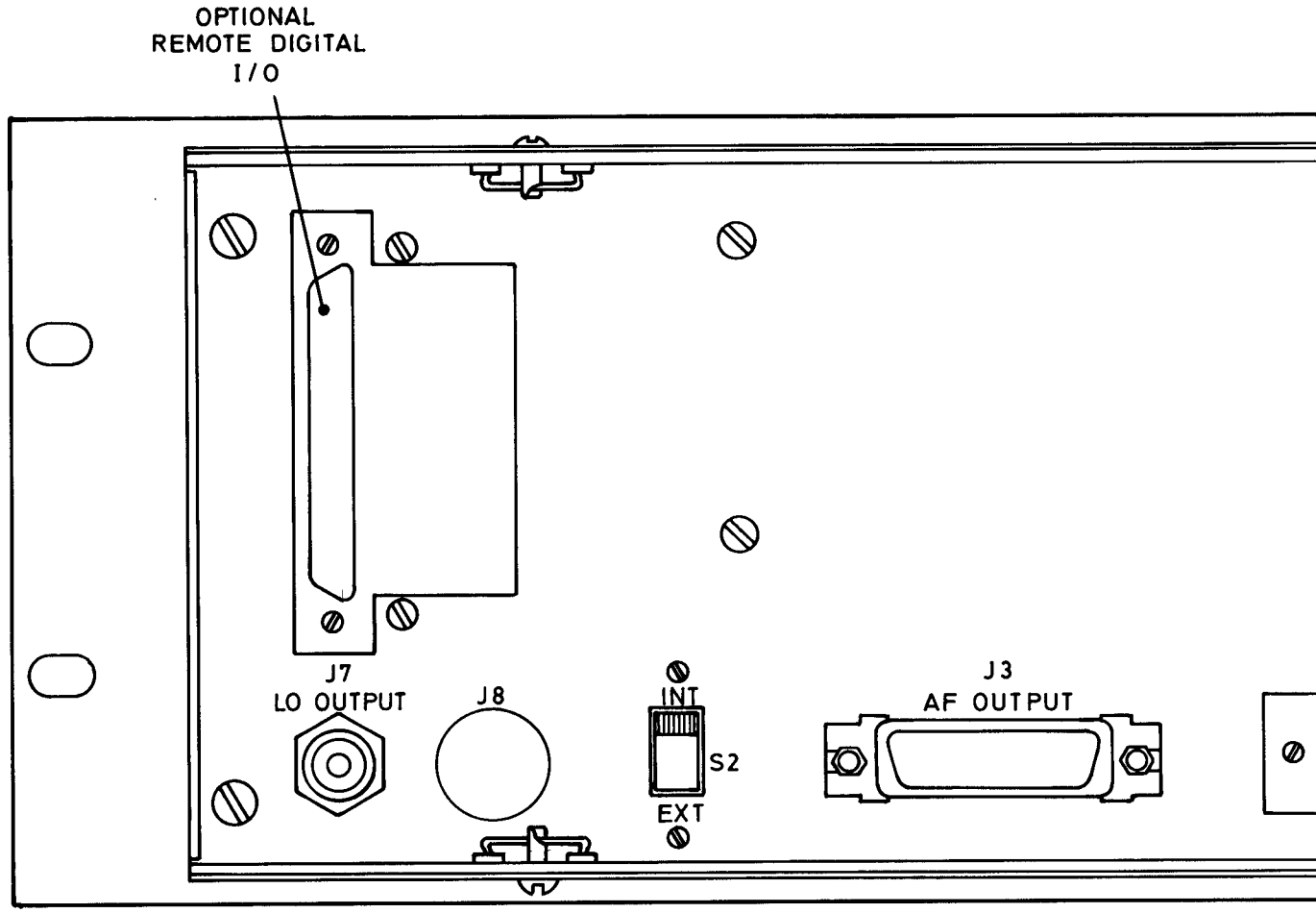
12 The front panel loudspeaker may be used by activating the L/S switch. When a headset jack is inserted in the PHONES jack the loudspeaker will be disabled. The VOLUME control is used for both the headphones and the loudspeaker.

13 The METER switch is used to display either the RF or the AF signal amplitude on the front panel meter. The IF GAIN control is used to adjust the IF signal amplitude if the MAN AGC mode is selected.

14 To select a station using the numeric keypad, depress the FREQ pushbutton. The frequency display will be set to all zeros, and an indicator will be present at the tens MHz digit. Use the numeric keypad to enter the desired tens MHz digit (0, 1, 2, or 3). Note that if a 3 is inserted, the receiver will not accept any additional digits since the maximum receiver frequency is 30 MHz. If a 0, 1, or 2 is entered, the indicator will move to the units MHz digit. After this digit (0 through 9) is entered the indicator will continue to step down to the 10 Hz digit. When the desired frequency is shown on the display, the ENTER pushbutton must be depressed to set the receiver to that frequency. The receiver mode, bandwidth, and AGC may be selected as described in steps 10 to 13.

15 The receiver may be turned off by depressing the SUPPLY rocker switch. When the receiver is turned back on, the receiver should automatically return to the last operating frequency and mode.

16 This completes the basic check-out procedure for the RA1792 receiver. Refer to the detailed operating instructions contained in Chapter 3 of this manual for additional instructions.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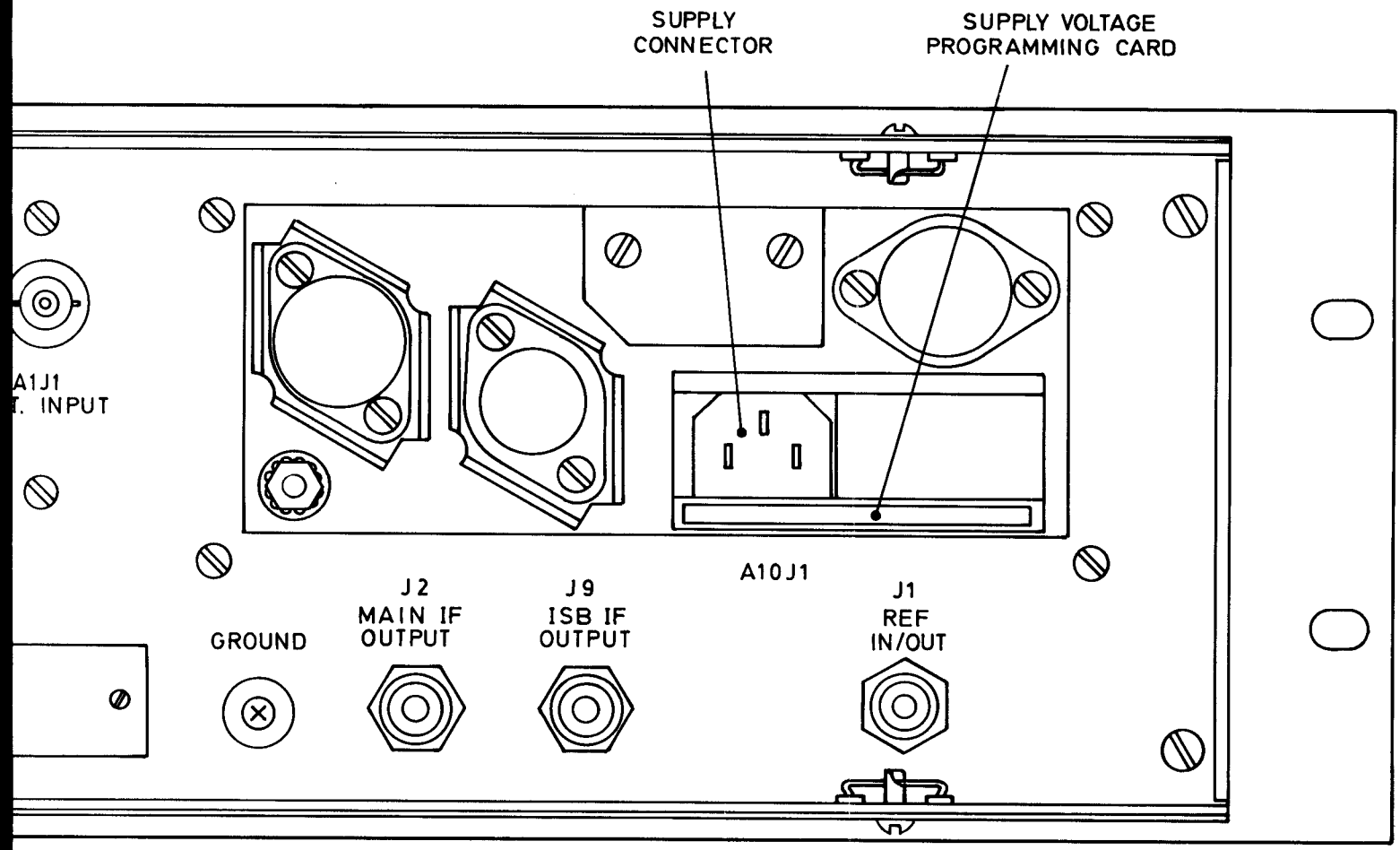
REMOTE DIGITAL
I/O
J7
LO OUTPUT
J8
INT
S2
EXT
J3
AF OUTPUT



RA1792: Rear Panel Fig.2.1

CHAPTER 3

OPERATION

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CHAPTER 3

OPERATION

INTRODUCTION

1 This chapter provides detailed instructions on the operating procedures associated with the RA1792 receiver. Paragraph 4 describes the function of the front panel controls and indicators; and paragraphs 5 to 37 contain detailed procedures for operating the receiver in the different modes.

2 Before attempting to operate the receiver, however, it is important to note that in some operating modes the receiver front panel is effectively independant from the receiver. That is, the receiver may be set to one station and will continue to receive that station even when the receiver front panel controls are set to a different frequency and operating mode. The receiver will not be switched to the 'new station' until the appropriate pushbutton is depressed. Additionally, the entire contents of the memory (100 channels) may be reviewed or modified, if desired, without affecting the receiver operation.

3 A second significant point is that some pushbuttons are used for more than one function. For example, the numeric keys (0 through 9) are used to enter five different levels of data into the receiver, as follows:

Level 1: Numeric Value of desired operating frequency
Level 2: Bandwidth and AGC mode selection
Level 3: Numeric Value of selected channel
Level 4: Scan Parameters (channels to be scanned and time duration for each channel)
Level 5: Automatic test mode parameters.

The desired level is selected by depressing one or more of the control pushbuttons.

OPERATING CONTROLS AND INDICATORS

4 The controls and indicators located on the front panel of the RA1792 receiver are shown in Figure 3-1 and listed in Tables 3-1 and 3-2. Figure 3-1 shows all indicators illuminated at the same time. In actual operation, however, only one or two indicators of a particular group would be illuminated at the same time.

TABLE 3-1. FRONT PANEL CONTROLS

Nomenclature	Function
SUPPLY	Rocker switch used to supply operating voltage to receiver.
TUNE	Pushbutton used to select tune mode. In this mode the tuning knob is used to select the operating frequency of the receiver.
BFO	Pushbutton used to enable BFO tuning mode. In this mode the tuning knob is used to vary the BFO frequency.
REM (Remote)	Pushbutton used to place the receiver under the control of a remote device.
Tuning Knob	Rotary knob used to select receiver operating frequency, BFO frequency, or channels (00 to 99). In the frequency mode the tuning control provides a continuously variable rate of change according to the speed at which it is turned. For example, if the knob is turned slowly, the receiver frequency may be easily tuned in 10 Hz increments. If the knob is turned rapidly (or spun) the rate of change per revolution will be much higher.
0 to 9, BW1 to BW5, MAN, SHORT, MED, LONG, AUX. (Numeric Keypad)	These ten pushbuttons are used along with other pushbuttons to enter the desired information into the receiver. When the FREQ pushbutton is depressed, the numeric value of the desired operating frequency may be entered. After the frequency has been selected the bandwidth may be selected (BW1 to BW5) and the AGC mode (MAN, SHORT, MED, LONG). The AUX pushbutton is used to recall a particular preset operating mode. The numeric keys are also used to select channels, change the time duration during a scan operation, and to enter test numbers during an automatic test operation.
STORE	This pushbutton is used to load all operating parameters into a specific memory location.
ENTER	This pushbutton is used to set the receiver to the operating parameters shown on the front panel when coming from the front panel monitor mode; and it is also used after the FREQ pushbutton has been activated, to enter the new frequency displayed.
FREQ (Frequency)	This pushbutton is used to enable the numeric keys to enter a specific operating frequency, in conjunction with the ENTER pushbutton.
CHAN (Channel)	This pushbutton is used to set the receiver to the channel mode.
RCL (Recall)	This pushbutton is used to set the receiver to the previous frequency and operating mode, before the ENTER pushbutton is depressed.
SCAN	This pushbutton is used to set or remove a scan flag from a particular channel. It is also used to set the receiver to the scan mode.

TABLE 3-1. FRONT PANEL CONTROLS (Cont.)

Nomenclature	Function
ISB, LSB, USB	These three pushbuttons are used to set the receiver to operate in the sideband mode. The ISB pushbutton will cause the receiver to switch between the LSB and USB mode each time the pushbutton is depressed. The LSB and USB pushbuttons are used to set the receiver to the lower or upper sideband operating mode.
AM	This pushbutton is used to set the receiver to the AM mode.
CW	This pushbutton is used to set the receiver to the CW mode. The BFO frequency is variable only when the receiver is set to this mode.
FM	This pushbutton is used to set the receiver to the FM operating mode.
IF GAIN	This control is used to manually set the IF gain level when the Manual AGC operating mode is selected. This control may also be used in conjunction with the Short, Medium, and Long AGC operating modes to set the receiver agc threshold.
VOLUME	This control is used to adjust the amplitude of the audio signal applied to the front panel loudspeaker and phones jack.
METER	This rocker switch is used to set the front panel meter to display either the AF audio level or the RF signal level.
L/S	This rocker switch is used to enable or disable the front panel loudspeaker.

TABLE 3-2. FRONT PANEL INDICATORS

Nomenclature	Function
CHANNEL 88	Indicates the receiver is set to the channel mode. The two digits below the channel indicator represent the channel designation (00 to 99).
⚠	Indicates that the receiver is operating independent of the front panel.
SCAN	Indicates that the receiver is set to the scan mode (if the ⚠ is not illuminated) or that the channel currently shown has a scan flag set (if the ⚠ is illuminated).
FREQUENCY, kHz 28 888.88	Indicates the frequency, in kHz, that the receiver is set to.

TABLE 3-2. FRONT PANEL INDICATORS (Cont.)

Nomenclature	Function
REMOTE	Indicates that the receiver is set to the remote control mode.
TUNE	Indicates that the receiver is set to the tune mode (front panel tuning knob is used to select the desired frequency).
BFO + 8.00 kHz	Indicates the BFO frequency.
AF - dBm RF - dB μV	Front panel digital meter indicates the audio level in dBm or the RF level in dB μV. The METER switch is used to select the meter function.
BW 6.0 kHz	Indicates the IF bandwidth selected.
AUX	Indicates that the preset auxiliary receiver detection mode has been selected.
MAN, SHORT, MED, LONG	Indicates the selected AGC mode. When two indicators are displayed (MAN, SHORT) it indicates that the receiver is set to operate with a variable agc threshold.
ISB, LSB, USB, AM, CW, FM	Indicates the receiver operating mode.

OPERATING PROCEDURES

5 The following paragraphs 6 to 37 describe the different operating modes associated with the receiver. It is recommended that all procedures associated with operating the receiver be reviewed in their entirety before attempting to operate the receiver.

Frequency Selection

6 The receiver frequency may be set either with the tuning knob or with the numeric keypad. To use the tuning knob, depress the TUNE pushbutton and spin the tuning knob in either direction to increase or decrease the frequency. Note that in this mode the receiver is under the direct control of the front panel. To disable the tuning mode, or lock the receiver to the selected frequency, the TUNE pushbutton is depressed a second time. To select a frequency using the numeric keypad, depress the FREQ pushbutton and enter the tens MHz digit (0, 1, 2 or 3). If a 3 is entered, the receiver will block any additional digits since the maximum receiver frequency is 30 MHz. If a 0, 1 or 2 is entered the digit indicator will move to the right as each digit is entered. In this mode, the front panel is operated independantly from the receiver. To set the receiver to the selected frequency depress the ENTER pushbutton.

Mode Selection

7 The receiver operating mode, FM, CW, AM, or sideband, is selected by depressing the appropriate pushbutton. The corresponding indicator will be illuminated in the display. In the FM, CW, and AM modes, the bandwidth and AGC operating mode may also be selected (see paragraphs 9 to 11). In the sideband mode the AGC mode may be selected as described in paragraphs 10 and 11. A BFO frequency may be used when the receiver is operated in the CW mode. This procedure is described in paragraph 12.

8 The bandwidth and AGC operating parameters may be preset, for each mode so that the receiver will automatically return to the selected parameters each time the mode is selected. Additionally, when using the AUX mode, the mode, bandwidth, AGC, and BFO parameters may be preset so that the receiver will return to these parameters each time the AUX mode is selected. Refer to paragraph 36 for detailed procedures on presetting these parameters. The ISB pushbutton can be used only when the receiver is equipped with the ISB option.

Bandwidth Selection

9 A total of 5 different IF bandwidths may be selected when the receiver is operated in the FM, CW, or AM modes. The desired bandwidth is selected by depressing the appropriate pushbutton (BW1 to BW5). The display will indicate the bandwidth in kHz.

AGC Selection

10 The receiver may be set to operate with a Short, Medium or Long agc time constant by pressing the appropriate pushbutton (SHORT, MED, or LONG). If MAN is pressed the receiver operates with a variable agc threshold, adjusted with the IF GAIN control and the agc time constant indicated. To disable the agc, after pressing MAN. the time constant previously selected may be cancelled by pressing the appropriate button (SHORT, MED. or LONG). The IF GAIN control now acts to set the receiver gain.

11 To return to agc operation, pressing MAN. disables the IF GAIN control and selects SHORT agc.

BFO Tuning

12 In the CW mode, the internal beat frequency oscillator is enabled. The frequency range of the oscillator is ± 8 kHz in 10 Hz increments. When the BFO pushbutton is depressed the tuning knob may be used to select the desired BFO signal. The BFO pushbutton must be depressed a second time to disable the tuning knob from the BFO tuning mode.

Channel Loading

13 Each of the 100 channels in the receiver may be preset to a particular frequency and operating mode. The following procedure details the steps required to load each of the channels.

14 Depress the FREQ pushbutton. The frequency indicator will be illuminated and the display set to all zeros.

15 Enter the desired frequency using the numeric keypad.

16 Select the desired mode, bandwidth, AGC, and BFO parameters. Verify the selected parameters by observing the display.

17 Press and hold the STORE pushbutton. Enter the desired channel number with the numeric keypad (10s digit first followed by 1s digit).

18 Release the STORE pushbutton. This will cause the frequency and mode data shown on the front panel to be written into the indicated channel.

19 At any time while operating the receiver, the current operating parameters may be stored using the procedure in paragraphs 17 and 18.

Memory Check

20 The contents of memory may be verified or checked at any time simply by depressing the CHAN pushbutton and turning the main tuning knob to select the desired memory channel. This procedure will not affect the operation of the receiver.

Memory Transfer

21 The contents of one memory location may be transferred to another memory location by depressing the CHAN pushbutton and using the main tuning knob to locate the channel to be transferred. Depress and hold the STORE pushbutton and use the numeric keypad to select the new memory location. The information shown on the front panel will be written into the new memory location when the STORE pushbutton is released.

Manual Scan Operation

22 After the operating data has been entered into the channels, the channels may be manually scanned by depressing the CHAN and ENTER pushbuttons. By turning the main tuning knob, the receiver will be set to the operating parameters contained in each channel.

Automatic Scan Operation

23 For automatic scan operation, the 100 channels in the receiver are divided into 10 groups of 10 channels each (channels 00 to 09, 10 to 19 etc.). The receiver will automatically scan each channel in a selected group that has asserted its scan flag. The following procedure details the steps necessary to initiate the automatic scan sequence.

24 Review the channels to be scanned by depressing the CHAN pushbutton and using the main tuning knob to check the operating parameters on each channel.

25 The receiver will scan only the channels where the scan flag is asserted; as indicated by the SCAN display just below the channel number.

26 The scan flag is asserted or deleted by depressing the SCAN pushbutton.

27 After all channels have been checked, use the numeric keypad to enter any channel number of the group to be scanned (00, 10, 20 etc.).

28 Press the ENTER pushbutton. This will set the receiver to the selected channel.

29 Press the SCAN pushbutton to initiate the automatic scan sequence. The receiver will scan each channel in the selected group with the scan flag asserted. The time duration that the receiver spends on each channel may be varied from approximately 100 milliseconds to 10 seconds. The desired time interval is selected during the scan operation, with the numeric keys. Depressing 0 will result in a 100 millisecond scan, 1 will result in a somewhat longer scan, and so on. Depressing 9 will result in the maximum scan interval, or 10 seconds.

30 The automatic scan sequence may be stopped by depressing the SCAN pushbutton. Depressing the SCAN pushbutton a second time will initiate the automatic scan operation again.

31 A SCAN INHIBIT input is provided on the rear panel of the receiver (J3, pin 23). The scan sequence may be stopped at any time by earthing this input. Removing the earth will cause the scan sequence to re-start providing SCAN is still selected on the front panel.

Recall Operation

32 The recall operation is used to reset the display to the operating mode of the receiver. For example, the receiver may continue to receive one station while the front panel portion of the receiver is used to check memory status, update the memory etc. Depressing the RCL pushbutton will cause the front panel to display the operating parameters of the station being received.

Preset Mode Parameters

33 To preset the mode parameters the dil switch S1a on the A9A2 board must be set to the 'closed' position. Refer to Figure 3-2 for the position of this switch. To preset the AUX mode, first select the desired mode, bandwidth, agc time constant and bfo offset (e.g. CW, 1 kHz, medium, +1.5 kHz). Depress the AUX button to store these parameters as the AUX mode.

To preset the sideband modes select ISB LSB, ISB USB, LSB, USB in turn together with the desired agc time constant. Different time constants may be selected for the two sidebands on ISB, if desired.

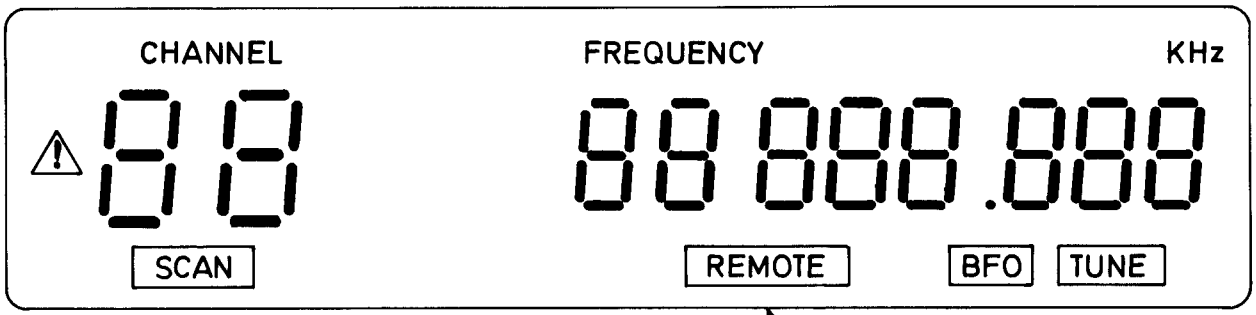
To preset the other modes select AM, FM, CW in turn together with the desired agc time constant, bandwidth and bfo offset (for CW only).

Return the dil switch S1a on the A9A2 board to the 'open' position.

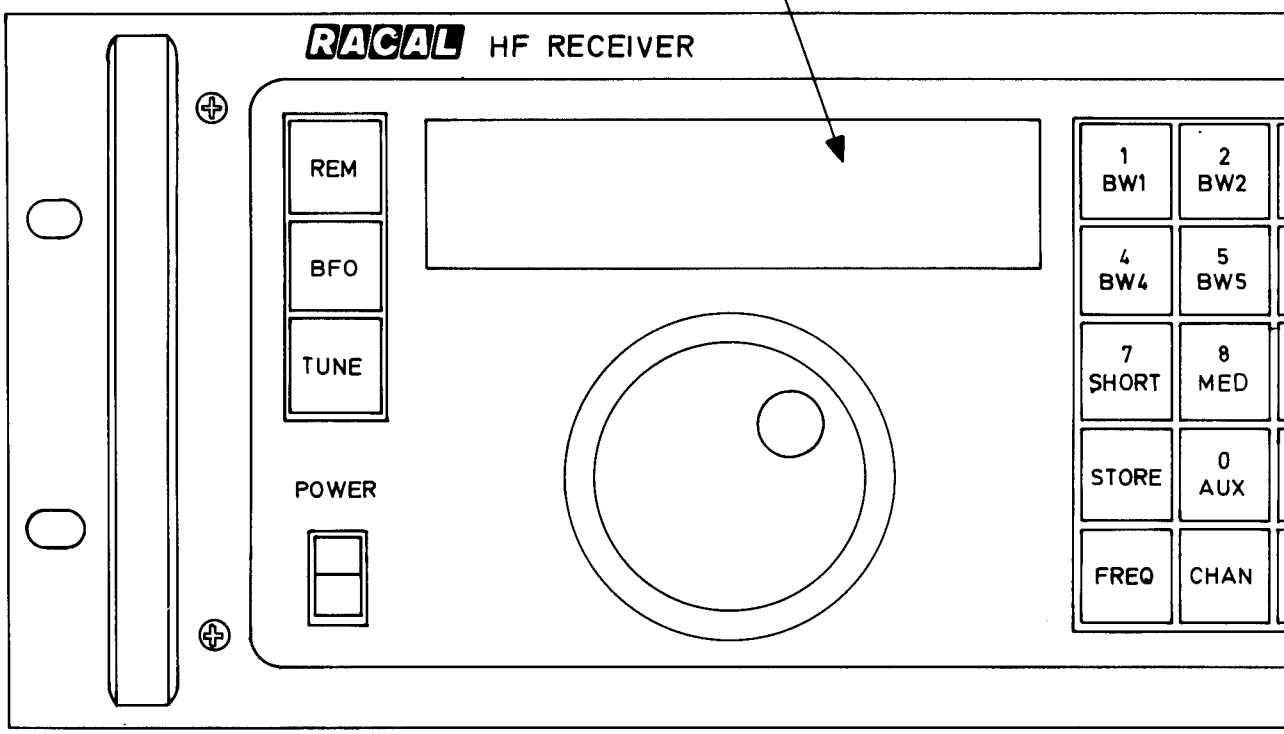
The preset parameter will now be recalled each time a mode is selected but may be changed by the operator using the procedure described in paragraphs 7-12.

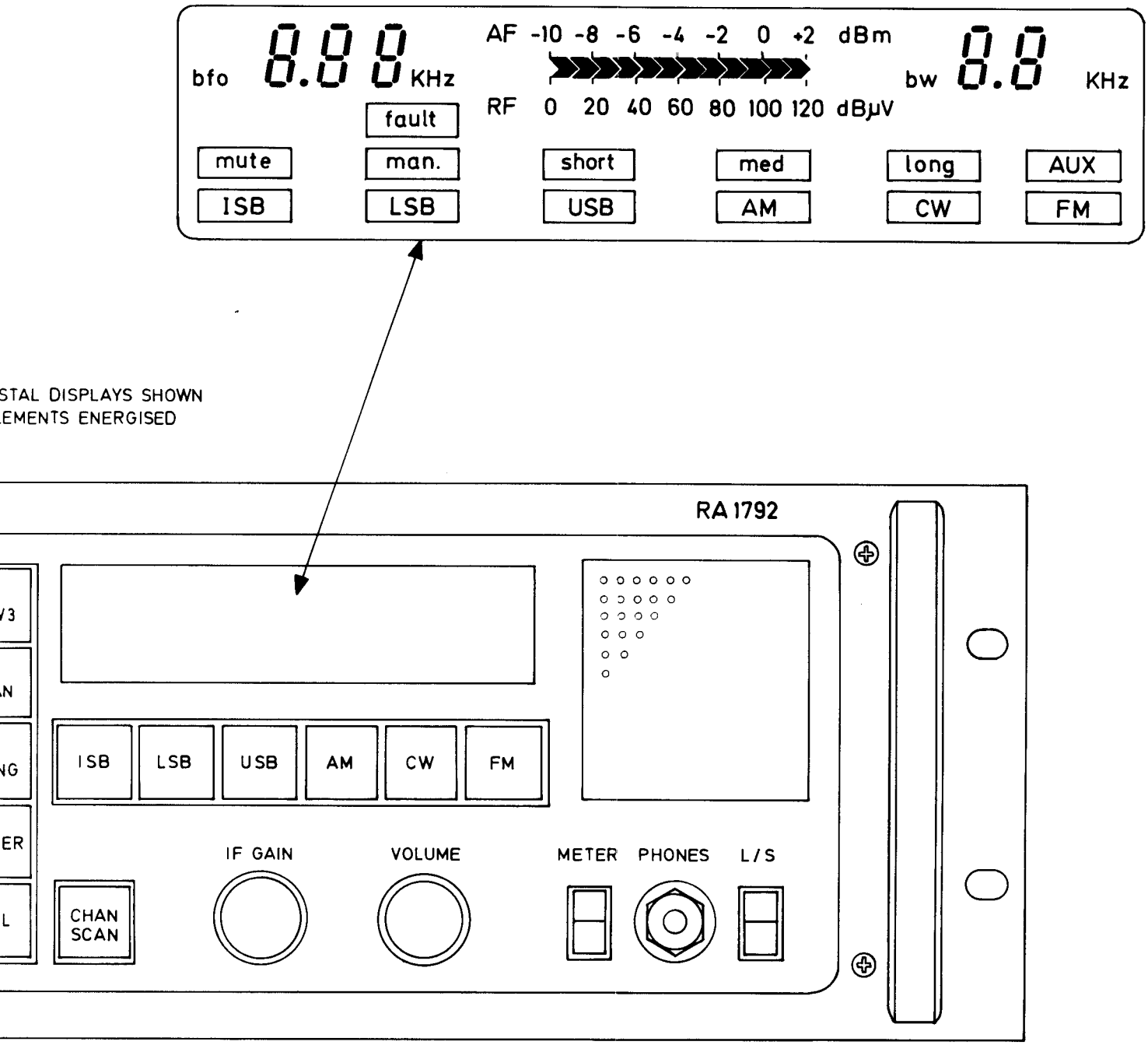
Operation without Preset Mode Parameters

34 If it is required that the agc time constant, bandwidth and bfo offset do not change when a new mode is selected, the receiver may be operated with the dil switch S1a on A9A2 permanently in the 'closed' position. Note, however, that the AUX mode cannot be used in this case.



NOTE: LIQUID
WITH AL



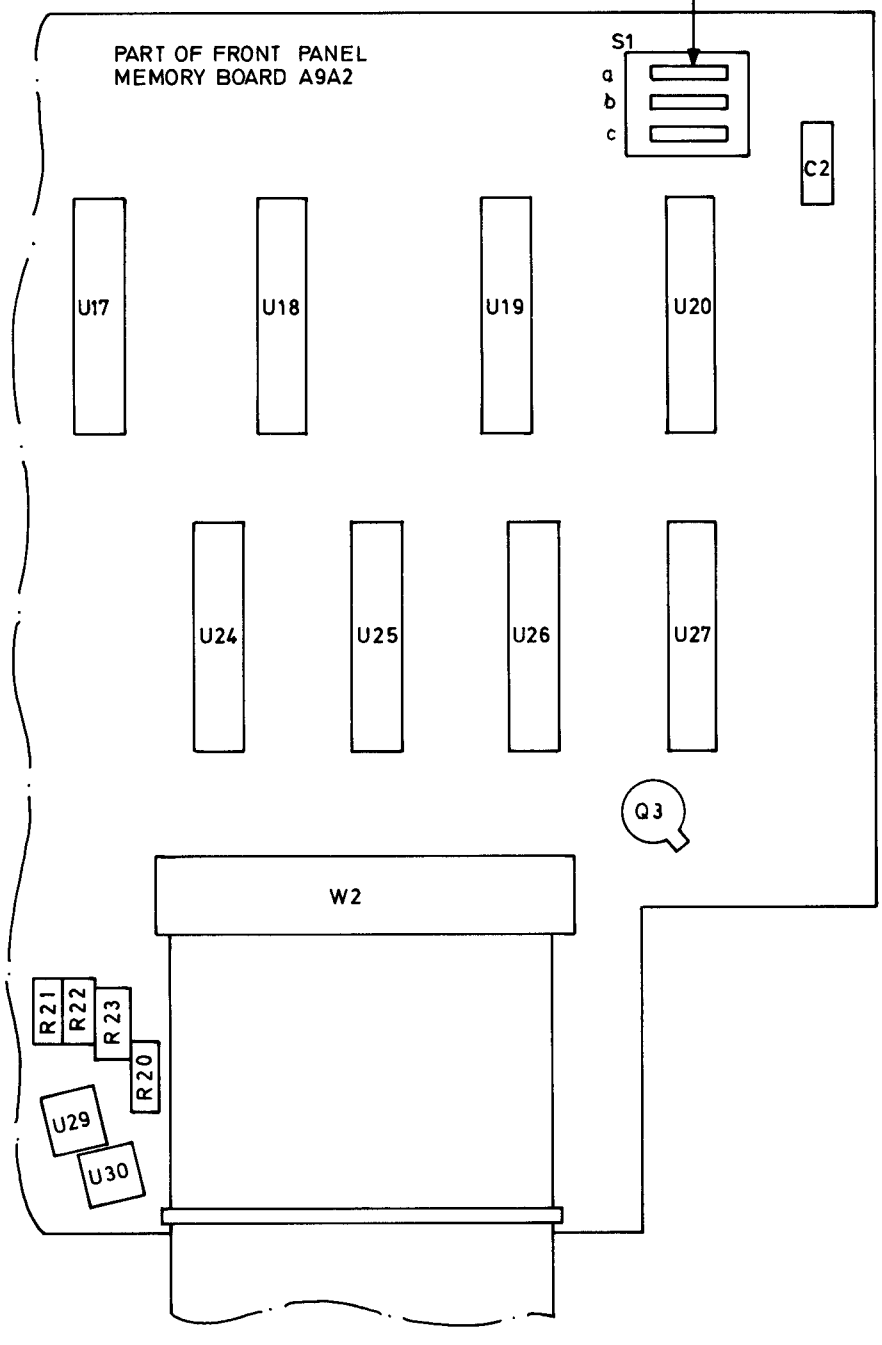


Operating Controls
and Indicators

Fig.3.1

CONTROL SWITCH S1

	OPEN	CLOSED
S1a	NORMAL	PRESET MODE
S1b	NORMAL	SELF TEST
S1c	NOT USED	



RACAL
TH1496

Control Switch S1 Location

Fig.3.2

CHAPTER 4

PRINCIPLES OF OPERATION

CONTENTS

ILLUSTRATIONS

CHAPTER 4

PRINCIPLES OF OPERATION

INTRODUCTION

1 This chapter describes the principles of operation for the RA1792 HF Communications Receiver. Figure 4-1 is an overall functional block diagram for the receiver which may be divided into four major sections. The RF/IF/AF section, the frequency synthesizer, the display and front panel section, and the power supply. The chapter has been arranged to cover these sections in that order.

RF/IF/AF SECTION

2 The RF/IF/AF section comprises the rf amplifier/low pass filter A1, the first mixer A2, the second mixer A3, and the second IF/AF assembly A4. The input to the RF/IF/AF section is received at the RF IN connector A1J1.

RF Amplifier/Low Pass Filter, A1

3 The incoming RF signal is passed from the antenna connector A1J1 through a protection circuit, an optionally connected RF amplifier and then through a 4-section elliptical low pass filter which has a cut-off frequency of 35 MHz. The RF amplifier may be connected or by-passed by linking. The filter provides the necessary protection to the receiver, from image signals at frequencies between 81.4 and 111.4 MHz; and from signals at the first intermediate frequency of 40.455 kHz. The filter also prevents first local oscillator reradiation from the antenna connection. The circuit diagram is shown in Figure 8-1.

4 The RF amplifier consists of transistor stage Q2-Q3. Linking E7 to E10 by-passes the amplifier. Linking E7 to E8 and E9 to E10 connects the amplifier between the input and the low pass filter.

5 Q1 is normally conductive, holding relay K1A closed. A MUTE input to A1J1 pin C will turn off Q1 opening the relay to disconnect the antenna input from the following stages of the receiver. A signal of greater than 5V rms approximately will also turn off Q1 and open the relay, thus protecting the receiver from large input signals.

First Mixer, A2

6 Figure 4-2 is a simplified block diagram of the first mixer module A-2. It consists of a signal low pass filter, first mixer, roofing filter, first IF amplifier and drive amplifier with its associated filters. The function of this module is to convert the incoming RF signal to the first intermediate frequency of 40.455 MHz, by mixing with the local oscillator frequency 40.605 to 70.455 MHz derived from the synthesizer. The circuit diagram from the first mixer is shown in Figure 8-2.

Signal Low Pass Filter and Mixer

7 The output of the A1 module is connected to the first mixer through a 2 section elliptical low pass filter which has a cut-off frequency of 35 MHz. The mixer consists of T1, Q2, Q3, Q4, Q5 and T3. The mixer output (from T3) is connected directly to the roofing filter FL1 which selects the 40.455 MHz mixing product. The 3 dB bandwidth of this filter is 16 kHz, and defines the widest bandwidth available in the receiver.

Drive Amplifier

8 The mixer drive amplifier comprises transistors Q1, Q6 and Q7. The local oscillator signal from the filter, which may be monitored at TP2, is coupled to the base of amplifier Q1. The output of Q1, which may be monitored at TP3, drives the differential amplifier stage Q6 and Q7. The output of this stage, through transformer T2, is the LO input to the mixer.

Output Amplifier

9 The mixer output, through filter FL1 and impedance matching transformer T4, drives the high linearity amplifier stage Q8. The output to the following second mixer stage (through A2J3) is taken from a tap on transformer T5, which is in the load circuit of Q8.

First IF AGC

10 The AGC input, through A2J2 pin 6, controls the current through the gain control diode CR1. Thus, the AGC input controls the load impedance and consequently the gain of Q8. The bias signal, through A2J2 pin 5, controls the bias on Q8. This varies the bias as the gain is varied (by the AGC input) so that sufficient current flows through Q8 to assure high amplifier linearity.

Second Mixer, A3

11 The second Mixer, A3, contains three amplification stages, filtering and a mixer. The circuit is shown in Figure 8-3.

12 Figure 4-3 is a simplified block diagram of the second mixer. The 40.455 MHz first IF output from the first mixer is amplified and applied through a 40.455 MHz bandpass filter to a balanced mixer where it is mixed with the 40 MHz output from the LO/BFO synthesizer board. The second IF is produced by selecting the 455 kHz difference frequency at the output of the mixer.

13 The output signal level from the first stage of IF amplification is controlled by the AGC input from the main IF/AF board. The output from the second stage of IF amplification is applied to the balanced mixer through a 40.455 MHz band pass filter. The 455 kHz difference frequency at the mixer output is filtered and amplified before being applied to the MAIN IF/AF module A4.

Amplifier Stage

14 The 40.455 MHz first IF output from the first mixer is applied to an amplifier stage, Q1 via board pin E1 and C3. The amplified output from the Q1 load transformer T1 is applied via C9 to a second amplifier stage, Q2.

Second IF AGC

15 The AGC voltage input, coming in through A3J1 pins 2 and 4, is applied to a circuit consisting of U2A, U1A, B, C which converts a linear voltage charge to a logarithmic current charge to drive pin diode CR1. The diode controls the gain of amplifier Q1. This circuitry is similar to that described in paragraph 10.

16 The AGC current drive for the first mixer is derived from stage U1D and comes out of A3J1 pin 6, while the bias signal for the first mixer is derived from stages U2B and U2C and comes out of A3J1 pin 3.

Mixer

17 The first IF signal from Q2 is applied to the signal port of the mixer U3 via a four section band pass filter tuned to 40.455 MHz. The 40 MHz second LO signal from A8 is applied via J2 to the mixer oscillator port. The difference signal at 455 kHz is selected at the mixer output by the tuned transformer T2 and the ceramic bandpass filter FL1. The output amplifier U4 provides a low impedance signal feed to the MAIN IF/AF module A4.

Main IF/AF Module A4

18 The Main IF/AF module A4 contains the 455 kHz filters used to determine the reception bandwidths, the second IF amplifier, the AM, FM, and Product detectors with associated AF power amplifiers, together with the IF output and AGC circuits.

19 Solid state switching circuits are also included for filter selection, detector selection, AGC time constants, remote gain control and signal level monitoring.

20 Provision is also made for the necessary signal and control inputs to the optional ISB IF/AF module A5 when this faciltiy is required.

21 Figure 4-4 is a simplified diagram of A4 and figure 8-4 is the circuit diagram.

IF Filters

22 The main IF/AF module will accommodate up to seven filters, five of these are normally symmetrical filters and two are sideband filters. When the 16 kHz bandwidth is selected these filters are bypassed and an attenuator is switched in to compensate for gain changes. When the 3 kHz bandwidth is selected the USB filter FL2, is switched in and the 1st LO synthesizer and bfo are offset by 1.7 kHz to make the USB filter appear symmetrical about the receiver frequency (unless optional 3 kHz symmetrical filter is fitted).

23 Filters are selected by the binary coded logic inputs to A4J2 pin 35 (DB0), pin 31 (DB1), pin 33 (DB2) and pin 37 (DB3). These logic inputs are applied through voltage level shifter, U3, to a latch, U2, and then to the one of eight decoder, U1. The latch is set or clocked by the input to A4J2 pin 29 (OP3C) through the level shifter, U16. The outputs from U1 and the output from pin 1 of the latch, U2, selects the appropriate filter by applying a +15 volt bias to the diode switch to select a filter and 0V to switch off the other filters.

24 The output of filter FL1, when selected, may be sent to the main IF/AF signal path or the ISB IF (through J3 out) path (in the optional A5 card) by connection of link LK1 for the SSB or ISB mode.

Input Amplifier

25 The source impedance of the signal from the selected filter is transformed from 5K ohms to about 200 ohms by Q1 and the signal is then applied to an integrated circuit gain-controlled amplifier, U8. This device contains two amplifier sections which are connected in cascade to provide high gain and AGC range. The input signal is applied via C33 to pin 1, and the output from the first section, at pin 12, is applied via R39 and C40 to the input of the second section at pin 10. The output taken from pin 7 is applied via a bandpass filter to an emitter follower, Q6 and also to the IF output amplifier composed of Q7, Q8, Q9, and from there to the back panel IF OUT jack, J4 at a level of 100 mV.

26 AGC is applied to both sections of U8 via pins 3 and 4, thus providing a control range of approximately 60 dB. The three terminal regulator U6 serves to stabilize the supply of U8 at 12 volts.

SSB Detector

27 The IF output from U8 and the bandpass filter is fed via emitter follower stage Q6 to the IC product detector U20. The BFO (455 + 8 kHz) signal from A8 is also fed to U20 via A4J5, the RF switch (CR22-CR25), when selected in other than the AM or FM modes, and U18. J6 out supplies a similar BFO signal to the optional A5 ISB module. The resulting beat difference output frequency at AF from U20 pin 6 is fed to the FET switch, U19A. The BFO output, through the RF switch, is selected by the binary coded logic input to A4J2 pin 39 (DB6).

AM Detector

28 In the AM, FM mode, the binary coded logic input to A4J2 pin 40 (DB7) allows the RF switch to pass the IF signal from Q6, through CR25 into limiter amplifier U18. The output from pin 10 of U18 feeds the carrier input, pin 8, of AM detector module U20. The IF input, from Q6 is also fed into the signal input, pin 1 of U20. The detected AF output from pin 6 is fed to the FET switch U19A.

FM Detector

29 In the AM, FM mode U18 also performs FM detection on the IF input (through the RF switch) yielding the AF output from pin 1 which is fed to the second input of the analogue switch, 19A.

Detector Selection

30 The required signal detector is selected by the application of a binary coded logic input to A4J2 pin 33 (DB2), through U3 and U23 (providing voltage level shifting and latching) which drives the analogue switch U19A. The latching of U23 is clocked by the OP3F input to A4J2 pin 25.

Audio Frequency Stages

31 An audio cross point switch, U25, is used to switch the detected audio from the main IF/AF and ISB IF/AF boards to the appropriate audio outputs (the Loudspeaker and monitor line outputs on the main IF/AF board and the LINE 1 and LINE 2 outputs on the ISB IF/AF board). In a receiver without the ISB option only one line output is provided (the monitor line) and the line level is adjusted using R129. In an ISB receiver there are three line outputs, all of which carry the same signal except when an ISB mode is selected. In this case the upper sideband is fed to the LINE 1 output and the lower sideband to the LINE 2 output. The signal at the monitor line output depends on the sideband selected for monitoring on the front panel. R129 adjusts the level on LINE 1 and R132 adjusts the level on LINE 2. The output on the monitor line is equal to that on the line being monitored. Switching of the cross point switch is controlled by the microprocessor data bus.

32 A dual audio amplifier, U26 provides the loudspeaker and monitor line outputs. The input to the loudspeaker amplifier is set by the VOLUME control mounted on the front panel.

AGC Detector and Amplifier Stages

33 The IF signal from the emitter follower Q6 feeds the U10 transistor array connected as a detector. U10B compensates the bias of U10C for temperature changes. The output from U10C feeds the AGC integrator U14A through one of two paths (Q4 controlled on or off by Q5 or U7C in series with switch U11B), dependant on whether carrier or peak signal AGC is selected. Q5 is controlled by the binary coded logic

input into A4J2 pin 39 (DB6) through U5 and U15. U11B switch is controlled by binary coded logic input into A4J2 pin 38 (DB5) through U5 and U15. Latch U15 is clocked by the OP3D input to A4J2 pin 27. The output from the integrator U14A goes through the AGC filter, which is set for carrier or peak signal AGC through U12C. The filtered output goes through stage U17B and on to control the gain of the IF AGC amplifier, U8. This output also goes on to stage U17D, where it is combined with the ISB AGC input (from A4J8 pin 1 through stage U17C). The output of this stage goes out of A4J2 pin 34 to the second mixer module, A3.

34 Three alternate AGC time constants are provided together with AGC 'hang' and 'dump' capabilities. These time constants are selected by the appropriate parallel combination of R52. R53 and R55, R53 and R55 are switched in or out by FET switches U11A and U12A. The switches are controlled by the binary coded logic inputs (through latch U13) on A4J2 pins 31 (DB1) and 35 (DB0). U12A ON selects short, U11A ON selects medium and both OFF select the long time constant. Latch U13 is clocked by the OP3D input to A4J2 pin 27.

35 When selected, the AGC 'hang' circuit disconnects R52, R53 and R55 from the decay circuit by cut-off of transistor U10D. This transistor is driven by 'hang' circuit stages U7A and U7B. Capacitor C42, through U7A, charges when a large enough signal is received from the AGC detector. The voltage on C42, through U7B, cuts off U10D when the signal is removed. This causes the AGC to 'hang' until C42 discharges. Transistor Q2, connected across C42, disables the 'hang' circuit when switched into the conducting state by the binary coded logic signal from A4J2 pin 38 (DB5) through U4 and U5. Latch U4 is clocked by the OP3C input to A4J2 pin 29.

36 When a 'dump' command is received at U4 pin 1 the Q output of U9A is clocked to a '1' turning on U10c and U12d. This causes the agc voltage to decay rapidly until comparator U7a detects a signal at the IF output. This resets U9A and turns off U10e and U12d.

Manual/Remote IF Control

37 When Manual gain selected, FET switches U12B and U11C are turned ON by the binary coded logic inputs to A4J2 pins 36 (DB4) and 37 (DB3) through latches U15 and U13. This allows the IF gain control voltage from the front panel (through A4J2 pin 22) to set the gain through stages U14C and U14A. Latches U13 and U15 are clocked by the OP3D input at A4J2 pin 27.

38 The output of the DAC, U21, is used to control the receiver gain when the receiver is under remote control by switching on U11d. The DAC voltage is stored by the sample and hold circuit consisting of U14C, U11d, R71 and C54 while the DAC is performing the receiver metering functions. When the receiver is under agc control the DAC is used to hold the output of U14C at 0V and also to set the agc voltage on TP9 to 10V when no signal is present.

Meter Circuits

39 The main IF agc, ISB IF agc and detected AF level are compared with the DAC output voltage in comparators U24c, U24b, U24a respectively. The outputs of the comparators are fed to the microprocessor which changes the DAC input data to adjust the DAC voltage until it is approximately equal to the voltage being compared. Thus the processor is able to measure the RF and AF levels and display the result on the front panel meter.

FREQUENCY SYNTHESIZER SECTION

40 The frequency synthesizer section consists of the first LO synthesizer module (A7) and the second LO/BFO synthesizer module (A8). Paragraph 41 describes the first LO synthesizer module, and paragraph 47 describes the second LO synthesizer module.

First LO Synthesizer Module

41 First LO Synthesizer is a VCO single loop synthesizer with an output frequency of 40.605 to 70.455 MHz in 10 Hz increments. The basic synthesizer circuits are shown in simplified block diagram Figure 4-5.

Simplified Block Diagram Description

42 The Voltage Controlled Oscillator generates the basic frequency which is applied to the first mixer module (A2) and to the divide by N circuit. The value of N is determined by the digital control logic, which in turn is controlled by the frequency selection inputs. The output of the divide by N circuit is applied to a phase comparator, which generates an output based on the phase difference between the divide by N signal and the reference signal. The phase comparator output is combined with additional frequency selection information from the digital control logic filtered and applied as a control voltage to the VCO.

43 A change in the value of N will change the value of the output frequency F_o by an amount equal to the reference F_r. For example, if F_r is 100 kHz and N is 10, then the output frequency F_o will be 1 MHz. If N is changed to 11, then, in order to maintain F_d at 100 kHz, the value of the control voltage will have to change in a direction and by an amount such as to adjust the frequency F_o of the VCO to 1.1 MHz.

44 For output frequency changes in less than 100 kHz increments (the value of F_r), the value of N is changed for brief periods of time. In order to more clearly understand the circuit operation, it may be helpful to assume that the control line to the VCO is disconnected, that F_o is 10.1 MHz, and N has a value of 10. Under these conditions, F_d is 101 kHz, and therefore not equal to F_r (which is 100 kHz). Therefore, a phase error will be detected by the phase comparator. For each period of F_r, F_o will produce 10.1 pulses (instead of 10) and will therefore advance in phase by 0.1 of a cycle. Thus, after 10 periods of F_r, F_o will have produced 101 pulses and will have advanced in phase by one complete cycle. Throughout this time, F_d will be advancing on F_r and the control voltage of the phase

comparator will continue to increase. If the control line were reconnected to the control input of the VCO this signal would of course tend to adjust F_o until it was exactly at 10 MHz.

45 The digital control unit is used to operate when F_o has advanced by one complete cycle to remove or absorb one complete cycle of F_o. This simultaneously adjusts the phase of F_d and brings F_d into phase with F_r. The output of the phase detector thus falls to zero.

46 Since frequency F_o is still at 10.1 MHz, the phase error between F_d and F_r will start again to build up and the value of the VCO control signal will increase once more, until, after a further 101 cycles of F_o (ten cycles of F_d), the digital control unit will once again absorb once complete cycle of F_o, eliminating the phase difference, and dropping the VCO control voltage to zero. The net effect of this circuitry is that a sawtooth waveform is produced as the control voltage to the VCO.

Second LO/BFO Synthesizer

47 This board contains the 5 MHz internal reference oscillator, the 40 MHz second LO and the 455 kHz BFO synthesizer circuits, together with the links and switching circuits necessary to enable the operation from, or the provision of, an external reference frequency of 1, 5 or 10 MHz. A 1 MHz reference output is also provided to the first LO synthesizer module A7. The block diagram is shown in Figure 4-6 and the circuit diagram in Figure 8-8.

Reference Oscillator (TCXO Optional)

48 Y1 is a temperature compensated crystal oscillator (TCXO) operating at 5 MHz. The power supply to Y1 is regulated by U1 and can be switched off via transistor Q1, when operation from an external reference signal is required, by ungrounding the /INT input (switch S2 set to EXT position).

49 With Y1 active, the 5 MHz reference signal is applied to the digital phase comparator U3 via the transistor switch Q5 and TTL shaper Q6. At this time, Q4 is made inoperative by the ground on the /INT line, and diode CR2. When operating from an external source Y1 and Q5 are turned off; Q4 is turned on.

40 MHz Crystal Oscillator/Phase Locked Loop

50 U22D operates as a crystal controlled oscillator in conjunction with crystal Y2. The oscillator frequency can be varied over narrow limits by the application of a d.c. control voltage to varactor diode, CR4. The oscillator is phase locked to either a 1 MHz, 5 MHz or 10 MHz reference signal as described in the following two paragraphs.

51 The 20 MHz oscillator output is fed to buffer U22A and isolation amplifier Q10, to divider chain U7, which is capable of dividing by either 20, 4 or 2. The division ratios are selected for the phase comparator reference and external reference output frequencies by using IC switches U4 and U5 and suitably linking LK1 and LK2. (For 1 MHz connect LK1 and LK2, for 5 MHz connect LK2 only, for 10 MHz connect LK1 only).

52 The divided output is applied to the digital phase comparator U3 together with the internal (or external) reference frequency. The phase comparator outputs are fed to a digital to analogue converter circuit Q7, Q8 and Q9 which provides a smooth d.c. control voltage to the oscillator varactor diode CR4 so as to phase lock the 20 MHz oscillator to the reference signal.

53 The 40 MHz output is provided by the frequency doubler stage, consisting of Q11, L9 and L10, through J3 to the second mixer on A3.

Reference Input/Output

54 The reference frequency output is amplified and buffered by Q3, Q2 when the internal reference oscillator is in use. When an external reference is employed the output impedance of this buffer serves to provide a 50 ohm termination for the external source.

Beat Frequency Oscillator

55 The required 455 ±8 kHz BFO frequency is derived from a single PLL synthesizer tunable in 10 Hz increments and locked to the reference frequency.

56 Q18, Q19 and associated components form a voltage controlled oscillator operating at 50 times the required BFO frequency in the range 22.350 MHz to 23.150 MHz.

57 The output of Q19 is buffered by Q20 and fed to an integrated circuit U20, fixed divide by 50, and is also fed to a programmable divider chain U14 to U19.

58 The fixed divider, U20 provides the required output frequency in the range 455 ±8 kHz to A4 while the output from the variable divider serves as one input to the phase comparator U10. The second (reference) input to the phase comparator is derived from the fixed divide by 2000 U8, and U9, operating with a 1 MHz input and an output of 500 Hz.

59 The phase comparison frequency is 500 Hz, thus enabling the VCO to be phase locked in discrete 500 Hz increments over the operating range, depending on the selected division ratio of the variable divider.

60 The particular division ratio required in the range 44,700 to 46,300 Hz is selected by BCD inputs from the control module, A9.

61 The phase comparator outputs are fed to digital to analogue converter circuit Q15, Q16, and Q17, which functions to provide a smooth d.c. control voltage to the oscillator varactor diode CR7 in such a manner as to phase lock the oscillator to the chosen multiple of the reference frequency.

62 The subsequent division by 50 in U20 provides the required BFO output signal, variable in 10 Hz increments over the range 447 - 463 kHz.

CONTROL SECTION

63 The control section comprises the microcomputer module A6A2, the receiver control module A9, and the optional rear panel interface module A6A1. Figure 4-7 is a simplified block diagram of the control section.

64 The overall operation of the RA1792 is controlled by the Central Processing Unit (CPU), an 8-bit integrated circuit computer. The microprocessor operates according to the Control Program, permanently stored in a Read Only Memory (ROM), and uses Random Access Memory (RAM) for temporary data storage (scratch pad). The CPU addresses the memory via the Memory Interface, a special large-scale integrated circuit, in order to fetch instructions and data.

65 Under the direction of the Control Program, the microcomputer controls specific functions within the RA1792, including:

(a) Display of information on the front panel.
(b) All data supplied to the receiver circuits.
(c) Memory retention of the receiver settings during power failure.
(d) Initialization of circuits following application of power.
(e) Interface with remote controller.
(f) Interface with local controls on front panel.
(g) Monitoring and display of receiver status.

66 A continuous sampling/enabling process sequentially presents data inputs and outputs for receiver control. This sampling/enabling process, encompassing control and monitor functions, is accomplished either on demand or at regular intervals as specified by the CPU. When there is a change in some front panel or remote control setting, the CPU detects this change and presents instructional data to the control circuitry of the synthesizer and RF paths, as well as presenting data to change the front panel display settings.

Detailed Circuit Description, Microcomputer, A6A2

67 The Microcomputer Module, A6A2, contains the CPU, the memory, input/output (I/O) expansion circuitry and the power on/power fail master reset system. The 3850 CPU manipulates data, provides both arithmetic and Boolean logic operations, performs data routing and memory address and I/O operations, under real time control. The memories are addressed by the CPU through the 3853 Static Memory Interface (SMI). The ROMC code from the CPU specifies the operation to be performed by the SMI. The Control Program for the CPU is stored in the erasable/programmable read-only memory (EPROM), and a 'scratch pad storage' is provided to the CPU through 256 bytes of random access memory (RAM). The method of communication between the CPU and all other components of the control section is through the bi-directional, 8-bit Processor Bus. The I/O expansion circuitry uses the Processor Bus and the ROMC codes to obtain a Control Bus (IOC) which provides both I/O strobes, the direction data is to go, and which address Processor Bus data is to go to or be obtained from. A Data Bus (IOD) is provided, isolated from the Processor Bus except during I/O operation. The power on/power fail master reset system is used to initialize the microprocessors, and to provide orderly cessation of microprocessor operations in event of Power Failure. Figure 8-6 in the circuit diagram of the Microcomputer Circuit Card Module.

Central Processor Unit, U1

68 Figure 4-8 presents a logical organization diagram of the 3850 CPU, U1. The timing for the entire microcomputer, the 2 MHz Φ output, is generated by Y1, C1 and C2. There are 4 or 6 Φ periods in an instruction cycle; the choice between short or long cycle is made by the CPU and is dependant on the instruction (ROMC) being executed. The instruction cycle control signal, WRITE, defines each machine cycle. The 16 bits of latched I/O data from the CPU, I/O ports 00 to 07 and I/O ports 10 to 17, and the interrupt logic are directly linked to the rear panel interface A6A1 only. The /RESET line is used to disable the CPU to end processing at the completion of a machine cycle. The /RESET is also used to initialize CPU operation. When /RESET is asserted, pulled low, the CPU will execute the program originated at address 0. The data buffers, DB0 to DB7, are the bi-directional Processor Bus. The serial stream of digital operations created by the real time processing of the microcomputer are passed along this 8-bit bus. The five control signals ROMC0 to ROMC5 identify the operations which other components of the microcomputer must perform. The 5-bit ROMC control signals are made available directly to the SMI, rear panel interface, and the I/O expansion circuitry.

System Memory

69 System Memory consists of the 3853 SMI, U2, the EPROMs U5, 6 and 7, the 'scratch pad' RAMs, U8 and 9 and the read/write and memory page control circuitry, U3A, U3B and U13. The SMI generates the 16-bit addresses for the microcomputer in accordance with the ROMC control signal output from the CPU. The top 4 bits of address are ignored. The /MEMW line, when low, specifies that data from the Processor Bus will be read into the RAM at the specified address. The READ line enables decoders U3A and U3B Address bits A11 and A12 specifying the memory device which is to read out to the Processor Bus the contents of a specific address. U13 maintains the correct logic for this address read to Processor Bus operation. Interrupt Request (/INT REQ) are made available to the CPU on the basis of interrupt priority (/PRI IN) at the SMI. This allows for orderly consideration of rear panel interface interrupt requests. Figure 4-10 provides a logic organization diagram of the SMI.

I/O Expansion

70 The I/O data on the Processor Bus is presented in a serial fashion consisting of an I/O address followed on the next execution cycle by the I/O data. The I/O system to the Processor Bus must be capable of holding on to the I/O address so the address and data can be used at the same time. Otherwise the address is a WRITE cycle ahead and gone from the Processor Bus by the time you have the data. The I/O system also instructs in which direction data is to be moved, input to, or output from the Processor Bus. U4, U11A, B, C, U12A, B and D, U13 and U14 provide for simultaneously available address/data and directions. They allow for the rest of the control section to be made up of decoders which address data to a specific Data Bus I/O Port and input or output strobe that I/O Port.

71 On the positive transistion of the clock, CLK (U14-11), the 'Q' outputs of U14 are set to the logic states of the Processor Bus, the I/O port addresses. U11A, U12A, and U11B are used to detect the specific ROMC state for I/O. When an I/O cycle is detected, CLK is then asserted, and the output control (Q5) of U14 and the enable (/G) of U4 are also set high. This isolates the Processor Bus (PB) from the Data Bus (IOD) and prevents U14 from transferring data to the Control Bus (IOC). The next WRITE cycle ROMC code brings low CLK, OC and /G. This causes the inputs of U14 (D0 to D7) to present a high impedance to the Processor Bus and enables U14 to output the address data to the Control Bus. The low on the /G line enables buffer U4 to transfer data bi-directionally between the Data Bus and the Processor Bus. This achieves coincidence of I/O data and address.

72 The direction of data transferred between the Data Bus and the Processor Bus is in accordance with the ROMC code detection. This code is provided by U11B, U11C and U12D. A low on the DIR line of U4 moves the data from the Data Bus to the Processor Bus and asserts the I/O READ strobe. When the ROMC code specifies a Processor Bus to Data Bus transfer, DIR is asserted so that NAND, U11B, /WSTB

strobes serve to enable I/O decoders in unison with the Control Bus addresses. The Control Bus (IOC), /WSTB, and /IO READ are available to both the rear panel interface, A6A1 and the front panel memory board A9A2 modules. The Data Bus (IOD) is available only to the front panel memory board A9A2.

Master Reset System

73 The master reset system is composed of the schmitt trigger, Q1 and Q2, the RAM shutdown timing system, Q4, Q5, R14, C15, Q6, the 2.0 volt RAM power source, BT1, R9, CR3, C16, the battery charging circuit and the switching transistor Q3.

Power Fail/Memory Retention

74 The schmitt trigger, Q1 and Q2, detects voltage variations of the +5 volt unregulated line. The collector of Q2 will go to ground when the power supply +5 volt unregulated line wanders past the trigger thresholds set by CR1 and R5. This asserts the /RESET line of the CPU and instructs the CPU to come to a stop at the end of the next execution cycle, no matter what that cycle is. Because the CPU may still require some memory access from or to the RAMs for that last execution cycle, there is a delay in the switch of the RAMs power source, determined by R14 and C15. When /RESET line is asserted, it proceeds to turn off the drive to Q4 turning off Q5 which lets R15 discharge C15. Once C15 brings the gate of Q6 within 2 volts of ground, the chip enable 2 line (CE_2) is brought low, allowing the V_{DD} to drop to 2 volts. The CE_2 line must be a solid low before the voltage on V_{DD} drops below 4.7 volts. The RAMs receive their 5 volt supply through Q3. When Q3 back biases it leaves an open circuit through C16, causing it to slowly discharge its +5 volts. As C16 discharges CR3 is brought into conduction providing 2.4 volts from BT1 to the RAMs. The battery leakage is greater than the current drawn by the RAMs therefore several months of memory retention is available

Power ON/System Initialization

75 At Power On, the +5 volt unregulated line comes up first which switches Q1 and Q2, bringing the /RESET line high. The CPU now starts the initialization process and executes the instructions located at address zero. /RESET going high turns Q4 and Q5 on. C15 is charged, the gate of Q6 goes negative and CE_2 is asserted, enabling both +5 volt V_{DD} and memory I/O. During the turn on cycle, Q3 will quickly become a saturated transistor and quickly charges C16. R11 protects Q3 from damage during turn on. Once C16 reaches a 4.7 volt charge, CE_2 at the RAMs has gone negative and a +5 volt operation begun. At the same time CR3 is back biased and CR6 and R9 charge the Ni-Cad battery, BT1. If the serial remote control option is installed, the /RESET line is also provided to the UART, A6A1U10, for start-up initialization of the microprocessor.

Front Panel, A9

76 The front panel assembly contains the front panel, the switch and display circuit card assembly A9A1 and memory board A9A2.

Switch and Display Circuit Card Assembly, A9A1

77 The Switch and Display Circuit Card assembly contains the liquid crystal displays (LCD's), their drivers and the switch matrix. Figure 8-9 is the circuit diagram of this assembly. This assembly connects to the memory board through connector W1P1.

78 U1 and U2 are liquid crystal displays. Access to the data bus, DB0 to DB7 (from the memory card), is provided to the LCD meter and mode display by the BCD to 4- or 7-segment decoder/driver circuits U3-U26 and U28. Strobing from the data bus into the latches of the decoder/drivers is provided by U27 (4 bit latch /4- to 16-bit decoder) driven by inputs N0, N1, N2 and N3 and the number display strobe, and display strobes OP32-OP37 (from the memory board). The display oscillator U29 supplies the required difference frequency signal to all decoder/drivers.

79 The switch matrix SA0-SC7 and SD0 (columns A, B, C and D and rows 0-7) connects directly to the memory board through connector W1P1. The function of each switch is shown in the switch function table. The L/S Phone assembly, Volume Control, IF Gain control and Meter switch are mounted on the front panel and connect to the switch and display circuit card assembly through terminals E1-E10 and then on to the memory board through connector W1P1.

Memory Board, A9A2

80 The memory board interfaces microprocessor A6 to the front panel switch and display circuit card and to circuit cards A1-A4, A7, A8 and A10. It serves to connect the circuitry in these cards to the microprocessor data bus and control lines, under control of the microprocessor. In this manner, functions requested by the front panel controls or the remote controller can be performed by the microprocessor programs. Figure 8-11 is the circuit diagram of the memory board. The microprocessor connects to the memory board through connector W1P1 while the switch and display circuit card connects through connector J2.

Switch Matrix

81 The status of the switch matrix is continually read by the microprocessor, Columns A, B, C and D of the switch matrix are activated, in turn, by microprocessor signals IOC0-IOC2, IOC5 and $\overline{\text{IO READ}}$, through multiplexer U10. The 7 rows of the switch matrix are strobed onto the microprocessor bus (IOD0-IOD7) through buffers U16b and U17a, to be read by the microprocessor.

Display Data and Strobes

82 The display data is transferred from the microprocessor bus to the receiver data bus (DB0-DB7) through latches U19 and U20 by microprocessor signals IOC5 and $\overline{\text{WSTB}}$. The strobes for the transfer of data from the receiver data bus to the appropriate display latches are generated by the 4 to 16 line decoder U8, driven by IOC0-IOC5, $\overline{\text{WSTB}}$ and timing stages U9a and U9b, and counter U12.

1st LO Synthesizer

83 Connections to the 1st LO synthesizer are provided through connector W5P1*. The serial strobe, serial clock and serial data signals out are generated by flip-flop U4 and gates U5C and U3C. They are then entered on the data bus and strobed by OP31 and OP39, via multiplexer U8.

2nd LO Synthesizer

84 Connections to the 2nd LO synthesizer are provided through connector W2P1. The BFO enable and frequency setting are output through flip-flops U24-U27, entered on the data bus and strobed by OP38, via multiplexer U8.

Main IF/AF

85 Connection to the main IF/AF card are provided through connector W6P1. The data bus and strobe signals OP3A-OP3F from multiplexer U8 are sent to the main IF/AF control circuitry. The IF gain, volume and L/S connections from the front panel are also fed to the main IF/AF through this connector. The scan inhibit, AF comparator, main RF comparator, and ISB RF comparator, from the main IF/AF board together with the meter switch input (from the switch and display circuit card) are strobed to the microprocessor bus for readout, through buffer U15 via output 5 from multiplexer U10. This same strobe, through U17b, strobes the tuning encoder outputs onto the microprocessor bus for readout.

Tuning Encoder Circuitry

86 The tuning knob is coupled to an optical encoder. An enscribed coding disc is attached to the encoder spindle, and rotates over two sets of LED/photo-transistor detectors U29 and U30. As the disc rotates, the detectors generate pulse waveforms that are input for pins 12 and 14 of buffer U17b. Access to the data bus is as described in paragraph 85. Detectors U29 and U30 are physically displaced so that the two outputs are 90° out of phase. Clockwise rotation of the tuning shaft (from the front) causes the output of U28 pin 14 to lead as shown in Fig. 4-11. Counterclockwise rotation causes the output of U28 pin 1 to lead. Resistors R12 and R13 and capacitors C14 and C15 provide a small amount of a.c. and d.c. hysteresis.

* W4P1 on early versions of receiver.

Memory

87 U13 and U14 are two 1024 x 4 bit EAROMs. These provide the channel memory. Data terminals D0-D7 connect to the microprocessor data bus while the address terminals A0-A9 connect to the receiver data bus and the outputs of Counter U12. Reading and writing into and from the EAROM is controlled by microprocessor signals IOC0, IOC1 and $\overline{\text{WSTB}}$, and output 1 of multiplexer U10.

POWER SUPPLY, A10

88 The power supply module includes a power line filter assembly, a power transformer, three rectifiers, and four integrated circuit regulators with associated smoothing and decoupling capacitors. The module can be set to operate with line input voltage of 100, 120, 220, or 240 Volts + 10% - 15% and line frequencies from 45 to 65 Hz. Power is controlled by an ON/OFF switch mounted on the receiver front panel. Figure 8-12 is the circuit diagram.

Power Input Circuit

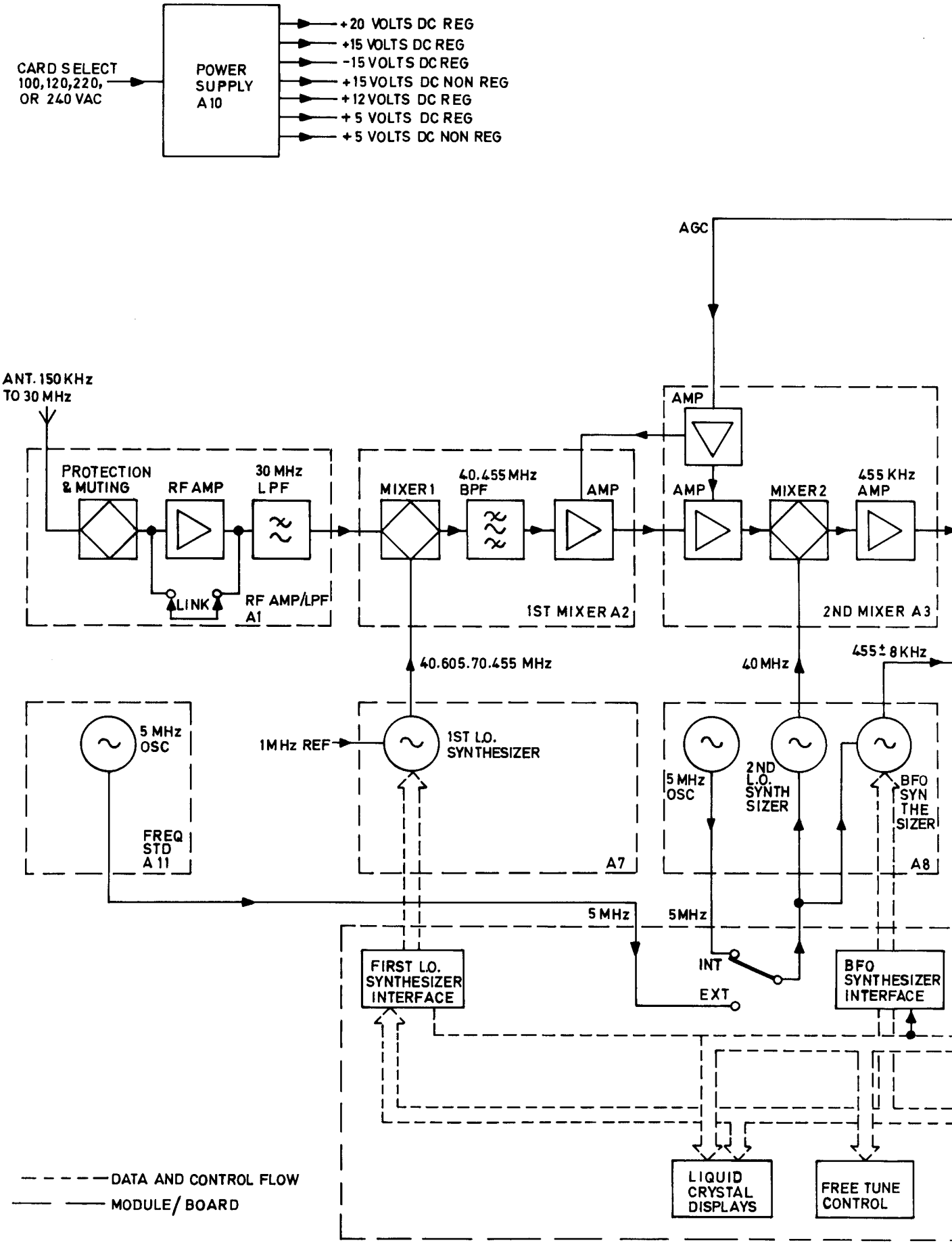
89 Power is applied to the power line filter assembly which includes the connector A10J1, the fuse F1, a line filter and a printed circuit card switch for transformer primary tap selection. The tap selection allows operation from nominal 100, 120, 220 or 240 volt power sources.

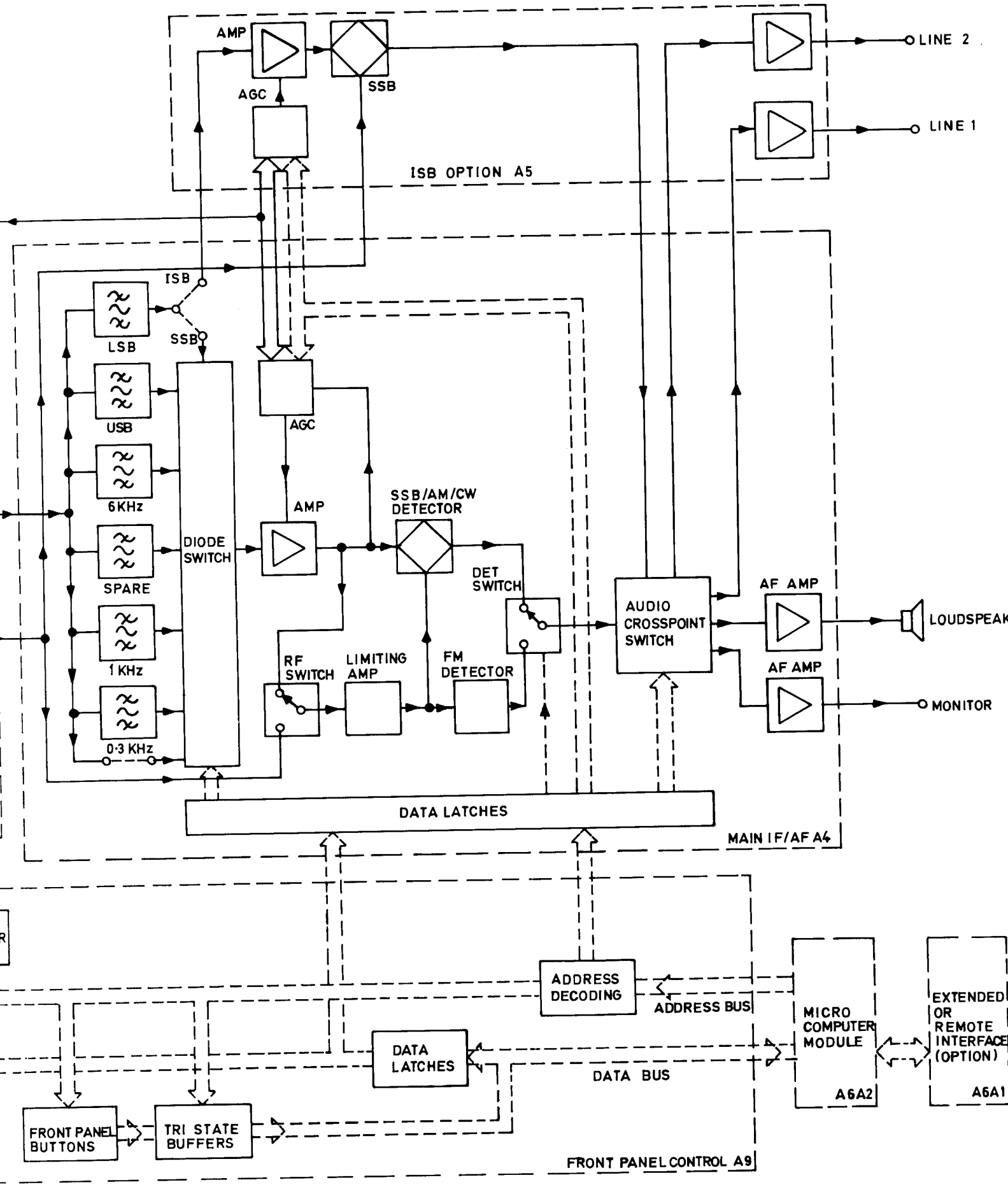
90 Power is provided via A10J2 pins 3, 4, to the front panel double pole ON/OFF switch and returns via A10J2 pins 8-9 to the selected taps on the power transformer A10T1.

DC Outputs

91 Full-wave rectifiers, smoothing capacitors and integrated circuit voltage regulators are employed to provide the required d.c. output voltages of +20, +15, +12, +5 and -15 regulated, and +15 and +5 unregulated for the various receiver modules. The d.c. voltages are supplied through connector A10A1J1.

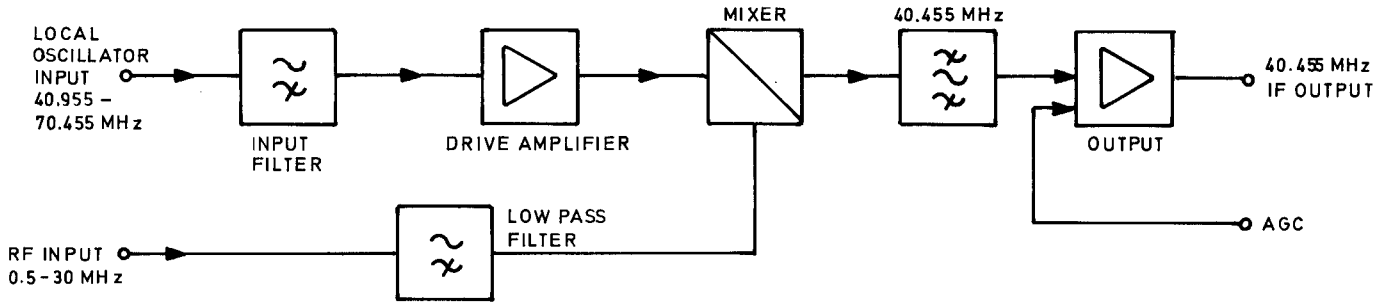
92 Zener diode VR1 provides over-voltage protection for the +5V bus. Capacitors C2, C3, C5, C6, C8, C9, C11, C12, C13 and C14 are fitted adjacent to the repective regulators to suppress possible oscillation. Bridge rectifiers CR1, CR2 and CR3 rectify the a.c. voltage from the secondary taps of T1 while capacitors C1, C4 C7 and C10 provide filtering for the a.c. ripple voltage.


CARD SELECT
100,120,220,
OR 240 VAC
POWER
SUPPLY
A10
+20 VOLTS DC REG
+15 VOLTS DC REG
-15 VOLTS DC REG
+15 VOLTS DC NON REG
+12 VOLTS DC REG
+5 VOLTS DC REG
+5 VOLTS DC NON REG
AGC
ANT. 150 KHz
TO 30 MHz
PROTECTION
& MUTING
RF AMP
30 MHz
LPF
LINK
RF AMP/LPF
A1
MIXER 1
40.455 MHz
BPF
AMP
1ST MIXER A2
AMP
AMP
MIXER 2
455 KHz
AMP
2ND MIXER A3
40.605.70.455 MHz
40 MHz
455 ± 8 KHz
5 MHz
OSC
FREQ
STD
A11
1MHz REF
1ST L.O.
SYNTHESIZER
A7
5 MHz
OSC
2ND
L.O.
SYNTH
SIZER
BFO
SYN
THE
SIZER
A8
5 MHz
5MHz
FIRST L.O.
SYNTHESIZER
INTERFACE
INT
EXT
BFO
SYNTHESIZER
INTERFACE
LIQUID
CRYSTAL
DISPLAYS
FREE TUNE
CONTROL
DATA AND CONTROL FLOW
MODULE/BOARD

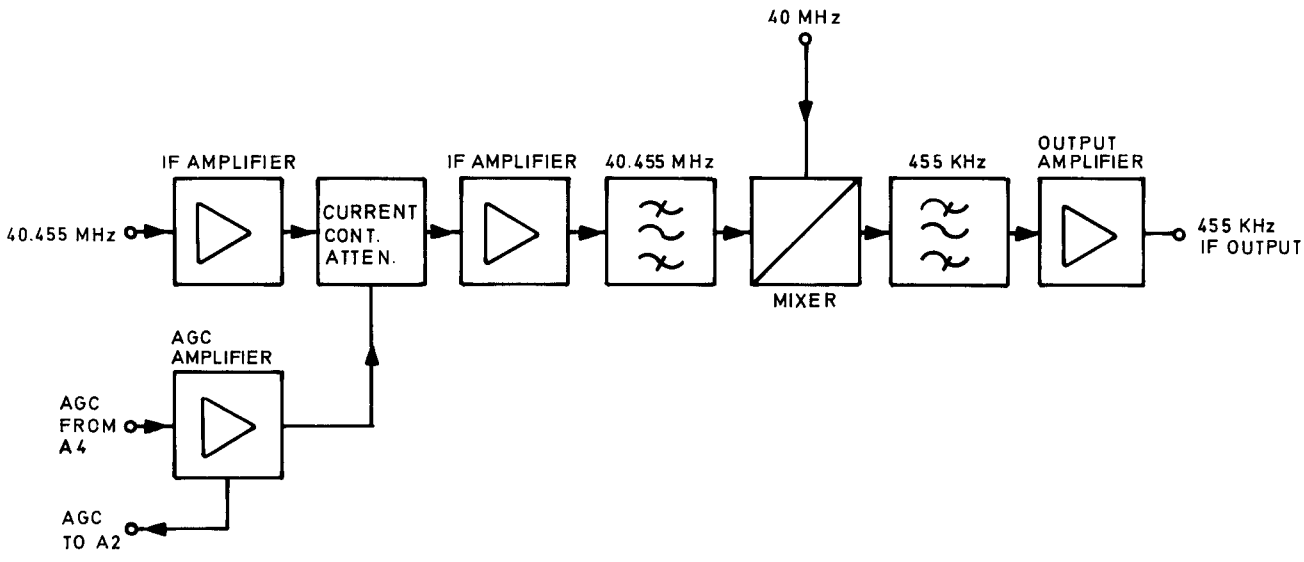


Overall Functional Diagram: RA 1792

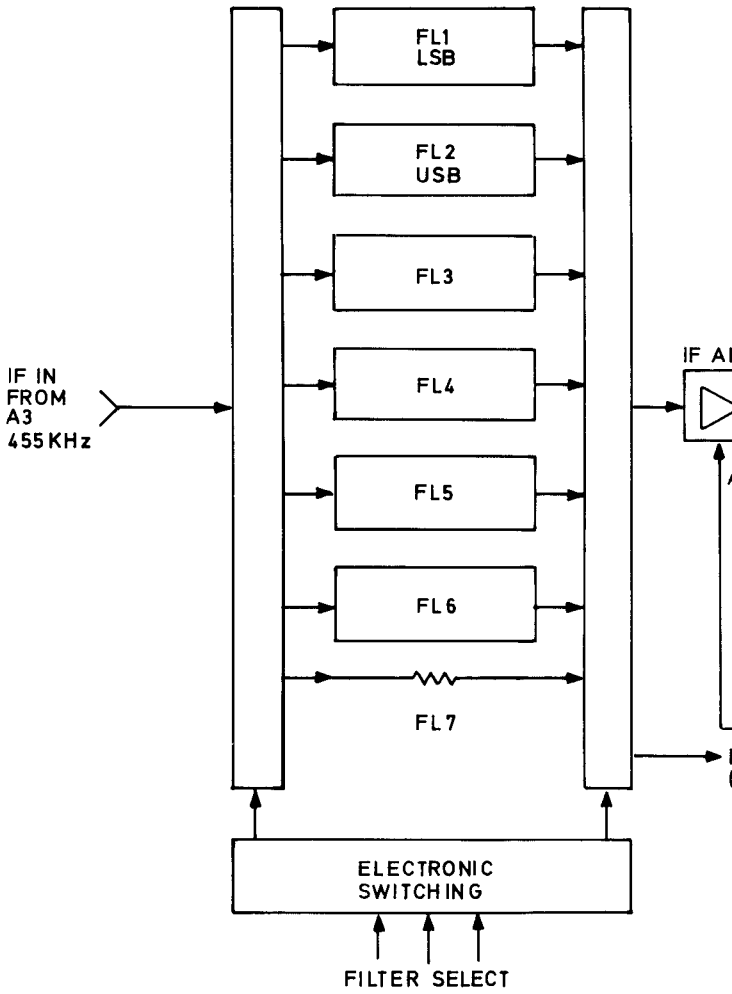
Fig. 4.1

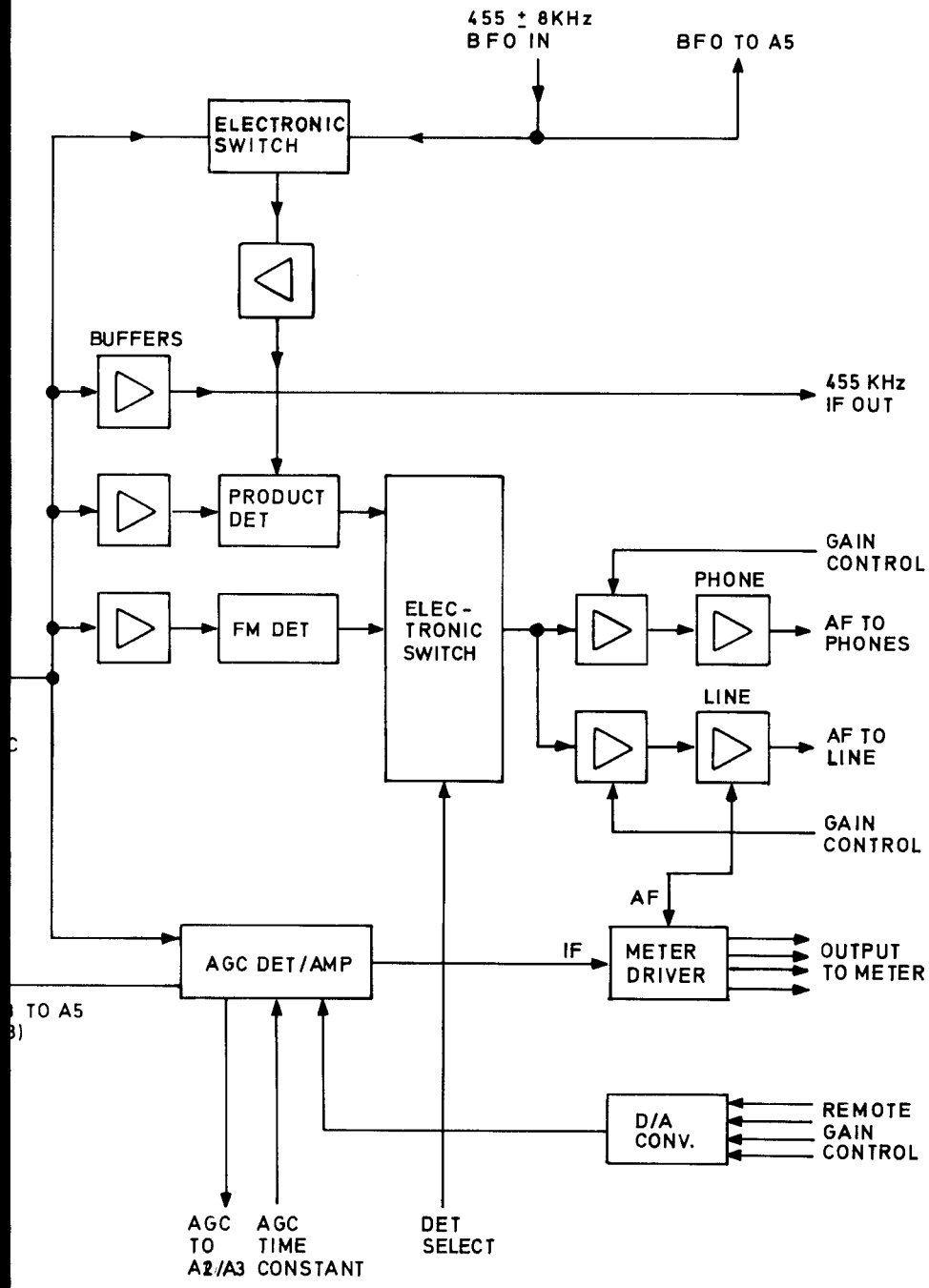


Simplified Block Diagram, First Mixer, A2 Fig.4-2



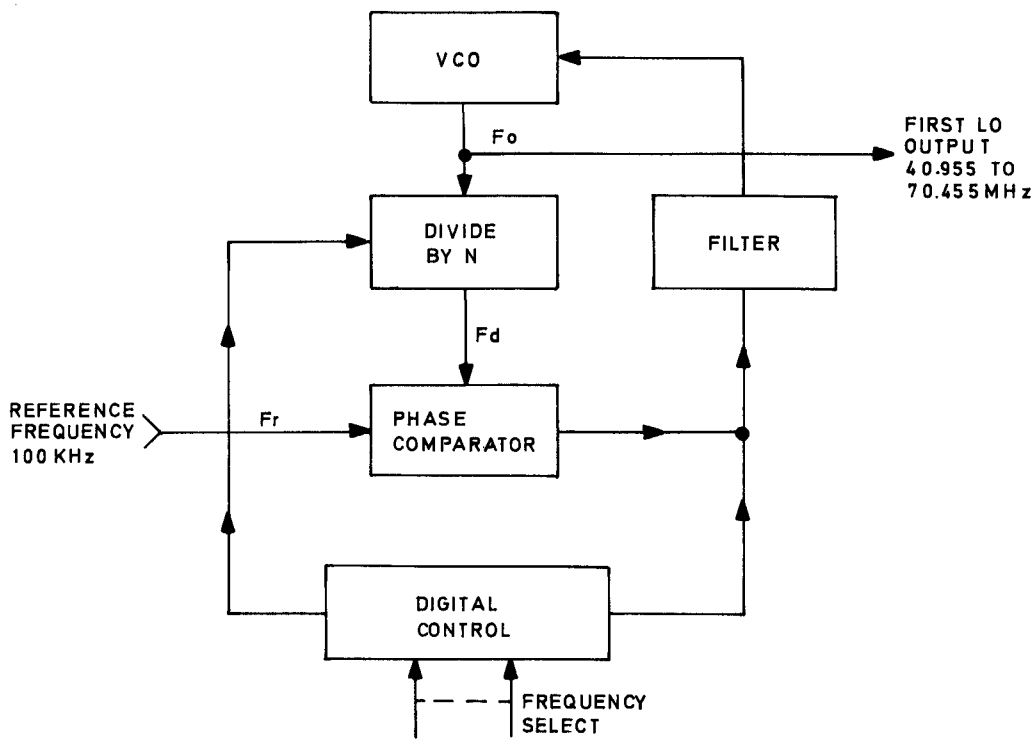
Simplified Block Diagram, Second Mixer, A3 Fig.4-3


FL1
LSB
FL2
USB
FL3
FL4
FL5
FL6
FL7
IF IN
FROM
A3
455KHz
ELECTRONIC
SWITCHING
FILTER SELECT



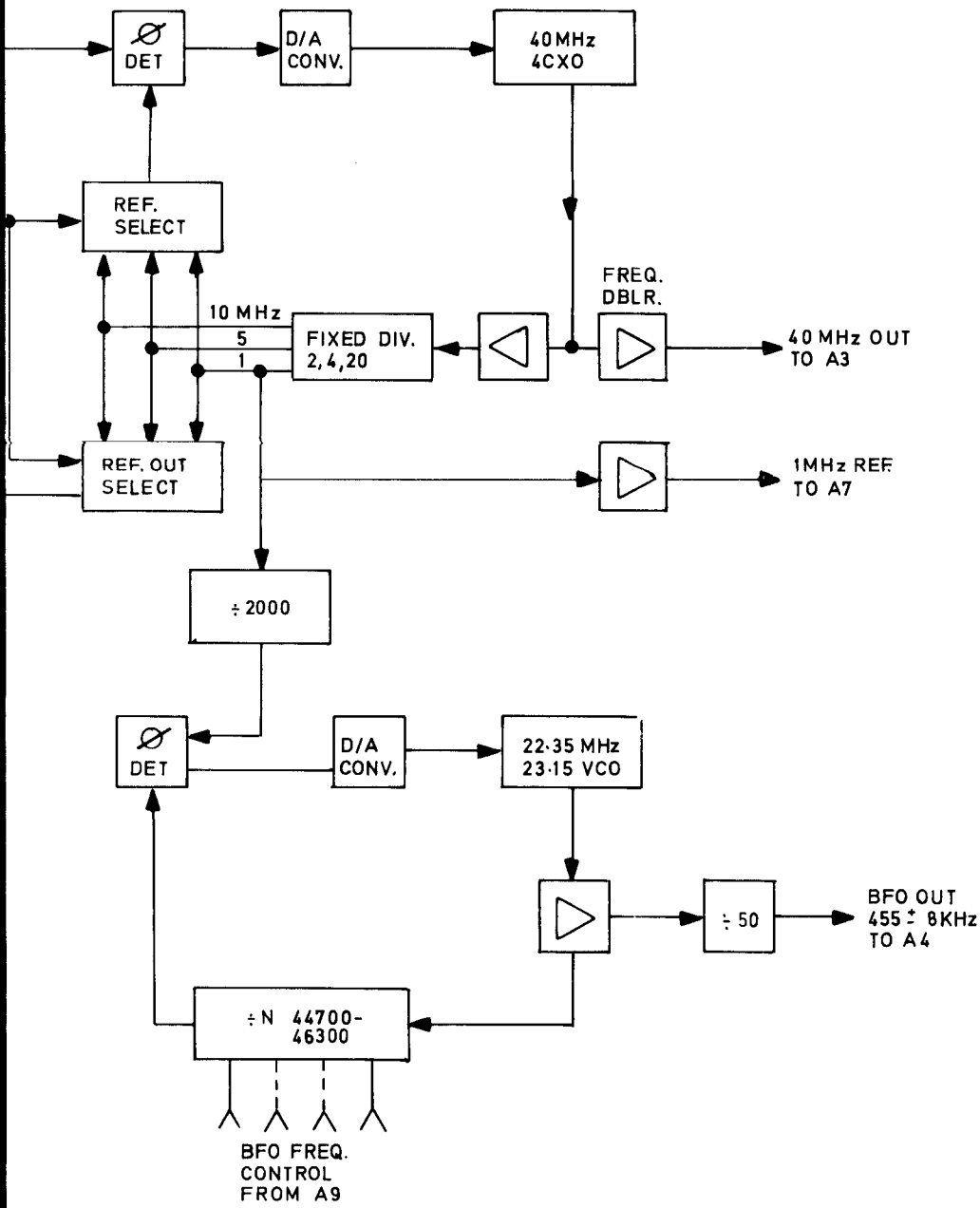
Simplified Block Diagram
Main IF/AF A4

Fig. 4.4

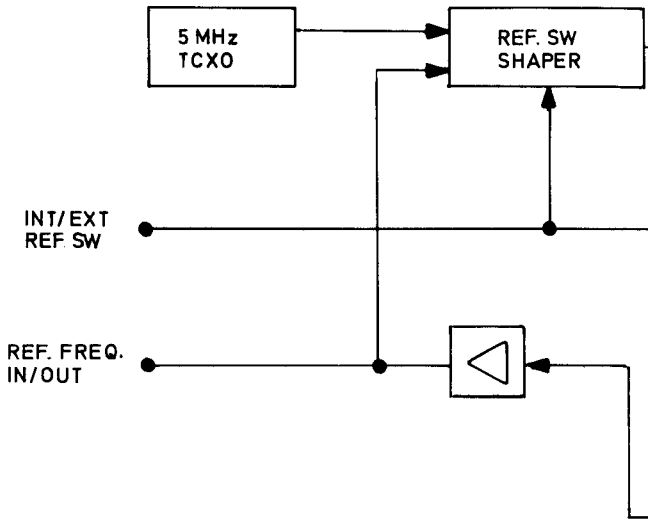


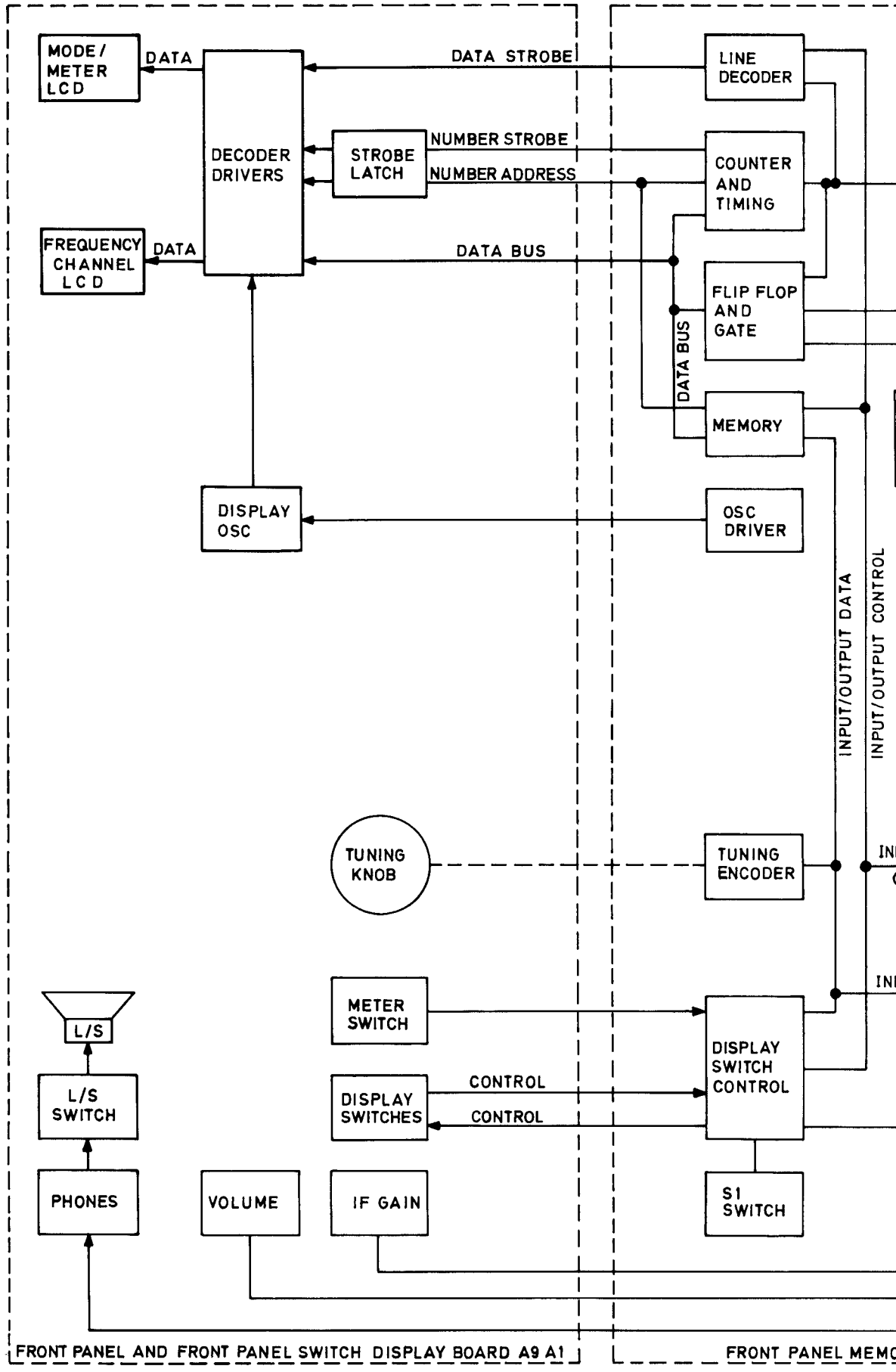
RACAL
TH1496

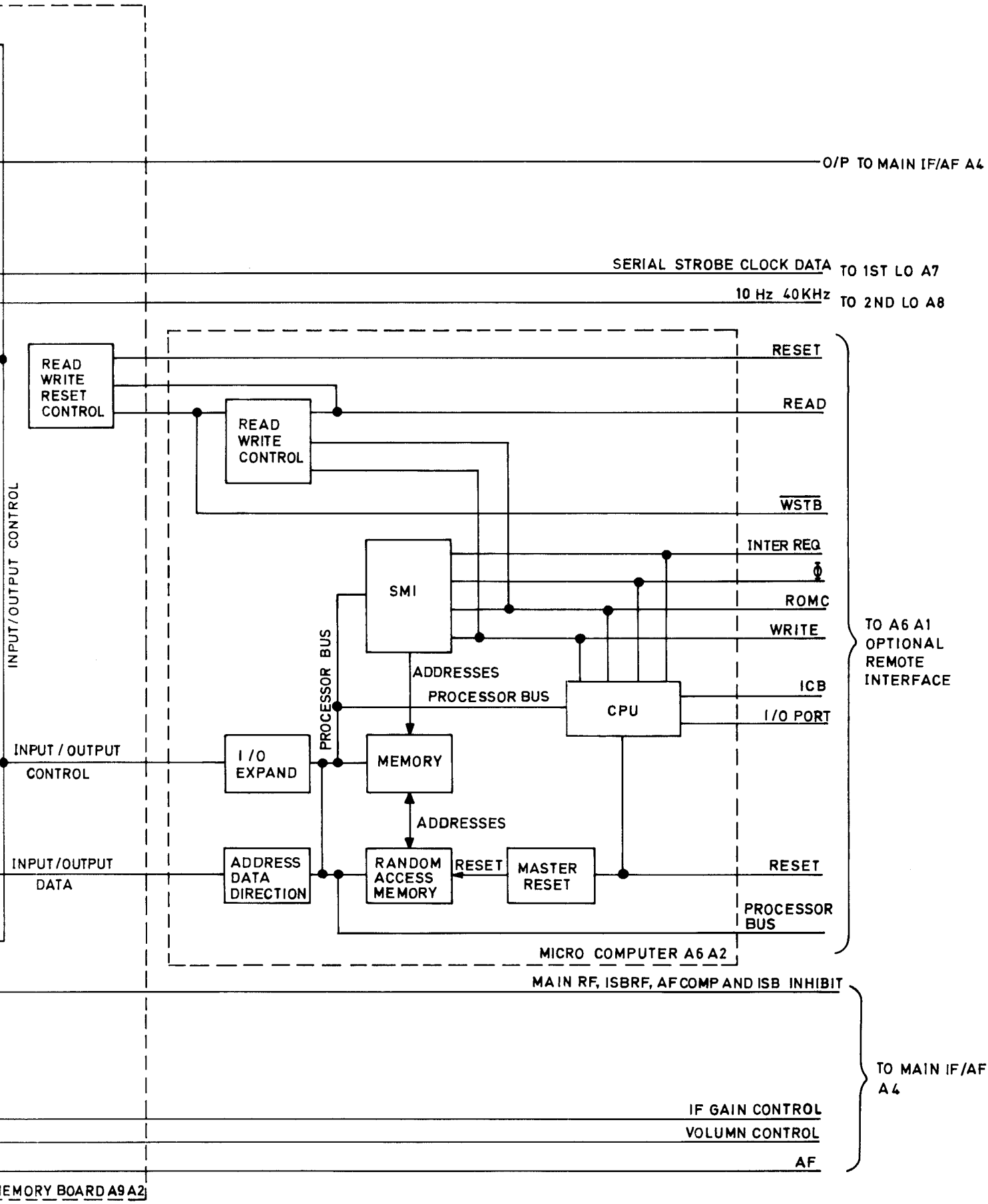
Simplified Block Diagram, First LO Synthesizer Fig.4-5



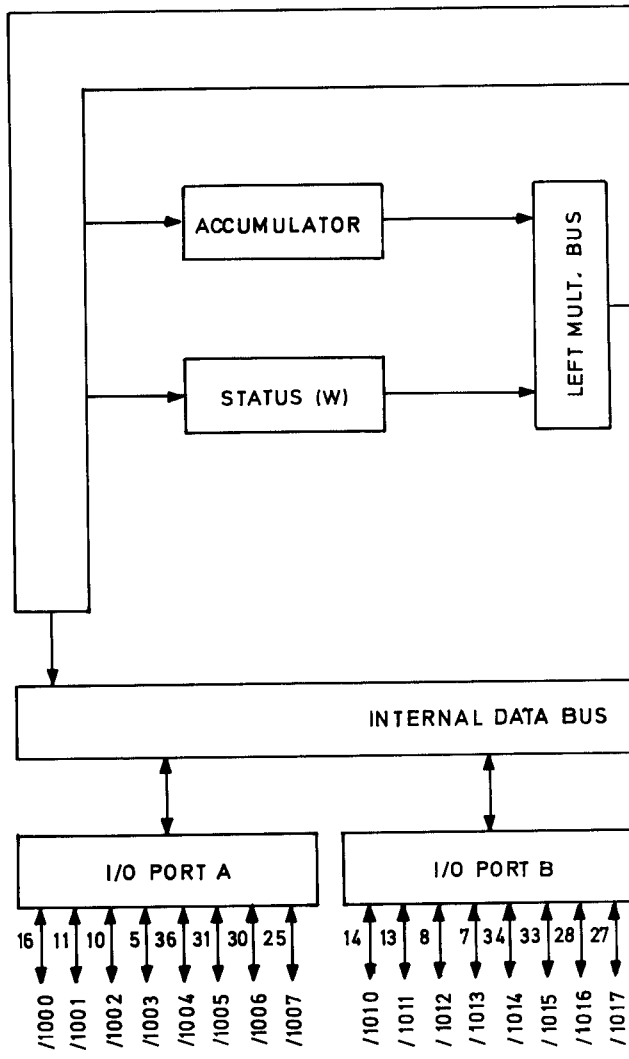
Simplified Block Diagram, Second LO/BFO Synthesizer, A8 Fig 4-6

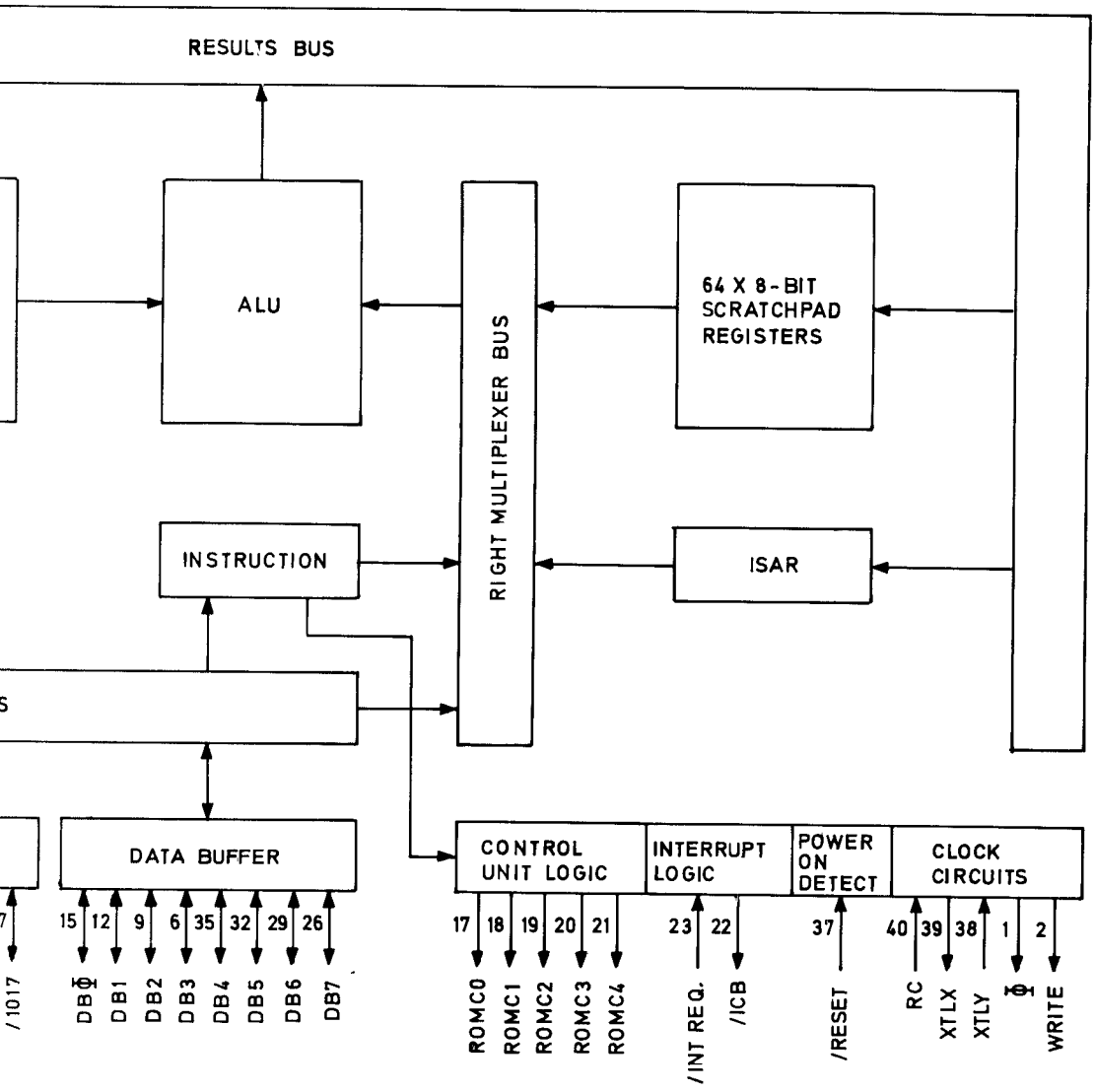

5 MHz
TCXO
REF. SW
SHAPER
INT/EXT
REF SW
REF. FREQ.
IN/OUT


MODE / METER LCD
DATA
DECODER DRIVERS
DATA STROBE
LINE DECODER
STROBE LATCH
NUMBER STROBE
NUMBER ADDRESS
COUNTER AND TIMING
FREQUENCY CHANNEL LCD
DATA
DATA BUS
FLIP FLOP AND GATE
DATA BUS
MEMORY
DISPLAY OSC
OSC DRIVER
INPUT/OUTPUT DATA
INPUT/OUTPUT CONTROL
TUNING KNOB
TUNING ENCODER
METER SWITCH
L/S
L/S SWITCH
DISPLAY SWITCHES
CONTROL
CONTROL
DISPLAY SWITCH CONTROL
PHONES
VOLUME
IF GAIN
S1 SWITCH
FRONT PANEL AND FRONT PANEL SWITCH DISPLAY BOARD A9 A1
FRONT PANEL MEMO



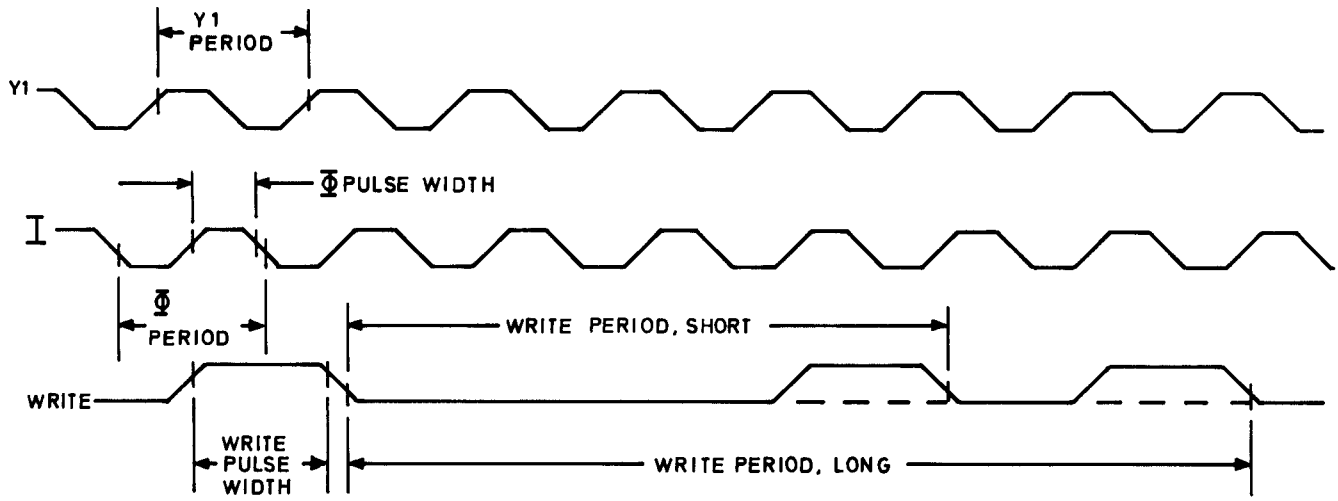
Functional Diagram : Control Section Fig. 4.7


ACCUMULATOR
STATUS (W)
LEFT MULT. BUS
INTERNAL DATA BUS
I/O PORT A
I/O PORT B
16 11 10 5 36 31 30 25
/1000 /1001 /1002 /1003 /1004 /1005 /1006 /1007
14 13 8 7 34 33 28 27
/1010 /1011 /1012 /1013 /1014 /1015 /1016 /1017



Logic Organisation and Pins for the 3850CPU

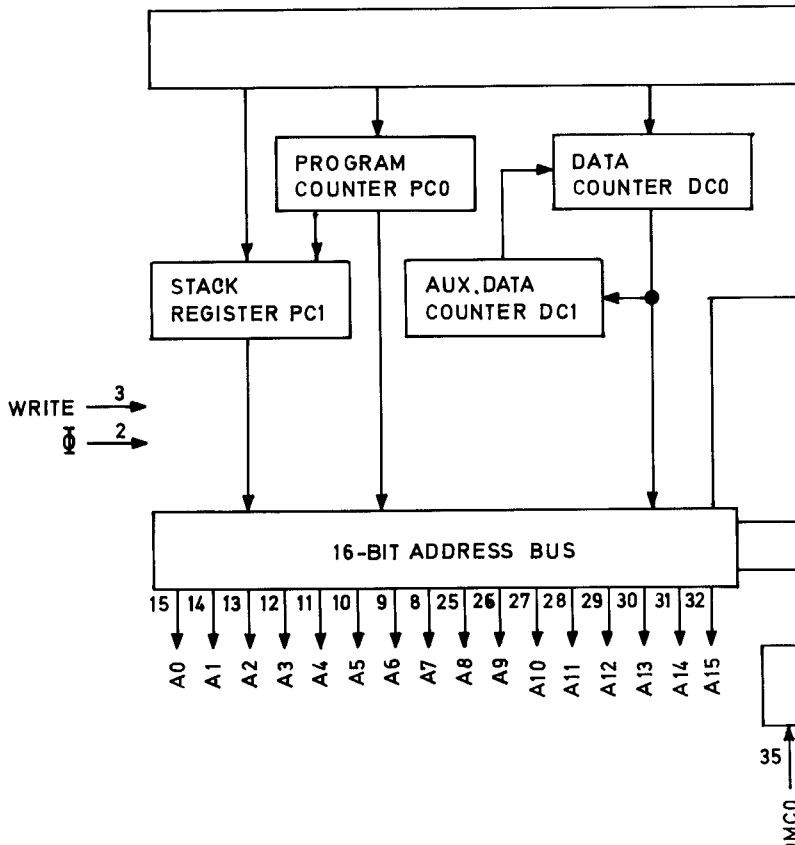
Fig. 4-8

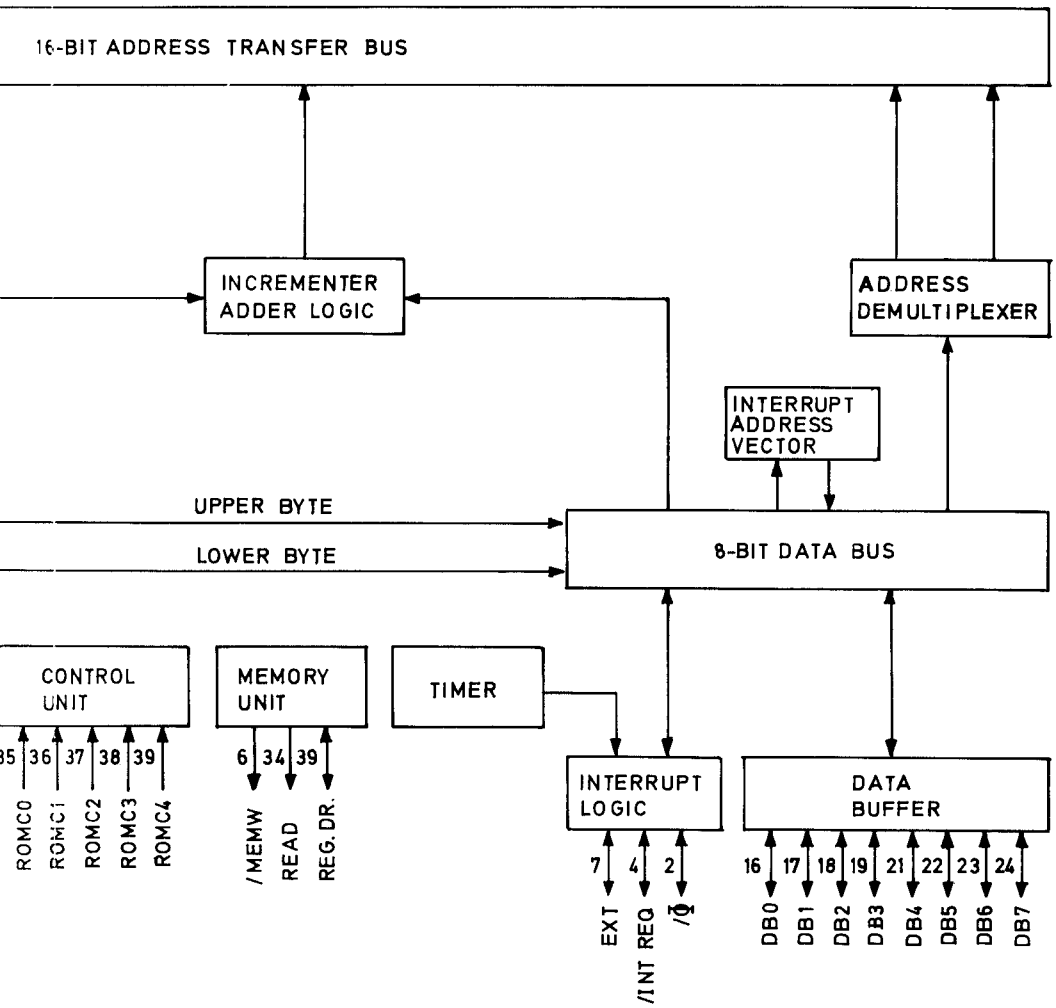


RACAL TH1496

Timing Signal Specifications

Fig.4-9

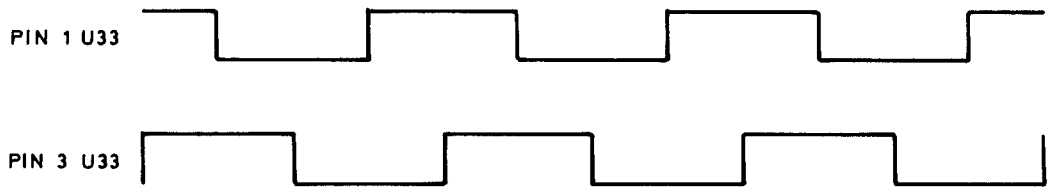

PROGRAM COUNTER PC0
DATA COUNTER DC0
STACK REGISTER PC1
AUX. DATA COUNTER DC1
WRITE
3
2
16-BIT ADDRESS BUS
15 14 13 12 11 10 9 8 25 26 27 28 29 30 31 32
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
35



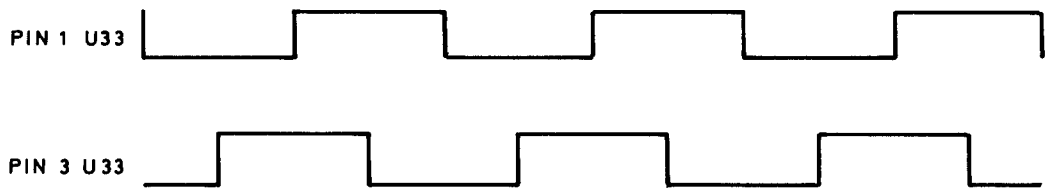
Logic Organisation and Pins for the 3853SMI

Fig. 4.10

CLOCKWISE:



COUNTER-CLOCKWISE:



Encoder Outputs

Fig. 4·11

CHAPTER 5

FAULT FINDING PROCEDURES

INTRODUCTION

1 This chapter contains a set of fault finding procedures for the RA1792 HF Communications Receiver. Tests have been provided for the major receiver unit and for module/board replacement. All procedures should be performed by a qualified technician with adequate training in electronic theory and practise includina digital and RF circuitry. The technician should also be thoroughly familiar with and skilful in the use of handtools and electronic test equipment.

2 Figure 5-1 is a signal flow diagram for the receiver; Figure 5-2 is a fault finding chart to aid in module troubleshooting; and Figure 5-3 is an RF level diagram for RF checks.

3 Paragraphs 8 - 9 describes the turn-on procedures and operator checks. Paragraphs 10 - 18 describes test procedures to isolate faults to a replaceable module, and to perform any correction maintenance required.

4 If specified performance cannot be obtained, then a fault must be suspected. Refer to Chapter 8 for the electrical circuit diagram of the particular module under test. When a module has been determined to be defective or suspected, it may be removed and replaced with one known to be of good operating condition. In any cases where alignment procedures are required, refer to Chapter 6, Alignment.

For operating instructions, refer to Chapter 3 of this manual.

SAFETY PRECAUTIONS

5 Observe all safety regulations. Do not replace modules or make adjustments (except when aligning trimmers or other adjustable components) with the a.c. line cord plugged in or external power supplies turned on.

WARNING

The power line voltages used in this equipment may be dangerous to personnel. Use caution when servicing the power supplies or their load components.

EQUIPMENT REQUIRED

List of Test Equipment

6 Table 5-1 is a list of test equipment recommended for conducting fault finding and maintenance procedures. Although not all of these instruments are specifically mentioned in the procedures of this chapter, they are nevertheless recommended in order to properly probe the RA1792 for faulty conditions.

TABLE 5-1. LIST OF TEST EQUIPMENT

Item	Description	Recommended Instrument or Equal
1	1 ea. HF Signal Generator	Racal 9084
2	1 ea. Frequency Counter	Racal 9911
3	1 ea. Oscilloscope	Tektronics 465
4	1 ea. RF Voltmeter	Racal 9301A
5	1 ea. Digital Multimeter	Racal 9077A
6	1 ea. AF Power Meter	Marconi TF893A

Special Tools

7 No special tools other than normal hand tools are required for the replacement of any module in the RA1792 receiver.

TURN-ON PROCEDURE AND OPERATOR CHECKS

8 The following procedure should be followed by an operator to turn on the RA1792 Receiver while observing certain indications. The procedure is useful as a first step to fault finding by identifying possible faulty operation of the receiver.

Procedure

9 (1) Inspect the equipment for signs of physical damage.

(2) Check all controls for correct mechanical action, i.e., freedom from binding, scraping of general interference of parts. Leave REF INT/EXT switch (S2) to INT.

(3) Connect the power cord from A10J1 to a suitable AC power source.

(4) Connect a set of headphones to the front panel PHONES jack.

(5) Turn the receiver SUPPLY switch to on.

(6) Select each control function in turn by pressing the appropriate key switches. Observe that the LCD displays indicate that the proper function has been selected and that the tuned and BFO frequencies are properly displayed.

(7) While listening to the noise output from the receiver, select 16 kHz bandwidth, AM detector, Man gain (IF GAIN control set to max) Tuned Frequency, and above 500 kHz.

(8) Observe that the noise level varies in accordance with the setting of the IF GAIN and VOLUME controls.

(9) With the IF GAIN and VOLUME controls set for maximum, select each bandwidth in turn and observe that the receiver noise level falls as the bandwidth is reduced. Select the 16 kHz bandwidth.

(10) Select FM then CW and observe that the character of the noise output changes for each demodulator.

(11) Select AGC MED, set the tuned frequency to all zero's, select BFO/Variable and tune the BFO from zero through the range $\pm$ 8 kHz. Observe that a beat note corresponding to the BFO offset is audible.

(12) Tune the BFO to indicate + 1.00 kHz, observe that the RF and AF levels are indicated as appropriate on the LCD meter scales.

(13) Select the AF meter scale and observe that the AF level indication varies in accordance with the setting of the VOLUME control. Leave this control set to indicate 0 dB output level on the AF meter scale.

(14) Connect an antenna to A1J1 and tune the receiver to a known transmission, observe that all controls function normally.

(15) Turn the SUPPLY switch off. Disconnect all equipment.

Corrective Maintenance

10 If all normal indications as described above were not obtained, faulty conditions can be suspected. A list of possible symptons has been provided on the fault finding chart, Figure 5-2, to aid in isolating a faulty module/board assembly.

RECEIVER DISASSEMBLY AND REASSEMBLY

11 Refer to Chapter 6, Alignment, paragraph 6 - 14 for receiver disassembly and reassembly.

FAULT FINDING PROCEDURES

12 The following procedure is to be followed to isolate a fault to a module within the receiver. Before proceeding with fault finding, check the fault finding chart, Figure 5-2, to determine the approximate location of the fault.

13 ## POWER SUPPLIES

Preliminary

(1) Plug in power cord A10J1 and connect to main power source.

(2) Connect a headset to the PHONES jack.

(3) Turn SUPPLY switch to ON, and observe that the front panel displays are active. If not, check power fuse on A10 assembly. Replace as required.

Tests

14 Check for the following voltages with respect to ground at power supply module A10, using the digital multimeter, item 5 of Table 5-1. A10 is located inside the chassis near the rear panel.

A10A1J1 Pin No.	Voltage
1, 14	+20V ± 1 volt
10, 11, 24	+15V ± 0.75 volt
3, 16	20V nominal unregulated
22, 23	-15V ± 0.75 volt
7, 8	+12V ± 0.5 volt
4, 17	+5V, +0.5 to -0.2 volt
5, 18	10V nominal unregulated
13, 19, 20	Ground, 0 volts

NOTE: Ripple on all regulated supplies should be less than 5 mV P-P.

Corrective Action

15 If any of the above voltages are not present or are outside the permitted tolerance check for short circuit conditions on the appropriate power bus. If no receiver fault condition is apparent replace the A10 module.

RF Section

16 Refer to the signal level diagram, Figure 5-3, for the following tests.

Preliminary

17 (1) Remove receiver from rack and disassemble as described in the alignment procedures of Section 6.2.

(2) Connect the RF voltmeter, Item 4 of Table 5-1 to the IF OUT connector on the receiver rear panel using the 50 ohm termination.

(3) Using the HF Signal Generator, Item 1 of Table 5-1, inject the test signal levels shown in Figure 5-3 as appropriate tc verify the performance of the individual signal path modules and/or the entire signal path as necessary.

(4) Verify the LO and BFO frequencies and levels as required, using the frequency counter, Item 2 and RF Voltmeter, Item 4 of Table 5-1.

(a) 1st LO frequency equals indicated tuned frequency plus 40.455 MHz (A2J1).

(b) 2nd LO frequency equals 40 MHz (A3J2).

(c) BFO frequency equals 455 ± 8 kHz (A4J5).

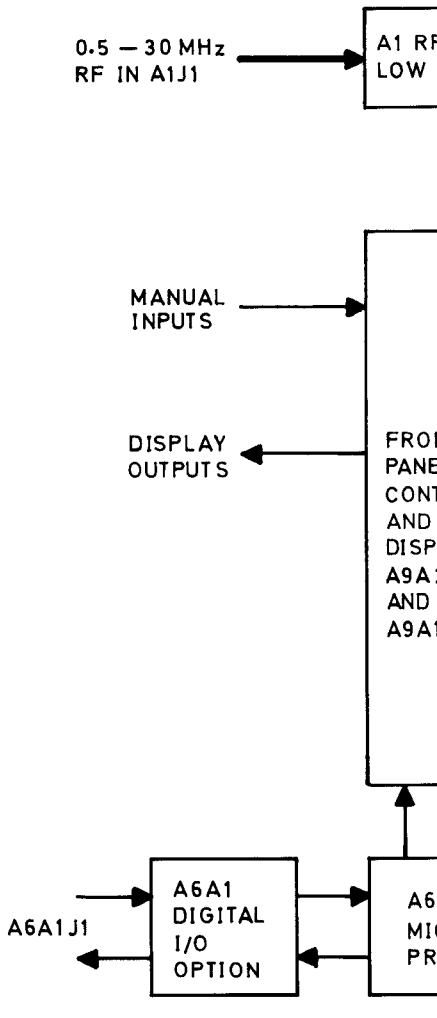
NOTE: It should be determined if the optional Internal Frequency Standard is installed. An external reference standard should be used where necessary for the above checks.

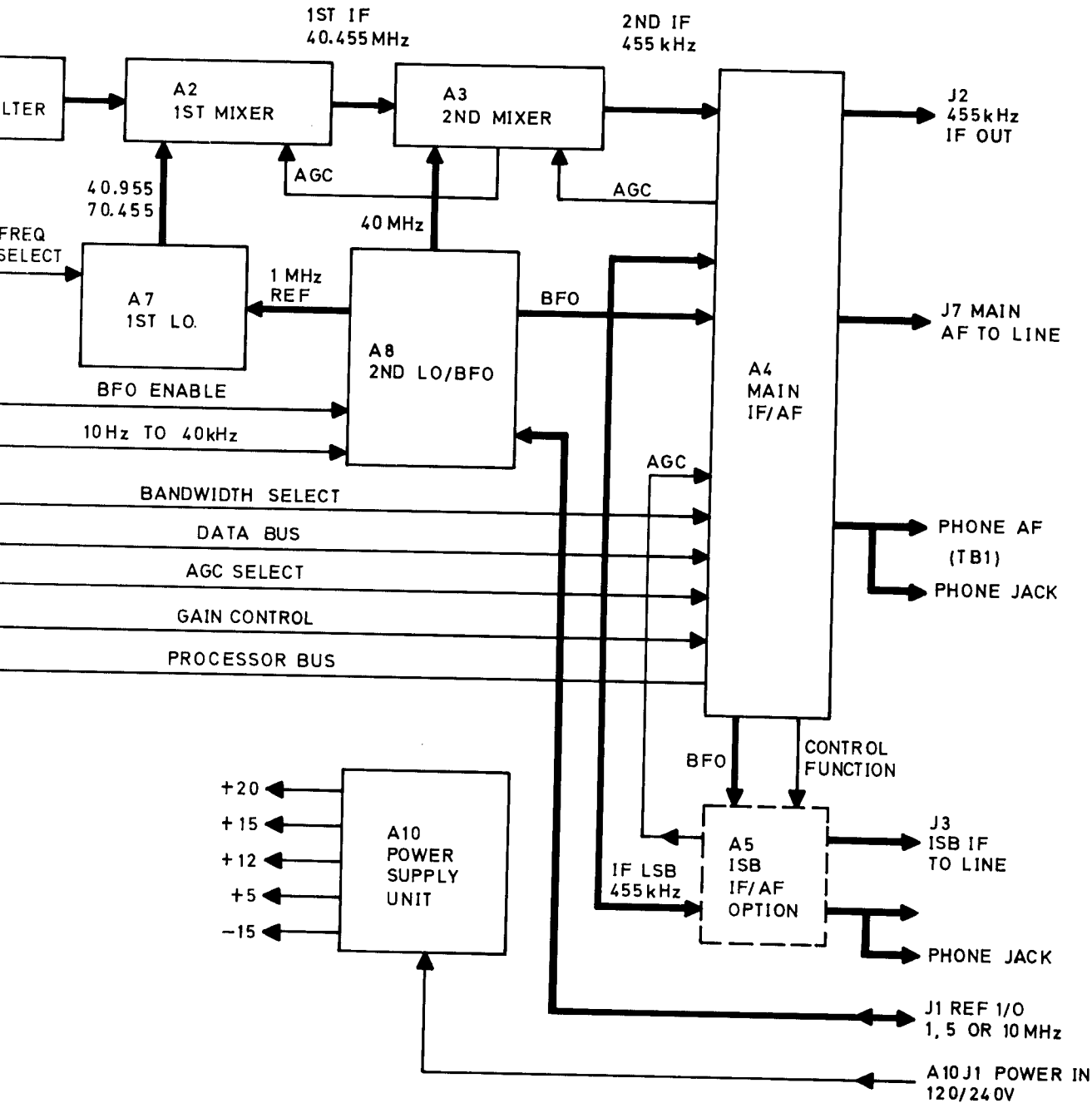
Control Malfunction

18 (1) Local control of RA1792 is affected via the A6 microcomputer and A9 Receiver Control modules with the associated keyswitch and tuning encoder controls. Before replacing these modules ensure that all ribbon cable connectors and the EPROM's A6U5, U6 and U7 are properly seated in their respective sockets.

(2) Remote control malfunctions are likely to be confined to fault conditions existing in the optional A6A1 Digital Interface module or the associated control connections.

NOTE: Since the above modules are interactive it may be necessary to substitute known working modules in turn to effect a repair. Start by disconnecting A6A1, then replace A6A2, then A9A2, then A9A1 as needed.


0·5 — 30 MHz
RF IN A1J1
A1 RF
LOW
MANUAL
INPUTS
DISPLAY
OUTPUTS
FRO
PANE
CONT
AND
DISP
A9A
AND
A9A
A6A1J1
A6A1
DIGITAL
I/O
OPTION
A6
MI
PR

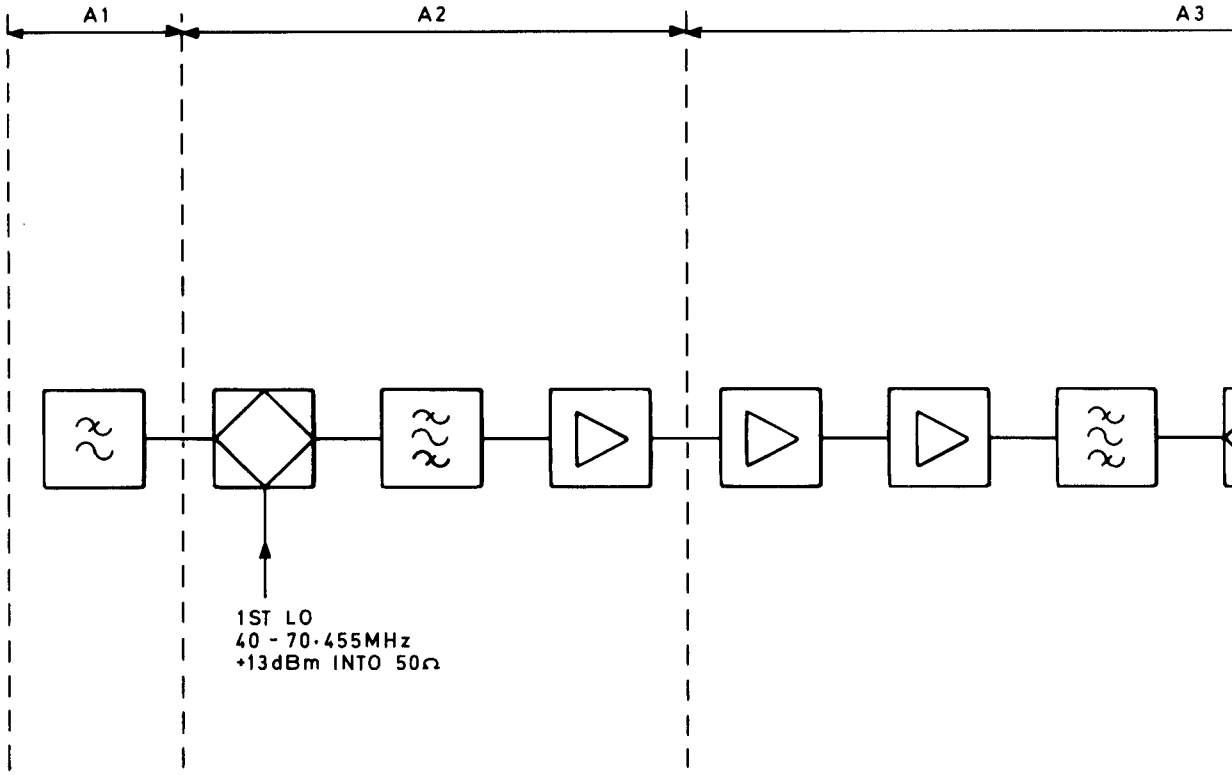


Signal Flow Diagram
RA.1792

Fig. 5·1

FAULT SYMPTONS	BOARD/MODULE PROBABLE FAULT											COMMENTS & NOTES
	A1	A2	A3	A4	A5	A6A2	A6A1	A7	A8	A9	A10	
	Check Module Board According To Number Order											
All voltages low											1	Check A10T1 primary tap selection
One or more d.c. bus voltages low											1	Check for short circuit conditions at A10A1J1
Sensitivity low	4	3	2	1				6	5			Ref. Figure 5-3
BFO wrong frequency						2			1	3		Check A8J (Control)
2nd LO wrong frequency									1			Check setting of S2
1st LO wrong frequency						3		2	1	4		Check Ref. 1 MHz at A7J2. Check TP11 (Control)
Poor bandpass response		3	2	1								
Low AF output				1					2			Check VOLUME control R2
Low IF output				1								Check cable to J2
Poor AGC range		3	2	1								Check AGC cabling
ISB Fault				2	1							
Control malfunction						1				2		Check all control cabling
Low Remote Control							1					Check cable to A6A1J1
No/Wrong REF FREQ Output									1			Check A8 links LK1 and LK2
Meter malfunction				1		3				2		

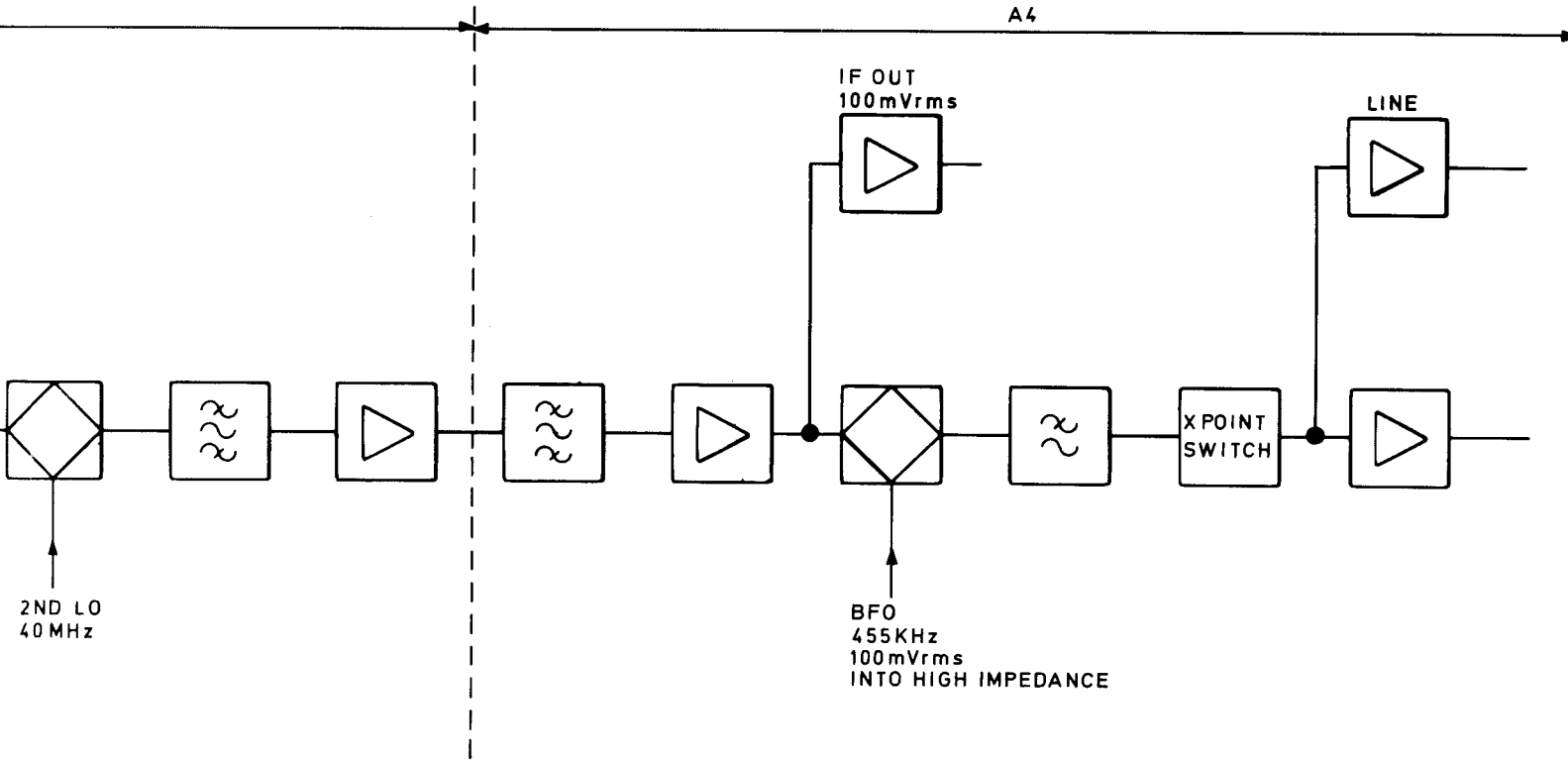
Figure 5-2. Fault Finding Chart



TEST POINT	— A1J1	J5	E9	A3E1	TP1	TP2
RELATIVE SIGNAL LEVEL	— 0dB	-1dB	-10dB	+4dB	+18dB	+24dB
SIGNAL LEVEL (rms)	— 0·5μV	0·46μV	0·16μV	0·8μV	4·0μV	7·9μV

FREQUENCY ← 40·455MHz →

ALL SIGNAL LEVELS ARE RELATIVE TO ANTENNA INPUT AND ARE MEASURED USING AN RF OR AF VOLTMETER WITH HIGH IMPEDANCE PROBE. MEASUREMENTS MADE WITH AGC OFF AND IF GAIN SET TO MAXIMUM.



	TP3	U4 PIN 14	A3E3	TP1	TP7	U28 PIN 7
	+37dB	+34dB	+55dB	+42dB	+116dB	
	35µV	25µV	280µV	63µV	300mV	350mV

455KHz — AUDIO

Signal Level Diagram Fig 5.3

CHAPTER 6

ALIGNMENT PROCEDURES

CONTENTS

TABLES

ILLUSTRATIONS

CHAPTER 6

ALIGNMENT PROCEDURES

INTRODUCTION

1 This chapter contains alignment procedures for the RA1792 Receiver as a complete assembly. Under normal operating conditions the receiver will maintain the factory alignment over a long period of time. Realignment should, therefore, only be carried out following the replacement of components which affect the alignment, or where a known misalignment exists. Refer to Chapter 3, Operation, for operating instructions.

2 Should it be necessary to realign the complete receiver, the following procedures must be followed in the order given. Before attempting to realign an individual sub-assembly it must be ascertained, where applicable, that the preceding assemblies are functioning correctly.

3 If the specified performance cannot be attained by alignment, then a fault must be suspected and reference should be made to Chapter 5, Fault Finding.

4 A certain amount of dismantling it necessary to gain access to certain areas of the receiver. Details for dismantling and reassembly are contained in paragraph 6. After alignment, ensure that all dismantled assemblies are correctly reassembled and that all shielding covers are replaced using all screws provided or their exact equivalents.

5 Table 6-1 lists the test equipment required. Those listed in the example column are recommendations only. Any instruments with equal or better characteristics may be substituted.

RECEIVER DISASSEMBLY AND REASSEMBLY

6 Figures 6.1 and 6.2 show the location of the printed circuit boards, and Figures 6.3 to 6.12 show the location of components on the printed circuit cards.

To disassemble the receiver proceed as follows:

(1) Remove the receiver from rack or cabinet. It is held by 4 screws on the front panel.

(2) Remove top and bottom cover plates by loosening six quarter-turn fasteners.

TABLE 6-1

TEST EQUIPMENT

Item	Instrument	Specification	Recommended Instrument
1	Digital Multimeter	Range: 0 to 150V a.c. and d.c. 0 to 1A a.c. and d.c. Display: $3\frac{1}{2}$ digits Accuracy: $\pm$ 3%	Racal 4002
2	Oscilloscope, Dual Trace	Sensitivity: 5 mV/div. Frequency: d.c. to 2 MHz	Tektronix 465
3	RF Voltmeter	Range: 300 mV to 3V r.m.s. Frequency: 100 kHz to 70 MHz Input Impedance: > 1 M ohm with 50 ohm adaptor Accuracy: $\pm$ 1% of full scale	Racal 9301A
4	Audio output power meter	1 mW - 1W 15Ω and 600Ω	Marconi TF893B
5	Digital Frequency Meter	Frequency Range: 0 to 50 MHz Sensitivity: 10 mV r.m.s. Impedance: 1 M ohm Accuracy: 1 part in 10^6 $\pm$ 1 count	Racal 9904
6	Signal Generator	Frequency Range: 450 kHz to 50 MHz Accuracy and Stability: Output frequency is locked to the frequency standard in use. Output Level Range: -130 dBm to +13 dBm into 50Ω Modulation: AM 800 mV into 600Ω gives 80% mod. depth. FM 1V into 600Ω gives peak selected deviation. Peak deviation is between 10 kHz and 300 kHz depending on selected range. Output Impedance: 50Ω	Racal 9084
7	Terminating Coupler	50-ohm BNC-SMB	

(3) The A1, A6A1 and A6A2 modules may now be removed from the chassis by unplugging all electrical connections, removing the screws securing each module, then lifting the module away from the chassis.

(4) The Power Supply module (A10) may be removed by disconnecting electrical connections, loosening the 4 captive screws, holding the module to the chassis, and 5 screws securing the module to the rear panel.

(5) To remove A4 and/or A5 (optional) modules, unplug all electrical connections, remove screws securing the module to the chassis and lift the module out.

(6) To remove either A9A1 or A9A2 modules, remove the five electrical connections from A9A2 that come from modules A6A2, A4, A7, A8 and A10, then remove four screws securing the front panel and front chassis and lower the whole assembly away from the main chassis. Remove the tuning disk from the tuning shaft, located behind module A9A2. Module A9A2 may now be removed by removing the screws securing it to module A9A1.

(7) To remove module A9A1 first perform step 6 above, then remove the IF GAIN and VOLUME control knobs and remove the front panel. The A9A1 module may now be removed from the front chassis plate by removing the screws securing it to that plate.

(8) Figure 6-2 shows a bottom view of the chassis which provides access to modules A2, A3, A7 and A8. To remove either of these four modules, remove the shielding cover from the respective module compartment, remove its electrical connections and then remove the module by removing the screws securing it to the chassis.

CHECKING PROCEDURE, POWER SUPPLY A10

7 Test Equipment Required: Digital Multimeter, item 1 of Table 6-1; and Oscilloscope, item 2.

Procedure

8 (1) Disconnect the cable from A10J3 located on the base of the power supply.

(2) Connect the digital voltmeter, item 1, between chassis (0V) and each of the following pins of the power supply, A10, in turn. Use the oscilloscope, item 2, to measure the a.c. ripple.

A10A1J1 Pin No's	Voltage	AC Ripple (p-p)
1, 14	+20V, ± 1V	5 mV
10, 11, 24	+15, ±0.75V	5 mV
3, 16	+20V nominal unregulated	
22, 23	-15V, ±0.75V	5 mV
7, 8	+12V, ± 0.5V	5 mV
4, 17	+5V, +0.5, - 0.2V	5 mV
5, 18	+10V nominal unregulated	5 mV
13, 19, 20	Ground, 0 Volts	

(3) Disconnect all test equipment and reconnect the cable to the power supply.

ALIGNMENT PROCEDURE - 2nd LO/BFO SYNTHESIZER A8

9 Test Equipment Required: Digital Multimeter, item 1 of Table 6-1, RF Voltmeter, item 3, Digital Frequency Meter, item 5, and Oscilloscope, item 2.

Procedure

10 (1) Check on the A8 board to ensure that the links LK1 and LK2 are made in accordance with Table 6-2 for the required REF Frequency IN/OUT mode of operation.

TABLE 6-2

Operating I/O	LK1	LK2
1 MHz	Link	Link
5 MHz	Open	Link
10 MHz	Link	Open

(2) Check that S2 REF INT/EXT switch on the rear panel is set to INT.

(3) Connect the digital frequency meter to J3 and the digital multimeter, set to the 10 Volt range, between TP5 and ground. Connect the frequency counter 1 MHz input to the receiver REF IN/OUT socket J1.

(4) Check Voltmeter for a reading between 6 to 11 Volts. Check frequency counter for a reading of 40.000000 MHz $\pm$ 1 Hz.

(5) Disconnect the frequency meter and measure the 40 MHz output level at J3 into 50 ohms, using the RF Voltmeter. This level should be not less than -5 dBm.

(6) Set the receiver controls for CW operation, BFO centre, and BFO indication to 0.00 kHz.

(7) Connect the digital frequency meter to J4 on the digital multimeter, set to the 10 Volt range, between TP8 and ground.

(8) Observe that the BFO output is 455,000 ± 1 Hz then adjust the tuning slug of L4 as necessary for a multimeter indication of 8 ± 0.5 volts.

(9) Select BFO variable and tune the BFO using the front panel control. Observe that the frequency meter agrees with the front panel indications.

(10) Typical frequencies, signal levels and voltages as they should be at various test points are shown below. When measuring at TP2 and J1, set INT/EXT switch to INT and links LK1 and LK2 are connected for 1 MHz I/O at J1.

Test Point	Frequency	Volts	Remarks
TP2	5 MHz	TTL	Use oscilloscope
TP5	DC	5.5 + 2.5V	Use multimeter
TP8	DC	8 + 2V	Use multimeter
TP9	22.75 MHz	200 mV min p-p	Use oscilloscope (BFO set to 0.00 kHz)
TP10	5 MHz	1V min p-p	Use oscilloscope
J1	1 MHz	222 mV min	Use RF voltmeter
J2	1 MHz	TTL	Use oscilloscope
J4	455 kHz	0.7V p-p	Use oscilloscope

ALIGNMENT PROCEDURE - 1st LO SYNTHESIZER A7

11 Test equipment required: Digital Multimeter, item 1 of Table 6-1, Oscilloscope with X1 probe: item 2, Digital Frequency Meter, item 5.

Procedure

12 (1) Connect the digital multimeter between TP5 and ground.

(2) Set R17 for a multimeter indication of 5.2 ± 0.01 Volts.

(3) Connect the multimeter between TP11 and ground.

(4) Tune the receiver to 29.99999 MHz, and adjust L5 for a multimeter indication of 14 Volts.

(5) Tune the receiver to 00.00000 MHz and ensure that the multimeter indication is not less than 2.5V.

(6) Set the receiver tune frequency to 1046 kHz. Set the oscilloscope to display 0.2 ms/div., external trigger. Trigger the scope from the signal on TP4 and connect the X1 oscilloscope probe to TP11. Set the vertical sensitivity to 5 mV/div.

(7) Adjust R4 to null out the signal on the oscilloscope.

(8) Connect the digital frequency meter to 1st LO output at A7 J3.

(9) Observe that the indicated frequency is equal to the receiver tuned frequency plus 40.455 MHz (± instrument error) over the full receiver tuning range.

(10) Disconnect all test equipment and re-connect all module interconnections.

ALIGNMENT PROCEDURE - MICROCOMPUTER A6A2

13 No adjustments are provided on the A6A2 module and alignment is not required. A6A2 clock frequency is 2 MHz nominal.

ALIGNMENT PROCEDURE - IF/AF BOARD A4

14 Test equipment required: Digital Multimeter, item 1 of Table 6-1, RF Voltmeter item 3, Audio Power Meter, item 4, Digital Frequency Meter, item 5, Signal Generator, item 6 and 50 ohm terminating coupler, item 7.

Procedure

15 (1) Connect the Digital Multimeter between TP9 and ground and select AGC SHORT on the front panel of the receiver. With no signal at antenna input adjust R119 for a multimeter reading of 10 ± 0.05 Volts.

(2) Set the AGC to MAN. and turn the IF GAIN control fully clockwise. Select CW BW5 (16 kHz).

(3) Connect the signal generator output to A4J1. Set the signal generator to 455.00 kHz and the output level to 250 µV pd.

(4) Connect the RF voltmeter with 50 ohm termination to the IF OUT socket, J2 on the rear panel.

(5) Adjust L1 and L2 for maximum indication on the RF voltmeter.

(6) Connect the RF Voltmeter, using the high impedance probe, to A4TP7.

(7) With IF GAIN at maximum, bandwidth to 3 kHz, adjust R39 on the A4 board for an indicated 300mV rms ± 1 dB on the RF Voltmeter.

(8) Set the AGC to SHORT. Increase the signal generator level by 35 dB and adjust R47 for 8.5V ± 0.05V on TP9 measured with the digital multimeter.

(9) Connect the RF Voltmeter to the rear panel IF OUT socket, J2. Select AGC MAN, 6 kHz BW. Adjust the IF GAIN control for 100 mV on the RF voltmeter.

(10) Select each bandpass filter in turn and verify that the required 6 dB bandwidths are obtained by tuning the signal generator through the receiver pass-band.

TABLE 6-3

	6 dB BW (min)	
BW1	0.3 kHz	
BW2	1.0 kHz	
BW3	3.2 kHz	
BW4	6.0 kHz	
	USB/LSB	-6 dB max, 250 Hz to 3.2 kHz in wanted sideband.
BW5	16 kHz	

NOTE: 1. LSB should be measured at A5J3 if ISB of A5 is fitted.

2. The 6 dB bandwidths may differ from those listed above if optional filters are fitted.

(11) Connect the audio power meter, set to 600 ohms, to the MONITOR LINE OUT, pins 4 and 17 of J3 on the rear panel.

(12) Set the receiver AGC to SHORT, MODE to CW, BFO 1 kHz offset.

(13) Connect the signal generator to the A4 IF input using the BNC adaptor.

(14) Set the signal generator to 455 kHz CW output at a level of 10 mV pd.

(15) Adjust AF LINE LEVEL preset control R129 on A4 for 1 mW output. (.775V in 600 ohms).

(16) Select AM mode and 6 kHz bandwidth.

(17) Connect the audio voltmeter to LINE OUT pins 1 and 14 on J3 on the rear panel. Modulate the signal generator to 30% at 1 kHz and check for audio output indication on the Audio Voltmeter.

(18) Select FM mode and 16 kHz bandwidth.

(19) Modulate the signal generator frequency at a 1 kHz rate with a peak deviation of 5.6 kHz.

(20) Peak L3 for maximum AF output.

(21) Connect the output power meter set to 15Ω to the output terminals of J3.

(22) Set the VOLUME control on the front panel to maximum. Ensure that the indicated AF output level is at least 200 mW into 15 ohms.

(23) Disconnect all test equipment, reconnect all removed module interconnections.

ALIGNMENT PROCEDURE ISB IF/AF A5

16 The circuits employed in A5 are identical to the relevant circuits of A4. Refer to the alignment procedures of A4 for realignment of this module.

ALIGNMENT PROCEDURE 2nd MIXER A3

17 Test equipment required: Digital multimeter, item 1 of Table 6-1, Signal Generator, item 6, RF voltmeter, item 3.

Procedure

18 (1) Set the receiver controls for AM reception, 16 kHz bandwidth, AGC manual, and IF GAIN maximum.

(2) Connect the RF voltmeter to the IF OUT connector J2 on the receiver rear panel.

(3) Disconnect P1 from A2J3. Set R24 on the A3 board fully clockwise.

(4) Using the Signal Generator inject a 40.455 MHz signal to P1 and adjust the level to produce an IF output indication of 100 mV rms.

(5) Adjust the following trimmers in the order shown for peak output indication on the RF voltmeter, reducing the signal generator level as required to maintain the 100 mV output reference. Adjust L7, L6, L5, L4, and T1 tor peak.

(6) With the signal generator input level of 1 μV emf at the A3 input, the signal plus noise to noise ratio at the audio output in a 3 kHz bandwidth should be at least 18 dB.

(7) Remove all test equipment and re-instate all module connections.

ALIGNMENT PROCEDURE - 1st MIXER MODULE A2

19 Test equipment required: RF Voltmeter, item 3 of Table 6-1 and Signal Generator, item 6.

Procedure

20 (1) Remove the local oscillator input to J1 of A2.

(2) Connect the signal generator to the LO input A2J1. Set the output to about 0 dBm.

(3) Connect the RF voltmeter using the high impedance probe to TP2 of A2.

(4) Set the receiver front panel controls to AM mode, AGC MAN, 16 kHz BW and IF GAIN to maximum.

(5) Turn SUPPLY switch to ON.

(6) Tune the signal generator to 17.6 MHz. Adjust coil L3 of A2 to provide a notch (minimum amplitude) at 17.6 MHz while observing the RF voltmeter indication.

(7) Tune the signal generator to 26.045 MHz. Adjust coil L4 in the same manner except to provide a notch at 26.045 MHz.

(8) Disconnect the signal generator from J1 and connect it to P1 (RF INPUT).

(9) Connect the RF voltmeter with the high impedance probe to the links between E3 and E5.

(10) Set the generator to 50.2 MHz. Adjust L5 for minimum level indication on the RF voltmeter.

(11) Set the generator to 40.45 MHz. Adjust L2 for minimum level indication on the RF voltmeter.

(12) Reconnect input cable P1 to chassis. Reconnect the LO input to J1.

(13) Set the receiver frequency to 2.00000 MHz.

(14) Connect the output of the signal generator to the chassis-mounted first mixer input coax connector. Set the signal generator frequency to 2.000 MHz and output level to 1 μV emf.

(15) Connect the RF voltmeter, with the 50 ohms input impedance adapter, to the IF OUT connector, J2 on the rear panel. Select CW, 3 kHz bandwidth, MAN. Turn IF GAIN control fully clockwise.

(16) Tune the signal generator to maximum output, as indicated on the RF voltmeter. Peak T5 for maximum output.

(17) With the signal generator input level of 1 μV emf at the A2 input the signal plus noise to noise ratio at the audio output in a 3 kHz bandwidth should be at least 10 dB and frequencies between 500 kHz and 30 MHz.

(18) Set the receiver supply switch to off. Disconnect all test equipment. Reinstate all module connections.

ALIGNMENT PROCEDURE - RF AMPLIFIER/LOWPASS FILTER A1

21 Signal generator, item 6; RF voltmeter, item 3.

NOTE: Do not attempt to align the four-section low pass filter without a spectrum analyser/tracking generator. The alignment details are shown on Fig. 8-1.

Procedure

22 (1) Connect the signal generator to the antenna input socket A1 J1 and the RF voltmeter with 50 ohm termination to the RF out connector W2P1. Set the signal generator level to -10 dBm.

(2) If the RF amplifier is linked out ensure that the loss through the A1 module does not exceed 1.5 dB from 500 kHz to 30 MHz.

(3) If the RF amplifier is linked in ensure that the gain through the A1 module is 8 dB $\pm$ 2 dB from 500 kHz to 30 MHz.

(4) Reconnect W2P1 to chassis connector J5.

(5) With a signal generator input level of 1 μV emf at the A1 input the signal plus noise to noise ratio at the audio output in a 3 kHz bandwidth should be at least 10 dB with the RF amplifier linked out and at least 15 dB with it linked in.

ALIGNMENT PROCEDURE - FRONT PANEL MODULES A9A1 AND A9A2

23 No adjustments are provided on either the A9A1 or A9A2 modules and alignment is not required.

FINAL GAIN AND AGC ADJUSTMENTS

24 Following the adjustment or replacement of the A1, A2, A3, A4 or A5 modules the following final gain and agc adjustments should be made.

(1) Connect the signal generator to the antenna input A1J1 and set the frequency to 1.02 MHz.

(2) Connect the audio power meter to the MONITOR line output, J3 pins 4 and 17. Connect the dvm to DIV AGC output, J3, pins 21 and 9. Set R105 on A4 fully clockwise.

(3) Set the receiver to USB, agc short and tune it to the signal generator. Set the signal generator level to 60 μV emf. Adjust R129 on A4 for 0 dBm output on the power meter.

(4) Reduce signal generator level to 1 μV emf, select MAN. and IF GAIN fully clockwise and adjust R39 on A4 for 0 dBm on the power meter.

(5) Select AGC SHORT and increase the signal generator level to 60 μV emf. Adjust R47 on A4 for an indication of 8.5 ± 0.05V on the dvm.

(6) Connect the RF voltmeter with high impedance probe to TP1 on A4 board. Note the level on the RF voltmeter and slowly turn R105 on A4 anti-clockwise until this level is reduced by 1 dB.

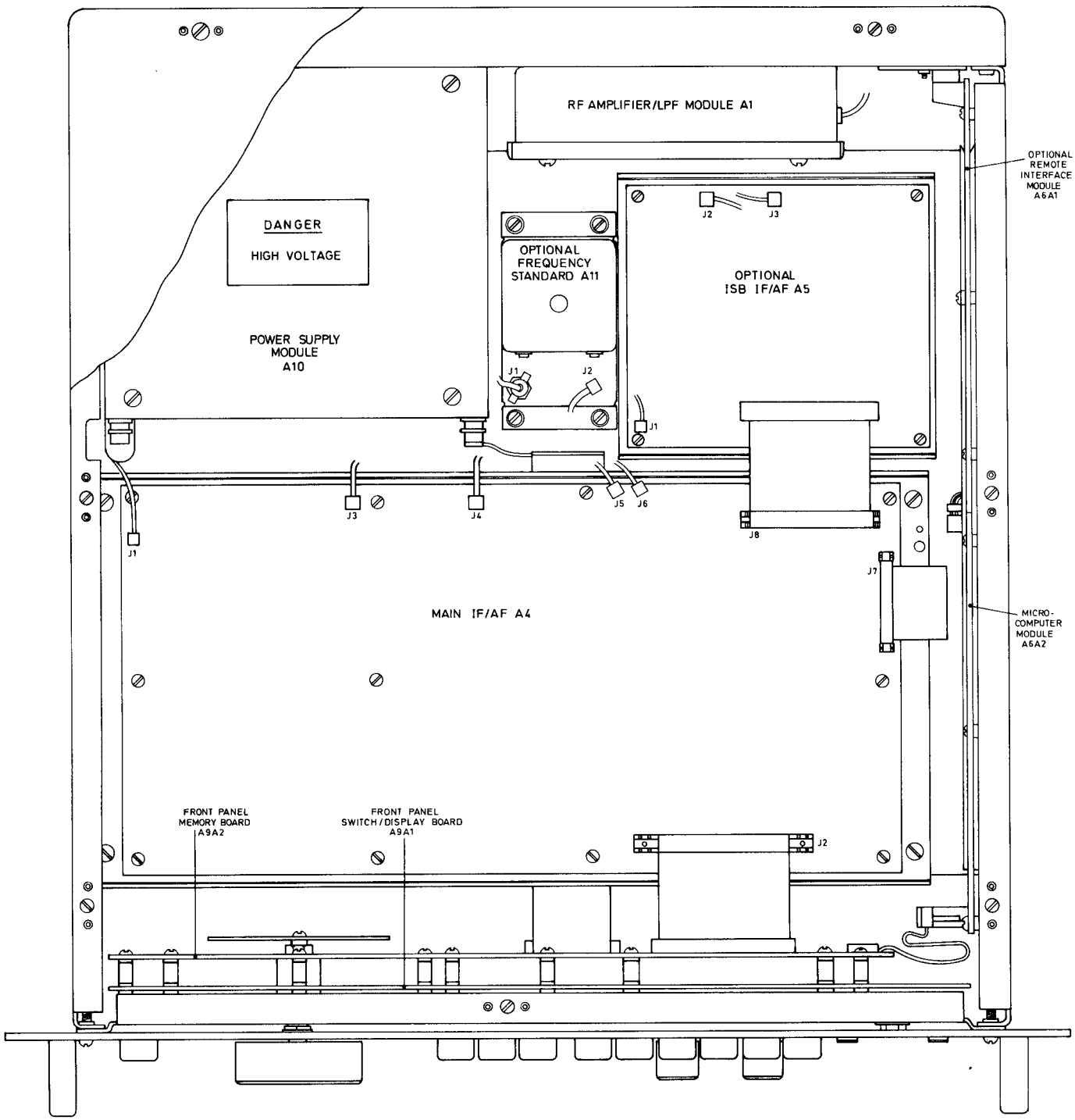
25 If the receiver is fitted with the ISB option the following adjustments should be made.

(1) Connect the dvm to the ISB DIV AGC output, J3 pins 22 and 9.

(2) Set the receiver to LSB, agc SHORT and tune it to the signal generator. Set the signal generator output level to 60 μV emf. Adjust R132 on A4 for 0 dBm output on the power meter.

(3) Reduce the signal generator level to 1 μV emf, select MAN. and set the IF GAIN control fully clockwise. Adjust R19 on A5 for 0 dBm on the power meter.

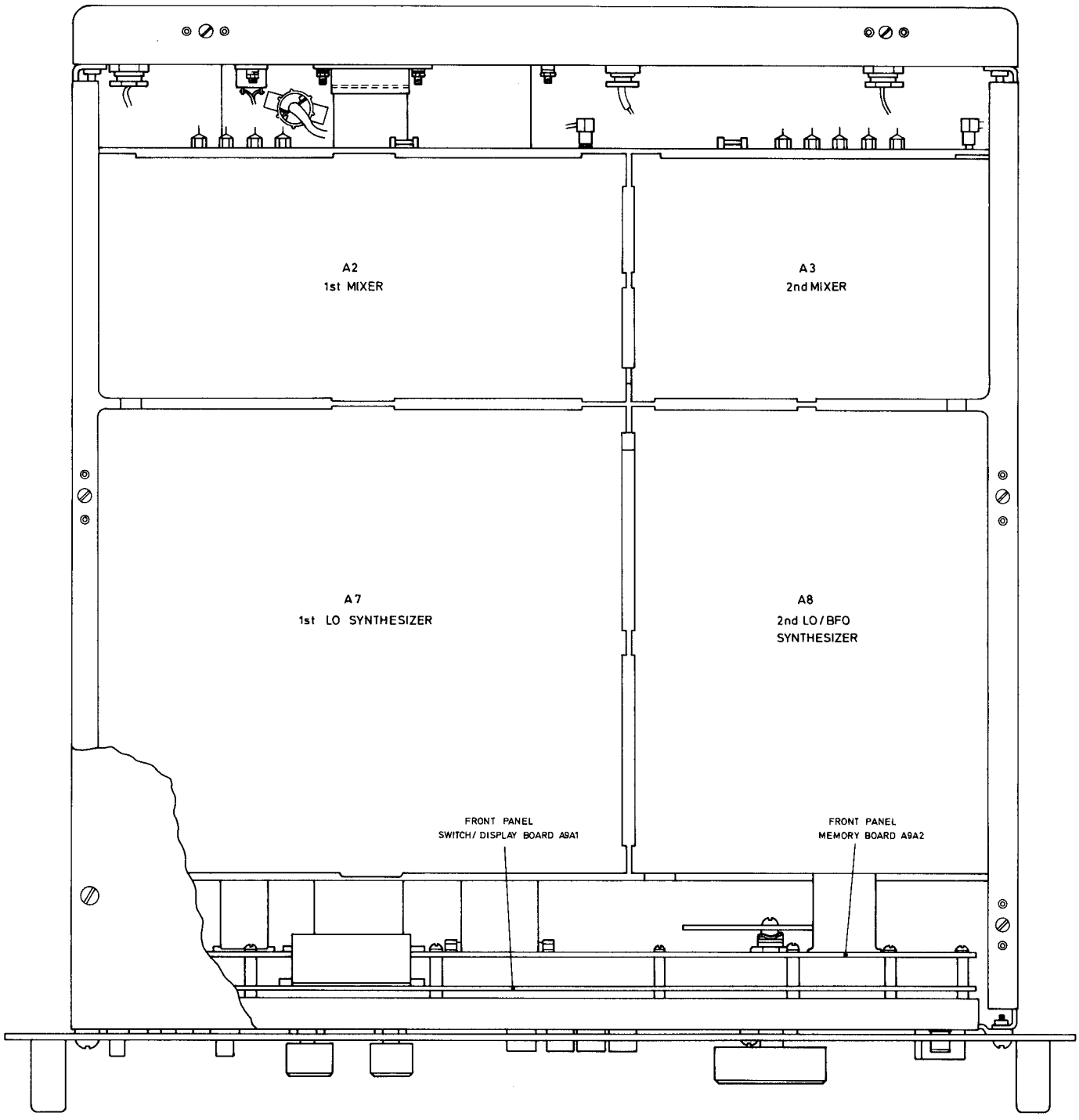
(4) Select AGC SHORT and increase the signal generator level to 60 μV emf. Adjust R23 on A5 for an indication of 8.5 ± 0.05V on the dvm.



RACAL TH1496

Top View: RA.1792 Receiver

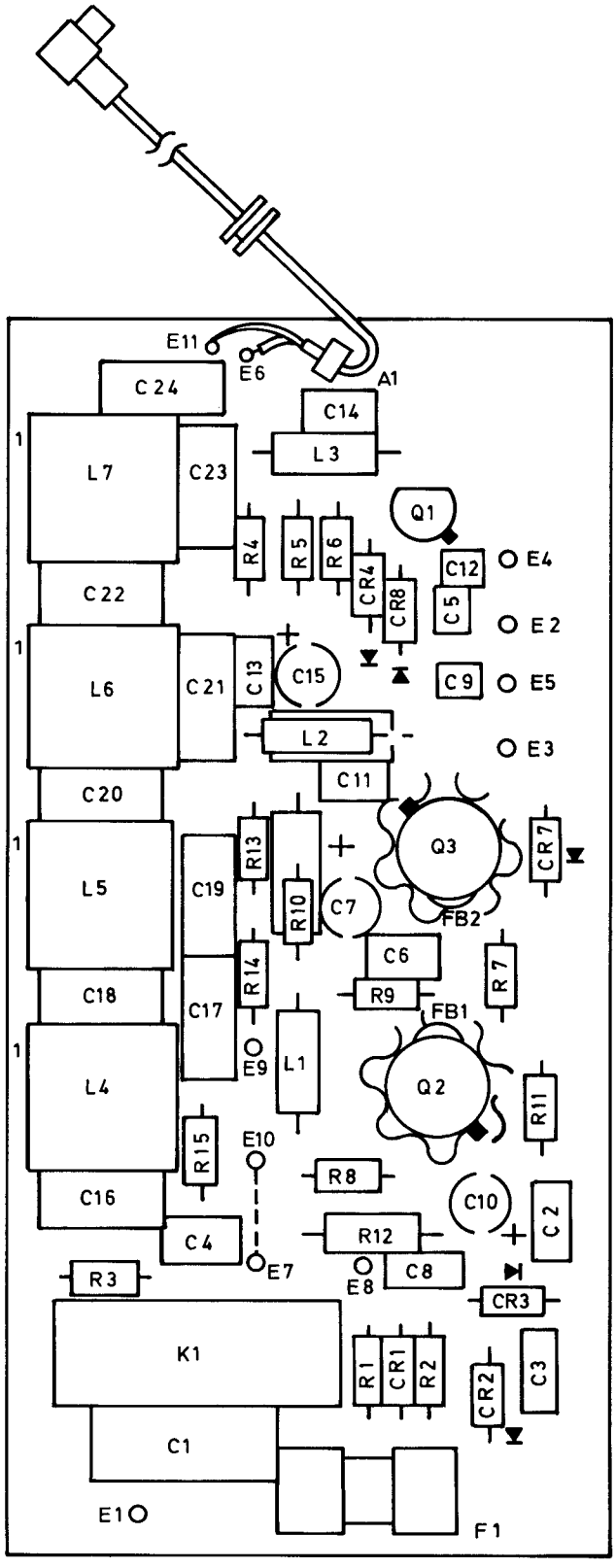
Fig.6.1



RACAL
TH1496

Bottom View RA.1792 Receiver

Fig.6.2

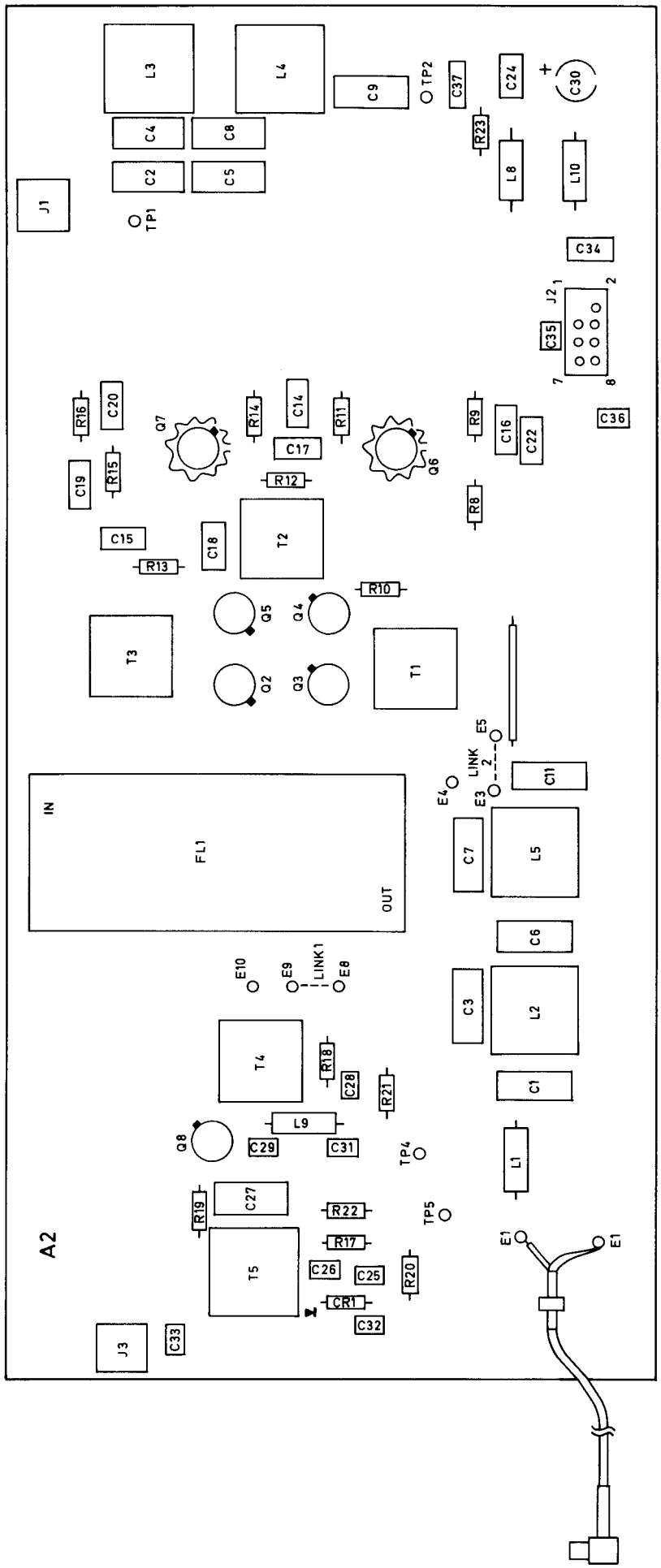


RACAL

TH1496	CO8078
1	

Component Layout: RF Amplifier / Low Pass Filter Board A1

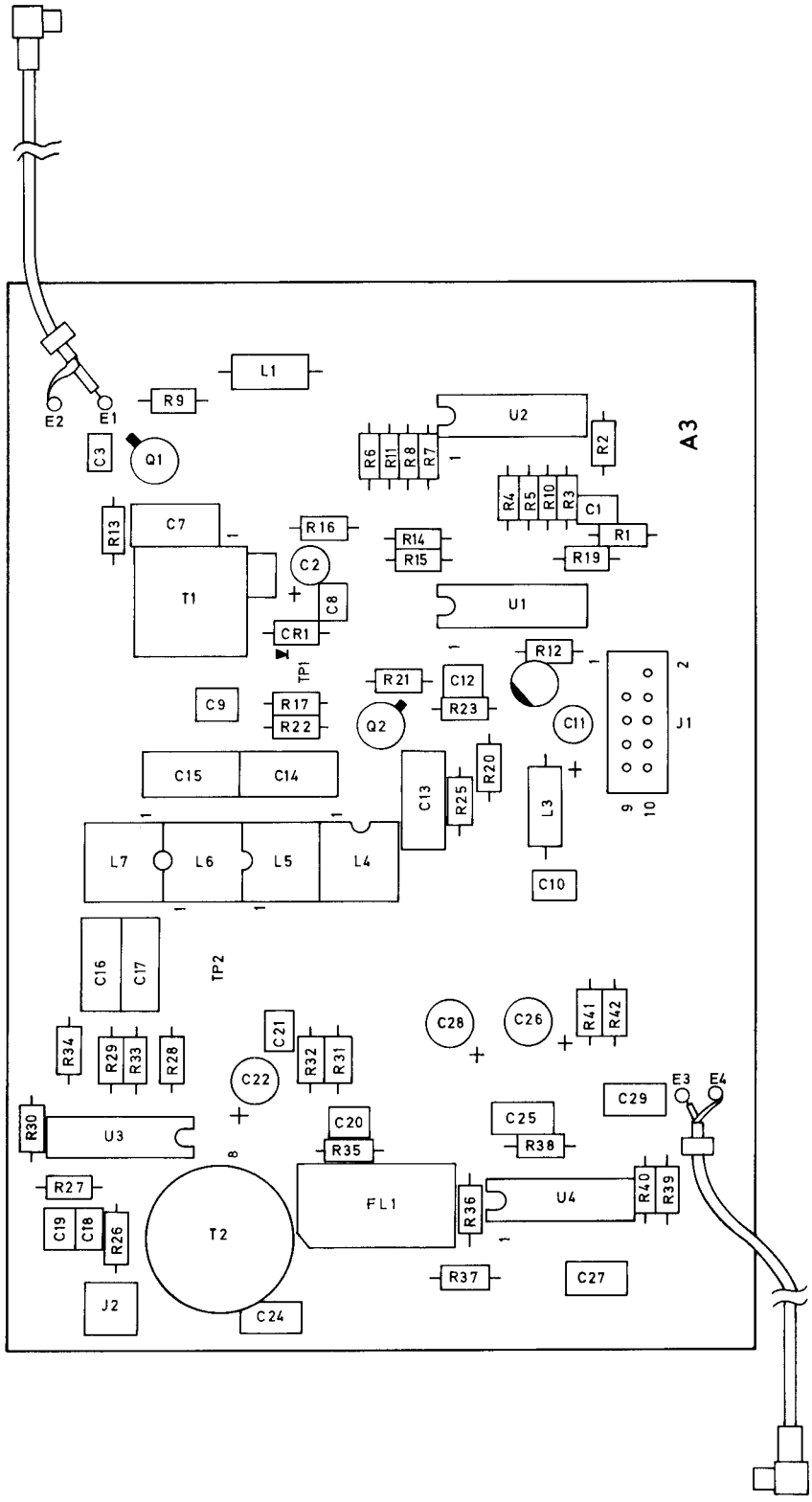
Fig.6.3



RACAL
TH1496 DO8184
2

Component Layout: First Mixer Board, A2

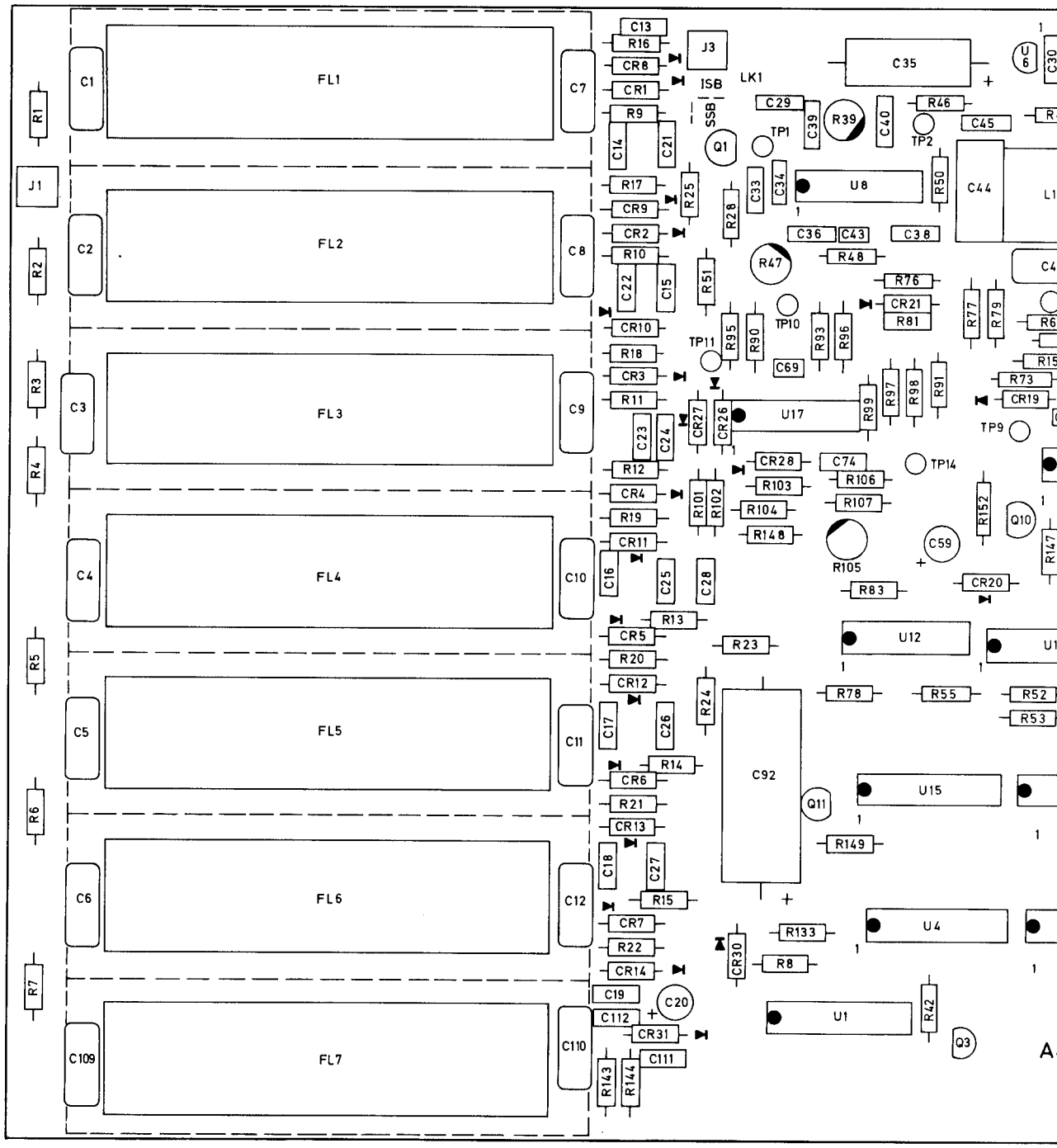
Fig.6.4

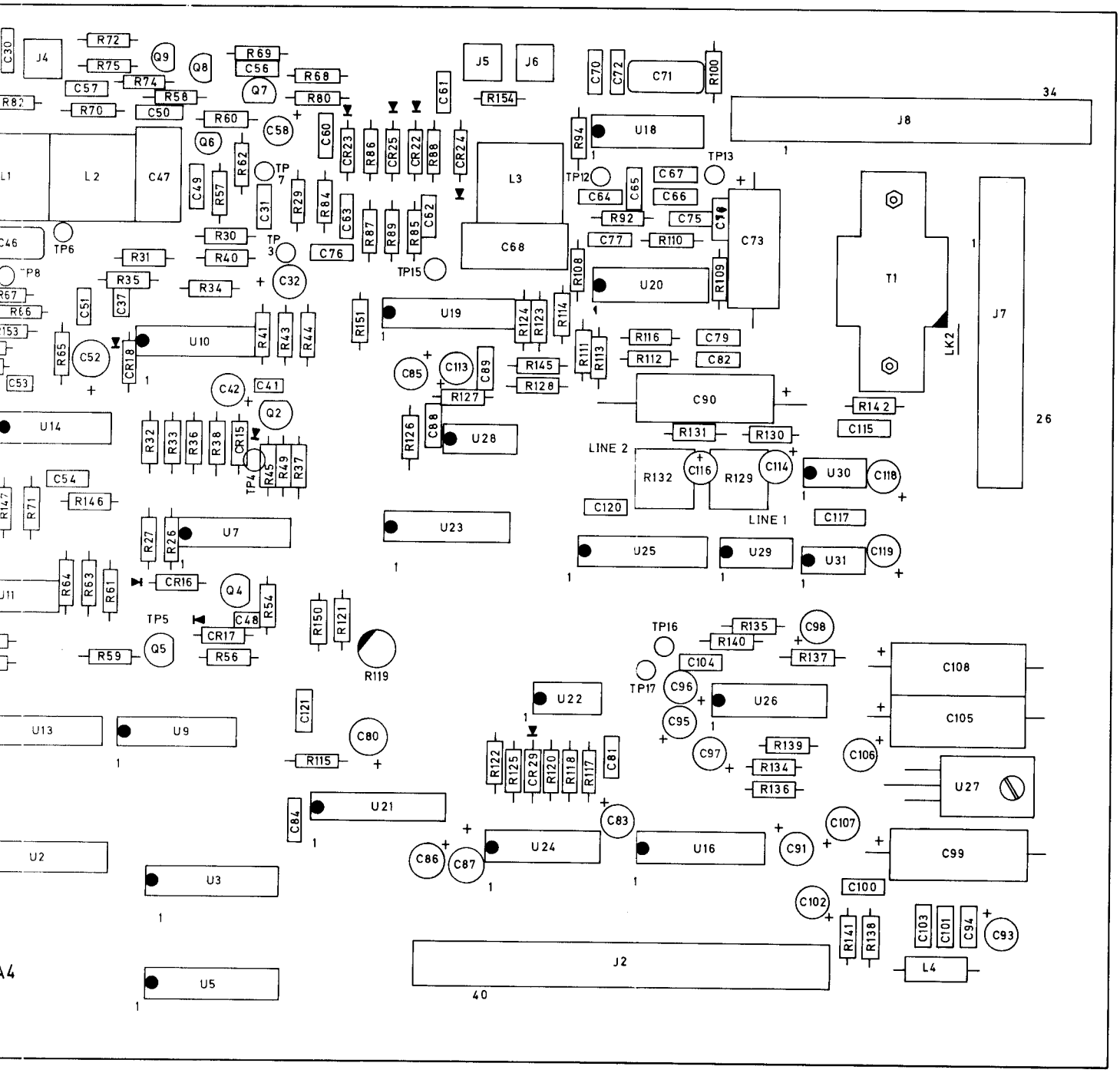


RACAL
TH1496 DO8093
1

Component Layout : Second Mixer Board, A3

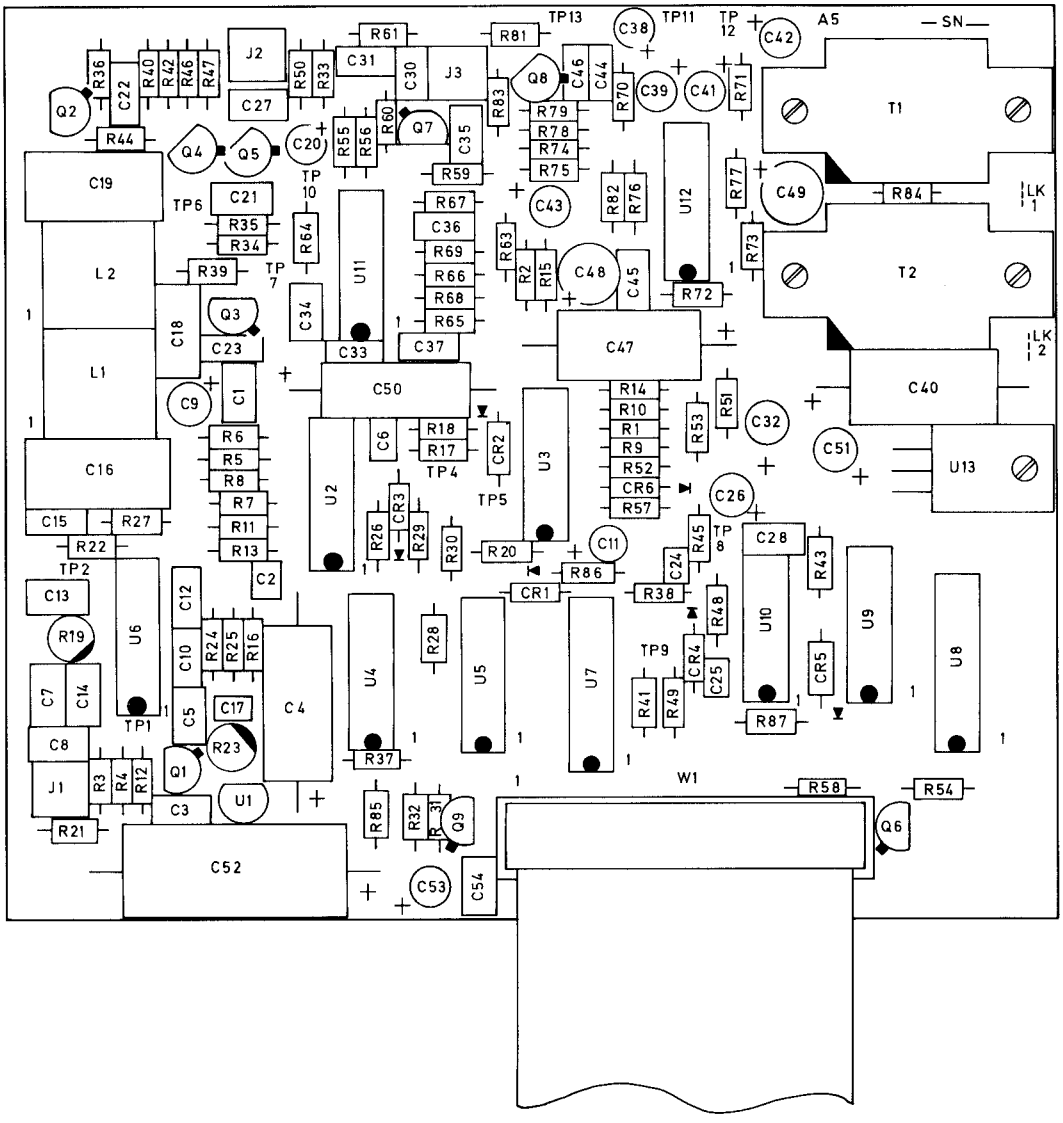
Fig.6.5


FL1
FL2
FL3
FL4
FL5
FL6
FL7
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C109
C110
R1
R2
R3
R4
R5
R6
R7
J1
J3
LK1
ISB
SSB
Q1
TP1
TP2
TP9
TP10
TP11
TP14
U8
U17
U12
U15
U4
U1
C92
R105
R39
R47
C35
C44
C45
C59
Q10
Q11
Q3
CR20
CR30
C20
R42
R133
R149
R83
R78
R55
R52
R53
R73
CR19
CR21
R81
R76
R48
R46
C29
C36
C43
C38
C69
R106
R107
R103
R104
R148
CR28
C74
R152
R147
C112
C111
R143
R144
CR31
C19
R8
R22
CR14
CR7
R15
C18
C27
C17
C26
R14
CR6
R21
CR13
R24
R23
CR5
R20
CR12
R13
C16
C25
C28
CR4
R19
CR11
R12
C23
C24
CR27
CR26
R99
R97
R98
R91
R101
R102
R95
R90
R93
R96
C69
R51
R25
R26
C33
C34
R50
C39
C40
C14
C21
C22
C15
R17
CR9
CR2
R10
R18
CR3
R11
R9
CR8
CR1
R16
C13
C30
C4
R6
R15
U6
U1
A



Component Layout :
Main IF/AF Board A4

Fig. 6.6

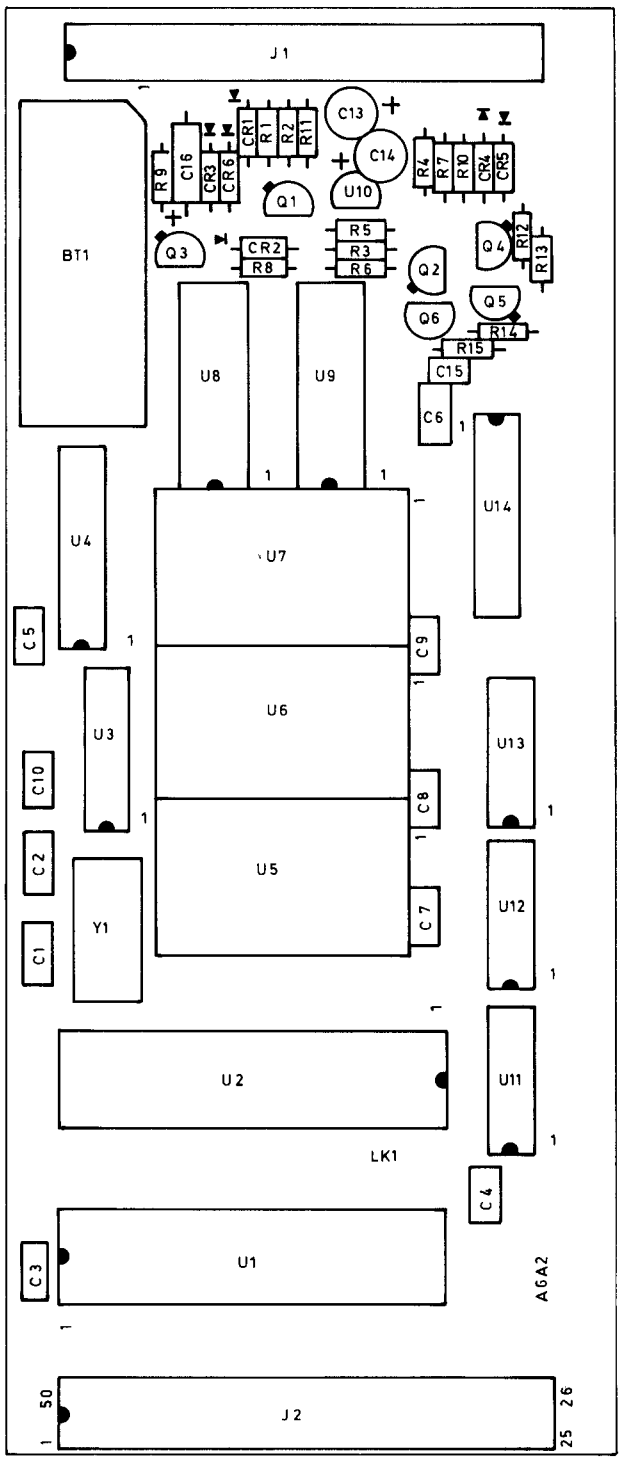


RACAL

TH1496	DO8109
1	

Layout : ISB IF/AF Board A5

Fig. App. 1.2

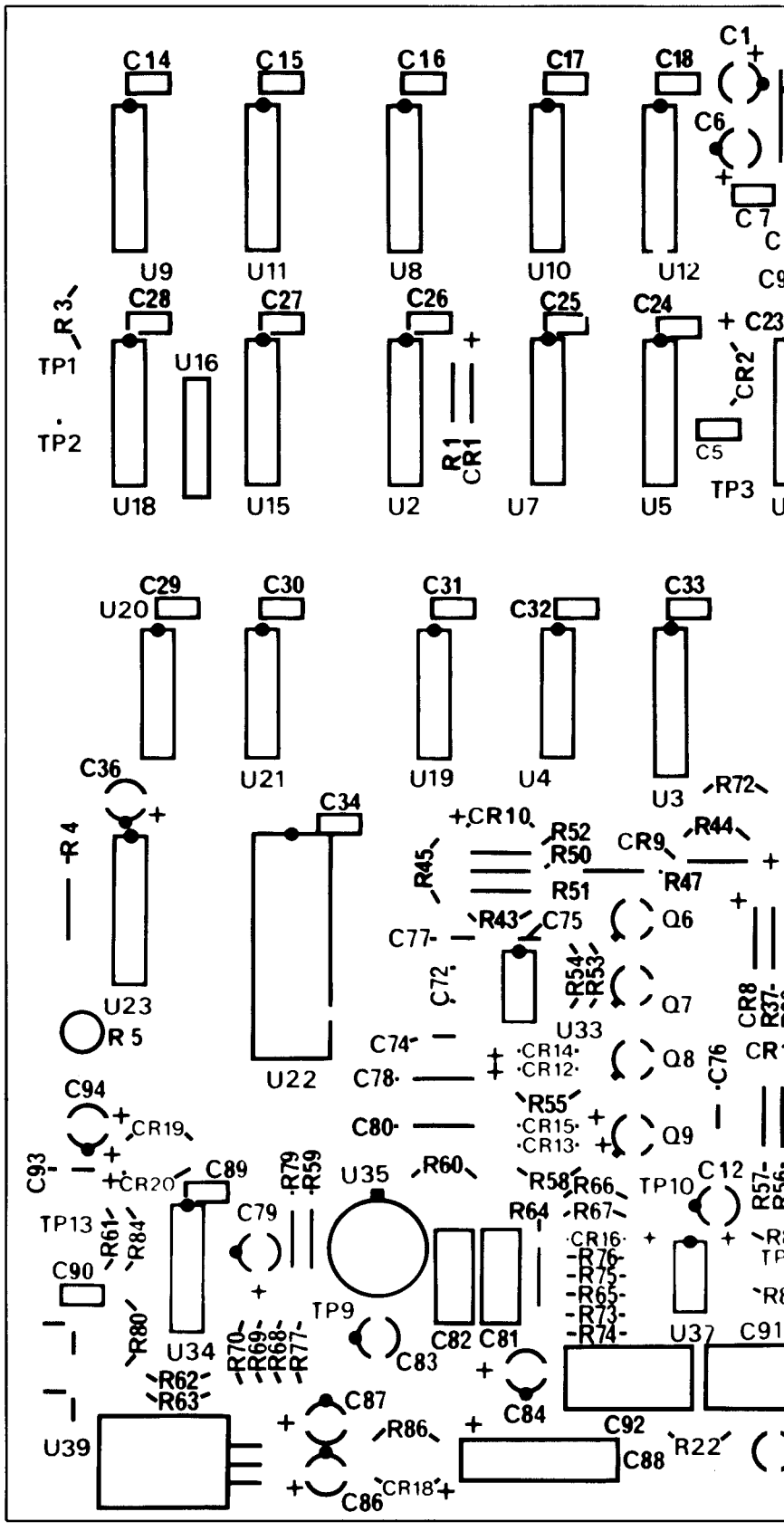


RACAL

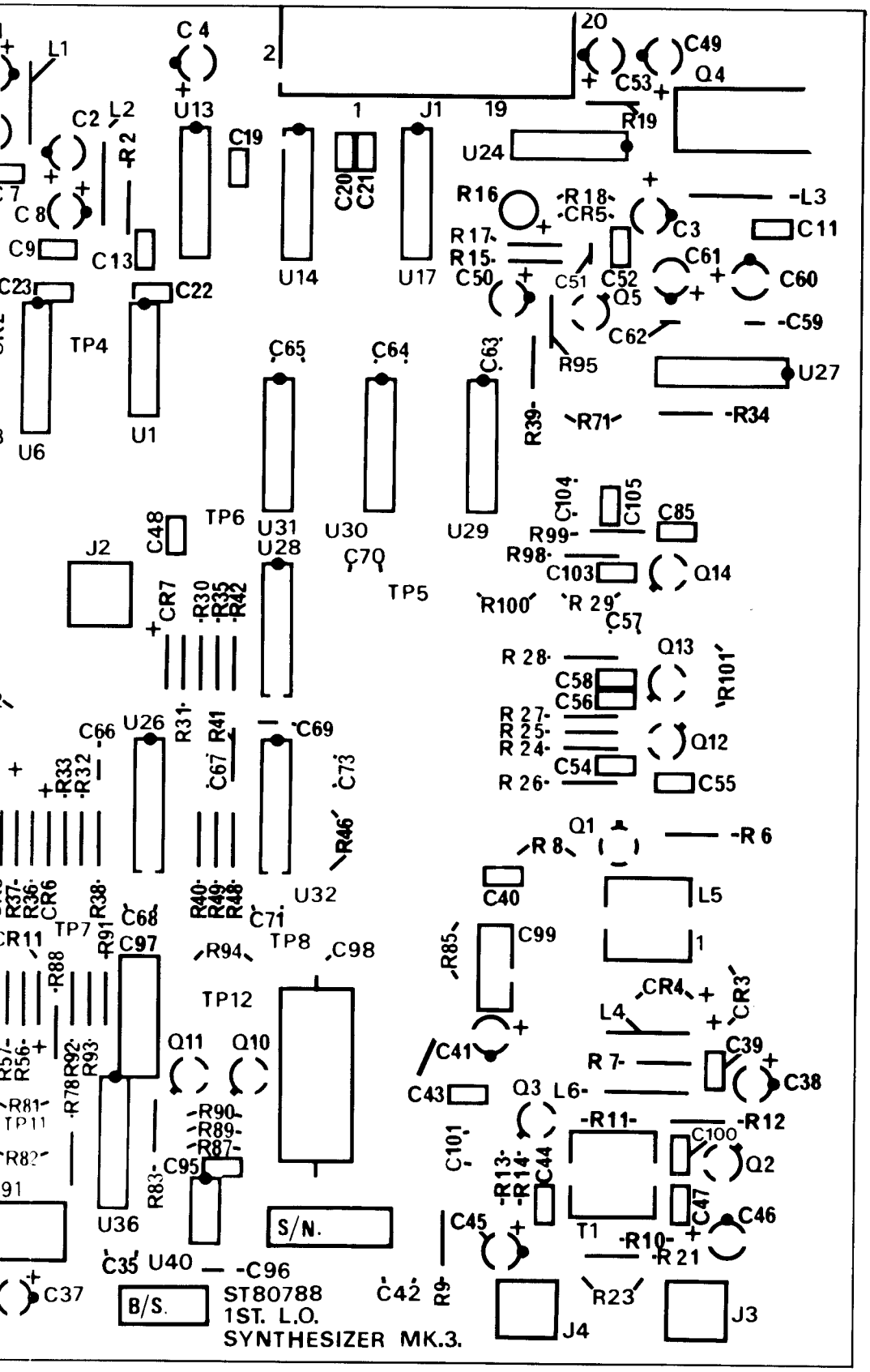
TH1496	DO8203
1	

Component Layout : Microcomputer Board A6A2

Fig.6.7

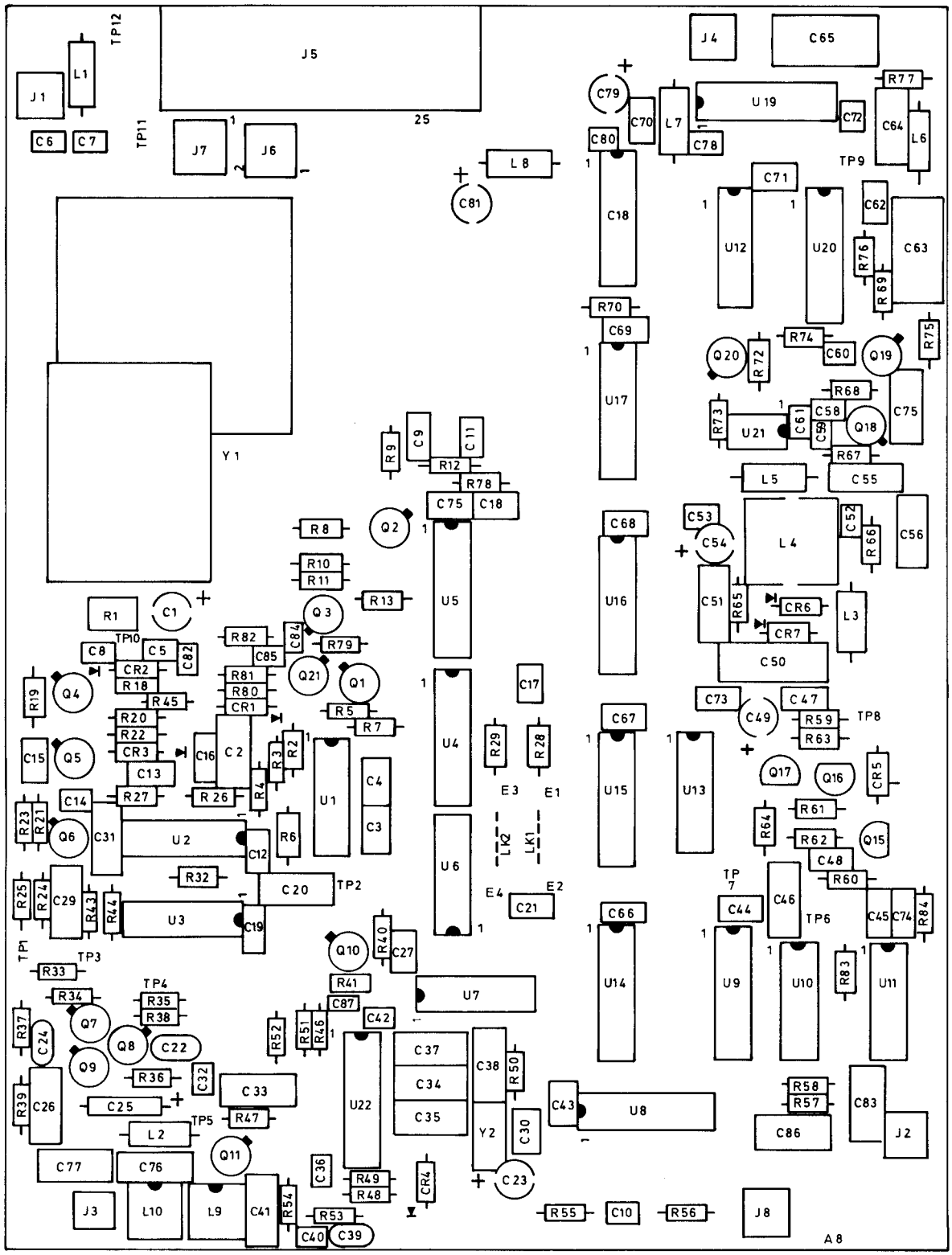


FOR EARLIER VERSIONS SEE APPENDIX 4



Component Layout:
First LO Synthesizer A7

Fig.6

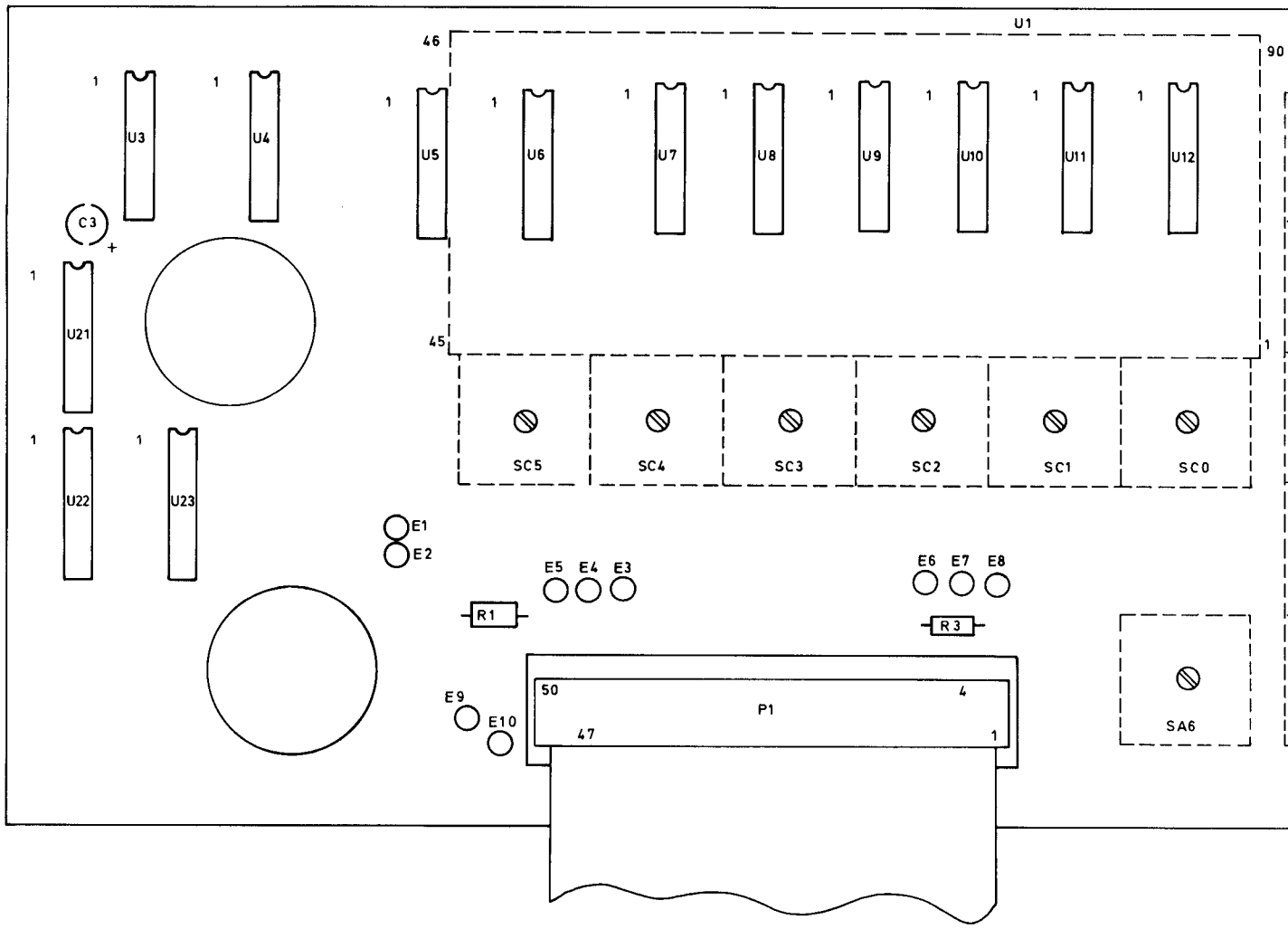


RACAL

TH1496	DO8283
1	

Component Layout: Second LO/BFO Synthesizer Board A8

Fig.6.9


U1
46
90
45
1
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
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+
U21
U22
U23
SC5
SC4
SC3
SC2
SC1
SC0
E1
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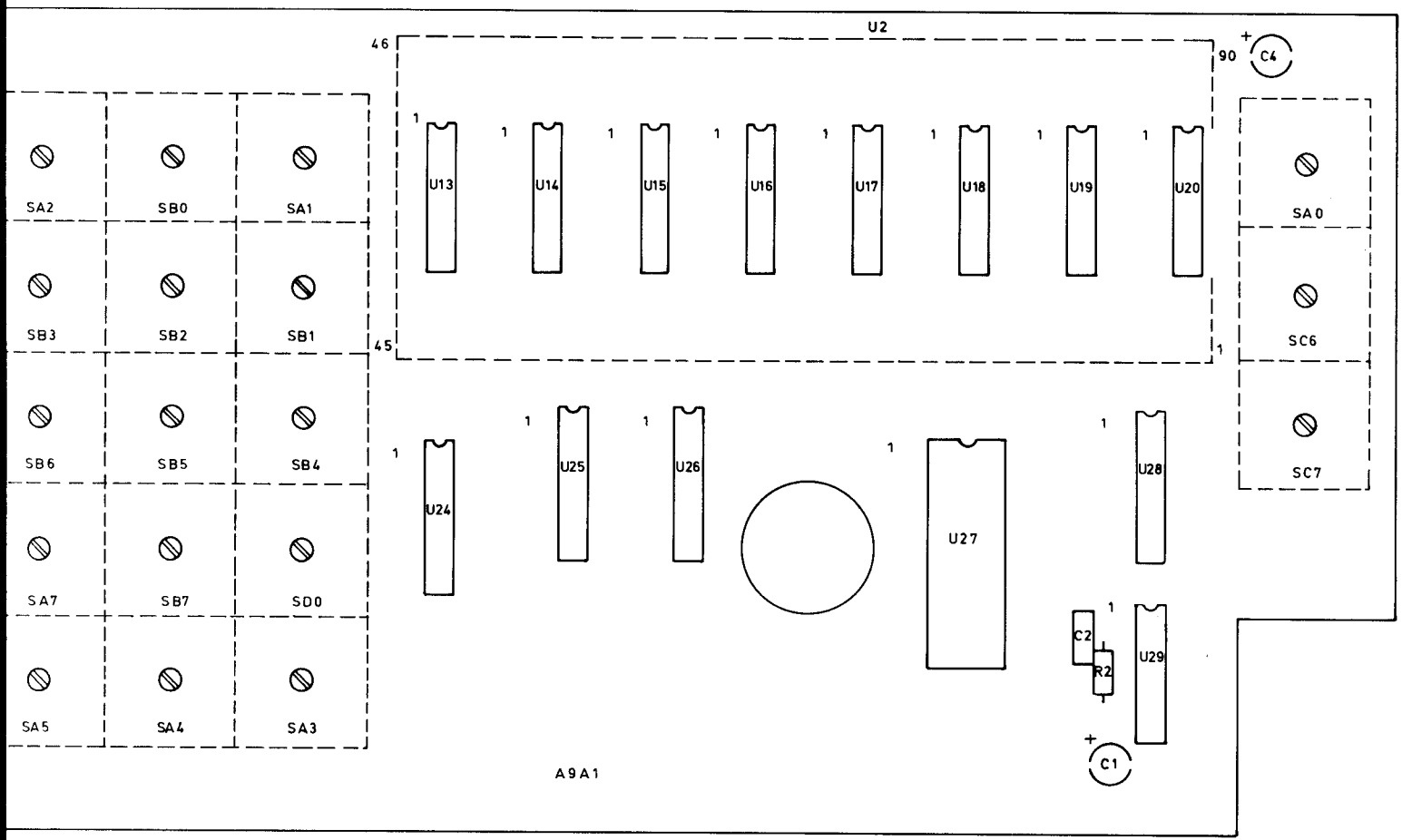
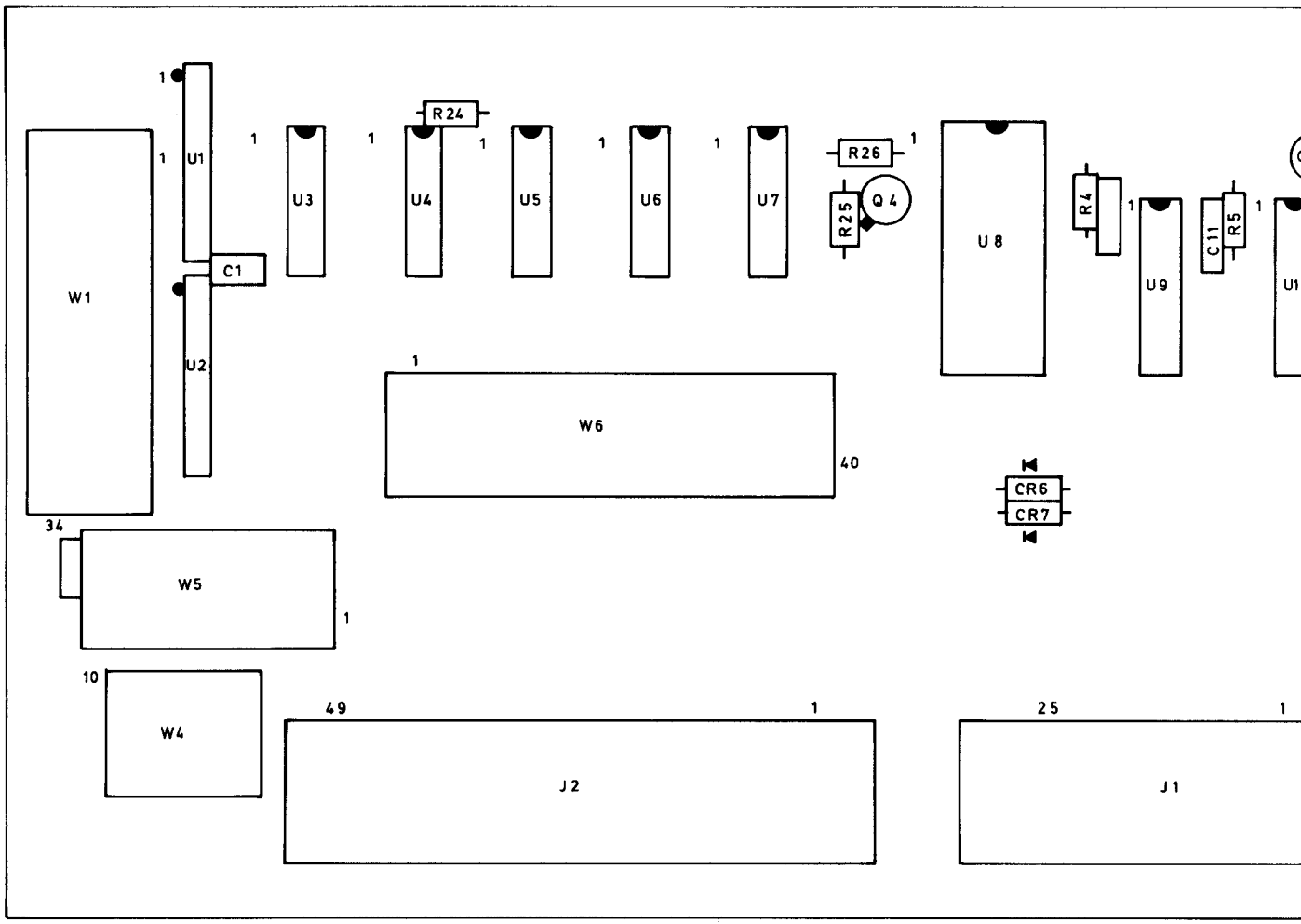
E9
E10
50
4
P1
47
1
SA6

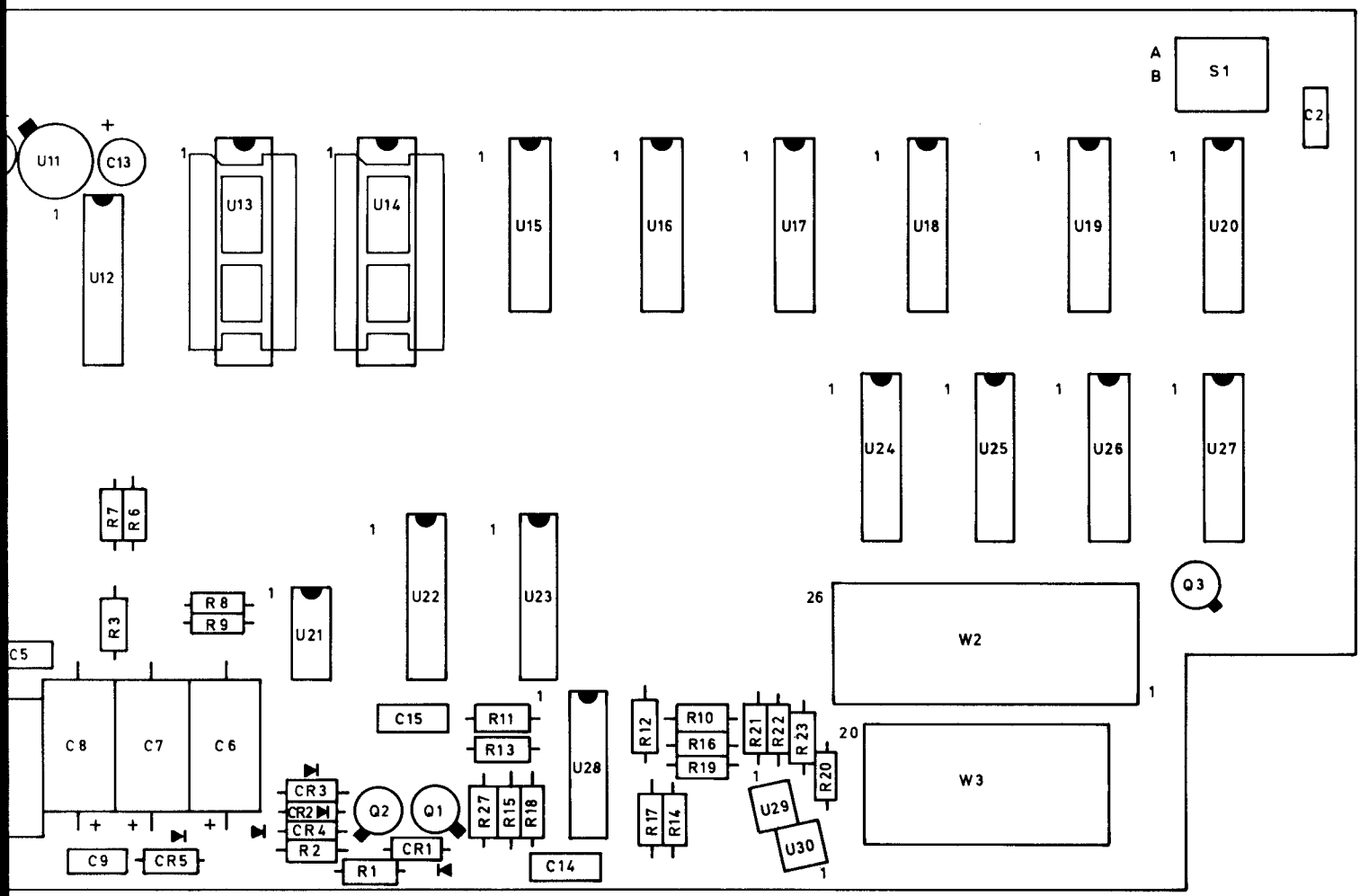


Component Layout: Front Panel Switch and Display Board A9A1 Fig.6.10

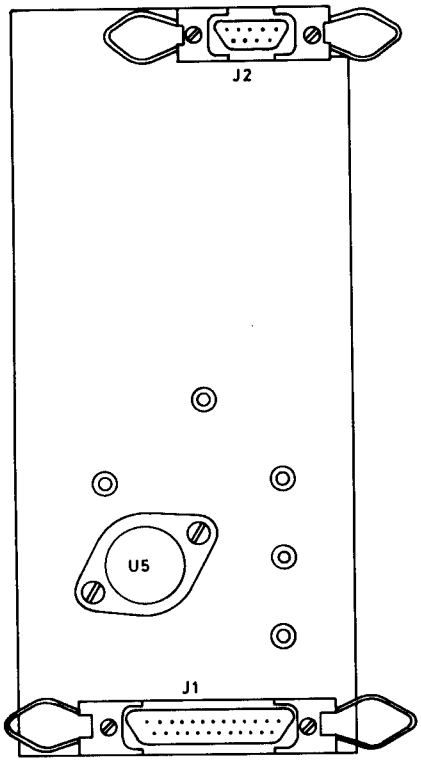


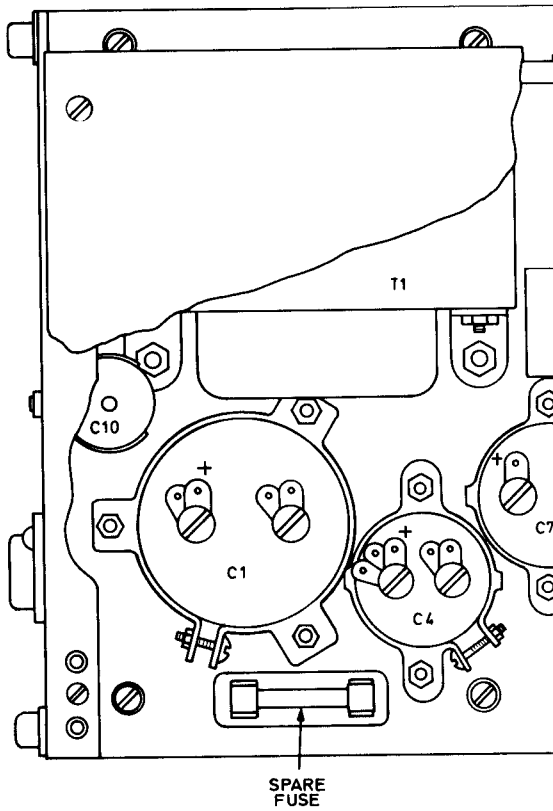
RACAL

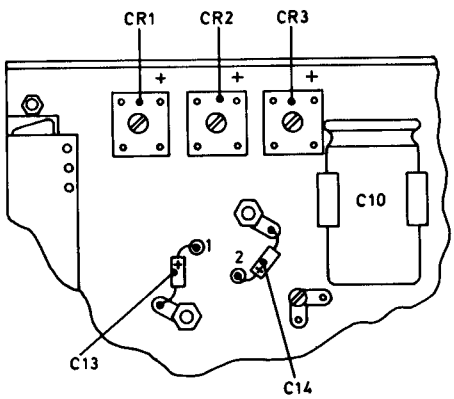
TH1496	DO8234
1	



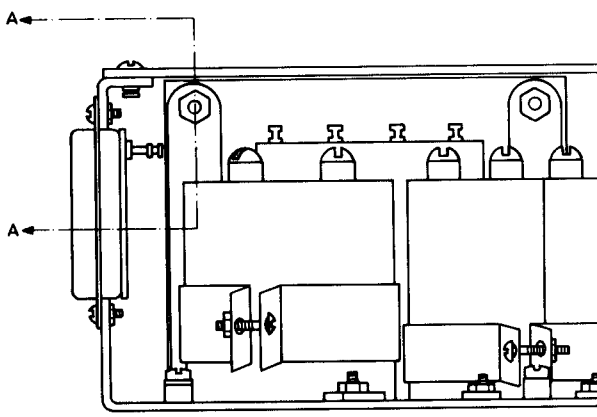
Component Layout:
Front Panel Memory Board A9A2 **Fig.6.11**

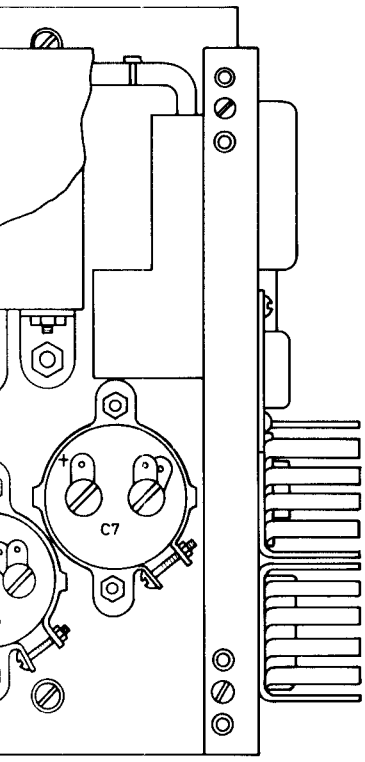


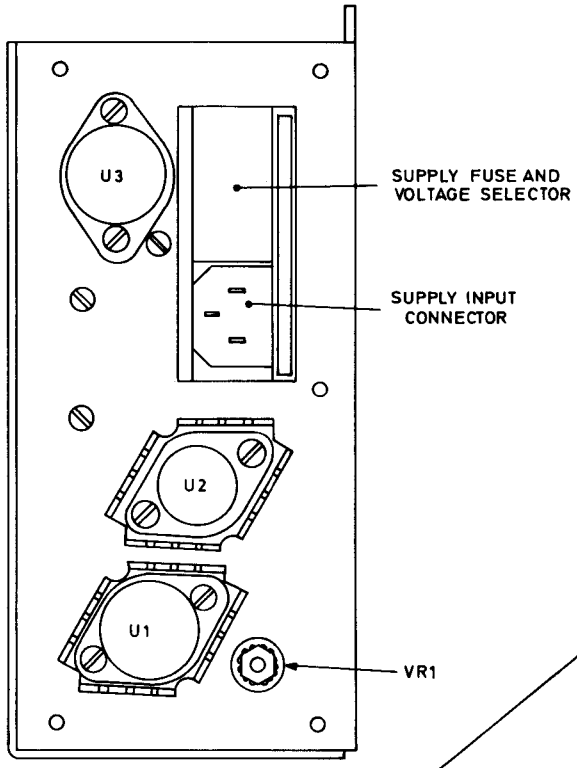


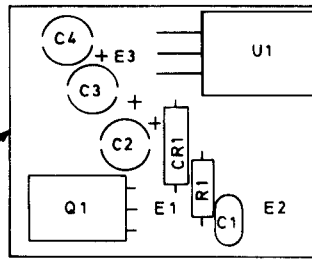


SECTION A-A

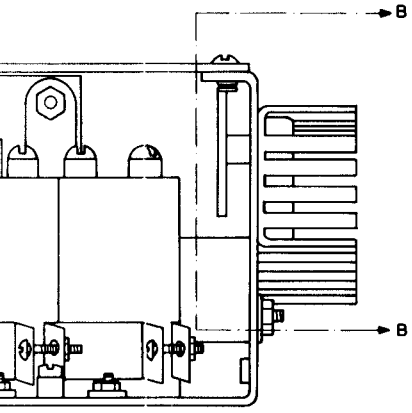


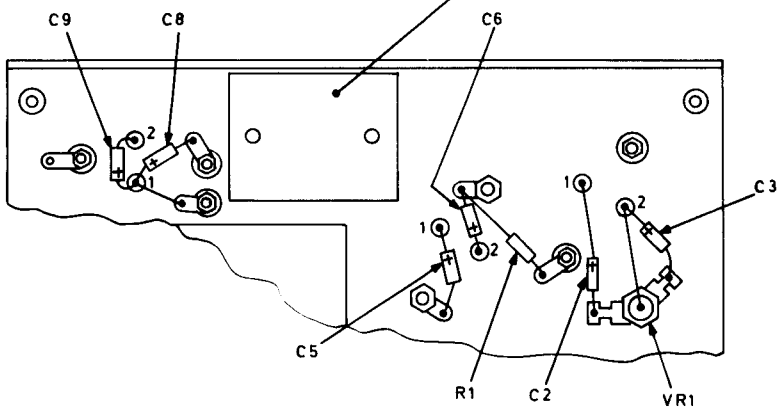






20V REGULATOR BOARD
(A10A2 - B08717)





SECTION B-B

Component Layout:
AC Power Supply Module A10

F

CHAPTER 7

COMPONENTS LIST

CONTENTS

ORDERS FOR SPARE PARTS

In order to expedite handling of part orders, please quote:-

(1) Type and serial number of equipment.

(2) Circuit reference, description, Racal part number, and manufacturer of part required.

(3) Quantity required.

NOTE: If the equipment is designed on a modular basis, please include the type and description of the module for which the replacement part is required.

CHASSIS COMPONENTS (ST80767)

(earlier versions ST80766)

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number
Resistors					
R1	50K	Potentiometer (IF GAIN)			B08243
R2	1K	Potentiometer (VOLUME)			B08244
R3	1K	Metal Oxide		2	910388
Capacitors					
C1	.001	Feedthrough	500	20	938668
C2	.001	Feedthrough	500	20	938668
C3	.001	Feedthrough	500	20	938668
C4	.001	Feedthrough	500	20	938668
C5	.001	Feedthrough	500	20	938668
C6	.001	Feedthrough	500	20	938668
C7	.001	Feedthrough	500	20	938668
C8	.001	Feedthrough	500	20	938668
C9	.001	Feedthrough	500	20	938668
Connectors					
J1		Socket, bulkhead, BNC (REF IN/OUT)			919499
J2		Socket, bulkhead, BNC (MAIN IF OUT)			919499
		Mating plug for J1, J2			900038
J3		Socket, 25-way (AF OUT)			938656
		Mating plug, 25-way			916489
		Shell junction, straight			918108
		Retainer			914245
J4		PHONES jack			938636
J5		Plug, bulkhead			938654
J6		Plug, bulkhead			938654
		Mating connector, snap-on			938423
J7		Socket, bulkhead, BNC (LO OUT)			919499
		Mating plug, BNC			900038
J8		Not used			
J9		Socket, bulkhead, BNC (ISB IF OUT)			919499
		Mating plug, BNC			900038

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number
Switches					
S1		SUPPLY			938535
S2		REF INT/EXT			938666
S3		METER			938535
S4		L/S			938535
Assemblies					
		RF Amp/LPF Module			ST08076
		A1 RF Amp/LPF Board			ST08078
		A2 First Mixer			ST08184
		A3 Second Mixer			ST08093
		A4 Main IF/AF			ST08276
		A5 ISB IF/AF (Option)			ST08109
		A6A1 Score Interface (Option)			ST08459
		A6A2 Microcomputer			ST08203
	*	A7 First LO Synthesizer			ST80788
		A8 Second LO/BFO Synthesizer			ST08283
		A9A1 Switch and Display Board			ST08198
		A9A2 Memory Board			ST08234
		A10 AC Power Supply Module			ST80784
		A10 DC Power Supply Module (option)			ST80762
		A11 Frequency Standard Module (option)			ST08140
Miscellaneous					
		Loudspeaker			B08269
		Encoder disc			B08194
		Encoder shaft assembly			B08195
		Knob (Frequency)			BA43873
		Knob (IF GAIN, VOLUME)			927731
		Knob end cap			927734
		Cable assemblies:			
		W1			B07909/1
		W2			B07909/2
		W3			B07909/3
		W4			B07909/4
		W5			B07909/16
		W6			B07909/5
		W7			B07910/1
		W12			B07910/6
		W16			C08336

* Earlier Versions ST 08545 (Appendix 4)

Cct. Ref.	Value	Description	Rat	Tol. %	Racal Part Number
Miscellaneous					
		W19			D08222
		W21			B08263
		W22			B08262
		W25			B07910/8

RF AMPLIFIER/LPF MODULE (ST08076)

Connectors			
A1J1		Socket, BNC (ANT. INPUT)	938474
		Mating plug, BNC	900038
A1J2		Plug, 4-pin	938475
		Mating socket	938658
Miscellaneous			
		RF Amplifier/LPF Board A1	ST 08078
E1		Lighting Arrestor	911141
		Box Spanner (for tuning knob removal)	AD81031

RF AMPLIFIER/LPF BOARD A1 (ST08078)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R2	4.7k	Metal Oxide	$\frac{1}{4}$	2	913490
R3	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R4	2.2k	Metal Oxide	$\frac{1}{4}$	2	916546
R5	4.7k	Metal Oxide	$\frac{1}{4}$	2	913490
R6	2.2k	Metal Oxide	$\frac{1}{4}$	2	916546
R7	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R8	470	Metal Oxide	$\frac{1}{4}$	2	920758
R9	270	Metal Oxide	$\frac{1}{4}$	2	910391
R10	47	Metal Oxide	$\frac{1}{4}$	2	917063
R11	10	Metal Oxide	$\frac{1}{4}$	2	920736
R12	22	Metal Oxide	$\frac{1}{4}$	2	920743
R13	270	Metal Oxide	$\frac{1}{4}$	2	910391
R14	18	Metal Oxide	$\frac{1}{4}$	2	916545
R15	270	Metal Oxide	$\frac{1}{4}$	2	910391
Capacitors			V		
C1	1	Polyester	100	+20	931163
C2	0.1	Ceramic	50	±20	938406
C3	0.1	Ceramic	50	±20	938406
C4	1	Ceramic	50	±20	938401
C5	0.01	Ceramic		±20	938053
C6	3p	Silver Mica		$\pm\frac{1}{2}$pf	938404
C7	1	Tantalum	35	±20	938405
C8	0.1	Ceramic	50	+20	938406
C9	0.01	Ceramic		±20	938053
C10	6.8	Tantalum	35	±20	938030
C11	1	Ceramic	50	+20	938401
C12	0.01	Ceramic		±20	938053
C13	0.1	Ceramic	50	±20	938406
C14	0.1	Ceramic	50	±20	938406
C15	6.8	Tantalum	35	±20	938030

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C16	110p	Silver Mica		2	938409
C17	10p	Silver Mica		½pf	938410
C18	150p	Silver Mica	350	1p	902238
C19	75p	Silver Mica		2	938411
C20	110p	Silver Mica		2	938409
C21	91p	Silver Mica		2	938412
C22	120p	Silver Mica	350	1p	902236
C23	43p	Silver Mica		2	938413
C24	82p	Silver Mica	350	1p	902232
Diodes					
CR1		IN3600			926132
CR2		IN3600			926132
CR3		IN916			913480
CR4		IN916			913480
CR5		Not used			
CR6		Not used			
CR7		IN916			913480
CR8		IN916			913480
Transistors					
Q1		Silicon (2N5089)			938417
Q2		Silicon (2N3866)			917219
Q3		Silicon (2N5160)			938418
Inductors					
L1	15µH	Choke		10	915850
L2	100µH	Choke			919471
L3	100µH	Choke			919471
L4		Coil, Variable			AT81393
L5		Coil, Variable			AT81394
L6		Coil, Variable			AT81395
L7		Coil, Variable			AT81396

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Miscellaneous					
F1		Fuse, 1 Amp, ¼ x 5/8 Std Blo			938415
XF1		Fuse Holder			938414
FB1		Ferrite Bead			907488
FB2		Ferrite Bead			907488
K1		Relay, Reed 2 Form A			938416

1ST MIXER BOARD A2 (ST 08184)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1		Not used			
R2		Not used			
R3		Not used			
R4		Not used			
R5		Not Used			
R6		Not Used			
R7		Not Used			
R8	1.2k	Metal Oxide		2	911179
R9	150	Metal Oxide		2	910389
R10	100k	Metal Oxide		2	915190
R11	22	Metal Oxide		2	920743
R12	1k	Metal Oxide		2	913489
R13	100k	Metal Oxide		2	915190
R14	22	Metal Oxide		2	920743
R15	1.2k	Metal Oxide		2	911179
R16	150	Metal Oxide		2	910389
R17	220	Metal Oxide		2	910390
R18	220	Metal Oxide		2	910390
R19	10	Metal Oxide		2	920736
R20	1k	Metal Oxide		2	913489
R21	100	Metal Oxide		2	910388
R22	10k	Metal Oxide		2	914042
R23	47	Metal Oxide		2	917063
Capacitors			V		
C1	100p	Silver Mica	350	±1p	902234
C2	43p	Silver Mica	350	2	938413
C3	91p	Silver Mica	350	2	938412
C4	390p	Silver Mica	350	2	902248
C5	33p	Silver Mica	350	±1p	902222

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C6	100p	Silver Mica	350	1p	902234
C7	43p	Silver Mica	350	2	938413
C8	150p	Silver Mica	350	1p	902238
C9	47p	Silver Mica	400	1p	938834
C10		Not used			
C11	68p	Silver Mica	350	1p	902230
C12		Not Used			
C13	0.1	Ceramic	50	20	938406
C14	680p	Ceramic			938479
C15	0.1	Ceramic	50	20	938406
C16	680p	Ceramic			938479
C17	680p	Ceramic			938479
C18	2.2p	Ceramic			938480
C19	680p	Ceramic			938479
C20	680p	Ceramic			938479
C21		Not Used			
C22	0.1	Ceramic	50	20	938406
C23		Not Used			
C24	0.1	Ceramic	50	20	938406
C25	0.01	Ceramic		20	938053
C26	1000p	Ceramic		20	938408
* C27	27p	Silver Mica	350	1p	902220
C28	1000p	Ceramic		20	938408
C29	1000p	Ceramic		20	938408
C30	15	Tantalum	20	20	938034
C31	0.01	Ceramic		20	938053
C32	1000p	Ceramic		20	938408
C33	1000p	Ceramic		20	938408
C34	0.1	Ceramic	50	20	938406
C35	0.01	Ceramic		20	938053
C36	0.01	Ceramic		20	938053
C37	0.01	Ceramic	250	20	916187

*Earlier Versions 33p. 902222

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Diodes					
CR1		KS8379			938424
Transistors					
Q1		Not used			
Q2		Silicon (Matched BSV81)			A08298
Q3		Silicon (Matched BSV81)			A08298
Q4		Silicon (Matched BSV81)			A08298
Q5		Silicon (Matched BSV81)			A08298
Q6		Silicon (2N3866)			917219
Q7		Silicon (2N3866)			917219
Q8		Silicon (U310)			932518
Transformers					
T1		RF Wide Band			AT80404
T2		RF Wide Band			AT81405
T3		RF Wide Band			AT81406
T4					AT81407
T5					AT81398
Inductors					
L1	0.27μH	Choke RF			938481
L2		RF Variable Coil			AT81395
L3		RF Variable Coil			AT81402
L4		RF Variable Coil			AT81880
L5		RF Variable Coil			AT81403
L6		Not used			
L7		Not used			
L8	10μH	Choke			921209
L9	15μH	Choke		10	915850
L10	15μH	Choke		10	915850

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Connectors					
J1		Plug, Coaxial RF			938429
J2		Plug, 8-way			B06846-4
J3		Plug, Coaxial RF			938429
Miscellaneous					
FL1	40.455MHz	Filter			BD80550

2ND MIXER BOARD A3 (ST 08093)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	100	Metal Oxide	¼	±2	910388
R2	220k	Metal Oxide	¼	±2	921771
R3	22k	Metal Oxide	¼	±2	913493
R4	22k	Metal Oxide	¼	±2	913493
R5	4.7k	Metal Oxide	¼	±2	919490
R6	100k	Metal Oxide	¼	±2	915190
R7	390	Metal Oxide	¼	2	916331
R8	2.2k	Metal Oxide	¼	2	916546
R9	220	Metal Oxide	¼	2	910390
R10	22k	Metal Oxide	¼	±2	913493
R11	27	Metal Oxide	¼	±2	920745
R12	560	Metal Oxide	¼	±2	917061
R13	10	Metal Oxide	¼	±2	920736
R14	10k	Metal Oxide	¼	2	914042
R15	1k	Metal Oxide	¼	2	913489
R16	220	Metal Oxide	¼	2	910390
R17	100	Metal Oxide	¼	±2	910388
R18		Not Used			
R19	100	Metal Oxide	¼	±2	910388
R20	100	Metal Oxide	¼	±2	910388
R21	39k	Metal Oxide	¼	±2	900993
R22	4.7k	Metal Oxide	¼	±2	919490
R23	56	Metal Oxide	¼	±2	917055
R24	500	Variable		20	938426
R25	2.2k	Metal Oxide	¼	2	916546
R26	1k	Metal Oxide	¼	2	913489
R27	47	Metal Oxide	¼	2	917063
R28	470	Metal Oxide	¼	2	920758
R29	470	Metal Oxide	¼	2	920758
R30	1k	Metal Oxide	¼	2	913489

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R31	39	Metal Oxide	$\frac{1}{4}$	±2	917062
R32	10	Metal Oxide	$\frac{1}{4}$	±2	920736
R33	100	Metal Oxide	$\frac{1}{4}$	±2	910388
R34	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R35	1k	Metal Oxide	$\frac{1}{4}$	2	913489
R36	1k	Metal Oxide	$\frac{1}{4}$	2	913489
R37	47	Metal Oxide	$\frac{1}{4}$	2	917063
R38	330	Metal Oxide	$\frac{1}{4}$	2	915690
R39	330	Metal Oxide	$\frac{1}{4}$	2	915690
R40	1k	Metal Oxide	$\frac{1}{4}$	2	913489
R41	47	Metal Oxide	$\frac{1}{4}$	2	917063
R42	47	Metal Oxide	$\frac{1}{4}$	2	917063
Capacitors			V		
C1	0.01	Ceramic		±20	938053
C2	1	Tantalum	35	±20	938405
C3	1000p	Ceramic		±20	938408
C4	1000p	Ceramic		±20	938408
C5		Not Used			
C6		Not Used			
* C7	27p	Silver Mica	350	±1p	902220
C8	1000p	Ceramic		±20	938408
C9	1000p	Ceramic		±20	938408
C10	1000p	Ceramic		±20	938408
C11	15	Tantalum	20	±20	938034
C12	1000p	Ceramic		±20	938408
C13	68p	Silver Mica	350	±1p	902230
C14	68p	Silver Mica	350	±1p	902230
C15	68p	Silver Mica	350	±1p	902230
C16	82p	Silver Mica	350	±1p	902232
C17	330p	Silver Mica	350	±1p	902246
C18	1000p	Ceramic		±20	938408
C19	1000p	Ceramic		±20	938408
C20	1000p	Ceramic		±20	938406

* Earlier Version 33p, 902222

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C21	1000p	Ceramic		+20	938408
C22	1	Tantalum	35	±20	938405
C23		Not Used			
C24	0.1	Ceramic		+20	938406
C25	0.1	Ceramic		±20	938406
C26	15	Tantalum	20	+20	938034
C27	0.1	Ceramic		±20	938406
C28	15	Tantalum	20	±20	938034
C29	0.1	Ceramic		±20	938406
Diodes					
CR1		KS8379			938424
Transistors					
Q1		Silicon (U310)			932518
Q2		Silicon (2N918)			906517
Integrated Circuits					
U1		CA3046			922907
U2		LM324N			925944
U3		MC1496P			938427
U4		MC1733			938429
Transformers					
T1		RF Variable			AT81398
T2		RF Variable			AT81399
Inductors					
L1	15µH	Choke RF			915850
L2		Not Used			
L3	100µH	Choke RF			919471
L4		Coil RF Variable			AT81397
L5		Coil RF Variable			AT81397

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Inductors					
L6		Coil RF Variable			AT81397
L7		Coil RF Variable			AT81397
Connectors					
J1		Plug, 10-way			B06846-5
J2		Plug, Coaxial RF			938429
Miscellaneous					
FL1		Filter VTD-3-A			938425

MAIN IF/AF BOARD A4 (ST 08276)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R2	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R3	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R4	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R5	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R6	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R7		Ref. FL7			
R8	47	Metal Oxide	$\frac{1}{4}$	±2	917063
R9	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R10	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R11	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R12	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R13	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R14	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R15	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R16	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R17	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R18	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R19	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R20	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R21	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R22	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R23	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R24	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R25	100	Metal Oxide	$\frac{1}{4}$	±2	910388
R26	22k	Metal Oxide	$\frac{1}{4}$	±2	913493
R27	1.5k	Metal Oxide	$\frac{1}{4}$	±2	911166
R28	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R29	47	Metal Oxide	$\frac{1}{4}$	±2	917063
R30	22k	Metal Oxide	$\frac{1}{4}$	±2	913493

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R31	3.3k	Metal Oxide	$\frac{1}{4}$	2	910111
R32	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R33	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R34	2.7k	Metal Oxide	$\frac{1}{4}$	2	916548
R35	560	Metal Oxide	$\frac{1}{4}$	2	917061
R36	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R37	100k	Metal Oxide	$\frac{1}{4}$	2	915190
R38	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R39	2k	Variable			938440
R40	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R41	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R42	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R43	680	Metal Oxide	$\frac{1}{4}$	2	910113
R44	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R45	220k	Metal Oxide	$\frac{1}{4}$	2	921771
R46	47	Metal Oxide	$\frac{1}{4}$	2	917063
R47	50k	Variable			938441
R48	680	Metal Oxide	$\frac{1}{4}$	2	910113
R49	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R50	4.7k	Metal Oxide	$\frac{1}{4}$	2	913490
R51	2.2k	Metal Oxide	$\frac{1}{4}$	2	916546
R52	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R53	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R54	220k	Metal Oxide	$\frac{1}{4}$	2	921771
R55	1k	Metal Oxide	$\frac{1}{4}$	2	913489
R56	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R57	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R58	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R59	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R60	100	Metal Oxide	$\frac{1}{4}$	2	910388
R61	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R62	1k	Metal Oxide	$\frac{1}{4}$	2	913489
R63	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R64	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R65	15k	Metal Oxide	$\frac{1}{4}$	2	920645

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R66	1k	Metal Oxide	¼	±2	913489
R67	18k	Metal Oxide	¼	±2	900994
R68	1k	Metal Oxide	¼	±2	913489
R69	15k	Metal Oxide	¼	±2	920645
R70	1.2k	Metal Oxide	¼	±2	911179
R71	10k	Metal Oxide	¼	±2	914042
R72	1k	Metal Oxide	¼	±2	913489
R73	22k	Metal Oxide	¼	±2	913493
R74	10k	Metal Oxide	¼	±2	914042
R75	390	Metal Oxide	¼	±2	916331
R76	3.3k	Metal Oxide	¼	±2	910111
R77	1k	Metal Oxide	¼	±2	913489
R78	1k	Metal Oxide	¼	±2	913489
R79	1k	Metal Oxide	¼	±2	913489
R80	47	Metal Oxide	¼	±2	917063
R81	22k	Metal Oxide	¼	±2	913493
R82	39	Metal Oxide	¼	±2	938440
R83	22k	Metal Oxide	¼	±2	913493
R84	3.3k	Metal Oxide	¼	±2	910111
R85	1k	Metal Oxide	¼	±2	913489
R86	10k	Metal Oxide	¼	±2	914042
R87	1k	Metal Oxide	¼	±2	913489
R88	10k	Metal Oxide	¼	±2	914042
R89	10k	Metal Oxide	¼	±2	914042
R90	47k	Metal Oxide	¼	±2	913496
R91	22k	Metal Oxide	¼	±2	913493
R92	3.9k	Metal Oxide	¼	±2	915074
R93	47k	Metal Oxide	¼	±2	913496
R94	4.7k	Metal Oxide	¼	±2	913490
R95	100k	Metal Oxide	¼	±2	915190
R96	100k	Metal Oxide	¼	±2	915190
R97	18k	Metal Oxide	¼	±2	900994
R98	12k	Metal Oxide	¼	±2	917952
R99	27k	Metal Oxide	¼	±2	913494
R100	10	Metal Oxide	¼	±2	920736

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R101	2.2k	Metal Oxide	$\frac{1}{4}$	±2	916546
R102	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R103	47k	Metal Oxide	$\frac{1}{4}$	±2	913496
R104	18k	Metal Oxide	$\frac{1}{4}$	±2	900994
R105	10k	Variable			935310
R106	180k	Metal Oxide	$\frac{1}{4}$	±2	920644
R107	18k	Metal Oxide	$\frac{1}{4}$	±2	900994
R108	6.8k	Metal Oxide	$\frac{1}{4}$	±2	910112
R109	3.3k	Metal Oxide	$\frac{1}{4}$	±2	910111
R110	470	Metal Oxide	$\frac{1}{4}$	±2	920758
R111	3.3k	Metal Oxide	$\frac{1}{4}$	±2	910111
R112	3.3k	Metal Oxide	$\frac{1}{4}$	±2	910111
R113	1.5k	Metal Oxide	$\frac{1}{4}$	±2	911166
R114	3.3k	Metal Oxide	$\frac{1}{4}$	±2	910111
R115	47	Metal Oxide	$\frac{1}{4}$	±2	917063
R116	3.3k	Metal Oxide	$\frac{1}{4}$	±2	910111
R117	100k	Metal Oxide	$\frac{1}{4}$	±2	915190
R118	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R119	10k	Variable			935286
R120	100k	Metal Oxide	$\frac{1}{4}$	±2	915190
R121	1.8k	Metal Oxide	$\frac{1}{4}$	±2	911148
R122	100k	Metal Oxide	$\frac{1}{4}$	±2	915190
R123	100k	Metal Oxide	$\frac{1}{4}$	±2	915190
R124	22k	Metal Oxide	$\frac{1}{4}$	±2	913493
R125	100k	Metal Oxide	$\frac{1}{4}$	±2	915190
R126	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R127	8.2k	Metal Oxide	$\frac{1}{4}$	±2	918202
R128	2.2k	Metal Oxide	$\frac{1}{4}$	±2	916546
R129	2k	Variable			917845
R130	22	Metal Oxide	$\frac{1}{4}$	±2	920743
R131	22	Metal Oxide	$\frac{1}{4}$	±2	920743
R132	2k	Variable			917845
R133	10	Metal Oxide	$\frac{1}{4}$	±2	920736
R134	27k	Metal Oxide	$\frac{1}{4}$	±2	913494
R135	10k	Metal Oxide	$\frac{1}{4}$	±2	914042

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R136	4.7k	Metal Oxide	¼	±2	913490
R137	4.7k	Metal Oxide	¼	±2	913490
R138	100	Metal Oxide	¼	±2	910388
R139	100k	Metal Oxide	¼	±2	915190
R140	100k	Metal Oxide	¼	±2	915190
R141	100	Metal Oxide	¼	±2	910388
R142	33	Metal Oxide	¼	±2	917060
R143	1.5k	Metal Oxide	¼	±2	911166
R144	1k	Metal Oxide	¼	±2	913489
R145	1k	Metal Oxide	¼	±2	913489
R146		Not Used			
R147		Not Used			
R148		Not Used			
R149		Not Used			
R150	100k	Metal Oxide	¼	±2	915190
R151	100k	Metal Oxide	¼	±2	915190
R152	1k	Metal Oxide		2	913489
R153	270k	Metal Oxide		2	923598
R154	1k	Metal Oxide		2	913489
Capacitors			V		
C1 to C12		Part of filter assemblies FL1 to FL6			
C13	0.1	Ceramic	50	±20	938406
C14	0.1	Ceramic	50	±20	938406
C15	0.1	Ceramic	50	±20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C16	0.1	Ceramic	50	±20	938406
C17	0.1	Ceramic	50	±20	938406
C18	0.1	Ceramic	50	±20	938406
C19	0.1	Ceramic	50	±20	938406
C20	15	Tantalum	20	±20	938034
C21	0.1	Ceramic	50	±20	938406
C22	0.1	Ceramic	50	±20	938406
C23	0.1	Ceramic	50	±20	938406
C24	0.1	Ceramic	50	±20	938406
C25	0.1	Ceramic	50	±20	938406
C26	0.1	Ceramic	50	±20	938406
C27	0.1	Ceramic	50	±20	938406
C28	0.1	Ceramic	50	±20	938406
C29	0.1	Ceramic	50	±20	938406
C30	0.1	Ceramic	50	±20	938406
C31	0.1	Ceramic	50	±20	938406
C32	15	Tantalum	20	±20	938034
C33	0.1	Ceramic	50	±20	938406
C34	0.1	Ceramic	50	±20	938406
C35	100	Electrolytic	25		935140
C36	0.1	Ceramic	50	±20	938406
C37	1000p	Ceramic		±20	938408
C38	0.1	Ceramic	50	±20	938406
C39	0.1	Ceramic	50	±20	938406
C40	0.1	Ceramic	50	±20	938406
C41	0.022	Ceramic		±20	930219
C42	6.8	Tantalum	35	±20	938030
C43	0.01	Ceramic		±20	938053
C44	1500p	Silver Mica		±2	938435
C45	0.1	Ceramic	50	±20	938406
C46	82p	Silver Mica		±2	902232
C47	1500p	Silver Mica		±2	938435
C48	1000p	Ceramic		±20	938408
C49	0.1	Ceramic	50	±20	938406
C50	0.1	Ceramic	50	±20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C51	0.01	Ceramic		±20	938053
C52	15	Tantalum	20	±20	938034
C53	0.01	Ceramic		±20	938053
C54	0.1	Ceramic	50	±20	938406
C55		Not Used			
C56	0.1	Ceramic	50	±20	938406
C57	0.1	Ceramic	50	±20	938406
C58	15	Tantalum	20	±20	938034
C59	6.8	Tantalum	35	±20	938030
C60	0.1	Ceramic	50	±20	938406
C61	0.1	Ceramic	50	±20	938406
C62	0.1	Ceramic	50	±20	938406
C63	0.1	Ceramic	50	±20	938406
C64	0.1	Ceramic	50	±20	938406
C65	0.1	Ceramic	50	±20	938406
C66	0.1	Ceramic	50	±20	938406
C67	0.1	Ceramic	50	±20	938406
C68	3300p	Silver Mica		±2	938400
C69	0.01	Ceramic		±20	938053
C70	0.1	Ceramic	50	±20	938406
C71	100p	Silver Mica		±2	902234
C72	0.1	Ceramic	50	±20	938406
C73	100	Electrolytic	25		935140
C74	1	Ceramic		±20	938401
C75	0.1	Ceramic	50	±20	938406
C76	0.1	Ceramic	50	±20	938406
C77	0.1	Ceramic	50	±20	938406
C78	0.1	Ceramic	50	±20	938406
C79	0.1	Ceramic	50	±20	938406
C80	15	Tantalum	20	±20	938034
C81	0.1	Ceramic	50	±20	938406
C82	0.1	Ceramic	50	±20	938406
C83	4.7	Tantalum	35	±20	938033
C84	10p	Ceramic			938446
C85	6.8	Tantalum	35	±20	938030

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C86	1	Tantalum	35		938405
C87	1	Tantalum	35		938405
C88	4700p	Ceramic		±5	938437
C89	2200p	Ceramic		±5	938438
C90	220	Electrolytic	16		938436
C91	6.8	Tantalum	35	±20	938030
C92	470	Electrolytic	25		938439
C93	15	Tantalum	20	±20	938034
C94	0.1	Ceramic	50	±20	938406
C95	6.8	Tantalum	35	±20	938030
C96	6.8	Tantalum	35	±20	938030
C97	6.8	Tantalum	35	±20	938030
C98	6.8	Tantalum	35	±20	938030
C99	220	Electrolytic	16		938436
C100	0.1	Ceramic	50	±20	938406
C101	0.1	Ceramic	50	±20	938406
C102	15	Tantalum	20	±20	938034
C103	0.1	Ceramic	50	±20	938406
C104	0.1	Ceramic	50	±20	938406
C105	220	Electrolytic	16		938436
C106	6.8	Tantalum	35	±20	938030
C107	68	Tantalum	15	±20	938036
C108	220	Electrolytic	16		938436
C109	)	Part of Filter Assembly			
C110	)	FL7			
C111	0.1	Ceramic	50	±20	938406
C112	0.1	Ceramic	50	±20	938406
C113	15	Tantalum	20	±20	938034
C114		Not Used			
C115		Not Used			
C116		Not Used			
C117		Not Used			
C118		Not Used			
C119		Not Used			
C120	0.1	Ceramic	50	±20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C121	0.1	Ceramic	50	±20	938406
Diodes					
CR1		IN916			913480
CR2		IN916			913480
CR3		IN916			913480
CR4		IN916			913480
CR5		IN916			913480
CR6		IN916			913480
CR7		IN916			913480
CR8		IN916			913480
CR9		IN916			913480
CR10		IN916			913480
CR11		IN916			913480
CR12		IN916			913480
CR13		IN916			913480
CR14		IN916			913480
CR15		IN916			913480
CR16		IN916			913480
CR17		IN916			913480
CR18		IN916			913480
CR19		IN916			913480
CR20		IN916			913480
CR21		IN916			913480
CR22		IN916			913480
CR23		IN916			913480
CR24		IN916			913480
CR25		IN916			913480
CR26		IN916			913480
CR27		IN916			913480
CR28		IN916			913480
CR29		IN916			913480
CR30		IN916			913480
CR31		IN916			913480

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Transistors					
Q1		Silicon (2N5089)			938417
Q2		Silicon (2N5089)			938417
Q3		Silicon (2N5089)			938417
Q4		Silicon (T1S74)			938450
Q5		Silicon (2N3906)			914047
Q6		Silicon (2N5089)			938417
Q7		Silicon (2N5089)			938417
Q8		Silicon (2N5089)			938417
Q9		Silicon (2N5089)			938417
Q10		Not Fitted			
Q11		Not Fitted			
Integrated Circuits					
U1		4028			938454
U2		4042			938443
U3		40109			931054
U4		4042			938443
U5		40109			929328
U6		78L12			938455
U7		324			925944
U8		757			938442
U9		4013			933644
U10		CA3046			922907
U11		4066			930148
U12		4066			930148
U13		4042			938443
U14		324			925944
U15		4042			938443
U16		40109			931054
U17		324			925944
U18		MC1357P			938456
U19		4053			938457
U20		MC1496P			938427

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U21		AD7524			938458
U22		1458			938459
U23		4042			938443
U24		339			929149
U25		CD22100			938460
U26		LM377N			938753
U27		7812			938445
U28		1458			938459
U29		1458			938459
U30		Not Fitted			
U31		Not Fitted			
Transformers					
T1					AT81401
Inductors					
L1		RF Coil			AT81400
L2		RF Coil			AT81400
L3		RF Coil			AT81408
L4	10μH	Choke		10	921209
Connectors					
J1		Plug, Coaxial RF			938429
J2		Plug, 40-way			938447
J3		Plug, Coaxial RF			938429
J4		Plug, Coaxial RF			938429
J5		Plug, Coaxial RF			938429
J6		Plug, Coaxial RF			938429
J7		Plug, 26-way			938449
J8		Plug, 34-way			938448

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Filters		Sideband:			
		3KHz USB			BD 81059
		3KHz LSB			BD 81058
		2.7KHz USB Marine			BD 81052
		Symmetrical:			
		0.1KHz			BD 81023
		0.3KHz			BD 81053
		1.0KHz			BD 81054
		1.6KHz			BD 81015
		2.0KHz			BD 81016
		3.2KHz			BD 81055
		6.0KHz			BD 81056
		16KHz			BD 81057

MICROCOMPUTER BOARD A6A2 (ST 08203)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	1k	Metal Oxide	¼	2	913489
R2	39k	Metal Oxide	¼	2	900993
R3	10k	Metal Oxide	¼	2	914042
R4	47k	Metal Oxide	¼	2	913496
R5	120k	Metal Oxide	¼	2	915373
R6	82k	Metal Oxide	¼	2	915189
R7	1k	Metal Oxide	¼	2	913489
R8	10k	Metal Oxide	¼	2	914042
R9	270	Metal Oxide	¼	2	910391
R10	33k	Metal Oxide	¼	2	913495
R11	47	Metal Oxide	¼	2	917063
R12	47k	Metal Oxide	¼	2	913496
R13	10	Metal Oxide	¼	2	909145
R14	100k	Metal Oxide	¼	2	915190
R15	33k	Metal Oxide	¼	2	913495
R16	10k	Metal Oxide		2	914042
Capacitors			V		
C1	15p	Ceramic		±5	938522
C2	15p	Ceramic		±5	938522
C3	0.1	Ceramic	50	±20	938406
C4	0.1	Ceramic	50	±20	938406
C5	0.1	Ceramic	50	±20	938406
C6	0.1	Ceramic	50	±20	938406
C7	0.1	Ceramic	50	±20	938406
C8	0.1	Ceramic	50	±20	938406
C9	0.1	Ceramic	50	±20	938406
C10	0.1	Ceramic	50	±20	938406
C11		Not Used			
C12		Not Used			
C13	6.8	Tantalum	35	±20	938030
C14	6.8	Tantalum	35	±20	938030
C15	0.001	Ceramic		±20	938408
C16	4.7	Tantalum	10	±20	938033

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Diodes					
CR1		Zener IN752			921717
CR2		IN916 Silicon			913480
CR3		IN270 Germanium			938523
CR4		IN916 Silicon			913480
CR5		IN916 Silicon			913480
CR6		IN916 Silicon			913480
Transistors					
Q1		Silicon (2N3906)			914047
Q2		Silicon (2N3904)			914046
Q3		Silicon (2N3904)			914046
Q4		Silicon (2N3906)			914047
Q5		Silicon (2N3904)			914046
Q6		Silicon (T15-74)			938450
Integrated Circuits					
U1		mk. 3850 CPU			938526
U2		mk 3853 Static memory device			938527
U3		74LS139			938528
U4		74LS245			938529
U5		2716 2kx8 EPROM)			
		) programmed Devices			
U6		2716 2kx8 EPROM)			
U7		2716 2kx8 EPROM)			
U8		445L 1kx4 Bit RAM			938038
U9		445L 1kx4 Bit RAM			938038
U10		Not used			
U11		74LS10			938530
U12		74LS02			938531
U13		74LS04			938532
U14		74LS374			938533
Crystals					
Y1	2MHz	Crystal			A07621

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Connectors					
XU1		IC Socket 40 Pin DIP			938646
XU2		IC Socket 40 Pin DIP			938646
XU3		Not Used			
XU4		Not Used			
XU5		IC Socket 24 Pin DIP			938534
XU6		IC Socket 24 Pin DIP			938534
XU7		IC Socket 24 Pin DIP			938534
J1		Plug, 34-way			938524
J2		Socket, 50-way			938525
Miscellaneous					
BT1	2.4V DC	Battery Ni-Cad			938521

FIRST LO SYNTHESIZER BOARD A7 (ST80788)

Earlier Versions (ST08545) see Appendix 4

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors					
R1	47k	Metal Oxide		2	913496
R2	10	Metal Oxide		2	920736
R3	10k	Metal Oxide		2	914042
R4	150	Metal Oxide		2	910389
R5	200	Variable	0.5	20	938618
R6	~~100~~ 47Ω	Metal Oxide		2	~~910388~~ 917063
R7	68	Metal Oxide		2	916476
R8	68	Metal Oxide		2	916476
R9	22	Metal Oxide		2	920743
R10	1.5k	Metal Oxide		2	911166
R11	680	Metal Oxide		2	910113
R12	10	Metal Oxide		2	920736
R13	390	Metal Oxide		2	916331
R14	56	Metal Oxide		2	917055
R15	820	Metal Oxide		2	917065
R16	500	Variable	0.5	20	938426
R17	2.2k	Metal Oxide		2	917652
R18	47	Metal Oxide		2	917063
R19	1.0	Composition		5	938617
R20		Not Used			
R21	82	Metal Oxide		2	917057
R22	10	Metal Oxide		2	920736
R23	220	Metal Oxide		2	910390
R24	100	Metal Oxide		2	910388
R25	1k	Metal Oxide		2	913489
R26	100	Metal Oxide		2	910388
R27	100	Metal Oxide		2	910388
R28	1k	Metal Oxide		2	913489
R29	1k	Metal Oxide		2	913489
R30	820	Metal Oxide		2	917065

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R31	220	Metal Oxide		2	910390
R32	220	Metal Oxide		2	910390
R33	820	Metal Oxide		2	917065
R34	470	Metal Oxide		2	920758
R35	470	Metal Oxide		2	920758
R36	220	Metal Oxide		2	910390
R37	820	Metal Oxide		2	917065
R38	470	Metal Oxide		2	920758
R39	1k	Metal Oxide		2	913489
R40	470	Metal Oxide		2	920758
R41	470	Metal Oxide		2	920758
R42	470	Metal Oxide		2	920758
R43	~~470~~ 820Ω	Metal Oxide		2	~~920758~~ 917065
R44	~~470~~ 330Ω	Metal Oxide		2	~~920758~~ 915690
R45	~~56k~~ 39K	Metal Oxide		2	~~909052~~ 900993
R46	470	Metal Oxide		2	920758
R47	820	Metal Oxide		2	917065
R48	470	Metal Oxide		2	920758
R49	470	Metal Oxide		2	920758
R50	10k	Metal Oxide		2	914042
R51	~~4.7k~~ 12K	Metal Oxide		2	~~913490~~ 917952
R52	~~2.2k~~ 2K7	Metal Oxide		2	917652 916568
R53	~~3.3k~~ 4K7	Metal Oxide		2	~~910111~~ 913490
R54	~~3.3k~~ 4 K7	Metal Oxide		2	~~910111~~ 913490
R55	470	Metal Oxide		2	920758
R56	~~2.2k~~ 1K8	Metal Oxide		2	~~917652~~ 911148
R57	~~3.9k~~ 3K3	Metal Oxide		2	~~915074~~ 910111
R58	470	Metal Oxide		2	920758
R59	3.3k	Metal Oxide		2	910111
R60	22	Metal Oxide		2	920743
R61	1k	Metal Oxide		2	913489
R62	10k	Metal Oxide		2	914042
R63	1k	Metal Oxide		2	913489
R64	39k	Metal Oxide		2	900993
R65	15k	Metal Oxide		2	920645

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R66	8.2k	Metal Oxide		2	918202
R67	18k	Metal Oxide		2	900994
R68	1k	Metal Oxide		2	913489
R69	3.3k	Metal Oxide		2	910111
R70	1k	Metal Oxide		2	913489
R71	82	Metal Oxide		2	917057
R72	10	Metal Oxide		2	920736
R73	10k	Metal Oxide		2	914042
R74	15k	Metal Oxide		2	920645
R75	15k	Metal Oxide		2	920645
R76	15k	Metal Oxide		2	920645
R77	100k	Metal Oxide		2	915190
R78	2.7k	Metal Oxide		2	916548
R79	12k	Metal Oxide		2	917952
R80	150k	Metal Oxide		2	917954
R81	10k	Metal Oxide		2	914042
R82	10k	Metal Oxide		2	914042
R83	10k	Metal Oxide		2	914042
R84	3.3k	Metal Oxide		2	910111
R85	100	Metal Oxide		2	910388
R86	470	Metal Oxide		2	920758
R87	47k	Metal Oxide		2	913496
R88	120k	Metal Oxide		2	915373
R89	47k	Metal Oxide		2	913496
R90	1k	Metal Oxide		2	913489
R91	150	Metal Oxide		2	910389
R92	10	Metal Oxide		2	920736
R93	680	Metal Oxide		2	910113
R94	10	Metal Oxide		2	920736
R95	1k	Metal Oxide		2	913489
R96		Not used			
R97		Not used			
R98	1k	Metal Oxide		2	913489
R99	680	Metal Oxide		2	916476
R100	100	Metal Oxide		2	910388
R101	10	Metal Oxide		2	920736

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C1	6.8	Tantalum	35	20	938030
C2	6.8	Tantalum	35	20	938030
C3	6.8	Tantalum	35	20	938030
C4	6.8	Tantalum	35	20	938030
C5	.01	Ceramic	50	20	938053
C6	6.8	Tantalum	35	20	938030
C7	.01	Ceramic	50	20	938053
C8	6.8	Tantalum	35	20	938030
C9	.01	Ceramic	50	20	938053
C10		Not used			
C11	.01	Ceramic	50	20	938053
C12	6.8	Tantalum	35	20	938030
C13	.01	Ceramic	50	20	938053
C14	.01	Ceramic	50	20	938053
C15	.01	Ceramic	50	20	938053
C16	.01	Ceramic	50	20	938053
C17	.01	Ceramic	50	20	938053
C18	.01	Ceramic	50	20	938053
C19	.01	Ceramic	50	20	938053
C20	.01	Ceramic	50	20	938053
C21	.01	Ceramic	50	20	938053
C22	.01	Ceramic	50	20	938053
C23	.01	Ceramic	50	20	938053
C24	.01	Ceramic	50	20	938053
C25	.01	Ceramic	50	20	938053
C26	.01	Ceramic	50	20	938053
C27	.01	Ceramic	50	20	938053
C28	.01	Ceramic	50	20	938053
C29	.01	Ceramic	50	20	938053
C30	.01	Ceramic	50	20	938053
C31	.01	Ceramic	50	20	938053
C32	.01	Ceramic	50	20	938053
C33	.01	Ceramic	50	20	938053
C34	.01	Ceramic	50	20	938053
C35	.01	Ceramic	50	20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C36	6.8	Tantalum	35	20	938030
C37	15	Tantalum	20	20	922516
C38	6.8	Tantalum	35	20	938030
C39	.01	Ceramic	50	20	938053
C40	.001	Ceramic	50	20	938408
C41	33	Tantalum	25	10	938606
C42	0.1	Ceramic	50	20	938406
C43	.001	Ceramic	50	20	938408
C44	.01	Ceramic	50	20	938053
C45	6.8	Tantalum	35	20	928030
C46	6.8	Tantalum	35	20	938030
C47	.01	Ceramic	50	20	938053
C48	.01	Ceramic	50	20	938053
C49	6.8	Tantalum	35	20	938030
C50	6.8	Tantalum	35	20	938030
C51	0.1	Ceramic	50	20	938406
C52	.001	Ceramic	50	20	938408
C53	150	Tantalum	6	20	938607
C54	.001	Ceramic	50	20	938408
C55	.001	Ceramic	50	20	938408
C56	.01	Ceramic	50	20	938053
C57	10p	Ceramic	500	5	917746
C58	.01	Ceramic	50	20	938053
C59	0.1	Ceramic	50	20	938406
C60	6.8	Tantalum	35	20	938030
C61	6.8	Tantalum	35	20	938030
C62	0.1	Ceramic	50	20	938406
C63	0.1	Ceramic	50	20	938406
C64	0.1	Ceramic	50	20	938406
C65	0.1	Ceramic	50	20	938406
C66	0.1	Ceramic	50	20	938406
C67	0.1	Ceramic	50	20	938406
C68	0.1	Ceramic	50	20	938406
C69	0.1	Ceramic	50	20	938406
C70	0.1	Ceramic	50	20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C71	0.1	Ceramic	50	20	938406
C72	0.1	Ceramic	50	20	938406
C73	0.1	Ceramic	50	20	938406
C74	0.1	Ceramic	50	20	938406
C75	0.1	Ceramic	50	20	938406
C76	0.1	Ceramic	50	20	938406
C77	0.1	Ceramic	50	20	938406
C78	100p	Mica	350	5	938510
C79	6.8	Tantalum	35	20	938030
C80	27p	Mica	350	1p	902220
C81	.001	Polyester	400	10	938671
C82	.047	Polycarbonate	100	10	931129
C83	6.8	Tantalum	35	20	938030
C84	6.8	Tantalum	35	20	938030
C85	.001	Ceramic	50	20	938408
C86	1.0	Tantalum	35	10	938032
C87	1.0	Tantalum	35	10	938032
C88	15	Tantalum	20	20	910060
C89	.047	Ceramic	50	20	938511
C90	2200p	Ceramic	100	20	937903
C91	4700p	Mica	350	5	939350
C92	2200p	Mica	350	2	902197
C93	0.1	Ceramic	50	20	938406
C94	6.8	Tantalum	35	20	938030
C95	.001	Ceramic	50	20	938408
C96	0.1	Ceramic	50	20	938406
C97	1.0	Polycarbonate	100	20	938098
C98	3.3	Polycarbonate	63	10	938673
C99	.068	Polycarbonate	100	10	938672
C100	4.7p	Ceramic	100	0.5p	938794
C101	10p	Mica	500	5	921270
C102		Not used			
C103	.01	Ceramic	50	20	938053
C104	0.1	Ceramic	50	20	938406
C105	.001	Ceramic	50	20	938408

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Diodes					
CR1		IN 916			913480
CR2		IN 916			913480
CR3		Varactor KV 2201			938614
CR4		Varactor KV 2201			938614
CR5		IN 916			913480
CR6		IN 916			913480
CR7		IN 916			913480
CR8		IN 916			913480
CR9		IN 916			913480
CR10		IN 916			913480
CR11		IN 916			913480
CR12		IN 916			913480
CR13		IN 916			913480
CR14		IN 916			913480
CR15		IN 916			913480
CR16		IN 916			913480
CR17		Not used			
CR18		Zener 9.1V, 400mW, IN757A			938674
CR19		IN 916			913480
CR20		IN 916			913480
CR21		IN 916			913480
CR22		IN 916			913480
CR23		HP 5082-2811 SCHOTTKY DIODE			919460
Transistors					
Q1		FET BFW11			921213
Q2		NPN RF 2N3866			917219
Q3		NPN RF 2N3866			917219
Q4		NPN Silicon 2N4921			938616
Q5		NPN Silicon 2N2369			906842
Q6		PNP Plastic 2N4126			912678
Q7		PNP Plastic 2N4126			912678
Q8		PNP Plastic 2N4126			912678
Q9		NPN Plastic 2N4124			915617
Q10		NPN Plastic 2N4124			915617

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Q11		PNP Plastic 2N4126			912678
Q12		NPN Silicon 2N2369			906842
Q13		NPN Silicon 2N2369			906842
Q14		NPN Silicon 2N2369			906842
Integrated Circuits					
U1		4001			938561
U2		4503			935215
U3		74LS174			939351
U4		74LS02			938531
U5		74LS174			939351
U6		74LS174			939351
U7		* 4070			938837
U8		4094			934550
U9		4094			934550
U10		4094			934550
U11		4094			934550
U12		4094			934550
U13		4094			934550
U14		4094			934550
U15		82583			938622
U16		10k resistor network			938625
U17		4008			938620
U18		* 40174			938838
U19		74LS74			939352
U20		4006			938628
U21		4006			938628
U22		40108			938629
U23		DAC 20			938631
U24		UA723			925040
U25		Not used			
U26		10231			938630
U27		11C90			938600
U28		10231			938630
U29		74LS169			938627
U30		74LS168			938626

* Use RCA, Motorola or National only.

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
U31		74LS168			938626
U32		10211			938633
U33		1458			938632
U34		LM339			929149
U35		AD518			938634
U36		DG201			934880
U37		1458			938632
U38		Not used			
U39		7812			938445
U40		3140E			932204
Transformers					
T1		RF wideband			AT81411
Inductors					
L1	6.8µH	Choke			919469
L2	6.8µH	Choke			919469
L3	6.8µH	Choke			919469
L4	6.8µH	Choke			919469
L5		Coil assembly			AT81189
L6	15µH	Choke		10	915850
Connectors					
J1		Plug 20-way			938675
J2		Plug, Coaxial 50 ohms			938429
J3		Plug, Coaxial 50 ohms			938429
J4		Plug, Coaxial 50 ohms			938429

2ND LO/BFO SYNTHESIZER - BOARD A8 (ST 08283/2)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	20k	Variable		10	938593
R2	33	Metal Oxide	¼	2	917060
R3	1.8k	Metal Oxide	¼	2	911148
R4	6.8k	Metal Oxide	¼	2	910112
R5	2.2k	Metal Oxide	¼	2	916546
R6	680	Metal Oxide	¼	2	910113
R7	4.7k	Metal Oxide	¼	2	913490
R8	47	Metal Oxide	¼	2	917063
R9	33	Metal Oxide	¼	2	917060
R10	1k	Metal Oxide	¼	2	913489
R11	330	Metal Oxide	¼	2	915690
R12	10	Metal Oxide	¼	2	920736
R13	1k	Metal Oxide	¼	2	913489
R14		Not Used			
R15		Not Used			
R16		Not Used			
R17		Not Used			
R18	3.3k	Metal Oxide	¼	2	910111
R19	1.8k	Metal Oxide	¼	2	911148
R20	3.3k	Metal Oxide	¼	2	910111
R21	1.8k	Metal Oxide	¼	2	911148
R22	820	Metal Oxide	¼	2	917065
R23	1k	Metal Oxide	¼	2	913489
R24	4.7k	Metal Oxide	¼	2	913490
R25	4.7k	Metal Oxide	¼	2	913490
R26	10	Metal Oxide	¼	2	920736
R27	330	Metal Oxide	¼	2	915690
R28	10k	Metal Oxide	¼	2	914042
R29	10k	Metal Oxide	¼	2	914042
R30		Not Used			

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R31		Not Used			
R32	47	Metal Oxide	¼	2	917063
R33	680	Metal Oxide	¼	2	910113
R34	680	Metal Oxide	¼	2	910113
R35	820	Metal Oxide	¼	2	917065
R36	10k	Metal Oxide	¼	2	914042
R37	3.3k	Metal Oxide	¼	2	910111
R38	680	Metal Oxide	¼	2	910113
R39	2.2k	Metal Oxide	¼	2	916546
R40	470	Metal Oxide	¼	2	920758
R41	3.3k	Metal Oxide	¼	2	910111
R42		Not used			
R43	1k	Metal Oxide	¼	2	913489
R44	1k	Metal Oxide	¼	2	913489
R45	1k	Metal Oxide	¼	2	913489
R46	56	Metal Oxide	¼	2	917055
R47	10k	Metal Oxide	¼	2	914042
R48	1k	Metal Oxide	¼	2	913489
R49	1k	Metal Oxide	¼	2	913489
R50	470	Metal Oxide	¼	2	920758
R51	470	Metal Oxide	¼	2	920758
R52	220	Metal Oxide	¼	2	910390
R53	100	Metal Oxide	¼	2	910388
R54	1k	Metal Oxide	¼	2	913489
R55	470	Metal Oxide	¼	2	920758
R56	47	Metal Oxide	¼	2	917063
R57	1k	Metal Oxide	¼	2	913489
R58	1k	Metal Oxide	¼	2	913489
R59	680	Metal Oxide	¼	2	910113
R60	2.2k	Metal Oxide	¼	2	916546
R61	10k	Metal Oxide	¼	2	914042
R62	3.3k	Metal Oxide	¼	2	910111
R63	680	Metal Oxide	¼	2	910113
R64	2.2k	Metal Oxide	¼	2	916546
R65	18k	Metal Oxide	¼	2	900994

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R66	560k	Metal Oxide	¼	2	920831
R67	680	Metal Oxide	¼	2	910113
R68	560k	Metal Oxide	¼	2	920831
R69	330	Metal Oxide	¼	2	915690
R70	330	Metal Oxide	¼	2	915690
R71		Not Used			
R72	4.7k	Metal Oxide	¼	2	913490
R73	10k	Metal Oxide	¼	2	914042
R74	1k	Metal Oxide	¼	2	913489
R75	1.8k	Metal Oxide	¼	2	911148
R76	820	Metal Oxide	¼	2	917065
R77	820	Metal Oxide	¼	2	917065
R78	10k	Metal Oxide	¼	2	914042
R79	3.3k	Metal Oxide	¼	2	910111
R80	2.2k	Metal Oxide	¼	2	916546
R81	4.7k	Metal Oxide	¼	2	913490
R82	3.3k	Metal Oxide	¼	2	910111
R83	47	Metal Oxide	¼	2	917063
R84	1k	Metal Oxide	¼	2	913489
Capacitors			V		
C1	6.8	Tantalum	35	±20	938030
C2	100p	Silver Mica	500	±5	938510
C3	0.1	Ceramic	50	±20	938406
C4	0.1	Ceramic	50	±20	938406
C5	0.01	Ceramic	50	±20	938053
C6	0.047	Ceramic	50	±20	938511
C7	0.047	Ceramic	50	±20	938511
C8	0.01	Ceramic	50	±20	938053
C9	0.1	Ceramic	50	±20	938406
C10	0.001	Ceramic	50	±20	938408
C11	0.1	Ceramic	50	±20	938406
C12	0.1	Ceramic	50	±20	938406
C13	0.1	Ceramic	50	±20	938406
C14	0.01	Ceramic	50	±20	938053
C15	0.1	Ceramic	50	±20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C16	0.1	Ceramic	50	±20	938406
C17	0.1	Ceramic	50	±20	938406
C18	0.1	Ceramic	50	±20	938406
C19	0.1	Ceramic	50	±20	938406
C20	12p	Silver Mica	350	±1p	902139
C21	0.1	Ceramic	50	±20	938406
C22	0.1	Ceramic	50	±20	938406
C23	6.8	Tantalum	35	±20	938030
C24	0.1	Ceramic	50	±20	938406
C25	3.3	Tantalum	15	±10	938692
C26	0.1	Polycarbonate	100	±20	938585
C27	0.1	Ceramic	50	±20	938406
C28		Not used			938053
C29	39p	Silver Mica	350	±1p	902224
C30	0.1	Ceramic	50	±20	938406
C31	39p	Silver Mica	350	±1p	902224
C32	0.01	Ceramic	50	±20	938053
C33	68p	Silver Mica	350	±1p	902230
C34	100p	Silver Mica	500	±5	938510
C35	100p	Silver Mica	500	±5	938510
C36	0.001	Ceramic	50	±20	938408
C37	100p	Silver Mica	500	±5	938510
C38	5p	Silver Mica	500	±½p	938586
C39	0.1	Ceramic	50	±20	938406
C40	0.001	Ceramic	50	±20	938408
C41	68p	Silver Mica	350	±1p	902230
C42		Not used			
C43	0.1	Ceramic	50	±20	938406
C44	0.1	Ceramic	50	±20	938406
C45	0.1	Ceramic	50	±20	938406
C46	100p	Silver Mica	500	±5	938510
C47	0.1	Ceramic	50	±20	938406
C48	0.1	Ceramic	50	±20	938406
C49	6.8	Tantalum	35	±20	938030
C50	0.47	Polycarbonate	100	±20	938587

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C51	0.1	Polycarbonate	100	±20	938585
C52	0.01	Ceramic	50	±20	938053
C53	0.01	Ceramic	50	±20	938053
C54	6.8	Tantalum	35	±20	938030
C55	56p	Silver Mica	500	±5	938588
C56	100p	Silver Mica	500	±5	938510
C57	100p	Silver Mica	500	±5	938510
C58	0.01	Ceramic	50	±20	938053
C59	0.01	Ceramic	50	±20	938053
C60	0.01	Ceramic	50	±20	938053
C61	0.01	Ceramic	50	±20	938053
C62	0.1	Ceramic	50	±20	938406
C63	820p	Silver Mica	500	±5	938589
C64	150p	Silver Mica	350	±1p	902238
C65	820p	Silver Mica	500	±5	938589
C66	0.1	Ceramic	50	±20	938406
C67	0.1	Ceramic	50	±20	938406
C68	0.1	Ceramic	50	±20	938406
C69	0.1	Ceramic	50	±20	938406
C70	0.1	Ceramic	50	±20	938406
C71	0.1	Ceramic	50	±20	938406
C72	0.01	Ceramic	50	±20	938053
C73	0.1	Ceramic	50	±20	938406
C74	0.1	Ceramic	50	±20	938406
C75	0.1	Ceramic	50	±20	938406
C76	82p	Silver Mica	350	1p	902232
C77	330p	Silver Mica	350	2	902246
C78	0.01	Ceramic	50	±20	938053
C79	6.8	Tantalum	35	±20	938030
C80	0.01	Ceramic	50	±20	938053
C81	6.8	Tantalum	35	±20	938030
C82	0.01	Ceramic	50	±20	938053
C83	39p	Silver Mica	350	±1p	902224
C84	0.01	Ceramic	50	±20	938053
C85	0.01	Ceramic	50	±20	938053

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C86	39p	Silver Mica	350	±1p	902224
C87	0.001	Ceramic	50	±20	938408
Diodes					
CR1		IN4001			915266
CR2		IN916			913480
CR3		IN916			913480
CR4		ZC707			937650
CR5		IN916			913480
CR6		KV650 (MV1650)			938591
CR7		KV650 (MV1650)			938591
Transistors					
Q1		Silicon (2N2369)			906842
Q2		Silicon (2N2369)			906842
Q3		Silicon (2N2369)			906842
Q4		Silicon (2N2369)			906842
Q5		Silicon (2N2369)			906842
Q6		Silicon (2N2369)			906842
Q7		Silicon (2N3904)			914046
Q8		Silicon (2N4126)			912679
Q9		Silicon (2N3904)			914046
Q10		Silicon (2N2369)			906842
Q11		Silicon (2N2369)			906842
Q12		Not Used			
Q13		Not Used			
Q14		Not Used			
Q15		Silicon (2N3904)			914046
Q16		Silicon (2N4126)			912679
Q17		Silicon (2N3904)			914046
Q18		Silicon (2N3823)			938592
Q19		Silicon (2N3823)			938592
Q20		Silicon (2N2369)			406842
Q21		Silicon (2N2369)			906842

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U1		UA723PC Voltage Regulator			925040
U2		74LS00			938594
U3		74LS74			939352
U4		74LS151			939355
U5		74LS151			939355
U6		74LS90			939358
U7		74LS74			939352
U8		74LS39C			938598
U9		74LS390			939353
U10		74LS74			939352
U11		74LS00			939356
U12		74LS02			938531
U13		74LS08			939357
U14		74LS160			939354
U15		74LS160			939354
U16		74LS160			939354
U17		74LS160			939354
U18		74LS160			939354
U19		11C90			938600
U20		74LS39C			938597
U21		4N28			938601
U22		10115 ECL			938602
Inductors					
L1	100µ	Choke		10	919471
L2	1µ	Choke		10	915849
L3	33µ	Choke		10	919465
L4		Coil Assembly			AT81409
L5	33µ	Choke		10	919465
L6	220µ	Choke		10	918986
L7	5.6µ	Choke		10	922275
L8	5.6µ	Choke		10	922275
L9		Coil Assembly			AT81397
L10		Coil Assembly			AT81397

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Crystals					
Y1		Oscillator TCXO (optional)			C07978
Y2		20000.00 KHz			AD80547
Connectors					
J1		Plug, Coaxial RF			938429
J2		Plug, Coaxial RF			938429
J3		Plug, Coaxial RF			938429
J4		Plug, Coaxial RF			938429
J5		Plug, 26-way			938569
J6		Plug, Int/Ext Select			B06846-2
J7		Plug, Coaxial RF			938429
J8		Plug, Coaxial RF			938429

FRONT PANEL SWITCH AND DISPLAY BOARD A9A1 (ST08198)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R2	15k	Metal Oxide	$\frac{1}{4}$	2	920645
R3	15k	Metal Oxide	$\frac{1}{4}$	2	920645
Capacitors			V		
C1	6.8	Tantalum	35	±20	938030
C2	0.1	Ceramic	50	±20	938406
C3	6.8	Tantalum	35	±20	938030
C4	6.8	Tantalum	35	±20	938030
Integrated Circuits					
U1		LCD Mode			C08180
U2		LCD Frequency			C08181
U3		4054B			938464
U4		4054B			938464
U5		4056B			938465
U6		4056B			938465
U7		4054B			938464
U8		4054B			938464
U9		4054B			938464
U10		4056B			938465
U11		4056B			938465
U12		4056B			938465
U13		4056B			938465
U14		4056B			938465
U15		4056B			938465
U16		4056B			938465
U17		4056B			938465
U18		4056B			938465
U19		4056B			938465
U20		4056B			938465

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U21		4054B			938464
U22		4054B			938464
U23		4054B			938464
U24		4056B			938465
U25		4056B			938465
U26		4054B			938464
U27		4514B			938466
U28		4054B			938464
U29		4047			938463
Switches					
SW1		RSM83-1A			938467
SW2		RSM83-1A			938467
SW3		RSM83-1A			938467
SW4		RSM83-1A			938467
SW5		RSM83-1A			938467
SW6		RSM83-1A			938467
SW7		RSM83-1A			938467
SW8		RSM83-1A			938467
SW9		RSM83-1A			938467
SW10		RSM83-1A			938467
SW11		RSM83-1A			938467
SW12		RSM83-1A			938467
SW13		RSM83-1A			938467
SW14		RSM83-1A			938467
SW15		RSM83-1A			938467
SW16		RSM83-1A			938467
SW17		RSM83-1A			938467
SW18		RSM83-1A			938467
SW19		RSM83-1A			938467
SW20		RSM83-1A			938467

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Switches					
SW21		RSM83-1A			938467
SW22		RSM83-1A			938467
SW23		RSM83-1A			938467
SW24		RSM83-1A			938467
SW25		RSM83-1A			938467

Switch Keytops (serial numbers 7400 onwards)

Switchtop	Part No.	Switchtop	Part No.	Switchtop	Part No.
ENTER	BD81103/36	STORE	BD81103/58	6/MAN	BD81103/67
AM	BD81103/45	ISB	BD81103/59	7/SHORT	BD81103/68
FM	BD81103/46	LSB	BD81103/60	8/MED	BD81103/69
CW	BD81103/47	USB	BD81103/61	9/LONG	BD81103/70
CHAN	BD81103/53	1/BW1	BD81103/62	0/AUX	BD81103/71
RCL	BD81103/54	2/BW2	BD81103/63	FREQ.	BD81103/79
TUNE	BD81103/55	3/BW3	BD81103/64	CHAN.SCAN	BD81103/80
BFO	BD81103/56	4/BW4	BD81103/65		
REM	BD81103/57	5/BW5	BD81103/66		

Connectors		
P1	Cable Assembly	BE08290
	Comprising:	
	PCB Connector, 50-way	927270
	Ribbon cable, 50-way	927301
	Socket, 50-way	934413
	Clamp, strain relief	934414

FRONT PANEL MEMORY BOARD A9A2 (ST08234)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	4.7k	Metal Oxide	$\frac{1}{4}$	±2	913490
R2	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R3	270	Metal Oxide	$\frac{1}{4}$	±2	910391
R4	47k	Metal Oxide	$\frac{1}{4}$	±2	913496
R5	47k	Metal Oxide	$\frac{1}{4}$	±2	913496
R6	68k	Metal Oxide	$\frac{1}{4}$	±2	916478
R7	68k	Metal Oxide	$\frac{1}{4}$	±2	916478
R8	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R9	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R10	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R11	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R12	1M	Metal Oxide	$\frac{1}{4}$	±5	929119
R13	1M	Metal Oxide	$\frac{1}{4}$	5	929119
R14	33k	Metal Oxide	$\frac{1}{4}$	±2	913495
R15	33k	Metal Oxide	$\frac{1}{4}$	±2	913495
R16	100k	Metal Oxide	$\frac{1}{4}$	±2	915190
R17	12k	Metal Oxide	$\frac{1}{4}$	±2	917952
R18	12k	Metal Oxide	$\frac{1}{4}$	±2	917952
R19	100k	Metal Oxide	$\frac{1}{4}$	±2	915190
R20	22k	Metal Oxide	$\frac{1}{4}$	±2	913493
R21	22k	Metal Oxide	$\frac{1}{4}$	±2	913493
R22	180	Metal Oxide	$\frac{1}{4}$	±2	915465
R23	180	Metal Oxide	$\frac{1}{4}$	±2	915465
R24	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R25	10k	Metal Oxide	$\frac{1}{4}$	±2	914042
R26	1k	Metal Oxide	$\frac{1}{4}$	±2	913489
R27	47	Metal Oxide	$\frac{1}{4}$	±2	917063

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C1	0.1	Ceramic	50	±20	938406
C2	0.1	Ceramic	50	±20	938406
C3	0.1	Ceramic	50	±20	938406
C4		Not Used			
C5	0.1	Ceramic	50	±20	938406
C6	330	Electrolytic	10	±20	938555
C7	100	Electrolytic	40		938554
C8	100	Electrolytic	40		938554
C9	0.1	Ceramic	50	±20	938406
C10	15p	Ceramic		5	938522
C11	15p	Ceramic		5	938522
C12	15	Tantalum	20	20	938034
C13	1	Tantalum	35	20	938405
C14	100p	Ceramic		10	938556
C15	100p	Ceramic		10	938556
Diodes					
CR1		IN916			913480
CR2		IN4001			915266
CR3		IN916			913480
CR4		IN916			913480
CR5		IN725A Zener,	30V	5%	937983
CR6		IN916			913480
CR7		IN916			913480
Transistors					
Q1		Silicon (2N2906A)			920963
Q2		Silicon (2N2906A)			920963
Q3		Silicon (2N3906)			914047
Q4		Silicon (2N2369)			906842

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U1	10k	Resistor Network 10 Pin			938558
U2	10k	Resistor Network 10 Pin			938558
U3		4066			930148
U4		4013			933644
U5		4081B			938559
U6		4011			938560
U7		4001			938561
U8		4514B			938466
U9		MC14528BCL			938562
U10		4051			929383
U11		μA79M12			938563
U12		4516			938564
U13		ER3400			934622
U14		ER3400			934622
U15		4503			935215
U16		4503			935215
U17		4503			935215
U18		4503			935215
U19		4042			938443
U20		4042			938443
U21		40107			928188
U22	10k	Resistor Network			938565
U23	10k	Resistor Network			938565
U24		4076B			938566
U25		4076B			938566
U26		4076B			938566
U27		4076B			938566
U28		LM339			929149
U29		OPB706A			938567
U30		OPB706A			938567
Connectors					
J1		Plug 26-way			938569
J2		Plug 50-way			938570

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Switches					
S1		DIP, SPST.			938557
Cable and Connector Assemblies					
W1		34-way comprising:			B08227
		PCB Connector, 34-way			938571
		Ribbon Cable, 34-way			927430
		Socket, 34-way			934213
		Clamp, Strain Relief			934124
W2		26-way comprising:			B08368
		PCB Connector, 26-way			938572
		Ribbon Cable, 26-way			927429
		Socket, 26-way			935019
		Clamp, Strain Relief			935020
W3		Not used			
W4		Not used			
W5		20-way comprising:			B08714
		PCB connector, 20-way			938062
		Ribbon cable, 20-way			927303
		Socket, 20-way			935017
		Clamp, Strain Relief			935018
W6		40-way comprising:			B08363
		PCB connector, 40-way			938574
		Ribbon Cable, 40-way			927302
		Socket, 40-way			935021
		Clamp, Strain Relief			935022

AC POWER SUPPLY MODULE A10 (ST80784)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	33	Metal Oxide	$\frac{1}{4}$	2	917060
Capacitors			V		
C1	12,500	Electrolytic	25	-10+75	938486
C2	1	Tantalum	35	+20	938487
C3	1	Tantalum	35	+20	938487
C4	5200	Electrolytic	40	-10+75	938488
C5	1	Tantalum	35	+20	938487
C6	1	Tantalum	35	+20	938487
C7	5200	Electrolytic	40	-10+75	938488
C8	1	Tantalum	35	+20	938487
C9	6.8	Tantalum	35	+20	938490
C10	1200	Electrolytic	50	-10+75	938489
C11		Not used			
C12		Not used			
C13	1	Tantalum	35	+20	938487
C14	1	Tantalum	35	+20	938487
C15	10n	Disc Ceramic	250	+40-20	916187
Diodes					
CR1		VH148			938491
CR2		VS148			938492
CR3		VS148			938492
VR1		Zener 6.8V			918491
Integrated Circuits					
U1		µA78HQ5KC +5V Regulator			938498
U2		µA7815KC +15V Regulator			932797
U3		µA7915KC -15V Regulator			938499
U4		Not used			
U5		7812K2 +12V Regulator			938501

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Transformers					
T1					CT81412
Connectors					
J1		Plug, 3-way, filtered inlet			938496
J2		Socket, 9-way			918090
Miscellaneous					
F1,F2	½A	Fuse 250V Slo Blo			938494
XF2		Fuse Holder - Clip Type			938495
		20V Regulator Board Comprising:			ST08717
R1	4.7k	Metal Oxide		2	913490
C1	.01	Ceramic	50	20	938053
C2	6.8	Tantalum	35	20	938030
C3	1	Tantalum	35	20	938405
C4	6.8	Tantalum	35	20	938030
CR1		Zener 27V, 400mW			919300
Q1		MIE 800			938641
U1		78M20			938642
		A10A1 Connector assembly comprising:			B08160
		Socket, 25-way			930819
		Connection Board			BA80777
		Mating socket for J1 (POWER IN)			930766

FREQUENCY STANDARD MODULE A11 (ST08140)

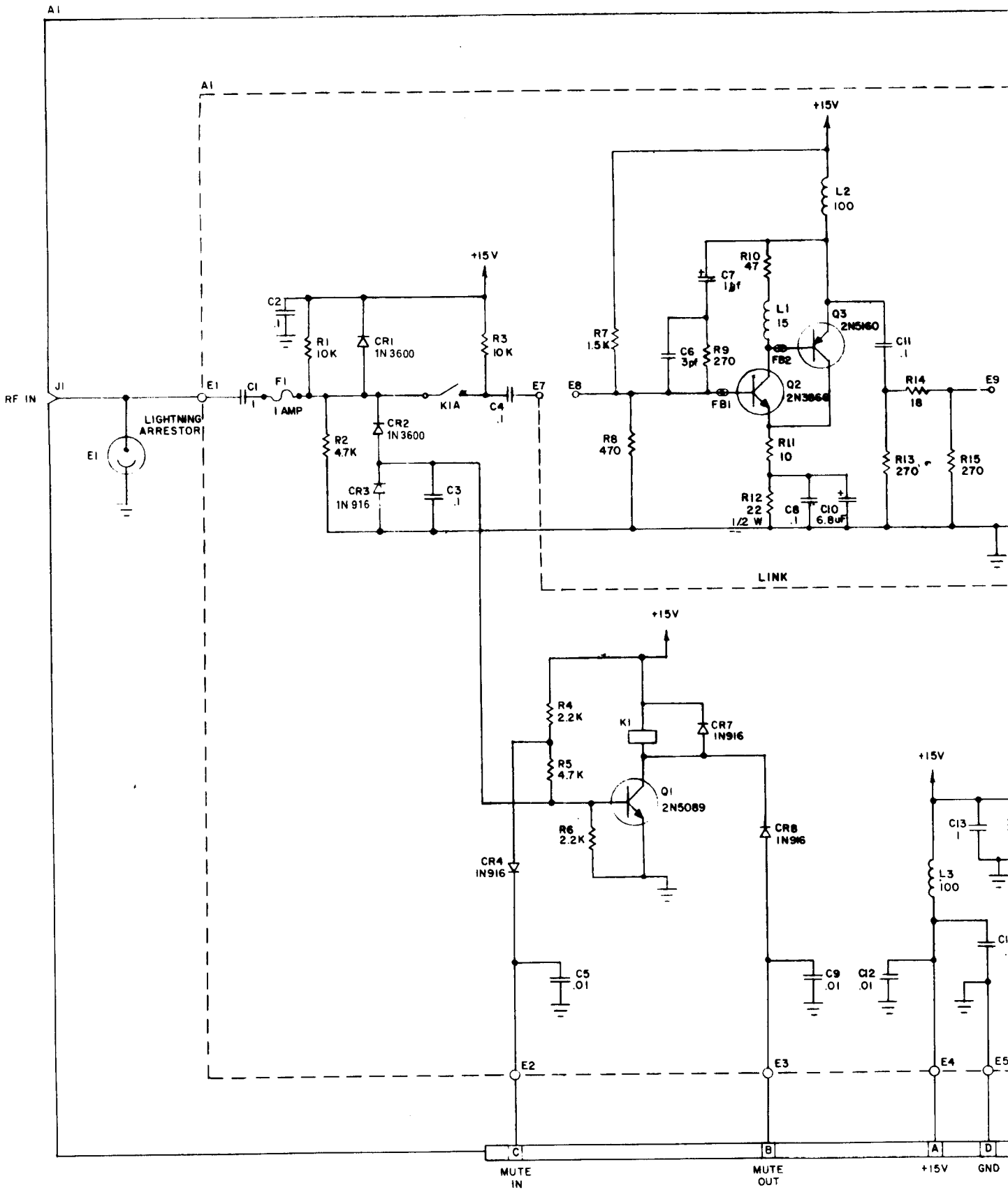
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors					
C1	0.01	Ceramic		±20	938053
C2	0.01	Ceramic		±20	938053
Inductors					
L1	15µH	Choke Fixed RF			915850
Frequency Standard					
Y1		9442/12			933706
Connectors					
J1		Plug, 3-way			938471
J2		Plug, Coaxial RF			938472
XY1		Socket 7-way			938473

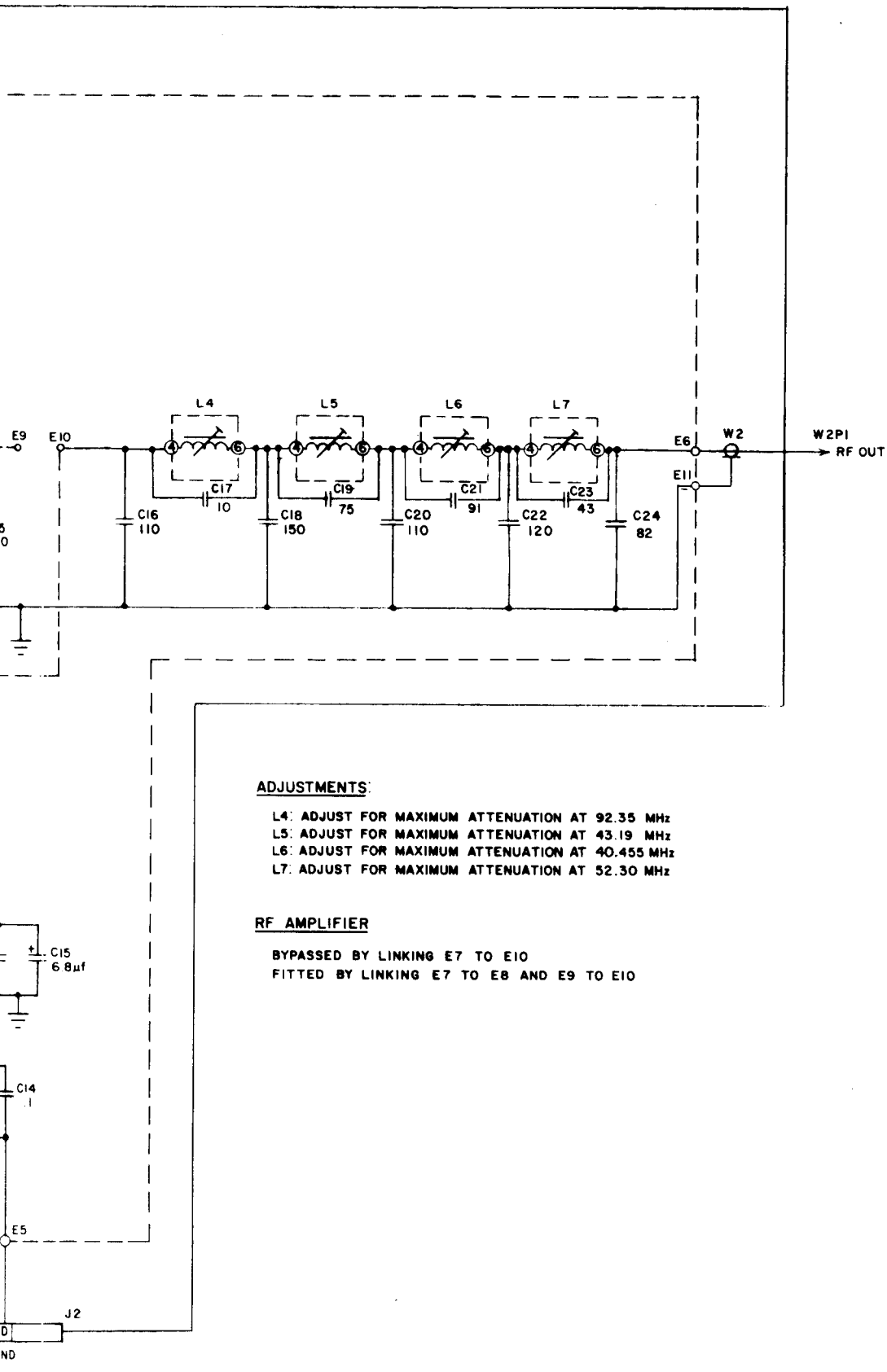
CHAPTER 8

DIAGRAMS

CONTENTS

ILLUSTRATIONS


A1
A1
RF IN
J1
E1
LIGHTNING ARRESTOR
E1
C1
.1
F1
1 AMP
R1
10K
CR1
1N3600
C2
.1
+15V
R3
10K
K1A
E7
C4
.1
R2
4.7K
CR2
1N3600
CR3
1N916
C3
.1
E8
R7
1.5K
R8
470
C6
3pf
R9
270
C7
1μf
R10
47
L1
15
FB2
FB1
Q3
2N5160
Q2
2N3866
C11
.1
R14
18
E9
R11
10
R12
22
1/2 W
C8
.1
C10
6.8uF
R13
270
R15
270
LINK
+15V
R4
2.2K
K1
CR7
1N916
R5
4.7K
Q1
2N5089
R6
2.2K
CR8
1N916
CR4
1N916
C5
.01
C9
.01
+15V
C13
1
L3
100
C12
.01
E2
E3
E4
E5
C
B
A
D
MUTE IN
MUTE OUT
+15V
GND



ADJUSTMENTS:

L4: ADJUST FOR MAXIMUM ATTENUATION AT 92.35 MHz
L5: ADJUST FOR MAXIMUM ATTENUATION AT 43.19 MHz
L6: ADJUST FOR MAXIMUM ATTENUATION AT 40.455 MHz
L7: ADJUST FOR MAXIMUM ATTENUATION AT 52.30 MHz

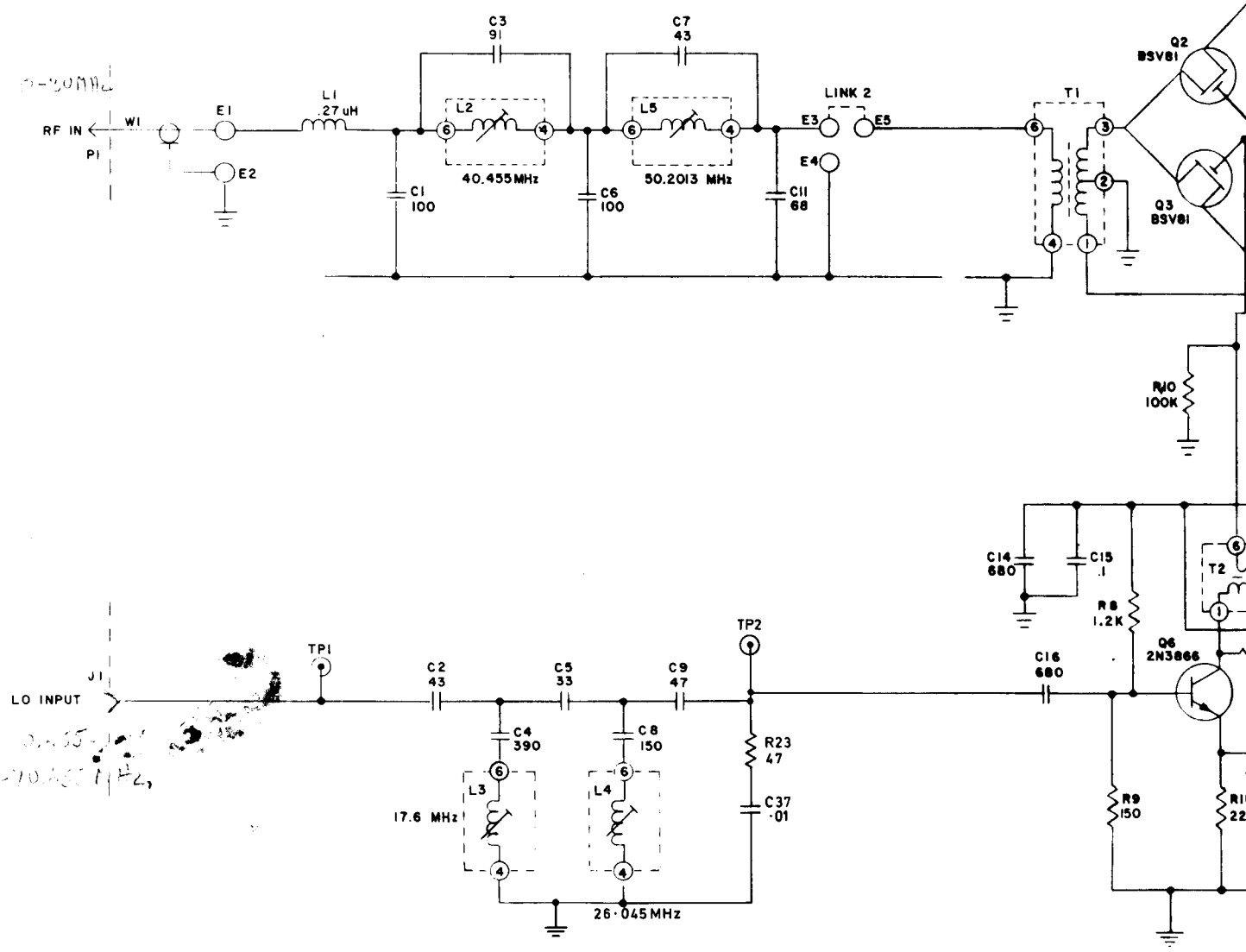
RF AMPLIFIER

BYPASSED BY LINKING E7 TO E10
FITTED BY LINKING E7 TO E8 AND E9 TO E10

UNLESS OTHERWISE NOTED

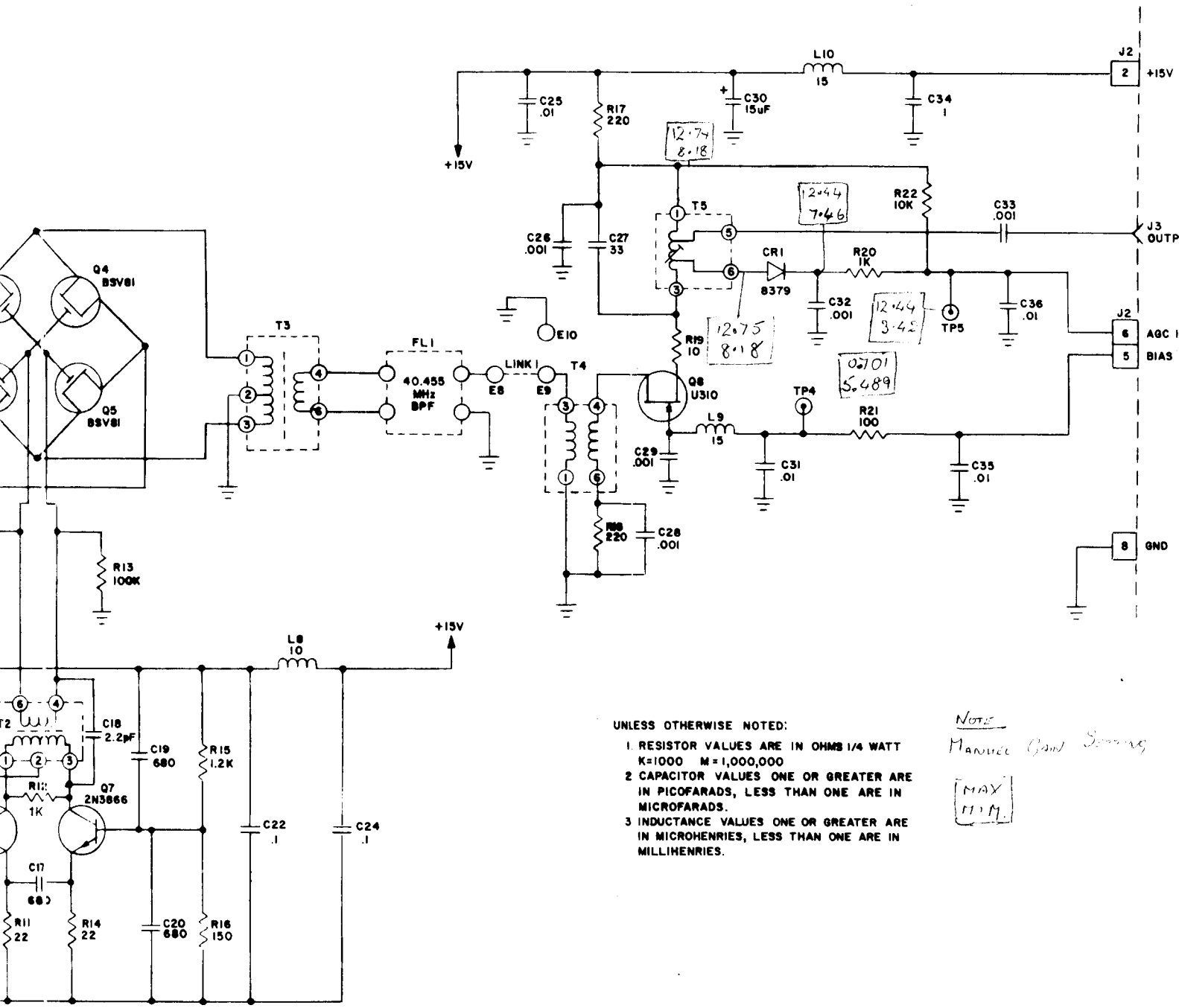
1. RESISTOR VALUES ARE IN OHMS 1/4 WAT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.

Circuit: RF Amplifier/LPF Module A1 Fig. 8.



RACAL

TH1496	D08185
3	

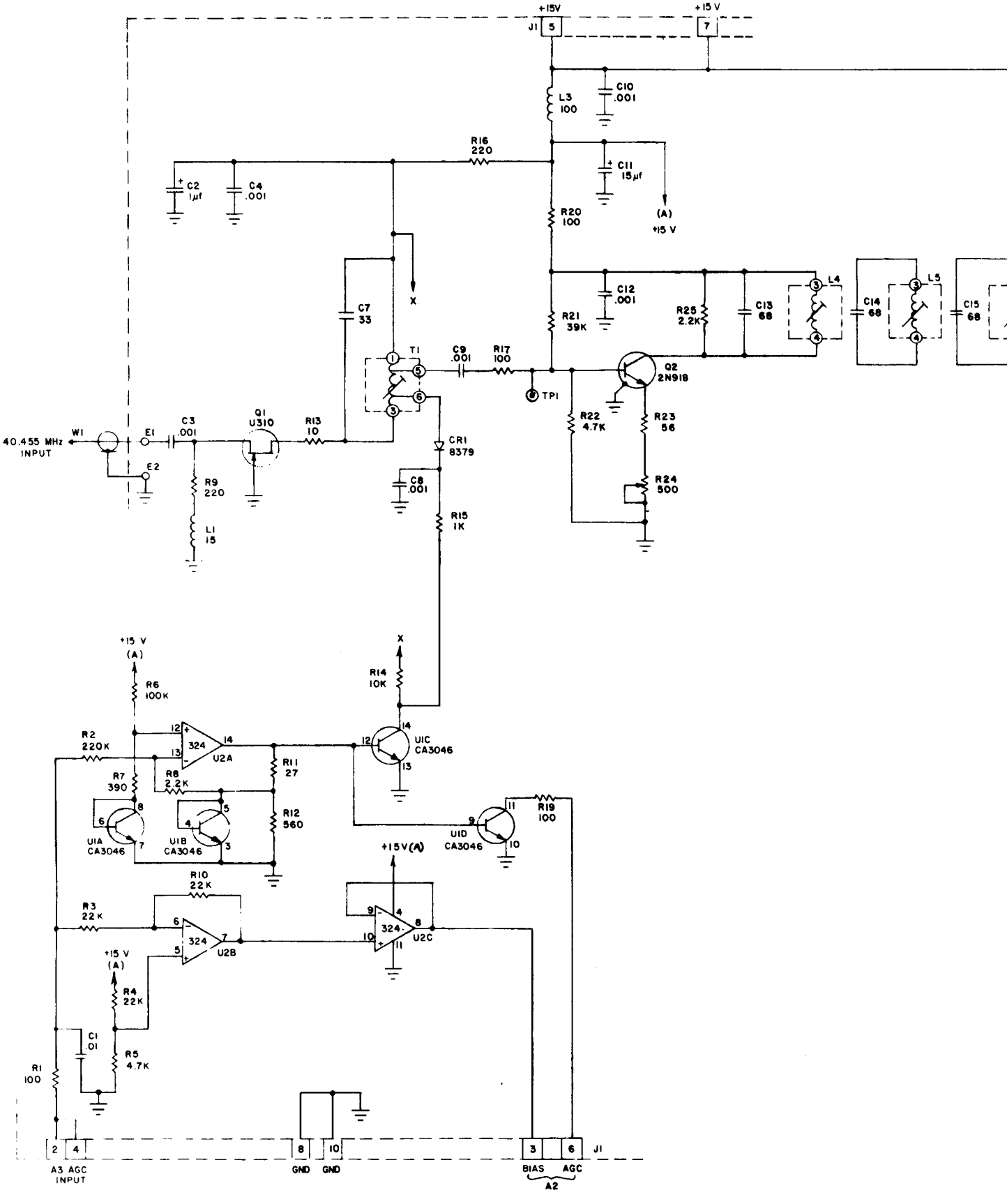


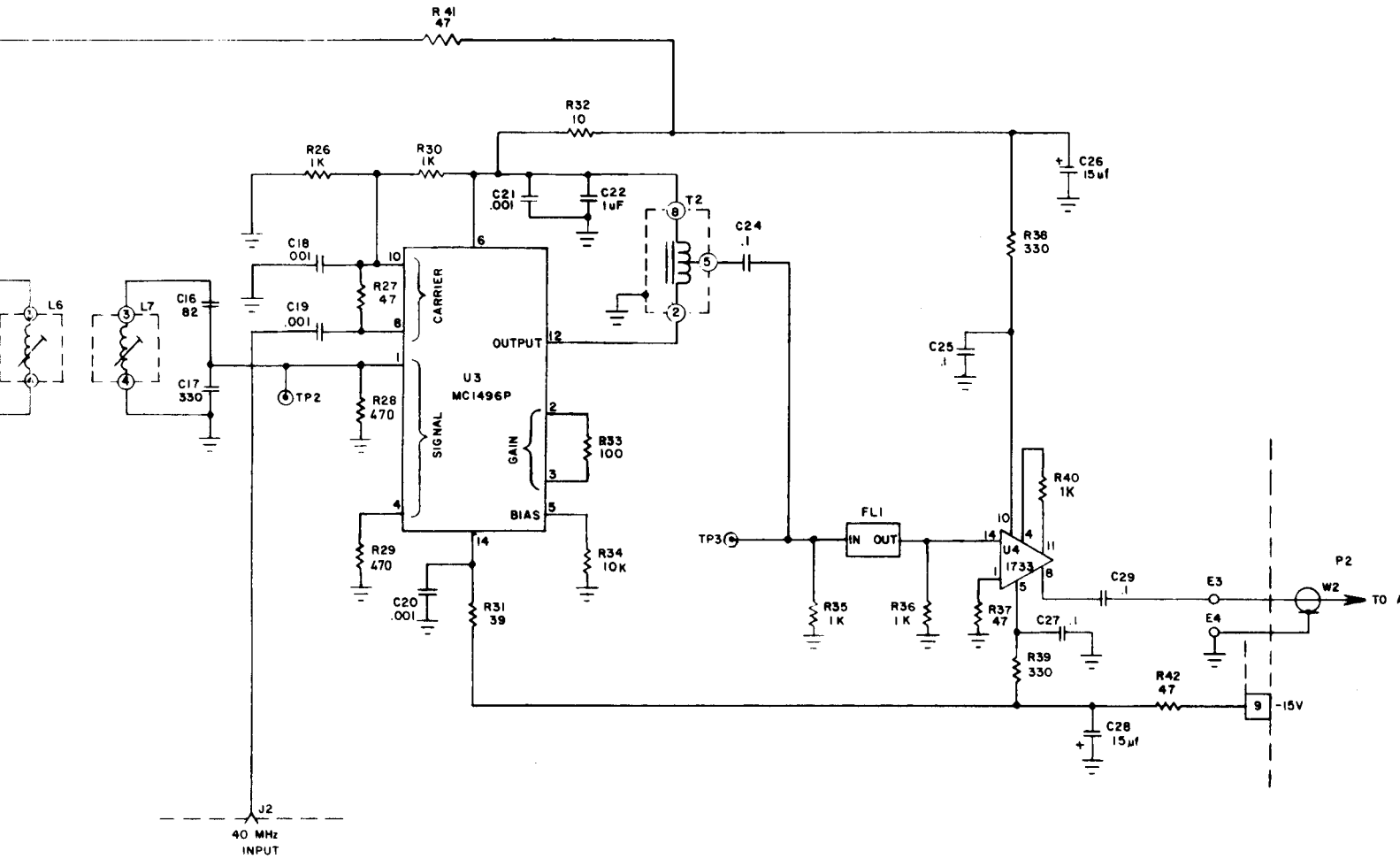
UNLESS OTHERWISE NOTED:

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.

NOTE
MANUAL GAIN SETTING
MAX
MIN.

Circuit: First Mixer Module A2 **Fig.8.2**

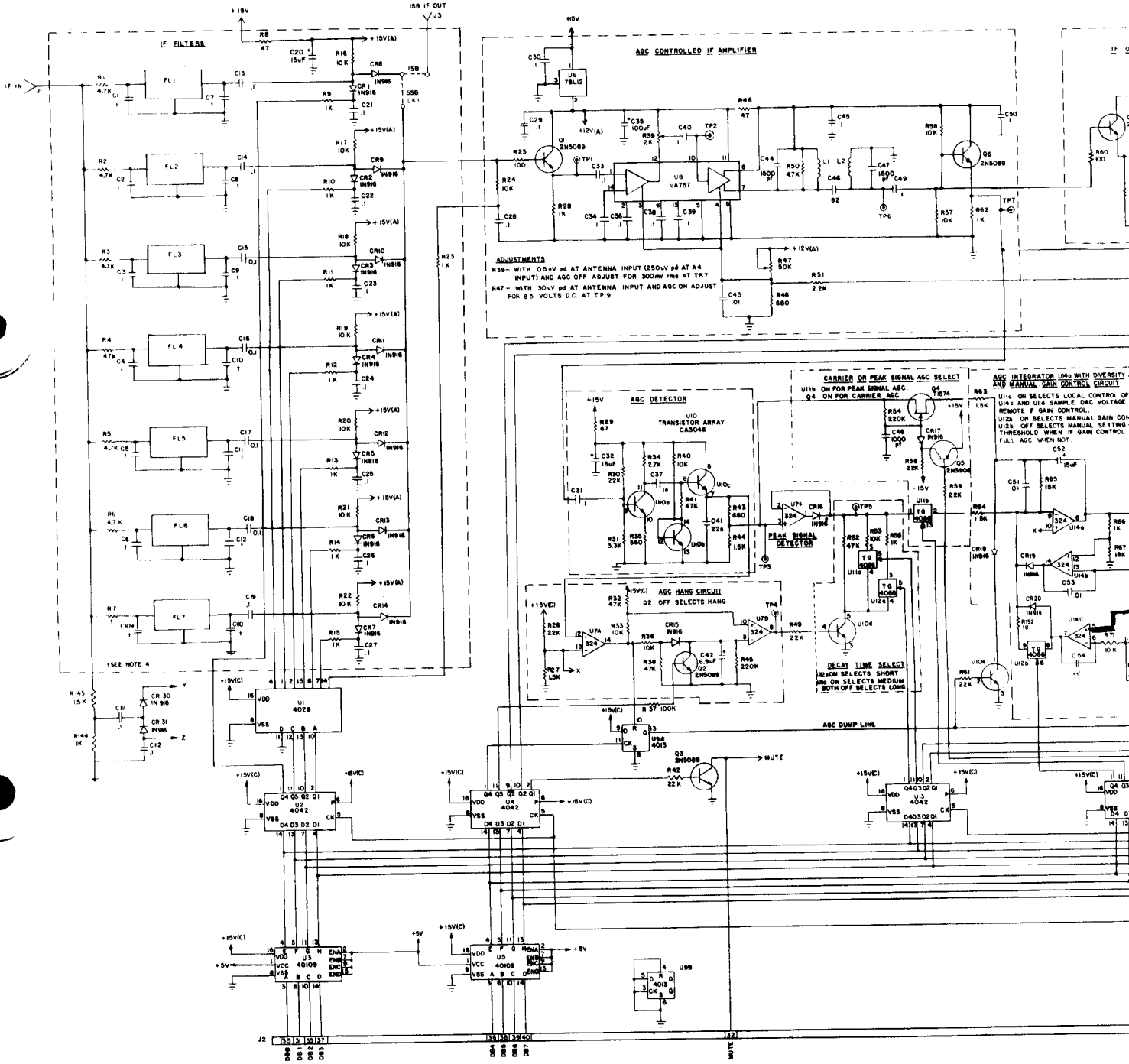

+15V
J1 5
+15 V
7
L3 100
C10 .001
R16 220
C2 1µf
C4 .001
C11 15µf
R20 100
(A) +15 V
C7 33
X
C12 .001
R21 39K
R25 2.2K
C13 68
L4
C14 68
L5
C15 68
T1
C9 .001
R17 100
Q2 2N918
TP1
R22 4.7K
R23 56
R24 500
W1
40.455 MHz INPUT
E1
E2
C3 .001
Q1 U310
R13 10
CR1 8379
C8 .001
R9 220
L1 15
R15 1K
+15 V (A)
R6 100K
X
R14 10K
R2 220K
U2A
UIC CA3046
R11 27
R7 390
R8 2.2K
R12 560
UIA CA3046
UIB CA3046
UID CA3046
R19 100
+15V(A)
R10 22K
R3 22K
U2B
U2C
+15 V (A)
R4 22K
C1 01
R5 4.7K
R1 100
2
4
A3 AGC INPUT
8
10
GND
GND
3
6
J1
BIAS
AGC
A2



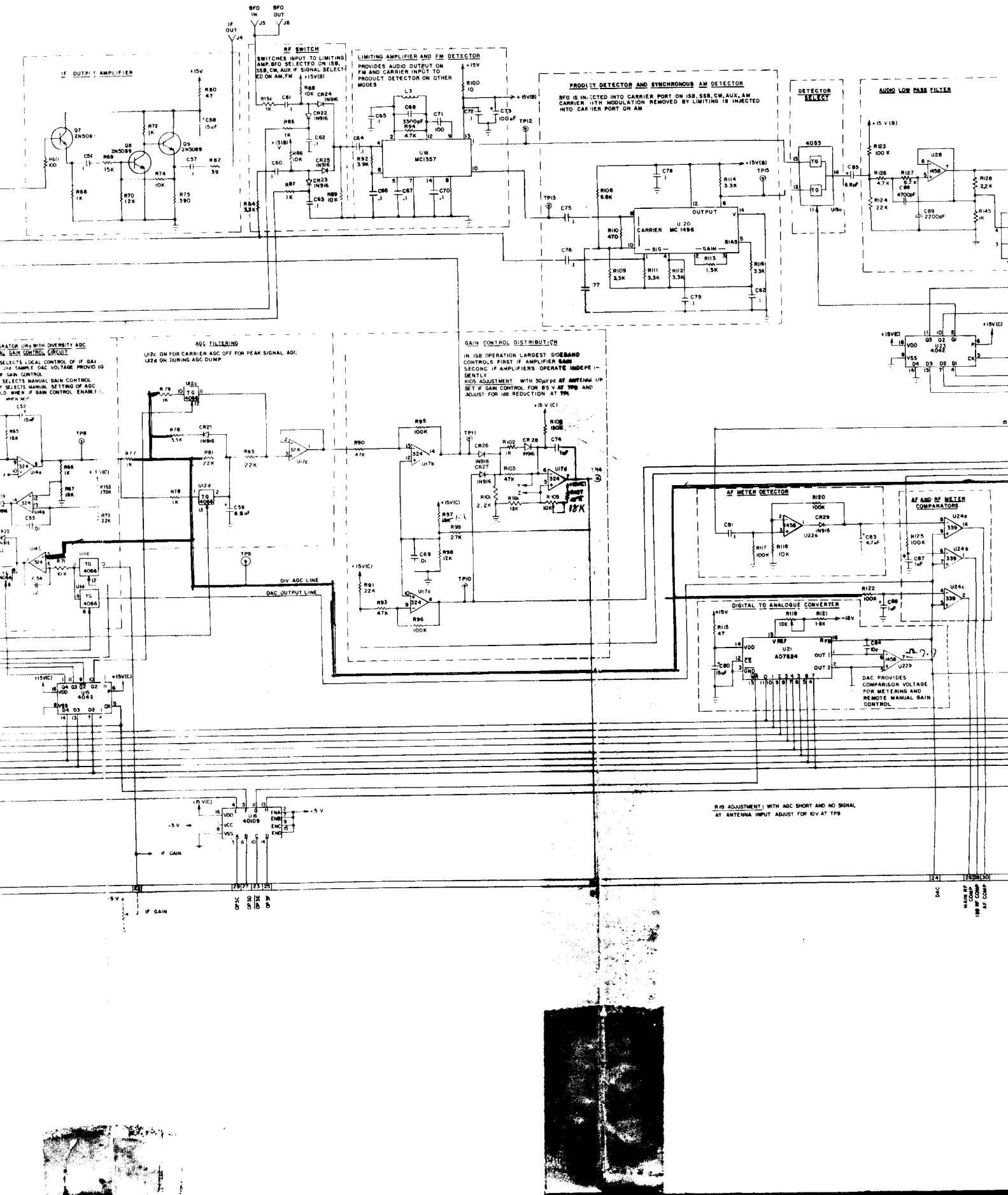
UNLESS OTHERWISE NOTED:

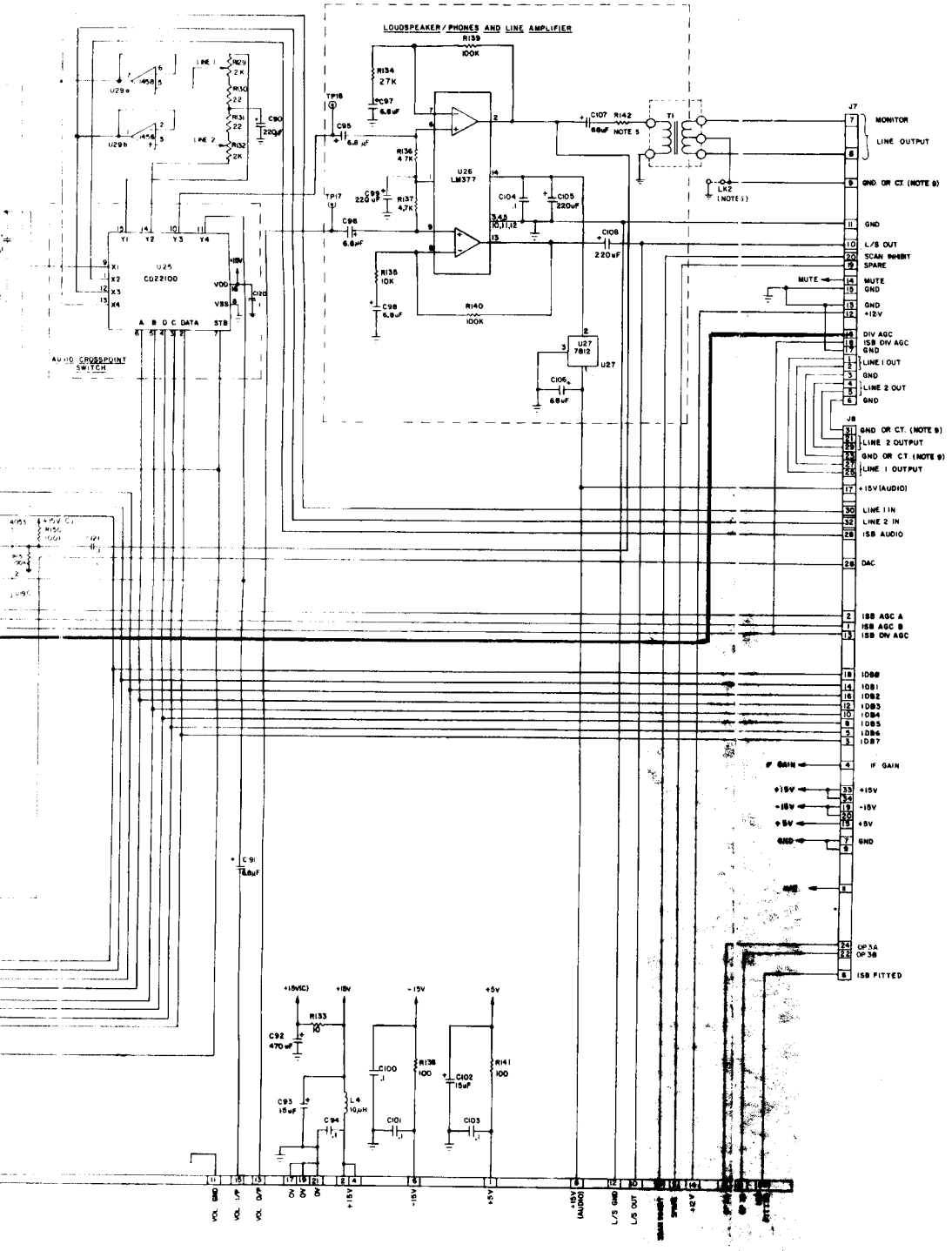
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT
   K=1000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.
4. C5, C6, C23, L2, R18 NOT USED

Circuit: Second Mixer Module A3 **Fig.8.3**



RACAL
TH1496 H08256
1


IF OUTPUT AMPLIFIER
RF SWITCH
SWITCHES INPUT TO LIMITING AMP, BFO SELECTED ON ISB, SSB, CW, AUX. IF SIGNAL SELECTED ON AM, FM
LIMITING AMPLIFIER AND FM DETECTOR
PROVIDES AUDIO OUTPUT ON FM AND CARRIER INPUT TO PRODUCT DETECTOR ON OTHER MODES
PRODUCT DETECTOR AND SYNCHRONOUS AM DETECTOR
BFO IS INJECTED INTO CARRIER PORT ON ISB, SSB, CW, AUX, AM
CARRIER WITH MODULATION REMOVED BY LIMITING IS INJECTED INTO CARRIER PORT ON AM
DETECTOR SELECT
AUDIO LOW PASS FILTER
AGC FILTERING
U12c ON FOR CARRIER AGC OFF FOR PEAK SIGNAL AGC.
U12d ON DURING AGC DUMP
GAIN CONTROL DISTRIBUTION
IN ISB OPERATION LARGEST SIDEBAND CONTROLS FIRST IF AMPLIFIER GAIN
SECOND IF AMPLIFIERS OPERATE INDEPENDENTLY
R105 ADJUSTMENT WITH 30μV pd AT ANTENNA I/P SET IF GAIN CONTROL FOR 8.5 V AT TP8 AND ADJUST FOR 10dB REDUCTION AT TP8
AF METER DETECTOR
AF AND RF METER COMPARATORS
DIGITAL TO ANALOGUE CONVERTER
DAC PROVIDES COMPARISON VOLTAGE FOR METERING AND REMOTE MANUAL GAIN CONTROL
R19 ADJUSTMENT: WITH AGC SHORT AND NO SIGNAL AT ANTENNA INPUT ADJUST FOR 10V AT TP9
DIV AGC LINE
DAC OUTPUT LINE
IF GAIN
BFO IN J5
BFO OUT J6
IF OUT J4
U18 MC1357
U 20 CARRIER MC 1496
OUTPUT
SIG
GAIN
BIAS
U21 AD7524
VREF
VDD
OUT 1
OUT 2
GND
DAC
MAIN RF COMP
2ND IF COMP
AF COMP



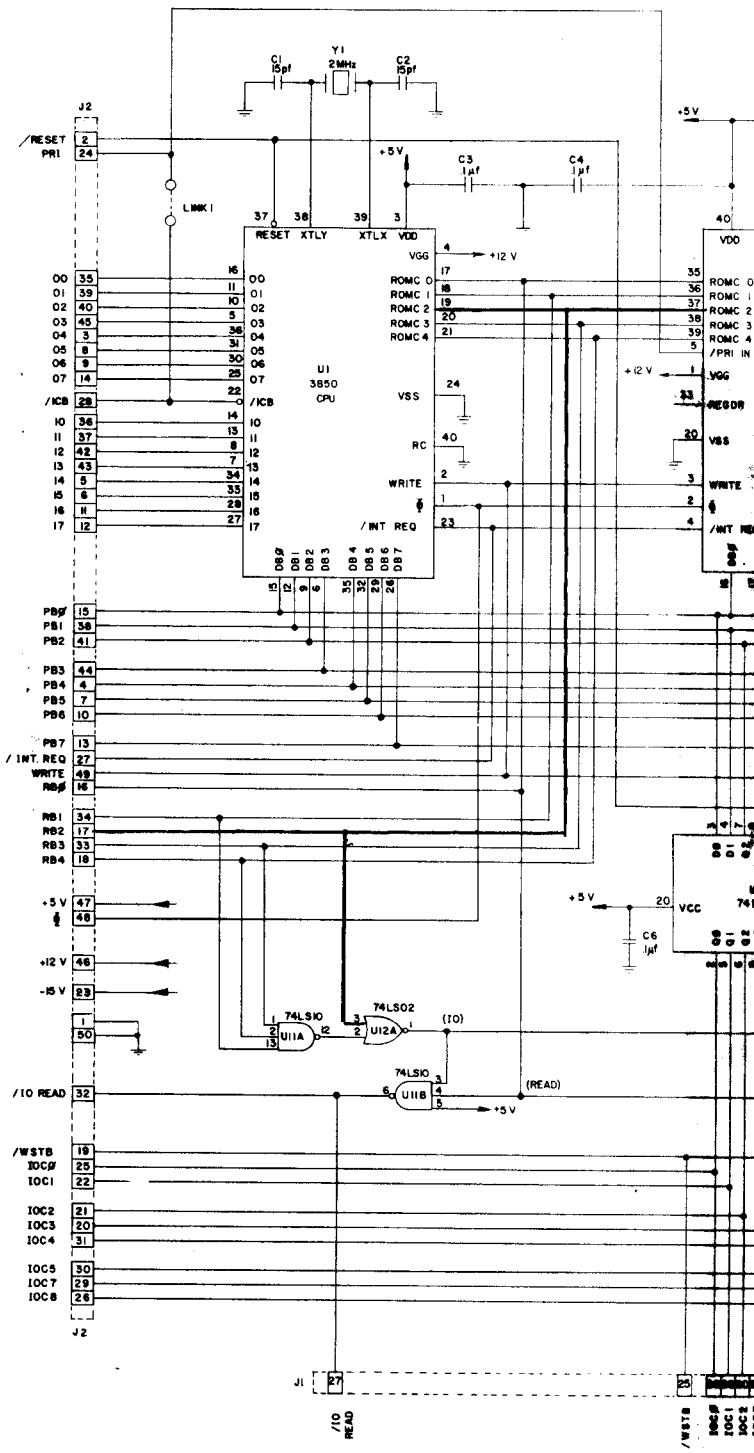
NOTES

1. RESISTOR VALUES ARE IN OHMS, K=1000 M=1 000 000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
4. ▽ VALUE DEPENDENT ON FILTER COMPLEMENT.
5. R142 VALUE DEPENDS ON T1
6. IF T1 HAS NO CENTRE TAP LK2 IS FITTED
   IF T1 HAS CENTRE TAP LK2 IS OMITTED

I.C. NO.	DEVICE	GND	+15V(B)	+15V(C)	-15V
U7	324	11		4	
U14	324	11		4	
U17	324	11		4	
U9	4013	7		14	
U11	4068	7		14	
U12	4066	7		14	
U19	4053	8,7,8		16	
U22	1458			8	4
U24	339	12		3	
U28	1458		8		4
U29	1458	4	8		

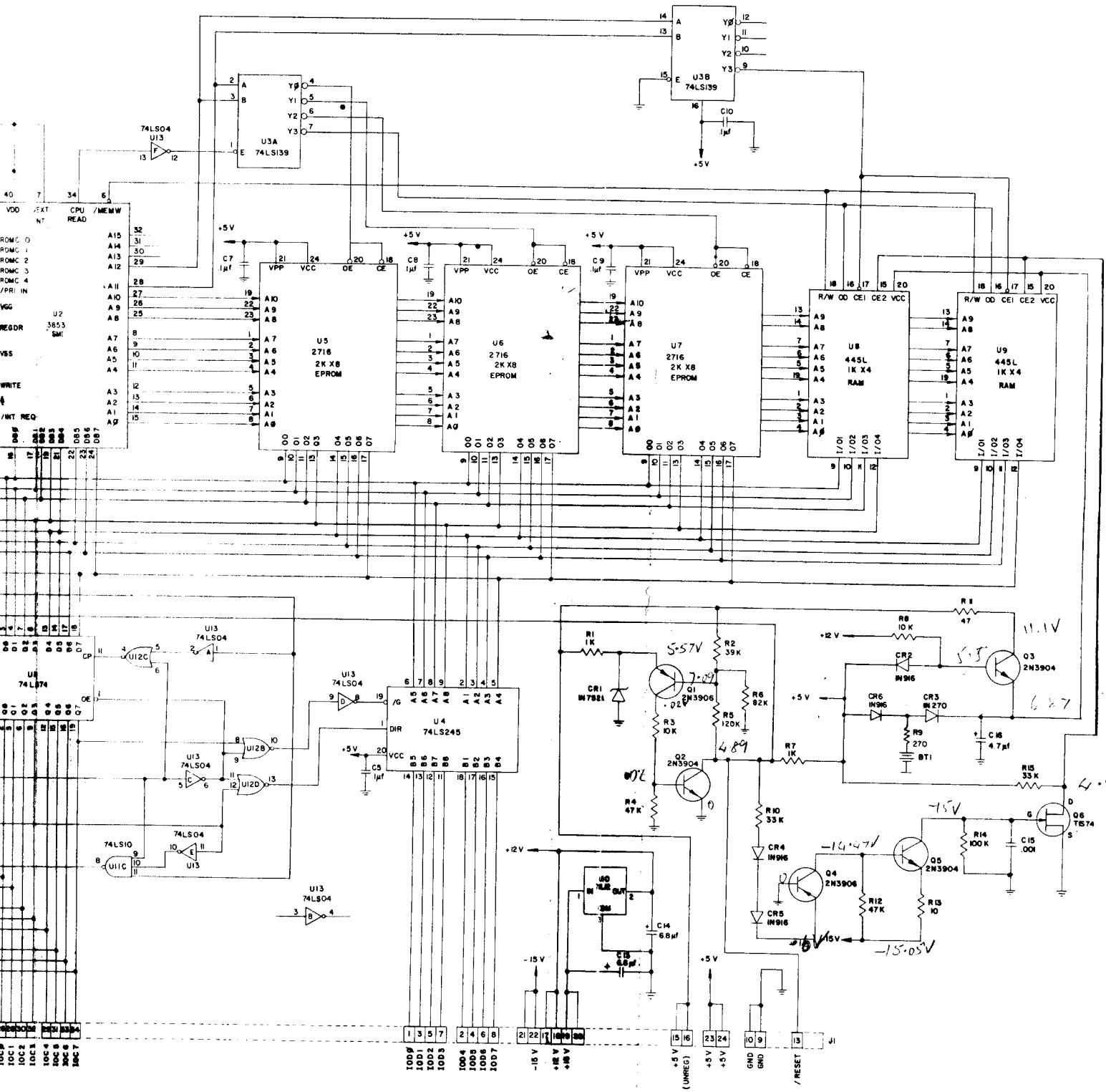
Circuit: Main IF/AF Module A4 **Fig.8.4**

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14
GND	24	20	8	10	12	12	12	8	8	3	7	7	7	10
+5	3	40	16	20	21 24	21 24	21 24				14	14	14	20
+12	4	1												
+15										1				



RACAL

TH1496	E08202
1	



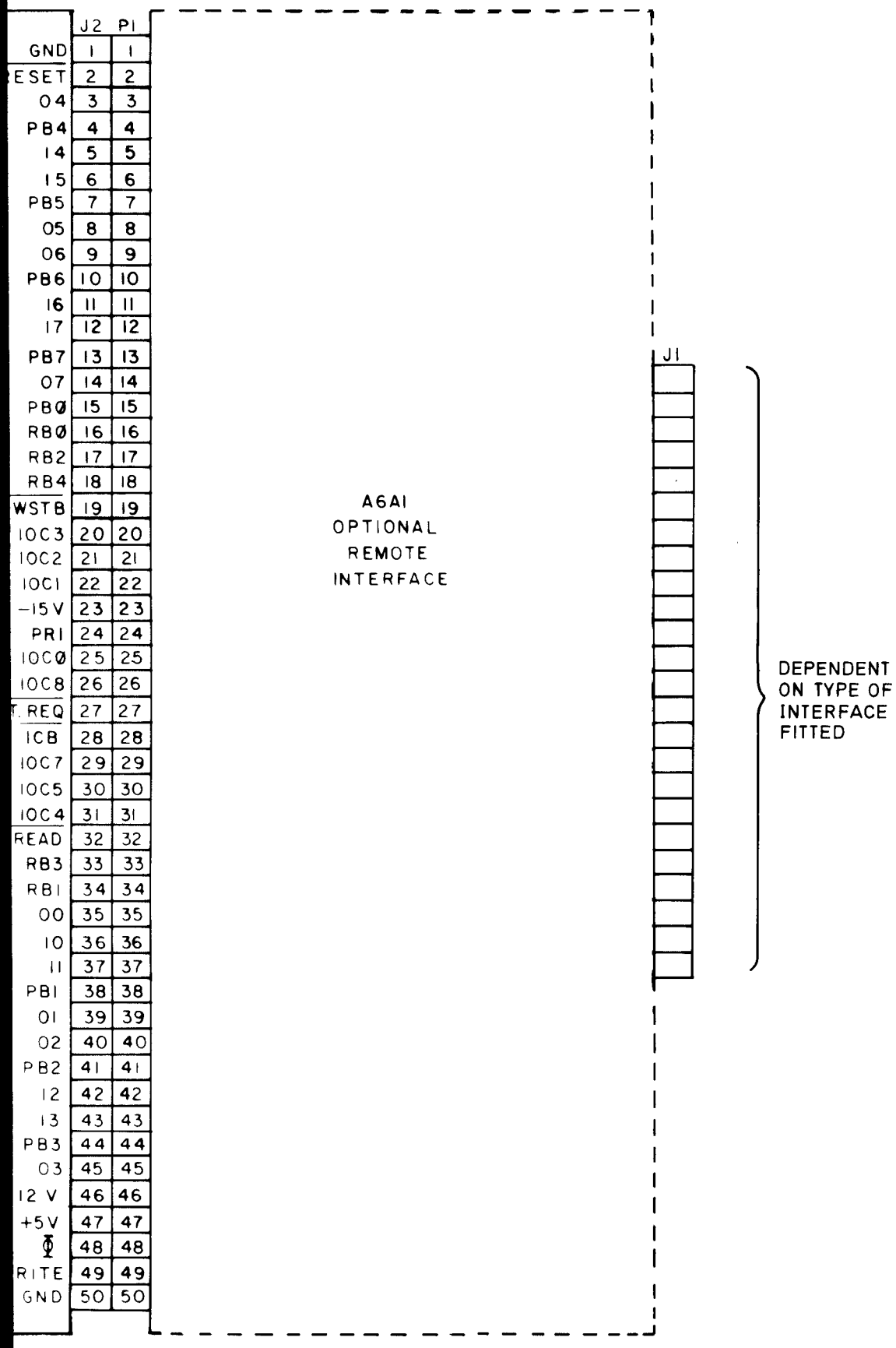
Circuit : Microcomputer Module A6 A2

Fig.8.5

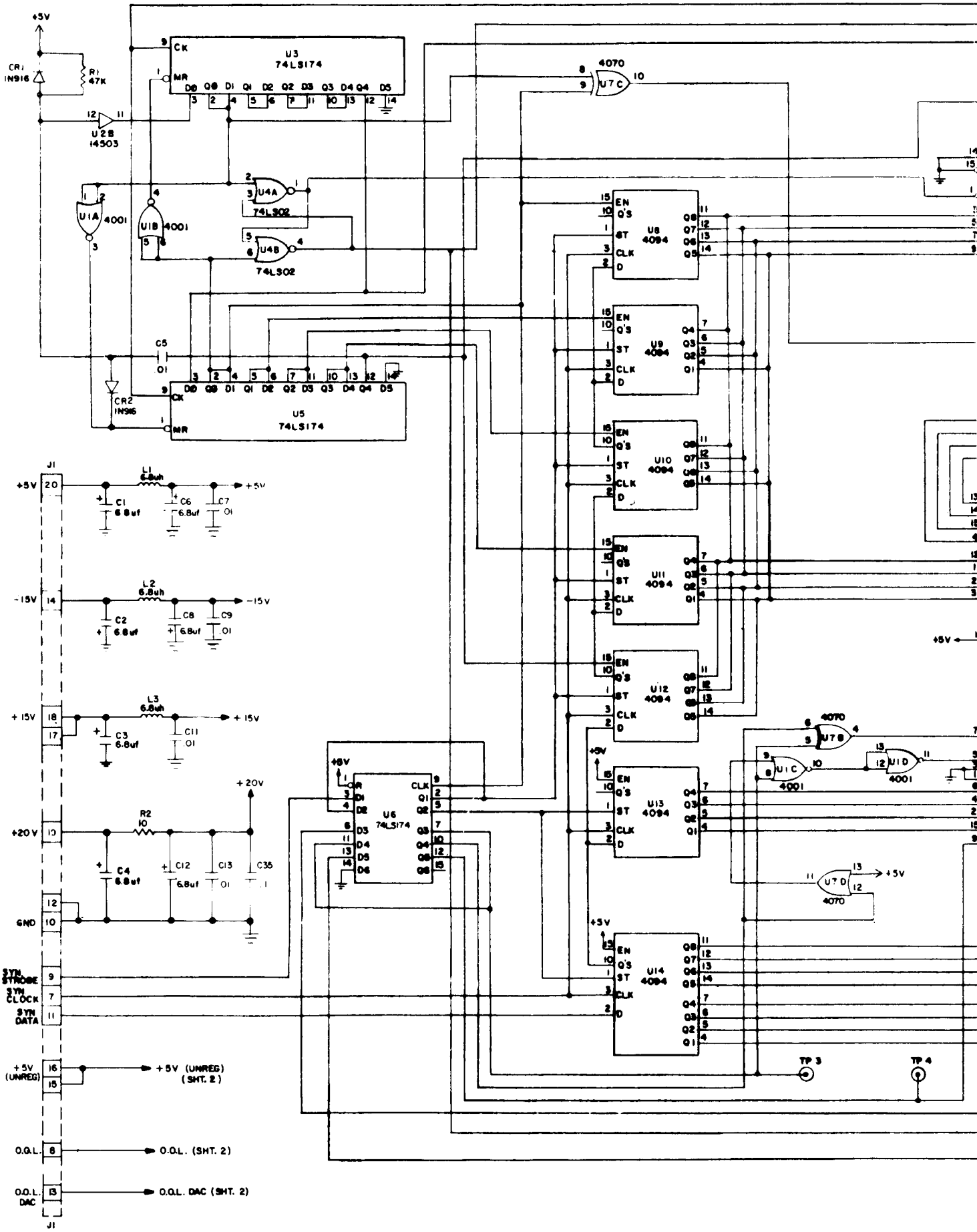
J1

1	IODO
2	IOD4
3	IOD1
4	IOD5
5	IOD2
6	IOD6
7	IOD3
8	IOD7
9	GND
10	GND
11	N/C
12	N/C
13	RESET
14	N/C
15	+5V (UNREG)
16	+5V (UNREG)
17	+12V
18	+12V
19	+15V
20	+15V
21	−15V
22	−15V
23	+5V
24	+5V
25	WSTB
26	IOCO
27	IO READ
28	IOC1
29	IOC4
30	IOC2
31	IOC5
32	IOC3
33	IOC6
34	IOC7

A6A2
MICROCOMPUTER
MODULE
E08202

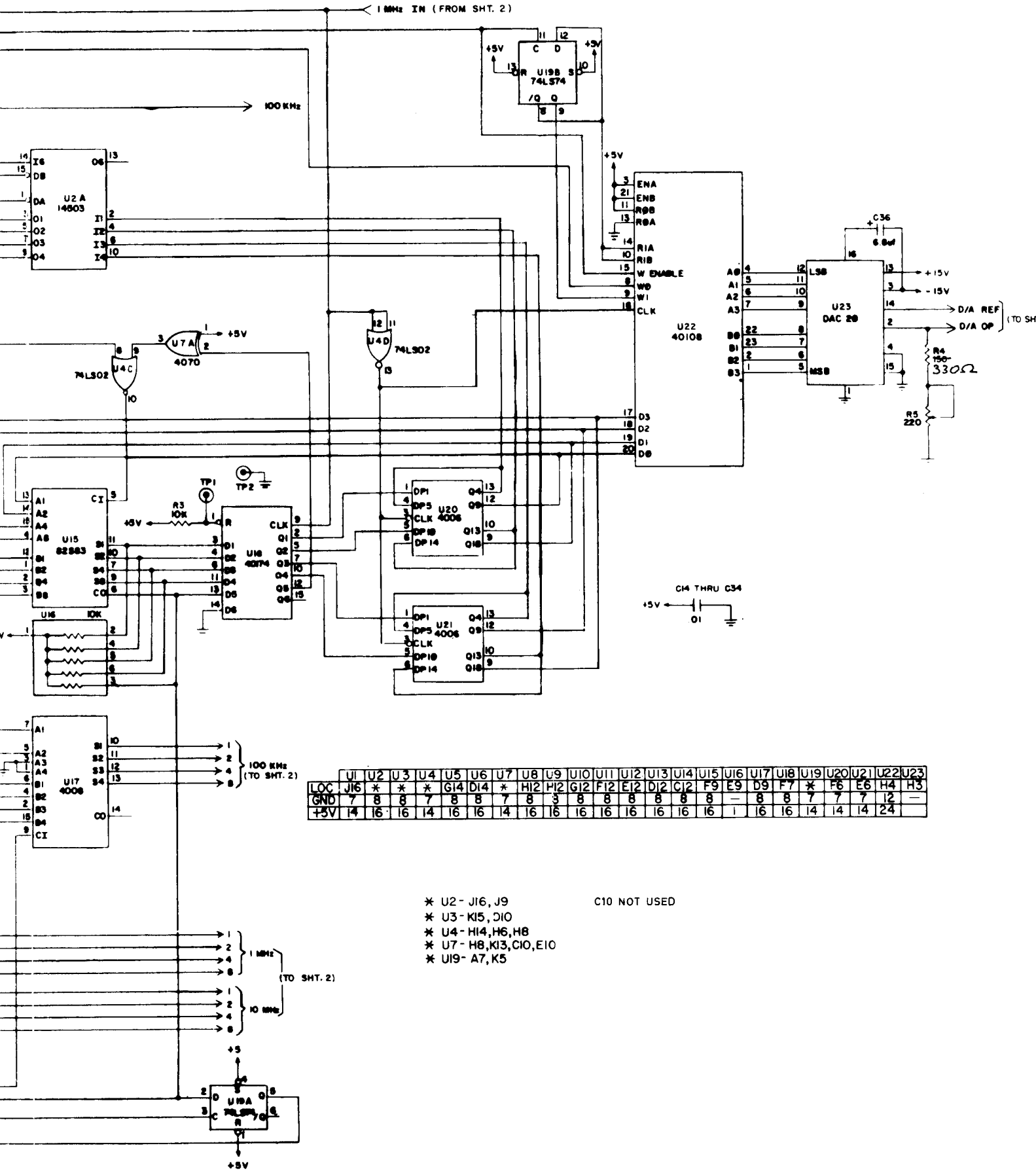


Interconnection Diagram : A6 A1 and A6 A2 Fig.8.6



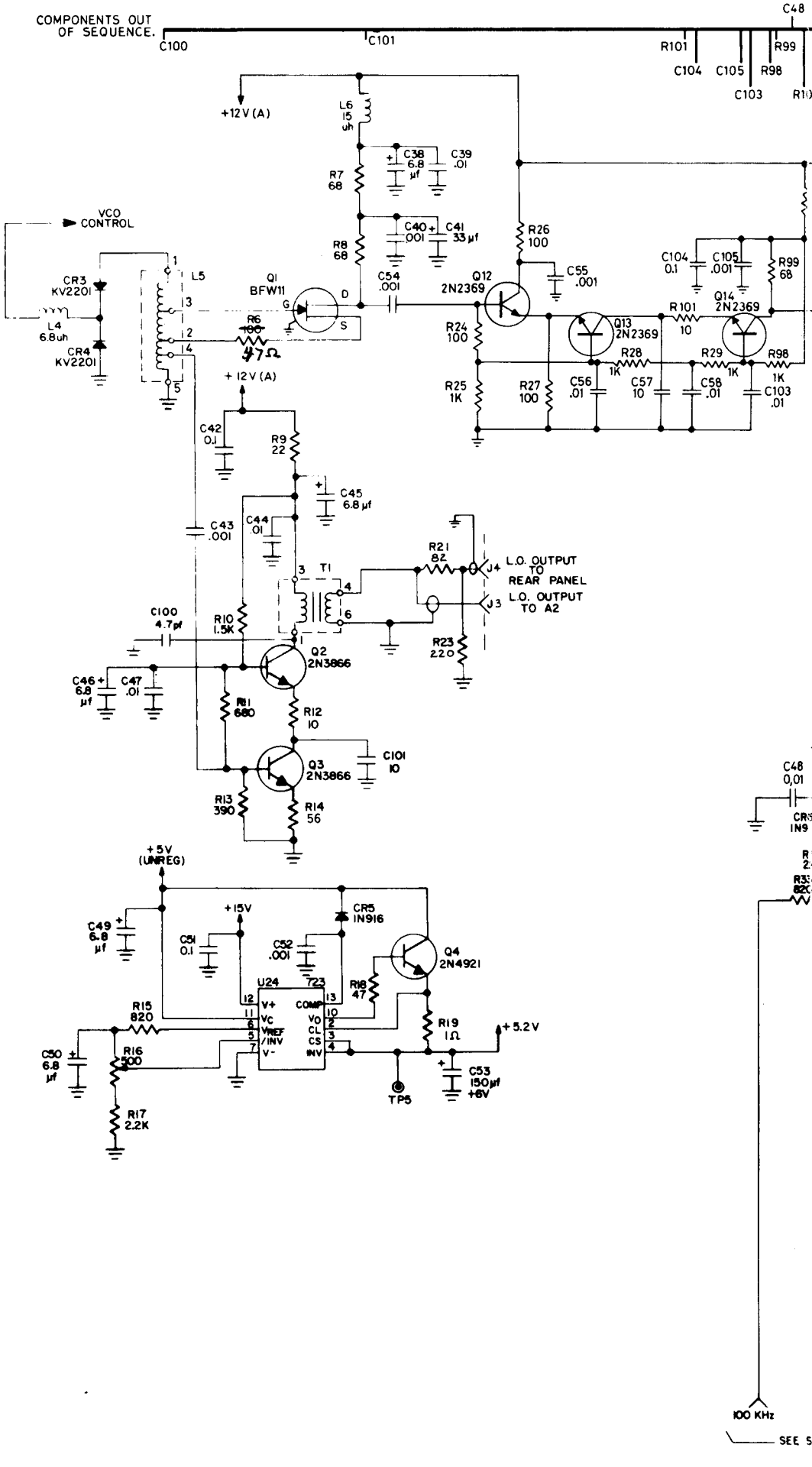
RACAL

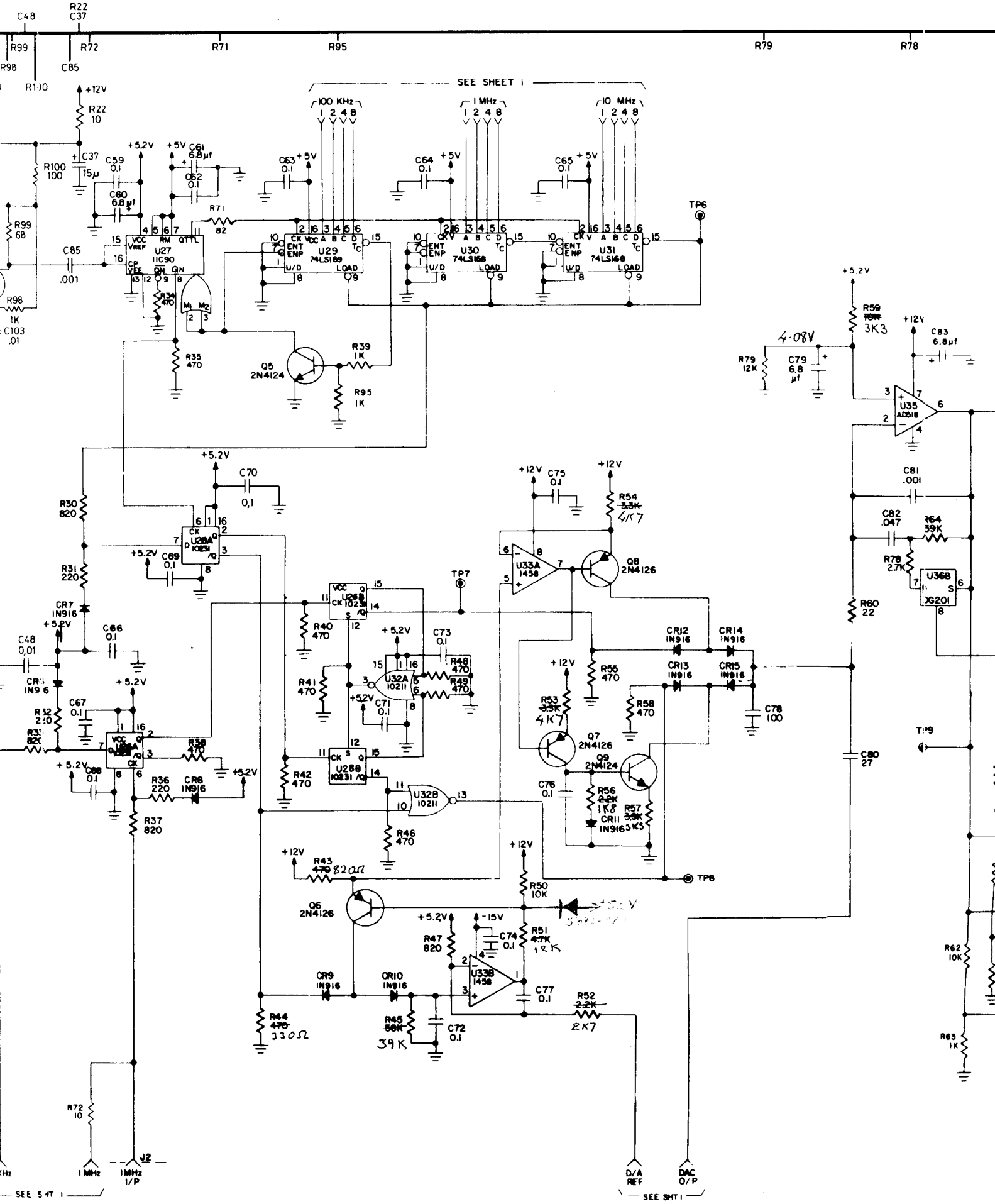
TH 1496	DC80788
1	

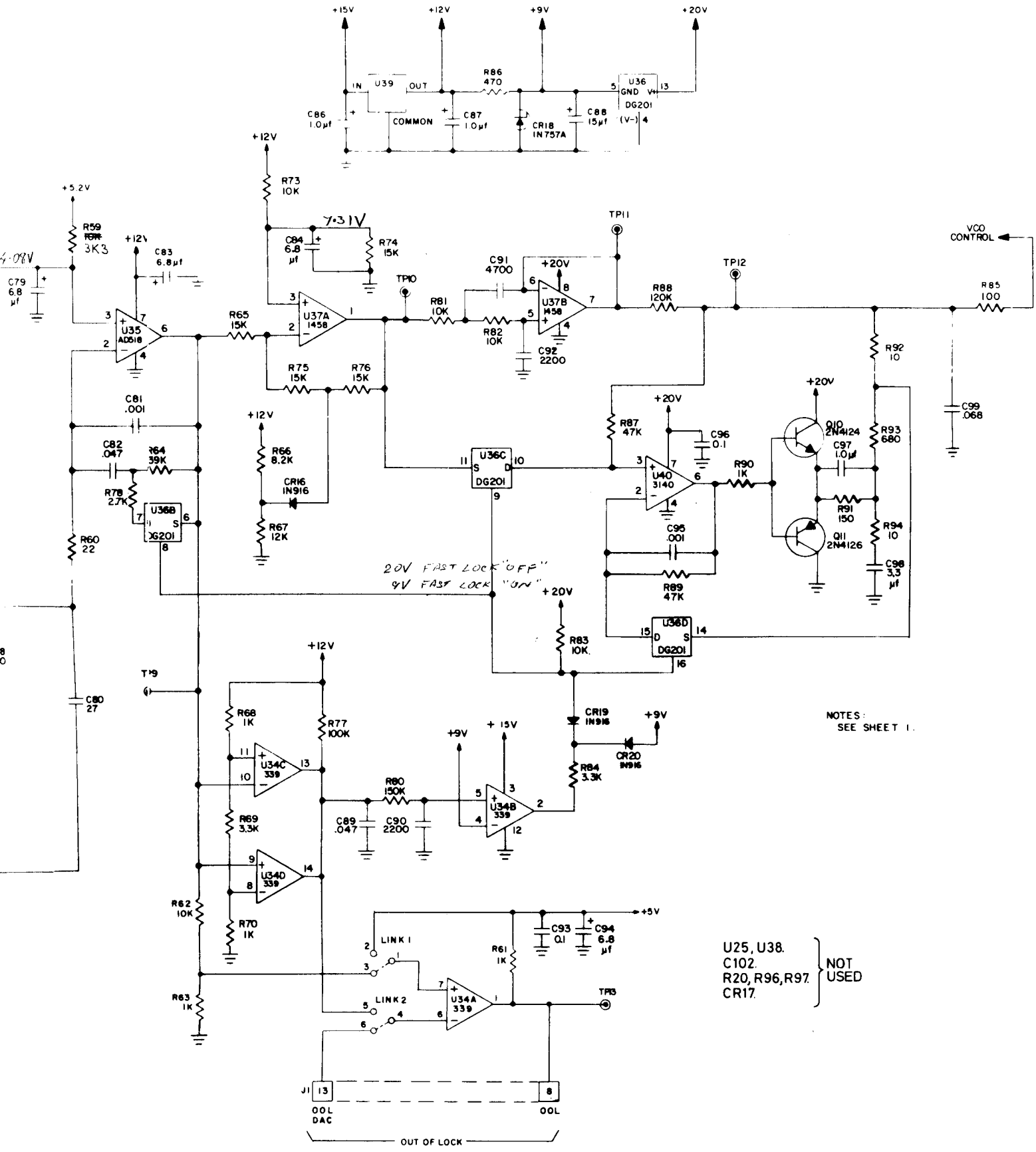


	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23
LOC	J16	*	*	*	G14	D14	*	H12	H12	G12	F12	E12	D12	C12	F9	E9	D9	F7	*	F6	E6	H4	H3
GND	7	8	8	7	8	8	7	8	8	8	8	8	8	8	8	—	8	8	7	7	7	12	—
+5V	14	16	16	14	16	16	14	16	16	16	16	16	16	16	16	1	16	16	14	14	14	24	

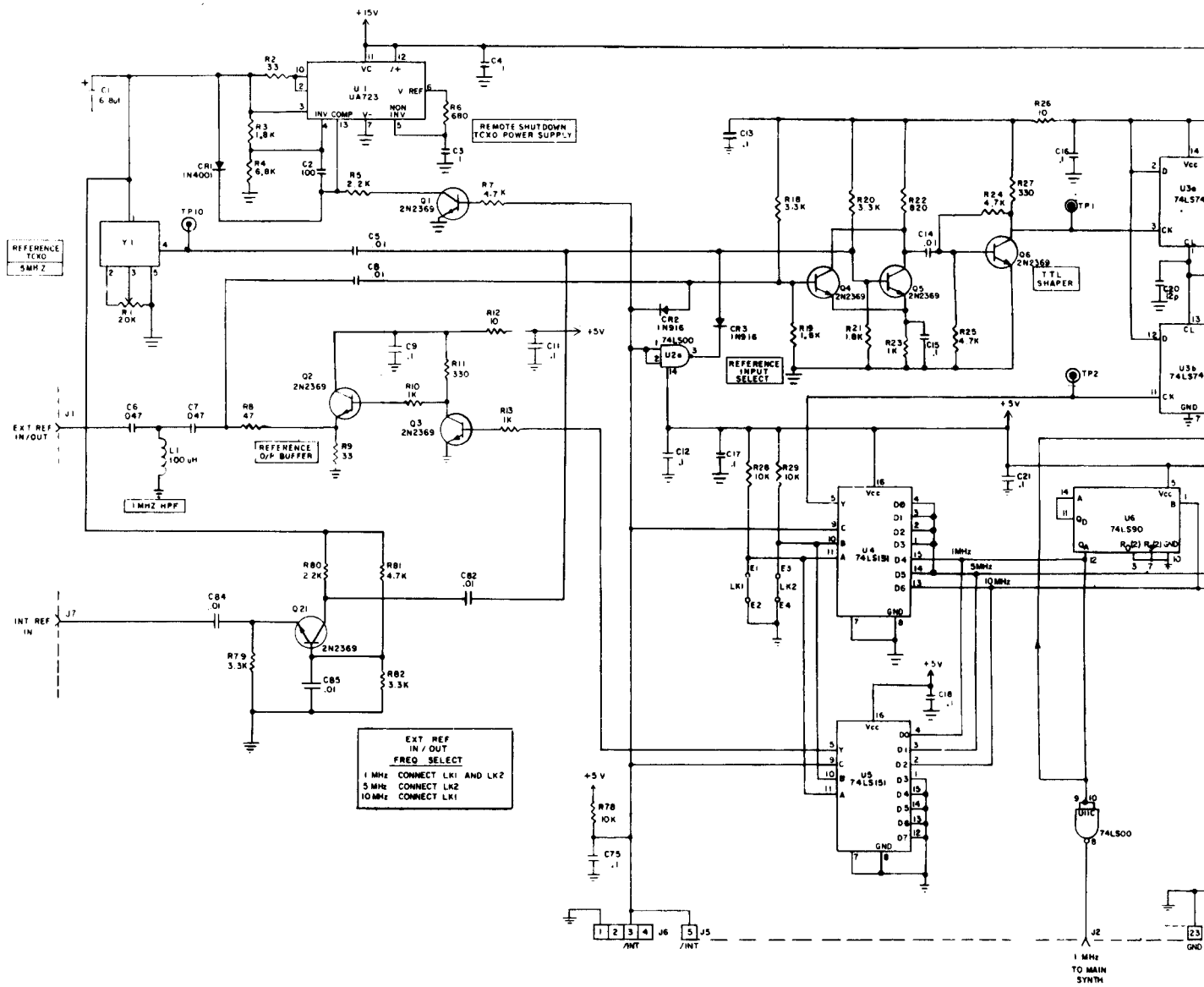
Circuit: First LO Synthesizer A7 (Sheet 1) Fig.8


COMPONENTS OUT OF SEQUENCE.
C100
C101
C48
R101
C104
C105
R98
R99
C103
+12V (A)
L6 15 uh
C38 6.8 µf
C39 .01
R7 68
R8 68
C40 .001
C41 33 µf
VCO CONTROL
CR3 KV2201
CR4 KV2201
L4 6.8uh
L5
Q1 BFW11
R6 100
47Ω
C54 .001
Q12 2N2369
R26 100
C55 .001
C104 0.1
C105 .001
R99 68
R101 10
Q13 2N2369
Q14 2N2369
R24 100
R28 1K
R29 1K
R98 1K
R25 1K
R27 100
C56 .01
C57 10
C58 .01
C103 .01
+12V (A)
C42 0.1
R9 22
C45 6.8 µf
C43 .001
C44 .01
T1
R21 82
J4
L.O. OUTPUT TO REAR PANEL
J3
L.O. OUTPUT TO A2
C100 4.7pf
R10 1.5K
R23 220
Q2 2N3866
C46 6.8 µf
C47 .01
R11 680
R12 10
C101 10
Q3 2N3866
R13 390
R14 56
+5V (UNREG)
C49 6.8 µf
+15V
CR5 IN916
C51 0.1
C52 .001
Q4 2N4921
U24
723
R18 47
R15 820
R19 1Ω
+5.2V
C50 6.8 µf
R16 500
C53 150µf +6V
TP5
R17 2.2K
C48 0,01
100 KHz
SEE S


SEE SHEET 1
100 KHz
1 MHz
10 MHz
+12V
+5.2V
+5V
U27 11C90
U29 74LS169
U30 74LS168
U31 74LS168
U35 AD518
U33A 1458
U33B 1458
U32A 10211
U32B 10211
U28A 10231
U28B 10231
Q5 2N4124
Q6 2N4126
Q7 2N4126
Q8 2N4126
Q9 2N4124
U36B JG201
TP6
TP7
TP8
TP9
4·08V
-15V
D/A REF
DAC O/P
SEE SHT 1
1 MHz
1MHz I/P

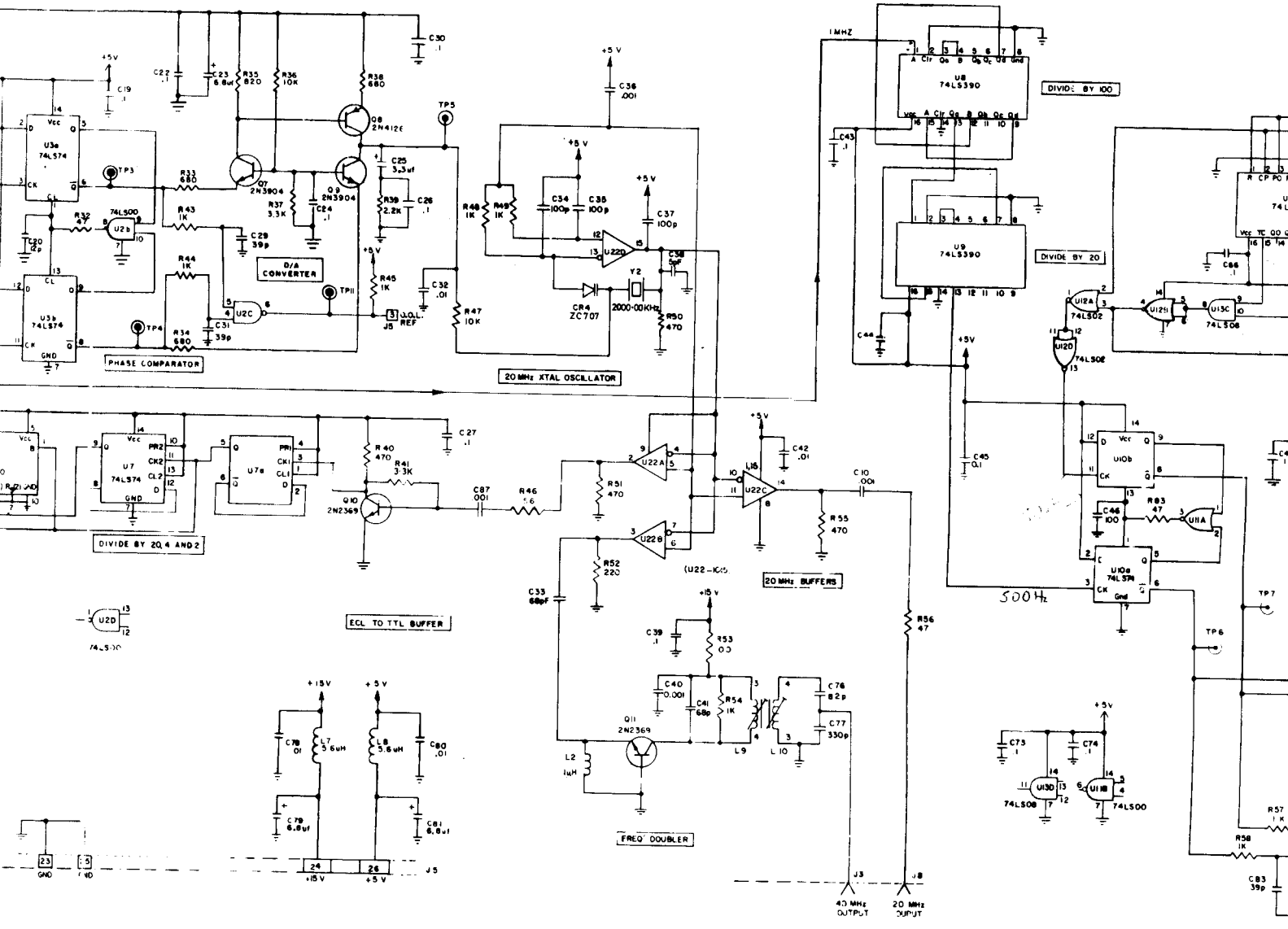


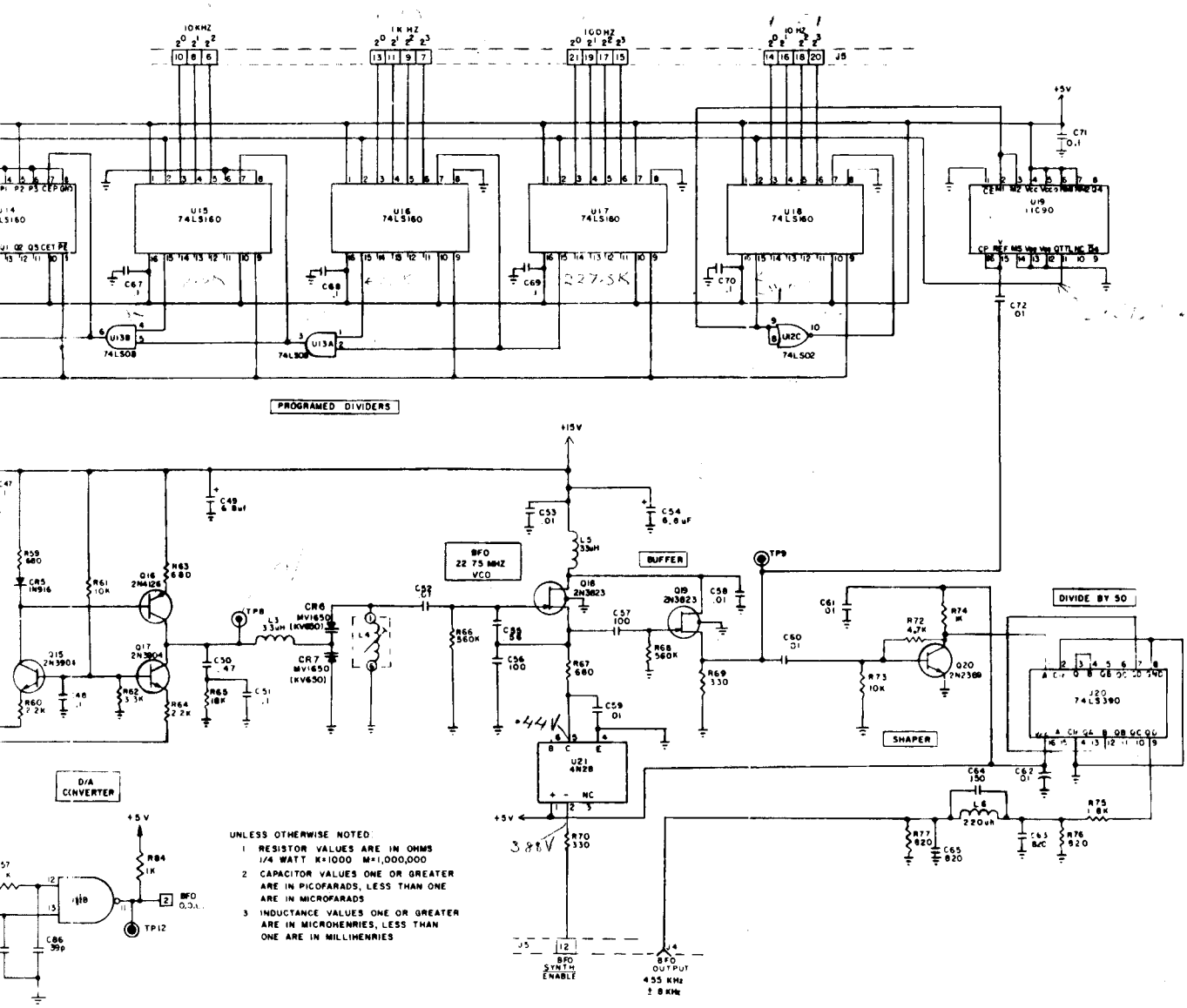
Circuit: First LO Synthesizer A7 Fig.8.8



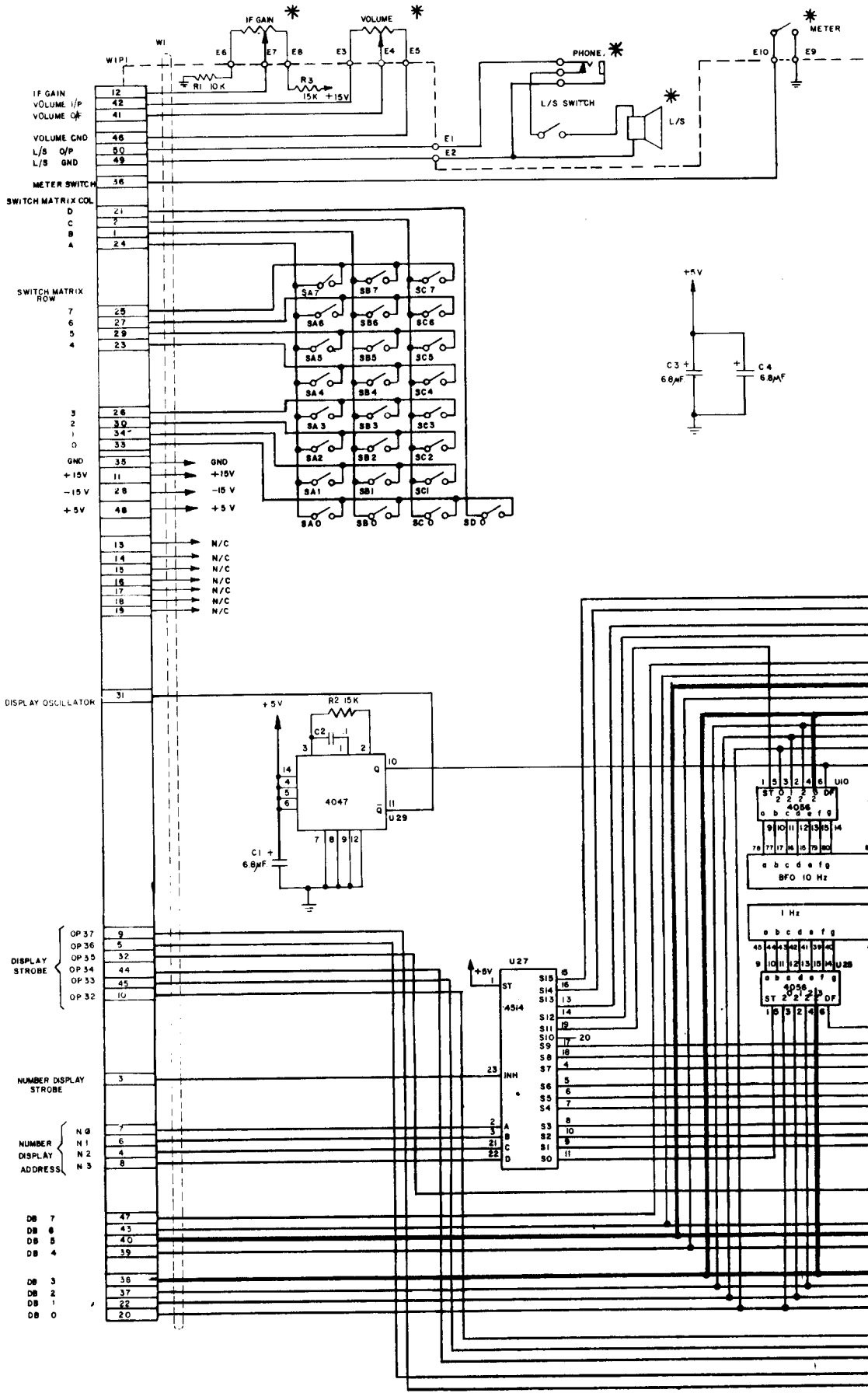
RACAL

TH 1496	HO8136
1	


PHASE COMPARATOR
D/A CONVERTER
20 MHz XTAL OSCILLATOR
DIVIDE BY 100
DIVIDE BY 20
DIVIDE BY 20,4 AND 2
ECL TO TTL BUFFER
20 MHz BUFFERS
FREQ DOUBLER
1MHZ
500Hz
40 MHz OUTPUT
20 MHz OUTPUT



Circuit: Second LO/BFO Synthesizer Module A8 Fig. 8.9



RACAL

TH1496 HO 8197

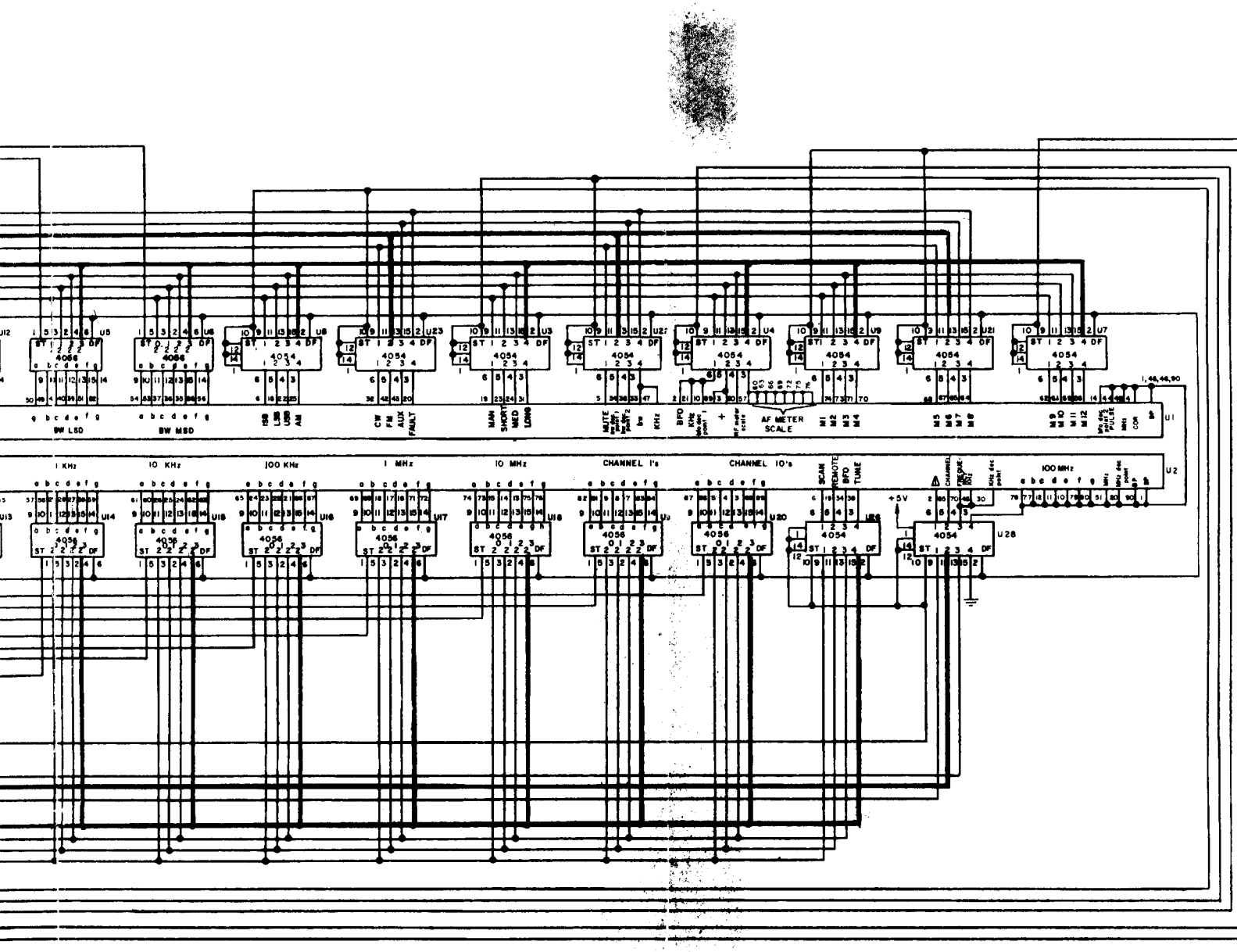
1

Circuit : Front F

SWITCH FUNCTIONS

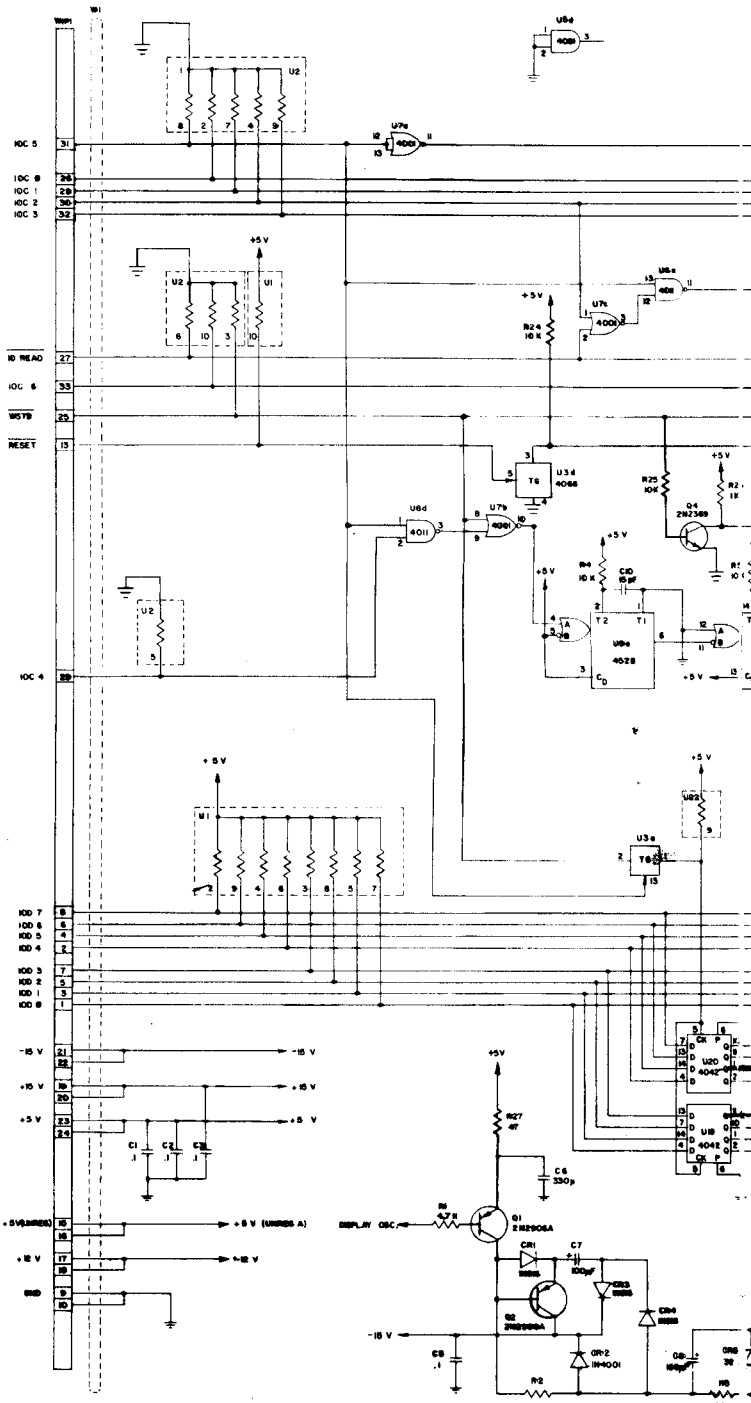
ROW \ COLUMN	A	B	C	D
7	ENTER	0 AUX	TUNE	
6	SCAN	9 LONG	BFO	
5	RECALL	8 MED	FM	
4	CHAN	7 SHORT	CW	
3	FREQ	6 MAN	AM	
2	3 BW 3	5 BW 5	USB	
1	BW	4 BW 4	LSB	
0	REMOTE	2 BW 2	ISB	STORE

	+5V	GND
4047	14	7
4054	16	7,8
4056	16	7,8
4514	24	12



nt Panel Switch/Display Board A9 A1

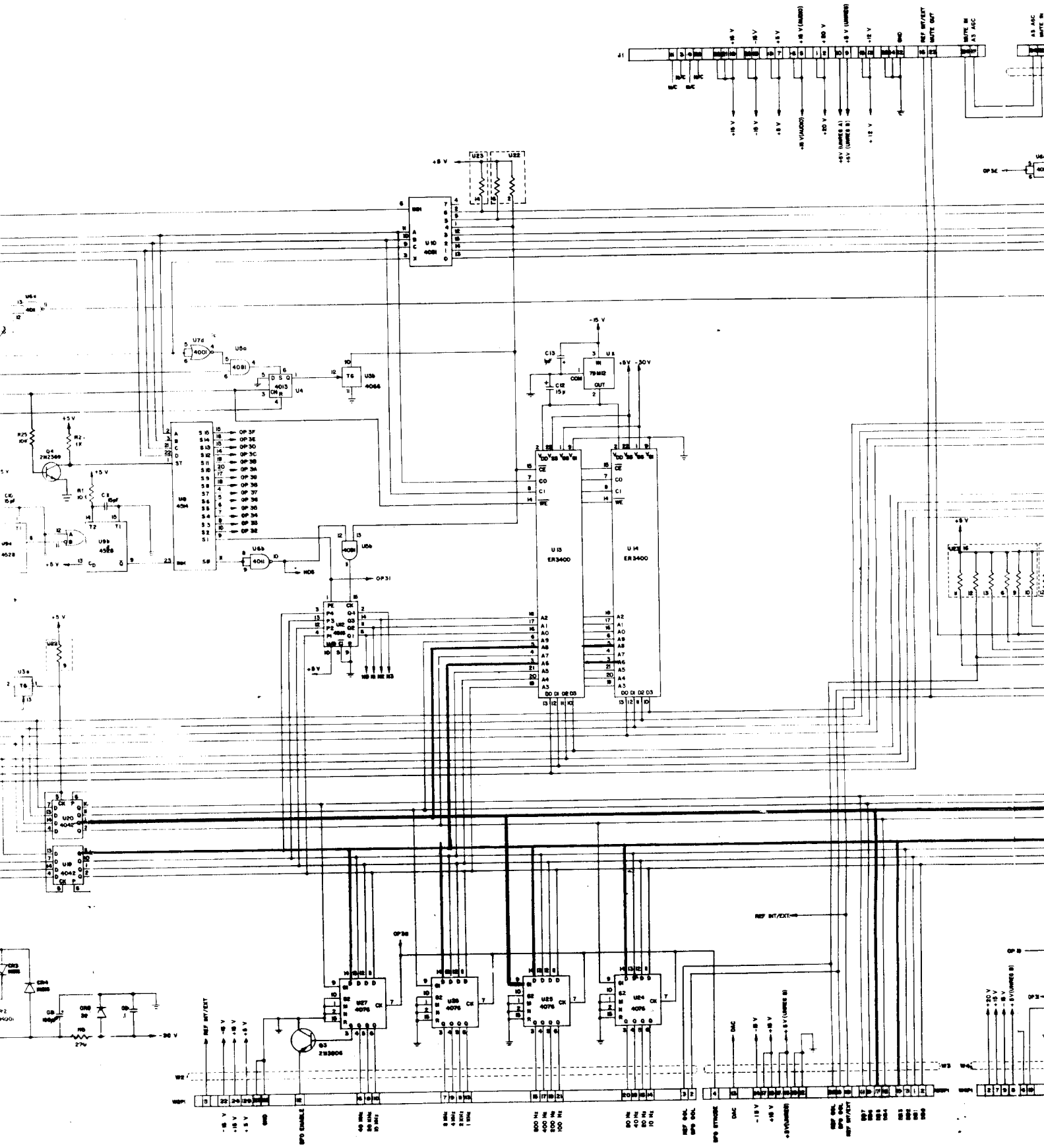
Fig.8



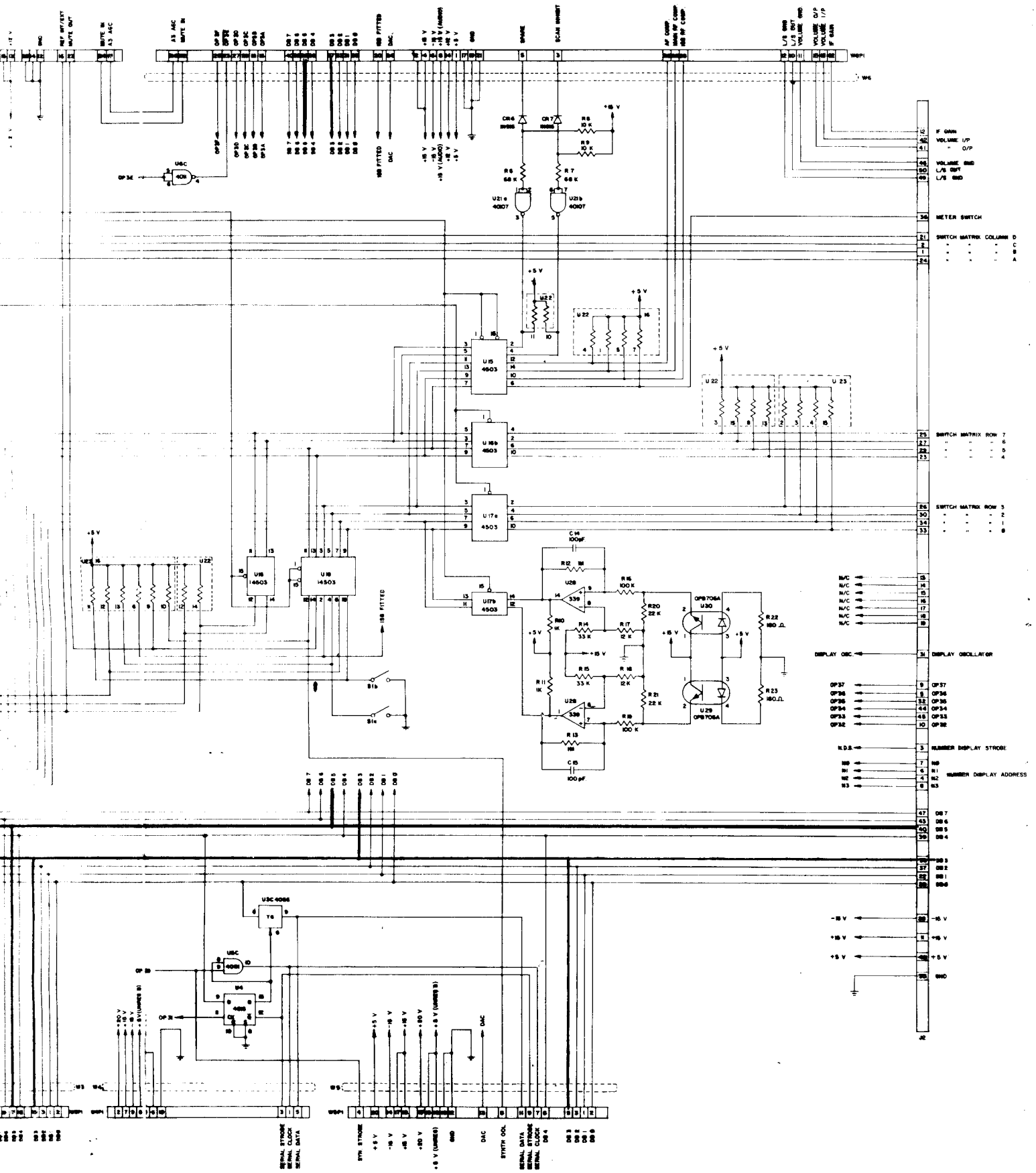
REF. DESIG.	IC	GND	+5 V	+15 V
U7	4001	7	14	
U6	4011	7	14	
U4	4013	7	14	
U19,U20	4042	8	16	
U10	4001	7,8	16	
U3	4066	7	14	
U24,U25,U26,U27	4076	8	16	
U5	4081	7	14	
U21	40107	4		8
U22,U23,U17,U18	4093	8	16	
U8	4099	12	24	
U12	4516	8	16	
U9	4528	8	16	
U28	339	12		3

RACAL

TH 1496	H0 8268
1	

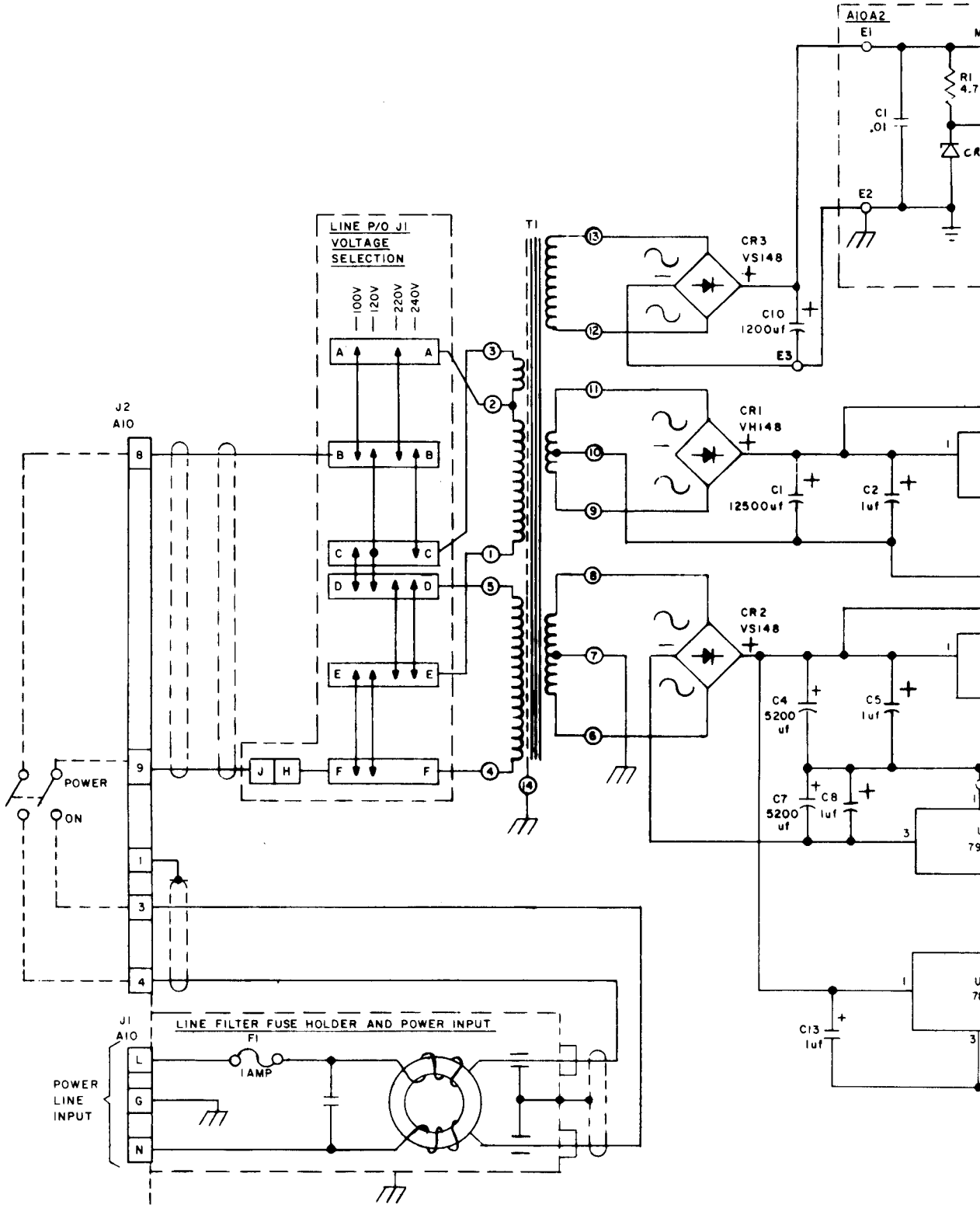


Circuit : Front Panel Memory Board A9 A2



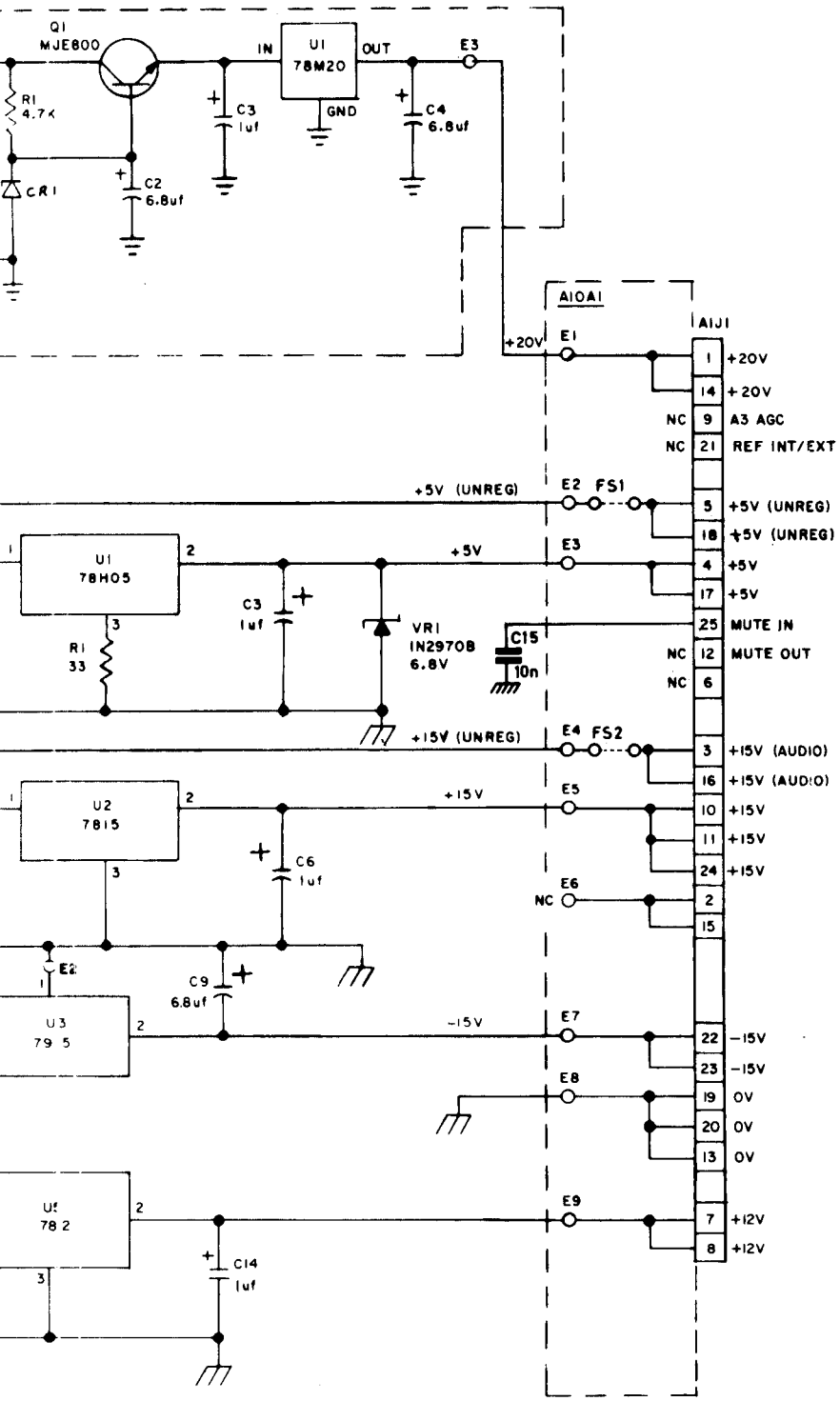
d A9 A2

Fig.8.11

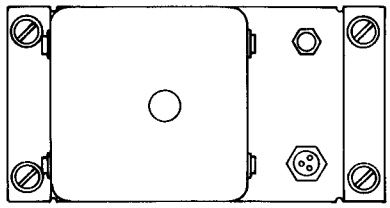


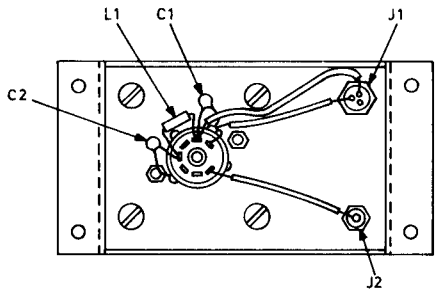
RACAL

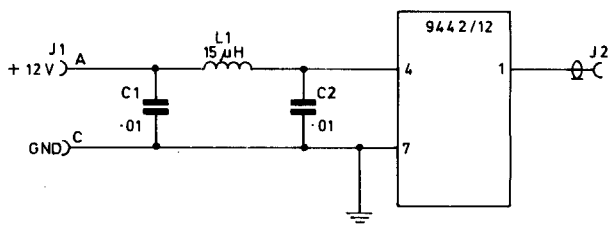
TH 1496	D08719
2	



Circuit: AC Power Supply Module A10 Fig. 8.





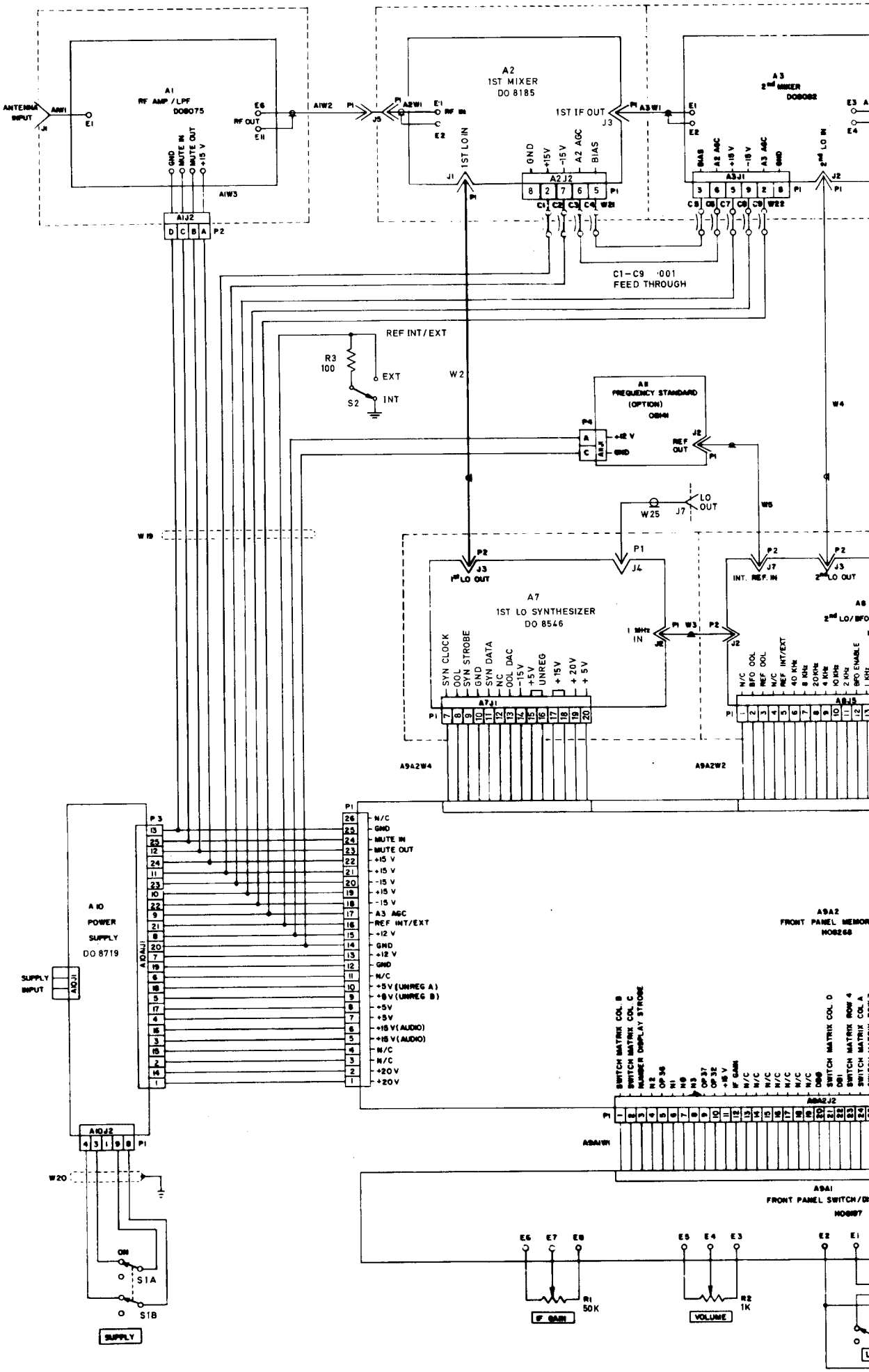


RACAL

TH1496	CO8140 &1
1	

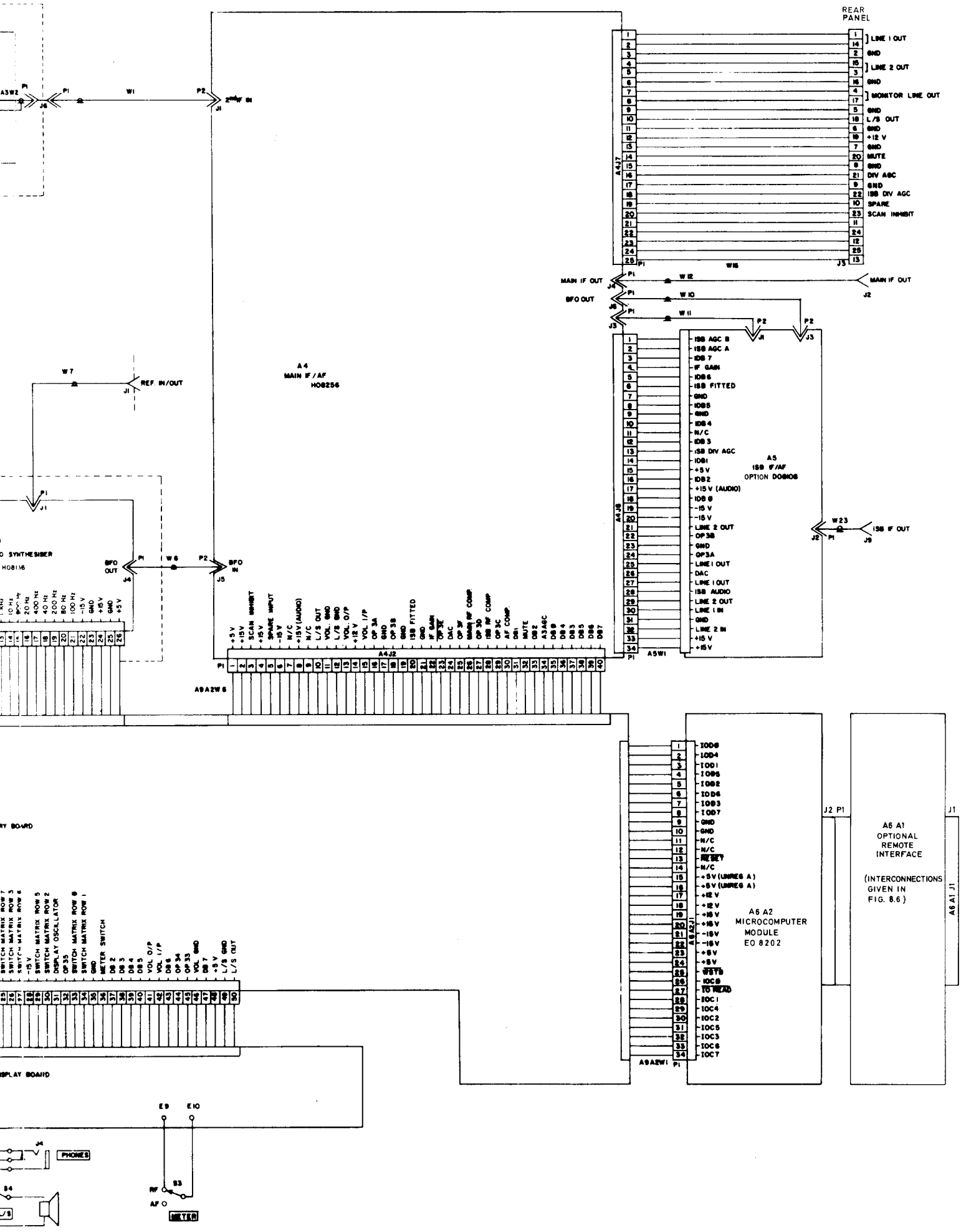
Circuit & Layout: Frequency Standard Module A11

Fig.8.13



RACAL

TH1498	EO8184
2	



Interconnection Diagram Fig. 8.14

ISB IF/AF BOARD A5 (ST08109)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R2	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R3	56k	Metal Oxide	$\frac{1}{4}$	2	909052
R4	12k	Metal Oxide	$\frac{1}{4}$	2	917952
R5	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R6	33k	Metal Oxide	$\frac{1}{4}$	2	910111
R7	2.7k	Metal Oxide	$\frac{1}{4}$	2	916548
R8	560	Metal Oxide	$\frac{1}{4}$	2	917061
R9	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R10	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R11	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R12	1k	Metal Oxide	$\frac{1}{4}$	2	913489
R13	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R14	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R15	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R16	47	Metal Oxide	$\frac{1}{4}$	2	917063
R17	680	Metal Oxide	$\frac{1}{4}$	2	910113
R18	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R19	2k	Variable			938440
R20	220k	Metal Oxide	$\frac{1}{4}$	2	921771
R21	100	Metal Oxide	$\frac{1}{4}$	2	910388
R22	47	Metal Oxide	$\frac{1}{4}$	2	917063
R23	50k	Variable			938441
R24	680	Metal Oxide	$\frac{1}{4}$	2	910113
R25	2.2k	Metal Oxide	$\frac{1}{4}$	2	916546
R26	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R27	4.7k	Metal Oxide	$\frac{1}{4}$	2	913490
R28	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R29	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R30	1k	Metal Oxide	$\frac{1}{4}$	2	913489

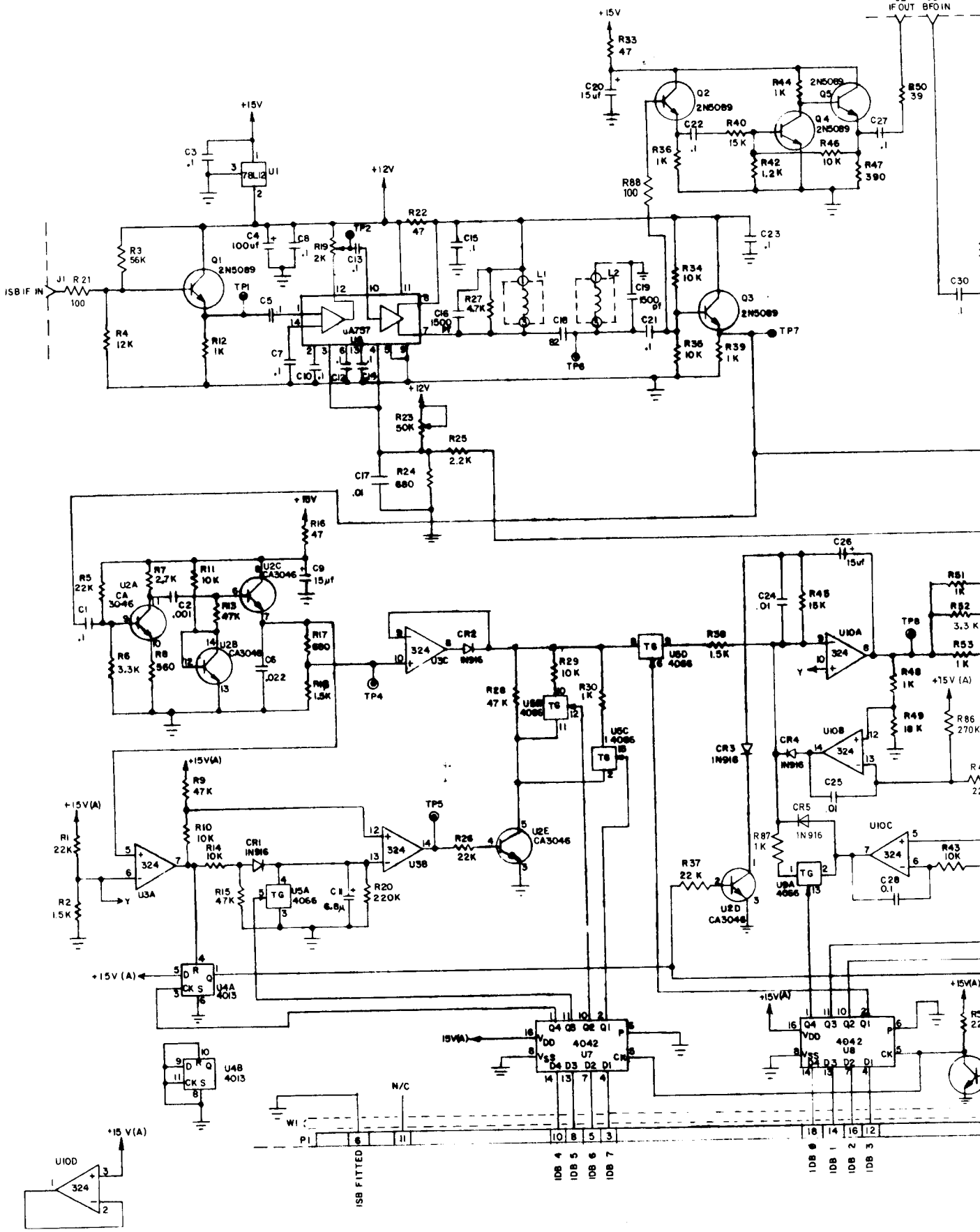
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R31		Not Used			
R32		Not Used			
R33	47	Metal Oxide	¼	2	917063
R34	10k	Metal Oxide	¼	2	914042
R35	10k	Metal Oxide	¼	2	914042
R36	1k	Metal Oxide	¼	2	913489
R37	22k	Metal Oxide	¼	2	913493
R38	1.5k	Metal Oxide	¼	2	911166
R39	1k	Metal Oxide	¼	2	913489
R40	1.5k	Metal Oxide	¼	2	920645
R41	22k	Metal Oxide	¼	2	913493
R42	1.2k	Metal Oxide	¼	2	911179
R43	10k	Metal Oxide	¼	2	914042
R44	1k	Metal Oxide	¼	2	913489
R45	15k	Metal Oxide	¼	2	920645
R46	10k	Metal Oxide	¼	2	914042
R47	390	Metal Oxide	¼	2	916331
R48	1k	Metal Oxide	¼	2	913489
R49	18k	Metal Oxide	¼	2	900994
R50	39	Metal Oxide	¼	2	917062
R51	1k	Metal Oxide	¼	2	913489
R52	3.3k	Metal Oxide	¼	2	910111
R53	1k	Metal Oxide	¼	2	913489
R54	22k	Metal Oxide	¼	2	913493
R55	33k	Metal Oxide	¼	2	913495
R56	10k	Metal Oxide	¼	2	914042
R57	22k	Metal Oxide	¼	2	913493
R58	22k	Metal Oxide	¼	2	913493
R59	1k	Metal Oxide	¼	2	913489
R60	33	Metal Oxide	¼	2	917060
R61	390	Metal Oxide	¼	2	916331
R62		Not Used			
R63	10k	Metal Oxide	¼	2	914042
R64	470	Metal Oxide	¼	2	920758
R65	3.3k	Metal Oxide	¼	2	910111

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R66	3.3k	Metal Oxide	¼	2	910111
R67	3.3k	Metal Oxide	¼	2	910111
R68	1.2k	Metal Oxide	¼	2	911179
R69	3.3k	Metal Oxide	¼	2	910111
R70	27k	Metal Oxide	¼	2	913494
R71	27k	Metal Oxide	¼	2	913494
R72	4.7k	Metal Oxide	¼	2	913490
R73	4.7k	Metal Oxide	¼	2	913490
R74	39k	Metal Oxide	¼	2	900993
R75	68k	Metal Oxide	¼	2	916478
R76	100k	Metal Oxide	¼	2	915190
R77	100k	Metal Oxide	¼	2	915190
R78	4.7k	Metal Oxide	¼	2	913490
R79	8.2k	Metal Oxide	¼	2	918202
R80		Not Used			
R81	2.2k	Metal Oxide	¼	2	916546
R82	33	Metal Oxide	¼	2	917060
R83	22	Metal Oxide	¼	2	920743
R84	33	Metal Oxide	¼	2	917060
R85	10	Metal Oxide	¼	2	909145
R86	270k	Metal Oxide		2	923598
R87	1k	Metal Oxide		2	913489
R88	100	Metal Oxide		2	910388
Capacitors			V		
C1	0.1	Ceramic	50	±20	938406
C2	1000p	Ceramic		20	938408
C3	0.1	Ceramic	50	±20	938406
C4	100	Electrolytic	25		935140
C5	0.1	Ceramic	50	±20	938406
C6	0.022	Ceramic		20	930219
C7	0.1	Ceramic	50	±20	938406
C8	0.1	Ceramic	50	±20	938406
C9	15	Tantalum	20	20	938034
C10	0.1	Ceramic	50	±20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C11	6.8	Tantalum	35	20	938030
C12	0.1	Ceramic	50	+20	938406
C13	0.1	Ceramic	50	±20	938406
C14	0.1	Ceramic	50	±20	938406
C15	0.1	Ceramic	50	±20	938406
C16	1500p	Silver Mica		2	938435
C17	0.01	Ceramic		20	938053
C18	82p	Silver Mica		2	902232
C19	1500p	Silver Mica		2	938435
C20	15	Tantalum	20	20	938034
C21	0.1	Ceramic	50	+20	938406
C22	0.1	Ceramic	50	±20	938406
C23	0.1	Ceramic	50	±20	938406
C24	0.01	Ceramic		±20	938053
C25	0.01	Ceramic		20	938053
C26	15	Tantalum	20	20	938034
C27	0.1	Ceramic	50	+20	938406
C28	0.1	Ceramic	50	±20	938406
C29		Not Used			
C30	0.1	Ceramic	50	±20	938406
C31	0.1	Ceramic	50	+20	938406
C32	6.8	Tantalum	35	±20	938030
C33	0.1	Ceramic	50	+20	938406
C34	0.1	Ceramic	50	±20	938406
C35	0.1	Ceramic	50	±20	938406
C36	0.1	Ceramic	50	+20	938406
C37	0.1	Ceramic	50	±20	938406
C38	6.8	Tantalum	35	±20	938030
C39	6.8	Tantalum	35	20	938030
C40	220	Electrolytic	16		938436
C41	6.8	Tantalum	35	20	938030
C42	6.8	Tantalum	35	20	938030
C43	6.8	Tantalum	35	20	938030
C44	4700p	Ceramic	5		938437
C45	0.1	Ceramic	50	±20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C46	2200p	Ceramic	5		938438
C47	200	Electrolytic	16		938436
C48	68	Tantalum	15		938036
C49	68	Tantalum	15		938036
C50	100	Electrolytic	25		935140
C51	6.8	Tantalum	35	20	938030
C52	470	Electrolytic	25		938439
C53	15	Tantalum	20	20	938034
C54	0.1	Ceramic	50	±20	938406
Diodes					
CR1		IN916			913480
CR2		IN916			913480
CR3		IN916			913480
CR4		IN916			913480
CR5		IN916			913480
CR6		IN916			913480
Transistors					
Q1		Silicon (2N5089)			938417
Q2		Silicon (2N5089)			938417
Q3		Silicon (2N5089)			938417
Q4		Silicon (2N5089)			938417
Q5		Silicon (2N5089)			938417
Q6		Silicon (2N2369)			906842
Q7		Silicon (2N5089)			938417
Q8		Silicon (2N5089)			938417
Q9		Not Fitted			
Integrated Circuits					
U1		78L12			938455
U2		CA3046			922907
U3		324			925944
U4		4013			933644
U5		4066			930148

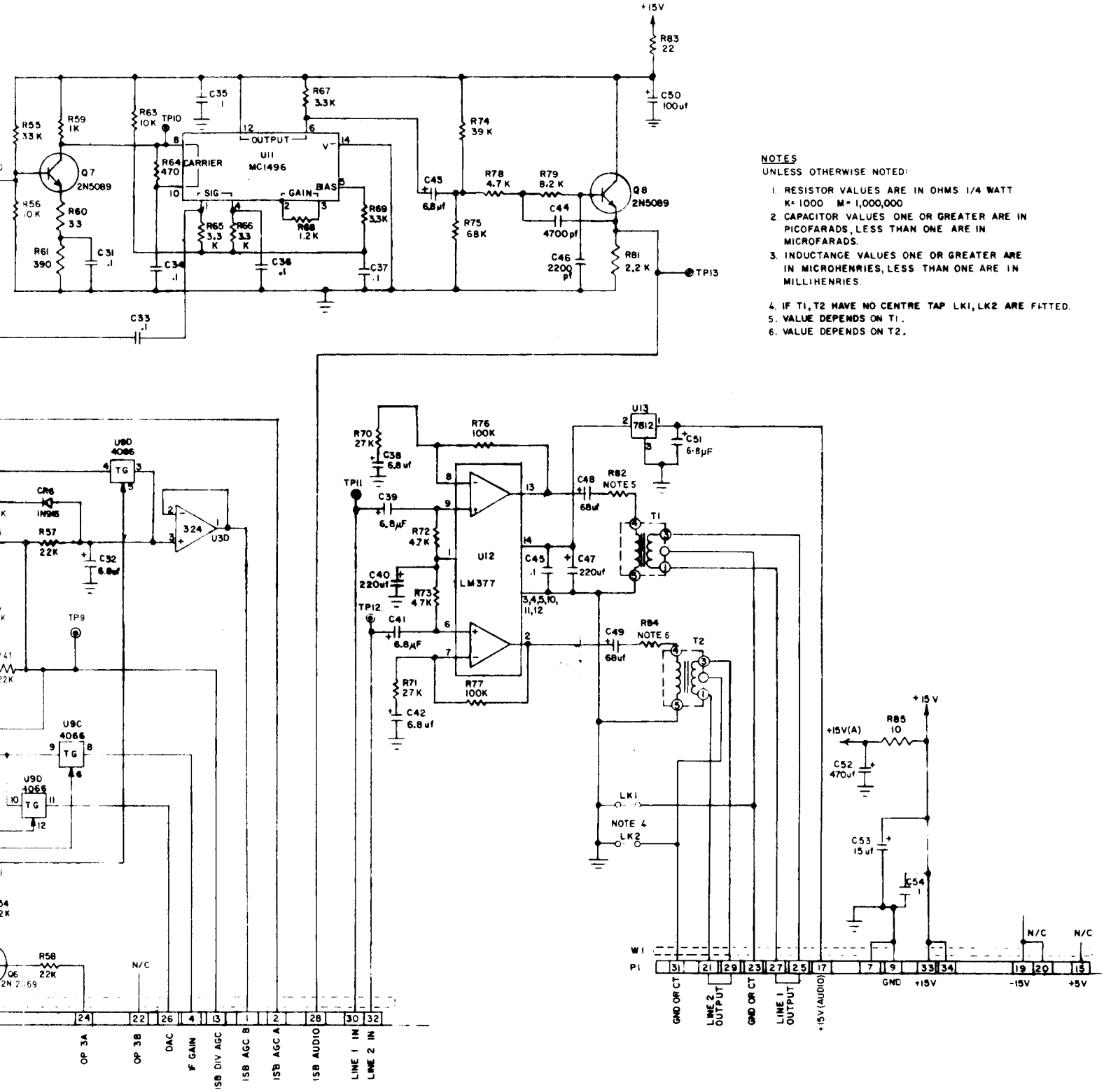
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U6		µA757			938442
U7		4042			938443
U8		4042			938443
U9		4066			930148
U10		324			925944
U11		MC1496P			938427
U12		LM377			928536
U13		7812UC			938455
Transformers					
T1		Assembly (AUDIO)			AT81401
T2		Assembly (AUDIO)			AT81401
Inductors					
L1		Coil RF Variable			AT81400
L2		Coil RF Variable			AT81400
Connectors					
J1		Coaxial RF			938429
J2		Coaxial RF			938429
J3		Coaxial RF			938429



		GND	+15 V(A)
U4	4013	7	14
U7, U8	4042	8	16
U5, U9	4066	7	14
U3, U10	324	11	4

RACAL

TH 1496	D08108
2	



Circuit: ISB IF/AF Module A5 Fig App.1.1

APPENDIX 2

SCORE INTERFACE MODULE

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Text :

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APPENDIX 2

SCORE INTERFACE MODULE

INTRODUCTION

1. The SCORE interface module is an optional internally mounted board which provides for extended or remote control of the receiver using a receiver control unit such as the Racal MA1075. It also allows two receivers, each fitted with a SCORE interface, to be interconnected for space diversity operation. The SCORE (Serial Control of Racal Equipment) control system is described in the following paragraphs.

SCORE FORMAT

2. The SCORE format for serial control is designed to cater for numerous applications and contains ample additional capacity for expansion. It is based on a number of 48-bit synchronous frames, each of which contain a 16-bit preamble (synchronisation, word number identification, etc) followed by a 32-bit data word. The total capacity of the system is sixteen 32-bit data words which is equivalent to approximately 400 separate lines. All sixteen words may be revertively checked.

3. Separate lines are used for both data and clock signals travelling in each direction. These comply with RS422/3, and, over short distances, are compatible with RS232/CCITT V28.

4. The SCORE format for the words used by the RA1792 (word numbers 0,1,2 and 5) is given in table 1. Although word 0 may be sent as part of a control data sequence, it does not contain any control information and is used only for revertive data.

ROUTINE AND NEW DATA

5. Under static conditions, i.e. when the control data being transferred from control unit to receiver does not contain change-of-function information, 'routine data' frames are sent in numerical sequence, and at a rate determined by the clock frequency. When a change of function is made however, instead of allowing the transfer of the full sequence of frames to occur before the change of function is executed at the receiver, the next frame to be sent will contain the data word carrying the change of function information. Thus the frames are sent out of sequence and priority is given to those frames containing new data. This is achieved under software control where a flag is set each time a control setting is changed to indicate that the appropriate word requires transmission. The flag is reset when the data word is transmitted.

FRAME COMPARISON

6. Error detection is accomplished by use of the frame comparison technique, which means that two identical frames must be received at the receiver before a change of function can occur. An exception to this is made for the frequency frame (containing word 1), which may be sent singly (new data frames only) by inclusion of external links.

PREAMBLE

7. A 16-bit preamble is added to each 32-bit data word to form one complete 48-bit frame. The preamble contains a 6-bit sync. code, a 2-bit transmit-receive (PTT) code, a control inhibit bit, a return monitor bit, a 2-bit address word security code and a 4-bit data word ident; these are described in the following paragraphs.

Sync. Code

8. The sync. code (bits 0 to 5) consists of a '0' followed by five consecutive '1's. The maximum number of consecutive '1's to occur in serial BCD data is four, e.g. BCD seven followed by BCD eight. This then makes five '1's a unique code. For added security, the next two bits of the preamble (used for PTT) may not consist of two consecutive '1's. This is done to 'terminate' the sync. code and to prevent the generation of a false sync. code following a line break etc.

Transmit/Receive

9. Bits 6 and 7 of the preamble are used for transmit/receive switching (PTT) where the transmit state mutes the receiver and may also set an associated transmitter to the transmit condition. As mentioned in para.8, these two bits must not consist of consecutive '1's. For the transmit state, bit 6 is set to a '1' and bit 7 is set to '0', whilst for the receive state, bit 6 is set to '0' and bit 7 is set to '1'.

Control Inhibit Bit

10. This bit of the preamble (bit 8) is used, as the name implies, to inhibit control of the receiver via the serial control data. When it is set to a '1', the control settings of the receiver remain unchanged and further control instructions conveyed by the 32-bit data words are ignored. The revertive data however, is returned in the normal way, i.e. the receiver settings are returned.

Return Monitor Bit

11. The return monitor bit is normally set to '0' and is only set to '1' to give continuous revertive monitor when single frequency frames are being sent from the control unit (para.6).

TABLE 1: SCORE Data Format

	BIT No	BIT FUNCTION OR FORCED STATE	MONITOR (0)	FREQUENCY (1)	ANALOGUE (2)	HF MODE (5)
PREAMBLE	0	0 |				
	1	1 |				
	2	1 | SYNC				
	3	1 | CODE				
	4	1 |				
	5	1 |				
	6	TRANSMIT				
	7	RECEIVE				
	8	CONTROL INHIBIT				
	9	RETURN MONITOR				
	10	ADDRESS	0	0	0	0
	11	EQUIPMENT	0	0	0	0
	12	1 | DATA	0	1	0	1
	13	2 | WORD	0	0	1	0
	14	3 | IDENT	0	0	0	1
	15	4 |	0	0	0	0
DATA WORD	16		A | USER	1 | 1Hz	1 | BFO	0 | NOT
	17		B | FUNCTION	2 |	2 |	0 | USED
	18		C |	4 |	4 | x 10 Hz	0 |
	19		D |	8 |	8 |	0 |
	20		0 |	1 |	1 |	0
	21		0 |	2 | 10 Hz	2 | BFO	0
	22		0 |	4 |	4 | x 100 Hz	0
	23		0 |	8 |	8 |	0
	24		0 | NOT	1 |	1 | BFO	0
	25		0 | USED	2 |	2 | xkHz	0
	26		0 |	4 | 100 Hz	4 |	0
	27		0 |	8 |	BFO SIGN	0
	28		0 |	1 |	0 |	1 | MODE
	29		0 |	2 |	0 |	2 |
	30		0 |	4 | kHz	0 |	4 |
	31		0 |	8 |	0 |	0
	32		MUTE	1 |	0 | NOT	SYMMETRICAL
	33		FAULT	2 |	0 | USED	0
	34		FC ERROR	4 | 10 kHz	0 |	0
	35		0	8 |	0 |	0
	36		RF METER	1 |	0 |	AGC DUMP
	37		0 |	2 |	0 |	1 |
	38		0 | NOT	4 | 100 kHz	0 |	2 | AGC
	39		0 | USED	8 |	1 |	4 |
	40		1 |	1 |	2 |	1 |
	41		2 |	2 |	4 | IF	2 | BANDWIDTH
	42		4 |	4 | MHz	8 | GAIN	4 |
	43		0 | METER	8 |	0 |	0
	44		8 | READING	1 | 10 MHz	16 |	W |
	45		16 |	2 |	32 |	X | USER
	46		32 |	1 | SINGLE FRAME	64 |	Y | FUNCTION
	47		64 |	2 | CHECK BITS	128 |	Z |

Address Security Code

12. Bits 10 and 11 of the preamble are used in words 8 and 9 of the SCORE control system (equipment and operator addressing words respectively) to provide added security against incorrect addressing. These two bits are set to '0' in all words used by the RA1792 (and the MA1075).

Data Word Ident

13. The last four bits of the preamble (bits 12 to 15) are used for the data word identification code, in binary format, i.e. 0 to 15 (decimal) or 0 to F (hexadecimal).

DATA WORDS

14. As stated in para.4, words 0,1,2 and 5 are used by the RA1792. These are described in the following paragraphs which should be read in conjunction with table 1. Certain words contain a number of 'forced zeros' to prevent the possible occurrence of five consecutive '1's which would otherwise be mistaken for a sync. code.

WORD 0 - MONITOR

15. This word is used for revertive signalling only; although it may be transmitted as part of a forward control data sequence, it does not contain any control data.

User Functions

16. The first four bits of data word 0 provide for the revertive user functions where up to four earth (0V) signals applied to the receiver are reproduced at rear panel connections of the control unit. The four bits are labelled A,B,C and D, and correspond with the A,B,C and D connections at both the receiver and control unit.

Revertive Indications

17. The next operative bits of word 0 are bits 32, 33 and 34. Bit 32 is set to a '1' when a mute signal is applied to the receiver, and this is conveyed to the control unit via the revertive data to illuminate the MUTE indicator on the control unit front panel. Data bit 33 (the fault bit) is set to a '1' following a fault condition in the synthesizer section of the RA1792 receiver, and this condition is conveyed to the control unit via the revertive data to illuminate the FAULT indicator on the control unit front panel. Data bit 34 is the frame comparison error bit and is normally at '0'; it goes to a '1' when three consecutive frame comparison errors are detected at the receiver, and this also results in the illumination of the FAULT indicator.

RF Metering

18. Data bit 36 is set to a '1' to select RF metering, and the RF meter reading data is conveyed, in 7-bit digital format, via data bits 40 to 42 and 44 to 47 (bit 43 is a forced zero).

WORD 1 - FREQUENCY

19. The first 30 bits of this word (16 to 45 inclusive) contain the frequency setting information in BCD format. The remaining two bits (46 and 47) determine whether frame comparison is required (for error detection), in which case each frame is sent twice, or whether single frequency frames are to be sent.

WORD 2 - ANALOGUE

20. Word 2 contains the analogue functions, BFO and IF gain. For a receiver set for local control, the range of the BFO is between plus 8 kHz and minus 8 kHz (centred on 455 kHz). For remote control however, the maximum offset is restricted to the range plus and minus 7.79 kHz i.e. three data bits (24, 25 and 26) are used for the kHz digit (giving a maximum figure of 7), and to prevent the generation of a spurious sync. code, data bit 23 must not be set to a '1' (thus giving a maximum figure of 7 for the 100 Hz digit). Data bit 27 is the BFO sign bit and is set to a '1' for negative BFO offset frequencies, to a '0' for positive BFO offset frequencies.

21. The receiver manual IF gain control data is conveyed between control unit and receiver via data bits 39 to 42 and 44 to 47 (bit 43 in a forced zero). This gain control data is not however, transferred from master receiver to slave receiver when two receivers are interconnected for space diversity operation. In this case the receiver diversity AGC outputs are interconnected.

WORD 5 - HF MODE

22. This word is used for mode, AGC and bandwidth selection, and for the forward user functions.

Mode

23. Bits 28 to 32 inclusive are concerned with mode selection. The state of bit 32 determines whether a symmetrical mode or a sideband mode is selected, as shown in the following table.

BCD coding of Bits 28 to 31	Bit 32 State	Mode Selected	
1	1	AM	
2	1	CW	Symmetrical
5	1	FM	
0	0	USB	
1	0	LSB	Sideband
2	0	ISB-U	
3	0	ISB-L	

AGC

24. Bit 36 is used for AGC dump; when set to a '1' it causes a rapid decay of the AGC voltage level so that the level may be re-established for the signal being received. The coding of bits 37,38 and 39 in given below.

BCD Code	Function
0	Manual and short
1	Manual and medium
2	Manual and long
3	Manual only
4	Short
5	Medium
6	Long
7	Not allowed

Bandwidth

25. The coding of bits 40 to 42 is given below. The actual filters fitted are dependent upon the particular receiver options. The filter numbers given correspond with those on the receiver main IF/AF board.

BCD Code	Filter No.
0	Not used
1	Not used
2	3 (Narrowest Bandwidth)
3	4
4	5*
5	6
6	7
7	Not used

* May select filter 2 if offset sideband filter.

User Functions

26. The last four bits of word 5 provide for the forward user functions where up to four earth (0V) signals applied to the receiver control unit are reproduced at rear panel connections on the RA1792 receiver. The four bits are labelled W, X, Y and Z and correspond with the similarly marked input and output connections of the control unit and receiver respectively.

REVERTIVE DATA

27. The format of the revertive data is the same as for the control data. Frame comparison however, does not take place, and the revertive data is generally sent in single frames.

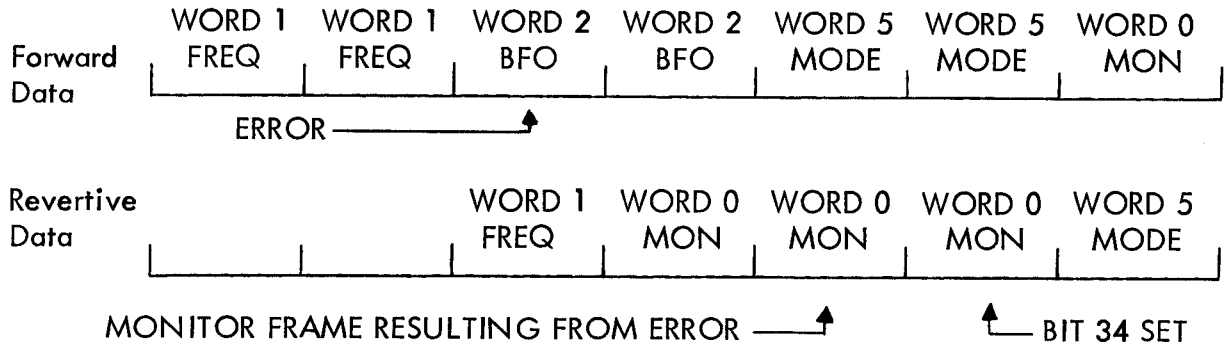
28. Provided that the control inhibit and return monitor bits of the forward data preamble are not set to a '1', that single frequency frames are not being sent, and that no errors occur in the control data, then the form of the revertive data is given by the following example.

Forward Data	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 1 FREQ	WORD 2 BFO	WORD 2 BFO	WORD 5 MODE
Resulting Revertive Data		WORD 0 MON	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 0 MON	WORD 2 BFO

29. In this example, the forward data consists of two word 0 frames, two word 1 frames, to word 2 frames and the first of two word 5 frames. Since two frames have to be sent and compared before any action can take place, the revertive data resulting from the forward data given in this example is shown lagging the forward data by two 48-bit frames (ignore for the moment the first revertive data word 0). The two forward data word 0 frames are compared; since no bit errors are present, the two frames are identical and a word 0 frame is returned. The next frame comparison however, is between a word 0 and a word 1. The comparison is therefore unsuccessful, and, although an error does not exist, it is arranged to send back a word 0 monitor frame. Two word 1 frames are now compared, and result in a revertive word 1 frame. The next comparison is between a word 1 frame and a word 2 frame, which results in a revertive word 0 frame, two word 2 frames result in a revertive word 2 frame, and so on. The control of the first (blank) revertive data frame is dependent on the previously sent data, whilst the next frame (the first word 0 frame in this example) must be a word 0 frame due to a comparison between two disimilar frames. Note that when two RA1792 receivers are interconnected for master/slave operation, word 0 control data frames are not sent by the master receiver.

Frame Comparison Error

30. A frame comparison error signal is generated only on the failure of three consecutive frame comparisons, as shown in the following example:



31. In this example the forward data consists of two word 1 frames, two word 2 frames, two word 5 frames and the first of a pair of word 0 frames. The two frequency word frames result in a revertive frequency word frame and the next two frames (frequency and BFO) result in a monitor word 0 frame. The two BFO word frames are compared, and this time, due to an error, the frame comparison is unsuccessful, resulting in a further revertive monitor frame. The next two frames (BFO and mode) being disimilar also result in a revertive monitor frame. Thus three consecutive revertive monitor frames result following the FAILURE of three consecutive frame comparisons; a frame comparison error signal is generated and this is conveyed by bit 34 of the revertive word 0 frame.

Control Inhibit

32. If the control inhibit bit (bit 8 of the preamble) in a forward control data frame is set to a '1', and provided that the return monitor bit (bit 9 of the preamble) is not set to a '1', then the revertive data frames are sent in pairs and in numerical sequence and convey the actual receiver setting data.

Return Monitor

33. If the return monitor bit (bit 9 of the preamble) in a series of forward control data frames is set to a '1', then the revertive data consists of a series of continuous monitor frames.

CLOCK CIRCUITS

34. These provide the timing signals required by the various parts of the system. The basic data rate clock signal may be generated either by an external unit, such as the receiver control unit or a modem, or may be provided by an internal clock generator (approximately 6 kHz).

SIGNAL-TO-LINE REQUIREMENTS

35. The RA1792 receiver signal-to-line requirements for the serial data and clock signals comply with EIA standards RS-422 and RS-423. The SCORE clock and data output drivers are configured for RS-422, a differential balanced voltage interface which is fully compatible with CCITT recommendations V11 and X27. The maximum permissable line length is dependent on factors such as data signalling (clock) rate, tolerable signal distortion and noise interference. In general, the maximum line length at a data signalling rate of 100 k bauds is 1200 metres (4000 ft), reducing to approximately 15 metres (50 ft) at the maximum data signalling rate of 10M bauds. Note however, that the maximum data signalling rate for the RA1792/MA1075 is 9.6k bauds. If no connection is made to the RS-422 positive output, a single ended interface suitable to drive an RS-232 receiver is produced, provided the line length does not exceed 15 metres (50 ft).

36. The line receivers used for the SCORE clock and data input signals comply with EIA standards RS-422 (balanced voltage interface) and RS-423 (unbalanced voltage interface). When connected for an unbalanced transmission line (positive input terminal grounded), the circuit may be driven from a single-ended RS-232 driver circuit provided the line voltages do not exceed plus and minus 12 V. A comparison of the specifications for EIA standards RS-232, RS-422 and RS-423 (as far as the RA1792 is concerned) is given in table 2, and the noise immunity figures for mixed single-ended interfaces are given in table 2.

Table 2: Comparison of Specifications

CHARACTERISTIC	RS-232C (CCITT V28)	RS-423	RS-422
Mode	Single Ended	Single Ended	Differential
Logic '1' (OFF State)	Negative Voltage	Negative Voltage	Negative Voltage
Logic '1' (ON State)	Positive Voltage	Positive Voltage	Positive Voltage
Maximum Line Length	15 m (50 ft) at 20 k Bauds	1200 m (4000 ft) at 3k Bauds	1200 m (4000 ft) at 100 k Bauds
Maximum Data Rate	20 k Bauds	300 k Bauds	1 M Bauds
Open Circuit Driver Voltage (maximum)	±25 V	±6 V	6 V differential
Loaded Driver Voltage (minimum)	±5 V to ±15 V	±3.6 V	2 V differential
Driver Output Load - Power Off	300 ohms	100 µA (-6 V to +6 V)	100 µA 6 V to 0.25 V
Driver Short - Circuit Current	±500 mA	±150 mA	±150 mA
Driver Slew Rate	30 V/µ second	Capacitor controlled	No restriction
Receiver Input Resistance	3 k ohms to	Equal to or greater than 4k ohms	Equal to or greater than 4k ohms
Receiver Threshold	-3 V to +3 V	-0.2 V to +0.2 V	-0.2 V to +0.2 V
Maximum Receiver Input Voltage	±25 V	±12 V	±12 V

Table 3: Noise Immunity

DRIVER	RECEIVER	NOISE IMMUNITY (MINIMUM)
RS-232C	RS-232C	2 V
RS-423	RS-423	3.4 V
RS-232C	RS-423	4.8 V
RS-423	RS-232C	0.6 V

37. The remaining external input and output connections to and from the SCORE interface conform to a common convention. Logic input signals are defined as follows:

Logic '1' - ON state: Steady state short-circuit current to 0V, less than 40 mA.
Logic '0' - OFF state: Internally pulled up to a positive voltage, usually +12 V (for C-MOS).

38. Logic output signals are defined as follows:

Logic '1' - ON state: represented by a short circuit to 0V via a current - saturated open-collector transistor.
Logic '0' - OFF state: represented by the open-circuit output from a transistor in the cut-off condition i.e. the externally applied open-collector pull-up voltage (up to +20 V).

INSTALLATION

39. Detailed installation information is beyond the scope of this appendix and reference should be made to the appropriate system manual. Typical interconnection diagrams are however given for a space diversity installation using a pair of RA1792 receivers (fig. App.2.1) and for a remote control installation using the MA1075 receiver control unit (fig. App.2.2).

SCORE INTERFACE BOARD

FUNCTIONAL DESCRIPTION

40. The following functional description should be read in conjunction with the block diagram of the SCORE interface board given in fig. App.2.3. When the unit is switched on, the initialisation routine resets the receive interrupt latch (/IO READ, IOC3 and IOC7 applied to the address decoder), resets the transmit interrupt latch (I/O port 1 bit 1) and enables the receive and transmit interrupt circuitry (via PIO port 84, bits 6 and 7).

SCORE Receiver

41. Inverted SCORE control data (from another RA1792 receiver or a receiver control unit) is clocked into a sync. code detector and, via an inverter, to an 8-bit serial in/ parallel and serial out shift register. When a correct inverted sync. code is detected, a strobe pulse is generated which is applied to:

    (1) the reset input of an 8-bit counter.

    (2) the strobe input of the shift register; the data in each shift register stage is transferred to a storage register and will appear at the parallel outputs when a '1' is applied to the enable input.

    (3) the set input of the receive interrupt latch; the output changes to a '1' and this causes the peripheral input/output (PIO) device to generate an interrupt signal which is routed to the microcomputer (via the control bus).

42. The microcomputer examines the receive and transmit interrupt pending lines, decides that a receive interrupt has occurred, and then applies address 88 (IOC3 and IOC7), together with the /IO READ Signal to the address decoder. The resulting '1' output resets the receive interrupt latch and enables the 8-bit shift register to route the first 8 bits of the received frame (bits 0 to 7 of the preamble) to the microcomputer via the processor data bus.

43. Successive bytes of received SCORE control data are transferred in a similar manner except that the strobe pulses are produced by the 8-bit counter instead of the sync. code detector i.e. the Q4 output from the 8-bit counter is applied to the set input of the strobe pulse generator, and reset is applied after the CR time constant.

44. The serial control data output from the shift register (delayed by eight clock periods) is routed via an inverter to a rear panel socket (Data out external) for connection to an external unit using the SCORE exta word facility (see fig.App.21(a)).

SCORE Transmitter

45. The SCORE transmit shift register receives parallel SCORE data frames (words 0, 1, 2 and 5) from the microcomputer (I/O port 0) or serial data frames (external revertive data from an external unit using the extra word facility) and transmits this SCORE data in serial form. For a remote control installation, revertive data resulting from received control data is transmitted back to the receiver control unit, whilst for the master/slave situation using a pair of RA1792 receivers, the forward control data is transmitted from the control receiver to the slave receiver, or revertive data from the slave receiver is transmitted back to the master receiver.

46. At the end of the last but one byte of a SCORE data frame handled by the SCORE receiver, the microcomputer applies a start-in-sync. set pulse to the timing and control circuitry of the SCORE transmitter. This causes the generation of a load pulse which is used to produce the following:

(1) A clock signal for the transmit interrupt latch; the '0' at the D input results in a '1' at the $\overline{Q}$ output which is routed to the interrupt control circuit and via an inverter to the microcomputer (I/O port 1).

(2) The parallel/serial control signal for the output shift register; if the next SCORE frame to be transmitted contains word 0, 1, 2 or 5, then the microcomputer sets line 6 of PIO port 85 to a '1' and the output shift register is set to receive parallel data from the microcomputer. If however, the next frame to be transmitted does not contain a word used by the receiver, then the output shift register is set to receive external serial revertive data (from an external unit using the extra word facility).

(3) A reset signal for an 8-bit counter. This reset signal is maintained until the end of the next load pulse (which is produced by the Q4 output signal from the SCORE receiver 8-bit counter). The two 8-bit counters are then synchronised and successive load pulses are then produced by the SCORE transmitter 8-bit counter. Counter synchronisation becomes relevant should gaps occur during successive received data frames (para. 62).

47. The Q4 output from the 8-bit counter is also applied to the clock input of the external strobe pulse generator. The D input of this stage is controlled by the microcomputer and is only set to a '1' following successful frame comparison of the received SCORE data. The external strobe pulse is then produced and is applied to the external extra word unit to enable the revertive data output.

SCORE Data Input and Output Timing

48. Fig. App.2(a) shows a typical situation where an RA1792 receiver is controlled by an MA 1075 control unit, and an extra-word control unit (using SCORE word 7) connected to the MA1075 controls an external unit connected to the RA1792. Pairs of SCORE control data frames containing words 0, 1, 2 and 5 are produced by the MA1075, and pairs of word 7 frames are inserted into the control data stream from the MA1075 on request by the extra word control unit. The revertive data from the SCORE word 7 controlled unit consists of 40-bit words from bit 8 to bit 47 i.e. the sync code (bits 0 to 7) is not included.

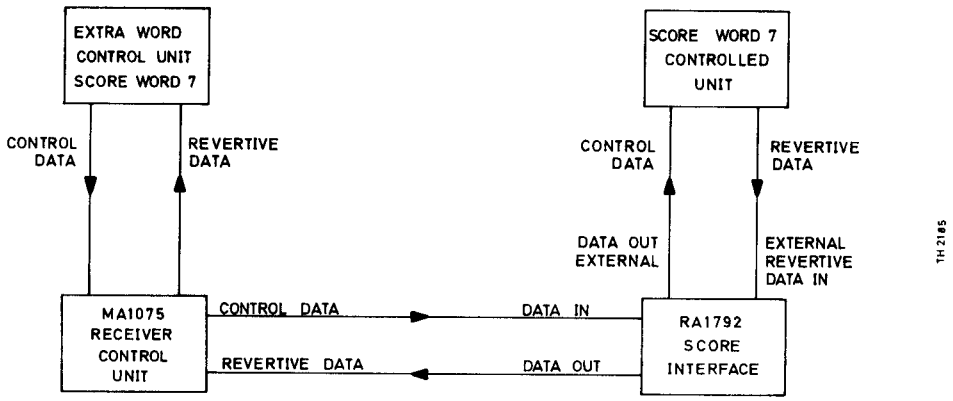


Fig. App. 2 (a) SCORE Data Routing

49. The timing diagram given in fig.App.2.(b) relates to fig.App.2(a) and shows the SCORE data input and output timing as far as the RA1792 SCORE interface is concerned. The DATA IN comprises a pair of word 7 frames (originating from the extra word control unit), two word 1 and two word 2 frames (from the MA1075), two further word 7 frames, and the first of a pair of word 5 frames (from the MA1075). This data is clocked into an 8-bit shift register and is then applied to the microcomputer in parallel bytes. It is also clocked out of the register in serial form for application to the SCORE word 7 controlled unit (DATA OUT EXTERNAL), delayed by eight clock periods due to the action of the shift register.

50. The microcomputer frame-compares the first word 7 frame with the last frame received, and since the two frames do not compare, a SCORE word 0 revertive data frame is produced (DATA OUT). The data content of the first DATA OUT frame shown in fig.App.2(b), marked X, is the result of the previous frame comparison. The next frame comparison undertaken by the microcomputer is between two word 7 frames, and in this example, successful frame comparison is assumed (if the comparison had failed, a further revertive word 0 frame (DATA OUT) would have been produced).

51. The microcomputer also examines the word identification bits of each DATA IN frame. Following the successful frame comparison between a pair of frames not used by the RA1792 i.e. the word 7 frames in this example, a sync. code is loaded into the SCORE transmit output shift register, and the register is then set to allow a serial input. The external strobe pulse is then produced and applied to the SCORE word 7 controlled unit. This responds by applying the revertive 40-bit word 7 data to the SCORE interface where it is clocked into and straight out of the SCORE transmit output shift register, preceded by the sync. code inserted by the microcomputer. This revertive word 7 frame is then routed via the MA1075 to the extra word control unit.

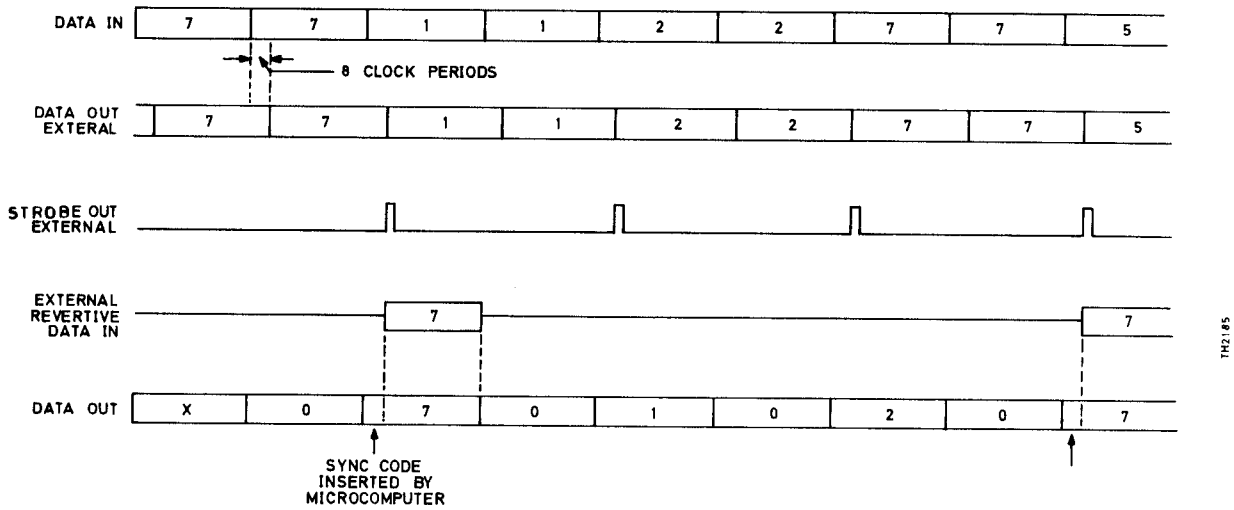


Fig. App. 2(b) Timing Diagram : SCORE Data

52. The next frame comparison takes place between a word 7 frame and a word 1 frame, and this results in a revertive (DATA OUT) word 0 frame. Two word 1 frames are then successfully compared, a word 1 frame is returned, and an external strobe pulse is generated. This pulse is applied to the SCORE word 7 controlled unit but because a further pair of word 7 frames have not been received, no revertive data is available and the strobe pulse has no effect.

User Functions

53. The input and output user functions are handled by a peripheral input/output (PIO) device which interfaces to the microcomputer via two high-speed I/O ports, designated 84 and 85, and a control bus. The frame comparison inhibit input is also routed to the microcomputer via I/O port 85 (bit 7).

CIRCUIT DESCRIPTION (fig. App. 2.4)

SCORE RECEIVER

Sync. Code Detector

54. The inverted SCORE input data (RS-423 or RS-232) is applied via a line receiver, U3A, to the D input of a 4-bit shift register U13B, and via inverter U14D to the D input of an 8-bit shift register U23 (para 57). The Q3 output of U13B is applied to the reset input of a further 4-bit shift register U13A, where the D input is connected to +5V (logic '1'). Data is shifted into these registers on the positive-going transition of the SCORE clock signal from line receiver U3B.

55. When an inverted sync. code is received i.e.1-0-0-0-0-0-X-X, it takes three clock pulses for the first '1' to reach the Q3 output of U13B; this holds U13A in the reset state for the duration of the next clock pulse, and a further four clock pulses are required before the Q4 output of U13A changes to a '1' (table 4). Thus the Q4 output of

Table 4: Sync. Code Detector

SHIFT REGISTER STATES		1	2	3	4	5	6	7	8
U13B	Q 1	1	0	0	0	0	0	X	X
	Q 2	X	1	0	0	0	0	0	X
	Q 3	X	X	1	0	0	0	0	0
	Q 4	X	X	0	1	0	0	0	0
U13A	Q 1	X	X	0	0	1	1	1	1
	Q 2	X	X	0	0	0	1	1	1
	Q 3	0	X	0	0	0	0	1	1
	Q 4	0	0	0	0	0	0	0	1

X = 0 or 1

U13A can only change to a '1' following the occurrence of five consecutive zeros at the D input of U13B. This circuit does not detect the state of the last two bits of the received sync-code but this is subsequently checked by the system software. The '1' at the Q4 output of U13A is applied to the clock input of the strobe pulse generator U10A via glitch suppression components R2, C8.

Strobe Pulse Generator

56. The strobe pulse generator comprises D-type flip-flop U10A. When clocked by the output from the sync. code detector, the '1' at the D input is transferred to the Q output, and reset is applied after the time constant presented by R1 and C7. The nominal 5 microsecond positive-going output pulse is applied to:

(1) the set input of the receiver interrupt latch U10B; the resulting '1' at the Q output is applied to NAND gate U15A of the interrupt control circuit (para 64), and via inverting buffer U14A to the microcomputer as the receive interrupt pending signal.

(2) the strobe input of the 8-bit shift register U23 to load the internal storage latches with the first eight bits (the sync. code) of the received frame (para. 57).

(3) the reset input of an 8-bit counter U11A; this counter produces a positive-going pulse at the Q4 output for every eight SCORE clock cycles following reset, and these pulses are applied to the set input of U10A to produce the strobe pulses for the remaining five bytes of the received data frame. The Q4 output of ML11A is also routed to NAND gate U16A which forms part of the output counter synchronisation circuit (para. 59).

Input Shift Register

57. U23 is an 8-stage serial shift register having a storage latch associated with each stage. The data in each shift register stage is transferred to the storage register when a '1' is applied to the strobe input, and the stored data appears at the Q1 to Q8 parallel outputs when a '1' is present at the enable input. When a '0' is present at the enable input, the Q1 to Q8 outputs are in the high-impedance 3-state condition. The serial output is taken from the Q's pin (where it appears eight clock periods after application to the D input) and is routed to J1 pin 2 via open-collector inverter Q5.

Address Decoder

58. The address decoder makes use of three transmission gates (analogue switches) U21D, U21B and U21C. For a SCORE read operation, the microcomputer sets the IOC3 and IOC7 control bus lines to a '1' and the I/O read line to a '0'. U21D is thus held off, U21B and U21C are turned on, and a '1' from R16 is applied to the enable input of the 8-bit shift register U23, and the parallel data at the Q1 to Q8 output pins is applied to the microcomputer via the processor data bus. The '1' from U21C is also applied to the reset input of the receive interrupt latch U10B, the Q output is reset to '0', and the receive interrupt is cancelled.

SCORE TRANSMITTER

Start-in-Sync. Latch

59. The start-in-sync. latch U22A is reset by the microcomputer during the initialisation routine (I/O port 1 bit 0) and is set by the microcomputer shortly after the start of the last byte of a SCORE data frame handled by the SCORE receiver (I/O port 1 bit 3). The $\overline{Q}$ output of U22A is thus set to a '0', this is routed to NAND gate U16B and the '1' output resets the 8-bit counter U11B. At the same time the Q output of U22A is set to the '1'; the combination of this and the next positive-going pulse from the SCORE receive 8-bit counter U11A (at the end of the last byte of a received data frame - see timing diagram fig. App.2(c)), results in a '0' at the output of NAND gate U16A. This is inverted by NAND gate U16D and a '1' is applied to the set input of the load pulse generator U17B.

Load Pulse Generator

60. The load pulse generator U17B is set either by the action of the start-in-sync. latch (as described in para.59) or subsequently by the Q4 output of the 8-bit counter (via U14E and U16D). In either case, U17B is effectively reset by the next negative-going transition of the SCORE clock, which is applied via inverter U14B (D input at 0V), and thus the positive and negative-going pulses at the Q and $\overline{Q}$ outputs extend for one half of a SCORE clock period.

61. With reference to the timing diagram given in fig. App.2(c), the first and last load pulses shown (U17B outputs) result following the Q4 output of the 8-bit counter U11B. The positive-going pulse at the Q output of U17B is applied to the clock input of the internal/external latch U17A (para.66) and also to the clock input of the start-in-sync. latch U22A; this however, has no effect as the Q output of U22A is already at logic '0'. The negative-going pulse at the $\overline{Q}$ output of U17B is inverted by U16B to reset the 8-bit counter U11B. It is also applied to NAND gate U16C, which forms part of the parallel/serial selection circuit for the output shift register (para.66), and to the clock input of the transmit interrupt latch U22B. Thus at the positive-going transition of the negative-going pulse, the '0' at the D input of U22B results in a '1' at $\overline{Q}$ output; this is routed to the microcomputer via inverter U14F as a transmit interrupt pending signal, and is also applied to NAND gate U15D which forms part of the interrupt control circuitry (para.64). The positive-going transition of the negative-going pulse from the $\overline{Q}$ output of U17B is also used to clock the output enable latch U12B (para.68).

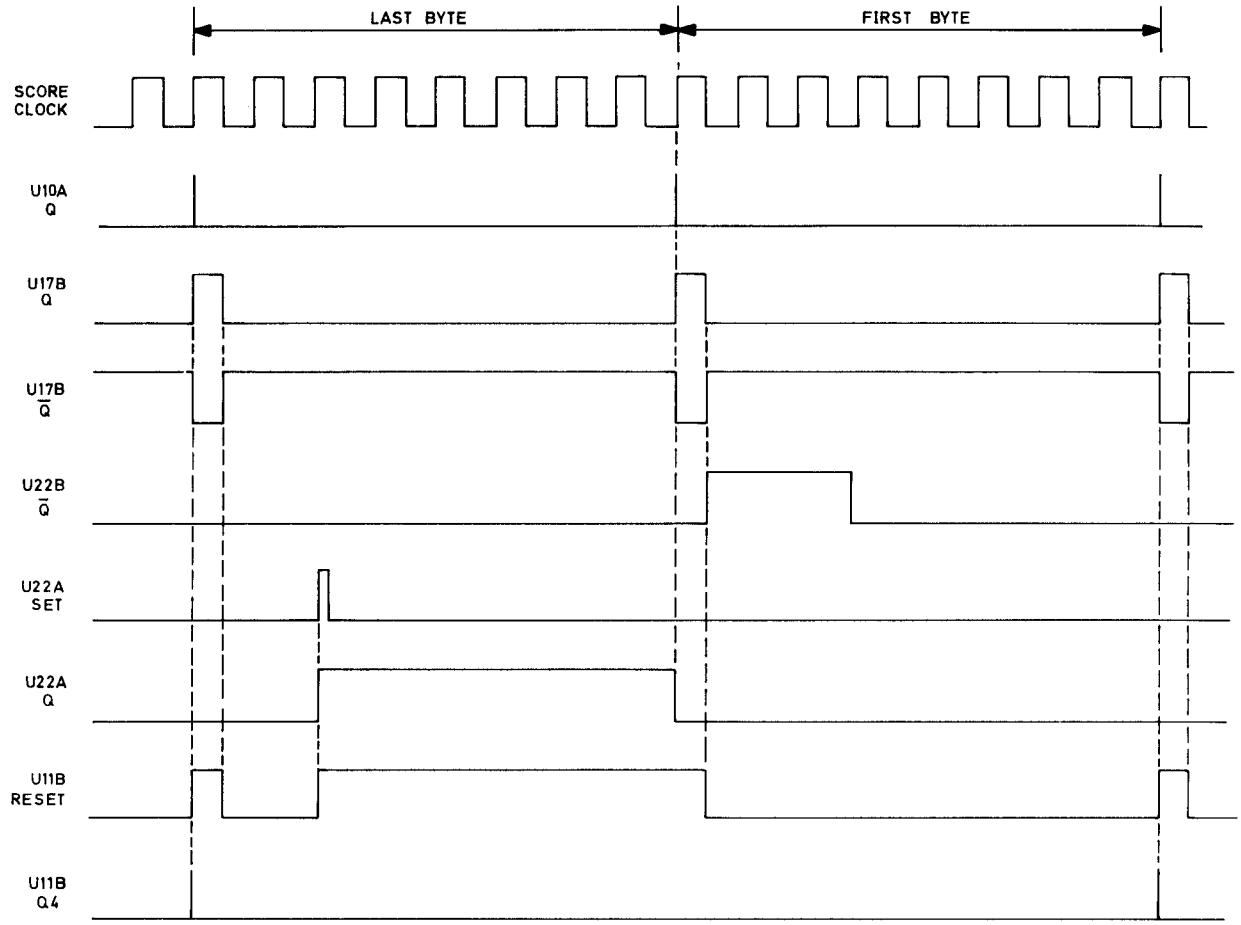


Fig. App. 2(c) Timing Diagram : Counter Synchronisation

62. The second load pulse shown in fig.App.2(c) results from the combination of a '1' at the Q output of the start-in-sync latch U22A and the positive-going output pulse from the 8-bit counter U11A. This time, the positive-going pulse at the Q output of U17B clocks the internal/external latch U17A as before, but also clocks the start-in-sync. latch U22A. The '0' at the D input is transferred to the Q output, is inverted by U16A, and a '1' is thus applied to U16D to allow load pulse generation by the Q4 output signals from the 8-bit counter U11B (applied to the set input of U17B via U14E and U16D). The negative-going pulse at the $\overline{Q}$ output of U17B extends the reset period of U11B for the duration of the pulse and then allows counting to commence so that the first Q4 output pulse from U11B occurs exactly eight SCORE clock periods after the previous Q4 output pulse from 8-bit counter U11A, i.e. synchronism between the two 8-bit counters is established.

63. Synchronisation between the two 8-bit counters is necessary due to the asynchronous nature of the received SCORE data, as illustrated in fig. App.2(d). This shows an example three-clock-period delay between the last byte of one frame and the first byte of the next frame. In this case, the first byte of data transferred to the microcomputer does not constitute a correct sync. code, and the data is rejected. Three clock periods later however, the sync. code detector detects the presence of a correct sync. code, a strobe pulse is produced, and the 8-bit counter U11A (which has reached a count of 3) is reset to zero and starts again. The example 3-bit delay is then automatically transferred to the output 8-bit counter U11B by the action of the synchronisation circuit.

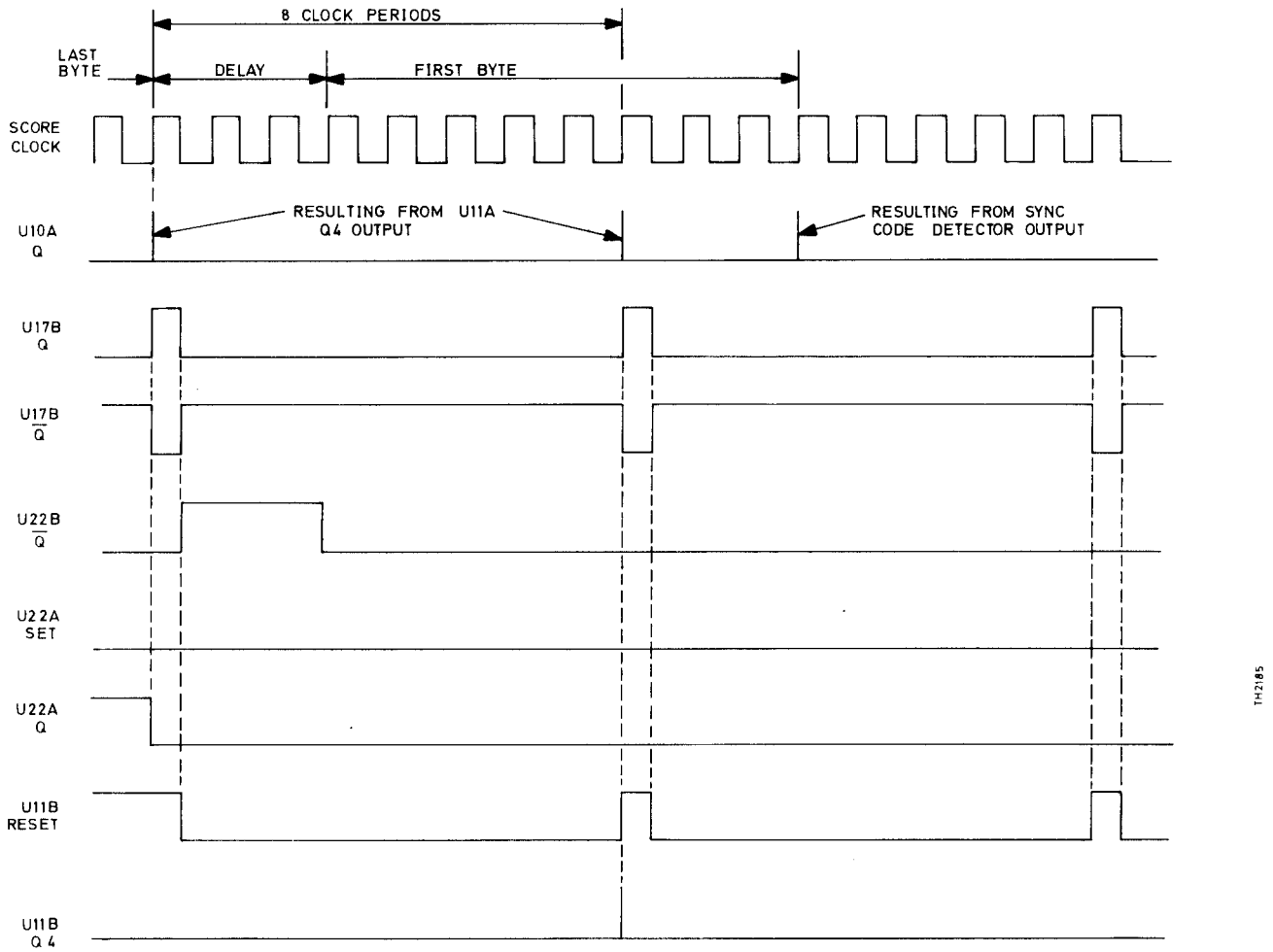


Fig. App. 2(d) Timing Diagram : Delayed SCORE Data

Interrupt Control

64. The logic '1' output signals from the receive and transmit interrupt latches, U10B and U22B respectively, are gated (U15A, U15D) with the respective software - controlled interrupt enable signal from U19 (I/O port 84, bits 6 and 7). The resulting '0' output from either U15A or U15D is inverted by U15C and applied to one input of

U15B. Provided an interrupt request from elsewhere within the receiver is not being serviced, then a '0' is present at P1 pin 28 ($\overline{ICB}$ input); this is applied to the priority in input of U19 to enable the interrupt circuitry, and is inverted by U14B to allow the output from U15C to produce a logic '0' external interrupt signal, which is applied to U19 pin 5. U19 then produces a logic '0' interrupt request signal, which is applied to the microcomputer, and also applies a mask-programmed interrupt vector address (hex 0680) to the microcomputer via the processor data bus. The microcomputer is then forced to execute the interrupt routine pointed to by vector address 0680. Whilst the interrupt routine is in progress, the priority out output from U19 is set to logic '1'; this is applied to the priority in input of the static memory interface (SMI) device in the microcomputer to prevent that device from initiating an interrupt.

External Strobe

65. The external strobe pulse generator U12A is clocked by the Q4 output from the 8-bit counter U11B. When an external strobe pulse is required, the microcomputer routes a '1' to the D input of U12A (strobe enable), this is transferred to the Q output on the positive-going transition of the Q4 output pulse from U11B, and U12A is reset after the time constant presented by R3, C12. The resulting positive-going pulse is inverted by open-collector transistor Q7 and is taken to J1 pin 21 for connection to equipment using the extra word facility.

Internal/External Data Control

66. The output shift register U24 is configured under software control to accept either parallel data from the microcomputer (via I/O port 0) or serial external revertive data at J1 pin 14 (applied to U24 via CR6 and inverting NAND buffer/driver U7B). For internal (parallel) input data operation, the microcomputer routes a '1' to the D input of the internal/external latch U17A; this is transferred to the Q output on the positive-going transition of the positive-going load pulse from U17B, transmission gate U21A is enabled, and the path between I/O port 0 bit 0 and the P8 input of U24 is completed. At the same time the negative going load pulse from U17B is inverted by U16C to momentarily enable the parallel inputs of U24, the parallel data is loaded in, and is then serially clocked out.

67. For external (serial) input data operation, the microcomputer routes a '0' to the D input of U17A; this time U21A is not enabled, the path between I/O port 0 bit 0 and the P8 input of U24 is broken, and U16C applies a '1' to U24 to enable the parallel inputs. The external revertive data is applied to the P8 input of U24 and is then serially clocked out.

68. The SCORE data and clock output driver U9 is enabled by the application of a '0' at pin 3. When the RA1792 receiver is switched on, the initialisation routine latches a '1' at U19 I/O port 84 bit 5. This is routed to the D input of the output enable latch U12B, and after the first load pulse from U17B, a permanent '0' is established at the $\overline{Q}$ output. The '1' at the Q output is applied to open collector

transistor Q9, but in the RA1792 no connection is made to J1 pin 1.

PERIPHERAL INPUT/OUTPUT (PIO) DEVICE

69. The PIO device U19 is mainly used for interrupt control purposes but is also used for the input output user function information. The device has two input/output ports, logic to handle an external interrupt (para.64), and a programmable interval timer (which is not used in this application). An 8-bit bi-directional data bus is used for the transfer of data between the PIO and the microcomputer, and a 5-bit bus (ROMC0 to ROMC4) is used for control purposes. A block diagram of the device is given in fig. App.2.(e).

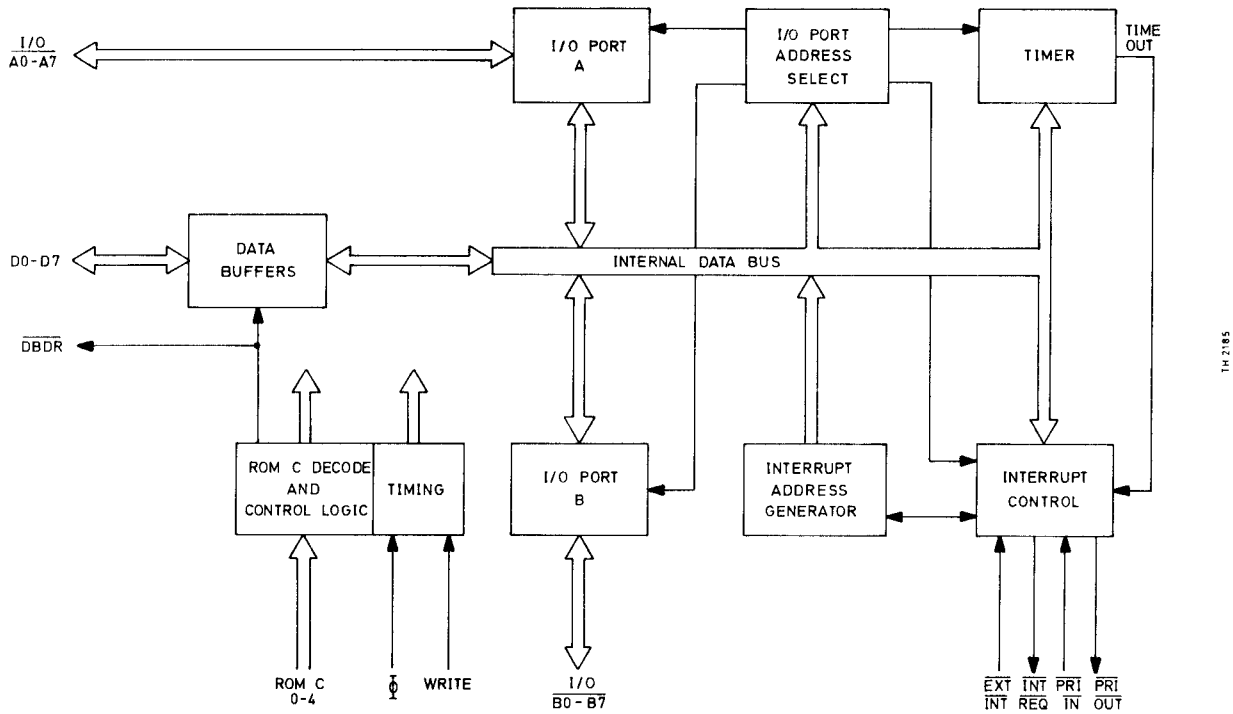


Fig. App.2(e) Block Diagram : 3861 PIO

70. The PIO device has four addressable ports, each with an assigned address. Two ports are used as 8-bit input/output ports (designated A and B in fig. App.2.(e)), whilst the remaining two ports are for the programmable timer and interrupt control purposes. The designated port addresses for the version of the 3861 PIO used in this application are in the range 04 to 07, as listed in Table 5. These addresses are however, modified by the action of the control bus (ROMC) decoder (para.75) so that the PIO responds to addresses in the range 84 to 87. Note that the timer and interrupt control ports are write only ports i.e. the contents of the associated port registers cannot be read by the microcomputer.

TABLE 5 : PIO PORT ADDRESSES

Address				Assigned To
Physical		Virtual		
Hex	Binary	Hex	Binary	
04	00000100	84	10000100	I/O Port A
05	00000101	85	10000101	I/O Port B
06	00000110	86	10000110	Interrupt Control Register
07	00000111	87	10000111	Programmable Timer

Device Connections

71. (1) Φ and WRITE: These are clock input signals derived by the microcomputer.

(2) ROMC0 to ROMC4: These are the control input signals from the microcomputer.

(3) DB0 to DB7: The bi-directional data bus lines which link the PIO to the microcomputer.

(4) $\overline{\text{EXT INT}}$: External interrupt input. When an external circuit applies a '0' to this input, an external interrupt request is latched into the PIO provided the interrupt control register has been set to allow external interrupts. The PIO subsequently communicates this interrupt request to the microcomputer via the $\overline{\text{INT REQ}}$ line.

(5) $\overline{\text{PRI IN}}$: Priority in. A '1' at this input denotes that a higher priority peripheral has a pending interrupt request. If the PIO receives an interrupt request, it is latched into the PIO but will not be serviced until a '0' is present at the $\overline{\text{PRI IN}}$ input.

(6) $\overline{\text{PRI OUT}}$: Priority out. This output signal is routed to the $\overline{\text{PRI IN}}$ input of the static memory interface unit in the microcomputer module. A '1' on this line denotes that the PIO has a pending interrupt request.

(7) $\overline{\text{INT REQ}}$: Interrupt request. A logic '0' on this output line is routed to the microcomputer to initiate the interrupt routine.

(8) $\overline{\text{DBDR}}$: Data bus drive. This output goes to a '0' whenever the PIO is driving the data bus as an output. This output is not used in this application.

(9) $\overline{\text{I/O A0-A7}}$ & $\overline{\text{I/O B0-B7}}$: Two bi-directional 8-bit input/output ports, A and B. In this application these ports respond to addresses 84 and 85 respectively.

Control Bus

72. The control bus, comprising the five lines labelled ROMC0 to ROMC4 conveys control signals to the PIO and also to the static memory interface (on the microcomputer board). The ROMC states decoded by the PIO are given in Table 5. Note that all ROMC states not listed in table 6 are decoded as 'no-operation'.

Instruction Execution

73. The microcomputer input/output instructions place the required I/O port address on the processor data bus during one instruction cycle, and then use the processor data bus in the following instruction cycle to carry out the actual I/O data transfer. The ROMC lines from the microcomputer (hex. states 1A and 1B) signal the PIO that an I/O data movement is occurring during the current instruction cycle. Thus for ROMC I/O transfer states 1A and 1B (table 5) the PIO requires to know whether the contents of the data bus during the previous instruction cycle matched any of the four assigned I/O addresses. This is accomplished by the I/O port address selection logic which constantly monitors the data bus. When an address match is detected, the information is held through the following instruction cycle.

74. Read instructions that select a port (addresses 84 and 85) cause the contents of the selected port to be placed on the processor data bus during the read instruction cycle. For write instructions, the PIO accepts a byte from the processor bus and loads it into one of the I/O ports or the interrupt control register (the programmable timer is not used in this application). Each I/O port output line is latched and thus holds the data transferred during the last I/O write instruction.

TABLE 6 : DECODED ROMC STATES

ROMC STATE		PIO FUNCTION
HEX	BINARY	
0F	01111	If an interrupt request is pending and $\overline{\text{PRI IN}}$ is at '0', the lower half of the interrupt vector address (80) is placed on the data bus.
10	10000	Place interrupt circuitry in an inhibit state that prevents altering the interrupt chain.
13	10011	If an interrupt request is pending and $\overline{\text{PRI IN}}$ is at '0', the upper half of the interrupt vector address (06) is placed on the data bus and the interrupt circuit is reset.
1A	11010	If an I/O port address was present on the data bus during the previous instruction cycle, move current contents of data bus into the appropriate port (I/O A, I/O B, timer or interrupt control).
1B	11011	If I/O port address 84 or 85 was present on the data bus during the previous instruction cycle, move contents of appropriate I/O port (I/O A or I/O B) onto the data bus.

Control Bus Decoder

75. The control bus decoder consists of a magnitude comparator U20 and a quad transmission gate U25. It monitors the ROMC control bus lines and when the 03 state is present, it inverts the level present on the PB7 processor data bus line which is applied to the PIO (U19 pin 7). Thus when an address in the range 84 to 87 is present on the processor data bus, it appears at the PIO data bus as an address in the range 04 to 07, i.e. the physical address range of the four PIO ports. The action of the circuit is as follows.

76. The magnitude comparator U20 produces a '1' at the A = B output when the logic levels at the A inputs are equal to these at the B inputs, and a '1' is also present at the A = B input. Thus when ROMC lines 0 and 1 are both at '1' and lines 2 to 4 are at '0' (03 code), a '1' is produced at the A = B output. This enables U25A and U25C, the '0' from U25A disables U25B, and the level present at the PB7 data bus line is inverted by U25D before application to pin 7 of U19 via U25C. For any other

ROMC code, the A = B output of U20 is at '0', U25A and U25C are disabled, and U25B is enabled to connect the PB7 data bus line directly to pin 7 of U19.

77. The microcomputer applies 03 to the ROMC lines each time a PIO port address is applied to the data bus. As far as the PIO device is concerned, ROMC state 03 is a 'no-operation' (para. 72).

USER FUNCTIONS

78. The input user functions are applied to the PIO (I/O port 85) via inverting buffer/drivers U5A, U5B, U6A and U6B. The output user functions from the PIO (I/O port 84) are routed to rear panel connector J1 via open-collector inverters Q1 to Q4. The new data output request signal from Q8 is not used in this application.

INTERNAL CLOCK GENERATOR

79. This uses the otherwise spare section of the quad line receiver U3C. R15 is selected on test to produce a squarewave output at approximately 6KHz.

-5V SUPPLY

80. The -5V supply required by the line driver device U9 is provided by three-terminal regulator U18 which is powered from the -15V supply at P1 pin 23.

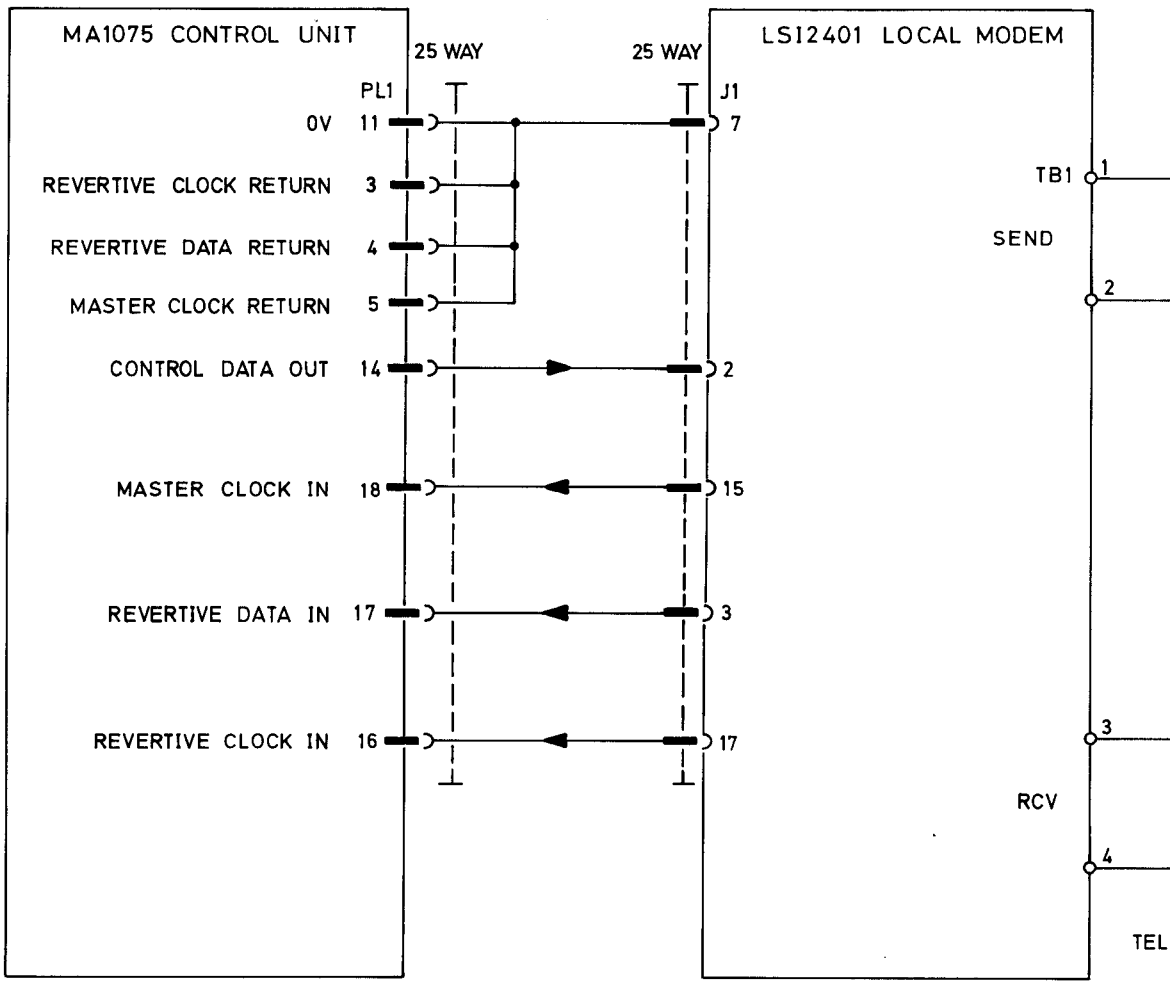
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SCORE INTERFACE BOARD (STO 8459)			
Resistors					
R1	68 k	Metal Oxide		2	916478
R2	68 k	Metal Oxide		2	916478
R3	68 k	Metal Oxide		2	916478
R4	68 k	Metal Oxide		2	916478
R5	68 k	Metal Oxide		2	916478
R6		Not used			
R7	22 k	Metal Oxide		2	913493
R8	10 k	Metal Oxide		2	914042
R9	10 k	Metal Oxide		2	914042
R10	10 k	Metal Oxide		2	914042
R11	10 k	Metal Oxide		2	914042
R12	10 k	Metal Oxide		2	914042
R13	15 k	Metal Oxide		2	920645
R14	33 k	Metal Oxide		2	913495
R15	15k to 56k	Selected on test			
R16	1 k	Metal Oxide		2	913489
R17	10 k	Metal Oxide		2	914042
R18	10 k	Metal Oxide		2	914042
R19	10 k	Metal Oxide		2	914042
R20	10 k	Metal Oxide		2	914042
Capacitors			Volts		
C1	0.1	Disc Ceramic	50	20	938406
C2	0.22	Disc Ceramic	50	20	938676
C3	.01	Disc Ceramic	50	20	938053
C4	22	Tantalum	10	20	921090
C5	6.8	Tantalum	10	20	938031
C6	6.8	Tantalum	10	20	938031
C7	100p	Disc Ceramic	500	10	938556
C8	47p	Disc Ceramic	500	10	917418
C9	47p	Disc Ceramic	500	10	917418
C10	47p	Disc Ceramic	500	10	917418
C11	47p	Disc Ceramic	500	10	917418
C12	100p	Disc Ceramic	500	10	938556
C13	.01	Disc Ceramic	50	20	938053
C14	47p	Disc Ceramic	500	10	917418

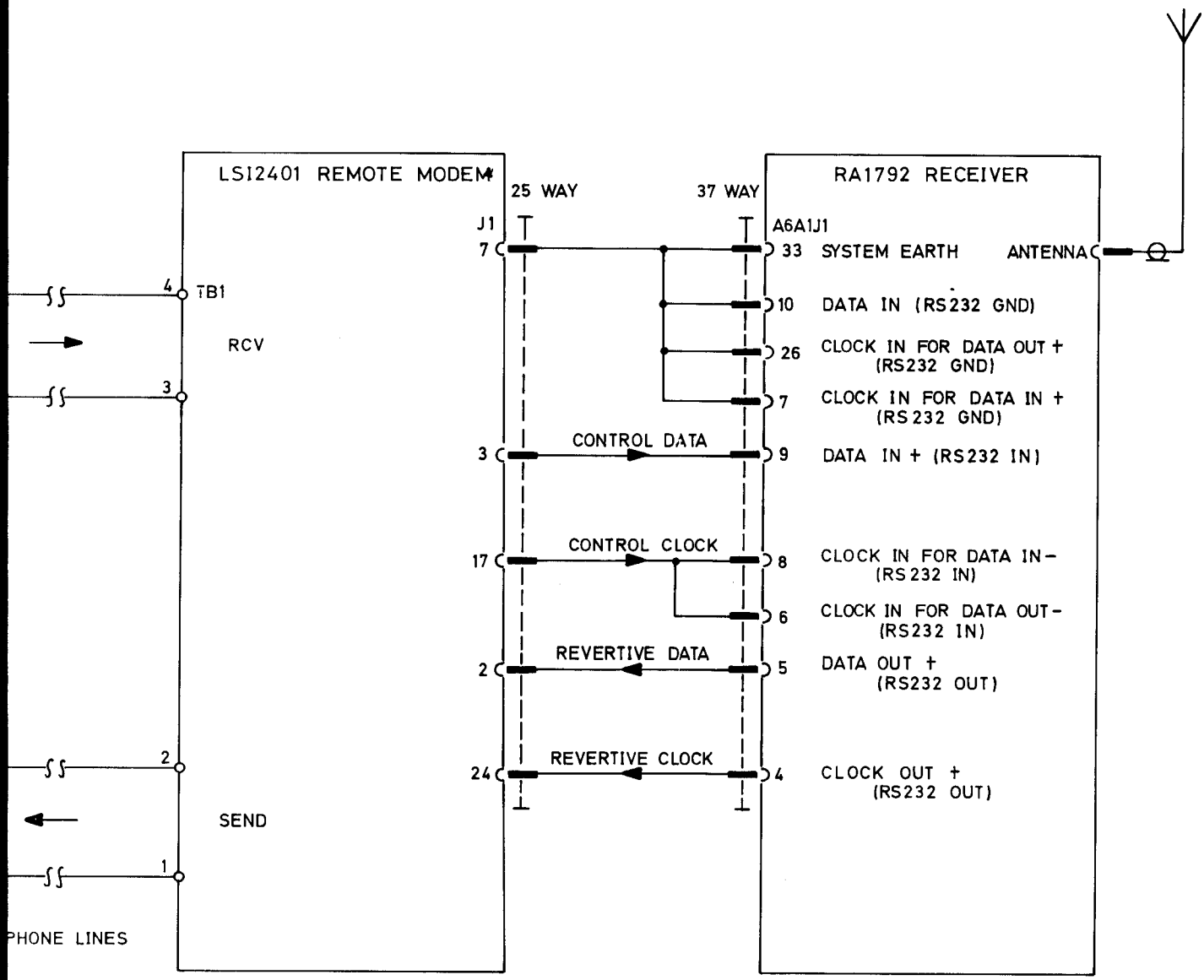
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
J1		Socket 37-way			938678
		Mating plug, 37-way			916507
		Shell, junction			918105
		Retainer			914245
P1		Plug, 50-way PCB			A07881
Diodes					
CR1		Silicon IN916			913480
CR2		Silicon IN916			913480
CR3		Silicon IN916			913480
CR4		Silicon IN916			913480
CR5		Silicon IN916			913480
CR6		Silicon IN916			913480
CR7		Silicon IN916			913480
CR8		Silicon IN916			913480
Transistors					
Q1		NPN Silicon IN3904			914046
Q2		NPN Silicon IN3904			914046
Q3		NPN Silicon IN3904			914046
Q4		NPN Silicon IN3904			914046
Q5		NPN Silicon IN3904			914046
Q6		NPN Silicon IN3904			914046
Q7		NPN Silicon IN3904			914046
Q8		NPN Silicon IN3904			914046
Q9		NPN Silicon IN3904			914046
Integrated Circuits					
U1	10 k	Resistor Network, SIL			933750
U2	68 k	Resistor Network, DIL			938680
U3		Quad line receiver 26L532			938683
U4		Not used			
U5		Dual 2-input NAND buffer 40107			928188
U6		Dual 2-input NAND buffer 40107			928188
U7		Dual 2-input NAND buffer 40107			928188
U8		Dual 2-input NAND buffer 40107			928188
U9		Dual RS422 line driver 26LS30			938684
U10		Dual D-type flip-flop 4013			926860

SCORE INTERFACE BOARD (STO 8459)

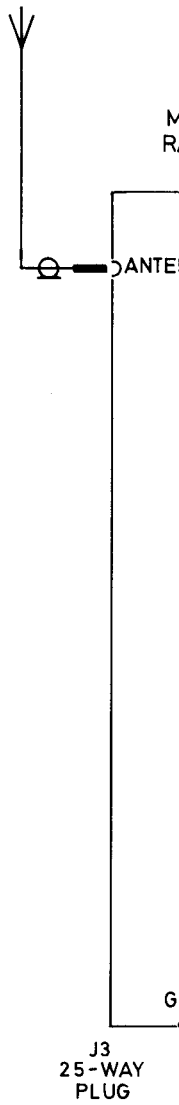
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
R1	68 k	Metal Oxide		2	916478
R2	68 k	Metal Oxide		2	916478
R3	68 k	Metal Oxide		2	916478
R4	68 k	Metal Oxide		2	916478
R5	68 k	Metal Oxide		2	916478
R6		Not used			
R7	22 k	Metal Oxide		2	913493
R8	10 k	Metal Oxide		2	914042
R9	10 k	Metal Oxide		2	914042
R10	10 k	Metal Oxide		2	914042
R11	10 k	Metal Oxide		2	914042
R12	10 k	Metal Oxide		2	914042
R13	15 k	Metal Oxide		2	920645
R14	33 k	Metal Oxide		2	913495
R15	15k to 56k	Selected on test			
R16	1 k	Metal Oxide		2	913489
R17	10 k	Metal Oxide		2	914042
R18	10 k	Metal Oxide		2	914042
R19	10 k	Metal Oxide		2	914042
R20	10 k	Metal Oxide		2	914042
Capacitors			**Volts**		
C1	0.1	Disc Ceramic	50	20	938406
C2	0.22	Disc Ceramic	50	20	938676
C3	.01	Disc Ceramic	50	20	938053
C4	22	Tantalum	10	20	921090
C5	6.8	Tantalum	10	20	938031
C6	6.8	Tantalum	10	20	938031
C7	100p	Disc Ceramic	500	10	938556
C8	47p	Disc Ceramic	500	10	917418
C9	47p	Disc Ceramic	500	10	917418
C10	47p	Disc Ceramic	500	10	917418
C11	47p	Disc Ceramic	500	10	917418
C12	100p	Disc Ceramic	500	10	938556
C13	.01	Disc Ceramic	50	20	938053
C14	47p	Disc Ceramic	500	10	917418

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
U11		Dual BCD Up- Counter 4518			928002
U12		Dual D-type flip-flop 4013			926860
U13		Dual 4-bit shift register 4015			930973
U14		Hex inverting buffer 4049			930033
U15		Quad 2-input NAND gate 4011			920028
U16		Quad 2-input NAND gate 4011			920028
U17		Dual D-type flip flop 4013			926860
U18		-5V 3-terminal regulator 79M05			938679
U19		PIO 3861A			938687
U20		Magnitude comparator 4585			938686
U21		Quad transmission gate 4066			930148
U22		Dual D-type flip flop 4013			926860
U23		8-Stage Shift register 4094			929324
U24		8-Stage Shift register 4014			930972
U25		Quad Transmission gate 4066			930148
U26	22 k	Resistor network SIL			938682


MA1075 CONTROL UNIT
25 WAY
25 WAY
LS12401 LOCAL MODEM
PL1
J1
0V 11
7
REVERTIVE CLOCK RETURN 3
REVERTIVE DATA RETURN 4
MASTER CLOCK RETURN 5
CONTROL DATA OUT 14
2
MASTER CLOCK IN 18
15
REVERTIVE DATA IN 17
3
REVERTIVE CLOCK IN 16
17
TB1
1
SEND
2
3
RCV
4
TEL



Interconnection Diagram : Typical
Remote Control Installation Fig. App.2.1



RACAL
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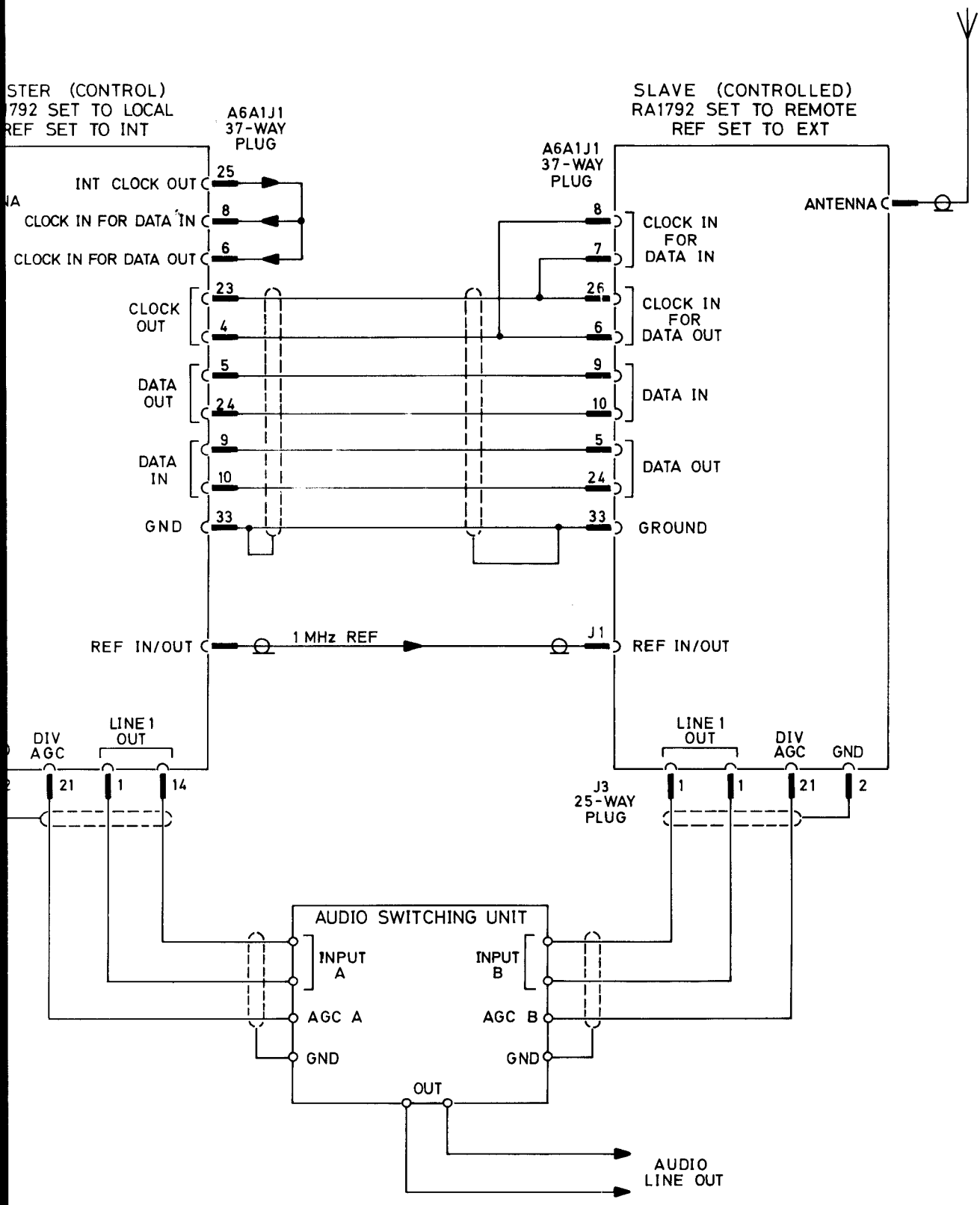
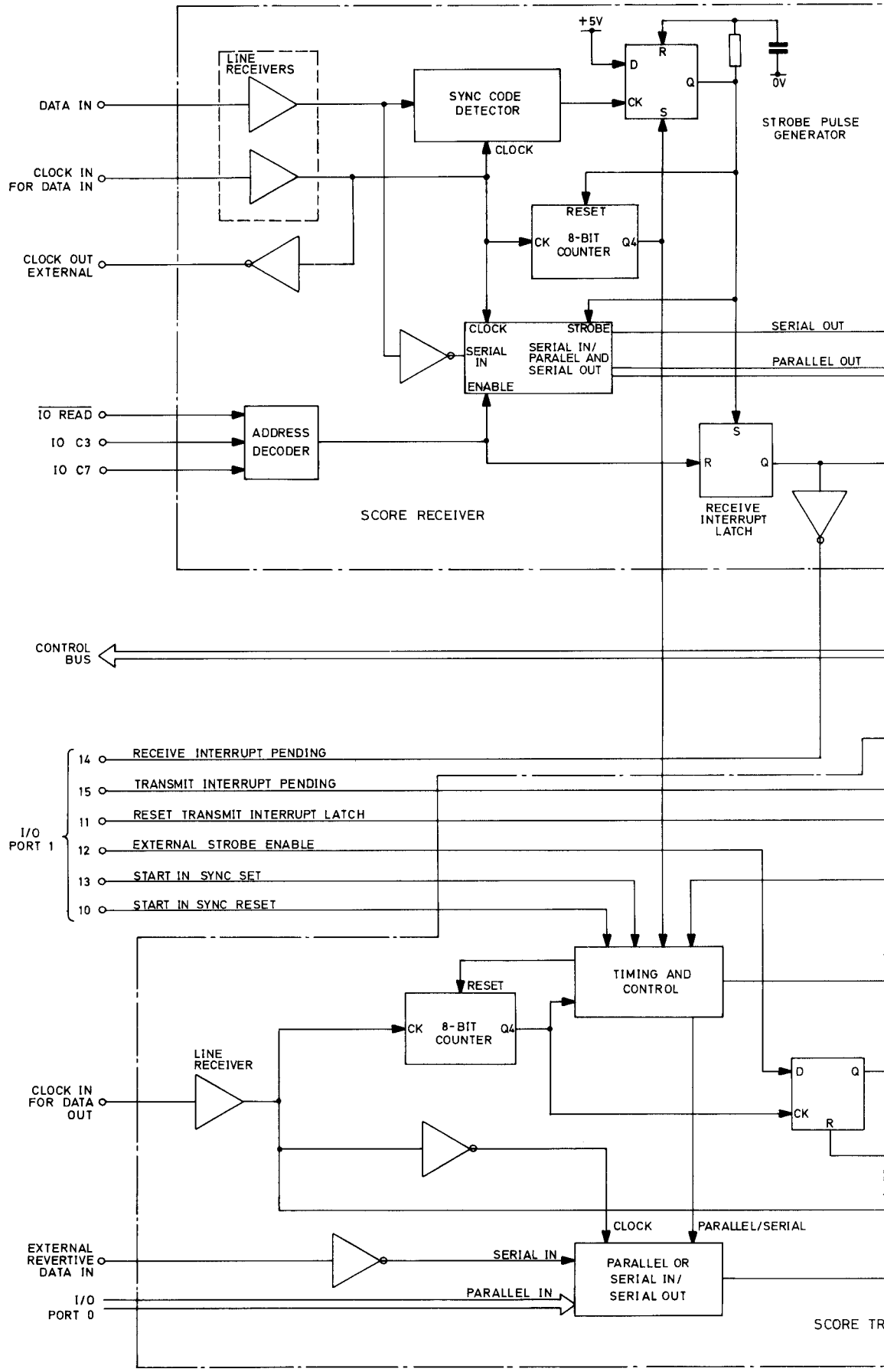
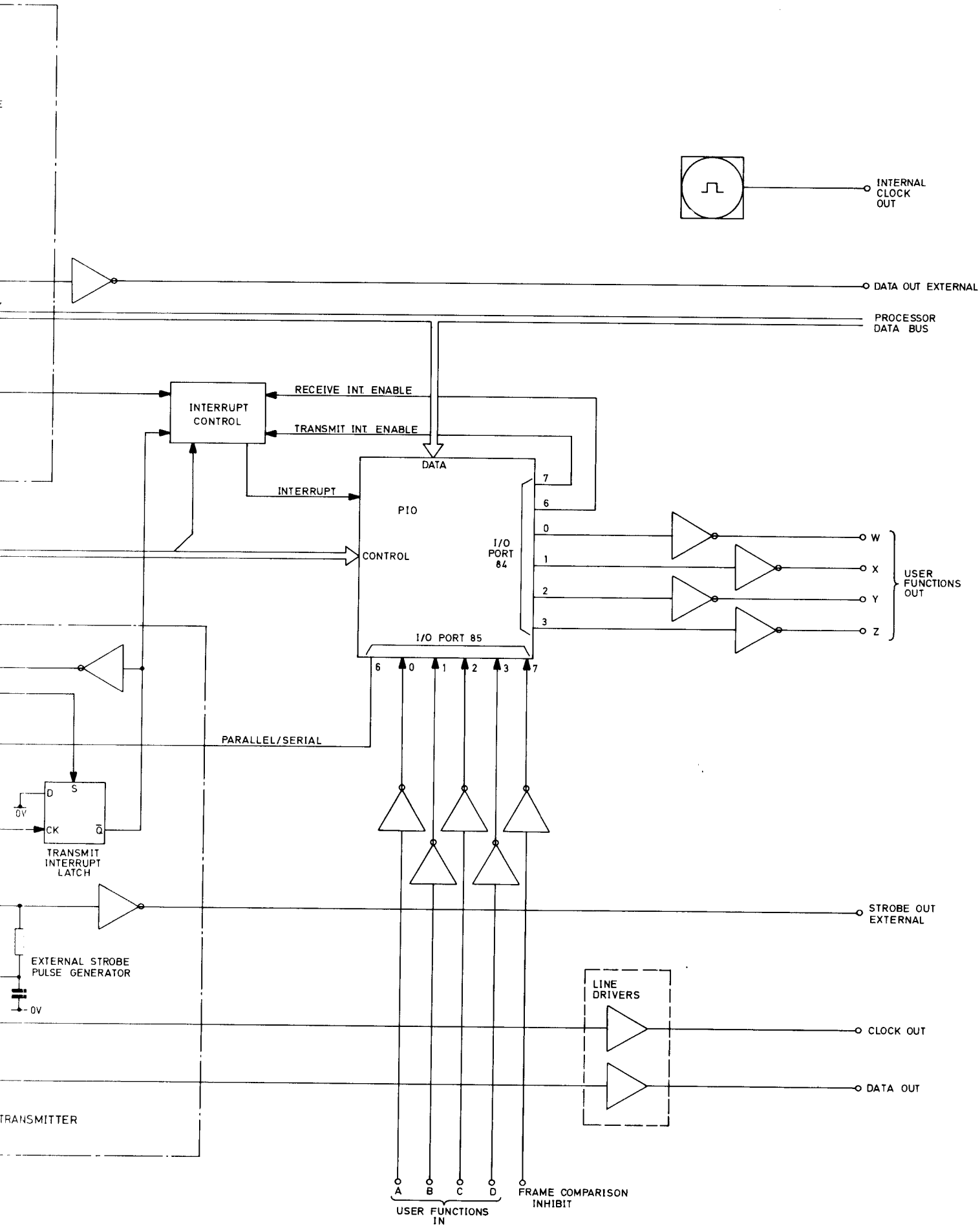


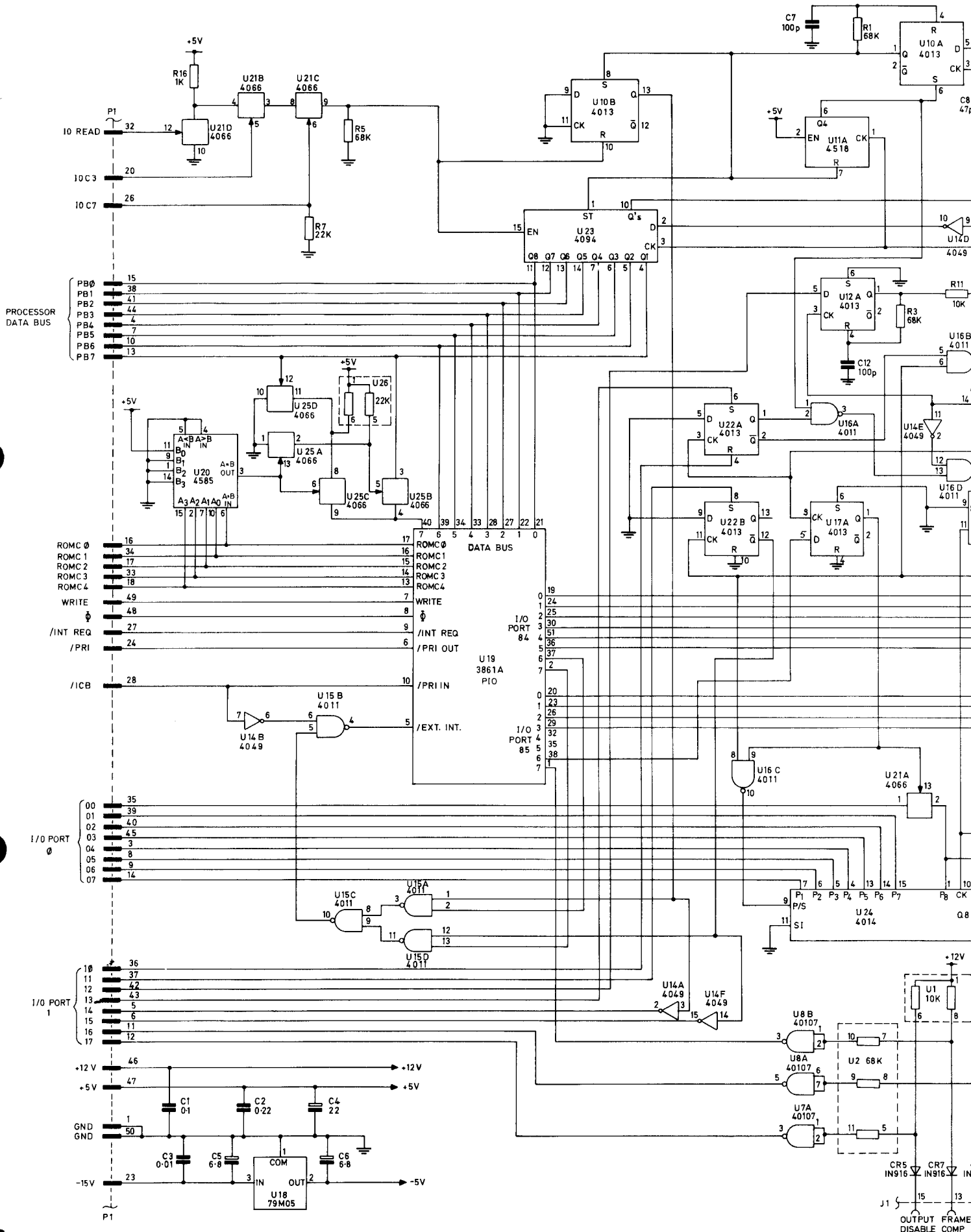
Interconnection Diagram : Typical
Space Diversity Installation Fig. App.2·2


+5V
LINE RECEIVERS
DATA IN
CLOCK IN FOR DATA IN
CLOCK OUT EXTERNAL
SYNC CODE DETECTOR
CLOCK
D
R
Q
CK
S
0V
STROBE PULSE GENERATOR
RESET
CK 8-BIT COUNTER Q4
CLOCK
STROBE
SERIAL IN
SERIAL IN/ PARALEL AND SERIAL OUT
ENABLE
SERIAL OUT
PARALLEL OUT
IO READ
IO C3
IO C7
ADDRESS DECODER
S
R
Q
RECEIVE INTERRUPT LATCH
SCORE RECEIVER
CONTROL BUS
I/O PORT 1
14 RECEIVE INTERRUPT PENDING
15 TRANSMIT INTERRUPT PENDING
11 RESET TRANSMIT INTERRUPT LATCH
12 EXTERNAL STROBE ENABLE
13 START IN SYNC SET
10 START IN SYNC RESET
TIMING AND CONTROL
RESET
CK 8-BIT COUNTER Q4
LINE RECEIVER
CLOCK IN FOR DATA OUT
D
Q
CK
R
CLOCK
PARALLEL/SERIAL
EXTERNAL REVERTIVE DATA IN
I/O PORT 0
SERIAL IN
PARALLEL IN
PARALLEL OR SERIAL IN/ SERIAL OUT
SCORE TR



Block Diagram :
SCORE Interface Board

Fig. App 2.3



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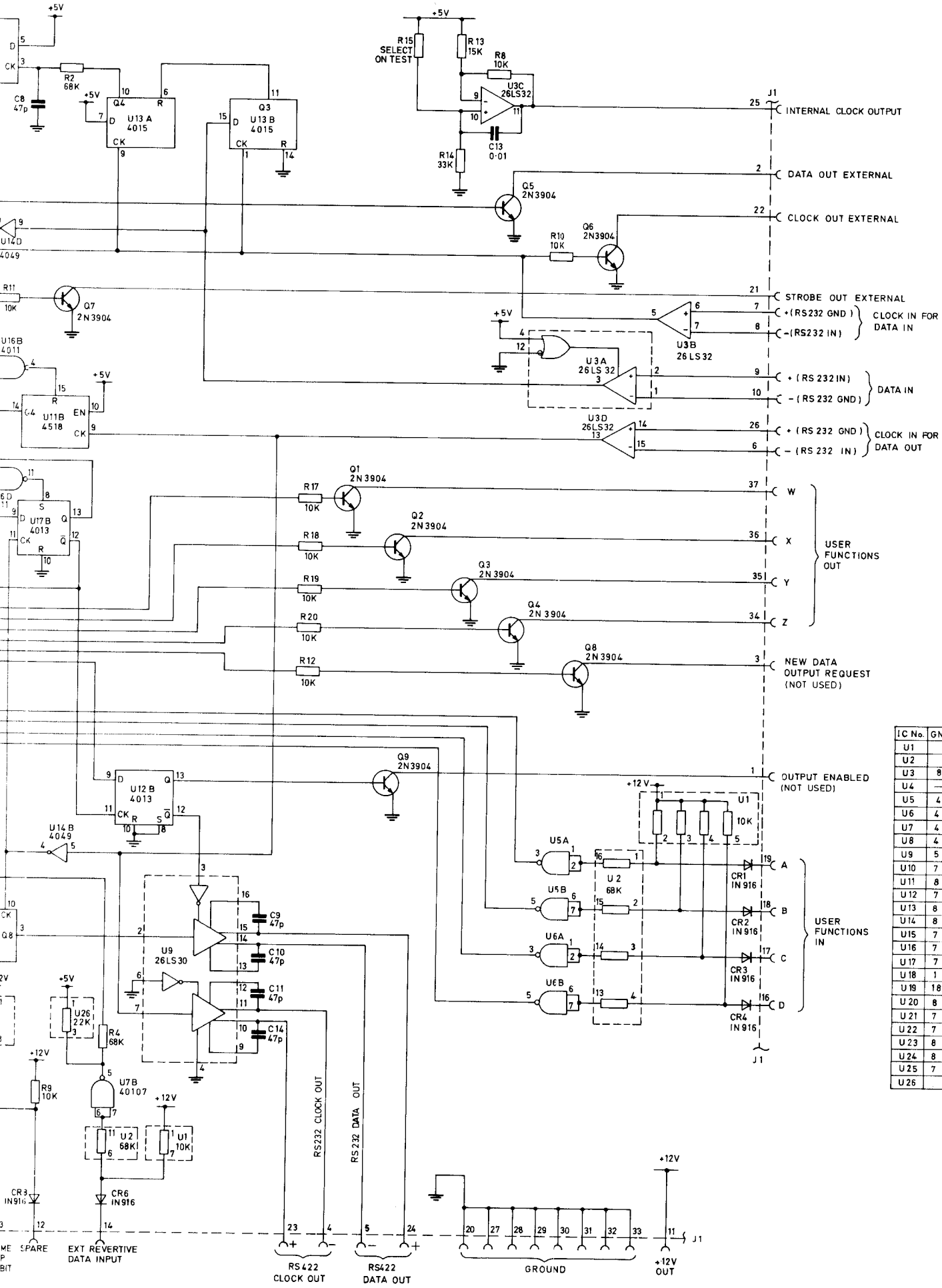
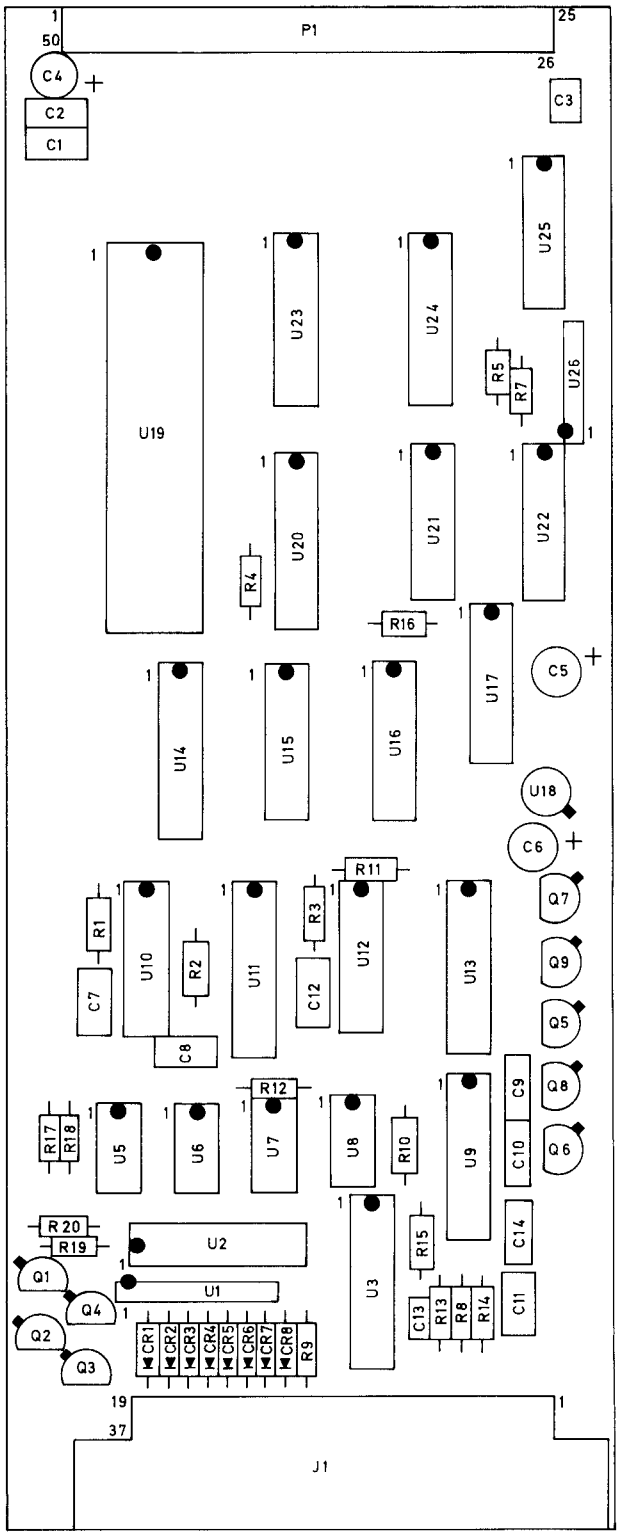


IC No.	GND	+5V	+12V	-5V	
U1			1		—
U2					—
U3	8	16			26LS
U4	—	—	—	—	—
U5	4		8		401
U6	4		8		401
U7	4		8		401
U8	4		8		401
U9	5	1		8	26LS
U10	7	14			4013
U11	8	16			451
U12	7	14			401
U13	8	16			401
U14	8	1			404
U15	7	14			401
U16	7	14			401
U17	7	14			4013
U18	1			2	79M
U19	18	4	3		386
U20	8	16			4585
U21	7	14			4066
U22	7	14			4013
U23	8	16			4094
U24	8	16			4014
U25	7	14			4066
U26		1			—

Circuit: SCORE Interface Module A6 A1 **Fig. App. 2**



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Layout : SCORE Interface Board A6A1

Fig. App. 2.5

SCORE INTERFACE BOARD (STO 8459)

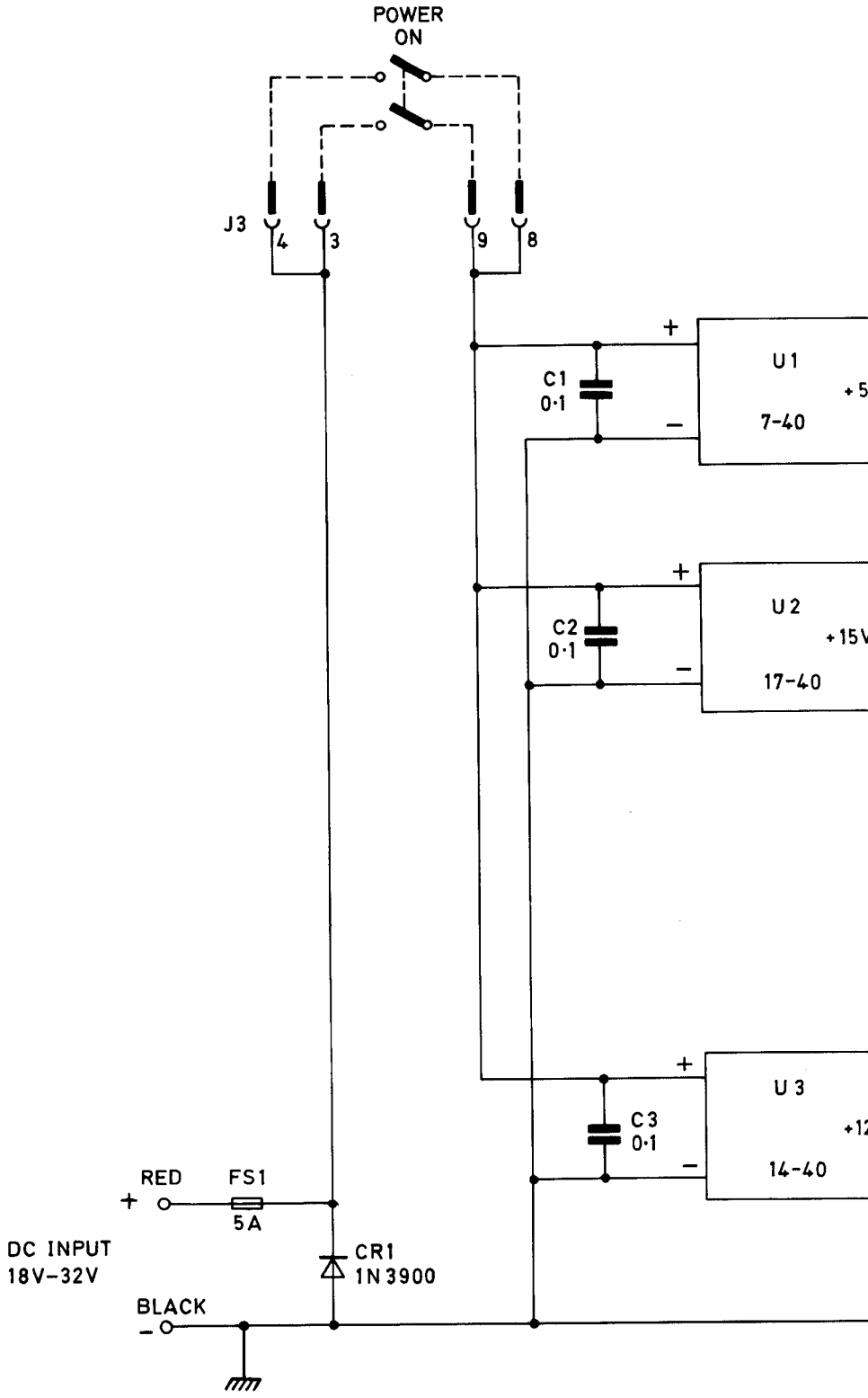
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Resistors					
R1	68 k	Metal Oxide		2	916478
R2	68 k	Metal Oxide		2	916478
R3	68 k	Metal Oxide		2	916478
R4	68 k	Metal Oxide		2	916478
R5	68 k	Metal Oxide		2	916478
R6		Not used			
R7	22 k	Metal Oxide		2	913493
R8	10 k	Metal Oxide		2	914042
R9	10 k	Metal Oxide		2	914042
R10	10 k	Metal Oxide		2	914042
R11	10 k	Metal Oxide		2	914042
R12	10 k	Metal Oxide		2	914042
R13	15 k	Metal Oxide		2	920645
R14	33 k	Metal Oxide		2	913495
R15	15k to 56k	Selected on test			
R16	1 k	Metal Oxide		2	913489
R17	10 k	Metal Oxide		2	914042
R18	10 k	Metal Oxide		2	914042
R19	10 k	Metal Oxide		2	914042
R20	10 k	Metal Oxide		2	914042
Capacitors			**Volts**		
C1	0.1	Disc Ceramic	50	20	938406
C2	0.22	Disc Ceramic	50	20	938676
C3	.01	Disc Ceramic	50	20	938053
C4	22	Tantalum	10	20	921090
C5	6.8	Tantalum	10	20	938031
C6	6.8	Tantalum	10	20	938031
C7	100p	Disc Ceramic	500	10	938556
C8	47p	Disc Ceramic	500	10	917418
C9	47p	Disc Ceramic	500	10	917418
C10	47p	Disc Ceramic	500	10	917418
C11	47p	Disc Ceramic	500	10	917418
C12	100p	Disc Ceramic	500	10	938556
C13	.01	Disc Ceramic	50	20	938053
C14	47p	Disc Ceramic	500	10	917418

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
J1		Socket 37-way			938678
		Mating plug, 37-way			916507
		Shell, junction			918105
		Retainer			914245
P1		Plug, 50-way PCB			A07881
Diodes					
CR1		Silicon IN916			913480
CR2		Silicon IN916			913480
CR3		Silicon IN916			913480
CR4		Silicon IN916			913480
CR5		Silicon IN916			913480
CR6		Silicon IN916			913480
CR7		Silicon IN916			913480
CR8		Silicon IN916			913480
Transistors					
Q1		NPN Silicon IN3904			914046
Q2		NPN Silicon IN3904			914046
Q3		NPN Silicon IN3904			914046
Q4		NPN Silicon IN3904			914046
Q5		NPN Silicon IN3904			914046
Q6		NPN Silicon IN3904			914046
Q7		NPN Silicon IN3904			914046
Q8		NPN Silicon IN3904			914046
Q9		NPN Silicon IN3904			914046
Integrated Circuits					
U1	10 k	Resistor Network, SIL			933750
U2	68 k	Resistor Network, DIL			938680
U3		Quad line receiver 26L532			938683
U4		Not used			
U5		Dual 2-input NAND buffer 40107			928188
U6		Dual 2-input NAND buffer 40107			928188
U7		Dual 2-input NAND buffer 40107			928188
U8		Dual 2-input NAND buffer 40107			928188
U9		Dual RS422 line driver 26LS30			938684
U10		Dual D-type flip-flop 4013			926860

DC POWER SUPPLY MODULE (ST 80762)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			**Volts**		
A1C1	100	Electrolytic	25		935140
C1	0μ1	Disc Ceramic	100	20	938406
C2	0μ1	Disc Ceramic	100	20	938406
C3	0μ1	Disc Ceramic	100	20	938406
C4	0μ1	Disc Ceramic	100	20	938406
C5	6μ8	Tantalum	35	20	921179
C6	0μ1	Disc Ceramic	100	20	938406
C7	6μ8	Tantalum	35	20	921179
C8	0μ1	Disc Ceramic	100	20	938406
C9	6μ8	Tantalum	35	20	921179
C10	6μ8	Tantalum	35	20	921179
C11	6μ8	Tantalum	35	20	921179
Resistors					
A1R1	220	Metal Film		2	910390
Fuses					
FS1	5A	Fuselink, quick blow			937892
		Fuseholder			938647
Diodes					
CR1		Std mounting 100 V 20 A			937889
Connectors					
J1		Terminal, Red			937895
J2		Terminal, Black			937894
J3		Socket, 9-way			918090
A1 J1		Socket, 25-way			915970

Cct Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Converter Modules					
U1		+5 V, 3 A			938648
U2		+15 V, 1.5 A			938649
U3		+12 V, 2 A			938650
U4		+20 V			938652
U5		-15 V, 670 mA			938651
Miscellaneous					
A1		Connector Board			B08688



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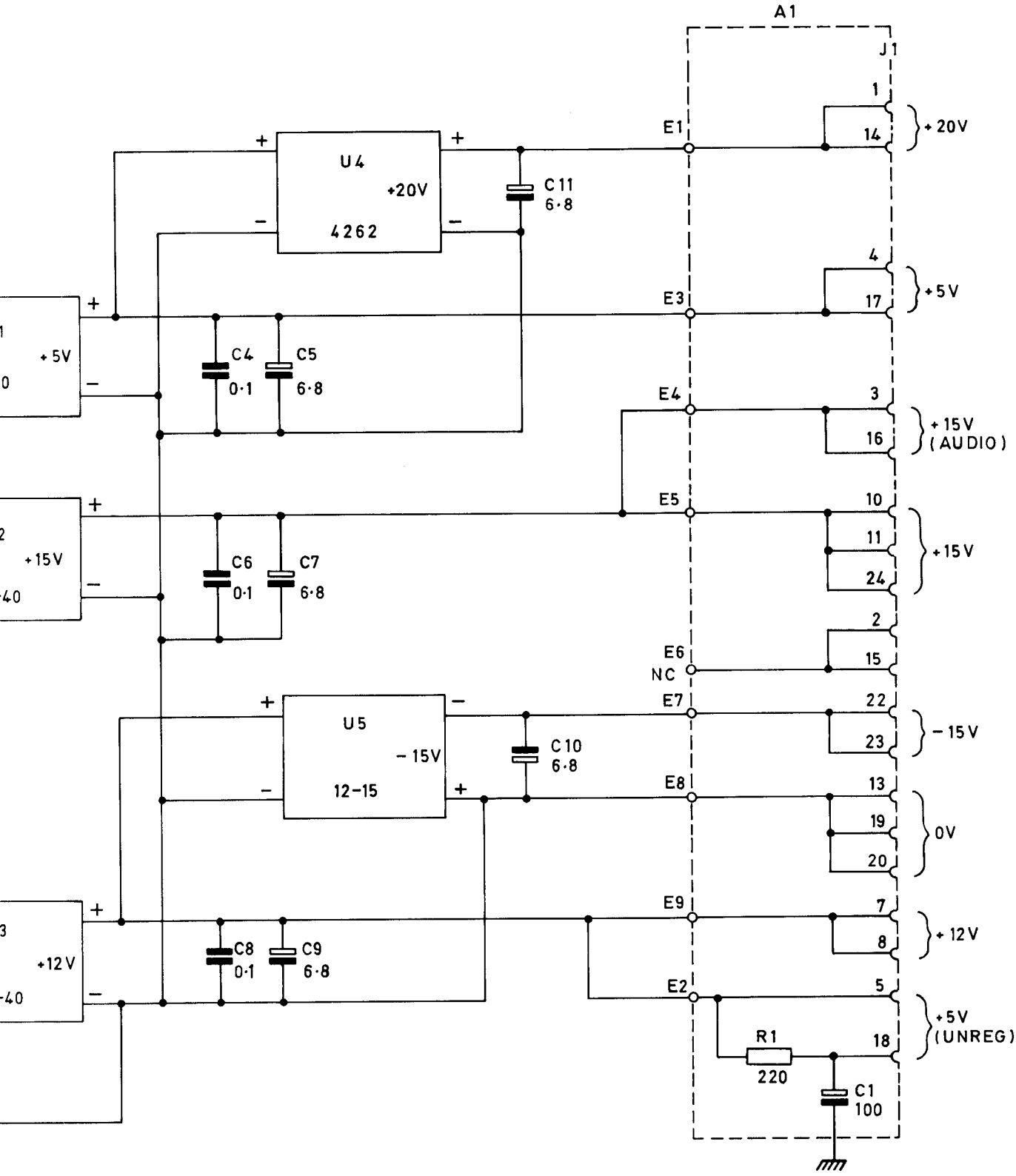
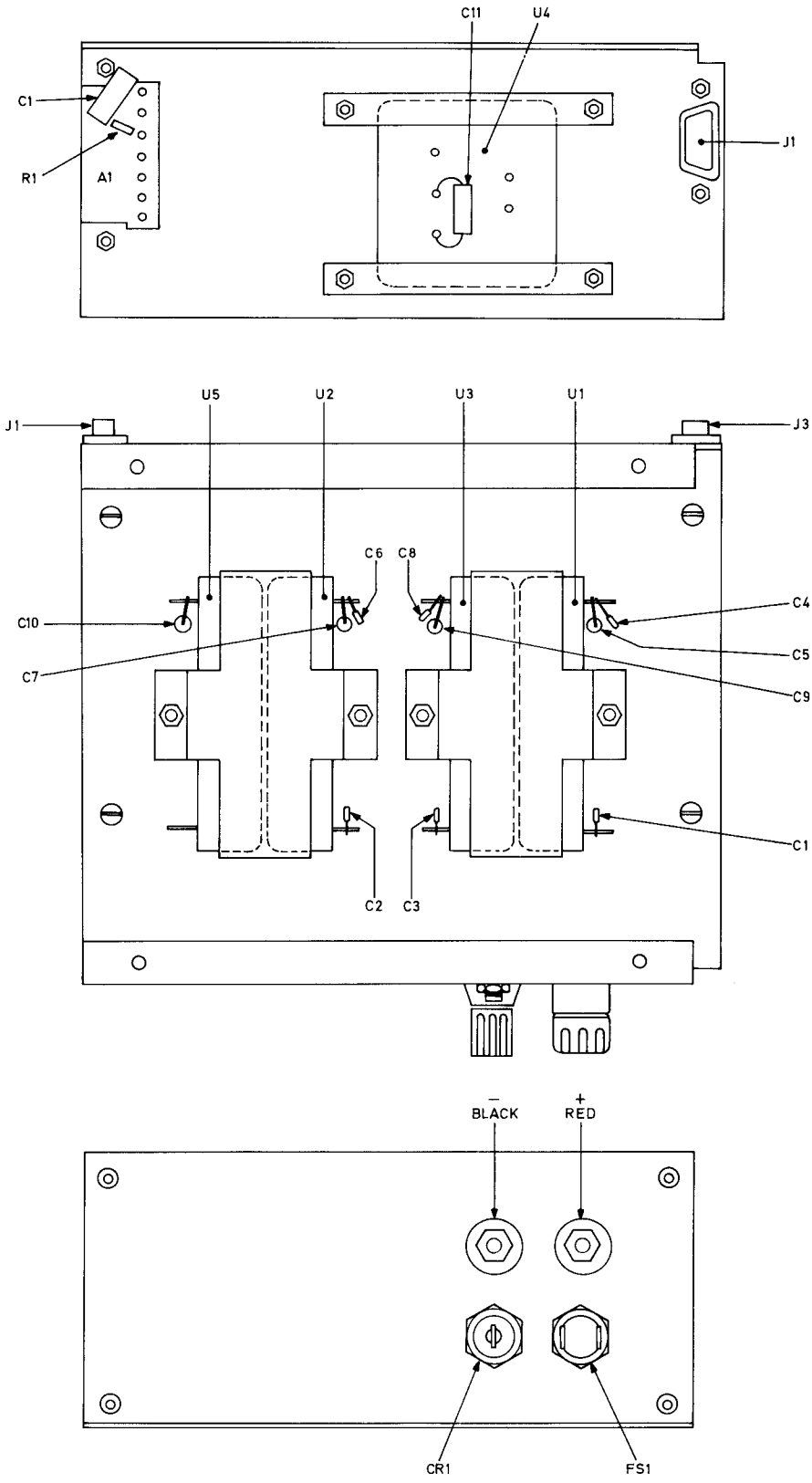


Circuit : DC/DC Power Supply Module A10 Fig. App.3



RACAL TH2185

Layout : DC/DC Power Supply Module A10 Fig. App. 3·2

FIRST LO SYNTHESIZER BOARD A7 (ST08545)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors					
R1	47k	Metal Oxide		2	913496
R2	10	Metal Oxide		2	920736
R3	10k	Metal Oxide		2	914042
R4	330	Metal Oxide		2	915690
R5	200	Variable	0.5	20	938618
R6	47	Metal Oxide		2	917063
R7	68	Metal Oxide		2	916476
R8	68	Metal Oxide		2	916476
R9	22	Metal Oxide		2	920743
R10	1.5k	Metal Oxide		2	911166
R11	680	Metal Oxide		2	910113
R12	10	Metal Oxide		2	920736
R13	390	Metal Oxide		2	916331
R14	120k	Metal Oxide		2	917062
R15	820	Metal Oxide		2	917065
R16	500	Variable		20	938426
R17	2.2k	Metal Oxide		2	916546
R18	47	Metal Oxide		2	917063
R19	1.0	Composition		5	938617
R20		Not used			
R21	82	Metal Oxide		2	917057
R22	22	Metal Oxide		2	920743
R23	220	Metal Oxide		2	910390
R24	470	Metal Oxide		2	920758
R25	1k	Metal Oxide		2	913489
R26	1.5k	Metal Oxide		2	911166
R27	330	Metal Oxide		2	915690
R28	10	Metal Oxide		2	920736
R29	100	Metal Oxide		2	910388
R30	820	Metal Oxide		2	917065

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R31	220	Metal Oxide		2	910390
R32	220	Metal Oxide		2	910390
R33	820	Metal Oxide		2	917065
R34	470	Metal Oxide		2	920758
R35	470	Metal Oxide		2	920758
R36	220	Metal Oxide		2	910390
R37	820	Metal Oxide		2	917065
R38	470	Metal Oxide		2	920758
R39		Not used			
R40	470	Metal Oxide		2	920758
R41	470	Metal Oxide		2	920758
R42	470	Metal Oxide		2	920758
R43	820	Metal Oxide		2	917065
R44	330	Metal Oxide		2	915690
R45	38k	Metal Oxide		2	900993
R46	470	Metal Oxide		2	920758
R47	820	Metal Oxide		2	917065
R48	470	Metal Oxide		2	920758
R49	470	Metal Oxide		2	920758
R50	10k	Metal Oxide		2	914042
R51	12k	Metal Oxide		2	917952
R52	2.7k	Metal Oxide		2	916548
R53	4.7k	Metal Oxide		2	913490
R54	4.7k	Metal Oxide		2	913490
R55	470	Metal Oxide		2	920758
R56	1.8k	Metal Oxide		2	911148
R57	3.3k	Metal Oxide		2	910111
R58	470	Metal Oxide		2	920758
R59	3.3k	Metal Oxide		2	910111
R60	22	Metal Oxide		2	920743
R61	1k	Metal Oxide		2	913489
R62	10k	Metal Oxide		2	914042
R63	1k	Metal Oxide		2	913489
R64	39k	Metal Oxide		2	900993
R65	15k	Metal Oxide		2	920645

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R66	8.2k	Metal Oxide		2	918202
R67	12k	Metal Oxide		2	917952
R68	1k	Metal Oxide		2	913489
R69	3.3k	Metal Oxide		2	910111
R70	1k	Metal Oxide		2	913489
R71	82	Metal Oxide		2	917057
R72	10	Metal Oxide		2	920736
R73	10k	Metal Oxide		2	914042
R74	15k	Metal Oxide		2	920645
R75	15k	Metal Oxide		2	920645
R76	15k	Metal Oxide		2	920645
R77	100k	Metal Oxide		2	915190
R78	2-7k	Metal Oxide		2	916548
R79	12k	Metal Oxide		2	917952
R80	150k	Metal Oxide		2	917594
R81	10k	Metal Oxide		2	914042
R82	10k	Metal Oxide		2	914042
R83	10k	Metal Oxide		2	914042
R84	3.3k	Metal Oxide		2	910111
R85	100	Metal Oxide		2	910388
R86	470	Metal Oxide		2	920758
R87	47k	Metal Oxide		2	913496
R88	120k	Metal Oxide		2	915373
R89	47k	Metal Oxide		2	913496
R90	1k	Metal Oxide		2	913489
R91	150	Metal Oxide		2	910389
R92	10	Metal Oxide		2	920736
R93	680	Metal Oxide		2	910113
R94	10	Metal Oxide		2	920736
R95	1k	Metal Oxide		2	913489
R96		Not used			
R97	1k	Metal Oxide		2	913489

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C1	6.8	Tantalum	35	20	938030
C2	6.8	Tantalum	35	20	938030
C3	6.8	Tantalum	35	20	938030
C4	6.8	Tantalum	35	20	938030
C5	.01	Ceramic	50	20	938053
C6	6.8	Tantalum	35	20	938030
C7	.01	Ceramic	50	20	938053
C8	6.8	Tantalum	35	20	938030
C9	.01	Ceramic	50	20	938053
C10	10p	Ceramic	500	5	917746
C11	.01	Ceramic	50	20	938053
C12	6.8	Tantalum	35	20	938030
C13	.01	Ceramic	50	20	938053
C14	.01	Ceramic	50	20	938053
C15	.01	Ceramic	50	20	938053
C16	.01	Ceramic	50	20	938053
C17	.01	Ceramic	50	20	938053
C18	.01	Ceramic	50	20	938053
C19	.01	Ceramic	50	20	938053
C20	.01	Ceramic	50	20	938053
C21	.01	Ceramic	50	20	938053
C22	.01	Ceramic	50	20	938053
C23	.01	Ceramic	50	20	938053
C24	.01	Ceramic	50	20	938053
C25	.01	Ceramic	50	20	938053
C26	.01	Ceramic	50	20	938053
C27	.01	Ceramic	50	20	938053
C28	.01	Ceramic	50	20	938053
C29	.01	Ceramic	50	20	938053
C30	.01	Ceramic	50	20	938053
C31	.01	Ceramic	50	20	938053
C32	.01	Ceramic	50	20	938053
C33	.01	Ceramic	50	20	938053
C34	.01	Ceramic	50	20	938053
C35	0.1	Ceramic	50	20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C36	6.8	Tantalum	35	20	938030
C37	0.1	Ceramic	50	20	938406
C38	6.8	Tantalum	35	20	938030
C39	.01	Ceramic	50	20	938053
C40	.001	Ceramic	50	20	938408
C41	33	Tantalum	25	10	938606
C42	0.1	Ceramic	50	20	938406
C43	.001	Ceramic	50	20	938408
C44	.01	Ceramic	50	20	938053
C45	6.8	Tantalum	35	20	938030
C46	6.8	Tantalum	35	20	938030
C47	.01	Ceramic	50	20	938053
C48	.01	Ceramic	50	20	938053
C49	6.8	Tantalum	35	20	938030
C50	6.8	Tantalum	35	20	938030
C51	0.1	Ceramic	50	20	938406
C52	.001	Ceramic	50	20	938408
C53	150	Tantalum	6	20	938607
C54	.001	Ceramic	50	20	938408
C55	.01	Ceramic	50	20	938053
C56	33	Tantalum	25	10	938606
C57	6.8	Tantalum	35	20	938030
C58	10p	Ceramic	500	5	917746
C59	0.1	Ceramic	50	20	938406
C60	6.8	Tantalum	35	20	938030
C61	6.8	Tantalum	35	20	938030
C62	0.1	Ceramic	50	20	938406
C63	0.1	Ceramic	50	20	938406
C64	0.1	Ceramic	50	20	938406
C65	0.1	Ceramic	50	20	938406
C66	0.1	Ceramic	50	20	938406
C67	0.1	Ceramic	50	20	938406
C68	0.1	Ceramic	50	20	938406
C69	0.1	Ceramic	50	20	938406
C70	0.1	Ceramic	50	20	938406

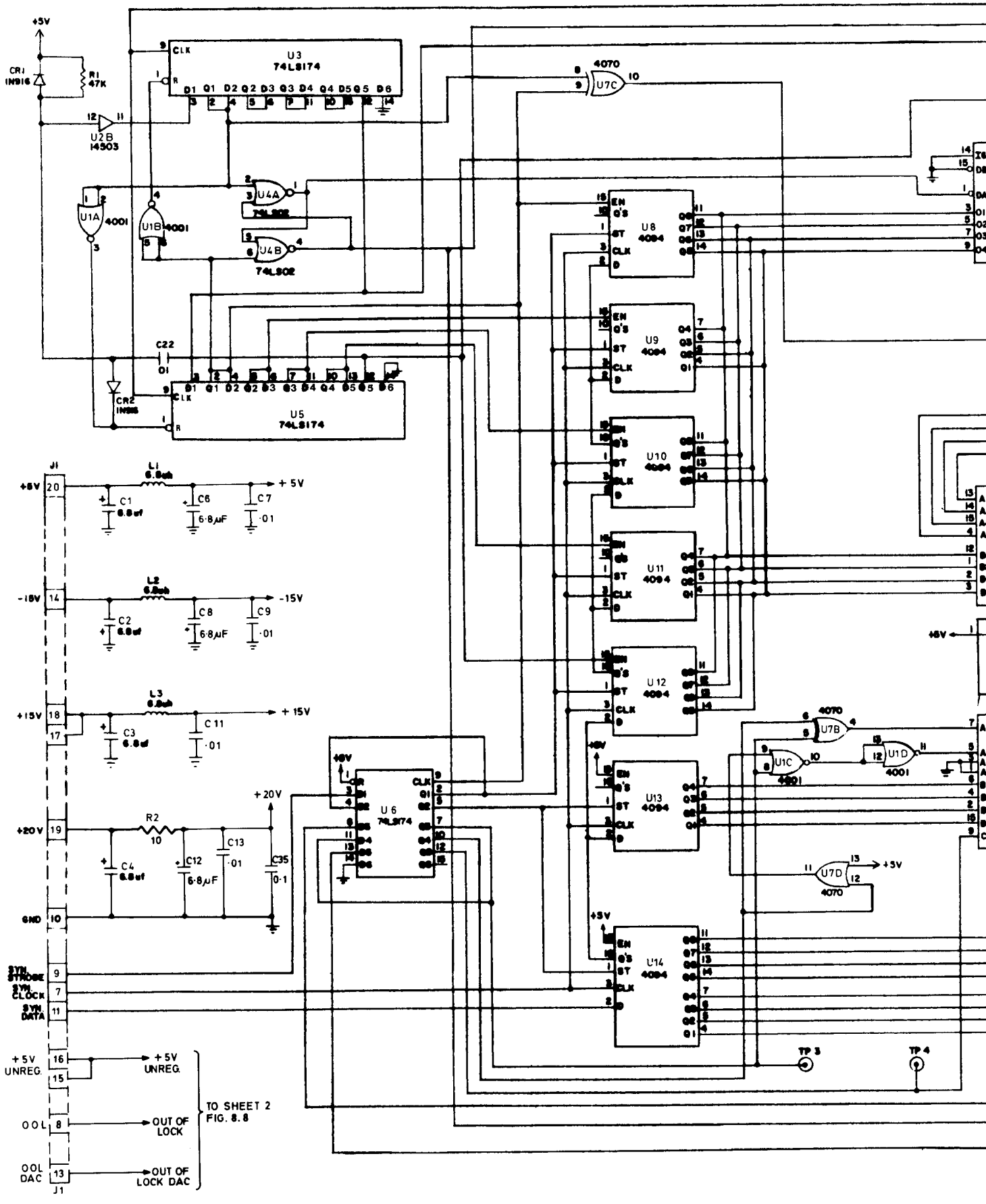
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C71	0.1	Ceramic	50	20	938406
C72	0.1	Ceramic	50	20	938406
C73	0.1	Ceramic	50	20	938406
C74	0.1	Ceramic	50	20	938406
C75	0.1	Ceramic	50	20	938406
C76	0.1	Ceramic	50	20	938406
C77	0.1	Ceramic	50	20	938406
C78	100p	Mica	350	5	938510
C79	6.8	Tantalum	35	20	938030
C80	27p	Mica	350	1p	902220
C81	.001	Polyester	400	10	938671
C82	.047	Polycarbonate	100	10	931129
C83	6.8	Tantalum	35	20	938030
C84	6.8	Tantalum	35	20	938030
C85	.01	Ceramic	50	20	938053
C86	1.0	Tantalum	35	10	938032
C87	1.0	Tantalum	35	10	938032
C88	15	Tantalum	20	20	910060
C89	.047	Ceramic	50	20	938511
C90	2200p	Ceramic	100	20	937903
C91	4700p	Mica	350	5	906253
C92	2200p	Mica	350	2	902197
C93	0.1	Ceramic	50	20	938406
C94	6.8	Tantalum	35	20	938030
C95	.001	Ceramic	50	20	938408
C96	0.1	Ceramic	50	20	938406
C97	1.0	Polycarbonate	100	20	923370
C98	3.3	Polycarbonate	63	10	938673
C99	.068	Polycarbonate	100	10	938672
C100	4.7p	Ceramic	100	0.5p	938794
C101	10p	Mica	500	0.5p	921270
C102	10p	Ceramic	500	5	917746
C103	47p	Mica	350	5	908617
C104	47p	Mica	350	5	908617

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Diodes					
CR1		IN 916			913480
CR2		IN 916			913480
CR3		Varactor KV 2201			938614
CR4		Varactor KV 2201			938614
CR5		IN 916			913480
CR6		IN 916			913480
CR7		IN 916			913480
CR8		IN 916			913480
CR9		IN 916			913480
CR10		IN 916			913480
CR11		IN 916			913480
CR12		IN 916			913480
CR13		IN 916			913480
CR14		IN 916			913480
CR15		IN 916			913480
CR16		IN 916			913480
CR17		Not used			
CR18		Zener 9.1V, 400mW, IN 757A			938674
CR19		IN 916			913480
CR20		IN 916			913480
CR21		IN916			913480
CR22		IN916			913480
Transistors					
Q1		FET 2N3823			938592
Q2		NPN RF 2N3866			917219
Q3		NPN RF 2N3866			917219
Q4		NPN Silicon 2N4921			938616
Q5		NPN Silicon 2N2369			906842
Q6		PNP Plastic 2N4126			912678
Q7		PNP Plastic 2N4126			912678
Q8		PNP Plastic 2N4126			912678
Q9		NPN Plastic 2N4124			915617
Q10		NPN Plastic 2N4124			915617
Q11		PNP Plastic 2N4126			912678
Q12		NPN Silicon 2N918			906517
Q13		NPN Silicon 2N2369			906842

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U1		4001			938561
U2		4503			935215
U3		94LS174			938624
U4		74LS02			938531
U5		74LS174			938624
U6		74LS174			938624
U7		* 4070			938837
U8		4094			934550
U9		4094			934550
U10		4094			934550
U11		4094			934550
U12		4094			934550
U13		4094			934550
U14		4094			934550
U15		82583			938622
U16		10k resistor network			938625
U17		4008			938620
U18		* 40174			938838
U19		74LS74			930602
U20		4006			938628
U21		4006			938628
U22		40108			938629
U23		DAC 20			938631
U24		UA 723			925040
U25		Not used			
U26		10231			938630
U27		11C90			938600
U28		10231			938630
U29		74LS169			938627
U30		74LS168			938626
U31		74LS168			938626
U32		10211			938633
U33		1458			938632
U34		LM339			929149
U35		AD518			938634

* Use RCA, Motorola or National only.

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
U36		DG 201			934880
U37		1458			938632
U38		Not used			
U39		7812			938445
U40		3140E			932204
Transformers					
T1		RF wideband			D06467/1
Inductors					
L1	6.8 µH	Choke			919469
L2	6.8µH	Choke			919469
L3	6.8µH	Choke			919469
L4	6.8µH	Choke			919469
L5		Coil Assembly			D08708
L6	15µH	Choke		10	915850
Connectors					
J1		Plug, 20-way			938675
J2		Plug, Coaxial 50 ohms			938429
J3		Plug, Coaxial 50 ohms			938429
J4		Plug, Coaxial 50 ohms			938429



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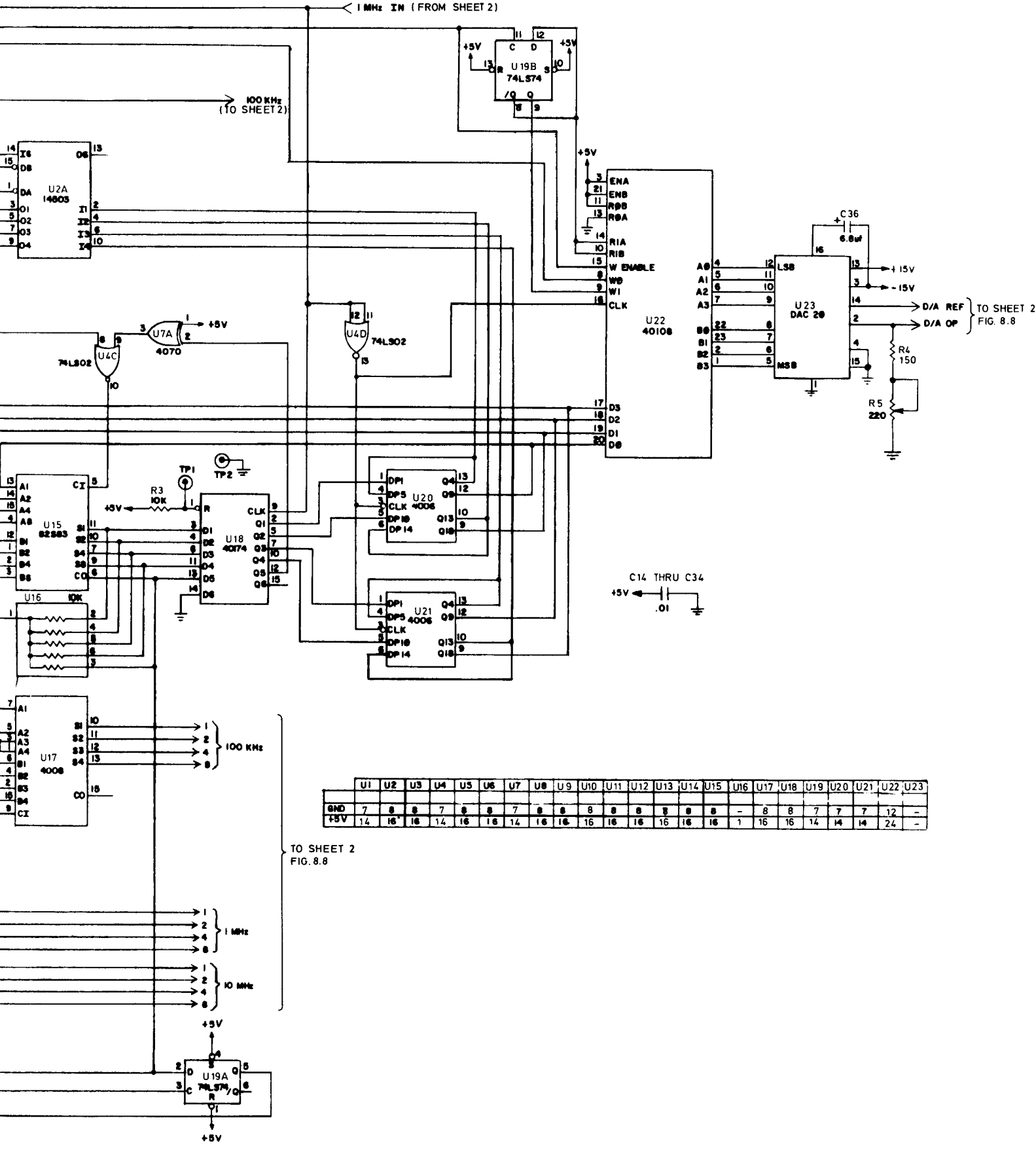
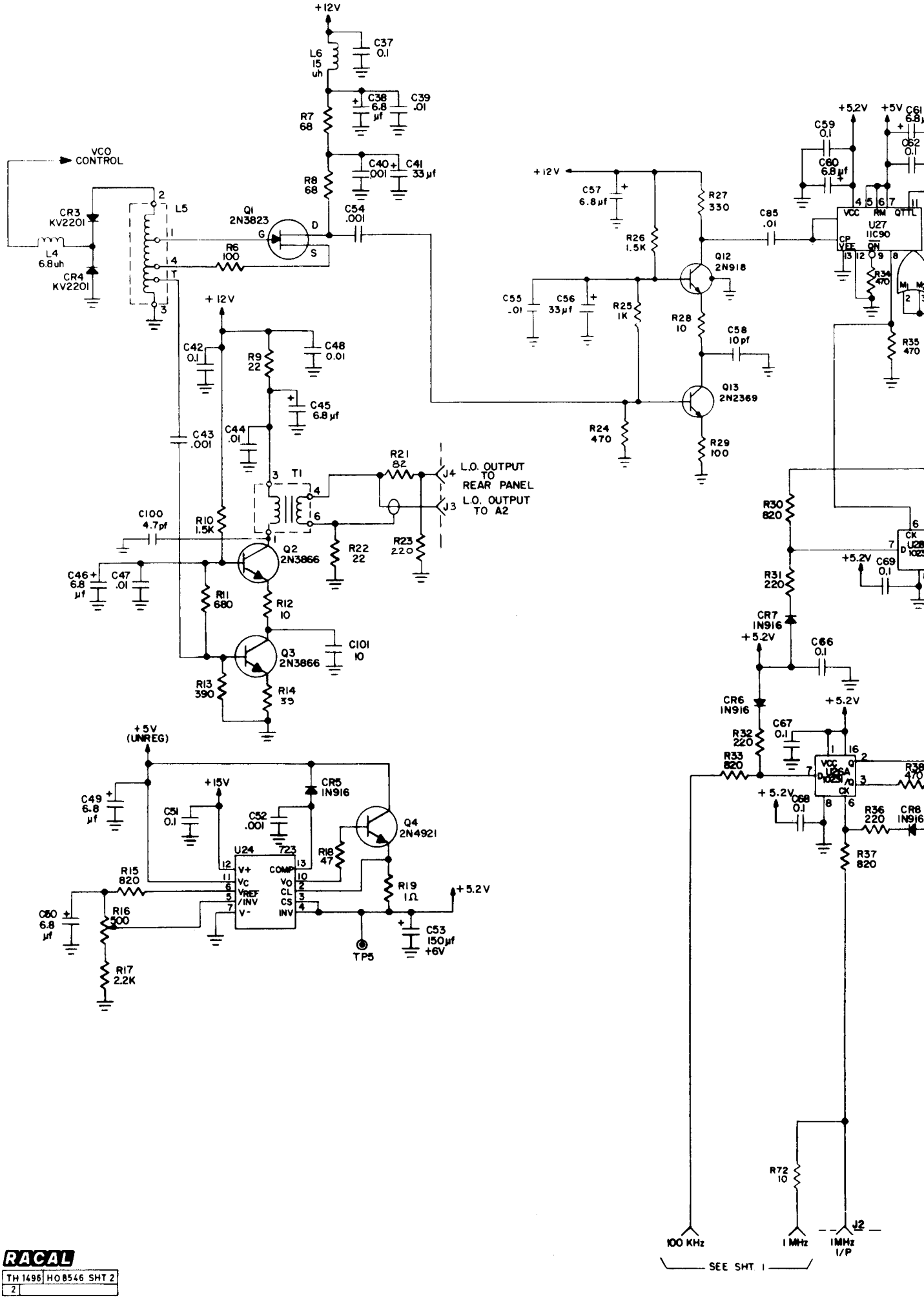
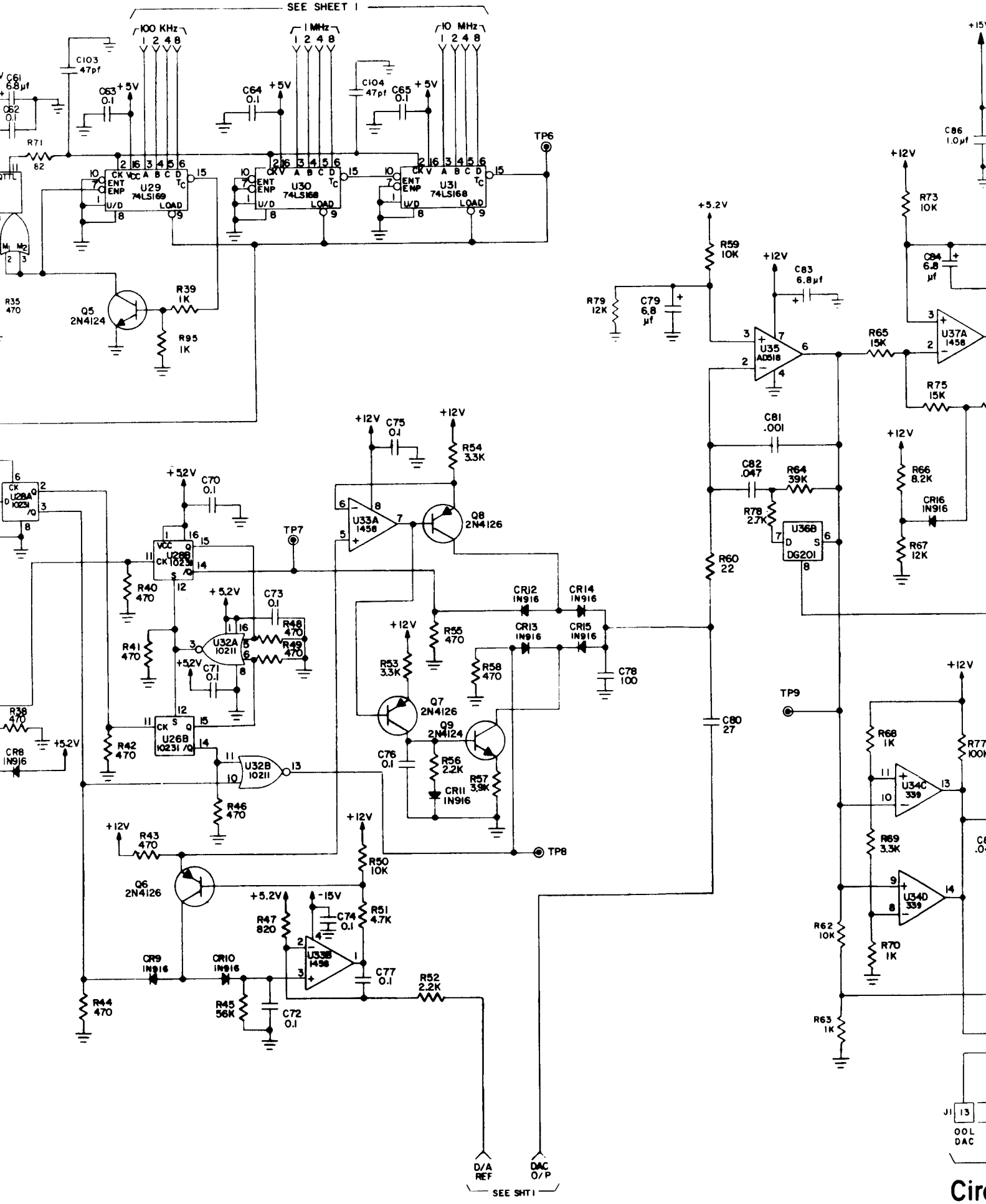
TH 1496	DO8546 SHT 1
2	

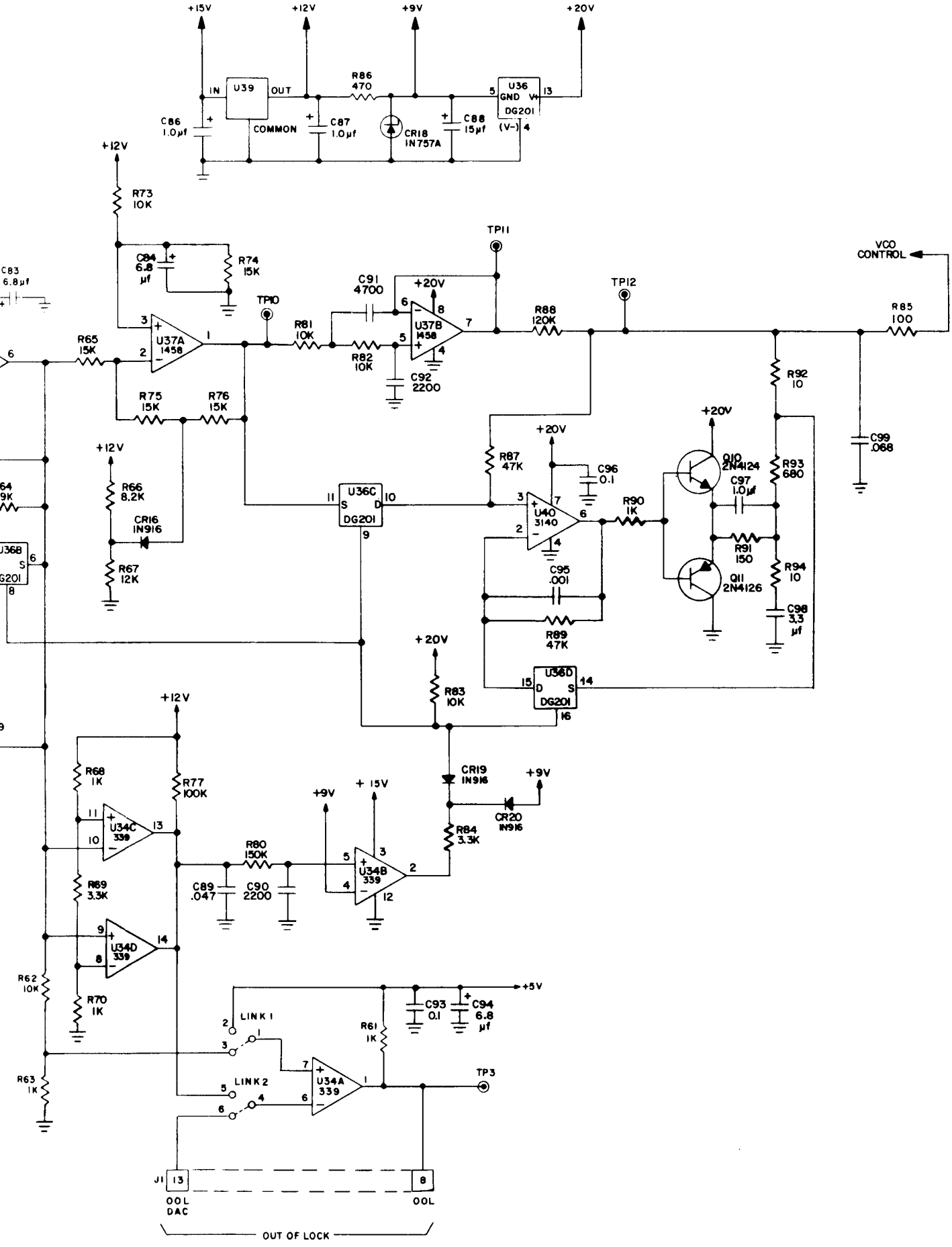


	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23
GND	7	8	8	7	8	8	7	8	8	8	8	8	8	8	8	-	8	8	7	7	7	12	-
+5V	14	16	16	14	16	16	14	16	16	16	16	16	16	16	16	1	16	16	14	14	14	24	-

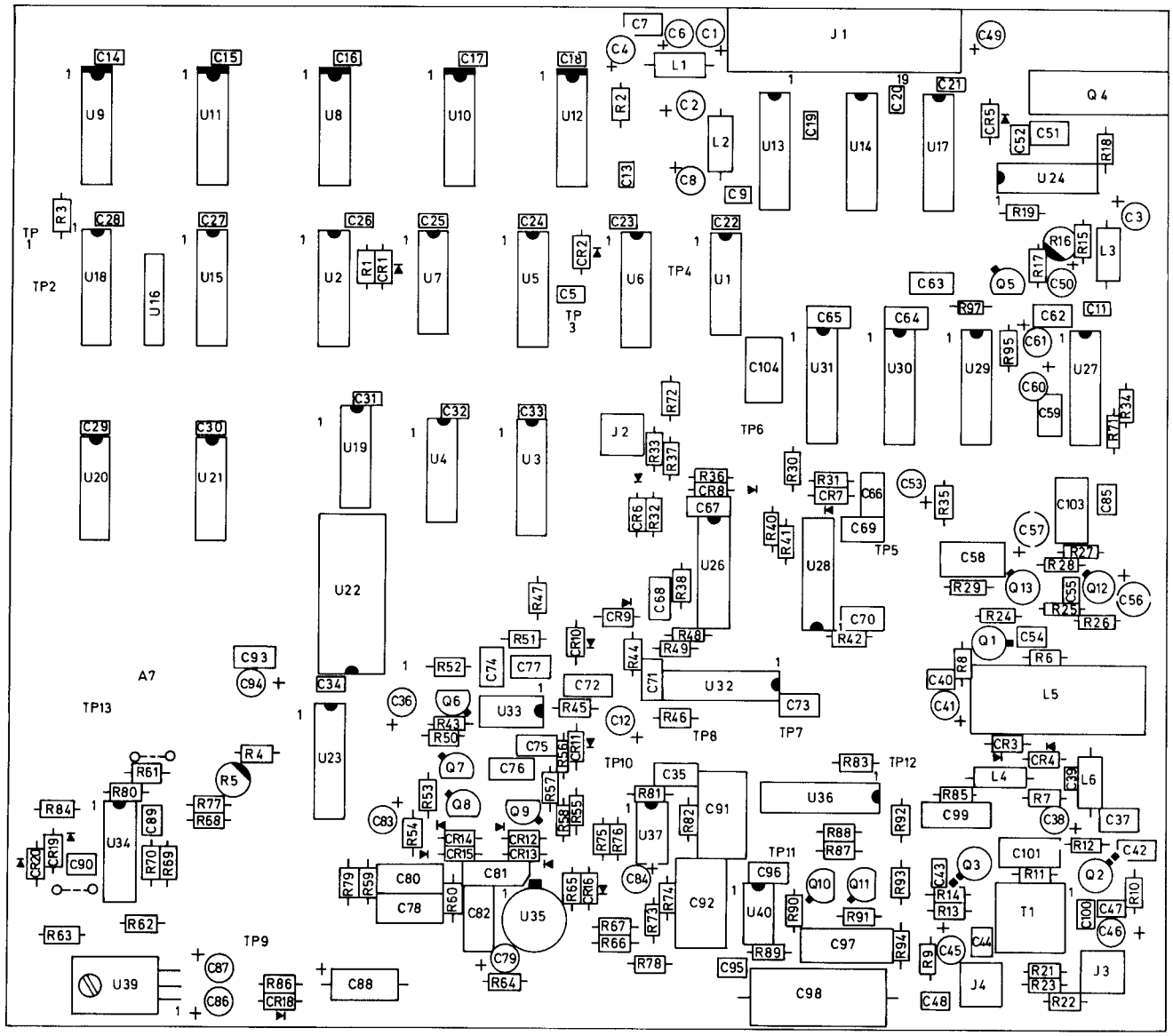
Circuit: First LO Synthesizer Module A7 (Sheet 1) Fig. App. 4.1


+12V
L6 15 uh
C37 0.1
C38 6.8 µf
C39 .01
R7 68
R8 68
C40 .001
C41 33 µf
C54 .001
VCO CONTROL
CR3 KV2201
CR4 KV2201
L4 6.8uh
L5
Q1 2N3823
R6 100
+12V
C42 0.1
R9 22
C48 0.01
C45 6.8 µf
C43 .001
C44 .01
T1
R21 82
J4 L.O. OUTPUT TO REAR PANEL
J3 L.O. OUTPUT TO A2
C100 4.7pf
R10 1.5K
R22 22
R23 220
Q2 2N3866
C46 6.8 µf
C47 .01
R11 680
R12 10
C101 10
Q3 2N3866
R13 390
R14 39
+5V (UNREG)
C49 6.8 µf
+15V
C51 0.1
C52 .001
CR5 IN916
Q4 2N4921
U24 723
R18 47
R15 820
R16 500
R17 2.2K
R19 1Ω
+5.2V
C53 150µf +6V
C60 6.8 µf
TP5
+12V
C57 6.8µf
R27 330
R26 1.5K
Q12 2N918
C55 .01
C56 33µf
R25 1K
R28 10
C58 10pf
Q13 2N2369
R24 470
R29 100
C85 .01
+5.2V
+5V
C59 0.1
C60 6.8µf
C62 0.1
U27 IIC90
R34 470
R35 470
R30 820
R31 220
+5.2V
C69 0.1
CR7 IN916
+5.2V
C66 0.1
CR6 IN916
+5.2V
C67 0.1
R32 220
R33 820
+5.2V
C68 0.1
R36 220
CR8 IN916
R37 820
R72 10
100 KHz
1 MHz
1MHz I/P
J2
SEE SHT 1


SEE SHEET 1
100 KHz
1 MHz
10 MHz
1 2 4 8
C103 47pf
C104 47pf
C63 0.1
C64 0.1
C65 0.1
+5V
R71 82
U29 74LS169
U30 74LS168
U31 74LS168
TP6
R35 470
Q5 2N4124
R39 1K
R95 1K
+12V
C75 0.1
R54 3.3K
+5.2V
C70 0.1
TP7
U33A 1458
Q8 2N4126
U28A 10231
U28B 10231
R40 470
C73 0.1
R48 470
R49 470
U32A 10211
R41 470
C71 0.1
R38 470
CR8 IN916
R42 470
U26B 10231
U32B 10211
R46 470
CR12 IN916
CR14 IN916
CR13 IN916
CR15 IN916
R55 470
R53 3.3K
R58 470
C78 100
Q7 2N4126
Q9 2N4124
C76 0.1
R56 2.2K
R57 3.9K
CR11 IN916
TP8
R43 470
Q6 2N4126
R50 10K
-15V
R47 820
C74 0.1
R51 4.7K
U33B 1458
CR9 IN916
CR10 IN916
C77 0.1
R52 2.2K
R44 470
R45 56K
C72 0.1
D/A REF
DAC O/P
SEE SHT 1
C61 6.8µf
C62 0.1
M1 M2
C86 1.0µf
R73 10K
C84 6.8 µf
C83 6.8µf
+5.2V
R59 10K
R79 12K
C79 6.8 µf
U35 AD518
R65 15K
U37A 1458
R75 15K
C81 .001
C82 .047
R64 39K
R78 2.7K
U36B DG201
R66 8.2K
CR16 IN916
R67 12K
R60 22
C80 27
TP9
R68 1K
U34C 339
R77 100K
R69 3.3K
U34D 339
R62 10K
R70 1K
R63 1K
J1 13
OOL
DAC
Cir



Circuit : First LO Synthesizer Module A7 (Sheet 2) Fig. App. 4.2



Component Layout: First
LO Synthesizer Board A7

Fig. App. 4.3

RACAL
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