

NOTES:

(UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICRO FARADS
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLI HENRIES
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

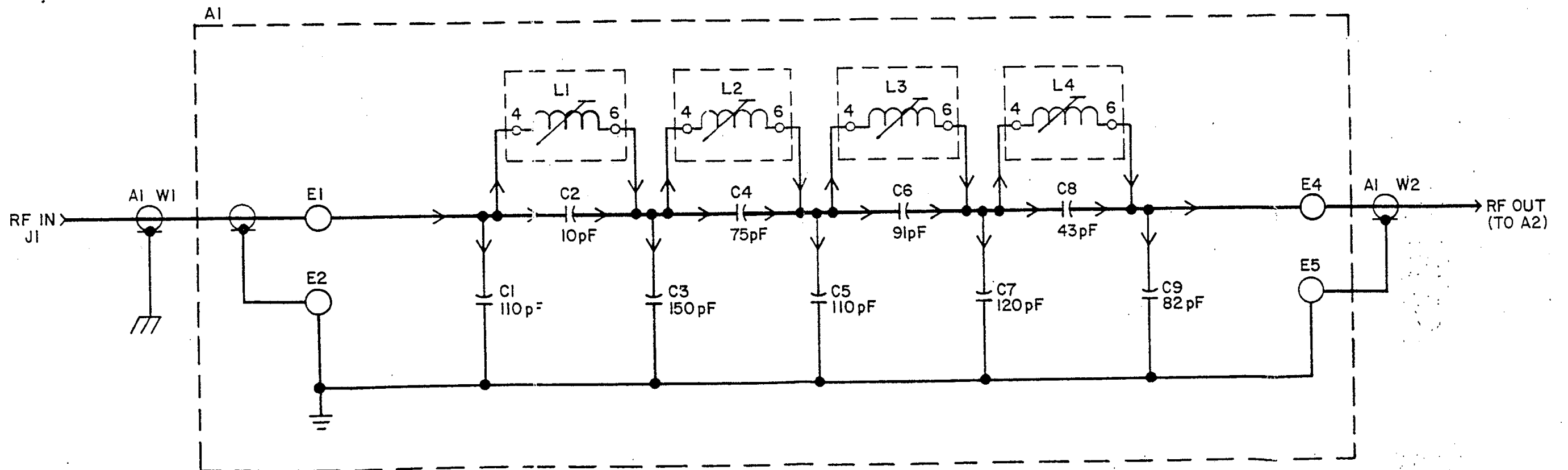
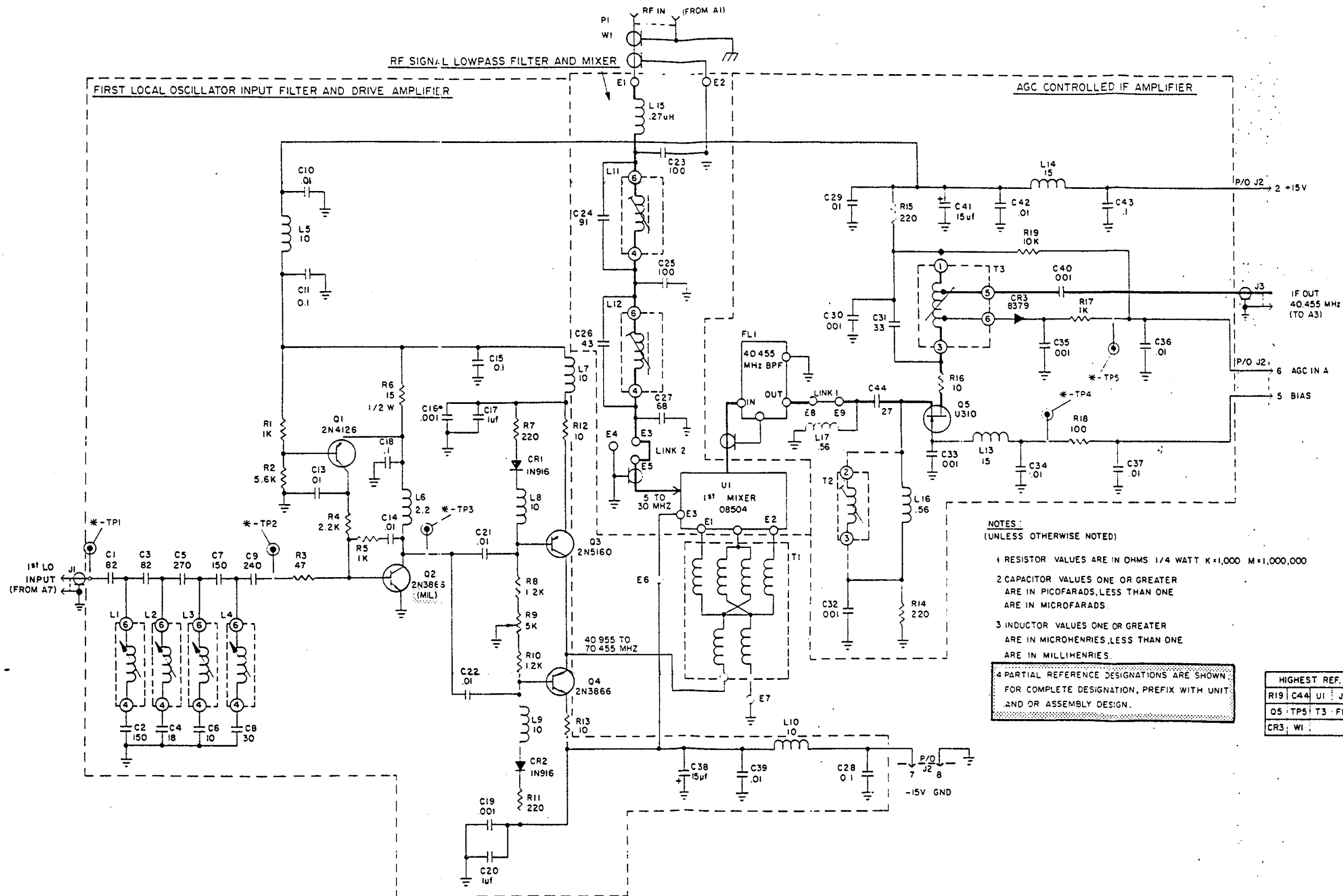


Figure 7-1. Schematic Diagram, RF Low Pass Filter, A1



- NOTES:
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 - 2 CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS
 - 3 INDUCTOR VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.

4 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

HIGHEST REF. DES.				
R19	C44	U1	J3	L17
Q5	TP5	T3	FL1	E9
CR3	W1			

Figure 7-2. Schematic Diagram 1st Mixer, A2

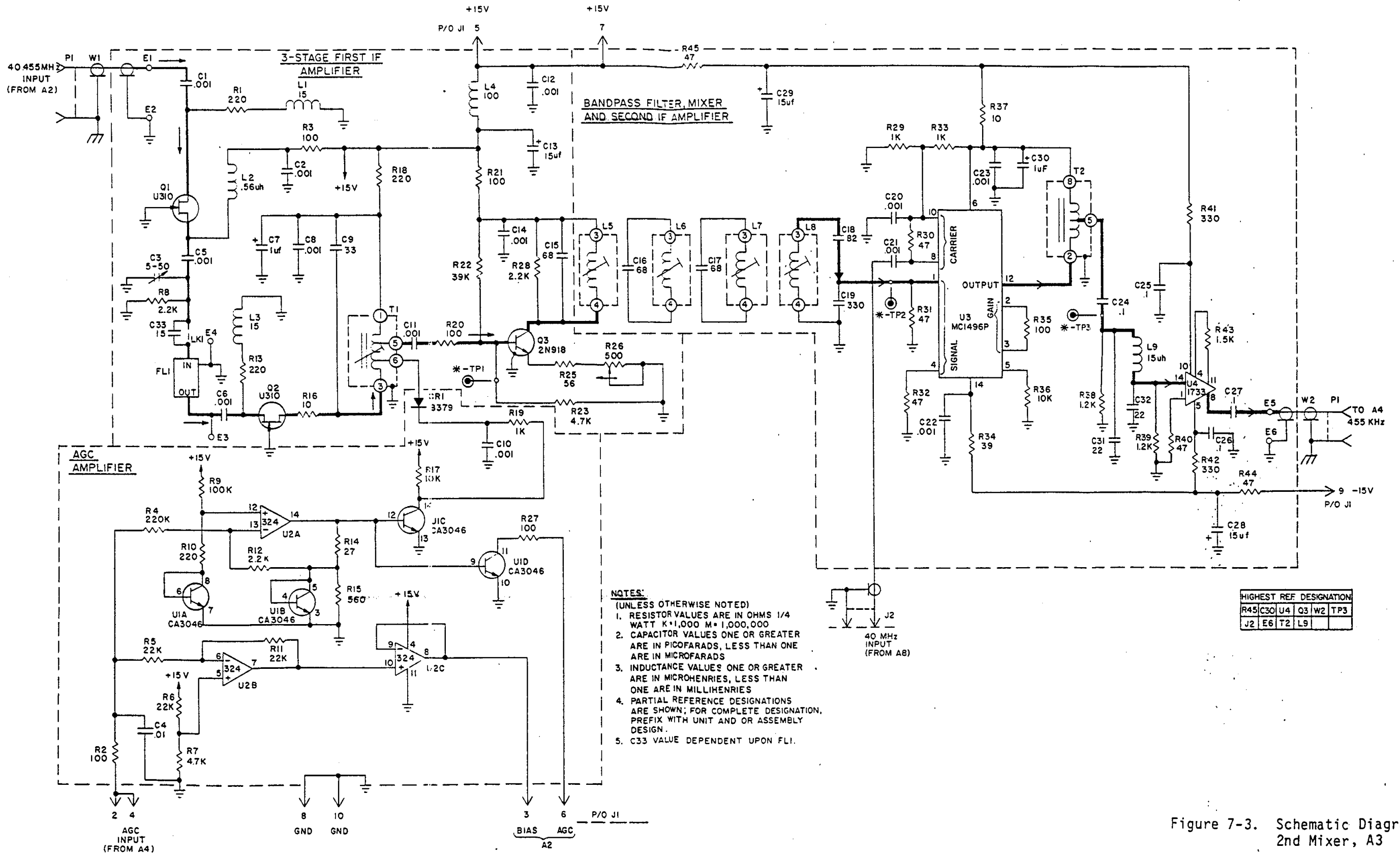
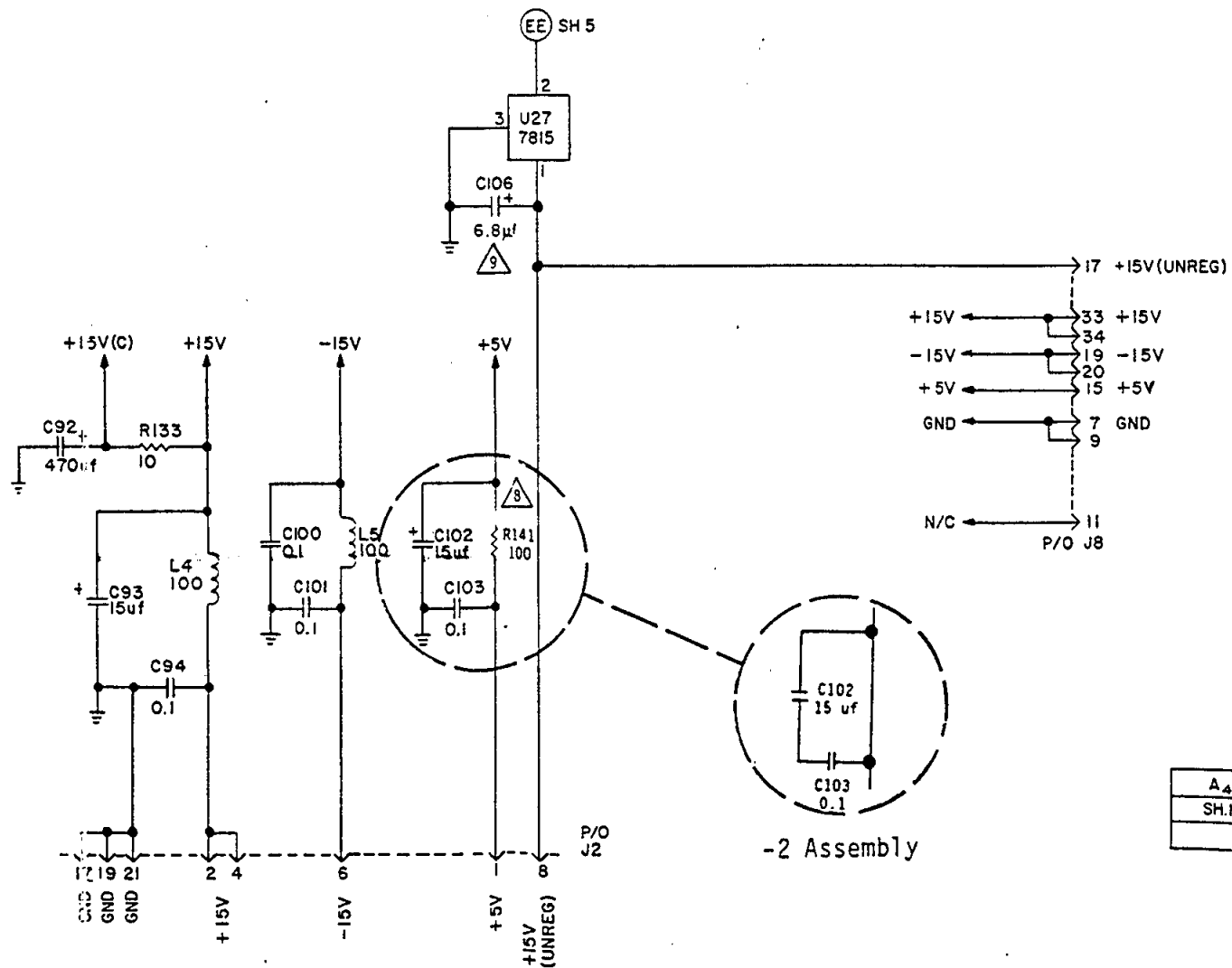


Figure 7-3. Schematic Diagram, 2nd Mixer, A3

NOTES: (UNLESS OTHERWISE NOTED)

1. RESISTOR VALUES ARE IN OHMS, K=1,000, M=1,000,000.
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES LESS THAN ONE ARE IN MILLEHENRIES.
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
5. Δ VALUE DEPENDENT ON FILTER COMPLEMENT.
6. Δ FOR ISB OPERATION CONNECT LINK 1 TO ISB.
7. PROVIDE MUTE ONLY IF MUTE MODULE IS INSTALLED.
8. Δ R141 IS USED ON -1 ASSEMBLY, AND IS DELETED ON -2 ASSEMBLY, AND REPLACED WITH BUSS WIRE AND SLEEVING.
9. Δ C106 IS 68 μ F FOR -2 ASSEMBLY ONLY.

I.C. NO.	DEVICE	GND	+15V (B)	+15V (C)	-15V
U7	324	11		4	
U14	324	11		4	
U17	324	11		4	
U9	4013	7		14	
U11	4066	7		14	
U12	4066	7		14	
U19	4053	6, 7, 8		16	
U22	1458			8	4
U24	339	12		3	
U28	1458		8		4
U29	1458	4	8		



A ₄	A ₄	A ₄	A ₄	A ₄	A ₄
SH.1	SH.2	SH.3	SH.4	SH.5	SH.6

REVISION STATUS OF SHEETS

Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 1 of 6)

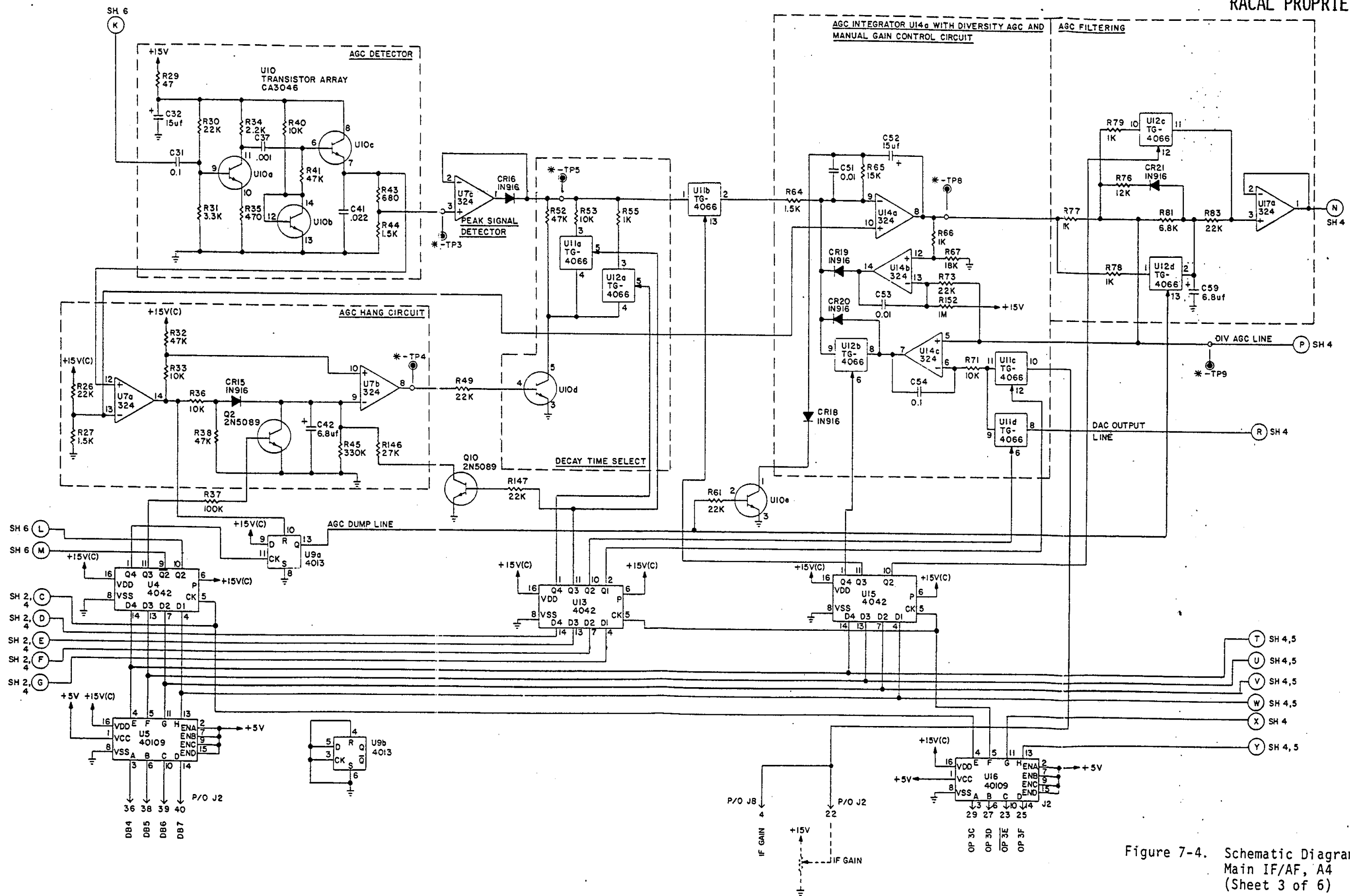


Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 3 of 6)

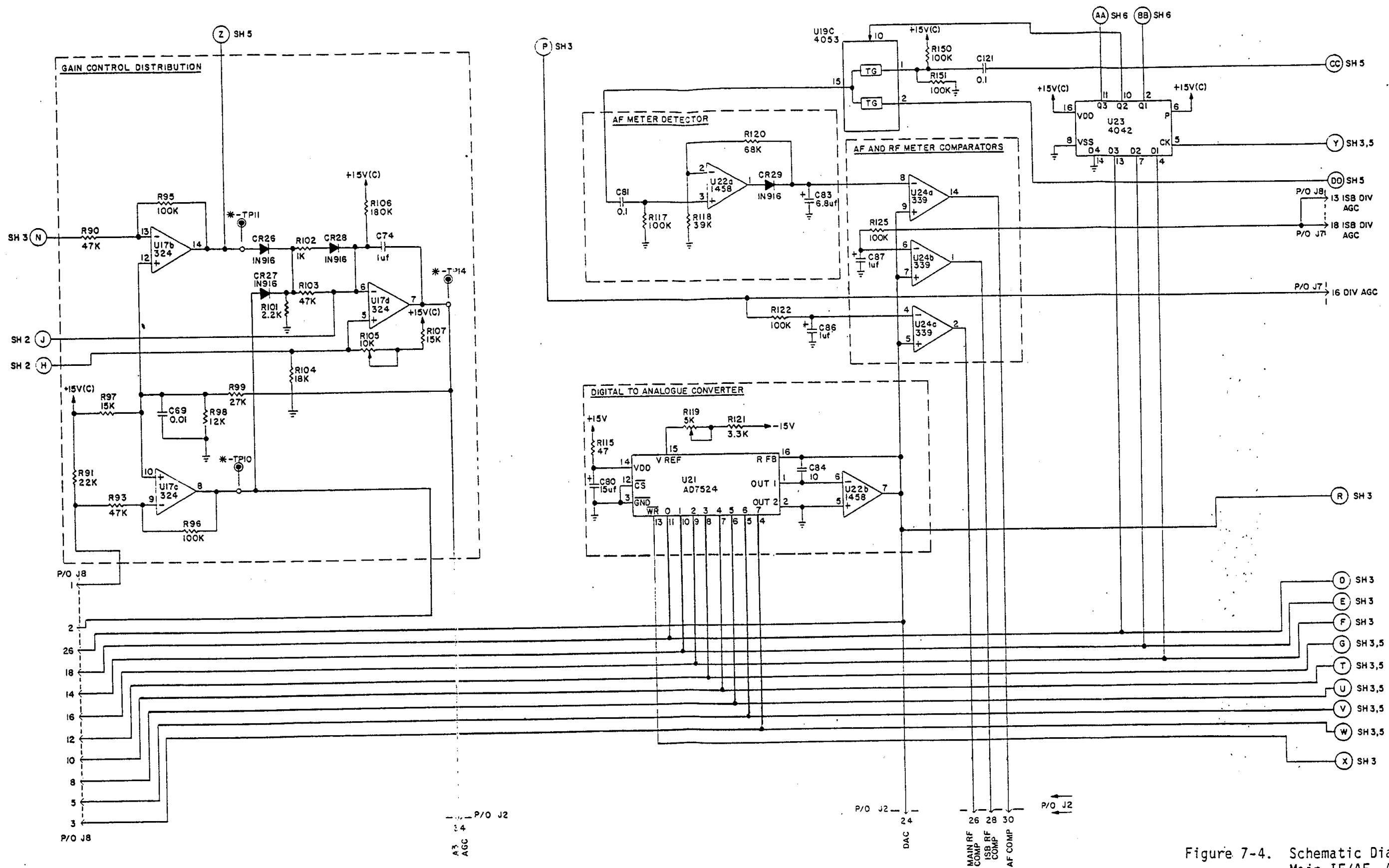


Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 4 of 6)

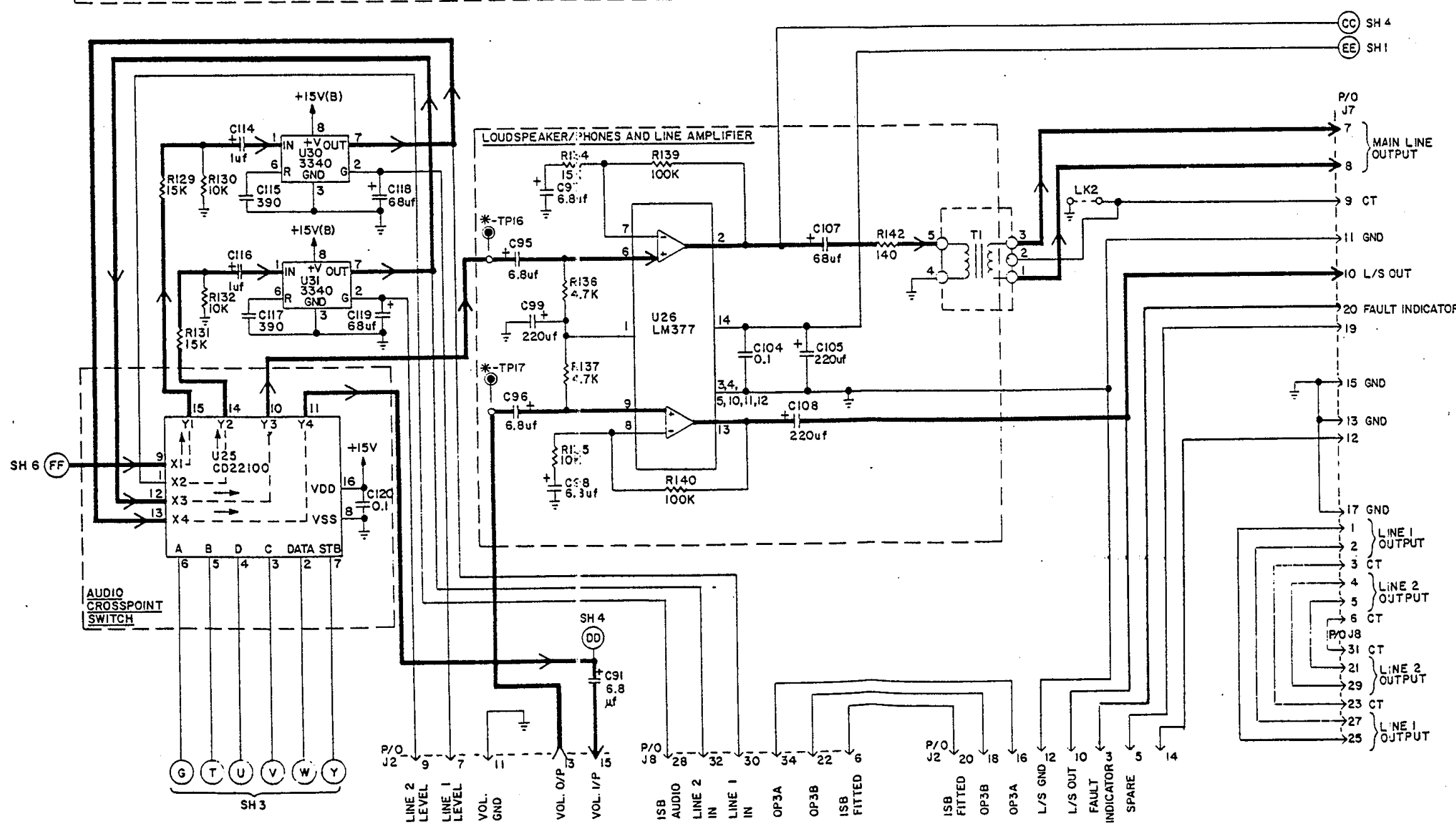
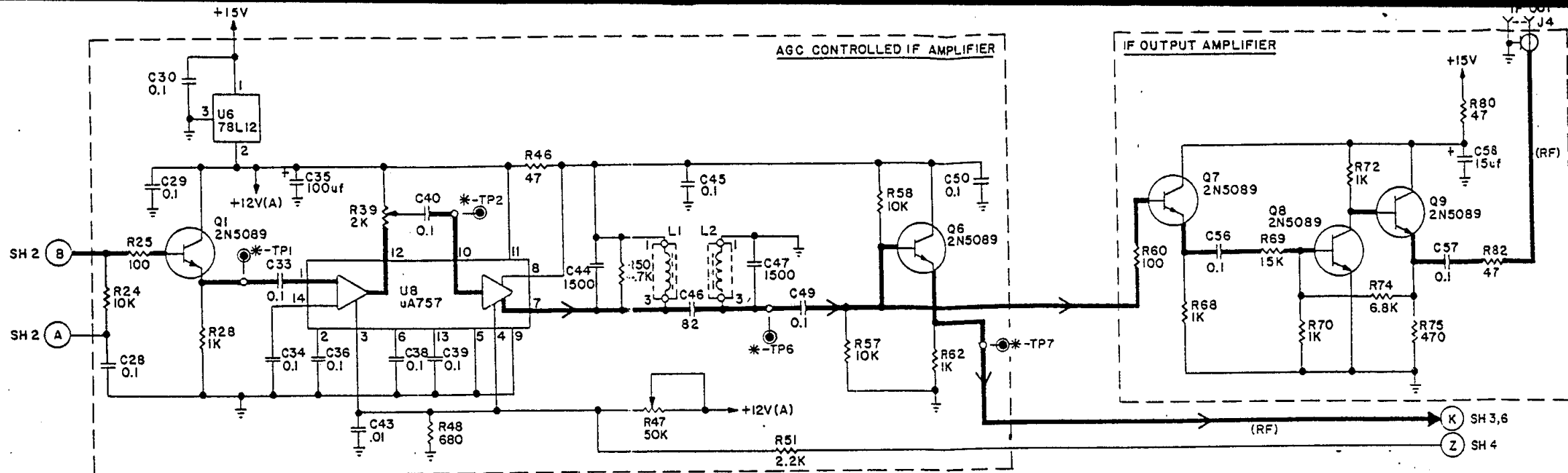


Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 5 of 6)

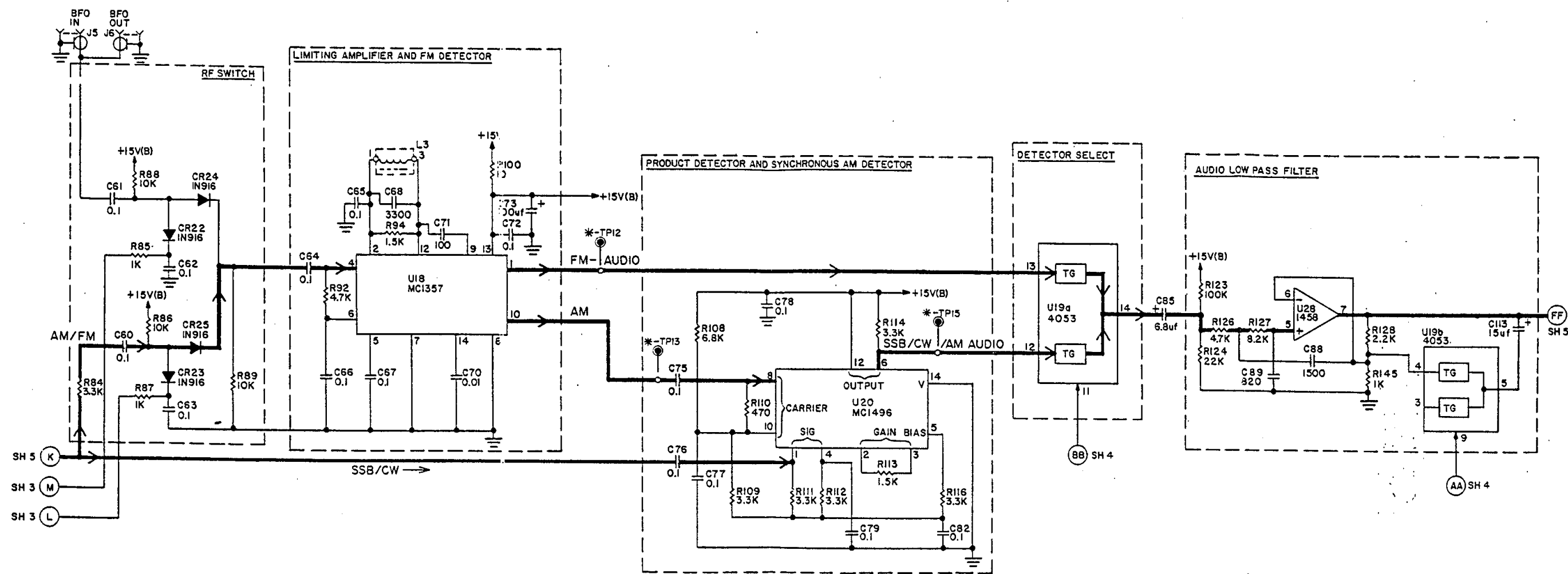
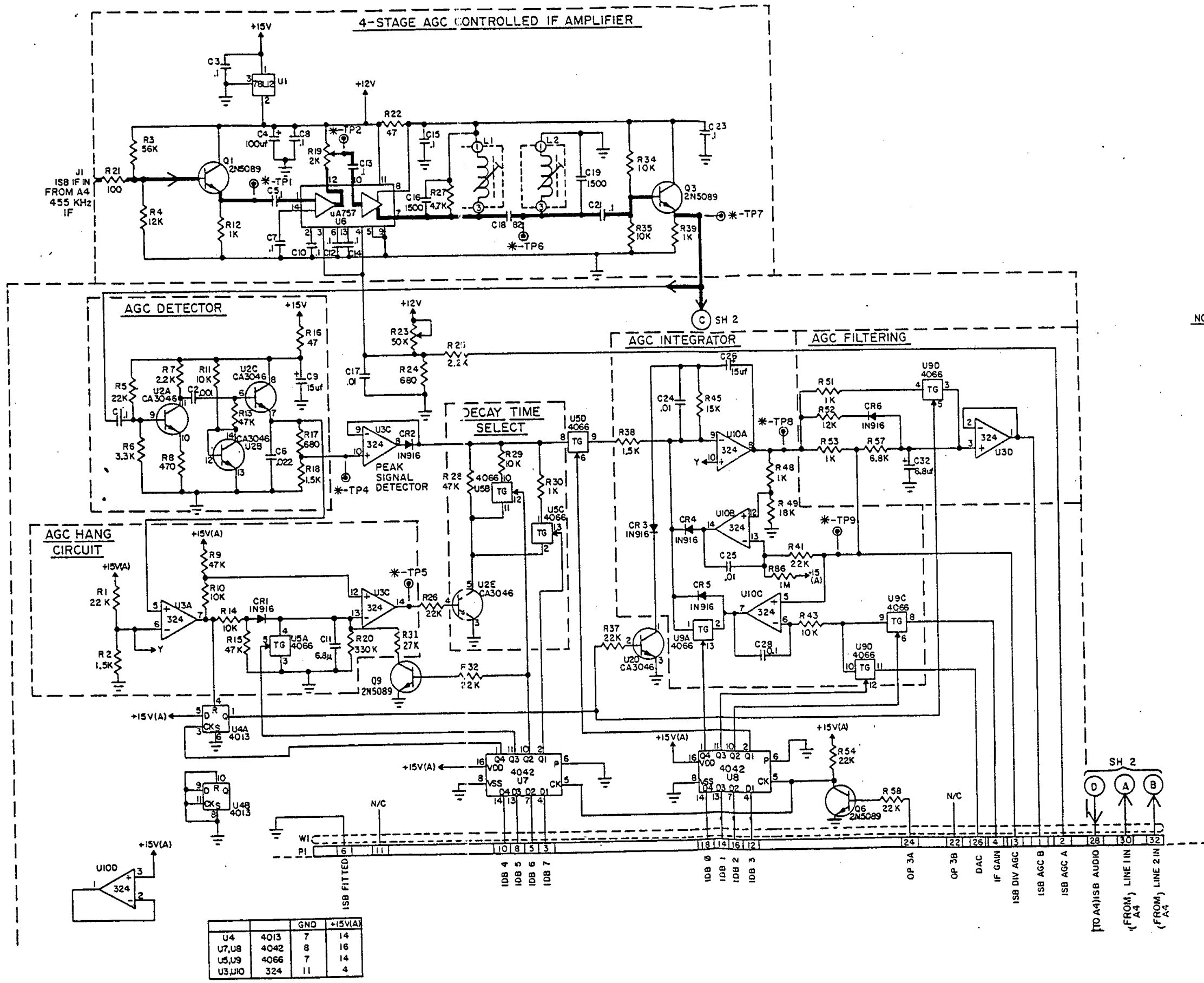


Figure 7-4. Schematic Diagram, Main IF/AF, A4 (Sheet 6 of 6)



- NOTES:
UNLESS OTHERWISE NOTED:
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT
K=1000 M=1,000,000.
 2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
 3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.
 4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

Figure 7-5. Schematic Diagram, ISB, A5 (Optional) (Sheet 1 of 2)

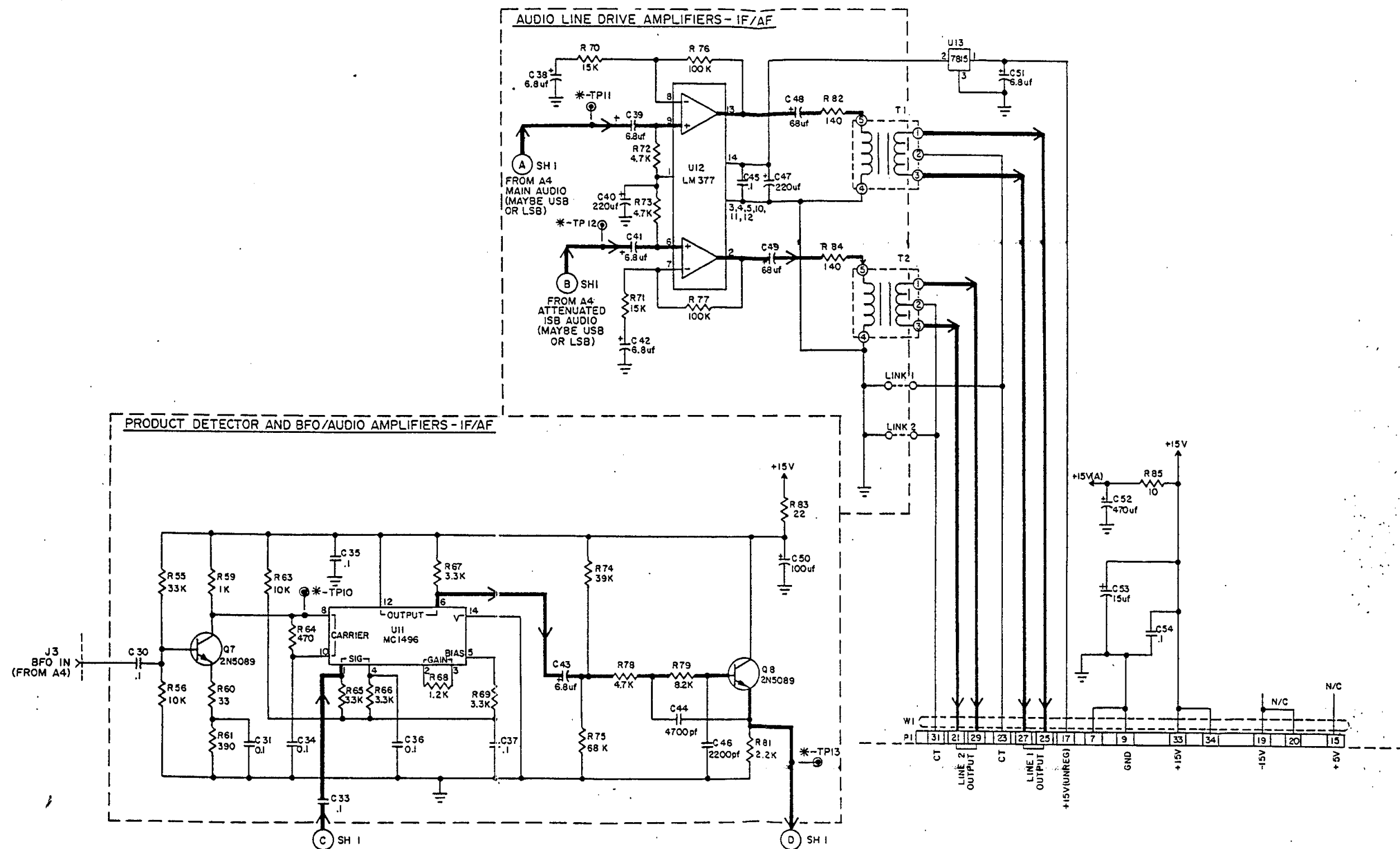


Figure 7-5. Schematic Diagram, ISB, A5 (Optional) (Sheet 2 of 2)

SEE TABLE I

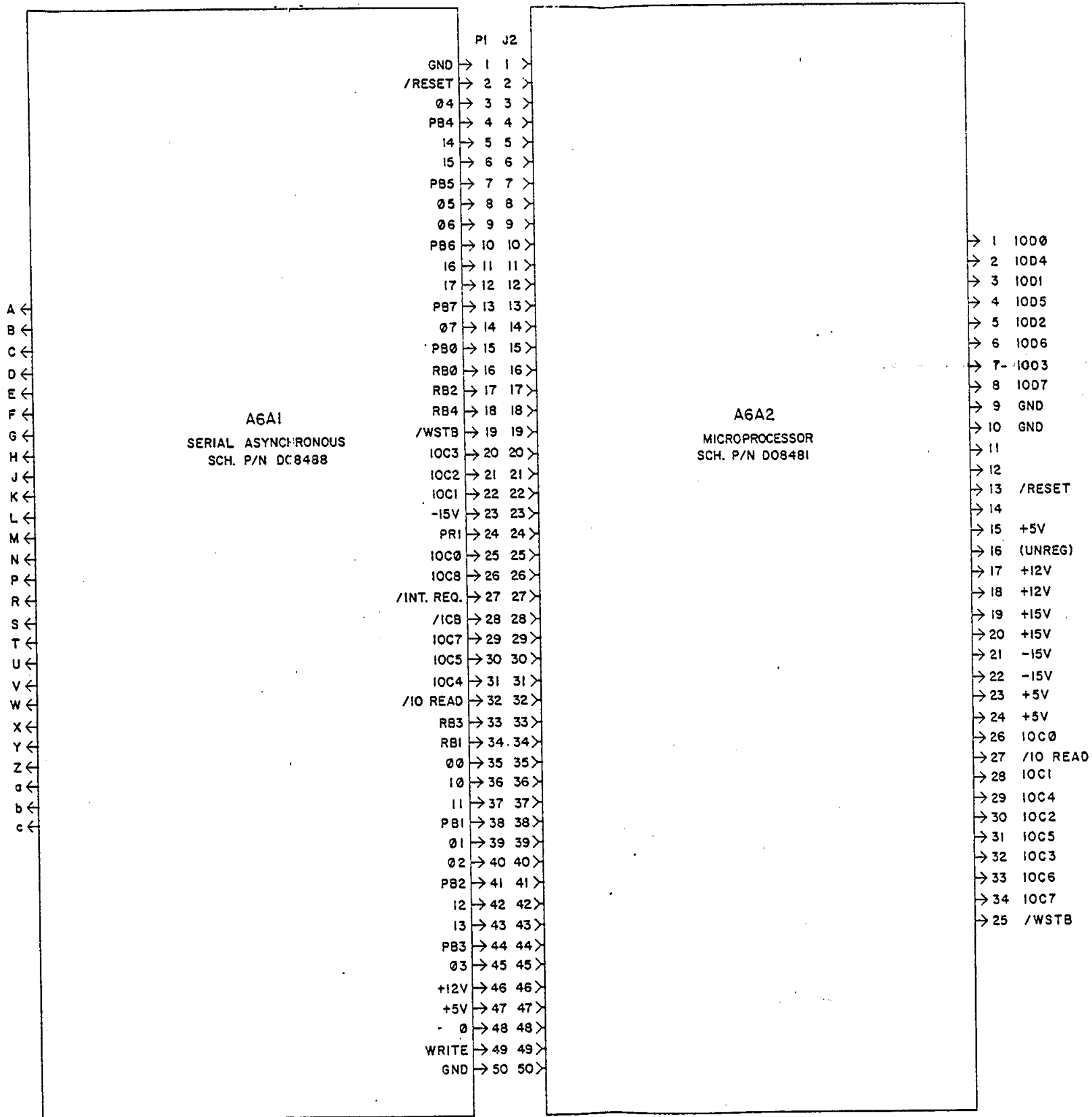
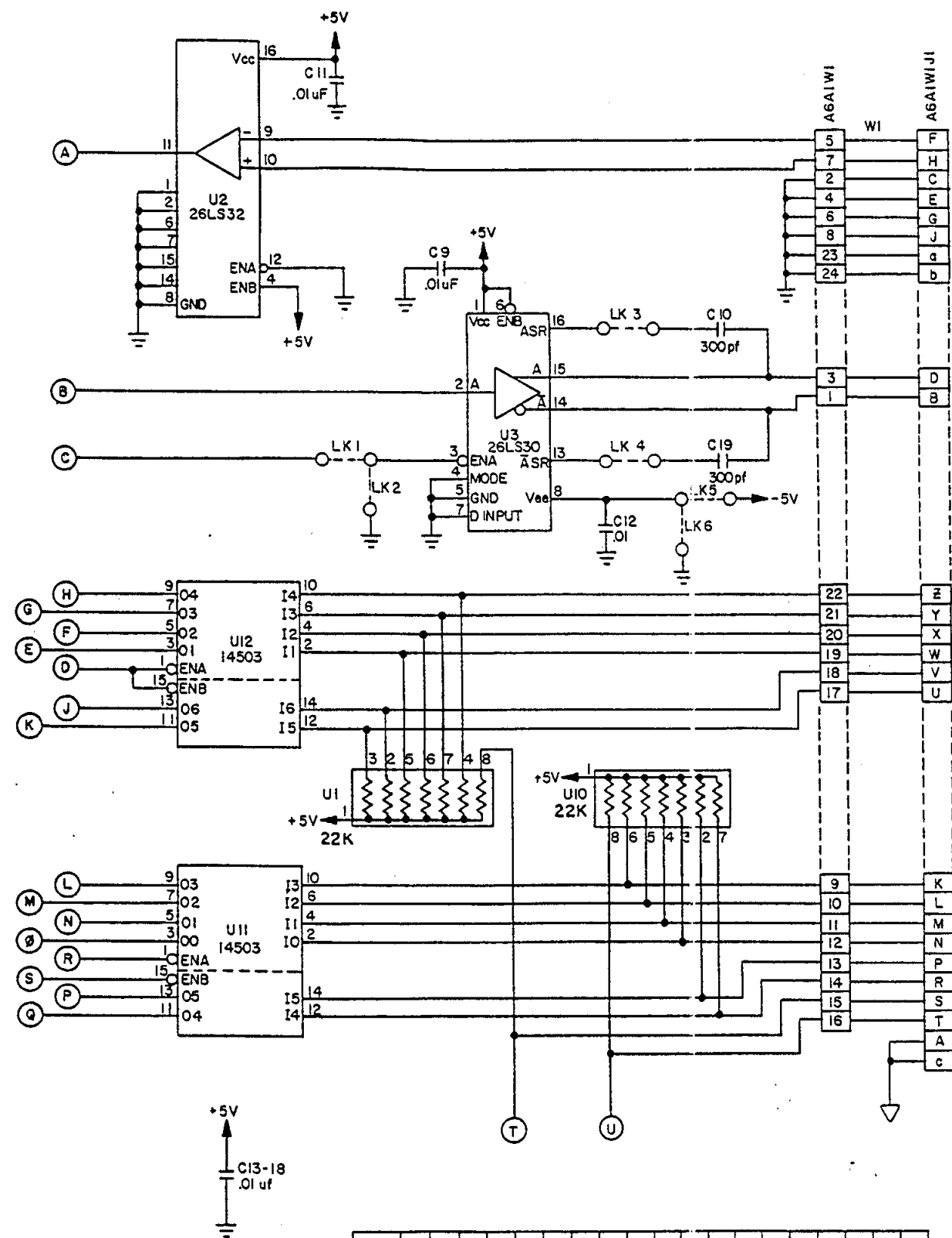


TABLE I

	FUNCTION
A	SYSTEM GND
B	DATA OUT A
C	DATA OUT GND
D	DATA OUT B
E	GND
F	DATA IN A
G	DATA IN GND
H	DATA IN B
J	GND
K	RECEIVER NUMBER DI-1
L	RECEIVER NUMBER DI-2
M	RECEIVER NUMBER DI-4
N	RECEIVER NUMBER DI-8
P	RECEIVER NUMBER D2-1
R	RECEIVER NUMBER D2-2
S	RECEIVER NUMBER D2-4
T	RECEIVER NUMBER D2-8
U	/ PARITY SELECT
V	EVEN/ODD PARITY
W	BAUD RATE B4
X	BAUD RATE B3
Y	BAUD RATE B2
Z	BAUD RATE B1
a	GND
b	GND
c	SYSTEM GND

Figure 7-6. Schematic Diagram, Microcomputer Assembly, A6



	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19
GND	-	8	5	11	1	7	7	7	3	-	1	8	8	8	7	8	7	-	8
+5V	1	16	1	2	-	14	14	14	1	1	3	16	16	16	14	16	14	1	16
+12V	-	-	-	9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-5V	-	-	8	-	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-

TABLE I

J1 PINS	FUNCTION
A	SYSTEM GND
B	DATA OUT A
C	DATA OUT GND
D	DATA OUT B
E	GND
F	DATA IN A'
G	DATA IN GND
H	DATA IN B'
J	GND
K	RECEIVER NUMBER D1-1
L	RECEIVER NUMBER D1-2
M	RECEIVER NUMBER D1-4
N	RECEIVER NUMBER D1-8
P	RECEIVER NUMBER D2-1
R	RECEIVER NUMBER D2-2
S	RECEIVER NUMBER D2-4
T	RECEIVER NUMBER D2-8
U	/PARITY SELECT
V	EVEN/ODD PARITY
W	BAUD RATE B4
X	BAUD RATE B3
Y	BAUD RATE B2
Z	BAUD RATE B1
a	GND
b	GND
c	SYSTEM GND

TABLE II DATA CONNECTION

J1 PINS	MS188C	RS232C RS423	RS422
A	SYSTEM GND	SYSTEM GND	SYSTEM GND
B	NU.	DATA OUT A	DATA OUT A
C	DATA OUT GND	DATA OUT GND	NU.
D	DATA OUT	NU.	DATA OUT B
E	JUMPER TO F	NU.	NU.
F	JUMPER TO E	DATA IN A'	DATA IN A'
G	DATA IN GND	DATA IN GND	NU.
H	DATA IN	JUMPER TO J	DATA IN B'
J	NU.	JUMPER TO H	NU.

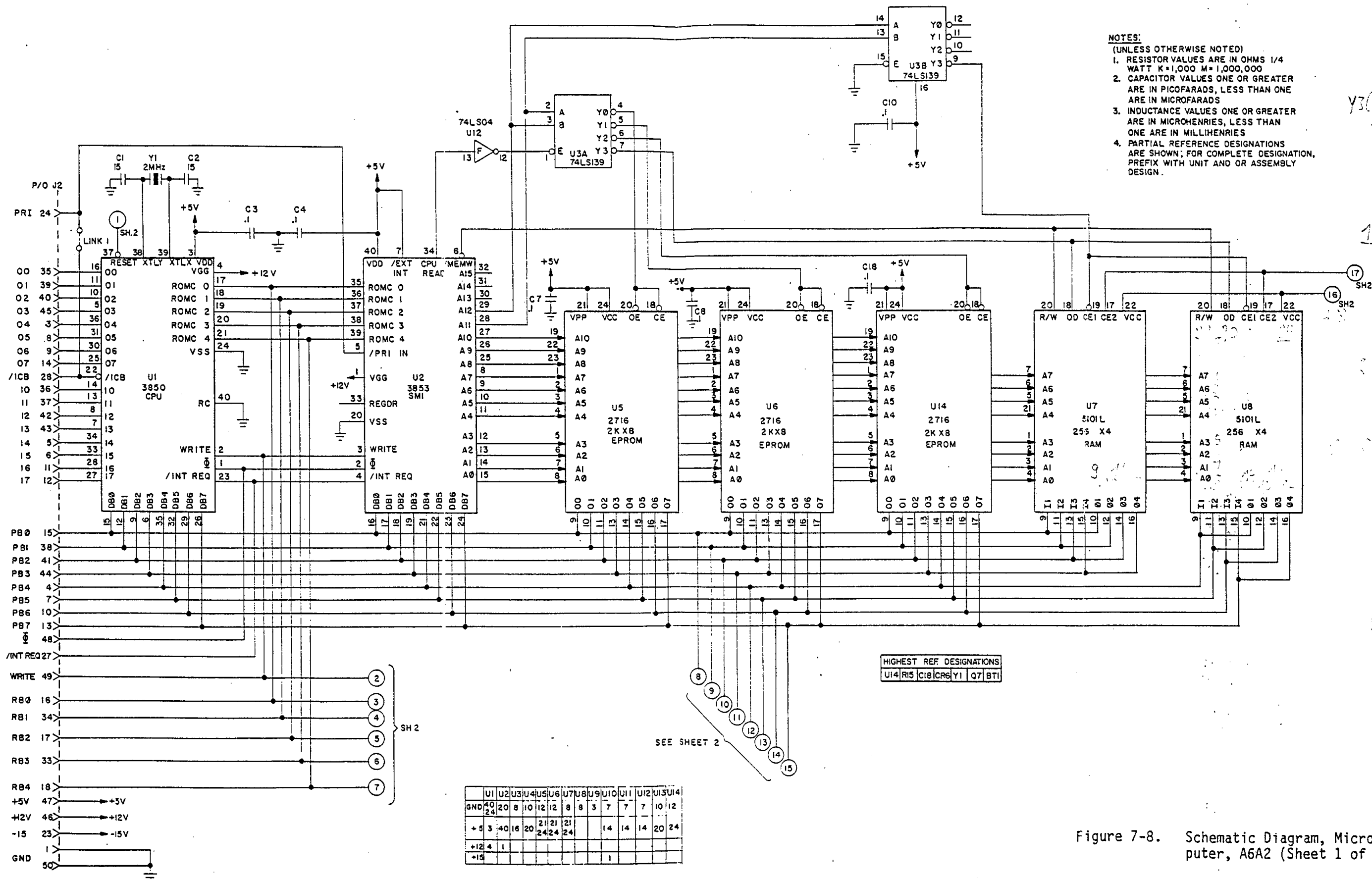
TABLE III BAUD RATE SELECTION

DATA RATE SELECTION BIT	DATA RATE (BAUD)
W X Y Z	
0 0 0 0	50
0 0 0 1	75
0 0 1 0	110
0 0 1 1	134.5
0 1 0 0	150
0 1 0 1	300
0 1 1 0	600
0 1 1 1	1200
1 0 0 0	1800
1 0 0 1	2000
1 0 1 0	2400
1 0 1 1	3600
1 1 0 0	4800
1 1 0 1	7200
1 1 1 0	9600
1 1 1 1	19,200

TABLE IV

LINK NO.	188C/232C/423	422
LK1	INSTALL	INSTALL
LK2	DELETE	DELETE
LK3	INSTALL	DELETE
LK4	INSTALL	DELETE
LK5	INSTALL	DELETE
LK6	DELETE	INSTALL

Figure 7-7. Schematic Diagram, Serial Asynchronous Interface, A6A1 (Optional) (Sheet 2 of 2)



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 3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
 4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.

Figure 7-8. Schematic Diagram, Microcomputer, A6A2 (Sheet 1 of 2)

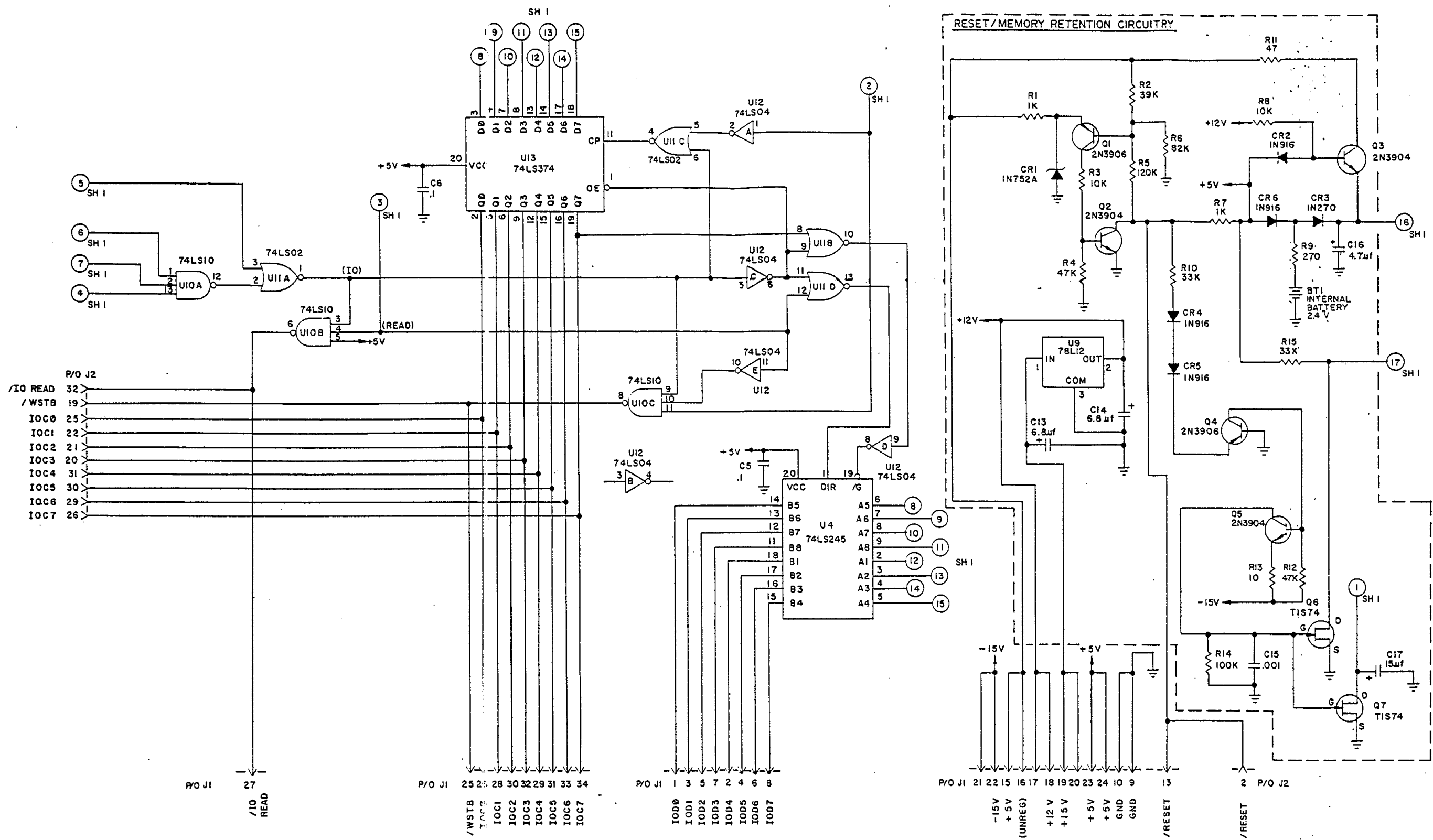
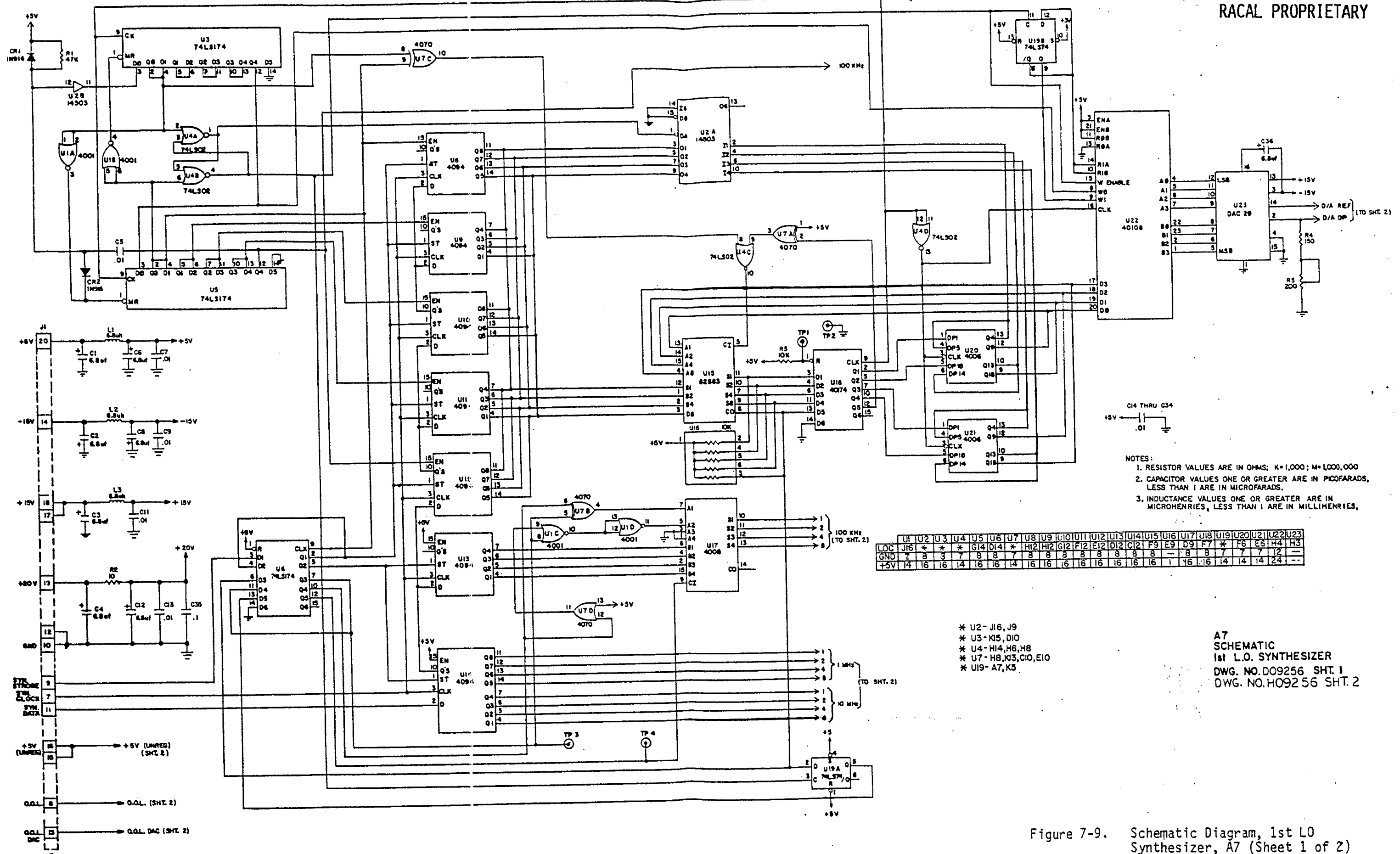


Figure 7-8. Schematic Diagram, Microcomputer, A6A2 (Sheet 2 of 2)



- NOTES:
 1. RESISTOR VALUES ARE IN OHMS; K=1,000; M=1,000,000
 2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN 1 ARE IN MICROFARADS.
 3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN 1 ARE IN MILLIHENRIES.

U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23	
LOC	J16	*	*	*	G14	D14	*	H12	H12	G12	F12	E12	D12	C12	F9	E9	D9	F7	*	F6	E6	H4	H3
GND	7	8	3	7	8	8	7	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
+5V	14	16	16	14	16	16	14	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	

- * U2 - J16, J9
- * U3 - K15, D10
- * U4 - H14, H6, H8
- * U7 - H8, K13, C10, E10
- * U19 - A7, K5

A7
 SCHEMATIC
 1st L.O. SYNTHESIZER
 DWG. NO. D09256 SHT. 1
 DWG. NO. H09256 SHT. 2

Figure 7-9. Schematic Diagram, 1st L.O. Synthesizer, A7 (Sheet 1 of 2)

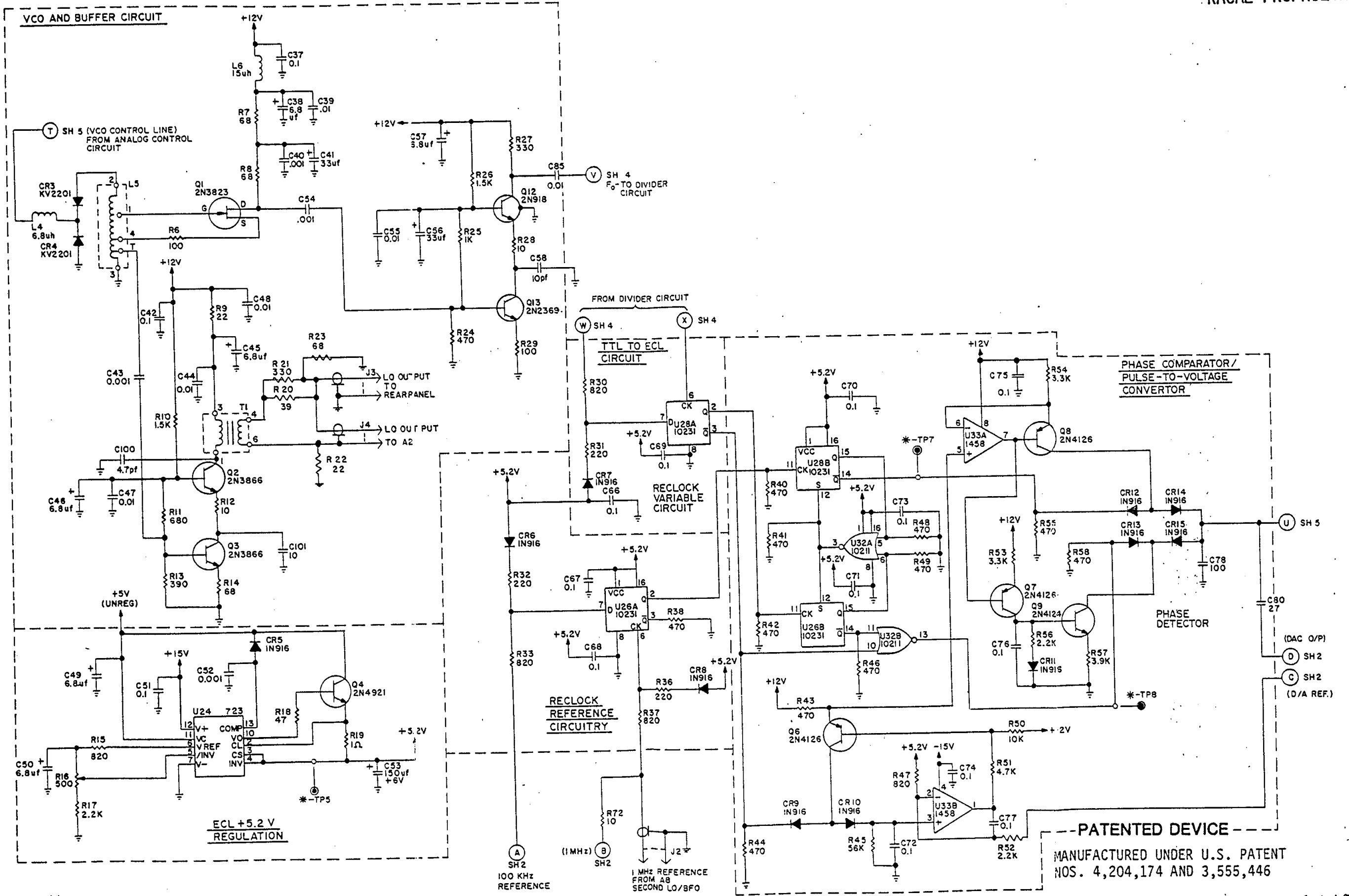
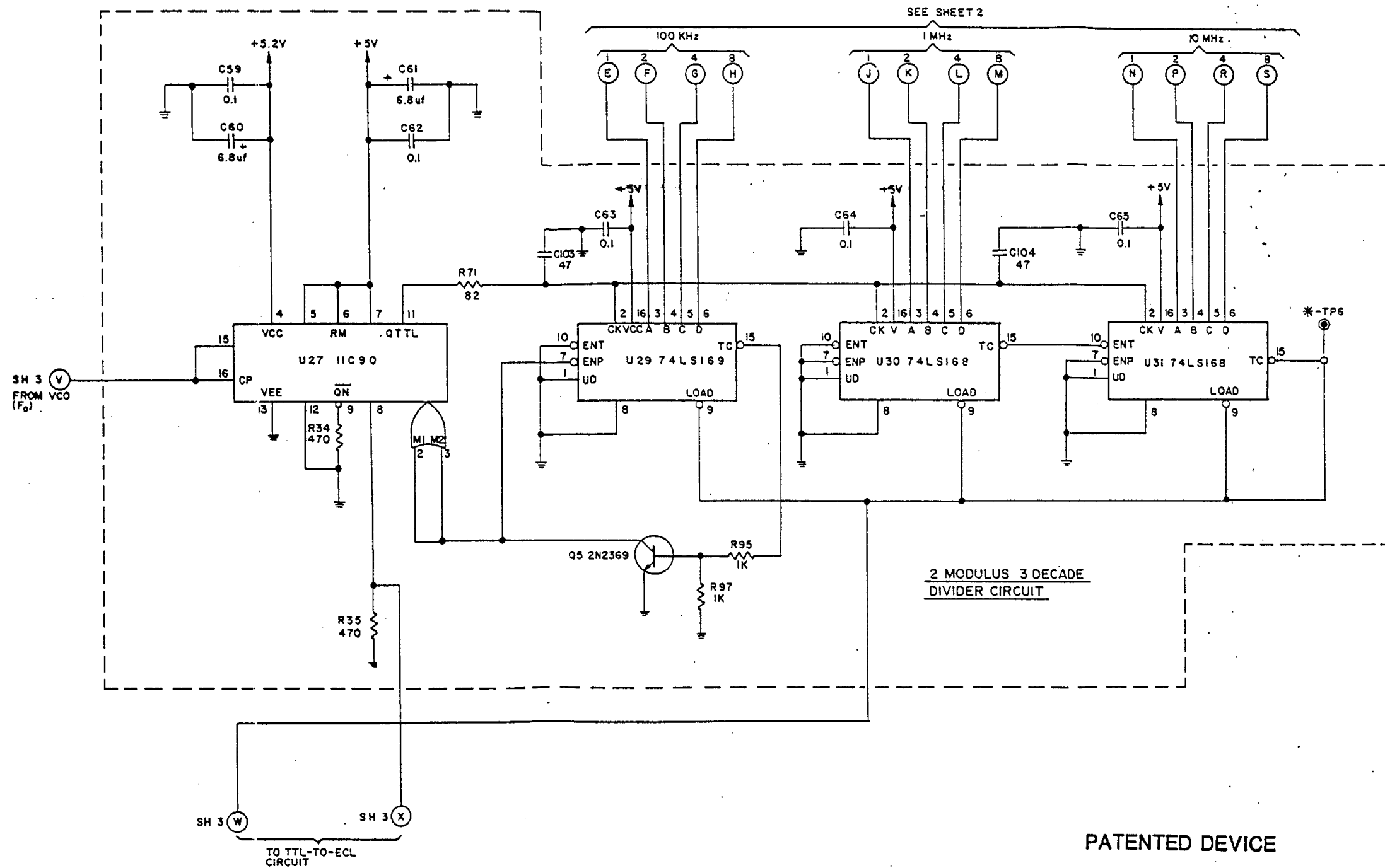


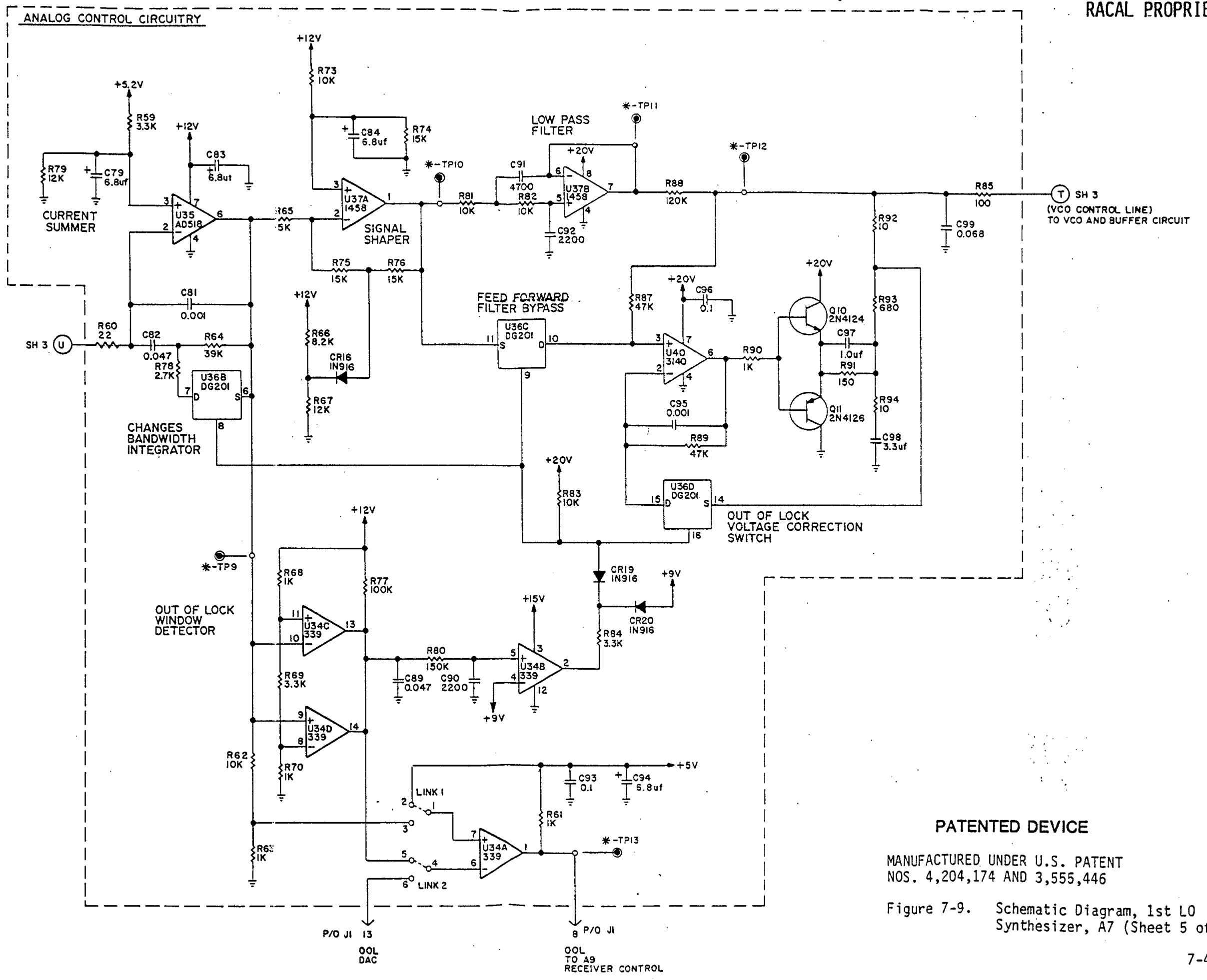
Figure 7-9. Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 3 of 5)



PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT
 NOS. 4,204,174 AND 3,555,446

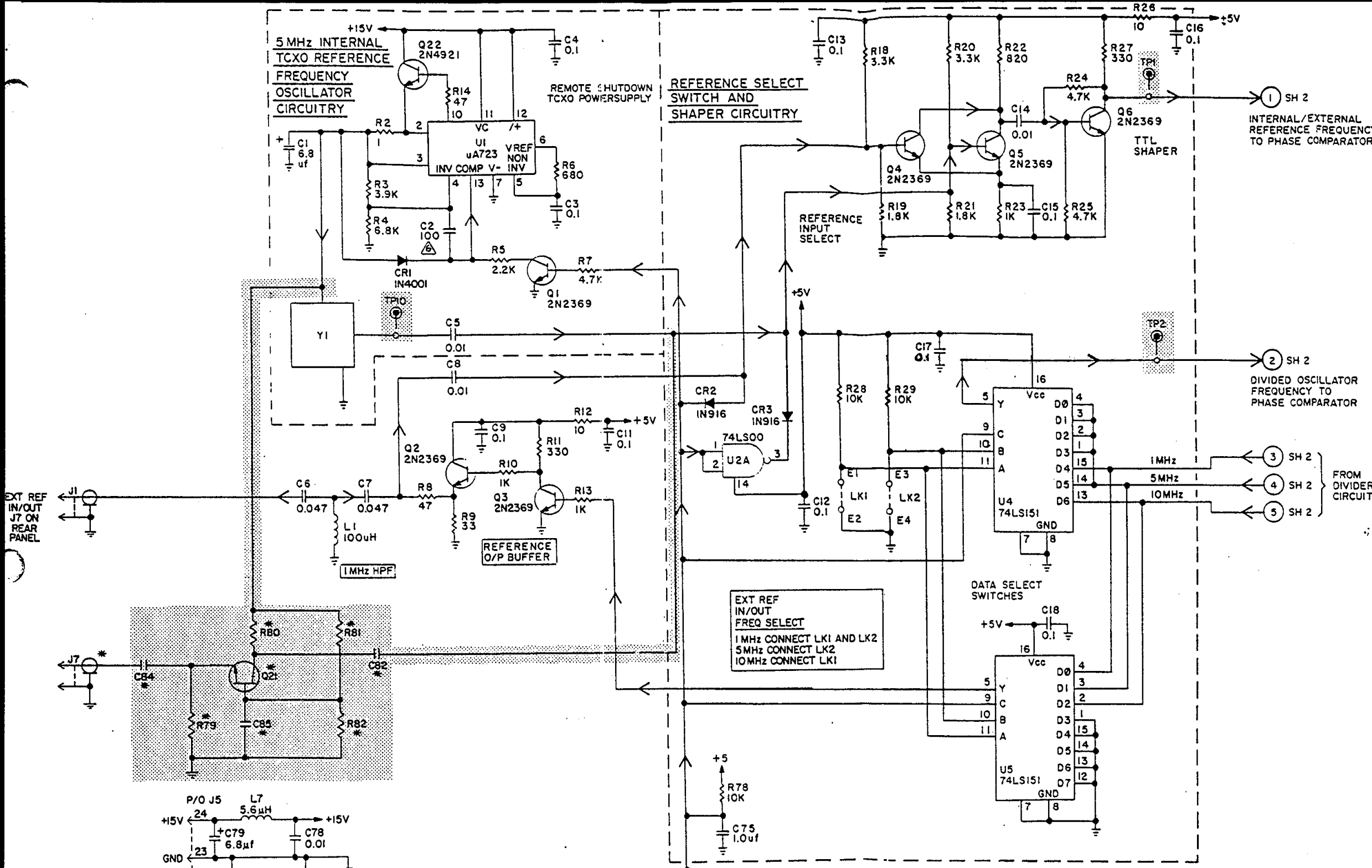
Figure 7-9. Schematic Diagram, 1st LO
 Synthesizer, A7 (Sheet 4 of 5)



PATENTED DEVICE

MANUFACTURED UNDER U.S. PATENT NOS. 4,204,174 AND 3,555,446

Figure 7-9. Schematic Diagram, 1st LO Synthesizer, A7 (Sheet 5 of 5)



INTERNAL/EXTERNAL REFERENCE FREQUENCY TO PHASE COMPARATOR

DIVIDED OSCILLATOR FREQUENCY TO PHASE COMPARATOR

FROM DIVIDER CIRCUITS

1 MHz

5 MHz

10 MHz

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 4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
 5. ASTERICKS INDICATE OPTIONAL PARTS.
- △ C2 VALUE IS 0.1 µF, FOR -+ ASSEMBLY ONLY.

Figure 7-10. Schematic Diagram, 2nd I/O/BFO Synthesizer, A8 (Sheet 1 of 3)

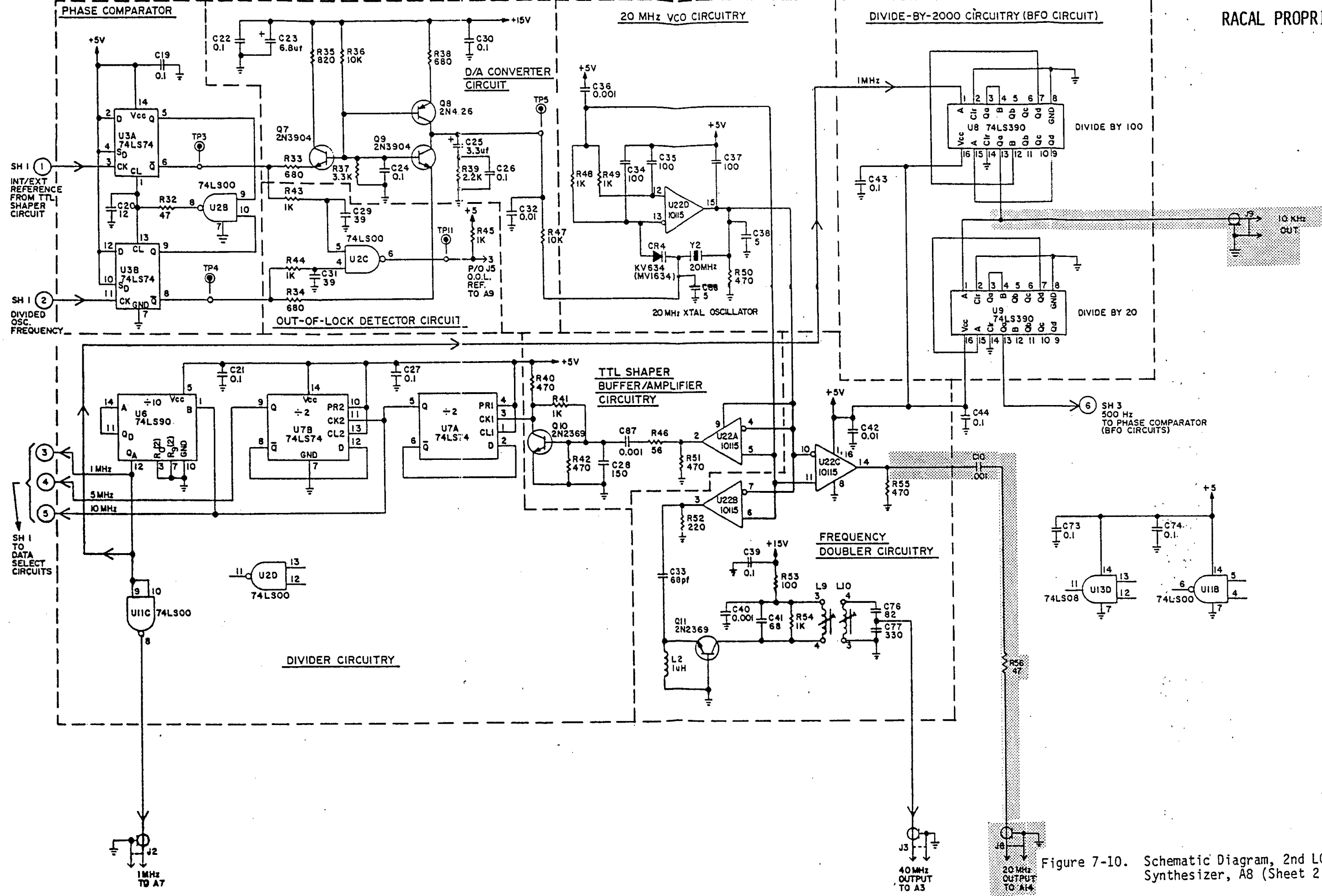


Figure 7-10. Schematic Diagram, 2nd LO/BFO Synthesizer, A8 (Sheet 2 of 3)

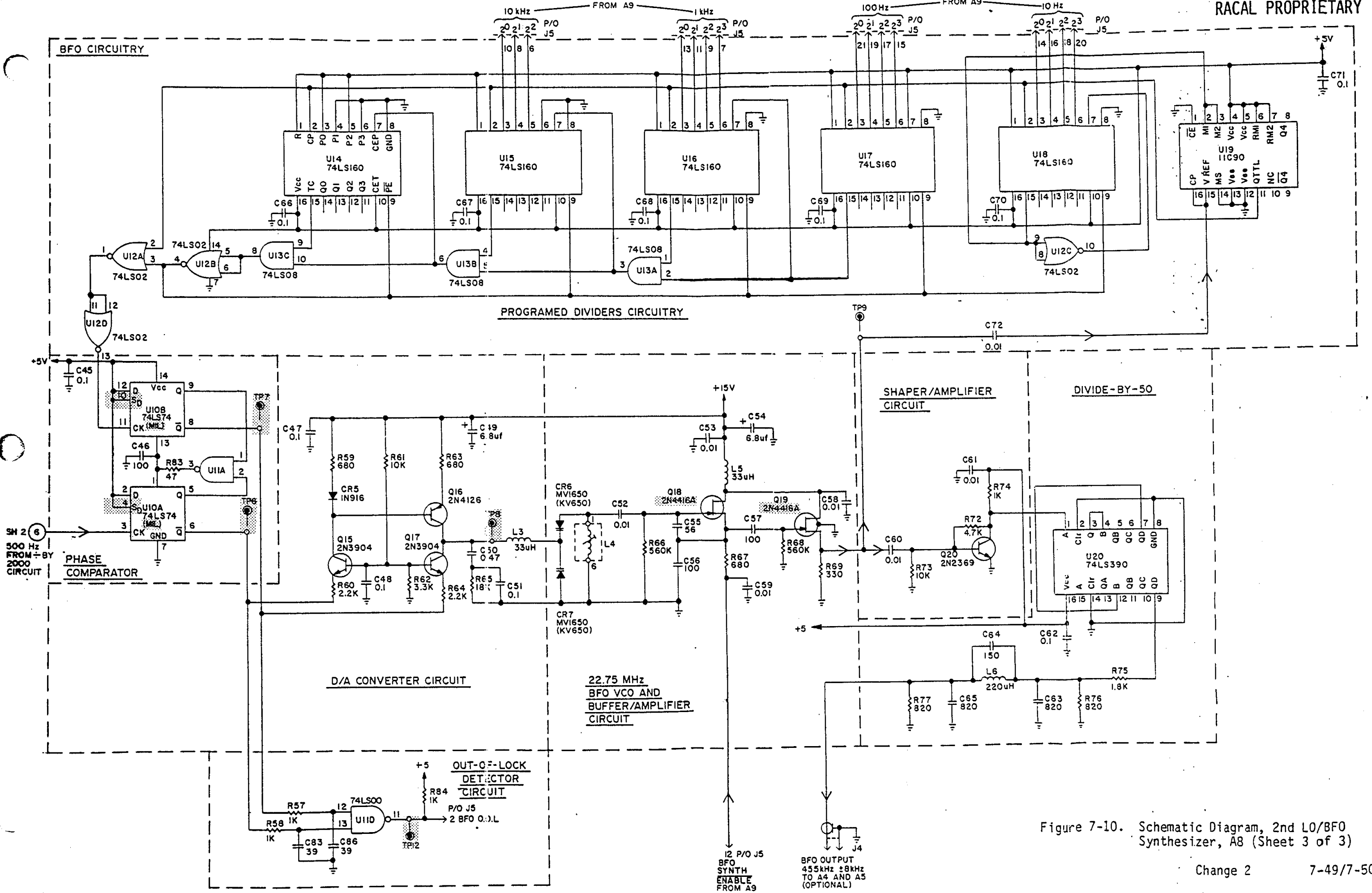
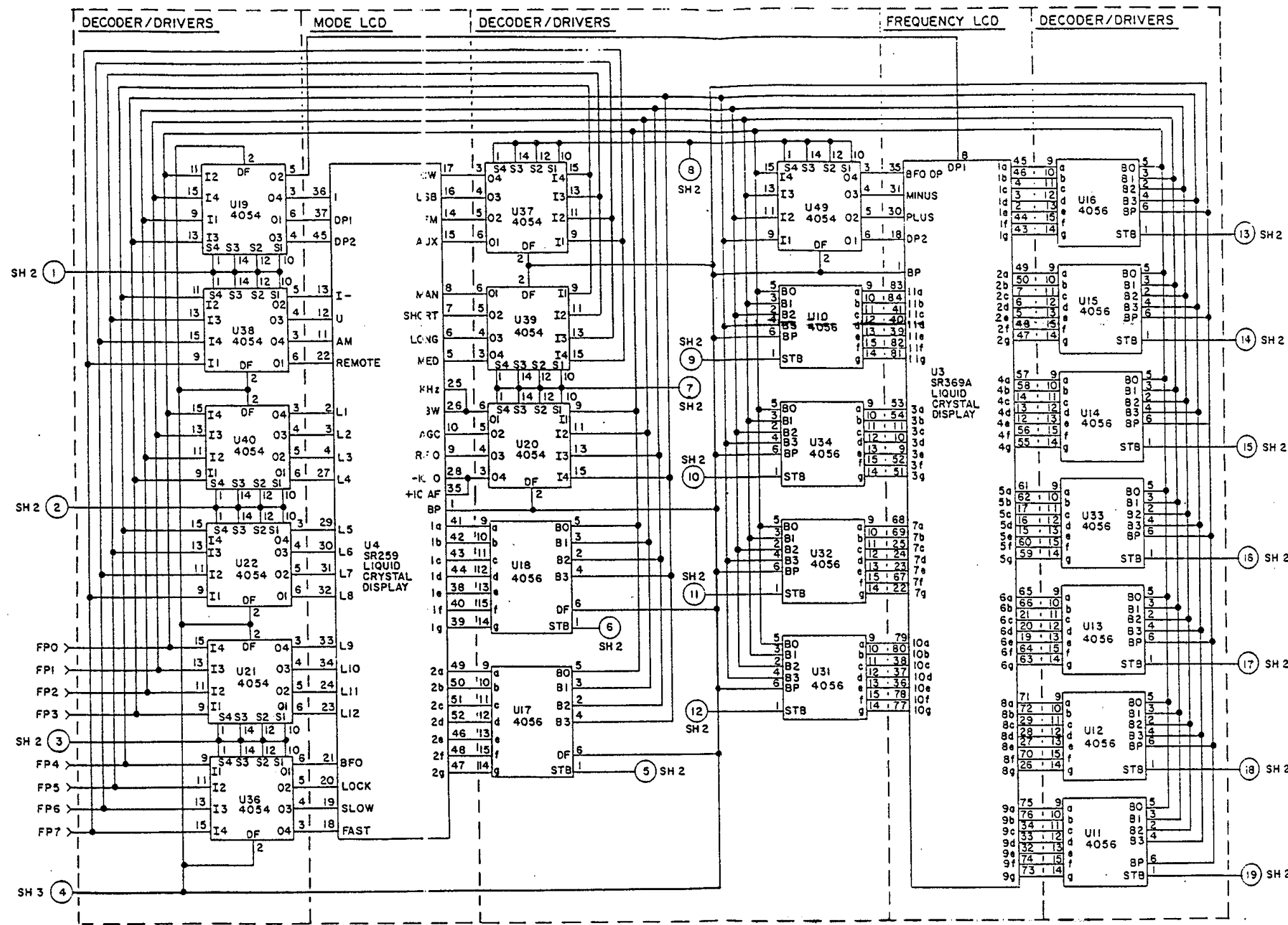


Figure 7-10. Schematic Diagram, 2nd LO/BFO Synthesizer, A8 (Sheet 3 of 3)



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 3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES
 4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND OR ASSEMBLY DESIGN.
 5. LAST USED - U63, C24, R32, J2, E8, J8, W1, DS4.

	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U31	U32	U33	U34	U36	U37	U38	U39	U40	U49
+5	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16
GND	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8	7,8
LOC	G10	A7	C7	D7	G7	J7	K7	D13	E13	K16	G13	F16	G16	C10	D10	F7	10	E16	J13	J16	H13	H16	J10

A	B	A 3
SH.1	SH.2	SH.3
REVISION STATUS OF SHEETS		

Figure 7-11. Schematic Diagram, Receiver Control, A9 (Sheet 1 of 3)

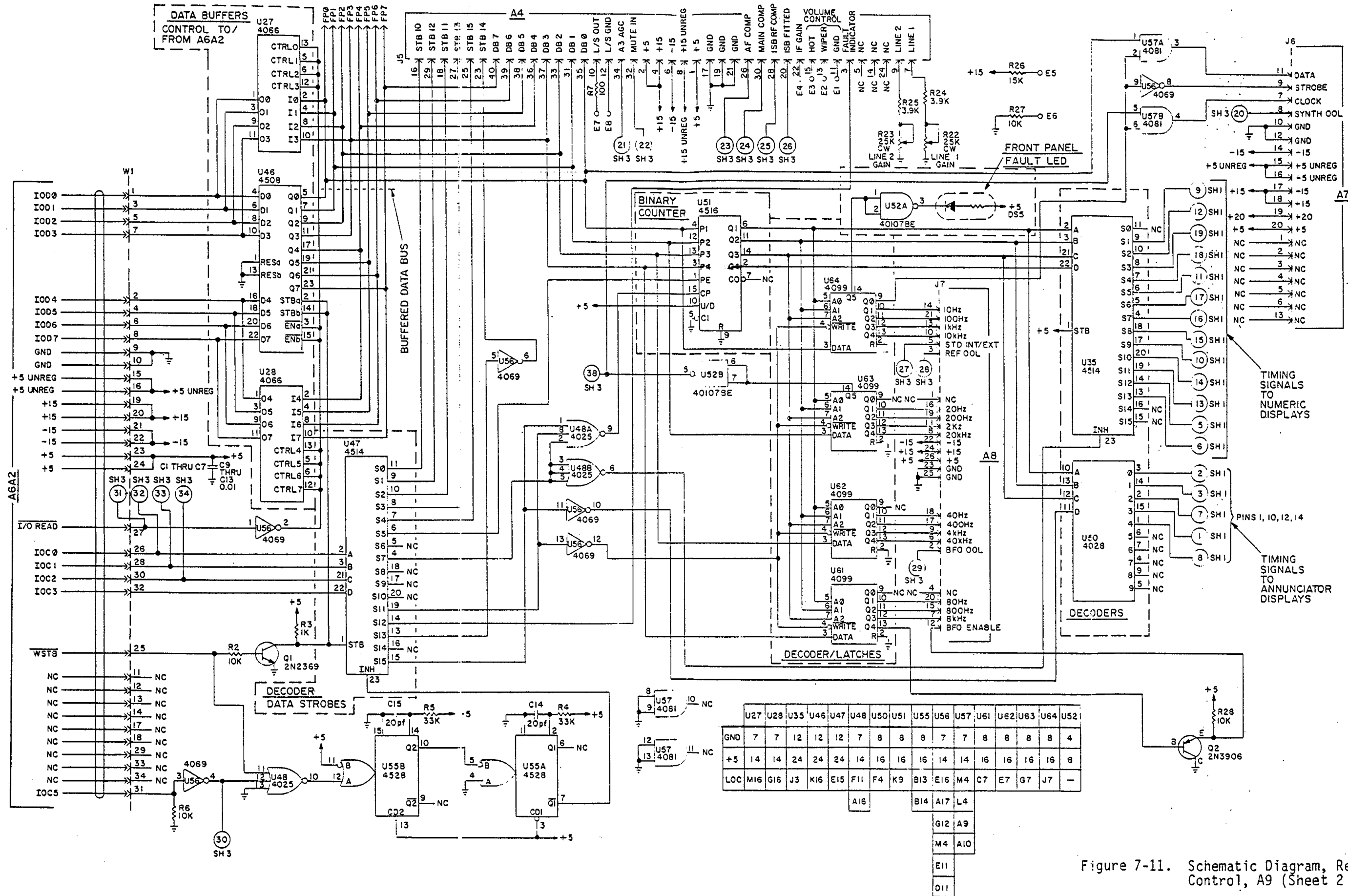


Figure 7-11. Schematic Diagram, Receiver Control, A9 (Sheet 2 of 3)

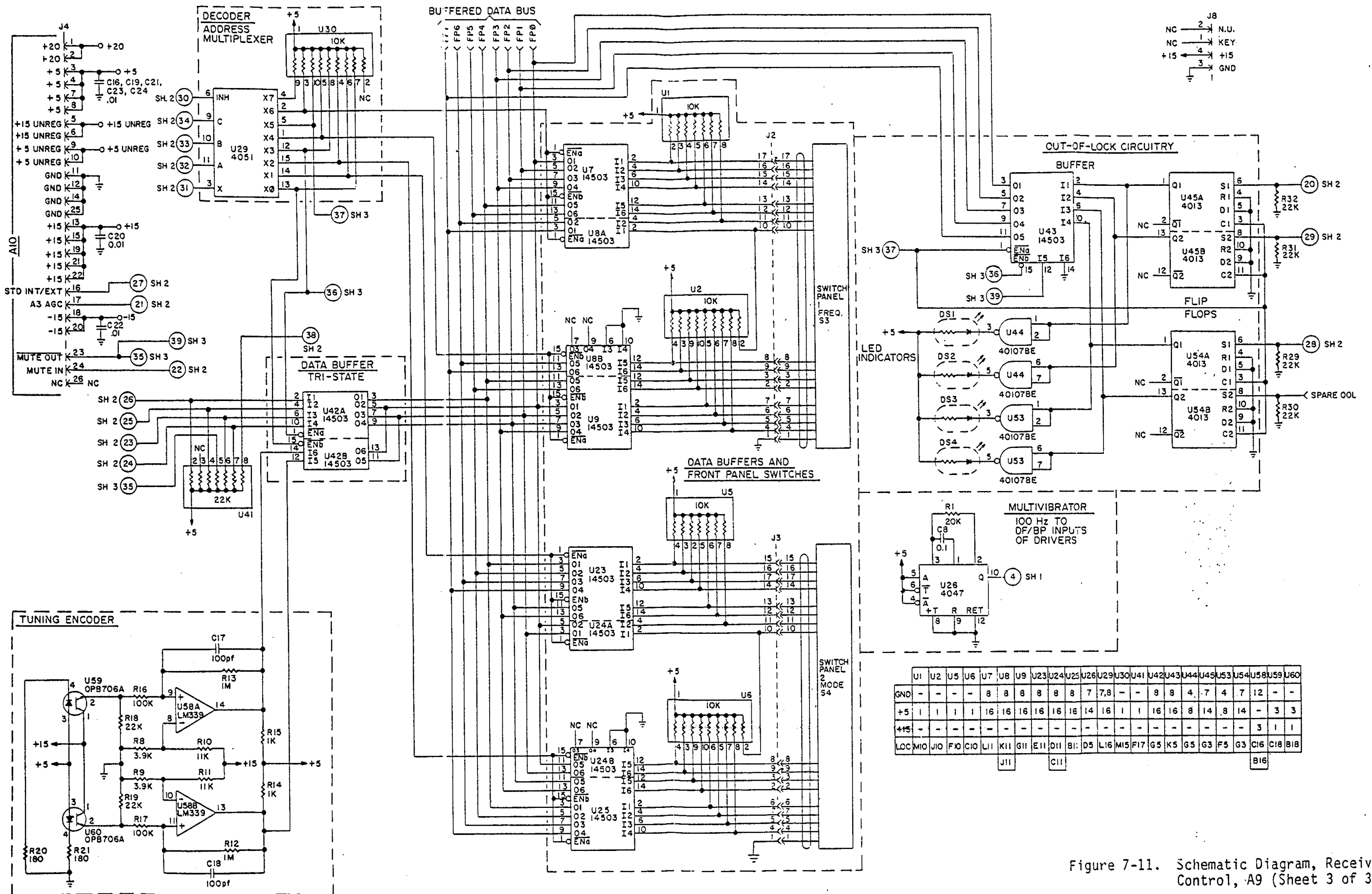


Figure 7-11. Schematic Diagram, Receiver Control, A9 (Sheet 3 of 3)

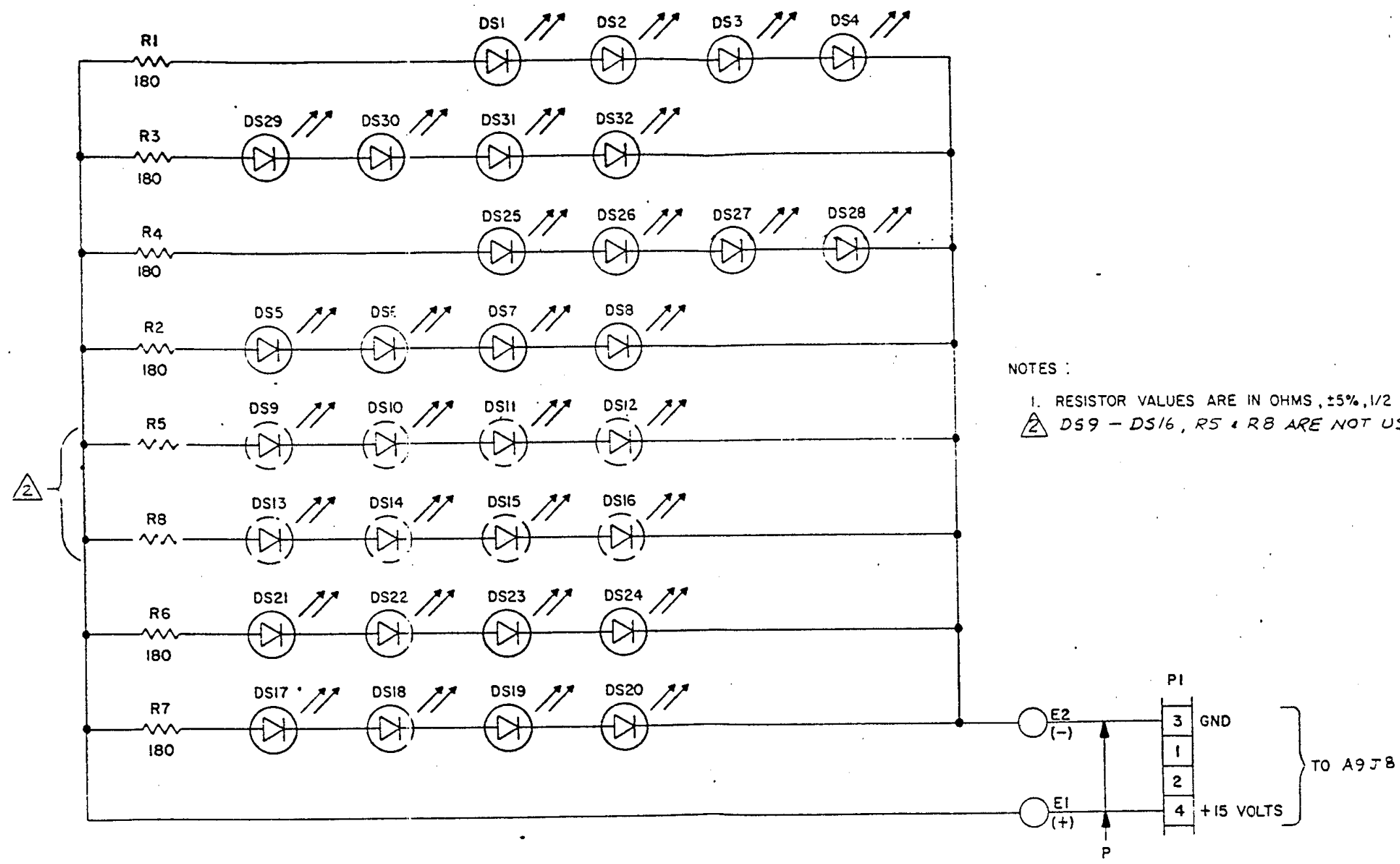


Figure 7-12. Schematic Diagram, Liquid Crystal Display Lamps

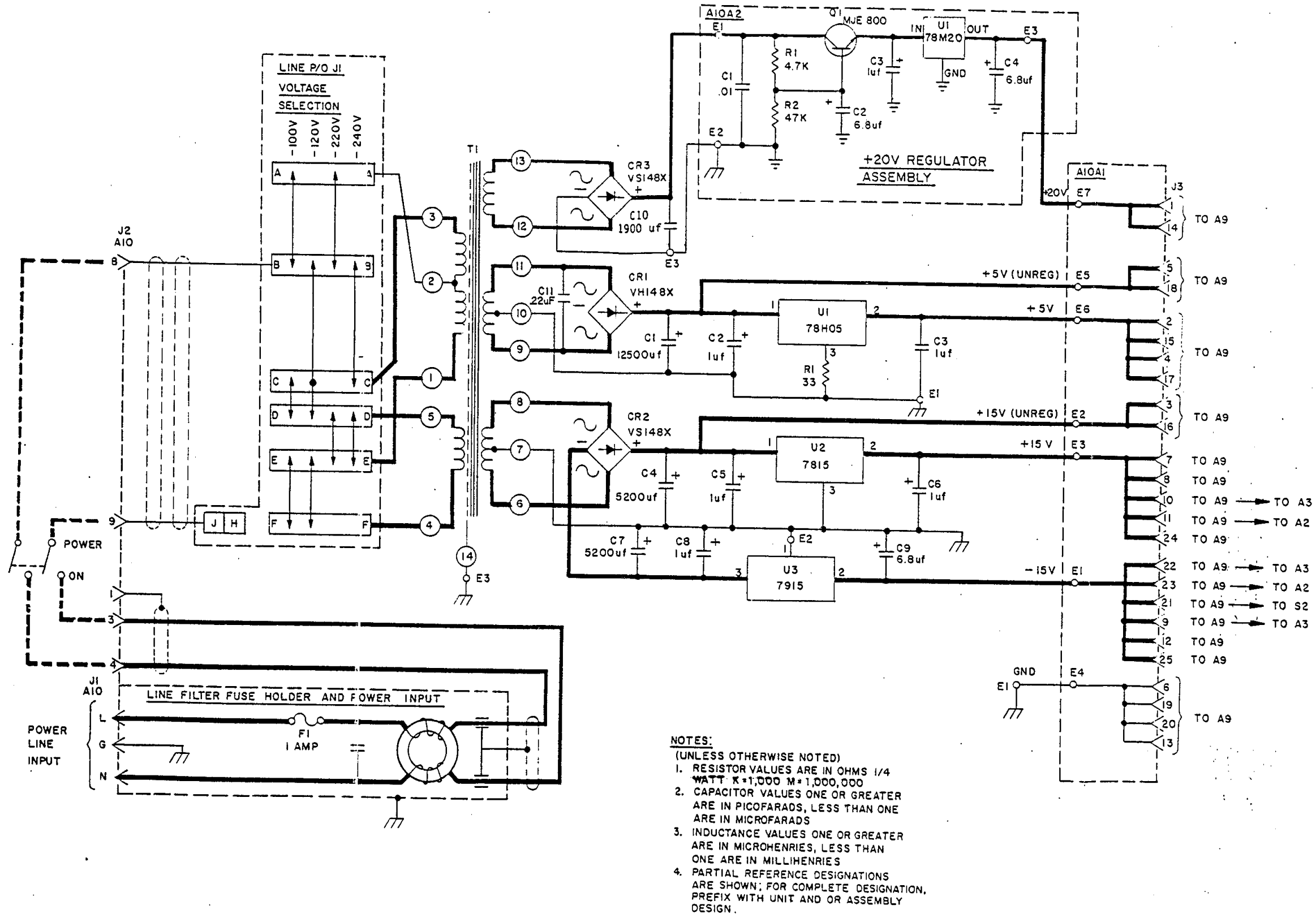
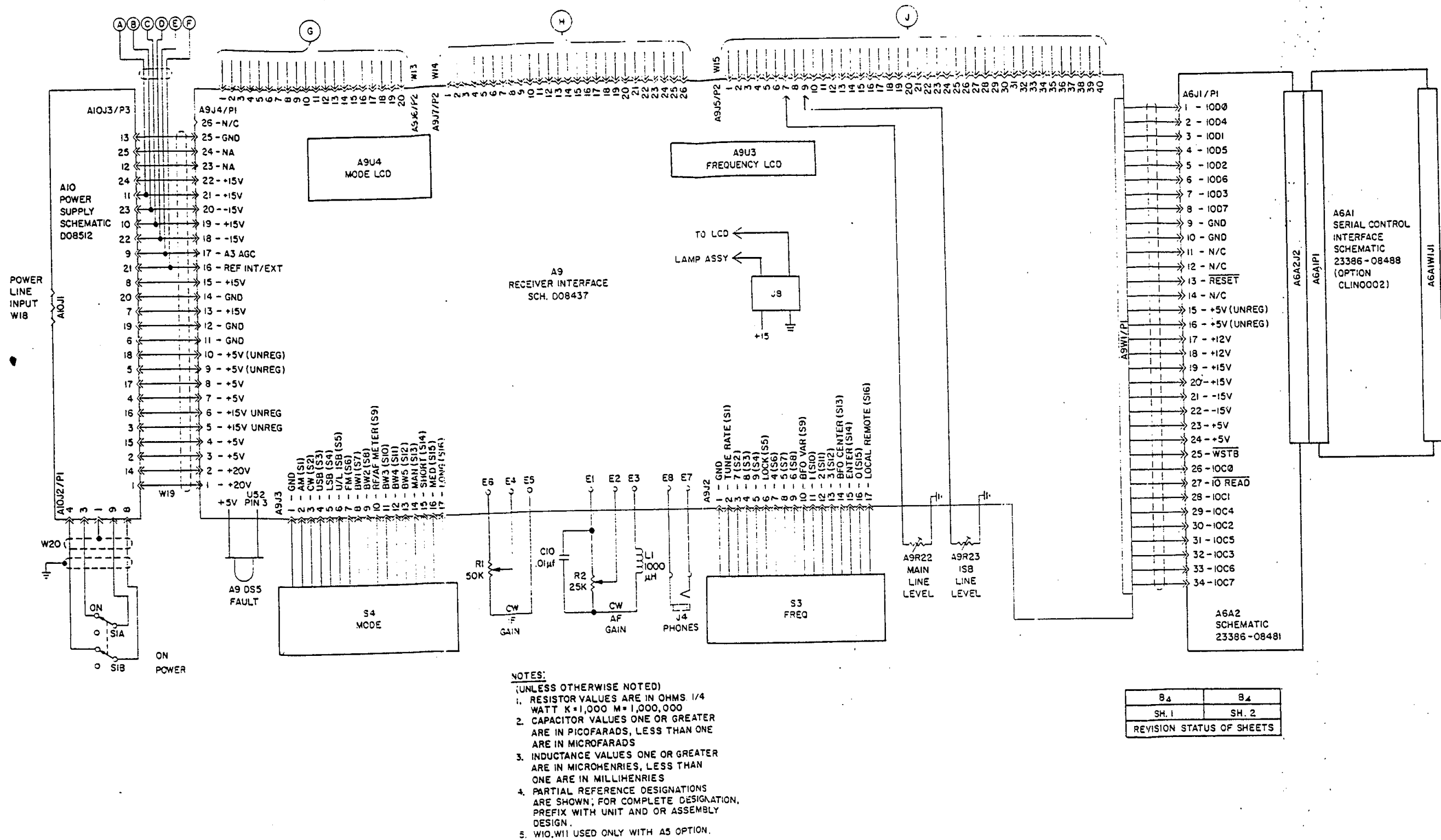


Figure 7-13. Schematic Diagram, Power Supply, A10



B _A	B _A
SH. 1	SH. 2
REVISION STATUS OF SHEETS	

Figure 7-14. Interconnection Diagram, RA6790/GM HF Receiver (Sheet 1 of 2)

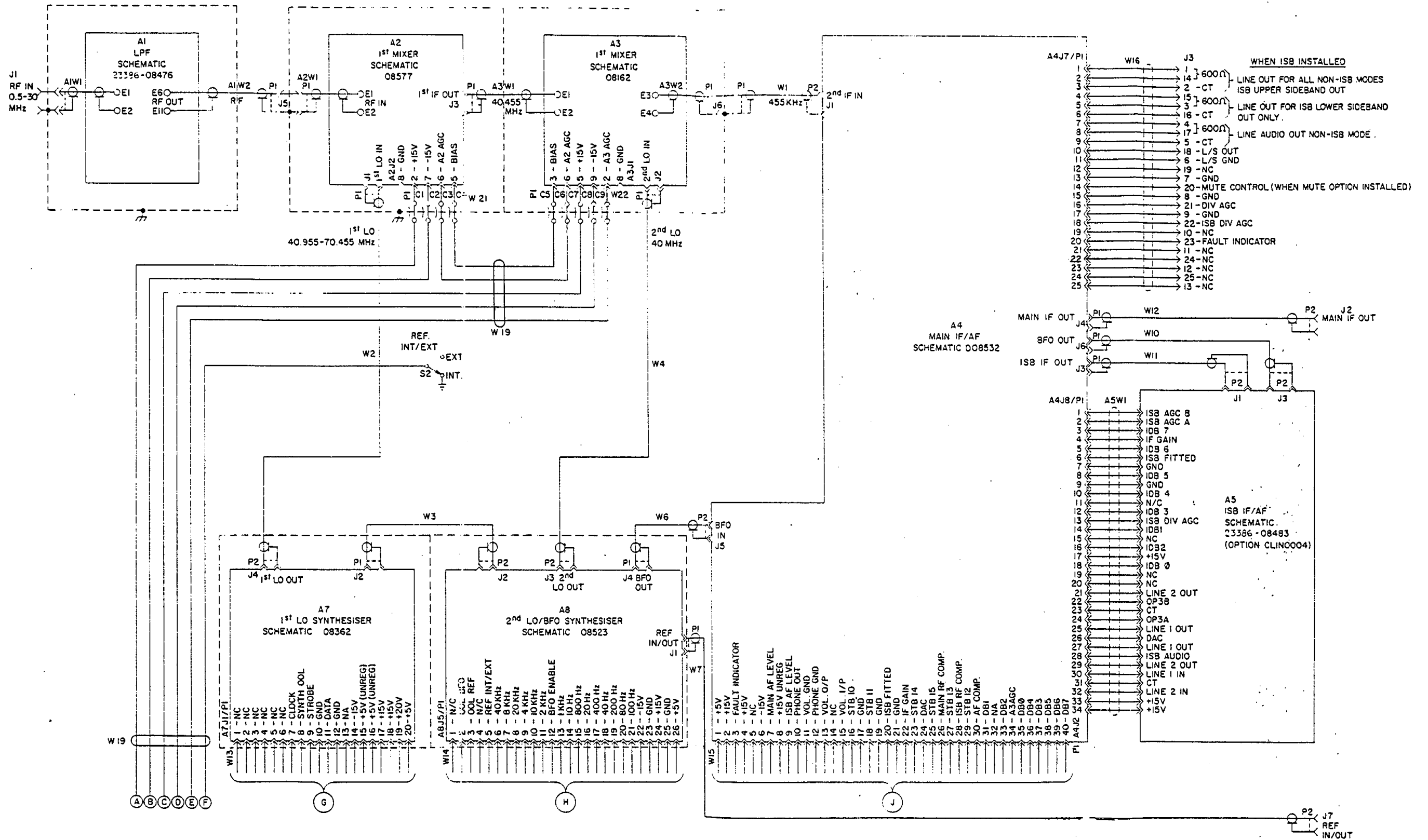


Figure 7-14. Interconnection Diagram, RA6790/GM HF Receiver (Sheet 2 of 2)