ISB IF/AF BOARD A5 (ST08109)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R1	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R2	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R3	56k	Metal Oxide	$\frac{1}{4}$	2	909052
R4	12k	Metal Oxide	$\frac{1}{4}$	2	917952
R5	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R6	33k	Metal Oxide	$\frac{1}{4}$	2	910111
R7	2.7k	Metal Oxide	$\frac{1}{4}$	2	916548
R8	560	Metal Oxide	$\frac{1}{4}$	2	917061
R9	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R10	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R11	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R12	1k	Metal Oxide	$\frac{1}{4}$	2	913489
R13	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R14	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R15	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R16	47	Metal Oxide	$\frac{1}{4}$	2	917063
R17	680	Metal Oxide	$\frac{1}{4}$	2	910113
R18	1.5k	Metal Oxide	$\frac{1}{4}$	2	911166
R19	2k	Variable			938440
R20	220k	Metal Oxide	$\frac{1}{4}$	2	921771
R21	100	Metal Oxide	$\frac{1}{4}$	2	910388
R22	47	Metal Oxide	$\frac{1}{4}$	2	917063
R23	50k	Variable			938441
R24	680	Metal Oxide	$\frac{1}{4}$	2	910113
R25	2.2k	Metal Oxide	$\frac{1}{4}$	2	916546
R26	22k	Metal Oxide	$\frac{1}{4}$	2	913493
R27	4.7k	Metal Oxide	$\frac{1}{4}$	2	913490
R28	47k	Metal Oxide	$\frac{1}{4}$	2	913496
R29	10k	Metal Oxide	$\frac{1}{4}$	2	914042
R30	1k	Metal Oxide	$\frac{1}{4}$	2	913489

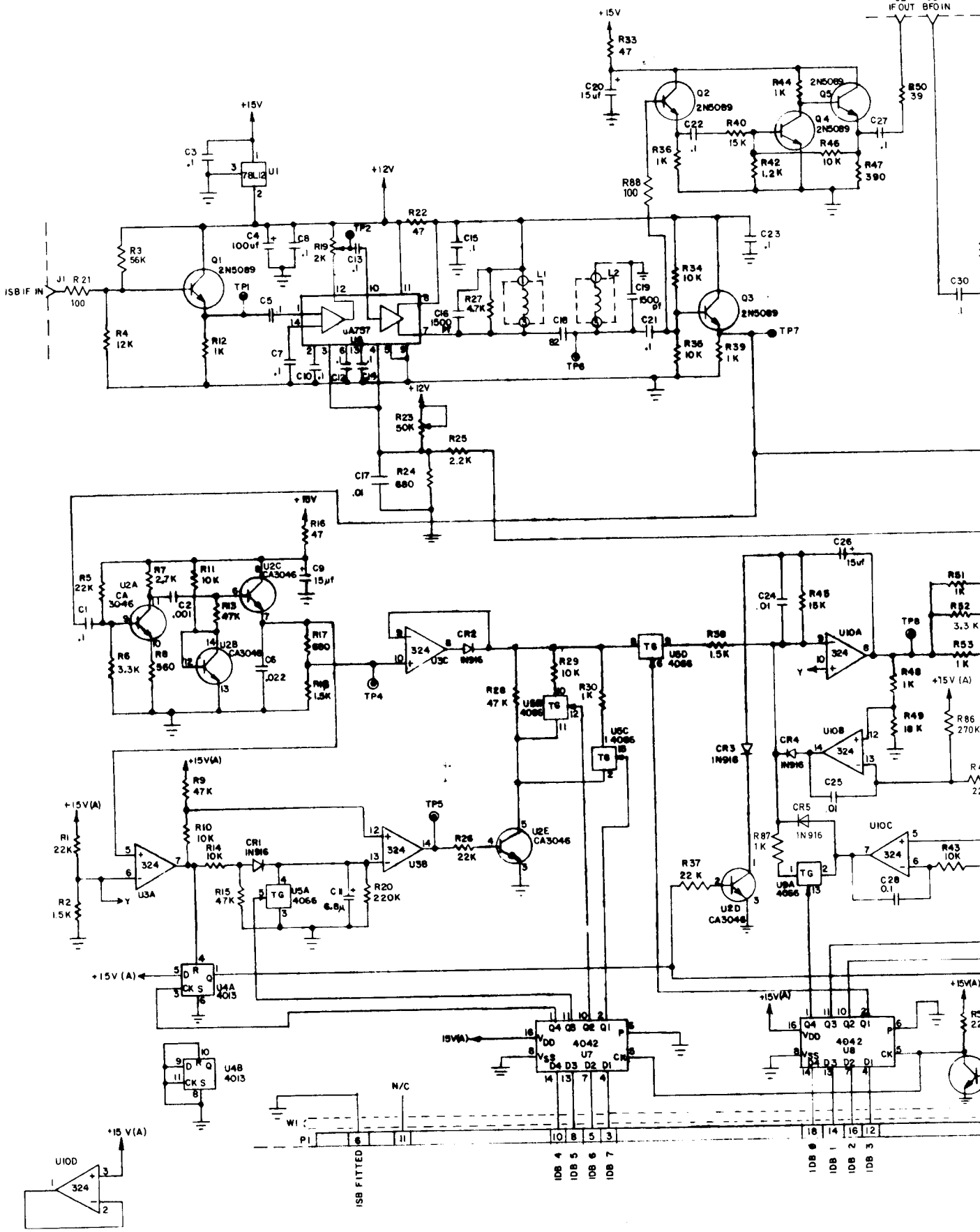
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R31		Not Used			
R32		Not Used			
R33	47	Metal Oxide	¼	2	917063
R34	10k	Metal Oxide	¼	2	914042
R35	10k	Metal Oxide	¼	2	914042
R36	1k	Metal Oxide	¼	2	913489
R37	22k	Metal Oxide	¼	2	913493
R38	1.5k	Metal Oxide	¼	2	911166
R39	1k	Metal Oxide	¼	2	913489
R40	1.5k	Metal Oxide	¼	2	920645
R41	22k	Metal Oxide	¼	2	913493
R42	1.2k	Metal Oxide	¼	2	911179
R43	10k	Metal Oxide	¼	2	914042
R44	1k	Metal Oxide	¼	2	913489
R45	15k	Metal Oxide	¼	2	920645
R46	10k	Metal Oxide	¼	2	914042
R47	390	Metal Oxide	¼	2	916331
R48	1k	Metal Oxide	¼	2	913489
R49	18k	Metal Oxide	¼	2	900994
R50	39	Metal Oxide	¼	2	917062
R51	1k	Metal Oxide	¼	2	913489
R52	3.3k	Metal Oxide	¼	2	910111
R53	1k	Metal Oxide	¼	2	913489
R54	22k	Metal Oxide	¼	2	913493
R55	33k	Metal Oxide	¼	2	913495
R56	10k	Metal Oxide	¼	2	914042
R57	22k	Metal Oxide	¼	2	913493
R58	22k	Metal Oxide	¼	2	913493
R59	1k	Metal Oxide	¼	2	913489
R60	33	Metal Oxide	¼	2	917060
R61	390	Metal Oxide	¼	2	916331
R62		Not Used			
R63	10k	Metal Oxide	¼	2	914042
R64	470	Metal Oxide	¼	2	920758
R65	3.3k	Metal Oxide	¼	2	910111

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors			W		
R66	3.3k	Metal Oxide	¼	2	910111
R67	3.3k	Metal Oxide	¼	2	910111
R68	1.2k	Metal Oxide	¼	2	911179
R69	3.3k	Metal Oxide	¼	2	910111
R70	27k	Metal Oxide	¼	2	913494
R71	27k	Metal Oxide	¼	2	913494
R72	4.7k	Metal Oxide	¼	2	913490
R73	4.7k	Metal Oxide	¼	2	913490
R74	39k	Metal Oxide	¼	2	900993
R75	68k	Metal Oxide	¼	2	916478
R76	100k	Metal Oxide	¼	2	915190
R77	100k	Metal Oxide	¼	2	915190
R78	4.7k	Metal Oxide	¼	2	913490
R79	8.2k	Metal Oxide	¼	2	918202
R80		Not Used			
R81	2.2k	Metal Oxide	¼	2	916546
R82	33	Metal Oxide	¼	2	917060
R83	22	Metal Oxide	¼	2	920743
R84	33	Metal Oxide	¼	2	917060
R85	10	Metal Oxide	¼	2	909145
R86	270k	Metal Oxide		2	923598
R87	1k	Metal Oxide		2	913489
R88	100	Metal Oxide		2	910388
Capacitors			V		
C1	0.1	Ceramic	50	+20	938406
C2	1000p	Ceramic		20	938408
C3	0.1	Ceramic	50	+20	938406
C4	100	Electrolytic	25		935140
C5	0.1	Ceramic	50	+20	938406
C6	0.022	Ceramic		20	930219
C7	0.1	Ceramic	50	+20	938406
C8	0.1	Ceramic	50	+20	938406
C9	15	Tantalum	20	20	938034
C10	0.1	Ceramic	50	+20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C11	6.8	Tantalum	35	20	938030
C12	0.1	Ceramic	50	+20	938406
C13	0.1	Ceramic	50	±20	938406
C14	0.1	Ceramic	50	±20	938406
C15	0.1	Ceramic	50	±20	938406
C16	1500p	Silver Mica		2	938435
C17	0.01	Ceramic		20	938053
C18	82p	Silver Mica		2	902232
C19	1500p	Silver Mica		2	938435
C20	15	Tantalum	20	20	938034
C21	0.1	Ceramic	50	+20	938406
C22	0.1	Ceramic	50	±20	938406
C23	0.1	Ceramic	50	±20	938406
C24	0.01	Ceramic		±20	938053
C25	0.01	Ceramic		20	938053
C26	15	Tantalum	20	20	938034
C27	0.1	Ceramic	50	+20	938406
C28	0.1	Ceramic	50	±20	938406
C29		Not Used			
C30	0.1	Ceramic	50	±20	938406
C31	0.1	Ceramic	50	+20	938406
C32	6.8	Tantalum	35	±20	938030
C33	0.1	Ceramic	50	+20	938406
C34	0.1	Ceramic	50	±20	938406
C35	0.1	Ceramic	50	±20	938406
C36	0.1	Ceramic	50	+20	938406
C37	0.1	Ceramic	50	±20	938406
C38	6.8	Tantalum	35	±20	938030
C39	6.8	Tantalum	35	20	938030
C40	220	Electrolytic	16		938436
C41	6.8	Tantalum	35	20	938030
C42	6.8	Tantalum	35	20	938030
C43	6.8	Tantalum	35	20	938030
C44	4700p	Ceramic	5		938437
C45	0.1	Ceramic	50	±20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C46	2200p	Ceramic	5		938438
C47	200	Electrolytic	16		938436
C48	68	Tantalum	15		938036
C49	68	Tantalum	15		938036
C50	100	Electrolytic	25		935140
C51	6.8	Tantalum	35	20	938030
C52	470	Electrolytic	25		938439
C53	15	Tantalum	20	20	938034
C54	0.1	Ceramic	50	±20	938406
Diodes					
CR1		IN916			913480
CR2		IN916			913480
CR3		IN916			913480
CR4		IN916			913480
CR5		IN916			913480
CR6		IN916			913480
Transistors					
Q1		Silicon (2N5089)			938417
Q2		Silicon (2N5089)			938417
Q3		Silicon (2N5089)			938417
Q4		Silicon (2N5089)			938417
Q5		Silicon (2N5089)			938417
Q6		Silicon (2N2369)			906842
Q7		Silicon (2N5089)			938417
Q8		Silicon (2N5089)			938417
Q9		Not Fitted			
Integrated Circuits					
U1		78L12			938455
U2		CA3046			922907
U3		324			925944
U4		4013			933644
U5		4066			930148

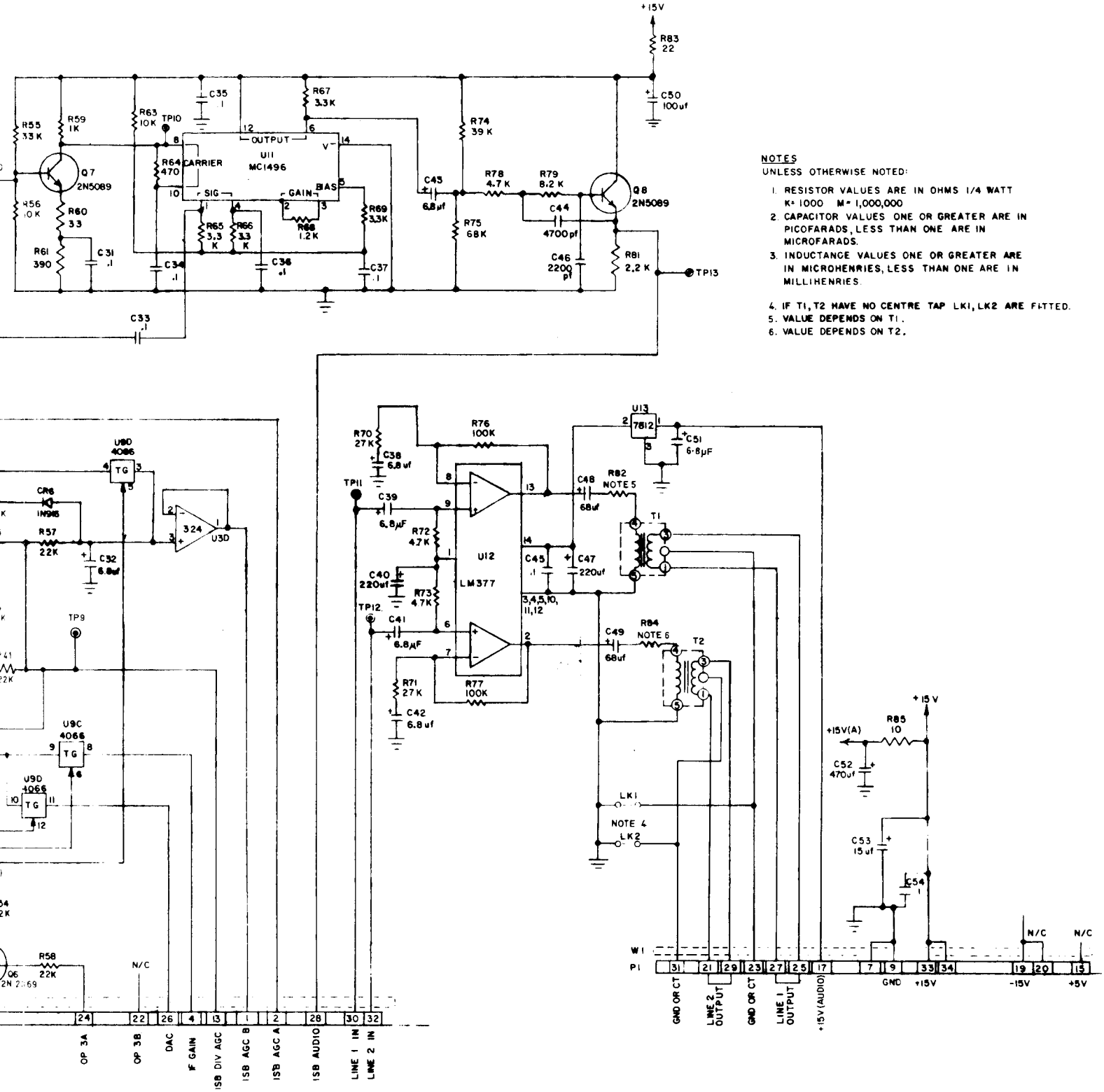
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U6		µA757			938442
U7		4042			938443
U8		4042			938443
U9		4066			930148
U10		324			925944
U11		MC1496P			938427
U12		LM377			928536
U13		7812UC			938455
Transformers					
T1		Assembly (AUDIO)			AT81401
T2		Assembly (AUDIO)			AT81401
Inductors					
L1		Coil RF Variable			AT81400
L2		Coil RF Variable			AT81400
Connectors					
J1		Coaxial RF			938429
J2		Coaxial RF			938429
J3		Coaxial RF			938429



		GND	+15 V(A)
U4	4013	7	14
U7, U8	4042	8	16
U5, U9	4066	7	14
U3, U10	324	11	4

RACAL

TH 1496	DO8108
2	



Circuit: ISB IF/AF Module A5

Fig App.1.1

APPENDIX 2

SCORE INTERFACE MODULE

CONTENTS

	Para
INTRODUCTION	1
SCORE FORMAT	2
ROUTINE AND NEW DATA	5
FRAME COMPARISON	6
PREAMBLE	7
Sync. Code	8
Transmit/Receive	9
Control Inhibit Bit	10
Return Monitor Bit	11
Address Security Code	12
Data Word Ident	13
DATA WORDS	14
WORD 0 - MONITOR	15
User Functions	16
Revertive Indications	17
RF Metering	18
WORD 1 - FREQUENCY	19
WORD 2 - ANALOGUE	20
WORD 5 - HF MODE	22
Mode	23
AGC	24
Bandwidth	25
User Functions	26
REVERTIVE DATA	27
Frame Comparison Error	30
Control Inhibit	32
Return Monitor	33

CLOCK CIRCUITS 34
SIGNAL-TO-LINE REQUIREMENTS 35
INSTALLATION 39
SCORE INTERFACE BOARD
FUNCTIONAL DESCRIPTION 40
SCORE Receiver 41
SCORE Transmitter 45
SCORE Data Input and Output Timing 48
User Functions 53
CIRCUIT DESCRIPTION
SCORE RECEIVER
Sync. Code Detector 54
Strobe Pulse Generator 56
Input Shift Register 57
Address Decoder 58
SCORE TRANSMITTER
Start-in-Sync. Latch 59
Load Pulse Generator 60
Interrupt Control 64
External Strobe 65
Internal/External Data Control 66
PHERIPHERAL INPUT/OUTPUT (PIO) DEVICE 69
Device Connections 71
Control Bus 72
Instruction Execution 73
Control Bus Decoder 75
USER FUNCTIONS 78
INTERNAL CLOCK GENERATOR 79
-5V SUPPLY 80
COMPONENTS LIST

Tables

		Page
Table 1:	SCORE Format	3
Table 2:	Comparison of Specifications	10
Table 3:	Noise Immunity	11
Table 4:	Sync. Code Detector	16
Table 5:	PIO Port Addresses	23
Table 6:	Decoded ROMC States	25

Illustrations

Text :

		Page
Fig. App.2(a)	SCORE Data Routing	14
Fig.App.2(b)	Timing Diagram : SCORE Data	15
Fig.App.2(c)	Timing Diagram : Counter Synchronisation	19
Fig.App.2(d)	Timing Diagram : Delayed SCORE Data	20
Fig.App.2(e)	Block Diagram : 3861 PIO	22

At End of Chapter:

	Fig.
Interconnection Diagram : Diversity Installation	App.2.1
Interconnection Diagram : Remote Control Installation	App.2.2
Block Diagram : SCORE Interface Board	App.2.3
Circuit : SCORE Interface A6A1	App.2.4
Layout : SCORE Interface A6A1	App.2.5

APPENDIX 2

SCORE INTERFACE MODULE

INTRODUCTION

1. The SCORE interface module is an optional internally mounted board which provides for extended or remote control of the receiver using a receiver control unit such as the Racal MA1075. It also allows two receivers, each fitted with a SCORE interface, to be interconnected for space diversity operation. The SCORE (Serial Control of Racal Equipment) control system is described in the following paragraphs.

SCORE FORMAT

2. The SCORE format for serial control is designed to cater for numerous applications and contains ample additional capacity for expansion. It is based on a number of 48-bit synchronous frames, each of which contain a 16-bit preamble (synchronisation, word number identification, etc) followed by a 32-bit data word. The total capacity of the system is sixteen 32-bit data words which is equivalent to approximately 400 separate lines. All sixteen words may be revertively checked.

3. Separate lines are used for both data and clock signals travelling in each direction. These comply with RS422/3, and, over short distances, are compatible with RS232/CCITT V28.

4. The SCORE format for the words used by the RA1792 (word numbers 0,1,2 and 5) is given in table 1. Although word 0 may be sent as part of a control data sequence, it does not contain any control information and is used only for revertive data.

ROUTINE AND NEW DATA

5. Under static conditions, i.e. when the control data being transferred from control unit to receiver does not contain change-of-function information, 'routine data' frames are sent in numerical sequence, and at a rate determined by the clock frequency. When a change of function is made however, instead of allowing the transfer of the full sequence of frames to occur before the change of function is executed at the receiver, the next frame to be sent will contain the data word carrying the change of function information. Thus the frames are sent out of sequence and priority is given to those frames containing new data. This is achieved under software control where a flag is set each time a control setting is changed to indicate that the appropriate word requires transmission. The flag is reset when the data word is transmitted.

FRAME COMPARISON

6. Error detection is accomplished by use of the frame comparison technique, which means that two identical frames must be received at the receiver before a change of function can occur. An exception to this is made for the frequency frame (containing word 1), which may be sent singly (new data frames only) by inclusion of external links.

PREAMBLE

7. A 16-bit preamble is added to each 32-bit data word to form one complete 48-bit frame. The preamble contains a 6-bit sync. code, a 2-bit transmit-receive (PTT) code, a control inhibit bit, a return monitor bit, a 2-bit address word security code and a 4-bit data word ident; these are described in the following paragraphs.

Sync. Code

8. The sync. code (bits 0 to 5) consists of a '0' followed by five consecutive '1's. The maximum number of consecutive '1's to occur in serial BCD data is four, e.g. BCD seven followed by BCD eight. This then makes five '1's a unique code. For added security, the next two bits of the preamble (used for PTT) may not consist of two consecutive '1's. This is done to 'terminate' the sync. code and to prevent the generation of a false sync. code following a line break etc.

Transmit/Receive

9. Bits 6 and 7 of the preamble are used for transmit/receive switching (PTT) where the transmit state mutes the receiver and may also set an associated transmitter to the transmit condition. As mentioned in para.8, these two bits must not consist of consecutive '1's. For the transmit state, bit 6 is set to a '1' and bit 7 is set to '0', whilst for the receive state, bit 6 is set to '0' and bit 7 is set to '1'.

Control Inhibit Bit

10. This bit of the preamble (bit 8) is used, as the name implies, to inhibit control of the receiver via the serial control data. When it is set to a '1', the control settings of the receiver remain unchanged and further control instructions conveyed by the 32-bit data words are ignored. The revertive data however, is returned in the normal way, i.e. the receiver settings are returned.

Return Monitor Bit

11. The return monitor bit is normally set to '0' and is only set to '1' to give continuous revertive monitor when single frequency frames are being sent from the control unit (para.6).

TABLE 1: SCORE Data Format

	BIT No	BIT FUNCTION OR FORCED STATE	MONITOR (0)	FREQUENCY (1)	ANALOGUE (2)	HF MODE (5)
PREAMBLE	0	0 | SYNC CODE				
	1	1				
	2	1				
	3	1				
	4	1				
	5	1				
	6	TRANSMIT				
	7	RECEIVE				
	8	CONTROL INHIBIT				
	9	RETURN MONITOR				
	10	ADDRESS	0	0	0	0
	11	EQUIPMENT	0	0	0	0
	12	1 | DATA	0	1	0	1
	13	2 | WORD	0	0	1	0
	14	3 | IDENT	0	0	0	1
	15	4	0	0	0	0
DATA WORD	16	A | USER FUNCTION	1 | 1Hz		1 | BFO x 10 Hz	0 | NOT USED
	17	B	2		2	0
	18	C	4		4	0
	19	D	8		8	0
	20	0	1 | 10 Hz		1 | BFO x 100 Hz	0
	21	0	2		2	0
	22	0	4		4	0
	23	0	8		8	0
	24	0 NOT USED	1 | 100 Hz		1 | BFO xkHz	0
	25	0	2		2	0
	26	0	4		4	0
	27	0	8		BFO SIGN	0
	28	0 | kHz	1		0	1 | MODE
	29	0	2		0	2
	30	0	4		0	4
	31	0	8		0	0
	32	MUTE | 10 kHz	1		0 NOT USED	SYMMETRICAL
	33	FAULT	2		0	0
	34	FC ERROR	4		0	0
	35	0	8		0	0
	36	RF METER	1		0	AGC DUMP
	37	0 | 100 kHz	2		0	1 | AGC
	38	0 NOT	4		0	2
	39	0 USED	8		1	4
	40	1 | METER READING	1 | MHz		2 | IF GAIN	1 | BANDWIDTH
	41	2	2		4	2
	42	4	4		8	4
	43	0	8		0	0
	44	8	1 | 10 MHz		16	W | USER FUNCTION
	45	16	2		32	X
	46	32	1 | SINGLE FRAME		64	Y
	47	64	2 | CHECK BITS		128	Z

Address Security Code

12. Bits 10 and 11 of the preamble are used in words 8 and 9 of the SCORE control system (equipment and operator addressing words respectively) to provide added security against incorrect addressing. These two bits are set to '0' in all words used by the RA1792 (and the MA1075).

Data Word Ident

13. The last four bits of the preamble (bits 12 to 15) are used for the data word identification code, in binary format, i.e. 0 to 15 (decimal) or 0 to F (hexadecimal).

DATA WORDS

14. As stated in para.4, words 0,1,2 and 5 are used by the RA1792. These are described in the following paragraphs which should be read in conjunction with table 1. Certain words contain a number of 'forced zeros' to prevent the possible occurrence of five consecutive '1's which would otherwise be mistaken for a sync. code.

WORD 0 - MONITOR

15. This word is used for revertive signalling only; although it may be transmitted as part of a forward control data sequence, it does not contain any control data.

User Functions

16. The first four bits of data word 0 provide for the revertive user functions where up to four earth (0V) signals applied to the receiver are reproduced at rear panel connections of the control unit. The four bits are labelled A,B,C and D, and correspond with the A,B,C and D connections at both the receiver and control unit.

Revertive Indications

17. The next operative bits of word 0 are bits 32, 33 and 34. Bit 32 is set to a '1' when a mute signal is applied to the receiver, and this is conveyed to the control unit via the revertive data to illuminate the MUTE indicator on the control unit front panel. Data bit 33 (the fault bit) is set to a '1' following a fault condition in the synthesizer section of the RA1792 receiver, and this condition is conveyed to the control unit via the revertive data to illuminate the FAULT indicator on the control unit front panel. Data bit 34 is the frame comparison error bit and is normally at '0'; it goes to a '1' when three consecutive frame comparison errors are detected at the receiver, and this also results in the illumination of the FAULT indicator.

RF Metering

18. Data bit 36 is set to a '1' to select RF metering, and the RF meter reading data is conveyed, in 7-bit digital format, via data bits 40 to 42 and 44 to 47 (bit 43 is a forced zero).

WORD 1 - FREQUENCY

19. The first 30 bits of this word (16 to 45 inclusive) contain the frequency setting information in BCD format. The remaining two bits (46 and 47) determine whether frame comparison is required (for error detection), in which case each frame is sent twice, or whether single frequency frames are to be sent.

WORD 2 - ANALOGUE

20. Word 2 contains the analogue functions, BFO and IF gain. For a receiver set for local control, the range of the BFO is between plus 8 kHz and minus 8 kHz (centred on 455 kHz). For remote control however, the maximum offset is restricted to the range plus and minus 7.79 kHz i.e. three data bits (24, 25 and 26) are used for the kHz digit (giving a maximum figure of 7), and to prevent the generation of a spurious sync. code, data bit 23 must not be set to a '1' (thus giving a maximum figure of 7 for the 100 Hz digit). Data bit 27 is the BFO sign bit and is set to a '1' for negative BFO offset frequencies, to a '0' for positive BFO offset frequencies.

21. The receiver manual IF gain control data is conveyed between control unit and receiver via data bits 39 to 42 and 44 to 47 (bit 43 in a forced zero). This gain control data is not however, transferred from master receiver to slave receiver when two receivers are interconnected for space diversity operation. In this case the receiver diversity AGC outputs are interconnected.

WORD 5 - HF MODE

22. This word is used for mode, AGC and bandwidth selection, and for the forward user functions.

Mode

23. Bits 28 to 32 inclusive are concerned with mode selection. The state of bit 32 determines whether a symmetrical mode or a sideband mode is selected, as shown in the following table.

BCD coding of Bits 28 to 31	Bit 32 State	Mode Selected	
1	1	AM	
2	1	CW	Symmetrical
5	1	FM	
0	0	USB	
1	0	LSB	Sideband
2	0	ISB-U	
3	0	ISB-L	

AGC

24. Bit 36 is used for AGC dump; when set to a '1' it causes a rapid decay of the AGC voltage level so that the level may be re-established for the signal being received. The coding of bits 37,38 and 39 in given below.

BCD Code	Function
0	Manual and short
1	Manual and medium
2	Manual and long
3	Manual only
4	Short
5	Medium
6	Long
7	Not allowed

Bandwidth

25. The coding of bits 40 to 42 is given below. The actual filters fitted are dependent upon the particular receiver options. The filter numbers given correspond with those on the receiver main IF/AF board.

BCD Code	Filter No.
0	Not used
1	Not used
2	3 (Narrowest Bandwidth)
3	4
4	5*
5	6
6	7
7	Not used

* May select filter 2 if offset sideband filter.

User Functions

26. The last four bits of word 5 provide for the forward user functions where up to four earth (0V) signals applied to the receiver control unit are reproduced at rear panel connections on the RA1792 receiver. The four bits are labelled W, X, Y and Z and correspond with the similarly marked input and output connections of the control unit and receiver respectively.

REVERTIVE DATA

27. The format of the revertive data is the same as for the control data. Frame comparison however, does not take place, and the revertive data is generally sent in single frames.

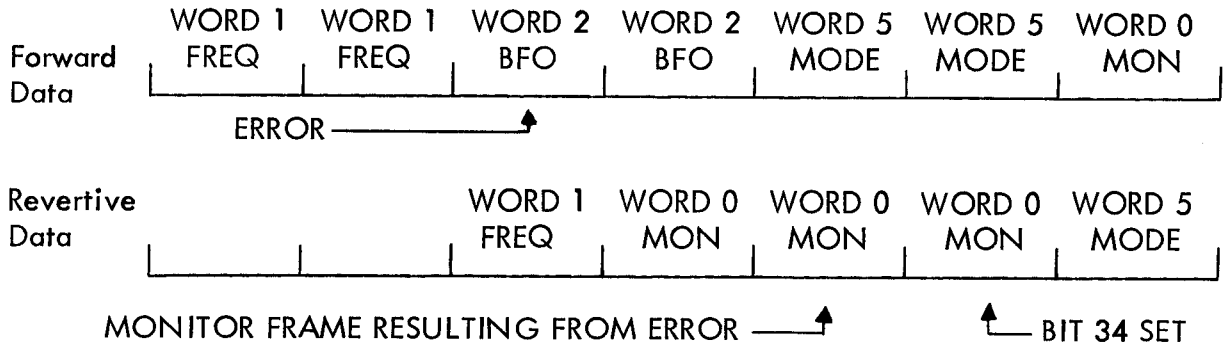
28. Provided that the control inhibit and return monitor bits of the forward data preamble are not set to a '1', that single frequency frames are not being sent, and that no errors occur in the control data, then the form of the revertive data is given by the following example.

Forward Data	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 1 FREQ	WORD 2 BFO	WORD 2 BFO	WORD 5 MODE
Resulting Revertive Data		WORD 0 MON	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 0 MON	WORD 2 BFO

29. In this example, the forward data consists of two word 0 frames, two word 1 frames, to word 2 frames and the first of two word 5 frames. Since two frames have to be sent and compared before any action can take place, the revertive data resulting from the forward data given in this example is shown lagging the forward data by two 48-bit frames (ignore for the moment the first revertive data word 0). The two forward data word 0 frames are compared; since no bit errors are present, the two frames are identical and a word 0 frame is returned. The next frame comparison however, is between a word 0 and a word 1. The comparison is therefore unsuccessful, and, although an error does not exist, it is arranged to send back a word 0 monitor frame. Two word 1 frames are now compared, and result in a revertive word 1 frame. The next comparison is between a word 1 frame and a word 2 frame, which results in a revertive word 0 frame, two word 2 frames result in a revertive word 2 frame, and so on. The control of the first (blank) revertive data frame is dependent on the previously sent data, whilst the next frame (the first word 0 frame in this example) must be a word 0 frame due to a comparison between two disimilar frames. Note that when two RA1792 receivers are interconnected for master/slave operation, word 0 control data frames are not sent by the master receiver.

Frame Comparison Error

30. A frame comparison error signal is generated only on the failure of three consecutive frame comparisons, as shown in the following example:



31. In this example the forward data consists of two word 1 frames, two word 2 frames, two word 5 frames and the first of a pair of word 0 frames. The two frequency word frames result in a revertive frequency word frame and the next two frames (frequency and BFO) result in a monitor word 0 frame. The two BFO word frames are compared, and this time, due to an error, the frame comparison is unsuccessful, resulting in a further revertive monitor frame. The next two frames (BFO and mode) being disimilar also result in a revertive monitor frame. Thus three consecutive revertive monitor frames result following the FAILURE of three consecutive frame comparisons; a frame comparison error signal is generated and this is conveyed by bit 34 of the revertive word 0 frame.

Control Inhibit

32. If the control inhibit bit (bit 8 of the preamble) in a forward control data frame is set to a '1', and provided that the return monitor bit (bit 9 of the preamble) is not set to a '1', then the revertive data frames are sent in pairs and in numerical sequence and convey the actual receiver setting data.

Return Monitor

33. If the return monitor bit (bit 9 of the preamble) in a series of forward control data frames is set to a '1', then the revertive data consists of a series of continuous monitor frames.

CLOCK CIRCUITS

34. These provide the timing signals required by the various parts of the system. The basic data rate clock signal may be generated either by an external unit, such as the receiver control unit or a modem, or may be provided by an internal clock generator (approximately 6 kHz).

SIGNAL-TO-LINE REQUIREMENTS

35. The RA1792 receiver signal-to-line requirements for the serial data and clock signals comply with EIA standards RS-422 and RS-423. The SCORE clock and data output drivers are configured for RS-422, a differential balanced voltage interface which is fully compatible with CCITT recommendations V11 and X27. The maximum permissable line length is dependent on factors such as data signalling (clock) rate, tolerable signal distortion and noise interference. In general, the maximum line length at a data signalling rate of 100 k bauds is 1200 metres (4000 ft), reducing to approximately 15 metres (50 ft) at the maximum data signalling rate of 10M bauds. Note however, that the maximum data signalling rate for the RA1792/MA1075 is 9.6k bauds. If no connection is made to the RS-422 positive output, a single ended interface suitable to drive an RS-232 receiver is produced, provided the line length does not exceed 15 metres (50 ft).

36. The line receivers used for the SCORE clock and data input signals comply with EIA standards RS-422 (balanced voltage interface) and RS-423 (unbalanced voltage interface). When connected for an unbalanced transmission line (positive input terminal grounded), the circuit may be driven from a single-ended RS-232 driver circuit provided the line voltages do not exceed plus and minus 12 V. A comparison of the specifications for EIA standards RS-232, RS-422 and RS-423 (as far as the RA1792 is concerned) is given in table 2, and the noise immunity figures for mixed single-ended interfaces are given in table 2.

Table 2: Comparison of Specifications

CHARACTERISTIC	RS-232C (CCITT V28)	RS-423	RS-422
Mode	Single Ended	Single Ended	Differential
Logic '1' (OFF State)	Negative Voltage	Negative Voltage	Negative Voltage
Logic '1' (ON State)	Positive Voltage	Positive Voltage	Positive Voltage
Maximum Line Length	15 m (50 ft) at 20 k Bauds	1200 m (4000 ft) at 3k Bauds	1200 m (4000 ft) at 100 k Bauds
Maximum Data Rate	20 k Bauds	300 k Bauds	1 M Bauds
Open Circuit Driver Voltage (maximum)	±25 V	±6 V	6 V differential
Loaded Driver Voltage (minimum)	±5 V to ±15 V	±3.6 V	2 V differential
Driver Output Load - Power Off	300 ohms	100 µA (-6 V to +6 V)	100 µA 6 V to 0.25 V
Driver Short - Circuit Current	±500 mA	±150 mA	±150 mA
Driver Slew Rate	30 V/µ second	Capacitor controlled	No restriction
Receiver Input Resistance	3 k ohms to	Equal to or greater than 4k ohms	Equal to or greater than 4k ohms
Receiver Threshold	-3 V to +3 V	-0.2 V to +0.2 V	-0.2 V to +0.2 V
Maximum Receiver Input Voltage	±25 V	±12 V	±12 V

Table 3: Noise Immunity

DRIVER	RECEIVER	NOISE IMMUNITY (MINIMUM)
RS-232C	RS-232C	2 V
RS-423	RS-423	3.4 V
RS-232C	RS-423	4.8 V
RS-423	RS-232C	0.6 V

37. The remaining external input and output connections to and from the SCORE interface conform to a common convention. Logic input signals are defined as follows:

Logic '1' - ON state: Steady state short-circuit current to 0V, less than 40 mA.
Logic '0' - OFF state: Internally pulled up to a positive voltage, usually +12 V (for C-MOS).

38. Logic output signals are defined as follows:

Logic '1' - ON state: represented by a short circuit to 0V via a current - saturated open-collector transistor.
Logic '0' - OFF state: represented by the open-circuit output from a transistor in the cut-off condition i.e. the externally applied open-collector pull-up voltage (up to +20 V).

INSTALLATION

39. Detailed installation information is beyond the scope of this appendix and reference should be made to the appropriate system manual. Typical interconnection diagrams are however given for a space diversity installation using a pair of RA1792 receivers (fig. App.2.1) and for a remote control installation using the MA1075 receiver control unit (fig. App.2.2).

SCORE INTERFACE BOARD

FUNCTIONAL DESCRIPTION

40. The following functional description should be read in conjunction with the block diagram of the SCORE interface board given in fig. App.2.3. When the unit is switched on, the initialisation routine resets the receive interrupt latch (/IO READ, IOC3 and IOC7 applied to the address decoder), resets the transmit interrupt latch (I/O port 1 bit 1) and enables the receive and transmit interrupt circuitry (via PIO port 84, bits 6 and 7).

SCORE Receiver

41. Inverted SCORE control data (from another RA1792 receiver or a receiver control unit) is clocked into a sync. code detector and, via an inverter, to an 8-bit serial in/ parallel and serial out shift register. When a correct inverted sync. code is detected, a strobe pulse is generated which is applied to:

    (1) the reset input of an 8-bit counter.

    (2) the strobe input of the shift register; the data in each shift register stage is transferred to a storage register and will appear at the parallel outputs when a '1' is applied to the enable input.

    (3) the set input of the receive interrupt latch; the output changes to a '1' and this causes the peripheral input/output (PIO) device to generate an interrupt signal which is routed to the microcomputer (via the control bus).

42. The microcomputer examines the receive and transmit interrupt pending lines, decides that a receive interrupt has occurred, and then applies address 88 (IOC3 and IOC7), together with the /IO READ Signal to the address decoder. The resulting '1' output resets the receive interrupt latch and enables the 8-bit shift register to route the first 8 bits of the received frame (bits 0 to 7 of the preamble) to the microcomputer via the processor data bus.

43. Successive bytes of received SCORE control data are transferred in a similar manner except that the strobe pulses are produced by the 8-bit counter instead of the sync. code detector i.e. the Q4 output from the 8-bit counter is applied to the set input of the strobe pulse generator, and reset is applied after the CR time constant.

44. The serial control data output from the shift register (delayed by eight clock periods) is routed via an inverter to a rear panel socket (Data out external) for connection to an external unit using the SCORE exta word facility (see fig.App.21(a)).

SCORE Transmitter

45. The SCORE transmit shift register receives parallel SCORE data frames (words 0, 1, 2 and 5) from the microcomputer (I/O port 0) or serial data frames (external revertive data from an external unit using the extra word facility) and transmits this SCORE data in serial form. For a remote control installation, revertive data resulting from received control data is transmitted back to the receiver control unit, whilst for the master/slave situation using a pair of RA1792 receivers, the forward control data is transmitted from the control receiver to the slave receiver, or revertive data from the slave receiver is transmitted back to the master receiver.

46. At the end of the last but one byte of a SCORE data frame handled by the SCORE receiver, the microcomputer applies a start-in-sync. set pulse to the timing and control circuitry of the SCORE transmitter. This causes the generation of a load pulse which is used to produce the following:

(1) A clock signal for the transmit interrupt latch; the '0' at the D input results in a '1' at the $\overline{Q}$ output which is routed to the interrupt control circuit and via an inverter to the microcomputer (I/O port 1).

(2) The parallel/serial control signal for the output shift register; if the next SCORE frame to be transmitted contains word 0, 1, 2 or 5, then the microcomputer sets line 6 of PIO port 85 to a '1' and the output shift register is set to receive parallel data from the microcomputer. If however, the next frame to be transmitted does not contain a word used by the receiver, then the output shift register is set to receive external serial revertive data (from an external unit using the extra word facility).

(3) A reset signal for an 8-bit counter. This reset signal is maintained until the end of the next load pulse (which is produced by the Q4 output signal from the SCORE receiver 8-bit counter). The two 8-bit counters are then synchronised and successive load pulses are then produced by the SCORE transmitter 8-bit counter. Counter synchronisation becomes relevant should gaps occur during successive received data frames (para. 62).

47. The Q4 output from the 8-bit counter is also applied to the clock input of the external strobe pulse generator. The D input of this stage is controlled by the microcomputer and is only set to a '1' following successful frame comparison of the received SCORE data. The external strobe pulse is then produced and is applied to the external extra word unit to enable the revertive data output.

SCORE Data Input and Output Timing

48. Fig. App.2(a) shows a typical situation where an RA1792 receiver is controlled by an MA 1075 control unit, and an extra-word control unit (using SCORE word 7) connected to the MA1075 controls an external unit connected to the RA1792. Pairs of SCORE control data frames containing words 0, 1, 2 and 5 are produced by the MA1075, and pairs of word 7 frames are inserted into the control data stream from the MA1075 on request by the extra word control unit. The revertive data from the SCORE word 7 controlled unit consists of 40-bit words from bit 8 to bit 47 i.e. the sync code (bits 0 to 7) is not included.

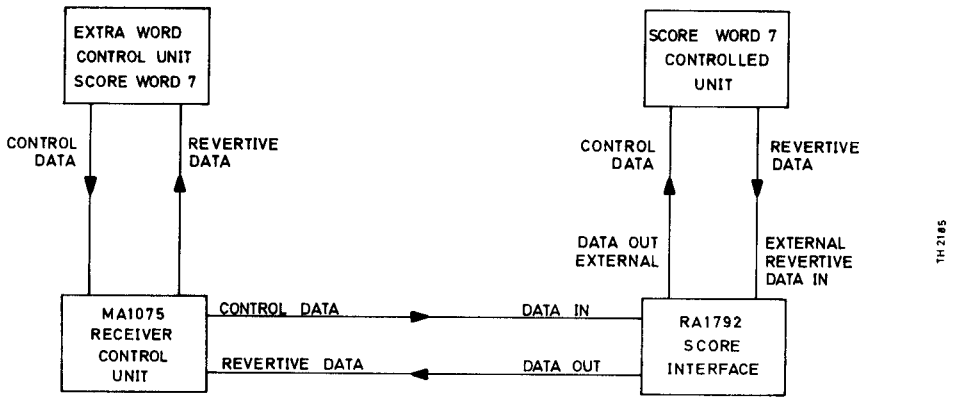


Fig. App. 2 (a) SCORE Data Routing

49. The timing diagram given in fig.App.2.(b) relates to fig.App.2(a) and shows the SCORE data input and output timing as far as the RA1792 SCORE interface is concerned. The DATA IN comprises a pair of word 7 frames (originating from the extra word control unit), two word 1 and two word 2 frames (from the MA1075), two further word 7 frames, and the first of a pair of word 5 frames (from the MA1075). This data is clocked into an 8-bit shift register and is then applied to the microcomputer in parallel bytes. It is also clocked out of the register in serial form for application to the SCORE word 7 controlled unit (DATA OUT EXTERNAL), delayed by eight clock periods due to the action of the shift register.

50. The microcomputer frame-compares the first word 7 frame with the last frame received, and since the two frames do not compare, a SCORE word 0 revertive data frame is produced (DATA OUT). The data content of the first DATA OUT frame shown in fig.App.2(b), marked X, is the result of the previous frame comparison. The next frame comparison undertaken by the microcomputer is between two word 7 frames, and in this example, successful frame comparison is assumed (if the comparison had failed, a further revertive word 0 frame (DATA OUT) would have been produced).

51. The microcomputer also examines the word identification bits of each DATA IN frame. Following the successful frame comparison between a pair of frames not used by the RA1792 i.e. the word 7 frames in this example, a sync. code is loaded into the SCORE transmit output shift register, and the register is then set to allow a serial input. The external strobe pulse is then produced and applied to the SCORE word 7 controlled unit. This responds by applying the revertive 40-bit word 7 data to the SCORE interface where it is clocked into and straight out of the SCORE transmit output shift register, preceded by the sync. code inserted by the microcomputer. This revertive word 7 frame is then routed via the MA1075 to the extra word control unit.

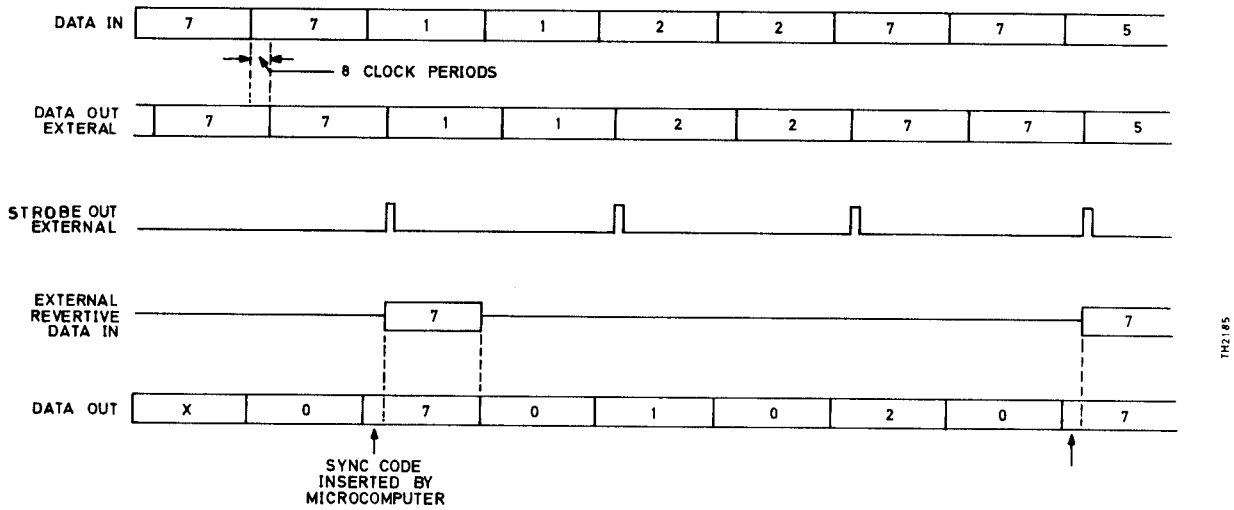


Fig. App. 2(b) Timing Diagram : SCORE Data

52. The next frame comparison takes place between a word 7 frame and a word 1 frame, and this results in a revertive (DATA OUT) word 0 frame. Two word 1 frames are then successfully compared, a word 1 frame is returned, and an external strobe pulse is generated. This pulse is applied to the SCORE word 7 controlled unit but because a further pair of word 7 frames have not been received, no revertive data is available and the strobe pulse has no effect.

User Functions

53. The input and output user functions are handled by a peripheral input/output (PIO) device which interfaces to the microcomputer via two high-speed I/O ports, designated 84 and 85, and a control bus. The frame comparison inhibit input is also routed to the microcomputer via I/O port 85 (bit 7).

CIRCUIT DESCRIPTION (fig. App. 2.4)

SCORE RECEIVER
Sync. Code Detector

54. The inverted SCORE input data (RS-423 or RS-232) is applied via a line receiver, U3A, to the D input of a 4-bit shift register U13B, and via inverter U14D to the D input of an 8-bit shift register U23 (para 57). The Q3 output of U13B is applied to the reset input of a further 4-bit shift register U13A, where the D input is connected to +5V (logic '1'). Data is shifted into these registers on the positive-going transition of the SCORE clock signal from line receiver U3B.

55. When an inverted sync. code is received i.e.1-0-0-0-0-0-X-X, it takes three clock pulses for the first '1' to reach the Q3 output of U13B; this holds U13A in the reset state for the duration of the next clock pulse, and a further four clock pulses are required before the Q4 output of U13A changes to a '1' (table 4). Thus the Q4 output of

Table 4: Sync. Code Detector

SHIFT REGISTER STATES		1	2	3	4	5	6	7	8
U13B	Q 1	1	0	0	0	0	0	X	X
	Q 2	X	1	0	0	0	0	0	X
	Q 3	X	X	1	0	0	0	0	0
	Q 4	X	X	0	1	0	0	0	0
U13A	Q 1	X	X	0	0	1	1	1	1
	Q 2	X	X	0	0	0	1	1	1
	Q 3	0	X	0	0	0	0	1	1
	Q 4	0	0	0	0	0	0	0	1

X = 0 or 1

U13A can only change to a '1' following the occurrence of five consecutive zeros at the D input of U13B. This circuit does not detect the state of the last two bits of the received sync-code but this is subsequently checked by the system software. The '1' at the Q4 output of U13A is applied to the clock input of the strobe pulse generator U10A via glitch suppression components R2, C8.

Strobe Pulse Generator

56. The strobe pulse generator comprises D-type flip-flop U10A. When clocked by the output from the sync. code detector, the '1' at the D input is transferred to the Q output, and reset is applied after the time constant presented by R1 and C7. The nominal 5 microsecond positive-going output pulse is applied to:

(1) the set input of the receiver interrupt latch U10B; the resulting '1' at the Q output is applied to NAND gate U15A of the interrupt control circuit (para 64), and via inverting buffer U14A to the microcomputer as the receive interrupt pending signal.

(2) the strobe input of the 8-bit shift register U23 to load the internal storage latches with the first eight bits (the sync. code) of the received frame (para. 57).

(3) the reset input of an 8-bit counter U11A; this counter produces a positive-going pulse at the Q4 output for every eight SCORE clock cycles following reset, and these pulses are applied to the set input of U10A to produce the strobe pulses for the remaining five bytes of the received data frame. The Q4 output of ML11A is also routed to NAND gate U16A which forms part of the output counter synchronisation circuit (para. 59).

Input Shift Register

57. U23 is an 8-stage serial shift register having a storage latch associated with each stage. The data in each shift register stage is transferred to the storage register when a '1' is applied to the strobe input, and the stored data appears at the Q1 to Q8 parallel outputs when a '1' is present at the enable input. When a '0' is present at the enable input, the Q1 to Q8 outputs are in the high-impedance 3-state condition. The serial output is taken from the Q's pin (where it appears eight clock periods after application to the D input) and is routed to J1 pin 2 via open-collector inverter Q5.

Address Decoder

58. The address decoder makes use of three transmission gates (analogue switches) U21D, U21B and U21C. For a SCORE read operation, the microcomputer sets the IOC3 and IOC7 control bus lines to a '1' and the I/O read line to a '0'. U21D is thus held off, U21B and U21C are turned on, and a '1' from R16 is applied to the enable input of the 8-bit shift register U23, and the parallel data at the Q1 to Q8 output pins is applied to the microcomputer via the processor data bus. The '1' from U21C is also applied to the reset input of the receive interrupt latch U10B, the Q output is reset to '0', and the receive interrupt is cancelled.

SCORE TRANSMITTER

Start-in-Sync. Latch

59. The start-in-sync. latch U22A is reset by the microcomputer during the initialisation routine (I/O port 1 bit 0) and is set by the microcomputer shortly after the start of the last byte of a SCORE data frame handled by the SCORE receiver (I/O port 1 bit 3). The $\overline{Q}$ output of U22A is thus set to a '0', this is routed to NAND gate U16B and the '1' output resets the 8-bit counter U11B. At the same time the Q output of U22A is set to the '1'; the combination of this and the next positive-going pulse from the SCORE receive 8-bit counter U11A (at the end of the last byte of a received data frame - see timing diagram fig. App.2(c)), results in a '0' at the output of NAND gate U16A. This is inverted by NAND gate U16D and a '1' is applied to the set input of the load pulse generator U17B.

Load Pulse Generator

60. The load pulse generator U17B is set either by the action of the start-in-sync. latch (as described in para.59) or subsequently by the Q4 output of the 8-bit counter (via U14E and U16D). In either case, U17B is effectively reset by the next negative-going transition of the SCORE clock, which is applied via inverter U14B (D input at 0V), and thus the positive and negative-going pulses at the Q and $\overline{Q}$ outputs extend for one half of a SCORE clock period.

61. With reference to the timing diagram given in fig. App.2(c), the first and last load pulses shown (U17B outputs) result following the Q4 output of the 8-bit counter U11B. The positive-going pulse at the Q output of U17B is applied to the clock input of the internal/external latch U17A (para.66) and also to the clock input of the start-in-sync. latch U22A; this however, has no effect as the Q output of U22A is already at logic '0'. The negative-going pulse at the $\overline{Q}$ output of U17B is inverted by U16B to reset the 8-bit counter U11B. It is also applied to NAND gate U16C, which forms part of the parallel/serial selection circuit for the output shift register (para.66), and to the clock input of the transmit interrupt latch U22B. Thus at the positive-going transition of the negative-going pulse, the '0' at the D input of U22B results in a '1' at $\overline{Q}$ output; this is routed to the microcomputer via inverter U14F as a transmit interrupt pending signal, and is also applied to NAND gate U15D which forms part of the interrupt control circuitry (para.64). The positive-going transition of the negative-going pulse from the $\overline{Q}$ output of U17B is also used to clock the output enable latch U12B (para.68).

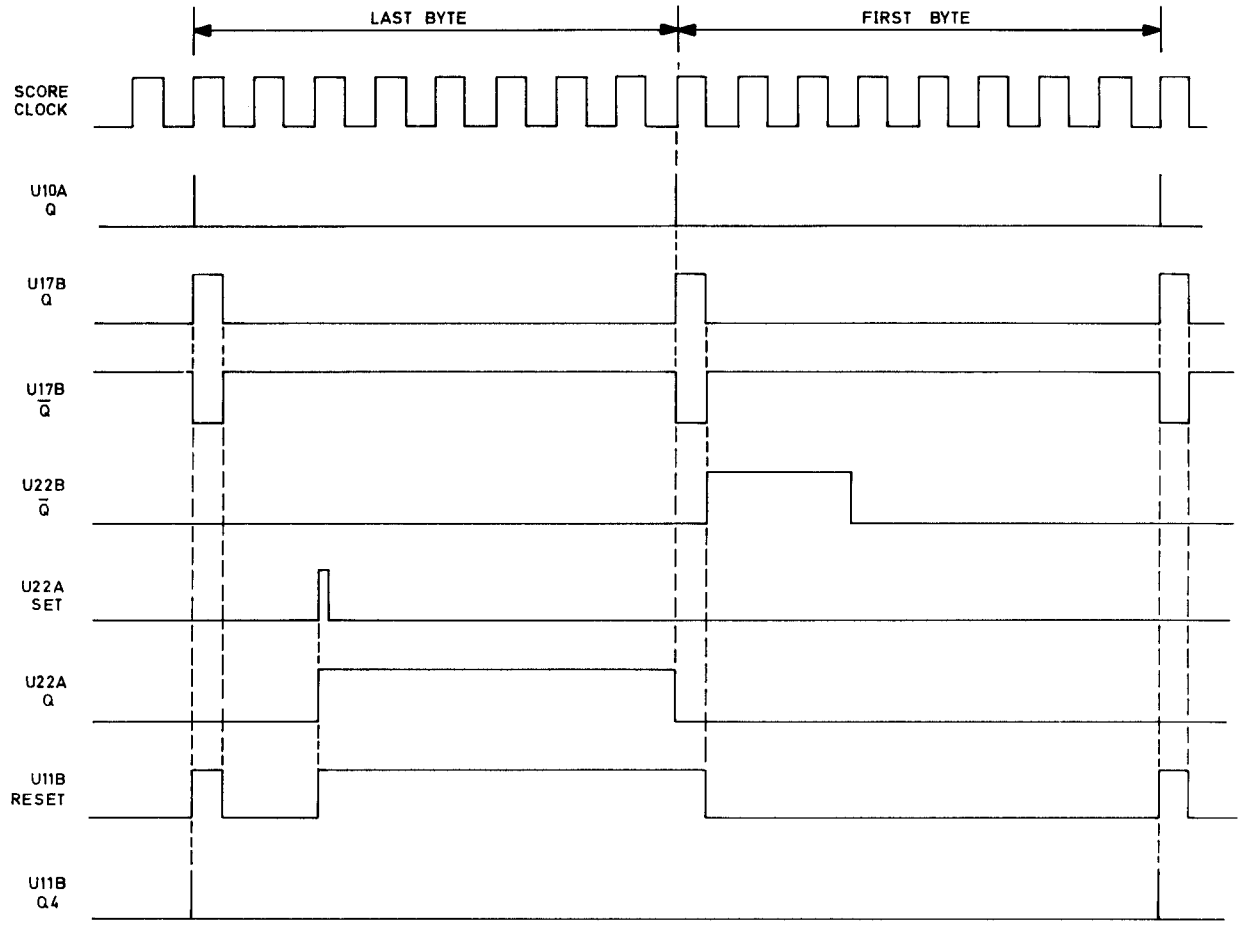


Fig. App. 2(c) Timing Diagram : Counter Synchronisation

62. The second load pulse shown in fig.App.2(c) results from the combination of a '1' at the Q output of the start-in-sync latch U22A and the positive-going output pulse from the 8-bit counter U11A. This time, the positive-going pulse at the Q output of U17B clocks the internal/external latch U17A as before, but also clocks the start-in-sync. latch U22A. The '0' at the D input is transferred to the Q output, is inverted by U16A, and a '1' is thus applied to U16D to allow load pulse generation by the Q4 output signals from the 8-bit counter U11B (applied to the set input of U17B via U14E and U16D). The negative-going pulse at the $\overline{Q}$ output of U17B extends the reset period of U11B for the duration of the pulse and then allows counting to commence so that the first Q4 output pulse from U11B occurs exactly eight SCORE clock periods after the previous Q4 output pulse from 8-bit counter U11A, i.e. synchronism between the two 8-bit counters is established.

63. Synchronisation between the two 8-bit counters is necessary due to the asynchronous nature of the received SCORE data, as illustrated in fig. App.2(d). This shows an example three-clock-period delay between the last byte of one frame and the first byte of the next frame. In this case, the first byte of data transferred to the microcomputer does not constitute a correct sync. code, and the data is rejected. Three clock periods later however, the sync. code detector detects the presence of a correct sync. code, a strobe pulse is produced, and the 8-bit counter U11A (which has reached a count of 3) is reset to zero and starts again. The example 3-bit delay is then automatically transferred to the output 8-bit counter U11B by the action of the synchronisation circuit.

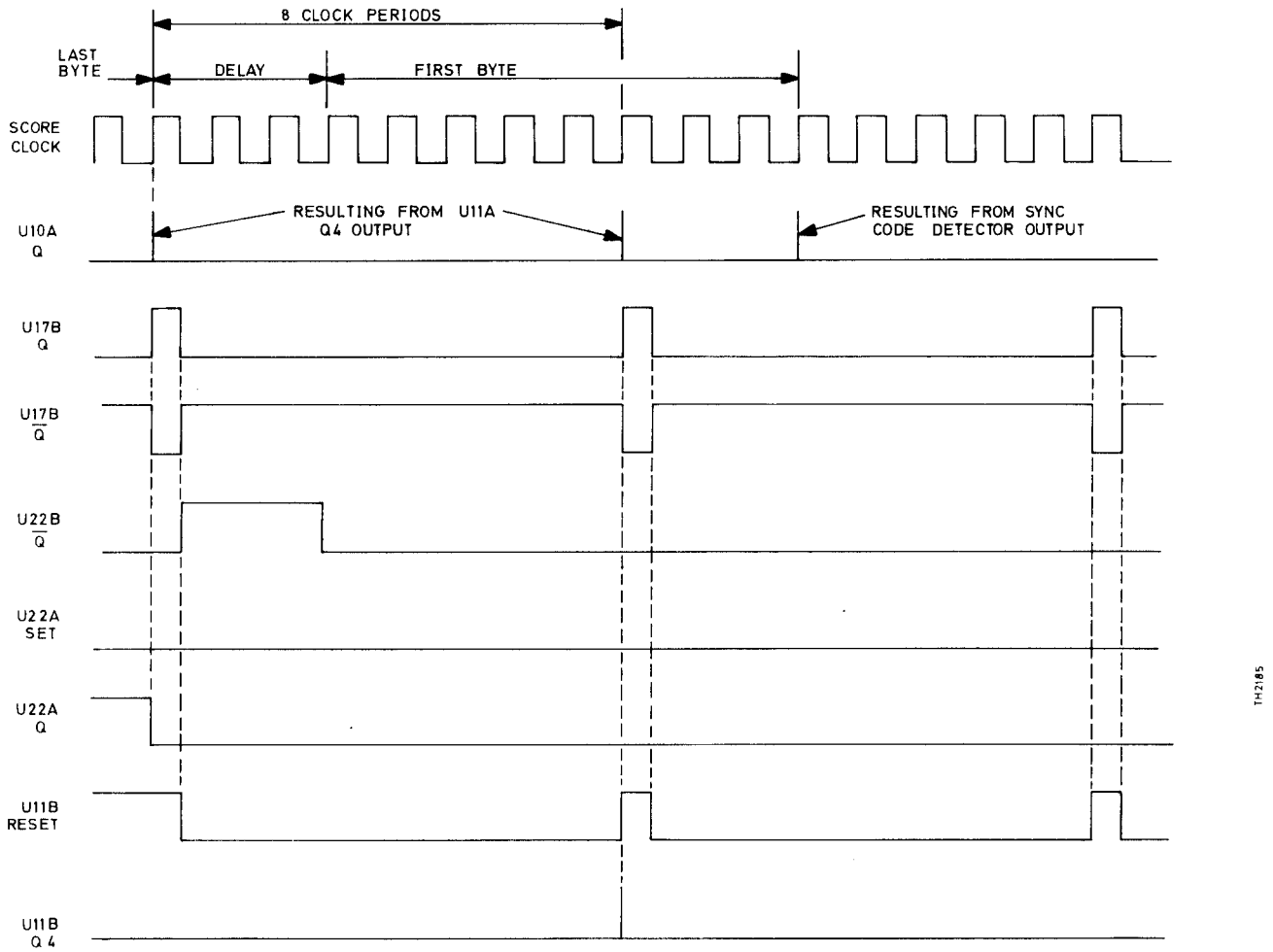


Fig. App. 2(d) Timing Diagram : Delayed SCORE Data

Interrupt Control

64. The logic '1' output signals from the receive and transmit interrupt latches, U10B and U22B respectively, are gated (U15A, U15D) with the respective software - controlled interrupt enable signal from U19 (I/O port 84, bits 6 and 7). The resulting '0' output from either U15A or U15D is inverted by U15C and applied to one input of

U15B. Provided an interrupt request from elsewhere within the receiver is not being serviced, then a '0' is present at P1 pin 28 ($\overline{ICB}$ input); this is applied to the priority in input of U19 to enable the interrupt circuitry, and is inverted by U14B to allow the output from U15C to produce a logic '0' external interrupt signal, which is applied to U19 pin 5. U19 then produces a logic '0' interrupt request signal, which is applied to the microcomputer, and also applies a mask-programmed interrupt vector address (hex 0680) to the microcomputer via the processor data bus. The microcomputer is then forced to execute the interrupt routine pointed to by vector address 0680. Whilst the interrupt routine is in progress, the priority out output from U19 is set to logic '1'; this is applied to the priority in input of the static memory interface (SMI) device in the microcomputer to prevent that device from initiating an interrupt.

External Strobe

65. The external strobe pulse generator U12A is clocked by the Q4 output from the 8-bit counter U11B. When an external strobe pulse is required, the microcomputer routes a '1' to the D input of U12A (strobe enable), this is transferred to the Q output on the positive-going transition of the Q4 output pulse from U11B, and U12A is reset after the time constant presented by R3, C12. The resulting positive-going pulse is inverted by open-collector transistor Q7 and is taken to J1 pin 21 for connection to equipment using the extra word facility.

Internal/External Data Control

66. The output shift register U24 is configured under software control to accept either parallel data from the microcomputer (via I/O port 0) or serial external revertive data at J1 pin 14 (applied to U24 via CR6 and inverting NAND buffer/driver U7B). For internal (parallel) input data operation, the microcomputer routes a '1' to the D input of the internal/external latch U17A; this is transferred to the Q output on the positive-going transition of the positive-going load pulse from U17B, transmission gate U21A is enabled, and the path between I/O port 0 bit 0 and the P8 input of U24 is completed. At the same time the negative going load pulse from U17B is inverted by U16C to momentarily enable the parallel inputs of U24, the parallel data is loaded in, and is then serially clocked out.

67. For external (serial) input data operation, the microcomputer routes a '0' to the D input of U17A; this time U21A is not enabled, the path between I/O port 0 bit 0 and the P8 input of U24 is broken, and U16C applies a '1' to U24 to enable the parallel inputs. The external revertive data is applied to the P8 input of U24 and is then serially clocked out.

68. The SCORE data and clock output driver U9 is enabled by the application of a '0' at pin 3. When the RA1792 receiver is switched on, the initialisation routine latches a '1' at U19 I/O port 84 bit 5. This is routed to the D input of the output enable latch U12B, and after the first load pulse from U17B, a permanent '0' is established at the $\overline{Q}$ output. The '1' at the Q output is applied to open collector

transistor Q9, but in the RA1792 no connection is made to J1 pin 1.

PERIPHERAL INPUT/OUTPUT (PIO) DEVICE

69. The PIO device U19 is mainly used for interrupt control purposes but is also used for the input output user function information. The device has two input/output ports, logic to handle an external interrupt (para.64), and a programmable interval timer (which is not used in this application). An 8-bit bi-directional data bus is used for the transfer of data between the PIO and the microcomputer, and a 5-bit bus (ROMC0 to ROMC4) is used for control purposes. A block diagram of the device is given in fig. App.2.(e).

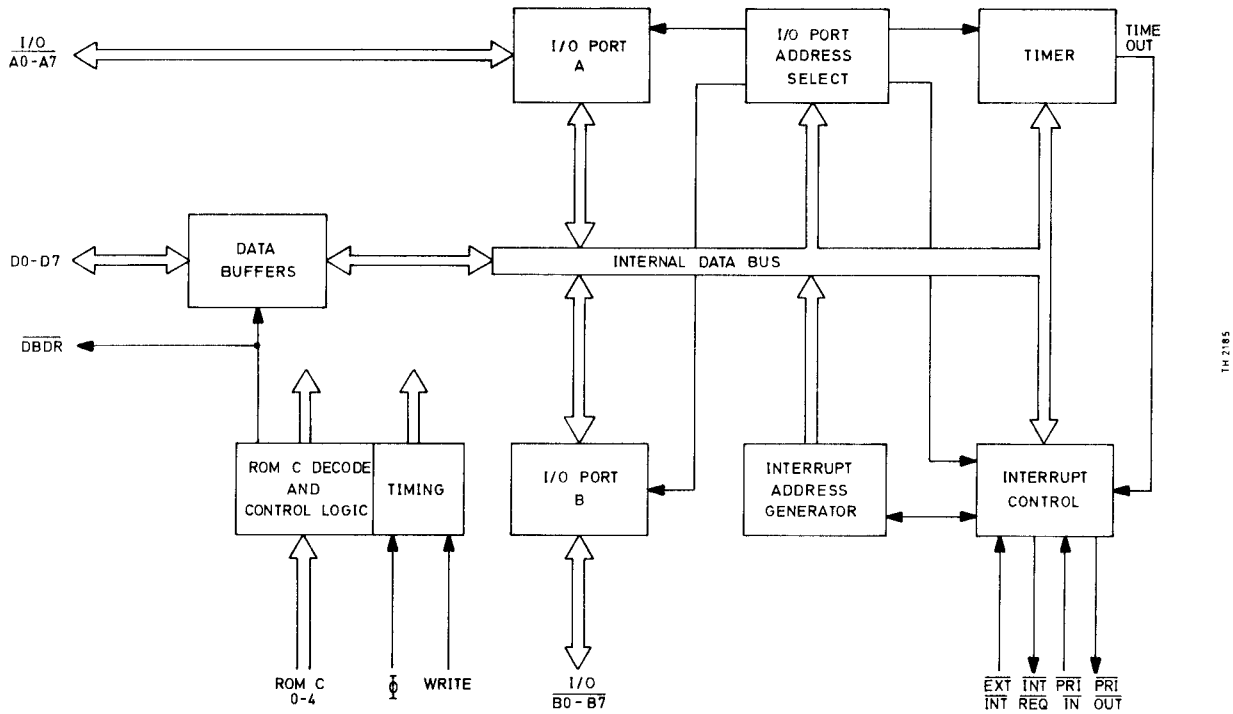


Fig. App.2(e) Block Diagram : 3861 PIO

70. The PIO device has four addressable ports, each with an assigned address. Two ports are used as 8-bit input/output ports (designated A and B in fig. App.2.(e)), whilst the remaining two ports are for the programmable timer and interrupt control purposes. The designated port addresses for the version of the 3861 PIO used in this application are in the range 04 to 07, as listed in Table 5. These addresses are however, modified by the action of the control bus (ROMC) decoder (para.75) so that the PIO responds to addresses in the range 84 to 87. Note that the timer and interrupt control ports are write only ports i.e. the contents of the associated port registers cannot be read by the microcomputer.

TABLE 5 : PIO PORT ADDRESSES

Address				Assigned To
Physical		Virtual		
Hex	Binary	Hex	Binary	
04	00000100	84	10000100	I/O Port A
05	00000101	85	10000101	I/O Port B
06	00000110	86	10000110	Interrupt Control Register
07	00000111	87	10000111	Programmable Timer

Device Connections

71. (1) Φ and WRITE: These are clock input signals derived by the microcomputer.

(2) ROMC0 to ROMC4: These are the control input signals from the microcomputer.

(3) DB0 to DB7: The bi-directional data bus lines which link the PIO to the microcomputer.

(4) $\overline{\text{EXT INT}}$: External interrupt input. When an external circuit applies a '0' to this input, an external interrupt request is latched into the PIO provided the interrupt control register has been set to allow external interrupts. The PIO subsequently communicates this interrupt request to the microcomputer via the $\overline{\text{INT REQ}}$ line.

(5) $\overline{\text{PRI IN}}$: Priority in. A '1' at this input denotes that a higher priority peripheral has a pending interrupt request. If the PIO receives an interrupt request, it is latched into the PIO but will not be serviced until a '0' is present at the $\overline{\text{PRI IN}}$ input.

(6) $\overline{\text{PRI OUT}}$: Priority out. This output signal is routed to the $\overline{\text{PRI IN}}$ input of the static memory interface unit in the microcomputer module. A '1' on this line denotes that the PIO has a pending interrupt request.

(7) $\overline{\text{INT REQ}}$: Interrupt request. A logic '0' on this output line is routed to the microcomputer to initiate the interrupt routine.

(8) $\overline{\text{DBDR}}$: Data bus drive. This output goes to a '0' whenever the PIO is driving the data bus as an output. This output is not used in this application.

(9) $\overline{\text{I/O A0-A7}}$ & $\overline{\text{I/O B0-B7}}$: Two bi-directional 8-bit input/output ports, A and B. In this application these ports respond to addresses 84 and 85 respectively.

Control Bus

72. The control bus, comprising the five lines labelled ROMC0 to ROMC4 conveys control signals to the PIO and also to the static memory interface (on the microcomputer board). The ROMC states decoded by the PIO are given in Table 5. Note that all ROMC states not listed in table 6 are decoded as 'no-operation'.

Instruction Execution

73. The microcomputer input/output instructions place the required I/O port address on the processor data bus during one instruction cycle, and then use the processor data bus in the following instruction cycle to carry out the actual I/O data transfer. The ROMC lines from the microcomputer (hex. states 1A and 1B) signal the PIO that an I/O data movement is occurring during the current instruction cycle. Thus for ROMC I/O transfer states 1A and 1B (table 5) the PIO requires to know whether the contents of the data bus during the previous instruction cycle matched any of the four assigned I/O addresses. This is accomplished by the I/O port address selection logic which constantly monitors the data bus. When an address match is detected, the information is held through the following instruction cycle.

74. Read instructions that select a port (addresses 84 and 85) cause the contents of the selected port to be placed on the processor data bus during the read instruction cycle. For write instructions, the PIO accepts a byte from the processor bus and loads it into one of the I/O ports or the interrupt control register (the programmable timer is not used in this application). Each I/O port output line is latched and thus holds the data transferred during the last I/O write instruction.

TABLE 6 : DECODED ROMC STATES

ROMC STATE		PIO FUNCTION
HEX	BINARY	
0F	01111	If an interrupt request is pending and $\overline{\text{PRI IN}}$ is at '0', the lower half of the interrupt vector address (80) is placed on the data bus.
10	10000	Place interrupt circuitry in an inhibit state that prevents altering the interrupt chain.
13	10011	If an interrupt request is pending and $\overline{\text{PRI IN}}$ is at '0', the upper half of the interrupt vector address (06) is placed on the data bus and the interrupt circuit is reset.
1A	11010	If an I/O port address was present on the data bus during the previous instruction cycle, move current contents of data bus into the appropriate port (I/O A, I/O B, timer or interrupt control).
1B	11011	If I/O port address 84 or 85 was present on the data bus during the previous instruction cycle, move contents of appropriate I/O port (I/O A or I/O B) onto the data bus.

Control Bus Decoder

75. The control bus decoder consists of a magnitude comparator U20 and a quad transmission gate U25. It monitors the ROMC control bus lines and when the 03 state is present, it inverts the level present on the PB7 processor data bus line which is applied to the PIO (U19 pin 7). Thus when an address in the range 84 to 87 is present on the processor data bus, it appears at the PIO data bus as an address in the range 04 to 07, i.e. the physical address range of the four PIO ports. The action of the circuit is as follows.

76. The magnitude comparator U20 produces a '1' at the A = B output when the logic levels at the A inputs are equal to these at the B inputs, and a '1' is also present at the A = B input. Thus when ROMC lines 0 and 1 are both at '1' and lines 2 to 4 are at '0' (03 code), a '1' is produced at the A = B output. This enables U25A and U25C, the '0' from U25A disables U25B, and the level present at the PB7 data bus line is inverted by U25D before application to pin 7 of U19 via U25C. For any other

ROMC code, the A = B output of U20 is at '0', U25A and U25C are disabled, and U25B is enabled to connect the PB7 data bus line directly to pin 7 of U19.

77. The microcomputer applies 03 to the ROMC lines each time a PIO port address is applied to the data bus. As far as the PIO device is concerned, ROMC state 03 is a 'no-operation' (para. 72).

USER FUNCTIONS

78. The input user functions are applied to the PIO (I/O port 85) via inverting buffer/drivers U5A, U5B, U6A and U6B. The output user functions from the PIO (I/O port 84) are routed to rear panel connector J1 via open-collector inverters Q1 to Q4. The new data output request signal from Q8 is not used in this application.

INTERNAL CLOCK GENERATOR

79. This uses the otherwise spare section of the quad line receiver U3C. R15 is selected on test to produce a squarewave output at approximately 6KHz.

-5V SUPPLY

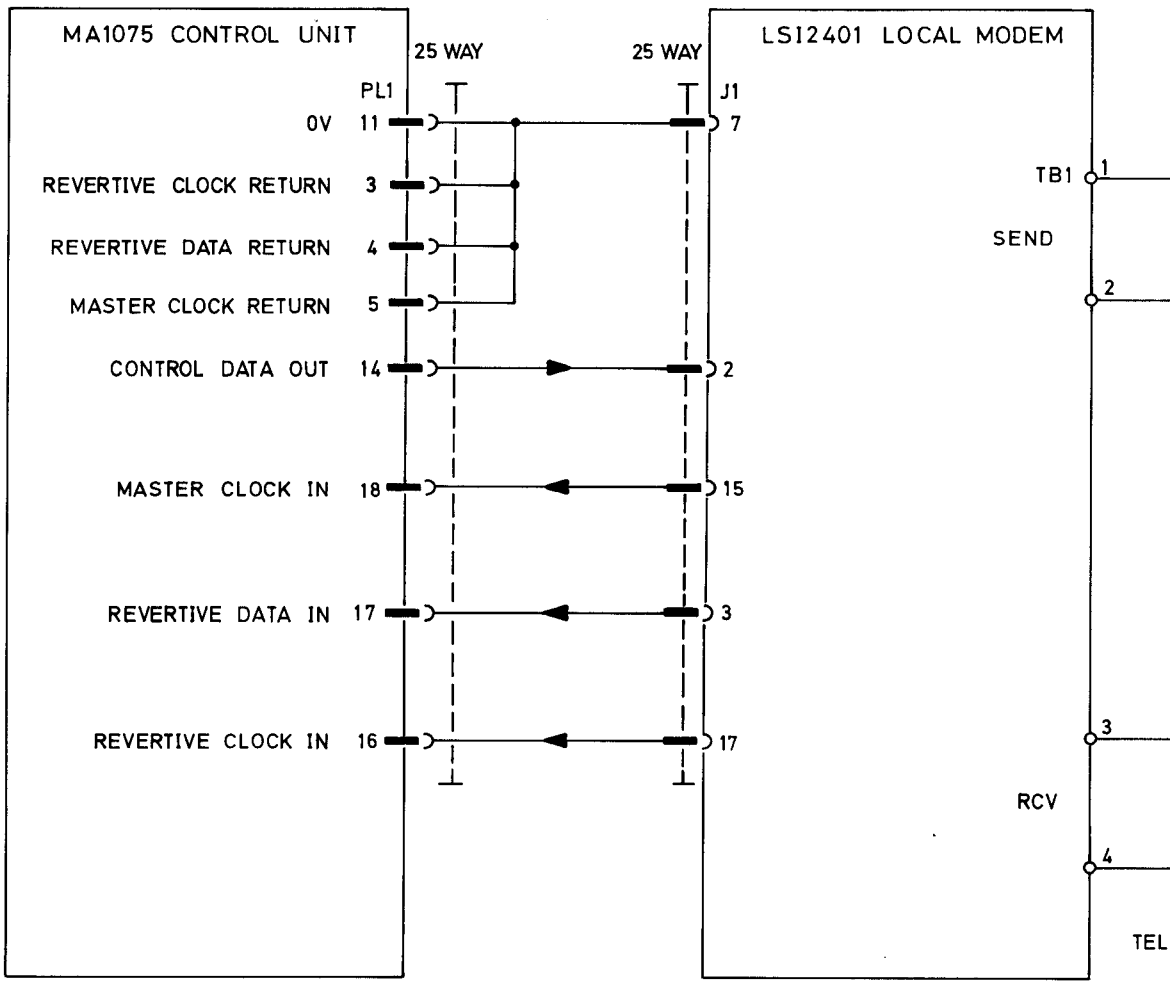
80. The -5V supply required by the line driver device U9 is provided by three-terminal regulator U18 which is powered from the -15V supply at P1 pin 23.

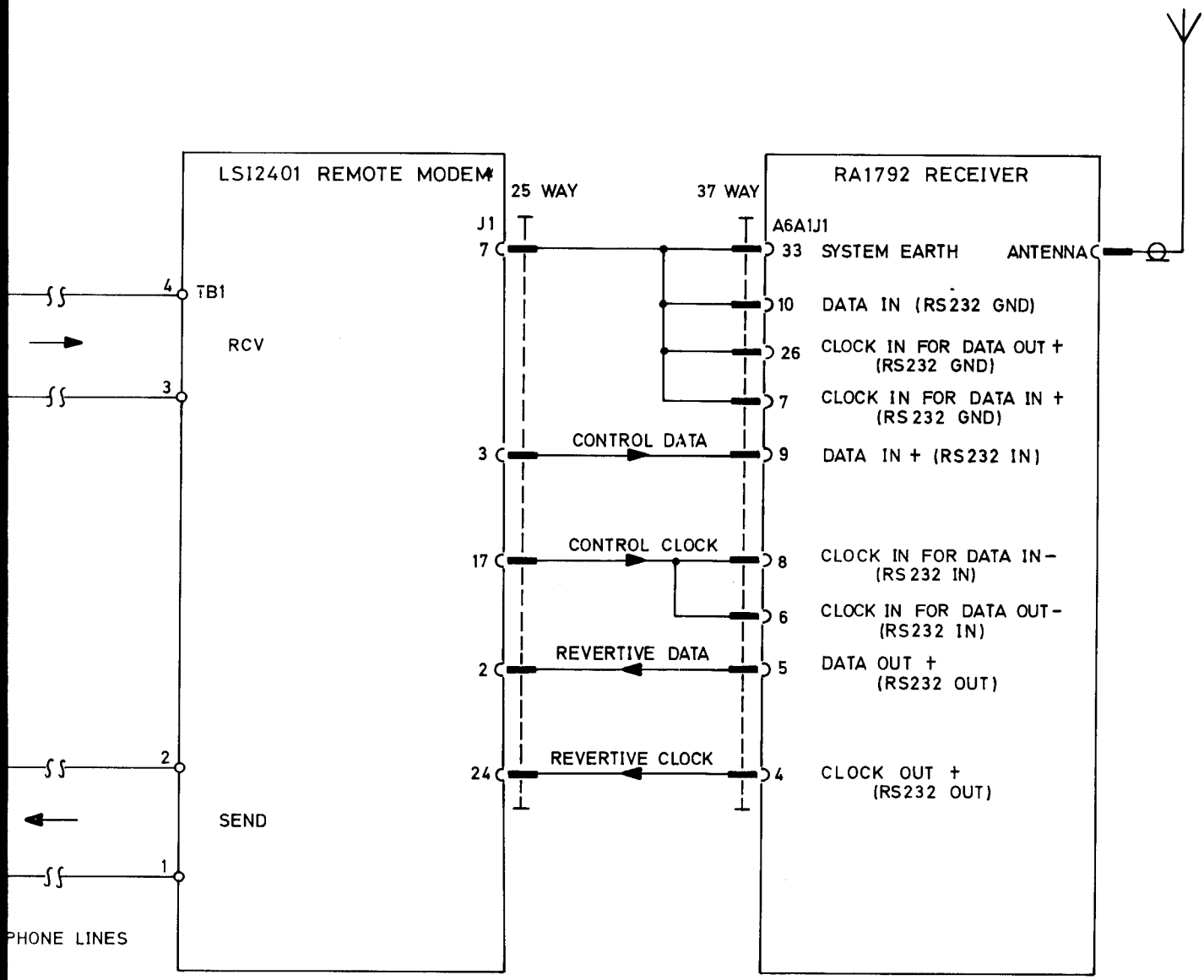
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SCORE INTERFACE BOARD (STO 8459)			
Resistors					
R1	68 k	Metal Oxide		2	916478
R2	68 k	Metal Oxide		2	916478
R3	68 k	Metal Oxide		2	916478
R4	68 k	Metal Oxide		2	916478
R5	68 k	Metal Oxide		2	916478
R6		Not used			
R7	22 k	Metal Oxide		2	913493
R8	10 k	Metal Oxide		2	914042
R9	10 k	Metal Oxide		2	914042
R10	10 k	Metal Oxide		2	914042
R11	10 k	Metal Oxide		2	914042
R12	10 k	Metal Oxide		2	914042
R13	15 k	Metal Oxide		2	920645
R14	33 k	Metal Oxide		2	913495
R15	15k to 56k	Selected on test			
R16	1 k	Metal Oxide		2	913489
R17	10 k	Metal Oxide		2	914042
R18	10 k	Metal Oxide		2	914042
R19	10 k	Metal Oxide		2	914042
R20	10 k	Metal Oxide		2	914042
Capacitors			Volts		
C1	0.1	Disc Ceramic	50	20	938406
C2	0.22	Disc Ceramic	50	20	938676
C3	.01	Disc Ceramic	50	20	938053
C4	22	Tantalum	10	20	921090
C5	6.8	Tantalum	10	20	938031
C6	6.8	Tantalum	10	20	938031
C7	100p	Disc Ceramic	500	10	938556
C8	47p	Disc Ceramic	500	10	917418
C9	47p	Disc Ceramic	500	10	917418
C10	47p	Disc Ceramic	500	10	917418
C11	47p	Disc Ceramic	500	10	917418
C12	100p	Disc Ceramic	500	10	938556
C13	.01	Disc Ceramic	50	20	938053
C14	47p	Disc Ceramic	500	10	917418

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
J1		Socket 37-way			938678
		Mating plug, 37-way			916507
		Shell, junction			918105
		Retainer			914245
P1		Plug, 50-way PCB			A07881
Diodes					
CR1		Silicon IN916			913480
CR2		Silicon IN916			913480
CR3		Silicon IN916			913480
CR4		Silicon IN916			913480
CR5		Silicon IN916			913480
CR6		Silicon IN916			913480
CR7		Silicon IN916			913480
CR8		Silicon IN916			913480
Transistors					
Q1		NPN Silicon IN3904			914046
Q2		NPN Silicon IN3904			914046
Q3		NPN Silicon IN3904			914046
Q4		NPN Silicon IN3904			914046
Q5		NPN Silicon IN3904			914046
Q6		NPN Silicon IN3904			914046
Q7		NPN Silicon IN3904			914046
Q8		NPN Silicon IN3904			914046
Q9		NPN Silicon IN3904			914046
Integrated Circuits					
U1	10 k	Resistor Network, SIL			933750
U2	68 k	Resistor Network, DIL			938680
U3		Quad line receiver 26L532			938683
U4		Not used			
U5		Dual 2-input NAND buffer 40107			928188
U6		Dual 2-input NAND buffer 40107			928188
U7		Dual 2-input NAND buffer 40107			928188
U8		Dual 2-input NAND buffer 40107			928188
U9		Dual RS422 line driver 26LS30			938684
U10		Dual D-type flip-flop 4013			926860

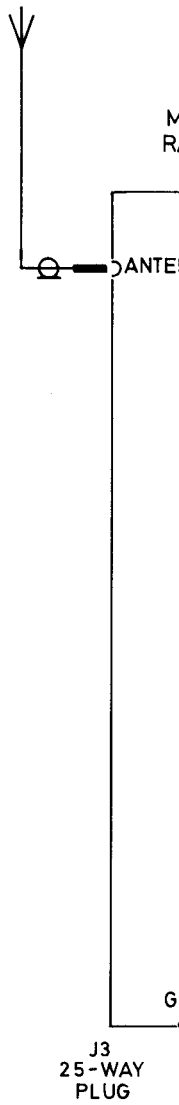
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SCORE INTERFACE BOARD (STO 8459)			
Resistors					
R1	68 k	Metal Oxide		2	916478
R2	68 k	Metal Oxide		2	916478
R3	68 k	Metal Oxide		2	916478
R4	68 k	Metal Oxide		2	916478
R5	68 k	Metal Oxide		2	916478
R6		Not used			
R7	22 k	Metal Oxide		2	913493
R8	10 k	Metal Oxide		2	914042
R9	10 k	Metal Oxide		2	914042
R10	10 k	Metal Oxide		2	914042
R11	10 k	Metal Oxide		2	914042
R12	10 k	Metal Oxide		2	914042
R13	15 k	Metal Oxide		2	920645
R14	33 k	Metal Oxide		2	913495
R15	15k to 56k	Selected on test			
R16	1 k	Metal Oxide		2	913489
R17	10 k	Metal Oxide		2	914042
R18	10 k	Metal Oxide		2	914042
R19	10 k	Metal Oxide		2	914042
R20	10 k	Metal Oxide		2	914042
Capacitors			Volts		
C1	0.1	Disc Ceramic	50	20	938406
C2	0.22	Disc Ceramic	50	20	938676
C3	.01	Disc Ceramic	50	20	938053
C4	22	Tantalum	10	20	921090
C5	6.8	Tantalum	10	20	938031
C6	6.8	Tantalum	10	20	938031
C7	100p	Disc Ceramic	500	10	938556
C8	47p	Disc Ceramic	500	10	917418
C9	47p	Disc Ceramic	500	10	917418
C10	47p	Disc Ceramic	500	10	917418
C11	47p	Disc Ceramic	500	10	917418
C12	100p	Disc Ceramic	500	10	938556
C13	.01	Disc Ceramic	50	20	938053
C14	47p	Disc Ceramic	500	10	917418

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
U11		Dual BCD Up- Counter 4518			928002
U12		Dual D-type flip-flop 4013			926860
U13		Dual 4-bit shift register 4015			930973
U14		Hex inverting buffer 4049			930033
U15		Quad 2-input NAND gate 4011			920028
U16		Quad 2-input NAND gate 4011			920028
U17		Dual D-type flip flop 4013			926860
U18		-5V 3-terminal regulator 79M05			938679
U19		PIO 3861A			938687
U20		Magnitude comparator 4585			938686
U21		Quad transmission gate 4066			930148
U22		Dual D-type flip flop 4013			926860
U23		8-Stage Shift register 4094			929324
U24		8-Stage Shift register 4014			930972
U25		Quad Transmission gate 4066			930148
U26	22 k	Resistor network SIL			938682

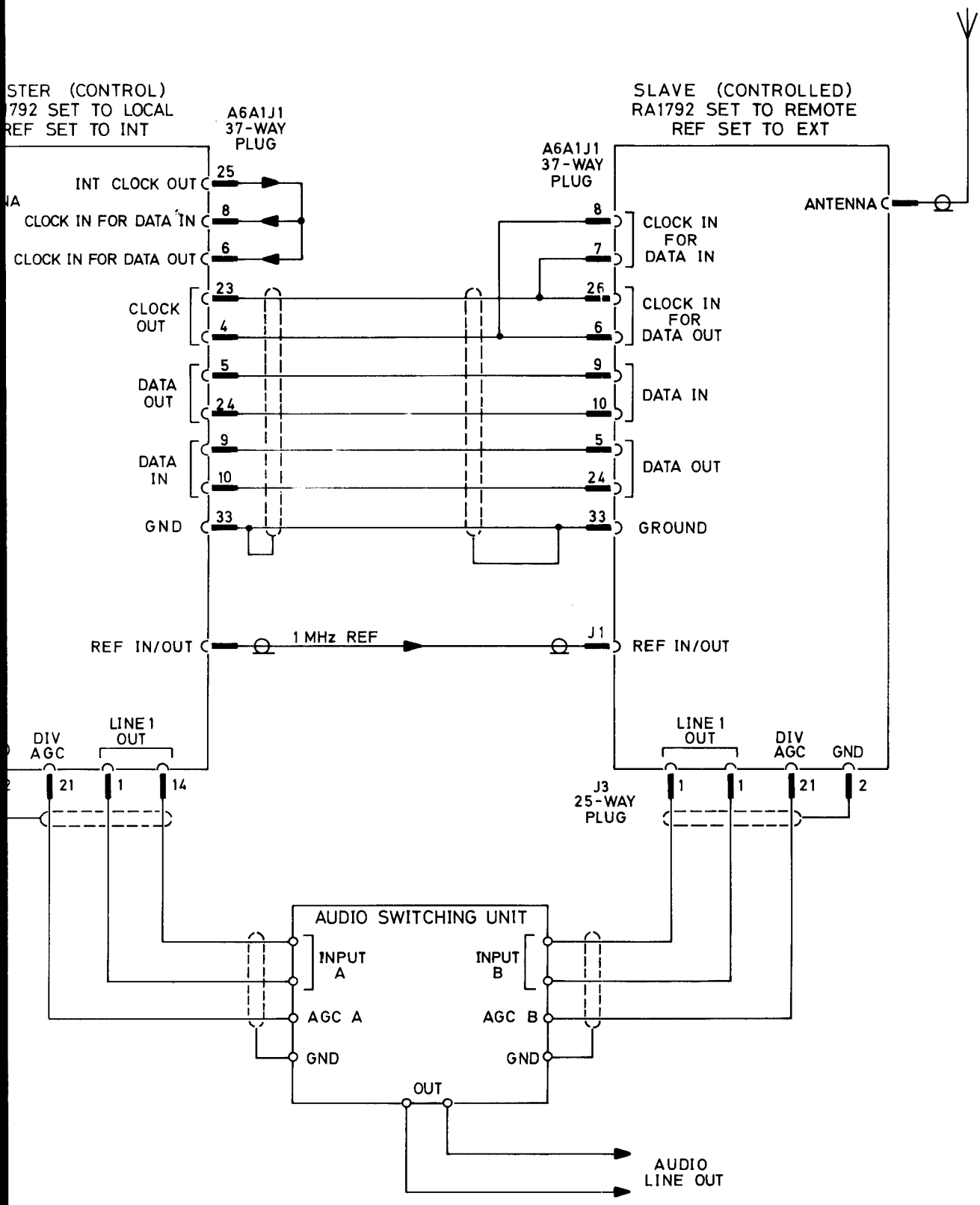

MA1075 CONTROL UNIT
25 WAY
25 WAY
LS12401 LOCAL MODEM
PL1
J1
0V 11
7
REVERTIVE CLOCK RETURN 3
REVERTIVE DATA RETURN 4
MASTER CLOCK RETURN 5
CONTROL DATA OUT 14
2
MASTER CLOCK IN 18
15
REVERTIVE DATA IN 17
3
REVERTIVE CLOCK IN 16
17
TB1
1
SEND
2
3
RCV
4
TEL



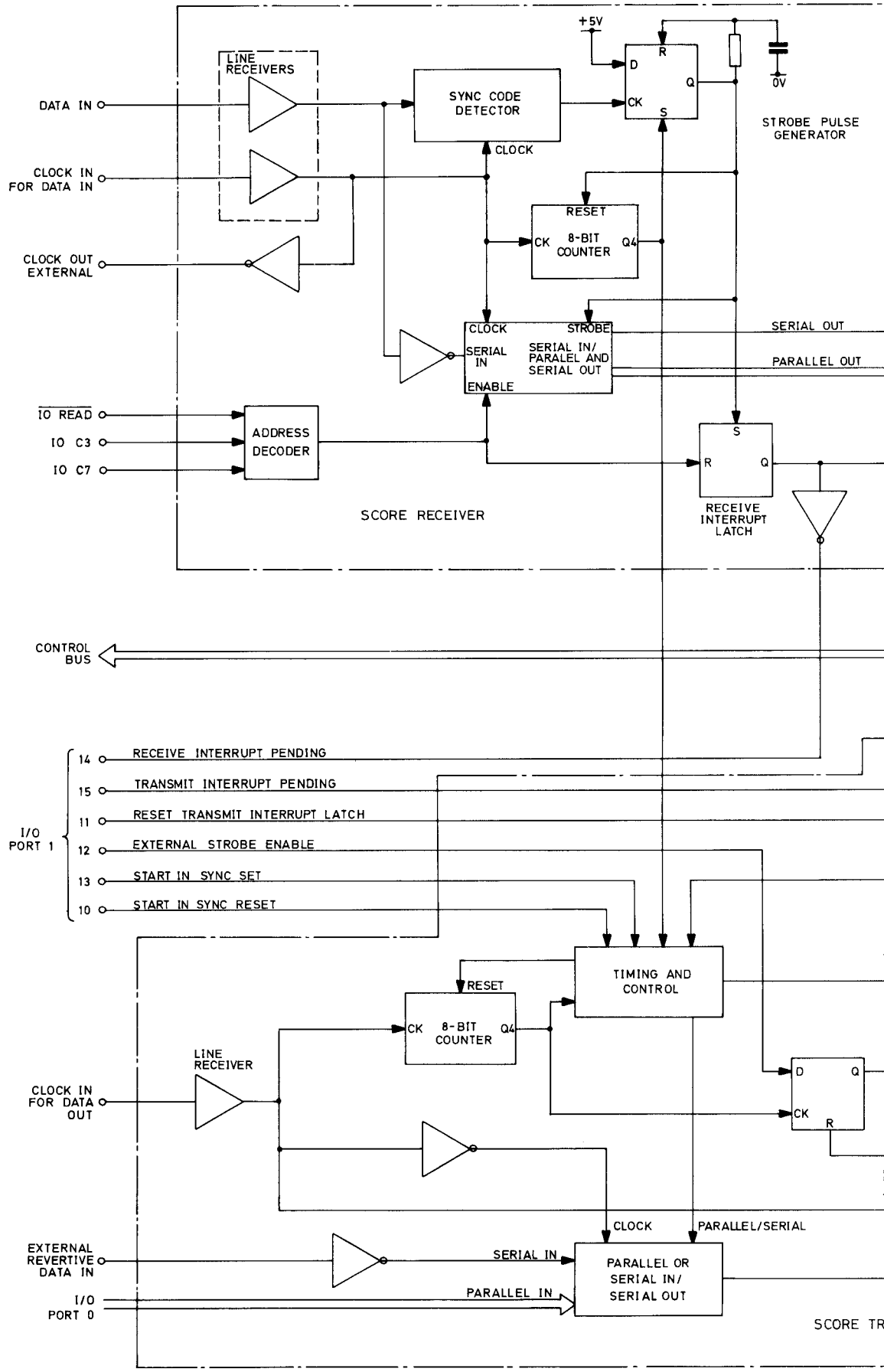
Interconnection Diagram : Typical
Remote Control Installation Fig. App.2.1

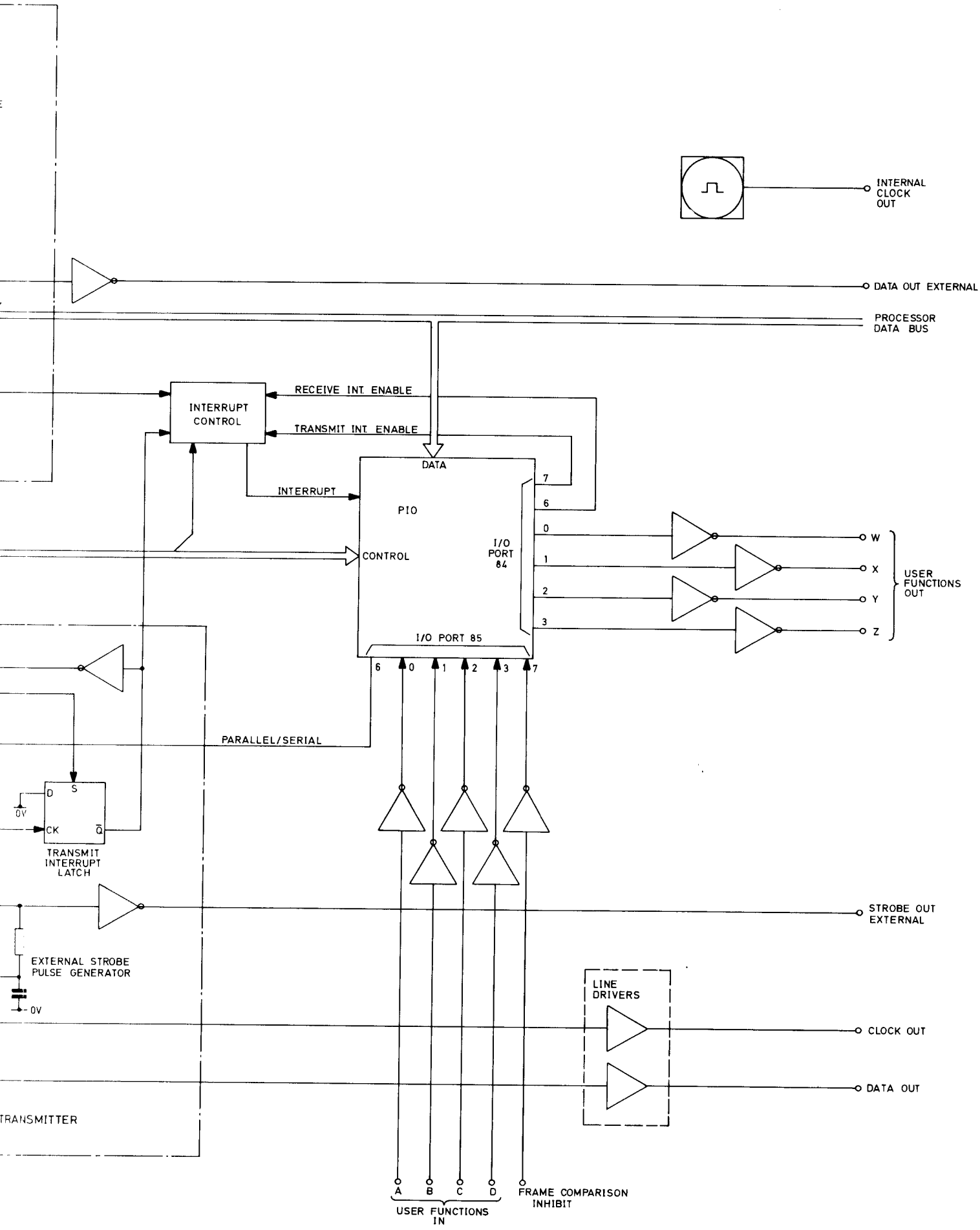


RACAL
TH2185



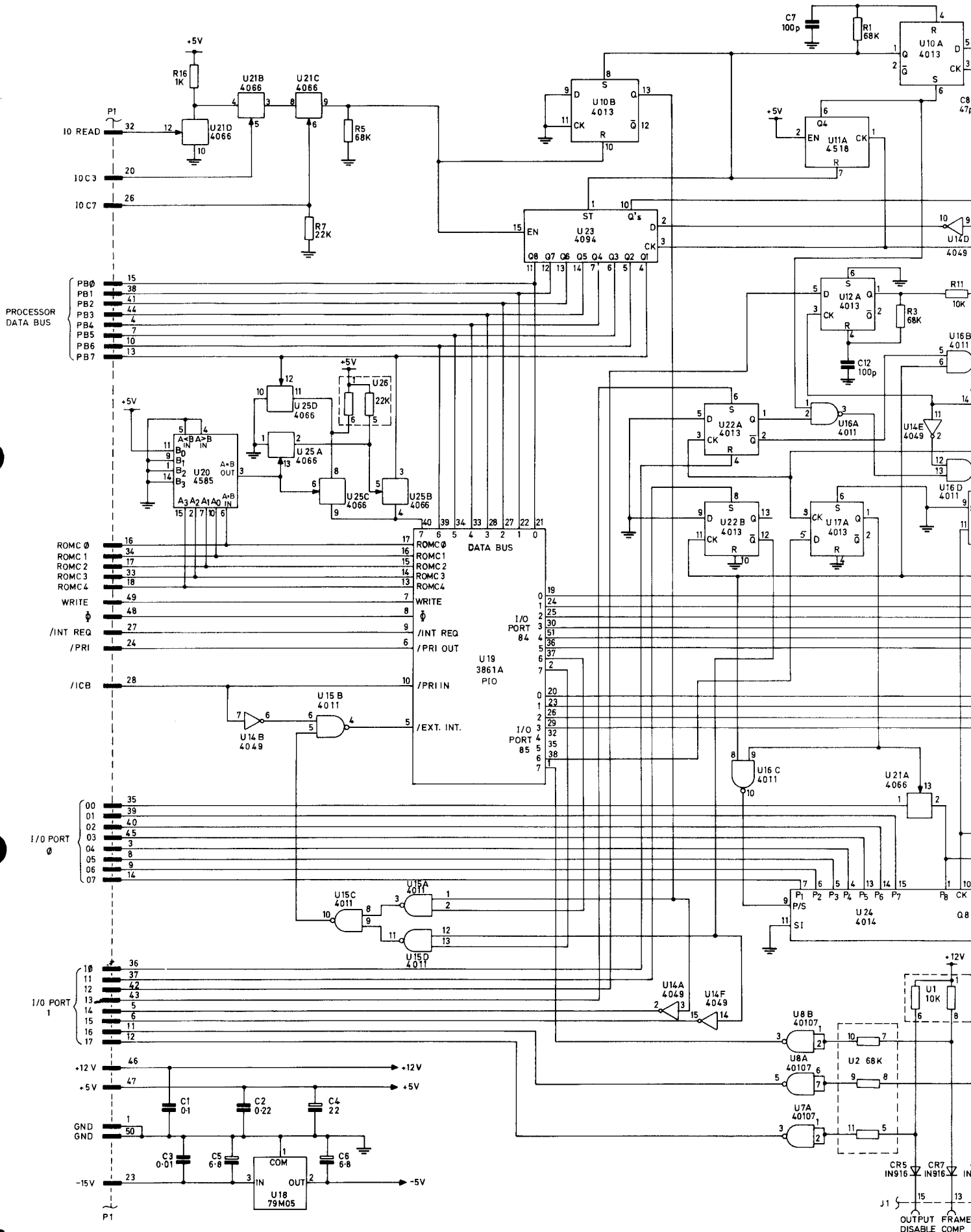
Interconnection Diagram : Typical
Space Diversity Installation Fig. App.2·2


+5V
R
D
Q
CK
S
0V
STROBE PULSE GENERATOR
LINE RECEIVERS
DATA IN
CLOCK IN FOR DATA IN
CLOCK OUT EXTERNAL
SYNC CODE DETECTOR
CLOCK
RESET
CK
8-BIT COUNTER
Q4
CLOCK
STROBE
SERIAL IN
SERIAL IN/ PARALEL AND SERIAL OUT
ENABLE
SERIAL OUT
PARALLEL OUT
IO READ
IO C3
IO C7
ADDRESS DECODER
S
R
Q
RECEIVE INTERRUPT LATCH
SCORE RECEIVER
CONTROL BUS
I/O PORT 1
14
RECEIVE INTERRUPT PENDING
15
TRANSMIT INTERRUPT PENDING
11
RESET TRANSMIT INTERRUPT LATCH
12
EXTERNAL STROBE ENABLE
13
START IN SYNC SET
10
START IN SYNC RESET
TIMING AND CONTROL
RESET
CK
8-BIT COUNTER
Q4
LINE RECEIVER
CLOCK IN FOR DATA OUT
D
Q
CK
R
CLOCK
PARALLEL/SERIAL
EXTERNAL REVERTIVE DATA IN
SERIAL IN
PARALLEL OR SERIAL IN/ SERIAL OUT
I/O PORT 0
PARALLEL IN
SCORE TR



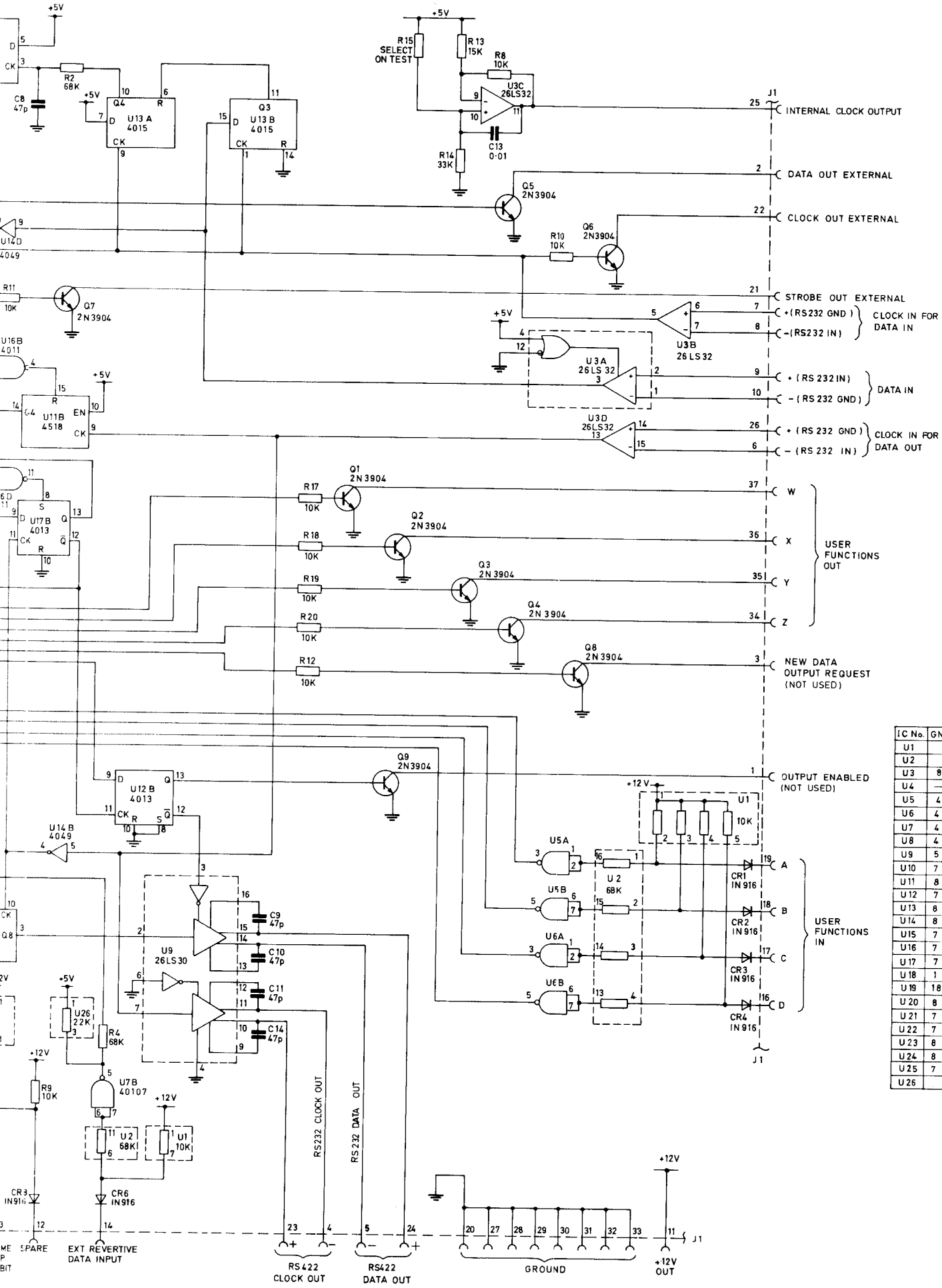
Block Diagram :
SCORE Interface Board

Fig. App 2.3



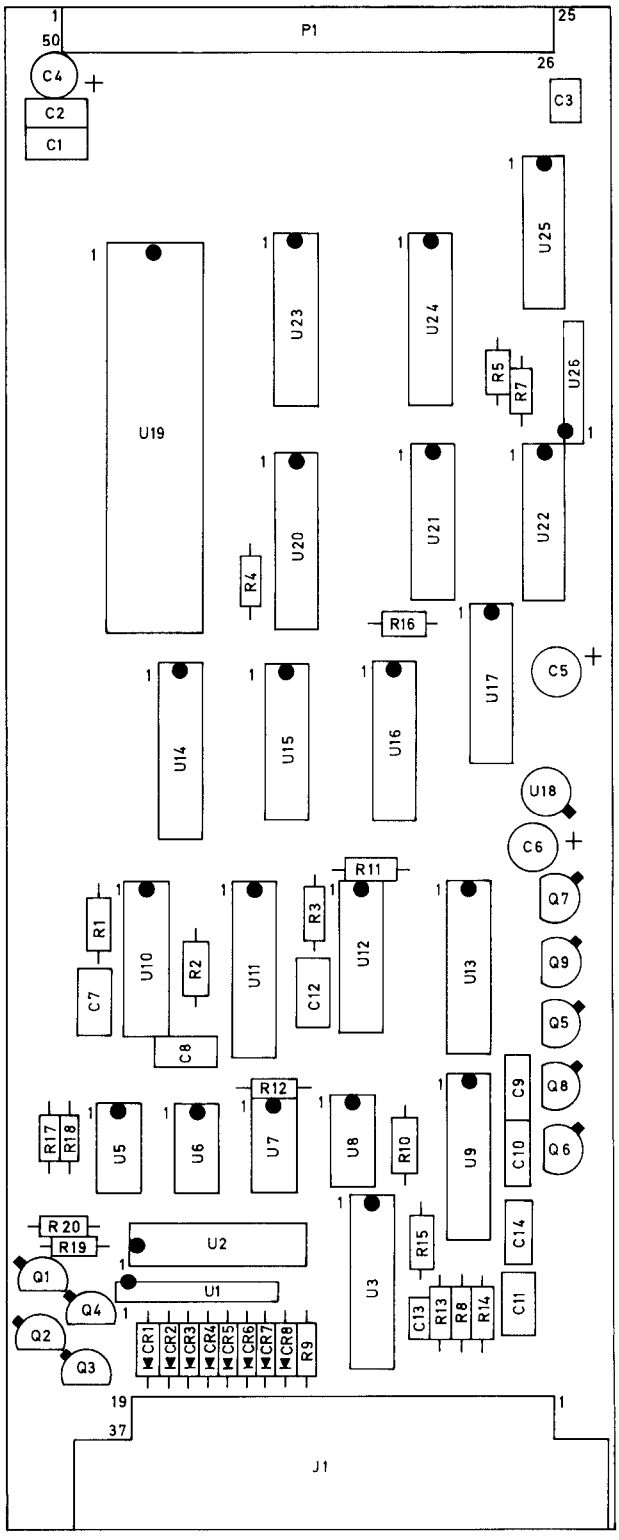
RACAL

TH 1496	EO 8458
2	



IC No.	GND	+5V	+12V	-5V	
U1			1		—
U2					—
U3	8	16			26LS
U4	—	—	—	—	—
U5	4		8		401
U6	4		8		401
U7	4		8		401
U8	4		8		401
U9	5	1		8	26LS
U10	7	14			4013
U11	8	16			451
U12	7	14			401
U13	8	16			401
U14	8	1			404
U15	7	14			401
U16	7	14			401
U17	7	14			4013
U18	1			2	79M
U19	18	4	3		386
U20	8	16			4585
U21	7	14			4066
U22	7	14			4013
U23	8	16			4094
U24	8	16			4014
U25	7	14			4066
U26		1			—

Circuit: SCORE Interface Module A6 A1 **Fig. App. 2**



RACAL
TH1496 | D08459
1

Layout : SCORE Interface Board A6A1

Fig. App. 2.5

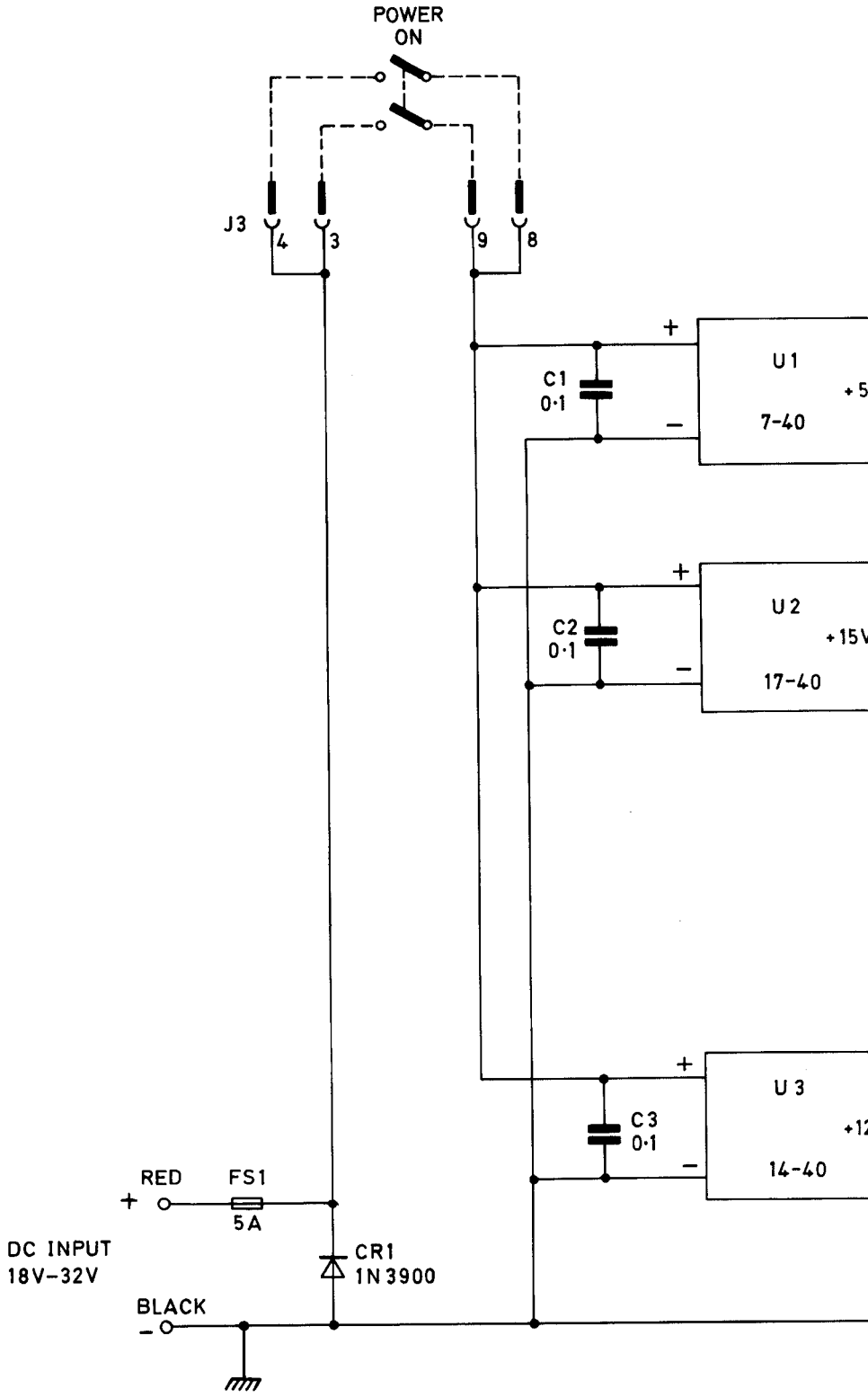
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SCORE INTERFACE BOARD (STO 8459)			
Resistors					
R1	68 k	Metal Oxide		2	916478
R2	68 k	Metal Oxide		2	916478
R3	68 k	Metal Oxide		2	916478
R4	68 k	Metal Oxide		2	916478
R5	68 k	Metal Oxide		2	916478
R6		Not used			
R7	22 k	Metal Oxide		2	913493
R8	10 k	Metal Oxide		2	914042
R9	10 k	Metal Oxide		2	914042
R10	10 k	Metal Oxide		2	914042
R11	10 k	Metal Oxide		2	914042
R12	10 k	Metal Oxide		2	914042
R13	15 k	Metal Oxide		2	920645
R14	33 k	Metal Oxide		2	913495
R15	15k to 56k	Selected on test			
R16	1 k	Metal Oxide		2	913489
R17	10 k	Metal Oxide		2	914042
R18	10 k	Metal Oxide		2	914042
R19	10 k	Metal Oxide		2	914042
R20	10 k	Metal Oxide		2	914042
Capacitors			Volts		
C1	0.1	Disc Ceramic	50	20	938406
C2	0.22	Disc Ceramic	50	20	938676
C3	.01	Disc Ceramic	50	20	938053
C4	22	Tantalum	10	20	921090
C5	6.8	Tantalum	10	20	938031
C6	6.8	Tantalum	10	20	938031
C7	100p	Disc Ceramic	500	10	938556
C8	47p	Disc Ceramic	500	10	917418
C9	47p	Disc Ceramic	500	10	917418
C10	47p	Disc Ceramic	500	10	917418
C11	47p	Disc Ceramic	500	10	917418
C12	100p	Disc Ceramic	500	10	938556
C13	.01	Disc Ceramic	50	20	938053
C14	47p	Disc Ceramic	500	10	917418

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Connectors					
J1		Socket 37-way			938678
		Mating plug, 37-way			916507
		Shell, junction			918105
		Retainer			914245
P1		Plug, 50-way PCB			A07881
Diodes					
CR1		Silicon IN916			913480
CR2		Silicon IN916			913480
CR3		Silicon IN916			913480
CR4		Silicon IN916			913480
CR5		Silicon IN916			913480
CR6		Silicon IN916			913480
CR7		Silicon IN916			913480
CR8		Silicon IN916			913480
Transistors					
Q1		NPN Silicon IN3904			914046
Q2		NPN Silicon IN3904			914046
Q3		NPN Silicon IN3904			914046
Q4		NPN Silicon IN3904			914046
Q5		NPN Silicon IN3904			914046
Q6		NPN Silicon IN3904			914046
Q7		NPN Silicon IN3904			914046
Q8		NPN Silicon IN3904			914046
Q9		NPN Silicon IN3904			914046
Integrated Circuits					
U1	10 k	Resistor Network, SIL			933750
U2	68 k	Resistor Network, DIL			938680
U3		Quad line receiver 26L532			938683
U4		Not used			
U5		Dual 2-input NAND buffer 40107			928188
U6		Dual 2-input NAND buffer 40107			928188
U7		Dual 2-input NAND buffer 40107			928188
U8		Dual 2-input NAND buffer 40107			928188
U9		Dual RS422 line driver 26LS30			938684
U10		Dual D-type flip-flop 4013			926860

DC POWER SUPPLY MODULE (ST 80762)

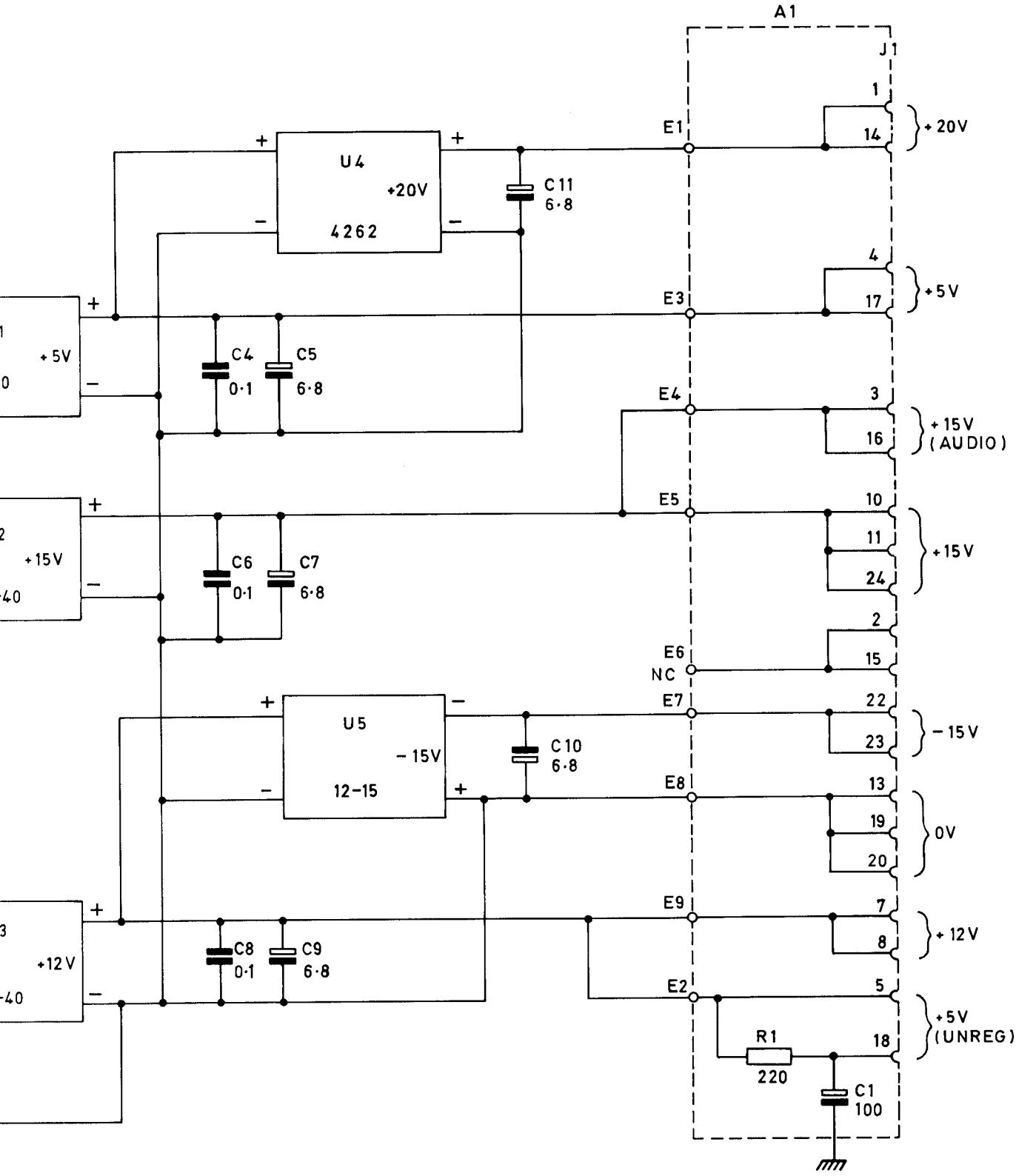
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			**Volts**		
A1C1	100	Electrolytic	25		935140
C1	0μ1	Disc Ceramic	100	20	938406
C2	0μ1	Disc Ceramic	100	20	938406
C3	0μ1	Disc Ceramic	100	20	938406
C4	0μ1	Disc Ceramic	100	20	938406
C5	6μ8	Tantalum	35	20	921179
C6	0μ1	Disc Ceramic	100	20	938406
C7	6μ8	Tantalum	35	20	921179
C8	0μ1	Disc Ceramic	100	20	938406
C9	6μ8	Tantalum	35	20	921179
C10	6μ8	Tantalum	35	20	921179
C11	6μ8	Tantalum	35	20	921179
Resistors					
A1R1	220	Metal Film		2	910390
Fuses					
FS1	5A	Fuselink, quick blow			937892
		Fuseholder			938647
Diodes					
CR1		Std mounting 100 V 20 A			937889
Connectors					
J1		Terminal, Red			937895
J2		Terminal, Black			937894
J3		Socket, 9-way			918090
A1 J1		Socket, 25-way			915970

Cct Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Converter Modules					
U1		+5 V, 3 A			938648
U2		+15 V, 1.5 A			938649
U3		+12 V, 2 A			938650
U4		+20 V			938652
U5		-15 V, 670 mA			938651
Miscellaneous					
A1		Connector Board			B08688

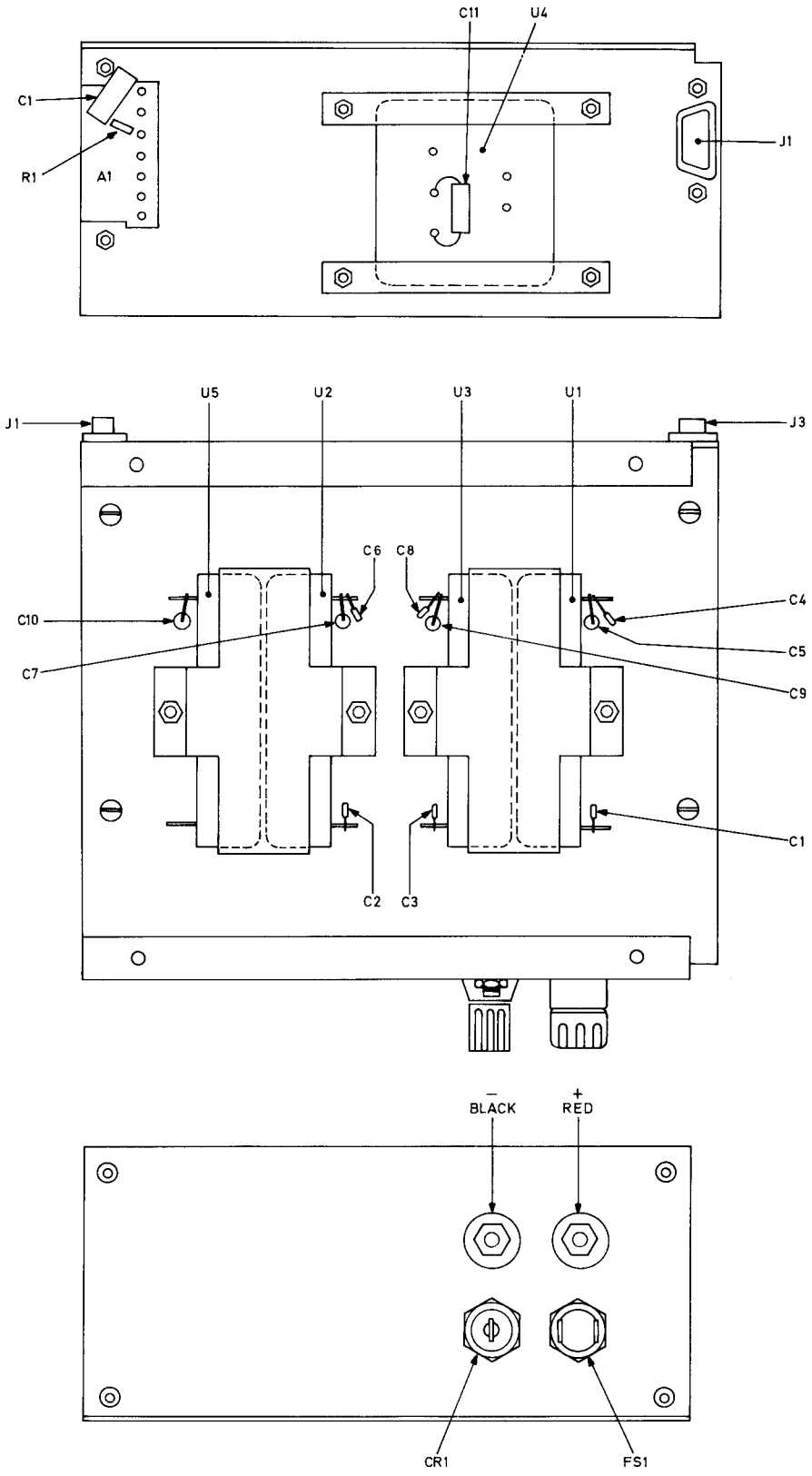


RACAL

TH 2185	DO 8300
1	



Circuit : DC/DC Power Supply Module A10 Fig. App.3



RACAL TH2185

Layout : DC/DC Power Supply Module A10 Fig. App. 3·2

FIRST LO SYNTHESIZER BOARD A7 (ST08545)

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Resistors					
R1	47k	Metal Oxide		2	913496
R2	10	Metal Oxide		2	920736
R3	10k	Metal Oxide		2	914042
R4	330	Metal Oxide		2	915690
R5	200	Variable	0.5	20	938618
R6	47	Metal Oxide		2	917063
R7	68	Metal Oxide		2	916476
R8	68	Metal Oxide		2	916476
R9	22	Metal Oxide		2	920743
R10	1.5k	Metal Oxide		2	911166
R11	680	Metal Oxide		2	910113
R12	10	Metal Oxide		2	920736
R13	390	Metal Oxide		2	916331
R14	120k	Metal Oxide		2	917062
R15	820	Metal Oxide		2	917065
R16	500	Variable		20	938426
R17	2.2k	Metal Oxide		2	916546
R18	47	Metal Oxide		2	917063
R19	1.0	Composition		5	938617
R20		Not used			
R21	82	Metal Oxide		2	917057
R22	22	Metal Oxide		2	920743
R23	220	Metal Oxide		2	910390
R24	470	Metal Oxide		2	920758
R25	1k	Metal Oxide		2	913489
R26	1.5k	Metal Oxide		2	911166
R27	330	Metal Oxide		2	915690
R28	10	Metal Oxide		2	920736
R29	100	Metal Oxide		2	910388
R30	820	Metal Oxide		2	917065

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R31	220	Metal Oxide		2	910390
R32	220	Metal Oxide		2	910390
R33	820	Metal Oxide		2	917065
R34	470	Metal Oxide		2	920758
R35	470	Metal Oxide		2	920758
R36	220	Metal Oxide		2	910390
R37	820	Metal Oxide		2	917065
R38	470	Metal Oxide		2	920758
R39		Not used			
R40	470	Metal Oxide		2	920758
R41	470	Metal Oxide		2	920758
R42	470	Metal Oxide		2	920758
R43	820	Metal Oxide		2	917065
R44	330	Metal Oxide		2	915690
R45	38k	Metal Oxide		2	900993
R46	470	Metal Oxide		2	920758
R47	820	Metal Oxide		2	917065
R48	470	Metal Oxide		2	920758
R49	470	Metal Oxide		2	920758
R50	10k	Metal Oxide		2	914042
R51	12k	Metal Oxide		2	917952
R52	2.7k	Metal Oxide		2	916548
R53	4.7k	Metal Oxide		2	913490
R54	4.7k	Metal Oxide		2	913490
R55	470	Metal Oxide		2	920758
R56	1.8k	Metal Oxide		2	911148
R57	3.3k	Metal Oxide		2	910111
R58	470	Metal Oxide		2	920758
R59	3.3k	Metal Oxide		2	910111
R60	22	Metal Oxide		2	920743
R61	1k	Metal Oxide		2	913489
R62	10k	Metal Oxide		2	914042
R63	1k	Metal Oxide		2	913489
R64	39k	Metal Oxide		2	900993
R65	15k	Metal Oxide		2	920645

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R66	8.2k	Metal Oxide		2	918202
R67	12k	Metal Oxide		2	917952
R68	1k	Metal Oxide		2	913489
R69	3.3k	Metal Oxide		2	910111
R70	1k	Metal Oxide		2	913489
R71	82	Metal Oxide		2	917057
R72	10	Metal Oxide		2	920736
R73	10k	Metal Oxide		2	914042
R74	15k	Metal Oxide		2	920645
R75	15k	Metal Oxide		2	920645
R76	15k	Metal Oxide		2	920645
R77	100k	Metal Oxide		2	915190
R78	2-7k	Metal Oxide		2	916548
R79	12k	Metal Oxide		2	917952
R80	150k	Metal Oxide		2	917594
R81	10k	Metal Oxide		2	914042
R82	10k	Metal Oxide		2	914042
R83	10k	Metal Oxide		2	914042
R84	3.3k	Metal Oxide		2	910111
R85	100	Metal Oxide		2	910388
R86	470	Metal Oxide		2	920758
R87	47k	Metal Oxide		2	913496
R88	120k	Metal Oxide		2	915373
R89	47k	Metal Oxide		2	913496
R90	1k	Metal Oxide		2	913489
R91	150	Metal Oxide		2	910389
R92	10	Metal Oxide		2	920736
R93	680	Metal Oxide		2	910113
R94	10	Metal Oxide		2	920736
R95	1k	Metal Oxide		2	913489
R96		Not used			
R97	1k	Metal Oxide		2	913489

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors			V		
C1	6.8	Tantalum	35	20	938030
C2	6.8	Tantalum	35	20	938030
C3	6.8	Tantalum	35	20	938030
C4	6.8	Tantalum	35	20	938030
C5	.01	Ceramic	50	20	938053
C6	6.8	Tantalum	35	20	938030
C7	.01	Ceramic	50	20	938053
C8	6.8	Tantalum	35	20	938030
C9	.01	Ceramic	50	20	938053
C10	10p	Ceramic	500	5	917746
C11	.01	Ceramic	50	20	938053
C12	6.8	Tantalum	35	20	938030
C13	.01	Ceramic	50	20	938053
C14	.01	Ceramic	50	20	938053
C15	.01	Ceramic	50	20	938053
C16	.01	Ceramic	50	20	938053
C17	.01	Ceramic	50	20	938053
C18	.01	Ceramic	50	20	938053
C19	.01	Ceramic	50	20	938053
C20	.01	Ceramic	50	20	938053
C21	.01	Ceramic	50	20	938053
C22	.01	Ceramic	50	20	938053
C23	.01	Ceramic	50	20	938053
C24	.01	Ceramic	50	20	938053
C25	.01	Ceramic	50	20	938053
C26	.01	Ceramic	50	20	938053
C27	.01	Ceramic	50	20	938053
C28	.01	Ceramic	50	20	938053
C29	.01	Ceramic	50	20	938053
C30	.01	Ceramic	50	20	938053
C31	.01	Ceramic	50	20	938053
C32	.01	Ceramic	50	20	938053
C33	.01	Ceramic	50	20	938053
C34	.01	Ceramic	50	20	938053
C35	0.1	Ceramic	50	20	938406

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C36	6.8	Tantalum	35	20	938030
C37	0.1	Ceramic	50	20	938406
C38	6.8	Tantalum	35	20	938030
C39	.01	Ceramic	50	20	938053
C40	.001	Ceramic	50	20	938408
C41	33	Tantalum	25	10	938606
C42	0.1	Ceramic	50	20	938406
C43	.001	Ceramic	50	20	938408
C44	.01	Ceramic	50	20	938053
C45	6.8	Tantalum	35	20	938030
C46	6.8	Tantalum	35	20	938030
C47	.01	Ceramic	50	20	938053
C48	.01	Ceramic	50	20	938053
C49	6.8	Tantalum	35	20	938030
C50	6.8	Tantalum	35	20	938030
C51	0.1	Ceramic	50	20	938406
C52	.001	Ceramic	50	20	938408
C53	150	Tantalum	6	20	938607
C54	.001	Ceramic	50	20	938408
C55	.01	Ceramic	50	20	938053
C56	33	Tantalum	25	10	938606
C57	6.8	Tantalum	35	20	938030
C58	10p	Ceramic	500	5	917746
C59	0.1	Ceramic	50	20	938406
C60	6.8	Tantalum	35	20	938030
C61	6.8	Tantalum	35	20	938030
C62	0.1	Ceramic	50	20	938406
C63	0.1	Ceramic	50	20	938406
C64	0.1	Ceramic	50	20	938406
C65	0.1	Ceramic	50	20	938406
C66	0.1	Ceramic	50	20	938406
C67	0.1	Ceramic	50	20	938406
C68	0.1	Ceramic	50	20	938406
C69	0.1	Ceramic	50	20	938406
C70	0.1	Ceramic	50	20	938406

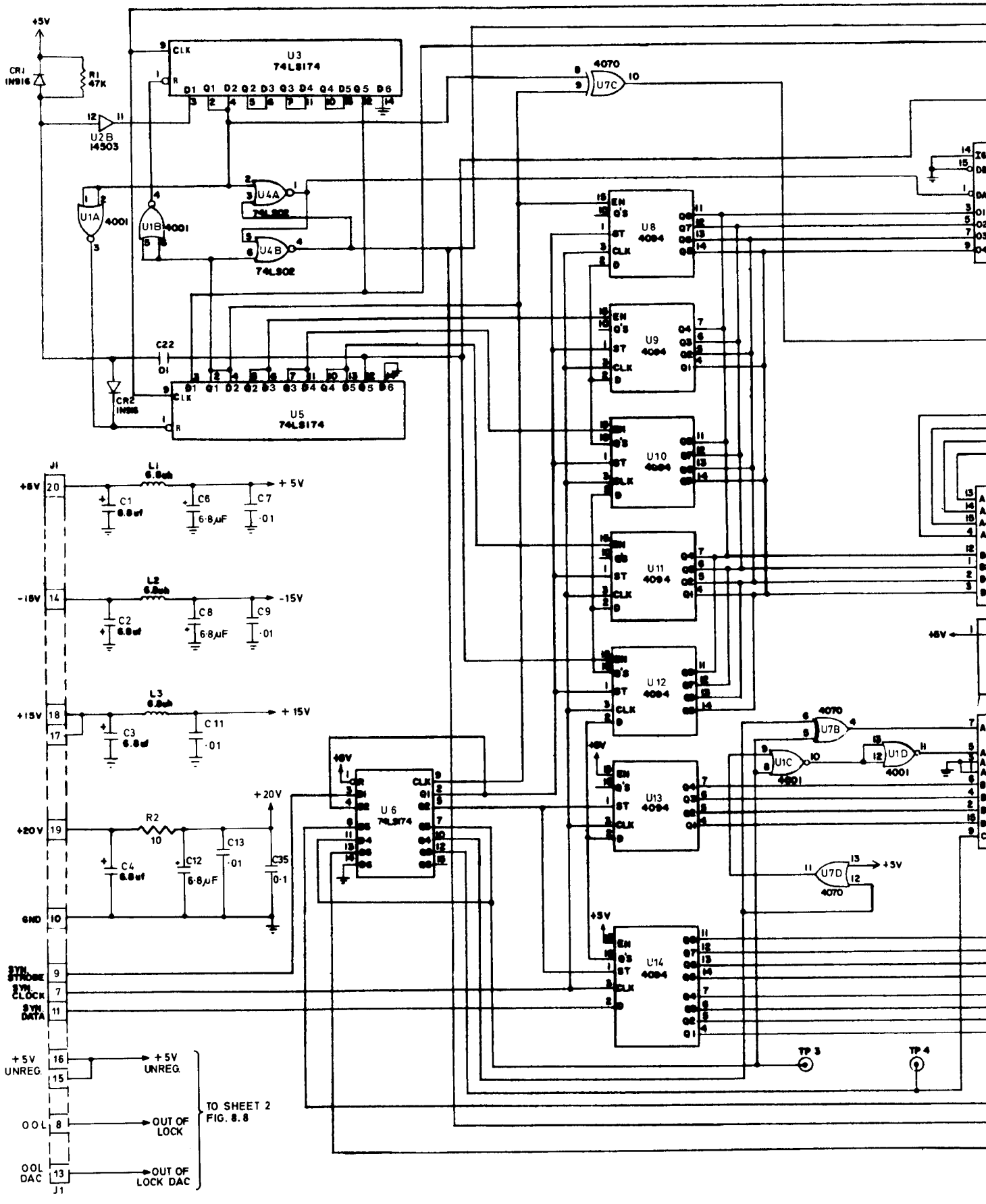
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C71	0.1	Ceramic	50	20	938406
C72	0.1	Ceramic	50	20	938406
C73	0.1	Ceramic	50	20	938406
C74	0.1	Ceramic	50	20	938406
C75	0.1	Ceramic	50	20	938406
C76	0.1	Ceramic	50	20	938406
C77	0.1	Ceramic	50	20	938406
C78	100p	Mica	350	5	938510
C79	6.8	Tantalum	35	20	938030
C80	27p	Mica	350	1p	902220
C81	.001	Polyester	400	10	938671
C82	.047	Polycarbonate	100	10	931129
C83	6.8	Tantalum	35	20	938030
C84	6.8	Tantalum	35	20	938030
C85	.01	Ceramic	50	20	938053
C86	1.0	Tantalum	35	10	938032
C87	1.0	Tantalum	35	10	938032
C88	15	Tantalum	20	20	910060
C89	.047	Ceramic	50	20	938511
C90	2200p	Ceramic	100	20	937903
C91	4700p	Mica	350	5	906253
C92	2200p	Mica	350	2	902197
C93	0.1	Ceramic	50	20	938406
C94	6.8	Tantalum	35	20	938030
C95	.001	Ceramic	50	20	938408
C96	0.1	Ceramic	50	20	938406
C97	1.0	Polycarbonate	100	20	923370
C98	3.3	Polycarbonate	63	10	938673
C99	.068	Polycarbonate	100	10	938672
C100	4.7p	Ceramic	100	0.5p	938794
C101	10p	Mica	500	0.5p	921270
C102	10p	Ceramic	500	5	917746
C103	47p	Mica	350	5	908617
C104	47p	Mica	350	5	908617

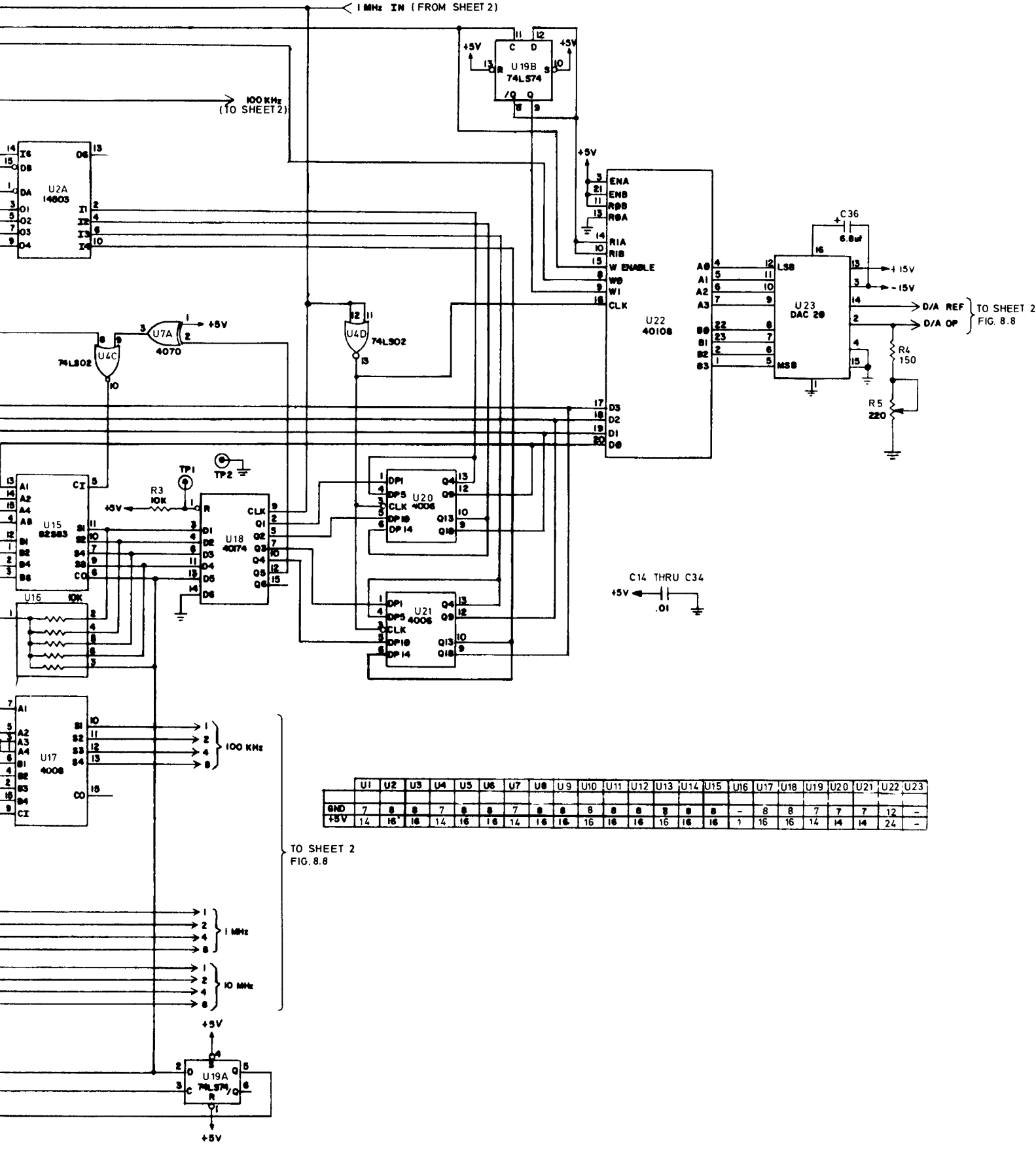
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Diodes					
CR1		IN 916			913480
CR2		IN 916			913480
CR3		Varactor KV 2201			938614
CR4		Varactor KV 2201			938614
CR5		IN 916			913480
CR6		IN 916			913480
CR7		IN 916			913480
CR8		IN 916			913480
CR9		IN 916			913480
CR10		IN 916			913480
CR11		IN 916			913480
CR12		IN 916			913480
CR13		IN 916			913480
CR14		IN 916			913480
CR15		IN 916			913480
CR16		IN 916			913480
CR17		Not used			
CR18		Zener 9.1V, 400mW, IN 757A			938674
CR19		IN 916			913480
CR20		IN 916			913480
CR21		IN916			913480
CR22		IN916			913480
Transistors					
Q1		FET 2N3823			938592
Q2		NPN RF 2N3866			917219
Q3		NPN RF 2N3866			917219
Q4		NPN Silicon 2N4921			938616
Q5		NPN Silicon 2N2369			906842
Q6		PNP Plastic 2N4126			912678
Q7		PNP Plastic 2N4126			912678
Q8		PNP Plastic 2N4126			912678
Q9		NPN Plastic 2N4124			915617
Q10		NPN Plastic 2N4124			915617
Q11		PNP Plastic 2N4126			912678
Q12		NPN Silicon 2N918			906517
Q13		NPN Silicon 2N2369			906842

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Integrated Circuits					
U1		4001			938561
U2		4503			935215
U3		94LS174			938624
U4		74LS02			938531
U5		74LS174			938624
U6		74LS174			938624
U7		* 4070			938837
U8		4094			934550
U9		4094			934550
U10		4094			934550
U11		4094			934550
U12		4094			934550
U13		4094			934550
U14		4094			934550
U15		82583			938622
U16		10k resistor network			938625
U17		4008			938620
U18		* 40174			938838
U19		74LS74			930602
U20		4006			938628
U21		4006			938628
U22		40108			938629
U23		DAC 20			938631
U24		UA 723			925040
U25		Not used			
U26		10231			938630
U27		11C90			938600
U28		10231			938630
U29		74LS169			938627
U30		74LS168			938626
U31		74LS168			938626
U32		10211			938633
U33		1458			938632
U34		LM339			929149
U35		AD518			938634

* Use RCA, Motorola or National only.

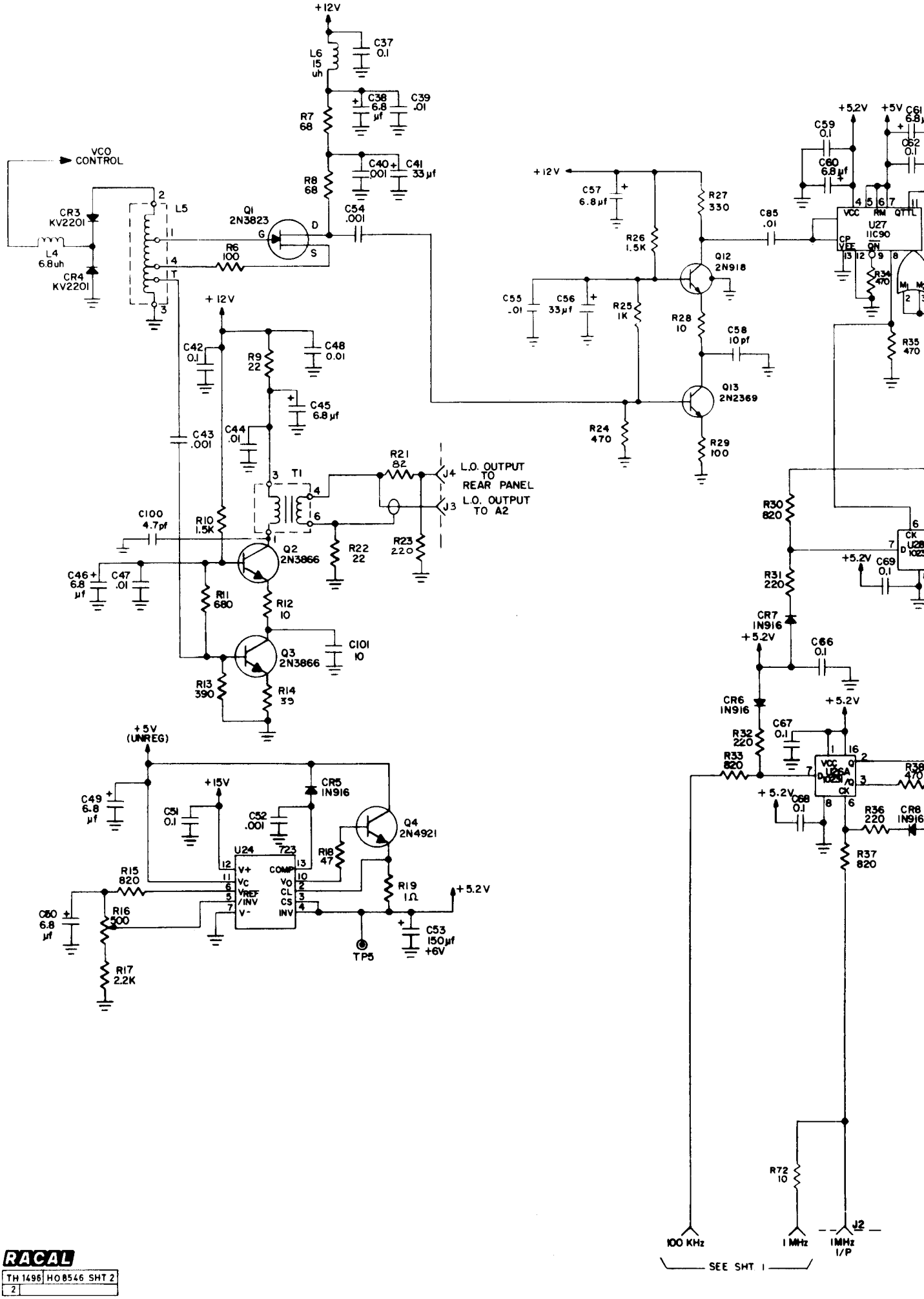
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
U36		DG 201			934880
U37		1458			938632
U38		Not used			
U39		7812			938445
U40		3140E			932204
Transformers					
T1		RF wideband			D06467/1
Inductors					
L1	6.8 µH	Choke			919469
L2	6.8µH	Choke			919469
L3	6.8µH	Choke			919469
L4	6.8µH	Choke			919469
L5		Coil Assembly			D08708
L6	15µH	Choke		10	915850
Connectors					
J1		Plug, 20-way			938675
J2		Plug, Coaxial 50 ohms			938429
J3		Plug, Coaxial 50 ohms			938429
J4		Plug, Coaxial 50 ohms			938429


+5V
CR1 IN916
R1 47K
U3 74LS174
U2B 14503
U4A
U4B
74LS02
U1A 4001
U1B 4001
C22 01
CR2 IN916
U5 74LS174
4070
U7C
U8 4094
U9 4094
U10 4094
U11 4094
U12 4094
U13 4094
U14 4094
U6 74LS174
J1
+5V 20
L1 6.8uh
C1 6.8uf
C6 6.8µF
C7 .01
+5V
-15V 14
L2 6.8uh
C2 6.8uf
C8 6.8µF
C9 .01
-15V
+15V 18
17
L3 6.8uh
C3 6.8uf
C11 .01
+15V
+20V 19
R2 10
C4 6.8uf
C12 6.8µF
C13 .01
C35 0.1
+20V
GND 10
SYN STROBE 9
SYN CLOCK 7
SYN DATA 11
+5V UNREG. 16
15
OOL 8
OOL DAC 13
+5V UNREG.
OUT OF LOCK
OUT OF LOCK DAC
TO SHEET 2 FIG. 8.8
U7B
U1C
U1D
4001
U7D
TP 3
TP 4



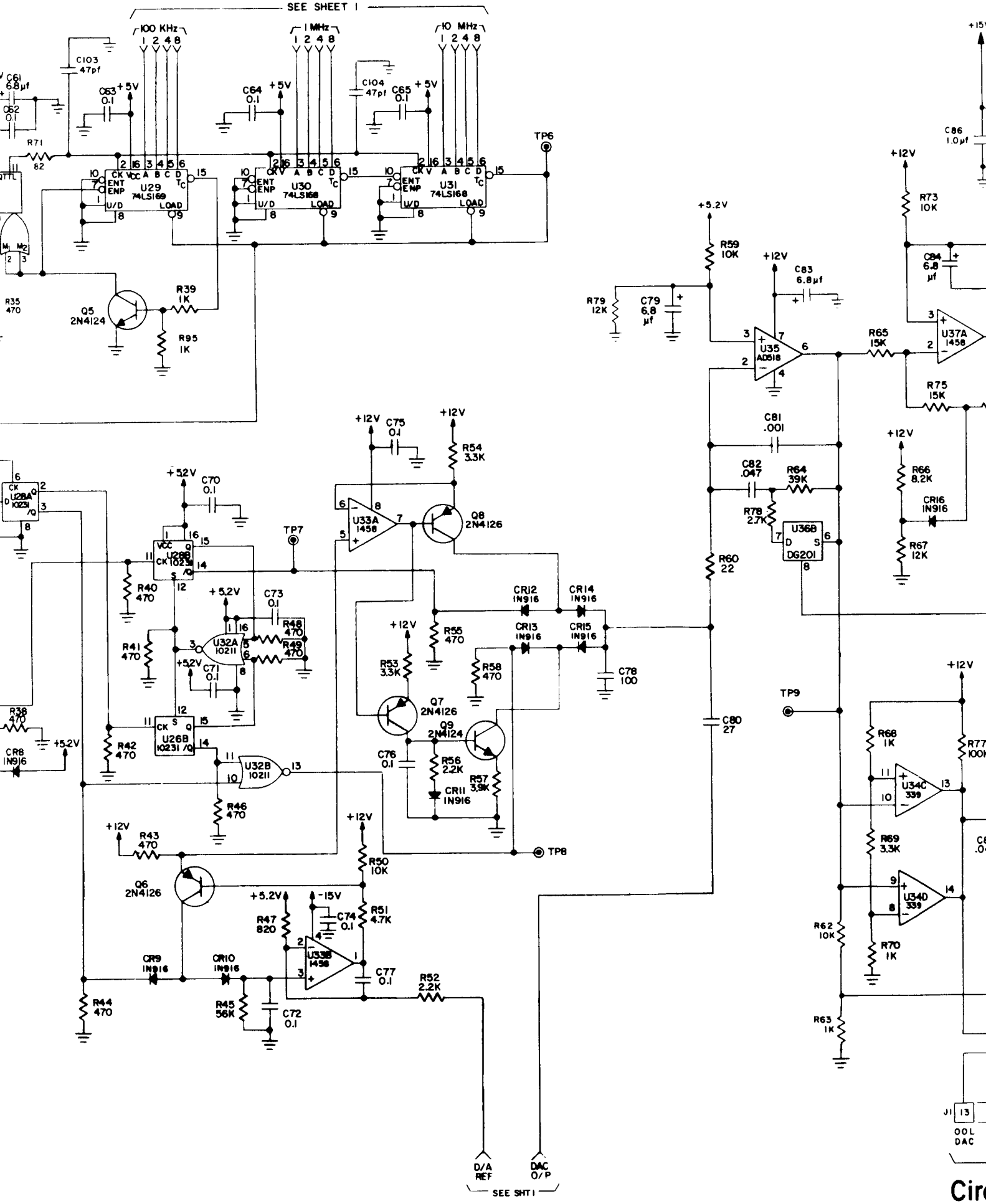
	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20	U21	U22	U23
GND	7	8	8	7	8	8	7	8	8	8	8	8	8	8	8	-	8	8	7	7	7	12	-
+5V	14	16	16	14	16	16	14	16	16	16	16	16	16	16	16	1	16	16	14	14	14	24	-

Circuit: First LO Synthesizer Module A7 (Sheet 1) Fig. App. 4.1

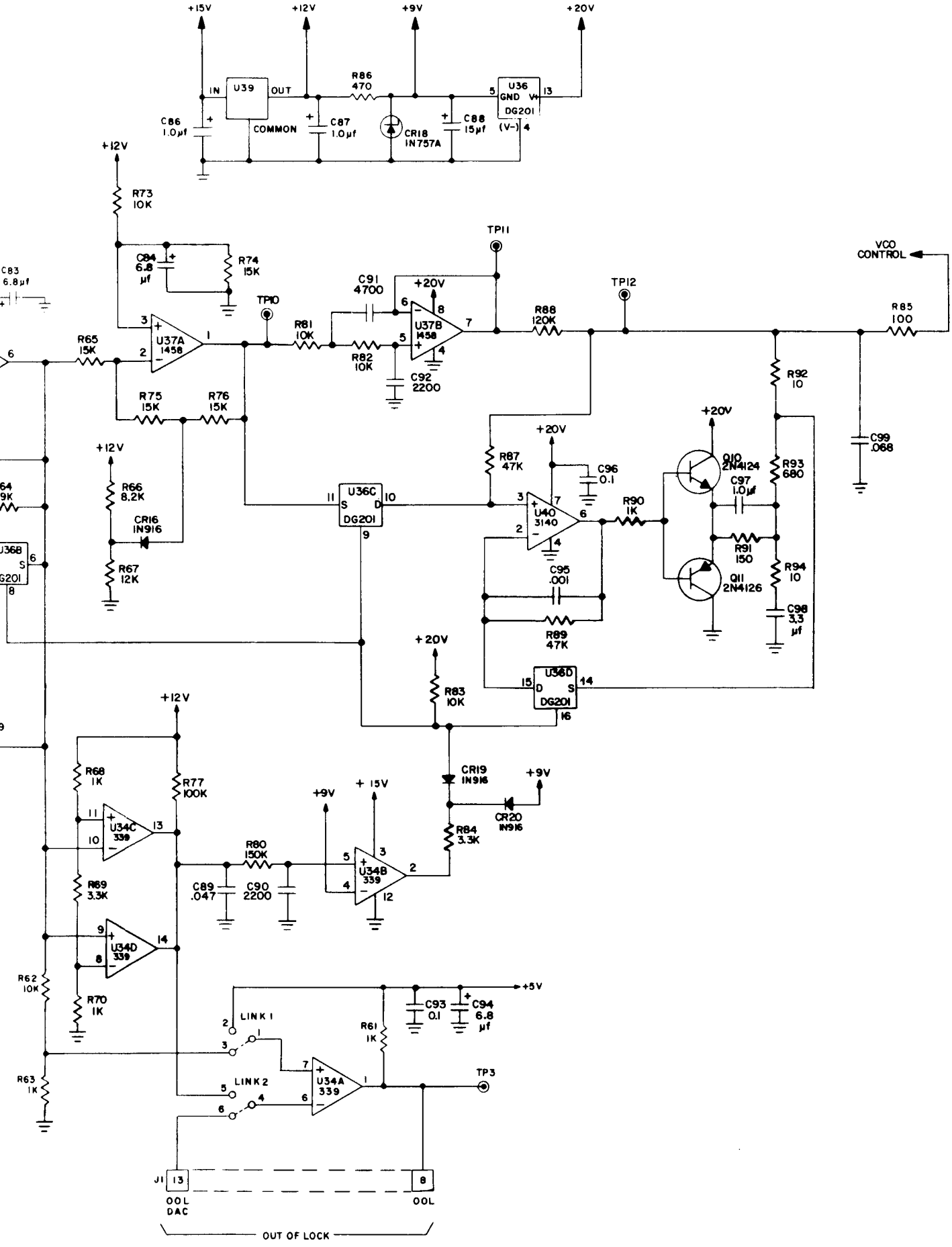


RACAL

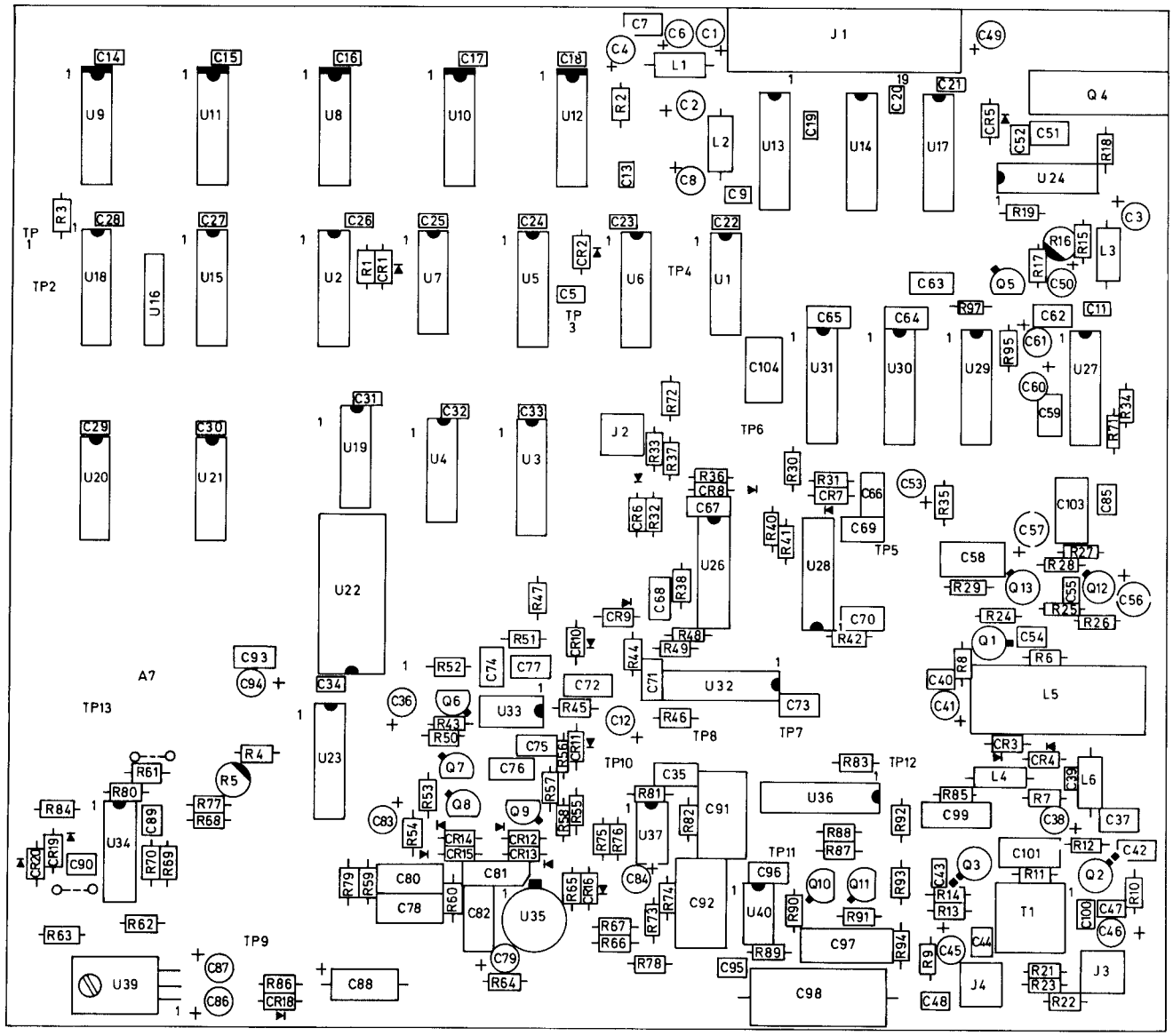
TH 1496	HO 8546 SHT 2
2	


SEE SHEET 1
100 KHz
1 MHz
10 MHz
U29 74LS169
U30 74LS168
U31 74LS168
TP6
TP7
TP8
TP9
Q5 2N4124
Q6 2N4126
Q7 2N4126
Q8 2N4126
Q9 2N4124
U33A 1458
U33B 1458
U35 AD518
U36B DG201
U37A 1458
U34C 339
U34D 339
U32A 10211
U32B 10211
U26B 10231
U28A 10231
U28B 10231
D/A REF
DAC O/P
SEE SHT 1
J1
OOL DAC

Cir



Circuit : First LO Synthesizer Module A7 (Sheet 2) Fig. App. 4.2



Component Layout: First
LO Synthesizer Board A7

Fig. App. 4.3

RACAL
TH1496 | EO8545
2