Ten-Tec Orion Synthesizer - Design Summary

Abstract

Design details of the low phase noise, synthesized, 1st local oscillator of the
Ten-Tec model 565 Orion transceiver are presented. History, design
philosophy, and performance tradeoffs are discussed. Circuit descriptions,
block and schematic diagrams, and phase noise plots are included, along
with some basic programming information.

Introduction

Over three decades ago, local oscillator (LO) generation by the Phase Locked Loop (PLL) method of indirect
frequency synthesis replaced the practice of mixing multiple banks of quartz crystals (direct synthesis) in
channelized radios such as CB, aircraft communications, and police/utility scanners. Eventually, fine tuning
PLLs migrated into the continuously-tuned radio services such as amateur and commercial single-sideband HF
operations. When compared to the typical temperature-compensated, permeability-tuned L-C oscillators
(PTOs) in use at the time for continuous tuning, these early PLL designs -- plagued by noisy VCOs, slow
programmable dividers and phase detectors, and the resulting limited loop bandwidths -- produced poor phase
noise performance. Lacking modern high-speed CMOS integration, these PLL synthesizers were often
complex, multiple-loop, multiple-board constructs.

Poor phase noise not withstanding, the early PLLs did offer a few advantages. Excellent frequency stability
without temperature compensation, broadband "general coverage" tuning, and remote computer controllability
were enough to ensure that PLLs would soon replace LC oscillators in nearly all commercial radios. Ten-Tec
jumped on the bandwagon too with the synthesized Paragon model.

When the Paragon was introduced, however, we were well aware of the phase noise limitation, so we kept the
permeability-tuned, crystal-mixed Omni transceivers in the line for serious contest-oriented operation in the HF
amateur bands. Eventually, a PLL based replacement for the permeability-tuned-oscillator (PTO) was
developed for the Omni line. This PTO replacement overcame the phase noise limitation of the PLL by
incorporating some of the same design techniques later used in the modern Orion synthesizer design to be
presented here.

To reduce the phase noise in the Omni PLL, the main VCO operated at VHF and, using the then newly
available low-cost ECL technology, divided down to the 5-5.5 MHz LO mixer injection frequency. To keep the
phase comparison frequencies high, a two loop / mixing loop architecture was chosen, along with a D/A
converter driven VCXO (quasi-direct synthesis) for the fine tuning loop. The Omni transceiver remains, to this
day, one of the lowest phase noise HF transceivers ever manufactured. Some of this architecture will be
recognized in the new Orion synthesizer described below.

Design Philosophy[1]

The main design goals for the Orion synthesizer were 1) phase noise performance at least equal to the Omni, 2)
elimination of the Omni's expensive crystal mixing scheme, and 3) 1 Hz tuning resolution. Elimination of the
crystal mixing would also eliminate some hard-to-filter spurious components from the first LO.

With no crystal mixing to help it out, the Orion synthesizer must cover the range of 10.8 to 39 MHz in 1 Hz
steps, and with phase noise better than 130 dBc/Hz[2] at all frequency offsets greater than 2 kHz. By application
of the philosophy and design techniques described below, the final Orion synthesizer met these goals and,
additionally, maintained (or exceeded) the 130 dB/Hz close-in phase noise performance all the way down to
200 Hz ! We believe this to be a world-best for close-in (less than 2 kHz) phase noise in a commercial
transceiver.

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[1] Reference to block diagram Fig. 1, and phase plots Fig. 2 may help the reader follow this discussion.

[2] Although not mathematically rigorous, I am dropping the minus sign on phase noise, normally -130 dBc/Hz, to enhance readability.

The Orion synthesizer main VCO outputs a half-octave band of frequencies at UHF. This output is then divided down to the first LO injection frequency by a high-speed programmable divider chain. The divider reduces the typical 110 dBc/Hz @ 50 kHz phase noise of this wideband VCO by 26 to 36 dB, depending on its programmed divide ratio. The practical noise floor of the divider chain output is about 140 dBc/Hz; well below the design goal of 130 dBc/Hz. At frequency offsets less than 50 kHz, it is the responsibility of the PLL system to maintain the phase noise below 110 dBc/Hz at the VCO output (better than 136 dBc/Hz at the divider output). Since the high-speed divider is limited to only four ratios (modulo 20,30,40 or 60) the PLL system must also provide the 20, 30, 40 or 60 Hz VCO fine tuning steps to produce the required 1 Hz LO tuning resolution.

A 300 MHz DDS (direct synthesis) chip was chosen to provide the fine tuning for the loop. This is much preferred over the more traditional PLL technique of dividing the VCO down to a very low comparison frequency to achieve small tuning steps. The worst-case level of discrete spurious at the output of this DDS is only down about 80 dBc over a limited tuning range[3], so care should be taken not to multiply these spurs up to objectionable levels inside the PLL loop bandwidth. With no loop multiplication, these spurious will be improved at the divider output by 26 to 36 dB, just like the random VCO phase noise. The resulting discrete spurs will be down 106 dBc worst case, that's about 30 dB above the 1 Hz phase noise, or equal to the phase noise floor in a 1 kHz detection bandwidth. This spur level is much lower than could be achieved with the Omni crystal mixing scheme, and is considered more than adequate for a 100 dB dynamic range radio. The main point to be taken here is that there should be no frequency division of the VCO output before it is phase-compared to the DDS. To do so would multiply the discrete DDS spurious to such a level that they would begin to reduce the dynamic range performance of the receiver.

Another important noise source to consider is the phase noise produced by the phase comparator. At the phase comparison frequencies of the Orion's main (upper) loop, worst case phase noise of the discrete fast CMOS phase detector was measured to be 145 dBc/Hz. This is far below the 110 dBc/Hz minimum VCO noise inside the loop bandwidth and, since we have decided there will be no multiplication by the loop, it is therefore negligible. The story is different, however, for the coarse (lower) loop to be discussed below.

Acceptable DDS spurious performance is only achievable when the DDS output frequency is below about 10 MHz[3]. This fact limits the useable tuning range of the DDS, and helps establish the approximate phase comparison frequencies. The Orion incorporated an existing design for its sub-receiver that required a reference frequency of 7.425 MHz. Since the main synthesizer board supplies all reference frequencies for the radio, it was convenient to use this 7.425 MHz frequency to establish the DDS tuning range. Now, since we allowed no dividers in the main loop, it is obvious that we must mix the main VCO output down to a band of frequencies below 10 MHz that spans a 7.425 MHz range. This is accomplished with a UHF quadrature mixer and a coarse (lower) loop that moves in 7.425 MHz steps. The VCO of this coarse loop operates at an offset frequency of 2 to 9.425 MHz above the main loop VCO. The 2 to 9.425 MHz offset becomes the main loop phase comparison frequency and also the required output frequency of the DDS.

So why a quadrature mixer? Simply because the mixer output frequency is so low compared to the tuning range of the main VCO that, within this tuning range, two different VCO offsets can exist that produce the desired comparison frequency -- upper or lower sideband mix. Only one of these sidebands produces negative feedback and a stable loop. The quadrature arrangement is necessary so that a phase comparison can be made between the quadrature components to detect the undesired sideband, and then steer the main loop to the desired (stable) offset frequency. A simple dual flip-flop and op-amp circuit can perform this sideband detect / presteer function.

The main (upper) and coarse (lower) loops have nearly identical VCOs and loop bandwidths, so their noise contributions to the main loop phase comparison would be identical -- except for one thing. Although we allowed no multiplication in the main loop because of the spur content of the DDS, some multiplication in the coarse loop is absolutely necessary to generate the 7.425 MHz coarse steps of the UHF VCO from the 7.425 MHz reference frequency. The necessary range of multiplier is 74 to 106, or about 37 to 40 dB. Luckily, the fixed 7.425 MHz reference can be derived from a divided-down TCXO, and we have no concern about spurious content or phase noise from that arrangement. But this brings up the issue of phase detector noise again. The coarse loop phase detector is identical to the one in the main loop and, at 7.425 MHz comparison frequency, its phase noise was measured at 150 dBc/Hz. This noise gets multiplied by 40 dB, worst case, and ends up at 110 dBc/Hz into the quadrature mixer. That's just enough noise to begin making a small, and quite acceptable, contribution to the synthesizer output phase noise. Factoring this contribution in, the worst case phase noise is about 133 dBc/Hz at the synthesizer output, or about the same as a typical Omni or Paragon at 50 kHz offset.

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[3] AD9852 Data Sheet, Analog Devices, Inc

So this design approach can match the Omni for low phase noise at 50 kHz offset and above, but the real beauty of this Orion design is how it performs close-in. Refer to the phase noise plots in Fig.2. With decreasing frequency offset, the Omni phase noise slowly increases to about 130 dBc/Hz[4] at 2kHz and then increases about 6dB per octave below that, passing through 100 dBc/Hz at 200 Hz, and continuing on up with about the same slope below that. Over the same range, the measured phase noise of this Orion synthesizer remains nearly flat, or even decreases slightly down to 2 kHz, and then barely climbs back to 133 dBc/Hz at 500 Hz, and is still about 129 dBc/Hz at 100 Hz offset! This amazing result is achieved because of the extremely high loop gain resulting from the fact that there is no loop divider at all in the main loop, and because the high phase comparison frequency allows a very wide loop bandwidth.

Circuit Descriptions

Refer to block diagram Fig.1 and schematic diagram Fig. 3. The 1st LO Synthesizer board provides four output signals to the rest of the transceiver: Master frequency oscillator Y1 (TCXO) and reference divider U17/18/24 develop fixed reference frequencies of 44.55 MHz and 7.425 MHz at connectors J4, J5, and J6 for use by the main receiver 2nd LO PLL and by the sub receiver 2nd LO and 1st LO PLLs. Connector J3 provides the variable 10.8 to 38.7 MHz 1st LO output for the main transceiver.

The 1st LO synthesizer is a DDS-driven two-loop architecture. The upper, or mixing loop comprises Phase Detector/Charge Pump A, VCO/Buffer A, and Quadrature Mixer sections. This loop locks to a 2–9.425 MHz reference signal developed by the DDS U7. The DDS is controlled by the CPU via J2 to provide frequency steps of 20, 30, 40, or 60 Hz to Phase Detector A, resulting in 1 Hz steps at J3 after output division. The output from VCO A at R58 drives the Output Divider/Filter at U15 pin 1. Dividers U15, U16, and U30, controlled by Band 0 and Band 1 lines on connector J7, provide a total output frequency division of 20, 30, 40, or 60. The high frequency knee of the output filter is also controlled by the Band 0 line to reduce harmonic content of the output signal. The buffered output of VCO A at Q8 is presented to the RF ports of the Quadrature Mixer at U13/U21 pins 1.

The lower, or coarse loop comprises ÷N/Phase Detector/Charge Pump B, and VCO/Buffer B sections. This loop is locked to a fixed 7.425 MHz reference from U24 in the reference divider section. The N divider in U28, controlled by the CPU at connector J7, moves VCO B in 7.425 MHz steps. The buffered output of VCO B is presented in approximate quadrature to the LO ports of U13/U21 pins 3.

In the Quadrature Mixer section, the mixer outputs at U13/U21 pins 6 are lowpass filtered, buffered, and applied to phase detector U19. The U19 circuit outputs a logic high at TP7 when the frequency of VCO B is higher than the frequency of VCO A. This is the normal state of operation and comparator U20A and clamp transistor Q13 are off. During certain transient conditions, such as power-up or for large negative frequency steps when the VCO A frequency is temporarily above the VCO B frequency, a logic low from U19 turns Q13 on, ramping the VCO A control voltage low toward the correct offset.

To further aid mixing loop acquisition, U14 and U20B form a window comparator to presteer the VCO A control voltage to within a range of 90% to 110% of the VCO B control voltage. Pulse detector circuit U9D/Q26 keeps the OOL line at TP12 low for normal operation of the window comparator. If lock pulses are not present at U9D, the frequency separation of the VCOs may be too great to develop a mixer output within the passband of the lowpass filters (L17/18, L24/25). In this case, Q26 is turned off allowing the OOL line at TP12 to float, temporarily forcing VCO A control voltage equal to that of VCO B.

Zener diode D20 helps compensate for reduced VCO tuning sensitivity at the higher control voltages by increasing both charge pump currents via the BWC (bandwidth control) line.

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[4] Remember the missing minus sign makes 130 dB/Hz a worse phase noise than 133 dB/Hz. "Bigger is better."
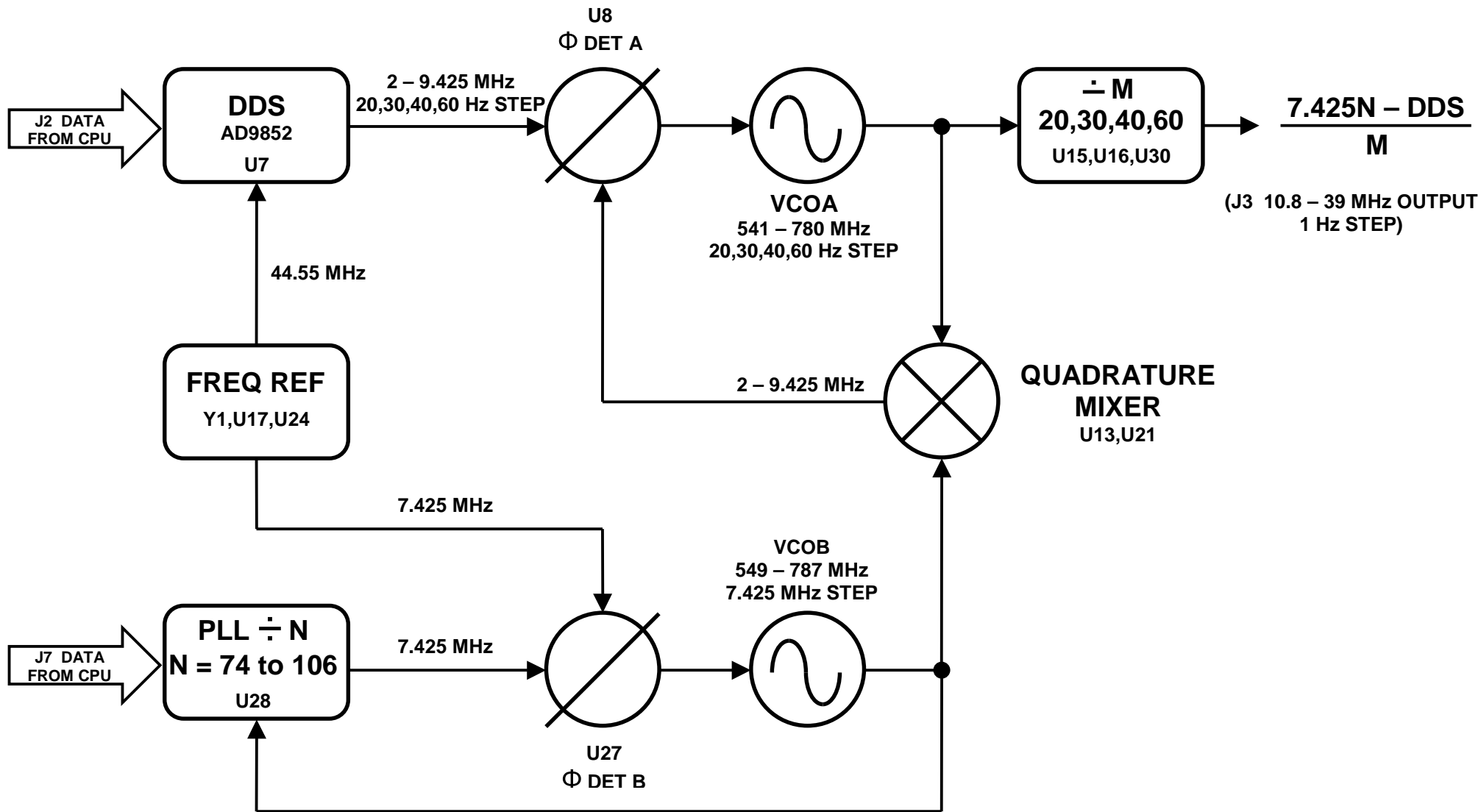
U8
Φ DET A

DDS
AD9852
U7

J2 DATA FROM CPU

2 – 9.425 MHz
20,30,40,60 Hz STEP

44.55 MHz

VCOA
541 – 780 MHz
20,30,40,60 Hz STEP

÷ M
20,30,40,60
U15,U16,U30

$$\frac{7.425N - DDS}{M}$$

(J3 10.8 – 39 MHz OUTPUT
1 Hz STEP)

FREQ REF
Y1,U17,U24

QUADRATURE
MIXER
U13,U21

2 – 9.425 MHz

7.425 MHz

VCOB
549 – 787 MHz
7.425 MHz STEP

PLL ÷ N
N = 74 to 106
U28

J7 DATA FROM CPU

7.425 MHz

U27
Φ DET B

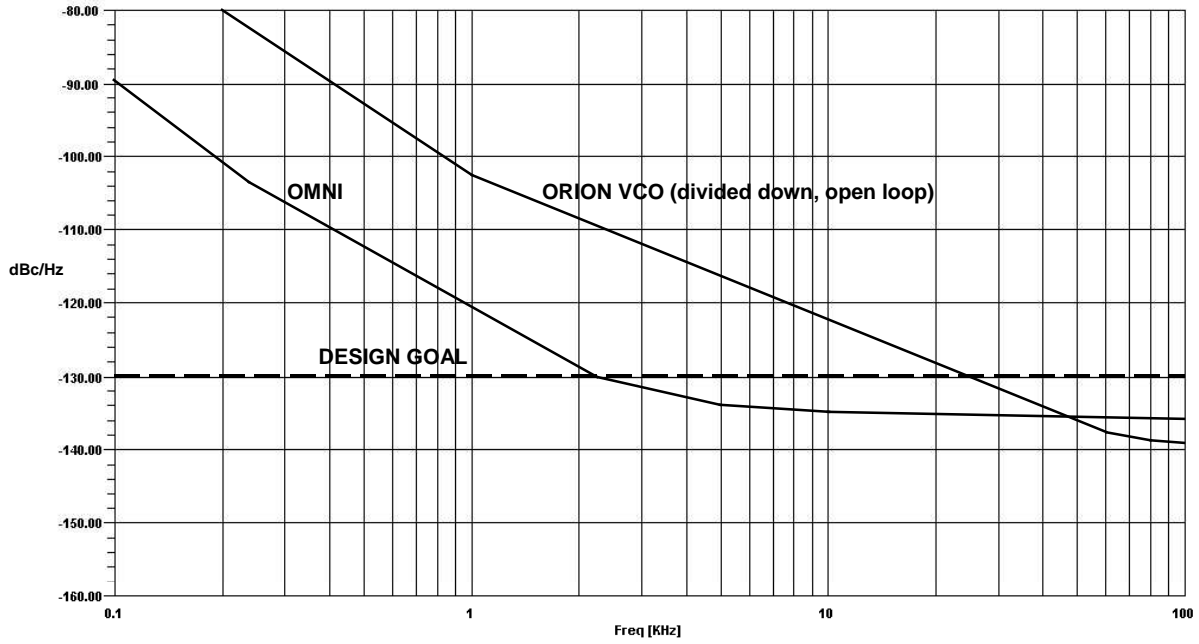**FIGURE 1 - ORION SYNTHESIZER BLOCK DIAGRAM**

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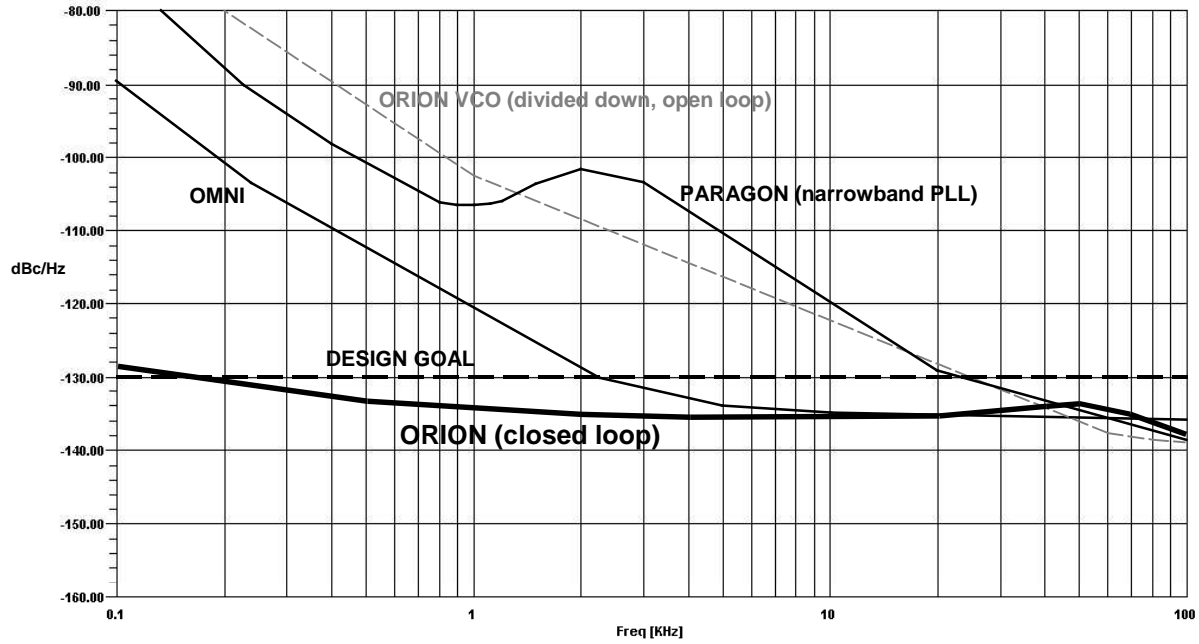**FIGURE 2a – ORION OPEN LOOP VCO (divided) vs OMNI PHASE NOISE**

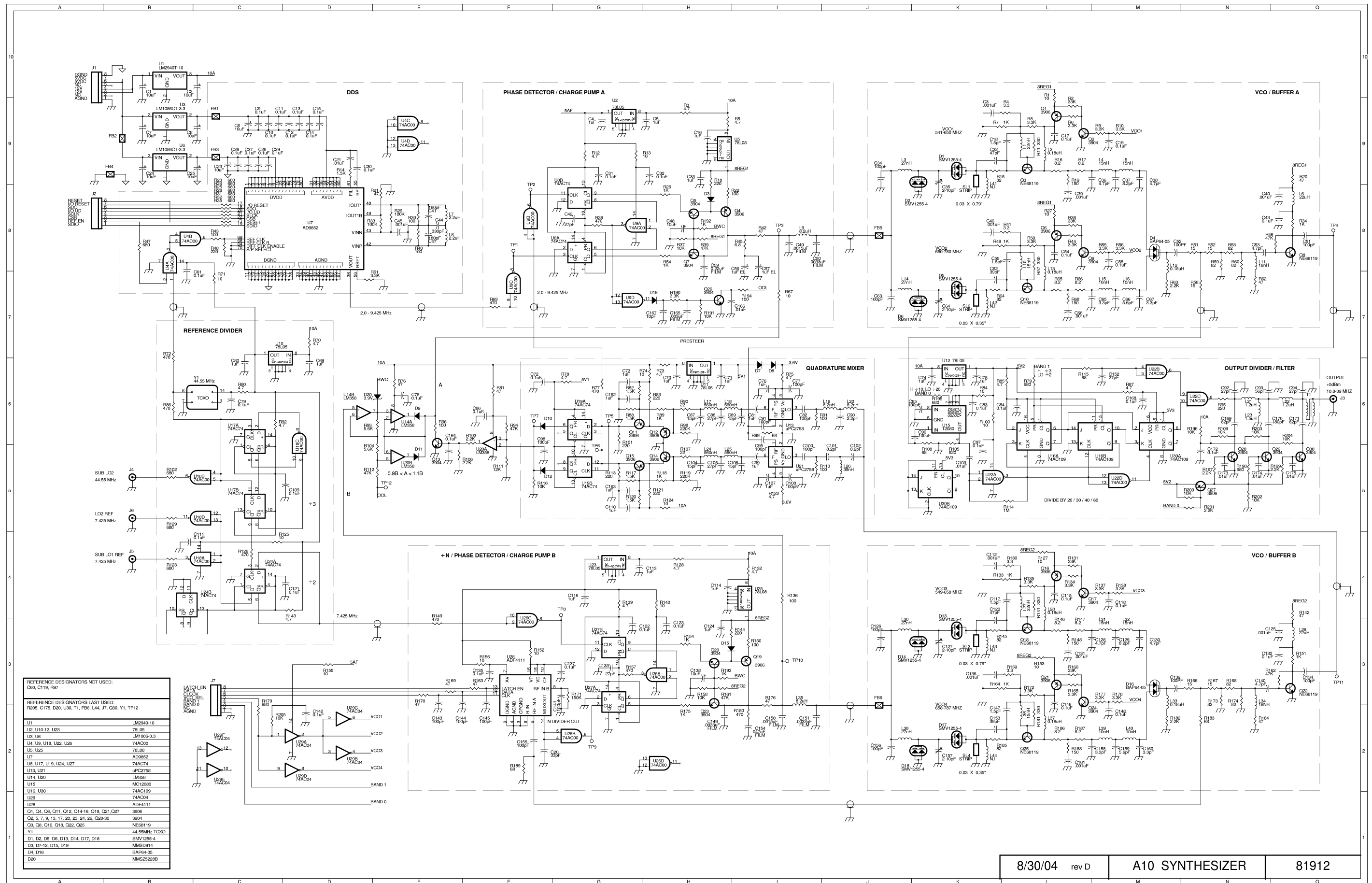**FIGURE 2b – ORION PHASE NOISE vs OMNI and PARAGON**

FIGURE 3 – ORION SYNTHESIZER SCHEMATIC DIAGRAM

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Programming

SYNTHESIZER OUTPUT FREQUENCY = [(7.425 N) – DDS] / M   (MHz)

N ranges 74 – 106. The 8/9 prescaler in U28 generates N from A and B: N = 8B + A

M = 20, 30, 40, or 60

M is determined by BAND 0 and BAND 1 bits as follows:

B0	B1	M
1	0	20
1	1	30
0	0	40
0	1	60

Settings for each amateur band:

BAND	OPERATING FREQUENCY	SYNTHESIZER FREQUENCY	B0	B1	M	VCO SEL	N	DDS	8/9 PRESCLR B	A
160	1.8 - 2.0	10.8 - 11.0	0	1	60	1	88 - 90	2.0 - 9.425	11	0-2
80	3.5 - 4.0	12.5 - 13.0	0	1	60	0	102 - 106	2.0 - 9.425	12/13	6-7/0-2
60	5.25 - 5.4	14.25 - 14.4	0	0	40	1	78	3.15 - 9.15	9	6
40	7.0 - 7.3	16.0 - 16.3	0	0	40	1	87 - 89	2.0 - 9.425	10/11	7/0-1
30	10.1 - 10.15	19.1 - 19.15	0	0	40	0	104	6.2 - 8.2	13	0
20	14.0 - 14.35	23.0 - 23.35	1	1	30	0	94 - 95	2.0 - 9.425	11	6-7
17	18.068 - 18.168	27.068 - 27.168	1	0	20	1	74	6.09 - 8.09	9	2
15	21.0 - 21.45	30.0 - 30.45	1	0	20	1	82 - 83	2.0 - 9.425	10	2-3
12	24.89 - 24.99	33.89 - 33.99	1	0	20	0	92	3.3 - 5.3	11	4
10	28 - 29.7	37.0 - 38.7	1	0	20	0	100 - 105	2.0 - 9.425	12/13	4-7/0-1

General coverage PLL tuning can be obtained by extending the range of N down to 71. The amateur band bandpass filters in the Orion prevent full utilization of this feature. Some MARS frequencies that are close to amateur band edges may be accommodated.

OPERATING FREQUENCY	SYNTHESIZER FREQUENCY	B0	B1	M	VCO SEL	N	8/9 PRESCALER B	A
0 - 2.1	9.0 - 11.1	0	1	60	1	73 - 90	9/10/11	1-7 / 0-7 / 0-2
2.1 - 4.08	11.1 - 13.08	0	1	60	0	91 - 106	11/12/13	3-7 / 0-7 / 0-2
4.08 - 7.65	13.08 - 16.65	0	0	40	1	71 - 90	8/9/10/11	7 / 0-7 / 0-7 / 0-2
7.65 - 10.6	16.65 - 19.6	0	0	40	0	91 - 106	11/12/13	3-7 / 0-7 / 0-2
10.6 - 13.2	19.6 - 22.2	1	1	30	1	80 - 90	10/11	0-7 / 0-2
13.2 - 17.1	22.2 - 26.1	1	1	30	0	91 - 106	11/12/13	3-7 / 0-7 / 0-2
17.1 - 24.3125	26.1 - 33.3125	1	0	20	1	71 - 90	8/9/10/11	7 / 0-7 / 0-7 / 0-2
24.3125 - 30.0	33.3125 - 39.0	1	0	20	0	91 - 106	11/12/13	3-7 / 0-7 / 0-2