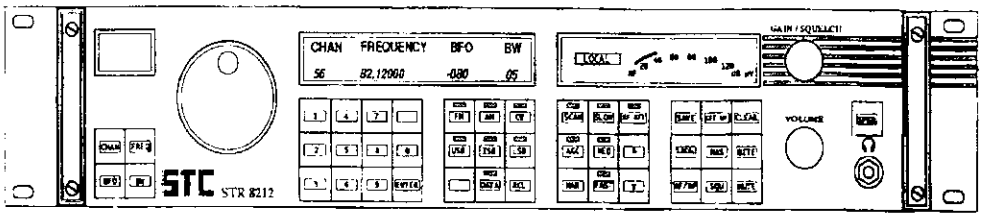
HF RECEIVER
STR 8212



TECHNICAL HANDBOOK

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STR8212 HF Receiver

Technical Handbook

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PRODUCT SAFETY INFORMATION SHEET

STR 8212 HF Receiver

This should be read in conjunction with the Product Data Sheets STR 8212
Failure to observe the ratings and the information on this sheet may result in a safety hazard.

1. MATERIAL CONTENT

The unit contains printed circuit board semiconductor assemblies with heatsinks. The heatsinks contain a substance which is mildly toxic if swallowed. The liquid crystal display contains a liquid mixture of cyanobiphenyl and cyanoterphenyl, not normally accessible but which is an irritant to eyes, skin and mouth. Materials contained within the unit include PTFE, Nylon, PVC, PBT, Perspex, Tessamol, Beryllium Copper (2% Be).

2. PHYSICAL FORM

The STR8212 HF receiver is housed in a vented steel enclosure suitable for mounting into a 19 inch rack system . Unit cooling is fan assisted and a 1 U space should be allowed below the unit for adequate air circulation. Enclosure dimensions are 482.6 mm X 89 mm X 512 mm. Total weight of the STR8212 is 15 Kg (approx).

3. INTRINSIC PROPERTIES

NON-OPERATING

Safe, when isolated from primary power source.

OPERATING

Removing covers during operation presents an electric shock hazard. Hazard warning labels are affixed to the outside of the unit.

4. FIRE CHARACTERISTICS

PRIMARY

Overload conditions could present a fire hazard. Some materials used in small quantities within the construction have limiting oxygen values of 16.8. A thermal cutout device is attached to the mains transformer. The case is vented to minimise heat and gas concentration .

There is an increased risk of fire if the unit is operated without the top cover fitted.

SECONDARY

When exposed to fire the external finishing paint plus some of the external components, display windows, key caps may burn. Excessive overload / heating of materials will cause emission of toxic gases.

5. HANDLING

The normal procedures for handling electronic equipment should be observed. The unit weighs 15 kg approximately. Handles on the unit are not for transportation. The front and rear handles aid removal of the unit from rack assemblies and give panel and connector protection . Units mounted into a 19 inch rack shall have secure fixings.

6. STORAGE

Normal care for the storage of electronic equipment should be observed . Units should not be stored in conditions exceeding the temperature range -40 to +70 degrees C.

7. DISPOSAL

Disposal of the unit should be in accordance with the toxic waste disposal procedure, current at the time of disposal. Units must not be incinerated due to the presence of materials such as PTFE which would emit toxic fumes.

8. UNSAFE USE

Electric shock hazard is present if panels are removed during operation. Fire hazard could exist during overload conditions. Replacement fuses should be of the correct rating to minimise overload conditions. Ensure that the mains voltage selector at the mains inlet to the equipment is correctly set before applying power. Toxic fume hazard possible if unit is overheated from internal or external source. Mechanical hazard can occur if the unit is mishandled or incorrectly secured. Under damage conditions do not use. The radio must not be operated unattended with the top cover removed, since operation of internal air cooling is impaired increasing the risk of fire under fault conditions. Internal modules may also present a heat hazard due to the impaired air cooling. Servicing only to be undertaken by qualified personnel. The unit must be earthed.

PS 8212/1 Issue 2 November 1991

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northern telecom

RX: STR 8212: c99-10:

IMPLEMENTATION OF T/R SWITCHING FOR AMATEUR USE

(a) CIRCUITRY / COMPONENT VALUES:

(b) BUILT: STANDARD VERO-BOARD: 0.1" MATRIX PCB CARD (2.5" x 3.75" / 64 x 95 mm)

(c) FUNCTION: MIMIC 'MUTE' P/B-INTO KEYBOARD MATRIC SCANNER

(d) BASIC OPERATIONAL ACTION: GIVING TOTAL PROTECTION, WITH SIMPLICITY

(e) MODIFICATION: USES "IEEE 488" - PCB POSITION / PLUGABILITY / EASY REMOVAL
THE SOCKET PROVIDES: B+; GND; AND DUMMY PIN = MECHANICAL STABILITY,
WHEN USED WITH FORWARD PCB CARD GUIDE (ORIGINAL)

(f) REMOVAL: TOTAL "FAIL-SAFE" - PLUGABILITY: NO CHANCE FOR ERROR, WITH CARE

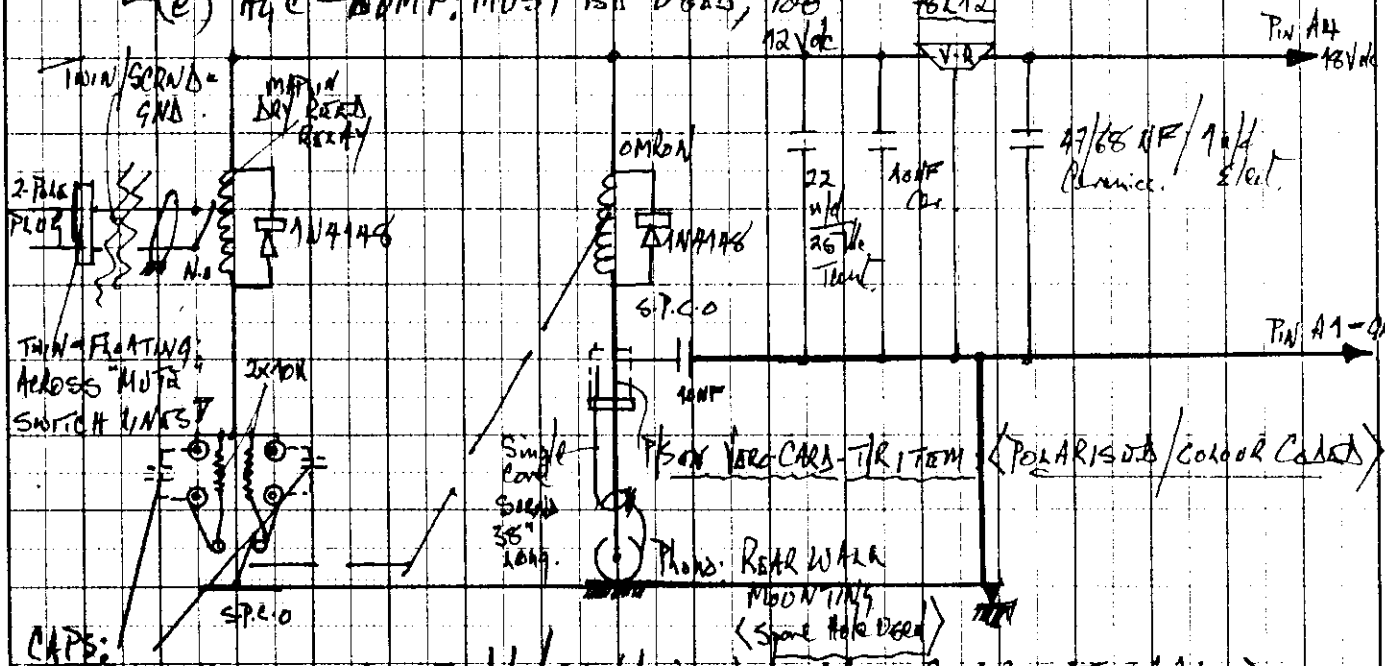
ACTION: (a) GIVES VERY EFFECTIVE T/R OPERATION PLUS, HIGH ISOLATION @ front end! FULL RX-SHUT DOWN.

(b) YES! IT GIVES an initial Pulse ON STR8212 "SWITCH ON."

(c) THIS 'Pulse' IS NOT RECOGNISED; 8212 - IS INHIBITED - BY VIRTUE OF ITS "SELF TEST" ROUTINE!

(d) FOR 'DATA' MOTOR-CURRENT SWITCHING SPEED MAY NOT BE GOOD ENOUGH

(e) AGC - DUMP: MUST BE USED, TOO



CAPS:

(a) CURRENT VALUES = 2 x 47n/d / 25Vdc in USE (ALL CURRENT CARDS)

(b) THEY ARE PLUGGABLE - ON ALL CURRENT CARDS

AT 18Vdc from 8212: STAND-BY CURRENT of T/R CARD = 10 Ma
THE "PULSED" CURRENT WHEN T/R ACTIONED = 50 Ma — ANALOGUE METERED

Chapter 1

PRINCIPLES OF OPERATION

1 INTRODUCTION

The STR8212 digital high performance HF receiver, operating in the frequency range 15 kHz to 40 MHz, is one of a new generation of radio receivers that use VLSI technology and Digital Signal Processing (DSP) techniques, giving many advantages over conventional analogue designs. Northern Telecom has developed a new form of Analogue to Digital Converter (ADC) having far greater resolution, linearity and accuracy than conventional ADCs. The Northern Telecom Pulse Density Modulator ADC has been designed specifically for radio applications and is implemented as two Very High Performance Integrated Circuits (VHPIC).

Once the signal has been digitised it is processed in the DSP modules which are based on standard VLSI DSP devices. The receiver functions of channel selection, filtering, demodulation and automatic gain control (AGC) are carried out by software algorithms operating within the DSP modules.

The steep roll off and high stop band rejection performance of the digital channel filters gives excellent selectivity when working in dense signal environments. Additional filters can be added to the standard receiver by software upgrades up to the limit of available memory. Filters can also be customised for special applications.

Digital demodulation is of high fidelity and special demodulation algorithms can be added by software upgrades to match the introduction of new signal modulation types.

The receiver is provided with extensive BITE (Built In Test Equipment) facilities which give a comprehensive fault detection and location capability. On line monitoring circuits are fitted which continually monitor the operation of the receiver without affecting its performance. In addition, the receiver is fitted with off line BITE circuits to monitor the performance both at power up and when commanded by the operator.

An optional digital output module gives the user access to the high resolution digital representation of the radio signal via an optical fibre interface on the rear panel. This interface can be used in many applications where the user wishes to carry out further signal processing or recording in the digital domain.

1.2 Architecture

A simplified block diagram is shown in Figure 1. The receiver is basically a triple superhet design of very high dynamic range where the signal path consists of amplification and up–conversion to a 1st IF of 70.050 MHz. The signal is filtered by a crystal roofing filter, further converted to a 2nd IF of 50 kHz and then digitised and converted to baseband in a format suitable for processing in DSP devices.

The IF levelling detectors, channel filtering, demodulation, audio AGC and post demodulation filtering are performed in the digital domain. The processed signal is then converted back to the analogue domain and the audio outputs generated.

The two synthesiser modules generate all the local oscillator and clock frequencies which are locked to the receiver reference oscillator. These frequencies can also be locked to an external 10 MHz reference.

The receiver operation is controlled via a CMOS 16–bit microprocessor and it can be operated both manually from the front panel or via a choice of remote control links.

1.3 Mechanical Design/Construction

The mechanical design ensures the maximum separation and screening of the digital and sensitive analogue sections of the receiver. This is used to prevent internal interference problems occurring whilst allowing plug–in modules to be used extensively to achieve excellent maintainability. The receiver layout is shown in Figure 2.

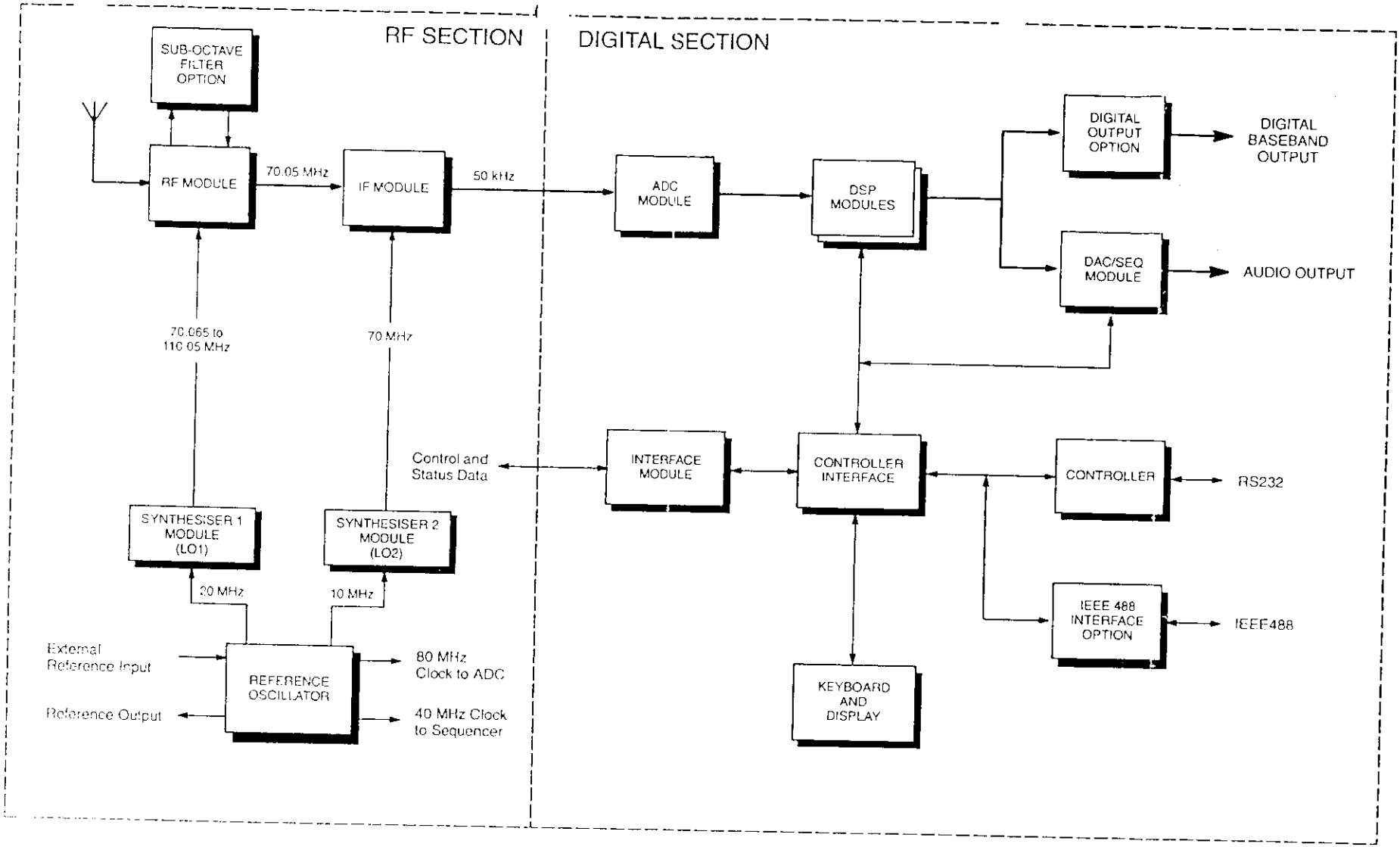


Figure 1 STR8212 Simplified Block Diagram

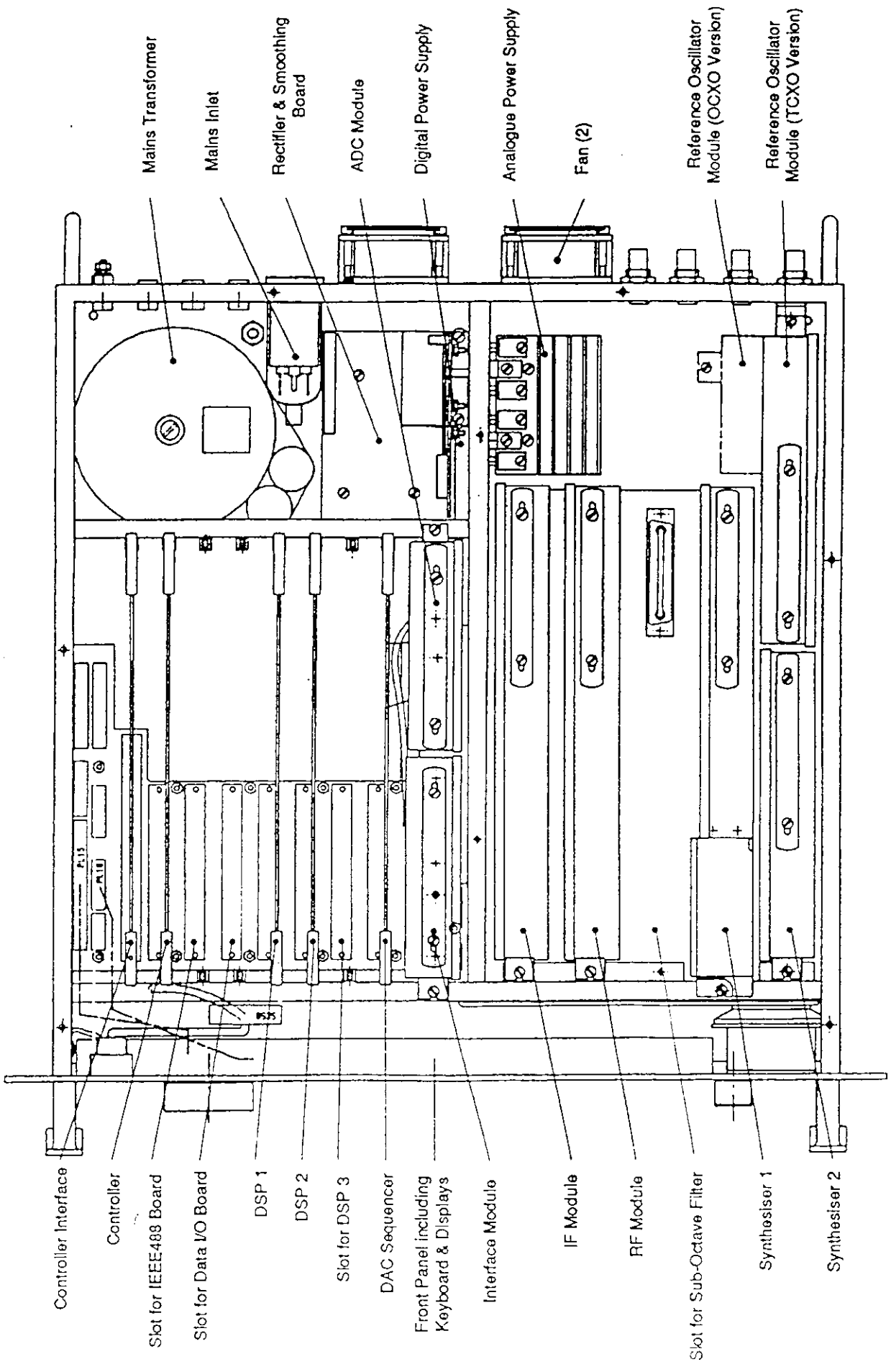


Figure 2 Mechanical Layout

2 RF SIGNAL PATH

RF amplification and conversion to the 1st IF is carried out in the 'RF Module'. Signal filtering and conversion to the 2nd IF is carried out in the 'IF Module'.

A block diagram of the RF module and IF module is shown in Figure 3.

The RF input to the receiver, in the frequency range of 15 kHz to 40 MHz, is routed from the antenna socket on the rear panel of the receiver to the RF module. The signal path is applied to the input protection circuit which protects the equipment from high level transients such as those induced by lightning and from other high level signals. The output of the protection circuit is then supplied to the optional sub–octave filter module which filters out signals that contribute to second order intermodulation distortion. In receivers not fitted with this module, a coaxial shorting link is fitted to the RF backplane, thus routing the signal path back to the RF module. The signal path then passes through the first of a pair of low pass filters which provide rejection to signals at the 1st IF frequency band (70.05 MHz) and to signals in the image frequency band (140–180 MHz). These filters also reduce the level of local oscillator leakage to the antenna input. The RF signal is then supplied to a pre–amplifier/attenuator stage. The pre–amp is used to maximise the sensitivity of the radio, although attenuators can be switched in when operating in the presence of large signals in order to enhance the spurious free dynamic range of the receiver. The signal then passes through the second low pass filter of the pair before being applied to the first mixer.

The RF signal path is then mixed with the first local oscillator (LO1) which translates the wanted signal frequency to an IF of 70.05 MHz. The tuning range of the first LO is thus 70.65–110.05 MHz. The mixer is terminated with an IF diplexer which maintains a constant impedance for the various mixer products. Finally the signal is amplified then fed out to the IF Module via a buffer stage.

The signal path is then connected to the first stage of the IF module which comprises a PIN diode attenuator. The IF attenuator has a control range of 40dB and is used to prevent overload of the subsequent A to D convertor stage when large in–band signals are present. The level of attenuation is determined by the IF AGC detector located in the Digital Signal Processor. The attenuation setting (or gain) is either automatically or manually controlled depending on operator setting of the front panel. Further details of operation is provided in Section 5.

The RF signal path is then applied to a crystal filter which band limits the wanted signal thus providing discrimination against out of band signals and unwanted mixer products. The standard roofing filter has a bandwidth of 16 kHz but provision is made for a second broader bandwidth roofing filter with low group delay characteristics. Low group delay filters are suitable for phased matched array applications. The signal is then presented to a low noise amplifier which is used to compensate for the filter loss. This is followed by a buffer amplifier which presents a good match to the second mixer stage. The second mixer mixes the signal with a pure 70 MHz signal from the second local oscillator (LO2) and thus down–converts to a 50 kHz second IF which is a suitable frequency for subsequent digitisation. The mixer is an image reject design which is used in conjunction with other filtering to reject the second image response at 69.95 MHz. The image reject mixer by itself provides rejection in excess of 35dB and details of how this is achieved are provided in Chapter 6.2.

Both RF and IF modules are provided with detection circuits and injection points to allow module diagnostics. These facilities, in conjunction with the STR8212 BITE circuitry, provide 'on–line' monitoring and 'off–line' testing of the modules.

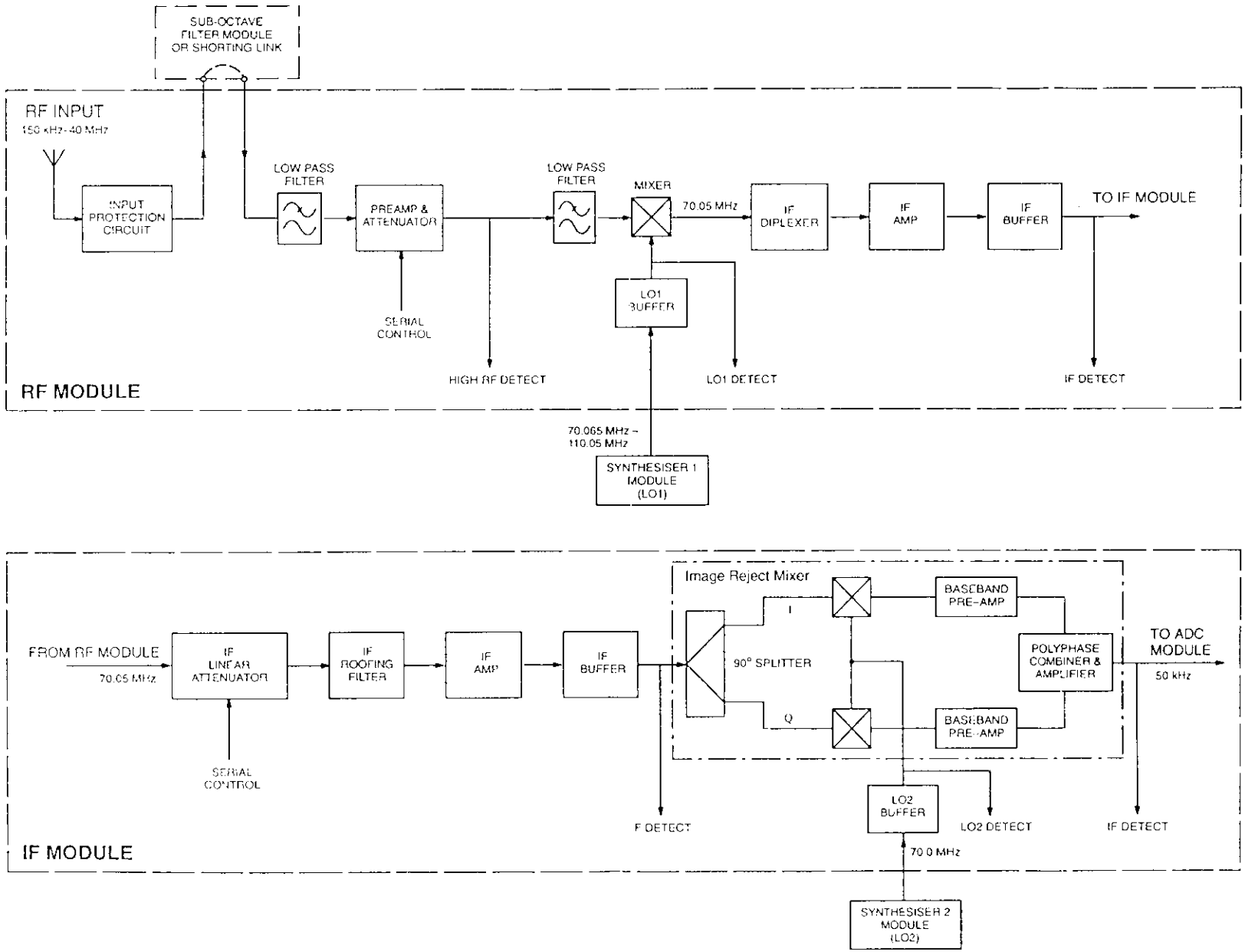


Figure 3 RF/IF Modules - Simplified Block Diagram

3 DIGITAL SIGNAL PATH AND AUDIO OUTPUT

The block diagram, shown in Figure 5, shows the signal path through the ADC, Digital Processing and Audio sections.

The second IF (50 kHz) is routed to the ADC where it passes through an anti–alias filter. This low pass filter augments other filtering in the receiver to provide suppression of an alias response centred 100 kHz above the wanted frequency. The signal is then supplied to the Pulse Density Modulator (PDM) for digitisation . The PDM is a form of signal–delta modulator that over–samples at many times the Nyquist rate. The single bit stream from the PDM is then applied to a simple 'SINC' filter which averages the high number of input samples. This increases the precision of the samples at the expense of decreasing the sample rate. After this first stage of digital filtering the signal is subjected to a digital mix which converts the 50 kHz IF to a 0 Hz IF with in–phase (I) and quadrature (Q) outputs. The I and Q channels are filtered further by a 120 tap FIR filter.

The digitised signal is passed to the DSP subsystem for further processing. The DSP subsystem contains two DSP cards (in the standard version of STR8212) each of which houses two DSP processors. These are designated DSP1A, DSP1B, DSP2A and DSP2B.

The digitised signal (I and Q) is firstly scaled up in size to ensure that dynamic range is not adversely affected by the precision of the arithmetic employed in subsequent DSP processes. The I and Q channels are then supplied to an IF level detector which calculates the level of the signal (an algorithm approximating $\sqrt{(I^2+Q^2)}$ is used for this). The I and Q channels are applied to a filter which is designed to correct for pass–band imperfections in the ADC module digital filters.

DSP1B contains a large number pre–programmed digital channel filters. These are of a linear phase design (FIR) which thus possess no group delay distortion. Shape factors of better than 1.66:1 (1dB to 100dB) are achieved for filters with bandwidths greater than 2.4 kHz. The 10 kHz filter has a shape factor of 1.12:1. Currently available filters are listed in Table 1. There is sufficient space in DSP memory to accommodate new filter requirements.

The DSP2B processor provides the demodulation function. The digital signal representation is converted from the rectangular co–ordinate system (I+Q) into polar form. The resulting magnitude and phase components (R and Θ) are summarised below for the different demodulators (AM, FM, CW and SSB). The R component represents the envelope of an AM signal and is therefore routed directly to the output of the demodulator. In order to provide an FM demodulator, delta changes in successive phase (Θ) samples are detected and these are output as an amplitude. In order to demodulate CW a 'Beat Frequency Oscillator' (BFO) is required. This is implemented by modifying phase (Θ) on a sample by sample basis to synthesise the required output tone frequency. R and Θ are then converted back to rectangular form where one of the ordinates ($R\cos\Theta$) provides the demodulated output. SSB demodulation is by the Weaver method. In this scheme, local oscillator 1 is off tuned to f_c as shown in Figure 4. The frequency the synthesiser tunes to is equal to $f_o \pm(0.3+B/2)$ where f_o is the nominal receiver frequency and B is the bandwidth of the selected filter.

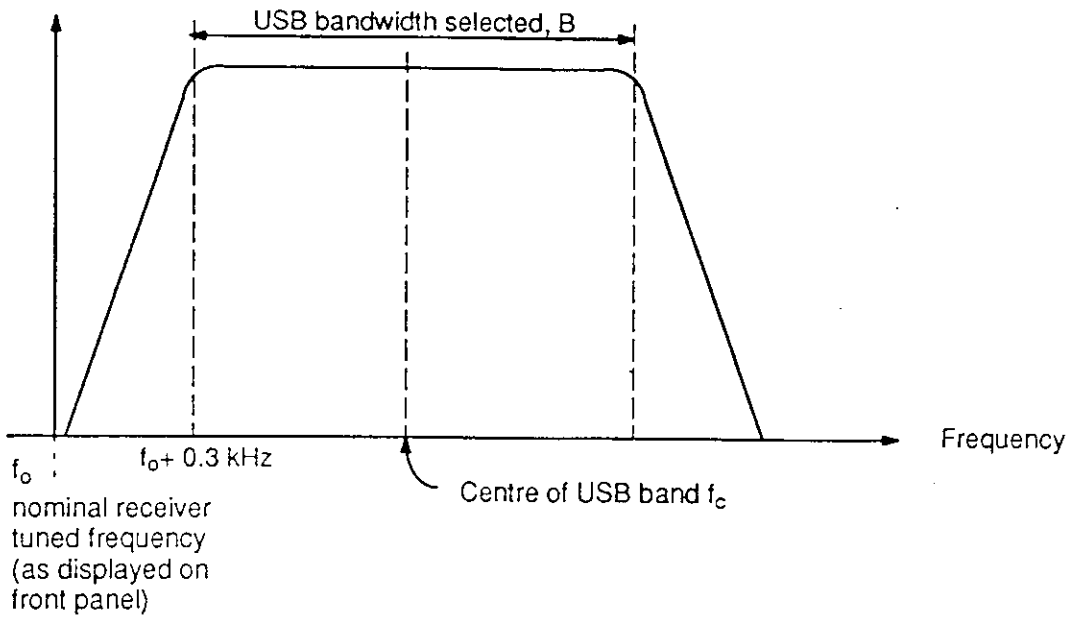


Figure 4 Frequency Settings for USB Demodulation

As a result of tuning the synthesiser to f_c and downconversion to 0 Hz IF, the USB signal folds over on itself about the centre frequency of the filter. The BFO is then used to translate the signal in frequency by B/2 and after polar to rectangular conversion a demodulated output is obtained.

An ISB demodulator is also available from Northern Telecom on request.

The DSP2B processor provides the audio AGC function and baseband filtering. The 'R' component from DSP2A is used to control the AGC function for AM, CW and SSB modes. The AGC function essentially scales the signal (either up or down) to maintain a constant audio output level. This is further discussed in Section 5. The signal path then passes through one of two baseband filters which can be selected from the front panel. A speech filter with a 300 Hz to 3 kHz passband is available or alternately a 'data' filter suitable for receiving digital speech can be selected. The 'data' filter is a low pass filter with a nominal bandwidth of 8 kHz.

The digitised signal is then routed from the DSP subsystem to the DAC/Sequencer card where the signal is converted to analogue form. A dual channel D to A convertor is employed to enable independent channels to be output in independent side-band (ISB) applications. The two outputs (LINE 1 and LINE 2) are routed through analogue filters which remove the quantisation steps from the signal before being supplied to the rear panel via buffer amplifiers. An audio amplifier is connected to LINE 1 and this drives the internal speaker and headphone output.

An optically coupled digital output interface is available as an option for the STR8212 receiver. This enables access to the digitised signal at various points in the DSP processing as shown in Figure 6.

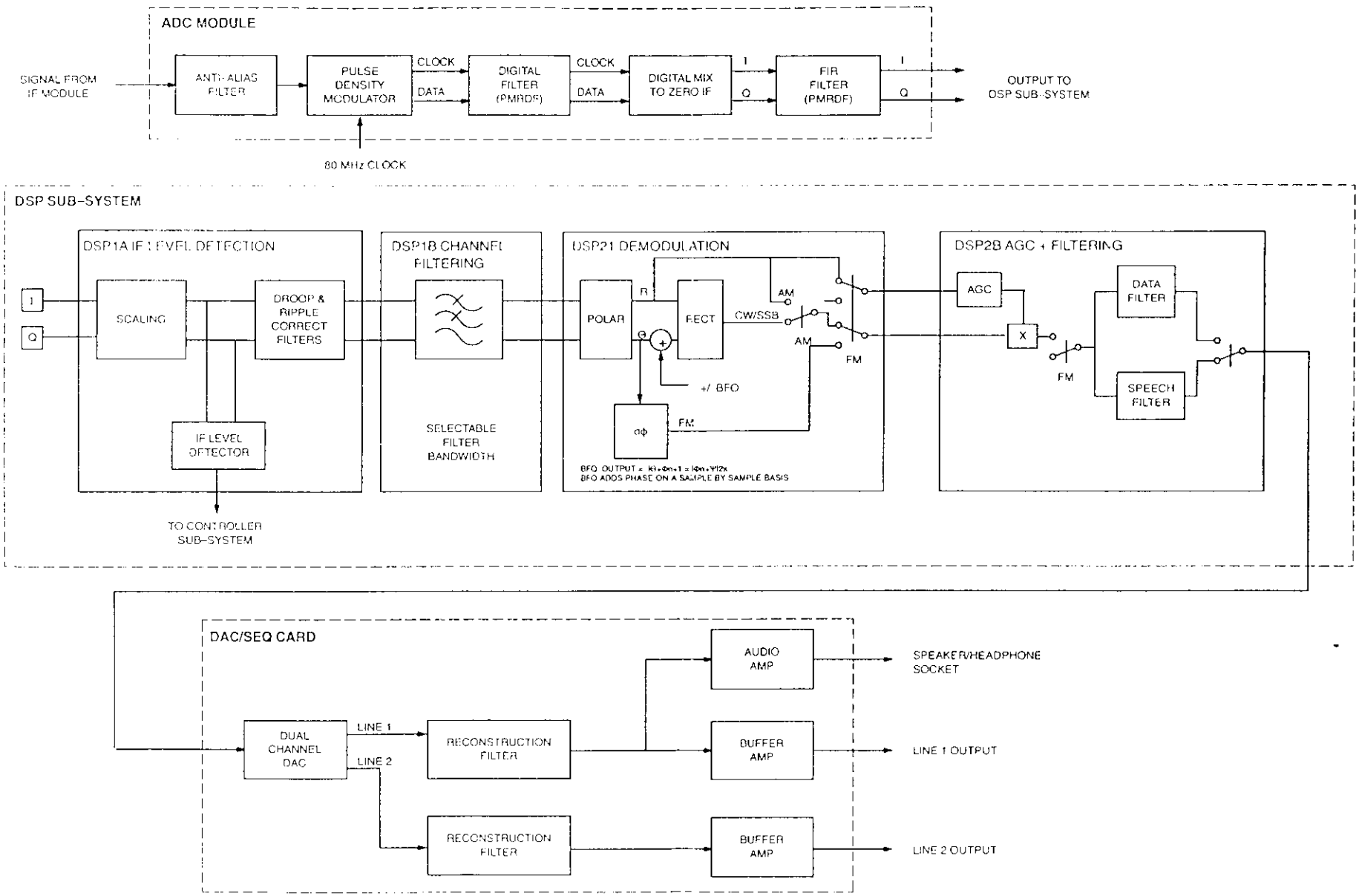


Figure 5 ADC, Digital Signal Processing and Audio Sections

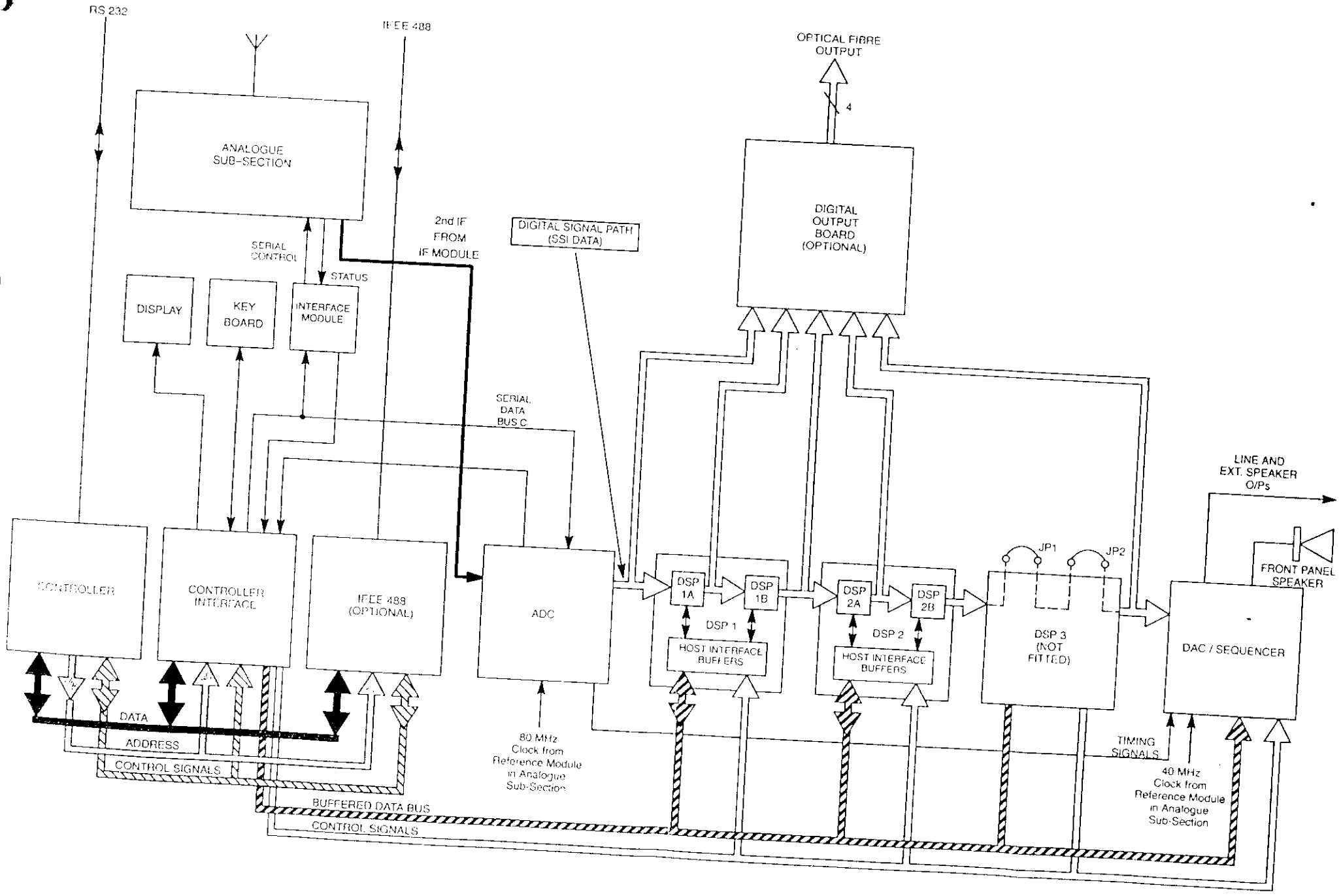


Figure 6 STR8212 Control Interfaces

	Nominal Bandwidth (Hz)	3dB point relative to centre (dB)	Stopband attenuation (dB)	Stopband edge relative to centre (Hz)	Shape factor
i)	320	160	80	612	3.83
ii)	360	179	100	745	4.16
iii)	500	250	100	909	3.64
iv)	680	340	100	968	2.85
v)	800	398	100	977	2.45
vi)	1200	598	100	1187	1.98
vii)	2400	1197	100	1781	1.49
viii)	2700	1350	100	2246	1.66
ix)	3000	1503	100	2059	1.37
x)	6000	3002	100	4995	1.66
xi)	10000	4995	100	5600	1.12
xii)	12000	6000	100	10000	1.66
xiii)	15000	Straight through from roofing filter			

Table 1 Channel Filter Bandwidths for Standard STR8212

4 FILTERING CHARACTERISTICS

The signal path contains a number of stages of filtering that reject unwanted signals and maximise the signal to noise ratio of the wanted signal. The following description summarises the characteristics of each stage.

4.1 Front End Low Pass Filter

This two stage filter produces rejection of signals at the first IF frequency of 70.05 MHz and signals in the image band of 140.1 to 180.1 MHz. These filters also provide isolation of the local oscillator with respect to the antenna input. Each filter stage provides in excess of 50dB of rejection.

4.2 Roofing Filter

The roofing filter resides in the IF module and has a centre frequency of 70.05 MHz. It provides the first stage of selectivity in the receiver rejecting out of band signals by 60 to 70dB. A typical plot of the standard filter is shown in Figure 7. Significantly, it rejects the second image frequency (69.95 MHz) in the first IF path by at least 60dB. When combined with the rejection provided by the image reject mixer in the IF module, a total second image rejection performance in excess of 95dB is typically achieved. The roofing filter also contributes to the suppression of the first alias response centred at 100 kHz above the tuned frequency of the receiver. The mechanism responsible for the generation of a potential first alias is of course in the digitisation process within the A to D convertor module.

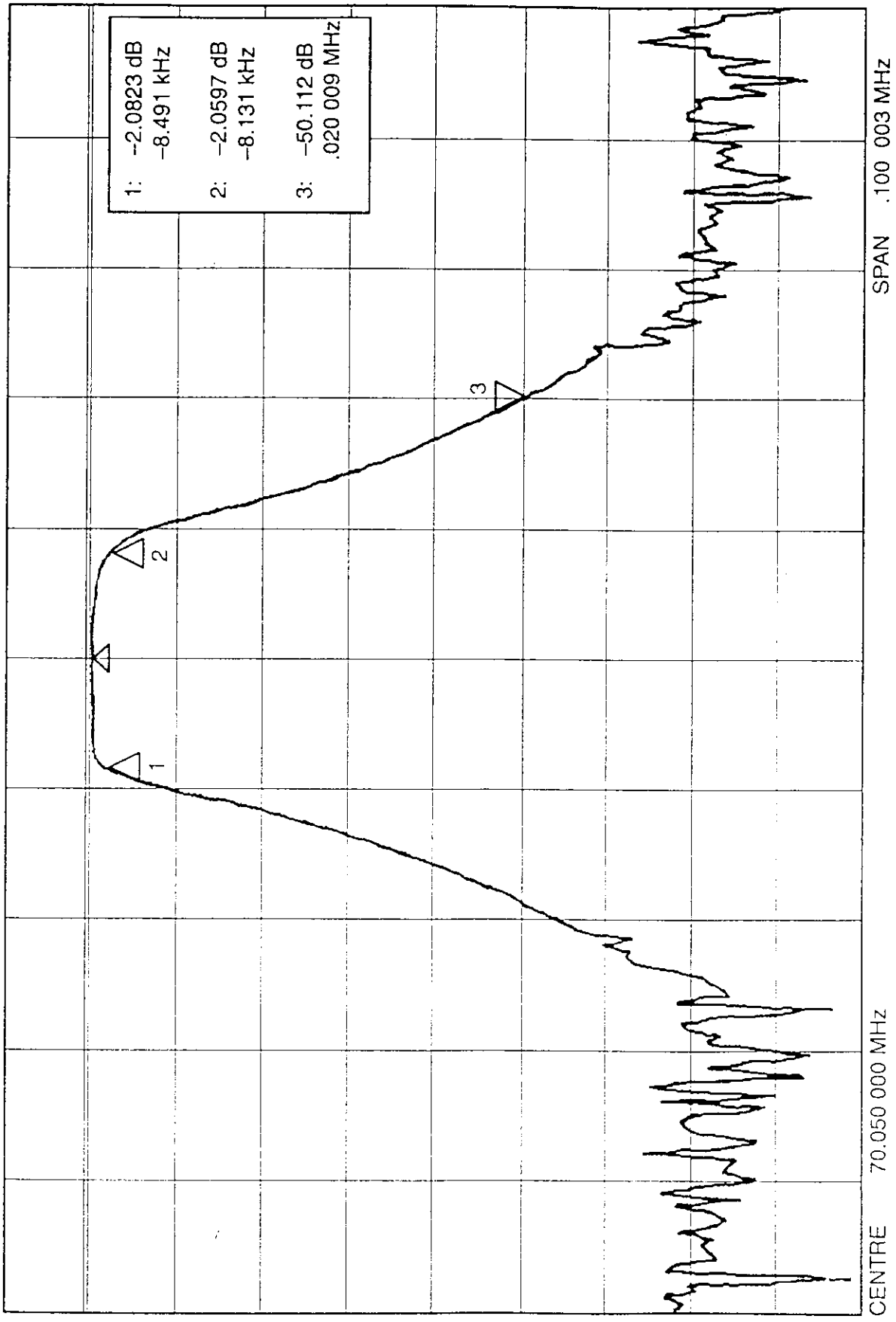


Figure 7 Crystal Filter Frequency Response

4.3 Filtering in the A To D Convertor Module

The A to D convertor is preceded with an anti–alias filter. This filter is situated in 2nd IF and is designed to provide at least 30dB of rejection of the first alias band which occurs 100 kHz above the wanted signal band (ie at 150 kHz). The SINC filters provide another 30dB of rejection to the first alias band. The total receiver rejection to the first alias is typically 130dB. Subsequent alias bands are suppressed even further than this. The final FIR filter in the ADC module provides a band limited digital signal at a down sampled output rate of 33.3 kHz. This filter is implemented as a low–pass filter because of the I and Q 0 Hz IF. It has a 1dB passband of 10 kHz (effectively 20 kHz passband) and achieves a stop band in excess of 110dB by the half sampling frequency.

4.3 DSP Filtering

DSP1B contains a number of selectable channel defining filters which have been listed in Table 1. A plot of the 10 kHz filter is provided in Figure 8.

DSP2B contains baseband filtering. Either a speech filter or a data filter can be selected. The speech filter consists of a 300 Hz highpass IIR section cascaded with 3 kHz lowpass FIR. Each stage has a 50dB stop band. The data filter is an 8 kHz lowpass filter implemented as an FIR with a 50dB stop band.

4.3 Audio Filtering

The DAC is followed by an audio reconstruction filter that removes the quantisation steps from the reconstructed analogue signal. This low pass filter is designed to ensure that alias outputs are suppressed by about 50dB at the audio output. The 3dB point is at approximately 8 kHz.

5 AGC OPERATION

The gain in the radio can be adjusted in one of three places, in the DSP, at the IF attenuator and at the RF attenuator. The RF attenuators are under the control of the user. They can be set to a specific value via the front panel or adjusted via the gain control if the receiver is in manual mode. If the radio receives a very large signal, which may adversely affect spurious free dynamic range the 'HIGH' legend appears on the front panel, as a prompt to the user to insert RF attenuation.

There are two AGC modes, full and partial AGC. Full AGC gives automatic control over the DSP gain and the IF attenuators, whereas partial AGC maintains automatic control of the DSP gain and allows the user to control the IF attenuators.

The AGC system of the radio consists of two subsystems; the feedback AGC, where the IF attenuators are controlled by the level detectors in DSP1A and the feedforward AGC system which is contained in DSP2A and DSP2B.

5.1 Feedback AGC

The signal amplitude is assessed in DSP1A. In CW or SSB modes the change in signal amplitude is also monitored and if the signal decays by more than a fixed amount a hold–off is implemented. The length of this hold–off is dependent upon the AGC speed selected on the front panel and is currently set to 1s for Fast and 1.5s for Med and Slow. The hold–off is overridden if the signal increases again. The threshold level is subject to hysteresis control. If the signal amplitude is greater than an upper threshold and the maximum IF attenuation level has not been reached then a request for more IF attenuation is sent to the controller. If it is less than a lower threshold and the minimum IF attenuation level has not been reached then a request for more IF gain is sent to the controller.

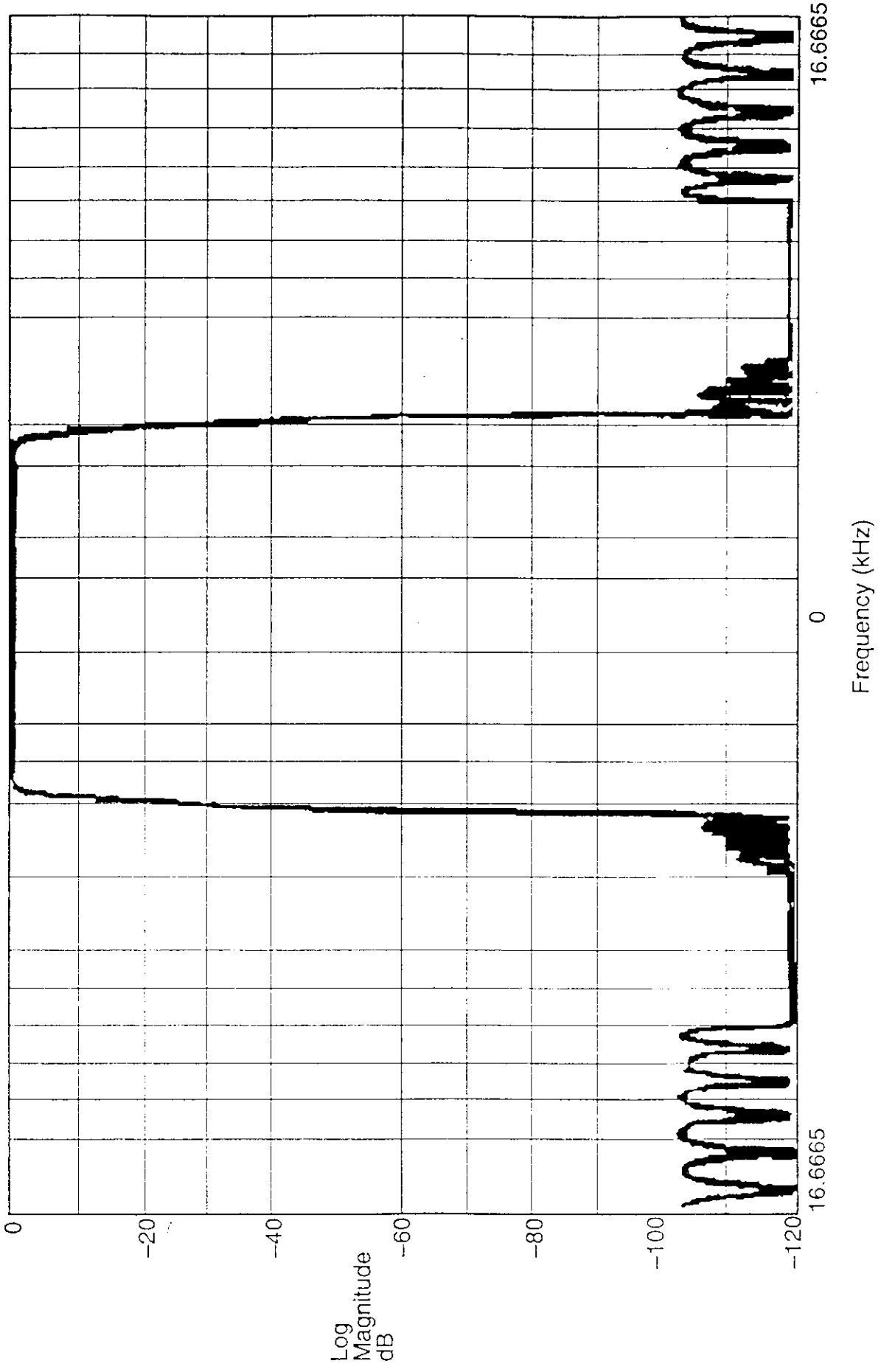


Figure 8 10 kHz Channel Filter Frequency Response

The controller, after ensuring that the radio has control of the IF attenuators, processes the request from the DSP and either increases or decreases the IF attenuation level by 6dB, sending a new control word to the IF attenuators in the IF module via the serial link. The controller also sends a reply to DSP1A to say that it has initiated the change and sends the new state of the IF attenuators, ie whether they are at maximum, intermediate or minimum IF attenuation level. DSP1A then holds off for 2ms, to allow the attenuators chance to settle, before reassessing the signal and requesting another 6dB change.

Note that the feedback AGC system only operates when signal powers in excess of –37dBm are present at the RF antenna input.

5.2 Feedforward AGC

The feedforward or audio AGC is accomplished in DSP2B. The signal is filtered using the appropriate time constants, incorporating any hold times if necessary according to the mode. The signal amplitude is then compared with a preset threshold value. This comparison is then used to calculate the scaling operations required to maintain a constant audio output. A combination of division and bit shifting is used to ensure the maximum amount of signal information is conveyed to the output at the correct audio level.

The signal level is also compared with any preset squelch level and a decision as to whether or not the output should be muted is made. The relevant messages are relayed back to the controller. The squelch level contains hysteresis such that the audio should not flicker on and off with small changes in signal strength.

5.3 Manual Operation

During full manual operation there is a defined order in which the various gain and attenuation levels are adjusted. When reducing the gain (turning the gain knob anti–clockwise) the DSP gain is reduced first, followed by an increase in IF attenuation up to maximum and finally an increase in RF attenuation up to the maximum value. This last step is indicated to the user by the RF ATT LED flashing on and off, which flags that the current RF attenuation level is no longer equal to the user defined level. The IF attenuation level is changed in 1dB steps whereas the RF attenuation level is changed in 5dB steps.

When increasing the gain level (turning the gain knob clockwise) any excess RF attenuation above the user defined level is removed first (switching off the flashing LED). This is followed by a reduction in the IF attenuation level, followed by an increase in DSP gain.

In partial manual control the same conditions apply except that the user has no control over the DSP gain level.

6 CONTROL SUB–SYSTEM

The Control sub–system consists of a 68000 based Controller card, a Controller Interface card, an optional IEEE488 card and the front panel assembly which comprises the keyboard, display board and other front panel controls.

The Controller card contains all the software required to control the radio. It accepts operator commands from the front panel and converts these into suitable formats for control for various modules such as Local Oscillator 1. The Controller sub–system also responds to remote commands from the RS232 interface or the IEEE488 interface if fitted. It also provides status information to these ports. Details of remote operation are provided in the Operator's Handbook. The Control sub–system is shown in Figure 6.

The Controller board directly controls the RS232 interface and interfaces with the rest of the radio and the man–machine interface via the Controller Interface board. The Controller communicates with the Controller Interface and IEEE488 interface via a 68000 data bus.

The Controller Interface board relays all the information input via the front panel to the Controller board and updates the displays in response to instructions from the Controller. It is also responsible for the serial control interface to the analogue sub–section, ADC module and the LEDs; these are covered in more detail in Chapter 6.16. Status information from the analogue modules is relayed back to the Controller board via the Interface module and the Controller Interface board.

The Controller communicates with the DSP sub–system via the Controller Interface. It informs the DSP of changes in bandwidth, BFO value, AGC constants, gain and squelch levels and the status of the IF attenuators. During BITE the Controller also instructs the DSPs to carry out their own BITE routines. The DSPs inform the Controller of the squelch status, the gain setting in manual mode, BITE status and request changes in the IF attenuators.

The Controller converts the frequency on the front panel to the correct synthesiser setting, the actual value is dependent upon the mode selected and informs the Synthesiser 1 module of the change.

The Controller board includes non–volatile memory which is used for the storage of up to 99 sets of channel information and up to 9 sets each of channel and frequency scan data.

The Controller exercises BITE at power up and on command from the front panel. The Controller also monitors BITE status lines during normal operation such as the 'Synthesiser out of lock' lines.

Chapter 2

INSTALLATION

1 INTRODUCTION

The purpose of this chapter of the manual is to provide sufficient information to allow the installer to correctly install and set up the STR8212 HF Receiver.

The receiver is housed in a vented steel enclosure which is designed for use in a 19 inch rack mounting system. Unit cooling is fan assisted and requires a 1U space below the unit for circulation. The unit can be free standing on a plane surface as long as suitable feet are used to provide adequate air circulation from beneath the unit.

The receiver can be used in several different configurations with various options as follows:

- Stand alone operation
- Remote operation (RS232 or IEEE 488)
- Computer controlled operation
- Digital output option
- Additional DSP PCB option

The options are described in Chapter 1, all variants of installation being described in this section.

Before the receiver is installed in an equipment rack, the following have to be checked and set up.

• Voltage Input and Fuse Setting	Paragraph 2
• IEEE 488 PCB Setting	Paragraph 3
• RS232 PCB Setting	Paragraph 4

2 VOLTAGE INPUT AND FUSE SETTING

CAUTION

Operating the unit on the wrong voltage setting will damage the circuitry of the receiver and will invalidate any warranty

IMPORTANT NOTICE

THE STR8212 IS CAPABLE OF OPERATING FROM 110V, 220V OR 240V AC MAINS SUPPLIES DEPENDING UPON THE SETTING OF THE VOLTAGE SELECTOR SWITCH THAT IS BUILT INTO THE MAINS CONNECTOR AT THE REAR OF THE UNIT. BEFORE THE RECEIVER IS CONNECTED TO THE MAINS SUPPLY, THE VOLTAGE SELECTOR SWITCH MUST BE CHECKED TO ENSURE THAT IT IS CORRECTLY SET FOR THE PARTICULAR LOCAL MAINS SUPPLY, AND THAT THE CORRECT MAINS FUSE IS FITTED (1.25A ANTISURGE FOR 220/240V OR 2.5A ANTISURGE FOR 110V, BOTH BUSSMAN TDC436).

2.1 Setting the Input Voltage

The method of setting the input voltage is as follows:

(1) Obtain access to the rear of the receiver.

(2) Place a flat bladed screwdriver in the slot at the top of the unit and twist. Pull down the plastic cover to obtain access to the voltage select drum.

> **CAUTION**
>
> Attempting to turn the drum without first removing it from its housing will damage the contacts at the rear of the drum.

(3) Use a small screwdriver to remove the drum.

(4) Replace the drum such that the required setting lies in the centre of the window.

(5) Close the cover and check that the required setting is shown in the window.

2.2 Fuse Setting

The method of setting the fuse to the correct value is as follows:

(1) Obtain access to the rear of the receiver.

(2) Place a flat bladed screwdriver in the slot at the top of the unit and twist. Pull down the plastic cover to obtain access to the voltage select drum.

(3) Use a small screwdriver to ease the fuse and fuseholder out of its housing.

(4) Fit the correct fuse in the fuseholder in accordance with the information given in Paragraph 2.

(5) Replace the fuse and fuseholder and close the cover.

3 IEEE 488 PCB SETTING

The setting of the IEEE 488 address on the IEEE 488 PCB is dependent upon the configuration required. The STR8212 receiver has a range of remote control capabilities as follows:

- Every receiver can be remotely controlled via an IEEE 488 link reporting status and data back to the remote controller.
- Every receiver can act as the Master Controller of other receivers via the IEEE 488 link.
- All features that can be exercised locally are available from the remote link with the exception of power switching, internal speaker switching and volume control.

If one receiver is controlling remote receivers, it must be set as the System Controller and all other receivers need to be assigned an IEEE 488 address between 01 and 30. If one or more receivers are being controlled by a computer or external IEEE 488 Controller, all receivers must be assigned an IEEE 488 address between 01 and 30.

The procedure to set the IEEE 488 PCB as the System Controller is as follows:

(1) Remove the IEEE 488 PCB in accordance with Chapter 5, paragraph 6, removal steps (2) to (5).

(2) Locate the IEEE 488 switch and set the System Controller switch to ON. (Figure 2 of Chapter 5 refers).

(3) Refit the PCB in accordance with Chapter 5, paragraph 6, replacement steps (3) to (6).

The procedure to set the IEEE 488 PCB address to a value of between 01 and 30 is as follows:

(1) Remove the IEEE 488 PCB in accordance with Chapter 5, paragraph 6, removal steps (2) to (5).

(2) Locate the IEEE 488 switch and use the five Address switches to set the required address. The address is a five bit binary number located on bits 0 to 4,

e.g. Adress 13 Bit 4 3 2 1 0
0 1 1 0 1

NOTE: No two receivers should be set to the same address as collisions will occur.

(3) Refit the PCB in accordance with Chapter 5, paragraph 6, replacement steps (3) to (6).

4 RS232 PCB SETTING

The RS232 link parameters for the STR8212 receiver are factory pre-set and there should be no requirement to change these settings for normal master/remote operation.

If a receiver is being controlled from an external computer, the RS232 Baud rate of the receiver must be set to match that of the computer. The procedure to set the RS232 Baud rate is as follows:

(1) Remove the Controller Interface PCB in accordance with Chapter 5, paragraph 6, removal steps (2) to (5).

(2) Locate the RS232 switch and set the Baud Select switches as follows:

Baud Rate Required	Switch Settings Bit 3	Bit 2	Bit 1
150	0	0	0
300	0	0	1
600	0	1	0
1200	0	1	1
2400	1	0	0
4800	1	0	1
9600	1	1	0
19200	1	1	1

(3) Refit the PCB in accordance with Chapter 5, paragraph 6, replacement steps (3) to (6).

5 INSTALLING THE RECEIVER IN THE RACK

The STR 8212 enclosure is compatible with standard 19 inch racking systems. The unit is 2U high (3.5 in. or 89 mm) and the depth measured from the rear of the front panel is 18.2 in. (466 mm). The STR 8212 is designed to sit on angle bracket runners and four slotted holes in the front panel permit the receiver to be secured to the rack. The air vents on the lower face of the chassis must not be obstructed, so a 1U spacing panel should be located below the unit.

The procedure to fit the receiver is as follows:

WARNING

THE UNIT WEIGHS APPROXIMATELY 15KG. SUITABLE PRECAUTIONS MUST BE TAKEN WHEN REMOVING THE UNIT FROM THE EQUIPMENT RACK TO PROTECT BOTH THE MAINTAINER AND THE EQUIPMENT.

(1) Locate the mounting position for the receiver and fit the angle bracket runners, as appropriate, to the rack.

(2) Fit receiver into rack and secure in place with four bolts through the slotted holes in the front panel.

6 CABLING THE UNIT

In addition to the mains earth, a safety earth stud is provided on the rear of the chassis. The receiver provides an N type female connector on the rear panel to which the connection from the feeder system of the antenna should be made. The receiver will operate without any ancillary audio connections being required as an audio output is available from the internal loudspeaker situated on the right hand side of the front panel.

With reference to Figure 1, determine which cables will be required for the various options available.

The procedure to cable the unit is as follows:

(1) Connect the antenna plug into the receiver and hand tighten only.

(2) Connect an earth lead between the stud on the receiver and the earth of the equipment rack.

(3) Connect the AUDIO lead to the AUDIO socket (If used).

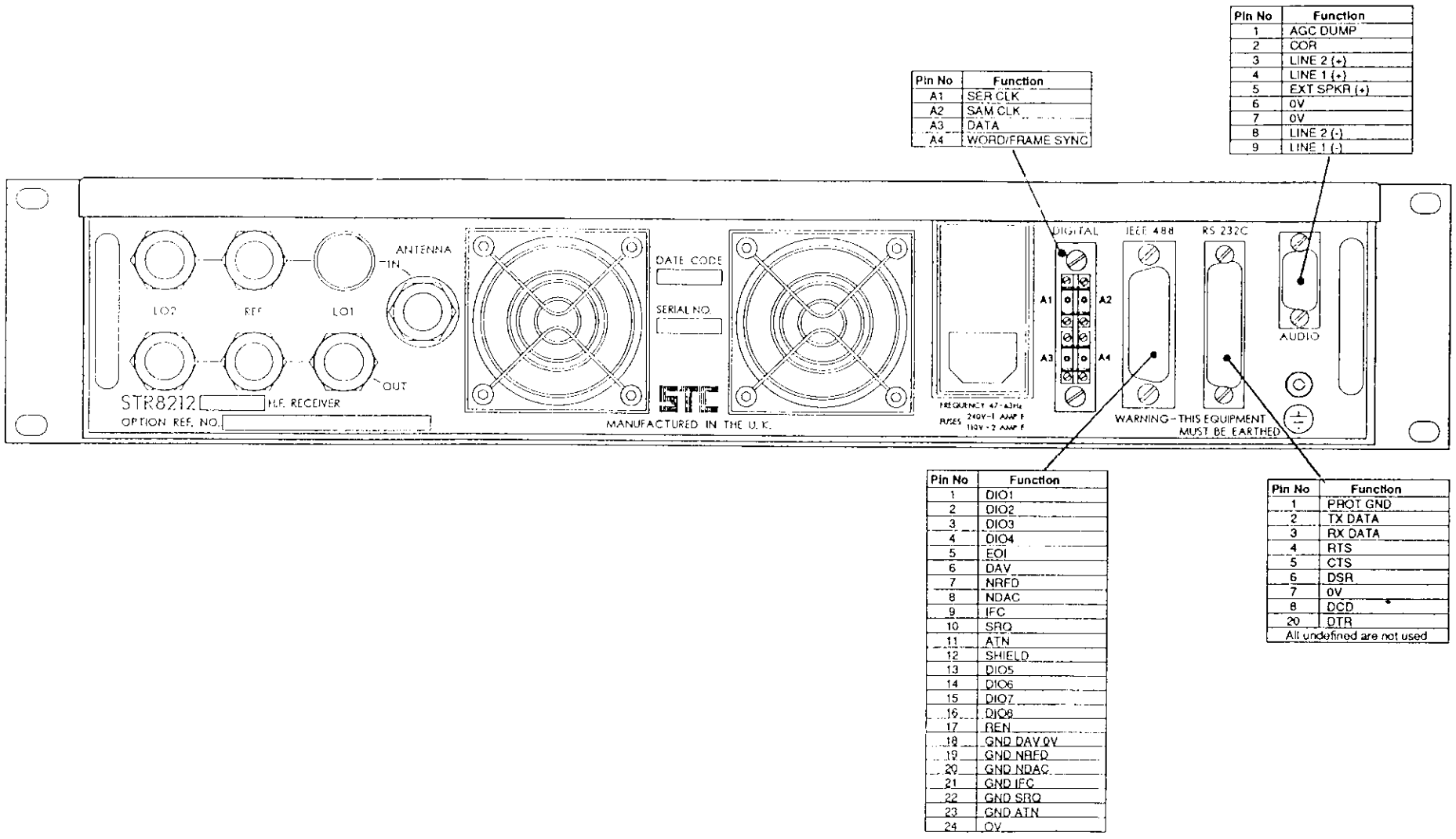
(4) Connect the RS232 lead to the RS232 socket (If used).

(5) Connect the DIGITAL lead to the DIGITAL socket (If used).

(6) Connect the IEEE 488 lead to the IEEE 488 socket (If used).

(7) Check that front panel ON/OFF switch is in its OFF position. Connect the power cable to the POWER INPUT SOCKET.

(8) Switch on the receiver and check basic operation.



Pin No	Function
A1	SER CLK
A2	SAM CLK
A3	DATA
A4	WORD/FRAME SYNC

Pin No	Function
1	AGC DUMP
2	COR
3	LINE 2 (+)
4	LINE 1 (+)
5	EXT SPKR (+)
6	0V
7	0V
8	LINE 2 (-)
9	LINE 1 (-)

Pin No	Function
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	SHIELD
13	DIO5
14	DIO6
15	DIO7
16	DIO8
17	REN
18	GND DAV 0V
19	GND NRFD
20	GND NDAC
21	GND IFC
22	GND SRQ
23	GND ATN
24	0V

Pin No	Function
1	PROT GND
2	TX DATA
3	RX DATA
4	RTS
5	CTS
6	DSR
7	0V
8	DCD
20	DTR
All undefined are not used	

Figure 1 - Connections for Remote Operation Showing Plastic Fibre Digital Output Option

Chapter 3

FAULT FINDING AND TEST PROCEDURE

1 INTRODUCTION

The aim of this Chapter is to allow fault diagnosis to module level and to provide a guide for the user about the built in test fault diagnosis. Built in test routines are invoked on power-up and on demand via the front panel. A flow chart is also included to aid the user should the radio not power-up correctly. For help with tracing faults within the module the user is referred to the modular breakdown in Chapter 6.

WARNINGS

PLEASE READ THE PRODUCT SAFETY INFORMATION SHEET BEFORE REMOVING THE TOP COVER.

WHEN THE TOP COVER IS REMOVED, DANGEROUS VOLTAGES ARE PRESENT IF THE UNIT IS CONNECTED TO THE SUPPLY. EVEN WITH THE POWER DISCONNECTED, A PERIOD OF TWO TO THREE MINUTES SHOULD BE LEFT TO ALLOW CAPACITORS TO DISCHARGE BEFORE WORKING NEAR THE POWER SUPPLY BOARD.

SEVERAL OF THE TESTS PERFORMED IN THIS CHAPTER INVOLVE THE REMOVAL OF MODULES. MODULES SHOULD ONLY BE REMOVED WHEN THE RADIO IS SWITCHED OFF AND DISCONNECTED FROM THE MAINS.

CAUTIONS

In the event of the radio being removed from its rack for test purposes, care should be taken when placing on a bench not to obstruct the air vents on the lower face of the radio.

Care should be taken to observe anti–static procedures where necessary.

2 USE OF EXTENDERS

At times it may prove necessary to lift the modules clear of the unit whilst still being connected to it, in order to monitor input and output signals. This can be achieved by the use of extenders. Drawings of the extenders and test lead required for the boxed modules are given in Appendix A. The 60mm board extenders for the digital cards are commercially available from BICC-Vero order code 38-42640F.

3 FAULT DIAGNOSIS

In order to verify correct operation of the receiver at power-up it is recommended that the user follows the procedure outlined in the flow chart provided in Figure 1. Alternatively, if a BITE failure message is displayed refer to Section 5.1 The aim of the flow chart is to provide an indication of possible faults. Additional notes have been included in Section 4 as further explanations for particular steps on the flow chart.

4 NOTES TO POWER-UP FLOW CHART

Step 3:

For further information on power supply faults refer to Chapter 6.13 Chassis and Power Supply.

Step 7:

Verify whether steps 9 and 15 take place successfully. If keyboards LEDs illuminate, fault is likely to be with the connection to the Display Board or on the Controller Interface. If steps 7, 9 and 15 do not verify, then the fault could be due to the Controller sub-system. As the bus interface between the Controller Interface card, Controller card and IEEE488 card is unbuffered, then a fault on any of the drivers will cause a failure of the control sub-system.

- If an IEEE488 is fitted then start by removing this card.
- The best way of isolating the fault to either the Controller or Controller Interface card is to replace each card in turn with a known operational card.
- An additional check to the Controller card is to ensure that the 8 MHz clock signal is present.
- If there are no spare boards available then the bus lines should be viewed to check for correct operation.

Step 11:

Need to replace the LED.
This involves a similar procedure to that for replacing the filament lamps.

- Follow the instructions in Chapter 4 Section 5 as far as paragraph 12.
- The key panels are now exposed to enable access. Take off the bezel surrounding the key button, this just pulls away from the key base. Remove the button containing the legend.
- Desolder the LED from the back of the Keyboard PCB.
- Note carefully the orientation of the LED and then pull out from the front of the Keyboard PCB.
- Replace with a new rectangular red LED, part number MEC 165.922.08, ensuring that it is in the same orientation as the original.
- Solder the legs of the LED on the back of the Keyboard PCB.
- Replace the legend button and then the bezel.
- Continue with the procedure given in Chapter 4 Section 5 from paragraph 17.

Step 16:

The Reference Module generates several of the main clock signals i.e. those for the ADC, DSP, DAC/Sequencer and the Synthesiser Modules. Apparent faults in any of these modules could originate in the Reference Module. Be sure to check that the clock signals are all available from the Reference Module by typically 500ms after power-up. The clock signals to the DSP come from the DAC/Sequencer board, therefore a failure on the DAC/Sequencer board can cause DSP failures.

NOTE . . . .
The DAC/Sequencer BITE Test is inoperative (forced to give PASS message) therefore DSP failures on both boards could indicate a DAC/Sequencer failure.

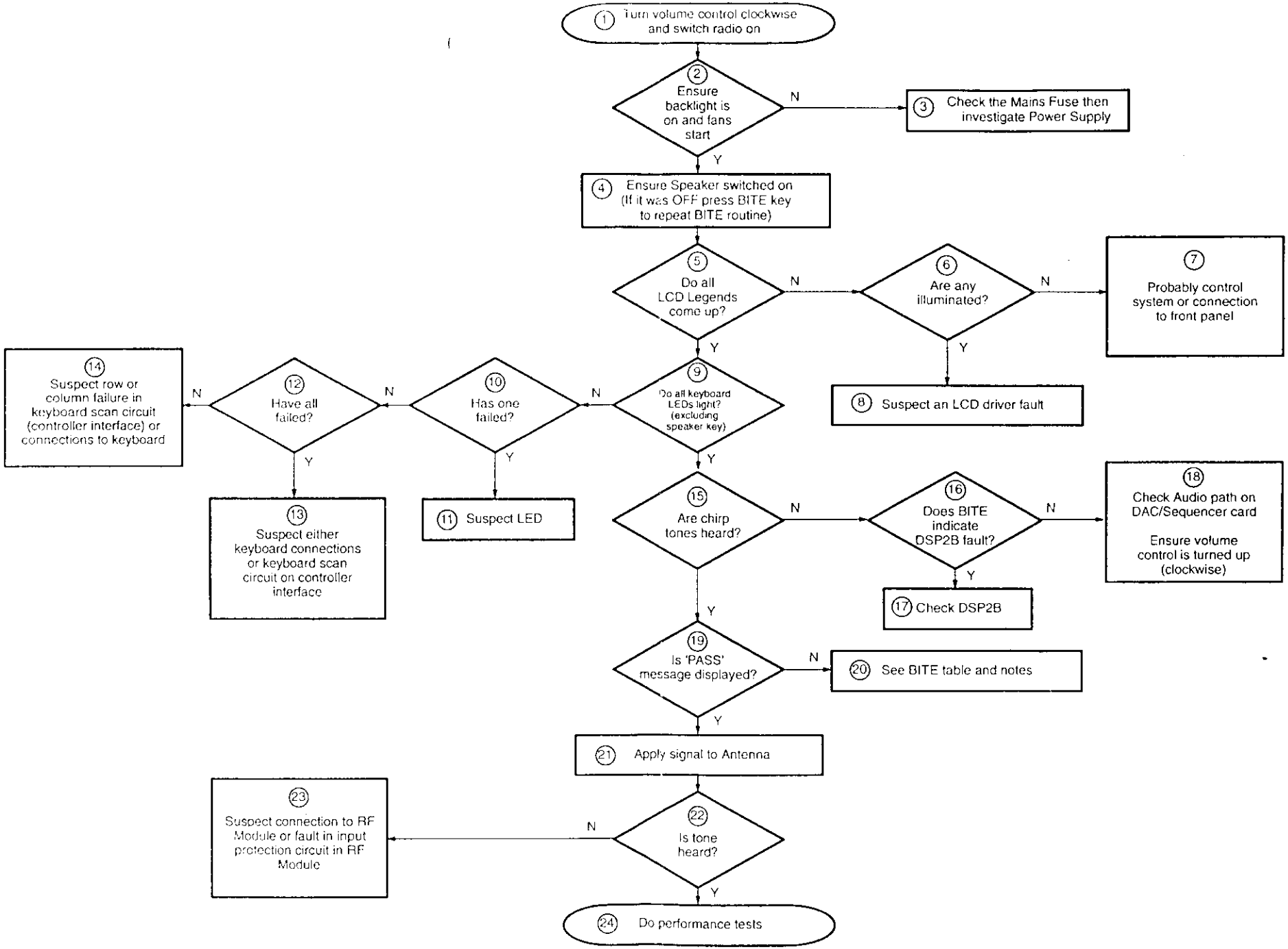


Figure 1 Power-Up Flow Diagram

Step 18:

To check the audio path on the DAC/Sequencer board refer to the fault finding section of Chapter 6.11.

Step 21:

To apply a signal to the antenna input, connect a signal generator to the antenna socket on the back of the radio. Set the signal generator to 4950 kHz and -40dBm. Set the radio to 4950 kHz, CW mode with bandwidth of 3 kHz and BFO of -0.8 kHz. An 800 Hz tone should be heard and the RF level meter should typically display about 60–70dBµV (i.e. 7 segments illuminated) and the AF meter should indicate full scale.

Step 23:

Having verified earlier that the audio path of the radio is functional and there are no faults indicated from the BITE test, then the only part not tested is the antenna connection to the RF Module. It can easily be verified that the signal path after the RF protection circuit in the RF Module is functional. With reference to the RF Module block diagram in Chapter 6.1 a test signal is injected at the 'FROM SO' point.

- Switch off the radio and remove the lid.
- Remove the link from the Sub-Octave Filter backplane connector and connect the backplane test lead (the coaxial lead with the Cambridge insert) to Pin A1.
- Set the signal generator to 4950 kHz and -40dBm, switch on the radio.
- After BITE has been completed set the radio to CW mode with a 3 kHz bandwidth and a BFO of -0.8 kHz and a frequency of 4950 kHz.
- An 800 Hz tone should be heard, the RF level meter should typically indicate 60–70dBµV (seven segments illuminated) and the AF meter should indicate full scale.

If the above test is positive then the fault is most probably the antenna connection to the RF Module or, failing that, in the RF protection circuitry.

Step 24:

If further confidence tests are required of the radio's functionality then performance tests can be performed. These are listed in the Test Specification given in Appendix B.

5 BITE

The STR 8212 is equipped with comprehensive BITE facilities. During power up and off-line BITE, a test signal is injected into the RF path to enable verification of the complete signal path. On -line monitoring of some functions such as the local oscillator level is provided.

5.1 On-Line Monitor

The STR 8212 is fitted with circuits to continuously monitor the operation of the receiver on-line without affecting the performance. If any of these circuits detects a fault condition then the "FAULT" legend on the right hand display panel is energised and remains energised until a successful off–line BITE test has been completed.

When the "FAULT" legend is displayed the user can interrogate the receiver to identify the area of the fault condition by operating the "BITE" key once. The response on the receiver will be to alter the frequency display to "FAIL nn" where "nn" represents the number of faulty modules identified by the off-line monitor. The user can then use the "UP" and "DOWN" keys to identify the status of all modules whether they have detected a fault or not. The format used for displaying the information is to generate messages in the frequency display of the type

"05 PASS" and "07 FAIL129"

The first 2 digit code represents the identity of the module or sub-system and is displayed in place of the Channel number (the "CHAN" legend is blanked). The final 3 digit number is the module or sub-system failure code and is arranged in the binary sequence 1, 2, 4, 8, 16, 32, 64, 128, 256. A failure code of 129 would therefore indicate 2 failures numbers 1 and 128. The failure code will always be in the range 1 to 511.

In some cases, because it is impossible to isolate a fault to a single module with 100% confidence, a failure message will be flagged against two modules. For example, a low level of 1st Local Oscillator drive will be flagged against both the RF unit and the synthesiser sub-system.

Table 1 provides a guide to module/sub-system codes, and lists the possible fault codes with corresponding descriptions. The fault codes marked * are those resulting from the on-line monitors. The other fault codes should be treated with caution as they are the stored results from the previous off-line BITE check and thus may no longer be relevant.

It is the recommended procedure that whenever "FAULT" is flagged on the display, a full off-line BITE check should be performed before fault diagnosis is attempted.

5.2 Off-Line/Power Up Tests

In addition to the on-line monitoring circuits, the STR 8212 receiver is fitted with extensive BITE circuitry to monitor the performance of the receiver both at power up and when commanded by the user. The off-line tests carried out by the BITE circuits include:

- Receiver Gain/Gain Control at various points in the received signal path
- Program and Data memory checks on the controller sub-system
- Program and Data memory checks on the DSP sub-system
- Loop round data tests on the DSP sub-system hardware
- Synthesiser locking and tuning characteristics over the whole frequency band
- ADC self test routines

Full off-line BITE testing will be performed at power up but can be selected by the user. If no "FAULT" legend is being displayed, a single operation of the "BITE" key invokes the full BITE sequence. However, if the "FAULT" legend is being displayed a double operation of the "BITE" key is required. The "BITE" sequence will return either a "PASS" or a "FAIL nn" message in the frequency display where "nn" refers to the number of failed modules. As in the case of the on-line monitoring, the user can use the "UP" and "DOWN" keys to scan the list of indicated faults.

Table 1 provides a guide to module/sub-system codes and lists the possible fault codes with corresponding descriptions. Interpretation of these codes is explained in Paragraph 5.1.

Table 1 BITE FAULT CODES

Module Sub-System Identity	Module Description	Fault Identity/Description
01	Controller Sub-System	1 DSP Interrupt error 2 IEEE Interface error 4 IEEE Receive Overflow error 8 MFP Timer fault 16 RAM Checksum fault at Power Up 32 RS232 Interface fault 64 Software Buffer error 128 Low EPROM fault 256 High EPROM fault
02	DSP Sub-System	1 to 32 Software incompatibility * 64 DSP Buffer fault
03	DAC Sequencer	1, 2, 4, 8, 16, 32, 64 not used 128 Fault 256 Module not tested
04	Digital Filter Part of ADC Module	1 Failed chip self test 2, 4, 8, 16, 32, 64 not used 128 Fault 256 Module not tested
05	ADC Module	1, 2, 4, 8, 16, 32, 64 not used 128 Fault with analogue chip 256 Module not tested
06	IF Module	*1 2nd Local Oscillator drive low 2 1st IF Attenuator slope incorrect 4 1st IF Attenuator characteristic shifted 8 2nd IF fault 16, 32, 64 not used 128 1st IF fault 256 Module not tested
07	RF Module	*1 RF Fuse blown *2 1st Local Oscillator drive low 4 RF Attenuator range/control faulty 8 RF frequency response faulty 16, 32, 64 not used 128 RF fault 256 Module not tested
08	Sub-Octave Filter Module (if fitted)	1 Module not fitted 2 Module fault, 1 Band 4 Module fault, several Bands 8 Module fault, all Bands 16, 32, 64, 126 not used 256 Module not tested

TABLE 1 BITE FAULT CODES (Contd)

Module Sub-System Identity	Module Description	Fault Identity/Description
09	Synthesiser Sub-System	*1 1st Local Oscillator out of lock *2 2nd Local Oscillator out of lock *4 Reference Oscillator out of lock *8 1st Local Oscillator drive low *16 2nd Local Oscillator drive low 32 Band 1 Tuning Curve faulty 64 Band 2 Tuning Curve faulty 128 Band 3 Tuning Curve faulty 256 Band 4 Tuning Curve faulty Refer to Note 3
10	PSU Sub-System	*1 Digital Power Supply Module faulty *2 Analogue Power Supply Module faulty 4, 8, 16, 32, 64, 128, 256 not used
11	DSP Board 1	1 RAM/SSI DSP1A fault 2 LO EPROM DSP1A fault 4 MID EPROM DSP1A fault 8 HI EPROM DSP1A fault 16 RAM SSI DSP1B fault 32 LO EPROM DSP1B fault 64 MID EPROM DSP1B fault 128 HI EPROM DSP1B fault
12	DSP Board 2	1 RAM/SSI DSP2A fault 2 LO EPROM DSP2A fault 4 MID EPROM DSP2A fault 8 HI EPROM DSP2A fault 16 RAM SSI DSP2B fault 32 LO EPROM DSP2B fault 64 MID EPROM DSP2B fault 128 HI EPROM DSP2B fault
13,14	SPARE	
15	Software Version	The version number in the range 0.00 to 9.99 is displayed in place of the BFO setting and the "BFO" legend is blanked

NOTES . . . .

1. 'Module not tested' will be flagged for the modules shown if the 1st or 2nd Local Oscillator is reported as being out of lock at the time of the BITE check.
2. Fault codes marked * are the results of on-line monitoring tests.
3. 1st Local Oscillator can be checked by connecting a Spectrum Analyser to LO1 output and ensuring that the output frequency tracks the tuned frequency of the receiver with an offset of 70.05 MHz. Ensure not in LSB or USB modes.

6 ADDITIONAL NOTES TO BITE CODE TABLE

6.1 RF Fuse

If the BITE code '07 FAIL 1' occurs then the RF fuse has blown. Replace the RF fuse as follows:

- Switch off the radio and remove the lid.
- Remove the retaining screw from the RF Module and ease the module out of the radio.
- Remove the lid.
- Unclip the fuse and replace with a serviceable item. The fuse is a PC-TRON Subminiature 500mA BUSSMAN BK/PCC/0.5A.
- Replace the lid on the RF Module and refit the module into the backplane connector and secure with retaining screw.
- Fit the lid to the radio.

6.2 Multiple Module Failures

Due to the nature of the BITE tests which are dependent upon the sensing of signals at various points throughout the radio, it is not always possible to identify the exact position of the fault. In these instances several possible points of failure are indicated which lead to multiple module BITE failure indications.

6.2.1 DSP Module Failures

DSP failures should always be addressed first as the DSP sub-system is a key test point where level sensing occurs for some of the other module tests. If a DSP Interrupt Error is indicated in Module 1 then this is a good guide that the DSPs have not powered up correctly and the fault lies with the clock signals prior to the DSP boards. If a DSP Interrupt Error is not indicated then the fault is likely to be on the DSP boards; carefully check that the DSP boards are in the correct positions.

6.2.2 IF Module Failures

A short circuit on the output of the IF Module will cause not only a 2nd IF fault but will also prevent signal levels during the 1st IF attenuator tests from being measured. Therefore, any diagnosed faults in the signal path after the IF attenuator should be rectified first.

NOTE . . . .
The user should not look for faults in the IF attenuators if a 2nd IF fault is indicated.

6.2.3 Signal Path Fault

A fault in the main signal path between the Antenna input and the DSP boards can be indicated during off-line BITE by a group of module failures. These can be a combination of the following:

- 04 FAIL 128 ADC Module
- 05 FAIL 128 ADC Module
- 06 FAIL 128 or 136 IF Module
- 07 FAIL 128 RF Module

The reason for this is if a signal path failure occurs in the RF module for example, no test signal is available for ADC testing.

A series of tests can be performed with the aid of a signal generator and an oscilloscope which can assist in isolating the fault to a particular module.

TEST ONE

The following test decides whether the fault lies in the analogue or digital section of the radio by injecting a test signal immediately prior to the ADC Module, bypassing the main analogue signal path. This test replaces the IF Module with a test signal at point 'SIG1' shown in the IF Module block diagram in Chapter 6.2.

1) Switch off the radio and remove the lid.

2) Remove the IF Module and fit the IF extender which includes the BNC socket.

3) Connect a signal generator set to 0.18V RMS and 50 kHz (the 2nd IF centre frequency) to the BNC socket.

4) Switch the radio on and at the end of BITE (ignore any BITE failures at this point) set the radio to CW mode with a 3 kHz bandwidth and a BFO of -0.8 kHz and a frequency of 4950 kHz (operating frequency is not important for this test).

5) An 800 kHz tone should be heard. The RF level meter on the front panel should typically read 60–70dBμV (seven segments illuminated) and the AF meter should indicate full scale.

6) If there is no clean, audible tone at approximately 800 Hz and an incorrect RF level reading then there is a fault in the digital sub-system. If no BITE faults were indicated for the rest of the digital sub-system then replace the ADC Module.

7) If there is an audible tone then the digital sub-system is serviceable. Proceed to Test Two.

TEST TWO

The aim of this test is to verify the operation of the IF Module to ensure that it is producing a 2nd IF signal at the correct frequency and of approximately the correct level. With reference to the IF Module block diagram in Chapter 6.2, the RF Module is replaced with a test signal at the IF input and 'SIG1' output is monitored on an oscilloscope.

1) Switch off the radio and refit the IF Module on to the extender. Connect the IF extender BNC socket to an oscilloscope.

2) Remove the RF Module. Fit the backplane test lead (see Appendix A) between pin A4 of the RF backplane connector and the signal generator.

3) Set the signal generator to -33dBm and 70.05 MHz and switch the radio on.

4) At the end of BITE (ignore any BITE failures at this point) set the radio to CW mode with a 3 kHz bandwidth and a BFO of -0.8 kHz and a frequency of 4950 kHz (operating frequency is not important for this test).

NOTE . . . .
Ignore the 'RF MUTE', 'HIGH' and '⚠' legends if they are lit.

5) The oscilloscope should typically display a 0.6V pk-pk 50 kHz sine wave. If this is present the IF Module is serviceable and there is a fault in the RF Module, replace the RF Module.

6) If the sine wave is not present at the correct level there is a fault in the IF Module, replace the IF Module.

7) If the sine wave is present at this point remove the Interface Module (which will stop the radio muting the audio output) and ensure that an 800 Hz audio output is obtained.

Chapter 4

ROUTINE MAINTENANCE

1 INTRODUCTION

The constituent parts of the STR8212 HF Receiver are manufactured to professional standards from high quality components and materials.

The use of 'solid state' technology in circuit design enables prolonged, maintenance free operation from the receiver in a wide range of environmental conditions.

The modular design of the receiver ensures trouble free operation of the unit. The only routine maintenance requirement is the periodic replacement of the units cooling fans and replacement of defective filament lamps on the Display Driver PCB.

2 COOLING FANS

The receiver is fitted with two axial cooling fans on the rear panel of the unit. One is located in the RF/IF Synthesiser section, the other being located in the digital circuitry section of the receiver. A simplified layout diagram of the interior of the receiver is given in Figure 1 on the following page which shows the two fans and the direction of air flow in the receiver.

Air is drawn into the unit via the two cooling fans in the rear of the receiver. The cool air is passed over the modules of the receiver and is blown out through a ventilator on the bottom face of the receiver.

The component part number for the co-axial fans is COMAIR-ROTRON FL12A306/032269. These fans are rated at 12 volt, 1.6 watts and have 55mm fixing centres. The fans have no replacement parts and must be exchanged if defective. In most cases, the fans will provide indication of failure by becoming rough or extremely noisy in operation. The method of removal and replacement of the fans is given in paragraphs 3 and 4.

3 RF SECTION FAN REMOVAL AND REPLACEMENT

Removal and replacement of this fan is relatively simple and requires a minimum of dismantling of the receiver with no requirement for the use of specialised tools.

3.1 Removal of RF Section Fan

The procedure to remove the fan is as follows:

(1) Switch OFF the unit by means of the front panel ON/OFF switch.

(2) Disconnect all plugs and sockets from the rear of the unit noting their positions for reconnection. Label any plugs/sockets not annotated.

WARNING

THE UNIT WEIGHS APPROXIMATELY 15KG. SUITABLE PRECAUTIONS MUST BE TAKEN WHEN REMOVING THE UNIT FROM THE EQUIPMENT RACK TO PROTECT BOTH THE MAINTAINER AND THE EQUIPMENT.

(3) If unit is rack mounted, remove from the rack and place on a suitable workbench.

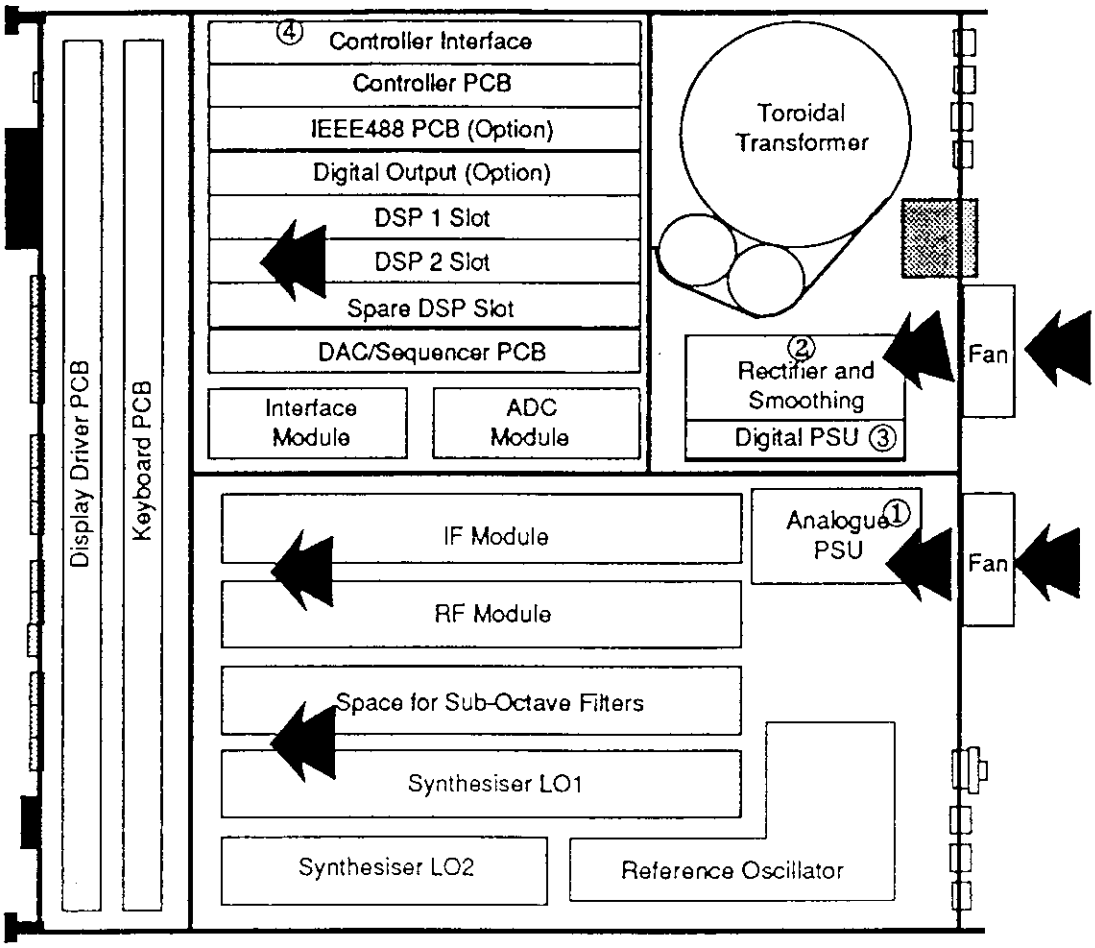


Figure 1 - Internal Layout and Air Flow Diagram

WARNING

WHEN THE TOP COVER IS REMOVED, DANGEROUS VOLTAGES ARE PRESENT IF THE UNIT IS CONNECTED TO THE SUPPLY. EVEN WITH POWER DISCONNECTED, A PERIOD OF TWO TO THREE MINUTES SHOULD BE LEFT TO ALLOW CAPACITORS TO DISCHARGE BEFORE WORKING NEAR THE POWER SUPPLY BOARD.

(4) Remove the units top cover by releasing the eight screws and lifting the cover plate clear.

(5) With reference to Figure 1 item annotated (1), release the plug in the top corner of the Analogue PSU to allow access to the fan wiring.

(6) On the rear of the fan, release the four screws holding the fan and guards in place. Note that the inside fixing nuts of the fan are locked with thread locking compound and need to be held with a ring spanner to allow the screws to be removed.

(7) Unsolder the two wires from the feed-through filters taking note of their position for reconnection, (red lead to No. 5, black lead to No. 6).

(8) The fan, internal guard and wire can now be lifted clear.

3.2 Replacement of RF Section Fan

The procedure to replace the fan is as follows:

(1) Ensure that replacement unit is serviceable by connecting across a 12 volt/0.5A dc supply.

(2) Check the direction arrows on the body of the fan to ensure that unit is fitted to provide flow **to** the receiver **from** the outside.

(3) Connect the red and black leads to the panel feed-through filter pins on the chassis; red lead to No. 5, black lead to No. 6, and resolder.

(4) Refit the four screws through the outer guard and into the fan.

(5) Ease the fan into position with the four screws going through the back-panel grommets.

(6) Refit the inner fan-guard ensuring that the leads are fed through it and do not obstruct the fan blades.

(7) Secure with the plain washers and nuts, ensuring that the threads are coated with screw locking compound. The screws should be lightly tightened to a torque setting of 0.5Nm so as not to over-compress the grommets.

(8) Refit the connector in the top corner of the Analogue PSU.

(9) Refit the units top cover and secure in place using the eight screws and washers previously removed.

(10) Refit the unit in the rack and reconnect all plugs and sockets previously disconnected.

(11) Switch on and check for correct operation of both the fan and the receiver.

4 DIGITAL SECTION FAN REMOVAL AND REPLACEMENT

Removal and replacement of this fan is not a simple task and requires the use of tools not part of a normal tool kit.

4.1 Removal of Digital Section Fan

The procedure to remove the fan is as follows:

(1) Switch OFF the unit by means of the front panel ON/OFF switch.

(2) Disconnect all plugs and sockets from the rear of the unit noting their positions for reconnection. Label any plugs/sockets not annotated.

WARNING

THE UNIT WEIGHS APPROXIMATELY 15KG. SUITABLE PRECAUTIONS MUST BE TAKEN WHEN REMOVING THE UNIT FROM THE EQUIPMENT RACK TO PROTECT BOTH THE MAINTAINER AND THE EQUIPMENT.

(3) If the unit is rack mounted, remove from the rack and place on a suitable workbench.

WARNING

WHEN THE TOP COVER IS REMOVED, DANGEROUS VOLTAGES ARE PRESENT IF THE UNIT IS CONNECTED TO THE SUPPLY. EVEN WITH POWER DISCONNECTED, A PERIOD OF TWO TO THREE MINUTES SHOULD BE LEFT TO ALLOW CAPACITORS TO DISCHARGE BEFORE WORKING NEAR THE POWER SUPPLY BOARD.

(4) Remove the units top cover by releasing the eight screws and lifting cover clear.

(5) Disconnect the large connector on the Rectifier/Smoothing PCB, (annotated (2) on Figure 1), and the connector on the Digital PSU (annotated (3)).

(6) On the rear of the fan, release the four screws holding the fan and guards in place. Note that the inside fixing nuts of the fan are locked with thread locking compound and need to be held with a ring spanner to allow the screws to be removed.

(7) Note that the wiring for this fan is made via the connector on the Rectifier/Smoothing PCB. To make connections to these sockets requires new contacts and a specialised removal tool which is not part of a normal test kit. The alternative method is to break into the cable run to the motor and make solder connections. These are to be suitably protected against accidental short circuit with heat shrink sleeving or similar.

(8) Cut the feed to the fan approximately 75mm from the wiring loom. Lift fan clear of the unit.

4.2 Replacement of Digital Section Fan

The procedure to replace the fan is as follows:

(1) Ensure that the replacement unit is serviceable by connecting across a suitable 12 volt/0.5A dc supply.

(2) Check the direction arrows on the body of the fan to ensure that unit is fitted to provide flow to the receiver from the outside.

(3) Refit the four screws through the outer guard and into the fan.

(4) Ease the fan into position with the four screws going through the back-panel grommets.

(5) Refit the inner fan guard ensuring that the leads are fed through it and do not obstruct the fan blades.

(6) Secure with the plain washers and nuts, ensuring that the threads are coated with screw locking compound. The screws should be lightly tightened to a torque of 0.5Nm so as not to over-compress the grommets.

(7) Cut off any excess wire from the fan leads and solder to the wires from the wiring loom. Cover joint with heat shrink sleeving and seal.

(8) Reconnect the large connector on the Rectifier/Smoothing PCB and the connector on the Digital PCB.

(9) Refit the units top cover and secure in place using the eight screws and washers previously removed.

(10) Refit the unit in the rack and reconnect all plugs and sockets previously disconnected.

(11) Switch on and check for correct operation of the fan and the receiver.

5 FILAMENT LAMPS

There are six filament lamps located on the Display Driver PCB. These lamps are hard wired to the PCB. The component part number for all lamps is VCH LTD. G1 7219 12V, 0.72W, 1.9 LUMEN. These are replaceable items but it does require a fair degree of dismantling to obtain access to these lamps. This should not be attempted by unskilled personnel as damage to the receiver circuitry can occur if the relevant safety precautions are not taken. The procedure to remove and replace defective filament lamps is given in the following paragraphs.

(1) Switch OFF the unit by means of the front panel ON/OFF switch.

(2) Disconnect all plugs and sockets from the rear of the unit noting their positions for reconnection. Label any plugs/sockets not annotated.

WARNING

THE UNIT WEIGHS APPROXIMATELY 15KG. SUITABLE PRECAUTIONS MUST BE TAKEN WHEN REMOVING THE UNIT FROM THE EQUIPMENT RACK TO PROTECT BOTH THE MAINTAINER AND THE EQUIPMENT.

(3) If the unit is rack mounted, remove from the rack and place on a suitable workbench.

WARNING

WHEN THE TOP COVER IS REMOVED, DANGEROUS VOLTAGES ARE PRESENT IF THE UNIT IS CONNECTED TO THE SUPPLY. EVEN WITH POWER DISCONNECTED, A PERIOD OF TWO TO THREE MINUTES SHOULD BE LEFT TO ALLOW CAPACITORS TO DISCHARGE BEFORE WORKING NEAR THE POWER SUPPLY BOARD.

(4) Remove the units top cover by releasing the eight screws and lifting cover clear.

(5) Using a 4mm Allen key, release and remove the four bolts holding the handles and front panel to the frame of the unit.

CAUTION

The circuitry used on the PCB's utilises CMOS integrated circuits. The relevant precautions **must** be taken to avoid damage to CMOS circuitry when any board is removed from the receiver.

(6) With reference to Figure 1, locate the Controller Interface PCB. On the Controller Interface PCB, pull handles up and release the PCB from its socket on the Digital Backplane PCB. Lift the PCB clear and lay on a non static surface.

(7) Obtain access to the connectors on the Digital Backplane PCB (annotated item 4 on Figure 1) and disconnect the two sockets that feed the complete front panel assembly.

(8) From the top of the unit at the front, disconnect the connector from the front panel ON/OFF switch.

(9) Remove IF Module by removing its retaining screw and gently pulling it clear of the unit. This allows access to the screw holding the rigidity spacer to the chassis. Remove this screw.

(10) Note the **exact** layout of the ribbon cable for re-fitting then ease the front panel forward and lay it on its face in front of the unit. The two ribbon cables may need to be eased through the aperture in the main chassis to facilitate this. Do not remove the earth wire from the main chassis unless the keyboard is going to be moved away from the rest of the radio.

(11) Release and remove the ten nuts and washers, (including the rigidity spacer), that hold the Keyboard PCB to the main frame of the front panel.

(12) Lift the Keyboard PCB clear of the ten studs and ease it back over the Display Driver PCB. **DO NOT** move the Keyboard PCB too far as the wires from the tuning control may be damaged. Access to the six filament lamps on the Display Driver PCB is now possible.

(13) Carefully snip the leads on the defective filament lamp and lift lamp clear from the Display Driver PCB.

(14) Unsolder and remove the two filament lamp wires from the Display Driver PCB.

(15) Carefully bend the wires of the new filament lamp to shape and trim off any excess wire.

(16) Fit the filament lamp into the appropriate hole and solder the two wires in place.

(17) Carefully ease the Keyboard PCB forwards back onto the ten studs. Pay particular attention to the foam dust seal around the LCD display to ensure that it does not get trapped by the keyboard. Now check that no wires have been trapped, particularly those on the right of the Keyboard PCB (pink wires).

(18) Replace the ten nuts and washers that hold the Keyboard PCB to the main frame and tighten evenly to just pinch them up.

(19) Check the operation of all the front panel pushbutton switches, ensuring that they click ON and OFF correctly. If any are stiff or do not operate correctly, ease the ten nuts and then retighten.

(20) When all keys operate correctly, torque to 0.7Nm the ten nuts that hold the Keyboard PCB to the main frame. **DO NOT** overtighten these nuts as damage to the PCB can occur. Recheck the operation of all front panel keys.

(21) If the earth wire was disconnected, reconnect it.

(22) Reconnect the connector from the front panel ON/OFF switch, the panel will need to be vertical for this.

(23) Ease the ribbon cables back through the aperture in the main chassis taking care to maintain the layout noted in paragraph (10) above.

(24) Refit the front panel to the chassis ensuring that no cables are trapped, particularly by the speaker.

Note: It is easier to ease the speaker end of the front panel in first. Do not force the front panel at the ON/OFF switch end as damage to the PCB will occur.

(25) Replace the screw for the rigidity spacer but do not tighten yet. Replace the front handles and secure in place with the four Allen key bolts previously removed.

(26) Reconnect the two connectors on the Digital Backplane PCB, ensuring that they are fully pushed home and locked in place.

(27) Refit the Interface PCB in its slot and push in place firmly.

(28) Tighten the screw for the rigidity spacer and replace IF module, securing it with its retaining screw.

(29) Refit the units top cover and secure in place using the eight screws and washers previously removed.

(30) Refit the unit in the rack and reconnect all plugs and sockets previously disconnected.

(31) Switch on and check for correct operation of the receiver.

Chapter 5

REMOVAL AND REFITTING OF SUB ASSEMBLIES

1 INTRODUCTION

This chapter of the manual details the removal and replacement procedures for the sub assemblies of the receiver. Replacement procedures are given with reference to the General Assembly drawing that is given in Chapter 6 of this manual and the simplified mechanical layout drawing, Figure 1 shown overleaf.

The unit should be disconnected from the power supply when effecting sub assembly replacement. When this is not desirable, eg when fault finding on the unit, the following warning and caution must be heeded.

WARNING

WHEN THE TOP COVER IS REMOVED, DANGEROUS VOLTAGES ARE PRESENT IF THE UNIT IS CONNECTED TO THE SUPPLY. EVEN WITH POWER DISCONNECTED, A PERIOD OF TWO TO THREE MINUTES SHOULD BE LEFT TO ALLOW CAPACITORS TO DISCHARGE BEFORE WORKING NEAR THE POWER SUPPLY BOARD.

CAUTION

Removal of the PCBs with power connected can damage FETs and Integrated Circuits. Remove power before removing PCBs

Faulty sub assemblies must be replaced with **known** serviceable items which carry a serviceable label. As the PCBs are multi-layered, it is not recommended that components on the boards are changed. Defective boards are to be returned for repair.

Sub assembly replacement procedures are detailed under the following headings:

Removing the Unit from the Rack	Paragraph 2
Replacing the Unit in the Rack	Paragraph 3
Removing and Replacing the Top Cover	Paragraph 4
Analogue Modules	Paragraph 5
Digital PCB's	Paragraph 6
Rectifier/Smoothing and Digital PSU Assembly	Paragraph 7
Analogue PSU Assembly	Paragraph 8
Front Panel Assembly	Paragraph 9
Backplane Removal and Refitting	Paragraph 10

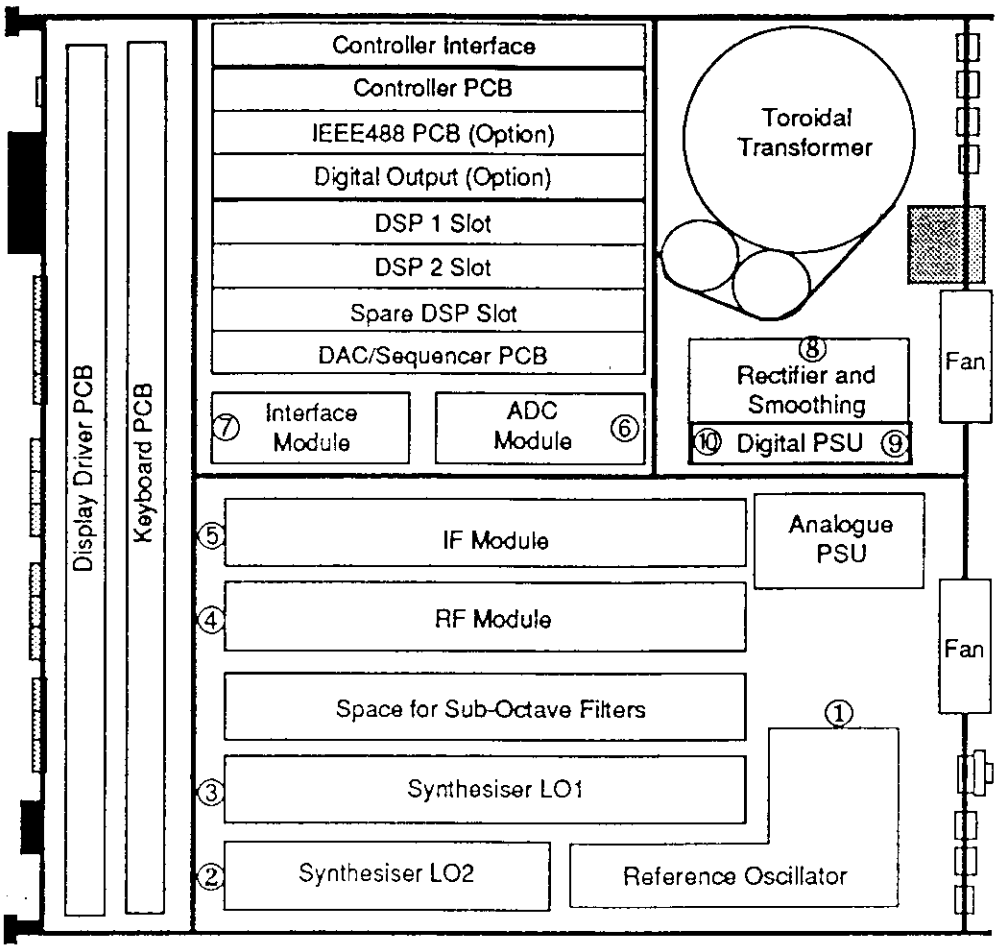


Figure 1 - Internal Layout Diagram

2 REMOVING THE UNIT FROM THE RACK

The procedure to remove the unit from the rack is as follows:

(1) Switch OFF the unit by means of the front panel ON/OFF switch.

(2) Disconnect all connectors from the rear of the unit noting their positions for reconnection. Label any connectors not annotated.

(3) If the receiver is fitted on runners in the equipment rack, release and remove the four securing screws that hold the unit to the rack.

WARNING

THE UNIT WEIGHS APPROXIMATELY 15KG. SUITABLE PRECAUTIONS MUST BE TAKEN WHEN REMOVING THE UNIT FROM THE EQUIPMENT RACK TO PROTECT BOTH THE MAINTAINER AND THE EQUIPMENT.

(4) If the receiver is **not** fitted on runners in the equipment rack, support the unit and then release and remove the four securing screws that hold the unit in the rack.

(5) Lift the unit onto a worksurface or bench.

3 REPLACING THE UNIT IN THE RACK

(1) Lift the unit into the rack and rest it on runners, if fitted.

(2) Refit the four securing screws that hold the unit in the rack.

(3) Reconnect all plugs and sockets on the rear panel of the unit.

(4) Switch ON and check for correct operation of the receiver.

4 REMOVING AND REPLACING THE TOP COVER

To gain access to any circuitry within the receiver, its top cover has to be removed. The procedure to remove and refit the cover is as follows:

4.1 Removing Top Cover

(1) Remove unit from the rack as detailed in Paragraph 2.

WARNING

WHEN THE TOP COVER IS REMOVED, DANGEROUS VOLTAGES ARE PRESENT IF THE UNIT IS CONNECTED TO THE SUPPLY. EVEN WITH POWER DISCONNECTED, A PERIOD OF TWO TO THREE MINUTES SHOULD BE LEFT TO ALLOW CAPACITORS TO DISCHARGE BEFORE WORKING NEAR THE POWER SUPPLY BOARD.

(2) Remove the eight screws holding the cover in place and lift clear.

4.2 Replacing Top Cover

(1) Replace the top cover and secure in place with eight screws previously removed.

5 ANALOGUE MODULES

The following modules all use the same method for removal and re-fitting:

- Reference Oscillator
- Synthesiser LO1
- Synthesiser LO2
- RF Module
- IF Module
- Interface Module
- ADC Module

Note: Special care must be taken with the ADC Module as this has a loose cable connecting it to the digital backplane as well as the fixed connector. When removing this module, it should be disconnected from the fixed connector as detailed in Paragraph 5.1 (1) to (5). Next ease the module slowly away from the unit until the connector on the base is accessible and disconnect. To replace the ADC Module it is easier to first remove the DAC/Sequencer Board as described in Paragraph 6. Reconnect the loose cable and refit the unit as normal. Check the opposite end of the loose cable to ensure that it has not pulled free from its connector, then carefully replace the DAC/Sequencer Board ensuring that it does not catch on the cable.

5.1 Removing Modules

The procedure to remove the required module is as follows:

(1) Remove the unit from the rack as detailed in Paragraph 2.

(2) Remove the top cover as detailed in Paragraph 4.1.

(3) With reference to Figure 1, locate the required module.

(4) Release and remove the module securing screw.

(5) Gently ease the module forwards and backwards to release the connectors at the base of the unit.

(6) Use the plastic handle on top of the module to pull it clear.

5.2 Replacing Modules

The procedure to replace the required module is as follows:

(1) Ensure that the replacement unit carries a serviceable label.

(2) Carefully place the module into the multiple connector in the RF Backplane Assembly.

(3) Use gentle pressure to push the connectors together. If the connectors will not easily connect, remove and check that they are lined up and are undamaged.

(4) When correctly fitted, replace module securing screw.

(5) Replace the top cover as detailed in Paragraph 4.2.

(6) Replace the unit in the rack as detailed in Paragraph 3.

6 DIGITAL PCB's

The following PCB's all use the same method for removal and re-fitting:

- DAC/Sequencer PCB
- Digital Signal Processing Board PCB 1
- Digital Signal Processing Board PCB 2
- Digital Output PCB
- IEEE 488 PCB
- Controller PCB
- Controller Interface PCB

Note: Care must be taken with the DAC/Sequencer PCB to ensure that it does not catch on the adjacent cabling.

Note: Optical fibre connectors on the Digital Output PCB are push fit. Ensure that cables are clearly marked. When removing, pull firmly and smoothly trying to bend the cable as little as possible.

6.1 Removing PCB's

The procedure to **remove** the required PCB is as follows:

(1) Remove the unit from the rack as detailed in Paragraph 2.

(2) Remove the top cover as detailed in Paragraph 4.1.

(3) With reference to Figure 1, locate the required PCB.

> **CAUTION**
>
> Removal of the PCBs with power connected can damage FETs and Integrated Circuits. Remove power before removing PCBs

(4) Use the two white extraction levers on the top of the PCB to lift the PCB out of the connector on the Digital Backplane Assembly.

(5) Lift the required PCB clear and place on an anti-static surface.

6.2 Refitting PCB's

The procedure to **refit** the required PCB's is as follows:

(1) Ensure that the replacement PCB carries a serviceable label.

(2) For the IEEE 488 PCB, Controller PCB and the Controller Interface PCB, refer to Paragraph 6.3, 6.4 or 6.5 as appropriate before continuing.

(3) Place the PCB in its correct slot, ensuring that the white extraction levers are flat on top of the PCB.

Note: The sockets on the Digital Backplane Assembly are the same, (with the exception of the Controller Interface PCB). Take care to ensure that the PCBs are not inadvertently fitted in the wrong socket.

(4) Use firm hand pressure on top of the PCB to make the connector on the Digital Backplane Assembly.

(5) Replace the top cover as detailed in Paragraph 4.2

(6) Replace the unit in the rack as detailed in Paragraph 3.

6.3 IEEE 488 PCB

The IEEE 488 PCB is an end user specified option which is configured by switches on the PCB. When a PCB is changed, the settings of the new PCB should be set to the same as the PCB it replaces. The procedure is as follows:

(1) Lay the old and replacement unit side by side and locate the 8 DIL switches, Figure 2 overleaf refers.

(2) Set the DIL switches on the replacement unit to the same as the old unit to retain the same hardware address.

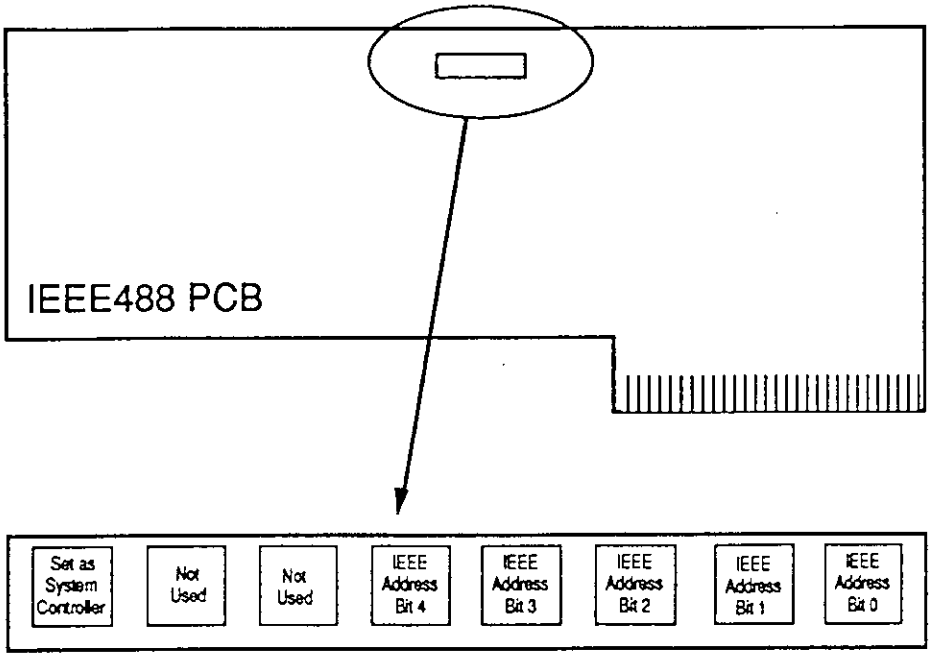


Figure 2 - IEEE 488 Switch Settings

6.4 Controller PCB

The Controller PCB has link settings which need to be checked when the PCB is changed. Links are to be set to the same as the PCB it replaces by removing link units from old to new PCB. The procedure is as follows:

(1) Lay the old and replacement unit side by side and locate the two link connections, LK1 and LK2, Figure 3 shown below refers.

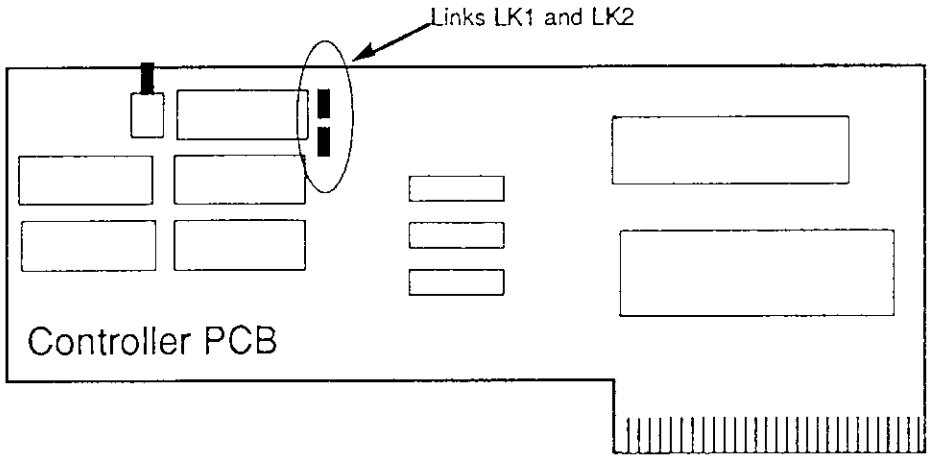


Figure 3 - Controller PCB Link Connections

(2) If the replacement PCB is **not** fitted with links LK1 and LK2, remove from old PCB and fit to new PCB.

6.5 Controller Interface PCB

The Controller Interface PCB has a link setting and DIL switches which need to be configured when the PCB is changed. The DIL switches set the Baud Rate of the board and they should be set to the same as the PCB it replaces. Similarly, the link should be set to the same as the PCB it replaces.The procedure is as follows:

(1) Lay the old and replacement unit side by side and locate Link connector 1, Figure 4 refers.

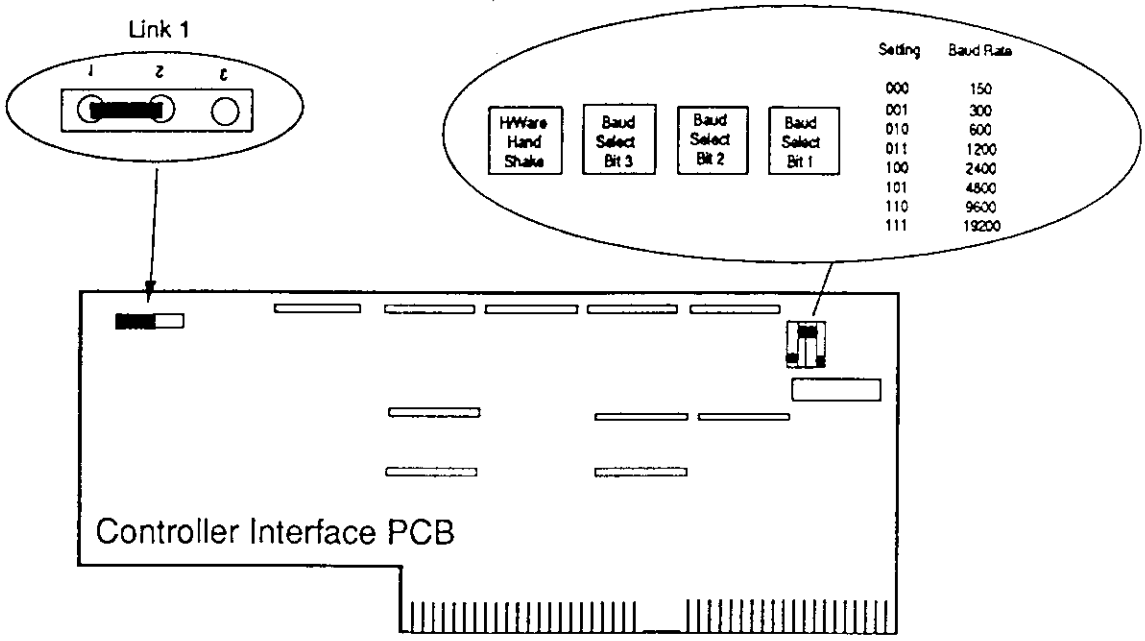


Figure 4 - Controller Interface PCB

(2) If the replacement PCB is **not** fitted with Link 1, remove from old PCB and fit to new PCB. If link is incorrectly fitted, fit to correct position.

(3) Locate the 4 DIL switches, Figure 4 refers.

(4) Set the DIL switches on the replacement unit to the same as the old unit to retain the same RS232 Baud Rate.

7 RECTIFIER/SMOOTHING AND DIGITAL PSU ASSEMBLY

This assembly consists of two parts, the Rectifier Smoothing PCB and the Digital PCB. These are replaced as a complete assembly.

The procedure to **remove** the assembly is as follows:

(1) Remove the unit from the rack as detailed in Paragraph 2.

(2) Remove the top cover as detailed in Paragraph 4.1.

> **CAUTION**
>
> Removal of the PCBs with power connected can damage FETs and Integrated Circuits. Remove power before removing PCBs

(3) Disconnect the large connector on the Rectifier/Smoothing PCB (annotated ⑧ on Figure 1), and two connectors on the Digital PCB (annotated ⑨ and ⑩ on Figure 1).

(4) Using a suitable nut driver, release and remove the three nuts and washers on the Rectifier/Smoothing PCB. These are located as follows:

- between C1/C2/D1
- between C2/C5/D2
- between C4/D5/Header

(5) Using a suitable nut driver, release and remove the two nuts and washers at the rear of the Digital PCB.

(6) Remove the screw and nylon washer at the top of the Digital PSU Board.

(7) Carefully lift out the Rectifier/Smoothing and Digital PSU as a complete assembly and place on an anti-static surface.

The procedure to **replace** the assembly is as follows:

(1) Ensure that the replacement unit carries a serviceable label.

(2) Refit the replacement assembly onto the five studs in the base of the unit.

(3) Secure assembly in place with the five nuts and washers previously removed.

(4) Secure the Digital PSU Board, with the screw, to the dividing panel ensuring that the nylon washer is between the PCB and mounting pillar.

(5) Reconnect the large connector on the Rectifier/Smoothing PCB and the two connectors on the Digital PCB.

(6) Replace the top cover as detailed in Paragraph 4.2

(7) Replace the unit in the rack as detailed in Paragraph 3.

8 ANALOGUE PSU ASSEMBLY

The Analogue PSU Assembly consists of a PCB and a heatsink complete with power transistors. The PCB, heatsink and transistors are replaced as a complete assembly.

The procedure to **remove** the assembly is as follows:

(1) Remove the unit from the rack as detailed in Paragraph 2.

(2) Remove the top cover as detailed in Paragraph 4.1.

> **CAUTION**
>
> Removal of the PCBs with power connected can damage FETs and Integrated Circuits. Remove power before removing PCBs

(3) Remove the IF Module in accordance with Paragraph 5.

(4) With reference to Figure 1, locate the Analogue PSU and disconnect the two connectors on the PCB.

(5) With reference to Figure 5 below, locate the two nuts that hold the assembly to the main frame of the receiver. Remove nuts and washers using a nut driver.

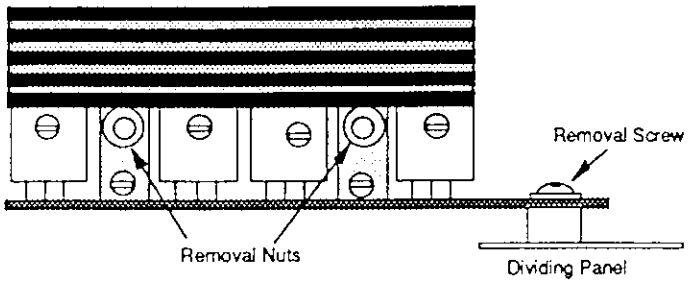


Figure 5 - Removing the Analogue PSU Assembly

(6) Remove the screw and washer in the top corner of the PCB.

(7) Lift the complete assembly upwards noting that the connector between the Analogue Assembly and the RF Backplane Assembly has to be eased gently apart.

(8) Place the assembly on an anti-static surface.

The procedure to **replace** the assembly is as follows:

(1) Ensure that the replacement unit carries a serviceable label.

(2) Refit the replacement assembly onto the two studs in the base of the unit and remake the connector between the assembly and the RF Backplane Assembly.

(3) Replace the two nuts and washers that secure the assembly to the frame.

(4) Replace the securing screw and washer to the top corner of the PCB.

(5) Reconnect the two connectors on the Analogue PCB.

(6) Replace the IF Module in accordance with Paragraph 5.

(7) Replace the top cover as detailed in Paragraph 4.2

(8) Replace the unit in the rack as detailed in Paragraph 3.

9 FRONT PANEL ASSEMBLY

The Front Panel Assembly consists of the following:

- Display Driver PCB
- Keyboard PCB
- Speaker and Tuning/Gain/Volume Controls.

The assembly is changed as a complete unit.

The procedure to **remove** the Front Panel Assembly is as follows:

(1) Remove the unit from the rack as detailed in Paragraph 2.

(2) Remove the top cover as detailed in Paragraph 4.1.

(3) Using a 4mm Allen key, release and remove the four bolts holding the handles and front panel to the frame of the unit.

CAUTION

The circuitry used on the PCB's utilises CMOS integrated circuits. The relevant precautions **must** be taken to avoid damage to CMOS circuitry when any board is removed from the receiver.

(4) Remove the Controller Interface PCB in accordance with Paragraph 6.

(5) Obtain access to the connectors on the Digital Backplane PCB and disconnect the two sockets that feed the complete front panel assembly.

(6) From the top of the unit at the front, disconnect the connector from the front panel ON/OFF switch.

(7) Remove the IF Module in accordance with Paragraph 5. Remove the screw holding the front panel rigidity spacer.

(8) Note carefully the layout of the ribbon cables for later re-assembly then ease the front panel forward and lay it on its face in front of the unit. The two ribbon cables will need to be eased through the aperture in the main chassis to facilitate this.

(9) Disconnect the earth strap between the front panel and the chassis of the receiver and lift the complete assembly clear.

The procedure to **replace** the Front Panel Assembly is as follows:

(1) Ensure that the replacement unit carries a serviceable label.

(2) Reconnect the earth cable between the front panel and the chassis.

(3) Reconnect the connector from the front panel ON/OFF switch, the panel will need to be vertical for this.

(4) Feed the two ribbon cables through the aperture in the chassis and route them to their sockets on the Digital Backplane Assembly, taking care to replace them in their previous layout.

(5) Refit the front panel to the chassis ensuring that no cables are trapped.

Note: It is easier to ease the speaker end of the front panel in first. Do not force the front panel at the ON/OFF switch end as damage to the PCB will occur.

(6) Refit the screw holding the front panel rigidity spacer but do not tighten it yet.

(7) Replace the front handles and secure in place with the four Allen key bolts previously removed.

(8) Reconnect the two connectors on the Digital Backplane PCB, ensuring that they are fully pushed home and locked in place.

(9) Tighten the rigidity spacer screw and then replace the IF Module in accordance with Paragraph 5.

(10) Refit the Controller Interface PCB in its slot and push in place firmly.

(11) Replace the top cover as detailed in Paragraph 4.2

(12) Replace the unit in the rack as detailed in Paragraph 3.

10 RF BACKPLANE REMOVAL AND REFITTING

The procedure to **remove** the RF backplane is as follows:

(1) Remove the unit from the rack as detailed in Paragraph 2.

(2) Remove the top cover as detailed in Paragraph 4.1.

CAUTION

The circuitry used on the PCB's utilises CMOS integrated circuits. The relevant precautions **must** be taken to avoid damage to CMOS circuitry when any board is removed from the receiver.

(3) Using the procedure detailed in Paragraph 5, remove the following modules:

IF Module
RF Module
Synthesiser 1 Module
Synthesiser 2 Module
Reference Oscillator Module

(4) Remove the link fitted in the SO socket.

(5) Disconnect the two DC connectors from the Analogue PSU.

(6) Unscrew the heatsink of the Analogue PSU from the chassis (2 x M3 nuts and washers) and the screw securing the PCB to the chassis partition (taking care to retain the spacer).

(7) Remove the Analogue PSU, carefully easing the multiway connector off the mating pins of the RF Backplane.

(8) The flexible PCB which interconnects the backplane to the Interface Module is secured by adhesive pads attached to the chassis partition. These should be eased free and the Interface Module connector removed (2 x M3 screws and washers).

(9) Remove the coaxial sockets fitted to the rear of the chassis.

(10) Remove the screws retaining the RF Backplane, taking care not to lose the spacers fitted beneath the connectors.

(11) Using the special extractor tool, (available from Cambridge Connectors Ltd, part number TLG66), disconnect the coax cable from the Reference Oscillator socket to the front chassis partition.

The procedure to **replace** the RF backplane is as follows:

(1) Reinstall the cable to the Reference Oscillator (no tool required).

(2) Check the lay of cables beneath the backplane prior to fitting the screws. Ensure that cable sleeves are not snagged on the soldered pins of the connectors and that the cables to the rear chassis panel are correctly routed.

(3) Refit the coaxial sockets to the rear of the chassis.

(4) Refit screws and spacers to secure backplane.

(5) Refit connector to Interface Module, renewing the adhesive pads on the flexible PCB interconnector.

(6) Carefully aligning the pins to mate with the correct connection refit the Analogue PSU, fitting the nuts and washers to the heatsink and finally the screw and spacer securing to the chassis partition.

(7) Replace modules, previously removed, in accordance with Paragraph 5 and the link in the SO socket.

(8) Replace the top cover as detailed in Paragraph 4.2

(9) Replace the unit in the rack as detailed in Paragraph 3.

Chapter 6

MODULE AND CHASSIS DESCRIPTIONS

1 INTRODUCTION

The purpose of this Chapter is to briefly describe the operation of the modules and chassis of the STR8212 Receiver at block diagram level. However, for the purpose of fault finding, full circuit diagrams and PCB layouts are provided for each area.

The location of the module/board in the radio chassis and the number of its associated backplane connector is given in Chapter 6.13 Figures 1 and 7.

For the purpose of this description, the receiver is divided into the following areas:

- RF Module . . . . . Chapter 6.1
- IF Module . . . . . Chapter 6.2
- Synthesiser 1 . . . . . Chapter 6.3
- Synthesiser 2 . . . . . Chapter 6.4
- Reference Oscillator Module . . . . . Chapter 6.5
- ADC Module . . . . . Chapter 6.6
- Interface Module . . . . . Chapter 6.7
- Controller Board Assembly . . . . . Chapter 6.8
- Controller Interface Board . . . . . Chapter 6.9
- Digital Signal Processor Boards . . . . . Chapter 6.10
- DAC/Sequencer Board Assembly . . . . . Chapter 6.11
- Front Panel Assembly . . . . . Chapter 6.12
- Chassis and Power Supplies . . . . . Chapter 6.13
- IEEE 488 Interface Board . . . . . Chapter 6.14
- Digital Output Board . . . . . Chapter 6.15
- Internal Interfaces . . . . . Chapter 6.16

Chapter 6.1

RF MODULE

1 INTRODUCTION

The RF Module assembly consists of a single PCB in a screened enclosure and occupies SK3 of the RF backplane within the radio.

The module description is given with reference to the following drawings/illustrations and items list:

- Figure 1 RF Module Simplified Block Diagram
- Figure 2 RF Module Layout Diagram
- Items List RF Module, Sheets 1 to 9 inc.
- Figure 3 RF Module Interconnection Circuit Diagram, Sheet 1 of 4
- Figure 4 RF Module Circuit Diagram, Sheet 2 of 4
- Figure 5 RF Module Circuit Diagram, Sheet 3 of 4
- Figure 6 RF Module Circuit Diagram, Sheet 4 of 4

2 MODULE DESCRIPTION

Module description is given under the following headings:

- RF Signal Path . . . . . Paragraph 2.1
- Typical Signal Levels . . . . . Paragraph 2.2
- Control Signals . . . . . Paragraph 2.3
- Options . . . . . Paragraph 2.4

2.1 RF Signal Path

The RF input at the antenna, in the frequency range 150 kHz to 40 MHz, is applied to the input protection circuitry which protects the equipment from damage by lightning and other high level signals. To avoid overloading the receiver during transmissions, the RF circuitry can be isolated from the antenna in Tx/Rx operations by the 'mute' relay RL1.

The RF signal now passes through the first low pass filter which provides rejection against 1st IF and image frequencies and reduces antenna leakage signals. After filtering, the signal passes through the RF Attenuator/Amplifier stage and then through a second low pass filter.

The RF signal is now mixed with the first local oscillator frequency (LO1) and converted to a fixed 1st IF frequency of 70.05 MHz. Finally the signal is amplified then fed out to the IF Module via a buffer stage.

BITE detector circuits provide 'on-line' monitoring for high RF level, open circuit RF fuse and low Local Oscillator level.

An 'off-line' BITE facility allows RF or IF test frequencies to be injected into the signal path for diagnostic purposes.

The basic building blocks of this module are:

- Input protection circuitry
- Low pass filter one
- Pre-amp and switched attenuators
- Low pass filter two
- Mixer
- Low noise amplifier
- Buffer

2.2 Typical Signal Levels

The required level of 'LO1' from the Synthesiser 1 module is between +3 and 6 dBm. For a signal at the antenna of -37 dBm, at the receiver tuned frequency, with CW mode selected and AGC on, the IF output from this module will be 70.05 MHz at a level of -30 dBm. Typical signal levels in the RF and IF paths are given in Chapter 3.

2.3 Control Signals

The module is controlled by serial data from the Controller interface. The Serial Data Control Interface within the module has the following three signal inputs:

(LOADA) indicates that data is valid and should be received by the interface. The interface takes action on the most recently received data on the trailing (positive going) edge of (LOADA). No action is taken on received data until a trailing edge of (LOADA) is received.

(SLOWDATA) is the serial data sent to the interface MSB first and is described in paragraph 5.3.

(SLOWCLOCK) indicates the boundaries between bits, the state of data is read by the interface on positive going edges of CLOCK.

Electrically the three interface signal inputs are 5V CMOS-compatible with a maximum operating speed of 10 kbit/second.

The output bits from the Serial Data Control Interface are as follows:

BIT 7 (MSB), BIT6 and BIT 5 relate to BITE and are described in paragraph 5.3.
BIT 4 is not used.

BIT 3	HIGH = 20 dB attenuator switched in
BIT 2	HIGH = 10 dB attenuator switched in
BIT 1	HIGH = 5 dB attenuator switched in
BIT 0 (LSB)	HIGH = 3 dB attenuator in; LOW = +7 dB pre-amplifier switched in

BIT7 of the Serial Data Control Interface is made available on the connector in latched logic true form as 'ENABLEDET'. This is intended for use by the IF module to enable the IF Detector B circuit.

2.4 Options

A Sub Octave Filter Module can be fitted to the radio in SK2 of the RF backplane This filter is inserted into the RF Signal path between the RF input protection circuitry and the first low-pass filter LPF1. Its function is to improve the 2nd order intermodulation performance.

3 CIRCUIT DESCRIPTION

Circuit description is given under the following headings:

- Input Protection Circuitry . . . . . Paragraph 3.1
- Low Pass Filter One . . . . . Paragraph 3.2
- Pre-Amp and Switched Attenuators . . . . . Paragraph 3.3
- Low Pass Filter Two . . . . . Paragraph 3.4
- Mixer . . . . . Paragraph 3.5
- LO Amplifier . . . . . Paragraph 3.6
- Diplexer . . . . . Paragraph 3.7
- IF Amplifier . . . . . Paragraph 3.8
- LC Tank - IF Interstage Filter . . . . . Paragraph 3.9
- IF Buffer . . . . . Paragraph 3.10

3.1 Input Protection Circuitry

The RF signal input protection circuit comprises a fuse, clamps, attenuators and a signal path 'mute' relay RL1. This circuit has several modes of operation depending on the degree of overload. In the case of lightning strike a spark gap (GAP1) absorbs energy long enough for the fuse (F1) to blow. For input voltage swings greater than 20V zener diodes (D7 and D8) will conduct causing the fuse to blow. For high level signals not greater than 20V a level detector (IC1) will cause (RL1-Mute) in-line relay to switch into an open circuit state.

3.2 Low Pass Filter One

The input to this filter from the input protection circuitry, is via a shorting link which connects between 'TO SO' and 'FROM SO' on SK2 of the RF backplane. This filter (L2, L3 and L4) is the first part of two stages of filtering and consists of an elliptical filter designed for maximum rejection at the first IF and first image frequencies. Loss directly affects noise figure. Stop band nulls are produced at 68.5 MHz, 79.5 MHz and 130.5 MHz. A test point TP1 (A6) in conjunction with the removal of JP2 facilitates the measurement and alignment of this filter.

3.3 Pre-amp and Switched Attenuators

The pre-amp (TR5, TR10) is a lossless feedback amplifier producing 7-8dB of gain. Four relays (RL2 to RL5) switch in combinations of amplifier or attenuators. The switched attenuator is arranged as four separate switched stages, pre-amp/3dB, 5dB, 10dB and 20dB. RL3 replaces the pre-amp with a 3dB pad, giving a net attenuation change of 10 to 13dB. The attenuation range available is 0 to 45dB in steps of 5dB via the SLOWDATA control. Test point TP1 (A6) with JP2 inserted and JP1 removed, in conjunction with test point TP2 (A5) with JP3 removed, facilitates the measurement of the pre-amplifier gain and attenuators as well as for the alignment of the following low-pass filter two.

3.4 Low Pass Filter Two

A second elliptical filter (L12, L13 and L14) provides further filtering of the received input. As with low-pass filter 1, stop band nulls are produced at 68.5 MHz, 89.5 MHz and 130.5 MHz.

3.5 Mixer

This active balanced mixer stage (T38, IC10, TR23, TR27 and T41), mixes the received RF (SIGNAL) with (LO1) a signal generated in the first Local Oscillator synthesiser unit, which is tuneable over the frequency range 70.05 -110.05 MHz. The mixer output comprises the difference frequency at 70.05 MHz and the sum frequency which is removed by the Diplexer. The mixer consists of a MOSFET ring (IC10) producing high dynamic range.

3.6 LO Amplifier

The (LO1) local oscillator input is filtered (L5, L6, L9 and L10) and amplified (TR17, TR18 and TR19) before being applied to the mixer. A test point (pad P2) prior to the push-pull mixer drive stage (T41 pin 4) allows tuning of the local oscillator band-pass filter. This filter produces stop band nulls at 40 MHz and 142 MHz.

3.7 Diplexer

The output of the mixer is via a diplexer (L15, L16 and L17) to maintain a wideband match.

3.8 IF Amplifier

The IF amplifier (TR24 and TR25) is a lossless feedback amplifier designed for low noise and provides 4.5dB of gain when cascaded with the interstage tuning of L19, C172.

3.9 LC Tank - IF Interstage Filter

This comprises a single tuned circuit (L19, C172) which reduces local oscillator breakthrough at the module output.

3.10 IF Buffer

This amplifier (TR29, TR30) has about 2dB of gain. The high input impedance at the transistor (TR29) base is resistively shunted to present a constant 50 ohm load to the preceding stage and therefore to the mixer IF port. This also isolates the mixer from impedance changes due to loading by the IF module.

4 ADJUSTMENTS

The module has, in total, fifteen adjustments, all of which are tunable inductors and are mainly for first, second and local oscillator band-pass filter alignment. These are factory set.

5 BITE FUNCTIONS

Detectors for open circuit RF fuse (IC2A), high RF levels A and B (TR12, TR13, TR14 and IC7) or 1st Local Oscillator drive low (TR26 and IC8D) are provided for the on-line BITE function. Correct logic levels at the output of all the above detectors are; '0' = OK or '1' = fault. The two RF levels A and B have typical thresholds of -13dBm for (HIGHRFA) and -19dBm for (HIGHRFB) whereby, when the lower is exceeded, a warning on the LCD panel informs the operator to add attenuation until the hysteresis level set by the other detector extinguishes the message. Typical 1st Local Oscillator Low threshold is -4dBm.

A dual purpose test source within the RF module provides the off-line BITE function to test the RF and IF bands. This source is enabled via the (SLOWDATA) input to the Serial Data Control Interface which, in turn, produces the (SOURCEON) and (RF/IF SOURCE) control signals. The onboard switchable RF and IF source inserts a comb of test tones at RF or IF frequencies into the signal path, and detectors are enabled to monitor for correct levels. Insertion at RF or IF is determined by the logic state of the (RF/IF SOURCE) input.

5.1 RF Source

The RF Source is derived from a crystal oscillator and divider (IC11A and D, IC3A and B, IC4A), which generates a harmonic-rich 921.6 kHz output. This is routed into the RF path via the Mute Relay RL1 when 'Mute' is enabled.

5.2 IF Source

The IF source is provided using a gate (IC5D) to mix a low frequency square-wave (IC5A and B) with an output of the BITE divider chain, which results in a waveform containing components around the IF frequency. This signal (IF Source) is injected at the diplexer following the first mixer.

5.3 Serial Control Bits Related to BITE (SLOWDATA)

The serial control word 'BIT 7' (MSB), when high (1), enables the test source, the IF BITE detector and also the IF detector within the IF module. This is controlled by one signal labelled either as (SOURCEON) or (ENABLEDET). When (ENABLEDET) is active, during BITE, the IF detector output (IFDETA) is switched through to the (HIGHRFB) output. Typical IF detector threshold is -21dBm.

Control 'Bit 6' operates,	when high(1), the RF Mute via RL1.
Control 'Bit 5' operates,	when high (1), the RF Source. when low (0), the IF Source.

RF MODULE SIGNAL DESCRIPTION	ON-LINE MONITORING	OFF-LINE TEST	
		RF SOURCE SELECTED	IF SOURCE SELECTED
Serial Control BIT 7	0	1	1
Serial Control BIT 6	0	1	1
Serial Control BIT 5	0	1	0
RF Detector 'A' - (HIGHRFA) O/P	Active	Active	0
RF Detector 'B' - (HIGHRFB) O/P	Active	Disabled	Disabled
IF Detector 'A' - (HIGHRFB) O/P	Disabled	Active	Active
IF MODULE SIGNAL DESCRIPTION			
IF Detector - (IFDETB)	Disabled	Active	Active
50 kHz IF Detector (BBDET)	Disabled	Active	Active

When using the RF source, the controller software will check for a signal at IF to ensure that the RF mixer is operational.

The IF source BITE test is used, in part, (ie when the test signal is injected at the diplexer) to check the operation of the IF attenuator within the IF module.

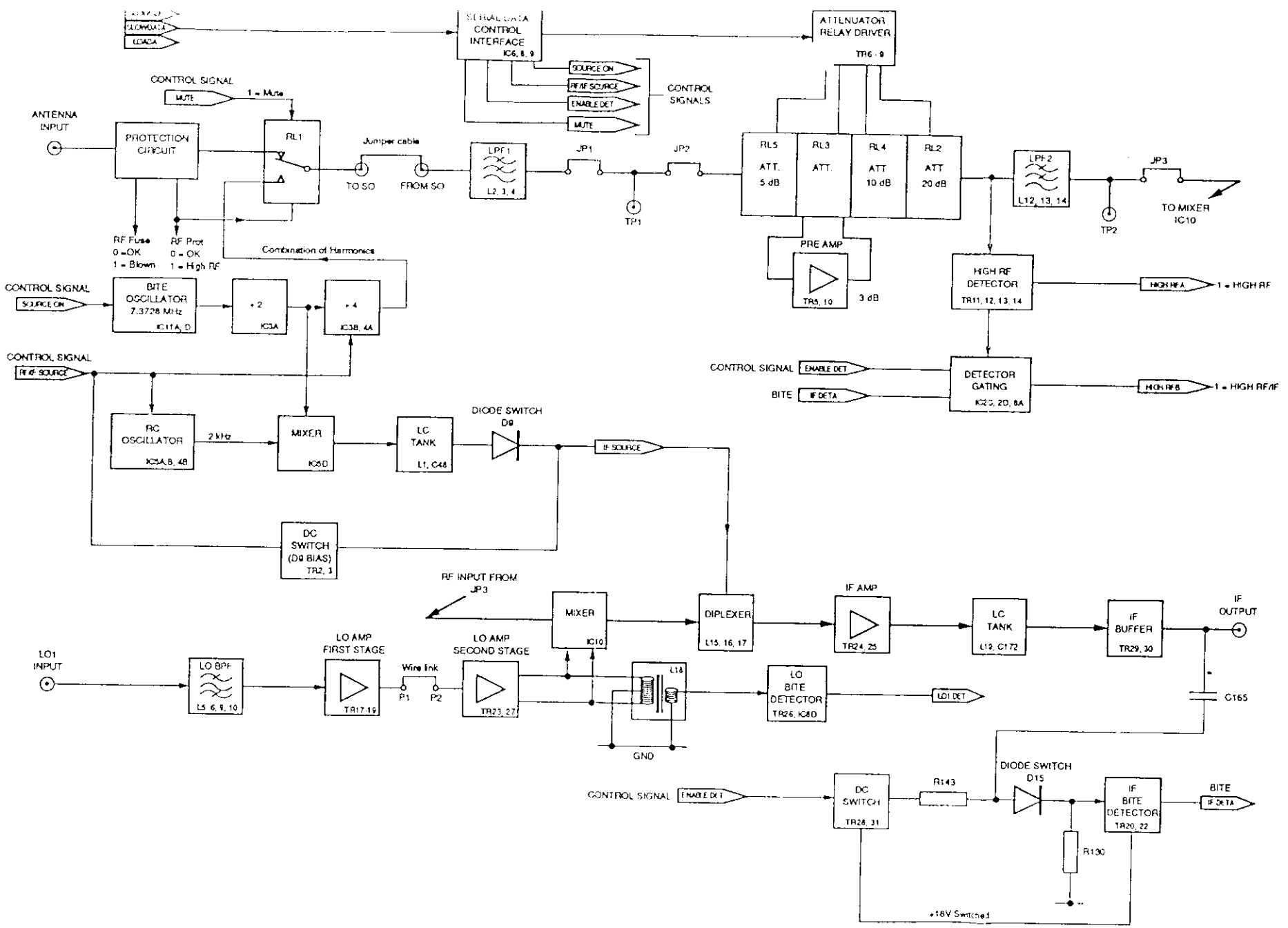


Figure 1 - RF Module Simplified Block Diagram

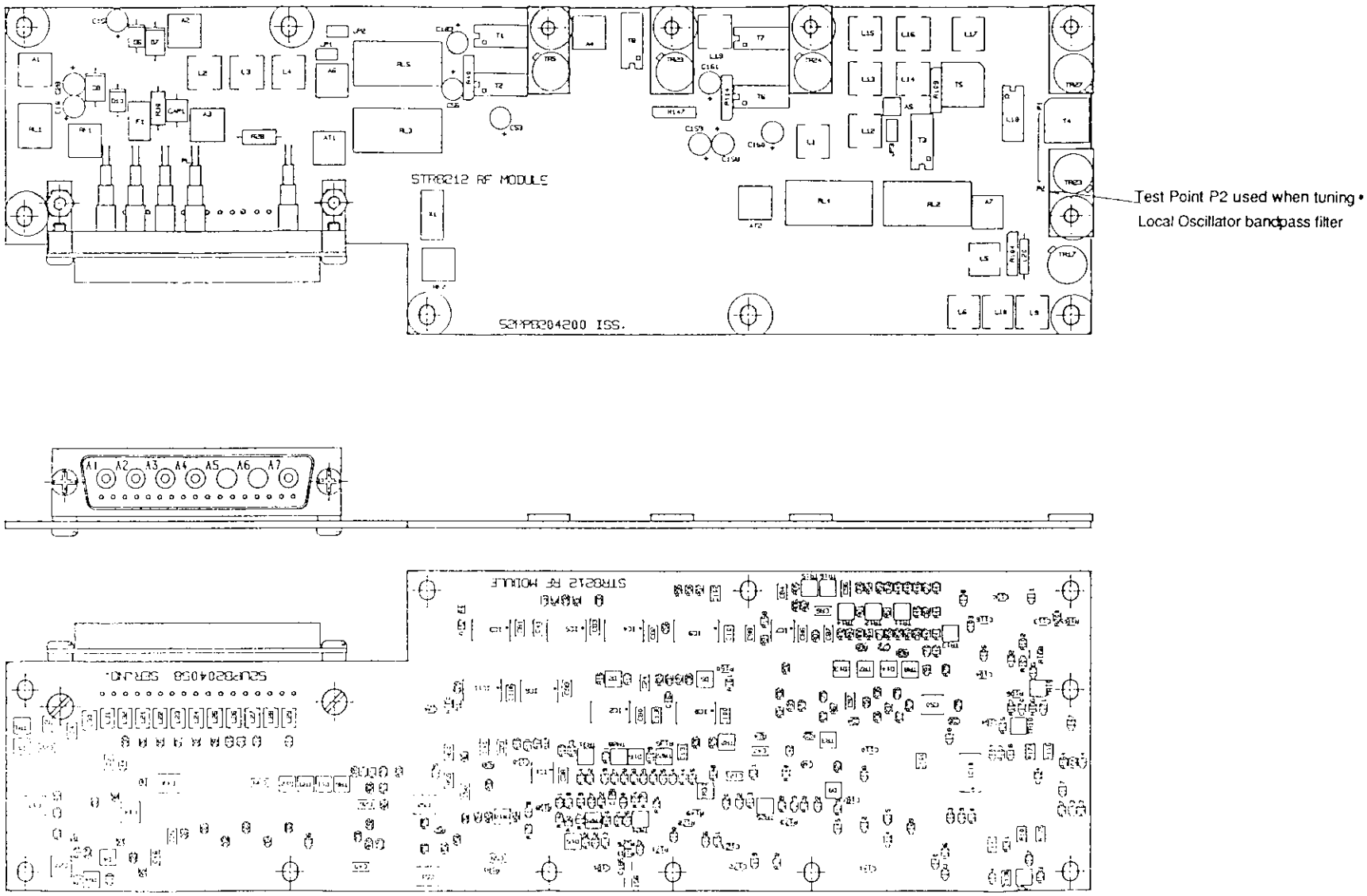


Figure 2 - RF Module Layout Diagram

Circuit Reference	Description	Value
C2 to C4	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C5 to C13	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C14	Capacitor, fixed, ceramic chip, 10%, 63V	470n
C15 to C16	Capacitor, fixed, ceramic chip, 5% 100V	100p
C17	Capacitor, fixed, ceramic chip, 10%, 63V	470n
C18 to C21	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C22 to 26	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C27	Capacitor, fixed, ceramic chip, 10%, 63V	470n
C28	Capacitor, fixed, al electrolytic, 20%, 100V	1µ
C29	Capacitor, fixed, ceramic chip, 5%, 100V	68p
C31	Capacitor, fixed, ceramic chip, 5%, 100V	82p
C32	Capacitor, fixed, ceramic chip, 5%,100V	3n3
C33	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C34	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C36	Capacitor, fixed, ceramic chip, 5%, 100V	220p
C37	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C38 to C41	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C42	Capacitor, fixed, ceramic chip, ± 0.5p, 100V	4p7
C43	Capacitor, fixed, ceramic chip, 10%, 63V	470n
C44	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C46 to C47	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C48	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C49 to C52	Capacitor, fixed, ceramic chip, 10%, 63V	470n
C53	Capacitor, fixed, al electrolytic, 20%, 100V	1µ
C54	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C55	Capacitor, fixed, al electrolytic, 20%, 50V	10µ
C56	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C57	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C58 to C59	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C60	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C62	Capacitor, fixed, ceramic chip, 5%, 100V	82p
C64	Capacitor, fixed, ceramic chip, 5%, 100V	82p
C65	Capacitor, fixed, ceramic chip, 5%, 100V	27p

Circuit Reference	Description	Value
C66	Capacitor, fixed, ceramic chip, 5%, 100V	56p
C67	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C68	Capacitor, fixed, ceramic chip, 5%, 100V	33p
C69 to C79	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C80 to C 87	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C88 to C95	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C96 to C102	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C103	Capacitor, fixed, ceramic chip, 5%, 100V	27p
C104	Capacitor, fixed, ceramic chip, 5%, 100V	12p
C105	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C106	Capacitor, fixed, ceramic chip, 5%, 100V	27p
C107	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C108	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C109	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C110	Capacitor, fixed, ceramic chip, 5%, 100V	68p
C111	Capacitor, fixed, ceramic chip, 5%, 100V	150p
C112	Capacitor, fixed, ceramic chip, 5%, 100V	39p
C113 to C114	Capacitor, fixed, ceramic chip, 5%, 100V	82p
C115	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C116	Capacitor, fixed, ceramic chip, 5%, 100V	56p
C117	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C118 to C120	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C121	Capacitor, fixed, ceramic chip, 10%, 10V	100n
C122 to C123	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C125	Capacitor, fixed, ceramic chip, 5%, 100V	56p
C126	Capacitor, fixed, ceramic chip, 5%, 100V	33p
C127 to C130	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C131	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C132	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C134	Capacitor, fixed, ceramic chip, 10%, 100V	4n7
C135	Capacitor, fixed, ceramic chip, 5%, 100V	27p
C136	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C137	Capacitor, fixed, ceramic chip, 10%, 100V	1n

Circuit Reference	Description	Value
C138	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C139	Capacitor, fixed, ceramic chip, 5%, 100V	56p
C140	Capacitor, fixed, ceramic chip, 5%, 100V	18p
C141	Capacitor, fixed, ceramic chip, 5%, 100V	33p
C143 & C144	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C145	Capacitor, fixed, ceramic chip, 5%, 100V	10p
C146	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C147 to C152	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C153	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C154 to C157	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C158	Capacitor, fixed, al electrolytic, 20%, 100V	1µ
C159	Capacitor, fixed, al electrolytic, 20%, 500V	10µ
C160	Capacitor, fixed, al electrolytic, 20%, 100V	1µ
C161	Capacitor, fixed, al electrolytic, 20%, 500V	10µ
C162	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C163	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C164 & C165	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C169 to C171	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C172	Capacitor, fixed, ceramic chip, 5%, 100V	68p
C173	Capacitor, fixed, ceramic chip, ± 0.5p, 100V	2p2
C175	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C177	Capacitor, fixed, ceramic chip, 5%, 100V	330p
C178	Capacitor, fixed, ceramic chip, ±0.5p, 100V	4p7
C180	Capacitor, fixed, ceramic chip, ±0.5p, 100V	2p2
C181	Capacitor, fixed, ceramic chip, 5%, 100V	82p
C182	Capacitor, fixed, ceramic chip, ±0.5p, 100V	2p2
C183	Capacitor, fixed, al electrolytic, 20%, 50V	10µ
C184	Capacitor, fixed, ceramic chip, 5%, 100V	180p
C185	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C186	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C187	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C188	Capacitor, fixed, ceramic chip, 5%, 100V	8p2
C189	Capacitor, fixed, ceramic chip, 5%, 100V	27p

Circuit Reference	Description	Value
C190	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C191	Capacitor, fixed, ceramic chip, 10%, 100V	10n
LI	Choke, wound, special purpose	
L2	Choke, wound, special purpose	
L3	Choke, wound, special purpose	
L4	Choke, wound, special purpose	
L5	Choke, wound, special purpose	
L6	Choke, wound, special purpose	
L9	Choke, wound, special purpose	
L10	Choke, wound, special purpose	
LI2	Choke, wound, special purpose	
LI3	Choke, wound, special purpose	
LI4	Choke, wound, special purpose	
LI5	Choke, wound, special purpose	
LI6	Choke, wound, special purpose	
LI7	Choke, wound, special purpose	
LI8	Choke, wound, special purpose	
LI9	Choke, wound, special purpose	
L20	Choke, fixed, RF, 10%	470µ
L21 to L32	Choke, fixed,chip, 10%	4µ7
IC1	High Performance Comparator, LM311D	
IC2	Quad 2-Input Nand Schmitt, HEF4093BT	
IC3	Dual D-Type Flip Flop, 74AC74SC	
IC4	Dual D-Type Flip Flop, 74AC74SC	
IC5	Quad 2-Input Nand, 74AC00SC	
IC6	Quad 2-Input Nand, HEF4011BT	
IC7	Dual Differential Comparator, LM393D	
IC8	Quad 2-Input Nand Schmitt, HEF4093BT	
IC9	8 Stage Shift & Store Bus Register, HEF4094BT	
IC10	Double Balanced Mixer, Si8901Y	
IC11	Quad 2-Input Nand, 74AC00SC	

Circuit Reference	Description	Value
R1	Resistor, fixed, chip, 2%, 0.1W	10M
R2	Resistor, fixed, chip, 1%, 0.1W	390R
R3	Resistor, fixed, chip, 1%, 0.1W	100k
R4 to R6	Resistor, fixed, chip, 1%, 0.1W	1k
R7	Resistor, fixed, chip, 1%, 0.1W	10k
R8	Resistor, fixed, chip, 1%, 0.1W	100k
R9 & R10	Resistor, fixed, chip, 1%, 0.1W	10k
R11	Resistor, fixed, chip, 1%, 0.1W	56k
R12 & R13	Resistor, fixed, chip, 1%, 0.1W	12k
R14	Resistor, fixed, chip, 1%, 0.1W	100k
R15	Resistor, fixed, chip, 1%, 0.1W	10k
R16	Resistor, fixed, chip, 1%, 0.1W	13k
R17	Resistor, fixed, chip, 1%, 0.1W	1k
R18	Resistor, fixed, chip, 1%, 0.1W	10k
R19	Resistor, fixed, chip, 1%, 0.1W	4k7
R20	Resistor, fixed, chip, 1%, 0.1W	10k
R22	Resistor, fixed, chip, 1%, 0.1W	10k
R23	Resistor, fixed, chip, 1%, 0.1W	3k3
R24	Resistor, fixed, chip, 1%, 0.1W	47k
R25	Resistor, fixed, chip, 1%, 0.1W	10k
R26	Resistor, fixed, chip, 1%, 0.1W	12k
R27	Resistor, fixed, chip, 1%, 0.1W	150k
R28	Resistor, fixed, metal film, 5%, 1W	10k
R29	Resistor, fixed, chip, 1%, 0.1W	12k
R30	Resistor, fixed, metal film,1%, 0.125W	100k
R32 & R33	Resistor, fixed, chip, 2%, 0.1W	27R
R34	Resistor, fixed, chip, 2%, 0.1W	36R
R35 & R36	Resistor, fixed, chip, 2%, 0.1W	43R
R37 & R38	Resistor, fixed, chip, 2%, 0.1W	10R
R40	Resistor, fixed, metal film,1%, 0.125W	43R
R41	Resistor, fixed, chip, 1%, 0.1W	10k
R42	Resistor, fixed, chip, 1%, 0.1W	15k
R43	Resistor, fixed, chip, 1%, 0.1W	1k

Circuit Reference	Description	Value
R44	Resistor, fixed, chip, 1%, 0.1W	150R
R45	Resistor, fixed, chip, 1%, 0.1W	8k2
R46	Resistor, fixed, chip, 1%, 0.1W	3k3
R47	Resistor, fixed, chip, 1%, 0.1W	1k
R48	Resistor, fixed, chip, 1%, 0.1W	150R
R49	Resistor, fixed, chip, 2%, 0.1W	47R
R50	Resistor, fixed, chip, 1%, 0.1W	220R
R51	Resistor, fixed, chip, 1%, 0.1W	8k2
R52	Resistor, fixed, chip, 1%, 0.1W	3k3
R53	Resistor, fixed, chip, 1%, 0.1W	150R
R54	Resistor, fixed, chip, 2%, 0.1W	27R
R55	Resistor, fixed, chip, 1%, 0.1W	1k
R56 & R57	Resistor, fixed, chip, 2%, 0.1W	15R
R58	Resistor, fixed, chip, 2%, 0.1W	82R
R59 & R60	Resistor, fixed, chip, 2%, 0.125W	8R2
R61	Resistor, fixed, chip, 1%, 0.1W	150R
R64 to R68	Resistor, fixed, chip, 1%, 0.1W	1k
R69 to R73	Resistor, fixed, chip, 1%, 0.1W	12k
R75 to R78	Resistor, fixed, chip, 1%, 0.1W	12k
R79 & R80	Resistor, fixed, chip, 1%, 0.1W	1k
R81	Resistor, fixed, chip, 1%, 0.1W	100k
R82	Resistor, fixed, metal film, 5%, 1W	100R
R83	Resistor, fixed, chip, 1%, 0.1W	8k2
R84	Resistor, fixed, chip,1%, 0.1W	47R
R85	Resistor, fixed, chip, 1%, 0.1W	8k2
R86	Resistor, fixed, chip, 1%, 0.1W	620R
R87	Resistor, fixed, chip, 1%, 0.1W	8k2
R88	Resistor, fixed, chip, 1%, 0.1W	10k
R89	Resistor, fixed, chip,	0R
R90	Resistor, fixed, chip, 1%, 0.1W	8k2
R91 & R92	Resistor, fixed, chip, 1%, 0.1W	4k7
R93	Resistor, fixed, chip, 1%, 0.1W	2k7
R94	Resistor, fixed, chip, 1%, 0.1W	10k

Circuit Reference	Description	Value
R95 to R97	Resistor, fixed, chip, 1%, 0.1W	47k
R99	Resistor, fixed, chip, 2%, 0.1W	22R
R101	Resistor, fixed, chip, 5%, 0.25W	2k2
R102	Resistor, fixed, chip, 1%, 0.1W	150R
R103	Resistor, fixed, chip, 1%, 0.1W	1k2
R104	Resistor, fixed, metal film, 1%, 0.125W	200R
R105 & R106	Resistor, fixed, chip, 1%, 0.1W	2k7
R107	Resistor, fixed, chip, 2%, 0.1W	10k
R109	Resistor, S.O.T.	
R110	Resistor, fixed, chip, 1%, 0.1W	1k5
R111	Resistor, fixed, chip, 2%, 0.1W	10R
R113	Resistor, fixed, chip, 1%, 0.1W	1k
R114	Resistor, fixed, metal film, 1%, 0.125W	43R
R116	Resistor, fixed, chip, 5%, 0.25W	2k2
R117	Resistor, fixed, chip, 1%, 0.1W	8k2
R118	Resistor, fixed, chip, 1%, 0.1W	3k3
R119	Resistor, fixed, chip, 1%, 0.1W	1k
R120	Resistor, fixed, chip, 1%, 0.1W	150R
R121	Resistor, fixed, chip, 2%, 0.1W	47R
R122	Resistor, fixed, chip, 1%, 0.1W	220R
R123	Resistor, fixed, chip, 1%, 0.1W	8k2
R124	Resistor, fixed, chip, 1%, 0.1W	3k3
R125	Resistor, fixed, chip, 1%, 0.1W	150R
R126	Resistor, fixed, chip, 2%, 0.1W	27R
R127	Resistor, fixed, chip, 1%, 0.1W	1k
R128	Resistor, fixed, chip, 1%, 0.1W	43k
R129 & R130	Resistor, fixed, chip, 1%, 0.1W	1k
R131	Resistor, fixed, chip,1%, 0.1W	10k
R132	Resistor, fixed, chip, 1%, 0.1W	47k
R133	Resistor, fixed, chip, 1%, 0.1W	100k
R134	Resistor, fixed, chip, 1%, 0.1W	4k7
R135	Resistor, fixed, chip, 1%, 0.1W	100k
R136	Resistor, fixed, chip, 2%, 0.1W	51R

Circuit Reference	Description	Value
R137	Resistor, fixed, chip, 2%, 0.1W	22R
R138	Resistor, fixed, chip, 2%, 0.1W	47R
R139	Resistor, fixed, chip, 1%, 0.1W	10k
R140	Resistor, fixed, chip, 1%, 0.1W	2k7
R141 & 142	Resistor, fixed, chip, 1%, 0.1W	470R
R143	Resistor, fixed, chip, 1%, 0.1W	3k9
R144	Resistor, fixed, chip, 2%, 0.1W	10R
R145	Resistor, fixed, chip, 1%, 0.1W	2k7
R147	Resistor, fixed, metal film, 1%, 0.125W	43R
R148	Resistor, fixed, chip, 1%, 0.1W	10k
R149	Resistor, fixed, chip, 1%, 0.1W	1k
R151	Resistor, fixed, chip, 1%, 0.1W	150R
R152 to R154	Resistor, fixed, chip, 1%, 0.1W	10k
R156	Resistor, fixed, chip, 1%, 0.1W	1k
R157	Resistor, fixed, chip, 2%, 0.1W	51R
R158	Resistor, fixed, chip, 1%, 0.1W	47k
R159	Resistor, fixed, chip, 1%, 0.1W	47R
R160 & R161	Resistor, fixed, chip, 2%, 0.1W	4M7
R163 & R164	Resistor, fixed, chip, 1%, 0.1W	100R
R166	Resistor, fixed, chip, 1%, 0.1W	100R
R167	Resistor, fixed, chip, 1%, 0.1W	620R
R168	Resistor, fixed, chip, 1%, 0.1W	150R
R169	Resistor, fixed, chip, 2%, 0.1W	27R
R170 & R171	Resistor, fixed, chip, 2%, 0.1W	10R
R173	Resistor, fixed, chip, 2%, 0.1W	10R
R174 & R175	Resistor, fixed, chip, 5%, 0.25W	2k2
R176	Resistor, fixed, chip, 2%, 0.1W	18R
R177	Resistor, fixed, metal film, 2%, 0.25W	100R
R178	Resistor, fixed, chip, 2%, 0.1W	56R
R179	Resistor, fixed, chip, 2%, 0.1W	27R
R181 to R183	Resistor, fixed, chip, 1%, 0.1W	100R
R200	Resistor, fixed, chip,1%, 0.1W	150R

Circuit Reference	Description	Value
D1	Diode, Silicon Planar, High Speed Switching, BAS16	
D2	Diode, BAV70	
D4	Diode, Silicon Planar, High Speed Switching, BAS16	
D5	Diode, Zener, BZX84C4V7	
D6	Diode, Rectifier, IN4001G	
D7 & D8	Diode, Zener, BZWO 3 C20	
D9	Diode, BAT18	
D10	Diode, Rectifier, IN4001G	
D11 to D14	Diode, Silicon Planar, High Speed Switching, BAS16	
D15	Diode, BAT18	
D16	Diode, Silicon Planar, High Speed Switching, BAS16	
TR1	Transistor, P Channel, ZVP3310F	
TR2	Transistor, PNP, BCW30	
TR3	Transistor, PNP, BCW31	
TR4	Transistor, P Channel, ZVP3310F	
TR5	Transistor, RF linear, LT1001A	
TR6 to TR9	Transistor, N Channel, VN10LF	
TR10	Transistor, PNP, BCW30	
TR11 to TR14	Transistor, RF Broad Band, BFS17	
TR15 & TR16	Transistor, NPN, BCW31	
TR17	Transistor, RF linear, LT1001A	
TR18	Transistor, RF Broad Band, BFS17	
TR19	Transistor, PNP, BSR12	
TR20 to TR22	Transistor, RF Broad Band, BFS17	
TR23 & TR24	Transistor, RF linear, LT1001A	
TR25	Transistor, PNP, BCW30	
TR26	Transistor, RF Broad Band, BFS17	
TR27	Transistor, RF linear, LT1001A	
TR28	Transistor, PNP, BCW30	
TR29	Transistor, RF linear, LT1001A	
TR30	Transistor, PNP, BCW30	
TR31	Transistor, NPN, BCW31	

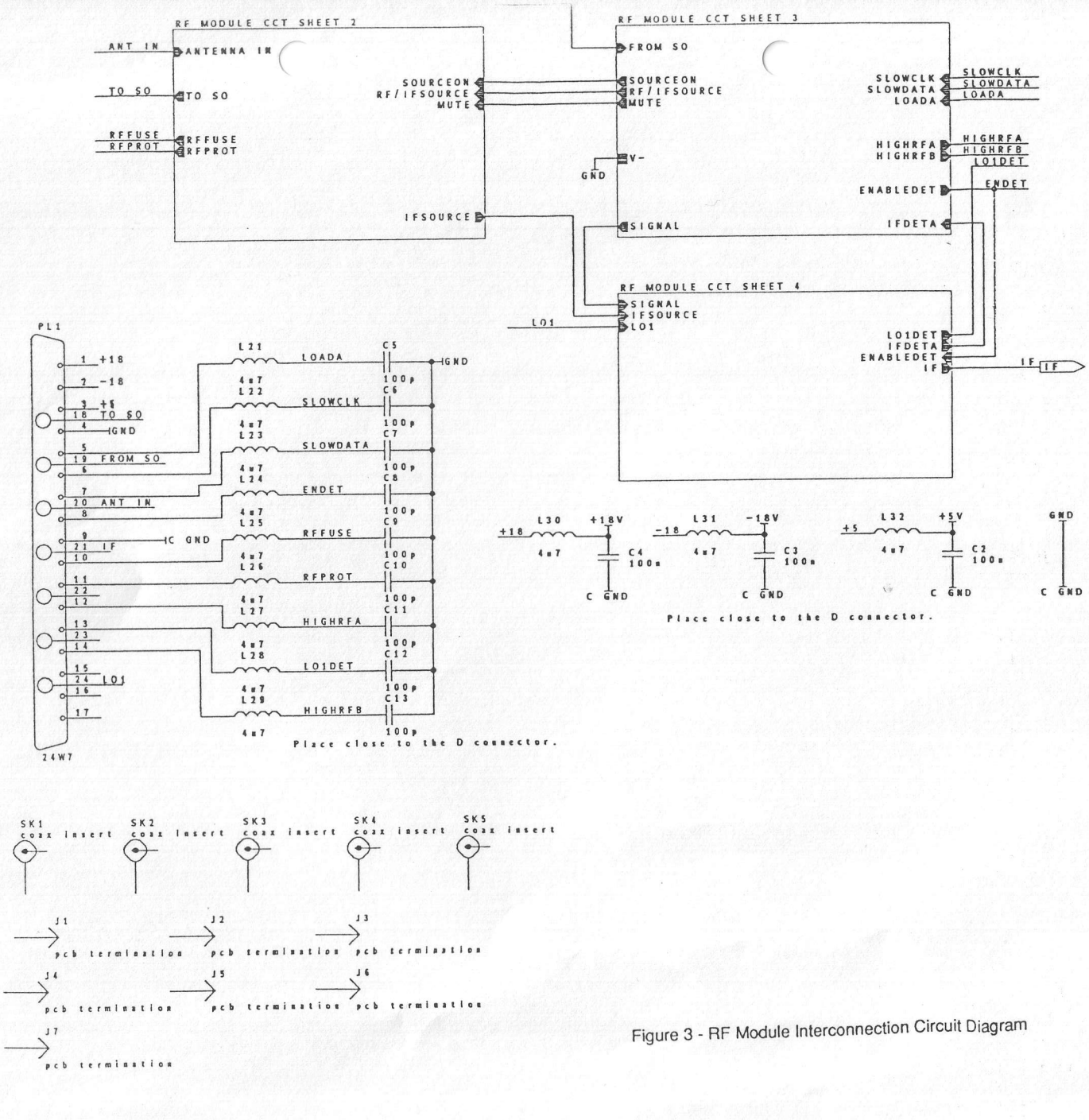


Figure 3 - RF Module Interconnection Circuit Diagram

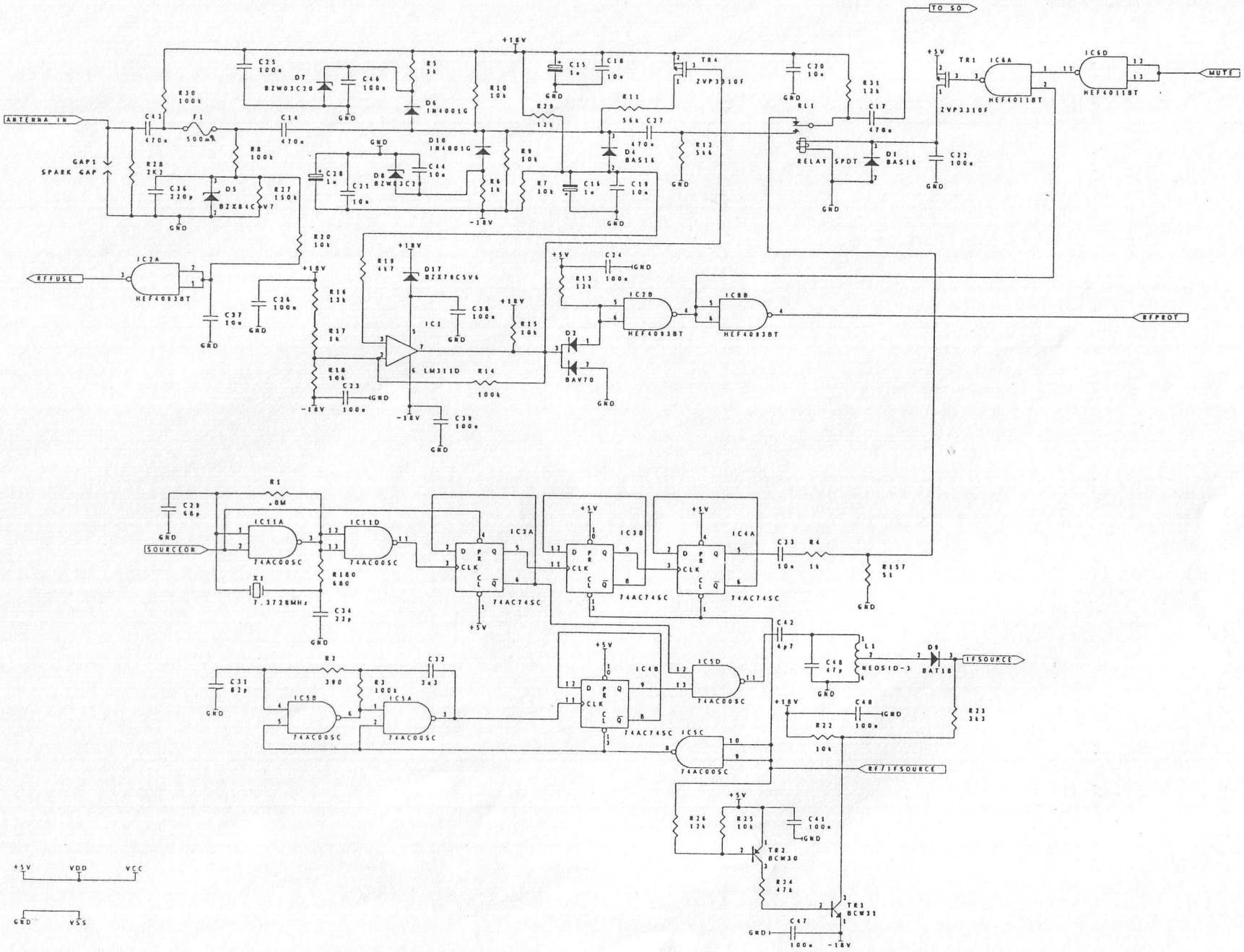


Figure 4 - RF Module Circuit Diagram

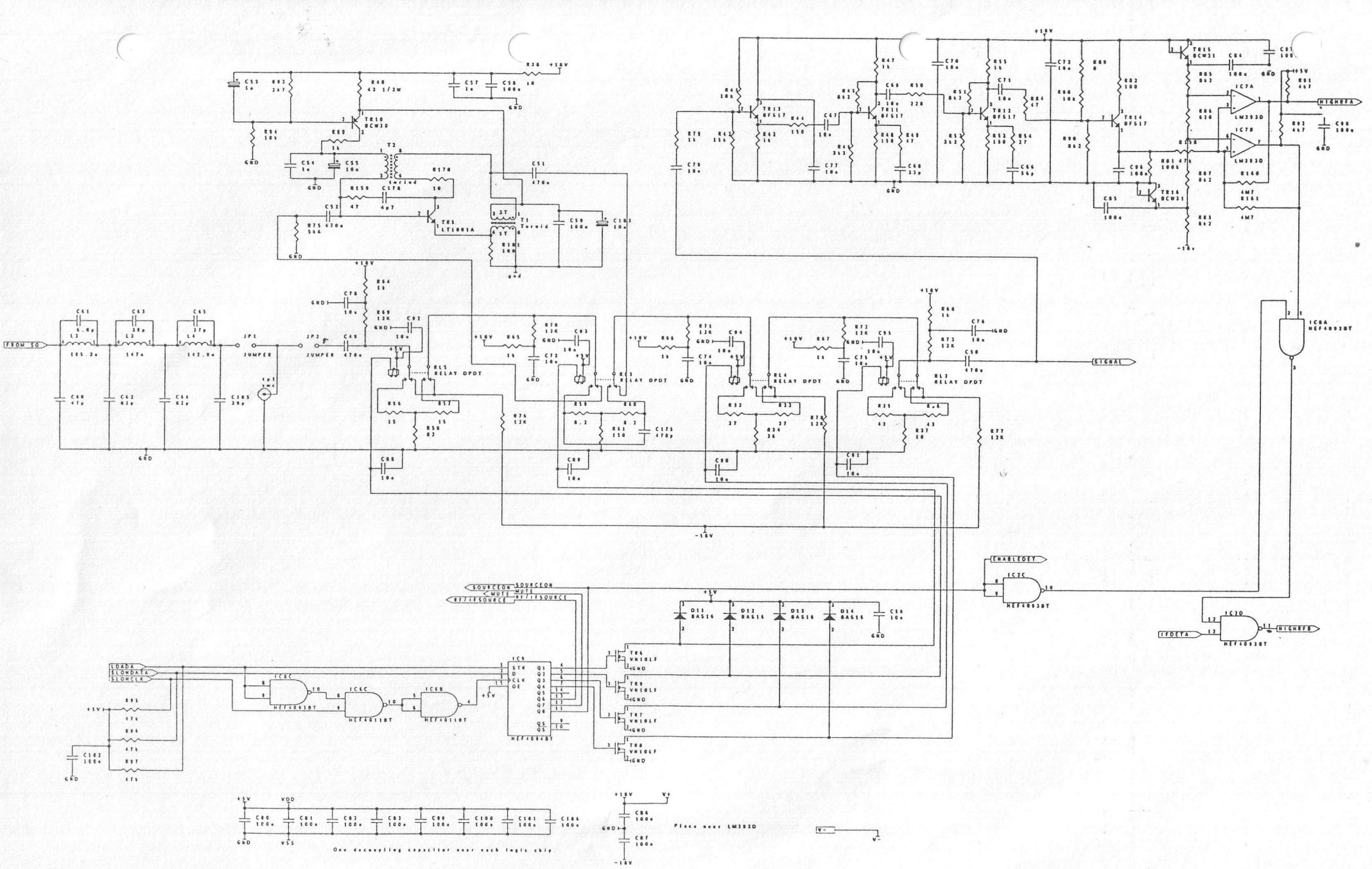


Figure 5 - RF Module Circuit Diagram

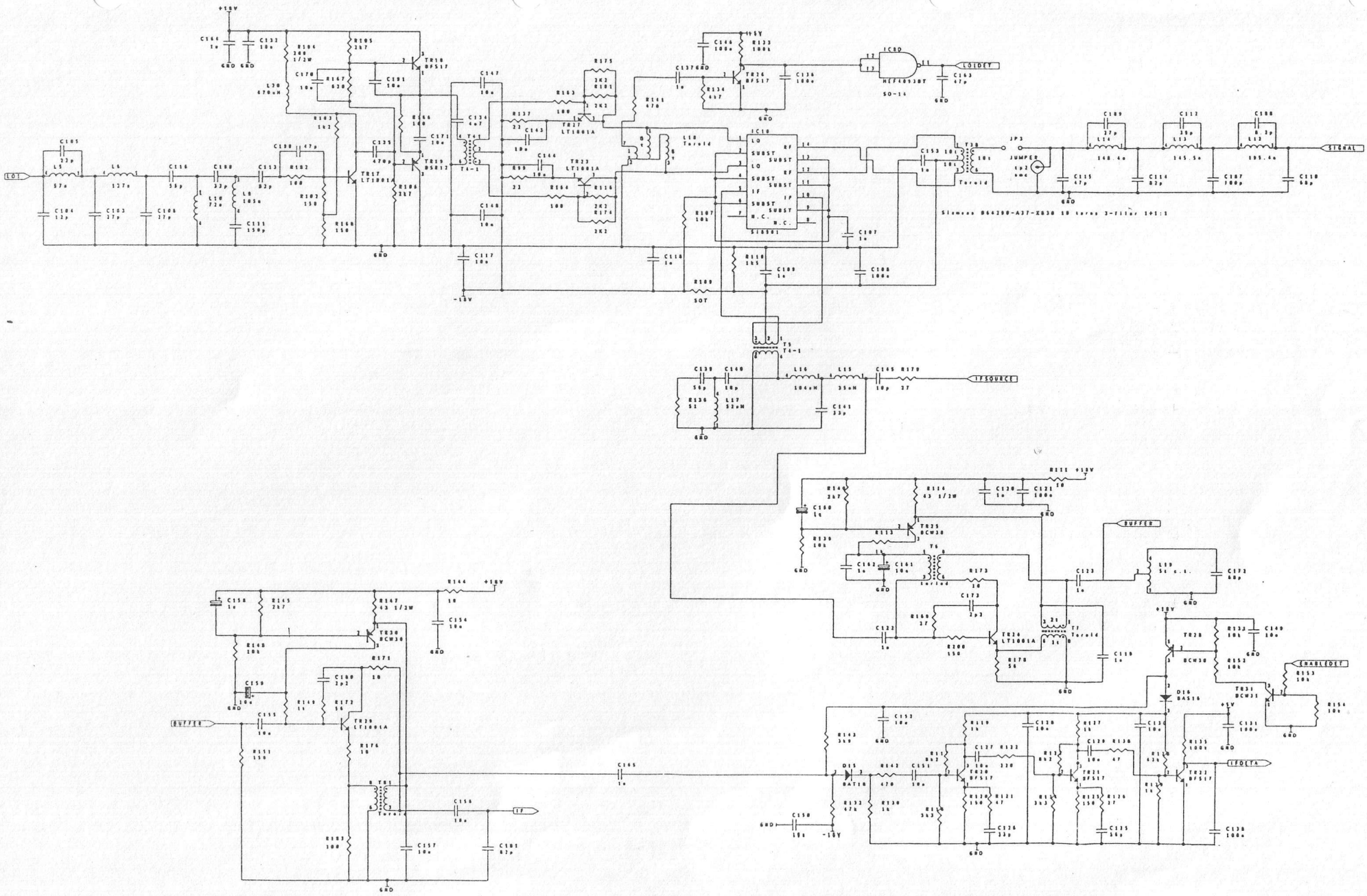


Figure 6 - RF Module Circuit Diagram

Chapter 6.2

IF MODULE

1 INTRODUCTION

The IF module assembly consists of a single PCB in a screened enclosure which plugs directly into SK1 of the RF backplane. A single connector carries both RF and d.c. signals.

The module description is given with reference to the following drawings/illustrations and items list:

- Figure 1 IF Module Simplified Block Diagram
- Figure 2 IF Module Layout Diagram
- Items list IF Module, sheets 1 to 9
- Figure 3 IF Module Circuit Diagram, sheet 1 of 3
- Figure 4 IF Module Circuit Diagram, sheet 2 of 3
- Figure 5 IF Module Circuit Diagram, sheet 3 of 3

2 MODULE DESCRIPTION

The module incorporates the first IF filter at a centre frequency of 70.05 MHz, and the IF attenuator which is the control element of the receivers IF AGC system. A mixer stage which is fed with a second local oscillator at 70 MHz, then converts the signal down to a second IF of 50 kHz.

The 70.05 MHz first IF input from the RF module first passes through the IF attenuator. Under normal operating conditions the attenuation will be set by a control word, generated within the Controller and sent via the Controller Interface in serial format, in response to a request from the sub system to increase or decrease the signal input to the ADC. This is the feed-back IF AGC system. This system is overridden in Manual or Manual+ AGC modes by operation of the Gain/Squelch control on the radio front panel. Paragraph 3 gives further details of the IF Attenuator circuit.

The receiver demodulation bandwidth is determined by digital filters in the DSP sub system, which gives the receiver its flexibility and repeatability of filtering performance. The crystal roofing filter in the IF module defines the bandwidth for IF amplification, downconversion and the digitisation process, and therefore also reduces the susceptibility of subsequent stages to overload from adjacent signals. The choice of suitable filter bandwidths is therefore a compromise between adjacent-channel rejection and the effect on the filtering performance obtained by the digital filters. Since the largest demodulation bandwidth required is 15 kHz, a crystal filter bandwidth slightly greater than this is ideal.

A low noise amplifier is now used to compensate for the filter loss. This is followed by a buffer amplifier to present a good match to the second mixer stages.

The first stage of the mixer splits the signal into its in-phase (I) and quadrature (Q) components. This is followed by two double balanced mixers that form an Image Reject Mixer which, in conjunction with the 70 MHz LO2 signal, generates a 50 kHz second IF signal. The LO2 signal is fed to the mixers via the LO2 Driver stage which has a push-pull output feeding the toroidal transformers T2 and T3. Paragraph 4 gives further details of the Image Reject Mixer.

The (I) and (Q) signals are amplified in low noise baseband pre-amplifiers and then finally combined in the Polyphase Combiner to form the 50 kHz second IF output to the ADC module.

2.1 Typical Signal Levels

The required level of LO2 from the Synthesiser 2 module is between 3 and 6 dBm. For a signal at the antenna of -40 dBm, at the receiver tuned frequency, with CW mode selected and AGC ON, the IF input to this module will be 70.05 MHz at a level of -33 dBm, and the output from this module will typically be a 0.6v pk-pk signal at 50 kHz.

2.2 Control signals

The module is controlled by serial data from the Controller Interface which provides the SLOWDATA, SLOWCLOCK and LOADD signals which are described in paragraph 3.2. An additional signal ENABLEDET from the RF Module enables the IF Detector during off-line BITE.

2.3 Options

The standard module includes a roofing filter optimised for selectivity and is a compromise in respect of group delay distortion. For specialist applications such as Direction Finding or data systems, a "broader bandwidth" linear phase filter can be provided in the alternate roofing filter position.

3 IF ATTENUATOR CIRCUIT

The IF Attenuator circuit description is given under the following headings:

- The Attenuator . . . . . Paragraph 3.1
- Control Circuit . . . . . Paragraph 3.2

3.1 The Attenuator

The IF attenuator comprises PIN diodes in a PI configuration giving a control range of >40dB. The RF resistance of each diode is controlled by means of controlled current sources. A fixed relationship is maintained over the full control range between the RF resistance of the series diodes and the RF resistance of the two shunt diodes. The RF chokes provide a DC bias current path, and the series capacitors act as DC blocks. The inductor L10 together with C102 and circuit strays form a parallel-tuned circuit at the IF frequency, thereby "resonating out" the shunt stray capacity which would otherwise reduce the available attenuation range.

3.2 Control Circuit

The attenuator is controlled by means of a serial control word input on SLOWDATA and clocked by SLOWCLK into a serial-to-parallel register IC16 whenever LOADD is low. When LOADD goes high the parallel word is latched at the output of IC16. The output 8-bit word controls the IF attenuator (bits 6 thro 0) while the MSB(bit 7) controls the optional selectable roofing filters.

The multiplying D to A converter IC13 obtains its reference input from the voltage reference IC, DA, and generates a "digitally controlled" current at Pin 6, which produces a "linearly varying" voltage at the output of IC12a. The transistor IC11d in conjunction with IC12d provides a logarithmically expanded negative voltage. The following stage comprises IC12c and the emitter follower TR19, arranged as an inverting unity gain amplifier. The output voltage determines the current into the current mirrors IC11a, b, c and hence the current in the series PIN diode of the attenuator. A small amount of positive feedback via R111 optimizes the attenuator control range by expanding the diode current control law. This permits use of the PIN characteristic over the whole of its characteristic including the low resistance (high current) region, thereby permitting operation with minimum residual attenuation.

The following stage IC14a, b, c, d, e is a current-steering amplifier, the available total current being determined by IC15a. This stage forms part of a negative-feedback loop with IC12b providing a feedback current into IC15b, the input stage of a current mirror formed by IC15a, b, d, e. Operation of this loop is such that the current through R117 is kept constant as the current through R115 increases (proportional to the current in the series PIN diode), by reducing the available total current from IC15a.

The current in the shunt PIN diodes of the attenuator is also determined by the current mirror (IC15d, e), with the result that the shunt PIN diode currents are inversely proportional to that in the series PIN diode, thereby maintaining the correct RF resistance relationship for a PI attenuator over the full control range.

Temperature compensation for the complete control circuit is provided by injecting a "temperature dependent" voltage into the non-inverting inputs of IC12a and IC12d.

4 THE IMAGE REJECT MIXER

The description for the Image Reject Mixer is given under the following headings

- The Second Mixer . . . . . Paragraph 4.1
- The Image . . . . . Paragraph 4.2
- Image Rejection Mixer . . . . . Paragraph 4.3

4.1 The Second Mixer

The first IF of 70.05 MHz gives the advantage of simplified RF filtering and excellent first image rejection, but the signal frequency must be reduced before digitisation can take place. This is done by a fixed frequency downconversion taking place in the second mixer, where the IF signal is mixed with the Second Local Oscillator (70 MHz) from Synthesiser 2.

4.2 The Image

The second IF of the receiver is very low compared with the first IF, which limits the degree of rejection provided by the crystal filter at the "image" response at 69.95 MHz (Second LO minus 50 kHz) where the rejection is typically 70 dB. In order to enhance the rejection an Image Rejection Mixer is employed which provides a minimum of 30 dB rejection.

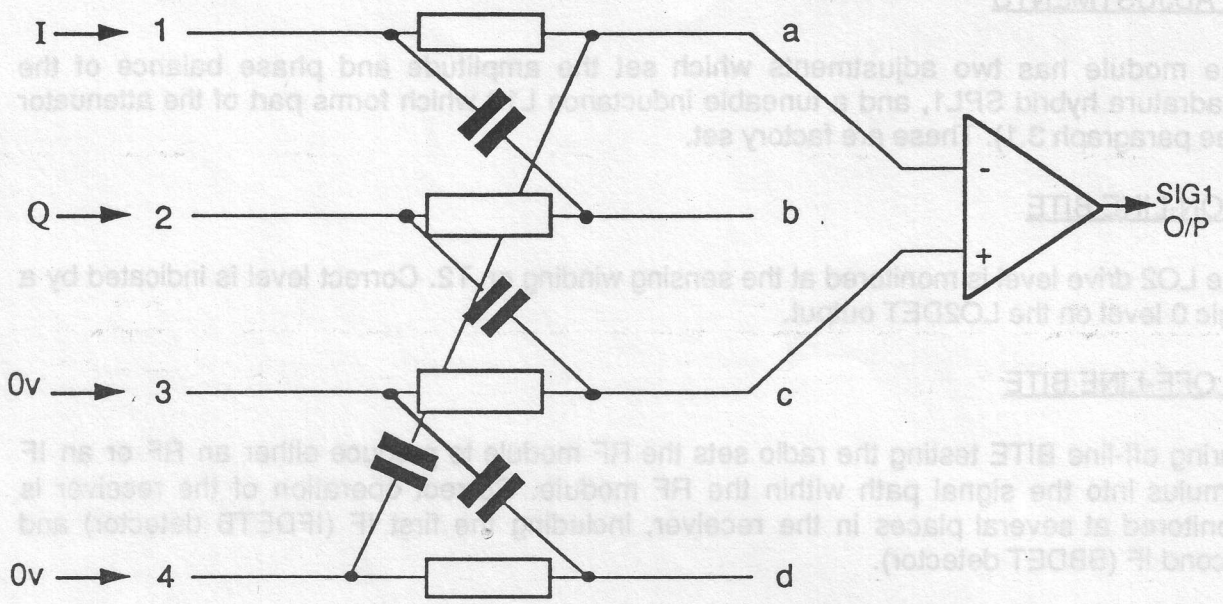
4.3 Image Rejection Mixer

The first section of the mixer is a hybrid splitter SPL1 which produces two outputs in quadrature. These signals are mixed with the LO2 signal in the mixers IC9 and IC10, which are arranged as commutating switches under control of the LO2 drive from T2 and T3, and the (IF - LO2) signal components at 50 kHz are fed as a current into the virtual earth input stages of the baseband pre-amplifiers formed by IC1, 3, 4 and IC2, 5, 6 respectively.

The mixer output signals are I and Q components of the downconverted signal. The I component is the same for wanted and "image" signals, but the mixing process puts the "image" Q component 180 degrees out of phase with the "wanted" Q component.

The polyphase network comprises four signal paths arranged so that over the passband the currents from the inputs to the outputs maintain a constant relative phase whereby the signals at **b**, **c**, and **d** are 90, 180 and 270 degrees phase offset with respect to **a**. The overall polyphase has three sections with nominal centre frequencies of 32, 50 and 62 kHz.

The basis of operation can be seen by examining a single section at a frequency $f=1/2\pi CR$.



Polyphase Network - Single Stage

The current from output **a** is the in-phase current from **1** while that at **c** is that from **2** but phase-leading by 90 degrees. Thus the wanted signal Q component is now 180 degrees out-of-phase with the I component at the input to the differential amplifier. Therefore the output SIG1 is the I and Q signals combined.

The image Q component, however, lags the I component by 90 degrees so that the signal at **c** is in-phase with that at **a** and therefore cancels at the input to the differential amplifier.

By cascading several sections the above phase relationship can be maintained over a wide frequency range.

5 ADJUSTMENTS

The module has two adjustments which set the amplitude and phase balance of the quadrature hybrid SPL1, and a tuneable inductance L10 which forms part of the attenuator (see paragraph 3.1). These are factory set.

6 ON-LINE BITE

The LO2 drive level is monitored at the sensing winding on T2. Correct level is indicated by a logic 0 level on the LO2DET output.

7 OFF-LINE BITE

During off-line BITE testing the radio sets the RF module to produce either an RF or an IF stimulus into the signal path within the RF module. Correct operation of the receiver is monitored at several places in the receiver, including the first IF (IFDETB detector) and second IF (BBDET detector).

To reduce the effect of loading on the signal path, IFDETB is only connected when ENABLEDET from the RF module is logic 1. A sufficient level of signal in the signal path during BITE is indicated by IFDETB output and BBDET output both being logic 1.

8 OPERATION WITHOUT LO2 SIGNAL

Since the image rejection mixers IC9 and IC10 operate as current switches into the virtual earth input of the following stage, the source impedance and hence the loop bandwidth of that stage are only defined if the LO signal is present. When LO2 is removed or absent due to a fault it is possible that oscillation of the succeeding stage will take place and will be indicated by BBDET output at logic 1.

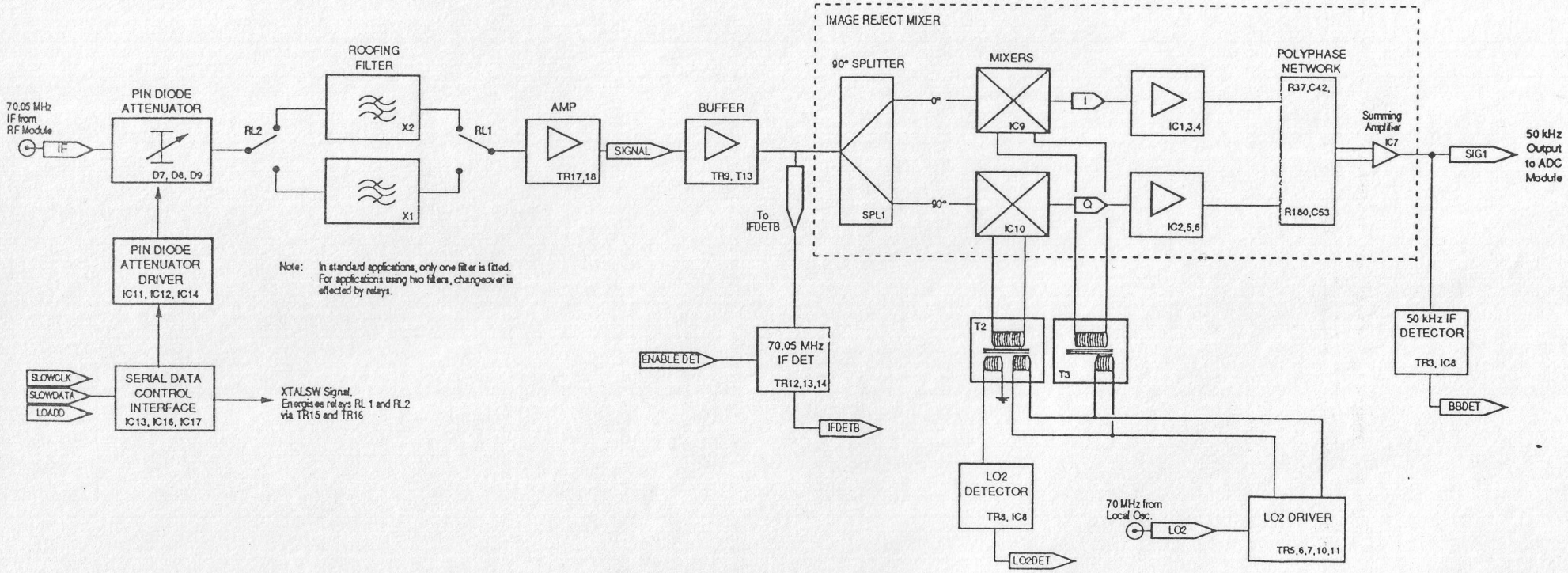


Figure 1 - IF Module Simplified Block Diagram

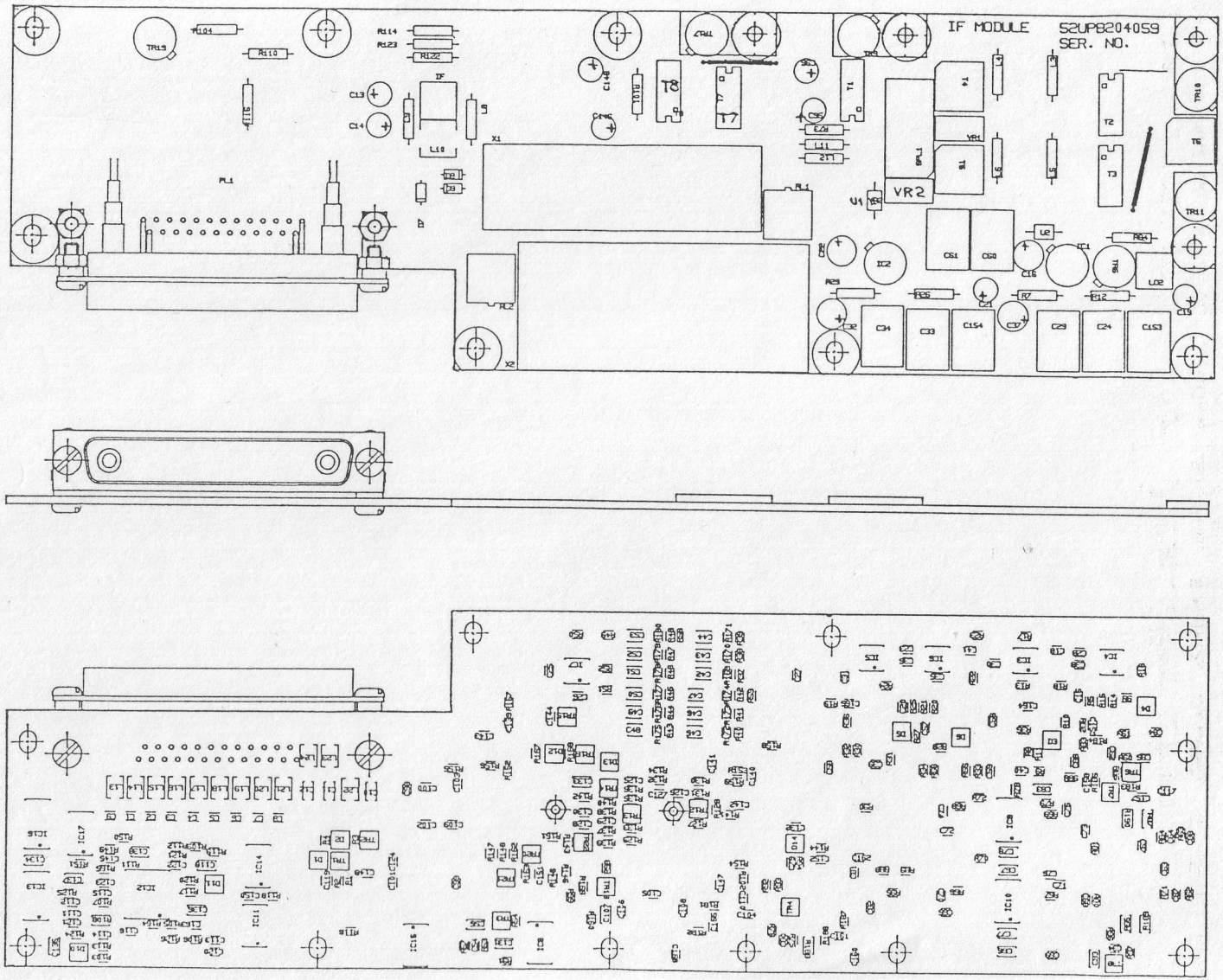


Figure 2 - IF Module Layout Diagram

Circuit Reference	Description	Value
C1 to C9	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C10 to C12	Capacitor, fixed, ceramic chip, 10%, 50V	100p
C13 & C14	Capacitor, fixed, al electrolytic 20%, 100V	1µ
C16	Capacitor, fixed, al electrolytic 20%, 100V	100µ
C18	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C19	Capacitor, fixed, al electrolytic 20%, 50V	10µ
C21	Capacitor, fixed, al electrolytic 20%, 50V	10µ
C22	Capacitor, fixed, al electrolytic 20%, 10V	100µ
C23	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C24	Capacitor, fixed, polyester, 5%, 63V	1µ
C25	Capacitor, fixed, ceramic chip, 5%, 100V	18p
C26 & C27	Capacitor, fixed, ceramic chip, 10%,100V	10n
C28	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C29	Capacitor, fixed, polyester, 5%, 63V	1µ
C30 & C31	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C32	Capacitor, fixed, al electrolytic 20%, 40V	33µ
C33 & C34	Capacitor, fixed, polyester, 5%, 63V	1µ
C35	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C36	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C37	Capacitor, fixed, al electrolytic 20%, 40V	33µ
C38 & C41	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C42 to C53	Capacitor, fixed, ceramic chip, 5%, 50V	4n7
C54	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C55	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C56 to C59	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C60 & C61	Capacitor, fixed, polyester, 5%, 63V	1µ
C62	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C63	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C64	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C65	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C66 & C67	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C68	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C69 to C71	Capacitor, fixed, ceramic chip, 5%, 100V	470p

Circuit Reference	Description	Value
C72 & C73	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C74 to C76	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C77 & C78	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C79 to C82	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C83	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C84	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C85	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C86	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C87 & C88	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C93	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C94	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C95	Capacitor, fixed, al electrolytic, 20%, 100V	1µ
C96	Capacitor, fixed, al electrolytic, 20%, 50V	10µ
C97	Capacitor, fixed, ceramic chip, 10%, 100V	4n7
C98 to C101	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C102	Capacitor, fixed, ceramic chip, 5%, 100V	10p
C103 to C106	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C107	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C108 & C109	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C110	Capacitor, fixed, ceramic chip, 5%, 100V	10p
C111 to C115	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C116	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C117	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C118	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C119 to C121	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C122 & C123	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C124	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C125	Capacitor, fixed, ceramic chip, 5%, 100V	56p
C126	Capacitor, fixed, ceramic chip, 5%, 100V	33p
C127 to C130	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C131	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C132	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C133 to C138	Capacitor, fixed, ceramic chip, 10%, 50V	100n

IF Module Items List - Sheet 2 of 9

Circuit Reference	Description	Value
C139 to C145	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C146	Capacitor, fixed, al electrolytic, 20%, 50V	10µ
C147	Capacitor, fixed, al electrolytic, 20%, 100V	1µ
C148	Capacitor, fixed, ceramic chip, 5%, 100V	33p
C149 to C151	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C152	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C153 & C154	Capacitor, fixed, polyester, 5%, 63V	680n
C155 & C156	Capacitor, fixed, ceramic chip, ±0.5p, 100V	2p2
C157 to C159	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C160 & C161	Capacitor, fixed, ceramic chip, ±0.5p, 100V	2p2
C162	Capacitor, fixed, ceramic chip, 5%, 100V	15p
C163	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C164 & C165	Capacitor, fixed, ceramic chip, 5%, 100V	47p
L3 to L6	Choke, fixed, RF, 10%	1µ
L8 & L9	Choke, fixed, RF, 10%	3µ3
L10	Choke, wound, special purpose	
L11 & L12	Choke, fixed, RF, 10%	1µ5
L13 to L21	Choke, fixed, chip, 10%	4µ7
L22	Choke, fixed, chip, 10%	10µ
L23	Choke, fixed, chip, 10%	15µ
L24	Choke, fixed, chip, 10%	39µ
IC1 & IC2	Super Matched Pair, LM394H	
IC3 to IC7	Low Noise Operational Amplifier, NE5534D	
IC8	Quad 2-Input NAND Schmitt Trigger, HEF4011BT	
IC9 & IC10	Double Balanced Mixer, Si8901Y	
IC11	Transistor Array, LM3086M	
IC12	Quad High Performance Operational Amplifier, NE5514D	
IC13	8 Bit D to A Converter, DAC08ED	
IC14 & IC15	Transistor Array, LM3086M	
IC16	8 Stage Shift and Store Bus Register, HEF4094BT	
IC17	Quad 2-Input NAND, HEF4011BT	

Circuit Reference	Description	Value
R1 to R4	Resistor, fixed, chip, 1%, 0.1W	3k3
R6	Resistor, fixed, chip, 1%, 0.1W	3k9
R7	Resistor, fixed, metal film, 1%, 0.25W	510R
R8	Resistor, fixed, chip, 1%, 0.1W	4k7
R7	Resistor, fixed, chip, 1%, 0.1W	10k
R8	Resistor, fixed, chip, 1%, 0.1W	100k
R10	Resistor, fixed, chip, 1%, 0.1W	1M
R11	Resistor, fixed, chip, 1%, 0.1W	2k2
R12	Resistor, fixed, metal film, 1%, 0.25W	30R
R13	Resistor, fixed, chip, 1%, 0.1W	470R
R14 & R15	Resistor, fixed, chip, 1%, 0.1W	4k7
R16	Resistor, fixed, chip, 1%, 0.1W	82k
R17	Resistor, fixed, chip, 1%, 0.1W	8k2
R18 & R19	Resistor, fixed, chip, 1%, 0.1W	470R
R20 & R21	Resistor, fixed, chip, 1%, 0.1W	4k7
R22	Resistor, fixed, chip, 1%, 0.1W	82k
R23	Resistor, fixed, chip, 1%, 0.1W	8k2
R24	Resistor, fixed, chip, 1%, 0.1W	470R
R26	Resistor, fixed, metal film, 1%, 0.25W	30R
R27	Resistor, fixed, chip, 1%, 0.1W	1M
R28	Resistor, fixed, chip, 1%, 0.1W	3k9
R29	Resistor, fixed, metal film, 1%, 0.25W	510R
R30	Resistor, fixed, chip, 1%, 0.1W	2k2
R31	Resistor, fixed, chip, 1%, 0.1W	1k2
R32	Resistor, fixed, chip, 1%, 0.1W	4k7
R34	Resistor, fixed, chip,	0R
R35 & R36	Resistor, fixed, chip, 1%, 0.1W	4k7
R38	Resistor, fixed, chip, 1%, 0.1W	1k1
R39	Resistor, fixed, chip, 1%, 0.1W	2k
R40	Resistor, fixed, chip, 1%, 0.1W	1k2
R41	Resistor, fixed, chip,1%, 0.1W	1k1
R42	Resistor, fixed, chip, 1%, 0.1W	2k
R43	Resistor, fixed, chip, 1%, 0.1W	1k2

Circuit Reference	Description	Value
R44	Resistor, fixed, chip, 1%, 0.1W	1k1
R45	Resistor, fixed, chip, 1%, 0.1W	2k
R46	Resistor, fixed, chip, 1%, 0.1W	1k2
R47	Resistor, fixed, chip, 1%, 0.1W	1k1
R48	Resistor, fixed, chip, 1%, 0.1W	2k
R49	Resistor, fixed, chip, 1%, 0.1W	4k7
R50	Resistor, fixed, chip, 1%, 0.1W	10k
R51	Resistor, fixed, chip, 1%, 0.1W	4k7
R52	Resistor, fixed, chip, 1%, 0.1W	10k
R53 & R54	Resistor, fixed, chip, 1%, 0.1W	100k
R55	Resistor, fixed, chip,	0R
R57	Resistor, fixed, chip, 1%, 0.1W	22k
R58 & R59	Resistor, fixed, chip, 1%, 0.1W	4k7
R60	Resistor, fixed, chip, 2%, 0.1W	22R
R61	Resistor, fixed, chip, 2%, 0.1W	47R
R62	Resistor, fixed, chip, 2%, 0.1W	82R
R63	Resistor, fixed, chip, 2%, 0.1W	22R
R64	Resistor, fixed, chip, 2%, 0.1W	82R
R65	Resistor, fixed, chip, 5%, 0.25W	2k2
R66 to R69	Resistor, fixed, chip, 2%, 0.1W	47R
R70	Resistor, fixed, chip, 1%, 0.1W	100k
R71	Resistor, fixed, chip, 2%, 0.1W	22R
R72	Resistor, fixed, chip, 1%, 0.1W	100k
R73	Resistor, fixed, metal film, 1%, 0.25W	33R
R75	Resistor, fixed, chip, 1%, 0.1W	22R
R76	Resistor, fixed, chip, 2%, 0.1W	51R
R78	Resistor, fixed, chip, 1%, 0.1W	2k2
R79	Resistor, fixed, chip, 1%, 0.1W	680R
R80 & R81	Resistor, fixed, chip, 1%, 0.1W	100k
R82	Resistor, fixed, chip, 1%, 0.1W	150R
R83	Resistor, fixed, chip, 1%, 0.1W	1k2
R84	Resistor, fixed, metal film, 1%, 0.25W	330R
R85 & R86	Resistor, fixed, chip, 1%, 0.1W	2k7

Circuit Reference	Description	Value
R87	Resistor, fixed, chip, 5%, 0.25W	2k2
R88	Resistor, fixed, chip, 1%, 0.1W	100R
R89	Resistor, fixed, chip, 2%, 0.1W	10R
R90	Resistor, fixed, chip, 2%, 0.1W	68R
R91	Resistor, fixed, chip, 1%, 0.1W	100k
R92	Resistor, fixed, chip, 2%, 0.1W	10R
R93	Resistor, fixed, metal film, 1%, 0.1W	2k7
R94	Resistor, fixed, metal film, 1%, 0.1W	10k
R95	Resistor, fixed, chip, 1%, 0.1W	10M
R96	Resistor, fixed, chip, 5%, 0.25W	330R
R97	Resistor, fixed, chip, 1%, 0.1W	470R
R98	Resistor, fixed, chip, 1%, 0.1W	1k
R99	Resistor, fixed, chip, 2%, 0.1W	10R
R101	Resistor, fixed, metal chip, 1%, 0.25W	43R
R102	Resistor, fixed, metal chip, 2%, 0.1W	47R
R103	Resistor, fixed, chip, 1%, 0.1W	360R
R104	Resistor, fixed, chip, 1%, 0.25W	1k2
R105	Resistor, fixed, chip, 1%, 0.1W	120R
R106	Resistor, fixed, chip, 1%, 0.1W	360R
R107	Resistor, fixed, chip, 1%, 0.1W	1k
R108	Resistor, fixed, chip, 5%, 0.25W	1k
R109	Resistor, fixed, chip, 1%, 0.1W	100k
R110	Resistor, fixed, metal film, 1%, 0.25W	33R
R111 to R113	Resistor, fixed, chip, 1%, 0.1W	1M
R114	Resistor, fixed, metal film, 1%, 0.25W	510R
R115	Resistor, fixed, metal film, 1%, 0.25W	330R
R116	Resistor, fixed, chip, 1%, 0.1W	18k
R117	Resistor, fixed, chip, 1%, 0.1W	15k
R118	Resistor, fixed, chip, 1%, 0.1W	18k
R119	Resistor, fixed, chip, 1%, 0.1W	10k
R120	Resistor, fixed, chip, 1%, 0.1W	7k5
R121	Resistor, fixed, chip, 1%, 0.1W	18k
R122 & R123	Resistor, fixed, metal film, 1%, 0.25W	2k7

Circuit Reference	Description	Value
R124	Resistor, fixed, chip, 1%, 0.1W	360R
R125	Resistor, fixed, chip, 1%, 0.1W	470R
R126	Resistor, fixed, chip, 1%, 0.1W	220R
R127	Resistor, fixed, chip, 1%, 0.1W	8k2
R128	Resistor, fixed, chip, 1%, 0.1W	3k3
R129	Resistor, fixed, chip, 1%, 0.1W	1k
R130	Resistor, fixed, chip, 1%, 0.1W	150R
R131	Resistor, fixed, chip, 2%, 0.1W	39R
R132	Resistor, fixed, chip, 1%, 0.1W	220R
R133	Resistor, fixed, chip, 1%, 0.1W	8k2
R134	Resistor, fixed, chip, 1%, 0.1W	3k3
R135	Resistor, fixed, chip, 1%, 0.1W	150R
R136	Resistor, fixed, chip, 2%, 0.1W	27R
R137	Resistor, fixed, chip, 1%, 0.1W	1k
R138	Resistor, fixed, chip, 2%, 0.1W	47R
R139	Resistor, fixed, chip, 1%, 0.1W	43k
R140	Resistor, fixed, chip, 1%, 0.1W	1k
R141	Resistor, fixed, chip, 1%, 0.1W	470R
R142	Resistor, fixed, chip, 1%, 0.1W	100k
R143	Resistor, fixed, chip, 1%, 0.1W	10k
R144	Resistor, fixed, chip, 1%, 0.1W	470R
R145	Resistor, fixed, chip, 1%, 0.1W	2k2
R146	Resistor, fixed, chip, 1%, 0.1W	47k
R147 & R148	Resistor, fixed, chip, 1%, 0.1W	10k
R149 to R151	Resistor, fixed, chip, 1%, 0.1W	47k
R152 to R155	Resistor, fixed, chip, 1%, 0.1W	1k
R156 to R159	Resistor, fixed, chip, 1%, 0.1W	4k7
R160	Resistor, fixed, chip, 1%, 0.1W	2k7
R161 to R164	Resistor, fixed, chip, 1%, 0.1W	10k
R165	Resistor, fixed, chip, 1%, 0.1W	910k
R166 & R167	Resistor, fixed, chip, 1%, 0.1W	10k
R168	Resistor, fixed, chip, 1%, 0.1W	1k
R169	Resistor, fixed, chip, 1%, 0.1W	1k5

Circuit Reference	Description	Value
R170	Resistor, fixed, chip, 1%, 0.1W	1k1
R171	Resistor, fixed, chip, 1%, 0.1W	2k2
R172	Resistor, fixed, chip, 1%, 0.1W	1k5
R173	Resistor, fixed, chip, 1%, 0.1W	1k1
R174	Resistor, fixed, chip, 1%, 0.1W	2k2
R175	Resistor, fixed, chip, 1%, 0.1W	1k5
R176	Resistor, fixed, chip, 1%, 0.1W	1k1
R177	Resistor, fixed, chip, 1%, 0.1W	2k2
R178	Resistor, fixed, chip, 1%, 0.1W	1k5
R179	Resistor, fixed, chip, 1%, 0.1W	1k1
R180	Resistor, fixed, chip, 1%, 0.1W	2k2
R181	Resistor, fixed, chip, 2%, 0.1W	47R
R182	Resistor, fixed, chip, 2%, 0.1W	10R
R183	Resistor, fixed, chip, 1%, 0.1W	100R
R184	Resistor, fixed, chip, 1%, 0.1W	150R
R185	Resistor, fixed, chip, 1%, 0.1W	620R
R186	Resistor, fixed, chip, 2%, 0.1W	47R
R187	Resistor, fixed, chip, 2%, 0.1W	10R
R188	Resistor, fixed, chip, 5%, 0.25W	6R8
R189 & R190	Resistor, fixed, chip, 5%, 0.25W	2k2
R191	Resistor, fixed, metal film, 2%, 0.125W	51R
VR1	Resistor, variable, 10%, 0.5W	1k
VR2	Resistor, variable, 10%, 0.5W	200R
D1 & D2	Diode, Zener, BZX84C13	
D3	Diode Schottky, ZC5800E	
D4	Diode, BAV70	
D5	Diode Schottky, ZC5800E	
D6	Diode, BAV70	
D7 to D9	Diode, PIN, IN5767	
D10	Diode, BAV70	
D11	Diode, Zener, BZX84C13	

Circuit Reference	Description	Value
D12 & D13	Diode, silicon, planar high speed switching, BAS16	
D14	Diode, BAT18	
TR1	Transistor, NPN, BCW31	
TR2	Transistor, PNP, BCW30	
TR3	Transistor, NPN, BCW31	
TR4	Transistor, PNP, BCW30	
TR5	Transistor, RF Linear, LT10001A	
TR6	Transistor, RF Broad Band, BFS17	
TR7	Transistor, PNP, BSR12	
TR8	Transistor, RF Broad Band, BFS17	
TR9 to TR11	Transistor, RF Linear, LT10001A	
TR12 to TR14	Transistor, RF Broad Band, BFS17	
TR15 & TR16	Transistor, N-Channel, VN10LF	
TR17	Transistor, RF Linear, LT10001A	
TR18	Transistor, PNP, BCW30	
TR19	Transistor, NPN, BFY50	
TR20	Transistor, NPN, BCW31	
TR21 & TR22	Transistor, NPN, BCW30	

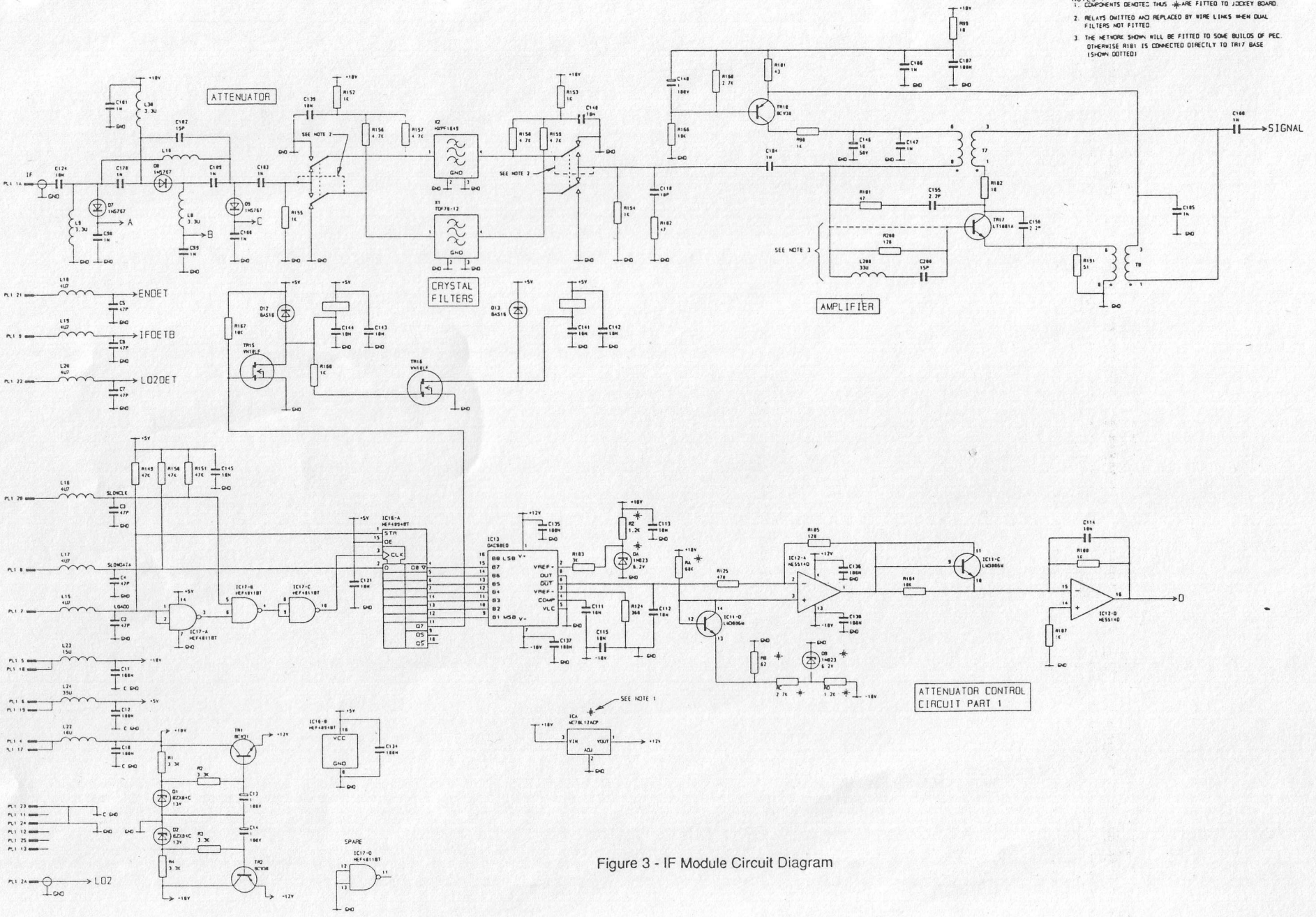


Figure 3 - IF Module Circuit Diagram

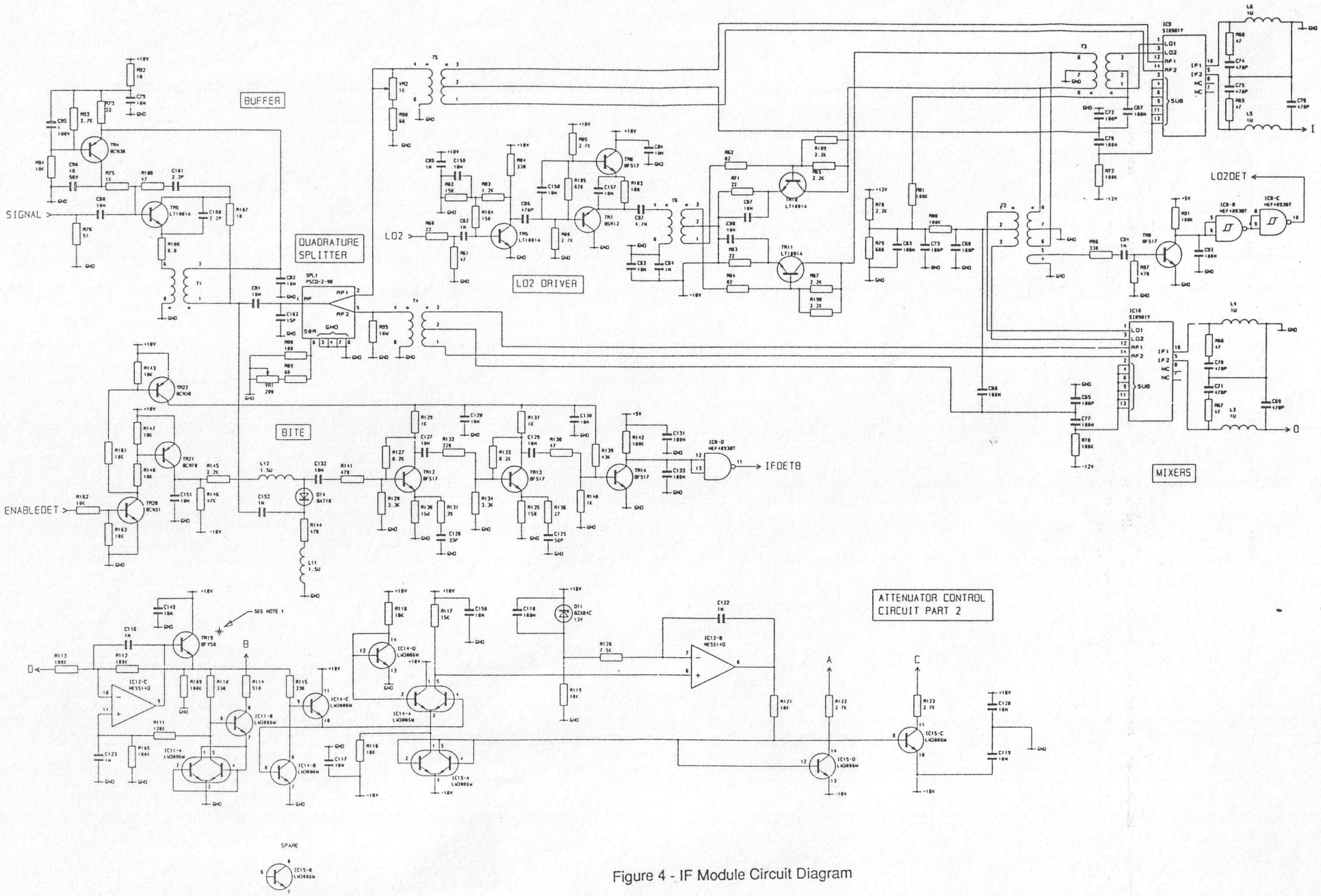


Figure 4 - IF Module Circuit Diagram

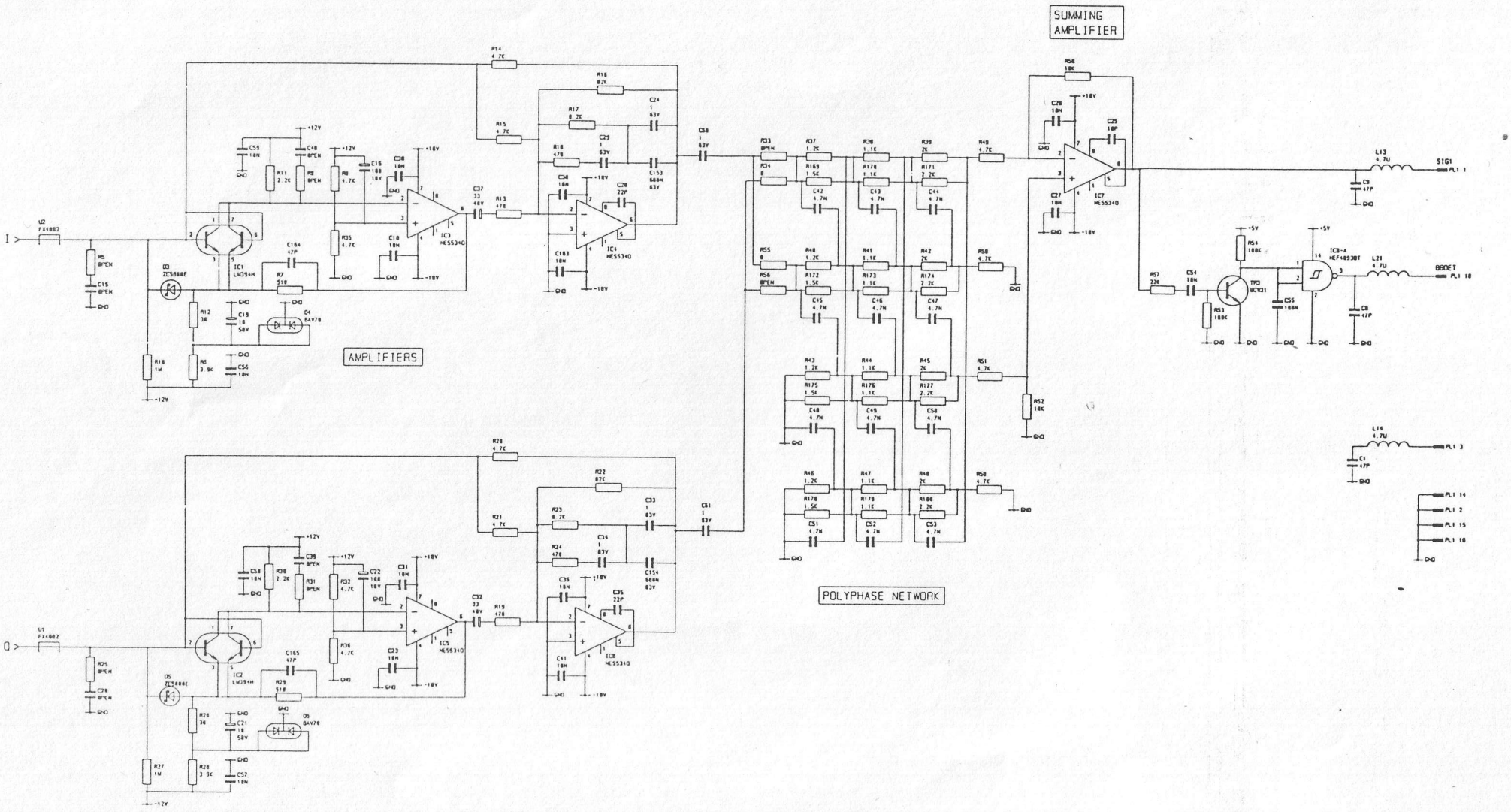


Figure 5 - IF Module Circuit Diagram

Chapter 6.3

SYNTHESISER 1

1 INTRODUCTION

The Synthesiser 1 Module comprises 3 PCBs and a VCO sub assembly housed in a screened enclosure. The 3 PCBs are:

- Buffer Board 52UPB504084
- Interpolation Board 52UPB504083
- Loop Board 52UPB504071

The VCO sub assembly is housed in a separate compartment within the module and comprises the following PCBs:

- VCO Board 52UPB504087
- Varactor Board 52YPB204093
- VCO Pin Board 52YPB204094.

Synthesiser 1 provides the main tuning signal in the receiver over the frequency range 70.050000 MHz to 110.050000 MHz with a step size of 1 Hz.

This is achieved by means of a single loop frequency synthesiser with a phase detector reference frequency of 1 MHz, derived from the receiver's main frequency standard.

A variation of the well publicised 'Fractional-N' technique involving the use of Digital Signal Processing gives a fine resolution of 1 Hz from what would normally be a 1 MHz step synthesiser.

The VCO Module, buffer board and loop board provides the basic Phase Lock Loop. The Interpolation board carries the Digital Signal Processing and Digital Control Circuits.

Module description is given with reference to the following drawings/illustrations and items list:

- Figure 1 Synthesiser 1 Simplified Block Diagram
- Figure 2 Adjustments
- Figure 3 Look-up Table Inputs and Outputs
- Figure 4 VCO Board Component Layout
- Figure 5 VCO Varactor and Pin Board Component Layout
- Figure 6 Interpolation Board Component Layout
- Figure 7 Loop Board Component Layout
- Figure 8 Buffer Board Component Layout
- Items List VCO Board, Sheets 1 to 4 inc.
- Items List VCO Pin Board, Sheet 1
- Items List VCO Varactor Board, Sheet 1
- Items List Buffer Board, Sheet 1
- Items List Interpolation Board, Sheets 1 to 2 inc.
- Items List Loop Board, Sheets 1 to 3 inc.
- Figure 9 Synthesiser 1 Module Interconnection Diagram
- Figure 10 VCO Board Circuit Diagram
- Figure 11 Phase Detector Circuit Diagram

- Figure 12 Loop Filter Circuit Diagram
- Figure 13 EXT LO Switch
- Figure 14 Controller Interface
- Figure 15 Swallow Counter
- Figure 16 Count Loader
- Figure 17 Reference Interface
- Figure 18 Count Modifier
- Figure 19 Buffer
- Figure 20 BITE Monitor

2 CIRCUIT DESCRIPTION

Circuit description is given under the following headings:

- VCO Module . . . . . Paragraph 2.1
- Buffer Board . . . . . Paragraph 2.2
- Loop Board . . . . . Paragraph 2.3
- Interpolation Board . . . . . Paragraph 2.4

2.1 VCO Module (52UQT004005)

This unit generates the RF signal which is output from the synthesiser. Two logic input signals determine which of the four frequency bands the signal is generated in. These are produced by PIN diode switched inductors tapped on the main resonator inductor. The band details are shown in the following table:

Frequency Band	Logic Input Band 0	Logic Input Band 1
70 - 80 MHz	0.0 - 0.5V	0.0 - 0.5V
80 - 90 MHz	2.4 - 5.5V	0.0 - 0.5V
90 - 100 MHz	0.0 - 0.5V	2.4 - 5.5V
100 - 110 MHz	2.4 - 5.5V	2.4 - 5.5V

Fine frequency control within each band is achieved by means of varactor tuning. The input is via a co-axial cable from the Loop Filter output. The steady state voltage on this input is between -11.5V and +11.5V. This voltage is accessible on a buffered output at the underside of CON2A/12 on the Interpolation Board.

There are two buffered RF outputs from the module on co-axial cables (RFOUT1 and RFOUT2 on Figure 2). The power output at both should be greater than +4 dBm.

2.2 Buffer Board 52UPB504084

The Buffer board accepts the two RF outputs from the VCO module. Its purpose is to provide RF isolation, to prevent unwanted signals from entering the VCO via its RF outputs. This prevents spurious sidebands from being generated on the VCO output.

The board also provides a level of filtering to the DC and band select inputs to the VCO.

When the Buffer board is driven by the VCO, a minimum power of +3 dBm should be obtained on both RF outputs to the synthesiser main connector. The other RF output, which drives the Loop Divider, should be at a level of -2 dBm minimum.

2.3 Loop Board (52UPB504071)

The Loop Board carries the other elements that make up the basic Phase Locked Loop (PLL) and contains the following:

2.3.1 Loop Divider (Swallow Counter)

This determines the VCO output frequency at which the loop is locked, by dividing its RF input frequency to an average of 1 MHz. The divider input is interfaced to the Buffer Board output

by a limiting amplifier. The Loop Divider output is fed as one of the inputs to the Phase Comparator.

The divider is a dual modulus counter, or swallow counter, made up of a prescaler with a selectable 8/9 division ratio, and two programmable counters.

The division ratio is determined by two digital words loaded to these counters from a PROM, in accordance with the following formula:

Division Ratio (N) = 8 (16 - M) + (15 - A)

Where A and M are the decimal values of the binary words loaded to the A and M counters.

2.3.2 Phase Comparator

This is a conventional type of phase-frequency comparator using D-type Flip-Flops. The loop divider output is compared with the 1 MHz input from the reference divider producing two output signals. These are fed to the loop filter inputs.

The problem of noise and spurious signals introduced by the non-linear nature of this type of phase detector at the zero phase crossing is overcome by summing a DC offset set by a potentiometer into one side of the phase detector output.

2.3.3 Loop Filter

The Loop Filter consists of an active integrator/lead - lag network, followed by a 2nd order active low pass filter. The final stage of the loop filter is a passive lag - lead - lag network.

The pole - zero frequencies were determined to give a closed loop bandwidth of 500 Hz when the synthesiser is locked. During locking, the pole - zero frequencies and active LPF cutoff frequencies are altered to increase the closed loop bandwidth so reducing the time taken to achieve lock.

2.3.4 Reference Divider

A 20 MHz sinewave clock from the Reference Module is input to the synthesiser, at a level of +6 dBm, via a co-axial socket in the main connector.

This input is converted to 5V logic, then divided in two counter stages to 1 MHz. The output provides a reference signal for the phase comparator.

A buffered 20 MHz logic output provides a clock for the Digital Signal Processing (DSP) section.

2.4 Interpolation Board (52UPB504083)

The Interpolation Board carries the DSP and digital control circuitry in the synthesiser.

The main input is the serial data bus originating from the controller card in the receiver (for timing details see Chapter 6.16 Internal Interfaces).

Frequency data is extracted from the input stream and manipulated into a form to drive the loop divider on the loop board.

Synthesiser BITE commands are also extracted from the data bus, and processed by the Interpolation Board.

2.4.1 Bus Interface Circuit

This consists of some simple logic to route the serial bus input data, clock and load pulses to the areas of circuitry that require them. The clocks output to each area are gated by the relevant load pulse.

2.4.2 DSP Circuit

The DSP circuit accepts the fractional part of the tuned frequency (when expressed in MHz) input on the serial data bus. Depending on the value of this, it computes a stream of numbers in a serial format. This data is then converted to a 3 bit parallel word and output at a rate of 500 kHz synchronised to the 1 MHz reference clock on the B0, B1 and B2 lines.

2.4.3 Frequency Decoder and Look Up Table

This section of circuitry accepts frequency data input from the bus and DSP and converts it to the form required by the loop divider A and M counters.

The integer part of the receiver tuned frequency and most significant bit of the fractional part routed from the bus interface circuit are converted to a 9 bit binary word. This is used as the least significant 9 address bits to a PROM containing a look up table.

The most significant 3 bits of the 12 bit address are those output from the DSP circuit.

The data output from the PROM is re-synchronised to the 1 MHz reference clock by a latch before being output to the loop divider. The PROM also supplies the frequency band data for the VCO module.

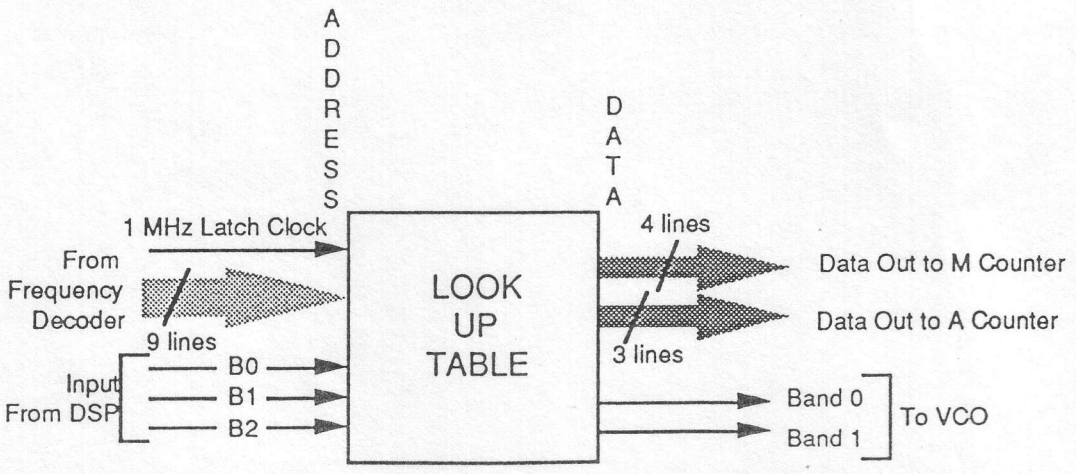


Figure 3 Look-up Table Inputs and Outputs

2.4.4 BITE Monitor Circuit

On Line BITE

A buffered version of the VCO control line voltage is fed to this area of circuitry from the loop board. This voltage is continually monitored by means of comparators to check that it stays within the VCO operating limits of -11.5V to +11.5V. If it does not, indicative of an 'out of lock' condition, the BITE line is set to logic high. This signal is fed out of the synthesiser on the main connector back to the receiver controller board, which recognises the fault.

Off Line BITE

Under control of the BITE load pulse, (LOAD G), serial data is extracted from the data bus and converted to an analogue voltage by means of a shift register and DAC. This is compared with the VCO control voltage, and the BITE output bit set according to which voltage is the largest.

3 PRINCIPLES OF OPERATION

Principles of Operation is given under the following headings:

- Simplified Case Analogous to a Normal Synthesiser . . . . . Paragraph 3.1
- Fractional Offset Sequence . . . . . Paragraph 3.2
- Generating the Fractional Offset Frequency from the Sequence . Paragraph 3.3

3.1 The Simplified Case Analogous to a Normal Synthesiser

Operation of the module, excluding the effect of the DSP, is straightforward and is similar to any other single loop frequency synthesiser with a step size of 1 MHz.

The receiver operating frequency is input to the synthesiser on the serial data bus. The integer (MHz) part of the frequency is fed to a look-up table. This decodes the receiver frequency to the synthesiser operating frequency in terms of the data needed by the two counters in the loop divider (see paragraph 2.3.1).

For example, if the receiver were tuned to 19 MHz, the synthesiser would need to be at a (integer) frequency of 19 + 70 = 89 MHz, and the division value (N) would be 89, since the reference (phase detector) frequency is 1 MHz.

The VCO would need to operate in the 80 - 90 MHz band. To do this, the look up table generates a logic high on the B0 output and a logic low on the B1 output.

3.2 The Fractional Offset Sequence

Assuming that the receiver is still tuned to 19 MHz, the absolute frequency that the synthesiser must generate is 89.050000 MHz. The integer part and most significant fractional bit of the frequency data is fed to the look-up table, and the fractional part to the DSP.

The DSP in response to this input generates a sequence of 3 bit words at a rate of 500 kHz, synchronised to the 1 MHz reference. Each 3 bit word can assume 1 of 6 different values. These 3 data bits are then used with the 8 bit representation of the integer frequency and single most significant fractional bit, to address the look-up PROM.

In the PROM, for each integer frequency there are 6 possible address locations that can be reached, dependent upon the instantaneous value of the 3 bit word from the DSP.

The data contained in these 6 locations are the A and M counter load values for the following synthesiser frequencies:

Fint - 5, Fint - 3, Fint - 1, Fint + 1, Fint + 3, Fint + 5 MHz

Where Fint is the integer frequency, in this case 89 MHz.

In the case where the fractional part of the frequency is 524288 Hz or more, the most significant fractional bit is high. This causes a different part of the look-up table to be addressed, and the 6 frequencies become:

Fint - 4, Fint - 2, Fint, Fint + 2, Fint + 4, Fint + 6 MHz

4.3 Generating the Fractional Offset Frequency from the Sequence

When a PLL is in lock, the VCO frequency is constantly adjusted such that the phase of the divided down VCO signal is constant with respect to that of the reference (in this case 0 radians). If the division ratio is changed, in time the loop responds by adjusting the VCO frequency to re-establish the phase continuity between the divider output and reference signal.

However, if the division ratio is varied at a rate in excess of the loop bandwidth, the VCO will no longer track the changes with discrete frequency steps, but will respond to the average value of division ratio, or in this case, the average value of the sequence.

Consequently the synthesiser output frequency is determined by the time average of the sequence of division ratios. As the phase detector frequency is 1 MHz, the division ratio is numerically the same as the output frequency. For example:

To synthesise the frequency 89.000000 MHz, the sequence would be made up with the following numbers:

84, 86, 88, 90, 92, 94

Since the average of these numbers is 89, the sequence would have to contain the same number of 88s as 90s, 86s as 92, and 84s as 92s. So the sequence might be:

84, 94, 86, 92, 88, 90 ...repeated

or

84, 90, 88, 92, 88, 90, 86, 90, 88, 94, 88, 90 ...repeated

To synthesise the frequency 89.500000 MHz, clearly the number of occurrences of 90, 92 and 94 will not equal that of 84, 86 and 88. In its simplest form the sequence may be made up of a 3:1 ratio of 90s to 88s, eg:

90, 90, 88, 90, 90, 88, 90, 90 ...repeated

In practice, the sequence would be longer than this, and involve more of the 6 possible division ratios, in order to minimise the level of any discrete spurii, eg:

90, 88, 90, 92, 88, 90, 84, 90, 92, 88, 92, 90 ...repeated.

5 A GUIDE TO FAULT FINDING SYNTHESISER 1

It is possible to carry out a number of simple tests on the synthesiser module in order to determine if and where a fault lies. Fault Finding Guide is given under the following headings:

- Output Frequency Fault . . . . . Paragraph 5.1
- Fault Location Table . . . . . Paragraph 5.2
- Output RF Level Faults . . . . . Paragraph 5.3
- Fault Find the Basic Loop . . . . . Paragraph 5.4
- Interpolation Board Tests: DSP Reset and Inhibit . . . . . Paragraph 5.5

5.1 Output Frequency Fault

The most likely type of fault with such a module is that it fails to generate the correct frequency.

In the worst case, the PLL will not be locked, as indicated by the receiver's BITE warning.

5.2 Fault Location Table

Incorrect Output Frequency							
Non-Lock Indicated by BITE 'Fault' Legend				Not Indicated by BITE 'Fault' Indicator			
Tunes		Does Not Tune		Tunes		Does Not Tune	
4 spot freqs. only Freq. drifts	Coverage limited	Freq. drifts	Freq. stable	1 MHz step only	Non-specific step Freq. un-stable	At all	4 spot freqs. only
See A	See B	See A	See C	See D	See E	See F	See G

A: Other Symptoms

True Out Of Lock.
VCO tunes by band switching only.
VCO control line voltage less than -11.5V or greater than +11.5V.

Causes

Fault unlikely to lie with Interpolation Board.
Fault could be:

1. Loop Filter.
2. 1 MHz Clock not reaching Phase Detector.
3. Loop Divider.
4. Buffer Board RF drive to Loop Divider low.

B: Other Symptoms

Fine tuning possible, but not over full frequency range.

Causes

Band switching logic signals not reaching VCO. Check output at Interpolation Board (CON 2A pins 10 & 11) and at VCO box wall feedthroughs (Figure 1 and 2).

C: Other Symptoms

Output frequency is 71.000 MHz if Cause 1 or 2 below:

Causes

1. Serial data not reaching Synthesiser module from Controller Board due to bus fault. Check for frequency display tuning.
2. Serial data not reaching Interpolation Board due to faulty connections between main connector and board connector.
3. Interpolation Board fault.

D: Other Symptoms

DSP output bits B0, B1, B2 latched high (test points at P41 - P43). Indicates DSP inoperative.

Causes

1. DSP crashed. Power up reset, or reset Interpolation Board by shorting across 'RESET' pad.

2. 20 MHz clock not reaching DSP. Check 20 MHz clock to Interpolation Board connector (CON3B) on Loop Board with Interpolation board removed for 20 MHz logic levelled signal.

E: Other Symptoms

Frequency unstable when viewed with Spectrum Analyser.

Causes

1. Loop Filter fault.
2. VCO fault.

F: Other Symptoms

Output frequency may be 71.000 MHz if Cause 1 below. Fault indicated by Off-Line BITE.

Causes

1. Frequency data not reaching Synthesiser. Bus fault.
2. Interpolation Board fault.
3. Power supply rail fault.

G: AS 'A', or, BITE circuit fault on Interpolation Board.

5.3 Output RF Level Faults

This type of fault may exist in conjunction with an output frequency fault.

5.4 Fault Location Table

No RF Output	RF Output Level Low	
VCO Fault	VCO Fault	Buffer Board Amplifier Fault
+18V/-18V Supply Down		

5.5 Fault Finding the Basic Loop

It is possible to operate the synthesiser with the Interpolation Board removed, by programming the A and M counters in the Loop Divider using external switches, connected to the 'CON 2B' socket on the Loop Board.

These must be wired to switch logic high and low levels (0 and 5V) to all inputs including band switch lines 'BAND 0' and 'BAND 1', allowing a 1 MHz step size to be obtained without an Interpolation Board.

Some examples of switch input codes for various frequencies are given in the following table:

Frequency	A and M Counter Input Logic Levels							Band	
	A0	A1	A2	M0	M1	M2	M3	B0	B1
75.000 MHz	0	0	1	1	1	1	0	0	0
85.000 MHz	0	1	0	0	1	1	0	1	0
95.000 MHz	0	0	0	1	0	1	0	0	1
105.000 MHz	0	1	1	1	1	0	0	1	1

5.6 Interpolation Board Tests: DSP Reset and Inhibit

Once the Synthesiser is running, the DSP may be reset by momentarily short circuiting the 'RESET' pads on the Interpolation Board, (see Figure 6 Interpolation Board Component Layout). This provides a useful indicator that the DSP is working, since the frequency should change such that the MHz part remains the same, but the fractional part becomes 0.100 MHz. Additionally, the DSP may be checked for life by checking the DSP output bits B0, B1, B2 (test points at P41 - P43) with an oscilloscope. They should be alternating in logic level.

The frequency decoder and look-up table sections of circuitry may be tested independent of the DSP by placing a shorting jumper across the 'INHIBIT' pins (JP1) on the Interpolation Board. This has the effect of holding B0-B3 high, and thus only allowing 1 MHz step operation from the frequency bus.

6 ADJUSTMENTS

Adjustments are given under the following headings with reference to Figure 2.

- VCO Module . . . . . Paragraph 6.1
- Operating Frequency . . . . . Paragraph 6.2
- RF Output Power . . . . . Paragraph 6.3

6.1 VCO Module

There are several parameters which may be adjusted on the VCO module. However, these are factory set, and should require no further adjustments.

Details are included here for completeness and diagnostic purposes only.

6.2 Operating Frequency

This is adjusted by means of C14 (see Figure 2) and affects the output frequency on all 4 bands for a given control voltage. The correct setting is that where an output frequency of 77.20 MHz is obtained in the 70-80 MHz band for a control line voltage of 0.0V.

Once set, an output frequency of 86.6 MHz should be obtained in the 80-90 MHz band for a control line voltage of 0.0V. If not, this may be adjusted using C36 (see Figure 2).

6.3 RF Output Power

RF output power is set at an operating frequency of 88.0 MHz in the 80-90 MHz band. There is an adjustment for each of the two outputs, L27 for RFOUT1, and L28 for RFOUT2. The level should be a minimum of 4.0 dBm.

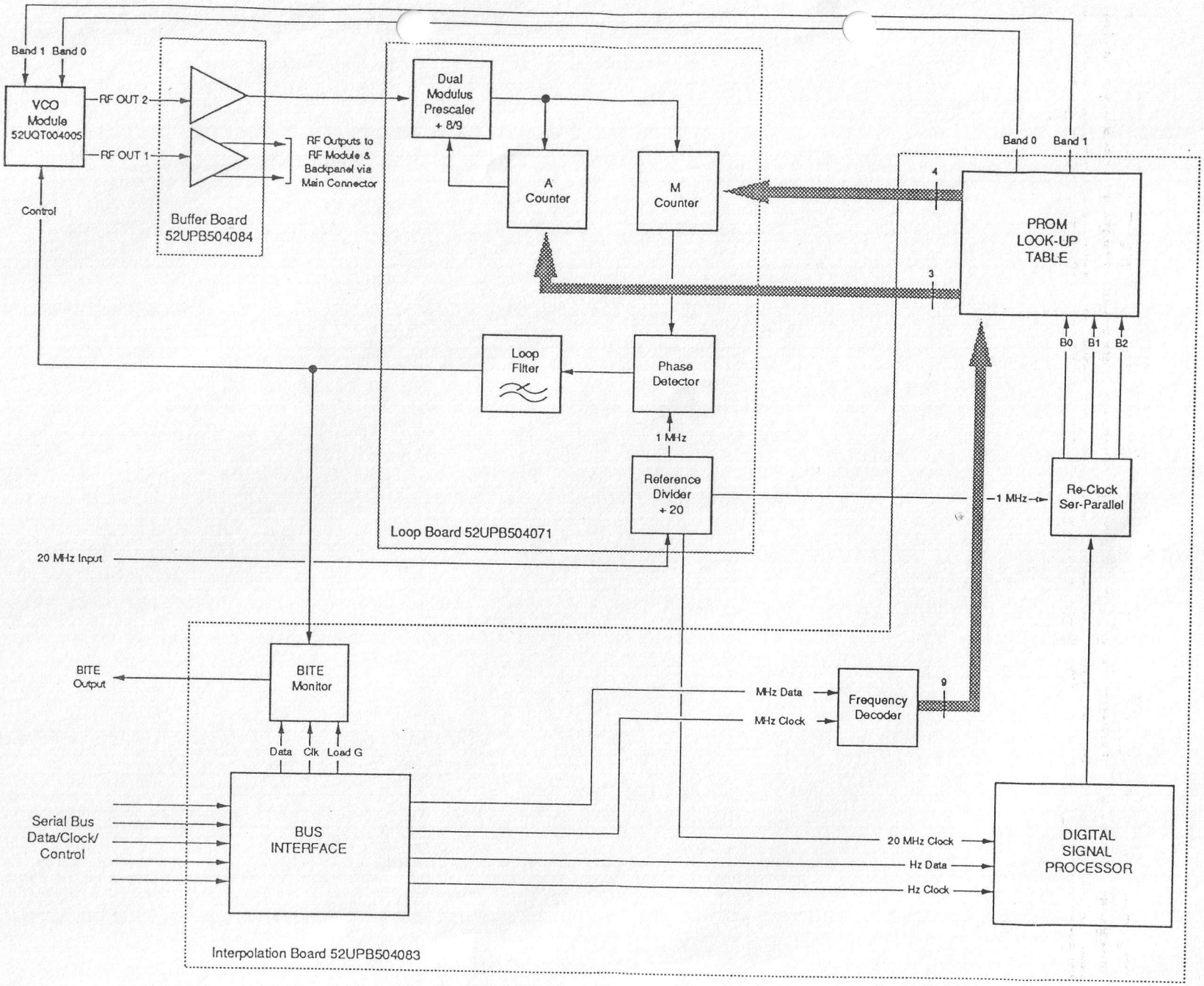
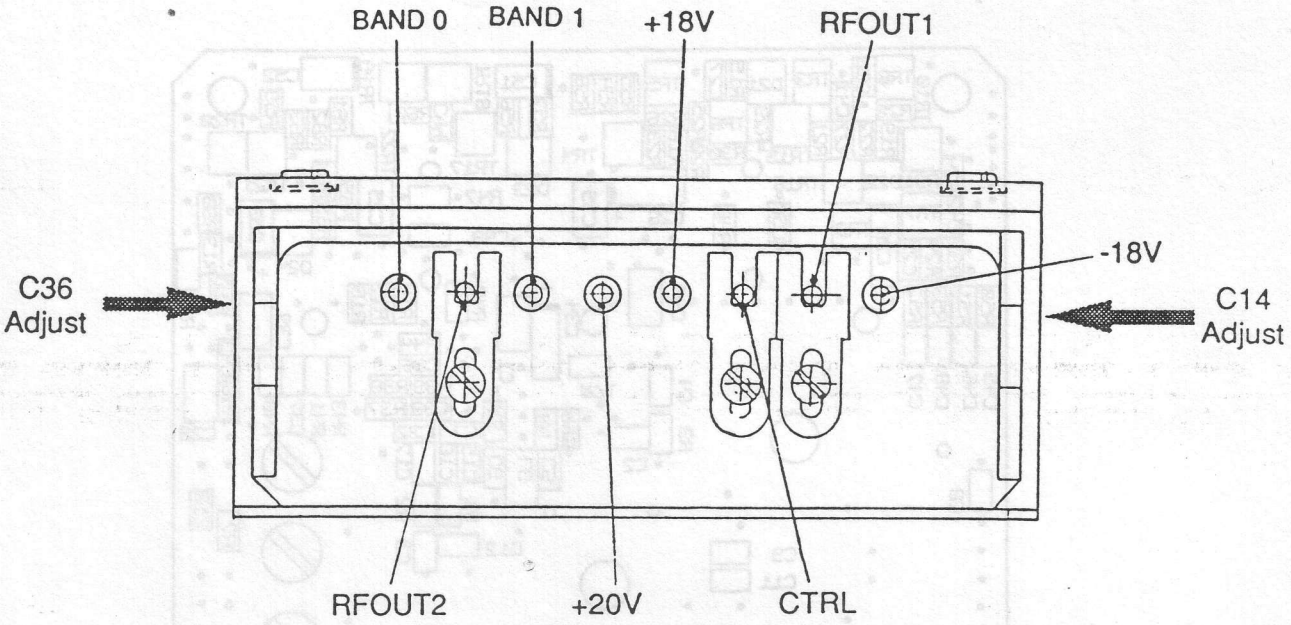


Figure 1 - Simplified Block Diagram



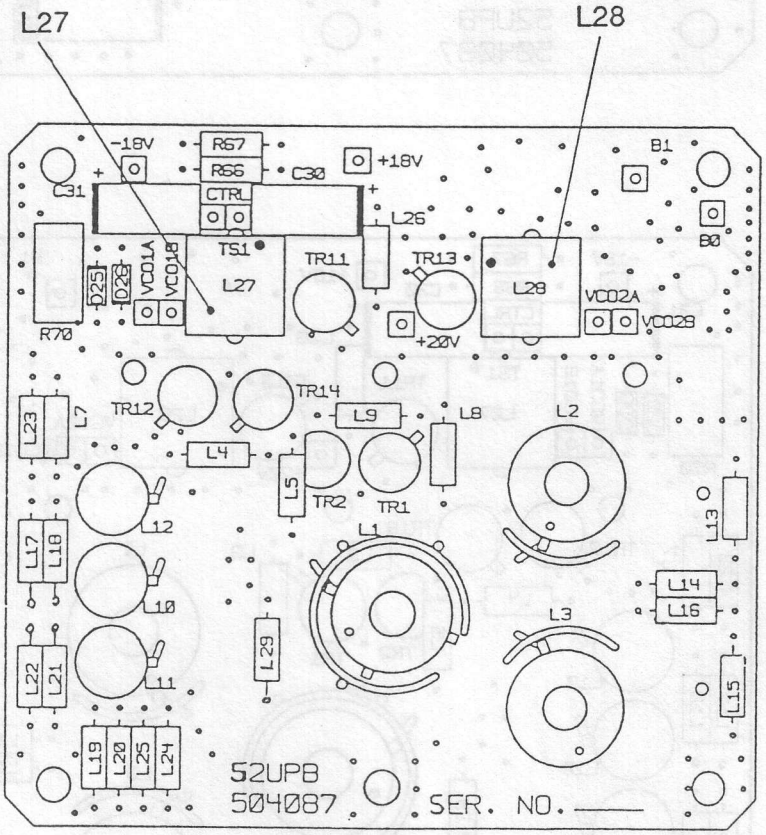


Figure 2 - Adjustments

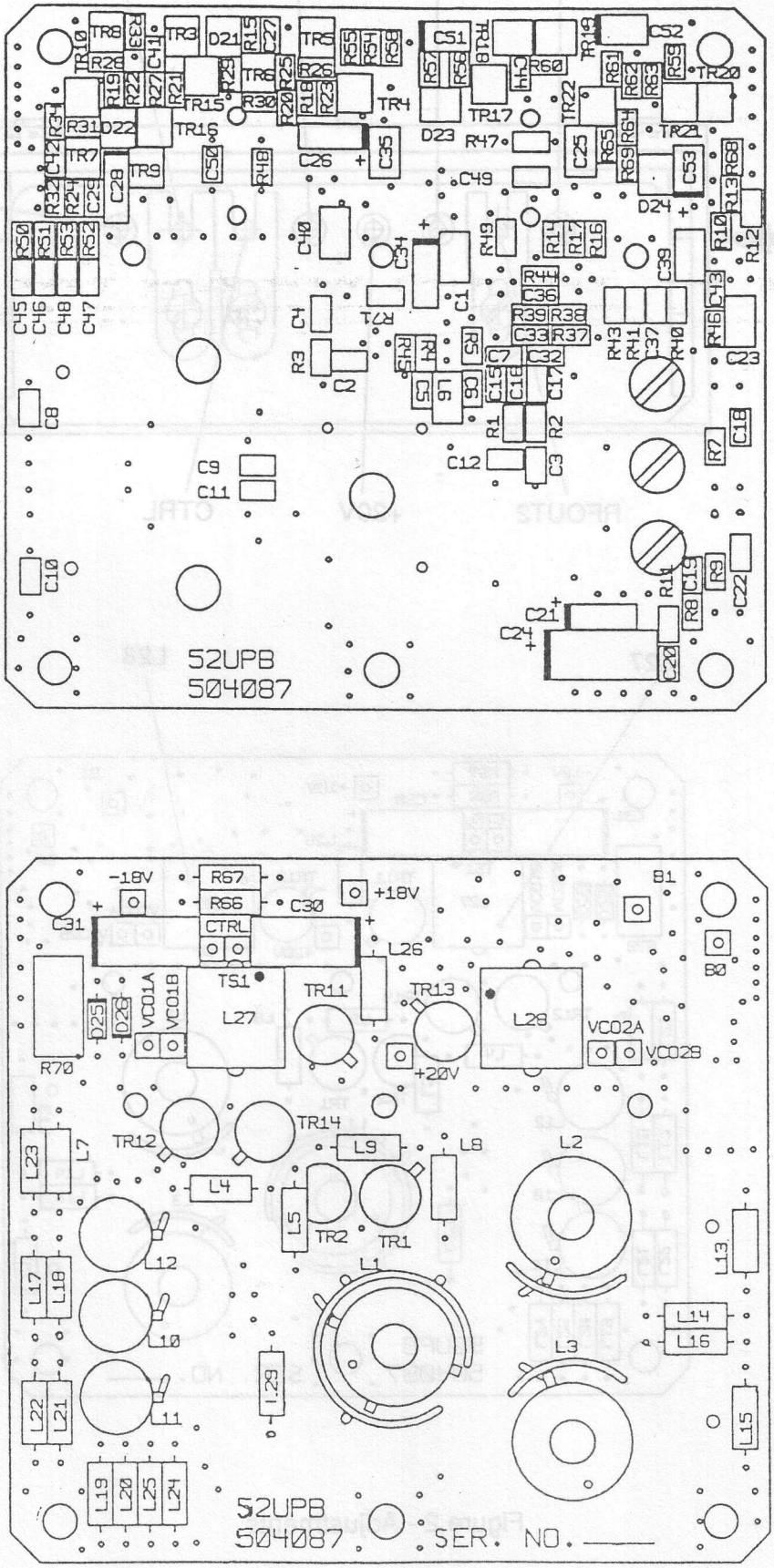
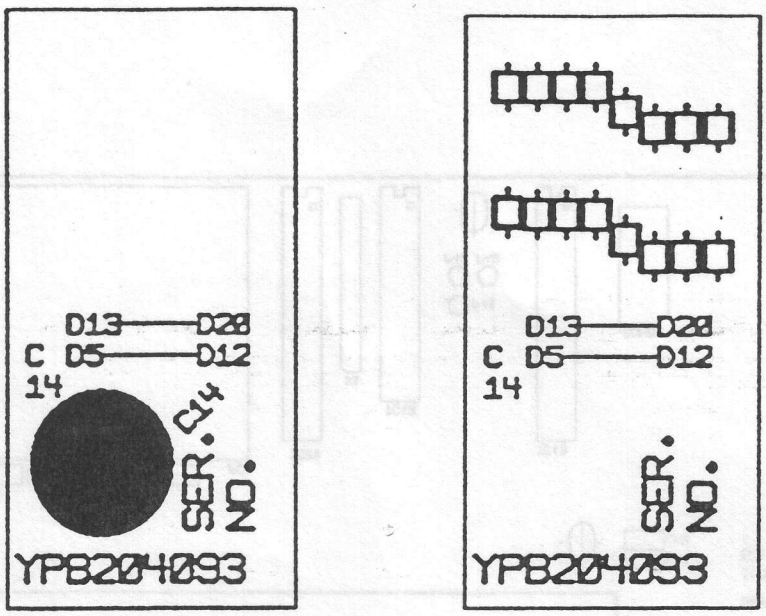
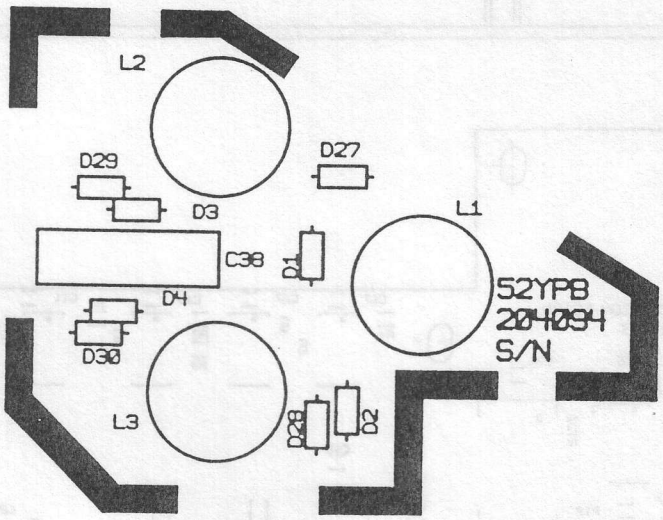


Figure 4 - VCO Board Component Layout



VCO Varactor Board 52YPB204093



VCO Pin Board 52YPB204094

Figure 5 - VCO Varactor and Pin Board Component Layout

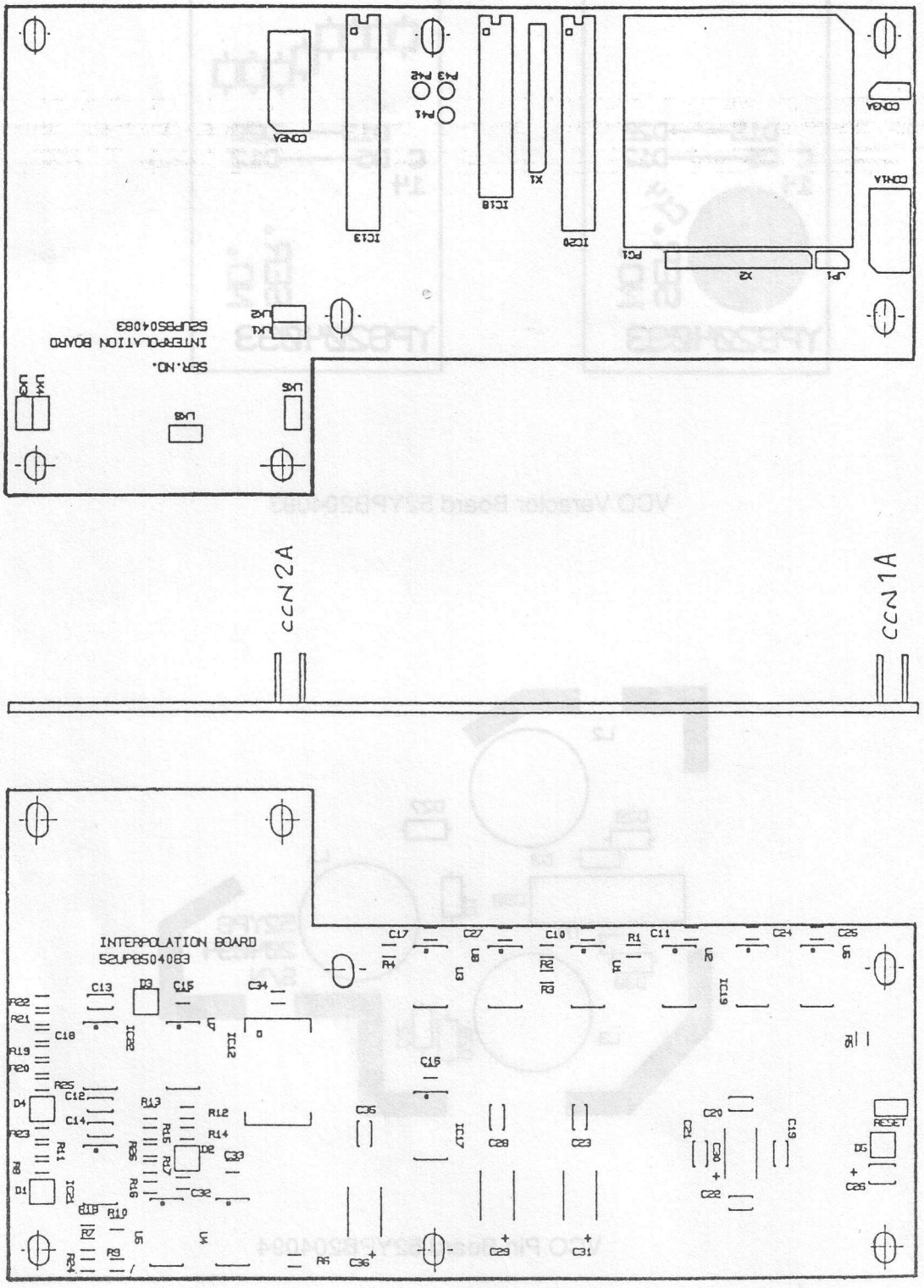


Figure 6 - Interpolation Board Component Layout

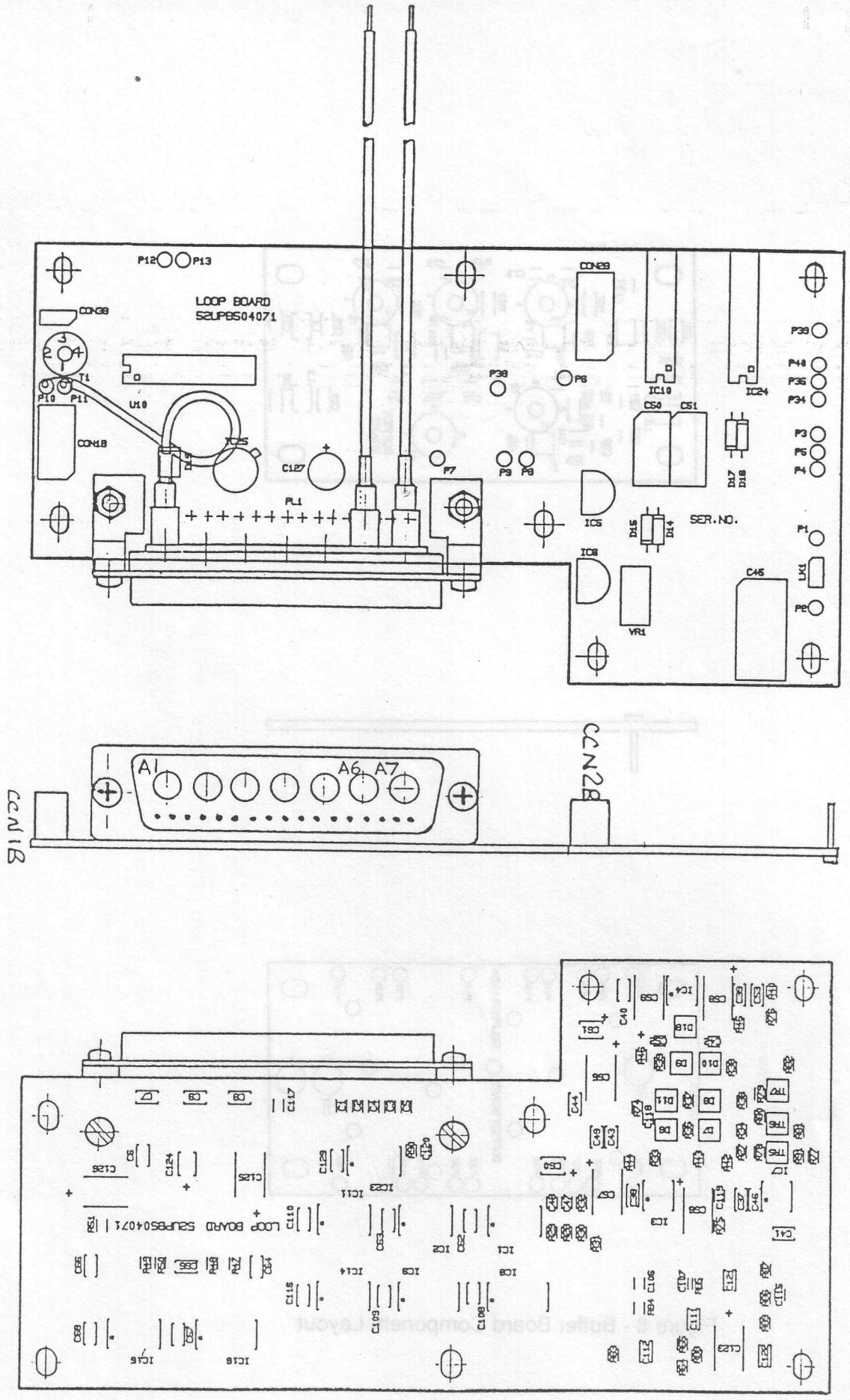
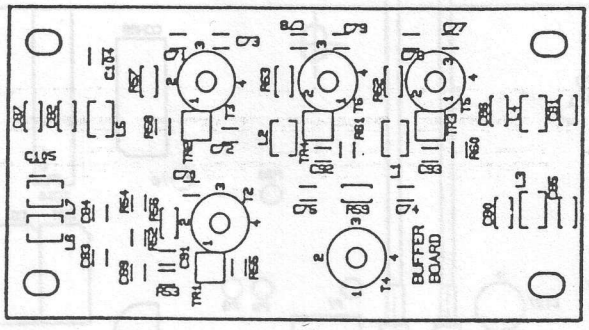
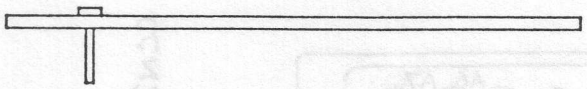


Figure 7 - Loop Board Component Layout





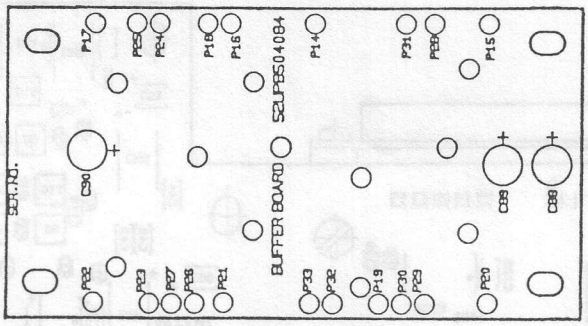


Figure 8 - Buffer Board Component Layout

Circuit Reference	Description	Value
C1	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C2 & C3	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C4 & C5	Capacitor, fixed, ceramic chip, 5%, 100V	15p
C6	Capacitor, fixed, ceramic chip, 5% 100V	100p
C7 to C12	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C16 & C17	Capacitor, fixed, ceramic chip, 5%, 100V	6p8
C18 & C19	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C20	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C21	Capacitor, fixed, solid tantalum chip, 20%, 20V	1µ
C22	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C23	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C24	Capacitor, fixed, solid tantalum chip, 20%, 20V	22µ
C26	Capacitor, fixed, solid tantalum chip, 20%, 20V	1µ
C27	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C28	Capacitor, fixed, solid tantalum chip, 20%, 20V	1µ
C29	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C30	Capacitor, fixed, solid tantalum chip, 10%, 35V	10µ
C31	Capacitor, fixed, solid tantalum chip, 10%, 35V	10µ
C32	Capacitor, fixed, ceramic chip, 5%, 100V	18p
C33	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C34	Capacitor, fixed, solid tantalum chip, 20%, 20V	1µ
C35	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C36 & C37	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C39 to C40	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C41 & C42	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C43	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C44 to C48	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C51 & C52	Capacitor, fixed, solid tantalum chip, 10%, 6.3V	2µ2
C53	Capacitor, fixed, solid tantalum chip, 20%, 20V	1µ

Synthesiser 1, VCO Board Items List - Sheet 1 of 4

Circuit Reference	Description	Value
L1	Choke, wound, special purpose	
L2	Choke, wound, special purpose	
L3	Choke, wound, special purpose	
L4 & L5	Choke, fixed, RF, 10%,	15µ
L6	Choke, fixed, chip, 20%	32n
L7	Choke, fixed, RF, 10%,	15µ
L8	Choke, fixed, RF, 10%	22u
L9	Choke, fixed, RF, 10%	2µ2
L10 to L12	Choke, wound, special purpose	
L13	Choke, fixed, RF, 10%,	15µ
L14	Choke, fixed, RF, 10%	2µ2
L15	Choke, fixed, RF, 10%,	15µ
L16	Choke, fixed, RF, 10%	2µ2
L17	Choke, fixed, RF, 10%	150n
L18	Choke, fixed, RF, 10%	10µ
L19	Choke, fixed, RF, 10%	150n
L20 & L21	Choke, fixed, RF, 10%	10µ
L22	Choke, fixed, RF, 10%	150n
L23	Choke, fixed, RF, 10%,	15µ
L24	Choke, fixed, RF, 10%	1µ5
L25	Choke, fixed, RF, 10%	1m
L26	Choke, fixed, RF, 10%,	15µ
L27 & L28	Choke, wound, special purpose	
R1	Resistor, fixed, chip, 1%, 0.1W	18k
R2	Resistor, fixed, chip, 1%, 0.1W	4k7
R3	Resistor, fixed, chip, 1%, 0.1W	680R
R4	Resistor, fixed, chip, 1%, 0.1W	1k
R5	Resistor, fixed, chip, 2%, 0.1W	51R
R7 to R9	Resistor, fixed, chip, 1%, 0.1W	470R
R10	Resistor, fixed, chip, 2%, 0.1W	36R
R11	Resistor, fixed, chip, 1%, 0.1W	820R
R12	Resistor, fixed, chip, 1%, 0.1W	150k

Synthesiser 1, VCO Board Items List - Sheet 2 of 4

Circuit Reference	Description	Value
R13	Resistor, fixed, chip, 1%, 0.1W	33k
R14	Resistor, fixed, chip, 1%, 0.1W	22k
R15	Resistor, fixed, chip, 2%, 0.1W	51R
R16 & R17	Resistor, fixed, chip, 1%, 0.1W	4k7
R18 & R19	Resistor, fixed, chip, 1%, 0.1W	22k
R20 & R21	Resistor, fixed, chip, 1%, 0.1W	1k5
R22 & R23	Resistor, fixed, chip, 1%, 0.1W	22k
R24	Resistor, fixed, chip, 2%, 0.1W	51R
R25	Resistor, fixed, chip, 1%, 0.1W	4k7
R26	Resistor, fixed, chip, 1%, 0.1W	1k
R27	Resistor, fixed, chip, 1%, 0.1W	4k7
R28	Resistor, fixed, chip, 1%, 0.1W	1k
R29	Resistor, fixed, chip, 1%, 0.1W	4k7
R30	Resistor, fixed, chip, 1%, 0.1W	470R
R31	Resistor, fixed, chip, 1%, 0.1W	4k7
R32	Resistor, fixed, chip, 1%, 0.1W	470R
R33 & R34	Resistor, fixed, chip, 1%, 0.1W	2k2
R37	Resistor, fixed, chip, 2%, 0.1W	51R
R38	Resistor, fixed, chip, 1%, 0.1W	1k
R39	Resistor, fixed, chip, 2%, 0.1W	51R
R40	Resistor, fixed, chip, 1%, 0.1W	4k7
R41	Resistor, fixed, chip, 1%, 0.1W	2k2
R43 & R44	Resistor, fixed, chip, 1%, 0.1W	680R
R45	Resistor, fixed, chip, 2%, 0.1W	10R
R46	Resistor, fixed, chip, 1%, 0.1W	470R
R49	Resistor, fixed, chip, 2%, 0.1W	51R
R50 to R54	Resistor, fixed, chip, 2%, 0.1W	10R
R55	Resistor, fixed, chip, 1%, 0.1W	1k5
R56	Resistor, fixed, chip, 2%, 0.1W	10R
R57	Resistor, fixed, chip, 1%, 0.1W	150R
R58 & R59	Resistor, fixed, chip, 1%, 0.1W	470R
R60	Resistor, fixed, chip, 1%, 0.1W	6k8
R61	Resistor, fixed, chip, 2%, 0.1W	10R

Circuit Reference	Description	Value
R62	Resistor, fixed, chip, 1%, 0.1W	1k5
R63	Resistor, fixed, chip, 2%, 0.1W	10R
R64	Resistor, fixed, chip, 1%, 0.1W	1k
R65	Resistor, fixed, chip, 1%, 0.1W	150R
R66 & R67	Resistor, fixed, chip, 1%, 0.1W	10k
R68	Resistor, fixed, chip, 1%, 0.1W	10k
R69	Resistor, fixed, chip, 1%, 0.1W	470R
R70	Resistor, variable, cermet, 10%, 0.5W	5k
R71	Resistor, fixed, chip, 1%, 0.1W	1k
D21 & D22	Diode, silicon planar high speed switching, BAS16	
D23 & D24	Diode, zener, BZX84C4V7	
D25 & D26	Diode, voltage reference, 6.2V, 400mW IN823	
TR1	Transistor, switching, NPN, 2N918	
TR2	Transistor, N channel, J Fet, J310	
TR3	Transistor, switching, NPN BSR13	
TR4	Transistor, switching, PNP, BSR15	
TR5	Transistor, switching, NPN, BSR13	
TR6 & TR7	Transistor, switching, PNP , BSR15	
TR8	Transistor, switching, NPN, BSR13	
TR9	Transistor, switching, PNP, BSR15	
TR10	Transistor, switching, NPN, BSR13	
TR11 to TR14	Transistor, switching, NPN, 2N918	
TR15 to TR17	Transistor, switching, PNP, BSR15	
TR18 & TR19	Transistor, switching , NPN, BSR13	
TR20 & TR21	Transistor, switching, PNP, BSR15	
TR22	Transistor, switching, NPN, BRS13	

Synthesiser 1, VCO Board Items List - Sheet 4 of 4

Circuit Reference	Description	Value
C38	Capacitor, variable,	0p2 - 1p2
D1 to D4	Diode PIN, HP 5082-3188	

Synthesiser 1, VCO PIN Board Items List - Sheet 1 of 1

Circuit Reference	Description	Value
C14	Capacitor, variable,	1 - 6p
D5 to D20	Diode tuning, BB405B	

Synthesiser 1, VCO Varactor Board Items List - Sheet 1 of 1

Circuit Reference	Description	Value
C69 to C73	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C74 & C75	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C76 to C79	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C80 to C82	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C83 & C84	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C85 to C87	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C88 to C90	Capacitor, fixed, aluminium electrolytic, 20%, 50V	10µ
C91 to C93	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C104 & C105	Capacitor, fixed, ceramic chip, 10%, 100V	10n
L1 & L2	Choke, fixed, chip , 20%	330n
L3 to L7	Choke, fixed, chip , 10%	47µ
R52	Resistor, fixed, chip, 2%, 0.1W	51R
R53 & R54	Resistor, fixed, chip, 1%, 0.1W	110R
R55	Resistor, fixed, chip, 1%, 0.1W	360R
R56 & R57	Resistor, fixed, chip, 5%, 0.25W	100R
R58	Resistor, fixed, chip, 1%, 0.1W	270R
R59	Resistor, fixed, chip, 5%, 0.25W	100R
R60 & R61	Resistor, fixed, chip, 1%, 0.1W	150R
R62 & R63	Resistor, fixed, chip, 5%, 0.25W	100R
TR1 to TR4	Transistor, N-channel, J Fet, SST310	

Synthesesier 1, Buffer Board Items List- Sheet 1 of 1

Circuit Reference	Description	Value
C10 & C11	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C12 to C14	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C15 to C17	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C18	Capacitor, fixed, ceramic chip, 50%, 100V	180p
C19 to C23	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C24 & C25	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C26	Capacitor, fixed, solid tant chip, 10%, 10V	10µ
C27	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C28	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C29 to C31	Capacitor, fixed, solid tant chip, 10%, 10V	47µ
C32 to C34	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C35	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C36	Capacitor, fixed, solid tant chip, 10%, 10V	47µ
IC12	Oct D F/F with clock enable, PC74HC377T	
IC13	2048 x 8 reprogrammable, CY7C291-50MC	
IC17	Quad latch, PC74HC175T	
IC18	Logic device programmable, PAL16R4A4CN	
IC19	Dual D-Type flip flop, PC74HC74T	
IC20	2048 x 8 reprogrammable, CY7C291-50MC	
IC21	Low power quad comparator, LM339M	
IC22	8 bit digital to analog converter, DAC08ED	
U1	IC, Hex Inverter, HEF4069BT	
U2	IC, quad 2 I/P Nand, HEF4011BT	
U3	IC, Hex Inverter, HEF4069BT	
U4 & U5	IC, 8 stage shift & store bus reg, HEF4094BT	
U6	IC, quad 2 I/P Nand, HEF4011BT	
U7	IC, 8 stage shift & store bus reg, HEF4094BT	
U8	IC, quad 2 I/P Nand, HEF4011BT	
PG1	IC, Digital signal processor + Ram, DSP56001RC20	

Synthesesier 1, Interpolation Board Items List- Sheet 1 of 2

Circuit Reference	Description	Value
R1 to R5	Resistor, fixed, chip, 1%, 0.1W	47k
R6	Resistor, fixed, chip, 1%, 0.1W	10k
R7	Resistor, fixed, chip, 1%, 0.1W	120k
R8	Resistor, fixed, chip, 1%, 0.1W	56k
R9	Resistor, fixed, chip, 1%, 0.1W	120k
R10	Resistor, fixed, chip, 1%, 0.1W	56k
R11	Resistor, fixed, chip, 1%, 0.1W	3k
R12	Resistor, fixed, chip, 1%, 0.1W	4k7
R13	Resistor, fixed, chip, 1%, 0.1W	3k
R14	Resistor, fixed, chip, 1%, 0.1W	4k7
R15	Resistor, fixed, chip, 1%, 0.1W	3k
R16 & R17	Resistor, fixed, chip, 1%, 0.1W	10k
R18	Resistor, fixed, chip, 1%, 0.1W	560k
R19 & R20	Resistor, fixed, chip, 1%, 0.1W	22k
R21	Resistor, fixed, chip, 1%, 0.1W	6k2
R22	Resistor, fixed, chip, 1%, 0.1W	6k2
R23	Resistor, fixed, chip, 1%, 0.1W	3k
R24	Resistor, fixed, chip, 1%, 0.1W	560k
R25	Resistor, fixed, chip, 1%, 0.1W	4k7
R26	Resistor, fixed, chip, 1%, 0.1W	10k
X1 & X2	Resistor Network, 2%, 1.125W,4609X-101	47k
D1 & D2	Diode, silicon planar high speed switching, BAS16	
D3	Diode, zener, BZX84-C8V2	
D4 & D5	Diode, silicon planar high speed switching, BAS16	

Synthesiser 1, Interpolation Board Items List- Sheet 2 of 2

Circuit Reference	Description	Value
C1 to C5	Capacitor, fixed, ceramic chip, 5%, 100V	220p
C6 to C9	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C37 to C41	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C42	Capacitor, fixed, ceramic chip, 10%, 100V	4n7
C43 & C44	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C45	Capacitor, fixed, polycarbonate, 5%, 63V	2µ2
C46	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C47 & C48	Capacitor, fixed, ceramic chip, 10%, 100V	4n7
C49	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C50 & C51	Capacitor, fixed, polycarbonate, 10%, 250V	47n
C52	Capacitor, fixed, ceramic chip, 10%, 100V	4n7
C55 to C59	Capacitor, fixed, solid tant chip, 10%, 25V	10µ
C60 & C61	Capacitor, fixed, solid tant chip, 10%, 25V	1µ5
C62 to C68	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C106 & C107	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C108 to C113	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C115	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C116	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C117	Capacitor, fixed, ceramic chip, 5%, 100V	220p
C120	Capacitor, fixed, ceramic chip, 5%, 100V	10p
C121 & C122	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C123	Capacitor, fixed, solid tant chip, 10%, 25V	10µ
C124	Capacitor, fixed, solid tant chip, 20%, 25V	470n
C125 & C126	Capacitor, fixed, solid tant chip, 10%, 10V	47µ
C127	Capacitor, fixed, electrolytic, 20%, 63V	22µ
IC1	Dual D F/F 74AC74SC	
IC2	Quad, 2 I/P Nand, 74AC00SC	
IC3	OP Amp, Low noise precision, OP37GS	
IC4	Op Amp, Single bifet I/P, LF351M	
IC5	Voltage reg, positive fixed, +15V, LM78L15ACZ	
IC6	Voltage reg, negative fixed, -15V, LM79L15ACZ	
IC7	Op Amp, Single bifet I/P, LF351M	

Synthesiser 1, Loop Board Items List - Sheet 1 of 3

Circuit Reference	Description	Value
IC8 & IC9	Synchronous presettable binary counter, 74ACT161SC	
IC10	Dual modulus high speed divider, SP8691BDG	
IC11	Dual D-type flip-flop, 74ACT74SC	
IC14	Dual 4-input Nand, CD74AC20M	
IC16	Dual decade ripple counter, PC74HCT390T	
IC23	Quad 2-input Nand, 74AC00SC	
IC24	Triple line receiver, MC10116P	
IC25	Voltage regulator, 78M05CG	
U10	Quad MECL-TTL translator, MC10H350P	
R27	Resistor, fixed chip, 1%, 0.1W	100k
R28 & R29	Resistor, fixed chip, 1%, 0.1W	1k6
R30 & R31	Resistor, fixed chip, 1%, 0.1W	3k3
R32	Resistor, fixed chip, 1%, 0.1W	47k
R33	Resistor, fixed chip, 1%, 0.1W	33k
R34	Resistor, fixed chip, 1%, 0.1W	6k8
R35	Resistor, fixed chip, 1%, 0.1W	300R
R36	Resistor, fixed chip, 1%, 0.1W	6k8
R37	Resistor, fixed chip, 1%, 0.1W	300R
R38	Resistor, fixed chip, 1%, 0.1W	56k
R39	Resistor, fixed chip, 1%, 0.1W	3k3
R40	Resistor, fixed chip, 1%, 0.1W	470R
R42	Resistor, fixed chip, 2%, 0.1W	10R
R43	Resistor, fixed chip, 1%, 0.1W	33k
R44 to R46	Resistor, fixed chip, 2%, 0.1W	10R
R47	Resistor, fixed chip, 1%, 0.1W	2k
R48 & R49	Resistor, fixed chip, 1%, 0.1W	5k6
R50	Resistor, fixed chip, 1%, 0.1W	2k
R51	Resistor, fixed chip, 2%, 0.1W	51R
R64	Resistor, fixed chip, 1%, 0.1W	3k6
R65	Resistor, fixed chip, 1%, 0.1W	1k5
R74 & R75	Resistor, fixed chip, 1%, 0.1W	1k8

Synthesiser 1, Loop Board Items List - Sheet 2 of 3

Circuit Reference	Description	Value
R76	Resistor, fixed chip, 1%, 0.1W	47R
R84 to R87	Resistor, fixed chip, 1%, 0.1W	510R
R88	Resistor, fixed chip, 1%, 0.1W	1k5
R89	Resistor, fixed chip, 2%, 0.1W	51R
R90	Resistor, fixed chip, 1%, 0.1W	1k5
VR1	Resistor, variable, 10%, 0.5W	10k
D6 to D11	Diode, silicon planar high speed switching, BAS16	
D14 to D17	Diode, silicon, IN4148	
D18	Diode, silicon planar high speed switching, BAS16	
D19	Diode, silicon rectifier, BY448	

Synthesiser 1, Loop Board Items List - Sheet 3 of 3

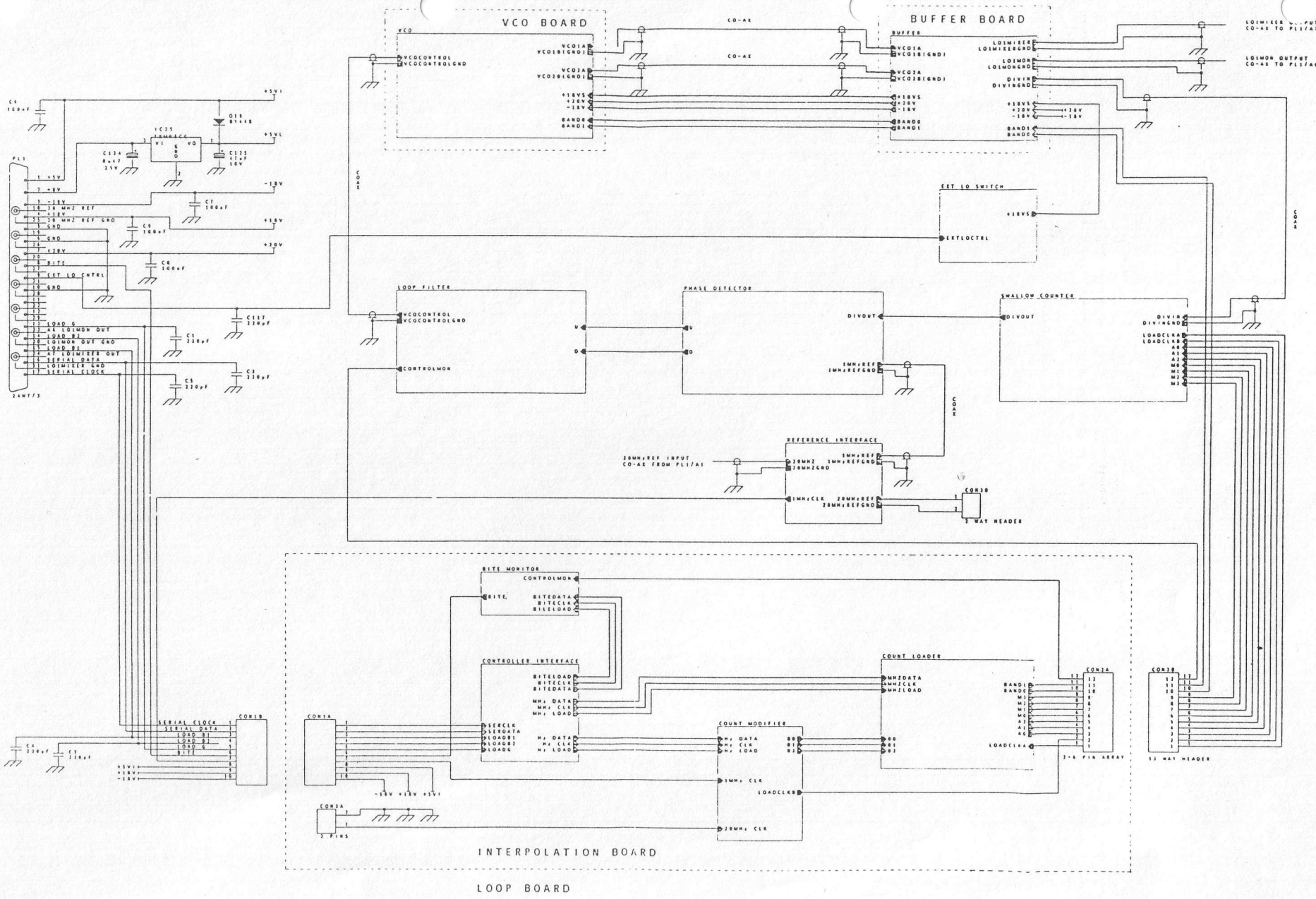


Figure 9 - Synthesiser 1 Module Interconnection Diagram

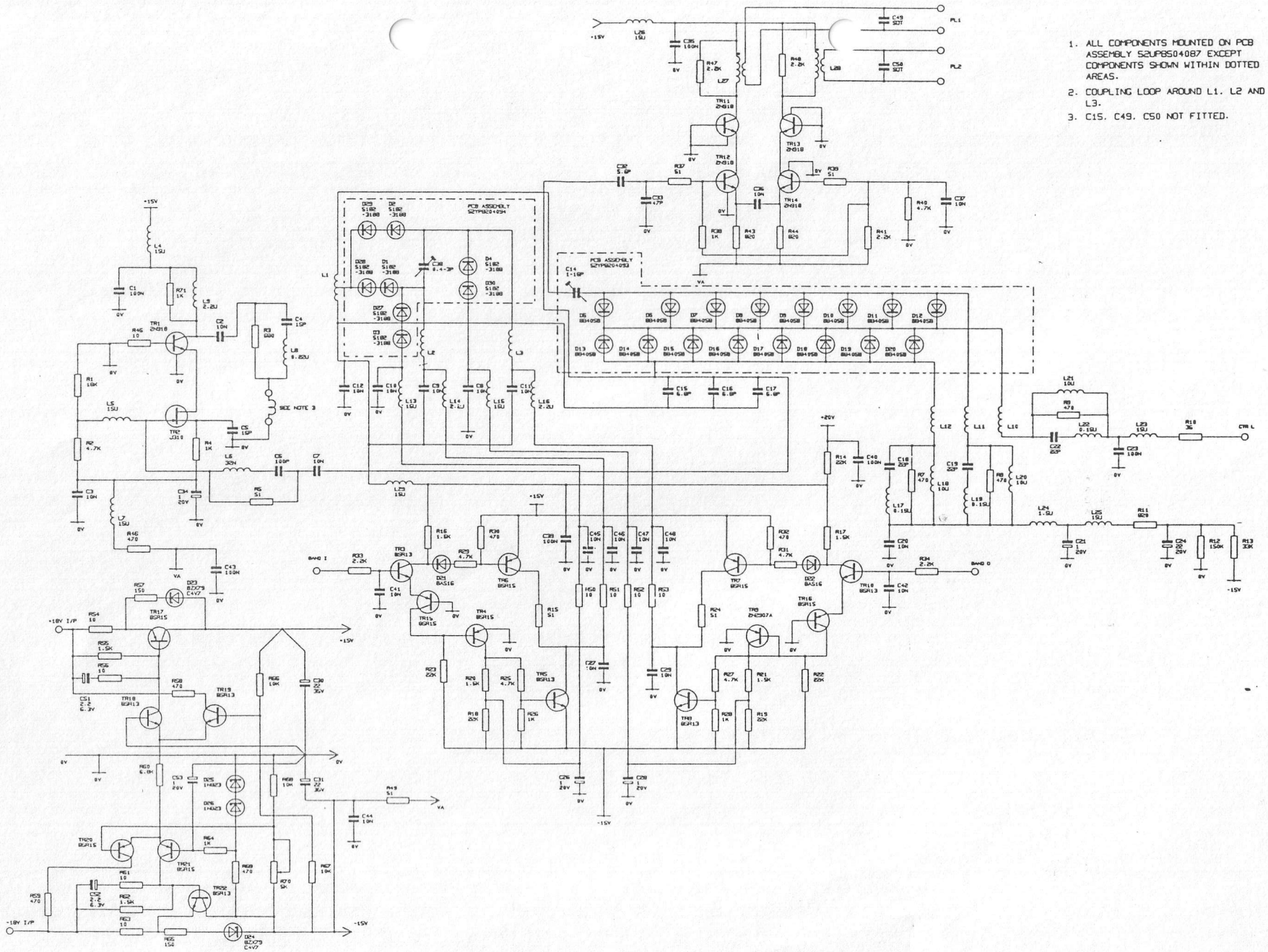


Figure 10 - VCO Board Circuit Diagram

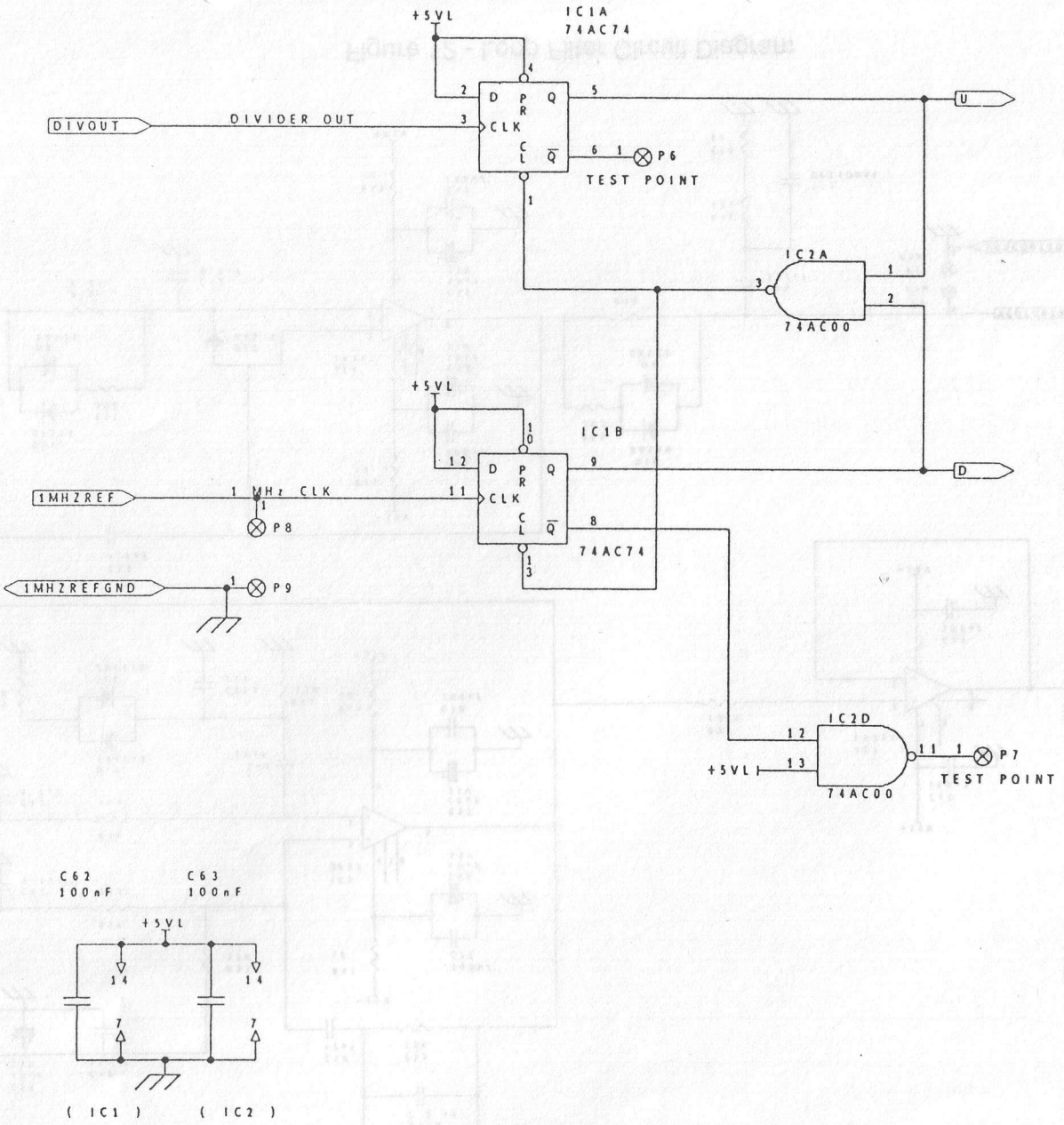


Figure 11 - Phase Detector Circuit Diagram

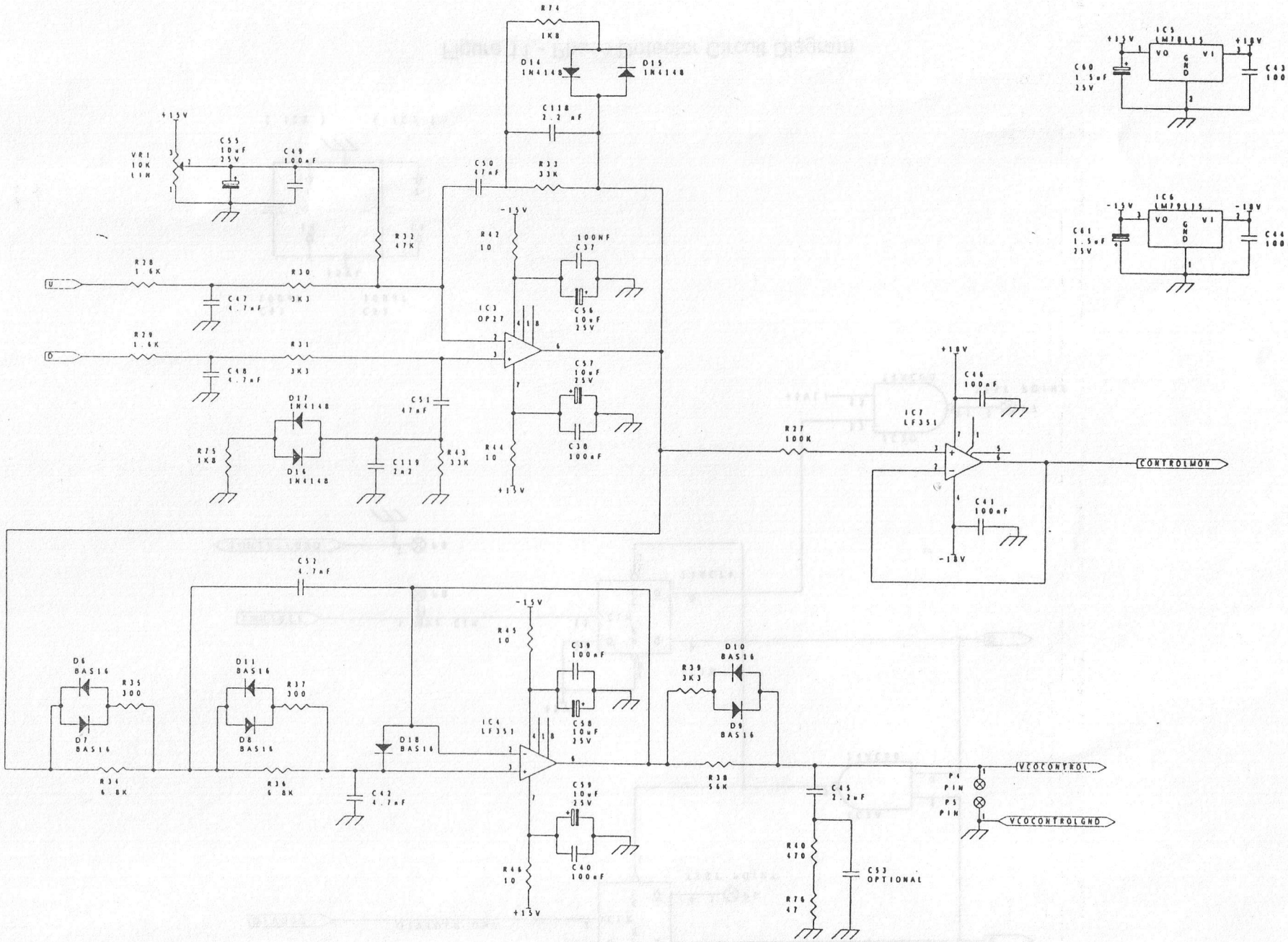


Figure 12 - Loop Filter Circuit Diagram

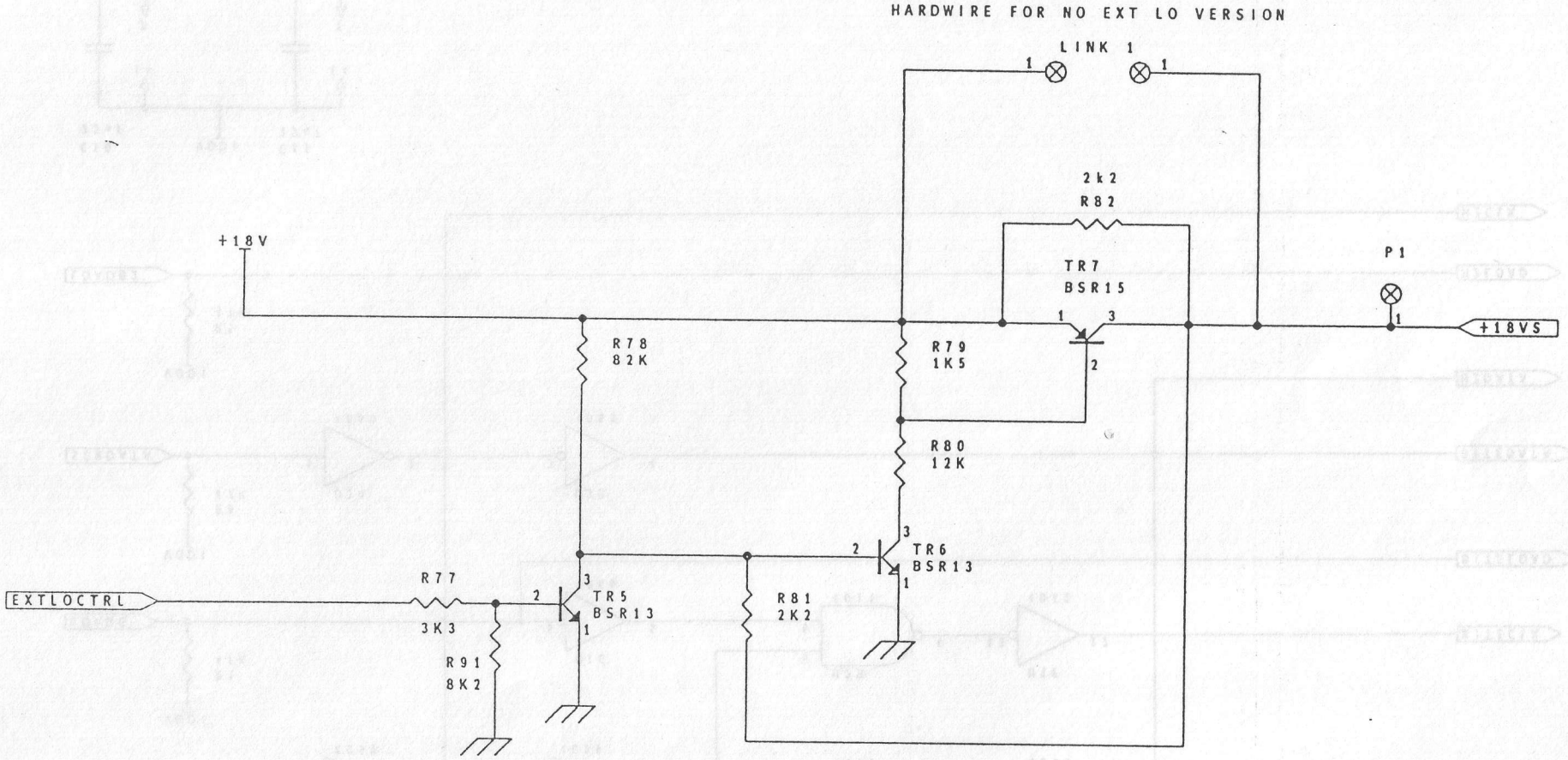


Figure 13 - EXT LO Switch

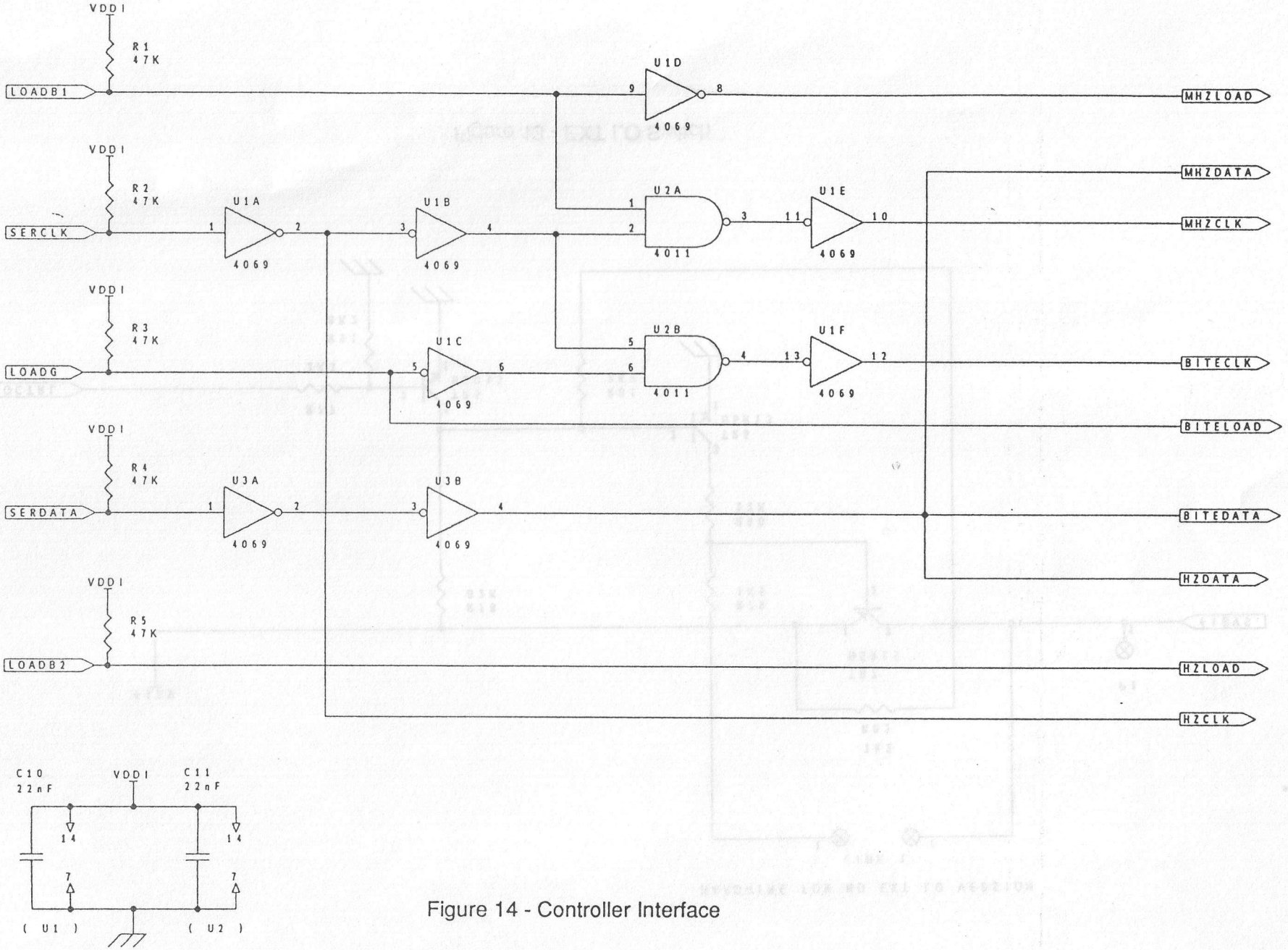


Figure 14 - Controller Interface

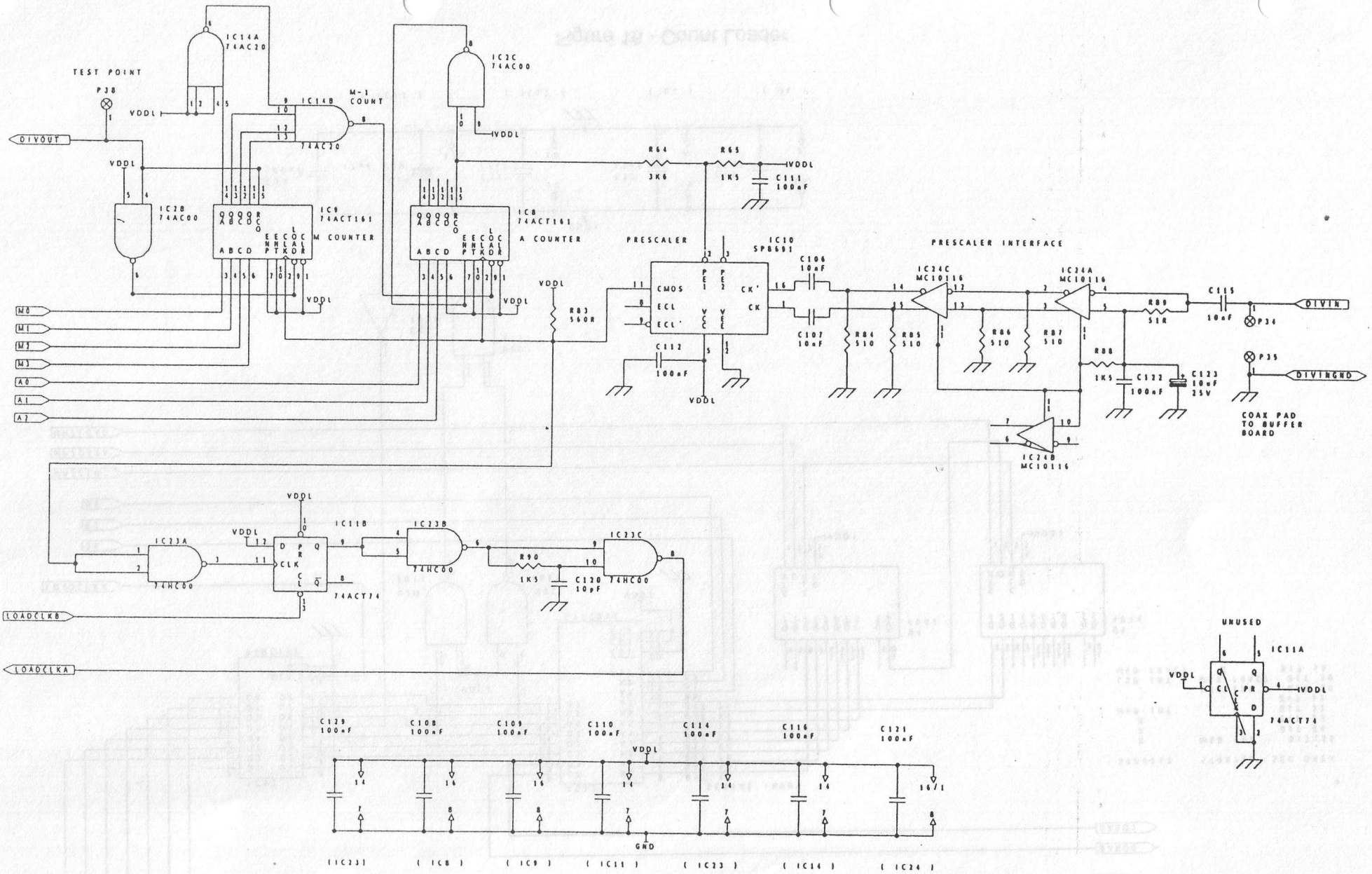


Figure 15 - Swallow Counter

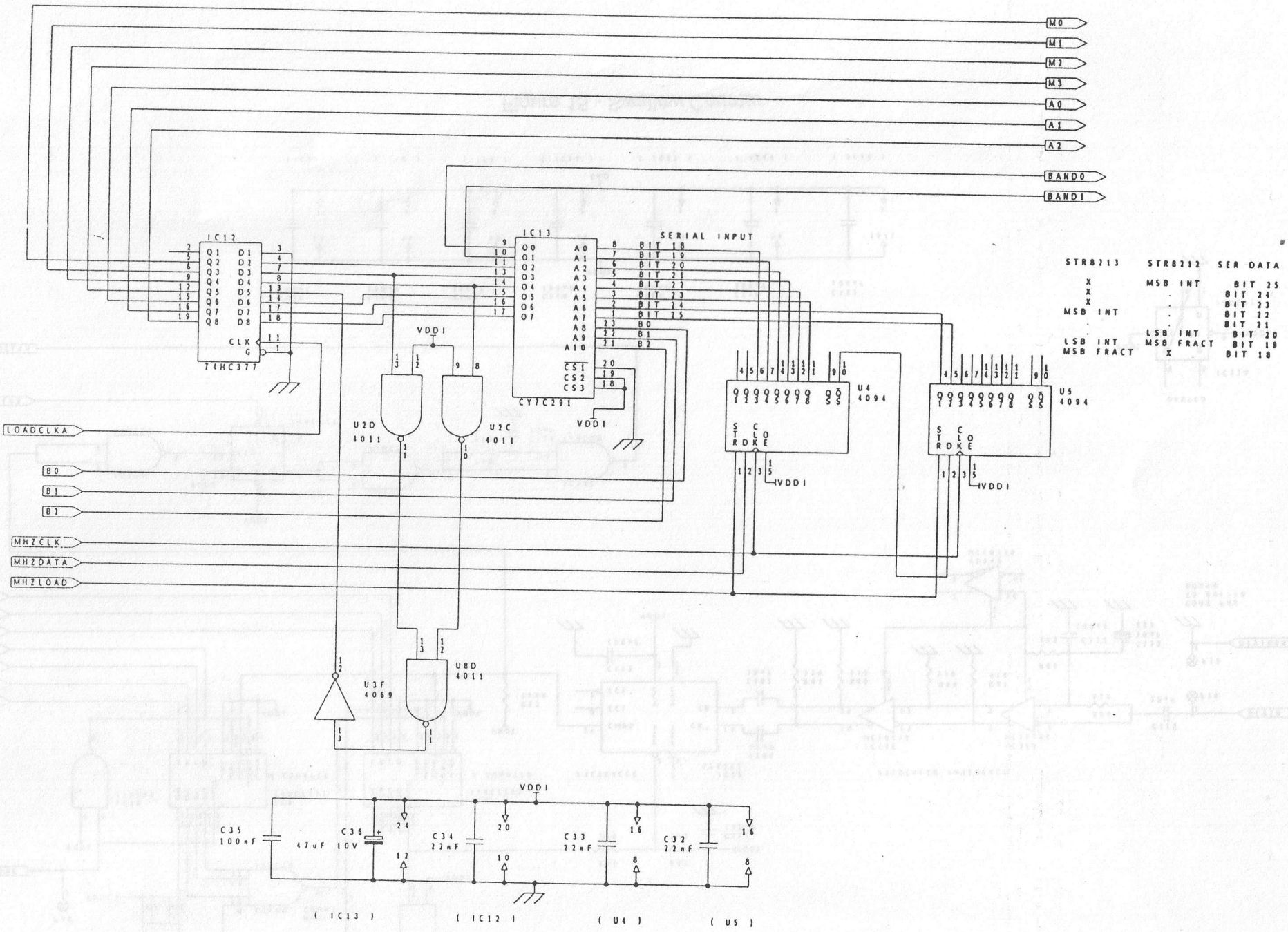


Figure 16 - Count Loader

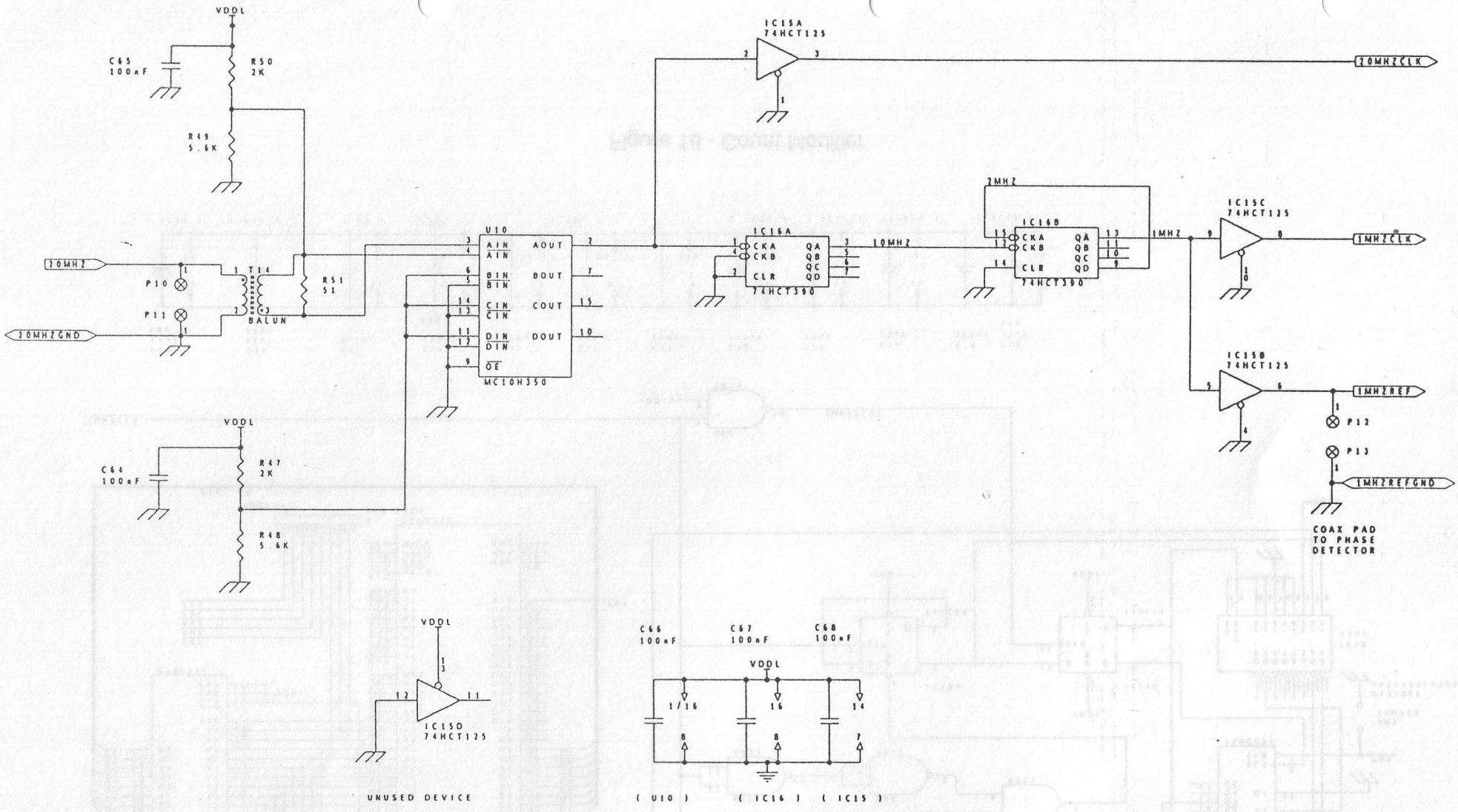


Figure 17 - Reference Interface

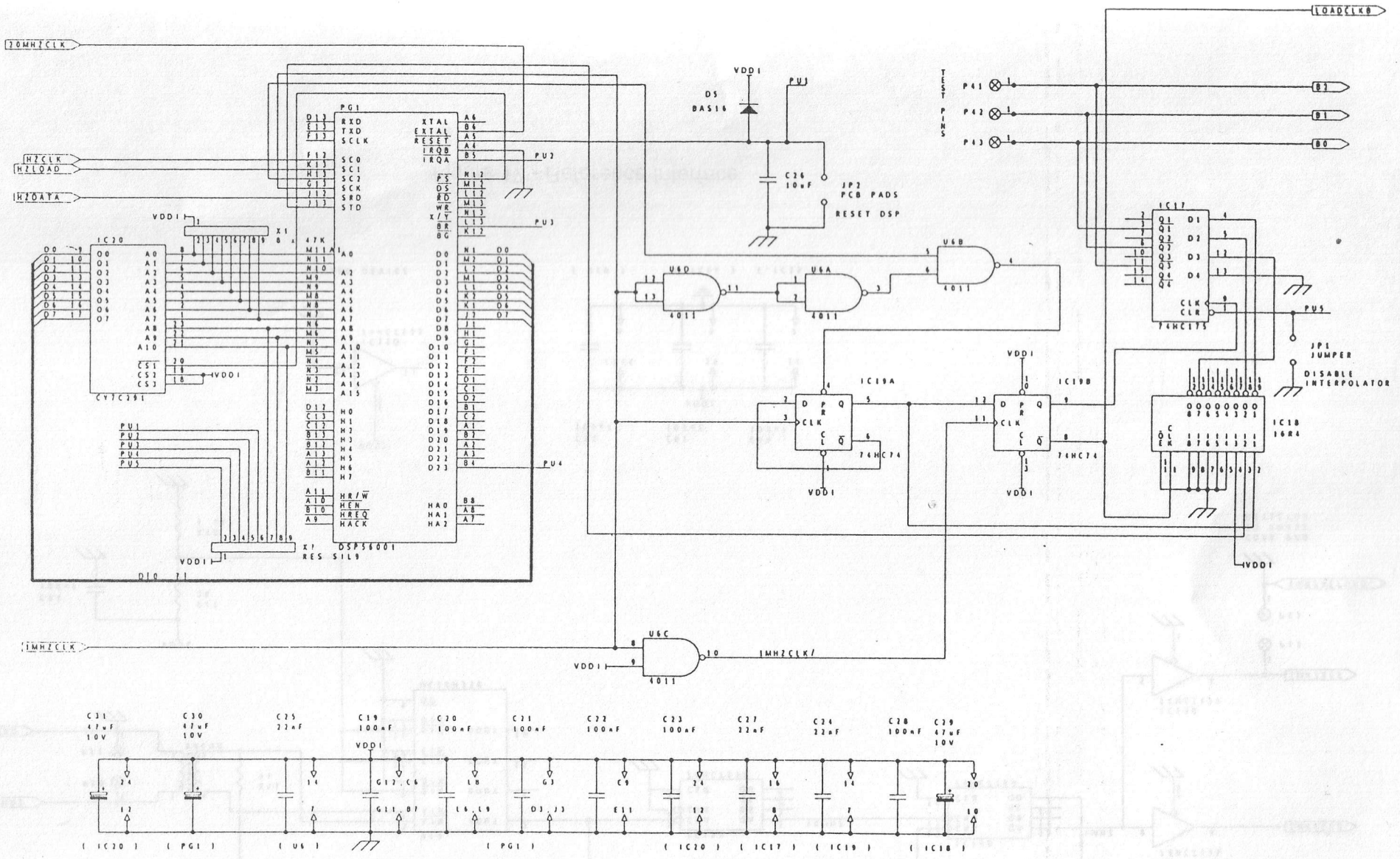


Figure 18 - Count Modifier

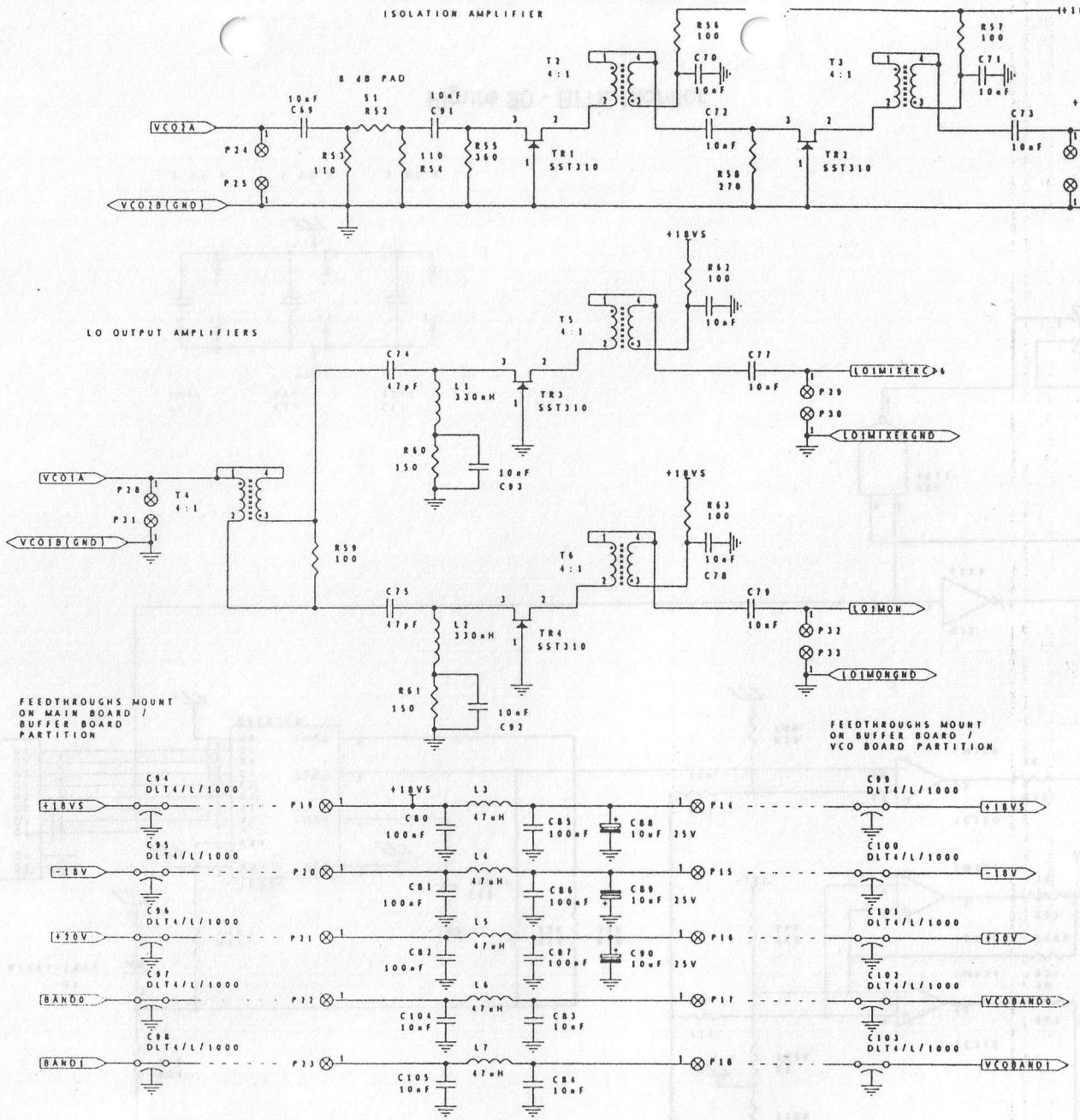


Figure 19 - Buffer

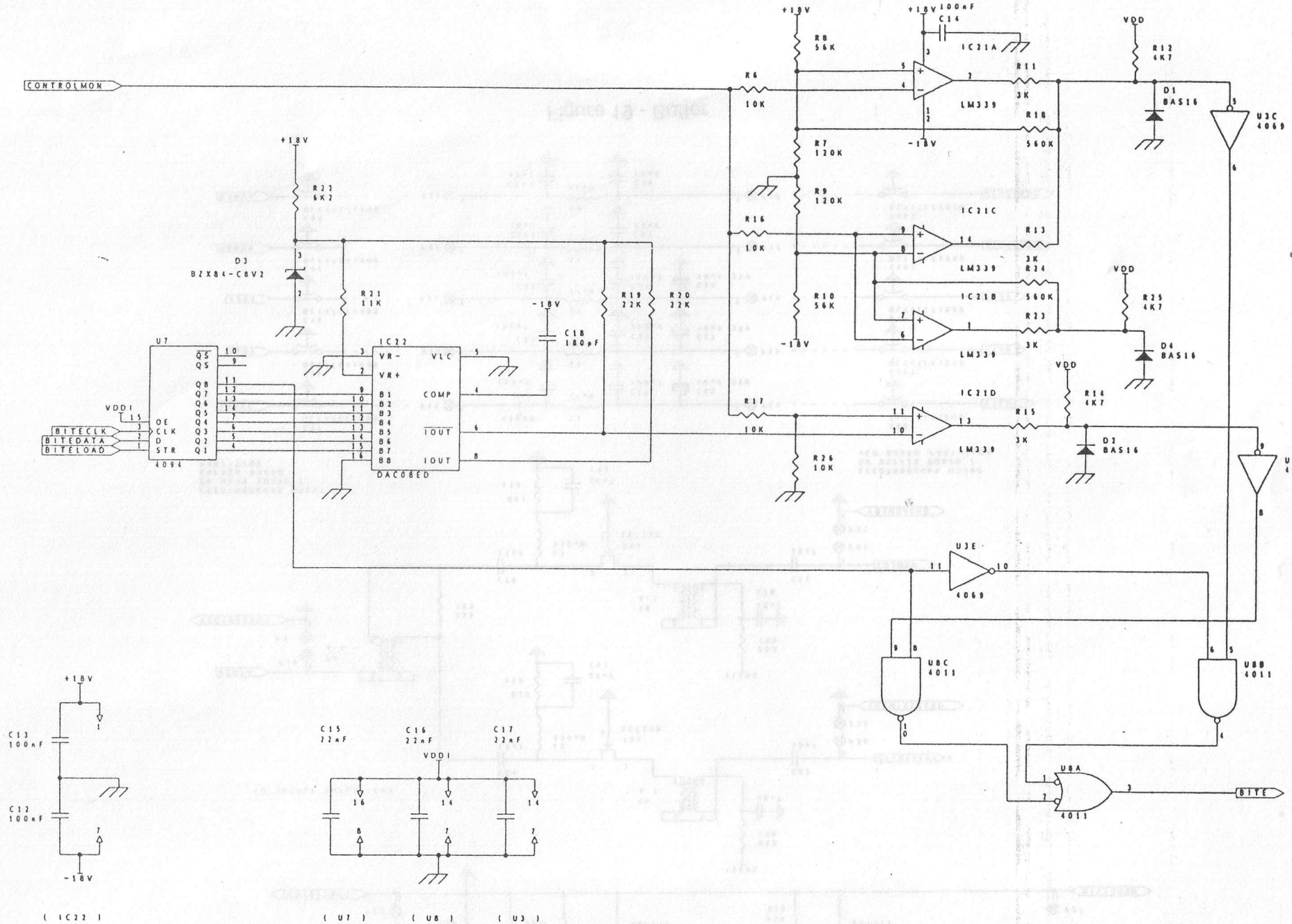


Figure 20 - BITE Monitor

Chapter 6.4

SYNTHESISER 2

1 INTRODUCTION

The Synthesiser 2 Module comprises a single PCB housed in a screened enclosure and occupies SK5 of the RF backplane within the receiver. The single connection carries both RF and DC signals.

Module description is given with reference to the following drawings/illustrations and items list:

- Figure 1 Synthesiser 2 Simplified Block Diagram
- Figure 2 Simplified Phase Detector & LOOP Amplifier
- Figure 3 Simplified BITE CCT
- Figure 4 Synthesiser 2 Layout Diagram
- Items List Synthesiser 2, Sheets 1 to 6 inc.
- Figure 5 Synthesiser 2 Circuit Diagram

2 MODULE DESCRIPTION

Module description is given under the following headings:

- Block Diagram . . . . . Paragraph 2.1
- Typical Signal Levels . . . . . Paragraph 2.2

2.1 Block Diagram

The module incorporates a synthesised phase-locked loop with two outputs at 70 MHz, locked to a 10 MHz reference signal from the Reference Oscillator Module.

The phase-locked loop consists of a Voltage Controlled Crystal Oscillator (VCXO) operating at 70 MHz. The output of this VCXO is divided down, in two stages to 100 kHz and fed via an equal mark/space converter to a phase detector.

The other input to this phase detector is derived from the 10 MHz reference input, which is divided down in one stage to 100 kHz. The output from the phase detector is fed into a loop filter amplifier to provide the tuning voltage to control the VCXO (70 MHz).

The module has the facility of being by-passed by an external 2nd local oscillator input (EXT LO2 INPUT) and incorporates a switching circuit to turn off the internal synthesiser to allow the external LO2 to be directly gated to the two 70 MHz outputs.

A logic output is also provided to give an indication when an external reference is present. BITE circuitry is incorporated and this provides a logic output to the receiver BITE function when the circuit is out of lock.

The basic building blocks of this module are:

- Voltage Controlled 70 MHz Crystal Oscillator/Buffer
- Divider (70 MHz to 100 kHz)
- Phase Detector
- Loop Filter-Amplifier
- External Reference Input Divider (10 MHz to 100 kHz)
- Output Splitter/Buffers
- Internal/External LO2 switch

2.2 Typical Signal Levels

The synthesised output signal levels for both 70 MHz outputs are typically 3dBm for A3 (limits +2 to +6dBm) and 7dBm for A4 (limits +6 to +12dBm).

The reference input (10 MHz REF A1) is typically 6dBm, supplied from the Reference Module and has a specified locking range at +3dBm minimum to +9dBm maximum input.

External LO2 input (A2) operates the hysteresis, internal/external LO2 switch at typical threshold levels of 0dBm for ON and -3dBm for OFF (specification level +1dBm to -5dBm).

3 CIRCUIT DESCRIPTION

Circuit description is given under the following headings:

- Voltage Controlled 70 MHz Crystal Oscillator . . . . . Paragraph 3.1
- Divider (70 MHz to 100 kHz) . . . . . Paragraph 3.2
- Phase Detector . . . . . Paragraph 3.3
- Loop Filter Amplifier . . . . . Paragraph 3.4
- External Reference Input Divider (10 MHz to 100 kHz) . . . . Paragraph 3.5
- Output Splitter/Buffers . . . . . Paragraph 3.6
- Internal/External LO2 Switch . . . . . Paragraph 3.7

3.1 VCXO

The 70 MHz VCXO is at the heart of the phase-locked loop. The circuit is a low distortion Colpitts oscillator with a cascode amplifier (L4, TR1 and TR2) which is locked by the varactor tuned 70 MHz crystal (D1, D2 and X1). The varactor voltage is supplied via the loop filter-amplifier, IC1 pin 6. The output from the cascode amplifier (TR1, TR2) is buffered by a common-base buffer (TR18) into the splitter (SPL1). The splitter diverts the buffered 70 MHz to the LO2 switch (D8) and also the first divider (IC4) of the phase-locked loop synthesiser.

3.2 Divider

Two divider stages, IC4 and IC7, provide a divide-down by 700 from the 70 MHz (VCXO) to provide 100 kHz. IC4 provides a divide by 100 function, with IC5 providing the divide by 7 function. The 100 kHz is shaped by IC6a to provide a precise 1:1 mark/space ratio for one side input of the phase comparator (IC3 pin 1).

3.3 Phase Detector

The phase detector, IC3 pins 1 to 3, (refer to Figure 2) is an exclusive 'OR' or digital phase detector with R76 and C41 as the low-pass filtering. Current injection by TR3 and TR6, amplify the error slope at the low-pass filter, R76 and C41, in order to tighten up the lock range of the synthesised loop.

3.4 Loop Filter Amplifier

Loop filter amplifier IC1, (refer to Figure 2), in conjunction with R12, R13 and C32 provide the loop stability function as well as a buffered drive voltage for the varactor tuning of the 70 MHz crystal in the (VCXO). It is essentially a voltage comparator to balance the phase detector error voltage at C41 with the 2.5V reference level, set between R22 and R23. The loop amplifier reference is set to 2.5V to allow an increase or decrease of phase in order to balance the loop at 90° phase which is also the frequency lock point. The maximum increase or decrease in phase allowable at the set reference is 0° to +180°, due to the 0V to +5V swing at IC3(a) output.

3.5 External Reference Input Divider

External reference input (10 MHz REF, A1), is supplied from the Reference Module and sets the frequency accuracy of the synthesised 70 MHz outputs (LO2). An impedance matching/limiter circuit (L19, C77, D11, D12), provides the correct input level to the divide by 100 circuit, IC7. The output of IC7 provides a 100 kHz reference signal to the other side of the phase comparator input, IC3 pin 2.

3.6 Output Splitter/Buffers

Output buffers, IC8 and IC9 provide 70 MHz to the 2nd IF (A3) and the external LO2 output of the receiver (A4). The input to these buffers is derived from a balanced splitter circuit, R54, R55 and R56. The input to the splitter is provided by the Internal/External LO2 (70 MHz) switch.

3.7 Internal/External LO2 Switch

A power level, sensing switch is provided to automatically gate an external LO2 input (A2) through to the output splitter/buffer, whilst switching off the internal synthesised phase-locked loop. This function is provided for matched radio applications. The switch consists of main elements TR8 to TR14, D7 and D8, and disables the internal phase-locked loop by R2, D9, D68 and R69. A logic output at pin 10 (EXTLO2) indicates on the LCD front panel display, 'UNCAL' when only an 'LO2' external input signal is used, whereby it is extinguished when either the external 'LO2' is removed or both the external 'LO1' and 'LO2' input signals are used.

4 ADJUSTMENTS

There are two trimmer capacitors, one fixed capacitor and three resistors which are select-on-test. C77 trimmer is tuned for maximum 10 MHz signal at IC7 pin 7 using a low capacitance probe and then C23 is adjusted until the loop locks and produces maximum output at A4. The fixed capacitor C84 and resistors R62, R63 and R64 are select-on-test batch adjustments and are factory set.

5 ON-LINE BITE

Out-of-lock indication BITE is provided by logic circuitry consisting of IC3 pins 4, 10 and 11, IC2, IC6b and IC10, (refer to Figure 2 and 3). Both the reference 100 kHz and VCXO 100 kHz, divided down, signals are buffered by IC3 pin 5 and IC3 pin 13 to the exclusive 'OR' digital phase comparator (IC3 pins 8 and 9). The phase comparator output (IC3 pin 10) provides an equal mark/space ratio squarewave output when both reference and VCXO 100 kHz frequencies are in lock at its input. The reason that this occurs is because the loop error amplifier, IC1 has its reference set at mid-point between the logic supply, (refer to Figure 2). This therefore means that when the reference and loop frequencies are in lock, the output of the locked-loop phase comparator filter, R78/C41, will be at mid-point between the logic supply rails with a resultant 90° shift between the leading edges of the reference and locked-loop 100 kHz waveforms.

IC2 circuitry supplies the trigger input of IC6b with pulses that represent the leading and trailing edges of the output waveform of the (IC3 pin 10) phase comparator, hence the trigger to IC6b has pulses equi-spaced during lock. IC6b is a positive edge-triggered re-triggerable monostable with the timing window set by R32 and C48. It is used to detect if the input trigger pulses move and widen relative to each other, greater or smaller than the 50% duty cycle. It is also known as a missing pulse detector. The output of IC6b is held in the active, triggered - high state and awaits the input trigger pulses to widen to allow the output to drop. The tightness of the timing components of IC6b to the input trigger pulse spacing set the out-of-lock detection range. IC10 is another monostable with negative edge-triggering and a long timing duration (1 second) that is used as the 'LO2' out-of-lock BITE output flag at pin 1.

6 FAULT FINDING

The front panel BITE 09 FAIL 2 and/or BITE 09 FAIL 16 should be the first indication of a fault. BITE 09 FAIL 2 refers to LO2 being out of lock and is derived from Synthesiser 2 module BITE. BITE 09 FAIL 16 refers to LO2 drive being low and is derived from the IF module BITE. If the output frequencies are significantly out of specification and a high (1) is present at pin 1 of the module, then go through the adjustments sequence, (paragraph 4). If the module is still at fault, a quick voltage check with a high input impedance DVM, across C41 should measure approximately +2.5V for a locked loop. Should the voltage read 0V or greater than 4.5V, then the input pins 1 and 2 to IC3 should be checked for 100 kHz (VCXO) and 100 kHz (10 MHz REF A1) inputs. If a healthy locked-loop is apparent, check out the BITE circuit function shown in Figure 3. The varactor tuning voltage of the (VCXO), when healthy, should be on average -3V across C32, which means that an external dc voltage source can be injected across C32 to this approximate value, in order to fault find on the (VCXO). To check the function of the External LO2 input switch, inject an LO2 signal into the connector at the back panel to the levels as in paragraph 2.2

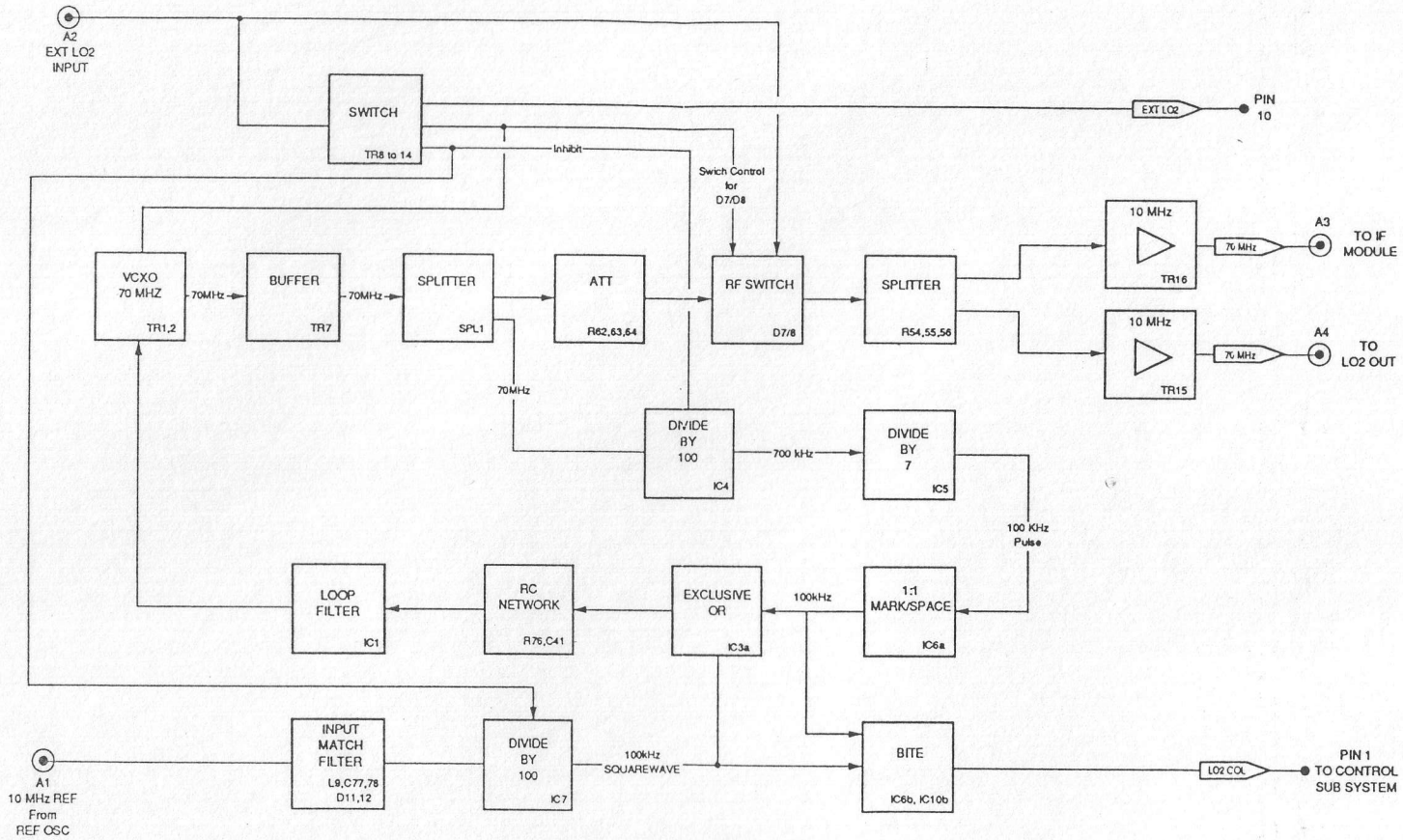
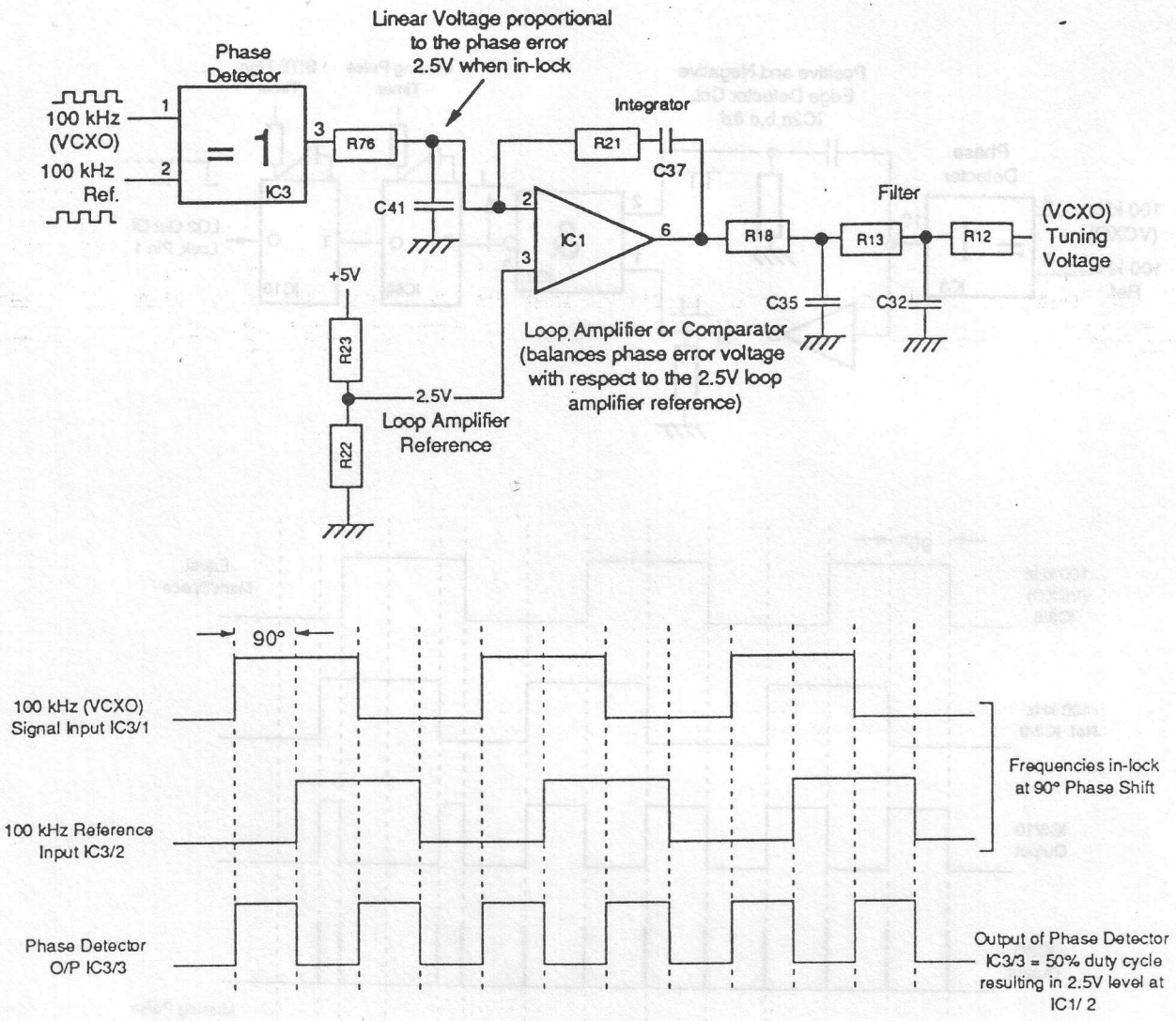


Figure 1 - Synthesiser 2 Module Simplified Block Diagram



With input frequencies in-lock

1. At 0° Phase Shift, output of Phase Detector filter = 0V
2. At 180° Phase Shift, output of Phase Detector filter = 5V

Note that because the output voltage of the Phase Detector can only swing between 0V and 5V, then the Loop Amplifier can only see a 0° to 180° phase error.

Figure 2 - Simplified Phase Detector and LOOP Amplifier

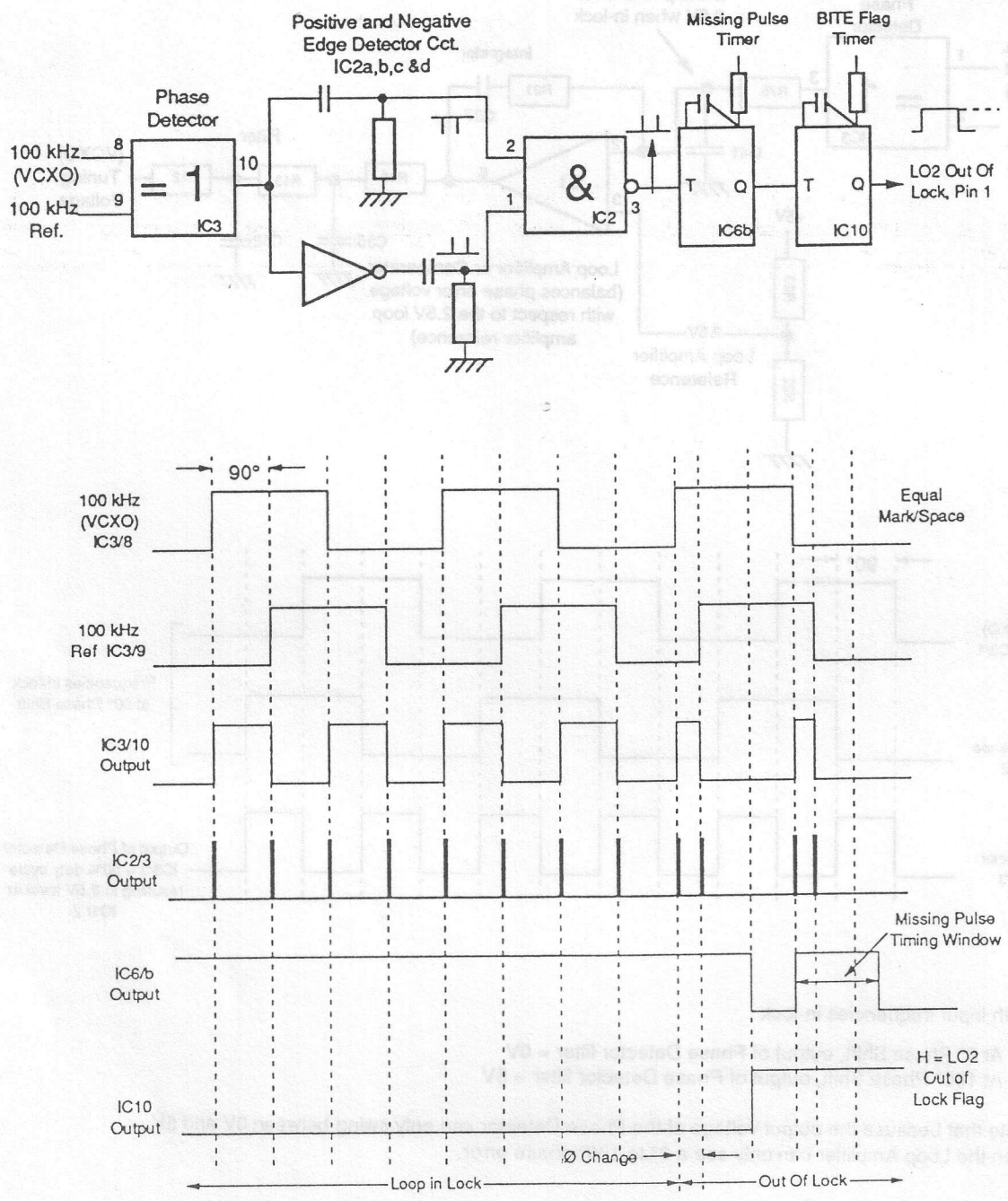


Figure 3 - Simplified BITE Circuit

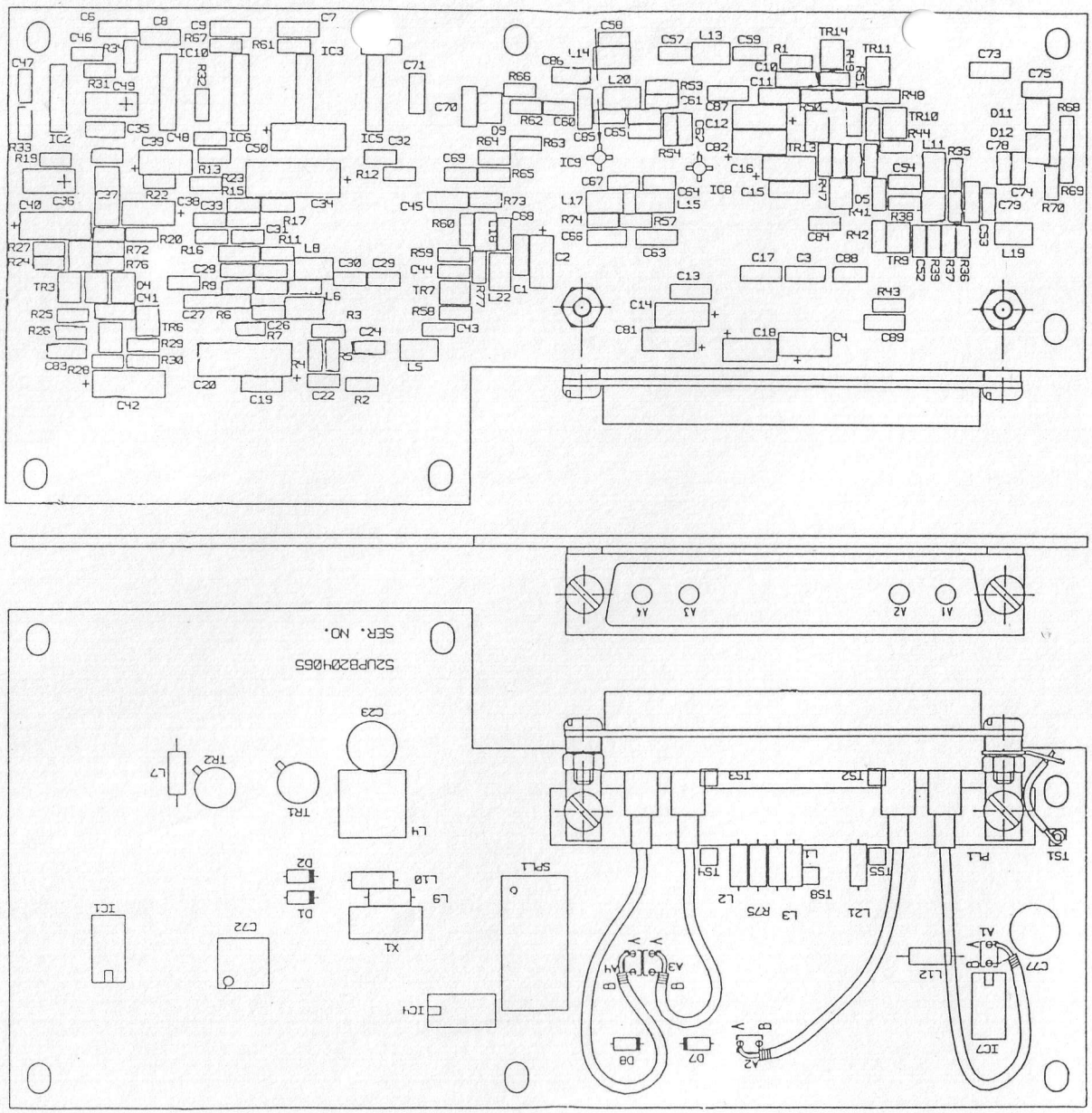


Figure 4 - Synthesiser 2 Layout Diagram

Circuit Reference	Description	Value
C1	Capacitor, fixed, ceramic chip, 100%, 50V	100n
C2	Capacitor, solid tant chip, 10%, 35V	1µ
C3	Capacitor, fixed, ceramic chip, 100%, 50V	100n
C4	Capacitor, solid tant chip, 10%, 35V	1µ
C5 to C11	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C12	Capacitor, solid tant chip, 10%, 35V	1µ
C13	Capacitor, fixed, ceramic chip, 10% 50V	100n
C14	Capacitor, solid tant chip, 10%, 35V	1µ
C15	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C16	Capacitor, solid tant chip, 10%, 35V	1µ
C17	Capacitor, fixed, ceramic chip, 10%, 500V	100n
C18	Capacitor, solid tant chip, 10%, 35V	1µ
C19	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C20	Capacitor, solid tant chip, 10%, 35V	10µ
C21	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C22	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C23	Capacitor, variable, Film Dielectric Trimmer, 300V	2p-18p
C24	Capacitor, fixed, ceramic chip, 5%, 100V	10p
C25	Capacitor, fixed, ceramic chip, 5%, 100V	220p
C26	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C27 & C28	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C29 & C30	Capacitor, fixed, ceramic chip, 5%, 100V	68p
C31	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C32 & C33	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C34	Capacitor, solid tant chip, 10%, 35V	10µ
C35	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C36	Capacitor, fixed, solid tant, 10%, 35V	1µ
C37	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C38 & C39	Capacitor, solid tant chip, 10%, 35V	1µ
C41	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C43	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C44	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C47	Capacitor, fixed, ceramic chip, 5%, 100V	27p

Circuit Reference	Description	Value
C45	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C46 & C47	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C48	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C49	Capacitor, solid tant chip, 10%, 35V	1µ
C50	Capacitor, solid tant chip, 10%, 10V	10µ
C51	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C52	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C53	Capacitor, fixed, ceramic chip, 10%, 500V	100n
C54	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C55	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C57 & C58	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C59 to C62	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C63	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C64 & C65	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C66	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C67	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C68	Capacitor, fixed, ceramic chip, ±0.5p, 100V	4p7
C69	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C70 & C71	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C72	Capacitor, fixed, polystrene, 1%, 63V	470p
C73	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C74	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C75	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C77	Capacitor, variable, film dielectric trimmer, 300V	2p-18p
C78	Capacitor, fixed, ceramic chip, 5%, 100V	10p
C79	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C81 & C82	Capacitor, fixed, solid tant chip, 10%, 35V	1µ
C84	Capacitor, S.O.T.	
C85	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C86 & C87	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C88 & C89	Capacitor, fixed, ceramic chip, 10%, 50V	100n

Circuit Reference	Description	Value
LI & L2	Choke, fixed RF, 10%	15µ
L3	Choke, fixed RF, 10%	1m
L3	Choke, fixed, chip coil, 20%	820n
L4	Choke, wound	
L5	Choke, fixed RF, 10%	1µ5
L6	Choke, fixed RF, 10%	47n
L7	Choke, fixed, RF,10%	100n
L8	Choke, fixed RF, 10%	47n
L9 & L10	Choke, fixed RF, 10%	680n
L11	Choke, fixed RF, 10%	1µ5
L12	Choke, fixed RF, 10%	15µ
L13 & L14	Choke, fixed RF, 10%	2µ2
L17	Choke, fixed RF, 10%	2µ2
L18	Choke, fixed RF, 10%	1µ
L19	Choke, fixed RF, 10%	10µ
L20	Choke, fixed RF, 10%	47n
L21	Choke, fixed RF, 10%	15µ
L22	Choke, fixed RF, 10%	47n
IC1	Single low noise OP-AMP, NE5534AN	
IC2	Quad 2-Input Nand Gate, HEF4011BT	
IC3	Quad Excl-OR Gate, HEF4070BT	
IC4	Fixed Modulus H/S Divider X 100, SP8629DP	
IC5	Programmable 4 Bit Binary Down Counter, HEF4526BT	
IC6	Dual Retriggerable Resettable Monostable Multivibrator, HEF4528BT	
IC7	Fixed Modulus H/S Divider X 100, SP8629DP	
IC8 & IC9	Monolithic Amplifier, Mini-circuits Mar-4	
IC10	Dual Prec Monostable Multivibrator, HEF4538BT	
R1	Resistor, fixed, chip, 2%, 0.1W	10R
R2	Resistor, fixed, chip, 1%, 0.1W	1k
R3	Resistor, fixed, chip, 1%, 0.1W	10k
R4	Resistor, fixed, chip, 2%, 0.1W	51R

Circuit Reference	Description	Value
R5	Resistor, fixed, chip, 1%, 0.1W	100R
R6	Resistor, fixed, chip, 2%, 0.1W	51R
R7	Resistor, fixed, chip, 2%, 0.1W	51R
R8	Resistor, fixed, chip, 1%, 0.1W	100R
R9	Resistor, fixed, chip, 1%, 0.1W	4k7
R10	Resistor, fixed, chip, 1%, 0.1W	1k5
R11	Resistor, fixed, chip, 1%, 0.1W	1k
R12	Resistor, fixed, chip, 1%, 0.1W	2k2
R13	Resistor, fixed, chip, 1%, 0.1W	1k
R14	Resistor, fixed, chip, 1%, 0.1W	2k2
R15	Resistor, fixed, chip, 1%, 0.1W	1k
R16	Resistor, fixed, chip, 1%, 0.1W	47k
R17	Resistor, fixed, chip, 1%, 0.1W	220k
R18	Resistor, fixed, chip, 1%, 0.1W	510k
R19 & R20	Resistor, fixed, chip, 1%, 0.1W	220R
R21	Resistor, fixed, chip, 1%, 0.1W	510k
R22 & R23	Resistor, fixed, chip, 1%, 0.1W	10k
R31	Resistor, fixed, chip, 1%, 0.1W	4k7
R32	Resistor, fixed, chip, 1%, 0.1W	15k
R33	Resistor, fixed, chip, 1%, 0.1W	4k7
R34	Resistor, fixed, chip, 1%, 0.1W	1M
R35 to R37	Resistor, fixed, chip, 1%, 0.1W	10k
R38	Resistor, fixed, chip, 1%, 0.1W	100R
R39	Resistor, fixed, chip, 1%, 0.1W	2k7
R40	Resistor, fixed, chip, 1%, 0.1W	150k
R41	Resistor, fixed, chip, 1%, 0.1W	1K
R42	Resistor, fixed, chip, 1%, 0.1W	4k7
R43	Resistor, fixed, chip, 1%, 0.1W	2k2
R44 & R45	Resistor, fixed, chip, 1%, 0.1W	4k7
R46	Resistor, fixed, chip, 1%, 0.1W	330k
R47	Resistor, fixed, chip, 1%, 0.1W	10k
R48 & R49	Resistor, fixed, chip, 1%, 0.1W	4k7
R50	Resistor, fixed, chip, 1%, 0.1W	1k

Circuit Reference	Description	Value
TR1 & TR2	Transistor, switching, NPN, BRS13	
TR& to TR9	Transistor, NPN, NEO2133	
TR10 & TR11	Transistor, switching, PNP, BSR15	
TR12 & TR13	Transistor, switching, NPN, BSR13	
TR14	Transistor, switching PNP, BSR16	

Synthesiser 2 Module Items List - Sheet 6 of 6

Circuit Reference	Description	Value
R51	Resistor, fixed, chip, 1%, 0.1W	8k2
R53	Resistor, fixed, chip, 1%, 0.1W	2k7
R54 to R56	Resistor, fixed, chip, 2%, 0.1W	51R
R57	Resistor, fixed, chip, 2%, 0.1W	47R
R58	Resistor, fixed, chip, 1%, 0.1W	470R
R59	Resistor, fixed, chip, 1%, 0.1W	4k7
R60	Resistor, fixed, chip, 1%, 0.1W	6k8
R61	Resistor, fixed, chip, 1%, 0.1W	220R
R62	Resistor, S.O.T.Set	
R63	Resistor, S.O.T.Set	
R64	Resistor, S.O.T.Set	
R65	Resistor, fixed, chip, 2%, 0.1W	22R
R66	Resistor, fixed, chip, 1%, 0.1W	47k
R67	Resistor, S.O.T.Set	
R68	Resistor, fixed, chip, 1%, 0.1W	15k
R69	Resistor, fixed, chip, 1%, 0.1W	4k7
R70	Resistor, fixed, chip, 1%, 0.1W	10k
R72	Resistor, fixed, chip, 1%, 0.1W	27k
R73	Resistor, fixed, chip, 1%, 0.1W	180R
R74	Resistor, fixed, chip, 2%, 0.1W	47R
R75	Resistor, fixed, metal oxide, 2%, 0.25W	10R
R76	Resistor, fixed, chip, 1%, 0.1W	10k
R77	Resistor, fixed, chip, 1%, 0.1W	470R
R78	Resistor, fixed, chip, 2%, 0.1W	10R
D1 & D2	Diode, tuning, BB405B	
D5	Diode, silicon planar high speed switching, BAS16	
D7 & D8	Diode, P-I-N, HP5082-3188	
D9	Diode, silicon planar high speed switching, BAS16	
D11 & D12	Diode, silicon planar high speed switching, BAS16	

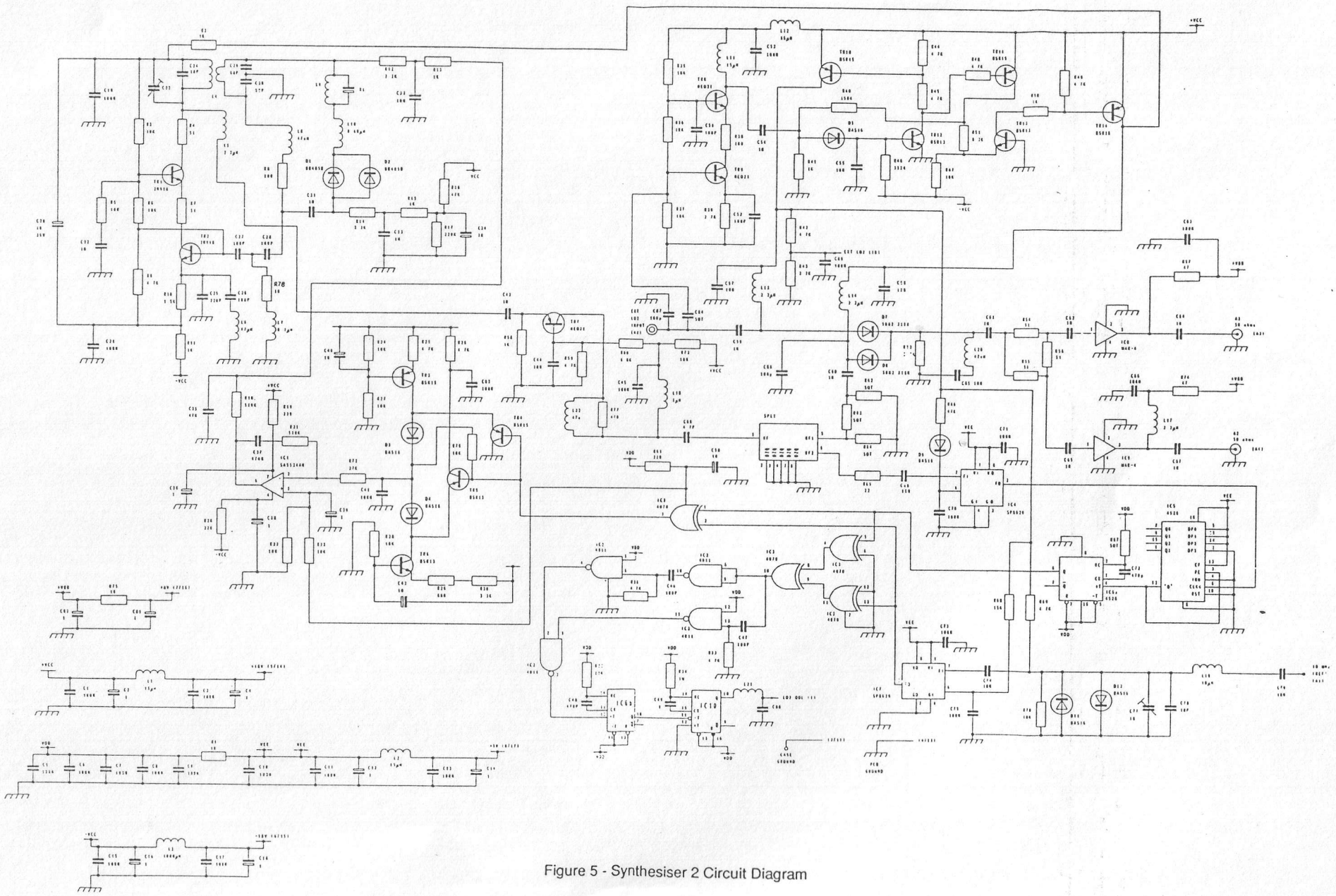


Figure 5 - Synthesiser 2 Circuit Diagram

Chapter 6.5

REFERENCE OSCILLATOR MODULE

1 INTRODUCTION

The Reference Oscillator Module comprises a single printed circuit board housed in a screened enclosure and occupies SK6 of the RF backplane within the receiver. A single connector carries both RF and DC signals.

This module description is given with reference to the following drawings, illustrations and items lists:

- Figure 1 Reference Module Simplified Block Diagram
- Figure 2 Simplified Phase Detector and Loop Amplifier
- Figure 3 Reference Module Layout Diagram
- Items List Reference Module, Sheets 1 to 7 inc
- Figure 4 Reference Module Circuit Diagram

In a standard STR8212 receiver the Reference Oscillator Module consists of a 10 MHz Temperature Compensated Crystal Oscillator (TXCO) to which is locked a 80 MHz Voltage Controlled Crystal Oscillator (VCXO). The module provides the following fully buffered outputs:

- 80 MHz to ADC Module
- 40 MHz to DAC/SEQ Module
- 20 MHz to LO1 Synthesiser Module
- 10 MHz to REF OUT connection on backpanel
- 10 MHz to LO2 Synthesiser Module

2 MODULE DESCRIPTION

Module description is given under the following headings:

- Block Diagram
- Typical Signal Levels
- Options

2.1 Block Diagram

The module incorporates a synthesised phase-locked loop with outputs at 80, 40 and 20 MHz and two outputs at 10 MHz.

The phase-locked loop consists of a Voltage Controlled Crystal Oscillator (VCXO) operating at 80 MHz. The output of this VCXO is divided down and the output at 10 MHz is fed, via suitable buffering, to a phase detector. The other input to this phase detector is derived from the basic 10 MHz reference (TCXO) and its output is fed via an amplifier and loop filter to control the VCXO (80 MHz). The circuit forms the phase-lock loop which locks the VCXO to eight times the frequency of the 10 MHz reference.

The basic frequency reference is provided by a crystal oscillator at 10 MHz. In the standard unit this is a Temperature Compensated Crystal Oscillator (TCXO) but an oven controlled crystal oscillator (OXCO) is available as an option.

The module has a facility for operating from an external 10 MHz reference. When the external reference is above a certain threshold level this is detected and the circuit switches over-automatically to operate on the external reference. The switch circuit also switches off the internal reference oscillator. A logic output is also provided to give an indication when an external reference is present.

A BITE circuit is incorporated, this provides a logic output to the radio BITE function when the circuit is out of lock.

The basic building blocks of this module are:

- Voltage Controlled 80 MHz Crystal Oscillator (VCXO)
- Divider
- Phase Detector
- Loop Filter Amplifier
- Internal 10 MHz Reference Crystal Oscillator (TCXO)
- Output Buffers
- Internal/External Reference Switch

2.2 Typical Signal Levels

The typical synthesised output signal level for the 80 MHz at A5 is 8dBm (+6dBm to +9dBm) whilst the 40, 20 and 10 MHz outputs at A3, A2, A6 and A7 are typically 6dBm (+3dBm to +9dBm). The external reference, if used, should typically be 0dBm (minimum -5dBm and maximum +1dBm) and its frequency within 5 ppm of 10 MHz.

2.3 Options

Provision is made on the printed circuit board for the incorporation of an oven controlled crystal oscillator (OCXO) to enhance the frequency stability to typically ±0.001 ppm. Circuitry for TR9, RL1 to isolate the supply to the OCXO during 'external reference' input is part of the OCXO installation.

3 CIRCUIT DESCRIPTION

Circuit description is given under the following headings:

- Voltage Controlled Crystal Oscillator . . . . . Paragraph 3.1
- Divider . . . . . Paragraph 3.2
- Phase Detector . . . . . Paragraph 3.3
- Loop Filter Amplifier . . . . . Paragraph 3.4
- Internal 10 MHz Reference Crystal Oscillator (TCXO) . . . . . Paragraph 3.5
- Output Buffers . . . . . Paragraph 3.6
- Internal/External Reference Switch . . . . . Paragraph 3.7

3.1 Voltage Controlled Crystal Oscillator

The 80 MHz voltage controlled crystal oscillator (VCXO) forms the heart of the phase-locked loop. The circuit is a low distortion, Colpitts oscillator with a cascode amplifier (L1, TR1 and TR2) which is locked by the varactor tuned 80 MHz crystal (D1, D2 and X1). The varactor voltage is supplied via the loop filter amplifier, IC3 pin 6. The output from the cascode amplifier (TR1, TR2) is buffered by a common-base buffer, TR18 into the 80 MHz output buffer amplifier and also the synthesiser, high speed divider IC1.

3.2 Divider

High speed divider, IC1 divides the 80 MHz (VCXO) down to 10 MHz for phase comparison with the reference 10 MHz. The 10 MHz output from the divider is buffered by IC2(b) into the phase comparator IC2(a) as well as by an adjustable output level buffer IC2(c) into two separate buffer amplifiers for the two 10 MHz module outputs.

3.3 Phase Detector

Phase detector IC2(a) is an exclusive OR or digital phase detector with R17 and C16 providing low-pass filtering. The divided-down 80 MHz (VCXO) frequency at 10 MHz is compared, via the phase detector, with the Reference 10 MHz. The digital output is low-pass filtered, (R17 and C16) to give a voltage that is directly proportional to the phase error. This phase detector error voltage is fed to the Loop Amplifier (IC3) and also to the BITE circuitry (IC4) for out-of-lock detection for the 'Out of Lock' indication at pin 8 output of the module.

3.4 Loop Filter Amplifier

Loop filter amplifier IC3, in conjunction with R15, R16 and C13, provide the loop stability function as well as a buffered drive voltage for the varactor tuning of the 80 MHz crystal in the (VCXO). It is essentially a voltage comparator to balance the Phase detector error voltage at C16 with the 2.5V reference level, set between R21 and R22. The loop amplifier reference is set to 2.5V to allow an increase or decrease of phase in order to balance the loop at 90° phase, which is also the frequency lock point. The maximum increase or decrease in phase allowable at the set reference is 0° to +180°, due to the 0V to +5V swing at IC2(a) output.

3.5 Internal 10 MHz Reference Crystal Oscillator (TCXO)

The internal 10 MHz reference crystal oscillator (TCXO) is a self contained temperature compensated unit with trim, achieved via R111. The TCXO sets the performance level of the phase-locked synthesiser to ±2 ppm over the full temperature range. It is used as the reference to one side of the phase comparator IC2(a) after being buffer/limited via TR13 circuitry.

3.6 Output Buffers

All module synthesised outputs are buffered by common-base buffer amplifiers and are output as sine waves to reduce the EMC problems. They are tuneable transformer coupled outputs to provide ground isolation between the analogue/digital sides of the receiver. The frequency outputs are assigned as follows:

A6 - 10 MHz Reference to LO2 (Synth 2 Module)
A2 - 10 MHz Reference frequency output (from receiver)
A3 - 20 MHz Reference clock for LO1 (Synth 1 Module)
A7 - 40 MHz Reference clock for DAC/Sequencer Module
A5 - 80 MHz Reference clock for ADC Module

3.7 Internal/External Reference Switch

A level sensing switch (TR3 to TR8 and TR20) is used to sense the presence of an external 10 MHz reference of greater than -5dBm. When this is sensed, it gates off the TCXO (D11) and passes through the external reference via D12 and the buffer/limiter (TR13) into the phase comparator IC2(a). TR20 removes the supply to the TCXO during external reference input.

Hysteresis is built into the switch to prevent any indeterminancy or chatter in the switching action. Note that TR9 and RL1 are only fitted with the OCXO option and remove the supply to the OCXO upon external reference input switch.

4 ADJUSTMENTS

There are three trim-pots, one trimmer capacitor and five tuned inductor adjustments. These are factory set but with the use of appropriate test equipment, can be checked or adjusted using the following procedure.

1. Trim C2 to get the loop to lock.
2. Adjust R11 to achieve 80 MHz at A5 output (± 0.2 ppm).
3. Trim L13 to tune the 80 MHz at A5 output to maximum power (+6 to +9 dBm).
4. Trim L15 to tune the 40 MHz at A7 to maximum power (+3 to +9dBm).
5. Trim L17 to tune the 20 MHz at A3 output to maximum power.
6. Adjust R61 to set the 20 MHz at A3 output to approximately 6dBm (+3 to +9dBm).
7. Trim L27 to tune the 10 MHz at A6 to maximum power.
8. Trim L30 to tune the 10 MHz at A2 to maximum power.
9. Adjust R119 to set 10 MHz, at A6 and A2 to approximately 6dBm (+3 to +9dBm).

5 ON-LINE BITE

The out-of-lock indication, module output pin 8, is determined by the BITE circuitry. This consists of window comparator, IC4a and b, and signal presence filters (C21 and C24) in conjunction with the 4-input 'OR' gate, IC6. The window comparator determines the phase-error limits and so, the frequency limits. Signal presence filters check that the 10 MHz VCXO and reference 10 MHz signals are present, whilst the 'OR' gate buffer - outputs one or more of its input faults. Note that the window comparator outputs indicate high for a fault, as with the signal presence filters, due to their negative rectification and level shifting by D15. Module output (pin 8) is a high (1) for out-of-lock error.

6 FAULT FINDING

The front panel BITE 09 FAIL 4 should be the first indication of a fault. If the output frequencies are significantly out of specification and a high (1) is present at pin 8 of the module, then go through the adjustment sequence, (paragraph 4). If the module is still at fault, a quick logic check at the inputs to IC6 will narrow the fault to three conditions:

1. A high (1) on pin 9 or pin 10 will indicate an out-of-lock problem.

2. A high on pin 11 will indicate that the divided-down VCXO 10 MHz signal has failed.

3. A high on pin 12 will indicate that the Reference 10 MHz signal has failed.

A 10 MHz Reference signal must be present before further investigation into the phase-locked loop. Check that this signal is present at IC2(a) pin 2, if not, apply an external 10 MHz reference as in Paragraph 2.2 to check the Reference Switch and to confirm if the (TCXO) is at fault.

Next check the voltage across C16. If it is at 0V or +4.5V or over, then the loop is out-of-lock and the window comparator IC4 may not be at fault. If the voltage across C16 is at 2.5V, then the loop is working, refer to Figure 2. A voltage check across C13 with a high input impedance D.V.M. should indicate approximately -5V to -7V for an operating loop. This means that an external dc voltage to that level can be injected across C13 and a frequency/power level check can be made at the 80 MHz output A5, in order to check the function of the varactor tuning and Colpitts oscillator.

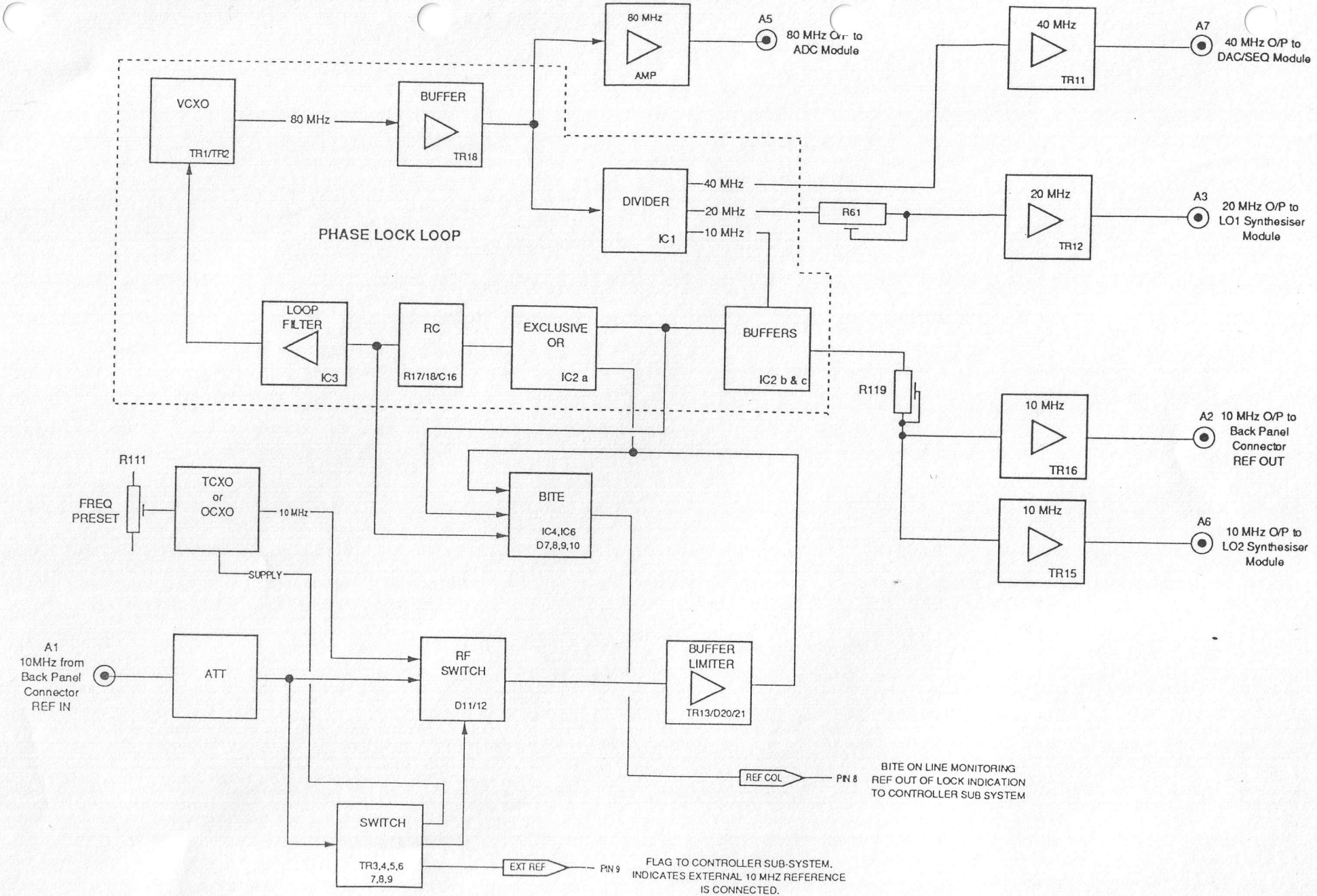
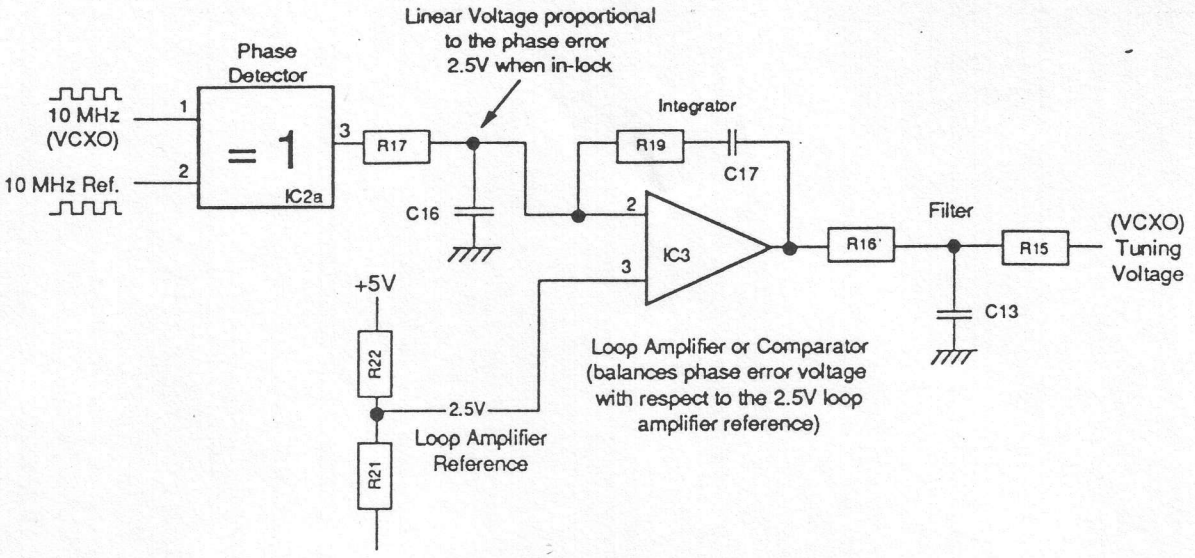
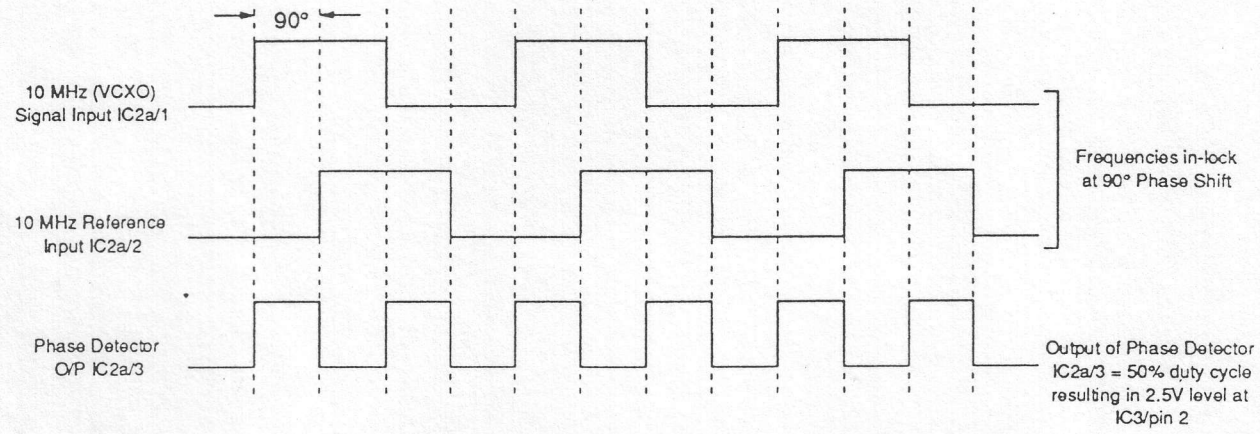


Figure 1 - Reference Module Simplified Block Diagram





With input frequencies in-lock

1. At 0° Phase Shift, output of Phase Detector filter = 0V
2. At 180° Phase Shift, output of Phase Detector filter = 5V

Note that because the output voltage of the Phase Detector can only swing between 0V and 5V, then the Loop Amplifier can only see a 0° to 180° phase error.

Figure 2 - Simplified Phase Detector and Loop Amplifier

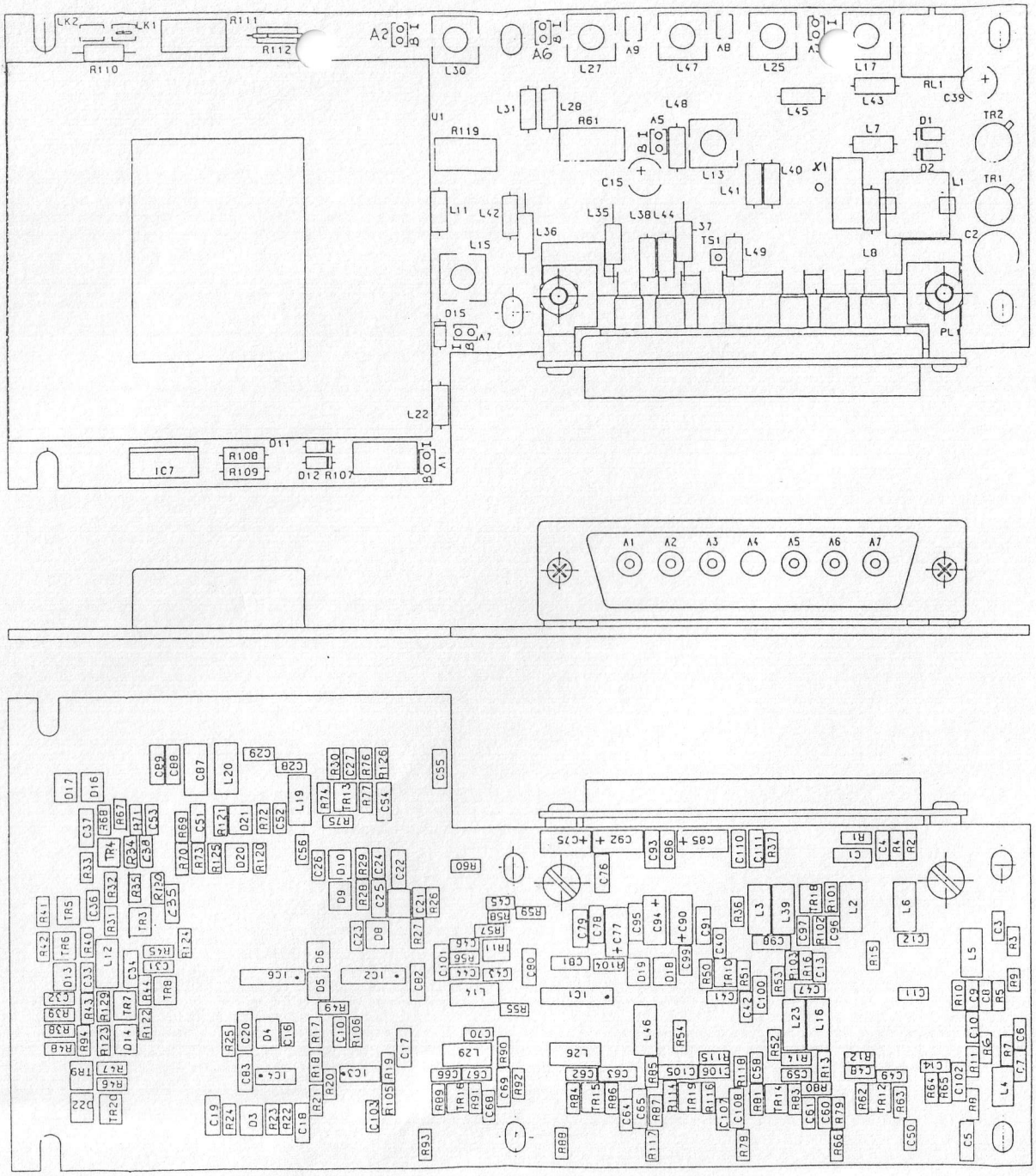


Figure 3 - Reference Module Layout Diagram

Circuit Reference	Description	Value
C1	Capacitor, fixed, ceramic chip, 100%, 50V	100n
C2	Capacitor, variable, dielectric trimmer film, 300V	2p-18p
C4	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C5	Capacitor, fixed, ceramic chip, 100%, 50V	100p
C6	Capacitor, fixed, ceramic chip, 5%, 100V	220p
C7 to C9	Capacitor, fixed, ceramic chip, 5% 100V	100p
C10	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C11 & C12	Capacitor, fixed, ceramic chip, 5%, 100V	68p
C13	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C14	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C15	Capacitor, fixed, solid tant, 10%, 35V	10µ
C16	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C17 to C20	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C21	Capacitor, fixed, ceramic chip, 10%,100V	10n
C22	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C23 & C24	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C25	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C26 to C29	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C31 & C32	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C33	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C34	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C35	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C36	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C37	Capacitor, fixed, ceramic chip, 5%, 100V	68p
C38	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C39	Capacitor, fixed, solid tant, 10%, 35V	10µ
C40 & C41	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C42	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C43	Capacitor, fixed, ceramic chip, 5%, 100V	15p
C44 & C45	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C46	Capacitor, fixed, ceramic chip, 50%, 100V	68p
C47	Capacitor, fixed, ceramic chip, 5%, 100V	27p
C48 & C49	Capacitor, fixed, ceramic chip, 10%, 100V	10n

Circuit Reference	Description	Value
C50	Capacitor, fixed, ceramic chip, 5%, 100V	180p
C51	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C52	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C53	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C54 & C55	Capacitor, fixed, ceramic chip, 10%, 500V	100p
C56	Capacitor, fixed, ceramic chip, 10% 100V	10n
C62	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C63	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C64	Capacitor, fixed, ceramic chip, 5%, 100V	35p
C65	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C66	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C67	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C68	Capacitor, fixed, ceramic chip, 5%, 100V	330p
C69	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C70	Capacitor, fixed, ceramic chip, 5%, 100V	150p
C75	Capacitor, fixed, solid tant, 10%, 35V	1µ
C76	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C77	Capacitor, fixed, solid tant, 10%, 35V	1µ
C78	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C80 to C83	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C85	Capacitor, fixed, solid tant, 10%, 35V	1µ
C86	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C90	Capacitor, fixed, solid tant, 10%, 35V	1µ
C91	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C92	Capacitor, fixed, solid tant, 10%, 35V	1µ
C93	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C94	Capacitor, fixed, solid tant, 10%, 35V	1µ
C95	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C96 & C97	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C98	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C99	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C100 to C 102	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C103 & C104	Capacitor, fixed, ceramic chip, 10%, 100V	10n

Circuit Reference	Description	- Value
C110 & C111	Capacitor, fixed, ceramic chip, 10%, 50V	100n
L1	Choke, wound,	
L2	Choke, fixed, chip coil, 20%	1µ
L3	Choke, fixed, chip coil, 20%	820n
L4	Choke, fixed, chip coil, 20%	39n
L5	Choke, fixed, chip coil, 10%	100n
L6	Choke, fixed, chip coil, 20%	47n
L7	Choke, fixed, RF,10%	470n
L8	Choke, fixed, RF, 10%	820n
L11	Choke, fixed, RF, 10%	15µ
L12	Choke, fixed, chip coil, 20%	10µ
L13	Choke, wound	
L14	Choke, fixed, chip coil, 20%	1µ
L15	Choke, wound	
L16	Choke, fixed, chip coil, 20%	2µ2
L17	Choke, wound	
L19	Choke, fixed, chip coil, 20%	10µ
L20	Choke, fixed, chip coil, 20%	330n
L22	Choke, fixed, RF, 10%	15µ
L26	Choke, fixed, chip coil, 20%	3µ3
L27	Choke, wound	
L28	Choke, fixed, RF, 10%	15µ
L29	Choke, fixed, chip coil, 20%	3µ3
L30	Choke, wound	
L31	Choke, fixed, RF, 10%	15µ
L35 & L36	Choke, fixed, RF, 10%	3µ9
L38	Choke, fixed, RF, 10%	15µ
L39	Choke, fixed, chip coil, 20%	1µ
L40 to L43	Choke, fixed, RF, 10%	15µ
L44	Choke, fixed, RF, 10%	330µ
L49	Choke, fixed, RF, 10%	15µ

Circuit Reference	Description	Value
IC1	4 Bit Binary counter, 74ACT163S	
IC2	Quad 2-Input Excl OR Gate,PC74HC86T	
IC3	OP-AMP NE5534D	
IC4	Programmable OP-AMP LM358M	
IC6	Dual 4 Input OR Gate HEF4072BT	
R1	Resistor, fixed, chip, 1%, 0.1W	470R
R2	Resistor, fixed, chip, 1%, 0.1W	10k
R3	Resistor, fixed, chip, 2%, 0.1W	51R
R4	Resistor, fixed, chip, 1%, 0.1W	100R
R5	Resistor, fixed, chip, 1%, 0.1W	10k
R6	Resistor, fixed, chip, 1%, 0.1W	4k7
R7	Resistor, fixed, chip, 1%, 0.1W	1k5
R8	Resistor, fixed, chip, 1%, 0.1W	470R
R9	Resistor, fixed, chip, 2%, 0.1W	51R
R10	Resistor, fixed, chip, 1%, 0.1W	100R
R11	Resistor, fixed, chip, 1%, 0.1W	2k2
R12	Resistor, fixed, chip, 1%, 0.1W	1k
R13	Resistor, fixed, chip, 1%, 0.1W	220k
R14	Resistor, fixed, chip, 1%, 0.1W	47k
R15	Resistor, fixed, chip, 1%, 0.1W	2k2
R16	Resistor, fixed, chip, 1%, 0.1W	1k
R17	Resistor, fixed, chip, 1%, 0.1W	2k2
R18	Resistor, fixed, chip, 1%, 0.1W	10k
R19	Resistor, fixed, chip, 1%, 0.1W	100k
R20	Resistor, fixed, chip, 1%, 0.1W	47k
R21 & R22	Resistor, fixed, chip, 1%, 0.1W	2k2
R23	Resistor, fixed, chip, 1%, 0.1W	47k
R24 & R25	Resistor, fixed, chip, 1%, 0.1W	1M
R26	Resistor, fixed, chip, 1%, 0.1W	220k
R27	Resistor, fixed, chip, 1%, 0.1W	1k
R28	Resistor, fixed, chip, 1%, 0.1W	220k
R29 & R30	Resistor, fixed, chip, 1%, 0.1W	1k

Circuit Reference	Description	Value
R31 to R33	Resistor, fixed, chip, 1%, 0.1W	10k
R34	Resistor, fixed, chip, 1%, 0.1W	2k7
R35	Resistor, fixed, chip, 1%, 0.1W	100R
R36	Resistor, fixed, chip, 1%, 0.1W	4k7
R37	Resistor, fixed, chip, 1%, 0.1W	2k2
R38	Resistor, fixed, chip, 1%, 0.1W	4k7
R39	Resistor, fixed, chip, 1%, 0.1W	1k
R40	Resistor, fixed, chip, 1%, 0.1W	330k
R41 & R42	Resistor, fixed, chip, 1%, 0.1W	4k7
R43	Resistor, fixed, chip, 1%, 0.1W	10k
R44	Resistor, fixed, chip, 1%, 0.1W	4k7
R45	Resistor, fixed, chip, 1%, 0.1W	47k
R46	Resistor, fixed, chip, 1%, 0.1W	4k7
R47	Resistor, fixed, chip, 1%, 0.1W	2k2
R49	Resistor, fixed, chip, 1%, 0.1W	6k8
R50	Resistor, fixed, chip, 1%, 0.1W	2k2
R51	Resistor, fixed, chip, 2%, 0.1W	51R
R52	Resistor, fixed, chip, 1%, 0.1W	6k8
R53	Resistor, fixed, chip, 1%, 0.1W	12k
R54 & R55	Resistor, fixed, chip, 1%, 0.1W	2k2
R56	Resistor, fixed, chip, 1%, 0.1W	1k5
R57	Resistor, fixed, chip, 2%, 0.1W	51R
R58	Resistor, fixed, chip, 1%, 0.1W	6k8
R59	Resistor, fixed, chip, 1%, 0.1W	12k
R60	Resistor, fixed, chip, 1%, 0.1W	2k2
R61	Resistor, variable cermet, 10%, 0.5W	10k
R62	Resistor, fixed, chip, 1%, 0.1W	1k5
R63	Resistor, fixed, chip, 2%, 0.1W	51R
R64	Resistor, fixed, chip, 1%, 0.1W	6k8
R65	Resistor, fixed, chip, 1%, 0.1W	12k
R66	Resistor, fixed, chip, 1%, 0.1W	2k2
R67	Resistor, fixed, chip, 1%, 0.1W	470R
R68	Resistor, fixed, chip, 2%, 0.1W	10R

Circuit Reference	Description	Value
R71	Resistor, fixed, chip, 1%, 0.1W	470R
R73	Resistor, fixed, chip, 1%, 0.1W	470R
R74	Resistor, fixed, chip, 1%, 0.1W	1k5
R75	Resistor, fixed, chip, 2%, 0.1W	51R
R76	Resistor, fixed, chip, 1%, 0.1W	12k
R77	Resistor, fixed, chip, 1%, 0.1W	6k8
R84	Resistor, fixed, chip, 1%, 0.1W	1k5
R85	Resistor, fixed, chip, 1%, 0.1W	6k8
R86	Resistor, fixed, chip, 2%, 0.1W	51R
R87	Resistor, fixed, chip, 1%, 0.1W	12k
R88	Resistor, fixed, chip, 1%, 0.1W	2k2
R89	Resistor, fixed, chip, 1%, 0.1W	1k5
R90	Resistor, fixed, chip, 1%, 0.1W	6k8
R91	Resistor, fixed, chip, 2%, 0.1W	51R
R92	Resistor, fixed, chip, 1%, 0.1W	12k
R93	Resistor, fixed, chip, 1%, 0.1W	2k2
R101	Resistor, fixed, chip, 1%, 0.1W	680R
R102	Resistor, fixed, chip, 1%, 0.1W	6k8
R103	Resistor, fixed, chip, 1%, 0.1W	12k
R104	Resistor, fixed, chip, 2%, 0.1W	51R
R105 & R106	Resistor, fixed, chip, 1%, 0.1W	680R
R111	Resistor, variable cermet, 10%, 0.5W	20k
R119	Resistor, variable cermet, 10%, 0.5W	10k
R120 & R121	Resistor, fixed, chip, 1%, 0.1W	6k8
R122	Resistor, fixed, chip, 1%, 0.1W	15k
R123 & R124	Resistor, fixed, chip, 1%, 0.1W	470R
R125	Resistor, fixed, chip, 2%, 0.1W	22R
R126	Resistor, fixed, chip, 1%, 0.1W	100R
R129	Resistor, fixed, chip, 1%, 0.1W	5k6
R130	Resistor, fixed, chip, 1%, 0.1W	100R
R131 & R132	Resistor, fixed, chip, 1%, 0.1W	100k

Reference Module Items List - Sheet 6 of 7

Circuit Reference	Description	Value
D1 & D2	Diode, Tuning, BB405B	
D3 to D10	Diode, Silicon Planar, High Speed Switching, BAS16	
D11 & D12	Diode, P-I-N 5082-3188	
D1 & D14	Diode, Silicon Planar, High Speed Switching, BAS16	
D15	Diode, Zener, 5V6 5% 400mW, BZX79C5V6	
D16 to D21	Diode, Silicon Planar, High Speed Switching, BAS16	
D22	Diode, IN4148	
TR1 & TR2	Transistor, PAD, T018-007	
TR3	Transistor, Switching, NPN, BSR13	
TR4	Transistor, RF, NPN, BRF92A	
TR5	Transistor, Switching, PNP, BSR15	
TR6 & TR7	Transistor, Switching, NPN, BSR13	
TR8	Transistor, Switching, PNP, BSR15	
TR10 to TR13	Transistor, High frequency, NPN, BFS20	
TR15 & TR16	Transistor, High frequency, NPN, BFS20	
TR18	Transistor, High frequency, NPN, BFS20	

Reference Module Items List - Sheet 7 of 7

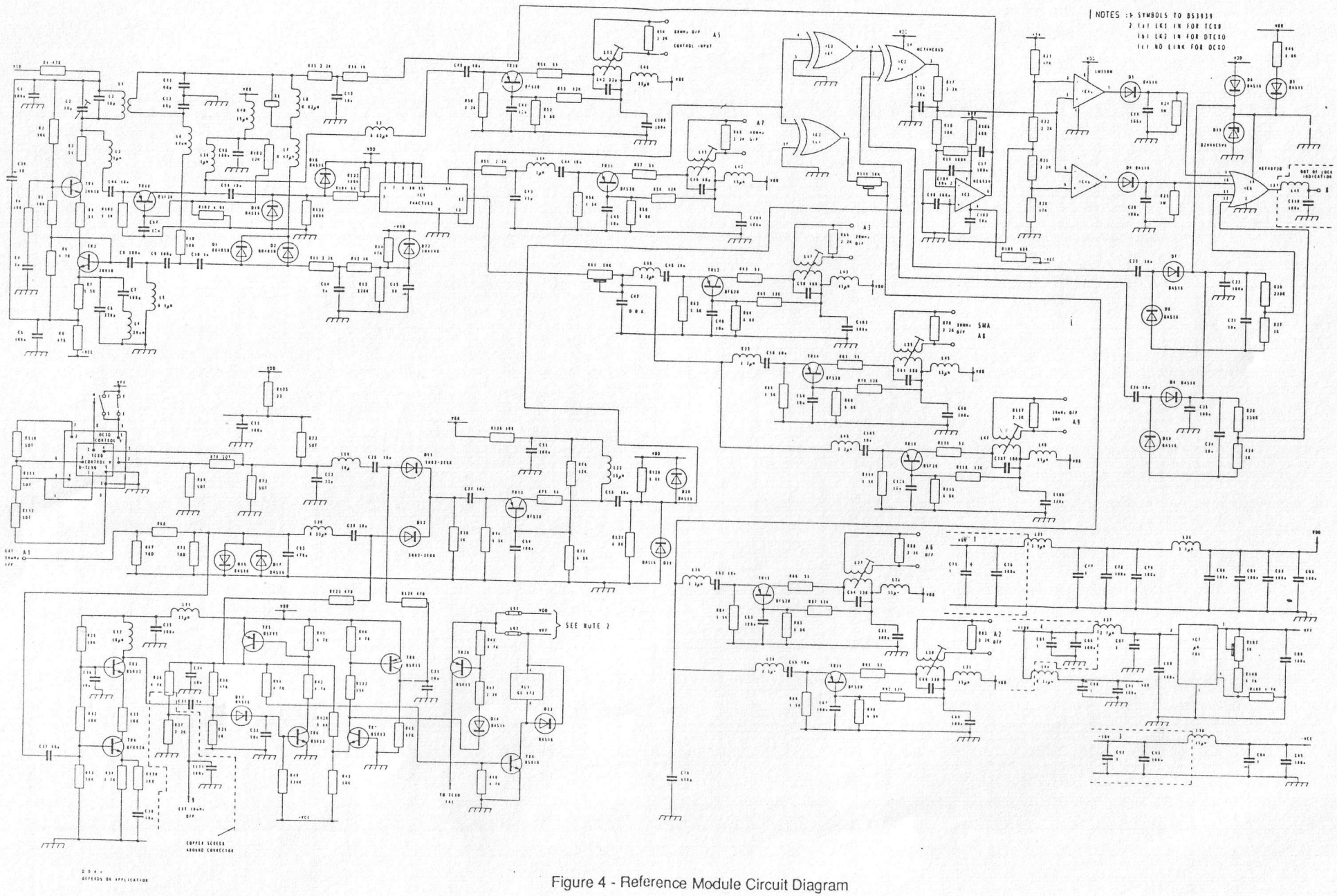


Figure 4 - Reference Module Circuit Diagram

ANALOGUE TO DIGITAL CONVERTER (ADC) MODULE

1 INTRODUCTION

The ADC module comprises 2 PCBs, ADC Board Assembly 52UPB504079 and ADC Buffer Board Assembly 52UPB504111, housed in a screened enclosure. The module has two connectors, one of these (PL1) plugs directly into a socket on the radio chassis which is connected to the RF Backplane and the other (PL2) is connected by a flying lead to PL39 on the Digital Backplane.

Module description is given with reference to the following drawings/illustrations and items list:

- Figure 1 Analogue to Digital Converter Simplified Block Diagram
- Figure 2 Analogue to Digital Converter Signal Flow and Timing Diagrams
- Figure 3 Digital Filter (PMRDF) Block Diagram
- Figure 4 Pulse Density Modulator Block Diagram
- Figure 5 Passband Spectrum of Baseband ADC Module
- Figure 6 Analogue to Digital Converter Layout Diagram
- Figure 7 Analogue to Digital Converter Buffer Board Layout Diagram
- Items list Analogue to Digital Converter, sheets 1 to 3 inc.
- Figure 8 Analogue to Digital Converter Circuit Diagram

2 MODULE DESCRIPTION

The function of the Analogue to Digital Converter (ADC) is to convert the radio's 2nd IF, centred on 50 kHz, to baseband digital data. It achieves this to an accuracy of approximately 22 bits (130 dB).

The ADC is a compact module containing two custom designed chips, a programmed logic chip (PAL) and a minimum of discrete components to achieve its function. The custom chips are a Pulse Density Modulator (PDM) [single bit ADC] and a digital filter chip. The PDM is fabricated using a bipolar process whilst the digital filter and PAL are fabricated in CMOS.

The PDM is in the form of a Sigma-Delta modulator that samples at many times the final Nyquist rate. Subsequently a large number of data points are averaged to achieve a highly accurate estimate of the analogue input signal in the digital filter. This averaging (decimation) process increases the number of bits of precision in the sample, at the expense of decreasing the sample rate by the decimation factor.

The digital filter chip (PMRDF) is configured so that the input signal frequency bandwidth is 20 kHz, centered at 50 kHz. This is achieved by using an overall decimation ratio of 2400 and an input sample rate of 80 MHz resulting in an output sample rate of 33.333 kHz.

3 CIRCUIT DESCRIPTION

Figure 1 shows the ADC split into its separate circuit blocks. Figure 2 expands on the blocks of Figure 1 to show the individual signals and the signal flow through the ADC. In Figure 2 waveforms and signal levels have also been shown at appropriate points to aid fault diagnosis.

The circuit description for the ADC module is given under the following headings:

- Anti-Alias Filter . . . . . Paragraph 3.1
- Input Protection Circuit . . . . . Paragraph 3.2
- Pulse Density Modulator . . . . . Paragraph 3.3
- Buffer Board . . . . . Paragraph 3.4
- Programmable Multi-Rate Digital Filter (PMRDF) . . . . . Paragraph 3.5

3.1 Anti-Alias Filter

The anti-alias filter is a low pass Cauer type which, in conjunction with the roofing filter in the IF module and the PMRDF filter, provides rejection to alias responses caused by sampling. The anti-alias filter's contribution to the rejection of the first alias band (100 kHz above the 2nd IF frequency) is approximately 30 dB.

3.2 Input Protection Circuit

The input protection circuit limits the input signal to 5.6 Volts peak to peak which is twice the ADC input saturation level but well below the damage level of the PDM input.

3.3 Pulse Density Modulator

Figure 4 shows a block diagram of the PDM chip. The PDM is a Sigma-Delta Coder configured as a first order lowpass quantiser surrounded by a high gain second order lowpass feedback loop. The PDM has a differential input and complementary ECL data and clock outputs. The average density of logic ones in the data output is directly proportional to the magnitude of the analogue input. The PDM chip is powered by its own regulated 6.2 Volt supply derived from the +8 Volt external supply.

3.4 Buffer Board

Both the PDM output and the PMRDF input ultilise non-standard logic levels to conserve power. The Buffer board shifts the logic levels of the PDM output up to the levels required by the PMRDF input.

3.5 Programmable Multi-Rate Digital Filter (PMRDF)

The PMRDF chip down samples and filters the one bit data stream from the Pulse Density Modulator, converting this single bit input data to a multi-bit output (complex) word at the much lower output sample rate. The digital filter uses a PAL (Programmable Array Logic) chip for control and to provide the quarter rate complex digital mix function. The digital filter output data is provided as two serial 32 bit words, each word consists of 30 data bits plus two redundant "zeros". A frame sync, word sync and clock output are produced along with the data output I and Q words. Although the PMRDF chip has been designed to be programmable, in this application the filter decimation factors and coefficients are fixed.

As shown in Figure 1 the PMRDF comprises three digital filters in series. The pre-filter has a $sinc^2$ response and decimates by a factor of 8. The conversion filter has a $sinc^4$ response and decimates by a factor of 50. The final 120 tap FIR filter decimates by a factor of 6. The overall decimation factor is thus 2400. Between the conversion filter and the final FIR filter the signal is fed through the PAL. In the PAL a pair of quadrature digitally generated 50 kHz signals are mixed with the main signal at 200 kHz to produce the complex (I and Q) baseband signal. The final FIR filter is thus formed of two independent filter blocks, one for each of the I and Q channels. The outputs from the I an Q final filters are time multiplexed together to form a single serial data output signal.

The timing diagram for the serial data output is shown on Figure 2. The I and Q data output forms a 64 bit block, the first 32 bits represent the I data and the second 32 bits represent the Q data. The start of each data block is synchronised by the FRAME SYNC output which goes low for one clock cycle. The frequency of the FRAME SYNC output represents the output sample rate of the PMRDF. The WORD SYNC output divides the 64 bit data block into four 16 bit words. The WORD SYNC output goes high for one clock cycle at the start of each 16 bit word.

The PMRDF has built in self test procedure controlled by the PAL. An output from the PAL is sent to the radio's control processor to confirm that the PMRDF and PAL have passed their self tests. The self test procedure is initiated each time the ADC receives a /TSTEN signal. Figure 3 shows the distribution of the control and self test signals and Table 1 describes the BITE and Control Signal functions.

TABLE 1 BITE AND CONTROL SIGNAL DESCRIPTION

Signal Name	Description
/RESET	Active low signal from the Controller to signal that a reset to default conditions is required. There are three causes for /RESET going active. Power on reset:- /RESET goes active for approximately 200 mS after the application of +5v to the Digital backplane. Software reset:- an instruction in the Controller software causes the reset signal to go active. Manual Reset:- /RESET goes active whilst SW1 on the Controller is depressed. /RESET is normally a logic high.
/TSTEN	Active low signal taken low by the Controller to signal the PMRDF that it should start its BITE testing. /TSTEN is normally a logic high.
/TSTVAL	/TSTVAL goes logic low to high after /TSTEN goes low whilst the PMRDF is performing its BITE tests. /TSTVAL goes logic low at the completion of BITE testing to indicate that the state of /TSTPASS is valid.
/TSTPASS	A logic low on /TSTPASS after a logic high to low transition on /TSTVAL indicates that the PMRDF has passed its BITE tests. /TSTPASS is normally a logic low.
PMRDF F	Not used.
PMRDF S	Not used.
SERCLK	Not used.
SERDATA	Not used.
/LOAD C	Not used.

4 ALIGNMENT AND DIAGNOSTIC NOTES

CAUTION

Alignment of the ADC module requires specialist equipment, a data capture unit, which is not available to service engineers. It is strongly recommended that no attempt is made to adjust the ADC module in the field.

There are four adjustable components in the ADC module.

RV1	Factory preset to control the DC offset of the PDM.
L1, L2 and L3	Factory preset to control the response of the anti-alias filter.

4.1 Failure Indication Interpretation

A power-on or user initiated BITE failure message showing failure code 1, 71, 101 or 171 for module 4, the PMRDF, indicates a fault in the PAL. It does not necessarily indicate a PMRDF fault.

If a failure occurs when carrying out the Sensitivity Tests of the STR8212 radio performance checks, then, providing that the RF and IF modules are known to be good, the fault is probably due to a defective PDM.

Figure 2 has been annotated with waveforms and signal levels to allow the service engineer to trace signals around the module.

4.2 Testing ADC Module (With Digital Output Board Fitted)

If a Digital Output board is fitted and if the data from it can be processed by a floating point Fast Fourier Transform of not less than 4096 points then it is possible to directly test the ADC module's performance.

Remove the IF Module and use a low distortion LF signal generator to apply a 51 kHz sine wave input at 1.44 Volts peak to peak to RF Backplane SK1 (IF Module) pin 1 with respect to pin 14.

Note: *that since the ADC has a low input impedance (approx 10 ohms) the input signal level should be measured.*

The resulting spectral plot should show a single output tone at 1 kHz of amplitude 24 dB below clip and an average noise level of better than -120 dB with respect to clip at 1 kHz from the carrier. The ADC's clipping level corresponds to an output of #7FFFFF. Figure 5 shows the general form expected for this spectrum.

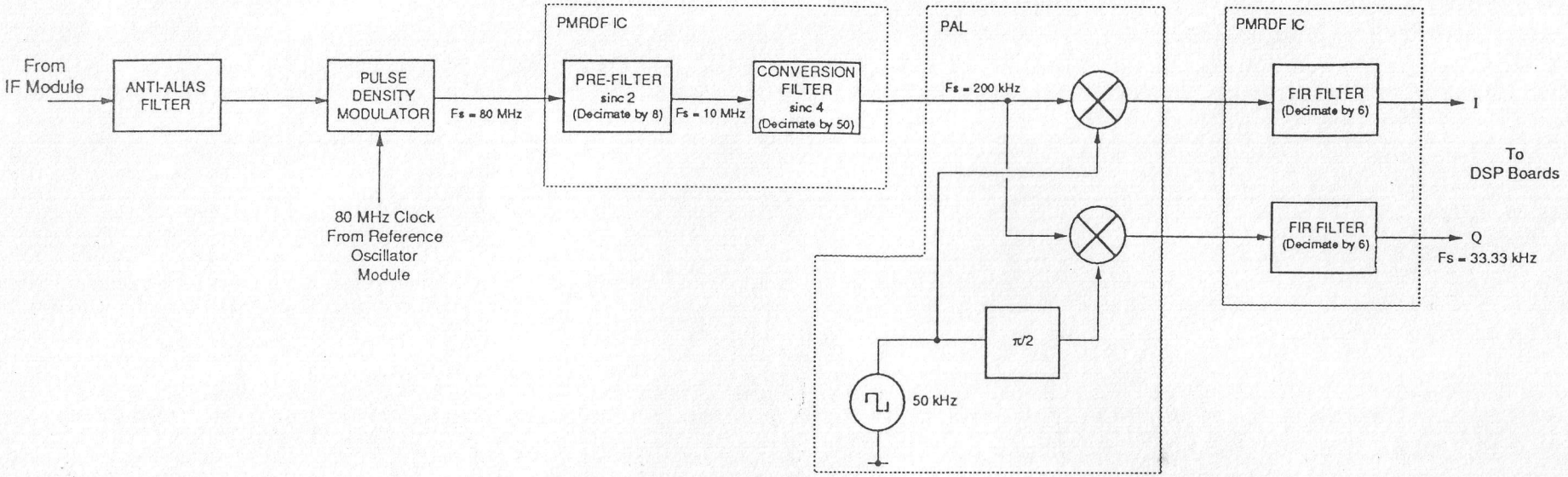


Figure 1 - Analogue to Digital Converter Simplified Block Diagram

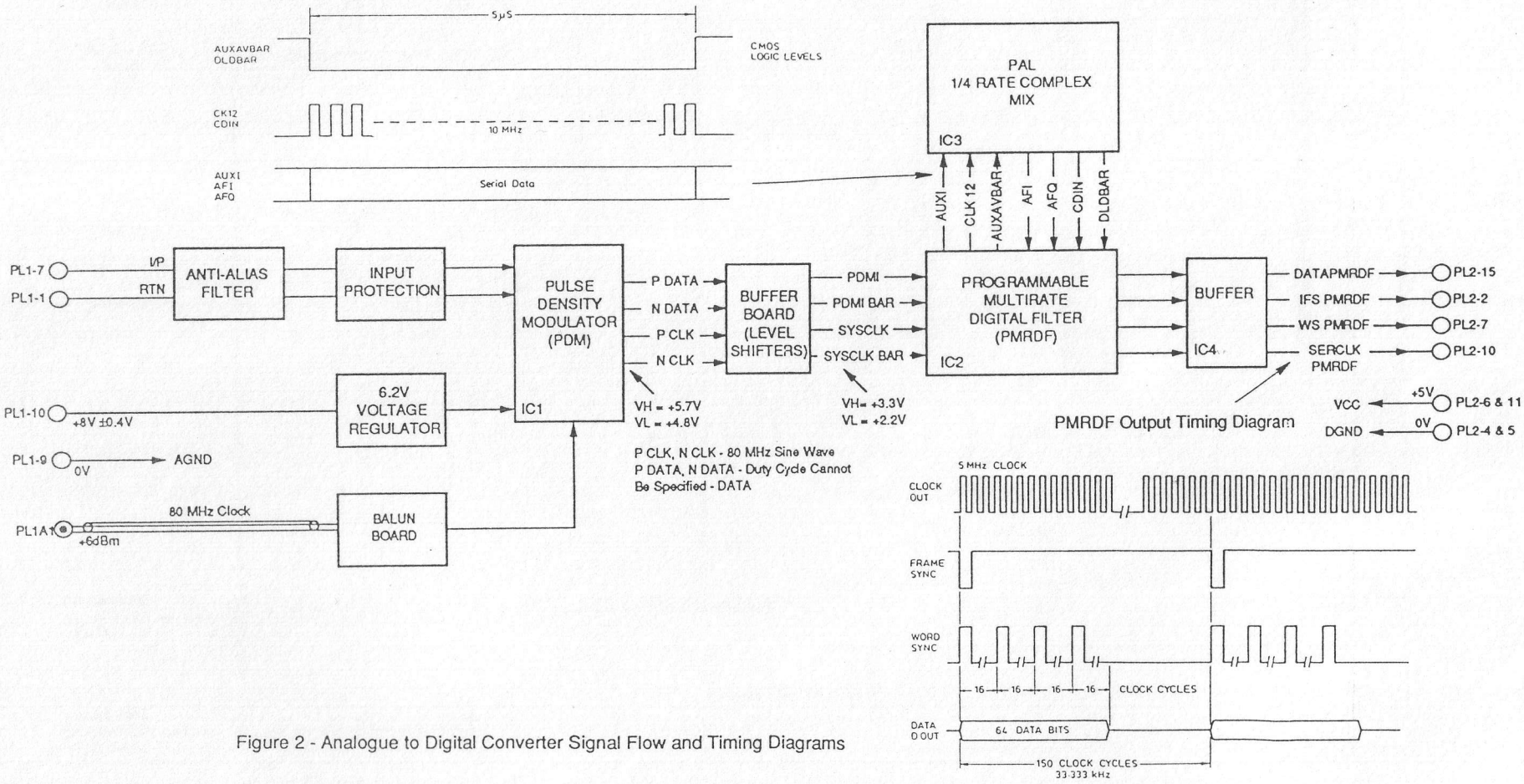


Figure 2 - Analogue to Digital Converter Signal Flow and Timing Diagrams

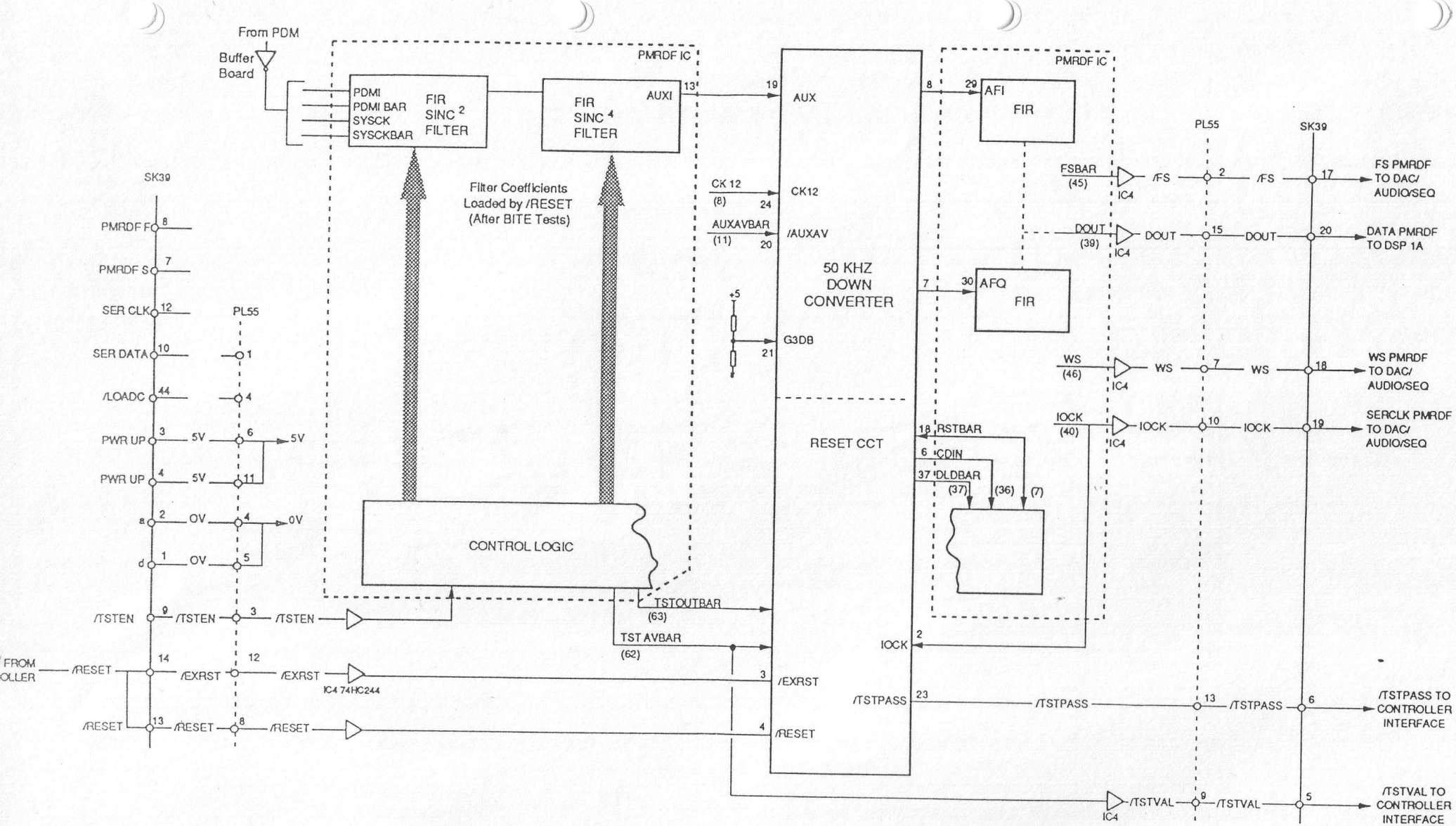


Figure 3 - Digital Filter (PMRDF) Block Diagram

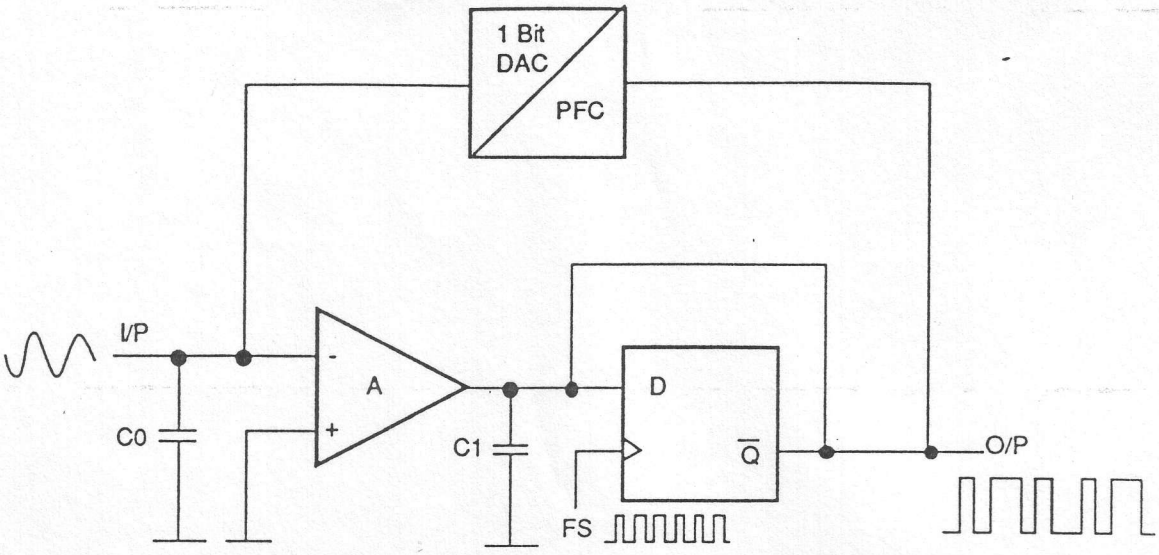


Figure 4 - Pulse Density Modulator Block Diagram

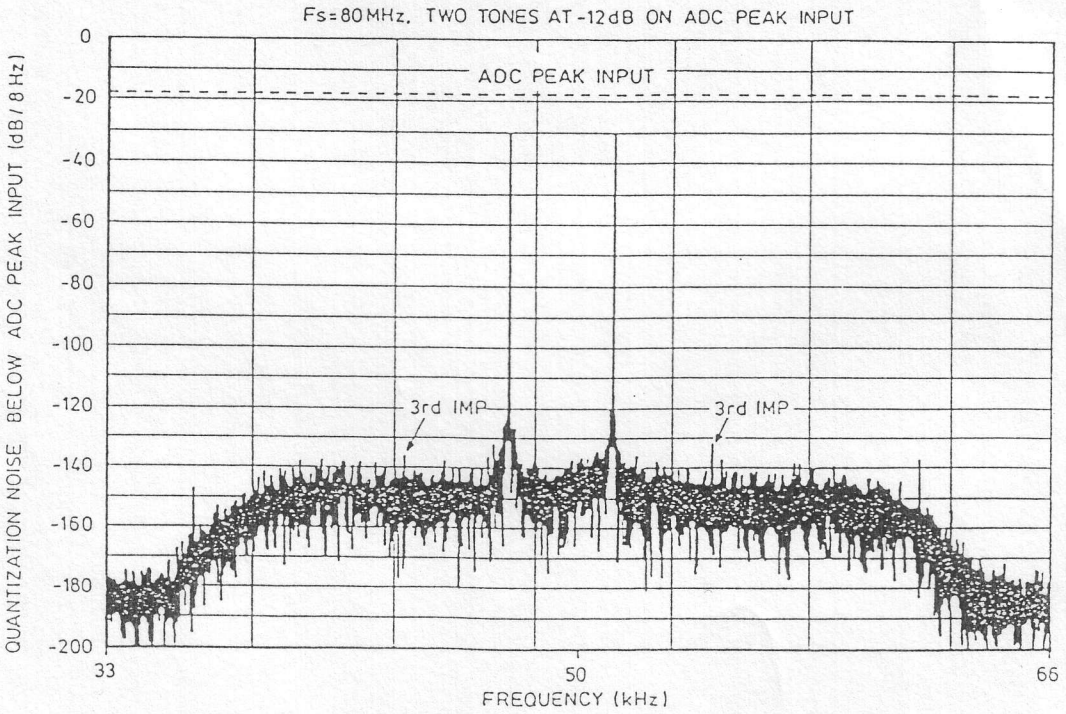


Figure 5 - Passband Spectrum of Baseband ADC Module

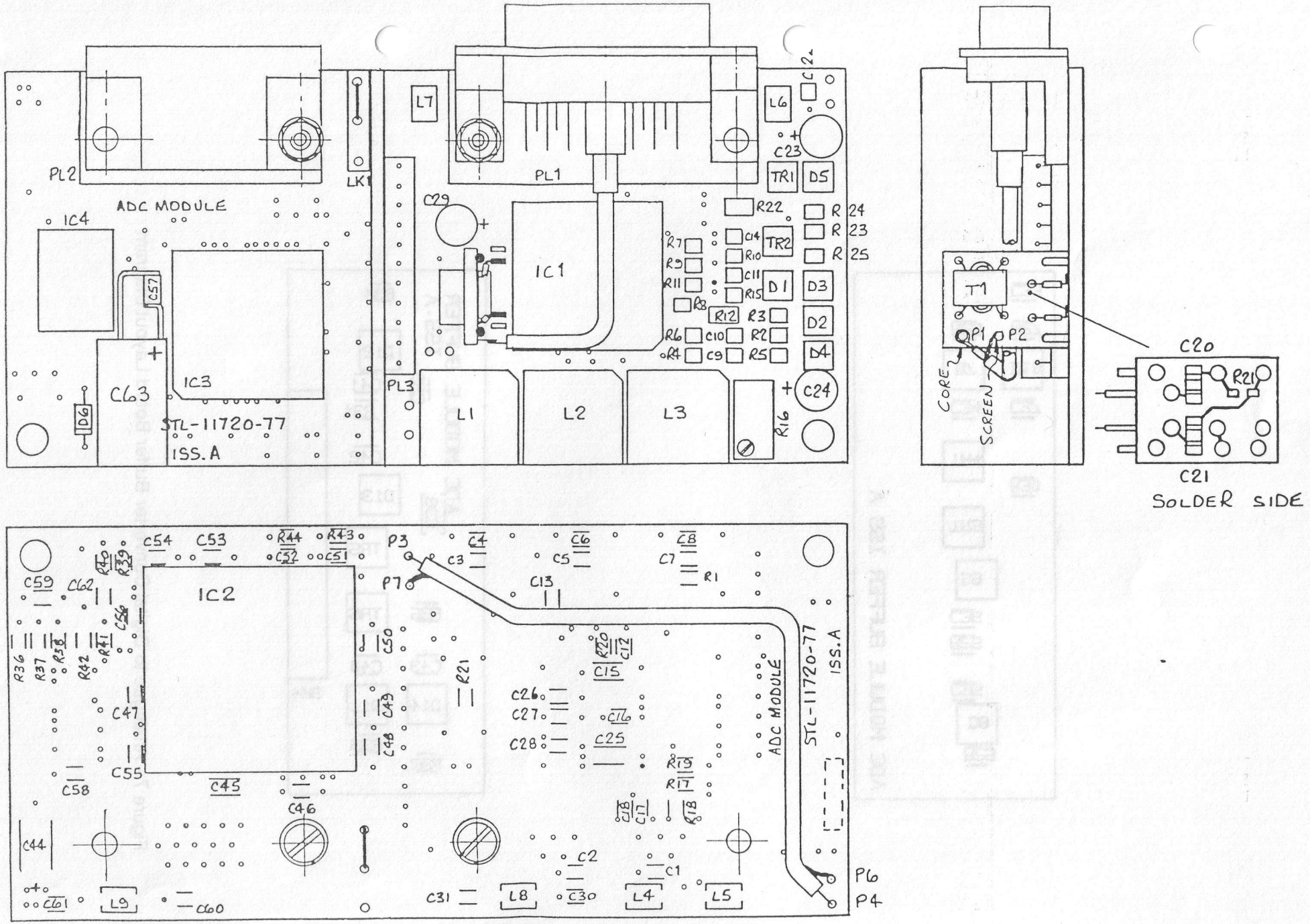
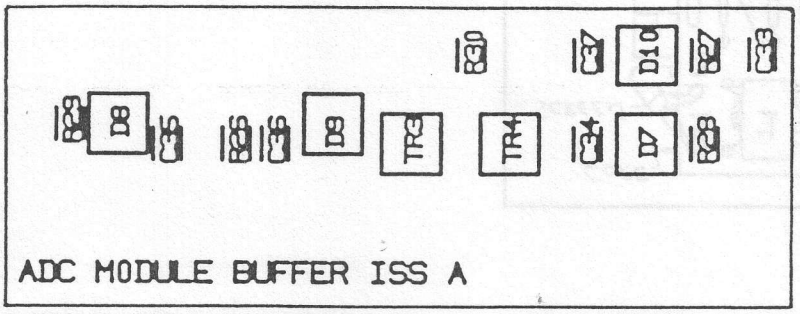


Figure 6 - Analogue to Digital Converter Layout Diagram



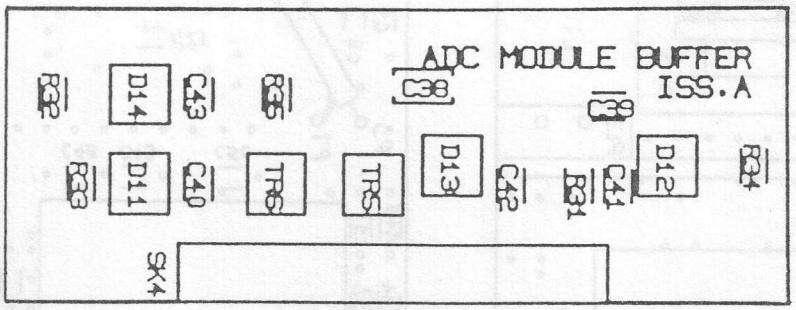


Figure 7 - Analogue to Digital Converter Buffer Board Layout Diagram

Circuit Reference	Description	Value
C1 & C2	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C3	Capacitor, fixed, ceramic chip, 5%, 100V	560p
C4	Capacitor, fixed, ceramic chip, 5%, 50V	2n2
C5	Capacitor, fixed, ceramic chip, 5% 50V	330p
C6	Capacitor, fixed, ceramic chip, 5%, 50V	2n2
C7	Capacitor, fixed, ceramic chip, 5%, 100V	820p
C8	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C9	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C10 & C11	Capacitor, fixed, ceramic chip, 5%, 100V	5p6
C12	Capacitor, fixed, ceramic chip, 5%, 100V	120p
C13	Capacitor, fixed, ceramic chip, 5%, 100V	150p
C14	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C15	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C16 & C17	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C18	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C20 & C21	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C22	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C23 & C24	Capacitor, fixed, aluminium electrolytic, 20%, 25V	100µ
C25	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C26 to C28	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C29	Capacitor, fixed, aluminium electrolytic, 20%, 25V	100µ
C44	Capacitor, fixed, solid tant chip, 20%, 16V	10µ
C45	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C46 to C48	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C49	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C50	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C51	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C52	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C53	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C54	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C55 & C56	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C57	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C58 & C59	Capacitor, fixed, ceramic chip, 10%, 50V	22n

ADC Board Assembly Items List - Sheet 1 of 3

Circuit Reference	Description	Value
C62	Capacitor, fixed, ceramic chip, 5%, 100V	270p
C63	Capacitor, fixed, aluminium electrolytic, 20%, 25V	220µ
L1 to L3	Choke, wound	
L4 & L5	Choke, fixed chip, 10%	10µ
L6	Choke, fixed, chip, 10%	22µ
L7 to L9	Choke, fixed, chip, 20 %	2µ2
IC1	PDM	
IC2	PMRDF	
IC4	Oct Buffer Line Driver 3 State, PC74HC244T	
R1	Resistor, fixed, chip, 1%, 0.1W	2k2
R2 to R9	Resistor, fixed, chip, 1%, 0.1W	510R
R10 & R11	Resistor, fixed, chip, 1%, 0.1W	390R
R12	Resistor, fixed, chip, 5%, 0.25W	3R3
R15	Resistor, fixed, chip, 1%, 0.1W	12k
R16	Resistor, variable, 10%, 0.5W	2k
R17	Resistor, fixed, chip, 1%, 0.1W	4k7
R18	Resistor, fixed, chip, 1%, 0.1W	1k8
R20	Resistor, fixed, chip, 1%, 0.1W	3k3
R21	Resistor, fixed, chip, 1%, 0.1W	470R
R22	Resistor, fixed, chip, 5%, 0.25W	56R
R23 & R25	Resistor, fixed, chip, 1%, 0.1W	300R
R36 to R38	Resistor, fixed, chip, 1%, 0.1W	100k
R39	Resistor, fixed, chip, 1%, 0.1W	560R
R40	Resistor, fixed, chip, 1%, 0.1W	100k
R41	Resistor, fixed, chip, 1%, 0.1W	82k
R42	Resistor, fixed, chip, 1%, 0.1W	6k8
R43	Resistor, fixed, chip	0R
D1 to D4	Diode, double, DAV99	
D5	Diode, sener, BZX84C5V6	
D6	Diode, schottky, BAT85	
TR 1 & TR2	Transistor, NPN BCX20	

ADC Assembly Board Items List - Sheet 2 of 3

Circuit Reference	Description	Value
C33 to C37	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C38	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C39 to C43	Capacitor, fixed, ceramic chip, 10%, 100V	1n
R26 & R27	Resistor, fixed, chip, 1%, 0.1W	100R
R28 & R29	Resistor, fixed, chip, 1%, 0.1W	470R
R30	Resistor, fixed, chip, 1%, 0.1W	120R
R31 & R32	Resistor, fixed, chip, 1%, 0.1W	100R
R33 & R34	Resistor, fixed, chip, 1%, 0.1W	470R
R35	Resistor, fixed, chip, 1%, 0.1W	120R
D7 & D8	Diode, zener, BZX84C3V6	
D9 & D10	Diode, Double BAV99	
D11 & D12	Diode, zener, BZX84C3V6	
D13 & D14	Diode, Double BAV99	
TR3 to TR6	Transistor, NPN, BSV52	

ADC Buffer Board Items List - Sheet 3 of 3

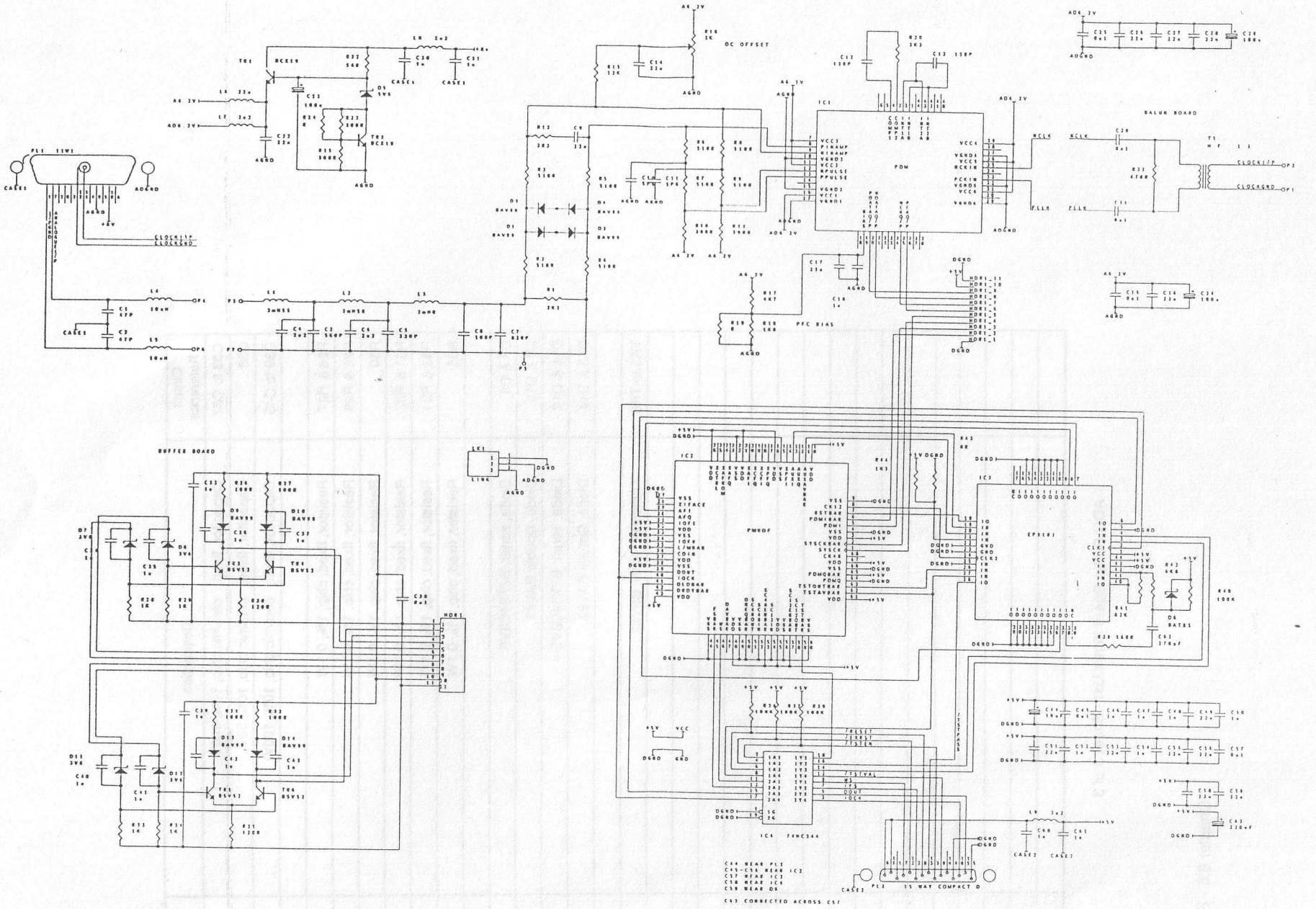


Figure 8 - Analogue to Digital Converter Circuit Diagram

Chapter 6.7

INTERFACE MODULE

1 MODULE DESCRIPTION

The Interface Module comprises two PCBs, Interface Board 1 Assembly 52UPB504068 and Interface Board 2 Assembly 52UPB504069, housed in a screened enclosure. Connections to the module are via a 44 way 'D' Type connector SK3 and a 26 way 'D' Type connector SK4. The module plugs directly into PL40 of the Digital Backplane and to the adjacent 40 way connector which links to the RF Backplane.

Module description is given with reference to the following drawings/illustrations and items list:

- Figure 1 Interface Board 1 Component Layout
- Figure 2 Interface Board 2 Component Layout
- Items List Interface Board 1, Sheet 1 of 1
- Items List Interface Board 2, Sheet 1 of 1
- Figure 3 Interface Module Circuit Diagram, Sheet 1 of 2
- Figure 4 Interface Module Circuit Diagram, Sheet 2 of 2

The Interface Module is used to protect the low signal level circuits of the Analogue Sub-Section from interference caused by the high speed logic signals used in the Digital Sub-Section. All of the logic signals between the two sub-sections are filtered on their way through the Interface Module. The Serial Buses pass through the module on their way from the Controller Interface Board to the Analogue modules. The BITE signals pass through in the opposite direction. The filtering results in the rise time of the logic signals being slowed. These slower rise times minimise electromagnetic interference.

The Interface Module is powered from the Analogue Power Supply only. There is no connection to 0 volts on the Digital Backplane, the radio's 0 Volt lines are only connected together on the Rectifier and Smoothing Board. To allow for DC offsets between the Analogue and Digital 0 volt lines all of the digital signals from the Digital Backplane are fed through comparators with a threshold of approximately 1.5 volts.

2 ALIGNMENT AND DIAGNOSTIC NOTES

There are no adjustments to be performed on the Interface Module.

Fault diagnosis is simply a case of signal tracing. The only thing to note is that the serial communication lines between the Controller Interface and the Analogue Sub-Section are only active when a message needs to be sent to a module (e.g. at a change in front panel settings). Therefore the operator will need to change the front panel settings in order to stimulate these signals (SERCLK, SERDATA and the LOAD signals).

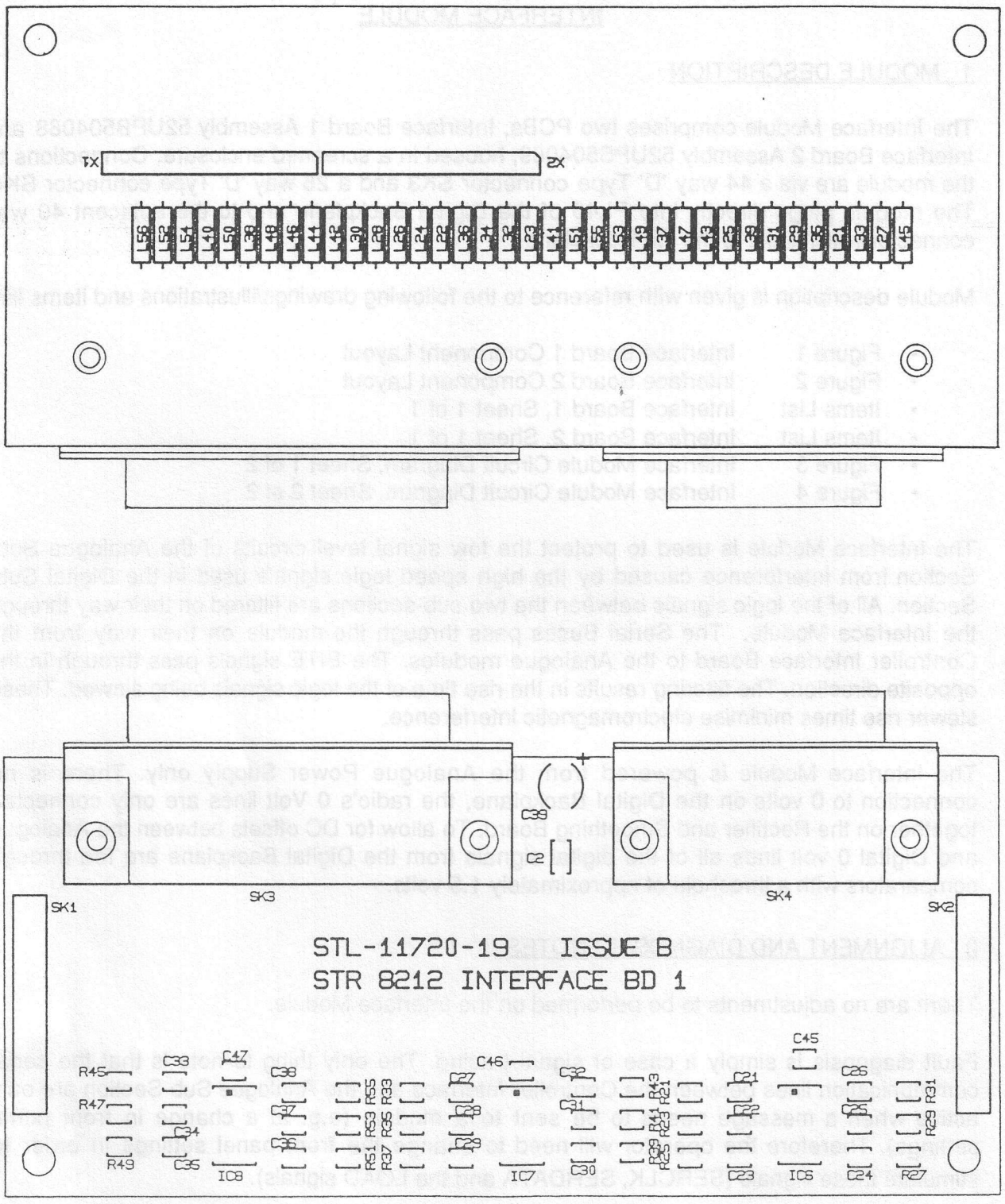


Figure 1 - Interface Board 1 Component Layout

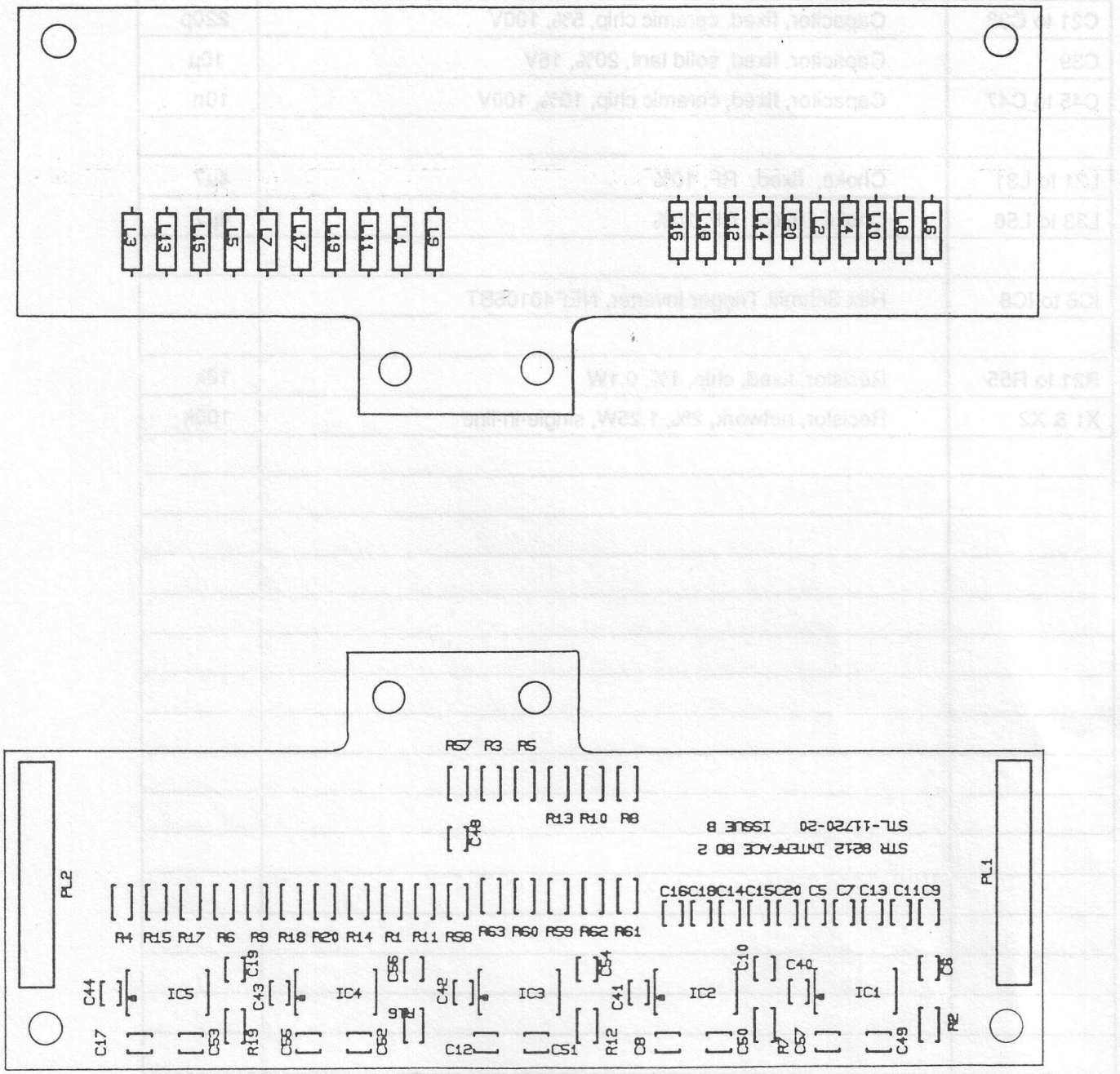


Figure 2 - Interface Board 2 Component Layout

Circuit Reference	Description	Value
C2	Capacitor, fixed, ceramic chip, 10%, 100V	100n
C21 to C38	Capacitor, fixed, ceramic chip, 5%, 100V	220p
C39	Capacitor, fixed, solid tant, 20%, 16V	10µ
C45 to C47	Capacitor, fixed, ceramic chip, 10%, 100V	10n
L21 to L31	Choke, fixed, RF, 10%	4µ7
L33 to L56	Choke, fixed, RF, 10%	4µ7
IC6 to IC8	Hex Schmitt Trigger Inverter, NEF40106BT	
R21 to R55	Resistor, fixed, chip, 1%, 0.1W	10k
X1 & X2	Resistor, network, 2%, 1.25W, single-in-line	100k

Interface Board 1, Items List - Sheet 1 of 1

Circuit Reference	Description	Value
C5	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C6	Capacitor, fixed, ceramic chip, 0.5p, 100V	4p7
C7	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C8	Capacitor, fixed, ceramic chip, 0.5p, 100V	4p7
C9	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C10	Capacitor, fixed, ceramic chip, 0.5p, 100V	4p7
C11	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C12	Capacitor, fixed, ceramic chip, 0.5p, 100V	4p7
C13	Capacitor, fixed, ceramic chip, 5%, 100V	22p
C14 to C16	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C17	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C18	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C19	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C20	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C40 to C44	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C48 to C53	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C54 to C56	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C57	Capacitor, fixed, ceramic chip, 0.5p, 100V	47p
L1 to L20	Choke, fixed, RF, 10%	4µ7
R1 & R2	Resistor, fixed, chip, 5%, 0.25W	10k
R3	Resistor, fixed, chip, 5%, 0.25W	750R
R4	Resistor, fixed, chip, 5%, 0.25W	10k
R5	Resistor, fixed, chip, 5%, 0.25W	750R
R6 & R7	Resistor, fixed, chip, 5%, 0.25W	10k
R8	Resistor, fixed, chip, 5%, 0.25W	750R
R9	Resistor, fixed, chip, 5%, 0.25W	10k
R10	Resistor, fixed, chip, 5%, 0.25W	750R
R11 & R12	Resistor, fixed, chip, 5%, 0.25W	10k
R13	Resistor, fixed, chip, 5%, 0.25W	750R
R14 to R20	Resistor, fixed, chip, 5%, 0.25W	10k
R57	Resistor, fixed, chip, 5%, 0.25W	1k5
R58	Resistor, fixed, chip, 5%, 0.25W	620R
R59 to R63	Resistor, fixed, chip, 5%, 0.25W	5k1

Interface Board 2, Items List - Sheet 1 of 1

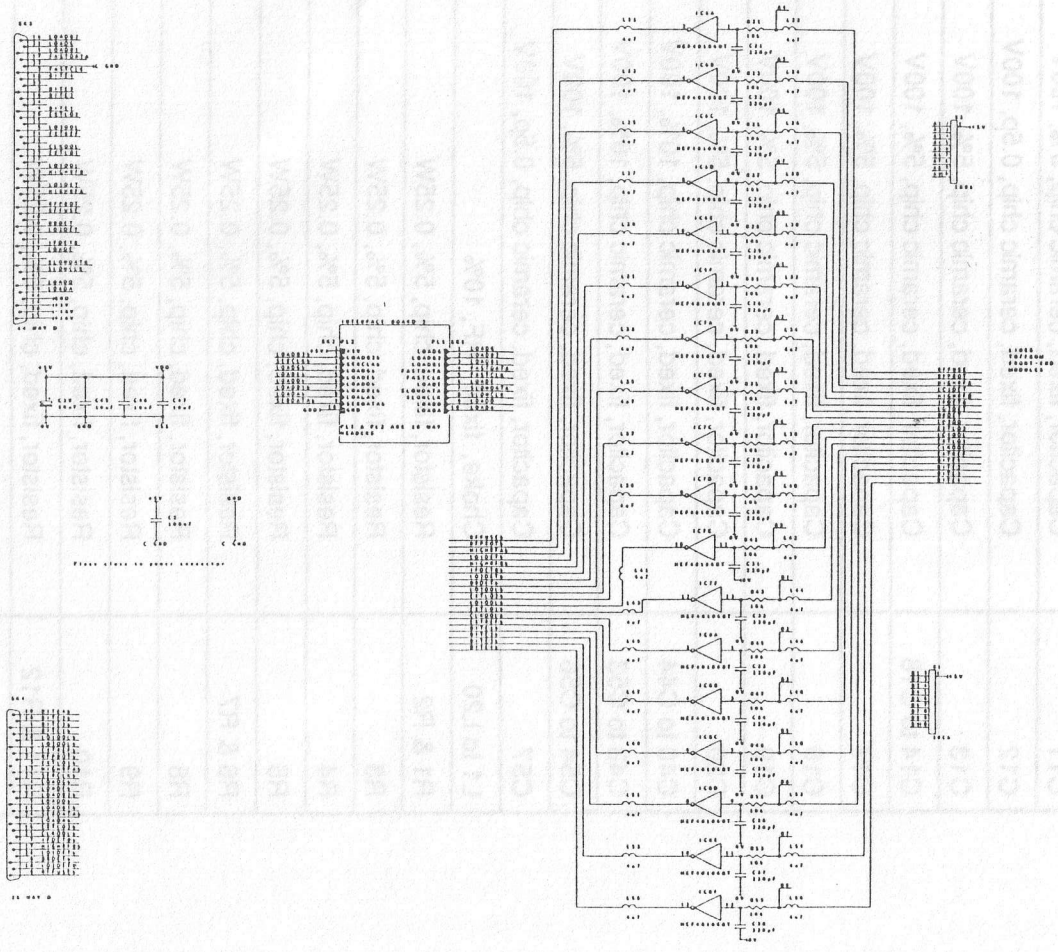


Figure 3 - Interface Module Circuit Diagram, Sheet 1 of 2

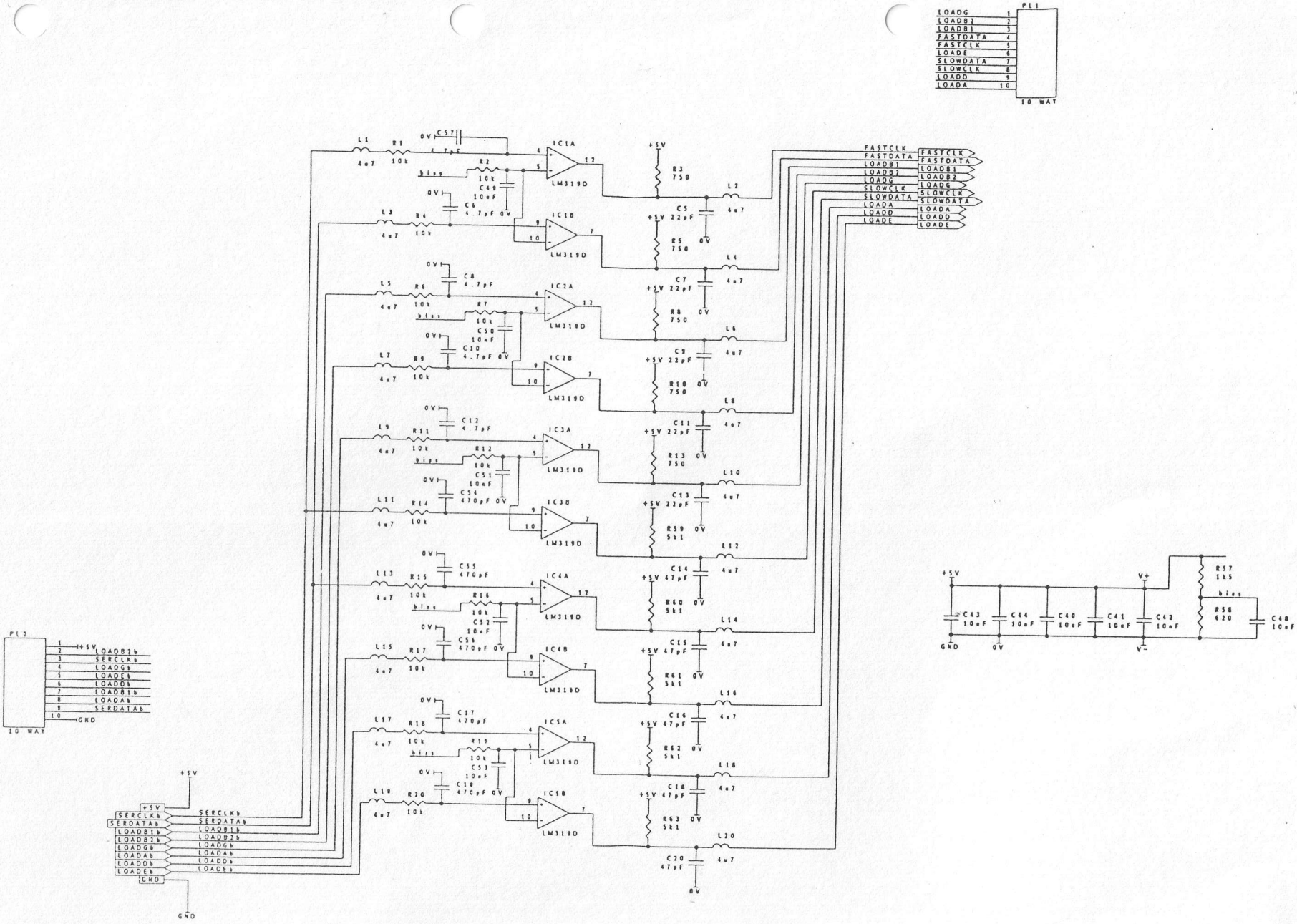


Figure 4 - Interface Module Circuit Diagram, Sheet 2 of 2

CHAPTER 6.8

CONTROLLER BOARD ASSEMBLY

1 INTRODUCTION

The Controller Board Assembly comprises a single PCB which plugs directly into the Digital Backplane via a single 96 way connector SKT 42.

The board is of multi-layer construction and has components fitted to both sides. The processor reset push button, SW1, is located near the upper edge of the board towards the rear.

This module description is given with reference to the following drawings, illustrations and items lists :-

- Figure 1 Controller Board Assembly - Simplified Block Diagram
- Figure 2 Controller Board Assembly - Component Layout
- Table 1 STR8212 Controller Address Map
- Table 2 Processor Interrupt Sources
- Items List Controller Board, Sheets 1 to 2 inc.
- Figure 3 Controller Board Assembly - Circuit Diagram

2 MODULE DESCRIPTION

The Controller board provides the overall control of the STR8212 receiver. It interfaces with the other modules of the radio via the Controller Interface board and to external services via an IEEE 488 Interface board. The Controller board contains a Motorola 68000 microprocessor which provides sufficient processing power for real time operations such as rapid frequency changing, IF AGC control and response to IEEE 488 control. The board also houses the associated EPROM, RAM and an EEPROM for non-volatile storage of preset channel information. A Multi Function Peripheral (MFP) chip provides three processor interrupt inputs and provides a RS232 interface for the radio.

The board houses the following programmed devices :-

- IC16 Programmable Logic Device PAL#1
- IC17 Programmable Logic Device PAL#2
- IC18 Programmable Logic Device PAL#3
- IC6 Program EPROM LOW
- IC6 Program EPROM HIGH

Note: *IC16, 17 and 18 are used for address decoding.*

The 68000 microprocessor communicates with its own memory, the MFP and external boards (Controller Interface and IEEE 488 Interface) via a standard 68000 bus. Address decoding is provided for on board peripherals and address select lines are passed to the Controller Interface where chip select lines for the other Digital Backplane boards are derived. Table 1 shows the processor address map and address decoder truth table. The processor address space occupied by the radio application, address #000000 to #02C1FF, takes up 180 kwords of the 16 Mwords in the 68000's address space.

The processor clock generator normally provides an 8 MHz clock for the 68000. The EPROM and RAM are accessed at 8 MHz. When EEPROM, the MFP or any other peripheral read or write operation is in process the 68000 clock is slowed to 4 MHz. PAL#2 (IC17) in the address decoder produces a signal, '/SLOW', whenever the processor addresses EEPROM, the MFP or a peripheral, the clock generator only allows changes in clock speed whilst the 4 MHz clock signal is high. The clock generator returns a feedback signal, '/SLOWED', to PAL#2. The EEPROM, MFP and peripheral address select signals can only become valid once '/SLOWED' is true. The clock generator provides clock outputs of 8, 4, 2 and 1 MHz for use by other boards.

The 68000's read and write cycles are normally 4 processor clock periods long. '/DTACK' can be used to control the read and write cycle lengths, '/DTACK' must be asserted for a read or write cycle to end. '/DTACK' is asserted by PAL#1 (IC16) for the EPROM, RAM and EEPROM addresses. '/DTACK' is also asserted by PAL#1 when 'VALID1' is true. The Controller Interface board asserts 'VALID1' for all assigned peripheral addresses except those for the TMS9914 (IEEE 488 Interface board) and Configuration Switches. These last two sets of addresses have '/DTACK' asserted by PAL#3 (IC18). See the truth table of Table 1.

The Encoder, IC19, provides encoding for interrupt request lines. The MFP provides expansion of priority level 3. The current interrupt mask determines whether the processor responds to an interrupt request. All interrupt requests (except 7) are maskable. A separate interrupt mask register in the MFP determines which devices cause an interrupt level 3 request. The devices originating the interrupts are listed in Table 2.

MFP Timer A is used to form a 10 second period watchdog timer. If the processor software's main routine fails to reset this timer within its 10 second period output, 'TAO' from the MFP triggers monostable IC13A which causes the power monitor chip, IC14, to generate a processor reset. This processor reset will restart the software processes both in the 68000 and the DSP modules and should remove the cause of the hang-up. The power monitor chip, IC14, generates a 200 mS (typical) '/RESET' pulse as the +5v supply rises through 4.55v (typical), if the watchdog fires or when SW1 is released ('/RESET' will stay active as long as SW1 is depressed). An instruction in the processor software can cause a pulse of 15.4 uS (typical) duration to occur on the '/RESET' line. The '/RESET' line is fed off to the rest of the sub assemblies on the Digital Backplane.

Table 1 - STR8212 Controller Address Map

Note: *Read labels of Decoder Output Signals vertically in columns: e.g. 1st label = /SLOW, 2nd = LOWADDR etc.*

Address From	To	No of Bits	Read/ Write	Usage	State of Decoder Output Signals: /SLOWDR, LOWADDR, LOWAPAGE, VPA/Y3, Y26, SWE, CSE(NMF), CSE(9P14), CSE(RAMO), CSE(RMP), CADLT(RCIM), IACK(IC), IACK(11&8)
000000	01FFFE	16	R	Program EPROM (64k x 8)	1 0 X 1 1 1 1 1 1 0 1 1 0 0
020000	023FFE	16	R/W	Data RAM (8k x 16)	1 1 X 1 1 1 1 1 1 1 0 1 0 0
024000	025FFE	16	R/W	Not used	1 1 X 1 0 1 1 1 1 1 1 1 0 Z
026000	027FFE	16	R/W	Not used	1 1 X X 0 1 1 1 1 1 1 1 0 Z
028001	02BFFF	8	R/W	Non-Vol. EEPROM (8k x 8)	0 1 X 0 1 1 1 1 1 1 1 0 0 0
02C001	02C02F	8	R/W	MFP Registers	0 1 1 0 1 0 1 0 1 1 1 1 0 Z
02C041	02C04F	8	W	TMS9914 Write Registers	0 1 1 0 1 0 1 1 0 1 1 1 0 0
02C040	02C04F	16	R	Config Switch and ADC I/Ps	0 1 1 0 1 0 0 1 1 1 1 1 0 0
02C051	02C05F	8	R	TMS9914 Read Registers	0 1 1 0 1 0 1 1 0 1 1 1 0 0
02C080	02C0FE	16	R/W	Not used	0 1 1 0 1 0 1 1 1 1 1 1 0 Z
02C101	02C10F	8	R/W	DSP1A Interface	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C111	02C11F	8	R/W	DSP1B Interface	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C121	02C12F	8	R/W	DSP2A Interface	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C131	02C13F	8	R/W	DSP2B Interface	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C141	02C14F	8	R/W	DSP3A Interface (Not used)	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C151	02C15F	8	R/W	DSP3B Interface (Not used)	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C161	02C16F	8	W	DAC/Sequencer Interface	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1C2		8	W	Serial Interface A	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1C4		16	W	Serial Interface B LS word	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1C6		16	W	Serial Interface B MS word	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1CA		16	W	Serial Interface C	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1CE		8	W	Serial Interface D	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1D2		8	W	Serial Interface E	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1D6		16	W	Serial Interface F	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1DA		16	W	Serial Interface G	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1E0		16	W	Output 1 register	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1E0		16	R	Input 1 register	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1E2		16	R	Input 2 register	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1E5		16	W	LCD driver register	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C1E7		8	R	Gain/Squelch ADC value	0 1 1 0 1 0 1 1 1 1 1 1 1 0
02C200	02DFFE	16	R/W	Not used	0 1 0 0 1 0 1 1 1 1 1 1 0 Z
02E000	02FFFE	16	R/W	Not used	0 1 0 0 1 1 1 1 1 1 1 1 0 Z
030000	FFFFFE	16	R/W	Not used	1 0 X 1 1 1 1 1 1 1 1 1 0 Z

Note: *Z = High Impedance State*

Table 2 - Processor Interrupt Sources

	Level	Usage
Highest	7	Not used
	6	Not used
	5	DSP Modules
	4	IEEE488 Interface (except BO & BI interrupts)
	3	MFP Interrupts
		15 IEEE488 BO and BI interrupts
		14 AGC Dump (rear panel input)
		13 Not used
		12 RS232 Receive Buffer Full
		11 RS232 Receive Error
		10 RS232 Transmit Buffer Empty
		9 Not used
		8 MFP Timer B interrupt
		7 Key Available (from Controller I/F)
		6 Not used
		5 Not used
		4 MFP Timer D interrupt
		3 Tuning Knob Count Pulse (from Controller I/F)
		2 Not used
		1 Not used
		0 Not used
	2	Not used
Lowest	1	Not used

3 ALIGNMENT AND DIAGNOSTIC NOTES

There are no alignment operations required on this assembly.

The Controller board has comprehensive BITE testing built into its software no further diagnostic testing should be necessary. Chapter 3 of this manual gives details of the BITE tests.

It should be noted that since the 68000 data bus is taken directly off the board, a failure of the bus interface components on the Controller Interface board or the IEEE 488 Interface board will cause an apparent failure of the Controller Board. This type of fault usually manifests itself by the Controller completely failing and hanging-up, the power-on BITE test will fail to complete (or maybe even start). The IEEE 488 Interface board may simply be removed from the radio to exclude it from suspicion. However, the Controller requires the Controller Interface board to communicate with the Keyboard and Display and a substitution test may be necessary in this case.

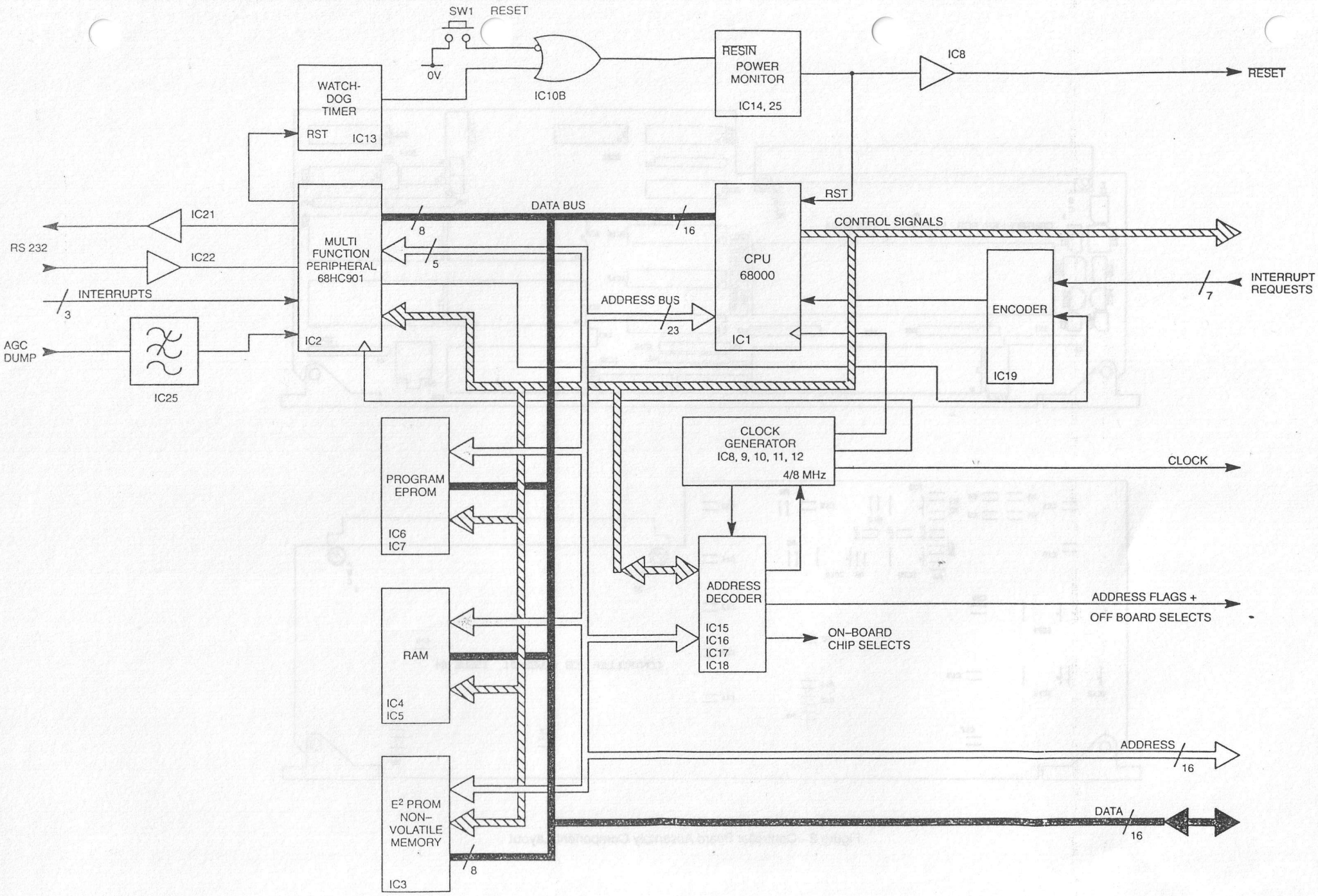


Figure 1 Controller Board Assembly Simplified Block Diagram

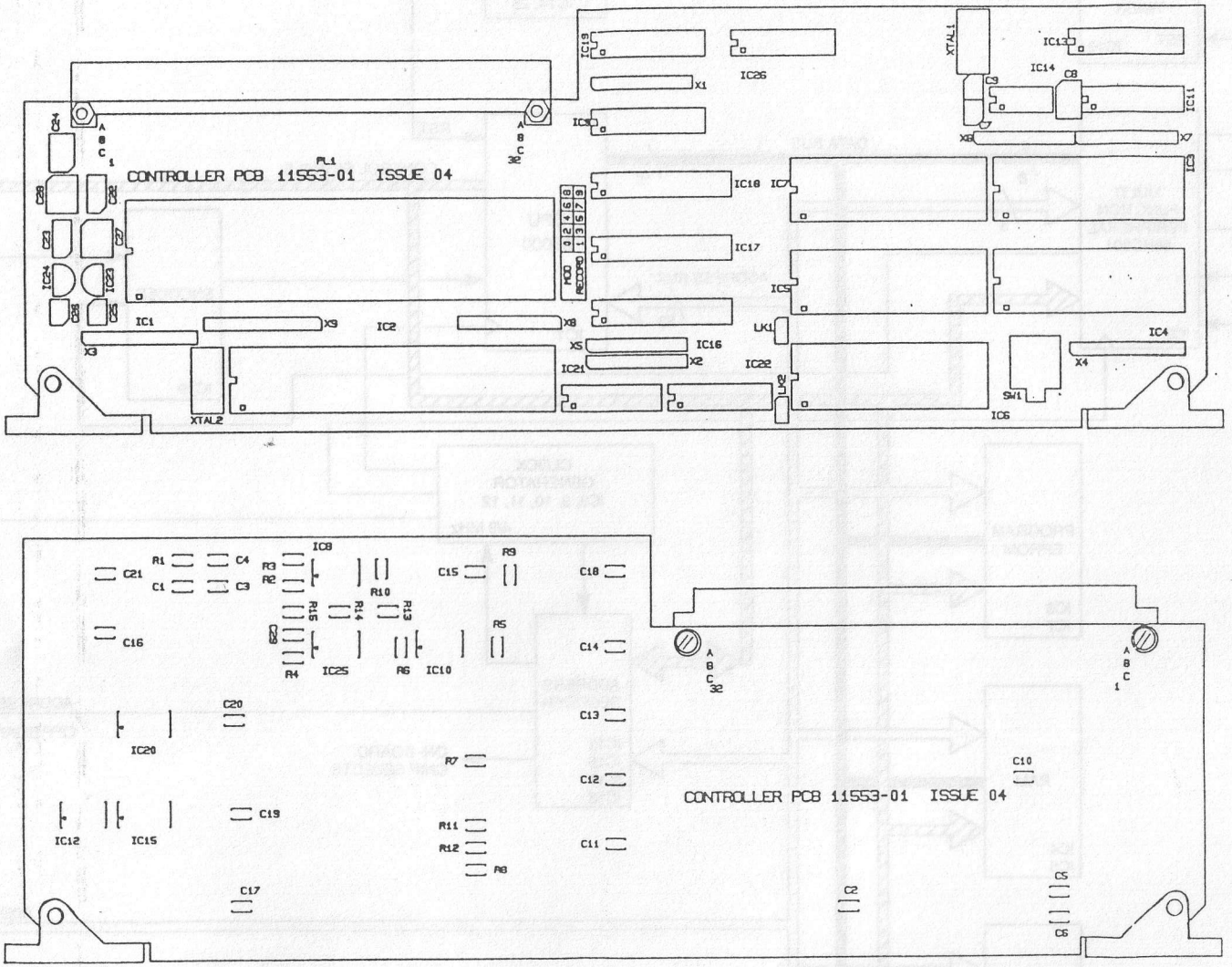


Figure 2 - Controller Board Assembly Component Layout

Circuit Reference	Description	Value
C1	Capacitor, fixed, ceramic chip, 5%, 100V	470p
C2	Capacitor, fixed, ceramic chip, 10%, 100V	22n
C3 to C6	Capacitor, fixed, ceramic chip, 5%, 100V	33p
C7	Capacitor, fixed, ceramic, radial, 10%, 50V	100n
C8	Capacitor, fixed, aluminium radial, 20% 16V	15µ
C9	Capacitor, fixed, ceramic, radial, 10%, 50V	100n
C10 to C21	Capacitor, fixed, ceramic chip, 10%, 100V	22n
C22 & C23	Capacitor, fixed, aluminium radial, 20% 25V	1µ
C24	Capacitor, fixed, aluminium radial, 20% 10V	22µ
C25 & C26	Capacitor, fixed, ceramic, radial, 10%, 50V	100n
C27 & C28	Capacitor, fixed, aluminium radial, 20% 16V	15µ
C29	Capacitor, fixed, ceramic chip, 5%, 100V	47p
IC1	16 Bit CPU CMOs, MC68HC000P8	
IC2	Multi-Function Peripheral, TS8HC901CP4B	
IC3	EEPROM, D28C64C-20	
IC4 & IC5	64K (8K x 8) CMOS Static RAM 100nS, HY6264LP-10	
IC6 & IC7	EPROM, TMS27C512-2JL	
IC8	Hex Inverter, MC74HC04AD	
IC9	4 Bit Counter Asynch, 74ACT16PC	
IC10	Triple, 3 Input Nand Gate, 74C11SC	
IC11	Dual D Type Flip-flop, CD74ACT74E	
IC12	1 Input Nand Gate, 74AC02SC	
IC13	Dual Retrig Mono Multi-Vibrator, MM74HC123AN	
IC14	Voltage Regulator, Positive, Fixed, TL7705ACP	
IC15	Dual 1 of 4 Decoder, 74AC139SC	
IC16 to IC18	Programmable Logic Device, PAL16L8B-2CN	
IC19	10 to 4 Priority Encoder, SN74HC138N	
IC20	1 of 8 Decoder, 74AC138SC	
IC21	Line Driver, CMOS Quad E1A RS232, DS14C88N	
IC22	Line Receiver CMOS, Quad EIA RS232, DS14C89AN	
IC23	Voltage Regulator, Positive, Fixed, MC78L12ACP	
IC24	Voltage Regulator, Negative, Fixed, MC79L12ACP	

Controller Board Items List - Sheet 1 of 2

Circuit Reference	Description	Value
IC25	Quad 2 Input Nand Trigger, MC74HC132AN	
IC26	Quad 2 Input Nand With Q/C, Open Drain, CD74HC03E	
R1	Resistor, fixed, chip, 5%, 0.25W	10k
R2	Resistor, fixed, chip, 5%, 0.25W	21M
R3	Resistor, fixed, chip	0R
R4	Resistor, fixed, chip, 5%, 0.25W	10k
R5 & R6	Resistor, fixed, chip, 5%, 0.25W	100k
R7 & R8	Resistor, fixed, chip, 5%, 0.25W	10k
R9	Resistor, fixed, chip, 1%, 0.25W	2k7
R10	Resistor, fixed, chip, 5%, 0.25W	10k
R11 to R13	Resistor, fixed, chip, 5%, 0.25W	100k
R14	Resistor, fixed, chip, 5%, 0.25W	1k
R15	Resistor, fixed, chip, 5%, 0.25W	330R
X1	Resistor, Network, 2%, 1W	10k
X2	Resistor, Network, 2%, 1W	100k
X3 & X4	Resistor, Network, 2%, 1.125W	10k
X5 to X8	Resistor, Network, 2%, 1W	100k
X9	Resistor, Network, 2%, 1.125W	10k

Controller Board Items List - Sheet 2 of 2

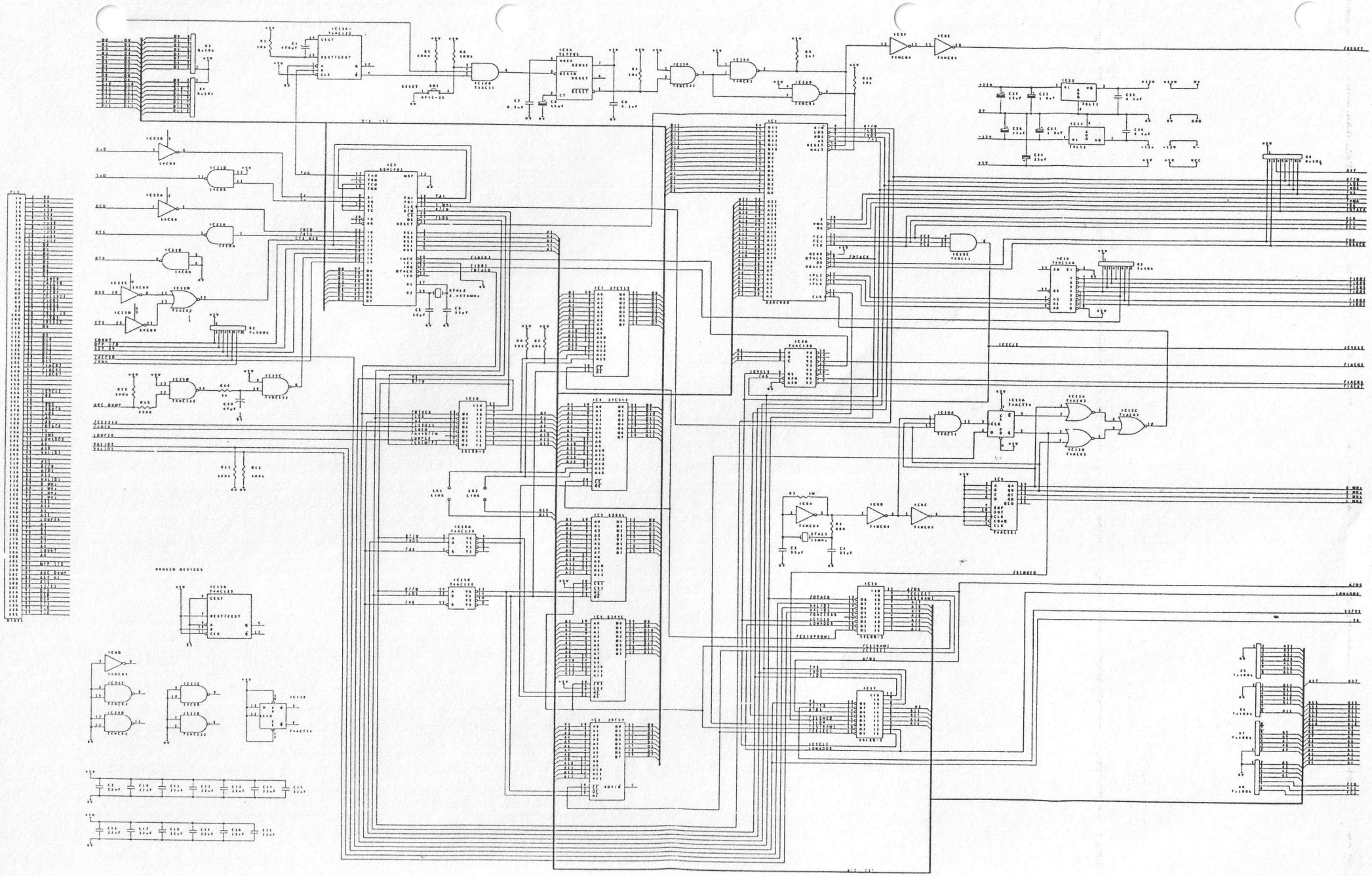


Figure 3 - Controller Board Assembly Circuit Diagram

Chapter 6.9

CONTROLLER INTERFACE BOARD

1 INTRODUCTION

The Controller Interface Board Assembly is a single PCB which plugs directly into the Digital Backplane via a single 182 way connector SKT 41.

The board is of multi-layer construction and has components fitted to both sides. The DIP switch, SW1, used for setting the RS232 baud rate and handshake, is located near the top edge of the board towards the front. See table 6.9.1 for a SW1 settings table.

Module description is given with reference to the following drawings, illustrations and items lists :-

- Figure 1 Controller Interface Board Simplified Block Diagram
- Figure 2 LCD Serial Data Timing Diagram
- Figure 3 Controller Interface Board Layout Diagram
- Items List Controller Interface Board, Sheets 1 and 2
- Figure 4 Controller Interface Board Circuit Diagram

2 MODULE DESCRIPTION

The Controller Interface board contains most of the interface logic between the Controller board and the rest of the modules in the STR8212 receiver. The interfaces comprise two serial output buses; one of which controls various modules and the other controls the LCD display; and also various parallel outputs and parallel inputs. All interfaces are memory mapped onto the Controller's data bus. See Table 6.8.1 for the interface memory addresses. [See Section 6.16 for the bit allocations of the serial interface words]. See Chapter 6.8 Table 1 for the interface memory addresses and Chapter 6.16 for the bit allocations of the serial interface words.

The basic building blocks of this module are:

- Address and Control Bus Decoding
- Buffered Data Bus
- Interface Signals
- Digital Input for BITE
- Keyboard Decoder
- Direction and Count Signals
- RS232 Configuration Switch
- ADC for Gain/Squelch
- Serial Interfaces
- Front Panel Display Driver Interface
- Carrier Operated Relay Output.

3 CIRCUIT DESCRIPTION

Circuit Description is given under the following headings:

- Address and Control Bus Decoding . . . . . Paragraph 3.1
- Buffered Data Bus . . . . . Paragraph 3.2
- Interface Signals . . . . . Paragraph 3.3
- Digital Input for BITE . . . . . Paragraph 3.4
- Keyboard Decoder . . . . . Paragraph 3.5
- Direction and Count Signals . . . . . Paragraph 3.6
- RS232 Configuration Switch . . . . . Paragraph 3.7
- ADC for Gain/Squelch . . . . . Paragraph 3.8
- Serial Interfaces . . . . . Paragraph 3.9
- Front Panel Display Driver Interface . . . . . Paragraph 3.10
- Carrier Operated Relay Output. . . . . Paragraph 3.11

3.1 Address and Control Bus Decoding

Address and control bus decoding for all interfaces is carried out on this board. The 'R/W' line from the Controller specifies the direction of a bus transfer, the Controller reads the data bus if 'R/W' = 1 during the bus cycle.

The '/LE0.../LE3' lines from IC11 are used to control the read or write bus access of the latches fitted to the board.

'/CS1A.../CS3B' (DSP processor chip selects), 'CS(SEQ)' (chip select for DAC/Sequencer and Digital Output board), 'HA0...HA2' (address lines), HR/W (read/write control) and HAS (address strobe) form the control signals for the buffered data bus to the DSP modules, DAC/Sequencer and Digital Output board.

The '/SE0.../SE7' lines from IC44 each initiate the corresponding serial transfer 'A...G'.

3.2 Buffered Data Bus

A buffered data bus (BD0 to BD15), is used on the board and passed on to the DSP boards, DAC/Sequencer and Digital Output board.

3.3 Interface Signals

Interface signals to the PMRDF in the ADC module are provided on this board. '/TSTEN', '/TSTVAL' and '/TSTPASS' are BITE initialisation and reporting signals. PMRDF FIRST, PMRDF SHIFT and Serial Interface 'C' are currently not used by the ADC.

3.4 Digital Input for BITE

20 bits of digital input for BITE and status signals are provided on this board. These bits are split between parallel input latches 1 & 2.

3.5 Keyboard Decoder

A keyboard decoder handling up to 44 keys is provided on the board. This utilises a MM74C923 keyboard scanner chip extended to cope with 11 columns ('KY1...11'). The 'KEY AVAILable' signal goes true whenever a key is pressed, this is passed to the Controller board where it forms one of the interrupt inputs to the MFP.

3.6 Direction and Count Signals

The board provides logic to translate quadrature pulses from the tuning knobs shaft encoder (A,B) into a direction signal (DIR) and a pulse output (COUNT). 'COUNT' is passed to the Controller board where it forms one of the interrupt inputs to the MFP.

3.7 RS232 Configuration Switch

An RS232 configuration switch is fitted on the board. The bus address for this switch is shared with the address switch on the IEEE 488 board. The following table shows the switch settings for the Baud rates available.

Function	SW1 Section			
	4	3	2	1
Data rate = 150 baud	any	on	on	on
Data rate = 300 baud	any	on	on	off
Data rate = 600 baud	any	on	off	on
Data rate = 1200 baud	any	on	off	off
Data rate = 2400 baud	any	off	on	on
Data rate = 4800 baud	any	off	on	off
Data rate = 9600 baud	any	off	off	on
Data rate = 19200 baud	any	off	off	off
Hardware handshake enabled	off	any	any	any
Hardware handshake disabled	on	any	any	any

The 'any' entry denotes a don't care condition, i.e. the switch section may be either on or off.

A switch section is 'on' when the end of the paddle carrying the switch marking is depressed. The switch 'on' condition is read as a logic 0 on the bus.

Table 6.9.1 - SW1 Settings Table (RS232 Configuration)

3.8 ADC for Gain/Squelch

An ADC is used to read the position of the Gain/Squelch potentiometer. This uses differential inputs to reduce common mode noise. The Gain/Squelch potentiometer is connected to 0 volts at the potentiometer terminals.

3.9 Serial Interfaces

Serial Interfaces are used to configure the sub-octave filters, RF module, IF module , Synthesizer 1 module, ADC module and the front panel LEDs. This interface comprises a serial output register, up to 32 bits long (selected by address), with '/LOAD' and 'SER CLK' outputs which become active depending on the address of the data written to the shift registers. The speed of the data transmission is controlled by the clock output this has two speeds; slow (7.8 kHz) or fast (500 kHz). The clock line does not run continuously. The three lines ('SER CLK', 'SER DATA' and '/LOAD') start synchronously triggered by a Controller write to the interface address. The transmission is terminated by a signal from the bit counter (IC 39 and IC49). Table 6.9.2 overleaf shows the clock speed and data word length for each of the serial interfaces. Chapter 6.16 gives a timing diagram and bit allocation for each of the serial interfaces.

Interface	Destination	Word Length (bits)	Clock Speed (kHz)
A	RF Module	8	7.8
B	Synthesizer 1 Module (Frequency control word)	32	500
C	ADC Module	16	500
D	IF Module	8	7.8
E	Sub-octave Filter Module	8	7.8
F	Keyboard (LEDs)	16	500
G	Synthesizer 1 Module (BITE control word)	16	500

Table 6.9.2 - Serial Interface Details

3.10 Front Panel Display Driver Interface

The interface to the Front Panel Display Drivers comprises serial data, control and clock lines. A higher speed clock, 250 kHz, is provided for the display drivers timing. The control lines come from the Parallel Output 1 latch. The data is sourced from the LCD Data shift register. A clock generator clocks the data out of the shift register and produces the 'LCD CLOCK' signal for the Front Panel Display Driver chips. Transfer of data into the shift register initialises this clock generator, however the transfer is not started until '/LCD BUSY' is a logic high. '/LCD BUSY' is taken low by the Front Panel Display Driver chips to signal that any one of them is not ready to receive data. '/LCD BUSY' is taken low at the end of a serial transfer and goes high again when the data has been processed. Signal 'LCD SHIFT' going low signals to the Controller (via the parallel input 1 latch) that a serial transfer to the Display Drivers is in progress. Refer to Figure 2 for a timing diagram. The Parallel Interface Bit Allocation is shown in Tables 6.9.3 to 6.9.6 inclusive.

3.11 Carrier Operated Relay Output

The rear panel Carrier Operated Relay (COR) output is controlled via the parallel output 1 latch. This output is driven by a relay and provides a low impedance path to 0 volts when activated by the Controller. The output line is protected by a PC-TRON subminiature 500 mA fuse, BUSSMAN BK/PCC/0.5A. This fuse is soldered directly into the board.

Bit	Usage
15	SHIFTING
14	LCDSHIFT
13	PSU 1 FAIL
12	PSU 2 FAIL
11	BITE 4
10	BITE 3
9	BITE 2
8	BITE 1
7	ADC INTerrupt
6	DIRection
5	RF PROTection
4	HIGH RF A
3	EXTernal REF
2	EXTernal LO1
1	LO2 OOL (Out of Lock)
0	LO1 OOL (Out of Lock)

Table 6.9.3 - Parallel Input 1 Bit Allocation

Bit	Usage
15	EXTernal LO2
14	CLK OOL (Out of Lock)
13	BB DETector
12	LO2 DET
11	IF DET
10	HIGH RF B
9	LO1 DET
8	RF FUSE
7	KEY AVAILable
6 - 0	Encoded Key Pressed data

Table 6.9.4 - Parallel Input 2 Bit Allocation

Bit	Usage
15 - 6	Not used
5	COR (Carrier Operated Relay)
4	TSTEN
3	LCD C/D
2	LCD CS3
1	LCD CS2
0	LCD CS1

Table 6.9.5 - Parallel Output 1 Bit Allocation

Bit	Usage
15	RS232 Handshake
14	RS232 baud rate 2
13	RS232 baud rate 1
12	RS232 baud rate 0
11	PMRDF FIRST
10	PMRDF SHIFT
9	TSTPASS
8	TSTVAL
7 - 0	Used by IEEE 488 board configuration switch

Table 6.9.6 - Parallel Interface Bit Allocation

4 ALIGNMENT AND DIAGNOSTIC NOTES

4.1 Board Set-Up

The jumper link should be in position linking LK1 pins 1 & 2 for an STR8212 radio.

OR

The jumper link should be in position linking LK1 pins 2 & 3 for an STR8213 radio.

SW1 should be set to the desired RS232 baud rate and handshake status.

There are no electrical alignment operations required on this assembly.

Diagnostic tests for the Controller Interface are a process of signal tracing. The various output data buses are only active when the state of a bit requires to be changed. The front panel settings will need to be changed to stimulate a bus transfer, refer to Chapter 6.16 for the serial bus bit allocations.

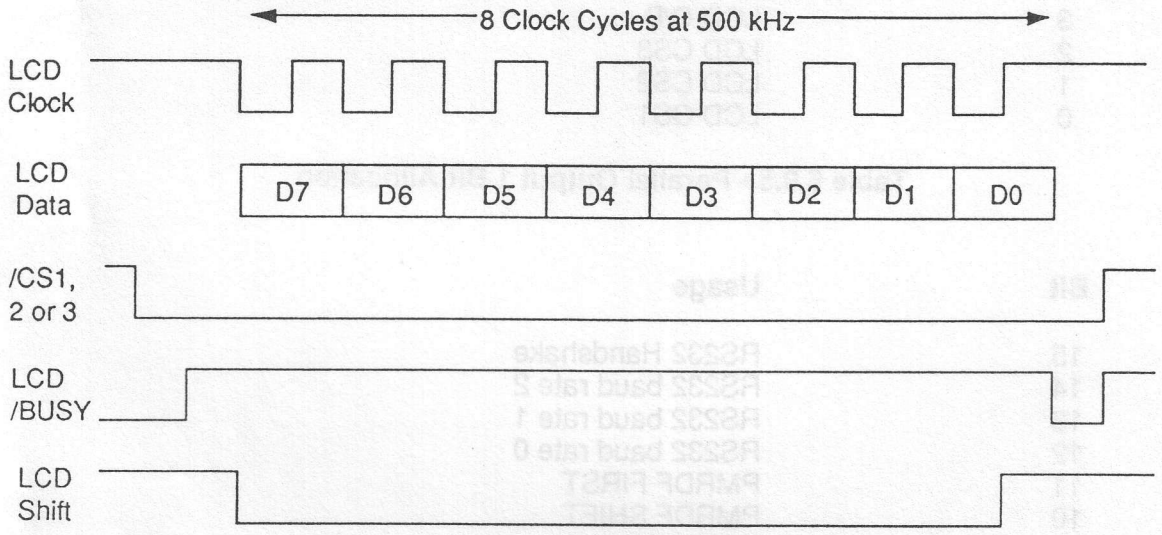


Figure 2 - LCD Serial Data Timing Diagram

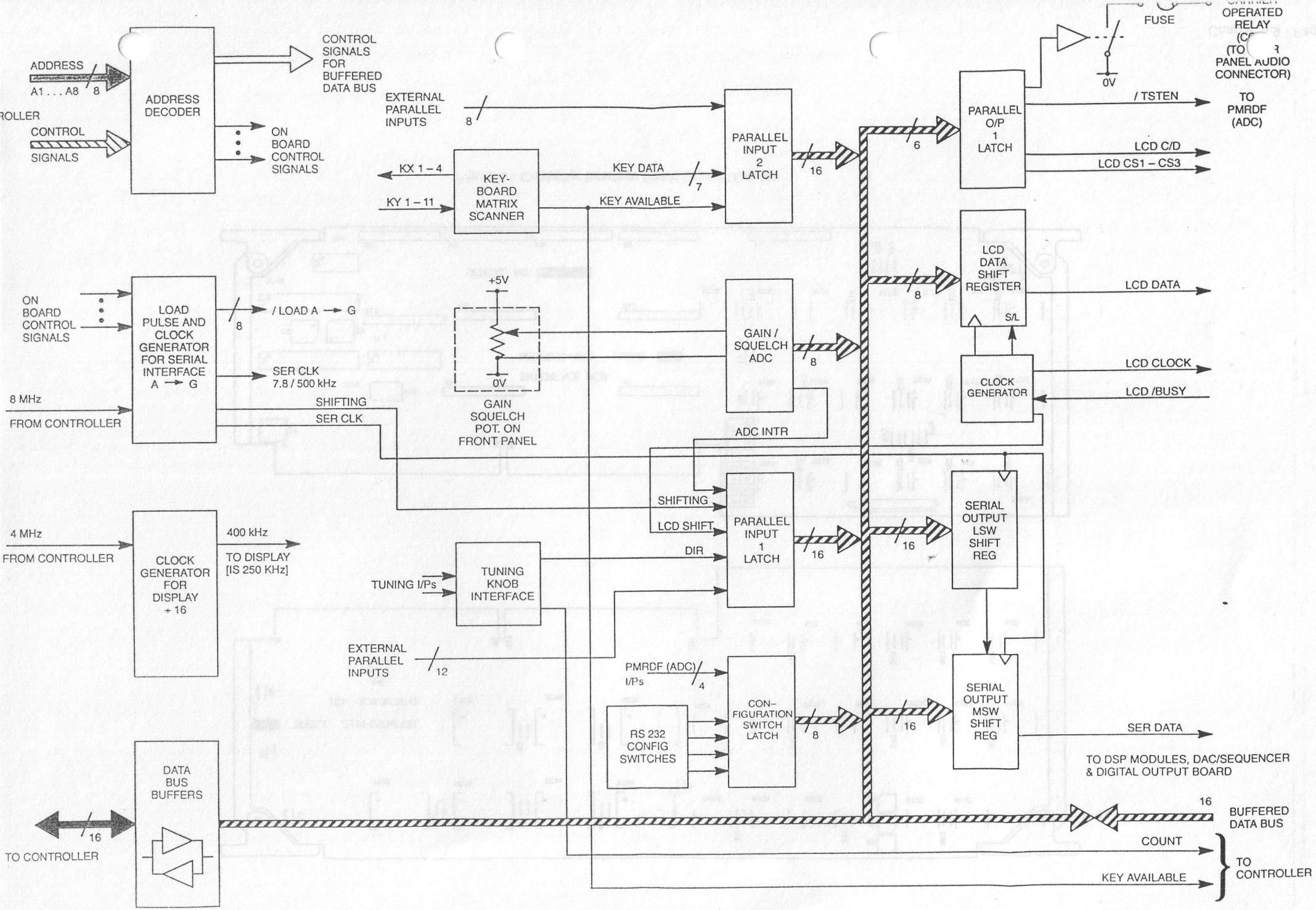


Figure 1 Controller Interface Simplified Block Diagram

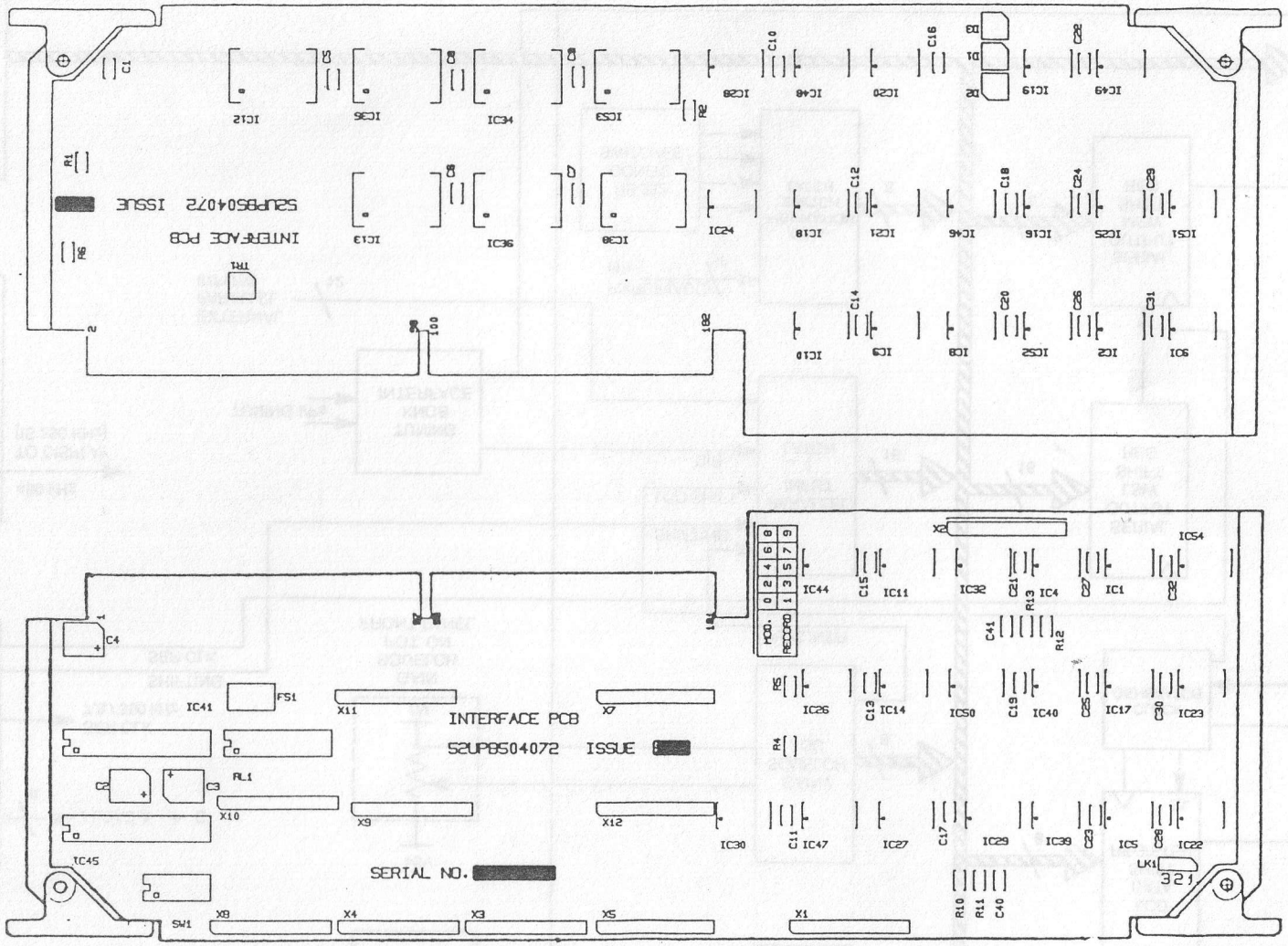


Figure 3 - Controller Interface Board Layout Diagram

Circuit Reference	Description	Value
C1	Capacitor, fixed, ceramic chip, 5%, 100V	150p
C2	Capacitor, fixed, solid tant, 20%, 35V	0.47µ
C3	Capacitor, fixed, solid tant, 20%, 10V	470n
C4	Capacitor, fixed, aluminium radial, 20%, 10V	4µ7
C5 to C32	Capacitor, fixed, ceramic chip, 10% 100V	22n
C40 & C41	Capacitor, fixed, ceramic chip, 10%, 100V	1n
IC1 & IC2	Quad, 2-Input Nand Gate, SN74HC00D	
IC4	Hex, Inverter, MC74HC04AD	
IC5	Triple, 3-Input Nand Gate, PC74HC10T	
IC6	Quad Input OR Gate, PC74HC32T	
IC8 & IC9	Quad Input OR Gate, PC74HC32T	
IC10 & IC11	1 of 8 Decoder, MC74HC138AD	
IC12 & IC13	Octal Bus Transceiver, PC74HC245T	
IC14	Quad 2-Input Nand Gate, SN74HC00D	
IC16	Quad 2-Input AND Gate SN74HC08D	
IC17	Hex, Inverter, MC74HC04AD	
IC18	Hed Buffer, MC14050BD	
IC19	Triple, 3-Input Nand Gate, PC74HC10T	
IC20 to IC26	Dual D-Type Flip-Flop, MC74HC74AD	
IC27 to IC29	8 Bit Shift Register, PC74HC165T	
IC30	Hex D-Type FLip-Flop, SN74HC174D	
IC32	Hex 3-State Buffer, CD74HC365M	
IC34 to IC36	Octal Latch 3-State O/P, CD74HCT373M	
IC38	Octal Latch 3-State O/P, CD74HCT373M	
IC39 & IC40	Dual 4-Bit Binary Ripple Counter, PC74HC393T	
IC41	20-Key Encoder, MM74C923N	
IC44	1 of 8 Decoder, MC74HC138AD	
IC45	Analog to Digital Converter, ADC0803LCN	
IC46	Dual D-Type Flip-Flop, MC74HC74AD	
IC47 & IC48	8 Bit Shift Register, PC74HC165T	
IC49	Dual 4-Bit Binary Ripple Counter, PC74HC393T	
IC50	Hex Inverter/Buffer, MC14049UBD	

Controller Interface Board Items List - Sheet 1 of 2

Circuit Reference	Description	Value
IC51 & IC52	Quad Input OR Gate, PC74HC32T	
IC53	Octal Latch 3-Stage O/P, CD74HCT373M	
IC54	4 Bit Synchronous Binary Counter, PC74HC163T	
R1	Resistor, fixed, chip, 5%, 0.25W	10k
R2	Resistor, fixed, chip, 5%, 0.25W	2k
R4 to R6	Resistor, fixed, chip, 5%, 0.25W	10k
R10 to R13	Resistor, fixed, chip, 5%, 0.25W	180R
X1 to X5	Resistor, Network, 2%, 1.125W	100k
X7	Resistor, Network, 2%, 1.125W	100k
X8 & X9	Resistor, Network, 2%, 1.125W	147k
X10 to X12	Resistor, Network, 2%, 1.125W	100k
D1 to D3	Diode, General Purpose, BAW56	
TR1	Transistor, NPN, BC849C	

Controller Interface Board Items List - Sheet 2 of 2

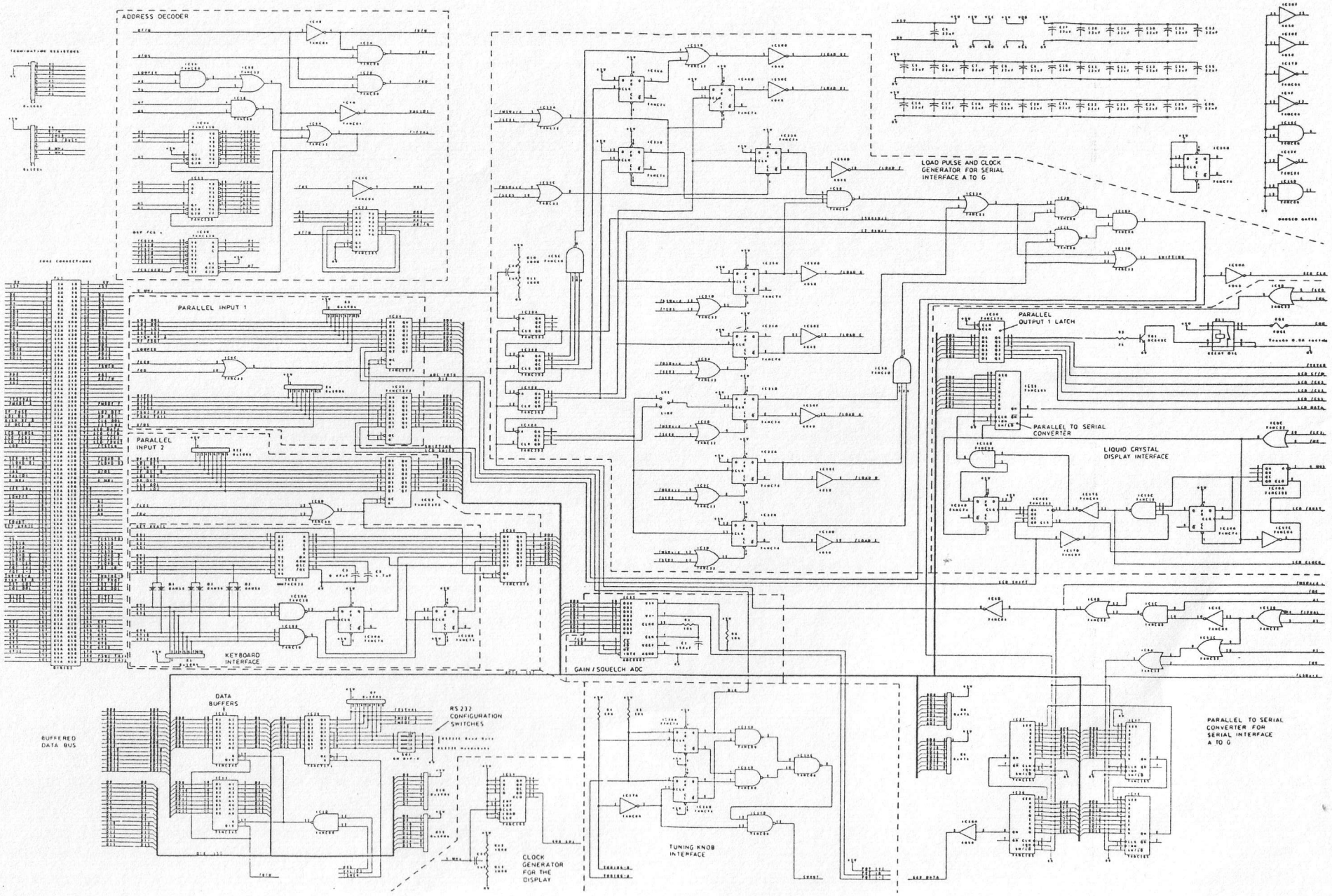


Figure 4 - Controller Interface Board Circuit Diagram

Chapter 6.10

DIGITAL SIGNAL PROCESSOR (DSP) BOARDS

1 INTRODUCTION

Each DSP56001 board assembly comprises a single PCB which plugs directly into the Digital Backplane of the radio via a single 64 way connector. Currently two DSP boards, DSP '1' and DSP '2', are fitted to sockets SK45 and SK46 respectively. A third position in the Digital Backplane, SK47, is kept as spare for a third DSP board. The module description is given with reference to the following drawings/illustrations and items list:

- Figure 1 DSP Boards Functional Diagram
- Figure 2 DSP Board Simplified Block Diagram
- Figure 3 DSP Board Timing Diagram
- Figure 4 DSP Board Component Layout
- Items List DSP Board, Sheets 1 to 2 inc.
- Figure 5 DSP Board Clock Buffer, Serial and Host Interface Circuit Diagram
- Figure 6 DSP Module 'A' Circuit Diagram
- Figure 7 DSP Module 'B' Circuit Diagram

2 MODULE DESCRIPTION

In the radio there is space for three hardware identical DSP boards of which two are currently in use. Referring to Figure 1, the DSP boards perform the following functions:

- Measures overall input power from ADC module (used by Controller Sub System for IF attenuator control).
- Droop and Ripple correction filtering.
- Channel filtering.
- Demodulation (AM, FM, SSB/CW)
- Audio AGC.
- Post demodulation filtering.

Referring to Figure 2, each DSP board comprises three functional blocks. The first block is the 'interface' and the other two are identical DSP blocks, DSP 'A' and DSP 'B', each containing a DSP56001 chip.

Module description is given under the following headings:

- Interface Block . . . . . Paragraph 2.1
- DSP56000 Circuit . . . . . Paragraph 2.2

2.1 Interface Block

The interface block comprises the following three sub-blocks:

- Master Clock Buffer
- Host Interface
- Serial Interface

2.1.1 Master Clock Buffer

The main 20 MHz clock for the DSP56001 chip is derived from the DAC/Sequencer board. The Master Clock Buffer converts the ECL clock inputs to TTL logic levels suitable for the DSP56001 chip.

2.1.2 Host Interface

This contains address and data line buffering from the Controller Interface board and some address control line decoding. The data passed from the controller to the DSP contains the following information:

> Bandwidth, Mode, BFO level, AGC time constants, AGC dump request, IF attenuation data, Manual gain level, Squelch level and BITE request.

The data bus is bi-directional as data is also returned to the controller. This returned data contains the following information:

> Request for change in IF attenuation, Squelch status & gain setting in manual mode and BITE messages.

The controller software has a hardware address assigned to each DSP. This address is decoded on the Controller Interface board into a chip select line for each DSP. Two of these chip select lines are part of the control lines in the host interface and are used to disable the data buffer should both DSPs be addressed at the same time. The three address lines HA(0, 1, and 2) are used to select internal registers in the DSP chip which contain status information and input/output buffers for the information data listed previously.

2.1.3 Serial Interface

This provides buffering for the Synchronous Serial Interface (SSI) which operates between the ADC, each DSP and the DAC and carries the digitised signal path. The SSI comprises a clock line, a data ready flag (DSP frame sync) and the data line, with both receive and transmit paths, timing and further details are given in paragraph 2.2.

2.2 DSP56000 Circuit

Each DSP56000 circuit comprises the following four sub-blocks:

- BITE
- RESET
- Program Memory
- DSP56001

2.2.1 BITE

This section includes both the watchdog circuit for use during normal operation and a loop around circuit to allow the SSI to be tested during off-line BITE.

2.2.2 RESET

This will trigger a reset in the DSP56001 if either the watchdog goes off or a reset pulse is received from the Controller board. It also contains the sample clock signal from the DAC/Sequencer board and inhibits this line if the DSP56001 is in reset.

2.2.3 Program Memory

This consists of three fast 2k x 8 EPROMs to provide the 24 bit data word to the DSP. There is also provision for a single slow EPROM which allows the download of the program from the EPROM into internal DSP memory on power-up, but this feature isn't utilised in the current radio configuration.

2.2.4 DSP56001

Each DSP provides further signal processing on the main signal path before passing the digitised signal onto the next stage. From the host interface section the DSP chip receives an eight bit data bus, a three bit address bus and four control lines. From the serial interface section the DSP chip receives the SSI information in the form of a 5 MHz serial clock, a frame sync pulse, a sample clock pulse and a data line. The timing for the DSP is shown in Figure 3.

The frame sync and data input to the first DSP chip (1A) comes from the PMRDF word sync and PMRDF data, from the ADC module. The DSP is set up such that the extra PMRDF word sync pulses are ignored as are any data bits after the first 24. The PMRDF frame sync goes to the DAC/Sequencer module where it is buffered and inverted before forming the sample clock line to each DSP chip.

3 ADJUSTMENTS

There are no fine adjustments on the DSP boards. There are twelve links on the board, all of which are left open in the current radio configuration. JP1 & JP2 and JP7 & JP8 are used to set the operating mode of the DSP on power-up. One of the other modes would be to instruct the DSP to download memory from the slow EPROM. JP3 & JP4 and JP9 & JP10 are used to allow two different size memory devices to be used for the fast EPROMs. If these links are fitted then 8k x 8 EPROMs can be used in place of the 2k x 8 currently in use. JP5 & JP6 and JP11 & JP12 are used to allow two different size slow EPROM memory, 16k x 8 or 32k x 8, to be fitted, the links again being fitted for the larger memory device.

4 ON-LINE BITE

During normal operation the status of the interface buffer between the DSP chips and the controller is monitored. Each time a message is received by the controller from one of the DSP chips it checks the address sent by the DSP with its own calculated address. If a fault should occur this will be indicated by the 'FAULT' legend appearing on the left hand LCD display. Pressing the BITE key will allow the individual module states to be interrogated. The faults are indicated by either:

02 FAIL 64, which means that the buffer interface between the DSP and the controller has failed. Recommended course of action switch off and then back on again.

02 FAIL xx, where xx is a number between 1 and 32 which indicates that the wrong DSP is being addressed. The fail numbers relate to the individual DSP chips as follows:

1	=	DSP1A
2	=	DSP1B
4	=	DSP2A
8	=	DSP2B
16	=	DSP3A
32	=	DSP3B

Check that each board is in the correct slot and each DSP in its correct place, the 'A' chips (as written on the EPROM labels) are fitted to the correct sockets (IC12, IC13 and IC14) located towards the bottom of the board. EPROMs labelled 'B' are fitted in sockets IC20, IC21 and IC22 located at the top of the board.

5 OFF-LINE BITE

During off-line BITE the DSP runs its own test programs to check RAM and ROM memory and the SSI interface. Any faults in these areas are indicated in modules 11 and 12 of the BITE status listing. Faults should be reported back to the factory.

6 FAULT FINDING

If a fault is suspected on any of the DSP boards then the first thing to check is the presence of the 20 MHz clock. The 20 MHz clock is differential ECL 10 kHz logic levels, the signal comes in on two pairs of lines (8A/9A or 8C/9C) which are identical. If this signal is not present then refer to section 6.11, the DAC/Audio/Sequencer board.

The only other section to check is the SSI. Again the only thing that can be done is to check for the presence of the various signals. At the connector, pins 22A and 23A contain the DSP frame sync pulse to the A and B DSP chips respectively bearing in mind that in the case of DSP1A this is actually PMRDF word sync as shown on the timing diagram. The serial 5 MHz clock to each DSP can be found on connector pins 24A and 25A. The sample clock is on pins 28A and 28C. If any of these are not present refer back to section 6.11, the DAC/Audio/Sequencer board.

The Data lines arrive on the board to DSP 'A' via pin 26A, the output of the first DSP and the input to the second are also available at the connector on pins 26C and 27A and the output from the second DSP is on pin 27C. These lines can only be checked for presence or absence of data and that the data is changing. Absence of data or constant data patterns indicate a fault and reference should be made to section 6.6, the ADC module.

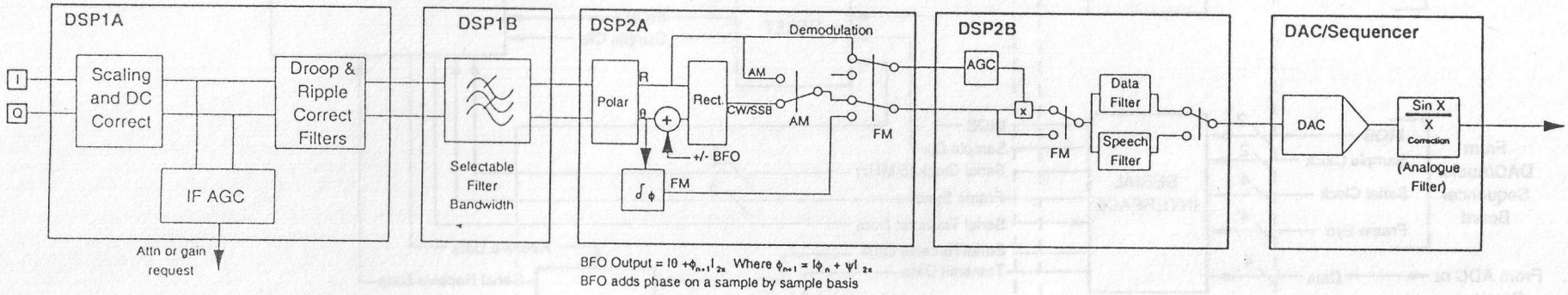


Figure 1 - DSP Boards Functional Diagram

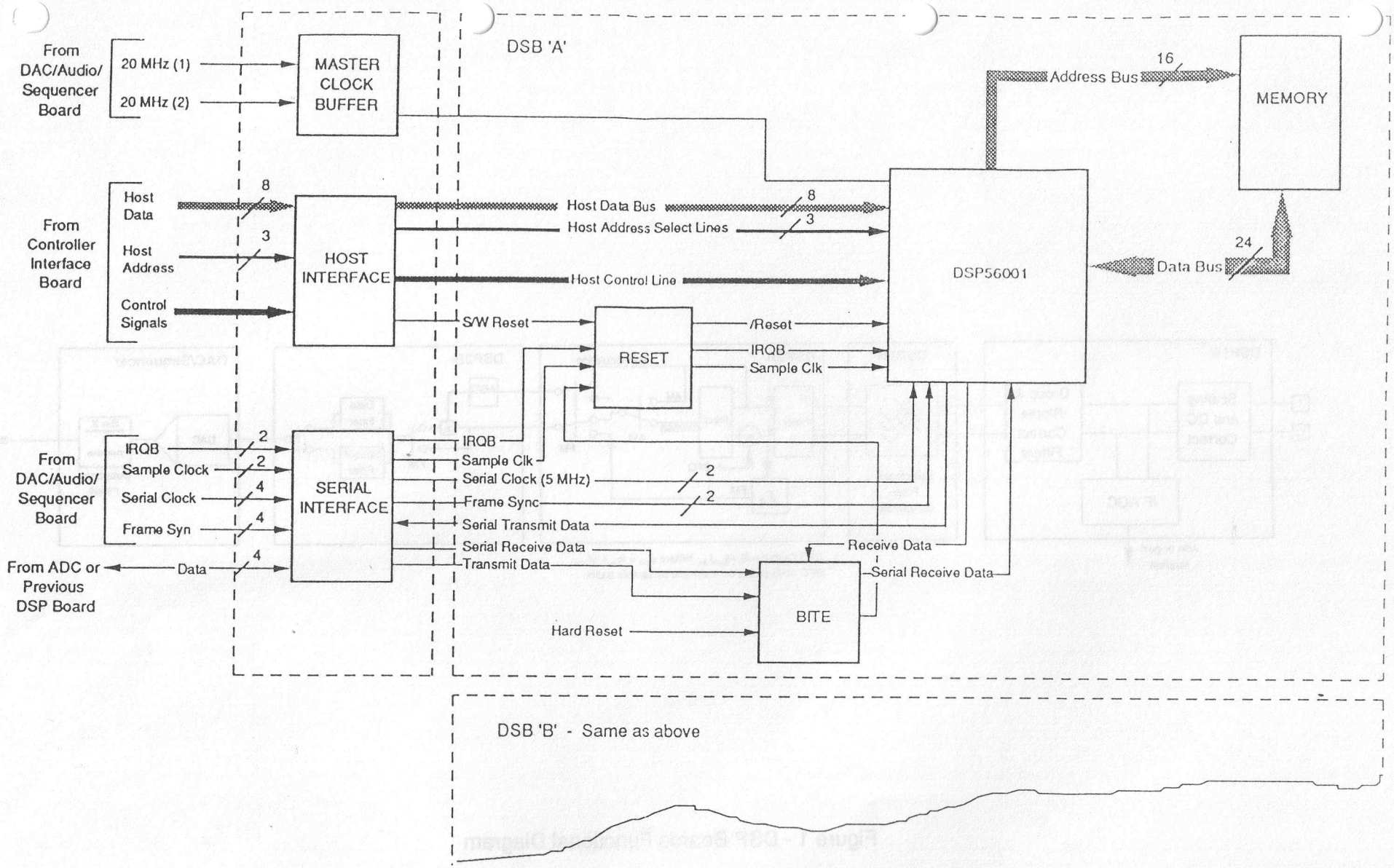
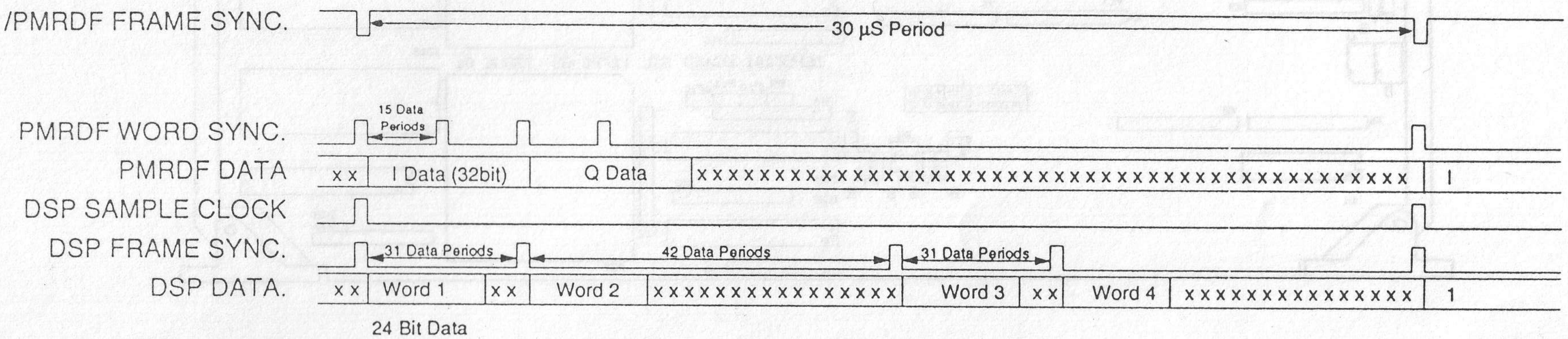


Figure 2 - DSP Board Simplified Block Diagram

Serial Link Timing



Expanded Timing Diagram

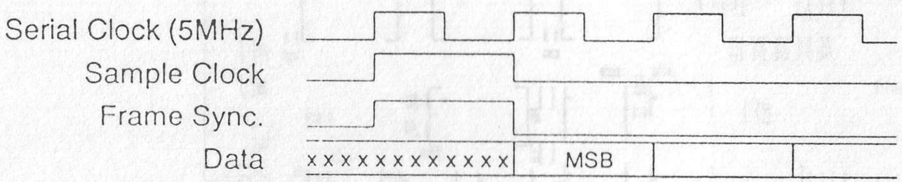


Figure 3 - DSP Board Timing Diagram

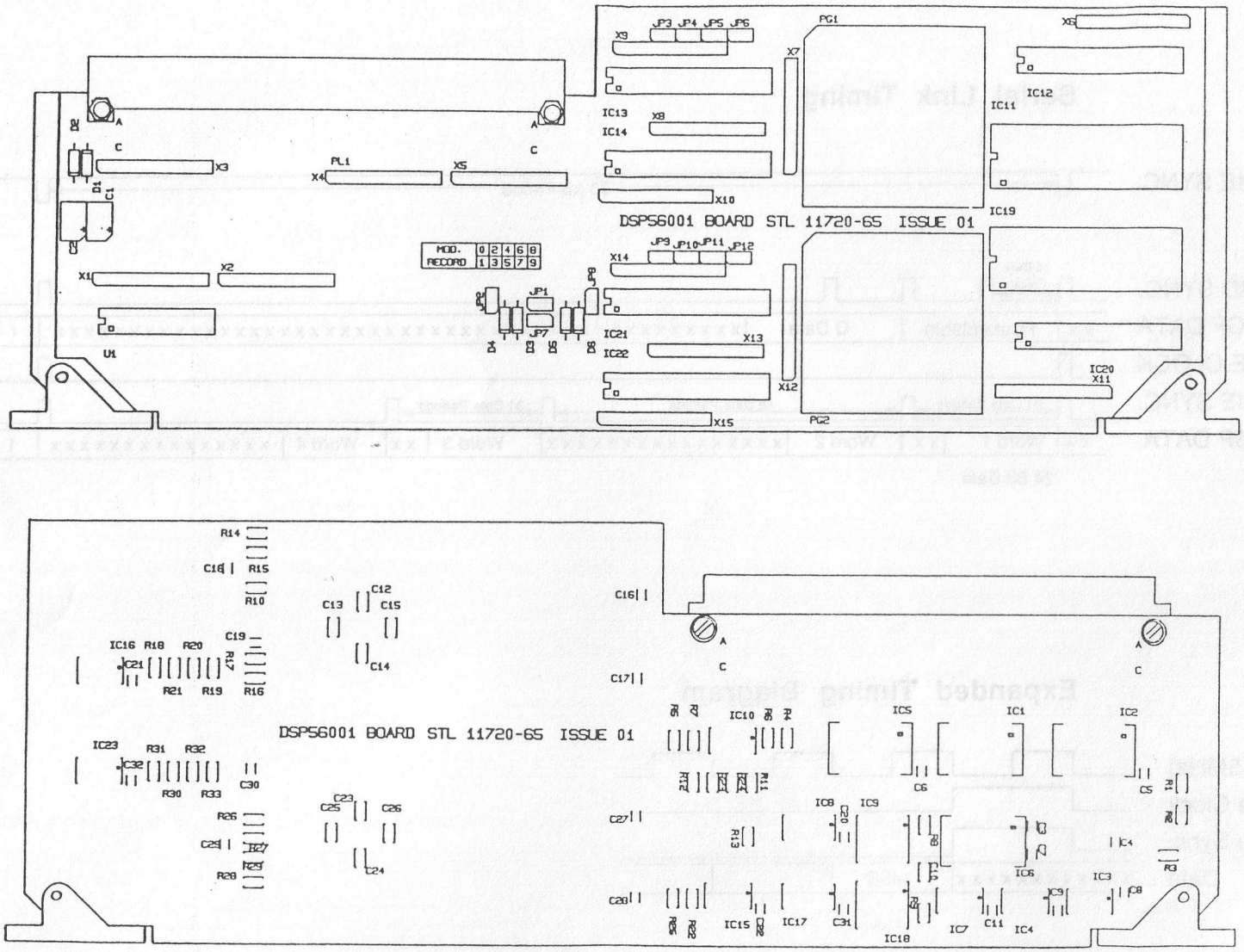


Figure 4 - DSP Board Component Layout

REF	DRAWING NUMBER	DESCRIPTION	N.S.N.	QTY	REMARKS
27	(52CGT004013)	INTEGRATED CIRCUIT, QUAD 2 I/P NAND, NAT SEMI 74AC00SC (14 PIN SOIC) SURFACE MOUNT	-	1	IC4
28	(52CGT004025)	INTEGRATED CIRCUIT, QUAD 2 I/P AND, NAT SEMI 74AC08SC (14 PIN SOIC) SURFACE MOUNT	-	1	IC3
29					
30	(52CGT004028)	INTEGRATED CIRCUIT, QUAD 2 I/P NAND OPEN DRAIN, PHILIPS PC74HC03T (14 PIN SOIC) SURFACE MOUNT	-	1	IC10
31	(52CGT004029)	INTEGRATED CIRCUIT, QUAD 2 I/P NOR, PHILIPS PC74HCT02T (14 PIN SOIC) SURFACE MOUNT	-	1	IC15
32	(52CGT004048)	INTEGRATED CIRCUIT, QUAD 2 I/P OR, NAT SEMI 74AC32SC (14 PIN SOIC) SURFACE MOUNT	-	2	IC16,IC23
33	(52CMU004001)	INTEGRATED CIRCUIT, QUAD 2 I/P MULTIPLEXER, PHILIPS PC74HC157T (16 PIN SOIC) SURFACE MOUNT	-	2	IC8,IC17
34					
35	(52CRS004033/Y)	RESISTOR, FIXED, CHIP, 100K, 5%, 0.25W, RC-01 (1206)	-	4	R4,R5,R6, R7
36	(52CRS004036/Y)	RESISTOR, FIXED, CHIP, 1K, 5%, 0.25W, RC-01 (1206) T/REEL	-	1	R8
37	(52CRS004062/Y)	RESISTOR, FIXED, CHIP, 4K7, 5%, 0,25W, RC-01 (1206)	-	1	R9
38	(52CRS004063/Y)	RESISTOR, FIXED, CHIP, 10K, 5%, 0.25W, RC-01 (1206) T/REEL	-	4	R14,R15, R26,R27
39	(52CRS004064/Y)	RESISTOR, FIXED, CHIP, 15K, 5%, 0,25W, RC-01 (1206) T/REEL	-	6	R11,R12,R13, R23,R24,R25
40	(52CRS004095)	RESISTOR, FIXED, CHIP, 2K, 5%, 0.25W, RC-01 (1206) T/REEL	-	3	R1,R2,R3

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TITLE DSP BOARD ASSEMBLY
N.S.N -
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CLASS UNCLASSIFIED

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REF	DRAWING NUMBER	DESCRIPTION	N.S.N.	QTY	REMARKS
41	(52CRS004116)	RESISTOR, FIXED, CHIP, 47K, 5%, 0.25W, RC-01 (1206) T/REEL	-	14	R10,R16,R17, R18,R19,R20, R21,R22,R28, R29,R30,R31, R32,R33
42					
43					
44	(52CRS004127)	RESISTOR, NETWORK, 100K, 2%, 1.125W, SINGLE-IN-LINE, BOURNS 4609X-101 9 PIN SIL, 8 RESISTOR ONE COMMON PIN	-	1	X1
45	(52CRS004246)	RESISTOR, NETWORK, 47K, 2%, 1.125W, SINGLE-IN-LINE, BOURNS 4609X-101 9 PIN SIL, 8 RESISTOR ONE COMMON PIN	-	14	X2,X3,X4,X5, X6,X7,X8,X9, X10,X11,X12, X13,X14,X15
46					
47					
48					
49	(52CSD234030)	DIODE, ZENER, PHILIPS BZX79C6V2 DO-35	-	2	D1,D2
50					
51	(52CSP004002)	INTEGRATED CIRCUIT, DIGITAL SIGNAL PROCESSOR + RAM, MOTOROLA DSP56001RC20 (68 PIN PGA)	-	2	PG1,PG2
52	(52CSR004009)	INTEGRATED CIRCUIT, 2048 X 8 REPROGRAMMABLE PROM, CYPRESS CY7C291-50WC (24 PIN 7.62 mm ROW SPACING)	-	6	IC12,IC13, IC14,IC20, IC21,IC22
53	(52CTV004014)	INTEGRATED CIRCUIT, OCT BUS TRANS TRI STATE, NAT SEMI MM74HCT245WM (20 PIN SOIC WIDE BODY) SURFACE MOUNT	-	1	IC2

	TITLE DSP BOARD ASSEMBLY	ITEMS LIST 52UPB504073-2.1
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REF	DRAWING NUMBER	DESCRIPTION	N.S.N.	QTY	REMARKS
27	(52CGT004013)	INTEGRATED CIRCUIT, QUAD 2 I/P NAND, NAT SEMI 74AC00SC (14 PIN SOIC) SURFACE MOUNT	-	1	IC4
28	(52CGT004025)	INTEGRATED CIRCUIT, QUAD 2 I/P AND, NAT SEMI 74AC08SC (14 PIN SOIC) SURFACE MOUNT	-	1	IC3
29					
30	(52CGT004028)	INTEGRATED CIRCUIT, QUAD 2 I/P NAND OPEN DRAIN, PHILIPS PC74HC03T (14 PIN SOIC) SURFACE MOUNT	-	1	IC10
31	(52CGT004029)	INTEGRATED CIRCUIT, QUAD 2 I/P NOR, PHILIPS PC74HCT02T (14 PIN SOIC) SURFACE MOUNT	-	1	IC15
32	(52CGT004048)	INTEGRATED CIRCUIT, QUAD 2 I/P OR, NAT SEMI 74AC32SC (14 PIN SOIC) SURFACE MOUNT	-	2	IC16,IC23
33	(52CMU004001)	INTEGRATED CIRCUIT, QUAD 2 I/P MULTIPLEXER, PHILIPS PC74HC157T (16 PIN SOIC) SURFACE MOUNT	-	2	IC8,IC17
34					
35	(52CRS004033/Y)	RESISTOR, FIXED, CHIP, 100K, 5%, 0.25W, RC-01 (1206)	-	4	R4,R5,R6, R7
36	(52CRS004036/Y)	RESISTOR, FIXED, CHIP, 1K, 5%, 0.25W, RC-01 (1206) T/REEL	-	1	R8
37	(52CRS004062/Y)	RESISTOR, FIXED, CHIP, 4K7, 5%, 0,25W, RC-01 (1206)	-	1	R9
38	(52CRS004063/Y)	RESISTOR, FIXED, CHIP, 10K, 5%, 0.25W, RC-01 (1206) T/REEL	-	4	R14,R15, R26,R27
39	(52CRS004064/Y)	RESISTOR, FIXED, CHIP, 15K, 5%, 0,25W, RC-01 (1206) T/REEL	-	6	R11,R12,R13, R23,R24,R25
40	(52CRS004095)	RESISTOR, FIXED, CHIP, 2K, 5%, 0.25W, RC-01 (1206) T/REEL	-	3	R1,R2,R3

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REF	DRAWING NUMBER	DESCRIPTION	N.S.N.	QTY	REMARKS
54	(52CVM004001)	INTEGRATED CIRCUIT, MICROMONITOR, DALLAS DS1232S (16 PIN SOIC) SURFACE MOUNT	-	2	IC9,IC18
55					
56	BS4185 (52PSW904195/Y)	SCREW, PAN HD., M2.5x0.45-6g x 10 LONG, ST.ST.	-	2	-
57	BS4463 (52PWX904013/Y)	WASHER, CRINKLE, M2.5, ST.ST.	-	2	-
58	BS3692 (52PNT904055/Y)	NUT, FULL, M2.5x0.45-6H, ST.ST.	-	2	-

	TITLE DSP BOARD ASSEMBLY	ITEMS LIST 52UPB504073-2.1
STC RADIO AND MICROWAVE PAIGNTON DEVON	N.S.N - USED ON STR8212 CLASS UNCLASSIFIED	SHEET 6 OF 6 ISSUE C MOD/AMEND TR104 DATE 13-9-90

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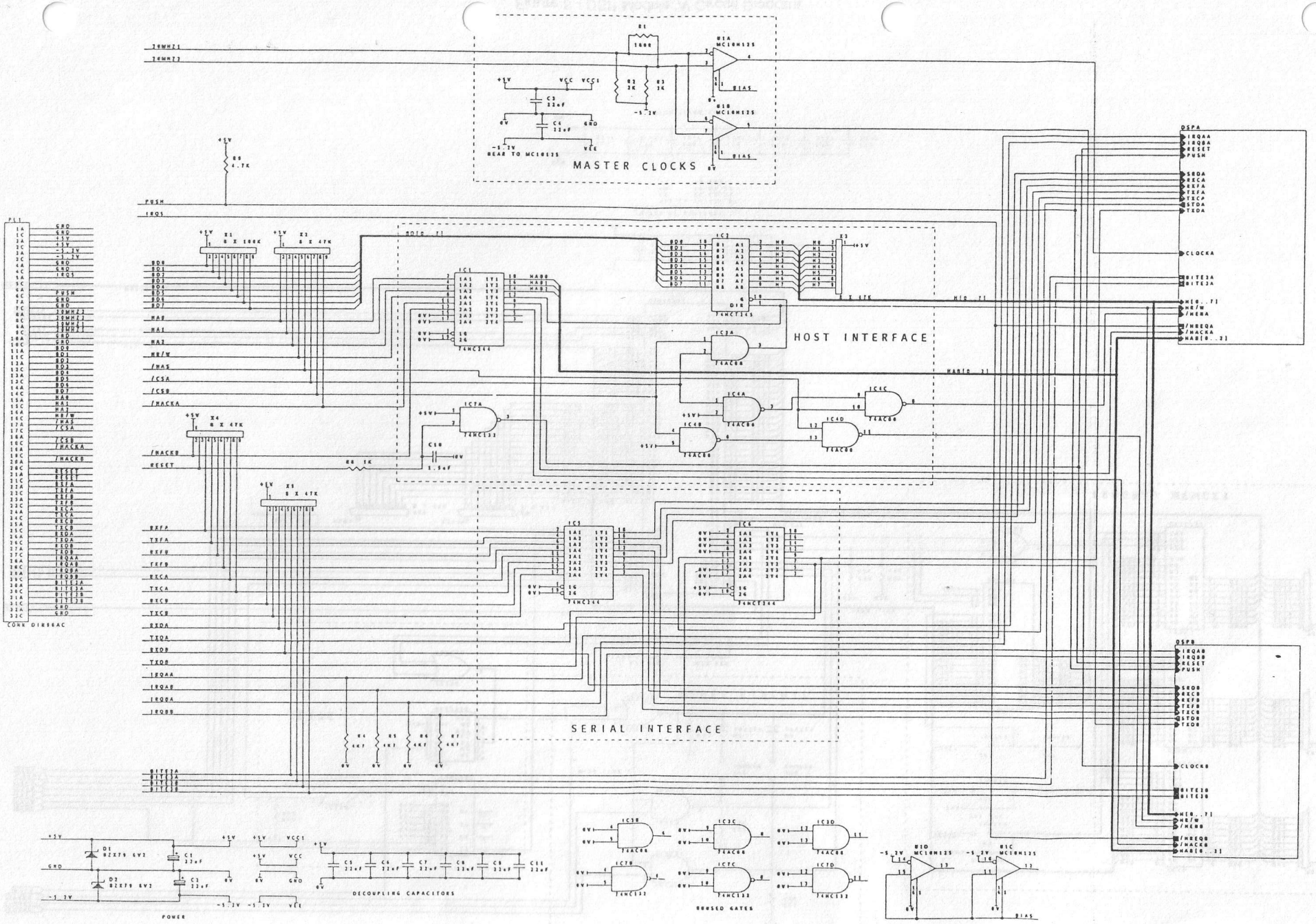


Figure 5 - DSP Board Clock Buffer, Serial and Host Interface Circuit Diagram

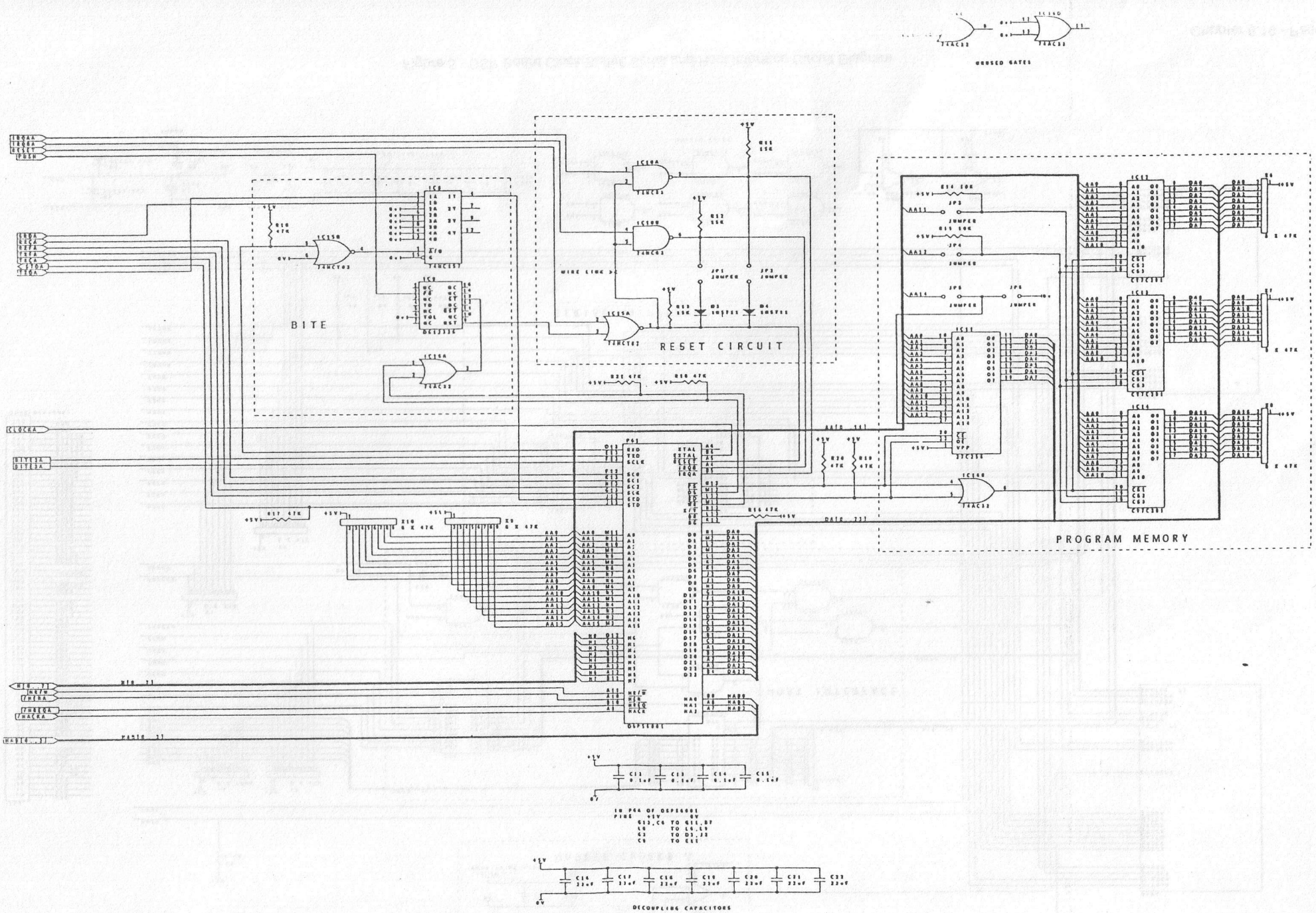


Figure 6 - DSP Module 'A' Circuit Diagram

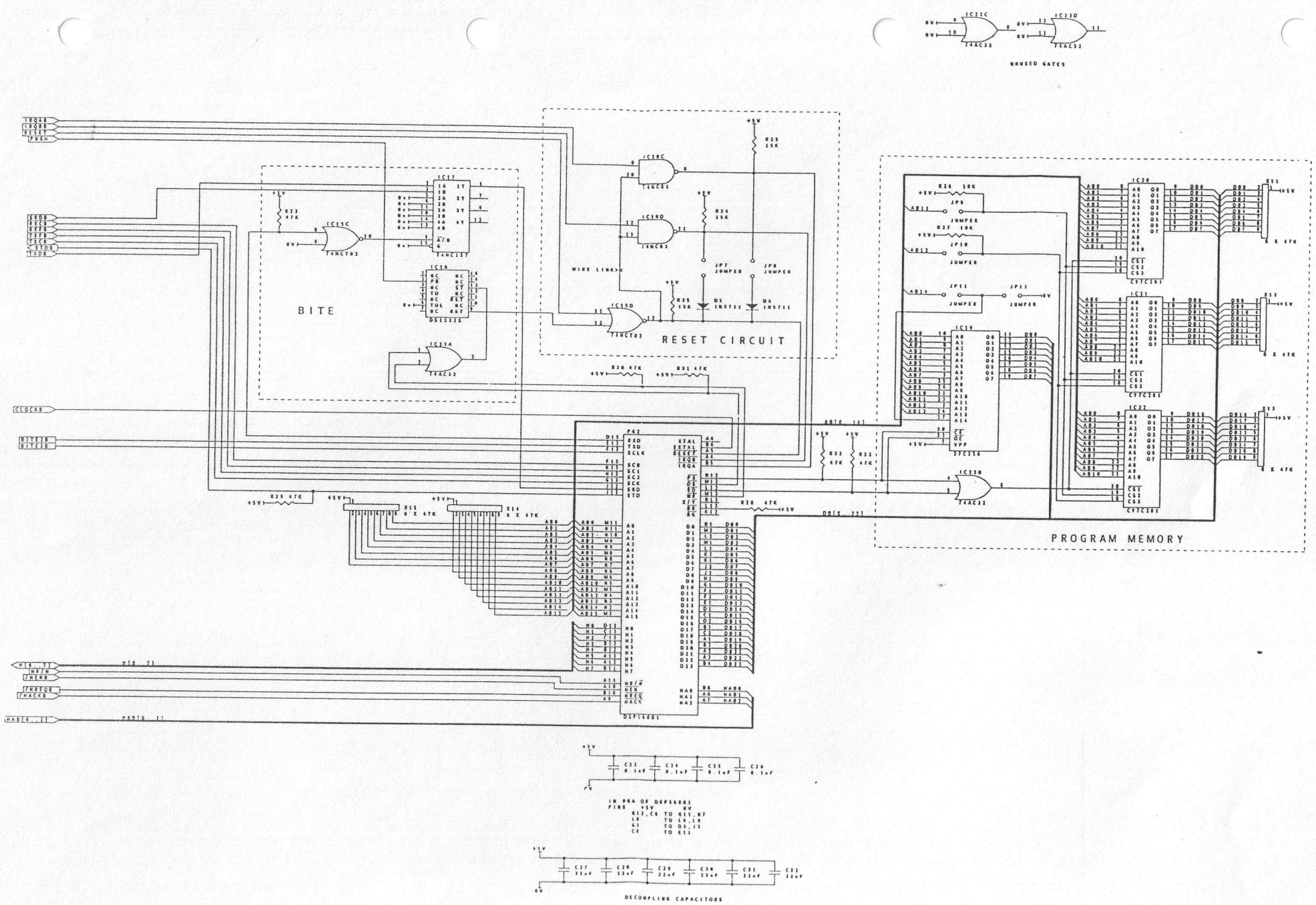


Figure 7 - DSP Module 'B' Circuit Diagram

Chapter 6.11

DAC/SEQUENCER BOARD ASSEMBLY

1 INTRODUCTION

The DAC/Sequencer Board Assembly is a single PCB which plugs directly into the Digital Backplane via a single 64 way connector SKT 48.

The board is of multi-layer construction and has components fitted to both sides. Two multi-turn potentiometers RV1 and RV2 are sited near the top edge of the board towards the rear. These potentiometers set the nominal output levels for the Line1 [BAL] and Line2 [ISB] outputs. Two single turn potentiometers, RV3 and RV4, are also sited near the top edge of the board. These potentiometers set the dc offset on the line outputs, these two potentiometers should not require user adjustment. An EPROM IC14 contains the Sequencer program.

This board description is given with reference to the following drawings, illustrations and items list:

- Figure 1 DAC/Sequencer Simplified Block Diagram
- Figure 2 Sequencer Output Timing Diagram
- Figure 3 DAC/Sequencer Board Component Layout
- Items List DAC/Sequencer board Sheets 1 to 6
- Figure 4 DAC/Sequencer Module Interconnection Diagram
- Figure 5 Line2 Active LPF Circuit Diagram
- Figure 6 Sample and Hold Amplifier Circuit Diagram
- Figure 7 Audio Amplifier Circuit Diagram
- Figure 8 Line1 Active LPF Circuit Diagram
- Figure 9 Digital to Analogue Converter (DAC) Circuit Diagram
- Figure 10 Line2 Buffer Circuit Diagram
- Figure 11 Line1 Buffer Circuit Diagram
- Figure 12 Sequencer Circuit Diagram
- Figure 13 DAC Connector Circuit Diagram

2 MODULE DESCRIPTION

The DAC/Sequencer board fulfills the following two completely separate functions:

- Analogue Output - The signals from the DSP modules are converted to the analogue domain. They are then filtered and amplified to form the receiver's audio outputs.
- DSP Timing - The sequencer provides the timing signals that ensure that the data transfers between the ADC, DSP Modules and DAC are performed in the correct sequence.

2.1 Analogue Output

The digital signal path from the DSP sub-system is converted by the DAC into two channels of analogue signals, 'L' and 'R'. The DAC has its own +5 volt regulator, IC25, running off the +18 volt supply to the board. The 'L' channel output is fed through an active low pass filter (LPF) which removes quantisation noise and produces a smooth analogue signal. The output from the filter stage is fed via RV1 to a buffer amplifier which produces the Line1 [BAL] (balanced) output on the receiver's back panel, this differential output has an output impedance of 600 ohms. The signal at the Line1 [BAL] active low pass filter output is also fed to the Audio Amplifier which drives the receiver's internal speaker and phone jack on the front panel. The Audio Amplifier has another output that drives the External Speaker output at the back panel Audio connector. The output level of the audio amplifier is controlled by the VOL signal from the front panel Volume Control potentiometer. This potentiometer is fed with a dc voltage from the DAC/Sequencer VOL(+) and VOL(-) outputs.

The 'R' channel output from the DAC is fed via a Sample and Hold amplifier before being passed through Line2 [ISB] active low pass filter. The smoothed analogue signal is then taken via RV2 to the Line2 [ISB] buffer amplifier producing the Line2 [ISB] (balanced) output on the receiver back panel.

The Line1 [BAL] and Line2 [ISB] active low pass filters and buffer amplifiers are identical. In a receiver not fitted with the ISB option the 'L' and 'R' outputs from the DAC are always identical leading to identical signals at the Line1 [BAL] and Line2 [ISB] outputs.

Note: *The amplitude of the signals may differ if the setting of RV1 or RV2 has been altered from the factory preset.*

2.2 DSP Timing

The Sequencer section of the board produces 'SAMCLK', 'FSDSP' and the DAC timing signals synchronised to 'SERCLK' and '/FS PMRDF' from the ADC module. 'SAMCLK' sets the radio's DSP sampling period. 'FSDSP' controls the timing of the serial data transfers into and out of the DSP modules. The ADC module is thus in control of the timing of the receiver's DSP sub-section.

The Sequencer EPROM (IC14) is a 32k x 8 device. Pin 27 (A14) is held high thus only the upper 16 kbytes are used. The binary counter (IC17 & IC18) is connected to the EPROM's 8 lowest address bits (A0...A7). The Sequencer EPROM is thus divided into pages of 256 bytes.

The upper 16 kbytes of the Sequencer EPROM contains 64 memory pages. Each page could potentially contain a separate signal sequence and circuitry has been included in the board design to allow page selection by the Controller via the Buffered Data bus (BD0...BD5). For the STR8212 receiver only one sequence is required therefore the same information has been copied into all 64 active memory pages, thus the output of the Input Register (IC15) can make no difference to the signal sequence. The signal sequence is purely controlled by address bits 'A0...A7' of the EPROM. These address bits are derived from a binary counter (IC17 & IC18). This counter is clocked by 'SERCLK' and uses '/FS PMRDF' (via the latch IC20A) as its load signal. The counter is preset to 0 by '/FS PMRDF' and counts up to 150 before '/FS PMRDF' occurs again to restart the sequence. The clear input of the counter is connected to a power on reset and '/RESET' from the Controller, this counter input is thus normally inactive. See Figure 2 for the Sequencer output timing diagram.

Sequencer EPROM output 'SAMCLK' is buffered and passed onto the DSP modules where it drives their 'IRQA' interrupt input, this enables the DSP processors to proceed with their program cycle one per sample period. 'FSDSP' is buffered and forms the 'RXFA', 'TXFA', 'RXFB' and 'TXFB' signals to the DSP boards, these serial link flag signals define the word positions on the digital signal path. 'SERCLK' is buffered and forms the 'RXCA', 'TXCA', 'RXCB' and 'TXCB' signals to the DSP boards, this is the clock signal for the serial data on the digital signal path.

The Sequencer also produces the timing signals 'LRCLK', 'WDCLK' and 'SHCLK'. 'LRCLK' and 'WDCLK' are DAC timing signals. 'SHCLK' controls the sample and hold circuit (IC6).

The 40 MHz input from the Reference Module is differentially received, divided by 2 and buffered to produce a complimentary 20 MHz ECL output which forms the clock for the DSP processors.

3 ALIGNMENT AND DIAGNOSTIC NOTES

Alignment and diagnostic notes are given under the following headings:

- Board Set-up — Paragraph 3.1
- Line Output Adjustment — Paragraph 3.2
- Diagnostics — Paragraph 3.3

3.1 Board Set-up

The board has six jumper link positions. For normal operation links are fitted in LK1, LK2 , LK4 and LK5 positions. LK3 and LK6 are left open.

3.2 Line Output Adjustment

Potentiometers RV1 & RV2 are factory preset to yield a nominal output level of +2 dBm at the Line1 [BAL] and Line2 [ISB] outputs into a balanced 600 ohm load. However the nominal output level from these outputs is designed to be adjustable over the range -20 dBm to +10 dBm. Should the user wish to set the nominal output level to a different level the following set up procedure is recommended:

Set the receiver frequency to 12276 kHz and set the BFO to -0.8 kHz. Set the mode to CW with a bandwidth of 3 kHz. Set the AGC to MED, turn the DATA filter on. Apply a CW signal of 12276 kHz at -50 dBm to the receiver's antenna input.

Measure the output at the Line1 [BAL] output into 600 ohms (Rear Panel Audio connector pin 4 wrt pin 9). Set RV1 to achieve the desired level.

Measure the output at the Line2 [ISB] output into 600 ohms (Rear Panel Audio connector pin 3 wrt pin 8). Set RV2 to achieve the desired level.

3.3 Diagnostics

All measurement figures given in this section are typical values.

3.3.1 Sequencer checks

Check the sequencer output signals 'SAMCLK', 'RXFA', 'TXFA', 'RXFB', 'TXFB', 'RXCA', 'TXCA', 'RXCB', 'TXCB', 'SHCLK', 'LRCLK' and 'WDCLK' are present. Figure 4 shows the timing of these pulses. 'RXFA', 'TXFA', 'RXFB' and 'TXFB' are buffered versions of 'FSDSP'. RXCA', 'TXCA', 'RXCB' and 'TXCB' are buffered versions of 'SERCLK' a 5 MHz continuous clock signal. 'SAMCLK', 'RXFA', 'TXFA', 'RXFB', 'TXFB', 'RXCA', 'TXCA', 'RXCB' and 'TXCB' must be present for the DSP modules to function and they must be present before the rest of the diagnostic tests are performed. Check that the 20 MHz ECL clock output is present.

3.3.2 Set-up for test

Set the receiver frequency to 12276 kHz and set the BFO to -0.8 kHz. Set the mode to CW with a bandwidth of 3 kHz. Set the AGC to MED, turn the DATA filter on. Apply a CW signal of 12276 kHz at -50 dBm to the receiver's antenna input.

3.3.3 DAC checks

Check that a 0.6 volt peak to peak stepped sine wave is present at test point P4, this sine wave will have a mean voltage of +2.2 volts. The sine wave frequency will be 800 Hz and the sampling frequency 66.7 kHz. This waveform will have high frequency noise and sampling spikes superimposed on it, these high frequency components are rejected by the following low pass filter. Check that a similar stepped sine wave is present on P5, the signals peak to peak amplitude will be 0.6 volts and its mean voltage will be -2.2 volts. The Digital Output board (if fitted) may be used to check for the presence of the 800 Hz sine wave in the input data to the DAC, the peak amplitude will be 1DF732 hexadecimal.

3.3.4 Line1 (BAL) channel checks

Check that a 3.4 volt peak to peak sine wave is present at test point P6. The sine wave frequency will be 800 Hz. Check that the sine wave output is present at Line1(+) [PL1 pin 30A] and Line1(-) [PL1 pin 30C], RV1 can be adjusted to vary the output level. When measured differentially into a 600 ohm load an output amplitude of +10 dBm should be achievable on the Line1 output by adjustment of RV1. Should the mean voltage at the Line1 output not be 0 volts, RV3 can be adjusted to null the mean voltage. Should a fault in the active low pass filter be suspected, shorting link LK1 can be removed to allow the injection of a signal into the filter. Shorting link LK3 can be inserted to remove the dc offset in the output at P6. The filter should have the following characteristics:

Passband	0 Hz to 8 kHz (3 dB point = 8 kHz)
Insertion loss at 3 kHz	< 0.5 dB
Attenuation at 25 kHz	> 50 dB
Attenuation at 58 kHz	> 65 dB

Shorting link LK2 may be removed to break the filters feedback loop to aid diagnostics at component level. Ensure all links are in their operational positions (See paragraph 3.1 'Board Set-up') at the completion of testing.

3.3.5 Audio amplifier checks

Without the headphones or external speaker connected it should be possible to achieve a drive level of 6 volts peak to peak to the internal speaker by adjustment of the Front Panel Volume Control. Setting the Volume control much higher than this will result in a distorted waveform to the speaker as the audio amplifier goes into current limit.

3.3.6 Sample and Hold check

Check that a 0.6 volt peak to peak stepped sine wave is present at test point P9, this sine wave will have a mean voltage of +2.3 volts. The sine wave frequency will be 800 Hz and the sampling frequency 66.7 kHz. This waveform will have high frequency noise and sampling spikes superimposed on it, these high frequency components are rejected by the following low pass filter.

3.3.7 Line2 (ISB) channel checks

Check that a 3.4 volt peak to peak sine wave is present at test point P8. The sine wave frequency will be 800 Hz. Check that the sine wave output is present at Line2(+) [PL1 pin 29A] and Line2(-) [PL1 pin 29C], RV2 can be adjusted to vary the output level. When measured differentially into a 600 ohm load an output amplitude of +10 dBm should be achievable on the Line2 output by adjustment of RV2. Should the mean voltage at the Line2 output not be 0 volts, RV4 can be adjusted to null the mean voltage. Should a fault in the active low pass filter be suspected, shorting link LK4 can be removed to allow the injection of a signal into the filter. Shorting link LK6 can be inserted to remove the dc offset in the output at P8. The filter should have the following characteristics:

Passband	0 Hz to 8 kHz (3 dB point = 8 kHz)
Insertion loss at 3 kHz	< 0.5 dB
Attenuation at 25 kHz	> 50 dB
Attenuation at 58 kHz	> 65 dB

Shorting link LK5 may be removed to break the filters feedback loop to aid diagnostics at component level. Ensure all links are in their operational positions (See paragraph 3.1 'Board Set-up') at the completion of testing.

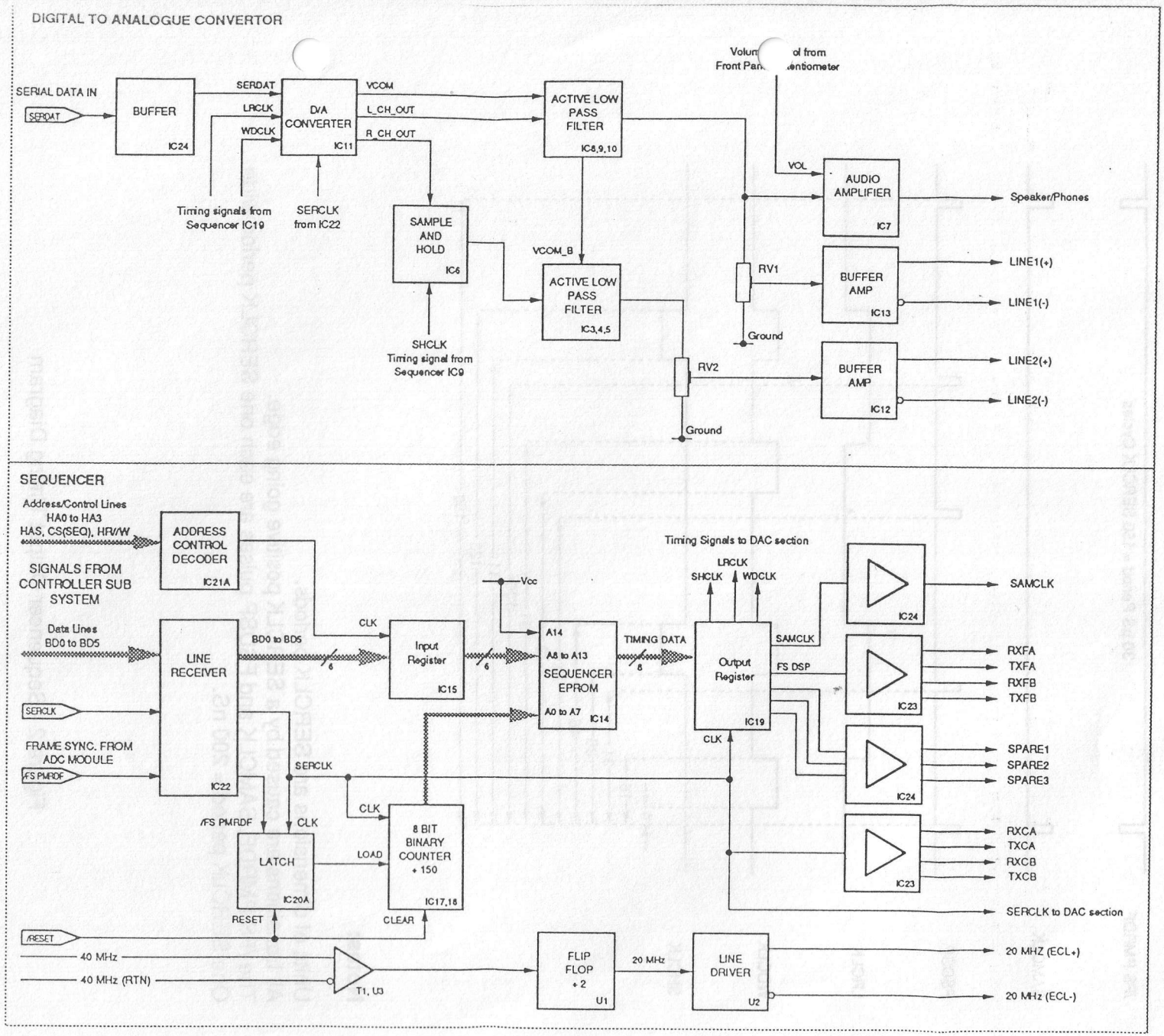
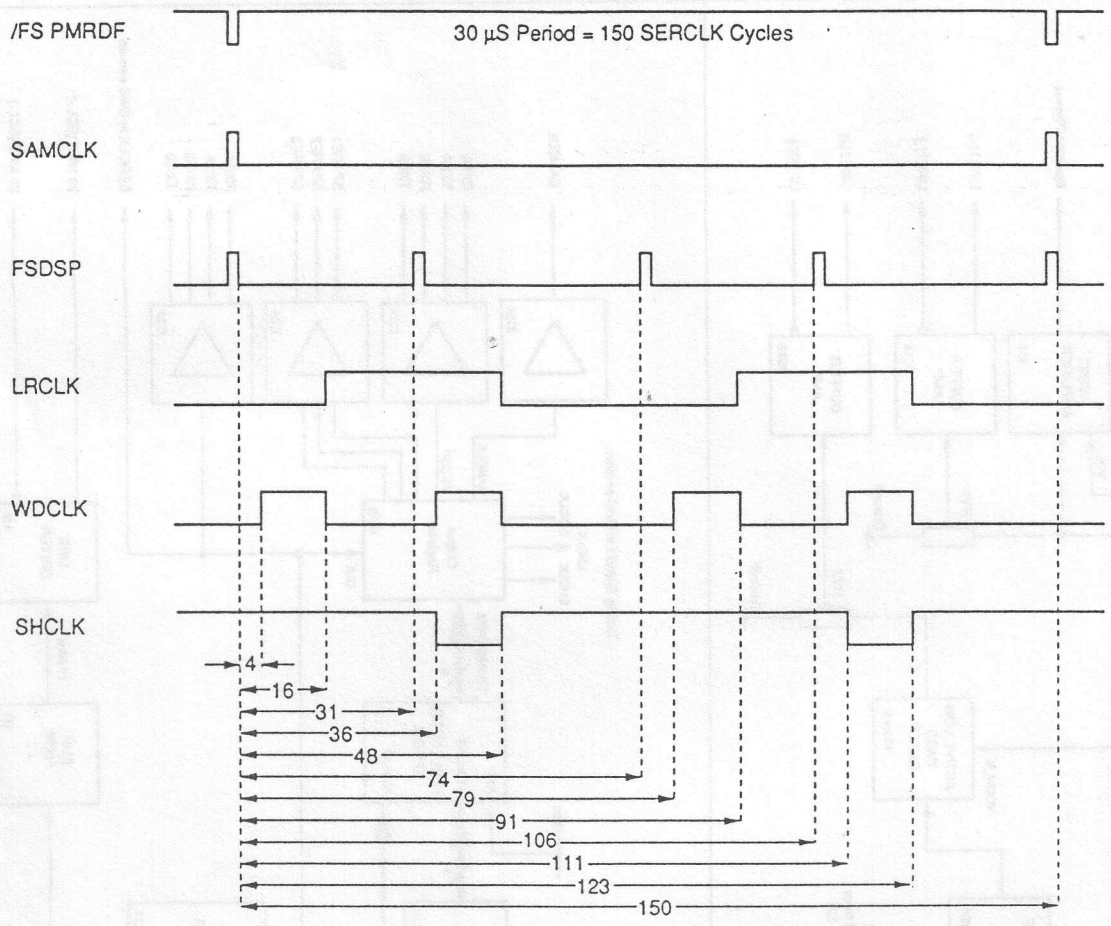


Figure 1 - DAC/Sequencer Simplified Block Diagram



Notes:

Units of dimensions are SERCLK periods.
All transitions are caused by a SERCLK positive going edge.
The /FS PMRDF, SAMCLK and FSDSP pulses are each one SERCLK period wide.
One SERCLK period = 200 nS.

Figure 2 - Sequencer Output Timing Diagram

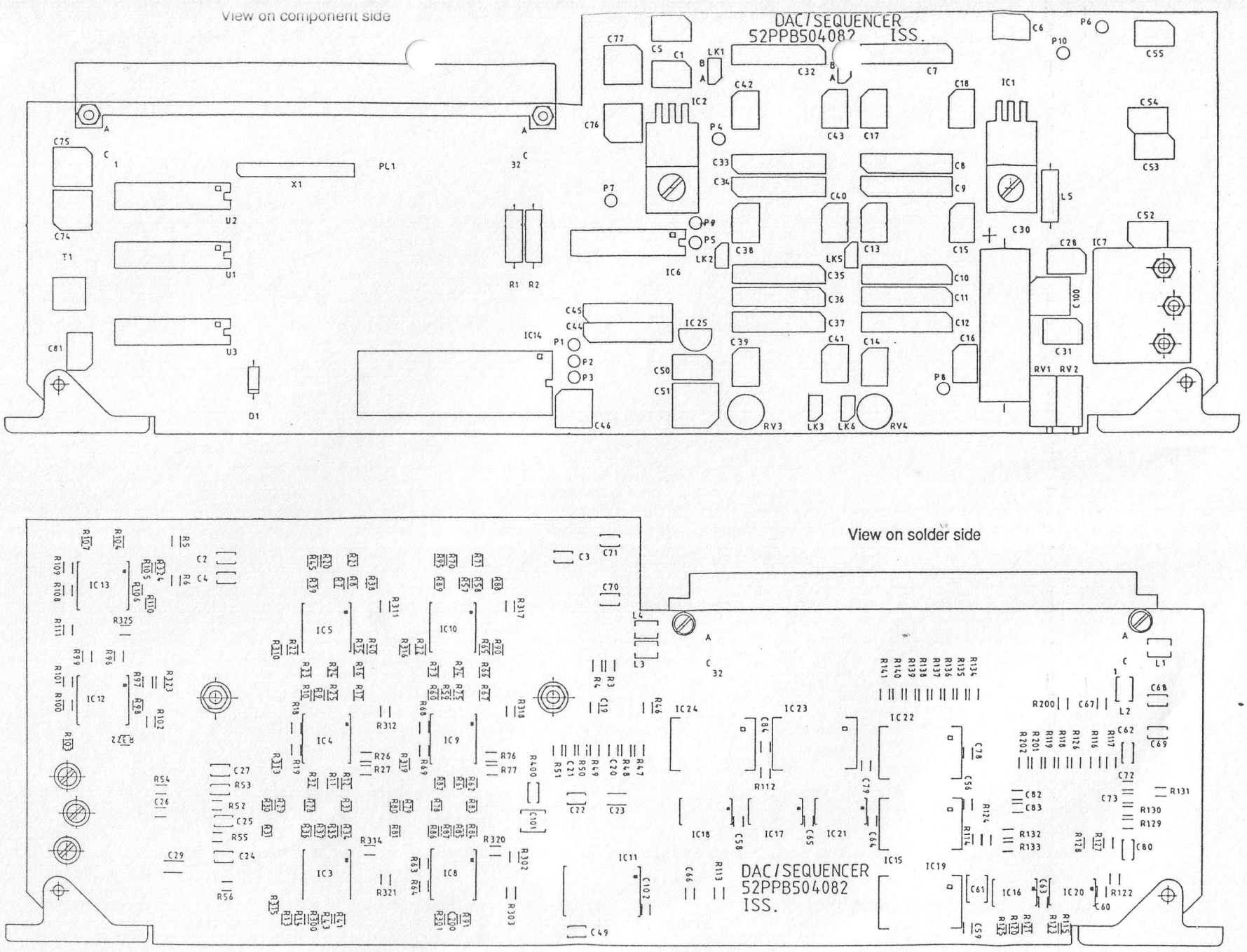


Figure 3 - DAC/Sequencer Board Component Layout

Circuit Reference	Description	Value
C1	Capacitor, fixed, solid tant, 20%, 35V	1µ
C2 to C4	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C5 & C6	Capacitor, fixed, solid tant, 20%, 35V	2µ2
C7 to C12	Capacitor, fixed, polystyrene, 63V	10n
C13 to C18	Capacitor, fixed, solid tant, 20%, 35V	1µ
C19	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C20	Capacitor, fixed, ceramic chip, 5%, 100V	100p
C21	Capacitor, fixed, ceramic chip, 5%, 100V	10p
C22 to C25	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C26	Capacitor, fixed, ceramic chip, 10%, 100V	2n2
C27	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C28	Capacitor, fixed, solid tant, 20%, 35V	1µ
C29	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C30	Capacitor, fixed, al electrolytic, 20%, 40V	470µ
C31	Capacitor, fixed, solid tantulum, 20%, 35V	2µ2
C32 to C37	Capacitor, fixed, polystyrene, 63V	10n
C38 to C43	Capacitor, fixed, solid tant, 20%, 35V	1µ
C44 & C45	Capacitor, fixed, polystyrene, 1%, 630V	300p
C46	Capacitor, fixed, solid tant, 20%, 35V	10µ
C49	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C50	Capacitor, fixed, solid tant, 20%, 35V	3µ3
C51	Capacitor, fixed, solid tant, 20%, 10V	100µ
C52 to C55	Capacitor, fixed, solid tant, 20%, 35V	1µ
C56	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C58 to C60	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C61	Capacitor, fixed, ceramic chip, 10%, 63V	470n
C62	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C63 to C67	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C68 to C71	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C72 & C73	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C74 to C77	Capacitor, fixed, solid tantulum, 20%, 35V	10µ
C78 & C79	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C80	Capacitor, fixed, ceramic chip, 10%, 50V	100n

Circuit Reference	Description	Value
C81	Capacitor, fixed, solid tantulum, 20%, 35V	1µ
C82 to C83	Capacitor, fixed, ceramic chip, ±0.5p, 100V	4p7
C84	Capacitor, fixed, ceramic chip, 10%, 50V	22n
C100	Capacitor, fixed, solid tantulum, 20%, 35V	10µ
C101	Capacitor, fixed, ceramic chip, 10%, 50V	330n
C102	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C200	Capacitor, fixed, ceramic chip, 10%, 100V	2n2
IC1	Voltage Regulator, 15V, LM7815CT	
IC2	Voltage Regulator, -15V, LM7915CT	
IC3 to IC5	Quad, Op Amp, LF347WM	
IC6	Sample and Hold Amp, TDA1535	
IC7	Audio Amp, TDA1013A	
IC8 to IC10	Quad, Op Amp, LF347WM	
IC12 to IC13	Low Noise, Op Amp, NE5532D	
IC14	CMOS EPROM, 85ns, HN27C256HG-85	
IC15	Octal D Type Flip Flop, Positive Edge Triggered, PC74HC574T	
IC16	Quad, 2 Input Nand Schmitt, PC74HC132T	
IC17 & IC18	Presettable Synchronous Binary Counter, PCHC161T	
IC19	Octal D Type Flip Flop, Positive Edge Triggered, PC74HC574T	
IC20	Dual D Type Flip Flop, 74ACT74SC	
IC21	1 of 8 Decoder, 74AC138SC	
IC22	Octal Buffer, Line Driver, 74AC541SC	
IC23 & IC24	Octal Buffer, PC74HC541T	
IC25	Voltage Regulator, +5V, LM78L05ACZ	
U1	Dual D Type Flip Flop, MC10131P	
U2	Quad OR/NOR, MC10101P	
U3	Triple Line Receiver, MC10116P	

DAC/Sequencer Board Items List - Sheet 2 of 6

Circuit Reference	Description	Value
R1	Resistor, fixed metal film,10%, 0.5W	1R5
R2	Resistor, fixed metal film,10%, 0.5W	2R7
R3	Resistor, fixed, chip, 1%, 0.125W	180R
R4	Resistor, fixed, chip, 1%, 0.1W	10k
R5	Resistor, fixed, chip, 1%, 0.1W	1k
R6	Resistor, fixed, chip, 1%, 0.1W	120R
R7 to R12	Resistor, fixed, chip, 1%, 0.1W	2k
R13	Resistor, fixed, chip, 1%, 0.1W	43k
R14	Resistor, fixed, chip, 1%, 0.1W	220k
R15	Resistor, fixed, chip, 1%, 0.1W	1k3
R16	Resistor, fixed, chip, 1%, 0.1W	2k
R17	Resistor, fixed, chip, 2%, 0.1W	82R
R18	Resistor, fixed, chip, 1%, 0.1W	2k2
R19	Resistor, fixed, chip, 2%, 0.1W	39R
R20	Resistor, fixed, chip, 1%, 0.1W	1k
R21	Resistor, fixed, chip	0R
R22	Resistor, fixed, chip, 1%, 0.1W	1k3
R23	Resistor, fixed, chip, 2%, 0.1W	43R
R24	Resistor, fixed, chip, 1%, 0.1W	2k
R25	Resistor, fixed, chip, 2%, 0.1W	82R
R27	Resistor, fixed, chip, 2%, 0.1W	39R
R26	Resistor, fixed, chip, 1%, 0.1W	2k2
R28	Resistor, fixed, chip, 1%, 0.1W	2k4
R29	Resistor, fixed, chip, 2%, 0.1W	22R
R30	Resistor, fixed, chip, 1%, 0.1W	3k3
R31	Resistor, fixed, chip, 1%, 0.1W	130R
R32	Resistor, fixed, chip, 1%, 0.1W	2k4
R33	Resistor, fixed, chip, 2%, 0.1W	22R
R34	Resistor, fixed, chip, 1%, 0.1W	3k3
R35	Resistor, fixed, chip, 1%, 0.1W	130R
R36	Resistor, fixed, chip, 1%, 0.1W	3k9
R37	Resistor, fixed, chip, 1%, 0.1W	270R
R38 & R39	Resistor, fixed, chip, 1%, 0.1W	100k

Circuit Reference	Description	Value
R40	Resistor, fixed, chip, 2%, 0.1W	43R
R41	Resistor, fixed, chip, 1%, 0.1W	220k
R43	Resistor, fixed, chip, 1%, 0.1W	100k
R45	Resistor, fixed, chip, 1%, 0.1W	1k
R46	Resistor, fixed, chip, 2%, 0.1W	22R
R47	Resistor, fixed, chip, 1%, 0.1W	1k
R48	Resistor, fixed, chip, 1%, 0.1W	270k
R49	Resistor, fixed, chip, 1%, 0.1W	1k
R50 & R51	Resistor, fixed, chip, 1%, 0.1W	10k
R52	Resistor, fixed, chip, 1%, 0.1W	5k6
R53	Resistor, fixed, chip, 5%, 0.25W	3R3
R54	Resistor, fixed, chip, 1%, 0.1W	220k
R55	Resistor, fixed, chip, 1%, 0.1W	470R
R56	Resistor, fixed, chip, 1%, 0.1W	1k
R57 to R62	Resistor, fixed, chip, 1%, 0.1W	2k
R63	Resistor, fixed, chip, 1%, 0.1W	43k
R64	Resistor, fixed, chip, 1%, 0.1W	220k
R65	Resistor, fixed, chip, 1%, 0.1W	1k3
R66	Resistor, fixed, chip, 1%, 0.1W	2k
R67	Resistor, fixed, chip, 2%, 0.1W	82R
R68	Resistor, fixed, chip, 1%, 0.1W	2k2
R69	Resistor, fixed, chip, 2%, 0.1W	39R
R70	Resistor, fixed, chip, 1%, 0.1W	1k
R71	Resistor, fixed, chip	0R
R72	Resistor, fixed, chip, 1%, 0.1W	1k3
R73	Resistor, fixed, chip, 2%, 0.1W	43R
R74	Resistor, fixed, chip, 1%, 0.1W	2k
R75	Resistor, fixed, chip, 2%, 0.1W	82R
R76	Resistor, fixed, chip, 1%, 0.1W	2k2
R77	Resistor, fixed, chip, 2%, 0.1W	39R
R78	Resistor, fixed, chip, 1%, 0.1W	2k4
R79	Resistor, fixed, chip, 2%, 0.1W	22R
R80	Resistor, fixed, chip, 1%, 0.1W	3k3

Circuit Reference	Description	Value
R81	Resistor, fixed, chip, 1%, 0.1W	130R
R82	Resistor, fixed, chip, 1%, 0.1W	2k4
R83	Resistor, fixed, chip, 2%, 0.1W	22R
R84	Resistor, fixed, chip, 1%, 0.1W	3k3
R85	Resistor, fixed, chip, 1%, 0.1W	130R
R86	Resistor, fixed, chip, 1%, 0.1W	3k9
R87	Resistor, fixed, chip, 1%, 0.1W	270R
R88 & R89	Resistor, fixed, chip, 1%, 0.1W	100k
R90	Resistor, fixed, chip, 2%, 0.1W	43R
R91	Resistor, fixed, chip, 1%, 0.1W	220k
R95	Resistor, fixed, chip, 1%, 0.1W	1k
R96	Resistor, fixed, chip, 1%, 0.1W	5k6
R97	Resistor, fixed, chip, 1%, 0.1W	5k1
R98	Resistor, fixed, chip, 1%, 0.1W	36k
R99	Resistor, fixed, chip, 1%, 0.1W	5k6
R100	Resistor, fixed, chip, 1%, 0.1W	30k
R101	Resistor, fixed, chip, 1%, 0.1W	5k6
R102 & R103	Resistor, fixed, chip, 1%, 0.1W	300R
R104	Resistor, fixed, chip, 1%, 0.1W	5k6
R105	Resistor, fixed, chip, 1%, 0.1W	5k1
R106	Resistor, fixed, chip, 1%, 0.1W	36k
R107	Resistor, fixed, chip, 1%, 0.1W	5k6
R108	Resistor, fixed, chip, 1%, 0.1W	30k
R109	Resistor, fixed, chip, 1%, 0.1W	5k6
R110 & R111	Resistor, fixed, chip, 1%, 0.1W	300R
R112 & R113	Resistor, fixed, chip, 1%, 0.1W	1k
R114	Resistor, fixed, chip, 1%, 0.1W	1M
R115	Resistor, fixed, chip, 1%, 0.1W	100k
R116	Resistor, fixed, chip, 1%, 0.1W	130R
R117	Resistor, fixed, chip, 2%, 0.1W	82R
R118 & R119	Resistor, fixed, chip, 1%, 0.1W	1k
R120 & R121	Resistor, fixed, chip, 1%, 0.1W	100k
R122 to R130	Resistor, fixed, chip, 1%, 0.1W	1k

Circuit Reference	Description	Value
R131	Resistor, fixed, chip, 2%, 0.1W	100R
R132 & R133	Resistor, fixed, chip, 1%, 0.1W	470R
R134 to R141	Resistor, fixed, chip, 1%, 0.1W	1k
R200	Resistor, fixed, chip, 1%, 0.1W	1k
R201 & R202	Resistor, fixed, chip, 1%, 0.1W	2k
R300 & R301	Resistor, fixed, chip, 1%, 0.1W	47k
R302 & R303	Resistor, fixed, chip, 1%, 0.1W	220k
R310 to R325	Resistor, fixed, chip, 2%, 0.1W	10R
R330	Resistor, fixed, chip, 2%, 0.1W	100R
R400	Resistor, fixed, chip,	0R
RV1 & RV2	Resistor variable, multiturn, 10%, 0.25W	10k
RV3 & RV4	Resistor variable, single turn, 20%, 0.5W	10k
X1	Resitor network, 2%, 1.125W	100k
D1	Diode, general purpose, IN916	
D2	Diode, IN4148	
TR1	Transistor, ZTX109L	
L1 & L2	Inductor, fixed, chip, 10%	4µ7
L3	Inductor, fixed, chip, 20%	470n
L4	Inductor, fixed, chip, 10%	4µ7
L5	Inductor, fixed, chip, 10%	5µ6

DAC/Sequencer Board Items List - Sheet 6 of 6

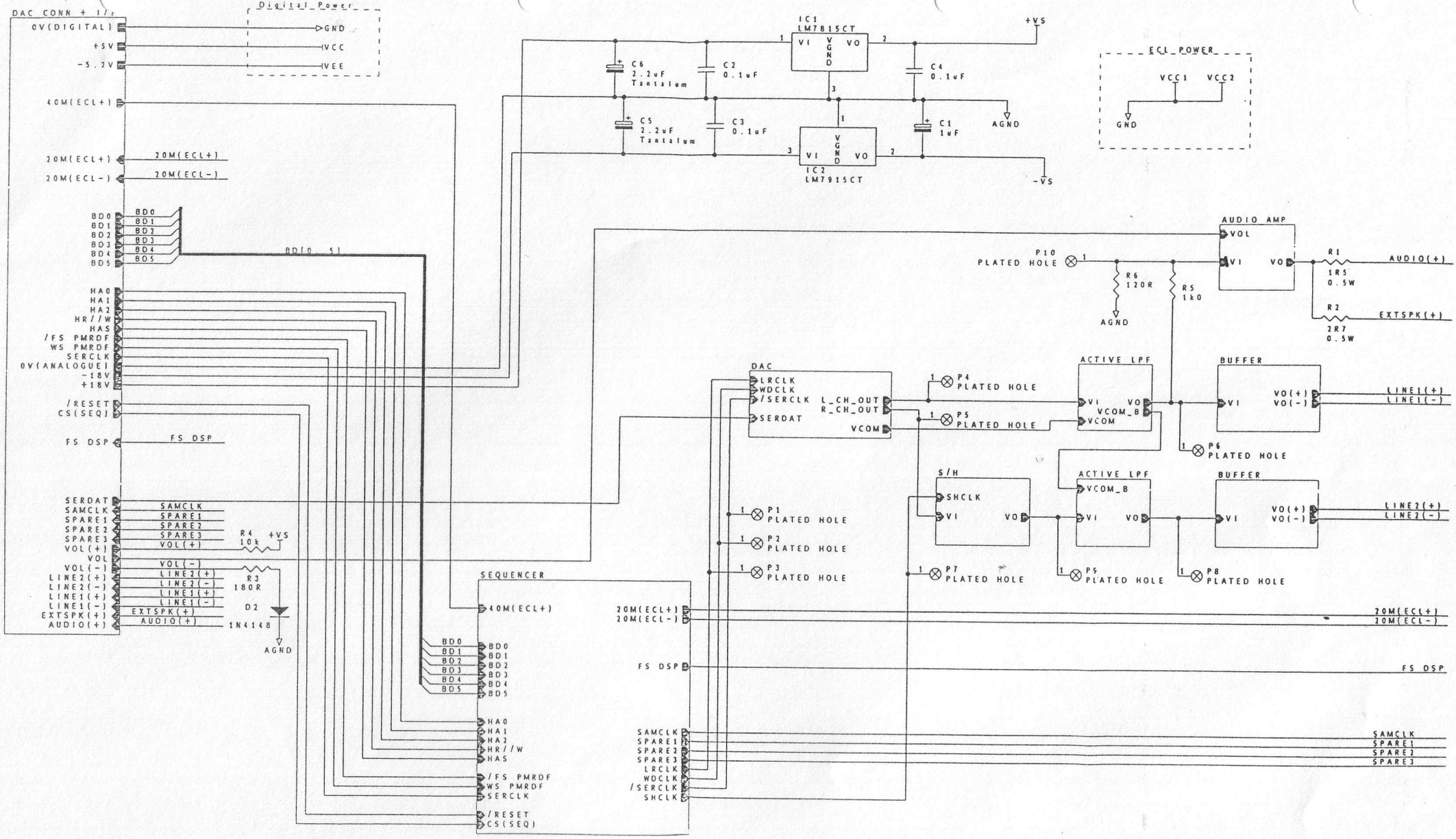


Figure 4 - DAC/Sequencer Module Interconnection Diagram

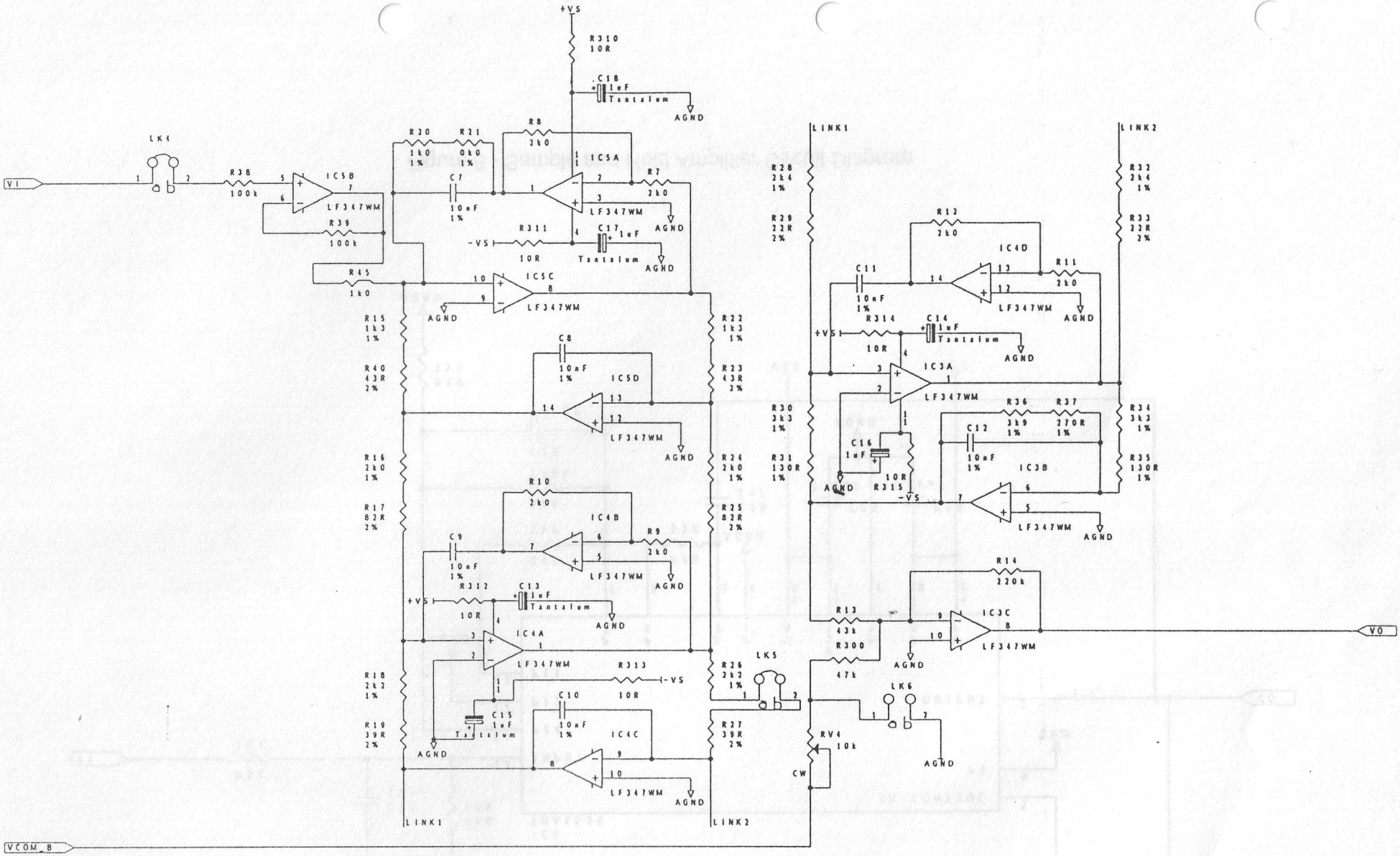


Figure 5 - Line2 Active LPF Circuit Diagram

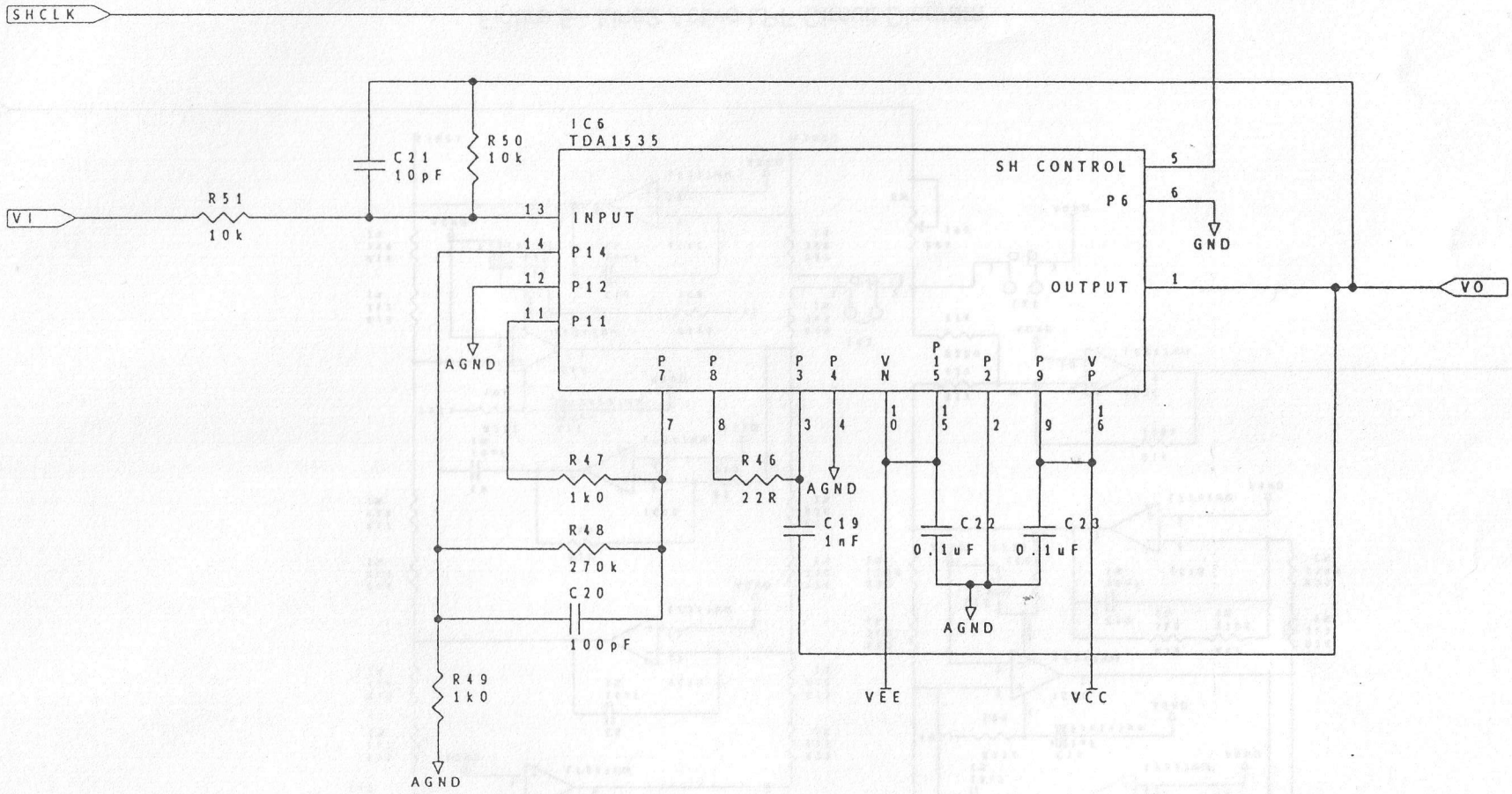


Figure 6 - Sample and Hold Amplifier Circuit Diagram

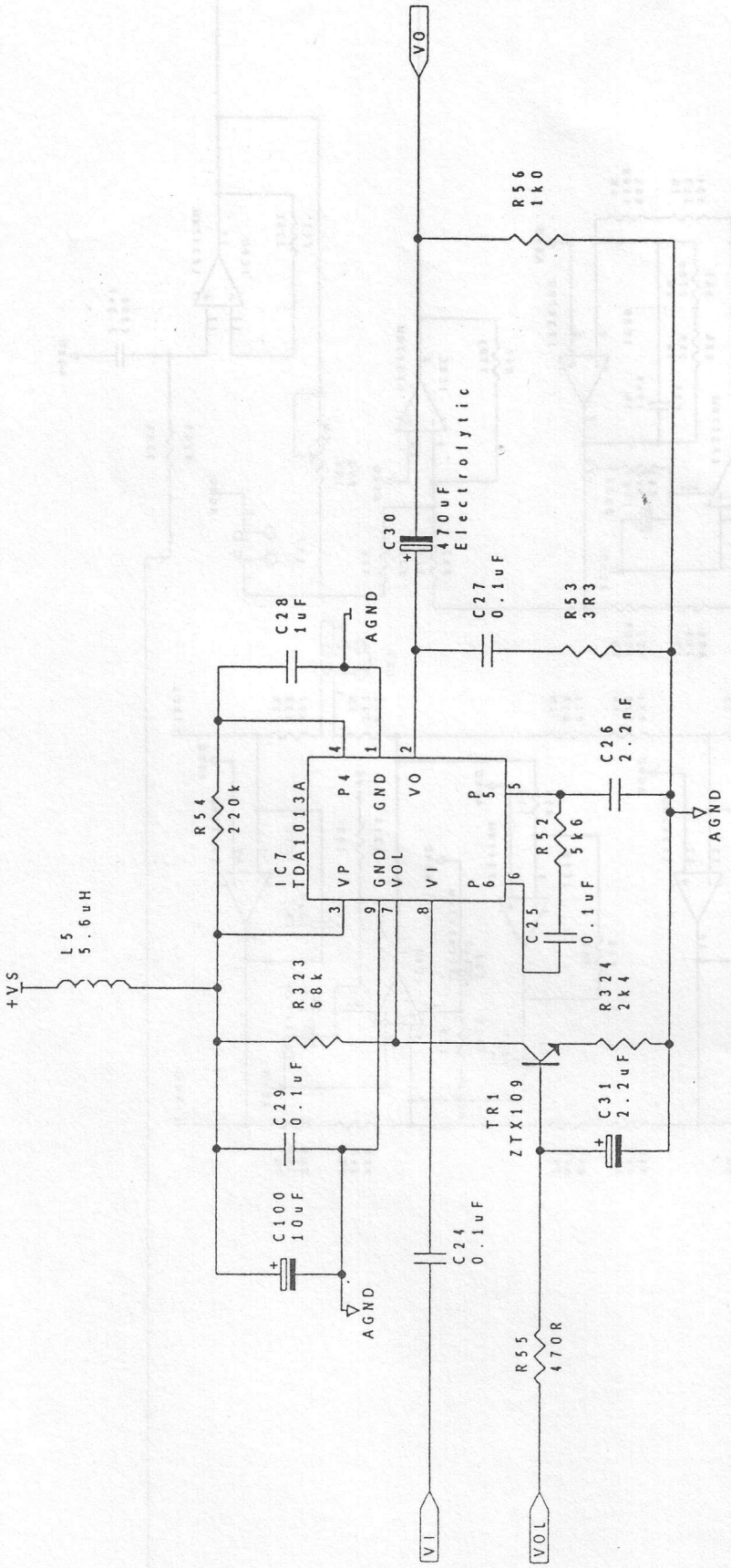


Figure 7 - Audio Amplifier Circuit Diagram

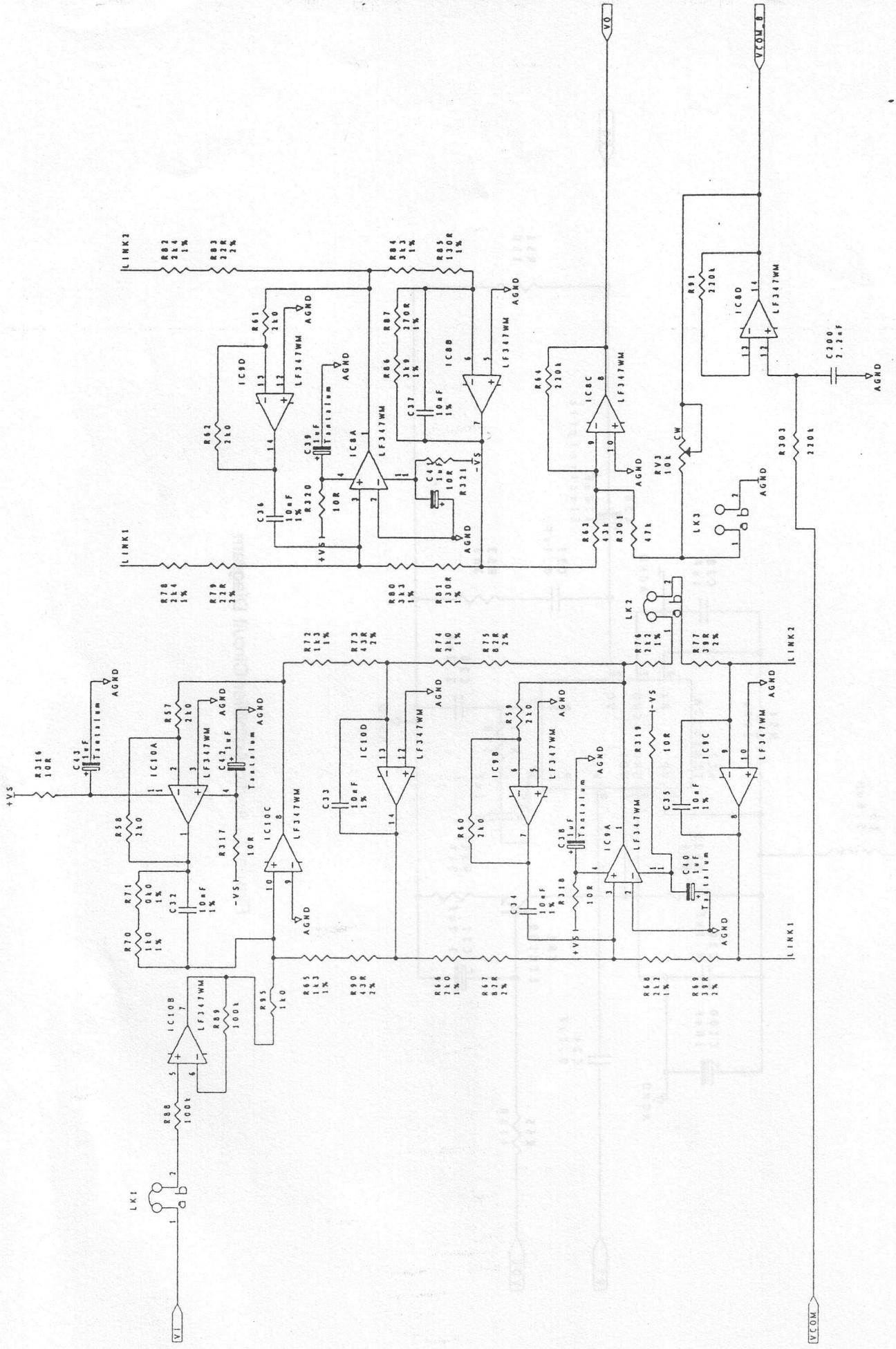


Figure 8 - Line1 Active LPF Circuit Diagram

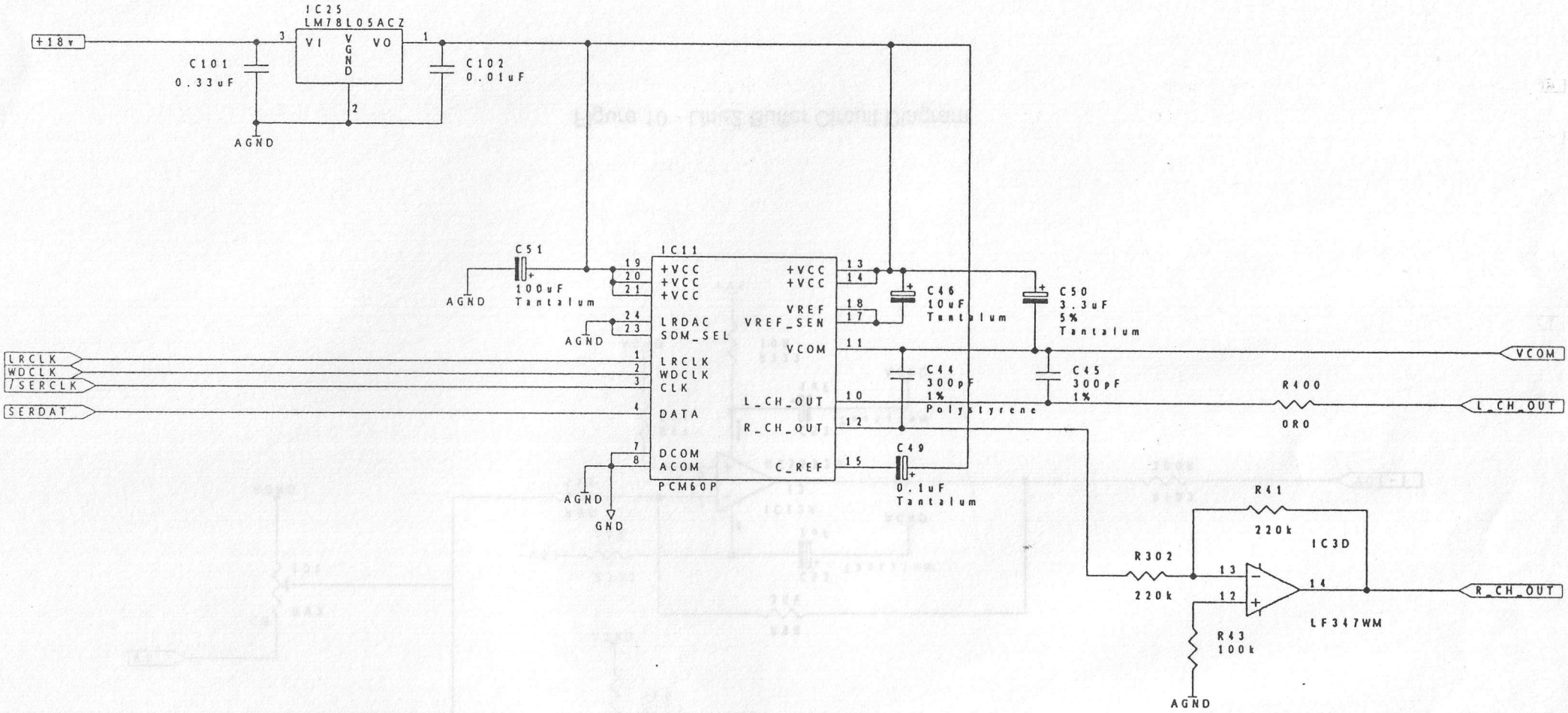


Figure 9 - Digital to Analogue Converter (DAC) Circuit Diagram

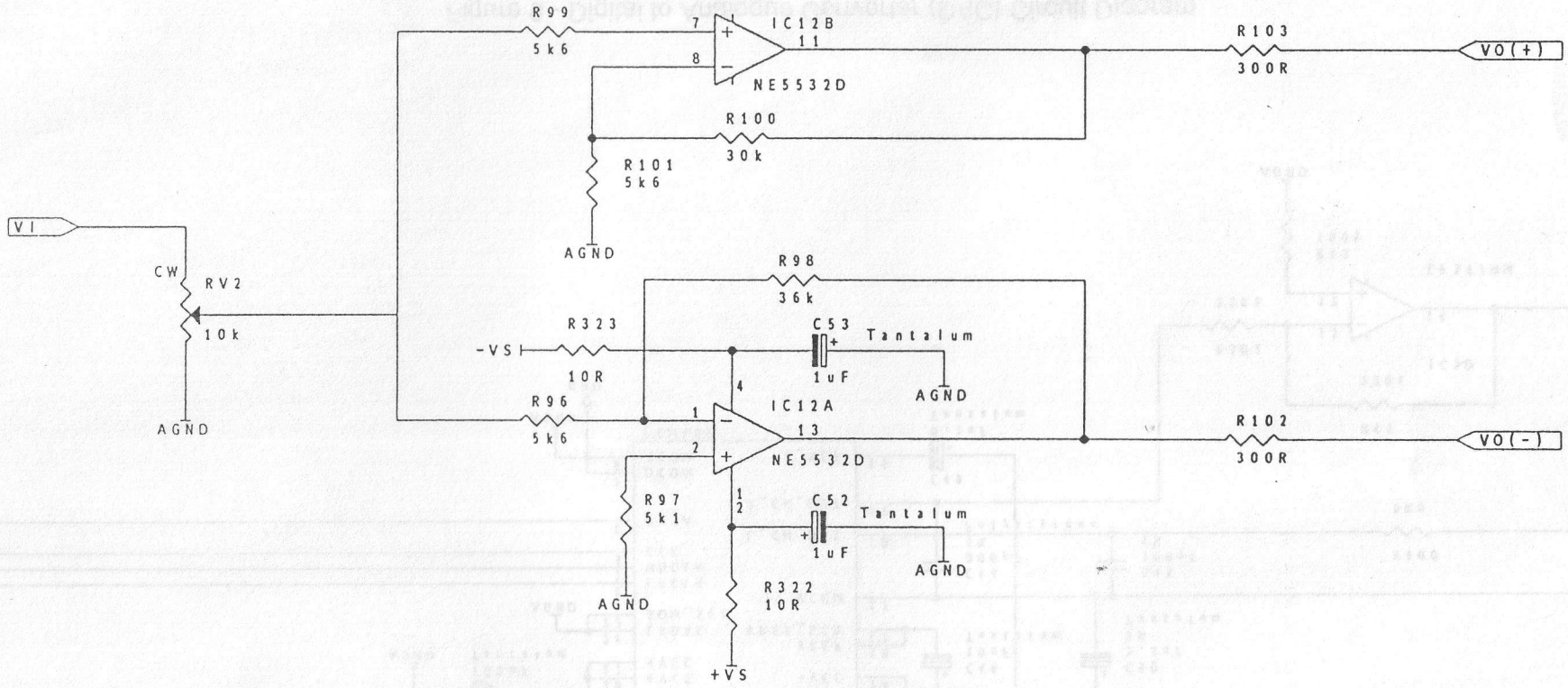


Figure 10 - Line2 Buffer Circuit Diagram

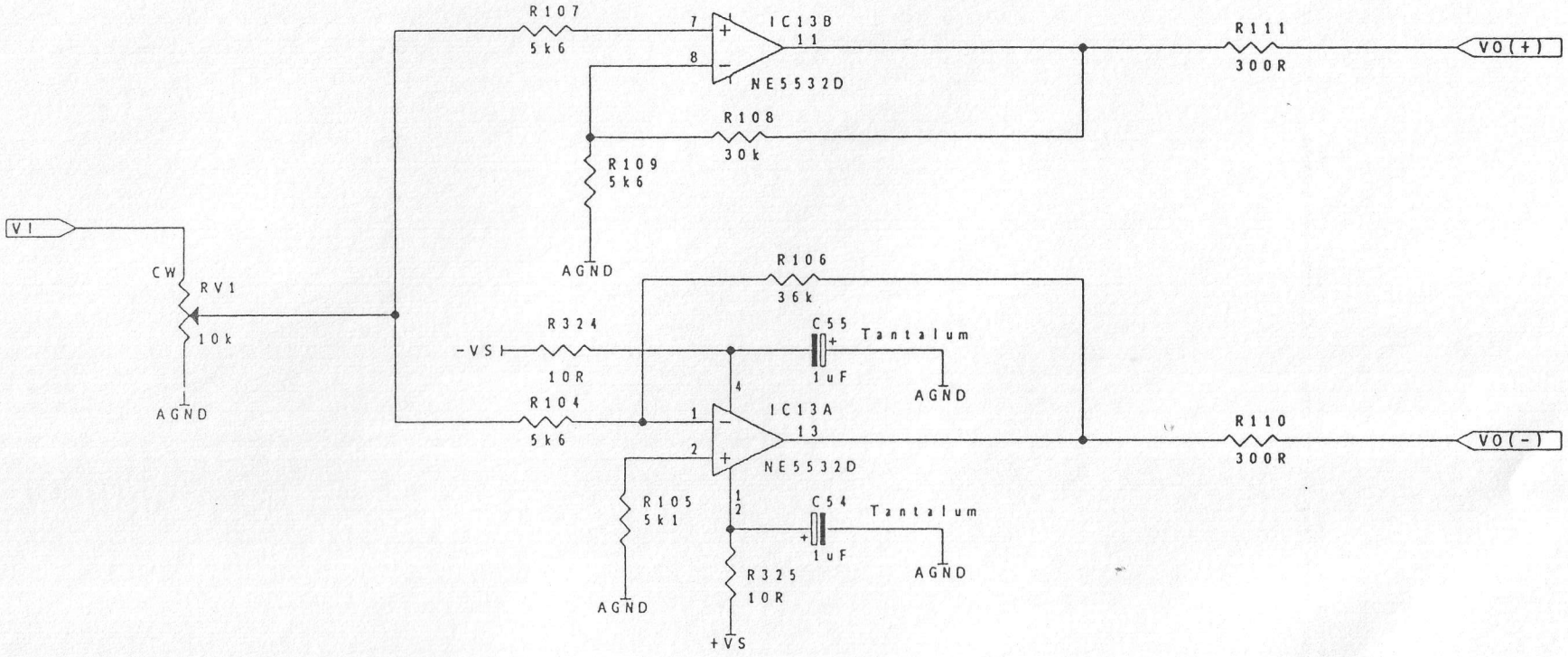


Figure 11 - Line1 Buffer Circuit Diagram

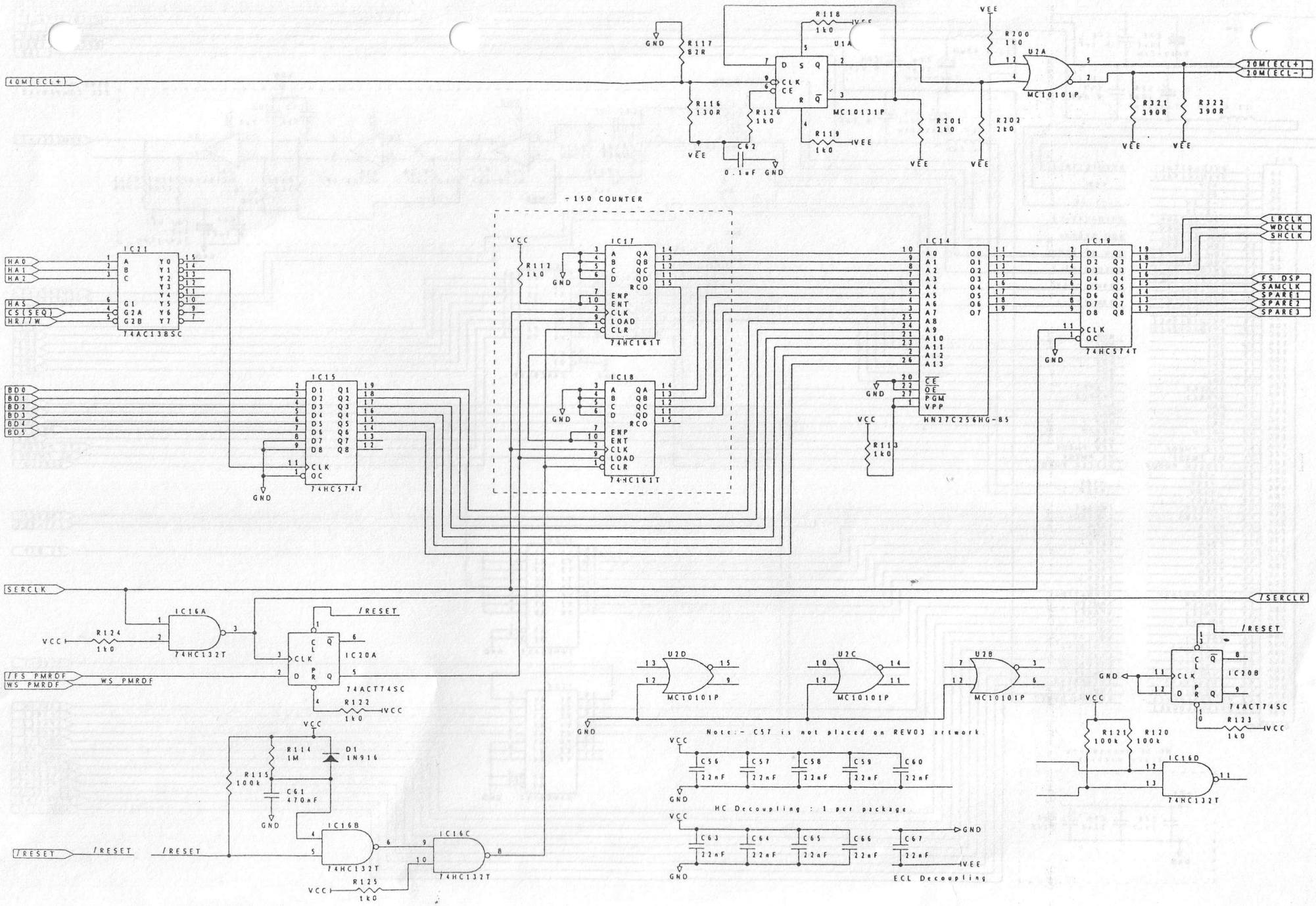


Figure 12 - Sequencer Circuit Diagram

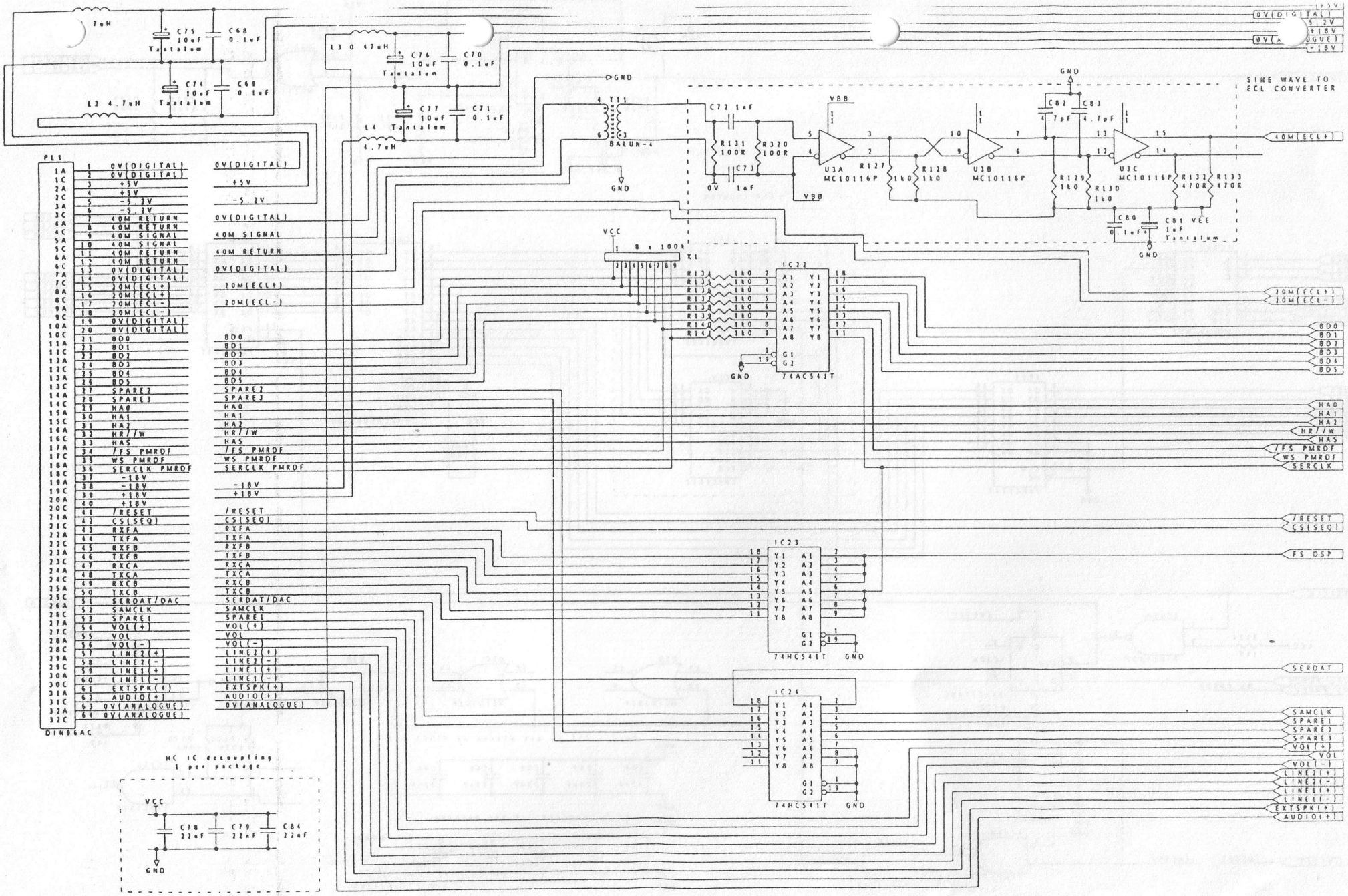


Figure 13 - DAC Connector Circuit Diagram

Chapter 6.12

FRONT PANEL ASSEMBLY

1 INTRODUCTION

The Front Panel Assembly is a complete interchangeable assembly which houses the Display Driver Board Assembly 52UPB504077 and the Keyboard Assembly 52UPB504078. Also mounted on the front panel are the speaker assembly, gain/squelch control, volume control, headphone socket, speaker switch, tuning control and the mains ON/OFF switch.

The Front Panel description is given with reference to the following drawings/illustrations and items list:

- Figure 1 STR8212 Front Panel Block Diagram
- Figure 2 LCD 1 Segment Map and Pin Functions
- Figure 3 LCD 2 Segment Map and Pin Functions
- Figure 4 STR8212 Front Panel General Assembly Drawing
- Figure 5 Display Driver Board Component Layout Diagram
- Figure 6 Keyboard Assembly Component Layout Diagram
- Items List Display Driver Board, Sheet 1 of 1
- Items List Keyboard Assembly, Sheet 1 of 1
- Figure 7 Display Driver Board Circuit Diagram
- Figure 8 Keyboard Circuit Diagram

The Front Panel Interconnection Diagram is included in Chapter 6.13, Chassis and Power Supplies.

2 GENERAL DESCRIPTION

The Front Panel Assembly provides the man-machine interface for the radio, it houses all of the radio's controls and displays. Mounted on the Front Panel are the Keyboard and Display printed circuit boards (PCBs). Each of these PCBs is connected to the radio's Digital Backplane by a ribbon cable. Discrete wires link the panel mounted controls to the Keyboard PCB, these are linked through the PCB to the Digital Backplane. The connections from the Front Panel to the main radio chassis are as follows:

- Ribbon cable from the Display PCB to PL16 on the Digital Backplane.
- Ribbon cable from the Keyboard PCB to PL15 on the Digital Backplane.
- Mains cable from front panel Mains Switch via in-line connector PL50/SKT50 to mains connector on the rear panel of the radio.
- Earth bonding wire from a stud on the Front Panel to a stud on the radio chassis.

2.1 Keyboard PCB

All of the front panel keys, with the exception of the Speaker key, are mounted on the Keyboard PCB. Light Emitting Diodes (LEDs) are mounted in some of the key housings, these LEDs give a visual indication of the radio's current settings. The LEDs are driven via a shift register on the Display PCB. The radio's Controller accesses this register via Serial Interface F from the Controller Interface. Chapter 6.16, covering the radio's internal interfaces, gives the

bit allocations for Serial Interface F. The key contacts are connected in a row/column matrix, this matrix is scanned by the Controller Interface board. Each of the 4 'KX' lines are marked in turn, the state of the 'KY' lines are read back. See Figure 1 for a block diagram of the Keyboard PCB.

2.2 Display PCB

Housed on the Display PCB are two custom Liquid Crystal Display (LCD) panels. Viewing from the front of the radio the left-hand one is LCD1, LCD2 is on the right. Figures 2 and 3 give the segment layout and pin function for each of these LCD panels. A backlight diffuser is fitted beneath the two LCDs. A black foam strip is fitted around both LCDs to avoid the ingress of dust into the void between the front surface of the LCDs and the front panel display window. Six small filament bulbs provide the light for the backlight, these bulbs are continuously lit while the radio is powered. The two LCDs are driven by three uPD7225 LCD driver chips, IC1, 2 & 3.

LCD1 is driven by IC1 and IC2. LCD2 is driven by IC3. All three chips share a common 8 bit serial data line (LCD DATA) and data clock line (LCD CLOCK). Each LCD driver has its own chip select line (LCD CS1...3), this line is taken low to address each chip. 'LCD C//D' indicates whether the serial word is aimed at the driver's Command or Data Register. The '/BUSY' line is taken low by any of the drivers when they are not ready to receive new commands or data.

IC4A divides the clock signal for the drivers by 2. The incoming clock frequency, at the input of IC4A, is 250 kHz. The circuit formed by IC5, IC4B, IC6A and IC6B conditions the '/RESET' signal applied to the drivers, the reset pulse is constrained to be not less than 16 driver clock periods long.

2.3 Panel Mounted Components

The radio's Tuning Knob is connected to a shaft encoder. This produces pulses on its output lines as the knob is rotated. The encoder's two output lines are in quadrature, they are decoded partly on the Controller Interface and partly by the Controller software, to yield direction, speed and angle of rotation data.

The radio's Gain/Squelch Control has a 20 kohm, 360 degree potentiometer without end stops. The dc voltage on the wiper is read by an ADC on the Controller Interface board. To reduce noise pickup in the signal lines the ADC's differential input is utilised.

The Volume Control uses a 1 kohm, 270 degree single turn potentiometer to supply the dc control voltage to the audio amplifier on the DAC/AUDIO/SEQUENCER board.

The speaker is mounted on a horn assembly that minimises the area of front panel occupied by the speaker aperture. The speaker switch allows the speaker to be disabled, this switch is provided with an LED which is lit when the speaker is enabled. The phones socket accepts a 2 pole standard (6.3mm) jack plug. The internal speaker is disabled when the phone jack is inserted.

3 ALIGNMENT AND DIAGNOSTIC NOTES

There are no electrical alignment operations required on this assembly.

SAFETY WARNING

After replacing, or working on, a front Panel Assembly, the operator must ensure that the Earth Bonding Wire between the Front Panel and Radio Chassis is re-connected before the radio is connected to the Mains supply.

Refer to Chapter 5 for Front Panel removal instructions.

It is unlikely that all three LCD drivers would fail simultaneously, a complete functional failure of both LCD1 and LCD2 points to a Controller or Controller Interface fault. However, since LCD1 is controlled by two driver chips, a partial failure of LCD1 points to a driver fault. Similarly, if LCD1 functions correctly but LCD2 doesn't a LCD driver fault is indicated.

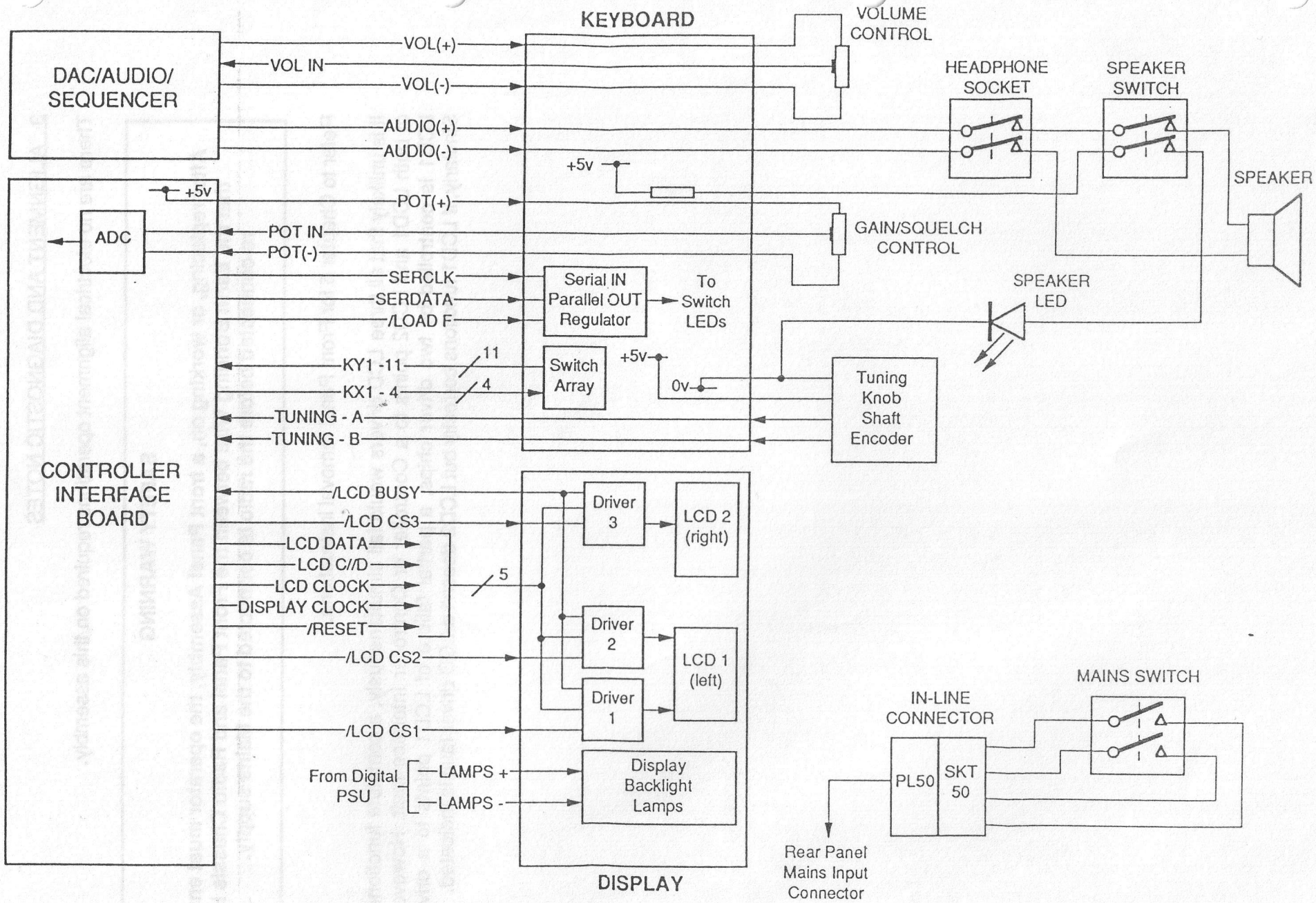
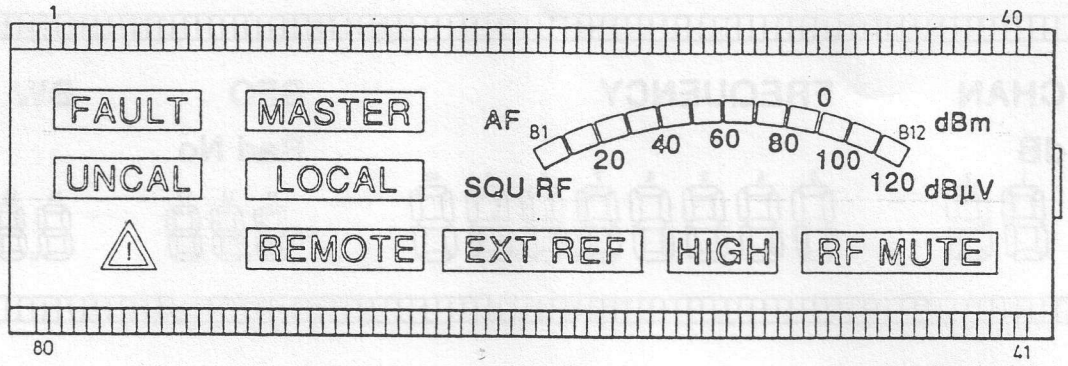
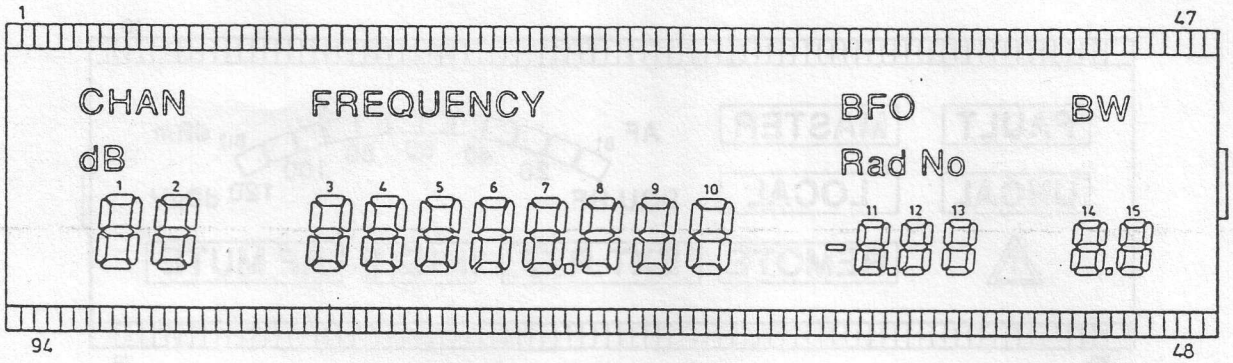


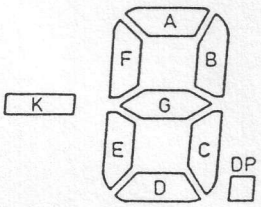
Figure 1 - STR8212 Front Panel Block Diagram



CONNECTION DETAILS																				
PIN NUMBER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
BACKPLANE 1	BP1	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c
BACKPLANE 2	-	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c
PIN NUMBER	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
BACKPLANE 1	B1	B2	B3	B4	B5	n/c	B6	B7	B8	B9	n/c	0	B10	B11	B12	n/c	dBm	n/c	n/c	BP1
BACKPLANE 2	-	-	-	-	-	n/c	-	-	-	-	n/c	-	-	-	-	n/c	-	n/c	n/c	-
PIN NUMBER	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
BACKPLANE 1	-	n/c	-	n/c	n/c	n/c	n/c	n/c	-	n/c	n/c	-	n/c	n/c	-	-	-	n/c	n/c	n/c
BACKPLANE 2	BP2	n/c	dBµV 100,200	n/c	n/c	n/c	n/c	n/c	RF MUTE	n/c	n/c	HIGH	n/c	n/c	20,40, 60,80	RF	EXT RF	n/c	n/c	n/c
PIN NUMBER	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
BACKPLANE 1	n/c	n/c	n/c	-	-	n/c	n/c	n/c	n/c	-	n/c	n/c	-	-	-	n/c	-	-	n/c	-
BACKPLANE 2	n/c	n/c	n/c	SQU	AF	n/c	n/c	n/c	n/c	REMOTE	n/c	n/c	LOCAL	MAST.	UNCAL	n/c	⚠	FAULT	n/c	BP2
n/c = no connection																				

Figure 3 - LCD 2 Segment Map and Pin Functions





CONNECTION DETAILS																							
PIN NUMBER	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
BACKPLANE 1	BP1	1A	n/c	2A	n/c	n/c	n/c	3A	4A	5A	6A	7A	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c
BACKPLANE 2	-	dB	n/c	CHAN	n/c	n/c	n/c	-	-	-	-	FREQ	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c	n/c
PIN NUMBER	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
BACKPLANE 1	n/c	n/c	n/c	8A	9A	10A	11A	12A	n/c	n/c	n/c	n/c	n/c	13A	14F	14A	14B	15F	n/c	n/c	15A	15B	-	-
BACKPLANE 2	n/c	n/c	n/c	-	-	-	-	Rad No	n/c	n/c	n/c	n/c	n/c	BFO	14E	-	14C	15E	n/c	n/c	BW	15C	BP2	BP2
PIN NUMBER	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72
BACKPLANE 1	15G	-	14G	13B	13G	13F	12B	12G	12F	-	11B	11G	11F	-	10B	10G	10F	9B	9G	9F	8B	8G	8F	-
BACKPLANE 2	15D	DP14	14D	13C	13D	13E	12C	12D	12E	DP11	11C	11D	11E	K	10C	10D	10E	9C	9D	9E	8C	8D	8E	DP7
PIN NUMBER	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94		
BACKPLANE 1	7B	7G	7F	6B	6G	6F	5B	5G	5F	4B	4G	4F	3B	3G	3F	2B	2G	2F	1B	1G	1F	BP1		
BACKPLANE 2	7C	7D	7E	6C	6D	6E	5C	5D	5E	4C	4D	4E	3C	3D	3E	2C	2D	2E	1C	1D	1E	-		
n/c = no connection																								

Figure 2 - LCD 1 Segment Map and Pin Functions

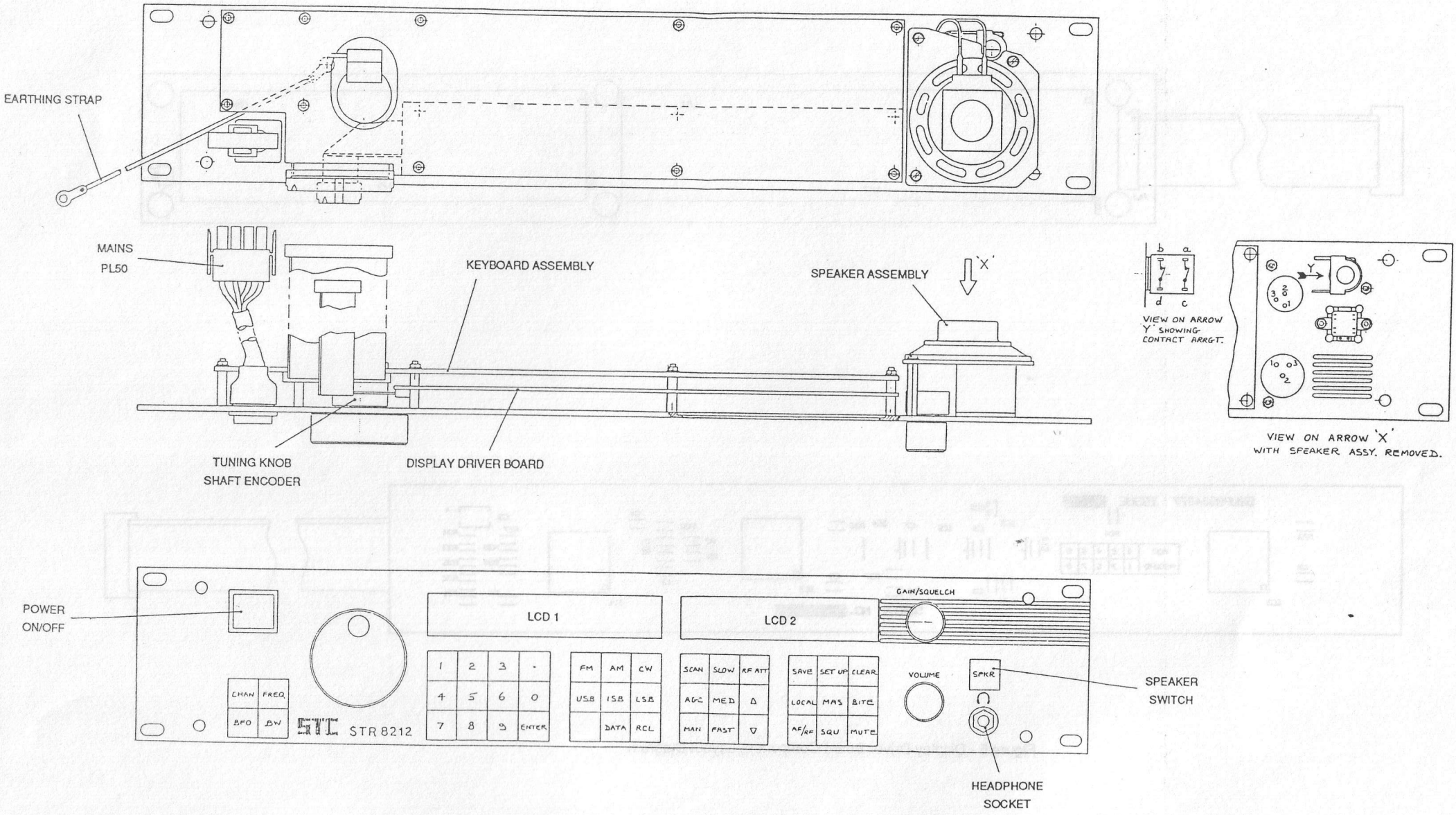


Figure 4 - STR8212 Front Panel General Assembly Drawing

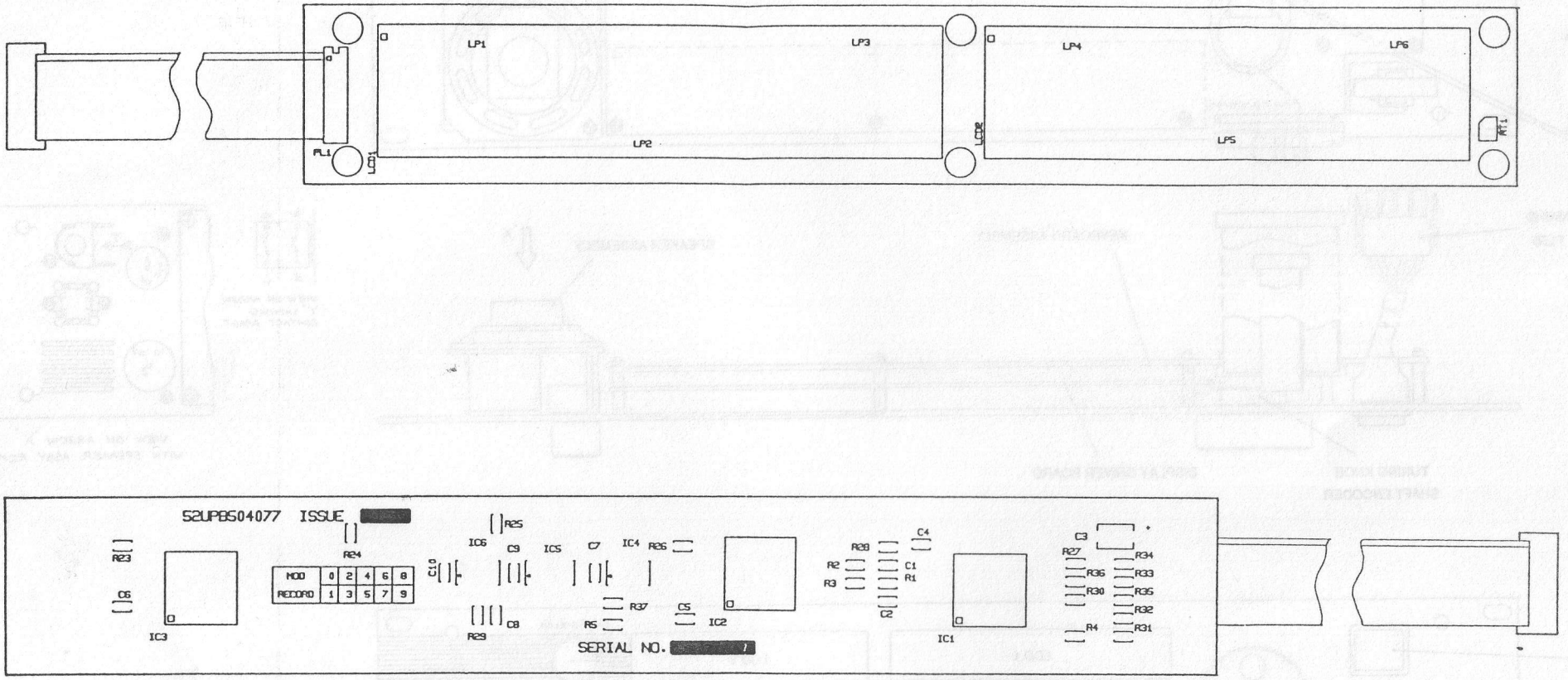


Figure 5 - Display Driver Board Component Layout Diagram

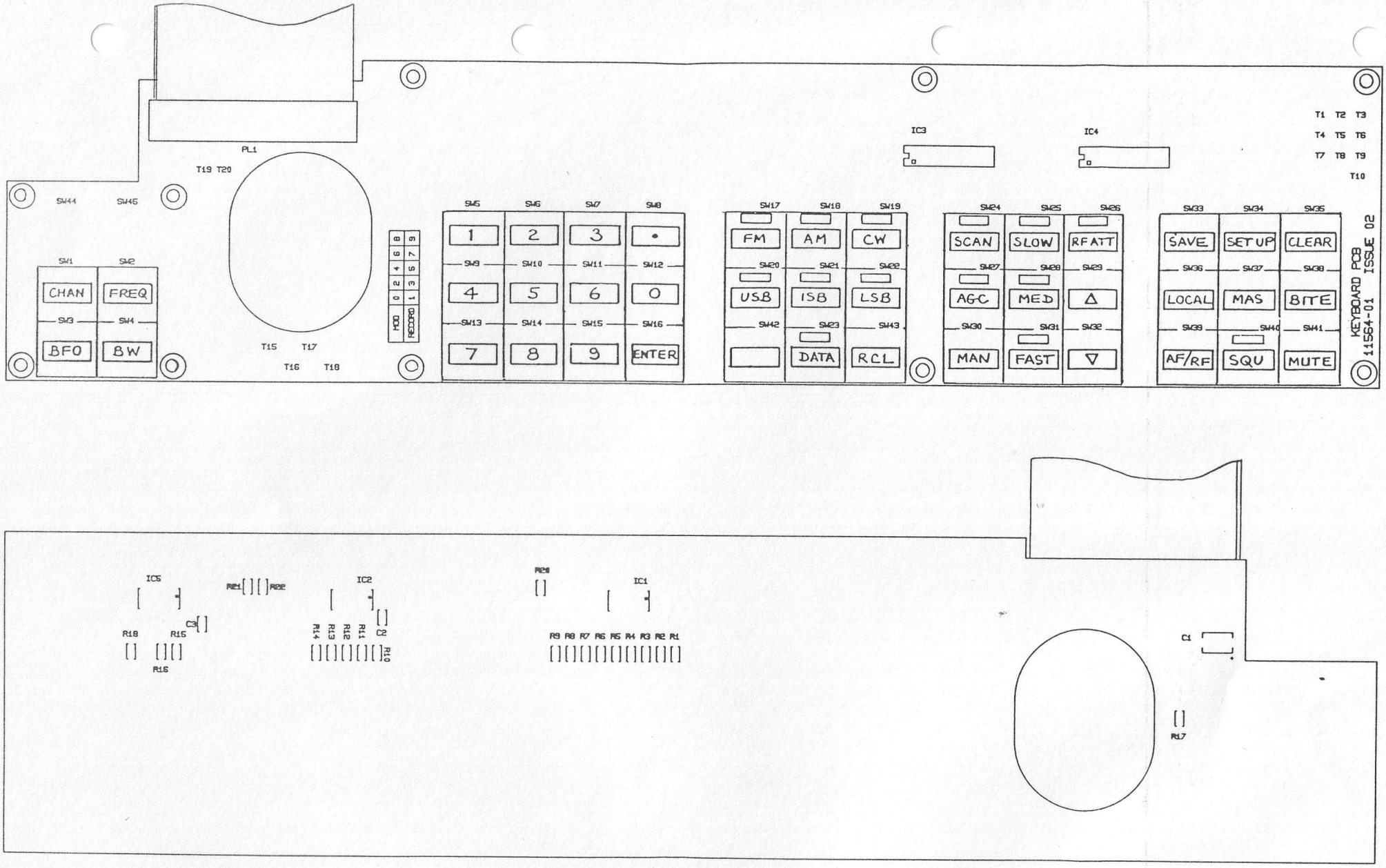


Figure 6 - Keyboard Assembly Component Layout Diagram

Circuit Reference	Description	Value
C1 & C2	Capacitor, fixed, ceramic chip, 10%, 100V	1n
C3	Capacitor, solid tant chip, 10%, 100V	10µ
C4 to C7	Capacitor, fixed, ceramic chip, 10%, 100V	22n
C8	Capacitor, fixed, ceramic chip, 5%, 100V	150p
C9 & C10	Capacitor, fixed, ceramic chip, 10%, 100V	22n
IC1 to IC3	7/14 Segment LCD Controller	
IC4	Dual D-type Flip Flop, MC74HC74AD	
IC5	4 Bit Synchronous Binary counter, PC74HC163T	
IC6	1 circuit Quad 2 Input Nand Gate, PC74HC00T	
R1 & R2	Resistor, fixed, chip, 5%, 0.25W	39k
R3	Resistor, fixed, chip, 5%, 0.25W	15k
R4	Resistor, fixed, chip, 5%, 0.25W	10k
R5	Resistor, fixed, chip, 5%, 0.25W	91k
R23 to R28	Resistor, fixed, chip, 5%, 0.25W	27R
R29	Resistor, fixed, chip, 5%, 0.25W	10k
R30 to R37	Resistor, fixed, chip, 5%, 0.25W	100k
D7 & D8	Diode, zener, BZX84C3V6	
D9 & D10	Diode, Double BAV99	
D11 & D12	Diode, zener, BZX84C3V6	
D13 & D14	Diode, Double BAV99	
TR3 to TR6	Transistor, NPN, BSV52	

Display Driver Board Items List - Sheet 1 of 1

Circuit Reference	Description	Value
C1	Capacitor, fixed, solid tant chip, 10%, 10V	10µ
C2 & C3	Capacitor, fixed, ceramic chip, 10%, 100V	22n
IC1 & IC2	High voltage, High current, Darlington Transistor Array	
IC3 & IC4	8 Bit Series to Parallel Shift Reg. MC74HC595AN	
IC5	High voltage, High current, Darlington Transistor Array	
R1 to R18	Resistor, fixed, chip, 5%, 0.25W	470R
R20 to R22	Resistor, fixed, chip, 5%, 0.25W	100k

Keyboard Board Assembly Items List - Sheet 1 of 1

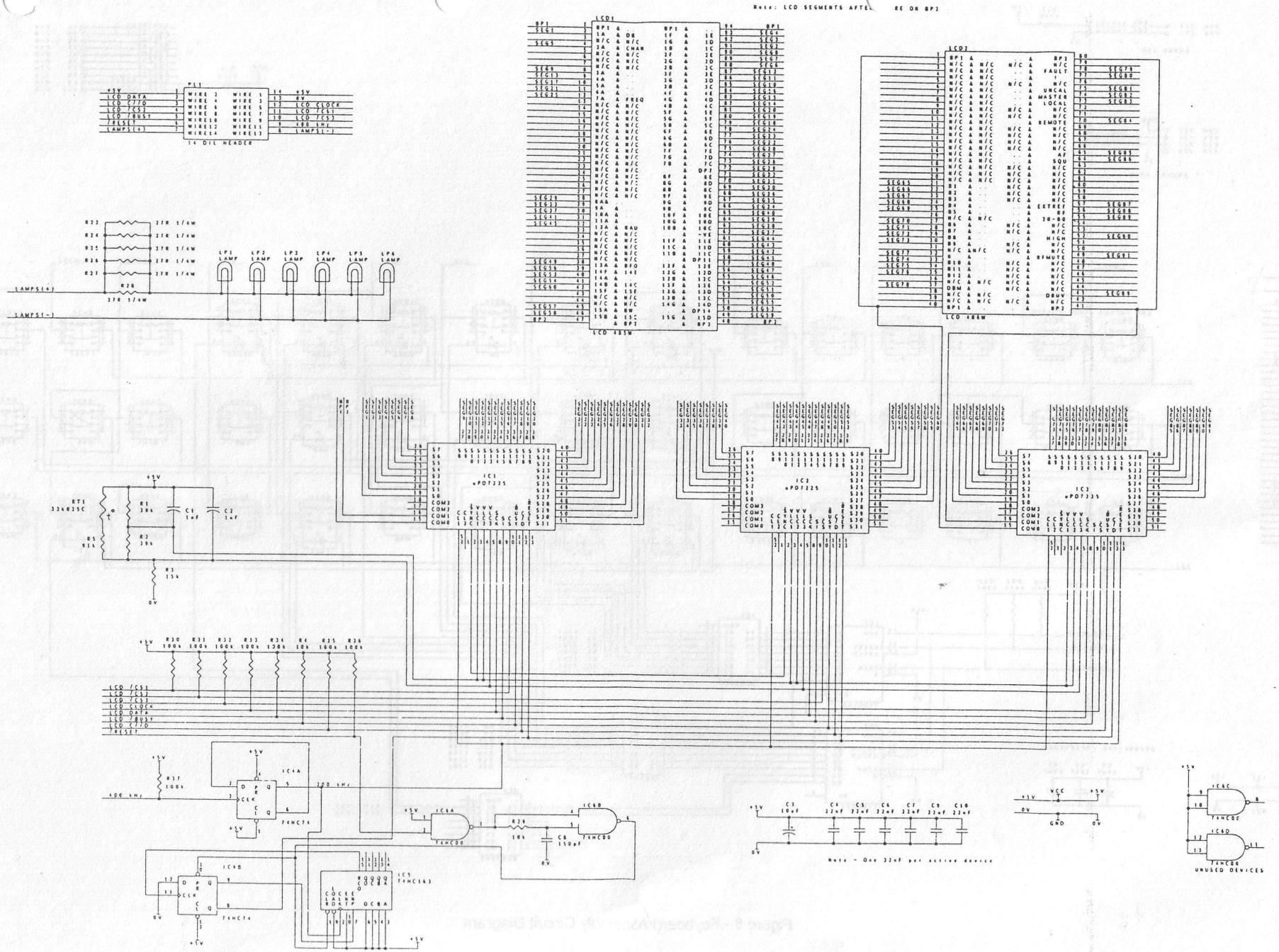


Figure 7 - Display Driver Board Circuit Diagram

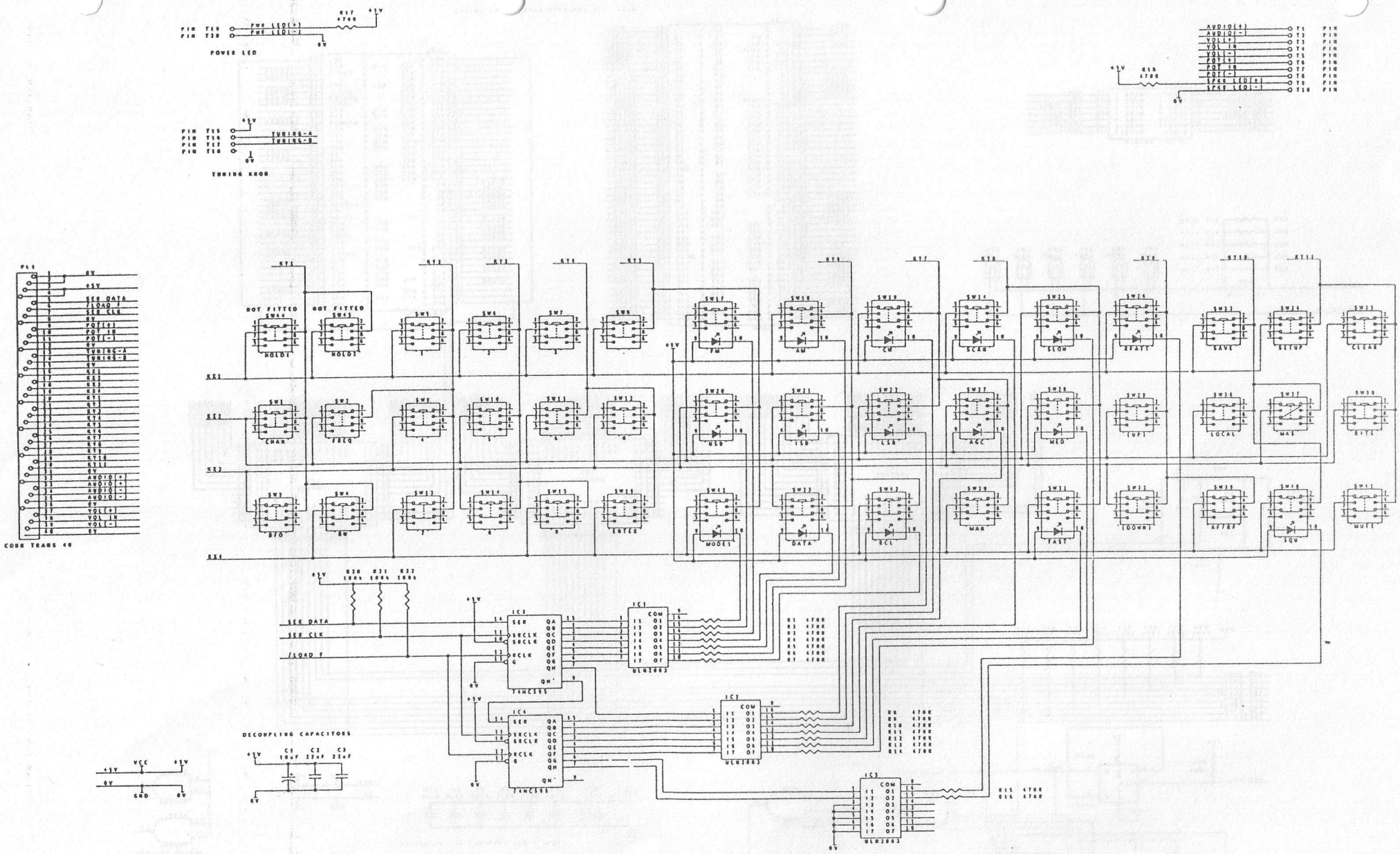


Figure 8 - Keyboard Assembly Circuit Diagram

Chapter 6.13

CHASSIS AND POWER SUPPLIES

1 INTRODUCTION

The STR8212 Receiver Chassis houses the Power Supply, the Front Panel Assembly, the Digital and RF Backplanes and Interconnection Wiring. Figure 1 shows a plan view of the receiver. The digital plug-in cards as well as the ADC module and the Interface Module plug-in into the Digital Backplane. Most of the digital cards (except the Controller Interface) plug-in by means of DIN 41612 connectors.

The RF Backplane carries the sockets for all the RF modules. Mixed connectors with standard and coax contacts are used. RF connections between the RF modules are made via coaxial connections which plug-in beneath the RF Backplane. The RF Backplane is connected to the interface module (which provides a filtering function) via a flexible printed circuit connection. The 50 kHz IF output from the IF module is connected to the ADC socket via hardwired coaxial cable. Connections from the Digital Backplane to the Rear Panel and Front Panel are made via ribbon cable. The Front Panel Assembly is described in Section 6.12.

The STR 8212 Power Supply converts power from the input 50/60 Hz ac supply to the dc supplies required for powering the various modules etc. in the receiver. It is of conventional type with mains transformer, bridge rectifiers, capacitor smoothing and linear series dc regulators.

- Figure 1 STR8212 Block Diagram
- Figure 2 Power Supply Simplified Block Diagram
- Figure 3 Analogue PSU 2 Layout Diagram
- Figure 4 Digital PSU 1A Layout Diagram
- Figure 5 Rectification and Smoothing Layout Diagram
- Figure 6 Chassis Assembly Drawing
- Figure 7 Digital Backplane Layout Diagram
- Figure 8 RF Backplane Layout Diagram
- Figure 9 Mains Power Section Interconnection Diagram
- Figure 10 Power Section Interconnection Diagram
- Figure 11 RF Backplane Interconnection Diagram
- Figure 12 Analog Section Interconnection Diagram
- Figure 13 Interface Section Interconnection Diagram
- Figure 14 Digital Section Interconnection Diagram
- Figure 15 Front Panel Interconnection to Digital Backplane
- Figure 16 Front Panel to Keyboard Interconnection Diagram
- Figure 17 Front Panel Interconnection Diagram
- Figure 18 Digital Backplane Interconnection Diagram
- Figure 19 RF Backplane Interconnection Diagram
- Items List Analogue PSU 2 Sheets 1 and 2
- Items List Digital PSU 1A Sheets 1 and 2
- Items List Rectification and Smoothing Sheet 1
- Items List Digital Backplane Sheet 1
- Items List RF Backplane Sheets 1 and 2
- Figure 20 Digital PSU 1A Circuit Diagram
- Figure 21 Analogue PSU Circuit Diagram
- Figure 22 Rectification and Smoothing Circuit Diagram

2 MODULE DESCRIPTION

The radio power supply consists mainly of four elements:

- The toroidal mains transformer with additional 5V smoothing capacitors.
- The rectification and smoothing PCB (PSU1)
- A digital supplies regulator PCB (PSU 1A) for the digital radio section
- An analogue supplies regulator PCB (PSU 2) for the RF radio section

Five separate outputs from the toroidal mains transformer are fed to bridge rectifiers (on PSU 1 board) to provide unregulated (raw) dc to the +18, +8, +5, -5.2 and -18 volt regulators. Separate regulators are used for the digital (PSU 1A) and analogue (PSU 2) sections of the receiver with the analogue regulators being mounted in the RF section and fed via filtercons in the wall. The digital (PSU 1A) plugs in directly into the horizontal rectifier and smoothing board (PSU 1).

The digital section uses four regulators for +18, +8, +5 and -18 volts and the analogue section uses six regulators for +20, +18, +18 low noise, +8, +5 and -18 low noise. Green LEDs are used to indicate the presence of line voltages from the regulators on both digital and analogue PCBs. Both PCBs have BITE circuits and provide both a BITE output and a fail indication (RED LED), if the outputs are out of limit.

The mains input is fed via a filtered IEX 320 connector unit which incorporates a fuse and voltage selector. The on/off switch is in the primary circuit of the transformers and is connected via an interface connector to enable easy removal of the front panel.

All voltage regulators are of the analogue type and are mainly of the three terminal-adjustable output type. BITE is built into PSU 1 and PSU 2 in the form of visible indication with a green LED per rail indicating that each rail is nominally providing the correct output level. A single red LED is provided for both the digital and the analogue PSU and monitors the voltage on each rail more accurately. Any rail which is out of tolerance will result in the LED illuminating.

In addition, both the analogue and digital PCB BITE fault signals are output from the Digital (PSU 1A) PCB and to the radio BITE controller.

3 CIRCUIT DESCRIPTION

Circuit description is given under the following headings:

- Mains Transformer . . . . . Paragraph 3.1
- Rectification and Smoothing PCB (PSU 1) . . . . . Paragraph 3.2
- Digital (PSU 1A) . . . . . Paragraph 3.3
- Analogue (PSU 2) . . . . . Paragraph 3.4
- Fans . . . . . Paragraph 3.5

3.1 Mains Transformer

The mains transformer is a low radiation toroidal transformer and contains a built-in thermostatic cut out in series with the primary winding. The primary has three tappings which are switch selectable via the voltage selector on the mains input unit of the back panel. The input power supply requirements are:

- 240V ± 10% at 47 to 63 Hz
- 220V ± 10% at 47 to 63 Hz
- 110V ± 10% at 47 to 63 Hz

There are five secondary windings which plug into the rectification and smoothing PCB via a connector, PL10.

3.2 Rectification and Smoothing PCB (PSU 1)

A rectification and smoothing PCB (PSU 1), rectifies and smooths the transformer secondaries before entering the digital regulator PCB (PSU 1A). Note that two additional capacitors C1 and C2 are strapped to the toroidal transformer and are coupled directly to the +5V rectification/smoothing circuit.

3.3 Digital (PSU 1A) PCB

Digital (PSU 1A) PCB derives its raw inputs supplies from the rectification and smoothing PCB (PSU1) via a 20 way header (Header 2). The raw input supplies are utilised by the digital regulators as well as being output via an 8 way header (Header 1) to feed through filters in the dividing panel and to the analogue regulators of PSU 2. The four regulators are very basic three-terminal regulators. A crude BITE indication is formed by zener diodes and green LEDs to indicate the availability of each supply output. A tighter sense of upper and lower voltage tolerances is handled by IC3 and IC4 which both contain window comparators to output a common fault signal into a red LED on the PCB as well as into a buffer, U1A and U1B, for BITE flag output to the radio BITE controller.

3.4 Analogue (PSU 2) PCB

Analogue (PSU 2) PCB derives its raw input supplies from the digital (PSU 1A) through-link from the rectification and smoothing PCB (PSU 1). Four of the regulators are basic three terminal type with two others utilising a UA723 chip to provide +18V (low noise) and -18V supplies. A crude BITE indication is provided by zener diodes and green LEDs to indicate the availability of each supply output. A tighter sense of the upper and lower voltage tolerances is handled by IC3 and IC4 which both contain window comparators to output a common fault signal into a red LED on the PCB as well as into a buffer, U1D and U1C, located on the digital supply board (PSU 1A), for BITE flag output to the radio BITE controller.

3.5 Fans

The fans are powered by the unregulated +5V supply. Connections for Fan 1 (which cools the digital side of the radio) are provided by a connection from the rectifier and smoothing board. Connections for Fan 2 are routed through digital power supply board and through the filter connections in the wall of the RF compartment.

4 ADJUSTMENTS

There are no adjustments within any of the PSU modules, all voltages being set by fixed resistor networks.

5 FAULT FINDING

The front panel BITE 10-FAIL1 and -or 10 -FAIL 2 should be the first indication of faults. If this is so, then a look at the red and green LEDs should narrow the fault down to specific voltages. Before removing the PSU modules for inspection, it is advisable to, one by one, remove the digital section and RF section modules, ensuring that the mains has been switched off prior to doing so. Bench fault finding can take place with the digital and analogue supply, provided appropriate dc supplies can be fed into the PSU modules, bearing in mind that the input voltages to the regulators need to be approximately 3.5V higher than the expected regulated output.

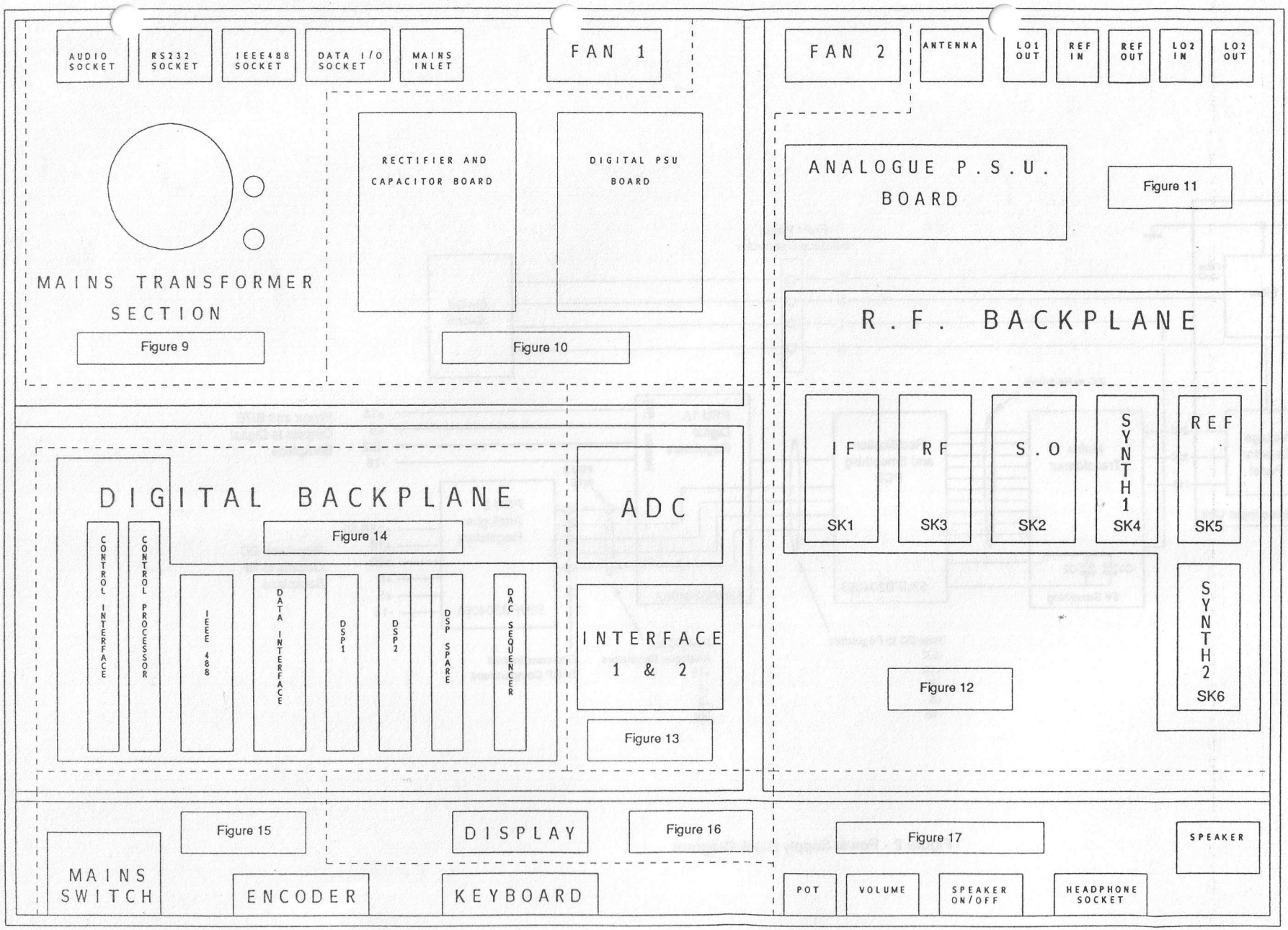


Figure 1 - STR8212 Block Diagram

NOTE:

DETAILED INTERCONNECTIONS ARE SHOWN IN THE DRAWINGS INDICATED WITHIN THE AREAS ENCLOSED BY THE THE DASHED LINES.

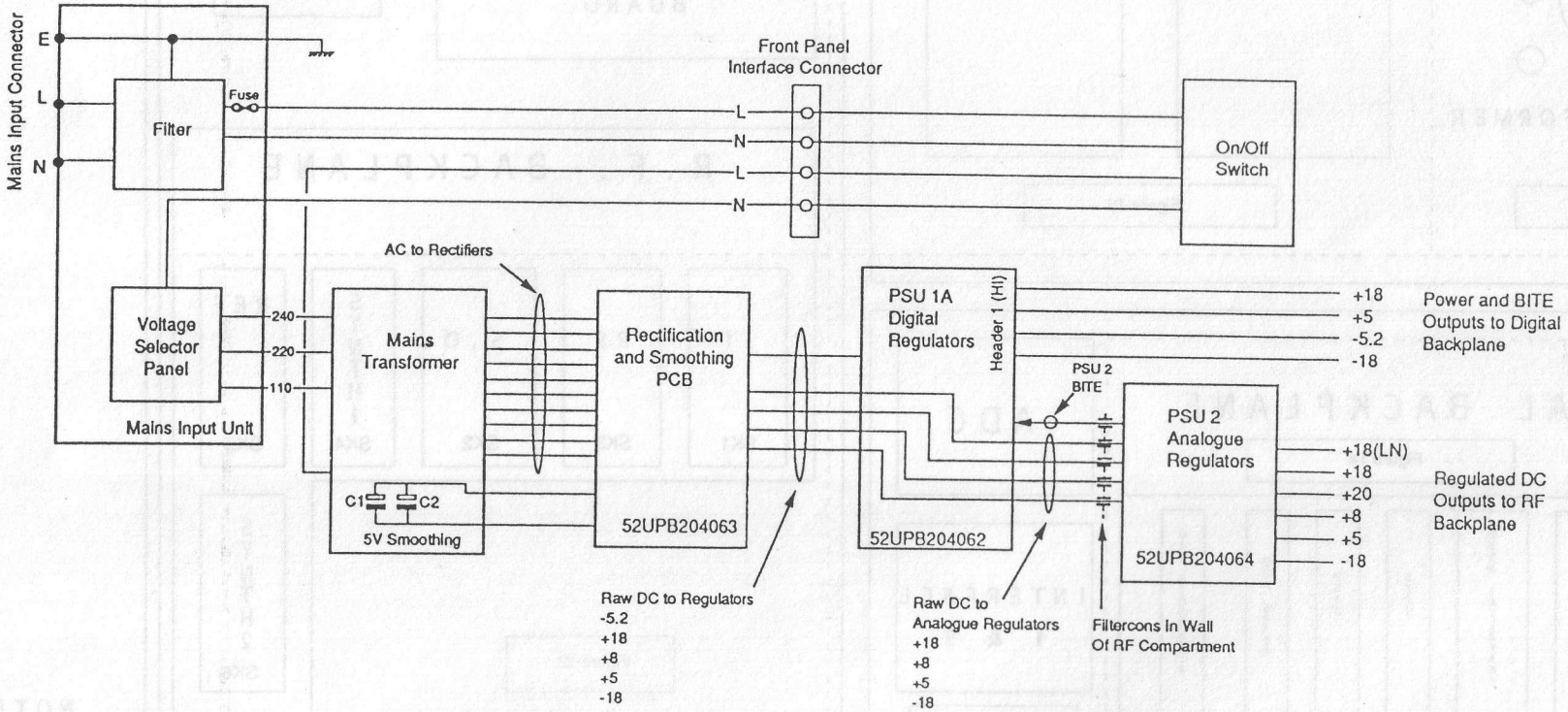


Figure 2 - Power Supply Block Diagram

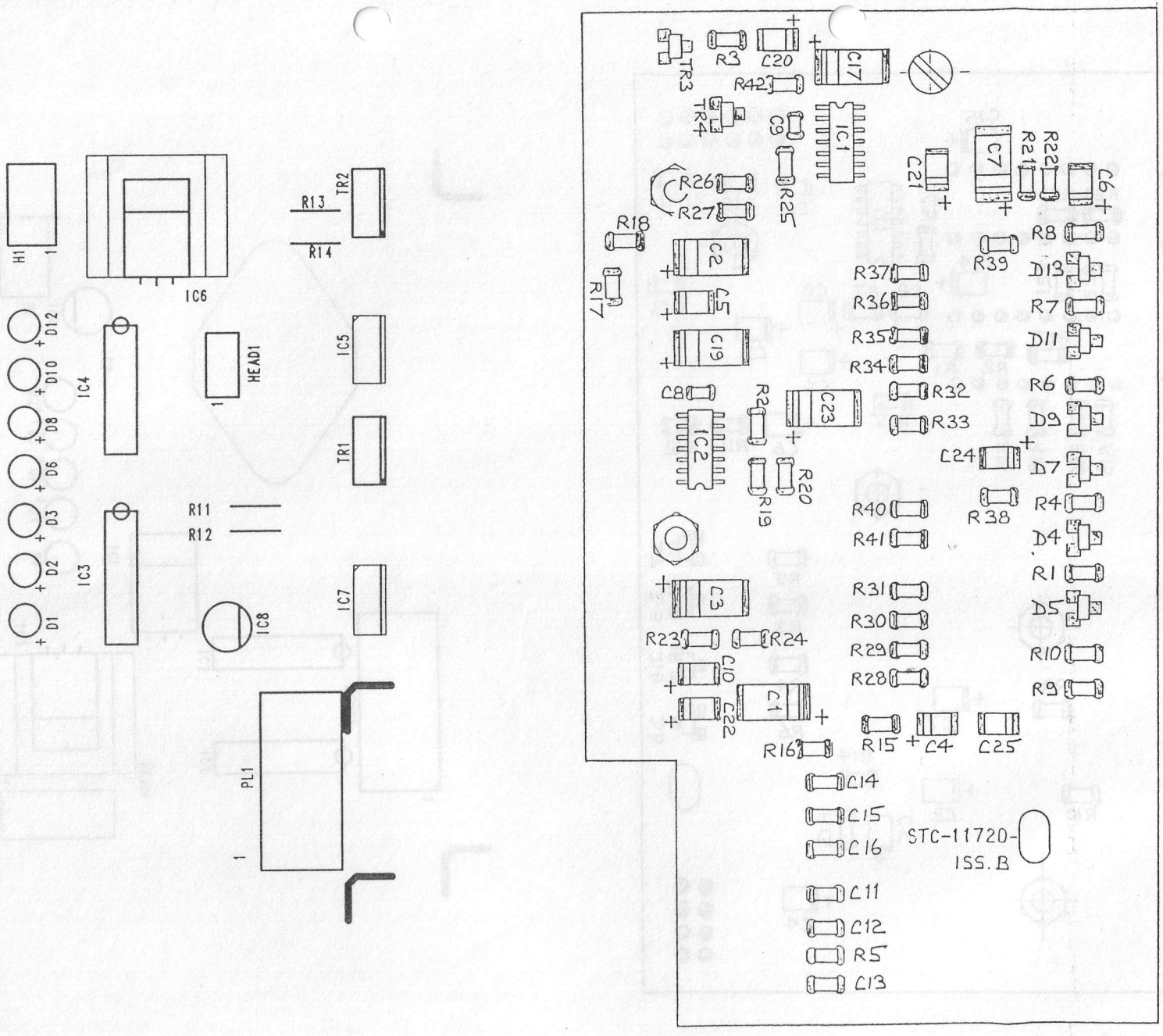
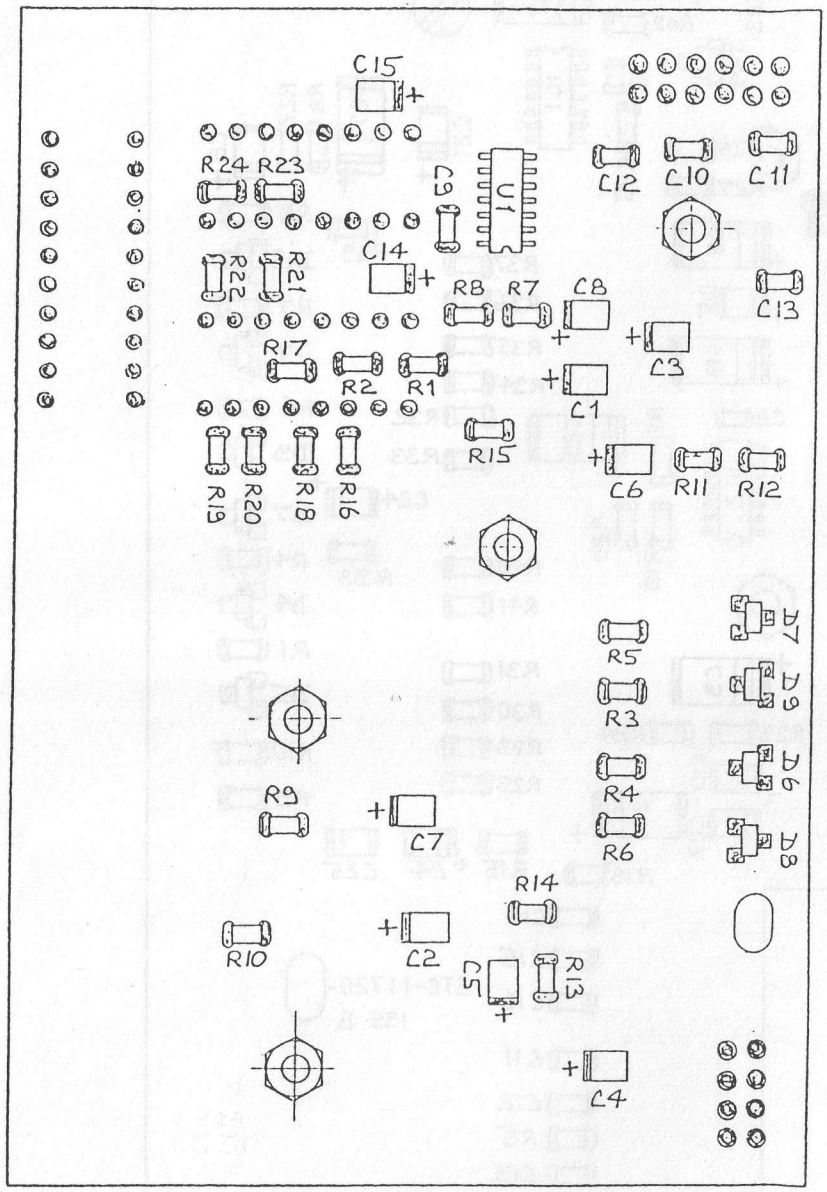


Figure 3 - Analogue PSU Layout Diagram



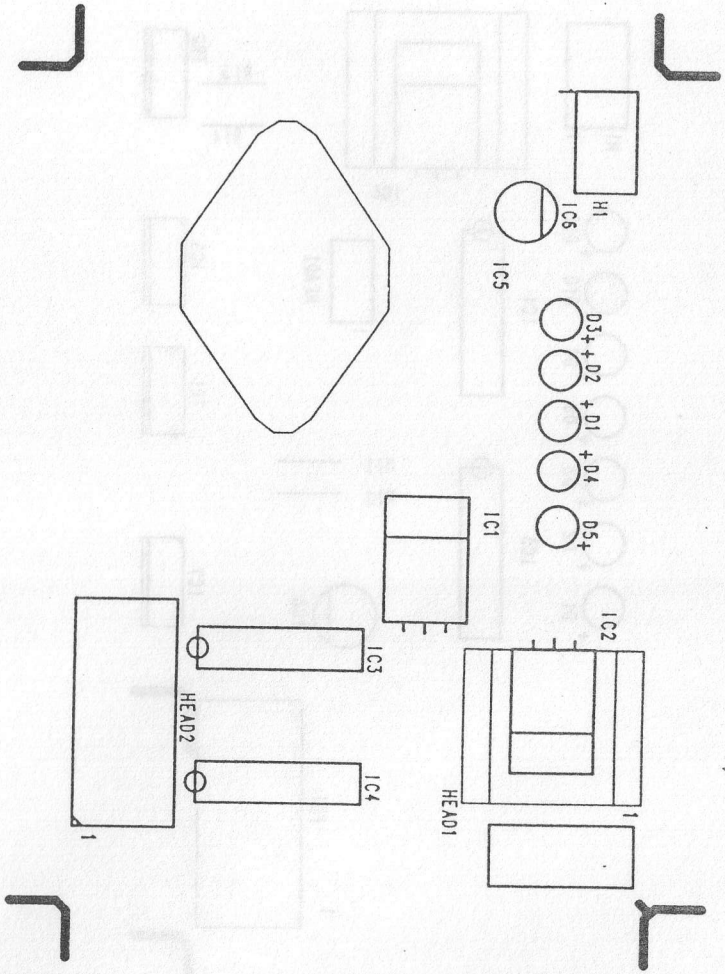


Figure 4 - Digital PSU 1A Layout Diagram

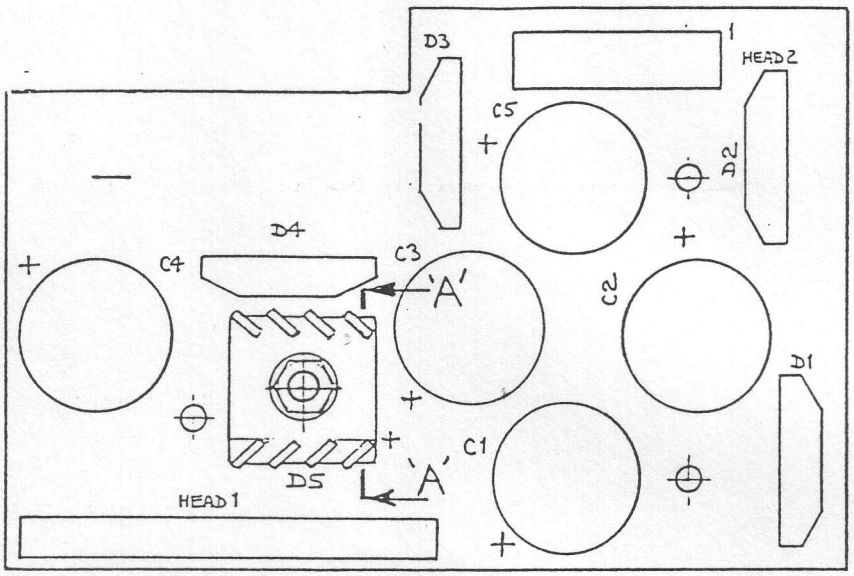


Figure 5 - Rectification and Smoothing Layout Diagram

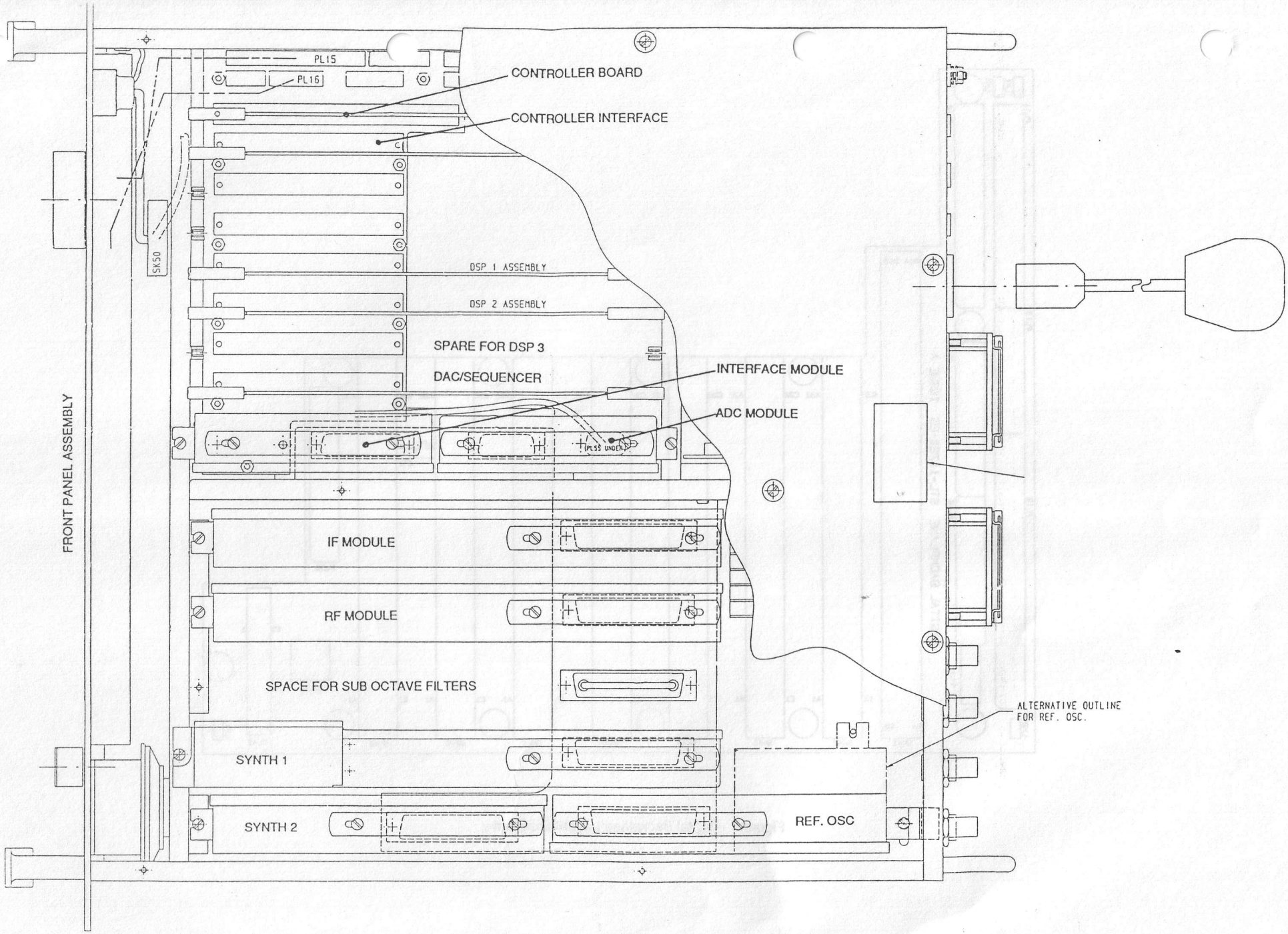


Figure 6 - Chassis Assembly Drawing

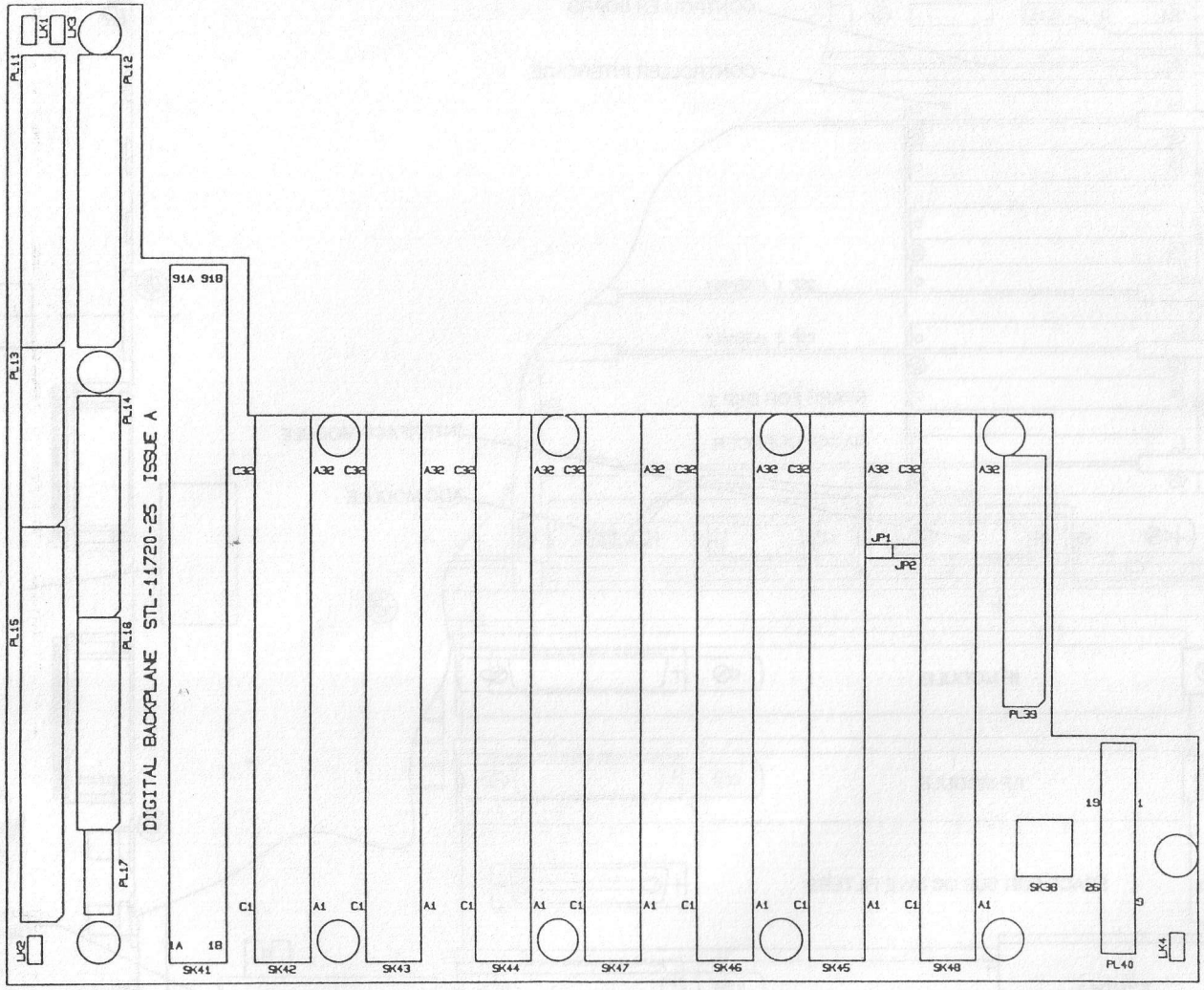


Figure 7 - Digital Backplane Layout Diagram

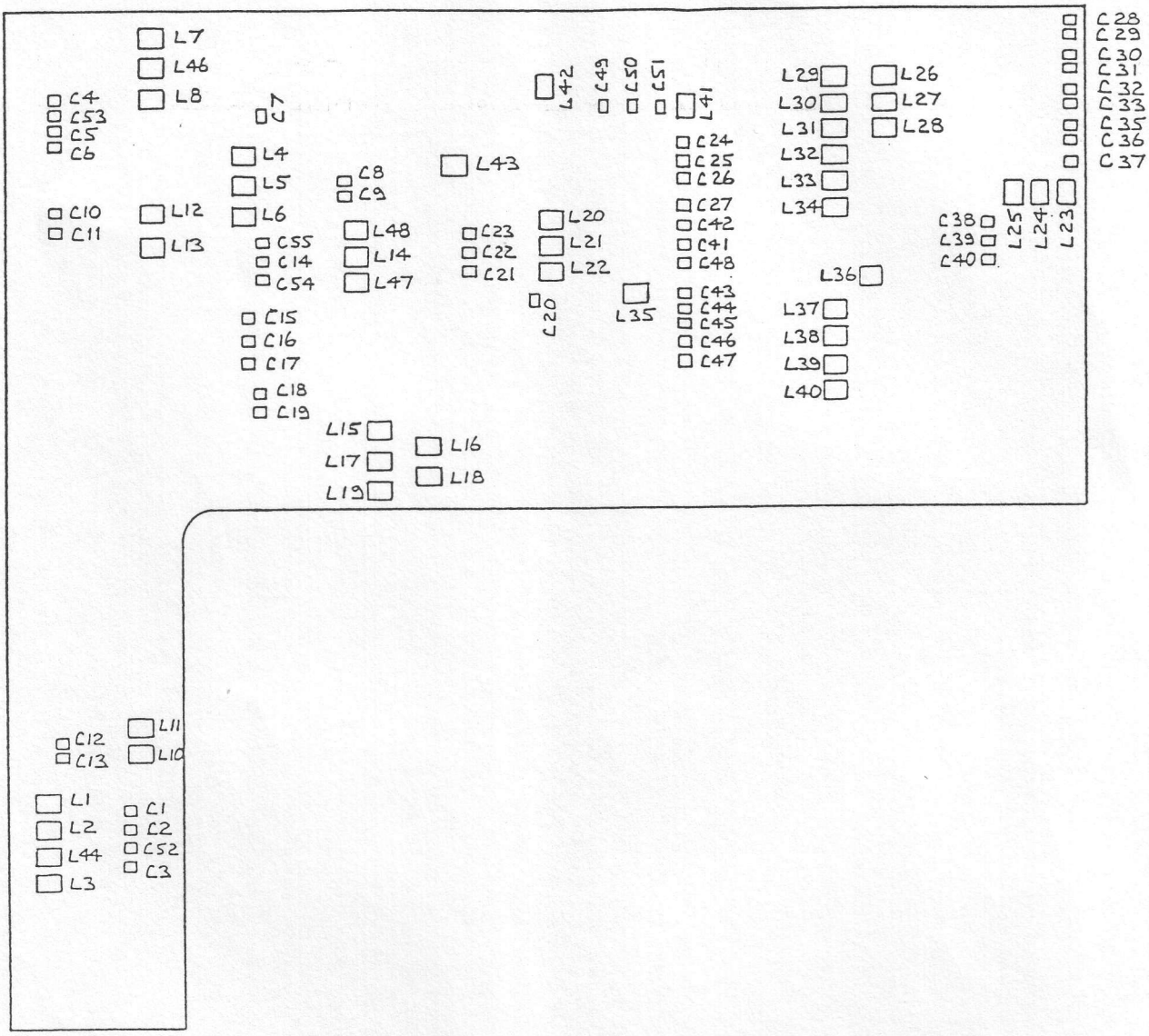


Figure 8 - RF Backplane Layout Diagram

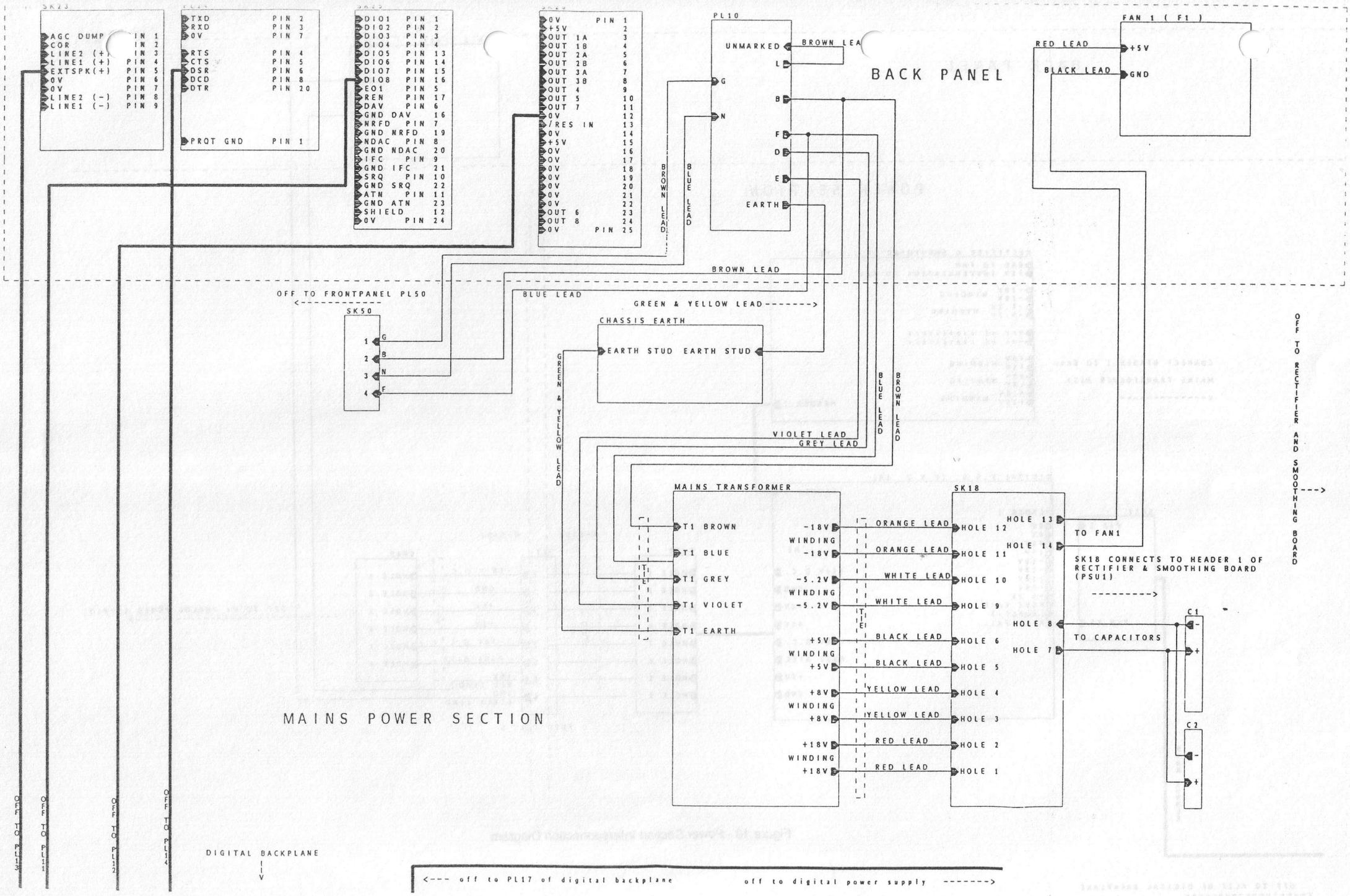


Figure 9 - Mains Power Section Interconnection Diagram

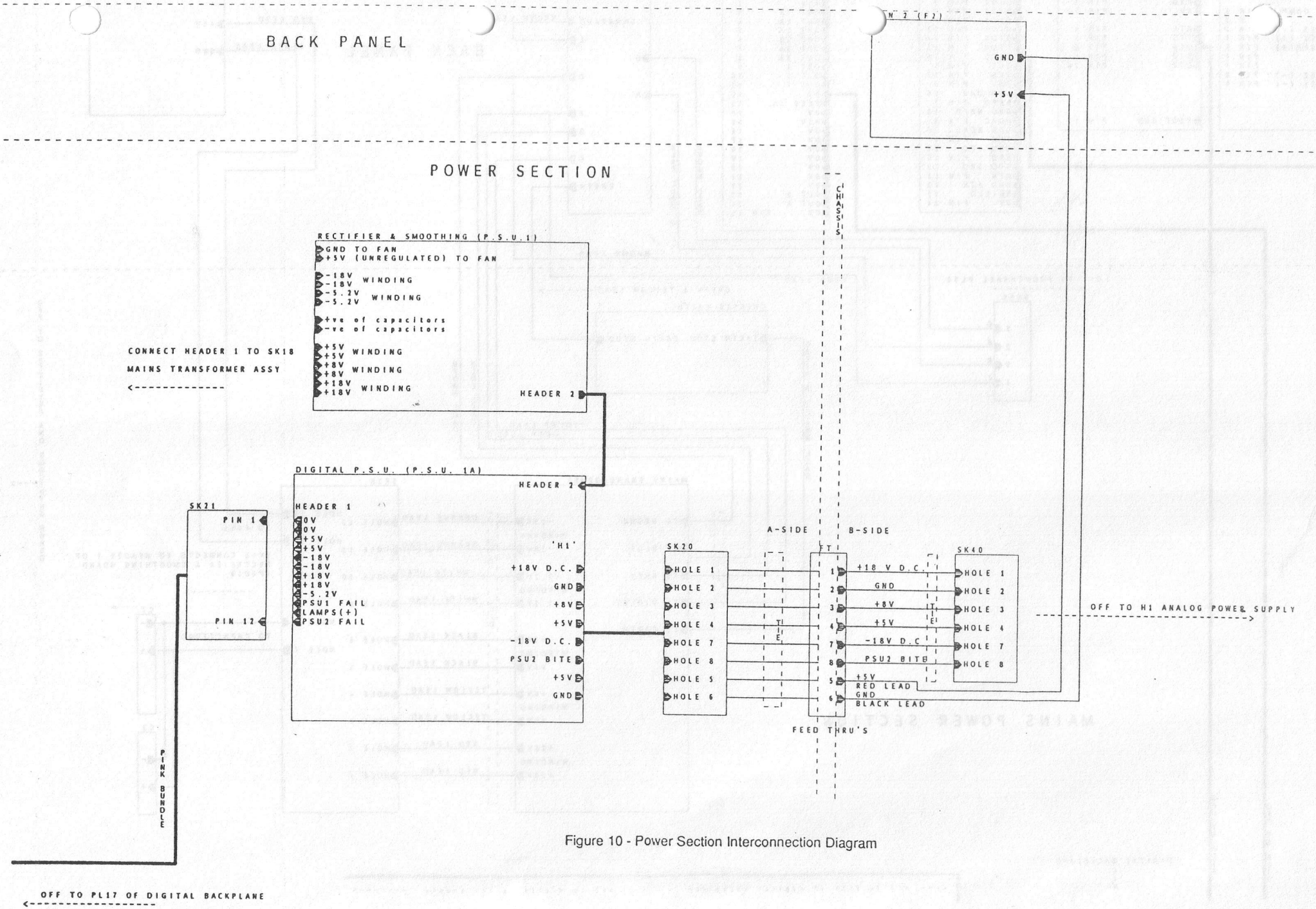


Figure 10 - Power Section Interconnection Diagram

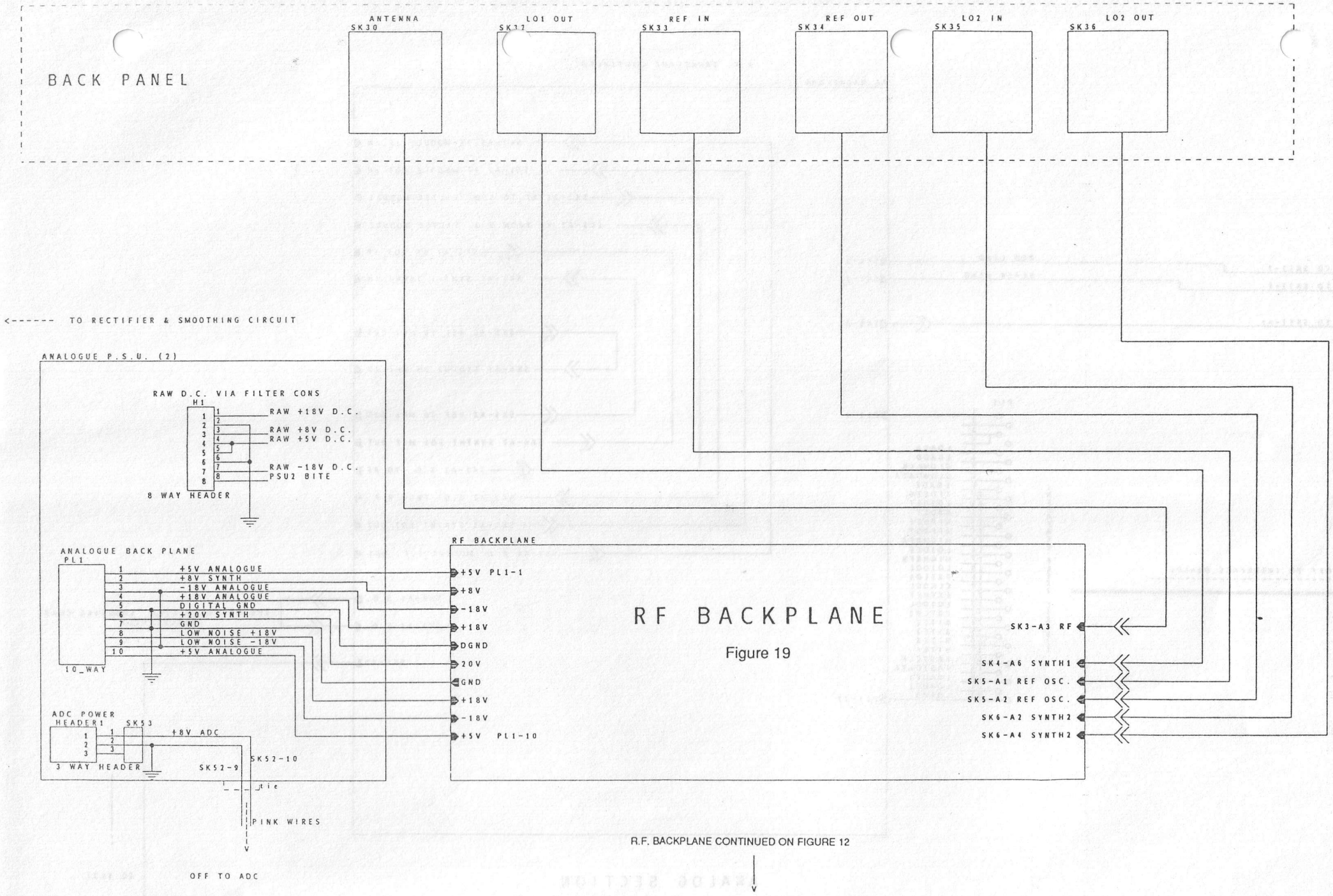


Figure 19

Figure 11 - RF Backplane Interconnection Diagram

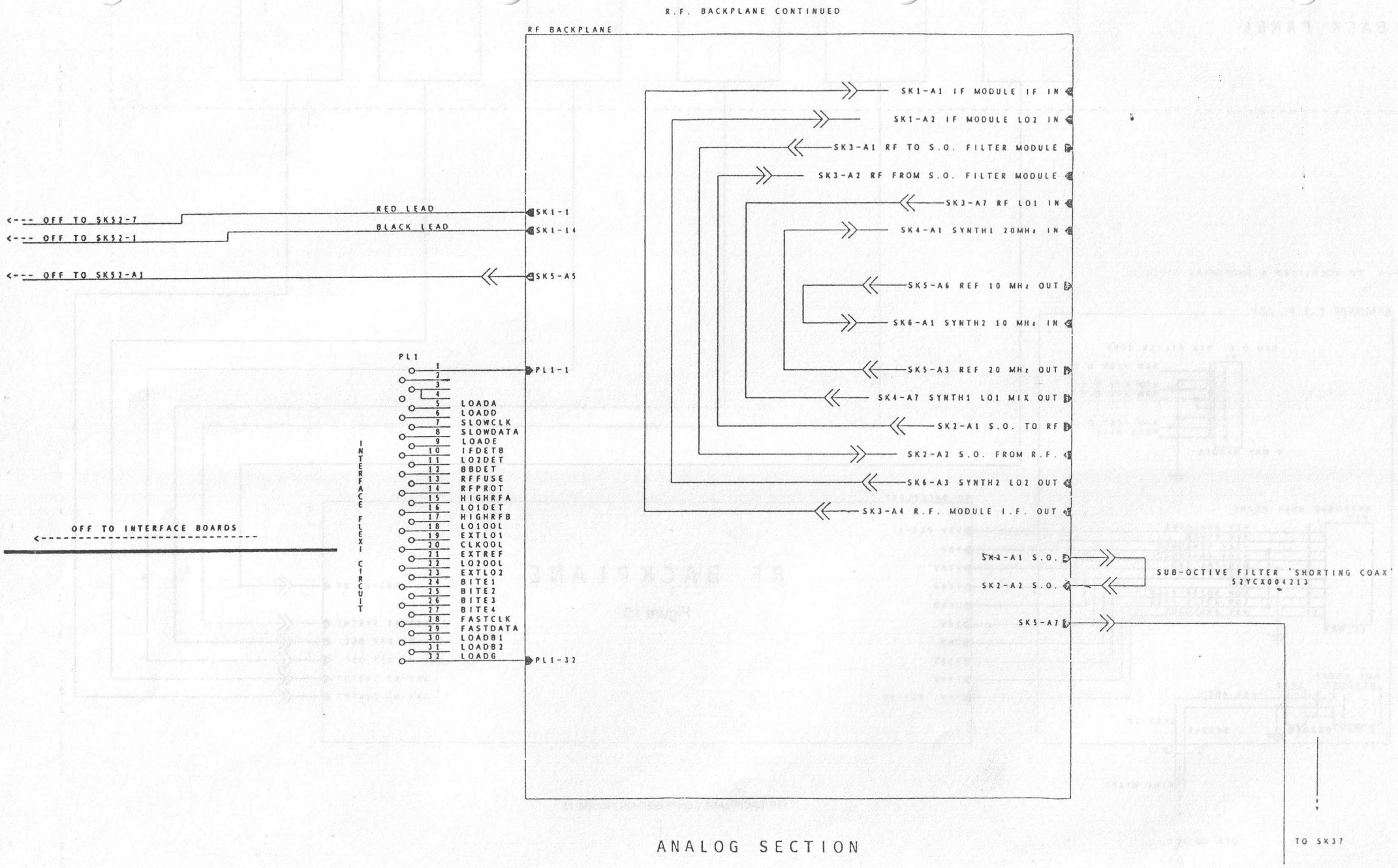


Figure 12 - Analog Section Interconnection Diagram

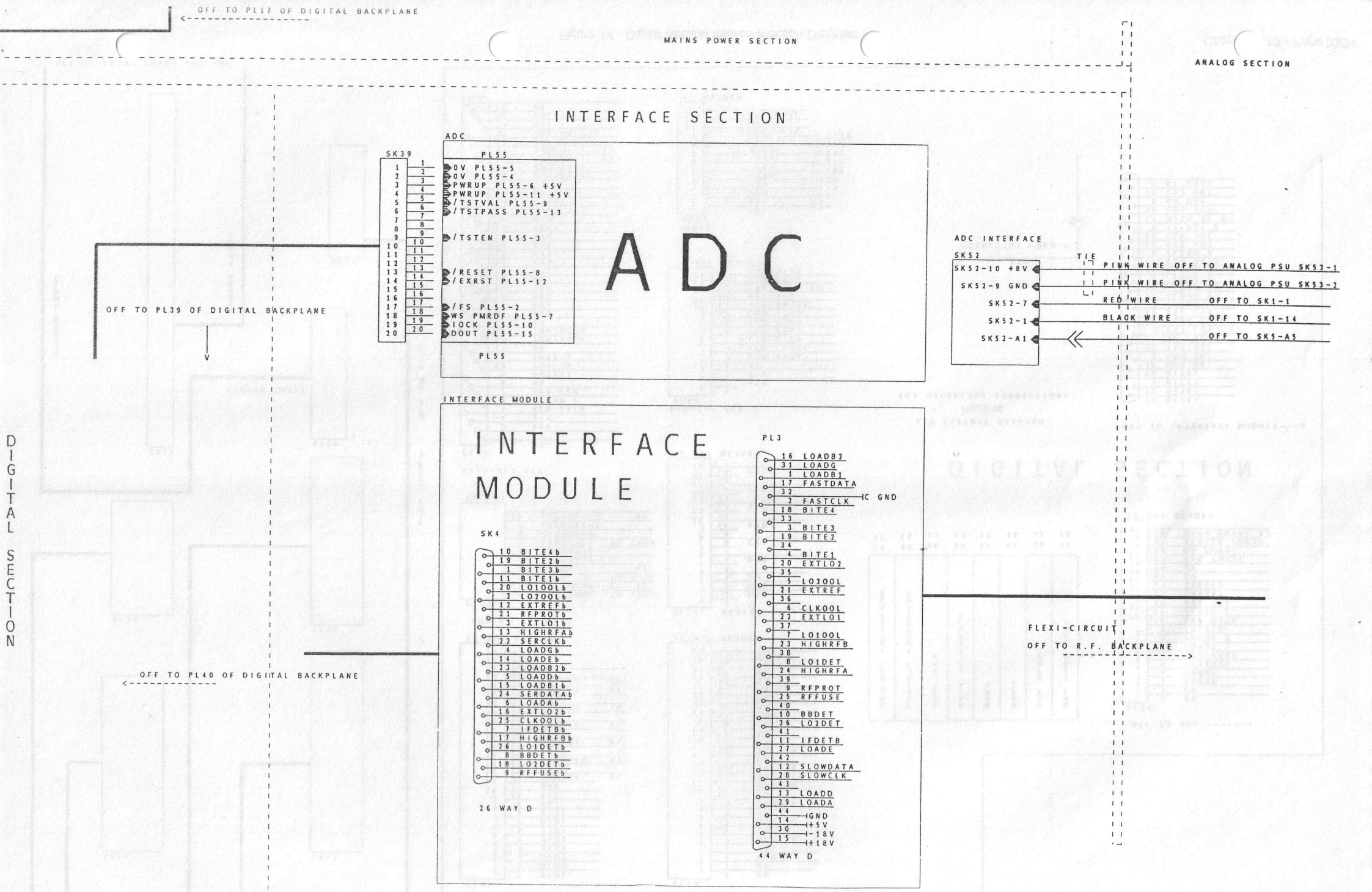


Figure 13 - Interface Section Interconnection Diagram

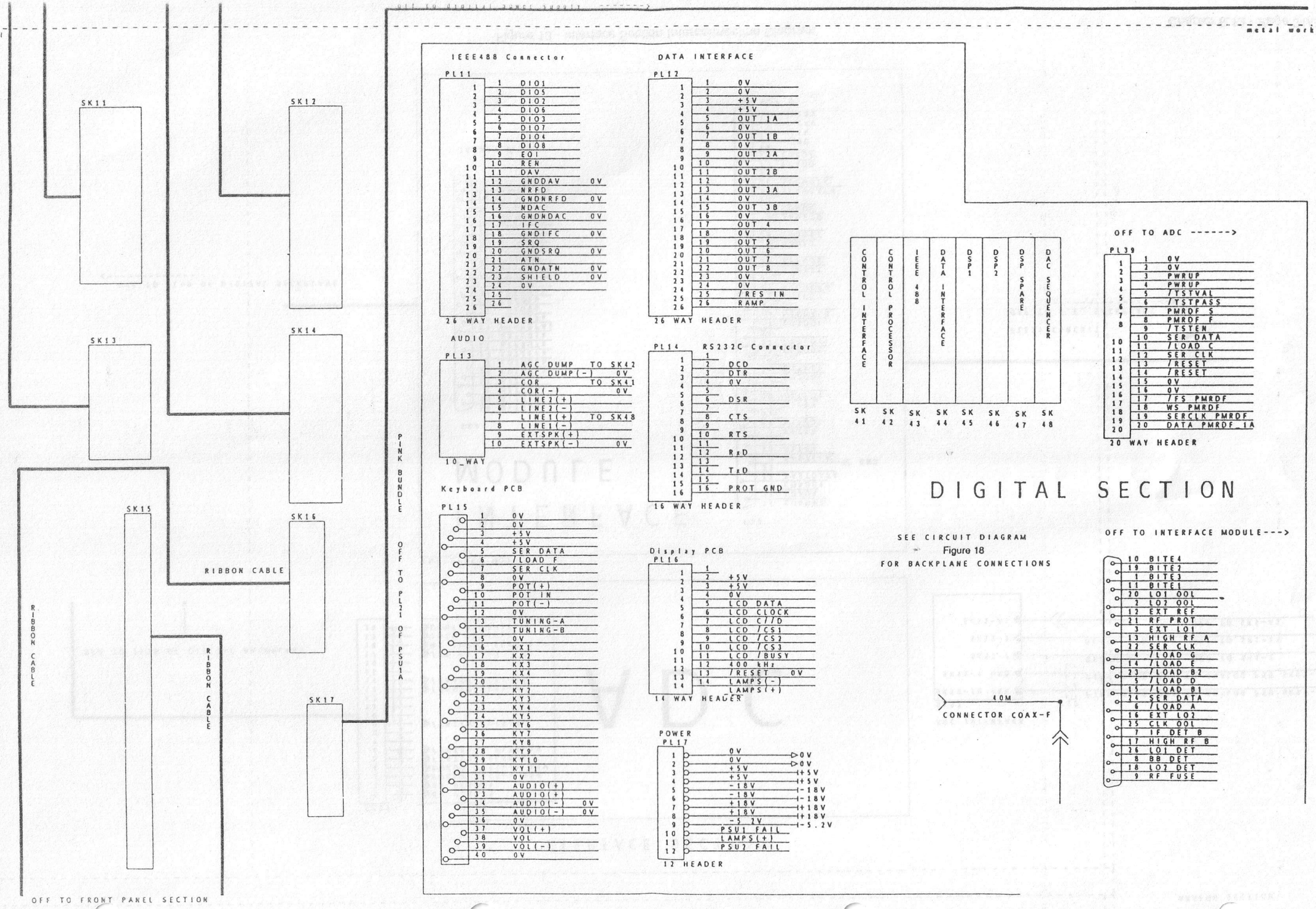


Figure 14 - Digital Section Interconnection Diagram

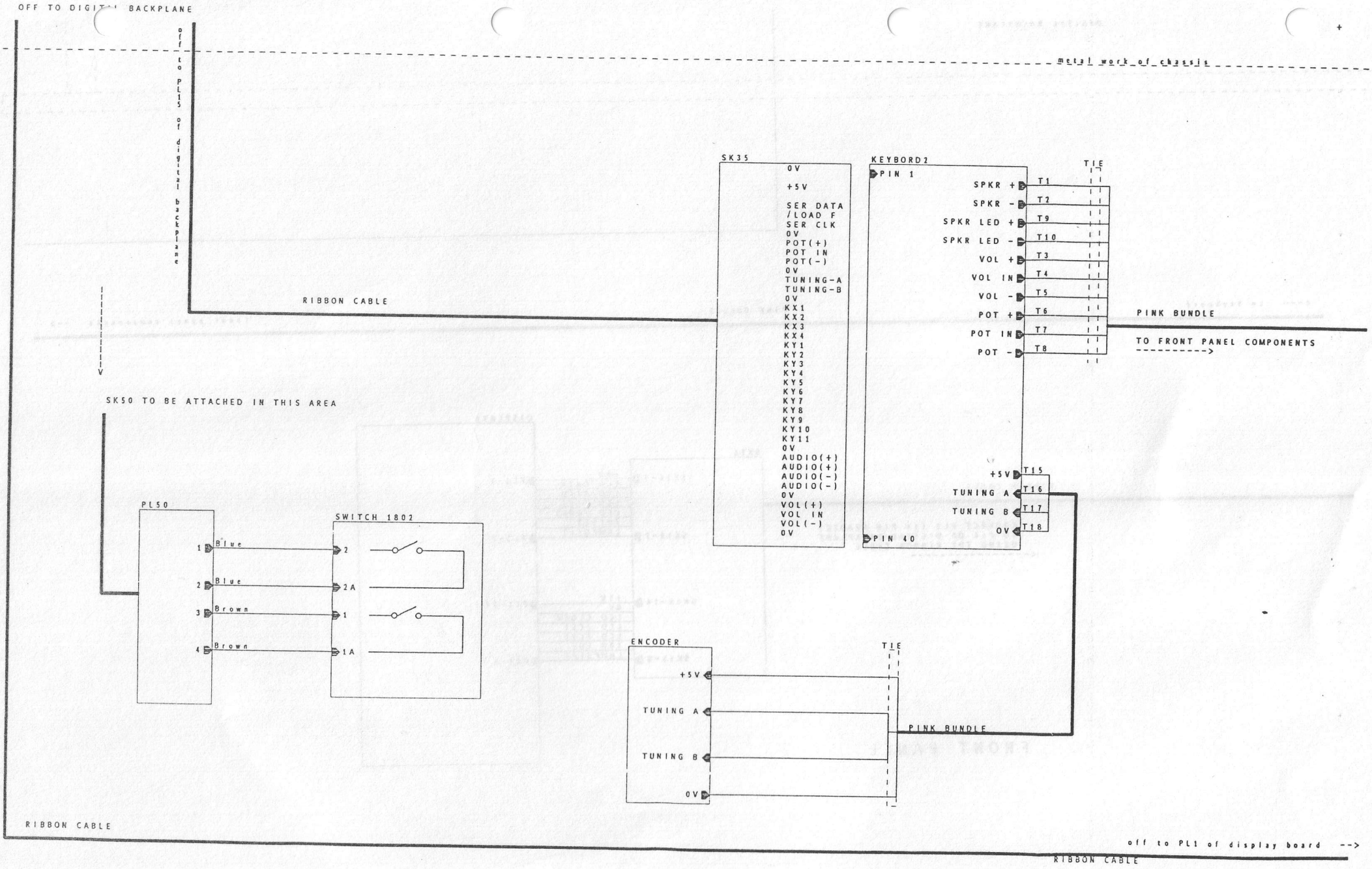


Figure 15 - Front Panel Interconnection to Digital Backplane

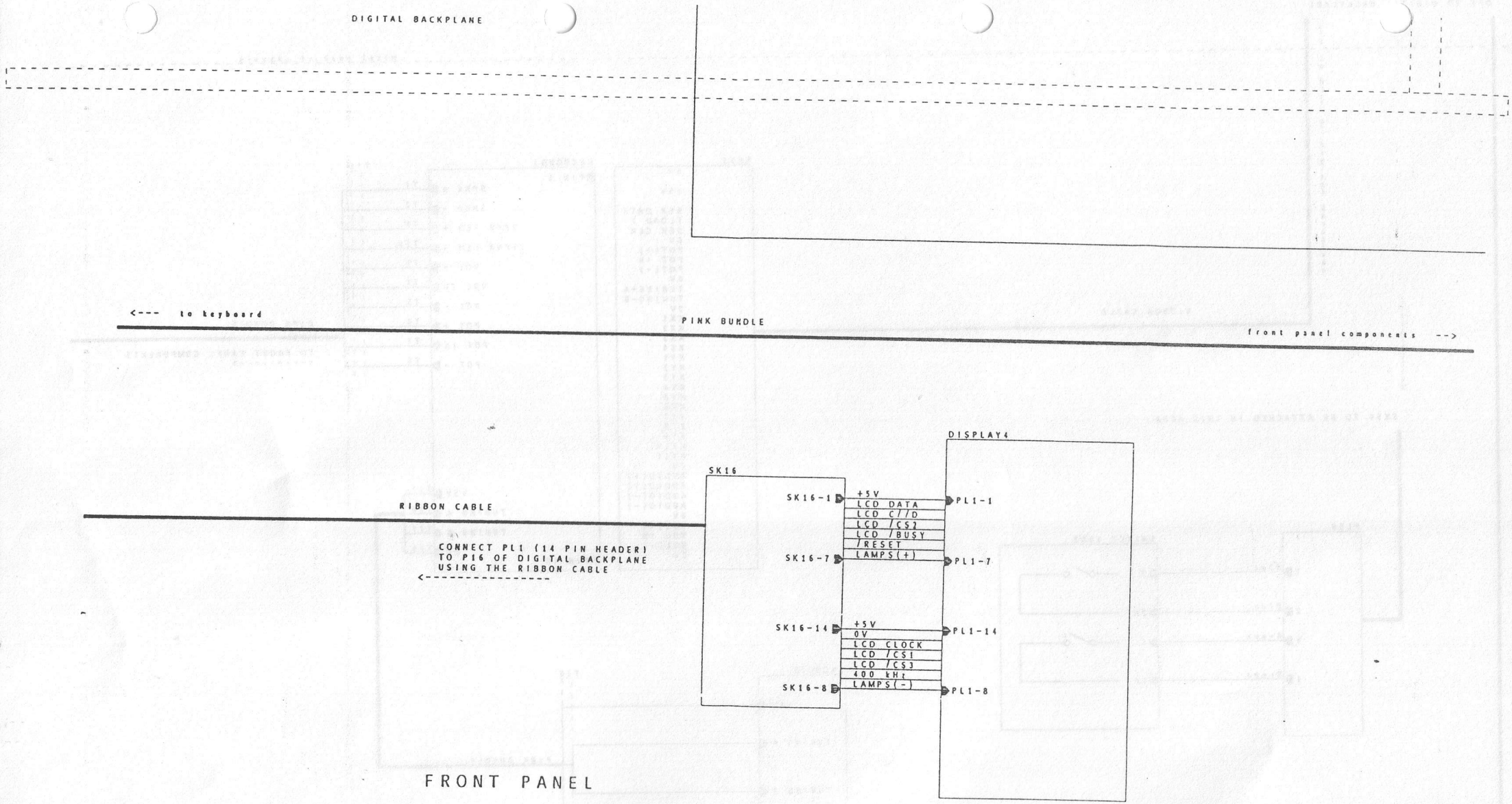


Figure 16 - Front Panel to Keyboard Interconnection Diagram

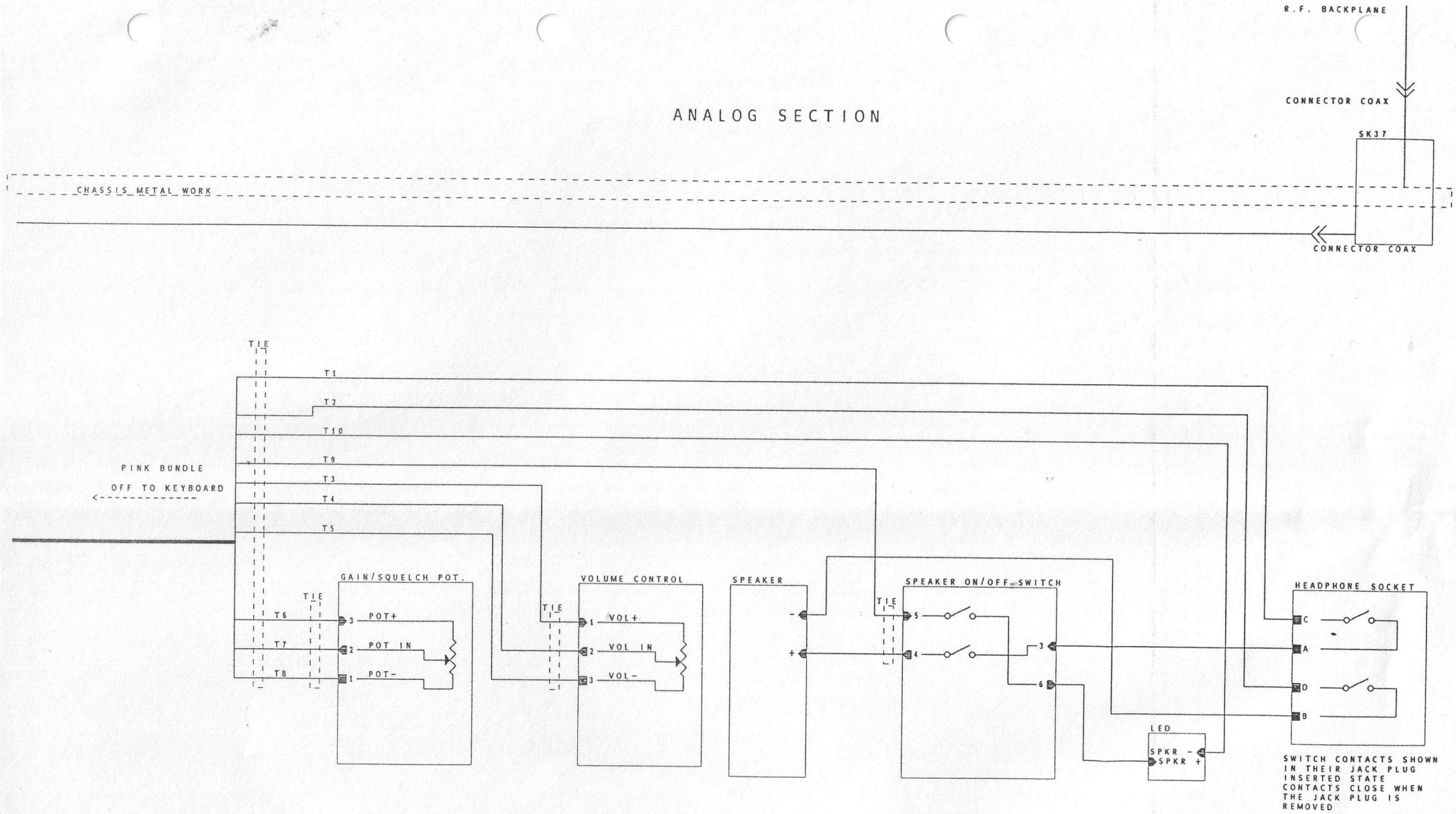


Figure 17 - Front Panel Interconnection Diagram

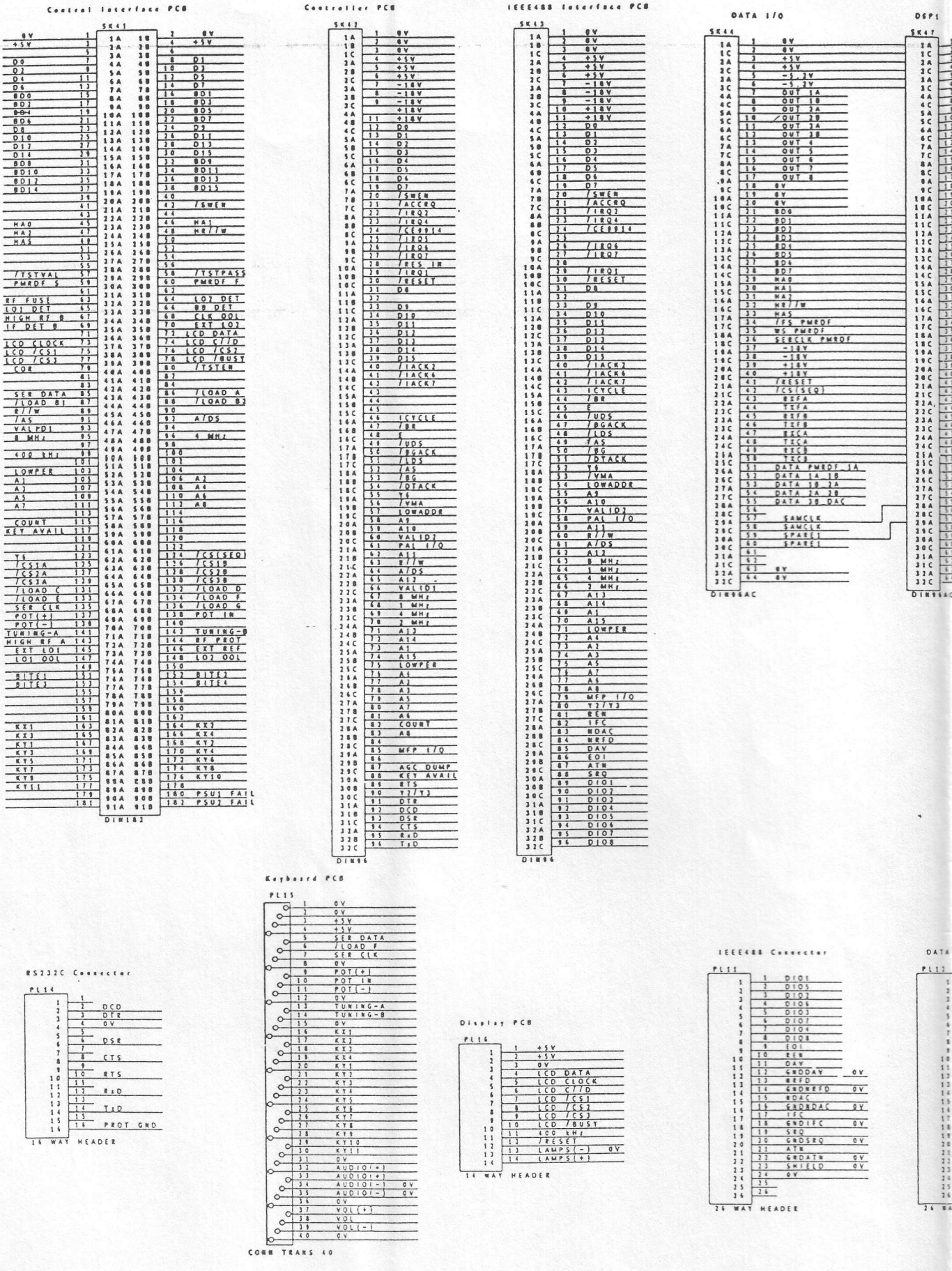
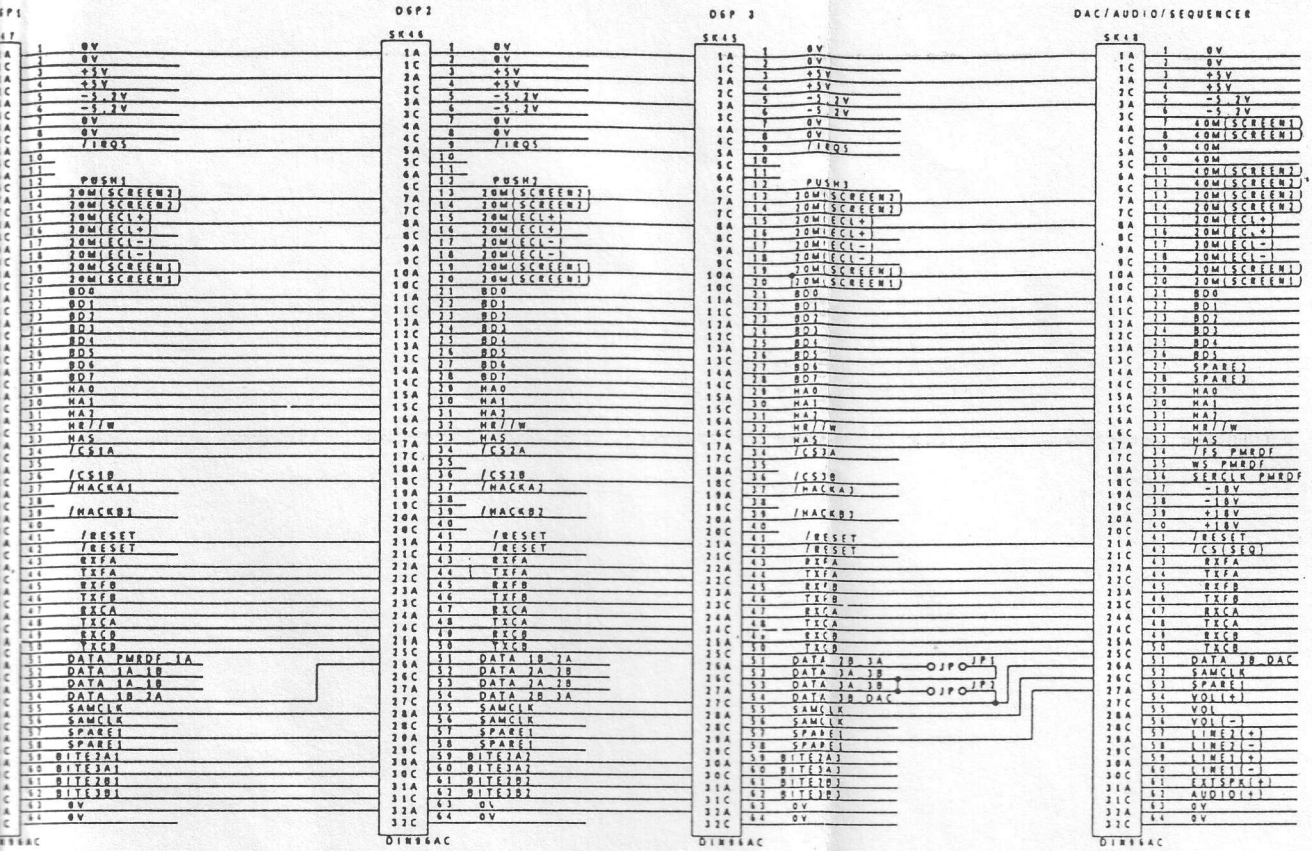
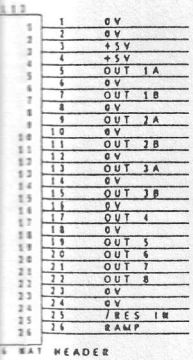
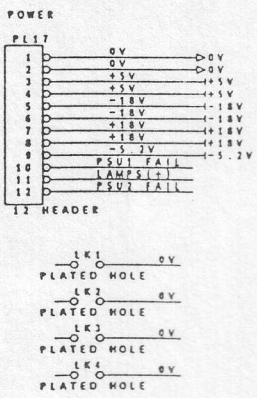


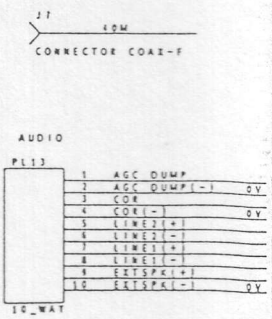
FIGURE 16

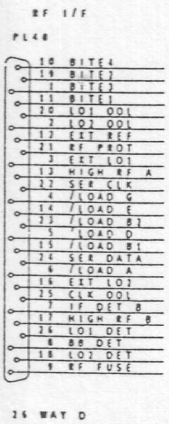
Figure 18 - Digital Back

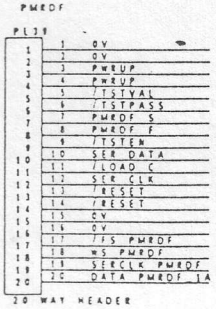












ackplane Interconnection Diagram

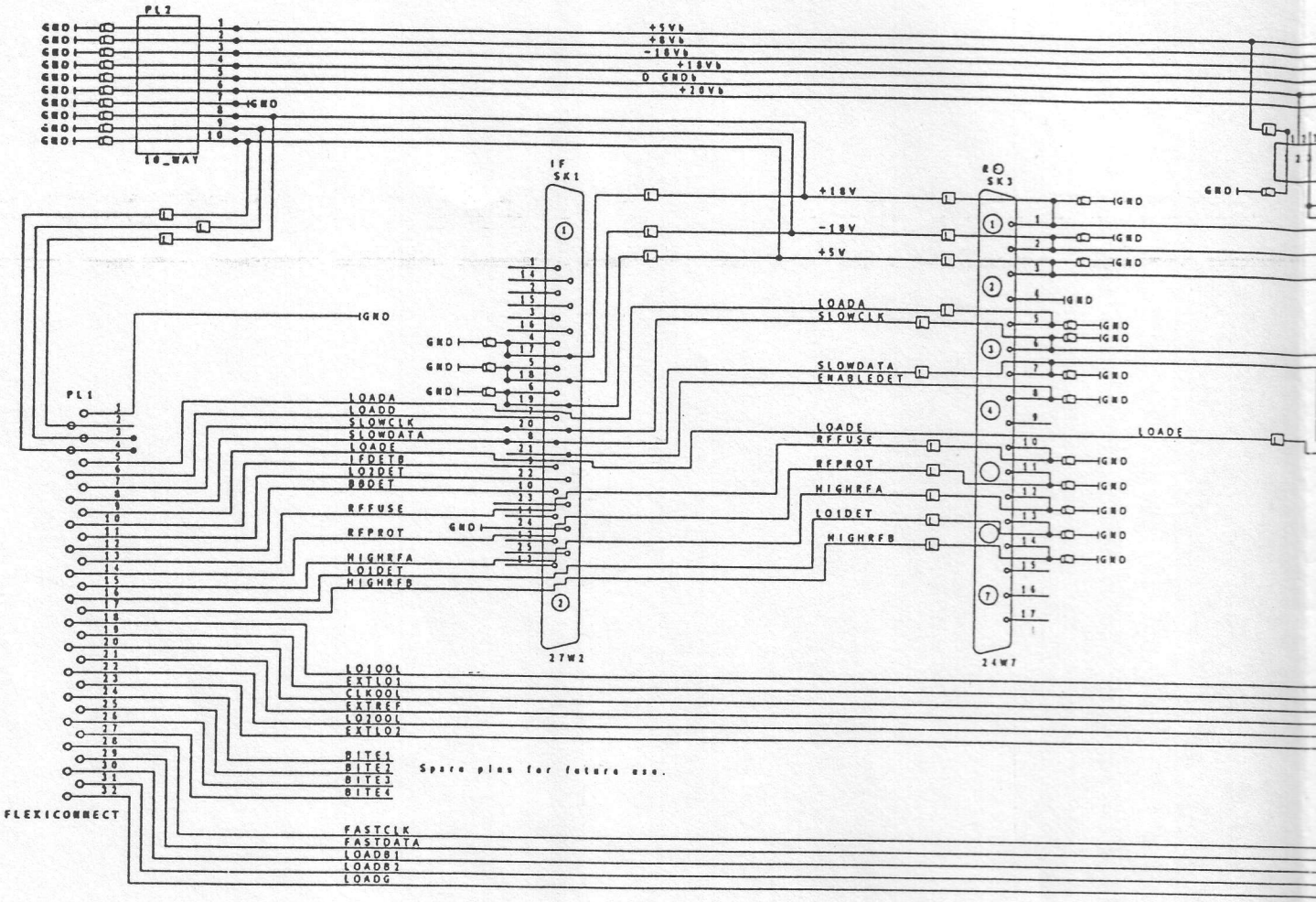
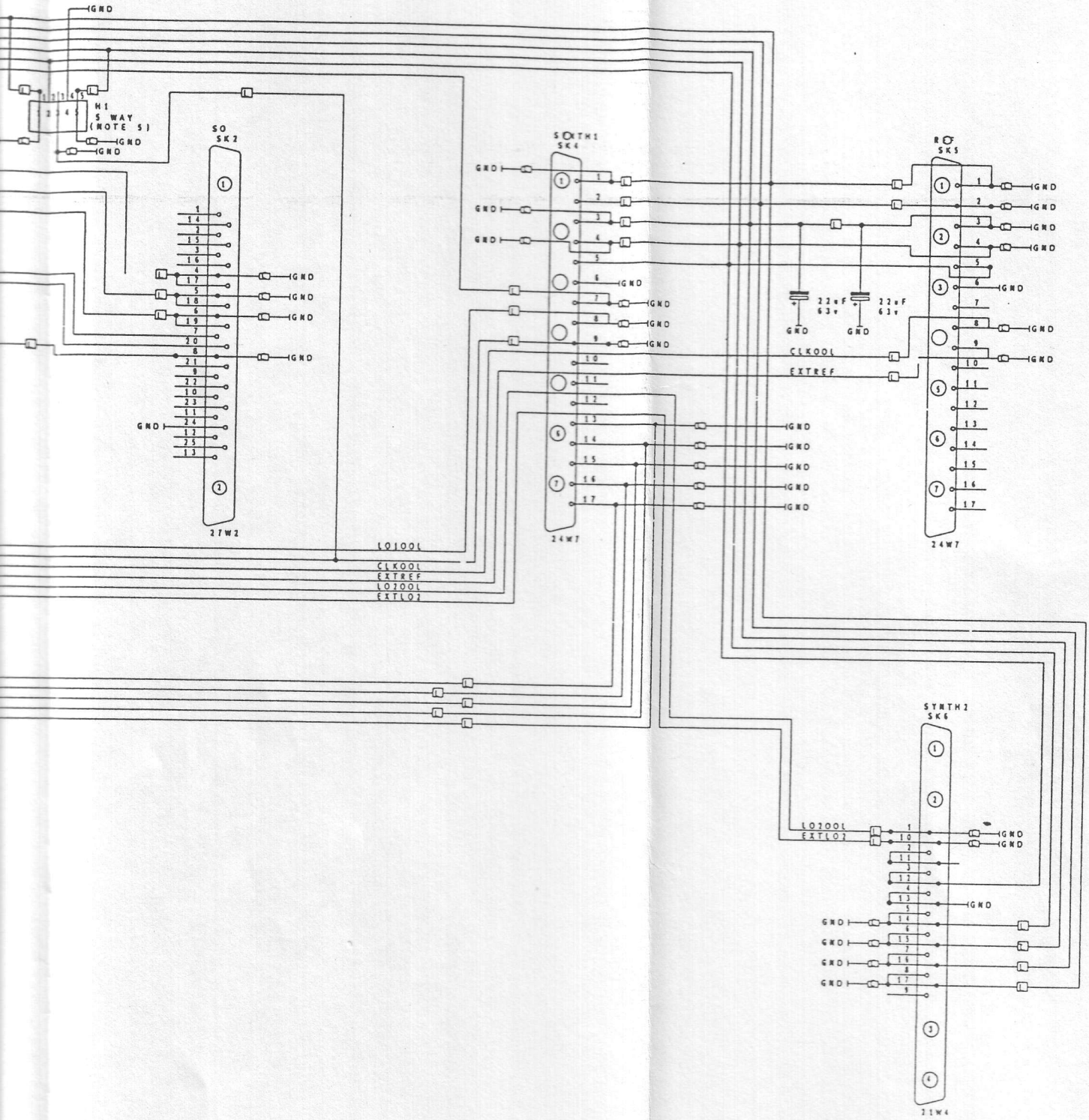


Figure 19 - RF Back

FIGURE 19



F Backplane Interconnection Diagram

Circuit Reference	Description	Value
C1 to C3	Capacitor, fixed, solid tant chip, 10%, 35V	10µ
C4 to C6	Capacitor, fixed, solid tant chip, 10%, 35V	1µ
C7	Capacitor, fixed, solid tant chip, 10%, 35V	10µ
C 8 & C9	Capacitor, fixed, ceramic chip, 10%, 50V	15n
C10	Capacitor, fixed, solid tant chip, 10%, 35V	1µ
C11 to C16	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C17 & C18	Capacitor, fixed, solid tant chip, 10%, 35V	10µ
C19	Capacitor, fixed aluminium electrolytic, ±20%, 63V	22µ
C20 to C22	Capacitor, fixed, solid tant chip, 10%, 35V	1µ
C23	Capacitor, fixed, solid tant chip, 10%, 35V	10µ
C24 & C25	Capacitor, fixed, solid tant chip, 10%, 35V	1µ
C26	Capacitor, fixed, aluminium electrolytic, -10%/+50%, 63V	100µ
C27	Capacitor, multilayer ceramic, 10%, 50V	100n
IC1 & IC2	Voltage regulator, uA7233CD (14 PIN)	
IC3 & IC4	Quad Power Fault Monitor, SG3548N (16 PIN)	
IC5 to IC7	Voltage regulator, positive variable, LM317T	
IC8	Voltage regulator, positive variable LM317LZ	
R1	Resistor, fixed, chip, 5%, 0.25W	100R
R2	Resistor, fixed, chip, 5%, 0.25W	1k2
R3	Resistor, fixed, chip, 5%, 0.25W	10k
R4	Resistor, fixed, chip, 5%, 0.25W	200R
R5	Resistor, fixed, chip, 5%, 0.25W	100R
R6	Resistor, fixed, chip, 5%, 0.25W	82R
R7	Resistor, fixed, chip, 5%, 0.25W	62R
R8	Resistor, fixed, chip, 5%, 0.25W	100R
R9	Resistor, fixed, chip, 1%, 0.125W	300R
R10	Resistor, fixed, chip, 5%, 0.25W	1k
R11 & R12	Resistor, fixed, metal film, 5%, 0.33W	1R5
R13 & R14	Resistor, fixed, metal film, 5%, 0.33W	1R8
R15	Resistor, fixed, chip, 1%, 0.125W	240R
R16	Resistor, fixed, chip, 1%, 0.125W	3k6

Analogue PSU Items List - Sheet 1 of 2

Circuit Reference	Description	Value
R17	Resistor, fixed, chip, 2%, 0.125W	82R
R18	Resistor, fixed, chip, 1%, 0.125W	1k1
R19	Resistor, fixed, chip, 1%, 0.125W	3k
R20	Resistor, fixed, chip, 1%, 0.125W	2k
R21	Resistor, fixed, chip, 1%, 0.125W	240R
R22	Resistor, fixed, chip, 1%, 0.125W	1k3
R23	Resistor, fixed, chip, 1%, 0.125W	100R
R24	Resistor, fixed, chip, 1%, 0.125W	300R
R25 & R26	Resistor, fixed, chip, 1%, 0.125W	3k
R27	Resistor, fixed, chip, 1%, 0.125W	12k
R28	Resistor, fixed, chip, 1%, 0.125W	3k3
R29	Resistor, fixed, chip, 1%, 0.125W	470R
R30	Resistor, fixed, chip, 1%, 0.125W	6k2
R31	Resistor, fixed, chip, 1%, 0.125W	1k
R32	Resistor, fixed, chip, 1%, 0.125W	6k2
R33	Resistor, fixed, chip, 1%, 0.125W	1k
R34	Resistor, fixed, chip, 1%, 0.125W	2k2
R35 to R37	Resistor, fixed, chip, 1%, 0.125W	1k
R38	Resistor, fixed, chip, 1%, 0.125W	110R
R39	Resistor, fixed, chip, 1%, 0.125W	2k
R40	Resistor, fixed, chip, 1%, 0.125W	13k
R41	Resistor, fixed, chip, 1%, 0.125W	1k8
R42	Resistor, fixed, chip, 1%, 0.125W	3k
D4 & D5	Diode, Zener, BZX84C15	
D7	Diode, Zener,BZX84C15	
D9	Diode, Zener, BZX84C5V1	
D11	Diode, Zener, BZZ84C2V4	
D13	Diode, Zener, BZX84C15	
TR1	Transistor, NPN, TIP41A	
TR2	Transistor, NPN, TIP42A	
TR3 & TR4	Transistor, PNP, BCW29	

Analogue PSU Items List - Sheet 2 of 2

Circuit Reference	Description	Value
C1 to C8	Capacitor, fixed, solid tant chip, 10%, 35V	1µ
C9 to C13	Capacitor, fixed, ceramic chip, 10%, 50V	100n
C14 to C15	Capacitor, fixed, solid tant chip, 10%, 35V	1µ
IC1	Voltage regulator, positive variable, LM317T	
IC2	Voltage regulator, negative variable, LM337T	
IC3 & IC4	Quad power fault monitor, SG3548N	
IC5	Voltage regulator, positive variable, LM350K	
IC6	Voltage regulator, negative variable, LM337T	
U1	Quad 2 input Nand Schmitt trigger, HEF4093BT	
R1	Resistor, fixed, chip, 1%, 0.125W	300R
R2	Resistor, fixed, chip, 5%, 0.25W	1k
R3	Resistor, fixed, chip, 5%, 0.25W	200R
R4	Resistor, fixed, chip, 5%, 0.25W	62R
R5	Resistor, fixed, chip, 5%, 0.25W	82R
R6	Resistor, fixed, chip, 5%, 0.25W	200R
R7	Resistor, fixed, chip, 2%, 0.125W	82R
R8	Resistor, fixed, chip, 1%, 0.125W	1k1
R9	Resistor, fixed, chip, 1%, 0.125W	100R
R10	Resistor, fixed, chip, 1%, 0.125W	300R
R11	Resistor, fixed, chip, 1%, 0.125W	150R
R12	Resistor, fixed, chip, 1%, 0.125W	470R
R13	Resistor, fixed, chip, 2%, 0.125W	82R
R14	Resistor, fixed, chip, 1%, 0.125W	1k1
R15	Resistor, fixed, chip, 1%, 0.125W	6k2
R16 to R18	Resistor, fixed, chip, 1%, 0.125W	1k
R19	Resistor, fixed, chip, 1%, 0.125W	2k7
R20	Resistor, fixed, chip, 1%, 0.125W	1k3
R21	Resistor, fixed, chip, 1%, 0.125W	110R
R22	Resistor, fixed, chip, 1%, 0.125W	2k

Digital PSU 1A Items List - Sheet 1 of 2

Circuit Reference	Description	Value
R23	Resistor, fixed, chip, 1%, 0.125W	13k
R24	Resistor, fixed, chip, 1%, 0.125W	1k8
D1 to D4	LED, Green diffused lens, LG3360-GK	
D5	LED, Red diffused lens, LG3360-DG	
D6 & D7	Diode, Zener, BZX84C2V4	
D8 & D9	Diode, Zener, BZX84C15	

Digital PSU 1A Items List - Sheet 2 of 2

Circuit Reference	Description	Value
C1 to C5	Capacitor, Fixed, Electrolytic, 35V	4m7
D1	Rectifier, Silicon Bridge, BY225-100	
D2 to D4	Rectifier, SKB2/D2L5A	
D5	Rectifier, Silicon Bridge, KBPC802	

Rectification and Smoothing Items List - Sheet 1 of 1

Circuit Reference	Description	Value
SK38	Socket, coaxial, right angle jack receptacle	
SK41	Socket, multiway, card edge	
SK42 & SK43	Socket, multiway, DIN41612 96 PIN	
SK44 to SK48	Socket, multiway, DIN41612 64 PIN	
PL11 & PL12	Plug, multi, 1"x1" STR. 4 wall, 26 way	
PL13	Plug, multi, 1"x1" STR. 4 wall, 10 way	
PL14	Plug, multi, 1"x1" STR. 4 wall, 16 way	
PL15	Plug, multi, 1"x1" STR. 4 wall, 40 way	
PL16	Plug, multi, 1"x1" STR. 4 wall, 14 way	
PL17	Plug, modified	
PL39	Plug, multi, x10 way Dubox	
PL40	Plug, Multiway, 'D' type, 26 way straight spill PCB	

Digital Backplane Items List - Sheet 1 of 1

Circuit Reference	Description	Value
C1 to C9	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C10 to C14	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C20	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C21 to C26	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C27	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C28 to C33	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C35 to C40	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C41 to C48	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C49	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C50	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C51 to C53	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C54	Capacitor, fixed, ceramic chip, 5%, 100V	47p
C55	Capacitor, fixed, ceramic chip, 10%, 100V	10n
C56 & C57	Capacitor, fixed, aluminium electrolytic, 20%, 63V	22µ
L1 to L3	Choke, fixed, chip, 10%	47µ
L4	Choke, fixed, chip, 10%	3µ3
L5 to L8	Choke, fixed, chip, 10%	47µ
L10 to L19	Choke, fixed, chip, 10%	4µ7
L20 & L21	Choke, fixed, chip, 10%	47µ
L22	Choke, fixed, chip, 10%	27µ
L23 to L25	Choke, fixed, chip, 10%	47µ
L26	Choke, fixed, chip, 10%	4µ7
L27	Choke, fixed, chip, 10%	15µ
L28	Choke, fixed, chip, 10%	47µ
L29	Choke, fixed, chip, 10%	4µ7
L30	Choke, fixed, chip, 10%	27µ
L31	Choke, fixed, chip, 10%	10µ
L32 to L40	Choke, fixed, chip, 10%	4µ7
L41 & L42	Choke, fixed, chip, 10%	47µ
L43	Choke, fixed, chip, 10%	4µ7
L44 & L46	Choke, fixed, chip, 10%	47µ
L47	Choke, fixed, chip, 10%	4µ7

RF Backplane Items List - Sheet 1 of 2

Circuit Reference	Description	Value
L48	Choke, fixed, chip, 10%	47µ
L49	Choke, fixed, RF, 10%	15µ
SK1 to SK6	Socket, multiway, mixed 'D' type	
SK52	Socket, multiway, mixed 'D' type	
PL2	Plug, multiway, 0.25" sq., header, 10 way	

RF Backplane Items List - Sheet 2 of 2

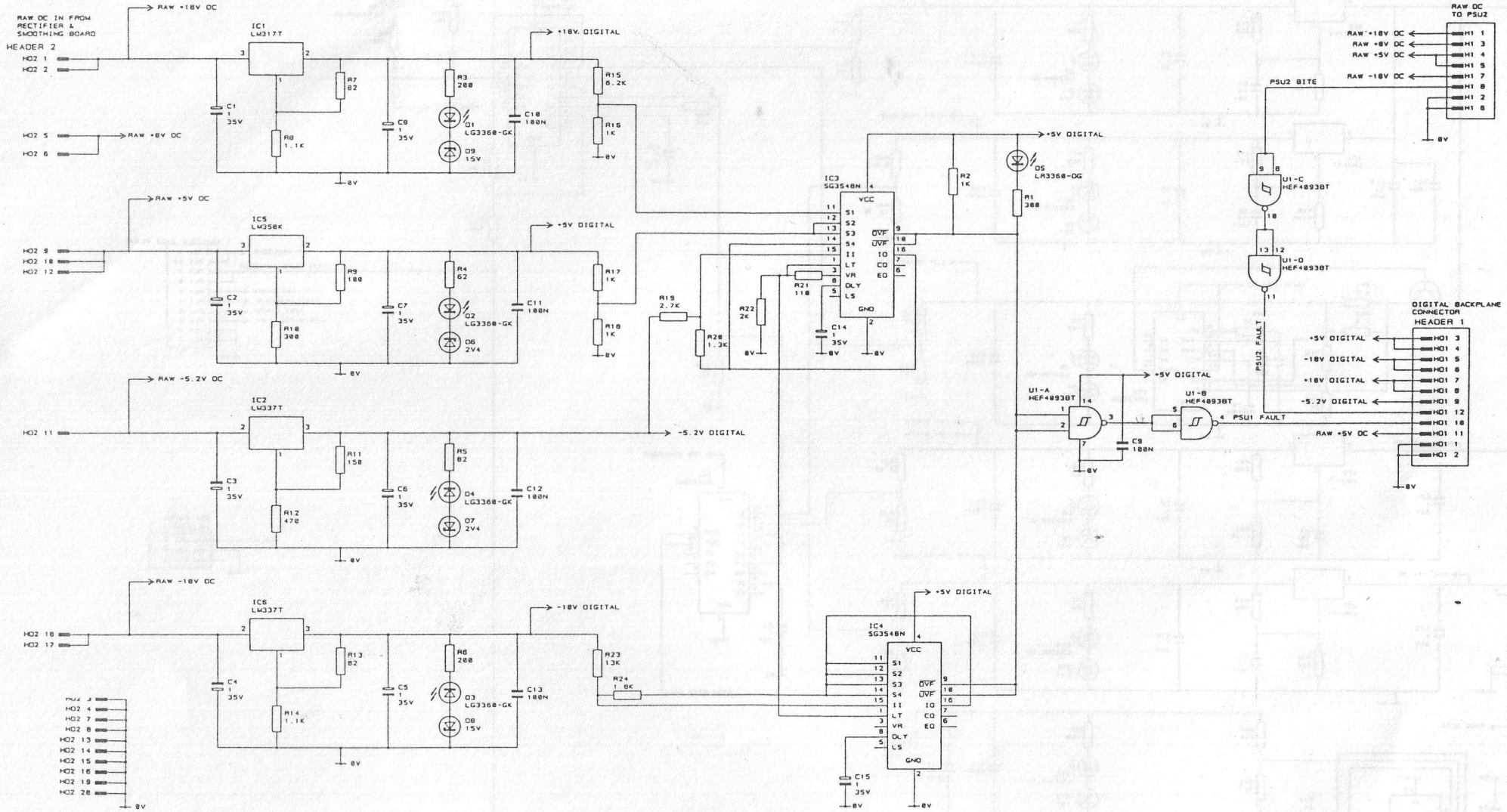


Figure 20 - Digital PSU Circuit Diagram

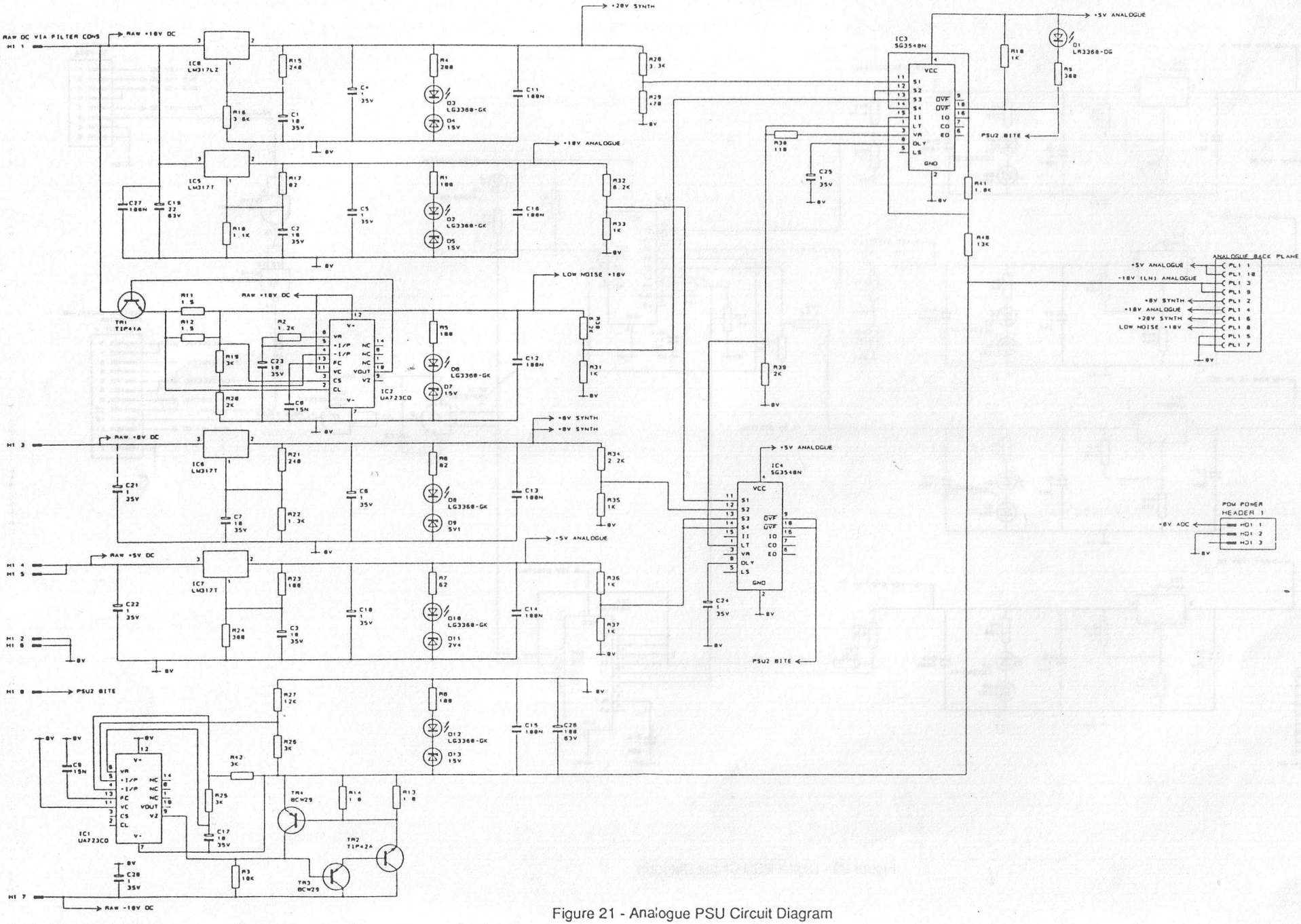


Figure 21 - Analogue PSU Circuit Diagram

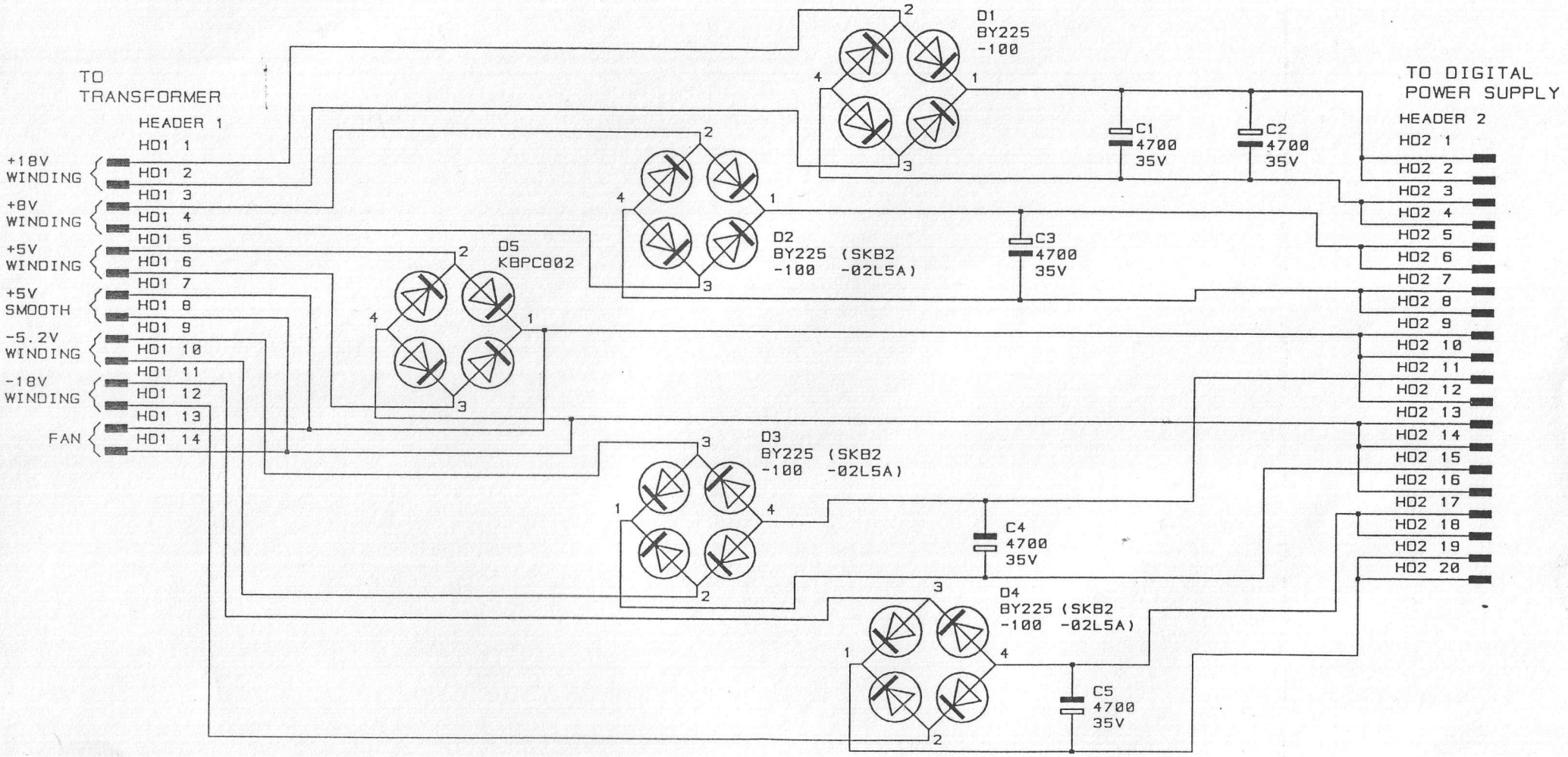


Figure 22 - Rectifier and Smoothing (PSU1) Circuit Diagram

Chapter 6.16

INTERNAL INTERFACES

1 INTRODUCTION

The STR8212 has a number of buses connecting all the digital sub-system and also going to the analogue sub-section as shown in Figure 1. This network is used for the transfer of digital control, clock and information signals around the radio. The Data, Address and Control Signal buses operating between the Controller, the Controller Interface and the optional IEEE 488 boards use the standard 68000 bus protocol. It should, however, be noted that the data and address buses are not buffered between the 68000 and the other two boards.

Description is given with reference to the following drawings:

- Figure 1 STR8212 Data Bus Diagram
- Figure 2 Data Bus Diagram Showing Detail of Controller Interface
- Figure 3 Digitised Signal Path Control and Timing Diagram

2 INTERFACE DESCRIPTION

The description of the Internal Interfaces is given under the following headings:

- DSP Interfaces Paragraph 2.1
- ADC and DAC/Sequencer Interfaces Paragraph 2.2
- Keyboard and Display Interfaces Paragraph 2.3
- Serial Interfaces from the Controller Paragraph 2.4

2.1 DSP Interfaces

Details of the buffered data bus and control signal paths between the controller interface and the DSP modules are shown in Figure 3. The data bus is 8 bits wide and bi-directional. The control signals from the controller interface comprise chip select lines to enable the addressed DSP and a three bit address bus which the DSP uses to differentiate between low, med, high data bytes and control data. When the DSP is sending data back to the controller it activates the IRQ5 line and the controller receives the information via its interrupt routines. The message content to and from each DSP is clearly shown in Figure 3. The ADC and DSP chips pass the digitised signal to each other along a Synchronous Serial Interface (SSI). The SSI inputs to each DSP are also available as an option in digital format via optical fibre connectors on the back of the radio.

2.2 ADC and DAC/Sequencer Interfaces

The ADC and DAC/Sequencer boards form the beginning and end of the digitised signal path. The ADC receives the 2nd IF analogue signal from the IF module at its input and feeds DSP1A with a digitised baseband IF. The TSTEN and TSTVAL/TSTPASS lines between the controller interface and the ADC (shown in Figure 2) are the BITE enable and BITE result lines respectively. The PMRDF FIRST and SHIFT lines are not currently in use. Both the ADC and the DAC/Sequencer receive their main clocks directly from the Reference module, 80 MHz for the ADC and 40 MHz for the DAC/Sequencer.

The control and timing details between the ADC, DAC/Sequencer and DSP chips are shown in more detail on Figure 3. The ADC generates PMRDF word sync, PMRDF frame sync and

erial clock pulses which go to the DAC/Sequencer. The DAC/Sequencer buffers the serial clock (a data clock running at 5 MHz) before distributing it to each of the DSP chips. The PMRDF frame sync pulse is used to control the sequencer which generates the sample clock signal (an inverted and buffered form of PMRDF frame sync) and the DSP frame sync signals. These are fed to each DSP chip. The sequencer outputs are also used to control the DAC.

The data bus and control signals from the controller interface to the DAC/Sequencer allow the controller to send a six bit word to the sequencer at power up to select the correct sequencer program. The DAC provides the analogue signals to the Line and external speaker outputs and the front panel speaker. The DAC/Sequencer board also provides the volume control for the front panel speaker.

2.3 Keyboard and Display Interfaces

The keyboard and display interfaces are shown in more detail on Figure 2. The keyboard lines transmit the switch matrix to the controller interface where a scanner interprets the matrix to find out which key has been pressed. The display interface consists of a serial bus to each of the three LCD drivers and is described in more detail in Chapter 6.12 - Front Panel Assembly.

2.4 Serial Interfaces from the Controller

The controller communicates with various modules in the STR8212 via a serial interface bus. This bus is shown in more detail on Figure 2 and comprises three parts, the serial clock, the serial data and the load lines. From the Controller Interface board there are eight load signals, six of which pass through the Interface module on route to the analogue sub-section, one goes to the ADC module and one to the keyboard. The serial clock and serial data are each single lines from the Controller Interface board to the Interface module, ADC module and the keyboard. In the Interface module the serial clock and serial data lines are each split into two, one for the fast path and one for the slow path as the filtering requirements are different for the two frequencies involved.

There are seven serial interfaces operated by the controller. They all use the same 32-bit parallel to serial shift register (located on the Controller Interface board) and therefore only one can be active at any time. Because of this there is a priority service order for handling the interfaces. If more than one interface requests a change during the same program loop then they are handled in the following order:

B	Synthesiser frequency (LO1 module)
G	Synthesiser BITE control (LO1 module)
C	PMRDF (ADC module)
E	Filter Bank (Sub-octave filter module)
A	RF Attenuator and RF/IF/Noise source control (RF module)
D	IF Attenuator and roofing filter control (IF module)
F	LED interface (Keyboard)

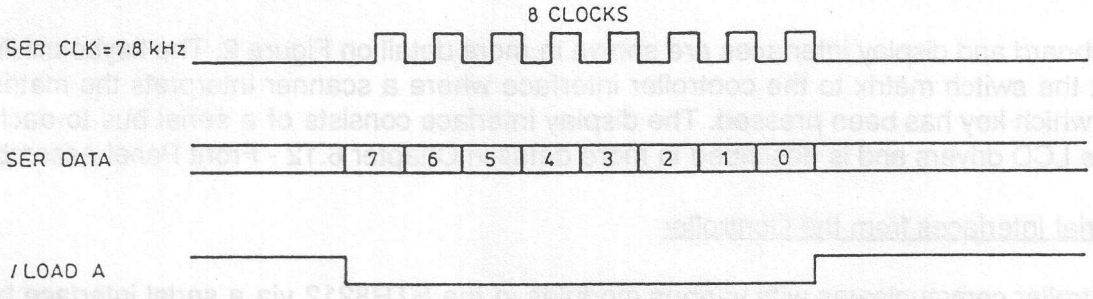
The controller identifies each interface by a separate address and these are interpreted by the Controller Interface board into individual load pulses. The amount of information being transmitted varies from 8 to 32 bits depending upon the interface. The speed of the data transmission is controlled by a clock line and this has two speeds, slow (7.8 kHz) and fast (500 kHz). The clock does not run continuously. The three lines (clock, data and load pulse) start synchronously triggered by a write to the hardware address by the controller.

2.4.1 Serial A

The serial A interface communicates with the RF module using 8 data bits with a slow clock. The eight data bits are allocated as follows:

0..3 - RF ATTN
4 - Noise source
5 - RF/IF Source
6 - RF Mute
7 - Source on

The source values are used during off-line BITE only. The RF ATTN bits give the number of the nine 5 dB step intervals allowed to give a range of 0 to 45 dB of attenuation.



SERIAL A TIMING DIAGRAM

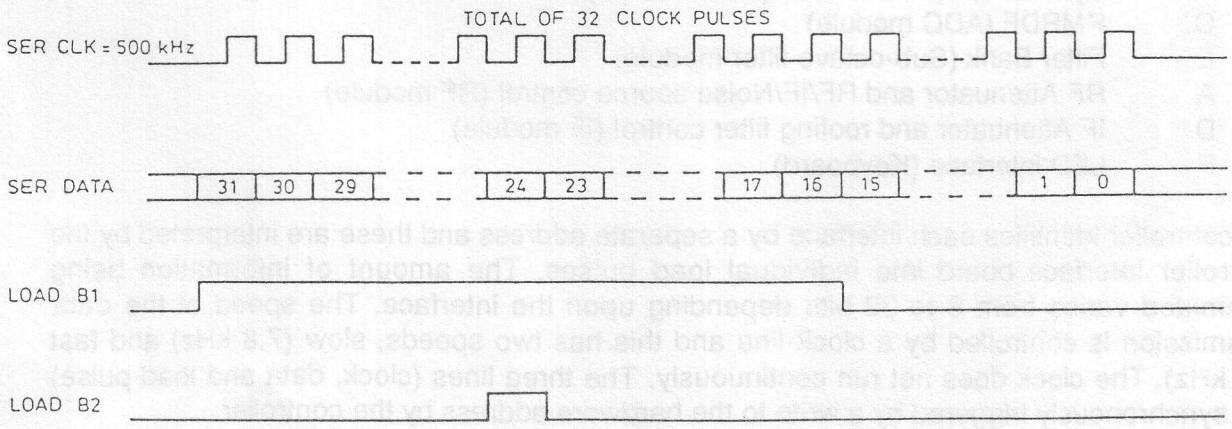
2.4.2 Serial B

The serial B interface communicates with the Synthesiser 1 module using 32 data bits with a fast clock. It is the only interface using the full 32 bits and therefore requires two load pulses as shown in the timing diagram. The data bits are allocated as follows:

0..19 - Hz part Synthesiser Frequency
20..31 - MHz part of Synthesiser Frequency

The actual frequency sent to the synthesiser is dependent upon the mode selected.

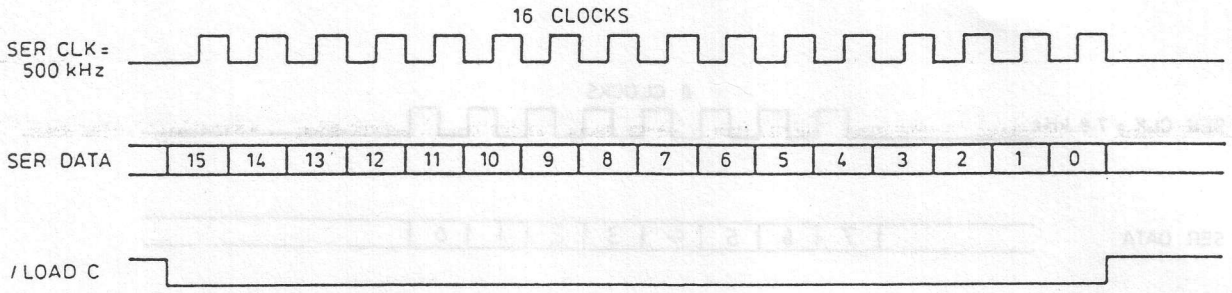
AM/FM/CW Synthesiser Frequency = Displayed Frequency + 50 kHz
USB Synthesiser Frequency = Displayed Frequency+50 kHz+(BW/2)+300 Hz-BFO
LSB Synthesiser Frequency = Displayed Frequency+50 kHz-(BW/2)-300 Hz+BFO



SERIAL B TIMING DIAGRAM

.3 Serial C

This is reserved for data transfer to the PMRDF in the ADC module, however it is not enabled in the current radio configuration.



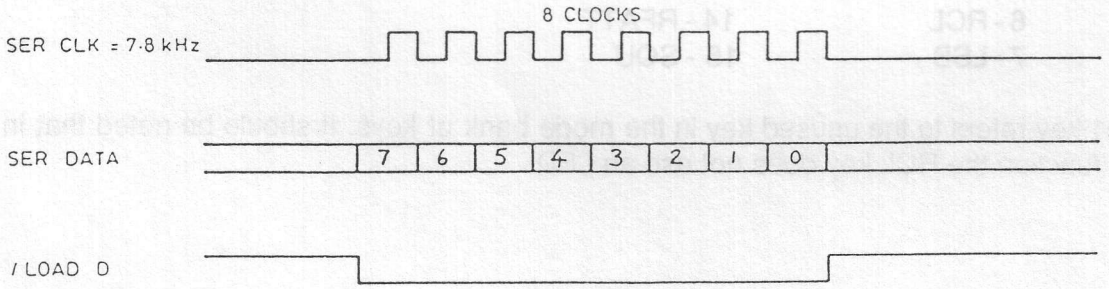
SERIAL C TIMING DIAGRAM

2.4.4 Serial D

This is an 8 bit data transfer to the IF module using the slow clock. The data bits are allocated as follows:

0..6 - IF ATTN
7 - IF optional selectable roofing filter

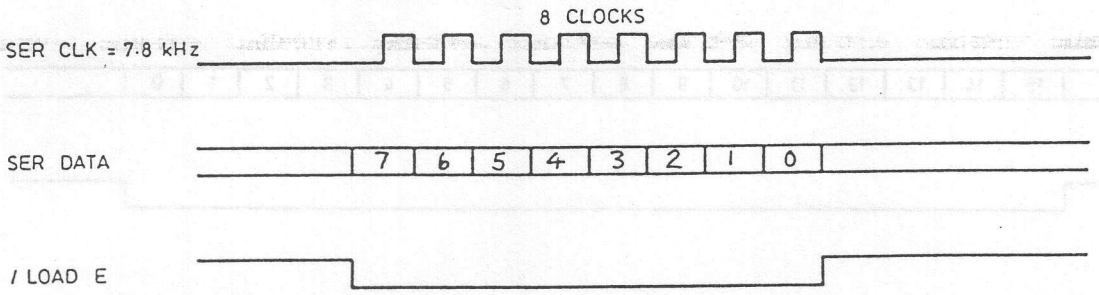
The seven bit IF ATTN word gives one of forty discrete values between 0 and 7F. The hex values are non-linear, however they result in approximately 1dB attenuation steps in the signal level into the DSP.



SERIAL D TIMING DIAGRAM

2.4.5 Serial E

The serial E interface communicates with the optional suboctave filter module using 8 data bits with a slow clock. The eight data bits form a word that selects which of the filter banks is most suitable to the operating frequency. The suboctave filter module is not fitted in the current radio configuration.



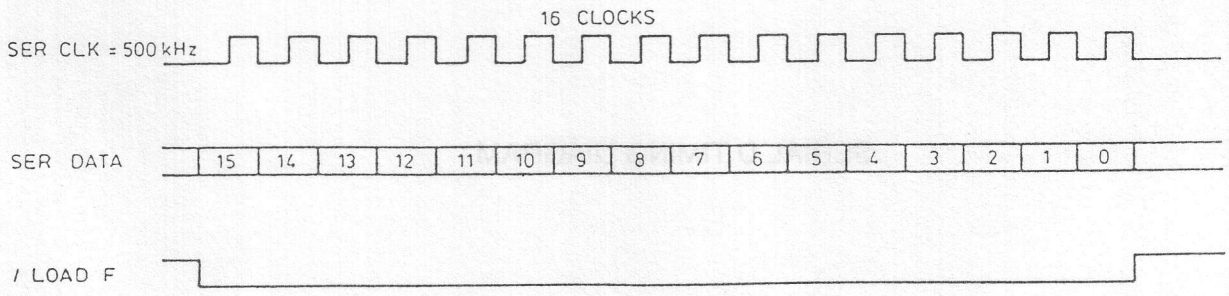
SERIAL E TIMING DIAGRAM

2.4.6 Serial F

The serial F interface communicates with the LEDs on the front panel using 16 data bits with a fast clock. The data bits are allocated as follows:

0 - MODE1	8 - CW
1 - USB	9 - AGC
2 - FM	10 - SCAN
3 - DATA	11 - FAST
4 - ISB	12 - MED
5 - AM	13 - SLOW
6 - RCL	14 - RFATT
7 - LSB	15 - SQU

The mode1 key refers to the unused key in the mode bank of keys. It should be noted that in its current function the RCL key does not use an LED.



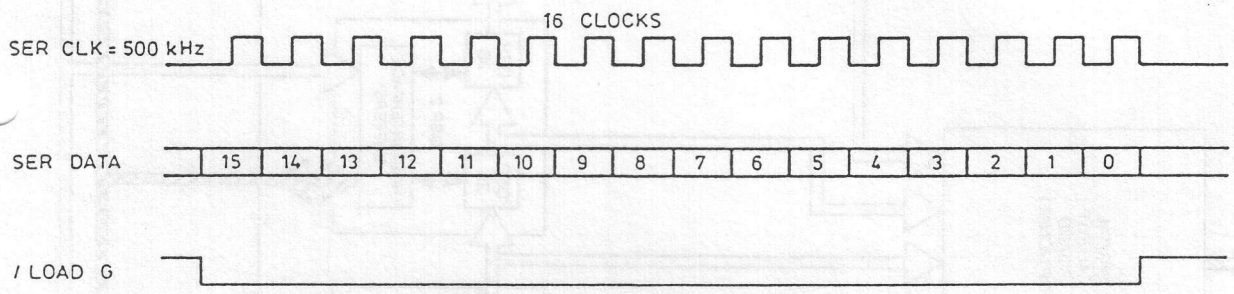
SERIAL F TIMING DIAGRAM

.4.7 Serial G

The serial G interface communicates with the Synthesiser 1 module using 16 data bits with a fast clock. The data bits are allocated as follows:

0..6 - DAC Voltage
7 - BITE ON
8.15 - Not Used

The BITE ON bit indicates to the synthesiser that it is currently undergoing its own test routine. The DAC voltage word is only used during this time for assessing the linearity of the four VCO bands.



SERIAL G TIMING DIAGRAM

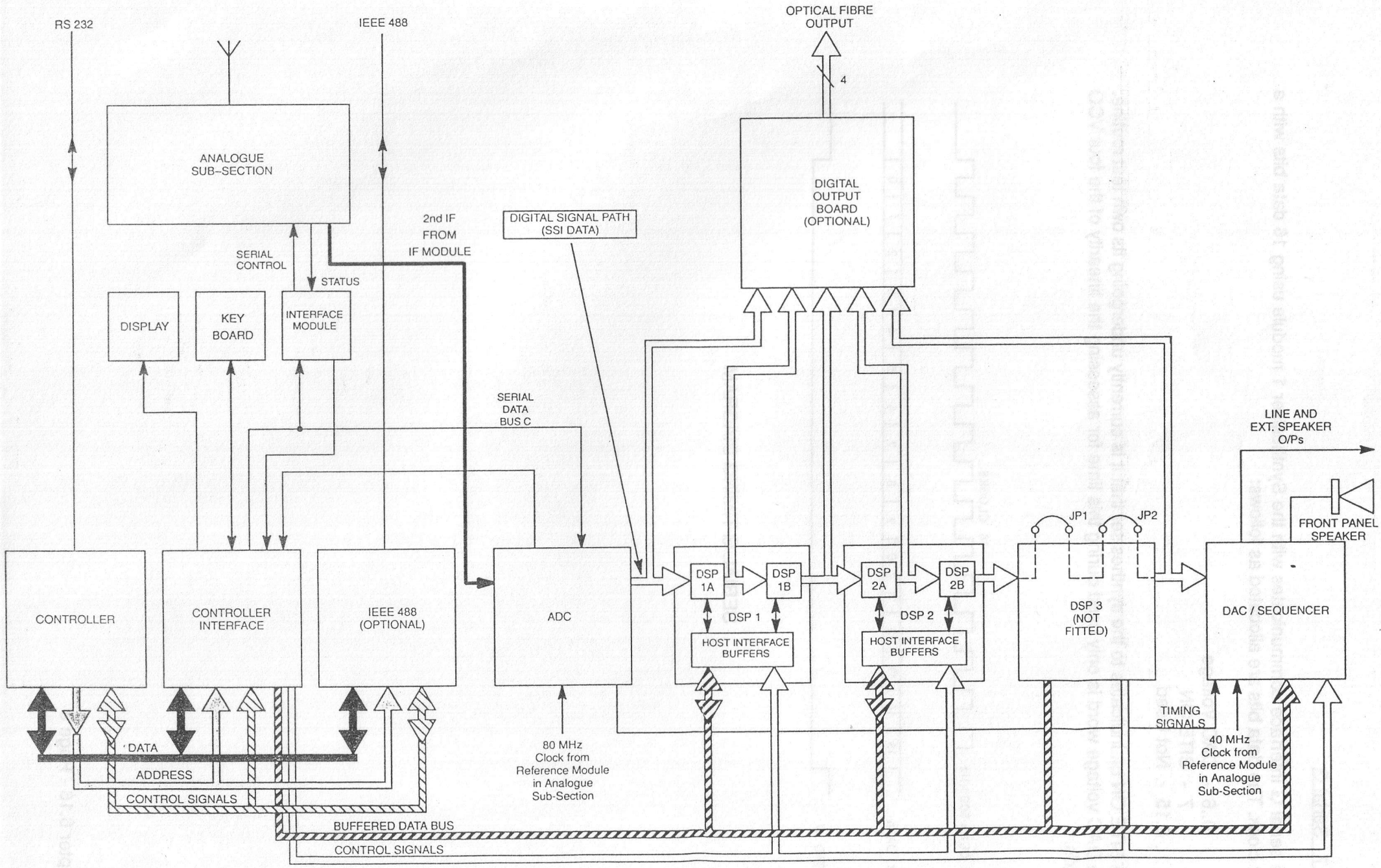


Figure 1. STR8212 Data Bus Diagram

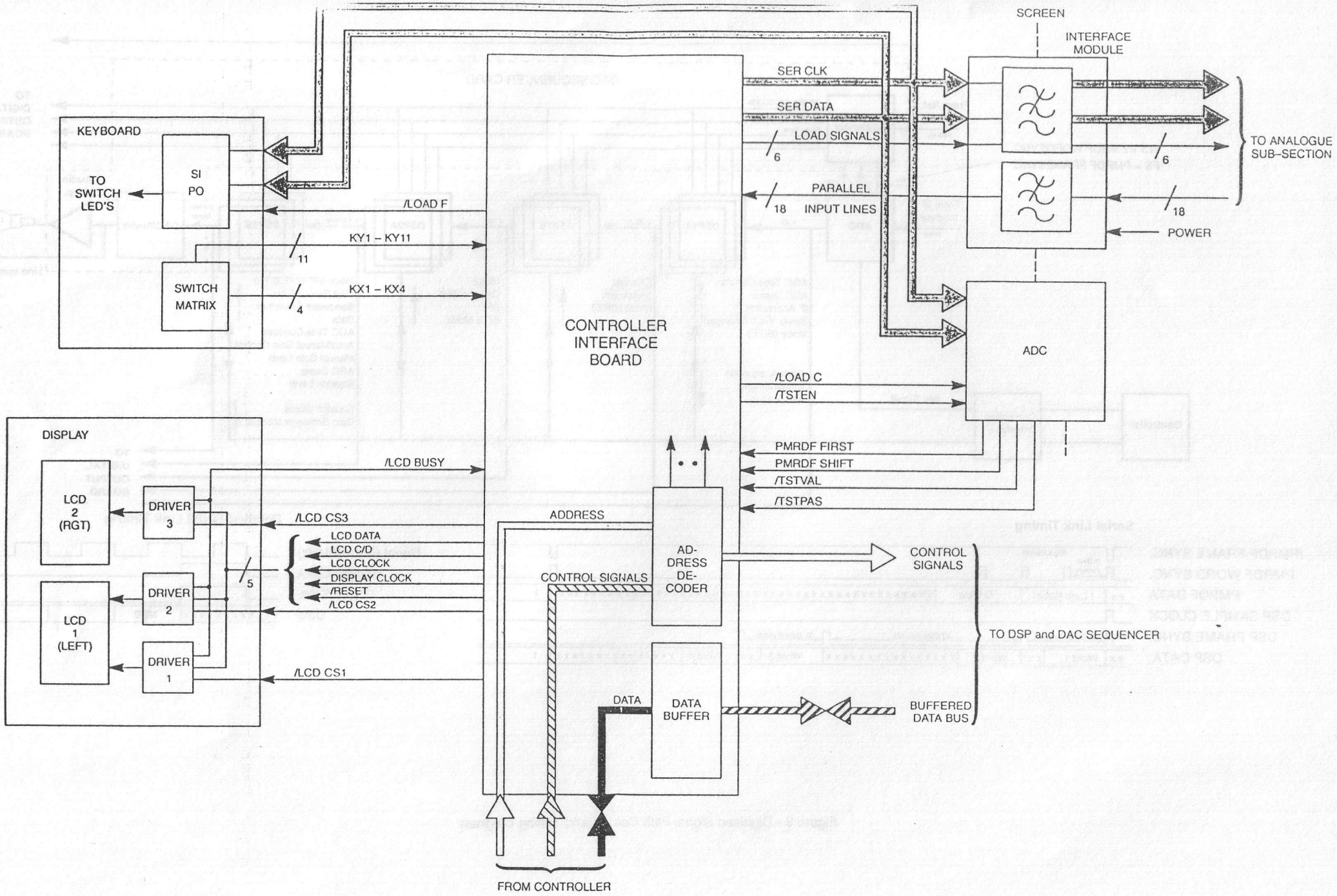


Figure 2 Data Bus Diagram Showing Detail of Controller Interface

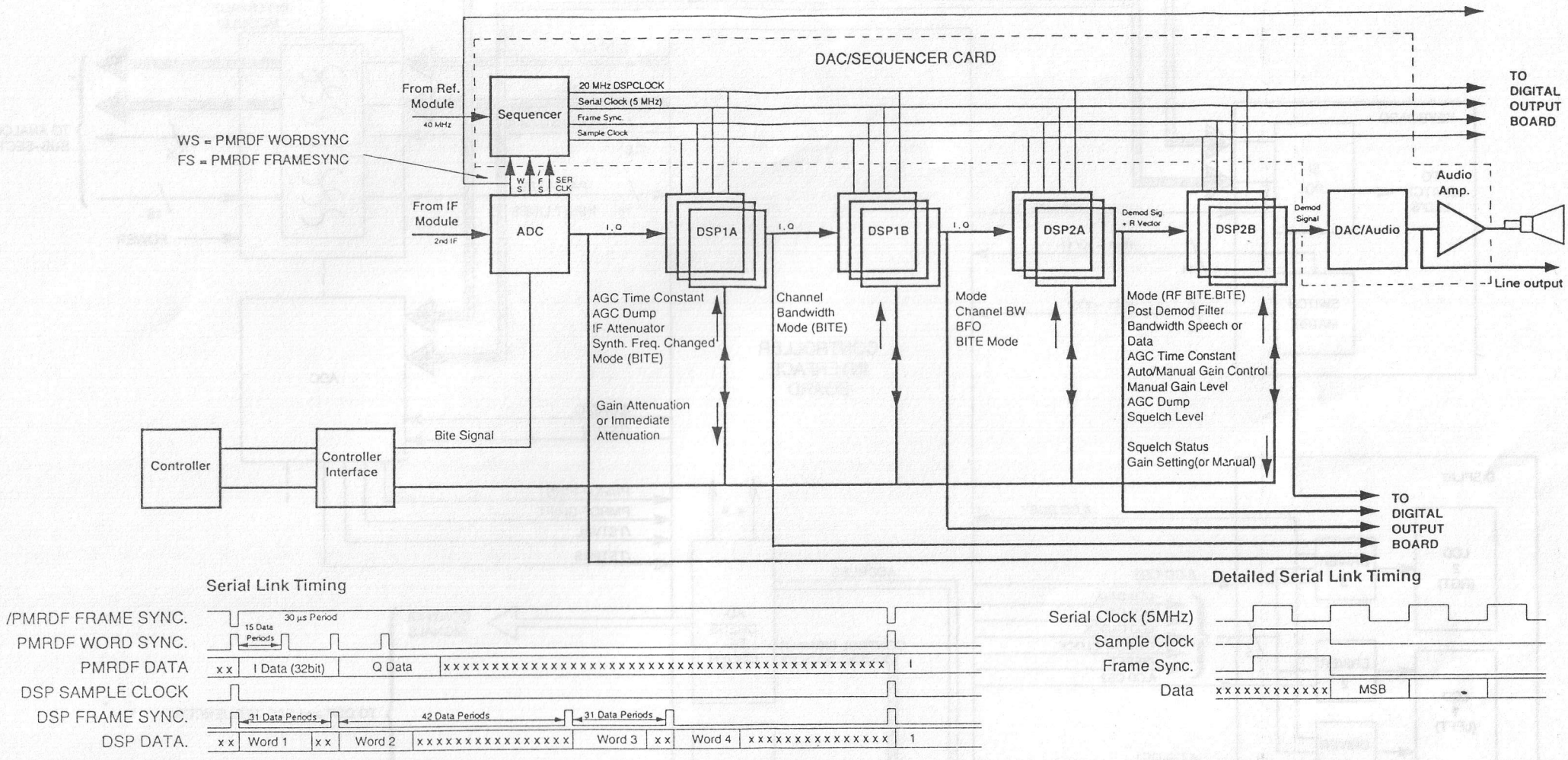


Figure 3 - Digitised Signal Path Control and Timing Diagram

APPENDIX A
TEST LEAD
AND TEST ADAPTORS

Appendix A

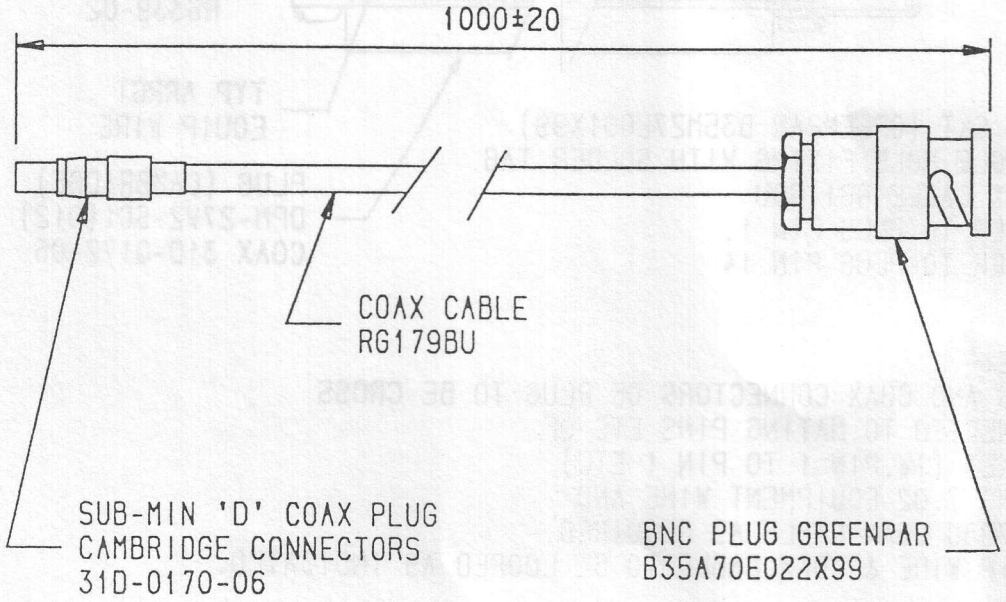
TEST LEAD AND TEST ADAPTORS

1 INTRODUCTION

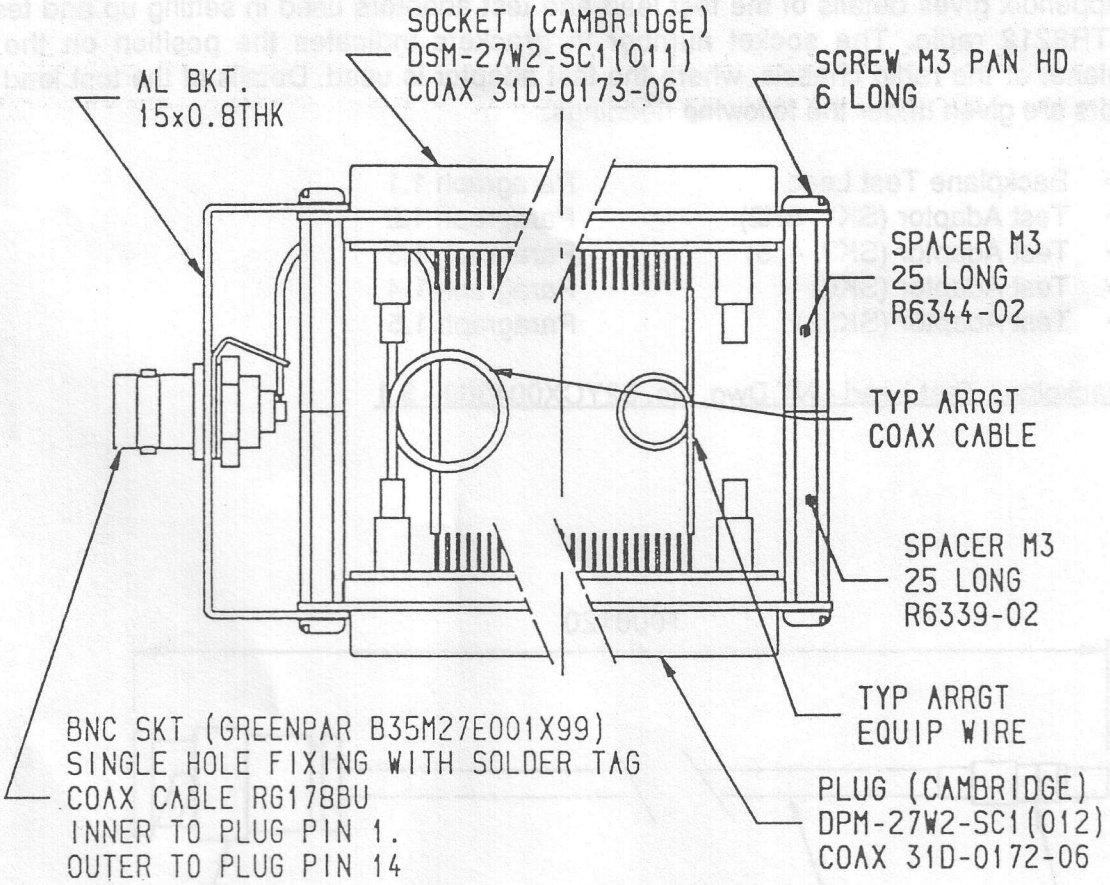
This appendix gives details of the test lead and test adaptors used in setting up and testing the STR8212 radio. The socket number in brackets indicates the position on the RF Backplane, or the radio chassis, where the test adaptor is used. Details of the test lead and adaptors are given under the following headings:

- Backplane Test Lead — Paragraph 1.1
- Test Adaptor (SK1, SK2) — Paragraph 1.2
- Test Adaptor (SK3, 4, 5) — Paragraph 1.3
- Test Adaptor (SK6) — Paragraph 1.4
- Test Adaptor (SK52) — Paragraph 1.5

1.1 Backplane Test Lead - NT Dwg. No. 52YCX004369 - 3.1

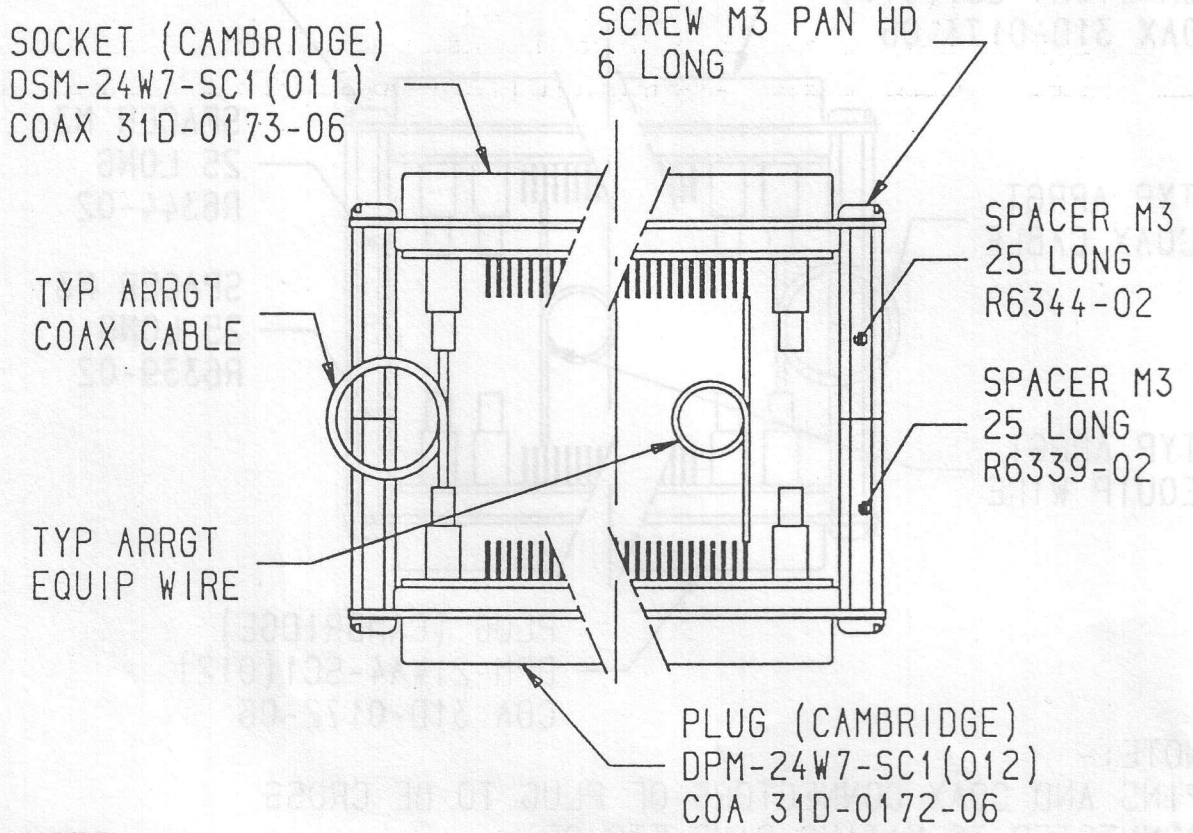


1.2 Test Adaptor (SK1, SK2) - NT Dwg. No. 52YCX004365 - 3.1



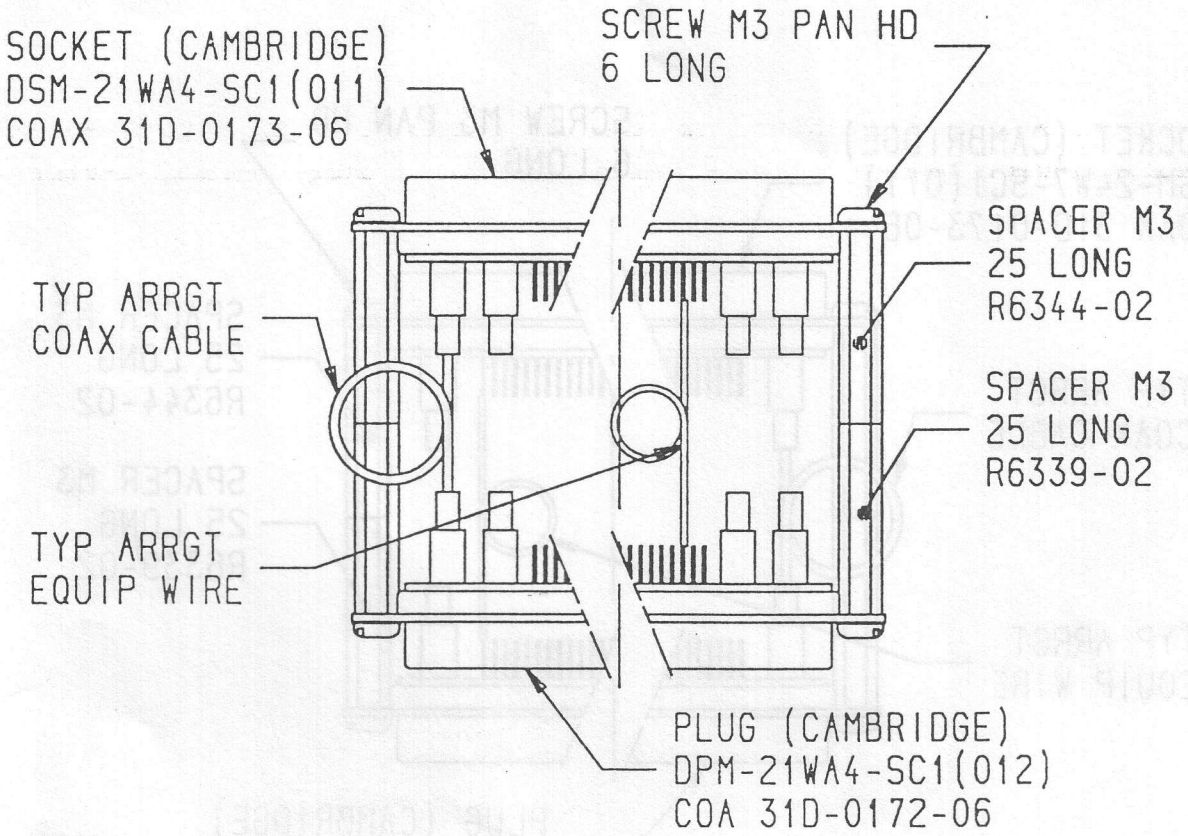
NOTE:-
PINS AND COAX CONNECTORS OF PLUG TO BE CROSS CONNECTED TO MATING PINS ETC OF SOCKET (ie.PIN 1 TO PIN 1 ETC)
USING 7.02 EQUIPMENT WIRE AND RG178BU COAX CABLE AS REQUIRED.
EQUIP WIRE & COAX CABLE TO BE LOOPED AS INDICATED.

1.3 Test Adaptor (SK3, 4, 5) - NT Dwg. No. 52YCX004366 - 3.1



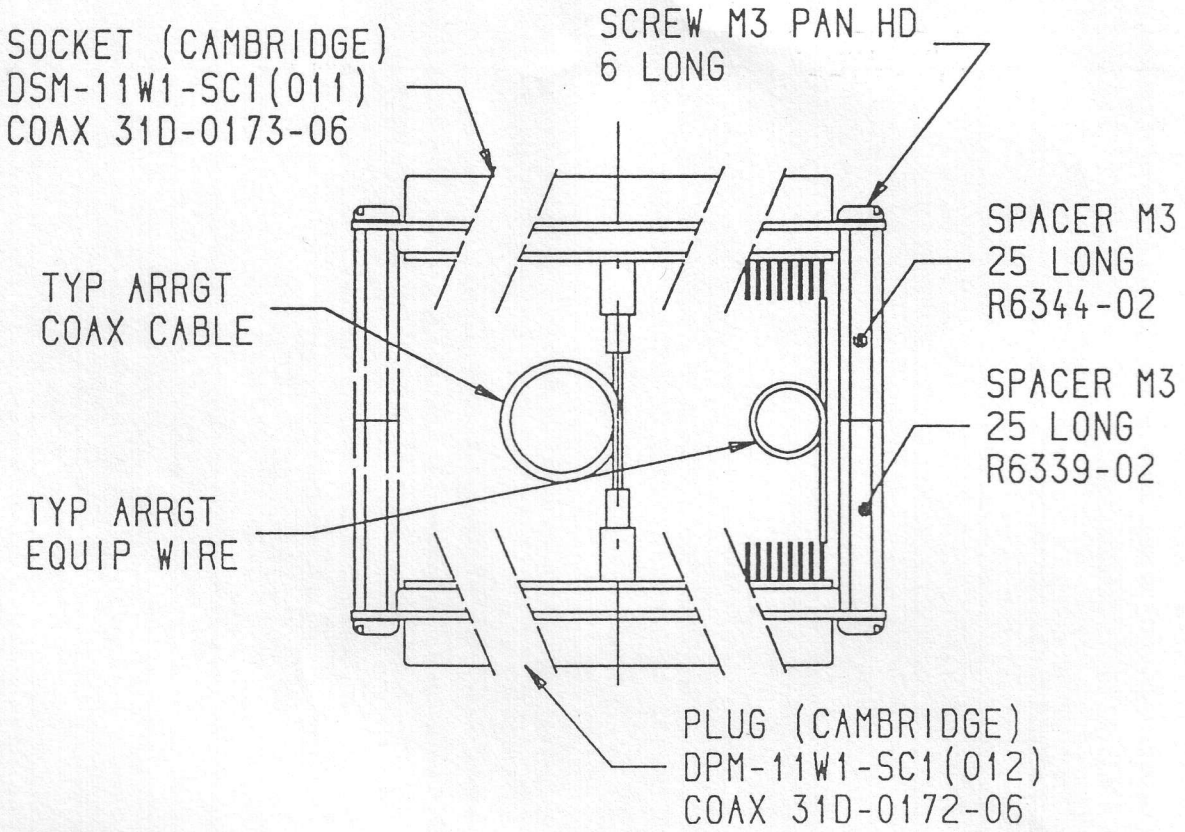
NOTE:-
PINS AND COAX CONNECTORS OF PLUG TO BE CROSS CONNECTED TO MATING PINS ETC OF SOCKET (ie.PIN 1 TO PIN 1 ETC)
USING 7.02 EQUIPMENT WIRE AND RG178BU COAX CABLE AS REQUIRED.
EQUIP WIRE & COAX CABLE TO BE LOOPED AS INDICATED.

1.4 Test Adaptor (SK6) - NT Dwg. No.52YCX004367



NOTE:-
PINS AND COAX CONNECTORS OF PLUG TO BE CROSS CONNECTED TO MATING PINS ETC OF SOCKET (ie.PIN 1 TO PIN 1 ETC)
USING 7.02 EQUIPMENT WIRE AND RG178BU COAX CABLE AS REQUIRED.
EQUIP WIRE & COAX CABLE TO BE LOOPED AS INDICATED.

1.5 Test Adaptor (SK52) - NT Dwg. No. 52YCX004368 - 3.1



NOTE:-
PINS AND COAX CONNECTORS OF PLUG TO BE CROSS CONNECTED TO MATING PINS ETC OF SOCKET (ie.PIN 1 TO PIN 1 ETC)
USING 7.02 EQUIPMENT WIRE AND RG178BU COAX CABLE AS REQUIRED.
EQUIP WIRE & COAX CABLE TO BE LOOPED AS INDICATED.

APPENDIX B
PRODUCT ACCEPTANCE TEST SPECIFICATION FOR STR8212

CONTENTS

1.0 INTRODUCTION

1.1 Scope of document
1.2 General Description
1.3 Related Documents
1.4 Drawings List
1.5 Circuit Diagram
1.6 Safety Requirements
1.7 Use of Conventional True Values
1.8 Essential Conditions of Test
1.9 Test Documentation

2.0 POWER REQUIREMENTS

3.0 PERFORMANCE REQUIREMENTS

3.1 Receiver Outputs
3.2 Internal Reference Frequency Accuracies
3.3 Performance Tests

4.0 SPECIAL TEST METHODS

5.0 TEST RESULTS SHEETS

Figure 1 STR8212 Simplified Block Diagram

1.0 Introduction

1.1 Scope of Document

The purpose of this document is to allow the major performance characteristics of the STR8212 HF Receiver to be verified. A general set of outline tests are provided which may be used to demonstrate contractual compliance.

1.2 General Description

The STR8212 HF Receiver is a modular high performance receiver covering frequencies between 50kHz and 40MHz. It makes extensive use of Digital Signal Processing and embodies a very high performance A to D convertor and digitally implemented demodulation, AGC and channel filtering for exceptional repeatability of key performance parameters.

The receiver is a double superhet design with a very low second i.f. at 50kHz.The signal is then digitised with 24 bit usable resolution. Conversion to baseband, channel filtering, IF AGC control, demodulation, Audio AGC and post demodulation filtering are performed digitally. The signal is finally converted back to the analogue domain for the generation of audio outputs.

1.3 Design and Associated Specification

Reference should be made to:
(i) STR8212 Quality Plan MS 1532/PQ
(ii) RMD Engineering Instructions and Procedures.

1.4 Drawings List

The Drawing List for this equipment is STR8212 - 1.1.

1.5 Block Diagram

A block diagram showing the main functional blocks within the Receiver is given in Figure 1.

1.6 Safety requirements

ALL TESTING TO THIS SPECIFICATION IS CARRIED OUT WITHOUT REMOVAL OF THE COVERS. THE VENTS BENEATH THE RECEIVER MUST NOT BE OBSTRUCTED DURING TESTING. READ THE PRODUCT SAFETY SHEET IN APPENDIX 1 BEFORE COMMENCING TESTS.

CAUTION: HAZARDOUS VOLTAGES EXIST WITHIN THIS UNIT !

1.7 Use of conventional true values

All values given in this specification are true RMS values unless otherwise stated.
All RF voltages are the terminated (PD) levels which apply in a 50 Ohm system.
All audio voltages are the terminated (PD) levels which apply in a 600 Ohm system.

1.8 Essential conditions of test

The performance tests defined in this specification should be carried out at room temperature.

Before applying power to the receiver, ensure that the mains voltage selector, which is integral with the mains inlet on the rear panel, is set to 240V.
Also check that the fuse holder contains a 1.25 Amp antisurge fuse.

1.9 Test Documentation

Documentation for tests performed on equipment supplied to this Specification shall have the form shown in Section 5.
The type, serial number and calibration status of all test equipment used shall be recorded.

2.0 Power Requirements

For testing, the receiver will require a 240V, 50Hz AC supply at approximately 0.5A.
Alternatively, the receiver may be tested using 110V or 220V (+/-10%), 47-63Hz AC supplies.

3.0 Performance Requirements

3.1 Receiver Outputs

The following receiver audio output specifications apply with an applied antenna signal within the operational tuning range of the receiver, at levels above the AGC threshold and with AGC operational. The applied signal should also be set up so that its power falls within the bandwidth of the receiver.

3.1.1 Audio Line Output

The audio output signal at 800Hz shall be at the factory preset level of +2dBm +/-2dB into a 600 ohm balanced load.

3.1.2 ISB Line Output

The audio output signal at 800Hz shall be at a level of +2dBm +/-2dB into a 600 ohm balanced load.

3.1.3 External Speaker Output

The audio output power delivered into an 8 ohm load shall exceed 0.5 Watts.

3.1.4 Headphone Level

The audio output power delivered into an 8 ohm load connected to the front panel jack socket, shall exceed 0.5 Watts.
Note that the internal speaker is disabled for this test.

3.2 Internal Reference Frequency Accuracies

With the receiver tuned to any operating frequency within its range, the internally generated Reference and Local Oscillator frequencies shall meet the following accuracy specification:

REF	:	10.000000 MHz +/- 5Hz
LO2	:	70.000000 MHz +/- 35Hz
LO1	:	(Indicated tuned frequency plus 70.05)MHz +/- 45Hz

3.3 Sensitivity

(i) Frequency Range 100kHz to 40 MHz:
With the receiver in USB mode and in a 3 kHz receiver bandwidth, the receiver shall give at least a 10 dB signal+noise-to-noise ratio for a signal at a level of -117 dBm at the receiver antenna input. (Note that the receiver specification requires -115.5dBm for a 10dB signal to noise ratio.) See section 4.2.1 for conditions of test.

(ii) Frequency Range 50kHz to 100 kHz:
With the receiver in USB mode and in a 3 kHz receiver bandwidth, the receiver shall give at least a 10 dB signal+noise-to-noise ratio for a signal at a level of -107 dBm at the receiver antenna input, at a frequency 1kHz higher than the receiver tuned frequency.

3.4 RF Attenuator Control

The RF Attenuator shall have incremental steps of attenuation within the limits below:

5	+/-0.5dB
10	+3.5 / -0.5dB
15	+4 / -1dB
20	+4 / -1dB
25	+4.5 / -1.5dB
30	+4 / -1dB
35	+4.5 / -1.5dB
40	+4.5 / -1.5dB
45	+5 / -2dB

3.5 In-band Intermodulation (third order)

This parameter is defined with AGC disabled. The test tones shall be such that both they and their third-order products fall within the receiver first IF passband (ie within +/-7 kHz of the tuned frequency).

The test tone levels shall be -7dBm per tone at the antenna connector. The intermodulation products generated within the receiver shall not exceed the following limit with respect to the level of each original tone at the receiver output:

Limit: -52dBmax

This corresponds to an in-band Third Order Intercept point of

(-7 + 52/2) dBm

ie., +19dBm.

3.6 Out of band Intermodulation (third order)

This parameter is defined with AGC disabled. The test tones shall be such that they lie at least 20 kHz from the tuned frequency and their third-order products fall within the receiver passband (ie within +/-7 kHz of the tuned frequency).
This test shall be performed for test tones both above and below the receiver passband.

Intermodulation products limits are defined with respect to a reference tone at the receiver tuned frequency at a power level of -68dBm at the antenna connector. AGC must be turned on to establish the correct receiver gain with a single reference tone present. AGC is then to be disabled and the audio level of the reference tone is noted.

The level of the offset frequency test tones at the antenna connector is increased until the intermodulation product generated in the receiver passband equals the the level of the reference tone output. The level of each of the intermodulating input tones (X) shall be at least 60dB above the level of the reference RF input tone (-68dBm).

The out-of-band Third Order Intercept point can then be calculated as follows:

$$ICP_3 = X + (X+68)/2 \text{ dBm}$$

This specification limit is therefore equivalent to +22 dBm.

3.7. Blocking

The receiver output level for a wanted signal at a level of -53dBm at the antenna connector shall not be reduced by more than the limit stated below due to blocking arising from an unwanted signal at least 20 kHz from the tuned frequency at a level of +7dBm at the antenna connector.

Limit: 3dB max

3.8 Second Image Rejection

The response to signals spaced 100 kHz above the receiver tuned frequency shall be at 91dB below the response to wanted signals. See paragraph 4.2.5 for conditions of test.

Limit: 91 dB min

3.9 First Image Rejection

The response to signals spaced 140.1 MHz above the receiver tuned frequency shall be at least 91dB below the response to wanted signals. See paragraph 4.2.5 for conditions of test.

Limit: 91 dB min

3.10 IF Rejection

The response to a signal at 70.05MHz shall be at least 91dB below the response to wanted signals. See paragraph 4.2.5 for conditions of test.

Limit: 91 dB min

3.11 Reciprocal Mixing (phase noise)

Any unwanted signal at a level of 96dBμV and separated by at least 20kHz from the wanted frequency shall produce a noise power at the audio output which when measured with a 3kHz receiver bandwidth selected is less than the power produced by a 1μV signal at the wanted frequency.
In order to perform this measurement the test source must have adequate phase noise and spectral purity performance.
In order to establish radio performance the following receiver settings are considered to be representative:

MODE	BAND-WIDTH	AGC	AGC SPEED	BFO	DATA
CW	3.0	ON	MED	-0.80	OFF

Further receiver frequencies sufficient to establish the required performance are:

CHANNEL	RECEIVER FREQUENCY (kHz)	SIG GEN FREQUENCY (kHz)
4	510.000	530.000
6	9790.000	9810.000
7	11320.000	11340.000
8	13140.000	13160.000
9	19500.000	19520.000
10	20940.000	20960.000
11	29820.000	29840.000
12	30120.000	30140.000
15	39975.000	39995.000

An Rf signal of -107dBm is applied to the receiver input and the audio output level is noted. The AGC is disabled and the receiver is off-tuned by 20kHz. The RF signal level is increased until the noted audio output level is reached. The increase in RF signal level shall exceed the stated limit.

Limit: 97dB min

4.0 Special Test Methods

4.1 Test Frequencies

In order to provide a suitable selection of frequencies and consistent test documentation the following standardised test frequencies have been defined:

CHAN	FREQUENCY	MODE	BAND-WIDTH	AGC	AGC SPEED	BFO	DATA LED
1	50.000	CW	3.0	ON	MED	-0.80	OFF
2	98.000	CW	3.0	ON	MED	-0.80	OFF
3	146.000	CW	3.0	ON	MED	-0.80	OFF
4	510.000	CW	3.0	ON	MED	-0.80	OFF
5	4950.000	CW	3.0	ON	MED	-0.80	OFF
6	9790.000	CW	3.0	ON	MED	-0.80	OFF
7	11320.000	CW	3.0	ON	MED	-0.80	OFF
8	13140.000	CW	3.0	ON	MED	-0.80	OFF
9	19500.000	CW	3.0	ON	MED	-0.80	OFF
10	20940.000	CW	3.0	ON	MED	-0.80	OFF
11	29820.000	CW	3.0	ON	MED	-0.80	OFF
12	30120.000	CW	3.0	ON	MED	-0.80	OFF
13	34250.000	CW	3.0	ON	MED	-0.80	OFF
14	37580.000	CW	3.0	ON	MED	-0.80	OFF
15	39975.000	CW	3.0	ON	MED	-0.80	OFF

4.2 Mandatory Test Methods

In order to satisfactorily perform the measurements described in the previous section the following test techniques are mandatory:

4.2.1 For sensitivity measurements, the audio output of the receiver will contain high frequency components from the digital subsystem and thus a single section low pass filter is required at the line output.

4.2.2 When combining multiple signals for, e.g., cross modulation and intermodulation tests, there must be sufficient inherent isolation in the test setup to prevent externally generated products from causing erroneous readings.

4.2.3 In order to measure reciprocal mixing to the limits required, the test source must have a phase noise of not worse than -138 dBc/Hz at 20 kHz offset , at frequencies below 40 MHz.

4.2.4 When measuring in-band intermodulation it is permissible to select a narrow bandwidth to reject the test tones, thereby permitting a conventional audio analyser to be used to measure the intermodulation products which lie within the receiver bandwidth.

This method is made possible by the use of digital signal processing for the bandwidth-defining filters and subsequent processing stages of the radio, so that these stages cannot contribute significantly to IMD. This also means that the in-band IMD is independent of bandwidth selected.

4.2.5 Image and IF rejection measurements are performed by noting the audio output level for a -117dBm input signal at the receiver tuned frequency. The AGC is then disabled and a signal at the image or IF frequency is applied. The signal level is increased until the noted audio output level is reached.

5.0 Test Results Sheets

EQUIPMENT: STR8212 HF Receiver Assembly

DRAWING NO: STR8212

TEST EQUIPMENT MAKE / MODEL	REF. NUMBER	CAL. STATUS

COMMENTS:

SER. NO.	TESTER	DATE	AUDIT	VALIDATION

Clause	Test	Limits		Unit	Result	Comments
		Min	Max			
	Performance Tests					
3.1.1	Audio line output level	0	4	dBm		
3.1.2	ISB line output level	0	4	dBm		
3.1.3	External speaker level	0.5		Watts		
3.1.4	Headphone level	0.5		Watts		
3.2	Reference frequency accuracies: Radio tuned to 15 MHz					
	REF (10.000000MHz)	-5	+5	Hz		
	LO2 (70.000000MHz)	-35	+35	Hz		
	LO1 (85.050000MHz)	- 45	+ 45	Hz		
3.3(i)	Sensitivity					
	CH 5 4950 kHz	10		dB		
	CH 2 98 kHz	10		dB		
	CH 3 146 kHz	10		dB		
	CH 4 510 kHz	10		dB		
	CH 6 9790 kHz	10		dB		
	CH 8 13140 kHz	10		dB		
	CH 10 20940 kHz	10		dB		
	CH 13 34250 kHz	10		dB		
	CH 14 37580 kHz	10		dB		
	CH 15 39975 kHz	10		dB		

Clause	Test	Limits		Unit	Result	Comments
		Min	Max			
3.3(ii)	CH 1 50 kHz	10		dB		
3.4	RF attenuator Control: Cumulative attenuation					
	5dB	4.5		dB		
	10dB	9.5		dB		
	15dB	14		dB		
	20dB	19		dB		
	25dB	23.5		dB		
	30dB	29		dB		
	35dB	33.5		dB		
	40dB	38.5		dB		
	45 dB attenuation	43		dB		
3.5	In-band Intermodulation	52		dB		
3.6	Out of band Intermodulation Intercept point (for -ve offsets)					
	CH 7 11320 kHz	22		dB		
	CH 11 29820 kHz	22		dB		
	CH 15 39975 kHz	22		dB		
	(for +ve offsets)					
	CH 7 11320 kHz	22		dB		
3.7	Blocking Audio reduction at:					
	+ 20 kHz offset		3	dB		
	- 20 kHz offset		3	dB		
3.8	2nd Image Rejection	91		dB		

Clause	Test	Limits		Unit	Result	Comment
		Min	Max			
3.9	1st Image Rejection					
	CH 7 11320 kHz	91		dB		
	CH 2 98 kHz	91		dB		
	CH 15 39975 kHz	91		dB		
3.10	IF Rejection	91		dB		
3.11	Reciprocal Mixing					
	CH 4 510 kHz	97		dB		
	CH 6 9790 kHz	97		dB		
	CH 7 11320 kHz	97		dB		
	CH 8 13140 kHz	97		dB		
	CH 9 19500 kHz	97		dB		
	CH 10 20940 kHz	97		dB		
	CH 11 29820 kHz	97		dB		
	CH 12 30120 kHz	97		dB		
	CH 15 39975 kHz	97		dB		

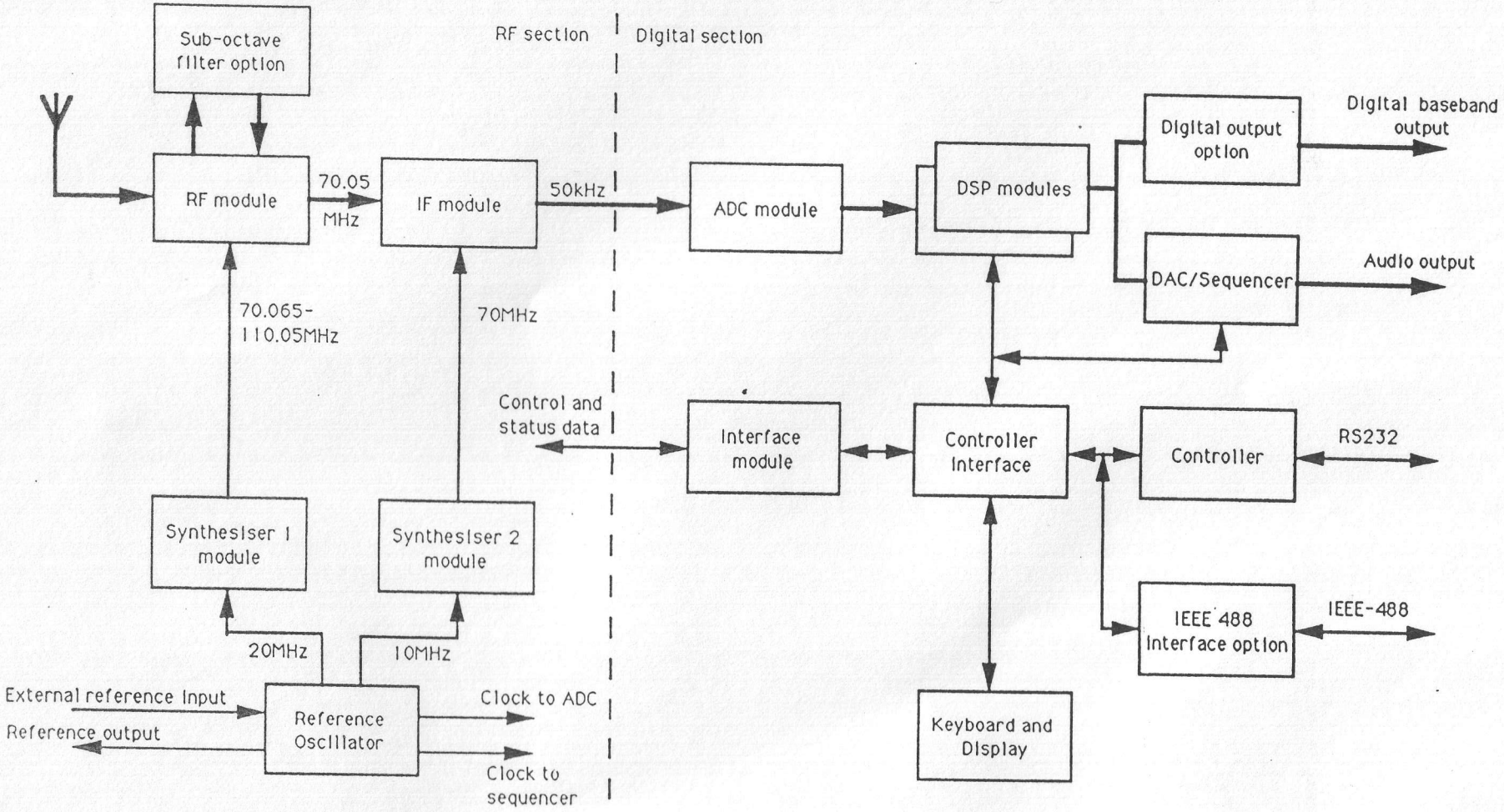


Figure 1 STR8212 SIMPLFIED BLOCK DIAGRAM