ALESIS
D4/DM5 Drum Modules Service Manual
V1.00
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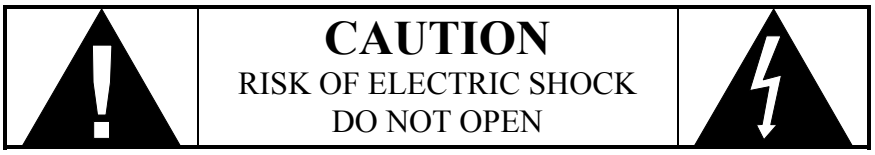
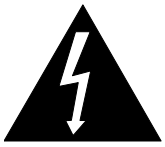
PREFACE

This document is intended to assist the service technician in the operation, maintenance and repair of the D4/DM5 Drum Modules. Together with the D4 and DM5 Reference Manuals, this document provides a complete description of the functionality and serviceability of the D4 and DM5. Any comments or suggestions you may have pertaining to the document are welcome and encouraged.

WARNINGS

TO REDUCE THE RISK OF ELECTRIC SHOCK OR FIRE, DO NOT EXPOSE THIS PRODUCT TO WATER OR MOISTURE.





The arrowhead symbol on a lightning flash inside a triangle is intended to alert the user to the presence of un-insulated "dangerous voltage" within the enclosed product which may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point inside a triangle is intended to alert the user to the presence of important operating, maintenance and servicing instructions in the literature which accompanies the product.

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Carefully read the applicable items of the operating instructions and these safety suggestions before using this product. Use extra care to follow the warnings written on the product itself and in the operating instructions. Keep the operating instructions and safety suggestions for reference in the future.

1. Power Source. The product should only be connected to a power supply which is described either in the operating instructions or in markings on the product.

2. Power Cord Protection. AC power supply cords should be placed such that no one is likely to step on the cords and such that nothing will be placed on or against them.

3. Periods of Non-use. If the product is not used for any significant period of time, the product's AC power supply cord should be unplugged from the AC outlet.

4. Foreign Objects and Liquids. Take care not to allow liquids to spill or objects to fall into any openings of the product.

5. Water or Moisture. The product should not be used near any water or in moisture.

6. Heat. Do not place the product near heat sources such as stoves, heat registers, radiators or other heat producing equipment.

7. Ventilation. When installing the product, make sure that the product has adequate ventilation. Improperly ventilating the product may cause overheating, which may damage the product.

8. Mounting. The product should only be used with a rack which the manufacturer recommends. The combination of the product and rack should be moved carefully. Quick movements, excessive force or uneven surfaces may overturn the combination which may damage the product and rack combination.

9. Cleaning. The product should only be cleaned as the manufacturer recommends.

10. Service. The user should only attempt the limited service or upkeep specifically described in the operating instructions for the user. For any other service required, the product should be taken to an authorized service center as described in the operating instructions.

11. Damage to the Product. Qualified service personnel should service the unit in certain situations including without limitation when:
    a. Liquid has spilled or objects have fallen into the product,
    b. The product is exposed to water or excessive moisture,
    c. The AC power supply plug or cord is damaged,
    d. The product shows an inappropriate change in performance or does not operate normally, or
    e. The enclosure of the product has been damaged.

Table of Contents

1.00 General Descriptions

The D4 is a rather simple unit to repair, as the component count has been greatly reduced by the use of the DM3AG ASIC (Application Specific Integrated Circuit). The basic building blocks of the unit are the 8031 micro controller (which handles all basic unit functions such as triggers , LCD output, Keypad input, and MIDI I/O), sample generation circuits (ASIC, DAC, Analog switch, and output filter/buffers), and some miscellaneous support circuits such as system reset, battery backup, etc.

The DM5 (Alesis product code D5) is extremely similar in design, with the one major difference being the use of better DACs. This has required the addition of on extra IC {D56IFT ASIC} for the purpose of converting parallel data to a serial format and generating clock signals for use with the new DACs. In addition this IC consolidates several other functions previously performed by discreet logic such as memory map decoding and handling the highest order Mask ROM addressing lines. Please note that there are several main PC Board revisions, and some differences will be noticed from unit to unit. Reference designators refer to the D4 unless in brackets {D5 reference} or otherwise noted.

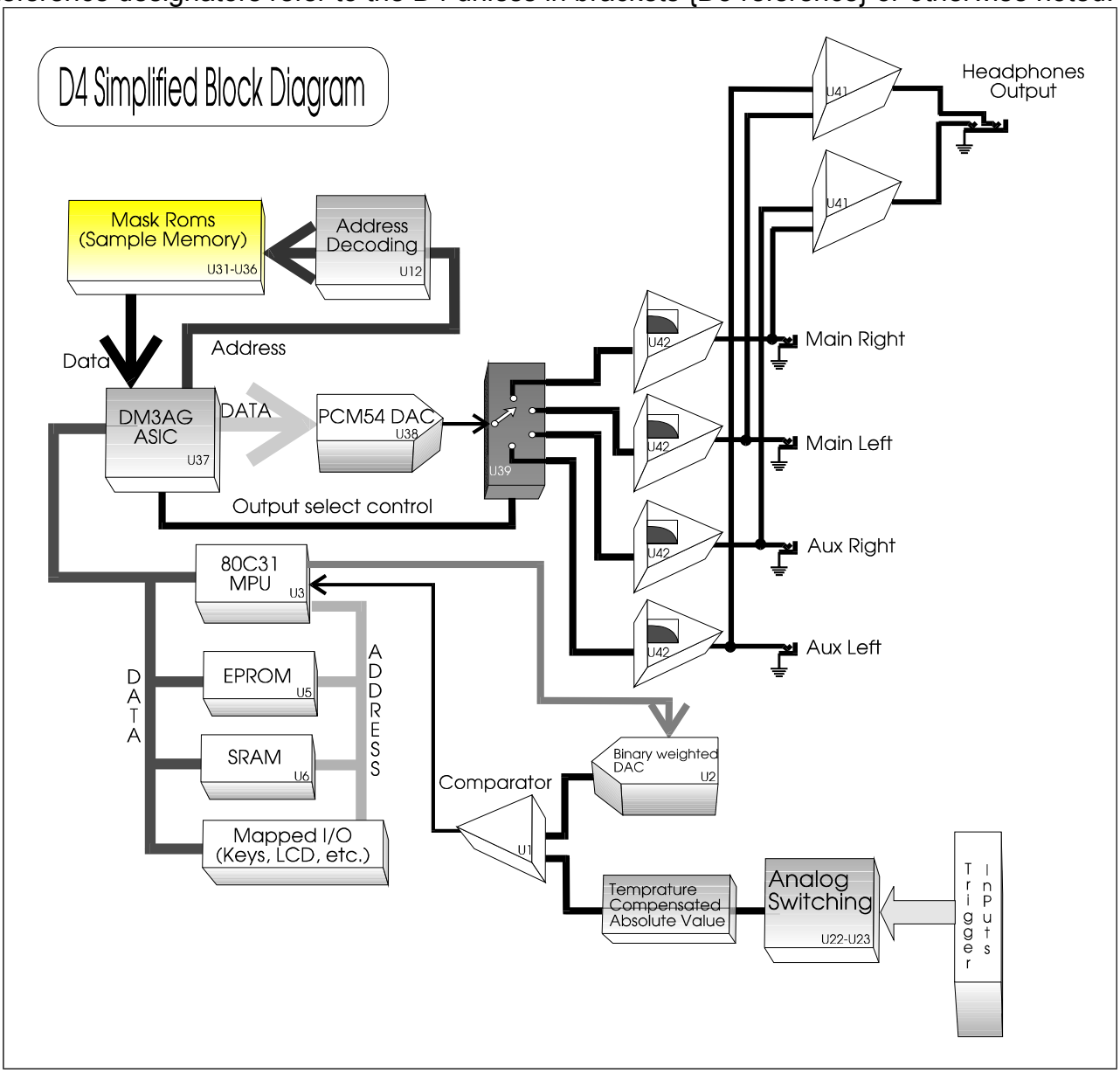


Diagram 1

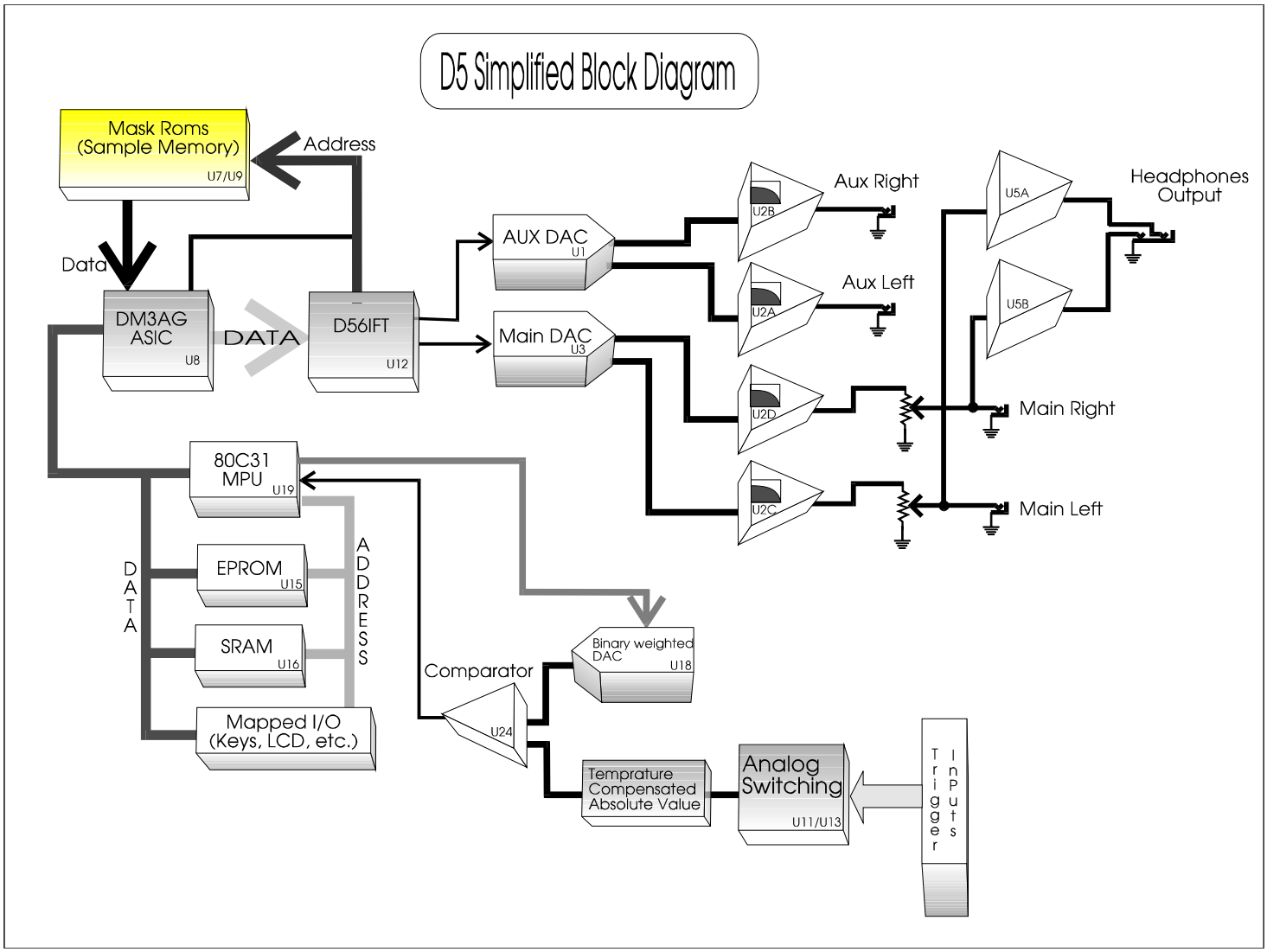


Diagram 2

2.00 Power Supply

The power supply begins with the 9V A.C. 750 mA transformer (Alesis P3 type). After being R.F. filtered by C26, and passing through the power switch, the A.C. is rectified into -12V, and +12V by D1 {D10}, D2 {D11}, and C2/C3 {C111/C112}, C1 {C108}. Regulators supply the +5V and -5V needed to run the unit. Note that the +12V raw supply (From D2) {D11} is used by the system reset circuit (see section 3.11) and battery backup (section 2.10). The D4's +12V and - 12V lines are also used to power the output op-amps via the PUP Circuit (section 2.20). +5V and -5V lines are used to power the PUP circuit in the D5.

2.10 Battery Backup

The battery backup circuit is more complex than it first appears, as it requires a good system reset (see section 3.11) to function properly. The actual backup circuit consists of the 3V battery, a current testing resistor (R38) {R92}, a steering diode (D6) {D2}, a Diode/Transistor/Resistor combination (D7, Q3, R24) {D1, Q6, R85} that acts as a steering diode, and filter capacitor C33 {C27}. The D/T/R combination serves a duel purpose. Besides acting as a steering diode, it also ensures that the supply voltage level of the SRAM is higher than the level of the data buss. This prevents data corruption during normal operation.

As mentioned before, the reset circuit is extremely important to battery backup. While covered more extensively in later sections, it should be noted here that it ties into backup system at the SRAM's chip enable line (pin 20) via Q4, and ensures that all access to the SRAM is shut off during power up, and power down. In the case of the D5, reset is tied in through the D56IFT ASIC and Q5.

Any time any part of the backup circuit (including the SRAM) is changed, battery current should be checked. This is accomplished by measuring the voltage across R38 {R92}. Specification for this is $1mV<V^{R76}<8mV$. Most units are in the range of 1mV to 2mV. Values outside of the normal range usually indicate a problem, and should be troubleshot.

2.20 PUP Circuit

The PUP (quiet Power UP) circuit is designed to prevent the unit from making noise during power up. The circuit utilizes the RESET line (section 3.11) to control the power supply lines to U42 {U2}, which is the final active stage before the outputs. The circuit essentially consists of a switchable regulator. Q12 {Q2} and Q14 {Q4} regulate the + and - analog supplies respectively. Q10, Q11, and Q13 {Q1, Q3} are used to switch the regulating transistors on and off depending on the state of the RESET line.

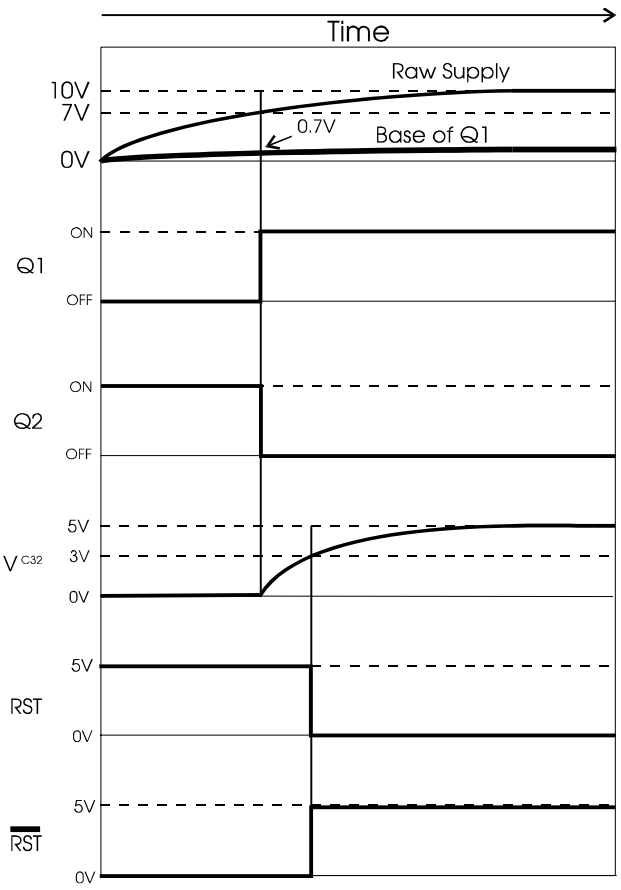
3.00 Digital Signal Paths

3.10 The 8031

The 8031 MPU is the heart of the D4/D5's control section. It handles everything from keypad input and MIDI I/O, to triggers. Note that the 8031 data buss serves a dual purpose. This buss multiplexes between low order addresses (1st 8 bits), and data. Latch U4 {internal to 56IFT ASIC} is used to hold the low order address half, during 8031 read and write cycles. The (U5) {U15} is used to hold 8031 program information. The SRAM (U6) {U16} holds system variables, as well as user parameter data. Z1 {Z1} provides the 12MHz 8031 clock. MIDI I/O is handled through the 8031's built in RXD (Read Serial Data), and TXD (Transmit Serial Data) ports. Piezo input is handled through the regular 8031 I/O ports. Keypad decoding, DM3AG ASIC control, and LCD output are handled through memory mapped I/O (see section 3.12).

3.11 Reset

The reset circuit is perhaps the most singly important circuit in the D4/D5. Failures in the reset circuit can cause symptoms ranging from loss of battery backup to a complete machine lock up. The circuit utilizes the positive raw supply voltage to determine when the supply voltage is high enough for the regulators to function properly. Diagram **Error! Bookmark not defined.** shows the sequence of events during power up. When the raw supply voltage reaches approximately 7.2V, Q1 {Q11} switches on, pulling the base of Q2 {Q7} low and shutting it off. This allows C32 {C106} to charge via R23 {R126}. Once C32 {C106} reaches roughly 3V, U7 {U27A} (pins 10 and 11) switches states,



D4 Reset Sequence of Events

Diagram 3

completing the reset process. The reverse process occurs anytime the raw supply falls below 7.2V. This ensures that all functions that might cause data corruption are not functioning when the power supply is unstable.

3.12 Memory mapped I/O

In order to easily control the vast number of hardware functions that the 8031 needs to access, a system of memory mapped I/O is used. The basic idea is to make hardware functions appear to the 8031 as unused memory locations. That way all that the software has to do is write to a memory location in order to send that information to a specific device such as the LCD, or ASIC. In the case of the D5 many of the map decoding functions are incorporated into the D56IFT ASIC, reducing the parts count relative to the D4.

74HC138 (U12) {D56IFT} performs the majority of the work in this circuit. Two things are required before U12 becomes active. 1> A15 must be low (i.e. the 8031 is accessing the lower 32K of address space). 2> The 8031 WRite line must be active (the 8031 is performing a memory write). A15 is used to directly control which function (memory or I/O) is active.

Once U12 is enabled, addresses A12-A14 are decoded by it, and the latch corresponding to the value of the decoded address is strobed. At this point, data on the 8031 data buss is "written" into the latch.

3.13 Data Entry Knob And Footswitches

The data entry knob and footswitches are read via the memory mapped latch U11 {U22}. This allows the 8031 to directly read any changes in the status of these inputs.

3.14 Keypad Decoding

The keypad is handled through a simple polling matrix implemented through the memory mapped latches U10 and U11 {U20, U22}. Each row is tested by the 8031, one at a time, via U10 {U20}. Any closed switches are read into U11 {U22}, and passed along to the 8031 for interpretation.

3.15 MIDI

The MIDI hardware is a standard implementation. MIDI out/thru begins at the 8031's TXD port (pin 11) and is buffered with two inverters of U7 {U27}.

MIDI in consists mostly of the opto isolator (U8) {U23}, protection diode D4 {D6}, pullup R18 {R128}, and threshold resistor R19 {R129}.

3.20 DM3AG ASIC

The DM3AG ASIC is a complex LSI device, specifically designed for the purpose of playing percussion samples. Obviously, the internal workings of such a device are beyond the scope of this manual, however, a brief description of the important pins follows.

NAME	PIN#(s)	Function
MD0-MD7	27-34	8031 Data Buss Input.
CLOCK	37	Asic Clock Input (8MHz in SR-16).
DAC0-DAC16	42-51, 53-60	Output to DAC.
A0-A19	3-17, 19-23	Mask Address Buss
D0-D7	61-68	Mask Rom Data Buss
SNH0	39	Output Sample and Hold Control
SNH1	40	" " " " "
SNHIN Inhibit.	41	Output Sample and Hold
STRES	26	Instruction reset strobe.
STB	25	Instruction latch strobe.

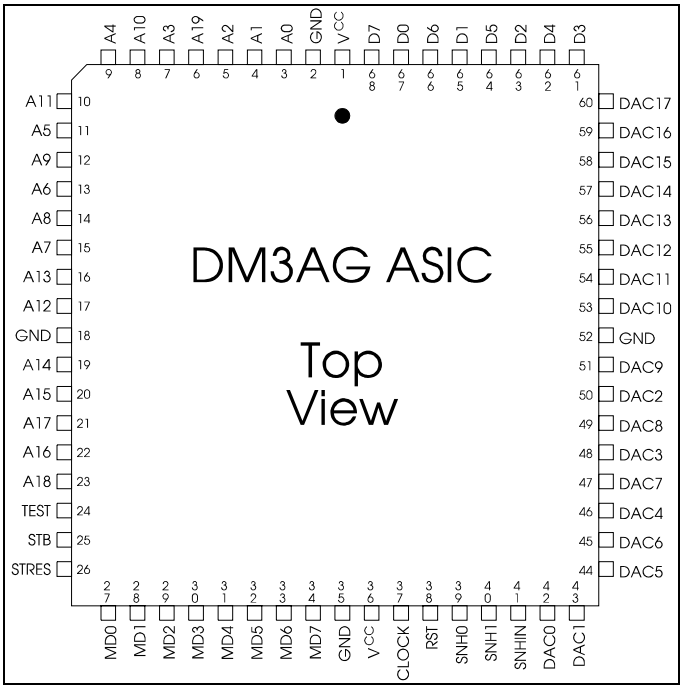


Diagram 2

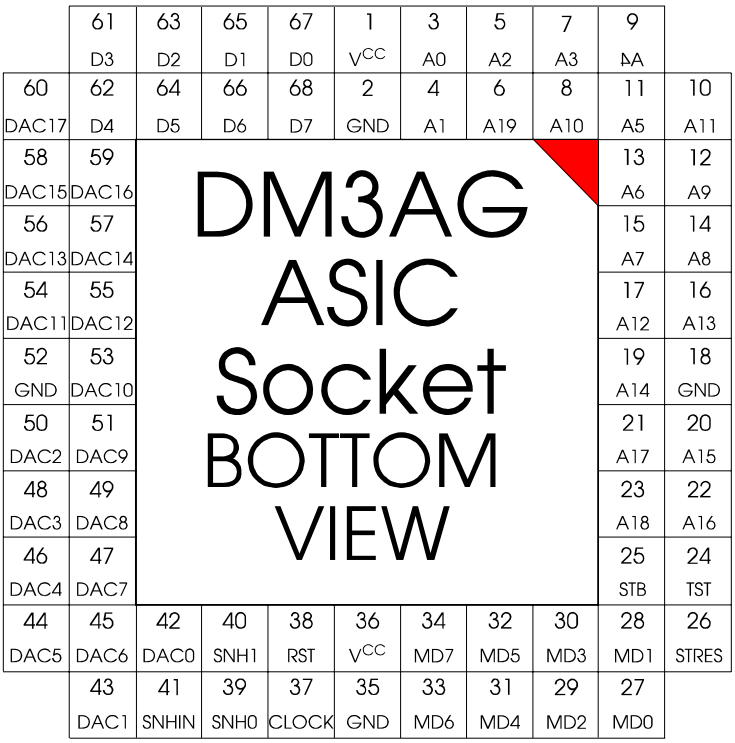


Diagram 5

3.21 Address Buss Decoding

Due to the fact that we are pushing the ASIC beyond it's original design, a little extra hardware was required to accomplish the design goals of the D4. Two limitations needed to overcome. 1> The address space directly accessible wasn't enough for all of the samples. 2> The ASIC clock speed was increased from earlier designs to 12MHz, making extra communication from the 8031 more difficult. This solution to these problems takes the form of an asynchronous decoder. The purpose of the decoder is to act as an extra set of address lines to ensure that only one Mask ROM is enabled at any given time.

Two bits are required for each sample read (6 Mask ROMs, 0-5). This, plus the fact that there are sixteen voices available means that 32 bits total are required for each "sample output cycle". Latches U14-U17 provide the storage area needed to hold all 32 "extra" address bits (which are provided by the software via memory mapped I/O [see section 3.12]). Binary counters U19-U20 are used to synchronize the decoding process. U13 is used to decode which latch the current voice's bit pair will come from, while U18 is used to mask the bit pair itself from the other outputs of the current latch. U30 does the actual decoding of the bit pair, providing the single Chip Enable needed to access the desired sample. Note that 1/2 of U43 is used as a one shot multivibrator to extend the time that the CLear line of the binary counters (U19-U20) is held low slightly longer than SNH0 is low. This is to ensure that the 8031 has time to communicate necessary parameters to the ASIC before the decoder starts it's processing.

Since the D5 uses much larger Mask ROMs, this type of decoding scheme is not necessary. The D56IFT ASIC contains all the extra hardware needed to handle extra address lines not dealt with in the DM3AG ASIC.

3.30 Mask ROMS

The Mask ROMs contain the all of the sample information. The 18 bit address buss allows for 2 megabytes per Mask ROM. Since Mask ROMs rarely fail, most problems in this area will consist of opens or shorts along the data and address busses. Mask Roms in the D5 have a 20 bit address buss (thus only 2 are needed).

4.00 Analog Signal Paths

4.10 D4 Audio Output

Output from the DAC is routed to the four individual output (Main and Aux, Left and Right) by an analog switch (U39). Output selection is controlled directly by the DM3AG ASIC. Each output section consists of an output sample capacitor (C96-C99), and a buffer/anti aliasing filter amplifier (U42, associated resistors and capacitors).

4.11 D4 Headphone Output

The left and right headphone outputs are a sum of the main and aux outputs sent though a pair of X10 inverting amplifiers. The output impedance is fixed by the sum of the op-amps output impedance, and R141/R142 in parallel with C34/C35, at roughly 150Ω. This makes the headphone outs more compatible with 600Ω pro headphones than the 8Ω consumer variety.

4.20 D5 Audio Output

The outputs of the '4319 DACs are buffered and low pass filtered by U2 (and surrounding resistors and capacitors) before being routed to the outputs via A.C. coupling capacitors {C11, C3, C35, C31}. Note that only the main outs run through the volume potentiometer just before being sent to the outputs. Output impedances are fixed at roughly 300Ω. C1, C2, C29, and C30 provide R.F. filtering at the outputs.

4.21 D5 Headphone Output

Headphone outputs are taken from the main out lines after the volume potentiometer. These signal are passed through a gain stage (approximately X10) consisting of U5 and it's associated circuitry. The signal is R.F. filtered {C42, C43} before passing on to the output jack. Note that supply lines to U5 are taken from the raw +/-12V. This is to provide the maximum possible amount of headroom to this output. A lower output impedance than the D4 provides for a little extra current when using 8Ω "consumer" headphones.

4.30 Trigger Inputs

The trigger input circuitry is much simpler than it might first appear. Note that due to the fact that the trigger inputs are the same, only "typical" designations appear on the D4 schematic. A chart of actual part designations appears below the trigger input circuit on the schematic. The input from JT1 is noise filtered by CT0 and CT1. The two sections of an LM339 act as a differential buffer amplifier, providing isolation for the input signal. CT2 provides further filtering and smoothing. The signal is then sent to the analog switches U22 {U11} (trigger ins 1-6) and U23 {U13} (trigger ins 7-12) where it is multiplexed with the other trigger inputs before analog to digital conversion. Trigger input selection is handled by the 8031 via memory mapped I/O (see section 3.12) latch U10 {U20} (*TRG A0-TRG A4*). The D5s trigger input circuitry is virtually identical to that of the D4. Note that on the D5 schematics all triggers are shown separately.

4.30 Analog-Digital Conversion

Successive approximation is an empirical approach to the process of analog to digital conversion. The idea is to divide the process into short, manageable sections. Each significant binary weight (starting with the Most Significant Bit) is taken in turn, thus requiring only 8 comparisons to achieve a final value. U2 {U18} is used to buffer the 8031 output ports. These signal are summed through the binary weighted resistor network consisting of R1-R5 and the resistor SIP R7 {R104-R114, R137}. This signal is compared to the filtered and shaped trigger input signal. The result of this comparison is sent back to the 8031. Once the 8031 has obtained a value for all 8 bits, it stores the final result in memory for further processing, and continues with the next trigger input. Note that when the 8031 examines the states of the trigger inputs, it doesn't use a specific amplitude to trigger on, rather it looks for a large change in amplitude over a short period of time. This helps to prevent false triggering from the other drums in the kit.

5.00 Test Procedures

The D4 contains a number of built in "hidden" routines to assist with troubleshooting and repair of the D4. These routines include:

- Self Test-Initiates internal diagnostics routines. (Power up while holding the "MIDI" and "DRUMSET" buttons simultaneously. Use the "MIDI" button to advance to the next test.)

- Reinitialization-Clears memory and resets software parameters to initial values. (Power up while holding "OUTPUT" and "VOICE" simultaneously.)

- Check Version-Shows current software version. (Select "DRUM SET" Mode. Press "CURSOR RIGHT" and "CURSOR LEFT" simultaneously.)

5.10 D4 Self Test

The self test consists of several separate routines to check different parts of the D4s circuitry. To initiate the self test hold "MIDI" and "DRUMSET" while powering up the unit.

The tests include (in order):

√ RAM: Tests each location in memory for accuracy. The is not memory destructive.
√ ROM: Generates a checksum of all ROM locations and compares it to the correct value stored in the ROM. The chances of this test failing to identify a true ROM failure are extremely low.
√ LEDs: Sequentially lights all LEDs beginning with the upper left corner.
√ MIDI: Tests MIDI I/O functions. (A MIDI cable MUST be connected between the D4's MIDI IN and OUT for the test to operate correctly.)
√ Level Check Test: Tests Main and aux output levels.
√ Triggers: Test individual triggers (See D5 self test procedures for details)
√ Buttons: Tests front panel buttons.
√ DAC Adjustment: While listening to the main outs, adjust the DAC trimpot for minimum distortion.

5.20 D5 Self Test

The D5 has two self test modes which allow the running of diagnostic tests on the digital circuitry. In Individual Test mode, one can select particular tests to run. In All Test mode, the D5 runs all of the tests in series.

To enter Individual Test mode:
- Power up the unit while holding down the DRUMSET and GROUP buttons. Use the Value Dial to select which test to run (each test is described below). Press STORE to execute the test. When the test is complete, you can either select another test to run or exit Individual Test mode by simultaneously pressing MIX and OUTPUT.

To enter All Test mode:
- Power up the unit while holding down the DRUMSET and MIDI buttons.

Individual Test Descriptions:

1. **ROM Test.** If the unit passes, the D5 will display "Passed ROM Test" and exit the test automatically. If the unit fails, the D5 will display "Failed ROM Test!" and won't exit the test. In this case, the user must press OUTPUT to exit.
2. **RAM Test.** If the unit passes, the D5 will display "Passed RAM test" and exit the test automatically. If the unit fails, the D5 will display "Failed RAM test!" and won't exit the test. In this case, the user must press OUTPUT to exit.
3. **LED Test (Individual).** Lights up each LED individually. The D5 automatically exits this test after all LEDs have been lighted.
4. **LCD TEST.** Lights up all the LCD pixels. Press OUTPUT to exit the test.
5. **Switch and Encoder Test.** Checks all of the buttons and the rotary encoder. The user must press every button and rotate the encoder in both directions in order for the test to pass. After pressing all the buttons, the user should simultaneously press the left and right Cursor buttons. If at this point all of the buttons have been pressed (i.e., the unit passed), then the D5 will simply exit. If instead not all of the buttons have been pressed, the D5 will display "Fail Switch Test". The user can either restart the test (by pressing STORE) or exit the test (by pressing OUTPUT).
6. **MIDI In/Out Test.** Before running this test the user must connect a MIDI cable from the MIDI Out to the MIDI In. If the unit passes, the D5 will display "Passed MIDI I/O" and exit the test. If the unit

fails, the D5 will display "Failed MIDI I/O!" and won't exit the test. In this case, the user must press OUTPUT to exit.

7. **Output Test.** This tests the four output channels by playing a trio of drum sounds through them. Pressing the STORE button starts the test. It starts with the Main Left channel. Pressing the OUTPUT button cycles through the Main and Aux channels, and then exits the test.
8. **Trigger Test.** This tests the twelve trigger inputs by playing a sound through the MAIN LEFT output, and triggering a trigger input. A cable must be connected from the MAIN LEFT output to one of the 12 Trigger Inputs, in order from 1 to 12 Pressing the STORE button starts the test. Once the test has been started, connect a cable from the MAIN LEFT output to the Trigger 1 input ONLY! Do NOT connect the output to all 12 triggers simultaneously! When the test has started, the LCD will display the message, "Testing Trig 1". At this point, plug the cable from the MAIN LEFT output into Trigger Input 1. Soon after, the display should change to "Testing Trig 2". If the display does not change, or displays the message "Fail Trig 1", then the test has failed for this trigger input. Pressing the OUTPUT will skip to the next trigger if an error occurs. Once the display shows "Testing Trig 2", unplug the cable from the Trigger 1 input, and plug it into the Trigger 2 input. The display should then show "Testing Trig 3". Repeat the process until all 12 triggers have been tested.

5.30 Further Testing

Because of the extensive self test capabilities of the D4/D5 very little extra testing is necessary. It is always a wise policy to listen to the unit (both through the headphones and via the main and aux outs) for any signs of distortion. Trigger inputs can be tested using a piezo element (such as the type commonly used for establishing front panel velocity) wired to a 1/4" jack. MIDI can be further tested using a sequencer or SYS-EX storage device (SYS-EX is probably more accurate as it allows data travel to be sent as well as received). As always, it is a good idea to shake the fully reassembled unit to ensure that no loose components are inside.

6.00 Updates and Corrections

6.10 D4 Updates

Revision C and higher boards require no updates as of this manual release. The remainder of this section applies to all Revision A and B PCBs unless otherwise noted.

Revision A PCBs will contain many odd jumpers. These were installed at the factory and should not be of too much concern to the technician.

Revision A & early revision B PCBs have gray ribbon cables between the main and front panel PCBs. These were found to be unreliable and should be replaced with standard SIL cables (ALPARTNO 4-19-7511). These same PCBs will also have black headers where the gray cable attaches. These headers should also be replaced for the same reason.

Add 20pF between left side of D3 and right side of R12. Note that this may already exist on the bottom of the board. This update filters out audio noise that occurs when the data wheel is in certain positions.

R153 should be changed from 200k to 100k and the trimpot from 250k to 50k on revision A PCBs only (later revisions have already incorporated this change). This changes the range of the DAC adjust circuitry. On some early units the DAC may not be adjusted correctly due to the fact that the range is not large enough

R9 should be changed to 100Ω from 470Ω. This speeds up the response of the output sample and hold circuitry resulting in a timbrely brighter output.

7.00 Common Solutions

The following table presents solutions to the most common problems that we have seen. Please be aware that this does mean that every possible scenario is covered here. There is always the possibility that other "odd" failures may lead to the same symptom. This table should help about 90% of the time.

NOTE: Due to the fact that the D5 has not been in the field long enough to establish a separate service history, a separate troubleshooting table will have to wait for future revisions of this manual. While the following applies specifically to the D4, it is likely that similar symptoms will lead to similar solutions in the D5.

Described Defect	Probable Cause	Solution
Unit Dead.	Faulty power switch.	Replace and retest.
	Faulty D1.	Replace and retest.
	Faulty A.C. Adapter.	Replace and retest.
	C26 shorted.	Replace and retest.
	Faulty 7805 regulator.	Replace and retest.
Unit locked up.	Faulty D1 or D2.	Replace and retest.
	Faulty 8031.	Replace and retest.
	Faulty SRAM.	Replace and retest.
	C32 leaking. (reset cap).	Replace and retest.
Only boxes in display.	Faulty D1 or D2.	Replace and retest.
	Faulty LCD.	Replace and retest.
	Faulty LCD Cable.	Replace and retest.
Intermittent reset.	Faulty D1.-This can be determined by checking the voltage at the cathode. If the peak voltage is less than 9V then the diode is defective.	Troubleshoot and repair as necessary.
	C32 (reset cap).	Replace and retest.
No battery backup.	Q3 or Q4 shorted.	Troubleshoot and repair as necessary.
	C33 shorted.	Replace and retest.
	Faulty SRAM.	Replace and retest.
	Dead Battery.	Troubleshoot and repair as necessary.
	Poor solder or missing component on D6.	Troubleshoot and repair as necessary.
Trigger failure.	Crashed-(check MIDI and external trigger setups for missing pages).	Troubleshoot and repair as necessary.
	Faulty or wrong Q6-9.	Troubleshoot and repair as necessary.
	Faulty U21.	Replace and retest.
	Faulty 8031.	Replace and retest.
Audio Distortion.	Poor connection/bad cable at J5.	Troubleshoot and repair as necessary.
	Faulty D2.	Replace and retest.
	Faulty DAC.	Replace and retest.
	Faulty ASIC.	Replace and retest.
	Faulty PUP circuit.	Troubleshoot and repair as necessary.
No MIDI In.	Faulty opto-isolator.	Replace and retest.
	Faulty 8031.	Replace and retest.
No MIDI Out.	Faulty U7.	Replace and retest.
	Faulty 8031.	Replace and retest.
Data wheel not working correctly.	Faulty shaft encoder.	Replace and retest.
	Cable at J3 faulty or loose.	Troubleshoot and repair as necessary.
No button function/LEDs after repair.	J2 or J1 header backwards (up to rev Bs).	Key towards front

8.00 Service Parts Lists

8.10 D4 Service Parts List

GROUP	DESCRIPTION	ALPARTNO	QTYPER	POSITION	PCB	MANUFACT	NOTES
ASS	PCB, D4 MAIN ASSY	8-20-0022	1	MAIN BOARD ASSEMBLY			
ASS	PCB, D4 KEYPAD ASSY	8-20-0023	1	FRONT PANEL (KEYPAD) BOARD ASSEMBLY			
CAB	14 PIN DIL 200mm	4-18-0415	1	J4-LCD			
CAB	3 PIN SIL 175mm	4-19-0103	1	J6-PHONES PCB			
CAB	3 PIN SIL 75mm	4-19-0104	2	J3-ENCODER PCB,J5-VOL PCB			
CAB	10 PIN SIL 75mm	4-19-7511	2	J1-KEYPAD PCB,J2-KEYPAD PCB			
CAP	0.47 MF ELEC 50V	1-07-1474	12	C4-15	MAIN		
CAP	2200 MF ELEC 16V	1-08-2200	3	C1-3	MAIN		
CER	1000 PF CERDISC	1-02-0102	1	C31	MAIN		
CER	0.01 MF CERDISC	1-02-0103	14	C17,18,44,46,48,50,52,54,59,60,62,63,65,66	MAIN		
CER	0.1 MF CERDISC	1-02-0104	39	C16,19,20,23-28,30,30,32-42,55-57,68-76,100,101,102,104,105	MAIN		
CER	150 PF CERDISC	1-02-0151	31	C29,43,45,47,49,51,53,58,61,64,67,77,79,80,82,83,85,87,88,90,91,94,95,106-113	MAIN		
CER	20 PF CERDISC	1-02-0200	4	C21,22,78, (REV D) C114	MAIN		
CER	5000 PF CERDISC	1-02-0502	8	C81,84,86,89,96-99	MAIN		
FIL	0.01 MF FILM	1-20-0103	1	C103	MAIN		
HDR	03 PIN SIL (SHROUDED)	4-14-0003	6	J3,J5,J6,ENCODER PCB,PHONE PCB,VOL PCB			
HDR	10 PIN SIL (SHROUDED)	4-14-0010	4	J1,J2,KEYPAD PCB (2)			
HDR	14 PIN DIL	4-14-0014	1				
HDW	6-32x1/4 PPB	5-00-0003	2	HEATSINKS	MAIN		
HDW	M3x7mm PHILSLOT	5-00-0020	9	CASE	MAIN		
HDW	6-32x1/2 STANDOFF	5-02-0003	2	HEATSINKS	MAIN		
HDW	SOLDER LUG	9-03-1036	17		MAIN		
HDW	RETAINER STRIP 11x200mm	9-13-1019	4	FRONT PANEL			
HDW	FOAM STRIP 6.5x180mm	9-23-1014	4	FRONT PANEL			
HDW	FOAM STRIP 6.5x100mm	9-23-1017	4	RACK EAR			
IC	7805 +5 V REG TO220	2-11-7805	1		MAIN	NAT	
IC	7905 -5 V REG TO220	2-11-7905	1		MAIN	NAT	
IC	74HC138 DEMUX	2-14-0138	3	U12,13,30	MAIN	NAT/TI	
IC	74HC153 DUAL 4-I/P MUX	2-14-0153	1	U18	MAIN	TI	
IC	74HC161 BINARY COUNTER	2-14-0161	2	U19,20	MAIN	TI	
IC	74HC541 OCTAL BUFFER	2-14-0541	2	U2,11	MAIN	TI	
IC	74HC573 3-STATE LATCH	2-14-0573	1	U4	MAIN	TI	
IC	74HC574 OCTAL FF	2-14-0574	6	U9,10,14-17	MAIN	TI	
IC	74HC04 HEX INVERTER	2-14-7404	1	U7	MAIN	TI	
IC	74HC74 DUAL D FF	2-14-7474	1	U43	MAIN	TI	
IC	8Kx8 SRAM 58128	2-17-0129	1	U6	MAIN	HYUNDAI	
IC	27C512 EPROM	2-19-0512	1	U5	MAIN	SIG	
IC	80C31 MPU	2-20-8031	1	U3	MAIN	SIG	
IC	TLO84 4 OP AMP	2-21-0084	2	U21,42	MAIN	TI	
IC	NE5532N DUAL OP AMP	2-21-5532	1	U41	MAIN	SIG	
IC	LM311 ANALOG COMP	2-22-0311	1	U1	MAIN	TI	
IC	LM339 QUAD COMP	2-22-0339	6	U24-29	MAIN	TI	
IC	4051 ANALOG SWITCH	2-23-4051	2	U22,23	MAIN	ST/HAR/RCA/SIG/PHIL	
IC	4052 ANALOG SWITCH	2-23-4052	1	U39	MAIN	HAR/PHIL	
IC	6N138 OPTO ISO	2-24-0138	1	U8	MAIN	TI/SIEMANS	
IC	PCM54HP 16-BIT DAC	2-25-0054	1	U38	MAIN	BURR-BROWN	
IC	MASK ROM D1 CHIP 1	2-27-0003	1	U36	MAIN	TOSH	
IC	MASK ROM D1 CHIP 2	2-27-0004	1	U35	MAIN	TOSH	
IC	MASK ROM D2 CHIP 1	2-27-0007	1	U34	MAIN	TOSH	
IC	MASK ROM D2 CHIP 2	2-27-0008	1	U33	MAIN	TOSH	
IC	MASK ROM D4-1	2-27-0013	1	U32	MAIN	TOSH	
IC	MASK ROM D4-2	2-27-0014	1	U31	MAIN	TOSH	
IC	DM3ET0 ASIC	2-27-0015	1	U37	MAIN	AMI	
JAC	5 PIN DIN JACK	4-00-0001	2		MAIN		
JAC	1/4 CLIFF (MONO)	4-02-0001	17		MAIN		
JAC	1/4 CLIFF (STER)	4-03-0001	1		MAIN		
JAC	3.5mm BAR JACK (P3)	4-16-0002	1	J7	MAIN		
GROUP	DESCRIPTION	ALPARTNO	QTYPER	POSITION	PCB	MANUFACT	NOTES

ME	1N4148 SIGNAL DIODE	2-00-4148	11	D3,4,6-14	MAIN		
ME	1N4003 DIODE	2-01-4003	2	D1,2	MAIN		
ME	1N5231B ZENER DIODE	2-02-5231	1	D5	MAIN	MOT ONLY- NO SUBS	
ME	1N5236B ZENER DIODE	2-02-5236	2	D15,16	MAIN	MOT ONLY- NO SUBS	
ME	MPS2369 TRANS	2-03-2369	2	Q4,5	MAIN	MOT	
ME	2N4401 NPN TRANS	2-03-4401	10	Q1-3,6-12	MAIN	NAT	
ME	2N4403 PNP TRANS	2-03-4403	3	Q13-15	MAIN	NAT	
ME	LED (RED) SOT-23	3-02-0004	10		KEY		
ME	DPDT SWITCH (QS)	6-02-0002	1		MAIN		
ME	PIEZO	7-00-0001	1		KEY		
ME	12 MHz CER RES	7-01-0003	1	Z1	MAIN		
ME	LITH BAT (PANA 3V)	7-05-0003	1	B1	MAIN	PANASONIC	
ME	DATA ENCODER	8-00-1008	1				
ME	LCD MODULE	9-44-1111	1				
MTL	RACK EAR 150mm	9-58-1007	2				
MTL	XTRUDED FRONT PANEL	9-03-1058	1				
MTL	CASE BOTTOM 150mm	9-03-1059	1				
MTL	CASE TOP 150mm	9-03-1060	1				
PCB	PCB, MAIN REV D	9-40-1057	1	(INCLUDES VOL PCB,DATA PCB,HDPH PCB)			
PCB	PCB, KEY REV B	9-40-1058	1				
PLS	LCD BEZEL	9-13-1018	1				
PLS	BUTTON TREE UPPER	9-15-0046	1				
PLS	LED LENSE	9-15-0047	10				
PLS	LCD FRAME	9-15-0048	1				
PLS	VOLUME KNOB	9-15-0049	1				
PLS	DATA KNOB	9-15-0050	1				
PLS	SWITCH XTENDER	9-15-0051	1				
PLS	BUTTON FRAME	9-15-0055	1				
PLS	BUTTON TREE LOWER	9-15-0063	1				
PLS	RUBBER KEYPAD	9-23-1025	1				
PLS	DATA KNOB RUB SLEEVE	9-23-1026	1				
POT	50K TRIMPOT	0-08-0502	1	R154	MAIN		
POT	5KA SINGLE	0-09-1015	1	R155	MAIN		
RES	100 1/8W 5%	0-00-0101	4	R9,141,142,148	MAIN		
RES	1K 1/8W 5%	0-00-0102	16	R8,18,21,24-26,38,50,103,111,109,113,114,116,124,145	MAIN		
RES	10K 1/8W 5%	0-00-0103	17	R10,19,22,52,53,115,117-120,121-123,125,130,133,140	MAIN		
RES	10K 1/8W 5%	0-00-0103	36	R57-59,61-63,65-67,69-71,73-75,77-79,80,81,83,84-86,88,89,91-94,96,97-100,131	MAIN		(RT 2-4)
RES	100K 1/8W 5%	0-00-0104	5	R4,46,47,147,153	MAIN		
RES	1M 1/8W 5%	0-00-0105	5	R23,110,112,128,129	MAIN		
RES	120K 1/8W 5%	0-00-0124	1	R51	MAIN		
RES	1.3K 1/8W 5%	0-00-0132	8	R30-37	MAIN		
RES	150 1/8W 5%	0-00-0151	4	R39-42	MAIN		
RES	2K 1/8W 5%	0-00-0202	2	R20,54	MAIN		
RES	20K 1/8W 5%	0-00-0203	12	R56,60,64,68,72,76,82,87,90,95,101,102	MAIN		
RES	200K 1/8W 5%	0-00-0204	3	R3,146,152	MAIN		
RES	220 1/8W 5%	0-00-0221	9	R14-17,43-45,106,107	MAIN		
RES	2.7K 1/8W 5%	0-00-0272	1	R6	MAIN		
RES	300K 1/8W 5%	0-00-0304	1	R150	MAIN		
RES	390K 1/8W 5%	0-00-0394	1	R2	MAIN		
RES	3.9M 1/8W 5%	0-00-0395	1	R151	MAIN		
RES	470 1/8W 5%	0-00-0471	5	R11,12,27-29	MAIN		
RES	5.1K 1/8W 5%	0-00-0512	8	R13,48,49,55,104,108,132,143	MAIN		
RES	51K 1/8W 5%	0-00-0513	3	R5,126,127	MAIN		
RES	8.2K 1/8W 5%	0-00-0822	1	R105	MAIN		
RES	820K 1/8W 5%	0-00-0824	1	R1	MAIN		
RES	910 1/8W 5%	0-00-0911	1	R149	MAIN		
RES	22K 9 PIN SIP	0-06-2239	2	R7,139	MAIN		
SOC	28 PIN DIP 0.6	4-06-0028	3	U5,6,38	MAIN		
SOC	40 PIN DIP 0.6	4-06-0040	1	U3	MAIN		
SOC	68 PIN ASIC SOC	4-12-0068	1	U37	MAIN		

8.20 D5 Service Parts List

Grp	ALPartNo	Description	Qnt y	PCB	Ref. Designator	Manufact.	Comments
ASY	9-79-0157	ASSY PCB MAIN D5	1				
ASY	9-79-0158	ASSY PCB FRONT PANEL D5	1				

ASY	9-79-0159	ASSY LCD D5	1				
CAB	4-18-1627	CABLE DIL 16-PIN 210MM .1 CTR M-F M4	1				
CAB	4-18-2020	CABLE 20-PIN DIL 200mm RIBBON	1				
CAB	4-19-1331	CABLE SIL 8-PIN 225MM 2MM (REV B)	1				
CAP	1-08-0101	CAP 10 uF ELEC 16V	10		C3,4,7,11,24,27,31,35,109,110		
CAP	1-08-0105	CAP 1.0 uF ELEC 16V	12		C40,47,48,56,61,62,70,73,80,87,88,95		
CAP	1-08-0228	CAP 2200 uF ELEC 16V	3		C108, 111, 112		
DIO	2-01-4003	DIODE POWER 1N4003	2		D10, 11		
DIO	2-02-5231	DIODE ZENER 1N5231B	1		D12		
HDR	4-14-0116	HEADER 16-PIN DIL 0.1 SHROUDED	1		J11		
HDR	4-14-1120	HEADER 20-PIN DIL SHROUDED O.1	1		J22		
HDR	4-15-1008	HEADER 8-PIN SIL 2MM CTR (SHROUDED)	1				
HDR	4-14-0020	HEADER 20-PIN DIL 0.1 XR/CL	1				
HDR	4-15-1008	HEADER 8-PIN SIL 2MM CTR (SHROUDED)	1				
HDW	5-00-0020	SCREW M-3 x 7mm PHIL SLOT	11				
HDW	5-02-0009	HEATSINK M3x20 D4	2		ATTACH TO U28, 29		
HDW	5-04-0009	WASHER M3 SPLITLOCK	2				
IC	2-24-0138	IC 6N138 OPTO ISO HEWLETT	1		U23		
IC	2-27-0039	IC ASIC D56IFT D5/D6 (64PQFPRECT)	1		U12		
IC	2-31-0064	IC SOFTWARE EPROM D5	1	MAIN	U15	MARSHAL	
IC	2-11-7805	REG 7805 +5V TO220 NATIONA	1		U29		
IC	2-11-7905	REG 7905 -5V TO220 NATIONA	1		U28		
JAC	4-02-0001	JACK 1/4 MONO CLIFF	17		J1-5, 7-10, 12-18, 21		
JAC	4-00-0001	JACK 5-PIN DIN (MIDI)	2		J19, 20		
JAC	4-16-0002	JACK 3.5MM BARREL (P3)	1		J23		
JAC	4-02-0005	JACK CLIFF STEREO (J/SKT S2/BBB BLK PC -A/S 12.5mm)	1				
LED	3-02-0012	LED GRN T1 HP HLMP1540	10				
LED	3-02-0016	LED BACKLIGHT (GRN) Q2	6				
LIT	7-51-1169	CHART SOUND D5	1				
LIT	7-51-1170	CHART QUICK SET-UP D5	1				
LIT	7-51-1175	MANUAL REFERENCE D5	1				
ME	7-05-0003	BATTERY 3V LITHIUM PANASONIC	1		B1		
ME	7-01-0009	CRYSTAL 12 MHz	1		Z1		
ME	7-00-0001	PIEZO KYOCERA	1				
MIS	9-23-1017	STRIP FOAM (SIDE) 7x95mm D4	4				
MIS	9-00-1011	ENCODER DATA (ALPS EC11B 15mm w/o SWITCH)	1				
MIS	9-23-1014	STRIP FOAM (F/P) 7 x 185mm	4				
MTL	9-03-1059	CASE BOTTOM 150MM D4	1				
MTL	9-03-1060	CASE TOP 150MM D4	1				
MTL	9-58-1007	PANEL SIDE/RACK EAR 150mm	2				
MTL	9-03-1036	LUG SOLDER PCB MNT	17				
MTL	9-03-0005	EXTRUSION F/P D5	1				
MTL	9-03-1165	CLIP STRIP RETAINER	8				
PCB	9-40-1174	PCB D5 MAIN	1				
PCB	9-40-1215	PCB FRONT PANEL D5	1				
PCB	9-40-1219	PCB HEADPHONE D5	1				
PLS	9-15-1078	BUTTON POWER Q2/S4/M4	1				
PLS	9-15-1117	EXTENDER SWITCH Q2	1				
PLS	9-10-0003	BEZEL FRONT PANEL A D5	1				
PLS	9-10-0004	BEZEL FRONT PANEL B D5	1				
PLS	9-10-0006	BEZEL FRONT LCD D5	1				
PLS	9-13-0020	STRIP RETAINER 20mm D5	2				
PLS	9-13-0130	STRIP RETAINER 130mm D5	2				
PLS	9-15-0087	KNOB DATA M4	1				
PLS	9-15-1112	KNOB STANDARD Q2	1				
POT	0-09-1022	POT 10KA DUAL CONTROL X2	1				
RES	0-05-0020	RES 2 OHM 1/2W 10%	1		R73		
RUB	9-23-1061	KEYPAD RUBBER D5	1				

Grp	**ALPartNo**	**Description**	**Qnt y**	**PCB**	**Ref. Designator**	**Manufact.**	**Comments**
SMC	1-50-0103	CAP 0.01 uF NPO 1206	12		C41,50,51,58,63,66,71,76,81,89,91,97		
SMC	1-50-0104	CAP 0.1 uF NPO 1206	41		C5,6,8,16,17,25,26,28,37,39,42-44,49,52,53,55,57,60,64,67,68,72,75,77,79,84,90,92,93,96,98-107		
SMC	1-50-0152	CAP 1500 PF NPO 1206 50V	8		C12, 13, 15, 18, 22, 23, 33, 34		
SMC	1-50-0220	CAP 22 PF NPO 1206	2		C82, 83		
SMC	1-50-1500	CAP 150 PF NPO 1206	12		C38, 45, 46, 54, 59, 65, 69, 74, 78, 85, 86, 94		
SMC	1-51-0015	CAP 0.001uF 1206	2		C29, 30		

SMC	1-51-0156	CAP 0.015uF 1206	2		C1, 2		
SMI	2-27-0015	ASIC DM3 ETO (SMD)	1		U8		
SMI	2-67-5168	IC 8K x 8 SRAM (LH5168N-10L)	1		U16		
SMI	2-70-8032	IC 80C31 PQFP SMD	1		U19		
SMI	2-71-0084	IC TL084 QUAD OPAMP SMD	2		U2, 25		
SMI	2-71-5532	IC NE5532 DUAL OPAMP SMD	1	MAIN	U5		
SMI	2-76-4319	IC AKM4319 DAC	2		U1, 3		
SMI	2-77-0030	IC MASK ROM D5-1	1		U9		
SMI	2-77-0043	IC MASK ROM D5-2	1		U7		
SMI	2-64-0541	IC 74HC541 OCTAL BUFFER SM	2		U18, 22		
SMI	2-64-0574	IC 74HC574 OCTAL D FF SMD	2		U20, 26		
SMI	2-64-7414	IC 74HC14 HEX INVERTER	1		U27		
SMI	2-72-0311	IC LM311 ANALOG COMP SMD	1		U24		
SMI	2-72-0339	IC LM339 ANALOG COMP SMD	6		U4,6,10,14,1721		
SMI	2-72-4051	IC CD4051 ANALOG MUX SMD	2		U11, 13		
SMM	2-50-4148	DIODE SIGNAL 1N4148 SMD	9		D1-9		
SMM	2-51-4401	TRANS 2N4401 NPN SMD	10		Q1, 4-12		
SMM	2-51-4403	TRANS 2N4403 PNP SMD	2		Q2, 3		
SMR	0-10-0102	RES 1K OHM 1/8W 5% 1206	8		R6, 25-27, 84, 131, 135, 141		
SMR	0-10-0103	RES 10K OHM 1/8W 5% 1206	49		R5,19-23,39,40,44-46,52-57,62-64,66-69,71,72,75-77,79,81-83,87-90,92,95-99,101-103,129,133,146		
SMR	0-10-0104	RES 100K OHM 1/8W 5% 1206	3		R113, 130, 145		
SMR	0-10-0105	RES 1M OHM 1/8W 5% 1206	2		R91, 126		
SMR	0-10-0124	RES 120K 1/8W 1206	1		R132		
SMR	0-10-0202	RES 2K OHM 1/8W 5% 1206	4		R24, 28-30		
SMR	0-10-0203	RES 20K OHM 1/8W 5% 1206	20		R7,12,14,16,17,31,34,38,43,50,51,61,65,70,74,80,86,93,94,100		
SMR	0-10-0204	RES 200K OHM 1/8W 5% 1206	1		R112		
SMR	0-10-0221	RES 220 OHM 1/8W 5% 1206	14		R3,4,32,33,122-125,127,139,140,143,147,148		
SMR	0-10-0222	RES 2.2K OHM 1/8W 5% 1206	2		R138, 142		
SMR	0-10-0223	RES 22K OHM 1/8W 5% 1206	14		R104-109, 115-121, 137		
SMR	0-10-0272	RES 2.7K OHM 1/8W 5% 1206	1		R134		
SMR	0-10-0393	RES 39K OHM 1/8W 5% 1206	8		R8-11, 13, 15, 18, 35		
SMR	0-10-0394	RES 390K OHM 1/8W 5% 1206	1		R111		
SMR	0-10-0470	RES 47 OHM 1/8W 5% 1206	2		R48, 49		
SMR	0-10-0471	RES 470 OHM 1/8W 5% 1206	6		R47, 58-60, 78, 128		
SMR	0-10-0472	RES 4.7K OHM 1/8W 5% 1206	6		R1, 2, 36, 42, 85, 144		
SMR	0-10-0512	RES 5.1K OHM 1/8W 5% 1206	1		R136		
SMR	0-10-0513	RES 51K OHM 1/8W 5% 1206	3		R37, 41, 114		
SMR	0-10-0824	RES 820K 1/8W 1206	1		R110		
SOC	4-06-0028	SOCKET 28-PIN DIP 0.6	1				
SWT	6-02-0002	SWITCH DPDT	1		SW1		

9.00 D4 Software History

9.10 Version 1.01

9/15/91

First production release. Changed the offensive drumset names found in version 1.00.

9.20 Version 1.02

12/13/91

1 A triggering bug existed when using two or more drum pads that would cause a pad hit to be ignored when a neighboring pad had been struck hard immediately before it. This would usually occur on the second hit of a two pad flam, or on the first hit to a tom pad during a drum-roll on the snare.

2 The trigger TYPE parameter has been replaced with three new parameters. These are the cross-talk suppression parameter XTALK, the post-trigger decay/recovery time parameter DCAY, and the noise floor threshold parameter NOISE. To accommodate these new parameters, a new page has been added under the EXT TRIG functions.

3 The trigger inputs now have an adjustable VCURVE parameter on the first page under EXT TRIG. (Where TYPE was.) This parameter selects one of seven pad-force to midi velocity response curves to suit different playing techniques.

4 The diagnostics routine's ram test is now non-destructive.

5 The signal threshold for the diagnostics trigger self-test has been lowered to keep units from failing unnecessarily in repair.

6 The note number assignment of trigger 9 has been changed on most preset drumsets from 039 D#1 (handclap) to 057 A2 (crash cymbal 2).

7 The dynamic voice allocation scheme has been improved so that voice-stealing is less noticeable.

8 Any system exclusive messages received that included nested midi real-time messages (i.e. timing clocks, active sensing, start, stop, or continue) would cause the system exclusive data to be ignored and the SYSEX DATA ERROR message would be displayed. This has been fixed so that any nested real-time message are ignored, and the sysex data reception continues uninterrupted.

9 A new system exclusive message has been added (opcode 05H) to transmit and receive the new trigger parameters. The new sysex messages will allow version 1.01 software to upload trigger gains to version 1.02, but the trigger types will be ignored. Version 1.02 trigger parameters sent to a version 1.01 machine will be ignored completely.

10 The reception of a "System Info Request" system exclusive message (opcode 40H) would result in the transmission of the complete 25 packet system exclusive dump of the entire D4's memory. This has been changed so that only the System Info message packet is sent.

11 The system exclusive message that allows an external device to display characters on the LCD (opcode 04H) had a bug that would cause the SYSEX DATA ERROR message to be displayed instead. This now works properly.

9.30 Version 1.03

1/2/92

1 A bug existed in the v1.02 voice allocation routine that would cause short sounds or individual samples within sounds to drop out or sputter until the machine was powered off. This is now fixed.

2 A bug existed (in v1.02 only) that could prevent the user from selecting a new trigger note number for triggers 3, 7, and 11. This is now fixed.

9.40 Version 1.04

3/19/92

1 A bug existed (in v1.03 only) that could crash the machine if a flurry of notes were sent to the D4 and if some of the voices assigned to those notes were set to SINGLE, GROUP1, or GROUP2 mode. This is now fixed.

2 The system exclusive receive routine has been modified so that the time out period used to detect unplugged midi cables and unfinished system exclusive messages is now 250mS instead of 80mS as in earlier versions. This was done to allow slow computers more time while transmitting to the D4 before the D4 panics and aborts the sysex load. In addition, the LCD will now correctly display the "MIDI BUFFER OVERFLOW" message when the buffer overflows during sysex reception instead of the "SYSEX DATA ERROR" message.

3 The signal threshold for the diagnostics trigger self-test has been lowered even further to keep units from failing unnecessarily in repair.

10.00 D5 Software History

10.10 Version 1.01

9/22/95

First production release.

11.00 MIDI Implementation

April 3, 1992
D4 Software Version 1.04
Including
September 22, 1995
D5 V1.01
D5 differences are noted in italics.

TRANSMITTED DATA
Channel Messages

Status	Second	Third	Description
1001 nnnn	0kkk kkkk	0vvv vvvv	Note On kkk kkkk = 0-127 (61 Key Window + Root Note) vvv vvvv = 1-127 vvv vvvv = 0 = Note Off

Universal System Exclusive Messages
(Transmitted on power up and when Inquiry Request is received)

Byte	Description
1111 0000	Exclusive Status
0111 1110	Non-Real Time Message ID
0uuu uuuu	Universal Sysex Channel (Same as D4 Midi Channel)
0000 0110	General Information Sub-ID
0000 0010	Inquiry Message Identity Reply
0000 0000	Manufacturers System Exclusive ID Code
0000 0000	Alesis = 00H,00H,0EH
0000 1110	
0000 0110	Device Family Code LSB (D4 = 6 *D5 = 13H*)
0000 0000	Device Family Code MSB
0000 0000	Device Family Member LSB (D4 = 0)
0000 0000	Device Family Member MSB
0qqq qqqq	Software Version LSB
0qqq qqqq	Software Version MSB
0rrr rrrr	Software Revision LSB
0rrr rrrr	Software Revision MSB
1111 0111	EOX

D4/D5 System Exclusive Messages

Byte	Description
1111 0000	Exclusive Status
0000 0000	Manufacturers System Exclusive ID Code
0000 0000	Alesis = 00H,00H,0EH
0000 1110	
0000 0110	Device ID (D4 = 6)
0000 nnnn	Midi Channel
00oo oooo	Opcode (see Sysex section for opcode definitions and data structures)
0ddd dddd	Data
---- ----	---
1111 0111	EOX

RECOGNIZED RECEIVE DATA
Channel Messages

Status	Second	Third	Description
1001 nnnn	0kkk kkkk	0vvv vvvv	Note On kkk kkkk = 0-127 (61 Key Window + Root Note) vvv vvvv = 1-127
1011 nnnn	0000 0110	0vvv vvvv	Data Entry MSB *1
1011 nnnn	0000 0111	0vvv vvvv	Volume *1
1011 nnnn	0110 0000	0xxx xxxx	Data Increment *1 xxx xxxx = Ignored
1011 nnnn	0110 0001	0xxx xxxx	Data Decrement *1 xxx xxxx = Ignored
1011 nnnn	0110 0010	0vvv vvvv	Non-Registered Parameter Number LSB *1
1011 nnnn	0110 0011	0vvv vvvv	Non-Registered Parameter Number MSB *1 (see Parameter section for specific values)
1011 nnnn	0110 0100	0vvv vvvv	Registered Parameter Number LSB *1
1011 nnnn	0110 0101	0vvv vvvv	Registered Parameter Number MSB *1 (see Parameter section for specific values)
1011 nnnn	0111 1001	0xxx xxxx	Reset All Controllers *1
1011 nnnn	0111 1010	0000 0000	Local Control Off
1011 nnnn	0111 1010	0111 1111	Local Control On
1011 nnnn	0111 1100	0xxx xxxx	Omni Mode Off
1011 nnnn	0111 1101	0xxx xxxx	Omni Mode On
1100 nnnn	0ppp pppp	---- ----	Program change
1110 nnnn	0mmm mmmm	0nnn nnnn	Pitch Bend Change *1

*1 Recognized only if CONTROLLERS is set to ON in MIDI page

Universal System Exclusive Messages

Byte	Description
1111 0000	Exclusive Status
0111 1110	Non-Real Time Message ID
0uuu uuuu	Universal Sysex Channel (ignored if OMNI = ON, 7FH = any channel)
0000 0110	General Information Sub-ID
0000 0001	Identity Request
1111 0111	EOX

D4 System Exclusive Messages

Byte	Description
1111 0000	Exclusive Status
0000 0000	Manufacturers System Exclusive ID Code
0000 0000	Alesis = 00H,00H,0EH
0000 1110	
0000 0110	Device I.D. (D4 = 6 *D5 = 13H*)
0uuu uuuu	Midi Channel 7FH = Any channel
00oo oooo	Opcode (see Sysex section for opcode definitions and data structures)
0ddd dddd	Data
---- ----	---
1111 0111	EOX

Byte	Description
1111 0000	Exclusive Status
0000 0000	Manufacturers System Exclusive ID Code
0000 0000	Alesis = 00H,00H,0EH
0000 1110	
0000 0110	Device I.D. (D4 = 6 *D5 = 13H*)
0uuu uuuu	Midi Channel 7FH = Any channel
01oo oooo	Data Request (see Sysex section for opcode definitions)
1111 0111	EOX

RECOGNIZED CONTINUOUS CONTROLLER PARAMETERS

The most reliable way to edit a parameter using a registered or non-registered parameter number is to first transmit the parameter number MSB. In the D4 this is always zero, and it only needs to be sent once to initialize registered or non-registered parameter number reception. If both MSB and LSB messages have not been sent, any data entry, data increment, or data decrement messages will alter the parameter selected by the user as indicated by the cursor position in the display.

When a valid parameter number has been set up for editing, the display and cursor will be updated just as though the parameter had been selected from the front panel. (If an associated display exists!) Since it is possible for the user to select a new parameter for editing from the front panel between a series of data entry, data increment, or data decrement messages, it is strongly recommended that the parameter number LSB always be re-sent immediately before transmitting any of these controllers. This will insure that they are always acting on the intended parameter.

The actual 7 bit values for continuous controller messages 96 (data increment) and 97 (data decrement) are ignored. Likewise, continuous controller message 38 (data entry LSB) is ignored. To find the value of the 7 bit data entry MSB message (controller 6) to transmit in order to select a real-life setting, multiply the desired value by 127, and divide the result by the maximum allowable value for that parameter.

For example, the data entry MSB value used to set the Preview note's volume to 50 is 64 because:

50 x 127 / 99 = 64

The data entry MSB value used to set the Drum set's Root Note's to 44 is 83 because:

44 x 127 / 67 = 83

Registered Parameter Numbers for Controllers 100 (LSB) and 101 (MSB)

MSB	LSB	Description
00H	00H	Pitch bend sensitivity. (maximum range = +/- 12 semitones)

Non-Registered Parameter Numbers for Controllers 98 (LSB) and 99 (MSB)

Trigger Parameters:

MSB	LSB	Description	Range
00H	00H	Select active trigger.	0-11
00H	01H	Active trigger v-curve.	0-7
00H	02H	Active trigger note number.	0 to 60 + Root Note
00H	03H	Active trigger gain.	0-99
00H	04H	Active trigger cross-talk.	0-99
00H	05H	Active trigger decay.	0-99
00H	06H	Active trigger noise floor.	0-99
00H	07H	Ignored	

Preview note specific:

MSB	LSB	Description	Range
00H	08H	Preview note drum bank	Kik, Snr, Cym, Tom, Prc, Efx *Kik, Snr, Tom Cym, Prc, Efx, Rnd*
00H	09H	Preview note drum sound.	Bank dependent
00H	0AH	Preview note coarse tune.	-4 to +3 semitones
00H	0BH	Preview note fine tune.	0 to +99 cents
00H	0CH	Preview note volume.	0 to 99
00H	0DH	Preview note pan.	<3, <2, <1, <>, 1>, 2>, 3>
00H	0EH	Preview note output pair.	MAIN, AUX
00H	0FH	Preview note assign group.	MULTI, SINGLE, GROUP1, GROUP2

Midi parameters:

MSB	LSB	Description	Range
00H	10H	Drumset root note	0-67
00H	11H	Midi channel.	1-16
00H	12H	Midi THRU.	OFF, ON, *FLO*
00H	13H	Program change enable.	OFF, ON
00H	14H	Controller enable.	OFF, ignored if already off!
00H	15H	Program table source.	0 to 127
00H	16H	Program table destination.	0 to 20
00H	17H	Ignored. *MIDI LOCAL*	*On, Off*

Miscellaneous:

MSB	LSB	Description	Range
00H	18H	Note Chase enable	Off, On
00H	19H	Quietly select preview note.	0 to 60 + Root Note
00H	1AH	Flange Rate.	0 = fast, 127 = slow
00H	1BH	Footswitch mode.	Hi Hat Pedal, Drumset Advance
00H	1CH	Footswitch close note.	0 to 60 + Root Note
00H	1DH	Footswitch held note.	0 to 60 + Root Note
00H	1EH	Ignored	
00H	1FH	Ignored	

Drumset Management:

MSB	LSB	Description	Range
00H	20H	Drumset name char 1	16-127
00H	21H	Drumset name char 2	16-127
00H	22H	Drumset name char 3	16-127
00H	23H	Drumset name char 4	16-127
00H	24H	Drumset name char 5	16-127
00H	25H	Drumset name char 6	16-127
00H	26H	Drumset name char 7	16-127
00H	27H	Drumset name char 8	16-127
00H	28H	Drumset name char 9	16-127
00H	29H	Drumset name char 10	16-127
00H	2AH	Drumset name char 11	16-127
00H	2BH	Drumset name char 12	16-127
00H	2CH	Drumset name char 13	16-127
00H	2DH	Drumset name char 14	16-127
00H	2EH	Store Drumset destination	0-20
00H	2FH	Store Drumset	False / True *On the D5 Asserting this acts as would the store button.*
00H	30H	Recall Alesis Drumset srce.	0 to 20
00H	31H	Recall Alesis Drumset dest.	0 to 20
00H	32H	Recall all Alesis Drumsets.	False / True *On the D5 first assert this, then press the store button (or assert Store Drumset)*
00H	33H thru 7FH	Ignored.	

SYSTEM EXCLUSIVE OPCODES AND DATA STRUCTURES

General Format:

All transmitted and received D4 system exclusive messages follow this template:

On the D4- F0H,00H,00H,0EH,06H,cc,qq,DATA ,F7H
On the D5-F0H,00H,00H,0EH,13H,cc,qq,DATA ,F7H

If the message originated from the D4/D5 the sixth byte "cc" will always be the same as the midi channel. If an originator wishes to send a system exclusive message to any D4 regardless of what midi channel is selected, "cc" should be set to 7FH. In addition, a D4/D5 set to OMNI will process all system exclusive messages it receives.

The seventh byte "qq" is the opcode. If bit 6 of this opcode is set the message is a data request and the opcode is always followed immediately by an end-of-exclusive status byte. Opcodes with bit 6 cleared are data dump headers that identify the type of data that is to follow. In either case, the lower six bits of the opcode represent the same data structure, whether the message is a data request or a data dump.

Most system exclusive messages on the D4 include a checksum byte after the data immediately before the F7H end-of-exclusive status byte. This checksum is the modulo 128 addition of all the data bytes contained in the message starting with the byte immediately following the opcode.

Opcode	Description	Length (Total bytes)	Checksum
0000 0000	System Info	11	No
0000 0001	Drumset Data for Edit Buffer	343	Yes
0000 0010	Old Trigger Setup (version 1.01 only)	33	Yes
0000 0011	Program Change Table	137	Yes
0000 0100	Display Message	40	No
0000 0101	New Trigger Setu	69	Yes
0000 0110	Reserved / Unused	x	x
---- ----	---	x	x
---- ----	---	x	x
0001 1111	Reserved / Unused	x	x
001p pppp	Drumset Data for Drumset 0-20	343	Yes
0011 0101	Reserved / Unused	x	x
---- ----	---	x	x
---- ----	---	x	x
0011 1111	Reserved / Unused	x	x
01qq qqqq	Requests for opcodes 0-63	8	No

When a "SYSTEM (ALL)" bulk dump is initiated from the front panel the D4's entire memory contents get transmitted out MIDI in a series of 25 system exclusive messages. This series begins with the Program Change Table message, and is followed by the Trigger Setup message, the Edit Buffer message, 21 consecutive Single Set messages (beginning with Drumset 0), and finally the System Info message.

Note that it is possible in some systems to overflow the D4's midi receive buffer when sending data for more than one drumset. If this happens the transmitting device should pause for at least 250 milliseconds every 256 bytes to insure that the receiving D4 has enough time to manage drumset memory.

Message 0 / System Info

Data Format (following header):

Byte	Bit Field	Description
7	0000 0000	Opcode = System Info
8	0bbb bbbb	System Byte (see specific bit definitions following)
9	0000 nnnn	Midi Channel (0-15)
10	000s ssss	Currently selected drumset (0-20)
11	1111 0111	EOX

System Byte Bit Definitions:

Bit	Function	Polarity
0	Omni Off	Set if omni mode is off.
1	Midi Thru Enable	Set if MIDI thru is enabled.
2	Program Change Enable	Set if program change receive is enabled.
3	Controllers Enable	Set if MIDI controllers are enabled.
4	Drumset Edited	Set if drumset in edit buffer has changed.
5	Footswitch Mode	0 = Hi Hat, 1 = Drumset Advance
6	Note Chase Enable	Set if Note Chase is on.

Message 1 / Edit Buffer
Data Format (following header):

Byte	Bit Field	Description	Range
7	0000 0001	Opcode = Edit Buffer	
8	0aaa aaaa	Drumset name character 1	(ascii)
9	0aaa aaaa	Drumset name character 2	(ascii)
---	---- ----	---	---
---	---- ----	---	---
21	0aaa aaaa	Drumset name character 14	(ascii)
22	0mmm mmmm	Drumset Root Note	(0-67)
23	00nn nnnn	Footswitch "closing" note	(0-60)
24	00nn nnnn	Footswitch "held" note	(0-60)
25	00nn nnnn	Trigger 1 note number	(0-60)
26	00nn nnnn	Trigger 2 note number	(0-60)
---	---- ----	---	---
---	---- ----	---	---
36	00nn nnnn	Trigger 12 note number	(0-60)
37-41	---- ----	Data packet for note 0	(see below for packet definitions)
42-46	---- ----	Data packet for note 1	---
---	---- ----	---	---
---	---- ----	---	---
337-341	---- ----	Data packet for note 60	---
342	0xxx xxxx	Checksum	(0-127)
343	1111 0111	EOX	

Note Data Packet Definitions (5 bytes per note):

Byte	Bit Field	Description
0	0vvv vvvv	v = volume (0-99)
1	0ppp obbb	p = panning: 0=left, 3=center , 6=right o = output: 0=main, 1 = aux b = drum bank: (0-6) Kik, Snr, Cym, Tom, Prc, Efx *{0-8} Kik, Snr, Tom, Hat, Cym, Prc, Efx, Rnd*
2	0nnn nnnn	n = drum number (0-99, drum bank specific)
3	0fff ffff	f = fine tuning (0-99 cents)
4	0xxg gccc	x = reserved, always 0 g = assign group (0-3): 0=multi, 1=single, 2=group 1, 3=group 2 c = coarse tuning (-4,+3 semitones)

Message 2 / Old Trigger Setup (version 1.01 only)
Data Format (following header):

Byte	Bit Field	Description	Range
7	0000 0010	Opcode = Trigger Setup	
8	000t tttt	Trigger 1 gain	(0-99)
9	000t tttt	Trigger 2 gain	(0-99)
---	---- ----	---	---
---	---- ----	---	---
19	000t tttt	Trigger 12 gain	(0-99)
20	000t tttt	Trigger 1 type	(0-25)
21	000t tttt	Trigger 2 type	(0-25)
---	---- ----	---	---
---	---- ----	---	---
31	000t tttt	Trigger 12 type	(0-25)
32	0xxx xxxx	Checksum	(0-127)
33	1111 0111	EOX	

Message 3 / Program Table
Data Format (following header):

Byte	Bit Field	Description	Range
7	0000 0011	Opcode = Program table	
8	000p pppp	Internal Drumset selected for external program change 0	(0-20)
9	000p pppp	Internal Drumset selected for external program change 1	(0-20)
-	---- ----	---	---
-	---- ----	---	---
135	000p pppp	Internal Drumset selected for external program change 127	(0-20)
136	0xxx xxxx	Checksum	(0-127)
137	1111 0111	EOX	

Message 4 / Display Message
This message will display 32 characters on the LCD for approximately 5 seconds and then restore the previous display.
Data Format (following header):

Byte	Bit Field	Description	Range
7	0000 0100	Opcode = Display Message	
8	0aaa aaaa	LCD character position 0	(ascii)
9	0aaa aaaa	LCD character position 1	(ascii)
---	---- ----	---	---
---	---- ----	---	---
39	0aaa aaaa	LCD character position 31	(ascii)
40	1111 0111	EOX	

Message 5 / New Trigger Setup (versions 1.02 and greater)
Note that the D5 can both transmit and receive trigger setups to and from a D4.
Data Format (following header):

Byte	Bit Field	Description	Range
7	0000 0101	Opcode = New Trigger Setup	
8	0ggg gggg	Trigger 1 gain	(0-99)
9	0ggg gggg	Trigger 2 gain	(0-99)
-	---- ----	---	---
-	---- ----	---	---
18	0ggg gggg	Trigger 11 gain	(0-99)
19	0ggg gggg	Trigger 12 gain	(0-99)
20	0000 0ccc	Trigger 1 vcurve	(0-7)
21	0nnn nnnn	Trigger 1 cross-talk	(0-99)
22	0xxx xxxx	Trigger 1 noise floor	(0-99)
23	0ddd dddd	Trigger 1 decay	(0-99)
24	0000 0ccc	Trigger 2 vcurve	(0-7)
25	0nnn nnnn	Trigger 2 cross-talk	(0-99)
26	0xxx xxxx	Trigger 2 noise floor	(0-99)
27	0ddd dddd	Trigger 2 decay	(0-99)
-	---- ----	---	---
-	---- ----	---	---
64	0000 0ccc	Trigger 12 vcurve	(0-7)
65	0nnn nnnn	Trigger 12 cross-talk	(0-99)
66	0xxx xxxx	Trigger 12 noise floor	(0-99)
67	0ddd dddd	Trigger 12 decay	(0-99)
68	0xxx xxxx	Checksum	(0-127)
69	1111 0111	EOX	

Messages 32 thru 52 / Single Drumset Only

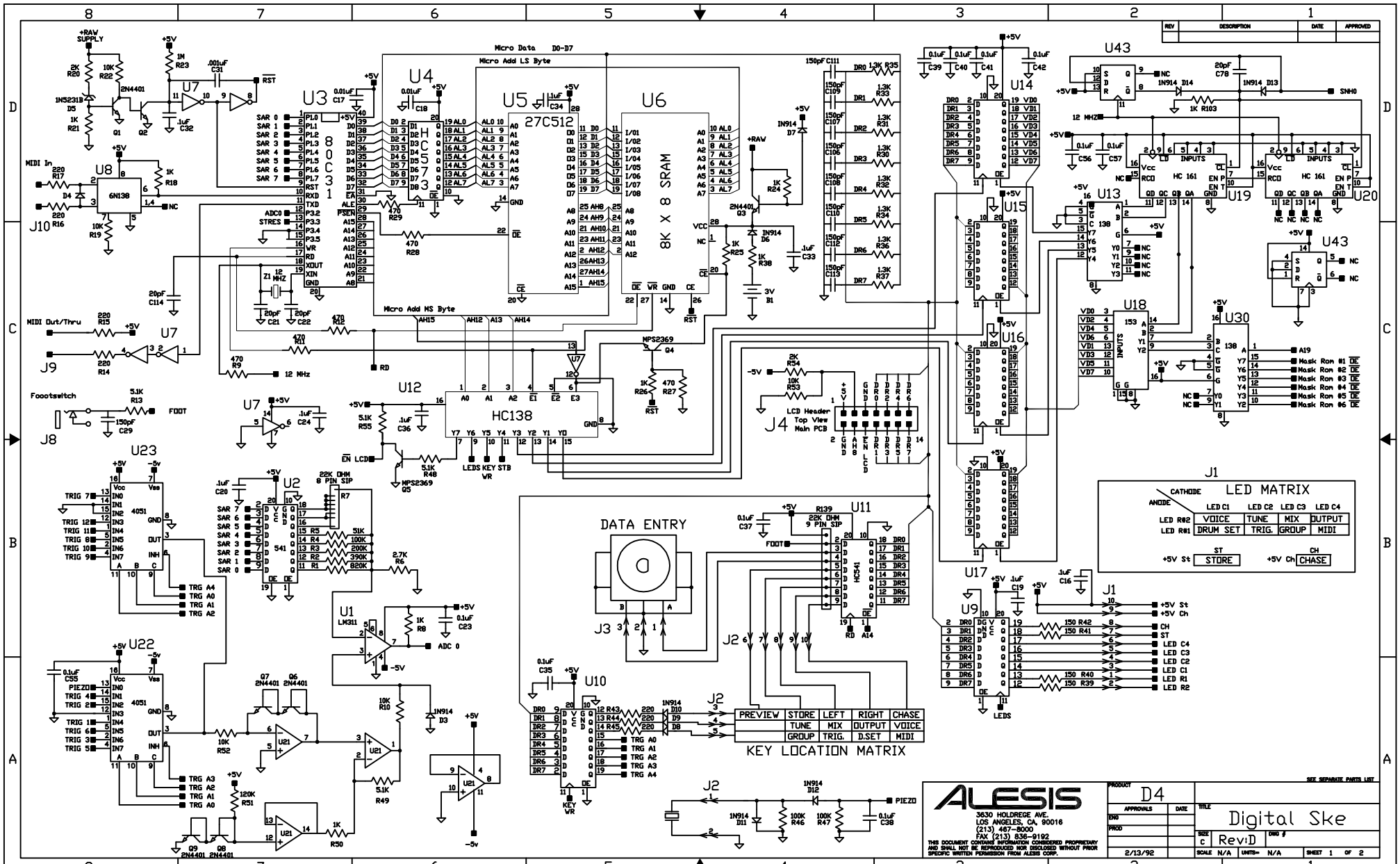
These messages contain the same Drumset data structures as the Edit Buffer message and are identical, with the exception of the opcode byte. When a D4 receives a complete Single Drumset message it will automatically "Store" the data in one of the 21 memory locations (as specified in the opcode) replacing the existing Drumset data for that slot. Its important to note that this new Drumset data does not effect the edit buffer. For a detailed listing of the Drumset data structure see the description under **Message 1 / Edit Buffer**.

12.00 Service Manual History

10/17/95 V1.00 Preliminary Release

13.00 Schematics

13.10 D4 Schematics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U4
HC573
U5
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U6
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U7
U8
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U9
U10
U11
U12
HC138
U13
U14
U15
U16
U17
U18
U19
U20
U22
U23
U30
U43
Micro Data D0-D7
Micro Add LS Byte
Micro Add MS Byte
MIDI In
MIDI Out/Thru
Foootswitch
FOOT
LCD Header
Top View
Main PCB
DATA ENTRY
KEY LOCATION MATRIX
PREVIEW
STORE
LEFT
RIGHT
CHASE
TUNE
MIX
OUTPUT
VOICE
GROUP
TRIG.
D.SET
MIDI
LED MATRIX
CATHODE
ANODE
LED C1
LED C2
LED C3
LED C4
LED R#2
LED R#1
VOICE
TUNE
MIX
OUTPUT
DRUM SET
TRIG.
GROUP
MIDI
ST
STORE
CH
CHASE
+5V St
+5V Ch
LED R2
LED R1
LED C1
LED C2
LED C3
LED C4
LEDS
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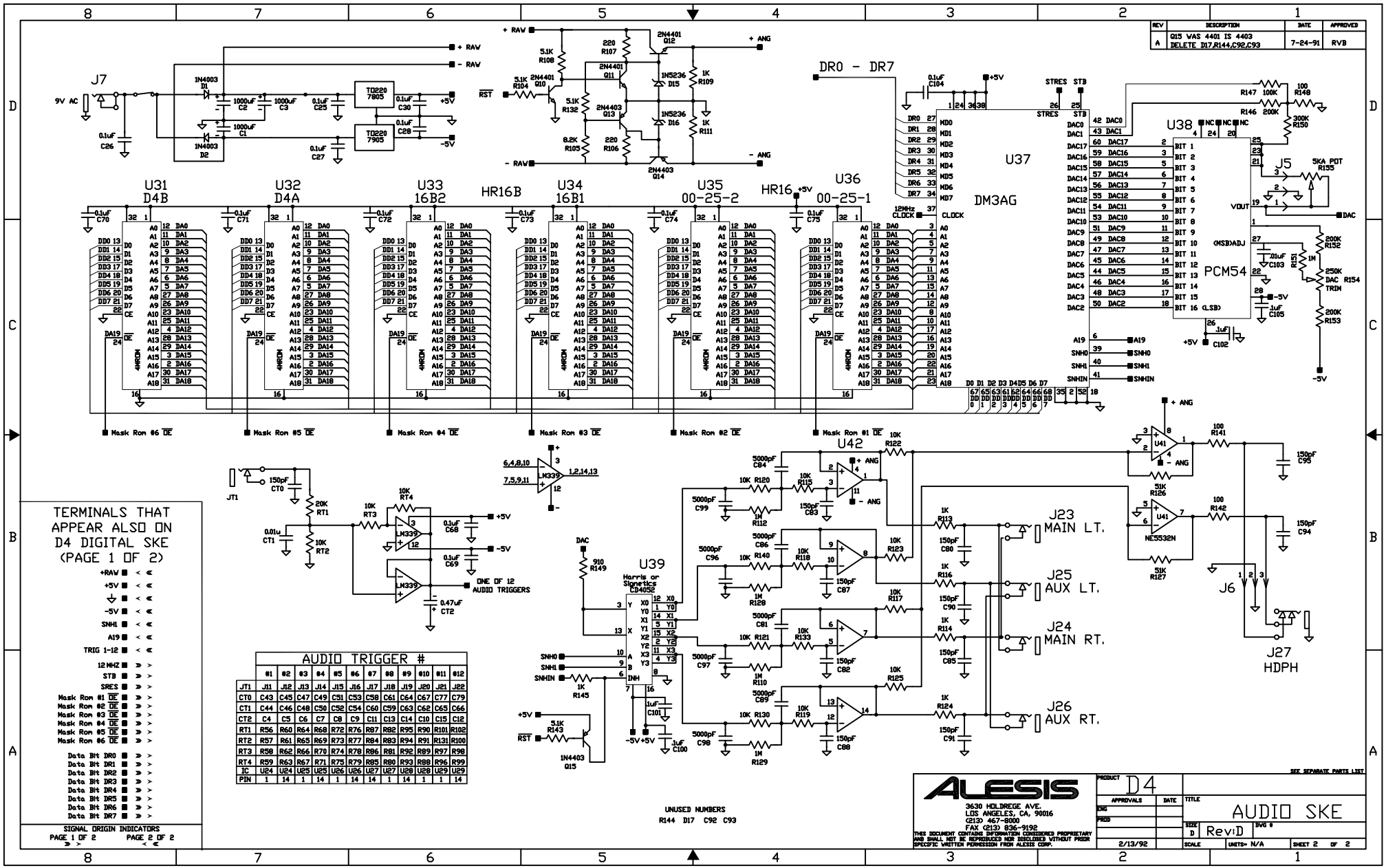
PRODUCT
D4
APPROVALS
DATE
ENG
PROD
2/13/92
TITLE
Digital Ske
SIZE
C
Rev:D
DWG #
SCALE N/A
UNITS= N/A
SHEET 1 OF 2
SEE SEPARATE PARTS LIST
REV
DESCRIPTION
DATE
APPROVED



REV	DESCRIPTION	DATE	APPROVED
A	Q15 WAS 4401 IS 4403 DELETE D17,R144,C92,C93	7-24-91	RVB

TERMINALS THAT APPEAR ALSO ON D4 DIGITAL SKE (PAGE 1 OF 2)

+RAW
+5V
-5V
SNH1
A19
TRIG 1-12
12 MHZ
STB
SRES
Mask Rom #1 OE
Mask Rom #2 OE
Mask Rom #3 OE
Mask Rom #4 OE
Mask Rom #5 OE
Mask Rom #6 OE
Data Bit DR0
Data Bit DR1
Data Bit DR2
Data Bit DR3
Data Bit DR4
Data Bit DR5
Data Bit DR6
Data Bit DR7

SIGNAL ORIGIN INDICATORS
PAGE 1 OF 2 PAGE 2 OF 2

AUDIO TRIGGER #

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12
JT1	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20	J21	J22
CT0	C43	C45	C47	C49	C51	C53	C58	C61	C64	C67	C77	C79
CT1	C44	C46	C48	C50	C52	C54	C60	C59	C63	C62	C65	C66
CT2	C4	C5	C6	C7	C8	C9	C11	C13	C14	C10	C15	C12
RT1	R56	R60	R64	R68	R72	R76	R87	R82	R95	R90	R101	R102
RT2	R57	R61	R65	R69	R73	R77	R84	R83	R94	R91	R131	R100
RT3	R58	R62	R66	R70	R74	R78	R86	R81	R92	R89	R97	R98
RT4	R59	R63	R67	R71	R75	R79	R85	R80	R93	R88	R96	R99
IC	U24	U24	U25	U25	U26	U26	U27	U27	U28	U28	U29	U29
PIN	1	14	1	14	1	14	14	1	14	1	1	14

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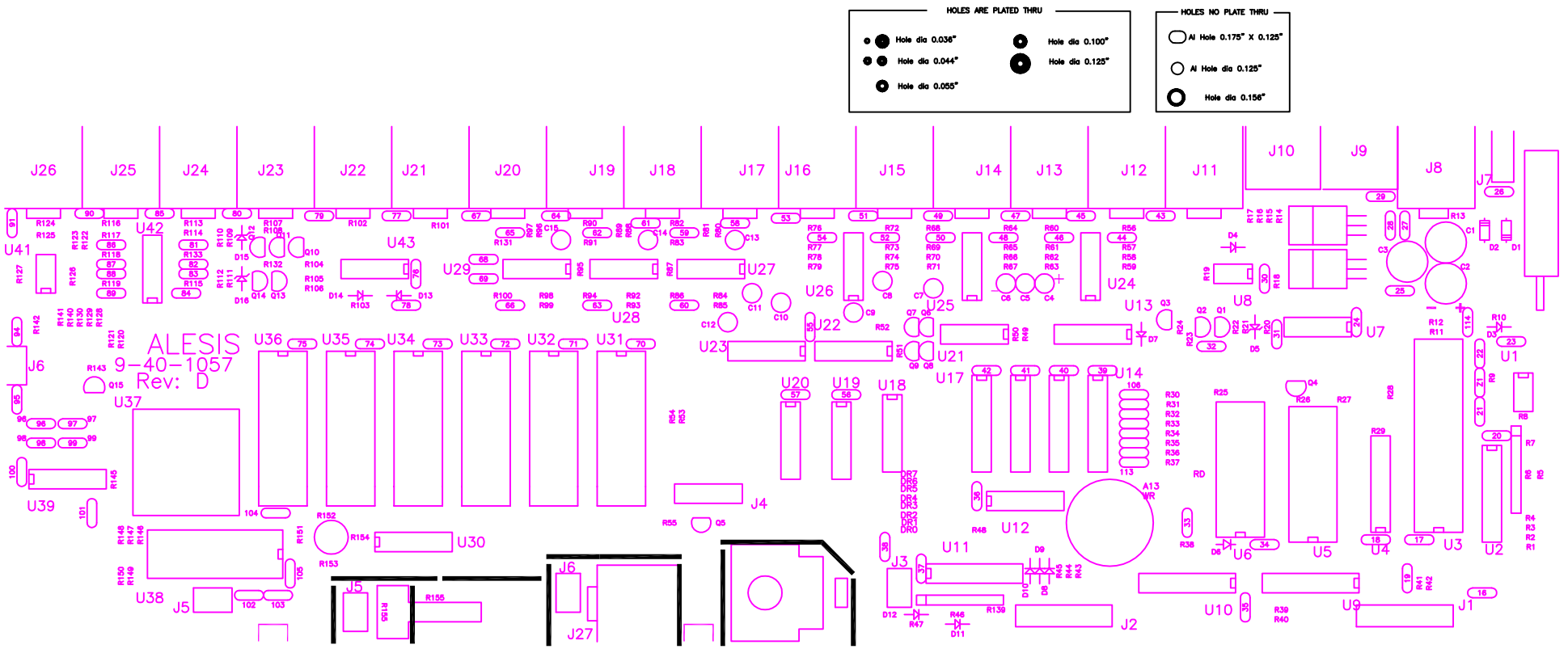
PRODUCT D4
APPROVALS DATE
ENG
PROD
2/13/92

TITLE AUDIO SKE
SIZE D REV:D SVG #
SCALE UNITS= N/A SHEET 2 OF 2

SEE SEPARATE PARTS LIST

Reduce to 409.00mm +/- 0.10mm between targets



Reduce to 409.00mm +/- 0.10mm between targets

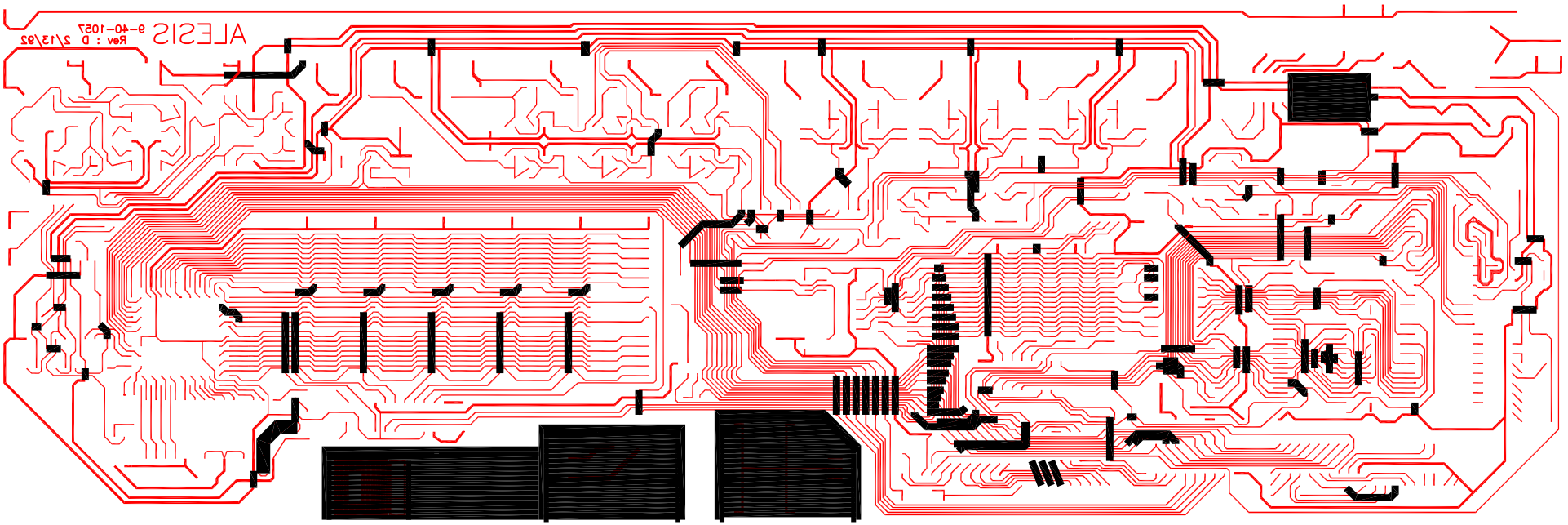
ALESIS
9-40-1057
Rev : D
2/13/92

HOLES ARE PLATED THRU

- Hole dia 0.036"
- Hole dia 0.044"
- Hole dia 0.055"
- Hole dia 0.100"
- Hole dia 0.125"

HOLES NO PLATE THRU

- Al Hole 0.175" X 0.125"
- Al Hole dia 0.125"
- Hole dia 0.156"



INDEX

NOTES