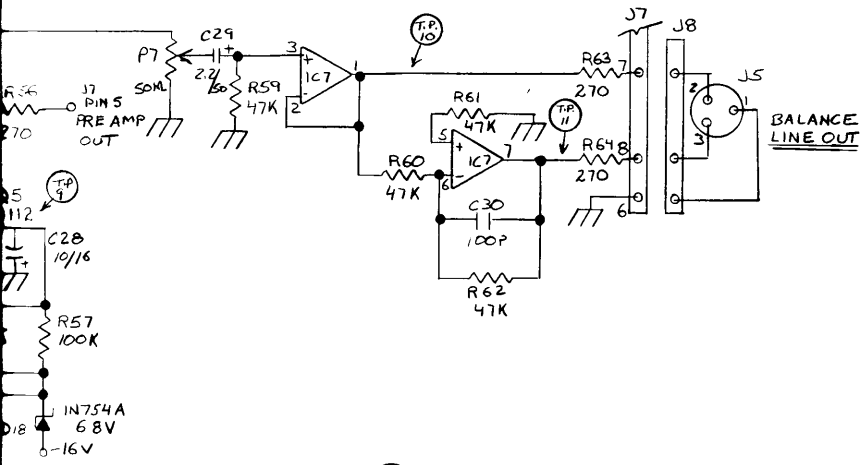


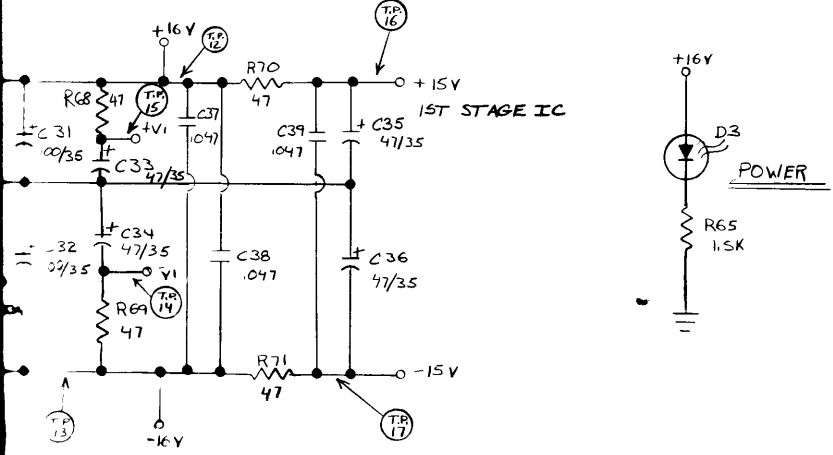
TEST CONDITIONS: TONES @ 5, 10 & 15 KHZ, BALANCED LINE OUT @ 10 W/100 OHM LOAD, 1 KHZ INPUT.



TEST PT.	LIMITER "ON" 2.2 VP-P INP	LIMITER "OFF" .22 VP-P INP
1	16 VP-P	OVDC
2	26 VP-P	OVDC
3	28 VP-P	OVDC
4	1 VP-P	OVDC
5	3 VP-P	OVDC
6	30 VP-P J-L	-11 VDC (AVE)
7	30 VP-P J-L	-11 VDC (AVE)
8	0	3.5 VDC
9	0	-10 VDC
10	3 VP-P	OVDC
11	3 VP-P	OVDC
12	40 MVP-P RIPPLE	17 VDC
13	40 MVP-P RIPPLE	-17 VDC
14	30 MVP-P RIPPLE	-17 VDC
15	30 MVP-P RIPPLE	17 VDC
16	80 MVP-P RIPPLE	17 VDC
17	80 MVP-P RIPPLE	-17 VDC

NOTE: UNDER THESE CONDITIONS, PEAK INDICATOR IS LIT.

NOTES: 1) ADJUST AP-1 FOR UNITY GAIN FROM T.P.3 TO T.P.5 WITH LIMITER "OFF".



PCB# 06AS11-01
A-F DESIGNED

TOLERANCES (EXCEPT AS NOTED)	REVISIONS			PREAMP SCHEMATIC	
	NO.	DATE	BY	SVT-70T/BIS-T/SVT-100T	
DECIMAL	1	12-28-87	S.A.	SLM ELECTRONICS	
FRACTIONAL	2			1400 FERGUSON ST. LOUIS MO. 63133	
ANGULAR	3			DRAWN BY J.C.	SCALE
	4			CHECK'D T.E.	DATE 1-5-87
	5			TRACED	APP'D
	6				DRAWING NO. 16-406-01