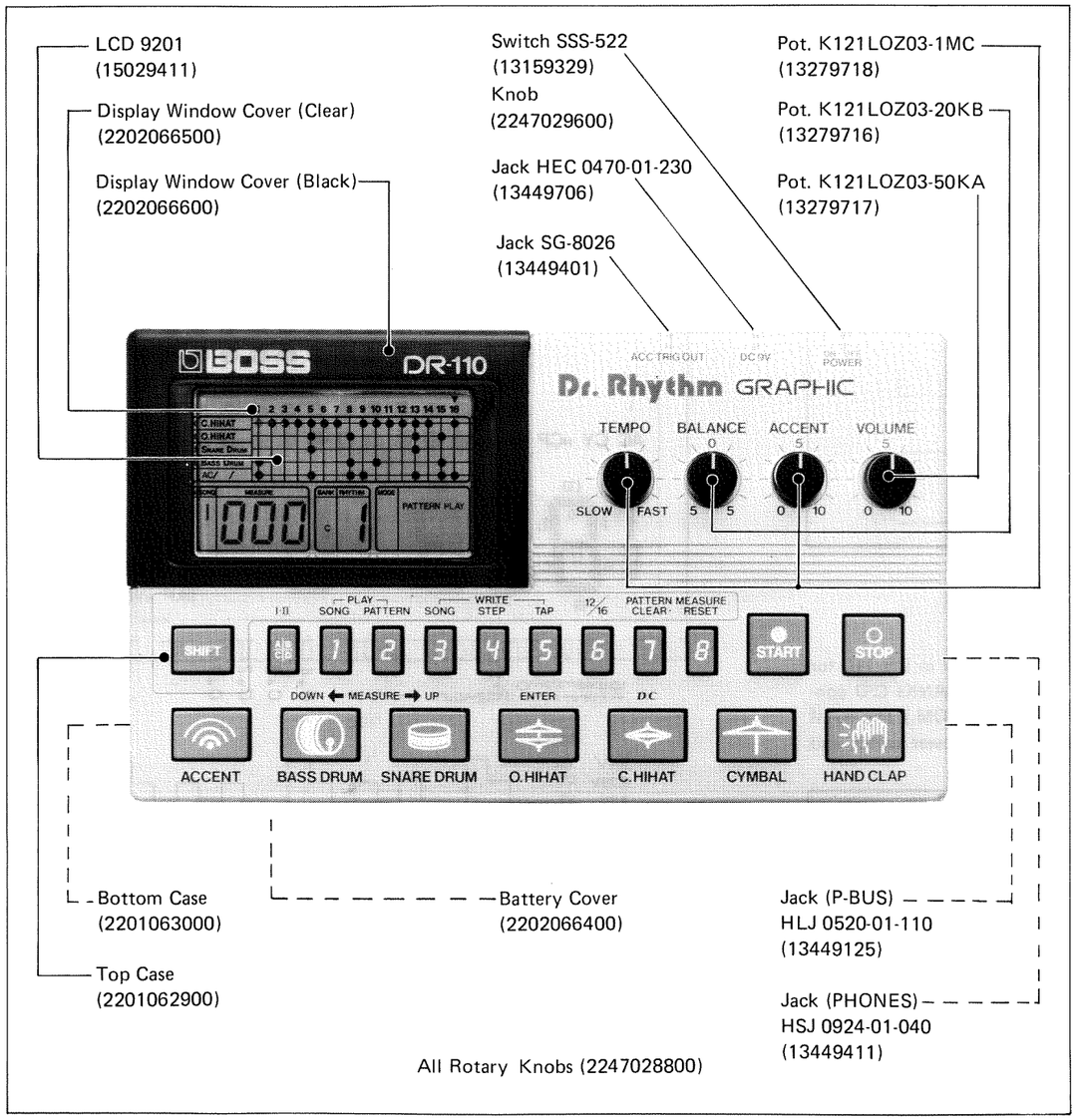
BOSS DR-110 SERVICE NOTES

First Edition

SPECIFICATIONS

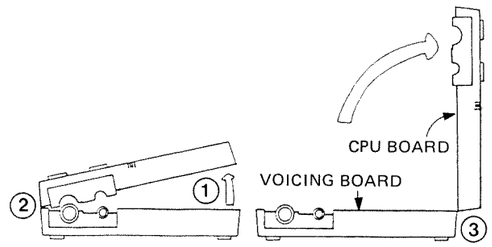
Power	: 9VDC (battery or AC adaptor)
Current Draw	: 7mA (at no signal) to 12mA (max.) @9V
Headphone Impedance	: 8Ω to 100Ω
P-BUS Impedance	: 10KΩ (IN/OUT)
ACC TRIG OUT Signal	: +6V, 10ms-width
Dimensions	: 190(W) x 110(D) x 30(H) mm 7-1/2(W) x 4-5/16(D) x 1-3/16(H) in
Weight	: 450g / 1 lb. (including batteries)



DISASSEMBLY

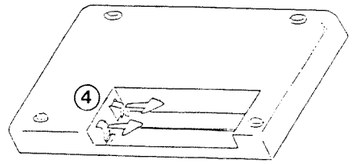
Exposing PCBs

1. Remove 4 rotary knobs.
2. Remove 3 x 12mm P type screws on Bottom case.
3. Open Top case, first at the rear end ①, gently push rearwards (unlock), then open at the front end ②. Insert a cloth between panels to protect the rear surface of top panel from scratching. This allows troublshooting for both PCBs while maintaining the unit operative from built-in drycells.



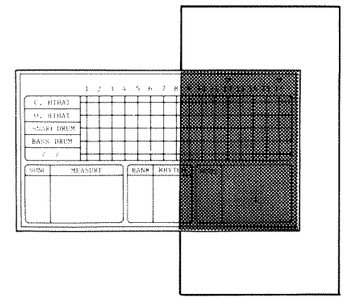
Dismounting VOICING Board

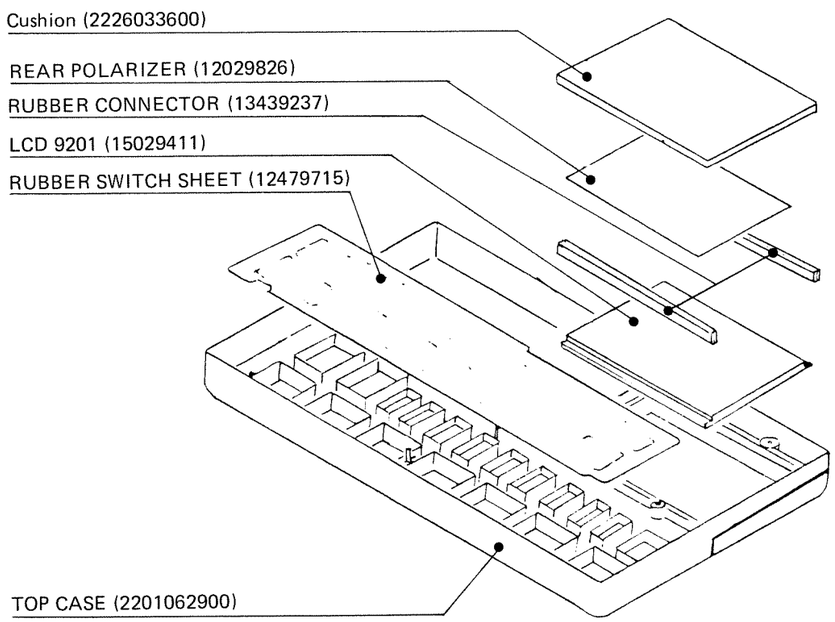
1. Remove Battery compartment cover and remove the dry cells.
2. Unlatching Battery clips ④, raise Bottom case.



LCD ASSEMBLY

Avoid unnecessary service to LCD Ass'y.
When reassembling, make sure that the face (not rear) of Rear Polarizer touches LCD.
The correct layer makes display dark when the LCD and polarizer are placed crosswise.

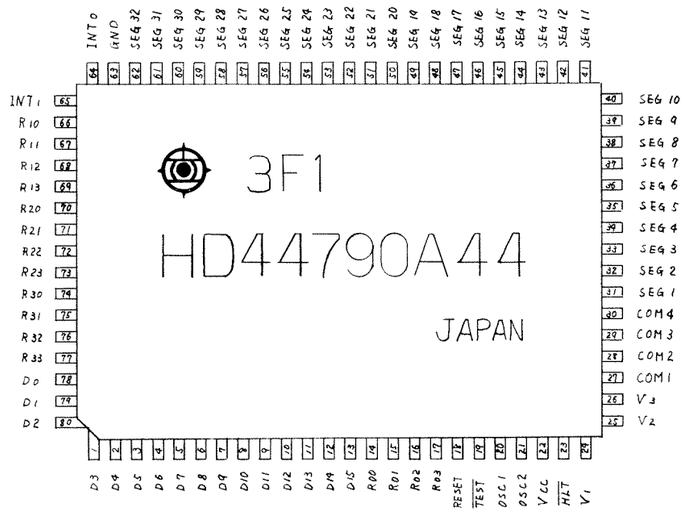




CIRCUIT DESCRIPTIONS

CPU IC1

HD44790A44 is a 2K word by 4 bit one chip CMOS microcomputer equipped with internal LCD drivers.



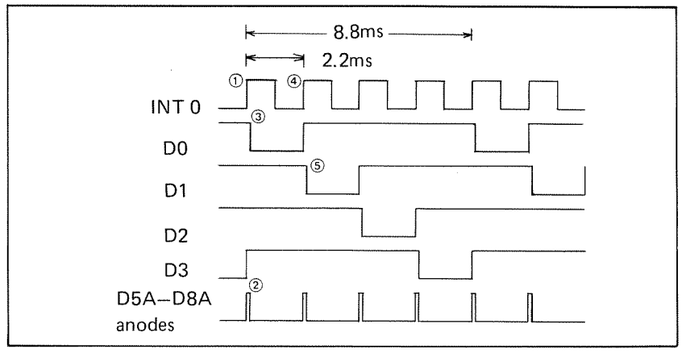
CPU HD44790A-44 PIN FUNCTIONS

Symbol	Name	Description
R00 R01 R02 R03	Input Port	Read in Key switches and TEMPO CLOCK.
R10 R11 R12 R13	I/O Port	External Memory Data Bus (Rhythm patterns A/B, Songs I/II)
R20 R21 R22 R23		External Memory Address Bus P20–P23: Used as OUTPUT Port.
R30 R31 R32 R33	Output Port	
D0 D1 D2 D3	Descrete I/O terminals	Output Switches and Tempo Clock Scanning signals.
D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15		External Memory Address Bus $\overline{WE}$ Memory Write Enable $\overline{CS}$ Memory Chip Select CH, OH, SD, BD, AC, CY, CPI, CPII: Output Trigger pulse to VOICEs.
INT 0 INT 1	Interrupt Inputs	Interrupt Input for Switch Scanning OPEN-pulled up internally
RESET	Reset Input	Accepts 400ms-width pulse on Power-up.
$\overline{HLT}$	Halt Input	When "low", the CPU retains all internal circuit status as they are.
$\overline{TEST}$	Test Input	No customer usable terminal.
V1 V2 V3	LCD DC Supply Inputs	Used as LCD driver signals.
Vcc	DC Supply Input	+5V (±10%) also used as LCD DC supply
GND	Ground Input	GND
SEG 1 ↓ SEG 32	SEGMENT Outputs	Output LCD drive signals
COM 1 ↓ COM 4	Common Outputs	Output LCD drive signals in 1/4 duty, 1/3 bias.

SWITCH MATRIX (See Fig. below)

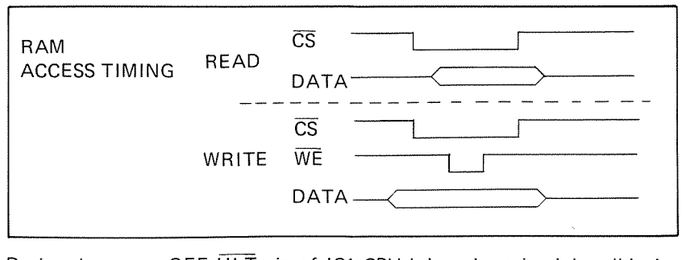
① The CPU enters external interrupt routine on a rising edge of INT CLK from IC2a, b which also serve as a part of CY Sound Generator, and reads in TEMPO CLK and key switches through ports D0–D3 and through R00–R03.
② In reading the aboves, the CPU first turns ports D0–D3 "H", cutting off D5A–D8A, D5B–D8B and D1B–D4B, disconnecting the diodes from IC3 NAND gates and the ports R00–R03. With an H being applied on one input pin, each gate of IC3 will turn its output to "L" when the other input pin is H (closing of STOP, START or BANK, or during H period of TEMPO CLK). Ports R00–R03 are pulled up internally and go low when their mate IC3 outputs turn to L.
③ Next, the CPU IC1 sets port D0 to "L" which pulls one inputs of IC3 down to low, turning all IC3 outputs to "H", reverse biasing D1A–D4A which in turn isolate IC3 from the read-in ports. Each of ports R00–R03 can be connected to port D0 through closed contacts (of CH, OH, SD or BD) and through D8B. Then the program returns to the main routine.
④ On the next rising edge of INT CLK, the program enters interrupt routine again and gates IC3.
⑤ Having reading IC3 outputs, this time the program sets D1 to L and reads SHIFT, CP, CY and AC switches through R0 ports.

The CPU repeats the same procedures for the remaining D ports and returns to ①, cycling TEMPO CLK, STOP, START and BANK readings at 2.2ms internals, and other switch groups at 8.8ms intervals.



MEMORY BACKUP

IC2 μPD444C is a 1K-word by 4 bits static RAM. It is used in DR-110 for storing BANKs A/B, SONGs I/II and STEPs 12/16 data. (BANKs C/D containing factory-set rhythms are stored into CPU's internal ROM.) The RAM memory is backed up by built-in battery which bypasses power switch and connects to RAM's VCC, $\overline{WE}$ and $\overline{CS}$ pins.

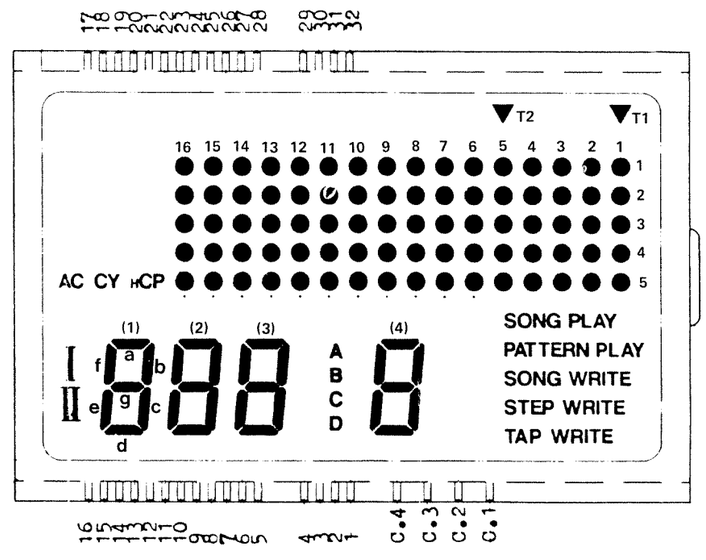


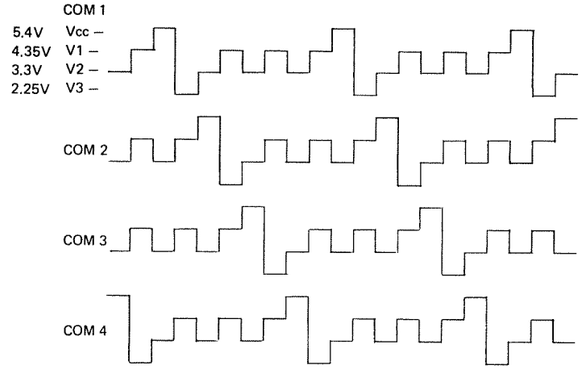
During the power OFF $\overline{HLT}$ pin of IC1 CPU is kept L, maintaining all its input and output pins high impedance, isolating its circuits from peripheral circuits and thus retains all the data so far obtained. When the CPU is repowered, it initializes internal circuits but still keeps some data intact.

LCD

Each segment in LCD has a pair of electrodes. Electrodes on one glass plate are grouped into four common (COM) terminals and the other plate electrodes into SEGs as shown below.

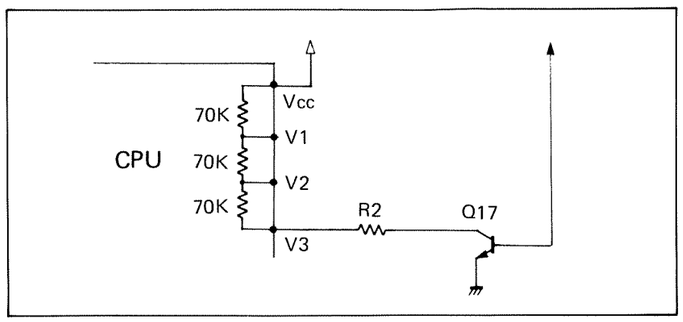
No.	COM.1	COM.2	COM.3	COM.4	No.	COM.1	COM.2	COM.3	COM.4
C.1	COM.1				15	II	1g	1b	15-5
C.2		COM.2			16	I	1f	1a	16-5
C.3			COM.3		17	16-1	16-2	16-3	16-4
C.4				COM.4	18	15-1	15-2	15-3	15-4
1	TAP W.	4d	——	1-5	19	14-1	14-2	14-3	14-4
2	STEP W.	4e	4c	2-5	20	13-1	13-2	13-3	13-4
3	SONG W.	4g	4b	3-5	21	12-1	12-2	12-3	12-4
4	PAT. P.	4f	4a	4-5	22	11-1	11-2	11-3	11-4
5	SONG P.	3d	——	5-5	23	10-1	10-2	10-3	10-4
6	D	3e	3c	6-5	24	9-1	9-2	9-3	9-4
7	C	3g	3b	7-5	25	8-1	8-2	8-3	8-4
8	B	3f	3a	8-5	26	7-1	7-2	7-3	7-4
9	A	2d	——	9-5	27	6-1	6-2	6-3	6-4
10	T1	2e	2c	10-5	28	5-1	5-2	5-3	5-4
11	T2	2g	2b	11-5	29	4-1	4-2	4-3	4-4
12	AC	2f	2a	12-5	30	3-1	3-2	3-3	3-4
13	CY	1d	——	13-5	31	2-1	2-2	2-3	2-4
14	CP	1e	1c	14-5	32	1-1	1-2	1-3	1-4





COM1–COM4 WAVEFORMS & TIMING

The LCD operates dynamically in 1/4 duty cycles and 1/3 bias. Each segment reads out when its COM terminal receives 2.25V(V3) and SEG terminal 5.4V (VCC) - - - this voltage difference will provide the sharp edged, most visible readout.
When the DC supply drops, Q17 increases resistance, further decreasing potential difference between COM and SEG terminals, which causes the readout duller. This effectively functions as a battery indicator.



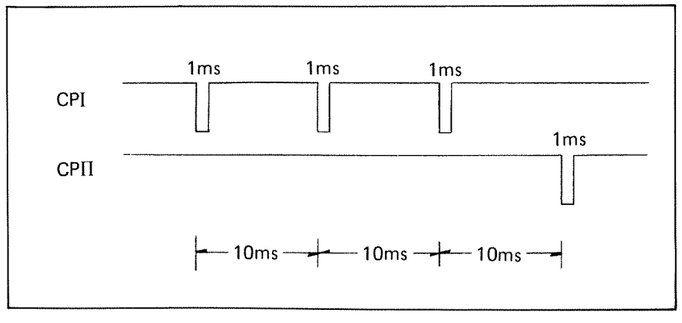
TRIG OUT

Ports D8–D15 of the CPU are normally at +6V and go to 0V for 1ms when triggering designated voice.

ACC TRIG – AC TRIG pulse passing D9 is lengthened and inverted to become positive 10ms-wide pulse and is routed to ACC TRIG OUT jack.

ACCENT – The AC TRIG pulse passing through Q18 conducts Q20 and Q21 until its fall time determined by the time constant, connecting ACCENT VR3 in parallel with audio signal path.

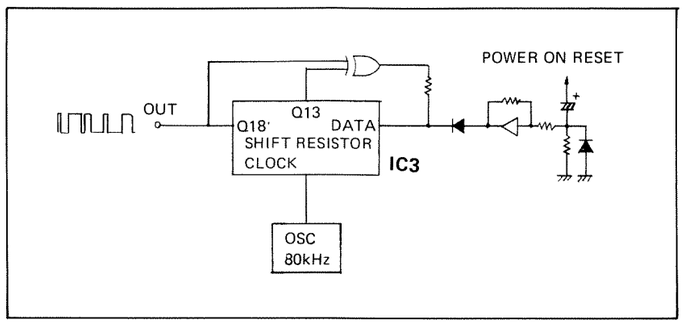
HAND CLAP – For Hand Clap two trigger pulses of different timing are provided to simulate reverbration effect.



NOISE GENERATOR

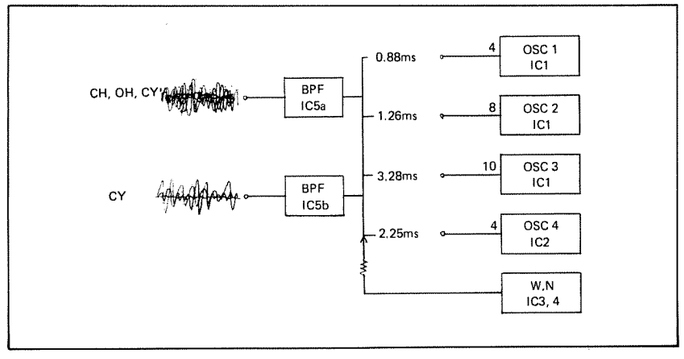
IC3 and IC4 are configured to function as a quasi-random impulse generator, a generation of a succession of random signals which are distributed over a wide frequency spectrum. On power-up, Power-ON Reset circuit turns pin 1 of IC3 H as a data "1". Because the shift register will not operate when its all D pins are at 0.

NOTE: Intermitent DC supply (such as loose AC adaptor or battery connection or quick turning OFF-ON of the power switch) may upset Power–ON Reset when a transient of DC voltage is shorter than the time constant of RESET circuit. The resultant will be loss of noise sound.



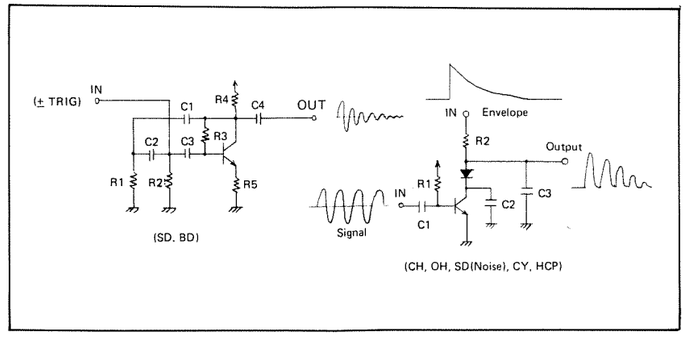
CY SOUND GENERATOR

Four generators oscillate at different frequencies which are determined based on analyses of live symbal sounds. Interrelations between frequencies are so critical that slight deviation of one frequency can cause beat sound or distortion. To let the generators stay in a specific frequency, C1, C4, C12 and C13 should be less than 5%(J) of tolerance.



VOICE GENERATORS

The voice generators are categorized into two groups: Damping oscillator for drum sound and a combination of Swing type VCA and Envelope generator for metalic sounds.



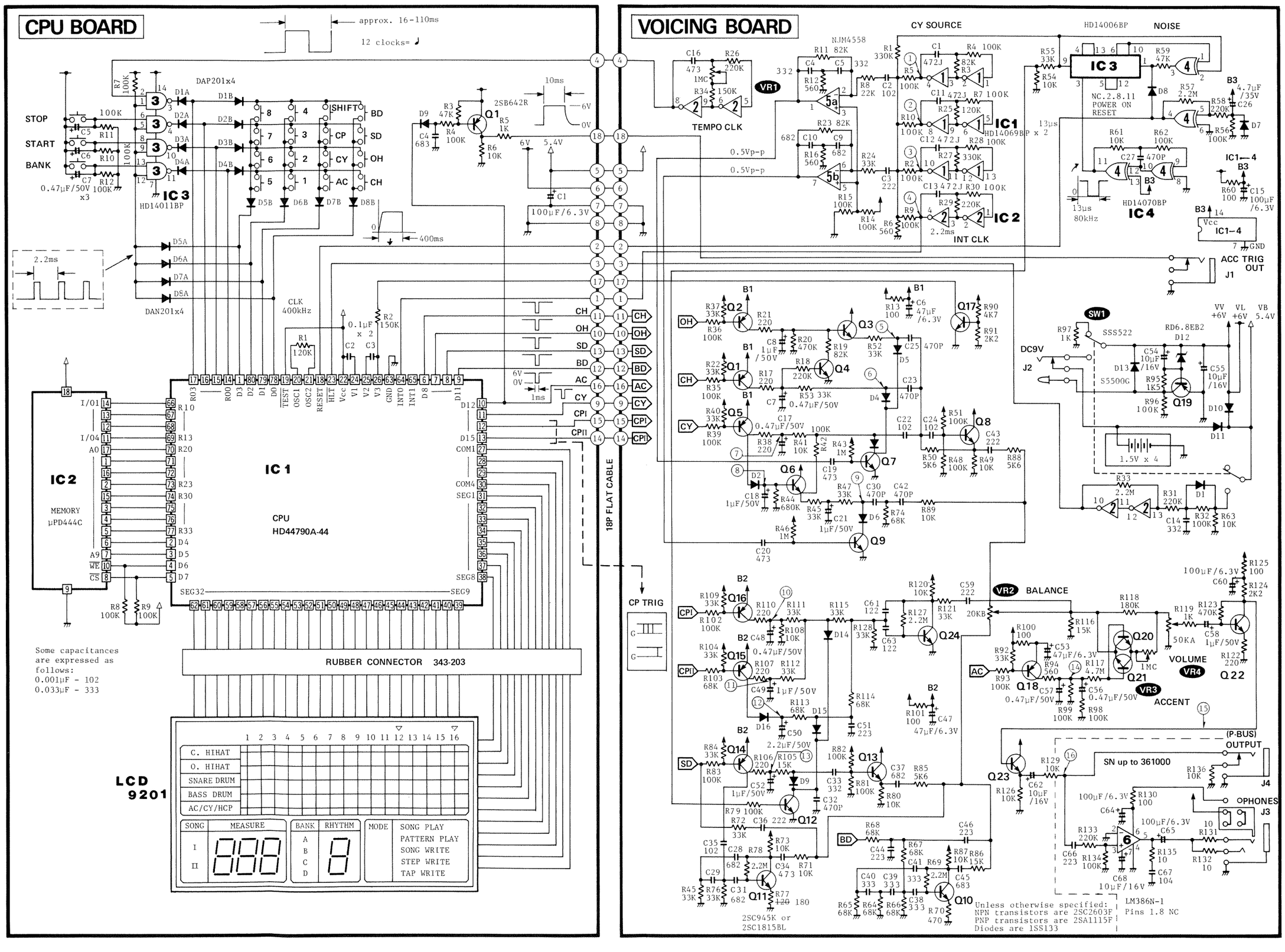
TEST PROGRAM

The CPU is equipped with TEST program for checking LCD and Switch Reading functions.
To enter the test program, press and hold START and STOP buttons and turn the power switch ON.

LCD CHECK - All readouts will be displayed in slightly dull black - because LCD drivers are being overloaded.
Check for lack of segment against the illustration and table in LCD section of the Circuit Description.

SWITCH READING - Press all key switches one by one in any order. Letters "OK" will appear upon pressing the last key, indicating all the keys pressed have been read by the CPU.

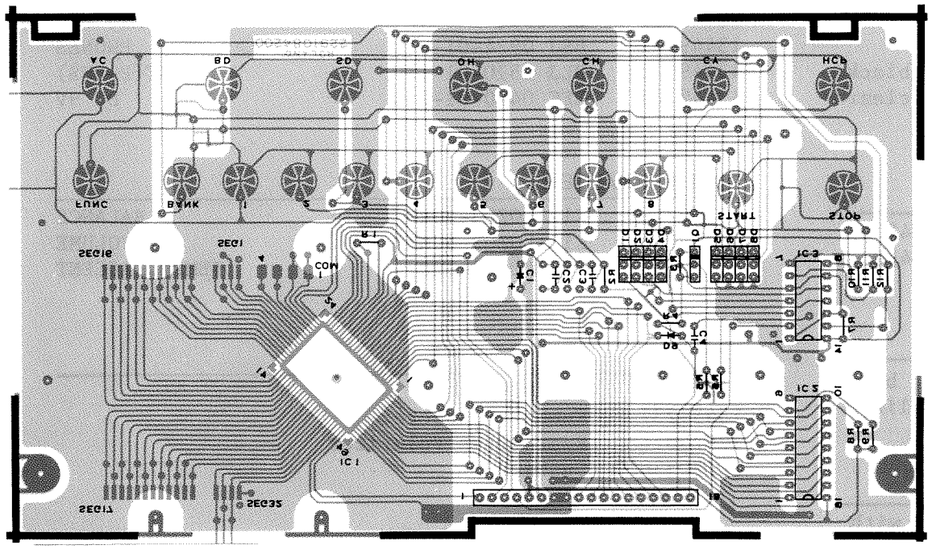
DR 110 CIRCUIT DIAGRAM



CPU BOARD

7313203000
(pcb 2291084200)

View from foil side



CHANGE INFORMATION (VOICING BOARD)

* Q11: from 2SC2603F to 2SC945K, 2SC1815BL or 2SC2603G
* R77: from 120 to 180ohms.

Reason — Shortening SD decay time.

*IC5 : from TL022CP to NJM4558DD

Reason — TL022CP would cause the filter to oscillate

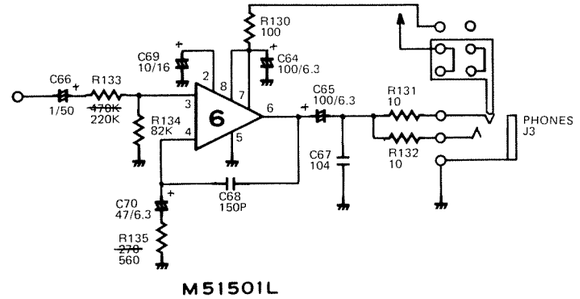
*D13 : from 1SS133 to S5500G (higher forward current type)

Reason — Plugging a high voltage/current AC adaptor of reverse polarity may destroy 1SS133.

*IC6 : from LM386N-1 to M51501L (incompatible) with PCB relaid out.

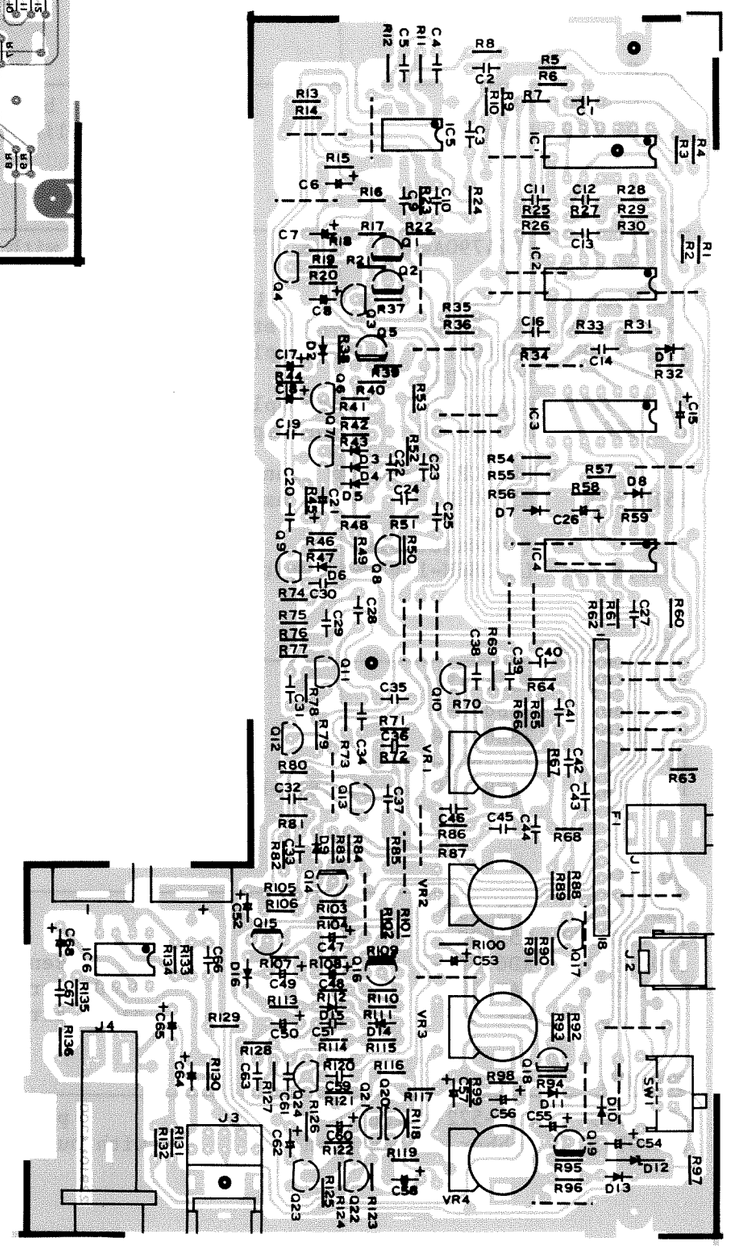
Reason — IC procurement problem.

SN 371100-up

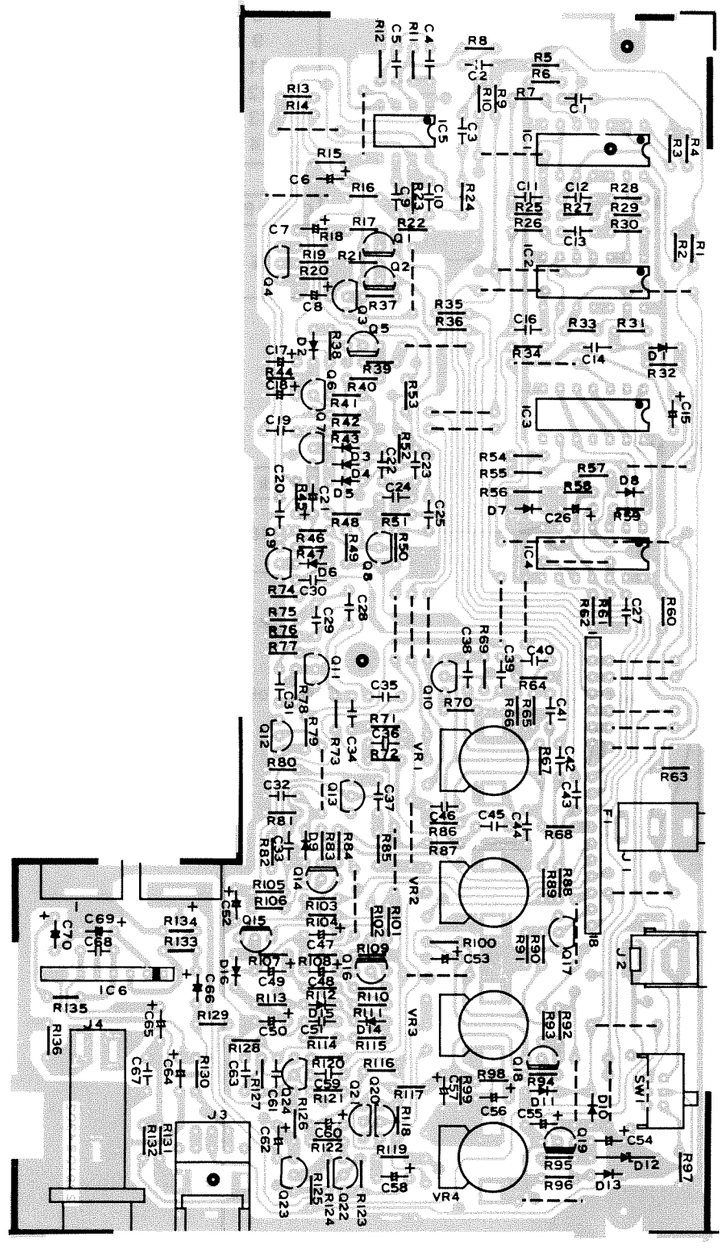


VOICING BOARD

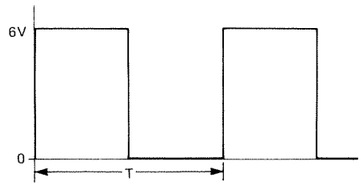
7313204006
(pcb 2291084300)
SN up to 361000



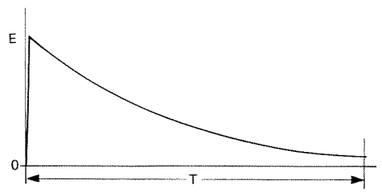
7313204009
(pcb 2291084302)
SN 371100-up



WAVEFORMS

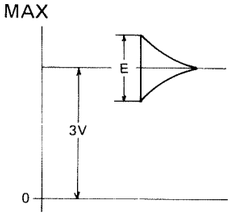


Check Point	T
1	0.87ms
2	1.22ms
3	3.15ms
4	2.15ms



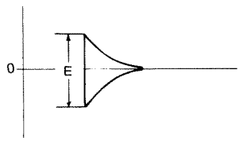
Check Point	T	E
5	700ms	6V
6	80ms	6V
7	60ms	6V
8	900ms	6V
9	1.4s	2.7V
11	140ms	5V
12	700ms	5V
13	100ms	5.7V
14	120ms	5.7V

VOL. MAX



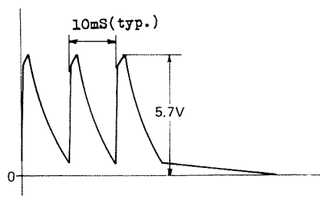
Check Point	ACCENT	E
15	MIN	1.5V
	MAX	4.5V

VOL. MAX



Check Point	ACCENT	E
16	MIN	0.8V
	MAX	1.9V

CP1



Check Point 10

Roland®

17059194

UPC 17059194

PARTS LIST

CASE

2201062900	Top Case	
2201063000	Bottom Case	
2202066600	Display Window Cover	black
2202066500	Display Window Cover	clear
2202066400	Battery Cover	

PCB

7313203000	CPU Board	(pcb 2291084200)
7313204009	Voicing Board	(pcb 2291084302)

KNOB

2247029600	Slide	blue
2247028800	Rotary	black(orange line)

IC

15179122	HD44790A44P	2K x 4bit CMOS CPU with LCD driver
15179305	μPD444C	1K x 4bit static RAM
15159140HO	HD14006BP	18-bit static shift register
15159104HO	HD14011BP	quadruple 2-input NAND gate
15159116TO	TC4069UBP	hex inverter
15159117HO	HD14070BP	quadruple exclusive-OR gate
15189102	NJM4558DD	OP amp(pcb 2291084302-UP)
	or	
	(TL022CP...use NJM brand as a replacement.)	
15199521	M51501L	power amp(pcb 2291084302-UP)
	or	
	(incompatible)	
15199517	LM-386N-1	power amp(pcb up to 2291084300)

TRANSISTOR

15119125	2SA1115-F
15119602	2SB647-C
15119607	2SB642-R
15129137	2SC2603-F
15129145	2SC945-K (or 2SC1815-BL)

DIODE

15019125	1SS-133	
15019209TO	S5500G	
15019530	RD6.8EB-2	zener
15019138	DAN 201	diode array
15019139	DAP 201	diode array

SWITCH

13159329	SSS-522(slide)	power
12479715	Rubber switch(push)	with button

JACK

13449401	SG-8026	ACC TRIG OUT
13449411	HSJ 0924-01-040	PHONES
13449125	HLJ 0520-01-110	OUTPUT(P-BUS)
13449706	HEC 0470-01-230	DC 9V

POTENTIOMETER

13279716	K121LOZ03-20KB	BALANCE
13279717	K121LOZ03-50KA	VOLUME
13279718	K121LOZ03-1MC	TEMPO, ACCENT

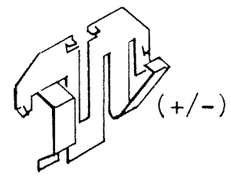
LCD

15029411	LCD 9201
13439237	Rubber Connector
12029826	Rear Glass Polarizer
2226033600	Cushion

OTHERS

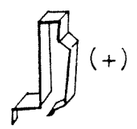
2225021700	Shield Cover
2345014200	Battery clip (+/-) ——————①
2345014300	Battery clip (+) ——————②
2345014400	Battery clip (-) ——————③
2343099100	Flat Cable 18P, 45mm

① (+/-)



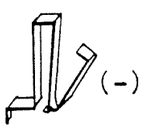
2345014200

② (+)



2345014300

③ (-)



2345014400