SERVICE MANUAL & PARTS LIST (without price)

CZ-5000

DIGITAL SYNTHESIZER

JUNE 1985

CZ-5000

CASIO®

CAUTION:

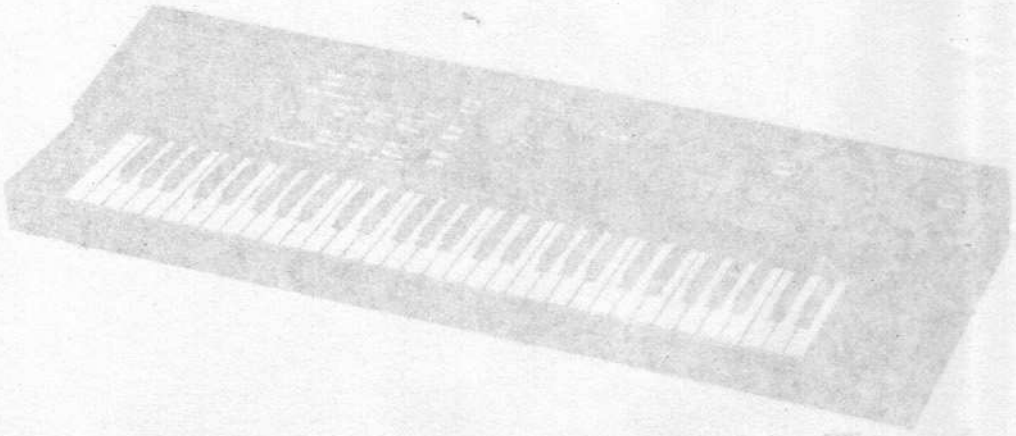
When the connector ○ (from the batteries) is disconnected, all the sound data in the Memory Bank are cleared. When this happens, initialize the unit by the following procedures.

1. **Turn the power switch off and press INITIALIZE button.**
2. **Turn the power switch on, then the display indicates;**

```
 SYSTEM  ALL
INITIALIZE(Y/N)?
```

3. **While pushing INITIALIZE button, press YES button on the data entry section of the panel. All the Memory Bank data are initialized, then the display shows:**

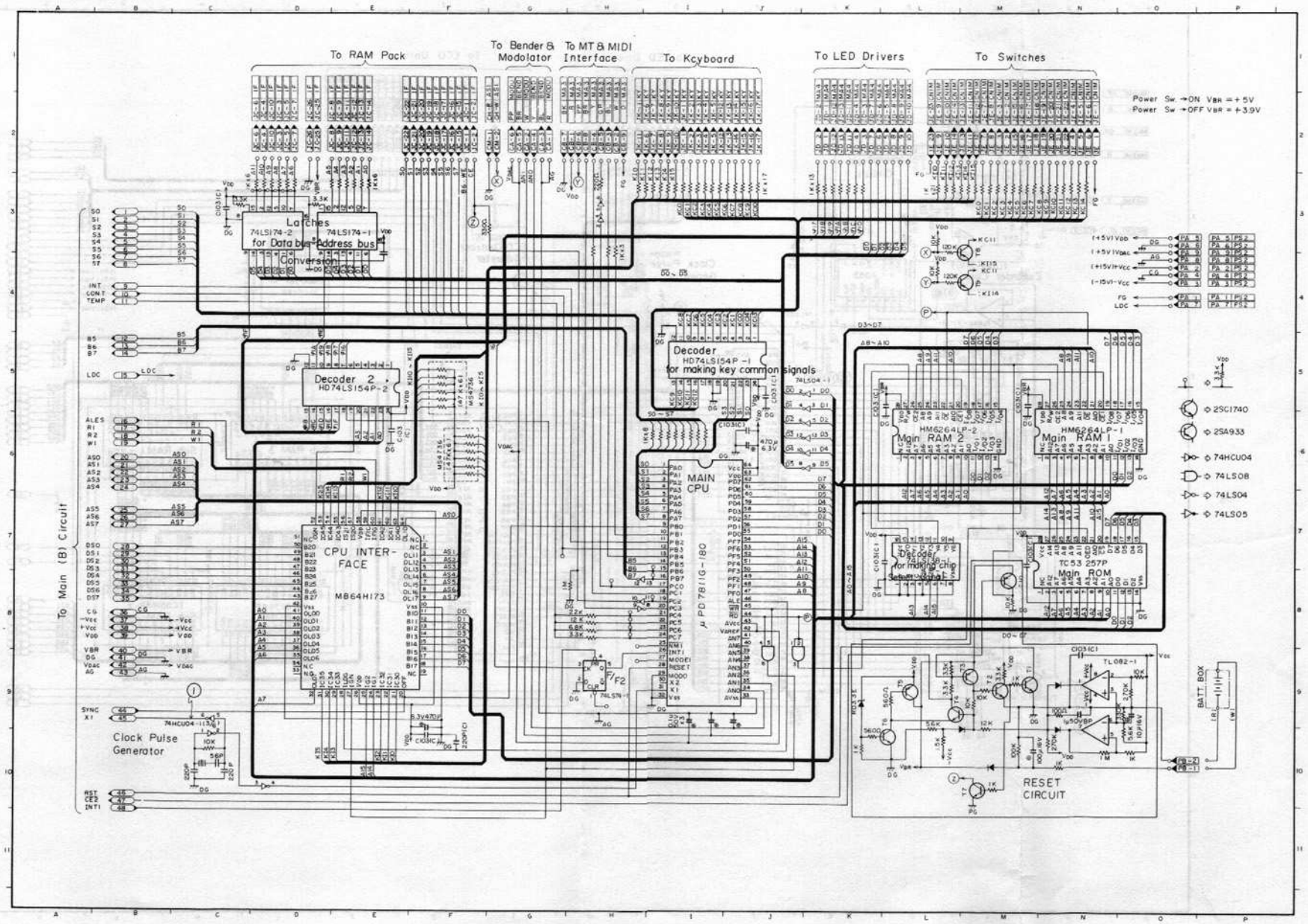
```
 SYSTEM
INITIALIZED  !!
```



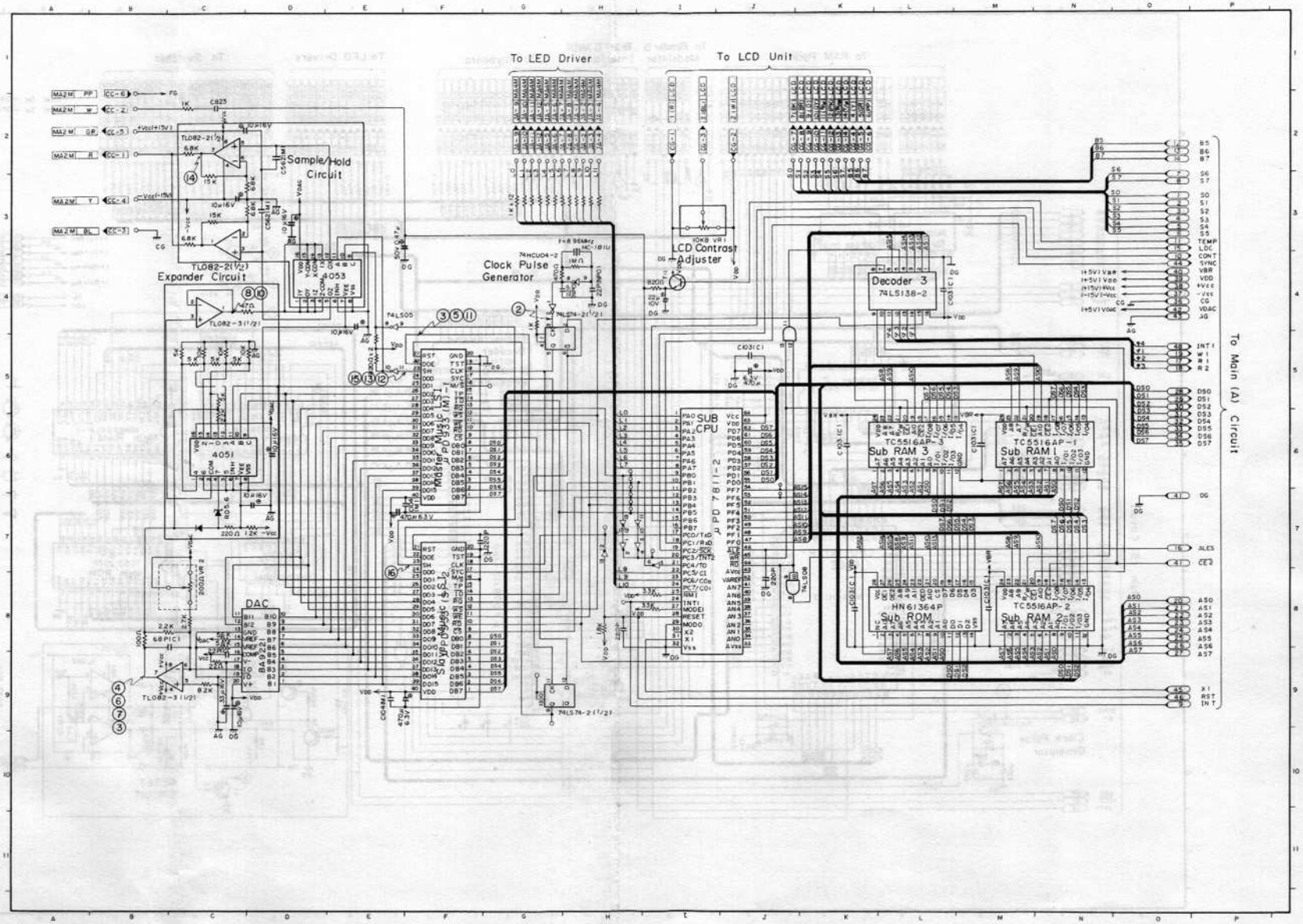
CONTENTS

1. SCHEMATIC DIAGRAM

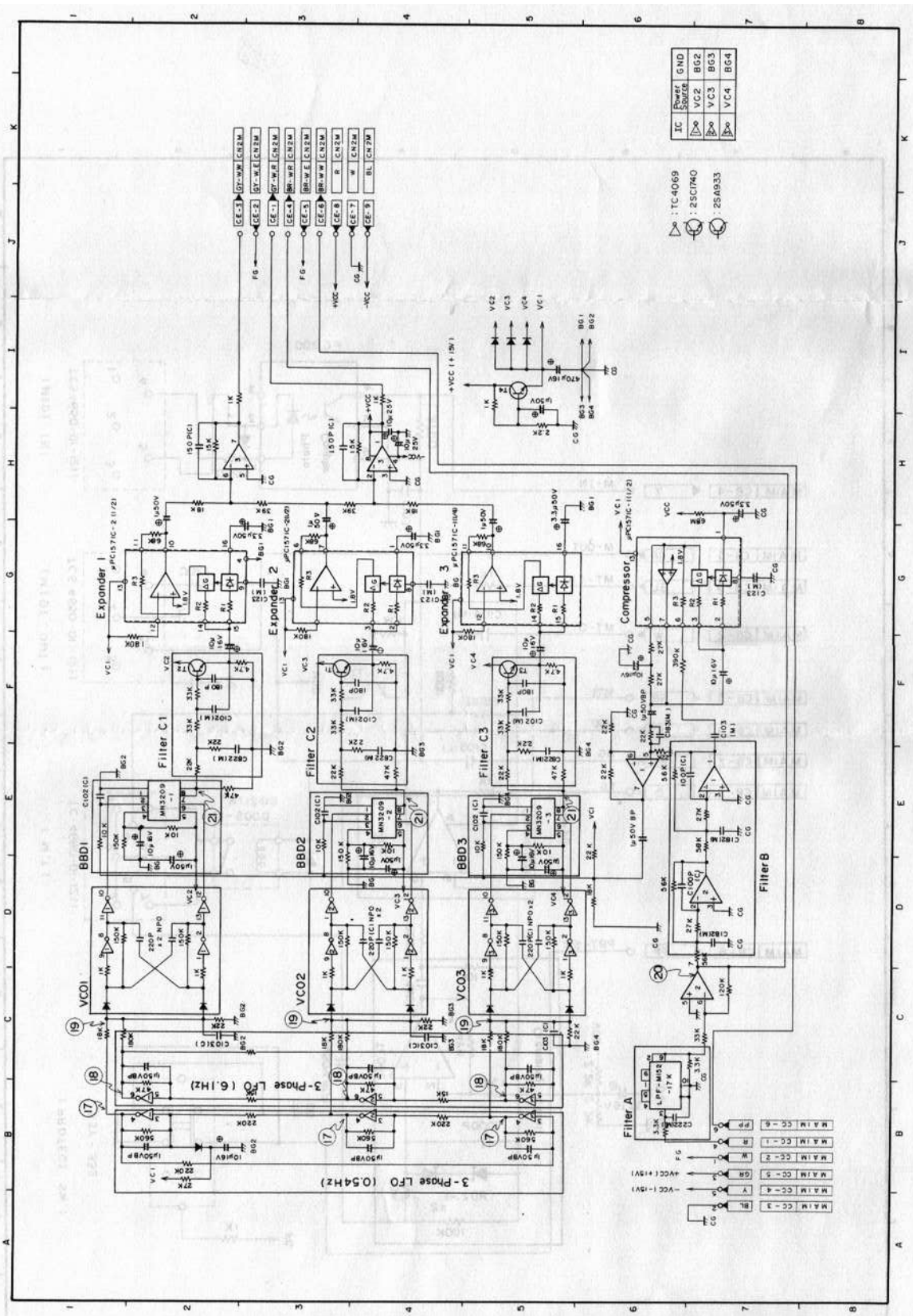
1-1. Main PCB (A) M5153-MA1M

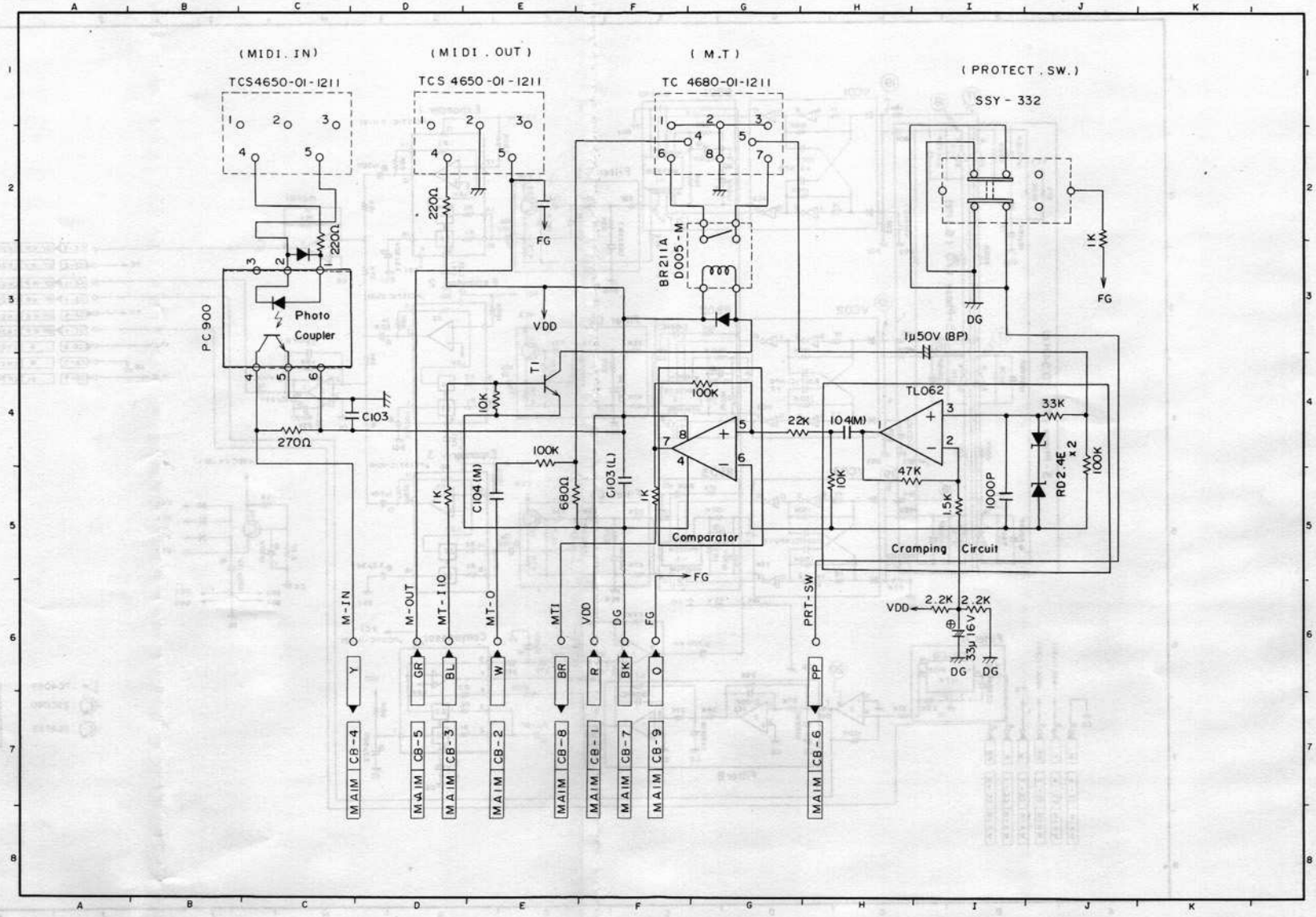


1-2. Main PCB (B) M5153-MA1M

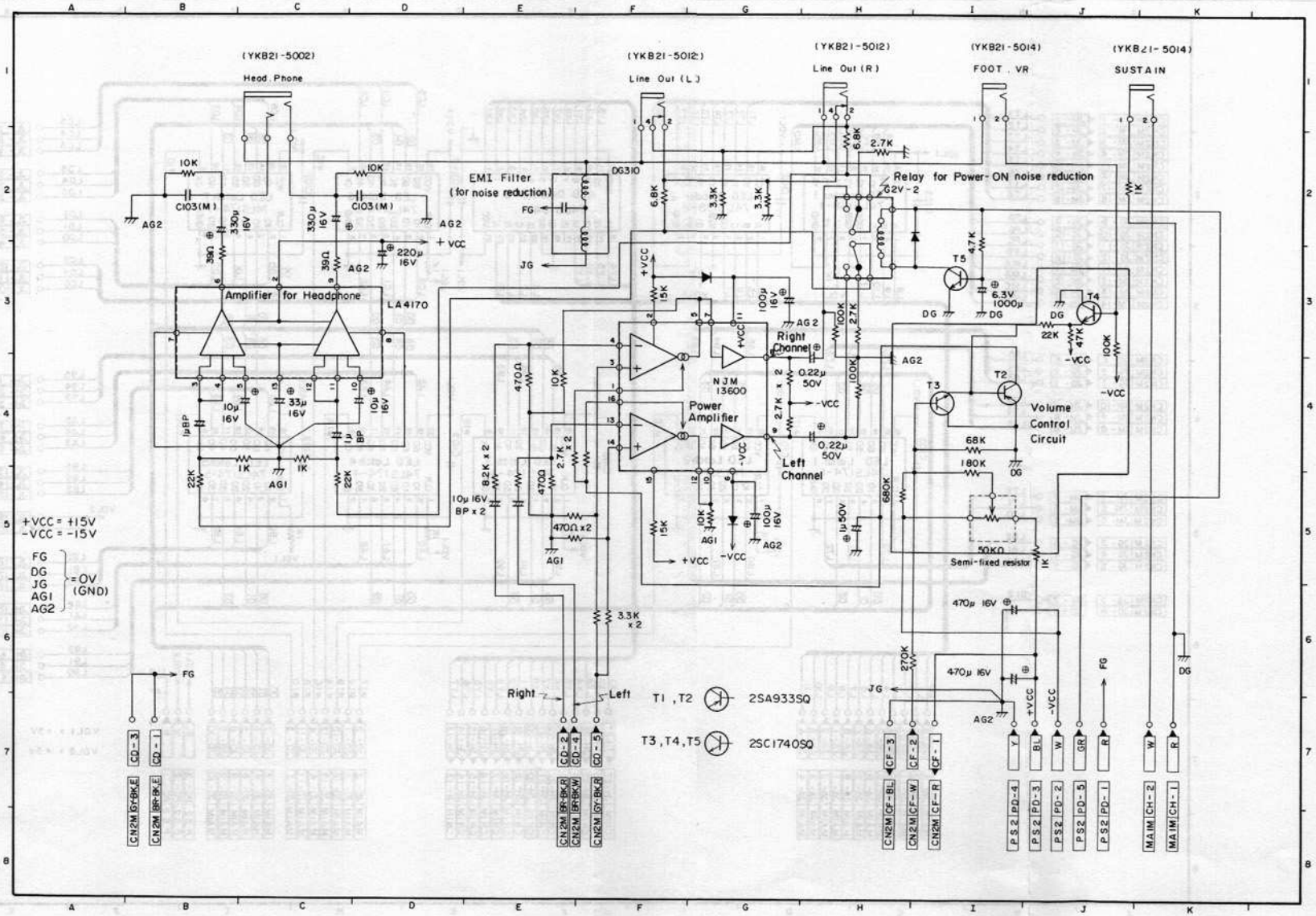


1-3. Stereo Chorus Circuit PCB M5153-MA2M

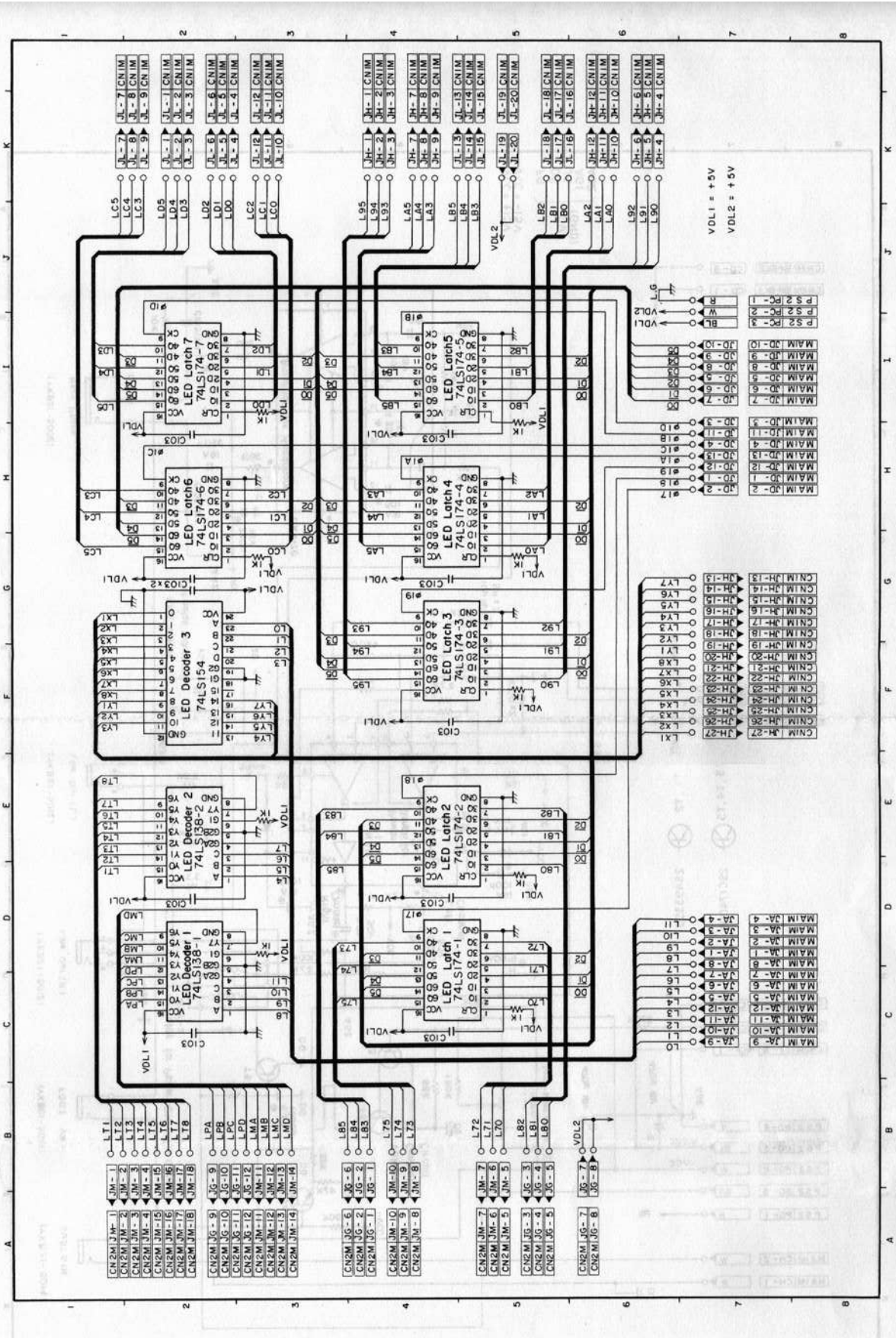



(MIDI. IN)
TCS4650-01-1211
(MIDI. OUT)
TCS 4650-01-1211
(M.T)
TC 4680-01-1211
(PROTECT. SW.)
SSY - 332
PC900
Photo Coupler
220Ω
270Ω
C103
FG
VDD
T1
10K
100K
680Ω
C104(M)
C103(L)
1K
BR211A
D005-M
1µ50V (BP)
TL062
22K
104(M)
33K
47K
10K
1.5K
1000P
RD2.4E x2
100K
Comparator
Cramping Circuit
2.2K
33µ 16V
DG
M-IN
M-OUT
MT-110
MT-0
MTI
PRT-SW
Y
GR
BL
W
BR
R
BK
O
PP
MAIM CB-4
MAIM CB-5
MAIM CB-3
MAIM CB-2
MAIM CB-8
MAIM CB-1
MAIM CB-7
MAIM CB-9
MAIM CB-6

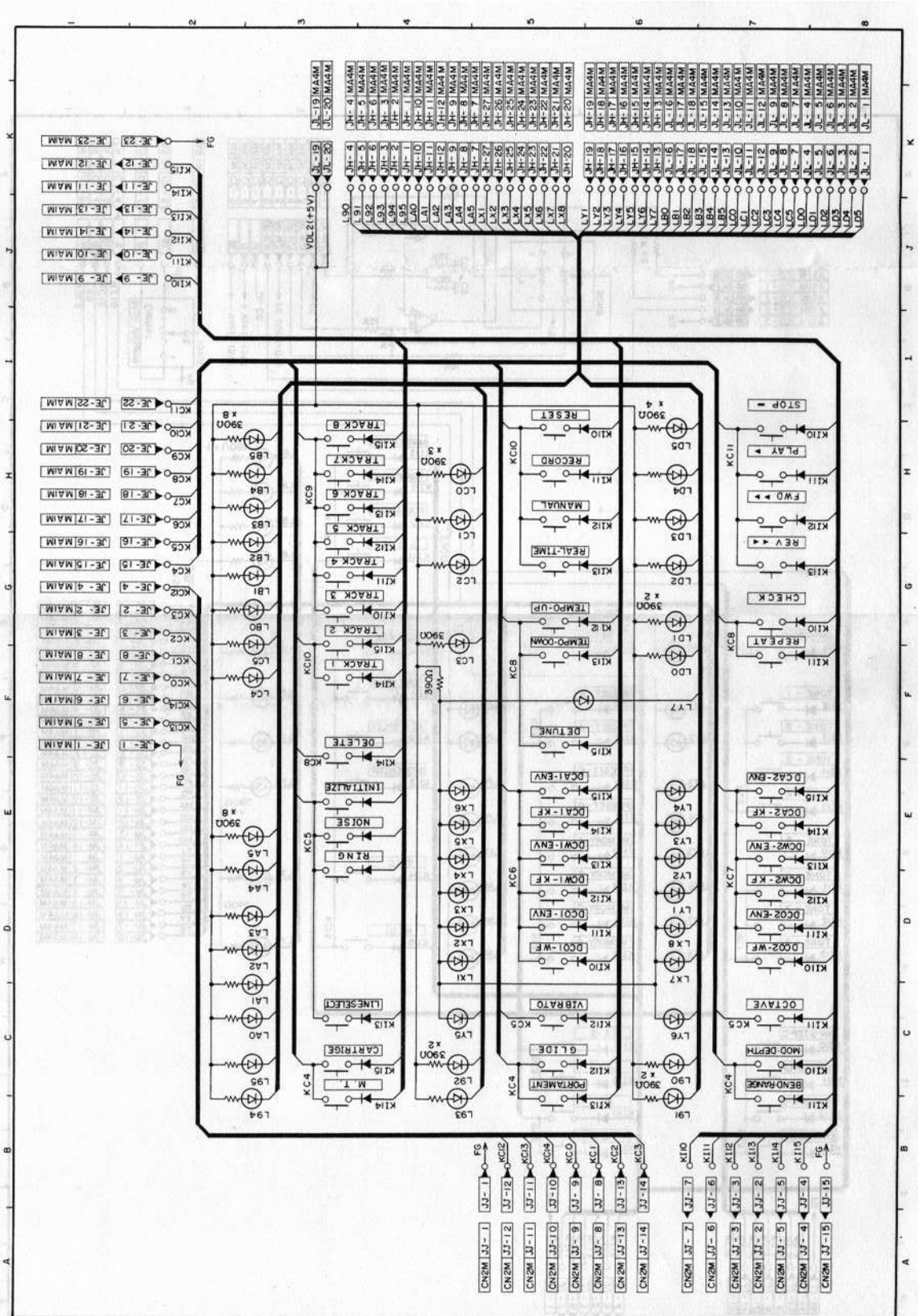
1-5. Amp. Block PCB M5153-AS1M



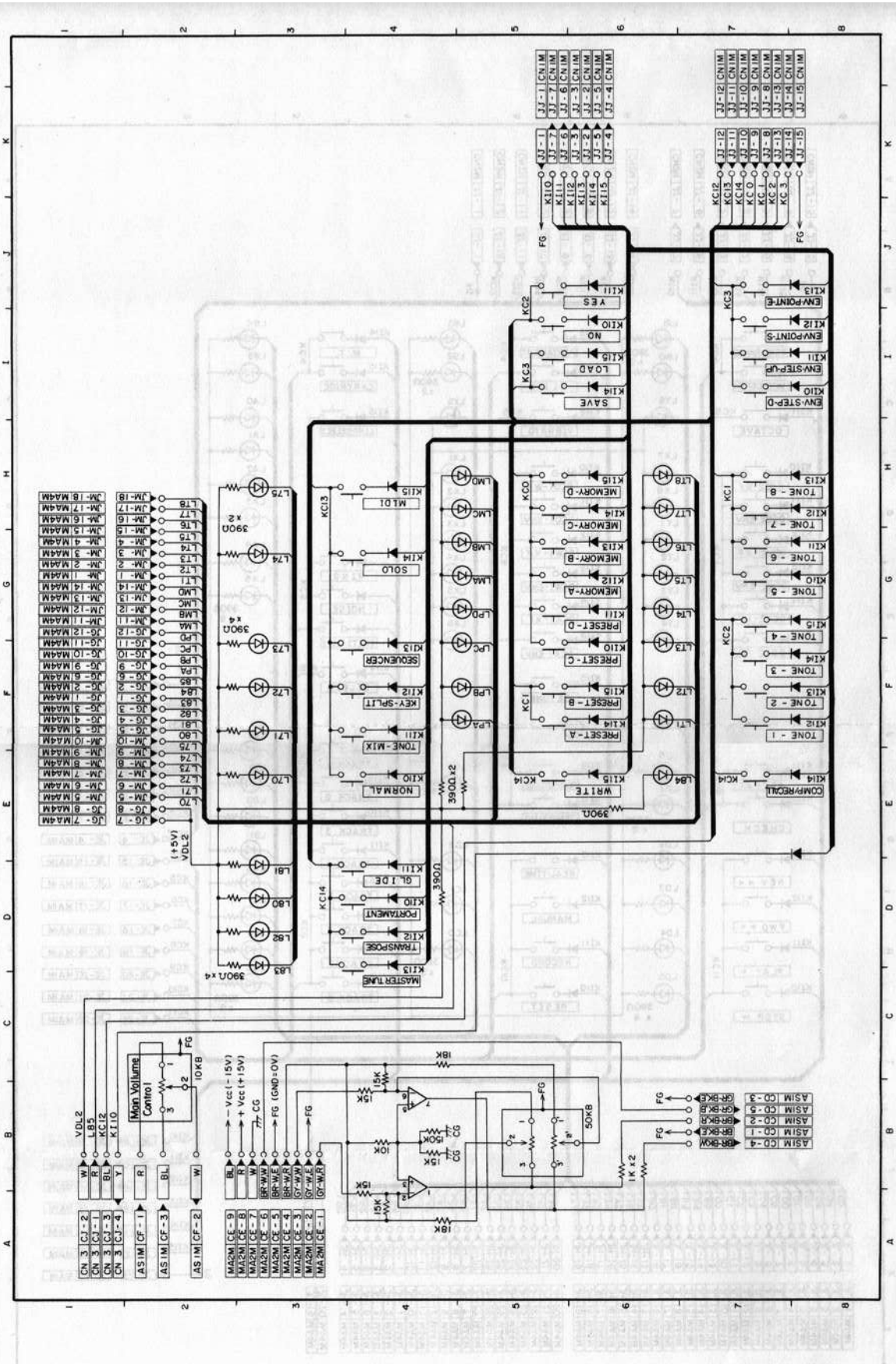
1-6. LED Drive Circuit PCB M5153-MA4M



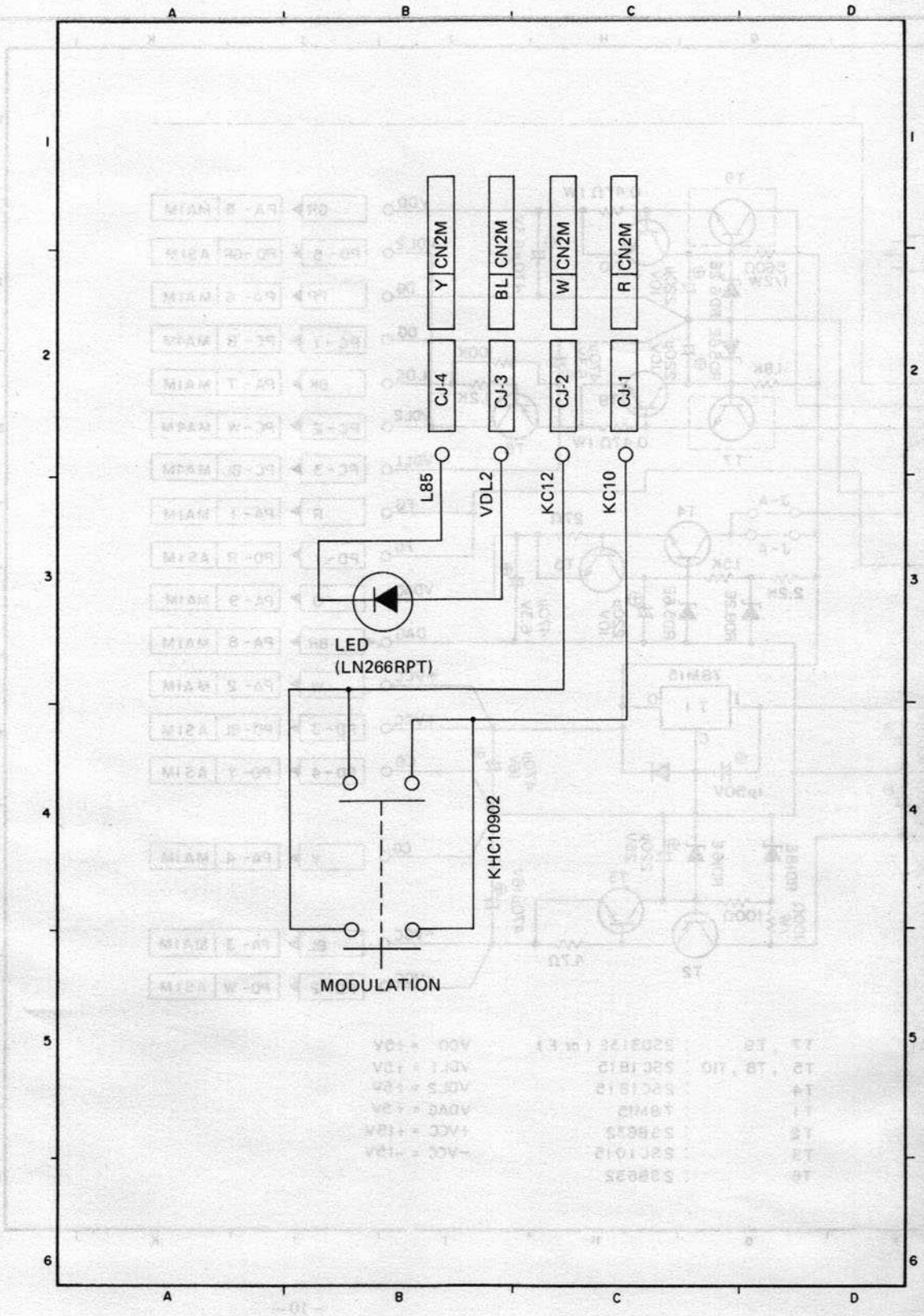
1-7. Panel Block (A) PCB M5153-CN1M

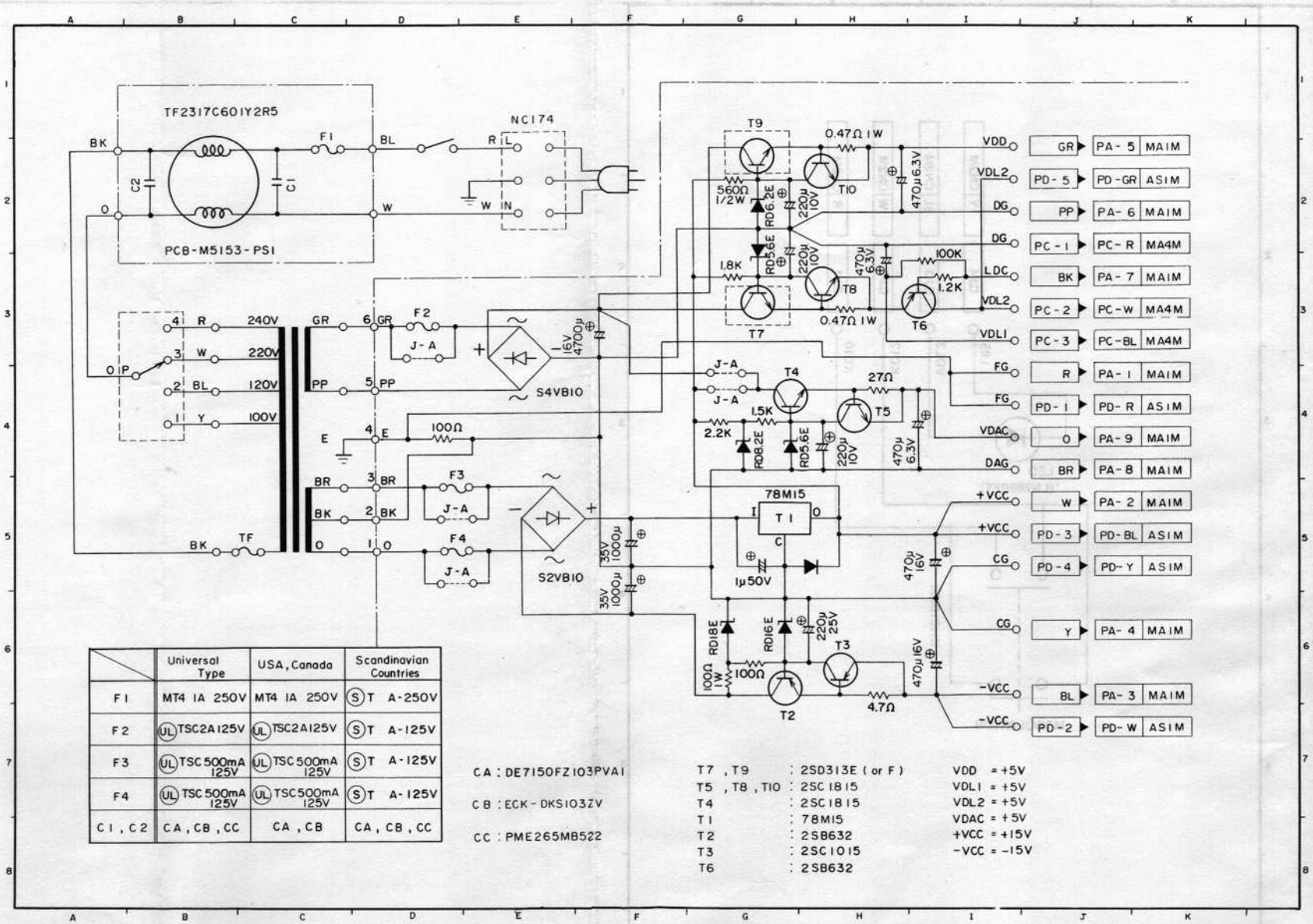


1-8. Panel Block (B) PCB M5153-CN2M



1-9. Modulation Switch PCB M5153-CN3





	Universal Type	USA, Canada	Scandinavian Countries
F1	MT4 1A 250V	MT4 1A 250V	(S) T A-250V
F2	(UL) TSC2A125V	(UL) TSC2A125V	(S) T A-125V
F3	(UL) TSC 500mA 125V	(UL) TSC 500mA 125V	(S) T A-125V
F4	(UL) TSC 500mA 125V	(UL) TSC 500mA 125V	(S) T A-125V
C1, C2	CA, CB, CC	CA, CB	CA, CB, CC

CA : DE7150FZ103PVA1

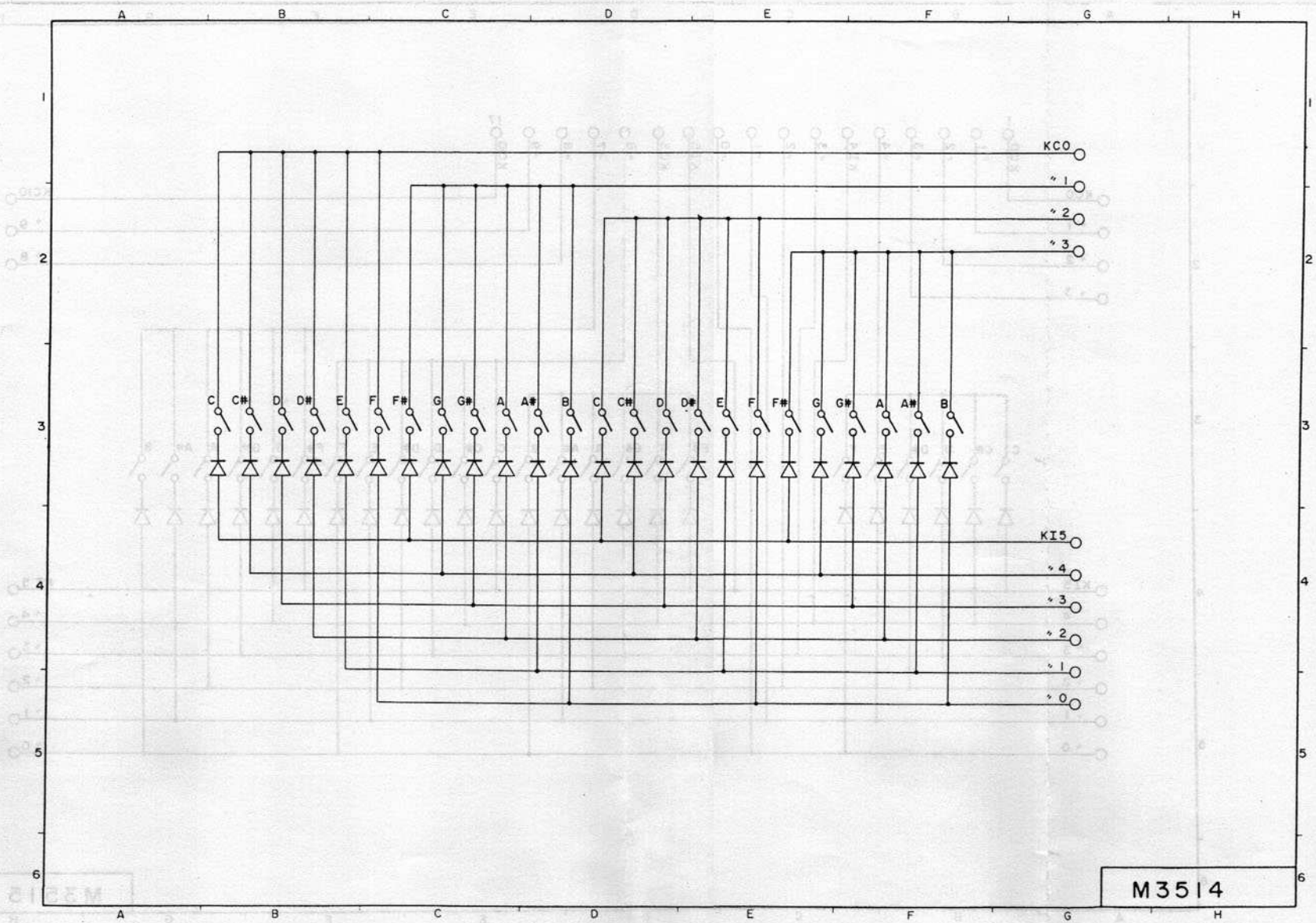
CB : ECK-DKS103ZV

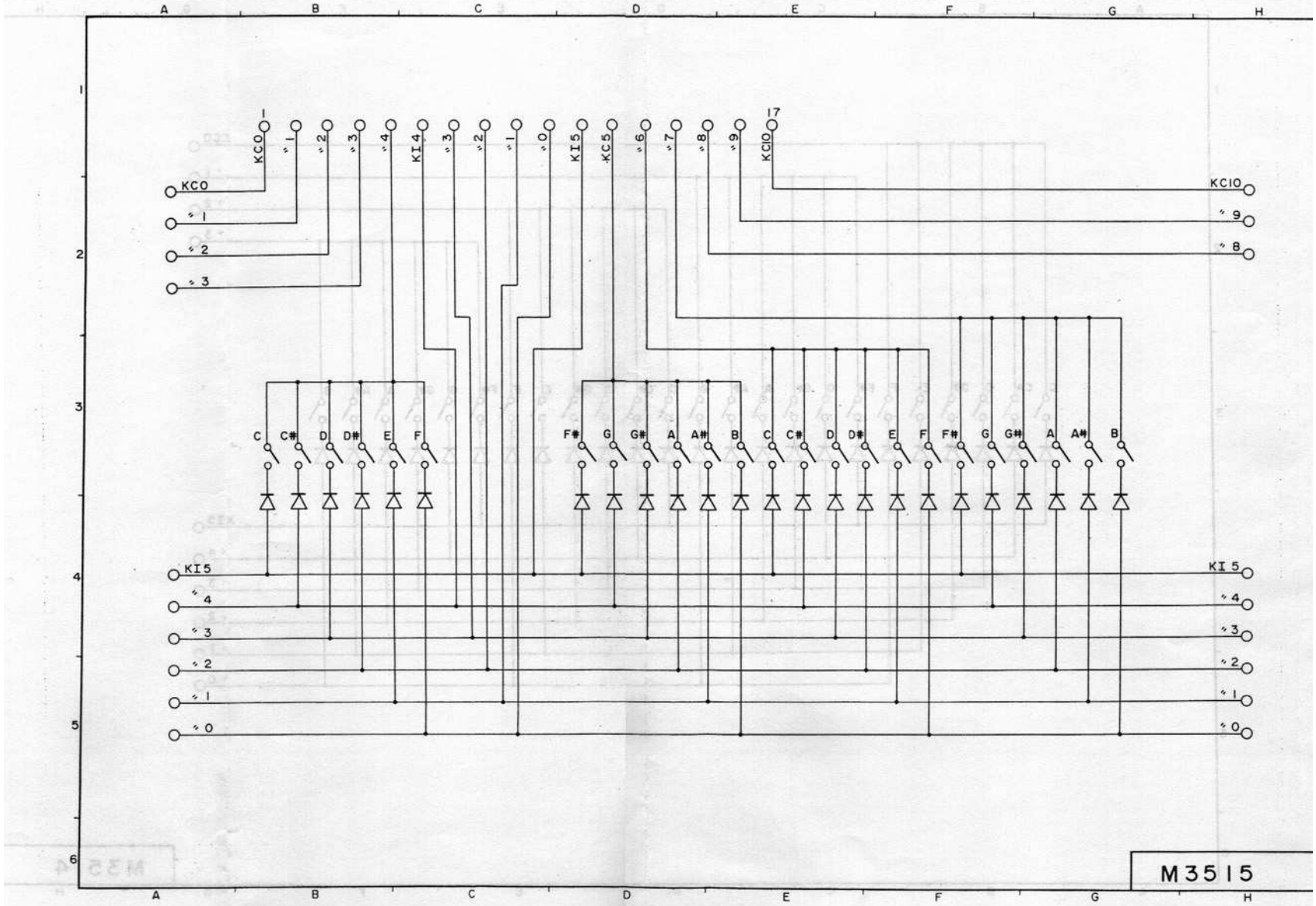
CC : PME265MB522

T7, T9	: 2SD313E (or F)
T5, T8, T10	: 2SC1815
T4	: 2SC1815
T1	: 78M15
T2	: 2SB632
T3	: 2SC1015
T6	: 2SB632

VDD	= +5V
VDL1	= +5V
VDL2	= +5V
VDAC	= +5V
+VCC	= +15V
-VCC	= -15V

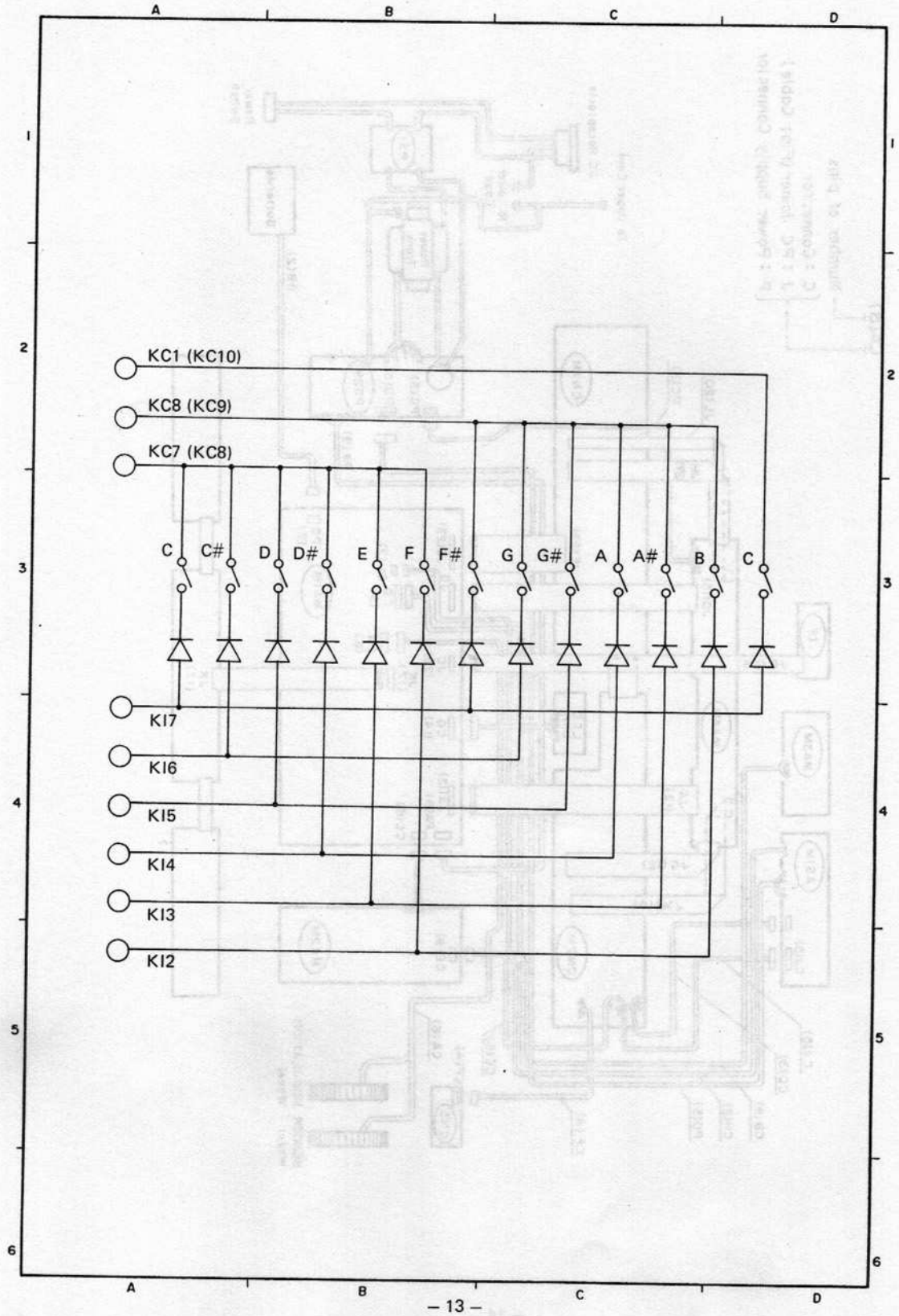
1-11. Keyboard (1) PCB M416-KY1



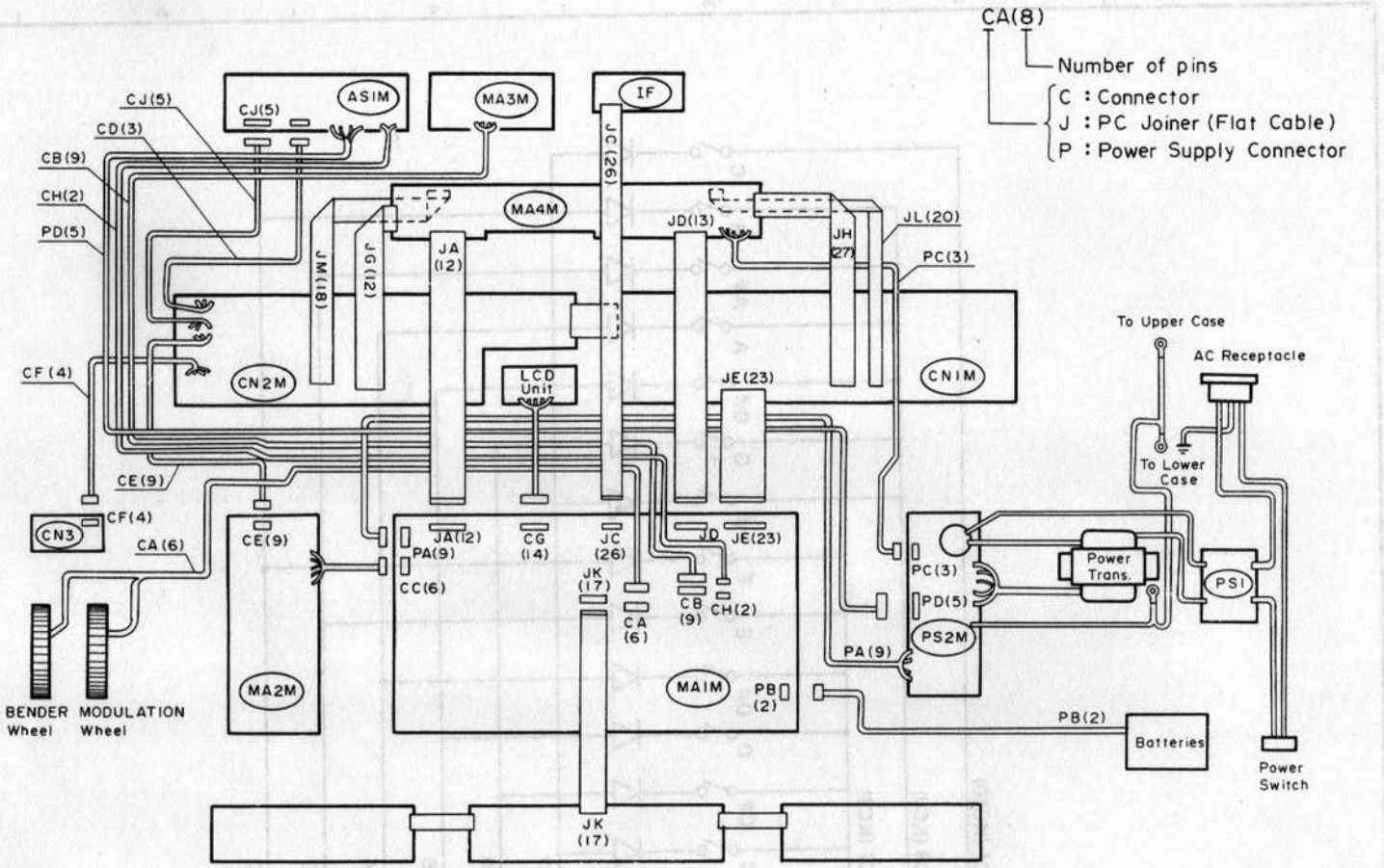

A
B
C
D
E
F
G
H
1
2
3
4
5
6
KC0
KC1
KC2
KC3
KC4
KI4
KI3
KI2
KI1
KI0
KI5
KC5
KC6
KC7
KC8
KC9
KC10
KC0
KC1
KC2
KC3
KC10
KC9
KC8
C
C#
D
D#
E
F
F#
G
G#
A
A#
B
KI5
KI4
KI3
KI2
KI1
KI0

M3515

1-13. Keyboard PCB M425-KY3



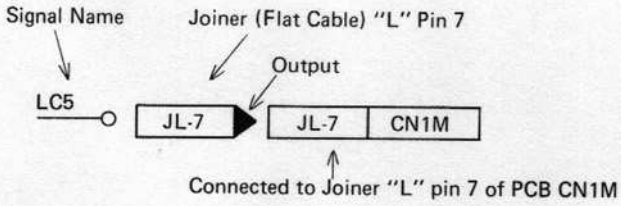
2. WIRING DIAGRAM

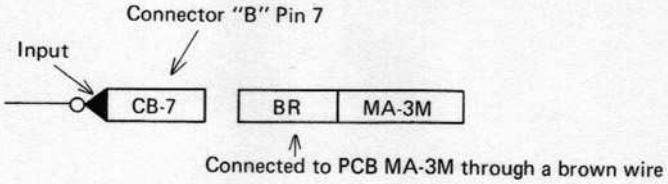


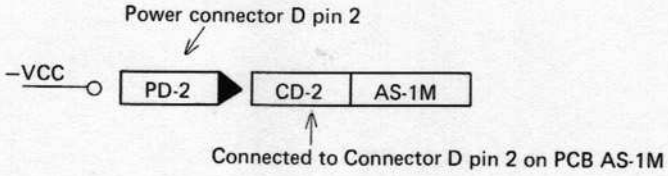
NOTE: **1. Wire Color Codes**

R : Red	W : White	BL: Blue
Y : Yellow	GR: Green	PP : Purple
BK: Black	BR : Brown	O : Orange
GY: Gray	PK : Pink	E : Shielded wire

2. Terminal Readings





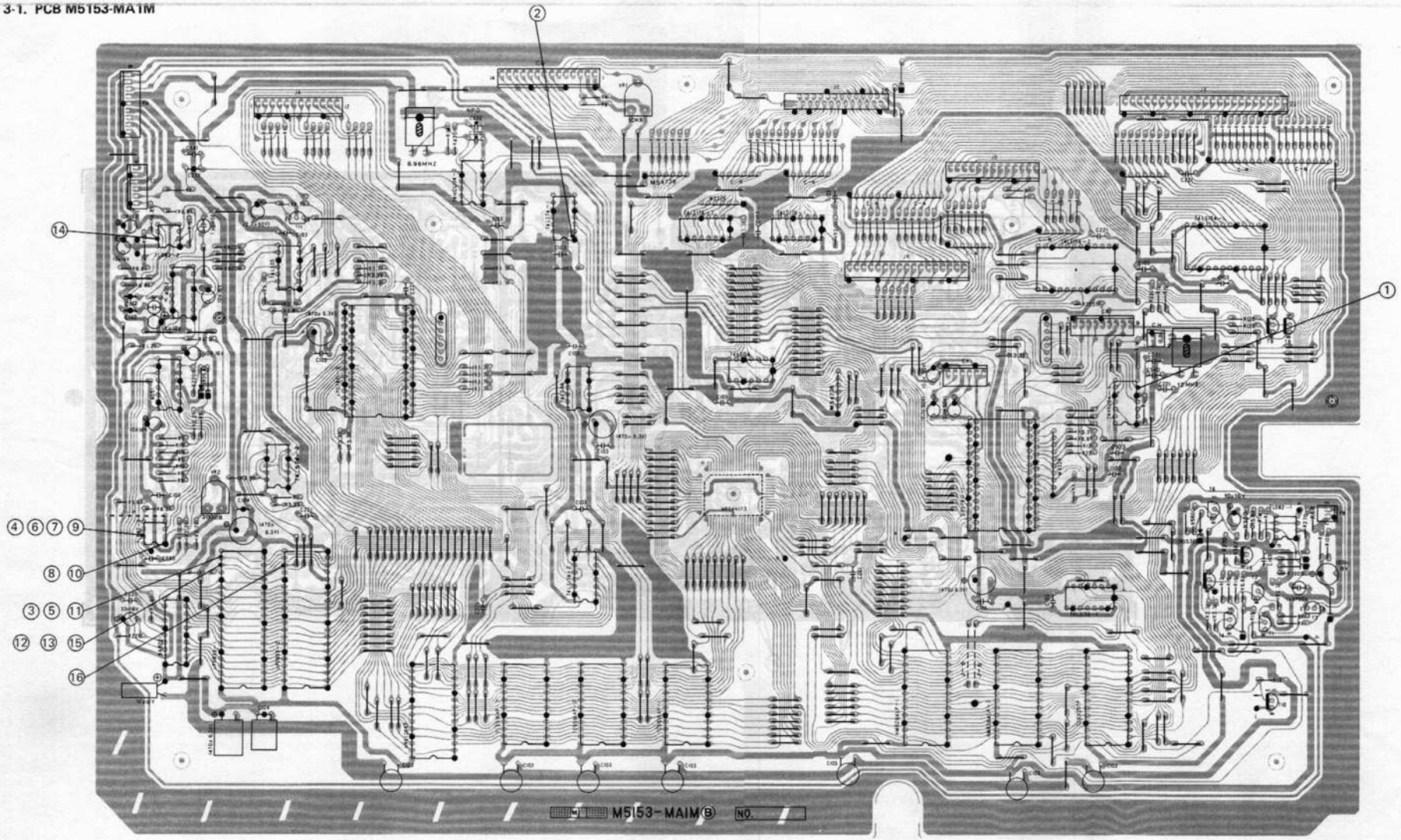


3. Voltage Levels

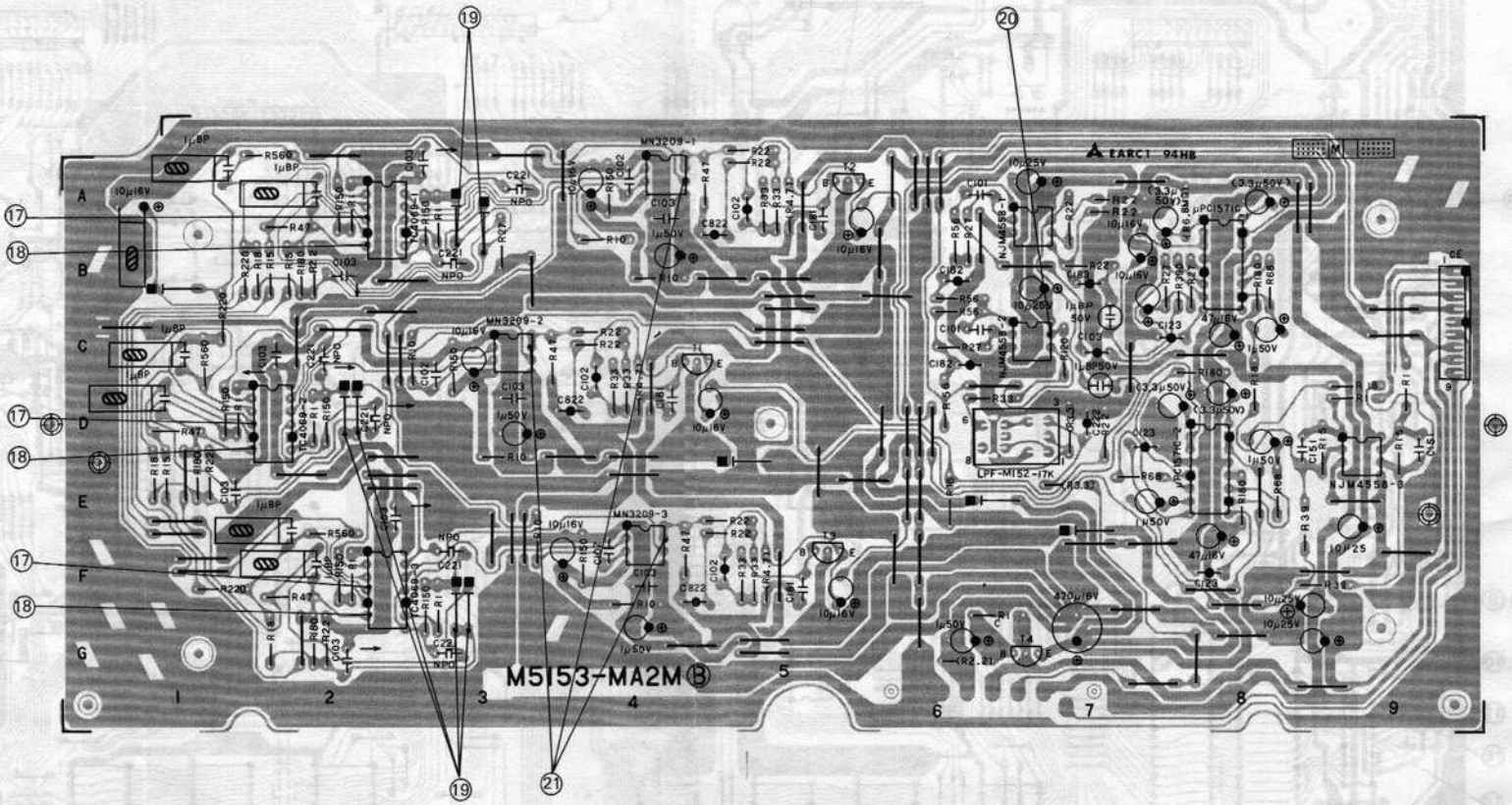
VDD	+5V	For digital circuits
VDL1	+5V	For LED driving
VDL2	+5V	For LED driving (rises to +5V approximately 830 milliseconds after Power ON)
VDAC	+5V	For DAC (Digital to Analog Converter)
+VCC	+15V	For analog circuits
-VCC	-15V	For analog circuits
DG	0V	Digital ground
FG	0V	Frame ground
DAG	0V	DAC ground
CG	0V	Analog ground
VBR	+5V at Power ON +3.9V at Power OFF	RAMs' backup voltage

3. PCB VIEW & MAJOR CHECKPOINT

3-1. PCB M5153-MA1M

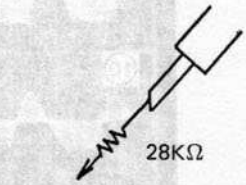


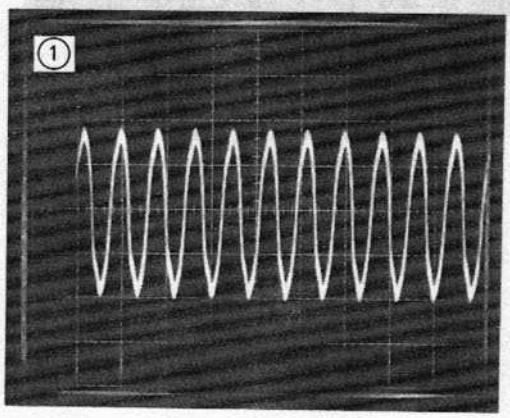
3-2. PCB M5153-MA2M



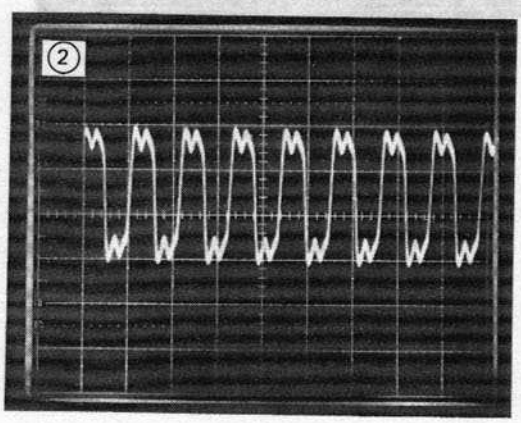
4. MAJOR WAVEFORMS

Notes: Photographs marked Ⓜ show stored waveforms in a memory scope.
The analog waveforms were observed via a 28 Kohm resistor.

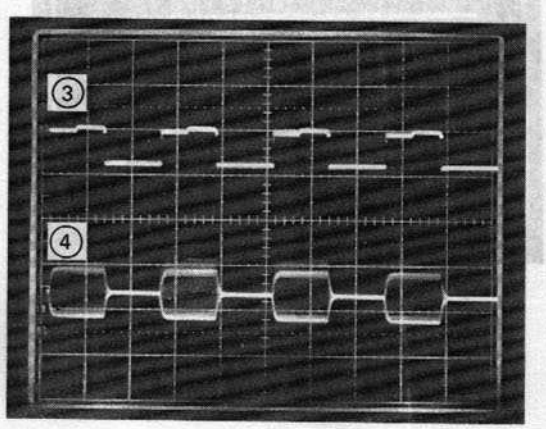




① μPD7811 clock pulse
PCB M5153-MA1M
74HCU04-1 pin 6
0.1μs/div., 2V/div.

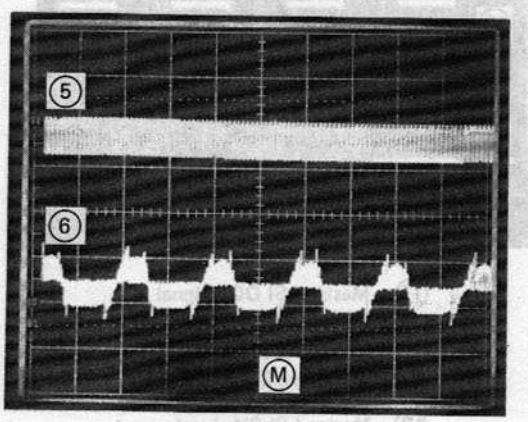


② μPD933 clock pulse
PCB M5153-MA1M
74HCU04-2 pin 2
0.1μs/div., 2V/div.

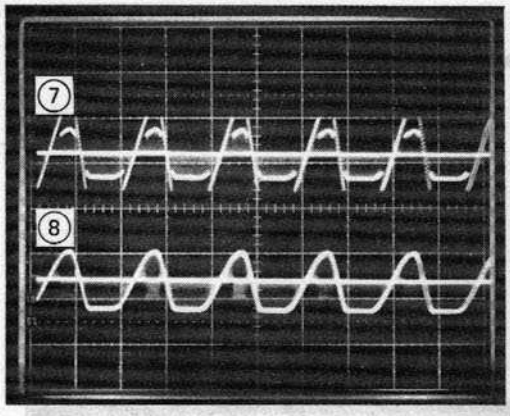


③ DOE
PCB M5153-MA1M
μPD933 pin 22
10μs/div., 5V/div.
Tone: Flute, Key: C4

④ DAC output
PCB M5153-MA1M
TL082-3 pin 7
10μs/div., 5V/div.
Tone: Flute, Key: C4

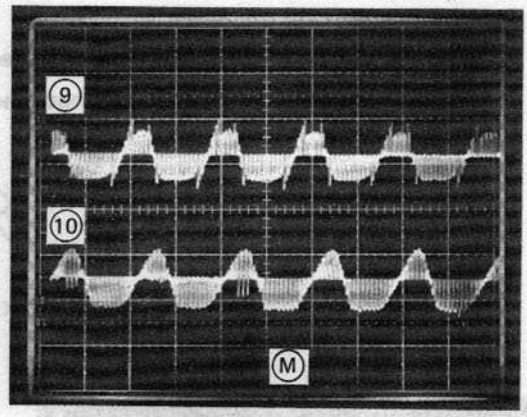


⑤ DOE and ⑥ DAC outputs
Same conditions as ③ and ④ except 2ms/div. of sweep time and using a memory scope.

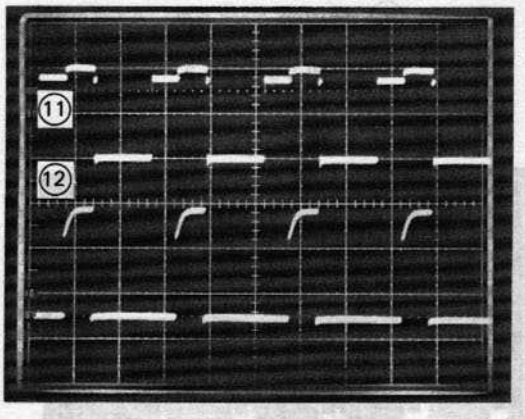


⑦ DAC output
PCB M5153-MA1M
TL082-3 pin 7
2ms/div., 5V/div.
Tone: Flute, Key: C4

⑧ Expander Circuit output
PCB M5153-MA1M
TL082-3 pin 1
2ms/div., 0.5V/div.
Tone: Flute, Key: C4

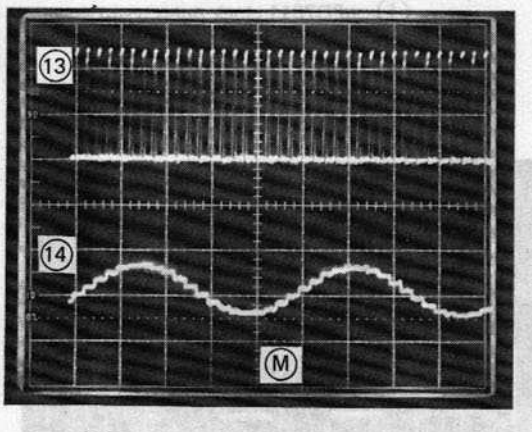


⑨ DAC output and ⑩ Expander Circuit output
Same conditions as ⑦ and ⑧ except using a memory scope.



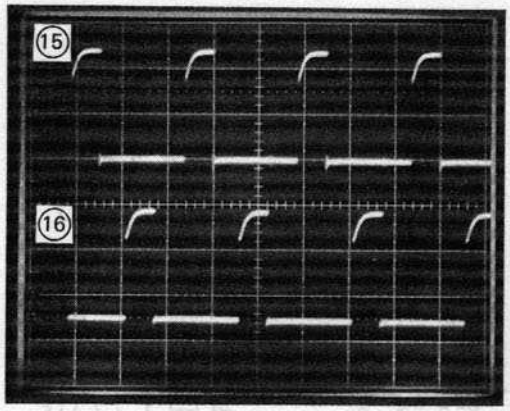
⑪ Master LSI DOE signal
PCB M5153-MA1M
μPD933-1 pin 22
10μs/div., 2V/div.

⑫ Master LSI SH signal
PCB M5153-MA1M
μPD933-2 pin 23
10μs/div., 2V/div.



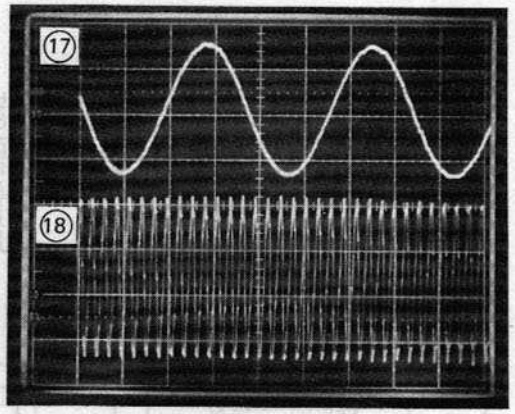
⑬ Master LSI SH signal
PCB M5153-MA1M
μPD933-1 pin 23
0.1μs/div., 2V/div.

⑭ Sample & Hold Circuit output
PCB M5153-MA1M
TL082-2 pin 7
0.1μs/div., 2V/div.
Tone: Flute, Key: C7



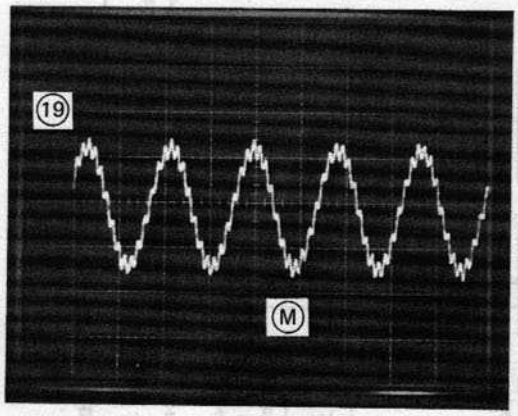
⑮ Master LSI SH signal
PCB M5153-MA1M
μPD933-1 pin 23
10μs/div., 2V/div.

⑯ Slave LSI SH signal
PCB M5153-MA1M
μPD933-2 pin 23
10μs/div., 2V/div.

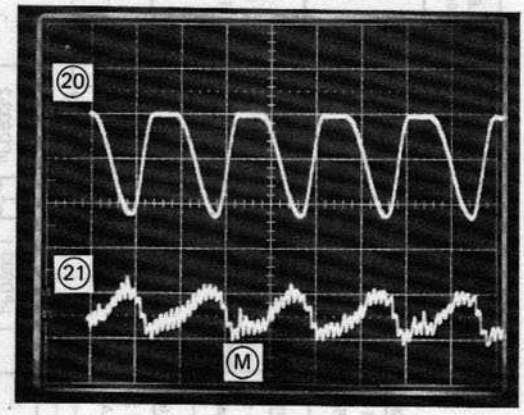


⑰ 0.54Hz LFO output
PCB M5153-MA2M
TC4069-1 pin 4
0.5s/div., 2V/div.

⑱ 6.1Hz LFO output
PCB M5153-MA2M
TC4069-1 pin 6
0.5s/div., 2V/div.



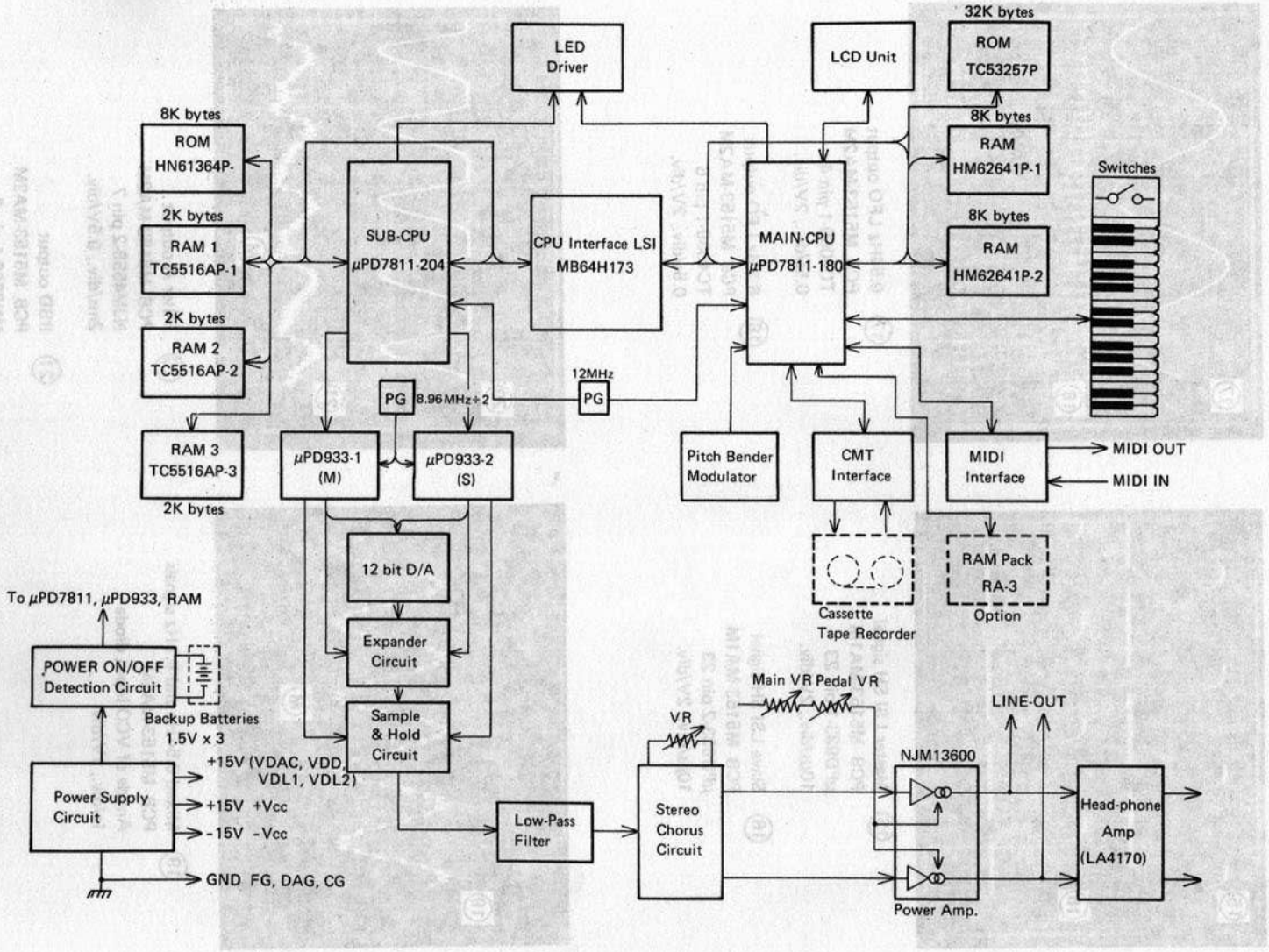
⑲ Mixed 0.54Hz and 6.1Hz signals
PCB M5153-MA2M
Anode of VCO input diode
1s/div., 1V/div.



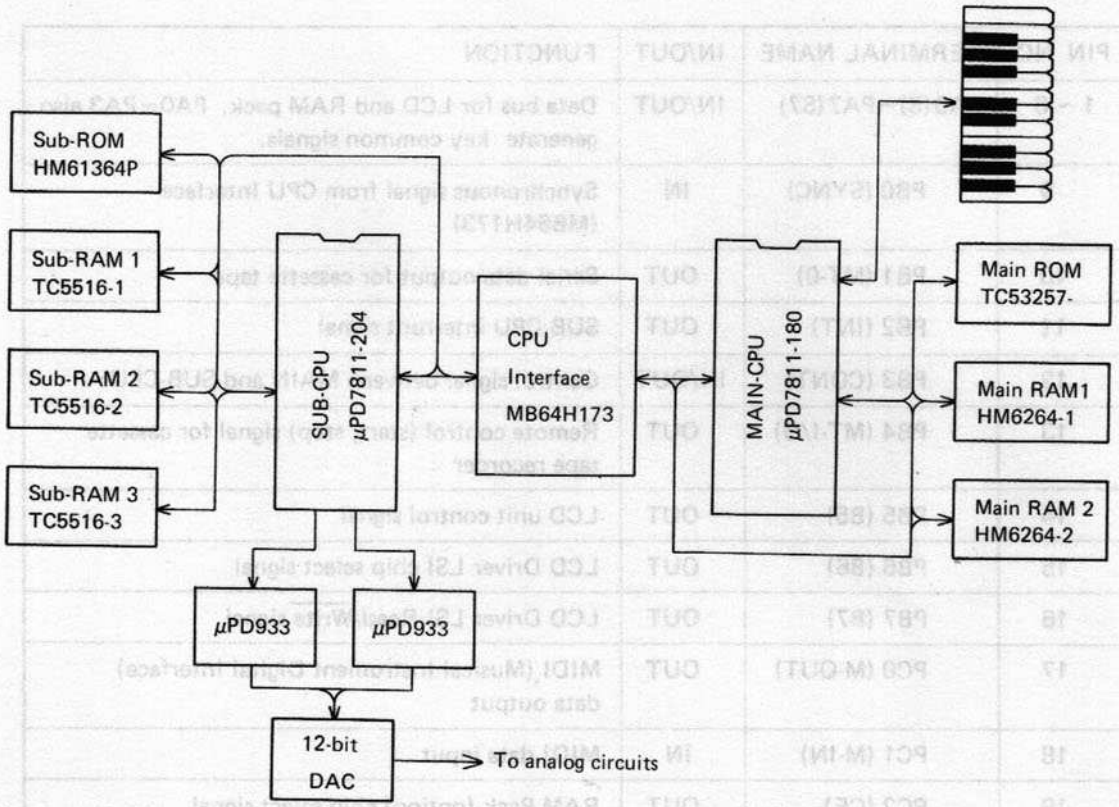
⑳ Filter A output
PCB M5153-MA2M
NJM4558-2 pin 7
2ms/div., 0.5V/div.

㉑ BBD output
PCB M5153-MA2M
MN3209-1 pin 7
2ms/div., 0.5V/div.

5. BLOCK DIAGRAM



6. DIGITAL CIRCUIT BLOCK DIAGRAM



Function of each block:

MAIN CPU	– Controls keys and switches scanning, sequencer, MIDI and cassette tape player.
SUB-CPU	– Mainly controls Music LSIs.
CPU Interface	– Interfaces between MAIN CPU and SUB-CPU.
Main RAM 1	– The first 2K bytes are for system execution and the rest of 6K bytes store the sequencer data.
Main RAM 2	– Stores the sequencer data.
Sub-RAM 1	– Having 2K-byte capacity, stores tone data for Memory Banks A and B.
Sub-RAM 2	– System execution area.
Sub-RAM 3	– Stores data fro Memory Banks C and D.

7. MAIN CPU (μPD7811-180)

PIN NO.	TERMINAL NAME	IN/OUT	FUNCTION
1 ~ 8	PA0(S)~PA7(S7)	IN/OUT	Data bus for LCD and RAM pack. PA0~PA3 also generate key common signals.
9	PB0 (SYNC)	IN	Synchronous signal from CPU Interface (MB64H173)
10	PB1 (MT-0)	OUT	Serial data output for cassette tape
11	PB2 (INT)	OUT	SUB-CPU interrupt signal
12	PB3 (CONT)	IN/OUT	Control signal between MAIN and SUB-CPUs
13	PB4 (MT-I/O)	OUT	Remote control (start, stop) signal for cassette tape recorder
14	PB5 (B5)	OUT	LCD unit control signal
15	PB6 (B6)	OUT	LCD Driver LSI chip select signal
16	PB7 (B7)	OUT	LCD Driver LSI Read/$\overline{\text{Write}}$ signal
17	PC0 (M-OUT)	OUT	MIDI (Musical Instrument Digital Interface) data output
18	PC1 (M-IN)	IN	MIDI data input
19	PC2 (CE)	OUT	RAM Pack (option) chip select signal
20	PC3 (MT-I)	IN	Data input from cassette tape
21 ~ 24	PC4 ~ PC7	OUT	Metronome (timing signal for music recording) pitch signals
26	INT1	IN	Interrupt from SUB-CPU
28	$\overline{\text{RESET}}$	IN	Initializes the LSI's internal circuits at Power ON.
31	X1	IN	12MHz clock pulse
32	VSS	IN	Logic ground (0V) source
33	AVSS	IN	Ground for the built-in ADC (Analog to Digital Converter)
34	AN0	IN	Bender wheel input. A voltage from the bender wheel is converted into digital data by a built-in ADC.
35	AN1	IN	Modulator wheel input. A voltage from the modulator wheel is converted into digital data by a built-in ADC.
42	VREF	IN	Reference voltage (+5V) for the built-in ADCs

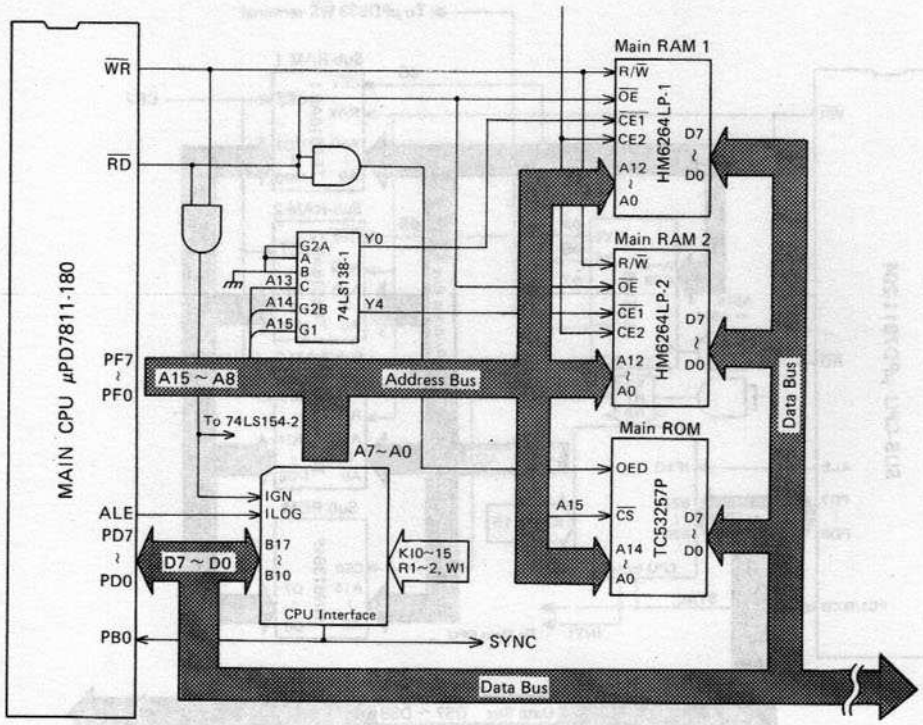
43	AVCC	IN	+5V power source for the built-in ADCs
44	$\overline{RD}$	OUT	Read signal. Drops to "L" when MAIN CPU reads data from the ROM and the RAMs.
45	$\overline{WR}$	OUT	Write signal. Drops to "L" when MAIN CPU writes data into the RAMs.
46	ALE	OUT	Address Latch Enable. When "H", data bus D0 ~ D7 becomes address bus A0 ~ A7.
47 ~ 54	PF0(A8)~PF7(A15)	OUT	Upper address bus (A8 ~ A15)
55 ~ 62	PD0(D0)~PD7(D7)	IN/OUT	Data bus (D0 ~ D7)
63, 64	VDD, VCC	IN	+5V power source

8. SUB-CPU (μPD7811-204)

PIN NO.	TERMINAL NAME	IN/OUT	FUNCTION
1~8	PA0(L0)~PA7(L7)	OUT	LED drive signals
9	PB0	IN	Data receive request from Master Music LSI
10	PB1	IN	Data receive request from Slave Music LSI
11	PB2	OUT	Master Music LSI chip select signal
12	PB3	OUT	Slave Music LSI chip select signal
13	PB4	OUT	Write enable signal for Music LSIs
14	PB5	OUT	ID (Interrupt Disable) signal. When SUB-CPU is busy, it sends ID signal to Music LSIs so as not to be interrupted.
15	PB6 (LDC)	OUT	Stays "H" level for approximately 830 milli-seconds after the power switch is turned on in order to avoid mis-lighting the LEDs at Power ON.
17	PC0 (TXD, L11)	OUT	LED drive signal
18	PC1 (RXD, SYNC)	IN	Synchronous signal from MAIN CPU
19	PC2 (SCK, CONT)	IN/OUT	Control signal between MAIN and SUB-CPUs
20	PC3 (INT2)	IN	Interrupt signal from Music LSIs
21	PC4 (T0)	OUT	Metronome envelope signal
22~24	PC5(L8)~PC7(L10)	OUT	LED drive signals
26	INT1	IN	Interrupt signal from MAIN CPU

28	$\overline{\text{RESET}}$	IN	At Power ON, the terminal stays "L" level for a while in order to initialize the internal circuits.
31	X1	IN	12MHz clock pulse
32	VSS	IN	Ground (0V) power source
44	$\overline{\text{RD}}$	OUT	Read signal. Drops to "L" when SUB-CPU reads data from the ROM, RAMs or Music LSIs.
45	$\overline{\text{WR}}$	OUT	Write signal. Drops to "L" when SUB-CPU writes data into the RAMs or Music LSIs.
46	ALE	OUT	Address Latch Enable. When "H", data bus PD9 (DS0) ~ PD7 (DS7) becomes address bus AS0 ~ AS7.
47~54	PF0(AS15) ~ PF7 (AS8)	OUT	Upper address bus
55~62	PD0(DS0) ~ PD7 (DS7)	OUT	Data bus
63, 64	VDD, VCC	IN	+5V power source

9. MAIN RAMS & ROM ACCESS



The first 2K bytes of Main RAM 1 are the data area for system execution and the rest of 6K bytes and the whole 8K bytes of Main RAM 2 are the data area for programmed music.
The capacity of Main ROM is 32K bytes and contains the program for system execution.
The lower address bus A0 ~ A7 is provided from CPU Interface LSI. When signal ALE from MAIN CPU rises to "H", data bus (D0 ~ D7) becomes address bus (A0 ~ A7) in CPU Interface LSI. The upper address A8 ~ A15 is directly supplied from MAIN CPU.

Chip select signals are provided from signals A13 ~ A15:

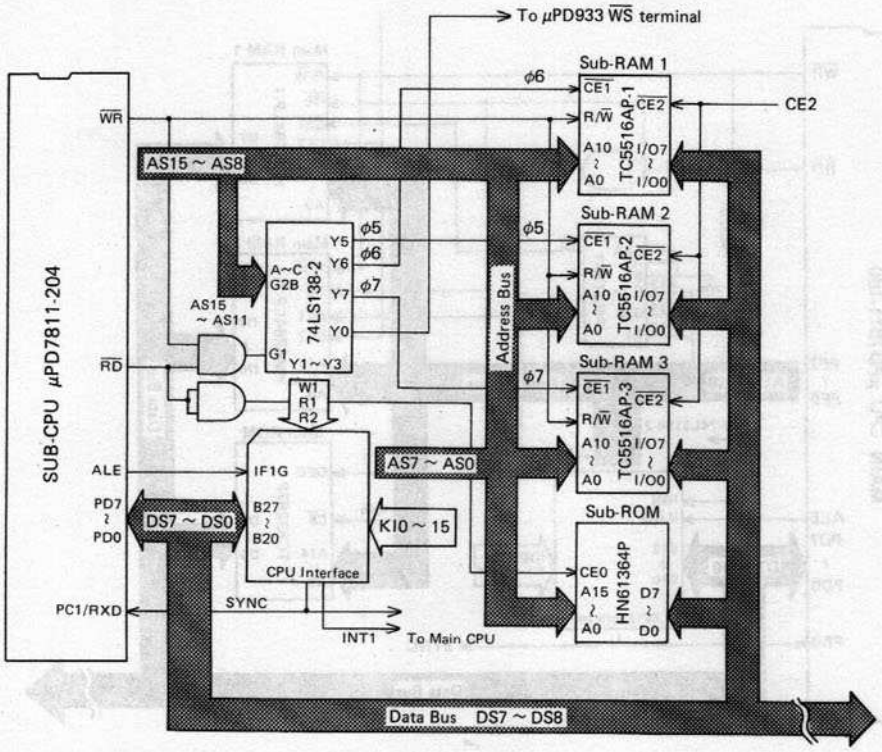
A13	A14	A5	
L	L	H	Main RAM1 chip selection
H	L	L	Main RAM2 chip selection
X	X	L	Main ROM chip selection

'LS138, 'S138 FUNCTION TABLE

INPUT					OUTPUT							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

10. SUB-RAMS & ROM ACCESS



TC5516AP is a 2K-byte RAM while HN61364P is an 8K-byte ROM.

Sub-RAM 1 – Tone data area for Memory Banks A and B.
Sub-RAM 2 – Data area for system execution.
Sub-RAM 3 – Tone data area for Memory Banks C and D.

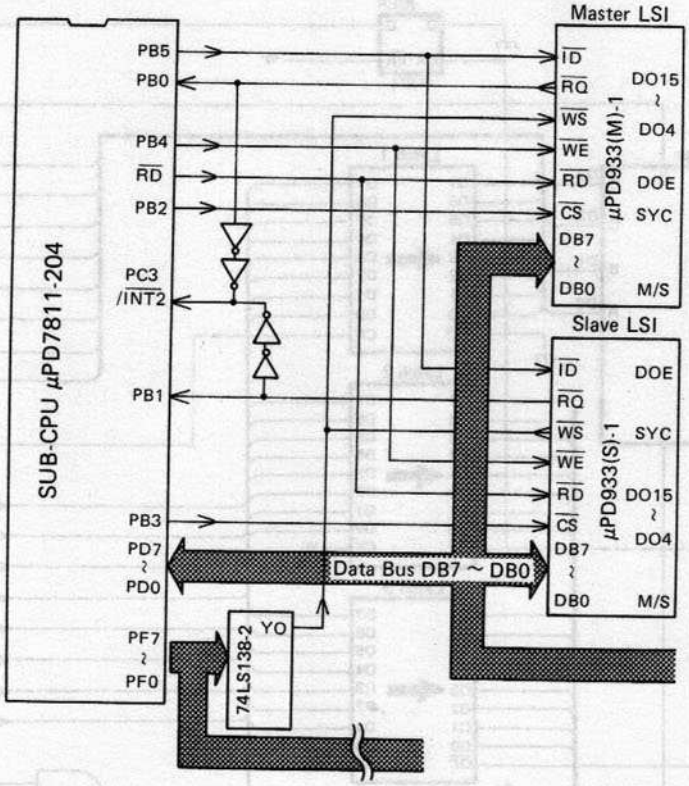
In the same procedures as for MAIN CPU, lower address bus AS0 ~ AS7 is generated from data bus DS0 ~ DS7 in CPU Interface LSI when signal ALE is "H". Upper address signals A8 ~ A15 are provided from SUB-CPU directly.

Decoder 74LS138-2 generates chip selection signals and other control signals from signals AS11 ~ AS15 as follows:

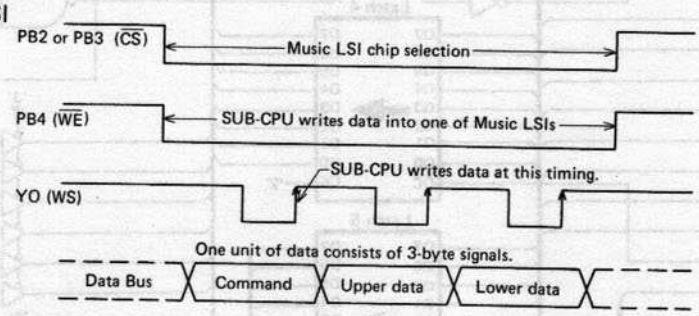
74LS138			IN					OUT								
			A14	A15	A13	A12	A11	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
A15	G1	Y0	L	H	L	L	L	L	H	H	H	H	H	H	H	Write strobe for Music LSIs
A14	G2	Y1	L	H	L	L	H	H	L	H	H	H	H	H	H	Data transfer: SUB-CPU → MAIN CPU
RD·WR	G2B	Y2	L	H	L	H	L	H	H	L	H	H	H	H	H	Data transfer: MAIN CPU → SUB-CPU
A11	A	Y3	L	H	L	H	H	H	H	H	L	H	H	H	H	Data transfer: MAIN CPU → SUB-CPU
A12	B	Y4	L	H	H	L	L	H	H	H	H	L	H	H	H	MAIN CPU interruption
A13	C	Y5	L	H	H	L	H	H	H	H	H	H	L	H	H	Sub-RAM2 chip selection
		Y6	L	H	H	H	L	H	H	H	H	H	H	L	H	Sub-RAM1 chip selection
		Y7	L	H	H	H	H	H	H	H	H	H	H	H	L	Sub-RAM3 chip selection

11. MUSIC LSIS ACCESS

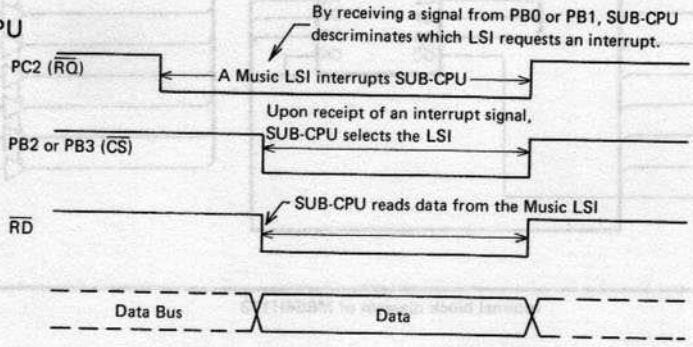
CZ-5000 employs two Music LSIs, Master LSI and Slave LSI, which are controlled by SUB-CPU.



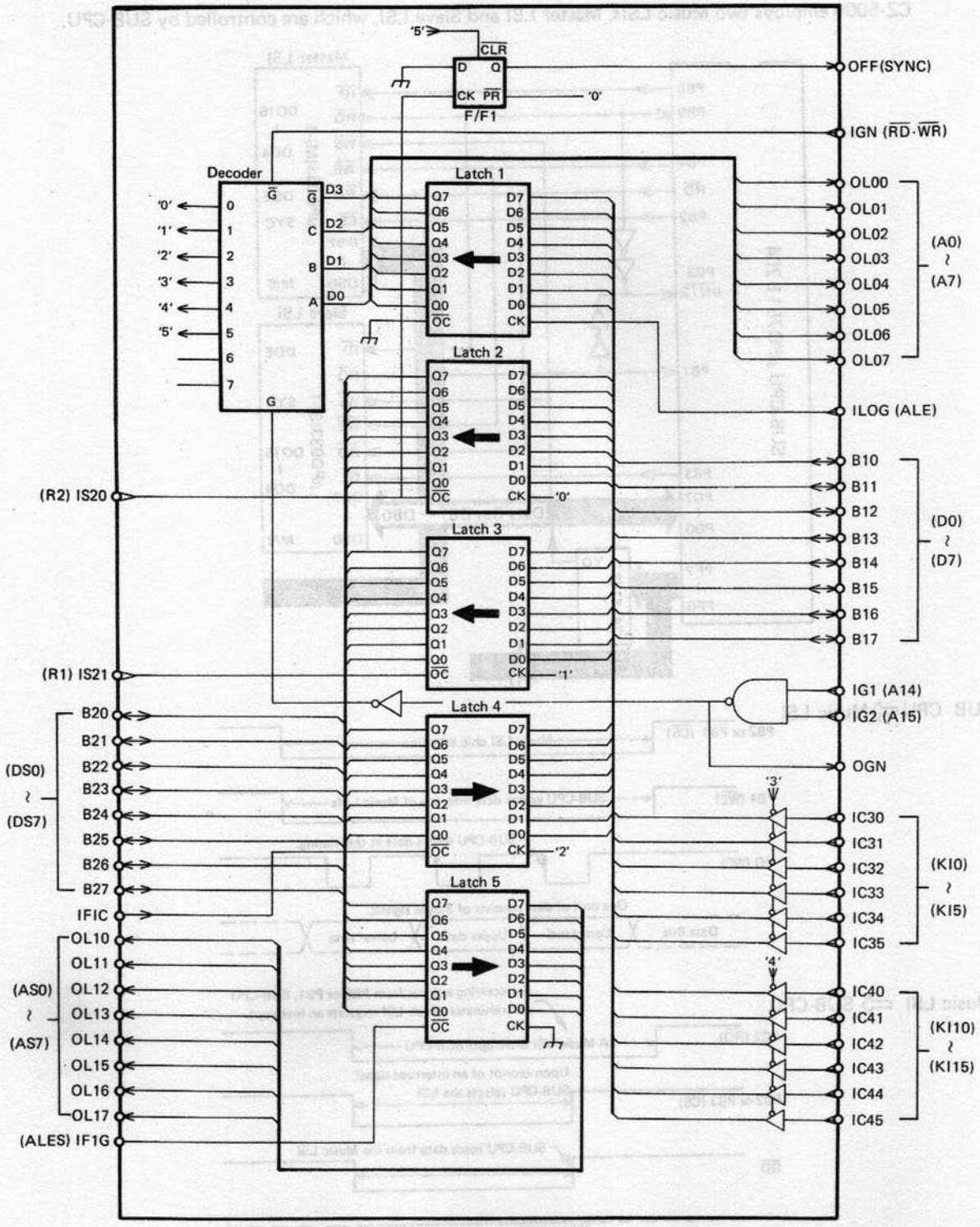
(1) SUB CPU ⇨ Music LSI



(2) Music LSI ⇨ SUB-CPU



12. CPU INTERFACE (MB64H173)



Internal block diagram of MB64H173

12-1. Function of Each Block

F/F 1 – Set by the clock pulse '0' and signal R2 from SUB-CPU, and generates signal SYNC which synchronizes MAIN and SUB-CPUs.

FUNCTION TABLE

INPUT				OUTPUT	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Decoder 1 – Generates clock pulses for the latches from signals A0 ~ A3, A14, A15, $\overline{RD}$ and $\overline{WR}$.

FUNCTION TABLE

ENABLE INPUT		SELECT INPUT			OUTPUT							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = \overline{G2A} + \overline{G2B}$

Latch 1 – Converts MAIN CPU's data bus (D0 ~ D7) into address bus A0 ~ A7, and generates clock pulses '0' ~ '5'.

Latch 2 – For the data transfer from MAIN CPU to SUB-CPU.

Latch 3 – Transfers the data from the pitch bender and modulator wheel to SUB-CPU.

Latch 4 – For the data transfer from SUB-CPU to MAIN CPU.

Latch 5 – Converts SUB-CPU's data bus (DS0 ~ DS7) into address bus AS0 ~ AS7.

FUNCTION TABLE (EACH LATCH)

INPUT			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

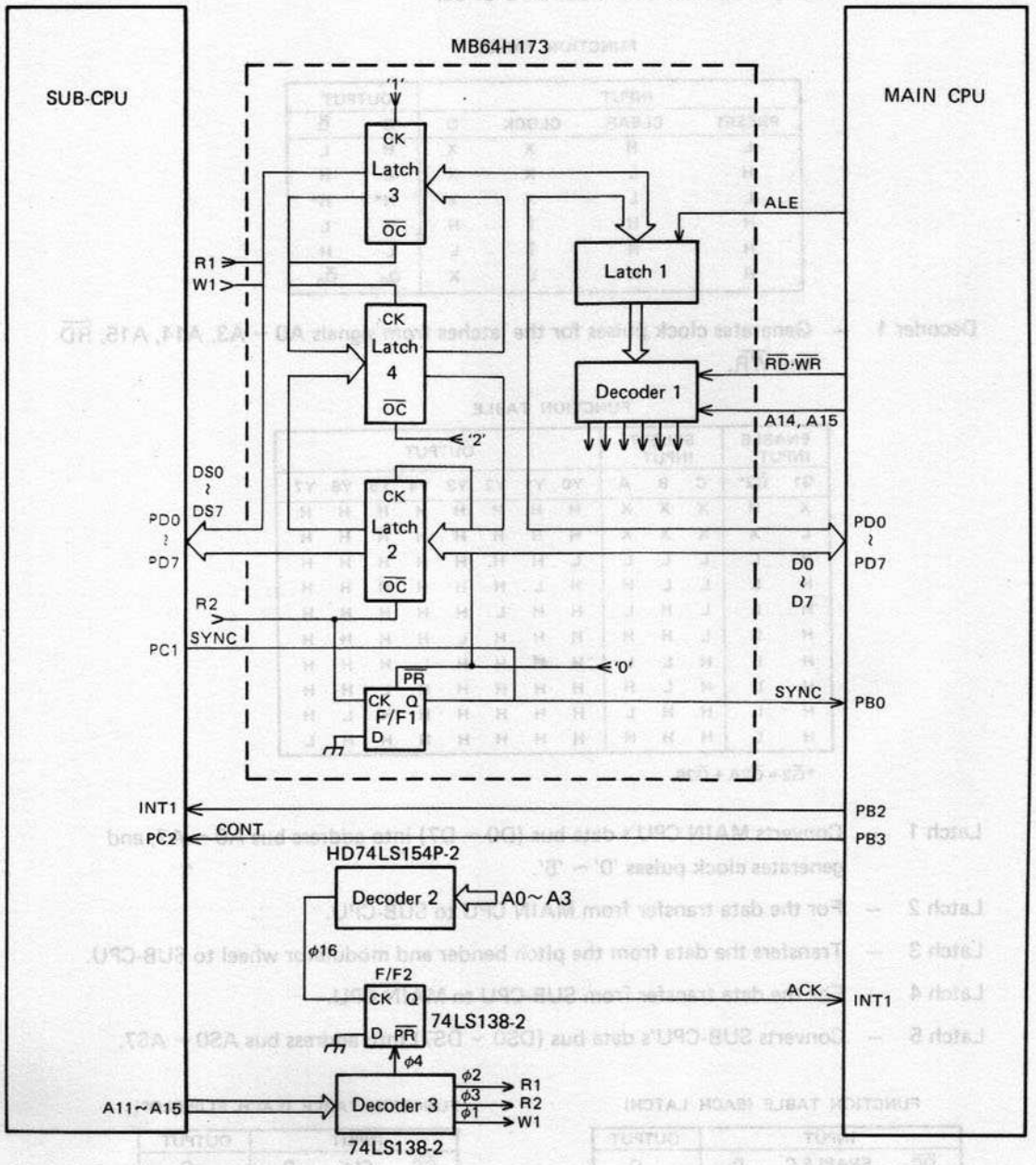
Latch 1 and 5

FUNCTION TABLE (EACH FLIP-FLOP)

INPUT			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Latch 2 ~ 4

12-2. Data Transfer Procedures



(1) Pitch Bender & Modulator ⇨ SUB-CPU.

① Voltage level from the pitch bender or the modulator is converted into digital data in the CPU's built-in ADC (Analog to Digital Converter) and output from data bus (D0 ~ D7).

② The data is entered into CPU Interface LSI.

③ Sending signal R1, SUB-CPU sets Latch 3 and reads data periodically.

(2) MAIN CPU ⇨ SUB-CPU.

① Via Latch 1 and Decoder 1, MAIN CPU drops clock pulse '0' to "L" level.
By clock pulse '0', F/F 1 is preset to rise signal SYNC.

② MAIN CPU puts data on data bus D0 ~ D7, and at the same time, clock pulse '0' rises to "H" level.
At the rising edge of clock pulse '0', data from MAIN CPU is set in Latch 2.

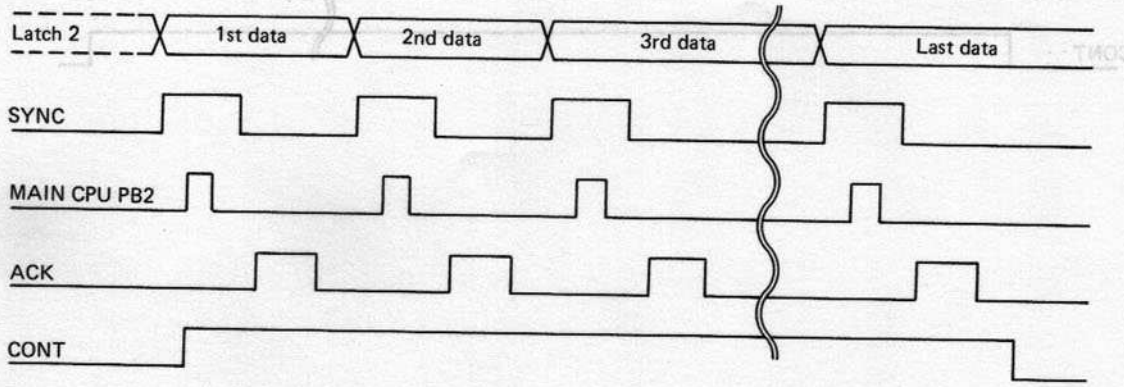
③ MAIN CPU interrupts SUB-CPU from terminal PB2, and simultaneously generates signal CONT from terminal PB3.

④ Generating signal R2 from Decoder 3, SUB-CPU reads the data from Latch 2 via data bus DS0 ~ DS7.

⑤ SUB-CPU sends signal ACK to MAIN CPU via Decoder 3 and F/F 2.
Upon receipt of signal ACK, MAIN CPU confirms that SUB-CPU has received the data and generates signal ϕ16 in Decoder 2.

⑥ When all the data have sent to SUB-CPU by repeating the above procedures ①~⑤, MAIN CPU drops signal CONT to "L".

⑦ Confirming that both CONT and SYNC are "L", SUB-CPU determines that all the data have been received.



(3) Sub-CPU ⇨ MAIN CPU.

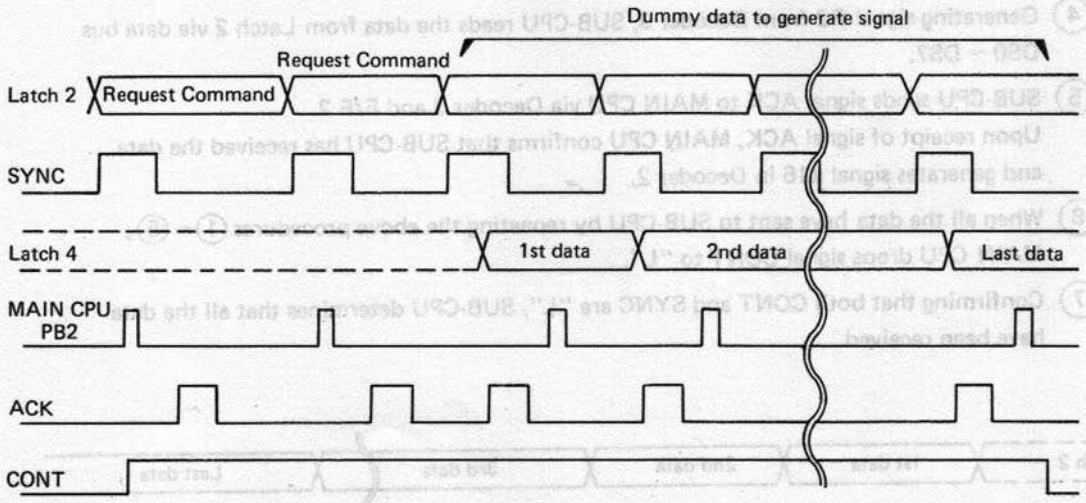
(1) In the same procedures as stated in the item (2), MAIN CPU sends "Request Command" that inquires SUB-CPU to transmit data.

(2) SUB-CPU puts data on the data bus DS0 ~ DS7 and sets the data in Latch 4 by signal W1. SUB-CPU then presets F/F 2 by pulse ϕ4, causing signal ACK to be entered in MAIN CPU.

(3) Acknowledging that the data is set in Latch 4 by signal ACK, MAIN CPU generates clock pulse '2', causing the data from SUB-CPU to be put on MAIN CPU data bus D0 ~ D7.

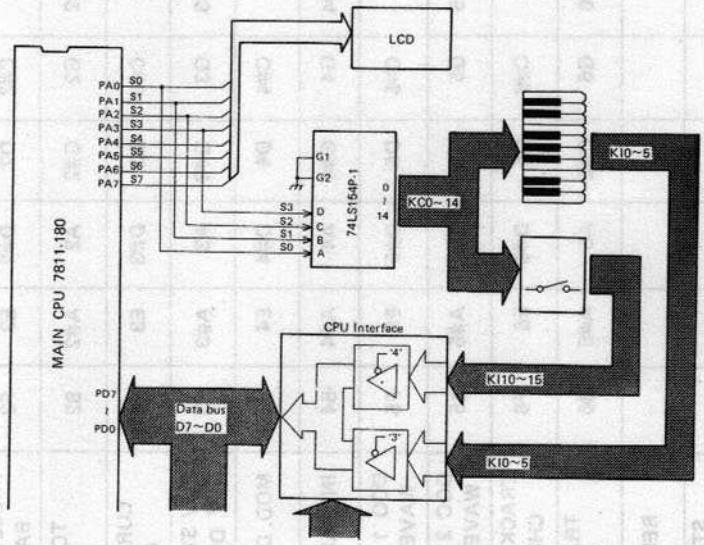
(4) After receiving the data, MAIN CPU sends SUB-CPU an interrupt signal from terminal PB2, and by the interrupt signal, SUB-CPU confirms that the data is received by MAIN CPU.

(5) Repeating the above procedures (2) ~ (4), SUB-CPU sends the next data to MAIN CPU.



(4) Key and switch scanning

Receiving a key common signal from data bus, MAIN CPU discriminates a key or a switch input.



(1) From signals PA0 ~ PA3 of MAIN CPU, 4-line to 16-line decoder 74LS154P-1 generates key common signals KC0 ~ KC14.

(2) When a key or a switch is hit, one of the input signals KI0 ~ KI5 (for keys) or KI10 ~ KI15 (for switches) is entered in CPU Interface MB64H173.

(3) MAIN CPU generates the clock pulse '3' (for keys) or '4' (for switches), causing the tristate buffers to be opened.

(4) The input pulse is entered into data bus.

(5) Discriminating the contents of the data bus, MAIN CPU determines which key is hit.

INPUT						OUTPUT															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

74LS154P Function Table

13. KEY MATRIX

	KI 0	KI 1	KI 2	KI 3	KI 4	KI 5	KI 10	KI 11	KI 12	KI 13	KI 14	KI 15
KC 0	C2	C#2	D2	D#2	E2	F2	PRESET BANK-C	PRESET BANK-D	PRESET BANK-A	MEMORY BANK-B	MEMORY BANK-C	MEMORY BANK-D
KC 1	F#2	G2	G#2	A2	A#2	B2	TONE 5	TONE 6	TONE 7	TONE 8	PRESET BANK-A	PRESET BANK-B
KC 2	C3	C#3	D3	D#3	E3	F3	CURSOR NO	CURSOR YES	TONE 1	TONE 2	TONE 3	TONE 4
KC 3	F#3	G3	G#3	A3	A#3	B3	ENV STEP ▼ DOWN	ENV STEP ▲ UP	ENV POINT SUSTAIN	ENV POINT END	VALUE ▼ SAVE	VALUE ▲ LOAD
KC 4	C4	C#4	D4	D#4	E4	F4	MOD. DEPTH	BEND RANGE	GLIDE	PORTAMENTO	MT	CARTRIDGE
KC 5	F#4	G4	G#4	A4	A#4	B4	INITIALISE	OCTAVE	VIBRATO	LINE SELECT	RING	NOISE
KC 6	C5	C#5	D5	D#5	E5	F5	DCO 1 WAVEFORM	DCO 1 ENV	DCW 1 KEY-F	DCW 1 ENV	DCA 1 KEY-F	DCA 1 ENV
KC 7	F#5	G5	G#5	A5	A#5	B5	DOC 2 WAVEFORM	DCO 2 ENV	DCW 2 KEY-F	DCW 2 ENV	DCA 2 KEY-F	DCA 2 ENV
KC 8	C6	C#6	D6	D#6	E6	F6	TRACK CHECK	REPEAT	TEMPO ▲ UP	TEMPO ▼ DOWN	DELETE	DETUNE
KC 9	F#6	G6	G#6	A6	A#6	B6	TRACK 3	TRACK 4	TRACK 5	TRACK 6	TRACK 7	TRACK 8
KC10	C7						RESET	RECORD	REC. TRACK MANUAL	REC. TRACK REAL TIME	TRACK 1	TRACK 2
KC11							STOP ■	PLAY ▶	FWD ▶▶	REV ◀◀	MEMORY PROTECT	FOOT SW (SUS)
KC12												MODULATION ON/OFF
KC13	C2					C7	NORMAL	TONE MIX	KEY SPLIT	SEQUENCER	SOLO	MIDI
KC14							PORTAMENTO ON/OFF	GLIDE ON/OFF	KEY TRANSPOSE	MASTER TUNE	COMPARE/ RECALL	WRITE

14. LED DRIVING CIRCUITS

74LS174

FUNCTION TABLE

(EACH FLIP-FLOP)

INPUT			OUTPUT	
CLEAR	CLOCK	D	Q	$\overline{Q}\uparrow$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

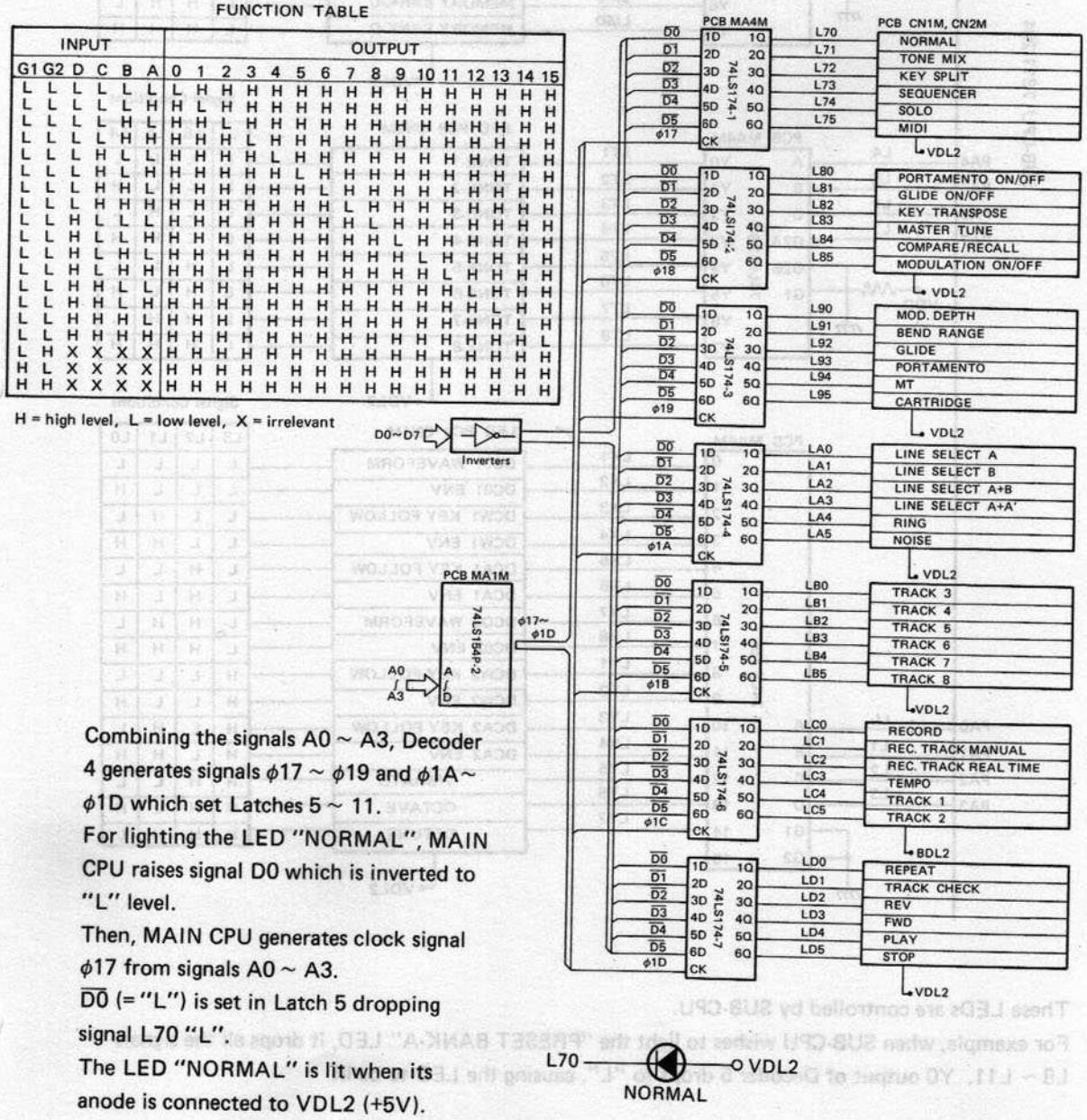
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.

74LS154P

FUNCTION TABLE

INPUT						OUTPUT													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant



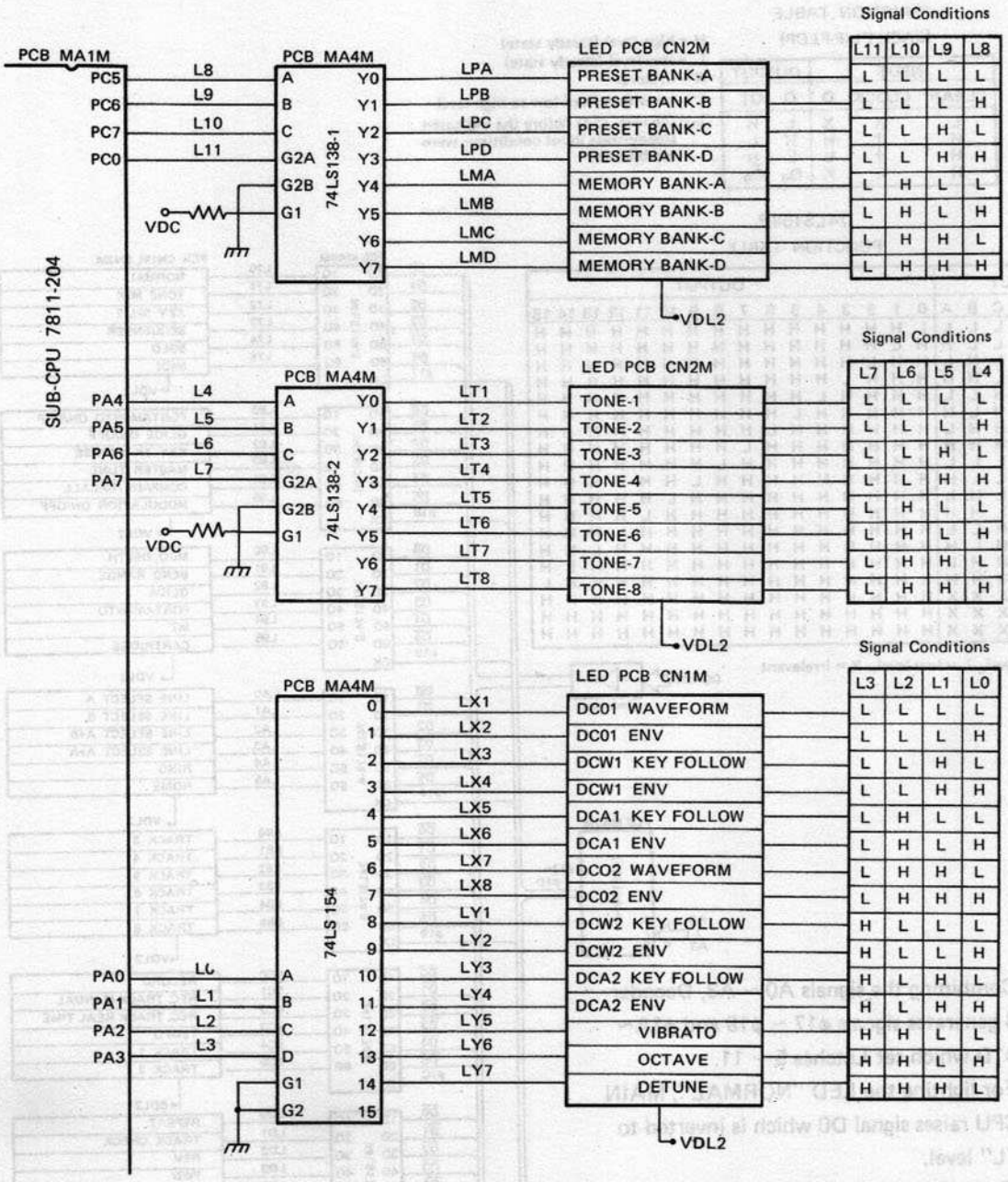
Combining the signals A0 ~ A3, Decoder 4 generates signals ϕ17 ~ ϕ19 and ϕ1A ~ ϕ1D which set Latches 5 ~ 11.

For lighting the LED "NORMAL", MAIN CPU raises signal D0 which is inverted to "L" level.

Then, MAIN CPU generates clock signal ϕ17 from signals A0 ~ A3.

$\overline{D0}$ (= "L") is set in Latch 5 dropping signal L70 "L".

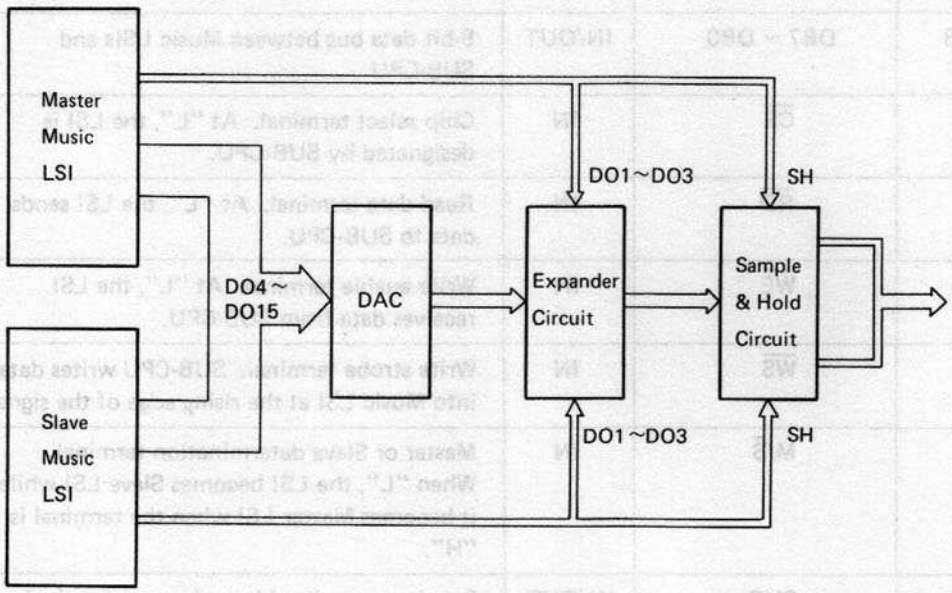
The LED "NORMAL" is lit when its anode is connected to VDL2 (+5V).



These LEDs are controlled by SUB-CPU.

For example, when SUB-CPU wishes to light the "PRESET BANK-A" LED, it drops all the signals L8 ~ L11. Y0 output of Decoder 5 drops to "L", causing the LED to be lit.

15. ANALOG CIRCUIT BLOCK DIAGRAM



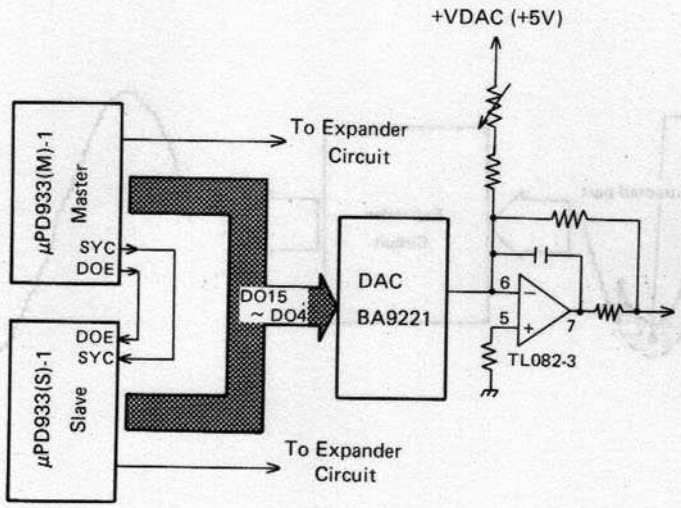
Master and Slave Music LSIs provide 12-bit digital sounds for DAC (Digital to Analog Converter). By means of time sharing, DAC mixes the two different signals and converts into analog waveforms. To obtain a wide dynamic range of the amplitude, Music LSIs' outputs are contracted and are reformed into a proper waveform shape by Expander circuits. Sample & Hold circuit removes a high frequency noise called as glitch contained in the DAC output.
Sample & Hold Circuit also separates the Master and Slave waveforms.

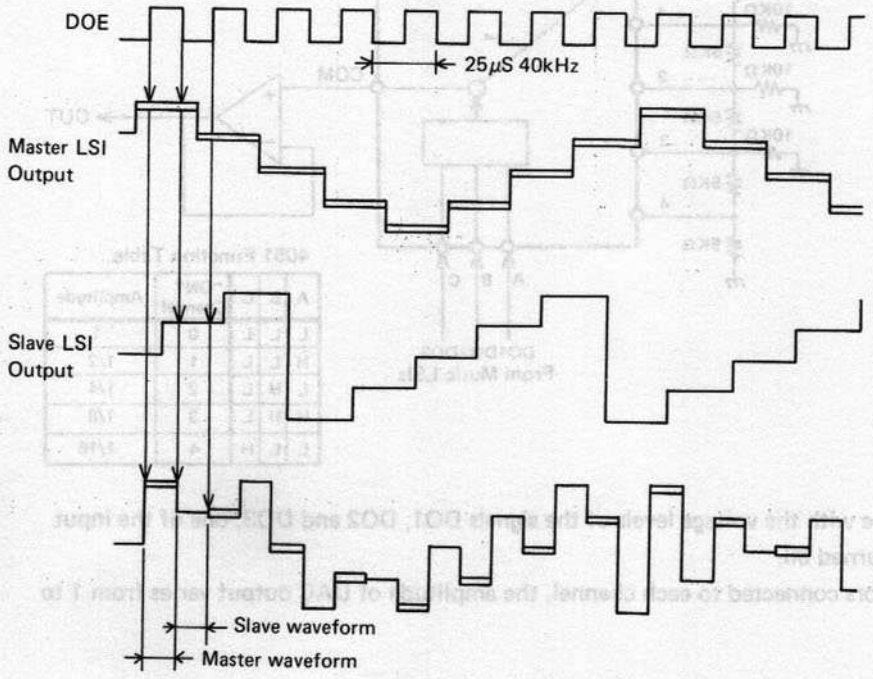
16. MUSIC LSI (μPD933)

PIN NO.	TERMINAL NAME	IN/OUT	FUNCTION
1 ~ 8	DB7 ~ DB0	IN/OUT	8-bit data bus between Music LSIs and SUB-CPU
9	$\overline{CS}$	IN	Chip select terminal. At "L", the LSI is designated by SUB-CPU.
10	$\overline{RD}$	IN	Read data terminal. At "L", the LSI sends data to SUB-CPU.
11	$\overline{WE}$	IN	Write enable terminal. At "L", the LSI receives data from SUB-CPU.
12	$\overline{WS}$	IN	Write strobe terminal. SUB-CPU writes data into Music LSI at the rising edge of the signal.
16	M/$\overline{S}$	IN	Master or Slave determination terminal. When "L", the LSI becomes Slave LSI while it becomes Master LSI when the terminal is "H".
17	SYC	IN/OUT	Synchronous signal input/output terminal. The synchronous signal is sent from Master LSI to Slave LSI.
18	CLK	IN	4.48 MHz clock pulse input
21	RST	IN	Reset signal input. Normally the terminal stays "L". At power ON, the terminal rises to "H" level for a while and the internal circuits of the LSI are initialized.
22	DOE	IN/OUT	Data output enable terminal. At "H", digital sound signals are output from Master LSI while Slave LSI outputs sound signal at "L" level.
23	SH	OUT	40 KHz sampling signal for Sample & Hold circuit
25 ~ 27	DO1 ~ DO3	OUT	Control signals for Expander circuit
28 ~ 39	DO4 ~ DO15	OUT	12-bit digital sound signals
40	VDD	IN	+5V power source

17. DAC (Digital to Analog Converter)

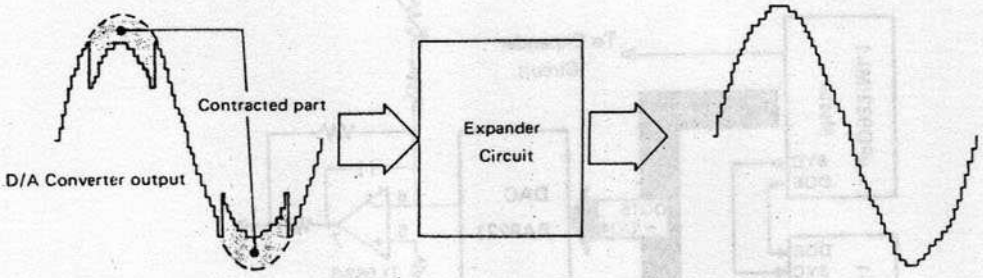
The two Music LSIs output different waveforms. When signal DOE is "H", Master LSI outputs a waveform while Slave LSI outputs a waveform at "L" level of DOE.

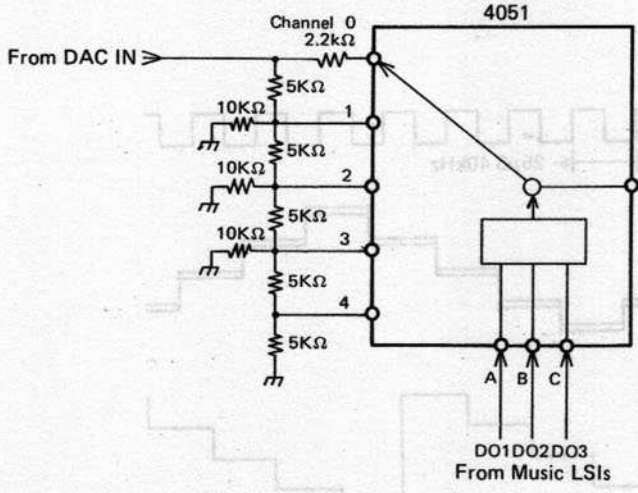




18. EXPANDER CIRCUIT

In order to extend the dynamic range of the melody signal, a part of DAC output waveform is contracted and expanded by Expander Circuit.



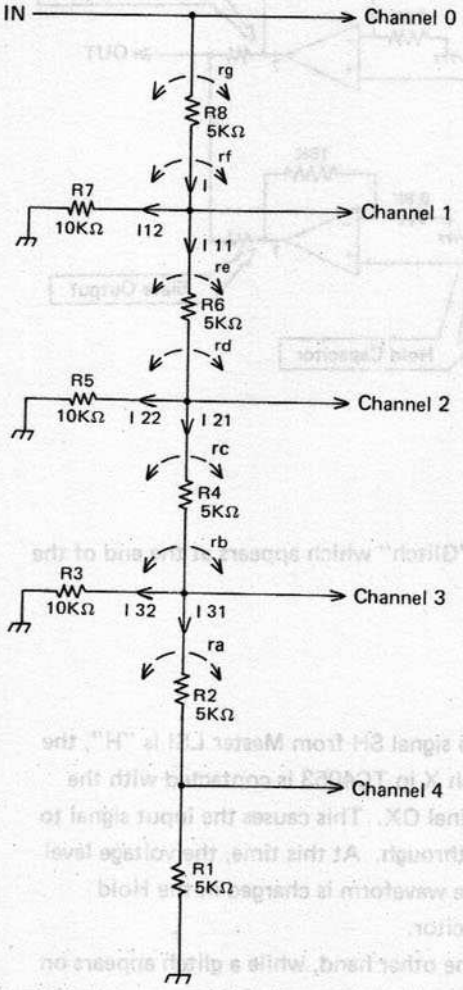


4051 Function Table

A	B	C	"ON" Channel	Amplitude
L	L	L	0	1
H	L	L	1	1/2
L	H	L	2	1/4
H	H	L	3	1/8
L	L	H	4	1/16

In accordance with the voltage levels of the signals DO1, DO2 and DO3, one of the input channels is turned on.

By the resistors connected to each channel, the amplitude of DAC output varies from 1 to 1/16.



Combined resistances at each point are:

ra = R1 (5KΩ) + R2 (5KΩ) = 10KΩ
rb = Parallel connected ra (10KΩ) and R3 (10KΩ) = 5KΩ
rc = rb (5KΩ) + R4 (5KΩ) = 10KΩ
rd = Parallel connected rc (10KΩ) and R5 (10KΩ) = 5KΩ
re = rd (5KΩ) + R6 (5KΩ) = 10KΩ
rf = Parallel connected re (10KΩ) and R7 (10KΩ) = 5KΩ
rg = rf (5KΩ) + R8 (5KΩ) = 10KΩ

Each current value is:

I = I11 + I12
I11 = I21 + I22
I21 = I31 + I32

Namely, I11 = I/2
I21 = I11/2 = I/4
I31 = I21/2 = I/8

Voltage level at each channel is:

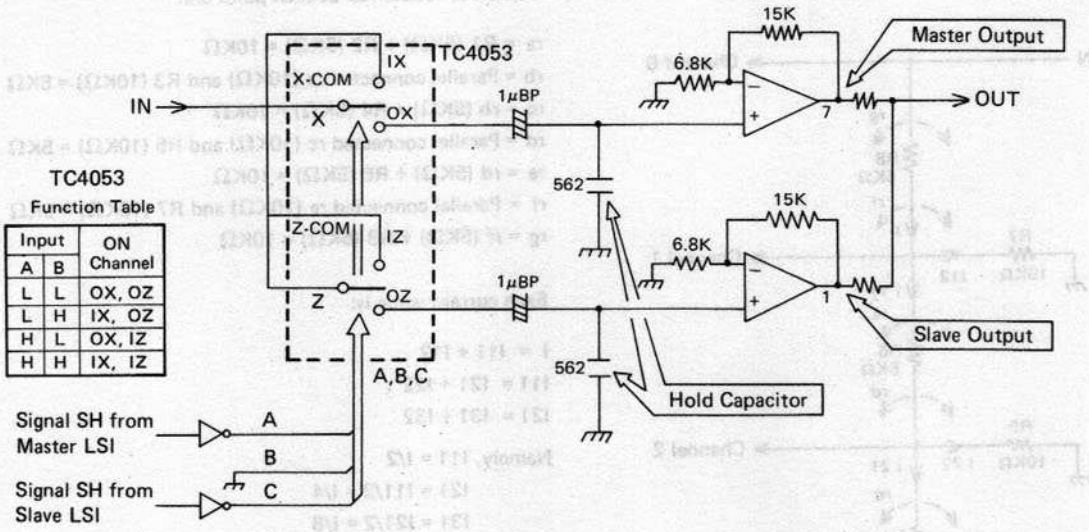
Channel 0: rg x I = 10KΩ x I
Channel 1: re x I11 = 10KΩ x I/2
Channel 2: rc x I21 = 10KΩ x I/4
Channel 3: ra x I31 = 10KΩ x I/8
Channel 4: R1 x I31 = 5KΩ x I/8 = 10K x I/16

If input voltage is E:

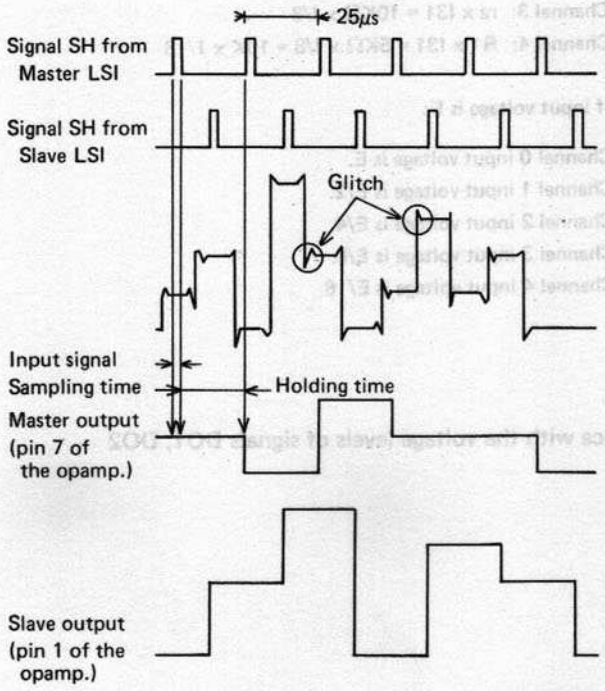
Channel 0 input voltage is E.
Channel 1 input voltage is E/2.
Channel 2 input voltage is E/4.
Channel 3 input voltage is E/8.
Channel 4 input voltage is E/16.

Thus, output of DAC is expanded in accordance with the voltage levels of signals DO1, DO2 and DO3.

19. SAMPLE & HOLD CIRCUIT



The block eliminates a high frequency noise called as "Glitch" which appears at the end of the stepped waveform.

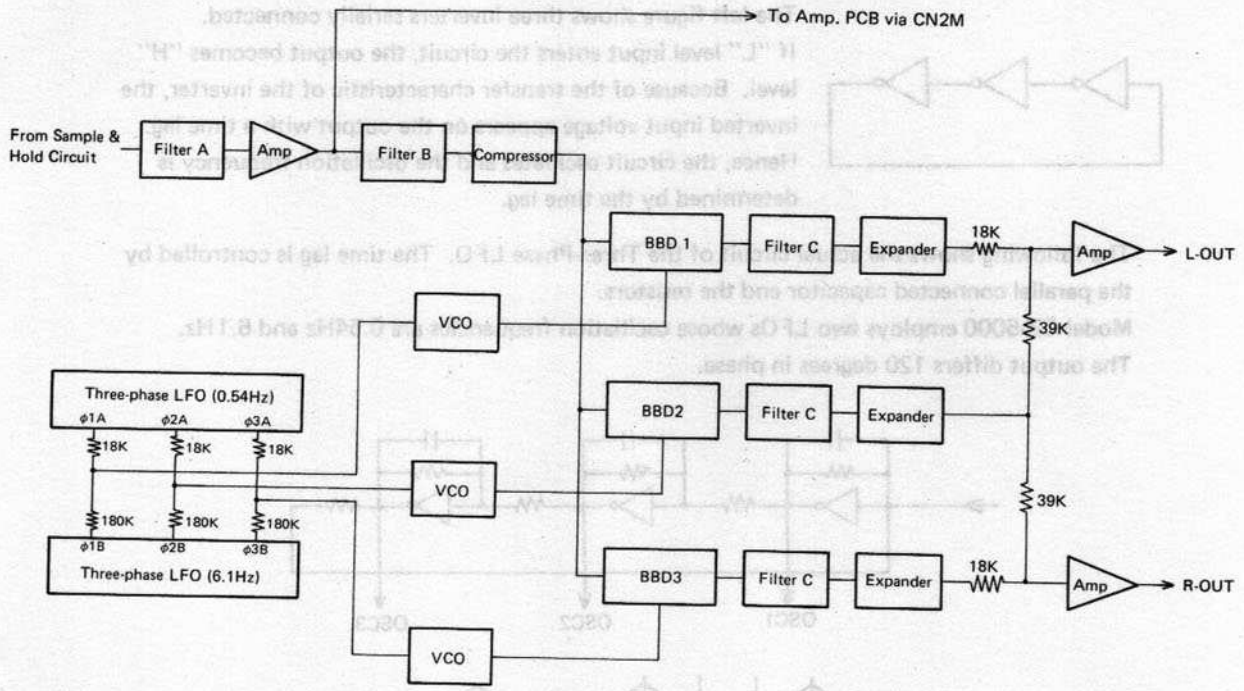


When signal SH from Master LSI is "H", the switch X in TC4053 is contacted with the terminal OX. This causes the input signal to pass through. At this time, the voltage level of the waveform is charged in the Hold Capacitor.

On the other hand, while a glitch appears on the waveform, the switch X is contacted with the terminal IX. This results in cutting off the glitch. Although no signal comes out of TC4053, the input of the opamp keeps the same voltage level by discharging of the Hold Capacitor.

Sampling or holding the slave waveform is performed by the same procedures using signal SH from Slave LSI and switch Z.

20. STEREO CHORUS CIRCUIT



Function of Each Block:

Filter A — Smoothes the stepped waveform of Samle & Hold Circuit output signal.

Filter B — As the BBD does not pass signals which exceed 20KHz, this block is a low-pass filter whose cutoff frequency is 20KHz.

Compressor — In accordance with input signal level, this block controls the amplitude. When the input signal is small, the circuit amplifies the signal whereas the amplitude becomes smaller when the input is a large-level waveform. The block is used for reducing the noise.

Three-Phase LFOs — Generates low-frequency triangle signals of 0.54Hz and 6.1Hz. The three outputs differ 120 degrees in phase.

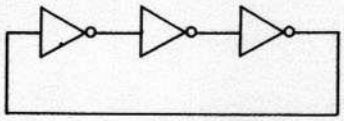
VCOs — Voltage Controlled Oscillator which generates the clock pulses for the BBDs. Their oscillation frequencies vary in accordance with the input voltage level.

BBDs — Bucket Brigade Device. Stereo chorus effect is given by delaying the right or the left sound.

Filter C — Since the output signal of the BBD carries a noise caused by clock pulses, the filter removes the noise.

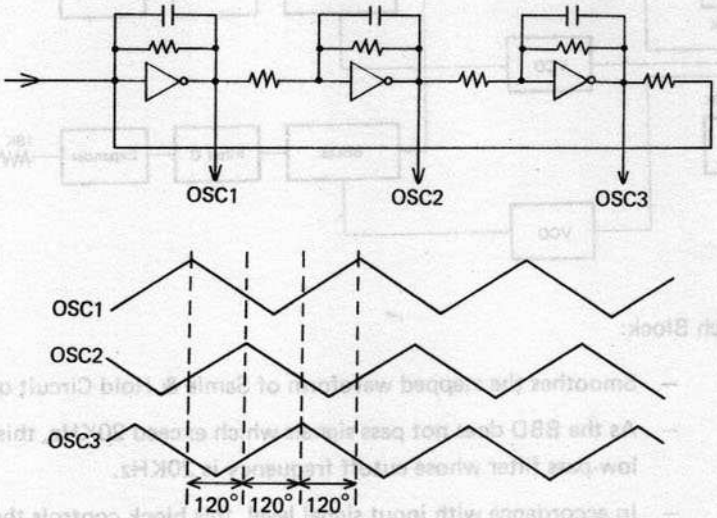
Expander — Functions contrary to the Compressor. This circuit is also used for reducing the noise.

20-1. Three-Phase LFO (Low Frequency Oscillator)

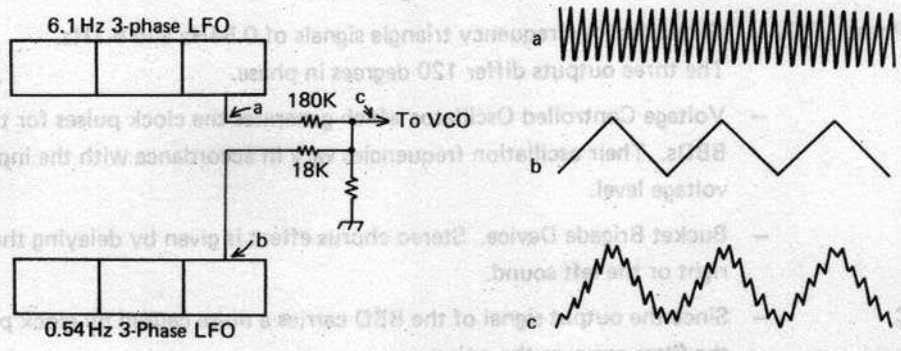


The left figure shows three inverters serially connected. If "L" level input enters the circuit, the output becomes "H" level. Because of the transfer characteristic of the inverter, the inverted input voltage appears on the output with a time lag. Hence, the circuit oscillates and the oscillation frequency is determined by the time lag.

The following shows the actual circuit of the Three-Phase LFO. The time lag is controlled by the parallel connected capacitor and the resistors.
Model CZ-5000 employs two LFOs whose oscillation frequencies are 0.54Hz and 6.1Hz.
The output differs 120 degrees in phase.

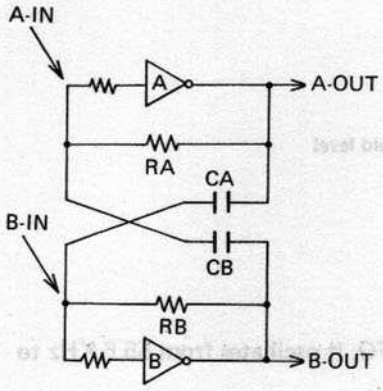


Both 0.54Hz and 6.1Hz triangle waveforms are mixed to give variational delays of the sound in the BBD.



The 0.54Hz and 6.1Hz waveforms are mixed in the ratio of 10:1 as they pass through 18Kohm and 180Kohm resistors, respectively.

20-2. VCO (Voltage Controlled Oscillator)

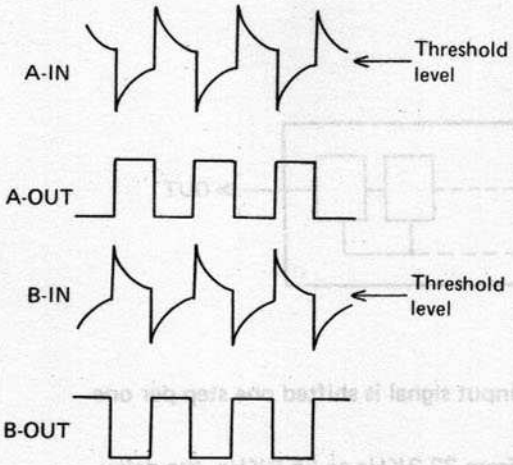


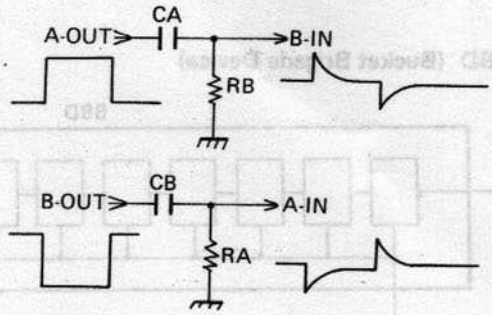
The VCO is an oscillator whose oscillation frequency varies in accordance with the input voltage level.

In the left figure, the voltage levels of the A-OUT and the B-OUT are opposite.

(1) When A-OUT is "H", B-OUT drops to "L".

(2) From A-OUT, electric current flows into B-IN via a differentiation circuit.
As a result, the voltage of B-IN drops gradually while the A-IN voltage gradually rises.

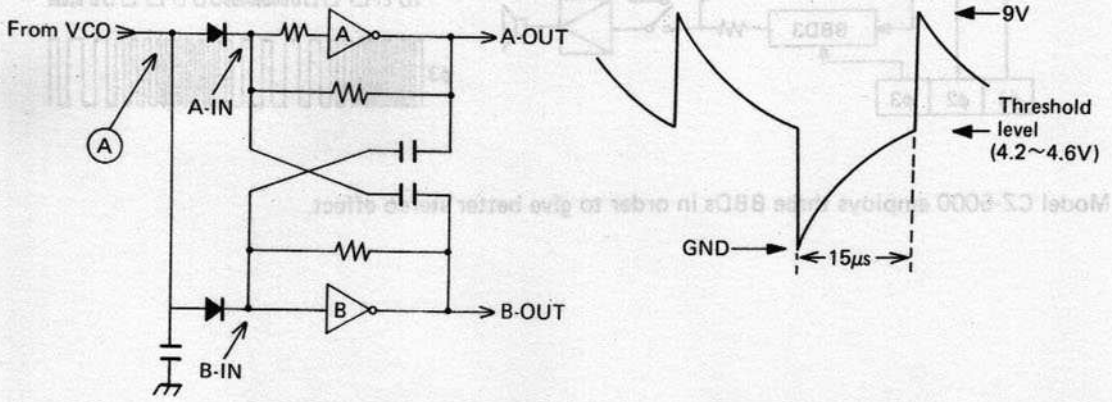




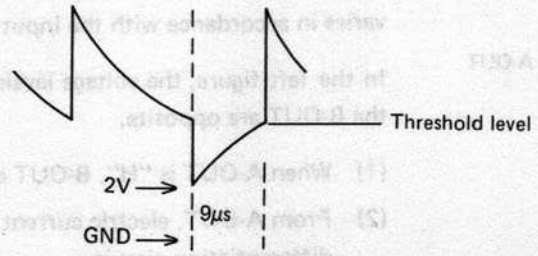
(3) When B-IN becomes lower than the threshold level, B-OUT rises to "H".
When A-IN becomes higher than the threshold level, A-OUT drops to "L".

(4) The circuit oscillates repeating the above operations.

The following shows the actual circuit of VCO. When control terminal (A) is GND (zero volt), it takes approximately 15 microseconds for the differentiation circuit to reach the threshold voltage.

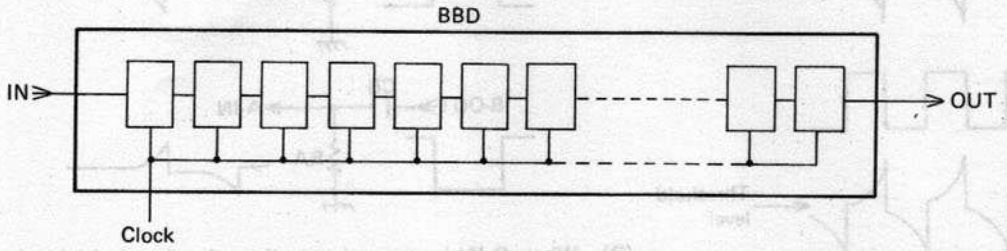


When the voltage of Ⓐ is 2 volts, it takes only 9 microseconds to reach the threshold level.



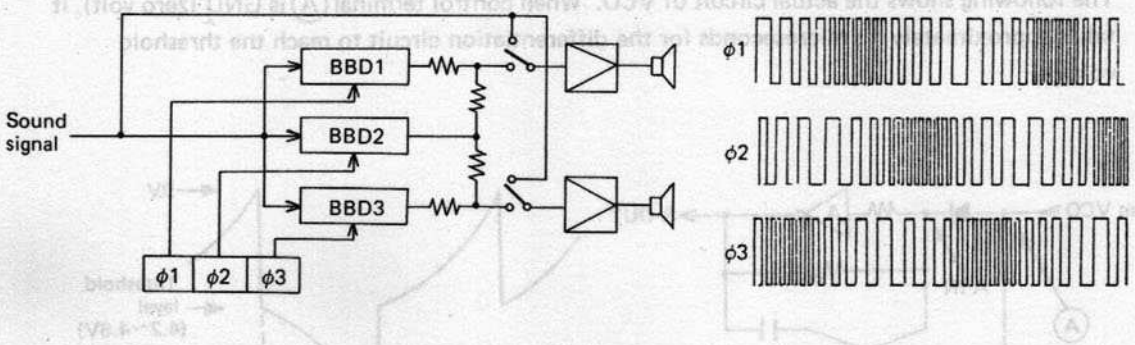
As VCO receives a triangle waveform from the Three-Phase LFO, it oscillates from 55.6 KHz to 33.3 KHz in accordance with the voltage level of LFO output.

20-3. BBD (Bucket Brigade Device)



The BBD contains serial-connected delay elements. The input signal is shifted one step per one clock pulse.

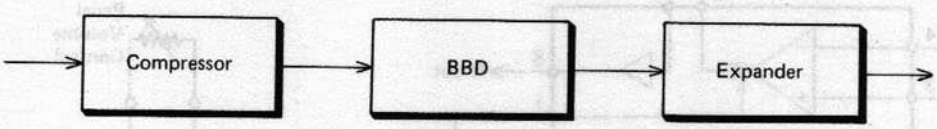
The clock pulse is generated in the VCO, and as it varies from 33.3 KHz to 55.6 KHz, the delay time varies.



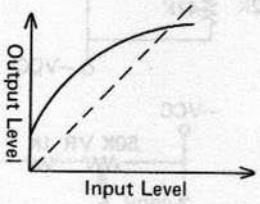
Model CZ-5000 employs three BBDs in order to give better stereo effect.

20-4. Compressor and Expander Circuits

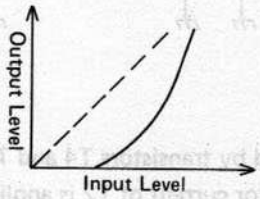
If a sound signal passes through the BBD, a noise is carried on the signal especially when the input level of the signal is low.



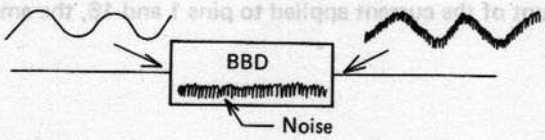
Compressor ..... When the level of input signal is low, the amplitude is large. If the input level is high, the amplitude decreases.



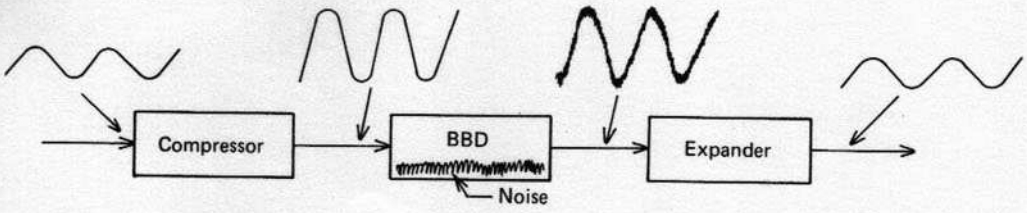
Expander ..... When the level of input signla is low, the amplitude is small. The amplitude increases when the input level is high.



When a low signal does not pass through the Compressor and the Expander;

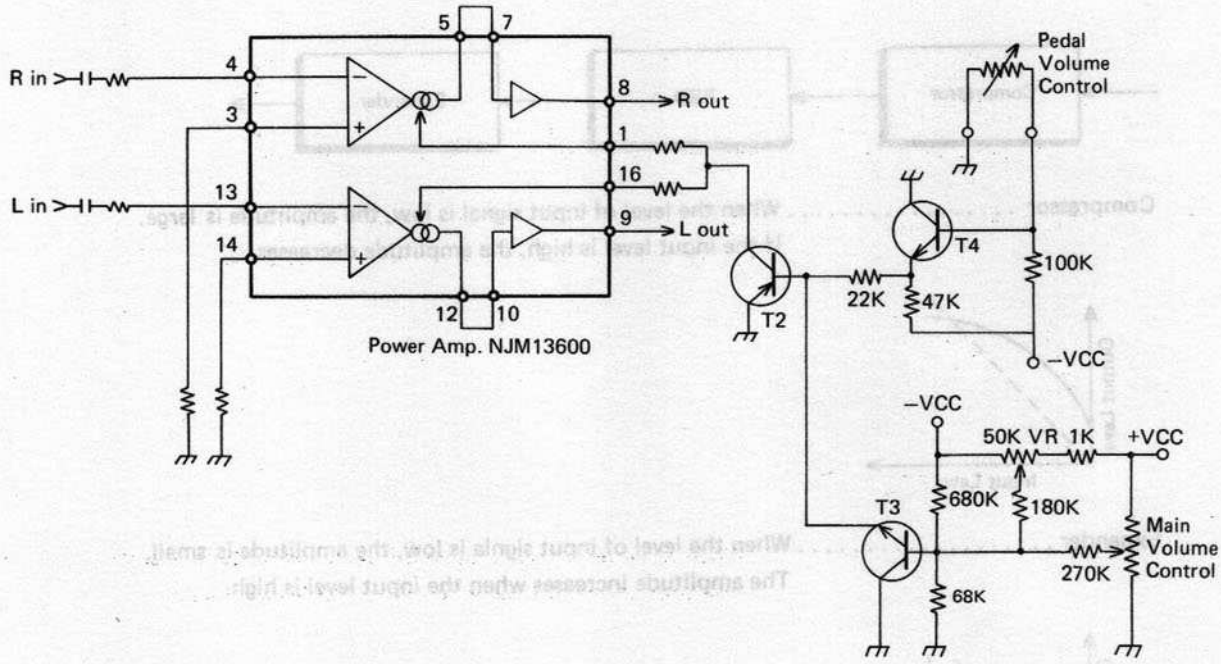


When a low signal passes through the Compressor and the Expander;



Thus, the S/N ratio of the circuit is heightened.

21. VOLUME CONTROL CIRCUIT

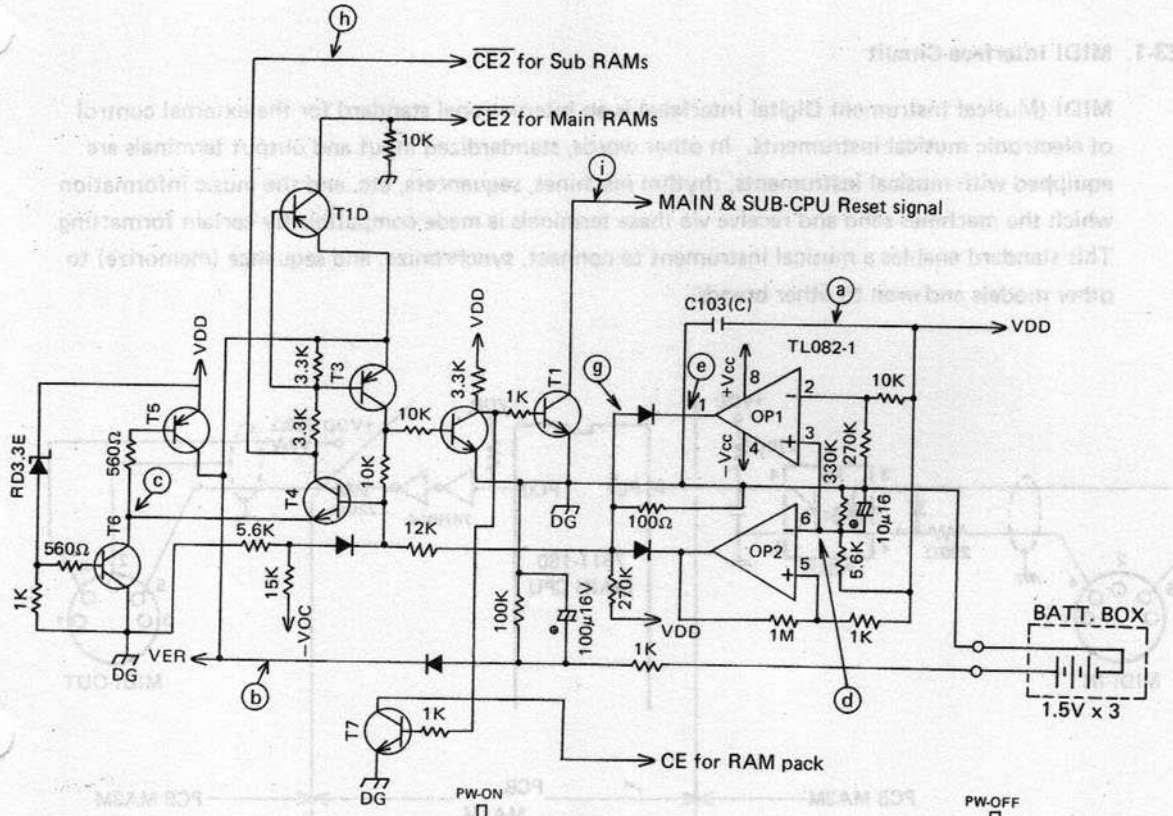


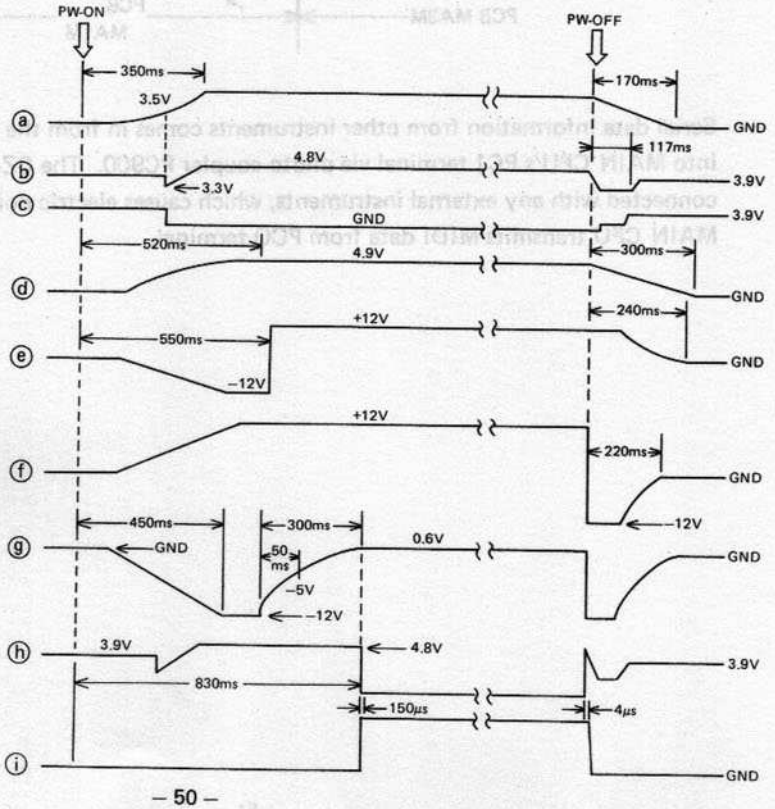
Electric current from pedal and main volume controls are amplified by transistors T4 and T3, respectively, and become the base current of transistor T2. Collector current of T2 is applied to NJM13600's control terminals.

NJM13600 is a power amplifier with control terminals.

In accordance with the amount of the current applied to pins 1 and 16, the amplitude of the amplifier varies.

22. RESET CIRCUIT

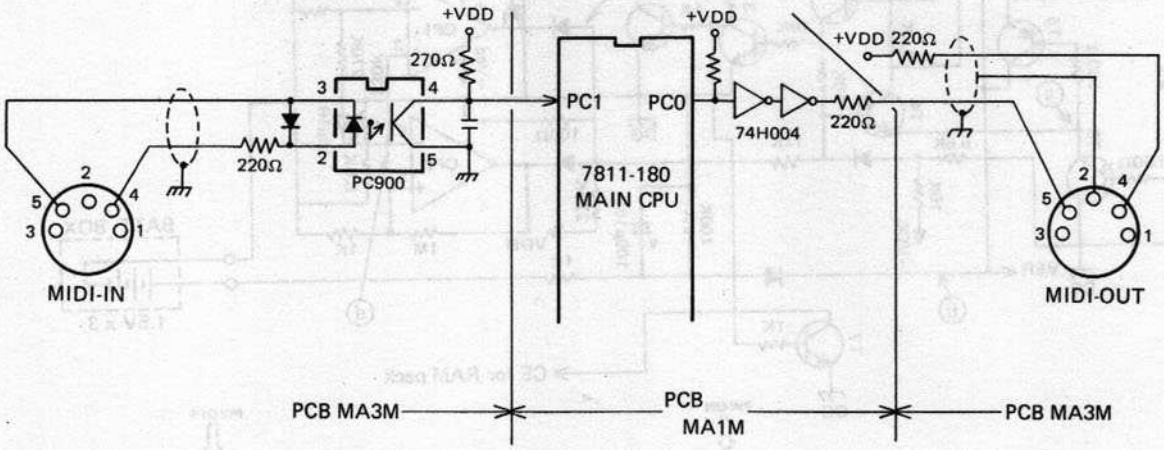




23. MIDI & MT INTERFACE CIRCUITS

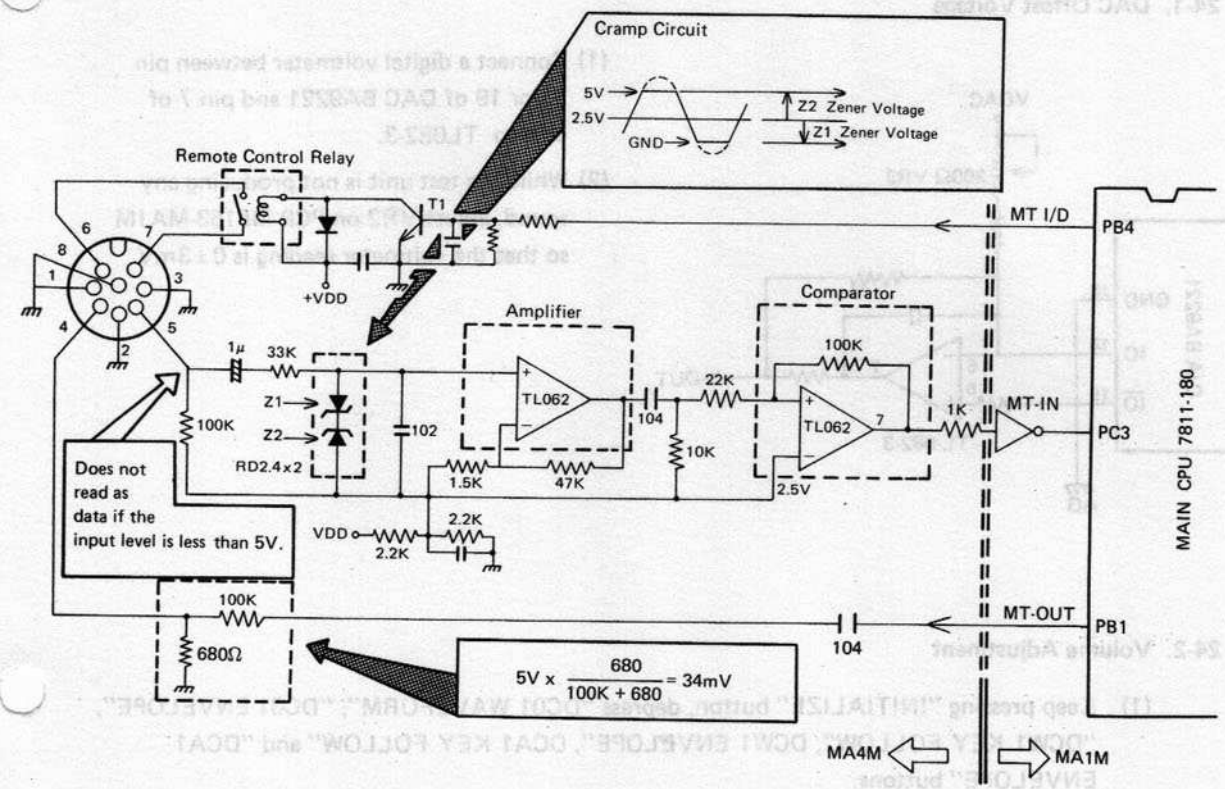
23-1. MIDI Interface Circuit

MIDI (Musical Instrument Digital Interface) is an international standard for the external control of electronic musical instruments. In other words, standardized input and output terminals are equipped with musical instruments, rhythm machines, sequencers, etc. and the music information which the machines send and receive via these terminals is made compatible by certain formatting. This standard enables a musical instrument to connect, synchronize, and sequence (memorize) to other models and even to other brands.



Serial data information from other instruments comes in from the MIDI-IN terminal and enters into MAIN CPU's PC1 terminal via photo coupler PC900. The CZ-5000 is not thus electrically connected with any external instruments, which causes electric noises to be cut off.
MAIN CPU transmits MIDI data from PCO terminal.

23-2. MT Interface Circuit



Digital data of 1 and 0 are recorded on magnetic tape as 2.4KHz and 1.2KHz sound, respectively. When data is read, a signal from a cassette tape player comes in from MT terminal pin 5.

As the voltage level varies depending on cassette tape players, the two zener diodes cramp the signal between 0 and +5 volts.

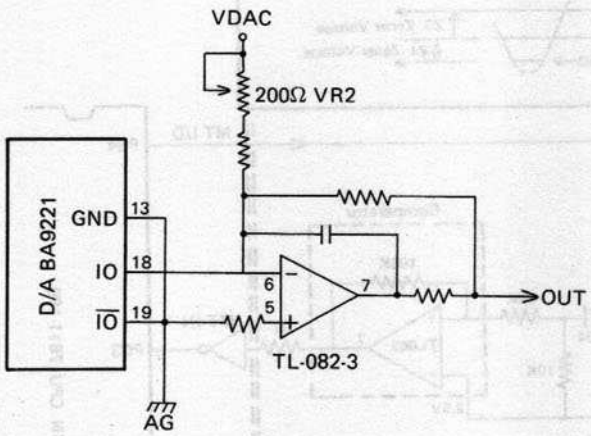
The cramped waveform is amplified by the first opamp. The second stage opamp is a comparator which examines whether the input voltage is higher or lower than 2.5V and outputs a square waveform to MAIN CPU's PC3 terminal.

As 5 volts of MAIN CPU's PB1 terminal is too high for a cassette tape recorder, it is dropped to 34 millivolts by the 100Kohm and 680ohm resistors.

Signal PB4 from MAIN CPU turns on and off the remote control relay which controls the motor in a cassette tape player.

24. ADJUSTMENT

24-1. DAC Offset Voltage



(1) Connect a digital voltmeter between pin 13 or 19 of DAC BA9221 and pin 7 of opamp TL082-3.

(2) While the test unit is not producing any sound, adjust VR2 on PCB M5153-MA1M so that the voltmeter reading is 0 ± 3mV.

24-2. Volume Adjustment

(1) Keep pressing "INITIALIZE" button, depress "DC01 WAVEFORM", "DC01 ENVELOPE", "DCW1 KEY FOLLOW", DCW1 ENVELOPE", DCA1 KEY FOLLOW" and "DCA1 ENVELOPE" buttons.

(2) Depress "DCW1 ENVELOPE" and then "END" buttons.

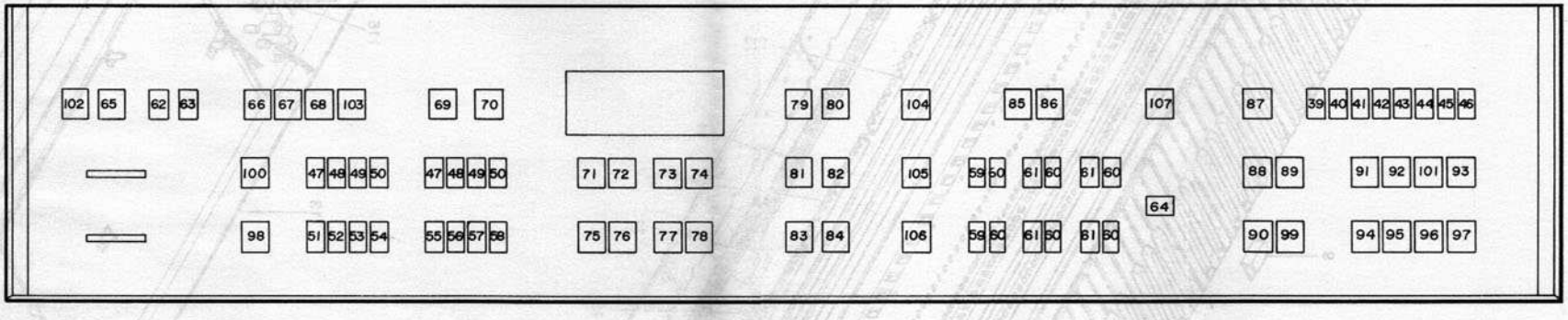
(3) Choose 1+1' by "LINE SELECT" button.

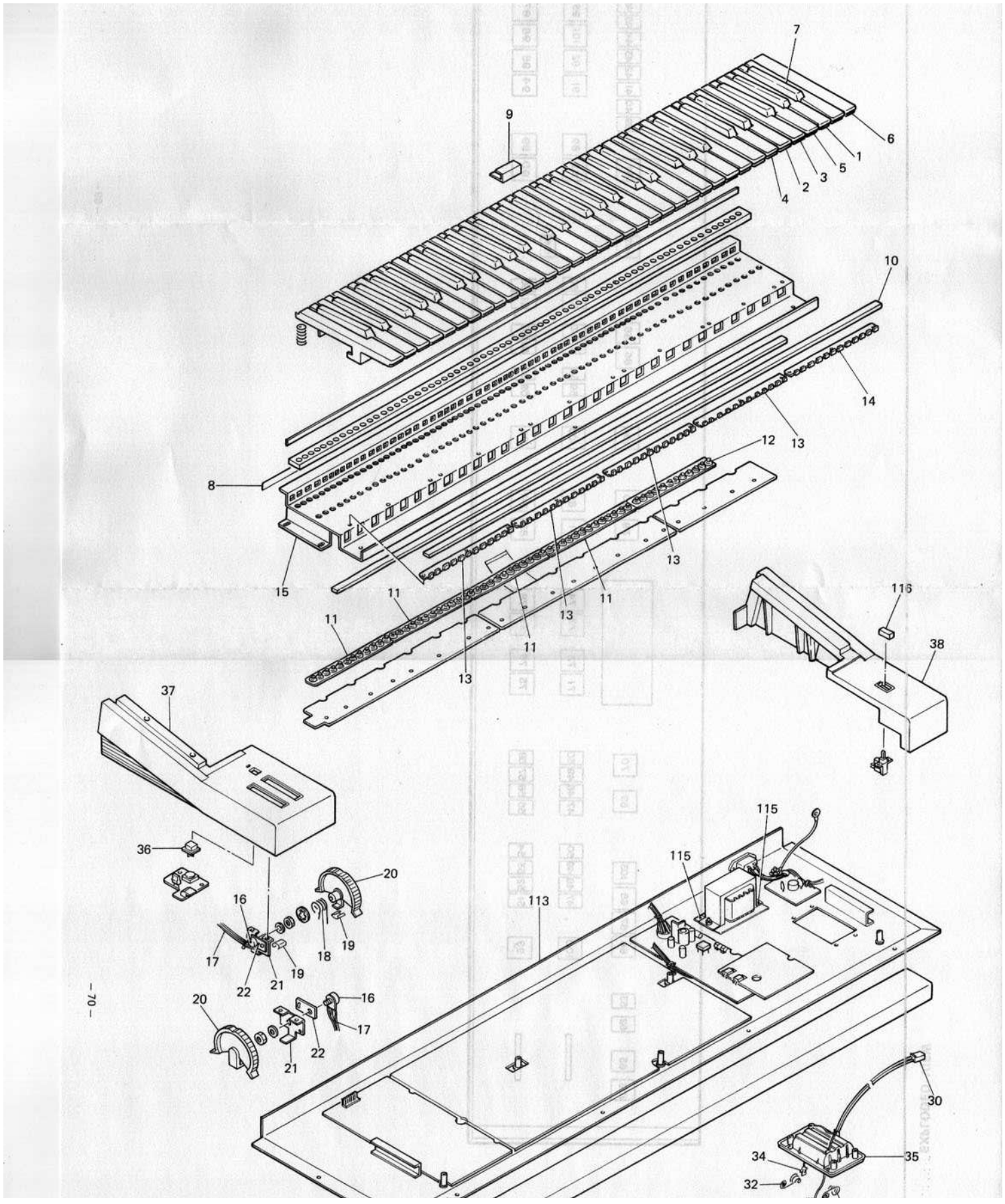
(4) Set the volume control to its maximum and the stereo chorus volume to its minimum.

(5) Connect a digital voltmeter between the ground and LINE-OUT terminal (either left or right output).

(6) Depressing a key, adjust 50K VR on the PCB M5153-AS1M so that the voltmeter reading is 360mV (510mV when an oscilloscope is used for checking the voltage).

EXPLODED VIEW

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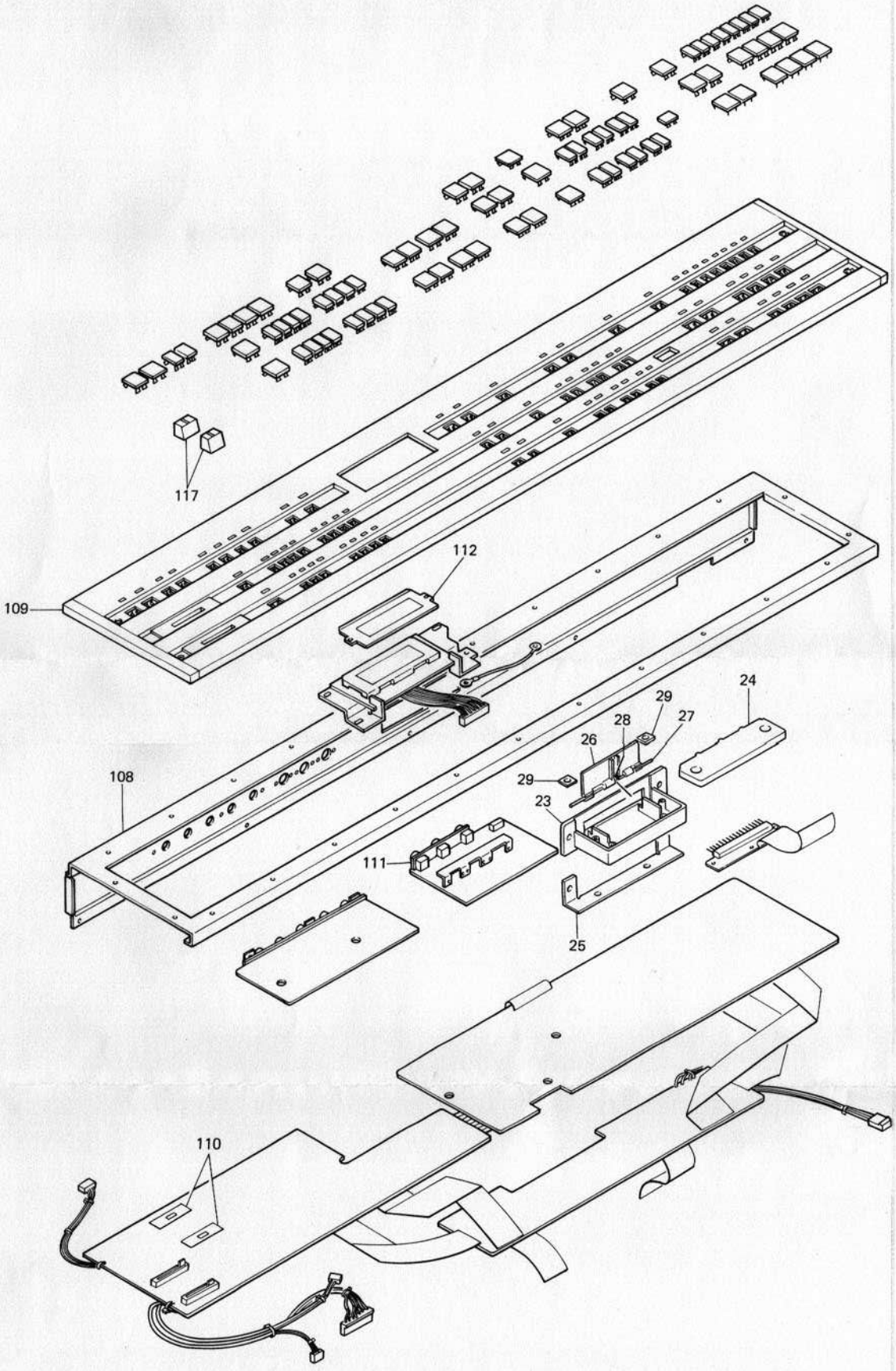
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