Type of Test or Adjustment	Input Signal and Load Parameters	Comments
13. Static Balance	No Signal No Load	Place the VZ Mode switches in the VZ-ODEP position (see Fig. 2.4). Measure ±VCC with respect to ground for channel 1. Values should be of equal magnitude and opposite polarity. If magnitudes vary by more than 500mV, adjust static balance pot R568 on the output module for null (no difference in magnitude). Switch to VZ (AUTO) position and verify null is maintained. Re-adjust only if necessary. Repeat check for channel 2, adjust if necessary.
14. Compressor	1kHz Sine Wave 8 Ohm	With each channel loaded to 8 ohms, insert a 1kHz sine wave and increase level until the amplifier is well into clip. Place the compressor switches in SLOW position and check for non-clipped output. Move switches to FAST position and again verify non-clipped output. Return switches to OFF position.
15. Dynamic Balance	1 kHz Sine Wave 2.7 Ohm	With channel 1 loaded to 2.7 ohms, increase input to obtain slight clipping. Watching TP1 pin 10 (main error amp output) and TP1 pin 16 (Low Side error amp output), simultaneously on a dual trace oscilloscope, verify that the output of the Low Side error amp clips at least as much (or very slightly more) than the main error amp output, and clip peaks reach 12-13V peak. If necessary adjust the dynamic balance pot R566 on the channel 1 output module. Repeat test for channel 2 measuring TP2 pin 10 and TP2 pin 16. *Note: 2.7 Ohm load is attained by placing three 8 Ohm loads in parallel.*
16. Over-voltage	No Signal No Load	With the amplifier powered from a variac, increase line voltage to 12% above the line voltage for which the amplifier is wired. The amplifier should trip off at 10.5% to 11% above the line voltage for which it is wired. If it does not set line voltage to 10.5% high and slowly adjust R780 on the control module until the amplifier trips into protect mode. If adjustment is performed, retest new adjustment.
17. ODEP & VZ-ODEP	60 Hz Sine Wave 2 Ohm	For the following tests, the cooling fan blade must be stopped. To stop the fans turn off and unplug the amplifier. Lift fan wire connector from P729/P730. Turn the amplifier back on and continue testing. At the end of this test step turn the amplifier off, unplug it, and return the fan wires to the appropriate position (P729 or P730). Place the VZ mode switches in the AUTO position (see Fig. 2.4). With a 2 ohm load per channel and output voltage of 60VRMS 60 Hz to both channels, allow the heatsinks to heat up until the ODEP

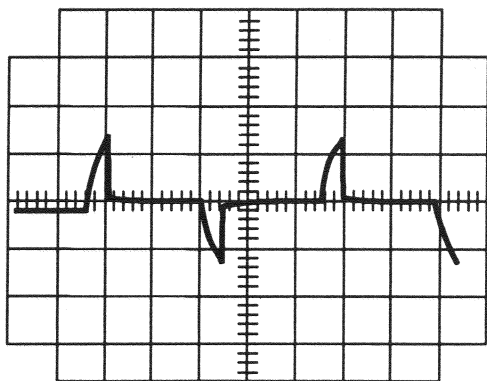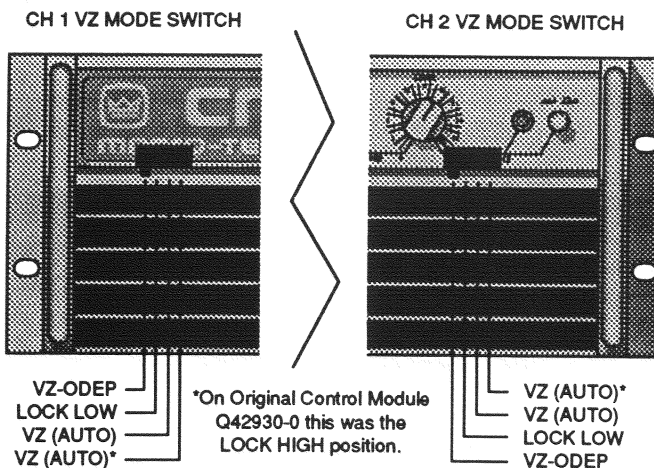| Type of Test or Adjustment	Input Signal and Load Parameters	Comments
		starts to limit the output signal (this should take a few minutes). A waveform like that in Fig. 2.3 below should be observed. Note: In VZ AUTO mode the flattened portion of the wave will probably not have the "clean" appearance of Figure 2.3, but should still resemble it. Check to see that the IOC LED is lit and that the ODEP LED dims and extinguishes when ODEP is activated. While ODEP limiting is taking place, switch the VZ mode switches to the VZ-ODEP position and verify that the amplifier locks into low voltage mode (the ODEP waveform should appear much more "clean"). Next configure the amp for parallel mono operation. With the input signal now present on channel one only, load channel one output with 8 ohms and channel two with 2 ohms. Observe that channel two ODEP protection circuit is limiting both channel one and channel two outputs. Next load channel one with 2 ohms and channel two with 8 ohms. Observe that channel one ODEP protection circuit is limiting both channel one and channel two outputs. Return the cooling fan blade to normal operation after this test has been completed, and allow a few minutes for the amplifier to cool with no signal input. Return all controls to initial conditions per section 2.3.1. *Correct operation of the ODEP circuit is dependent upon correct ODEP null settings (Step 6).*
18. Current Sense Balance	No Signal No Load	Place the Stereo/Mono switch in the PARALLEL MONO position. Measure the channel 1 hot output with respect to the channel 2 hot output. Verify null of less than ±10mVDC. If necessary adjust null via R2 current sense balance pot.

Fig. 2.3 ODEP Protection

CH 1 VZ MODE SWITCH　　　　　CH 2 VZ MODE SWITCH

VZ-ODEP
LOCK LOW
VZ (AUTO)
VZ (AUTO)*

*On Original Control Module Q42930-0 this was the LOCK HIGH position.

VZ (AUTO)*
VZ (AUTO)
LOCK LOW
VZ-ODEP

Fig. 2.4 VZ Mode Switch Locations

Type of Test or Adjustment	Input Signal and Load Parameters	Comments
19. Parallel Balance	1 kHz Sine Wave 8 ohm	Place the Stereo/Mono switch in the PARALLEL MONO position. Load each channel to 8 ohms separately, (loads must be precisely equal) and insert a 1 kHz sine wave. Adjust for 60VRMS output. Measure the channel 1 hot output with respect to the channel 2 hot output. Verify null of less than ±40mVAC with signal applied. If necessary adjust null via R4 parallel balance pot. Ensure Stereo/Mono switch is returned to STEREO upon completion of this check.
20. Current Sense Cal.	1 kHz Sine Wave 1 ohm	Factory set adjustment normally will not require recalibration. Perform this check as a verification, adjust only if the measurement is out of tolerance. With channel 1 loaded to 1 ohm, insert a 1 kHz sine wave and adjust for an output of 10VRMS, ±20mV. Measure TP1 pin 1 with respect to ground. Value should be 2VRMS ±10mV. If necessary adjust V/A cal pot R759 on the current sense module. Repeat test for channel 2 measuring TP2 pin 1; adjust R859 if necessary.
21. Current Limit Test	1kHz Sq. Wave 1 ohm	Note: The current limit check is performed as a part of the LED check in step 8. It is not necessary to repeat this check or perform more in depth checks as current limit circuitry is pretested when modules are manufactured. If a component affecting current limiting is replaced as a part of the repair, note that current limiting should occur at about 52-57VRMS into a 1 ohm load with a 1 kHz (20% Duty Cycle) square wave input.
22. 10 kHz Square Wave Slew Rate Test	10kHz Sq. Wave 8 ohm	With an 8 ohm load on each channel, insert a 10 kHz square wave and adjust amplitude to produce an output 10V below clipping (Fig. 2.4, following page). Observe a 30V/µS (or higher) slew rate. The output waveform should be stable with no ringing or overshoot.
23. DC/LFI	4 Hz Sq. Wave 8 ohm	Insert a 5Vpp 4 Hz square wave with an 8 ohm load on the output. The protection relay should cycle.

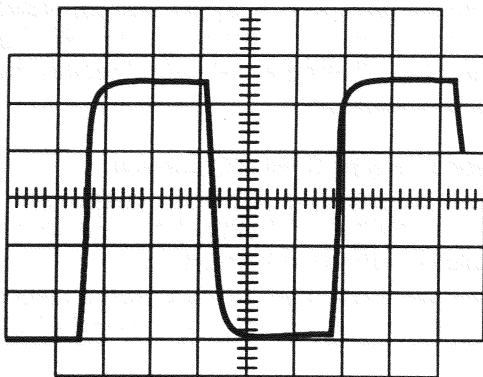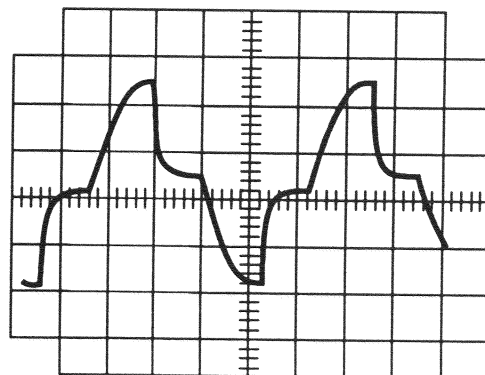| Type of Test or Adjustment	Input Signal and Load Parameters	Comments
24. 1kHz Power + THD	1 kHz Sine Wave Various Loads	Note: Operation with a sine wave into a low impedance load, when operating at AC voltages of less than 200VAC, will cause the 30A fuses to blow after 30 to 60 seconds. **AC Mains at 60Hz; or 230V, or 240V at 50Hz:** **8 Ohm Load:** Minimum voltage is 101.99VAC (1300W) with <0.05% THD. **4 Ohm Load:** Minimum voltage is 89.4VAC (2000W) with <0.05% THD. **2 Ohm Load:** Minimum voltage is 70.8VAC (2500W) with <0.05% THD. **AC Mains of 100-220V 50Hz:** **8 Ohm Load:** Minimum voltage is 101.99VAC (1300W) with <0.05% THD. **4 Ohm Load:** Minimum voltage is 86.0VAC (1850W) with <0.05% THD. **2 Ohm Load:** Minimum voltage is 69.3VAC (2400W) with <0.05%THD.
25. Inductive Load	1 kHz Sine Wave 8 ohm + Inductor	Insert a 1 kHz sine wave into both channels and adjust for approximately 36V into an 8 ohm load on the output. Connect a 163 microhenry inductive load (14AWG minimum), in parallel with an 8 ohm resistor, on the output of each channel and observe the output waveform. It should be similar to that in Fig. 2.6, below. Note: Under the conditions of this test, certain variations may be present in the waveform including flyback limiting.

Fig. 2.5 10kHz Square Wave

Fig. 2.6 Inductive Load

Type of Test or Adjustment	Input Signal and Load Parameters	Comments
26. I.M.D.	I.M. Signal Source 8 ohm	Place the sensitivity switches in the 26 dB position. Using a 60Hz/7 kHz input signal summed in a 4:1 ratio with the 60 Hz portion at 76.49V and 8 ohm loads on both channels, measure the I.M. distortion of each channel. Check in -5dB (power) steps until -35dB is reached (range is 1300W down to 0.41W). Readings should be less than .05% at each level.
27. Noise	No Signal No Load	Set the sensitivity switches to the 26dB position, level controls fully clockwise. Using a 20-20kHz bandpass filter on the input of the voltmeter, check that the noise level is 105dB below rated (1300W) output, with an 8 ohm load.
28. Crosstalk Check	1kHz Sine Wave 8 ohm	Set the sensitivity switches to the 26dB position. With each channel loaded to 8 ohms, insert a 1 kHz sine wave into channel 1 and adjust for 45V$_{RMS}$ output. Measure <25mV on the output of channel 2. Move signal from channel 1 to channel 2 (ensure channel 2 output is 45V$_{RMS}$) input and measure <25mV at the output of channel 1. There is not adjustment for crosstalk.
29. VZ Modes	1 kHz Sine Wave 8 ohm	*Note: VZ-ODEP mode was checked during the ODEP test, step 17. I.M.D. and 1 kHz power checks adequately tested the VZ (AUTO) mode. LOCK HIGH was (if present) checked adequately in the static balance adjustment check, step 13.* Place the VZ Mode Switches in LOCK LOW. With an 8 ohm load on each channel, insert a 1 kHz sine wave into each channel. Clipping should occur at approximately 36V$_{RMS}$ (410W).
Post-testing Procedure:		At the completion of testing, replace the 30A fuses (if testing was done at 100 - 120VAC, and set all switches per customer request. If none are specified by the customer, the following are standard factory settings for original shipment:

Dual Mono Switch: STEREO position.
Sensitivity Switches: Both to 1.4V position.
Compressor Switches: Both to FAST position.
LOI Switches: Both to ON position.
VZ Mode Switches: Both to VZ-ODEP position.
Level Controls: Both down (counter-clockwise) fully.

In most applications, VZ-ODEP is the best position for the VZ Mode switches for best thermal performance. |

3 Voltage Conversion

This Macro-Tech® 5000VZ™ power amplifier may easily be converted to a variety of AC mains voltages and may operate at 50 or 60 Hz. Complete directions to accomplish line voltage and/or frequency changes are found on a label placed under the top cover of the unit. For convenience this information is duplicated here and on the following page. Wiring lists and instructions are below with a graphic of the unit showing physical wire locations on the following page.

INSTRUCTIONS

CAUTION: Because there is a risk of electric shock, only a qualified technician should change the line voltage configuration.

1. Turn the amplifier off and disconnect it from the AC power source. (The enable switch alone does not remove lethal voltage from the line cord.) Wait at least 10 seconds before proceeding.

2. Drain any remaining energy from the power supplies by shorting them as follows: Touch a 100 ohm, 10 watt resistor across terminals A1 and A2 and across terminals B1 and B2 as shown in the illustration. The resistor should be held across the terminals for 10 seconds. **Be careful—the resistor can become hot.**

3. Locate the Control Board. It is the circuit board closest to the front of the amplifier. It contains numerous power supply connections which set the voltage and one jumper block which sets the frequency.

4. Use the information in the table at left to connect the color-coded wiring harness correctly for the desired voltage. Configure each wire group one at a time so the wires are not confused. **Do not mix wires between groups.** This step may require you to cut one or more tie wraps. If you do, replace them to make sure no loose wires are able to prevent the fans from rotating.

5. Locate the frequency jumper (JP1) and set it for either 60 Hz (left) or 50 Hz (right).

6. Double check that all connections are correct and replace the top cover.

NO**	100 V	120 V	200 V	208 V	230 V	240 V
Control Board Wiring for Different AC Voltages						
P712	BLK	BLK	BLK	BLK	BLK	BLK
P711	WHT	WHT	--NONE--	--NONE--	--NONE--	--NONE--
P724B	BLU*	BLU*	BLU*	BLU*	BLU*	BLU*
P707	BLK/GRN	BLK/YEL	BLK/GRN	BLK/GRN	BLK/YEL	BLK/YEL
P704	--NONE--	--NONE--	BLK/YEL	BLK/YEL	WHT	WHT
P705	--NONE--	--NONE--	WHT	WHT	BLK/GRN	BLK/GRN
P710	WHT/GRN	WHT/YEL	WHT/RED	WHT/YEL	WHT/YEL	WHT/YEL
P706	WHT/RED	WHT/RED	WHT/GRN	WHT/GRN	WHT/GRN	WHT/RED
P708	WHT/YEL	WHT/GRN	WHT/YEL	WHT/RED	WHT/RED	WHT/GRN
P703	BLK/YEL	BLK/GRN	--NONE--	--NONE--	--NONE--	--NONE--
P701	GRY	GRY	GRY	GRY	GRY	GRY
P700	GRY	GRY	GRY	GRY	GRY	GRY
P702	GRN/YEL	GRN/YEL	GRN/YEL	GRN/YEL	GRN/YEL	GRN/YEL
P713	BLK/YEL	BLK/GRN	--NONE--	--NONE--	--NONE--	--NONE--
P714	WHT/YEL	WHT/GRN	WHT/YEL	WHT/RED	WHT/RED	WHT/GRN
P722	BRN*	BRN*	BRN*	BRN*	BRN*	BRN*
P749	WHT/RED	WHT/RED	WHT/GRN	WHT/GRN	WHT/GRN	WHT/RED
P750	WHT/GRN	WHT/YEL	WHT/RED	WHT/YEL	WHT/YEL	WHT/YEL
P718	--NONE--	--NONE--	WHT	WHT	BLK/GRN	BLK/GRN
P716	--NONE--	--NONE--	BLK/YEL	BLK/YEL	WHT	WHT
P721	BLK/GRN	BLK/YEL	BLK/GRN	BLK/GRN	BLK/YEL	BLK/YEL
P719	BLK	BLK	BLK	BLK	BLK	BLK
P715	WHT	WHT	--NONE--	--NONE--	--NONE--	--NONE--
P724A	BLU*	BLU*	BLU*	BLU*	BLU*	BLU*
P736	GRN/YEL	GRN/YEL	GRN/YEL	GRN/YEL	GRN/YEL	GRN/YEL
P735	GRY	GRY	GRY	GRY	GRY	GRY
P734	GRY	GRY	GRY	GRY	GRY	GRY
P742	BLK/YEL	BLK/GRN	--NONE--	--NONE--	--NONE--	--NONE--
P737	WHT/YEL	WHT/GRN	WHT/YEL	WHT/RED	WHT/RED	WHT/GRN
P744	WHT/RED	WHT/RED	WHT/GRN	WHT/GRN	WHT/GRN	WHT/RED
P743	WHT/GRN	WHT/YEL	WHT/RED	WHT/YEL	WHT/YEL	WHT/YEL
P738	--NONE--	--NONE--	WHT	WHT	BLK/GRN	BLK/GRN
P739	--NONE--	--NONE--	BLK/YEL	BLK/YEL	WHT	WHT
P745	BLK/GRN	BLK/YEL	BLK/GRN	BLK/GRN	BLK/YEL	BLK/YEL
P724C	BLU*	BLU*	BLU*	BLU*	BLU*	BLU*
P741	WHT	WHT	--NONE--	--NONE--	--NONE--	--NONE--
P740	BLK	BLK	BLK	BLK	BLK	BLK
P729*** P730***	120 V Position		240 V Position			

Group labels: GROUP 1 (P712–P702), GROUP 2 (P713–P724A), GROUP 3 (P736–P740)

*Wire colors marked with a single asterisk connect to the power cord.
**The connector numbers are listed in clockwise order from left to right as you face the front of the amplifier.
***Connection P729 and P730 are combined on a single four-pin connector. It mates to a "120 V" connector for 100 or 120 V operation or a "240 V" connector for 200, 208, 230 or 240 V.

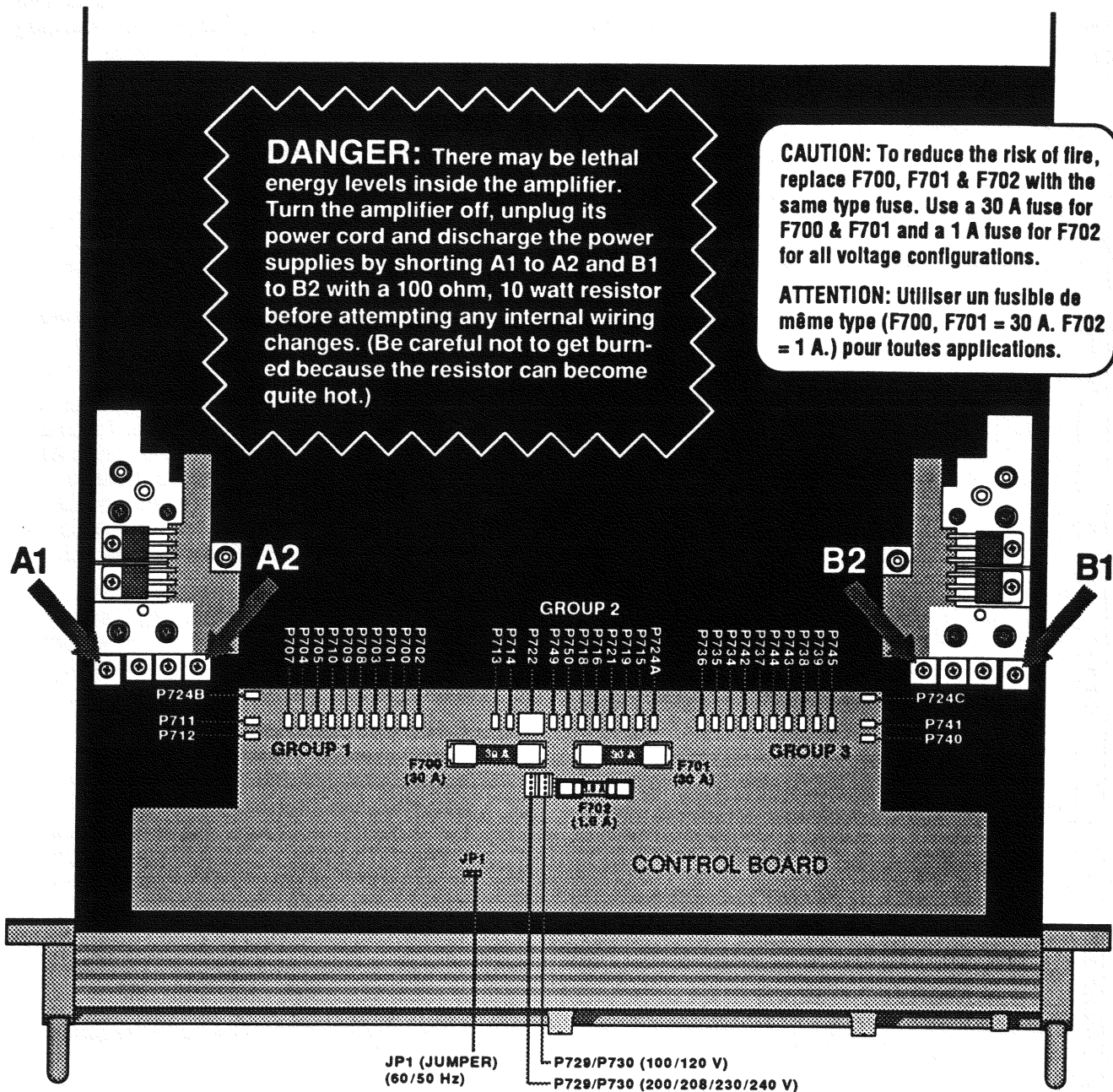*Fig. 3.1 Voltage/Frequency Conversion Chart*

DANGER: There may be lethal energy levels inside the amplifier. Turn the amplifier off, unplug its power cord and discharge the power supplies by shorting A1 to A2 and B1 to B2 with a 100 ohm, 10 watt resistor before attempting any internal wiring changes. (Be careful not to get burned because the resistor can become quite hot.)

CAUTION: To reduce the risk of fire, replace F700, F701 & F702 with the same type fuse. Use a 30 A fuse for F700 & F701 and a 1 A fuse for F702 for all voltage configurations.

ATTENTION: Utiliser un fusible de même type (F700, F701 = 30 A. F702 = 1 A.) pour toutes applications.

JP1 (JUMPER) (60/50 Hz)

P729/P730 (100/120 V)
P729/P730 (200/208/230/240 V)

Fig. 3.2 Voltage/Frequency Conversion Physical Layout

4 Circuit Theory

4.1 OVERVIEW

Note: Sketches have been added to this section for clarification of the various concepts presented, as well as block diagrams for the amplifier and specific portions of the amplifier. For detailed schematics refer to section 6.

The Macro-Tech 5000VZ amplifier incorporates several new technological advancements including real-time computer simulation of output transistor stress, low-stress output stages, an advanced heat diffuser embodiment, a programmable input processor (P.I.P.) expansion system, and articulated VZ power supplies. Custom circuitry is incorporated to limit temperature and current to safe levels—making it highly reliable and tolerant of faults. Unlike many lesser amplifiers, it can operate at its voltage and current limits without self-destructing.

Real-time computer simulation is used to create an analog of the junction temperature of the output transistors (herein referred to as the output devices). Current is limited only when the device temperature becomes excessive—and just by the minimum amount necessary. This patented approach, called ODEP® or Output Device Emulation Protection, maximizes the available output power and eliminates overheating—the major cause of device failure. ODEP, in the MA-5000VZ, also provides indication of amplifier thermal reserve (front panel ODEP indicators) and may provide control of VZ mode when the VZ mode select switches are placed in the VZ-ODEP position.

The amplifier is protected from all common hazards that plague high-power amplifiers, including shorted, open or mismatched loads, overloaded power supplies, excessive temperature, chain-destruction phenomena, input-overload damage, and high-frequency blowups. The unit protects loudspeakers from DC in the input signal and from turn-on and turn-off transients. It also detects and prevents unwanted DC on the outputs. Additional protection features include input voltage sense, overvoltage (AC mains).

A mode of protection which may be switched on or off is called Loudspeaker Offset Integration (LOI). The LOI circuit, when switched on, prevents excessive bass frequency cone excursions below the audible frequency range. It operates essentially as a bandpass filter. The low frequencies are rolled off at 18dB/octave with a -3dB corner of 35 Hz (Butterworth response). Ultra-sonics are rolled off with a second order Bessel response and -3dB corner of 50kHz.

A compression circuit in each channel may be switched off, on slow, or on fast by switches on the rear panel. This compressor is activated by either input overload or distortion (clipping). Input overload compression is in fast speed when compressor switch is in off position. Compression ratio is infinite (operates as a peak limiter).

The four-quadrant topology used in the grounded output stages is called the grounded bridge and makes full use of the power supplies. This patented topology also makes peak-to-peak voltages available to the load which are twice the voltage any output device is ever exposed to. The grounded bridge is covered in detail in section 4.2.

The two channels may be used together to double the voltage (bridged-mono) or the current (parallel-mono) presented to the load. This feature gives the user flexibility in maximizing the power available to the load.

Macro-Tech amplifiers utilize a wide bandwidth multiloop feedback design with state of the art compensation techniques. This produces ideal behavior and results in ultra-low distortion values.

Aluminum extrusions have been widely used for heatsinks in power amplifiers due to their low cost and reasonable performance. However, measured on a watts per pound or watts per volume basis, that extrusion technology doesn't perform nearly as well as the cut fin radiator technology developed for Macro-Tech 5000VZ power amplifier.

Our thermal diffusers are custom cut radiator fins on a solid heat sink block. They provide an extremely high ratio of area to volume, or area to weight. All power devices are mounted directly to massive heat spreaders, which are electrically hot. Making the heat spreaders electrically hot allows improved thermal performance by eliminating the insulating interface underneath the power devices. The chassis itself is used as part of the thermal circuit, and this maximizes utilization of the available resources.

Simplified Grounded Bridge... In Operation
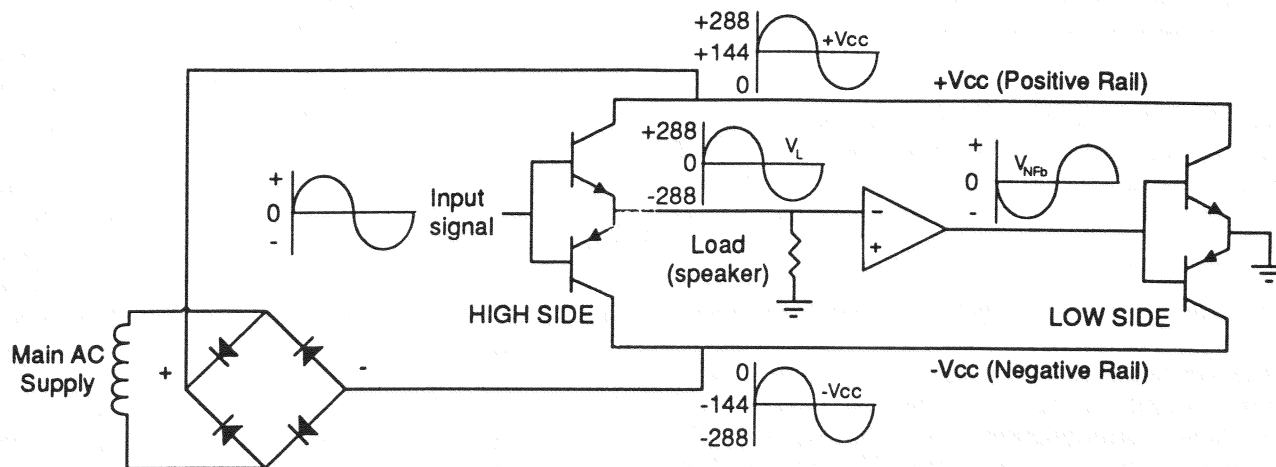### (MA-5000VZ with supply in high voltage mode)

Fig. 4.1 Simplified Grounded Bridge

4.2 GROUNDED BRIDGE THEORY

The Grounded Bridge topology is ground-referenced by the output stages rather than the power supply. Composite devices are constructed to function as gigantic NPN and PNP devices since the available currents exceed the limits of existing individual devices.

The devices connected to the load are referred to as "high-side NPN and PNP" and the devices connected to ground are referred to as "low-side NPN and PNP." Positive voltage is delivered to the load by increasing conductance simultaneously in the high-side NPN and low-side PNP stage, while decreasing conductance of the high-side PNP and low-side NPN in synchrony.

4.2.1 Grounded Bridge Operation

Fig. 4.1 is a *simplified* example of Crown's patented Grounded Bridge output topology (ignoring the articulating characteristics of the VZ supply). It consists of four quadrants of three deep Darlington (composite) emitter-follower stages per channel: one NPN and one PNP on the high side of the bridge (driving the load), and one NPN and one PNP on the low side of the bridge (controlling the ground reference for the rails). The output stages are biased to operate class AB+B for ultra low distortion in the signal cross-over region.

The high side of the bridge operates similar to a conventional bipolar push-pull output configuration.

As the input drive voltage becomes more positive the high side NPN conducts current and delivers positive voltage to the speaker load. Eventually full +Vcc is across the load. At this time the high side PNP is biased off. When the drive signal is negative going the high side PNP conducts to deliver -Vcc to the load and the high side NPN stage is off.

The low side operates quite differently. The power supply bridge rectifier is not ground referenced. This allows the power supply to deliver +Vcc and -Vcc from the same bridge rectifier and filter as a total difference in potential, regardless of their voltages with respect to ground. The low side of bridge uses inverted feedback from the high side output to control the ground reference for the rails.

As the output swings positive the output signal is fed back to the low side and is inverted to drive the low side with a negative signal. The negative signal causes the low side PNP to conduct (as the high side NPN conducts) shifting the ground reference to toward -Vcc until, at the peak, -Vcc = 0V. At this time +Vcc equals the full potential (from rail to rail, not rail to ground) of the power supply with positive polarity. Since the high side is delivering +Vcc to the speaker load (which is ground referenced at all times), the speaker sees the full potential developed by the power supply with a positive polarity.

When the input drive signal is negative and the high side PNP conducts to deliver a negative voltage to the

load, that output is again fed to the low side and inverted to cause the low side NPN to conduct. As the low side NPN conducts, +Vcc swings toward the 0V ground potential. At the peak: +Vcc = 0V. At this time -Vcc equals the full potential developed by the power supply, but with negative polarity. Since the high side is delivering -Vcc to the speaker load, the load sees the full (negative) potential developed by the power supply.

The total effect is to deliver a peak to peak voltage to the speaker load which is twice the (static) voltage produced by the power supply. Benefits include full utilization of the power supply (it conducts current during both halves of the output signal; conventional designs require two power supplies per channel, one positive and one negative), and never exposing any output device to more than half of the peak to peak output voltage (which does occur in conventional designs).

4.2.2 Output Stage Circuitry

Circuitry on the positive and negative output modules include bias circuitry, current limit circuitry, last voltage amplifiers (LVA's), pre-drivers, drivers, output devices, and the Low Side error amp. Temperature sensors are also mounted to the heatsinks via the output modules.

The positive LVA's (Q501, Q502, and Q503) convert the negative output of the voltage translator stage to a positive drive voltage for the NPN High Side (HS) predriver. There are three LVA transistors in parallel due to the very high voltages (therefor higher current and thermal requirements) that are present when the power supply is in high voltage mode. D522 prevents the +LVA's from producing a high negative output to the HS NPN stage.

Q507, Q508, and Q509 are the -LVA's and are arranged in mirror image to the +LVA's, including D513.

On the positive side D514, D515, and C506 via the +LVA's act to limit slew rate. D514 and D515 also prevent dangerously excessive current through the LVA's. D516, D517, and C507 are the negative HS mirror image.

Q534 and Q540 provide two-speed current limiting in the output stage. Sense lines are arranged such that excessive current through any single HS output device will result in current limit protection. Q535 and Q541 are the negative side mirror image.

Q505 on the positive output module works in tandem with Q505 on the negative output module as a Vbe multiplier circuit. They produce and, with great stability, control bias for the High Side NPN and PNP devices. Potentiometer R505 is used to precisely set bias voltage. Bias voltage is easily measured from pin 2 (hot) to pin 4 of ATE ports TP1 and TP2. Refer to section 2 for appropriate test procedures.

Q504 is the HS NPN pre-driver and Q511 is the HS NPN driver. These devices are biased class AB for ultra low distortion in the zero-crossing region.

Q513, Q515, Q517, and Q536 are the HS NPN output devices. These devices are biased class B, in soft cut-off. Together with driver and pre-driver, they function as a three-deep darlington. The output devices work in parallel as a giant composite. The over-all bias topology is referred to as AB+B, originally conceived and patented by Crown engineers in 1966. This is still the most efficient, stable, and distortion free method used today.

D506 is the flyback diode for the HS NPN output quadrant. In the event that a back EMF (flyback) pulse exceeds power supply voltage, the flyback diode will shunt this voltage to the supply in order to protect the output devices.

PNP pre-drivers, drivers, output devices, and flyback diode D508 are a mirror image of the NPN side.

Overall the High Side of bridge operates much like a conventional output stage, but the Low Side (LS) is quite unique.

The LS senses output voltage and common buss (0.04 ohms above ground) potential. The audio output is inverted by U503. Also in the U503 input circuitry are static and dynamic balance controls. These controls provide a fine balance of the grounded bridge. Output of the op-amp drives the LS pre-driver circuits through the LS bias network.

LS bias is controlled in a fashion similar to that of the HS. Two transistors, Q529 and Q530, along fix LS bias voltage as measured from pin 15 (hot) to pin 13 of applicable ATE port TP1 or TP2. Potentiometer R556 adjusts bias in the LS.

Diodes D504 and D505 control polarity of applied LS drive signal. Via the bias transistors signal is delivered to the bases of the pre-drivers Q527 (NPN) and Q528

(PNP). Pre-drivers, drivers, and output devices in the LS operate class AB+B, exactly like the HS. The major difference is that rather than driving a load, the NPN and PNP stages control the ground reference for the high voltage rails. As the HS NPN's conduct, LS PNP's conduct, and vice versa (as explained in section 4.2.1).

When the ODEP circuit senses that limiting drive is necessary to prevent a dangerous thermal condition, it provides an output which limits drive to the output stages. For the HS, this limiting is accomplished on the main module and is explained in section 4.4. For the LS, ODEP provides (via wires labeled ±LL) a signal which limits bias feed to the LS output devices. This is accomplished through current mirrors Q532 and Q531 (LS NPN quadrant), and Q542 and Q543 (LS PNP quadrant).

4.3 VZ POWER SUPPLY

VZ means Variable Impedance and is the name of Crown's patented articulated power supply technology. It enables Crown to pack tremendous power into just 5.25 inches of vertical rack space.

A power supply must be large enough to handle the maximum voltage and current necessary for the amplifier to drive its maximum rated power into a specified load. In the process of fulfilling this requirement conventional power supply designs produce lots of heat, are heavy, and take up precious real estate. And it's no secret that heat is one of a power amplifiers worst enemies.

According to Ohm's Law, the bigger the power supply, the more heat the power transistors must dissipate. Also, the lower the resistance of the power transistors, the more voltage you can deliver to the load. But at the same time that you lower the resistance of the transistors, you increase the current passing through them, and again increase the amount of heat they must dissipate.

4.3.1 VZ Supply Operation

An articulated power supply, like VZ, can circumvent much of this problem by reducing the voltage applied to the transistors when less voltage is required. Reducing the voltage reduces the heat. Since the amplifier runs cooler, you can safely pack more power into the chassis.
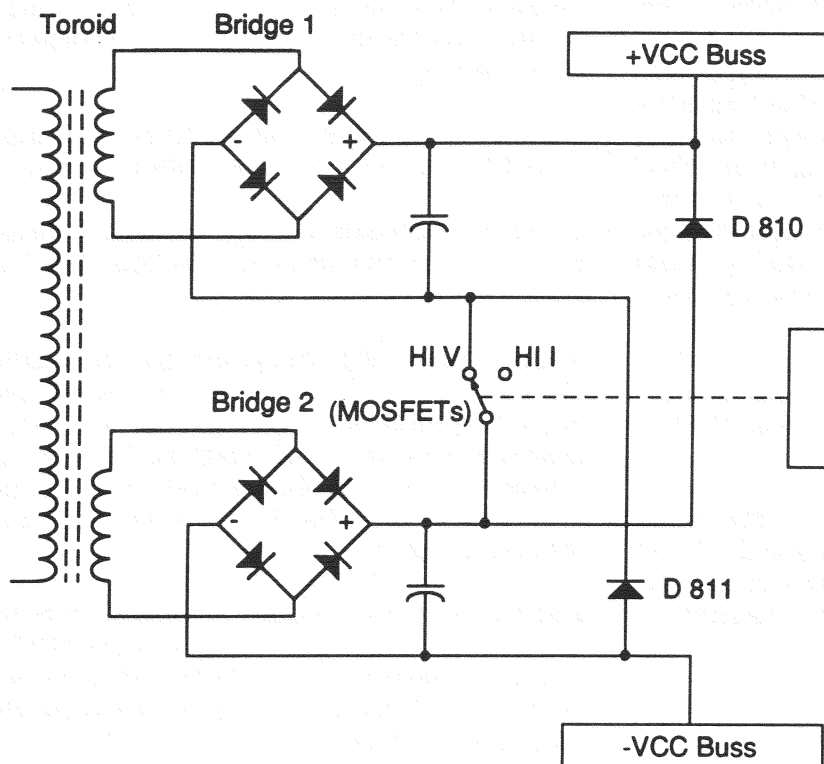
The VZ supply is divided into segments to better match the voltage and current requirements of the power transistors. Remember that audio signals like music are complex waveforms. Refer to Fig. 4.2 and 4.3.

For music the average level is always much less than the peak level. This means a power supply does not need to produce full voltage all the time.

The VZ supply is divided into two parts. When the voltage requirements are not high, it operates in a parallel mode to produce less voltage and more current.

The power transistors stay cooler and are not forced to

Fig. 4.2 Simplified VZ Supply Diagram

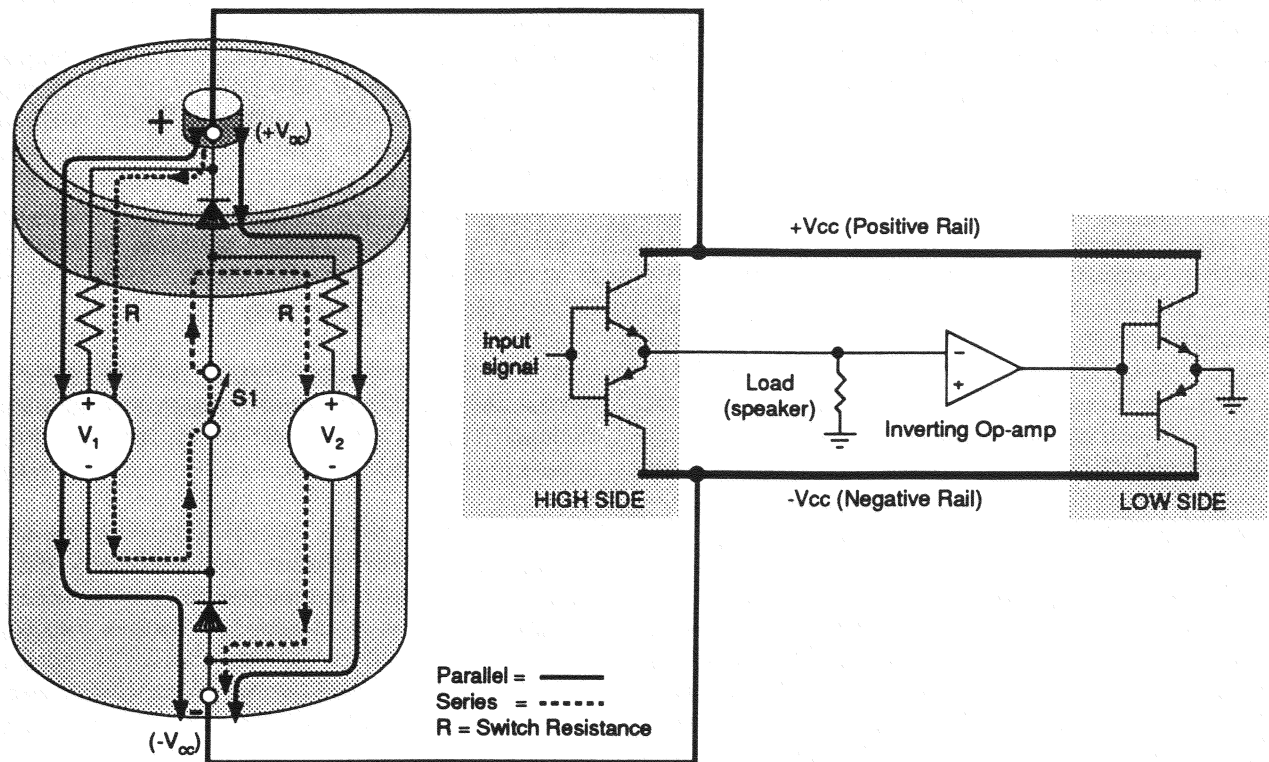# VZ Power Supply & Grounded Bridge Output Topology

Fig. 4.3 Simplified VZ Supply in Operation

needlessly dissipate heat. This is the normal operating mode of the VZ power supply.

When the voltage requirements are high VZ switches to a series mode to produce higher voltage and less current. The amplified output signal never misses a beat and gets full voltage when it needs it—not when it doesn't need it.

Sensing circuitry watches the voltage of the output signal to determine when to switch VZ modes. The switching circuitry is designed to prevent audible switching distortion to yield the highest dynamic transfer function — you hear only the music and not the amplifier. You get not only the maximum power with the maximum safety, you also get the best power matching to your load.

In Fig 4.2, the individual components are shown. Upstream of the toroid transformer, though not shown, is where shutdown protection and soft-start circuitry taps in to control AC mains input to the power supply.

The VZ Control circuitry senses audio level and switches the articulating VZ supplies to either parallel (high current) mode for lower level audio, or series (high voltage) mode for high program peaks.

Fig. 4.3 shows current flow with power supply and grounded bridge operating together. Notice that the ungrounded VZ supply operates much like a battery. More exactly, it is a floating DC supply made up of two internal batteries which operate in either series or parallel.

In both examples it can be seen that when the MOSFET switch is off, the dual supplies are forced to operate in a parallel mode. Audio level is sensed via a line tapping off the NFb loop. When audio level is rising and at about 80% of the parallel mode supply voltage, the MOSFETs (the switch is actually a three-device composite switch) are turned on. No current will flow through either of the control diodes (D810 and D811, as shown for channel 1) because reverse polarity is applied through the MOSFET switch. Since this

happens to both rectifier sources at the same time, and the negative side of Bridge 1 is then shorted to the positive side of Bridge 2, the supplies are forced to operate in series mode. Like two batteries, the supplies will provide double voltage in series mode, double current in parallel mode.

Although shipped from the factory in VZ-ODEP mode, the user may switch modes to Lock Low voltage (high current), or operate the supply in VZ-AUTO mode. VZ-ODEP is similar to VZ-AUTO mode, except that in the event ODEP is activated to protect the amplifier, the VZ will automatically lock into low voltage (high current) mode. While this mode of operation will cool the amplifier more quickly in the event that the thermal reserve is exhausted, it may cause voltage clipping rather than ODEP limiting. Seldom will the amplifier be operated locked in high current mode unless a very low impedance is being driven.

4.3.2 VZ Supply Circuitry

For simplicity, only channel 1 circuitry will be covered unless noted otherwise. The actual VZ switch circuit is located on the VZ switch assembly. In this assembly are the filter capacitors, MOSFET switches, and control diodes (D810 and D811). Three MOSFETs are used in parallel for sharing the high current supplied to the rails. Operation of this section was covered in detail, minus circuit designations, in section 4.3.1.

WARNING: From a service standpoint, it is critical to note that VZ switch control circuitry is NOT ground referenced. Any attempt to take voltage measurements using a ground reference when voltage is applied will not only be unreliable, but may be extremely dangerous. Serious damage to equipment or personnel may occur if this is attempted.

The output of a 555 timer (U703) on the control module determines whether the MOSFETs are switched on (high) or off (low). This 555 device and the various sources that feed the 555 are the things that make the articulation work.

The master 555 trigger is controlled by the output of U702A. S700, physically accessible from behind the front grille, determines the VZ operating mode. In high voltage mode (Q42930-0 Control Module only) the output of U702A is held low. This in turn keeps the 555 output high and the MOSFETs are kept on. In the high current mode U702A is held in the opposite polarity keeping the output of the 555 low and the MOSFETs off. In the AUTO position of S700, the audio level

sense circuitry controls the threshold and reset inputs to the 555. The 555 will then switch states to high voltage when the audio level is sufficient and will switch back down automatically when level has dropped sufficiently. Capacitors in the U705 circuitry control the speed of the down-shift. In the VZ-ODEP mode, the switch operates as it would in AUTO mode unless ODEP limiting is in progress. When ODEP limiting occurs, optic coupler U704 pulls the reset control low to the 555 to turn the MOSFET switches off, and keep them off (low voltage/high current mode) until the ODEP limiting condition clears.

Upstream of the toroids are the soft-start and protection mechanisms used to power down the amplifier. Although tied into the power supply primary, these circuits are covered in section 4.6, Protection Systems.

The low voltage power supply utilizes a separate transformer. The front panel power switch and a 1A fuse (F702) are the only components upstream of this transformer. The output of the rectifier produces ±24VDC unregulated. U715 and U716 produce regulated ±15VDC respectively. (A separate fullwave rectifier produces pulsed DC for Over-voltage sense and Soft-start control.)

4.4 ODEP THEORY

To protect the output stages from adverse thermal conditions, a specially developed "ODEP" (Output Device Emulator Protection) circuit is used. It produces a complex analog output signal proportional to the always changing safe-operating-area (SOA) margin of the output transistors. This output signal controls the Voltage Translator stage and Low Side output stage bias. This action removes only the drive that may exceed the safe-operating-area of the output stage.

Thermal sensors give the ODEP circuitry vital information on the operating temperature of the heat sinks on which the output devices are mounted. This temperature signal combines with the complex ODEP signal to form the heart of our patented ODEP protection scheme.

4.4.1 ODEP Operation

Refer to Fig. 4.4. for a discussion of the basic operation of the ODEP system.

The ODEP circuitry actually comes in two parts, one positive and the other negative. For the purposes of

discussion, only channel 1 ODEP circuitry is covered here, and focus will primarily be on the positive half.

An LM-334Z thermal sensor provides a calibrated output from the output modules. At 25°C its output is 2.98V, with a 10mV increase per every 1°C rise in heatsink temperature.

This thermal sensor output, from the positive sensor, goes to three destinations. First is a buffer which drives the calibrated temperature test point at pin 7 of TP1/TP2. Second is an over-temperature limit trip (thermal limit amplifier, as shown below). This will cause both the positive and the negative ODEP circuit to go into and remain in hard ODEP until the heatsinks cool. Third, it goes down into a circuit which combines thermal and output power information.

The thermal sensor from the negative output module only performs this last function.

Channel 1 ODEP Circuitry shown (channel 2 is identical)

ODEP Inputs:
Temperature
±VCC
Output Current

ODEP Outputs:
Calibrated Temperature, for monitoring
±ODEP Level, for monitoring
±ODEP Level, for Bi-ODEP control of VZ Supply
±ODEP Level, to limit drive at ±Voltage Translators (±LH)
±ODEP Level, to limit Low Side Bias (±LL)
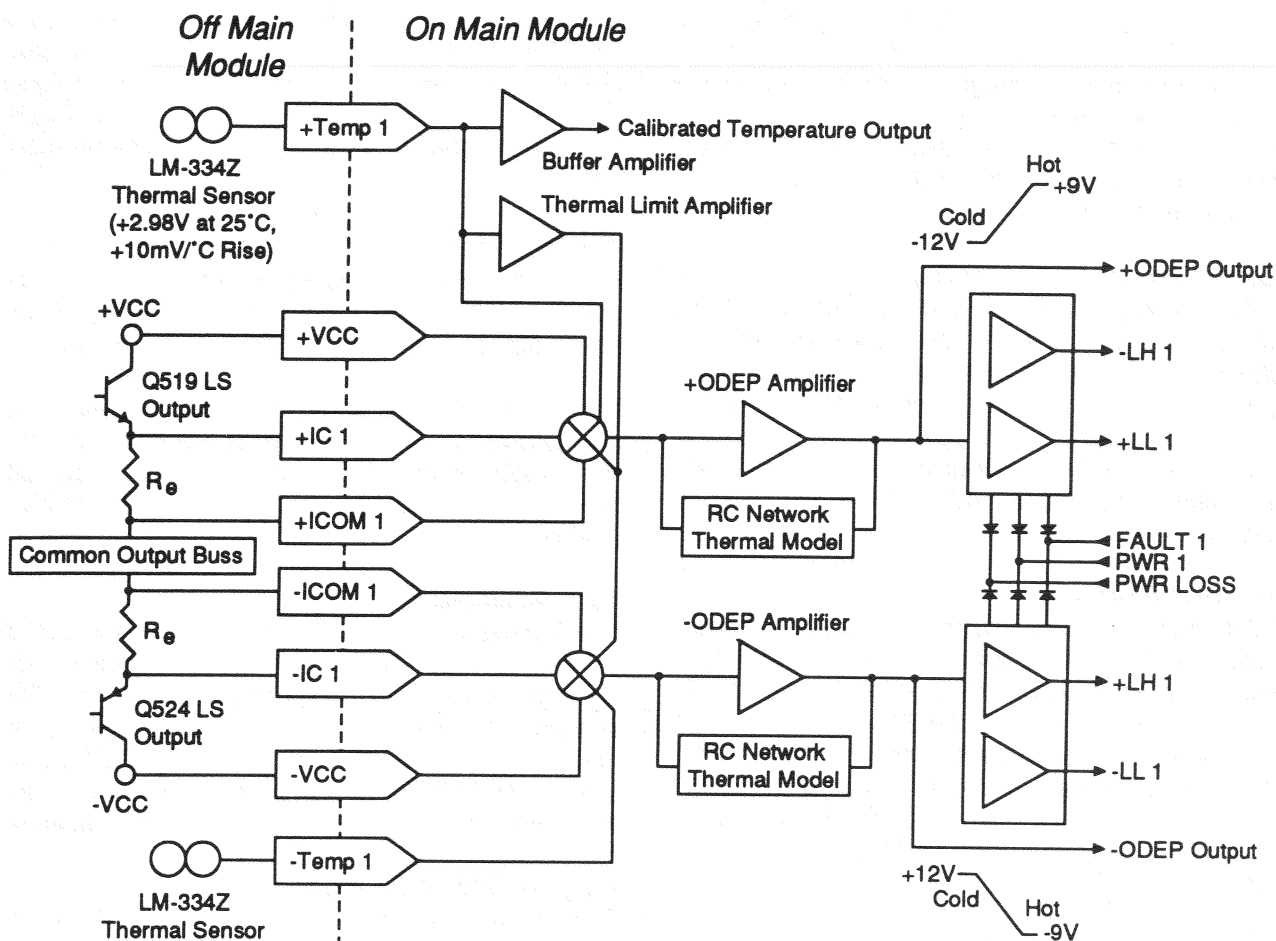ODEP Indication (front panel LEDs)

Fig. 4.4 Simplified ODEP Circuitry

A pair of sense lines from the Low Side emitter resistors provide current information. Combined with VCC information actual instantaneous power is calculated. A combining circuit determines the net thermal condition based on the power being delivered for the existing heat level. The ODEP amplifier accepts this input information and, using an RC model of the heat transfer characteristics of the output devices (as mounted in the heatsinks), creates a complex output proportional to the thermal reserve of the output devices.

Output from the positive ODEP amplifier ranges from -12V (cold) to +9V (hard ODEP). This output drives the positive LS bias feed control circuit (see section 4.2.2) and the negative HS Voltage Translator feed control circuit (see section 4.5.2). Also, this circuit provides test point monitoring information and VZ-ODEP VZ mode control information.

Output from the negative ODEP amplifier ranges from +12V (cold) to -9V (hard ODEP). This output drives the negative LS bias feed control circuit (see section 4.2.2) and the positive HS Voltage Translator feed control circuit (see section 4.5.2). Also, this circuit provides test point monitoring information, VZ-ODEP control information, and front panel ODEP (thermal reserve) LED control information.

Also tapping in to the ODEP output control of LS bias feed and Voltage Translator feed are signals from the fault, power (turn-on delay), and power loss (brown-out) circuits. By using the output of ODEP for ±LL and ±LH control, these sources can mute the audio to the output stage: a. until power-up delay has timed out; b. immediately upon indication of any failure mode; c. and immediately upon loss of AC mains (power-down or actual loss of AC service).

4.4.2 ODEP Circuitry
±TEMP signals are produced by U500 and U501 on the output modules. U108, on the main module, is a buffer which drives the temperature sense test point. U117A has a fixed window voltage of 6.2V via Zener D129. If heatsink temperature level exceeds about 130°C U117A output will cause both the positive and negative ODEP amplifiers to go into hard ODEP limiting. When the thermal condition clears this limiting condition will also clear.

+VCC enters via dual PNP transistor pack U116. Positive ODEP bias is adjusted by R182. The voltage at that point controls the static balance of the U116

device. U116 combines the VCC and output current sense information, the output of which represents output power level. The common output is brought into RN101 where it provides the reference for temperature and power. U112B is the active device and, together with the power signal, drives the ODEP amplifier U112A. The RC network in the feedback path of U112A models the thermal junctions from output device die to housing, housing to case, and case to heatsink under both static and dynamic conditions.

The output of the positive ODEP amplifier drives +ODEP test point pin 11. It also drives U114A and U114B which in turn drive -LH and +LL respectively. The output of the negative ODEP amplifier drives the ODEP indication circuitry and -ODEP test point pin 9. Negative ODEP also drives U114C and U114D which in turn drive +LH and -LL respectively.

Also entering the U114 comparator networks are the PWR (power relay engage), PWRLOSS (brown-out), and FAULT (any protection which shuts down the amplifier) signals via blocking diodes. If any of these signals drop low the feed to LS bias and Voltage Translator drive will be shut down via ±LL and ±LH. This action mutes all audio in the event of a dramatic failure.

4.5 FRONT END THEORY
Fig. 4.5 on the following page explodes the front-end portion of the over-all block diagram (Fig. 4.). Once again, only channel 1 will be discussed in detail.

Input to the amplifier is only via P.I.P. module. The standard module shipped with the MA-5000VZ is the P.I.P.-FXQ. Whether this or any other module is used, the amplifier senses a balanced input from the installed module.

4.5.1 Balanced Gain Stage
The Balanced Gain Stage (BGS) amplifier U100A converts the input audio from a balanced configuration to single-ended with (electrically) unity gain. The compression device is essentially a resistive shunt across the balanced BGS input. The BGS drives the Variable Gain Stage and provides information to the compressor control circuit and to the P.I.P. connector.

4.5.2 Variable Gain Stage
The Variable Gain Stage (U100B) taps signal from the wiper of the front panel level control (R120). Gain of the front-end is set by the gain of this stage. The sensitivity switch (S100, located on the rear panel) selects the
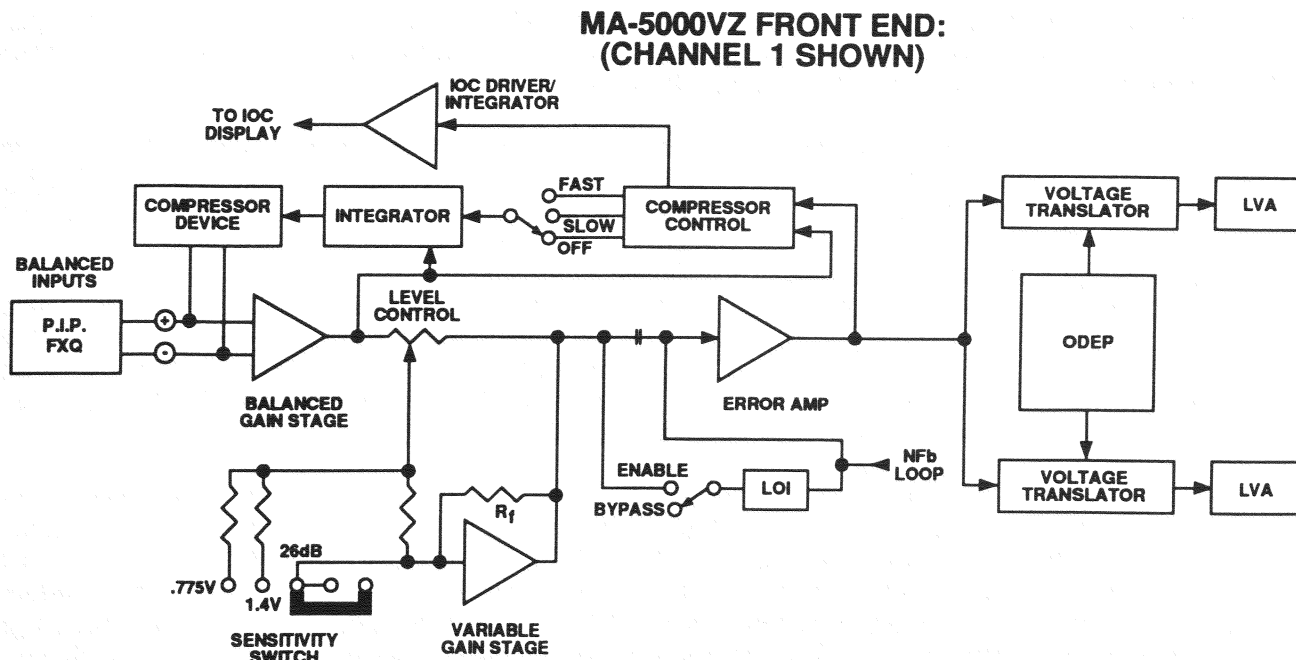
MA-5000VZ FRONT END:
(CHANNEL 1 SHOWN)

Fig. 4.5 Front End Circuitry Block Diagram

amount of gain in this stage. Overall amplifier sensitivity may be set for 26dB fixed gain (about 5.1VRMS), 1.4V, or 0.775V. Since overall amplifier gain after this stage is 26dB, this stage will have a fixed gain of 0dB (26dB setting), about +12dB (1.4V setting), or about +16dB (0.775V setting). The output of this stage drives the Error Amp.

4.5.3 Error Amp
The Error Amp (U105) input comes from the Variable Gain Stage with or without Loudspeaker Offset Integration (LOI), and is summed with amplifier output in a negative feedback (NFb) configuration. Output of the Error Amp drives the Voltage Translators and provides error signal information.   An error signal (spike) is produced any time the shape of the output waveform differs from the output of the Variable Gain Stage and LOI by more than 0.05%. This error signal drives the error signal (ES) input to the P.I.P. connector, the error signal sense test point, and the compression control circuit.

4.5.4 Compressor
The compression circuitry senses error signal and BGS level. If the BGS overloads, or an error signal is present, the compression control circuit (U101) produces a compression drive pulse. A switch on the rear panel selects speed of the integrator circuit to follow. In the off position the error driven compression

is disabled, but the input overload compression remains on (in fast speed) to protect the front end. The compression drive pulse also drives the IOC Integrator (U102). The IOC integrator not only tells the IOC indicator circuit when to turn on, but ensures that the indicator will remain on long enough to be visible to the human eye.

The compression integrator (U102, Q100) sets compression speed and produces an output pulse which controls attack and decay times. An optic device (U103) provides a resistive shunt to the input audio according to the degree of compression required and the duration of that compression. The amplifier input impedance is not affected by compressor operation.

4.5.5 Loudspeaker Offset Integration
LOI (U104A/B) senses amplifier feedback and prevents dynamic DC offset. It operates essentially as a dual filter system with band pass from about 35 Hz to about 50kHz. The upper roll-off has a second order Bessel response while the lower roll-off has a third order Butterworth response.

4.5.6 Voltage Translator and LVA Stages
The Voltage Translator stages (Q104, Q104) channel the signal to the Last Voltage Amplifiers (LVA's, located on the output modules), depending on the signal polarity, from the error amp U105. The ±LVA's, with