Type of Test/Adjustment	Input Signal Characteristics	Comments
Multiplier Balance	C. 100Hz sine wave; variable (no load)	C. This adjustment must be made **if and only if** the protection circuitry (steps 11A, B) is not functioning properly. Apply the input signal to full output (without a load) without clipping the signal. Adjust R124 and R224 for minimum signal null at test pins 1, 2, 3 and 4 on main board module (scope should be set at 100mV for proper viewing). Repeat steps 11A, B; proceed to step 11D.
Temperature Computer	D. 10Hz sine wave; 30V output level with 4 ohm load	D. Measure the AC voltage across C112, C212, C113, C213, C114 and C214 with a true RMS meter. This may be done by measuring across the proper pins of RN103, RN203 (see schematic). Across: C112/C212 measure .4VAC ±10% C113/213 measure 1.7VAC ±10% C114/214 measure .036 ±10% If these measurements cannot be obtained, a problem exists in the thermal computer circuitry.
12. Anti-pop Circuit (earlier PSA-2/ SA units have this circuit on separate module. Later amps include this circuit on Main Module).	1KHz sine wave; 2V no load	Observe the output of pins M and U on the Main Module while turning the unit on and off several times. A spike should be noticable upon each turn-on. Observe the signals at the output terminals. They should not exhibit any spike during turn-on.
13. Display Module (PSA-2/PSA-2X)	A. 1KHz sine wave; variable no load	A. Increase input level until the green "Signal" presence indicators illuminate. The voltage level should be approximately 1.2 volts peak at the output. Connect an oscilliscope to the amplifier output. Again raise the input level to the point just before clipping is observed. Note the IOC indicators; they should illuminate prior to the visible clipping point on the scope.
Display Module SA2/PSA-2D PSA-2DX)	B. 1KHz sine wave; variable no load	B. Vary input level, noting upward progression of ladder display proportional to the input signal variance. Connect an oscilliscope to the amplifier output. Raise the input level to the point just before clipping is observed. Note the IOC indicators, they should illuminate prior to the visible clipping point on the scope.
14. Power	A. 1KHz sine wave, 2Vrms; 8 ohm load	A. 44V minimum should be obtainable before clip.
	B. 1KHz sine wave, 2V; 8 ohm and inductive (159uh) load	B. 20V minimum should be obtainable before clip.
	C. 1KHz sine wave, 2V; 4 ohm load	C. 41V minumum should be obtainable before clip.

Type of Test/Adjustment	Input Signal Characteristics	Comments
	D. 1KHz sine wave; 2V; 1 ohm load	D. 30V minimum should be obtainable before clip.
	E. 20KHz sine wave; 2V; 8 ohm load	E. 44V minimum should be obtainable before clip.
	F. 10KHz sq. wave; 2V; 8 ohm load	F. 50V minimum should be obtainable before clip; signal should be a good square wave with no abberations (Fig. 7.22).

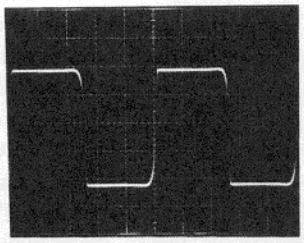


Fig. 7.22 Correct Square Wave Output Waveform

15.	Thermal	20KHz sine wave, variable input; 1 ohm load (output at 21V)	On each output module, observe the voltage (actually temperature) on test pin "Q". Voltage should drop to approximately 3.0V-3.2V as signal reduces in amplitude.
16.	Mono	1KHz sine wave; 2V; no load	Using only channel 1, apply input signal with mono/stereo switch in MONO position. Observe the output signal simultaneously of both red or "hot" terminals of both channels. They should be 180° out of phase (see Fig. 7.23).

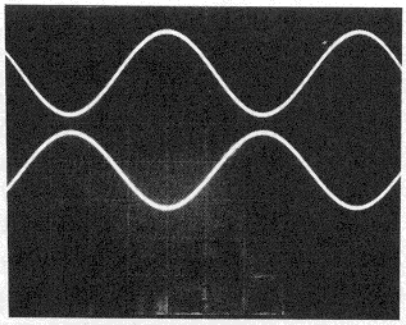


Fig. 7.23 Mono Output Waveform

17.	IM Distortion	60Hz/7KHz signal summed in a 4:1 ratio (See Fig. 7.24 for hook-up)	Using Crown IMA, readings should be from 0 to -25dB, less than .004%, all other, less than .01%.
18.	Signal/Noise	None - (See Fig.7.25 for hook-up)	With a sensitive ACVM, output signal should be at least 110dB below rated output power. Also, use a 20Hz-20KHz bandpass filter ahead of the voltmeter.
19.	Quiescent Power	None	Should be less than 90W.

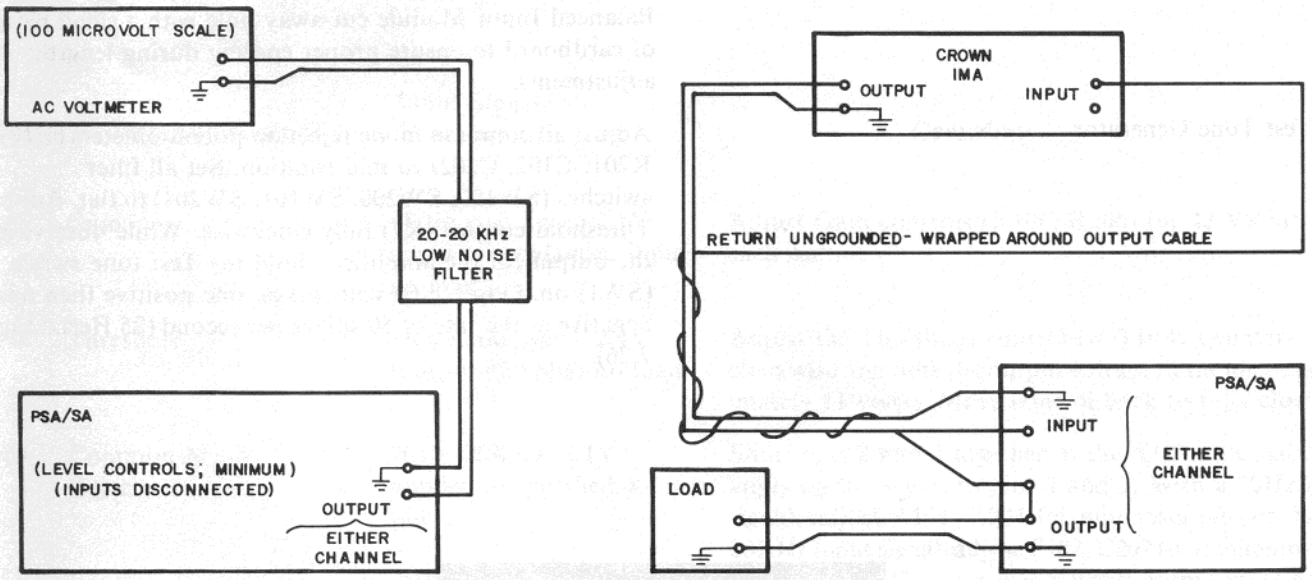


Fig. 7.24 IM Distortion Test Set-Up

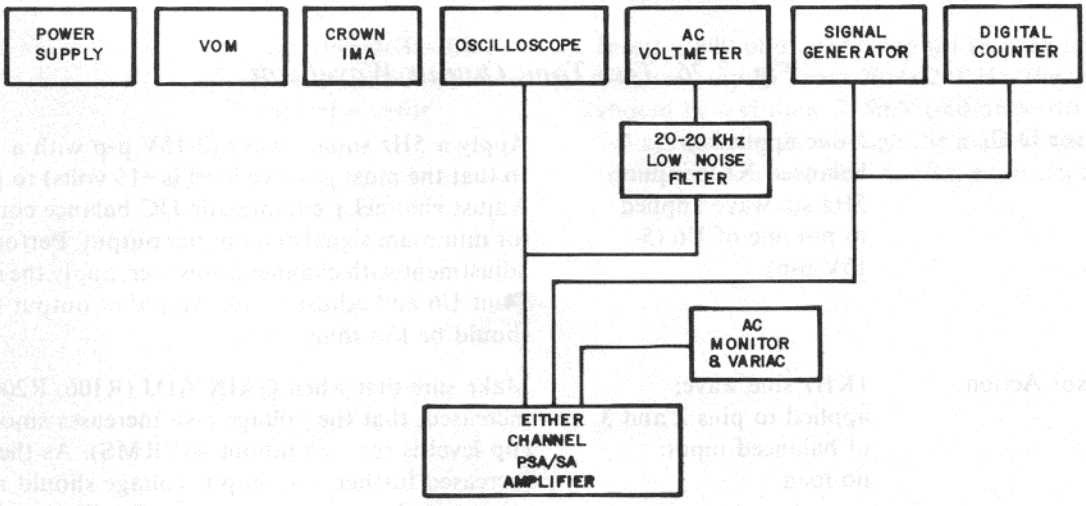


Fig. 7.25 Signal To Noise Test Set-Up

	Type of Test/Adjustment	Input Signal Characteristics	Comments
	PSA-2 Balanced Input Module		In order to make proper repairs/adjustments with the PSA-2 balanced input module, it is necessary to remove the control panel plate and utilize an extender card (CPN M 20149-7). This allows easy access to all controls and adjustments. **Note:** Be sure to block air passage of the Balanced Input Module cut-away hole with a small piece of cardboard to ensure proper cooling during lengthy adjustments.
20.	Test Tone Generator	None	Adjust all common mode rejection potentiometers (R101, R201, C102, C202) to mid rotation. Set all filter switches (SW100, SW200, SW101, SW201) to flat. Adjust Threshold control (R7) fully clockwise. While observing the output (of the amplifier), hold the Test tone switch (SW1) on. Observe 60 volt spikes, one positive then one negative at the rate of 50 spikes per second (25 Hertz; Fig. 7.26).

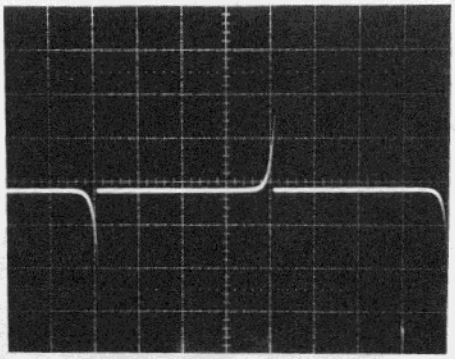


Fig. 7.26 Test-Tone Output Waveform

21.	Compressor D.C. Balance	None applied to balanced XLR inputs; 5Hz sq. wave applied to pin one of U6 (5-15V p-p)	Apply a 5Hz square wave (5-15V p-p with a DC offset so that the most positive level is +15 volts) to pin 1 of U6. Adjust channel 1 compressor DC balance control (R116) for minimum signal at amplifier output. Perform the same adjustment with channel 2 however, apply the signal to pin 14 of U6 and adjust R216. Amplifier output for both should be less than 1 volt.
22.	Compressor Action	1KHz sine wave; applied to pins 2 and 3 of balanced input; no load	Make sure that when GAIN ADJ (R106, R206) is slowly increased, that the voltage also increases smoothly until clip level is reached (about 44VRMS). As the control is increased further, the output voltage should remain constant and then, increase once again. The exact range of compression can be measured by turning the gain adjust control fully clockwise and measuring the input voltage verses output voltage (see performance graph, Fig. RVW.17).

Type of Test/Adjustment	Input Signal Characteristics	Comments
23. Gain	1KHz sine wave, 2.1V applied to balanced inputs no load	Adjust Gain controls (R106, R206) for 42 VRMS at each output
24. Threshold	1KHz sine wave, 2.1V (output 42 volts) no load	Adjust the Threshold control (R7) fully counter-clockwise and note the output voltage (it should be approximately 11 volts). Move control back to fully clockwise.
25. Common Mode Rejection	20Hz/20KHz, 2.1V applied to specified XLR pins	Short pins 2 and 3 together of the XLR input jack while applying the signal to pins 1 and 2. With a 20Hz input signal, adjust R101, R201 for minimum output. With a 20KHz input signal, adjust C102, C202 for minimum output.
	200Hz and 2KHz, 2.1V sine wave; no load	Check the CMR Response output; output must be: 70dB below 42V from 5Hz-3KHz and 55dB below 42V at 20KHz.
26. Filter Response	50Hz, 15KHz; 2.1V sine wave; no load	Activate all LO and HI PASS filter switches (SW100, SW200, SW101, SW201). Apply 50Hz signal to each channel. Vary the input signal frequency and make the following observations: Response should be flat within ±1dB of the center frequency. At the 3dB down point from center frequency, the frequency should vary no more than ±5%. Follow the same procedure for the 15KHz high pass filter. Return filter switches to "flat".
27. Noise	Variable 20Hz-20KHz sine wave; 600 ohm center tapped resistor	Insert a 600 ohm center tapped resistor into the balanced input. From 20Hz-20KHz, the amplifier output should be less than .775mV (-60 on V/dB scale). With a voltage gain of 20 through the main amplifier (see specs), this corresponds to the -86dBm equivalent input noise.

7.10 PSA-2 HI/LO Pass Filter Frequency Alterations

In order to alter the roll-off frequency of the HI/LO pass filters, it is necessary to change several components located on the Filter Module (within the Balanced Input Module). A portion of the Balanced Input Module schematic and filter board layout diagram are duplicated below to aid in familiarity with the component parts referred to in conversion formulas.

Step 1: Remove the Balanced Input Module from the rear of the unit.
Step 2: Remove the shield board by gently crimping together each of the two retaining clips; lift board upward.
Step 3: Remove the filter board by gently crimping together the one retaining clip while simultaneously lifting board upward.
Step 4: Perform the following calculations which will determine the value of C107, C108, C109, C207, C208, C209, R102, R103, R104, R202, R203 and R204.

Component changes for various highpass and lowpass cutoff frequencies

1. **C103, 203, 104, 204, 105, and 205 all equal C***
2. **R107, 207, 108, 208, 109, and 209 all equal R***
3. **R* and C* are chosen according to the following general limitations:**
   a) **1K< R*< 330K (increasing R* value gives increased noise)**
   b) **R102, 202 > 2K**
   c) **R104, 204 <1M**
4. **With valid values of R* and C*, the other resistor and capacitor values are chosen according to the following formulas:**

R102, 202= $\frac{.7184}{2\pi f_h C^*}$

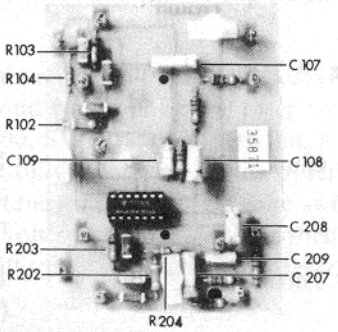
R103, 203= $\frac{.2820}{2\pi f_h C^*}$

R104, 204= $\frac{4.941}{2\pi f_h C^*}$

C107, 207= $\frac{1.392}{2\pi f_l R^*}$

C108, 208= $\frac{3.546}{2\pi f_l R^*}$

C109, 209= $\frac{.2024}{2\pi f_l R^*}$



when f_h = highpass cuttoff
when f_l = lowpass cuttoff
5. **For values shown in schematic f_h = 50Hz and f_l = 15KHz**

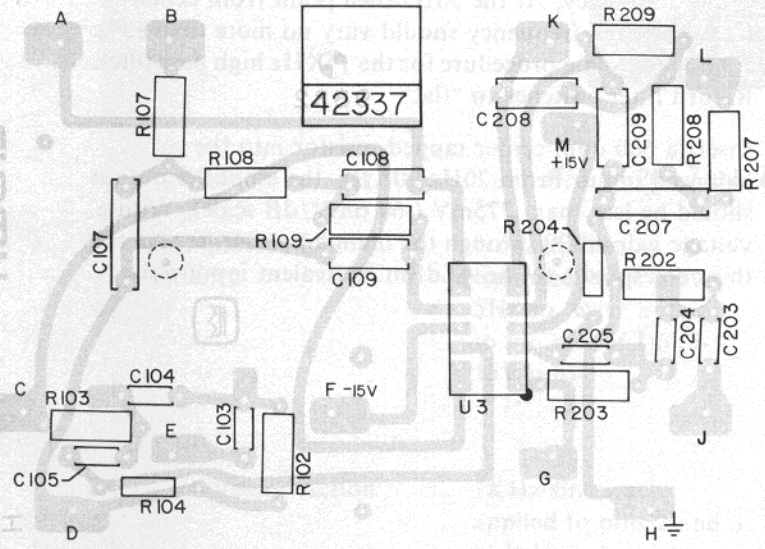


Fig. 7.27 Filter Board Schematic

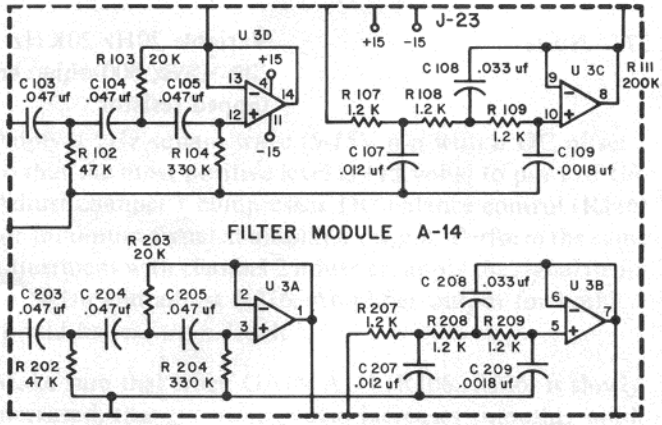


Fig. 7.28 Filter Board Component Layout

7.11 Voltage Conversion Instructions

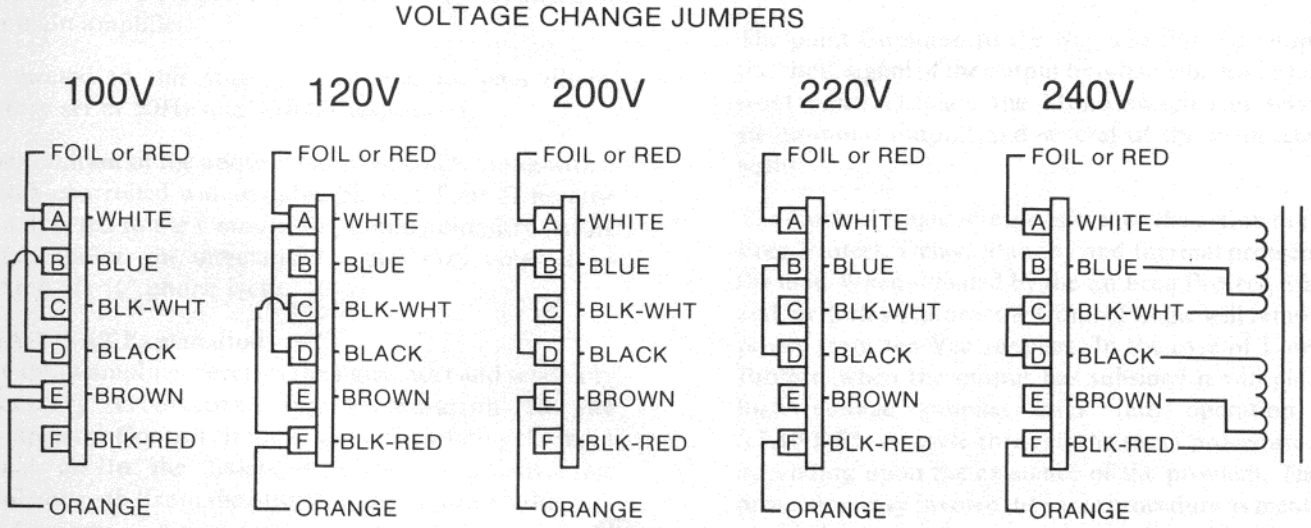
Quite often it is necessary to transport a unit to another country. If so, it will be necessary to alter the operating voltage of the unit to match the standard voltage used there. For this reason a world-wide voltage map is supplied (Fig. 7.30) as well as the following interconnect diagram. **(Note:** On earlier units, this diagram is placed on the interior of the bottom cover should this manual not be readily available.)

In order to change the voltage, it is first necessary to disconnect power and remove the bottom cover from the unit.

Warning

When removing PSA-2/SA2 covers, always discharge the unit as described in Section 7.5.

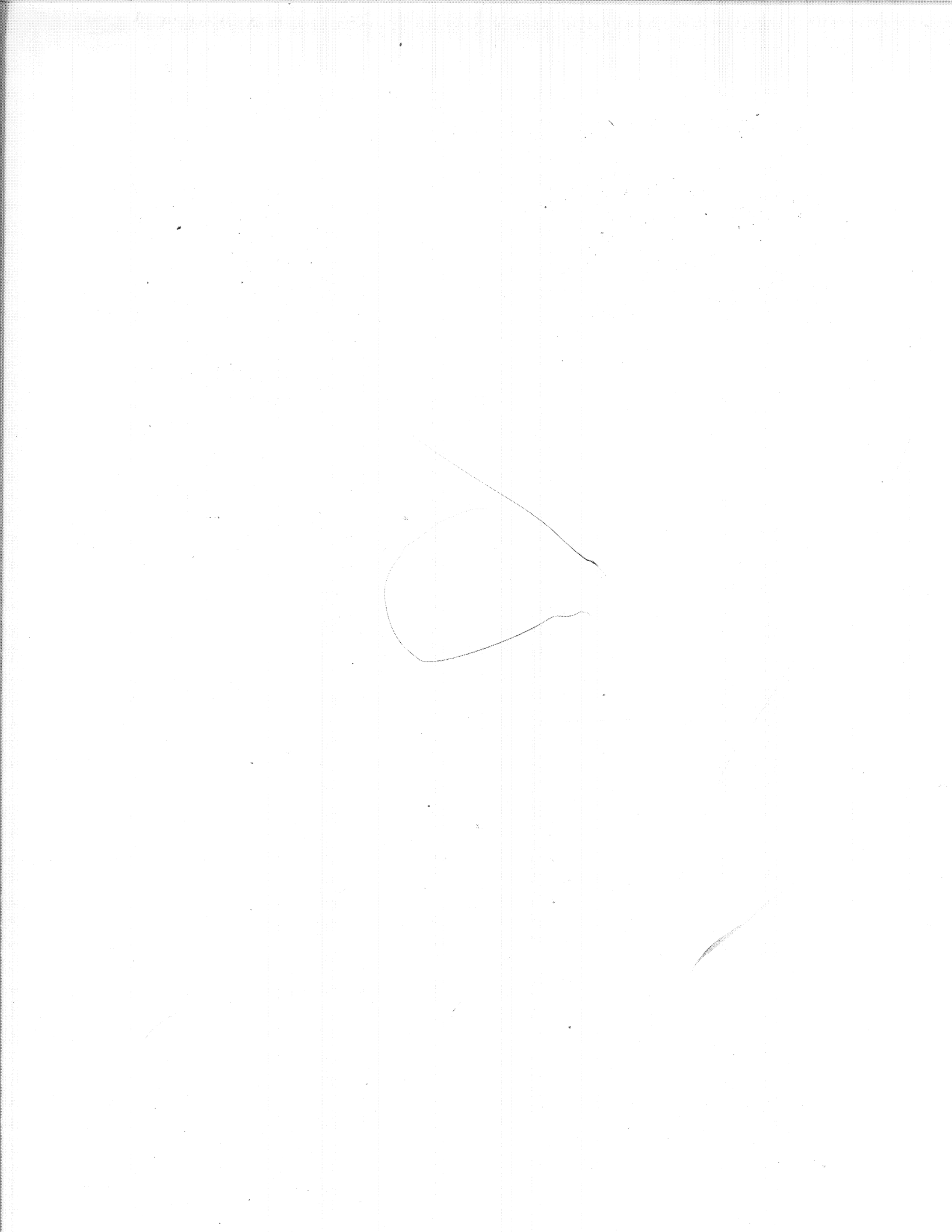
The voltage connections are made with push on terminals. After the correct operating voltage has been chosen and all leads properly identified, follow the connect drawing (Fig. 7.29). Be sure to also make all necessary fuse changes (if needed).



NOTE:

THREE SETS OF JUMPERS MUST BE CHANGED. ONE SET ON EACH LARGE POWER TRANSFORMER AND ONE SET ON THE RELAY BOARD. A 20 AMP FUSE SHOULD BE USED ON 100 AND 120 VOLTS. FOR 200, 220 AND 240 VOLTS USE A 10 AMP FUSE.

Fig. 7.29 Voltage Conversion



7.12 Block Diagram Circuit Theory

General

Refer to the block diagram, Fig. 7.31. The diagram does not show all circuit connections or feedback loops due to circuit complexity, but there is sufficient data to grasp the function of each circuit. Note also that only channel one is shown for simplicity.

PSA-2 Input Explanation Only

An input signal is fed to the initial stages via the standard unbalanced input or the balanced input. Both cannot be used simultaneously due to the "interrupt" function of the unbalanced input jacks.

The balanced input jacks are located on a separate, rear panel plug-in module board which also contains many of the professional features unique to the PSA-2.

A Variable Gain stage, next in line on the Balanced Input Module, adds an adjustable voltage gain (0-10) ahead of the main amplifier.

Connected to this stage, are Hi and Lo pass filters, factory set at 50Hz and 15KHz respectively.

The resultant of the above mentioned stage, along with a switch-controlled wide-bandwidth Test Tone Generator signal, is fed to the Compressor-Limiter circuitry. At its output point, an unbalanced signal may enter if so desired via ¼" phone jacks.

PSA-2/SA2 Explanation

The input amplifier receives the signal next and sends any necessary error-correcting information to the Compressor Control circuitry as well as sending the main signal on to the Balanced Stage. Essentially, this feedback path (from the output of the input amp through the Compressor Control circuitry) adjusts the amount of compression needed at that particular instant to provide distortion-free output.

In order to drive the NPN and PNP Output Stages, a Balanced Stage is necessary. Should a situation be encountered where protection of the Output Stages is needed, the Protection Circuitry will automatically reduce the drive available to the Balanced Stage and thus remove the stress on the output devices.

Both the NPN and PNP Output Stages consist of four SOA analyzed and V_{BE} matched output transistors plus a predriver/driver combination that also aid in carrying the quiescent power load. Together they help form the quasicomplementary, Class AB method of operation used in the PSA-2/SA2.

Feeding positive current to the NPN OUTPUT STAGE, and negative current to the PNP OUTPUT STAGE, are the POS and NEG Vcc (high Voltage) Supplies. The common point between the two Output Stages is ground. A departure from previous smaller Crown amps, this method allows sophisticated information to be fed to the protection Circuitry from the Output Stages with reference to ground. Both channel's High Voltage supplies work independently of one another.

The point Common to the Neg and Pos Vcc supplies is the "hot" signal of the output terminal which also feed the front panel Display, the Mono switch (for selectable stereo-mono output) and several of the main feedback paths.

The Control Logic is responsible for the action of the Lo Freq Protect, Delay, Standby and thermal protection of the unit. When signaled by the Lo Freq Protect, Standby and/or Delay feature, the Control Logic will remove the power from the Vcc supplies. In the case of Low Freq Protect, when the output has subsided it will place the high voltage supplies back into operation from STANDBY or cycle through the same procedure again depending upon the existence of the problem. Thermal protection may involve the same procedure as mentioned above but only in extreme cases. A thermal switch imbedded in the high voltage transformer's windings will activate the Control Logic when potentially damaging current demands are being placed on it.

The Low Voltage supply drives all low-power signal path circuitry including the Control Logic, Display and Fan speed logic. At an internal temperature of 47°C, the unit will automatically shift to "high" fan speed operation for additional cooling.

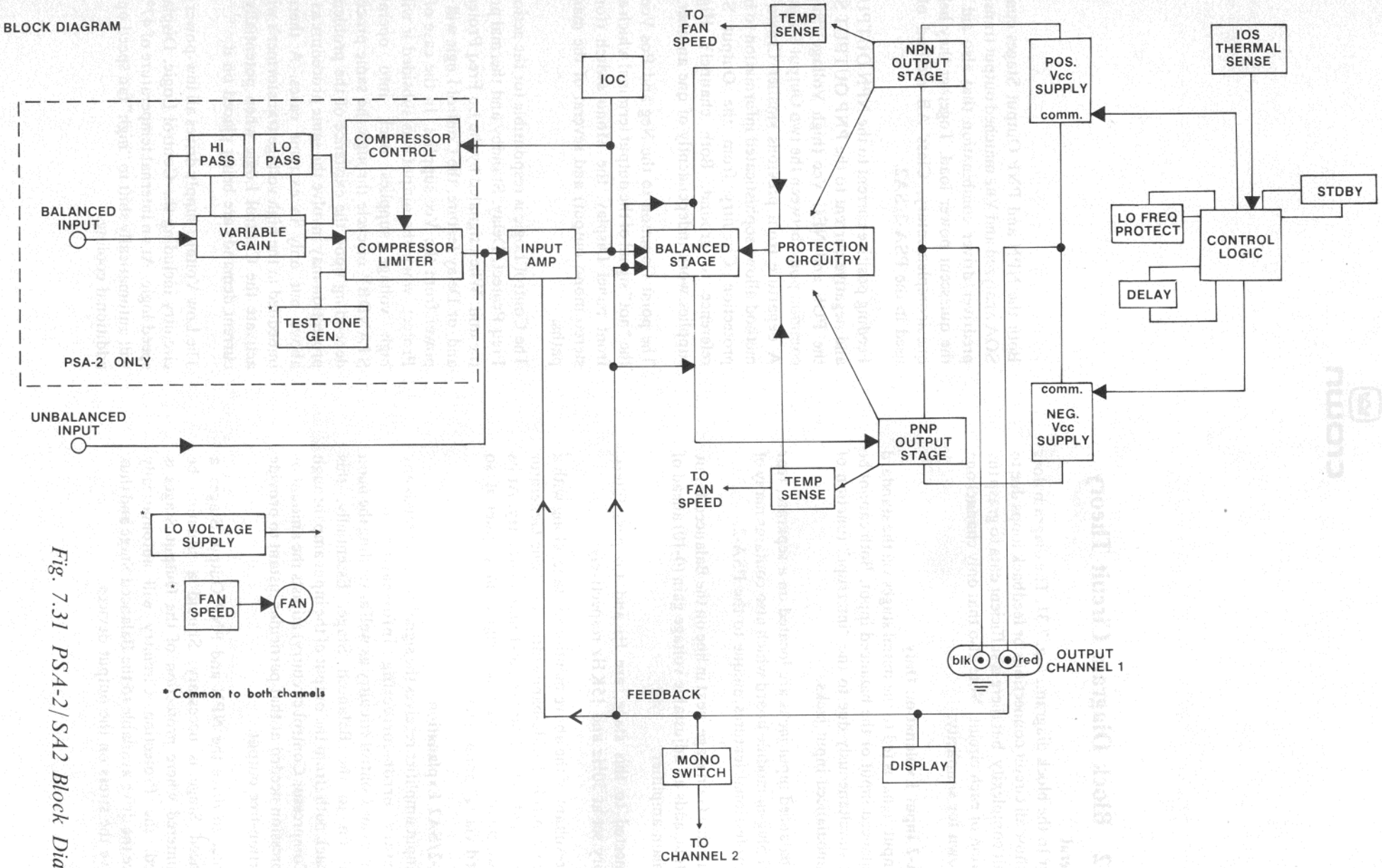


Fig. 7.31 PSA-2/SA2 Block Diagram

7.13 Theory of Operation

General

The Crown PSA-2 and SA2 are two unique power amplifiers which incorporate revolutionary design concepts as well as high performance technology. Much product research was done prior to the actual production of these units. For example, self analyzing protection circuitry was needed in order to meet the demanding headroom requirements of very low impedance loads (usually the result of paralleling speakers). Modular internal construction was also needed in order to make servicing more time-efficient especially for those users involved in commercial sound. Delayed power-up and low frequency (including DC) protection is a feature long requested by loyal Crown users. For the cosmetically sensitive audiophile, an elaborate dual function LED display was developed and made standard on the SA2, but also available for the PSA-2D and PSA-2DX.

As well as the above mentioned features, many "pro-oriented" circuits such as balanced inputs, internal crossover capability, limiter-compressor and remote-control power capability were added to the PSA-2.

The SA2 and the PSA-2 amplifiers from Crown's standpoint (as also from the customer's) were well worth the many months of design research and hard labor.

Principles of Operation for the PSA2/SA2

Because the PSA-2/SA2 circuitry is different from any other previously designed Crown amplifier, the following explanation is provided in hopes that the service-person will find it less confusing.

Shown in Fig. 7.32 is a diagram of the output configuration used most commonly in all other Crown stereo amplifiers. Note that the ground side of the load is connected between the positive and negative Vcc supply.

In Fig. 7.33 the output configuration used in the PSA-2/SA2 is shown. This topology is commonly referred to as "the low side of the bridge" circuit. With this configuration, the load terminals are reversed with respect to ground (ground not connected between the positive and negative Vcc supply). This was done with the intent of making the output stage more readily controlled and observable to the voltage amplifier stages and

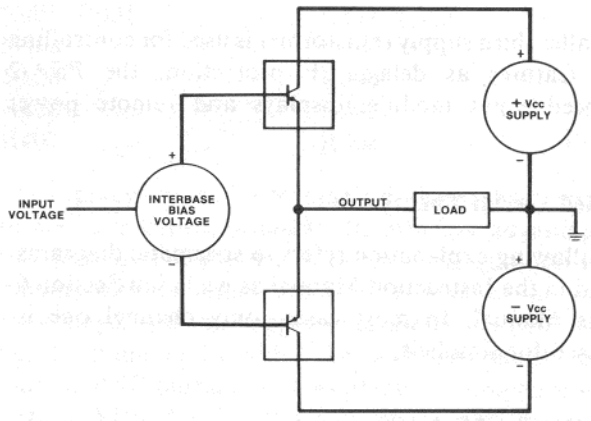


Fig. 7.32 Common Output Configuration

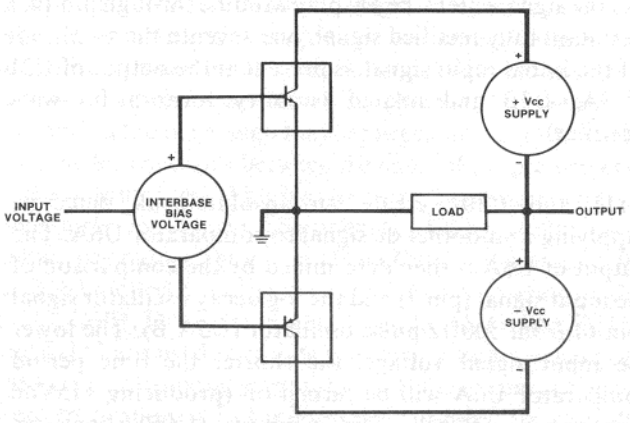


Fig. 7.33 SA2 Output Configuration

protection stages of the unit. Also, the output stages can now be more easily driven from low-voltage stages (15V) while operating at ±75Vdc, rather than previously higher voltage requirements for similiar-type circuitry.

As mentioned earlier; because the protection circuitry is no longer common to the large AC voltage of the output signal but rather common to ground, a more sophisticated yet easily monitored circuit is possible. This complex circuitry is the "heart" of the self-analyzing amplifier, but is actually easier to trouble-shoot than any other Crown amplifier.

By using two power transformers rather than one, the transformer weight is kept close to the rack mounting surfaces and an additional 40% more power is available. Another advantage is the independent operation of each channel, particularly helpful should a supply problem arise.

A smaller third supply transformer is used for controlling such features as delay, LF protection, the PSA-2 balanced input module, displays and remote power control.

Detailed Circuit Theory

The following explanation refers to schematic diagrams located in the Instruction Manual as well as in Section 6 of this Manual. In most cases, only channel one is discussed for simplicity.

SA2 Display Module

The display of the SA2 is a combined set of indicators to show the state of the output signal amplitude, the dynamic range and to show if the amplifier may be experiencing any problems.

Amber Power Indicator LED D5, is powered by R6 and the -24Vdc unregulated supply. Yellow LED's D100 and D200 are used to indicate the standby condition of their respective channels.

As the signal enters the Display Module through pin 14, a resultant fully rectified signal, one-seventh the amplitude of the initial input signal, is present at the output of U3B (U3A, U3B and related circuitry form a full-wave rectifier).

R111 and C101 create an absolute-peak detector, supplying a smoother dc signal to comparator U6A. The output of U6A is then determined by the comparison of the input signal (pin 7) and the log decay oscillator signal (pin 6) from 500Hz pulse oscillator (U5A,B). The lower the input signal voltage, the shorter the time period comparator U6A will be turned on (producing +15Vdc logarithmic pulses). The window (U6B) however, compares the same log decay signal (pin 6) to a constant 10V on pin 5. When the oscillator signal is greater than 10V, U6B is turned on and produces a +15Vdc at its output (pin 2). Note here that this output is constant and is in no way related to the input signal. It is simply used to limit the upper and lower ends of the pulsating scale.

The output from these comparators then, is fed to exclusive OR gate U5C. The length of time the OR gate is turned on, is primarily attributed to the pulse transmitted by the log time base oscillator (U5A, B).

The resistors (R114, R115, R116) and capacitors (C102, C103) following U5C are filters that average the overall DC voltage output. The result is a DC voltage that rises and falls logarithmically with respect to the input signal.

U2D is a unity gain buffer stage, simply converting a high impedance signal to a low impedance output . This output is fed to U2A and associated circuitry, particularly C104. The level at which C104 charges, is the level of the peak hold of the display.

C105 is responsible for the actual "hold-time" of the peak by the amount of time it takes to discharge through R122 and U2B.

The DC voltages from the peak hold circuitry and the output of the log amp are then multiplexed into one signal that is fed into the LED display drivers. Here the signal is divided evenly among 15 LED's. The display will show one bright illumination shifting with the "alwayschanging" output amplitude while another, less bright illumination will have a short hold time (about 4 seconds) respective to "peak amplitudes" only. Voltage divider R126, R127 and R128 assist the display driver in determining the high and low end of the display scale.

A. Output Stage - PSA-2/SA2

There are two types of output modules within each amplifier. The module which produces the negative half of the output current waveform and is powered by the positive Vcc supply, (this is a result of the inverting output topology being used), and the module which produces the positive half of the output waveform and is powered from the negative Vcc supply. For the sake of discussion we will call them by the names of the type of transistor which they simulate (the former being referred to as the NPN stage and the latter the PNP stage). Note that this is identical to the type of pre-driver used in each.

The PNP stage is constructed with NPN outputs and driver, much the same as a Crown DC-300A negative output stage. The differences are that the current sensing is the sum of all the collector junctions rather than just one device. This is necessary to eliminate the TO-3 IC housing to sink insulating hardware from all of the devices and maximize the available output power by keeping the heatsink thermal resistance as low as

possible. All heatsinks in the amplifier are electrically hot! Q402-405 are the output devices and are selected types whose Safe Operating Area is not voltage derated within the operating range of the amplifier. The driver (Q401) is a high Ft (Gain Bandwidth) type having power handling capability sufficient to eliminate it from the protection design. The collector of the driver is grounded to provide additional voltage when the output stage is driven to saturation. As such, the driver does not saturate. The pre-driver (Q400) is prevented from saturating by the diode clamp circuit of D401 and D402. D400 is part of the bias circuit of the output stages and is thermally joined to the predriver which at first characteristically cools as the drive to the output stage becomes large. This is due to the fundamentally class AB nature of the output stage accompanied by the high current gain of the driver and output devices.

It should be noted that the amplifier is usually biased for class AB operation rather than class AB+B as the other Crown products. It is possible to bias the unit for AB+B if the higher efficiency is desired. The heatsinking capacity is large enough to minimize any such need.

C400 constitutes the local voltage feedback loop immediate to the output stage. (This is functionally identical to the capacitor (typically 200pf) which is placed from the collector of the last voltage amplifier to ground in the other amplifiers.) Note that since in those units the Vcc supplies and ground are common that this is the same as making a connection to the Vcc supply as is done here.

Current degeneracy and phase compensation are achieved in the pre-driver circuit by R401 parallelled by C401.

D403 serves as a flyback diode as in all other Crown amps.

U400 along with R408 and R407 constitute an IC absolute temperature sensor to measure the heatsink temperature. This is needed to provide the protection system with knowledge of the absolute temperature of the transistor junctions of the output devices. The current flowing in U400 is proportional to absolute temperature: one microamp = one degree Kelvin. R408 is selected to obtain this constant as determined by grading of the ICs. R407 is selected to protect U400 from large signals and as such its value is not critical.

The NPN output stage is similar to the PNP as indicated:

PNP	NPN
Q402-405	Q302-305
Q401	Q301
Q400	Q300
D401, 402	D301, D302
D400	D300
C400	C300
C401, R401	C301, C302
D403	D303
U400	U300
R408	R309
R407	R308

The topology of the NPN stage is different than any used in previous Crown products. Its principle advantage at this time is that the driver of this configuration must operate with minimum Vce which is less than that of the PNP stage, and this suggests the use of the PNP driver which retains its Ft with lower voltages than the NPN part. If PNP outputs were available to complement the rugged NPN devices, It would be possible to use the topology of the PNP stage for the NPN stage as well and obtain a similar advantage for the PNP driver by grounding its collector. The tendancy of three-stage Darlington amplifier stages to oscillate at positive clip is often tracable to an Ft problem in the driver as its Vce becomes small.

B. Balanced Gain Stage - PSA-2/SA2

Continuing to follow the signal backwards through the amplifier we encounter the balanced gain stage. It is composed of two differential stages of complementary type. The differential amplifiers are constructed with monolithic dual bipolar NPN and PNP transistors. Resistor networks are used to balance the collector currents in the pairs such that the necessary current flows thru the bias network between the bases of the pre-drivers of the output stages. This bias network is composed of the previously mentioned components, D300, R300, and D400. The path of the current from Q102 (collector pin 7) to Q103 (collector pin 1) in channel 1 also flows through D113, D301, D401, D118, D117, and D115. Diodes D113 and D115 are used to isolate the driving stages in case of catastrophy from the output stages. If the output supplies were to propogate to the ± 15VDC supplies, the overall damage would be great.

Diodes D117 and D118 are part of an instantaneous current limiter bias arrangement which limits the peak output current to approximately 7A per device. The remaining part of this current limiter is provided by diodes D114 and D116.

When sufficient current flows in the output devices, diodes D114 and D116 will become forward biased by the drive voltage to the output stages. When this occurs the current will be effectively limited. Note that the diodes are connected to the opposing output current sensing line rather than to ground. This is a simple means to limit common-mode current spiking in the output stage to values less than 7A per device. The spiking current can only reach a value which is 7A minus the per device load current. Since the worst spiking occurs when the load current is large, the reduction in spiking current is large.

The differential amplifiers are rather precisely balanced by the precision resistor packs RN101 and RN102. RN102 contains the bias control which is used to tweak the balanced to result in the desired bias. The standard bias at quiescent temperature is 2.5mV as measured across the current sensing resistors R409-412.

The input to the balanced gain stage can be conveniently probed at pin 7 of RN101. This point constitutes a virtual ground in the amplifier receiving input signals through the network from pin 6 of U100 and feedback from the output signal via R114. The signal propogates from this virtual ground to the bases of Q102 and Q103 (pin 2 and pin 6 respectively). These devices act as emitter-followers and drive the remaining half of each differential pair through resistors R112, 111 and R115, 116 respectively. Acting in the grounded-base mode of operation these remaining devices provide a high quality current generator to drive the output stages.

R113 and C110 are used to compensate the closed-loop amplifier formed by the balanced gain stage and the output stages. It has a closed loop voltage gain which is about -8, as measured from the output of U100 to the output terminal. When debugging the amplifier this is a useful relationship to observe if the output voltage is unusual. In normal operation the diodes D104 and D105 should not be in conduction. They are provided to limit the charge which can be stored on C110 upon overload. This charge if allowed to become large would produce an overload recovery delay. By limiting the voltage at pin 7 of RN101 in this manner, the voltages necessary to limit the drive of the balanced gain stage are confined. This is in regard to the voltages that would result in conduction of D111 and D112. These voltages are produced by the protection circuits analog computer junction temperature simulator U101C and U101B. Conduction of these diodes limit the drive of the balanced gain stage to the respective overheating output stage.

The resistors in RN102 which parallel these diodes are used to provide the bias servo temperature feedback signal as is provided by the heatsink attachment of the bias servo transistor in other Crown amplifiers. The heating of the output devices is used to reduce the bias current control signal.

In the original design the diodes D106-110 were used to limit the voltage on pin 7 of RN101. R113 was chosen small enough that the effects of these diodes become negligible and as such these diodes are omitted from later units.

C107 and C111 are used to optimize the high-frequency behavior of the grounded-base side of the differential pairs.

C. Input Amplifier - PSA-2/SA2

At the far left of the full schematic is the stage which receives the input signal and the overall feedback loop with the resulting highly amplified error signal being used to drive the amplifier composed of the balanced gain stage and the output stages.

A monolithic dual JFET, Q101 is used as a differential amplifier to drive the Bi-FET op-amp U100. The source leads of Q101 are current degenerated by resistors R105 and R106. The drain circuit loads of the differential amplifier are provided by RN100.

Compensation is provided by C102, R109, C105, and C103. The diodes D102 and D103 are used to limit the stored charge that could accumulate on C102 upon overload.

The main feedback loop is composed of R102, R101, and C100 which controls the closed loop frequency response as in all other Crown amplifiers. Note that the channel two equivalent of R102, R202 is a larger value. This is because in the stereo mode of operation the "mono-ing" resistor R200 is grounded, parallelling R202. R200 results in a gain of -1 at its input.

The DC offset voltage of Q101 can be compensated by the adjustment provided by R104 in conjunction with R103. Input overdrive protection is provided by R108. Diodes D100 and D101 are used to prevent overdriving of the common-mode input range of the input stage upon overload. R107 is used to provide a ground reference for the input signal should the signal line become open. Since the bias current of Q101 is negligible, no bias current adjustment is needed.

R110 is used to provide an output to the IOC or compressor circuits. This output will be at approximately 13 volts if any form of overload should occur in the amplifier. Should no overload be present the signal will be a ⅛ scale inverted replica of the output signal. This fact will allow the PSA-2 compressor to respond to levels

below the overload threshold when the threshold is appropriately selected.

The supplies to the input differential amplifier stages are filtered by R7, C3, R8, and C4 to remove the noise induced by the 15 volt regulators.

D. Protection Circuitry

The protection circuitry of the SA2 amplifiers is perhaps the most unusual of all its new features. It is the result of an indepth study of the heating behavior of semiconductor junctions and the design and construction of a considerable amount of special hardware. It was necessary to implement the following equipment:

A. SOA III Transistor Analyzer
B. 12 bit A/D Convertor Data Aquisition Unit
C. Microcomputer (Altair 8800)
D. Instrument Amplifier
E. Dummy Heatsink with devices slaved to SOA

Once it was known what the nature of the sought after information would take, it was readily realized that this information would only be available by direct observation, since it was not available from the semiconductor manufacturers.

What was needed was a direct observation of the heating/cooling characteristics of a large sample of devices of the desired type. Data must be gathered over a large time interval (tens of seconds) with a maximum of data being gathered indicative of the shortest of time intervals. This constitutes a data gathering strategy which is not compatible with means such as storage oscilloscopes, strip-chart recorders, etc.

To meet this requirement it was necessary to program a computer to gather the data at the precise time intervals desired. The Altair was programmed to gather the data and then to transmit the data to the Crown Engineering Wang Computer for storage on disk and do the very elaborate number crunching which is needed to uncover the equivalent thermal circuit of the physical devices.

Without the use of the computers the proper development of this circuitry would have been nearly impossible. The circuitry acts to simulate via an electrical signal the junction temperature inside the worst device that is likely to be mounted in the output stage. The circuitry does this without any direct probing of the output chip.

The knowledge we required was the time behavior of the junction temperature for an arbitrary power input signal. This was deduced by watching the cooldown phase of power transistors which had been heated in an environment identical to the heatsinking used in the amplifier.

In the amplifier we must also know what power has been applied to the output devices. This information is provided by the multiplier circuits; i.e. Q104 with U101D and Q105 with U101A. Assuming that we limit our attention to the protection circuit that protects the NPN output stage of channel one; Q104 is used to multiply the Vce of the output stage as sensed through R120 with the collector current as sensed by R304 via RN104 pins 8 to 7 and R119. Q104 is what is commonly referred to as a two-quadrant transconductance multiplier. Its operation is based on the logarithmic nature of the base-emitter voltage as a function of collector current.

Since the output of Q104 is balanced, the currents at its collector must be converted to provide an unbalanced signal. U101D forms an op-amp current mirror. The current of the collector of Q104 pin 7 is mirrored by the action of the output of U101D pin 7 RN104. The current in the feedback resistor pins 1 to 2 is equal and opposite to the current in the collector of Q104 pin 7. Since the resistor from pins 2 to 3 is of equal value to the first, the current will be identical. This current is joined with the current from the other collector output of Q104, pin 1. This node constitutes the output of the multiplier. Summed with these currents is a current proportional to the heatsink temperature upon which the output devices are mounted.

The current from the IC sensor on the output stage is bypassed with a capacitor C117 to minimize audio signals capacitively coupled to the sensor wiring. Since the sensor is intimate to the heatsink which is electrically hot, such coupling is to be expected. To allow for monitoring of the temperature by the fan speed control circuits and troubleshooting, the current is input to a precision sense resistor (10K) in RN104. This converts the sensor signal to a voltage which is proportional to absolute temperature with a scale factor of -10mVDC/degree Kelvin. In other words, the voltage for room temperature (25 degrees centigrade) would be -2.93VDC at +Ts. This is a convenient point to probe should either the sink temperature or the sensor be suspect.

A fourth current is added to the output node from the multiplier. This current provides a bias for the temperature computer and references the device to the rating temperature of 25 degrees centigrade. The current is provided by RN104 pins 3 to 5. These combined currents are input to a virtual ground of the op-amp U101C which simulates the junction temperature. The feedback network of pins 1-4 of RN103 and C112-114 is an electrical analog of the thermal impedance of the output semiconductors. Therefore when a current which represents the power being input to the transistors is input to this analog computer the output is a voltage which responds as the temperature of the transistors' junctions. When this temperature exceeds 200 degrees centigrade, the device is too hot. The output of the analog computer progressively remove operating bias from the associated balanced gain stage by forward biasing D111. Being unable to provide more drive for the output devices, the output dissipation must decrease until the junction temperature is acceptable.

The dynamics of the output voltage of the analog computer ranges from approximately -12VDC at 25 degrees C. to +9VDC at 200 degrees C junction temperature. This voltage may be readily probed at TP-1.

The multiplier dual transistor has an offset adjustment for balancing composed of R117 and R118. This may be adjusted by removing all current from the output stage and producing a low-frequency output from the amplifier. If the multiplier is balanced no AC voltage will appear at TP-1.

The operation of the protection circuit for the PNP stage is similar except for the polarity reversal of the multiplier and simulator stages. By attaching the heatsink temperature sensor and offset current to the other output of the multiplier, i.e. the input to the current mirror, it is not necessary to reverse the polarity of the sensor. This allows all of the sensors to provide the same polarity of output voltage, simplifying the design of the fan speed controller.

The fan speed controller is shown on the full schematic between the input amplifier stages of the two channels. It perhaps is best discussed along with the protection system since its function is to increase the air flow by engaging the fan relay in high-speed whenever any one heat sink's temperature exceeds 50 degrees C. The quad-comparator U1 monitors the four heat sink temperature sensors. When one is sensed over-temp the output of U1 will turn on both Q1 and the fan relay. Q1 provides a temperature hysteresis for the controller to prevent erratic switching.

E. Muting Module applies to earlier units only; (circuit incorporated into Main Module above indicated SN).

The power-up and power-down phases of operation were found to produce noises in the output. While these signals were of such amplitude as to be harmless, it was recognized from experience that customers would not necessarily view such noises as insignificant. To prevent such noises, a simple circuit was added to the design to prevent the operation of the balanced gain stages until the +&- 15VDC supplies were adequate to have the amplifier in control of its output.

Referring to the muting module schematic, the transistor Q4 driven by D1 acts to sense sufficient voltage on the supply rails. The conduction of D1 and Q4 act to turn off Q3 which saturates Q1 and Q2 in the low voltage state of operation. With Q1 and Q2 in saturation, the resulting conduction of diodes D100, D101, D200, and D201 inhibit all output drive from the balanced gain stage, which totally disables the output stages. This will happen both during power-up and power-down. Of course with the voltage very low none of these effects will occur including any drive to produce output noises.

F. Power Supplies

U2 and U3 constitute adjustable IC regulators which are protected against overload and over-temperature by internal circuitry. Their output is adjusted to ±15VDC by RN3 and RN4 respectively. The unregulated input to these supplies is derived from T3 by diodes D4-7 and filter capacitors C5 and C6. C4 is used to prevent RFI from diodes D4-7. Capacitor C7 is used to reduce the high-frequency output noise of U2. C8 and C9 act also to suppress supply noise and impedance. Diodes D8 and D9 are the traditional diodes to prevent damage from application of reverse polarity voltages to the outputs of the supplies.

Transformer T3 is used as an autoformer to power the fan motor when the unit is wired for voltages other than 120VAC. T3 uses the typical universal primaries format used in other Crown products. In order to reduce the current drawn by the fan motor its power factor is corrected by the capacitor C4. T3 has a low voltage secondary which is used to power the LED's in the SA display module. This is more efficient than using the 15 volt supplies for all such power.

Quad-comparator U1 sections B and D are used to control the relay driver transistor Q100 and Q200 which power the channel 1 and channel 2 output stage supplies respectively. When Q100 or Q201 are off, the collector voltage will drive Q101 or Q200 respectively to light the corresponding standby lights for the down-powered channel. By grounding of the drive circuits at the junction of D107 and D207 and R111 or R211, the output stage supplies may be forced into the standby state.

Focusing our attention upon just the channel 1 relay control circuitry (channel 2 is identical) we find the following. Upon power-up the capacitor C105 is discharged and starts to charge with the current supplied by resistor R107. When the potential on U1B pin 11 exceeds the approximately 7.5 volts on pin 10 the output on pin 13 will proceed positive allowing Q100 to turn on. The result of Q100 turning on is the production of a small hysteresis voltage on pin 10 as a result of R109. This insures the decisive switching of U1B and Q100 for proper relay action. If C103 were switched in parallel with C105 (which is the function of the DELAY switch), the time needed to charge this circuit would result in a 4-5 second delay in the turn-on of the unit.

R105 is wired in series with a thermal switch wound in the windings of the output stage power supply transformer T1. Should T1 overheat the thermal switch will open causing U1B via D107 to turn off Q100. This method of protecting T1 allows for much larger outputs from the amplifier without fuse blowing. The use of conventional fuses or circuit breakers is not an optimum means of protecting a power transformer because the time constants of these devices are many times shorter than the thermal time constant of a large transformer whose time constant may be a matter of hours.

Low frequency protection of loads is made available by switching the output signal to drive R100 and C104 which act to low-pass the output signal. Should the output be too long in excess of 26VDC the diode network composed of D101-104 and zener D105 will conduct removing the bias-off voltage from the input of the comparator U1A as provided by resistors R101-104. The output of will act to discharge C105 and C103 via R106. This will remove power from the output stage and cycle the supply back on as soon as the DC input dissipates which caused the shut-down. This approach is more reliable than the use of a relay in the load circuit since such a relay may not be able to break a DC circuit due to prolific arcing caused by load inductance.

D106 is used to prevent back biasing of C105 and C103. Were this not necessary R106 would be unnecessary.

G. Output Power Supplies

The output supplies are two thermally protected transformers T1 and T2 with bridge rectifiers driving filter capacitors C101, C102, C201 and C202. Capacitors C100 and C200 are used for RFI suppression.

T1 and T2 each have arc suppression across their relay contacts (C2, R5 and C1, R4) to improve relay life and to reduce radio frequency interference. These transformers have universal primaries. Fuses F1 and F2 are the aforementioned fault protection fuses. Only shorted supplies should be able to dislodge these fuses in normal circumstances.

Switch S1 is arc suppression protected by C3 and R3 and is the main front panel power switch. Should F3 be blown, indicating a failure in the control supplies, nothing will function in the amplifier. It would be as if the power were turned off.

The fan motor operates in low speed when the power is applied through resistor R1. To operate in high speed R1 is paralleled by R2. R2 is used to prevent destruction to the fan speed relay when engaging and charging C4.

All of the relays have damping diodes across their coils to protect their drivers.

H. PSA-2 Balanced Input Module

The balanced input module is used only on the PSA-2(D). It provides the following functions that are particularly useful to professional sound reinforcement users:

A. Balanced inputs with XLR connectors.
B. Gain adjustments for normalizing line levels.
C. Filters for use as crossovers, etc.
D. Variable threshold compressor limiter.
E. Impulse tone generator.

The channels are identical in design and the discussion will focus on channel 1. The balanced input amplifier is provided by U1A which receives its signal from J24. R101 is used as a low frequency common-mode rejection adjustment while C102 is provided for optimizing the high frequency common-mode rejection.

The output signal from U1A is high-pass filtered by U3D and is routed to SW100 where the user may select either the HP filtered or unfiltered signal for input to the gain stage. The filter constructed by U3D is a 3-pole Butterworth type of 50Hz, as supplied with the standard unit. It may be changed by swapping the filter module board or changing the component values on the filter board. This allows a sound installer to have an inventory of his preferred crossover frequencies available for use.