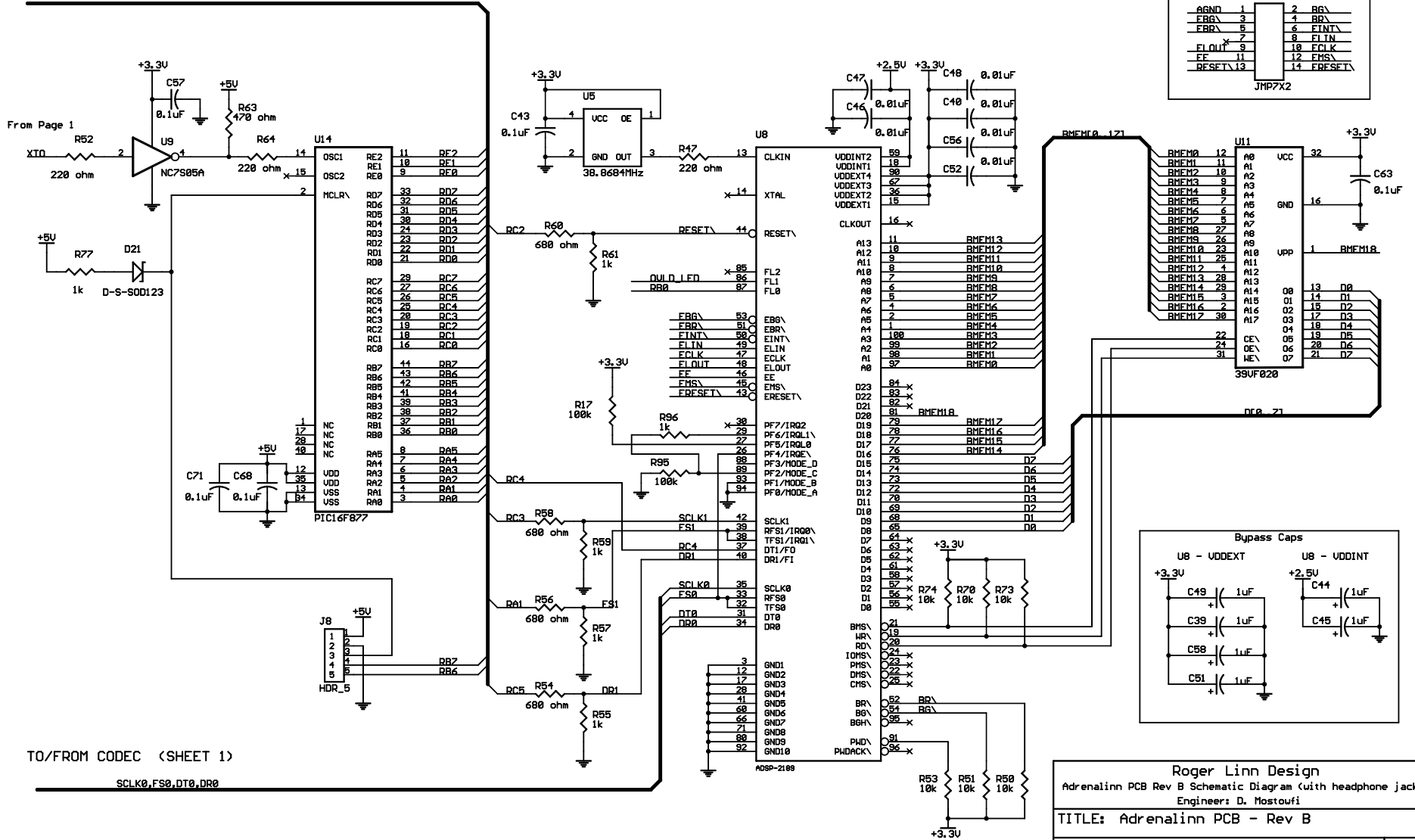


TO/FROM DIGITAL I/O (SHEETS 1 AND 3)

RA0..5J, RB0..7J, RC0..7J, RD0..7J, RE0..2J



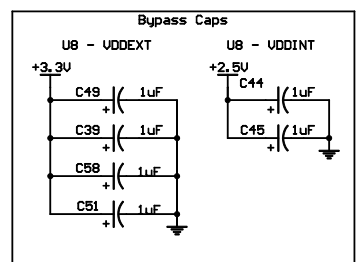
TO/FROM CODEC (SHEET 1)

SCLK0, FS0, DT0, DR0

EZ-ICE Port (ADSP-218x Debug) J4

AGND	1	2	BG\
FBG\	3	4	BB\
FBR\	5	6	FI IN\
FLOUT\	7	8	FOL IN\
FF	9	10	FMS\
RESET\	11	12	FRESET\
	13	14	

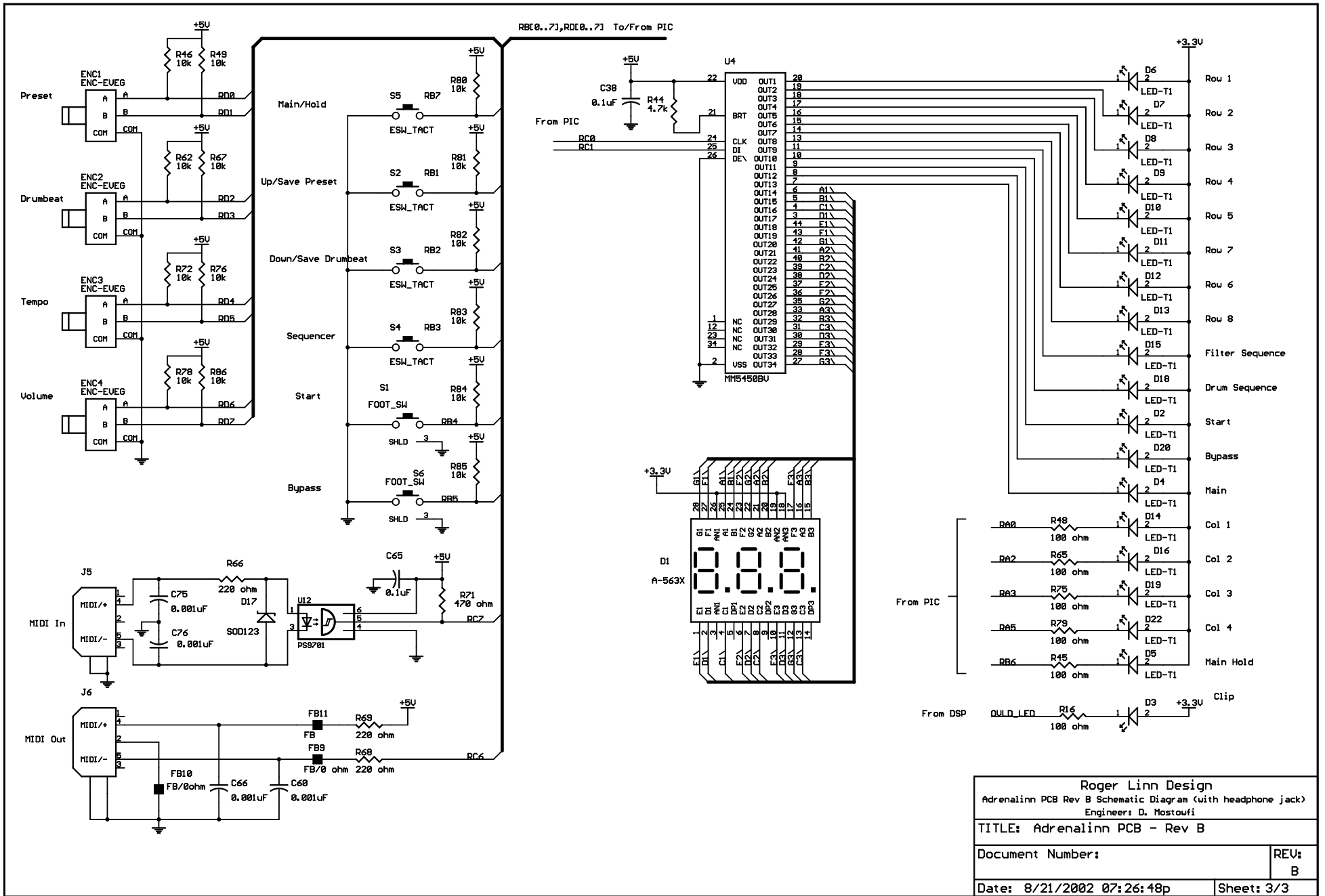
JHP7X2



Roger Linn Design  
Adrenalinn PCB Rev B Schematic Diagram (with headphone jack)  
Engineer: D. Mostoufi

TITLE: Adrenalinn PCB - Rev B

Document Number:	REU: B
Date: 8/21/2002 07:26:48p	Sheet: 2/3



<b>Roger Linn Design</b> Adrenalinn PCB Rev B Schematic Diagram (with headphone jack) Engineer: D. Mostoufi	
<b>TITLE: Adrenalinn PCB - Rev B</b>	
Document Number:	REV: B
Date: 8/21/2002 07:26:48p	Sheet: 3/3