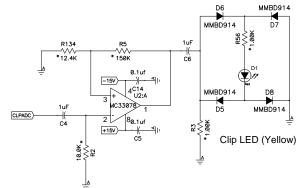
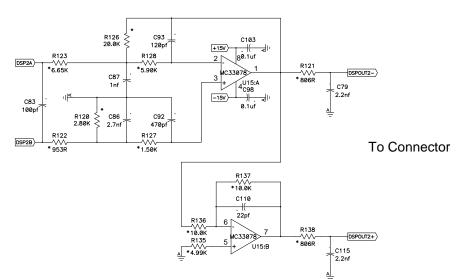
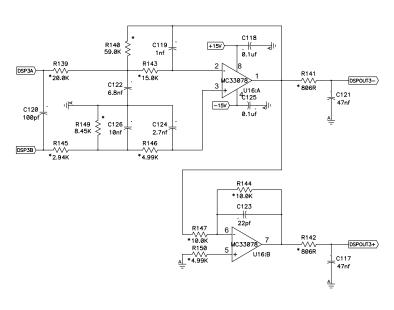


This is a comparator configuration. Monitors the ADC input (CLPADC) and when near saturation (+/- 1.20V pk) outputs a square wave The threshold is set by the resistor network at the (+) input









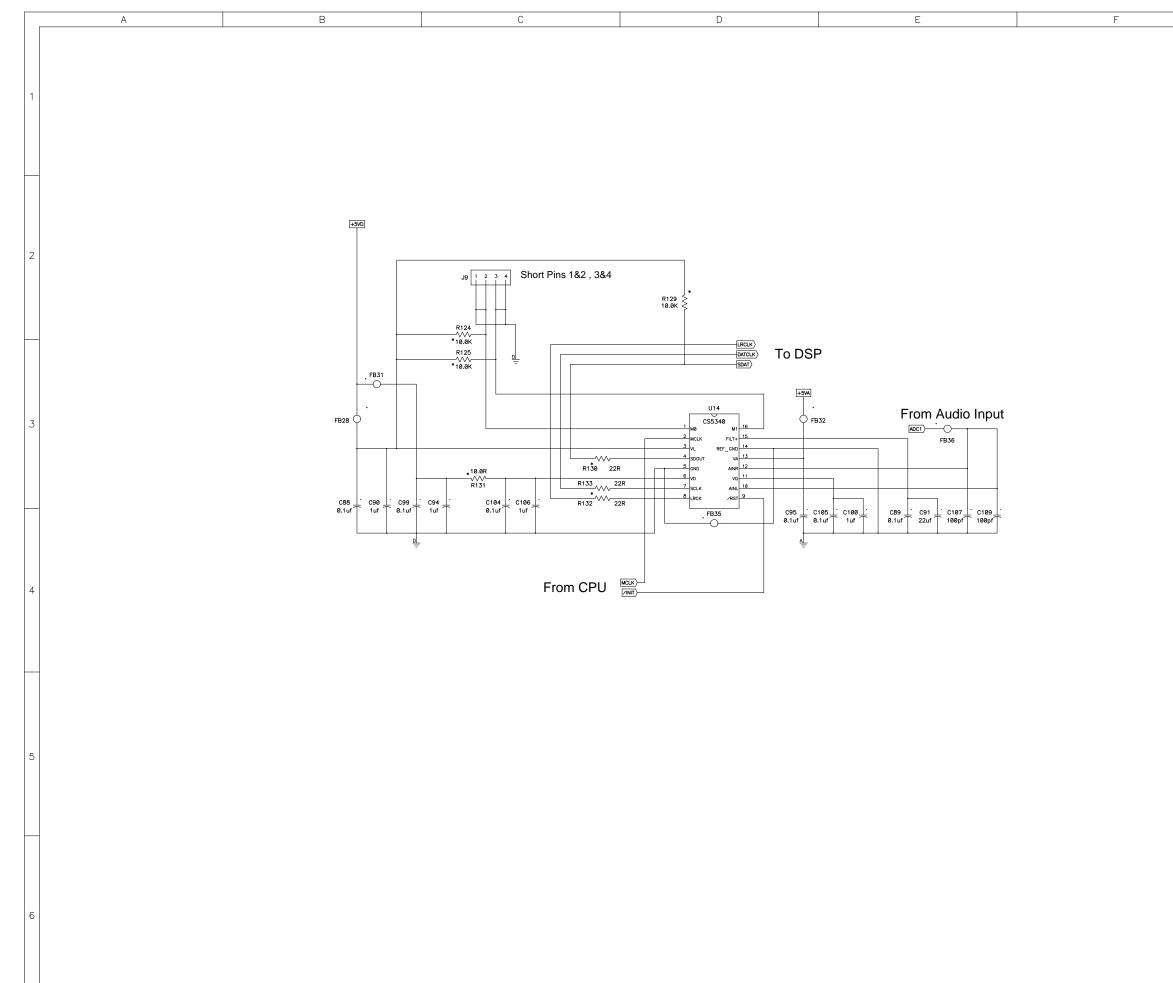
Α	В	С	D	E	F

G	Н

Signal present LED (Green)

G

Title	Analog Filters						
Size	Number			Rev	1		
D				В			
Date	Tue Jul 31, 2007	neering					
362 <b>90</b> 2en2	9 FR1_FR2 SCHEMATIC F REV (INPUT M	018.hteèsch	2 of	5			
		Н					



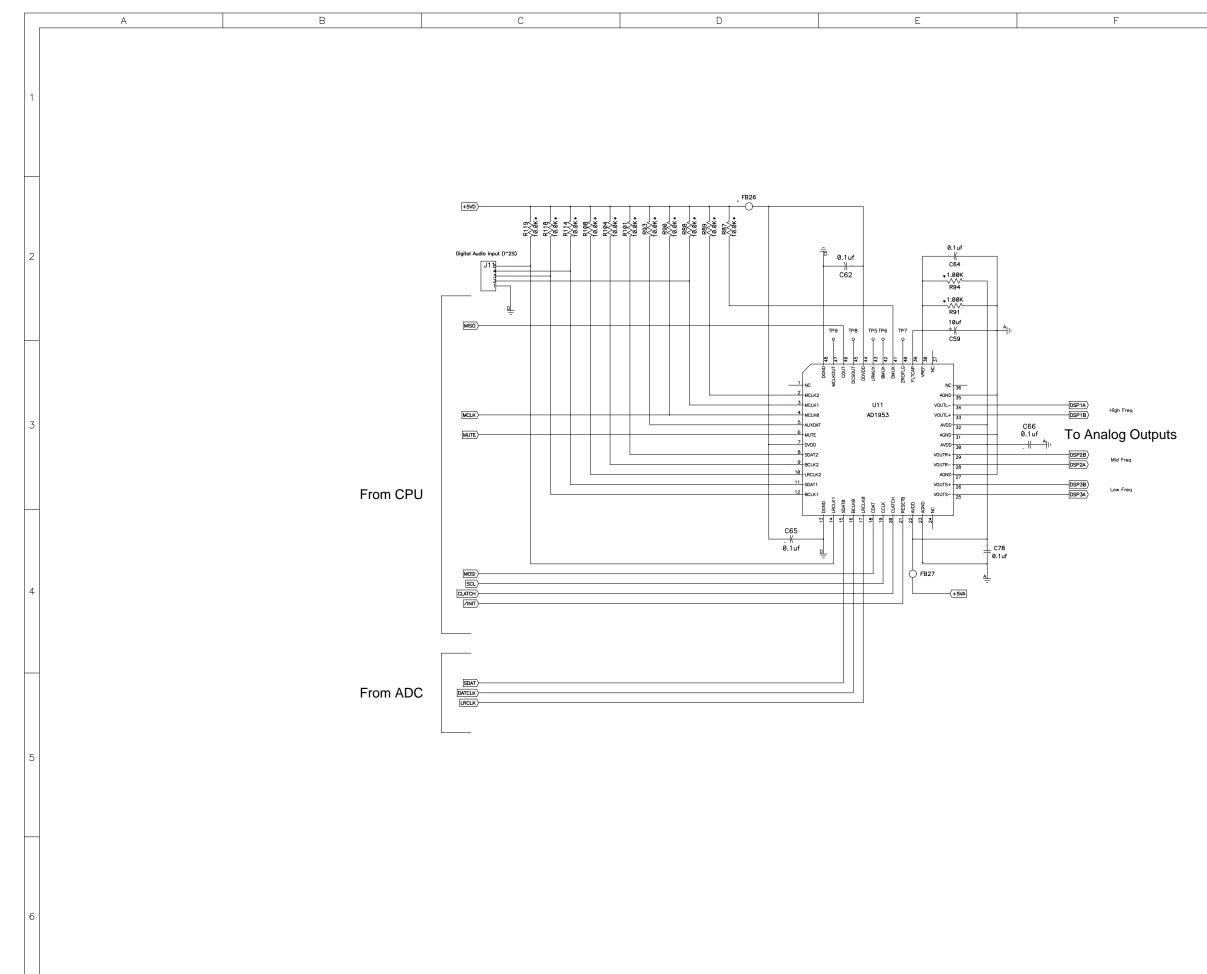
А	В	С	D	E	F
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G	Н

Title	AE		6		
Size	Number			Rev	
D				В	
Date	Tue Jul 31, 2007 Drawn by Home Engine				
362399923+112	Ø FR1_FR2 SCHEMATIC F REV (INPUT M	10 <b>BibleEi)</b> tsch	3 of	5	
		Н			-

G

Α	В	C	D	E	F	G	н
1							1
		+5/0		1			
2			C56				2
		R14 ≥ C15 10.0K ≥ 10.0K ≥ C15		<			
		R14 2 ( 10.0K 0.1uf	U10				
		U3 (RXD)	1 VPP VCC 20 2 P3.0 P1.7 19				
			3 P3.1 P1.6 18   TP1 0 4 XTAL2 P1.5 17	3 0 4 TP3 TP3			
		2 GND OUT 3	5 XTAL1 P1.4 16 6 P3.2 P1.3 15				
		12.288Mhz	P1.2 14 8 P3.4 P1.1 13		_		
			TP2 9 P3.5 P1.0 12 10 GND P3.7 11				
		R8 2 10.0K2	AT89LP4052 OR AT89S4051				
3			OR AT89S4051		CLATCH TO DSP		3
		u					
		sw2 22R ≶					
		SW2 22R 22R 3 3 1 2 3 22R 22R 22R 22R 22R 22R 22	To Relays				
		D					
		*					
		10.0K <					
4							4
		10.8K ≥ 10.8K ≥ 10.8K ≥ 10.8K ≥ 10.8K ≥ 10.8K ≥ 10.1uf 0.1uf			JIG		
		-					
5							5
6							Title CPU 6
							Size Number Rev B
							Date Tue Jul 31, 2007 Drawn by Home Engineering   3621892:r1269 FR1_FR2 SCHEMATIC F REV (INPUT MOSBideBidsch 4 of 5
A	В	С	D	E	F	G	Н



А	В	С	D	E	F

G	Н

Title	DS		6		
Size	Number	Rev	1		
D					
Date	Tue Jul 31, 2007 Drawn by Home Engine				
56721269233112	Ø FR1_FR2 SCHEMATIC F REV (INPUT №	10 <b>53blieEe)</b> tsch	5 of	5	
		Н			-

G