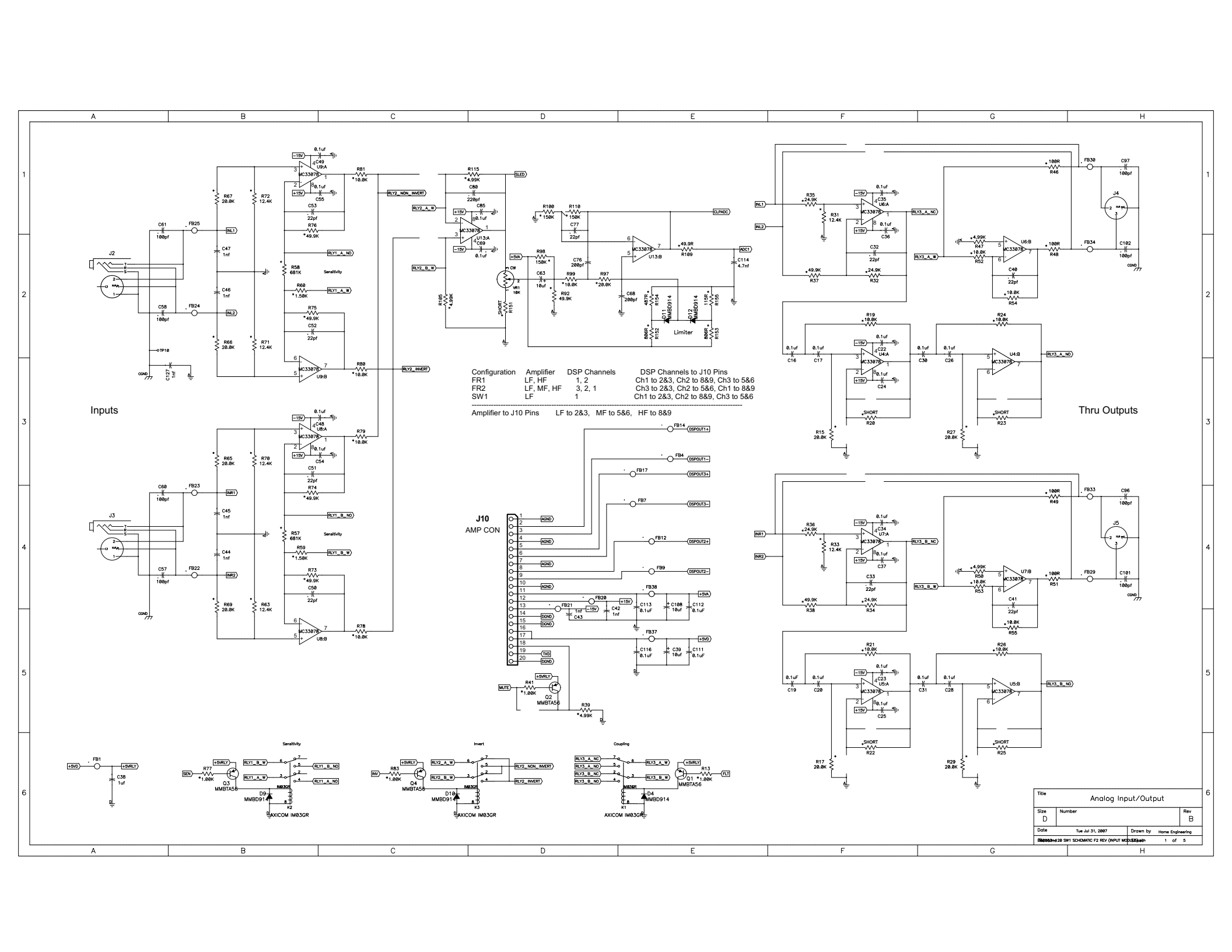
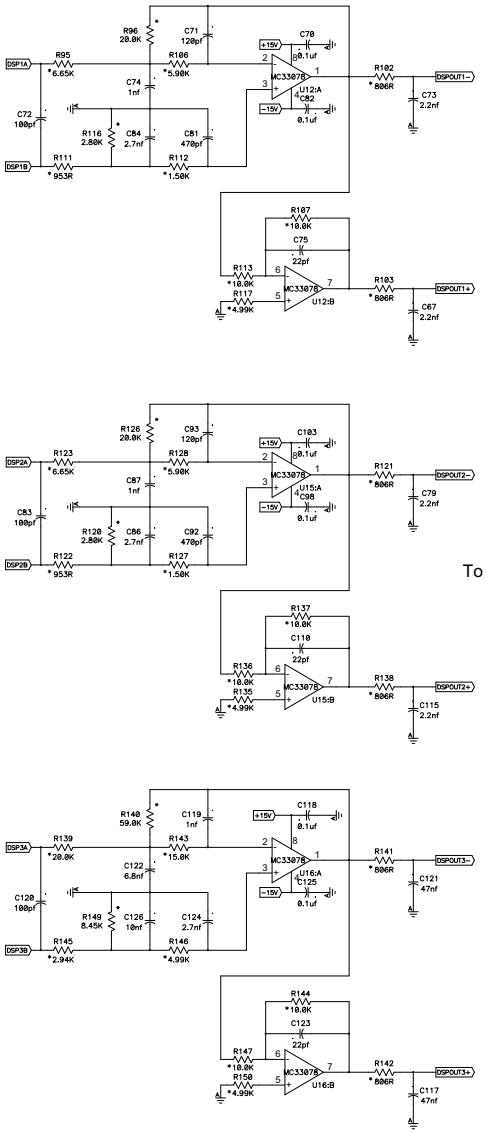
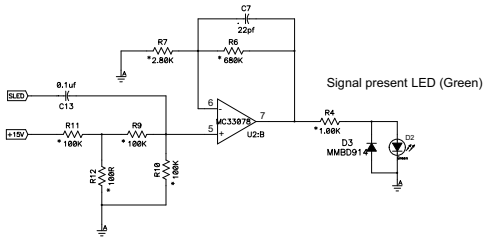

Inputs
Thru Outputs
Limiter
Sensitivity
Invert
Coupling
J10
AMP CON
Configuration Amplifier DSP Channels DSP Channels to J10 Pins
FR1 LF, HF 1, 2 Ch1 to 2&3, Ch2 to 8&9, Ch3 to 5&6
FR2 LF, MF, HF 3, 2, 1 Ch3 to 2&3, Ch2 to 5&6, Ch1 to 8&9
SW1 LF 1 Ch1 to 2&3, Ch2 to 8&9, Ch3 to 5&6
Amplifier to J10 Pins LF to 2&3, MF to 5&6, HF to 8&9
AXICOM IM03GR
Title
Analog Input/Output
Size D
Number
Rev B
Date Tue Jul 31, 2007
Drawn by Home Engineering
1 of 5

From DSP

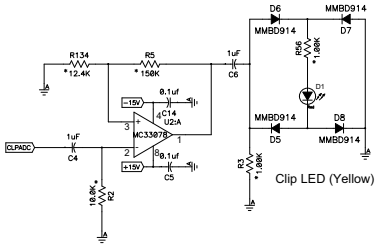


To Connector

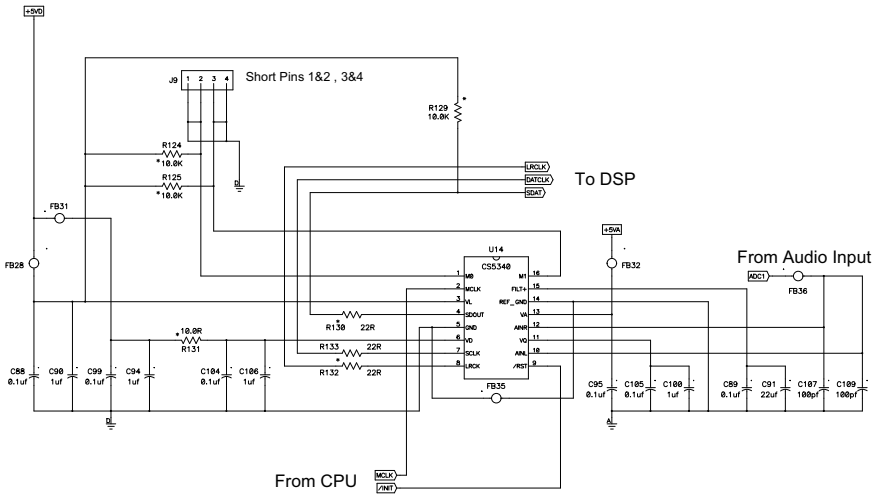
High gain (244), BW=1Khz with output offset approx +1V



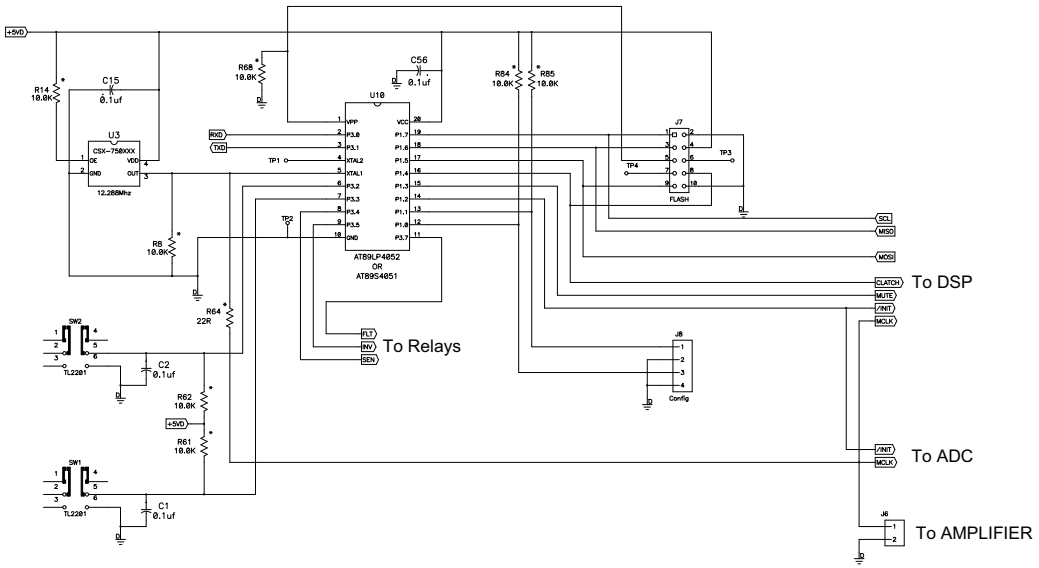
This is a comparator configuration. Monitors the ADC input (CLPADC) and when near saturation (+/- 1.20V pk) outputs a square wave
The threshold is set by the resistor network at the (+) input



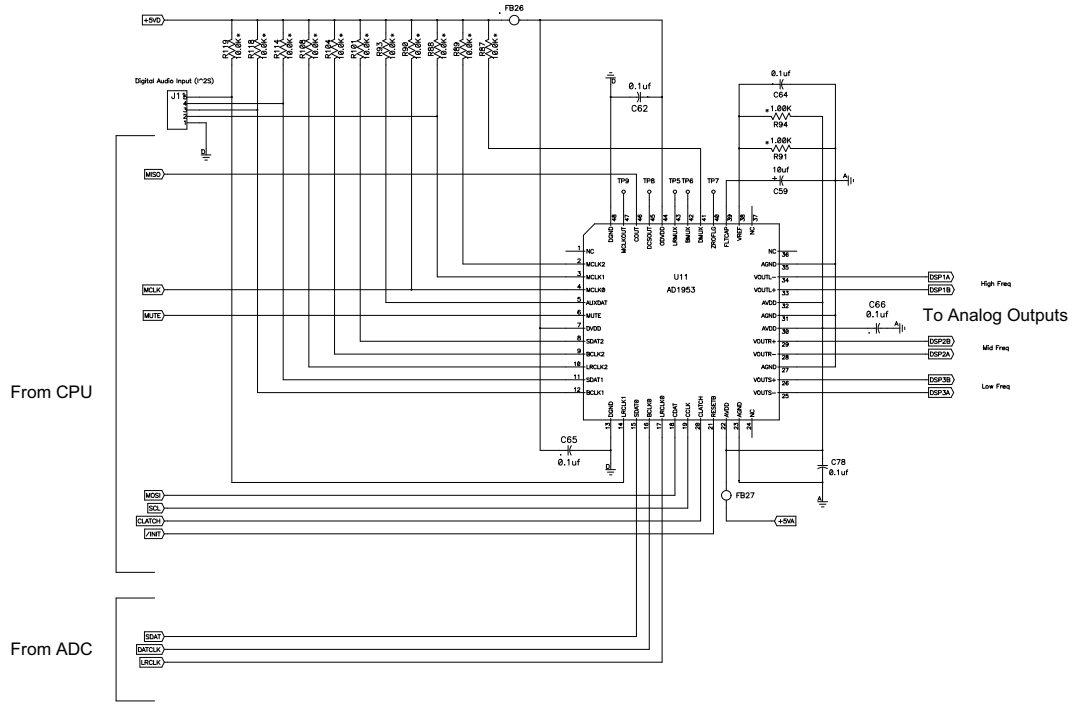
Title	Analog Filters		
Size D	Number		Rev B
Date	Tue Jul 31, 2007	Drawn by	Home Engineering
[illegible] SW1 SCHEMATIC F2 REV (INPUT MOD[illegible]			2 of 5



Title	ADC
Size: D	Number:
Rev: B	
Date: Tue Jul 31, 2007	Drawn by: Home Engineering
[illegible] SW1 SCHEMATIC F2 REV (INPUT MODULE).SchDoc	Sheet 3 of 5



Title	CPU		
Size D	Number		Rev B
Date	Tue Jul 31, 2007	Drawn by	Home Engineering
[illegible]28 SW1 SCHEMATIC F2 REV (INPUT MODULE).SchDoc		Sheet	4 of 5



Title	DSP		
Size D	Number		Rev B
Date	Tue Jul 31, 2007	Drawn by	Home Engineering
[illegible]28 SW1 SCHEMATIC F2 REV (INPUT MODULE).SchDoc		Sheet	5 of 5