Service Manual

480L

Digital Effects System

lexicon

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Obtaining Factory Service and Parts

This chapter describes how to return units for service, and how to order parts.

1.1 Returning Units for Service

***Before* returning a unit, consult with Lexicon to determine the extent of the problem.**

If you choose to return a 480L to Lexicon or a designated facility for service, Lexicon assumes no responsibility for the unit in shipment from customer to factory, whether the unit is in or out of warranty. All shipments must be well-packed (using the original packing materials if possible) properly insured and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Address
- City, state, zip code, country
- Telephone number (including area code)
- Serial number of unit
- Description of problem
- Desired return date
- Preferred method of return shipment

Please include a brief note describing conversations with Lexicon personnel, and give the name and telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, etc. with the unit.

1.2 Ordering Parts

When ordering parts, identify each part by its type, value, and Lexicon Part Number. Example:

10 kilohm rotary pot, Lexicon #200-02616

Replacement parts can be ordered from :

Lexicon Inc.
100 Beaver Street
Waltham, MA 02154 USA
617-891-6790
Telex 923 468 LEXICON WHA
FAX: 617/891-0340

Attn: Customer Service

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Description and Specifications

This chapter contains specifications and a basic description of the 480L.

2.1 Introduction

The Lexicon 480L is the most advanced digital effects system available. With its unique 18 bit linear A/D and D/A converters, the 480L produces a dynamic range of 98 dB in the wet signal path. It is probably the only effects system available that doesn't raise the noise floor of a digital master. And the PCM 1610/1630 compatible digital I/O interface lets you add true stereo ambience and effects without leaving the digital domain.

The 480L doesn't just sound better—sheer computational power allows it to perform multiple audio tasks at the same time. And what tasks! In the current glut of throwaway digital devices with ever-cheaper versions of the same sounds, the 480L offers remarkable new effects and reverb sounds.

Its innovative reverb algorithms reflect a more accurate and natural model of the acoustic and psychoacoustic phenomena of reverb and ambience. Put the 480L up against any other reverberator—you'll be amazed at the difference.

Reverb is only part of the story. The 480L produces astonishing effects you haven't even begun to dream about yet. And its sampling program offers a variety of useful and unique features.

The present software is powerful and complex, a dramatic step forward in digital signal processing technology. Yet it hasn't explored the limit of the 480L's architecture, which is itself configured for future hardware expansion.

If you are familiar with the venerable 224XL, you'll feel right at home with the LARC used to control the 480L. However, there are enough differences in the way the two units operate that we strongly suggest that you read this manual as soon as possible. In it, you'll discover that the 480L's two high speed processors can operate in a variety of configurations. Samples can be processed with reverb or effects, all in the digital domain. One 480L can serve two control rooms. Or two 480Ls can be connected through their digital I/O ports for even wider creative horizons. The 480L can even be connected to a 224XL and both units operated from a single LARC.

2.2 About the Rear Panel

Main Inputs (L & R)
The left and right Inputs accept 3-pin male XLR connectors. They are electronically balanced and (optionally) transformer isolated. Either pin 2 or 3 can be used as high, but to maintain polarity in the digital domain, pin 2 should be high. Pin 1 and either pin 2 or pin 3 of each input *must* be grounded for unbalanced operation. Input impedance is 30 kilohms in parallel with 100 pF. Inputsaccept input levels from +6 to +28 dBm.

Main Outputs (L & R)
The left and right Main Outputs accept 3-pin female XLR connectors. They are electronically balanced and (optionally) transformer isolated. Either pin 2 or 3 can be used as high, but to maintain polarity in the digital domain, pin 2 should be high. Pin 1 and either pin 2 or pin 3 of each output *must* be grounded for unbalanced operation. Output impedance is 33 ohms, and levels up to +24 dBm are possible.

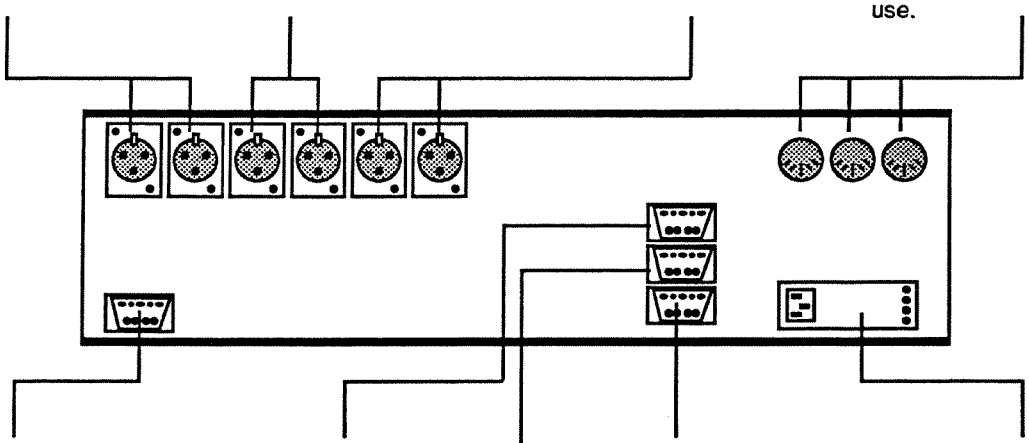
Aux Ouputs (L & R)
The left and right aux outputs are identical to the Main Outputs, except that they are used as secondary outputs when split or cascade modes are selected.

Important. Reversing polarity on either input or output connectors can produce audible phase inversion effects. Improper phasing in the stereo path can create a weak or thin mix. Make sure that inputs and outputs are wired consistently.

MIDI Connectors
MIDI IN receives MIDI information from other MIDI-equipped devices.

MIDI Thru retransmits MIDI information received at the MIDI In connector, without any change.

MIDI Out is currently not in use.



Lexicon Digital Audio I/O Connector
This DE9 connector provides PCM 1610-compatible digital I/O. It has 18-bit word length capability and can be slaved to a 48 kHz, 44.1 kHz or 44.056 kHz external word clock.

LARC 1 Connector
This DE9 connector connects the mainframe to the Lexicon Alphanumeric Remote Control (LARC) via a flexible 50-ft cable (supplied).

Automation Connector
The Automation Connector is provided for future computer control and automation features.

Important: Never connect a LARC to this connector.

LARC 2 (Thru) Connector
This DE9 connector allows connection of a second LARC to the mainframe. It also allows the 480L to be connected to a 224XL, with both units under control of one LARC. A 10-ft cable is provided for this application.

Power Connector and Fuse Holder Cartridge
The Power Connector is a standard 3-pin IEC power connector. The Fuse Holder Cartridge contains the AC mains fuse(s). The voltage changeover card is also contained in this compartment. Read Appendix A for voltage changeover information.

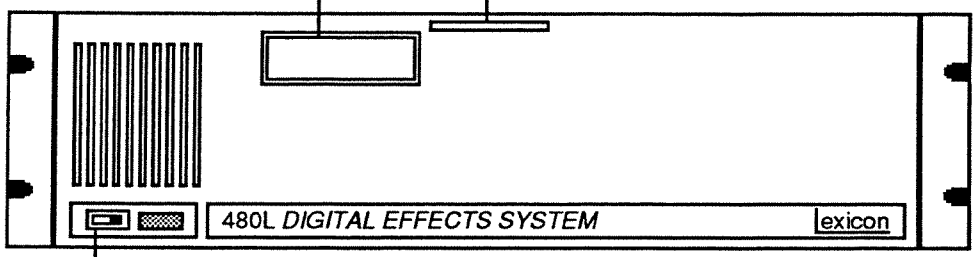
Figure 2.1. 480L Rear Panel.

2.3 About the Front Panel

Nonvolatile Memory Cartridge Slot
The 480L is shipped with one Nonvolatile Memory Cartridge, providing five banks of portable register storage. A write-protect switch prevents accidental erasure of contents.

Note: Cartridges may be shipped with the write-protect switch in the *ON* position.

Front Panel Latch
The front panel is hinged at the bottom; pull on the handle to open. Keep the front panel closed during normal operation to maintain dust filtration.



Power Switch and Indicator
The Power Switch turns the 480L on and off; the indicator lights when the unit is on. The 480L powers up in the same condition it was in when it was last turned off. A lithium battery retains the data memory when power is off or disconnected.

Figure 2.2. 480L Front Panel.

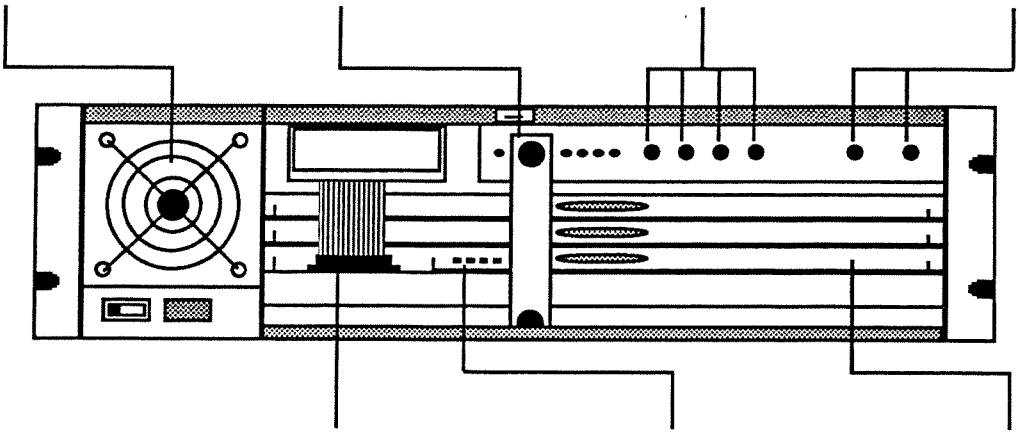
2.4 Behind the Front Panel

Cooling Fan
The cooling fan provides filtered forced air (the front panel vent is an air intake). The filter is removable for periodic cleaning.

Card Retainer
The card retainer ensures that the HSP and host processor cards remain firmly seated.

Output Level Controls
The output levels for the Main and Aux analog outputs may be adjusted independently over a range from +6 to +24 dBm (into 600 ohms) with these controls.

Input Level Controls
The input sensitivity for the left and right analog inputs may be adjusted independently to match inputs over a range of +8 to +28 dBm with these controls.



Nonvolatile Cartridge Cable
This ribbon cable connects the cartridge slot to the host processor card via a locking connector on the host processor card.

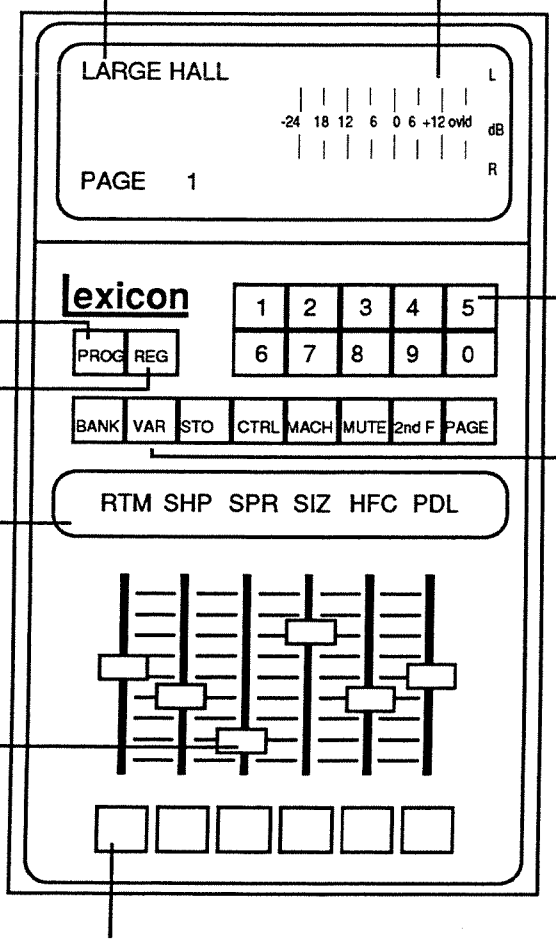
Caution: Use of excessive force when inserting cards into the 480L can result in serious damage. Always make sure that the connectors are lined up properly before applying seating force.

Diagnostic Indicators
The four diagnostic indicators on the host processor card flash briefly upon powerup.

Removable Modules
The 480L is completely modular. Every subassembly in the mainframe can be unplugged and removed for service or exchange. The standard complement for a 480L is two HSP cards and a host processor card. The cards can be plugged into any slot in the mainframe, but for best noise performance, the HSP cards should be installed in the two top slots, and the host processor card directly beneath them. The empty bottom slot is provided for future optional expansion.

Figure 2.3. Behind the Front Panel.

2.5 About the LARC



Main Display
Shows names and values for all selections.

Headroom Indicator
+12 dBm indicates analog or digital clipping. Proper input level is with +12 dB and ovld LEDs *unlit*.

Program-Select Key
Press repeatedly to scroll through programs in a bank.

Register-Select Key
Press repeatedly to scroll through registers in a bank.

Slider Display Line
Shows abbreviated names of the parameters currently under the control of the sliders. Full name appears in the Main Display.

Control Sliders
Adjust parameter values.

Slider Display Keys
Show parameter name and value in main display. Press twice to engage vernier (fine) adjustment mode in some parameters.

Also used to trigger record and play events in Doppler and Sampler programs.

Numeric Keypad
Press one of these keys to load a program selected with PROG or REG. Also used to select pages.

Function Keys
Bank scrolls through groups of programs or registers.

VAR displays the running program or register name and the machine that the LARC is controlling.

STO stores edited parameter settings in registers (when REG is pressed at the same time.

CTRL toggles in and out of the control mode.

MACH toggles between machines when Split or Cascade modes are selected, and also between the 480L and 224XL when a 224XL is connected to the 480L.

MUTE removes processed audio from outputs (only while it is pressed).

2nd F is inactive.

PAGE steps through pages of parameters.

Figure 2.4. The LARC.

2.6 Specifications

The following specifications are subject to change without notice.

2.6.1 Audio

Audio Inputs (Two)

Levels	+6 to +28 dBm; electronically balanced +6 to +28 dBm; unbalanced
Impedance	30 kilohms in parallel with 100 pF
Common Mode Rejection Ratio	>40 dB, 20 Hz to 20 kHz
Connectors	Female XLR
Transformer Option	User-installable; Jensen JE-11P-1

Audio Outputs (Four)

Levels	+6 to +24 dBm transformerless balanced (600 ohms) +6 to +20 dBm unbalanced (600 ohms) Minimum load impedance 150 ohms
Impedance	33 ohms
Common Mode Rejection Ratio	>35 dB, 20 Hz to 20 kHz
Connectors	Male XLR
Transformer Option	User-installable; Jensen JE-123-SLPC

Frequency Response*	20 Hz to 20 kHz, +0.5 dB, -1 dB
Dynamic Range*	98 dB typical over temp. range, 22.4 kHz unweighted noise bandwidth
Total Harmonic Distortion and Noise	<0.015% @ 1 kHz limit level (+18 dBm unity gain) <0.05% 20 Hz to 20 kHz @ 20 dB below limit level
IM Distortion	<0.05% SMPTE IM @ limit level
Channel Separation	>75 dB @ 1 kHz
Encoding	18 bit equivalent linear PCM
Sampling Rate	48.0 kHz/44.1 kHz -- selectable

*These specifications are for 48 kHz sampling rate setting.

2.6.2 LARC (Lexicon Alphanumeric Remote Control)

Controls	Four mode-select buttons (BANK, PROG, VAR, REG) used with ten numeric select buttons (1 to 0); a page select button (PAGE); a control program key (CTRL); a machine-select key (MACH); two auxiliary control buttons (MUTE, STO); six sliders for smooth control of up to 128 paramaters per program with associated display-select buttons
Display	Two lines of 12 alphanumeric LEDs for interactive display; additional line of 24 alphanumeric LEDs (six groups of four for each slider); dual 16-position LED headroom indicator (calibrated -24 to +12 dBm with overload warning)
Connector Type	DE9
Cable	50-ft extra-flexible cable; cables can be linked
Operating Distance	Up to 100 feet when powered from mainframe; up to 1000 feet possible with optional remote power source for LARC

2.6.3 Interface

Digital Audio Interface

Interface	PCM 1610-compatible digital I/O; 18-bit word length capability; slaveable to 48 kHz, 44.1 kHz, or 44.056 kHz external word clock
Connector Type	Female DE9
LARC Connector	Female DE9 (2) -- Dual LARC control
Mainframe Controls and Indicators	Power switch and indicator light; Left and Right input level controls, four output level controls; four LEDs for internal DC power supplies
Automation Port	Female DE9 -- for future expansion
MIDI Interface	In, Thru, Out (Standard 5-pin female DIN)

2.6.4 Power Requirements

Mainframe

Nominal	100, 120, 220, 240 Vac (+5, -10%) Switch-selectable; 50-60 Hz, 180 W maximum, 70 W typical
Protection	All secondaries fused; voltage transient suppression; overvoltage and short circuit protection on logic supply
Mains Fuse	100/120 Vac: 3AG 3 A SLO-BLO 220/240 Vac: 5x20 mm 1.6 A SLO-BLO; dual-fused
Connector	Standard 3-pin IEC power connector with rear-panel accessible mains fuse and voltage selector
LARC	10 to 24 Vdc or 10 to 18 Vac, 6.25 W; Normally powered by 480L mainframe; miniature jack accepts optional remote power supply (for operation at distances greater than 100 feet from mainframe)

2.6.5 Miscellaneous

Nonvolatile Memory Cartridge	CMOS static RAM with built-in lithium battery provides storage for registers; write-protect switch prevents accidental erasure of contents
Serviceability	Most major assemblies are modular and can be replaced in the field; hinged front panel allows access to plug-in boards, and fan filter
Diagnostic Programs	Control and display with LARC
Muting	Audio outputs are muted during power-up, power-down, power failure, or power supply failure
RFI Shielding	Ac power connector, audio connectors, and LARC cables are RFI-shielded; unit complies with FCC Class A computer equipment requirements

2.6.6 Environment

Operating Range	0 to 40°C (32 to 104°F)
Max. Storage	-30 to 70°C (-22 to 158°F)
Humidity	95% maximum without condensation
Cooling	Filtered forced air with ultra-quiet fan; filter is removable for cleaning

2.6.7 Dimensions

Mainframe	Standard 19" rack mount 19"w x 5.25"h x 14.5"d(483 x 133 x 368 mm)
LARC	5.9"w x 9.5"h x 3.2"d (150 x 242 x 82 mm)

2.6.8 Weight

Mainframe	24 lbs (10.89 kg)

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Performance Verification and Calibration Procedures

This chapter describes how to verify that the 480L meets published specifications.It also contains recalibration procedures.

Note: If you are encountering difficulties with a unit, read Chapter 11, "Solving Problems" in the 480L *Owner's Manual* before continuing with this chapter.

3.1 Performance Verification

The following tests will assist in determining whether or not a unit is operating correctly and meets published specifications. Always complete them before proceeding to calibration procedures and repairs.

3.1.1 Basic Functional Tests

Load a few programs from each bank and verify operation of parameters. Listen for sonic quality of audio processing at all outputs.

Move all level controls through their entire range and check for mechanical and audible smoothness. Verify smooth operation of all sliders and buttons on the LARC.

Verify that the LARC control head works when plugged into either LARC 1 or LARC 2 port on the rear of the 480L. If you have two LARCs connected verify that they both have control. If one LARC is used to control both a 480L and a 224XL, verify that it is correctly controlling both units.

Verify that the 480L can be controlled from an external MIDI controller. Be sure to assign the proper MIDI channel. Set the program change mode to fixed. Select some presets on the controller and verify that the 480L responds by changing programs or registers. Verify that the MIDI Thru jack works by connecting it to another MIDI device and noting operation.

Try passing digital 1610 compatible audio to the 480L and verify that the analog output from the 480L is clean. Pass digital audio out of 480L to a 1610-compatible device and verify that the audio is clean.

Verify that the RAM cart door hinge operates smoothly and closes when cart is removed.

Verify that the front panel opens and closes smoothly and latches tight.

Verify that the power indicator on the front panel lights when power is turned on and that the fan is operating. Also verify that the power indicators behind the front panel light.

3.1.2 Performance Tests

The following equipment is required to complete the performance tests:

1. Variac
2. Digital multimeter
3. Low distortion sinewave oscillator (0.001% THD)
4. Dual trace oscilloscope (100MHz bandwidth)
5. T.H.D. & N distortion analyzer/level meter (switchable audio band pass filtering)
6. 1610/1630 digital audio device or second 480L
7. Non Volatile RAM cartridge
8. High quality music source/monitor system
9. 480L *Owners Manual*
10. Load capable of sinking 10 amps @ 5vdc
11. Misc. cables

3.1.3 Power Supply

Initial Setup

480L powered up, in Single configuation, In_Out program loaded (bank 9, program 1) and 48kHz sample rate selected.

1. The normal operating line voltages are l00V, l20V, 220V, or 240V All line voltages should be +5/-l0% of their nominal value.

Note: When shipped from the factory, all units have the line voltage setting labelled on the rear panel.

2. Power up 480L with a variac to the nominal voltage. Current drawn by 480L should be <0.9 A (AC).

3. For the following measurements check voltage with reference to the supply's gnd.

Location or Pin #	Ground	DC Specification	DC Voltage
Right C7	Left C7	(4.85-5.15)	+5*
TP6.1	TP6.2	(4.75-5.25)	+5 analog*
CR20 Cathode	TP6.2	(4.75-5.25)	+5 A/D
TP6.6	TP6.5	(14.25-15.75)	+15*
TP6.4	TP6.5	(14.25-15.75)	-15*
TP1 square pad	TP1 round pad	(22.0-27.0) unregulated	+20 LARC

**Reduce line voltage with variac by 10% and repeat.*

Table 3.1. Voltage Ranges.

4. For the following measurements use a scope to measure ripple.

Location or Pin #	Ground	Nominal Voltage	Ripple
cathode of CR7 (motherbd)	GND TP6.5	+21V unregulated	<1.5Vp/p
anode of CR11 (motherbd)	GND TP6.5	-21V unregulated	<1.5Vp/p
P2.2 (pwr supply bd)	GND P4.1 or 2	+28V unregulated	<2 Vp/p

Table 3.2. Power Supply Ripple.

5. For the following measurements use a noise meter with a low pass audio band pass filter.

Location or Pin #	Power Supply	Measured Noise
TP6.1 (gnd @ TP6.2)	+5 AN	< .5 mV
TP6.6 (gnd @ TP6.5)	+15V	< .5 mV
TP6.4 (gnd @ TP6.5)	-15V	< .5 mV
Right side C7 (gnd @ left side C7)	+5 Dig	< 3.5mV

Table 3.3. Measured Noise.

Testing the +5 Vdc supply load capabilites requires a variable load capable of sinking 10 amps. See Section 3.2, *Calibration* for more information.

The 480L is factory calibrated to have +5vdc switching supply foldback @ 8.5 amps. Connect the variable load and monitor voltage and current with meters.

6. Power on the 480L and check the +5vdc supply. It should be between 4.85-5.15 Vdc. Slowly increase the load until the ammeter indicates 8.5 amps. The voltage should drop at this point (foldback). If the supply does not foldback at 8.5 amps, see the calibration procedure before proceeding any further.

7. Short the +5V supply. Verify <1.0 Amp.

8. Remove the short and lower line voltage -10% from nominal. Increase load to just before foldback which is 8.5 Amps, verify 4.85-5.15V, and quiet operation.

9. Set load for minimum loading and increase line voltage +5% above nominal, verify 4.85-5.15V.

10. Set the 480L's sampling frequency to 44.1kHz. Verify a 22.7 us period across C9 on the power supply board (see Figure 3.1). Check for +5 4.85 - 5.15V and quiet operation. Remove load and return to normal operation.

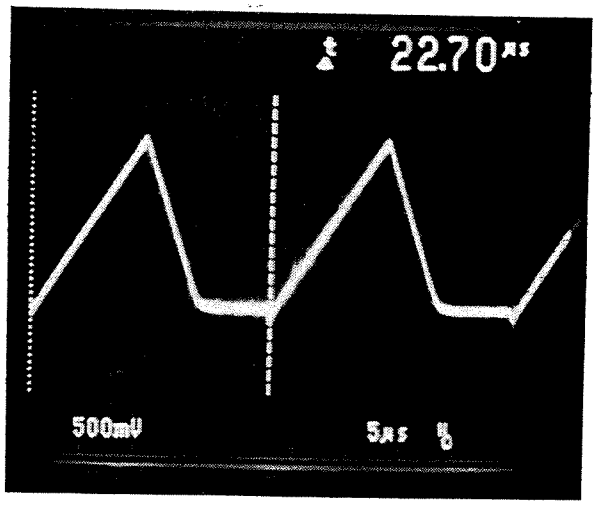

Figure 3.1. 22.7 uS Sync Signal Across C9 on Power Supply.

3.1.4 Audio Functional and Level Control Tests

Initial Setup

Use of Tektronix 5000 or 500 series instruments or equivelent are recommended for audio performance tests. Connect the Sync Output of the Oscillator to the external trigger of an oscilloscope, and the Function Output of the Distortion Analyzer to one of the scope's input channels. The oscillator should be initialized as follows:

Waveform: Sine. Frequency: 1 kHz. Level: 1 Volt. Output Impedance: 600 ohms, Balanced.

The distortion analyzer should be initialized as follows:

Input Level: Auto-range, Function: Level. Scale: Volts. Distortion: Auto-range.
Filter: 80kHz Low-pass and audio band pass on.

All audio performance tests are based on transformerless 480L and 48kHz sample rate.

Power on the 480L and set all level controls to minimum (full ccw). Set meter to read dBm with audio band pass on. Place jumpers on motherboard W1 and W2 to RUN position, set sample frequency 48kHz, load IN_OUT program, and set configuation to Single.

1. Input +28 dBm @ 1kHz to right and left inputs. Expected output from all outputs into 600 ohms is +4.6 dBm ±0.6 dBm. Remove W13 (ground).

2. Terminate input and check noise of all output stages (LLA5200), expected to be < -83 dBm. Replace W13 (ground).

3. Set all level controls to maximum (full cw). Input -4dBm @1kHz to left and right inputs. Expected output is +17dBm ±0.5 dBm into 600 ohms.

3.1.5 Input CMRR (Common Mode Rejection Ratio)

Initial Setup

Set all level controls full clockwise.

1. Prepare CMRR input cables so pin 2 and 3 of XLR have same signal and pin 1 is ground.

2. Using CMRR cables, input -4 dBm @ 1 kHz. Expected output < -20 dBm Verify the same for 20 Hz-20 kHz. Check both left and right channels.

3. Remove CMRR cables. Return to balanced input.

3.1.6 Frequency Response

Initial Setup

Remove the audio band pass filter from meter input. Set all level controls full clockwise.

1. Input 1 kHz and adjust input levels so the 0dB headroom LEDs are just on.

2. Sweep the oscillator from 20 Hz to 20 kHz. Verify that the unit meets specification (+.5 dB / -1 dB from1 kHz reference) at all outputs. Refer to sample plot in Figure 3.2.

3.1.7 T.H.D. + Noise

Input Setup

Input oscillator (200Hz, 18dBm) into the 480L and set right and left input level controls to just below limit. (Use a distortion meter for accuracy.) Set all outputs to +24dBm into 600 ohms.

1. Check the following on all four outputs, with audio band pass filter in. Do not touch the level controls once set as above.

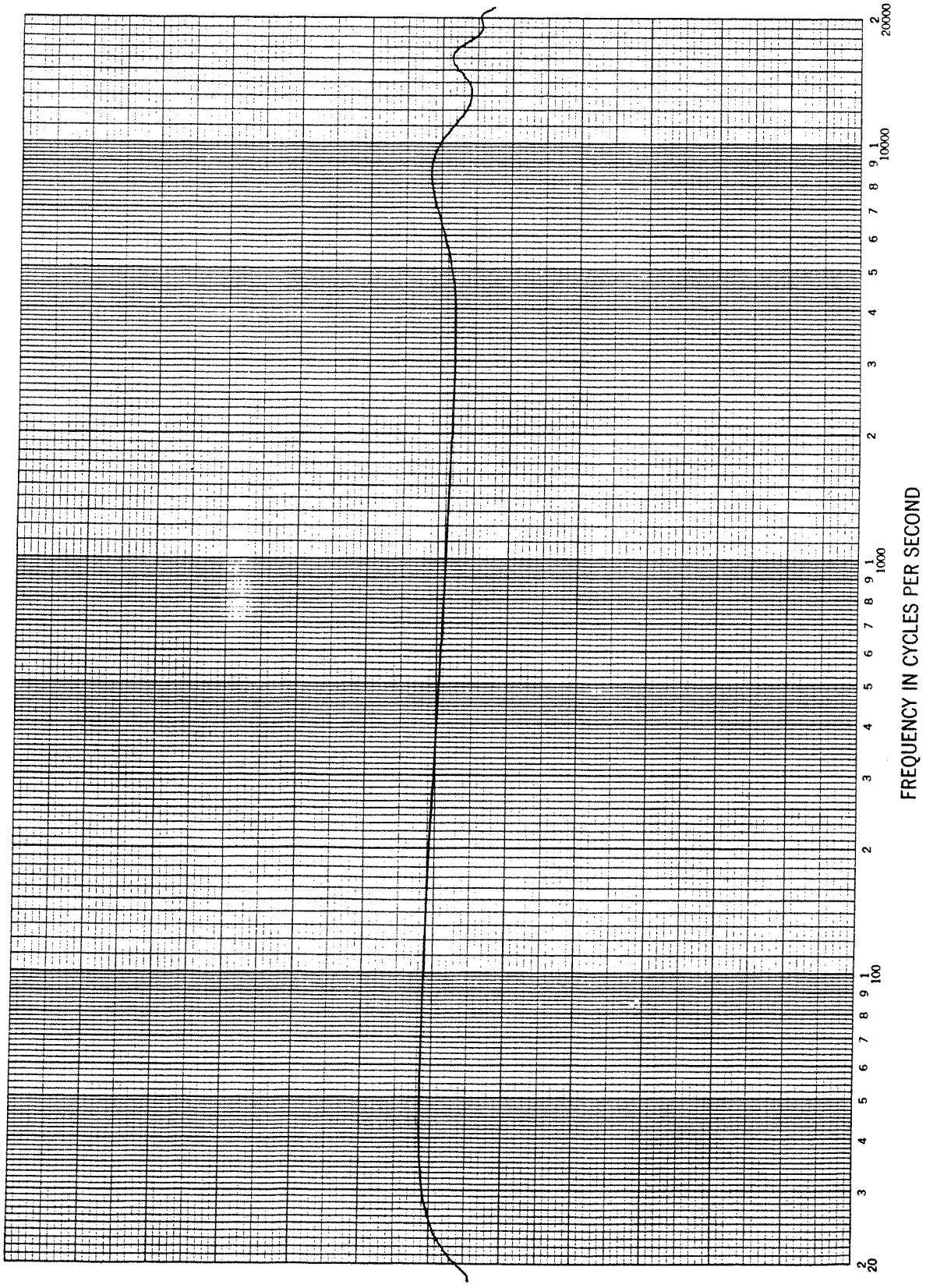

Figure 3.2. Through 480L System - 1 Channel - 1 dB/in.

Input	Output THD+Noise
+18dBm @ 20Hz	< 0.015% THD+N
+18dBm @ 200Hz	< 0.015% THD+N
+18dBm @ 1KHz	< 0.015% THD+N
+16dBm @ 10kHz	< 0.05% THD+N
+16dBm @ 20kHz	< 0.1% THD+N
-2dBm @ 20kHz	< 0.05% THD+N
-2dBm @ 10kHz	< 0.05% THD+N
-2dBm @ 1kHz	< 0.05% THD+N
-2dBm @ 20Hz	< 0.05% THD+N
+16dBm @ 7kHz IM 60Hz	< 0.05% SMPTE IMD
-2dBm @ 7kHz IM 60Hz	< 0.10% SMPTE IMD

Table 3.4. T.H.D. + N at various levels and frequencies.

2. Terminate input to 480L. Measure noise (dynamic range). It should be <-66 dB. Dynamic Range should be 90 dB minimum.

3.1.8 150 Ohm Load Test

Initial Setup

Input oscillator (200 Hz, +18 dBm) into the 480L and set the right and left input level controls to just below limit. (Use a distortion meter to make this adjustment accurate.) Set all outputs to +24 dBm into 600 ohms. Change output load to 150 ohms. Change input to +12 dBm @ 1 kHz.

1. Measure output from 480L. It should be +16.68dBm ±0.79 dBm.

2. Measure T.H.D. at the same level. It should be < 0.02%.

3. Repeat for all four outputs.

3.1.9 Crosstalk Tests

Initial Setup

Input oscillator (1 kHz, +18 dBm) into the 480L and set right and left input level controls to just below limit. Use a distortion meter to make this adjustment accurate. Set all outputs to +24 dBm into 600 ohms. Change input level to +12 dBm @ 1 kHz. Terminate right input.

1. Input +12 dBm to left input, verify right main output @1 kHz is < -57 dBm. Verify right aux. output @1kHz is < -57dBm.

2. Move motherboard jumpers W1 and W2 to ST (self test) position.

3. Verify that the right aux. output @1 kHz is < -57 dBm.

4. Verify that the left aux. output @1 kHz is < -57 dBm.

5. Return input to the right input and terminate the left input.

6. Input 12dBm to right input, verify right main output @1 kHz is < -57 dBm.

7. Verify that the left main output @1 kHz is < -57 dBm.

8. Move jumpers on motherboard (W1 and W2) to RUN position.

9. Verify that the left main output @1 kHz is <-57 dBm.

10. Verify that the left aux. output @1 kHz is <-57 dBm.

3.1.10 System Test

1. Make sure that the unit passes power-on diagnostics. See the diagnostics in Chapter 5, *Troubleshooting Guide* if a failure is indicated.

2. Check both LARC ports L1 and L2 by powering up system using both ports.

3. Check digital input at 44.1kHz and 48kHz, using another 480L or 1610/1630 device.

4. Check RAM Cart by storing and loading registers if space is available.
5. Test Automation Connector if option available. (Not implemented in V1.23 software.)

6. Check batteries on Host with power off. Voltage should be ≥2.50 VDC (measured at BT1 and BT2). A reading lower than 2.5 VDC indicates that the battery should be replaced.

7. Check current drain on batteries by measuring voltage across R14 (BT2) and R12 (BT1). It should be <.5 mV.

8. Check U49 pin 1 (RAMBUFEN) on Host board to make sure it is low with power off.

9. Power 480L from variac at nominal voltage. Load a program, note program, lower variac to 30% of nominal then return to nominal. The 480L should reset and return to the same program. If it doesn't, check power fail calibration (see calibrations).

10. Verify that all programs are present for the version installed (refer to *Owners Manual*). Carefully listen to all programs.

11. Verify that the headroom indicators are operating correctly. If they are not, refer to calibration procedures.

12. Verify that the overload indicators light if overdriven in running reverb program.

13. Verify correct Mute operation during power up/down and when running a program. It should be a clean mute without any clicks or pops.

14. Check and verify that you can run two reverb (2 processer) programs if the second HSP option is installed. (use mono split, stereo split or cascade configuation)

3.1.11 LARC Tests

Initial Setup

Press PAGE and hold then press PROG to enter diagnostics. Press page to display different tests. Press PROG to execute selected test.

1. Perform "slider test" LARC
2. Perform "button test" LARC
3. Perform "display test" LARC (3 varieties) Press PAGE to select different display.
4. Perform "voltage test" LARC

Note: V1.23 and V. 2.00 do not perform Serial test, Tape out and Drop out tests; these are supported only with the LARC connected to Lexicon 224XL)

3.1.12 Tape Interface Test

Not available in 480L, used in 224XL only.

3.2 Calibration

Calibration should not be necessary unless a component in a particular circuit has been changed.

3.2.1 PLL Test and Calibration

This procedure requires a 1610 compatible digital audio for calibration of phase lock loop (PLL). Connect the1610 to the 480L under test with the HOST board on an extender card (Lexicon # 021-04938). Attach one probe to U96 (Rev 1), or U92 (Rev 2 and up) MC4044 pin 1 (WCI/) and the other probe to pin 3 (WC/). Set 480L to recieve digital audio and verify the two signals are in sync and pin 12 (PLOCK) is high. If not, adjust C76 on the Host board until this is true. Check and verify sync at 44.1 and 48 kHJz.

Note: The 1610 interface will not work properly if a poor cable is used. Lexicon recommends use of a twisted pair cable.

3.2.2 + 5 VDC Power Supply Calibration

Note: Some early units had the foldback set at 10A (normal setting = 8.5 A). This procedure requires a variable load capable of sinking 10 A.

1. Unplug all boards (minimum load +5 VDC). Turn R5 and R11 CCW on power supply.

2. Attach scope gnd. clip to top side of C9 and probe bottom of C9. (this is the timing cap for the oscillator section of U1 on power supply).

3. Turn R11 CCW and set for approximately 5us fall time on scope. Sawtooth waveform should approach 70% duty cycle. (see Figure 3.3.)

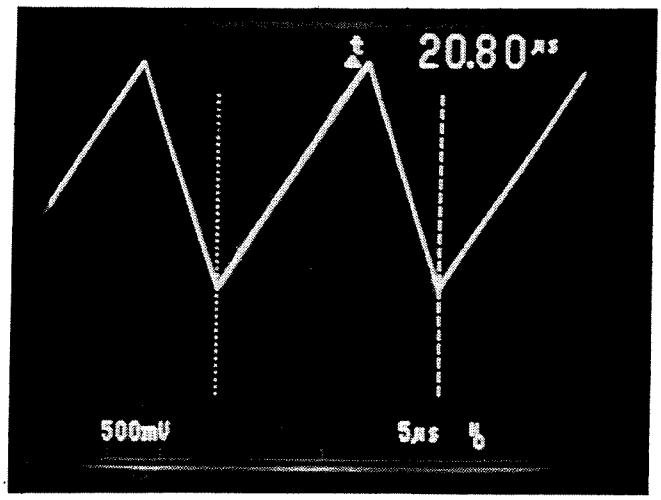

Figure 3.3. 20.8 uS Sync Signal Free Running Across C9 on Power Supply.

4. Verify 20.8 us period across C9.

5. Return plug in boards to backplane and power up 480L with load set to minimum.

6. Slowly increase load to 8.5 A. Turn R5 CW until foldback begins (voltage begins to drop).

7. Increase loading and verify that voltage continues to drop, and current does not exceed 8.5 Amps.

8. Reduce loading to 8.0 A and verify 4.85 - 5.15 V.

3.2.3 Power Fail Calibration

1. Connect power cord and power up with with the load on +5 VDC supply adjusted to 8.0 A.

2. Set variac voltage -20% from nominal, clip scope probe to right side of R30 (PF/) on motherboard. Trim R32 (PWR-FAIL ADJUST) so that PF/ begins to pulse low (due to ripple on the secondary).

3.2.4 Converter Calibration

Initial Setup

Use of Tektronix 5000 or 500 series instruments or equivalent is recommended for audio performance tests. Connect the Sync Output of the Oscillator to the external trigger of an oscilloscope and the Function Output of a Distortion Analyzer to one of the scope's input channels.

The oscillator should be initialized as follows:

Waveform: Sine. Frequency: 1 kHz. Level: 1 Volt. Output Impedance: 600 ohms. Balanced.

The distortion analyzer should be initialized as follows:

Input Level: Auto-range. Function: Level. Scale: Volts. Distortion: Auto-range.
Filter: 80kHz Low-pass and audio band pass on.

The input channels will be referred to as L-IN for left and R-IN for right. They should be driven simultaneously, unless otherwise noted. All output channels (herein referred to as LM-OUT (left main), RM-OUT (right main), LA-OUT (left auxiliary), and RA-OUT (right auxiliary) are to be loaded with 600 ohms, unless otherwise noted.

On the motherboard, put W3 and W4 in RUN position, and W13 (ground jumper) installed, W1 and W2 set to self test.

1. Set both input level controls to minimum. Turn trimpots R214 and R224 (Window Adjust) full ccw. Set sample frequency to 48 kHz.

2. Input 18 dB @100 Hz to left. Increase L-IN until the onset of clipping and back off slightly. Move W3 to CAL position Set LM-OUT to +24 dBm.

3. Measure T.H.D. at the left main out, trim R149 (L-Ch Gain) and R127 (L-CH offset) for minimum distortion (<0.015% THD+N).

4. Input 18 dB @ 10 kHz to left. Slowly turn R214 (L-Ch Window) cw until large spikes begin to appear in the distortion product <0.05% THD+N.

5. Input 18 dB @100 Hz to right. Increase R-IN until the onset of clipping and back off slightly. Move W4 to CAL position. Set RM-OUT to +24dBm.

6. Measure T.H.D. at the right main out. trim R146 (R-Ch Gain) and R121 (R-CH offset) for minimum distortion (< 0.015% THD+N).

7. Input 18 dB @ 10 kHz to right. Slowly turn R224 (R-Ch Window) cw until large spikes begin to appear in the distortion product < 0.05% THD+N.

8. Calibration of offset trim both channels: (terminate L/R inputs). Probe MSB pin 1/U45 and adjust R121 for 50% dither on scope. See Figure 3.4. Measure voltage at wiper of R121 (south side of R120) and then adjust R121 for a 1.00 Volt decrease below (negative) what it was at dither.

9. Probe MSB pin 1/U47 and adjust R127 for 50% dither on scope. Measure voltage at wiper of R127 (south side of R126) and then adjust R127 for a 1.00 Volt decrease below (negative) what it was at dither.

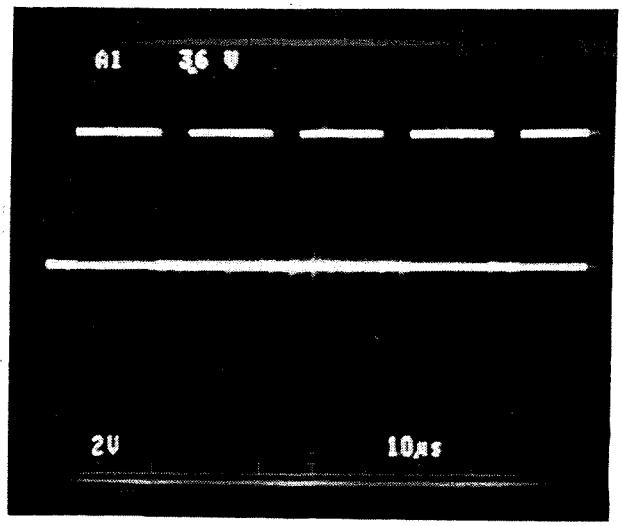

Figure 3.4 Converter Calibration Dither.

4

Circuit Description

This chapter is a guide to the organization and function of the various circuit blocks within the 480L. It is provided as an aid to qualified service personnel and is not intended to serve as a primer in digital and analog circuitry.

Note: Throughout this chapter, three different methods are used to indicate hexadecimal numbers:

474FH
10h
$C0015

All of these indicate a hexadecimal number.

4.1 Organization

The circuit descriptions are presented in the following order:

4.2 HSP (High Speed Processor) board
4.3 Host Processor - Rev. 1
4.4 Host Processor - Rev. 2 and up
4.5 Motherboard
4.6 Power Supply
4.7 LARC
4.8 SME board (Optional)

4.2 High Speed Processor Board

4.2.1 Overview

The HSP board is a digital signal multiprocessor system composed of two identical self-contained signal processing subsystems. Each subsystem has five functional sections:

1) Slave Processor
2) Writable Control Store
3) Microcode Pipeline
4) Digital Signal Processor
5) Digital Audio I/O

The Slave Processor receives programs from the host processor board, which writes them into the slave's memory using Direct Memory Access (DMA). After a program is written the slave is released and executes the program in its memory.

The slave first writes the microprogram for the Digital Signal Processor (DSP) into the Writable Control Store (WCS). Thereafter the slave dynamically updates the microcode store with new values of offsets and coefficients. The slave accesses the WCS during one of the four phases of the the high speed processor. During the three remaining phases, microcode is read from the WCS and passed into the microcode pipeline. The pipeline aligns the microcode bits in order to drive the DSP. The microword is composed of 48 bits which provide offset, coefficient, and control information.

The DSP is composed of the arithmetic unit, the memory management unit and the audio memory. All audio information is passed into or out of the DSP via the Digital Audio I/O section. The I/O section allows each of the audio processors to access the shared audio bus. Each of the processors can write to or read from other signal processors on the bus, write to or read from the D/A or A/D, or write to or read from the transfer registers. Each of the five sections will be discussed separately in the following text.

4.2.2 Slave Processor

The Slave Processor is a 4 MHz version of the Z80. It receives all operating system code via a DMA link to the Host Processor board. U1 and U2 provide address buffering, U3 provides data buffering and one half of U41 provides control buffering for Slave processor #1. Similarly U16 and U17 provide address buffering, U18 provides data buffering and the other half of U41 provides control buffering for Slave processor #2. The scenario for the downloading of code (both operating or music programs) is as follows.

The Master issues a DMAREQ/ to the appropriate slave. The slave upon relinquishing control of the bus issues a BUSACK/ which signals the host that the bus is free and also enables the tristate buffers onto the slave's environment enabling the Master to write to the Slave RAM. Once the Master has finished the desired download, the Slave is released and continues either at the point where it left off or the Slave can be reset to start from a known point. In order to smoothly initiate the slaves upon power up, a quad latch is provided (U30). This latch is cleared upon power on placing all slaves into the reset condition. The Master can now individually load each of the slaves with the appropriate code by first releasing the reset and immediately requesting the bus. Once a particular slave has received its code, the Master can again place it into the reset condition and continue loading the other slave memories. After all slaves have been loaded, the Master can release all the slaves simultaneously. U30 also provides the Master with the ability to interrupt each of the slaves individually.

The sole purpose of the Slave processor is to provide dynamic updating of the microcode program running the DSP. In order to synchronize the Slave with the running micro program a WAIT state generator has been provided. When the Slave writes to a particular address (see memory map) WAITEN on U20 strobes high, providing a clocking edge to U43. This places the Slave into a wait state. The WAIT state is removed when PCCLR/ goes low signalling the beginning of the next sample period.

One of the more elegant features of the Slave interaction with the WCS is that the Slave essentially steals one of the phases of the DSP in order to write to or read from the WCS. The WCS appears as a dual ported memory in which one fourth of the time is devoted to the

Strobe	Address	Function
RAM0/	0000H-1FFFH	ENABLE 8kx8 STATIC RAM
DABRD/	2000H-3FFFH	READ DAB TO SLAVE
BANKA/	4000H-47FFH	WCS BANKA
PGSEL/	4000H	SELECT CURRENT HSP PAGE
IOEN/	4001H	ENABLE I/O LATCHES & BUFFERS & CPCC/, CURRENT POSITION COUNTER CLEAR
SLAVEINT/	4002H	SLAVE INTERRUPT STROBE TO HOST
WAITEN	4003H	ENABLE SYNCHRONIZING WAIT STATE
	4800H-5FFFH	NOT USED
BANKB/	6000H-67FFH	WCS BANKB
	6800H-7FFFH	NOT USED
	8000H-FFFFH	NOT USED

Table 4.1. Memory Map.

Slave and three fourths of the time is taken by the DSP. More will be said about this feature in the section on the WCS. Memory decoding is provided by U6 on Slave #1 and by U33 on Slave #2. See the memory map in Table 4.1.

4.2.3 Clock Generation

The 480L uses a four phase clock to drive the HSP and micro pipeline, provide addressing to the WCS and to allow the slaves access to the WCS during one of these phases. The four phases MPH<A/:D/> are generated using D-flip flop U102 and ROM U103. The outputs of U103 are latched in U104 to provide minimum clock skew between MC and each phase. ZCLK is also derived from ROM U103 and latched by U104. The ZCLK is one fourth the MC frequency and because it is latched along with the phase clocks, it is in phase with the DSP.

4.2.4 Writable Control Store

The WCS is composed of two banks, A & B. Each bank consists of two pages in one 2k x 8 static RAM. The WCS appears as a dual port memory to the Slave and DSP. The dual porting of the RAM is accomplished as follows:

As explained above in the clock generation section, the 480L is a four phase machine and the Slave's clock is synchronized with the start of phase A/. Because of this synchronization, the WCS appears as a dual port memory. When the Slave wants to write to the WCS, it simply writes as though the memory were its own. During phase A/, address muxes U10, U11 and U12 or muxes U37,U38 and U39 are enabled allowing the Slave address bus access to the WCS. During a write, the enable pins on U23 (bank A) or U25 (bank B) are pulled low allowing data to be passed to the WCS. Decoding of the WR/ and BANK1/ is provided by U8 and U21. During a memory read, everything above applies but data is now latched by U22 or U24. The data must be latched to provide correct data read timing to the Slave. The output enable and clock signals are provided by decoding RD/ and BANK1/ with U8 or U21.

During phases B/, C/, and D/, the DSP is allowed access to the WCS. All muxes mentioned above are selected for the program counter. PC<0:6> is enabled onto the WCS address bus. The DSP always reads the WCS and therefore WR/ on U21 and U8 is always high during these three phases. PCCLR/ provides synchronization of the reset of the program counter to the beginning of the sample cycle. The program counter will normally count to 79 decimal and then be reset. U9 and U36 are the counters used to provide the PC which are clocked at the end of phase D/. A feature provided with the WCS is the ability of the Slave to choose which half of bank A and B that the microcode is being read from to run the DSP. Slave data bit zero is used to select the bank page in conjunction with PGSEL/ and OP/. U7 or U34 provide the latching of the page select. A memory map of the WCS is provided in Table 4.2.

Bank	Address	Byte	Page
A	4000H-40FFH	STROBE DECODE	1
A	4100H-41FFH	NOT USED	1
A	4180H-41DFH	4	1
A	41E0H-427FH	NOT USED	1
A	4280H-42DFH	2	1
A	4300H-434FH	0	1
A	4350H-457FH	NOT USED	1
A	4580H-45DFH	4	2
A	46E0H-467FH	NOT USED	2
A	4680H-46DFH	2	2
A	4700H-474FH	0	2
A	4750H-47FFH	NOT USED	2
B	6000H-617FH	NOT USED	1
B	6180H-61DFH	5	1
B	61E0H-627FH	NOT USED	1
B	6280H-62DFH	3	1
B	6300H-634FH	1	1
B	6350H-657FH	NOT USED	1
B	6580H-65DFH	5	2
B	65E0H-667FH	NOT USED	2
B	6680H-66DFH	3	2
B	6700H-674FH	1	2
B	6750H-67FFH	NOT USED	2

Table 4.2. WCS Memory Map.

Because the WCS is read and write accessible to the Slave processor, the unused blocks of memory can be used by the Slave for storage or scratch pad memory.

the ARU. Eight bits are used to specify a value from 0 to 255. The coefficients can be loaded in one read cycle from the WCS, facilitating rapid ramp up and ramp down of coefficients. Hardware is provided in the pipeline to align the micro bits of the coefficients and the associated control bits needed to drive the ARU through the series of multiplies. These control bits are contained in byte 3 of the microword. They are:

RA10,RA00. Read address for the register file in the ARU used in a single precision multiply, and all cycles of n-precision double precision multiply except the last cycle.

CLKEN/. Enables clocking of U79 and U80 thru U116. The clock is always enabled on a single precision multiply and enabled on all cycles of n-precision multiplies except the last cycle. It also selects the register to be used during the current multiply cycle. A 0 enables U79 which is used during all single precision multiplies and all cycles of n-precision multiplies except for the last cycle. A 1 enables U80 which is used for the last cycle of the n-precision multiplies.

SHORT/. Signals the timing ROM that the result of the current n-precision multiply will be used as the source to the n-precision multiply which is to follow.

RA01,RA11. Register file address for the last cycle of a n-precision multiply.

ENACC/. During the last cycle of an n-precision multiply this bit determines whether to accumulate or not.

Byte	MS							LS
0	7	6	5	4	3	2	1	0
1	15	14	13	12	11	10	09	08
2	C7/	C6/	C5/	C4/	C3/	C2/	C1/	C0/
3	SIGN	ENACC/	RA11	RA01	SHORT/	CLKEN/	RA10	RA00
4	IORD/	IOWR/	SLVWRT/	WADB 4	WADB 3	WADB 2	WADB 1	WADB 0
5	MWR	MCEN/	OP/	XCLK/	DP/	ACC/	WA1	WA0

Table 4.3. 48 bit Microword.

4.2.4 Microcode Description

The microcode for the 480L is a 48 bit microword. The composition of the microword is shown in Table 4.3. All even numbered bytes reside in bank A of the WCS while all odd bytes reside in bank B.

The first two bytes (0 and1) are used to specify the offsets to the MMU. These offset bytes are latched directly into the MMU at the end of micro phase B. Byte 2 is used to specify the coefficients for the multiply in

SIGN. Determines the sign of the coefficient during the last cycle of an n-precision multiply.

Byte 4 contains the five Wet address bits used by each HSP to address all I/O ports in the system. A total of 32 addresses for I/O are provided. The I/O map is provided in Table 4.4.

Hex Address	I/O Function
10h	READ WET CH0
11h	READ WET CH1
12h	READ WET CH2
13h	READ WET CH3
14h	READ WET CH4
15h	READ WET CH5
16h	NOT USED
17h	NOT USED
18h	D/A PRIMARY LEFT
19h	D/A PRIMARY RIGHT
1Ah	D/A SECONDARY LEFT
1Bh	D/A SECONDARY RIGHT
1Ch	A/D IN LEFT
1Dh	A/D IN RIGHT
1Eh	WRITE XREG
1Fh	READ XREG

Table 4.4. I/O Map.

The two most significant bits of byte 4, IORD/ and IOWR/ indicate a read or write operation during a I/O operation. A detailed description of the I/O operations will be given below. The last byte of microcode (byte 5) contains the remaining control bits for the DSP. These bits are:

WA1,WA0. Register file write address

ACC/. Determines the source of the multiply or the source of the accumulate. ACC/ = 0 specifies the source as the register file. ACC/ = 1 specifies the accumulator.

DP/. Indicates a double precision multiply or an n-precision multiply. DP/ = 0 indicates either the first cycle of a double precision or any cycle of a n-precision multiply other than the last cycle where DP/ = 1.

XCLK/. Transfers the accumulated result in the ARU accumulator to the transfer register in the ARU

OP/. Indicates an I/O instruction enabling the HSP address buffer page selection onto the WET address bus and WET control bus

MCEN/. Memory control enable. Is used to enable audio memory read and writes in conjunction with MWR. A 0 allows audio read or writes.

MWR. Purposes depends on the level of MCEN/. Table 4.5 shows the different possibilities.

MWR	MCEN/	Operation
0	0	Audio memory read, disable output of ARU transfer register
0	1	used on I/O reads
1	0	Audio memory write, enable output of ARU transfer register onto DAB
1	1	used for I/O writes and to pass the ARU transfer register to the ARU register files

Table 4.5. MCEN Operations.

4.2.5 Microcode Pipeline

The microcode pipeline aligns the microcode for driving the digital signal processor through the phases of operation. The offset information is latched directly into the MMU and therefore requires no additional phase alignment. The remaining thirty-two bits of microcode must be extensively realigned. Latches U70, U71, U83 and U84 or U99, U100, U118 and U119 represent the beginning of the pipe. Coefficient information and several control bits are latched out of the WCS during phase C. This information is passed on to U79 and U80 and then to U78 or to U114 and U115 and then to U113. I/O information is latched in U71 or U100 and then relatched in U106 or U107. These I/O bits are global control and address bits for the WET busses. U109 is provided to handle the control bits in a local sense. These locally used bits provide each of the DSPs with the ability to pass information to the WET latches from the DAB or read information from the WET bus to the DAB. Finally, miscellaneous control bits are latched in U84 or U119 and passed on for phase alignment in latches U82 and U63 or latches U117 and U92.

4.2.6 Digital Signal Processor

The 480L digital signal processor is composed of two major functional blocks: the digitized audio management and memory section, and the arithmetic section. Each of these sections is explained separately below.

4.2.7 Audio Management and Memory

This section can be subdivided into three functional subsections: the Memory Management Unit (MMU), memory timing, and the Digitized Audio Memory (DAM). The MMU (U69 or U98) provides addressing of the DAM by subtracting offsets (micro bits 0-15) from

an internal position pointer. The offsets are clocked into buffers directly from the WCS. They are then subtracted from the current pointer to memory to generate the row and column addresses for the DAM. The current position pointer is incremented once a sample cycle by the falling edge of WC (word clock). The signal SEL is used to multiplex out the addresses necessary for correct memory access. Delay line U40 and inverter U51 provide correct timing for the RAS/, CAS/ and SEL strobes. U50 or U51, D-flip-flop U28 and AND gate U15 provide decoding of the delayed signals. The DAM is composed of five 64k x 4 dynamic RAMs for a total of 64K 20-bit audio words. Eighteen bits are to provide the audio word and two bits are used for further expansion.

4.2.8 Arithmetic Section

The arithmetic section is made up of the timing and control subsection and the ARU. The timing and control subsection is composed of ROMs U77 and U62 with latches U76 and U61 and ARU U60 or ROMs U112 and U91 with latches U111 and U90 and ARU U89. Coefficient bits C<0:4>, state bits ST<0:2> and several control bits make up the address bits for the ROMs. The data is latched on every master clock (MC) for control of the ARU. The ARU performs an eighteen by four bit multiply and accumulate every instruction cycle. Data is read into or gated out of the ARU buffers onto the DAB once an instruction cycle.

4.2.9 Digital Audio I/O

The 480L has two 18-bit audio busses. The first bus is the WET bus which is a global bus used by all HSPs plugged into the backplane. It provides access from one HSP to another, access to an HSP by the Host processor and access by any HSP to or from the audio input or output channels. The second audio bus is the DAB bus which is local to each HSP and not directly accessible to any other HSP or Host. For the purpose of the discussions below the latches from the DAB to the WET data bus are U73, U75 and U58 or U86, U88, and U59. The buffers from the WET data bus to the DAB are U72, U74, and U57 or U85, U87, and U56.

4.2.10 HSP X TO HSP Y

Let's assume that HSP x wants to pass one digitized audio word to HSP y for further processing. HSP x first strobes data off the x DAB into its WET bus output latches. This is done by HSP x by either reading from audio memory the desired word while setting IOWR/ to a 0 and leaving OP/ inactive (1), or performing a write with MCEN/ inactive, OP/ inactive and IOWR/ a 0. Once this has been done, IOWR/ is set back to a 1. When HSP y needs the audio word from HSP x, it has to perform an I/O operation. OP/ is now set active by HSP y which enables HSP x's address onto the WET ADDRESS bus and sets IORD/ low on the WET CONTROL bus. This causes HSP x's WET output latch to be enabled onto the WET DATA bus. This data is subsequently gated onto HSP y's DAB. IOWR/ used by HSP x is only a local usage without OP/ enabled the WET CONTROL bus is not affected.

4.2.11 HSP X to Audio Output

Let's assume that HSP x wants to write to one of the four output channels. HSP x first strobes the audio word into the WET output latches, using the same method as above. On the instruction where the audio word is to be written to the audio output, HSP x sets OP/ active enabling all WET busses, sets IOWR/ low and places the WET address of the output port on the WET ADDRESS bus. The DAB output latch is gated to the WET DATA bus and the IOWR/ signal on the WET CONTROL bus clocks the audio word into the addressed audio output register.

4.2.12 AUDIO Input to HSP X

HSP x Audio data is read from the audio inputs by enabling the audio input buffer onto the WET DATA bus and simultaneously gating the WET DATA bus to the DAB. The following method is used by HSP x. HSP x performs an I/O read by setting OP/ active. IORD/ is set low, gating the WET data to DAB x. At the same time HSP x places the audio input address on the WET ADDRESS bus, enabling the desired input channel onto the WET DATA bus. The data passes to HSP x and the transfer is complete.

4.2.13 HSP X to XREG or XREG to HSP X

A method has been provided to allow the Host processor to pass audio data to and from any HSP. This feature is enabled only during test and is not meant to be a real time exchange of audio information. A register called XREG is used for the passing of the audio data from/to the DAB to/from the Host data bus. The method used to pass data to the Host from the HSP is the same as passing data to audio output except that the WET address of the XREG is placed on the WET ADDRESS bus. To read data is the same as reading the audio input except, again, the WET address is for the XREG.

4.3 Host Processor (Rev. 1)

The 480L Host Processor is a 68008-based microprocessor system that interprets external control events and services the needs of the Slave/High Speed Processor subsystems. External control events include multiple LARCs, MIDI, and (in the future) Computer Automation communications. The Slaves rely on the Host Processor for program download and control via interrupts, reset, and DMA read/write to Slave memory. Additionally, the Host provides system clock generation, digital audio I/O, Serial-to-Parallel and Parallel-to-Serial conversion, and support of the audio parallel bus.

The Host Processor hardware kernel is shown on sheet 1 of the schematics. An 8 MHz clock is generated by the 16 MHz crystal oscillator module U18 and counter U16. U16 also generates MIDICLK (500 kHz) and ERRCLK (62.5 kHz). MIDICLK is used by the DUARTs for either timing or MIDI baud-rate communication. ERRCLK is used by U14 to flag bus time-out errors on the processor bus.

Bus operations are most easily explained by walking through a typical bus transaction. The 68008 places an address on A19-A0, a code indicating access type on FC2-FC0, and then strobes valid address by bringing AS/ low. For any function code other than 111 (or access type Interrupt Acknowledge), the output of U12 is driven low, enabling U23 and U24. U23 decodes which area of memory is being accessed. If the memory access is to ROM or RAM, then U24 will select the appropriate IC. In the case of a ROM access, U23 will drive ROMRAMSEL (U9-8) high. ROMRAMSEL is delayed for two 8 MHz cycles by U28. This delayed edge propogates through U27, U29, and U25, finally bringing the DTACK/ input to the 68008 low. DTACK/ low completes the asynchronous bus handshake, the 68008 brings DS/ and AS/ high. AS/ high drives AS low, clearing U28 and releasing DTACK. The 68008 responds by commencing the next bus transaction.

DTACK generation may be simply summarized. The memory map in U23 reflects the maximum configuration of the system, four 1 Megabit ROMs and two 32k x 8 nonvolatile RAMs. The map in device U24, which does the ROM and RAM Chip Selects, will change as device sizes are changed. The intent here is to do DTACK generation for any possible system with a single U23, and change U24 for specific configurations. DTACKs are generated by U28 for the cases ROM, RAM, RAMCART, and Strobes. In the case of DUART access, the DUARTs generate DTACKs. DTACK is generated by the Slave DMA circuit for the case of Slave channel access. There are two remaining cases of DTACK generation. The DUARTs will generate their ordinary DUARTXDTACK/ in the case of an Interrupt Acknowledge cycle after a DUART interrupt. Device U23 will generate a ROMRAMSEL DTACK in the case of a level 7 or level 2 Interrupt Acknowledge. This is accomplished via signal IACKSTB/, generated by U25.

Bus Errors are closely connected to the asynchronous bus handshake. If, through program error, the 68008 presents an address outside the limits of the maximum system, U23 will fail to decode. No device will respond with DTACK, and the uP will hang in the middle of its handshake, waiting for DTACK/ falling edge. After four cycles of ERRCLK, or 64 usec, U14 will drive the BERR/ input to the 68008 low forcing a Bus Error Cycle. The 68008 responds by beginning a Bus Error exception process, fetching a specific vector and commencing execution at that location. Information about the errant bus cycle is preserved in a stack frame to permit analysis of the fault. Bus errors may also be generated during slave access. If a slave fails to respond to the Host's request for bus access, after 64 usec a bus error cycle will be initiated.

The operating system distinguishes between several classes of bus error:

- Bus error during power-up diagnostic check of NVRAM, RAMCART, etc., indicating faulty DTACK hardware.

- Bus error during power-up diagnostic check of DUARTs, indicating faulty DUART hardware.

- Bus error at run-time due to access of nonexistent memory, indicating either hardware fault or program logic fault.

- Bus error during initial access of a Slave, indicating no slave in place.

- Bus error during subsequent access of a Slave, indicating a lunched slave.

There are four types of reset in the system: power-up reset to the 68008 and Slave processors; hard reset of the 68008 due to power failure; 68008 generated reset; and 68008 generated reset to the Slaves, SR/.

Devices R15, C35, and CR10 generate POPI/ on

power-up. POPI/ forces U52 to drive HRESET driving the 68008's HALT/ and RESET/ pins low simultaneously. This reset condition lasts for about 100 msec. Upon release of POPI/, the 68008 will fetch two vectors needed for initialization: the Supervisor Stack Pointer and the Initial Program Counter. Fetching these two vectors requires eight byte read operations. During this time a mechanism operates to ensure that these fetches occur from the first eight locations of ROM0. HRESET high loads zeros into shift register U30, driving MAP/ low. MAP/ stays low for the next eight AS/ falling edges, thus forcing selection of ROM0 through gate U25. After the eighth fetch, MAP/ goes high and the 68008 begins execution at the location specified by the Initial Program Counter. This mechanism allows one important system advantage. During hard reset the system accesses ROM for its initialization. At all other times, base or zero, page is located in NVRAM allowing soft write of the exception processing vectors.

The RESET/ line of the 68008 is bidirectional/open collector. Execution of a RESET instruction will drive RESET/ low, resetting the DUART's and Slave interrupt flop, but leaving the Slave processor's unaffected. The 68008 may read location $C0007, strobing SOFTR/, which will drive SR/ (System Reset) low, resetting all Slaves. SR/ is also driven active by POPI/ (Power-On Prime), so that the slaves are reset at power-on. There is a separate mechanism for resetting Slaves individually, which is discussed below.

The 68008 supports three levels of external interrupt. PF/ (Power Fail) drives interrupt level 7, the highest level. DUARTs U7 and U6 drive level 5, the second-highest level. SLAVEINT/ (Slave Interrupt) drives interrupt level 2, the lowest level. Priority encoder U19 places the current highest level on IPL2/0, IPL1/, holding lower priority interrupts pending.

Host interrupt processing is most easily explained by walking through each of the possible interrupt cycles: Slave, Power Fail, and DUART.

A Slave Z80 requests service by driving SLAVEINT/ low. SLAVEINT/ is buffered by U22. The buffered signal, SLAVINTB/, clears U8, making IR2/ active. If neither IR5/ nor PF/ is active, IR2/ will be encoded by U19 and presented to the 68008. The 68008 will respond within an instruction cycle if interrupt level 2 is enabled.

The interrupt level is output on the address bus, function code FC2-FC0 is set to 111, and AS/ is set active. U26, the IACK decoder, is enabled by FC2-FC0 high, and outputs IACK2/ active. IACK2/ clocks U8 removing the IR2/. IACK2/ enables U67, sending 66 decimal on D7-D0. IACKSTB/ is active, forcing U23 to set ROMRAMSEL, initiating a DTACK/ handshake. The 68008 completes the bus cycle, fetches user vector 66 from its base page memory (NVRAM), and commences interrupt exception processing.

The Motherboard will set PF/ active upon detecting low unregulated DC on the 5V power supply. PF/ is encoded by U19 and presented to the 68008 as interrupt level 7. Level 7 is the highest priority, and not maskable by the uP. The train of events is similar to the case of SLAVEINT/: an interrupt acknowledge cycle is decoded by U26; IACK7/ enables U67; vector 67 is thus returned to the uP; IACKSTB/ is input to U23 and U23 sets ROMRAMSEL active completing the DTACK handshake. The 68008 commences interrupt exception processing. The tasks to be performed by the power fail interrupt are discussed in greater detail later.

DUART interrupts employ a different hardware path. The 68681s, U6 and U7, each have IRQ/ and IACK/ signal lines. IRQ/, output from the DUART, signals that an interrupt condition has occurred. IACK/ is an input to the DUART that signals a 68008 IACK bus cycle. Due to the limited number of interrupt levels available, both DUARTs share interrupt level 5, in round-robin fashion.

Let us presume that DUART1, U7, has just completed transmission of a character and is set up to issue an interrupt on TX Ready. U7 drives IRDUART1/ active. If there is no request pending from DUART2, then U10 will be clocked low by the next falling edge of 8MCLK. IR5/ is driven active by U25, encoded by U19, and presented to the 68008. The 68008 responds with an IACK cycle. IACK5/ is generated by U26. U12 steers IACK5/ to IACKDUART1/. U7 responds by placing the contents of its Interrupt Vector Register on the data bus D7-D0. U7 completes the DTACK handshake via the DUART1 DTACK/ signal. If DUART2 (U6) were to issue an IRDUART2/ during DUART 1's IACK cycle or while DUART1's IRQ was being held pending (by 68008 mask), then DUART2's interrupt request would be held pending, with the IRQ5/ issued only after DUART1's IRQ had been removed. Note that each half of U10 is clocked on opposite phases of 8MCLK, precluding races in the round-robin circuit.

The principle system features of DUART interrupts are:

❖ DUART interrupts may be programmed to occur on TX, RX, and Timer/Counter events as described in the 68681 manual.

❖ DUART1 and DUART2 interrupts are serviced in round-robin fashion, both arriving at IR level 5, second in priority only to Power Fail.

❖ Each DUART issues a user vector number, programmed by register, which points to an entry in the user vector table in NVRAM. Thus, each DUART may have its own interrupt service routine or routines. The uP must poll the DUART requesting service to determine which event triggered the interrupt.

❖ The DUART round-robin circuit arbitrates the hardware interrupt requests. Since the 68008's interrupt mask is set within software, the service routines may set interrupt mask to allow interruption of one DUART's service routine by the other's requests.

Host communication to the Slaves is done via DMA (Direct Memory Access) on one of six 16k byte channels, one channel dedicated per slave. See the address map for definition of the boundaries of the slave channels. PAL U23 sets SLAVEAS/ active when a read or write operation is to one of the slaves. Buffers U32, U21, and U22 are enabled by SLAVEAS/, and present address bus A19-A0 to the slaves as PAB19-PAB0. The Slave DMA interface operates in either byte mode or block mode. In byte mode, BLOCK/, originating at DUART1, is set inactive. A19-A14 appear at hex D-latch U48. The falling edge of SLAVEAS/ latches this high order address into U48. U33 decodes the address as being in one of the six channels and sets one of its outputs. This output is buffered by U37 and appears as one of DMAREQ5/ to DMAREQ0/. The Slave Z80 receives the DMAREQ as a Bus Request. After completion of its current instruction cycle, the Z80 relinquishes its bus and returns Bus Grant, which appears as a low on the open-collector wired-or signal DMAACK/. During this time, the 68008 has been held with DTACK incomplete. DMAACK/ low satisfies gate U54, and permits U17 to generate DMADTACK/. On the next processor access outside of the slave channels, AS will be high indicating valid address. This is delayed one 8MCLK edge by U17 and appears at U15 as ASDELAY. SLAVEAS/ is high (since we are outside the slave channels), BLOCK/ is high, and U15 clears U48. This removes the DMAREQ from DMAREQ5/ - DMAREQ0/ . The slave last accessed is released, and processing continues. Note that byte mode is a misnomer in that multi-byte operations are supported. Any byte or multi-byte write, read, or read/modify/write access to a slave will run as an automatic event under byte mode. This is possible since the slave bus is not relinquished until the 68008 accesses its own memory outside the slave channel space.

The slave channel block mode permits the host uP to read or write the memory space of a particular slave without relinquishing control of the slave busses between accesses. First, the Host uP sets BLOCK/ active (Output Bit 4 of DUART1). The Host then accesses the first byte in Slave memory space. Operation for this first access is identical to that of byte mode, except that U15 does not clear U48. U48 remains latched, the Slave remains in Bus Grant, and DMAACK/ remains low. Subsequent accesses to the Slave are made with U17 generating DMADTACK/ after the falling edge of SLAVEAS/. To terminate block mode for a particular slave, the host uP sets BLOCK/ inactive. On the next memory access outside of slave channel space, U15 will clear U48, releasing the slave.

There is one final mechanism for controlling slaves. The host uP may write to a register on the Slave/HSP PCA, setting RESET/ and INT/ for each slave processor. There is one write-only register per Slave/HSP PCA, controlling two Slave processors, as shown in Table 4.6.

D3	D2	D1	D0	
1	1	1	0	INT/ Lo-order Slave
1	1	0		RESET/ Lo-order Slave
1	0			INT/ Hi-order Slave
0				RESET/ Hi-order Slave

Table 4.6. Slave Control.

These registers are mapped into the Host memory as shown in Table 4.7.

$C0015	SP0WR/	Write address for Slave 0,1
$C0016	SP1WR/	Write address for Slave 2,3
$C0017	SP2WR/	Write address for Slave 4,5

Table 4.7. Register Mapping.

In order to reset Slave 0, the Host uP writes byte $0D to $C0015. During this write, decoder U92 drives SP0WR/ low. SLAVEBUSEN/ is also low, enabling buffer U36.

Buffer U36 drives host D7-D0 onto PDB7-PDB0 on the backplane. $0D is presented to the Slave register and latched on the rising edge of SP0WR/.

When the unit is powered on, Slave registers will be cleared by SR/, holding all Slaves reset. If the Host wishes to stop all Slaves as a result of some cataclysm,

it may assert SR/ by reading address $C0007. To initiate a program on a Slave after power-up, the Host must do the following:

1. Reset the Slave by writing to its slave register.

2. Disable interrupts and task switching. Assert BLOCK/.

3. Release the Slave from reset by writing to its slave register. (This is necessary becauses a Slave in reset will not respond to Bus Requests from the Slave DMA interface.)

4. Immediately read or write to that slave channel. The slave now has its operations suspended and is held in Bus Grant.

5. Download a minimal program to slave location zero.

6. Reset the Slave by writing to its slave register.

7. Deassert BLOCK/. Reenable interrupts and task switching.

8. Release the Slave from reset.

Slaves may be interrupted by asserting INT/ on the appropriate Slave register, as described in the Slave/HSP section.

The Host communicates over four external serial channels provided by two 68681 DUARTs (Dual Asynchronous Receiver/Transmitter). DUART1, U7, is memory mapped with its internal registers appearing at locations $60000 through $6000F. DUART2, U6, appears at locations $64000 through $6400F. DUART registers are summarized in Table 4.8.

The DUARTs provide four serial channels, programmable for any of 20 baud rates from 50 baud to 38.4k baud, including MIDI baud rate of 31.25k baud. U7 pins X1/CLK and X2 drive crystal Y1, 3.6864 MHz. U6 X1/CLK is driven at the same clock rate by HCT04 U9. Access to the DUARTs is mediated by R/W, DUARTxCS/, and DUARTxDTACK/, with A3-A0 being internally decoded to select one of the 16 internal registers. DUART interrupt function is as described above.

DUART1 Channel A is dedicated to MIDI input and output. MIDICLK provides a 500 kHz (16 x 31.25k baud) clock to input pins IP4 and IP3 for this purpose. Additionally, MIDICLK is connected to IP2 to be used as a clock source for the 16-bit internal counter/timer. IP5, IP1, and IP0 on U7 are used for additional system status inputs. Buffers for the MIDI channel are located on the Motherboard. U7 Channel B is buffered by RS422 buffers U2 and U4 and provides LARC1 serial. FB3 and FB4 (Ferrite Bead) serve to limit slew rate on the L1SD/ and L1SD outputs. R2 provides serial termination on the Receive Data differential inputs and R66 improves noise immunity. Output pins OP7 through OP0 provide control over various system functions.

DUART2 Channel A is dedicated to Computer Automation functions, buffered by RS422 buffers U1 and

DUART1 Add	DUART2 Add	Register/Function Read	Register/Function Write
$6000F	$6400F	Stop Counter Command	Bit Reset Command
$6000E	$6400E	Start Counter Command	Bit Set Command
$6000D	$6400D	Input Port (Unlatched)	Output Port Config.
$6000C	$6400C	Interrupt Vector Reg.	Int. Vector Reg.
$6000B	$6400B	Receiver Buffer B	Trans. Buffer B
$6000A	$6400A	Do Not Access	Command Reg. B
$60009	$64009	Status Register B	Clock Sel. Reg. B
$60008	$64008	Mode Register B	Mode Register B
$60007	$64007	Counter Mode: LSB	Counter/Time Lower
$60006	$64006	Counter Mode: MSB	Counter/Time Upper
$60005	$64005	Interrupt Status Reg.	Interrupt Mask Reg.
$60004	$64004	Input Port Change Reg.	Auxilliary Control
$60003	$64003	Receiver Buffer A	Trans. Buffer A

Table 4.8. DUART Register Summaries.

U3, and may run at any of the 20 baud rates including MIDI rate. DUART2 Channel B is dedicated to the second LARC. LARC2 inputs and outputs are buffered and terminated similarly to those of LARC1. All serial receive channels are quadruple-buffered internally. All serial transmit channels are double-buffered internally.

On DUART2, IP2 provides a WC0 (Work Clock Out) input. IP1 and IP0 monitor W2 and W1 jumpers for setting test or diagnostic modes, etc., Output pins OP7 through OP0 provide control over various system functions. DUART1 and 2 parallel input and output functions are summarized in Table 4.9.

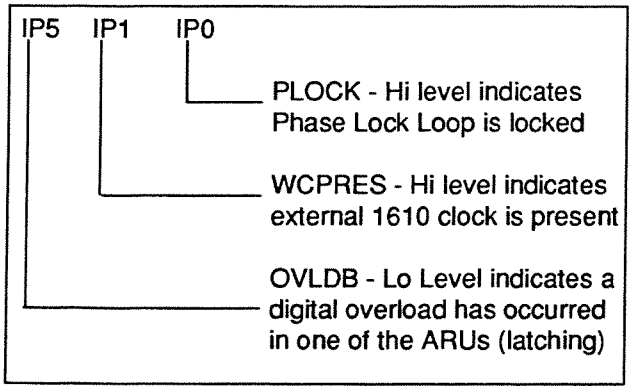

Table 4.9. DUART 1 and 2 I/O Port Functions.

Devices U40, U41, U42, and U43 are ROM sockets designed for either 27256 or 27512 EPROMs. PAL U24 decodes the chip select signals ROMOM/, ROM1/, ROM2/, and ROM3/. A different U24 will be programmed for different selections of memory size. Table 4.10 summarizes jumper positions and pin functions for the different EPROM sizes.

EPROM/ ROM Type	Jumper Position	Pin Function
27256	W11,13,17,20 to +5V	Pin 1-Vpp
	W10,14,15,18 to ROMx/	Pin 22-OE/
27512	W11,13,17,20 to A15	Pin 1- A15
	W10,14,15,18 to ROMx/	Pin 22-EO/

Table 4.10. Jumper Positions and Pin Functions.

The remaining core functions of the Host processor are shown on sheets 2 and 4 of the schematics. Connector J1 is the interface to the nonvolatile RAM Cartridge. The RAM cartridge is mapped by PAL U23 to $70000 through $77FFF and may contain as much as 32k x 8 nonvolatile store, depending upon the cartridge chosen. Buffers U20 and U31 present processor address bus A19-A0 to the J1 connector. These buffers are enabled by RAMCASEL/, generated by PAL U23. RAMCASEL/ also serves to drive CARTENABLE/ and OUTENABLE/. U44 drives WRENABLE/ (cartridge write enable) low when the cartridge is selected and uP R/W is low. U35 buffers the cartridge data bus and uP data bus D7-D0.

Device U38 is either a 4364C (8k x 8) or 43256C (32k x 8) nonvolatile RAM. U39 is a 43256 (32k x 8). Jumper W9 is connected to a pull-up for the 4364 or to A13 for a 43256. Backup power for the RAMs and U49 is provided by two batteries, BT1 and BT2. When +5V is present, diode CR8 supplies current to bring BATVCC to approxiamately 4.5V. When +5v falls to 0V, CR7 and CR9 conduct, supplying approximately 2.6V to BATVCC, supplying standby voltage to the CMOS RAMs. BT1 and BT2 each have a capacity of 150 mAH. At typical leakage currents in the circuit, this provides battery backup for greater than 80,000 hours. The diode isolation between BT1 and BT2 prevents a defective battery from destroying NVRAM contents. Either BT1 or BT2 may be changed (with an isolated soldering iron) without disrupting RAM contents. U49, the RAM protect flop, is also a CMOS device powered by BATVCC. In response to a PF/ interrupt, or other command to go into a standby state, the Host uP will complete housekeeping tasks dictated by software and then pulse DISRAM high. U49 will be reset with RAMBUFEN low. U50, which buffers the RAM select signals HIRAMSEL/ and LORAMSEL/ will be disabled, preventing RAM access. On power-up, the Motherboard will keep PF/ active for greater than 120 msec. This time is required for Host uP reset. When the processor comes out of reset, it's first task will be to enable NVRAM by pulsing ENRAMSTB. RAMBUFEN will then go high and NVRAM access is permitted. U50, the isolating gate, is an LS-family device to prevent excessive leakage while in power-down. Note that on power-up, U54 forces MUTE/ to the Motherboard. Before enabling RAM, the uP will wish to set FORCEMUTE high forcing MUTE/ active while slaves are brought to life.

The remaining functions of the Host are system clock generation and digital audio interface, both of which are peripheral to the Host uP itself, but essential to

DUART1 Outputs	Signal	Notes
OP7	DISRAM	Hi level disables non-volative RAM
OP6	MCSEL1	
OP5	MCSEL0	Selects Master Clock source 00 - 15.36 MHz internal 01 - 14.112 MHz internal 10 - 15.36 MHz external 11 - 14.112 MHz external
OP4	BLOCK/	Lo level enables block slave DMA mode
OP3	PEAKSEL	Selects source to be monitored by peak detect circuit 0 - Monitor A/D 1 - Monitor D/A
OP1	SELIN	Selects input to Serial-to-Parallel input registers. 0 - Input serial from 1610 1 - Input serial from A/Ds
OP0	WCOFF/	Forces selection of internal clock for 1610 word clock.

Table 4.11. DUART1 Outputs and Signals.

Note: The signal OVLD/ is an open-collector wired-or output of the slave/HSPs. A pulse indicates that an overflow has occurred within the ARU. Pulse's on OVLD/ clock U8, setting OVLDB active. OVLDB is available as an input to DUART1. U8 is cleared by a low-going pulse on CLROVLD/. Clearing U8 sets OVLDB inactive.

DUART2 Inputs	Signal	Notes
IP5	PF/	Input for monitoring power fail.
IP2	WC0	Word Clock Out is available as a source of interrupts to synchronize Host operations to the sample period.
IP1	W1	Input jumper.
IP0	BLOW/	

Table 4.12. DUART2 Inputs and Signals.

DUART2 Outputs	Signal	Notes
OP7		Hi level signal illuminates CR3, the most significant LED.
OP6		Hi level illuminates CR4.
OP5		Hi level illuminates CR1.
OP4		Hi level illuminates CR2, the least significant LED.
OP3		Not used.
OP2		Not used.
OP1	CLROVLD/	Low-going pulse clears overload flop.

Table 4.13. DUART2 Outputs and Signals.

system operation. There are three principal clocks in the system: WCB/, BCB/, and MCB, buffered Word Clock Bar, buffered Bit Clock Bar, and buffered Master Clock, respectively. Internal to the Host these are generated as BC, BC/, MC, and WC/. The 8 MHz processor clock is also supplied to the system as 8MCLKB.

With the exception of 8MCLKB, the system clocks are derived from MC. MC (Master Clock) is provided by either the Phase Lock Loop or one of two internal crystal oscillators. Regardless of MC source, the generation of BC, BC/ and WC/ is identical. The timing diagram on the following page illustrates the relationship between MC, BC, BC/, 64CLK5 and WC/. MC is driven by the 1Y output of the multiplexer U105. MC clocks U107, a 74F161 configured as a divide-by-five counter. The rising edge of BC/ is coincident with the rising edge of MC. BC/ remains high for three MC periods, then goes low for two periods. BC is the inverse of BC/, as generated by the 74F04 U106. BC rising edges clock U108 and U109, who together constitute a divide-by-64 counter. The six bits of this divide-by-64 counter (64CLK5 - 64CLK0) drive the state ROM U68. U68 is used to control serialization and 1610 transfers. 64CLK5 is a square-wave clock at the sample frequency. The rising edge of 64CLK5 clocks U95, setting it. WC/ is driven low, and remains low for two MC periods until BC goes low clearing U95. U107, U108, and U109 constitute a divide-by-320 counter. Thus, at an MC frequency of 15.36 MHz, a sample frequency of 48 kHz is generated. At an MC of 14.112 MHz, the sample frequency is 44.1 kHz.

When operating with external bits in (1610 interface) the bits-in source supplies a sample frequency square-wave clock. This clock appears, in buffered form, as signal WCI at U100. It is neccesssary to generate all system clocks in phase-lock with this signal. When MCSEL0,1 are set to 11, U105 routes the output of U106-6 to MC. U106-5 is driven by Q3, a level converter, which is in turn driven by the ECL oscillator U110. By virtue of the varactor diode VRC1 on its tank circuit, U110 is a VCO, or Voltage-Controlled Oscillator. The MC4044 amplifier, in conjunction with the transistor Q2 and associated discretes, serve as a LPF, or Low-Pass Filter. The LPF is driven by the phase detector section of U96. The phase detector compares input signals WCI (the external reference) and WC/ (the output of the divide-by-320 chain). The phase-detector, LPF, VCO, and divider chain constitute a fixed divide ratio frequency synthesizer with MC as the output and WCI as the input.

The VCO is switched between a high and low range by a second varactor, VRC2. The signal VSEL is high when MCSEL1,0 = 10. VSEL thus biases VRC2 with approxiamately +4.6 V, setting it's capacitance to a low value of approx. 24 pf. This is appropriate for a WCI input frequency of 48 kHz. When MCSEL1,0 is set to 11, VSEL is set to 0V, and VRC2 is biased at a voltage less than 5V determined by the value of R51, which is Selected At Test. This lower bias voltage results in a higher varactor capacitance, so that the VCO will run at 44.1 kHz. The bits-in interface (1610) is specified at 44.1 kHz; however, the interface will run at 48 kHz, a non-standard 1610 frequency. When running on external word clock, the internal crystal oscillators, U93 and U94, are not powered on. Transistor Q1 is in cut-off. This is to prevent beating between the internal oscillators and the Phase Lock Loop VCO.

In addition to the 48 kHz and 44.1 kHz external clock modes described above, the clock generation circuit will also run 44.1 kHz and 48 kHz internal. When MCSEL1,0 = 00 or 01, Q2 is saturated and either 15.36 MHz or 14.112 MHz is selected at MC by U105. MCSEL1,0 = 00 selects 15.36 MHz; 01 selects 14.112 MHz. Note that the U107, U108, U109 counter chain functions identically whether internal or external clocks are chosen. When running from either of the internal oscillators, the PLL VCO is unconnected. The PLL is thus open loop, and runs to either its highest or lowest frequency, depending upon: internal states in the MC4044; whether external WCI is present; and frequency chosen.

The 1610 interface requires an output word clock, WCO. The Host will fulfill this requirement by either passing on the received 1610 word clock in, WCI, or by passing on an internally derived clock 64CLK5. The received 1610 clock, WCI, is buffered by U100, a Schmitt trigger inverter. U100 pin 8 drives CR11, connected to R30 and C63. When WCI is present, U100 pin 3 will be pulled low and WCPRES will go high. WCPRES is available to the 68008 uP as an input at the DUARTs. If the uP sets WCOFF/ active, then 64CLK5 will be selected through U99 and will appear as WCO. If WCOFF/ is inactive, WCI will be selected as WCO. If WCI is not present, WCPRES inactive guarantees that 64CLK5 is selected as WCO.

Four functional blocks on the Host PCA manipulate digital audio data. Input data from 1610 interface or the A/D converters is converted from serial to parallel by the serial input registers. High-speed processor output is converted from parallel to serial and transmitted by the serial output registers. The digital peak detect

circuit monitors either A/D inputs or D/A outputs. The transfer registers permit interchange of audio data between the Host uP and the high speed processors.

Timing and control EPROM U68 provides control signals for serial input and output. U68 is addressed by 64CLK5-0, generating 64 states per sample period. Data slew is eliminated by clocking register U81 with BC. Thus, the serial timing and control signals appear in phase lock with the sample frequency, at bit clock rate.

Digital audio input will come from either 1610 format bits-in, or from 480L internal format from the motherboard A/D converters. The 1610 format is 16 bits; internal format is 18 bits. Schematic page six shows the input registers. SELIN, supplied by DUART 1, selects the input mode. With SELIN high, GBCLKIN is selected at U102 and clocks the SCLK input of the input registers. GBCLKIN (Gated bit clock in) appears at rising edges of BC and is gated by the signal BGATEIN from the timing ROM. Serial input data from the motherboard (ADDB) is selected by U102 to appear at U60 serial input. U88's serial output, PASSOUT, is passed through to the second set of registers, U59, U73, and U87. Serial data from the A/Ds is presented by the motherboard at ADDB in two bursts of 18 bits, left channel first, followed by right channel. The HCT595 serial registers are fully buffered. The outputs at A,B,C,D,E,F,G,H are the contents of an output register; shift register operations proceed without disturbing the contents of the output register. The first BGATEIN pulse lasts for 24 BC clocks and clocks the 18 left channel bits so that the MSB appears at position H of U88 and the LSB appears at position G of U60. The second BGATEIN pulse also lasts for 24 BC clocks. The left channel data appears at PASSOUT and is clocked through the U102 multiplexer into U59, U73, and U87. Meanwhile, the right channel data appears at ADDB and is clocked into U60, U74, and U88. WC/ pulses low on the last BC period of the sample. This pulse transfers the parallelized data from the shift registers into the output registers of the HCT595s.

A small digression to explain wet bus operation is now in order. The WET Bus serves to transfer parallel audio data from input and output to the high speed processors and intermediate values between the high speed processors. The WET Bus consists of twenty-four data lines (WETDB<23:0>), five address lines (WETADB<4:0>), and two control lines (IORD/ and IOWR/). The Host is a passive partner in WET Bus transactions in that only HSPs drive the address and control lines. For example, to read the A/D left channel input, an HSP places 11100 b on the WETADB and simultaneously pulses IORD/ low. This address is decoded by U98 (schematic sheet 7) as ADINL/. ADINL/ enables the input register U59, U73, and U87 onto the WETDB. The addresses and functions of Host peripherals on the WET bus are shown in Table 4.14.

Address	Strobe Signal	Function
11000 (38)	DAPRIML/	Left Primary D/A
11001 (39)	DAPRIMR/	Right Primary D/A
11010 (3A)	DASECL/	Left Secondary D/A
11011 (3B)	DASECR/	Right Secondary D/A
11100 (3C)	ADINL/	Left A/D input
11101 (3D)	ADINR/	Right A/D input
11110 (3E)	WRXREG/	Write wet data to transfer register
11111 (3F)	RDXREG/	Read transfer register to wet bus

Table 4.14. Host Peripheral Addresses and Functions.

A/D left and right input from the previous sample period are available for transfer to the wet bus during the entire current sample. As described below, the D/A data must be presented to Host output registers within two time slots.

1610 input operation is similiar to A/D input. SELIN is set low. The input registers are clocked by 1610CLK. 1610 input data appears on SADILB (Serial Audio Data Input Left Buffered) and SADIRB. 1610CLK, generated by the timing ROM, clocks the 16 bits of 1610 data in and then clocks 8 additional cycles to bring the data to the top bits of the input registers. WC/ clocks the parallelized data into the HCT595 output registers. As with internal A/D inputs, the audio data from the previous sample cycle is available to the HSPs throughout the entire sample period. The Host microprocessor's only task in this operation is to set the input mode via SELIN.

Output of audio data to the D/As and 1610 interface is slightly more complicated. There are four D/A output channels. These four channels are supported by two sets of registers: U57, U71, U85; and U58, U72, U86 (sheet 7). The four D/A outputs are time-multiplexed into the two registers sets. 1610 bits-out is supported by two separate sets of registers: U55, U69, U83; and U56, U70, U84. The HSPs write primary output data during the latter half of the sample period. WET bus writes to DAPRIML/ and DAPRIMR/ are latched into the input registers of all four sets of HCT597s. Note that

1610 output data is the same as the data presented to the Primary D/A channels. On the last BC period of the sample period NLDAD/ and 1610XFOUT pulse low, transferring the HCT597 input register data to the serial output registers. 1610OUTCLK begins clocking 1610 data out at the beginning of the next sample cycle. 1610 data is clocked at 32 times the sample frequency and appears on the bus at SADOL and SADOR. Simultaneously, the primary D/A channels are being clocked out by GBCLKOUT. GBCLKOUT is produced by delaying BC by one MC cycle and gating it with BGATEOUT, a ROM output. A total of 18 BCs are used, clocking the full output word to the primary D/As. During this time-

The Host uP writes a value to the 24 bit transfer out register by writing the low, middle, and high bytes to $C0010, $C0011, and $C0012. Host uP D<7:0> is latched into U62, U76, and U90. To read the contents of the transfer out register, the HSP must read wet address $3F. Wet address $3F generates RDXREG/, enabling U62, U76, and U90 onto the bus. To write a digital audio word to the transfer in register the HSP must write to wet address $3E. Wet address $3E generates WRXREG/, latching wet bus data into U61, U75, and U89. The Host uP may read this word by reading $C0002, $C0001, and $C0000 generating

stored value, then U63 is clocked, latching the present value in as the new peak. Comparator output is gated by the output of mux U103, indicating a Wet bus I/O operation, and by ZRCLK, to allow propagation time. Latch U63 and U64 are clocked simultaneously. By reading location $C0003, the Host uP reads the 8 MSBs of the previous peak and simultaneously clears U63, enabling it to start a new cycle of peak detection. The time between uP reads of the peak detector sets the periodicity of the peak detect. The signal PEAKSEL determines which of the Wet bus I/O operations is monitored by the detector. With PEAKSEL low, U44 gates ADINL/ and ADINR/ to the detectors. With PEAKSEL high, the D/A primary left and right channels are monitored. The right section of the peak detect circuit functions identically to the left.

4.4 Host Processor Board (Rev. 2 and up)

Note: The Rev. 2 and up Host Processor boards are revisions of the original Rev. 1 board, incorporating all ECOs. The Rev.2 and up boards also use multilayer technology for improved signal quality.

The Host Processor is a 68008-based microprocessor system that interprets external control events and services the needs of the slave/High Speed Processor subsystems. External control events include multiple LARCs, MIDI, and (in the future) Computer Automation communications. The slaves rely on the Host Processor for program download and control via interrupts, reset, and DMA read/write to slave memory. The Host also provides system clock generation, digital audio I/O, Serial-to-Parallel and Parallel-to-Serial conversion, and support of the audio parallel bus.

The Host Processor hardware kernel is shown on sheet 1 of the schematics. An 8 MHz clock is generated by the 16 MHz crystal oscillator module U14 and counter U13. U13 also generates MIDICLK (500 kHz) and ERRCLK (62.5 kHz). MIDICLK is used by the DUARTs for either timing or MIDI baud-rate communication. ERRCLK is used by U12 to flag bus time-out errors on the processor bus.

Bus operations are best explained by walking through a typical bus transaction. The 68008 places an address on A19-A0, a code indicating access type on FC2-FC0, and then strobes valid address by bringing AS/ low. For any function code other than 111 (or access type Interrupt Acknowledge), the output of U27 is driven low, enabling U23 and U24. U23 decodes which area of memory is being accessed. If the memory access is to ROM or RAM, U24 selects the appropriate IC. In the case of a ROM access, U23 drives MEMSEL high. MEMSEL is delayed for two 8 MHz cycles by U10. This delayed edge propogates through U27, and U21, finally bringing the DTACK/ input to the 68008 low. DTACK/ low completes the asynchronous bus handshake, the 68008 brings DS/ and AS/ high. AS/ high drives AS low, clearing U10 and releasing DTACK. The 68008 responds by commencing the next bus transaction.

The memory map in U23 reflects the maximum configuration possible; four 1-Mbit ROMs and two 32k x 8 nonvolatile RAMs. The map in device U24, which performs the ROM and RAM Chip Selects, will change as device sizes are changed. The intent is to provide DTACK generation for any possible system with a single U23, and change U24 for specific configurations. DTACKs are generated by U10 for the cases ROM, RAM, RAMCART, and Strobes. In the case of DUART access, the DUARTs generate DTACKs. DTACK is generated by the slave DMA circuit for the case of slave channel access. There are two remaining cases of DTACK generation. The DUARTs generate their ordinary DUARTXDTACK/ in the case of an Interrupt Acknowledge cycle after a DUART interrupt. Device U23 generates a MEMSEL DTACK in the case of a level 7 or level 2 Interrupt Acknowledge. This is accomplished via signal IACKSTB/, generated by U21.

Bus Errors are closely connected to the asynchronous bus handshake. If, through program error, the 68008 presents an address outside the limits of the maximum system, U23 will fail to decode. No device will respond with DTACK, and the uP will hang in the middle of its handshake, waiting for DTACK/ falling edge. After four cycles of ERRCLK (64 usec) U12 drives the BERR/ input to the 68008 low forcing a Bus Error Cycle. The 68008 responds by beginning a Bus Error exception process, fetching a specific vector and commencing execution at that location. Information about the errant bus cycle is preserved in a stack frame to permit analysis of the fault. Bus errors may also be generated during slave access. If a slave fails to respond to the Host's request for bus access, a bus error cycle is initiated after 64 usec.

The operating system distinguishes between several classes of bus error:

- Bus error during power-up diagnostic check of NVRAM, RAMCART, etc., indicating faulty DTACK hardware.

❖ Bus error during power-up diagnostic check of DUARTs, indicating faulty DUART hardware.

❖ Bus error at run-time due to access of non-existent memory, indicating either a hardware or program logic fault.

❖ Bus error during initial access of a slave, indicating no slave in place.

❖ Bus error during subsequent access of a slave, indicating a defective slave.

There are four types of resets in the system: power-up reset to the 68008 and slave processors; hard reset of the 68008 due to power failure; 68008 generated reset; and 68008 generated reset to the slaves, SR/.

Devices R21, C24, and CR6 generate POPI/ (Power-On Prime) on power-up. POPI/ forces U36 to drive HRESET driving the 68008's HALT/ and RESET/ pins low simultaneously. This reset condition lasts for about 100 msec. Upon release of POPI/, the 68008 fetches two vectors needed for initialization: the Supervisor Stack Pointer and the Initial Program Counter. Fetching these vectors requires eight byte read operations. During this time a mechanism operates to ensure that these fetches occur from the first eight locations of ROM0. HRESET high loads zeros into shift register U28, driving MAP/ low. MAP/ stays low for the next eight AS/ falling edges, forcing selection of ROM0 through U24. After the eighth fetch, MAP/ goes high and the 68008 begins execution at the location specified by the Initial Program Counter. During hard reset the system accesses ROM for its initialization. At all other times, base or zero, page is located in NVRAM allowing soft write of the exception processing vectors.

The RESET/ line of the 68008 is bidirectional/open collector. Execution of a RESET instruction drives RESET/ low, resetting the DUART's and slave interrupt flop, but leaving the slave processor's unaffected. The 68008 may read location $C0007, strobing SOFTR/, which drives SR/ (System Reset) low, resetting all slaves. SR/ is also driven active by POPI/ (Power-On Prime), so that the slaves are reset at power-on. A separate mechanism for resetting slaves individually is discussed below.

The 68008 supports three levels of external interrupt. PF/ (Power Fail) drives interrupt level 7, the highest level. DUARTs U7 and U6 drive level 5, the second-highest level. slaveINT/ (slave Interrupt) drives interrupt level 2, the lowest level. Priority encoder U17 places the current highest level on IPL2/0, IPL1/, holding lower priority interrupts pending.

Host interrupt processing is best explained by walking through each of the possible interrupt cycles: slave, Power Fail, and DUART.

A slave Z80 requests service by driving slaveINT/ low. slaveINT/ is buffered by U20. The buffered signal, SLAVINTB/, clears U8, making IR2/ active. If neither IR5/ nor PF/ is active, IR2/ is encoded by U17 and presented to the 68008. The 68008 responds within an instruction cycle if interrupt level 2 is enabled.

The interrupt level is output on the address bus, function code FC2-FC0 is set to 111, and AS/ is set active. U22, the IACK decoder, is enabled by FC2-FC0 high, and outputs IACK2/ active. IACK2/ clocks U8 removing the IR2/. IACK2/ enables U26, sending 66 decimal on D7-D0. IACKSTB/ is active, forcing U23 to set MEMSEL, initiating a DTACK/ handshake. The 68008 completes the bus cycle, fetches user vector 66 from its base page memory (NVRAM), and commences interrupt exception processing.

The Motherboard sets PF/ active upon detecting low unregulated DC on the 5V power supply. PF/ is encoded by U17 and presented to the 68008 as interrupt level 7. Level 7 is the highest priority, and not maskable by the uP. The train of events is similar to the case of slaveINT/: an interrupt acknowledge cycle is decoded by U22; IACK7/ enables U26; vector 67 is thus returned to the uP; IACKSTB/ is input to U23 and U23 sets MEMSEL active completing the DTACK handshake. The 68008 then commences interrupt exception processing.

DUART interrupts employ a different hardware path. The 68681s, U6 and U7, each have IRQ/ and IACK/ signal lines. IRQ/, output from the DUART, signals that an interrupt condition has occurred. IACK/ is an input to the DUART that signals a 68008 IACK bus cycle. Due to the limited number of interrupt levels available, both DUARTs share interrupt level 5, in round-robin fashion.

Let us presume that DUART1 (U7) has just completed transmission of a character and is set up to issue an interrupt on TX Ready. U7 drives IRDUART1/ active. IR5/ is driven active by U21, encoded by U17, and presented to the 68008. The 68008 responds with an IACK cycle. IACK5/ is generated by U22. U7 responds by placing the contents of its Interrupt Vector Register on the data bus D7-D0. U7 completes the DTACK handshake via the DUART1DTACK/ signal.

If DUART2 (U6) were to issue an IRDUART2/ during DUART 1's IACK cycle or while DUART1's IRQ was being held pending (by 68008 mask), DUART2's interrupt request would be held pending, with the IRQ5/ issued only after DUART1's IRQ had been removed.

The principle system features of DUART interrupts are:

❖ DUART interrupts may be programmed to occur on TX, RX, and Timer/Counter events as described in the 68681 manual.

❖ DUART1 and DUART2 interrupts are serviced in round-robin fashion, both arriving at IR level 5, second in priority only to Power Fail.

❖ Each DUART issues a user vector number, programmed by register, which points to an entry in the user vector table in NVRAM. Thus, each DUART may have its own interrupt service routine or routines. The uP must poll the DUART requesting service to determine which event triggered the interrupt.

❖ The DUART round-robin circuit arbitrates the hardware interrupt requests. However, since the 68008's interrupt mask is set with software, the service routines may set interrupt mask to allow interruption of one DUART's service routine by the other's requests.

Host communication to the slaves is via DMA on one of six 16k byte channels, one channel dedicated per slave. See the address map for definition of the boundaries of the slave channels. PAL U23 sets slaveAS/ active when a read or write operation is to one of the slaves. Buffers U30, U19, and U20 are enabled by slaveAS/, and present address bus A19-A0 to the slaves as PAB19-PAB0.

The slave DMA interface operates in either byte mode or block mode. In byte mode, BLOCK/, originating at DUART1, is set inactive. A16-A14 appear at hex D-latch U44. The falling edge of slaveAS/ latches this high order address into U44. U31 decodes the address as being in one of the six channels and sets one of its outputs. This output is buffered by U32 and appears as one of DMAREQ5/ to DMAREQ0/.

The slave Z80 receives the DMAREQ as a Bus Request. After completion of its current instruction cycle, the Z80 relinquishes its bus and returns Bus Grant, which appears as a low on the open collector wired-or signal DMAACK/. During this time, the 68008 is held with DTACK incomplete. DMAACK/ low satisfies gate U51, and permits U16 to generate DMADTACK/.

On the next processor access outside of the slave channels, AS will be high indicating valid address. This is delayed one 8MCLK edge by U16 and appears at U50 as ASDELAY. slaveAS/ is high (since we are outside the slave channels), BLOCK/ is high, and U50 clears U44. This removes the DMAREQ from DMAREQ5/ - DMAREQ0/. The slave last accessed is released, and processing continues.

Note that "byte mode" is a misnomer in that multi-byte operations *are* supported. Any byte or multi-byte write, read, or read/modify/write access to a slave will run as an automatic event under byte mode. This is possible since the slave bus is not relinquished until the 68008 accesses its own memory outside the slave channel space.

The slave channel block mode permits the host uP to read or write the memory space of a particular slave without relinquishing control of the slave busses between accesses. First, the Host uP sets BLOCK/ active (Output Bit 4 of DUART1). The Host then accesses the first byte in slave memory space. Operation for this first access is identical to that of byte mode, except that U50 does not clear U44. U44 remains latched, the slave remains in Bus Grant, and DMAACK/ remains low. Subsequent accesses to the slave are made with U16 generating DMADTACK/ after the falling edge of slaveAS/. To terminate block mode for a particular slave, the host uP sets BLOCK/ inactive. On the next memory access outside of slave channel space, U50 clears U44, releasing the slave.

There is one final mechanism for controlling slaves. The host uP may write to a register on the slave/HSP PCA (Processor Control Adder), setting RESET/ and INT/ for each slave processor. There is one write-only register per slave/HSP PCA, controlling two slave processors, as shown in Table 4.16.

D3	D2	D1	D0	
1	1	1	0	INT/ Lo-order Slave
1	1	0		RESET/ Lo-order Slave
1	0			INT/ Hi-order Slave
0				RESET/ Hi-order Slave

Table 4.16. Write-Only Registers.

These registers are mapped into the Host memory as shown in Table 4.17.

$C0015	SP0WR/	Write address for Slave 0,1
$C0016	SP1WR/	Write address for Slave 2,3
$C0017	SP2WR/	Write address for Slave 4,5

Table 4.17. Slave Write Addresses.

In order to reset slave 0, the Host uP writes byte $0D to $C0015. During this write, decoder U88 drives SP0WR/ low. Slave BUSEN/ is low, enabling buffer U33. Buffer U33 drives host D7-D0 onto PDB7-PDB0 (Processor Data Bus) on the backplane. $0D is presented to the slave register and latched on the rising edge of SP0WR/.

When the unit is powered on, slave registers are cleared by SR/, holding all slaves reset. If the Host wishes to stop all slaves as a result of some cataclysm, it asserts SR/ by reading address $C0007. To initiate a program on a slave after power-up, the Host must:

1. Reset the slave by writing to its slave register.

2. Disable interrupts and task switching and assert BLOCK/.

3. Release the slave from reset by writing to its slave register. This is necessary because a slave in reset doesn't respond to Bus Requests from the slave DMA interface.

4. Immediately read or write to that slave channel. The slave now has its operations suspended and is held in Bus Grant.

5. Download a minimal program to slave location zero.

6. Reset the slave by writing to its slave register.

7. Deassert BLOCK/. Reenable interrupts and task switching.

8. Release the slave from reset.

Slaves may be interrupted by asserting INT/ on the appropriate slave register, as described in Section 4.1.

The Host communicates over four external serial channels provided by two 68681 DUARTs (Dual Asynchronous Receiver/Transmitter). DUART1, U7, is memory mapped with its internal registers appearing at locations $60000 through $6000F. DUART2, U6, appears at locations $64000 through $6400F. DUART registers are summarized in Table 4.18.

The DUARTs provide four serial channels, programmable for any of 20 baud rates from 50 baud to 38.4k baud, including MIDI baud rate of 31.25k baud. U7 pins X1/CLK and X2 drive crystal Y1, 3.6864 MHz. U6 X1/CLK is driven at the same clock rate by HCT04 U9. Access to the DUARTs is mediated by R/W, DUARTxCS/, and DUARTxDTACK/, with A3-A0 being internally decoded to select one of the 16 internal registers. The DUART interrupt function is as described above.

DUART1 Add	DUART2 Add	Register/Function Read	Register/Function Write
$6000F	$6400F	Stop Counter Command	Bit Reset Command
$6000E	$6400E	Start Counter Command	Bit Set Command
$6000D	$6400D	Input Port (Unlatched)	Output Port Config.
$6000C	$6400C	Interrupt Vector Reg.	Int. Vector Reg.
$6000B	$6400B	Receiver Buffer B	Trans. Buffer B
$6000A	$6400A	Do Not Access	Command Reg. B
$60009	$64009	Status Register B	Clock Sel. Reg. B
$60008	$64008	Mode Register B	Mode Register B
$60007	$64007	Counter Mode: LSB	Counter/Time Lower
$60006	$64006	Counter Mode: MSB	Counter/Time Upper
$60005	$64005	Interrupt Status Reg.	Interrupt Mask Reg.
$60004	$64004	Input Port Change Reg.	Auxilliary Control
$60003	$64003	Receiver Buffer A	Trans. Buffer A

Table 4.18. DUART Register Summaries.

DUART1 Channel A is dedicated to MIDI input and

DUART1 Outputs	Signal	Notes
OP7	DISRAM	Hi level disables non-volative RAM
OP6	MCSEL1	
OP5	MCSEL0	Selects Master Clock source 00 - 15.36 MHz internal 01 - 14.112 MHz internal 10 - 15.36 MHz external 11 - 14.112 MHz external
OP4	BLOCK/	Lo level enables block slave DMA mode
OP3	PEAKSEL	Selects source to be monitored by peak detect circuit 0 - Monitor A/D 1 - Monitor D/A
OP1	SELIN	Selects input to Serial-to-Parallel input registers. 0 - Input serial from 1610 1 - Input serial from A/Ds
OP0	WCOFF/	Forces selection of internal clock for 1610 word clock.

Table 4.19. DUART1 Outputs and Signals.

Note: The signal OVLD/ is an open-collector wired-or output of the slave/HSPs. A pulse indicates that an overflow has occurred within the ARU. Pulse's on OVLD/ clock U8, setting OVLDB active. OVLDB is available as an input to DUART1. U8 is cleared by a low-going pulse on CLROVLD/. Clearing U8 sets OVLDB inactive.

DUART2 Inputs	Signal	Notes
IP5	PF/	Input for monitoring power fail.
IP2	WC0	Word Clock Out is available as a source of interrupts to synchronize Host operations to the sample period.
IP1	W1	Input jumper.
IP0	BLOW/	

Table 4.20. DUART2 Inputs and Signals.

DUART2 Outputs	Signal	Notes
OP7		Hi level signal illuminates CR3, the most significant LED.
OP6		Hi level illuminates CR4.
OP5		Hi level illuminates CR1.
OP4		Hi level illuminates CR2, the least significant LED.
OP3		Not used.
OP2		Not used.
OP1	CLROVLD/	Low-going pulse clears overload flop.

Table 4.21. DUART2 Outputs and Signals.

output. MIDICLK provides a 500 kHz (16 x 31.25k baud) clock to input pins IP4 and IP3 for this purpose. Additionally, MIDICLK is connected to IP2 to be used as a clock source for the 16-bit internal counter/timer. IP5, IP1, and IP0 on U7 are used for additional system status inputs. Buffers for the MIDI channel are located on the Motherboard. U7 Channel B is buffered by U2 and U4 and provides LARC1 serial. FB3 and FB4 (Ferrite Bead) serve to limit slew rate on the L1SD/ and L1SD outputs. R5 provides serial termination on the Receive Data differential inputs and R4 improves noise immunity. Output pins OP7 through OP0 provide control over various system functions.

DUART2 Channel A is dedicated to Computer Automation functions, buffered by U1 and U3, and may run at any of the 20 baud rates including MIDI rate. DUART2 Channel B is dedicated to the second LARC. LARC2 inputs and outputs are buffered and terminated similarly to those of LARC1. All serial receive channels are quadruple-buffered internally. All serial transmit channels are double-buffered internally. On DUART2, IP2 provides a WC0 (Work Clock Out) input. IP1 monitors W1 jumper for setting test or diagnostic modes, etc., Output pins OP7 through OP0 provide control over various system functions. DUART1 and 2 parallel input and output functions are summarized in Table 4.18.

Devices U40, U41, U42, and U43 are ROM sockets designed for 27512 EPROMs. PAL U24 decodes the chip select signals ROM0/, ROM1/, ROM2/, and ROM3/.

The remaining core functions of the Host processor are shown on sheets 2 and 4 of the schematics. Connector J3 is the interface to the nonvolatile RAM Cartridge. The RAM cartridge is mapped by PAL U23 to $70000 through $77FFF and may contain as much as 32k x 8 nonvolatile store, depending upon the cartridge in use. Buffers U15 and U18 present processor address bus A14-A0 to the J3 connector. These buffers are enabled by RAMCASEL/, generated by PAL U23. RAMCASEL also serves to drive CARTENABLE/ and OUTENABLE/. U25 drives WRENABLE/ (cartridge write enable) low when the cartridge is selected and uP R/W is low. U29 buffers the cartridge data bus and uP data bus D7-D0.

Backup power for the RAMs and U46 is provided by two batteries, BT1 and BT2. When +5V is present, diode CR8 supplies current to bring BATVCC to approxiamately 4.5V. When +5v falls to 0V, CR7 and CR9 conduct, supplying approximately 2.6V to BATVCC, supplying standby voltage to the CMOS RAMs. BT1 and BT2 each have a capacity of 150 mAH. At typical leakage currents in the circuit, this provides battery backup for greater than 80,000 hours. The diode isolation between BT1 and BT2 prevents a defective battery from destroying NVRAM contents. Either BT1 or BT2 may be changed (with an isolated soldering iron) without disrupting RAM contents. U46, the RAM protect flop, is also a CMOS device powered by BATVCC. In response to a PF/ interrupt, or other command to go into a standby state, the Host uP will complete housekeeping tasks dictated by software and then pulse DISRAM high. U46 will be reset with RAMBUFEN low. U47, which buffers the RAM select signals HIRAMSEL/ and LORAMSEL/ will be disabled, preventing RAM access. On power-up, the Motherboard will keep PF/ active for greater than 120 msec. This time is required for Host uP reset. When the processor comes out of reset, it's first task will be to enable NVRAM by pulsing ENRAMSTB. RAMBUFEN will then go high and NVRAM access is permitted. U47, the isolating gate, is an LS-family device to prevent excessive leakage while in power-down. Note that on power-up, U51 forces MUTE/ to the Motherboard. Before enabling RAM, the uP will wish to set FORCEMUTE high forcing MUTE/ active while slaves are brought to life.

The remaining functions of the Host are system clock generation and digital audio interface, both of which are peripheral to the Host uP itself, but essential to system operation. There are three principal clocks in the system: WCB/, BCB/, and MCB, buffered Word Clock Bar, buffered Bit Clock Bar, and buffered Master Clock, respectively. Internal to the Host these are generated as BC, BC/, MC, and WC/. The 8 MHz processor clock is also supplied to the system as 8MCLKB.

With the exception of 8MCLKB, the system clocks are derived from MC. MC (Master Clock) is provided by either the Phase Lock Loop or one of two internal crystal oscillators. Regardless of MC source, the generation of BC, BC/ and WC/ is identical. MC is driven by the 1Y output of the multiplexer U102. MC clocks U104, a 74F161 configured as a divide-by-five counter. The rising edge of BC/ is coincident with the rising edge of MC. BC/ remains high for three MC periods, then goes low for two periods. BC is the inverse of BC/, as generated by the 74F04 U103. BC rising edges clock U105 and U106, who together constitute a divide-by-64 counter. The six bits of this divide-by-64 counter (64CLK5 - 64CLK0) drive the state ROM U65. U65 is used to control serialization and 1610 transfers. 64CLK5 is a square-wave clock at the sample fre-

quency. The rising edge of 64CLK5 clocks U91, setting it. WC/ is driven low, and remains low for two MC periods until BC goes low clearing U91. U104, U105, and U106 constitute a divide-by-320 counter. Thus, at an MC frequency of 15.36 MHz, a sample frequency of 48 kHz is generated. At an MC of 14.112 MHz, the sample frequency is 44.1 kHz.

When operating with external bits in (1610 interface) the bits-in source supplies a sample frequency square-wave clock. This clock appears, in buffered form, as signal WCI at U97. It is neccesssary to generate all system clocks in phase-lock with this signal. When MCSEL0,1 are set to 11, U102 routes the output of U103-6 to MC. U103-5 is driven by Q3, a level converter, which is in turn driven by the ECL oscillator U107. By virtue of the varactor diode VRC1 on its tank circuit, U107 is a VCO, or Voltage-Controlled Oscillator.

The MC4044 amplifier, in conjunction with the transistor Q2 and associated discretes, serve as a LPF, or Low-Pass Filter. The LPF is driven by the phase detector section of U92. The phase detector compares input signals WCI/ (the external reference) and WC/ (the output of the divide-by-320 chain). The phase-detector, LPF, VCO, and divider chain constitute a fixed divide ratio frequency synthesizer with MC as the output and WCI as the input.

The VCO is switched between a high and low range by a second varactor, VRC2. The signal VSEL is high when MCSEL1,0 = 10. VSEL thus biases VRC2 with approxiamately +4.6 V, setting it's capacitance to a low value of approx. 24 pf. This is appropriate for a WCI input frequency of 48 kHz. When MCSEL1,0 is set to 11, VSEL is set to 0V, and VRC2 is biased at a voltage less than 5V.

This lower bias voltage results in a higher varactor capacitance, so that the VCO will run at 44.1 kHz. The bits-in interface (1610) is specified at 44.1 kHz; however, the interface will run at 48 kHz, a non-standard 1610 frequency. When running on external word clock, the internal crystal oscillators, U89 and U90, are not powered on. Transistor Q1 is in cut-off. This is to prevent beating between the internal oscillators and the Phase Lock Loop VCO.

In addition to the 48 kHz and 44.1 kHz external clock modes described above, the clock generation circuit will also run 44.1 kHz and 48 kHz internal. When MCSEL1,0 = 00 or 01, Q2 is saturated and either 15.36 MHz or 14.112 MHz is selected at MC by U102. MCSEL1,0 = 00 selects 15.36 MHz; 01 selects 14.112 MHz. Note that the U104, U105, U106 counter chain functions identically whether internal or external clocks are chosen. When running from either of the internal oscillators, the PLL VCO is unconnected. The PLL is thus open loop, and runs to either its highest or lowest frequency, depending upon: internal states in the MC4044; whether external WCI is present; and frequency chosen.

The 1610 interface requires an output word clock, WCO. The Host will fulfill this requirement by either passing on the received 1610 word clock in, WCI, or by passing on an internally derived clock 64CLK5. The received 1610 clock, WCI, is buffered by U97, a Schmitt trigger inverter. U97 pin 8 drives CR18, connected to R52 and C75. When WCI is present, U97 pin 3 will be pulled low and WCPRES will go high. WCPRES is available to the 68008 uP as an input at the DUARTs. If the uP sets WCOFF/ active, then 64CLK5 will be selected through U96 and will appear as WCO. If WCOFF/ is inactive, WCI will be selected as WCO. If WCI is not present, WCPRES inactive guarantees that 64CLK5 is selected as WCO.

Four functional blocks on the Host PCA manipulate digital audio data. Input data from 1610 interface or the A/D converters is converted from serial to parallel by the serial input registers. High-speed processor output is converted from parallel to serial and transmitted by the serial output registers.

The digital peak detect circuit monitors either A/D inputs or D/A outputs. The transfer registers permit interchange of audio data between the Host uP and the high speed processors.

Timing and control EPROM U65 provides control signals for serial input and output. U65 is addressed by 64CLK5-0, generating 64 states per sample period. Data slew is eliminated by clocking register U78 with BC. The serial timing and control signals appear in phase lock with the sample frequency at bit clock rate.

Digital audio input comes from either 1610 format bits-in or 480L internal format from the motherboard A/D converters. The 1610 format is 16 bits; internal format is 18 bits. Schematic page six shows the input registers. SELIN, supplied by DUART 1, selects the input mode. With SELIN high, GBCLKIN is selected at U99 and clocks the SCLK input of the input registers. GBCLKIN (Gated bit clock in) appears at rising edges of BC and is gated by the signal BGATEIN from the timing ROM. Serial input data from the motherboard

(ADDB) is selected by U99 to appear at U57 serial input. U84's serial output (PASSOUT) is passed through to the second set of registers–U56, U70, and U83. Serial data from the A/Ds is presented by the motherboard at ADDB in two bursts of 18 bits, left channel first, followed by right channel. The HCT595 serial registers are fully buffered. The outputs at A,B,C,D,E,F,G,H are the contents of an output register; shift register operations proceed without disturbing the contents of the output register. The first BGATEIN pulse lasts for 24 BC clocks and clocks the 18 left channel bits so that the MSB appears at position H of U84 and the LSB appears at position G of U57. The second BGATEIN pulse also lasts for 24 BC clocks. The left channel data appears at PASSOUT and is clocked through the U99 multiplexer into U56, U70, and U83. Meanwhile, the right channel data appears at ADDB and is clocked into U57, U71, and U84. WC/ pulses low on the last BC period of the sample. This pulse transfers the parallelized data from the shift registers into the output registers of the HCT595s.

A small digression to explain wet bus operation is now in order. The WET Bus transfers parallel audio data from input and output to the high speed processors and intermediate values between the high speed processors. It consists of 24 data lines (WETDB<23:0>), five address lines (WETADB<4:0>), and two control lines (IORD/ and IOWR/). The Host is a passive partner in WET Bus transactions; only HSPs drive the address and control lines. For example, to read the A/D left channel input, an HSP places 11100 b on the WETADB and simultaneously pulse IORD/ low. This address is decoded by U95 (Schematic Sheet 7) as ADINL/. ADINL/ enables the input register U56, U70, and U83 onto the WETDB. The addresses and function of Host peripherals on the WET bus are shown in Table 4.22.

Address	Strobe Sig.	Function
11000 (38)	DAPRIML/	Left Primary D/A
11001 (39)	DAPRIMR/	Right Primary D/A
11010 (3A)	DASECL/	Left Secondary D/A
11011 (3B)	DASECR/	Right Secondary D/A
11100 (3C)	ADINL/	Left A/D input
11101 (3D)	ADINR/	Right A/D input
11110 (3E)	WRXREG/	Write wet data to transfer register
11111 (3F)	RDXREG/	Read transfer register to wet bus

Table 4.22. Host Peripheral Addresses.

A/D left and right input from the previous sample period are available for transfer to the wet bus during the entire current sample. As described below, the D/A data must be presented to Host output registers within two time slots.

1610 input operation is similiar to A/D input. SELIN is set low. The input registers are clocked by 1610CLK. 1610 input data appears on SADILB (Serial Audio Data Input Left Buffered) and SADIRB. 1610CLK, generated by the timing ROM, clocks the 16 bits of 1610 data in and then clocks 8 additional cycles to bring the data to the top bits of the input registers. WC/ clocks the parallelized data into the HCT595 output registers. As with internal A/D inputs, the audio data from the previous sample cycle is available to the HSPs throughout the entire sample period. The Host microprocessor's only task in this operation is to set the input mode via SELIN.

Output of audio data to the D/As and 1610 interface is slightly more complicated. There are four D/A output channels. These four channels are supported by two sets of registers: U54, U68, U81; and U55, U69, U82 (sheet 7). The four D/A outputs are time-multiplexed into the two registers sets. 1610 bits-out is supported by two separate sets of registers: U52, U66, U79; and U53, U67, U80. The HSPs write primary output data during the latter half of the sample period. WET bus writes to DAPRIML/ and DAPRIMR/ are latched into the input registers of all four sets of HCT597s. Note that 1610 output data is the same as the data presented to the Primary D/A channels. On the last BC period of the sample period NLDAD/ and 1610XFOUT pulse low, transferring the HCT597 input register data to the serial output registers. 1610OUTCLK begins clocking 1610 data out at the beginning of the next sample cycle. 1610 data is clocked at 32 times the sample frequency and appears on the bus at SADOL and SADOR. Simultaneously, the primary D/A channels are being clocked out by GBCLKOUT. GBCLKOUT is produced by delaying BC by one MC cycle and gating it with BGATEOUT, a ROM output. A total of 18 BCs are used, clocking the full output word to the primary D/As. During this time (the first half of the sample period), the HSPs may write the DASECL/ and DASECR/ data to the input registers. A second pulse of NLDAD/ transfers the secondary data to the serial output registers of the HCT597s. This data is shifted out to the motherboard (appearing on DADL and DADR) during the latter half of the sample cycle. This is accomplished by a second pulse of BGATEOUT producing a second set of 18 GBCLKOUT clocks.

The Host uP uses its transfer registers as a source and sink of digital audio data to and from the Wet bus. As with the A/D and D/A registers, the HSPs supply addresses and control signals governing the Wet bus transactions. Decoders U87 and U88 generate address derived strobes as shown in Table 4.23.

Write address	Strobe	Function
$C0017	SP2WR/	Write to Slave Pair 2 control reg.
$C0016	SP1WR/	Write to Slave Pair 1 control reg.
$C0015	SP0WR/	Write to Slave Pair 0 control reg.
$C0014	(not used)	
$C0012	XFEROUTHI/	Writes high byte to transfer out
$C0011	XFOUTMID/	Writes middle byte to transfer out
$C0010	XFOUTLO/	Writes low byte to transfer out
Read Address	**Strobe**	**Function**
$C0007	SOFTR/	Soft reset (generates SR/)
$C0006	(not used)	
$C0005	(not used)	
$C0004	RDPEAKR/	Read peak detect right channel
$C0003	RDPEAKL/	Read peak detect left channel
$C0002	XFERINHI/	Read xfer reg. high byte
$C0001	XFERINMID/	Read xfer reg. middle byte
$C0000	XFERINLO/	Read xfer reg. low byte

Table 4.23. Host Addresses and Strobes.

The Host uP writes a value to the 24 bit transfer out register by writing the low, middle, and high bytes to $C0010, $C0011, and $C0012. Host uP D<7:0> is latched into U59, U73, and U86. To read the contents of the transfer out register, the HSP must read wet address $3F. Wet address $3F generates RDXREG/, enabling U59, U73, and U86 onto the bus. To write a digital audio word to the transfer in register the HSP must write to wet address $3E. Wet address $3E generates WRXREG/, latching wet bus data into U58, U72, and U85. The Host uP may read this word by reading $C0002, $C0001, and $C0000 generating XFERINHI/, XFERINMID/ and XFERINLO/. The WC0 input to DUART2 may be used to monitor WC by the Host, synchronizing Host execution with the sample period. However, an exchange of flags between the Host and Slave is more appropriate for mediating most transfer register exchanges. The use of the transfer registers are manifold and include: download of wave tables to the HSPs; diagnostic testing of the HSPs; monitoring of intermediate HSP calculations; and even upload of samples to the Host for FFT or other analysis.

Sheet 9 of the schematics shows the digital peak detect circuitry. The digital peak circuitry detects and holds the values of peaks in the digital audio data with eight bit resolution. Byte-wide latches U61 and U62 hold the old peak values. When bit 23 of the Wet bus is low, indicating a positive value (Wet bus is 2's complement), comparators U74 and U75 compare the old peak value with the current Wet bus value latched in U61 or U62, the high-order byte of which is presented on bits WETDB22 through WETDB15. If the Wet bus value is greater than the stored value, then U61 or U62 is clocked, latching the present value in as the new peak. Comparator output feeds PAL U77. Latch U63 or U64 are then clocked simultaneously. By reading location $C0003, the Host uP reads the 8 MSBs of the previous

peak and simultaneously clears U63 or U64, enabling it to start a new cycle of peak detection. The time between uP reads of the peak detector sets the periodicity of the peak detect. The signal PEAKSEL determines which of the Wet bus I/O operations is monitored by the detector. With PEAKSEL low, U77 gates ADINL/ and ADINR/ to the detectors. With PEAKSEL high, the D/A primary left and right channels are monitored.

4.5 Motherboard

The 480L Motherboard consists of the following sections:

MIDI interface
±15 V and +5 V linear supplies
Two channels of audio input and A to D conversion
Two D to A converters
Four channels of audio output
Timing and control section

In this description left channel ICs are shown unbracketed and right channel are shown bracketed.

4.5.1 Audio Input Stages

Signals enter in either balanced or unbalanced mode thru a 3 pin XLR to a balanced differential input stage with active common-mode impedance boosting, U62 (U54). The gain of this stage is -10 dB, allowing +28 dBm signals to be directly connected to the machine without overloading the input.

The signal is routed to the input level pot and then to a gain stage, U63 (U55), resulting in +18 to -5 dB of gain before going to a hybrid 9-pole elliptical low-pass (20 kHz) filter, LPF6 (LPF5). This is followed by a 2-pole high-pass filter with a cutoff frequency of around 10 Hz. The 20 kHz LPF has a gain of -6 dB, and the high pass filter has a gain of 11 dB in their passbands.

The next stage is a track/hold amplifier which is comprised of a charge pump, U64 (U56), DMOS switch IC, U65 (U57), a composite amplifier (consisting of a matched FET pair, Q12 (Q10), followed by a low noise bipolar op amp, U66 (U58)), and a FET-input low-offset op amp, U67, configured as an integrator, which nulls dc offsets in the circuit.

The sampled waveform from the track/hold stage then branches to two circuits. First, it is fed to a window comparator circuit U69 & U70 (U60 & U61), which will trigger if the absolute value of the level of the sample is greater than 1/4 (-12 dB) of the maximum A to D converter level (+10 V peak). This is done by comparing the sampled waveform to +2.5V generated by U68 (U59) derived from the reference voltage of the DAC in the A to D converter. The other circuit which is fed by the track/hold is a gain-ranging circuit U52 & U53 (U50 & U51) which will provide unity gain or gain of 4 (+12 dB), depending on the output of the window comparator circuit. The window comparator drives a precision one-shot, U27, which will immediately switch the gain-range circuit to unity gain if the signal exceeds +2.5V (1/4 of full scale), but will not switch back to +12 dB gain unless the signal remains below +2.5V for the full time-out period (about 75 ms) of the one-shot. This prevents "noise pumping" when the signal is constantly crossing the gain range threshold, and it means that the gain-range circuit need not maintain 18 or even 16 bit accuracy since gain changes occur relatively intermittently.

4.5.2 A TO D Conversion

The output of the gain range circuit is fed to a 16-bit DAC, U47 (U45), in conjunction with a precision comparator U46 (U44), and a 16-bit SAR and latch LSI, U35 (U34), the CMU, performs a successive approximation conversion on the input signal.

At the appropriate time in the cycle, each channel's data is enabled from the CMU and loaded into a 16-bit parallel-to-serial shift register. The data is then shifted out to a high speed opto-coupler, U12, which then transmits the data to the backplane, where it is sent to the Host Processor board for conversion back to parallel format and subsequent processing.

4.5.3 D TO A Conversion

Serial data is received from the Host Processor board via backplane connector P1, is opto-coupled by U3, and routed to two banks (left & right) of latching serial-to-parallel shift registers U22, 23, & 24 (U18, 19, & 21). Both channels are received simultaneously, each containing 18 bits of data per output channel. The main channels are received, latched, and outputted in the first half of the word clock cycle, followed by the auxiliary channels in the second half cycle. The latched data for each channel is imme diately presented to that channel's DAC. There are two output DACs, one for the left, U31, and one for the right channels (U29). Each DAC converts both main and auxiliary channel data. The DACs are current output devices which are each followed by an op amp configured as a current-to-

voltage converter, U32 (U30). The voltage thus obtained is sampled by the appropriate front or rear channel deglitch circuit. The deglitch circuits use the Blesser technique of charging a cap on the op amps output, and then in the hold mode, switching the grounded end of the cap to the virtual ground inverting input node of the op amp. This is done to reduce acquisition time and to decrease hold mode noise bandwidth. These circuits are comprised of a quad DMOS switch IC (U36, 38, 40, 42), a low noise, high output current op amp (U37, 39, 41, 43) and associated components.

The deglitch circuits are followed by 2 pole aperture correction filters, U49 (U48) with a mid-band gain of -7.5 dB. These correct for the sinx/x loss inherent in the reconstruction process.

This signal is then routed to the 9 pole anti-imaging low pass filter LPF3 & 4 (LPF1 & 2) , the same as used for input anti-alias filtering, with a loss of 6 dB in the passband. This is then passed through a passive single pole high pass filter and to the output level pots, which control the gain of the hybrid balanced output amplifiers OPA2 & 4 (OPA1 & 3).

The gain of this stage is 0 dB to +21 dB. This signal is routed to the 3 pin male output XLRs. Output muting is accomplished by clamping the inputs to the output amplifiers via low on-resistance FETs Q6-9. Muting occurs when either MUTE/ from the Host Processor goes low, or if a power fail (PF/) is detected. These signals are opto-coupled by U8 and then level shifted (BMUTE) in order to drive the FETs.

4.5.4 Timing and Control

The 480L was designed to produce minimal noise. To that end, the mother board operates on totally separate power supplies from the digital portion of the system, so that noise generated by the digital processing is isolated from the "audio world". The interface between these two separate systems is handled by opto-couplers, which allow clocks and data to be transmitted without the drawback of electrically connecting the two ground systems.

To minimize the number of opto-couplers required, digital audio data is transmitted and received in serial format and only two clock and synchronization signals are received, BCB/, (a 3.072MHz clock, when operating a 48 kHz sample rate), and WCB/, a synchronization pulse which occurs once per sample period. The remainder of the timing signals used for A/D and D/A conversion are generated in a CMOS ROM, U6. WCB/ is opto-coupled and inverted to become CLR which synchronizes the 8 bit counter, U5, to the rest of the unit. This counter is clocked by BCLK/, generated from BCB/. The ROM data is latched by U14 at the same time the counter is clocked. This means that the timing signals outputted by U14 are one BCLK period behind the ROM state, something to keep in mind when examining the timing diagram. The signal SYNC/, generated by the counter, is opto-coupled, inverted and run to the backplane via PI, where it is sent to the power supply board in order to synchronize the switcher to the sample frequency. This minimizes the generation of "beat frequencies" due to the combination of unrelated clock frequencies.

4.5.5 Conversion Chronology

When SAMP goes high, the track/hold circuit will begin tracking the filtered and gain conditioned input signal. This sample period is around 3.9 us long, at which time the circuit goes into hold mode. During this sample period, STRB/ is low, which enables the window comparator's output to be fed to the one-shot. If the signal is within the window (+2.5V), this signal will remain high, and the one-shot will not be triggered. If the signal is outside the window, this signal will go low, which will trigger a 75 ms long pulse from the one-shot. This pulse will immediately clear the D flop at the one-shots output and cause the gain range signals to switch to unity gain setting (unless a sample within the past 75 ms had already cleared the flop). When 75 ms elapses without retriggering the one-shot, the clear pulse goes away, and on the next rising edge of STRB/, the D flop clocks, thereby returning to gain of 4 mode. 1.3 us is then allowed for the gain-range amp and comparator to settle before the CMU chip containing the SAR latches the first (most significant) bit. The successive approximation then continues for the remaining 15 bits, as controlled by CCLK. Notice that the SAR is cleared and the MSB set for the next conversion immediately following the LSB being converted. This is to allow as much time as possible for the DAC's MSB to settle.

Meanwhile, the status of the gain range bits is clocked into another D flop, the output of which, GRL, is fed to the timing ROM. The just-converted 16 bit word for the left channel is enabled onto the ADC bus by INL/, and loaded into the parallel-to-serial shift registers, U26 and U28, by LD/. If GRL is low, indicating the signal is greater than +2.5V, CLKINH is disabled by the timing ROM and the 16 bit word is shifted out on each successive rising edge of BCLK. This is followed by 16 shifts of 0. Thus the 18 bit word transmitted is the 16

MSBs generated by the ADC followed by two 0s.

If GRL is high, indicating the ADC data has been gained up by a factor of 4 (input signals less than +2.5V), CLKINH is enabled, which inhibits the clocking of the shift register for two BCLK cycles, and then goes away. The 18 bit word then transmitted consists of the MSB repeated 3 times followed by the 15 remaining bits.

In the second half of the cycle, the right channel data is enabled onto the ADC bus by INR/, and clocked into the shift registers by LD/. Meanwhile, the right channel gain bit, GRR will have determined whether or not the timing ROM should activate CLKINH, and the data will be shifted out as described above.

Simultaneous to the shifting out of the left channel A/D data, the left and right main output data is being shifted into the serial to parallel shift registers, MSB first, and clocked by BCLK/. After the 18th bit is clocked in, OCLK causes this data to be latched and enabled to the two output DACs U31 and U29.

About 2.5 us is allowed for the DAC and I to V op amp to settle, after which the front channel deglitch circuit will acquire the signal. The acquisition period is approximately 7.5 us, after which the deglitch circuit goes into the hold mode until new front channel data gets converted on the next cycle.

Simultaneous to the shifting out of the right channel A/D data, the left and right auxiliary output data is being shifted into the serial to parallel shift registers as above. Once again OCLK latches this data, it gets converted and the rear channel deglitch circuit will acquire and then hold the signal as the entire process gets repeated in the next cycle.

4.6 Power Supply

The 5 Volt Power Supply Board uses a switching regulator and is configured as a buck (DC to DC stepdown) regulator.

The transformer secondary is rectified by CR1 and filtered by C3 and C4. This results in a DC voltage of between 24 and 32 volts, depending on loading and line voltage. This voltage is chopped by a MOSFET switch, Q1, and the resultant squarewave is filtered by inductor L1 and capacitors C13 and C14.

Remote sensing of the output voltage is used in order to compensate for the IR losses in the wiring harness going to the backplane. With this scheme, the regulator IC U1 regulates the voltage at the backplane, and not at the actual outputs of the supply board. The regulator IC has a 5.00 volt reference output which is divided by R9 and R10 and sent to the non-inverting input of the transconductance error amplifier, pin 1 of U1. The +5 Volts on the backplane is divided by R7 and R8 and sent to the inverting input of the error amp, pin 2 of U1. C8 and R6 provide pole-zero compensation for the error amp. The output of the error amp is compared to a ramping waveform generated by the oscillator section of U1. The SYNC signal, via Q2, synchronizes this internal oscillator to the sample rate of the machine. R11 controls discharge time of the oscillator, while C9 and R3 are the components which control the free-run (non-synchronized) frequency and ramp rate. The output of this comparator goes through some gating functions to prevent double pulsing and then drives the gate of P-channel MOS FET, Q1. R13 and R14 set the proper gate voltage when pin 14, an open collector output of U1, goes low, thereby turning Q1 on. CR3, a 16 volt Zener, prevents excessive source-gate voltage under high line conditions. CR4, a high current Schottky diode, clamps the drain of Q1 to about -0.5V when Q1 is turned off.

In short, a feedback loop is created which seeks to maintain the backplane voltage equal to the reference voltage by modulating the on-time (or pulse width) of the MOSFET. The greater the load or the lower the input voltage, the greater the duty cycle at which the MOSFET is operated, and vice-versa.

4.6.1 Power-Up/Down

The regulator IC has an undervoltage lockout circuit which protects the IC itself and the MOSFET it controls from inadequate supply voltage. If the input voltage is too low (below approximately 7V), the circuit disables the output drivers (pin 14) and holds the RST/ pin low (pin 5). This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft start timing capacitor (C7) in a discharged state.

The soft-start circuit protects the rectifier diodes (CR1) and MOSFET (Q1) from high current surges during power supply turn-on. When the undervoltage lockout circuit releases RST/, an internal current source begins charging C7. As the voltage on this capacitor ramps up to +5 V, the duty cycle of the MOSFET linearly increases to whatever value the voltage regulation loop requires for an error null. Ramp time is about100 msec.

4.6.2 Current Limit/Foldback

Current limiting is accomplished by sensing the voltage drop across a .02 ohm resistor in series with the +5V output line. With the configuration of R4, R5 and R18, a foldback effect is produced whereby the output voltage of the supply will drop as more current is demanded of it, beyond the current limit threshold. The current sense amplifier (pins 6 & 7) has a threshold of 100mV. If this threshold is exceeded, the SHTDN pin (pin 8) goes low. This pin is tied to the RST/ pin (which is bidirectional) which will cause the soft-start capacitor, C7, to be discharged and the output drive (pin 14) to be disabled, thereby shutting off the supply. Since no more current is being supplied, the current sense amp allows SHTDN/ to return high (and thereby RST/) and C7 will begin charging. This allows the duty cycle of the MOSFET to ramp up as in the power-up sequence. If the output of the supply is a dead short (or close to it) this current limit sequence repeats itself until the short is removed. This is known as a "hiccup mode." The supply will keep trying to power up, but is immediately shut down due to excessive current draw.

4.6.3 Overvoltage Protection

The 5 volt supply is protected against overvoltage either by shorting to a higher potential supply or by failure of the regulator circuitry. There are two circuit configurations provided. When the MPC2005 becomes available, CR5, R19, and C16 will be eliminated. The MPC2005 is a monolithic overvoltage protector with built-in reference, comparator, and clamping SCR. It clamps the 5 volt supply to ground, thereby blowing fuse F1 if the supply voltage exceeds 6.2 volts.

Until availability of this part, it is replaced by a 2N6400 SCR which, in conjunction with the three components previously mentioned, provides the same protection. As the voltage of the supply rises, CR5 will begin to conduct at 5.6 volts. If the supply voltage increases further, the voltage at the gate (pin 3) of the SCR rises due to the current flowing through R19. Once the voltage across R19 reaches approximately 0.7 volts, the SCR goes into conduction, shunting the supply to ground.

4.7 LARC

4.7.1 Power Supply

The power supply for the LARC is a 5V switching regulator. The central item in this regulator is an MC34060 or TL494 pulse width modulation (PWM) control chip. The 34060 produces an output control whose duty cycle multiplied by the input voltage is equal to 5V. This control is then applied to a pass transistor (Q1) located between the input voltage and an output filter. The output filter is a low-pass filter with a single pole at a frequency sufficiently low to attenuate the switching frequency and harmonic components in the switched square wave.

The input section is relatively simple. The LARC may be powered from one of two sources; from the mainframe through J1, or from an alternate power source through J2. Note that whenever a plug is inserted into J2, an integral switch disconnects the mainframe power source. C30, and FB3-4 form a simple RF filter for the mainframe power source; C23 and R13 provide a bypass for RF and static between the cable shield and LARC ground; and C31-33 and FB5-8 form a two stage RF filter for the alternate power source. The CR7 bridge rectifier is provided so that either AC or DC power may be used (the mainframe power is rectified). C35-37 form a composite filter capacitor operating over a large frequency range with low ESR. F1 was chosen through extensive testing to be a 1 amp fast fuse. Note, however, that one fault condition can occur that can not be protected by this (or any other) fuse: while the LARC is being powered by the mainframe, the fuse will not blow if a short occurs in the LARC circuitry after the regulator, because the mainframe can not provide enough power to blow the fuse. This fault condition will not damage the regulator or the mainframe.

The 34060 accepts a Vcc input (pin 12) from which the chip is powered and a 5 V reference (Vref, pin 14) is produced. This Vcc may be from 7 to 40 Vdc, and need not be carefully regulated. The dead time input (DT, pin 4) is used to "soft-start" the regulator; when DT is near Vref the regulator is effectively shut down, and when DT is near ground the regulator is allowed to function normally. Thus as C39 is charged from Vref through R19 and R20, the output of the power supply ramps up from 0 V to the normal 5 V output. The 34060 generates the switching frequency internally using the external timing components RT (pin 6 connected to R21) and CT (pin 5 connected to C40). The switching frequency is 1.1/(RT*CT), which figures out to approximately 50

kHz in the LARC. The output transistor of the 34060 is controlled by the product of comparators whose inputs are an internal ramp waveform at the switching frequency, the dead time input, and the sum of two other comparators whose inputs are pins 1 and 2, and 16 and 15. The first comparator is used to compare the regulator output voltage with the reference voltage. The second comparator (which is normally used for current limiting) is not used, and its inputs are tied off. The COMP input (pin 3) is used for compensation of the comparators. The output transistor is used common-emitter fashion to control the pass transistor.

The output section of the regulator consists of the pass transistor (a P-channel MOSFET) and output filter (a single pole LC low-pass filter). The pass transistor is turned on when its gate is pulled to ground by the output transistor of the 34060. R22 is used to quickly discharge the pass transistor's stray gate capacitance when the 34060 output transistor turns off. The output of the pass transistor is a 50 kHz square wave which swings from ground to the input voltage and whose average voltage is 5 V. The output filter (which consists of CR8, FB 9 and 10, L1, and composite capacitor C41 and C42) has its pole at 83 Hz and is used to block the 50 Khz (and higher harmonic) components of the square wave, yielding only the DC component at the output (the desired 5 VDC).

4.7.2 CPU

The central processing unit of the LARC is an 8749, containing the CPU, clock oscillator, RAM, UV erasable ROM, and three 8-bit I/O ports on a single chip.

The XTAL 1 and XTAL 2 (pins 2 and 3) are connected to a 4.608 MHz crystal, yielding a processor throughput of 307,200 instruction cycles/second. The ALE output (pin 11) is a 20% duty cycle square wave at the same frequency as instruction cycles (307.2 kHz), and is present whenever the 8749 has power. This the first place to verify that the processor's clock is correctly functioning.

The three I/O ports are used as follows: The BUS port (pins 12-19) is used as a bidirectional data bus. It is used in two modes; in the tristate mode to transfer 8-bit data to the Litronix DL-1414 intelligent displays from the ADC0809 A/D converter, and both to and from the CDP1854 UART; and in the latched mode (through the NE594 buffer/driver) to scan the switches and headroom LEDs. Bits 0-6 of Port 2 are outputs used as the address bus bits A0-A6, and bit 7 is used as the FSK tape output. Bits 0-3 of Port 1 are used as inputs from the switch array (B0-B3), and bits 4-7 are used as outputs controlling which section/row is lit in the headroom LED array (S0-S3).

There are also several control pins on the 8749: the SS input (pin 5), which must be unconnected for correct operation; the EA input (pin 7), which must be grounded for correct operation; the INT/ input (pin 6), which the UART pulls low to signal the processor when a character is available; the T0 input (pin 1), which the processor can read to determine if there was a framing error on the last character received (this feature is not currently used by the software); the T1 input (pin 39), which the processor reads during FSK tape input; the PROG/ output (pin 25), which is normally used with a 8243 I/O port expander, but is used in the LARC to clock the address of the slider to convert into the ADC0809; and the RD, WR and PSEN (pins 8, 9, and 10) outputs, which are normally used for external memory access, but are not used in the LARC.

4.7.3 Reset Logic

Both the 8749 and the CDP1854 need to be reset after power up. A simple RC (R7 and C9) circuit is used as an input to a differential driver (U3, the uA9638) to produce the required RES and RES/ signals, which are asserted for approximately 1/4 second after power is applied. The CR5 Schottky diode is used to quickly discharge C9 when power is removed (or when power is momentarily lost). To manually reset the LARC, momentarily ground pin 3 of U3.

4.7.4 Address Decoding Logic

In order to be able to access the devices that share the data bus (the ADC0809, CDP1854, and 12 DL-1414s), an address decoder is used. Address bits A2-A5 are decoded into 16 low-active chip select lines using a CD4515 4-to-16 line decoder. Address bit A6 is used as the decoder enable so that any race conditions (which may cause glitches in the decoder outputs) are eliminated.

When addressing devices, the software in the 8749 goes through several steps to assure that the addressing is done without any glitches. When addressing devices for output (such as the CDP1854 and DL-1414s), the 8749 first places the output data on the BUS port, presents the address of the desired device on A0-A5, then pulls A6 low to address the device, and lastly pulls A6 high again to disable the device. When addressing devices for input (such as the CDP1854 and ADC0809), the 8749 first tristates the BUS port,

presents the address of the desired device on A0-A5, pulls A6 low to address the device, then reads the desired input data from the BUS port, and lastly pulls A6 high again to disable the device.

A simple device address map is shown in Table 4.24.

Device	A5	A4	A3	A2	A1	A0
DL-1414, U1, Display Bd	0	0	0	0	C	C
DL-1414, U2, Display Bd	0	0	0	1	C	C
DL-1414, U3, Display Bd	0	0	1	0	C	C
DL-1414, U4, Display Bd	0	0	1	1	C	C
DL-1414, U5, Display Bd	0	1	0	0	C	C
DL-1414, U6, Display Bd	0	1	0	1	C	C
DL-1414, U1, Panel Bd	0	1	1	0	C	C
DL-1414, U2, Panel Bd	0	1	1	1	C	C
DL-1414, U3, Panel Bd	1	0	0	0	C	C
DL-1414, U4, Panel Bd	1	0	0	1	C	C
DL-1414, U5, Panel Bd	1	0	1	0	C	C
DL-1414, U6, Panel Bd	1	0	1	1	C	C
CDP1854 character output	1	1	0	0	X	X
CDP1854 character input	1	1	0	1	X	X
ADC0809 input	1	1	1	0	X	X

Table 4.24. Device Address Map.

Where: XX are don't cares, and CC is the code for the character within a DL-1414 display chip: 00 is the right-most character, 01 is the second from the right, 10 is the second from the left, and 11 is the left-most character.

4.7.5 ADC Logic

The first item of interest concerning the ADC0809 is its power source; in order to guarantee that any switching supply noise will not affect the converter, a filter is used between the 5 V supply and the ADC0809's Vcc input. The filter is an RC filter consisting of R12 and the composite capacitor C16 and C17. Since the ADC0809 is CMOS (and consequently low power), the voltage drop across R17 is minimal. Note also that all the analog inputs are decoupled for further noise immunity.

Parts of the addressing logic for the ADC0809 are slightly more complicated than the other chips on the data bus. The ADC0809's internal analog multiplexer address (the address of the slider to convert) is transferred to the ADC0809 using the 8749's PROG/ output, which is normally used with 8243 Port 2 expander chips. When the processor wishes to change the address of the slider to convert, it uses a command which places a flurry of (mostly useless) information on A0-A3. During this command, the address of the slider to convert is placed on A0-A3 400 ns before the rising edge of PROG/, and is held for 90 ns after the rising edge.

After the processor sets up the address of the next slider to convert, the processor will read the results of the last conversion and start the next conversion simultaneously by addressing the ADC0809 for input as described in section 4. Note that the ADC0809's end of conversion (EOC) output is not used since the processor's software never accesses the ADC0809 more often than the 250 microsecond conversion time.

The last item of interest concerning the ADC0809 is the circuitry associated with analog inputs IN6 and IN7, which is used to measure the 5 V power supply's actual voltage. The circuit connected to IN6 is a resistor/zener diode constant voltage source (R10 and CR6). The digital code resulting from the conversion of this signal will change as the supply voltage to the ADC0809 changes, because the ratio of the supply voltage to the constant voltage will change. The circuit connected to IN7 is simply a resistive voltage divider (R9 and R11) with an adjustable output voltage. Since the voltage source to this divider is the same as the ADC0809 supply voltage, the resulting digital code from the conversion of this signal will be always a constant. If the adjustable voltage source is adjusted so that it is the same as the constant voltage source when the 5 V power supply is at 5.00 V, then the actual voltage of the 5 V power supply is calculated using a linearization of the system equations governing these circuits.

4.7.6 UART Logic

The UART data is read and written using the addressing scheme in section 4. The UART clock inputs (RCLK and TCLK pins 17 and 40), which are 16 times the 9600 baud data rate, are derived by dividing the 307.2 kHz ALE clock by two using 1/2 of the CD4013 flip-flop. The UART is strapped to provide and recognize 8-bit characters with no parity and 2 stop bits. The UART data available (DA, pin 19) output, which signals that the UART has received a complete character, is inverted before being used to interrupt the processor.

4.7.7 RS-422 Logic

The serial data to and from the UART is converted to RS-422 compatible signals by the uA9637 (U2) differential receiver and the uA9638 (U3) differential driver. The LC filter comprised of C27, FB1 and FB2 is used

to rate limit the signal rise and fall times (and thereby reduce RF noise), and the R14 termination resistor is used to eliminate signal reflections.

4.7.8 Litronix Display Logic

The Litronix DL-1414 displays act very much like as a memory device that happens to display its memory's contents. Once a character has been written to the DL-1414, it will be displayed without any need for refresh from the processor. When the addressing scheme from section 4 is used to output data to the DL-1414, the data on the BUS port is the character to display (in ASCII), the A0 and A1 lines correspond to the character to display within a given display chip, and the A2-A5 lines correspond to the address of the display chip. Remember that these lines are decoded by the CD4515 into low-going enable lines, which are connected to the WR/ (pin 3) lines of the DL-1414s and used to clock the data into the displays. Remember that the characters within a chip are numbered from character 00 on the right to character 11 on the left.

4.7.9 Tape Interface Logic

Unused with 480L.

4.7.10 Buffered Bus and Sink logic

The NE594 driver circuit buffers the BUS port and provides current drive capability for the headroom LEDs. No headroom LEDs, however, will light unless the appropriate current sink (the 75492, U4) is activated also. Therefore when the processor is using the data bus to communicate with the DL-1414s, ADC0809, or the CDP1854, it keeps the sinks deactivated so that the LEDs do not light up spuriously. Upon reset of the 8749, all the bits on Port 1 and Port 2 are set to logic 1; therefore Port 1 bits 4-7 are inverted before the 75492 so the LEDs do not light up during power up. R5-R12 on the Panel board are provided for LED current limiting.

The Panel board switches are also scanned from the NE594 buffered BUS output. CR1-CR8 of the Panel board are provided so that "sneak paths" will not cause the LEDs to light if multiple buttons are pushed. R1-R4 of the Panel board provide a pulldown to ground, which is the default condition when buttons are not pushed.

Unlike many other Lexicon products, the LARC processor software does not scan its LEDs and switches simultaneously. The software first will scan the LEDs, lighting eight at a time: the data for each group is placed on the BUS port, then the appropriate bit on Port 1 is set low for several hundred microseconds, then it is set high again. After all the LEDs have been scanned, then the processor will scan all the switches, scanning four at a time: the appropriate bit for each group on the BUS port is set high, then the processor reads the B0-B3 bits from Port 1 to determine the states of the buttons in the selected column. Note that the processor scans only the switches during the Diagnostic Menu Mode; the LEDs are not scanned.

4.8 SME Board (Optional - requires V.2.0 or higher software)

The Sample Memory Expander (SME) is an optional processor board for the Lexicon M480L. The purpose of the board is to provide current and future users with the ability to increase the amount of audio storage currently provided with the standard M480L. The SME provides over twenty-one seconds of digitized audio storage in mono or greater then ten seconds stereo storage at 48 KHz. All samples are stored as 18 bit words. The SME is conceptually divided into several logical blocks (See SME Block Diagram, Chapter 8.) The individual blocks are:

1. Slave Processor and Associated Circuitry
2. Writable Control Store
3. Micro Pipeline
4. Memory Management Unit
5. Digitized Audio Memory
   (1 megaword audio storage)
6. Disk Interfaces and DMA
7. Wet Bus Interface

The system works much like the HSP boards currently used in the 480L. The Z80 is controlled by the Host processor and is responsible for supplying and updating the microcode in the WCS. The WCS provides information to the DSP to drive the hardware to perform a specific function. The micro pipeline redistributes the microbits to provide correct phasing of control and data. Microcode also provides offset pointers fed to the MMU for audio addressing. The audio store is physically divided into four 256k word blocks of eighteen bits per word. An optional disk interface is provided and will, in the future, allow storage and retrieval capability all under DMA control. Audio is accessible to the rest of the system over the Wet bus via the Wet bus interface. A detailed description of each of the sections described above is provided on the following pages with reference made to the SME board schematics.

4.8.1 Slave Processor and Associated Circuitry

The Slave processor used on the SME board is an eight (8) MHz Z80 (U66). The processor is provided with a 32k x 8 static RAM for data and program storage. Programs and data are downloaded to the board from the Host processor via the DMA port composed of the address buffers (U25 and U65), the control buffer (U101) and the data buffer (U87). The Host releases the Slave from reset by removing the low level on the reset pin through quad latch U103. Once the reset has been removed the Host requests the Slave bus by asserting DMAREQA/. The Slave responds by asserting BUSACK/ thus enabling the DMA buffers to control the Slave environment. Note that on the very first access to the Slave environment it is assumed that the Host processor will read one byte or word. This will provide the Host with an identifier code set by jumpers W10-W17. The code on powerup is enabled onto the Slave data bus through U113 and flip-flop U165. Once the DMA request is removed U113 is disabled by clocking U165. Upon completing this sequence the Host may now carry on in the normal mode.

Memory decoding is performed by PAL U102. This PAL also provides WAIT/ to the processor for synchronization and bus requests are also arbitrated between the disk DMA U155 and Host DMA requests. I/O decoding is performed by U104, U107, and U27. A map of both the memory decoding and the I/O decoding is provided below. IORD/ and IOWR/ signals for the DMA U155 and SCSI controller U115 are created by U121, U134, U123 and U124.

STROBE	ADDRESS	FUNCTION
RAM0/	0000H-7FFFH	ENABLE 32kx8 STATIC RAM
BANKA/	8000H-87FFH	WCS BANKA
BANKB/	9000H-97FFH	WCS BANKB

WCS ADDRESSING

BANK	ADDRESS	BYTE	PAGE
A	8000H-817FH	NOT USED	1
A	8180H-81DFH	4	1
A	81E0H-827FH	NOT USED	1
A	8280H-82DFH	2	1
A	8300H-834FH	0	1
A	8350H-857FH	NOT USED	1
A	8580H-85DFH	4	2
A	86E0H-867FH	NOT USED	2
A	8680H-86DFH	2	2
A	8700H-874FH	0	2
A	8750H-87FFH	NOT USED	2
B	9000H-917FH	NOT USED	1
B	9180H-91DFH	5	1
B	91E0H-927FH	NOT USED	1
B	9280H-92DFH	3	1
B	9300H-934FH	1	1
B	9350H-957FH	NOT USED	1
B	9580H-95DFH	5	2
B	95E0H-967FH	NOT USED	2
B	9680H-96DFH	3	2
B	9700H-974FH	1	2
B	9750H-97FFH	NOT USED	2

SME SLAVE I/O MAP

The following is the listing of the I/O ports for the SME Z80.

ADDRESS
HEX FUNCTION

0xh DISK SELECT

00h-0Fh: This section of I/O addresses varies in function based on the interface type used, SCSI or Floppy

1xh DMA SELECT

10h INIT PORT
11h CHANNEL REGISTER PORT R/W
12h COUNT REGISTER PORT R/W
13h NOT USED
14h LSB OF MEMORY START ADDRESS, R/W
15h MID BYTE OF MEMORY START ADDRESS, R/W
16h MSB OF MEMORY START ADDRESS R/W
17h NOT USED
18h DEVICE CONTROL REGISTER, R/W
19h DEVICE CONTROL REGISTER, R/W
1Ah MODE CONTROL REGISTER, R/W
1Bh STATUS REGISTER R ONLY
1Ch NOT USED
1Dh NOT USED
1Eh REQUEST REGISTER, R/W
1Fh MASK REGISTER, R/W

2xh DAB REGISTER

20h LSB DAB WRITE REGISTER W ONLY
21h MID BYTE DAB WRITE REGISTER W ONLY
22h MSB DAB WRITE REGISTER, W ONLY
23h LSB DAB READ REGISTER, R ONLY
24h MID BYTE DAB READ REGISTER, R ONLY
25h MSB DAB READ REGISTER, R ONLY
26h CLEAR CURRENT POSITION COUNTER, R/W
27h WAIT ENABLE, R/W
3xh WORD CLOCK COUNT REGISTER AND CURRENT POSITION COUNT
30h WORD CLOCK COUNTER LSB, W ONLY
31h WORD CLOCK COUNTER MID BYTE, W ONLY
32h WORD CLOCK COUNTER MSB, W ONLY
33h WORD CLOCK COUNTER REGISTER LOAD, R/W
34h CURRENT POSITION COUNTER STORE, W ONLY
35h CURRENT POSITION COUNTER LSB, R ONLY
36h CURRENT POSITION COUNTER MID, R ONLY
37h CURRENT POSITION COUNTER MSB, R ONLY
4xh SLAVE INTERRUPT, R/W
5xh WCS PAGE SELECT (DATA BIT 0 DETER MINES PAGE)
6xh WRITE STATUS REGISTER

N/A	N/A	N/A	IOEN	CLEAR DISK	CLEAR DMA INT	CLEAR WC INT	CLEAR HST INT INT

7xh READ STATUS REGISTER

N/A	N/A	N/A	IOEN	DISK INT	DMA INT	WC INT	HST INT

DAB Register

These registers are bidirectional latches (U100, U96, U90) that are used for transfering audio data to and from the audio store. The write registers (addresses 20h-22h) are used by the Slave to send data to the audio store. The microprogram is responsible for reading this information onto the DAB by asserting SLVRD/ . The microprogram is also responsible for writing audio data into this register by asserting SLVWRT/ for the Slave to read (addresses 23h-25h).

Clear current position counter (CPCC/) is used to clear the current position counter output register. The current position counter is composed of U127-U129 and U139-U140.

Wait enable is used in the same manner as the HSP board.

Word Clock Counter and Current Position Counter Value Register

The SME board has a Word Clock Counter (U1, U2 and U3). A register is provided to allow the count to be loaded to the counters without affecting the count. Once the count has been loaded to these buffers the Slave strobes CLOAD/ (addr 34h), loading the counters. The register is preloadable from addresses 30h-32h. When the counters carry out from the MSB an interrupt is generated.

A set of registers has been provided for the Slave to read the CPC at any time (Read addresses 35h-37h). The Slave must first arm the these registers by strobing CPSTOR/. Note that the Slave should now wait one sample cycle to insure that a current position clock occurs. The next current position clock will clock the current position -1 into registers U93-U95. The Slave can now read this value at any time without it being corrupted. The only way for the Slave to get a new value is to arm the clocking mechanism again.

SLAVE INTERRUPT

Writing to address 4xh generates a Slave interrupt to the host.

PAGE SELECT

The strobe is used to select the active page of the WCS. Writing with the data reset 1s bit set to 0 sets the page to zero. If this bit is set to 1, the page is set to one.

WRITE STATUS REGISTER

This register (U91) is used to clear interrupts. Four sources are provided on the MXP, each of which is maskable. On power up all interrupts are disabled. By writing 1s to the proper bits, each of the interrupts can be enabled. Once an interrupt has been enabled an interrupt will be sent to the Z80. The interrupt is cleared by writing a 0 and then activating it by writing a 1.

READ STATUS REGISTER

This buffer (U106) enables the Slave to determine which device has interrupted if the interrupts have been enabled. Otherwise the Slave can poll for interrupts.

4.8.2 Writable Control Store

The Writable Control Store (WCS) on the SME board is very similar to the that of the current HSP boards. Clocking is generated by PAL U125. These clocks are used to determine the access to the WCS RAM U149 and U173 and also generates PCCLR/ which starts the program counter (U161,U171) at zero. Access to the WCS RAMs for the Z80 occurs during phase A/ of the four-phase clock. For writing and reading to Bank A buffer (U160), latch U159 and OR gates U146 are used. For access to Bank B buffer (U170), latch U169 and OR gates U132 are used. Micro accesses are performed during phases B/, C/ and D/. For more detail on the WCS see the HSP circuit description.

Microcode Description

The microcode for the M480L is a 48 bit microword. The composition of the microword is shown below. Note that all even numbered bytes reside in bank A of the WCS, while all odd bytes reside in bank B.

BYTE	MS							LS
0	7	6	5	4	3	2	1	0
1	MWR/	MCEN/	PROT/	SLVWR/	SLVRD/	ADDREN/	OREGWR/	CPCLK
2	15	14	13	12	11	10	9	8
3	23	22	21	20	19	18	17	16
4	IORD/	IOWR/	WOE/	WADB4	WADB3	WADB2	WADB1	WADB0
5	-	-	-	-	-	-	-	-

The bytes 0, 2, and 3 are used to specify the offsets to the MMU. Byte 0 is latched during phase B/ and bytes 2 and 3 are latched during phase C/. Offset bytes are latched into the MMU augend registers which are summed with the output of the current position counter, which provides the addends for the calculation of the row-col addresses. These offsets are provided in the microcode as the 2's complement of the offset. Byte 1 is used to specify the source or destination of all audio transfers except for the Wet bus transfers. Each bit is described below.

CPCLK
Cureent Position Clock: used to clock the current position counter. The rising edge of this signal is the clocking edge to the counter; the falling edge clocks the value of the counter into the output registers.

OREGWR/
Output Register Write: clocks audio data from a source into the Wet bus output registers. Sources may be the Slave audio registers, audio memory, or the Wet bus.

ADDREN/
Address Enable: used to enable the micro controlled portion of the SME to access the audio store. During normal operation the DMA address circuitry is enabled for addressing the the audio store.

SLVRD/
Slave Read: used to enable data onto the DAB from the slave's audio data registers.

SLVWR/
Slave Write: used to clock audio data from the DAB into the slave's audio registers.

PROT/
Protect: used in conjunction with any audio access from the microcoded section of the machine. Its purpose is to prevent access to the DAM by the DMA section. The bit will be automatically set by the micro-assembler when appropriate. It must be pipelined one instruction ahead of the micro-instruction which requires access to the DAB.

MCEN/
Memory Control Enable: indicates a microcoded memory operation is occurring.

MWR/
Memory Write: used to indicate either a read or write to the audio store. It is used in conjunction with MCEN

Byte 4 contains the five Wet address bits used by each HSP to address all I/O ports in the system. A total of 32 addresses for I/O are provided. The I/O map is provided below.

HEX ADDRESS	I/O FUNCTION
10h	READ WET CH0
11h	READ WET CH1
12h	READ WET CH2
13h	READ WET CH3
14h	READ WET CH4
15h	READ WET CH5
16h	NOT USED
17h	NOT USED
18h	D/A PRIMARY LEFT
19h	D/A PRIMARY RIGHT
1Ah	D/A SECONDARY LEFT
1Bh	D/A SECONDARY RIGHT
1Ch	A/D IN LEFT
1Dh	A/D IN RIGHT
1Eh	WRITE XREG
1Fh	READ XREG

Bit 5 WOE/ enables all wet transactions. It is used to enable the wet output registers onto the bus or for reading from the Wet bus onto the DAB. The two most significant bits of byte 4, IORD/ and IOWR/ indicate a read or write operation during a wet I/O operation. For phantom reads the IORD/ bit is set low without setting WOE/ low. The last byte of microcode (byte 5) is not used.

4.8.3 Micro-Pipeline

The micro-pipeline is responsible for aligning microcode for driving the SME board through the proper phases of operation. Offset information is clocked directly from the WCS into the registers U152-U154. Control information is clocked into register U174 and is realigned by U165 and U137. These bits provide source and destination information for movement of data on the Memory Data bus (MD). Register U150 receives WET bus control and address bits from the WCS. These bits are reclocked by U158 and are used when a WET bus operation occurs.

4.8.4 Memory Management Unit

The memory management unit is responsible for providing offset pointer information to the Digitized Audio Memory (DAM). Offsets from the WCS are clocked into U152-U154. This information is subtracted from the current position pointer contained in counters U109-U111. The current position counter is clocked by setting CPCLK/ active in the microcode. The counter can also be cleared by setting CPCC/ low in the Slave status register. The result of the computation generated by adders U127-U129, U139 and U140 is used to generate nine bits each of row and column information for DAM addressing. Two bits for bank selection are also generated to select the 256k word bank currently used. Multiplexers generate the row and column information by manipulating the SEL line.

4.8.5 Digitized Audio Memory

The Digitized Audio Memory (DAM) is composed of four banks of 256k words. A word is composed of eighteen bits. These four banks are:

Bank 1: U68-U85
Bank 2: U47-U64
Bank 3: U28-U45
Bank 4: U7-U24

The memory has been designed to have DMA accesses performed by DMA controller U155 or to perform normal micro accesses from the DSP. The selection of the provider of row-column addresses is determined by the ADDEN/ bit in the microcode. The default case has the DMA controller providing the addresses. The drivers responsible for providing addresses to the memories are U67 and half of U105 for micro accesses and U88 and the other half of U105 for DMA accesses. Bank selection is decoded using OFSA bits 0,1 for micro accesses and address bits A1 and A2 for DMA addressing. For RAS, CAS generation PAL U178 is used. Half of U4 and half of U5 generate the selected bank RAS and CAS signals. By selecting only one bank at a time the power requirements of the system are greatly reduced. Termination resistors U6,U46 and U86, along with series resistors R1 and R8-R15 provide signal conditioning of the row addresses. DMA accesses are byte wide accesses. The bank is selected as above but the byte high or low is selected by decoding address bit A0 of the DMA. The decoding is performed by U121, U147 and half of U4 and U5.

Note: Data transfers via the DMA port result in only 16 bit words being stored. The low two bits of the audio are discarded.

4.8.5 Disk Interfaces and DMA (Not supported as of V. 2.0 software release)

The SME board has been provided with two possible disk interfaces. Only one interface can be populated on the board at a time. The two interfaces provided are:

1) Floppy disk interface
2) SCSI interface

The Floppy interface is composed of floppy disk controller U156, driver U157, open collector drivers U167 and inverters U179. This interface can potentially be connected to 8 inch, 5.25 inch and 3.5 inch floppy drives. Floppy interfaces require a 34-pin header located at the front edge of the board.

The SCSI interface is the industry standard 5380 SCSI controller along with termination resistors U116-U118. The standard connector used by this interface is a 50-pin header.

The DMA operates in the following manner for disk requests. The DMA controller is programmed by the Slave processor to perform Memory - I/O transfers, byte wide. For example, assume a request for service comes from the floppy controller (or SCSI). The controller issues a DRQ/ to the DMA controller. The DMA controller issues a request to the Slave for access to the Slaves bus by asserting HLDREQ/. If the Slave accepts the request it relinquishes its bus and asserts BUSACK/. This event then causes PAL U102 to issue DMAOK/ to the RAS /CAS Pal U178. If the PROT/ bit of the microcode is not active then this PAL issues HLDACK/ to the DMA controller to start the memory access. The DMA controller asserts IOWR/ or IORD/ to the disk controller and simultaneously generates the memory address to be accessed in the DAM. Buffers U97 and U99 are used to write information to the DAM and latches U89 and U98. Addresses for row and column are provided by multiplexers U122, U151 and U175. Once a byte has been transferred the process begins all over.

4.8.6 Wet Bus Interface

The WET bus interfaces exactly as the HSP board, except for the fact that the SME board has only one read address (RDWET0-RDWET5). Register U158 drives the addresses and control bits out to the WET bus when WOE/ is asserted. U168 provides decoding for interprocessor data exchange. Registers U119, U131, and U144 provide audio input to the SME from the WET bus and U120, U135 and U143 provide output audio to the WET bus. Data is read from a WET bus address and clocked into the input registers for reading onto the DAB on a subsequent cycle. Data is written from the DAB to the output registers and is read or driven out to another WET address in a subsequent cycle.

5

Troubleshooting Guide

This chapter contains troubleshooting procedures to help locate malfunctions in the 480L. A good knowledge of digital and analog electronics is assumed.

5.0 Introduction

This chapter is divided into seven sections:

5.1 Visual inspection
5.2 Shock, heating, cooling testing
5.3 Recommended repairs and maintenance
5.4 Engineering change orders
5.5 Diagnostics (Host Rev. 2 and up)
5.6 Diagnostics (Host Rev. 1)
5.7 Problems and possible solutions
5.8 General
5.9 Letter Codes

5.1 Visual Inspection

Always perform a complete visual inspection of the system and installation prior to any troubleshooting.

1. Thoroughly inspect the 480L for any physical damage (inside and out). Verify that the potentiometers, sliders, switches, jacks, screws, rivets, card retainer and cables are installed and secure.

2. Remove top and bottom covers and verify that all internal parts (printed circuit boards, cables, integrated circuits etc.) are secure.

3. Verify that the voltage select switch is in the correct setting for the line voltage used. (100, 120, 220 or 240 VAC). Refer to the 480L *Owner's Manual* for details)

Primary (Rear Panel)	Secondary
100/120v - 3 AMP SLO-BLO 220/240v - 1.6 AMP SLO-BLO	+5 V Supply F1 = 6.3 AMP SLO-BLO (Supply board) +5/+15V Supply F1 = 1.25 AMP SLO-BLO (Mother board) -15V Supply F2 = 1.25 AMP SLO-BLO (Mother board) +20V (LARC) Supply F1 = 1.25 AMP SLO-BLO (Backplane) +5 (Automation) Supply F2 = 1.25 AMP SLO-BLO (backplane)

Table 5.1. Fuse Rating.

4. Verify that all fuses are good.

5. Verify that lead dress is neat—no pinched wires.

6. Verify proper installation of jumper blocks, as described below

Rev.1-2 Motherboard: W1, 2, 3, 4 = 1-2. W5-12 = 2-3 (transformerless) 1-2 (with transformers). W13 installed unless customer has removed to float chassis from analog ground.

Rev.1 V1.23 Host: W1 none, W2 none, W3 none, W4 1-2, W9 2-3, W10 2-3, W11 1-2, W13 1-2, W14 2-3, W15 2-3, W17 1-2, W18 2-3, W20 2-3

Rev.3 Host: None

Rev.1,2 Hsp #1: W1 none, W2 1-2, W3 1-2, W4 none, W5 none, W6 none, W7 1-2, W8 none, W9 none, W10 1-2, W11 1-2, W12 none, W13 none, W14 none, W15 none.

Hsp #2: W1 none, W2 none, W3 none, W4 1-2, W5 1-2, W6 none, W7 none, W8 1-2, W9 none, W10 none, W11 none, W12 1-2, W13 1-2, W14 none, W15 none.

7. Verify that bodies of all regulators are open circuit to heatsink (meter to lowest scale) U17 motherboard U2, Q1 on power supply board.

8. Inspect for any flux on boards, poor solder joints, bent pins, damaged PC board traces or broken cables.

9. Power on the unit and verify that the cooling fan is operating quietly. (no rubbing or clicking)

10. Verify that all power leds, and pilot light are on.

11. Verify proper seating of all components and assemblies.

5.2 Shock, Heat & Cooling Testing

Note: All of these tests should be done with care in mind (think nondestructive!).

Shock or vibration testing may be used to assist with a failure which is intermittent. Tapping lightly on the PC boards or rocking the system on a bench top may help locate the source of the problem. Twisting p.c. boards on an extender card is also useful. When shock testing

is used, the following guidlines should be followed:

For intermittent audio problems, input a 300Hz tone, listen to all outputs (or the problem output) while shock testing. Keep one corner of the unit touching the bench at all times. Always inspect all boards to be sure nothing was loosened. Move a probe from stage to stage while shock testing to isolate a defect. With digital problems it will be more difficult to isolate. Swapping boards with a known good unit would be most helpful if available. Use the diagnostics as a tool to help determine the board level of the problem. You can also use the unit with one HSP at a time jumpered as a HSP 1 (see visual inspection for jumpers).

For heat testing, be sure not to exceed the specified temperature of components in the system.

Use of heat (such as powering on the system with all covers on over a period of time) is helpful in recreating an intermittent failure condition. Restricting air flow through the unit by blocking part of the fan intake will raise the temperature of the unit. A heat gun or hairdryer is a good tool to isolate heat-related problems. Sometimes the problem may only happen when the unit is first turned on. This type of failure can be isolated by the use of freeze spray. Combinations of the above will help isolate intermittent problems.

5.3 Recommended Repairs and Maintenance

Here are some suggestions on how to approach troubleshooting.

First, some items which should be performed on all 480Ls in for repair.

1. Clean all rotary pots and jacks on mainframe and sliders on LARC with non-residue cleaner by spraying and working the part through it's full range, or installing aplug into a jack.

2. Verify seating of all components firmly into sockets.

3. Inspect cable connectors for good connection and crimp.

4. Reseat cables and clean with no-residue cleaner.

5. Vacuum the entire unit and clean air filter. The air filter should be cleaned every six months. Clean with mild detergent and water.

6. Remove VRTX foil label on HOST board and place a paper label under it. This aluminum label was attached to the PC board on early units and can cause intermittent shorts to vias. If VRTX label will not hold after removal use adhesive tape. This label is required for software use agreement.

7. Upgrade software to V1.23 if not already at this level or higher.

8. On the power supply, change R13 to 202-00501 1/2W 5% 150ohm, R6 to 203-02655 1/8W 1% 6.04K, and C5 to 245-03610 .01 uf 100 V Ceramic. This will eliminate power supply noise. (s/n 1008-1018, 1021 only) All other units have this done.

9. On motherboard change R239 to 220 ohm 1/4W 5% 202-00518. This will speed up mute. (S/n1000-1090 only) (Effective s/n 1091).

10. On motherboard add eight capacitors to hybird amp LLA5200 C229-236 33pf 245-03868. This will improve high level output performance. (S/n 1000-1148 only) (Effective s/n 1149).

11. Check battery voltages on HOST.

5.4 Engineering Change Orders

Chassis. Change gnd from poprivet to screw/nut (effective s/n 1181). This was done to comply with European requirements.

Front panel basket. Weld four corners 700-04393. Mechanical changes for structural strength and new packing material.

Host. Cut etch on host Rev.1 only U104 pin 1. This eliminates problem of noise due to and unused 8 MHz clock going to backplane. (Effective s/n 1351.)

Add pull up resistor AS/ to correct power up. Remove Rev. 3 pull down resistor on ZCLK. Rev. 1 = add 10K 202-00549 from pin 11 U22 to C19 (+5vdc). Rev. 3=add 10K 202-00549 from pin 11 U20 to C18 (+5vdc). On Rev. 1 only, remove R62 pull down from U44.7 to feedthrough. (Effective s/n 1439 "C".)

Rev. 3 and up, change 350-05801 peak pal to V1.10 to correct intermittent headroom indication without input. (Effective s/n 1498.)

HSP. Change U45 to 330-04567 74HCT32 (was F32). (Effective s/n 1550 "C".)

Power supply. Change R13 to 202-00501 1/2W 5% 150ohm, R6 to 203-02655 1/8W 1% 6.04K, and C5 to 245-03610 .01uf 100V Ceramic. This eliminates power supply noise (s/n 1008-1018, 1021 only). All other units have this done.

Motherboard. Change R239 to 220 ohm 1/4W 5% 202-00518. This will speed up mute (s/n 1000-1090 only) (Effective s/n 1091).

Add eight capacitors to hybrid amp LLA5200 C229-236 33pf 245-03868. This improves high level output performance (s/n 1000-1148 only) (effective s/n 1149). See schematics for placement.

Change R28 to 330 ohm 202-00521 to improve opto-isolator time over temperature. (Effective s/n 1382.)

5.5 Diagnostics–Host Rev. 2 and up

5.5.1 Internal Diagnostics

The 480L Cartridge Diagnostics are designed to run with Version 1.23 software and later releases. This software has a built-in start-up procedure which runs automatically when the 480L is powered on. Before performing cartridge diagnostics, power on the 480L with no cartridge in the cartridge slot and allow this start-up procedure to run.

If all four of the Host board LEDs turn off and remain off, start-up has run properly and you can procede to cartridge diagnostics. If any or all of the LEDs remain on, refer to the following information.

All four LEDs remain on X X X X

This indicates failure of the initialization routine. The first task that the 68008 performs is to load the PC (program counter) and SP (stack pointer). This occurs during the first eight instruction cycles. The information is fetched from the first eight locations of ROM 0 (U40). The enable signal for U40 is generated by U28 pin 9. If these initial fetches are incorrect the system will not start correctly. If the fetches are correct and the processor starts correctly then the processor writes to DUART 2 (U6). The DUART is loaded with the information to turn off the LEDs connected to the output of U11. If the code is correct then the LEDs go off (the outputs of U11 are high). Failure in the mode may be caused by:

Defective U34 (68008) .

U14 (osc), U13 (HCT393) failing to produce 8MCLK (8MHz processor clock) for the processor (U34 pin 34).

U36 (4538), U37 (LS03) failing to produce either Halt/ or Reset/. A 120 ms time is required to properly reset the 68008 on power up.

U28 (HCT165), U48 (HCT04) failing to produce a correct MAP/.

U23 (PAL 16P8) failing to produce MEMSEL. This could be caused by a defective PAL or IACKSTB/ being low on power up (check U21 pin 6).
U24 (PAL 16P8) failing to produce ROM0/. This signal enables ROM0 for fetching instructions.

One other mode of failure is caused by more than one device driving the data bus simultaneously. Check U26 (HCT244), U35 U38 U39 (4364/256 RAMS), U6 U7 (DUARTS), U29 U33 (HCT245), U85 U72 U58 (HCT374), U63 U64 (HCT374) to insure that all OE/ pins are high.

Check U34 pin 31 to see if DTACK/ occurs. If it does not check to see if BERR/ U34 pin 40 is low. If it is, check U10, U27, U21.

LED 1 stays on X O O O

This indicates failure of the Host ROM checksum test. This test checks to see if the ROM (U40) can be entirely read. The sum of all bytes of data is computed by the processor in a 16 bit value . This value is added to the stored checksum and the result must be read. Failure can be caused by:

defective Pals U23 U24
defective ROM U40
address bus shorted or open

LED 2 stays on O X O O

This indicates failure of the RAM test. Several tests are performed to check RAMs U38 and U39 nonvolatility (battery backup). The RAMs are tested by checking to see if a value was stored before the last time the system was powered down. A value is written and then read to verify the write. If failure occurs after the second power up:

Check RAMs U38 U39; U47 (LS03) pin 3,6,8,11; U48 (HCT04) pin 12,10.
Check batteries voltage.
Check DUART U7 (DISRAM) pin 15 for a low; U46 (RAMBUFEN) pin 1 for a high.

5.5.2 Cartridge Diagnostics

Never insert or remove the cartridge with the power on. Power down and insert the diagnostics cartridge into the cartridge slot of the 480L.

Make sure that the cartridge's Write Protect switch is set to ON, and that there is a LARC connected to LARC Port 1. Any combination of HSP or SME boards can be tested at a time, as long as they are jumpered so as not to conflict with one another.

Note: SME boards must be jumpered as either Slave 0, 2 or 4. In order for the SME SLVREG test to pass, there must be at least one regular HSP board in the system. A MIDI cable must be connected from MIDI OUT to MIDI IN for the MIDI test to pass.

The following jumper positions are required:
SME:

SLAVE 0	Jumper	W1,W4,W18
SLAVE 1	Jumper	W2,W5,W20
SLAVE 2	Jumper	W3,W6,W22

All configurations must have jumpers at W12, W13, W14 and W15.

Turn on the 480L and a series of messages will appear on the LARC. The Diagnostics Cartridge determines what boards are present in the system and displays that information in the area above the six sliders. The display above the sliders correspond, from left to right, to Slave 0-5. If this information is incorrect, it is probably due to DMA failure. Refer to the DMA Test troubleshooting procedure for the appropriate board, described below. After the "SLAVES IDENTIFIED" mesage, the display will switch to: "RUN TESTS BANK1 PGM 1." "PGM 1" will be blinking, signifying that the diagnostics are in program mode.

There are four banks of test programs. Bank 1: ALL TESTS, contains two programs which run all the tests one after another, either once or repeatedly. Bank 2: HOST TESTS, contains four tests which can be run separately to test the Host board. Bank 3: HSP TESTS, contains ten tests which can be run separately to test the HSP board. Bank 4: SME TESTS contains tests to test the SME board.

Bank Mode is used for selection of tests; tests can only be run in Program Mode.

To switch from Program Mode to Bank Mode, press the BANK button once and the "BANK 1" portion of the display will start blinking. Pressing BANK repeatedly will cause the display to switch between banks. When the display shows the bank you want, press PROG to return to Program Mode. Program 1 of the bank you have selected will be displayed in the upper display. From Bank Mode pressing one of the buttons numbered"1," "2," or "3" will switch banks and put the system directly into Program Mode. In Program Mode, pressing PROG will switch the display to the next program. To run a test, press the button corresponding to the test you want to run. The upper display will show that program.

While a test is running, the upper display shows the name of the test, and the lower display shows the number of the slave being tested. If all the slaves pass, the display will eventually print "TEST COMPLETED." If there is a failure, an error message will appear in the lower display and the upper display will read: "PRESS PAGE TO CONTINUE." Pressing PAGE will cause testing to resume and continue to the end. When all the slaves have been tested, the "TEST COMPLETED" message will appear, regardless of how many slaves passed or failed. The bank 1 program: RUN TESTS is the equivalent of running all of the Bank 2 and Bank 3 tests one after another. If there is a failure, pressing PAGE will cause testing to resume and continue to the end. The Bank 4 program: SME ALL TEST works the same way on the SME tests.

The Bank 1 program: "RUN INFINITE" is the same as RUN TESTS, except that after the second to last test it loops around to the beginning and starts again. The only way to stop this test is to power down.

The first test in Bank 2: RAM TEST, also runs in an infinite loop. It exercises the Host board while flashing "RUNNING RAM TEST" on the LARC.

When running any of the tests in Bank 3: HSP TESTS, it is important that Program 1 of that Bank (WCS TEST) be run first to initialize the Writable Control Store. Likewise, in Bank 4, the WCS test must be run before CPC, SLVREG, MEM or ADDR.

When testing has been completed, power down the 480L before removing the diagnostics cartridge.

The tests in the Diagnostics Cartridge were designed to be run sequentially, with each successive test checking a more remote function of the system. If a test fails, later tests which depend on the failed function may not produce valid results. Run the Bank 1: RUN TESTS program first. If there is a failure, begin by troubleshooting the first test to fail.

Below are detailed descriptions of the individual tests. In these descriptions, "SLAVE 0" refers to the first slave on an HSP Board, which could actually be Slave 0, 2 or 4, depending on how the board is jumpered. Likewise, "SLAVE 1" can refer to Slave 1, 3 or 5.

1. Bank 2 PGM 1 RAM Test

This test exercises the Host's address bus, data bus, and control lines. It writes to and reads from RAM, testing locations 8100H to 2000H. The data written to any location is the same as the address for that location. As long as the data read from a location is the same as that written into it, the test loops in this mode indefinitely. If there is an error, a failure message is displayed. Pressing PAGE will cause the test sequence to resume. *This test wipes out data stored in user registers.*

2. Bank 2 PGM 2 MIDI Test

In this test DUART 1 (U7) passes data from its serial output to its serial input. If failure occurs:

Check MIDI cable.
Check U7 pin 30,31 transmit/receive.

3. Bank 2 PGM 3 DMA Test

The DMA test checks communication between the Host and the HSP boards. The test program asserts BLOCK/ on DUART 1 U7 pin 27. It then begins writing values into slave memory space and reading them back. There are two types of errors that can occur with the DMA test: Bus Error or Bad Data. A Bus Error occurs if the 68008 does not receive a low on DMADTACK/ after addressing slave address space. This produces the error message "SLAVE X NOT RESPONDING." Since all subsequent tests involve writing to slave memory, a failure in this mode will produce similar results in all later tests. A Bad Data error occurs if the 68008 receives a DMADTACK/and writes and reads slave memory, but does not read back correct data. This produces the error message "DMA TEST - SLAVE X FAIL."

Bus Error: The 68008 writes the appropriate address of SLAVE0 or SLAVE1 to U44. This is decoded by U31 (HCT138) and passed into U32 (HCT244). One of the outputs of U32 is low, depending on which slave is being tested. Only one output of U32 should be low at any given time. If failure occurs:

Check BLOCK/ on U49 pin 2 (HCT00); it should be high.

Check the outputs of U44, U31 and U32 to make sure that these ICs are operating properly.

If these conditions are correct, check U33 (HCT245). This IC can be dynamically checked by powering the unit off and then on. When the DMA test is run, strobing should be seen on pin 9 of U33 and data should change on the outputs.

If everything appears to have the correct levels check DMAACK/ at pin 12 on U51 (HCT02); it should be low. Also try powering unit off and then on and see if U16 pin 11 (HCT175) produces DMADTACK/ during this test.

If the Host board is sending a DMAREQ/ to the HSP board but receives no DMAACK/ back, follow the signal path through the HSP board. When a DMAREQ/ is received by the HSP board W2 and W3 rout it to U29 (HCT244). These signals are fed to the BUSREQ/ pins on Z80 U4 or U31 (pin 25). The Z80 is then required to acknowledge the request by pulling BUSACK/ pin 23 low. This signal is wired or'd to produce DMAACK/. If failure occurs check that BUSREQ/ on the failed processor is low. Check that U29 (HCT244) pin 16 or 14 is low. Check that jumpers W2 and W3 are in place. If all of the above are correct check:

ZCLK at pin 6 of Z80s
WC/ at pin 8 U101 (F32)
RESET/ is high on pin 26 of U4 or U31 and U30 (HCT175) pin 7 or pin 15.
Check SR/ pin 1 U30 (HCT175) is high.
Check that INT/ is high at pin 16 of the Z80s and at U30 pin 2,10.

Bad Data: If the Host is able to write and read slave memory space but reads back bad data, check the integrity of the data path.

For SLAVE0 check:

U1,U2 (HCT244), U3 (HCT245) for enables at pins 1,19
U41 (HCT244) pin 18,16 (MREQ/, WR/).
U6 (HCT139)
U5 (4364)

For SLAVE1 check:

U16,U17 (HCT244), U18 (HCT245) for enables at pins 1,19
U41 (HCT244) pins 7,9 (WR/, MREQ/).
U33 (HCT139)
U32 (4364)

4. Bank 2 PGM 4 Interrupt Test

In the Interrupt Test the Host downloads a program to the slave. This is done by first releasing reset then requesting the slave BUSREQ/ by DMAREQ/. Once the bus is obtained the program is written into the slave RAM. The slave is reset then released from reset. The slave now runs the downloaded program. The program requireses the slave to interrupt the Host 1000 times. When the slave has asserted 1000 interrupts, it clears a designated memory location to let the Host know it has finished. The Host monitors this location and upon finding it cleared checks to see how many interrupts it received. An error occurs if either too much time passes before the memory location is cleared, or if it is cleared but the Host finds that there were an incorrect number of interrupts. If a failure occurs, check the path of the interrupt signals.

HSP Board:

Check U6 or U33 (HCT139) pin 10 (SLVINT1/ or SLVINT2/).
Check U52 (HCT03) pin 8.

Host Board:

Check U20 (HCT244) pin 3 (SLAVEINTB/).
Check U8 (HCT74) pin 9 and U17 (HCT148) pins 6,7.

5. Bank 3 PGM 1 WCS Test

In the WCS test the Host downloads a program telling the slave to write values from 0-255 to each bank of the WCS and read them back. When the slave finishes this and the correct values have been read then the slave writes to a known memory location which the Host reads to verify results. If the test fails, the slave is left doing reads and writes to the failed address. Once the error message is received, look at the hardware surrounding the WCS. Sync the scope on the enable pins of the HCT244s or the enable pin of the HCT374s to verify that the data written to the 2018 RAMs is the same as that being read. The slave which has failed will loop in this mode until PAGE is pressed.

For SLAVE0 failure check:

A1/ on U21 & U8 pin 2 (F32)
U10, U11, U12 (F157)
RD/ & WR/ strobes at U21 & U8
U22 & U24 (HCT374) for reads
U23 & U25 (HCT244) for writes
Check U13 & U14

For SLAVE1 failure check:

A2/ on U45,U35 (F32)
U37, U38, U39 (F157)
RD/ & WR/ strobes at U35 & U45
U46 & U48 (HCT374) for reads
U47 & U49 (HCT244) for writes
Check U26 & U27

6. Bank3 PGM 2 Zero Delay

Once the operation of the WCS has been verified, the first microprogram loaded is a zero delay program with no attenuation i.e. a multiply by 1. The purpose of the test is to verify the operation of the WET, ADDRESS, DATA, and CONTROL busses. A microprogram is downloaded to the microstore (WCS). This program reads from the Host XFEROUT registers U59, U73, & U86 and writes back to the Host XFERIN registers U58, U72, & U85. The Host writes the value AA AA 40 to the XFEROUT registers. This value is read by the microprogram and written back unchanged to the XFERIN registers. If the Host reads the correct value then it writes 55 55 80. If there is a failure the LARC will display which byte of the value written was bad, and which slave caused the failure. In this and all subsequent tests through the Allpass Filter test, a failure by one slave will cause the same microprogram to be loaded into the other slave's microstore, so that side-by-side comparisons may be made. Both microprograms will continue to run until PAGE is pressed.

On the Host board:

For testing the transfer registers on the Host sync a scope on pin 1 of U59 (low byte), U73 (mid byte), or U86 (high byte). This signal will allow reading of the value which has been written to the registers.

If there is no signal, check U95 (HCT138) pin 7 and IORD/ at U98 pin 9.

If the data is found to be bad at the outputs of these registers check U88 (HCT138).

If the data is correct, sync the scope on pin 11 of U58 (low byte), U72 (mid byte), or U85 (high byte). This is the output strobe generated by the microcode.The data sent by the HSP can be seen at the inputs to these registers.

If no strobe is found check pin 9 on U95 (HCT138) and check that IOWR/ is low at U98 pin 10.

If a byte is found bad but all of the above signals are correct, the problem resides in the HSP.

On the HSP board:

On the HSP the micropipeline is used minimally. The MMU is not used nor is the dynamic RAM. The Zero Delay test exercises the WETBUS addresses and control, and several bits of control for the ARU. WETBUS addresses used are 1FH for reading the XREG and 1EH for writing the XREG. These addresses can be validated in the pipeline at U106 outputs for SLAVE0 (sync on pin 1) and at U107 outputs for SLAVE1.

On U109 check for strobing on pins 11,15 for SLAVE0 and pins 3,7 for SLAVE1. These strobes should occur once every sample.

On the input of data SLAVE0 uses U72, U74 and 1/2 of U57. Check U72 (high byte) and U74 (mid byte) for AAH or 55H at the inputs.

Check U57 (low byte) for 40H or 80H at the inputs. The corresponding buffers of SLAVE1 are U85, U87 and 1/2 of U56. By syncing on pin 1 of these buffers a scope can be used to see the data at their outputs.

If this sync pulse is not found check the IORD/ lines at U109.

If data is valid at the input buffers to the DAB check pin 29 (XCLK/) of the ARU (U60 for SLAVE0; U89 for SLAVE1). This strobe should occur once a sample cycle.

XCLK/ clocks data from the ACCU of the ARU to the output register of the ARU. Data is now passed to the output registers (U73, U75 and U58 for SLAVE0; U86, U88 and U59 for SLAVE1). The data is first written to the registers, and then passed to the WETBUS on the following cycle.The writing of the data can be validated by syncing on pin 11 of these registers and checking the data inputs. The passing of the data to the WETBUS can be validated by syncing on pin 1 of U73, U75 or pin 19 of U57 (SLAVE0); pin 1 of U86, U88 or pin 19 of U56 (SLAVE1).

If no strobing is found on these pins check U108, U110 and U101 (SLAVE0); U42, U110 and U101 (SLAVE1). If this test passes a large portion of the HSP data paths has been validated.

7. Bank 3 PGM 3 Double Precision Multiply Test (xAA)

This test is used to verify operation of the multiply circuitry around and in the ARU. Double precision insinuates an eight bit multiply. The eight bit multiply occurs over two micro-instructions. The first coefficient used is AAH. If SLAVE0 fails sync on DP1/ (pin 9, U63). This bit should be low for an instruction cycle once a sample period. If this is correct check the outputs of U70. The value AAH should be seen. If the value is correct sync on CLKEN/ at pin 1 of U116. When CLKEN/ is low and A1/ goes high, the outputs of U79 pins 2, 5, 6, 9 and 12 should be 0AH respectively. These bits should also appear at the outputs of U78 on the rising edge of B/. During the second half of the multiply (CLKEN/ is now high as well as DP1/), the value at the outputs of U78 should be 05H for C1<0:4>. This value can be seen by syncing on DPDX1/ (pin 19 of U78), which will be low. Refer to Figure 5.1 for the output of U76 and U61 for proper signals to the ARU. If all signals appear correct, the ARU may be at fault. For SLAVE1 failure check U92 pin 9 for DP2/. Check the output of U99 for AAH. Check the input of U116 pin 4 for CLKEN/. Check the outputs of U114 and U115 as described above and finally the outputs of U113. The outputs of U111 and U90 should follow Figure 5.1.

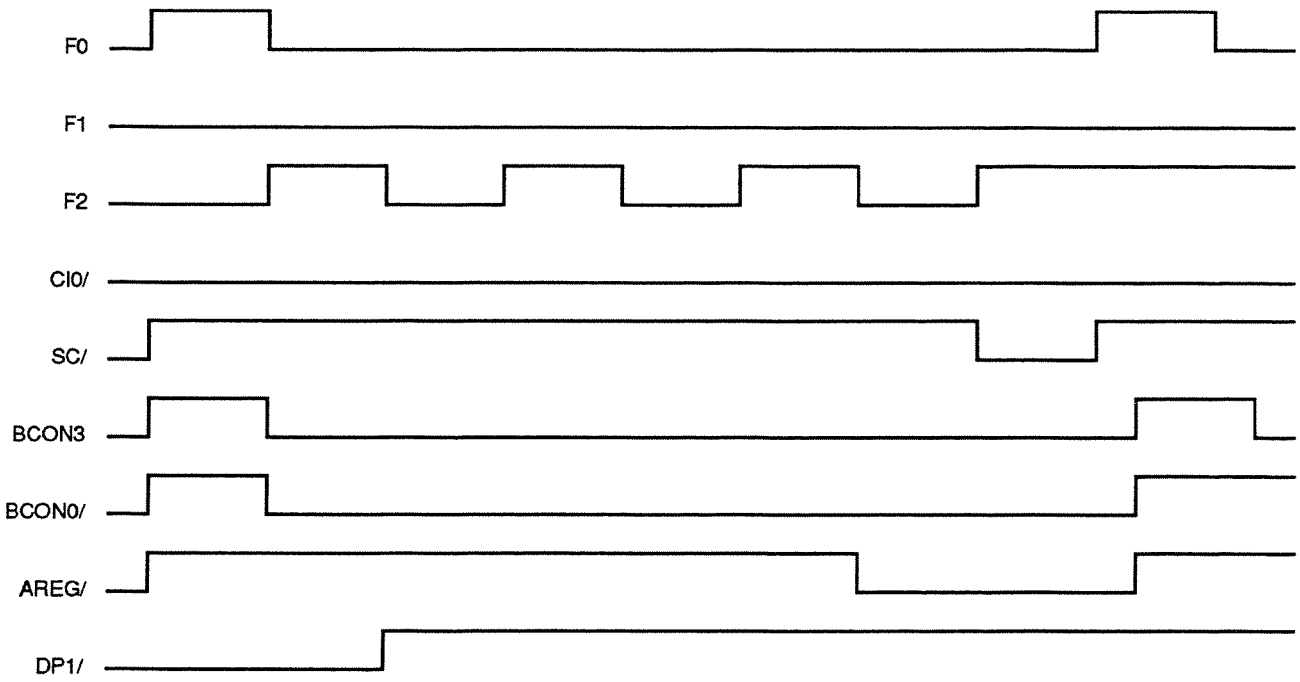

Figure 5.1. Double Precision Multiply Test (xAA).

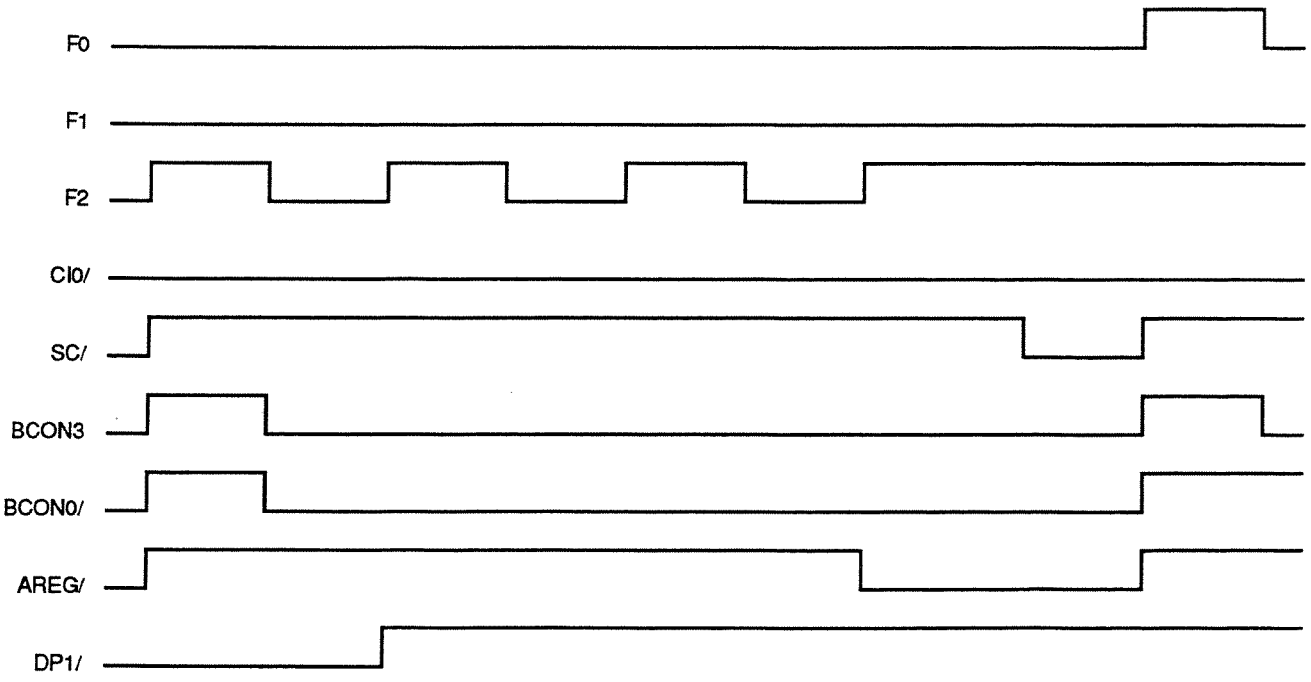

Figure 5.2. Double Precision Multiply Test (x55).

8. Bank 3 PGM 4 Double Precision Multiply Test (x55)

This test is the same as the test above except that the coefficient used is 55H. The value of C<0:4> should be 15H during the first half of the multiply and 02H during the second half. Figure 5.2. shows the outputs of U76 and U61 (SLAVE0) or U111 and U90 (SLAVE1).

9. Bank 3 PGM 5 MMU Test

This test checks the operation of the Memory Management Unit. The Host passes the value AAAA40H to a microcode program which writes that value into audio memory. The MMU continuously increments the address, so that eventually all of memory is written with that value. Then the value 555580H is passed to the microcode program and the MMU is given time to move a few memory locations ahead. A value is read. If the value read equals 555580H, it is assumed that the memory addresses are not being incremented by the MMU and that the MMU is faulty. Check U69 for SLAVE0 and U98 for SLAVE1. The test is also performed writing 555580H first and then AAAA40H.

10. Bank 3 PGM 6 Full Delay AA x 1/2

During this test all locations in memory are written and read. Check the outputs of U50 (SLAVE0) or U55 (SLAVE1) to verify that RAS/ and CAS/ are cycling. If these outputs are not correct check that Delay U40 is functioning. Pin 12 should be delayed 30 ns from the input on pin 1. Pin 10 should be delayed 90ns from the input on pin 1. The RAS/ output strobes every cycle, but CAS/ only strobes when a memory operation occurs. By syncing on pin 13 of U50 or U55 one can observe all strobes for a memory operation. MCEN indicates that a memory read or write is taking place. Verify that MWR/ is low during write operations (U82, pin 11 for SLAVE0; U117, pin 11 for SLAVE1). Check that all signals reach the five dynamic RAM chips (U64-U68 for SLAVE0, U93-U97 for SLAVE1). If a slave fails this test the RAM at fault will be displayed by its reference designator. This Full Delay multiply uses data AAAA40H for the multiply. If all signals look correct and a failure is indicated, the ARU is suspect (U60 for SLAVE0, U89 for SLAVE1).

11. Bank 3 PGM 7 Full Delay 55 x 1/2

This test is the same as above except that the data used is 555580H.

12. Bank 3 PGM 8 All Pass Filter

The allpass filter is a common filter used in audio effects. This test utilizes short (7 bit coefficient) multiplies to check the operation of this filter.

If SLAVE0 fails:

Check for SHORT1/ low once a sample period (U63 pin 15 and U62 pin 17). If this appears to be correct then ARU (U60) failure is likely. The test is performed first with data A5A540H and then with data 5A5A80H.

For SLAVE1 failure:

Check SHORT2/ at U92 pin 15 and U91 pin 17. If this is correct then the ARU U89 is suspect. The same data patterns are used.

13. Bank 3 PGM 9 Peak Detector Test

This test is used to verify the operation of the headroom mechanism for the LARC. The peak detector detects positive peaks only and compares only the most significant byte of audio data. This test first clears the peak detector peak registers U61 and U62 on the Host board. The transfer register (U85 on the Host) is then loaded with data 01H. The left channel is tested first. The value 01H is compared to 00H in the peak register U61. After a brief wait the Host reads the left channel peak register U63. If the value 01H is read then the next value 02H is loaded and the process continues. Values from 01H to 7FH are tested. The right channel is then tested and U64 is read to obtain the peak value. If the test fails check to be sure that DAPRIML/ is strobing at U77 pin 4 and that DAPRIMR/ is strobing at U77 pin 5. Check that PEAKSEL/ at U77 pin 6 is high. If these signals are not present check the outputs of U95 pin 15 (DAPRIML/) or pin 14 (DAPRIMR/). Check that the address to U95 is 18H for DAPRIML/ and 19H for DAPRIMR/. Sync on the IOWR/ signal (U98 pin 10). If these signals are not present, check on the HSP board the outputs of U106. Also check to see that pin 5 on U74 is strobing occasionally. Also check for the RDPEAKL/ strobe (U77 pin 8) and the RDPEAKR/ strobe (U77 pin 9).

14. Bank 3 PGM 10 Two In Four Out

This test is used for testing the audio quality of the system. The two inputs on the rear of the machine are routed to the four outputs. The left input is sent to the left and right secondary outputs, and the right input is sent to the left and right primary outputs. Both outputs represent the unattenuated inputs.

15. Bank 4 PGM 2 SME DMA Test

The DMA test checks communication between the Host board and the SME board. The Host writes values into slave memory space and reads them back. There are two types of errors that can occur: bus error which produces the message "SLAVE X NOT RESPONDING" and bad data which produces the message "SME DMA TEST - SLAVE X FAIL." Since all subsequent tests involve writing to slave memory, a failure in this mode renders all the other SME tests invalid.

If the HSP DMA test passes but the SME DMA test fails, the problem is probably in the SME board and not the Host.

Bus Error: If the Host board is sending a DMAREQ/ to the SME board but receives no DMAACK/ back, follow the signal path through the SME board. When a DMAREQ/ is received by the SME board it is routed by W4, W5, or W6 to U101 (HCT244). From U101 DMAREQA/ goes to PAL U102 which pulls low the BUSREQ/ pin on the Z80 U66 (pin 25). The Z80 is then required to acknowledge the request by pulling BUSACK/ pin 23 low. This signal passes through PAL U102 causing HBUSACK/ (pin 14) to go low. HBUSACK/ low enables buffers U25, U65, U87 and the top half of buffer U101, allowing the Host access to the slave's memory space. Also, the enabling of buffer U101 causes the DMAACK/ signal to go low, acknowledging the Host's DMA request. f failure occurs check that BUSREQ/ on the failed processor is low (U66 pin 25). Check that U101 (HCT244) pin 7 and pin 14 are low. Check that the correct jumper W4, W5, or W6 is in place. If all of the above are correct check:

ZCLK at pin 6 of Z80 -WC/ at U145 pin 3
RESET/ is high on pin 26 of Z80
SR/ pin 1 U103 (HCT175) is high.
INT/ is high at pin 16 of Z80

Bad Data: If the Host is able to write and read slave memory space but reads back bad data, check the integrity of the data path.

U25,U65 (HCT244), U87 (HCT245) for enables at pins 1,19.

U101 (HCT244) pin 18,16 (MREQ/, WR/).
U26 (43256)

16. Bank 4 PGM 3 SME Interrupt Test

In the Interrupt Test the Host downloads a program to the SME. The program is for the slave to interrupt the Host 1000 times. When the slave has asserted 1000 interrupts, it clears a designated memory location to let the Host know it has finished. The Host monitors this location and upon finding it cleared checks to see how many interrupts it received. An error occurs if either too much time passes before the memory location is cleared, or if it is cleared but the Host finds that there were too many or too few interrupts. If a failure occurs check the path of the interrupt signals.

SME Board:

Check U87,U101,U103,U136,U124 Host Board:
Check U22 (HCT244) pin 3 (SLAVEINTB/).
Check U8 (HCT74) pin 9 and U19 (HCT148) pins 6,7.

17. Bank 4 PGM 4 SME WC Count Test

In the Word Clock Counter Test the Host downloads a program in which the slave tells the word clock counter to interrupt it after a specified number of word clocks. There are two possible types of failure, timeout error and count error. A timeout error occurs when the slave does not receive the expected interrupt within a certain time limit. Bad count means that an interrupt was received but not at the correct time. If there is a failure:

Check the word clock counter (U1, U2, U3) on the SME board. At the start of the test a value should be clocked into the counter registers (check WCCLKL/, WCCLKM/ , WCCLKH/ at pin 13 of U1, U2, U3) and this value should be loaded into the counters by CLOAD/ (pin 14).

Check for a valid WC/ at U3, pin 11. U3, U2, and U1 form a ripple counter.

The final output (WCINT/, U1 pin 9) clocks U136 pin 3, causing WCINT to be asserted. This signal passes through inverter U124 and pulls the INT/ line low, which causes the slave to be interrupted (U66 pin 16).

Check to make sure that none of the other interrupt lines are high (HSTINT U136 pin 9, DSKINT U142 pin 5, DMAINT U142 pin 9).

Check the operation of U106 (used to poll the interrupting devices) and U91 (used to clear the int flip-flops U136 or U142 once an interrupt has been serviced).

18. Bank 4 PGM 5 SME WCS Test

In the Wrieable Control Store Test the Host downloads a program telling the slave to write values from 0-255 to each bank of the WCS and read them back. When the slave finishes this and the correct values have been read, the slave writes to a known memory location, which the Host reads to verify results. If the test fails, the slave is left doing reads and writes to the failed address. Once the error message is received, look at the hardware surrounding the WCS. Sync the scope on the enable pins of the HCT244's or the enable pin of the HCT373's to verify that the data written to the 2018 RAMs is the same as that being read. If there is failure the slave will loop in this mode until PAGE is pressed.

SME board:

A/ on U146 & U132 (F32)
U148, U162, U172 (F157)
RD/ & WR/ strobes at U146 & U132
U159 & U169 (HCT373) for reads.
U160 & U170 (HCT244) for writes.
Check U149 & U173.

19. Bank 4 PGM 6 SME Host Interrupt Test

The Host Interrupt Test tests the Host's ability to interrupt the slave. The Host downloads a program to the slave telling it to set a known memory location to an error code. The slave then waits to be interrupted by the Host. When the interrupt occurs the slave clears the memory location, which is then read by the Host. If there is a failure, run the test again, checking that the Host interrupt disable line (CLRHST/ U136 pin 13) goes high during the test. (There is about a 1 second delay between the timne the button is pressed and the time the test actually runs.) If this signal is correct, check the path of the interrupt line from the host to the slave.

Host board:

Check U88,U33,U51

SME board:

Check HSTINT/ signal going low, U103 pin 2.

Check HSTINT signal going high, U136 pin 9.

Check the other int signals are low (WCINT, DSKINT, and DMAINT).

Check INT/ going low at U66 pin 16.

Check a single strobe on RDSTAT/(U106 pin 19) and data 01H on the slave data bus during this strobe (device polling).

Check HSTINT flag is cleared by WRSTAT/ strobing U91 pin 11.

20. Bank 4 PGM 7 SME CPC Test

The Current Position Counter Test is the first of the SME tests to use microcode. The Host first loads a microcode program into slave memory. It then loads a slave program and releases the slave. The slave loads the microprogram, which clocks the CPC 16 times per sample, into the WCS. It then clears the CPC and waits for a specified period of time. At the end of this time it reads the CPC. If the CPC does not contain the proper value, an error message is displayed and the DSP continues clocking the CPC 16 times per sample (until PAGE is pressed).

SME board:

Check U109, U110, U111 for CPCLK/ (pin 13) and its inverted version (through inverter U133 to pin 11).

Check incrementing binary count at outputs of U109, U110, U111.

Check single low strobe on CPCC/ at start of test (U109, U110, U111 pin 10).

Check single low strobe on CPSTOR/ at end of test (U180 pin 1), and subsequent rising edge on U93, U94, U95 pin 11. These signals clock the current address from CP bus into latches.

Check single strobes on read lines at end of test (CPCHI/ U95 pin 1, CPCMID/ U94 pin 1, CPCLOW/ U93 pin 1).

21. Bank 4 PGM 8 SME SLVREG Test

The Slave Register Test tests the operation of the transfer registers, wet bus, and slave registers. The Host first loads a microcode program into slave memory. It then loads a slave program and releases the slave. The slave loads the microprogram into the WCS. The microcode causes the DSP to perform two alternating functions. It reads the Host transfer registers, writing the value to the slave registers, and reads the slave registers, writing the value to the Host transfer registers. The slave, meanwhile, reads the slave registers and writes the value to a set of known memory locations, and also reads another set of known memory locations and writes the value to the slave registers. In this mode the slave and DSP are able to pass data in two directions. The Host first writes AAH to the transfer registers, waits a short time, then reads slave memory to determine if the value was transferred correctly (the bottom 6 bits must be masked off). The Host then writes AAH to slave memory, waits a short time, and reads the transfer registers. If these are correct, it repeats the procedure with the value 55H. In case of failure, the slave and DSP continue passing data. Follow the data path through the SME board in each direction.

SME Board:

Check slave registers U90, U96, U100 to see if slave is writing data (strobing on pin 1) and reading data (strobing on pin 3).

Check data at slave registers inputs/outputs for 55H or AAH pattern.

Check transfer registers U119, U131, U144 for data input from Host (strobing on pins 1 and 11, 55H or AAH pattern at outputs).

If no strobing is seen on pins 1 and 11, check U137 and Pal U125.

Check transfer registers U120, U135, U143 for data output to Host (strobing on pins 1 and 11, 55H or AAH pattern at outputs).

If no strobing is seen on pins 1 and 11, check for RDWETA/ signal (U168, U147, U163), IOEN/ (U91, U133), and WETWR/ (U180).

22. Bank 4 PGM 9 SME Memory Test

The SME Memory Test tests the 1 meg of audio memory on the SME board. The Host loads a microcode program into slave memory, then loads a slave program and releases the slave. The slave loads the microprogram into the WCS. The microcode causes the DSP to read the slave registers U90, U96 and U100, writing the value into audio memory. The DSP then reads the audio memory location that it just wrote to, writes the value back to the slave registers, and clocks the current position counter to the next location. It goes through this procedure once per sample cycle. At the beginning of the test the slave writes 55H to the slave register and clears the CPC. It then checks the slave register once per sample to make sure that the correct value has been written to it by the DSP. When the entire audio memory has been tested in this way (about 22 seconds), the slave repeats the test with the value AAH. If there is an error, the LARC will display the memory bank and the highest incorrect data bit. Since the data is stored one bit per chip, the bad data bit may correspond to a bad memory chip.

Also check for strobing on memory control lines RAS/ and CAS/, and on the write enable control (pin 3) of the memory chips.

If no strobing is seen, check U4, U5, U121, U147 and U178.

A "BAD ERROR CODE" message probably means the Host was interrupted to soon. Check U104, U179, U167. The SINT/ and SLVINT/ signals should strobe low once halfway through the test, and once at the end.

23. Bank 4 PGM 10 SME Address Test

The SME Address Test also tests the SME audio memory. It is different from the Mem Test in that there are two different microprograms used. During the first half of the test, the DSP reads the slave registers, writes the value into audio memory, and clocks the current position counter to the next location. The slave synchronously increments the value in the slave registers such that the value written into each location is the address of that location. During the second half of the test, the DSP reads the audio memory, writes the value to the slave registers, and clocks the CPC to the next location. The slave reads the slave registers once per cycle, expecting to find the value incrementing by one each time. If there is an error, the LARC will display the memory bank and the highest incorrect data bit. Since

the data is also supposed to be the address, the bad data bit might correspond to a bad address bit. Check the address lines:

The OFSA bus <0:19> (U127-9, U139 and U140) is the sum of the Current Position Counter outputs (U109, U110 and U11) and the OFSTB/ <0:19> outputs (U152-4).

The OFSTB/ outputs (U152-4) should all be zero during the test.

The Current Position Counter outputs (U109, U110, U11) should be incrementing in a binary count, as should the OFSA outputs (U127-9, U139, U140). Check for shorts in any of these lines.

The 18 OFSA signals are multiplexed into the 9 MAB signals by U108, U126 and U138. OFSA <2:10> become MAB <0:8> during the RAS/ part of the address cycle, and OFSA <11:19> become MAB <0:8> during CAS/.

Check for proper strobing of the SEL signal (pin 1 of U108, U126 and U138) which controls this multiplexing.

Check for shorts in the MAB, MA, and BMA address busses.

Check PAL U178 for RAS/ and CAS/ generation.

A "BAD ERROR CODE" message probably means the Host was interrupted too soon. Check U104, U179, U167. The SINT/ and SLVINT/ signals should strobe low once halfway through the test, and once at the end.

If the Mem Test indicates failure after an Address Test failure has been solved, it is probably because the memory had not previously been fully accessed by the Mem Test. This is one of many possible situations where solving a problem found by one test can uncover another problem. However, in this case (unlike most) the new problem would be found by a previous test.

5.6 Diagnostics — Rev.1 Host

5.6.1 Internal Diagnostics

The 480L Cartridge Diagnostics are designed to run with Version 1.23 software or later versions. This software has a built-in start-up procedure which runs automatically when the 480L is powered on. Before performing cartridge diagnostics, power on the 480L with no cartridge in the cartridge slot and allow this start-up procedure to run. If all four of the Host board LEDs turn off and remain off, start-up has run properly and you can procede to cartridge diagnostics. If any of the LEDs remain on, refer to the following information.

All four LEDs remain on ***X X X X***

This indicates failure of the initialization routine.The first task that the 68008 performs is to load the PC (program counter) and SP (stack pointer). This occurs during the first eight instruction cycles. The information is fetched from the first eight locations of ROM 0 (U40). The enable signal for U40 is generated by U30 pin 9. If these initial fetches are incorrect the system will not start correctly. If the fetches are correct and the processor starts correctly then the processor writes to DUART 2 (U6). The DUART is loaded with the information to turn off the LEDs connected to the output of U11. If the code is correct then the LEDs go off (the outputs of U11 are high). Failure in the mode may be caused by:

Defective U34 (68008)

U18,U16 (osc, HCT393) failing to produce 8MCLK (8MHz processor clock) for the processor (U34 pin 34)

U45 (4538), U52 (HCT132), U47 (LS03) failing to produce either Halt/ or Reset/; a 120ms time is required to properly reset the 68008 on power up

U30 (HCT165), U51 (HCT04) failing to produce a correct MAP/. U23 (PAL 16P8), U9 (HCT04) failing to produce ROMRAMSEL. This could be caused by a defective PAL or IACKSTB/ being low on power up (check U25 pin 6)

U24 (PAL 16P8), U25 (HCT08) failing to produce ROM0M/. This signal enables ROM0 for fetching instructions.

One other mode of failure is caused by more than one device driving the data bus simultaneously. Check U67 (HCT244), U38 U39 (4364/256 RAMS), U6 U7

(DUARTS), U35 U36 (HCT245), U89 U75 U61 (HCT374), U64 U66 (HCT374). Check to insure that all OE/ pins are high.

Check U34 pin 31 to see if DTACK/ occurs. If it does not check to see if BERR/ U34 pin 40 is low, if it is then check U28, 27, 29, 25.

LED 1 stays on ***X O O O***

This indicates failure of the Host ROM checksum test. This test checks to see if the ROM (U40) can be entirely read. The sum of all bytes of data is computed by the processor in a 16 bit value. This value is added to the stored checksum and the result must be read. Failure can be caused by:

defective Pals U23 U24
defective ROM U40
address bus shorted or open

LED 2 stays on ***O X O O***

This indicates failure of the RAM test. Several tests are performed to check RAMs U38 U39 nonvolitility (battery backup). The RAMs are tested by checking to see if a value was stored before the last time the system was powered down. A value is written and then read to verify the write. If failure occurs after the second power up:

Check RAMs U38 U39; U50 (LS03) pin 3,6,8,11;
U51 (HCT04) pin 12,10.
Check batteries voltage.
Check Duart U7 (DISRAM) pin 15 for a low; U49 (RAMBUFEN) pin 1 for a high.

5.6.2 Cartridge Diagnostics

Never insert or remove the cartridge with the power on. Power down and place the Diagnostics Cartridge in the cartridge slot of the 480L. Make sure that the cartridge's Write Protect switch is set to ON, and that there is a LARC connected to LARC Port 1. Any combination of HSP or SME boards can be tested at one time, as long as they are jumpered so as not to conflict with each other.

NOTE: SME boards must be jumpered as either Slave 0, 2 or 4. In order for the SME SLVREG test to pass, there must be at least one regular HSP board in the system. A MIDI cable must be connected from MIDI OUT to MIDI IN for the MIDI test to pass..

The following jumper positions are required:
SME:

SLAVE 0	Jumper	W1,W4,W18
SLAVE 1	Jumper	W2,W5,W20
SLAVE 2	Jumper	W3,W6,W22

All configurations must have jumpers at W12, W13, W14 and W15.

Power on the 480L and a series of messages will appear on the LARC. The Diagnostics Cartridge determines which boards are present in the system and displays that information in the area above the six sliders. The display above the sliders corresponds, from left to right, to Slave 0-5. If this infomration is incorrect, it is probabnly due to DMA failure. (Refer to the DMA Test trouble-shooting procedure for the appropriate board, desctbed below.) After the "SLAVES IDENTIFIED" message, the display will switch to "RUN TESTS BANK1 PGM 1". The "PGM 1" will be blinking, signifying that the diagnostics are in program mode.

There are four banks of test programs. Bank 1: ALL TESTS, contains two programs which run all the Host and HSP tests sequentially, either once or repeatedly. Bank 2: HOST TESTS, contains four tests which can be run separately to test the Host board. Bank 3: HSP TESTS, contains ten tests which can be run separately to test the HSP board. Bank 4: SME TESTS, contains tests to test the SME board.

Bank Mode is used for selection of tests; tests can only be run in Program Mode.

To switch from Program Mode to Bank Mode, press the BANK button once and the "BANK 1" portion of the display will start blinking. Pressing BANK repeatedly will cause the display to switch between banks. When the display shows the bank you want, press PROG to return to Program Mode, with Program 1 of whatever bank you have selected displayed in the upper display. Pressing one of the buttons numbered 1, 2, 3 or 4 will switch banks and put the system directly into Program Mode. In Program Mode, pressing PROG will switch the display to the next program. To run a test, press the button corresponding to the test you want to run. The upper display will show that program.

While a test is running, the upper display shows the name of the test; the lower display shows the number of the slave being tested. If all the slaves pass, the display will eventually show "TEST COMPLETED." If there is a failure, an error message will appear in the lower display and the upper display will read: "PRESS PAGE TO CONTINUE." Pressing PAGE will allow testing to resume with the next slave. When all the tests have been run, the "TEST COMPLETED" message will appear, regardless of how many slaves passed or failed.

The Bank 1 program: RUN TESTS is the equivalent of running all of the Bank 2 and Bank 3 tests one after another. If there is a failure, pressing PAGE will cause testing to resume and continue to the end. The Bank 4 program: SME ALL TEST works the same way on the SME tests.

The bank 1 program: RUN INFINITE is the same as RUN TESTS, except that after the second to last test it loops to the beginning and starts again. The only way to stop this test is to power down.

The first test in bank 2: RAM TEST, also runs in an infinite loop. It exercises the Host board while flashing "RUNNING RAM TEST on the LARC.

When running any of the tests in Bank 3: HSP TESTS, it is important that Program 1 of that bank (WCS TEST) be run first to initialize the Writable Control Store. Likewise, in Bank 4, the WCS test must be run before CPC, SLVREG, MEM or ADDR.

When testing has been completed, power down the 480L before removing the Diagnostics Cartridge.

The tests in the Diagnostics Cartridge were designed to be run sequentially, with each successive test checking a more remote function of the system. If a test fails, later tests which depend on the failed function may not produce valid results. Run the Bank : RUN TESTS program first. If there is a failure, begin by troubleshooting the first test to fail.

Following are detailed descriptions of the individual tests. In these test descriptions, "SLAVE 0" refers to the first slave on an HSP board. This could actually be Slave 0, 2 or 4, depending on how the board is jumpered. Likewise, "SLAVE 1" can refer to Slave 1, 3 or 5.

1. Bank 2 PGM 1 RAM Test

This test exercises the Host's address bus, data bus, and control lines. It writes to and reads from RAM, testing locations 8100H to 2000H. The data written to any location is the same as the address for that location. As long as the data read from a location is the same as that written into it, the test loops in this mode indefinitely. If there is an error, a failure message is displayed. Pressing PAGE will cause the test sequenceto resume. *This test wipes out data stored in user registers.*

2. Bank 2 PGM 2 MIDI Test

In this test DUART 1 (U7) passes data from its serial output to its serial input. If failure occurs:

Check MIDI cable.
Check U7 pin 30,31 transmit/receive.

3. Bank 2 PGM 3 DMA Test

The DMA test checks communication between the Host and the HSP boards. The test program asserts BLOCK/ on DUART 1 U7 pin 27. It then begins writing values into slave memory space and reading them back. There are two types of errors that can occur with the DMA test: Bus Error or Bad Data. A Bus Error occurs if the 68008 does not receive a low on DMADTACK/ after addressing slave address space. This produces the error message "SLAVE X NOT RESPONDING." Since all subsequent tests involve writing to slave memory, a failure in this mode will produce similar results in all later tests. A Bad Data error occurs if the 68008 receives a DMADTACK and writes and reads slave memory, but does not read back correct data. This produces the error message "DMA TEST - SLAVE X FAIL."

Bus Error: The 68008 writes the appropriate address of SLAVE0 or SLAVE1 to U48. This is decoded by U33 (HCT138) and passed into U37 (HCT244). The output of U37 is low either at pin 3 (DMAREQ0/) or pin 12 (DMAREQ1/) depending on which slave is being tested. If failure occurs on SLAVE0:

Check BLOCK/ on U15 pin 9 (HCT174); it should be high.

If these lines are good, check that the outputs of U48 are pin 2,5,10,15 low, pin 7,12 high.

Check that pin 3 on U37 (HCT244) is low.

If these conditions are correct, check U36 (HCT245).

U33 can be dynamically checked by powering the unit off and then on.

When the DMA test is run, strobing should be seen on pin 9 of U36 and data should change on the outputs.

For SLAVE1 failure:

U48 has pin 10 low, pin 12,15 high, U33 pin 12 low and U37 pin 12 low.

Only one output of U37 should be low at a given time.

If everything appears to have the correct levels, check DMAACK/ at pin 12 on U54 (HCT02); it should be low.

Also try powering unit off and then on and see if U17 pin 11 (HCT175) produces DMADTACK/ during this test.

If the Host board is sending a DMAREQ/ to the HSP board but receives no DMAACK/ back, follow the signal path through the HSP board. When a DMAREQ/ is received by the HSP board W2 & W3 route it to U29 (HCT244). These signals are fed to the BUSREQ/ pins on Z80s U4 or U31 (pin 25). The Z80 is then required to acknowledge the request by pulling BUSACK/ pin 23 low. This signal is wired or'd to produce DMAACK/. If failure occurs:

Check that BUSREQ/ on the failed processor is low.

Check that U29 (HCT244) pin 16 or 14 is low.

Check that jumpers W2 and W3 are in place. If all of the above are correct check:

ZCLK at pin 6 of Z80s
WC/ at pin 8 U101 (F32)
RESET/ is high on pin 26 of U4 or U31 and U30 (HCT175) pin 7 or pin 15
Check SR/ pin 1 U30 (HCT175) is high
Check that INT/ is high at pin 16 of the Z80s and at U30 pin 2,10

Bad Data: If the Host is able to write and read slave memory space but reads back bad data, check the integrity of the data path.

For SLAVE0:

U1,U2 (HCT244), U3 (HCT245) for enables at pins 1,19.
U41 (HCT244) pin 18,16 (MREQ/, WR/).
U6 (HCT139)
U5 (4364)

For SLAVE1:

U16,U17 (HCT244), U18 (HCT245) for enables at pins 1,19.
U41 (HCT244) pins 7,9 (WR/, MREQ/).
U33 (HCT139)
U32 (4364)

4. Bank 2 PGM 4 Interrupt Test

In the Interrupt Test the Host downloads a program to the slave. This is done by first releasing reset then requesting the slave BUSREQ/ by DMAREQ/. Once the bus is obtained the program is written into the slave RAM. The slave is then reset then released from reset. The slave now runs the downloaded program. The program requires the slave to interrupt the Host 1000 times. When the slave has asserted 1000 interrupts, it clears a designated memory location to let the Host know it has finished. The Host monitors this location and upon finding it cleared checks to see how many interrupts it received. An error occurs if either too much time passes before the memory location is cleared, or if it is cleared but the Host finds that there were and incorrect number of interrupts. If a failure occurs check the path of the interrupt signals.

HSP Board:

Check U6 or U33 (HCT139) pin 10 (SLVINT1/ or SLVINT2/)
Check U52 (HCT03) pin 8

Host Board:

Check U22 (HCT244) pin 3 (SLAVEINTB/)
Check U8 (HCT74) pin 9 and U19 (HCT148) pins 6,7

5. Bank 3 PGM 1 WCS Test

In the Writable Control Store Test, the Host downloads a program telling SLAVE0 or SLAVE1 to write values from 0-255 to each bank of the WCS and read them back. When the slave finishes this and the correct values have been read then the slave writes to a known memory location which the Host reads to verify results.

If the test fails, the slave is left doing reads and writes to the failed address. Once the error message is received, look at the hardware surrounding the WCS. Sync the scope on the enable pins of the HCT244's or the enable pin of the HCT374's to verify that the data written to the 2018 RAMs is the same as that being read. The slave which has failed will loop in this mode until PAGE is pressed.

For SLAVE0 failure:

A1/ on U21 & U8 pin 2 (F32)
U10, U11, U12 (F157)
RD/ & WR/ strobes at U21 & U8
U22 & U24 (HCT374) for reads
U23 & U25 (HCT244) for writes
Check U13 & U14

For SLAVE1 failure:

A2/ on U45,U35 (F32)
U37, U38, U39 (F157)
RD/ & WR/ strobes at U35 & U45
U46 & U48 (HCT374) for reads
U47 & U49 (HCT244) for writes
Check U26 & U27

6. Bank 3 PGM 2 Zero Delay

Once the operation of the WCS has been verified, the first microprogram loaded is a zero delay program with no attenuation, i.e. a multiply by 1. The purpose of the test is to verify the operation of the WET, ADDRESS, DATA, and CONTROL busses. A microprogram is downloaded to the microstore (WCS). This program reads from the Host XFEROUT registers U62, U76, and U90 and writes back to the Host XFERIN registers U61, U75, and U89. The Host writes the value AA AA 40 to the XFEROUT registers. This value is read by the microprogram and written back unchanged to the XFERIN registers. If the Host reads the correct value then it writes 55 55 80. If there is a failure the LARC will display which byte of the value written was bad, and which slave caused the failure. In this, and all subsequent tests through the Allpass Filter test, a failure by one slave will cause the same microprogram to be loaded into the other slave's microstore, so that side-by-side comparisons may be made. Both microprograms will continue to run until PAGE is pressed.

On the Host board, for testing the transfer registers on the Host sync a scope on pin 1 of U62 (low byte), U76 (mid byte), or U90 (high byte). This signal will allow reading of the value which has been written to the registers.

If there is no signal, check U98 (HCT138) pin 7 and IORD/ at U101 pin 9.

If the data is found to be bad at the outputs of these registers, check U92 (HCT138).

If the data is correct, sync the scope on pin 11 of U61 (low byte), U75 (mid byte), or U89 (high byte). This is the output strobe generated by the microcode. The data sent by the HSP can be seen at the inputs to these registers.

If no strobe is found check pin 9 on U98 (HCT138) and check that IOWR/ is low at U101 pin 10.

If a byte is found bad, but all of the above signals are correct, the problem resides in the HSP.

On the HSP board the micropipeline is used minimally. Neither the MMU nor the dynamic RAM is used. The Zero Delay test exercises the WETBUS addresses and control, and several bits of control for the ARU. WETBUS addresses used are 1FH for reading the XREG and 1EH for writing the XREG. These addresses can be validated in the pipeline at U106 outputs for SLAVE 0 (sync on pin 1) and at U107 outputs for SLAVE 1.

On U109 check for strobing on pins 11,15 for SLAVE 0 and pins 3,7 for SLAVE 1. These strobes should occur once every sample.

On the input of data SLAVE 0 uses U72, U74 and 1/2 of U57. Check U72 (high byte) and U74 (mid byte) for AAH or 55H at the inputs.

Check U57 (low byte) for 40H or 80H at the inputs. The corresponding buffers of SLAVE1 are U85, U87 and 1/2 of U56. By syncing on pin 1 of these buffers a scope can be used to see the data at their outputs.

If this sync pulse is not found, check the IORD/ lines at U109.

If data is valid at the input buffers to the DAB, check pin 29 (XCLK/) of the ARU (U60 for SLAVE 0; U89 for SLAVE 1). This strobe should occur once a sample cycle.

XCLK/ clocks data from the AU of the ARU to the output register of the ARU. Data is now passed to the output registers (U73, U75 and U58 for SLAVE 0; U86, U88 and U59 for SLAVE 1). The data is first written to the registers, and then passed to the WETBUS on the following cycle.

The writing of the data can be validated by syncing on pin 11 of these registers and checking the data inputs. The passing of the data to the WETBUS can be validated by syncing on pin 1 of U73, U75 or pin 19 of U57 (SLAVE 0); pin 1 of U86, U88 or pin 19 of U56 (SLAVE 1).

If no strobing is found on these pins, check U108, U110 and U101 (SLAVE0); U42, U110 and U101 (SLAVE1).

If this test passes, a large portion of the HSP data paths has been validated.

7. Bank 3 PGM 3 Double Precision Multiply Test (xAA)

This test is used to verify operation of the multiply circuitry around and in the ARU. Double precision insinuates an eight bit multiply. The eight bit multiply occurs every two micro-instructions. The first coefficient used is AAH.

If SLAVE 0 fails:

Sync on DP1/ (pin 9, U63). This bit should be low for an instruction cycle once a sample period.

If this is correct, check the outputs of U70. The value AAH should be seen.

If the value is correct, sync on CLKEN/ at pin 1 of U116. When CLKEN/ is low and A1/ goes high, the outputs of U79 pins 2, 5, 6, 9 and 12 should be 0AH respectively. These bits should also appear at the outputs of U78 on the rising edge of B/.

During the second half of the multiply (CLKEN/ is now high as well as DP1/), the value at the outputs of U78 should be 05H for C1<0:4>. This value can be seen by syncing on DPDX1/ (pin 19 of U78), which will be low.

Refer to Figure 5.1 for the output of U76 and U61 for proper signals to the ARU. If all signals appear correct, the ARU may be at fault.

For SLAVE1 failure:

Check U92 pin 9 for DP2/.

Check the output of U99 for AAH.
Check the input of U116 pin 4 for CLKEN/.

Check the outputs of U114 and U115 as described above and, finally, the outputs of U113. The outputs of U111 and U90 should follow Figure 5.1.

8. Bank 3 PGM 4 Double Precision Multiply Test (x55)

This test is the same as the test above except that the coefficient used is 55H. The value of C<0:4> should be 15H during the first half of the multiply and 02H during the second half. Figure 5.2 shows the outputs of U76 and U61 (SLAVE 0) or U111 and U90 (SLAVE 1).

9. Bank 3 PGM 5 MMU Test

This test checks the operation of the Memory Management Unit. The Host passes the value AAAA40H to a microcode program which writes that value into audio memory. The MMU continuously increments the address, so that eventually all of memory is written with that value. Then the value 555580H is passed to the microcode program and the MMU is given time to move a few memory locations ahead. A value is read. If the value read equals 555580H, it is assumed that the memory addresses are not being incremented by the MMU and that the MMU is faulty. Check U69 for SLAVE 0 and U98 for SLAVE 1. The test is also performed writing 555580H first and then AAAA40H.

10. Bank 3 PGM 6 Full Delay AA x 1/2

During this test all locations in memory are written and read. Check the outputs of U50 (SLAVE 0) or U55 (SLAVE 1) to verify that RAS/ and CAS/ are cycling. If these outputs are not correct:

Check that Delay U40 is functioning. Pin 12 should be delayed 30ns from the input on pin 1. Pin 10 should be delayed 90ns from the input on pin 1. The RAS/ output strobes every cycle, but CAS/ only strobes when a memory operation occurs.

By syncing on pin 13 of U50 or U55 one can observe all strobes for a memory operation. MCEN indicates that a memory read or write is taking place. Verify that MWR/ is low during write operations (U82, pin 11 for SLAVE0; U117, pin 11 for SLAVE1).

Check that all signals reach the five dynamic RAM chips (U64-U68 for SLAVE0, U93-U97 for SLAVE1).

If a slave fails this test, the RAM at fault will be displayed by its reference designator. This Full Delay multiply uses data AAAA40H for the multiply.

If all signals look correct and a failure is indicated, the ARU is suspect (U60 for SLAVE 0, U89 for SLAVE 1).

11. Bank 3 PGM 7 Full Delay 55 x 1/2

This test is the same as above except that the data used is 555580H.

12. Bank 3 PGM 8 All pass Filter

The Allpass Filter is a common filter used in audio effects. This test utilizes short (7 bit coefficient) multiplies to check the operation of this filter.

If SLAVE 0 fails:

Check for SHORT1/ low once a sample period (U63 pin15 and U62 pin 17).

If this appears to be correct, ARU (U60) failure is likely. The test is performed first with data A5A540H and then with data 5A5A80H.

For SLAVE 1 failure:

Check SHORT2/ at U92 pin 15 and U91pin 17. If this is correct, the ARU U89 is suspect. The same data patterns are used.

13. Bank 3 PGM 9 Peak Detector Test

This test is used to verify the operation of the headroom mechanism for the LARC. The peak detector detects positive peaks only and compares only the most significant byte of audio data. This test first clears the peak detector peak registers U63 and U65 on the Host board. The transfer register (U89 on the Host) is then loaded with data 01H. The left channel is tested first. The value 01H is compared to 00H in the peak register U63. After a brief wait the Host reads the left channel peak register U64. If the value 01H is read then the next value 02H is loaded and the process continues. Values from 01H to 7FH are tested. The right channel is then tested and U66 is read to obtain the peak value. If the test fails:

Check to be sure that DAPRIML/ is strobing at U103 pin 3 and that DAPRIMR/ is strobing at U103 pin 6.

Check that PEAKSEL/ at U103 pin 1 is high.

Check that the outputs of U103 pins 4 and 7 reflect the inputs.

If these signals are not present, check the outputs of U98 pin 15 (DAPRIML/) or pin 14 (DAPRIMR/).

Check that the address to U98 is 18H for DAPRIML/ and 19H for DAPRIMR/. Sync on the IOWR/ signal (U101 pin 10).

If these signals are not present, check on the HSP board the outputs of U106.

If these signals are correct, check the levels at the inputs and outputs of U53 and U112 on the Host board.

Also check to see that pin 5 on U77 or U79 is strobing occasionally.

Also check for the RDPEAKL/ strobe (U63 and U64, pin 1) and the RDPEAKR/ strobe (U65 and U66, pin1).

14. Bank 3 PGM 10 Two In Four Out

This is used for testing the audio quality of the system. The two inputs on the rear of the machine are routed to the four outputs. The left input is sent to the left and right secondary outputs, and the right input is sent to the left and right primary outputs. Both outputs represent the unattenuated inputs.

15. Bank 4 PGM 2 SME DMA Test

The DMA test checks communication between the Host and the SME boards. The Host writes values into slave memory space and reads them back. There are two types of errors that can occur: Bus Error which produces the message: "SLAVE X NOT RESPONDING" and Bad Data which produces the message: "SME DMA TEST - SLAVE X FAIL." Since all subsequent tests involve writing to slave memory, a failure in this mode renders all the other SME tests invalid.

If the HSP DMA test passes but the SME DMA test fails, the problem is probably in the SME board, not the Host.

Bus Error: If the Host board is sending a DMAREQ/ to the SME board but receives no DMAACK/ back, follow the signal path through the SME board. When a DMAREQ/ is received by the SME board it is routed by W4, W5, or W6 to U101 (HCT244). From U101 DMAREQA/ goes to PAL U102 which pulls low the BUSREQ/ pin on the Z80 U66 (pin 25). The Z80 is then required to acknowledge the request by pulling BUSACK/ pin 23 low. This signal passes through PAL U102 causing HBUSACK/ (pin 14) to go low. HBUSACK/ low enables buffers U25, U65, U87 and the top half of buffer U101, allowing the Host access to the

slave's memory space. Also, the enabling of buffer U101 causes the DMAACK/ signal to go low, acknowledging the Host's DMA request. If failure occurs:

Check that BUSREQ/ on the failed processor is low (U66 pin 25).

Check that U101 (HCT244) pin 7 and pin 14 are low.

Check that the correct jumper W4, W5, or W6 is in place.

If all of the above are correct check:

ZCLK at pin 6 of Z80
WC/ at U145 pin 3
RESET/ is high on pin 26 of Z80
Check that SR/ pin 1 U103 (HCT175) is high.
Check that INT/ is high at pin 16 of Z80

Bad Data: If the Host is able to write and read slave memory space but reads back bad data, check the integrity of the data path.

U25,U65 (HCT244), U87 (HCT245) for enables at pins 1,19.
U101 (HCT244) pin 18,16 (MREQ/, WR/).
U26 (43256)

16. Bank 4 PGM 3 SME Interrupt Test

In the Interrupt Test the Host downloads a program to the SME. The program requires the slave to interrupt the Host 1000 times. When the slave has asserted 1000 interrupts, it clears a designated memory location to let the Host know it has finished. The Host monitors this location and upon finding it cleared checks to see how many interrupts it received. An error occurs if either too much time passes before the memory location is cleared, or if it is cleared but the Host finds that there were an incorrect number of interrupts. If a failure occurs check the path of the interrupt signals.

SME Board:

Check U87,U101,U103,U136,U124

Host Board:

Check U22 (HCT244) pin 3 (SLAVEINTB/).
Check U8 (HCT74) pin 9 and U19 (HCT148) pins 6,7.

17. Bank 4 PGM 4 SME WC Count Test

In the Word Clock Counter Test the Host downloads a program in which the slave tells the word clock counter to interrupt it after a specified number of word clocks. There are two possible types of failure, Timeout Error and Count Error. A Timeout Error occurs when the slave does not receive the expected interrupt within a certain time limit. Bad Count means that an interrupt was received, but not at the correct time. If there is a failure:

Check the word clock counter (U1, U2, U3) on the SME board. At the start of the test a value should be clocked into the counter registers (check WCCLKL/, WCCLKM/ , WCCLKH/ at pin 13 of U1, U2, U3) and this value should be loaded into the counters by CLOAD/ (pin 14).

Check for a valid WC/ at U3, pin 11. U3, U2, and U1 form a ripple counter. The final output (WCINT/, U1 pin 9) clocks U136 pin 3, causing WCINT to be asserted. This signal passes through inverter U124 and pulls the INT/ line low, which causes the slave to be interrupted (U66 pin 16).

Check to make sure that none of the other interrupt lines are high (HSTINT U136 pin 9, DSKINT U142 pin 5, DMAINT U142 pin 9).

Check the operation of U106 (used to poll the interrupting devices) and U91 (used to clear the int flip-flops U136 or U142 once an interrupt has been serviced).

18. Bank 4 PGM 5 SME WCS Test

In the Writable Control Store Test the Host downloads a program telling the slave to write values from 0-255 to each bank of the WCS and read them back. When the slave finishes this and the correct values have been read, the slave writes to a known memory location, which the Host reads to verify results. If the test fails, the slave is left doing reads and writes to the failed address. Once the error message is received, look at the hardware surrounding the WCS. Sync the scope on the enable pins of the HCT244's or the enable pin of the HCT373's to verify that the data written to the 2018 RAMs is the same as that being read. If there is failure the slave will loop in this mode until PAGE is pressed.

SME board:

A/ on U146 & U132 (F32)
U148, U162, U172 (F157)
RD/ & WR/ strobes at U146 & U132
U159 & U169 (HCT373) for reads.
U160 & U170 (HCT244) for writes.
Check U149 & U173.

19. Bank 4 PGM 6 SME Host Interrupt Test

The Host Interrupt Test tests the Host's ability to interrupt the slave. The Host downloads a program to the slave telling it to set a known memory location to an error code. The slave then waits to be interrupted by the Host. When the interrupt occurs, the slave clears the memory location which is then read by the Host.

If there is a failure, run the test again, checking that the Host interrupt disable line (CLRHST/ U136 pin 13) goes high during the test. (There is about a 1 second delay between when the button is pressed and when the test actually runs.)

If this signal is correct, check the path of the interrupt line from the host to the slave.

Host board:

U92,U36,U54

SME board:

Check for HSTINT/ signal going low, U103 pin 2.

Check for HSTINT signal going high, U136 pin 9.

Check that the other int signals are low (WCINT, DSKINT, and DMAINT).

Check for INT/ going low at U66 pin 16.

Check for a single strobe on RDSTAT/ (U106 pin 19) and data 01H on the slave data bus during this strobe (device polling).

Check that the HSTINT flag is cleared by WRSTAT/ strobing U91 pin 11.

20. Bank 4 PGM 7 SME CPC Test

The Current Position Counter Test is the first of the SME tests to use microcode. The Host first loads a microcode program into slave memory. It then loads a slave program and releases the slave. The slave loads the microprogram, which clocks the CPC 16 times per sample, into the WCS. It then clears the CPC and waits for a specified period of time. At the end of this time it reads the CPC. If the CPC does not contain the proper value, an error message is displayed and the DSP continues clocking the CPC 16 times per sample (until PAGE is pressed).

SME board:

Check U109, U110, U111 for CPCLK/ (pin 13) and its inverted version (through inverter U133 to pin 11).

Check for incrementing binary count at outputs of U109, U110, U111.

Check for single low strobe on CPCC/ at start of test (U109, U110, U111 pin 10).

Check for single low strobe on CPSTOR/ at end of test (U180 pin 1), and subsequent rising edge on U93, U94, U95 pin 11. These signals clock the current address from CP bus into latches.

Check for single strobes on read lines at end of test (CPCHI/ U95 pin 1, CPCMID/ U94 pin 1, CPCLOW/ U93 pin 1).

21. Bank 4 PGM 8 SME SLVREG Test

The Slave Register Test tests the operation of the transfer registers, wet bus, and slave registers. The Host first loads a microcode program into slave memory. It then loads a slave program and releases the slave. The slave loads the microprogram into the WCS. The microcode causes the DSP to perform two alternating functions. It reads the Host transfer registers, writing the value to the slave registers. It also reads the slave registers, writing the value to the Host transfer registers. The slave, meanwhile, reads the slave registers and writes the value to a set of known memory locations, and also reads another set of known memory locations and writes the value to the slave registers. In this mode the slave and DSP are able to pass data in two directions. The Host first writes AAH to the transfer registers, waits a short time, then reads slave memory to determine if the value was transferred

correctly (the bottom 6 bits must be masked off). The Host then writes AAH to slave memory, waits a short time, and reads the transfer registers. If these are correct, it repeats the procedure with the value 55H. In case of failure the slave and DSP continue passing data. Follow the data path through the SME board in each direction.

SME Board:

Check slave registers U90, U96, U100 to see if slave is writing data (strobing on pin 1) and reading data (strobing on pin 3).

Check data at slave registers inputs/outputs for 55H or AAH pattern.

Check transfer registers U119, U131, U144 for data input from Host (strobing on pins 1 and 11, 55H or AAH pattern at outputs).

If no strobing is seen on pins 1 and 11, check U137 and Pal U125.

Check transfer registers U120, U135, U143 for data output to Host (strobing on pins 1 and 11, 55H or AAH pattern at outputs).

If no strobing is seen on pins 1 and 11, check for RDWETA/ signal (U168, U147, U163), IOEN/ (U91, U133), and WETWR/ (U180).

22. Bank 4 PGM 9 SME Memory Test

The SME Memory Test tests the 1 meg of audio memory on the SME board. The Host loads a microcode program into slave memory, then loads a slave program and releases the slave. The slave loads the microprogram into the WCS. The microcode causes the DSP to read the slave registers U90, U96 and U100, writing the value into audio memory. The DSP then reads the audio memory location that it just wrote to, writes the value back to the slave registers, and clocks the current position counter to the next location. It goes through this procedure once per sample cycle. At the beginning of the test the slave writes 55H to the slave register and clears the CPC. It then checks the slave register once per sample to make sure that the correct value has been written to it by the DSP. When the entire audio memory has been tested in this way (about 22 seconds), the slave repeats the test with the value AAH. If there is an error, the LARC will display the memory bank and the highest incorrect data bit. Since data is stored one bit per chip, the bad data bit may correspond to a bad memory chip. Also:

Check for strobing on memory control lines RAS/ and CAS/, and on the write enable control (pin 3) of the memory chips. -

f no strobing is seen, check U4, U5, U121, U147 and U178.

A "BAD ERROR CODE" message probably means the Host was interrupted too soon. Check U104, U179, U167. The SINT/ and SLVINT/ signals should strobe low once halfway through the test, and once at the end.

23. Bank 4 PGM 10 SME Address Test

The SME Address Test also tests the SME audio memory. It is different from the Mem Test in that there are two different microprograms used. During the first half of the test, the DSP reads the slave registers, writes the value into audio memory, and clocks the current position counter to the next location. The slave synchronously increments the value in the slave registers so that the value written into each location is the address of that location. During the second half of the test, the DSP reads the audio memory, writes the value to the slave registers, and clocks the CPC to the next location. The slave reads the slave registers once per cycle, expecting to find the value incrementing by one each time. If there is an error, the LARC will display the memory bank and the highest incorrect data bit. Since the data is also supposed to be the address, the bad data bit might correspond to a bad address bit. Check the address lines:

The OFSA bus <0:19> (U127-9, U139 and U140) is the sum of the Current Position Counter outputs (U109, U110 and U11) and the OFSTB/ <0:19> outputs (U152-4).

The OFSTB/ outputs (U152-4) should all be zero during the test.

The Current Position Counter outputs (U109, U110, U11) should be incrementing in a binary count, as should the OFSA outputs (U127-9, U139, U140). Check for shorts in any of these lines.

The 18 OFSA signals are multiplexed into the 9 MAB signals by U108, U126 and U138. OFSA <2:10> become MAB <0:8> during the RAS/ part of the address cycle, and OFSA <11:19> become MAB

<0:8> during CAS/. Check for proper strobing of the SEL signal (pin 1 of U108, U126 and U138) which controls this multiplexing.

Check for shorts in the MAB, MA, and BMA address buses.

Check Pal U178 for RAS/ and CAS/ generation.

A "BAD ERROR CODE" message probably means the Host was interrupted too soon. Check U104, U179, U167. The SINT/ and SLVINT/ signals should strobe low once halfway through the test, and once at the end.

If the Mem Test indicates failure after an Address Test failure has been solved, it is probably because the memory had not previously been fully accessed by the Mem Test. This is one of many possible situations where solving a problem found by one test can uncover another problem. In this case, however, the new problem would be found by a previous test.

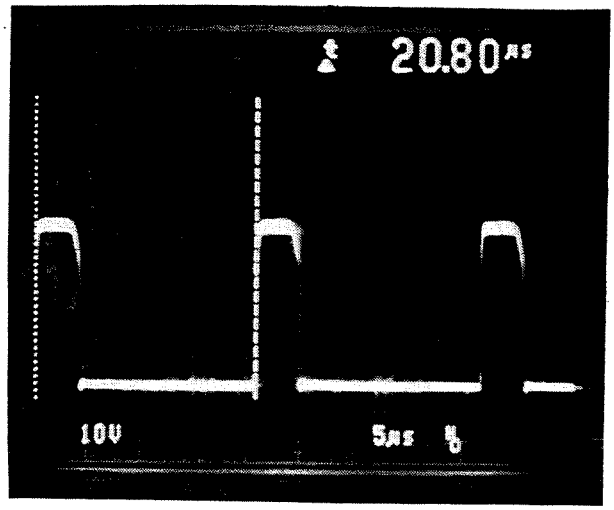

Figure 5.3. Switching Signal on Q1 of Power Supply.

5.7. Problems and Possible Solutions

Unit dead—no power at all.

Check power cord continuity. Check power module fuse and voltage select switch connections. Verify that VR1 and VR2 are not shorted (Varistors located by power module). Check for any pinched wires. Check transformer continuity.

No +5 VDC switching power supply.

Verify that F1 on power supply module is good (6.3 A slo-blo). Disconnect P4 from power supply module to determine if problem is a short in the system or a weak or defective power supply. Verify 21 VAC from E2 E3 on power supply module. Check to see if oscillator is running, probe C9 5100pf.

Check for about 28 vdc at pin 17 of U1 on power supply module. Check for large switching signal on FET Q1. See Figure 5.3. Read circuit description for the power supply (Section 4.6), then continue.

No ±15 VDC power supplies.

Verify F1 and F2 on motherboard (1.25 A slo-blo). Power off unit and check for shorts.

480L won't pass audio, or has distorted audio.

Check all audio cables for continuity, tight connection, shorts and intermittents.

Verify that there is not some other equipment causing problem by disconnecting 480L input and output cables and connecting them together (bypass 480L).

Check to see if 480L will pass audio in IN_OUT test. If it is still distorted try passing audio in self test, jumpers on motherboard move W1 & 2 to 2-3 (self test). If it still has distorted audio then problem is likely on motherboard. If audio is clean problem is likely on one of the plug in boards.

The LARC control head will not light.

Verify +20 vdc at TP1 on motherboard and pin 5 of either LARC port on rear panel. If +20 volts is getting to the LARC controller then proceed to troubleshoot LARC controller. (The LARC only needs power to operate.)

Touching a slider on LARC resets unit.

Check U11 on LARC, Signetics 4515's have proven to be unreliable. Replace with RCA or other brand.

The LARC display is frozen, can't change parameters.

Try the other LARC port on rear of 480L. If this cures problem, suspect board is Host. If LARC 1 port is problem U2 (9638), U4 (9637) and U7 (68681) are suspect. If LARC 2 port U2, U4 and U6 are suspect. If the other LARC port still produces problem,verify that there is power to LARC controller at the end of the cable. If power is present then proceed to troubleshoot LARC control head. Run all LARC diagnostics.

There is no audio from unit with proper input.

Verify that the level controls are adjusted properly. Try powering off unit and reloading program.

If this corrects the problem there may by a problem in the system which caused the system to crash. Suspect Host. Verify that the batteries produce at least 2.50 VDC, check seating of all processor circuits, check sockets for damage and possible broken pins (this can be determined by heating pins with soldering iron on solder side and verifying that pins are not loose when solder is molten, verify 68681 (DUART) is not receiving false input information due to noise on 9637 serial receivers, verify good clean power +5 VDC, verify proper power reset U45, U47, U52 on the Host board.

Try running the 480L IN_OUT program. If it passes audio in IN_OUT, run diagnostics to determine whether the problem is on the Host or an HSP. (Refer to section on diagnostics.)

Try changing the sample rate to the other frequency (44.1kHz or 48kHz).If this cures the problem, the Host board is suspect. Check the host board clock selection circuit (U105, Q1, U94, U93, U7)

Try running the 480L in single configuration. This will help determine if it is a multiprocessor problem.
If running the 480L in single configuration cures the problem try using the unit with only one HSP board at a time. Unplug the HSP2 and try to pass audio in single configuration. If it passes audio, the HSP2 is suspect. Try removing HSP1 and jumper suspect HSP2 as a HSP1 and try to pass audio.

Strapping the HSP 2 as a HSP 1 can help determine which HSP is bad. Once you determine a board is bad, run diagnostics tests for HSP to debug to component level. (diagnostics test only configuration HSP 1).

When the problem is in only some programs.

Identify programs and check current manual to determine if the problem you found is normal operation or a possible software bug.

Run the problem program in single configuration. If problem does not occur in single configuration then suspect HSP board. Strapping the HSP 2 as a HSP 1 can help determine which HSP is bad. If one of the HSP boards is bad, use diagnostics and signatures to determine component defect. If you use signatures to determine fault be sure to use signatures that are going to produce problem ie. if unit sounds good in IN_OUT program do not use those signatures. There are signatures for IN_OUT and Reverb (see signature tables in Chapter 6).

If problem is lack of output in all programs.

Place unit in Self Test via jumpers on motherboard. This will allow audio to pass through the unit without processing it. It will determine if the analog section and converters are operating. If the unit will still not pass audio in self test then verify BCLK, BLC/, CLR are being received on the motherboard, check power supplies +/ -15, +5 d/a, +5 dig, follow input signal through and use standard troubleshooting procedures. If the unit passes audio in Self Test but not in Run Mode problem is in boards (Host, HSP's). Run diagnostics to determine what board level problem is at then use signatures and other troubleshooting aids to determine fault.

If unit passes audio in Self Test and passes diagnostics but will not pass audio in run mode. Verify that ADD/ is being passed through opto device U12 HCPL2630 on motherboard and to Host board U97 74HCT244 where it's buffered and ADDB is converted to parallel WETDB data bus for processing. Verify that DADLB and DADRB are being received back on motherboard through opto U3.

Input CMRR problem.

Careful matching of C144 & C145 (right) and C184 & C185 (left) 100pf capacitors on motherboard is a good place to check if out of specification. These capacitors require a 2.5% tolerance.

Mute function does not work.

Verify that when you press mute button on LARC the display reads "AUDIO MUTED". If not, proceed to LARC button test. Press PAGE, hold then PROG then PAGE switch until button test is displayed. Then press PROG to execute test. Proceed to debug LARC controller. If display operates but mute still will not operate check on Host board for force mute signal to go to logic high when pressing mute. If not suspect U7 (68681 DUART) on HOST. Next check on motherboard for presence of BMUTE (right side of R239 220ohm) which will be -15vdc and be +5vdc when mute switch is pressed.

Note: Q6-9 are the muting fets which terminate input to final amplifier stage. Lexicon has used both J105 and J108 parts at this location. The J105's have lower on resistance of about 3 ohms with the J108's having about 8 ohms.

LARC will not control 224XL through 480L.

First verify a LARC will control both 224XL and 480L by itself. Then verify RS422 cable between 480L and 224XL is good by measuring continuity of it out with an ohmmeter (shorts and opens).

Note: The 224XL has full diagnostics which take about 15 seconds. If the 224XL does not respond after power up be sure to give it time to complete diagnostics.

480L LARC control seems slow, locks up or passes distorted audio when boards are placed on extender card.

Possible problem on Host. An etch cut is required on U104 pin 11 (rev.1 boards only). If this does not correct problem try using right angle Eurodin connectors soldered to create an extender which keeps the board close to the backplane and the board comes out of the bottom of the unit.

Host Trouble

If system fails to come up properly open front panel and check Host leds. They should all be off for normal operation. As of V1.23 there are limited diagnostics resident in rom which perform rom, ram and operating system test each time you power up. Error codes are shown in Table 5.2.

Note: The errors are only displayed for two seconds, so power on and observe LEDs until system is operational.

U40 000X	hex 1
U41 00X0	hex 2
U42 00XX	hex 3
U43 0X00	hex 4
U39 0X0X	hex 5
U38 0XX0	hex 6
System failure	0XXX hex 7

Table 5.2. Error Codes (0=OFF X=ON).

If unit is failing but there are no diagnostic failure leds, try the ram cart diagnostics. Check the hardware that drives the leds (U11 Host) with a scope.

Host failures: Once you have determined you have a bad Host board via swapping with a known good unit or by diagnostics. Use the diagnostic guide to direct you to location suspect. Then use signatures to assist to component level.

It is good practice to check clocks for good logic level waveforms @ TP3 & 4 on Host.

Master clock MC TP4 3
MIDI clock U16/11 Host
Word Clock WC/ TP4 4
Bit clock BC/ TP4 2
8MCLK TP3 2
3.6864 MHz TP3 1

Verify that host power up reset to 68008 and CLK are correct.

Read Chapter 4, *Circuit Description,* and also the information in the Motorola data book on 68008 to help with complex problems. Always check jumpers. Always replace any logic gates with equivalent part. Do not substitute any other family type. The product has particular parts in locations for design reasons. If you replace a part try to use the same manufacturer if possible and always use same family; i.e., F, LS, HC, HCT, ALS, AHCT, etc.

HSP failures: Once you have determined you have a bad HSP board via swapping with a known good unit or by diagnostics. Use the diagnostic guide to direct you to location suspect. Then use signatures to assist to component level. It is good practice to check clocks for good logic level waveforms. Read theory of operation

on HSP to assist with complex problems. Always replace any logic gates with equivalent parts. Do not substitute any other family type. The product has particular parts in locations for design reasons. If you replace a part try to use the same manufacturer if possible and always use the same family (F, LS, HC, HCT, ALS, AHCT etc.).

5.8 General

Suggestions prior to returning unit to operating location after repair.

1. If any components were replaced in a unit, the unit should be powered on and operated overnight prior to returning to location for user.

2. Check all boards for proper seating with card retainer.

3. Check unit for completeness, burnt parts, cosmetics.

4. Test all operating funtions.

5.8.1 Misc. Notes

Polypropylene capacitors at the input must be accurate for good CMRR. 1610 interface can cause problems if improper cable is used (use twisted pair cable). Some early units had the foldback set at 10 amps (now all 8.5 A).

First rev 2 HSP is 2-1241 "A" in mainframe 480-1119. First rev 2 Motherboard "B" is in mainframe 480-1119. "Ulveco" power transformers had colored shrink tube changes on wires. (effective s/n 1000-1149)

Version 1.20 was sent out for beta test only (it is not released). It will cause unpredictable problems, and should be replaced with V1.23. Version 1.23 was released effective s/n 1196 and shipped to dealers at no charge.

Do not mix IC families from what is on parts list unless it applies to an ECO (i.e., HCT, AHCT, HC, LS, F, ALS).

5.9. Letter Codes

5.9.1 Motherboard

Rev. 1 p.c. board

Rev. "A" #860902-00 Change R239 220 ohm 202-00518. (Speed up mute) Effective s/n 1091.

Rev. "B" Introduce Rev. 2 p.c. board.

Rev. "C" #861015-00 Add C229-236 33pf 245-03868. (Improve high level output performance.)Effective s/n 1149.

Rev. "D" #870317-00 Delete C64, C69, C74, C79, remove pins 5 & 12 on U36, U38, U40, U42. (improve high frequency T.H.D.) Effective s/n 1271.

5.9.2 Power supply

Rev. "A" #860703-00 R13 change to 150 ohm 202-00501, R6 to 6.04k 202-02655, C5 to .01uf 245-03610. (Quiet power supply.) Effective s/n 1022.

5.9.3 HSP

Rev. "A" Rev. 2 HSP, s/n 870317-01 Delete R4, R5 (not needed.) Effective s/n 1329.

5.9.4 Host

Rev. "B" Introduce Rev. 3. Effective s/n 1388 as of 6/19/87.

6

Parts Lists

This chapter contains parts lists for the 480L, arranged as follows:

6.1 Misc. Items

CUST LITERATURE			
070-04737	1	MANUAL,OWNER'S,480L	
070-04988	1	NOTICE,SOFT RELEASE,V1.23,480L	
CABLES/CORDS			
680-00841	1	CORD,POWER,PHILLIP #13E37-1	
680-04734	1	CABLE,10',RS-422,MNFRM/MNFRM	
SUB-ASSY			
750-04718	1	CARTRIDGE,SRAM,8KX8	

6.2 Backplane

CARBON FLM RES			
202-00549	1	RES,CF,5%,1/4W,10K OHM	R1
FUSES			
440-01877	2	FUSE,5X20MM,SLO-BLO,1.25AMP	F1,2
PC EDGE CONN			
500-03620	8	CONN,EURO,C,ROW a+c,FEM	J4-7, 9-12
PC MNT CONN			
510-03551	4	CONN,D-SUB,9FC,MB,PC	J1-3,15
ELECTRONIC HDWR			
600-02227	4	FUSE CLIP,20MM,PC	F1,2
SPCR,NON-INSUL			
635-04650	8	SPCR,SWAGE,4-40X.429,1/4RD,BR	J1-3,15 MTG
635-04651	3	SPCR,SWAGE,4-40X.469,1/4RD,BR	
BULK WIRE			
670-01974	1	WIRE,JMP,22AWG,0.1",NON-INSUL	W1
CABLES/CORDS			
680-04560	1	CABLE,XITION/SCKT,26C,7.0"	P1
680-04701	1	CABLE ASSY,6C,18G,24",ST&T/HSG	E4-9
680-04702	1	CABLE ASSY,3C,22G,20",ST&T/HSG	E1-3
SLEEVING			
690-04703	1	SLEEVING,HEAT SHRINK,15",3/8ID	6 & 3 COND
690-04704	1	SLEEVING,HEAT SHRINK,4",3/8ID	6COND
PC BOARDS			
710-04364	1	PC BD,BACKPLANE,M480L	

6.3 480L Extender Board Option

PC EDGE CONN		
500-04557	2	CONN,EURO,C,ROW a+c,MALE,RA
500-04903	2	CONN,EURO,C,ROW,a+c,FEM,RA
PC MNT CONN		
510-01067	12	CONN,POST,100X025,HDR,12MCG
PC HDWR		
610-04904	2	GUIDE/EJECTOR,EXTENDER BD
BULK WIRE		
670-01689	4	WIRE,18AWG,16/30,BLK,6"
670-01689	7	WIRE,18AWG,16/30,BLK,4.5"
670-01689	5	WIRE,18AWG,16/30,BLK,3"
670-01689	2	WIRE,18AWG,16/30,BLK,2"

6.4 480L Chassis/Mechanical

ROCKER SWITCH			
454-03900	1	SW,ROCKER,1P1T,QDC,INTL LINE	CHASSIS INSERT
CONN HDWR			
527-00138	8	CONN,D-SUB,JACKSOCKET,.150"	BACKPLANE
STRAIN REL			
530-02488	3	TIE,CABLE,NYL,.14"X5 5/8"	XFORMER WIRING
530-04719	2	CLIP,WIRE HRNS,3/8"DIA,ADH BAK	
GROMMETS			
540-00874	1	GROMMET,9/16 OD,7/16 ID	PWR SW WIRING
540-03483	4	GROMMET,3/8 OD,7/32 ID,BLUE	FAN MTG
540-04648	6	BUSHING,.250ID/.312OD,BLK	INSERT, POT SHAFTS
FEET			
541-00780	4	BUMPER,FEET,3-M #SJ5023	
KNOBS/CAPS			
550-04665	1	HANDLE,EXT W/ VINYL,BLK,1.7"L	FRONT PANEL
550-04720	6	KNOB,11MM,6MM/FLAT,BLK,WHT LN	ON SHAFT EXT
ELECTRONIC HDWR			
600-04526	6	SPCR,D/D,.125/.236,7.600L,PVC	POT SHAFT EXT
600-04558	1	CABINET LATCH,DOUBLE BALL	
600-04643	1	LID SUPPORT,RH,6-9/16"	SIDE,WRAPAROUND
600-04646	10	CARD GUIDE,4.5"	
600-04647	10	CARD GUIDE,6"	
600-04657	1	BEZEL,LED LIGHT BAR,HLMP-2899	CHAS INSERT
LUGS			
620-01999	1	LUG,SOLDER,LCKNG,#6,.020THK	AC GND MTG

SPRINGS			
625-04405	1	SPRING,6TURN,.06"ID,.5LEG	CART DOOR MTG
INSUL/SPACRS			
630-04690	1	WSHR,1/4CLX2.75"OD,NEOPRENE	
630-04994	2	WSHR,SHLDR,.359SHNK,1/4CL,FBR	XFORMER MTG
SPCR,NON-INSUL			
635-00949	4	SPCR,#6CLX1/4,AL	FAN MTG
635-04406	2	SPCR,SWAGE,.143CLX.125L,.281RD	SHIELD MTG
635-04413	1	BSHG,SHDR,.15SHNK,4-40,STEEL	LID SUPPORT MTG
MACHINE SCREWS			
640-01708	2	SCRW,6-32X3/16,PNH,PH,ZN	MOTHERBOARD MTG
640-01716	2	SCRW,6-32X3/8,PNH,PH,ZN	SHIELD MTG
640-02051	3	SCRW,6-32X3/8,FH,100DEG,PH,ZN	HANDLE MTG (2), AC GND MTG (1)
640-02288	4	SCRW,6-32X1,PNH,PH,ZN	FAN MTG
640-02715	12	SCRW,4-40X1/4,FH,PH,ZN	XLR MTG
640-02749	10	SCRW,6-32X1/4,PNH,PH,SEMS,BLK	TOP & BOTTOM COVER MTG
640-02811	8	SCRW,8-32X7/16,PNH,PH,SEMS,BLK	RACK EAR MTG
640-02812	11	SCRW,4-40X3/8,PNH,PH,BLK	DIN CONN MTG (6), BACKPLANE (3) CORCOM (2)
640-03087	6	SCRW,6-32X3/8,PNH,PH,SEMS,BLK	XFORMER SUPPORT (4) HEATSINK TO CHASSIS MTG (2)
640-03713	6	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	PWR SUP BD (4), LID SUP MTG (2)
640-03957	1	SCRW,6-32X3/16,TH,PH,BLK	"L" BRACKET MTG
640-04339	1	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	LID SUPPORT MTG
640-04691	1	BOLT,CRG,1/4-20X3-1/4,SS	XFORMER HARDWARE
THRD-FORM SCRW			
641-04556	2	SCRW,TAP,F,6-32X3/8,FH,PH,ZN	LATCH AND HANDLE MTG
NUTS			
643-01728	9	NUT,6-32,KEP,ZN	KEYSTONE TO CHASSIS MTG (2) FAN MTG (4) HEATSINK TO CHASSIS MTG (2) "L" BRACKET MTG (1)
643-01729	1	NUT,6-32,HEX,SMALL,ZN	AC GND MTG
643-01732	10	NUT,4-40,KEP,ZN	DIN CONN MTG (6), CORCOM (2) CABLE MTG (2)
643-04694	2	NUT,1/4-20,HEX,ZN	XFORMER MTG
WASHERS			
644-01735	2	WSHR,FL,#6CLX3/8ODX1/32THK	LID SUPPORT MTG
644-01736	1	WSHR,FL,#4CLX.218ODX.032THK	LID SUPPORT MTG
644-02379	4	WSHR,FL,#6CLX3/8ODX.031THK,BLK	XFORMER SUPPORT
644-04414	8	WSHR,FL,#6CLX.5"ODX.062"THK	FAN MTG
644-04527	5	WSHR,LOCK,SPLIT,1/4"	XFORMER MTG
644-04695	2	WSHR,WAVE,.13OIDX.290ODX.01THK	FRONT PANEL MTG
644-04696	1	WSHR,DIMPLE,1/4CLX2.75"OD,ZN	
644-05802	1	WSHR,FL,3/8CLX1ODX.083THK	XFORMER MTG

THREADLS FASTNR			
650-02586	2	FASTNR,NYLATCH,HN5G-52-1	PCB RETAINER
650-02587	2	FASTNR,NYLATCH,HN5P-52-4-1	PCB RETAINER
650-03982	6	POPRVT,5/32X1/4,120DEG FLAT HD	CHASSIS INSERT MTG
650-04697	2	ROLL,PIN,.125ODX.625LONG	FRONT PANEL MTG
650-04896	3	POPRVT,5/32X1/8,REG PROT HD,AL	KEYSTONE MTG (2) "L" BRACKET MTG (1)
BULK WIRE			
670-04528	1	WIRE,.045"DIAX2.5",STEEL	CART DOOR MTG
CABLES/CORDS			
680-04561	1	CABLE,EDGE/SCKT,3.0"	RAM CART SOCKET
680-04698	1	CABLE ASSY,2C,22G,20",ST&T/HSG	PILOT LIGHT ASSY
CHASSIS/MECH			
700-03555	1	FAN GUARD,3.25"MNT	FAN MTG
700-04392	1	CHASSIS,WRAPAROUND,M480L	
700-04393	1	CHASSIS,INSERT,FP,M480L	
700-04395	2	COVER,TOP/BOTTOM,M480L	
700-04415	1	GUIDE,RAM CART,M480L	CHASSIS INSERT
BRACKETS			
701-00299	4	BRACKET,KEYSTONE #617	MTHBD TO CHASSIS INSERT MTG(3)
701-04396	2	BRACKET,MTG,RACK	MTHBD TO WRAPAROUND MTG(1)
701-04699	1	BRACKET,"L",3.872X1.29X.50	HEATSINK TO CHASSIS INSERT
701-04990	1	SUPPORT,BRACKET,"C",XFORMER	XFORMER SUPPORT
PANELS			
702-04394	1	PANEL,BAFFLE,FAN	CHASSIS INSERT
702-04397	1	PANEL,FRONT,5.168X16.950X.29	
702-04400	1	PANEL,OVERLAY,CHASSIS,M480L	Rear Panel overlay.
702-04402	1	PANEL,OVERLAY,SUB,M480L	
702-04404	1	PANEL,OVERLAY,PWR SW,.89X3.70	
702-04412	1	DOOR,CARTRIDGE,RAM,M480L	
702-04520	1	STRAP,RETAINER,PCB,.80X3.690	2.0"
PC BOARDS			
710-04407	1	PC BD,DIGITAL SHIELD	
PLASTICS			
720-03272	1	TAPE,FOAM,SGL-STK,1/8THX3/4W,2.9"	PCB RETAINER
720-03272	2	TAPE,FOAM,SGL-STK,1/8THX3/4W,2.25"	BPL CABLE PROT
720-03389	2	VELCRO ARROWHEAD,PRESSURE SENS,3.0"	FILTER MTG
720-03389	1	VELCRO ARROWHEAD,PRESSURE SENS,1.5"	FILTER MTG
720-03548	4	TAPE,FOAM,1/16X1/2X3.4	XFORMER SUPPORT
720-04524	1	AIR FILTER,3.376X3.400X.25,BLK, FOR FRONT PANEL	
LABEL/NAMEPLTS			
740-04732	1	LABEL,FUSE,480L FP INSERT	

6.5 Fan Assembly

FANS/MOTRS/RELY			
410-04684	1	FAN,TUBE-AX,3.25X1,14CFM,24V	
CABLE CONN			
490-04685	2	CONN,QDC,FEM,.110X.020	
CONN HDWR			
527-04689	2	CONN,QDC,FEM,HSG,.110X.020	

6.6 Power Transformer Assembly

SEMICONDUCTORS			
360-01612	2	SEMICOND,VARISTOR	AC CONN
FUSES			
440-01624	1	FUSE,3AG,SLO-BLO,3AMP,250V	CORCOM CONN
440-01876	2	FUSE,5X20MM,SLO-BLO,1.6AMP	CORCOM CONN
TRANSFORMERS			
470-04408	1	XFORMER,POWER,TOROID,200VA	SIDE, WRAPAROUND
CABLE CONN			
490-04599	1	CONN,AC,RFI,FUSE & VOLT CHNG	REAR, WRAPAROUND
490-04685	6	CONN,QDC,FEM,.110X.020	SEC 1,2
490-04886	2	CONN,QDC,FEM,.250X.032	XFORMER WIRING
CONN HDWR			
527-04689	6	CONN,QDC,FEM,HSG,.110X.020	SEC 1,2
527-04888	2	CONN,HSG,QDC,FEM,.250X.032	XFORMER WIRING
STRAIN REL			
530-02489	1	TIE,CABLE,NYL,.1"X4"	
LUGS			
620-01999	1	LUG,SOLDER,LCKNG,#6,.020THK	XFMR SHIELD LUG
BULK WIRE			
670-01844	1	WIRE,JMP,24AWG,BUSS WIRE,1/2"	CORCOM WIRING
PRE-CUT WIRE			
675-04686	1	WIRE,16G,GRN,3.5",ST&T1/4X1/2	AC GND WIRE
675-04700	2	WIRE,18G,BLK,18",QDCXST&T.3"	PWR SW WIRING
SLEEVING			
690-02061	7	SLEEVING,SHRINK,1/8",1/2"L	CORCOM WIRING
690-04529	3	SLEEVING,TEFLON,.04"ID	VAR MTG

6.7 HSP Board Rev. 2

CARBON FLM RES			
202-00542	3	RES,CF,5%,1/4W,4.7K OHM	R2,3,6
ELECTROLYT CAP			
240-02048	2	CAP,ELEC,47uF,25V,AX	C61,62
CERAMIC CAP			
245-03609	60	CAP,CER,.1uF,50V,Z5U,AX	C1-60
DIGITAL/CMOS IC			
330-03340	6	IC,DIGITAL,74F157	U10-12,37-39
330-03586	12	IC,DIGITAL,74HCT244	U1,2,16,17,29,41, U56,57,72,74,85,87
330-03715	16	IC,DIGITAL,74HCT374	U22,24,46,48,53,54,73, U75,79,80 U86,88,106,107,114,115
330-03766	2	IC,DIGITAL,MMU,64K,CMOS	U69,98
330-04041	3	IC,DIGITAL,74F10	U50,55,108
330-04042	17	IC,DIGITAL,74AHCT374	U61,63,70,71,76,78,83, U84,90,92,99,100, U104,111,113,118,119
330-04084	6	IC,DIGITAL,74HCT175	U30,58,59,82,109,117
330-04260	2	IC,DIGITAL,74HCT04	U20,51
330-04261	1	IC,DIGITAL,74HCT00	U42
330-04273	4	IC,DIGITAL,74HCT74,ZYTREX	U7,34,43,81
330-04275	2	IC,DIGITAL,74HCT139	U6,33
330-04292	6	IC,DIGITAL,74F32	U8,21,35,45,101,116
330-04293	2	IC,DIGITAL,74F74	U28,102
330-04294	1	IC,DIGITAL,74HCT138	U105
330-04362	2	IC,DIGITAL,ARU,18 BIT,CMOS,15M	U60,89
330-04511	4	IC,DIGITAL,74AHCT244	U23,25,47,49
330-04564	1	IC,DIGITAL,74HCT08	U110
330-04566	1	IC,DIGITAL,74HCT27	U44
330-04567	1	IC,DIGITAL,74HCT32	U19
330-04572	2	IC,DIGITAL,74HCT245	U3,18
330-04588	1	IC,DIGITAL,74HCT03	U52
330-04675	1	IC,DIGITAL,74F08	U15
330-04676	2	IC,DIGITAL,74F161A	U9,36
MEMORY IC			
350-04282	2	IC,SRAM,4364,8KX8,150NS,LPS	U5,32
350-04434	10	IC,DRAM,64KX4,120NS	U64-68,93-97
350-04655	4	IC,SRAM,2018,2KX8,35NS	U13,14,26,27
350-04680	1	IC,ROM,82S123,M480L,TIMING	U103
350-04721	2	IC,ROM,74S472,M480L,CONTROL	U62,91
350-04722	2	IC,ROM,74S472,M480L,COEF	U77,112
MICROPROC IC			
365-04284	2	IC,uPROC,Z80,CMOS,4MHz	U4,31

MODULES			
380-03956	1	MOD,DLY LINE,5 TAP,30/150NS,LS	U40
CABLE CONN			
490-02356	5	CONN,JUMPER,.1X025,2FCG	W2,3,7,10,11
PC EDGE CONN			
500-04557	2	CONN,EURO,C,ROW a+c,MALE,RA	J1,2
PC MNT CONN			
510-04687	5	CONN,POST,100X025,HDR,3X2MCG	W1-15
SOCKETS			
520-00946	6	IC SCKT,40 PIN,PC,LO-PRO	U4,31,60,69,89,98
520-01458	2	IC SCKT,28 PIN,PC,LO-PRO	U5,32
KNOBS/CAPS			
550-04705	1	HANDLE,"U",1.5"	
MACHINE SCREWS			
640-03713	2	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	HANDLE MTG
THREADLS FASTNR			
650-04772	3	POPRVT,1/8X3/16,REG PROT HD,AL	STFNR MTG
BRACKETS			
701-04521	1	BRACKET,STFNR,PC,.25X.44X12.15	

6.8 HSP Board Rev. 3

CARBON FLM RES			
202-00542	3	RES,CF,5%,1/4W,4.7K OHM	R2,3,6
ELECTROLYT CAP			
240-02048	2	CAP,ELEC,47uF,25V,AX	C61,62
CERAMIC CAP			
245-03609	60	CAP,CER,.1uF,50V,Z5U,AX	C1-60
DIGITAL/CMOS IC			
330-03340	6	IC,DIGITAL,74F157	U10-12,37-39
330-03586	12	IC,DIGITAL,74HCT244	U1,2,16,17,29,41, U56,57,72,74,85,87
330-03715	16	IC,DIGITAL,74HCT374	U22,24,46,48,53,54,73, U75,79,80 U86,88,106,107,114,115
330-03766	2	IC,DIGITAL,MMU,64K,CMOS	U69,98
330-04041	3	IC,DIGITAL,74F10	U50,55,108
330-04042	17	IC,DIGITAL,74AHCT374	U61,63,70,71,76,78,83, U84,90,92,99,100, U104,111,113,118,119
330-04084	6	IC,DIGITAL,74HCT175	U30,58,59,82,109,117
330-04260	2	IC,DIGITAL,74HCT04	U20,51
330-04261	1	IC,DIGITAL,74HCT00	U42
330-04273	4	IC,DIGITAL,74HCT74,ZYTREX	U7,34,43,81
330-04275	2	IC,DIGITAL,74HCT139	U6,33
330-04292	6	IC,DIGITAL,74F32	U8,21,35,45,101,116
330-04293	2	IC,DIGITAL,74F74	U28,102
330-04292	2	IC,DIGITAL	U45,120
330-04294	1	IC,DIGITAL,74HCT138	U105
330-04362	2	IC,DIGITAL,ARU,18 BIT,CMOS,15M	U60,89
330-04511	4	IC,DIGITAL,74AHCT244	U23,25,47,49
330-04564	1	IC,DIGITAL,74HCT08	U110
330-04566	1	IC,DIGITAL,74HCT27	U44
330-04572	2	IC,DIGITAL,74HCT245	U3,18
330-04588	1	IC,DIGITAL,74HCT03	U52
330-04675	1	IC,DIGITAL,74F08	U15
330-04676	2	IC,DIGITAL,74F161A	U9,36
MEMORY IC			
350-04282	2	IC,SRAM,4364,8KX8,150NS,LPS	U5,32
350-04434	10	IC,DRAM,64KX4,12ONS	U64-68,93-97
350-04655	4	IC,SRAM,2018,2KX8,35NS	U13,14,26,27
350-04680	1	IC,ROM,82S123,M480L,TIMING	U103
350-04721	2	IC,ROM,74S472,M480L,CONTROL	U62,91
350-04722	2	IC,ROM,74S472,M480L,COEF	U77,112
MICROPROC IC			
365-04284	2	IC,uPROC,Z80,CMOS,4MHz	U4,31

MODULES			
380-03956	1	MOD,DLY LINE,5 TAP,30/150NS,LS	U40
CABLE CONN			
490-02356	5	CONN,JUMPER,.1X025,2FCG	W2,3,7,10,11
PC EDGE CONN			
500-04557	2	CONN,EURO,C,ROW a+c,MALE,RA	J1,2
PC MNT CONN			
510-04687	5	CONN,POST,100X025,HDR,3X2MCG	W1-15
SOCKETS			
520-00946	6	IC SCKT,40 PIN,PC,LO-PRO	U4,31,60,69,89,98
520-01458	2	IC SCKT,28 PIN,PC,LO-PRO	U5,32
KNOBS/CAPS			
550-04705	1	HANDLE,"U",1.5"	
MACHINE SCREWS			
640-03713	2	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	HANDLE MTG
THREADLS FASTNR			
650-04772	3	POPRVT,1/8X3/16,REG PROT HD,AL	STFNR MTG
BRACKETS			
701-04521	1	BRACKET,STFNR,PC,.25X.44X12.15	

6.9 Interface Adaptor Option

CABLE CONN			
490-00141	1	CONN,D-SUB,9MC,FB,SDR	
PC MNT CONN			
510-04933	6	CONN,BNC,1FC,MB,PC	
CONN HDWR			
527-04998	1	CONN,D-SUB,HOOD,9C,RND CA,RF1	
STRAIN REL			
530-02489	1	TIE,CABLE,NYL,.1"X4"	
530-04882	1	CLAMP,CABLE,3/8"	
LUGS			
620-01999	1	LUG,SOLDER,LCKNG,#6,.020THK	
INSUL/SPACRS			
630-02740	6	SPCR,#4CLX.21,3/16 RD,NYL	PCB MTG
SPCR,NON-INSUL			
635-04885	2	FASTNR,SWAGE,PCB,6-32X.065,SS	CABLE CLAMP & SOLDER LUG MTG
MACHINE SCREWS			
640-01700	6	SCRW,4-40X1/2,PNH,PH,SS	PCB MTG
640-01710	2	SCRW,6-32X1/4,PNH,PH,ZN	LUG, CLAMP
NUTS			
643-04942	6	NUT,1/2-28,HEX,BRASS/NI	BNC MTG
WASHERS			
644-01739	1	WSHR,INT STAR,#6	CLAMP
644-04943	12	WSHR,INT STAR,1/2"	BNC MTG
BULK WIRE			
670-04932	1	CABLE,24AWG,6TW-PR,FOIL SHLD,10'	
SLEEVING			
690-02522	2	SLEEVING,SHRINK,3/8"IDX1"	
PC BOARDS			
710-04874	1	PC BD,INTERFACE ADAPTOR,M2400	
LABEL/NAMEPLTS			
740-04884	1	LABEL,INTERFACE ADAPTER	ENCLOSURE
PURCH SUB-ASSY			
750-04978	1	ENCLOSURE,PLYS,MODIFIED,480L	

6.10 LARC Display Board

CERAMIC CAP			
245-01651	4	CAP,CER,.1uF,50V,80/20%	C1-4
DSPLY/IND/LED			
430-03413	6	LED,DSPLY,4-CHAR,DL-1414	U1-4
430-04985	8	LED,DSPLY,STICK,4 RED	CR1-32
SOCKETS			
520-02718	4	SOCKET STRIP,MACH,20C,.100X020	CR1-32
BULK WIRE			
670-03530	1	CABLE,FLEX-JUMP,29C,1.5X0.1	P3
PC BOARDS			
710-03393	1	PC BD,DISPLAY BD,LARC	

6.11 LARC Electronics Board

POTENTIOMETERS			
200-01445	6	POT,SLD,PC,10K-U,25MM X 45MM	R23-28
TRIM RESISTORS			
201-00439	1	RES,TRM,ST,PC,25K,SA,CER	R9
CARBON FLM RES			
202-00502	1	RES,CF,10%,1/2W,270 OHM	R22
202-00514	2	RES,CF,5%,1/4W,100 OHM	R12,13
202-00523	1	RES,CF,5%,1/4W,390 OHM	R20
202-00524	2	RES,CF,5%,1/4W,470 OHM	R10,30
202-00529	3	RES,CF,5%,1/4W,1K OHM	R6,14,29
202-00534	1	RES,CF,5%,1/4W,2.2K OHM	R3
202-00538	3	RES,CF,5%,1/4W,3.3K OHM	R1,4,31
202-00542	3	RES,CF,5%,1/4W,4.7K OHM	R15,18,19
202-00549	2	RES,CF,5%,1/4W,10K OHM	R8,11
202-00556	1	RES,CF,5%,1/4W,22K OHM	R21
202-00563	2	RES,CF,5%,1/4W,47K OHM	R7,17
202-00564	1	RES,CF,5%,1/4W,51K OHM	R2
202-00571	1	RES,CF,5%,1/4W,110K OHM	R5
202-00580	1	RES,CF,5%,1/4W,1M OHM	R16
NETWORK RES			
205-03531	4	RES,NET,SIP,2%,10KX5	RP1-4
ELECTROLYT CAP			
240-00609	3	CAP,ELEC,10uF,16V,RAD	C9,17,39
240-00616	1	CAP,ELEC,470uF,16V,AX	C41
240-00619	1	CAP,ELEC,1000uF,25V,AX	C36
240-02048	1	CAP,ELEC,47uF,25V,AX	C37

TANTALUM CAP			
241-00652	1	CAP,TANT,4.7uF,25V,RAD	C26
CERAMIC CAP			
245-00585	2	CAP,CER,18pF,50V,10%	C24,25
245-00590	1	CAP,CER,150pF,500V,10%	C1
245-00594	5	CAP,CER,.001uF,500V,10%,Z5F	C18,23,27,29,40
245-00598	15	CAP,CER,.01uF,16V,80/20%	C2,4,10-16,19-22,34,38
245-01651	12	CAP,CER,.1uF,50V,80/20%	C3,5-8,28,30-32,33,35,42
INDUCTORS			
270-00779	10	FERRITE,BEAD	FB1-10
270-03497	1	INDUCTOR,300uH,1A,SWITCHING	L1
DIODES			
300-01024	1	DIODE,1N746	CR6
300-01029	4	DIODE,1N914 AND 4148	CR1-4
300-02401	1	DIODE,BAR 35,SCHOTTKY,LOW VF	CR5
300-03498	1	DIODE,SCHOTTKEY,POWER,3A	CR8
300-03546	1	DIODE,BRIDGE,2A,200V	CR7
TRANSISTORS			
310-03438	1	TRANSISTOR,IRFD9120,FET	Q1
DIGITAL/CMOS IC			
330-00767	1	IC,DIGITAL,4013,CMOS	U10
330-00768	1	IC,DIGITAL,4049,CMOS	U6
330-03496	1	IC,DIGITAL,CD4515,CMOS	U11
LINEAR IC			
340-00725	1	IC,LINEAR,LM311	U1
340-03499	1	IC,LINEAR,MC34060 OR TL494	U12
INTERFACE IC			
345-00751	1	IC,INTER,75492,LED DRVR	U4
345-02913	1	IC,INTER,NE594,DSP DRVR,8-SEG	U7
345-03207	1	IC,INTER,uA9638,LINE DRVR	U3
345-03208	1	IC,INTER,uA9637A,LINE RCVR	U2
CONVERTER IC			
355-02903	1	IC,CONVERTER,ADC 0809	U5
MICROPROC IC			
365-03526	1	IC,uPROC,CDP1854 or IM6402	U8
365-04066	1	IC,uPROC,8749,LARC,V1.0A	U9
CRYSTALS			
390-02210	1	CRYSTAL,4.608 MHz	Y1
FUSES			
440-02466	1	FUSE,1AG,FAST,1AMP,32V	F1
CABLE CONN			
490-00998	1	CONN,DIN,5FC,180DEG	J0

PC MNT CONN			
510-03088	1	CONN,POST,100X025,HDR,10MCG	W1
510-03484	1	CONN,DC POWER,PC,SMK S-G9314	J2
510-03549	1	CONN,D-SUB,9MC,FB,PCRA	J1
SOCKETS			
520-00941	3	IC SCKT,8 PIN,PC,LO-PRO	U1-3
520-00942	2	IC SCKT,14 PIN,PC,LO-PRO	U4,10
520-00943	2	IC SCKT,16 PIN,PC,LO-PRO	U6,12
520-00945	1	IC SCKT,24 PIN,PC,LO-PRO	U11
520-00946	2	IC SCKT,40 PIN,PC,LO-PRO	U8,9
520-01458	1	IC SCKT,28 PIN,PC,LO-PRO	U5
520-02177	1	IC SCKT,18 PIN,PC,LO-PRO	U7
ELECTRONIC HDWR			
600-00871	2	FUSE CLIP,1/4",PC	F1
INSUL/SPACRS			
630-00953	2	WSHR,FL,#6CLX3/80DX1/16,FBR	COMP SIDE ELECT BD TO ENCLOSURE
630-03544	2	WSHR,FL,#6CLX3/8ODX.032,FBR	SUB-PNL TO CIRC SIDE ELECT BD
MACHINE SCREWS			
640-01701	2	SCRW,4-40X1/4,PNH,PH,ZN	DE-9 TO ELECT PCB MTG
NUTS			
643-01732	2	NUT,4-40,KEP,ZN	DE-9 TO ELECT PCB MTG
PRE-CUT WIRE			
675-02884	3	WIRE,24G,WHT,1.5",ST&T1/4X1/4	P1 TO J0
675-03722	1	WIRE,24G,WHT,2",ST&T1/4X1/4	P1-1 TO J0-4

6.12 LARC Mechanical

CONN HDWR			
527-00138	2	CONN,D-SUB,JACKSOCKET,.150"	DE-9 TO CHASSIS BRKT MTG
GROMMETS			
540-03532	1	GUARD,DUST,LARC	
KNOBS/CAPS			
550-03388	6	KNOB,SLIDE POT,WHITE	
550-03415	1	BUTTON,.57X.47,"PROG" LEG,BLU	
550-03416	1	BUTTON,.57X.47,"REG" LEG,BLU	
550-03417	1	BUTTON,.57X.47,"0" LEG,WHT	
550-03418	1	BUTTON,.57X.47,"1" LEG,WHT	
550-03419	1	BUTTON,.57X.47,"2" LEG,WHT	
550-03420	1	BUTTON.,57X.47,"3" LEG,WHT	
550-03421	1	BUTTON,.57X.47,"4" LEG,WHT	
550-03422	1	BUTTON,.57X.47,"5" LEG,WHT	
550-03423	1	BUTTON,.57X.47,"6" LEG,WHT	
550-03424	1	BUTTON,.57X.47,"7" LEG,WHT	
550-03425	1	BUTTON,.57X.47,"8" LEG,WHT	
550-03426	1	BUTTON,.57X.47,"9" LEG,WHT	
550-03427	1	BUTTON,.57X.47,"VAR" LEG,WHT	
550-03428	1	BUTTON,.57X.47,"BANK" LEG,WHT	
550-03429	1	BUTTON,.57X.47,"STO" LEG,WHT	
550-03431	1	BUTTON,.57X.47,"MUTE" LEG,WHT	
550-03433	1	BUTTON,.57X.47,"2nd F" LEG,WHT	
550-03434	1	BUTTON,.57X.47,"PAGE" LEG,WHT	
550-04724	1	BUTTON,.57X.47,"MACH" LEG,WHT	
550-04725	1	BUTTON,.57X.47,"CTRL" LEG,WHT	
PC HDWR			
610-02269	2	HARDWARE,PC,RICHCO #MB-3-156	DISPLAY BD TO PANEL BD
SPCR,NON-INSUL			
635-01655	2	SPCR,6-32X7/16,1/4HEX,AL	ELECT BD TO CASE MTG
635-03541	2	SPCR,#6CLX.355,1/4RD,BR/N	SUB-PNL TO PNL BD MTG
MACHINE SCREWS			
640-02378	4	SCRW,6-32X7/16,TH,PH,BLK	PCB TO CASE MTG
640-02746	6	SCRW,2-M3X.5MMX.175L,PNH,PH,ZN	R23-28 MTG
640-02812	2	SCRW,4-40X3/8,PNH,PH,BLK	DIN TO CHASSIS BRKT MTG
640-03713	2	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	CONN BRKT TO PNL BD MTG
THRD-FORM SCRW			
641-03543	2	SCRW,TAP,F,4-40X1/4,PNH,PH,ZN	DSPLY BD MTG
NUTS			
643-01733	2	NUT,4-40,HEX,SMALL,ZN	DIN TO CHASSIS BRKT MTG

WASHERS			
644-01736	2	WSHR,FL,#4CLX.218ODX.032THK	DSPLY BD MTG
644-01737	2	WSHR,LOCK,SPLIT,#4	DIN TO CHASSIS BRKT MTG
644-01747	6	WSHR,INT STAR,#4	
644-02379	4	WSHR,FL,#6CLX3/8ODX.031THK,BLK	PCB TO CASE MTG
644-02716	2	WSHR,FL,#4CLX.312ODX.03THK	DIN TO CHASSIS BRKT MTG
CABLES/CORDS			
680-03525	1	CABLE,50',LARC	
CHASSIS/MECH			
700-03391	1	ENCLOSURE,BOTTOM,LARC	
700-03392	1	ENCLOSURE,TOP,LARC	
700-03448	1	CHASSIS,BRACKET,LARC	
PANELS			
702-03374	1	PANEL,SUB,LARC	
702-03375	1	PANEL,OVERLAY,LARC	
702-03545	1	PROTECTIVE COVER,LARC	
LENS/PLATE/PANL			
703-03410	1	LENS,DISPLAY,LARC w/white Lines	
PLASTICS			
720-03548	2	TAPE,FOAM,1/16X1/2X3.4	BUMPER FEET

6.13 LARC Panel board

CARBON FLM RES			
202-00509	8	RES,CF,5%,1/4W,47 OHM	R5-12
202-00529	4	RES,CF,5%,1/4W,1K OHM	R1-4
ELECTROLYT CAP			
240-00609	1	CAP,ELEC,10uF,16V,RAD	C1
CERAMIC CAP			
245-01651	4	CAP,CER,.1uF,50V,80/20%	C2-5
DIODES			
300-01023	8	DIODE,1N283	CR1-8
DSPLY/IND/LED			
430-03413	6	LED,DSPLY,4-CHAR,DL-1414	U1-6
PSH BUT SWITCH			
453-03440	26	SW,PBM,1P1T,TANG,PC	SW1-16,18-22,26-30
SOCKETS			
520-02718	4	SOCKET STRIP,MACH,20C,.100X020	U1-6

KNOBS/CAPS			
550-03390	6	BUTTON,.57X.47,WHT	SW1-6
SPCR,NON-INSUL			
635-03542	2	SPCR,SWAGE,#6CLX.594,1/4RD,BR	PNL BD TO ELECT BD MTG
BULK WIRE			
670-02837	1	CABLE,FLEX-JUMP,19C,1.5X0.1	P2 (USE 10 OF 19 PINS)
670-03530	1	CABLE,FLEX-JUMP,29C,1.5X0.1	P2

6.14 LARC Shipping Kit

CUST LITERATURE		
070-03759	1	INSTR,PANEL MOUNT,LARC
INSUL/SPACRS		
630-00953	2	WSHR,FL,#6CLX3/80DX1/16,FBR
SPCR,NON-INSUL		
635-03720	2	SPCR,6-32X1/2,1/4HEX,BR/N

6.15 Motherboard

POTENTIOMETERS			
200-04559	6	POT,RTY,PC,10K-A,1/8"/FLAT	R103,104,144,145,156,191
TRIM RESISTORS			
201-00159	4	RES,TRM,ST,PC,100K,SA,CER	R121,127,146,149
201-01619	3	RES,TRM,ST,PC,500 OHM,SA,CER	R32,214,224
CARBON FLM RES			
202-00505	2	RES,CF,5%,1/4W,10 OHM	R72,74
202-00510	8	RES,CF,5%,1/4W,51 OHM	R164,165,183,184,199,200, R221,222
202-00512	2	RES,CF,5%,1/4W,75 OHM	R56,67
202-00515	3	RES,CF,5%,1/4W,150 OHM	R70,168,203
202-00518	8	RES,CF,5%,1/4W,220 OHM	R1,2,4-6,58,69,239
202-00525	15	RES,CF,5%,1/4W,510 OHM	R8-17,36,37,44,77,122
202-00529	11	RES,CF,5%,1/4W,1K OHM	R24-28,30,33,71,73,185,223
202-00533	13	RES,CF,5%,1/4W,2K OHM	R22,23,42,43,75,76,117,123,147 R151,182,209,217
202-00535	4	RES,CF,5%,1/4W,2.4K OHM	R3,7,34,35
202-00538	6	RES,CF,5%,1/4W,3.3K OHM	R18,19,175,176,225,226
202-00555	9	RES,CF,5%,1/4W,20K OHM	R21,29,49,52,60,63,148,150,R204
202-00557	3	RES,CF,5%,1/4W,24K OHM	R31,53,65
202-00570	4	RES,CF,5%,1/4W,100K OHM	R40,41,119,125
202-00580	11	RES,CF,5%,1/4W,1M OHM	R95-98,120,126,136-139,186
202-01497	2	RES,CF,5%,1/4W,2M OHM	R212,213
202-02650	1	RES,CF,5%,1/2W,750 OHM	R20
METAL FLM RES			
203-00450	6	RES,MF,1%,1/8W,100 OHM	R50,51,61,62,169,205
203-00457	16	RES,MF,1%,1/8W,1.50K OHM	R100,102,118,124,142,143,157 R161,171,172,174,192,196,207 R208,211
203-00471	22	RES,MF,1%,1/8W,10.0K OHM	R38,39,57,68,78,79,88-90,128 R129,131,154,155,166,167,177 R189,190,201,202,215
203-00472	2	RES,MF,1%,1/8W,10.2K OHM	R153,188
203-00476	2	RES,MF,1%,1/8W,12.1K OHM	R54,64
203-00480	4	RES,MF,1%,1/8W,15.0K OHM	R99,101,140,141
203-00482	2	RES,MF,1%,1/8W,20.0K OHM	R160,195
203-01137	4	RES,MF,1%,1/8W,4.12K OHM	R48,55,59,66
203-01229	4	RES,MF,1%,1/8W,6.98K OHM	R108,110,113,116
203-01230	4	RES,MF,1%,1/8W,8.25K OHM	R107,109,112,115
203-01491	6	RES,MF,1%,1/8W,4.22K OHM	R84-87,158,193
203-01495	2	RES,MF,1%,1/8W,33.2K OHM	R162,197
203-01996	14	RES,MF,1/2%,1/8W,3.01K OHM	R105,106,111,114,170,178-181 R206,216,218-220
203-02291	4	RES,MF,1%,1/8W,5.49K OHM	R159,194,236,238
203-02701	2	RES,MF,1%,1/8W,13.3K OHM	R163,198
203-04562	8	RES,MF,1%,1W,33.2 OHM,FP	R45,46,80,82,91,92,130,132

NETWORK RES			
205-01133	4	RES,NET,DIP,1%,10KX8	RP1-4
ELECTROLYT CAP			
240-00613	17	CAP,ELEC,22uF,25V,RAD	C29,41,42,47,49,110,112,116 C118,174,177,153,154,189,190 C213,216
240-00614	12	CAP,ELEC,47uF,16V,RAD	C12,16,32,38,44,51,93,95,113 C119,125,127
240-01262	2	CAP,ELEC,330uF,25V,RAD	C27,28
240-03574	2	CAP,ELEC,3300uF,35V,RAD,LO-PRO	C15,26
240-03901	1	CAP,ELEC,1000uF,35V,RAD,LO-PRO	C4
TANTALUM CAP			
241-00652	14	CAP,TANT,4.7uF,25V,RAD	C81,82,84,86,129,133,135,139 C161,162,168,197,199,206
PCRB/PP CAP			
244-00660	4	CAP,MYL,.01uF,100V,10%,RAD	C94,96,126,128
244-01151	2	CAP,PP,1000pF,2.5%	C166,202
244-01171	4	CAP,PP,5100pF,2.5%	C97,102,103,108
244-02342	8	CAP,MYL,.68uF,50V,10%,RAD	C36,37,159,160,195,196,209,210
244-04585	10	CAP,PP,100pF,50V,2.5%,RAD	C144,145,147-151,184,185,187
~~244-04586~~	4	CAP,PP,240pF,50V,2.5%,RAD	C98,100,104,106
244-04587	8	CAP,PP,510pF,50V,2.5%,RAD	C61,62,66,67,71,72,76,77
CERAMIC CAP			
245-00590	12	CAP,CER,150pF,500V,10%	C58,59,88-90,120-122,141,142 C181,182
245-00594	1	CAP,CER,.001uF,500V,10%,Z5F	C180
245-03609	77	CAP,CER,.1uF,50V,Z5U,AX	C1-3,5-11,13,14,17-25,30,31 C33-35,39,46,53-57,60,63,65,68 C70,73,75,78,91,92,99,101,105 C107,109,111,114,115,117,123 C124,134,140,146,152,156,158 C169,171,175,176,178,179,186 C188,192,194,204,205,208,214 C215,217,218
245-03610	17	CAP,CER,.01uF,100V,Z5U,AX	C40,45,48,52,80,83,85,87,130 C132,136,138,163,165,198,201 C221
245-03867	7	CAP,CER,10pF,100V,COG,10%,AX	C43,50,131,137,170,207,222
245-03868	12	CAP,CER,33pF,100V,COG,10%,AX	C155,157,191,193,229-236
245-03869	4	CAP,CER,100pF,100V,COG,10%,AX	C172,173,211,212
245-03871	2	CAP,CER,1000pF,100V,X7R,10%,AX	C167,203
INDUCTORS			
270-00779	16	FERRITE,BEAD	FB1-16
270-03899	1	INDUCTOR,2.2mH,LINE CHOKE	L1

DIODES			
300-01029	12	DIODE,1N914 AND 4148	CR1,8,9,13,23-30
300-01030	7	DIODE,1N4004 AND 4005	CR2,5-7,10-12
300-01154	1	DIODE,1N751,ZENER,5.1V	CR20
300-02401	4	DIODE,BAR 35,SCHOTTKY,LOW VF	CR18,19,21,22
300-03546	2	DIODE,BRIDGE,2A,200V	CR3,4
TRANSISTORS			
310-01646	2	TRANSISTOR,2N4403	Q4,5
310-01647	5	TRANSISTOR,2N4401	Q1-3,11,13
310-04289	4	TRANSISTOR,J105	Q6-9
310-04582	2	XISTOR,NPD5566	Q10,12
DIGITAL/CMOS IC			
330-03715	1	IC,DIGITAL,74HCT374	U14
330-03768	2	IC,DIGITAL,CMU,16 BITS,CMOS	U34,35
330-04260	2	IC,DIGITAL,74HCT04	U20,33
330-04261	1	IC,DIGITAL,74HCT00	U25
330-04273	2	IC,DIGITAL,74HCT74,ZYTREX	U15,16
330-04570	2	IC,DIGITAL,74HCT165	U26,28
330-04573	1	IC,DIGITAL,74HCT393	U5
330-04589	3	IC,DIGITAL,74HCT14	U2,11,13
330-04672	6	IC,DIGITAL,74HC595	U18,19,21-24
330-04674	1	IC,DIGITAL,74HC4538	U27
LINEAR IC			
340-00725	5	IC,LINEAR,LM311	U10,60,61,69,70
340-00742	1	IC,LINEAR,7805 (LM 340 T-5)	U1
340-00745	1	IC,LINEAR,7815 (LM 340 T-15)	U7
340-00747	1	IC,LINEAR,7915 (LM 320 T-15)	U17
340-03328	10	IC,LINEAR,NE5534	U30,32,37,39,41,43,56,58 U64,66
340-03587	2	IC,LINEAR,OP-37	U51,53
340-03858	2	IC,LINEAR,RC4560NB	U59,68
340-04433	6	IC,LINEAR,LM833	U48,49,54,55,62,63
340-04678	2	IC,LINEAR,LM211H	U44,46
340-04681	1	IC,LINEAR,TL288CP	U67
SS SW IC			
346-03329	8	IC,SS SWITCH,SD5000N	U36,38,40,42,50,52,57,65
MEMORY IC			
350-04868	1	IC,ROM,27C64,TIMING,M480L	U6
CONVERTER IC		A to D converter	
355-04590	4	DAC,PCM53KP-I	U29,31,45,47
SEMICONDUCTORS			
360-01612	1	SEMICOND,VARISTOR	VR3
HYBRID CIRCUITS			
370-04426	4	HYBRID,LINE AMP,LLA5200	OPA1-4

OPTO ISLTOR IC			
375-02247	2	IC,OPTO-ISOLATOR,6N 138	U8,9
375-04591	3	IC,OPTO-ISOLATOR,HCPL2630	U3,4,12
MODULES			
380-04512	6	MOD,LPF,9P,20.0KHz	LPF1-6
DSPLY/IND/LED			
430-04642	4	LED,T1,RED,RA BLOCK	CR14-17
430-04656	1	LED,RED,LIGHT BAR,HLMP-2685	DS1
FUSES			
440-01877	2	FUSE,5X20MM,SLO-BLO,1.25AMP	F1,2
CABLE CONN			
490-02356	5	CONN,JUMPER,.1X025,2FCG	W1-4,13
PC MNT CONN			
510-02534	4	CONN,XLR,3MC,PCRA	J4-7
510-02535	2	CONN,XLR,3FC,PCRA	J8,9
510-02671	4	CONN,POST,100X025,HDR,3MC,GOLD	W1-4
510-03711	1	CONN,POST,100X025,HDR,26MC,LOK	P5
510-03922	3	CONN,POST,100X025,HDR,6MCG	TP2,3,6
510-03961	1	CONN,POST,100X025,HDR,2MCG	W13
510-04286	3	CONN,CIRC DIN,5FC@180DEG,PCRA	J1-3
510-04639	8	CONN,QDC MALE,PCRA,.110"X.020"	P1-4,6-9
SOCKETS			
520-00941	7	IC SCKT,8 PIN,PC,LO-PRO	U3,4,12,30,32,58,66
520-00943	9	IC SCKT,16 PIN,PC,LO-PRO	U36,38,40,42,50,52,57,65, DS1
520-00945	4	IC SCKT,24 PIN,PC,LO-PRO	U29,31,45,47
520-00946	2	IC SCKT,40 PIN,PC,LO-PRO	U34,35
520-01458	1	IC SCKT,28 PIN,PC,LO-PRO	U6
ELECTRONIC HDWR			
600-01668	1	BUSS BAR,2C,.7X14,.3 OFF,PVF/N	
600-02227	4	FUSE CLIP,20MM,PC	F1,2
INSUL/SPACRS			
630-00952	3	INSUL,SEMI,BUSHING,TO-220	U1,7,17
630-01853	3	INSUL,SEMI,SIL RUB,TO-220	U1,7,17
THRD-FORM SCRW			
641-02827	6	SCRW,TAP,F,2-56X3/16,PNH,PH,ZN	J4-9
641-04021	3	SCRW,TAP,SW,4-40X1/4,PNH,PH,ZN	U1,7,17
THREADLS FASTNR			
650-03970	2	POPRVT,1/8X1/8,REG PROT HD,SS	HEATSINK BRKT MTG
BULK WIRE			
670-01974	8	WIRE,JMP,22AWG,0.1",NON-INSUL	W5-12
670-04918	4	WIRE,JMP,22AWG,0.4",TEF,WHT	R227,229,231,233

BRACKETS			
701-04162	1	BRACKET,HEATSINK,M70	
PC BOARDS			
710-04371	1	PC BD,MOTHERBD,M480L	
PLASTICS			
720-03571	4	TAPE,KAPTON,1/2"	C229-236

6.16 Host Processor Board (Rev. 2 and Higher)

CARBON FLM RES			
202-00505	6	RES,CF,5%,1/4W,10 OHM	R35,37,38,42,50,51
202-00510	3	RES,CF,5%,1/4W,51 OHM	R39,43,47
202-00512	3	RES,CF,5%,1/4W,75 OHM	R40,44,48
202-00516	3	RES,CF,5%,1/4W,180 OHM	R1,5,9
202-00517	6	RES,CF,5%,1/4W,200 OHM	R16-19,54,62
202-00525	3	RES,CF,5%,1/4W,510 OHM	R33,63,64
202-00529	10	RES,CF,5%,1/4W,1K OHM	R14,24-30,55,59
202-00533	2	RES,CF,5%,1/4W,2K OHM	R53,56
202-00538	9	RES,CF,5%,1/4W,3.3K OHM	R10,12,13,36,41,45,46,49,52
202-00543	6	RES,CF,5%,1/4W,5.1K OHM	R2-4,6-8
202-00549	5	RES,CF,5%,1/4W,10K OHM	R11,31,32,57,58
202-00570	2	RES,CF,5%,1/4W,100K OHM	R15,61
METAL FLM RES			
203-00488	1	RES,MF,1%,1/8W,37.4K OHM	R21
203-01495	1	RES,MF,1%,1/8W,33.2K OHM	R20
203-02352	1	RES,MF,1%,1/8W,24.9K OHM	R60
203-03345	2	RES,MF,1%,1/8W,3.4K OHM	R22,23
NETWORK RES			
205-01590	1	RES,NET,SIP,2%,2.2KX9	U5
ELECTROLYT CAP			
240-02048	2	CAP,ELEC,47uF,25V,AX	C25,26
TANTALUM CAP			
241-00652	1	CAP,TANT,4.7uF,25V,RAD	C23
241-00654	2	CAP,TANT,22uF,16V,RAD	C24,50
PCRB/PP CAP			
244-01488	1	CAP,MYL,.22uF,100V,10%,RAD	C52
CERAMIC CAP			
245-01164	1	CAP,CER,10pF,50V,10%	C10
245-03609	63	CAP,CER,.1uF,50V,Z5U,AX	C1-9,11-22,27-49,51,53-66,68 C75,77,79
245-03610	1	CAP,CER,.01uF,100V,Z5U,AX	C76
245-03868	3	CAP,CER,33pF,100V,COG,10%,AX	C71,73,74
245-03869	3	CAP,CER,100pF,100V,COG,10%,AX	C70,72,81
245-03870	1	CAP,CER,150pF,100V,COG,10%,AX	C80
245-03871	2	CAP,CER,1000pF,100V,X7R,10%,AX	C67,69

VARIABLE CAP			
246-04649	1	CAP,TRIM,4-27pF,VAR,PCRA	C78
INDUCTORS			
270-00779	8	FERRITE,BEAD	FB1-8
270-04706	1	INDUCTOR,1.2uHy,SHIELDED	L1
DIODES			
300-01029	14	DIODE,1N914 AND 4148	CR5,6,10-17,19-22
300-01030	1	DIODE,1N4004 AND 4005	CR8
300-02401	3	DIODE,BAR 35,SCHOTTKY,LOW VF	CR7,9,18
300-02507	1	DIODE,VARACTOR,MV209	VRC1,2
TRANSISTORS			
310-01007	1	TRANSISTOR,2N3904	Q2
310-01008	1	TRANSISTOR,2N3906	Q1
310-01647	3	TRANSISTOR,2N4401	Q4-6
310-02517	1	TRANSISTOR,2N5910	Q3
DIGITAL/CMOS IC			
330-00694	3	IC,DIGITAL,74LS03	U11,37,47
330-00698	1	IC,DIGITAL,74LS14	U97
330-00767	1	IC,DIGITAL,4013,CMOS	U46
330-01298	1	IC,DIGITAL,MC4044	U92
330-03586	8	IC,DIGITAL,74HCT244	U15,18-20,26,30,32,93
330-03715	10	IC,DIGITAL,74HCT374	U58,59,61-64,72,73,85,86
330-04040	1	IC,DIGITAL,74F04	U103
330-04084	2	IC,DIGITAL,74HCT175	U12,16
330-04260	2	IC,DIGITAL,74HCT04	U9,48
330-04261	2	IC,DIGITAL,74HCT00	U49,96
330-04271	2	IC,DIGITAL,74HCT273	U60,78
330-04273	1	IC,DIGITAL,74HCT74,ZYTREX	U10
330-04274	1	IC,DIGITAL,74HCT132	U98
330-04292	1	IC,DIGITAL,74F32	U101
330-04293	2	IC,DIGITAL,74F74	U91,100
330-04294	5	IC,DIGITAL,74HCT138	U22,31,87,88,95
330-04563	1	IC,DIGITAL,74HCT02	U51
330-04564	2	IC,DIGITAL,74HCT08	U21,50
330-04565	1	IC,DIGITAL,74HCT11	U27
330-04567	1	IC,DIGITAL,74HCT32	U25
330-04568	1	IC,DIGITAL,74HCT148	U17
330-04569	2	IC,DIGITAL,74HCT157	U94,99
330-04570	1	IC,DIGITAL,74HCT165	U28
330-04571	1	IC,DIGITAL,74HCT174	U44
330-04572	2	IC,DIGITAL,74HCT245	U29,33
330-04573	1	IC,DIGITAL,74HCT393	U13
330-04640	2	IC,DIGITAL,74HCT85	U74,75
330-04644	1	IC,DIGITAL,MC1648	U107
330-04672	6	IC,DIGITAL,74HC595	U56,57,70,71,83,84
330-04673	12	IC,DIGITAL,74HC597	U52-55,65-67,69,79-82
330-04674	1	IC,DIGITAL,74HC4538	U36
330-04676	3	IC,DIGITAL,74F161A	U104-106
330-04677	1	IC,DIGITAL,74F253	U102
330-04892	2	IC,DIGITAL,74HCT74,RCA	U8,76

LINEAR IC			
340-01363	1	IC,LINEAR,LM339	U45
INTERFACE IC			
345-03207	2	IC,INTER,uA9638,LINE DRVR	U1,2
345-03208	2	IC,INTER,uA9637A,LINE RCVR	U3,4
MEMORY IC			
350-04709	1	IC,PAL,16P8A,M480L,MEM,V2.10 for Rev. 1 Host	U24
350-04710	2	IC,SRAM,43256,150NS,LPS	U38,39
350-05824	1	IC,PAL,16P28A,MEM,V3.00 for Rev. 3 Host	U41
350-04867	1	IC,ROM,27C64,HOST,M480L,V1.00	U68
350-04920	1	IC,ROM,27512,M480L,V1.23-1	U40
350-04921	1	IC,ROM,27512,M480L,V1.23-2	U41
350-04922	1	IC,ROM,27512,M480L,V1.23-3	U42
350-05800	1	IC,PAL,16P8A,M480L,DTACK,V2.00	U23
350-05801	1	IC,PAL,16R8A,M480L,PEAK,V1.00	U77
MICROPROC IC			
365-04593	2	IC,uPROC,DUART,MC68681	U6,7
365-04594	1	IC,uPROC,MC68008	U34
CRYSTALS			
390-04595	1	CRYSTAL OSC,14.112 MHz	U89
390-04596	1	CRYSTAL OSC,15.360 MHz	U90
390-04597	1	CRYSTAL OSC,16.000 MHz	U14
390-04645	1	CRYSTAL,3.6864MHz	Y1
DSPLY/IND/LED			
430-04642	4	LED,T1,RED,RA BLOCK	CR1-4
BATTERIES			
460-04598	2	BATTERY,LITH,3V,FLAT	BT1,2
CABLE CONN			
490-02356	2	CONN,JUMPER,.1X025,2FCG	W3,4
PC EDGE CONN			
500-04557	2	CONN,EURO,C,ROW a+c,MALE,RA	P1,2
PC MNT CONN			
510-02671	4	CONN,POST,100X025,HDR,3MC,GOLD	W2-4; TP1
510-03922	1	CONN,POST,100X025,HDR,6MCG	TP4
510-03961	3	CONN,POST,100X025,HDR,2MCG	W1; TP2,3
510-04638	1	CONN,HDR,PCRA,30MC,LOK	J1
SOCKETS			
520-00946	2	IC SCKT,40 PIN,PC,LO-PRO	U6,7
520-01361	3	IC SCKT,20 PIN,PC,LO-PRO	U23,24,77
520-01458	4	IC SCKT,28 PIN,PC,LO-PRO	U35,38,39,68
520-04688	1	IC SCKT,48 PIN,PC,LO-PRO	U34
520-04999	4	IC SCKT,32 PIN,PC,MACH,TIN	U40-43

KNOBS/CAPS			
550-04705	1	HANDLE,"U",1.5"	
MACHINE SCREWS			
640-03713	2	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	HANDLE MTG
THREADLS FASTNR			
650-04772	3	POPRVT,1/8X3/16,REG PROT HD,AL	STFNR
BULK WIRE			
670-01974	2	WIRE,JMP,22AWG,0.1",NON-INSUL	W2,5
BRACKETS			
701-04523	1	BRACKET,STFNR,PC,.25X.44X9.65	
PC BOARDS			
710-04378	1	PC BD,HOST PROC BD,M480L,REV 3	
PLASTICS			
720-02751	1	TAPE,FOAM,DBL-STK,1/8THX3/4W	

6.17 Host Processor Board (Rev. 1)

CARBON FLM RES			
202-00505	6	RES,CF,5%,1/4W,10 OHM	R35,37,38,42,50,51
202-00510	3	RES,CF,5%,1/4W,51 OHM	R39,43,47
202-00512	3	RES,CF,5%,1/4W,75 OHM	R40,44,48
202-00517	6	RES,CF,5%,1/4W,200 OHM	R5-8,23,31
202-00525	3	RES,CF,5%,1/4W,510 OHM	R21,33,34
202-00529	16	RES,CF,5%,1/4W,1K OHM	R1-4,11-14,16-19,25,28,62,63
202-00533	2	RES,CF,5%,1/4W,2K OHM	R22,26
202-00538	10	RES,CF,5%,1/4W,3.3K OHM	R30,36,41,45,46,49,53-56
202-00543	3	RES,CF,5%,1/4W,5.1K OHM	R64-66
202-00549	3	RES,CF,5%,1/4W,10K OHM	R20,24,27
202-00570	2	RES,CF,5%,1/4W,100K OHM	R32,61
METAL FLM RES			
203-00456	4	RES,MF,1%,1/8W,1.00K OHM	R57-60
203-00488	1	RES,MF,1%,1/8W,37.4K OHM	R10
203-01495	1	RES,MF,1%,1/8W,33.2K OHM	R9
203-02352	1	RES,MF,1%,1/8W,24.9K OHM	R29
203-02656	1	RES,MF,1%,1/8W,182K OHM	R15
NETWORK RES			
205-01590	1	RES,NET,SIP,2%,2.2KX9	U5
ELECTROLYT CAP			
240-02048	2	CAP,ELEC,47uF,25V,AX	C26,27
TANTALUM CAP			
241-00652	2	CAP,TANT,4.7uF,25V,RAD	C24,35
241-00654	1	CAP,TANT,22uF,16V,RAD	C25
PCRB/PP CAP			
244-01488	1	CAP,MYL,.22uF,100V,10%,RAD	C53

CERAMIC CAP			
245-02105	2	CAP,CER,5pF,500V,10%,NPO	C10,11
245-03609	63	CAP,CER,.1uF,50V,Z5U,AX	C1-9,12-23,28-34,36-52,55 C57-72,74
245-03610	1	CAP,CER,.01uF,100V,Z5U,AX	C75
245-03868	3	CAP,CER,33pF,100V,COG,10%,AX	C78,80,82
245-03869	3	CAP,CER,100pF,100V,COG,10%,AX	C77,79,81
245-03870	1	CAP,CER,150pF,100V,COG,10%,AX	C73
245-03871	2	CAP,CER,1000pF,100V,X7R,10%,AX	C54,56
VARIABLE CAP			
246-04649	1	CAP,TRIM,4-27pF,VAR,PCRA	C76
INDUCTORS			
270-00779	7	FERRITE,BEAD	FB1-7
270-04706	1	INDUCTOR,1.2uHy,SHIELDED	L1
DIODES			
300-01029	15	DIODE,1N914 AND 4148	CR5,6,10,12-23
300-01030	1	DIODE,1N4004 AND 4005	CR8
300-02401	3	DIODE,BAR 35,SCHOTTKY,LOW VF	CR7,9,11
300-02507	1	DIODE,VARACTOR,MV209	VRC1,2
TRANSISTORS			
310-01007	1	TRANSISTOR,2N3904	Q2
310-01008	1	TRANSISTOR,2N3906	Q1
310-01647	3	TRANSISTOR,2N4401	Q4-6
310-02517	1	TRANSISTOR,2N5910	Q3
DIGITAL/CMOS IC			
330-00694	3	IC,DIGITAL,74LS03	U11,47,50
330-00698	1	IC,DIGITAL,74LS14	U100
330-00767	1	IC,DIGITAL,4013,CMOS	U49
330-01298	1	IC,DIGITAL,MC4044	U96
330-03586	8	IC,DIGITAL,74HCT244	U20-22,31,32,37,67,97
330-03715	8	IC,DIGITAL,74HCT374	U61,62,64,66,75,76,89,90
330-04040	1	IC,DIGITAL,74F04	U106
330-04084	2	IC,DIGITAL,74HCT175	U14,17
330-04260	3	IC,DIGITAL,74HCT04	U9,27,51
330-04261	2	IC,DIGITAL,74HCT00	U15,99
330-04271	4	IC,DIGITAL,74HCT273	U28,63,65,81
330-04273	1	IC,DIGITAL,74HCT74,ZYTREX	U10
330-04274	1	IC,DIGITAL,74HCT132	U52
330-04292	1	IC,DIGITAL,74F32	U104
330-04293	2	IC,DIGITAL,74F74	U95,113
330-04294	5	IC,DIGITAL,74HCT138	U26,33,91,92,98
330-04563	1	IC,DIGITAL,74HCT02	U54
330-04564	3	IC,DIGITAL,74HCT08	U25,53,112
330-04565	1	IC,DIGITAL,74HCT11	U29
330-04567	2	IC,DIGITAL,74HCT32	U12,44
330-04568	1	IC,DIGITAL,74HCT148	U19
330-04569	3	IC,DIGITAL,74HCT157	U102,103,111
330-04570	1	IC,DIGITAL,74HCT165	U30
330-04571	1	IC,DIGITAL,74HCT174	U48

330-04572	2	IC,DIGITAL,74HCT245	U35,36
330-04573	1	IC,DIGITAL,74HCT393	U16
330-04640	4	IC,DIGITAL,74HCT85	U77-80
330-04644	1	IC,DIGITAL,MC1648	U110
330-04672	6	IC,DIGITAL,74HC595	U59,60,73,74,87,88
330-04673	12	IC,DIGITAL,74HC597	U55-58,69-72,83-86
330-04674	1	IC,DIGITAL,74HC4538	U45
330-04676	3	IC,DIGITAL,74F161A	U107-109
330-04677	1	IC,DIGITAL,74F253	U105
330-04892	1	IC,DIGITAL,74HCT74,RCA	U8
330-04926	1	IC,DIGITAL,74HC08	U101
INTERFACE IC			
345-03207	2	IC,INTER,uA9638,LINE DRVR	U1,2
345-03208	2	IC,INTER,uA9637A,LINE RCVR	U3,4
MEMORY IC			
350-04282	1	IC,SRAM,4364,8KX8,150NS,LPS	U38
350-04708	1	IC,PAL,16P8A,M480L,DTACK	U23
350-04709	1	IC,PAL,16P8A,M480L,MEM,V2.10	U24
350-04710	1	IC,SRAM,43256,150NS,LPS	U39
350-04867	1	IC,ROM,27C64,M480L,HOST,V1.00	U68
350-04920	1	IC,ROM,27512,M480L,V1.23-1	U40
350-04921	1	IC,ROM,27512,M480L,V1.23-2	U41
350-04922	1	IC,ROM,27512,M480L,V1.23-3	U42
MICROPROC IC			
365-04593	2	IC,uPROC,DUART,MC68681	U6,7
365-04594	1	IC,uPROC,MC68008	U34
CRYSTALS			
390-04595	1	CRYSTAL OSC,14.112 MHz	U93
390-04596	1	CRYSTAL OSC,15.360 MHz	U94
390-04597	1	CRYSTAL OSC,16.000 MHz	U18
390-04645	1	CRYSTAL,3.6864MHz	Y1
DSPLY/IND/LED			
430-04642	4	LED,T1,RED,RA BLOCK	CR1-4
BATTERIES			
460-04598	2	BATTERY,LITH,3V,FLAT	BT1,2
CABLE CONN			
490-02356	9	CONN,JUMPER,.1X025,2FCG	W9-11,13-15,17,18,20
PC EDGE CONN			
500-04557	2	CONN,EURO,C,ROW a+c,MALE,RA	P1,2
PC MNT CONN			
510-02671	10	CONN,POST,100X025,HDR,3MC,GOLD	W9-11,13-15,17,18,20; TP3
510-03922	1	CONN,POST,100X025,HDR,6MCG	TP4
510-03961	3	CONN,POST,100X025,HDR,2MCG	W1-3
510-04638	1	CONN,HDR,PCRA,30MC,LOK	J1

SOCKETS			
520-00946	2	IC SCKT,40 PIN,PC,LO-PRO	U6,7
520-01361	2	IC SCKT,20 PIN,PC,LO-PRO	U23,24
520-01458	7	IC SCKT,28 PIN,PC,LO-PRO	U38-43,68
520-04688	1	IC SCKT,48 PIN,PC,MACH,TIN	U34
KNOBS/CAPS			
550-04705	1	HANDLE,"U",1.5"	
ELECTRONIC HDWR			
600-01668	1	BUSS BAR,2C,.7X14,.3 OFF,PVF/N	
MACHINE SCREWS			
640-03713	2	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	HANDLE MTG
THREADLS FASTNR			
650-04772	3	POPRVT,1/8X3/16,REG PROT HD,AL	STFNR
BULK WIRE			
670-01974	1	WIRE,JMP,22AWG,0.1",NON-INSUL	W4
BRACKETS			
701-04523	1	BRACKET,STFNR,PC,.25X.44X9.65	

6.18 Power Supply Board

TRIM RESISTORS			
201-00424	2	RES,TRM,ST,PC,100 OHM,SA,CER	R5,11
CARBON FLM RES			
202-00501	2	RES,CF,5%,1/2W,150 OHM	R13,14
202-00505	3	RES,CF,5%,1/4W,10 OHM	R12,16,17
202-00510	2	RES,CF,5%,1/4W,51 OHM	R15,19
202-00531	1	RES,CF,5%,1/4W,1.5K OHM	R4
202-00542	2	RES,CF,5%,1/4W,4.7K OHM	R1,2
METAL FLM RES			
203-00464	1	RES,MF,1%,1/8W,4.99K OHM	R3
203-01996	4	RES,MF,1/2%,1/8W,3.01K OHM	R7-10
203-02655	1	RES,MF,1%,1/8W,6.04K OHM	R6
WIREWOUND RES			
204-04574	1	RES,WW,5%,7W,.02 OHM	R18
ELECTROLYT CAP			
240-01262	1	CAP,ELEC,330uF,25V,RAD	C12
240-03574	1	CAP,ELEC,3300uF,35V,RAD,LO-PRO	C13
240-04579	1	CAP,3300uF,63V,ELEC,LO PRO,RAD	C4
TANTALUM CAP			
241-00652	1	CAP,TANT,4.7uF,25V,RAD	C7

PCRB/PP CAP			
244-00660	1	CAP,MYL,.01uF,100V,10%,RAD	C1
244-00662	1	CAP,MYL,.1uF,5%,RAD	C2
244-01171	1	CAP,PP,5100pF,2.5%	C9
244-04901	1	CAP,MYL,.022uF,100V,10%,RAD	C8
CERAMIC CAP			
245-03609	6	CAP,CER,.1uF,50V,Z5U,AX	C3,6,10,14-16
245-03610	1	CAP,CER,.01uF,100V,Z5U,AX	C5
245-03868	1	CAP,CER,33pF,100V,COG,10%,AX	C11
INDUCTORS			
270-00779	1	FERRITE,BEAD	FB1
270-04592	1	INDUCTOR,SWITCHING,100uH,12A	L1
DIODES			
300-01029	1	DIODE,1N914 AND 4148	CR2
300-04580	1	DIODE,BRIDGE,10A,200V	CR1
300-04583	1	DIODE,SCHOTTKY,16A,MBR1645	CR4
300-04584	1	DIODE,ZENER,16V,1N4745A	CR3
300-04748	1	DIODE,ZENER,Z5.6,1%	CR5
TRANSISTORS			
310-01007	1	TRANSISTOR,2N3904	Q2
310-04581	1	XISTOR,MOSFET,12A,80V,PNP	Q1
SCR			
320-01013	1	TRANSISTOR,2N 6400-6401	U2
LINEAR IC			
340-04679	1	IC,LINEAR,SG3526,SW REG	U1
FUSES			
440-02680	1	FUSE,5X20MM,SLO-BLO,6.3AMP	F1
CABLE CONN			
490-04887	2	CONN,QDC,MALE,.250X.032	XFORMER WIRING
PC MNT CONN			
510-00826	1	CONN,POST,156X045,HDR,4MCG,LOK	P3 SYNC CONN
510-01481	1	CONN,POST,156X045,HDR,6MCG,LOK	P4 POWER CONN
510-03989	1	CONN,POST,156X045,HDR,2MCG,LOK	P1 FAN OR PILOT LIGHT CONN
CONN HDWR			
527-04889	2	CONN,HSG,QDC,MALE,.250X.032	XFORMER WIRING
ELECTRONIC HDWR			
600-02227	2	FUSE CLIP,20MM,PC	F1
INSUL/SPACRS			
630-00952	3	INSUL,SEMI,BUSHING,TO-220	CR4,Q1,U2 MTG
630-04658	1	INSUL,WSHR,SIL RUB,1ODX.255ID	L1
630-04659	3	INSUL,SEMI,SIL RUB,HP,TO-220	CR4,Q1,U2 MTG

SPCR,NON-INSUL			
635-01454	3	SPCR,SWAGE,6-32X5/8,1/4RD,BR/N	
MACHINE SCREWS			
640-04692	1	BOLT,10-32X1.5",HH,NYLON	L1
THRD-FORM SCRW			
641-04021	3	SCRW,TAP,SW,4-40X1/4,PNH,PH,ZN	CR4,Q1,U2 MTG
NUTS			
643-04693	1	NUT,10-32,HEX,NYL	L1
THREADLS FASTNR			
650-03970	2	POPRVT,1/8X1/8,REG PROT HD,SS	HEATSINK MTG
PRE-CUT WIRE			
675-02891	1	WIRE,18G,GRN,7",ST&T1/4X0	
675-02891	1	WIRE,18G,GRN,8",ST&T1/4X0	
BRACKETS			
701-04522	1	BRACKET,HEATSINK,"U",.75X.75X4	
PC BOARDS			
710-04513	1	PC BD,PWR SUPPLY BD,5V,12A	

6.19 V1.23 Software Update

CUST LITERATURE			
070-04987	1	INSTR,SOFT-UP,RETRO,V1.23,M480	
070-04988	1	NOTICE,SOFT RELEASE,V1.23,M480	
MEMORY IC			
350-04709	1	IC,PAL,16P8A,M480L,MEM,V2.10 for Rev. 1 Host	U24
350-05824	1	IC,PAL,16P8A,M480L,MEM,V.3.00 for Rev. 3 Host	
350-04920	1	IC,ROM,27512,M480L,V1.23-1	U40
350-04921	1	IC,ROM,27512,M480L,V1.23-2	U41
350-04922	1	IC,ROM,27512,M480L,V1.23-3	U42
TOOLS			
780-01925	1	TOOL,IC EXTRACTOR	

6.20 V. 2.00 Software Update

CUST LITERATURE			
070-06206	1	INSTR,SOFT-UP,RETRO,V2.00,M480	
070-04487	1	NOTICE,SOFT RELEASE,V2.00,M480	
MEMORY IC			
350-04710	1	IC,SRAM,43256,150NS,LPS for Rev. 1 Host	U24
350-06406	1	IC,ROM,27512,M480L,V.2.00-1	U40
350-06407	1	IC,ROM,27512,M480L,V2.00-2	U41
350-06408	1	IC,ROM,27512,M480L,V2.00-3	U42
350-06409	1	IC,ROM,27512,M480L,V2.00-4	U43
TOOLS			
780-01925	1	TOOL,IC EXTRACTOR	

6.21 SME Option

M480 SME BOARD

PART NO.	QTY	DESCRIPTION	REF.
CARBON FLM RES			
202-00505	9	RES,CF,5%,1/4W,10 OHM	R1,8-15
202-00525	2	RES,CF,5%,1/4W,510 OHM	R4,7
202-00529	1	RES,CF,5%,1/4W,1K OHM	R2
202-00549	3	RES,CF,5%,1/4W,10K OHM	R3,5,6
NETWORK RES			
205-05638	1	RES,NET,SIP,2%,10KX9	U114
205-05639	3	RES,NET,SIP,2%,330/470X8	U6,46,86
205-05834	1	RES,NET,SIP,2%,150X9	U166
ELECTROLYT CAP			
240-02048	1	CAP,ELEC,47uF,25V,AX	C88
CERAMIC CAP			
245-03609	42	CAP,CER,.1uF,50V,Z5U,AX	C1,2,21,58,77-87,89-115
245-05835	72	CAP,CER,.33uF,50V,Z5U,AX	C3-20,22-57,59-76

DIGITAL/CMOS IC			
330-00674	1	IC,DIGITAL,7438	U167
330-00698	1	IC,DIGITAL,74LS14	U179
330-00716	5	IC,DIGITAL,74LS283	U127-129,139,140
330-03340	9	IC,DIGITAL,74F157	U108,122,126,138,148,151,162 U172,175
330-03586	5	IC,DIGITAL,74HCT244	U25,65,101,106,113
330-03611	1	IC,DIGITAL,74HC273	U91
330-03715	12	IC,DIGITAL,74HCT374	U92-95,119,120,131,135, U137,143,144,152
330-04040	2	IC,DIGITAL,74F04	U133,164
330-04042	5	IC,DIGITAL,74AHCT374	U150,153,154,158,174
330-04084	1	IC,DIGITAL,74HCT175	U103
330-04291	5	IC,DIGITAL,74F244	U67,88,97,99,105
330-04292	4	IC,DIGITAL,74F32	U130,132,145,146
330-04293	2	IC,DIGITAL,74F74	U177,U134
330-04294	4	IC,DIGITAL,74HCT138	U27,104,107,168
330-04511	2	IC,DIGITAL,74AHCT244	U160,170
330-04564	3	IC,DIGITAL,74HCT08	U112,147,181
330-04567	2	IC,DIGITAL,74HCT32	U121,163
330-04572	1	IC,DIGITAL,74HCT245	U87
330-04676	2	IC,DIGITAL,74F161A	U161,171
330-04758	1	IC,DIGITAL,74LS05	U124
330-04892	6	IC,DIGITAL,74HCT74,RCA	U123,136,142,165,176,180
330-05836	4	IC,DIGITAL,74AHCT373	U89,98,159,169
330-05837	3	IC,DIGITAL,74HCT646	U90,96,100
330-05838	3	IC,DIGITAL,74LS590	U109-111
330-05839	3	IC,DIGITAL,74LS592	U1-3
330-05840	1	IC,DIGITAL,uPD71071,DMA CTL	U155
330-05931	2	IC,DIGITAL,74F139	U4,5
MEMORY IC			
350-04655	2	IC,SRAM,2018,2KX8,35NS	U149,173
350-05825	72	IC,DRAM,256KX1,120NS,DIP	U7-24,28-45,47-64,68-85
350-05841	1	IC,SRAM,43256,100NS	U26
350-06214	1	IC,PAL,16P8A,M480SME,MEM,V1.00	U102
350-06215	1	IC,PAL,16R8A,M480SME,CLK,V1.00	U125
350-06216	1	IC,PAL,16R8A,M480SME,RAM,V1.00	U178
MICROPROC IC			
365-05842	1	IC,uPROC,Z80,CMOS,8MHz	U66
CABLE CONN			
490-02356	7	CONN,JUMPER,.1X025,2FCG	W3,6,12-15,22
PC EDGE CONN			
500-04557	2	CONN,EURO,C,ROW a+c,MALE,RA	P1,2
PC MNT CONN			
510-03961	20	CONN,POST,100X025,HDR,2MCG	W1-6,10-23

SOCKETS			
520-00942	1	IC SCKT,14 PIN,PC,LO-PRO	U177
520-00943	72	IC SCKT,16 PIN,PC,LO-PRO	U7-24,28-45,47-64,68-85
520-00946	1	IC SCKT,40 PIN,PC,LO-PRO	U66
520-01361	3	IC SCKT,20 PIN,PC,LO-PRO	U102,125,178
520-01458	1	IC SCKT,28 PIN,PC,LO-PRO	U26
520-04425	2	IC SCKT,24 PINX.3",PC,LO-PRO	U149,173
520-04688	1	IC SCKT,48 PIN,PC,MACH,TIN	U155
KNOBS/CAPS			
550-04705	1	HANDLE,"U",1.5"	
MACHINE SCREWS			
640-03713	2	SCRW,6-32X1/4,PNH,PH,SEMS,ZN	
THREADLS FASTNR			
650-04772	2	POPRVT,1/8X3/16,REG PROT HD,AL	STFNR
BRACKETS			
701-05843	1	BRACKET,STFNR,PC,.25X.44X8.25	
PC BOARDS			
710-05816	1	PC BD,SME BD,M480L	
PLASTICS			
720-02751	1	TAPE,FOAM,DBL-STK,1/8THX3/4W	

M480 SME FLOPPY OPTION

PART NO.	QTY	DESCRIPTION	REF.
CERAMIC CAP			
245-00585	2	CAP,CER,18pF,50V,10%	C116,117
DIGITAL/CMOS IC			
330-05779	1	IC,DIGITAL,74F240	U157
INTERFACE IC			
345-05845	1	IC,INTER,82072,FLOP CTL	U156
CRYSTALS			
390-05847	1	CRYSTAL,24.000 MHZ	Y1
PC MNT CONN			
510-05848	1	CONN,POST,100X025,HDR,34MC,PCR	J1
SOCKETS			
520-00946	1	IC SCKT,40 PIN,PC,LO-PRO	U156

M480 SME SCSI OPTION

PART NO.	QTY	DESCRIPTION	REF.
CARBON FLM RES			
202-00549	1	RES,CF,5%,1/4W,10K OHM	R16
NETWORK RES			
205-05638	1	RES,NET,SIP,2%,10KX9	U182
205-05844	3	RES,NET,SIP,2%,220/330X8	U116-118
INTERFACE IC			
345-05846	1	IC,INTER,5380,SCSI	U115
PC MNT CONN			
510-02692	1	CONN,POST,100X025,HDR,50MC,PCR	J1
SOCKETS			
520-00946	1	IC SCKT,40 PIN,PC,LO-PRO	U115

M480 SME SHIPPING KIT

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-06333	1	INSTR,UPDATE,SME,M480L	
070-06405	1	NOTICE,SOFT REL,V2.00/SME,M480	
SHIPPING MAT			
730-01926	1	BAG,PINK,ANTI-STAT,15X18	
730-06217	1	BOX,PP TOP,LOCK END,16X16X3	
730-06218	1	INSERT,FOAM,16X16X3	
730-06411	1	BAG,CONDUCTIVE,15X18X.004	
LABEL/NAMEPLTS			
740-03170	1	LABEL,CAUTION STATIC SENSITIVE	