Service Manual

LXP-15

Multi-Effects Processor

lexicon

Precautions

The LXP-15 is a rugged device with extensive electronic protection. However, you should observe the same reasonable precautions that apply to any piece of audio equipment:

- Always use the correct line voltage.
- Don't install the LXP-15 in a closed, unventilated rack, or directly above heat-producing equipment such as power amplifiers.
- Never attach audio power amplifier outputs (speaker outputs) directly to any of the LXP-15's connectors.
- To prevent fire or shock hazard, do not expose the LXP-15 to rain or moisture.

Notice

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class A computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to identify and Resolve Radio/TV Interference Problems."

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure... voltage that may be sufficient to constitute a risk of shock.

This triangle, which appears on your component, alerts you to important operating and maintenance instructions in this accompanying literature.

3 Oak Park Drive
Bedford MA 01730 USA
617-280-0300
Customer Service Fax: 617-280-0499

Lexicon Part # 070-07832 Rev 1

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Table of Contents

1

Controls and Connectors

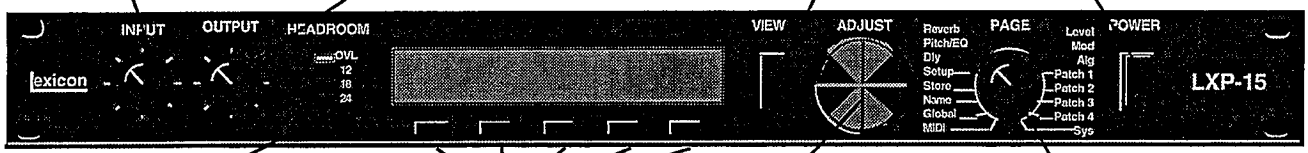
LXP-15
Front Panel
Controls

Input
Sets the audio input level.

Output
Controls the signal level sent to the LXP-15 outputs.

View
Used to display alternate screen information.

POWER
Power on/off.



Headroom
Green LEDs indicate signal present; red LED indicates the signal is -3dB from peak overload, or at processor overload.

Soft buttons
Each of these five buttons is used for assigning the parameter displayed directly above it to ADJUST knob control.

Adjust
Soft knob used to edit parmaters displayed and selected with the Soft buttons.

Page knob
Used for selection of 16 display pages.

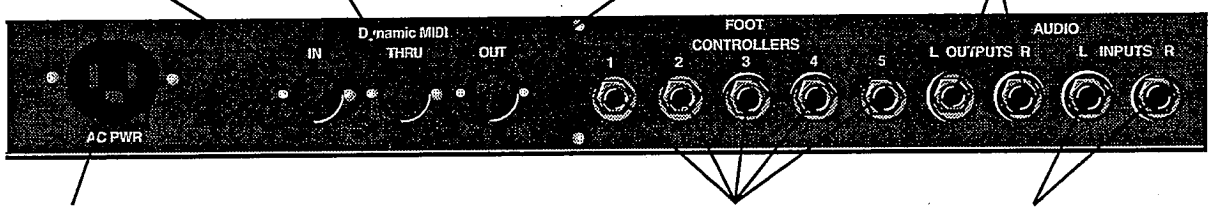
LXP-15 Rear Panel Connections

MIDI IN
Receives MIDI information from other MIDI equipment such as master keyboard controllers, MIDI foot controllers, sequencers and synthesizers.

MIDI THRU
Passes any MIDI data received without change.

MIDI OUT
Transmits MIDI data to other equipment.

Outputs (L and R)
Single-ended (unbalanced) stereo outputs provide +4dBu nominal output level. Either can be used for mono output.



AC Power

Foot Controllers
Five connectors for toggle (Push on/push off) momentary contact foot switches, or continuous footpedals (50 kΩ).

Inputs (L and R)
Single-ended (unbalanced) inputs accept levels to -26dBu. Input impedance is 50 kΩ in stereo, 25 kΩ in mono. Either can be used for mono input.

Power

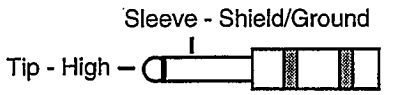
Connect the appropriate end of the LXP-15 line cord to the LXP-15 power connector, and the cable end to an AC wall socket.

Audio Cabling

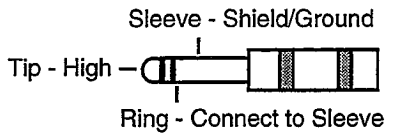
Under most conditions, cables which have a single conductor and a shield are adequate to connect the audio inputs and outputs of the LXP-15 to other equipment.

However, to insure the best performance, especially under high EMI (Electrical Magnetic Interference) conditions, cables with a twisted pair and separate shield are recommended. When using this type of cable, connect one of the twisted pairs to the tip of the phone jack, the other to the sleeve. (Be sure to connect the shield at one end only.) The shield should be connected at the input jack of the LXP-15 for input cables, and at the input of the piece of equipment connected to the LXP-15 output jack.

A tip/sleeve phone jack is recommended for the audio connections.



A tip/ring/sleeve jack may also be used. Just be sure to short the ring and sleeve.



Periodic Maintenance

Under normal conditions the LXP-15 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners.

Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the LXP-15 exterior.

Obtaining Factory Parts and Service

Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon Inc.
3 Oak Park Drive
Bedford MA 01730
Telephone: 617-788-0499
Fax: 617-891-0340

ATT: Customer Service

Returning units for service

Before returning a unit, consult with Lexicon to determine the extent of the problem. No equipment will be accepted without Return Authorization from Lexicon.

If you choose to return an LXP-15 to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Description of the problem
- Return Authorization #, both inside and outside of package
- Preferred method of return shipment

Please include a brief note describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, etc. with the unit unkless specifically requested to do so by Lexicon Service personnel.

2

Performance Verification

Performance Verification

Inspect the unit for any obvious signs of physical damage. Verify that all pots, switches, and the 16-position rotary switches operate smoothly and correctly. (Refer to the LXP-15 Owner's Manual for detailed explanations of functionality.) Verify that all screws and rear panel jacks are secure, and inspect the AC power cable for any signs of physical damage.

Front Panel Diagnostics

Power on the LXP-15 while holding in the VIEW button on the front panel of the unit. When VIEW is released, the LXP-15 will enter Diagnostic Mode and will be awaiting the selection of a diagnostic test.

Diagnostic test programs are selected by turning the ADJUST knob. Once a diagnostic test has been selected, the program is activated by pressing and releasing the VIEW button.

Generally, a test is performed once and the results are displayed upon completion of the test. Unless noted otherwise in the test descriptions, successful completion of a diagnostic test is indicated by the message "Passed" in the upper right corner of the display. Failure is indicated by the message "Failed".

On the following page is a list of the available diagnostic tests.

Using the Diagnostic Tests

The LXP-15 diagnostic tests are designed to facilitate the "process of elimination" technique of troubleshooting, but running a single diagnostic test will not always sufficiently isolate a hardware failure. Although related tests are indicated in each test description, it is recommended that the appropriate section of Chapter 3: Circuit Description be read to maximize the usefulness of the diagnostic tests. Chapter 3 also contains a reference glossary of signal and bus abbreviations.

For example: a unit is behaving in an inconsistent manner and Diagnostic tests are run to isolate possible hardware problems. *Master RAM test* is run and passes. *Master All RAM test* runs and fails. The diagnostic description of *Master All RAM test* states that the test checks all Master Processor addressable memory. In Chapter 3: Circuit Description: Memory, it is noted that the Master Processor can address all of the Slave RAM and the WCS located in the Lexichip-1.

Because the *Master RAM test* passed, you can assume that the Master RAM (U17) is functioning properly, and the problem must be in the Slave RAM or WCS. *Slave RAM, Shared RAM, Slave WCS* and *Master WCS* tests should be performed.

1. If *Shared RAM* and *Slave RAM tests* both fail, the Slave RAM is suspect.
2. If *Shared RAM test* and *Master WCS tests* fail, the Master/Slave interface circuitry is suspect. Running further diagnostics which exercise the Master Processor's access to the slave bus will verify this. (*Slave Communications test,* and *Slave Interrupt.*)
3. If both *Master* and *Slave WCS tests* fail, the Lexichip-1 is probably faulty.

Diagnostic Test Programs

The diagnostics for the LXP-15 are invoked on power up by holding down the VIEW button. The operator selects the desired diagnostic by turning the ADJUST knob and pressing VIEW when the desired test is displayed on the LCD display.

When a test has been run, an error condition is signaled by the illumination of the red overload LED for approximately half a second and a message on the display (if possible). A pass condition is signaled by the illumination of the bottom green LED for approximately half a second and a Passed message on the display (if possible).

Following is a list of the available diagnostics:

1. Pre burn in Test
2. Switch Test
3. Direct Audio Test
4. Processed Audio Test
5. ADC Test (factory only)
6. Go To System
7. Post Burn in Test
8. ADC Monitor
9. Bank Test
10. Base ROM Test
11. Bank A ROM Test
12. Bank B ROM Test
13. All ROM Test
14. Master RAM Test
15. Shared RAM Test
16. Master WCS Test
17. Master All RAM Test
18. Clear All RAM
19. Interrupt Test
20. MIDI Test
21. Non-Volatile Memory Test
22. Non-Volatile Test Init
23. Audio DRAM Test
24. Go to System (skip Diagnostics)
25. Slave Reset
26. Slave Communications Test
27. Slave RAM Test
28. Slave WCS Test
29. All Slave Tests
30. Display Contrast
31. Display Brightness
32. Display Test
33. Repeating Test

Power Up Diagnostics

Upon normal power up, the LXP-15 automatically runs the following sequence of diagnostic tests:

Display Test
Bank Test
All ROM Test
All Master RAM Test
Interrupt Test
All Slave Tests

Each of the 33 diagnostic tests is described on the following pages.

1. Pre burn in Test, incl Clear RAM

This test consists of a series of tests which are run sequentially when the test is invoked. The test is typically used to verify the basic operationality of units which are being powered up for the first time, and to initialize the non-volatile RAM. Pressing VIEW while the Pre burn in Test is selected, will cause the following sequence of tests to be run:

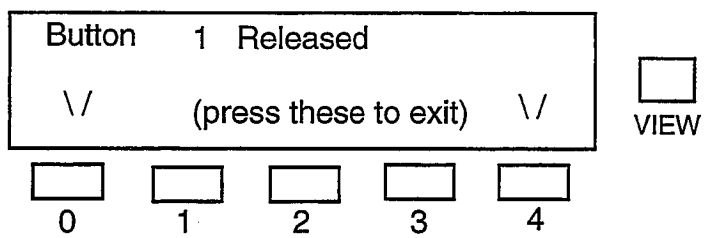
Display Test
Bank Switch Test
All ROM Test
All Master RAM Test
Interrupt Test
MIDI Test (requires MIDI cable to be connected from LXP-15 MIDI IN to MIDI OUT)
All Slave Tests
Clear RAM (clears all registers)
Non-Volatile Test init
DRAM Test

Each test is run once with the sequence halting on any tests that fail. Note that this sequence runs the Non-Volatile Test init which stores a specific pattern of data in the RAM. This data is later checked for corruption by the Post burn in test. Note also that a MIDI cable must be connected from MIDI IN to MIDI OUT for the unit to pass the MIDI test.

2. Switch Test

This test allows the operator to verify the operation of most of the controls on the front panel. When invoked, the test displays the name of each switch or rotary control being pressed or turned (with the exception of the Input and Output Level pots and the Power switch). While a switch is pressed, the switch number, and the word "Pressed" are displayed; when the switch is released, the word "Released" is displayed. The rotary controls display the position of the control in hex (0-F). (Note that as the ADJUST or PAGE knob is turned clockwise, the hex number increments; the number decrements when the knob is turned counter clockwise.)

The last switch or control touched remains displayed until another control is tested, or until the test is exited. To exit the test the operator must simultaneously press buttons 0 and 4.



The following table outlines the PAGE knob positions with their displayed values and the hex/binary data values generated by the encoder (SW7) at the input to U42:

Page Postiton	Display	Hex	U42 pin 2	3	4	5
Setup	0	8	1	0	0	0
Dly	1	A	1	0	1	0
Pitch/EQ	2	B	1	0	1	1
Reverb	3	3	0	0	1	1
Level	4	2	0	0	1	0
Mod	5	0	0	0	0	0
Alg	6	1	0	0	0	1
Patch 1	7	5	0	1	0	1
Patch 2	8	4	0	1	0	0
Patch 3	9	6	0	1	1	0
Patch 4	A	7	0	1	1	1
Sys	B	F	1	1	1	1
MIDI	C	E	1	1	1	0
Global	D	C	1	1	0	0
Name	E	D	1	1	0	1
Store	F	9	1	0	0	1

The following table outlines the displayed values and the hex/binary data value generated by the ADJUST encoder (SW6) at the input to U42:

Display	Hex	U42 pin 6	7	8	9
0	8	1	0	0	0
1	A	1	0	1	0
2	B	1	0	1	1
3	3	0	0	1	1
4	2	0	0	1	0
5	0	0	0	0	0
6	1	0	0	0	1
7	5	0	1	0	1
8	4	0	1	0	0
9	6	0	1	1	0
A	7	0	1	1	1
B	F	1	1	1	1
C	E	1	1	1	0
D	C	1	1	0	0
E	D	1	1	0	1
F	9	1	0	0	1

3. Direct Audio Test

The Direct Audio Test sets the audio path through the LXP-15 for 100% dry, allowing no processed audio to be mixed with the signal. The system accomplishes this by setting the A portion of the MDACs (U12 and 14) completely off (00) and allowing the operator to write a value to the B portion (ADJUST Level = nn). From the operator's perspective this is like a second output level control set by the ADJUST knob. The resulting gain is adjustable in increments of 6dB from 01 to 09, with 03 being unity gain through the unit (both Input and Output Level pots fully clockwise). The following table shows the data sent to the MDACs and the output signal level for each level setting: (Input a 1kHz sine wave at -25dBv.)

"Level"	Output Level	Hex	Binary 76543210 - data bits
00	-40dBv	00	00000000
01	-35dBv	01	00000001
02	-31dBv	02	00000010
03	-25dBv	04	00000100
04	-19dBv	08	00001000
05	-13dBv	10	00010000
06	-7dBv	20	00100000
07	-1dBv	40	01000000
08	+5dBv	80	10000000
09	+11dBv	FF	11111111

NOTE: The actual output level may vary ±1dBv for all Level settings—except for 00 and 01 which may vary as much as ±2dBv.

4. Processed Audio Test

The Processed Audio Test sets the audio path through the LXP-15 for 100% wet, allowing no dry audio to be mixed with the signal. The system accomplishes this by setting the B portion of the MDACs (U12 and 14) completely off (00) and allowing the operator to write a value to the A portion (ADJUST Level = nn). From the operator's perspective this is like a second output level control which is set by the ADJUST knob. The resulting gain is adjustable in increments of 6dB from 01 to 09, with 03 being approximately unity gain through the unit (both Input and Output Level pots fully clockwise and signal being applied to both inputs). The following table shows the data sent to the MDACs and the output signal level for each level setting: (Input a 1kHz sine wave at -25dBv.)

"Level "	Output Level	Hex	Binary 76543210 - data bits
00	-40dBv	00	00000000
01	-35dBv	01	00000001
02	-31dBv	02	00000010
03	-25dBv	04	00000100
04	-19dBv	08	00001000
05	-13dBv	10	00010000
06	-7dBv	20	00100000
07	-1dBv	40	01000000
08	+5dBv	80	10000000
09	+11dBv	FF	11111111

NOTE: The actual output level may vary ±1dBv for all Level settings except for 00 and 01 which may vary as much as ±2dBv.

Using the Processed Audio Test and the Direct Audio Test, the technician can eliminate major functional sections of the system when troubleshooting distortion problems in a system. (i.e. distortion in the Processed Audio Test only implies that the input and output circuitry of the system are operating properly and that the + and - 15V supplies are probably good. Concentrate on the circuitry related to processed audio only.)

5. ADC Test (factory only)

This is for factory testing only. Refer to the *ADC Monitor Test* on the following page.

6. Go To System

This selection runs the normal power up diagnostic sequence (shown below) and leaves the unit in the normal operating system. It is essentially the same as power cycling the unit.

Display Test
Bank Test
All ROM Test
Master All RAM Test
Interrupt Test
All Slave Tests

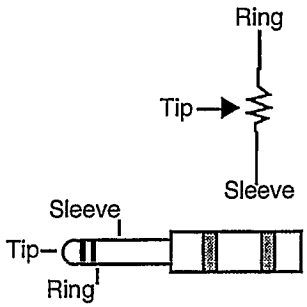
7. Post burn in Test

This test, like the Pre burn in test, is actually a series of tests which are run sequentially when the test is invoked. The test is used on units which have already had the Pre burn in Test run, and which have completed their burn in cycle. Pressing VIEW when the Post burn in Test is selected causes the following tests to be run:

Display Test
Bank Switch Test
All ROM Test
All Master RAM Test
Non-Volatility Test
Interrupt Test
MIDI Test
All Slave Tests
DRAM Test

Each test is run once with the sequence halting on any tests that fail. Note that the sequence runs the Non-Volatility Test which checks the data stored during the Non-Volatile Test init for data corruption. If that test has not been run, either by itself or as part of the Pre burn in Test, this test will fail.

8. ADC Monitor



The ADC Monitor test gives the operator a direct display of the values being generated by the ADC chip (U26) to represent the analog signals at its inputs. These signals consist of the 5 CONTROLLER INPUTS available on the rear panel of the unit (AN0-4), a battery voltage checking signal (AN5) and a headroom signal (AN6). The values are displayed in hex from 00 to 7F with each input being assigned a seperate field on the display. The fields are assigned to the inputs from left to right as follows:

CONTROLLER INPUT 1	0V = 00, 5V = 7F
CONTROLLER INPUT 2	0V = 00, 5V = 7F
CONTROLLER INPUT 3	0V = 00, 5V = 7F
CONTROLLER INPUT 4	0V = 00, 5V = 7F
CONTROLLER INPUT 5	0V = 00, 5V = 7F
Battery Check	Bat V >2.5V = 00, Bat V <2.5V = 7F
Signal Headroom	approx. -45dBV = 00, approx. -16dBV = 7F *

* @1kHz with Input Level pot fully clockwise.

9. Bank Test

The Bank Test verifies that the bank switching in the Master processor is working properly by checking for a short message in each of the banks in the ROM (U45).

10. Base ROM Test

This test preforms a checksum on the base ROM in the system and compares the total with a predetermined value stored in the base ROM itself. Note that the base ROM consists of the first 1k (400 Hex) of both banks of the master ROM (U45) with identical data in both banks.

11. Bank A ROM Test

This test performs a checksum on the upper half of the ROM and compares the total with a predetermined value stored in the base ROM.

12. Bank B ROM Test

This test performs a checksum on the lower half of the ROM and compares the total with a predetermined value stored in the base ROM.

13. All ROM Test

This test performs a checksum on the entire ROM (U45) and compares the total with a predetermined value stored in the base ROM.

14. Master RAM Test

This test is a standard memory test that writes a unique address into each memory location, except for the non-volatile area. The data is then read back to verify that it is correct. The procedure is repeated with fixed values of 55, AA, FF and 00. The memory is left filled with 00 in each loaction when the test is complete. Any problems with the Master Processors RAMs (U43,44) should be detected by this test.

15. Shared RAM Test

This is a test run by the Master processor on the Slave's RAM (U49). This test is a standard memory test that writes a unique address into each memory location. The data is then read back to verify that it is correct. The procedure is repeated with fixed values of 55, AA, FF and 00. The memory is left filled with 00 in each loaction when the test is complete. Any problems with the Slave Processor RAM (U49) or the Master processor's communication with it should be detected by this test. Because the Master processor communicates with the Slave processor through its RAM, problems here must be solved before any Slave tests will have any meaning.

16. Master WCS Test

This simultaneously tests the Master processor communications with the Lexichip-1 and the Lexichip-1 WCS (Writeable Control Store). This test is a standard memory test that writes a unique address into each memory location, except for the non-volatile area. The data is then read back to verify that it is correct. The procedure is repeated with fixed values of 55, AA, FF and 00. The memory is left filled with 00 in each loaction when the test is complete. Any problems with the Lexichip-1's WCS (RAM) or control from the Master Processor should be detected by this test.

17. Master All RAM Test

This test is a standard memory test that writes a unique address into each memory location, except for the non-volatile area. The data is then read back to verify that it is correct. The procedure is repeated with fixed values of 55, AA, FF and 00. The memory is left filled with 00 in each loaction when the test is complete. Any problems with the Slave Processor RAM (U49), the Master Processor RAM (U43,44), or the Lexichip-1 WCS should be detected by this test.

18. Clear All RAM (erases all registers)

This test runs a RAM test on the entire RAM area including the non-volatile area similar to the previous RAM tests. If the test passes, the presets are copied into the register storage area. When invoked, the test requires that the operator simultaneously press the leftmost and rightmost parameter buttons (0 and 4 as shown on Page 2-4) to acknowledge that you want to overwrite the non-volatile memory. If the Post Burn-in test is to be run on the system at some later date, the Non-Volatility init test must be run after this test.

19. Interrupt Test

The Interrupt Test checks the rate at which interrupts are received in the MINT/ line. Based on a 31.25kHz sampling rate, the MINT/ line at the output of the MIDI Interrupt circuit should be running at 3.472kHz, or one pulse every 288µs.

20. MIDI Test

This test transmits data out of the MIDI OUT jack and attempts to read the data back through the MIDI IN jack. To run this test a MIDI cable must be connected between the MIDI OUT jack and the MIDI IN jack. If the MIDI TEST JUMPER (W1C) is set for OUT (pins 2,3), this test can also be performed by connecting a MIDI cable from the MIDI THRU jack to the MIDI IN jack to test the THRU jack and it's associated circuitry.

21. Non-Volatile Memory Test This test is used in conjunction with the Non-volatile Test init to check the battery backup system in the unit as well as the static RAM's (U43,44) ability to retain data. This test checks the data left in the RAM by the init test and reports any inconsistencies.

22. Non-Volatile Test Init This test is used in conjunction with the Non-volatile Memory Test to check the battery backup system in the unit as well as the static RAM's (U43,44) ability to retain data. This test writes data into the RAM which will later be checked by the Non-Volatile Memory Test.

23. Audio DRAM Test (takes 25 seconds) This test puts the Lexichip-1 (U25) into a mode that allows the Master processor to read and write directly to the DRAM. To actually test the RAM, the Master processor performs two tests: a data test and an address test. During the data test the Master processor writes hex AAAAs (1010101010101010) into all of the memory locations then reads them back to check them. It repeats the process with 5555s (0101010101010101), FFFFs (1111111111111111) and 0000s (0000000000000000). For the address test, the Master processor writes a count into the memory then reads it back (i.e. 0000000000000001, 0000000000000010, 0000000000000011).

24. Go To System (Skip Diagnostics) This selection skips all diagnostics and immediately exits to the normal operating system.

25. Slave Reset Test In this test the Master Processor loads the Slave Processor with a program that instructs it to signal the Master when it has received a reset (SRST/). The Master issues a reset via its CONTROL PORT (U30) and waits for the slave to respond.

26. Slave Communications Test This test tries to verify that both the Master and Slave Processors can access the Slave's shared RAM (U49). Each processor writes to the RAM and the other tries to read it back.

27. Slave RAM Test In this test, the Master Processor loads a RAM test into the Slave Processor's memory then instructs the Slave to run the test and waits for the results. The Slave runs the RAM test and reports any errors back to the Master. The test itself is similar to the other RAM tests in which addresses 55, AA,FF and 00 are written into the RAM and then read back.

28. Slave WCS Test In this test, the Master Processor loads a Lexichip-1 WCS test into the Slave Processor which executes the test.

29. All Slave Tests This test simply executes tests 25-27 automatically and stops on the first test that fails.

30. Display Contrast

This test allows the operator to adjust the display contrast while in diagnostic mode. The following table shows the various displayed contrast settings along with the resulting binary/hex output from U60 pins 2, 5, 6 and 9:

	U60 Pins (binary)				(hex)
Display value	2	5	6	9	
00	1	1	1	1	F
01	1	1	1	0	E
02	1	1	0	1	D
03	1	1	0	0	C
04	1	0	1	1	B
05	1	0	1	0	A
06	1	0	0	1	9
07	1	0	0	0	8
08	0	1	1	1	7
09	0	1	1	0	6
0A	0	1	0	1	5
0B	0	1	0	0	4
0C	0	0	1	1	3
0D	0	0	1	0	2
0E	0	0	0	1	1
0F	0	0	0	0	0

31. Display Brightness

This test allows the operator to adjust the display brightness while in diagnostic mode. The following table shows the various displayed brightness settings along with the resulting binary/hex output from U60 pins 12, 15, 16 and 19 and the output frequency of U59 from pin 15:

	Pins (binary)				(hex)	
Display value	12	15	16	19		Freq
00	1	1	1	1	F	0Hz
01	1	1	1	0	E	15.64kHz
02	1	1	0	1	D	10.42kHz
03	1	1	0	0	C	7.82kHz
04	1	0	1	1	B	6.25kHz
05	1	0	1	0	A	5.21kHz
06	1	0	0	1	9	4.46kHz
07	1	0	0	0	8	3.91kHz
08	0	1	1	1	7	3.47kHz
09	0	1	1	0	6	3.12kHz
0A	0	1	0	1	5	2.84kHz
0B	0	1	0	0	4	2.60kHz
0C	0	0	1	1	3	2.40kHz
0D	0	0	1	0	2	2.23kHz
0E	0	0	0	1	1	2.08kHz
0F	0	0	0	0	0	1.95kHz

(Frequency tolerance: ±5%)

32 Repeating Test This test is similar to the Post Burn-In test, except that it will loop continuously until a failure is encountered. The following tests are run:

Display Test
Bank Switch Test
All ROM Test
All Master RAM Test
Non-volatility Test
Interrupt Test
MIDI Test
All Slave Tests
DRAM Test

To exit the test, hold down the VIEW button for an entire test cycle. (The unit monitors the button just before the Display test.) Alternatively, youy can force a test failure by unplugging the MIDI loop cable.

33 Display Test This test reads and writes to the registers in the LCD display. If no problems are found, all of the display characters are turned off, then on, and each headroom LED is lit one at a time.

Static Electricity Precautions

Many of the LXP-15's internal components are extremely sensitive to static electricity. The following practices minimize possible IC damage which can result from electrostatic discharge.

1. Don't handle ICs and boards any more than is necessary.
2. Discharge personal static by touching the LXP-15 mainframe before handling ICs or boards.
3. Handle each IC by its body.
4. Do not slide ICs or boards over a surface.
5. Avoid having plastic, vinyl or styrofoam in the work area.
6. Handle ICs only at a static-free workstation.
7. Use only grounded-tip soldering irons.
8. Use antistatic containers for handling and transport.

Clocks and Power Supply Measurements

Equipment Required

Variac
DMM
Frequency Counter (50MHz)
50 MHz Oscilloscope

Remove the top cover of the LXP-15. This requires removing seven screws (2 on each side, 2 on the top of the unit, and 1 on the rear).

1. Plug the LXP-15 power cable into the Variac and set output for nominal line voltage.

2. Set the DMM to measure VDC and check the regulated voltages for proper levels:

	Supply	Power	Ground	Specification
	+4.7vdc	U53.14	U53.7	(4.25-5.00)
	+15vdc	U61.3	U61.2	(14.25-15.75)
	-15vdc	U62.3	U62.1	(14.25-15.75)
	+5vdc	U63.3	U63.2	(4.75-5.25
CR8	+5.1vdc	Cathode	Anode	(5.61-4.59)
CR7	-5.1vdc	Anode	Cathode	(5.61-4.59)

3. Power off the LXP-15 and measure DC voltage across battery BAT1 with DMM; it should be 3.00 VDC or greater. If voltage is low, replace the battery.

   Note: Variac voltages assume the LXP-15 is configured for nominal voltage operation.

Brown Out / Power Down Test

1. Set oscilloscope for 2.5v/div (w/X10 probe) and a 1 mSec/div time base.

2. Connect scope probe to U53 pin 2.

3. Vary the Variac output level between 104VAC to 125VAC while monitoring U53 pin 2 on oscilloscope. This level should remain in a logical high condition (+5V).

4. Continue to monitor U53 pin 2 with oscilloscope and slowly reduce Variac output to 85 VAC. Pin 4 signal level should go to a logical low condition when the Variac output passes through the 100 - 85VAC range.

5. Return Variac to 120 VAC.

Clock Measurements

Using the frequency counter, measure the clock frequencies at the following points:

Signal Name	Location	Meas	Toleranc
ZCLK	U46 /pin 6	4MHz	±0.5%(3980000-4020000 Hz)
MIDICLK	U57 /pin 9	500kHz	±0.5% (497500 -502500 Hz)

Peformance Tests

Equipment Required

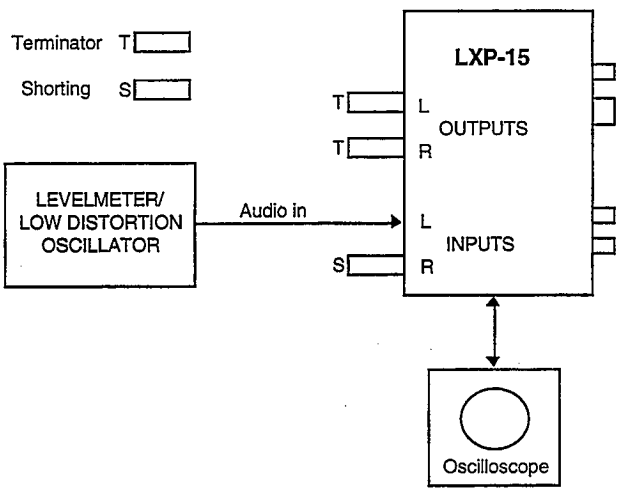
Low Distortion Oscillator	with single-ended 600 ohm output, <.005% THD.
THD+N Distortion Analyzer/Level Meter	with switchable 30kHz or audio bandpass filtering
Audio input cable	single-ended, shielded audio cable with 1/4" plug on one end and proper connector on other end to connect to Low Distortion Oscillator output
Audio output cable	single-ended, shielded audio cable w/ 1/4" plug on one end and the proper connectors on other ends to connect to THD+N Distortion Analyzer
Audio terminator plugs	two 1/4" plugs, each with a 100KΩ resistor attached between tip and sleeve
1/4" Shorting plug	with tip and sleeve shorted inside shielded casing

Audio Signal Tracing

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Program: *Direct Audio Test (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to left or right channel input
2. 1/4" shorting plug to unused channel input
3. Audio terminator plugs to left and right channel outputs



Procedure

1. Apply a 1kHz signal at -25dBV (159mVp/p) to left channel input for *Left Channel* connection, or to right channel input for *Right Channel* connection.

2. With an oscilloscope set to DC coupling, 2v/division sensitivity at 5mS/division sweep rate, trace audio signal as follows. Observe any excessive DC offset levels on any input or output stage, as this could indicate a supply or amp problem which would affect the audio signal.

3. Select the Direct Audio Test from the System Diagnostics. (Turn ADJUST and press VIEW once the test name is displayed.)

Analog Input Stage (U6)

	Signal Level	
	Left Channel	Right Channel
Left channel output (pin 1)	2.5Vp/p (2.4-2.6Vp/p)	No Signal
Right channel output (pin 7)	No Signal	2.5Vp/p (2.4-2.6Vp/p)

4. Turn Input Level Control fully counter clockwise

	Signal Level	
	Left Channel	Right Channel
Left channel input (pin 3)	No Signal	No Signal
Right channel input (pin 5)	No Signal	No Signal

Summing Amp (U3)

	Signal Level
Left and Right (pin 1)	2.5Vp/p 2.3-2.7Vp/p

5. Set Input Level fully clockwise

Pre-emphasis Stage (U3)

	Signal Level
Input (pin 5)	1.0Vp/p (0.9-1.1Vp/p)
Output (pin 7)	2.7Vp/p (2.6-2.8Vp/p)

Input Hold Stage (U1)

	Signal Level
Hold Input (pin 2)	Virtual Ground (No Signal)
Hold Output (pin 6)	2.7Vp/p staircase waveform (2.5 - 2.9Vp/p)

Comparator (U16)

	Signal Level
Input (pin 3)	2.7Vp/p staircase waveform (2.5 - 2.9Vp/p)

Output Hold Stage (U8)

	Signal Level
Left channel output (pin 7)	2.7Vp/p staircase waveform (2.5 - 2.9Vp/p)
Right channel output (pin 1)	2.7Vp/p staircase waveform (2.5 - 2.9Vp/p)

De-emphasis Stage (U11)

	Signal Level
Left channel input (pin 5)	1.15Vp/p (1.10 - 1.20Vp/p)
Right channel input (pin 3)	1.15Vp/p (1.10 - 1.20Vp/p)
Left channel output (pin 7)	2.25Vp/p (2.10 - 2.40Vp/p)
Right channel output (pin 1)	2.25Vp/p (2.10 - 2.40Vp/p)

Dry Mix Buffers (U5)

	Signal Level	
	Left Channel	Right Channel
Left channel (pin 1)	5Vp/p	No Signal
Right channel (pin 7)	No Signal (Both 4.75 - 5.25Vp/p)	5Vp/p

Mix Amps (U13) (Dry)

	Signal Level	
	Left Channel	Right Channel
Left channel (pin 1)	5Vp/p	No Signal
Right channel (pin 7)	No Signal (Both 4.75 - 5.25Vp/p)	5Vp/p

Output Stage (U15) (Dry)

	Signal Level	
	Left Channel	Right Channel
Left channel input (pin 3)	5.0Vp/p (4.75 - 5.25Vp/p)	No Signal
Right channel input (pin 5)	No Signal	5.0Vp/p (4.75 - 5.25Vp/p)
Left channel output (pin 1)	10.0Vp/p (9.5 - 10.5Vp/p)	No Signal
Right channel output (pin 7)	No Signal	10.0Vp/p (9.5 - 10.5Vp/p)

6. Select the *Processed Audio Test* diagnostic program.

Mix Amps (U13) (Wet)

	Signal Level
Left channel	2.25Vp/p (2.1 - 2.4Vp/p)
Right channel	2.25Vp/p (2.1 - 2.4Vp/p)

Output Stage (U15) (Wet)

	Signal Level
Left channel input (pin 3)	2.25Vp/p (2.1 - 2.4Vp/p)
Right channel input (pin 5)	2.25Vp/p (2.1 - 2.4Vp/p)
Left channel output (pin 1)	4.5Vp/p (4.2 - 4.8Vp/p)
Right channel output (pin 7)	4.5Vp/p (4.2 - 4.8Vp/p)

	Signal Level
Left channel (FB4)	4.5Vp/p (4.2 - 4.8Vp/p)
Right channel (FB3)	4.5Vp/p (4.2 - 4.8Vp/p)

Output Mute (either side of FB3 and 4)

7. Select the *Direct Audio Test* diagnostic program.

	Signal Level	
	Left Channel	Right Channel
Left channel (FB4)	10Vp/p (9.5 - 10.5Vp/p)	No Signal
Right channel (FB3)	No Signal	10Vp/p (9.5 - 10.5Vp/p)

8. Set Output Level Control fully counter clockwise

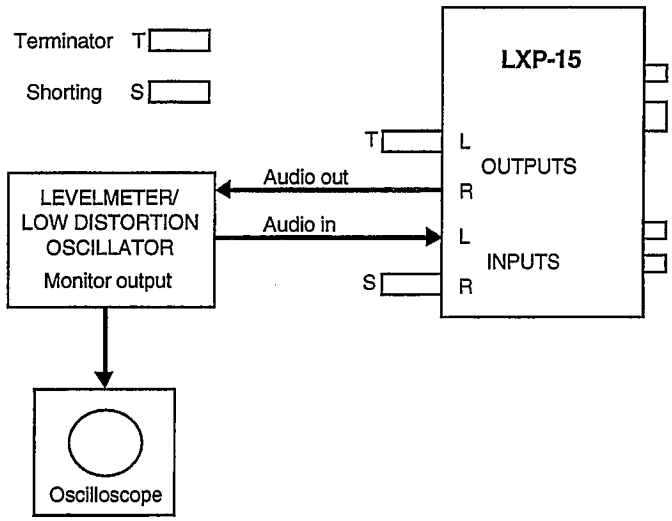
	Signal Level
Left Channel (FB4)	No Signal
Right channel (FB3)	No Signal

Inter-Channel Crosstalk Measurement

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Program: *Direct Audio Test (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to left channel input
2. 1/4" shorting plug to right channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 15 kHz signal at -20dBV (283mVp/p) to left channel input.

2. Measure Right channel output level . Acceptable level < -44dBV (1.78mVp/p).

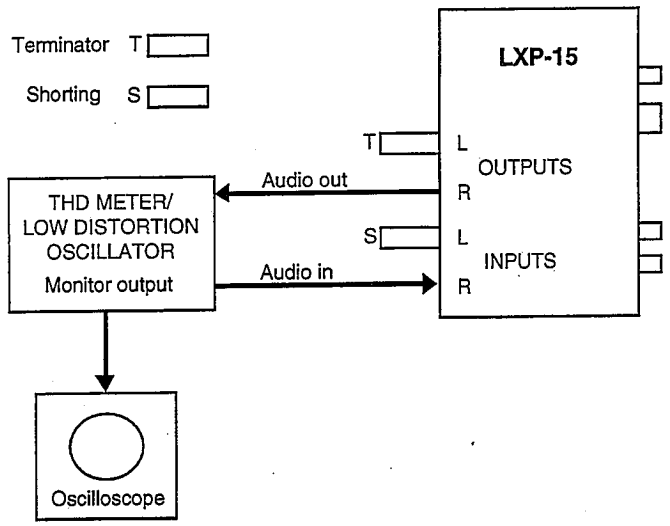
3. Swap all right and left channel audio connections and repeat steps 1 and 2 on left channel .

Dry (unprocessed) THD Measurement

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Program: *Direct Audio Test (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to THD+N Analyzer input
4. Audio terminator (100k) plug to left channel output



Procedure

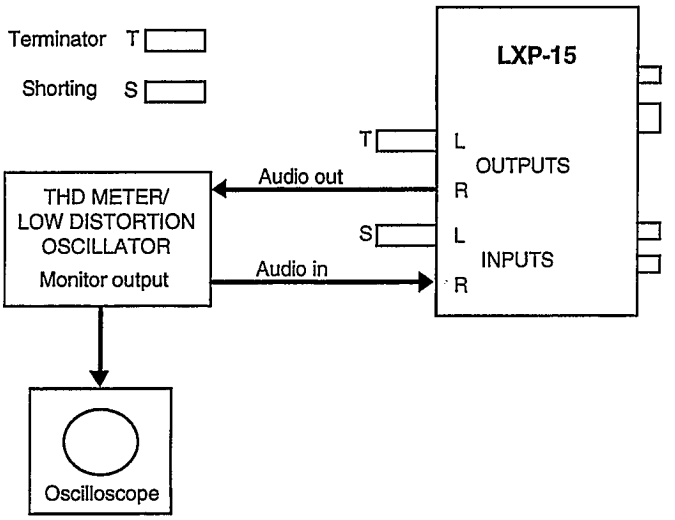
1. Apply a 1 kHz signal at -20dBV (283mVp/p) to right channel input.
2. Measure THD+N at right channel output.
3. 30kHz or audio bandpass filter on meter is ON. Acceptable reading will be <.01%.
4. Swap all right and left channel audio connections and repeat steps 1-3 on left channel.

Dry (unprocessed) Frequency Response

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Program: *Direct Audio Test (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -20dBV (283mVp/p) to right channel input. Set Level Meter to measure right channel output as the 0 dB reference.

2. Filters on meter are OFF.

3. Sweep from 20 Hz to 20kHz.

4. Right channel output should measure within ±0.1 dB (referenced to 1kHz output) over the range.

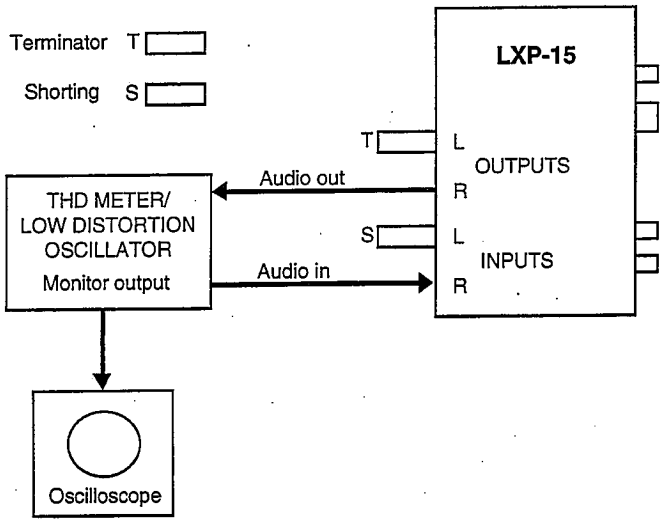
5. Swap right and left channel audio connections and repeat steps 1-4 on left channel.

Wet (processed) THD Measurement

Input Level: Fully clockwise to Maximum Level
Output Level: Fully clockwise to Maximum Level
Program: Processed Audio Test (See Diagnostic Tests)

Audio Connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to THD+N Analyzer input
4. Audio terminator (100k) plug to left channel output



Procedure

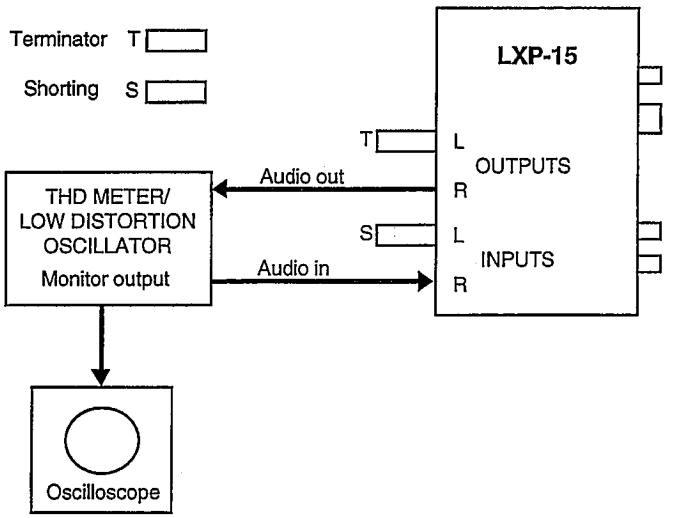
1. Apply a 1 kHz signal at -20dBV (283mVp/p) to right channel input.
2. Measure THD+N at right channel output.
3. THD meter has 30 kHz or audio bandpass filter ON. Acceptable reading will be < .02%.
4. Swap all right and left channel audio connections and repeat steps 1-3 on left channel.

Wet (processed) Frequency Response Measurement

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Program: *Processed Audio Test (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -25dBV (159mVp/p) to right channel input. Set Level Meter to measure the right channel output as the 0 dB reference.

2. Meter has 30 kHz or audio bandpass filter OFF.

3. Sweep from 20 Hz to 15kHz.

4. Right channel output should measure within +1.0 to -1.5 dB (referenced to1kHz output) over the range.

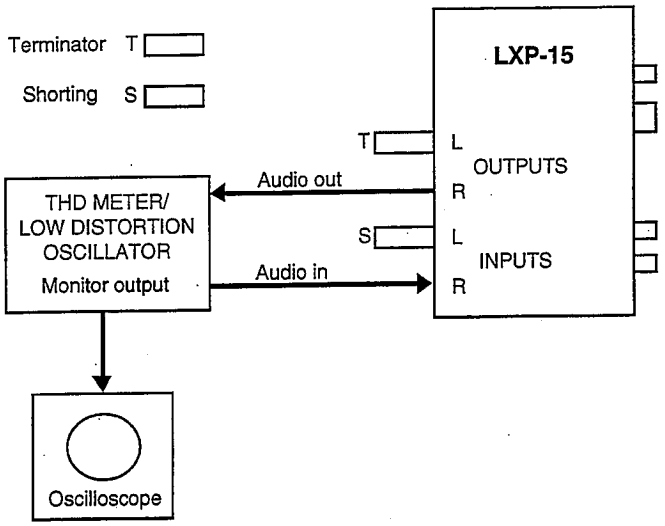
5. Swap right and left channel audio connections and repeat steps 1-4 on left channel.

Dynamic Range/ Signal to Noise

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Program: *Processed Audio Test (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -20dBV (283mVp/p) to right channel input. Set Level Meter to measure right channel output as the 0 dB reference.

2. Meter has 30 kHz or audio bandpass filter ON.

3. Unplug input to right channel. This will short out both right and left channel inputs.

4. Measure level on right channel output. Acceptable reading will be ≤ -75dB (referenced to 1kHz output level; typical reading will be about -85dB.)

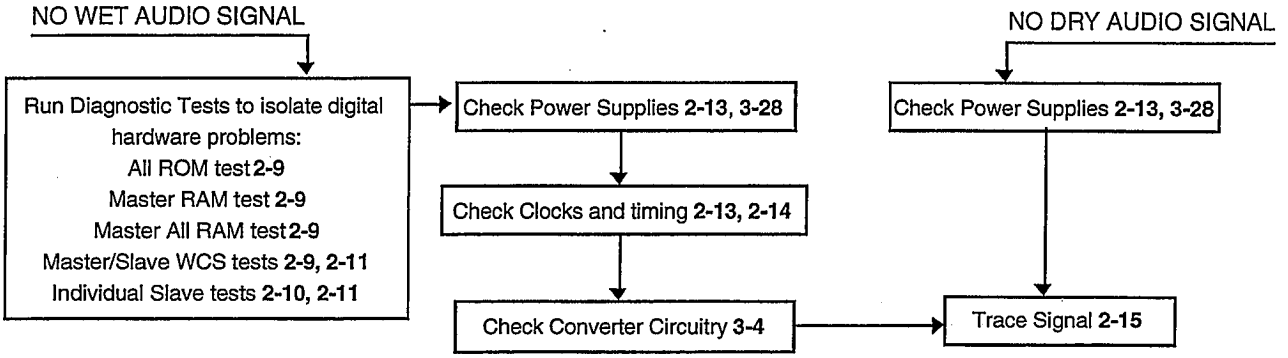
5. Swap right and left channel audio connections and repeat steps 1-4 on left channel.

Troubleshooting

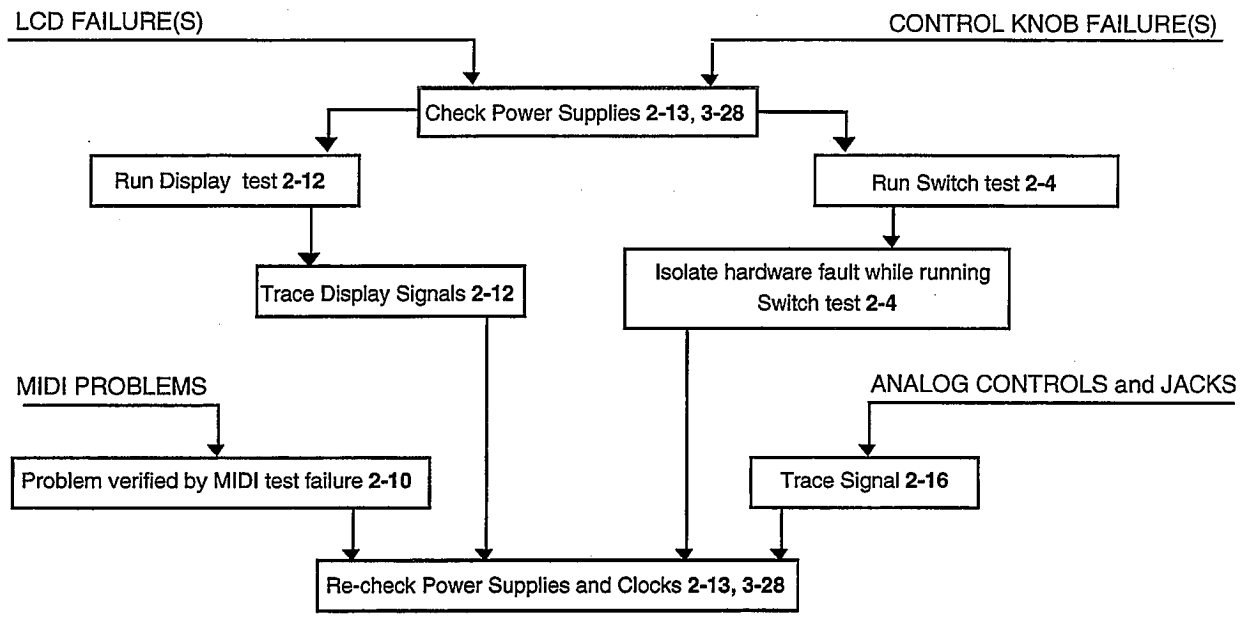
Since Diagnostic Tests can be performed without opening the unit they should generally be run first. This greatly reduces repair time, as a problem can be isolated to a specific circuit, even to a specific IC before opening the unit.

The following presents a diagrammatic version of the recommended troubleshooting procedure with page references.

AUDIO SIGNAL PROBLEMS



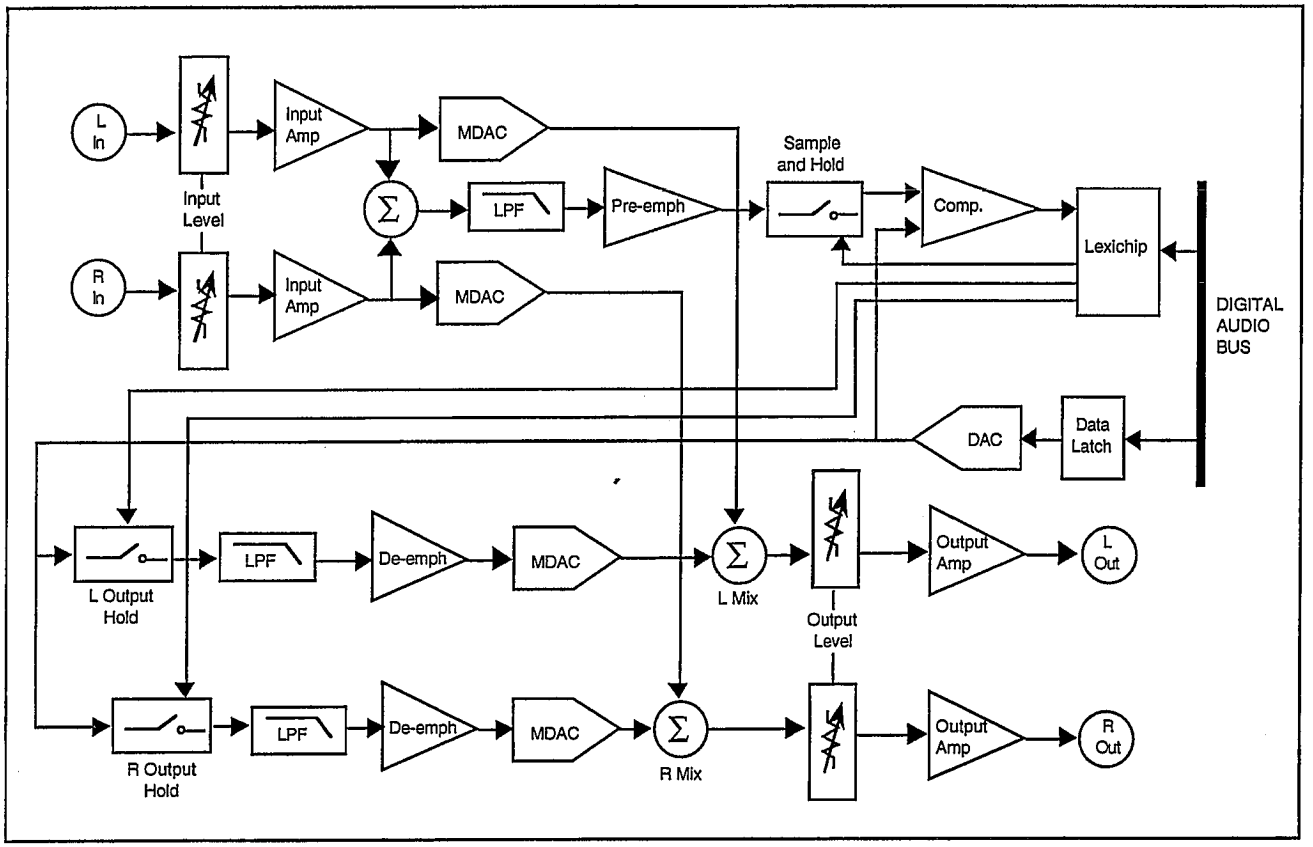
I/O PROBLEMS



3

Circuit Description

Analog Circuit Description



Analog Inputs

Input Jacks:	J2 (L)
	J1 (R)
Input RFI Filtering:	C2, FB2 (L)
	C1, FB1 (R)
Input DC Isolation:	C29 (L)
	C28 (R)
Input Level Pot:	R1 (located on front panel PC board)
Input Amp:	U6, R24 - R26, C24 (L)
	U6, R27 - R29, C27 (R)
L+R Summing Amp:	U3, R11 - R13, C12
Low Pass Filter:	U4, R14, R18, R19, C11

Separate unbalanced 1/4" phone jacks (J1 and J2) are provided for left and right input signals. A mono input source may be applied to either input jack, where it will be routed to both left and right channels.

Ferrite beads (FB1 and FB2) and capacitors (C1 and C2) are found at the inputs to prevent unwanted high frequency interference from entering or leaving the LXP-15 through the input cables. Additionally, a capacitor (C30) provides a path for high frequencies between input and output grounds.

DC isolation is incorporated by bipolar capacitors (C28 and C29) in line with the signal path. The left and right signals feed a dual potentiometer (R1) through a ribbon cable. This pot is located on the front panel printed circuit board where it controls the input signal level to the preamplifier stage. A dual op amp (U6) acts as the preamp and provides 24 dB of gain. This enables the LXP-15 to perform satisfactorily for nominal input levels as low as -26 dBu, where 0 dBu = 0.775 Vrms.

The left and right outputs of the preamp are applied to the Dry Mix buffers (U5) and to a summing amplifier (U3) through resistors R12 and R13. The summing amplifier provides 6 dB of gain by adding the left and right signals together. The output of U3 (pin 1) feeds a passive 7 pole 15 kHz low pass filter (U4, R19) through an AC coupling capacitor (C11) to eliminate any DC offset. Resistors R18 and R14 provide the correct input and output impedance for the filter. The output from the filter is passed on to the pre-emphasis stage.

Pre-Emphasis

Circuitry: U3, R15 - R17, C15, C17

A one-pole pre-emphasis curve is created by an op amp (U3), two resistors (R16 & R17) and a capacitor (C17). R15 determines the overall gain of the circuit (approx. 7 dB), while C15 provides high frequency compensation. The output, pin 7 of U3, drives the input hold and signal headroom circuits. The pre-emphasis offers no provisions for user calibration.

Signal Headroom

Circuitry: U2, R4 - R10, C7, C10, C16, CR1 - CR4

The output from the pre-emphasis stage passes through an AC coupling capacitor (C16) to resistors R5 and R9. One stage of dual op amp U2, combined with resistors R4 and R5 and diodes CR3 and CR4, produce a half-wave rectified signal with a gain of -2. The signal is applied to the other stage of U2 through resistor R8. This op amp sums the original signal (through R9) with the -2 gain half-wave rectified signal to produce a +1 gain full-wave signal. R10 determines the amplitude of the full-wave signal whereas C10 provides high frequency compensation. Diode CR2 and capacitor C7 act as a charge pump that provide a peak response to the audio signal being measured. R7 determines the rise time while R6 controls the fall time. A 5.1 volt zener diode (CR1) provides overload protection for the analog to digital converter's input. The signal headroom output feeds one of the eight inputs (at pin 4) of the analog to digital converter (U24) which converts the analog signal to an 8-bit digital word. After being read by the master processor, the results are transmitted by the master data bus (MDB) to a 74HCT273 latch (U27). Four outputs (HR0 - HR3) from U27 are applied to the base of transistors Q1 - Q4 through resistors R7 - R10 on the front panel board. These transistors drive four LEDs (CR3 - CR6) on a separate PC board that provide level indication.

Input Hold

Circuitry: U1, U7, R1 - R3, C3, C6

The sample and hold (SAH) circuitry consists of op amp (U1), an SPDT analog switch (U7) two resistors (R2 & R3) and a capacitor (C6). The SAH is controlled by the SAMP signal command from the Lexichip, which terminates at pin 11 of U7. When SAMP is high, pins 13 and 14 of switch U7 are shorted, and the sample function is performed. At this time, an output voltage from pin 6 of U1 charges C6. The hold function takes place when SAMP goes low, which shorts pins 12 and 14 of switch U7. The charge across C6 keeps the audio signal level constant during the analog to digital conversion. The output of the SAH passes through an AC coupling capacitor (C3) and a pulldown resistor (R1) to prevent DC offsets from affecting system performance.

The 74HC4053 analog switch (U7) requires +/- 5 volt power rails referenced to analog ground. +5.1 volts is created by connecting R40 and CR8 in series between +15 volts and analog ground. Similarly, -5.1 volts is produced by R41 and CR7 connected in series between -15 volts and analog ground. C35 thru C38 act as bypass capacitors.

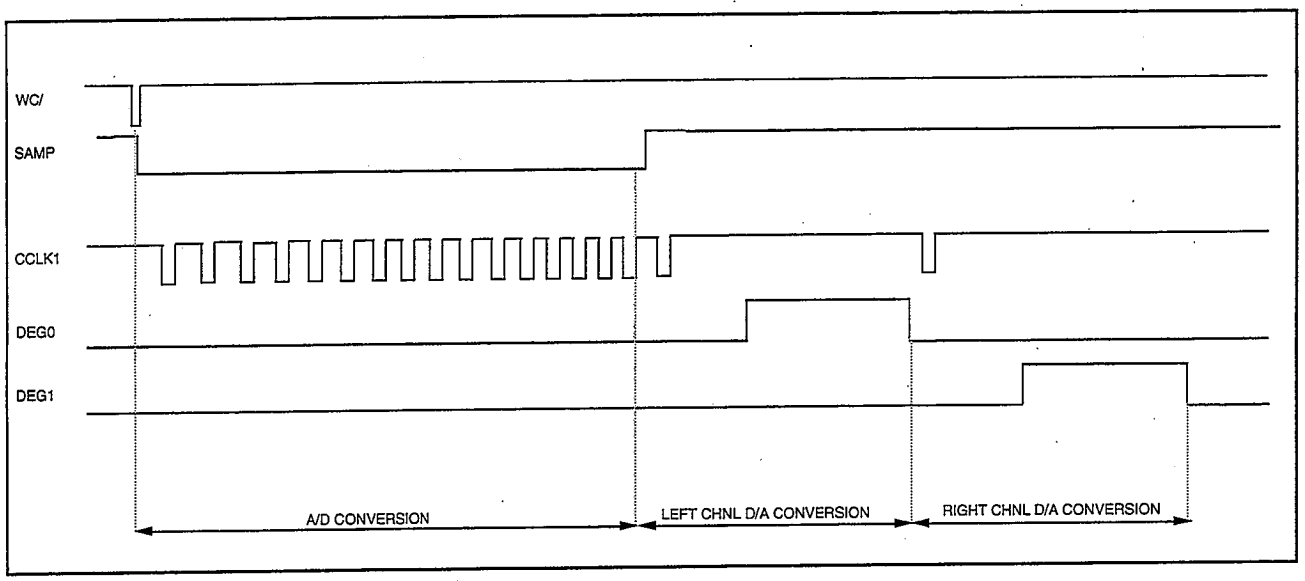
Converter

Digital to Analog Converter (DAC):	U17
Comparator:	U16
Lexichip-1:	U25
Digital Audio Bus (DAB) Latches:	U18, U19

The analog to digital conversion involves use of a comparator (U16), a 16-bit digital to analog converter (DAC, U17), the Lexichip (U25) and two 74HCT574 latches (U18, U19). The SAH output is applied to pin 3 of the comparator. The output of the DAC feeds pin 2 of the comparator. During the analog to digital conversion cycle, the internal successive approximation register (SAR) of the Lexichip-1 is used in conjunction with the DAC to output different voltage levels. These voltages are compared with the audio signal level. The conversion is completed when the two voltage levels are equal. After the conversion, the L+R signal is processed digitally.

After the signal has undergone digital processing, separate left and right analog signals reappear by the digital to analog conversion. At this time, the Lexichip-1 sends 16-bit data through the latches to the DAC, which converts it into analog voltage levels (see Data to Voltage chart below). These voltage levels are applied to the output hold circuitry.

Digital Input Code	Analog Output
0000h	+2.99991V
7FFFh	0.0000V
8000h	-91.6uV
FFFFh	-3.0000V



A/D SAR Conversion Timing

Left: U7, U8, R38, R39, C39
Right: U7, U8, R42, R43, C43
Low Pass Filters: U9, R44, R45, R48, C40 (L)
U10, R46, R47, R54, C44 (R)

Output Hold

Separate output hold circuits are provided for reconstructing the left and right processed audio signals. This circuitry includes a dual op amp (U8) and two analog switches (U7). DEG0 and DEG1 command signals from the Lexichip-1 terminate respectively at pins 10 and 9 of U7, providing separate control of the right and left output hold switches. During the digital to analog conversion cycle, either the DEG0 or DEG1 signal goes high when the DAC is ready to output the respective right or left analog voltage. This permits capacitors C39 or C43 to charge to the corresponding voltage level for the audio waveform. When the DEG0 or DEG1 signal goes low, the related capacitor will remain at the current signal level until the next conversion cycle.

The left and right signals from the output hold circuitry are applied to separate 7 pole passive 15 kHz filters (U9, R45 and U10, R47) through AC coupling capacitors C40 and C44. Resistors R44 and R46 provide the optimal input impedance for the filters. R48 and R54 appropriately terminate the outputs of the filters where the left and right signals are passed to the de-emphasis stages.

De-Emphasis

Left: U11, R49, R50, R51, C47, C48
Right: U11, R52, R53, R55, C49, C50

De-emphasis circuitry is incorporated into the signal path to compensate for the pre-emphasis function performed before the analog to digital conversion. Both pre-emphasis and de-emphasis are used to help compensate for high frequency roll-off due to the conversion process.

Capacitors C47 and C49 along with resistors R49, R51, R53 and R55 form separate one-pole filters with dual op amp U11. R50 and R52 control the overall gain (approx. 7 dB) of the left and right de-emphasis stages, respectively. The outputs from U11 pass through C48 and C50 to remove any DC offsets before entering the Dry/Wet Mix Adjust circuitry.

Dry/Wet Mix Adjust

Dry Mix Buffers:	U5, R20, R21, C18, C19 (L)
	U5, R22, R23, C22, C23 (R)
MDACs:	U14 (L)
	U12 (R)
Dry/Wet Summing Amps:	U13, C58 (L)
	U13, C53 (R)
MDAC Interface ICs:	U22, U23, U26, U29

The left and right signals from the input preamplifier stage are applied to the dry mix buffers (dual op amp U5) at R21 and R23. U5 incorporates 6 dB of gain into the left and right dry audio signal paths. The outputs from the mix buffers pass through AC coupling caps C18 and C22 to remove any DC offsets, and feed the 8-bit multiplying digital to analog converters (MDACs).

Two dual MDACs (U12, U14) are used to control the balance of dry and wet signals. Each package controls either the left or right dry/wet signals. The dry signal is fed into pin 18 (VREFB) and the wet signal is fed into pin 4 (VREFA) of each dual MDAC. The MDACs provide the input and feedback resistors for the left and right sides of dual op amp U13. 8-bit data is sent to each MDAC by a dedicated 74HCT541 latch; U22 serves MDAC, U12; U23 serves MDAC, U14. This data tells the MDAC what to set the input resistance value to. Since they are dual MDACs, pin 6 (A/B) is used for writing data to the desired side, corresponding to the wet or dry signal. A 74HCT138 (U29) decodes the A/B command. Write (pin16) and Chip Select (pin 15) commands come from a 74HCT32 (U26) and are used when writing data.

The MDAC outputs (pins 2,20) are summed together by a dual op amp (U13). One stage of U13 sums the dry and wet signals from U12; the other stage sums the dry and wet signals from U14. The feedback loop is completed by connecting the op amp outputs to pin 19 (RFBB) of each MDAC. C53 and C58 are incorporated into the feedback loops for high frequency compensation. Pin 1 of U13 outputs the combined dry/wet left signal; pin 7 outputs the right signal.

This circuit provides processor control over dry/wet mix ratio, which is also used for various DSP effects.

Analog Outputs

Output Level Pot:	R2 (located on front panel PC board)
Output Amp:	U15, R60 - R63, C59, C60, C66 (L)
	U15, R64 - R67, C63, C64, C65 (R)
Output Mute:	U27, Q3, R69, R72, C76 (control circuitry)
	Q2, R36, R37, C34 (L)
	Q1, R32, R33, C32 (R)
Output Protection:	CR9, CR10, R34, R35 (L)
	CR5, CR6, R30, R31 (R)
Output RFI Filtering:	C33, FB4 (L)
	C31, FB3 (R)
Output Jacks:	J4 (L)
	J3 (R)

The left and right signals from the MDAC summing amps pass through AC coupling caps (C65, C66) and a ribbon cable to the Output level control (R2), located on the front panel printed circuit board. R2 adjusts the signal level being applied to the output amplifier, U15. This dual op amp provides 6 dB of gain for both left and right signals. An output impedance of 600 ohms is developed by resistors R30, R31 for the right output, and R34, R35 for the left output. These resistors also provide current limiting protection. Bipolar AC coupling capacitors (C59 and C63) and pulldown resistors (R60 and R64) are installed to prevent DC offset voltages from appearing at the outputs of the LXP-15.

Two discrete JFETs, Q1 and Q2, provide a muting function by creating a low impedance path to ground along both output signal paths. In this case, R31 and R35 serve as current limiting resistors by preventing the outputs of op amp U15 from shorting directly to ground. The mute function is under software control. The MUTE/ command signal emanates from U27 pin 19, and is applied to the base of transistor Q3 through R72. When MUTE/ is low, Q3 is on, which provides a positive DC voltage to the gates of Q1 and Q2. The JFETs turn on and enable mute. When MUTE/ is high, Q3 turns off which allows a negative voltage to be applied to the JFETs. Q1 and Q2 turn off and disable mute. C76 and R69 insure a quiet transition between mute and unmute by ramping the gate voltages. Mute is enabled during power up or power down conditions, and program change sequences.

The output jacks (J3 and J4) are located next to the input jacks on the rear panel. The 1/4" unbalanced phone jacks are configured in such a way that the left and right output signals are summed together if only one plug is connected. However, both output jacks should be utilized to attain full stereo effects.

Static protection is provided for the output circuitry by diodes CR5, CR6, CR9 and CR10. Ferrite beads FB3 and FB4 and capacitors C31 and C33 prevent unwanted high frequency interference from entering or leaving the LXP-15 through the output cables.

Controller Inputs

1. J9, R99 - R101, C107, C108, CR19, CR20, FB9; R86, C93
2. J8, R81 - R83, C89, C90, CR17, CR18, FB8; R85, C92
3. J7, R78 - R80, C87, C88, CR15, CR16, FB7; R84, C91
4. J6, R73 - R75, C79, C80, CR13, CR14, FB6; R88, C95
5. J5, R68, R70, R71, C77, C78, CR11, CR12, FB5; R87, C94

Five 1/4 inch tip/ring/sleeve phone jacks are provided at the rear panel for either swept or switched controller inputs. Since the circuitry is similar for each input, only controller #1 will be described.

The sleeve of phone jack J9 is connected to digital ground. The ring provides a +5 volt output. Ferrite bead FB9 and capacitor C108 prevent high frequency interference from entering or leaving the LXP-15 at this point. R100 is a current limiting resistor. The tip of the phone jack receives the control voltage. Resistor R99 and capacitor C107 act as a low pass filter for unwanted high frequencies, whereas diodes CR19 and CR20 provide static and overvoltage protection. R86 and C93 are located close to the analog to digital converter's inputs to help isolate unwanted signals.

An ADC0809 8-bit analog to digital converter (U24) is used to convert the analog control voltages to 8-bit digital words. This particular converter has eight separate analog inputs which are scanned. Five inputs are used for the controller inputs (pins 26, 27, 28, 1, 2), one is used for signal headroom monitoring (pin 4), another is used to check the battery voltage (pin 3), and the last input is not used and terminated to digital ground (pin 5).

When nothing is plugged into a controller input jack, the tip of the jack is shorted to ground. To operate a switch, it should be connected between the tip and sleeve. When the switch is open, the input voltage will be high as +5 volts conducts through a resistor (R101, for controller #1). Closing the switch will short the input to ground. A swept voltage may be obtained by connecting a potentiometer across the ring and sleeve with its wiper hooked to the tip. The minimum impedance for the pot is 50 kilohms to provide sufficient voltage range.

Power Fail/Reset

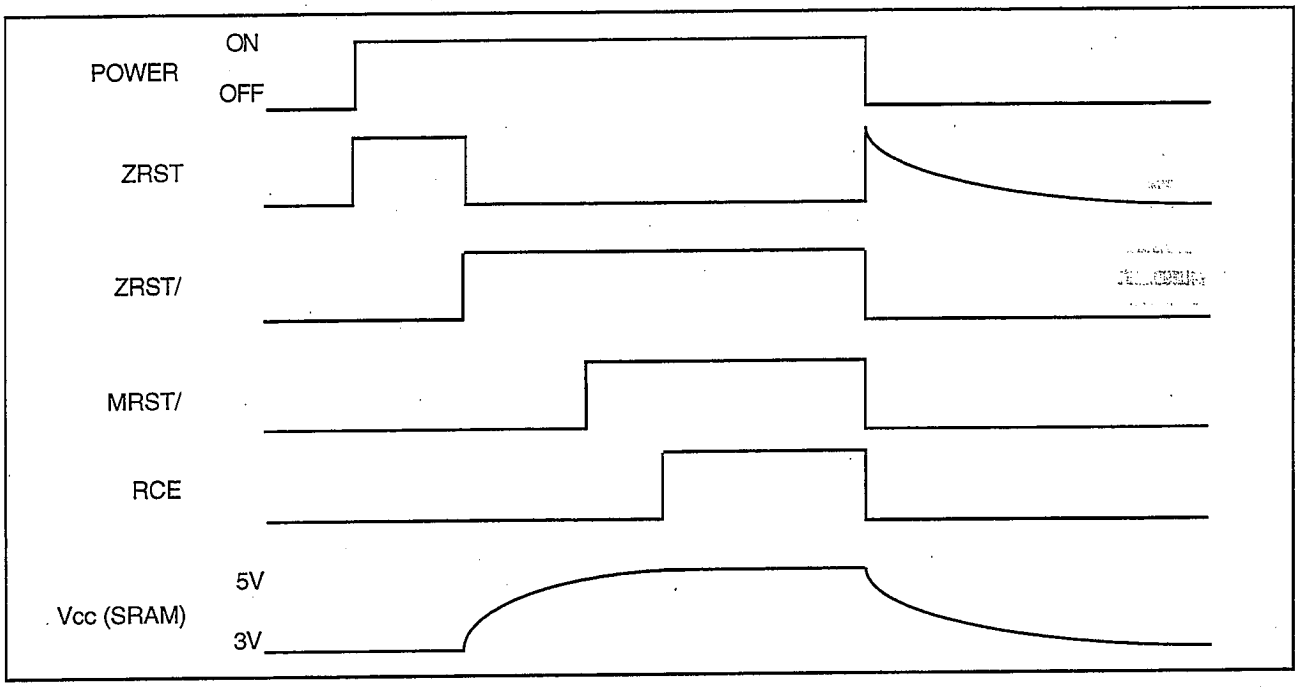
Low voltage detect:	U53, Q7, R126, R127, R129, R130, C138, C141, FB14
ZRST:	U53 (pin 1)
ZRST/:	U53 (pin 2)
MRST/:	U53 (pin 4), R128, C137, CR24
RCE:	Q8 (collector, pin 3), R132 - R134, CR26

The reset circuitry insures proper operation of the LXP-15 during power up and power fail conditions. This circuitry monitors the +5VUNREG supply and provides ZRST, ZRST/, MRST/ and RCE command signals.

The +5VUNREG supply is filtered by FB14 and C141 to prevent noise spikes on the AC line from tripping the reset function. R129 and R130 create a voltage divider which feeds C138 and the base of transistor Q7. C138 provides low frequency filtering for the base voltage. Q7 has a common emitter configuration with a pull-up resistor (R126) to +5 VDC on its collector.

The collector voltage is applied to the input of a Schmitt inverter (U53, pin 1) whose output provides feedback to the base of Q7 through R127. During power up Q7 is off until the +5VUNREG supply exceeds the level necessary to bring the transistor into its active state. At this time, the collector voltage starts to drop, which causes the inverter output to go high and turns Q7 on. During a power fail or low power sequence, the +5VUNREG supply starts to drop, bringing Q7 out of saturation and into its active state. The collector voltage starts to increase which causes the inverter output to go low and turns the transistor off.

With the power transformer wired for 120 VAC, an AC line voltage above 100% will turn Q7 on and insure the proper power up sequence for the LXP-15 circuitry. If the AC line voltage drops below 100%, Q7 turns off, enabling the required reset signals.



The collector of Q7 provides the ZRST command signal. ZRST is applied to the UART's Reset pin (U57, pin 21) and the Battery Backup circuitry, which require an active high signal for reset to occur.

The inverter output (U53, pin 2) provides the ZRST/ command signal. ZRST/ is applied to the Lexichip's Reset pin (U25, pin 74) which requires an active low signal for reset to occur. The ZRST/ command is also used to clear two 74HCT273 latches (U27, U60) and two 74HCT161 counters (U58, U59). Pin 12 of a 74F08 AND gate (U20) is connected to ZRST/ as well.

ZRST is also applied to another inverter input (U53, pin 3) through a delay circuit made up of CR24, C137 and R128. The output of this inverter (pin 4) provides the MRST/ command signal. MRST/ is used to reset the Master Z80 Processor (U46, pin 26) which requires an active low signal. The Master Z80 Processor is the last device enabled by the LXP-15 Reset circuitry, due to the delay circuit associated with MRST/. This insures that all other devices are in a known active state when the Master Z80 is enabled.

MRST/ is also used to provide RCE, which is the SRAM Chip Enable. RCE is controlled by Q8. The collector of Q8 is connected to the chip enable pins of the SRAMs (U43, U44, U49; pin26), and provides the RCE command signal. MRST/ is applied to the emitter of Q8 through R133. The base of the transistor is biased by CR26 and R132. Upon power up, MRST/ will go high after a delay, causing RCE to go high and enabling the SRAMs. The delay provided by MRST/ allows the SRAM VCC to stabilize before they are enabled. MRST/ and RCE immediately go low upon power fail, before +5 VDC goes out of regulation and the SRAM VCC drops to +3 volts.

The 74HCT14 hex inverter (U53) is an important component in the LXP-15 Reset circuitry. Therefore, its power supply is independent from the +5 VDC supply. CR23, R124, C133 and C134 provide a separate +4.7 VDC supply to insure proper operation of U53 for a brief time during a power fail condition.

Battery Backup/ Voltage Monitor

Battery Backup: Q9, Q10, R135, R138, C144, CR27, CR28, BAT1
Battery Voltage Monitor: U56, R136, R137, C142

Battery Backup is required in the LXP-15 to maintain the non-volatile function of the master processors' associated SRAMs. A 3 volt lithium battery (BAT1) maintains the minimum power requirement of the SRAM IC's, (U43, U44) while power is disconnected from the unit.

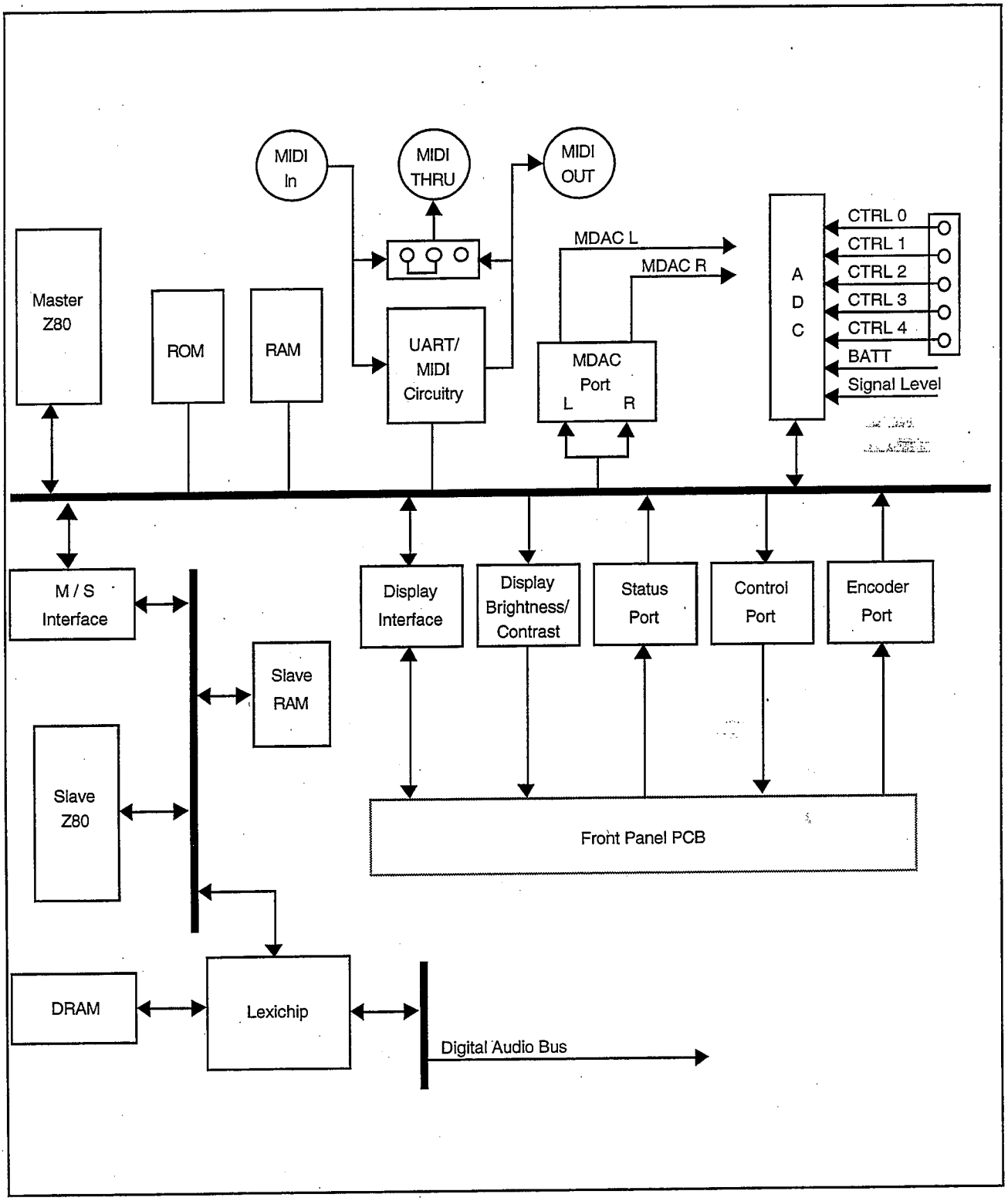
ZRST is used for controlling the Battery Backup circuitry, and drives the base of Q9 through R135. During power up, ZRST goes low which turns Q9 off. In turn, Q10 becomes active in its emitter follower configuration. The base of Q10 is biased by R138 and CR28, causing its emitter to ramp to +5 volts as C144 charges. This voltage is applied to the VCC pins of the SRAMs (U43, U44). Under these conditions CR27 is reverse biased, preventing the +5 volts from reaching BAT1.

Upon a power fail condition, ZRST goes high which turns Q9 on and Q10 off. C144 discharges until CR27 becomes forward biased, which provides +3 volts from the lithium battery for the SRAM VCC.

The Battery Backup circuitry, along with the RCE signal command, prevents stored data from being destroyed during power failure.

An LM393 comparator (U56) is used to monitor the battery voltage. A voltage divider is set up by R136 and R137 to supply a reference voltage of +2.5 volts to pin 3 of U56. Pin 2 of the comparator is connected to the positive side of the battery. If the battery voltage is higher than the reference voltage, the output of the comparator (pin 1) will be low. When the battery voltage is lower than the reference voltage pin 1 will be high (+5 volts). The output from the comparator is applied to an input of the A to D converter (U24, pin 3) where it is scanned by the master processor. Battery status is shown on the front panel display .This comparator maintains a very high input impedance upon power down which keeps battery drain to a minimum.

Digital Circuitry



Overview

The LXP-15 utilizes two Z80 microprocessors and the Lexchip digital signal processor to perform multiple digital audio effects. These effects are controlled viafront-panel user interface and by MIDI commands from serial dynamic MIDI interface. Each processor has its own support circuitry, data and address buses. Communication between processors is performed via two interfaces.The Master/Slave Interface allows Master Z80 access to the Slave bus where read/write operations can be performed on Slave RAM and Lexichip-1 Writeable Control Store (WCS). The Lexichip-1 WCS contains program memory and registers. It can be accessed via its on-chip Z80 interface which connects directly to the Slave Bus.

During normal operation, sampled audio is converted into digital data using pulse-code modulation(PCM). Digital effects processing is performed by the Lexichip under the control of both Master and Slave Z80 processors. The Master Z80, which handles all operator I/O and housekeeping functions, is able to pass on DSP control information to the other two processors.The Slave Z80 is dedicated to the task of controlling the Lexichip-1 and is, therefore, used to perform any DSP control functions which require precise timing, such as pitch shifting.

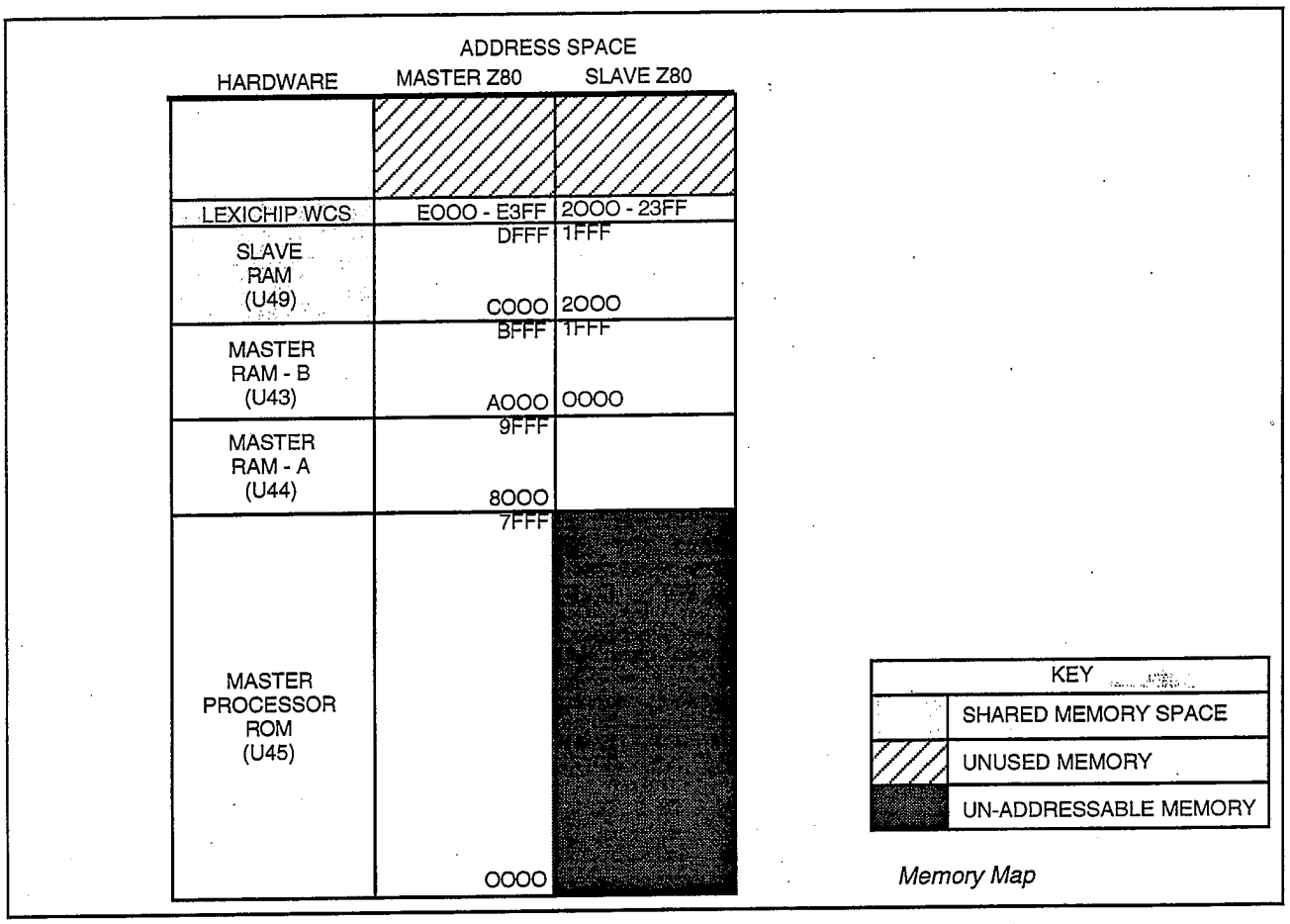
Processor Circuitry

Master Processor Functions

The Master Z80 (U46) handles basic system control and user interface I/O operations. It has the ability to write program code and data directly into the Slave Z80 Program RAM and Lexichip Writeable Control Store (WCS) by directly accessing the Slave Z80 bus via the Master / Slave Interface. Its specific tasks are:

- Processing data and instructions to and from the UART
- Processing data and instructions to and from the Lexichip-1
- Handling user-data input and LED operations
- Maintenence of non-volatile, user-controlled registers.
- Loading and manipulation of Slave processor program code and data
- Controlling Slave processor reset and interrupt functions
- Controlling audio muting hardware

Memory



Memory Map

64K of bank-switched ROM space is contained in one 27C512 (U45). 32K of this ROM space is mapped into the Master Z80's memory space at one time. Bank switching is performed as an I/O operation, and controls address line 15 (MADR15). Stored in this 64K area are Slave and Lexichip program routines which are loaded by the Master Z80 via the Master/Slave interface. Diagnostics, I/O and housekeeping subroutines executed by the Master Z80 are also contained in this ROM space, as well as all of the factory-shipped User and Preset programs.

Read/Write memory includes 16K of static RAM directly on Master processor bus (Master RAM), 8K of static RAM shared with the Slave Z80 (Slave RAM) and 1K Writeable Control Store in the Lexichip (WCS).

The 16K of Master RAM is kept non-volatile at power down with a 3-volt lithium cell (BAT1). This RAM consists of two 62C64 8Kx8 static RAM ICs (U44 and U43). The RCE signal from the Power Fail/Reset circuitry controls this RAM's active high CE input for proper power up/down control of non-volatile RAM.

Slave RAM consists of one 62C64 IC which is connected to the Master/Slave interface circuitry. Master and Slave Z80s have access to all 8K of this memory. Slave Z80 receives program instructions from this memory space. The Master Z80 uploads Slave code into Slave RAM. Master access to Slave RAM occurs during two conditions:

1. When Slave Z80 is in RESET,
2. When Slave Z80 is in the last two clock periods of an instruction fetch operation.

See Master/Slave interface section for more information.

The Lexichip-1 has its own on-chip program memory and I/O registers called the Writeable Control Store (WCS). The WCS can be accessed by both Master and Slave Z80s. The conditions for Master access to the WCS are the same as for Slave RAM access (i.e. during the Slave refresh cycle).

Decoding Circuitry

Associated circuitry: U40, U29, U21, U20, U30

U40, a GAL16V8 is programmed to handle basic Master Z80 signal input decoding for memory and I/O functions. U29, a 74HCT138, further decodes I/O signal for specific I/O functions.

Bank switching is also controlled by U40. The BIO output is set HIGH by one I/O address and LOW by another. This signal is ANDed with power up reset (ZRST/) and fed back into U40 to complete a set/reset flop circuit.

ZRST/ ensures that the BANK signal is LOW on power up.

The MSYNC signal (U21.13) is an I/O decoded signal generated by the Master Z80. This signal, fed directly into the Slave GAL16V8 (U54.3), requests synchronization to the Lexichip audio signal processing. The result of this signal is that the Master Z80 is put into a wait state until the next word clock pulse (WC/) is generated by the Lexichip. This pulse marks the start of the audio processing cycle within the Lexichip. See the Slave Z80 section for timing information on this signal, which enables the system software to get in phase with DSP functions.

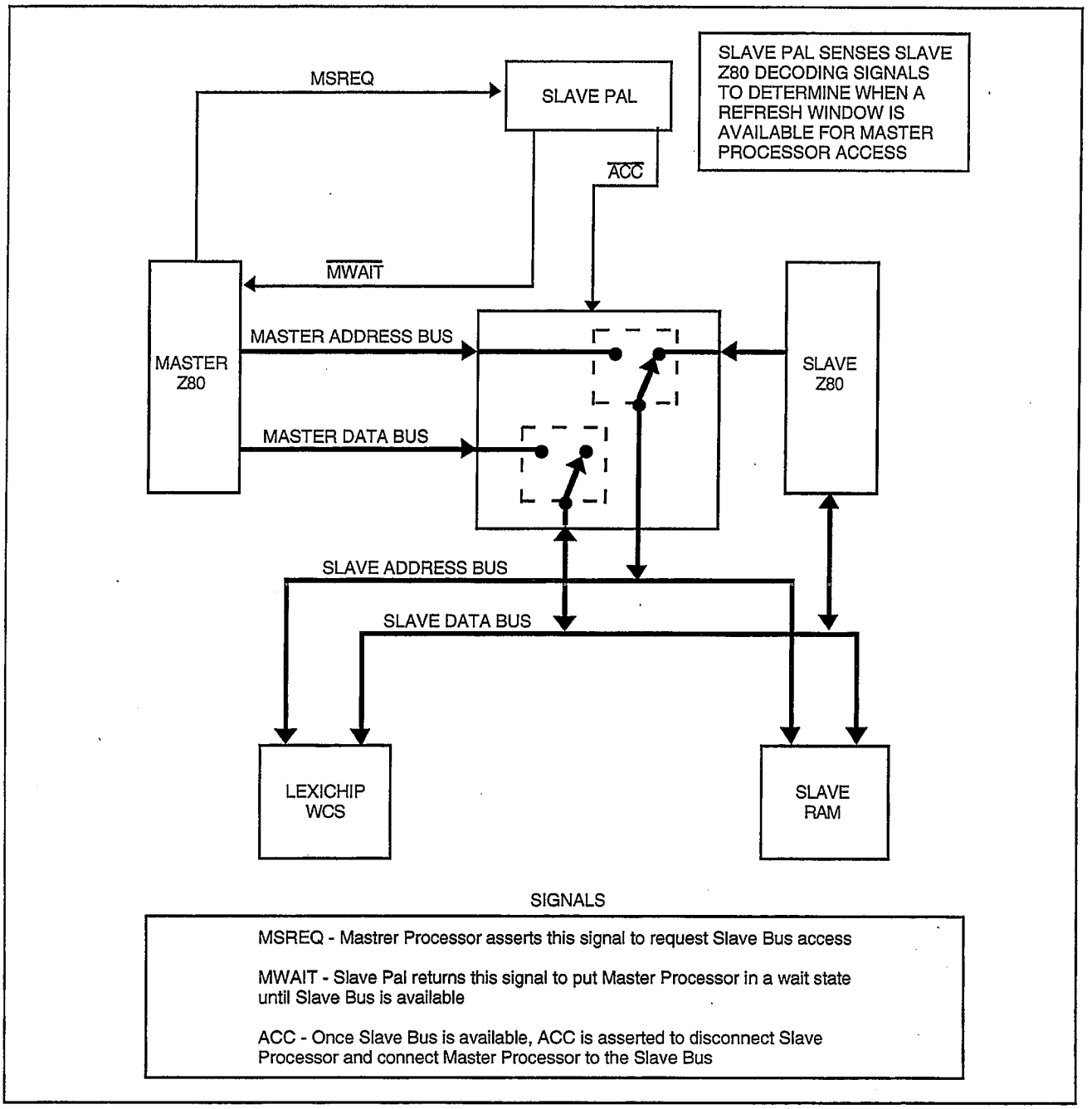
Signal Name	Hex Address	Description
ROM/	0000-7FFF	Master ROM chip enable
RAMA/	8000-9FFF	Master RAM chip enable (lower 8K)
RAMB/	A000-BFFF	Master RAM chip enable (upper 8K)
MSREQ	C000-E300	Master to Slave bus request
IOEN2/	CO	I/O enable for MSYNC and LCDCI
BIO	80(LO)/40(HI)	ROM bank switch enable
IOEN	00	I/O decoder (U29) enable
MSYNC	C0	Master processor sync request
BANK	B0(LO)/40(HI)	ROM bank select bit
LCDCI	E0	LC display contrast/intensity control enable
DISPEN/	00	LC display enable
MAEN/	08	MDAC A (left channel) enable
MBEN/	10	MDAC B (right channel) enable
ADC/	18	ADC enable
CONT/	20	Control register enable
UART/	28	UART chip enable
STATUS/	30	Status register select
ENCEN/	38	Encoder status enable

Decoding Map

Master/Slave Interface

A memory refresh period is produced by a Z80 processor for two clock cycles during every instruction fetch. Since the static RAM used by the Master and Slave Z80s does not require refreshing, the master processor utilizes the Slave Z80's available refresh period to gain access to Slave memory. If the Slave Z80 is in reset, the Master is not required to wait for this refresh operation, and gains immediate access to the Slave bus. Syncronization of timing and handling of access signaling for the Slave Bus is performed by the Slave Decoder (U54).

The following diagram illustrates the actual hardware interface.



Master /Slave Interface Diagram

Slave Z80 Circuitry

The Slave Z80 (U55) is strictly dedicated to controlling Lexichip operations. This task is performed by accessing the Lexichip WCS, the on-chip memory and register storage which is connected to the Slave Z80 bus via a Read/ Write port .

Memory

The Slave Z80 has access to the 8K of Slave RAM, as well as the Lexichip WCS. Slave code is uploaded into the Slave RAM by the Master Z80. This memory serves as program memory storage, as well as random access read/ write memory for the Slave processor.

Both Z80s are capable of writing instructions to the Lexichip-1 but, due to Master/Slave interface architecture, the Slave processor functions without interruption by the Master processor as it gains access to the Slave RAM and WCS. Because the Master processor functions are transparent to the Slave processor, the Slave processor is used to perform time-sensitive tasks such as pitch detection for the pitch shifting algorithm.

Decoding/Timing

SLAVE DECODING/TIMING					
SRMREQ/	MSREQ	LRADR13	ACC/	SRAM/	LEX/
0	1	0	1	0	1
X	0	0	0	0	1
0	1	1	1	1	0
X	0	1	0	1	0

1=High Level; 0=Low Level; X=Don't Care

The Slave decoder (U54) , GAL16V8, performs the following functions:

1. Memory decoding for Lexichip and Slave RAM
2. Slave Bus access management
3. UCLK (UART clock) generation

The Slave decoder decodes Lexichip/Slave RAM address line 13 (LRADR13) for SRAM and LEX select signals. Internal logic determines whether the Master or Slave Z80 currently has bus access by internally sensing the status of ACC/ (Master processor access enable). SRAM/ and LEX signals are then decoded accordingly. See Slave memory decoding chart above.

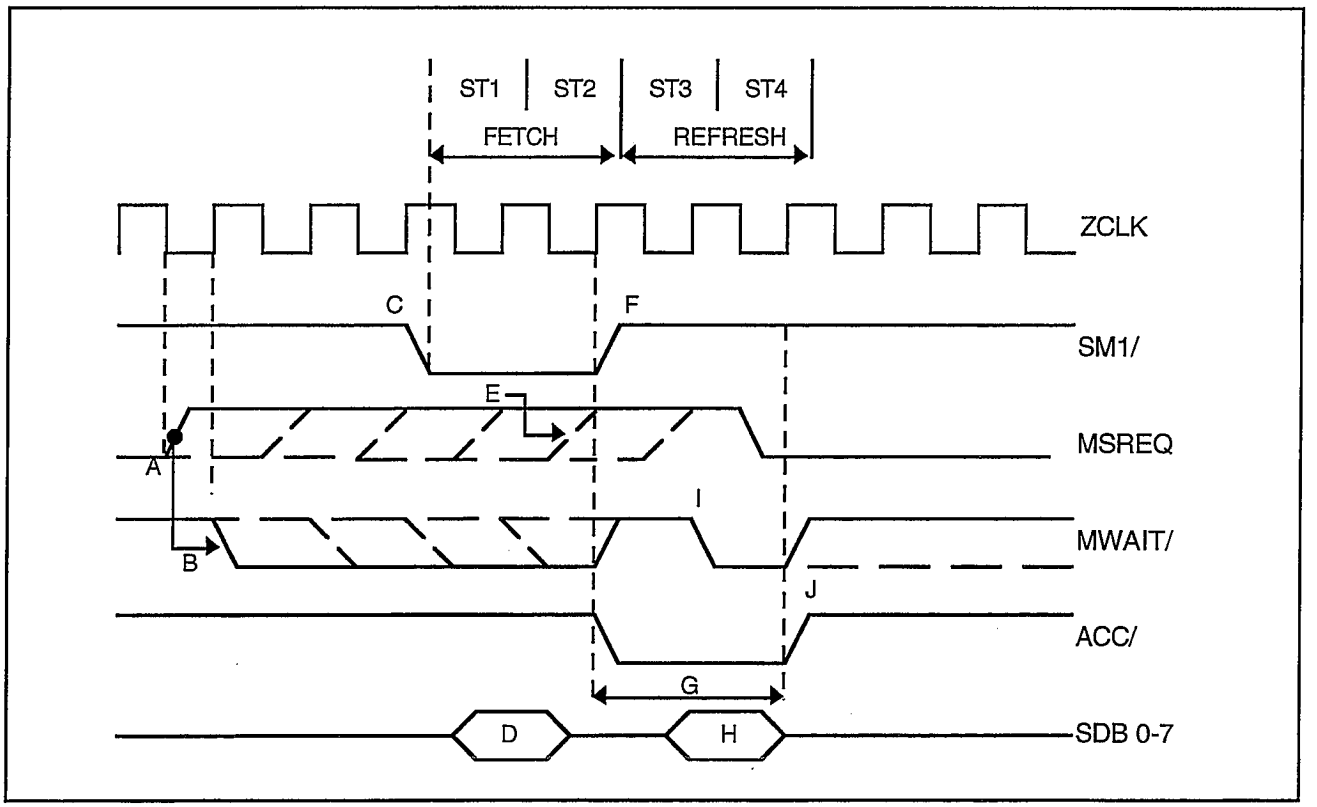
The Master/Slave Z80 bus access is determined by the status of the Slave Z80. There are two instances where the Master Z80's request to gain Slave bus access is honored:

1. Slave Z80 reset (SRST/) has been asserted.
2. Slave Z80 is in the memory refresh period of an instruction fetch.

Slave Decoding

The Slave decoder senses associated Z80 signals to manage bus access. When MSREQ is asserted by the Master processor, WAIT is asserted by the Slave decoder unless or until either of the conditions stated above is satisfied. Diagrams of Slave bus access timing are shown below.

Slave Refresh Access



A The Master Z80 requests Slave Access by asserting MSREQ.

B MWAIT/ is asserted to keep the Master Z80 in a wait state until the Refresh window occurs.

C SM1/ indicates Slave Z80 Instruction Fetch period.

D Instruction code is read from the 8-bit data bus.

E If MSREQ is asserted during the second T state of Instruction Fetch period (SM1/), the Master Z80 is in sync with the Slave Z80 Refresh period and no wait states will occur.

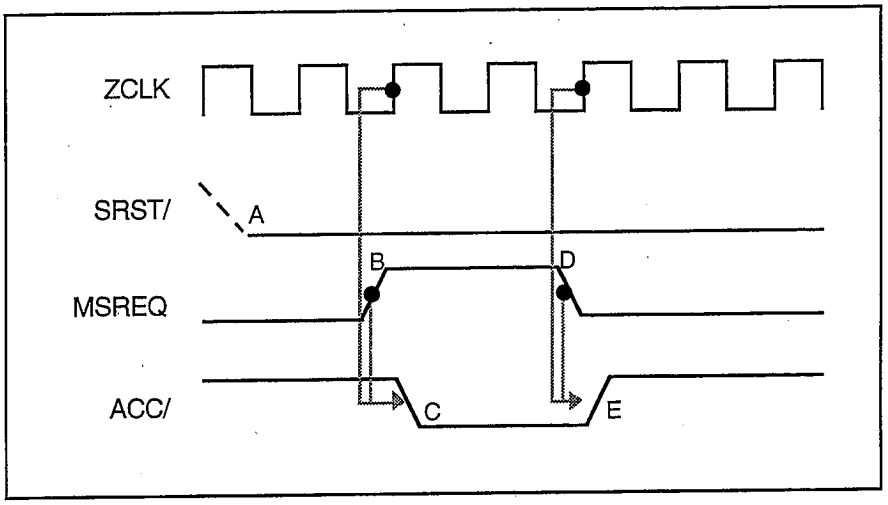
F The rising edge of SM1/ indicates the beginning of Slave Z80 Refresh period, which is the Slave Bus access window.

G The Refresh access window occurs for the last two T states during a Slave Z80 Instruction Fetch cycle. If MSREQ has been previously asserted, ACC/ will go low and set DATA selector ICs and Master buffer (U31) to allow Master Z80 access to Slave data and address busses.

H During this Refresh period, the Slave Z80 data lines are placed in a high impedance state. The Master Z80 is then allowed access to the 8-bit data bus and 14-bit address bus for a read or write operation.

I MWAIT/ goes low for the 4th T state of the Slave Instruction Fetch. If the Master Z80 has already gained access to the Slave Bus at this point this MWAIT/ will be ignored. If MSREQ is activated just after D, this wait signal will be acknowledged, and the Master processor will insert waits until the next Refresh period.

J At the end of Slave Refresh Access, ACC/ is returned to a logical high, which removes Master Z80 from the Slave Bus .

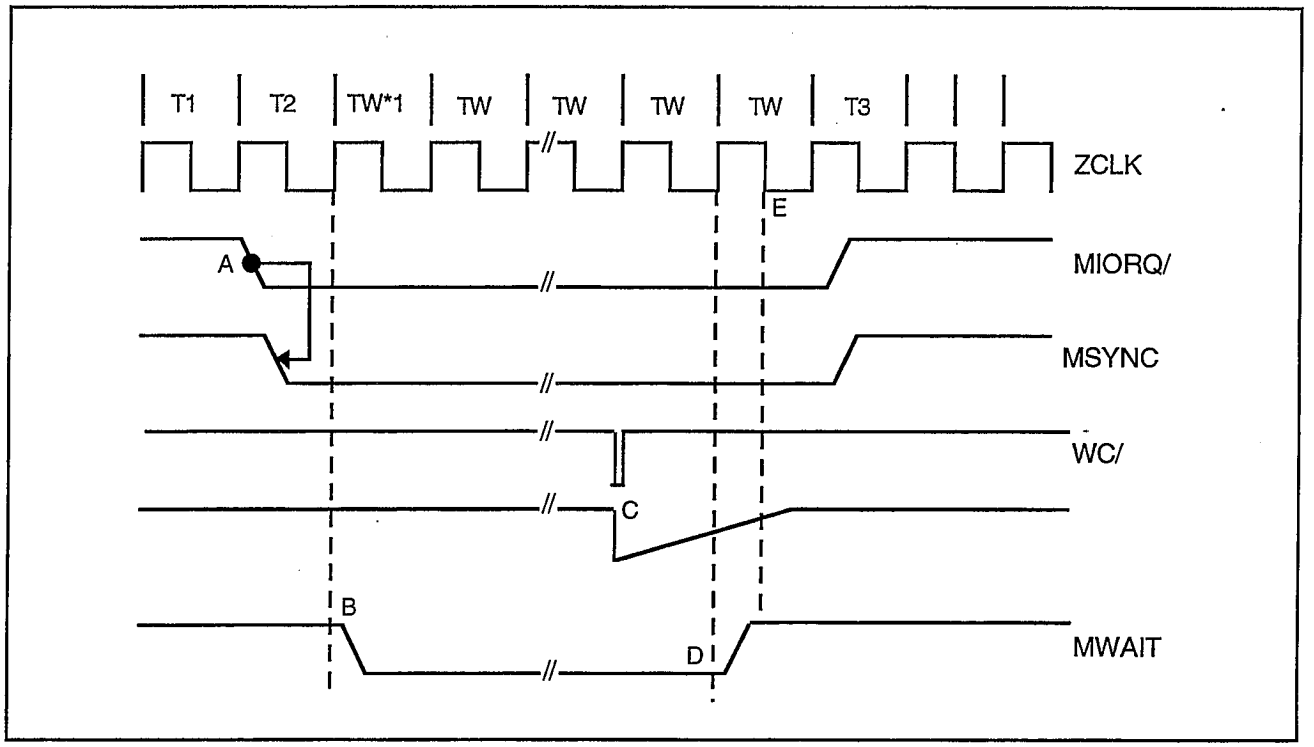


Slave Reset Access

A Slave Z80 reset signal is active (low).	D After read/write operation is performed, MSREQ is de-activated.
B Master Z80 requests access to Slave bus by asserting MSREQ.	E On rising edge of ZCLK, ACC/ is de-activated and bus is returned to Slave Z80.
C On rising edge of ZCLK, ACC/ is asserted, allowing Master Z80 access to Slave bus.	

MSYNC Signaling

The Master Z80 generates the MSYNC request when it requires synchronization with audio processing (as explained in the Master Z80 decoding section). The Slave decoder receives this request and places the Master Z80 into a wait state by activating MWAIT/. The WC/ pulse duration is extended with an RC network (CR25, R125, C136) to allow the Slave decoder enough time to sense its presence. Once this extended pulse (WCE/) occurs, MWAIT/ is deactivated and the Master processor will be synchronized to the Lexichip WC/ timing. See the timing diagram below.



A MIORQ/ goes low and I/O address for MSYNC request is asserted. B As a result of MSYNC input, Slave decoder asserts MWAIT/ until WCE/ is asserted.	C WC/ is asserted and is extended to produce WCE/. D On rising edge of ZCLK Slave decoder, seeing WCE/ active, removes MWAIT/ signal.	E On falling edge of ZCLK Master Z80 sees MWAIT/ removed and continues I/O instruction TS period on next clock cycle. *One wait state is asserted automatically by Z80 during I/O operations. Additional wait states occur if MWAIT is asserted.

Digital Audio Processor Circuitry

LEXICHIP: Z80 Interface

The Lexichip-1 (U25) performs all the digital effects processing calculations for the LXP-15. It receives instructions from its internal program RAM, referred to as the Writeable Control Store (WCS). Address, data, and control lines for the WCS are shared with the Slave Z80 bus. This allows both Slave and Master Z80 processors to load audio effects programs into the Lexichip-1, monitor status of audio data, and synchronously change program parameter values in audio programs. Both Master and Slave Z80 processors treat the 1K bytes of WCS as mapped memory space.

Clocks

An internal crystal oscillator driver circuit drives a 16MHz crystal mounted across pins 75 and 76 on the Lexichip-1. Internal Lexichip-1 circuitry divides this clock frequency down to provide the 4MHz ZCLK which is used by the Z80 processors.

The PCLK1 (pin 73) output is programmed to divide down the 16MHz clock to the 500kHz MIDICLK signal. This signal is utilized by the UART IC (U3) to set up the serial communications baud rate.

WC/ (pin 59) is used as a clock reference by the LXP-15. It operates at a 31.25 kHz sample rate and is utilized by the UART interrupt timing circuitry, as well as by the Slave decoding circuitry, to sync the Master processor to DSP operations.

Audio Memory

Four 64K x 4-bit dynamic RAM ICs (U32,U34,U36,U38) provide the 64K x 16-bit RAM space used by the Lexichip-1 for audio data storage. DRAM read, write, and refresh functions are performed by a dedicated set of address and control lines and a 16-bit data bus provided by the Lexichip-1.

LEXICHIP: DAC/ADC Control Logic and Data Port

Internal control logic circuitry enables the Lexichip-1 to command complete control over external DAC functionality with minimal external circuitry.

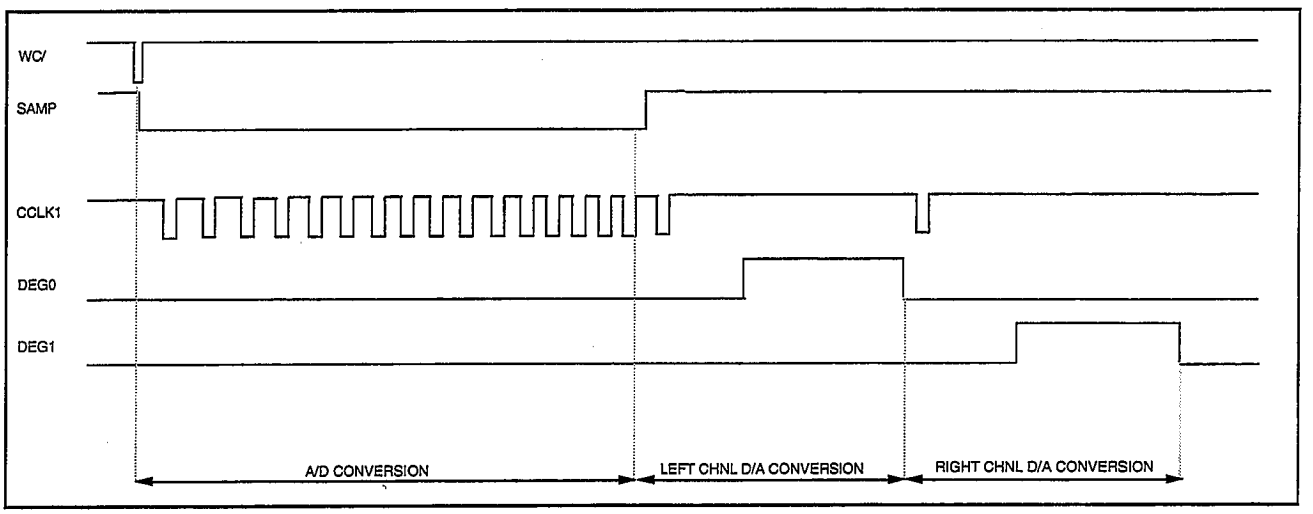
Two 8 bit latches (U18,U19) are used to latch 16 bit data out to the DAC via the DRAM data bus. Lexichip output CCLK1 clocks DAC data into these DAC conversion latches.

An internal Successive Approximation Register (SAR) allows the DAC, in conjunction with an external comparator, to perform analog to digital conversions. A data value is latched into the conversion latch. DAC output is compared to analog input by the comparator. The comparator's resulting output (DATA) is applied to Lexichip-1 input SI1, and the SAR logic circuitry determines either the next DAC output value or an end of conversion. Converted data is then processed by the Lexichip-1 with instructions from its RAM resident digital effects program.

DAC logic signals are provided by the Lexichip-1 to control the Sample and Hold (SAH) and deglitch functions and conversion data latching. A Word Clock signal (WC/) is used as a clock reference and indicates the beginning of a conversion cycle.

On the falling edge of WC/, SAMP goes low in order to hold an input sample for an A/D conversion. The internal SAR then applies a DAC data output to DAB0-15. This data is latched into conversion latches on the positive edge of the CCLK1 signal. The DATA signal from comparator is then compared by Lexichip-1 to determine the next SAR output value. Sixteen SAR output samples are required to perform an analog conversion. Since the later samples produce smaller voltage changes on DAC output, less time is required for DAC to settle, therefore, the time duration between CCLK1 pulses towards the end of the A/D conversion is reduced.

The 17th CCLK1 pulse after WC/ latches left channel data out to the DAC. After sufficient DAC settling time, the left channel deglitch switch is disabled by the high state of DEG0, applying a DAC sample to the left channel output circuitry. The last CCLK1 pulse in the WC/ cycle latches right channel data to the DAC. DEG1 goes high which applies the DAC sample to the right channel output circuitry.



Converter Timing

UART/MIDI Interface

ADDR	RD	WR	Function
28H	0	1	Read receive data
28H	1	0	Write transmit data
29H	0	1	Read UART status
29H	1	0	Write command

Decoding Map

UART

An 82C51 UART IC (U57) is utilized to process the 31.25kHz baud rate MIDI serial communications in the LXP-15. This serial communications processor works in conjunction with the Master Z80 to process MIDI commands and incoming messages. It receives two clocks: UCLK, a 2MHz clock divided down from ZCLK by the Slave GAL, and MIDICLK, a 500kHz clock generated by the Lexichip (pin 73). UCLK functions as a processor clock for U37 and MIDICLK is divided down internally to produce the proper baud rate for serial communications.

MIDI Interrupt

A MIDI interrupt circuit asserts a maskable interrupt on the Master Z80 every 288µs to service any incoming MIDI messages received via the MIDI interface. This interrupt is generated by a 74HCT161 counter (U58). WC/, which also occurs at a 31.25kHz rate, is the clock input signal for this counter. U58 is wired to produce an overflow (RCO) signal every nine WC/ clocks, thereby causing a maskable interrupt to the system at a rate slightly faster than the MIDI character rate.

MIDI Hardware

The MIDI hardware utilized by the LXP-15 complies with MIDI specs. It incorporates 5 pin, female DIN connectors for input, output, and thru connections (J10, J11, and J12). MIDI IN is ground-isolated by optocoupler U52 and applied to UART input R x D. TxD from UART is the source of transmitted MIDI signals from LXP-15. This signal is applied to an inverter (U53), and then connected to current loop driver Q4. MIDI THRU circuitry routes inputs back out to current loop driver Q5. Jumper W4 is for test purposes, and allows the THRU port to be set to behave as an OUT port, so that MIDI loop diagnostic tests can be performed on THRU port circuitry. It can permit the THRU to function as another MIDI OUTput when applications call for more drive capacity. This, however, is not its intended purpose.

MDAC Ports

ADDR	Function
08H	MDAC A (left) data port
10H	MDAC B (right) data port

Decoding Map

There are two dual Multiplying DACs utilized in the LXP-15 for wet and dry signal level controls (as explained in the Analog Circuit description section). OCIAL buffers U22 and U23 function as the interface for MDAC A and MDAC B. A quad OR gate (U26) further decodes control signals to produce the wet/dry select signals MASEL and MBSEL, as well as isolated write signals MAWR/ and MBWR/. These signal functions are shown in the chart on the following page.

MASEL	MBSEL	MAWR	MBWR	
0	X	0	1	Sets left channel wet level
1	X	0	1	Sets left channel dry level
X	0	1	0	Sets right channel wet level
X	1	1	0	Sets right channel dry level

1=High Level; 0=Low Level; X=Don't Care

A data value of 00H sets gain at selected control channel to zero. A value of FFh sets gain to One. MDACs allow for 256 gain levels to be software-selected via MDAC ports.

ADC Circuitry

Decoding Map

ADDR	WR	RD	Function
18H	0	1	External Input 1 conversion (AN0)
19H	0	1	External Input 2 conversion (AN1)
1AH	0	1	External Input 3 conversion (AN2)
1BH	0	1	External Input 4 conversion (AN3)
1CH	0	1	External Input 5 conversion (AN4)
1DH	0	1	Battery monitor conversion (AN5)
1EH	0	1	Signal level conversion (AN6)
18	1	0	Read converted value

U24, an ADC809, performs analog-to-digital conversion on five (5) external control voltage inputs, as well as on the Audio Signal Level monitor input and Battery Level monitor. Once digitally converted, these signals are processed by the Master Z80.

The five external inputs can be software-assigned by the user to control various parameters of audio effects. The Battery monitor and Signal Level monitor circuits are described in the Analog Circuit description .

Two OR gates (U21) decode ADC/ enable signals from the Master decoder, along with Master read and write signals to produce the START signal and ADCOE/ signals. START, which is active when MWR and ADC are active LOW, starts the conversion for the analog input specified by I/O address. When conversion is complete, U24 asserts EOC on pin 7 which is monitored by Master processor via its STATUS I/O port. The conversion result is read when ADC/ and MRD/ are active, thereby causing ADCOE/ to enable U24's data port output.

Display Interface

Decoding Map

ADDR	RD	WR	Function
00H	0	1	Display data read
00H	0	1	Display busy/address counter status
01H	0	1	Display data write
03H	1	0	Display command write

Associated circuitry: U28, U30, P2

U28 and U30 buffer signal lines from the Master Z80 to the data port on the LCD which is located on the front panel of the LXP-15. U28 is a bidirectional buffer (74HCT245) which allows 8-bit data to pass through and from the LCD via P2 connector. Address lines MADR0 and 1, along with the decoded display enable signal DISPEN/, are buffered by U30 and connect to the front panel PCB via P2 connector.

Display Brightness/Contrast Control

Decoding Map

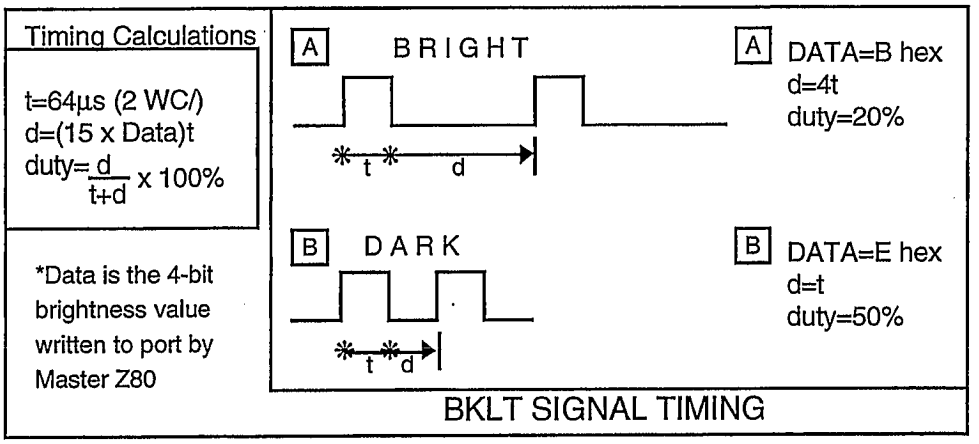
ADDR	WR	DATA	Function
C0H	0	MADR0-3	Contrast control (0=max, F=min)
C0H	0	MADR4-7	Brightness control (0=max, F=min)

Associated circuitry: U60, U59, U30, Q6, P5

User control of LCD contrast and brightness is provided by software. Master Z80 data lines are latched to provide output data for the contrast and brightness circuitry.

The contrast control output VO+ is a control voltage generated by the lower four bits in the contrast/brightness byte. MADR0-3 are latched and fed into a weighted resistor network (R141-144) via decodes CR29-32. A summing resistor R140 sums the currents out of this weighted network to provide a voltage level roughly proportional to the 4-bit digital value applied. VO+ is supplied to the LCD on the front panel via connector P2. As VO+ becomes more positive, display contrast will decrease.

The brightness control signal BKLT provides current to the LED backlight matrix on the LCD. This is a pulsewidth-modulated signal whose duty cycle determines the current level in the backlight LED matrix. The duty cycle of BKLT is derived from latched 4-bit value (MADR4-7) by U59 which is a 4-bit counter (74HCT161). The overflow output of U59 (RCO) is buffered by U30 and drives Q6. The LED matrix is the collector load for Q6 and makes its connection via P5 on the main PCB. The longer the duration of pulsewidth LOW condition, the brighter the display backlight. The 31.25kHz WC/ clock is used to clock U59. This frequency is divided down according to the 4-bit data input as shown on the following page.



BKLT SIGNAL TIMING

Status Port

I/O ADDR: 30H
RD: 0

Decoding Map

Data	Function
MADR0	PBIO-Pushbutton matrix input 0
MADR1	PBI1-Pushbutton matrix iinput 1
MADR2	PBI2-Pushbutton matrix input 2
MADR3	No connection
MADR4	ADC EOC
MADR5	BANK status (0=low, 1=high)
MADR6	No connection
MADR7	No connection

U41 functions as a buffer for the LXP-15 status byte. It is a read only port which allows the Master Z80 to monitor the status of the front panel pushbutton matrix, ADC end of conversion status, and ROM bank switching status. Bit assignments are shown in the chart above.

Control Port

I/O ADDR: 20H
WR: 0

Data	Function
MADR0	Headroom 0
MADR1	Headroom 1
MADR2	Headroom 2
MADR3	Headroom 3
MADR4	PBO0 (Pushbutton matrix output 0)
MADR5	PBO1 (Pushbutton matrix output 1)
MADR6	Slave reset (SRST/)
MADR7	MUTE/ (Audio muting)

Decoding Map

U27 performs the function of a buffer for the write only control port. The LXP-15 Master Z80 writes data to this port to set Headroom indicator LEDs ON or OFF, Pushbutton matrix outputs 0 and 1, Slave reset, and audio muting, to active or inactive states. Data is latched by U27 (a 74HCT273). Pushbutton matrix outputs and Headroom indicator signals are sent to the front panel PCB via P3.

Encoder Port

I/O ADDR: 38H
RD: 0

Data	Function
MADR0-3	Soft knob 0-3
MADR4-7	Select knob 0-3

Decoding Map

The encoder port is a read only I/O port. U42, a 74HCT541 is a buffer which provides status bits from the front panel 16-position encoders to the Master Z80 data bus.

Power Supply Circuit Description

Primary side components: C149, C150, F1, F2, L1, VR1, VR2
+15 VDC components: C151, C152, C156, CR34, CR36, CR38, CR39, U61
-15 VDC components: C153, C154, C157, CR35, CR37, CR40, CR41, U62
+5 VDC components: C155, C158 - C161, CR42 - CR45, U63

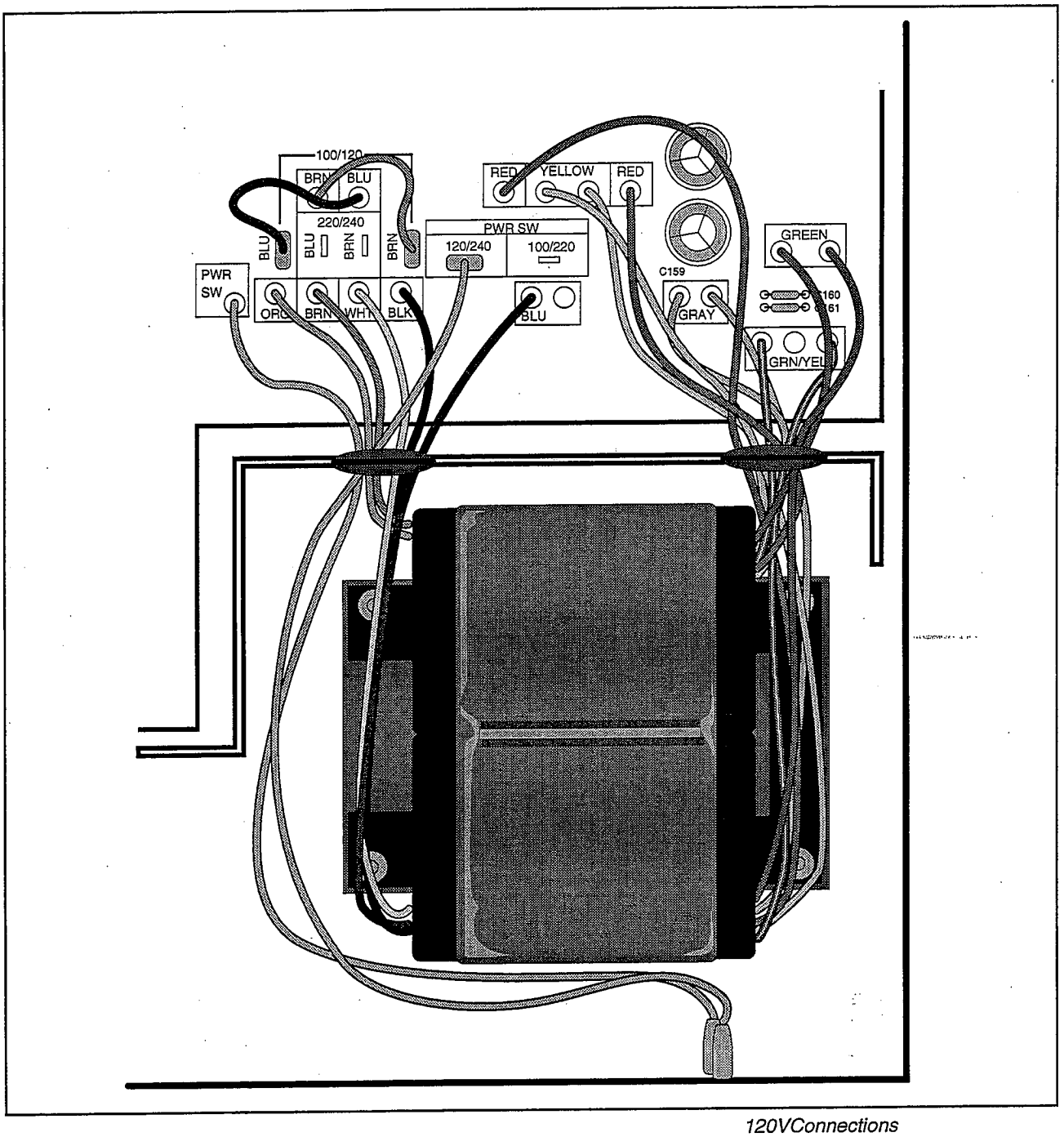
The LXP-15 has an internal power supply that produces its required DC voltages from AC line voltages ranging from 100 to 240 volts at 50 or 60 Hz. Since the same transformer is used for all line voltages, its primary side must be wired appropriately. The table below shows what to do for the various line voltages encountered:

Transformer Primary (All Line Voltages)

Black wire	J18
Blue wire(s)	J23 and/or J26
White wire	J16
Brown wire	J19
Orange wire	J15
Power Switch	
Brown wire	J14

Primary Components	100 VAC	120 VAC	220 VAC	240 VAC
Power switch Brown wire	100/220 J25	120/240 J22	100/220 J25	120/240 J22
Brown jumper wire (from J20)	100/120 J37	100/120 J37	220/240 J38	220/240 J38
Blue jumper wire (from J17)	100/120 J40	100/120 J40	220/240 J39	220/240 J39
Fuse installed (1, Slo-blo)	0.25 Amp 3AG (F1)	0.25 Amp 3AG (F1)	0.125 Amp 20 mm (F2)	0.125 Amp 20 mm (F2)

The AC line voltage comes in through an IEC connector on the rear panel. It is filtered by capacitors C149 and C150, and line choke L1. The hot side passes through fuse F1 or F2 and goes to the power switch located on the front panel. The return from the power switch is connected to the appropriate transformer primary winding(s). Two varistors (VR1 & VR2) provide overvoltage protection for the transformer primary windings.



120VConnections

The secondary windings are connected in the following manner:

Transformer Secondary	**±15 VDC**	**+5 VDC**
Red wires	J21 & J28	
Yellow wires	J24 & J27	
Green wires		J31 & J32
Grey wires		J29 & J30

The ±15 volt supplies are created using CR34 - CR37 in a full-wave center tap configuration. C156 and C157 provide high frequency filtering. The positive unregulated voltage develops across C151, while the negative unregulated voltage is across C153. Voltage regulators U61 and U62 are used for supply regulation and short circuit protection. CR38 and CR41 protect the voltage regulators from being reverse biased. In addition, a path is provided for reverse polarity voltage spikes by CR39 and CR40. Bypass capacitors (C152, C154) are found at the regulator outputs. The ±15 volt supplies can produce +15 VDC at 150 mA and -15 VDC at 150 mA for the LXP-15's analog circuitry.

The +5 volt supply is also created by a full-wave center tap configuration. CR44 and CR45 create the unregulated voltage (+5VUNREG) across C158 and C159. High frequency filtering is provided by C160 and C161. +5VUNREG is applied to the voltage regulator (U63), the front panel display bright/contrast circuitry (P5, Q6, C122), the power fail/reset circuitry (FB14), and the battery backup circuitry (Q10, R138). Supply regulation and short circuit protection are provided by U63. CR42 protects the voltage regulator from being reverse biased, and CR43 provides a path for negative voltage spikes. C155 is a bypass capacitor for the output of U63. The +5 volt supply is capable of producing +5 VDC at 1 Amp for the LXP-15's digital circuits.

±5.1 volt supplies are required by a 74HC4053 analog switch (U7). 5.1 volt zener diodes are connected in series with resistors (+5.1V: CR8, R40; -5.1V: CR7, R41) to the ±15 volt supplies to create the ±5.1 volt supplies. C35 - C38 are bypass capacitors.

+4.7 volts is supplied to the 74HCT14 inverter (U53) to provide extended operation during power down conditions. A schottky diode (CR23) drops the +5 volt supply to +4.7 volts, and prevents C133 from discharging when the +5 volt supply starts dropping. R124 insures a minimum current is drawn through the diode for an insignificant voltage drop. C134 is a bypass capacitor.

Bypass capacitors are shown on the bottom of the power supply schematic for the various analog and digital ICs used in the LXP-15. These capacitors are located near their associated ICs.

LXP-15 Signal Descriptions

Analog

AN0-6 ADC analog inputs 0-6 (AN7 is unused)

HOLDIN Signal applied to Input Hold Circuitry

MAEN/ Left channel mix MDAC enable

MAIN Left channel Wet output applied to Wet/Dry mix MDAC

MASEL Left channel mix MDAC select signal for Dual MDAC U14

MAWR/ Left channel mix MDAC data Write signal

MBEN/ Right channel mic MDAC enable

MBIN Right channel Wet output applied to Wet/Dry mix MDAC

MBSEL Right channel mix MDAC select signal for Dual MDAC U12

MDACA<0:7> Left channel MDAC data bus

MDACB<0:7> Right channel MDAC data bus

MDWR/ Right channel mix MDAC data write signal

MUTE Output mute control signal

RETINL Left channel return from input level control

RETINR Right channel return from input level control

RETOUTL Left channel return to output level control

RETOUTR Right channel return to output level control

SNDINL Left channel send to input level control

SNDINR Right channel send to input level control

SNDOUTL Left channel send to output level control

SND OUTR Right channel send to output level control

A/D D/A Conversion

ADCDE/ Analog control ADC data output enable signal

DAC<0:15> Audio DAC data lines 1-15

DATA Audio A/D comparator signal

EOC Analog control ADC end of conversion signal

START Analog control ADC start conversion signal

Reset/Battery Backup

MRST/ Master Z80 reset

RCE Nonvolatile RAM power up/down chip enable

SRST/ Slave Z80 reset

VRAM Nonvolatile RAM Vcc

ZRST UART reset signal

ZRST/ Z80 support circuitry reset

Master Z80

MADR<0:15> Master Z80 address lines 0-15

MDB<0:7> Master Z80 data lines 0-7

MINT/ Master Z80 interrupt

MIORQ/ Master Z80 I/O request

MM1/ Master Z80 M1 cycle signal

MMREQ/ Master Z80 memory request

MRD/ Master Z80 read

MWAIT/ Master Z80 wait signal

MWR/ Master Z80 write

PLUP Pull up resistor for unused inputs

Master Memory I/O Decode

ROM/ ROM enable

RAMA/ Master RAM A (U44) enable

RAMB/ Master RAM B (U43) enable

IOEN2/ I/O enable for MSYNC and LCDCI signals

MSREQ Master request for Slave bus

BIO Bank switch I/O select signal

IOEN I/O enable for U29 I/O decoder

MSYNC Master sync request signal

LCDCI LC display data/control port enable

CONT/ Control port enable signal

UART/ UART enable

STATUS/ Status byte enable

ENCEN/ Encoder status input enable

BANK ROM bank select bit

MIDI Signals

MIDICLK/ 500kHz MIDI clock inout

MIDIIN MIDI data input

MIDIOUT MIDI data output

Clocks

UCLK 2MHz UART clock

WC/ Word clock

WCE/ Extended word clock

ZCLK 4MHz Z80 clock

Slave Z80

SADR<0:13> Slave Z80 address bus

SDB<0:7> Slave Z80 fdata bus

SIORQ/ Slave Z80 I/O request

SM1 Slave Z80 M1 signal

SMREQ/ Slave Z80 memory request

SRD/ Slave Z80 data read

SRTS/ Slave Z80 reset

SWAIT/ Slave Z80 wait

SWR/ Slave Z80 data write

Slave Bus Decoder

ACC/ Master access grant to slave bus

LEX/ Lexichip WCS enable

LRADR<0:13> Lexichip/Slave RAM address bus

LRCB Lexichip/Slave RAM control bus (LRWR/ and LRRD/)

LRRD/ Lexichip/Slave RAM data read

LRWR/ Lexichip/Slave RAM data write

MCB Master Z80 control bus (MRD/ and MWR/)

SRAM/ Slave RAM enable

I/O Interface Hardware

BKLT LC display backlight (intensity) control

DISP<0:7> LC display data bus

E LC display enable

ENCA<0:3> Encoder A (Adjust Knob) data bus

ENCB<0:3> Encoder B (Page Knob) data bus

HR<0:3> Headroom LED signals

LCDG LC display ground

LCDV+ LC display Vcc

LCDVO LC display contrast voltage (same as VO+)

PBI<0:2> Pushbutton matrix input signals

PBO<0:1> Pushbutton matrix output signa;ls

RS LC display control register select

R/W LC display read/write signal

VO+ LC display contrast voltage

Lexichip

CAS/ DRAM column address strobe

CAS1 Conditioned DRAM column address strobe

DAB<0:15> Digital audio bus

DEG0 Left channel conversion deglitch

DEG1 Right channel conversion deglitch

MA<0:8> Lexichip memory address lines

RAS/ DRAM memory row address strobe

SAMP Input conversion sample/hold signal

WE/ Lexichip data write enable

WE1 Conditioned Lexichip data write enable

4

Specifications

Specifications

Audio Inputs (2)
Level: -26 dBu minimum (0 dBu = 0.775 Vrms)
Impedance: Stereo: 50 kΩ, unbalanced
Mono: 25 kΩ unbalanced
Connectors: 1/4" tip/sleeve phone jacks
(L or R may be used for mono input)

Audio Outputs (2)
Level: +4 dBu nominal, +8 dBu max into 600Ω
+14 dBu maximum into >10kΩ
Impedance: 600Ω unbalanced
Connectors: 1/4" tip/sleeve phone jacks

Mute Protection
removes unwanted transients during power up/down or any power interruption

Static Protection

Frequency Response
Wet: 20 Hz to 15 kHz +1.0/-1.5 dB
Dry: 20 Hz to 20 kHz ±0.1 dB

Dynamic Range
85 dB typical, 20 Hz to 20 kHz bandwidth

Total Harmonic Distortion and Noise
Wet: <0.02% at 1 kHz
Dry: <0.01% at 1 kHz

Encoding
16-bit linear PCM

Sampling Frequency
31.25 kHz

Memory
128 presets with 128 user registers available

Dynamic MIDI®
5-pin DIN connectors provided for MIDI IN, MIDI OUT, and MIDI THRU

Controller Inputs
Five 1/4" tip/ring/sleeve phone jack inputs provided for connection to any on/off toggle switch or analog voltage controller

Signal Level Indicators
Four signal level LED indicators, including processed signal overload

Front Panel Display
Two lines of 40 alphanumeric characters each, backlit liquid crystal display

Front Panel Controls
Input Level Adjust
Output Level Adjust
Page knob: used for selecting 16 display pages
View button: used for viewing additional display pages
Adjust knob: used for editing parameters
Soft switches (5): used for assigning Adjust knob parameters
Power Switch

RFI Shielding
Complies with FCC Class A requirements for computer equipment

Safety Approvals
CLA approval pending
CSA approval pending
VDE approval pending

Power Requirements
100/120/220/240 VAC 50-60 Hz 20W

Dimensions
19.0"W x 1.75"H x 13.9"D
(483 x 45 x 353mm)
Conforms to 19" rack mount standard, 1U high

Weight
12.0 lbs (5.5 kg)
Shipping Weight 14.0 lbs (6.4 kg)

Shipping materials meet or exceed Project 1A of the National Safe Transit Association (NSTA) packaged-product specifications: vibration test, drop test, static compression test.

Environment
Operating Temperature: 32° to 95°F (0° to 35° C)
Storage Temperature: -22° to 167°F (-30° to 75°C)
Humidity: 95% maximum without condensation

Specifications subject to change without notice.

5

Parts List

Parts List
MAIN BOARD

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
CARBON FLM RES				
202-00496	RES,CF,5%,1/2W,2.2 OHM	1		R111
202-00508	RES,CF,5%,1/4W,33 OHM	1	09/23/94•	R148
202-00514	RES,CF,5%,1/4W,100 OHM	9		R30,34,68,73,78,81,99,108,109
202-00517	RES,CF,5%,1/4W,200 OHM	1		R110
202-00518	RES,CF,5%,1/4W,220 OHM	5		R112,113,115,116,122
202-00520	RES,CF,5%,1/4W,270 OHM	1		R123
202-00521	RES,CF,5%,1/4W,330 OHM	21		R56-59,89,90,97,98, R102-107,118-121,139,145,146
202-00524	RES,CF,5%,1/4W,470 OHM	3		R7,26,28
202-00525	RES,CF,5%,1/4W,510 OHM	3		R31,35,140
202-00529	RES,CF,5%,1/4W,1K OHM	5		R132,133,136-138
202-00533	RES,CF,5%,1/4W,2K OHM	2		R40,41
202-00534	RES,CF,5%,1/4W,2.2K OHM	2		R114,117
202-00535	RES,CF,5%,1/4W,2.4K OHM	1		R144
202-00542	RES,CF,5%,1/4W,4.7K OHM	7	•11/08/94	R70,74,76,77,79,82,100
202-00542	RES,CF,5%,1/4W,4.7K OHM	2	11/08/94•	R76,77
202-00543	RES,CF,5%,1/4W,5.1K OHM	3		R63,66,143
202-00549	RES,CF,5%,1/4W,10K OHM	15		R84-88,91-96,131,134,135,142
202-00553	RES,CF,5%,1/4W,15K OHM	1		R69
202-00555	RES,CF,5%,1/4W,20K OHM	1		R141
202-00559	RES,CF,5%,1/4W,30K OHM	2		R60,64
202-00562	RES,CF,5%,1/4W,39K OHM	2		R6,72
202-00570	RES,CF,5%,1/4W,100K OHM	1		R128
202-00576	RES,CF,5%,1/4W,200K OHM	5		R71,75,80,83,101
202-00579	RES,CF,5%,1/4W,470K OHM	4		R32,33,36,37
202-00580	RES,CF,5%,1/4W,1M OHM	1	09/23/94•	R147
202-10779	RES,CF,5%,1/4W,910 OHM	5	11/08/94•	R70,74,79,82,100
METAL FLM RES				
203-00456	RES,MF,1%,1/4W,1.00K OHM	1		R129
203-00457	RES,MF,1%,1/4W,1.50K OHM	3		R19,45,47
203-00459	RES,MF,1%,1/4W,2.00K OHM	9		R2,3,38,39,42,43,49,55,126
203-00465	RES,MF,1%,1/4W,6.49K OHM	2		R51,53
203-00467	RES,MF,1%,1/4W,7.15K OHM	1		R16
203-00468	RES,MF,1%,1/4W,7.50K OHM	7		R11-13,21,23,24,27
203-00471	RES,MF,1%,1/4W,10.0K OHM	10		R5,8,9,15,61,62,65,R67,125,130
203-00480	RES,MF,1%,1/4W,15.0K OHM	2		R20,22
203-00482	RES,MF,1%,1/4W,20.0K OHM	2		R4,10
203-00487	RES,MF,1%,1/4W,30.1K OHM	1		R1
203-01142	RES,MF,1%,1/4W,39.2K OHM	1		R127
203-01489	RES,MF,1%,1/4W,499 OHM	2		R25,29
203-01490	RES,MF,1%,1/4W,3.09K OHM	1		R17
203-02010	RES,MF,1%,1/4W,4.87K OHM	2		R50,52
203-02611	RES,MF,1%,1/4W,5.62K OHM	6		R14,18,44,46,48,54
NETWORK RES				
205-05638	RES,NET,SIP,2%,BUS EL,10KX9	2		RP1,2
ELECTROLYT CAP				
240-00608	CAP,ELEC,2.2uF,50V,RAD	2		C7,138
240-00613	CAP,ELEC,22uF,25V,RAD	13		C36,37,51,57,67,70,72,73,117, C122,144,152,154
240-05764	CAP,ELEC,330uF,25V,RAD,LO-PRO	1		C155
240-06096	CAP,ELEC,10uF,25V,RAD,NON-POL	13		C3,11,16,18,22,28,29, 40, 44, 48, C50,65,66

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
240-06738	CAP,ELEC,1000uF,35V,RAD,105C	2		C151,153
240-07335	CAP,ELEC,47uF,25V,RAD,NON-POL	2		C59,63
240-07843	CAP,ELEC,2200UF,25V,RAD,105C	2		C158,159
PCRB/PP CAP				
244-01151	CAP,PP,1000pF,2.5%	1		C6
244-03919	CAP,MYL,.015uF,250V,INTL APP	2		C149,150
244-06883	CAP,MYL,.01uF,5%,RAD	3		C17,47,49
CERAMIC CAP				
245-03609	CAP,CER,.1uF,50V,Z5U,AX	86	•09/23/94	C4,5,8,9,13,14,20,21,25,26,32,34, C35,38,41,42,45,46,52,54-56, C61,62,68,69,71,74,76,78,80-86, C88,90-98,100-106,108-116, C118-121,127-132,134,135,137, C140,142,143,145-148,156, C157,160
245-03609	CAP,CER,.1uF,50V,Z5U,AX	87	09/23/94•	C4,5,8,9,13,14,20,21,25,26,32,34, C35,38,41,42,45,46,52,54-56,61, C62,68,69,71,74,76,78,80-86,88, C90-98,100-106,108-116,118-121, C127-132,134,135,137,140,142, C143,145-148,156,157,160,161
245-03610	CAP,CER,.01uF,100V,Z5U,AX	7		C30,75,77,79,87,89,107
245-03867	CAP,CER,10pF,100V,COG,10%,AX	9	09/23/94•	C10,12,15,19,23,53,58,60,64
245-03867	CAP,CER,10pF,100V,COG,10%,AX	11	•09/23/94	C10,12,15,19,23,53,58,60,64, C99,139
245-03868	CAP,CER,33pF,100V,COG,10%,AX	3	•09/23/94	C24,27,99
245-03868	CAP,CER,33pF,100V,COG,10%,AX	2	09/23/94•	C24,27
245-03869	CAP,CER,100pF,100V,COG,10%,AX	9		C1,2,31,33,123-126,141
245-03870	CAP,CER,150pF,100V,COG,10%,AX	1		C136
245-07344	CAP,CER,470pF,100V,COG,10%,AX	2		C39,43
INDUCTORS				
270-00779	FERRITE,BEAD	14		FB1-14
270-06940	INDUCTOR,COMMON MODE,1mH,1A	1		L1
DIODES				
300-01024	DIODE,ZENER,3.3V,1N746	1		CR26
300-01029	DIODE,1N914 AND 4148	25		CR2-6,9-22,28-33
300-01030	DIODE,1N4004 AND 4005	10		CR34-43
300-01154	DIODE,ZENER,5.1V,1N751	3		CR1,7,8
300-02401	DIODE,BAR 35,SCHOTTKY,LOW VF	4		CR23-25,27
300-03546	DIODE,BRIDGE,2A,200V	1		CR44
TRANSISTORS				
310-01007	TRANSISTOR,2N3904	3		Q7,9,10
310-01008	TRANSISTOR,2N3906	2		Q3,8
310-01647	TRANSISTOR,2N4401	2		Q4,5
310-01238	TRANSISTOR,MJE-180	1		Q6
310-06612	TRANSISTOR,J108	2		Q1,2
DIGITAL/CMOS IC				
330-04260	IC,DIGITAL,74HCT04	1		U30
330-04271	IC,DIGITAL,74HCT273	2		U27,60
330-04294	IC,DIGITAL,74HCT138	1		U29
330-04509	IC,DIGITAL,74HC74	1	09/23/94•	U64
330-04563	IC,DIGITAL,74HCT02	1		U21
330-04567	IC,DIGITAL,74HCT32	1		U26
330-04569	IC,DIGITAL,74HCT157	4		U47,48,50,51

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
330-04572	IC,DIGITAL,74HCT245	2		U28,31
330-04589	IC,DIGITAL,74HCT14	1		U53
330-04675	IC,DIGITAL,74F08	1		U20
330-04763	IC,DIGITAL,74HCT161	2		U58,59
330-06204	IC,DIGITAL,LEXICHIP 1	1	09/23/94•	U25
330-06878	IC,DIGITAL,74HCT541	4		U22,23,41,42
330-06879	IC,DIGITAL,74HCT574	2		U18,19
330-09350	IC,DIGITAL,LEXICHIP 2A	1	•09/23/94	U25
LINEAR IC				
340-00725	IC,LINEAR,LM311	1		U16
340-01183	IC,LINEAR,LF 356	1		U1
340-01566	IC,LINEAR,LF353,DUAL OP AMP	3		U2,8,13
340-04036	IC,LINEAR,7815(LM340T-15),BENT	1		U61
340-04037	IC,LINEAR,7915(LM320T-15),BENT	1		U62
340-05945	IC,LINEAR,LM393	1		U56
340-06036	IC,LINEAR,uPC4570,DUAL OP AMP	5		U3,5,6,11,15
340-07270	IC,LINEAR,7805(LM340T-5),BENT	1		U63
INTERFACE IC				
345-06037	IC,INTER,82C51A	1		U57
SS SW IC				
346-06896	IC,SS SWITCH,74HC4053	1		U7
MEMORY IC				
350-04434	IC,DRAM,64KX4,120NS	4		U32,34,36,38
350-08261	IC,ROM,27C512,LXP-15,V1.32	1	05/24/94	U45 - LXP-15 ONLY
350-08262	IC,GAL,16V8A,LXP-15,MSTR,V1.10	1		U40-unprogram GAL 350-08211
350-08263	IC,GAL,16V8A,LXP-15,SLAVE,V1.2	1		U54-unprogram GAL 350-08211
350-08570	IC,SRAM,6264,8KX8,100NS,LO PWR	3		U43,44,49
350-10275	IC,ROM,27C512,LXP-15,V2.00	1	•05/24/94	U45 - LXP-15II ONLY
CONVERTER IC				
355-02903	IC,CONVERTER,ADC 0809	1		U24
355-06038	DAC,PCM54HP	1		U17
355-07542	DAC,AD7628,CMOS,2X8BIT,MDAC	2		U12,14
SEMICONDUCTORS				
360-01612	SEMICOND,VARISTOR	2		VR1,2
MICROPROC IC				
365-04284	IC,uPROC,Z80,CMOS,4MHz	2	•01/22/93	U46,55
365-04834	IC,uPROC,Z80B,CMOS,6MHZ	2	01/22/93•	U46,55
OPTO ISLTOR IC				
375-02247	IC,OPTO-ISOLATOR,6N138	1		U52
MODULES				
380-06039	MOD,LPF,LC,7P,15KHz	3		U4,9,10
CRYSTALS				
390-06647	CRYSTAL,16.000 MHZ,.01%	1		Y1

* Early units containing V1.00 software were found to have an anomaly in the Delay/Reverb algorithm: The reverb decay parameter should shut off the wet input signal when entering the maximum decay setting (infinite) to provide infinite reverberation. On exiting infinite reverb, the wet input should be restored. In V 1.10 the wet input level is not always restored when exiting from the infinite reverb setting, and reverb is not always infinite when decay is set to maximum. Software Version 1.20 contains a correction.

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
FUSES				
440-00860	FUSE,3AG,SLO-BLO,.250 AMP	1		F1 - 120V ONLY
440-02347	FUSE,5X20MM,SLO-BL0,.125AMP	1		F2 - 220V, 240V ONLY
440-02348	FUSE,5X20MM,SLO-BLO,.250AMP	1		F2 - 100V ONLY
BATTERIES				
460-04285	BAT,LITH,3V@160mAh,VERT COIN	1		BAT1
490-02356	CONN,JUMPER,.1X025,2FCG	1		W4
490-09182	CONN,QDC,FEM,INS,.187X.032	3		
PC MNT CONN				
510-02106	1/4" PHONE JACK,PCRA,3C,SWITCH	9		J1-9
510-02671	CONN,POST,100X025,HDR,3MC,GOLD	1		W4
510-04286	CONN,CIRC DIN,5FC@180DEG,PCRA	3	J10-12	
510-06168	CONN,POST,079,HDR,15MC	3		P1,3,4
510-07888	CONN,AC,3MC,PCRA,IEC,6A	1		J13
510-07895	CONN,POST,100X025,HDR,14MCG,LK	1		P2
510-07896	CONN,156X45,HDR,2MCG,STR,LK	1		P5
510-08255	CONN,QDC,MALE,PC MNT,.187X.032	6		NEAR POWER SWITCH
SOCKETS				
520-00946	IC SCKT,40 PIN,PC,LO-PRO	2	•11/08/94	U46,55
520-01361	IC SCKT,20 PIN,PC,LO-PRO	4	•11/08/94	U12,14,40,54
520-01361	IC SCKT,20 PIN,PC,LO-PRO	2	11/08/94•	U40,54
520-01458	IC SCKT,28 PIN,PC,LO-PRO	7	•11/08/94	U17,24,43-45,49,57
520-01458	IC SCKT,28 PIN,PC,LO-PRO	1	11/08/94•	U45
520-02177	IC SCKT,18 PIN,PC,LO-PRO	4	•11/08/94	U32,34,36,38
520-06184	IC SCKT,PLCC,84 PIN	1		U25
TIE CABLES				
530-02489	TIE,CABLE,NYL,.1"X4"	5		XFMR WIRES
FEET				
541-00781	BUMPER,FEET,3-M #SJ5018	3		
ELECTRONIC HDWE				
600-00871	FUSE CLIP,1/4",PC	1	•05/19/92	F1
600-00871	FUSE CLIP,1/4",PC	2	05/19/92•	F1
600-02227	FUSE CLIP,20MM,PC	1	•05/19/92	F2
600-02227	FUSE CLIP,20MM,PC	2	05/19/92•	F2
INSUL/SPACRS				
630-00952	INSUL,SEMI,BUSHING,TO-220	3		H/S TO MAIN BD
630-03969	INSUL,COVER,AGC,FUSE	1		F1
630-07339	INSUL,SEMI,SIL RUB,TO-220SHORT	3		H/S TO MAIN BD
630-08045	INSUL,COVER,5X20MM FUSE	1		F2
MACHINE SCREWS				
640-01706	SCRW,4-40X3/8,PNH,PH,ZN	5		H/S TO MAIN BD (3); AC CONN TO MAIN BD (2)
NUTS				
643-01732	NUT,4-40,KEP,ZN	5		AC CONN TO MAIN BD (2); H/S TO MAIN BD (3)
WIRE				
670-02037	WIRE,28AWG,KYNAR,GRN	3	08/28/92•01/20/94	(1) 1.2" LONG; (1) 1.25" LONG (1) 1.30" LONG

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
670-03001	WIRE,JMP,22AWG,0.6",TEF,WHT	1	01/20/94•11/08/94	
670-04918	WIRE,JMP,22AWG,0.4",TEF,WHT	1	•11/08/94	U46 pin29 TO U45 pin 14
670-10068	WIRE,JMP,22AWG,0.7",TEF,WHT	1	01/20/94•11/08/94	
670-10069	WIRE,JMP,22AWG,0.9",TEF,WHT	1	01/20/94•11/08/94	
PRE-CUT WIRE				
675-08256	WIRE,22G,BLU,2.5",.187QDC/ST	1		"RED" ON NOMEN (NEAR PWR SW)
675-08257	WIRE,22G,BRN,2.5",.187QDC/ST	1		"BRN" ON NOMEN (NEAR PWR SW)
675-08258	WIRE,22G,BRN,12",.187QDC/ST	1		PWR SWITCH
675-08259	WIRE,22G,BRN,12",.187QDCX2	1		PWR SWITCH
675-08272	WIRE,18G,GRN/YEL,3",#6RING/SS	1		J13
HEAT SINKS				
704-07829	HEATSINK,LXP-15	1		
PLASTICS				
720-02751	TAPE,FOAM,DBL-STK,1/8THX3/4W	1		Y1

FRONT PANEL MAIN BOARD ASSEMBLY (X & II, after 6/7/91) (025-08896)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
CARBON FLM RES				
202-00524	RES,CF,5%,1/4W,470 OHM	4		R8-11
202-00534	RES,CF,5%,1/4W,2.2K OHM	4		R4-7
202-00549	RES,CF,5%,1/4W,10K OHM	3		R3,12,13
ELECTROLYT CAP				
240-00613	CAP,ELEC,22uF,25V,RAD	1		C1
DIODES				
300-01029	DIODE,1N914 AND 4148	2		CR1,2
TRANSISTORS				
310-01007	TRANSISTOR,2N3904	4		Q1-4
LEDS				
430-03624	LED,RED,RECT,.22X.125,DIFFUSED	1	07/01/92•	CR3
430-03896	LED,GRN,RECT,.197X.079	3	•07/01/92	CR4-6
430-03898	LED,RED,RECT,.197X.079	1	•07/01/92	CR3
430-09401	LED,GRN,RECT,.22X.125,DIFFUSED	3	07/01/92•	CR4-6
PSH BUT SWITCH				
453-08183	SW,PBM,1P1T,6MM SQX5MM H,150GF	6		SW1-5,8
CABLES/CORDS				
680-08892	CABLE,SCKT/BICONN,15C,7.5"	1		P3

FRONT PANEL GAIN BOARD ASSEMBLY (LXP15X & LXP15II, after 6/7/91)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
POTENTIOMETERS				
200-06035	POT,RTY,PC,50KAX2,6MM/FLT,16MM	2	•06/21/93	R1,2
200-09545	POT,RTY,PC,50KAX2,6MMFL,16,17L	2	06/21/93•	R1,2
CABLES/CORDS				
680-07897	CABLE,079,SCKT/BICONN,15C,4.0"	1		P1

FRONT PANEL ENCODER BOARD ASSEMBLY (LXP15X & LXP15II, after 6/7/91)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
CARBON FLM RES				
202-00549	RES,CF,5%,1/4W,10K OHM	8		R14-21
SWITCHES				
452-08891	SW,RTY,GRAY CODE,16 POS,PVB	2		SW6,7
CABLES/CORDS				
680-08892	CABLE,SCKT/BICONN,15C,7.5"	1		P4

LXP-15 FRONT PANEL MECHANICAL (LXP15X & LXP15II, after 6/7/91)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
DISPLAY/IND/LED				
430-07847	DISP,LCD,40X2,POS,12:00,LED,AM	1		
ROCKER SWITCH				
454-03900	SW,ROCKER,1P1T,6A@250V,BLK,"0"	1		
KNOBS/CAPS				
550-04212	KNOB,1.00,6MM/ROUND,BLK	1		
550-08254	KNOB,.66,6MM,FL,BLK/BOT,WHT LN	3	•07/21/92	
550-08889	BUTTON,.15X.60,BLK	6		
550-09118	KNOB,17MM,6MM/FLT,BLK/WHT LN	3	07/21/92•	
INSUL/SPCRS				
640-01841	SCRW,2-56X1/4,PNH,PH,ZN	4		LCD TO FP MAIN BD
640-04339	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	4		FP MAIN BD TO INSERT
NUTS				
643-01728	NUT,6-32,KEP,ZN	2		CHASSIS INSERT TO FP
643-01855	NUT,2-56,HEX,ZN	4		LCD TO FP MAIN BD
WASHERS				
644-02265	WSHR,FL,.297IDX.437ODX.060THK	2	07/21/92•06/21/93	R1,2
644-07893	WSHR,FL,.427IDX.550X.035THK,ZN	2	•07/21/92	SW6,7
644-07893	WSHR,FL,.427IDX.550X.035THK,ZN	4	07/21/92•	SW6,7
644-08899	WSHR,FL,#2CLX.186ODX.03THK,NYL	4		LCD TO FP MAIN BD

CABLES				
680-08356	CABLE,ASSY,2C,22G,7",SS/HSG	1		LCD
CHASSIS INSERTS				
700-08885	CHASSIS,INSERT,FP,LXP-15X	1		
PANELS				
702-08886	PANEL,FRONT,LXP-15X	1		
LENS/PLATE/PANL				
703-08887	PANEL,OVLY,FRONT,LXP-15X	1	•05/24/94	LXP-15 ONLY
703-10276	PANEL,OVLY,FRONT,LXP-15II	1	05/24/94•	LXP-15II ONLY

FRONT PANEL MAIN BOARD ASSEMBLY (before 6/7/91)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
POTENTIOMETERS				
200-06035	POT,RTY,PC,50KAX2,6MM/FLT,16MM	2	•06/21/93	R1,2
200-09545	POT,RTY,PC,50KAX2,6MMFL,16,17L	2	06/21/93•	R1,2
CARBON FLM RES				
202-00524	RES,CF,5%,1/4W,470 OHM	4		R3-6
202-00534	RES,CF,5%,1/4W,2.2K OHM	4		R7-10
202-00549	RES,CF,5%,1/4W,10K OHM	3		R11-13
NETWORK RES				
205-05638	RES,NET,SIP,2%,BUS EL,10KX9	1		RP1
ELECTROLYT CAP				
240-00613	CAP,ELEC,22uF,25V,RAD	1		C1
DIODES				
300-01029	DIODE,1N914 AND 4148	2		CR1,2
TRANSISTORS				
310-01007	TRANSISTOR,2N3904	4		Q1-4
ROTARY SWITCH				
452-07887	SW,RTY,GRAY CODE,16 POS	2		SW6,7
PSH BUT SWITCH				
453-07837	SW,PBM,2P2T,PCRA,LO-PRO	5		SW1-5
PC MNT CONN				
510-06568	CONN,POST,079,HDR,6MC	2		P2,5
FEET				
541-00781	BUMPER,FEET,3-M #SJ5018	1		
541-08377	BUMPER,FEET,STRIP,1/8X3/8X3/4L	1		
CABLES/CORDS				
680-07897	CABLE,079,SCKT/BICONN,15C,4.0"	3		P1,3,4

FRONT PANEL LED BOARD ASSEMBLY (before 6/7/91)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
DISPLAY/IND/LED				
430-03896	LED,GRN,RECT,.197X.079	3		CR4-6
430-03898	LED,RED,RECT,.197X.079	1		CR3
CABLES/CORDS				
680-07898	CABLE,079,SCKT/BICONN,6C,2.0"	1		P7

FRONT PANEL SWITCH BOARD ASSEMBLY (before 6/7/91)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
PSH BUT SWITCH				
453-07554	SW,PBM,1P1T,PC,1MM,TRAV	1		SW8
CABLES/CORDS				
680-07898	CABLE,079,SCKT/BICONN,6C,2.0"	1		P6

FRONT PANEL MECHANICAL (before 6/7/91)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
DISPLAY/IND/LED				
430-07847	DISP,LCD,40X2,POS,12:00,LED,AM	1		
ROCKER SWITCH				
454-03900	SW,ROCKER,1P1T,6A@250V,BLK,"0"	1		
KNOBS/CAPS				
550-04212	KNOB,1.00,6MM/ROUND,BLK	1		
550-07575	BUTTON,.335X.592,BLK	1		
550-07836	BUTTON,.39X.22X.44,BLK	5		
550-08254	KNOB,.66,6MM,FL,BLK/BOT,WHT LN	3		
INSUL/SPCRS				
630-08788	SPCR,2-56X3/8,5/32HEX,NYL	4		LCD TO FP
MACHINE SCREWS				
640-04339	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	4		FP LED BD TO FP (2), FP SW BD TO FP (2)
640-08789	SCRW,2-56X1/4,PNH,PH,NYL	4		LCD TO FP
WASHERS				
644-07090	WSHR,INT STAR,M2.7,ZN	1		
CABLES/CORDS				
680-08356	CABLE,ASSY,2C,22G,7",SS/HSG	1		LCD
PANELS				
702-07820	PANEL,FRONT,LXP-15	1		

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
LENS/PLATE/PANL				
703-07821	PANEL,OVLY,FRONT,LXP-15	1		

CHASSIS/MECHANICAL (all versions)

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
TRANSISTORS				
310-01238	TRANSISTOR,MJE-180,NPN	1		
TRANSFORMERS				
470-07889	XFORMER,POWER,15VA,UI75,INTL	1		
GROMMETS				
540-00874	GROMMET,9/16 OD,7/16 ID	2		CHAS SUPPORT
LUGS				
620-08252	LUG,PCB/#4CL	1		MAIN PCB - J11 MTG
INSUL/SPCRS				
630-03955	WSHR,SHLDR,3/16SHNK,#6CL,FBR	8		XFORMER MTG
630-07846	SPCR,PCB/FOOT,.250,NYL	1		PCB SUPPORT
630-08260	INSUL,SEMI,SIL RUB,TO-126	1		TO-126 TO CHAS SUPP
SPCR,NON-INSUL				
635-07841	SPCR,#4CLX3/8,5/16HEX,AL	1		TO-126
635-07848	SPCR,#6CLX.375ODX.25L,AL	2		
635-07848	SPCR,#6CLX.375ODX.25L,AL	2		XFRMR TO CHASSIS WRP
MACHINE SCREWS				
640-01710	SCRW,6-32X1/4,PNH,PH,ZN	6		FP SW BD TO CHAS SUPP
640-01713	SCRW,6-32X5/16,PNH,PH,ZN	2		HEATSINK TO CHAS WRP
640-02467	SCRW,4-40X7/8,PNH,PH,ZN	1		TO-126 TO CHAS SUPP
640-02812	SCRW,4-40X3/8,PNH,PH,BLK	8		DIN CONN TO CHAS WRP (6) AC CONN TO CHAS WRP (2)
THRD-FRM SCRW				
641-06575	SCRW,TAP,SW,6-32X1/4,THG,PH,BZ	18		CHAS SUP TO CHAS WRP (4); BOT CVR TO CHAS WRAP (7) TOP CVR TO CHAS WRAP (7)
NUTS				
643-01728	NUT,6-32,KEP,ZN	7		XFORMER (4); GND (1); HEATSINK TO CHAS WRAP (2)
643-01732	NUT,4-40,KEP,ZN	9		DIN CONN TO CHAS WRAP (6); AC CONN TO CHAS WRAP (2);
TO-126 (1)				
643-01734	NUT,8-32,KEP,ZN	4		CHAS WRAP TO FRONT PANEL
THREADLS FASTNR				
650-07551	RVT,SNAP-IN,.16DIA,NYL	4		PROT COVER
CHASSIS/MECH				
700-07825	COVER,TOP/BOTTOM,LXP-15	2		
700-07827	CHASSIS,WRAPAROUND,LXP-15	1		
700-07828	CHASSIS,SUPPORT,LXP-15	1		

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
PANELS				
702-07842	INSUL,GSKT,.40DX2@.87	1		
702-07845	COVER,PROTECTIVE,AC,LXP-15	1		
LENS/PLATE/PANL				
703-07823	PANEL,OVLY,REAR,LXP-15	1		
SHIPPING MAT				
541-00781	BUMPER,FEET,3-M #SJ5018	4		
630-08670	WSHR,FIN,#10,NYL,BLK	4		CABINET MTG HDWR
640-08671	SCRW,10-32X3/4,FH,PH,BLK	4		CABINET MTG HDWR
680-00841	CORD,POWER,NA/IEC,SVT,18/3,7'6	1		
680-08830	CORD,POWER,IEC,6A,2M.EURO	1		
730-07838	INSERT,FOAM,20X5X3	2		

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Service Bulletin Summary

Service Bulletin Summary

Service Bulletins which have been issued since the last printing of this manual are summarized here to assure completeness of material.

V1.31 Software Update

Installation of Version 1.31 software is recommended for any LXP-15 which exhibits the behavior described in the LXP-15 Owner's Manual Addendum, 070-09167, Rev 1.

Required Equipment and Documents
LXP-15 Update Kit: 021-09168
Contains:
- 1 070-09166 LXP-15 Update Installation Instructions, Software V1.31
- 1 070-09167 Owner's Manual Addendum
- 1 350-08261 IC, ROM 27C512, LXP-15V1.31
- 1 780-01925 IC Extractor Tool

CAUTION

THIS PROCEDURE WILL ERASE THE ENTIRE CONTENTS OF THE USER REGISTER AND REPLACE IT WITH A COPY OF THE ORIGINAL FACTORY-LOADED PRESETS. IF YOU HAVE SETUPS STORED IN THE USER REGISTER THAT YOU DON'T WANT TO LOSE, MAKE A RECORD OF THEM BEFORE INSTALLING V1.31 SOFWARE.

Possible Failure of JUNG POONG 50K ohm Rotary Pots

Failures of JUNG POONG 50K ohm rotary pots used as input and output level controls in early units have caused the following symptoms: "Scratchy" and/or clicking sounds at output when pots are turned and "explosive" sounds at output in reverb mode when pots are turned.

Although it is normal for pots to develop these symptoms with age and dirt accumulation, and not all JUNG POONG pots have exhibited the tendency to fail prematurely, Lexicon has replaced Part No. 200-06035, POT,RTY,50KAX2,6MM/FLT,16MM with Part No. 200-09545,POT,RTY,PC,50KAX2,6MMFL,16,17L. These pots are used at locations R1 and R2 on the FP GAIN BD ASSY, LXP-15X, 025-08897 and FP MAIN BD ASSY, LXP-15, 024-07863 (inactive).

Units exhibiting similar symptoms should have this part checked for failure.

Required Equipment and Documents
Technician's Tool Kit
LXP-15 Service Manual
2 Lexicon Part No. 200-09545 R1, R2

CAUTION

Observe Electrostatic Discharge (ESD) Precautions

Note that the new part has a different shaft length and, therefore, requires the removal of a washer (Lexicon Part No. 644-02265, WSHR, FL,. 297IDX. 437ODX. 060THK) for each pot, for assembly of the front panel. See appropriate assembly drawings.

Older front panels may require the addition of a washer, Lexicon Stock Part No. 644-07893, at the Page Knob rotary switch mounting (SW7). This will correct knob alignment variances when the new pots are installed.

Foot Pedal Input Circuit Modification

The LXP-15 footpedal inputs are designed for 50k ohm input. A lesser value pedal will not control the full range of a global parameter. Most commercially available foot pedals use 10k ohm pots. The LXP-15 footpedal input circuit can be modified to work correctly with these pedals by changing a resistor.

This modification should be performed by qualified technical personnel only. Damage caused by this modification may void the manufacturer's warranty.

Required Equipment and Documents

Soldering iron

1-5 910 ohm, 5%, 1/4 watt, carbon film resistors; Lexicon Part No. 202-10779

for modification of one or any combination of foot pedal inputs

CAUTION

Observe Electrostatic Discharge (ESD) Precautions

1. Power off the LXP-15 and unplug the power cord.
2. Locate and remove seven (7) screws on the top, and seven (7) screws on the bottom cover of the LXP-15. Remove the covers.
3. Change the following resistors from 4.7k ohms (5%, 1/4 watt, carbon film) to 910 ohm (5%, 1/4 watt, carbon film). Lexicon Part No. 202-10779.

   Foot pedal 1: R100 Foot pedal 2: R82 Foot pedal 3: R79
   Foot pedal 4: R74 Foot pedal 5: R70
4. Replace covers.

Problems noted with V2.0 Software Upgrades

Units with REV 1-4 motherboards may not initialize or may "lock up" at any point after the installation of V2 software. Corrective action includes:

Adding grounding jumpers to reduce the amount of ringing on the +5V and Ground lines in the Master Processor section of the PC board.

Verifing GALs at U40 and U54, and updating if necessary

This modification should be performed by qualified technical personnel only. Damage caused by this modification may void the manufacturer's warranty.

Required Equipment and Documents
Soldering iron
4 pcs. jumper wire, 22 AWG. (Lengths: 1.2", 1.25", 1.30", .4")
1 U40 GAL P/N 350-08262 (if necessary) V1.10
1 U54 GAL P/N 350-08263 (if necessary) V1.20 or V1.00, depending on letter code described later in this document.

CAUTION

Observe Electrostatic Discharge (ESD) Precautions

1. Power off the LXP-15 and unplug the power cord.
2. Locate and remove 7 screws on the top and 7 screws on the bottom cover. Remove the covers.

Install Wires:

Wire #1:

1. On the solder side of board install .4" jumper wire between pin 29 of U46, the master processor and pin 14 of U45, the EPROM.

Wire #2:

1. With 1.20" piece of wire, .25" trimmed off both ends, install one end of the wire into the via hole that is .2" directly below the south side of C119.
2. Install the other end into the south side of the via hole that is also used by C120.

Wire #3:

1. With 1.25" piece of wire, .25" trimmed off both ends, install one end of the wire into the via hole that is on the large width, heavy, ground track that is .7" below the south side of C120.

2. Install the other end into the via hole that is .1" above and .1" to the right of the via hole that is the south side of C120.

Wire # 4:

1. With 1.30" piece of wire, .25" trimmed off both ends, install one end of the wire into the via hole that is .1" to the left and .1" above the via hole referenced in instruction number 1 of wire #3.
2. Install the other end into the via hole that is .1" directly above the via hole that is referenced in instruction number 2 of wire #3.

Verify GAL Revisions

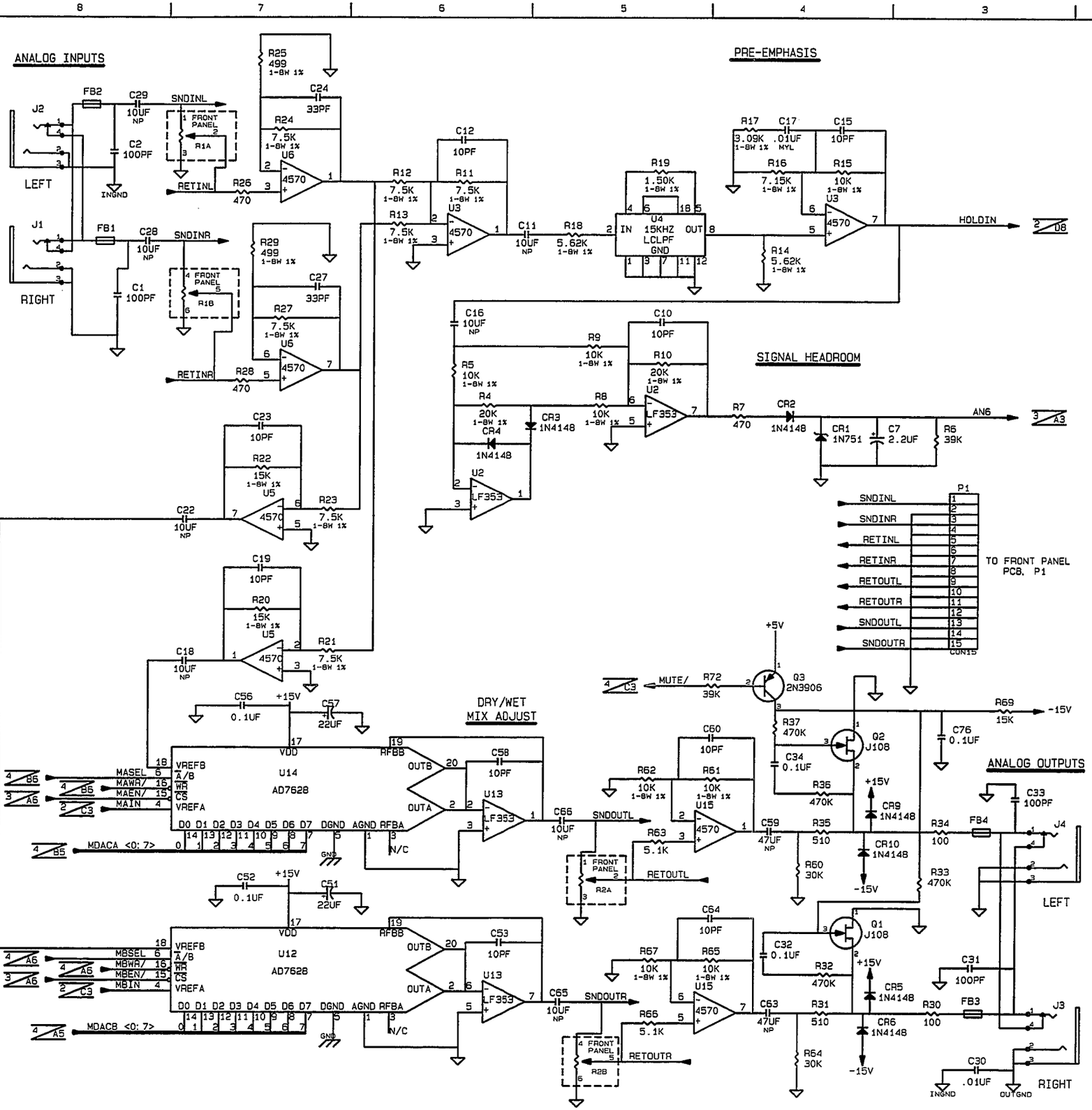
1. Verify that the GAL (20 pin socketed IC) located at U40 is V1.10 or higher. Lexicon P/N 350-08262.
2. Units with a "V" before the serial number, check that the GAL (20 pin socketed IC) located at U54 is V1.20 or higher. Lexicon P/N 350-08263
3. Units with a "K" before the serial number, check that the GAL located at U54 is V1.00 or higher.

7

Schematics and Assembly Drawings

The schematics contained in this service manual are the most current at the time of print. Units may contain component and layout differences depending on date of manufacture. Please refer to the list below as well as service bulletins contained in this manual revision for significant changes.

Reference	Description
V1.31 Bulletin	Main Bd. R1: value change from 30k ohm 5% carbon film type (P/N 202-00559) to 30.1kΩ 1% or 2% metal film type (P/N 203-00487); improve signal-to-noise
Main Bd.	CR45: deleted (P/N 300-01032), C161: deleted (P/N 245-03609) CR44: replaced (P/N 300-01032) with bridge diode (P/N 300-03546); change implemented - Rev 3 Main Bd.
S/W Upgrade Bulletin	May be required when upgrading older units to newer software versions or for intermittent loss of front panel controls referred to as "Lock-up".
Jung Poon Bulletin	Rotary Pot (R1, R2) manufacturer: JUNG POONG deleted from component spec (P/N 200-06035); Part replaced with (P/N 200-09545)
V1.32 Bulletin	no user fixes or enhancements, diagnostic enhancement only (refresh timing change for audio DRAM diagnostic).
Main Bd.	R70, 74 79, 82 & 100, 4.7k ohm (P/N 202-00542) can be changed to 910 ohm (P/N 202-10779) to change footpedal inputs from 50k ohm to 10k ohm.



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	D.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	AF 12/11/89	LDR 12/11/89
		MWH 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	AF 1/11/90	LDR 1/11/90
		MWH 1/11/90	DHS 1/11/90
2	CHANGED SHEETS 3, 6 AND 7 AS PER ECO# 900226-00	MWH 3/12/90	RWH 3/12/90
		AF 3/12/90	DHS 3/14/90
3	CHANGED DOC. CTL. BLK. & SHEETS 2, 5 & 8 PER ECO #900530-00	JV 6/20/90	RW 6/28/90
		AF 6/20/90	DHS 7/2/90
4	CHANGE DOC CTL BLK & SHEET 3, PER ECO 900927-01.	JV 10/12/90	RW 10/25/90
		SF 10/22/90	JV 6/20/90
5	CHANGED DOC CTL BLK & SHEET 3, PER ECO 900226-00-A.	JV 11/13/90	RW 11/13/90
		MWH 11/13/90	DHS 11 13 90
6	CHANGED DOC CTL BLOCK AND SHEET 2, PER ECO 910220-01	JV 3/3/91	RW 3/19/91
		DHS 3/7/91	DHS 3/7/91
7	CHANGED DOC CTL BLOCK AND SHEET 8, PER ECO 910329-00	JV 3/3/91	RWH 5/10/91
		SF 5/10/91	DHS 5/20/91
8	REDESIGN FOR LEXICHIP-2 (SHEETS 7, 8), ADD 9TH SHEET, ADD NOTE 7 PER ECO 940915-02. CHANGE RES VALUES (SHEET 2) PER ECO 941104-00.	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

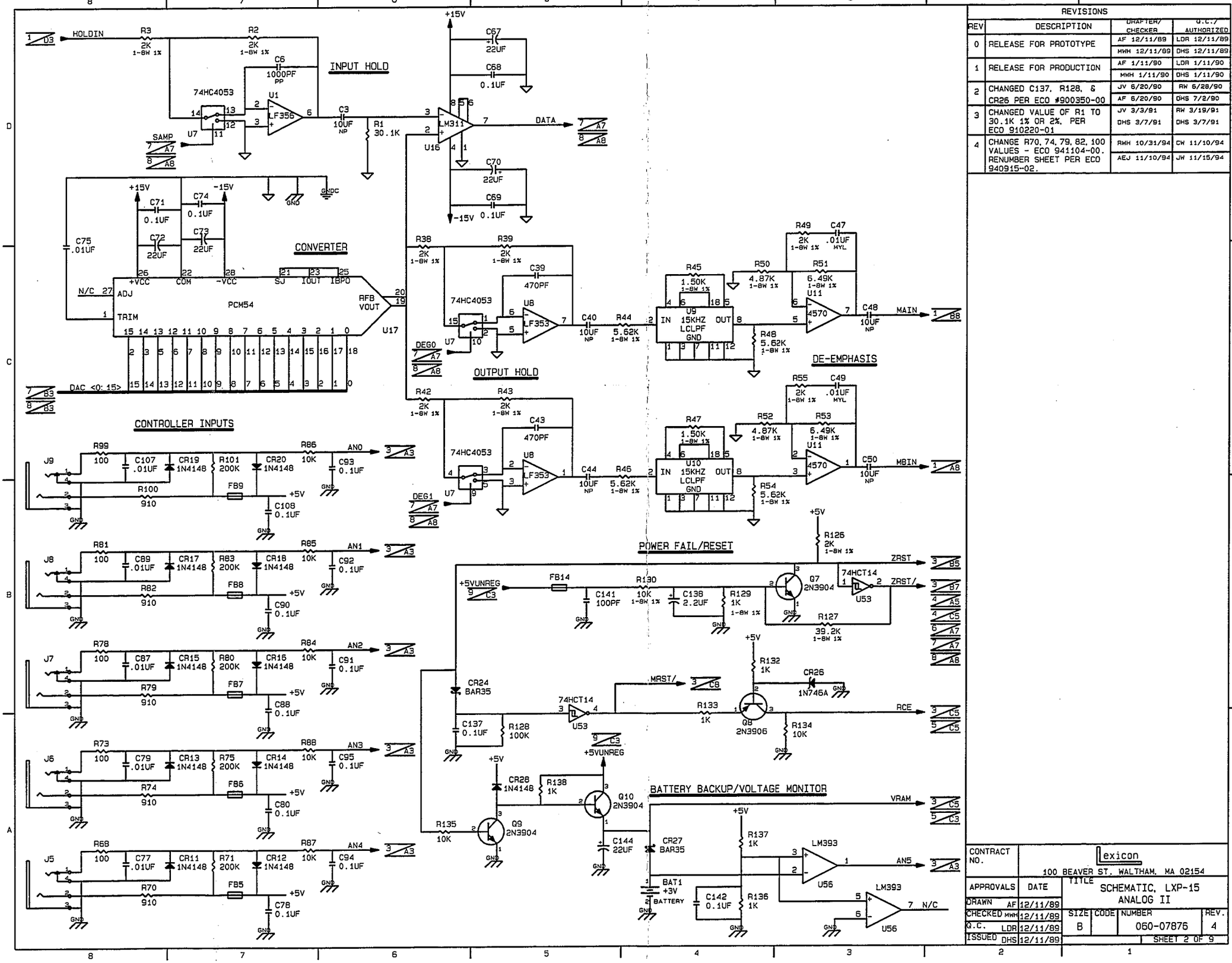
NOTES

1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION
7. THIS SCHEMATIC REPRESENTS PCBs: 710-07870 AND 710-10770

DOCUMENT CONTROL BLOCK: #060-07876

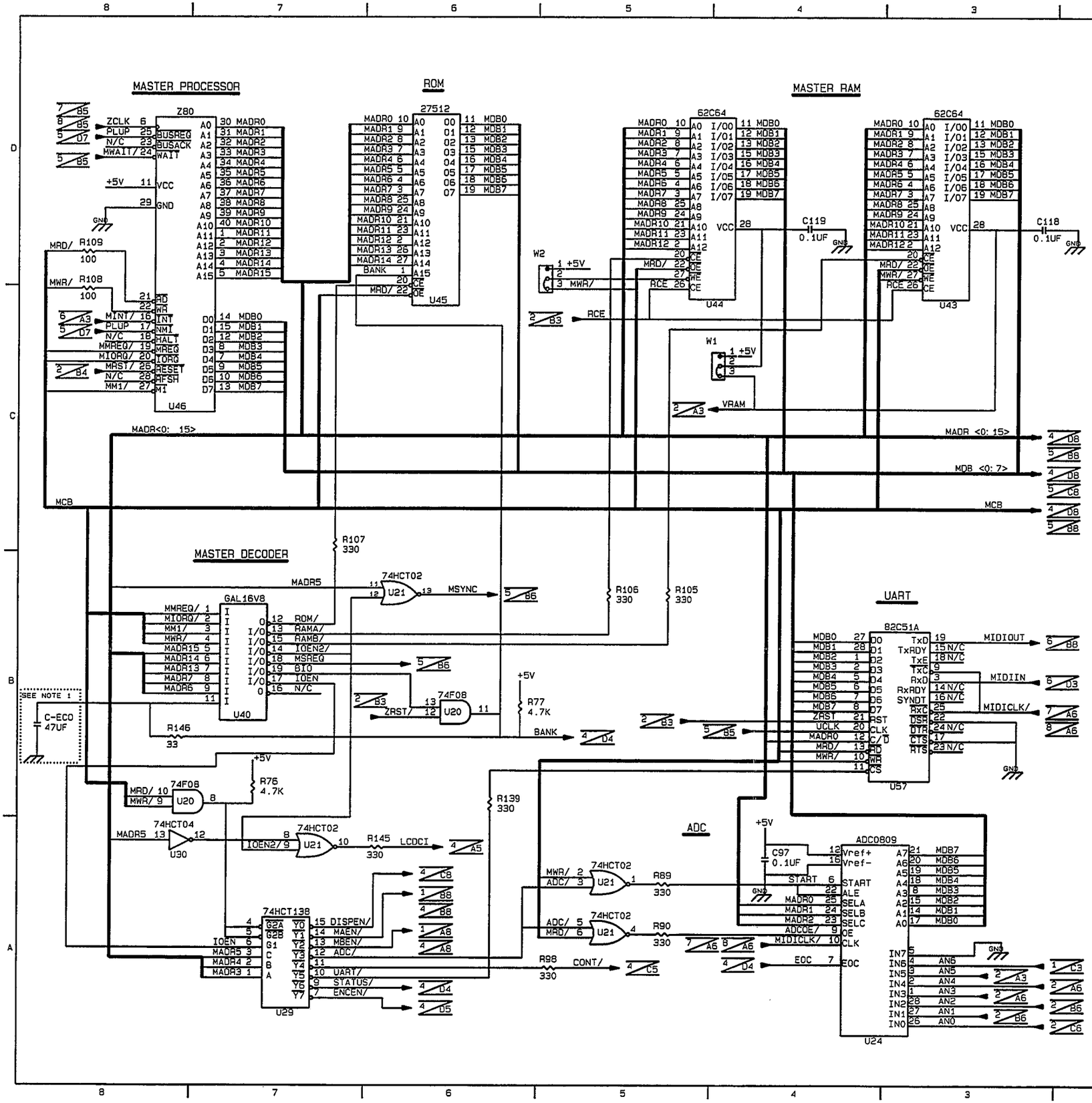
SHEET NUMBER	REVISION NUMBER
1 OF 9	8
2 OF 9	4
3 OF 9	5
4 OF 9	2
5 OF 9	2
6 OF 9	4
7 OF 9	3
8 OF 9	3
9 OF 9	4

CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEMATIC, LXP-15 ANALOG I
DRAWN AF	12/11/89	
CHECKED MWH	12/11/89	SIZE: B; CODE: ; NUMBER: 060-07876; REV.: 8
Q.C. LDR	12/11/89	
ISSUED DHS	12/11/89	SHEET 1 OF 9



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	AF 12/11/89	LDR 12/11/89
		MWH 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	AF 1/11/90	LDR 1/11/90
		MWH 1/11/90	DHS 1/11/90
2	CHANGED C137, R128, & CR26 PER ECO #900350-00	JV 6/20/90	RW 6/28/90
		AF 6/20/90	DHS 7/2/90
3	CHANGED VALUE OF R1 TO 30.1K 1% OR 2%. PER ECO 910220-01	JV 3/3/91	RW 3/19/91
		DHS 3/7/91	DHS 3/7/91
4	CHANGE R70, 74, 79, 82, 100 VALUES - ECO 941104-00. RENUMBER SHEET PER ECO 940915-02.	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEMATIC, LXP-15 ANALOG II
DRAWN AF	12/11/89		
CHECKED MWH	12/11/89	SIZE B	CODE
Q.C. LDR	12/11/89	NUMBER 060-07875	REV. 4
ISSUED DHS	12/11/89	SHEET 2 OF 9	

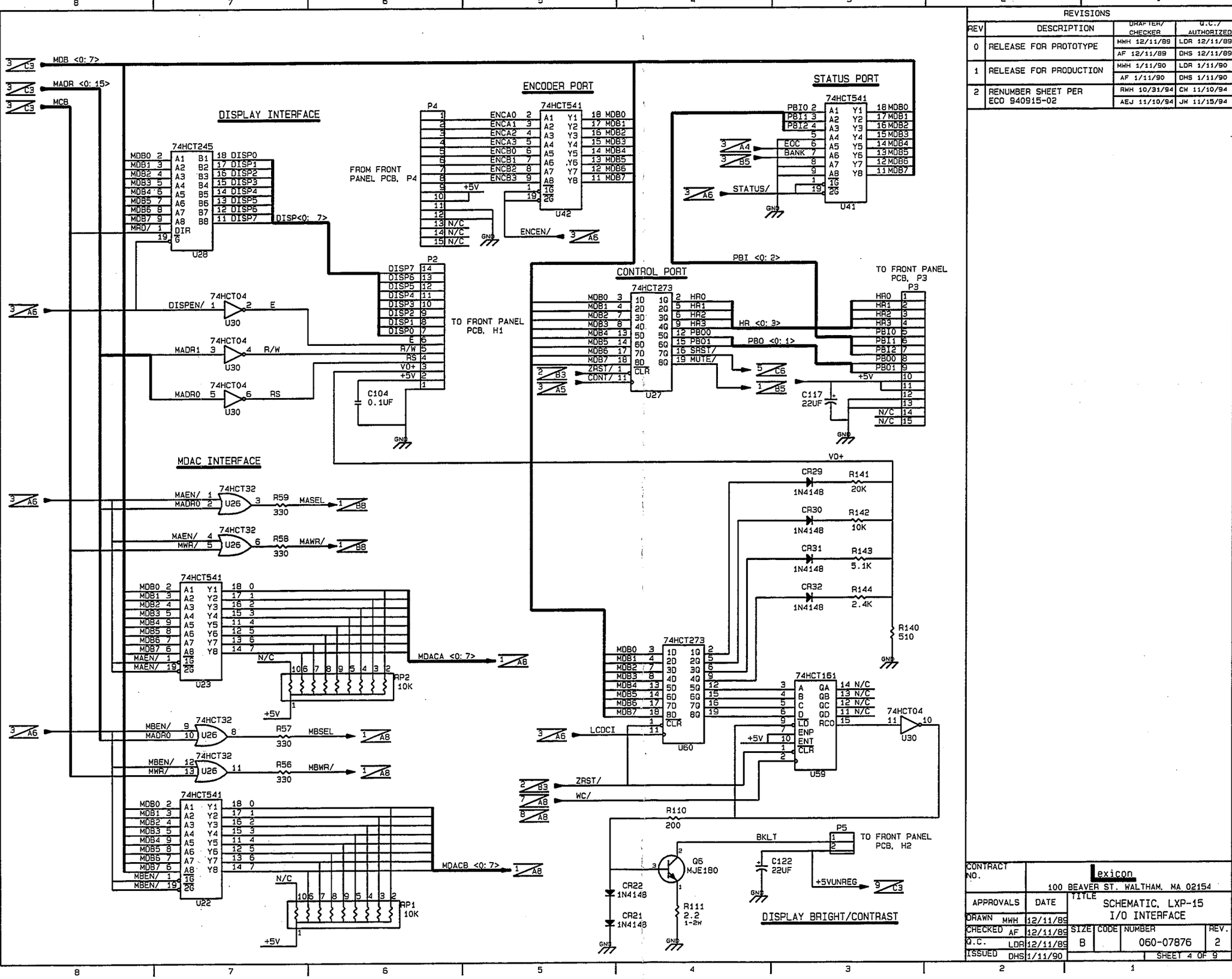


REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	D.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 12/11/89	LDR 12/11/89
		AF 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	MWH 1/11/90	LDR 1/11/90
		AF 1/11/90	DHS 1/11/90
2	ADD R146 AS PER ECO# 900226-00	MWH 3/12/90	RWH 3/12/90
		AF 3/12/90	DHS 3/14/90
3	CHANGE PILOT UNIT #'S TO 900-909. PER ECO NO. 900927-01.	JV 10/12/90	RW 10/25/90
		SF 10/22/90	DHS 10/29/90
4	CHANGE R146 TO 330 OHMS PER ECO NO. 900226-00-A.	JV 11/13/90	RW 11/13/90
		MWH 11/13/90	DHS 11/13/90
5	RENUMBER SHEET PER ECO 940915-02	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

NOTES

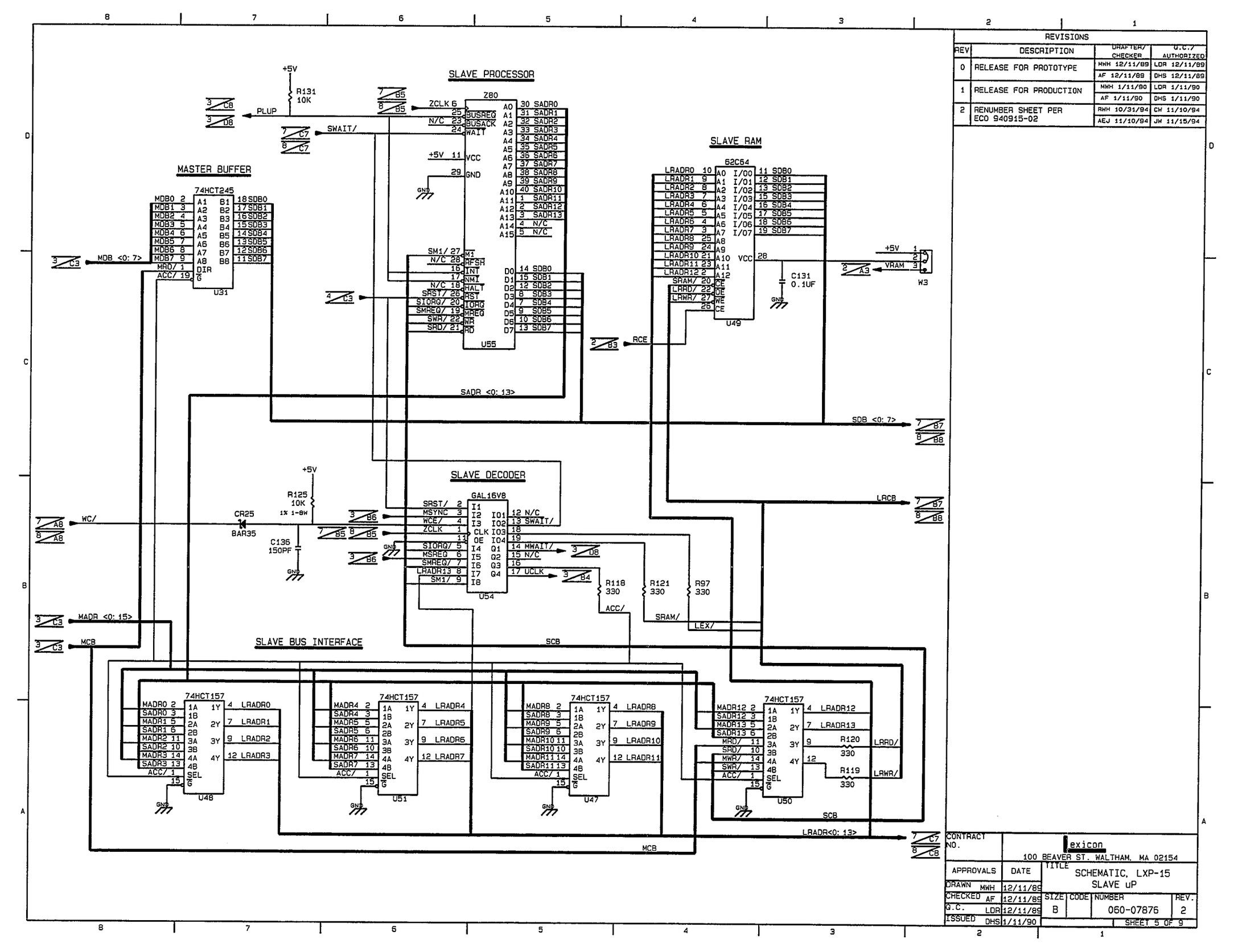
1. C-ECO IS INSTALLED IN PILOT UNITS 900-909. R146 IS NOT INSTALLED IN THESE UNITS.

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE: SCHEMATIC, LXP-15 MASTER uP	
DRAWN MWH	12/11/89		
CHECKED AF	12/11/89	SIZE: B	CODE:
D.C. LDR	12/11/89	NUMBER: 060-07876	REV: 5
ISSUED DHS	12/11/89	SHEET 3 OF 9	



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 12/11/89	LDR 12/11/89
		AF 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	MWH 1/11/90	LDR 1/11/90
		AF 1/11/90	DHS 1/11/90
2	RENUMBER SHEET PER ECO 940915-02	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

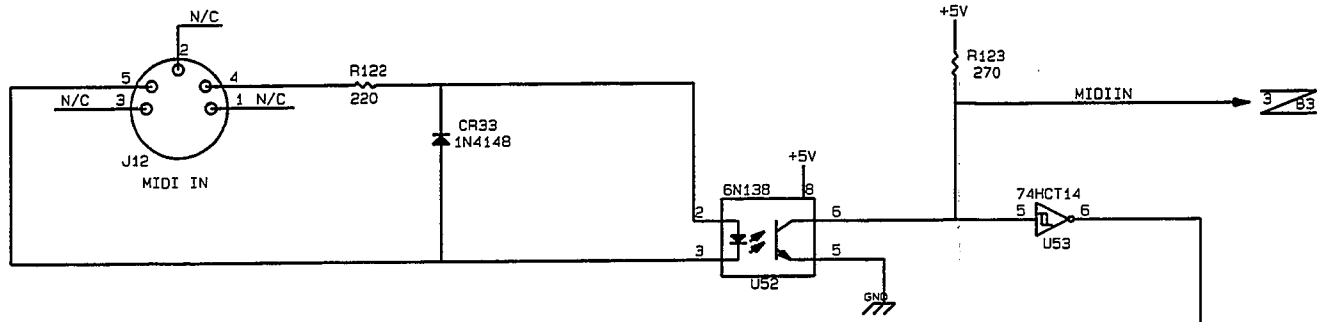
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEMATIC, LXP-15 I/O INTERFACE
DRAWN MWH	12/11/89		
CHECKED AF	12/11/89	SIZE B	CODE
Q.C. LDR	12/11/89	NUMBER 060-07876	REV. 2
ISSUED DHS	1/11/90	SHEET 4 OF 9	



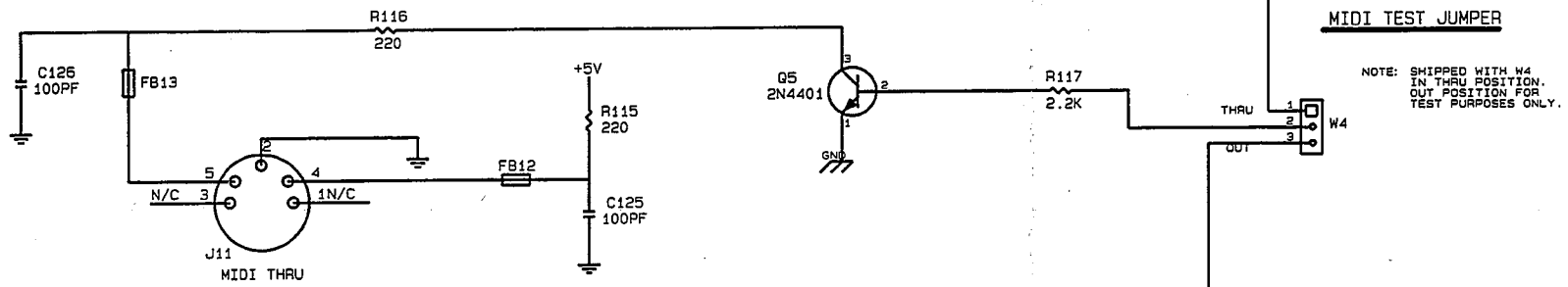
REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	C.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 12/11/89	LDR 12/11/89
		AF 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	MWH 1/11/90	LDR 1/11/90
		AF 1/11/90	DHS 1/11/90
2	RENUMBER SHEET PER ECO 940915-02	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

CONTRACT NO.		Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEMATIC, LXP-15 SLAVE uP	
DRAWN MWH	12/11/89		
CHECKED AF	12/11/89	SIZE: B	CODE:
Q.C. LDR	12/11/89	NUMBER: 060-07876	REV: 2
ISSUED DHS	1/11/90	SHEET 5 OF 9	

MIDI INPUT



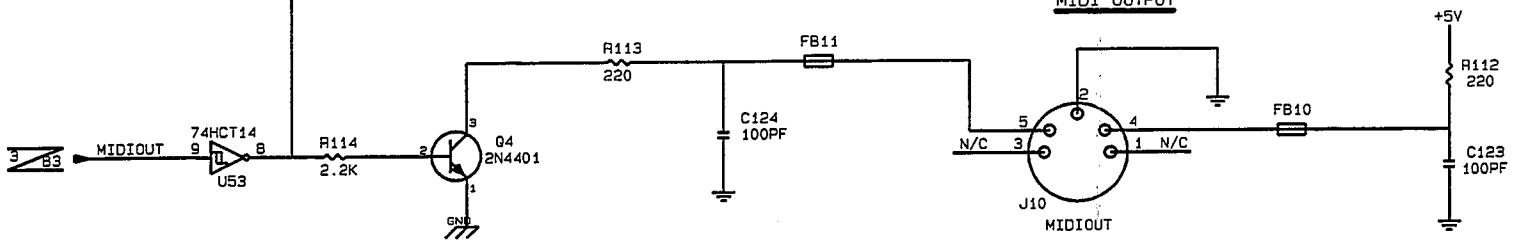
MIDI THRU



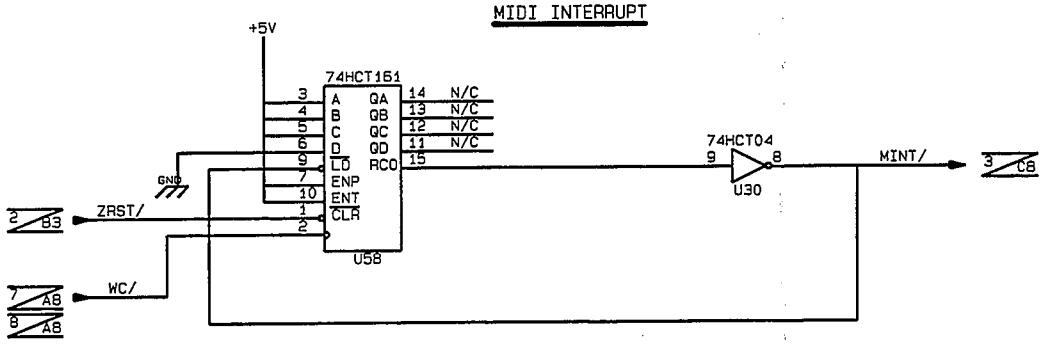
MIDI TEST JUMPER

NOTE: SHIPPED WITH W4 IN THRU POSITION. OUT POSITION FOR TEST PURPOSES ONLY.

MIDI OUTPUT



MIDI INTERRUPT



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 12/11/89	LDR 12/11/89
		AF 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	MWH 1/11/90	LDR 1/11/90
		AF 1/11/90	DHS 1/11/90
2	AS PER ECO# 900226-00 RE-ROUTE MIDI THRU AT RE-ROUTE CR33 PIN 2	MWH 3/12/90	RWH 3/12/90
		AF 3/12/90	DHS 3/14/90
3	CORRECTED NOTE PER ECO #900530-00	JV 6/20/90	RW 6/28/90
		AF 6/20/90	DHS 7/2/90
4	RENUMBER SHEET PER ECO 940915-02	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

CONTRACT NO.

Lexicon
100 BEAVER ST. WALTHAM, MA 02154

APPROVALS	DATE
DRAWN MWH	12/11/89
CHECKED AF	12/11/89
Q.C. LDR	12/11/89
ISSUED DHS	12/11/89

TITLE: SCHEMATIC, LXP-15 MIDI

SIZE	CODE	NUMBER	REV.
B		060-07876	4

SHEET 6 OF 9

AUDIO MEMORY

NOTE: U33, 35, 37, 39 ARE LEFT UNPOPULATED.
(RESERVED FOR 256K BY 16 DRAM OPTION)

44256 U33, U35, U37, U39

4464 U32, U34, U36, U38

DAB<0: 15>

MA<0: 7>

GND

AUDIO PROCESSOR

+5V

74HC74 U64

LRADR<0: 13>

R148 330

N/C

ZCLK

SWAIT/

R103 330 RAS/

SDB<0: 7>

MCLK

LRCB

C99 10PF

Y1 16MHZ

R147 1M

ZRST/

R95 10K

C139 10PF

WC/

MIDICLK/

R92 10K

R91 10K

R94 10K

R93 10K

R96 10K

DATA

LEXICHIP-2A U25

CONVERSION LATCH

74HCT574 U18

74HCT574 U19

DAC <0: 15>

74F08 U20

R104 330 CAS1/

R102 330 WE1/

REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	D.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 12/11/89	
		AF 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	MWH 1/11/90	LDR 1/11/90
		AF 1/11/90	DHS 1/11/90
2	AS PER ECO# 900226-00 DEPOPULATE C139	MWH 3/12/90	RWH 3/12/90
		AF 3/12/90	DHS 3/14/90
3	REDESIGN FOR LEXICHIP-2, ADD NOTE 1, RENUMBER SHEET PER ECO 940915-02	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

NOTES

1. THIS SHEET REPRESENTS PCB #710-10770 (WITH LEXICHIP-2A). REFER TO SHEET 8 FOR PCB #710-07870 (WITH LEXICHIP-1).

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEMATIC, LXP-15 LEXICHIP-2A
DRAWN MWH	12/11/89		
CHECKED AF	12/11/89	SIZE B	CODE
ISSUED LDR	12/11/89	NUMBER 060-07876	REV. 3
Q.C. DHS	12/11/89	SHEET 7 OF 9	

AUDIO MEMORY

NOTE: U33, 35, 37, 39 ARE LEFT UNPOPULATED.
(RESERVED FOR 256K BY 16 DRAM OPTION)

44256 U33 · 44256 U35 · 44256 U37 · 44256 U39
4464 U32 · 4464 U34 · 4464 U36 · 4464 U38

DAB<0: 15>
MA<0: 7>

GND

AUDIO PROCESSOR

LRADR<0: 13>
SWAIT/
SDB<0: 7>
LRCB
C99 33PF · Y1 16MHZ
+5V
ZRST/
R95 10K
WC/
C6
LRAD/
LRWR/
LEX/
LEXICHIP1 U25

ZCLK
NOTE: DEPOPULATE C139
C139 33PF

R103 330 RAS/
R104 330 CAS1/
R102 330 WE1/

74F08 U20

MIDICLK/
R92 10K
R91 10K
R94 10K
R93 10K
R96 10K

CONVERSION LATCH

74HCT574 U18 · 74HCT574 U19

DAC <0: 15>

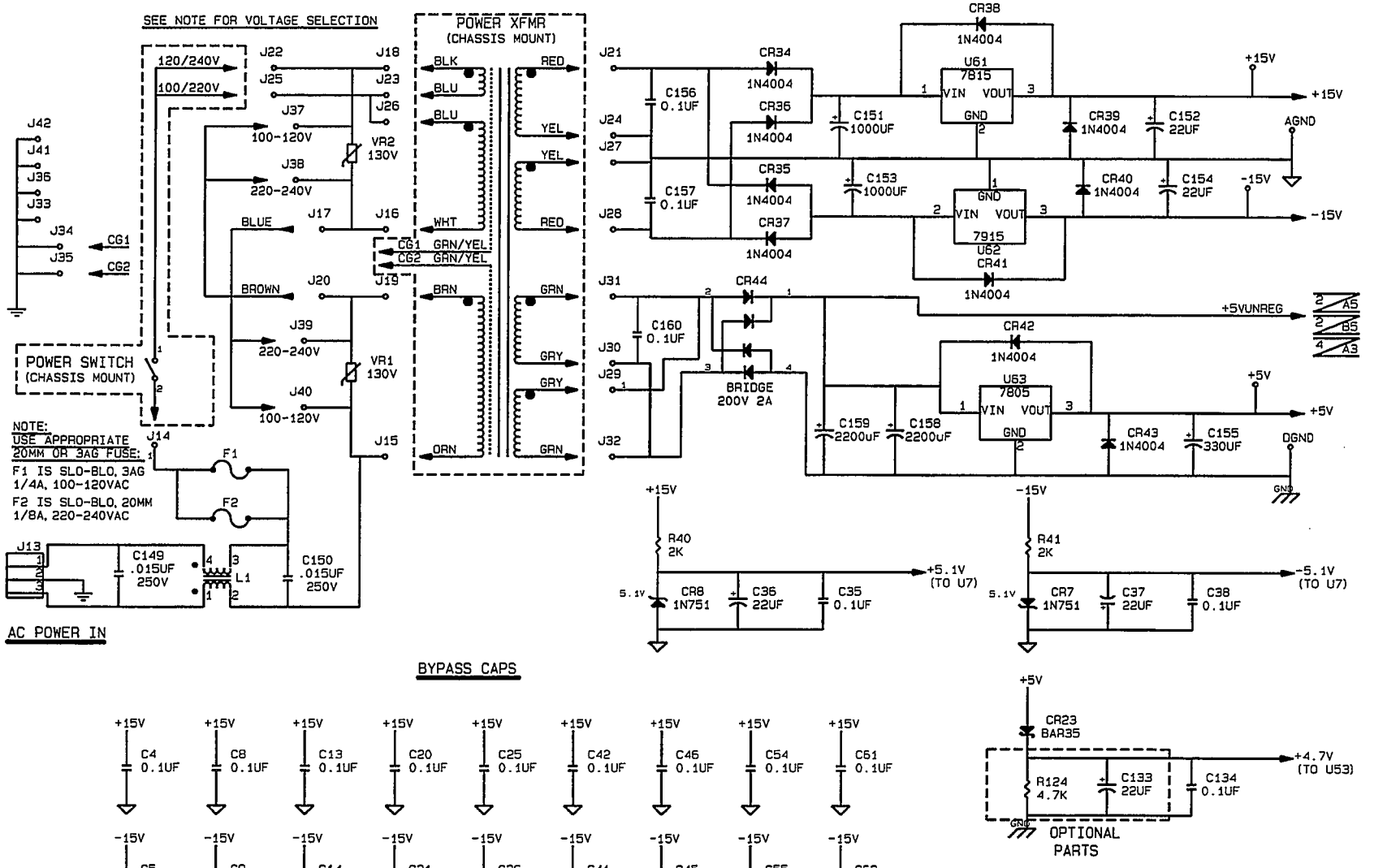
REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 12/11/89	
		AF 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	MWH 1/11/90	LDR 1/11/90
		AF 1/11/90	DHS 1/11/90
2	AS PER ECO# 900226-00 DEPOPULATE C139	MWH 3/12/90	RWH 3/12/90
		AF 3/12/90	DHS 3/14/90
3	ADD NOTE 1 AND RENUMBER SHEET PER ECO 940915-02	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

NOTES

1. THIS SHEET REPRESENTS PCB #710-07870 (WITH LEXICHIP-1). REFER TO SHEET 7 FOR PCB #710-10770 (WITH LEXICHIP-2A).

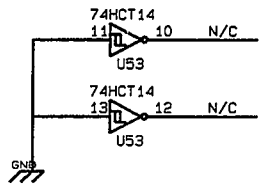
CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE: SCHEMATIC, LXP-15 LEXICHIP-1	
DRAWN MWH	12/11/89		
CHECKED AF	12/11/89	SIZE: B	CODE:
ISSUED LDR	12/11/89	NUMBER: 060-07876	REV.: 3
Q.C. DHS	12/11/89	SHEET 8 OF 9	

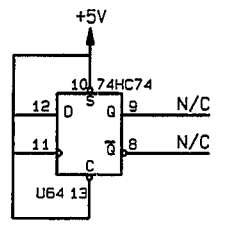


REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	D.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	AF 12/11/89	LDR 12/11/89
		MWH 12/11/89	DHS 12/11/89
1	RELEASE FOR PRODUCTION	AF 1/11/90	LDR 1/11/90
		MWH 1/11/90	DHS 1/11/90
2	R124, C133, ARE OPTIONAL PER ECO #900530-00	JV 5/20/90	RW 6/28/90
		AF 6/20/90	DHS 7/2/90
3	DELETED CR45, C161, CHANGED CR44 TO A BRIDGE, PER ECO 910329-00	RW 5/10/91	RWH 5/10/91
		SF 5/10/91	DHS 5/20/91
4	ADD C161 & SPARE U64, RENUMBER SHEET PER PER ECO 940915-02	RWH 10/31/94	CW 11/10/94
		AEJ 11/10/94	JW 11/15/94

SPARES





VOLTAGE SELECTION

CONNECT THE APPROPRIATE WIRES ACCORDING TO THE TABLE BELOW PER THE AC VOLTAGE REQUIREMENT:

VAC	(J17) BLUE	(J20) BROWN	FROM PWR SW
100V	J40	J37	J25
120V	J40	J37	J22
220V	J39	J38	J25
240V	J39	J38	J22

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE: SCHEMATIC, LXP-15 POWER SUPPLY	
DRAWN AF	12/11/89		
CHECKED MWH	12/11/89	SIZE: B	CODE:
Q.C. LDR	12/11/89	NUMBER: 060-07876	REV: 4
ISSUED DHS	1/11/90	SHEET 9 OF 9	

CONN,CIRC DIN,5FC@180 DEG,PCRA
P/N 510-04286 (3 PLACES)

NUT,4-40,KEP,ZN
P/N 643-01732 (6 PLACES)

SCRW,4-40 X 3/8,PNH,PH,BLK
P/N 640-02812 (6 PLACES).

LUG,PCB/#4CL
P/N 620-08252

DETAIL C-C
(MOUNTING #4 LUG SOLDER AT J41 & FASTEN WITH J11 MOUNTING SCREW)

DETAIL A-A
(MOUNTING POWER CONN.)

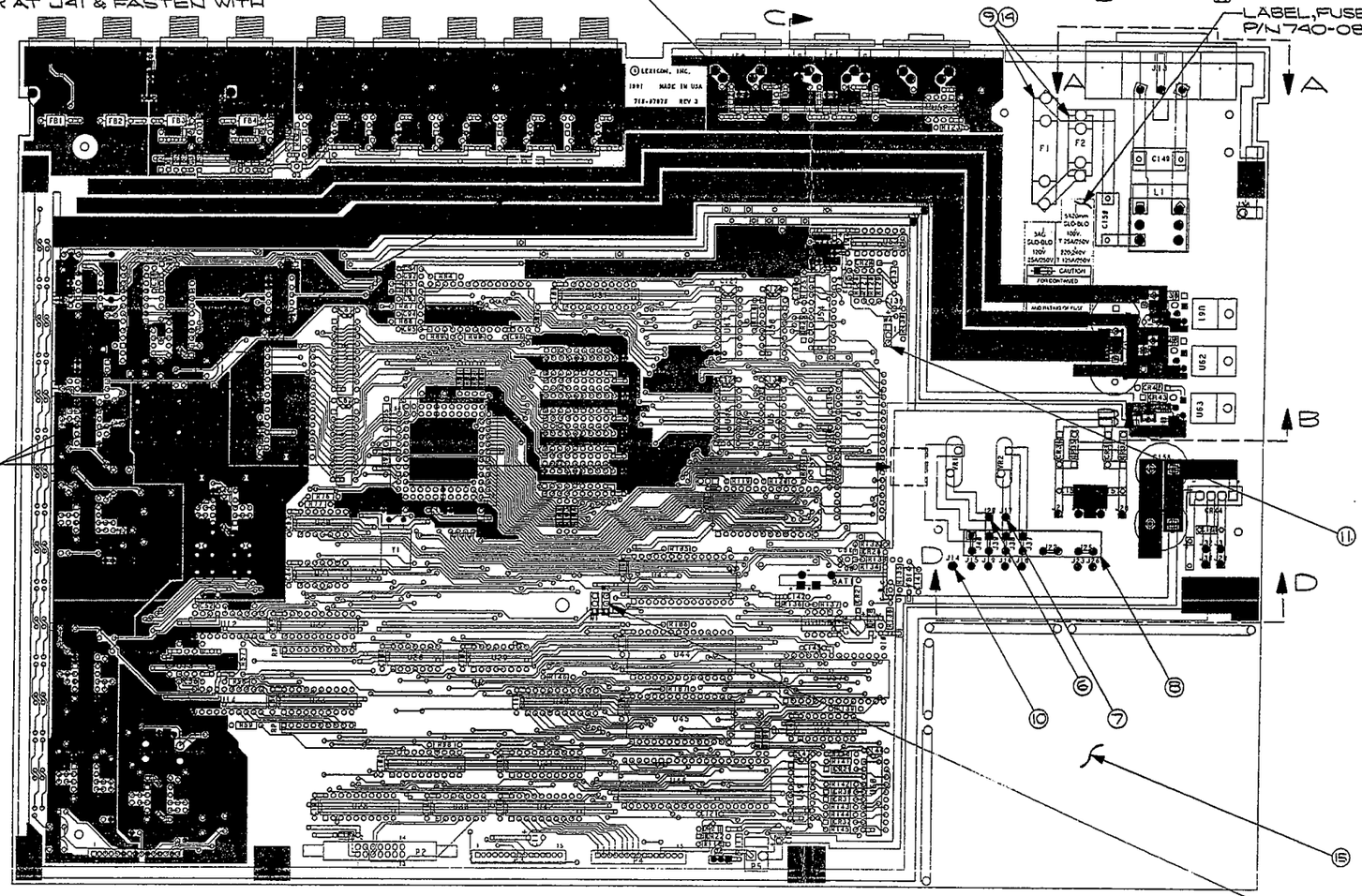
SCRW,4-40X3/8,PNH,PH,ZN
P/N 640-01706 (2 PLACES)

CONN,AC,3MC,PCRA,IEC,6A
P/N 510-017888

NUT,4-40,KEP,ZN
P/N643-01732
(2 PLACES)

LABEL,FUSE,FRENCH,LXP-15
P/N 740-08587 (120V ONLY)

LABEL,FUSE,CAUTION,LXP-15
P/N 740-08359



BUMPER,FEET,3-M #SJ5018
P/N 541-00781 (3 PLACES)
(INSTALL ON BOTTOM SIDE IN THESE LOCATIONS).

SCRW,4-40X3/8,PNH,PH,ZN
P/N 640-01706 (3 PLACES)

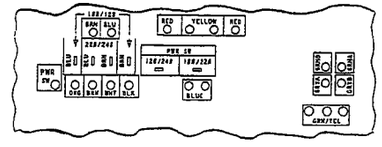
INSUL,SEMI,BUSHING,TO-220
P/N 630-00952 (3 PLACES)

INSUL,SEMI,SIL RUB,TO-220,SHORT
P/N 630-07339 (3 PLACES)

HEATSINK,LXP-15
P/N 704-07829

NUT,4-40,KEP,ZN
P/N 643-01732 (3 PLACES)

DETAIL B-B
(TYPICAL MOUNTING OF U61-63)



DETAIL D-D
(WIRE MOUNTING GUIDE, SEE PAGE 2)

REV	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.
Ø	RELEASE FOR PILOT	JV 11/13/89 AF 11/13/89	
1	RELEASE FOR PRODUCTION	JV 1/12/90 AF 1/29/90	CW 2/2/90 DHS 2/13/90
2	CHANGED PER ECO 900226-00	MAF 4/19/90 MWH 4/25/90	CW 5/16/90 DHS 5/11/90
3	ADDED NOTE 9. ON SHT 2. AND UPDATED DOC. CTL BLOCK, PER ECO 900508-02	JV 5/16/90 AF 5/16/90	CW 5/16/90 DHS 5/16/90
4	UPDATED FUSE LABEL AND NOTE 10. ADDED NOTE 13 AND SKETCH. PER ECO 900612-01	JV 7/3/90 AF 7/3/90	DHS 7/11/90 DHS 7/11/90
5	ADDED FRENCH FUSE LABEL. AND NOTE 14., PER ECO 900906-00	MAF 9/25/90 AF 9/28/90	CW 10/2/90 DHS 10/2/90
6	ADDED BUMPER FEET. PER ECO 910328-00 REVISED BD OUTLINE AND POWER SUPPLY. PER ECO 910329-00 & ADDED SHEET 3	JV 4/18/91 6/4/91	6/11/91
7	ADDED NOTE 16 PER ECO# 911106-00	JV 11-25-91 12-2-91	12-2-91
8	UPDATE DOC. CTL BLK PER ECO#911216-00	JV 12/20/91	12/31/91
9	CHANGE NOTE 14 PER ECO# 920225-00. ADDED A THIRD BUMPER FOOT PER ECO# 910328-00-A.	JV 3/5/92 3/6/92	3/9/92 3/11/92
10	CHANGE NOTE 4 PER DCR #920608-00	JV 6/15/92 6/18/92	6/19/92
11	DELETED NOTE 5; CHANGED NOTE 12 & SHEETS 2 & 3; UPDATED DOC. CTL BLK PER ECO #940524-00	JV 6/29/94 6/30/94	7/6/94 7/12/94

NOTES

1. ALL COMPONENTS TO BE INSTALLED FROM COMPONENT SIDE OF PCB EXCEPT SWAGED STANDOFFS UNLESS OTHERWISE INDICATED.
2. MASKING FOR POST-SOLDER ASSEMBLY IS INDICATED BY SOLID AREAS
3. COMPONENT HEIGHT 1.18" MAXIMUM.
4. LEAD PROTRUSIONS FROM CIRCUIT SIDE OF PCB: MIN-END IS VISIBLE IN THE SOLDER. MAX-0.100 (2.5mm).
6. INSERT STRIPPED LEAD OF 22AWG BROWN WIRE, P/N 675-08257, AT J20, AND SOLDER.
7. INSERT STRIPPED LEAD OF 22AWG BLUE WIRE, P/N 675-08256, AT J17, AND SOLDER.
8. INSERT ODC'S, P/N 510-08255 AT J22, 25, 37-40. SECURE ODC'S MECHANICALLY BY BENDING LEGS ON SOLDER SIDE OF PCB, AT A MINIMUM OF 60° BEFORE SOLDERING. ZIERICK TOOL ZPT81-A MAY BE USED FOR INSERTION. USE ANVIL P/N 90-0102-0300 AND HOLDER P/N 90-0112-1375 WITH ARBOR PRESS OR EQUIVALENT FOR BENDING LEGS.
9. FOR 120 VAC, INSTALL 0.25A/250V 3AG FUSE, P/N 440-00860, IN POSITION F1. FOR 100 VAC, INSTALL 0.25A/250V 20MM FUSE, P/N 440-02348, OR FOR 220/240 VAC, INSTALL 0.125/250V 20MM FUSE P/N 440-02347, IN POSITION F2.
10. INSERT STRIPPED LEAD OF 22AWG BROWN WIRE, P/N 675-08258, AT J14, AND SOLDER.
11. INSERT W4 POST-SOLDER JUMPER AT PINS 1 AND 2.
12. REFER TO BOM#'S 023-08278,023-10262/100V;023-07856,023-10263/120V;023-08756,023-10264/220V;023-07867,023-10265/240V.
13. INSERT STRIPPED LEAD OF 18 AWG GRN/YEL WIRE P/N 675-08272 THROUGH HOLE IN J13, AND TWIST TOGETHER FOR A GOOD MECHANICAL CONNECTION. BEFORE SOLDERING.
14. APPLY A DROP OF CLEAR RTV SILICONE P/N 120-02023 TO PCB AND FUSE COVERS BEFORE INSTALLING.
15. BREAK AWAY P.C.B. BEFORE INSTALLING IN CHASSIS.
16. JUMPER W2 PINS 2 AND 3 ON REV 3 PCB.

DOCUMENT CONTROL BLOCK

SHEET	REV.
1	11
2	6
3	2

		710-07875	
		REV. 3+	
NEXT ASSY.	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX

MATERIAL

FINISH

DO NO SCALE DRAWING

CONTRACT NO.

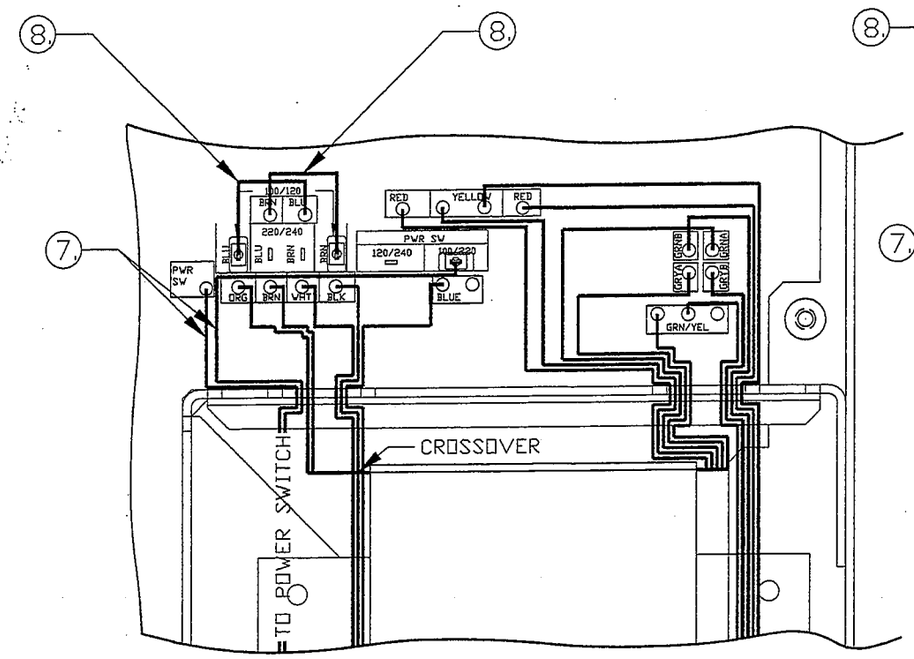
lexicon

APPROVALS	DATE
DRAWN JV	1/12/90
CHECKED AF	1/29/90
Q.C. CW	2/2/90
ISSUED DHS	2/13/90

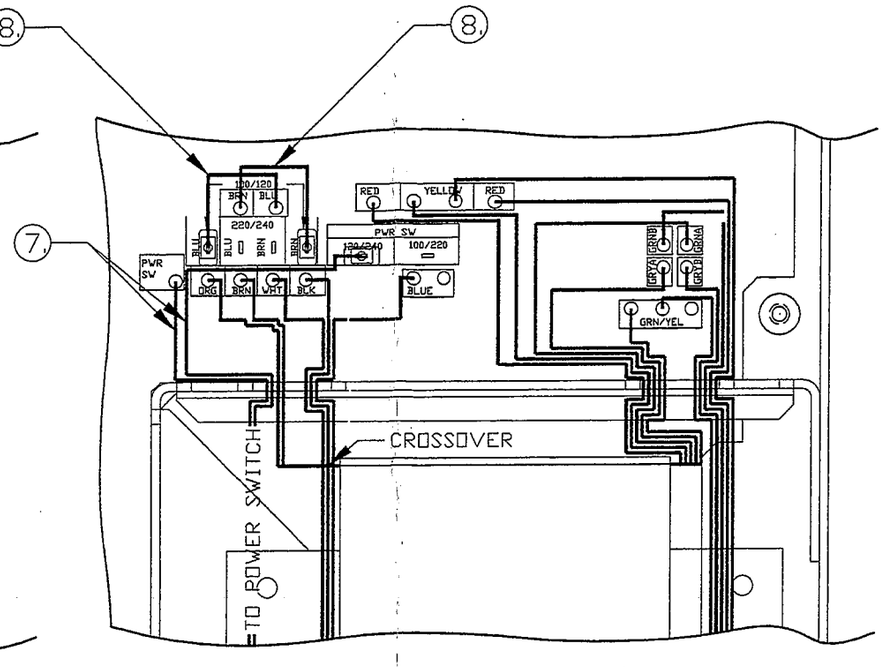
PC BD, MAIN BD., LXP-15
ASSEMBLY DRAWING

SIZE D | FSCM NO. | DWG. NO. 080-07875 | REV 11

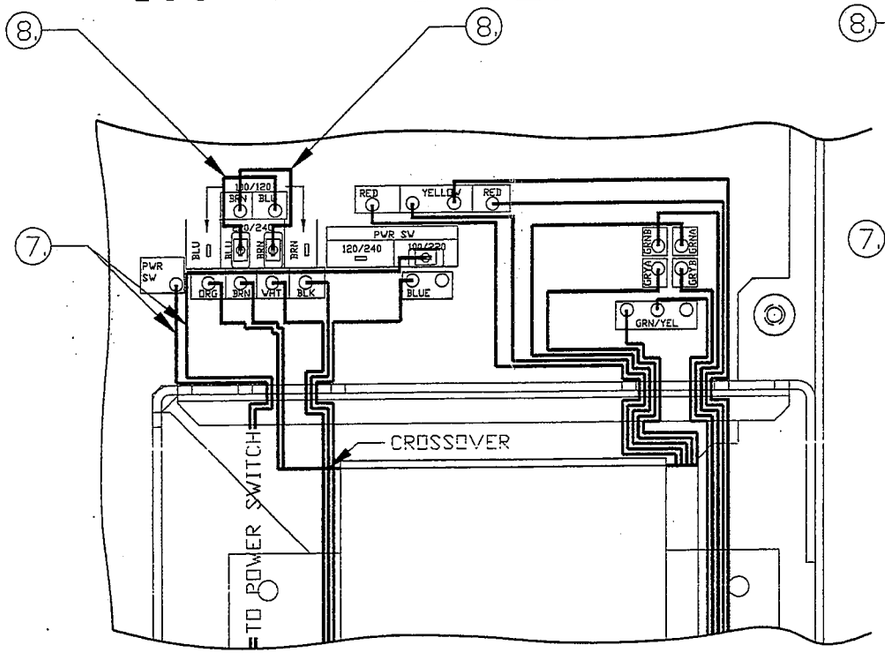
SCALE 1:1 | SHEET 1 OF 3



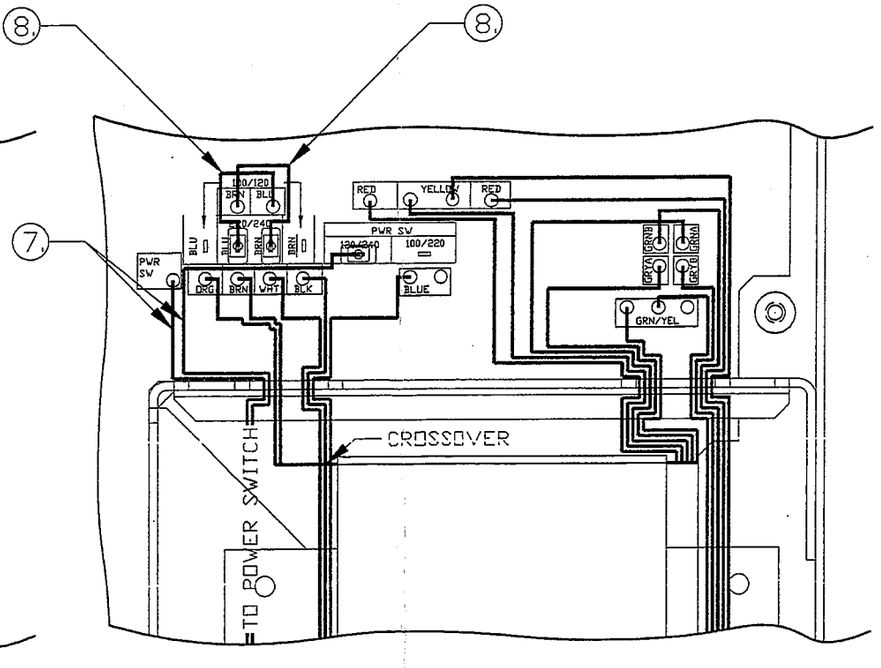
100 VOLTS SELECTION



120 VOLTS SELECTION



220 VOLTS SELECTION



240 VOLTS SELECTION

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	RELEASE FOR PRODUCTION	JV 2/13/90 AF 2/13/90	CV 2/13/90 DHS 2/13/90
2	ADDED NOTE 9 PER ECO#900503-02	JV 5/16/90 AF 5/16/90	CV 5/16/90 DHS 5/16/90
3	UPDATED NOTE 7 AND ADDED NOTE 10 PER ECO#900812-01	JV 7/3/90 AF 7/3/90	CV 7/12/90 DHS 7/12/90
4	UPDATED WIRING & SILKSCREEN PER ECO#910329-00	JV 5/10/91 DHS 6/5/91	CV 6/10/91 DHS 6/11/91
5	CHANGED NOTE 9 PER ECO#911216-00	JV 12/23/91 MK 12/30/91	CV 12/30/91 DHS 12/31/91
6	CHANGED NOTE 1 PER ECO#940524-00	JV 6/29/94 MK 6/30/94	CV 7/6/94 DHS 7/7/94

NOTES

1. REFER TO BOM#'S 023-07855, 024-07857 OR 024-10266.
2. FOR 100VAC, INSTALL FUSE, 5X20MM, SLO-BLO, .250 AMP P/N 440-02348.
3. FOR 120VAC, INSTALL FUSE, 3AG, SLO-BLO, .250 AMP P/N 440-00860.
4. FOR 220/240VAC, INSTALL FUSE, 5X20MM, SLO-BLO, .125 AMP P/N 440-02347.
5. TRANSFORMER SHOWN IS XFORMER, POWER, 15VA, UI75, INTL P/N 470-07889.
6. SOLDER TRANSFORMER WIRES AS SHOWN.
7. FOR POWER SWITCH CONNECTIONS USE WIRE, 22G, BRN, 12", .187QDC/ST P/N 675-08258 & WIRE, 22G, BRN, 12", .187QDCX2 P/N 675-08259.
8. FOR JUMPER VOLTAGE SELECTION USE WIRE, 22G, BLU, 2.5", .187QDC/ST P/N 675-08256 & WIRE, 22G, BRN, 2.5", .187QDC/ST P/N 675-08257 AT POINTS INDICATED.
9. PLACE QDC CONN P/N 490-09182 OVER BARE CONNECTORS.
10. TY-WRAP THE FOLLOWING WIRES TOGETHER APPROXIMATELY 1/2" ABOVE ABOVE THE P.C. BOARD:
    A. THE ORANGE, BROWN, WHITE, BLACK AND BLUE WIRES FROM THE TRANSFORMER WITH THE BROWN WIRE FROM THE POWER SWITCH.
    B. THE (2) RED AND (2) YELLOW WIRES FROM THE TRANSFORMER.
    C. THE (2) GRAY WIRES FROM THE TRANSFORMER.
    D. THE (2) GREEN WIRES FROM THE TRANSFORMER.
    E. THE (2) GRN/YEL WIRES FROM THE TRANSFORMER.

	710-07870
	REV. 3+
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 12 FILE NAME 07875-62

APPROVALS		DATE
DRAWN	JV	2/13/90
CHECKED	AF	2/13/90
Q.C.	CV	2/13/90
ISSUED	DHS	2/13/90

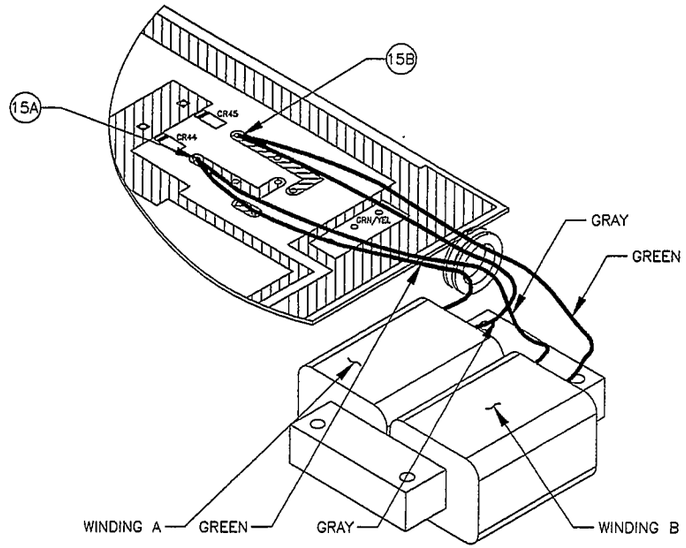
lexicon

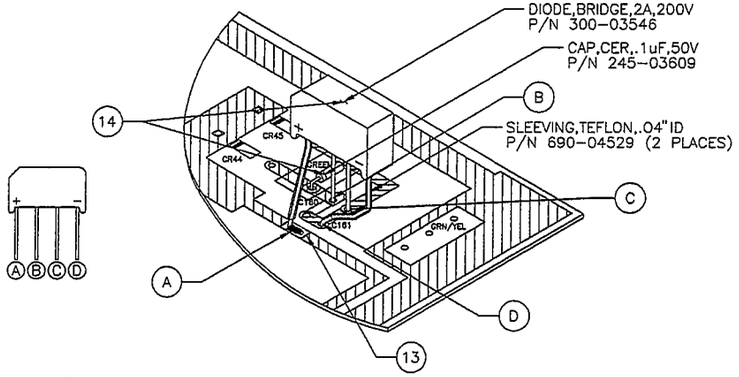
TITLE PC BD,MAIN BD,LXP-15, ASSEMBLY,DRAWING

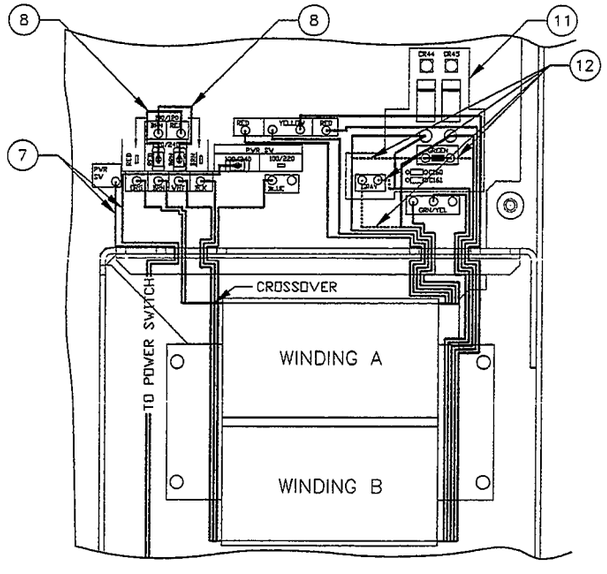
SIZE	FSCM NO.	DWG. NO.	REV.
D		080-07875	6

SCALE N/A SHEET 2 OF 3

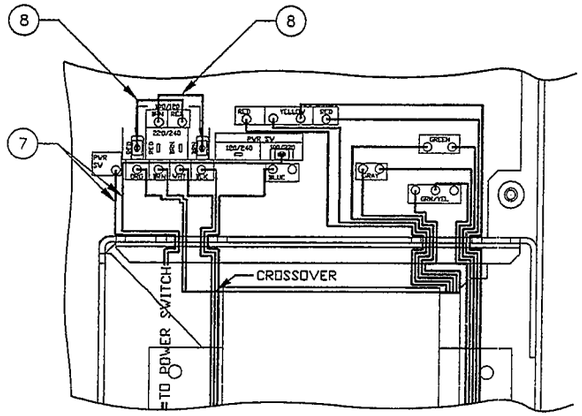
LEXICON, INC.



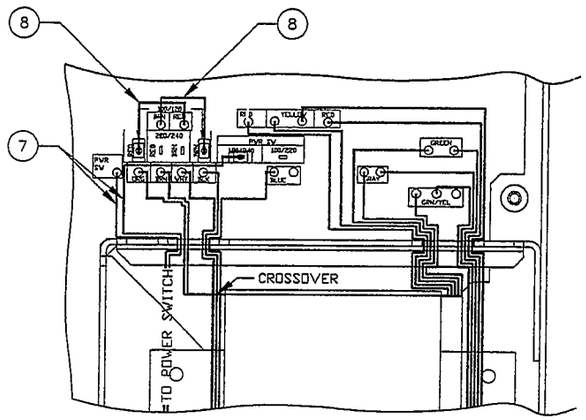




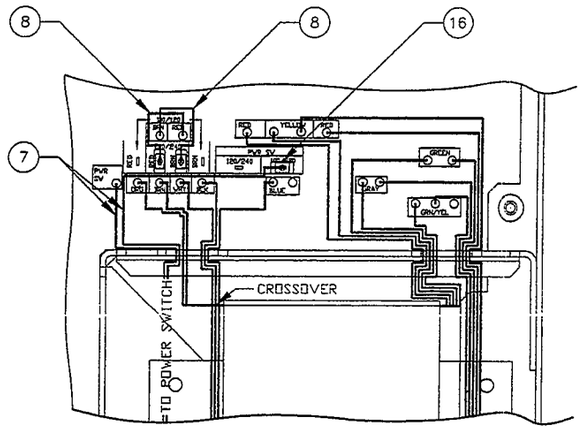
220/240 VOLTS RETRO FIT



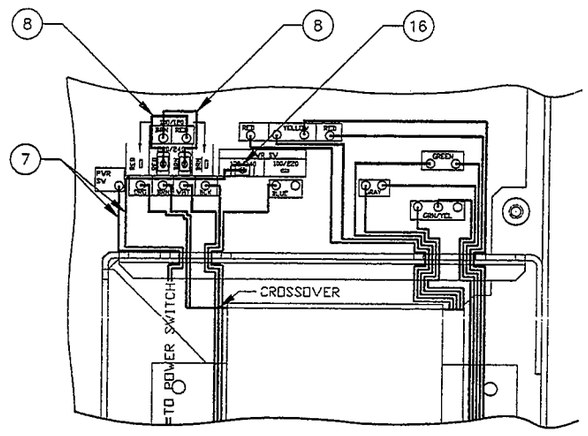
100 VOLTS SELECTION



120 VOLTS SELECTION



220 VOLTS SELECTION



240 VOLTS SELECTION

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	JV 5/10/91 DHS 6/5/91	CV 6/10/91 DHS 6/11/91
1	UPDATED NOTE 9 PER ECO #911216-00	JV 12/23/91 HK 12/27/91	CV 12/30/91 DHS 12/31/91
2	CHANGED NOTE 1 PER ECO #940524-00	JV 6/29/94 HK 6/30/94	CW 7/6/94 DHS 7/7/94

NOTES

1. REFER TO BOM#'S:023-07855, 024-07857
2. FOR 100VAC, INSTALL FUSE, 5X20MM, SLO-BLO, .250 AMP P/N 440-02348.
3. FOR 120VAC, INSTALL FUSE, 3AG, SLO-BLO, .250 AMP P/N 440-00860.
4. FOR 220/240VAC, INSTALL FUSE, 5X20MM, SLO-BLO, .125 AMP P/N 440-02347.
5. TRANSFORMER SHOWN IS XFORMER, POWER, 15VA, UI75, INTL P/N 470-07889.
6. SOLDER TRANSFORMER WIRES AS SHOWN.
7. FOR POWER SWITCH CONNECTIONS USE WIRE, 22G, BRN, 12", .187QDC/ST P/N 675-08258 & WIRE, 22G, BRN, 12", .187QDCX2 P/N 675-08259.
8. FOR JUMPER VOLTAGE SELECTION USE WIRE, 22G, BLU, 2.5", .187QDC/ST P/N 675-08256 & WIRE, 22G, BRN, 2.5", .187QDC/ST P/N 675-08257 AT POINTS INDICATED.
9. PLACE QDC CONN P/N 490-09182 OVER BARE CONNECTORS.
10. TY-WRAP THE FOLLOWING WIRES TOGETHER APPROXIMATELY 1/2" ABOVE ABOVE THE P.C. BOARD:
    A. THE ORANGE, BROWN, WHITE, BLACK AND BLUE WIRES FROM THE TRANSFORMER WITH THE BROWN WIRE FROM THE POWER SWITCH.
    B. THE (2) RED AND (2) YELLOW WIRES FROM THE TRANSFORMER.
    C. THE (2) GRAY WIRES FROM THE TRANSFORMER.
    D. THE (2) GREEN WIRES FROM THE TRANSFORMER.
    E. THE (2) GRN/YEL WIRES FROM THE TRANSFORMER.

PCB REV-2 TO REV-3 RETRO FIT NOTES

1. REMOVE COMPONENTS FROM P.C.B. MAIN BD, LXP-15, REV. 2, 220/240V OPTION ONLY; CR44, 45; C160, 161.
2. DESOLDER (2) GREEN WIRES & (2) GRAY TRANSFORMER SECONDARY LEADS FROM P.C.B AS SHOWN.
3. REMOVE SOLDERMASK FROM ETCH, AS SHOWN.
4. INSTALL CAP, CER, .1uF, 50V P/N 245-03609 & DIODE, BRIDGE, 2A, 200V P/N 300-03546, AS SHOWN.
5. CONNECT GREEN WIRE FROM WINDING A, WITH GRAY WIRE FROM WINDING B TO POSITION 15A, AS SHOWN.
   CONNECT GREEN WIRE FROM WINDING B, WITH GRAY WIRE FROM WINDING A TO POSITION 15B, AS SHOWN.
6. CONNECT POWER SWITCH WIRE FOR 240 VOLT SELECTION, OR 220 VOLT SELECTION AS SHOWN.

	710-07870
	REV-2
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD REL 12 FILE NAME 07875-23

APPROVALS		DATE
DRAWN	JV	5/10/91
CHECKED	DHS	6/5/91
Q.C.	CW	6/10/91
ISSUED	DHS	6/11/91

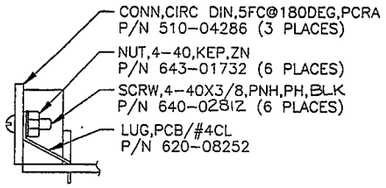
lexicon

TITLE PC BD,MAIN BD,LXP-15, ASSEMBLY,DRAWING

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-07875	2

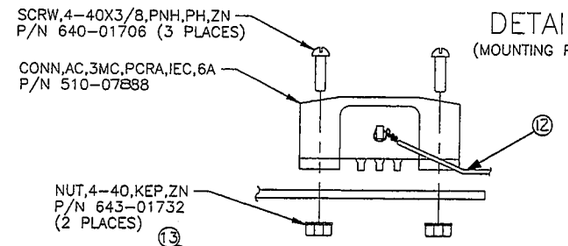
SCALE N/A SHEET 3OF 3

LEXICON, INC.



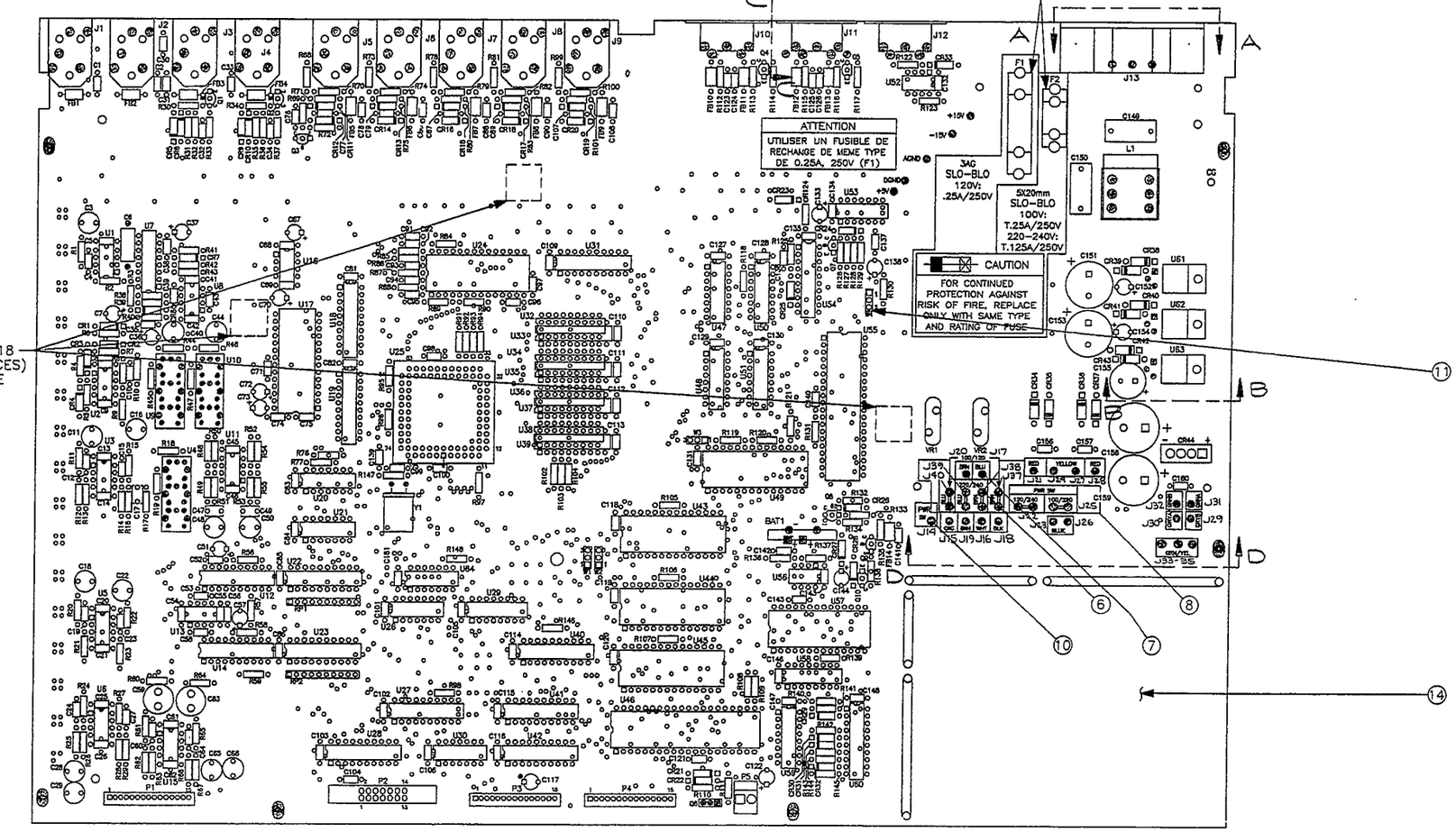
DETAIL C-C

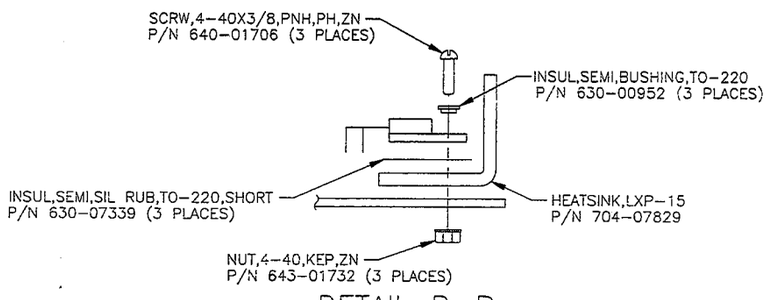
(MOUNTING #4 LUG SOLDER AT J41 & FASTEN WITH J11 MOUNTING SCREW.)



DETAIL A-A

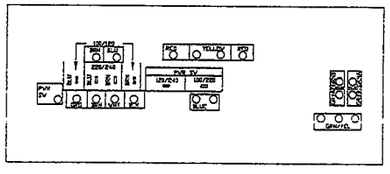
(MOUNTING POWER CONN)





DETAIL B-B

(TYPICAL MOUNTING OF U61-63)



DETAIL D-D

(WIRE MOUNTING GUIDE, SEE PAGE 2)

REV	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.

NOTES

1. REFER TO BOM #s 023-10262 FOR 100V; 023-10263 FOR 120V; 023-10264 FOR 220V; AND 023-10265 FOR 240V.
2. ALL COMPONENTS TO BE INSTALLED FROM COMPONENT SIDE OF PCB EXCEPT SWAGED STANDOFFS UNLESS OTHERWISE INDICATED.
3. MASKING FOR POST-SOLDER ASSEMBLY IS INDICATED BY SOLID AREAS
4. COMPONENT HEIGHT 1.10" MAXIMUM.
5. LEAD PROTRUSIONS FROM CIRCUIT SIDE OF PCB: MIN: END IS VISIBLE IN SOLDER. MAX: 0.100" (2.5mm)

(6) INSERT STRIPPED LEAD OF 22AWG BROWN WIRE,P/N 675-08257, AT J20,AND SOLDER.

(7) INSERT STRIPPED LEAD OF 22AWG BLUE WIRE,P/N 675-08256, AT J17,AND SOLDER.

(8) INSERT QDCs,P/N 510-08255 AT J22,25,37-40. SECURE QDCs MECHANICALLY BY BENDING LEGS ON SOLDER SIDE OF PCB, AT A MINIMUM OF 60° BEFORE SOLDERING. ZIERICK TOOL ZPT81-A MAY BE USED FOR INSERTION. USE ANVIL P/N 90-0102-0300 AND HOLDER P/N 90-0112-1375 WITH ARBOR PRESS OR EQUIVALENT FOR BENDING LEGS.

(9) FOR 120 VAC, INSTALL 0.25A/250V 3AG FUSE,P/N 440-00860, IN POSITION F1.FOR 100 VAC, INSTALL 0.25A/250V 20MM FUSE,P/N 440-02348, OR FOR 220/240 VAC, INSTALL 0.125/250V 20MM FUSE P/N 440-02347, IN POSITION F2.

(10.) INSERT STRIPPED LEAD OF 22AWG BROWN WIRE,P/N 675-08258, AT J14,AND SOLDER.

(11.) INSERT W4 POST-SOLDER JUMPER AT PINS 1 AND 2.

(12.) INSERT STRIPPED LEAD OF 18 AWG GRN/YEL WIRE P/N 675-08272 THROUGH HOLE IN J13,AND TWIST TOGETHER FOR A GOOD MECHANICAL CONNECTION, BEFORE SOLDERING.

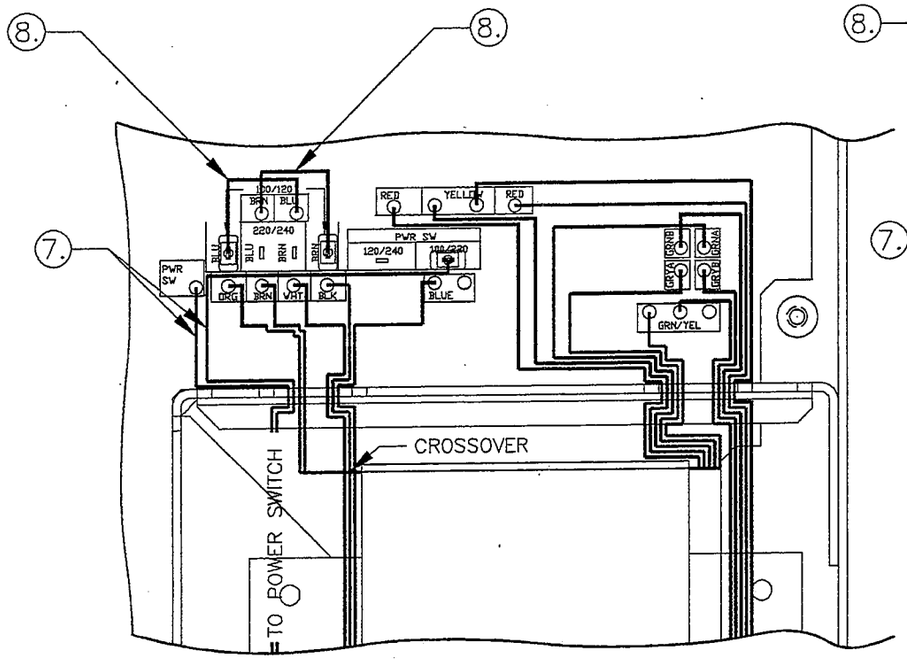
(13.) APPLY A DROP OF CLEAR RTV SILICONE P/N 120-02023 TO PCB,AND FUSE COVERS, BEFORE INSTALLING.

(14.) BREAK AWAY PCB BEFORE INSTALLING IN CHASSIS.

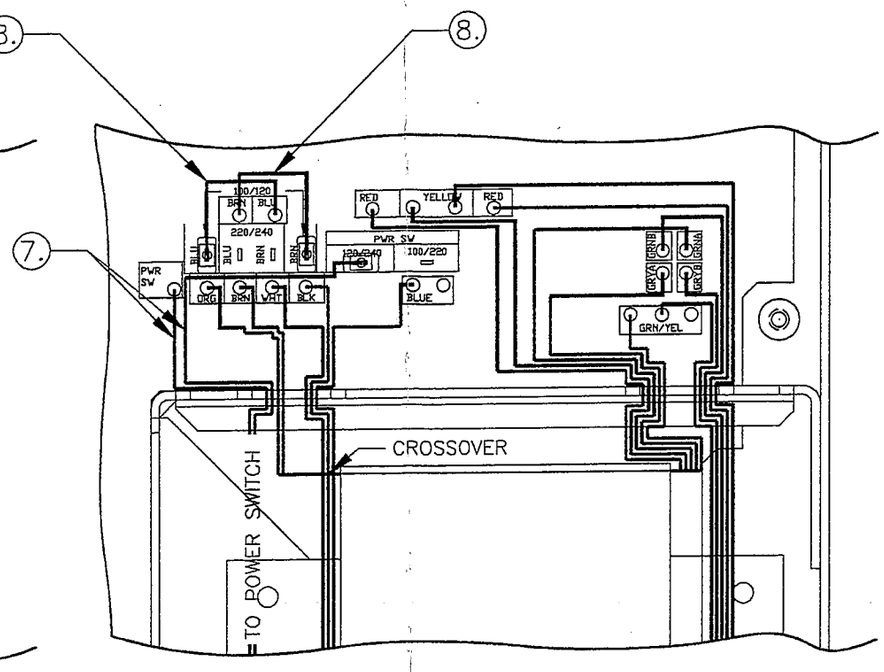
15. PACKAGE COMPLETED ASSEMBLY IN A STATIC SHIELDING BAG TO PREVENT ESD DAMAGE DURING SHIPMENT.

DOCCUMENT CONTROL BLOCK	
SHEET	REVISION
1	0
2	0

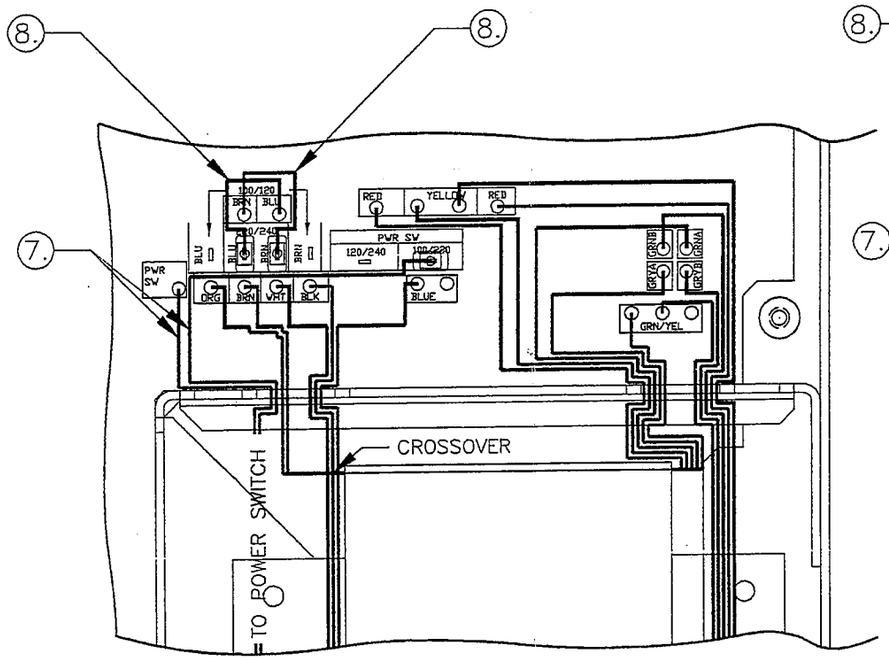
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005	CONTRACT NO. lexicon
		MATERIAL	APPROVALS / DATE: DRAWN JV 11/14/94; CHECKED 11/15/94; Q.C. CW 11/15/94; ISSUED DAM 11/16/94
	710- 10770	FINISH	PC BD, MAIN BD, LXP-15, LC2 ASSEMBLY DRAWING
NEXT ASSY.	USED ON	DO NO SCALE DRAWING	SIZE D; FSCM NO.; DWG. NO. 080-10775; REV 0
APPLICATION			SCALE 1:1; SHEET 1 OF 2



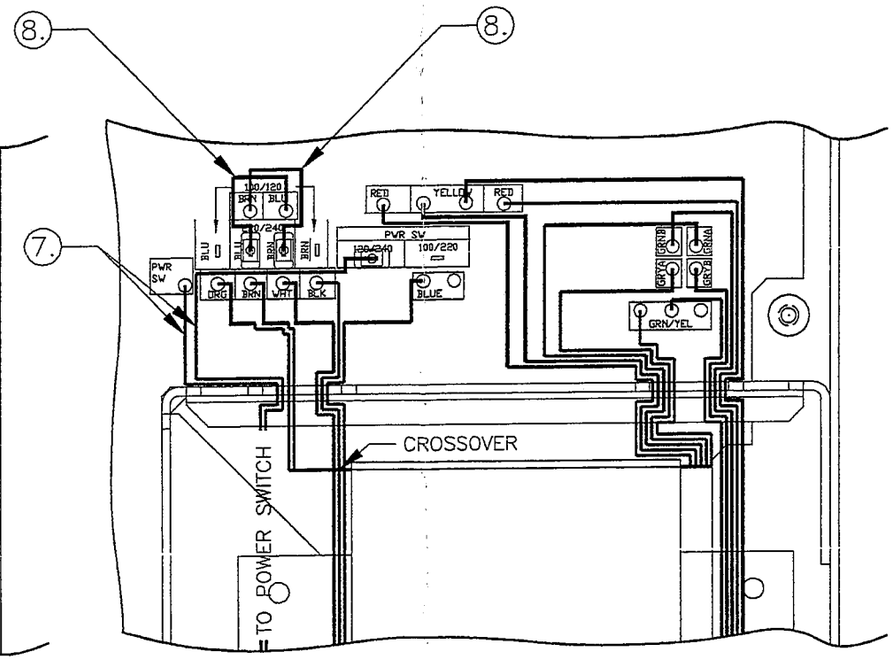
100 VOLTS SELECTION



120 VOLTS SELECTION



220 VOLTS SELECTION



240 VOLTS SELECTION

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH

NOTES

1. REFER TO BOM#'S:023-07855 AND 024-10266.
2. FOR 100VAC, INSTALL FUSE, 5X20MM, SLO-BLO, .250 AMP P/N 440-02348.
3. FOR 120VAC, INSTALL FUSE, 3AG, SLO-BLO, .250 AMP P/N 440-00860.
4. FOR 220/240VAC, INSTALL FUSE, 5X20MM, SLO-BLO, .125 AMP P/N 440-02347.
5. TRANSFORMER SHOWN IS XFORMER, POWER, 15VA, UI75, INTL P/N 470-07889.
6. SOLDER TRANSFORMER WIRES AS SHOWN.
7. FOR POWER SWITCH CONNECTIONS USE WIRE, 22G, BRN, 12", .187QDC/ST P/N 675-08258 & WIRE, 22G, BRN, 12", .187QDCX2 P/N 675-08259.
8. FOR JUMPER VOLTAGE SELECTION USE WIRE, 22G, BLU, 2.5", .187QDC/ST P/N 675-08256 & WIRE, 22G, BRN, 2.5", .187QDC/ST P/N 675-08257 AT POINTS INDICATED.
9. PLACE QDC CONN P/N 490-09182 OVER BARE CONNECTORS.
10. TY-WRAP THE FOLLOWING WIRES TOGETHER APPROXIMATELY 1/2" ABOVE THE P.C. BOARD:
    A. THE ORANGE, BROWN, WHITE, BLACK AND BLUE WIRES FROM THE TRANSFORMER WITH THE BROWN WIRE FROM THE POWER SWITCH.
    B. THE (2) RED AND (2) YELLOW WIRES FROM THE TRANSFORMER.
    C. THE (2) GRAY WIRES FROM THE TRANSFORMER.
    D. THE (2) GREEN WIRES FROM THE TRANSFORMER.
    E. THE (2) GRN/YEL WIRES FROM THE TRANSFORMER.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 12 FILE NAME: 10775-02

APPROVALS	DATE
DRAWN JV	11/14/94
CHECKED	11/14/94
Q.C.	11/15/94
ISSUED JW	11/15/94

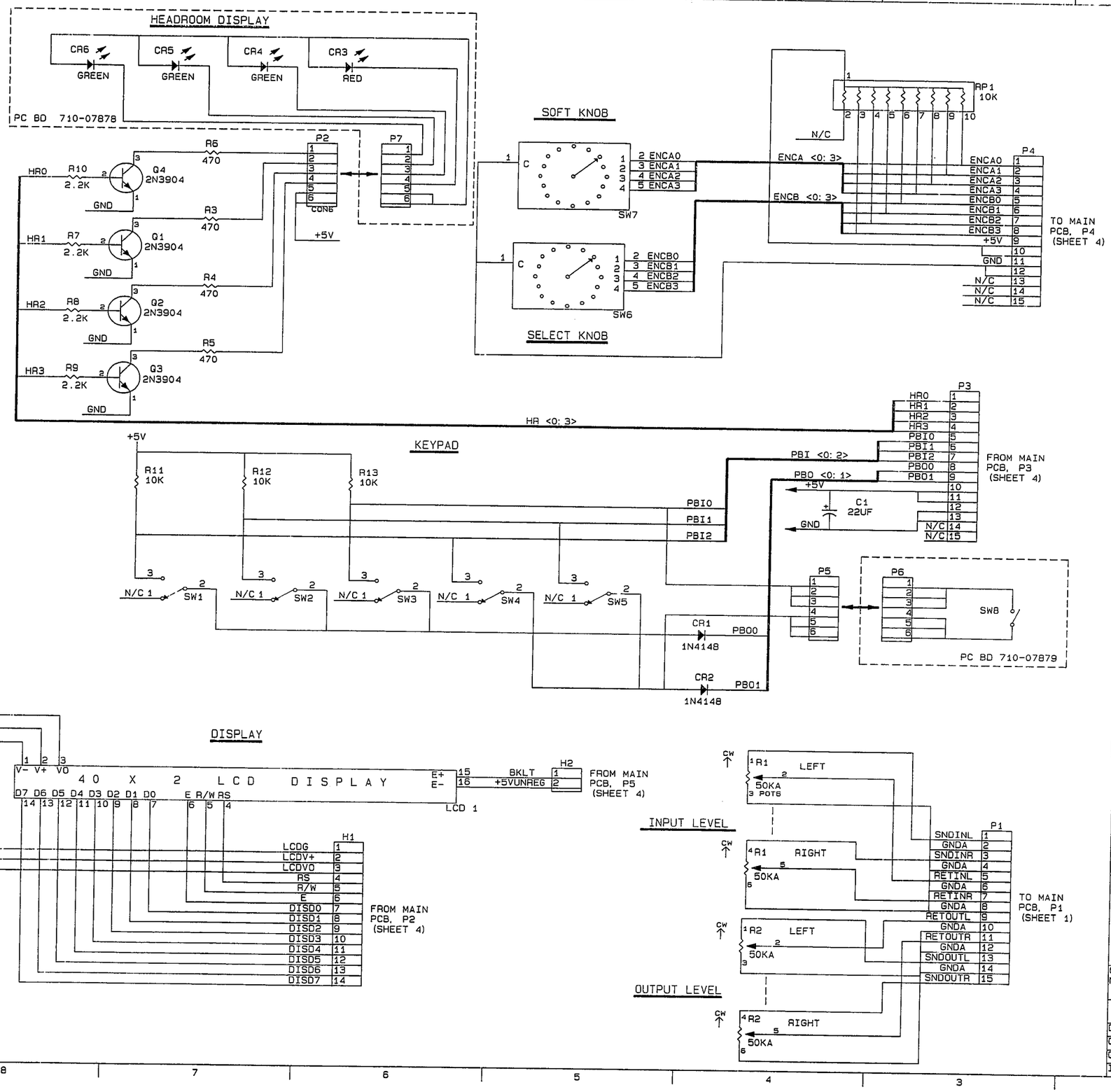
lexicon

TITLE: PC BD,MAIN BD,LXP-15, LC2 ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-10775	0

SCALE N/A SHEET 2 OF 2

LEXICON, INC.



REVISIONS			
REV	DESCRIPTION	DRAFTER/CHECKER	Q.C. / AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 12/11/89	AF 12/11/89
1	RELEASE FOR PRODUCTION	AF 1/11/90	AF 1-11-90

NOTES

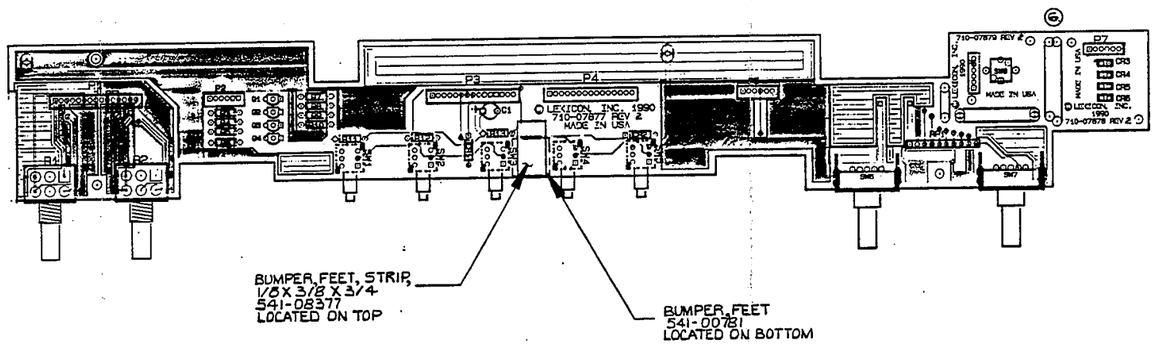
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION

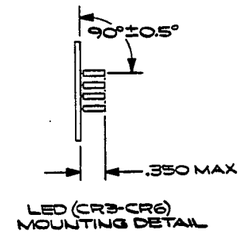
DOCUMENT CONTROL BLOCK #060-07885

SHEET NUMBER	REVISION NUMBER
1 OF 1	1

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154	
APPROVALS	DATE	TITLE: SCHEMATIC, LXP-15 FRONT PANEL
DRAWN MWH	12/11/89	
CHECKED AF	12/11/89	SIZE: D; CODE: ; NUMBER: 060-07885; REV.: 1
Q.C.	12/11/89	
ISSUED	1-11-90	SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.
0	RELEASE FOR PILOT	J.V. 11/15/89 AF 11/16/89	LCM 11/17/89 DWA 11-16-89
1	RELEASE FOR PRODUCTION	J.V. 1/10/90 AF 1/11/90	LCM 1-11-90 1-11-90 DWA
2	ADDITION PER ECO# 900323-00	MAF 4-20-90 LCM 5/25/90	CW 5-11-90 DWA 5/14/90





LED (CR3-CR6)
MOUNTING DETAIL

NOTES

1. ALL COMPONENTS TO BE INSTALLED FROM COMPONENT SIDE OF P.C.B. EXCEPT SWITCHES SW1-5.
2. ALL COMPONENTS ARE POST-SOLDER ASSEMBLED.
3. COMPONENT HEIGHT .90" MAXIMUM
4. LEAD PROTRUSIONS .080" MAXIMUM FROM CIRCUIT SIDE OF P.C.B.
5. SW1-SW7, R1 & R2 ARE TO BE MOUNTED SO SHAFTS ARE PERPENDICULAR TO FRONT EDGE OF P.C.B. (90°±0.5°).
6. INSTALL ALL COMPONENTS & SNAP OFF BREAK-AWAY P.C.B.'S.
7. REFER TO LEXICON BOM#9: 024-07861, 024-07862 & 024-07863.

	710-07877
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.01
.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN J.V.	11/15/89
CHECKED AF	11/16/89
Q.C. LCM	11-16-89
ISSUED DWA	1-11-90

lexicon

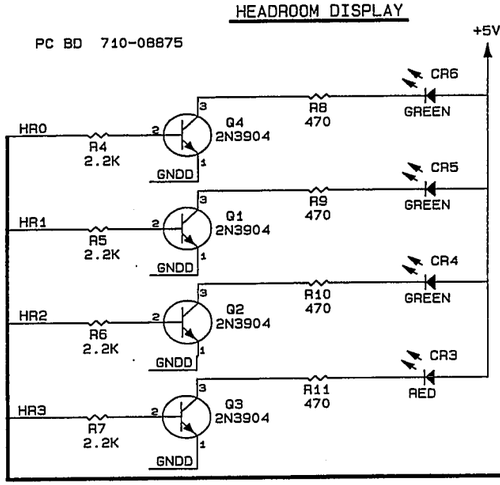
PC BD, FRONT PANEL, LXP-15
ASSEMBLY DRAWING

SIZE D | FSCM NO. | DWG. NO. 080-07884 | REV 2

SCALE 1:1 | SHEET 1 OF 1

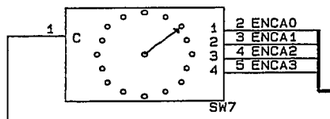
HEADROOM DISPLAY

PC BD 710-08875

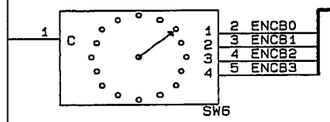


PC BD 710-08877

SOFT KNOB



SELECT KNOB



R14 10K, R15 10K, R16 10K, R17 10K, R18 10K, R19 10K, R20 10K, R21 10K

ENCA <0:3>

ENCB <0:3>

P4

ENCA0	1
ENCA1	2
ENCA2	3
ENCA3	4
ENCB0	5
ENCB1	6
ENCB2	7
ENCB3	8
+5V	9
	10
GND	11
	12
N/C	13
N/C	14
N/C	15

HR <0:3>

P3

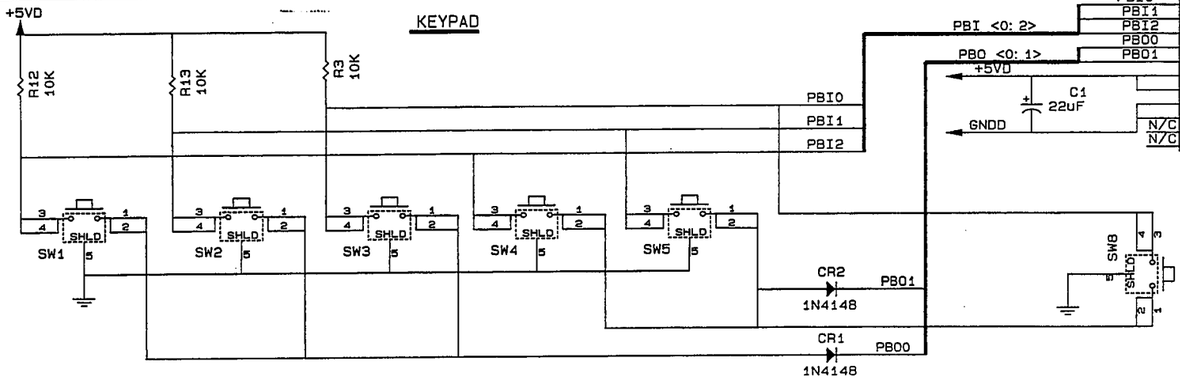
HR0	1
HR1	2
HR2	3
HR3	4
PBI0	5
PBI1	6
PBI2	7
PB00	8
PB01	9
	10
	11
	12
	13
N/C	14
N/C	15

FROM MAIN PCB, P3

PBI <0:2>

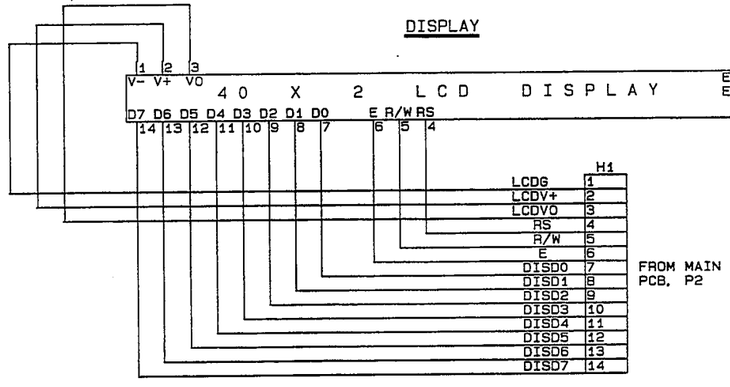
PBO <0:1>

KEYPAD



PC BD 710-08876

DISPLAY

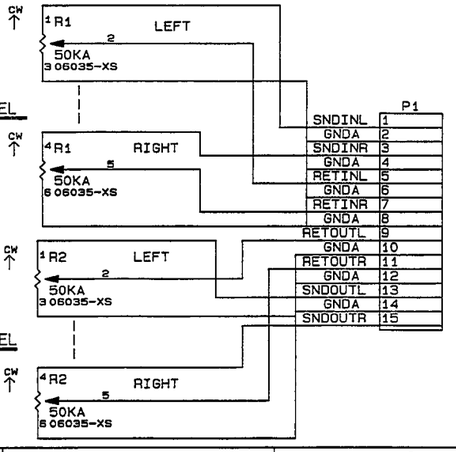


FROM MAIN PCB, P5

FROM MAIN PCB, P2

INPUT LEVEL

OUTPUT LEVEL



P1

SNDINL	1
GNDA	2
SNDINR	3
GNDA	4
RETINL	5
GNDA	6
RETINR	7
GNDA	8
RETOUTL	9
GNDA	10
RETOUTR	11
GNDA	12
SNDOUTL	13
GNDA	14
SNDOUTR	15

TO MAIN PCB, P1

REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PRODUCTION	MW 5/13/91	MW 5/22/91
		DNH 5/14/91	DNH 6/4/91

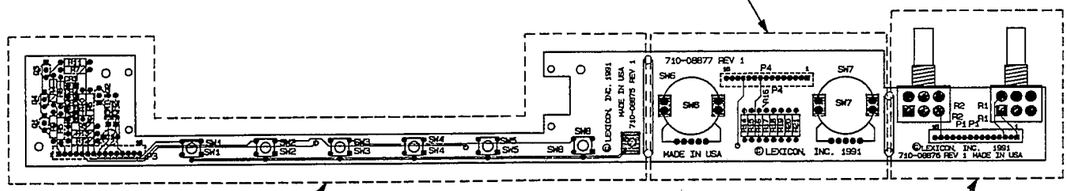
NOTES

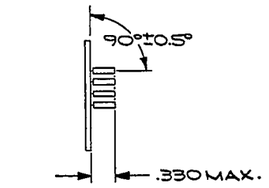
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE: SCHEMATIC, LXP-15X FRONT PANEL	
DRAWN RR	5/13/91		
CHECKED DNH	5-14-91	SIZE: D	CODE:
Q.C. MW	5-22-91	NUMBER: 060-08884	REV.: 0
ISSUED DNH	6-14-91	SHEET 1 OF 1	

REV	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.
0	RELEASE FOR PRODUCTION	JV 6/11/91	CW 6/12/91
		DHP 6/12/91	DHP 6/14/91

REFER TO PL,FP ENCODE BD ASSY,LXP-15X Ⓢ
P/N 025-08898 (INSTALL P4 ON SOLDER-
SIDE OF P.C.B.)





LED'S CR3-6
MOUNTING DETAIL

REFER TO PL,FP MAIN BD ASSY,LXP-15X Ⓢ
P/N 025-08896 (INSTALL CR3-6 & SW1-5
ON COMPONENT SIDE,ALL OTHER
PARTS ARE ON SOLDERSIDE OF P.C.B.

REFER TO PL,FP GAIN BD ASSY,LXP-15X Ⓢ
P/N 025-08897

NOTES

1. REFER TO LEXICON BOM NO. 025-08896, 025-08897, 025-08898
2. ALL COMPONENTS TO BE INSTALLED FROM COMPONENT SIDE OF PCB EXCEPT SWAGED STANDOFFS UNLESS OTHERWISE INDICATED.
3. MASKING FOR POST-SOLDER ASSEMBLY IS INDICATED BY SOLID AREAS
4. COMPONENT HEIGHT .900" MAXIMUM.
5. LEAD PROTRUSIONS .080" MAXIMUM FROM CIRCUIT SIDE OF PCB.
Ⓢ INSTALL ALL COMPONENTS & SNAP OFF BREAK-AWAY P.C.B.'S.

710-08875	
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .01 .005
MATERIAL
FINISH
DO NO SCALE DRAWING

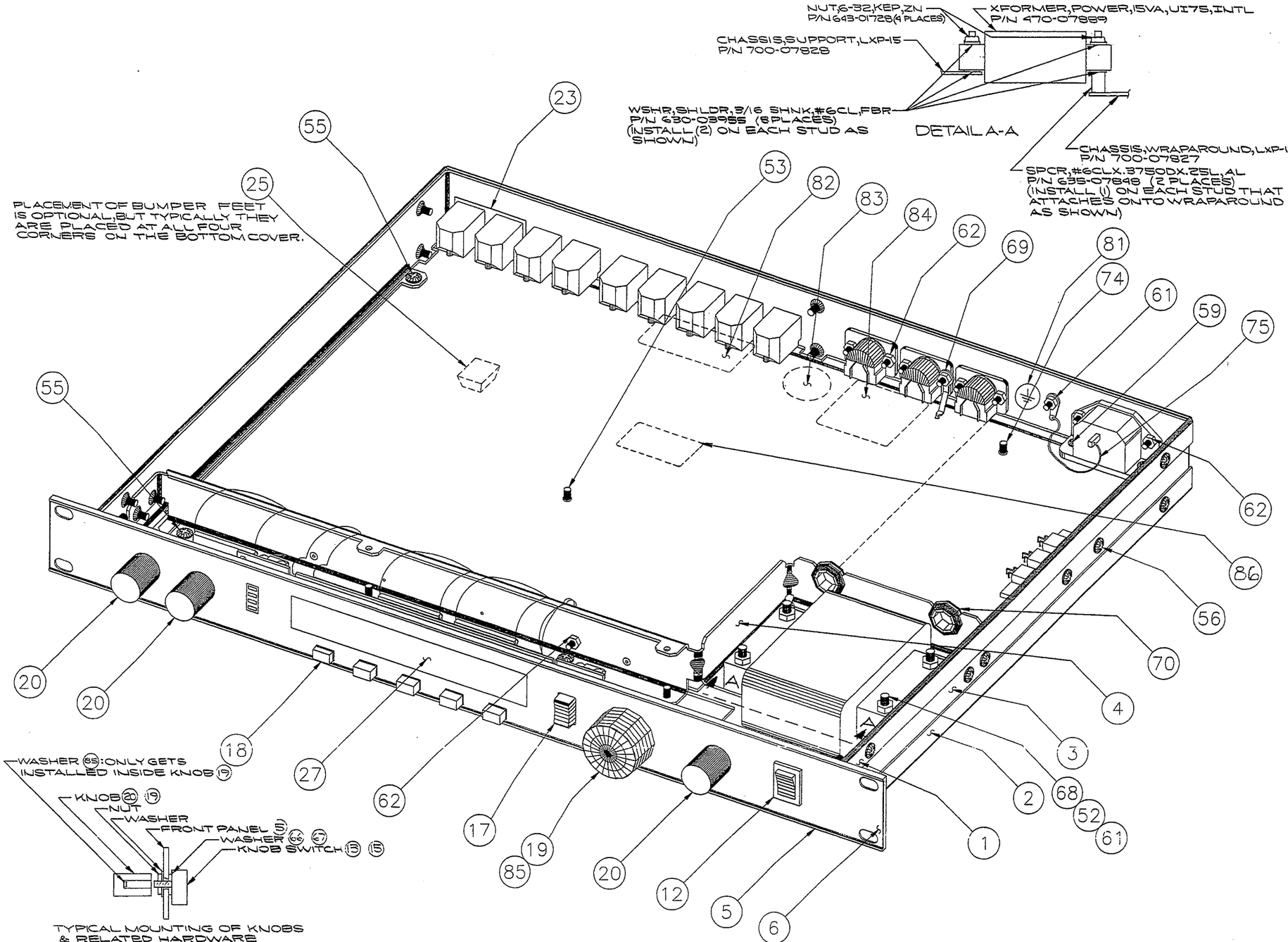
CONTRACT NO.

APPROVALS	DATE
DRAWN JV	6/11/91
CHECKED DHP	6/14/91
Q.C. CW	6/12/91
ISSUED DHP	6/12/91

lexicon

PC BD, FRONT PANEL, LXP-15X
ASSEMBLY DRAWING

SIZE D | FSCM NO. | DWG. NO. 080-08883 | REV 0
SCALE 1:1 | SHEET 1 OF 1



REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	JV 6/19/90 AF 8/9/90	[illegible] 8/13/90
1	ADDITIONS PER ECOS #'S 900906-00 AND 900919-00	[illegible] 10-11-90 AF 10/17/90	[illegible] 11/16/90
2	CHANGED SHEETS 2 & 3 AND UPDATED DOC. CTL BLK PER ECO#930616-00	JV 6/24/93 AF 7/29/93	[illegible] 7-26-93

NOTES

1. REFER TO SHEET 3 FOR PART NUMBER LISTING.

DOCUMENT CONTROL BLOCK	
SHEET	REVISION
1	2
2	1
3	2

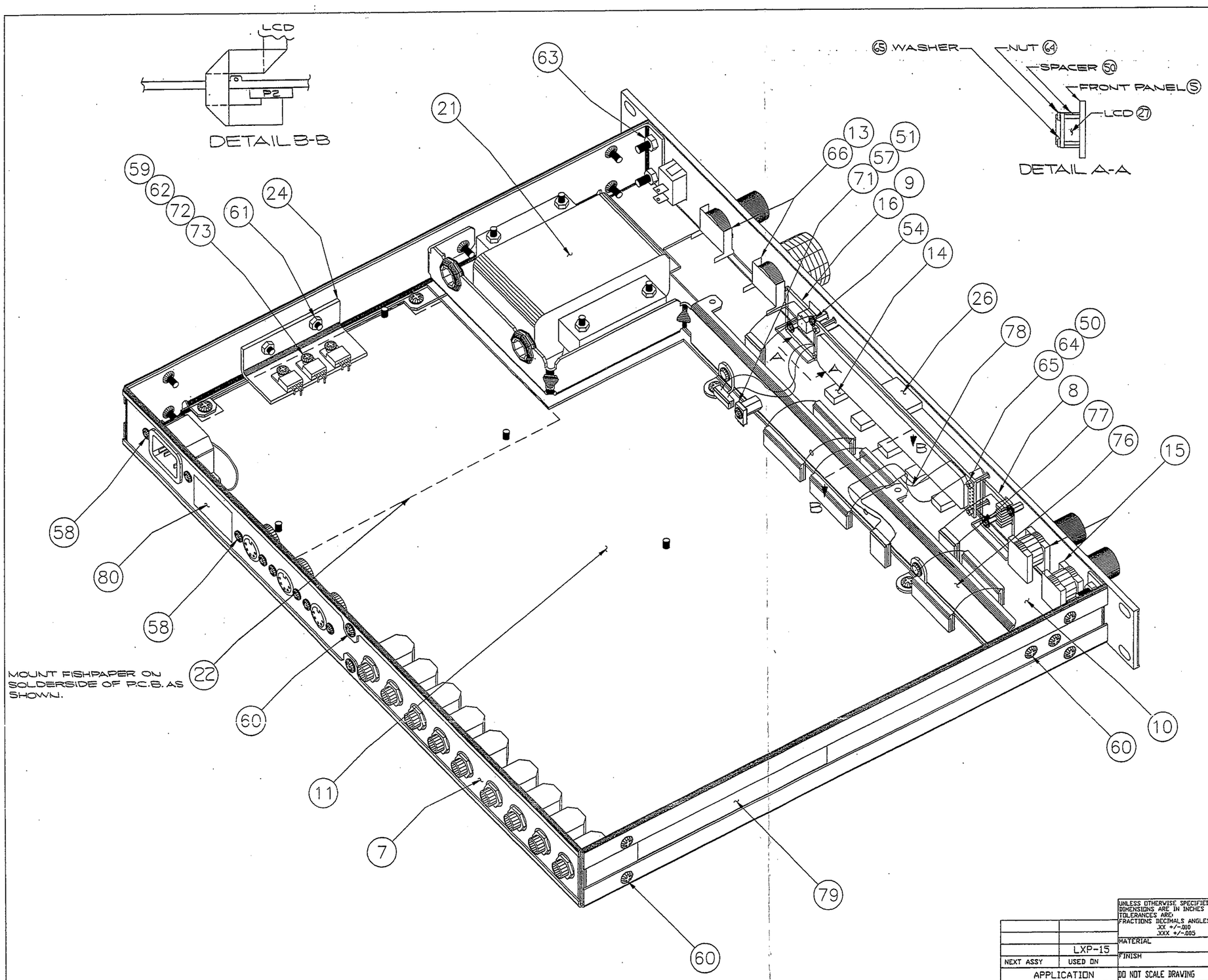
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX +/-.010 XXX +/-.005	ACAD REL 10 FILE NAME 07830S1
		MATERIAL	APPROVALS / DATE
	LXP-15	FINISH	DRAWN JV 6/19/90
NEXT ASSY	USED ON		CHECKED AF 8/9/90
APPLICATION		DO NOT SCALE DRAWING	Q.C. [illegible] 8/13/90
			ISSUED [illegible] 8/13/90

lexicon

TITLE: ASSY DWG CHASSIS, LXP-15

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-07830	2

SCALE N/A



REVISIONS			
REV.	DESCRIPTION	DVR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	JV 6/19/90 AF 8/9/90	cw 9/13/90 DWH 9/13/90
1	DELETE (67) PER ECO#930616-00	JV 6/24/93 AF 7/12/93	JV 7/9/93 DWH 7-26-93

NOTES

1. REFER TO SHEET 3 FOR PART NUMBER LISTING.

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX +/-.010 .XXX +/-.005	ACAD REL 10 FILE NAME 07830S2
		MATERIAL	APPROVALS / DATE
	LXP-15	FINISH	DRAWN JV 6/19/90
NEXT ASSY	USED ON		CHECKED AF 8/9/90
APPLICATION		DO NOT SCALE DRAWING	Q.C. cw 9/13/90
			ISSUED DWH 9/13/90

Lexicon

TITLE: ASSY DWG, CHASSIS, LXP-15

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-07830	1

SCALE N/A SHEET 2 OF 3

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	JV 6/12/90 A 8/9/90	CW 8/13/90
1	ADDITIONS PER ECOS# 900906-00 AND 900919-00	MLX 10-11-90 A 10/15/90	CW 10/16/90
2	CHANGED (15) & DELETE (67) PER ECO# 930616-00	JV 6/28/93	CW 7/9/93

PARTS LIST
(SEE NOTE #1)

ITEM#	COMPONENT#	DESCRIPTION	QTY	WHERE USED
1.	700-07825	COVER, TOP, LXP-15	1	
2.	700-07826	COVER, BOTTOM, LXP-15	1	
3.	700-07827	CHASSIS, WRAPAROUND, LXP-15	1	
4.	700-07828	CHASSIS, SUPPORT, LXP-15	1	
5.	702-07820	PANEL, FRONT, LXP-15	1	
6.	703-07821	PANEL, OVLY, FRONT, LXP-15	1	
7.	703-07823	PANEL, OVLY, REAR, LXP-15	1	
8.	024-07861	PL, FP LED BD ASSY, LXP-15	1	
9.	024-07862	PL, FP SW BD ASSY, LXP-15	1	
10.	024-07863	PL, FP MAIN BD ASSY, LXP-15	1	
11.	023-08278	PL, MAIN BD ASSY, LXP-15, 100V	1	
	023-07856	PL, MAIN BD ASSY, LXP-15, 120V	1	
	023-07867	PL, MAIN BD ASSY, LXP-15, 220/240V	1	
12.	454-03900	SW, ROCKER, 1P1T, QDC, INTL LINE	1	
13.	452-07887	SW, RTY, GRAY CODE, 16 POS	2	SW6,7
14.	453-07837	SW, PBM, 2P2T, PCRA, LO-PRO	5	SW1-5
15.	200-09545	POT, RTY, PC, 50KAX2, 6MMFL,16,17L	2	R1,R2
16.	453-07554	SW, PBM, 1P1T, PC, 1MM, TRAV	1	SW8
17.	550-07575	BUTTON, .335X.592, BLK	1	
18.	550-07836	BUTTON, .39X.22X.44, BLK	5	
19.	550-04212	KNOB, 1.00, 6MM/ROUND, BLK	1	
20.	550-08254	KNOB, .66, 6MM, FL, BLK/BOT, WHT LN	3	
21.	470-07889	XFORMER, POWER, 15VA, UI75, INTL	1	
22.	702-07845	COVER, PROTECTIVE, AC, LXP-15	1	
23.	702-07842	INSUL, GSKT, .406X2@.875, FSH/AD	1	
24.	704-07829	HEATSINK, LXP-15	1	
25.	541-00781	BUMPER, FEET, 3-M# SJ5018	4	
26.	541-08377	BUMPER, FEET, STRIP, 1/8X3/8X3/4L	1	
27.	430-07847	DISP, LCD, 40X2, NEG, 12:00, LED, AM	1	
50.	630-07886	SPCR, #2CLX3/8, 3/16 RD, NYL	4	LCD TO FRT PANEL
51.	635-07841	SPCR, #4CLX3/8, 5/16 HEX, AL	1	TO-126
52.	635-07848	SPCR, #6CLX.375ODX.25L, AL	2	XFRMR TO CHASSIS WRAP
53.	630-07846	SPCR, PCB/FOOT, .250 NYL	1	PCB SUPPORT
54.	640-04339	SCRW, 4-40X1/4, PNH, PH, SEMS, ZN FP SW BD TO FP (2)	4	FP LED BD TO FP (2)
55.	640-01710	SCRW, 6-32X1/4, PNH, PH, ZN FP SW BD TO CHAS SUPPORT (2)	8	MAIN BD TO CHAS WRAP & SUPT (6)
56.	640-01713	SCRW, 6-32X5/16, PNH, PH, ZN	2	HEATSINK TO CHAS WRAP
57.	640-02467	SCRW, 4-40X7/8, PNH, PH, ZN	1	TO-126 TO CHAS SUPPORT
58.	640-02812	SCRW, 4-40X3/8, PNH, PH, BLK AC CONN TO CHAS WRAP (2)	8	DIN CONN TO CHAS WRAP (6)
59.	640-01706	SCRW, 4-40X3/8, PNH, PH, ZN AC CONN TO MAIN BD (2)	5	H/S TO MAIN BD (3)
60.	641-06575	SCRW, TAP, C, 6-32X1/4, THG, PH, BLK BOTTOM COVER TO CHAS WRAP (7) TOP COVER TO CHAS WRAP (7)	18	CHAS SUP TO CHAS WRAP (4);
61.	643-01728	NUT, 6-32, KEP, ZN HEATSINK TO CHAS WRAP (2)	7	XFORMER (4); GND (1);
62.	643-01732	NUT, 4-40, KEP, ZN AC CONN TO MAIN BD (2); H/S TO MAIN BD (3)	14	DIN CONN TO CHAS WRAP (6); AC CONN TO CHAS WRAP (2) TO-126 (1)
63.	643-01734	NUT, 8-32, KEP, ZN	4	CHAS WRAP TO FRONT PANEL
64.	643-08250	NUT, 2-56, HEX, NYL	4	LCD TO FRONT PANEL
65.	644-06635	WSHR, INT STAR, #2, ZN	4	LCD TO FRONT PANEL
66.	644-07893	WSHR, FL, .427IDX.550X.035THK, ZN	3	SW6,7
68.	630-03955	WSHR, SHLDR, 3/16 SHNK, #6CL, FBR	8	XFORMER MTG
69.	620-08252	LUG, PCB/#4CL	1	MAIN PCB - J11 MTG
70.	540-00874	GROMMET, 9/16 OD, 7/16 ID	2	CHAS SUPPORT
71.	630-08260	INSUL, SEMI, SIL RUB, TO-126	1	TO-126 TO CHASSIS SUPPORT
72.	630-00952	INSUL, SEMI, BUSHING, TO-220	3	H/S TO MAIN BD
73.	630-07339	INSUL, SEMI, SIL RUB, TO-220 SHORT	3	H/S TO MAIN BD
74.	650-07551	RVT, SNAP-IN, .16DIA, NYL	4	PROT COVER
75.	675-08272	WIRE, 18G, GRN/YEL, 3", #6RING/SS	1	J13
76.	680-07897	CABLE, 079, SCKT/BICONN, 15C, 3.0"	3	P1, 3, 4
77.	680-07898	CABLE, 079, SCKT/BICONN, 6C, 2.0"	2	P6, 7
78.	680-08356	CABLE, ASSY, 2C, 22G, 7", SS/HSG	1	LCD
79.	740-08373	LABEL, CAUTION, LO-PRO	1	LEFT SIDE (REAR)
80.	740-08375	LABEL, S/N+ELEC, 1.40CX.625	1	REAR PANEL
81.	740-08556	LABEL, GROUND SYMBOL, 0.5" DIA	1	INSIDE REAR PANEL
82.	740-05471	LABEL, CSA CERTIFIED, COMMERCIAL	1	BOTTOM COVER (120V ONLY)
83.	740-08585	LABEL, CLA APPROVAL,LXP15	1	BOTTOM COVER (120V ONLY)
84.	740-08558	LABEL, TUV CERTIFIED, BAYERN	1	BOTTOM COVER (220/240V ONLY)
85.	644-07090	WSHR, INT STAR, M2.7, ZN	1	INSIDE SW6 KNOB
86.	740-08589	LABEL, RACK MOUNT ONLY	1	BOTTOM COVER (120V ONLY)

NOTES

1. PART NUMBER LISTING IS REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILL OF MATERIAL #020-07850, 020-07890, 020-08264 & 020-08265.
2. ITEM#65 IS OPTIONAL. APPLY LOCTITE TO STUDS & #64 AFTER TIGHTENING.

NEXT ASSY	USED ON
	LXP-15
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX +/-.010 .XXX +/-.005

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD REL 10 FILE NAME 07830S3

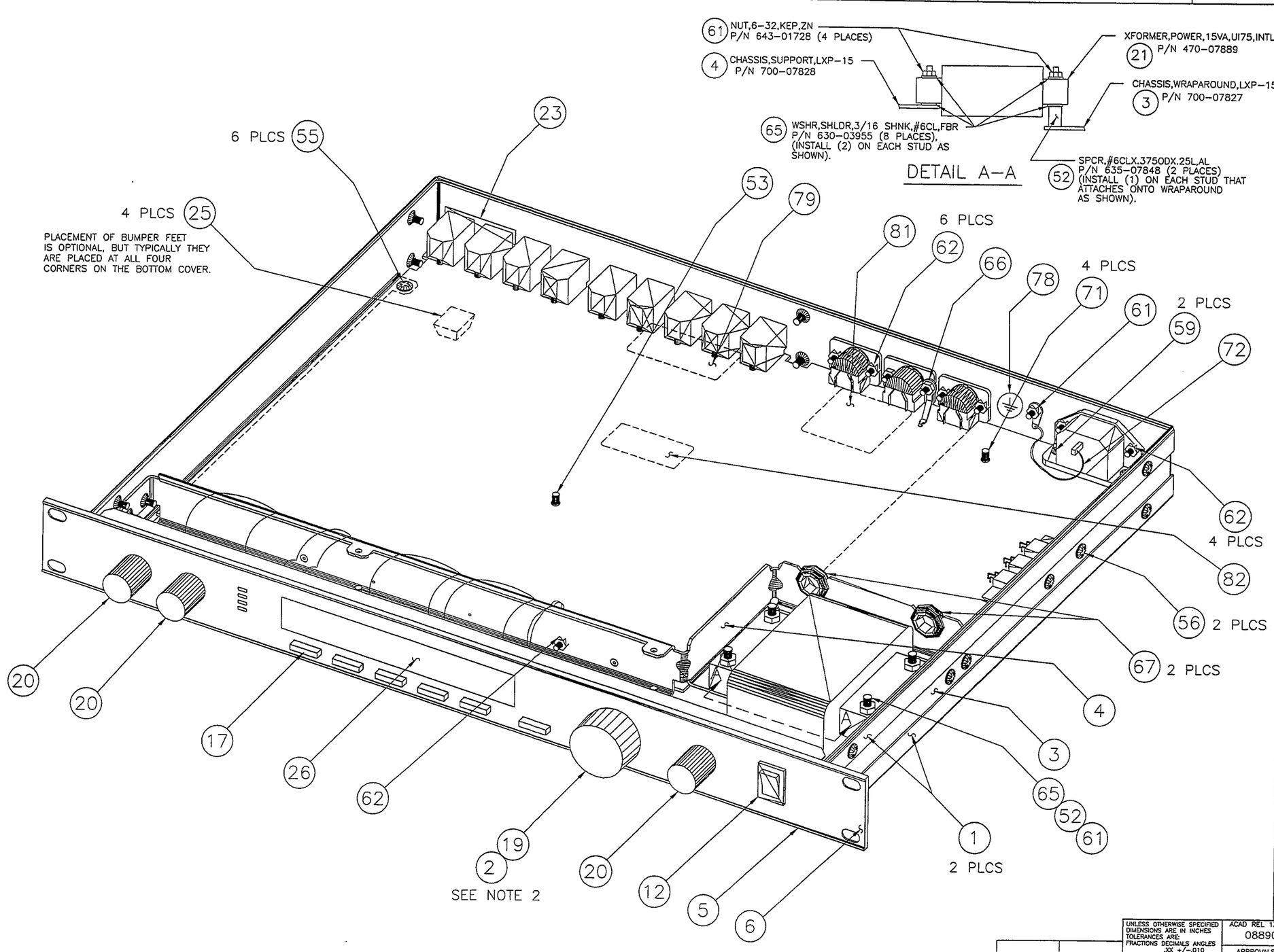
APPROVALS	DATE
DRAWN JV	6/12/90
CHECKED	8/9/90
Q.C. CW	8/13/90
ISSUED	8/13/90

Lexicon

TITLE ASSY DWG CHASSIS, LXP-15

SIZE D | FSCM NO. | DWG. NO. 080-07830 | REV. 2

SCALE N/A | SHEET 3 OF 3



REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	AN 6/11/91 DHS 6/11/91	CW 6/11/91 DHS 6/11/91
1	TOP & BOTTOM COVERS SAME P/N-ITEM 1, CHG'D SHTS 1,4, UPDATED DOC CTL BLK PER ECO #910716-00-A	JV 9/13/91 AN 9/16/91	CW 9/18/91 DHS 9/18/91
2	CHANGED ITEM 77 TO PRODUCT ID LABEL PER ECO #911114-01	MAF 12/4/91 MK 12/20/91	CW 12/20/91 DHS12/20/91
3	ADD ITEM 2 (RTV) & NOTE 2,UPDATED DOC CTL BLK PER ECO #920225-00	JV 3/5/92 MK 3/6/92	CW 3/9/92 DHS3/11/92
4	MOVE CLA LABEL 80 PER DCR #920408-00	JV 4/21/92 CLC 4/21/92	CW 4/22/92 DHS4/22/92
5	UPDATED DOC. CTL BLK PER ECO #920717-01	MAF 7/27/92 AN 7/29/92	CW 8/3/92 DHS 8/3/92
6	CHANGED SHEETS 3 & 4, AND UPDATED DOC. CTL BLK PER ECO #930616-00	JV 6/24/93 MK 7/8/93	CW 7/9/93 DHS 7/26/93
7	CHANGED SHEET 4 AND UPDATED DOC. CTL BLK PER ECO #940524-00	JV 6/28/94 MK 6/30/94	CW 7/6/94 JW 7/7/94
8	ADDED CE LABEL ITEM 83 PER ECO #960529-00	AN 6/6/96 MK 6/7/96	CW 6/7/96 DHS 6/7/96

NOTES

1. REFER TO SHEET 4 FOR PART NUMBER LISTING.
2. OPTIONAL USE OF RTV P/N 120-02023 IF KNOB/SHAFT FIT TOO LOOSE.

DOCUMENT CONTROL BLOCK	
SHEET	REVISION
1	8
2	2
3	3
4	7

NEXT ASSY	LXP-15X
USED ON	
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 08890-81

APPROVALS	DATE
DRAWN AN	5/15/91
CHECKED DHS	6/11/91
Q.C. CW	6/11/91
ISSUED DHS	6/11/91

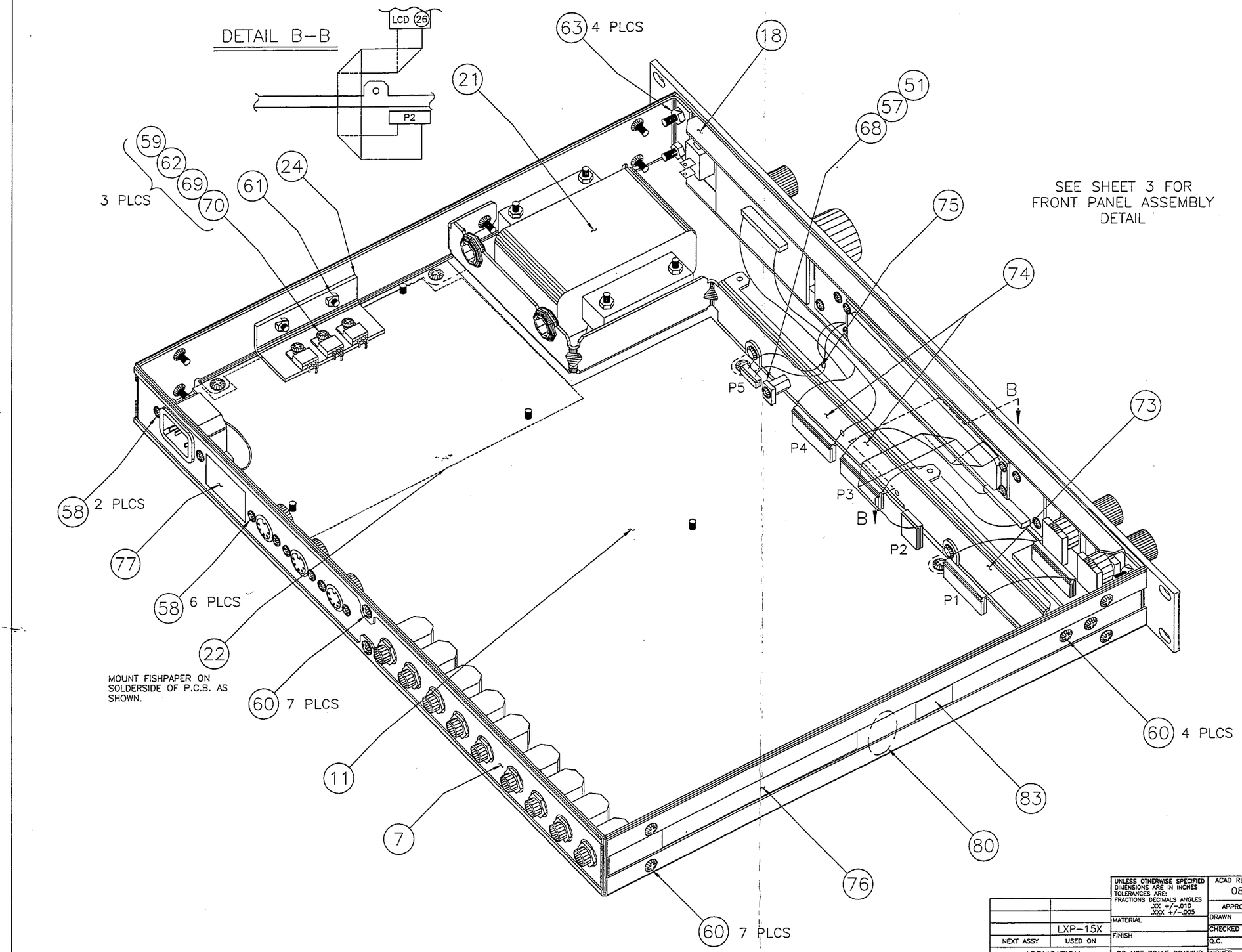
lexicon

TITLE: ASSY DWG, CHASSIS, LXP-15X

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-08890	8

SCALE N/A SHEET 1 OF 4

LEXICON INC. 5/91



REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	AN 6/11/91 DHS 6/11/91	CW 6/11/91 DHS 6/11/91
1	MOVE CLA LABEL 80 PER DCR #920408-00	JV 4/21/92 CLC 4/21/92	CW 4/22/92 DHS 4/22/92
2	ADD CE LABEL ITEM 83 PER ECO #960529-00	AN 6/6/96 MK 6/7/96	CW 6/7/96 DHS 6/7/96

NOTES

1. REFER TO SHEET 4 FOR PART NUMBER LISTING.

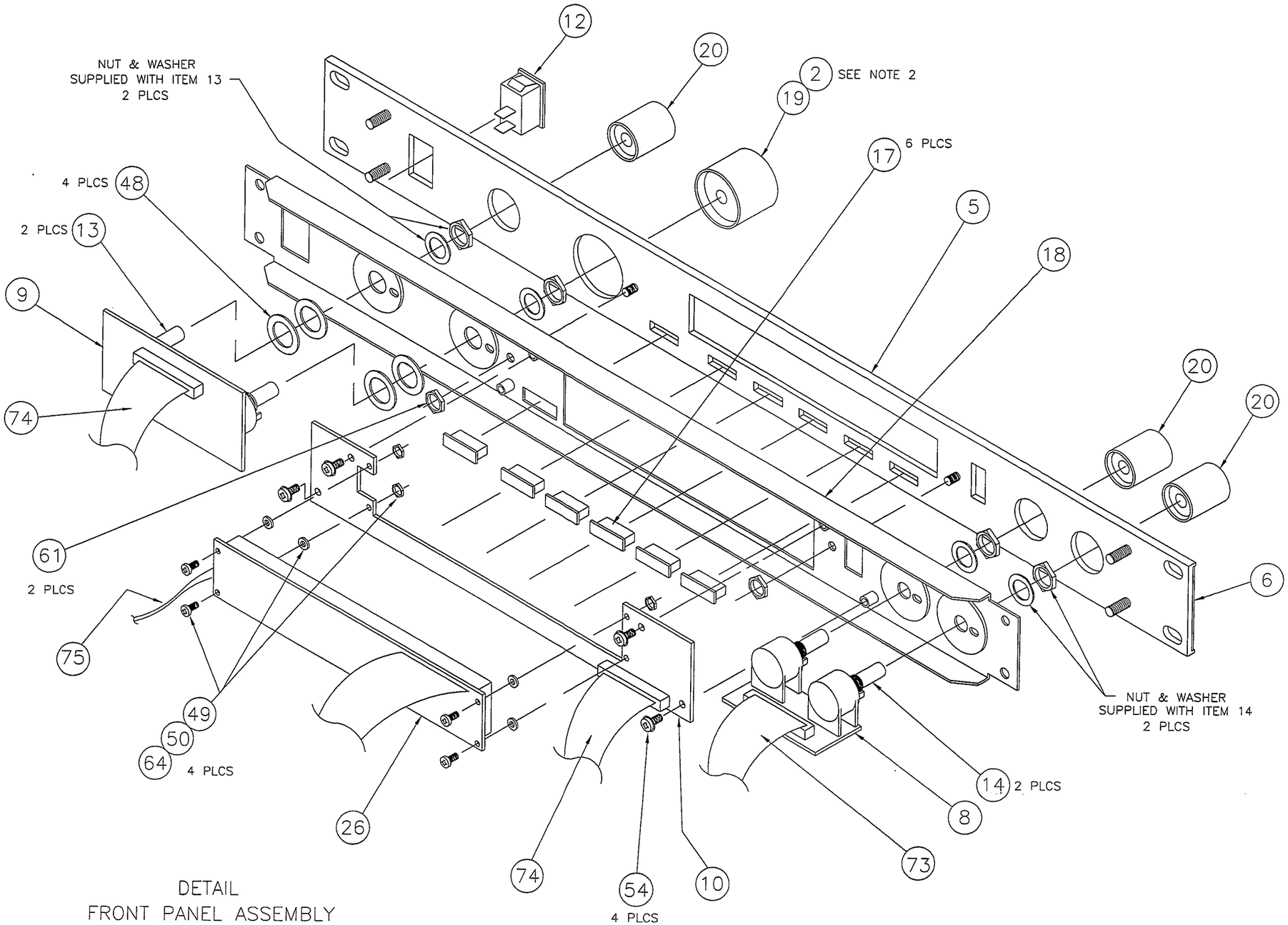
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX +/-.010 .XXX +/-.005	ACAD REL 13 FILE NAME 08890-22
		MATERIAL	APPROVALS / DATE
	LXP-15X	FINISH	DRAWN AN 5/15/91
NEXT ASSY	USED ON		CHECKED DHS 6/11/91
APPLICATION		DO NOT SCALE DRAWING	Q.C. CW 6/11/91
			ISSUED DHS 6/11/91

lexicon

TITLE: ASSY DWG, CHASSIS, LXP-15X

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-08890	2

SCALE N/A SHEET 2 OF 4



DETAIL
FRONT PANEL ASSEMBLY

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	AN 6/11/91 DHS 6/11/91	CW 6/11/91 DHS 6/11/91
1	ADD ITEM 2(RTV) & NOTE 2 PER ECO# 920225-00	JV 3/5/92 MK 3/6/92	CW 3/9/92 DHS 3/11/92
2	ADD ITEM 47 & CHG QTY OF ITEM 48 PER ECO #920717-01	MF 7/27/92 AN 7/29/92	CW 8/3/92 DHS 8/3/92
3	DELETE ITEM 47 PER ECO #930616-00	JV 6/24/93 MK 7/9/93	CW 7/9/93 DHS 7/26/93

NOTES

1. REFER TO SHEET 4 FOR PART NUMBER LISTING.
2. OPTIONAL USE OF RTV P/N 120-02023 IF KNOB/SHAFT FIT IS TOO LOOSE

NEXT ASSY	USED ON
APPLICATION	LXP-15X

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 08890-33

APPROVALS		DATE
DRAWN	AN	6/3/91
CHECKED	DHS	6/11/91
Q.C.	CW	6/11/91
ISSUED	DHS	6/11/91

lexicon

TITLE: ASSY DWG, CHASSIS, LXP-15X

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-08890	3

SCALE N/A SHEET 3 OF 4

PARTS LIST (SEE NOTE #1)

ITEM#	COMPONENT#	DESCRIPTION	QTY	WHERE USED
1.	700-07825	COVER, TOP/BOTTOM, LXP-15	2	
2.	120-02023	ADHESIVE SILICONE,RTV,CLEAR	.003 OZ	
3.	700-07827	CHASSIS, WRAPAROUND, LXP-15	1	
4.	700-07828	CHASSIS, SUPPORT, LXP-15	1	
5.	702-08886	PANEL, FRONT, LXP-15X	1	
6.	703-08887	PANEL, OVLY, FRONT, LXP-15X	1	
	703-10276	PANEL, OVLY, FRONT, LXP-15II	1	
7.	703-07823	PANEL, OVLY, REAR, LXP-15	1	
8.	025-08897	PL, FP GAIN BD ASSY, LXP-15X	1	
9.	025-08898	PL, FP ENCODE BD ASSY, LXP-15X	1	
10.	025-08896	PL, FP MAIN BD ASSY, LXP-15X	1	
11.	023-08278	PL, MAIN BD ASSY, LXP-15, 100V	1	
	023-07856	PL, MAIN BD ASSY, LXP-15, 120V	1	
	023-08756	PL, MAIN BD ASSY, LXP-15, 220V	1	
	023-07867	PL, MAIN BD ASSY, LXP-15, 240V	1	
	023-10262	PL, MAIN BD ASSY, LXP-15II, 100V	1	
	023-10263	PL, MAIN BD ASSY, LXP-15II, 120V	1	
	023-10264	PL, MAIN BD ASSY, LXP-15II, 220V	1	
	023-10265	PL, MAIN BD ASSY, LXP-15II, 240V	1	
12.	454-03900	SW, ROCKER, 1P1T, QDC, INTL LINE	1	
13.	452-08891	SW, RTY, GRAY CODE, 16 POS, PVB	2	SW6,7
14.	200-09545	POT, RTY, PC, 50KAX2, 6MMFL, 16, 17L	2	R1,R2
17.	550-08889	BUTTON, .150 X .600, BLK	6	
18.	700-08885	CHASSIS, INSERT, FP, LXP-15X	1	
19.	550-04212	KNOB, 1.00, 6MM/ROUND, BLK	1	
20.	550-09118	KNOB, 17MM, 6MM/FL, BLK/WHT LN	3	
21.	470-07889	XFORMER, POWER, 15VA, UI75, INTL	1	
22.	702-07845	COVER, PROTECTIVE, AC, LXP-15	1	
23.	702-07842	INSUL, GSKT, .406X2@.875, FSH/AD	1	
24.	704-07829	HEATSINK, LXP-15	1	
25.	541-00781	BUMPER, FEET, 3-M# SJ5018	4	
26.	430-07847	DISP, LCD, 40X2, POS, 12:00, LED, AM	1	(WITH CABLE)
48.	644-07893	WSHR, FL .427 ID X.550 X.035THK, ZN	4	SW6,7
49.	643-01855	NUT, 2-56, HEX, ZN	4	LCD TO FP MAIN BD
50.	644-08899	WSHR, FL #2CL X.1860D X.03 THK, NYL	4	LCD TO FP MAIN BD
51.	635-07841	SPCR, #4CLX3/8, 5/16 HEX, AL	1	TO-126
52.	635-07848	SPCR, #6CLX.3750DX.25L, AL	2	XFRMR TO CHASSIS WRAP
53.	630-07846	SPCR, PCB/FOOT, .250 NYL	1	PCB SUPPORT
54.	640-04339	SCRW, 4-40X1/4, PNH, PH, SEMS, ZN	4	FP MAIN BD TO INSERT
55.	640-01710	SCRW, 6-32X1/4, PNH, PH, ZN	6	MAIN BD TO CHAS WRAP & SUPT
56.	640-01713	SCRW, 6-32X5/16, PNH, PH, ZN	2	HEATSINK TO CHAS WRAP
57.	640-02467	SCRW, 4-40X7/8, PNH, PH, ZN	1	TO-126 TO CHAS SUPPORT
58.	640-02812	SCRW, 4-40X3/8, PNH, PH, BLK	8	DIN CONN TO CHAS WRAP (6)
				AC CONN TO CHAS WRAP (2)
59.	640-01706	SCRW, 4-40X3/8, PNH, PH, ZN	5	H/S TO MAIN BD (3)
				AC CONN TO MAIN BD (2)
60.	641-06575	SCRW, TAP, C, 6-32X1/4, THG, PH, BLK	18	CHAS SUP TO CHAS WRAP (4);
				COVERS TO CHAS WRAP (14)
61.	643-01728	NUT, 6-32, KEP, ZN	9	XFORMER (4); GND (1);
				INSERT TO FRT PNL (2)
				HEATSINK TO CHAS WRAP (2)
62.	643-01732	NUT, 4-40, KEP, ZN	14	DIN CONN TO CHAS WRAP (6);
				AC CONN TO BD & CHAS (4)
				H/S TO MAIN BD (3) TO-126 (1)
63.	643-01734	NUT, 8-32, KEP, ZN	4	CHAS WRAP TO FRONT PANEL
64.	640-01841	SCRW, 2-56X1/4, PNH, PH, ZN	4	LCD TO FP MAIN BD

TORQUE
B
B
C
A
A
A
B
F
F
G
G
E
D
D
A
H

TORQUE SPECIFICATION

LETTER	TORQUE (INCH-POUNDS)
A	4 - 5
B	4 - 6
C	5 - 6
D	5 - 7
E	6 - 7
F	7 - 8
G	10 - 14
H	15 - 17

ITEM#	COMPONENT#	DESCRIPTION	QTY	WHERE USED
65.	630-03955	WSHR, SHLDR, 3/16 SHNK, #6CL, FBR	8	XFORMER MTG
66.	620-08252	LUG, PCB/#4CL	1	MAIN PCB - J11 MTG
67.	540-00874	GROMMET, 9/16 OD, 7/16 ID	2	CHAS SUPPORT
68.	630-08260	INSUL, SEMI, SIL RUB, TO-126	1	TO-126 TO CHASSIS SUPPORT
69.	630-00952	INSUL, SEMI, BUSHING, TO-220	3	H/S TO MAIN BD
70.	630-07339	INSUL, SEMI, SIL RUB, TO-220 SHORT	3	H/S TO MAIN BD
71.	650-07551	RVT, SNAP-IN, .16DIA, NYL	4	PROT COVER
72.	675-08272	WIRE, 18G, GRN/YEL, 3", #6RING/SS	1	J13
73.	680-07897	CABLE, 079, SCKT/BICONN, 15C, 4.0"	1	P1 BACK LIGHT
74.	680-08892	CABLE, 079, SCKT/BICONN, 15C, 7.5"	2	P3, 4
75.	680-08356	CABLE, ASSY, 2C, 22G, 7", SS/HSG	1	LCD
76.	740-08373	LABEL, CAUTION, LO-PRO	1	LEFT SIDE (REAR)
77.	740-09195	LABEL, PRODUCT ID, LXP-15	1	REAR PANEL
78.	740-08556	LABEL, GROUND SYMBOL, 0.5" DIA	1	INSIDE REAR PANEL
79.	740-08471	LABEL, CSA CERTIFIED, COMMERCIAL	1	BOTTOM COVER (120V ONLY)
80.	740-08585	LABEL, CLA APPROVAL, LXP-15	1	LEFT SIDE
81.	740-08558	LABEL, TUV CERTIFIED, BAYERN	1	BOTTOM COVER (220/240V ONLY)
82.	740-08589	LABEL, RACK MOUNT ONLY	1	BOTTOM COVER (120V ONLY)
83.	740-10823	LABEL, CE 95	1	LEFT SIDE

REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	AN 6/11/91 DHS 6/11/91	CW 6/11/91 DHS 6/11/91
1	TOP & BOTTOM COVER SAME P/N -ITEM 1 PER ECO #910716-00-A	JV 9/13/91 AN 9/16/91	CW 9/18/91 DHS 9/18/91
2	CHANGE ITEM 77 TO PROD.ID LABEL PER ECO #911114-01	MAF 12/4/91 MK 12/9/91	CW 12/20/91 DHS12/20/91
3	ADDED RTV & NOTE 3 PER ECO #920225-00	JV 3/5/92 MK 3/6/92	CW 3/9/92 DHS 3/11/92
4	ADDED NEW KNOB (20) WASHERS (47), CHG QTY 2 TO 4 ITEM (48) PER ECO #920717-01	MF 7/27/92 AN 7/29/92	CW 8/3/92 DHS 8/3/92
5	CHANGED (14) & DELETED (47) PER ECO #930616-00	JV 6/24/93 MK 7/12/93	CW 7/9/93 DHS 7/26/93
6	ADDED P/N TO (6) AND BOM #'S TO (11) PER ECO #940524-00	JV 6/29/94 MK 6/30/94	CW 7/6/94 JW 7/7/94
7	ADDED LABEL ITEM (83) PER ECO #960529-00	AN 6/6/96 MK 6/7/96	CW 6/7/96 DHS 6/7/96

NOTES

1. PART NUMBER LISTING IS REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILLS OF MATERIAL.
2. APPLY LOCTITE TO SCREW (64) BEFORE INSTALLATION.
3. APPLY A DROP OF CLEAR RTV ITEM 2 TO SHAFT BEFORE INSTALLING KNOB ITEM 19. ONLY IF LOOSE FIT

NEXT ASSY	LXP-15X
USED ON	
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX +/-.010 .XXX +/-.005

MATERIAL

FINISH

DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 08890-74

APPROVALS		DATE
DRAWN	AN	5/15/91
CHECKED	DHS	6/11/91
Q.C.	CW	6/11/91
ISSUED	DHS	6/11/91

lexicon

TITLE: ASSY DWG, CHASSIS, LXP-15X

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-08890	7

SCALE N/A SHEET 4 OF 4

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