Service Manual

LXP-5

Effects Processing Module

lexicon

Precautions

The LXP-5 is a rugged device with extensive electronic protection. However, you should observe the same reasonable precautions that apply to any piece of audio equipment:

- Always use the correct line voltage and power pack.
- Don't install the LXP-5 in a closed, unventilated rack, or directly above heat-producing equipment such as power amplifiers.
- Never attach audio power amplifier outputs (speaker outputs) directly to any of the LXP-5's connectors.
- To prevent fire or shock hazard, do not expose the LXP-5 to rain or moisture.

FCC Notice

Class A Computing Device

This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the instruction manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J, Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area may cause interference, in which case the user at his/her own expense will be required to take whatever measures are needed to correct the interference.

The Federal Communications Department has prepared a booklet which you may find useful:

"How to Identify and Resolve Radio-TV Interference Problems"

This booklet is available from the US Government Printing Office, Washington, DC 20402, Stock No. 004-000-0345-4.

Lexicon Inc.
100 Beaver Street
Waltham MA 02154 USA
617-891-6790
Fax: 617-891-0340

Lexicon Part # 070-07333

Printed in the United States of America

Table of Contents

1

Controls and Connectors

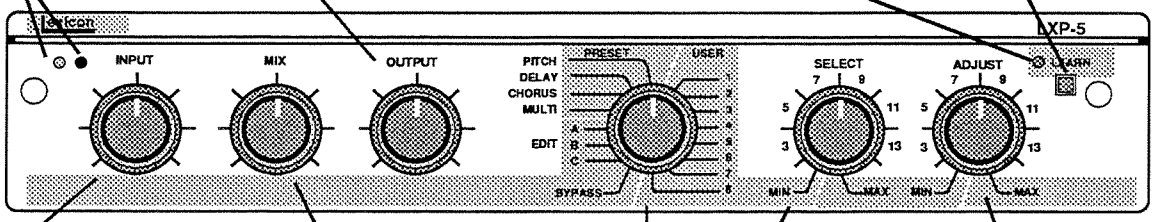
Front Panel

Level indicators
The left LED indicates signal present; the right flashes red when the signal is -3 dB from peak overload.

Output
Controls the signal level sent to the LXP-5's outputs.

Learn LED
Confirms that power is on, and blinks in red or green at different rates to indicate LXP-5 status.

Learn
This button is used with an external MIDI device to select a MIDI channel, store, edit and retrieve User registers and learn patches.



Input
Sets the audio input level.

Mix
Controls the ratio of dry (source) to wet (effect) signal present at the LXP-5 outputs. Turn the control all the way to the left for 100% dry/0% wet. Straight up is 50% dry/50% wet. All the way to the right is 0% dry/100% effect.

Function and Select
Used for selection of factory presets, User registers, Bypass and three edit modes.

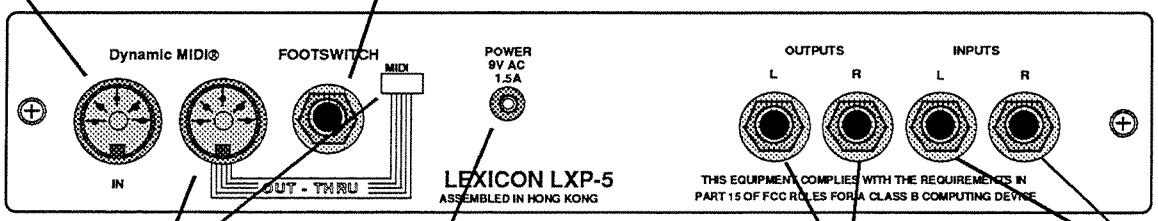
Adjust
Used to adjust a single parameter in a factory preset or User register, or to adjust the selected parameter in Edit Mode.

Rear Panel

MIDI IN
Receives MIDI information from other MIDI equipment, such as master keyboard controllers, MIDI foot controllers, sequencers, and synthesizers.

Footswitch
Connector for toggle (push-on/push-off) or momentary contact footswitch for:

Defeat Input
Defeat Output
Bypass
Memory Step



MIDI THRU (OUT)
With the recessed slide switch set for MIDI THRU, any MIDI data received is sent without change. The recessed slide switch can also be set for MIDI OUT.

Power
Accepts power from the supplied power pack.

Outputs (L and R)
Single-ended (unbalanced) stereo outputs provide +4dBu nominal output level.

Inputs (L and R)
Single-ended (unbalanced) inputs accept levels from -20 to +20 dBu. Input impedance is 50 kilohms in stereo, 25 kilohms in mono.

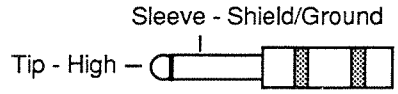
Power

Connect the LXP-5 power pack to an appropriate AC wall socket, and the cable end to the LXP-5 power connector. The LXP-5 must be used only with the supplied power pack. Voltage requirements are printed on the power pack. The LXP-5 has no power switch—it can be left on all the time. To keep the power plug from working loose from the rear of the unit during travel, you may wish to apply a small amount of silicone sealer to the plug after inserting it.

Audio Cabling

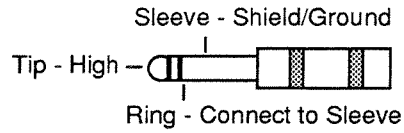
Under most conditions, cables which have a single conductor and a shield are adequate to connect the audio inputs and outputs of the LXP-5 to other equipment.

However, to insure the best performance, especially under high EMI (Electrical Magnetic Interference) conditions, cables with a twisted pair and separate shield are recommended. When using this type of cable, connect one of the twisted pairs to the tip of the phone jack, the other to the sleeve. (Be sure to connect the shield at one end only.) The shield should be connected at the input jack of the LXP-5 for input cables, and at the input of the piece of equipment connected to the LXP-5 output jack.



A tip/sleeve phone jack is recommended for the audio connections.

A tip/ring/sleeve jack may also be used. Just be sure to short the ring and sleeve.



Periodic Maintenance

Under normal conditions the LXP-5 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners.

Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the LXP-5 exterior.

Obtaining Factory Parts and Service

Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon Inc.
100 Beaver Street
Waltham MA 02154
Telephone: 617-891-6790
Fax: 617-891-0340

ATT: Customer Service

Returning units for service

Before returning a unit, consult with Lexicon to determine the extent of a problem.

If you choose to return an LXP-5 to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Description of the problem
- Desired return date
- Preferred method of return shipment

Please include a brief note describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, etc. with the unit.

2

Performance Verification

Performance Verification

Inspect the unit for any obvious signs of physical damage. Verify that all pots, the MIDI OUT/THRU selector switch, the LEARN momentary push button and the 16-position rotary switches operate smoothly and correctly. (Refer to the LXP-5 Owner's Manual for detailed explanations of functionality.)

Verify that all screws and rear panel jacks are secure.

Inspect the AC power transformer for any signs of physical damage. Make sure its output rating is 9VAC at 1.5 Amp and the appropriate 5mm/2.5mm barrel connector is attached.

Front Panel Diagnostics

Power on the LXP-5 while holding in the LEARN button on the front panel of the unit. When the LEARN button is released, the LXP-5 will enter Diagnostic Mode and will be awaiting the selection of a diagnostic test.

Diagnostic test programs are selected by turning the FUNCTION knob to one of its 16 positions (see Table 1 below). *Slave Tests* and *Alternative System Exits* also require a turn of the ADJUST knob to choose the specified diagnostic program. (See Tables 2 and 3.) Once a diagnostic test has been selected, the program is activated by pressing and releasing the LEARN button.

Generally, a test is performed once and the results are displayed upon completion of the test. In the case of tests marked by an asterisk (*) the tests are performed continuously; the results are displayed when the LEARN button is pressed and released a second time.

Unless noted otherwise in the test descriptions, successful completion of a diagnostic test is indicated by red flashing of the bicolor LEARN LED (located at the far right of the front panel). Failure is indicated by alternate red flashing of the LEARN LED and the OVLD LED (located at the far left of the front panel)

The following tables show the available diagnostic tests . For convenience, some related tests are grouped together under another test, such as *Run All.*

FUNCTION Knob Position	Diagnostic Test Program Names
BYPASS	LED test
EDIT C	Run All Master tests
EDIT B	Rotary Switch test
EDIT A	Clear RAM test (special procedure required)
MULTI	Non-volatile memory test
CHORUS	Footswitch test
DELAY	Audio Test Loop (runs continuously)
PITCH	Exit to system
USER 1	ROM test*
USER 2	Master RAM test*
USER 3	Master address test
USER 4	Master interrupt test*
USER 5	MIDI wraparound test
USER 6	Slave tests (requires selection via ADJUST)
USER 7	DRAM test
USER 8	Alternative system exits (requires selection via ADJUST)

Table 1
Diagnostic Test Programs accessed by FUNCTION knob

ADJUST Knob Position	Slave Diagnostic Program Names
MIN	Run All Slave tests
2	Shared RAM test
3	Slave Reset test
4	Slave Communications test
5	Slave Interrupt test
6	Slave RAM test
7	Master WCS test
8	Slave WCS test
9	Run All Slave tests
10	Run All Slave tests
11	Run All Slave tests
12	Run All Slave tests
13	Run All Slave tests
14	Run All Slave tests
15	Run All Slave tests
MAX	Run All Slave tests

Table 2
Slave Diagnostic Test Programs
(User 6)
accessed by ADJUST knob

ADJUST Knob Position	Alternative System Exit Program Names
MIN	All Registers Dump exit
2	N/A
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A
8	N/A
9	Exit to System without Diagnostics
10	N/A
11	N/A
12	N/A
13	N/A
14	N/A
15	N/A
MAX	N/A

N/A=none available.
An error indication will occur if these positions are used to select a program.

Table 3
Alternative System Exit
(User 8)
accessed by ADJUST knob

Using the Diagnostic Tests

The LXP-5 diagnostic tests are designed to facilitate the "process of elimination" technique of troubleshooting, but running a single diagnostic test will not always sufficiently isolate a hardware failure. Although related tests are indicated in each test description, it is recommended that the appropriate section of Chapter 3: Circuit Description be read to maximize the usefulness of the diagnostic tests. Chapter 3 also contains a reference glossary of signal and bus abbreviations.

For example: a unit is behaving in an inconsistent manner and Diagnostic tests are run to isolate possible hardware problems. *Master RAM test* is run and passes. *Master Address test* runs and fails. The diagnostic description of *Master Address test* states that the test checks all Master Processor addressable memory. In Chapter 3: Circuit Description: Memory, it is noted that the Master Processor can address all of the Slave RAM and the WCS located in the Lexichip.

Because the *Master RAM test* passed, you can assume that the Master RAM (U17) is functioning properly, and the problem must be in the Slave RAM or WCS. *Slave RAM, Shared RAM, Slave WCS* and *Master WCS* tests should be performed.

1. If *Shared RAM* and *Slave RAM tests* both fail, the Slave RAM is suspect.

2. If *Shared RAM test* and *Master WCS tests* fail, the Master/Slave interface circuitry is suspect. Running further diagnostics which exercise the Master Processor's access to the slave bus will verify this. (*Slave Communications test, Slave Reset* and *Slave Interrupt.*)

3. If both *Master* and *Slave WCS tests* fail, the Lexichip is probably faulty.

Test Programs

LED test
(Bypass)

This test should cause the OVLD and LEARN LEDs to blink red in unison until the next test selection. If it does not, check the OVLD or LEARN LED hardware, the Master Z80 or MIDI Serial circuitry, or the Lexichip.

If either the OVLD or the LEARN LED does not flash in this test, their associated pulsed signals can be traced while the LED test is being run. Keep in mind that these signals originate from different places. —the LEARN LED signal originates at U5 pins 7 and 10; the OVLD LED signal originates from pin 24 on the UART (U3).

Run All Master tests
(Edit C)
requires a MIDI cable

This test is designed to save time by performing the following tests in sequence:

ROM test
Master Address test
Master Interrupt test
MIDI Wraparound test
Run All Slave tests
DRAM test

This test requires a 5 pin DIN MIDI cable to be connected from the MIDI IN jack to the MIDI OUT/THRU jack located at the rear of the unit. The MIDI OUT/THRU switch should be set to its OUT position (toward the MIDI jacks).

The LEARN LED will flash a few times while this sequence of tests is running. After approximately 30 seconds, the tests should be completed and the results displayed. If all tests pass, the LEARN LED will flash red. If any of the tests fail, the LEARN and OVLD LEDs will alternately flash red. In the event of a failure indication, each test in the sequence should be run individually to determine which has failed.

Rotary Switch test
(Edit B)

This test compares the positions of the Function, Select and Adjust knobs. When the positions match, the LEARN LED will be green. The LEARN LED will be red when any one of these three knobs is in a different position than the other two. Turn each knob to every position to complete this test. If the test fails, knob hardware may be faulty.

If a switch position combination triggers a failure indication, keep the switches in the failing position. With an oscilloscope set to measure DC levels at 2V/cm, probe pin 1 on SW2, SW3,and SW5 and compare. When all switches are in the same position they should all have the same level. Repeat this procedure on pins 2 through 6, noting any dissimilarities. If one out of the three switches is at a different level, suspect the switch or the signal line's associated pullup resistor (RP1 or RP2).

Clear RAM test
(Edit A)
special procedure required

CAUTION: RUNNING THIS TEST WILL DELETE THE CONTENTS OF ALL USER REGISTERS.

This diagnostic program clears the contents of the master processor's static RAM, and runs a series of write/read tests on the RAM. Since this program will delete any stored user registers, a series of steps are required to activate this procedure. The steps are as follows:

1 Set FUNCTION to *EDIT A*; set SELECT and ADJUST to *MIN.* Press LEARN. (The LEARN LED will flash red once.)

2 Set SELECT and ADJUST to *2*; set FUNCTION to *BYPASS.* Press LEARN. (The LEARN LED will flash red once.)

3 Set FUNCTION to *EDIT C*, and press LEARN. (The LEARN LED will flash red once.)

4 Press LEARN once again to run the test.

If the LEARN and OVLD LEDs flash alternately at any time during the first three steps, the procedure is not being performed correctly and needs to be reselected by turning FUNCTION to *EDIT A* and pressing LEARN. When the procedure is followed correctly, and the test has been successfully completed, the LEARN LED will flash continuously. Alternate flashing of the LEARN and OVLD LEDs after step 4 indicates test failure. If failure occurs, the Slave and Master RAM ICs (U20, U17) are suspect. If the Slave RAM is failing, run the *Slave tests* to determine whether failure is caused by the support circuitry or the Slave RAM IC.

Non-volatile Memory test
(MULTI)

This test checks the non-volatile area of RAM used by both the master and slave processors by comparing a character string stored in ROM to a character string stored at a specific address in RAM. When the two differ, a failure will result, indicating RAM storage failure may have occurred. Pressing the LEARN button a second time will copy the character string from ROM to RAM and perform the test again. A second failure indicates a possible RAM hardware malfunction or defective Battery Backup circuitry. If the test passes on the second try, power down the unit for at least 10 seconds, then power up in Diagnostic Mode and rerun this test.

Note: This test will fail if the Clear Ram test has been performed since the last copy of the character string from ROM to RAM.

Test Programs, cont'd.

Footswitch test
(Chorus)

Performance of this test requires a toggling off/on or momentary contact footswitch with an appropriate 1/4" tip/sleeve plug connected to the FOOTSWITCH jack on the rear panel. If a footswitch is not available, a 1/4" shorting plug may be used.

The OVLD LED will light to indicate that the footwitch is OFF (or that nothing is plugged into the footswitch jack). When the footswitch is ON (or the shorting jack is inserted) the OVLD LED will turn off. If this test fails, check footswitch hardware for defects. Check also J3, R19, C16, CR8, CR7, RP2 and U19.

Audio Test Loop
(Delay)
runs continuously

This diagnostic program tests the converter circuitry audio specifications by producing a digitally processed output signal which is identical to the input signal. When this test is selected, and the the LEARN button is pressed, the LEARN LED will flash once to indicate that the program has been successfully loaded. The Audio Test Loop runs continuously until another diagnostic program is selected. If this test fails, refer to *Audio Signal Tracing* test later in this chapter. **Note that *Audio Test Loop* does not write or read from the DRAMs in processing the signal.**

Exit to System
(Pitch)

This allows the user to exit Diagnostic Test mode and returns the LXP-5 to its normal operating mode.

ROM test
(User 1)

This test calculates the ROM checksum and compares it to the stored value. Failure indicates that the code programmed in ROM is probably corrupt.

Master RAM test
(User 2)

This tests the area of volatile RAM which is used by the master processor, by requiring the master procesor to store and read various values. If this test fails, check Master RAM (U17), Master data and address busses, Master Z80 and PAL U11.

Master Address test
(User 3)

This diagnostic program performs an address test as well as a test of all areas of volatile RAM used by the master processor. The test requires the master procesor to store and read various values in this area of RAM. If this test fails, check Master Ram and associated hardware, as well as Slave RAM, Master/ Slave interface and Lexichip WCS. This test can be used in conjunction with the *Slave RAM test* and other Slave tests to isolate the specific hardware problem.

Master Interrupt test
(User 4)

This test checks the interrupt timing of the master processor by comparing it to coded timing loops. Failure indicates a problem in the Interrupt Timing circuitry (U13, U1), or the Lexichip WC/ signal line.

MIDI Wraparound test
(User 5)
requires a MIDI cable

This test checks the MIDI serial port transmit and receive functions. It requires a 5 pin DIN MIDI cable to be connected from the MIDI IN jack to the MIDI OUT/ THRU jack located at the rear panel. The MIDI OUT/THRU switch should be set to its OUT position (toward the MIDI jacks). This test takes approximately 5 seconds before results are displayed. Failure indicates a problem with MIDI hardware, or UART (U3).
The following steps will isolate the problem to the component level:

1. Power down the unit and power up in the normal operating mode.
2. Set FUNCTION to PITCH; set SELECT to MIN.
3. Connect a MIDI cable from MIDI IN to MIDI OUT and set the rear-panel MIDI OUT/THRU switch to OUT.
4. When ADJUST is turned, a MIDI message will be sent (and returned to the LXP-5) at each new knob position. The Master Processor should cause the LEARN LED to flicker to acknowledge the receipt of each MIDI signal. If it does not, there is probably a hardware error.
5. While ADJUST is turned, the serial MIDI signal can be traced through the MIDI circuitry with an oscilloscope. A pulsed waveform can be traced from the UART TxD pin (U3,pin 19) to U1 pin 10 , and then to MIDI output jack J2 pin 5. The signal can then be traced on the MIDI input J1 pin 5. Check the optocoupler output U2 pin 6 for the presence of serial MIDI data and verify that U3 receives this signal on its RxD pin (3).

Slave tests
(User 6)

When this position is selected by FUNCTION, the specific slave test is chosen by turning ADJUST to the appropriate position (see Table 2). Remember to press and release the LEARN button after turning ADJUST to select a test.

Run All Slave tests
(User 6: MIN, 9-MAX)

Choosing any of the designated *Run All Slave tests* runs the following tests sequentially:

Shared RAM test
Slave reset test
Slave communications test
Slave interrupt test
Slave RAM test
Master WCS test
Slave WCS test

This program will display success or failure after approximately 5 seconds. If any test in the sequence fails, a failure indication will be displayed. In this case,run each test individually to pinpoint the area of failure.

Shared RAM test
(User 6: 2)

This diagnostic program tests the area of volatile RAM shared by the master and slave processors. This test consists of storing and reading various values in RAM by the master processor. Failure indicates a problem with the Slave RAM or the Master/Slave interface. Run *Master Address* and *Slave RAM* tests to isolate the problem.

Test Programs, cont'd.

Slave Reset test
(User 6: 3)

This test checks the ability of the master processor to put the slave processor in reset mode. This test requires the master processor to send a program to the slave processor while holding it in reset. The program instructs the slave processor to load a message into a specific area of memory upon removal of reset. After removing reset, the master processor checks to see if the message is in memory. If this test fails, check the Master/Slave interface and the Master I/O decoding signal. Run all other Slave tests to further isolate the problem.

Slave Communications test
(User 6: 4)

This test checks the ability of the master and slave to communicate with each other using shared memory space. Failure indicates a problem with the Slave Decoder, or the Master/Slave interface. Run all other Slave tests to further isolate the problem.

Slave Interrupt test
(User 6: 5)

This test checks the ability of the master processor to send interrupts to the slave processor. A program is sent to the slave processor from the master which tells the slave to load a message into a specific area of memory upon receipt of an interrupt. The master processor then sends an interrupt, and checks for the message in memory. Failure indicates a problem in the Master Decoder (U11), or SINT signal hardware. Run all other Slave tests to further isolate the problem.

Slave RAM test
(User 6: 6)

This test checks the area of volatile RAM used by the Slave Processor. This test consists of storing and reading various values in RAM by the Slave Processor. This test can be used to help isolate Slave RAM problems by determining if a Slave RAM problem is caused by RAM, Master/Slave interface, or Slave Processor problems. **Note that only the upper 4K of RAM is exercised in this test.**

Master WCS test
(User 6: 7)

This test performs a RAM test on the WCS portion of the Lexichip by the master processor. Failure indicates possible Lexichip problems. This test should be run in conjunction with the *Slave WCS* and *Master Address* tests to eliminate Master/Slave interface problems, and to isolate Lexichip WCS errors.

Slave WCS test
(User 6: 8)

This test performs a RAM test on the WCS portion of the Lexichip by the slave processor. Failure of this test and the *Master WCS* test indicate problems with Lexichip WCS.

DRAM test
(User 7)

This test checks the DRAM in the Lexichip address area. The duration of this test is approximately 30 seconds, after which the results are displayed. Failure indicates a problem with Audio Memory (U22, 23, 29, 30). Faulty WCS will also cause this test to fail.

Test Programs, cont'd.

Alternative System Exits
(User 8)

When this position is selected by FUNCTION, an alternative system exit can be chosen by turning ADJUST (see Table 3). If an ADJUST position is selected for which there is no program, the LEARN and OVLD LEDs will flash alternately to indicate an error. At this time another diagnostic program may be selected.

All Registers Dump Exit
(User 8: MIN)

This system exit program instructs the LXP-5 to dump the contents of all user registers through the MIDI OUT jack. This program allows the user to copy these registers to another unit.

Exit to System without Diagnostics
(User 8: 9)

This program allows the user to exit to the system without going through the boot diagnostic tests. This procedure is useful when troubleshooting a unit that will not power up correctly due to a boot diagnostic failure.

Static Electricity Precautions

Many of the LXP-5's internal components are extremely sensitive to static electricity. The following practices minimize possible IC damage which can result from electrostatic discharge.

1. Don't handle ICs and boards any more than is necessary.
2. Discharge personal static by touching the LXP-5 mainframe before handling ICs or boards.
3. Handle each IC by its body.
4. Do not slide ICs or boards over a surface.
5. Avoid having plastic, vinyl or styrofoam in the work area.
6. Handle ICs only at a static-free workstation.
7. Use only grounded-tip soldering irons.
8. Use antistatic containers for handling and transport.

Clocks and Power Supply Measurements

Equipment Required

Variac
DMM
Frequency Counter (50MHz)
50 MHz Oscilloscope

Remove the two screws from the LXP-5 front panel and the center screw from the rear panel. Remove the 5 hex nuts from the 1/4" phone jacks on the rear panel. The pc board should now slide out towards the front of its case, allowing easy access to the circuitry.

1. Plug the LXP-5 power pack into the Variac and set output for 120 VAC.

2. Set the DMM to measure VAC. Apply power to the LXP-5 and measure the voltage across C25; it should measure between 9 and 11 VAC. If measurement is below 9VAC, the power pack may be faulty.

3. Set the DMM to measure VDC and check the regulated voltages for proper levels:

Location: Power/Ground	Allowable voltage range
U25 pin 3/U25 pin 2	11.40 to 12.60 VDC
U26 pin 3/U26 pin 1	-11.40 to -12.60 VDC
U24 pin 3/U24 pin 2	4.75 to 5.25 VDC
U1 pin 14/pin 7	4.25 to 4.50 VDC
U38 pin 16/pin 8	6.75 to 8.25 VDC
U38 pin 7/pin 8	-6.75 to -8.25 VDC

4. Power off the LXP-5 and measure DC voltage across battery BAT1 with DMM; it should be 3.00 VDC or greater. If voltage is low, replace the battery.

Brown Out / Power Down Test

1. Set oscilloscope for 2.5v/div (w/X10 probe) and a 1 mSec/div time base.

2. Connect scope probe to U1 pin 4.

3. Vary the Variac output level between 104VAC to 125VAC while monitoring U1 pin 4 on oscilloscope. This level should remain in a logical high condition (+5V).

4. Continue to monitor U1 pin 4 with oscilloscope and slowly reduce Variac output to 85 VAC. Pin 4 signal level should go to a logical low condition when the Variac output passes through the 100 - 85VAC range. If this test fails, make certain that transformer AC output (across C25) is between 9.0-11.0VAC with 120VAC input. If AC transformer is OK, suspect LXP-5 power down reset circuitry failure.

5. Return Variac to 120 VAC.

Clock Measurements

Using the frequency counter, measure the clock frequencies at the following points:

Signal Name	Location	Meas	Tolerance
ZCLK	U4 /pin 6	4MHz	±0.5%(3980000-4020000 Hz)
MIDICLK	U3 /pin 9	500kHz	±0.5% (497500 -502500 Hz)

Peformance Tests

Equipment Required

Low Distortion Oscillator with single-ended 600 ohm output, <.005% THD.

THD+N Distortion Analyzer/Level Meter with switchable 30Khz or audio bandpass filtering

Audio input cable single-ended, shielded audio cable with 1/4" plug on one end and proper connector on other end to connect to Low Distortion Oscillator output

Audio output cable single-ended, shielded audio cable w/ 1/4" plug on one end and the proper connectors on other ends to connect to THD+N Distortion Analyzer

Audio terminator plugs two 1/4" plugs, each with a 100K ohm resistor attached between tip and sleeve

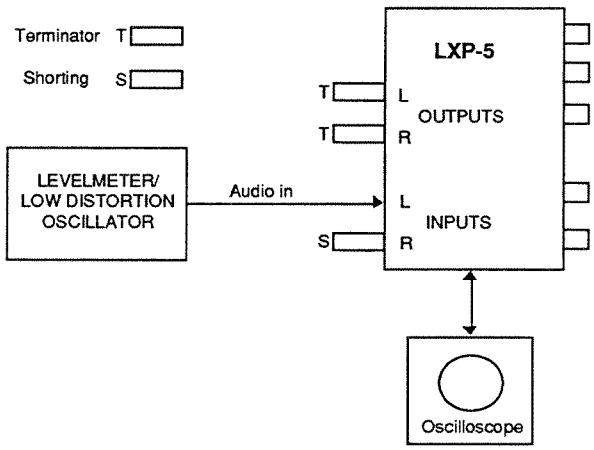
1/4" Shorting plug with tip and sleeve shorted inside shielded casing

Audio Signal Tracing

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Mix: *Fully counter clockwise to 100% Dry (unprocessed)*
Program: *Audio Test Loop (See Diagnostic Tests, Page 2-2)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to left or right channel input
2. 1/4" shorting plug to unused channel input
3. Audio terminator plugs to left and right channel outputs



Procedure

1. Apply a 1kHz signal at -25dBV (159mVp/p) to left channel input for *Left Channel* connection, or to right channel input for *Right Channel* connection.

2. With an oscilloscope set to DC coupling, 2v/division sensitivity at 5mS/division sweep rate, trace audio signal as follows. Observe any excessive DC offset levels on any input or output stage, as this could indicate a supply or amp problem which would affect the audio signal.

3. Set Mix control fully counter clockwise.

Analog Input Stage (U42)

	Signal Level	
	Left Channel	Right Channel
Left channel output (pin 7)	4.8Vp/p (4.6 - 5.0Vp/p)	No Signal
Right channel output (pin 1)	No Signal	4.8Vp/p (4.6 - 5.0Vp/p)

4. Turn Input Level Control fully counter clockwise

	Signal Level	
	Left Channel	Right Channel
Left channel input (pin 5)	No Signal	No Signal
Right channel input (pin 3)	No Signal	No Signal

5. Set Input Level fully clockwise

Pre-emphasis Stage (U40)

	Signal Level
Input (pin 5)	1.0Vp/p (0.95 - 1.05Vp/p)
Output (pin 7)	2.7Vp/p (2.6 - 2.8Vp/p)

Input Hold Stage (U39)

	Signal Level
Hold Input (pin 2)	Virtual Ground (No Signal)
Hold Output (pin 6)	2.7Vp/p staircase waveform (2.6 - 2.8Vp/p)

Comparator (U32)

	Signal Level
Input (pin 3)	2.7Vp/p staircase waveform (2.6 - 2.8Vp/p)

Output Hold Stage (U37)

	Signal Level
Right channel output (pin 1)	2.7Vp/p staircase waveform (2.6 - 2.8Vp/p)
Left channel output (pin 7)	2.7Vp/p staircase waveform (2.6 - 2.8Vp/p)

De-emphasis Stage (U34)

	Signal Level
Right channel input (pin 3)	1.15Vp/p (1.10 - 1.20Vp/p)
Left channel input (pin 5)	1.15Vp/p (1.10 - 1.20Vp/p)
Right channel output (pin 1)	1.15Vp/p (1.10 - 1.20Vp/p)
Left channel output (pin 7)	1.15Vp/p (1.10 - 1.20Vp/p)

Output Stage (U33)

	Signal Level	
	Left Channel	Right Channel
Right channel input (pin 3)	No Signal	4.8Vp/p (4.6 - 5.0Vp/p)
Left channel input (pin 5)	4.8Vp/p (4.6 - 5.0Vp/p)	No Signal
Right channel output (pin 1)	No Signal	4.8Vp/p (4.6 - 5.0Vp/p)
Left channel output (pin 7)	4.8Vp/p (4.6 - 5.0Vp/p)	No Signal

6. Set Mix Control fully clockwise

	Signal Level
Right channel input	2.5Vp/p (2.4 - 2.6Vp/p)
Left channel input	2.5Vp/p (2.4 - 2.6Vp/p)
Right channel output	2.5Vp/p (2.4 - 2.6Vp/p)
Left channel output	2.5Vp/p (2.4 - 2.6Vp/p)

7. Keep Mix Control fully clockwise (100% Wet)

Output Mute (either side of FB6 and 7)

	Signal Level
Right channel (FB7)	2.5Vp/p (2.4 - 2.6Vp/p)
Left channel (FB6)	2.5Vp/p (2.4 - 2.6Vp/p)

8. Set Mix Control fully counter clockwise (100% Dry)

	Signal Level	
	Left Channel	Right Channel
Right channel (FB7)	No Signal	4.8Vp/p (4.6 - 5.0Vp/p)
Left channel (FB6)	4.8Vp/p (4.6 - 5.0Vp/p)	No Signal

9. Set Output Level Control fully counter clockwise

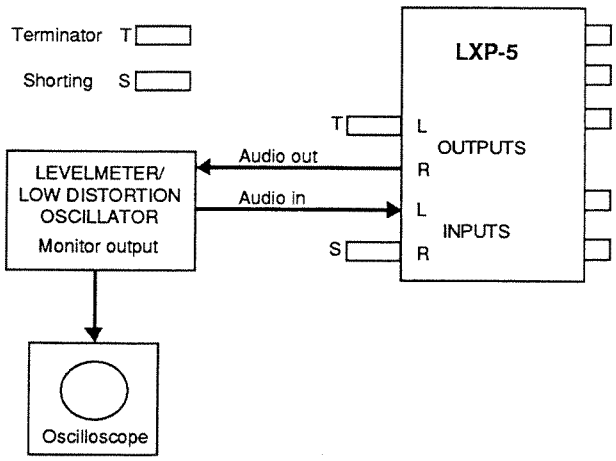
	Signal Level
Right channel (FB7)	No Signal
Left Channel (FB6)	No Signal

Inter-Channel Crosstalk Measurement

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Mix: *Fully counter clockwise to 100% Dry (unprocessed)*
Program: *Audio Test Loop (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to left channel input
2. 1/4" shorting plug to right channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -20dBV (283mVp/p) to left channel input.

2. Measure Right channel output level . Acceptable level < -60dBV (2.8mVp/p).

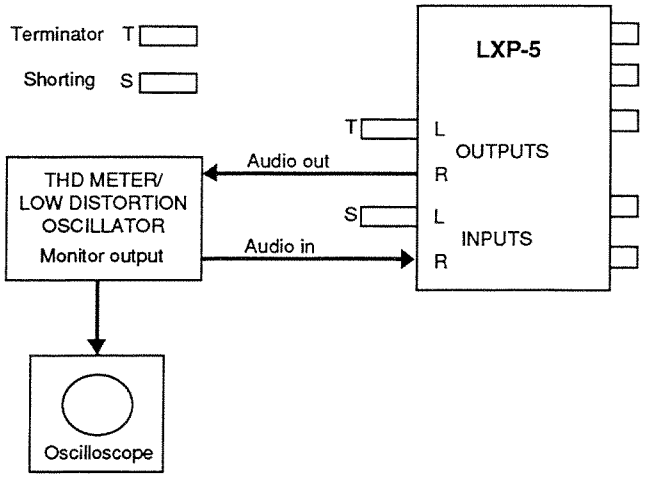
3. Swap all right and left channel audio connections and repeat steps 1 and 2 on left channel .

Dry (unprocessed) THD Measurement

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Mix: *Fully counter clockwise to 100% Dry (unprocessed)*
Program: *Audio Test Loop (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to THD+N Analyzer input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -20dBV (283mVp/p) to right channel input.

2. Measure THD+N at right channel output. Make sure 30kHz or audio bandpass filter on meter is ON. Acceptable reading will be <.01%.

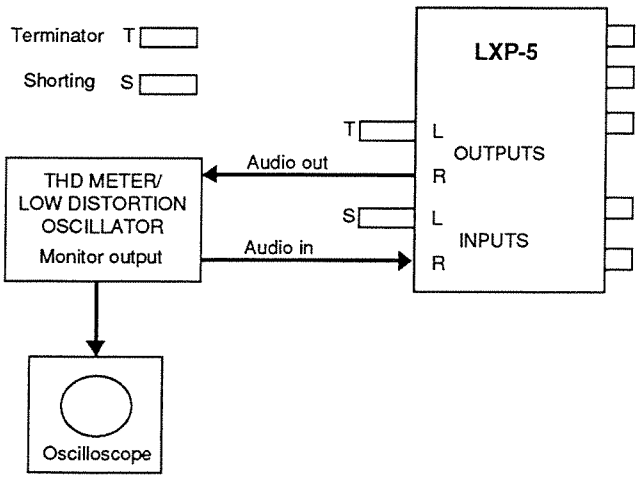
3. Swap all right and left channel audio connections and repeat steps 1 and 2 on left channel.

Dry (unprocessed) Frequency Response

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Mix: *Fully counter clockwise to 100% Dry (unprocessed)*
Program: *Audio Test Loop (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -20dBV (283mVp/p) to right channel input. Set Level Meter to measure right channel output as the 0 dB reference. Make sure all filters on meter are OFF.

2. Sweep from 20 Hz to 20kHz.

3. Right channel output should measure within ±0.1 dB (referenced to 1kHz output) over the range.

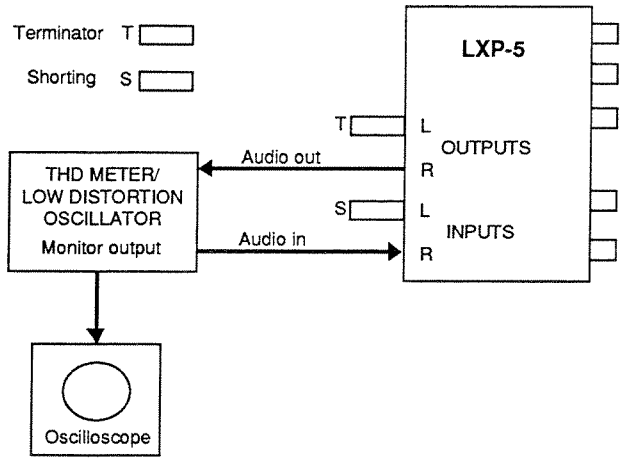
4. Swap right and left channel audio connections and repeat steps 1-3 on left channel.

Wet (processed) THD Measurement

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Mix: *Fully clockwise to 100% Wet (processed)*
Program: *Audio Test Loop (See Diagnostic Tests)*

Audio Connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to THD+N Analyzer input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -25dBV (159mVp/p) to right channel input.

2. Measure THD+N at right channel output. Make sure THD meter has 30 kHz or audio bandpass filter ON. Acceptable reading will be < .02%.

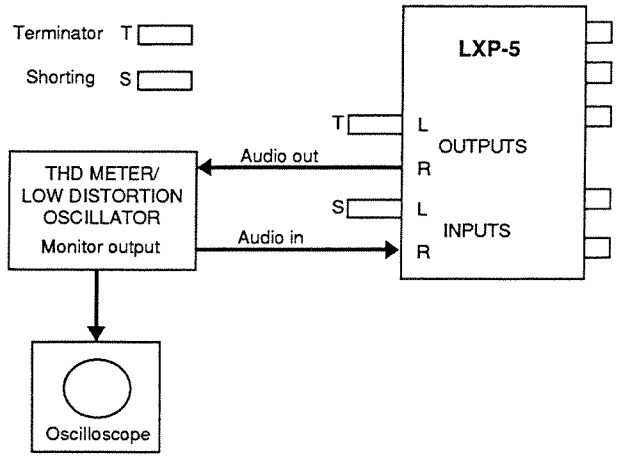
3. Swap all right and left channel audio connections and repeat steps 1 and 2 on left channel.

Wet (processed) Frequency Response Measurement

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Mix: *Fully clockwise to 100% Wet (processed)*
Program: *Audio Test Loop (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -25dBV (159mVp/p) to right channel input. Set Level Meter to measure the right channel output as the 0 dB reference. Make sure meter has 30 kHz or audio bandpass filter OFF.

2. Sweep from 20 Hz to 15kHz.

3. Right channel output should measure within +1.0 to -1.5 dB (referenced to1kHz output) over the range.

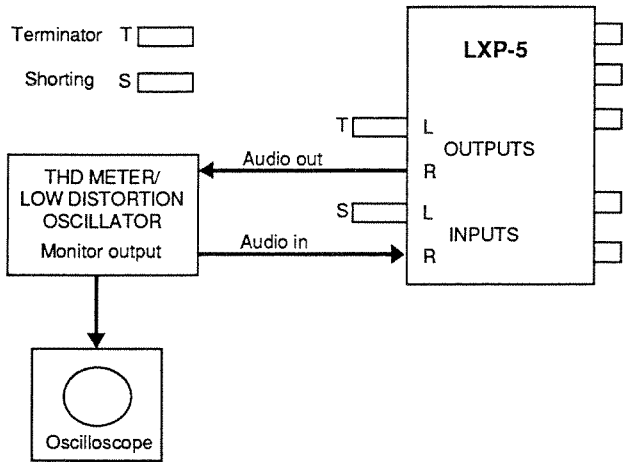
4. Swap right and left channel audio connections and repeat steps 1-3 on left channel.

Dynamic Range/ Signal to Noise

Input Level: *Fully clockwise to Maximum Level*
Output Level: *Fully clockwise to Maximum Level*
Mix: *Fully clockwise to 100% Wet (processed)*
Program: *Audio Test Loop (See Diagnostic Tests)*

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator (100k) plug to left channel output



Procedure

1. Apply a 1 kHz signal at -25dBV (159mVp/p) to right channel input. Set Level Meter to measure right channel output as the 0 dB reference. Make sure meter has 30 kHz or audio bandpass filter ON.

2. Unplug input to right channel. This will short out both right and left channel inputs.

3. Measure level on right channel output. Acceptable reading will be $\leq$ -75 dB (referenced to 1kHz output level; typical reading will be about -85dB.)

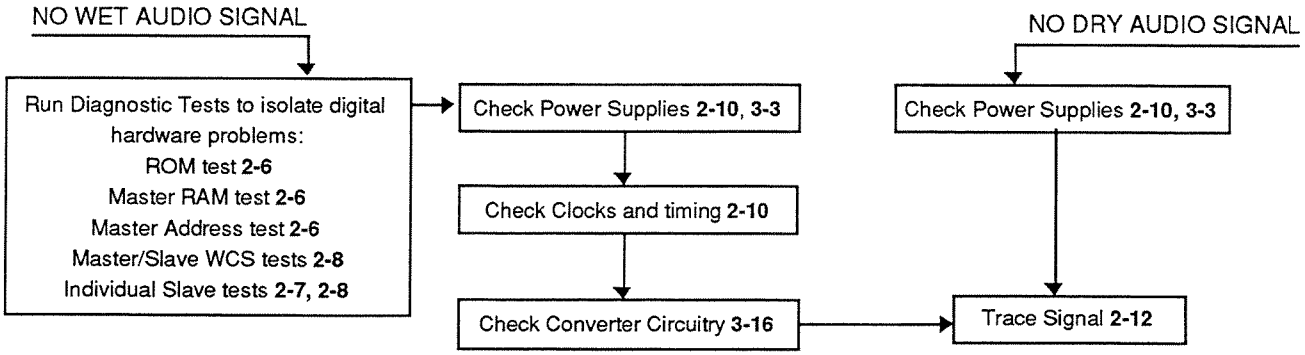
4. Swap right and left channel audio connections and repeat steps 1-3 on left channel.

Troubleshooting

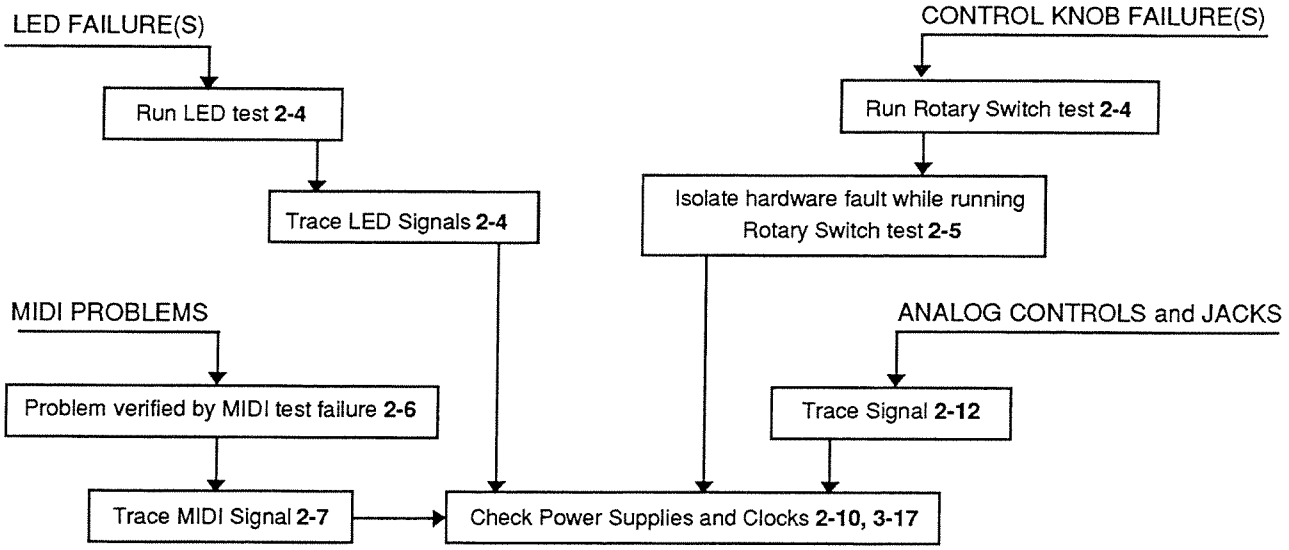
Since Diagnostic Tests can be performed without opening the unit they should generally be run first. This greatly reduces repair time, as a problem can be isolated to a specific circuit, even to a specific IC before opening the unit.

The following presents a diagrammatic version of the recommended troubleshooting procedure with page references.

AUDIO SIGNAL PROBLEMS



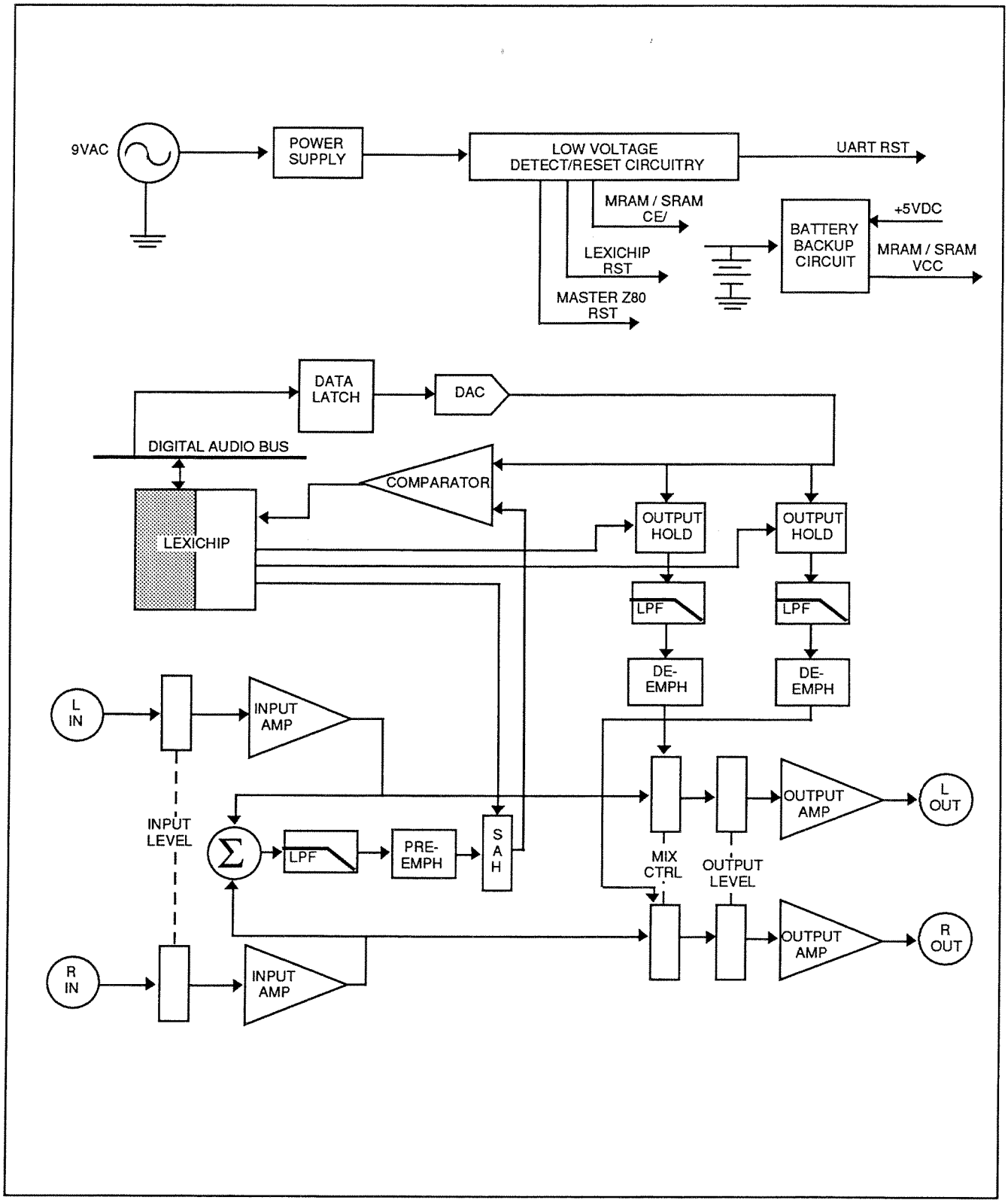
I/O PROBLEMS



3

Circuit Description

Analog Circuit Description



Power Supply

The LXP-5 power supply provides five regulated DC output voltages:

+5 VDC
+12 VDC
-12 VDC
-7.5 VDC
+7.5 VDC

AC power is provided by an external transformer rated at 9 VAC @ 1.5 A. The transformer output is terminated with a 5 mm/2.5 mm barrel-type connector, with its mating input jack located at the rear panel of the LXP-5. A .01 uF capacitor, C25, is connected across the AC input to help prevent noise spikes from entering the unit. In addition, C25 along with C38 and ferrite beads FB4 and FB5 stop circuit-generated RFI from radiating through the power line.

A pair of voltage doubler circuits develop the unregulated DC voltages for the ± 12 volt supplies. C27 and C28 store the peak level of AC input voltage during one half of the AC cycle. This stored charge adds with the next AC half cycle to produce approximately twice the peak AC input voltage across C29 and C40. Diodes CR9 and CR12 are polarized to produce the unregulated +12 volt supply (approximately +20 VDC) across C29. CR10 and CR13 are polarized to produce the unregulated - 12 volt supply (approximately - 20 VDC) across C40.

A single diode (CR11) is used as a half wave rectifier to produce the unregulated + 5 volt supply (approximately + 10 VDC) across C26 and C39. The +5VUNREG supply powers two of the front panel LEDs and is monitored by the LXP-5 Reset and Battery Backup circuits for power up and power fail conditions.

Voltage regulation is handled by three TO220 packaged ICs:

+12 VDC regulation - U25 (7812)
-12 VDC regulation - U26 (7912)
+5 VDC regulation - U24 (7805)

Current limiting and short circuit protection are incorporated into the internal circuitry of these ICs.

A ±7.5 VDC supply is created from the ±12 VDC supply by using 1K resistors in series with 1N755 zener diodes and 22uF capacitors. R59 and CR21 develop the +7.5 volt supply across C90, while R58 and CR19 develop the -7.5 volt supply across C84. ±7.5 VDC is required by the CD4053 analog switch (U38) only.

A +4.7 VDC supply is produced from the +5 VDC supply by placing a schottky diode (CR3) in series with R6 and C5. A charge is stored across C5 which provides the +4.7 volt supply for an extended time during power down due to the polarization of CR3. This supply is used by a 74HCT14 (U1) to insure proper operation of the LXP-5 Reset and Battery Backup circuitry when power failure occurs.

Reset Circuitry

The reset circuitry insures proper operation of the LXP-5 during power up and power fail conditions. This circuitry monitors the +5VUNREG supply and provides ZRST, ZRST/, MRST/ and RCE command signals.

The +5VUNREG supply is filtered by FB3 and C17 to prevent noise spikes on the AC line from tripping the reset function. R17 and R18 create a voltage divider which feeds C11 and the base of transistor Q3. C11 provides low frequency filtering for the base voltage. Q3 has a common emitter configuration with a pull-up resistor (R11) to +5 VDC on its collector. The collector voltage is applied to the input of a Schmitt inverter (U1, pin 3) whose output provides feedback to the base of Q3 through R12. During power up Q3 is off until the +5VUNREG supply exceeds the level necessary to bring the transistor into its active state. At this time, the collector voltage starts to drop, which causes the inverter output to go high and turns Q3 on. During a power fail or low power sequence, the +5VUNREG supply starts to drop, bringing Q3 out of saturation and into its active state. The collector voltage starts to increase which causes the inverter output to go low and turns the transistor off.

With the supplied 120 VAC power pack, an AC line voltage above 100 volts will turn Q3 on and insure the proper power up sequence for the LXP-5 circuitry. If the AC line voltage drops below 100 volts, Q3 turns off, enabling the required reset signals.

The collector of Q3 provides the ZRST command signal. ZRST is applied to the UART's Reset pin (U3, pin 21) and the Battery Backup circuitry, which require an active high signal for reset to occur.

The inverter output (U1, pin 4) provides the ZRST/ command signal. ZRST/ is applied to the Lexichip's Reset pin (U21 pin 74) which requires an active low signal for reset to occur. The ZRST/ command is also used to clear a latch (U5) and the MIDI timer (U13).

ZRST is also applied to another inverter input (U1,pin 13) through a delay circuit made up of CR5, C10 and R5. The output of this inverter provides the MRST/ command signal. MRST/ is used to reset the Master Z80 Processor (U4, pin 26) which requires an active low signal. The Master Z80 Processor is the last device enabled by the LXP-5 Reset circuitry, due to the delay circuit associated with MRST/. This insures that all other devices are in a known active state when the Master Z80 (U4) is enabled.

MRST/ is also used to provide RCE, which is the SRAM Chip Enable. RCE is controlled by Q1. The collector of Q1 is connected to the chip enable pins of the SRAMs (U17 & U20, pin26), and provides the RCE command signal. MRST/ is applied to the emitter of Q1 through R4. The base of the transistor is biased by CR2 and R3. Upon power up, MRST/ will go high after a delay, causing RCE to go high and enabling the SRAMs. The delay provided by MRST/ allows the SRAM VCC to stabilize before they are enabled. MRST/ and RCE immediately go low upon power fail, before +5 VDC goes out of regulation and the SRAM VCC drops to +3 volts.

The 74HCT14 hex inverter (U1) is an important component in the LXP-5 Reset circuitry. Therefore, its power supply is independent from the +5 VDC supply. CR3, R6 and C5 provide a separate 4.7VDC supply to insure proper operation of U1 for a brief time during a power fail condition.

Battery Backup

Battery Backup is required in the LXP-5 to maintain the non-volatile function of the processors' associated SRAMs. A 3 volt lithium battery (BAT1) maintains the minimum power requirement of the SRAM IC's, U17 and U20, while power is disconnected from the unit.

ZRST is used for controlling the Battery Backup circuitry, and drives the base of Q4 through R16. During power up, ZRST goes low which turns Q4 off. In turn, Q5 becomes active in its emitter follower configuration. The base of Q5 is biased by R20 and CR4, causing its emitter to ramp to +5 volts as C42 charges. This voltage is applied to the VCC pins of the SRAMs (U17 & U20, pin 28). CR16 is reverse biased, preventing the +5 volts from reaching BAT1.

Upon a power fail condition, ZRST goes high which turns Q4 on and Q5 off. C42 discharges until CR16 becomes forward biased, which provides +3 volts from the lithium battery for the SRAM VCC.

The Battery Backup circuitry, along with the RCE signal command, prevents stored data from being destroyed during power failure.

Analog Circuitry

Input Stage

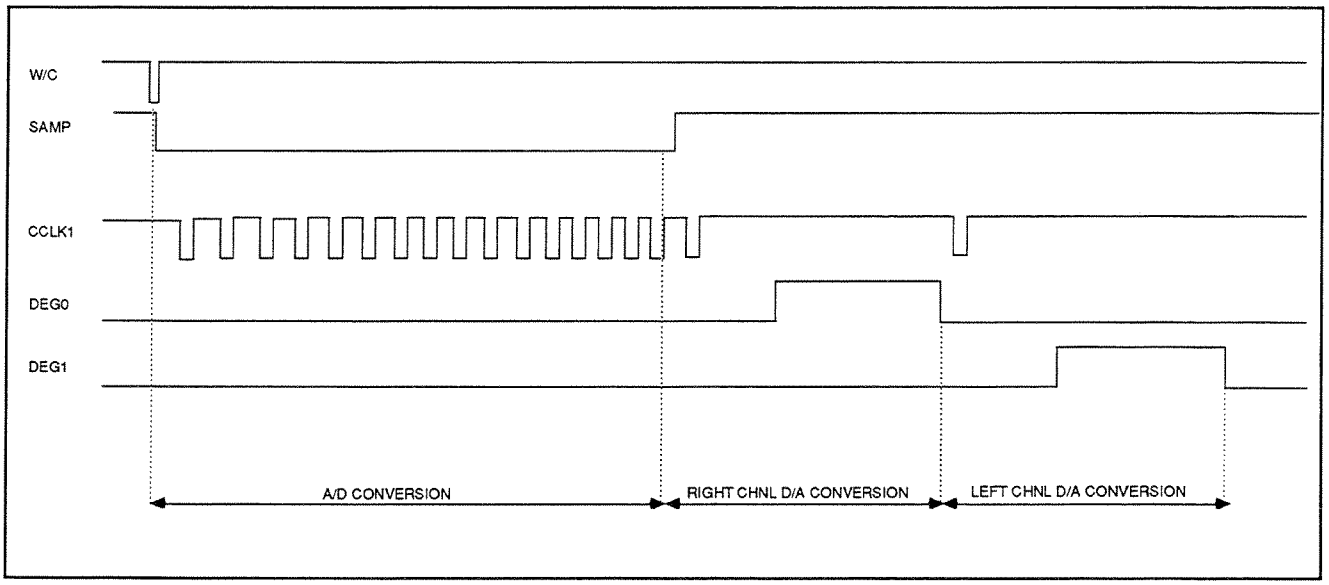
Separate unbalanced 1/4" phone jacks (J7 and J8) are provided for left and right input signals. A single input source will be routed to both left and right input stages by applying the signal to either input jack, thereby maintaining the proper operating level.

Ferrite beads (FB8 and FB9) and capacitors (C71 and C73) are found at the inputs to prevent unwanted high frequency interference from entering or leaving the LXP-5 through the input cables. DC isolation is incorporated by bipolar capacitors (C72 and C74) in line with the signal path. The left and right signals feed a dual potentiometer (R77) which controls the input signal level to the preamplifier stage. A dual op amp (U42) acts as the preamp by providing 30 dB of gain. This enables the LXP-5 to perform satisfactorily for nominal input levels as low as -27 dBV.

The left and right outputs of the preamp are applied to the stereo Mix control (R41) through AC coupling capacitors (C68 and C69). The preamp output signals also terminate at resistors R69 and R73 which sum the left and right signals. This summed signal is applied to a passive 7 pole 15 kHz low pass filter (U41) through an AC coupling capacitor (C99). A pre-emphasis function is performed by an op amp (U40), whose output drives the sample and hold circuit. The pre-emphasis is calibrated at the factory, and offers no provisions for user calibration.

The pre-emphasis amplifier also drives the signal detect circuitry. The signal passes through R63 after which a diode (CR20) removes the negative portion of the audio signal and develops an average DC level across capacitor C96. A sufficient DC voltage level will turn on transistor Q10, which illuminates a green LED (LED3) by conducting +5VUNREG through R80. This LED can be found on the front panel, and will illuminate at an input signal level of -34 dBV or greater, with the input level control set at maximum.

Converter Circuitry



A/D SAR Conversion Timing

SAH The sample and hold (SAH) circuitry consists of op amp U39, an SPDT analog switch U38 and capacitor C89. The SAH is controlled by the SAMP signal command from the Lexichip, which terminates at pin 11 of U38. When SAMP is high, pins 13 and 14 of switch U9 are shorted, which performs the sample function. At this time, an output level from pin 6 of U39 is used to charge C89. The hold function takes place when SAMP goes low, which shorts pins 12 and 14 of switch U38. The charge across C89 keeps the audio signal level constant during the analog to digital conversion. The output of the SAH passes through an AC coupling capacitor (C92) and a pulldown resistor (R62) to prevent DC offsets from affecting system performance.

DAC The analog to digital conversion involves use of a comparator (U32), the Lexichip (U21), and a 16 bit digital to analog converter (DAC, U31). The SAH output is applied to pin 3 of the comparator. The output of the DAC feeds pin 2 of the comparator. During the analog to digital conversion cycle, the internal successive approximation register (SAR) of the Lexichip is used in conjunction with the DAC to output different voltage levels. These voltages are compared with the audio signal level. The conversion is completed when the two voltage levels are equal. After the conversion, the L+R signal is processed digitally.

After the signal has undergone digital processing, separate left and right analog signals reappear after the digital to analog conversion. At this time, the Lexichip sends 16-bit data to the DAC, which converts it into analog voltage levels (see Data to Voltage chart below). These voltage levels are applied to the output hold circuitry.

Digital Input Code	Analog Output
0000h	+2.99991V
7FFFh	0.0000V
8000h	-91.6uV
FFFFh	-3.0000V

DAC Data to Voltage

Output Hold

Separate output hold circuits are provided for reconstructing the left and right audio signals. This circuitry includes a dual op amp (U37) and two analog switches (U38). DEG0 and DEG1 command signals from the Lexichip terminate respectively at pins 10 and 9 of U38, providing separate control of the right and left output hold switches. During the digital to analog conversion cycle, either the DEG0 or DEG1 signal goes high when the DAC is ready to output the respective right or left analog voltage. This permits capacitors C80 or C85 to charge to the corresponding voltage level for the audio waveform. When the DEG0 or DEG1 signal goes low, the related capacitor will remain at the current signal level until the next conversion cycle.

Output Circuitry

The left and right signals from the output hold circuitry are applied to separate 7 pole passive 15 kHz filters (U35 and U36). De-emphasis circuitry is incorporated into the signal path to compensate for the pre-emphasis function performed before the conversion process. A dual op amp (U34) with its associated circuitry provides the de-emphasis function.

Mix and Output Level Controls

The outputs of U34 are applied to one end of the stereo Mix control, R41. The other end of this potentiometer is connected to the outputs of the input preamplifier. By adjusting the wiper of the Mix control, the ratio of wet (processed) to dry (unprocessed) signal can be controlled.

The wipers of R41 are connected to one end of the Output level control, R32. R32 adjusts the signal level being applied to the output amplifier, U33. This dual op amp provides unity gain and buffers the left and right signals separately. An impedance of 600 ohms is developed by resistors R33, R34 for the right output, and R25, R26 for the left output. These resistors also provide current limiting protection. Bipolar AC coupling capacitors (C62 and C63) and pulldown resistors (R37 and R38) are installed to prevent DC offset voltages from appearing at the outputs of the LXP-5.

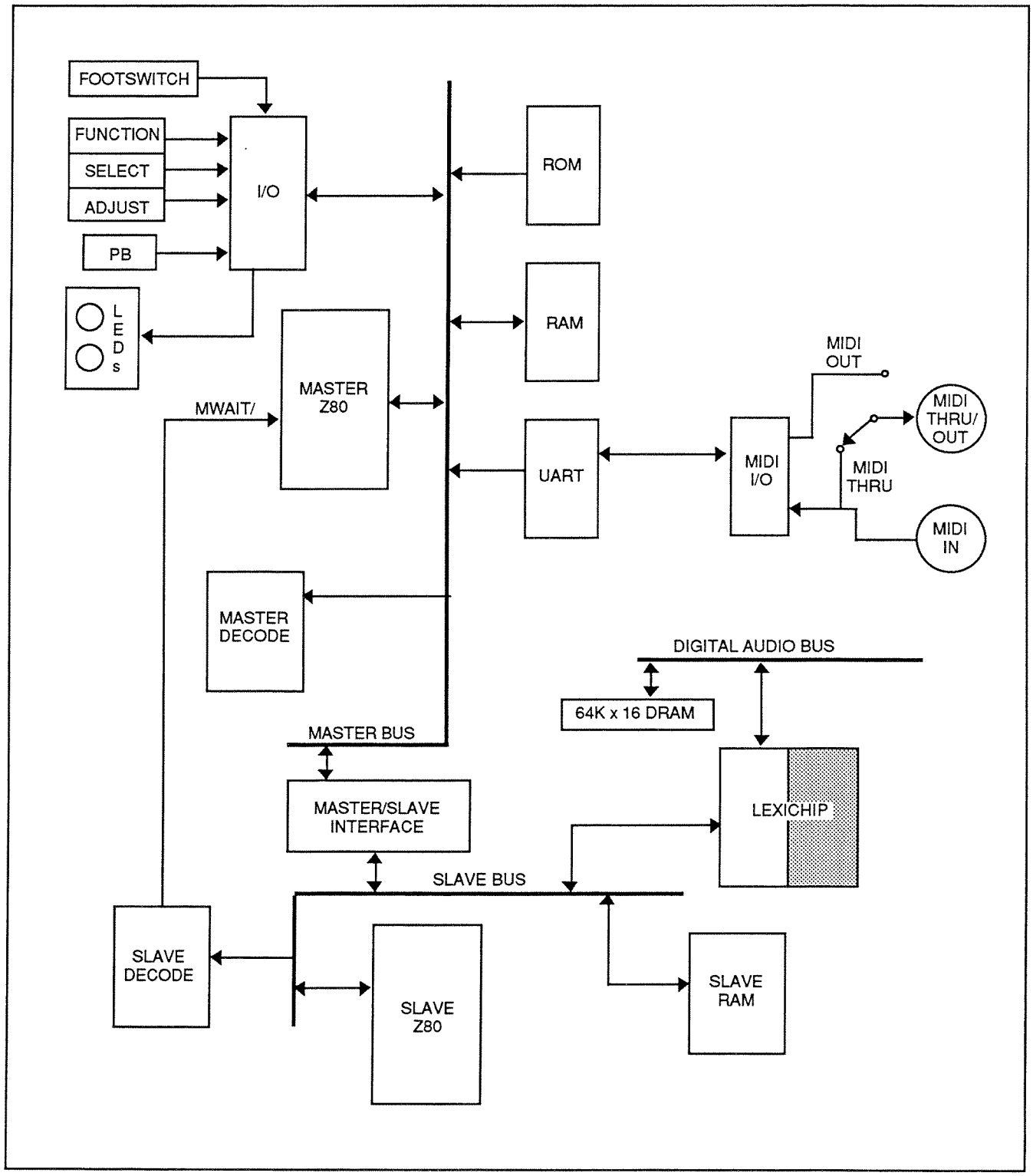
Output Buffer and Mute Circuitry

Two discrete JFETs, Q6 and Q8, provide a muting function by creating a low impedance path to ground along the output signal path. In this case, R26 and R34 serve as current limiting resistors by preventing the outputs of op amp U33 from shorting directly to ground. The mute function is under software control. The Mute/ command signal emanates from U5 pin 2, and is applied to the base of transistor Q7 through R30. When Mute/ is low, Q7 is on, which provides a positive DC voltage to the gates of Q6 and Q8. The JFETs turn on and enable mute. When Mute/ is high, Q7 turns off which allows a negative voltage to be applied to the JFETs. Q6 and Q8 turn off and disable mute. C50 insures a quiet transition between mute and unmute by ramping the gate voltages. Mute is enabled during power up or power down conditions, and some program change sequences.

The output jacks (J5 and J6) are located next to the input jacks on the rear panel. The 1/4" unbalanced phone jacks are configured in such a way that the left and right output signals are summed together if only one plug is connected. However, both output jacks should be utilized for the full stereo effect to be attained.

Static protection is provided for the output circuitry by diodes CR14, CR15, CR17 and CR18. Ferrite beads FB6 and FB7 and capacitors C48 and C51 prevent unwanted high frequency interference from entering or leaving the LXP-5 through the output cables.

Digital Circuitry



Overview

The LXP-5 utilizes two Z80 microprocessors and the Lexchip digital signal processor to perform multiple digital audio effects which are controlled via three front-panel selections, as well as a serial MIDI interface. Each processor has its own support circuitry, data and address buses. Communication between processors is performed via two interfaces.The Master/Slave Interface allows Master Z80 access to the Slave bus where read/write operations can be performed on Slave RAM and Lexichip. The Lexichip Writeable Control Store (WCS) contains program memory and registers. It can be accessed via its on-chip Z80 interface which connects directly to the Slave Bus.

During normal operation, sampled audio is converted into digital data by the converter circuitry. Digital effects processing is performed by the Lexichip under the control of both Master and Slave Z80 processors. The Master Z80, which handles all operator I/O and housekeeping functions, is able to pass on DSP control information to the other two processors.The Slave Z80 is dedicated to the task of controlling the Lexichip and is, therefore, used to perform any DSP control functions which require precise timing, such as pitch shifting.

Z80 Microprocessor Circuitry

The LXP-5 utilizes two 4 MHz Z80 microprocessors (U4 and 14) in a master/slave configuration. Tasks are shared between these two processors as described below :

Master Processor Functions

The Master Z80 (U4) handles basic housekeeping and user interface I/O operations. It has the ability to write program code and data directly into the Slave Z80 Program RAM and Lexichip Writeable Control Store (WCS) by directly accessing the Slave Z80 bus via the Master / Slave Interface. Its specific tasks are:

- Processing data and instructions to and from the UART
- Processing data and instructions to and from the Lexichip
- Handling user-data input and LED operations
- Maintenence of non-volatile, user-controlled registers.
- Loading and manipulation of Slave processor program code and data
- Controlling Slave processor reset and interrupt functions
- Controlling audio muting hardware

Slave Processor Functions

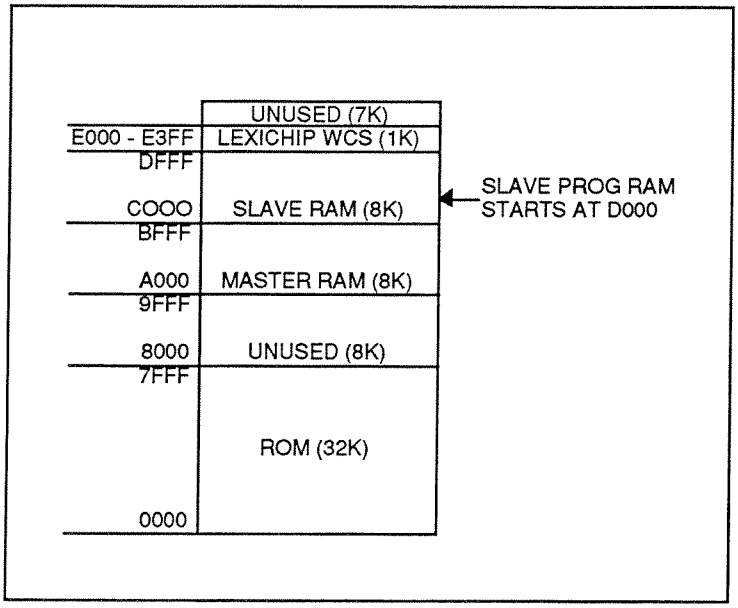
The Slave Z80 (U14) is strictly dedicated to controlling Lexichip operations. This task is performed by accessing the Lexichip Writeable Control Store, the on-chip memory and register storage which is connected to the Slave Z80 bus via a Read/Write port .

Memory

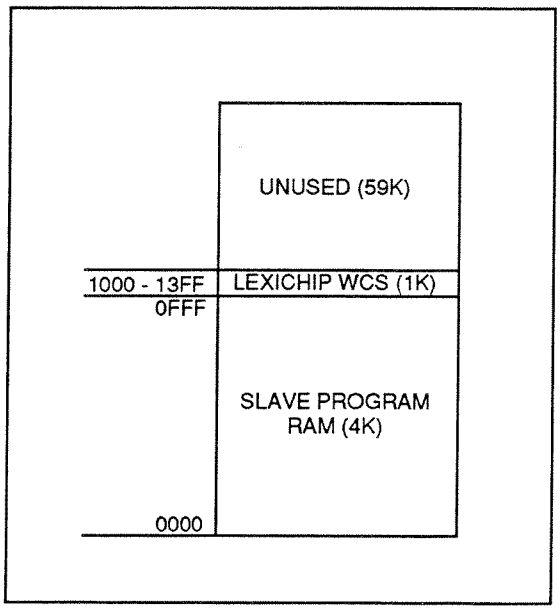
32K bytes of ROM space is contained in a single 27C256 PROM (U10). This ROM is mapped into the Master processor memory space. It contains Slave Z80 and Lexichip program routines which are loaded by the Master Z80 via the Master/ slave interface. Diagnostics, I/O, and housekeeping subroutines executed by the Master Processor are also contained in this ROM space.

Two CMOS 4364C SRAM ICs (U17, U20) provide a total of 16K of RAM space for both Z80 processors. This RAM is kept non-volatile by the Battery Backup circuitry explained in the power supply section of this chapter. All 16K bytes of RAM are mapped into the Master Z80 memory space. Because U20 is connected to the Slave bus, the Master Z80 must access this upper 8K of RAM via the Master/Slave interface explained below. Only the upper 4K of RAM contained in U20 is mapped into the Slave Z80's memory space to function as both program and data memory for that processor. Slave Z80 code is loaded into memory by the Master Z80. The lower 4K of space contained in U20 serves as user-register storage. This is managed by the Master processor and cannot be accessed by the Slave Z80.

The Lexichip (U21) contains its own on-chip program RAM and I/O registers which are addressable by both Z80 processors via the Slave Bus. This 1K byte of memory is mapped into the 64K of addressable memory space of both Master and Slave processors.



Master Processor Memory Map

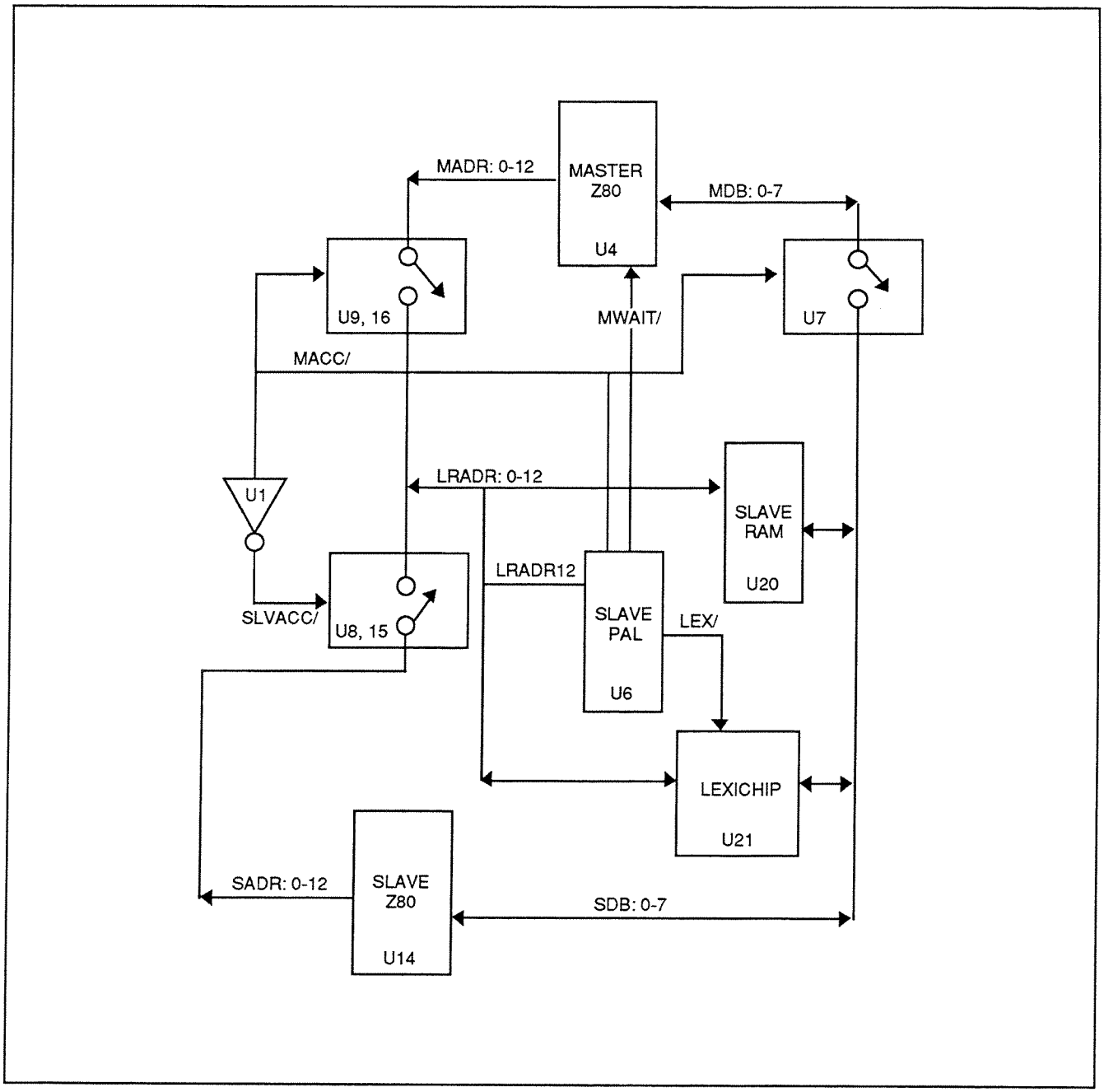


Slave Processor Memory Map

Master/Slave Interface

A memory refresh period is produced by a Z80 processor for two clock cycles during every instruction fetch. Since the static RAM used by the Master and Slave Z80s does not require refreshing, the master processor utilizes the Slave Z80's available refresh period to gain access to the Slave processor bus in a manner that is completely transparent to Slave operations. Syncronization of timing for Master Z80 access to the Slave Bus is performed by the Slave Decoding PAL (U6).

The following diagram illustrates the actual hardware interface.



Master /Slave Interface Diagram

Master Decoding

U11, a PAL16L8 decodes address bus signals of the Master Z80 into memory and I/O device signaling. Two AND gates (U18) ,an inverter (U1) and a 74HCT174 D latch (U5) are also utilized in this function. The chart below shows the PAL decoding scheme for Memory and I/O operations. A description of each output signal provided by the Master Z80 decoding circuitry is also provided at the end of this section.

Master Decoding Chart

MASTER PAL DECODING CHART: (MMREQ/ = L)						MEMORY
MADR:	15	14	13	HEX ADDRESS	Active Sel Line	H/L
	0 0	0 1	0 1	000h through 7FFFh	ROM/	L
	1	0	1	A000h through BFFFh	RAM/	L
	1	1	0	C000h through DFFFh	MSREQ/ SLAVE PAL DECODE: SRAM/	L
	1	1	1	E000h through E3FFh	MSREQ/ SLAVE PAL DECODE: LEX/	L

MASTER PAL DECODING CHART: (MIORQ/ = L)							
MADR:	7	6	5	HEX ADDRESS	Active Sel Line	R/W	H/L
	0	0	0	00h	IO1/	R	L
	0	0	1	20h	IO2/	R	L
	0	1	0	40h	IO3	R	H
	0 .	1	1	60h MDB 7 6 5 4 3 2 1 0	IO4	W	H
				X X X X X X X 0	MSYNC/	X	L
				X X X X X X 0 X	MUTE/	X	L
				X X X X X 0 X X	SRST/	X	L
				0 1	MIDI LED=GREEN		
				1 0	MIDI LED=RED		
				0 0 or 1 1	MIDI LED=OFF		
	1	0	0	80h	UART/	R/W	L

Slave Decoding

The Slave PAL (U6) handles the Mapping of the Slave RAM and Lexichip WCS into both Z80 processors' memory. Address and control signals on the Slave Bus are decoded as shown below.

Master Z80 access to the Slave Bus is also controlled by the Slave PAL. Access is synchronized to occur during the memory refresh period of the Slave Z80 by forcing wait states on the Master Z80. This is also illustrated in the timing diagram in the following section.

Slave Decoding Chart

KEY	
X	DON'T CARE
↑	RISING EDGE
↑↑	TWO RISING EDGES (ONE FULL CLOCK PERIOD)
0	LOGICAL LOW
1	LOGICAL HIGH

SLAVE PAL DECODING CHART

SLAVE BUS ACCESS AND MASTER Z80 WAIT SIGNALING

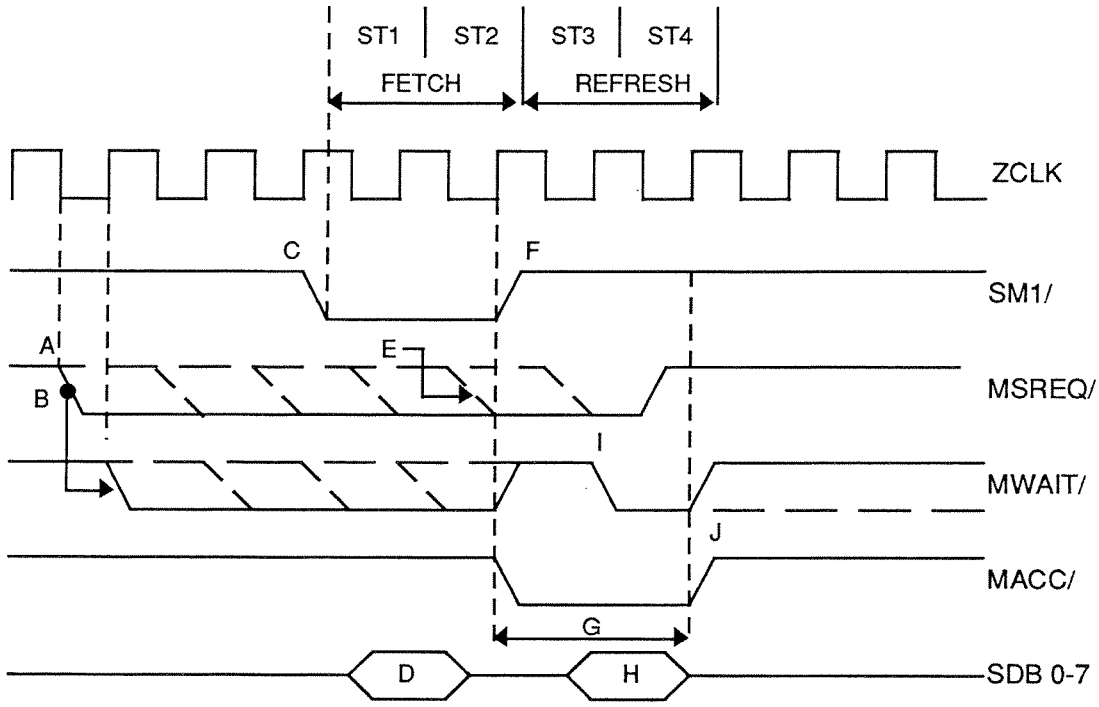
INPUT SIGNALS								OUTPUT SIGNAL	
ZCLK	SRST/	MSYNC/	WCE/	MSREQ/	SM1/	MWAIT/	SWAIT/	X	
								MWAIT/	MACC/
↑	1	X	X	0	1	X	1	a	1
↑	1	X	X	0	X	X	0	b	
↑	1	0	1	X	X	X	1	c	
↑↑	1	X	X	0	0	0	1	clears condition a or b	
or									
↑	1	0	0	X	X	0	1	clears condition c	
↑	1	X	X	0	0	↑		X	0
or									
↑	0	X	X	0	X	X			

SLAVE BUS DECODING

ZCLK	LRMREQ/	MSREQ/	LRADR12	SM1/	SIORQ/	SRAM/	LEX/	INTACK/	UCLK
X	0	X	0	X	X	0	1		
X	X	0	0	X	X				
X	0	X	1	X	X	1	0		
X	X	0	1	X	X			X	X
X	1	1	X	X	X	1	1	X	X
X	X	X	X	0	0	X	X	0	X
↑	X	X	X	X	X	X	X	X	$\overline{UCLK}$

Slave Instruction Fetch Cycle

There are three different periods where the Master Z80's request to gain access to the Slave Bus is honored. The first is when Slave Z80 reset (SRST) has been asserted. In this case the Master Z80 gains immediate access with no wait states. The other two periods occur while the Slave Z80 is performing either an instruction fetch or an interrupt acknowledge. Timing for these two conditions are illustrated and explained below.



A The Master Z80 requests Slave Access by asserting MSREQ/

B MWAIT/ is asserted to keep the Master Z80 in a wait state until the Refresh window occurs.

C SM1/ indicates Slave Z80 Instruction Fetch period.

D Instruction code is read from the 8-bit data bus.

E If MSREQ/ is asserted during the second T state of Instruction Fetch period (SM1/), the Master Z80 is in sync with the Slave Z80 Refresh period and no wait states will occur.

F The rising edge of SM1/ indicates the beginning of Slave Z80 Refresh period, which is the Slave Bus access window.

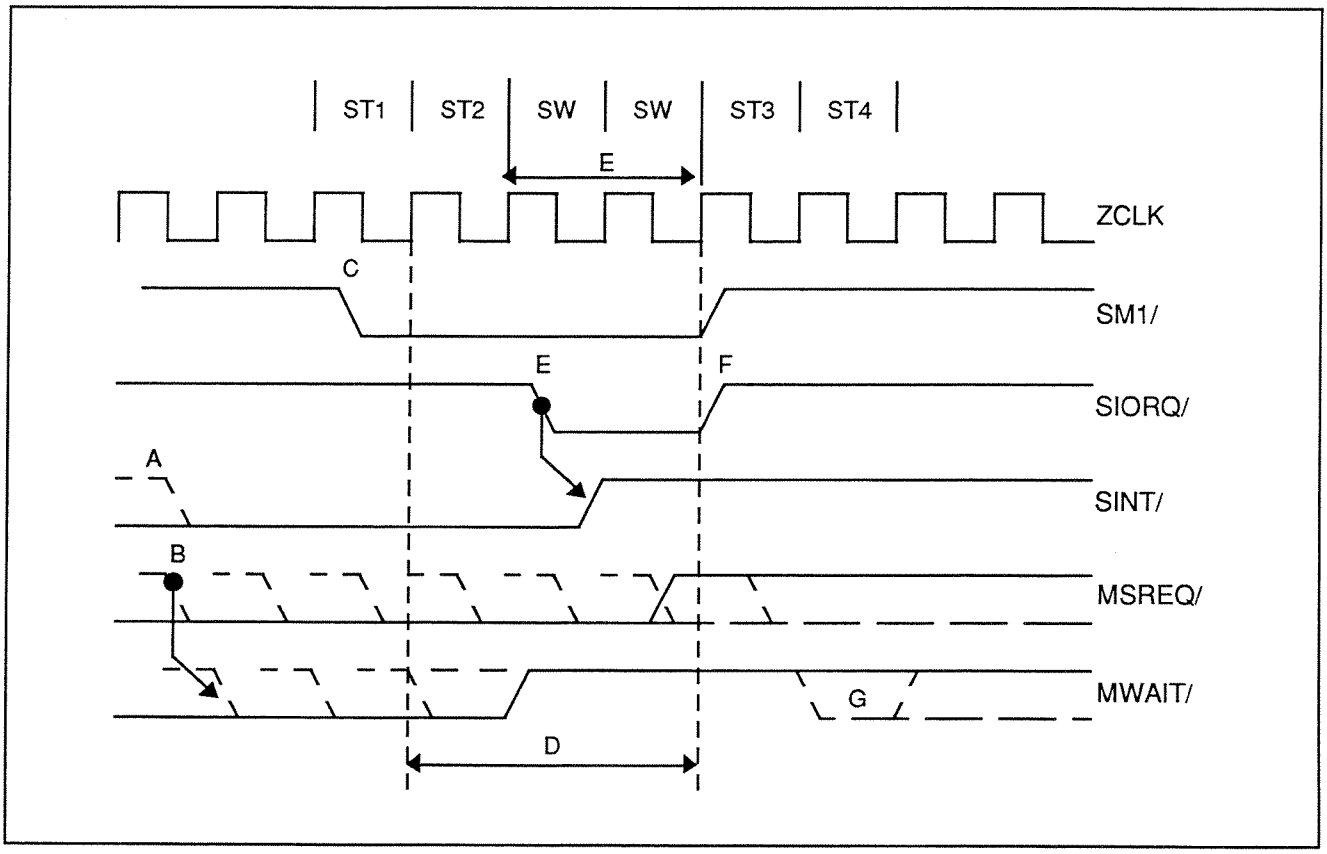
G The Refresh access window occurs for the last two T states during a Slave Z80 Instruction Fetch cycle. If MSREQ/ has been previously asserted, MACC/ will go low to enable Slave Bus buffers for the Master Z80, allowing it access to Slave RAM or Lexichip WCS.

H During this Refresh period, the Slave Z80 data lines are placed in a high impedance state. The Master Z80 is then allowed access to the 8-bit data bus for a read or write operation.

I MWAIT/ goes low for the 4th T state of the Slave Instruction Fetch. If the Master Z80 has already gained access to the Slave Bus at this point this MWAIT/ will be ignored. If MSREQ/ is activated just after D, this wait signal will be acknowledged, and the Master processor will insert waits until the next Refresh period.

J At the end of Slave Refresh Access, MACC/ is returned to a logical high, which removes Master Z80 from the Slave Bus .

Interrupt Request/Acknowledge Cycle



A Master Z80 requests an Interrupt from the Slave processor

B Master Z80 requests Slave Bus Access. Since this request is not syncronous with a Refresh window, MWAIT/ is activated. Master Z80 inserts wait states until the next available window.

C SM1 goes low as the beginning of an interrupt acknowledge cycle is occurring. In the interrupt mode used by the Slave Z80, its data bus will be in a high impedance state during this entire cycle.

D SM1/ is low for 4 T states during the Interrupt Acknowledge cycle. Due to this extended SM1, the Master Z80 can request Slave Bus Access (by activating MSREQ/) and gain access without wait states during the last 3 T-states of SM1/.

E SIORQ/ goes low. This, in conjunction with SM1/ staying low for an additional two wait periods, creates the Interrupt Acknowledge signal.

F SM1/ and SIORQ/ both go high, indicating Refresh period has begun.

G If MSREQ/ is low during ST4, MWAIT will become active. This wait will be ignored by the Master Z80 if MSREQ/ went low on the last SW clock before Refresh, as the Master has already gained access. If MSREQ/ goes low during ST3, wait states will be inserted by the Master Z80 until the next Refresh window occurs.

Digital Audio Processor Circuitry

LEXICHIP: Z80 Interface

The Lexichip (U21) performs all the digital effects processing calculations for the LXP-5. It receives instructions from its internal program RAM, referred to as the Writeable Control Store (WCS). Address, data, and control lines for the WCS are shared with the Slave Z80 bus. This allows both Slave and Master Z80 processors to load audio effects programs into the Lexichip, monitor status of audio data, and synchronously change program parameter values in audio programs. Both Master and Slave Z80 processors treat the 1K bytes of WCS as mapped memory space.

Clocks

An internal crystal oscillator driver circuit drives a 16MHz crystal mounted across pins 75 and 76 on the Lexichip. Internal Lexichip circuitry divides this clock frequency down to provide the 4MHz ZCLK which is used by the Z80 processors.

The PCLK1 (pin 73) output is programmed to divide down the 16MHz clock to the 500kHz MIDICLK signal. This signal is utilized by the UART IC (U3) to set up the serial communications baud rate.

WC/ (pin 59) is used as a clock reference by the LXP-5. It operates at a 31.25 kHz sample rate and is utilized by the UART interrupt timing circuitry, as well as by the Slave decoding circuitry, to sync the Master processor to DSP operations.

Audio Memory

Four 64K x 4-bit dynamic RAM ICs (U22,U23,U29,U30) provide the 64K x 16-bit RAM space used by the Lexichip for audio data storage. DRAM read, write, and refresh functions are performed by a dedicated set of address and control lines and a 16-bit data bus provided by the Lexichip.

LEXICHIP: DAC/ADC Control Logic and Data Port

Internal control logic circuitry enables the Lexichip to command complete control over external DAC functionality with minimal external circuitry.

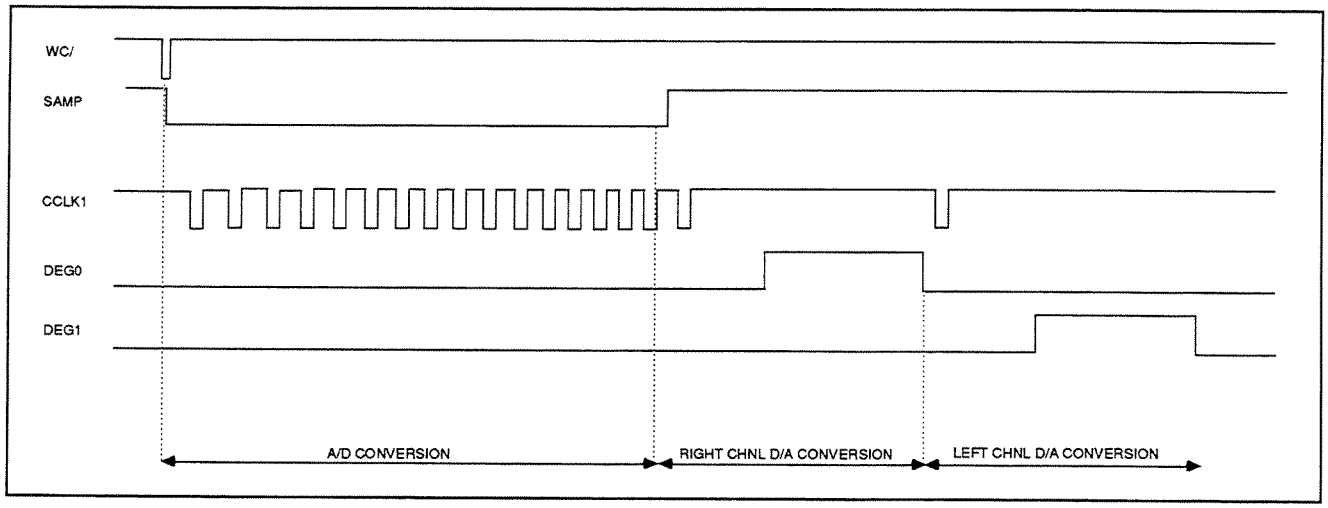
Two 8 bit latches (U27,U28) are used to latch 16 bit data out to the DAC via the DRAM data bus. Lexichip output CCLK1 clocks DAC data into these DAC conversion latches.

An internal Successive Approximation Register (SAR) allows the DAC, in conjunction with an external comparator, to perform analog to digital conversions. A data value is latched into the conversion latch. DAC output is compared to analog input by the comparator. The comparator's resulting output (DATA) is applied to Lexichip input SI1, and the SAR logic circuitry determines either the next DAC output value or an end of conversion. Converted data is then processed by the Lexichip with instructions from its RAM resident digital effects program.

DAC logic signals are provided by the Lexichip to control the Sample and Hold (SAH) and deglitch functions and conversion data latching. A Word Clock signal (WC/) is used as a clock reference and indicates the beginning of a conversion cycle.

On the falling edge of WC/, SAMP goes low in order to hold an input sample for an A/D conversion. The internal SAR then applies a DAC data output to DAB0-15. This data is latched into conversion latches on the positive edge of the CCLK1 signal. The DATA signal from comparator is then compared by Lexichip to determine the next SAR output value. Sixteen SAR output samples are required to perform an analog conversion. Since the later samples produce smaller voltage changes on DAC output, less time is required for DAC to settle, therefore, the time duration between CCLK1 pulses towards the end of the A/D conversion is reduced.

The 17th CCLK1 pulse after WC/ latches left channel data out to the DAC. After sufficient DAC settling time, the left channel deglitch switch is disabled by the high state of DEG0, applying a DAC sample to the left channel output circuitry. The last CCLK1 pulse in the WC/ cycle latches right channel data to the DAC. DEG1 goes high which applies the DAC sample to the right channel output circuitry.



Converter Timing

UART, I/O

UART

Serial communications are handled by U3, an 82C51A UART IC. U3 is mapped into the Master Z80's I/O space at locations 80h (data register) and 8Ih (instruction register). The Slave PAL decoder provides it with a 2MHz clock (UCLK). The MIDICLK input from the Lexichip is a 500kHz baud rate clock. It is frequency divided by U3 internally to produce the 31.25kHz baud rate used in MIDI serial communications.

The transmit and receive data connections (TXD,RXD) are applied to the MIDI standard I/O hardware. The hand shake signal (DTR) is used to drive the OVLD LED (LED2). The Master Z80 will set this bit high to light this LED, indicating that the Audio signal is about to exceed, or has exceeded, the digital clipping level.

Master Interrupt The 31.25kHz WC/ signal is applied to the digital counter U13. Every nine clock pulses, RCO (pin 15) will go high in order to force an interupt routine on the Master Z80 processor. The processor will then access the UART to examine the RXD port for any MIDI input data received.

MIDI Hardware The MIDI hardware utilized by the LXP-5 complies with MIDI specs. It incorporates 5 pin, female DIN connectors for input and output connections (J1 and J2). MIDI IN is optocoupled into UART R x D line for ground isolation purposes. A switch (SW4) located on the rear panel allows the user to select either the MIDI THRU or MIDI OUT function for J2. With SW4 in MIDI THRU position , received data is sent back out through an inverter to a current loop driver, Q2. In MIDI OUT position, TXD output from the UART will be connected to Q2, allowing MIDI output functions to be performed. Ferrite beads FB1, FB2 and C8, C9 are used to reduce RFI from being radiated from the MIDI OUT/ THRU port.

User I/O Hardware Two tri-state buffers, U12 and U19, provide input ports to the Master Z80. The IO1/ address decode enables buffer U12 allowing status of SW2 (Select control) and SW3 (Adjust control) to be examined.

IO2/ enables U19. SW1 (MIDI LEARN button on front panel) is connected to a pullup resistor in RP2. When pressed, a low state is produced on pin 11 of U19. An external on/off switch connected to the FOOTSWITCH input jack on the rear panel will control the logical state of the FOOT/ signal. FOOT/ is normally high due to its connection to a pullup resistor (RP2). R19 and C16 on FOOT/ act as an RFI filter. CR7 and CR8 provide overvoltage and static protection for the FOOT/ input. SINT/, which indicates the status of Slave Processor interrupt, is monitored on pin13 of U19. A low state indicates the Slave Z80 interrupt has been asserted but not acknowledged.

The bi-color front panel LEARN LED is controlled by the status of bits 3 and 4, which are latched into U5 by a Master Z80 write-to-port address IO4. Bit 3 high; bit 4 low will result in a green display. Bit 3 low; bit 4 high results in a red display. When bit 3 = 4, the LED is off.

Signal and Bus Descriptions

[L] = active Low
[H] = active High

Master PAL

ROM/ U11 Pin 12 [L]
Master ROM enable. Activates the ROM IC, U10.

RAM/ U11 Pin 13 [L]
Master RAM enable. Activates RAM IC U17.

MSREQ/ U11 Pin 14 [L]
Requests access to Slave bus.

IO1/ U11 Pin 16 [L]
Enables input buffer so that status of SW2 and 3 can be read.

UART/ U11 Pin 15 [L]
Enables UART IC for R/W operations.

IO2/ U11 Pin 17 [L]
Enables input buffer so that status of SW5, LEARN button, Footswitch and SINT/ can be read.

IO3 U11 Pin 19 [H]
Sets slave interupt (SINT/). This output remains high once set by Master Z80. SINT/ , the active low Slave interrupt signal is produced by inverting IO3 with inverter U1. When Slave Z80 services the interrupt, INTACK/ is generated by its decoding PAL to clear SINT/ and gate U18 pin 8 with a signal fed back into the Master PAL creating an SR latch function set by the Master Z80 and cleared by the Slave Z80.

IO4 U11 Pin 18 [H]
Data bits 0, 1, and 2 are used to control the following functions :

Bit 0 is ANDed with IO4 to produce MSYNC. This syncronizes the Master Z80 with the WC signal produced by the Digital Audio Processor by placing Z80 into a wait condition until the falling edge of WC/ occurs.

Bits 1,2,3 and 4 are latched into U5 , a 74HCT174 . Bit 1 sets the active low MUTE/ signal which controls the Audio Muting Circuitry. Bit 2 sets the active low SRST/ signal which controls Slave Z80 Reset. Bits 3 and 4 control the status of the multicolor LEARN LED as described previously. Note that the 74HCT174, U5 ,outputs are all set low on power up by ZRST/, activating both MUTE/ and SRST/ and setting the LEARN LED to an OFF condition.

Slave PAL

INTACK/ U6 Pin 12 [L]
Slave Interrupt is used to clear the SINT/ signal asserted by the Master Z80. This signal is created by ANDing the Slave IORQ and Slave M1 signals. This is performed by the Z80 to indicate interrupt acknowledgement .

LEX/ U6 Pin 18 [L]
Lexichip Z80 port enable. Allows Z80 R/W access to the internal Writeable Control Store of the Lexichip.

SRAM/ U6 Pin 19 [L]
Slave RAM enable. Activates Slave RAM IC ,U20.

MWAIT/ U6 Pin 14 [L]
Master Z80 WAIT. This signal is activated by one of the following two conditions:

If MSREQ/ is asserted outside the Slave Z80 refresh period MWAIT will force the Master Z80 to insert wait states until the next available Slave refresh period before gaining access to the Slave Bus.

When MSYNC is asserted by the Master Processor, MWAIT will force the Master Z80 to insert wait states until the falling edge of WC/.

MACC/ U6 Pin 16 [L]
Master access. In a low state , this signal disables Slave Z80 address bus buffers (U8, U15) and enables Master Z80 address buffers (U9, U16) and data bus buffer (U7), thereby allowing Master Processor access to Slave bus. This active low state occurs if MSREQ/ has been asserted AND either a Slave Refresh period occurs or Slave reset (SRST/) is activated.

UCLK U6 Pin 17
UART Clock. The 4MHz ZCLK input is divided by two to create this 2MHz UART clock.

Signal Glossary

CAS/ Column address strobe low (from Lexichip)

CAS1/ Column address strobe 1 low (to DRAMs)

DAB <0:15> Digitized audio bus (from Lexichip)

DAC <0:15> Digitized audio bus (to D/A Converter)

DATA Serial audio data (from comparator)

DEG0 Deglitch 0

DEG1 Deglitch 1

FOOT/ Footswitch low

INTACK/ Interrupt acknowledge low

IO1/ Input/Output enable 1 low

IO2/ Input/Output enable 2 low

IO3 Input/Output enable 3

IO4 Input/Output enable 4

LEX/ Lexichip enable low

LRADR <0:12> Lexichip RAM address bus

LRCB Lexichip RAM control bus

LRMREQ/ Lexichip RAM memory request low

LRRD/ Lexichip RAM read low

LRWR/ Lexichip RAM write low

MA <0:7> Audio memory address bus

MACC/ Master Z80 access low

MADR <0:15> Master Z80 address bus

MCB Master Z80 control bus

MDB <0:7> Master Z80 data bus

MIDICLK/ MIDI clock

MINT/ Master Z80 interrupt low

MIORQ/ Master Z80 I/O request low

MM1/ Master Z80 machine cycle 1 low

MMREQ/ Master Z80 memory request low

MRD/ Master Z80 read low

MRST/ Master Z80 reset low

MSREQ/ Master Z80 slave bus request low

MSYNC Master Z80 sync

MUTE/ Audio mute enable low

MWAIT/ Master Z80 wait low

MWR/ Master Z80 write low

N/C No connection

OVLD/ Processed signal overload low

PB Pushbutton (signal from LEARN switch)

PLUP Pull-up

PU1 Pull-up 1

RAM/ Master RAM enable low

RAS/ Row address strobe low

RCE RAM chip enable

ROM/ Master ROM enable low

SADR <0:12> Slave Z80 address bus

SAMP Sample

SCB Slave Z80 control bus

SDB <0:7> Slave Z80 data bus

SINT/ Slave Z80 interrupt low

SIORQ/ Slave Z80 I/O request low

SLVACC/ Slave Z80 access low

SM1/ Slave Z80 machine cycle 1 low

SMREQ/ Slave Z80 memory request low

SRAM/ Slave RAM enable low

SRD/ Slave Z80 read low

SRSEL Slave RAM select

SRST/ Slave Z80 reset low

SW1-[1-4] Rotary switch 1; data bits 1-4

SW2-[1-4] Rotary switch 2; data bits 1-4

SW3-[1-4] Rotary switch 3; data bits 1-4

SWAIT/ Slave Z80 wait low

SWR/ Slave Z80 write low

UART/ UART enable low

UCLK UART clock

VRAM RAM supply voltage

WC/ Word clock

WCE/ Word clock extended

WE/ Write enable low (from Lexichip)

WE1/ Write enable 1 low (to DRAMs)

ZCLK Z80 clock

ZRST Z80 reset

4

Specifications

Specifications

Audio Inputs (2)
Level: -20 dBu minimum
Impedance: Stereo:50 kilohms unbalanced
Mono:25 kilohms unbalanced
Connectors: 1/4" phone jacks
(L or R may be used for mono input)

Audio Outputs (2)
Level: +4 dBu nominal,
+18 dBu maximum
Impedance: 600 ohms unbalanced
Connectors: 1/4" phone jacks
Mute Protection: removes unwanted transients during power up/down, or any power interruption
Static Protection

Frequency Response
Wet: 20 Hz - 15 kHz, + 1.0, -1.5 dB
Dry: 20 Hz - 20 kHz, ± 0.1 dB

Dynamic Range
85 dB, typical, 20 Hz to 20 kHz bandwidth

Total Harmonic Distortion (THD)
Wet: < 0.02% @ 1 kHz
Dry: < 0.01% @ 1 kHz

Encoding
16-bit linear PCM

Sampling Frequency
31.25 kHz

Memory
64 presets with 128 user registers available

Dynamic MIDI®
5 pin DIN connectors provided for MIDI IN and MIDI OUT (THRU) (MIDI OUT or THRU may be selected by rear panel switch)
LEARN button and status indicator provided on front panel

Footswitch
1/4" phone jack for connection to any on/off toggle or momentary contact switch. Functions include:
Input defeat
Output defeat
Bypass
Preset/user register memory step

Signal Level Indicators
Green Signal Present LED
Red Processed Signal Overload LED

Front Panel Controls
Input Level Adjust
Dry/Wet Mix Adjust
Output Level Adjust
Function and Select Controls (used for selecting a preset, user register, or edit parameter)
Adjust Control (used to modify a preset/register or adjust a specific parameter)

RFI Shielding
Complies with FCC Class A requirements for computer equipment

Power Requirements
9 VAC, 1.5 A from supplied wall transformer
5.0 mm/2.5 mm connector provided on rear panel

Dimensions
8.5" W x 1.7" H x 9.5" D (215.9 x 43.2 x 241.3 mm)

Weight
4.5 lb (2.05 kg)
Shipping weight: 5.0 lb (2.27 kg)

Environment
Operating temperature: 32° - 95°F (0° - 35°C)
Storage temperature: -22° - 167°F (-30° - 75°C)
Humidity: 95% maximum without condensation

(0dBu = 0.775 Vrms)

Specifications subject to change without notice

5

Parts List

Parts List

PC BOARD

PART NO.	QTY	DESCRIPTION	REF.
POTENTIOMETERS			
200-06034	1	POT,RTY,PC,50KBX2,6MM/FLT,16MM	R41
200-06035	2	POT,RTY,PC,50KAX2,6MM/FLT,16MM	R32,77
CARBON FLM RES			
202-00505	1	RES,CF,5%,1/4W,10OHM	R82
202-00514	3	RES,CF,5%,1/4W,100 OHM	R19,25,33
202-00515	1	RES,CF,5%,1/4W,150 OHM	R8
202-00517	1	RES,CF,5%,1/4W,100OHM	R81
202-00518	3	RES,CF,5%,1/4W,220 OHM	R1,9,15
202-00520	1	RES,CF,5%,1/4W,270 OHM	R7
202-00521	2	RES,CF,5%,1/4W,330 OHM	R72,76
202-00524	1	RES,CF,5%,1/4W,470 OHM	R80
202-00525	2	RES,CF,5%,1/4W,510 OHM	R26,34
202-00529	5	RES,CF,5%,1/4W,1K OHM	R3,4,20,58,59
202-00531	1	RES,CF,5%,1/4W,1.5K OHM	R79
202-00533	4	RES,CF,5%,1/4W,2K OHM	R11,60,61,63
202-00534	1	RES,CF,5%,1/4W,2.2K OHM	R10
202-00542	1	RES,CF,5%,1/4W,4.7K OHM	R6
202-00545	2	RES,CF,5%,1/4W,6.8K OHM	R39,40
202-00549	10	RES,CF,5%,1/4W,10K OHM	R2,5,13,16,21-24,31,78
202-00553	1	RES,CF,5%,1/4W,15K OHM	R29
202-00559	3	RES,CF,5%,1/4W,30K OHM	R37,38,62
202-00562	1	RES,CF,5%,1/4W,39K OHM	R30
202-00579	4	RES,CF,5%,1/4W,470K OHM	R27,28,35,36
METAL FLM RES			
203-00456	1	RES,MF,1%,1/8W,1.00K OHM	R17
203-00457	3	RES,MF,1%,1/8W,1.50K OHM	R50,51,68
203-00459	6	RES,MF,1%,1/8W,2.00K OHM	R44,49,54-57
203-00465	2	RES,MF,1%,1/8W,6.49K OHM	R45,48
203-00467	1	RES,MF,1%,1/8W,7.15K OHM	R66
203-00471	4	RES,MF,1%,1/8W,10.0K OHM	R18,65,70,75
203-01230	1	RES,MF,1%,1/8W,8.25K OHM	R14
203-01490	1	RES,MF,1%,1/8W,3.09K OHM	R67
203-02010	2	RES,MF,1%,1/8W,4.87K OHM	R42,47
203-02352	1	RES,MF,1%,1/8W,24.9K OHM	R12
203-02611	5	RES,MF,1%,1/8W,5.62K OHM	R43,46,52,53,64
203-02658	2	RES,MF,1%,1/8W,340 OHM	R71,74
203-02700	2	RES,MF,1%,1/8W,11.3K OHM	R69,73
NETWORK RES			
205-05638	2	RES,NET,SIP,2%,BUS EL,10KX9	RP1-2

PART NO.	QTY	DESCRIPTION	REF.
ELECTROLYT CAP			
240-00608	2	CAP,ELEC,2.2uF,50V,RAD	C10,11
240-00613	8	CAP,ELEC,22uF,25V,RAD	C5,42,54,56,58,61, 84,90
240-06096	8	CAP,ELEC,10uF,25V,RAD,NON-POL	C68,69,72,74,79, 81,92,99
240-06611	4	CAP,ELEC,1000uF,25V,RAD	C27-29,40
240-07335	2	CAP,ELEC,47uF,25V,RAD,NON-POL	C62,63
240-07336	2	CAP,ELEC,2200uF,25V,RAD	C26,39
PCRB/PP CAP			
244-01151	1	CAP,PP,1000pF,2.5%	C89
244-06883	3	CAP,MYL,.01uF,5%,RAD	C77,78,97
CERAMIC CAP			
245-03609	52	CAP,CER,.1uF,50V,Z5U,AX	C1-4,6,7,13-15,18-24,30-33 C35-37,41,43-47,49,50,52,55, C57,59,60,65,66,75,76,82,83, C86-88,91,93,94,100,101, C106,107
245-03610	5	CAP,CER,.01uF,100V,Z5U,AX	C25,38,53,70,96
245-03867	5	CAP,CER,10pF,100V,COG,10%,AX	C64,67,95,98,102
245-03868	4	CAP,CER,33pF,100V,COG,10%,AX	C34,104,105,108
245-03869	10	CAP,CER,100pF,100V,COG,10%,AX	C8,9,12,16,17,48,51,71,73,103
245-07344	2	CAP,CER,470pF,100V,COG,10%,AX	C80,85
INDUCTORS			
270-00779	9	FERRITE,BEAD	FB1-9
DIODES			
300-01024	1	DIODE,ZENER,3.3V,1N746	CR2
300-01028	2	DIODE,ZENER,7.5V,1N755	CR19,21
300-01029	9	DIODE,1N914 AND 4148	CR1,4,7,8,14,15,17,18,20
300-01030	5	DIODE,1N4004 AND 4005	CR9-13
300-02401	4	DIODE,BAR 35,SCHOTTKY,LOW VF	CR3,5,6,16
TRANSISTORS			
310-01007	5	TRANSISTOR,2N3904	Q3-5,9,10
310-01008	2	TRANSISTOR,2N3906	Q1,7
310-01647	1	TRANSISTOR,2N4401	Q2
310-06612	2	TRANSISTOR,J108	Q6,8
DIGITAL/CMOS IC			
330-01290	4	IC,DIGITAL,74LS244	U8,9,15,16
330-03586	2	IC,DIGITAL,74HCT244	U12,19
330-04271	2	IC,DIGITAL,74HCT273	U27,28
330-04272	1	IC,DIGITAL,74HCT163	U13
330-04572	1	IC,DIGITAL,74HCT245	U7
330-04589	1	IC,DIGITAL,74HCT14	U1
330-04675	1	IC,DIGITAL,74F08	U18
330-04764	1	IC,DIGITAL,74HCT174	U5
330-06204	1	IC,DIGITAL,LEXICHIP 1	U21

PART NO.	QTY	DESCRIPTION	REF.
LINEAR IC			
340-00725	1	IC,LINEAR,LM311	U32
340-00742	1	IC,LINEAR,7805 (LM 340 T-5)	U24
340-00743	1	IC,LINEAR,7812 (LM 340 T-12)	U25
340-01183	1	IC,LINEAR,LF 356	U39
340-01463	1	IC,LINEAR,7912	U26
340-01566	1	IC,LINEAR,LF353,DUAL OP AMP	U37
340-06036	4	IC,LINEAR,uPC4570,DUAL OP AMP	U33,34,40,42
INTERFACE IC			
345-06037	1	IC,INTER,82C51A	U3
SS SW IC			
346-00770	1	IC,SS SWITCH,4053	U38
MEMORY IC			
350-04282	2	IC,SRAM,4364,8KX8,150NS,LPS	U17,20
350-04434	4	IC,DRAM,64KX4,12ONS	U22,23,29,30
350-07351	1	IC,PAL,16L8B,LXP-5,MSTR,V1.00	U11
~~350-07352~~ 350-08236	1	IC,PAL,16RA,LXP-5,SLV,V1.00	U6
350-07353	1	IC,ROM,27C256,LXP-5,V1.00	U10
CONVERTER IC			
355-06038	1	DAC,PCM54HP	U31
MICROPROC IC			
365-04284	2	IC,uPROC,Z80,CMOS,4MHz	U4,14
OPTO ISLTOR IC			
375-02247	1	IC,OPTO-ISOLATOR,6N 138	U2
MODULES			
380-06039	3	MOD,LPF,LC,7P,15KHz	U35,36,41
CRYSTALS			
390-06647	1	CRYSTAL,16.000 MHZ,.01%	Y1
DSPLY/IND/LED			
430-07325	1	LED,RED,T1,LITON	LED2
430-07326	1	LED,GRN,T1,LITON	LED3
430-07337	1	LED,T1,RED/GRN	LED1
SLIDE SWITCH			
451-07338	1	SW,SL,2P2T,PCRA,ALCO MMS-22R	SW4
ROTARY SWITCH			
452-06045	3	SW,RTY,BCD,16 POS	SW2,3,5

PART NO.	QTY	DESCRIPTION	REF.
PSH BUT SWITCH			
453-06040	1	SW,PBM,2P2T,PCRA,2MM TRAV	SW1
BATTERIES			
460-04285	1	BAT,LITH,3V@160mAh,VERT COIN	BAT1
TRANSFORMERS			
470-07345	1	XFORMER,PLUG-IN,120V,9VAC,1.5A	
PC MNT CONN			
510-06041	2	CONN,DIN,5FC@180DEG,PCRA,DJ006	J1,2
510-06042	1	CONN,DC POWER,PC,DJ005,2.5MM	J4
510-07342	5	1/4" PHONE JACK,SWCFT-RN112APC	J3,5-8
SOCKETS			
520-00946	2	IC SCKT,40 PIN,PC,LO-PRO	U4,14
520-01361	2	IC SCKT,20 PIN,PC,LO-PRO	U6,11
520-01458	5	IC SCKT,28 PIN,PC,LO-PRO	U3,10,17,20,31
520-02177	4	IC SCKT,18 PIN,PC,LO-PRO	U22,23,29,30
520-06184	1	IC SCKT,PLCC,84 PIN	U21
KNOBS/CAPS			
550-06044	1	BUTTON,5MMSQ,2.8MM TANG,BLK	SW1
INSUL/SPACRS			
630-00952	3	INSUL,SEMI,BUSHING,TO-220	U24-26
630-07339	3	INSUL,SEMI,SIL RUB,TO-220SHORT	U24-26
THRD-FORM SCRW			
641-04021	3	SCRW,TAP,SW,4-40X1/4,PNH,PH,ZN	U24-26
BRACKETS			
701-07334	1	BRACKET,HEATSINK,LXP-5	U24-26
PC BOARDS			
710-07310	1	PC BD,LXP-5	

MECHANICAL

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-07332	1	MANUAL,OWNER'S,LXP-5	
GROMMETS			
540-06032	2	BUMPER,GUIDE,PCB,5.75"	
FEET			
541-06033	2	BUMPER,FEET,STRIP,7.0"	
KNOBS/CAPS			
550-06031	6	KNOB,.75,6MM/FLAT,SKT,BLK	
MACHINE SCREWS			
640-02749	1	SCRW,6-32X1/4,PNH,PH,SEMS,BLK	HEATSINK TO REAR PANEL
THRD-FORM SCRW			
641-06575	2	SCRW,TAP,C,6-32X1/4,THG,PH,BLK	REAR PANEL
641-06757	2	SCRW,TAP,SW,6-32X1/2,PNH,PH,BK	FRONT PANEL
CHASSIS/MECH			
700-07317	1	ENCLOSURE,LXP,8.90L	
PANELS			
702-07319	1	PANEL,FRONT,LXP-5	
702-07321	1	PANEL,REAR,LXP-5	
702-07341	1	INSUL,GSKT,.406DX2,FISHPPR/ADH	J7,8
SHIPPING MAT			
730-02813	1	CARD,REGISTRATION,LEXICON	
730-06760	1	BAG,CLEAR,12X12X.004	
730-06785	1	CARD,WARRANTY,LEXICON,5.5X7	
730-07327	1	BOX,17-9/16X10-7/8X3-3/4	
730-07328	1	INSERT,FOAM,TOP,LXP-5	
730-07329	1	INSERT,FOAM,BOTTOM,LXP-5	
LABEL/NAMEPLTS			
740-06422	1	LABEL,PRODUCT ID,UNIVERSAL	
740-07346	1	LABEL,LEXICON LOGO	TOP OF UNIT

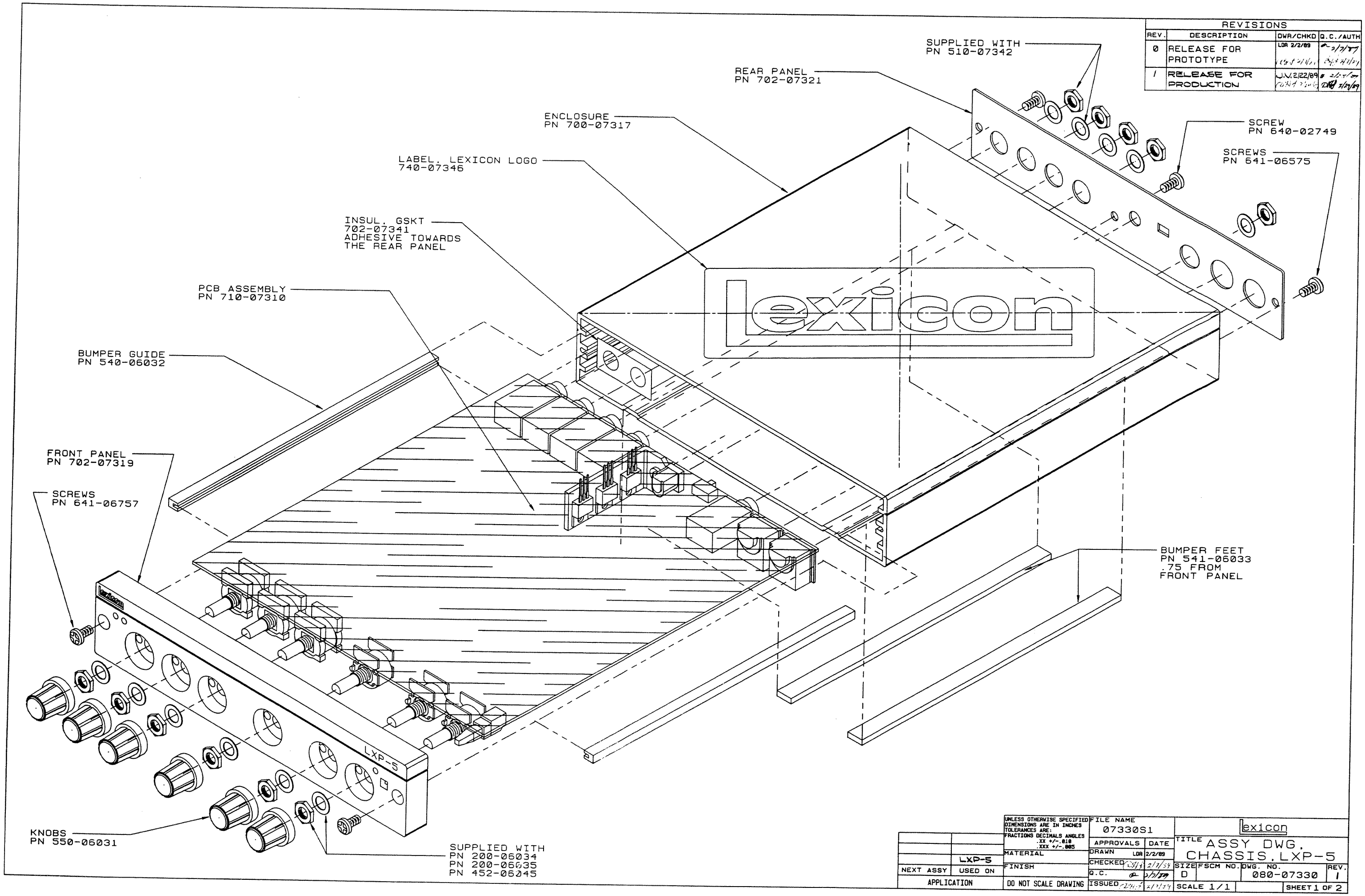
MOUNTING TRAY OPTION

PART NO.	QTY	DESCRIPTION	REF.
MACHINE SCREWS			
640-06961	2	SCRW,10-32X5/16,FH,UNDC,PH,BLK	
CHASSIS/MECH			
700-06543	1	TRAY,MTG,RACK,LXP-1	
SHIPPING MAT			
730-02824	1	BAG,CLEAR,3X5X.002	
730-06796	1	BOX,19X8X1.75	

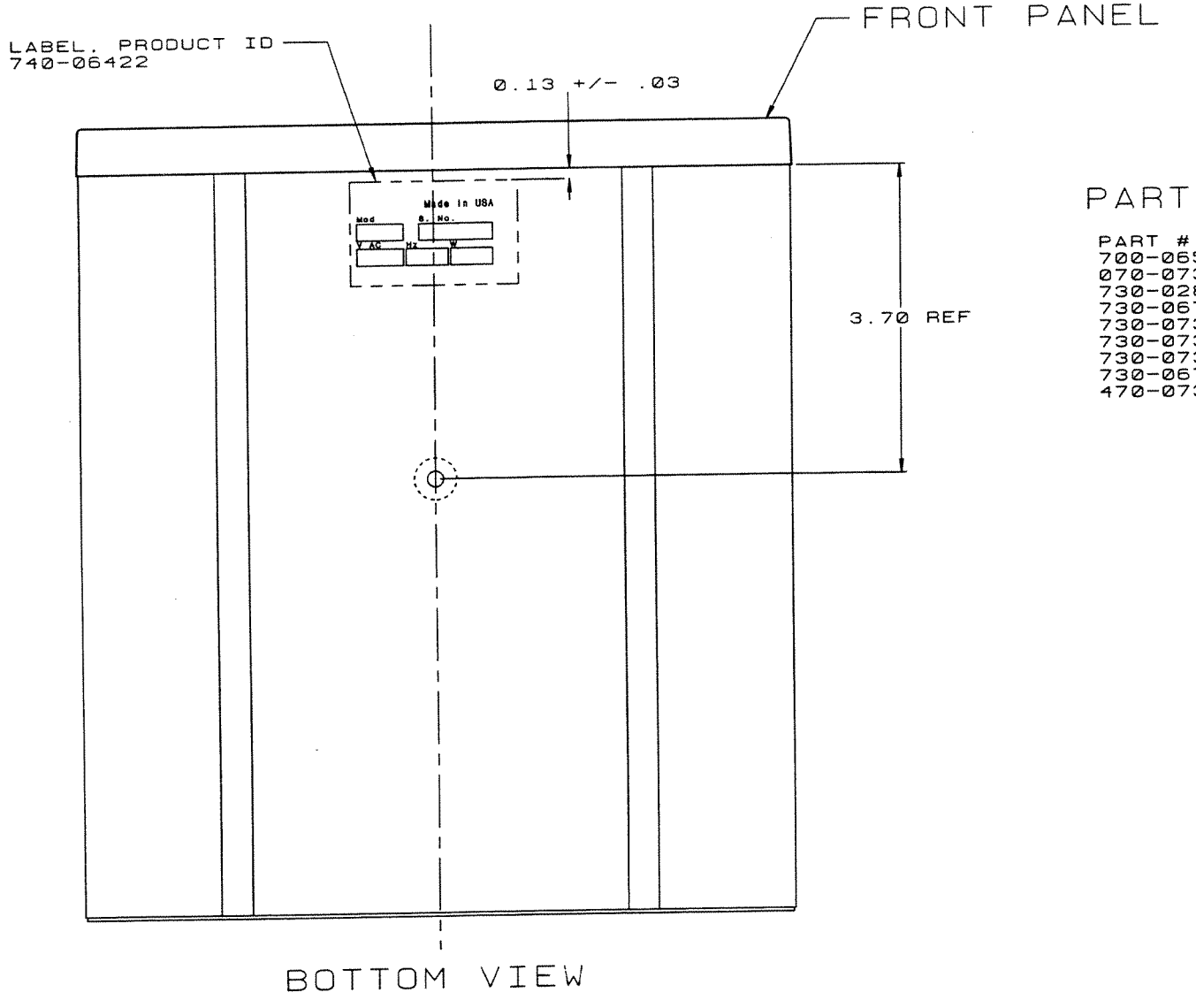
6

Schematics and Assembly Drawings

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
0	RELEASE FOR PROTOTYPE	LDR 2/2/89	2/2/89
1	RELEASE FOR PRODUCTION	J.V. 2/22/89	2/27/89



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX +/-.010 .XXX +/-.005	FILE NAME 07330S1	Lexicon	
			APPROVALS / DATE	TITLE ASSY DWG. CHASSIS.LXP-5	
	LXP-5	MATERIAL	DRAWN LDR 2/2/89		
NEXT ASSY	USED ON	FINISH	CHECKED 2/27/89	SIZE D / FSCM NO. / DWG. NO. 080-07330 / REV. 1	
APPLICATION		DO NOT SCALE DRAWING	Q.C. 2/27/89		
			ISSUED 2/27/89	SCALE 1/1	SHEET 1 OF 2



BOTTOM VIEW

PARTS NOT SHOWN

PART #	DESCRIPTION
700-06543	RACK MOUNTING TRAY
070-07332	OWNER'S MANUAL
730-02813	REGISTRATION CARD
730-06785	WARRANTY CARD
730-07329	FOAM INSERT, REAR, LXP
730-07328	FOAM INSERT, FRONT, LXP
730-07327	SHIPPING BOX
730-06760	CLEAR SHIPPING BAG
470-07345	TRANSFORMER, 120V, 9VAC, 1.5A

REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
Ø	RELEASE FOR PROTOTYPE	LDR 2/2/89 DKB 2/7/89	DKB 2/7/89
1	RELEASE FOR PRODUCTION	J.V. 2/22/89 LDR 2/24/89	DKB 2/27/89

NOTES

1. FRONT POT NUTS TO BE TIGHTENED TO 6-8 IN-LBS FRONT SWITCH NUTS TO BE TIGHTENED TO 4 IN-LBS MAX. REAR PHONE JACK NUTS TO BE TIGHTENED TO 4-6 IN-LBS.
2. INSURE THE POWER JACK ALIGNS TO THE REAR PANEL, PRIOR TO SECURING THE REAR PANEL TO THE ENCLOSURE AND THE PCB.

	LXP-5
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH
DO NOT SCALE DRAWING

FILE NAME 07330S2

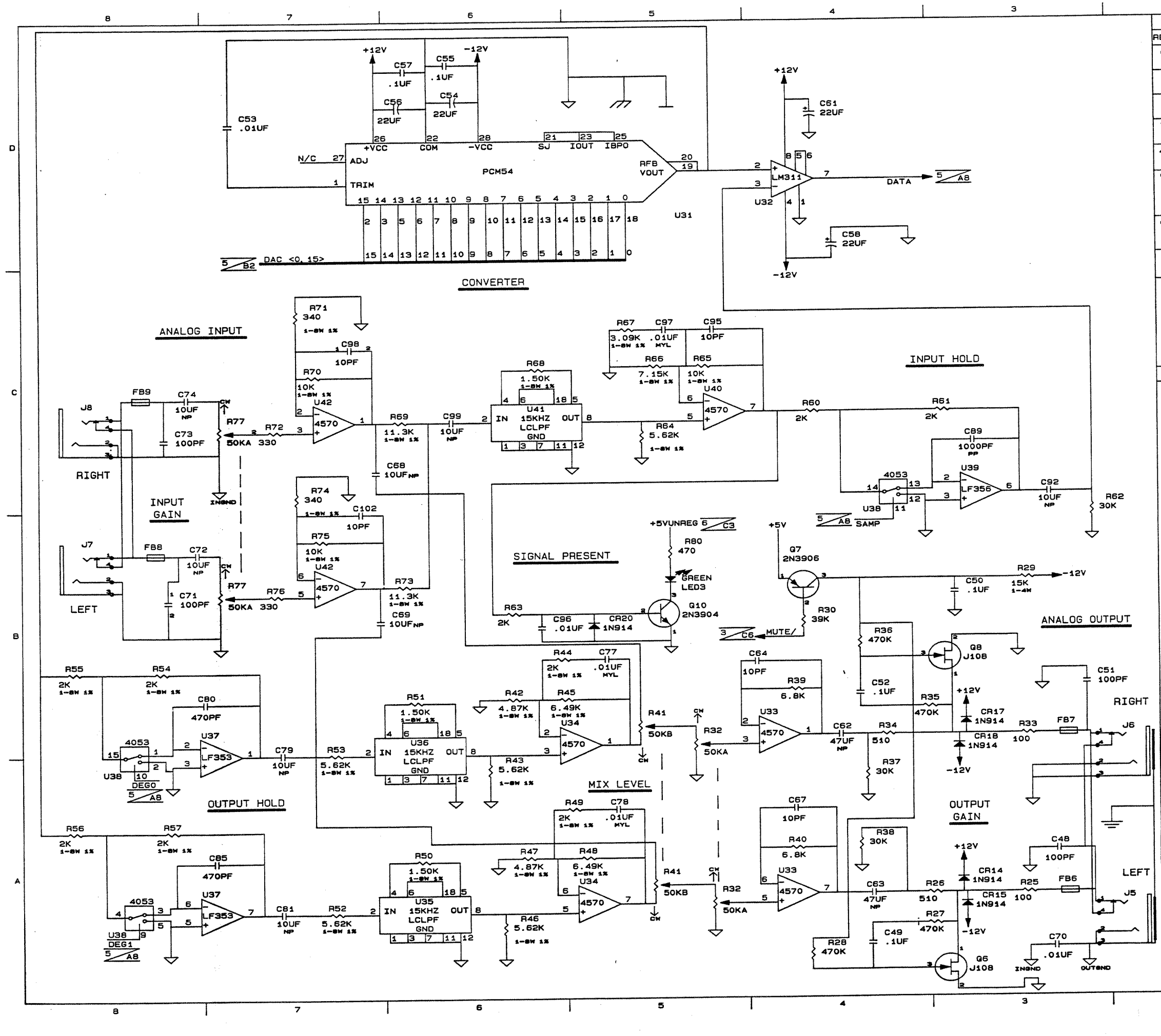
APPROVALS	DATE
DRAWN LDR	2/2/89
CHECKED	
Q.C.	2/7/89
ISSUED	

Lexicon

TITLE ASSY, DWG CHASSIS, LXP-5

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-07330	1

SCALE 1/1 SHEET 2 OF 2



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	G.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 1/18/89 AF 1/18/89	RWH 1/18/89 DHS 1/18/89
1	RELEASE FOR PILOT	DHS 2/27/89 AF 2/27/89	DHS 2/27/89 DHS 2/27/89
2	RELEASE FOR PRODUCTION	AF 3/1/89 MWH 3/1/89	DHS 3/1/89 DHS 3/1/89
3	CHANGED SHEET 3 PER ECO#890508-00	J.V. 6/2/89 RWH 6/7/89	RWH 6/7/89 6/7/89 DHS
4	CHANGED SHEETS 1,2,3,4 & 6, PER ECO#890718-00	J.V. 7/18/89 AF 7/20/89	JV 7/24/89 DHS 7/31/89
5	CHANGED SHEETS 3 & 5 PER ECO#891122-01 & CHANGED SHEET 3 PER ECO#900105-00	J.V. 12/15/89 DHS 12/15/89	JV 12/13/89 MWH 1/4/90 DHS 1/29/90
6	CHANGED DOC.CTL. BLK. SHEETS 1 & 6 PER ECO#900202-02.	J.V. 2/16/90 DHS 3/9/90	CW 3/9/90 DHS 3/12/90
7	CHANGED DOC. CTL. BLK. SHEET 1 & 2 PER ECO# 900530-01	MWH 6-19-90 AF 6/20/90	RWH 6/19/90 7/2/90 DHS

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. 1/A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO, ON BOARD CONNECTION-FROM, SOLDER CONNECTION

DOCUMENT CONTROL BLOCK: #060-07316	
SHEET NUMBER	REVISION NUMBER
1 OF 6	7
2 OF 6	4
3 OF 6	5
4 OF 6	3
5 OF 6	3
6 OF 6	4

CONTRACT NO.	exicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEMATIC, LXP - 5 ANALOG AND CONVERTER			
DRAWN MWH	1/11/89				
CHECKED AF	1/18/89	SIZE	CODE	NUMBER	REV.
G.C. RWH	1/18/89	D		060-07316	7
ISSUED DHS	1/18/89	SHEET 1 OF 6			

MASTER PROCESSOR

ROM

RAM

REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 1/18/89 AF 1/18/89	RWH 1/18/89 DHS 1/18/89
1	RELEASE FOR PILOT	DHS 2/27/89 AF 2/27/89	DHS 2/27/89 DHS 2/27/89
2	RELEASE FOR PRODUCTION	AF 3/1/89 MWH 3/7/89	DHS 3/2/89 DHS 3/2/89
3	CHANGED PER ECO#890718-00	JV 7/18/89 AF 7/20/89	RW 7/19/89 DHS 7/24/89
4	CHANGED PER ECO# 900530-01	MWH 6.19.90 AF 6/20/90	RWH 6/19/90 DHS 7/2/90

MADR<0: 15>

PLUP

ZCLK 6

Z80

BUSREQ, BUSACK, WAIT, VCC, GND

A0–A15 → MADR0–MADR15

MRD/, MWR/, MINT/, NMI, HALT, MREQ, IORQ, RESET, RFSH, M1

D0–D7 → MDB0–MDB7

U4

R81 200

MM1/ C104 33PF

DECODER

MADR15

27256 (U10)

MADR0–MADR14 → A0–A14

O0–O7 → MDB0–MDB7

Vpp → W1 → +5V

ROM/, CE, OE

62C64 (U17)

MADR0–MADR12 → A0–A12

I/O0–I/O7 → MDB0–MDB7

MWR/ → WE, RAM/ → CE1, RCE → CE2, MRD/ → OE

VCC → C22 .1UF

MDB<0: 7>

MCB

PAL16L8 (U11)

MMREQ/, MIORQ/, MM1/, MADR15, MADR14, MADR13, MADR7, MADR6, MADR5

ROM/, RAM/, MSREQ/, UART/, IO1/, IO2/, IO4, IO3

74F08 U18: MDB0, IO3 → MSYNC

74F08 U18: IO4, IO2/ → 74AC14 U1 → SINT/

INTACK/

CR5 BAR35, C10 0.1UF, R5 100K → 74AC14 U1 → ZRST

ZRST/

VRAM

+5VUNREG

CR4 1N914, R20 1K, Q5 2N3904

R16 10K, Q4 2N3904

CR16 BAR35, C42 22UF, BAT1 +3VDC

BATTERY BACKUP

POWER FAIL

+5VUNREG, FB3, C17 100PF, R18 10K 1-8W 1%, C11 2.2UF, R17 1K 1-8W 1%

R11 1.5K,1%, 1/8W, Q3 2N3904

R12 24.9K 1-8W 1%

RESET

+5V, R3 1K, CR2 1N746, R4 1K, Q1 2N3906, R2 10K

RCE

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA. 02154		
APPROVALS	DATE	TITLE	SCHEMATIC, LXP - 5 MASTER PROCESSOR
DRAWN MWH	1/11/89		
CHECKED AF	1/18/89	SIZE / CODE / NUMBER	D / / 060-07316
Q.C. RWH	1/18/89	REV.	4
ISSUED DHS	1/18/89	SHEET 2 OF 6	

MASTER BUFFER

74HCT245 — U7

MDB0	18	B1	A1	2	SDB0
MDB1	17	B2	A2	3	SDB1
MDB2	16	B3	A3	4	SDB2
MDB3	15	B4	A4	5	SDB3
MDB4	14	B5	A5	6	SDB4
MDB5	13	B6	A6	7	SDB5
MDB6	12	B7	A7	8	SDB6
MDB7	11	B8	A8	9	SDB7
MWR/	1	DIR			
	19	G			

2/B3 MCB

MIDI

2/B3 MDB<0: 7>

R8 150 — LED1 R/G

74HCT174 — U5

MDB1	3	1D	1Q	2	MUTE/
MDB2	4	2D	2Q	5	SRST/
MDB3	6	3D	3Q	7	
MDB4	11	4D	4Q	10	
	13	5D	5Q	12	N/C
	14	6D	6Q	15	N/C
	1	CLR			
	9				

1/B4

2/A5 ZRST/

2/B5 IO4

C103 100PF

+5V

R14 8.25K 1-8W 1%

5/A8 WC/ — CR6 BAR35 — WCE/

C12 100PF

SLAVE PROCESSOR

Z80 — U14

5/B6 ZCLK	6	A0	30	SADR0
+5V	25	A1	31	SADR1
N/C	23	A2	32	SADR2
SWAIT/	24	A3	33	SADR3
5/B7 SCB		A4	34	SADR4
	11	A5	35	SADR5
VCC		A6	36	SADR6
	29	A7	37	SADR7
GND		A8	38	SADR8
		A9	39	SADR9
		A10	40	SADR10
		A11	1	SADR11
		A12	2	SADR12
		A13	3	N/C
		A14	4	N/C
		A15	5	N/C
SM1/	27	M1		
N/C	28	AFSH		
SINT/	16	INT		
+5V	17	NMI		
N/C	18	HALT		
SRST/	26	RST		
SIORQ/	20	IORQ		
SMREQ/	19	MREQ		
SWR/	22	WR		
SRD/	21	RD		
2/B5		D0	14	SDB0
		D1	15	SDB1
		D2	12	SDB2
		D3	8	SDB3
		D4	7	SDB4
		D5	9	SDB5
		D6	10	SDB6
		D7	13	SDB7

SCB

SLAVE BUFFER

74LS244 — U8

SADR0	2	1A1	1Y1	18	LRADR0
SADR1	4	1A2	1Y2	16	LRADR1
SADR2	6	1A3	1Y3	14	LRADR2
SADR3	8	1A4	1Y4	12	LRADR3
SADR4	11	2A1	2Y1	9	LRADR4
SADR5	13	2A2	2Y2	7	LRADR5
SADR6	15	2A3	2Y3	5	LRADR6
SADR7	17	2A4	2Y4	3	LRADR7
	1	1G			
SLVACC/	19	2G			

SADR

74LS244 — U15

SADR8	2	1A1	1Y1	18	LRADR8
SADR9	4	1A2	1Y2	16	LRADR9
SADR10	6	1A3	1Y3	14	LRADR10
SADR11	8	1A4	1Y4	12	LRADR11
SADR12	11	2A1	2Y1	9	LRADR12
SRD/	13	2A2	2Y2	7	LRRD/
SWR/	15	2A3	2Y3	5	LRWR/
SMREQ/	17	2A4	2Y4	3	LRMREQ/
	1	1G			
SLVACC/	19	2G			

LRADR<0: 12>

SDB<0: 7>

LRCB

5/C8 5/B8 4/A3 5/B8

74AC14 — U1

1 — 2 SLVACC/

SLAVE DECODER

74LS244 — U9

MADR0	2	1A1	1Y1	18	LRADR0
MADR1	4	1A2	1Y2	16	LRADR1
MADR2	6	1A3	1Y3	14	LRADR2
MADR3	8	1A4	1Y4	12	LRADR3
MADR4	11	2A1	2Y1	9	LRADR4
MADR5	13	2A2	2Y2	7	LRADR5
MADR6	15	2A3	2Y3	5	LRADR6
MADR7	17	2A4	2Y4	3	LRADR7
	1	1G			
	19	2G			

2/B5 2/B6 5/B6 2/B6

PAL16R4 — U6

SRST/	2	I1		
MSYNC	3	I2	IO1	12	INTACK/
WCE/	4	I3	IO2	13	SWAIT/
ZCLK	1	CLK	IO3	18	LEX/
	11	OE	IO4	19	SRAM/
SIORQ/	5	I4	Q1	14	MWAIT/
MSREQ/	6	I5	Q2	15	N/C
LRMREQ/	7	I6	Q3	16	MACC/
LRADR12	8	I7	Q4	17	UCLK
SM1/	9	I8			

2/B8 SCB 5/B7

2.7Ω LEXL R83 5/B6

MCB 2/B3

4/C8

2/B3 MADR<0: 15>

74LS244 — U16

MADR8	2	1A1	1Y1	18	LRADR8
MADR9	4	1A2	1Y2	16	LRADR9
MADR10	6	1A3	1Y3	14	LRADR10
MADR11	8	1A4	1Y4	12	LRADR11
MADR13	11	2A1	2Y1	9	LRADR12
MADR12	13	2A2	2Y2	7	SRSEL
MRD/	15	2A3	2Y3	5	LRRD/
MWR/	17	2A4	2Y4	3	LRWR/
	1	1G			
	19	2G			

2/B3 MCB

SRSEL 4/A3

SLAVE RAM

62C64 — U20

LRADR0	10	A0	I/O0	11	SDB0
LRADR1	9	A1	I/O1	12	SDB1
LRADR2	8	A2	I/O2	13	SDB2
LRADR3	7	A3	I/O3	15	SDB3
LRADR4	6	A4	I/O4	16	SDB4
LRADR5	5	A5	I/O5	17	SDB5
LRADR6	4	A6	I/O6	18	SDB6
LRADR7	3	A7	I/O7	19	SDB7
LRADR8	25	A8			
LRADR9	24	A9			
LRADR10	21	A10	VCC	28	
LRADR11	23	A11			
SRSEL	2	A12			
SRAM/	20	CE			
LRRD/	22	OE			
LRWR/	27	WE			
	26	CE			

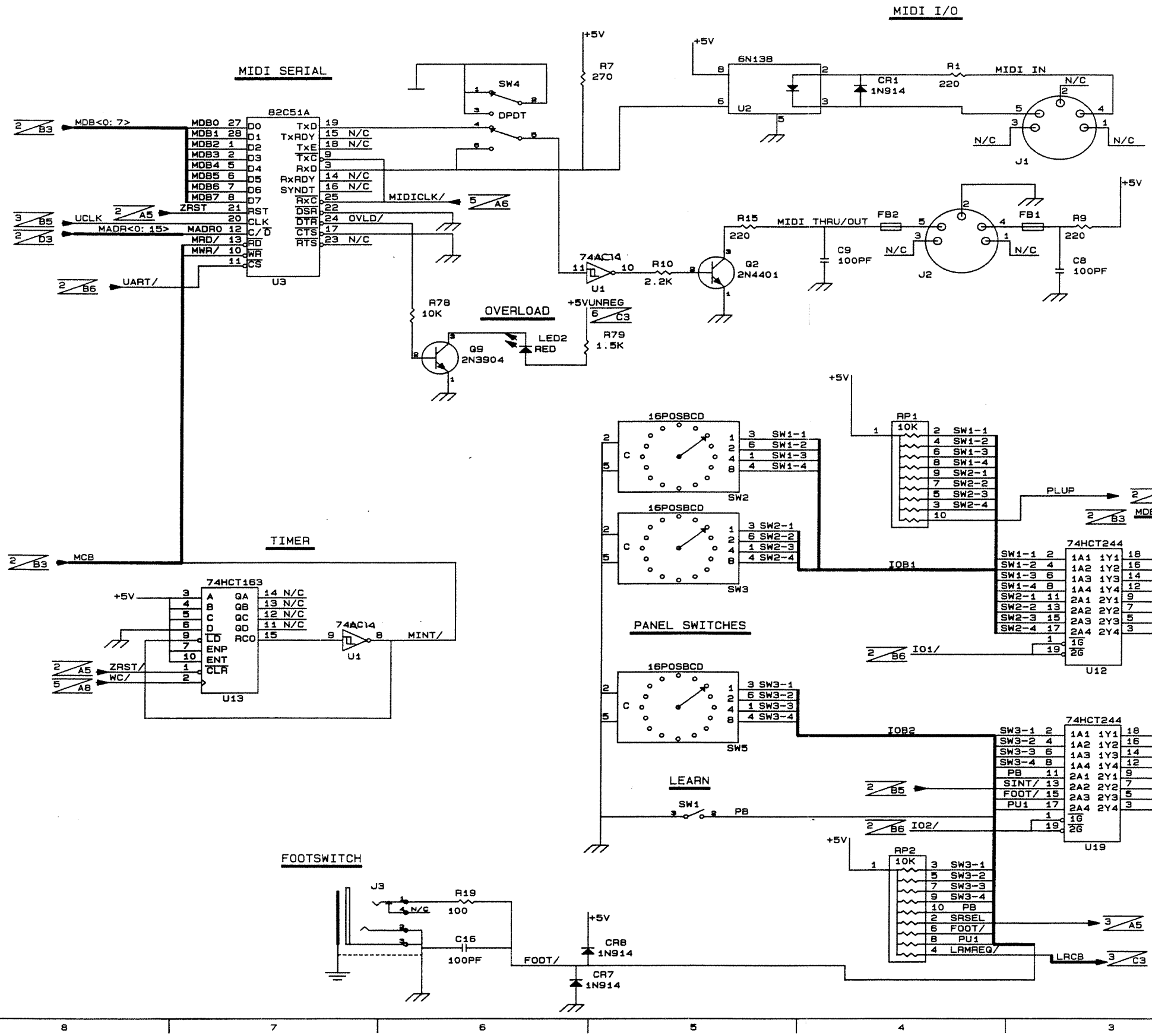
VRAM 2/B3

C43 .1UF

RCE 2/A3

REVISIONS				
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 1/18/89 AF 1/18/89	RWH 1/18/89 DHS 1/18/89
1	RELEASE FOR PILOT	DHS 2/27/89 AF 2/27/89	DHS 2/27/89 DHS 2/27/89
2	RELEASE FOR PRODUCTION	AF 3/1/89 MWH 3/1/89	DHS 3/1/89 DHS 3/1/89
3	ADD 100pf CAP FROM U20 PIN 27 TO GND, TO BE USED WHEN RCA SRAMS ARE INSTALLED PER ECO#890508-00	J.V. 6/2/89	RWH 6/7/89 DHS 6/7/89
4	CHANGED PER ECO#890718-00	J.V. 7/18/89 AF 7/20/89	RW 7/24/89 DHS 7/24/89
5	CHANGED U6, PAL16R4 TO GAL16V8 PER ECO#891122-01. ADD R83 CHANGED U6 GAL16V8 TO PAL16R4 PER ECO#900105-00.	J.V. 12/15/89 DHS 1/9/90	RW 1/11/90 RWH 1/11/90 DHS 1/25/90

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEMATIC, LXP - 5 SLAVE PROCESSOR
DRAWN MWH	1/11/89		
CHECKED AF	1/18/89	SIZE: D	CODE:	NUMBER: 060-07316	REV: 5
Q.C. RWH	1/18/89		
ISSUED DHS	1/18/89	SHEET 3 OF 6	



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 1/18/89 AF 1/18/89	MWH 1/18/89 DHS 1/18/89
1	RELEASE FOR PILOT	DHS 2/27/89 AF 2/27/89	DHS 2/27/89 DHS 2/27/89
2	RELEASE FOR PRODUCTION	AF 3/1/89 MWH 3/1/89	DHS 3/2/89 DHS 3/2/89
3	CHANGED PER ECO#890718-00	J.V. 7/18/89 AF 7/20/89	7/21/89 DHS 7/24/89

NOTES

1. SW4 SHOWN IN MIDI OUT POSITION.

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE	SCHEMATIC, LXP - 5 I/O, MIDI, COUNTER
DRAWN MWH	1/11/89		
CHECKED AF	1/18/89	SIZE: D	CODE:
Q.C. RWH	1/18/89	NUMBER: 060-07316	REV.: 3
ISSUED DHS	1/18/89	SHEET 4 OF 6	

AUDIO MEMORY

4464 DRAM — U22, U23, U29, U30

MA7 10, MA6 6, MA5 7, MA4 8, MA3 11, MA2 12, MA1 13, MA0 14 → A7, A6, A5, A4, A3, A2, A1, A0

VDD 9 → +5V

CAS 16 → CAS1/

RAS 5 → RAS/

WRT 4 → WE1/

U22: D3 3 → DAB3; D2 2 → DAB2; D1 17 → DAB1; D0 15 → DAB0

U23: D3 3 → DAB7; D2 2 → DAB6; D1 17 → DAB5; D0 15 → DAB4

U29: D3 3 → DAB11; D2 2 → DAB10; D1 17 → DAB9; D0 15 → DAB8

U30: D3 3 → DAB15; D2 2 → DAB14; D1 17 → DAB13; D0 15 → DAB12

VSS 18 → GND; G 1 → GND

DAB<0: 15>

MA<0: 7>

74F08 U18: 1, 2 → 3 CAS1/

74F08 U18: 4, 5 → 6 WE1/

AUDIO PROCESSOR

3/C3 LRADR<0: 12>

3/D6 SCB

LRADR9 80, LRADR8 81, LRADR7 82, LRADR6 3, LRADR5 4, LRADR4 5, LRADR3 6, LRADR2 7, LRADR1 8, LRADR0 9 → ZA9, ZA8, ZA7, ZA6, ZA5, ZA4, ZA3, ZA2, ZA1, ZA0

ZCLK 79 → ZCLK → 3/B6, 3/D6, 2/D8

WAIT 18 → SWAIT/

OVLD 58 → N/C

IN 68 → N/C

OUT 69 → N/C

67 → N/C

XA1 66 → N/C

XA0 23 → MA7

A7 28 → MA6

A6 26 → MA5

A5 24 → MA4

A4 25 → MA3

A3 27 → MA2

A2 29 → MA1

A1 31 → MA0

A0 30

RAS 33 → CAS/

CAS 32 → WE/

3/C3 SDB<0: 7> → SDB7 10, SDB6 11, SDB5 12, SDB4 13, SDB3 14, SDB2 15, SDB1 16, SDB0 17 → ZD7, ZD6, ZD5, ZD4, ZD3, ZD2, ZD1, ZD0

3/C3 LACB

LRAD/ 20 → RD

LRAWR/ 21 → WR

LEX/ 19 → CS

3/B5, 2/A5 ZRST/74 → RESET

77 → MCIN

78 → MCOUT

76 → XTALO

75 → XTAL1

C34 33PF; Y1 16MHZ

4/B8, 3/C8 WC/ 59 → WC

63 → CCLK1

N/C 62 → CCLKO

DEG1 61 → DEG1

DEG0 60 → DEG0

SAMP 65 → HOLD

1/A8, 1/B4

70 → SIO

DATA 71 → SI1

1/D3

R13 10K; +5V

LEXICHIP U21

DAB19 57 → DAB15

DAB18 56 → DAB14

DAB17 55 → DAB13

DAB16 54 → DAB12

DAB15 53 → DAB11

DAB14 52 → DAB10

DAB13 51 → DAB9

DAB12 50 → DAB8

DAB11 49 → DAB7

DAB10 48 → DAB6

DAB09 44 → DAB5

DAB08 43 → DAB4

DAB07 42 → DAB3

DAB06 41 → DAB2

DAB05 40 → DAB1

DAB04 39 → DAB0

DAB03 38

DAB02 37

DAB01 36

DAB00 35

PCLKO 72 → MIDICLK/ → 4/C6

PCLK1 73

R82 10; RAS/; C105 33PF

R23 10K; R24 10K; R21 10K; R22 10K; R31 10K

CONVERSION LATCH

74HCT273 U28: DAB0 3, DAB1 4, DAB2 7, DAB3 8, DAB4 13, DAB5 14, DAB6 17, DAB7 18 → 1D, 2D, 3D, 4D, 5D, 6D, 7D, 8D

1Q 2, 2Q 5, 3Q 6, 4Q 9, 5Q 12, 6Q 15, 7Q 16, 8Q 19 → 0, 1, 2, 3, 4, 5, 6, 7

CLR 1; 11 → +5V

74HCT273 U27: DAB8 3, DAB9 4, DAB10 7, DAB11 8, DAB12 13, DAB13 14, DAB14 17, DAB15 18 → 1D, 2D, 3D, 4D, 5D, 6D, 7D, 8D

1Q 2, 2Q 5, 3Q 6, 4Q 9, 5Q 12, 6Q 15, 7Q 16, 8Q 19 → 8, 9, 10, 11, 12, 13, 14, 15

CLR 1; 11 → +5V

DAC<0: 15> → 1/D7

REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 1/18/89; AF 1/18/89	RWH 1/18/89; DHS 1/18/89
1	RELEASE FOR PILOT	DHS 2/27/89; AF 2/27/89	DHS 2/27/89; DHS 2/27/89
2	RELEASE FOR PRODUCTION	AF 3/1/89; MWH 3/1/89	3/4/89; 3/3/89
3	DELETE C108 PER ECO#891122-01	JV 12/15/89; 12/13/89	12/13/89; 1/5/90

CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE: SCHEMATIC, LXP - 5 LEXICHIP, DRAM	
DRAWN MWH	1/11/89		
CHECKED AF	1/18/89	SIZE: D	CODE:
Q.C. RWH	1/18/89	NUMBER: 060-07316	REV.: 3
ISSUED DHS	1/18/89	SHEET 5 OF 6	

ANALOG DOUBLERS

DIGITAL POWER

C38 .01UF

FB5

FB4

9VAC IN

J4 (1, 2 N/C, 3)

C25 .01UF

C27 1000UF

C28 1000UF

C29 1000UF

CR9 1N4004

CR10 1N4004

C40 1000UF

C90 22UF +7.5V (TO U38 PIN 16)

CR21 1N755

R59 1K 1-4W

C84 22UF -7.5V (TO U38 PIN 7)

CR19 1N755

R58 1K 1-4W

CR12 1N4004

U25 7812 VIN VOUT ADJ +12V

CR13 1N4004

U26 7912 VIN VOUT ADJ -12V

CR11 1N4004

C26 2200UF

C39 2200UF

+5VUNREG

C6, A8, B4, B5

R6 4.7K 1-4W

C5 22UF DGND

CR3 1N914

+4.7V (TO U1 PIN 14)

U24 7805 VIN VOUT ADJ +5V

C106 .1UF

C107 .1UF

SPARES

U40 4570

+5V: C14 .1UF, C3 .1UF, C32 .1UF, C24 .1UF, C30 .1UF, C36 .1UF, C37 .1UF, C47 .1UF, C33 .1UF, C31 .1UF, C15 .1UF, C46 .1UF, C1 .1UF, C19 .1UF, C2 .1UF, C13 .1UF, C23 .1UF

+5V: C7 .1UF, C35 .1UF, C4 .1UF, C18 .1UF, C21 .1UF, C45 .1UF, C20 .1UF, C41 .1UF, C44 .1UF, C6 .1UF

+12V: C60 .1UF, C91 .1UF, C83 .1UF, C76 .1UF, C94 .1UF, C66 .1UF, C101 .1UF, C100 .1UF

+7.5V: C87 .1UF

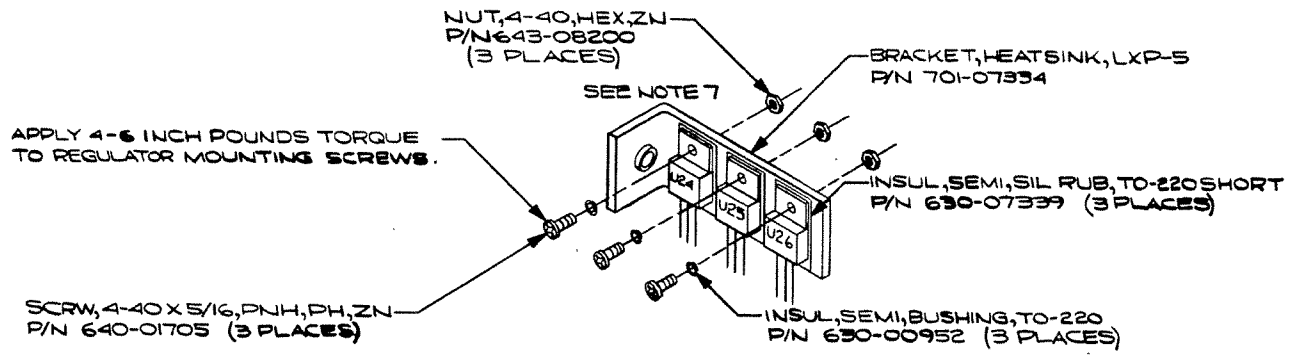
-12V: C88 .1UF, C93 .1UF, C82 .1UF, C65 .1UF, C75 .1UF, C59 .1UF

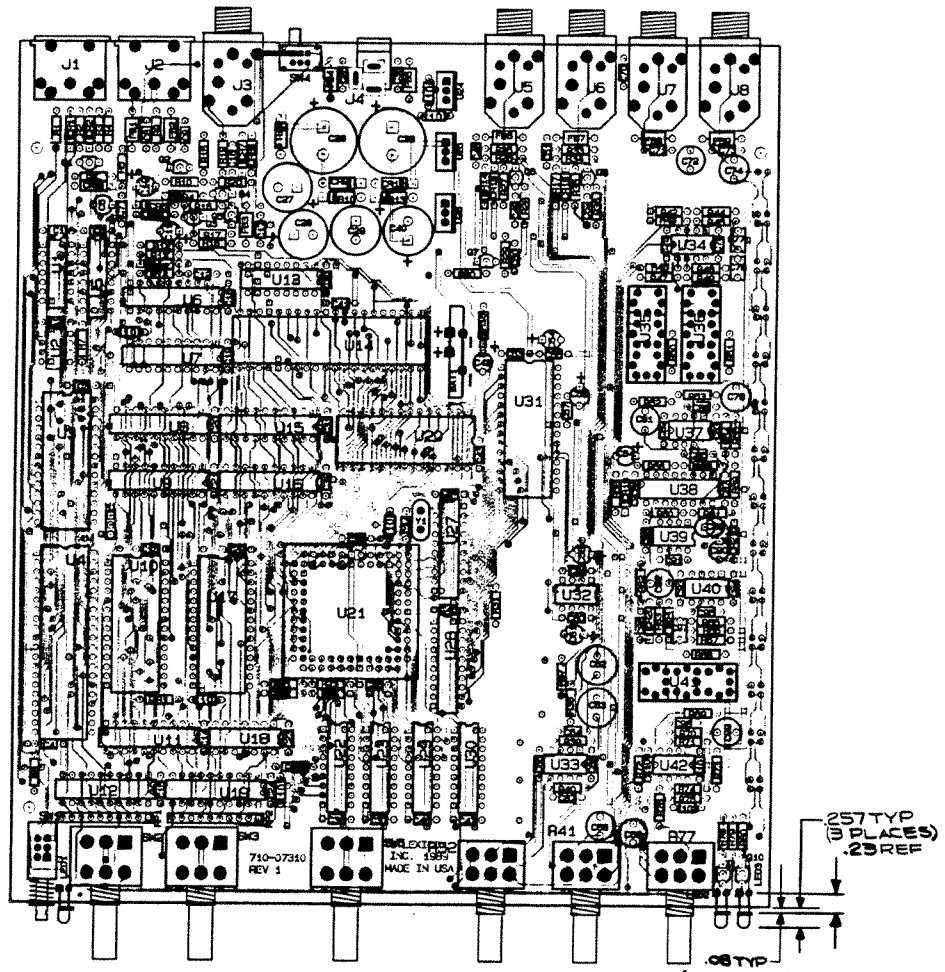
-7.5V: C86 .1UF

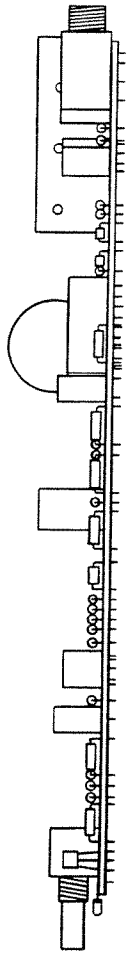
REVISIONS

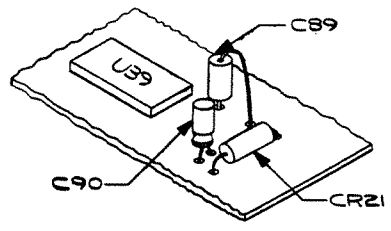
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	MWH 1/18/89	RWH 1/18/89
		AF 1/18/89	DHS 1/18/89
1	RELEASE FOR PILOT	DHS 2/27/89	DHS 2/27/89
		AF 2/27/89	DHS 2/27/89
2	RELEASE FOR PRODUCTION	AF 3/1/89	DHS 3/2/89
		MWH 3/1/89	DHS 3/2/89
3	CHANGED PER ECO#890718-00	J.V. 7/18/89	RWH 7/21/89
		AF 7/20/89	DHS 7/24/89
4	CHANGED J4 SYMBOL PER ECO#900202-02.	J.V. 3/6/90 DHS 3/9/90	CW 3/9/90 DHS 3/14/90

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154				
APPROVALS	DATE	TITLE: SCHEMATIC, LXP - 5 POWER SUPPLY			
DRAWN MWH	1/11/89				
CHECKED AF	1/18/89	SIZE: D	CODE:	NUMBER: 060-07316	REV.: 4
Q.C. RWH	1/18/89				
ISSUED DHS	1/18/89	SHEET 6 OF 6			









REVISIONS			
REV.	DESCRIPTION	DRAFTER/CHECKER	Q.C./AUTH.
0	RELEASE FOR PROTOTYPE	JV 1/11/89 MH 1/16/89	DR 1/18/89 DHS 1/24/89
1	RELEASE FOR PILOT	JV 2/22/89 DHS 2/24/89	LDR 3/3/89 DHS 3/3/89
2	RELEASE FOR PRODUCTION	J.V. 3/3/89 DHS 3/3/89	DHS 3/3/89 LDR 3/3/89
3	CHANGED PER ECO#890309-01	J.V. 3/10/88 DHS 3/3/89	LDR 3/10/89
4	CHANGED PER ECO#890728-00	J.V. 8/9/89 LDR 8/14/89	LDR 8/14/89 DHS 8/17/89

NOTES

1. REFER TO LEXICON BOM NO:025-07308,024-07307,024-07309.
2. ALL COMPONENTS TO BE INSTALLED FROM COMPONENT SIDE OF P.C.B. EXCEPT SWAGED STANDOFFS.
3. MASKING FOR POST-SOLDER ASSEMBLY IS INDICATED BY SOLID AREAS ■ ●
4. COMPONENT HEIGHT .900" MAXIMUM
5. LEAD PROTRUSIONS .080" MAXIMUM FROM CIRCUIT SIDE OF P.C.B.
6. SOCKET IC POSITIONS:U3,4,6,10,11,14,17,20-23,29-31.
7. HEATSINK ASSEMBLY.

	710-07310
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

lexicon

APPROVALS		DATE
DRAWN	JV	1/11/89
CHECKED	MH	1/16/89
Q.C.	LDR	1/18/89
ISSUED	DHS	1/24/89

PC BD, LXP-5
ASSEMBLY DRAWING

SIZE D | FSCM NO. | DWG. NO. 080-07315 | REV 4

SCALE 1:1

SHEET 1 OF 1