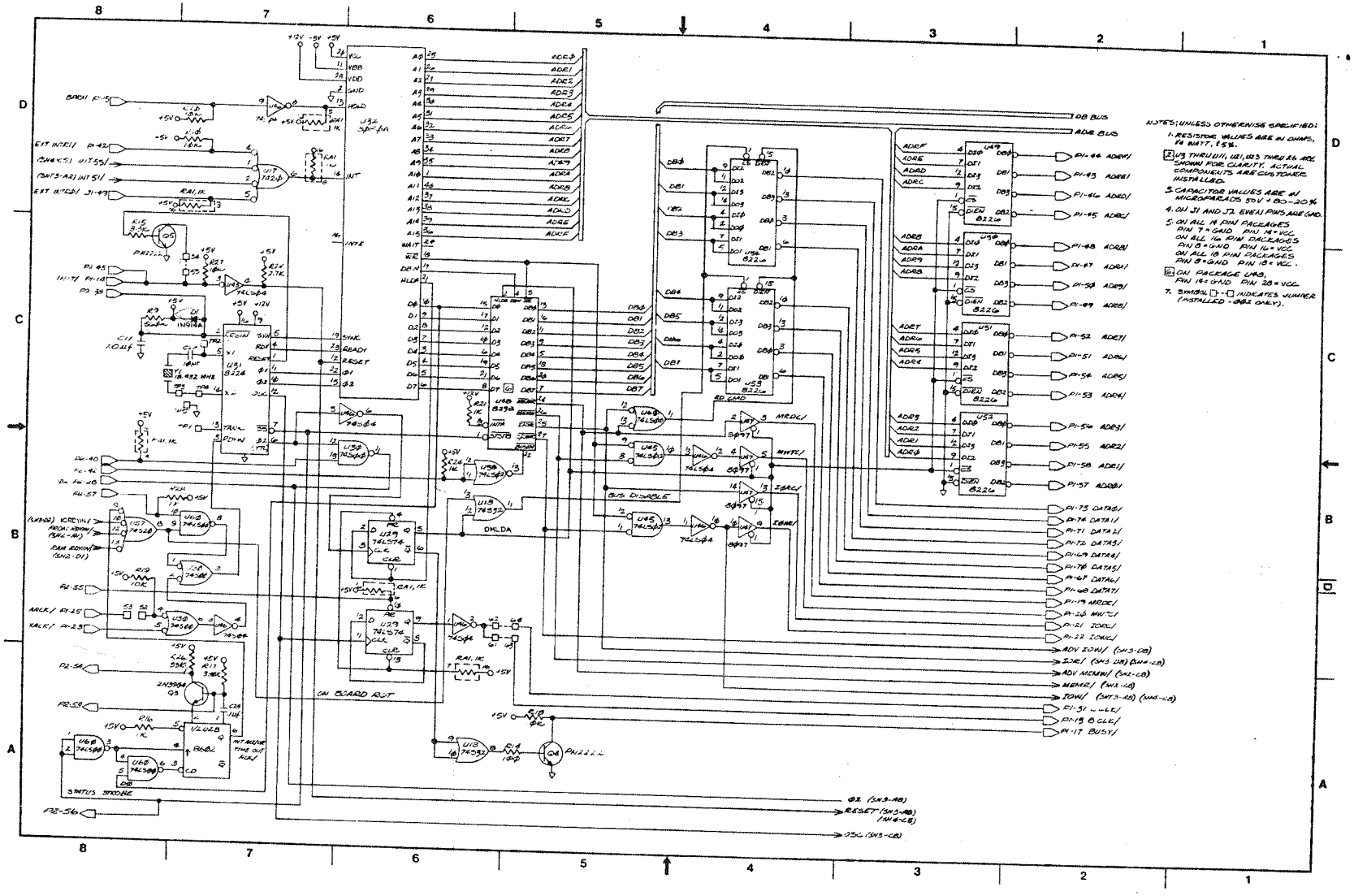
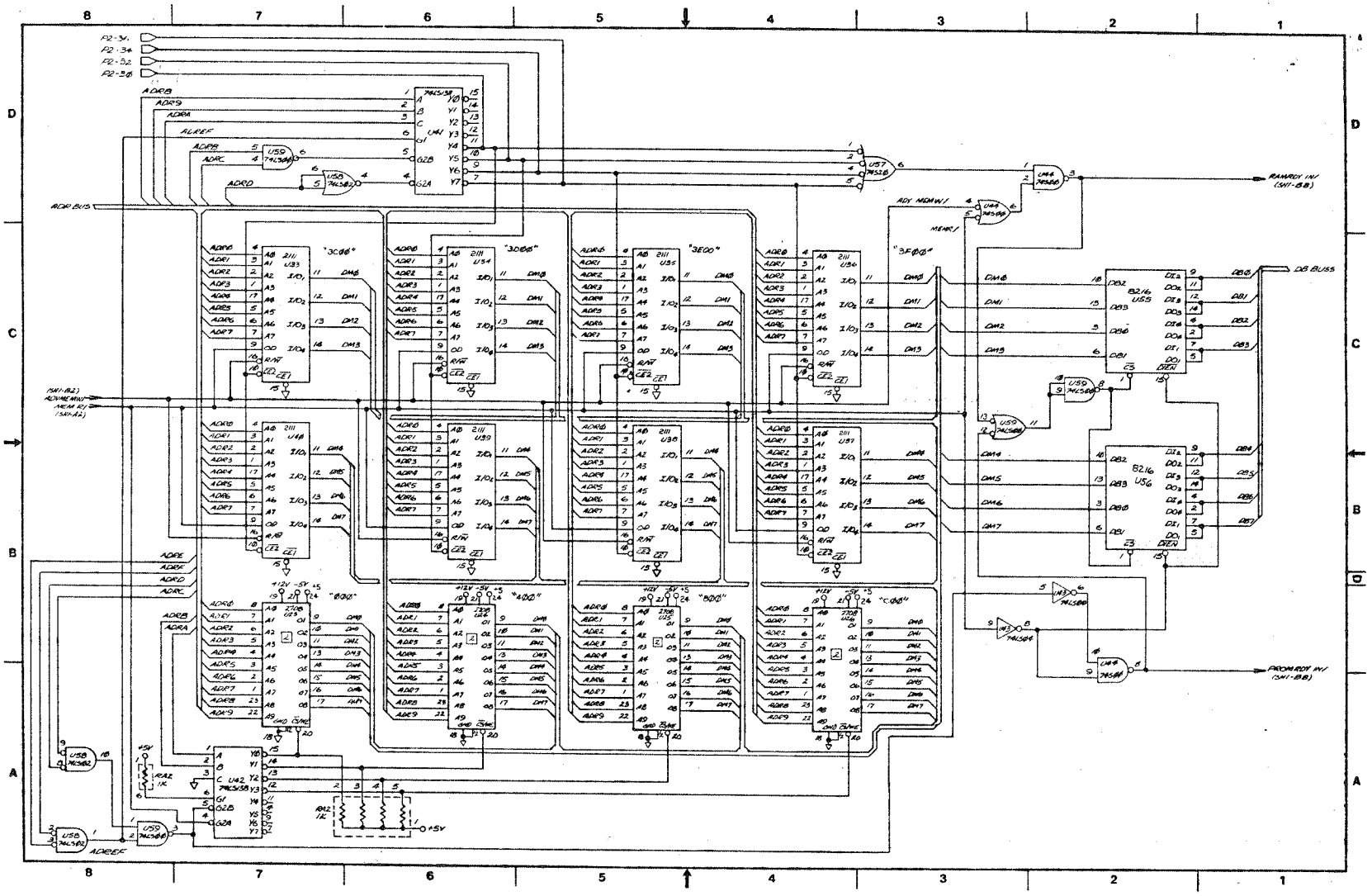
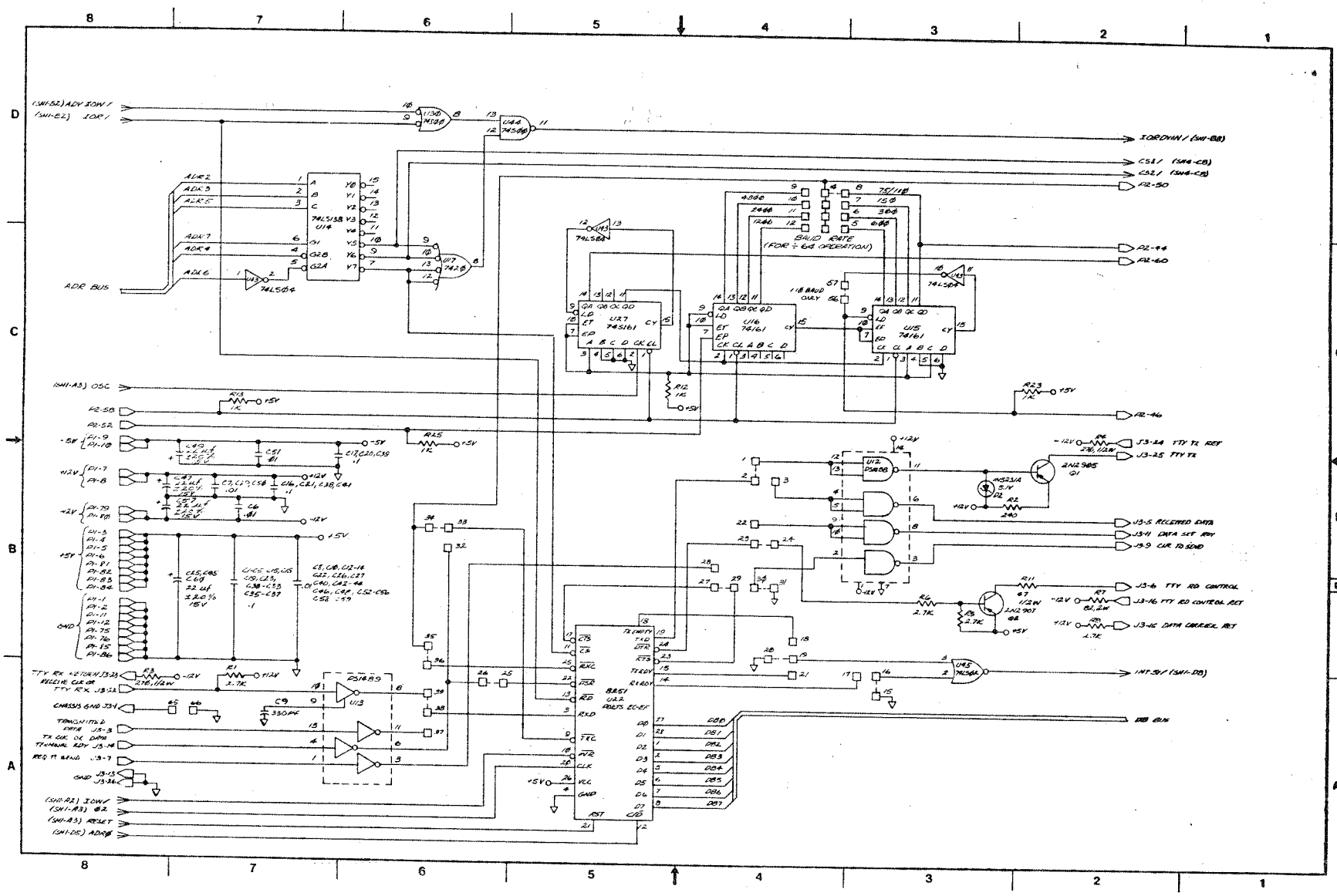


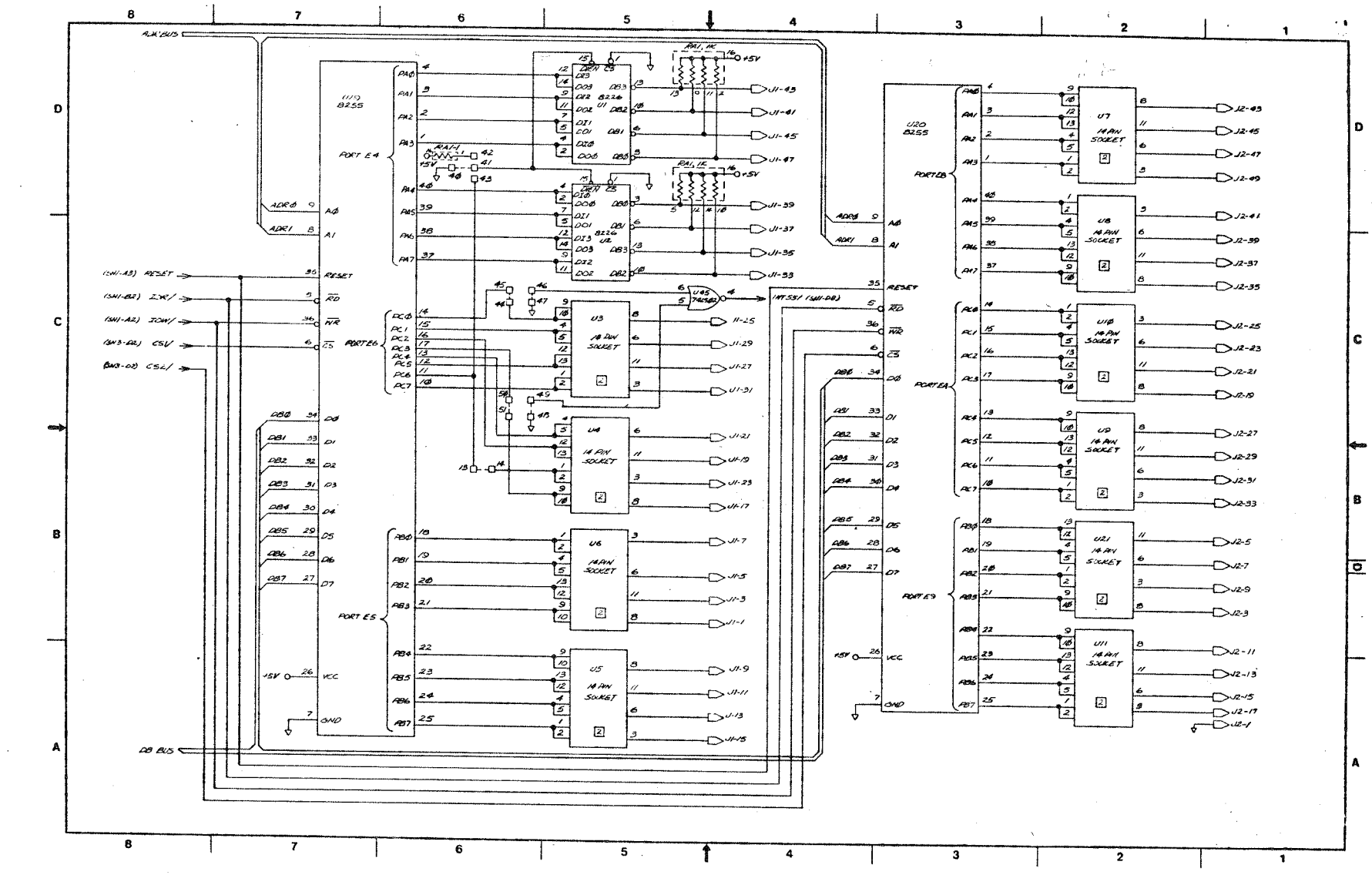
A-1 BLC 80/10 LOGIC DIAGRAM (Sheet 1 of 4)



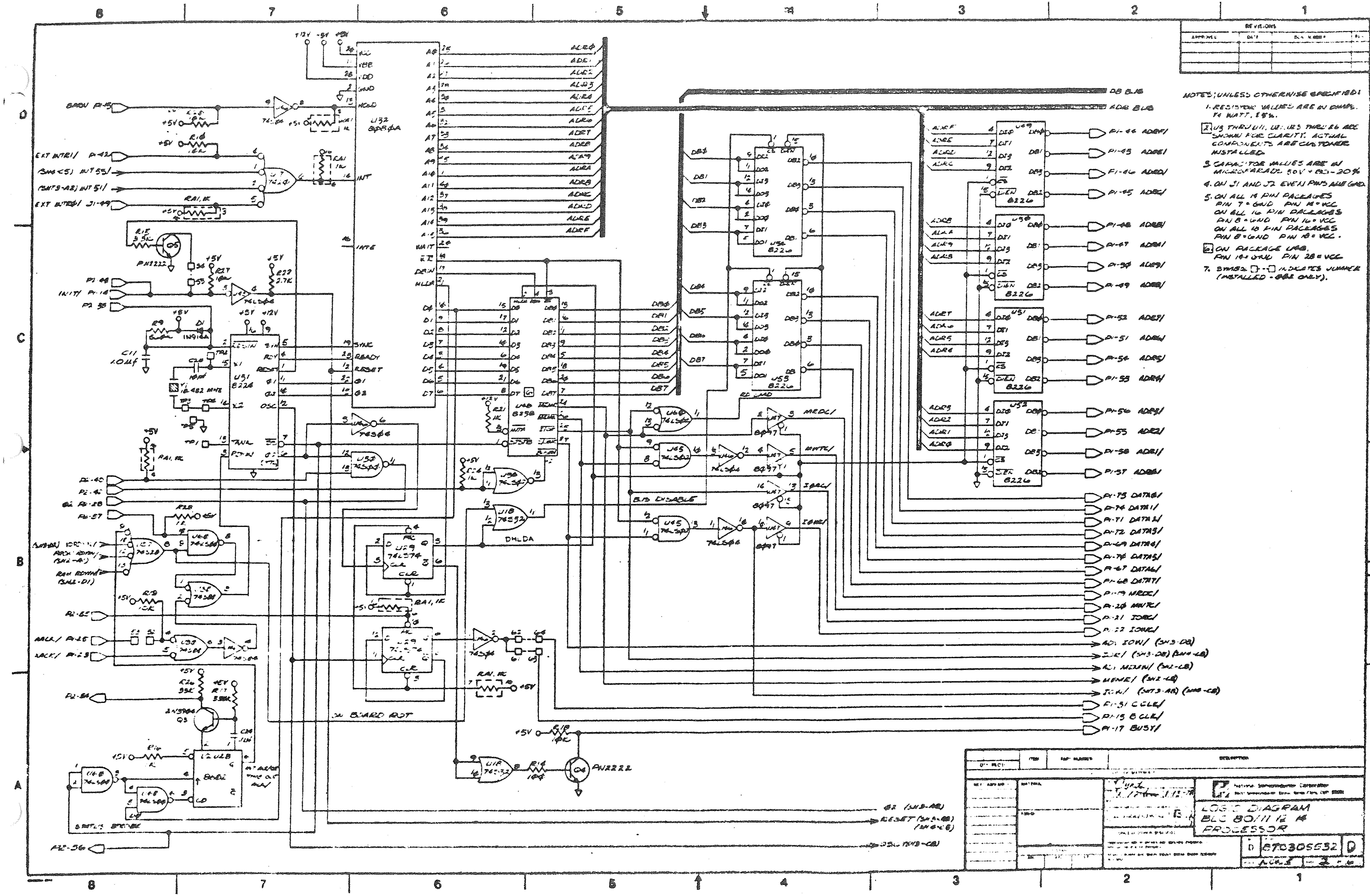
A-2 BLC 80/10 LOGIC DIAGRAM (Sheet 2 of 4)



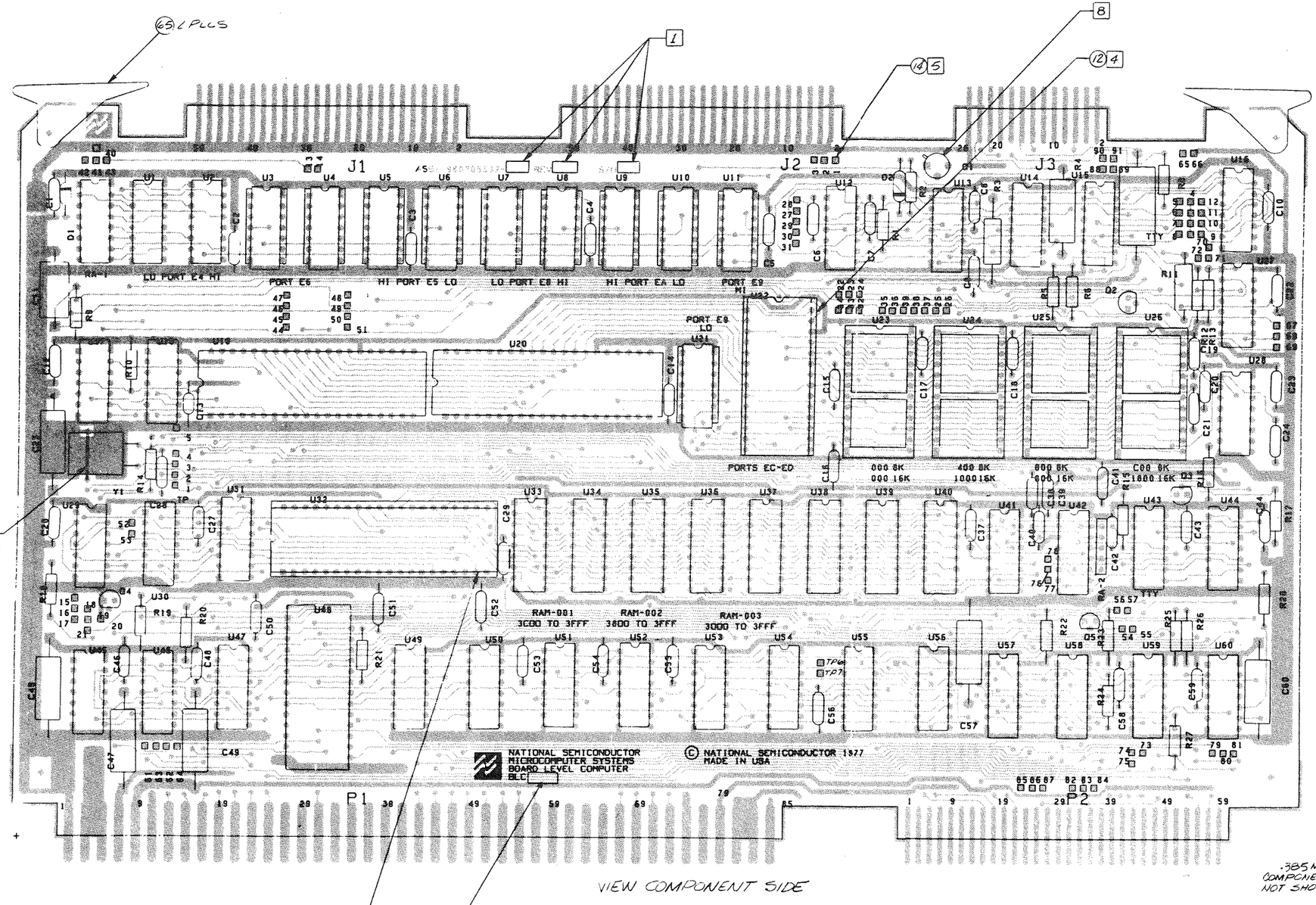
A-3 BLC 80/10 LOGIC DIAGRAM (Sheet 3 of 4)



A-4 BLC 80/10 LOGIC DIAGRAM (Sheet 4 of 4)


NOTES; UNLESS OTHERWISE SPECIFIED:
1. RESISTOR VALUES ARE IN OHMS. 1/4 WATT, ±5%.
2. U8 THRU U11, U21, U23 THRU U26 ARE SHOWN FOR CLARITY. ACTUAL COMPONENTS ARE CUSTOMER INSTALLED
3. CAPACITOR VALUES ARE IN MICROFARADS. 50V +80-20%
4. ON J1 AND J2 EVEN PINS ARE GND.
5. ON ALL 14 PIN PACKAGES PIN 7 = GND PIN 14 = VCC
ON ALL 16 PIN PACKAGES PIN 8 = GND PIN 16 = VCC
ON ALL 18 PIN PACKAGES PIN 9 = GND PIN 18 = VCC.
6. ON PACKAGE U48. PIN 14 = GND PIN 28 = VCC
7. SYMBOL □-□ INDICATES JUMPER (INSTALLED - 80/12 ONLY).
DB BUS
ADR BUS
U32
8080A
U31
8224
U48
8238
8226
74LS04
74LS74
PN2222
2N3904
BUS DISABLE
ON BOARD RQT
DMLDA
P1-33 DATA0/
P1-34 DATA1/
P1-31 DATA2/
P1-32 DATA3/
P1-29 DATA4/
P1-30 DATA5/
P1-27 DATA6/
P1-28 DATA7/
P1-19 MRDC/
P1-20 MWTC/
P1-21 IORC/
P1-22 IOWC/
P1-31 CCLK/
P1-13 BCLK/
P1-17 BUSY/
LOGIC DIAGRAM
BLC 80/11 12 14
PROCESSOR
870305532
D

REVISIONS			
APPROVED	DATE	DCN NUMBER	REV
	11/8/78	PROD SEC 687	A
	3/4/78	DCN # IMP 3001	B
	11/8/78	DCN # IMP 3056	C
	12-15-78	DCN = IMP-3082	D
	1-26-79	DCN = IMP-3106	D1



1 MARK APPLICABLE DASH NO., REV LEVEL AND S/N .12-.18 HIGH CHARACTERS APPROX. AS SHOWN.

2. LOCATION NO./REF DESIGNATIONS SHOWN FOR REF ONLY

3. FOR LOGIC DIAGRAM SEE DWG NO. 8703055532.

4. INSTALL SOCKET (ITEMS 10 & 12) BEFORE INSTALLING U22 & U32.

5. WIRE WRAP PINS ARE STAKED INTO BOARD (93 PLCS) IN LOCATIONS 1-31 AND TP1-7.

6. INSTALL ITEM #64 (#22 GA WIRE) WHERE SHOWN.

7. INSTALL JUMPERS (ITEM) BETWEEN WIRE WRAP PINS AS SHOWN IN APPROPRIATE TABLE BELOW (32 PLCS) INSTALL WHERE INDICATED BY □.

8. INSTALL PAD (ITEM 63) UNDER Q1 WHERE SHOWN.

JUMPER INSTALLATION -001, -004
1K RAM 2708 PROM 2308 ROM

TO	FROM	TO	FROM	TO	FROM	TO	FROM
1	2	30	31	50	51	76	77
4	8	33	34	54	55	80	81
13	14	35	36	56	57	83	84
15	16	38	39	61	63	86	87
19	20	40	41	62	64	88	89
23	24	44	45	68	69	90	91
25	26	46	47	71	72	TP3	TP4
27	29	48	49	74	75	TP6	TP7

JUMPER INSTALLATION -002, -005
2K RAM 2708 PROM 2308 ROM

TO	FROM	TO	FROM	TO	FROM	TO	FROM
1	2	30	31	50	51	76	77
4	5	33	34	54	55	80	81
13	14	35	36	56	57	82	83
15	16	38	39	61	63	86	87
19	20	40	41	62	64	88	89
23	24	44	45	68	69	90	91
25	26	46	47	71	72	TP3	TP4
27	29	48	49	74	75	TP6	TP7

JUMPER INSTALLATION -003, -006
4K RAM 2708 PROM 2308 ROM

TO	FROM	TO	FROM	TO	FROM	TO	FROM
1	2	30	31	50	51	76	77
4	8	33	34	54	55	79	80
13	14	35	36	56	57	82	83
15	16	38	39	61	63	85	86
19	20	40	41	62	64	88	89
23	24	44	45	68	69	90	91
25	26	46	47	71	72	TP3	TP4
27	29	48	49	74	75	TP6	TP7

ROM/PROM JUMPER INSTALLATION
2385, 2708 2316/2716

FROM	TO	FROM	TO	FROM	TO	FROM	TO
69	59	76	75	67	68	73	74
71	72	78	77	70	71	78	78

9 MARK APPLICABLE MARKETING NUMBER IN .12-.18 HIGH CHARACTERS APPROX. AS SHOWN:

80/11 FOR -001 VERSION
80/12 FOR -002 VERSION
80/14 FOR -003 VERSION
80/11T FOR -004 VERSION
80/12T FOR -005 VERSION
80/14T FOR -006 VERSION

MATERIAL

FINISH

TOLERANCE
ANG | 3 PL | 3 PL

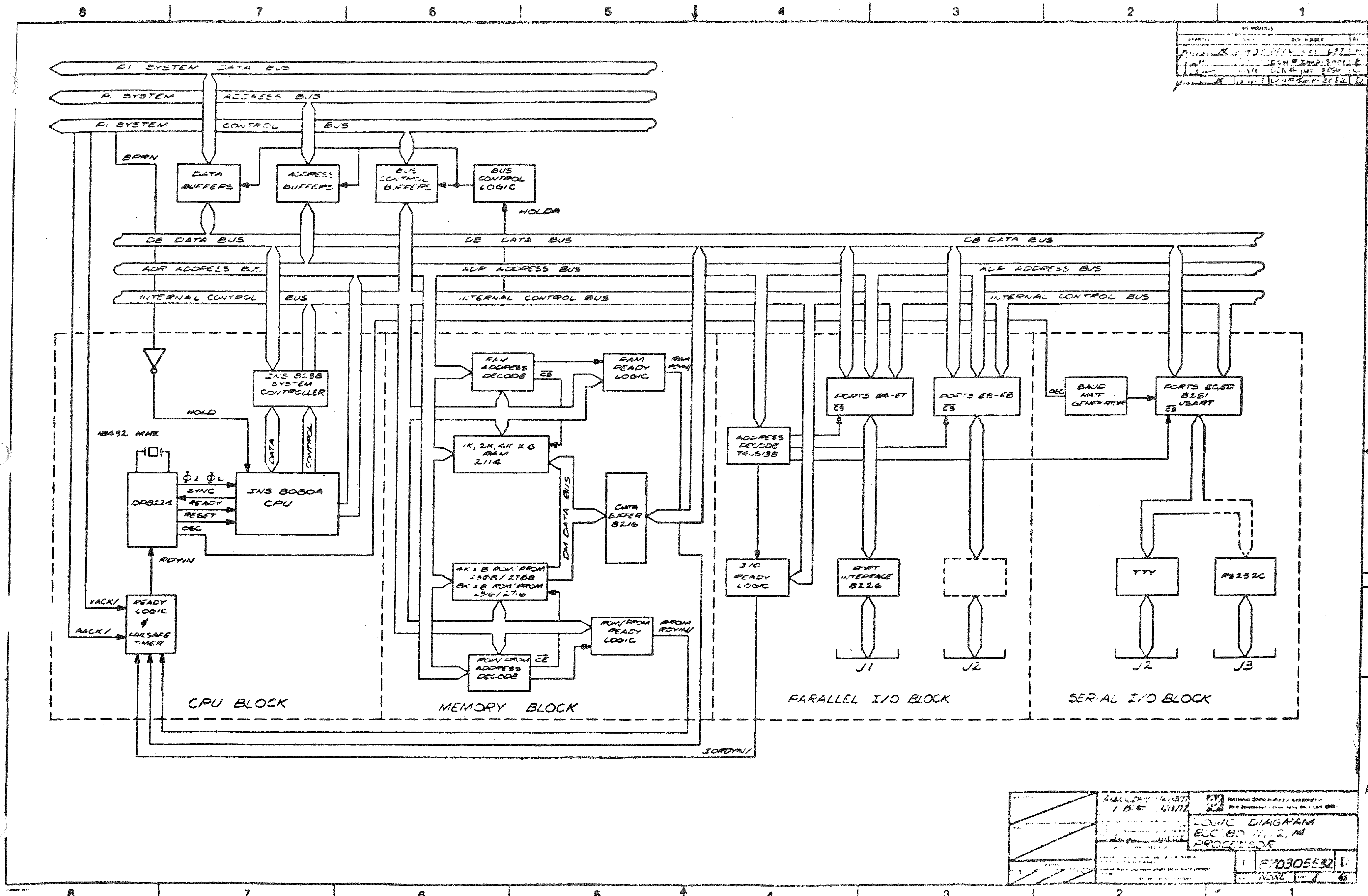
DR BY 1-13-78
CHK BY 1-13-78
M E
E E
P E
UNLESS OTHER SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX
DO NOT SCALE DRAWING

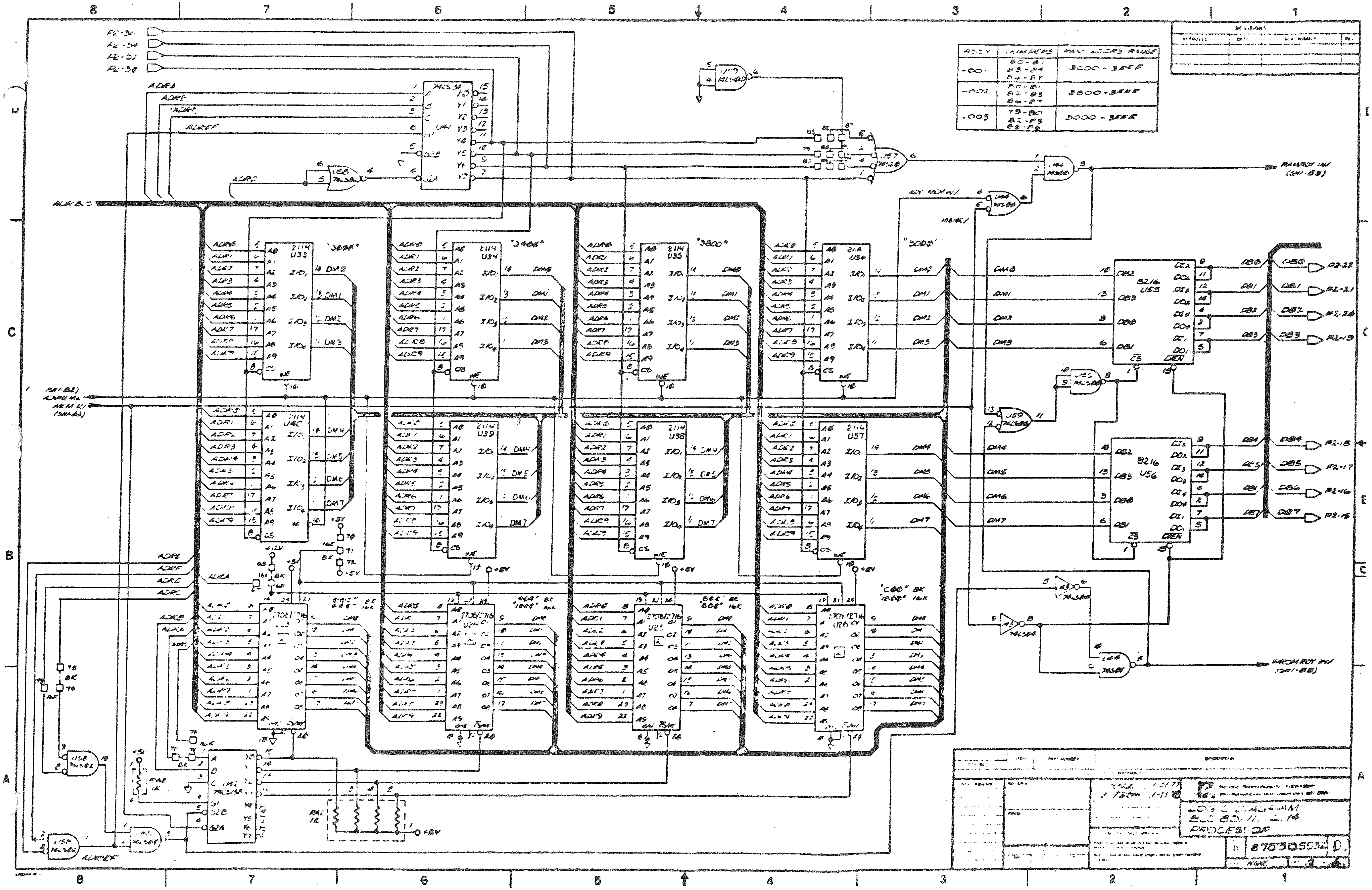
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

PWA
BLC 80/11, 12, 14

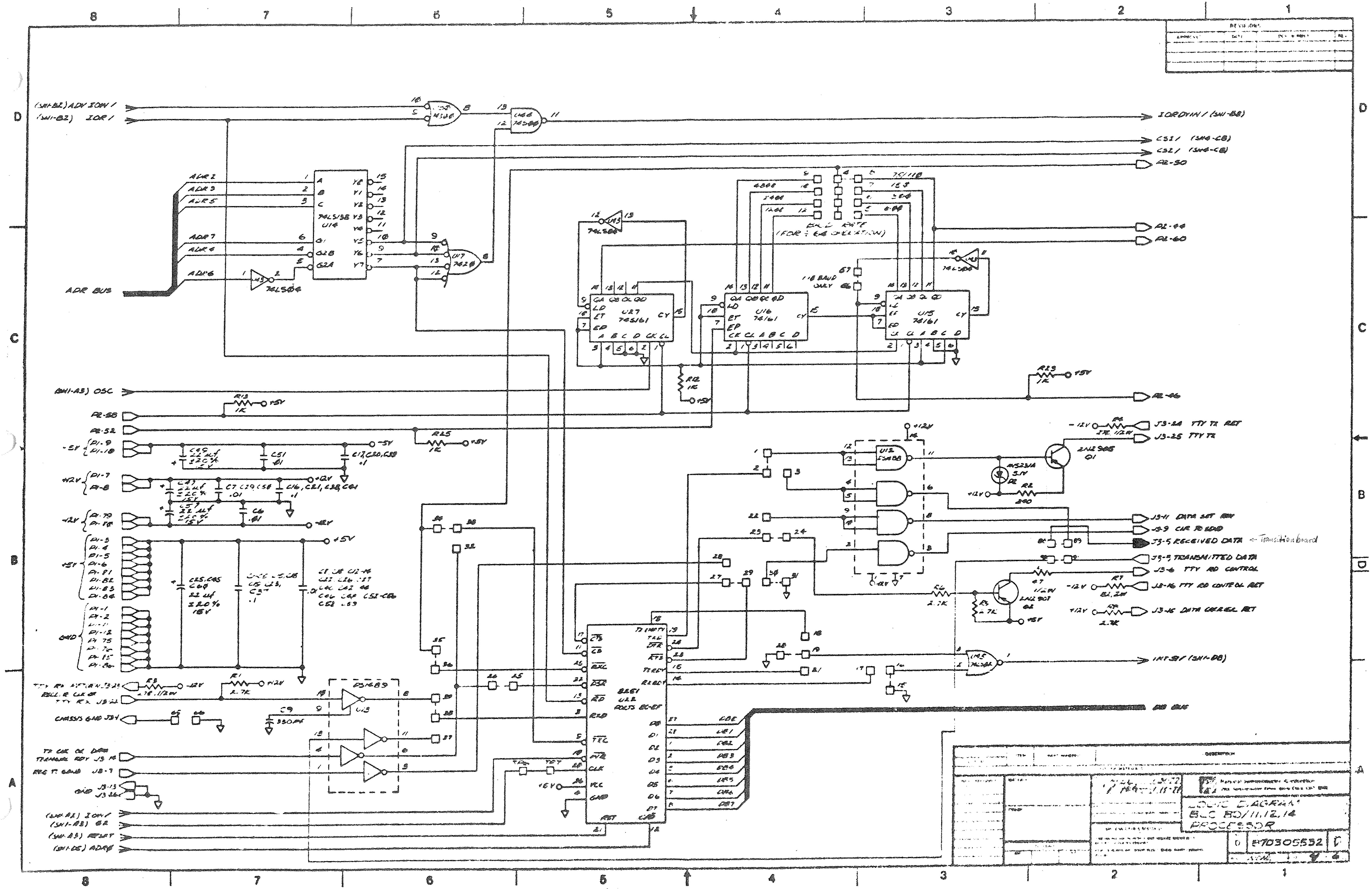
SIZE D | DR NO 8703055532 | D
SCALE | SHEET 1 OF 1

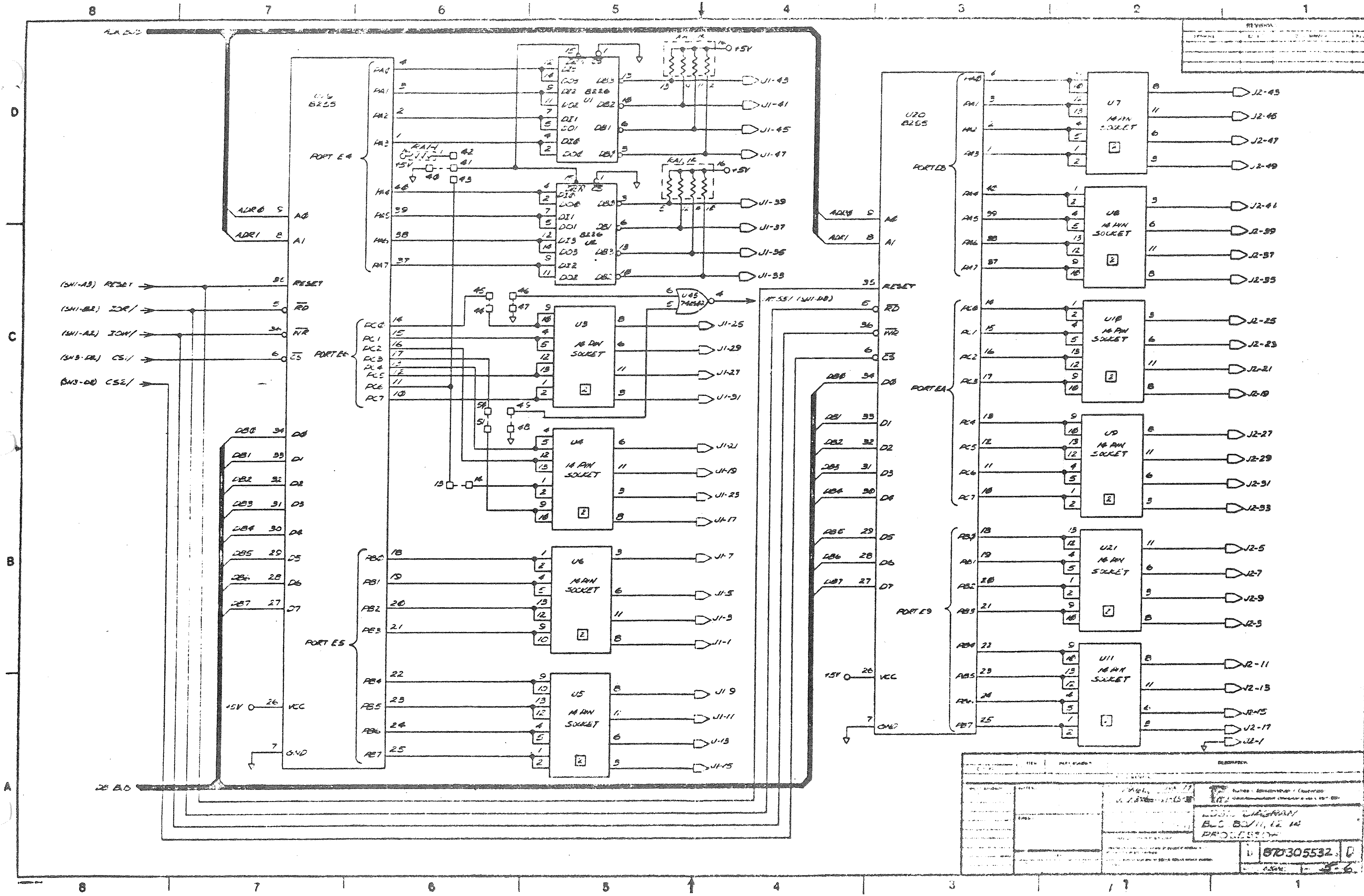


SYSTEM DATA BUS
SYSTEM ADDRESS BUS
SYSTEM CONTROL BUS
BPRN
DATA BUFFERS
ADDRESS BUFFERS
BUS CONTROL BUFFERS
BUS CONTROL LOGIC
HOLDA
DB DATA BUS
ADR ADDRESS BUS
INTERNAL CONTROL BUS
INS 8238 SYSTEM CONTROLLER
HOLD
18432 MHZ
DATA
CONTROL
DP8224
INS 8080A CPU
SYNC
READY
RESET
OSC
RDYIN
XACK/
AACK/
READY LOGIC & FAILSAFE TIMER
CPU BLOCK
RAM ADDRESS DECODE
RAM READY LOGIC
1K, 2K, 4K X 8 RAM 2114
DM DATA BUS
DATA BUFFER 8216
ROM/PROM READY LOGIC
ROM/PROM ADDRESS DECODE
MEMORY BLOCK
ADDRESS DECODE 74LS138
I/O READY LOGIC
PORTS E4-E7
PORTS E8-EB
PORT INTERFACE 8226
J1
J2
PARALLEL I/O BLOCK
BAUD RATE GENERATOR
PORTS EC,ED 8251 USART
TTY
RS232C
J3
SERIAL I/O BLOCK
IORDYIN/
LOGIC DIAGRAM
PROCESSOR
870305532



P2-36
P2-34
P2-32
P2-30
ADRB
ADRF
ADRD
ADREF
ADRC
U41
U58
U57
U44
U59
U65
U63
U55
U56
8216
2114
U33
U34
U35
U36
U40
U39
U38
U37
"3C00"
"3400"
"3800"
"3C00"
2708/2716
U23
U24
U25
U26
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
P2-22
P2-21
P2-20
P2-19
P2-18
P2-17
P2-16
P2-15
RAMRDY INV (SH1-B8)
PROMRDY INV (SH1-B8)
ADR MEMW/
MEMR/
ASSY | JUMPERS | RAM ADDRS RANGE
-001 | 80-81 83-84 86-87 | 3C00-3FFF
-002 | 80-81 82-85 86-87 | 3800-3FFF
-003 | 79-80 82-85 86-89 | 3000-3FFF
LOGIC DIAGRAM
ELC 80/11, 14
PROCESSOR
8703055


(SH1-B2) ADV IOW/
(SH1-B2) IOR/
IORDYIN/ (SH1-B8)
CS1/ (SH6-C8)
CS2/ (SH6-C8)
ADR BUS
74LS138
U14
74LS04
74LS161
74161
BAUD RATE
(FOR ÷ 64 OPERATION)
(SH1-A3) OSC
8251
U12
DB BUS
INT-S1/ (SH1-B8)
J3-24 TTY TX RET
J3-25 TTY TX
2N2905
Q1
J3-11 DATA SET RDY
J3-9 CLR TO SEND
J3-5 RECEIVED DATA
J3-5 TRANSMITTED DATA
J3-6 TTY RD CONTROL
J3-16 TTY RD CONTROL RET
J3-16 DATA CARRIER RET
2N2907
Q2
DS1489
U13
CHASSIS GND J3-Y
(SH1-A2) IOW/
(SH1-A3) RESET
(SH1-D5) ADR0
LOGIC DIAGRAM
BLC 80/11,12,14
PROCESSOR
P70305532


U20
8255
8226
PORT E4
PORT E6
PORT E5
PORT E8
PORT EA
PORT E9
14 PIN SOCKET
RESET
28 B.B
+5V
870305532