5 TROUBLESHOOTING

5.1 Overall Approach

A through visual inspection of the 224X and control head is good general troubleshooting practice. Check for any obvious component failures, such as burnt or overheated parts or damaged PC board traces. There should be no loose ICs, connectors, or cables. Observe whether the malfunction is intermittent, heat related, or shock related.

Figure 5.1 shows a flow chart for troubleshooting problems in the Model 224X. As can be seen, the power-up software diagnostics are an important tool in the troubleshooting process. One of the first things to do is to see whether the unit can run the power-up diagnostics. If these diagnostics do not run, the problem probably is in the power supply module, the SBC module, or the remote control head. (Note that the power-up diagnostics will run with only these three modules in the unit.) First look at the power supplies, then check the cable to the control head. If the problem is with the control head or the connecting cable, and the mainframe is functional, the unit will eventually run one of the reverberation/effects programs (after running the power-up diagnostics), with the remote control head disconnected.

If the unit can run the power-up diagnostics, the diagnostic error codes it produces often supply some information about the nature of the malfunction. Note that the power-up diagnostics test only the digital signal processor (DSP) circuitry, that is, the NVS, SBC, DMEM, T&C, and ARU modules. Although the power-up diagnostics are thorough, they do not test these modules completely. Also, with noise-related or intermittent problems, the power-up diagnostics may not catch an error. Thus, if the unit passes power-up diagnostics, but the reverberation/effects programs sound bad, the DSP may have problems that are not diagnosed by the power-up diagnostics, or the analog conversion system, that is, the FPC, AIN, and AOUT modules, may have problems.

Furthermore, it is possible for the reverberation/effects programs to sound OK and the unit to fail power-up diagnostics. Possibly, the diagnostic hardware or a low-order bit may be malfunctioning. In any case, these kinds of problems should be pursued.

The analog conversion system can be tested on its own through a self-test procedure. Self-test is accomplished by removing the DSP, NVS, DMEM, T&C, and ARU modules. The SBC module is retained to generate a clock signal. If the unit works in the self-test mode, the problem is likely to lie with the DSP.

The 224X has several other diagnostic programs available to help when troubleshooting problems. These programs are called by pushing one of the eight program pushbuttons at the beginning of the power-up diagnostics. The diagnostic programs are listed in Table 5.1.

The first diagnostic programs to run are a maximum delay (0.5-sec) program (diagnostic program 8) and a zero delay program (diagnostic program 7).

These delay programs are similar, except that the maximum delay program uses the DMEM module and the zero delay program does not. Thus, if the unit works in the zero delay program, but not in the maximum delay program, the problem is probably in the DMEM module. These two programs also help in exercising the digital-to-analog interface that is not tested in the self-test mode and in diagnosing where a problem is in the analog conversion system. (Note that the self-test mode does not run at the correct sampling rate when the SBC module is used to generate the clock signal.)

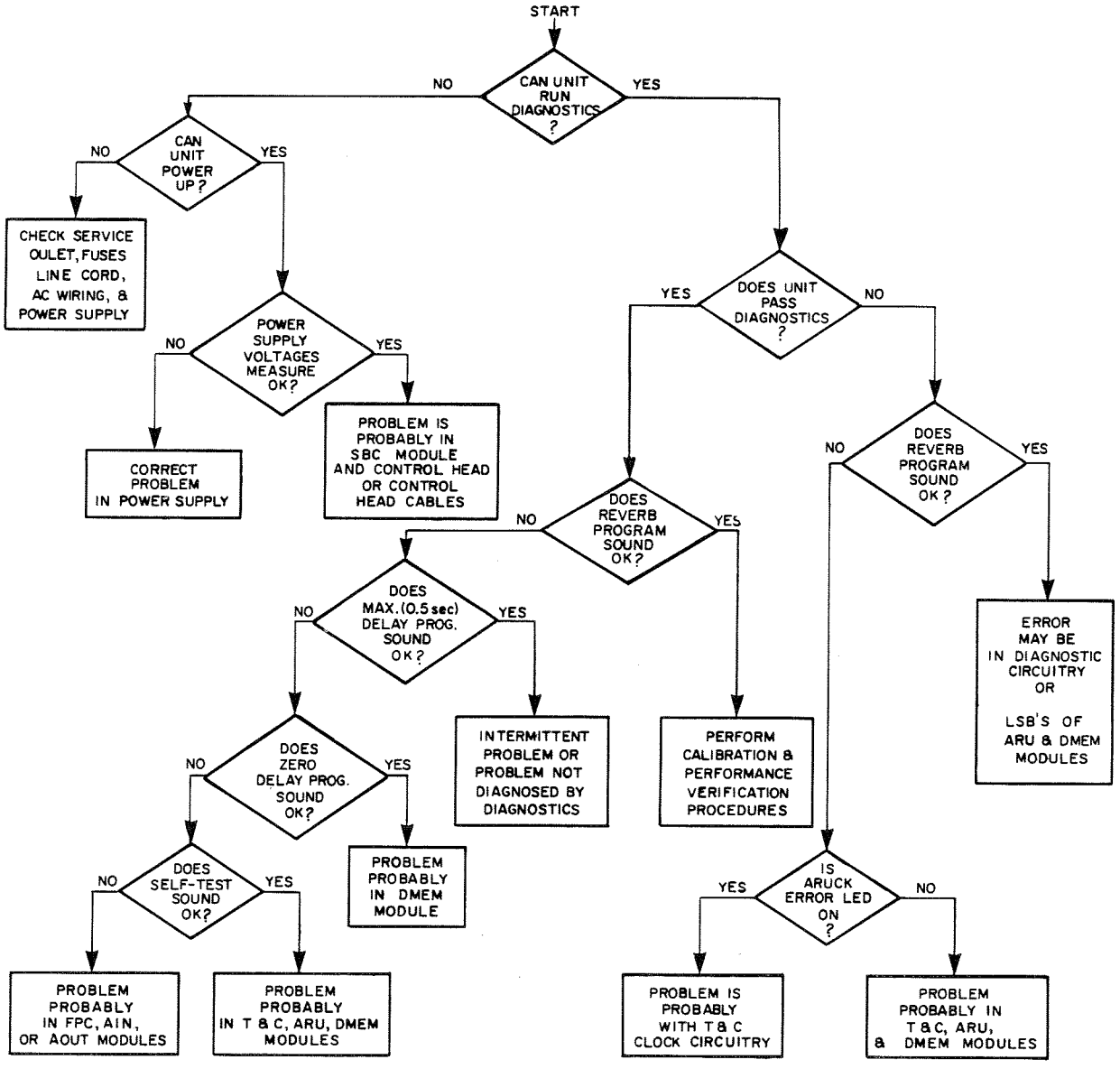


Fig. 5.1. Troubleshooting Approach.

Table 5.1. Diagnostic Programs.

Program*	Description
1 RESTART	restarts self-testing power-up diagnostics and returns to normal operation
2 QUICK EXIT	exits directly to normal operation
3 ARU SIGNAT	generates signature analysis signals; for use by service personnel to test the ARU module
4 ARU TEST	runs a quick test of the ARU module and returns to menu
5 NVS STROBE	generates analysis signals; to test the NVS module
6 FPC SIGNAT	generates signature analysis signals; to test the FPC module
7 ZERO DELAY	loads a 0-second delay-line program for setting input and output levels; Left input passes to outputs A and D, and Right input passes to outputs B and C
8 MAX DELAY	loads a 0.5-second delay-line program for setting input and output levels; Left input passes to outputs A and D, and Right input passes to outputs B and C

*Programs 3, 4, 5, 6, and 7 are not implemented in V8.0 software.

The ARU test (diagnostic 4) exercises the ARU module more thoroughly than the power-up diagnostics and can be tried when the unit passes power-up diagnostics but the ARU is still suspected to be bad. The NVS strobe program (diagnostic 5) continuously sends signals to the NVS module so that they can be checked with an oscilloscope. In addition, two signature programs (diagnostics 3 and 6) can be used with signature analyzers for troubleshooting some of the modules. The signature programs are also useful in troubleshooting with oscilloscopes, because they provide simplified and more observable signals to the various modules.

5.2 Power Supplies

If the 224X does not power up, first check the ac line cord for a good connection and the service outlet for power. Next check the power fuse at the rear of the mainframe. If the fuse is blown, replace with an exact replacement fuse: 3AG 3A slow blow for 100/120 Vac operation, 3AG 1.5A slow blow for 220/240 Vac operation.

The 224X mainframe has a 10-Vac unregulated power supply (ac-fused), three pairs of ac-fused regulated power supplies, and one dc-fused regulated power supply. A blown internal fuse generally indicates a problem in the related power supply circuitry, which should be thoroughly checked out.

Table 5.2 lists the power supply fuses. Replacement fuses should always have the correct rating to ensure protection from circuit damage or fire. Table 5.3 shows the location of each of the power supplies.

Table 5.2. Power Supplies and Fuses.

Schematic Fuse No.	Fuse Board Designation	Power Supply Fusing	Fuse Rating
F1, F2	±15 V	±15 Vac Secondary	2 A slow blow
F3, F4	±12 V	±12 Vac Secondary	3 A slow blow
F5	Viso	+10 Vac Secondary	2 A slow blow
F6, F7	±5 V	±5 Vac Secondary	15 A slow blow
F8	-5 Vdc	-5 Vdc	2.5 A slow blow

Table 5.3. Location of Power Supplies.

Power Supply	Output Supply Voltage/Current Rating	Location	
		Rectified/ Filtered	Regulated
+15 V	+15 Vdc/750 mA	PS2	PS2
-15 V	-15 Vdc/750 mA	PS2	PS2
+12 V	+12 Vdc/1.25 A	PS3	PS2
-12 V	-12 Vdc/150 mA	PS3	PS3
+10 Viso	+5 Vdc/500 mA	Control Head	Control Head
+5 V	+5 Vdc/10 A	PS1	PS3
-5 V	-5 Vdc/250 mA	PS1	PS3

The first test of any faulty operation is to make sure all power supplies are working properly.

5.3 Power-up Diagnostics

The 224X diagnostic programs test many components of the digital hardware. Although a diagnostic routine may not point out the exact component that has failed, a faulty module or section can usually be isolated. Diagnostic error messages are easier to understand if you are familiar with the overall operation of the 224X and the hexadecimal numbering system.

Table 5.4 shows number conversion between decimal, hexadecimal, and binary numbering systems. Figure 5.2 shows how errors and correct data are displayed on the control head.

Table 5.4. Number System Conversion.

Decimal	Hex	Binary
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111
16	10	0001 0000
.	.	.
.	.	.
.	.	.
255	FF	1111 1111

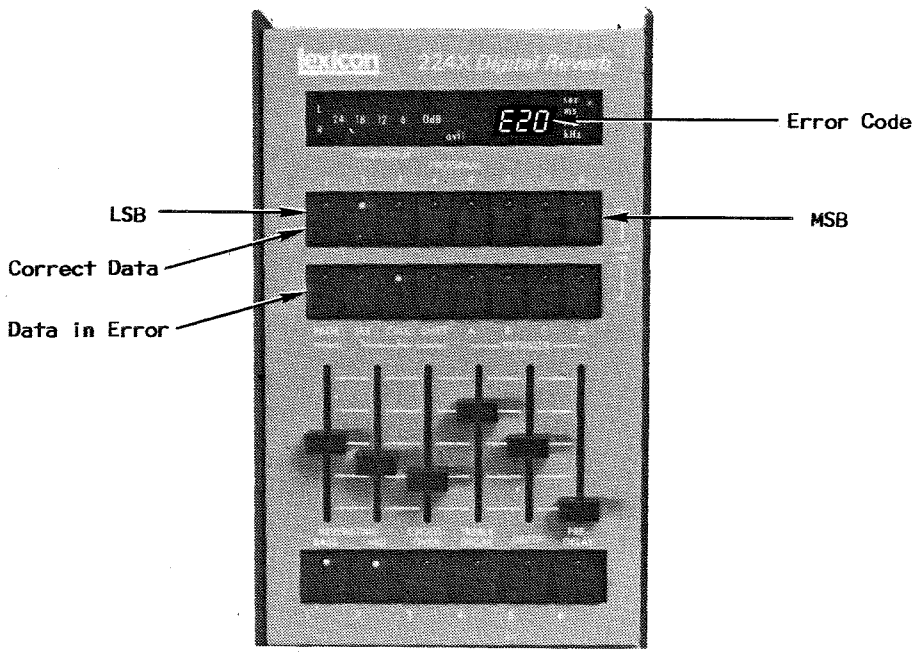


Fig. 5.2. Control Head Error Display.

The 224X diagnostic programs are run whenever the machine is turned on or reset. They can also be run by holding the SHIFT key while pushing CALL and PROGRAM 1 (SHIFT/CALL/PGM 1). The diagnostics make a single pass through all testable features of the machine. If the 224X passes all tests, normal operation begins. If an error is detected, an error message is displayed.

The diagnostic sequence varies for the nonvolatile storage (NVS) module, depending on how the diagnostics are started. When the diagnostics are started by powering up or resetting the 224X, a checksum test is performed on all ROMs on the NVS module, but the nonvolatile RAM is not tested because data can be lost if the power becomes unstable during testing. When the key sequence CALL/SHIFT/PGM 1 is used to start the diagnostics, testing of the nonvolatile RAM on the NVS module is included in the diagnostic program sequence. When the NVS module's nonvolatile RAM is tested, the contents are loaded into the RAM on the SBC module and reloaded to the NVS module when the test is finished. This procedure ensures that registers are not lost as a result of testing.

Caution: Do not reset or power down the unit while the NVS diagnostic is in progress; otherwise contents of the NVS registers may be lost.

During a diagnostic test, or when an error is displayed, all controls and pushbuttons on the control head, except the PROGRAM pushbuttons, are inactive. Briefly pushing PGM 1 allows the unit to go to the next diagnostic test after an error display. Pushing PGM 2 bypasses all further diagnostics and starts normal system operation. Pushing PGM 7 calls a zero delay test program and pushing PGM 8 calls a maximum delay test program.

The diagnostic programs compare the actual data in one part of the machine to the data that should be there if the machine were working perfectly. The diagnostic programs display the expected data pattern (the good data) using the LEDs on the PROGRAM pushbuttons. If different from the expected data pattern, the pattern of the actual data resident in the machine is displayed using the mode/register pushbutton LEDs. Usually an error is displayed when the two data patterns do not agree. The patterns displayed by these LEDs are essential in determining the cause of error. If errors appear, the error message numbers and the lighting patterns of the LEDs should be noted in the order of occurrence when diagnosing or referring a problem to Lexicon service technicians. Table 5.5 is a summary of the 224X error codes, Sec. 5.3.1 describes in detail how to run the programs during troubleshooting, and Sec. 5.3.2 gives in-depth descriptions of the error codes.

Table 5.5. Summary of 224X Error Codes.

Error Type*	Cause of Error
E0X	SBC ROM checksum
E1X	SBC RAM
E2X, E3X, E4X	T&C (may also be DMEM)
E5X - E8X	ARU (may also be T&C or DMEM)
E91, E92, E95, E96	DMEM
H0X, H2X	NVS ROM checksum
H1X	NVS RAM
H2F, H10	NVS card missing

* Where X is from 0 to 9 or from A to F.

5.3.1 Running the diagnostics

The 224X diagnostic programs are run in a particular order. In general, if the diagnostics indicate an error, the source of the first error should be found before much time is spent on any others. The checksum and microprocessor tests come first. Errors here may not disrupt the reverberation or effects programs and are easy to interpret. The remaining diagnostics work by loading the T&C module with a simple program and testing the effects of the program on the machine. The microprocessor must communicate with the T&C module to perform these tests. Failure to communicate usually results in an E23 error, which means that either the timing is incorrect between the T&C module and the microprocessor or a memory chip on the T&C module is faulty. The T&C module has a single LED diagnostic indicator labeled ARUCK ERROR. If this LED lights, the timing signal ARUCK (ARU Clock) is missing, indicating a failure within the clock circuitry on the T&C module. Because the entire machine depends on the T&C module, any problem on this module generally gives errors in other diagnostic tests, even if other sections are not faulty.

Some parts of the tests cannot be easily separated. All tests of the DMEM module require that the ARU module work at least minimally. Most of the microprocessor communication and test circuits for both the T&C and ARU modules are on the DMEM module. A failure here may cause the T&C test to take a long time to complete and may also cause an unusual flashing pattern of the LEDs on the control head. In addition, a short circuit or defective IC on the ARU or FPC modules can cause an error that appears to be on the T&C module. It is sometimes useful to unplug the ARU and FPC modules to see if the error still occurs. The FPC module is not testable by the microprocessor, and the machine should pass all diagnostics with the FPC module unplugged.

If the machine does not appear to work at all, the cable to the control head should be checked first. If no diagnostic errors occur, the machine will eventually run the sonic ambience programs with the control head unplugged. If so, the control head or the cable is faulty. However, it is more likely that a transformer plug in the power supply has come loose, or that a power supply fuse has opened. See Sec. 5.2 for the power supply test points. Failure of the machine to respond with either diagnostics or reverb programs when the power supplies are good probably means that the SBC module is faulty.

5.3.2 Descriptions of error codes

E00 through E0F: SBC ROM checksum test. Each ROM in the SBC module is checked by adding all data bytes; if the data is correct, the sum is 0. If an error is detected, one of the error messages E00 through E0F is displayed, depending on which ROM is faulty. The least-significant hexadecimal digit of the error code represents an encoded nibble (4-bit quantity) binary value. Within that binary value, the bit positions corresponding to a logic 1 identify which chip numbers are faulty. ROM 1 (U23) is indicated by a binary equivalent of 1, ROMs 2 and 3 are both indicated by a binary equivalent of 6, etc., for example:

Error Message	Binary Representation	Faulty ROM*
E01	0001	1
E02	0010	2
E06	0110	2 and 3
E0F	1111	1, 2, 3, and 4
E0A	1010	2 and 4

*ROM 1 = U23, 2 = U25, 3 = U24, and 4 = U26

Note that a checksum error does not always result in a noticeable machine malfunction.

E10 through E13: SBC module RAM test. The RAM on the SBC module is tested using a semirandom pattern, altering all contents. Errors are indicated by display of one of the error messages E10 to E13, depending on the address of the incorrect byte; for example, E10 corresponds to hexadecimal addresses 3C00 to 3CFF and E11 corresponds to addresses 3D00 to 3DFF. The correct pattern is displayed on the Program LEDs, and any incorrect pattern is displayed on the mode/register LEDs. The bit positions corresponding to the elements of the patterns that do not match isolate the location of the error. The error messages and bit patterns are defined as follows:

Error Messages

E10 = RAM addresses 3C00-3CFF
E11 = RAM addresses 3D00-3DFF
E12 = RAM addresses 3E00-3EFF
E13 = RAM addresses 3F00-3FFF

Bit Patterns

	LSB* 1	2	3	4	5	6	7	MSB 8	
PROGRAM LEDs	0	0	0	0	0	0	0	0	Correct Data
Mode LEDs	0	0	0	0	0	0	0	0	Incorrect Data
Bit No.	0	1	2	3	4	5	6	7	(Bits 0 to 3 are in U36 of the SBC module and bits 4 to 7 are in U37)

*LSB = least significant bit; MSB = most significant bit

The test is accomplished in two passes. First, the memory is loaded with the contents of ROM 1, starting from location zero. This data is complemented twice in two separate passes. The data in RAM is then compared with the original data in ROM. (Data is read from the top down.) The test will stop as soon as any error has been detected. This RAM test is sensitive to addressing errors and data errors.

Control Head Display Test. The panel test outputs data to the control head to light all LEDs (except the 7-segment displays, which display the revision number of the resident software). The test is bypassed if PROGRAM 1 is pushed. The control head display should blank out after the panel test for about 10 to 15 seconds, while the unit is performing diagnostics. Failure of the DMEM and T&C modules to return a ready signal to the SBC module causes the writable control store (WCS) memory test to require more than a minute to complete. If the 224X is not initialized after several minutes, the protect circuitry on the T&C module may be locking the 8080 on the SBC in a hold state. This condition means that the HALT decoding circuitry on the DMEM module or the protect gating on the T&C module is faulty.

E20 through E23: Writable Control Store (WCS) memory test. The WCS (U3, U18, U33, U48, and associated circuits on the T&C module) are tested in the same way as the RAM on the SBC module is tested. The error codes, E20 to E23, are as follows:

Error Message	Hexadecimal Address	Component
E20	4000, 4004 ... 41FC	U49 & associated circuits
E21	4001, 4005 ... 41FD	U33 & associated circuits
E22	4002, 4006 ... 41FE	U18 & associated circuits
E23	4003, 4007 ... 41FF	U3 & associated circuits

Correct data is displayed on the program LEDs, and faulty data is displayed on the mode/register LEDs. Error message E23 could mean that the entire program memory is faulty. If so, or if a problem on the DMEM module prevents data from being properly loaded into the program memory, the memory test will take a long time to complete. Such a delay indicates faults in the SBC bus-decoding checks in the DMEM module or on the T&C module. Two of the memory chips can be swapped to see if different error messages are displayed. Other problems, such as open or shorted address lines, or defective address or data buffers, can also cause a faulty program memory. The diagnostics detect such problems, but require additional steps to isolate them.

E32: 8080 bus test register test. If an error is found when checking the contents of the 8080 bus test register, the 8080 microprocessor in the SBC module cannot communicate with the DSP (consisting of the T&C, ARU, and DMEM modules). If an actual system error occurs, as opposed to a fault in the diagnostic test, it will seriously affect proper operation of further diagnostics as well as the reverberation and effects programs. Short circuits on the T&C or DMEM modules may be the cause. Check to see if the error occurs with the T&C module unplugged. If so, the DMEM module, the Backplane, or the SBC module is faulty. If the reverberation or effects programs seem to be running properly, the bus test register itself (U34 on the DMEM module) is faulty, and the error can be ignored, because it will not interfere with the proper operation of the reverberation and effects programs in the machine.

E40 & E41: Halt and single-step mode tests. Both the halt and single-step mode tests display an error if the return data matches, indicating the halt state cannot be initiated. Because the first program step is continually repeated in the halt state and many tests load known data into the first program step and look for that data at the output of the T&C module, it is necessary to be able to initiate the halt state for subsequent diagnostics to be valid. The halt test works by loading an instruction in the second executable address of the WCS memory. This instruction transfers data from the input of the XREG to the output, and a value loaded into the XREG is checked against the value output. If a halt condition has occurred within the 224X, the values will be different. If no halt has occurred, the values will be identical.

E43: XREG read/write test. The ability of the DSP to read correctly from and write correctly to the transfer register (XREG) on the DMEM module is tested. The WCS memory is first loaded with a NOP and then with an instruction to read the XREG and write to it. If the DSP cannot execute these functions, it means either a faulty XREG itself, or incorrect decoding of the bus control bits of the T&C module. It is important that these errors be corrected before further diagnostics are run, because incorrect XREG contents may invalidate results in all subsequent tests. This error may indicate short circuits or faulty chips at any location along the DAB (digital audio bus). The ARU and FPC modules may be unplugged to be sure they do not contribute to this error. If the same error code is still given, the problem is probably with the transfer registers themselves (U38, U39, U40, and U41 on the DMEM module).

E51 to E7F: ARU register test. All four ARU registers are tested. The registers are composed of four 16-bit memory chips, with each chip organized into four rows of nibbles (4-bit quantities). The first row of chips 1, 2, 3, and 4 constitute the 16 bits of register 1, with chips 1 and 2 containing the higher-order byte of the register and chips 3 and 4 containing the lower-order byte. The second row of the four chips constitutes register 2, the third row register 3, and the fourth row register 4.

Error messages E51 to E5F indicate one or both of the chips comprising the lower-order byte of a register is faulty, E61 to E6F indicate a faulty chip or chips in the higher-order byte of a register, and E71 to E7F indicate chips in both bytes are faulty. The registers are identified by the least-significant hexadecimal digit of the error code. This represents an encoded nibble value. The positions of the bits in a logic 1 state in the binary representation of the nibble value indicate which registers are faulty. For example, the 5 in error code E51 represents a lower-order byte of a register and the 1 corresponds to a binary representation of 0001, indicating an error in register 1. The 9 in E59 corresponds to a binary code of 1001, indicating an error in registers 1 and 4, the 3 in E53 corresponds to 0011, indicating an error in registers 1 and 2, and the 4 in E54 corresponds to 0100, indicating an error in register 3, etc. The following chart shows an example. Incorrect bits within a register are displayed by the mode/register pushbutton LEDs.

ARU register decoding

Error Message	Address Bytes	Binary Code of LSD	Register Number
E67	high	0111	1, 2, and 3
E52	low	0010	2
E69	high	1001	1 and 4
E75	high and low	0101	1 and 3
E7B	high and low	1011	1, 2, and 4

2.8. E54 → U29
E52 → U32

To understand the significance of these diagnostics, examine the following conditions:

1. The multiplier is OK, but the registers are faulty.

   a. If both high and low bytes are faulty, register addressing is probably invalid. This condition could result in an error in some registers and not in others.

   b. If a register file chip is faulty, only one byte is affected, and only part of that byte. This may affect all addresses or just one. The data on the LEDs must be checked to determine which chip is actually faulty.

2. The registers are OK, but the multiplier is faulty.

   All file addresses are incorrect, and this may propagate errors to areas that are not faulty, so that just replacing the faulty chip does not correct the errors.

E80 to E8F: Multiplier test. The multiplier test is divided into four parts, each of which displays separate error codes. E81 to E83 indicate an error when the multiply coefficient is ±21/32. E81 indicates a low-order byte error, E82 a high-order byte error, and E83 indicates both bytes are incorrect. E85 to E87 indicate an error when multiplying by ±42/32. E89 to E8B indicate an error in the coefficient ±63/64. Four multiplications are made with each coefficient. The incorrect and correct data are displayed on the pushbutton LEDs in the same way as previous tests. If both the high-order and low-order bytes are incorrect, the data in the low-order byte is displayed. The last two coefficients should set the saturation monostable multivibrator. If not, error code E80 is displayed.

Note that E89 to E8B will test the intermediate address. Therefore, if E89 to E8B is displayed, check U13, U24 to U25, and U38 and U39.

E91, E92, E95, and E96: data memory test. This test makes two passes with complementary data. For this test to be valid, the multiplier must be operating correctly. Error message E91 indicates a low-order byte error and E92 indicates a high-order byte error. If both bytes are incorrect, E91 is displayed, which may mean that the entire memory is faulty, or it may mean that the multiplier or T&C module is faulty. The memory test is sensitive to both data errors and addressing errors, and should detect most problems. If either E91 or E92 are the only errors displayed and only a single LED indicates incorrect data, the problem is most likely to be a faulty memory chip, which is identified by the pushbutton LED. The defective memory chip can be swapped with the lowest-order memory chip (U1). This increases the noise level of the machine by 6 dB, but allows immediate operation if needed. For units with two banks of 16K dynamic RAMs. E91 and E92 refer to bank 1 (U20 to U35), and E95 and E96 refer to bank 2 (U1 to U16).

EA0 to EB3: Additional Multiplier Test. This test is performed when diagnostic program 4 (not available in V8.0) is called. Even error codes indicate a problem with the low byte and the odd error codes indicate a problem with the high byte. The error codes are grouped in fours; in any group, the first two groups use even test data and the second two use odd test data. EA0 to EA3 test a multiply by 1. EA4 to EA7 test a multiply by 1/2. EA8 to EAB test a multiply by -1. EAC to EAF test a multiply by 1/4. EB0 to EB3 test a multiply by 5/4.

If EA0 to EA3 all appear, the coefficients into the 74LS00 (U14, U26 to U28, U40 and U41, and U50 to U53) should be checked. If the high byte is bad with the bad data reading hexadecimal 80 or 7F, check the saturation logic (U42) or the MSB's of the data path through the ARU. If EA0 to EA3 appear, but EA4 to EA7 do not, check the 74LS00's or the intermediate adder (U13, U24, U25, U38, and U39). If EA0 to EA7 appear but EA8 to EAB

do not, check the 74S86's (U5 to U9). EAC to EAF test the shift registers (U3, U4, and U15 to U18) and coefficients. EB0 to EB3 test the second adders (U19 to U23).

5.4 Maximum Delay (0.5-sec) Program

The 224X's maximum delay diagnostic program is stereo and can be used as an abbreviated machine test (or for setting output levels). This program can be called during normal operation by the key sequence CALL/SHIFT/PGM 2, or by pressing PGM 8 at the beginning of the power-up diagnostics. The nonadjustable delay provided by this program is approximately half a second. In this program, the left input is passed to outputs A and D; and the right input is passed to outputs B and C.

5.5 Zero Delay Program

The zero delay program is similar to the maximum delay program except that the DMEM module is not used and the delay is zero; that is, the analog inputs are immediately transmitted to the analog outputs. (The digitized signals still pass through the ARU module, however.) This program is called by pushing PGM 7 at the beginning of the power-up diagnostics. In this program, the left input is passed to outputs A and D; and the right input is passed to outputs B and C. The zero delay program is recommended for troubleshooting the analog circuitry and also for setting input and output levels.

5.6 Self-Test Mode

If operating difficulties arise, it is possible to determine proper operation of the AIN, AOUT, and FPC modules by performing a self-test. This test usually isolates problems in the analog conversion subsystem. To perform the self-test, loosen the DMEM, T&C, ARU, and NVS modules. When these modules are removed from the motherboard, a control signal (FPC DBUG) to the FPC module goes HIGH, initiating self-test mode. Do not remove the DMEM, T&C, ARU, and NVS modules when you loosen them; just free them from their edge connectors. If there is no response of any kind in self-test mode, check the power supplies and connections, as well as the clock on the SBC module. Then perform a stage-by-stage investigation from the AIN to the AOUT module to determine where the problem is.

The self-test allows the 224X analog and digitizing subsystems to operate without any intervention from the DSP. This mode digitizes analog information from the left input, and outputs the information to outputs A and B; the right channel input is passed to outputs C and D. Note that the signal routing is different than that in both the maximum delay and zero delay programs. This can sometimes help in determining which channel is bad in a malfunctioning AIN or AOUT module. For example, if the output B is bad in self-test but good in the zero delay program, then the left input channel is bad. If output B is bad in both self-test and zero delay program, then probably the B output channel is bad.

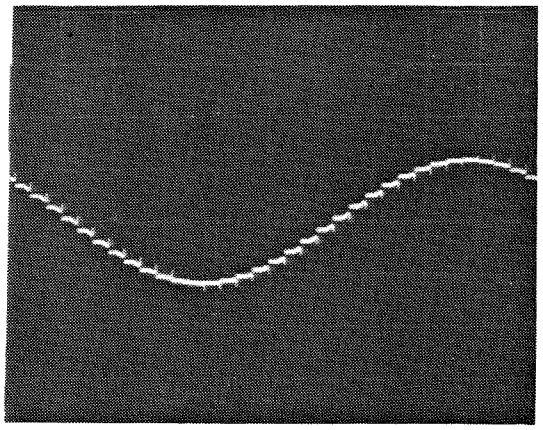
The digital sampling rate in the self-test is only 20 kHz. Therefore, when using the self-test, do NOT use input signals above 10 kHz. The self-test mode samples at only 20 kHz; therefore, it is meant for a preliminary check of the operation of the FPC, AIN, and AOUT modules. If measurements and calibrations are necessary, the zero delay program should be used. The self-test mode can also be exercised at the proper sampling rate of 34.13 kHz by removing the SBC module also and injecting a 3.413-MHz TTL level compatible clock from an external signal generator to pin A28 at the backplane connector for the SBC module. The self-test mode exercises about 95% of the circuitry in the AIN and AOUT modules and about 85% of the circuitry in the FPC module.

5.7 Signature Analysis

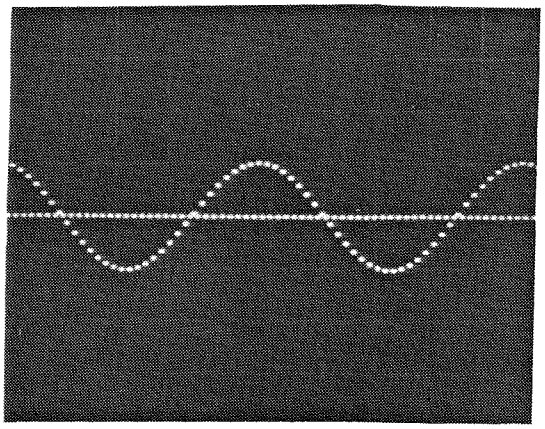
Because the digital signals on the digital modules in the 224X can be quite complex, signature analysis tables have been provided as a useful aid in tracing problems to a malfunctioning node.

Signature analysis is a technique used to troubleshoot electronic logic circuits. A signature analyzer (Hewlett Packard 5004A or equivalent) is connected to the unit being tested and the test program of the unit being tested is started. Long, complex data stream patterns are compressed into a unique 4-segment "signature" that the analyzer will display for each point in the unit being tested as the analyzer probe is moved from point to point. The analyzer requires several signals from the unit under test: the clock signal synchronizes the analyzer and the unit under test; the start and stop signals define the bounds between which the data signal is examined by the analyzer. After the stop signal, the analyzer displays the signature of the data it received. If the signature displayed does not match the corresponding signature given in the table, the circuitry connected to the node is malfunctioning.

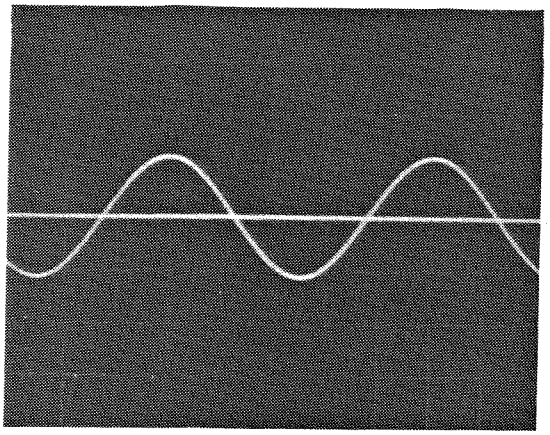
The correct signatures for the various modules in the 224X are summarized in the signature tables that follow. The conditions for taking the signatures are listed with each module and setup. Figure 5.3 shows what some of the waveforms should look like.



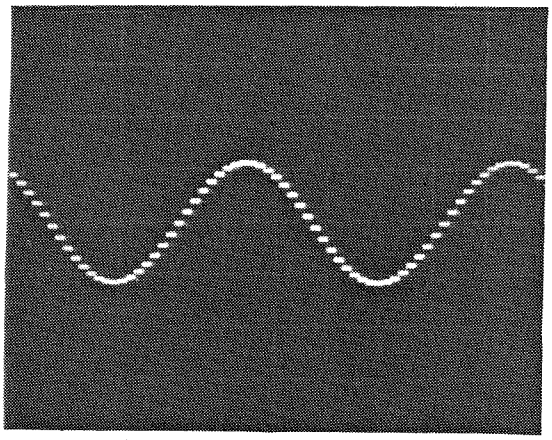
U21 pin 5, AIN board (AGR)
(output of input S/H)
2 V/DIV., 0.1 ms/DIV.
1 kHz input



U22 pin 4, AIN board
(output of channel MUX)
2 V/DIV., 0.2 ms/DIV.
1 kHz input



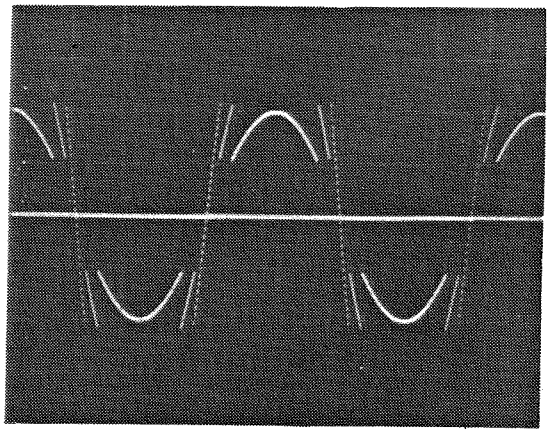
U4 pin 6, AOUT board
(output of output gain range amplifier)
2 V/DIV., 0.2 ms/DIV.
1 kHz input



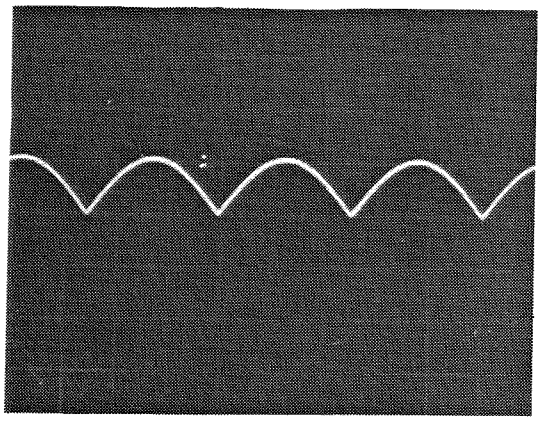
U8 pin 1, AOUT board
(output of output S/H)
2 V/DIV., 0.2 ms/DIV.
1 kHz input

These waveforms are observed with the unit in zero delay program. Input signal level is +12 dBm to the left input channel; input level potentiometer is set so that the level indicator is just beneath overload.

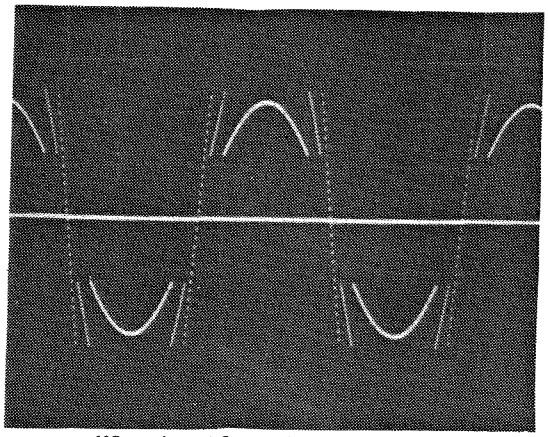
Fig. 5.3. Converter Waveforms.



U23 pin 6, AIN board
(output of input gain range amplifier)
2 V/DIV., 0.2 ms/DIV.
100 Hz input



U12 pin 7, AIN board
output of gain range rectifier)
2 V/DIV., 0.2 ms/DIV.
1 kHz input



U2 pin 18, AOUT board
(output of DAC)
2 V/DIV., 2 ms/DIV.
100 Hz input

These waveforms are observed with the unit in zero delay program. Input signal level is +12 dBm to the left input channel; input level potentiometer is set so that the level indicator is just beneath overload.

Fig. 5.3 (cont'd.). Converter Waveforms.