Operator/Service Manual

Digital Audio Delay Synchronizer

Model 1300

lexicon

NOTICE

Lexicon, Inc., reserves the right to make improvements at any time and without notice in the product described in this manual.

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1 INTRODUCTION

1.1 Description

The Lexicon Model 1300/S Digital Audio Delay Synchronizer is a high-performance 16-bit PCM digital delay line optimized for broadcast applications.

The 1300 provides time delay of audio signals. The amount of time delay can be set manually or determined automatically through sensing circuitry in a plug-in control module or a combination of manual and automatic modes. The 1300 converts audio input signals into a digital format that is continuously written into memory and then read out at the required delay time. Four memory options are available with maximum delays of up to 4096 milliseconds for mono units (Model 1300) and 2048 milliseconds for stereo units (Model 1300S).

The front-panel controls are designed for optimum efficiency, with an easily understood layout. The construction used in the 1300 guarantees long, trouble-free operation and provides maximum protection; Euro-DIN gold-contact connectors are used throughout. To facilitate servicing, all analog/digital conversion circuitry is on an easily removable module.

1.2 Specifications

General Performance

Frequency Response
- 20 Hz to 20 kHz, +0.5dB, -1 dB
- 20 Hz to 18 kHz, ±0.5 dB

Distortion
- <0.02% @ 1-kHz limit level (+24 dBm unity gain)
- <0.05% SMPTE IM @ limit level
- <0.1%, 50 Hz to 15 kHz (+8 dBm unity gain)

Dynamic Range
- >90 dB (22.4-kHz unweighted noise bandwidth per CCIR 468-2 and DIN 45405)

Channel Separation
- >80 dB @ 1 kHz
- >60 dB, 20 Hz to 20 kHz

Interchannel Phase Differential
- <15°, 50 Hz to 15 kHz

Encoding
- 16-bit linear PCM

Delay Capacity
1300 mono: 680, 1365, 2731, or 4096 milliseconds
1300S stereo: 341, 683, 1365, or 2048 milliseconds

Resolution of Maximum Delay
Refer to control module specification

Sampling Rate
1300 mono: 48 kHz
1300S stereo: 48 kHz simultaneous

Master Clock
Internal 6.14-MHz frequency or external source

Filtering
9-pole elliptical input and output filters

Configurations
1-in/1-out -- 1300 mono
2-in/2-out -- 1300S stereo
For other configurations, consult factory.

Controls and Indicators

Front Panel

Fixed Delay (BASE DELAY)
4-position digit switch

Display Mode Switch (DISPLAY - FRAMES/ms)
Delay display value selectable in milliseconds or frame units

Bypass Switch (AUDIO - BYPASS/NORM)
Relay bypasses delay line without repatching or unplugging

Delay Display (DELAY)
4-digit, 7-segment readout

Headroom Display (HEADROOM)
10-LED 3-dB step peak-reading display indicating actual operating headroom relative to converter limiting;
calibration range: 0 to 27 dB

Level Setting (LEVEL ADJ. - IN/OUT)
Single-turn pot on input and output channels, providing adjustment range of 16 dB

Units/Mode LEDs
4 LED indicators (functions dependent on options)

Compensation Switch (COMP. - IN/OUT)
Selects either total compensated delay (delay determined by sensing logic in the control module plus fixed delay) or fixed delay alone (ignoring delay-sensing logic in the control module)

Rear Panel

Audio Input

XLR connector, balanced line input, pin 2 high
(transformer isolation or direct coupling available)

Input Impedance
Nominal: >10 kilohms in parallel with 150 pF
Selectable: 150 ohms 2% or 600 ohms 2% returned to >10 kilohms in bypass mode

Input Level
+8 to +24 dBm, protected from static and overvoltage stress

Audio Output

XLR connector, balanced line output
(transformer isolation or direct coupling available)

Output Impedance
<150 ohms

Maximum Output Level
At least +24 dBm (600 ohms) and at least +22 dBm into 150 ohms (equivalent voltage into 600 ohms) transformer isolated

MASTER CLOCK IN, MASTER CLOCK OUT
BNC connectors, TTL-compatible signals;
allows cascading of multiple units with a common time base

FUSE
Mains fuse connector (secondary fuses inside chassis on printed circuit board)

Power and Dimensions

Power
100, 120, 220, or 240 Vac (-10%, +5%), 50 to 60 Hz, 30 W max

Power Connector
Standard 3-pin IEC power connector

Mains Fuse
100/120 Vac: 3AG, 0.5A
220/240 Vac: 20 mm, 0.25A

Voltage Selection
Internally switched

Protection
Mains and secondary fuses
Voltage transient suppressor on ac mains, overvoltage protection on logic power supplies, thermal and short-circuit protection on all power supplies

Power-Up/Down
Noise-free via delayed relay pull-in with mute and relay drop-out upon power failure; gold relay contacts for audio bypass in event of circuit or power failure

RFI Shielding
FCC -- Class A for computing device

Operating Temperature Range
0 to 40°C

Dimensions
Standard 19-inch relay rack:
19"w by 1 3/4"h by 13 1/2"d
(488 by 44 by 343 mm)

Weight
Net: 10.5 lb (4.76 kg)
Shipping: 13.5 lb (6.12 kg)

2 INSTALLATION

2.1 Unpacking and Inspection

Upon receipt of the 1300, inspect the container for dents, water damage, or other obvious signs of improper handling. Remove the 1300 from its shipping container and protective plastic bag. Save all packing materials for reshipment. Remove the top cover and inspect the interior for loose material or other signs of damage. Report any damage to the carrier.

2.2 Mounting

The 1300 can rest on any flat surface or it can be mounted in a standard 19-in. EIA relay rack; it is 13 1/2 in. deep and 1 3/4 in. high. In any installation, the 1300 must always be mounted to allow sufficient airflow for proper ventilation. Ensure that the top panel vents are never blocked.

To protect from mechanical shock during transport, support the rear chassis of rack-mounted units.

2.3 Power Requirements

The factory preset nominal operating voltage appears on the rear panel. Maximum power consumption is 30 W. The power cord uses a standard 3-pin IEC connector, providing chassis grounding to the ac mains line.

The 1300 can be operated at either 100, 120, 220, or 240 Vac (-10%, +5%), from 50 to 60 Hz, by changing the setting of the voltage changeover switches and installing a mains fuse with a rating compatible with the selected voltage.

Voltage Changeover. To change the voltage setting to other than the factory preset selection, use the following procedures:

1. Remove the power cord.
2. Remove the screws holding the top panel in place.
3. Using a small screwdriver, set the two voltage changeover switches (shown in Fig. 2.1) to the appropriate settings as shown in Fig. 2.2.
4. Reinstall the top panel.
5. Make sure the proper mains fuse is installed in the rear panel -- install a new fuse if necessary. (For fuse information, refer to Table 2.1.)
6. Affix a label to the rear panel indicating the new voltage setting.
7. Refit the power cord.

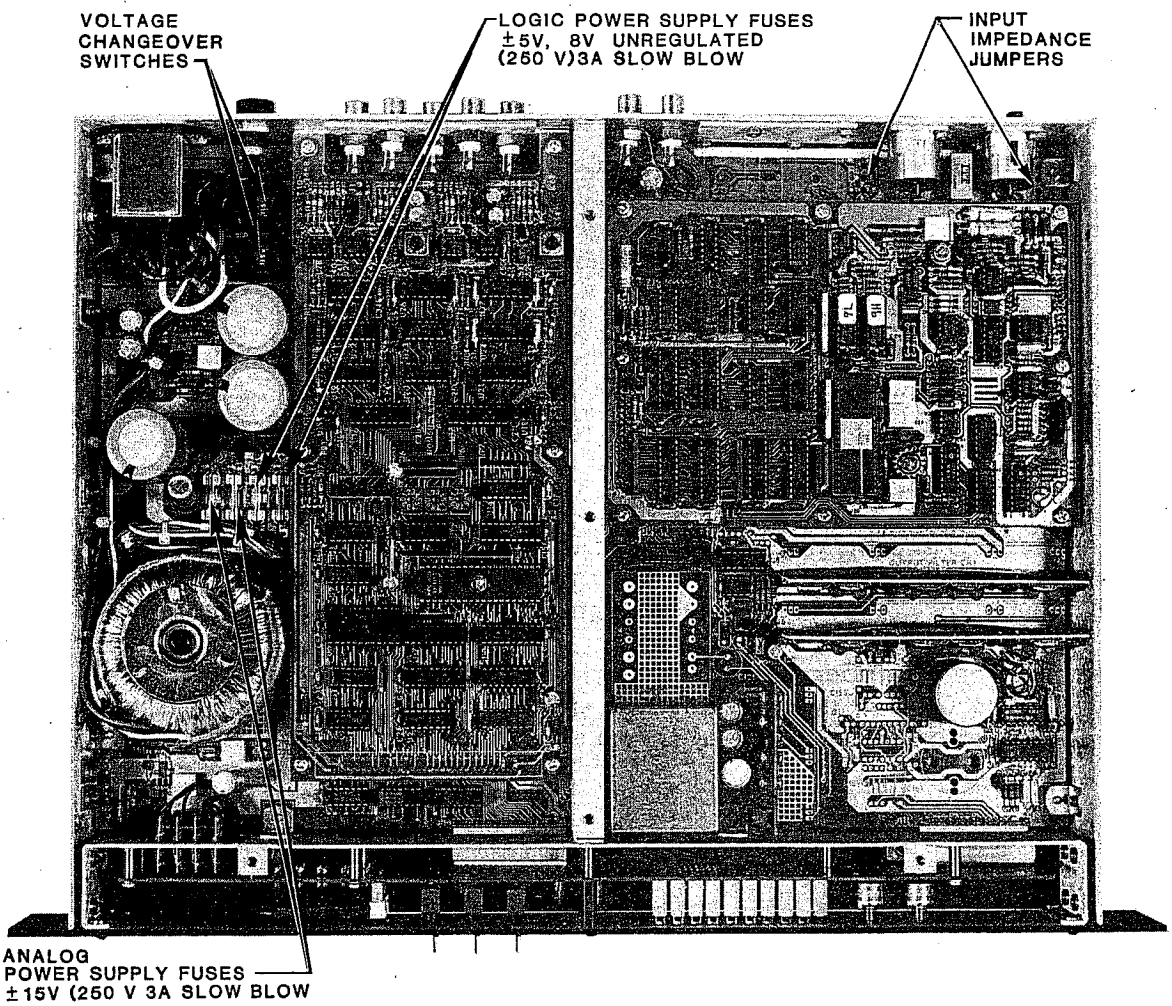

Fig. 2.1. Location of Voltage Changeover Switches and Secondary Fuses.

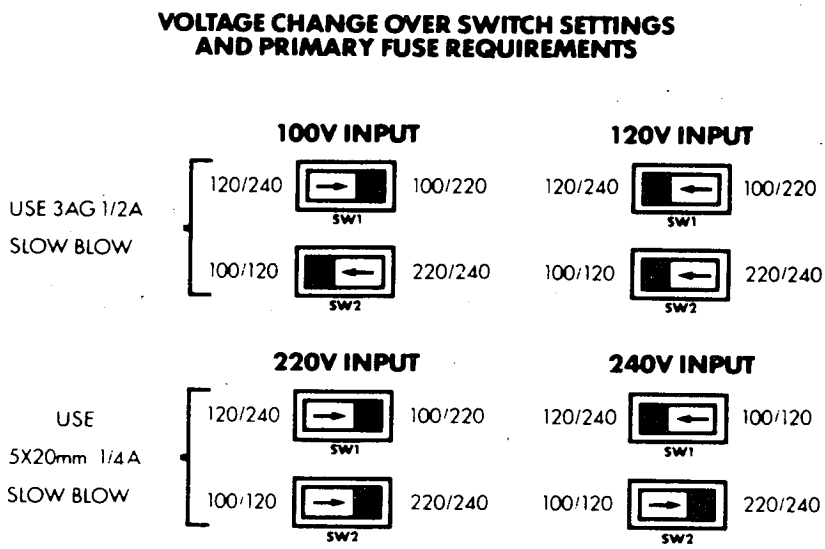

Fig. 2.2. Voltage Changeover Switch Settings.

Table 2.1. Rear Mains Fuse Ratings for Operating Voltages.

Nominal Voltage (Vac)	Operating Range (Vac)	Fuse Rating
100	90-105	3AG 0.5A slow blow
120	108-126	
220	198-231	20 mm 0.25A slow blow
240	216-252	

2.4 System Interconnections

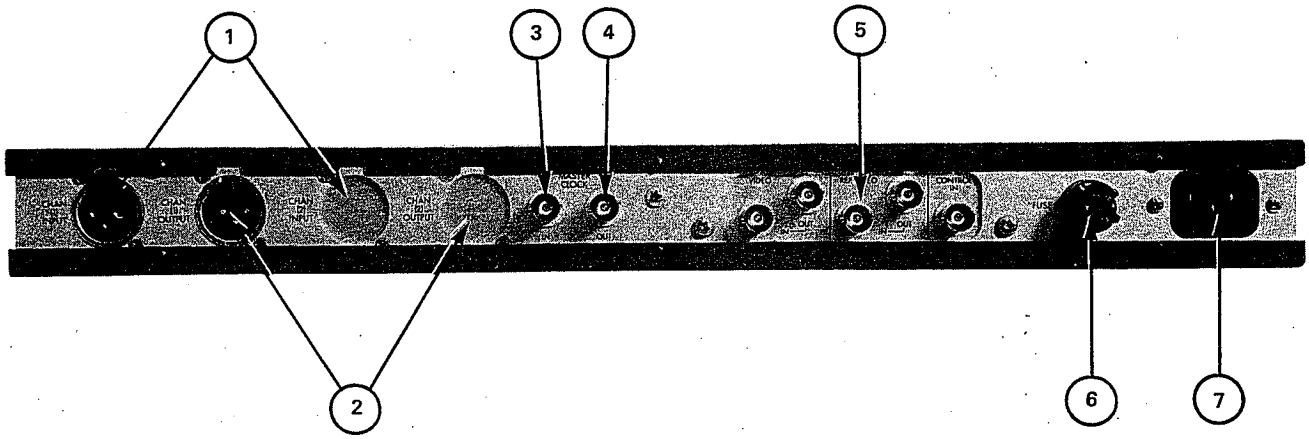

Fig. 2.3. Model 1300 Rear Panel.

1 **CHAN INPUT** balanced line inputs using XLR connectors (pin 2 high). Input impedance is jumper selectable to 150 pF capacitance in parallel with 150 ohms 2%, 600 ohms 2%, or >10 kilohms. Inputs are protected from static and overvoltage stress with maximum input levels from +8 dBm to +24 dBm. (Transformer isolated or direct-coupled units available.)

2 **CHAN OUTPUT** balanced line outputs using XLR connectors (pin 2 high). Output impedance is <150 ohms with a maximum output level of +24 dBm into 150 ohms. (Transformer isolated or direct-coupled units available.)

3 **MASTER CLOCK IN** TTL-compatible input line using a BNC connector. This input accepts MASTER CLOCK OUT signals from another 1300 unit to allow cascading of multiple units with a common time base. When a MASTER CLOCK OUT line from one unit is connected to the MASTER CLOCK IN line of a second unit, automatic switching is activated so that the clock pulse of the first unit drives the second unit.

4 **MASTER CLOCK OUT** TTL-compatible output line using a BNC connector. This output passes clock pulses to another 1300 so that units can be cascaded using a common time base for stereo or other multichannel applications. The MASTER CLOCK OUT pulse is the master timing signal controlling another 1300 in a master/slave relation.

5 **Control Module Connectors** actual configuration dependent on control module option.

6 **FUSE** panel-mounted connector for the mains fuse. It accepts 3AG fuses.

7 **Power Connector** accepts a standard 3-pin IEC ac power cord (supplied) and operates on 100, 120, 220, or 240 Vac (-10%, +5%) from 50 to 60 Hz, depending on the setting of the voltage-changeover switches and mains fuse.

Signal Connection Requirements

The audio input and output XLR connectors on the 1300 conform to IEC standards, with pin 2 high, pin 3 low, and pin 1 ground. Because all inputs and outputs are balanced lines, the pin-3-high convention can be used if applied consistently to inputs and outputs. Figure 2.4 shows a wiring diagram for the XLR connectors. Requirements for all connectors except those associated with the control module are listed in Table 2.2. Table 2.3 lists the internal jumper configurations for selecting input impedances.

Table 2.2. General Signal Connection Requirements.

Connectors	Signal Requirements
MASTER CLOCK IN	TTL-level clock signal input; BNC terminal
MASTER CLOCK OUT	TTL-level clock signal output; BNC terminal
CHAN INPUT	Audio input, balanced, +8 to +24 dBm; 150-ohm, 600-ohm, or >10-kilohm impedance in parallel with 150 pF capacitance
CHAN OUTPUT	Audio output, balanced, maximum output level >+24 dBm (600-ohm load) and >+22 dBm into 150 ohms (equivalent voltage into 600 ohms)

Table 2.3 Input Impedance Jumper Selection.

	Jumper Configurations*	
Impedance	W27	W28
150 ohms	1, 2	1, 2
600 ohms	2, 3	2, 3
>10 kilohms	**	**

*Location of input impedance jumpers is shown in Fig. 2.1; W27 is for channel 2, W28 for channel 1.
**No jumpers connected.

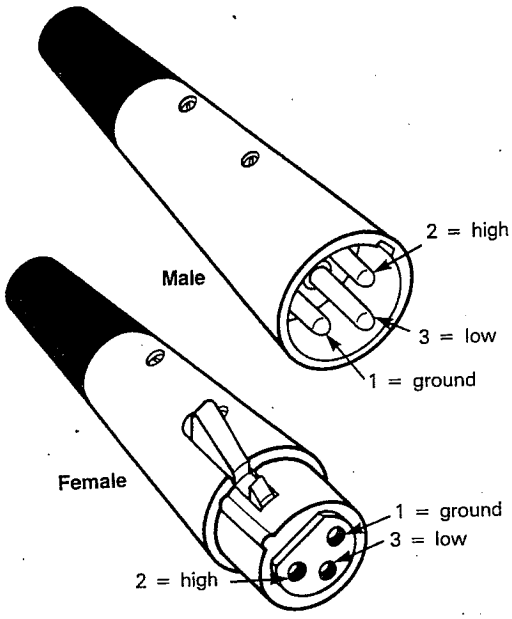

Fig. 2.4. Wiring Diagram for XLR Connectors.

3 OPERATION

3.1 Front-panel Controls and Indicators

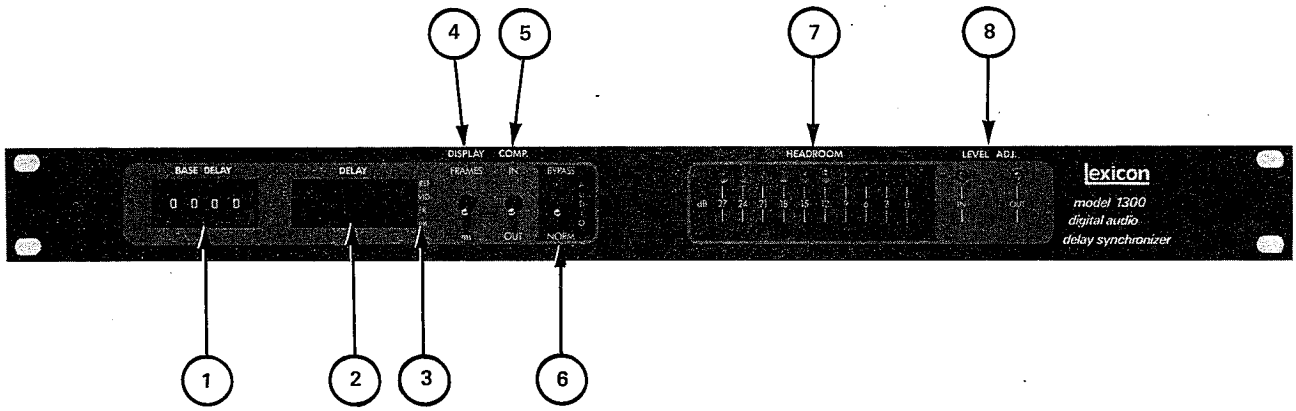

Fig. 3.1. Model 1300 Front Panel.

1 **BASE DELAY switch** This four-position digit switch selects the amount of fixed delay in 1-ms intervals applied to the audio input signals.

2 **DELAY display window** This window digitally displays either (1) the fixed delay time set by the BASE DELAY switch or (2) the total compensated delay time, which includes both the fixed delay and the variable delay determined by the sensing logic in the control module. Note: Delay time can be displayed in milliseconds or frame units, depending on the setting of the DISPLAY switch.

3 **LED status indicators** When lit, these LEDs in the display window show the following conditions:

REF -- Reference signal is not present at the appropriate input on the control module

VID -- Operating signal is not present at the appropriate input on the control module

FR -- Delay time is displayed in frames

ms -- Delay time is displayed in milliseconds

4 **DISPLAY toggle switch** When this switch is set to FRAMES, delay time shown in the display window is shown in frame units. When the switch is set to ms, delay time is shown in milliseconds.

5 **COMP (compensation) toggle switch** When this switch is set to IN, total compensated delay time is applied to the audio input signal; total compensated delay time includes both the variable delay determined by the sensing logic in the control module and the fixed delay determined by the BASE DELAY switch. When this switch is set to OUT, only the fixed delay determined by the BASE DELAY switch is applied to the audio input signal.

6 **BYPASS toggle switch** When this switch is set to BYPASS, the audio input signal is routed directly to the audio output, bypassing the 1300 delay line. When this switch is set to NORM, the audio input signal is routed through the 1300's delay processing circuitry. Note: When set to BYPASS, "bP" appears in the display window.

7 **HEADROOM indicators** This 10-segment LED display shows true headroom in 3-dB steps, from 27 to 0 dB.

8 **LEVEL ADJ. potentiometers** These single-turn potentiometers adjust the audio level up to a maximum of 16 dB. IN controls the audio input level, and OUT controls the audio output level. Use a small flat-blade screwdriver to make adjustments.

3.2 Clock Operations

To synchronize the clocks in two or more units, connect a line from the designated master unit's MASTER CLOCK OUT connector to the slave's MASTER CLOCK IN connector. The slave's MASTER CLOCK OUT line can then be connected to a third unit's MASTER CLOCK IN connector (and so on).

3.3 Power-Up Diagnostics and Power-Fail Operation

Power-Up. When the unit is first turned on, a power-up diagnostic test is run. During this test, all LEDs momentarily flash, and when the test is completed, the unit is ready for normal operation.

Power-Fail. The 1300 provides a special power-fail routine to protect it from unusual behavior during momentary power losses. When the ac power drops below the lowest level that can sustain proper operation (typically about 80 V for a nominal 120-V line), the 1300 automatically goes into bypass mode, locking out delay processing and showing "bP" in the display window, regardless of the active control settings. When power is restored, the 1300 remains in bypass mode with "bP" still displayed. To reset the unit for delay processing, toggle the AUDIO switch from NORM to BYPASS and then back to NORM.

Note: Depending on the extent and duration of a power loss, when power is restored the unit may return to the normal power-up routine (recovery from total power failure), or it may return to operation in the bypass mode (recovery from a momentary power loss).

3.4 Delay Response

The 1300 has a built-in latency period of approximately 1 second for all delay settings. When the BASE DELAY switch is changed, a latency period of about 1 second occurs before the new value takes effect and is shown in the display window. This latency period allows the delay time to stabilize, preventing the 1300 from tracking incorrect or irrelevant information, such as values between switch settings as the settings are being changed.

3.5 General Theory of Operation

Overview

The 1300 is a digital delay line designed to compensate for delay inherent in broadcast environments. To that end, it can be configured with a variety of control module options designed for unique applications with versions available for various transmission systems (for example, NTSC, PAL, or SECAM).

The basic delay line in the 1300 is factory preset for one of two audio input/output assignments:

- 1-in/1-out mono -- Model 1300
- 2-in/2-out stereo -- Model 1300S

Four memory options are available:

- 680, 1360, 2048, or 4096 milliseconds for mono models
- 340, 680, 1024, or 2048 milliseconds for stereo models

The 1300's audio circuitry accepts all standard analog audio signals and after conditioning converts those signals into digital form. The digitized information is then processed by the 1300's delay-line circuitry, which is under the control of the control module, converted back into analog, and passed to the audio output. Figure 3.2 shows a generalized block diagram for a stereo system, and the remainder of this section describes characteristics of the delay-line and converter circuitry that are unique to the 1300. The control module is described in Sec. 4.

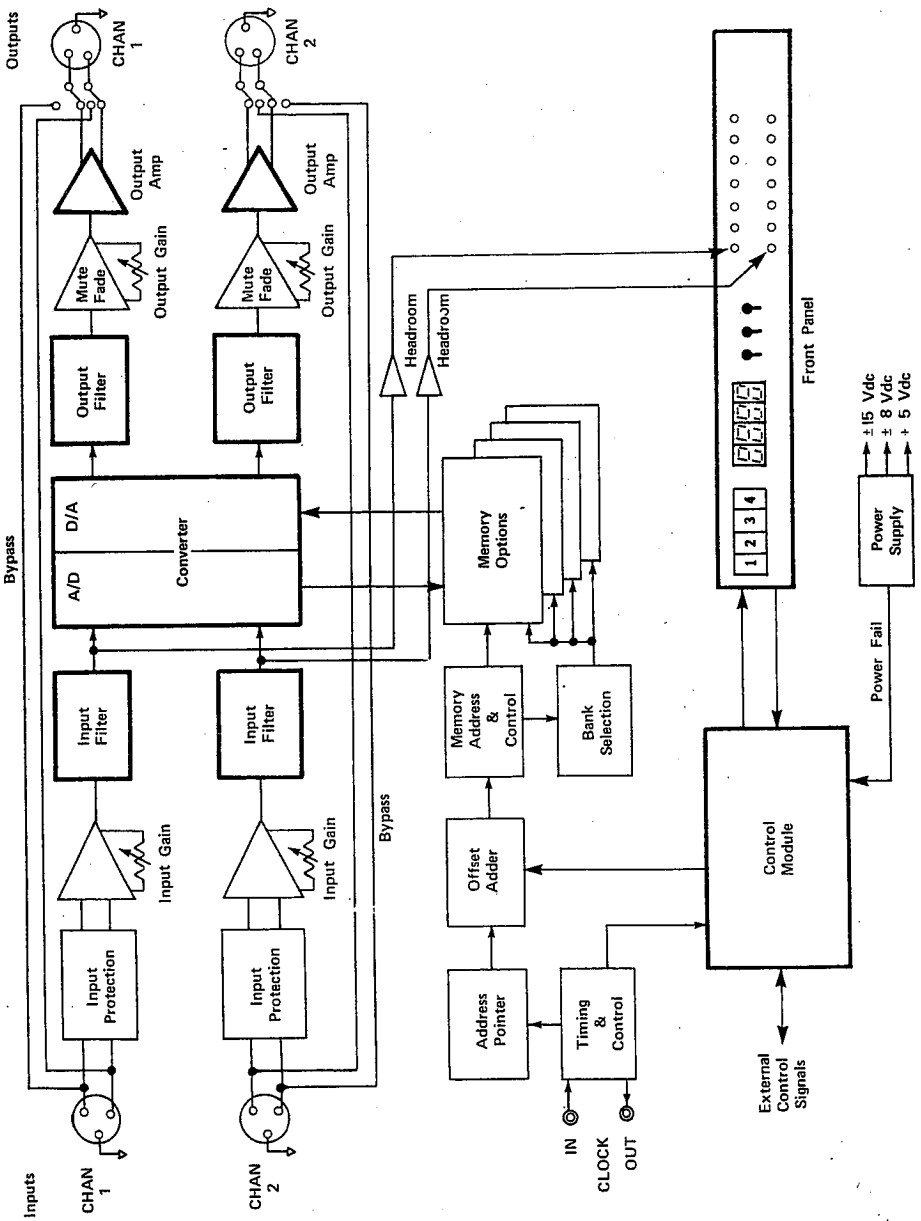

Fig. 3.2. Block Diagram for the Model 1300S (Stereo Version).

3.5.1 Delay-Line Circuitry

The 1300 has a standard binary counter with offset adder structure designed to accommodate mono or stereo configurations; audio configurations are factory preset. The 1300 can have one, two, four, or six banks of memory (depending on the option selected) and can be controlled by either its internal clock or an external clock. Provision is made to develop memory offsets of one address location by using an offset adder that equals the maximum number of bits in the address counter, which allows memory resolution down to 20.8 microseconds.

Clock. The 1300's internal clock is a 6.144-MHz oscillator. Output is selected by a gate selection circuit that selects the internal clock source, provided no external clock input signal is present. With an external clock, transistor Q3 dumps a charge from C95 each time the external clock input goes low. Between cycles, C95 does not charge to the threshold of U73 and U74, thus rerouting the external clock input to the delay-line counter chains.

Counter Chain. The first 5 bits of the counter chain WC0 to WC4 are used to define 32 time slots for partitioning the basic word cycle of the delay-line operation. WC0 to WC4 address ROM U76; U76's output is deglitched by U78, a 374 D-latch. Transistor Q4 applies power to U76 on a 25% duty cycle basis to reduce the power consumption of the 82S123 ROM. Power is applied for 160-ns intervals and is shut off immediately after ROM data is latched into U78. See Fig. 3.3.

The counter stage, which follows the WC counter, has different jumper assignments (factory preset) for mono or stereo operation. In the stereo mode, the input bits of U71 are loaded to 1000 to allow overflow after eight word cycles (see Table 3.1). Additional jumpers connect MA0 and MA1 to the QB and QC outputs of the counter to increment the memory address after each word cycle.

The basic period of the 6.144-MHz clock is 162.76 ns. This clock is further divided by 2 (for stereo) or 4 (for mono) by jumper assignments to provide a 50% duty cycle MC signal and signal RME/, a 25% duty cycle signal to power the 82S123 ROM only when actual data is accessed.

The following description is based on a jumper setting of divide-by-two, the case for stereo inputs sampled at 48 kHz. The word cycle is divided into 32 325.52-ns intervals; a standard binary counter implemented with LS/HC counters provides status lines WC0 to WC4. All five of these lines are used to address a 32- x 8-bit ROM, which in turn provides timing signals for delay-line and converter operation. A complete stereo cycle requires two word cycles.

The first 16 states of the word cycle are used to implement two memory read operations: the first read is designated "high byte" and provides the first 8 bits of memory read data; a second read provides the low byte of read data.

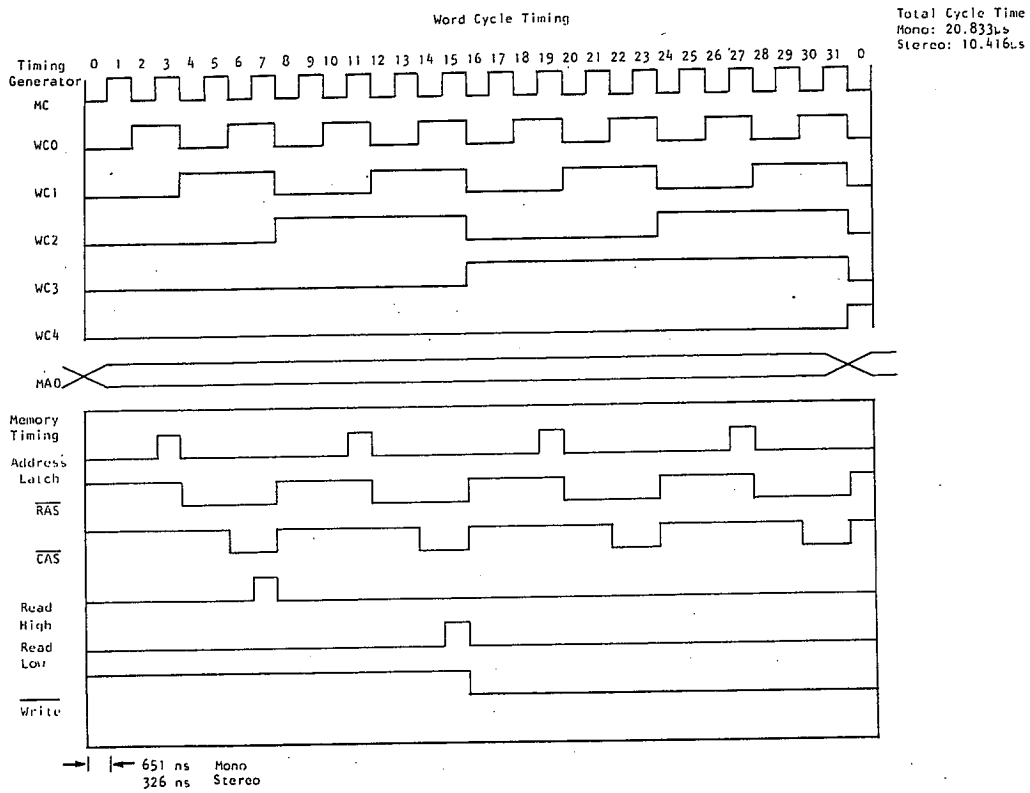

Fig. 3.3. Word Cycle Timing Diagram for Counter Chain.

Table 3.1. Word Cycle and Memory Timing.

Configuration	U71 Counter
1300 Mono 1 in/1 out	MSB LSB* 1000 • • • 1111 not used — WC4 MA1 — MA0
1300S Stereo 2-in/2-out	MSB LSB 1000 • • • 1111 not used — WC4 MA1 — MA0(L/R)

* MSB = most significant bit; LSB = least significant bit.

Memory Read Cycle. Offset memory counter data is latched into a pair of HC octal registers at the beginning of time slots 3 and 11. During time slot 3, signal WC2 is low, thus enabling the outputs of U56 (the low 8 bits of the memory address) onto the memory address lines. The rising edge of WC2 (326 ns later) strobes the row address data into all memory circuits. A short (about 150-ns) delay is provided after row select to delay the select signal, which places the column address data on the address bus and de-selects the row address data. This delay is implemented with a 150 pf, 1k time constant at the input of U64 pin 10. Column select is asserted about 652 ns after row select. At this time only one bank of memory is selected with an inverted column address select (CAS/) signal as determined by the high-order bits of the address counter and offset adder.

Memory output data is latched 326 ns after the falling edge of CAS/.

Memory Write Cycle. Memory write occurs during the second half of the word cycle. WC4/ is used to develop the write control signals to the RAMs (WR0/ - WR3/). All other row address select (RAS/) and CAS/ signals are identical to the read cycle. To create a write address that equals the address counter scale, a word of all 1s with a carry input of 1 is used for an offset word. This is actually a subtraction of 0. The offset of this is generated by placing the offset bus latches in a high-impedance state and allowing pull-up resistors to bring the bus to all 1s. Signal WC4/ connected to U70 pin 10 goes to ground during write, causing pin 8 of U70 to go high, thus providing a carry input of 1.

Delay Select with Control Module Removed. When the control module is removed, the entire offset bus is pulled high to logic 1s, and pins 4/5 of U70 are pulled high, causing a logic 1 to be placed at the carry input of the low order adder. In this condition, read occurs before write at identical addresses, thus providing maximum delay to be read from memory, which facilitates delay testing in the absence of a control module.

Memory Offset. The address logic is designed to allow adding an offset to all bits by an 18-bit offset word (OFFS0 - 17). For mono configurations, the lowest offset bit corresponds to a least amount of delay time or one sample in duration. In this instance, the microprocessor can provide offset setting of the lowest order offset bit.

For stereo configurations, the lowest address bit is used to define channels 1 and 2; the microprocessor always sets this bit to 0 to prevent reversal of output channels.

High-order offset bits -- To prevent wrap-around delay selection errors, the high-order offset bits are set so that the total offset word never exceeds the size of the maximum memory address. Offset read locations must fall somewhere behind the write counter address to represent a relative read-after-write data delay. This lagging address is the

complement of an addition to the write pointer to find a delay position behind the write pointer's position and direction. Subtraction is performed by using the 1's complement of the delay value required. Hardware implementation requires that the upper offset bits be memory size (modulo) restricted. For example, the complement of 0 through 5 (memory banks) must be 5 through 0 inclusive and not 7 through 2 (the direct 1's complement). Table 3.2 shows the maximum offset word size as a function of installed memory.

Table 3.2. Maximum Offset Words.

	Bits					
Banks	OFF17	OFF16	OFF15	OFF14	OFF13 ⟶ 1	OFF0 (Stereo only)
1	0	0	0	1	any	0
2	0	0	1	1	any	0
4	0	1	1	1	any	0
6	1	0	1	1	any	0

Memory Size Selection and Control. The basic memory element is a 65536-x 1-bit dynamic RAM. RAM is organized into banks of eight elements. To provide a 16-bit data element, all read and write operations are done in pairs. The first read or write is called the "high byte" and the second the "low byte."

Eight memories (one bank) provide 32768 individual 16-bit storage locations. Counter bit WC3 is used to select high/low byte cycles and is connected directly to the low position of the low-order (row address) address latch.

The logic implementation allows use of one, two, four, or six banks of memory. For mono configurations, all memory locations are allocated to the single channel; for stereo configurations, memory byte pairs are allocated on an alternating basis to channel 1 and then to channel 2. In the latter instance, the counter bit following WC4 (MA0) is used as a channel-1, channel-2 pointer. The microprocessor always sets the corresponding offset bit to 0.

Memory Refresh. All memory reads and writes cycle sequentially through the address map.

Two sequential address locations are selected every 10.4 us. For complete refresh of all memory banks, 128 sequential locations must be selected. Refresh time is 10.4 us x 64 or 665.6 us (or 0.66 ms). If the input clock is divided by 4 rather than 2, refresh takes 1.33 ms. In either case, refresh occurs in less than the 2 ms specified by Intel for the 2164 RAM.

Delay Time. With a sample rate of 48 kHz, available delay time is as follows:

Banks	Mono (1300)	Stereo (1300S)
1	682.66 ms	341.3 ms
2	1.365 sec	682.66 ms
4	2.730 sec	1.365 sec
6	4.096 sec	2.048 sec

Memory Map. The use of one, two, or four banks of memory is easily accomplished by setting the modulo of the last counter to two, four, or eight, which causes counter overflow to occur after 2E15, 2E16, or 2E17 counts.

The count sequences for the last (high-order) counter bits are listed in Table 3.3.

Table 3.3. High-order Memory Address Counter Bits.

Banks	High-order Memory Address Counter Bits MA17	MA16	MA15	MA14
1	0	0	0	0
2	0	0	0	1
1	0	0	1	0
4	0	0	1	1
1	0	1	0	0
6	0	1	0	1
1	0	1	1	0
2	0	1	1	1
1	1	0	0	0
4	1	0	0	1
1	1	0	1	0
2	1	0	1	1
1	1	1	0	0
6	1	1	0	1
1	1	1	1	0
2	1	1	1	1
1	1	0	0	0
4	1	0	0	1
1	1	0	1	0
2	1	0	1	1
1	1	1	0	0
6	1	1	0	1
1	1	1	1	0
2	1	1	1	1

For counts of 2E15, 2E16, and 2E17, adder U57 acts as a straight through path for memory address data; the 138 decoder selector is jumpered to select CAS0, CAS0/CAS1, or CAS0 to CAS4 as follows:

138 Decoder Inputs

	Inputs		
Banks	C	B	A
1	GND	GND	GND
2	GND	GND	MA15
4	GND	MA16	MA15
6	MA17	MA16	MA15

Jumper settings for one, two, or four banks of memory ensure that high-order counter bits are ignored if they are not required. With proper constraint of the address offset word, a carry out of the high-order adder is not generated and OMA16 and OMA17 are never high at the same time, ensuring that U57 always adds 0 to the memory address.

For configurations using six memory banks, several considerations must be noted.

First, consider the memory map representation shown in Fig. 3.4 for the high-order three bits of address when six banks of memory are used. The map divides into eight sectors, the last two of which must be mapped out of the legal address space. For the specific case where the offset word is 0, the counter skips over states 110 and 111. If we add an offset to a legal count, we find that the sum could lie inside the excluded address space or it could "add across" the excluded space. In instances where the sum address lies inside the excluded space, we can see that desired address region is the sector two positions clockwise from its current position. In either excluded sector, the state of MA17 and MA16 will be 11.

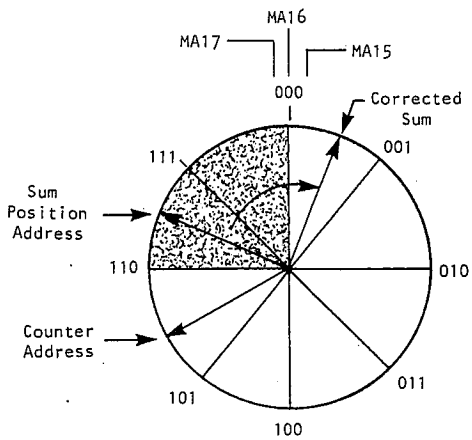

Fig. 3.4. Memory Map Representation.

The address correction is adding 2 to the offset address. Gate U64 (pins 1 and 2) detects the 11 state of MA16 and MA17 and enables a logic high to the pin 3 (A2) input of adder U57, thus adding 2 to the resultant sector address. This correction works for all sums that fall inside the excluded address sectors.

Second, consider the situation that results when the offset sum adds across the excluded region. For example, assume that MA17 to MA15 is 101 and that the offset is 011:

```
MA          101
Offset      011
        1 | 000
Carry           Sum
```

The sum is 000 and a carry of 1 is generated. The carry tells us that the resultant addition forced a result that added across the excluded boundary. In this instance, the carry-out bit from the high-order adder U61 forces a logic 1 to the pin 3 input of adder U57. The corrected sum now falls in the 010 sector or two sectors ahead of its uncorrected position. Note: the second to the highest order adder has only its first 3 bits used and that the pin 10 (E4) output then becomes its carry out.

The highest order adder has its A4 input grounded and its B4 input controlled by WC4G/. This configuration ensures that the carry out of this adder will not occur during write or selection of maximum delay with WC4/ at 0:

```
MA          0111
Offset      0111
        0 | 1110
Carry           Sum
```

Even with offset and address counter at 111, no carry can result. During read, WC4/ = logic 1, and any addition that adds across the excluded region causes a carry out to be produced; for example:

```
MA          1101
Offset      0011
        1 | 0000
Carry           Sum
```

Table 3.4 lists jumper assignments for various delay-line configurations, and Table 3.5 lists jumper assignments for the memory options. Table 3.6 contains ROM timing data for U76.

Table 3.4. Jumper Assignments for Delay-line Configurations.

Configuration	Second Counter Jumpers	Clock Jumpers	Processor Mode Jumpers
1300 Mono 1-in/1-out (48-kHz)	W10 (1, 2) W20, W18	W22 (2, 3)	none
1300S Stereo 2-in/2-out	W10 (1, 2), W20, W18	W22 (1, 2)	W14

Table 3.5. Jumper Assignments for Memory Options.

Banks	CAS Jumpers	Last Counter Jumpers	Processor Mode Jumpers
1	W6, W3, W9	none	none
2	W5, W3, W9	W11	W15
4	W5, W2, W9	W11, W12	W16
6	W5, W2, W8	W11, W13	W15, W16

Table 3.6. ROM Timing Data.

Addr (Hex)	Data Bits 7 6 5 4 3 2 1 0	Data (Hex)
1F		
00	0 0 0 1 1 1 0 0	1C
01	0 0 0 1 1 1 0 0	1C
02	1 0 0 1 1 1 0 0	9C
03	0 0 0 1 1 1 0 0	1C
04	0 0 0 1 1 1 1 0	1E
05	0 0 0 1 1 1 0 0	1C
06	0 1 0 1 1 1 0 0	5C
07	0 0 0 1 1 1 0 0	1C
08	0 0 0 1 1 1 0 0	1C
09	0 0 0 1 1 1 0 0	1C
0A	1 0 0 1 1 1 0 0	9C
0B	0 0 0 1 1 1 0 0	1C
0C	0 0 0 1 1 1 0 0	1C
0D	0 0 0 1 1 1 0 0	1C
0E	0 0 1 1 1 1 0 0	3C
0F	0 0 0 1 1 1 0 0	1C
10	0 0 0 1 1 1 0 0	1C
11	0 0 0 1 1 0 0 0	18
12	1 0 0 0 1 1 0 0	8C
13	0 0 0 0 1 1 0 0	0C
14	0 0 0 0 1 1 0 0	0C
15	0 0 0 0 1 1 0 0	0C
16	0 0 0 0 1 1 0 0	0C
17	0 0 0 1 1 1 0 0	1C
18	0 0 0 1 1 1 0 0	1C
19	0 0 0 1 1 1 0 0	1C
1A	1 0 0 1 0 1 0 0	94
1B	0 0 0 1 0 1 0 0	14
1C	0 0 0 1 0 1 0 0	14
1D	0 0 0 1 0 1 0 0	14
1E	0 0 0 1 0 1 0 0	14
1F	0 0 0 1 1 1 0 0	1C
00		

3.5.2 Converter Circuitry

The 1300's converter is designed to process two discrete audio channels at a 48-kHz sampling rate.

The converter uses two 16-bit analog-to-digital converters (ADCs) and one 16-bit digital-to-analog converter (DAC). The DAC is sufficiently fast to be time-shared between the two channels.

A timing diagram of critical signal waveforms appears in Fig. 3.5.

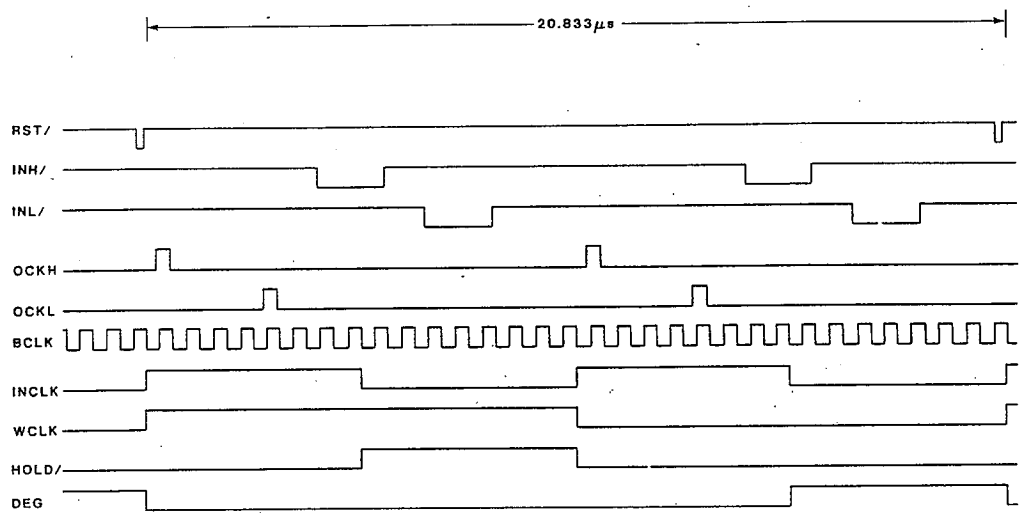

Fig. 3.5. Timing Diagram for 1300 Converter.

Circuit Description

A/D Conversion

This description refers to one channel; both channels operate identically. The ADC uses a multiple-slope single-integration method of conversion. A description of this technique follows.

The incoming signal is first sampled by a track-and-hold circuit composed of op amp U29 (configured as a noninverting buffer), FET switch U26, op amp U25 (configured as an integrator), and associated components. In addition to sampling the incoming signal, this circuit reduces the signal gain by 6 dB and level shifts to produce a negative-biased unipolar sampled waveform. Note that the input node is clamped to ground during the hold period to reduce through-talk and to keep a low reverse voltage on the off FET.

When HOLD/ is high (see Fig. 3.5), the input signal is sampled and the output of the track-and-hold circuit attains a voltage proportional (level-shifted and gain-adjusted) to the input voltage at that moment. The sampling period is 5.2 us. When HOLD/ goes low, the FET switch, U26, opens and the circuit is put in the hold mode. At this time, two current sources internal to the ADC, whose values are set by trimpot R18 and are proportioned internally at the ratio of 127:1, are switched on. These current sources are connected to the summing node of the integrator, U25. This provides a discharge path for the hold capacitor, C50, and the output voltage of the track-and-hold circuit now increases toward ground potential at a constant rate. This voltage is monitored by a comparator internal to the ADC. Simultaneous to the discharge of the hold cap, a 9-bit high-speed counter in the ADC is enabled and begins counting at 48 MHz; this frequency is set by the external crystal oscillator circuit composed of Y1, T1, and associated components. At the level set by trimpot R15, the previously mentioned comparator toggles and causes three actions inside the ADC: (1) the 9-bit counter is disabled, (2) a 7-bit counter is enabled, and (3) the high-current source is turned off, leaving only the low-current source to discharge the hold cap. The hold cap is now discharged at a much slower rate, completing the process of multiple-slope integration.

The track-and-hold circuit is also fed to a noninverting amplifier composed of U20 and associated components, which, because of diode CR7, is essentially unity gain for input voltages below (more negative than) about -50 mV. When the track-and-hold circuit has discharged to a level above -50 mV, this circuit provides a gain of 16. Another comparator internal to the ADC monitors the output of this circuit and toggles at the zero crossing. The high gain enables a more precise zero crossing detection. When this second comparator toggles, the 7-bit counter and the low current source are disabled.

The 9-bit counter and the 7-bit counter now contain the most significant and least significant bytes, respectively, and this data is then dumped into a 16-bit latch, also internal to the ADC. This sequence is then repeated as the next sample is taken and evaluated. While this next sample is being converted (when WCLK goes low), the data from the previous conversion cycle is serially shifted out of the ADC, starting with the MSB, on each falling edge of BCLK.

Digital Circuitry

The serial data output of the ADC, which operates from a -5-V supply, is level-shifted up to standard TTL/HC logic levels by a common-base transistor circuit, Q1, and is sent to one of the two inputs of an 8-bit serial-in/parallel-out shift register, U6. This shift register, along with U11, is clocked on the rising edge of BCLK. After 16 BCLK periods (1/2 of a complete stereo cycle), these two shift registers, and therefore the ADC bus, contain the whole 16-bit word from the channel 1 ADC. Likewise, shift registers U9 and U13 contain the 16-bit data from the channel 2 ADC. At this point, two 8-bit latches, U3 and U7, are clocked by control signal INCLK and thereby latch the data present on the ADC bus.

As shown earlier, this data is the channel 1 16-bit word, and it is subsequently enabled onto the DAB bus, high byte first, when INH/ and then INL/ go low, and written into memory.

Returning to when the channel 1 data is latched by INCLK: simultaneously WCLK goes high, and the serial data output of both ADCs goes high as the internal shift registers are disabled. This enables the other input of shift register U6, coming from the channel 2 shift registers, U9 and U13. During the next 1/2 cycle, the channel 2 data is shifted into U6 and U11. After 16 BCLK counts, these two 8-bit shift registers contain the complete channel 2 16-bit word. The previously mentioned latches are once again clocked by INCLK, and the channel 2 data is written into memory when INH/ and INL/ subsequently go low.

The data in memory is read in the same order in which it was written. Channel 1 high byte is read first and clocked into latch U15 by the signal OCKH, followed by the channel 1 low byte, which is clocked into latch U4 by the signal OCKL. The outputs of these latches are always enabled (except in self-test mode), so the DAC, U18, immediately receives this data via the DAC bus. By receiving the high byte first, the DAC is allowed more time to settle the most significant bits before its output is sampled. Channel 2 data is subsequently clocked in the same manner during the next 1/2 cycle.

Self-test. In self-test mode, which is enabled by installing jumper W1, the DAB bus, and therefore the memory, is bypassed by latches U8 and U12, which load the data directly from the ADC bus to the DAC bus. Latches U4 and U15 are disabled in self-test. The clocking signal for the self-test latches, STCLK, is a delayed version of INCLK to prevent DAC glitches from being sampled when new data is clocked into the DAC.

D/A Conversion

The DAC is a voltage-output 16-bit device with complementary data inputs. The MSB is inverted to match the two's complement data output of the ADCs. The channel 1 data is converted first. A track-and-hold circuit composed of U23, U24, Q5, and associated components, samples the DAC's output when HOLD/ goes high, and then holds this level when HOLD/ returns low. The channel 2 data is then converted by the DAC and is sampled by the deglitch circuit of U22, U31, and Q3, when DEG goes high. Simultaneously, the deglitch circuit of U23, U32, and Q4 samples the channel 1 level being held in the previously mentioned track-and-hold circuit. Thus, both channels are deglitched and output simultaneously. The outputs of these two deglitch circuits are fed to their respective two-pole aperture correction circuits, U34 for channel 1 and U33 for channel 2, which provide amplitude correction for the high-frequency loss inherent in the deglitch circuits.