PCM 91

Digital Reverberator

Service Manual

Lexicon

Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.

*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and liquid entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage requiring service The unit should be serviced by qualified service personnel when:

the power supply cord or the plug has been damaged,

objects have fallen, or liquid has been spilled into the unit,

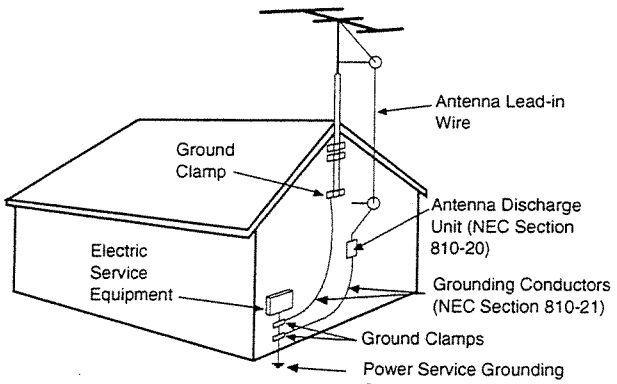
the unit has been exposed to rain,

the unit does not appear to operate normally or exhibits a marked change in performance,

the unit has been dropped, or the enclosure damaged.

Outdoor Antenna Grounding If an outside antenna is connected to the receiver, be sure the antenna system is grounded so as to provide some protection against voltage surges and built-up static charges. Section 810 of the National Electrical Code, ANSI/NFPA No. 70-1984, provides information with respect to proper grounding of the mast and supporting structure, grounding of the lead-in wire to an antenna-discharge unit, size of grounding conductors, location of antenna-discharge unit, connection to grounding electrodes, and requirements for the grounding electrode. See figure below.

Power Lines An outside antenna should be located away from power lines.



NEC — National Electrical Code

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING — The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION — The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

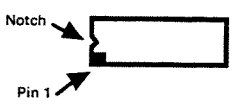
CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow to dry without rinsing.



CAUTION

ICs inserted backwards will be destroyed. Incorrect insertion of ICs is also likely to cause damage to the board.

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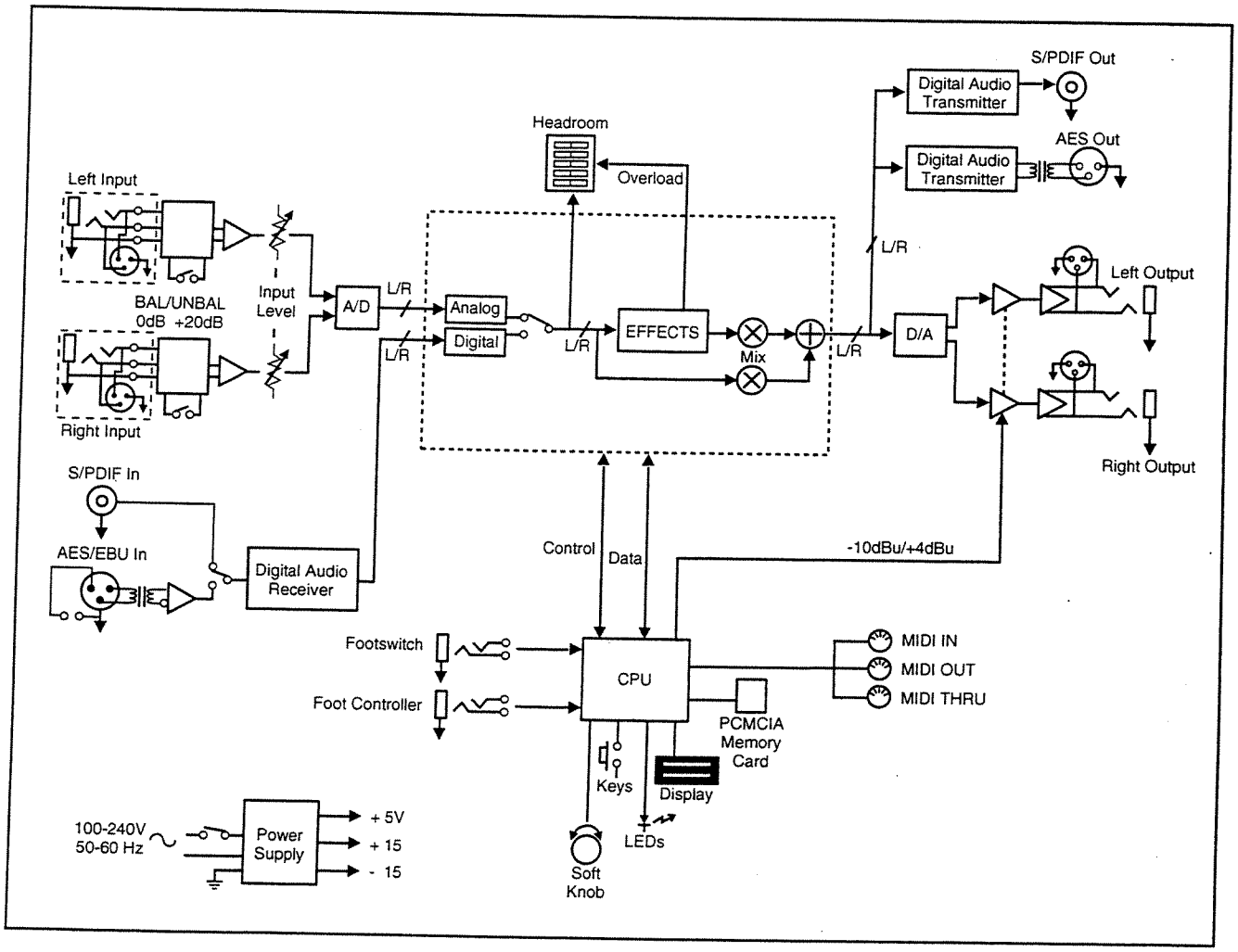
Product Overview

Block Diagram



Front Panel Overview

HEADROOM
5-position indicator for analog and digital signal levels and overload conditions.

INPUT
Adjusts analog input level.

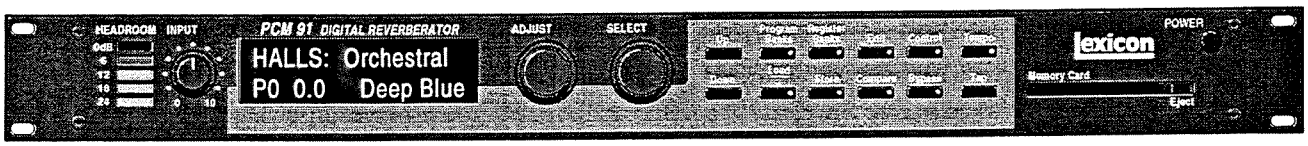
Display
Two rows of 20 alphanumeric characters display effect names and ID numbers, and parameter names and values.

ADJUST
In Edit mode, changes values of parameters chosen with SELECT. With Program Banks or Register Banks selected, behaves as a soft knob for patched parameters.

SELECT
Scrolls through presets, registers or parameters. With Program Bank or Register Bank selected, scrolls through the 50 programs in the selected bank, then begins scrolling through the programs in the next bank. With Edit selected, scrolls through matrix parameters.

POWER
On/Off.

Memory Card
Slot for optional preset ROM or register RAM cards. Press Eject button to remove card.



Up/Down
Press to move up and down through program and register banks, or a parameter matrix.

Program Banks
Enables selection of factory presets. Press repeatedly to cycle selection of 5 internal preset banks and a KeyWord sorted display. Press and hold to display the name and algorithm of the current program.

Load/*
In Program or Register mode, loads the selected program. In Edit mode, scrolls through any multi-field parameter.

Register Banks
Enables selection of user memory. If a RAM card is loaded into the Memory Card slot, each press of this button selects a new register bank. Press and hold to display the name and algorithm of the current program.

Store
Initiates register store function.

Edit
Enables parameter selection for editing of values.

Compare
Active in Program, Register, and Edit modes. Press to compare the active version of the current effect with the most recently stored version.

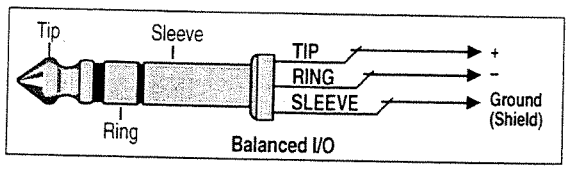
Control
Enables selection of system and global parameters.

Bypass
Bypasses or mutes audio, depending on the setting of each program's bypass parameter.

Tempo
Press to display tempo rate and to initiate tempo functions. LED flashes in time with current tempo rate.

Tap
Sets tempo. Press twice in rhythm to establish tempo rate. Press once to reset LFO.

Rear Panel Overview



AES/EBU and S/PDIF Inputs

AES/EBU format digital connectors conform to AES 3-1992 and EBU professional standards. S/PDIF format digital connectors conform to IEC-958 consumer standards. Only one of these options (AES or S/PDIF) may be selected for input.

Balanced Outputs

Output impedance is 50Ω, balanced, and levels up to +18dBu maximum full scale. 1/4" phone connectors and XLRs provided. Both S/PDIF and AES outputs are active at all times.

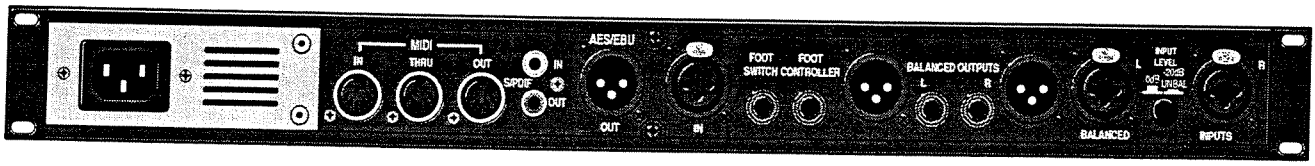
Input Level

2-position (In/Out) switch for matching input gain to the source being used. In position adds 20dB of gain to the input stages. Out position provides 0dB of gain. Use either position for balanced or unbalanced sources.

Balanced Inputs

Combined 3 pole XLR and 1/4" jacks, electronically balanced.

Input impedance is 50kΩ unbalanced, and 100kΩ balanced. Inputs accept input levels from -22dBu to +20dBu.



AC Power

Standard 3-pin IEC power connector. 100-240V, 50-60Hz automatic switching to correct voltage range.

MIDI

IN

Receives MIDI information from other MIDI equipment such as master keyboard controllers, MIDI foot controllers, sequencers and synthesizers.

THRU

Passes received MIDI data without change.

OUT

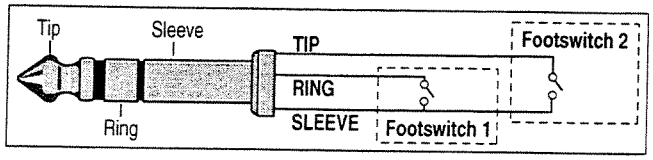
Transmits MIDI data to other equipment.

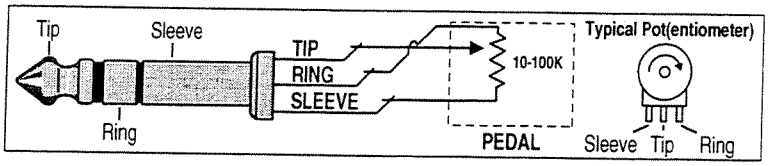
Footswitch

1/4" Tip/Ring/Sleeve phone jack for two independent momentary footswitches

Foot Controller

1/4" Tip/Ring/Sleeve phone jack provided for footpedal with 10kΩ to 100Ω impedance.





Installation Notes

Mounting

The PCM 91 uses one EIA-standard rack space, and can be mounted on any level surface or in a standard 19 inch (483 mm) rack. If the PCM 91 is mounted in a rack or road case, support the rear of the chassis to prevent possible damage from mechanical shock and vibration.

The maximum ambient operating temperature is 104°F (40°C). Provide adequate ventilation if the PCM 91 is mounted in a closed rack with heat-producing equipment such as power amplifiers.

Power Requirements

The PCM 91 is equipped with a 3-pin IEC power connector and detachable cord.

The PCM 91 will operate with power sources from 100 to 240 volts AC, 50-60Hz. Power switching to actual line voltage is automatic.

Audio Connections

Analog Audio

For best performance, maintain balanced connections, and use high-quality, low-capacitance, twisted-shielded pair cable.

When connecting to single-ended, unbalanced devices, connect the low side to signal ground at the unbalanced piece of equipment. Output level does not change when connected to an unbalanced input.

Mono Applications

Use a Y-connector inserted at the analog inputs and outputs to have the signal summed to mono.

NOTE

Be careful to keep input and output to all channels wired consistently. Out-of-phase wiring can produce audible effects.

Digital Audio

S/PDIF (IEC-958) Consumer Digital Audio I/O. 75Ω coaxial cable suited for digital audio or video signals is required. Audio grade cable is *not* suitable. AES/EBU connections require balanced connections using high quality, low capacitance, controlled impedance, data communication, twisted-shielded pair cable. **Microphone cable may introduce a significant amount of jitter into the signal, causing distortion.**

Control Connections

Dual Footswitch/Foot Controller

One 1/4 inch T/R/S phone jack is provided for 2 momentary footswitches. Another 1/4 inch T/R/S phone jack is provided for a footpedal (minimum 100Ω to maximum 10kΩ impedance). Normally open or normally closed momentary switches are suitable. At power on, the PCM 91 assumes the switch is off. Use shielded, twisted-pair cable with shield connected to sleeve. See diagram on previous page.

MIDI

5-pin DIN connectors are provided for MIDI IN, THRU and OUT. Use standard 5-pin DIN MIDI cable assemblies, available from your local dealer.

Footswitch/Foot Controller

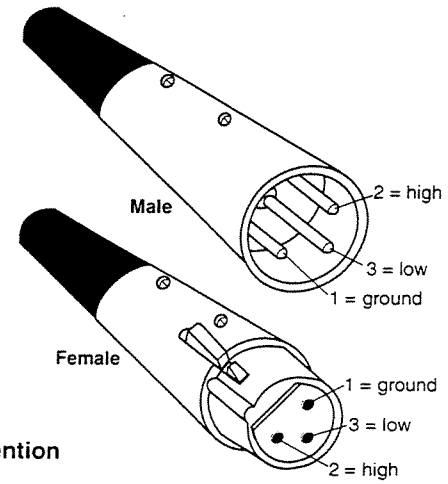
One 1/4 inch T/R/S phone jack is provided for 2 momentary footswitches. Another 1/4 inch T/R/S phone jack is provided for a footpedal (minimum 100Ω to maximum 10k impedance). Normally open or normally closed momentary switches are suitable. At power on, the PCM 81 assumes the switch is off. Use shielded, twisted-pair cable with shield connected to sleeve. See diagram on page 3.

MIDI

5-pin DIN connectors are provided for MIDI IN, THRU and OUT. Use standard 5-pin DIN MIDI cable assemblies, available from your local dealer.

Connectors

Signal	Mating Connector	Description
L and R Analog Audio Input	XLR A3M	Active balanced, pin 2 high +2dBu min; +20dBu max at 0dB setting
L and R Analog Audio Output	XLR A3F	Active balanced, pin 2 high -2dBu to +18dBu at full scale output
AES/EBU Digital Input	XLR A3M	AES 3-1992 Professional Digtial Audio Format, balanced, pin 2 high
AES/EBU Digital Output	XLR A3F	AES 3-1992 Professional Digtial Audio Format, balanced, pin 2 high
S/PDIF CP-340 Type II Consumer Digital Audio Input and Output	RCA	IEC-958 Consumer Digital Audio Format tip high
MIDI In MIDI Out MIDI Thru	5-pin DIN	Standard MIDI Interface



pin 2 high by convention

Setting Audio Levels

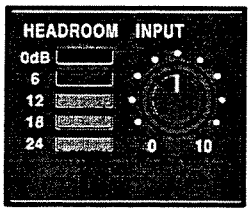
The PCM 91, with both analog and digital input and output connections, requires some attention to proper setting of signal level.

Analog inputs are first gain-conditioned by the rear panel input gain switch, and then by the front panel INPUT knob. Proper setting of both the switch and knob are important for best performance of the A/D converter.

Analog and the selected digital sources are selected in Control mode (**0.0 Audio Input Source**). The selections are: **44.1, 48, Ext: XLR** and **Ext: Coax.**

Proper setting of Input level on the PCM 91 is dependent on:

- Proper signal level into the analog front end to avoid signals causing overload at the DSP input (rear panel Input Level button),
- Proper adjustment of the signal level into the analog-to-digital converter to optimize noise and avoid overload (front panel INPUT knob),
- Proper setting of signal level into the digital signal processor to optimize noise (**InLvl** parameter in each algorithm).



Headroom Display

The headroom display provides both headroom and overload information from a variety of measurement points. The meters display analog or digital input data, depending on the selected **Audio Input Source** (Control mode **0.0**).

The chart below illustrates the adjustment range that will set input levels for both balanced and unbalanced operation.When a choice can be made, it is best to operate at the higher amplitude end of the recommended range to optimize noise performance.

	+20dB Gain	0dB Gain
overload:	>+20dBu	> 0dBu
acceptable:	+20dBu to -2dBu	0dBu to -22dBu
too low (noisy):	<-2dBu	<-22dBu

Overload

The 0db (overload) indicators will light under the following conditions:

- A/D overload
- overload at any point in effects processing
- input level within 1dB of maximum

For example, level buildup from certain reverberation modes can result in overload, even when the input A/D or digital receiver data stream is not at full scale. Such conditions are most often caused by a combination of extreme parameter settings. Adjusting parameter/level settings can eliminate these overload conditions.

Selecting a Digital Input Source

1. Press **Control**.
2. Press **Up** or **Down** until the leftmost digit in the lower lefthand corner of the display is **0**.
3. Turn SELECT to **0.0 Word Clock**, and turn ADJUST to display **Ext: XLR or Ext: Coax**, depending on the input you are using.

Setting Input Levels

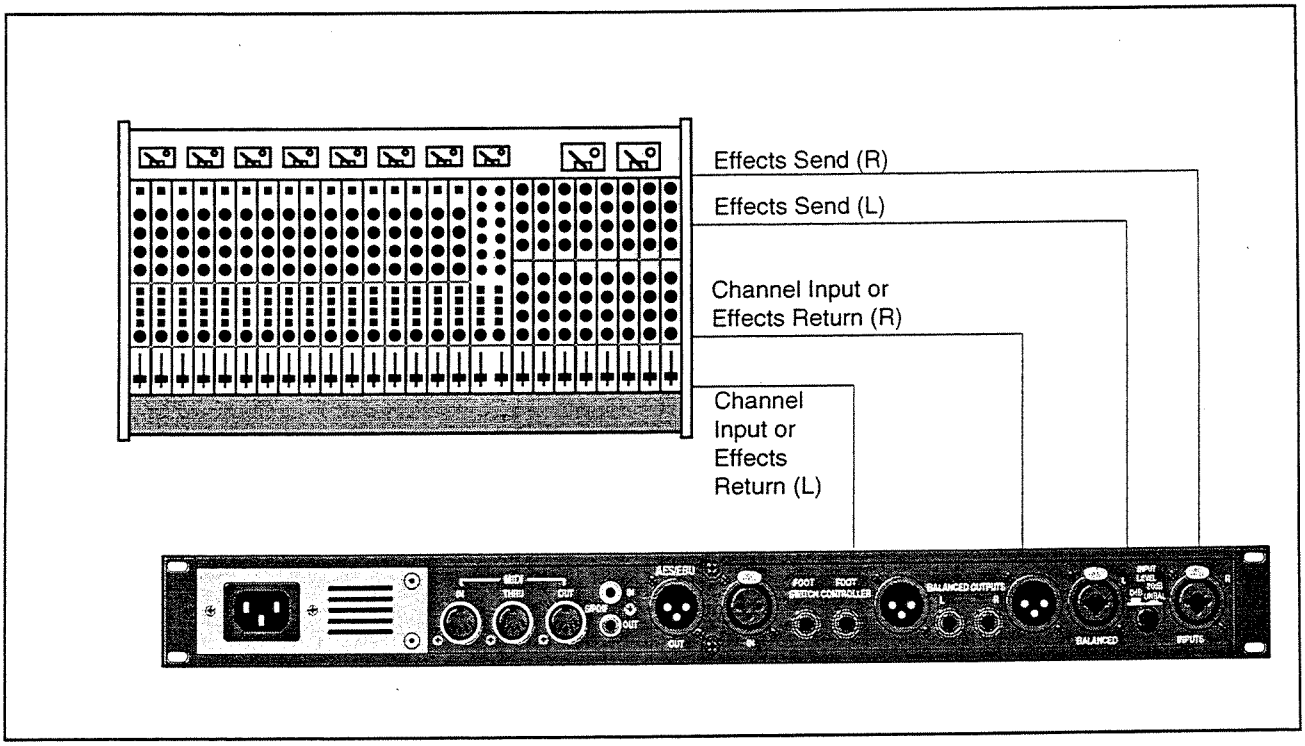
1. Press **Control**.
2. Press **Up** or **Down** until the leftmost digit in the lower lefthand corner of the display is **0**.
3. Turn SELECT to **0.0 Audio Input Source.**
4. Turn ADJUST to select **Analog: 48kHz** or **Analog: 44.1kHz.**
5. Adjust the front panel INPUT knob so that program material level peaks cause the headroom display to reach the top of the column *without* lighting the overload indicators. An occasional large signal peak causing momentary flashing of the overload indicator is acceptable in most instances, but should be validated by listening to the actual result.
6. Turn ADJUST to select **Dig:.** The display will show any valid digital format which is properly connected to the PCM 91 rear panel digital input.

Setting Analog Output Level

While still in Control mode, turn SELECT to **0.3 Output Level**. The Output Level parameter has two range positions. The appropriate position depends on the level handling capability of the device connected to the analog outputs. Devices capable of handling outputs with peak levels of 18dBu require setting **Output Level** to the **+4dBu** setting. Devices which cannot handle peak levels greater than +4dBu require the **-10dBu** setting.

Configurations

Connection to a mixing console's effects sends



If you will be using a PCM 91 as your primary effects unit, and your system includes a console with one or more auxiliary (effects) sends, connect the PCM 91 as shown above. In most applications, it is preferable to connect the PCM 91 outputs to two of the console's input channel strips, panned full left and right, rather than to the effects returns. This allows the greatest flexibility in routing and equalization.

In this configuration the console controls are used to set the amount of effect heard—the PCM 91's MIX control should be set for 100% wet. To assign a global MIX setting:

1. Press **Control.**
2. Press **Up** or **Down** until **1.x** is displayed in the lower left of the display and **System** is displayed on the upper line.
3. Turn SELECT until **System Mix Mode** is displayed on the upper line. **1.1** will be displayed in the lower left.
4. Turn ADJUST until the lower line reads:

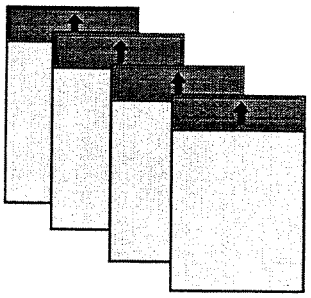
   1.1 * Global
5. Press **Load /*** to show the current global setting of MIX; use ADJUST to set it to 100% wet.

Memory Cards

You can use Memory cards to store as many as 1000 PCM 91 registers (20 banks of 50 — on a 1 Meg card). Registers stored on a properly formatted card will be recognized whenever the card is inserted, and can be accessed via the front panel **Register Banks** button, exactly as internal registers.

Memory cards can also be used to store "setups" (your system configuration, as set in Control mode). As many as 5 PCM 91 setups can be stored on a card, allowing you to transport not only your effects, but complete PCM 91 environments to another PCM 91. Cards also provide storage for additional program maps and effect chains.

See *Control Mode* Store and Load functions for details on saving setups on a card and reloading them.



Memory cards can be used to store PCM 91 registers, or setups.

Memory cards must be of the following type:

PCMCIA SRAM Memory Card — 68 pin, Type I	
Usable densities:	64 kByte 128 kByte 256 kByte 1 MByte (Cards larger than 1MByte can be used, but the PCM 91 will only make use of 1MByte.)
Access Time:	250 nsec or faster

Conforms to PCMCIA 2.0/JEDIA 4.1. Can use either 8-bit or 8/16-bit bus configuration. Attribute memory can be present, but is not used.

Periodic Maintenance

Under normal conditions the PCM 91 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

Ordering Parts

When ordering parts, identify each part by type, value and Lexicon Part Number. Replacement parts can be ordered from:

Lexicon, Inc.
3 Oak Park
Bedford MA 01730-1441
Telephone: 781-280-0300; Customer Serivce Fax 781-280-0499
ATT: Customer Service

Returning units for service

Before returning a unit, for warranty or non-warranty service, consult with Lexicon to determine the extent of the problem, and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If you choose to return a PCM 91 to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured, and consigned to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company name
- Street address
- City, State, Zip Code, Country
- Telephone number (including Area Code)
- Serial number of unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, both inside and outside of package

Please enclose a brief note describing conversations with Lexicon personnel and give the name and telephone number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Service personnel.

2

PCM 91 Specifications

Audio Input	**Connectors:**	Combined 3 pole XLR and 1/4 inch T/R/S phone jacks (2)
	Impedance:	0 dB/BAL switch position: 100kΩ, balanced -20 dB/UNBAL switch position: 50kΩ, unbalanced
	Levels:	0 dB/BAL switch position: -2 dBu min for full scale, +20 dBu max -20 dB/UNBAL switch position: -22 dBu min for full scale, 0 dBu max
	CMRR:	0 dB/BAL switch position: 50 dB minimum, 10 Hz to 20 kHz
Audio Output	**Connectors:**	1/4 inch T/R/S phone jacks (2); balanced XLRs, pin 2 "high" (2)
	Impedance:	100Ω, balanced
	Levels:	+18 dBm, full scale (+4 dBu setting) balanced, unbalanced +4 dBm, full scale (-10 dBu setting)
	Protection:	Relays provided for output muting during power on/off
A/D Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	<-65 dB, 10 Hz to 20 kHz
	S/N Ratio:	>102 dB, 20 kHz bandwidth
	THD:	<0.003%, 10 Hz to 20 kHz
	Dynamic Range:	>102 dB, 20 kHz bandwidth
	Delay:	24 samples (0.54 msec for 44.1 kHz, 0.50 msec for 48 kHz)
D/A Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	<-80 dB, 10 Hz to 20 kHz
	S/N Ratio:	>98 dB, 20 kHz bandwidth
	THD:	<0.005%, 10 Hz to 20 kHz
	Dynamic Range:	>98 dB, 20 kHz bandwidth
	Delay:	50 samples (1.13 msec for 44.1 kHz, 1.04 msec for 48 kHz)
A/A Performance	**Frequency Response:**	10 Hz to 20 kHz, ±0.5 dB
	Crosstalk:	<-55 dB, 10 Hz to 20 kHz
	S/N Ratio:	>96 dB, 20 kHz bandwidth
	THD:	<0.006%, 10 Hz to 20 kHz
	Dynamic Range:	>96 dB, 20 kHz bandwidth

Digital Audio Interface	**Connectors:**	Coaxial, RCA type (2); Balanced, XLR (2)
	Format:	S/PDIF (IEC-958) consumer and AES/EBU (AES3-1995) professional interface
	Sample Rates:	44.1 kHz, 48 kHz
Internal Audio Data Paths	**Conversion:**	20 bits
	DSP:	20 bits
External Memory Card	**Connector:**	Accepts PCMCIA Type I cards, 68 pins
	Standards:	Conforms to PCMCIA 2.0 / JEIDA 4.0
	Card Format:	Supports up to 1MB SRAM (attribute memory not required)
Control Interface	**MIDI:**	5-pin DIN connectors provided for MIDI IN, THRU, & OUT
	Footswitch:	1/4 inch T/R/S phone jack provided for 2 independent momentary footswitches System detects normal-open, or normal-closed on power up
	Foot controller:	1/4 inch T/R/S phone jack provided for footpedal (100Ω minimum, 10kΩ maximum impedance)
General	**Dimensions:**	19.0"W x 1.75"H x 12.0"D (483 x 45 x 305 mm) 19 inch rack mount standard, 1U high
	Weight:	Net: 6.4 lbs (2.9 kg) Shipping: 9.5 lbs (4.3 kg)
	Power Requirements:	100-240 VAC, 50-60 Hz, 35 W, 3-pin IEC power connector
	RFI/ESD:	Conforms to FCC Class B, EN55022 Class B (CE), IEC 801-2, IEC 801-3
	Environment:	Operating temperature: 32˚ to 104˚F (0˚ to 40˚C) Storage temperature: -22˚ to 167˚F (-30˚ to 70˚C) Humidity: maximum 95% without condensation

Unless otherwise noted, all audio specifications assume rear-panel switch set to BAL, input level control is set for unity gain (0dB), and analog I/O connections wired for balanced configuration.

Specifications subject to change without notice.

3

Performance Verification

Quick Performance Check

This section describes a quick verification of the normal operation of the PCM 91's internal processors and the integrity of the analog and digital audio signal paths. This procedure does not require extensive equipment or removal of the PCM 91 covers.

Diagnostics

There are two types of PCM 91 Diagnostics: Power Up Diagnostics and Extended Diagnostics. When the PCM 91 is powered up, the unit will automatically run the Power Up Diagnostics to verify proper operation of its internal system, and digital signal processors. When proper operation is confirmed, the unit exits the self-test mode and will briefly display:

Lexicon PCM 91
Version n.nn

This display is followed by the message: **Loading effect...** at which time the last effect used is loaded to the digital signal processors.

The following series of tests will be run automatically:

Host V40 CPU Test
ROM Checksum Test
Host (V40) SRAM Test
Display Test
Host (V40) Timer / Counter Test
Host (V40) Interrupt Test
Peak Detect Chip Test
Lexichip DRAM Test (X/Y)
Host (V40) DRAM Test
Battery Test
Audio Data Transfer Reg Test

When the unit is powered on, all front panel switch LEDs and all display pixels are turned on. The display pixels remain on for approximately two seconds, during which time the first four diagnostic tests are run. Once the Display test is completed, the message: **Memory Test** indicates that the rest of the tests are running. After completion of all of the tests, all the headroom LEDs are turned on briefly while the unit is initializing, and the message: **Lexicon PCM 91** is displayed. To access the Extended Diagnostics, simultaneously press and hold down the front panel **Control** and **Tempo** buttons while powering on the PCM 91. Hold down the buttons until the display reads:

PCM 91 Diagnostics
SELECT Test

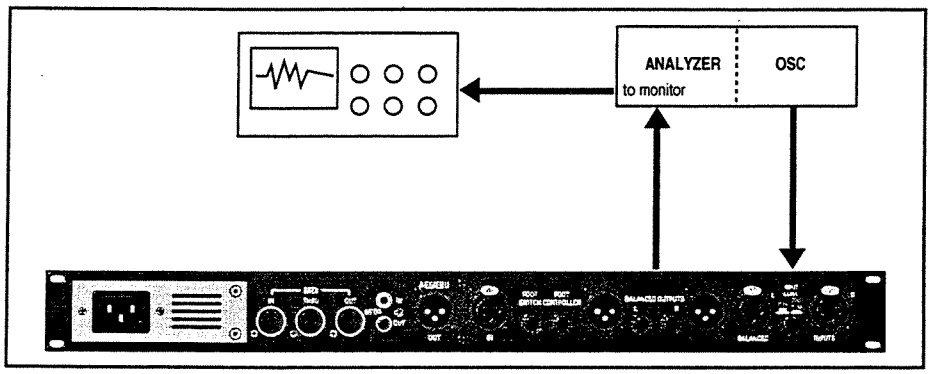
Detailed descriptions of the Power Up Diagnostics and Extended Diagnostics Tests are given in Chapter 4.

Analog Audio Performance Check

Required Equipment

- Low Distortion Oscillator with single-ended or balanced output,<100Ω output impedance, <0,005% THD.
- Distortion Analyzer and Level Meter with single-ended or balanced input, switchable 30 kHz high pass filter or audio bandpass (20-20 kHz) filter.
- Oscilloscope
- Audio Input Cable with shield and male XLR or 1/4" plug on one end (T/S for single-ended, T/R/S for balanced) and an appropriate connector on the opposite end for connection to Low Distortion Oscillator.
- Audio Output Cable with shield and female XLR or 1/4" plug on one end (T/S for single-ended, T/R/S for balanced) and an appropriate connector on the opposite end for connection to the Distortion Analyzer.
- Two (2) Audio Terminator Plugs, 1/4" with 600Ω-100kΩ resistor between tip and sleeve (single-ended configurations) or tip and ring (balanced configurations). An extra audio cable with a 1/4" connector at one end may be substituted if a termination plug is not available.

* Note all of the above tests use 1/4 phone jacks. To insure full and proper testing, perform all Audio tests using XLR jacks as well.



Setup

1. **Set Input Level**
   Turn on the PCM 91 on and wait for the Power Up Diagnostics cycle to finish.
   Load Program **P0 0.0 Deep Blue.**

   Press **Edit.** The display should read:
   Controls
   Mix 100%

   Turn SELECT to display:
   Controls InLvl
   FULL

2. **Set Audio*Input Source**
   Press **Control.** The display should read:
   Audio *Input Source
   0.0 Analog: 48kHz

   If 48kHz is not displayed, turn ADJUST.

3. **Set Output Level**
   Turn SELECT clockwise to select:

   Audio Output Level
   0.3 +4dBu

   If the Output Level is not set to +4dBu, turn ADJUST.

4. **Put PCM 91 into Bypass mode.**
   Press Down to display:

   System *Bypass Mode
   1.3 InputMute

   Turn ADJUST clockwise until the display reads:

   System *Bypass Mode
   1.3 Bypass

   Press the front panel Bypass button. The LED in the button should light and the message: **Bypass is on** should be briefly displayed.

5. **Connect the audio input cable between the Low Distortion Oscillator and the Left input of the PCM 91 and insert terminator plug.**
   As the PCM 91 automatically routes any audio signal present at either input to both Left and Right inputs, you must insert a terminator plug into the unused input jack to activate only one input channel.

6. **Select balanced or unbalanced input switch.**
   Set the PCM 91 rear panel switch out for input requiring 0dB gain. Push the switch in to test unbalanced input requiring +20dB gain.

7. **Connect the audio output cable between the PCM 91 Left Output and the Distortion Analyzer.**

8. **Insert an audio terminator plug into the PCM 91 Right Output jack.**

Check Signal Levels

1. Apply a 1kHz sinewave signal to the left input at +20dBu=7.75Vrms for balanced (0dBu=0.775Vrms for unbalanced).

2. Measure the Left output level:
   - Connect the Oscilloscope to the Monitor jack of the Distortion Analyzer.
   - Set the Analyzer to voltmeter mode
   - Turn the PCM 91 front panel Input Level knob up full (completely clockwise). The signal on the oscilloscope will be clipping.
   - Slowly turn the Input Level knob counterclockwise until the signal is just below clipping. Note this setting as you will be reminded to return to it in the following tests.

3. Switch the Distortion Analyzer back to level and read the Left output measurement. Acceptable levels are between +18.5 and +21.5dBu.

4. On the PCM 91, press **Control** then turn SELECT to display **Output Level**. Turn ADJUST to display **-10dBu**.

5. Measure the Left output again on the Distortion Analyzer. The reading should be between 7.5 and 4.5dBu .

6. Swap the I/O and terminator connectors, reset the PCM 91 **Audio Output Level** to **+4dBu** , and repeat steps 2-5 for the right output .

Frequency Response Measurement

1. Apply a 1kHz +20dBu sinewave signal to the right input of the PCM 91. Turn the PCM 91 front panel Input Level to the position established as being just under clipping .

2. Measure the right output and set the Analyzer for 0dBr reference.

3. Turn off all filters on the Analyzer.

4. Sweep the Oscillator from 10Hz to 20kHz.

5. The right output should vary less than ±0.5dB, referenced to the 1kHz output level.

6. Swap the I/O and terminator connectors and repeat steps 1-5 for the left output.

THD+N Measurement

1. Apply a 1kHz +20dBu sinewave signal to the left input of the PCM 91. On the Analyzer the only filter used should be in the range of 20Hz to 20kHz of audio bandpass, or 30kHz low pass filters can be used.Turn the PCM 91 front panel Input Level to the position established as being just before clipping .
2. Set the PCM 91 **Audio Output Level** to **+4dBu**.
3. Measure the Left output THD+Noise level on the Analyzer, for a reading of <0.008 %
4. Swap the I/O and terminator connectors on both inputs and outputs and measure THD+Noise level for the right output <0.008 %

Signal To Noise Ratio

1. Apply a 1kHz +20dBu sinewave signal to the right input of the PCM 91. Turn the PCM 91 front panel Input Level to the position established as being just before clipping .
2. Set Analyzer to dB Ratio and zero it for a reference level. Turn off the oscillator output and measure the right output. The reading should be greater than a 90dB ratio.
3. Swap the I/O and terminator connectors and repeat on the left output.

Digital I/O Test

The following two tests confirm the PCM 91 S/PDIF and AES/EBU digital input and output ports.

S/PDIF Test

The S/PDIF circuit is verified with an on-board wraparound test in the Extended Diagnostics.

1. Connect an RCA cable between the PCM 91 S/PDIF IN jack and the S/PDIF OUT jack.
2. Press and hold the front panel **Control** and **Tempo** buttons while powering up the PCM 91. Continue to hold down the buttons until the display reads:

   PCM 91 Diagnostics
   SELECT Test
3. Turn SELECT until the display reads: **Dig Aud IO Wrap Test**
4. Press **Load**. The lower half of the display should read: **WAIT! Executing Test**

If the test passesthe display will read: **PASSED.** If it fails the display will read: **FAILURE.**

AES Test

The following test, which verifies the AES/EBU ports, requires a second PCM 91, or another device that can transmit and receive AES/EBU formatted signals.

1. Place the two devices one on top of the other. Connect power to each and power on.
2. Attach XLR cables between the AES/EBU inputs and outputs of both units.
3. On the PCM 91 you are testing, press **Control** and select

   Audio*Word Clock
   Analog: 44.1kHz

4. Turn ADJUST tol change the display to::

   Audio*Word Clock
   Ext:XLR Prf 44.1

   This verifies that the PCM 91 under test is receiving a 44.1kHz digital signal from the other device.
5. To test the 48kHz path, set the transmitting device to 48kHz. The PCM 91 display should read:

   Error:Lock
   (Press any button)

6. Press any button on the PCM 91 front panel to have the PCM 91 attempt to lock to the incoming signal. If lock is successful, the PCM 91 display should read:

   Audio*Word Clock
   0.0 Ext:XLR Prf 48

Footpedal Functionality

Before performing this test, press **Control**. Use **Up** and **Down** and SELECT to locate matrix postion **1.0 Edit Mode**. Use ADJUST to set the mode to **Pro**.

1. Connect a footpedal to the PCM 91 rear panel Foot Controller connector.
2. Press **Program Banks** to select Bank **P0**. Turn SELECT to display:

   Halls: Orchestral
   P0 0.0 Deep Blue

3. Press **Load/*** to load **P0.0 Deep Blue**.
4. Press **Edit**. The display should read:

   Controls Mix
   S.O 100%

5. Press **Up** until the display reads:

   Patch 0 *Src
   Int Adjust

6. Turn ADJUST counterclockwise until the display reads

   Patch 0 *Src
   Int Footpedal

7. Press **Load/*** to display:

   Patch 0 *Dst
   Time Mid Rt

8. Turn ADJUST counterclockwise todisplay:

Patch 0	***Dst**
Controls	**Mix**

9. Press **Down** until the isplay reads:

Controls	**Mix**
S.0	**24%**

10. Press the footpedal up and down and verify that the wet value goes between 24 and 87%

Footswitch Functionality

1. Connect a dual footswitch with a 1/4" tip-ring-sleeve plug into the PCM 91 rear panel Footswitch connector. These tests can also be done with a single footswitch with a mono 1/4" tip-sleeve plug inserted half-way in to test Footswitch 1, then inserted completely to test Footswitch 2.
2. Press **Control**. Use **Up** and **Down** and SELECT to locate matrix position **1.3 * Bypass Mode**.
3. Press **Load/*** to display the parameter **Bypass Src**.
4. Use ADJUST to select **Foot Sw 1**.
5. Press the first footswitch. The Bypass light should toggle from off to on, or on to off.
6. Use ADJUST to select **Foot Sw 2**.
7. Press the second footswitch. The Bypass light should toggle from off to on, or from on to off.

After finishing this test, use ADJUST to select **Off** (and leave Bypass in its Off default state).

Listening/Q.C.

Required Equipment

- Clean, antistatic, well lighted work area
- Low Distortion sine wave oscillator
- Headphone Amplifier
- (4) 1/4" to 1/4" stereo phone plug cable (3 ft. minimum)
- Two 1/4" female to 1/4" male Y-adapter cables
- Stereo Headphones

Setup

1. Use two audio cables and a Y-adapter to connect the output of a low distortion sine wave oscillator to the left and right audio inputs of the PCM 91.
2. Use 2 cables to connect the headphone amp inputs to the PCM 91 outputs.
3. Set the oscillator to 220Hz at –45dBV.
4. Turn the volume control on the headphone amplifier all the way to minimum (fully counterclockwise) and plug in the headphones.

5. Set the Input Level switch on the rear panel of the PCM 91 to the IN position (-20dB).
6. Power up the PCM 91. Press **Program Banks** repeatedly to select Program Bank 0 (**P0**).
7. Turn the SELECT knob to display:

   Hall: Orchestral

   P0 0.0 Deep Blue
8. Press **Load/*.** (Make sure **Bypass** is OFF.)

Verify Clean Audio

1. Put the headphones on.
2. Set the PCM 91 INPUT control fully clockwise.
3. Slowly increase the volume on the headphone amplifier until it's at a comfortable listening level.
4. Adjust INPUT over its entire range.
5. Verify that no pops, clicks or scratchiness are heard when turning the pot.
6. Adjust PCM 91 INPUT so the peak level just turns on the –6dB (yellow) headroom LED.
7. Adjust the volume on the headphone amplifier to a comfortable listening level.
8. Mute and unmute the signal source at different frequencies. Carefully listen to the outputs for grossly unusual noise, audible distortion or other gross audio irregularities through entire decay time of the reverb.

Shock Test

1. Lift each corner of PCM 91 four inches off of the workbench and drop.
2. Verify that no audio or display intermiitents are caused by this action.

KEEP ONE CORNER OF UNIT TOUCHING THE BENCH AT ALL TIMES TO PREVENT DAMAGE TO THE UNIT

MIDI Functionality

PCM 91 Extended Diagnostics will verify the integrity of the MIDI circuit function.

1. Plug one end of a MIDI cable into the PCM 91 rear panel MIDI IN jack and the other end into the MIDI OUT jack
2. Power up the PCM 91 while pressing **Control** and **Tempo**. Continue pressing both buttons until the display reads:

   PCM 91 Diagnostics
   SELECT Test
3. Turn SELECT clockwise until the display reads: **MIDI Test.**
4. Press **Load/*** to display: **WAIT: Executing Test.** If the test runs successfully, **PASSED** is displayed.

4

Troubleshooting

Diagnostics

The PCM 91 contains two types of diagnostics: Power Up Diagnostics and Extended Diagnostics. Power Up Diagnostics are executed automatically on system power up. Extended Diagnostics are accessed by powering up the PCM 91 while holding down the front panel **Control** and **Tempo** buttons. Release the buttons when the display reads:

PCM 91 Diagnostics
SELECT Test

To facilitate interpretation of diagnostic results, the diagnostic operating system is kept as simple as possible, and the watchdog timer is inoperative.

Power Up Diagnostics

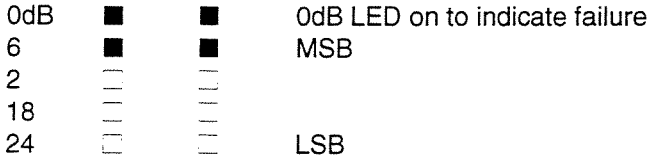
Power Up Diagnostics are automatically executed on power up. Before any tests are executed, all front panel switch LEDs are turned on. These remain on until all Power Up Diagnostics are completed. If all tests pass, the display will read: **Lexicon PCM 91...** . If any test fails, an error message such as **E8** will be displayed and the 0dB headroom LED will light to indicate the failure. (The lighting of headroom LEDs in addition to 0dB are explained in detail later in this document.)

As the Power Up Diagnostics begin, all display pixels will be turned on for approximately two seconds while the first four tests are executed. Following the Display test (4), the message:

Memory Tests

is displayed for the duration of the remaining tests. Power Up Diagnostics take approximately 25 seconds to run. If the unit is being turned on for the first time, following reinitialization, a more thorough and more time consuming memory test will be performed. You can elect to have this extended version of the Power Up Diagnostics run by pressing the front panel **Compare** button prior to power on. This extended version takes approximately 45 seconds to run. All error messages for normal and extended Power Up Diagnostics are identical.

Test codes which are binary numbers representing each test are displayed on the headroom LEDs just before each test is executed to allow identification of failed tests if the unit hangs or crashes during the test. The following is an example of a test code on the headroom LEDs:



Binary Code 8 (1000) Lexichip DRAM Test. While this, or any other, test is being executed, the front panel display will read: **Memory Tests.**

The following table shows the Power Up Tests in the order in which they are executed, along with the corresponding test codes, error messages and failure codes. Hexadecimal numbers representing failure codes are stored in an Error Log, described later in this section.

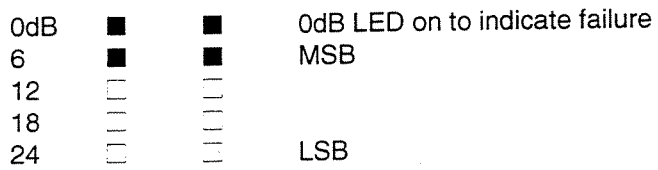
	Test	Error Message	Error Log # (Hex)
1	Host V40 CPU Test	E1	01
2	ROM Checksum Test	E2	02
3	Host (V40) SRAM Test	E3	03
4	Display Test	E4	04
5	Host (V40) Timer/Counter Test	E5	05
6	Host (V40) Interrupt Mask Test	E6	06
7	Peak Detect Chip Test	E7	07
8	Lexichip DRAM Test (X/Y)	E8	08
9	Host (V40) DRAM Test	E9	09
10	Battery Test	Replace Battery Soon	0A
11	Audio Data Transfer Reg Test	E11	0B
NA	Undetermined Error*	NA	FF

*Undetermined Errors (FFH), occur when the V40 (U46) CPU tries to load code from the V40 ROM to the Slave Z80 SRAM and to the Lexichip. This failure indicatesa faulty link between the Host and the Z80 bus.

The Lexichip DRAM and the Host DRAM tests are simultaneously executed by independent CPUs to shorten the total Diagnostics execution time.

Diagnostic Failures

Failures cause the red 0dB LEDs to turn on, and a binary error code to be displayed on both headroom LED columns. The LED error codes are 4-bit binary numbers with the -24dB LED representing the LSB, and the yellow -6dB LED representing the MSB as shown below.



Binary Code 8 (1000)

This code indicates failure of the Lexichip DRAM Test. In addition to the headroom display, a number is displayed on the front panel to indicate which test failed. For example, **E8** indicates that the Lexichip DRAM test failed. Information about the failure is stored in an error log file in SRAM for future analysis.

Failure of any test will halt the test series. To continue to the next test, press **Load/*** . The unit will proceed to the next test and halt again. Continuing to press **Load/*** .after each test will allow you to finish executing the Power Up Diagnostics but the system will not become operational. At this point, you have three options:

1. Press **Load/*** again to continue the power cycle. (This option is not available if the CPU test has failed.)

2. If failure occurred in the CPU, ROM or SRAM test, press **Down** to enter a special diagnostic test loop which walks ones and zeros through the Address and Data bus. (For more information about the diagnostic test loop, refer to the description of the Host V40 CPU Test.

3. After pressing **Load/*** , you can access the Extended Diagnostics error log. (See Error Log and Failure Viewing Mode.)

NOTE: CPU test failures are not stored in the error log. Failures of the ROM and SRAM tests are not stored unless **Load/*** is pressed to progress beyond the SRAM test. Depending on the seriousness of the problem, data may not be stored or the unit may crash.

If the unit hangs during Power Up Diagnostics, it will generally be during a test execution with no display error message or LED indicator. Although the headroom binary code will indicate a test code, do not depend on this for verification of the problem.

Bypassing the Diagnostic Failure Lockup

If problems arise during the Power Up Diagnostics cycle, the unit will not boot into the main system. Pressing **Load/*** will display the message:

DIAGNOSTIC FAILURE
OCCURRED

Simultaneously press **Control** and **Tempo** to access the Extended Diagnostics. The display will show:

PCM 91 Diagnostics
SELECT Test

Simultaneously press **Up** and **Tempo** to display:

WARNING!
DO NOT CONTINUE

Simultaneously press **Down** and **Tap** to bypass the failure message and continue the boot sequence.

Bypassing error messages can result in excessive speaker excursion and/or loss of user register data.

Error Log and Failure Viewing Mode
All failures that occur are recorded in a 20 record ring buffer (First In First Out — FIFO) called the Error Log. From the Extended Diagnostics, turn SELECT or press **Up** or **Down** until the display reads: **Show Error Log**, then press **Load/ ✱** to access an error log as shown.

XXXXXXXX YYYYYYYY
AAAAAAAA TT

Each record in the log consists of 5 elements, represented above as #, X, Y, A and T.

A test number, which identifies which test failed.

X The tested value. For example, in the case of a Host DRAM Test failure, the value 000000AA might indicate that the CPU wrote that pattern to the DRAM. A value of 00000000 could indicate that the CPU tried writing all zeros to the DRAM, or it could mean that the value is not applicable for the type of failure that occurred, such as timeout failure.

Y The failed value. In the case of a Host DRAM Test failure, the value 0000002A might indicate a problem with bit 7 on the Host Data Bus, or a possible problem with the DRAM. A value of 00000000 could mean that the value is not applicable for the type of failure that occurred, such as timeout failure.

A Address/location where failure occurred. In case of a Host DRAM Test failure, the address might be 00000000 which is where the DRAM is located. A value of 00000000, could also indicate mean that the value is not applicable for the type of failure that occurred, such as timeout failure.

T Type of failure. In the case of a Host DRAM Test, 01 would indicate a data type of failure. (Refer to failure code descriptions in the next section.)

The first log entry will be the last error which occurred. Pressing **Up** or **Down** will scroll backward through the 20 failure records. Press **Load/✱** . to exit the error log.

Note: Accessing the error log when a failure occurs involves less risk of destroying user registers or crashing the unit than continuing the boot cycle.

The following table shows failure types (T). Remember that CPU failures are never be stored, as the unit will suspend operation due to the seriousness of the problem. ROM and SRAM failure information will not be stored unless the SRAM test is been completed.

Error Log Failure Codes

Display	Hex	Description
0	00H	Unknown / No failure
1	01H	Data failure (Indicates that failure happened, for example during RAM Data test)
2	02H	Address failure (Indicates that failure happened during RAM Address test)
3	03H	Timeout failure (Occurs if there is no response from the co-processor or if a test is taking too long.)
4	04H	No RAM size information available
5	05H	Wrong RAM size
6	06H	Data transfer failure
8	08H	CPU failure
9	09H	Slave Z80 loading the Lexichip WCS failed
10	0AH	Data transfer to Slave Z80 SRAM failure
12	0CH	MIDI Test timeout failure, Transmit buffer didn't get emptied*
13	0DH	MIDI Test timeout failure, Receive buffer didn't get filled*
14	0EH	MIDI Test data transfer error detected by the Serial Control Unit*
15	0FH	MIDI Test transmitted data vs. received data mismatch*
16	10H	MIDI Test Transmit interrupt failed*
17	11H	MIDI Test Receive interrupt failed*
18	12H	PCMCIA Card Test, No card installed*
19	13H	PCMCIA Card Test, Write Protect is on*
20	14H	PCMCIA Card Test, Backup battery voltage is too low*
21	15H	PCMCIA Card Test, Bank switching failed*
22	16H	PCMCIA Card Test, Attribute register failed*
23	17H	PCMCIA Card Test, Transferring code from card to DRAM failed*
24	18H	Foot controller ADC test failed (Requires special test fixture)*
25	19H	Watchdog Timer Test failed, timed-out too soon*
26	1AH	Watchdog Timer Test failed, failed to time-out*
28	1CH	Stack failure during Watchdog Timer test (Software related)
29	1DH	The Z80 did not initialize the mailbox and has ikely crashed*
30	1EH	48 kHz Word Clock frequency is too high*
31	1FH	48 kHz Word Clock frequency is too low*
32	20H	44.1 kHz Word Clock frequency is too high*
33	21H	44.1 kHz Word Clock frequency is too low*
39	27H	The Digital Audio Receiver is locking to a data stream that shouldn't be there
40	28H	The Digital Audio Receiver is detecting a word clock frequency outside the 48kHz +/ - 400 PPM tolerance. Note: The receivers reference clock is the 48kHz crystal oscillator for the transmitter chip
41	29H	The Digital Audio Receiver is detecting a word clock frequency outside the 44.1kHz +/- 400 PPM tolerance. Note:The receivers reference clock is the 48kHz crystal oscillator for the transmitter chip
42	2AH	The Digital Audio Receiver is detecting Professional Audio coming in instead of Consumer
432	40H	The Digital Audio Receiver detected an error by setting the ERF signal high
44	41H	The Digital Audio Receiver detected a Validity error
45	42H	The Digital Audio Receiver detected a Confidence error
46	43H	The Digital Audio Receiver detected a Slip Sample error
47	44H	N/A (The Digital Audio Receiver detected a CRC error)
48	45H	The Digital Audio Receiver detected a Parity Error
49	46H	The Digital Audio Receiver detected a Bi-Phase Error
50	47H	The Digital Audio Receiver detected a No Lock Error

* Tests residing in the Extended Diagnostics. Note that the failure codes are different for the Host (V40) Timer/Counter Test.

Power On Diagnostics Active Buttons

During the power up test sequence, the front panel buttons are scanned. These buttons must be pressed when the PCM 91 is powered on and released when all the front panel display pixels are turned off.

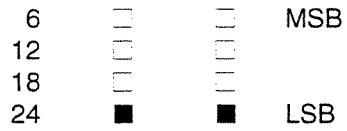
Press	Action Taken
Up and **Bypass**	Bypasses some of the diagnostics and speeds up the boot cycle — reduces the boot cycle by 5 seconds.
Compare	Initiates extensive Lexichip DRAM (X&Y) and Host DRAM tests. This test will take about 45 seconds (approximately 20 seconds longer than the normal diagnostics test sequence.
Up and **Control**	Loops the diagnostics test sequence until the unit is turned off.
Control and **Tempo**	Activates the Extended Diagnostics. Displays the message: **PCM 91 Diagnostics** **Select Test** Pressing these buttons when a ROM or SRAM test failure occurs will activate the Extended Diagnostics. **WARNING! Depending on the seriousness of the failure, data stored in the registers could be lost if you opt to ignore the failure message and continue.** In order for the Extended Diagnostics to work, certain parts of the system (V40-CPU, ROM, SRAM, Host DRAM, and card interface) must be working. Press **Control** and **Tempo** when the message: **DIAGNOSTIC FAILURE OCCURRED** is displayed to access Extended Diagnostics.
Up and **Tempo**	Pressed when the message: **DIAGNOSTIC FAILURE OCCURRED** is displayed to ignore the error message. **WARNING! Bypassing this error message is not recommended.** Press **Control** and **Tempo** when the message: **DIAGNOSTIC FAILURE OCCURRED** is displayed to access Extended Diagnostics.
Load/*	Ignores a failure and continues the boot cycle
Down	Available when the V40 CPU, ROM and/or SRAM tests fail, activates a special test that keeps the Host Data and Address bus active.
Down and **Tap**	Initializes PCM 91 to factory settings. **WARNING! This action erases the user setup and the diagnostic failure log by clearing the memory (SRAM).** The Message: WARNING! Press STORE to clear the SRAM is displayed. Press **Store** to clear memory and display the message: **SRAM Cleared /Press any button to continue.** Pressing any button reboots the system. Pressing any button other than **Store** will display the message: **SRAM Clear cancelled**, and the already started boot cycle will continue without clearing the memory.

Power Up Diagnostics Test Descriptions

1 Host V40 CPU Test

This test verifies if there are any stuck CPU register bits. The V40 (U34) Host processor tries to pass the value 55AAH through its internal registers. In second pass, the data is inverted to AA55H and passed through the registers. If an error is detected, an attempt is made to write an error code to the front panel headroom LEDs and the boot cycle will be halted.

Before the test is executed, the following binary code is displayed on the headroom LEDs:



If failure occurs, the 0dB (red) LEDs are turned on in an addition to the binary code.

If a CPU error occurs, pressing **Down** will enter the test loop. In addition to reading data from the ROM, the V40 writes a walking "1" value to location 0000H in the SRAM. (Mapped to B0000H). By using an oscilloscope and triggering on the HMWR/ pulse, verify that all the data lines are connected to all the devices and that there are no shorts. If there is a problem with the data bus and/or the address bus between the V40 CPU and the ROM, the unit will not boot at all.

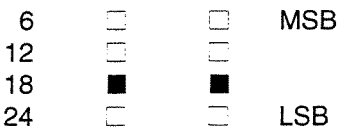
A walking "1" test on the address bus is performed by rotating a "1" through the CPU registers and reading the location pointed to by these registers. If the CPU registers used by this test are broken, the test will not work as intended.

Given the gravity of a CPU error, it is doubtful that the program will reach the test loop. The only way to exit the test loop is by power cycling the unit.

No failure log is generated or stored.

2 ROM Checksum Test

The ROM checksum, which is a byte size value, is located as the last byte in the ROM (U55). The test adds up the entire ROM including the Checksum byte. The result should be 0 (8 bit value.)



Pressing **Load/*** in response to a ROM checksum test failure will allow you to proceed to the next test. The failure will not be stored in the error log until just before the Display Test is executed.

Pressing **Control** and **Tempo** to access Extended Diagnostics is a risk as a checksum error indicates that the program in the ROM is wrong or that a problem exists with some of the address lines. Therefore, the diagnostic system may or may not work and may destroy the user registers. Note that no data other than the test number is stored in the failure log.

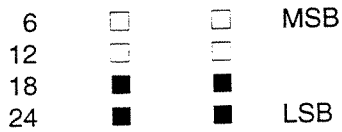
Pressing **Down** will start executing the same test loop described in the CPU test. The unit must be power cycled to exit the test loop.

Failure log:

Test number	2
Tested value	N/A
Failed value	N/A
Address/location	N/A
Type of failure	N/A

3 Host (V40) SRAM Test

This SRAM test does not touch the volatile SRAM area (where register and other system information is stored). It does nondestructive testing in the first 4k of the SRAM (U54). The nondestructive test reads one location and stores it in a CPU register. Then it does a walking "1" test at that location followed by a walking "0" test at the same location. The test location is incremented by one until the end of the diagnostic SRAM area is reached. Since the SRAM is used as a temporary stack until the DRAM has been proven OK, a destructive counting test is done on the area where the temporary stack is located (approx. the first 200H bytes) The stack is not used until after the SRAM Test to ensure address independence in the temporary stack area.



Pressing **Load/*** in response to an SRAM test failure will allow you to proceed to the next test. The failure will not be stored in the error log until just before the Display Test is executed.

Pressing **Control** and **Tempo** to access Extended Diagnostics is a risk as the program stack is probably not operational. Therefore, the program will crash is likely to destroy the user registers. Note that no data other than the test number is stored in the failure log.

Pressing **Down** will start executing the same test loop described in the CPU test. The unit must be power cycled to exit the test loop.

Failure log:

Test number	3
Tested value	N/A
Failed value	N/A
Address/location	N/A
Type of failure	Address or Data

4 Display Test

This test checks the display busy bit (DISPBSY at U33 pin 9) by writing a "reset" display command to the display. The test verifies if the display busy signal is activated and then deactivated again. If that doesn't take place, a failure is reported. Maximum busy time is specified as 45µs.

6	■	■	MSB
12	□	□	
18	□	□	
24	□	□	LSB

Error information is stored in the failure log automatically when failure occurs. Press **Load/*** to proceed to the next test.

Failure log:

Test number	4
Tested value	N/A
Failed value	N/A
Address/location	N/A
Type of failure	N/A

5 Host (V40) Timer / Counter Test

The timer/counter test checks the 3 V40 (U34) internal counters, verifying that the status registers and the count registers don't have any stuck bits.

6	□	□	MSB
12	■	■	
18	□	□	
24	■	■	LSB

NOTE: Failure of this test has a totally different meaning than in other tests. See below.

Failure log:

Test number	5
Tested value	N/A
Failed value	N/A
Address/location	N/A
Type of failure	Bit 0 = Timer 0 Status test failed if 1 Bit 1 = Timer 1 Status test failed if 1 Bit 2 = Timer 2 Status test failed if 1 Bit 4 = Timer 0 Counter test failed if 1 Bit 5 = Timer 1 Counter test failed if 1 Bit 6 = Timer 2 Counter test failed if 1

6 Host (V40) Interrupt Mask Test

This test is limited to the internal V40 (U34) interrupt controller mask register. The register will be tested by a marching "1" and a marching "0" test.

6	□	□	MSB
12	■	■	
18	■	■	
24	□	□	LSB

Failure log:

Test number	6
Tested value	Expected written data
Failed value	Actual read back value
Address/location	N/A
Type of failure	N/A

7 Peak Detect Chip Test

This tests the Peak Detect Chip (U15 DSP) by writing audio data sequences to it via Lexichip X. Peak information is checked via Slave Z80 X as well as the host.

This test checks the four Peak Accumulation Registers of the Peak-Detect Chip: PAR0, PAR1, PAR2, and PAR3. Several groups of value sequences are written to each of the Peak Accumulation registers. Both positive peaks and negative peaks are checked. If an error occurs, expected and actual data values are displayed. Also the address field displays which Peak Accumulation Register failed.

6	□	□	MSB
12	■	■	
18	■	■	
24	■	■	LSB

Error information is stored in the failure log automatically when a failure occurs. Press **Load/*** to proceed to the next test.

Failure Log:

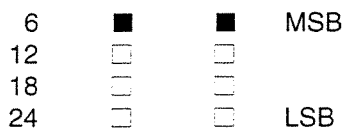
Test Number	07
Tested Value	Expected data written
Failed Value	Actual value read
Address/location	0=Peak Accumulation Register 0 failed 1=Peak Accumulation Register 1 failed 2=Peak Accumulation Register 2 failed 3=Peak Accumulation Register 3 failed

8 Lexichip X and Y DRAM Test

This tests the 256Kx20 DRAM of Lexichip X and of Lexichip Y respectively. Lexichip X's DRAM is implemented with a 256Kx16 DRAM (U12 DSP) for the 16 most significant audio data bits,and a 256Kx4 DRAM (U8 DSP) for the 4 least significant audio data bits. Lexichip Y's DRAM is implemented with a 256Kx16 DRAM (U27DSP) for the 16 most significant audio data bits, and a 256Kx4 DRAM(U28 DSP) for the 4 least significant audio data bits. If there is a DRAM chip or connectivity failure, the error information loggedby this test should isolate the problem.

This test is primarily performed by Slave X Z80. Data writing and fetching is performed by the Lexichip X from which data ispassed from and to the Slave Z80 respectively. The Host V40 CPU is responsible for loading this test code to the slave Z80, and for logging test results.

To save test time, the Lexichip X DRAM test and the Lexichip DRAM test are started at the same time. While they are running, the host also concurrently executes the Host DRAM test. After that, error checking is then done for the Lexichip X DRAM test first, then for the Lexichip Y DRAM Test.



Error information is stored in the failure log automatically when a failure occurs. Press **Load/✱** to proceed to the next test.

The following two Headroom LED display codes indicate the status of the Lexichip X & Y DRAM Test:

DRAM Test Running
DRAM Test Failure

Error information is stored in the failure log automatically when a failure occurs. Press **Load/✱** to proceed to the next test.

Failure Log:

Test Number	08
Tested Value	Expected data written
Failed Value	Actual value read
Address/location	Address of first bad location

The most significant bit indicates whether it was Lexichip X DRAM or Lexichip Y DRAM that failed.
Specifically:

0xxxxxxx indicates that Lexichip X DRAM failed
8xxxxxxx indicates that Lexichip Y DRAM failed
Type of Failure Various

9 Host (V40) DRAM Test

The Host DRAM test is executed by the V40 (U34) CPU while it is waiting for the other CPUs to complete their respective DRAM tests. As with the other DRAM tests, two versions are available. A simpler and quicker version is executed under normal conditions. The other version, which is more thorough and more time consuming, is initiated : when the unit is powered on for the first time in manufacturing, when **Compare** is pressed during power-on, or when the SRAM has been cleared.

6	■	■	MSB
12	□	□	
18	□	□	
24	■	■	LSB

Error information is stored in the failure log automatically when a failure occurs. Press **Load/*** to proceed to the next test.

Failure log:

Test number	9
Tested value	Expected written data
Failed value	Actual read back value
Address/location	Address of first bad location
Type of failure	Various

10 Battery test

The Host CPU reads the battery low indicator and, if there is a "low" reading, the information is saved for the main operating system which takes care of informing the user of low battery status. The boot cycle is not discontinued on a low battery condition. More than one reading is done because there is no hysteresis built into the monitoring circuitry. When the battery voltage is close to the trigger level of the comparator, the comparator could start oscillating.

6	■	■	MSB
12	□	□	
18	■	■	
24	□	□	LSB

No failure log is generated or stored but, after the power up diagnostic sequence is completed, the display will read:

Replace Battery Soon
(Press any button)

11 Lexichip Audio Data Transfer Register Test

This tests the integrity of the audio data transfer registers between Lexichip X and Lexichip Y. Test patterns are written and checked in each direction, from X to Y, and Y to X. The Lexichip X passes data patterns sourced by Slave Z80 X to the X-to-Y Transfer Registers, and they are read by Lexichip Y and finally checked by Slave Z80 Y. Similarly, Lexichip Y passes data patterns sourced by Slave Z80 Y to the Y-to-X Transfer Registers, and they are read by Lexichip X and finally checked by Slave Z80 X. Error information is passed to the host V40 to display test information.

Error information is stored in the failure log automatically when a failure occurs. Press **Load/*** to proceed to the next test.

Failure Log:

Test Number	0BH
Tested Value	Expected data written
Failed Value	Actual data read
Address/location	Address of first bad location

The most significant bit indicates whether it was X-to-Y or Y-to-X Transfer Register that failed. Specifically:

0xxxxxxx indicates that X-to-Y Transfer Register failed
8xxxxxxx indicates that Y-to-X Transfer Register failed
Type of Failure: Various

Extended Diagnostics

The Extended Diagnostics Tests and Troubleshooting Tools are accessed by powering up the PCM 91 while holding down the **Control** and **Tempo** buttons on the front panel. Release the buttons when the display reads:

PCM 91 Diagnostics
SELECT Test

Turn SELECT to scroll through the tests and tools listed below. Press **Load/*** to enter the test.

Encoder Test
Switch Test
LED Test
Display Char Test
Display Block Test
PCMCIA Card Test (#0DH)
Auto Test Execution
Foot Cntrl. ADC Test (#0EH)
MIDI Test # (0CH)
Slave Z80 SRAM Test (#14H)
Watchdog Timer Test (#0FH)
Word Clock Select Tst (#10H)
Slave To Host Interrupt Test (#16H)
Digital Audio I/O Through
Infinite Test Loop
Show Error Log
Clear Error Log

The following tests require technician interaction and judgment. No test number is assigned as these tests do not generate error messages stored in the Error Log File.

Encoder Test (the ADJUST and SELECT knobs are only used)
Switch Test
LED Test
Display Char Test
Display Block Test

Extended Diagnostics Test Descriptions

Encoder Test

This test verifies the operation of the front panel encoders (ADJUST and SELECT) including correct sequence and ID. The test displays the encoder name and the bit pattern status of the encoders. It also displays a cumulative value which increments or decrements depending on the rotational direction. Press **Load/*** to exit the test.

Switch Test

This test verifies the operation of the twelve front panel buttons, and the two rear panel footswitch and two audio output jacks. Two 1/4" phone plugs should be connected to the audio output jacks during this test. If phone plugs are not connected to these jacks, the bottom half of the display will read **Single Aud Out Jack** when no switches are being tested.

When a button or a footswitch is pressed, the bottom half of the display will read **Pressed** next to the button name. When the button is released, the display will read **Press Any Button**. The same approach is used for the Footswitches. When either or both of the phone plugs are removed from the audio output jacks, the bottom half of the display will read **Single Aud Out Jack**. This verifies that the mono audio output feature is working.

To exit the test, press and hold down **Load/*** for five seconds or until the display goes blank.

LED Test

This test verifies operation of all the LEDs (D101-122). When the test is first executed, all the headroom and button LEDs are lit. Turn ADJUST clockwise, or press **Up** to individually light each LED. After testing the **Bypass** LED (when testing in a clockwise sequence) no LEDs are lit. Turn ADJUST one more position clockwise to light all LEDs again. Turn ADJUST counterclockwise or press **Down** to reverse the sequence. Press **Load/*** to exit .

Display Character Test

This test displays a single character at each of the 40 display character positions. The character displayed can be changed by turning ADJUST or pressing **Up** or **Down**. All of the letters in the alphabet and some other ASCII characters are available. The point of this test is to provide a display that allows the technician to easily pick out display problems and to control the activity on the driver lines for easier troubleshooting. Press **Load/*** to exit .

Display Block Test

This test turns on all the pixels of a single display character with all of the other characters off. When ADJUST is turned, or **Up** or **Down** is pressed, the lit character increments or decrements, effectively walking the block. When the position jumps from the last position to the first, or vice-versa, the display is filled with a block character. This is another tool for checking and troubleshooting the display. When used in conjunction with the character test, most display problems can be easily identified and debugged. Press **Load/*** to exit .

PCMCIA Card Test (0D)

This test requires a 1 Meg card with Attribute Register. The test verifies that all the Data lines (D0-D7), all the Address lines (A0-A15, CA16-CA19) and control lines work as intended. The test does not verify the card itself.

Turn SELECT to display **PCMCIA Card.** Press **Load/*** to enter the test. Verify that the display reads:

PCMCIA Card Test
INSTALL Test Card

Install a memory card in the PCM 91, Press **Load/*** and verify that the display reads: **Passed.**

If there are problems with any of the control lines, the display will indicate what test has failed, and the test will not continue until the problem has been repaired. Press **Load/*** to discontinue testing. Once testing is completed, remove the Memory Test Card from the Memory Card Slot.

Error report:

Test number	(0DH)
Expected data	8 bits
Actual read data	8 bits
Address location	20 bits, shows where failure occurred if applicable

Type of failure (data, address, control signals)

Auto Test Execution

This automatic test series requires a MIDI Cable connected between PCM 91 MIDI OUT and MIDI IN and a special Foot Controller Test Fixture (Lexicon part #770-08508) connectedto the Foot Controller Input Jack.

The following tests are run:

- Foot Cntrl. ADC Test (0EH)
- MIDI Test (#0CH)
- Slave To Host Interrupt Test (#16H)
- Watchdog Timer Test (0FH)
- Word Clock Select Tst (#10H)
- Slave Z80 SRAM Test (#14H)

If a failure occurs, the Auto Execution Test will halt on the test that failed, display the name of the test on the top half of the display and display **Failure** on the bottom half of the display. Pressing **Load/*** will allow the test series to continue, but the **Failure** message will remain on the bottom half of the display during the remaining tests.

Foot Cntrl. ADC Test (#0EH)
This test is performed with the custom Foot Controller Test Fixture (described at the end of this section) to verify ADC804 (U23). The test checks out only the Foot Pedal Controller (J11) and must be run with the test fixture or comparable circuitry. (Running this test without the fixture will cause an error message to be displayed just as though the test had failed. When the error message is displayed, press **Load/*** to continue.)

The Foot Controller Test Fixture contains an LFO to sweep the controller input from its minimum value (0VDC) to its maximum voltage (+5VDC) then back to its minimum. The ADC test analyzes the data generated by the ADC chip during the sweep and confirms that the chip accurately reports the voltage to the CPU. When the sweep (from minimum to maximum to minimum) has been completed successfully, the display will read: **PASSED**.

Error report:	
Test number	(0EH)
Expected data	N/A
Actual read data	N/A
Type of failure	(ADC Test Failed 03H, 18H)

Press **Load/*** to exit.

MIDI Test (#0CH)
This verifies the functionality of the MIDI input and output circuit. The test transmits data to the MIDI OUT jack and attempts to read the data at the MIDI IN jack. The first stage of the test is done by sending data through the Transmitter and then polling the receiver until data sent is received. This happens a number of times. The correctness of the data is also verified. The second stage of the test relies on the MIDI interrupt (internal to the V40) working satisfactorily.

NOTE: Each stage is repeated 255 times and the data transmitted error value is the actual counter value. Thus, it is possible to determine from the failure log how many bytes were transmitted successfully before failure occurred.

Error report:	
Test number	(0CH)
Transmitted Value	8 bit data sent out
Received Value	8 least significant bits data received 8 most significant bits indicate the status of the SCU status register
Address	N/A
Type of failure	Transmit, receive, interrupt, data, timeout

Slave Z80 SRAM Test (#14H)
This is a standard memory test that writes 55 (hex) into all memory locations, then reads them back to verify the correctness of the data. The procedure is repeated with AA, FF and 00. 00's are left in the SRAM when the test is complete. Any problems with the Static RAMs (U3 and U4 for Slave X, U46 and U47 for Slave Y) such as missing or shorted Address, Data or control lines should be detected by this test.

Error Log:	
Test Number	14
Tested Value	Expected data written
Failed Value	Actual value read
Address/location	Address of first bad location Bit 4 indicates whether it was Slave X SRAM or Slave Y SRAM that failed. Specifically: 000A0xxx indicates that Slave X SRAM failed; 000A8xxx indicates that Slave Y SRAM failed
Type of Failure	Various

Watchdog Timer Test (#0FH)
This test first kicks the Watchdog approximately every 50ms for a period of approximately 2 seconds. During this time the Watchdog should not reset the unit. (If it does, the test fails.) The second stage of the test allows the Watchdog Timer to time out and reset the unit. (If it does not reset the unit, the test fails.)

Due to the structure of the Power On Diagnostics, the Power Up CPU, ROM and SRAM Tests will be executed after reset, before the rest of the test is completed. In the unlikely event the CPU, ROM and/or SRAM Tests fail, the Watchdog test will be aborted and the unit will go through its normal cold boot cycle and report and log any such error.

Error report:	
Test number	(0F)
Type of failure	(19H, 1AH)

Word Clk Select Test (#10H)

The Word Clock Test confirms that the internal 48kHz and 44.1kHz word clocks are operational and within a reasonable preset frequency limit. It utilizes the V40 built-in timer. The accuracy of the test is therefore also dependent on the accuracy of the Host V40 oscillator. The test is set to detect failures that are not within ±0.5% tolerance (47760Hz - 48240Hz for the 48kHz clock to pass, 44321Hz - 44830Hz for the 44.1kHz clock to pass.) If either or both of the word clocks are not present, the system will lock up. This test starts the 56K and Z80 slave processors and leaves them running after the test is completed. In other words, the processors are not reset after the Word Clock Test is completed. The following error messages are available and will be displayed in the Error Log File if the Word Clock frequencies are out of spec:

44.1kHz WC Freq. too high 10 00000000 00000000 00000000 20	44.1kHz WC Freq. too low 10 00000000 00000000 00000000 21
48kHz WC Freq. too high 10 00000000 00000000 00000000 1E	48kHz WC Freq. too low 10 00000000 00000000 00000000 1F

Error report:

Test number	(0FH)
Expected data	N/A
Actual read data	N/A
Type of failure	(Word Clock Freq. too high or too low)

Slv to Host Int Test (#16H)

This test checks the Slave X (SHINTX) and Slave Y (SHINTY) interrupt signals by toggling each line once with a 50ms positive going pulse when the test is executed. To monitor the activity of (SHINTX) with an oscilloscope, probe connection B22 at connector J1 on the DSP board and connection B13 for monitoring (SHINTY). Set the oscilloscope for 20ms/div, 2V/div. Set the trigger for DC and + Slope. The interrupt lines will toggle as soon as **Load/*** is pressed.

The following error messages are available and will be displayed in the Error Log File if a failure occurred.

Slave X (SHINTX) Failed 16 00000000 00000000 00000001 03	Slave Y (SHINTY) Failed 16 00000000 00000000 80000001 03

Dig Aud IO Through

This diagnostic mode bypasses the main operating system to set up digital input and analog input mixing. The mixed stereo output is then fed to both the analog output and the digital output. The digital outputs left and right should put out the same as the analog outputs left and right. You can select internal 44.1 KHz wordclock, 48.0 KHz wordclock, or external wordclock.

Note that if this test is used for critical audio testing, the fact that analog and digital inputs are summed together must be taken into account. For instance, D-to-D and D-to-A performance will have analog noise added in. However, A-to-A and A-to-D performance will be accurate if no digital input is plugged in, as the digital input is zeroed in such a case. In general, it is better to follow previously outlined procedures that take performance measurements while running the main operating system of the unit. This test is just a quick diagnostic tool.

Infinite Test Loop

This test requires a MIDI cable connected between the PCM 91 MIDI OUT and MIDI IN jacks. This continuous test series was designed to discover intermittent failures.

Note: If a failure occurs while running the Infinite Test Loop, previous error log information may be overwritten

It is good practice to clear the Error Log File before executing the loop. (See Clear Error Log File below.) It will then be easier to identify which test failed and how many times the failure occurred.

The following tests are executed in the Infinite Test Loop:

MIDI Test (#0CH)
Slave Z80 SRAM Test (#14H)
Word Clock Select Tst (#10H)
Slave To Host Interrupt Test (#16H)

After the first loop, **PASSED** will be displayed. If a failure occurs, the bottom half of the display will read: **FAILURE**. If 10 errors occur during the Infinite Test Loop, the loop will halt to prevent the Error Log file from being overwritten. This file protection feature is active only for the Infinite Test Loop. In all other situations ,the oldest information in the Error Log is overwritten once 20 errors are recorded.

Show Error Log

This feature allows the Error Log File to be viewed while Extended Diagnostics are being executed. When selected, the display will indicate the last failed test that was recorded in the 20 record ring buffer.

Clear Error Log File
Clearing the Error Log File erases all error information in the 20 record ring buffer. When selected, the message: **WARNING! Erase Log?** will appear on the bottom half of the display. Pressing **Store** will clear the log and display: **Error Log Cleared**.

Another way to clear the Error Log is to clear the SRAM. This is done by powering on the PCM 91 while pressing **Down** and **Tap**. Release the buttons when the display reads:

WARNING! Press STORE
to clear the SRAM

Press **Store** to clear the SRAM, then press any button to continue the Power Up Diagnostics.

The Error Log File is not cleared by System Initialization.

Foot Controller Fixture

Lexicon uses a specially-designed test fixture for testing foot controllers. Following is a description of this fixture as well as a parts list and a reference drawing, in the event you want to build a similar fixture for your own use.

The Foot Controller Test Fixture provides an automatic 0 to +5V sweep for testing Lexicon products equipped with foot controller inputs. The fixture minimizes operator error when testing the controller inputs while still providing a thorough test.

The fixture provides a triangle waveform to the Controller Inputs with a low frequency sweep rate of approximately .5Hz. When monitored by the Foot Controller, A/D Converter Test (OEH), the display will sweep from 00 to FF in hex with a short pause at each extreme.

The fixture also contains a circuit for detecting the presence of +5V at the ring of the controller input beingtested. If the voltage at the ring is below 4V, the fixture output is muted and its LED will light.

Theory Of Operation
The fixture is powered by an external ELPAK WM063, or equivalent, power supply module which provides ±12V at 180mA each and +5V at 380mA. Power is fed into the fixture via a 5-pin DIN connector. The first half of U1 (a 4558 op amp) is configured as a low-frequency oscillator with R4 setting the rate. The output of U1 is routed through a 1kΩ resistor to SW1 which normally connects to the output of the fixture. When SW1 is pressed, the output of the fixture is connected to R14 (200K) which forms a resistive ladder with the internal pullup resistor.

When the fixture is connected to the PCM 91, +5V will be fed from the ring of the controller input being tested to the ring on connector J1 of the fixture. This voltage is sent to the base of transistor Q3 through resistor R10. R10 combined with R11 enables the voltage and/or impedance of the +5V line to turn the transistor on or off. If voltage drops below 4V, Q3 turns on. This biases both Q1 and Q2 on, lighting the LED and muting the fixture output. This verifies that +5V is present at the ring of the controller input and also checks the value of the resistor feeding the ring of the controller input.