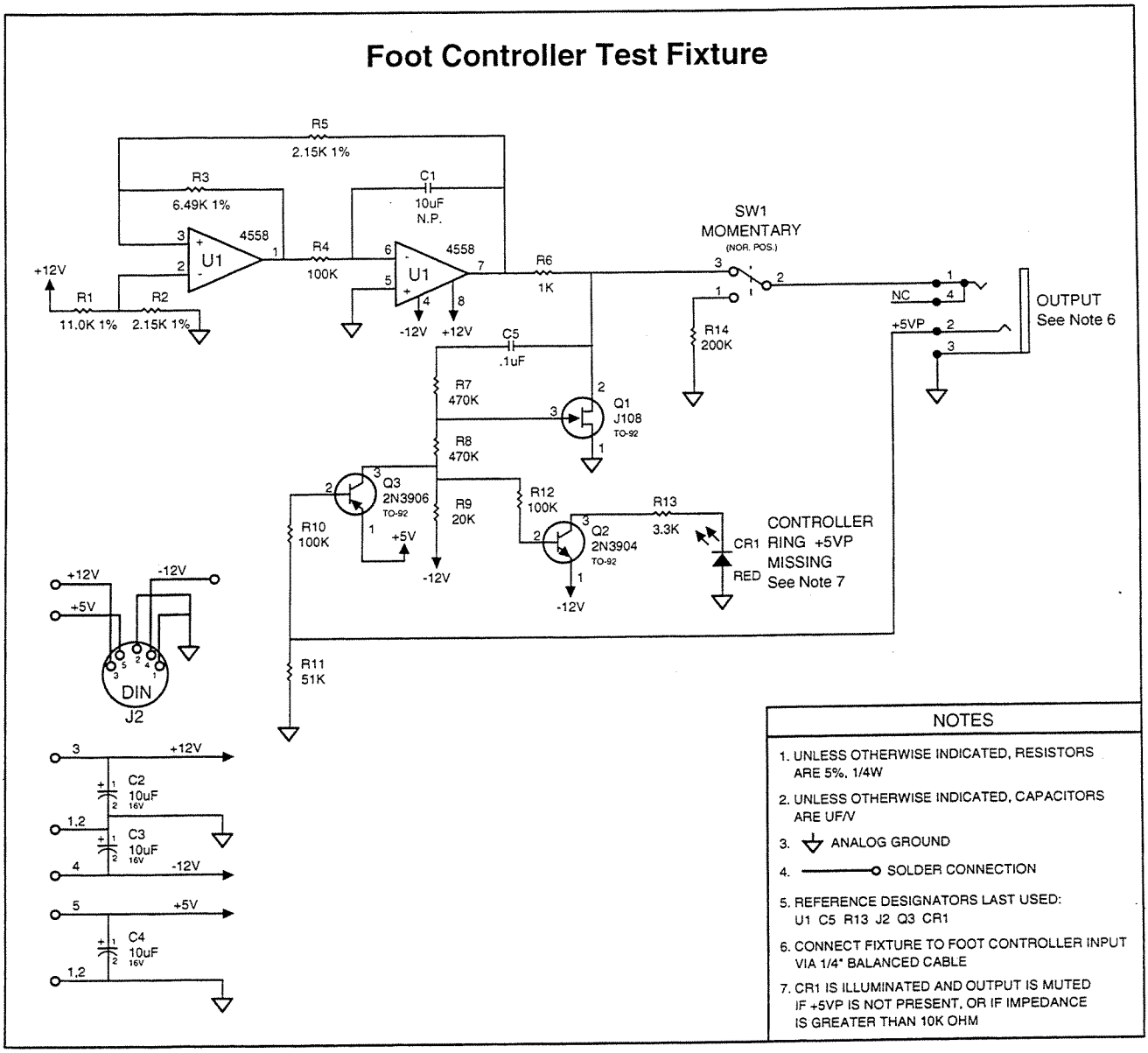
Foot Controller Test Fixture



NOTES

1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
3. ANALOG GROUND
4. SOLDER CONNECTION
5. REFERENCE DESIGNATORS LAST USED: U1 C5 R13 J2 Q3 CR1
6. CONNECT FIXTURE TO FOOT CONTROLLER INPUT VIA 1/4" BALANCED CABLE
7. CR1 IS ILLUMINATED AND OUTPUT IS MUTED IF +5VP IS NOT PRESENT, OR IF IMPEDANCE IS GREATER THAN 10K OHM

Foot Controller Fixture Parts List

PART NO.	DESCRIPTION	QTY	REFERENCE
340-00740	IC,LINEAR,4558	2	U1
520-00941	IC SCKT,8 PIN,PC,LO-PRO	2	U1
202-00529	RES,CF,5%,1/4W,1K OHM	1	R6
202-00538	RES,CF,5%,1/4W,3.3K OHM	1	R13
202-00555	RES,CF,5%,1/4W,20K OHM	1	R9
202-00564	RES,CF,5%,1/4W,51K OHM	2	R11
202-00570	RES,CF,5%,1/4W,100K OHM	2	R4,10,12
202-00576	RES,CF,5%,1/4W,200K OHM	2	R14
202-00579	RES,CF,5%,1/4W,470K OHM	3	R7,8
203-00460	RES,MF,1%,1/8W,2.15K OHM	1	R2,5
203-00465	RES,MF,1%,1/8W,6.49K OHM	3	R3
203-00474	RES,MF,1%,1/8W,11.0K OHM	1	R1
240-00609	CAP,ELEC,10uF,16V,RAD	4	C2,3,4

Troubleshooting

Problems with the PCM 91 can usually be classified as user interface problems or audio problems. User interface problems can range from one non-functioning front panel control to no display. Audio problems affect the signal quality from the analog or digital audio inputs and outputs. Some failures can be traced directly to one particular subsystem within the PCM 91, while others are caused by multiple sub-system failures.

When a problem is encountered, it is good practice to verify overall operation of the PCM 91 by running both the Power Up and the Extended Diagnostics. Refer to the Diagnostic functional instructions and troubleshooting hints given earlier in this chapter.

User Interface Problems

Display problems

Verify that all cable connections from the Host/Motherboard (J18-J22) to the various Front Panel boards are secure.

Vibration can eventually break the strands of cables making them intermittent or possibly open. Connections can become oxidized, corroded or otherwise contaminated causing them to be intermittent, open or resistive. For all of these reasons, caution should be used in troubleshooting. Before any cables are removed, they should be carefully inspected for proper seating and checked for continuity at all points between the Host/Motherboard and the Front Panel boards.

Verify that the +5VD supply is operational and within specification. Check the distribution of the supply to ensure that power is reaching the appropriate front panel display buffer and the register ICs.

If only one control on the Front Panel is failing, then the problem is probably a bad switch, encoder or potentiometer. If more than one control is failing, the problem may be with the Host Processor. Refer to the Diagnostic Descriptions and Theory of Operation.

Audio Problems

The first step when troubleshooting audio problems is to collect as much information as possible. The following lists some basic questions which should be answered before any repairs are attempted.

Is the problem:

1. on one output only?
2. at certain signal frequencies only?
3. at certain signal levels only?
4. in certain programs only?
5. at certain sample frequencies only?
6 with input only?
7. only without input?
8. temperature sensitive?
9. shock sensitive?

In general, it is best to verify overall audio performance and to further isolate the problem by running all of the audio proof-of-performance tests. This can be vital when troubleshooting subtle problems. Some system failures may cause a variety of tests to fail but troubleshooting based on one symptom type may be much easier than another. For example, a bad capacitor may produce a high level of distortion and a frequency response problem. The frequency response problem is easier to trace because the signal level can be monitored throughout the signal path on an ordinary oscilloscope.

One Bad Channel

One of the most useful pieces of information is determining whether a problem occurs on only one or on both channels. If the problem occurs at only one output, the following assumptions can generally be made with some level of confidence:

1. The power supplies are OK.
2. The system timing (clocks) is OK.
3. The digital circuitry (except for A/D and D/A conversion) is OK.

This type of problem can be fairly easy to troubleshoot, as the working channel can be used as a reference. With the same signal applied to both inputs, compare the signals on both channels at various points along the analog signal path. This may localize the problem fairly quickly.

The system diagnostics may be helpful in isolating RAM or DSP processor failures that might cause bad audio. Refer to the Diagnostics Descriptions for more information.

Both Channels Bad

As the likelihood of two separate components failing in the same way at the same time is remote, problems which occur in both channels can usually be traced to a component or components that are common to both channels, or to a system problem such as a power supply or timing problem. Verify that the power supplies are operational and within specification. If there is no output, refer to the next section.

No Output

First, determine whether the problem occurs on one or both channels.

When the machine has no output from only one channel, apply the same signal to both inputs, then compare the signals on both channels at various points along the analog signal path.

When the machine has no output from either channel, verify that the $\pm$15V and the $\pm$5V analog power supplies are operational and within specification. If the power supplies are OK, determine whether the problem lies within the A/D or the D/A conversion, then troubleshoot the corresponding circuitry.

Internal Adjustments and Troubleshooting

The following information allows testing of a non-functioning unit: no display, pegged input meters, load noises, popping crashes and /or no output. Test procedures are provided for checking power supplies, system clocks , battery voltage, and both analog and digital signal paths.

WARNING **CAUTION**

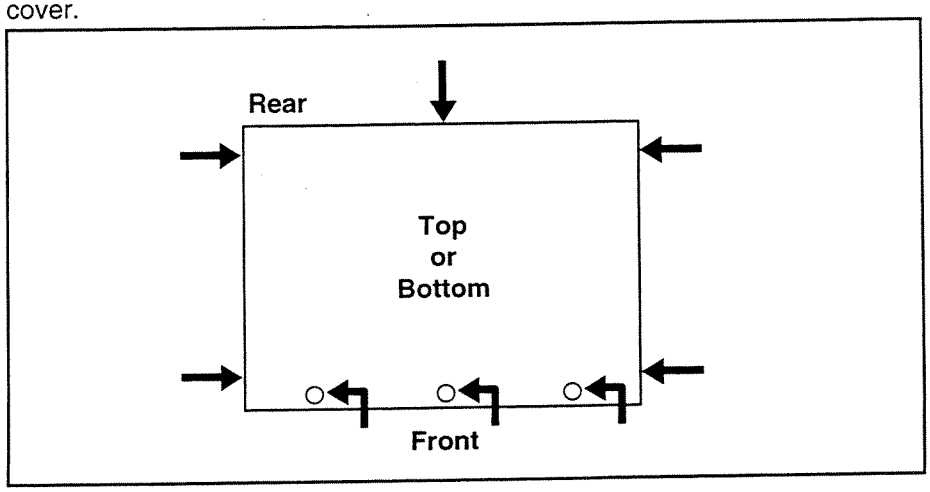
As these tests require removal of the PCM 91 cover, it is imperative that these tests be performed with regard to all safety and ESD precautions.

Required Equipment

- DMM (Digital Mulitimeter)
- Frequency Counter
- 100 MHz oscilloscope (with 1X ,10X probes)
- Bench power supply providing a variac voltage adjustment and transformer isolation

Removing the Top and Bottom Covers

Remove the eight (8) screws which attach the top cover. Repeat for the bottom cover.



WARNING

THE POWER SUPPLY IN THIS UNIT HAS A LIVE HEAT SINK. DO NOT TOUCH WHILE THE UNIT IS PLUGGED IN AND POWERED ON.

Power Supply

1. Plug in the PCM 91 and set the variac for nominal line voltage. A clicking noise from the relays should occur 30 seconds after you have powered up the PCM 91.

2. Set DMM to measure VCD, and check the regulated voltages for proper levels. Use the ground test point (GND-4), located on the board to the right of U9 as a ground reference, The test points for the supplies in the unit are shown below.

Supplies	Location	Range
+5VD	U37 Pin 20	(4.85-5.35)
+15V	Right of U9	(15.00-16.95)
-15V	Just above U9	14.25-15.75)
+5VA	Right of U9	(4.75-5.25)
-5VA	Right of U9	(4.75-5.25)

Internal Battery Voltage

1. Power off the PCM 91 and detach the power cord.
2. Set DMM for a DC voltage reading on the 20volts DC scale.
3. Place the positive (red) DMM Probe on top of the battery located just behind the front panel on the main board.
4. Place the negative (black) probe on the test point marked FOOTPEDAL ADC GND-10 to the right of U37 in the middle of the board.
5. The reading on the DMM should be ≥ 2.75volts. Replace the battery if the voltage is at 2.75 volts or lower.

System Clocks

These procedures test the major crystals and other clocks that are important to the operation of the unit. A frequency counter and an oscilloscope are required for these tests. The oscilloscope's ground lead should be connected to the PCM 91 chassis (away from the power supply).

1. Looking down on the unit with the top cover off, locate the DSP board which is screwed on to standoffs just to the right of the power supply area. Near the center of this board is Y1, a crystal that runs the Lexichip. Measure either side of this with the frequency counter. The reading should be 25.8MHz.

2. Turn PCM 91 power off and detach the power cord. Remove the screws that hold the DSP board in place. Remove the board and turn the power on. The message: Error E7 will be displayed.

3. Measure Y1, Y2, and Y3. Y3, the 16MHz clock that runs the microprocessor, is located to the left of the microprocessor (U34). Place the probe at U40 pin 1.

   Crystals Y1 (the 12.28MHz crystal) and Y2 (the 11.29MHz crystal) are located toward the rear of the unit. To measure Y1, which is used to generate the 48kHz Sample Rate Clock, place the probe at U21 pin 10.

   To measure Y2, which is used to generate the 44.1 kHz Sample Rate, place the probe at U22 pin 10.

Analog Audio Signal Tracing

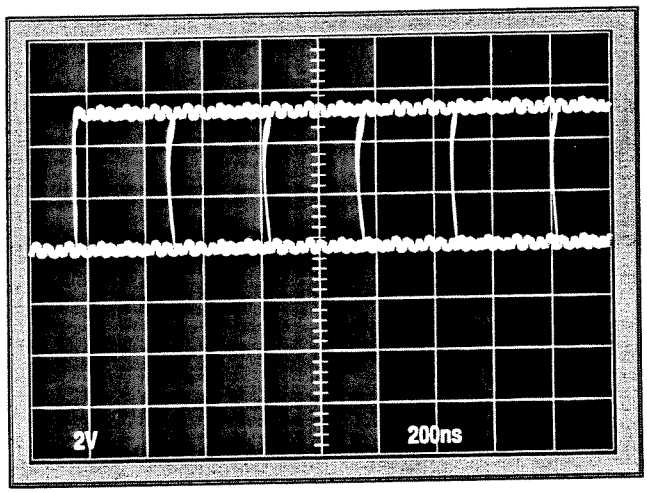
Required Equipment

- Level meter with oscillator
- Oscilloscope (to confirm audio signals for any visible problems)

Setup

1. Place the PCM 91 in Bypass, Analog InLvl=100%, OutLvl=+4dBu, Sample Rate=Internal 44.1 or 48kHz. (See Analog Audio Performance Check: Setup).
2. Apply a 1kHz signal @ -20dBu (77.5 mVrms)
3. Turn input pot fully clockwise.

Name	Measurement Point	Levels
Input Stage	U3 Pin 7 Left signal U3 Pin 1 Right signal	-20dBu – Input Switch OUT or 0dBu – Input Switch IN
Input Level Pot	R93 Left Signal R92 Right Signal	-20dBu OUT or 0dBu IN (77.5mVrms-0.775 Vrms)
Left ADC Buffer	LADC+, LADC-	-17dBu OUT or +3dBu IN (0.108 mVrms–1.085Vrms)
Right ADC Buffer	RADC+, RADC-	-17dBu OUT or +3dBu IN (0.108 mVrms–1.085Vrms)
ADC Inputs	U10 Pins 4+5 Left U10 Pins 24+25 Right	-17dBu OUT or +3dBu IN (0.108 mVrms–1.085Vrms)
ADC Outputs	U10 Pin15 or R76	This is a Digital audio signal +5volt CMOS Characteristics If there is no output at this pin check for clocks at 256FSA at pin 19, 64FSA at pin 14, WCA/ at pin 13) WCA/ = Sample Rate (44.1 or 48kHz) 64FSA = 64xSample Rate (2.82 or 3.07MHz) 256FSA = 256xSample Rate (11.29 or 12.28MHz)



D/A Converter Input	U8, Pin10	Digital audio signal

DAC Outputs Audio signal	R58+R60 R72+R74	Left out Right out	-16dBu OUT (0.123m Vrms)	or +4dBu IN (1.23 Vrms)
Lowpass Filter	LDAC RDAC	Left out Right out	-14dBu OUT (0.154mVrms)	+6dBu IN (1.54Vrms)
Output Gain Stage	LOUT ROUT	Left in Left out	With output level set at +4dBu: -4dBu OUT (0.489mVrms With output level set at -10dBu: -18dBu OUT (97.5mVrms)	+16dBu IN (4.89 Vrms) +4dBu IN (0.975Vrms)
	LOUT+, LOUT- ROUT+, ROUT-	Right in Right Out	With output level set at +4dBu: -4dBu OUT (0.489mVrms With output level set at -10dBu: -18dBu OUT (97.5mVrms)	+16dBu IN (4.89 Vrms) +4dBu IN (0.975Vrms)

Digital Audio Signal Tracing

This procedure verifies the Digital Audio Path of the PCM 91.

1. The input for the Digital signal is RCA J12 (white, marked S/PDIF) or XLR J10 (marked AES/EBU) on the back of the PCM 91.Typical input level is 0.5 Vpp for S/PDIF. The signal goes to the input of the Digital Audio Receiver (U15, Pin 9) after buffering (U19 pin 12/10) and selected by U16 pin 2/15. Depending on which is selected, S/PDIF or AES/EBU digital signals will appear at U16 pin 15. U15 outputs a serial audio data stream at 5Vpp (typical) via Pin 26.
2. The signal travels to pin A8 of J16, then goes to the DSP board for processing.
3. After the signal is processed, it comes back down onto the Host board via pin B16 of J16, and then passes through a gate (U45, Pins 1 and 3). The 5Vpp signal goes to the input of the Digital Audio transmitters (U17, U18, pin 8). Audio Transmitter U17 generates the AES/EBU formatted signals which are output through the isolation transformer (TX2) to meet the AES standard at the output jack (J11).
4. The Digital Audio Transmitter (U18) generates the S/PDIF formatted signal. This 5Vpp signal exits U18 at Pin 20 and goes through a resister divider network (R110, R111) to bring the signal level down to 1Vpp. When properly terminated by 75Ω, the signal level will drop further to 0.5Vpp.

System Signal Tracing

This procedure tests basic digital control signals in the PCM 91. For each of the following signals, load **P0 0.0 Prime Blue**, probe at the indicated place, and check for the expected results.

DSP Board Clocks

FCLK — DSP board: Probe on circuit-side at either side of R44
DSP56002 Clock: Should be a 40MHz square wave.

SLVCLK, SLVCLK/ — DSP board: Probe on circuit-side at either side of R47 and R46, respectively
Slave Clocks: Should be a 10 MHz square wave.

Misc Signals

HWAIT/ — DSP board connector: Probe on circuit-side of DSP board J2 pin B26) Host Wait Signal. Double low-going pulse spaced at about 10 µS apart. These two pulses should repeat every 20mS. More activity can be seen when adjusting the size parameter in the Edit menu (matrix position **2.0**).

MUTE/ — (U32 pin 15) Master Mute Line: Normally high, low on power-up.

Reset Signals

MRST/ — (U69 pin 1) Master Reset: Normally high, low on power-up.

SLVRST/ — DSP board connector: Probe on circuit-side of DSP board (J2 pin A22).
Slave Reset: Normally high, low on power-up.

LEXRST/ — DSP board connector: Probe on circuit-side of DSP board (J2 pin A20).
Lexichip Reset: Normally high, low on power-up.

56KRST/ — DSP board connector: Probe on circuit-side of DSP board (J2 pin B10).
DSP56002 Reset: Normally high, low on power-up.

Interrupt Signals (See Theory of Operation: Interrupt Timing)

HNMI — (U38 pin 3) V40's NMI line: Normally low. When DIOIMSK/ is high, it is pulsed high on digital I/O errors such as as loss-of-lock

PROGINT5 — (U49 pin 2) V40's INTP5 line: Periodic high-going pulse
Pulse width=10mS (approx.)
Period=20ms

PROGINT7 (U49 pin 6) V40's INTP7 line: Periodic high-going pulse
Pulse width=11ms (approx.)
Period=40 ms

WDKICK/ (U48 pin 5) Watch Dog Timer Kick Pulse:
Pulsewidth=150nS
Period=1mS

Encoder Signals

ASNB, ASNA (U73 pins 3 and 2 respectively)
Adjust Soft Knob Lines B and A: As ADJUST is rotated clockwise, the following patterns should rotate in relative order:
High, High
High, Low
Low, Low
Low, High

SSNB, SSNA (U73 pins 5 and 4 respectively)
Select Soft Knob Lines B and A: As ADJUST is rotated clockwise, the patterns described above should rotate in relative order.

LED/Switch Scanning Signals

LHRCOL/, RHRCOL/ (U65 pins 14 and 13 respectively)
Left and Right Headroom LED Column Strobes: Square Wave with a 4mS period.

SWC0/, SWC1/, SWC2/ (U68 pins 19, 18, 17 respectively)
Switch & LED Column Strobes: Low-going pulse, Pulse width=2 mS, Period=6mS

LDRW0/, LDRW1/, LDRW2/ U68 pins 16, 15, 14 respectively)
LED Row Strobes: Reload P0.0 Prime Blue.
Observe the following on U68 pin 16:
Low-going pulse, Pulse width=2mS, Period =6mS

Press "Edit" Button.
Observe the following on U68 pin 15:
Low-going pulse, Pulse-width=2mS, Period=6mS

Press "Register" Button.
Observe the following on U68 pin 14:
Low-going pulse
Pulse width=2mS, occasionally 4mS when tempo light blinks
Period=6mS

Restoring Factory Settings

The following procedure restores the PCM 91 factory default settings. This may be necessary due to memory problems, or following internal battery replacement.

This procedure will destroy any user settings or registers. Save setups and registers on a Memory Card to reload after this proceudre is completed.

1. Set the INPUT GAIN switch on the rear panel of the PCM 91 to the OUT position.
2. Set the front panel INPUT control fully counterclockwise.
3. Press **Down** until the display reads: **System Edit Mode/1.0/Go**
4. Turn SELECT until the display reads: **System/Initialize/1.9 (Press STORE)**
5. Press **Store** and verify that the display flashes the following message: **Are you sure? (Press STORE)**
6. Press **Store** and verify that the display flashes the following message for about 1/2 second: **Restoring Original Factory Settings...** then the message: **Loading Effect ...** then the display: **Chorus+Rvb/P0 0.0/Prime Blue**
7. Turn off the PCM 91 and detach the power cord.
8. Remove the 4 phone plug cables from the PCM 91.

The following procedure will restore the factory defaults without destroying the user registers, but may leave erroneous data in RAM.

1. Press **Control**, then use the ▲ and ▼ buttons to display: **Row 4 Setup.**
2. Turn SELECT until the display reads: **4.1 Load.**
3. Turn ADJUST counterclockwise to display: **Factory Settings.**
4. Press **Load.** The display should show: **Setup restored.**

5

Theory of Operation

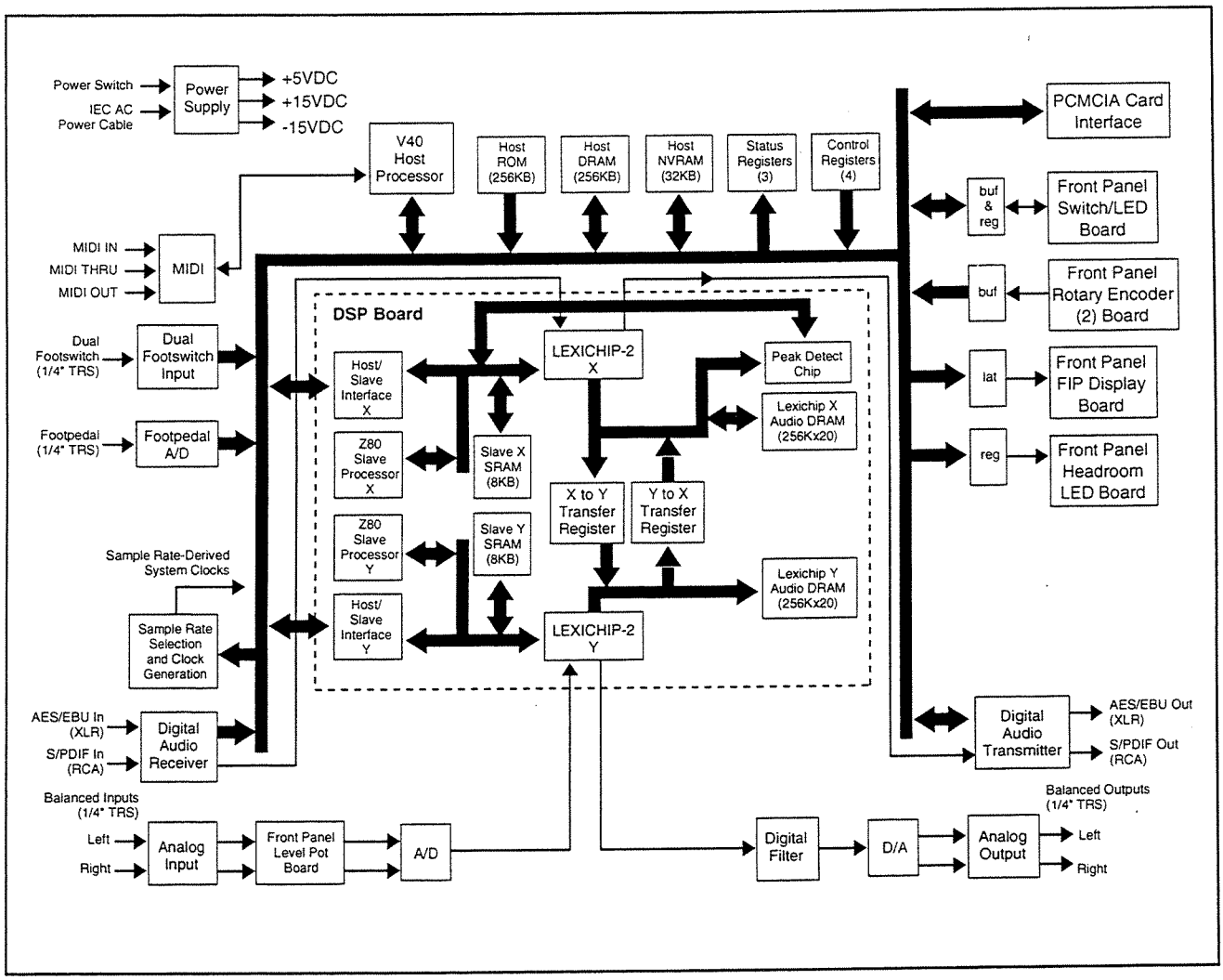
Architectural Overview

The PCM 91 digital hardware utilizes multiple microprocessors and digital signal processors to perform digital audio effects which are controlled via the front-panel interface, and the MIDI serial interface.

The PCM 91 features five major circuit sections: Host, DSP (Digital Signal Processing), Digital I/O, Analog Conversion, and Power Supply sections. A 10 MHz NEC uPD70208, also known as the V40, provides host microprocessor functions. The host processor circuit manages the user interface including the FIP display, softknobs, switchboard, status and headroom LEDs, MIDI, the footswitch and footpedal, and digital I/O circuitry. It is also responsible for program-load and parameter-passing to the DSP circuitry on the DSP board. The DSP board is responsible for the digital effects processing of the PCM 91. It has a multi-DSP engine featuring two of Lexicon's proprietary Lexichip-2 ASICs. A slave microprocessor, the Zilog Z-80, provides independent house-keeping functions for the Lexichip-2. The analog conversion circuitry handles A-to-D conversion and D-to-A conversion as well as a high performance analog interface to the balanced-line jacks on the rear-panel. The digital I/O circuitry implements AES/EBU and S/PDIF digital audio I/O.

The PCM 91 is physically sectioned into two major circuit boards, five minor circuit boards and a power supply module. The two major circuit boards are the Host Board and the DSP Board. The host processor, digital I/O and analog conversion circuitry reside on the Host Board while the DSP circuitry resides on the DSP Board which connects to the Host Board directly via a 72-pin connector. Smaller boards which are connected to the Host Board include the Front-Panel Switch Board, Front-Panel Encoder Board, Front-Panel Headroom Indicator LED Board, Front-Panel Input Level Pot Board, and the Intelligent FIP Display Module. The Power Supply Module supplies +5VDC, +15VDC, and -15VDC.

Block Diagram



Host Processor Circuitry

The Host Circuit is responsible for management of front-panel controls and displays, MIDI interface, Tap/Tempo/LFO functions, and download and real-time control of DSP code. There are 256K bytes of ROM, 256K bytes of DRAM, and 32K bytes of battery backed-up SRAM. The 32K bytes of SRAM are for non-volatile system parameter and user register storage.

The main processor of the host circuit is the NEC V40 (uPD70208) (U34). The V40 CPU has several on-chip peripherals including an 8-level priority interrupt controller, DMA controller, timers, and a serial port. The 8-level interrupt controller allows for management of several time-critical periodic tasks in order to meet the real-time requirements of the PCM 91. The DMA controller allows DSP-code download to happen in the background without significant impact on system performance. The timers provide MIDI UART clock generation, and timing references for tempo and LFO functions. The serial port is used to implement the MIDI interface.

In summary, the main host responsibilities are:

- Management of the user-interface:
  Intelligent front panel display FIP
  Front-panel switches
  Switch status LEDs
  Headroom LEDs
  Foot controller pedal jack via 8-bit A/D
  Footswitch jack
- Processing data and instructions to and from the MIDI UART (internal)
- Maintenance of non-volatile SRAM for storage of user registers
- Transparent refresh of Host DRAM.
- Providing download/upload to/from PCMCIA card interface
- Loading of slave Z80/Lexichip program code and data
- Controlling slave Z80/Lexichip reset and interrupt functions.
- Selecting sampling rate to be 44.1 kHz, 48 kHz or PLL frequency
- Management of channel status and reset functions for digital I/O interface
- Controlling audio muting hardware
- Management of user-defined control patching and LFO functions
- Management of Tap key and Tempo functions

Clocks

A 16 MHz crystal (Y3) is used to generate an 8 MHz clock used as the internal processor clock. This clock is also sourced from the V40 (HCLK) to clock external control logic: a hex flip-flop (74HC174) at U46 and a GAL20V8 at U40. HCLK is also inverted by a 74AC00 (U42) to source HCLK/. HCLK/ clocks a hex flip-flop (74AC174) at U47 and a GAL16V8 on the DSP board.

Bus Interface

The V40's 8-bit data bus is bidirectionally buffered by a 74HC245 (U35). Since twelve of the twenty V40 address lines are multiplexed with data and processor status, two 74HC573s (U36, U41) are used to latch and buffer sixteen of them (HA<19:0> less HA<11:8>). HA<11:8> are sourced directly from the V40.

Host Bus Status lines (HBS<2:0>), Host Memory Read Line (HMRD/), Host Memory Write Line (HMWRB/), and the Host Refresh Request Lines (HREFREQ/) are sourced to the GAL20V8 for memory interface logic.

Interrupts

The host processor has nine interrupts: one non-maskable interrupt (NMI) and eight maskable priority interrupts (INTPx). The priority ordering of the eight priority interrupts is preset as follows: INTP0 (highest) to INTP7 (lowest).

	Non-Maskable Interrupt
NMI	Digital Audio Receiver Error Condition
	Maskable Interrupts
INTP0	Timer 0 (LFO Interrupt) (Periodic: 1 msec) (Internal) (Highest Priority)
INTP1	MIDI Port Transmit/Receive (Internal)
INTP2	Timer 2 (Front Panel Display Interrupt)
INTP3	Unused
INTP4	DSP Interrupt (Z80)
INTP5	Programmable Interrupt P5 (Patch Calculations Process)
INTP6	Programmable Interrupt P6 (MIDI Data Process)
INTP7	Programmable Interrupt P7 (Front Panel Interface Process) (Lowest Priority)

INTP0 and INTP1 are sourced internal to the V40. INTP2 is sourced from the V40's Timer 2. INTP4 is sourced externally by an interrupt sourced either by the Z80 on the DSP board. The interrupt can be identified by reading bits 1 and 0 in Status Register 1. INTP5, INTP6 and INTP7 are sourced by software-programmable bits in Control Register 1 (U49 pins 2, 5 and 6). The interrupts are rising-edge triggered.

When probing with an oscilloscope, the following should be observed on each of the V40's interrupt pins, while running the program **P0 0.0 Deep Blue**:

NMI	(U34 pin 66)	Normally low. (When DIOIMSK/ is high, it is pulsed high on digital I/O error such as loss-of-lock)
INTP0		Not accessible (Internal to V40)
INTP1	(U34 pin 37)	Not accessible (Internal to V40) (Externally grounded)
INTP2	(U34 pin 38)	Periodic low-going pulse (Pulse-width=250ns, Period=2ms)
INTP3	(U34 pin 39)	Periodic low-going pulse (Pulse-width=125ns, Period=3.6ms (approx.)
INTP4	(U34 pin 40)	Non-periodic
INTP5	(U34 pin 41)	Periodic high-going pulse (Pulse-width=10ms (approx.), Period 20ms)
INTP6	(U34 pin 42)	Reserved for future enhancement
INTP7	(U34 pin 43)	Periodic high-going pulse (Pulse-width=11ms (approx.), Period 40ms)

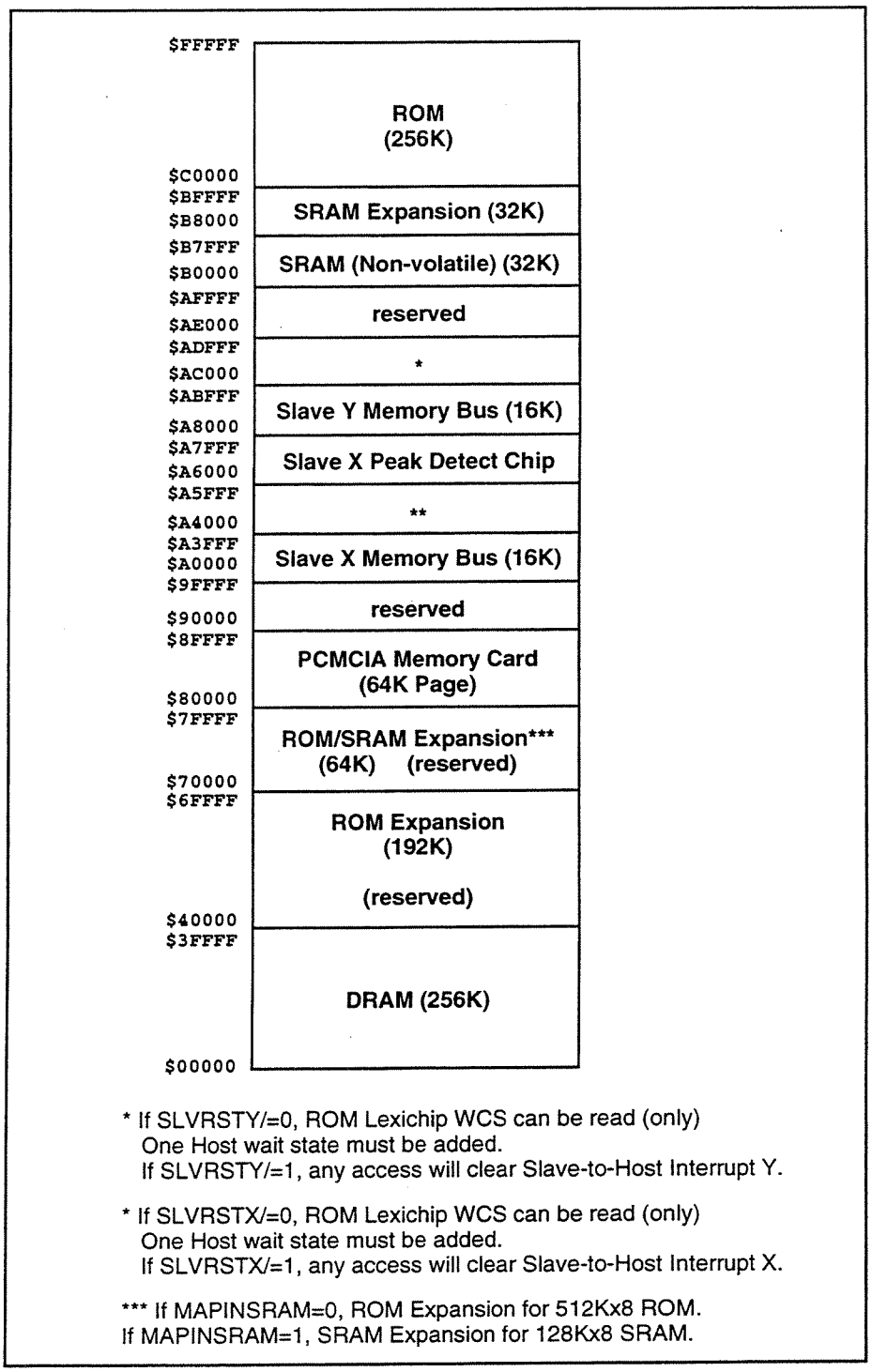
On-Chip Peripherals

V40 on-chip peripherals include:

- Clock generator
- Bus interface
- Bus arbitration
- Programmable wait-state generator
- DRAM refresh controller
- 3 16-bit timer/counters:1 for MIDI UART clock, 1 for 2ms display interrupt tick, 1 for 1ms interrupt tick
- Asynchronous serial I/O controller (for MIDI)
- 8-input interrupt controller
- 4-channel DMA controller

Host Memory

A GAL20V8 (U40) provides memory decoding for ROM, SRAM, DSP56002 Host port, Slave Z80 RAM Access, and DRAM. Following is the Host V40 memory map:



Memory Address Map

ROM

A 27C020/27C2001 (U55) which is a 2-megabit EPROM in a 256Kx8 configuration is installed.

The ROM enable signal (HROMEN/) is sourced by the GAL20V8 (U40) to enable the ROM when the memory address range is $C0000 to $FFFFF. (If a 512Kx8 ROM is used, the lower 256KB is mapped to $40000 to $7FFFF, and the higher 256KB is mapped to $C0000 to $FFFFF. Note that the upper 64K of the lower 256KB is displaced by SRAM if a 128KB SRAM is used and the control bit MAPINSRAM is asserted.)

Dynamic RAM (DRAM)

256Kx8 Dynamic RAM is provided. Two 44256 (256Kx4) parts at locations U50 and U51 in 20-pin ZIP packages are used to implement high and low nibble. U51 implements the low nibble. Refresh is taken care of by the V40 automatic refresh cycle which needs to be set up by software. Host address bits 17-0 are multiplexed to provide 9 row and 9 column address bits.

DRAM control is implemented by a GAL20V8 (U40) and a 74AC174 (U47). The GAL generates two signals DMEMOP/ and SELCA. DMEMOP/ is asserted for both read and write accesses to the DRAM. This signal is clock-delayed by U47 to generate HRAS/, the row address strobe. PTHRAS/ (pre-terminated version of HRAS/) is clock-delayed once again to generate HCAS/, the column address strobe. SELCA goes to 74AC157 multiplexers (U56, U57, U58) to source row and column address lines. When SELCA is asserted high, address lines HA<19:10> are selected to source the column address to HDRA<9:0>. When SELCA is not asserted (low), address lines HA<9:0> are selected to source the row address to HDRA<9:0>. During DRAM access, HMRD/ distinguishes between reads and writes. When HMRD/ is asserted low, it is a read operation. Otherwise it is a write operation.

The timing of the Host DRAM interface is shown in detail in later in this chapter.

Non-Volatile Battery Backed-Up Static RAM

A battery backed-up 32Kx8 Static RAM (U54) is provided to implement non-volatile storage. It is primarily used for system control parameter and user register storage. The 32-pin SRAM socket is factory shipped with a 28-pin 32Kx8 SRAM, installed with pin 1 of the IC aligned to pin 3 of the 32-pin socket.

The following table outlines the memory mapping for various configurations. The signal NVRAMEN is asserted by the GAL20V8 depending of the address lines and the control signal MAPINSRAM. MAPINSRAM, when asserted, allows the full use of 128Kx8 SRAMs. However, the lower 64KB of SRAM displaces the upper 64K portion of the reserved ROM expansion space. As current software only supports the 32Kx8 SRAM, MAPINSRAM should never be asserted.

RAM Type	MAPINSRAM	Memory Size	Address Range
32K x 8	0	32KB	$B0000-$B7FFF
128K x 8	0	64KB	$B0000-$BFFFF (upper 64KB only)
128K x 8	1	128KB	$70000-$7FFFF (lower 64KB)
			$B0000-$BFFFF (upper 64KB)

NVRAMEN is inverted by a 74AC00 (U61) NAND gate to yield QNVRAMEN/ which is an asserted-low signal going to the chip enable of the SRAM. QNVRAMEN/ is also qualified by PWR_OK which is source from the +5V Monitor (MC34164-U53). When power is going down, PWR_OK gets asserted and QNVRAMEN/ is gated off. The 74AC00 is powered by VRAM which is the battery backup voltage. This ensures that as power goes down, that the CE1/ pin of the RAM tracks Vcc as required by the SRAM manufacturer for reliable data retention. When the unit is on, VRAM should be at 5V. When the unit is on, VRAM follows the voltage from the backup lithium battery (3V) (BAT1).

Battery Backup

The Battery Backup circuitryis designed to protect data in the non-volatile SRAM. It is triggered (controlled) by the +5V Monitor, U53. To ensure the lowest possible leakage current during power on, two transistors (Q8 and Q9) are used to switch between backup operating modes.

A buffer (HC08), guaranteed to operate down to 2V is used to drive Q8. R205 ensures that the transistor stays off while the HC08 Vcc is less than 2V.

D19 is a Schottky diode to minimize the forward voltage drop while power is off. R209 protects the battery in case the diode should fail.

The battery low indicator is set to trigger at approximately 2.1-2.5V. If the battery is low, the status line BATLOW is asserted.

PCMCIA Memory Card

A PCMCIA memory card slot (J23) provides removable user register storage, and capability for algorithm and host software updates. Up to 1 MB of memory on a PCMCIA card is accessable. The host has a 64K window into the card memory space. The PCMCIA card enable signal CARDEN/ is asserted by the HOST GAL20V8 (U40) whenever the address accessed is the range $80000-$8FFFF. The PCMCIA interface in the PCM 91 is designed to handle all cards with an access time of 250ns or faster. The selected 64KB page within the 1MB of card space is set by 4 bits in Control Register 3. This allows up to 16 pages (16x64KB=1MB). The location within the page is selected by the 16 LSBs when the card is selected. The 4-bit page register CA<19:0>, set by Control Register 3 <3:0>, extends the card addressing capability to 1MByte. When the CREG/ control bit (Control Register 3 bit 7) is asserted low, the card's configuration register is selected instead of normal memory access.

Three 71HC541 octal buffers provide address line buffering (U59, U60) and control line buffering (U71). All three are enabled by software when doing card operations, and are disabled otherwise. They are enabled by de-asserting (setting high) DISCARD/ (Control Register bit 6.)

When DISCARD is asserted high:

- Address lines are pulled-down to ground via R187-R202.
- CCE1/, COE/, and CWE/ are pulled-up to CVCC via R228, 227, 225.
- CARDENB/ is pulled to a high by R223, disabling the bidirectional data buffer (U70).

A bidirectional data buffer 74HCT245 (U70) is used to isolate the card data lines from the host data bus HD<7:0>. The signal HMRD/ determines the direction. When low, data is enabled from the card data bus CD<7:0> to HD<7:0>. When high, data is enabled from HD<7:0> to CD<7:0>.

Software detects whether or not there is a card installed by reading CARDDET/ (Status Register 0 bit 4). This signal is asserted low when both ends of the PCMCIA card are plugged in, ensuring that the card is not powered-up or accessed until fully plugged in. The end-pin signals: CDET1/ and CDET2/ are pulled high when their respective pins are not inserted. These pins are grounded and, when they are inserted into J23, the corresponding lines are pulled low. A 74AC32 (U72) provides this logic by ANDing CDET1/ and CDET2/ to assert CARDDET/ (low).

Software reads the PCMCIA card write protection switch by reading CWRPROT (Status register 0 bit 5). CWRPROT is a buffered version of CWP via U71. Both CWRPROT and CWP are pulled-up to CVCC. When no card is inserted, CVCC will dischage to ground. Therefore, CWRPROT is not valid unless the card is fully inserted and enabled by setting DISCARD/ high.

The three remaining sections of the 74AC32 (U72) are used to produce a gated version of HMWR/ called PREBCWE/ . This signal gives an earlier rising edge to give the PCMCIA card the proper data setup time. PREBCWE/ is buffered by U66 to source CWE/ (the write enable that goes directly to the card).

The timing of the PCMCIA Card interface is shown in detail later in this chapter. Note that one wait state (generated by the V40 preset by software) is inserted for all card access.

Two status lines (CARDBVD<2:1>) from an inserted SRAM PCMCIA card indicate the condition of its battery. These are read by the host from Status Register 0 bits 3:2 respectively. Both signals are kept asserted when the battery is in good condition. A replacement warning condition is signaled by CARDBVD1 asserted and CARDBVD2 not asserted. In that case, data integrity on the card is still assured. If CARDBVD1 is not asserted, with CARDBVD2 either asserted or not asserted, the battery is no longer servicable and data is lost.

The following summarizes PCMCIA card control bits via Control Register 3:

Control Register 3 (I/O location=$0006)

7	6	5	4	3	2	1	0
CREG/	**DISCARD/**	AESINSEL	MAPINSRAM	**CA19**	**CA18**	**CA17**	**CA16**

The following outlines the PCMCIA card status via Status Register 0

Status Register 0 (I/O location=$0000 Read-Only)

7	6	5	4	3	2	1	0
FOOTSWT	SINGOUT/	**CWRPROT**	**CARDDET/**	**CARDBVD2**	**CARDBVD1**	spare	FOOTSWR

Host-to-Slave Z80/Lexichip Interface

The host has direct access to the DSP board's Slave Z80 8K SRAM. The Z80, in turn, is responsible for loading and modifying Lexichip program code internal to the chip. The address range for host access to the Slave Z80 SRAM is $A0000-$A1FFF. This memory address range is decoded by the HOST GAL20V8 (U40) to assert SBUSEN/ (low). (This corresponds to the Z80's local address range of $0000-$1FFF.)

Host I/O

I/O Address Map

Two 74HC138s (U62 and U63) provide I/O decoding for writeable and readable registers. The 74AC00 (U42) provides decode for the 8-bit ADC used to read the foot controller jack. The 74HC174 (U46) provides various HCLK delayed signals for I/O interface control. Host I/O address mapping is summarized as follows:

READS:

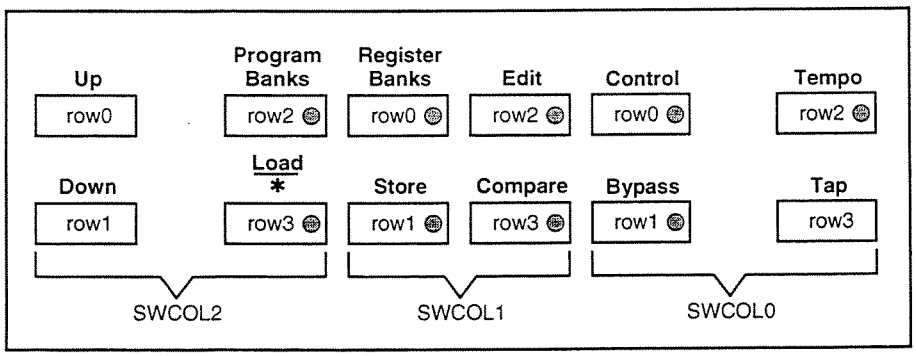
Host I/O Address HA<15:0>	Actual Address Used	I/O
xxxx xxxx xxx1 xxxx (B)	$0090 (H)	Footcontroller A/D Conversion Data
xxxx xxxx xxx0 111x (B)	$008E (H)	Watchdog Timer Kick
xxxx xxxx xxx0 110x (B)	$008C (H)	Switch Matrix Row and Soft Knobs
xxxx xxxx xxx0 101x (B)	$408A (H)	(unused)
xxxx xxxx xxx0 100x (B)	$0088 (H)	Clear Lexichip Overload Flag
xxxx xxxx xxx0 011x (B)	$0086 (H)	(unused)
xxxx xxxx xxx0 010x (B)	$0084 (H)	Status Register 2
xxxx xxxx xxx0 001x (B)	$0082 (H)	Status Register 1
xxxx xxxx xxx0 000x (B)	$0080 (H)	Status Register 0

WRITES:

Host I/O Address HA<15:0>	Actual Address Used	I/O
xxxx xxxx xxx1 xxxx (B)	$0090 (H)	Foot Controller A/D Conversion Start
xxxx xxxx xxx0 111x (B)	$008E (H)	Front Panel Display FIP
xxxx xxxx xxx0 110x (B)	$008C (H)	Switch/Status LED Matrix Cols/Rows
x1xx xxxx xxx0 101x (B)	$408A (H)	Set Host-to-Slave Interrupt Y
x0xx xxxx xxx0 101x (B)	$008A (H)	Set Host-to-Slave Interrupt X
xxx xxxx xxx0 100x (B)	$0088 (H)	Headroom LED rows
xxxx xxxx xxx0 011x (B)	$0086 (H)	Control Register 3
xxxx xxxx xxx0 010x (B)	$0084 (H)	Control Register 2
xxxx xxxx xxx0 001x (B)	$0082 (H)	Control Register 1
xxxx xxxx xxx0 000x (B)	$0080 (H)	Control Register 0

Front Panel Switches

The front-panel switches are arranged on the front-panel board as shown below.



Switches are arranged in a 4 row x 3 column matrix in which each column of 4 rows are read by:

1. Asserting one bit of the Switch Column (SWCOL<2:0>/) field of the SWITCH/ LEDs MATRIX REGISTER (74HC574,U68).
2. Then reading the Switch Row (SWROW<3:0>) field of the the Switch Matrix Input Buffer (74HC541, U73).

The control register and the Switch Column Matrix Buffer are outlined follows:

Switch/LED Matrix Register (I/O location=$000C Write-Only)

7	6	5	4	3	2	1	0
spare	spare	LDRW2	LDRW1	**LDRW0/**	**SWC2/**	**SWC1/**	**SWC0/**

Switch Matrix/Soft Knobs Input Buffer (I/O location = $000C Read-Only)

7	6	5	4	3	2	1	0
SWROW3	**SWROW2**	**SWROW1**	**SWROW0**	SSNB	SSNA	ASNB	ASNA

Soft Knobs

Two 36-position 2-bit gray-code encoded knobs with detents are used to implement the SELECT and ADJUST Soft Knobs. The 2-bits of each (available by reading the Switch Matrix/Soft Knobs Input Buffer) are assigned as follows:

Switch Matrix/Soft Knobs Input Buffer (I/O location = $000C Read-Only)

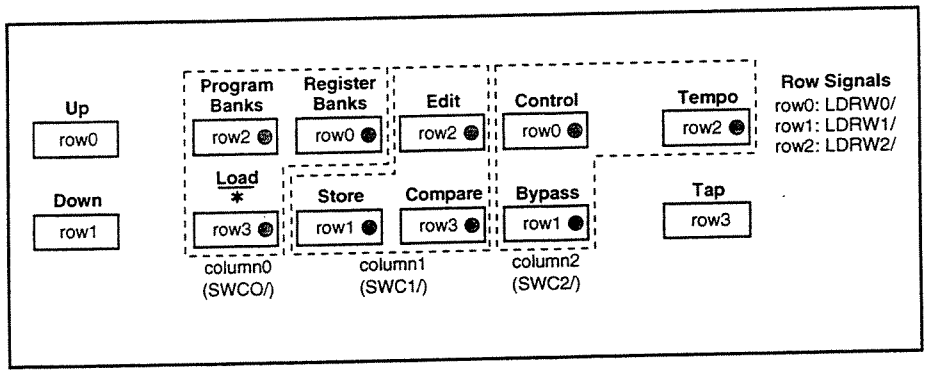
7	6	5	4	3	2	1	0
SWROW3	SWROW2	SWROW1	SWROW0	**SSNB**	**SSNA**	**ASNB**	**ASNA**

The encoded bits for the SELECTSoft Knob are SSNB and SSNA. The encoded bits for the ADJUST Soft Knob are ASNB and ASNA. As each knob is rotated clockwise, the sequence for each pair (SSNB:SSNA, and ASNB:ASNA) should be: LL, LH, HH, and HL, etc. in a rotating sequence. This can be observed at the inputs of the Soft Knobs Input Buffer (U73) pins 5 & 4, and 3 & 2 respectively.

Front Panel LEDs

Switch-Status LEDs

On the front-panel board, green LEDs are physically embedded in each of 9 switch button-caps. These LEDs are matrix-driven determined by 6 register bits consisting of 3 columns and 3 rows. The columns are the same as those that drive the switch columns (SWCOL<2:0>). The LED matrix columns and rows are determined by 6 bits of a 74HC574 Octal Register (U68). During operation, each column should individually be asserted for 2ms of a 6ms period. Transistors Q12, Q13, and Q14 source the needed current for each column. R248, R251 and R253 pull down each column when any respective transistor is off. Any LED within a column can be lit by asserting the corresponding rows (LEDROW<2:0>) (asserted-low). When LED(s) are on, peak current through R254, R255, and R256 should be about 20 mA. As the control bit LEDSEN tri-states all the LED control register bits, all LEDs are off during reset. LEDSEN must be asserted before any LEDs can come on. The front panel switches and LEDs are arranged as shown below.



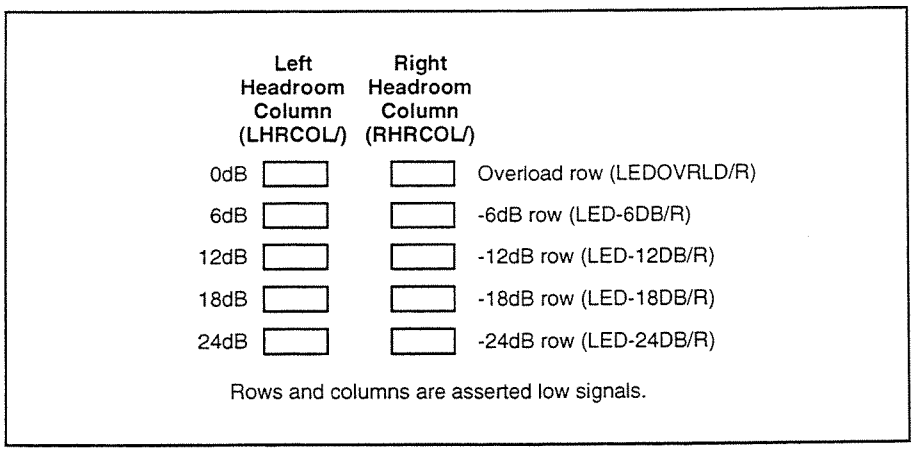
Status LED Column Grouping and Row Assignments

Switch/LEDs Matrix Register (I/O location = $000C Write-Only)

7	6	5	4	3	2	1	0
spare	spare	LDRW2/	LDRW1/	LDRW0/	SWC2/	SWC1/	SWC0/

Headroom Indicator LEDs

The Headroom LEDs are matrix-driven determined by 2 columns of 5 rows. The columns and rows are determined by 7 bits of a 74HC574 Octal Register (U65). During operation, each column should individually be asserted for 2ms of a 4ms period. The two columns are LHRCOL/ for the left input level, and RHRCOL/ for the right input level. Transistors Q10 and Q11 provide the necessary current to drive each column's LEDs. R235 and R237 pull down each column when its respective transistor is off. LEDs within a column can be lit by asserting the corresponding rows (LED-24DB/R, LED-18DB/R, LED-12DB/R, LED-6DB/R, LEDOVRL/R). When LED(s) are on, peak current through R238-242 should be about 10.4mA. As the control bit LEDSEN tri-states all the LED control register bits, all LEDs are off during reset. LEDSEN must be asserted before any LEDs can come on. The headroom indicator LEDs are arranged as shown below.



Headroom Indicator LEDs

Column and row control bits are in the headroom LED register. They are summarized as follows:

HeadroomLED Register (I/O location = $0008 Write-Only)

7	6	5	4	3	2	1	0
HIOUTLVL	**RHRCOL/**	**LHRCOL/**	**LEDOVRLD/**	**LED-6DDB/**	**LED-12DB**	**LED-18DB**	**LED-24DB**

Front Panel Display

The front panel alphanumeric display is a Futaba M202SD01HA, an intelligent vacuum fluorescent display module with 2 rows of 20 characters each. The module has its own display controller and is connected to the host system bus via an 8-bit data latch (U66). The display data write signal, DISPDWR/, is sourced from the I/O write decoder (74HC138 (U62). It is inverted by a 74HC04 (U44) to be the latch signal DISPDWR for the 74HC573 (U66) which is the display data latch. When the signal is asserted,. data from the host (HD<7:0>) flows through to source the display connector, then the display. When the signal is de-asserted, the latch is closed, and data should be held. This provides proper hold time for the display. DISPDWR/ goes to the display directly. DISPBSY is a handshake signal that, when asserted high, indicates that the display is busy. When the signal is low, it indicates that the display is ready to accept the next character or command. DISPBSY is monitored by the host via Status Register 1 bit 7 (U33 pin 9).

Display Data Buffer Latch (I/O location = $000E Write-Only)

7	6	5	4	3	2	1	0
DISPD7	**DISPD6**	**DISPD5**	**DISPD4**	**DISPD3**	**DISPD2**	**DISPD1**	**DISPD0**

For more information, including the character set codes and cursor commands, see the Futaba Dot Matrix VFD Module M202SD01HA Instruction Manual.

Footpedal ADC

An Analog Devices ADC0804 (U37) performs 8-bit A-to-D conversion for the footpedal input. Note that this input (J8) can also be used as a footswitch input in addition to the dual footswitch input jack (J9).

Conversion is started by an I/O write to location $0090. Conversion data is ready after the ADCDONE/ is asserted low (Status Register 0 bit 7). Conversion data is read by an I/O read from location $0090. ADCEN/, the enable for both reads and writes, is sourced by a 74AC00 (U42) via a series-terminating resistor.

Footswitches

The stereo 1/4" jack at J9 provides input for two footswitches. The primary switch should be wired from the tip to the sleeve. (This is the circuit that is used on a mono-plug footswitch.) The secondary switch should be wired from the ring to the sleeve. Each one can be normally-open or normally-closed. The two inputs can also accept a 0-5V voltage level. FB15-16 and C111-112 provide RFI isolation of the footswitches to prevent any high frequency signals from entering or exiting the box. R100, R102, D15 and D16 provide current limiting and overvoltage protection. R99 and R101 pull the inputs high when the circuit is open. FOOTSWT and FOOTSWR and the respective signals that go to Status Register 0 bits 7 and 0 for host processor monitoring.

MIDI

The MIDI interface in the PCM 91 complies with the MIDI specification. MIDI is implemented using the on-chip serial port of the V40 with buffering between it and the rear-panel 5-pin DIN jacks (J13-J15).

MIDI IN is accepted from J15. A 6N138/139 (U24) provides opto-isolation to source the buffered MIDI signal MIDIIN. This buffered signal goes to the RxD input of the V40 (U34 pin 34).

The unbuffered MIDIOUT signal is sourced from the TxD output of the V40 (U34 pin 35). It is then buffered by a 74HC14 schmitt trigger inverter (U25) and a 2N3904 transistor (Q5) before going to the MIDI OUT jack (J13).

MIDI THRU is sourced by a 74HC14 (U25) and a 2N3904 transistor (Q6) which is a buffered version of the MIDI input (MIDIIN). The MIDI THRU output is provided at the rear panel via J14. W4 provides selection between normal MIDI THRU operation of J14, and a special test mode. For normal operation, W4 should have a jumper shunt on pins 1 and 2. For testing, the jumper may be put on 2 and 3 to have the MIDI THRU jack duplicate the function of the MIDI OUT jack.

Analog I/O (Host Control Interface)

The following describes analog I/O control signals from the host. For further information, see Analog Circuitry.

ADCAL/ is a host control signal going to the A-to-D converter (ADC) and the D-to-A converter (DAC). ADCAL/ must be asserted low during power-up to calibrate the ADC and DAC, then brought high for normal operation. ADCAL/ must be brought low whenever the samp[le rate changes to maintain proper operation of the converters.

Control Register 1 (I/O location = $0001 Write-Only)

7	6	5	4	3	2	1	0
FIMTMSK/	DIOMSK/	LEDSEN	**ADCAL/**	**Spare**	PRGINTP7	PRGINTP6	PRGINTP5

The MUTE/ signal when asserted (low) opens the analog output relays to prevent any audio glitches from reaching the analog outputs during power-up and power-down. Also, the MUTE/ signal, when asserted-low gates off analog input, analog output, and digital input serial streams. This gating is done by three sections of a 74HC08 AND gate (U45). When the MUTE/ signal is de-asserted (high), the analog output relay is closed, and the serial audio streams are enabled, allowing audio to pass through.

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTLVLD	**MUTE/**	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

When the control signal HIOUTLVL is asserted (high), the +4 dBu setting for analog output level is selected. When HIOUTLVL is not asserted (low), the -10 dBu setting for analog output level is selected.

Headroom LED Register 1 (I/O location = $0008 Write-Only)

7	6	5	4	3	2	1	0
HIOUTLVL	RHRCOL/	LHRCOL/	LEDOVRLD/	LED-6DB	LED-12DB	LED-18DB	LED-24DB

Digital I/O

The host is responsible for managing the channel status of the Crystal Semiconductor CS8412 digital audio receiver, and the Crystal Semiconductor CS8402 digital audio transmitters. Status Register 2 and Control Register 2 contain bits to monitor and set channel status bits received and transmitted respectively. More details on Digital I/O are given later in this chapter.

System WordClock Source Selection

The user can select from among three different wordclocks (sample-rates): 44.1kHz, 48kHz and External. An 11.2896 MHz crystal (Y2) is used to derive the 44.1kHz wordclock, and a 12.2880 MHz crystal (Y1) is used to derive the 48.0kHz wordclock. (Both crystal circuits use a 74HCU04 (U22,U21) as crystal drivers operating the crystal in its parallel resonance mode.) An on-chip PLL on the CS8412 (U15) digital audio receiver is used to derive External wordclock.

The following table outlines the options for the wordclock source under host control. Note that appropriate digital I/O bits need to be set accordingly.

CTRL2<7> SRSSEL1	CTRL2<6> SRSSEL0	Wordclock Source
0	0	Internal 44.1kHz
0	1	Internal 48kHz
1	0	External Sync from Digital Input
1	1	Disabled (DC tied low)

A 74HC253 (U23) multiplexer controls selection of sources. The multiplexer's output is 256FS. A 74AC74 dual flip-flop (U27), two 74HC161 counters (U28,U29), and a 74HC175 quad flip-flop (U26) divide down 256FS to other various wordclock-dependent clock signals. The following is a summary of these clock signals and their functions:

256FS
Other Variations: PT256FS, 256FSA
Frequency: 256 x selected wordclock frequency (50% duty cycle) @44.1 KHz = 11.2896MHz; @48.0kHz = 12.2880MHz
Function:
a. Goes to 74AC74 (U27) to divide clock down further.
b. Goes to the A/D and D/A converters (U8, U10) as their master input clock.
c. Goes to DSP board connector (J16) for future functions.

128FS
Other Variations: PT128FS
Frequency: 128 x selected wordclock frequency (50% duty cycle) @44.1kHz: 5.6448MHz; @48.0kHz: 6.1440MHz
Function:
a. Goes to 74AC74 (U27) to divide clock down further.
b. Goes to CS8402 digital audio transmitters (U17, U18) as their master clock.

64FS
Other Variations: PT64FS, 64FSB, 64FS/, 64FSA (inverted)
Frequency: 64 times the selected wordclock frequency (50% duty-cycle)
@44.1kHz: 2.8224MHz; @48.0kHz: 3.0720MHz
Function:
a. Goes to two 74HC161s (U28, U29) and a 74HC175 (U26) to divide the clock down further.
b. Goes to AK5391 ADC (U10), CS4390 DAC (U8), and the Lexichip-2 on the DSP board.
c. Goes to CS8412 digital audio receiver (U15) and CS8402 digital audio transmitters (U17, U18).

AIOFRAME	Frequency:	2 times the selected wordclock frequency (High going pulse once every 32 64FS bit clocks.)
	Function:	Goes to the Lexichips on the DSP board to mark the start of a sample frame. (2 frames/Wordclock period.)
WC/	Other variations:	WCA/, CHSEL (inverted)
	Frequency:	User-selected Wordclock frequency of 44.1kHz, 48kHz, or External.
	Function:	a. The falling edge of WC/ (or the rising edge of CHSEL) denotes the beginning of a sample period. b. Goes to Lexichip on the DSP board via connector J16 to interrupt or reset the processors to the first instruction of the sample-period's instruction sequence. c. WCA/ goes to the ADC and DAC to indicate, when low, that the serial audio data frame corresponds to the right channel. Otherwise it corresponds to the left channel.

System Reset Circuitry

PCM 91 reset circuitry consists of four functional blocks, three of which join together and generate the Master Reset (MRST/) signal. The Watchdog Timer, the +5V Monitor, the reset delay circuitry and the Reset Register. The reset circuitry has no provision for early detection of power failure. Therefore, if the +5V Monitor detects less than 4.3V, the hardware will immediately force reset.

After a successful power on and a delay of approximately 0.75 sec., the Host CPU reset, the Reset Register reset, and the UART reset are released. The outputs of the Reset Register, except the Host Master Reset (HMRST), are left in an active state. It is, therefore, the responsibility of the software to release reset for other devices after the reset cycle. The Host can assert Host Master Reset, causing the Watchdog Timer circuitry to create a reset pulse to prevent reset latchup.

Watchdog Timer

The main component of the Watchdog timer circuitry is a Monostable Multivibrator, U48 (74HC4538). The HC4538 has a very well defined trigger input. They are all edge sensitive and have hysteresis. This design takes advantage of that and the retrigger capability of the multivibrator. Kicks from the Host ensure that the Q output of the first device stays high, provided that the kicks occur in shorter intervals than the pulse width. If a kick does not happen within the required time period, the first device will time out and its output will change state from high to low, triggering the second device, which will generate a pulse which will cause C182 to discharge, resetting the system. After the reset pulse disappears, C182 will start charging, as during the power on cycle. The output or the +5V Monitor is also connected to the second MMV, through an AND gate, to ensure an instant reset pulse when power is interrupted. The HMRST signal is connected to the second device's positive edge input, thereby triggering a reset pulse when HMRST is asserted.

As the Watchdog timer circuitry is inactive after power on until it is kicked, the software has to deliver the first kick to activate the timer.

+5V Monitor: The +5V monitor U53 (Motorola MC34164) is a Micropower Undervoltage Sensing Circuit which triggers at +4.33V (+5V increasing) and +4.27V (+5V decreasing). It has an Open Collector output. This device is used to control the Battery Backup and Reset circuitry. The combination of R183 and R184 is selected to ensure minimum VIH when C182 is fully discharged and the +5V monitor's output transistor is turned off.

All control registers are initialized with their outputs in a low state. Control Register 0 contains all other sub-system resets including resets for the digitial I/O circuitry (DIORST/), SLVRSTX/, SLVRSTY/, and LEXICHIP-2 (LEXRST/) on the DSP board. HMRST is a control register bit which will, when set, reset the entire unit. When the unit is reset via HMRST, the control register itself will be cleared after a delay.

MUTE/ is another initialization related control bit. Like the other control bits, it powers up in the low state. This enables all muting circuitry, including holding the audio output relays in an open state. The MUTE/ signal, when asserted, isolates the outputs (both digital and analog) from any power-on/power-off glitches.

The following summarizes the bits involved reset and initialization in Control Register 0:

Control Register 0 (I/O location = $0000 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTLVLD	MUTE/	DIORST/	FRCMOD	56KRST/	LEXRST/	SLVRST/

Status Bits Summary

Host Status Register 0 (I/O location = $0080 Read-Only)

7	6	5	4	3	2	1	0
FOOTSWT	Spare	CWRPROT	CARDDET/	CARDBVD2	CARDBVD1	spare	FOOSWR

FOOTSWT	Footswitch Jack Tip Input Level.
CWRPROT	PCMCIA Card Write Protect.
CARDDET/	PCMCIA Card Detect (Asserted-Low).
BVD2	PCMCIA Card Battery Voltage Detect Bit 2
BVD1	PCMCIA Card Battery Voltage Detect Bit 1
FOOTSWR	Footswitch Jack Ring Input Level

Host Status Register 1 (I/O location = $0082 Read-Only)

7	6	5	4	3	2	1	0
DISPBSY	LWAITY/	BATLOW	LEXCFLG/	SHINTY/	LWAITX/	reserved	SHINTX

DISPBSY	Front-Panel Display Busy Flag.
LWAIT/	Lexichip Y WC Wait line (Asserted Low)
BATLOW	Battery-Low Condition for Non-Volatile SRAM.
LEXCFLG/	Lexichip X CCLK Flag (Asserted-Low)
SHINTY/	Slave Z80 Y to Host Interrupt
LWAITX/	Lexichip X WC wait line (Asserted Low)
SHINTX	Slave (Z80) X to Host Interrupt.

Host Status Register 2 (I/O location = $0086 Read-Only)

7	6	5	4	3	2	1	0
ADCDONE/	ERF	F2/IGC	FI/ORG	F0/C3/	E2/C2/	E1/C1/	E0/C0/

ADCDONE/ Footpedal ADC done. (Asserted-low)

The following bits are explained in more detail in the Digital I/O Receiver section.

ERF Digital I/O Receiver Error Flag.
F2/IGC Digital I/O Receiver Frequency Reporting Bit 2/ Ignorant Category Bit.
F1/ORG Digital I/O Receiver Frequency Reporting Bit 1/ Original Bit
F0/C3/ Digital I/O Receiver Frequecy Reporting Bit 0 / CS3/
E2/C2/ Digital I/O Receiver Error Condition Bit 2 (asserted high)/ CS2/ (asserted low)
E1/C1/ Digital I/O Receiver Error Condition Bit 1 (asserted high)/ CS2/ (asserted low)
E0/C0/ Digital I/O Receiver Error Condition Bit 0 (asserted high) CS2/ (asserted low)

Control Bits Summary

Control Register 0 (I/O location = $0080 Write-Only)

7	6	5	4	3	2	1	0
HMRST	OUTVLD	MUTE/	DIORST/	SLVRSTY/	reserved	LEXRST/	SLVRSTX/

HMRST Host Master Reset.
OUTVLD Digital Output Valid Bit.
MUTE/ Mute Analog I/O (asserted low)
DIORST/ Digital I/O Circuitry Reset (Asserted Low)
SLVRSTY/ Slave Z80 Y Reset (Asserted Low)
LEXRST/ Lexichip-2 Reset (Asserted Low)
SLVRSTX/ Slave Z80 X Reset (Asserted Low)

Control Register 1 (I/O location = $0082 Write-Only)

7	6	5	4	3	2	1	0
SHYIMSK/	DIOIMSK/	LEDSEN	ADCAL/	Spare	PRGINTP7	PRGINTP6	PRTGINTP5

SHYIMSK/ Slave-to-Host Interrupt Y Mask (Asserted Low)
DIOIMSK/ Digitial Input Interrupt Mask
LEDSEN Front-Panel LEDs enable
ADCAL/ A-to-D Converter Calibrate (asserted low)
PRGINTP7 Programmable Interrupt Priority 7
PRGINTP6 Programmable Interrupt Priority 6
PRGINTP5 Programmable Interrupt Priority 5

Control Register 2 (I/O location = $0084 Write-Only)

7	6	5	4	3	2	1	0
SRSSEL1	SRSSEL0	DIOCSSEL	OUTCS15/	OUTCS3/	OUTCS2/	FC1	FC0

The following bits are explained in more detail later in this section.

SRSSEL1:0	Wordclock Source Selection Bits 1:0
DIOCSSEL	Digital I/O Receiver Channel Status Select.
OUTCS15/	Digital I/O Transmitter Channel Status Bit 15 Output (asserted low)
OUTCS3/	Digital I/O Transmitter Channel Status Bit 3 Output (asserted low)
OUTCS2/	Digital I/O Transmitter Channel Status Bit 2 Output (asserted low)
FC1:0	Digital I/O Transmitter Frequency Control Bits 1:0.

Control Register 3 (I/O location = $0086 Write-Only)

7	6	5	4	3	2	1	0
CREG/	DISCARD/	AES_INSEL	MAPINSRAM	CA19	CA18	CA17	CA16

CREG/	PCMCIA Register Select (Asserted-Low)
DISCARD/	Disable PCMCIA Card Drivers (Asserted-Low)
AES_INSEL	Select AES/EBU Digital Audio Input (otherwise S/PDIF Input is selected)
MPINSRAM	Map In RAM to reserved ROM space
CA<19:16>	PCMCIA Card Address <19:16> (Page Address)

DSP Board Circuitry

The PCM 91's DSP board is Lexicon's proprietary digital signal processing module. It does not contain any servicable parts. Contact an authorized repair facility, or Lexicon Customer Service for exchange or repair.

Digital I/O

Digital Audio I/O Circuitry

The PCM 91 supports both S/PDIF (IEC-958) consumer and AES/EBU professional digital audio formats. Two RCA jacks (J12) are provided on the rear panel for the S/PDIF interface. The white jack is the input, the red jack is the output. Male and female XLR connectors are used for the AES/EBU interface. Sample rates of 48, 44.1 and 44.056kHz are supported.

Digital Audio Receiver

The S/PDIF input is terminated with a 75Ω resistor per IEC 958 specifications and 33 pF caps for RFI suppression. The input signal passes through a 0.01uF DC blocking cap to a 74HCU04 (U19) configured as an amplifier to insure its levels exceed the threshold of the CS8412 receiver. BAV99 diodes provide overvoltage protection for the 74HCU04.

The AES/EBU input is terminated by a 1:1 transformer and an 110W resistor. The input signal goes to a 75ALS180 differential receiver (U14) which features a TTL-compatible output.

A 74HC4053 multiplexer (U16) selects the appropriate digital audio input. When AES_INSEL is high, the AES/EBU input is chosen; when low, S/PDIF is selected. The output of the mux is AC-coupled to the input of the CS8412 digital audio receiver (U15). Note that the meaning of the Channel Status bits decoded by the CS8412 change depending on whether the digital audio format is professional or consumer.

The CS8412 locks onto the frequency of the incoming S/PDIF signal with its internal PLL. R105 and C117 provide the time constant for the PLL Filter. C115, C116, and R104 provide power supply isolation and bypass capacitance for the CS8412's PLL circuitry and other analog circuitry. The output of the PLL, the MCK pin, sources the 256FS master clock. When external lock is selected by the 74HC253 Multiplexer (U23), this serves as a master clock for all digital audio clocking. This clock has 256 pulses per wordclock period.

The CS8412 has individual output pins for the more popular channel status bits. The function of Host Status Register 2 bits 5:0 is determined by DIOCSSEL (Control Register 2 bit 5). If DIOCSSEL is high, Status Register 2 bits 5:0 are channel status bits. When DIOCSSEL is high DIOCSSEL/ should be low clearing the output of the 74HC74 (U39) that sources the CS12 pin of the CS8412. This ensures that the channel status corresponds to sub-frame 1 (as opposed to sub-frame 2). If DIOCSSEL is low, those bits become Error Condition and Frequency Reporting bits. In either case, Status Register 2 bit 6 indicates an digital audio receiver error condition detected by the CS8412. This is outlined in the following table:

Host Status Bit	DIOCSSEL	Function		
STAT2<0>	0	E0	Error Condition bit 0	
STAT2<1>	0	E1	Error Condition bit 1	
STAT2<2>	0	E2	Error Condition bit 2	
STAT2<3>	0	F0	Frequency Reporting bit 0	
STAT2<4>	0	F1	Frequency Reporting bit 1	
STAT2<5>	0	F2	Frequency Reporting bit 2	
STAT2<6>	X	Error Flag		
STAT2<0>	1	C0/	Professional (low)	Consumer (high)
STAT2<1>	1	C1/	Non Audio	Non Audio
STAT2<2>	1	CB	EMO Emphasis	C2/ Copy Inhibit
STAT2<3>	1	CC	EM1 Emphasis	C3/ Emphasis
STAT2<4>	1	CD	C9/ Channel Mute	ORIG Original Copy
STAT2<5>	1	CE	CRCE/ CRC Error	IGCAT Ignorant Category

The Error Flag signal is gated by the Digital I/O Interrupt Mask (DIOIMSK/) with a 74HC08 AND gate (U45). The signal, after being buffered by a 74HC32 OR gate (U38), sources the V40's Non-Maskable Interrupt (HNMI). (The other input to U38 should always be low.) When DIOIMSK/ is high, ERF can trigger the V40's NMI. At that time, the type of error condition can be determined by reading the Error Decode bits. (When doing so, DIOCSSEL, Control Register 2 bit 5, must be set low.) When an error occurs, the corresponding error decode is latched. Since only one error can be indicated at any given time, there is a priority associated with each error code. Validity has the lowest priority while No-Lock has the highest priority. The error code is cleared by bringing the SEL pin of the CS8412 (U15) high for more than eight MCK cycles. From the V40's perspective, this is done by keeping DICSSEL high for 12 T-states or 3 instructions cycles. The following table describes the error conditions:

E2	E1	E0	Error	Comments
0	0	0	No Error	
0	0	1	Validity Bit High	Validity bit for a previous sample was high since the last clearing of the error codes
0	1	0	Confidence Flag	The received data eye opening is less than half a bit period, indicating a poor transmission link
0	1	1	Slipped Sample	A stereo sample has been dropped or re-read due to differences in internal vs. external sample rates
1	0	0	CRC Error (Pro only)	N/A
1	0	1	Parity Error	Incoming sub-frame does not have even parity as specified by digital audio interface standards
1	1	0	Biphase Coding Error	Biphase coding violation occurred
1	1	1	No Lock	PLL is not locked on incoming data stream. Lock is lost after not receiving 4 consecutive frame preambles

The frequency reporting bits are status bits from the CS8412 (U15) that indicate the sample rate of the incoming digital input. When digital input is selected, the system sample-rate should lock to the sample-rate of the incoming signal. In this case, one of three sample-rates is supported: 44.056kHz, 44.1kHz and 48kHz. (32kHz is accepted and will be locked to, but none of the DSP algorithms support it.) The frequency reporting bits' status is the result of a measurement by an internal circuit that uses a 6.144MHz clock as a reference. This reference is supplied by a 74HC74 (U39) that divides down the output of the 12.288 MHz crystal oscillator circuit. If all three frequency reporting bits are zero, it indicates that the incoming sample-rate is out-of-range. Note that the No-Lock condition, indicated by the Error Decoding bits, is a separate condition from being out-of-range. In either case, audio is muted. The CS8412 receiver outputs zeros upon loss of lock, and outputs the previous valid data for each channel upon detection of an error condition. To meet the Level 2 (Normal Accuracy Mode) specification, of the EIAJ CP-340 standard, only the 400 ppm tolerance is acceptable. Otherwise, the PCM 91 should be considered out-of-lock or going-out-of-lock. The decoding of the frequency reporting bits are summarized in the following table:

F2	F1	F0	Sample Frequency
0	0	0	Out of Range
0	0	1	48kHz +4%
0	1	0	44.1kHz +4%
0	1	1	32kHz +-4%
1	0	0	48kHz +-400ppm
1	0	1	44.1kHz +-400ppm
1	1	0	44.056kHz +-400ppm
1	1	1	32kHz +-400ppm

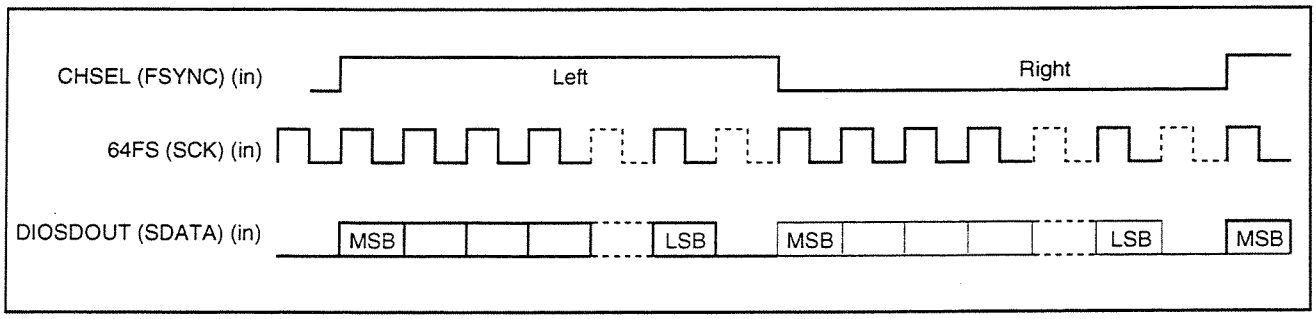
Digital Audio Transmitter

Two independent CS8402 digital audio transmitter ICs are used to implement the digital audio outputs. One CS8402 (U18) is wired for consumer format and dedicated to the S/PDIF output, while the other CS8402 (U17) is wired for professional format and dedicated to the AES/EBU output. The PCM81 cannot support the professional format on the S/PDIF output or the consumer format on the AES/EBU output.

For S/PDIF, the TXP output of U18 goes through a resistive voltage divider to provide a 1 volt peak-to-peak output waveform with a 75W output impedance per IEC 958 specifications. A 33pF capacitor is placed across the output to suppress RFI.

The TXP and TXN outputs of U17 are AC-coupled to a transformer per AES/EBU specifications. After the transformer, the output signal passes through a filter composed of 22W resistors and a 150pF capacitor. This filter suppresses RFI by limiting the rise and fall times of the signal while maintaining the required 110W output impedance.

Both CS8402s are hard-wired for the identical serial audio input format as shown:



CS8402 Audio Serial Port Format

Each CS8402 outputs the appropriate Channel Status for the professional (U17) and consumer (U18) digital audio formats. Most of the status bits are set in control register 2 as shown below:

Digital Audio Transmitter Control Bits

Host Control Bit	Function	
CTRL2<0>	FC0	Frequency Control bit 0
CTRL2<1>	FC1	Frequency Control bit 1
CTRL2<2>	CS2/	Copy Inhibit Out (asserted low)
CTRL2<3>	CS3/	Emphasis Out (asserted low)
CTRL2<4>	C15	Generation Status (asserted low)

The professional Emphasis Status bits (AES_EM0, AES_EM1) are set by gating CA[16:17] from control register 3 with LEDSEN. The CS8402 uses AES_EM0 and AES_EM1 to encode the professional channel status bits C2, C3, and C4. Their encoding and definition is shown in the following table.

Professional Emphasis Encoding

AES_EM1	AES_EM0	C2	C3	C4	Function
0	0	1	1	1	CCITT J.17
0	1	1	1	0	50/15 us
1	0	1	0	0	No emphasis
1	1	0	0	0	Not indicated

Frequency control bits FC0 and FC1 specify the sample rate channel status for both consumer and professional formats. Some glue logic (U38, U44) is required to interface FC0 and FC1 with the professional audio transmitter. The following table outlines the function of the frequency control bits.

Sample Frequency Encoding

FC1	FC0	C24 (cons)	C25 (cons)	Function	C6 (pro)	C7 (pro)
0	0	0	0	44.1 kHz	1	0
0	1	0	1	48 kHz	0	1
1	0	1	1	32 kHz*	1	1
1	1	0	0	44.1k-CD/48k* (consumer/pro)		

*Not supported

CS8402 is reset by the host control bit DIORST/. This signal is asserted low on power-up and, therefore, will not pass through audio until the host releases this signal after DSP code is loaded. In that case, the CS8402's internal transmit timing counters are not enabled until eight and one-half 64FS clocks after the first active edge of FSYNC after DIORST/ is released. On a power-fail condition (which happens on power-down and brown-out conditions), DIORST/ should be asserted. When DIORST/ is asserted, the differential line drivers of the CS8402 are set to ground. Though this cuts off the digital output mid-stream, it should not send speaker-damaging signals to the box receiving the PCM 91's digital output. It is up to the receiving box to handle a lost digital input gracefully. (In the PCM 91, the CS8412 receiver outputs zeros upon loss of lock, and outputs the previous valid data for each channel upon detection of an error condition.)

Analog Circuitry

Analog Inputs

Two combination XLR with 1/4" tip/ring/sleeve phone jacks (J1,2) are provided for balanced or unbalanced sources. Balanced sources should be connected so the hot (+) side goes to pin 2 of the XLR connector or the tip of the phone plug. Unbalanced signals may be applied to either pin 2 (tip) or pin 3 (ring). 150pF ceramic caps and ferrite beads are included for RFI suppression.

Input Amplifier

Three op amp stages (U1-3) are configured as an instrumentation amplifier for each analog input. A 2-pole double-throw switch (SW1), located on the rear panel, changes the input gain from 0dB to 20dB. 4.99kΩ, 0.1% resistors are used to insure a minimum common mode rejection ratio of 54dB. Nonpolar 10uF capacitors block any DC bias on the incoming signals from affecting the performance of the input stage while the 49.9 kΩ resistors provide 100kΩ input impedance. Overvoltage protection for the op amp is provided by the series 100Ω resistors and BAV99 diodes.

The outputs of the input amplifiers go through another set of DC blocking caps before going to the input level pot (R201) on a separate PC board. The caps serve to prevent any DC offset due to the op amps' bias currents from affecting the quietness of the level pot or introducing bias in the A/D conversion.

A/D Conversion

After the input level pot, the left and right signals return to the main board and pass through 220Ω resistors in series with the non-inverting inputs of a dual op amp (U13). These resistors protect the inputs of the op amp from high-level signals. This op amp has a gain of 10.8dB and drives the hot (+) side of the A/D converter and an inverting stage (U12) through a DC blocking capacitor. The dual op amp (U12) not only inverts the signals for the cold (-) side of the A/D converter, but also provides a 2.5 volt bias for the differential signal. The bias voltage is created by a voltage divider (R85,87) which is applied to the non-inverting inputs of the inverter. The bias voltage appears at the (+) side of the A/D as well. 200kΩ resistors to ground (R261,262) reduce the bias voltage slightly on the (+) side in order to maximize performance of the A/D converter. The signals pass through a one-pole low pass filter before the A/D input which limits aliasing during conversion. Both op amps operate off ±5 volt rails to insure signal levels do not exceed the maximum specified for the converter.

Conversion is performed by a stereo monolithic 24-bit Delta-Sigma AK5391 A/D converter (U10). This device uses a dual-bit sampler operating at 128x the sample rate and a noise shaping filter. This filter pushes the granularity noise beyond the audio spectrum. A digital decimation filter removes this high frequency noise and reduces the word rate to 24 bits. A differential architecture on the converter's front-end improves noise rejection. The AK5391 has independent power supply pins for the analog and digital sections. The digital side runs off +5VD which is filtered through a ferrite bead and 10uF tantalum cap in parallel with a 0.1uF ceramic cap. The analog section is powered by the separately regulated +5VA and includes 10uF tantalum and 0.1uF ceramic bypass capacitors.

The AK5391's serial data interface operates in slave mode and requires a master clock (256FSA), bit clock (64FSA), and left/right framing signal (WCA/). Serial data (AIOSDIN) is MSB first and left-justified within the frame. Sample rates of 44.1 and 48kHz are supported in the PCM81/91. An active low, calibration signal (ADCAL/) is asserted during power up and whenever the sample rate is changed. This initializes the converter's offset calibration cycle. Data from the converter is discarded for the first 200ms after ADCAL/ goes high due to the calibration process.

D/A Conversion

The CS4390 D/A converter (U8) is a Delta-Sigma (single-bit) type operating at 128x oversampling with 24-bit resolution. The CS4390 includes a switched-capacitor analog low pass filter located before the analog outputs. This type of filter reduces the effect of jitter on the incoming data from increasing THD at the analog outputs. The CS4390 requires +5 volts for both analog and digital supplies. +5VD is filtered through a ferrite bead and 10uF tantalum capacitor with a 0.1uF ceramic cap for the digital supply; this voltage passes through a 5.1Ω resistor with separate tantalum and ceramic bypass capacitors for the analog supply.

The CS4390's serial data interface operates in slave mode and requires a master clock (256FSA), bit clock (64FSA) and framing signal (WCA/). Serial data (DIOSDOUT) is MSB first and left-justified within the frame. The CS4390 will mute its analog outputs whenever MUTE/ is asserted.

The CS4390 provides differential outputs for the analog signals which go into active 3-pole low pass filters (U6,7). Each filter has a Butterworth response to insure flatness in the passband, with a gain of 1.9dB and -3dB point at 37kHz. The filter topology includes two op amp stages. The first stage converts the differential signal into a single-ended one while incorporating the first two poles of the filter. The third pole is developed in the second stage. The outputs from the first stage pass through 47uF capacitors in order to remove the 2.2 volt DC bias from the D/A converter's outputs.

Output Level Switching

Two J108 FETs (Q1,2) provide the ability to attenuate the output signals by 14dB by controlling the gain of an inverting op amp (U7). The FETs act like switches which change the input impedance to the inverter, thereby changing the gain. The gain is +10.3dB when the FETs are turned on, -3.7dB when the FETs are off.

The FETs are controlled by a 2N3906 transistor (Q3). When HIOUTLVL is high, Q16 turns off. A negative voltage is applied to the gates of the FETs, which turns them off. In this case the input resistance to the inverting stage is 11.8kΩ. With HIOUTLVL low, Q16 turns on. A small positive voltage is applied to each gate by the voltage divider, R61 and R62, thereby turning the FETs on. This action changes the input impedance by placing the 2.94kΩ and 11.8kΩ resistors in parallel, reducing the input resistance to approximately 2.36kΩ.

Balanced Output Amplifiers

Two dual op amps are employed as output amplifiers (U4,5). The circuit topology provides unity gain whether the outputs are driving balanced or single-ended loads. 4.99kΩ resistors with a 0.1% tolerance are used to insure the output levels are matched. 220 uF non-polar capacitors eliminate DC offsets from the outputs while BAV99 diodes and series 51Ω resistors provide overvoltage and short circuit protection.

Analog Outputs

Output connectors include two XLR (J3,7) and two 1/4" tip/ring/sleeve phone jacks (J5,6). Balanced outputs should be connected so the hot (+) side goes to pin 2 of the XLR connector or the tip of the phone plug. Unbalanced loads may be accommodated by grounding the unused pin [either pin 2 (tip) or pin 3 (ring)]. Ferrite beads and 100pF capacitors are included for RFI suppression.

Output muting is accomplished by miniature relays (RY1,2) controlled by MUTE/. When MUTE/ is low, Q4 turns off, breaking the current path to the relay coils, thereby shorting the analog outputs to ground. Likewise, when MUTE/ is high, Q1 turns on, activating the relays and connecting the stereo output signals to the output jacks.

Power Supply

A universal input switching power supply produces the voltages required by the PCM 91 circuits. It operates over an input voltage range of 90-264 VAC at 50 or 60Hz. The supply is capable of producing +5 VDC @ 3 Amps, +15 VDC @ 2 Amps and -15 VDC @ 0.35 Amps. The +5 Volt supply is used for all of the digital circuitry, while the ±15 Volt supplies are required for the analog circuitry.

The AC voltage is terminated by a 2-pin connector located towards the rear of the unit. A 6-pin connector at the opposite end of the supply accommodates the DC output voltages and returns. A cable assembly with a ferrite sleeve brings the supply voltages over to the main board. +5 Volt and digital ground connections to the main board are made near the power supply, while the ±15 Volt and analog ground terminate near the analog I/O jacks.

The power supply is not field serviceable. Contact an authorized repair facility, or Lexicon Customer Service for exchange or repair. A 3.15 Amp fast-acting fuse is incorporated on the supply module's AC input side. Always replace with a fuse of identical rating.

The ±15 Volt rails pass through a π filter to reduce high frequency noise before they are distributed to any analog circuitry. After this filter, the ±15VA rails go two voltage regulators. These regulators (U9,11) are used to produce ±5VA for the op amps that drive the A/D converter's analog inputs as well as the +5 volt analog supply required by the A/D converter.

The +5 Volt supply passes through low and high frequency bypass capacitors (C177-179) upon entering the main board. +5VD is distributed to the appropriate circuitry after passing through these capacitors.

Signal Names

16FS	Digital Audio Clock (16x Wordclock).
64FS, 64FSD	Digital Audio Clock (64x Wordclock)
64FSA	Analog Clock (64x Wordclock)
128FS	Digital Audio Clock (128x Wordclock)
256FS	Digital Audio Clock (256x Wordclock)
256FSA	Analog Clock (256x Wordclock)
56KINT	Interrupt from DSP56002
56KOVRL/	DSP56002 Interrupt from DSP to host
56KRST/	DSP56002 Reset Line
-15VA	-15 Volts Analog
-5VA	-5 Volts Analog
+5VA	+5 Volts Analog
+5VD	+5 Volts Digital
+15VA	+15 Volts Analog
ADCAL/	ADC Calibration Enable
ADCDONE/	Footpedal ADC Conversion Done Signal
ADCEN/	Foot Controller ADC Enable
AES_INSEL	Digital Audio Input Select (1=AES,0=S/PDIF)
AES_EM<1:0>	AES Digital Output Emphasis Status Bits
AIOFRAME	Analog I/O Framing Signal
AIOSDIN	Analog I/O Serial Data Input
ASNA	Adjust Soft Knob A
ASNB	Adjust Soft Knob B
BATLOW	Battery Low Signal
BVD<2:1>	PCMCIA Battery Voltage Status
CA<19:0>	PCMCIA Card Address
CARDET/	Card Detection
CARDEN/	PCMCIA Card Slot Enable
CARDENB/	Buffered Card Enable
CD<7:0>	PCMCIA Card Data
CDET1/	PCMCIA Card Detect 1
CDET2/	PCMCIA Card Detect 2
CCE1/	PCMCIA Card Enable 1
CCE2/	PCMCIA Card Enable 2
CLOVRL/	Clear Lexichip Overload Line
COE/	PCMCIA Card Output Enable
CSHINT/	Clear Slave-to-Host Interrupt
CTRL3..0WR/	Control Register 3 thru 0 Write Enable
CVCC	PCMCIA Card Vcc
CWE/	PCMCIA Card Write Enable
CWP	PCMCIA Card Write Protect
CWRPROT	PCMCIA Card Write Protect
DIOCSSEL/	Digital I/O Channel Status Select
DIOIMSK/	Digital I/O Interrupt Mask
DIOINT	Digital I/O Interrupt
DIORST/	Digital I/O Reset
DIOSDIN	Digital I/O Serial Data Input
DIOSDOUT	Digital I/O Serial Data Output
DISCARD	Disable PCMCIA Card
DISPBSY	Display Busy
DISPD<7:0>	Display Data Bus
DISPDWR	Display Data Write
DISPDWR/	Display Data Write Enable
DISPTST/	Display Test Mode
DMEMOP/	DRAM Memory Operation
DSPHEN/	DSP Host Enable
ERF	Digital Input Error Flag
E0/C0/	Error/Channel Status Bit 0
E1/C1/	Error/Channel Status Bit 1
E2/C2/	Error/Channel Status Bit 2

FC<1:0>	Digital Output Sample Frequency Status Bits
FINTMSK/	DSP56002 Interrupt Mask
FOOTSWR	Footswitch Jack Ring Input
FOOTSWT	Footswitch Jack Tip Input
FPASNA	Front-Panel Adjust Soft Knob A
FPASNB	Front-Panel Adjust Soft Knob B
FPLOCK/	DSP56002 PLL Lock Status
FPSSNA	Front-Panel Select Soft Knob A
FPSSNB	Front-Panel Select Soft Knob B
FRCMOD	DSP56002 Force Mode Line
F0/C3/	Digital Input Frequency Reporting Bit 0 / Channel Status Bit 3
F1/ORG	Digital Input Frequency Reporting Bit 1 / Original Bit
F2/IGC	Digital Input Frequency Reporting Bit 2 / Ignorant Catagory
GTAIOSDIN	Gated AIOSDIN
HA<19:0>	Host Address Bus
HACK/	Host DMA Acknowledge
HAD<7:0>	Host Multiplexed Address/Data Lines
HASTB	Host Address Strobe
HASTBQ	Clock-Delayed version of HASTB
HBEN/	Host Bus Enable
HBR/W	Host Bus Read-Not Write
HBS<2:0>	Host Bus Status
HBSQ0	Clock-Delayed Host Bus Status 0
HBSQQ0	Double Clock-Delayed Host Bus Status 0
HBW/RQ	Clock Delayed version of Host Bus Write-Not Read
HCAS/	Host DRAM Column Address Strobe
HCLK	Host Clock
HD<7:0>	Host Data Bus
HDRA<9:0>	Host DRAM Address Lines
HIORD/	Host IO Read Enable
HIOUTLVL	High Output Level Enable
HIOWR/	Host IO Write Enable
HMRD/	Host Memory Read
HMRDQ/	Clock-Delayed version of HCB-HMRD/
HMRD2Q	Double Clock-Delayed version of HCB-HMRD
HMRD3Q	Triple Clock-Delayed Host Memory Read
HMRST	Host Master Reset Control Bit
HMWR/	Host Memory Write
HMWRB/	Host Memory Write Buffered
HRAS/	Host DRAM Row Address Strobe
HREFREQ/	Host Refresh Request
HREQ	Host DMA Request Line
HREQQ	Host DMA Request
HRLEDWR/	Headroom LEDs Write Enable
HROMEN/	Host ROM Enable
HWAIT/	Host Wait Enable
LARWR/	LEDs Row and Column / Switch Column Register Write Enable.
LED-6DB/	Headroom LED -6dB Row Line
LED-12DB/	Headroom LED -12dB Row Line
LED-18DB/	Headroom LED -18dB Row Line
LED-24DB/	Headroom LED -24dB Row Line
LEDOVRLD/	Headroom LED Overload Row Line
LEXRST/	Lexichip Reset
LHRCOL	Left Headroom Column Strobe
LEDROW<2:0>/	LED Row Lines
LEDSEN	LED Buffers Enable
LIN	Left Analog Audio Input (post level control)
LOGICHI	LogicHigh

LOUT	Left Analog Audio Output (from DAC)
LOVLDP/	Lexichip Overload Pulse
LWAITY/	Lexichip Wait Line
MAPINSRAM	Map In SRAM.
MIDIIN	MIDI Input Serial Data
MIDIINTHRU	Buffered MIDI Input for MIDI THRU
MIDIOUT	MIDI Output Serial Data
MIDITHOUT	MIDI Output for THRU Jack Testing
MIDITHRU	MIDI THRU
MRST/	Master Reset
MUTE/	Analog Output Mute
NVRAMEN	Non-Volatile RAM Enable
OUT_USER	Digital Output User Bits
OUTCS<15,3,2>	Output Channel Status Bits 15, 3 and 2
OUTVLD	Digital Output Validity Bit
PGDIOSDOUT	Pre-Gated DIOSDOUT
PREBCWE/	Pre-Buffered Version of Card Write Enable
PRGINT<7:5>	Programmable Interrupts 7 thru 5
PWR_OK	Power OK
RHRCOL	Right Headroom Column Strobe
RIN	Right Analog Audio Input (post level control)
ROUT	Right Analog Audio Output (from DAC)
ROWRD/	LEDs Row Read Enable
SBUSEN/	Slave Bus Enable
SELCA	Select DRAM Column Address Enable
SHINT	Slave-to-Host Interrupt
SHSINT/	Set Slave-to-Host Interrupt
SLVRST/	Slave Reset
SRSSEL<1:0>	Wordclock Source Select Lines
SSNA	Select Soft Knob A
SSNB	Select Soft Knob B
STAT2..0RD/	Status Register Read Enable 2 thru 0
SWCOL<2:0>	Switch Column Strobe Bits
SWROW<3:0>	Switch Row 3 thru 0
TACOSWAP	Tacochip Swap Signal
VRAM	Non-Volatile SRAM Power
VREFADC	Footpedal ADC Voltage Reference
WC/	Word Clock
WCA/	Analog Wordclock
WDKICK/	Watchdog Timer Kick

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Parts List

POWER CORDS

PART NO.	DESCRIPTION	QTY	REFERENCE
680-09149	CORD,POWER,NA/IEC,SVT,VW-1,10A	1	N.AMER
680-08830	CORD,POWER,IEC,6A,2M,EURO	1	
680-10093	CORD,POWER,IEC,5A,2M,UK	1	
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1	
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1	
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1	
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1	
680-10098	CORD,POWER,IEC,6A,2M,UNIVERSAL	1	

SHIP MAT'LS

PART NO.	DESCRIPTION	QTY	REFERENCE
541-00781	BUMPER,FEET,3-M #SJ5018	4	
730-11361	BOX,21.5X5.38X20,BLANK	1	OUTER BOX
730-11364	INSERT,FOAM,ENDCAP,1UX9&12	2	
730-11444	INSERT,CORR,ACC,21X4.5	1	POWER CORD
730-11459	BOX,21X5X19,LEXICON	1	INNER BOX

MECH/CHASSIS

PART NO.	DESCRIPTION	QTY	REFERENCE
430-09785	DISPLAY,VF,20X2 CHAR,5X7DOT	1	
510-09985	CONN,MEM CARD,68 PIN,EJECTOR	1	HOST BD (J23)
530-02488	TIE,CABLE,NYL,.14"X5 5/8"	1	PS TO HOST CABLE
530-09382	CLIP,WIRE HRNS,.15DIA,ADH BAK	2	PS TO HOST CABLE
530-09979	CLAMP,CABLE,.169",ZN	1	AC INPUT CABLE
550-03827	BUTTON,.346RD,BLK	1	PWR SW
550-09087	KNOB,15MM,6MM/FLAT,BLK	1	LVL POT
550-09759	BUTTON,.20X.50,BLK	3	
550-09760	BUTTON,.20X.50,BLK,W/LENS	9	
550-09767	KNOB,21MM,6MM/FL,BLK/BLK	2	ENCODERS
550-12351	CAP,SW,7.5MMRDX22.5MML,BLK	1	LVL SW
630-02737	WSHR,FL,#8CLX.02TH,BLK,NYL	4	FP TO CHASSIS
630-03669	SPCR,#4CLX3/8,3/16RD,NYL	2	PWR SW SUPPORT
630-09709	SPCR,PCB/FOOT,.188,NYL	1	HOST BD
640-01706	SCRW,4-40X3/8,PNH,PH,ZN	4	FP SW BD TO INSERT(2); AC CONN TO CHASSIS(2)
640-02034	SCRW,4-40X5/8,PNH,PH,ZN	2	MEMCD TO HOST BD
640-02736	SCRW,8-32X3/8,BH,SCKT,BLK	4	FP TO CHASSIS
640-03957	SCRW,6-32X3/16,TH,PH,BLK	16	COVERS TO CHASSIS AND INSERT
640-04339	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	6	DSP TO HOST BD (4); HDRM BD TO INSERT (2)
640-07696	SCRW,M3X8MM,PH,PNH,ZN	2	DSPLY TO INSERT
640-09758	SCRW,M3X16MM,PH,FH,ZN	2	PWR SW TO CHASSIS

PART NO.	DESCRIPTION	QTY	REFERENCE
640-09987	SCRW,6-32X5/16,PNH,PH,SEMS,ZN	14	PS TO CHASSIS&BRKT (4); HOST BD TO CHASSIS, INSERT & PS BRKT (9); AC CLAMP TO CHASSIS(1)
640-11284	SCRW,M3X8MM,FH,PH,BZ	4	J1,2 (Use 641-11466 w/510-13799)
641-09699	SCRW,TAP,AB,#2X5/16,PNH,PH,ZN	3	MIDI CONN TO CHASSIS
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	13	J3,7,10,11 (12) (J1,2 w/510-13799) RCA CONN TO CHASSIS (1);
643-01728	NUT,6-32,KEP,ZN	2	CHASSIS GND (1); AC CABLE CLAMP (1)
643-01732	NUT,4-40,KEP,ZN	6	AC CONN TO CHASSIS(2); FP TO INSERT (2); MEMCD CONN TO HOST (2)
644-01735	WSHR,FL,#6CLX3/8ODX1/32THK	1	CHASSIS GND
644-07893	WSHR,FL,.427IDX.550X.035THK,ZN	2	FP ENCODER TO INSERT
650-05899	POPRVT,5/32X1/4,REG PROT HD,AL	3	PS BRKT TO CHASSIS
680-11709	CABLE,AC PWR,SHLD,14",P1=N	1	AC CONN TO PWR SUP AND PWR SWITCH
700-09856	CHASSIS,INSERT,FP,PCM-80	1	
700-09859	BRACKET,PWR SUP,PCM-80	1	
700-12646	CHASSIS,WRAP,PCM81/91	1	
700-12647	COVER,TOP/BOTTOM,PCM81/91	2	
701-09860	BRACKET,POT,SHIELD,PCM-80	1	INPUT LVL POT
702-09858	COVER,PROTECTIVE,TOP,PS,PCM-80	1	
702-09861	COVER,PROTECTIVE,BOT,PS,PCM-80	1	
702-12642	PANEL,FRONT,PCM91	1	
703-09862	LENS,DISPLAY,PCM-80	1	
703-12644	PANEL,OVLY,REAR,PCM81/91	1	
710-10190	PC BD,MEMCD CVR,PCM80&1/90&1	1	
740-08556	LABEL,GROUND SYMBOL,0.5"DIA	1	CHASSIS GND
740-08558	LABEL,TUV CERTIFIED,BAYERN	1	TOP COVER
740-11482	LABEL,WARN/APP,FCC/C-UL/CE,PRO	1	TOP COVER
740-12665	LABEL,PRODUCT ID,PCM91	1	TOP COVER
750-11396	PWR SUP,+5V@3A,+/-15V,40W	1	

HOST BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	10	R114,117,119,204,235,237,257-260
202-09871	RESSM,RO,5%,1/10W,1K OHM	23	R95,105,132,150,154,158-160,169, R171,185,203,205,209,230,234,236, R248-253
202-09873	RESSM,RO,5%,1/10W,10K OHM	52	R25,26,38,39,63,131,140-142,153,155 R167,186-202,207,208,210-223, R232,233,243-247
202-09894	RESSM,RO,5%,1/10W,1M OHM	3	R52,65,143
202-09899	RESSM,RO,5%,1/10W,47 OHM	21	R76,125,130,135,136,139,144-149,156, R157,161-166,172
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	8	R62,183,224-229
202-10558	RESSM,RO,5%,1/10W,47K OHM	3	R99,101,113
202-10559	RESSM,RO,5%,1/10W,100 OHM	10	R173-182
202-10569	RESSM,RO,5%,1/10W,10 OHM	5	R104,129,133,134,151
202-10570	RESSM,RO,5%,1/10W,120 OHM	2	R100,102
202-10571	RESSM,RO,5%,1/10W,100K OHM	1	R97
202-10572	RESSM,RO,5%,1/10W,200K OHM	2	R261,262

PART NO.	DESCRIPTION	QTY	REFERENCE
202-10573	RESSM,RO,5%,1/10W,470K OHM	2	R168,170
202-10574	RESSM,RO,5%,1/10W,10M OHM	2	R123,127
202-10585	RESSM,RO,5%,1/4W,51 OHM	8	R27,28,40,41,77,79,82,84
202-10586	RESSM,RO,5%,1/4W,100 OHM	4	R1,2,9,10
202-10835	RESSM,RO,5%,1/4W,470 OHM	2	R124,128
202-10889	RESSM,RO,5%,1/10W,75 OHM	2	R137,138
202-10891	RESSM,RO,5%,1/10W,270 OHM	5	R238-242
202-10943	RESSM,RO,5%,1/10W,22K OHM	1	R206
202-10948	RESSM,RO,5%,1/10W,390 OHM	1	R231
202-11071	RESSM,RO,5%,1/4W,75 OHM	1	R112
202-11072	RESSM,RO,5%,1/4W,220 0HM	8	R92,93,98,115,116,118,120,121
202-11683	RESSM,RO,5%,1/10W,5.1 OHM	1	R75
202-12365	RESSM,RO,5%,1/4W,110 OHM	1	R103
202-12366	RESSM,RO,5%,1/4W,22 OHM	4	R106-109
202-12368	RESSM,RO,5%,1/4W,120 OHM	6	R94,96,122,254-256
202-12369	RESSM,RO,5%,1/10W,36K OHM	4	R61,64,152,184
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	2	R85,87
203-11080	RESSM,RO,1%,1/10W,1.15K OHM	4	R55,56,69,70
203-11727	RESSM,RO,1%,1/10W,562 OHM	4	R3,8,11,13
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	4	R57,59,71,73
203-12167	RESSM,RO,1%,1/10W,374 OHM	1	R110
203-12363	RESSM,RO,1%,1/10W,90.9 OHM	1	R111
203-12372	RESSM,THIN,1%,1/10W,4.99K OHM	2	R89,91
203-12373	RESSM,THIN,1%,1/10W,7.68K OHM	2	R54,68
203-12374	RESSM,THIN,1%,1/10W,8.06K OHM	4	R58,60,72,74
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	6	R78,80,81,83,88,90
203-12720	RESSM,THIN,1%,1/10W,2.94K OHM	2	R51,66
203-12721	RESSM,THIN,1%,1/10W,11.8K OHM	2	R53,67
203-12722	RESSM,THIN,1%,1/10W,49.9K OHM	4	R5,7,14,16
203-12723	RESSM,THIN,1%,1/10W,102 OHM	2	R34,47
203-12724	RESSM,THIN,.1%,1/10W,4.99K OHM	28	R4,6,12,15,17-24,29-33,35-37,42-46, R48-50
240-00613	CAP,ELEC,22uF,25V,RAD	1	C182
240-00614	CAP,ELEC,47uF,16V,RAD	4	C39,48,84,87
240-06096	CAP,ELEC,10uF,25V,RAD,NON-POL	6	C3,4,11,12,92,93
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	5	C100,103,108,177,208
240-12725	CAP,ELEC,220uF,25V,NONPOL,20%	4	C23,24,31,32
241-09366	CAPSM,TANT,10uF,25V,20%	4	C25,30,33,38
241-09798	CAPSM,TANT,10uF,10V,20%	14	C57,59-61,63,68,70-72,75,86,115 C159,160
244-00662	CAP,MYL,.1uF,5%,RAD	1	C196
244-04960	CAP,MYL,1uF,5%,RAD	2	C195,206
244-06173	CAP,MYL,4700pF,5%,RAD	4	C45,46,54,55
244-06176	CAP,MYL,.047uF,5%,RAD	1	C117
244-06177	CAP,MYL,.33uF,10%,RAD	2	C172,173
244-10423	CAP,MYL,.22UF,10,RAD	5	C95,97,98,101,178
245-09291	CAPSM,CER,470pF,50V,NPO,5%	2	C109,110
245-09875	CAPSM,CER,.1uF,50V,Z5U,20%	97	C5,8,13,16,17,22,26,29,34,37,41,42 C47,50,51,56,58,62,64-67,69,73,74 C76-78,83,85,88,91,113,114,116,119 C122-126,130,131,136-138,141, C144-152,155-157,161-171,174-176, C180,181,183-194,197-205,207
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	4	C118,120,128,158
245-10561	CAPSM,CER,100pF,50V,COG,5%	12	C80,81,89,90,104-107,132-135
245-10562	CAPSM,CER,150pF,50V,10%	12	C1,2,9,10,94,96,99,102,111, C112,121,179

PART NO.	DESCRIPTION	QTY	REFERENCE
245-10588	CAPSM,CER,33pF,50V,COG,10%	5	C127,139,140,142,143
245-10977	CAPSM,CER,330pF,50V,NPO,5%	4	C43,44,52,53
245-11591	CAPSM,CER,560pF,50V,COG,5%	2	C40,49
245-11594	CAPSM,CER,2200pF,50V,COG,5%	2	C79,82
245-11625	CAPSM,CER,33pF,50V,COG,5%	13	C6,7,14,15,18-21,27,28,35,36,129
245-12070	CAPSM,CER,15pF,50V,COG,10%	2	C153,154
270-00779	FERRITE,BEAD	18	FB1-6,9-20
270-06671	FERRITE CHOKE,2.5 TURN	2	FB7,8
300-01030	DIODE,1N4004 AND 4005	5	D9-13
300-10509	DIODESM,1N914,SOT23	1	D18
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	12	D1-8,14-17
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT23	1	D19
310-10422	TRANSISTORSM,2N4403,SOT23	7	Q9-15
310-10510	TRANSISTORSM,2N3904,SOT23	5	Q4-8
310-10565	TRANSISTORSM,2N3906,SOT23	1	Q3
310-12196	TRANSISTORSM,J108,N-CH,SOT23	2	Q1,2
330-04572	IC,DIGITAL,74HCT245	1	U70
330-04674	IC,DIGITAL,74HC4538	1	U48
330-05901	IC,DIGITAL,74HC253	1	U23
330-09239	ICSM,DIGITAL,74HC74,SOIC	2	U20,39
330-09796	ICSM,DIGITAL,74AC00,SOIC	2	U42,61
330-09845	ICSM,DIGITAL,74AC174,SOIC	1	U47
330-09877	ICSM,DIGITAL,74HC174,SOIC	1	U46
330-09884	ICSM,DIGITAL,74AC32,SOIC	1	U72
330-09885	ICSM,DIGITAL,74AC74,SOIC	1	U27
330-09891	ICSM,DIGITAL,74AC157,SOIC	3	U56-58
330-10372	ICSM,DIGITAL,74HC574,SOIC	2	U65,68
330-10522	ICSM,DIGITAL,74HC04,SOIC	1	U44
330-10523	ICSM,DIGITAL,74HCU04,SOIC	3	U19,21,22
330-10524	ICSM,DIGITAL,74HC08,SOIC	3	U43,45,52
330-10525	ICSM,DIGITAL,74HC14,SOIC	1	U25
330-10526	ICSM,DIGITAL,74HC32,SOIC	1	U38
330-10527	ICSM,DIGITAL,74HC138,SOIC	2	U62,63
330-10532	ICSM,DIGITAL,74HC175,SOIC	1	U26
330-10533	ICSM,DIGITAL,74HC245,SOIC	1	U35
330-10536	ICSM,DIGITAL,74HC273,SOIC	4	U31,32,49,69
330-10537	ICSM,DIGITAL,74HC541,SOIC	7	U30,33,59,60,67,71,73
330-10589	ICSM,DIGITAL,74HC161,SOIC	2	U28,29
330-12069	ICSM,DIGITAL,74HC573,SOIC	3	U36,41,66
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	7	U1-3,6,7,12,13
340-10567	ICSM,LIN,MC34164,+5V MON,SOIC	1	U53
340-11045	ICSM,LIN,LM393,DUAL COMP,SOIC	1	U64
340-11575	ICSM,LIN,7805,+5V REG,TO263	1	U11
340-11576	ICSM,LIN,7905,-5V REG,TO263	1	U9
340-12367	ICSM,LIN,OP275,DU OP AMP,SOIC	2	U4,5
345-12038	ICSM,INTER,75ALS180,DR/RC,SOIC	1	U14
345-12059	ICSM,INTER,CS8402A,XMTR,SOIC	2	U17,18
345-12060	ICSM,INTER,CS8412,RCVR,SOIC	1	U15
346-10508	ICSM,SS SWITCH,74HC4053,SOIC	1	U16
350-09749	IC,GAL,20V8,PCM-80,HOST,V1.00	1	U40
350-09976	IC,SRAM,128KX8,1M,100NS	1	U54
350-10374	ICSM,DRAM,256KX4,80NS,SOJ	2	U50,51
350-12666	IC,ROM,27C040,PCM91,V1.00	1	U55
355-04283	IC,CONV,ADC0804	1	U37
355-12333	ICSM,DAC,CS4390,24BIT,STR,SSOP	1	U8
355-12349	ICSM,ADC,AKM5391,24BIT,STR,SOP	1	U10

PART NO.	DESCRIPTION	QTY	REFERENCE
365-09774	ICSM,uPROC,uPD70208(V40),8MHz	1	U34
375-02247	IC,OPTO-ISOLATOR,6N138	1	U24
390-12144	CRYSTALSM,16.000MHz,PAR,18pF	1	Y3
390-12361	CRYSTALSM,11.2896MHz,PAR,HC49	1	Y2
390-12362	CRYSTALSM,12.288MHz,PAR,HC49	1	Y1
410-03584	RELAY,2P2T,LOW LEVEL,DIP,12V	2	RY1,2
453-03993	SW,PBPP,2P2T,PCRA,2.5MM TRAV	1	SW1
460-04598	BATTERY,LITH,3V,FLAT	1	BAT1
470-07652	XFORMER,PULSE,AES,1:1	2	TX1,2
490-02356	CONN,JUMPER,.1X025,2FCG	5	W1-3; W4 PINS 1 & 2;W7 PINS 2 & 3
510-02899	CONN,POST,100X025,HDR,3MC	2	W4,7
510-03961	CONN,POST,100X025,HDR,2MCG	3	W1-3
510-06568	CONN,POST,079,HDR,6MC	1	J21
510-07785	CONN,RCA,PCRA,1FCGX2,VERT	1	J12
510-09765	CONN,POST,079,HDR,10MC	1	J22
510-09773	CONN,MEM CARD,PC,68PIN,CONTACT	1	J23
510-09783	CONN,POST,100X025,36X2MCG,ELEV	1	J16
510-09790	CONN,DIN,5FC@180DEG,PCRA,SHLD	3	J13-15
510-10880	CONN,XLR/JACK,3FC,1/4"TRS,PCRA	2	J1,2 (Replace w/ 510-13799; use screw: 641-11466
510-10881	CONN,XLR,3MC,PCRA,PLASTIC CMPT	3	J3,7,11
510-10884	CONN,JMP,.6X2.5mm,7FC,TRAP	2	J18,19
510-11086	CONN,XLR,3FC,PCRA,LATCH,SMALL	1	J10
510-12636	1/4"PH JACK,PCRA,3C,SW-TR,G,NR	4	J5,6,8,9
520-04425	IC SCKT,24 PINX.3",PC,LO-PRO	1	U40
520-09736	IC,SCKT,32 PIN,PC,TIN,LO-PRO	2	U54,55
620-10413	LUG,#4,INT STAR,RCA GND	1	J12
635-09770	SPCR,SWAGE,4-40X7/8,1/4RD,BR	4	HOST TO DSP BD
680-09757	CABLE,XITION/SCKT,20C,6"	1	DISPLAY TO HOST-J20
680-12718	CABLE,HSG/ST&T,6C,26/8.5,SLV	1	PWR SPLY TO HOST-J4,17
710-12620	PC BD,HOST,PCM81/91	1	

DSP BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
202-09894	RESSM,RO,5%,1/10W,1M OHM	1	R48
202-09897	RESSM,RO,5%,1/10W,470 0HM	14	R3,8,17,21,28,44,50,55,59,61,70-72,94
202-09899	RESSM,RO,5%,1/10W,47 OHM	78	R1,2,4-7,9-16,18-20,23-27,29-43,45-47 R49,51,52,54,56-58,60,62-69,73-93,95
202-10890	RESSM,RO,5%,1/10W,220 OHM	2	R22,53
241-09798	CAPSM,TANT,10uF,10V,20%	5	C1-5
245-09869	CAPSM,CER,.001uF,50V,Z5U,20%	27	C8,9,13,16,17,19,21,22,24,28,31-33,35 C37,40,42,45,47,49,54-56,58,60,62,64
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	30	C6,7,10-12,14,15,18,20,23,25,29,30 C34,36,38,39,41,43,44,46,48,50-53,57 C59,61,63
245-09895	CAPSM,CER,10pF,50V,COG,10%	2	C26,27
330-07538	IC,DIGITAL,PEAK DETECT,PDC412	1	U1
330-09239	ICSM,DIGITAL,74HC74,SOIC	1	U25
330-09350	IC,DIGITAL,LEXICHIP 2	2	U2,35
330-09796	ICSM,DIGITAL,74AC00,SOIC	1	U33
330-09797	ICSM,DIGITAL,74AC04,SOIC	1	U31
330-09845	ICSM,DIGITAL,74AC174,SOIC	2	U13,38
330-09877	ICSM,DIGITAL,74HC174,SOIC	4	U5,6,39,40

PART NO.	DESCRIPTION	QTY	REFERENCE
330-09884	ICSM,DIGITAL,74AC32,SOIC	2	U34,51
330-09885	ICSM,DIGITAL,74AC74,SOIC	2	U7,32
330-09886	ICSM,DIGITAL,74HC373,SOIC	2	U29,36
330-09890	ICSM,DIGITAL,74AC541,SOIC	2	U24,41
330-09891	ICSM,DIGITAL,74AC157,SOIC	8	U11,16,17,26,43,44,49,50
330-10372	ICSM,DIGITAL,74HC574,SOIC	6	U18-23
350-10373	ICSM,DRAM,256KX16,80NS,SOJ	2	U12,27
350-10374	ICSM,DRAM,256KX4,80NS,SOJ	2	U8,28
350-10376	ICSM,GAL,16V8,PCM90,LEXX,V1.00	1	U9
350-10377	ICSM,GAL,16V8,PCM90,LEXY,V1.00	1	U45
350-10378	ICSM,GAL,16V8,PCM90,SLV1X,V1.0	1	U14
350-10379	ICSM,GAL,16V8,PCM90,SLV1Y,V1.0	1	U42
350-10380	ICSM,GAL,20V8,PCM90,SLV2X,V1.0	1	U15
350-10381	ICSM,GAL,20V8,PCM90,SLV2Y,V1.0	1	U37
350-11238	ICSM,SRAM,8KX8,25NS,SOJ	4	U3,4,46,47
365-09883	ICSM,uPROC,Z80,CMOS,10MHz,QFP	2	U10,48
390-09791	CRYSTAL,25.8MHz	1	Y1
390-10382	CRYSTAL OSC,1/2,20.000MHz	1	U30
510-09784	CONN,POST,100X025,36X2FCG,TEMP	1	J1
710-10390	PC BD,DSP,PCM-90	1	

POT BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
200-09761	POT,RTY,PC,10KAX2,6MMFL,16,20L	1	R201
680-10885	CABLE,RIB,24-26G,7CX.1,1.5",NW	1	J104
710-09813	PC BD,POT,PCM80&1/90&1	1	

HEADROOM BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
430-03896	LED,GRN,RECT,.197X.079	6	D103-105,108-110
430-03897	LED,YEL,RECT,.197X.079	2	D102,107
430-03898	LED,RED,RECT,.197X.079	2	D101,106
680-10886	CABLE,RIB,24-26G,7CX.1,5.5",NW	1	J101
710-09838	PC BD,HDRM,PCM80&1/90&1	1	

SWITCH BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
300-01029	DIODE,1N914 AND 4148	3	D112,115,119
430-09818	LED,GRN,T1,LITON,20DEG,12MCD	9	D111,113,114,116-118,120-122
453-09771	SW,PB,1P1T,6MM SQX7MM H,160GF	12	SW2-13
680-09763	CABLE,079,SCKT/SCKTRA,10C,2.0"	1	J102
710-09836	PC BD,SW,PCM80&1/90&1	1	

ENCODER BOARD

PART NO.	DESCRIPTION	QTY	REFERENCE
202-00514	RES,CF,5%,1/4W,100 OHM	4	R202-205
245-03610	CAP,CER,.01uF,100V,Z5U,AX	4	C200-203
452-09762	SW,RTY,ENCODER,36 POS,VERT MNT	2	SW14,15
680-09764	CABLE,079,SCKT/SCKTRA,6C,2.0"	1	J103
710-09837	PC BD,ENC,PCM80&1/90&1	1	