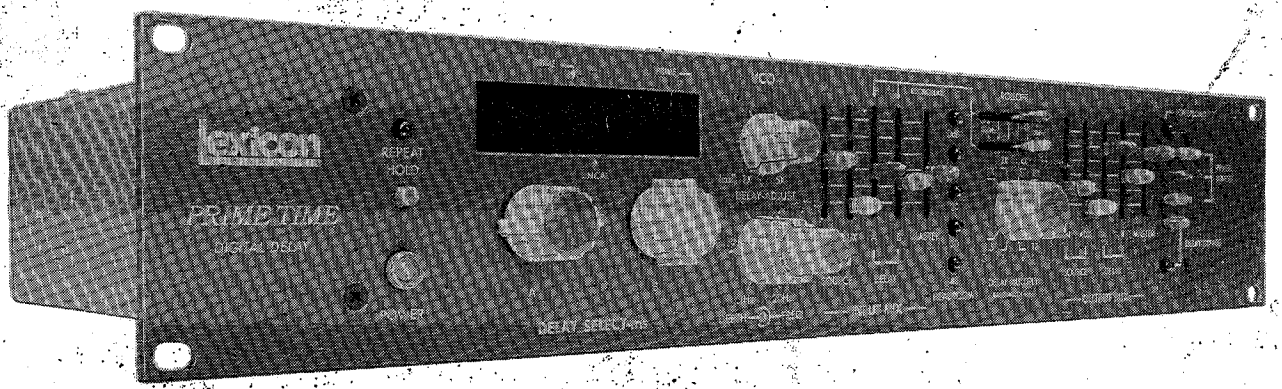
PRIME TIME

MODEL 93
DIGITAL DELAY
PROCESSOR



Service Manual

lexicon

PRIME TIME MODEL 93 SERVICE MANUAL

OUTLINE

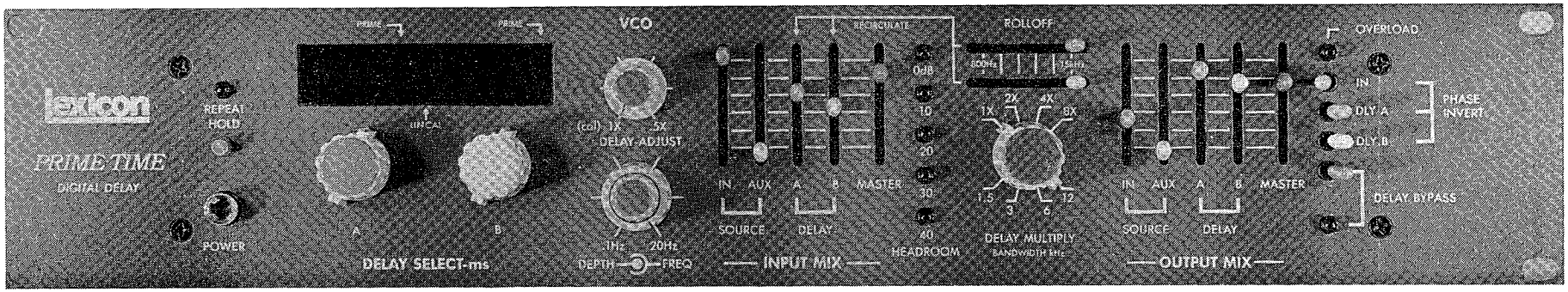


FIG. 1.0 FRONT AND REAR PANELS

1.Ø INTRODUCTION

This service manual is designed to provide complete service and maintenance information for the PRIME TIME Model 93 Digital Delay System.

Complete maintenance of the Model 93 requires a good understanding of both analog and digital circuitry.

Efficient service of the Model 93 calls for a 1ØMHz (min) dc triggered sweep dual trace scope, a low distortion audio generator (<.Ø4% THD at 1kHz), an ac VTVM with a 1mV full scale range, a 1ØMHz frequency counter and a good multimeter. Additional equipment such as a pulse generator, a distortion analyzer,and a delay time measuring device will be helpful but not absolutely essential for Model 93 servicing.

PRIME TIME owners who do not have the right equipment, or who are experiencing difficultly with a knotty problem are encouraged to refer the servicing problem to the factory by module or mainframe shipment.

1.1 GENERAL DESCRIPTION

The PRIME TIME Model 93 is a versatile digital delay processor. It incorporates all the necessary control features for on-board generation of delay and reverb effects. Flexible mixing facilities, varied time base modification capabilities , and special effects controls provide the studio engineer or entertainer in live performance with a wide variety of audio enhancement capabilities not previously available in a single package.

Design of the Model 93 is an outgrowth of two previous generations of highly regarded digital delays. Use of Low Power Schottky TTL and 4K-bit RAMS (Random Access Memories) for memory results in reduced power consumption, lower internal operating temperatures and increased reliability. Thus we're confident that PRIME TIME will more than live up to our excellent reputation for reliability.

We have maintained our standards of audio performance, as seen by PRIME TIME's 9ØdB dynamic range, distortion of less than .1%, and flat frequency response. In addition, use of sophisticated elliptical filters improves aliasing performance and eliminates sampling components.

PRIME TIME is a mono delay line with two independant delay taps. The output mixer allows mixing the two taps together into the Master Output, plus either or both of two input sources. In addition the two delay taps are available on the rear panel with individual

level controls. Phase invert switches enable phase relationships to be varied in the output mix. The input mixer produces a mix of the two sources, plus frequency contoured recirculating delays,into the delay line. The input mix is also available on the rear panel.

Multi-position Delay Select switches enable selecting delay times up to 128ms at full bandwidth. This is expandable to 256ms with the optional add-on memory. The Delay Multiply control allows the selected delay to be increased by a factor of 2,4 or 8 with a corresponding reduction in band-pass. Thus you can achieve over 2 seconds of delay with PRIME TIME. The Delay Adjust control allows continuous variation of delay time, from 100% to 50% of the selected value. With this control any delay time from .25ms to 2048ms can be obtained.

Special effects can be obtained with the low frequency VCO continuously modulating the delay time. The Repeat Hold switch allows data to be locked up in memory and continuously repeated. The delay time can be modulated by an external waveform, and the Repeat Hold and Bypass functions can be remotely controlled with a foot switch.

Rugged construction and the aforementioned electronic reliability ensure consistant, long term use. Sufficient modularity has been retained internally to make servicing simple and efficient.

For complete operating instructions and applications information, refer to PRIME TIME Owner's Manual (070-01060).

1.2 SPECIFICATIONS

*Dynamic Range:	95dB typical; 90dB min. "A" weighted 90dB typical; 86dB min. unweighted
**Total Distortion and Noise:	less than 0.08% at limit reference level and 1kHz less than 0.3% at -34dB

*Defined as the ratio of the 1kHz output level at reference limit level to the output level with 600 ohms across the input. Unweighted noise is measured over the bandwidth of 20Hz to 20kHz. Weighted noise is measured according to the ANSI "A" curve.

**Input sensitivity set so that an 18dBm input corresponds to "0" LED just going out (this is "limit level"). Output sensitivity set to produce +18dBm with 600 ohms load under these conditions.

Frequency Response:	20Hz to 12kHz +1, -2dB measured 12dB below limit level with Delay Muliply at X1; bandpass is reduced to 6kHz, 3kHz, and 1.5kHz with Delay Multiply at X2, X4, and X8 respectively.
Delay Capacity:	128ms at full bandpass--standard; 256ms at full bandpass with optional add-on Delay Memory Module
Delay Multiply:	Extends delays by X2, X4, or X8. (2048ms with add-on Memory option)
Delay Taps:	Two, individually selectable in 60 steps with digital display of each setting
VCO Modulation:	Depth adjustable from 0 to 100% of Delay Adjustment range; frequency adjustable from 0.1 to 20 HZ
Delay Accuracy:	0.01% long term in Cal. mode plus .12ms delay offset
Inputs:	Main and auxilary inputs: balanced, 40K input impedance, 20dB gain switch allows matching of levels from -18dB to +18dB at limiting, XLR-3 type connectors
Master Output:	Transformer isolated, balanced, 90 ohms max., adjustable to +18dBm max., XLR-3 type connectors
Supplemental Outputs:	Delay A, Delay B, and Input Mix, 100 ohms max, single ended, 1/4" phone jack connectors; A and B Outputs adjustable from +8 to +18dBm
Input Mixer:	5 faders for Main Input, Auxiliary Input, Delay A and B recirculation, and Master; 5 level LED Headroom Indicator verifies proper mix level
Recirculated Delay Rolloff:	Individual control for recirculated Delays A and B from 15kHz to 800 Hz
Output Mixer:	5 faders for IN Input, Aux Input, Delay A, Delay B and Master Out with overload indicator
Repeat/Hold:	Repeats signal in delay memory indefinitely without audio degradation; alternate action with LED indicator
Delay Bypass:	Bypasses or cuts in delay system; when bypassed connects Input Mix to Master Output; switch actuated with LED indicator
Remote Control Capability:	1/4" phone jacks on rear panel for Repeat/Hold foot switch, Delay Bypass foot switch, and Delay Adjust foot pedal pot or 0-10 volt signal
Phase Inversion:	3 switches allow Input, Delay A and/or Delay B to be inverted

Pre-emphasis/ De-emphasis:	75/15 us; max boost 12dB at 12kHz
Size:	Standard 19" rack mount, 3 1/2" high x 11 1/2" deep (483 x 89 x 292 mm)
Weight:	11 lbs. (5 kg); 15 lbs. shipping
Power:	115/230V +/-10% switch selectable (100/200V available as option), 50/60Hz, 35 watts max; standard IEC 3 wire power connector and cord
Protection:	Mains fused; secondary supplies fused, with over voltage crowbar and/or current limited with thermal protection
Connector Option:	Substitution of tip-ring-sleeve 1/4" phone jacks for all XLR-3 type connectors

1.3 INITIAL INSPECTION

Prior to applying power, determine that the Model 93 is set for the correct mains voltage and that the correct fuses are installed. The power mains voltage selector switch and fuses are located on the motherboard to the rear of the power on/off switch. The correct fuse ratings are as follows:

115 Volts -- 0.75A "Slo Blow" (1 1/4 x 1/4 inches)
230 Volts -- 0.375A "Slo Blow" (1 1/4 x 1/4 inches)
5 Volt supply fuse -- 2.5A 7AG medium acting
(7/8 x 1/4 inches) Littlefuse 30302.5 or equivalent

Lexicon normally sets the fuse rating and voltage to match the destination country prior to shipment. The voltage setting is marked on the rear panel. If not familiar with the overall Model 93 operation refer to the PRIME TIME Model 93 Owner's Manual, Lexicon Document No. 070-01060.

1.4 POWER UP

With power applied and no audio signal present only the numerical displays should illuminate (VCO in cal position, all mixer pots down). Failure to do so indicates a problem with the unregulated 8.5V supply. If the headroom indicators are illuminated the cause should be determined before proceeding with performance testing.

1.5 CONTROL FEATURES

1.5.1 The Mixers

There are two four-in, one-out mixers with master level

controls. The output mixer provides a mix of two inputs and the two delay taps. Phase inversion is available for the IN input and the two delay taps.

The input mixer allows a mix of two inputs and the two delay taps (recirculation) to feed the delay line. The two recirculated delay taps can be frequency contoured with the Rolloff controls which provide a 6dB/ octave rolloff above the frequency indicated.

The two balanced inputs are electronically coupled into PRIME TIME. With the 20dB gain switch PRIME TIME accepts input levels from -18dBm to +18dBm.

The level going into the delay line is monitored on the 5 position headroom indicator to allow optimal use of available dynamic range. Output overload is indicated by the Overload LED. The Master output fader does not affect output overload.

1.5.2 DELAY SELECTION

The 60 position Delay Select switches individually set delay times for the two delay taps. Delays are stepped between 0 and 256ms (milliseconds). For machines without the optional memory extension, maximum delay time is 128ms. Selection of a switch position greater than 128ms will result in illumination of the lower left decimal point of the display. In this case, actual delay is 128ms. For machines with the memory expansion option, all delay times are as indicated on the delay time display. Switch selection of a prime number delay time results in illumination of the Prime indicator. This is useful for obtaining maximum echo density in recirculation type effects.

The Delay Multiply switch allows the selected delay time to be increased by a factor of 2, 4 or 8 with a corresponding reduction in bandwidth (bandwidth is 6kHz , 3kHz and 1.5kHz, respectively). With the Delay Multiply switch in 8X and the Delay Select on 256ms, PRIME TIME yields over 2 seconds of delay.

1.5.3 VCO

With the Delay Adjust control in the "cal" position (full CCW) the master clock is generated by a stable crystal oscillator. In this position, displayed delay times are accurate to within 250us (micro seconds). Turning the delay adjust control clockwise results in illuminating the "uncal" indicator. With the "uncal" indicator lit, the master clock is generated by a high frequency voltage controlled oscillator(VCO). Turning the Delay Adjust clockwise results in changing the delay time from 100% to 50% of the indicated value.

In addition to the manual control of delay time with the Delay Adjust, PRIME TIME has a low frequency (.1 Hz to 20 Hz) triangle generator which can also be used to modulate the delay time. The

frequency of this triangle wave is varied with the FREQ control and the amplitude is increased by turning the Depth control clockwise. With the Depth control full clockwise, delay time is continuously varied from 100% to 50% (of the indicated value) and back again.

1.5.4 OTHER FEATURES

When the Repeat Hold button is pushed, the Repeat Hold LED comes on. Data is locked up in memory and is repeated indefinitely, similiar to a tape loop (until Repeat Hold is pressed again). No new information is written into memory. Length of the repeating segment is the same as the maximum delay time available (eg. 256ms in 1x with the memory extension, and 2048ms in 8x with the memory extension). The Delay A and B taps are similar to two playback heads in the tape loop. Varying the Delay A and B delay times is analagous to changing the relative position of the two playback heads.

The Delay Bypass switch routes the output of the input mixer to the Master Output when the led is illuminated, bypassing the delay circuitry. In addition, the two recirculation paths into the input mixer are opened so the signal appearing at the Master Output in Bypass is a mix of only the two inputs.

The Repeat Hold and Delay Bypass functions can be remotely controlled with foot switches which plug into the rear panel of PRIME TIME. The VCO can be externally modulated by a 0-10V control signal or a 50K linear pot via a 1/4" phone jack on the rear panel.

In addition the two delay taps are available as individual outputs on the rear panel with individual level controls. The output of the input mixer is also available. All three signals are on 1/4" phone jacks available through the rear panel.

For further operating instructions and applications information, refer to PRIME TIME Owner's Manual, Lexicon Document #070-01060.

1.6 CONSTRUCTION DETAILS

The PRIME TIME front panel is 3 1/2" high and mounts in a standard 19" relay rack. Chassis construction is two pieces: the front panel is secured via two angle brackets to the aluminum wrap-around chassis. Top and bottom covers are secured to the chassis by seven 6-32 1/4" pan head screws with internal star washers. The top cover has no lip, to allow clearance for the display window.

Internal construction was designed for ease of assembly and dis-assembly. This involves minimal hand wiring and modular printed circuit construction. Refer to Figure 6.0.1 for printed circuit board location. Front panel controls are mounted on a vertical printed circuit board located behind the front panel. See section 5.0.1 for front panel and module removal instructions.

2.Ø CALIBRATIONS

Calibrations are originally done at the factory and should be good for the life of the machine. Should component replacement become necessary, the affected circuit will probably need recalibration. Use of a non-magnetic screwdriver is recommended.

2.1 FILTERS

The analog section of the PRIME TIME employs precision elliptical low pass filters on the input and outputs. These filters exhibit very steep rolloff; in the input they are used to eliminate high frequencies which could cause aliasing of the sampled signal, and in the outputs they filter out the sampling frequency components to leave only the original audio signal. The filters employ frequency dependent negative resistance (FDNR) elements to eliminate the use of inductors. The FDNR elements are fine tuned for optimum performance of the filters.

The Delay Multiply must be set to X1 for this calibration procedure. Refer to Motherboard Schematic, Part 2 (Fig. 6.2.2)

Input Filter:

1. Remove U16
2. Inject 16,ØØØ Hz (+/-1ØØ Hz) (+13 dBm +/-2dB) at R1Ø1
3. Adjust R1Ø2 for a null at Pin 1 U13. Null should be at least -35 dBm
4. Inject 22,53Ø Hz (+/-15Ø Hz) (+13 dBm) at R1Ø1
5. Adjust R93 for a null at Pin 1 U13. Null should be at least -35 dBm
6. Replace U16

Output Filters:

Delay A (Delay B in parentheses)

1. Remove the Analog Daughter board. Insert a 1Ø-pin male connector (Molex #22-Ø3-21Ø1) in J7
2. Inject 16,ØØØ Hz (+/-1ØØ Hz) at +13 dBm (+/-2 dB) on J7-6 (J7-8)
3. Adjust R37 (R24) for a null at Pin 1 U9 (U4). Null should be at least -35 dBm
4. Inject 22,53Ø Hz (+/- 15Ø Hz) at +13 dBm on J7-6 (J7-8)
5. Adjust R61 (R53) for a null at Pin 1 U9 (U4). Null should be at least -35 dBm
6. Replace Analog Daughter board.

2.2 CONVERTERS

Note: Reference numbers for Rev. 1 Analog Daughter boards are different from those for Rev. 3 boards. Reference numbers in parentheses refer to Rev. 3 PC boards.

Comparator:

The nominal internal level in PRIME TIME is +13 dBm (+5V peak). The comparator must be calibrated so that this level causes limit (Ø dB indicator on headroom to just light).

1. At 1 kHz, adjust input level to read +13 dBm (+5V peak) at pin 5 U11 (U2) (LF398).
2. Adjust R37 (R9) (analog daughter board) so the Ø dB headroom indicator just comes on.

DAC:

The D/A converter must be calibrated so that with +13 dBm IN we get +13 dBm OUT.

1. Make sure comparator is calibrated as above.
2. Set both delay taps on Ø ms
3. Adjust R38 (R18) for +13 dBm (+5V peak) at pin 7 U2 (U8).

2.3 VCO CALIBRATION:

The PRIME TIME VCO is a Texas Instrument 74S124 calibrated to run between 4.992 MHz and 9.984 MHz (2:1 range). There are two adjustments, range and frequency, which are non-interactive if done in the proper sequence. Refer to Motherboard Schematic, Part 3 (Fig. 6.2.3)

1. On front panel, turn Depth control full CCW.
2. On front panel, set manual tune (Delay Adjust) full CCW ("uncal" mode)
3. On motherboard, adjust C188 for f = 4.992 MHz (+/-.Ø25 MHz) at pin 8 U57 (or pin 7 U62). R159 should have no effect.
4. Turn Delay Adjust full CW
5. Adjust R159 for f = 9.984 MHz (+/-.Ø25 MHz)
6. Turn Delay Adjust back to full CCW; recheck for f = 4.992 MHz

Alternate VCO calibration procedure:

This procedure tunes the VCO by ear and can be used if an accurate frequency counter is not available.

1. With the Delay Multiply on 1x, inject a 1 kHz limit level tone into the IN input (Delay Adjust in "cal" position).

2. Monitor a mix of the input and Delay A on the output mixer, using headphones or speakers to listen to the result.

3. Press Repeat Hold

4. On the front panel, set the Delay Adjust control full CCW ("uncal" mode). You are now listening to a mix of the original tone and a repeating segment of the tone.

5. Monitor the output while adjusting C188. Adjust C188 to "zero beat" the tones.

6. Put the Delay Multiply on 2x. Turn the Delay Adjust full CW.
7. Adjust R159 to again "zero beat" the tones.
8. Go back to Delay Multiply on 1x and Delay Adjust full CCW ("uncal" mode) and check that the output is still in tune.

When done carefully, this procedure is quite accurate.

3.Ø PERFORMANCE TESTS

3.1 HEADROOM INDICATOR AND GAIN RANGE

Apply a 1kHz tone at +13dBm (+5V peak) to the IN Input (with the input gain switch in the ØdB position). In the input mixer, raise the IN and MASTER pots. As you do so the headroom indicator LED's should come on in sequence. Set the input mixer so the top LED (ØdB) is just extinguished. Now reduce the generator output 14dB and then in 1ØdB steps and observe the operation of the headroom indicator. Each 1ØdB drop should extinguish an additional indicator -- below -3ØdBm none of the indicator LED's should be illuminated. Set the Delay Select for Ø ms and raise the Delay A and Master pots in the output mixer. Set the output mixer for +1ØdBm at the Master Output. Verify a 1ØdB drop in output amplitude for each 1ØdB drop in input amplitude. Next examine the signal output at the point where headroom indicator changes range by slowly adjusting the signal generator amplitude. No abrupt change in amplitude should be observed at the output. Repeat for Delay B in the output mixer.

3.2 DELAY TIME TESTING

Accurate testing of delay time can be performed in one of several ways. A simple straight-forward method is presented in the following test. If the required instrumentation is not available, a reasonable check on delay can be performed by a simple binaural listening test.

DELAY MEASUREMENT WITH TRIGGERED SCOPE AND TONE BURST OR PULSE GENERATOR SOURCE

This test requires a tone burst or pulse generator with an amplitude output of about 1 to 1Ø volt peak and a calibrated triggered sweep oscilloscope (either single or dual trace). Connect equipment as shown in Fig. 3.1.

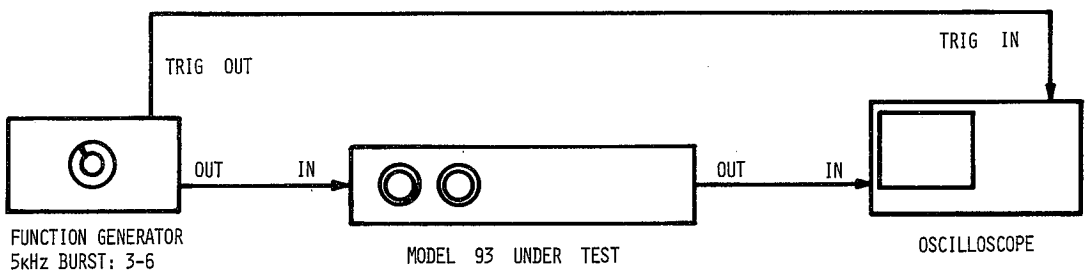


FIG. 3.1 DELAY TIME TESTING

Adjust scope to trigger on the leading edge of each tone burst or pulse. Burst frequency or pulse width are not critical, however several cycles of 5kHz or 500us pulse width are reasonable.

This test will initiate sweep when each pulse or burst is introduced at the input of the PRIME TIME. The delayed burst time can be measured directly on the oscilloscope face.

The following circuit may be used to generate pulses at a 2 per second repetition rate. It may be powered by either a six volt battery or a simple 5 volt logic supply.

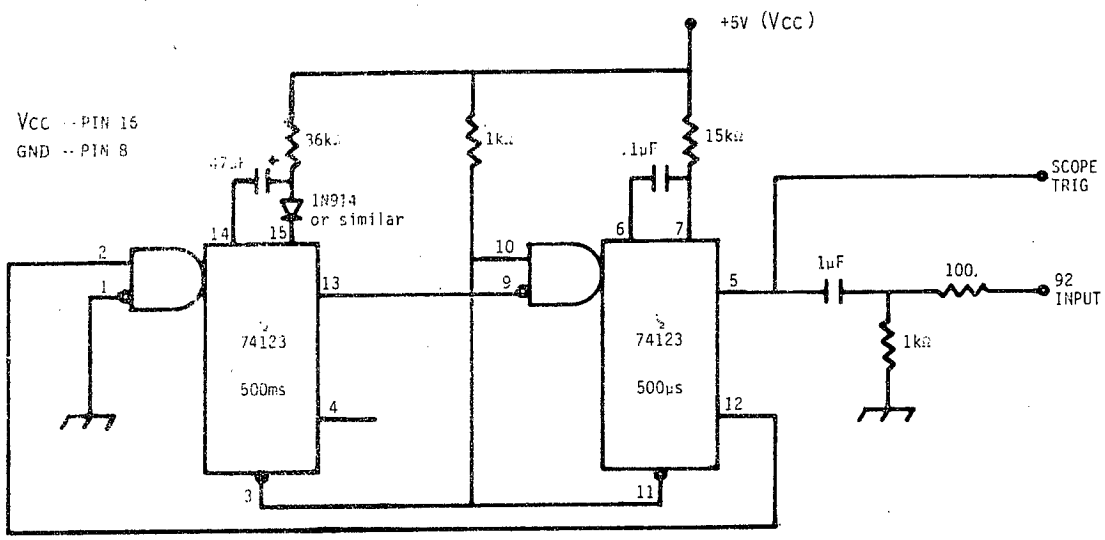


FIG. 3.2 PULSE GENERATOR FOR DELAY TIME TEST

3.2.1 DELAY SELECT

As the Delay Select control for a channel is stepped through the 60 positions, the time seperation between the trigger pulse and the output pulse as observed on the oscilloscope should increase.

3.2.2 DELAY MULTIPLY

As the Delay Multiply switch is turned, you should see a corresponding change in delay time on the oscilloscope. In "cal" mode, actual delay time should be the value displayed in the window times the multiplier setting. For example, with the Delay Select set for 30ms and the Delay Multiply on 4x, observed delay should be 120ms.

3.2.3 VCO

Refer to Motherboard Schematic, Part 3 (Fig. 6.2.3)

3.2.3.1 DELAY ADJUST

In "uncal" mode, actual delay time will be from 100% to 50% of the value indicated by the Delay Select and Delay Multiply controls (Depth control full CCW). As the Delay Adjust control is turned clockwise the delay time should decrease, and you should see the output pulse move closer to the trigger pulse on the oscilloscope screen.

3.2.3.2 FREQUENCY:

Turn Depth full CW. Output pulse should now be moving back and forth across scope face. Vary FREQ knob and verify that the frequency of modulation is changing.

To verify frequency range set FREQ full CCW and measure period of excursion (max delay to min delay and back again). This should be 10 sec (+/-2.0 sec).

Set FREQ full CW and verify 50ms (+/-7ms) period of triangle at pin 6 U65.

3.2.3.2a SYMMETRY:

Observe pin 6 U65. With FREQ on 20 Hz, 1/2 cycle should be 25ms (+/-3.5ms); with FREQ on .1 Hz, 1/2 cycle should be 5 sec (+/-1 sec). To observe low FREQ period, observe output as in 3.2.3.2 above.

3.2.3.3 DEPTH

Observe pin 1 U64. Set FREQ to 20 Hz. As Depth is varied, amplitude of triangle should change. Set Depth to 12 o'clock. As Delay Adjust is varied, D.C. offset of triangle should vary. Set Depth full CCW. As Delay Adjust is varied, you should observe a varying D.C. voltage (D.C. range = 2.2V to 3.7V).

3.3 INPUTS, MIXERS, INVERTERS, ROLLOFF

PRIME TIME has two four in, one out mixers: one for input to the delay line and one for the Master output.

The Input Mix supplies the input signal to the digital delay processor. It consists of four functions with independently adjustable level controls and a Master control which determines the level of the resultant blend. The four functions are two identical but independent inputs, IN and AUX, and two delay taps, A and B. The delay taps are recirculated from the outputs through variable 6 dB/ octave Rolloff filters which adjust the high end rolloff FREQ from 15 kHz to 800 Hz. Optimum levels can be achieved by proper adjustment of the Input Mix Master control which provides up to 13dB of gain and

up to 18dB of attenuation.

The two inputs, IN and AUX, are identical active differential stages with switchable 20dB gain. With the gain switch in the ØdB position, input levels from +1dBm to +18dBm should be able to limit the delay line (ØdB headroom just lit).

a. Input 1 kHz at +1 dBm (+/-.5dB) and verify that there is a combination of IN (AUX) and Master settings that will cause the Ø dB Headroom indicator to light.

b. Repeat for 1 kHz +18 dBm input.

c. With gain +2Ø dB, verify limit with -18 dBm and +1 dBm (+/-.5 dB)

The Output Mix supplies signal to the Master Output. Like the Input Mix, it blends four functions of which two are the inputs, IN and AUX, and two are the delay taps, A and B. The overall level is adjusted with the Master control which can provide from zero to infinite attenuation. When in danger of overloading the output stage, the Overload indictor will light. The Overload function indicates the levels of the four mixer functions only and is not affected by the Master control. For additional flexibility IN, A, and B functions can be inverted with their respective Phase Invert switches before the Output Mix. The Phase Invert switches also determine the phase of the recirculated delays to the Input Mix.

To verify proper output levels set up input to just limit PRIME TIME. Set Delay A full up in output mix. Verify that with Master control you can get +18 dBm OUT (Overload indicator should not be lit) with 6ØØ ohm load. Repeat for delay B.

With input at +13 dBm, verify that Overload indicator works by bringing up IN in Output Mix (all others down).

To verify operation of all pots:

a. Apply 1 kHz at +13 dBm to both IN and AUX inputs.

b. With input Master about halfway up, verify operation of IN and AUX pots on input mixer by observing pin 1 U16 (Motherboard).

c. Set IN and Master so -2Ø dB headroom light is lit. Verify operation of recirculated A and B by bringing these pots up and down and observing corresponding amplitude changes on pin 1 U16 (Delay = Ø).

d. Set Input Mixer to just limit with IN and Master. Put Output Master about halfway up and observe the Master output for proper operation of each pot in Output Mixer.

To verify operation of Rolloff pots:

Apply 1Ø kHz at +3 dBm. Set Input Mixer to just limit. Observing the top of the Recirculate A (or B) pot, slide the Rolloff A (or B) pot. You should see the amplitude of the waveform decrease as the Rolloff moves right to left.

To verify proper operation of Phase Invert switches, inject pulses into IN input. Observe dual trace on scope (input and Master out). Set input mixer to just limit. Push IN and Master up in Output Mix and observe scope trace. Flip invert switch and observe pulse polarity reversal(this test is also possible with a sine wave input).
Repeat for Delay A and B.

NOTE: Unless otherwise specified, all following tests are done with VCO in "cal" mode and both Delay Selects on Øms.

3.4 FREQUENCY RESPONSE

PRIME TIME ia specified at +1, -2dB from 2ØHz to 12 kHz with the Delay Multiply at 1x, referenced to ØdB at 1kHz. Typically machines will measure +Ø, -1dB.

Frequency response should be measured at 18dB below limit reference in order to avoid limiting at higher freqencies due to pre-emphasis. Apply 1kHz at +18 dBm and adjust the input mixer to just limit the delay line (ØdB headroom indicator just lit). Reduce the generator level to ØdBm and adjust the Output Mixer for ØdBm at the Master Output. ØdBm is convenient because it allows easy data interpretation. Care should be taken to account for any oscillator amplitude changes with frequency setting.

Frequency response should be done with the VCO in "cal" mode.

With the Delay Multiply switch in 2x, 4x or 8x the overall machine bandwidth should be reduced to 6kHz, 3kHz and 1.5kHz, respectively.

3.5 DYNAMIC RANGE

Dynamic range is defined as the difference in dB between the maximum possible output level and the level of the residual noise with the input terminated.

To measure dynamic range, apply 1kHz at +18dBm to the input. Adjust the input mixer to just limit the delay line. Push Delay A full up in the output mixer and adjust the output master for +18dBm at the Master Output. Now terminate the input with 15Ø ohm across the balanced input and measure the residual output noise with a good audio voltmeter, taking care not to change the mixer settings. The broadband reading (2ØHz-2ØkHz) should be at least 86dB below +18dBm, or -68dBm. If the voltmeter has an "A" weighted response the noise

reading should be at least 90dB below +18dBm, or -72dBm. Repeat for Delay B.

3.6 NOISE AND DISTORTION TESTING

Total noise and distortion is measured at 1kHz at limit level (VCO in "cal" mode and Delay Select on 0ms).

Apply 1kHz at +18dBm. Set the Input Mixer to just limit. Push Delay A full up in the Output Mixer and adjust the output Master for +18dBm at the Master Output. For this test a low distortion oscillator with about .04% max THD and a high quality distortion analyzer such as the HP331A or similar is required.

It is also recommended that instruments be floated and that attention be paid to ground loops and stray noise sources such as AC bench wiring, soldering irons, flourescent lights, etc. when trying to take distortion and noise measurements. The total noise and distortion measured at the +18dBm levels should be less than 0.08%. Next reduce the generator level by 34dB and measure noise and distortion. This measurement should be less than 0.3%. Repeat for Delay B.

3.6.1 DISTORTION IN VCO MODE

With the machine set for unity gain at +18dBm, put VCO in "uncal" mode (Delay Adjust full CCW, Depth full CCW). Distortion levels should still be less than .08%. With VCO full CW, distortion should still be less than .08%.

In VCO mode with delay, distortion readings may rise slightly. Some combinations of Delay Select and Delay Adjust settings may cause distortion to rise to approximately .14%.

3.7 DELAY BYPASS

To verify operation of Bypass, observe dual trace (input and Master Out) on scope. Inject pulses(approx. 500us pulse width) into IN input. Set input mixer to just limit. Set Delay A to 10ms. Put machine in bypass. LED should come on. (Bypass output will be inverted in earlier machines). Take machine out of Bypass, set output mix so level equals bypass level. Observe delay varying from 10ms to 0ms when switching in and out of bypass.

Next, bring up Delay A and Delay B in the Input Mix. You should see recirculating delayed pulses on the scope. Put machine in Bypass. Recirculation should stop and you should observe zero delay.

3.8 REPEAT HOLD

To verify Repeat Hold, observe Master Output on scope. Inject

pulses into IN input. Observe output. Put machine into Repeat Hold. Push all Input Mixer pots all the way down. You should still see output on the scope. Machine cannot be on Ø delay. Verify that the Repeat Hold LED works.

Push switch on and off a number of times to verify consistent operation.

3.9 REAR PANEL

To verify operation of input gain switches and Master Output, see section 3.3.

3.9.1 REAR PANEL OUTPUTS

With input just limiting, Delay A and B outputs should be adjustable from +8dBm to +18dBm (+/-.5dB) with their associated level controls. The In mix Out should be +13dBm (+/-.5dB).

3.9.2 EXTERNAL INPUTS

To verify operation of rear panel Repeat Hold and Bypass, plug in jacks and repeat 3.7 and 3.8. The Repeat Hold requires a closure to ground from a normally open momentary single pole, single throw (SPST) switch. The Delay Bypass requires a normally open SPST switch.

To verify operation of Ext. Delay input, plug in 5ØK pot and repeat Delay Adjust test. Next inject Ø - 1ØV and observe Delay Adjust results, as in section 3.2.3.1.

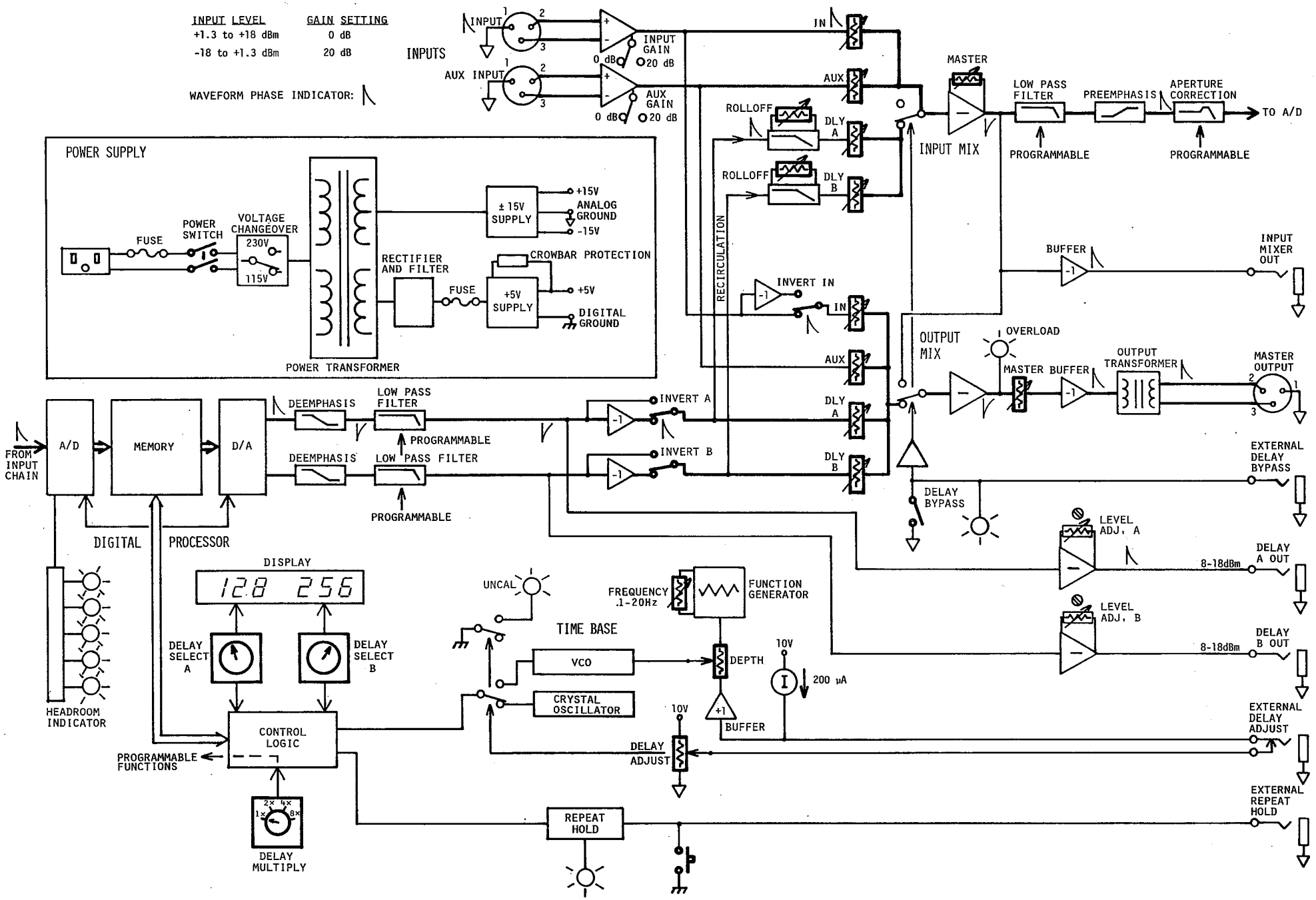


FIG. 4.1 PRIME TIME BLOCK DIAGRAM

4.Ø THEORY OF OPERATION

The Model 93 consists of four major assemblies:

1. Chassis and Motherboard assembly
2. Gain switch and ADC/DAC converter subsystem(Analog Daughter Board)
3. Memory assembly (Memory and Memory Extension Boards)
4. Front Panel assembly

The input audio signal is processed and routed to the Analog Daughter Board and its amplitude is sampled 32,ØØØ times per second (with Delay Mulitply in 1x in "cal" mode). Each sample is converted into a 12 bit floating point word. Ten bits are used for the mantissa and 2 bits for exponent. The exponent portion of the word contains gain information and the mantissa represents instantaneous signal amplitude.

The 12 bit sample is transferred in parallel to a 4Ø96 x 12 bit Random Access Memory on the Memory assembly (8192 x 12 bits with the optional Memory Extension). Each new sample is placed in the next highest memory address location. Memory address wrap-around causes each new word to over-write a previous sample which has been in the memory for exactly 128ms (256ms with memory option).

Recovery of delayed data is implemented by reading the memory at address locations trailing, or offset, behind the current input address. The larger the offset the greater the delay time. Naturally, the offset is limited by memory size and for the Model 93 corresponds to 256ms or 8192 address locations with the Memory Extension. In order to accommodate two delay taps, two read cycles are performed during each machine cycle. Each read address is dictated by its respective Delay Selector switch setting.

Recovered memory data is then converted to an amplitude sample and stored by a sample and hold circuit for one word time. These samples are then gain conditioned, filtered and processed. The resulting signal is fed to the output mixer to be used as delayed audio.

The following sub-system descriptions describe operation in greater detail. Refer to Figure 4.1, Model 93 Block Diagram, as needed.

4.1 AUDIO SECTION

The audio section of Model 93 is located on the right half of the Motherboard. It includes all analog signal processing and analog-to-digital/digital-to-analog conversions. Gain ranging and ADC/DAC conversions take place on the Analog Daughter Board. Digital

signals are interfaced to the Analog Daughter Board, but no actual digital operations take place there.

Major systems in this section are:

1. Inputs and mixers
2. Filters
3. Gain Rangers
4. Analog-to-Digital and Digital-to-Analog Converters
5. Output Stage

4.1.1 INPUT AND MIXERS

Refer to Motherboard Schematic, Part 2, (Fig. 6.2.2) and Front Panel Schematic (Fig. 6.2.8).

PRIME TIME has two identical electronically balanced input stages. Input is via XLR-3 type connectors. Tip, ring, sleeve 1/4" phone jacks are available as an option for the two inputs and the Master output.

Use of close tolerance resistor arrays (RP1,2) in the input stages ensures accurate gain and high common mode rejection. Input gain is programmed by resistors R3 and R4 and is set by switches S1 and S2.

Resistors R166, 167, 168, 169 set the input impedance at 40K ohm balanced, 20K ohm single-ended. Capacitors C5, 6, 9, 10 serve to help keep unwanted high freqency signals out of the input while at the same time keeping any digital clock noise generated inside the machine from radiating via the input cables.

The input mixer (1/2 U16) is a variable gain, inverting stage. The Master pot is the variable gain control. The gain of the input mixer is adjustable from +13dB to -18dB for input signals and from +.6dB to -30dB for feedback signals. The four function pots (IN, AUX, Delay A and B) are passive attenuators. Analog switch U19 opens the feedback paths in Bypass mode. Analog switches are located at the summing nodes of the mixers to minimize voltage differential across the switch. Nominal level at the output of the input mixer is +13dBm (+5V peak) when the delay line is at limit. The recirculated delays are routed through variable single pole rolloff filters. Frequency cutoff can be varied from 15kHz to 800Hz to contour the feedback signals. The output of the input mixer is also routed through U10 to the Input Mixer Out jack on the rear panel.

The output mixer (1/2 U20) is a fixed gain inverting stage. The four function pots and the master pot are all passive attenuators. Gain is +6dB for delayed signals and +20dB for input signals. Overload of the output mixer is indicated by the overload circuit (U11). The overload indicator is a halfwave rectifier/averager followed by a comparator with .5V of hysteresis. The Overload LED comes on when the output mixer signal is approximately 9V peak and

goes off when the signal is approximately 8.5V peak. To achieve phase inversion the IN input and the two delays in the output mixer can be routed through unity gain inverters U15 and 1/2 U20. Analog switch U19 routes the input mix to the output in Delay Bypass. The unused signals in the analog switch are shorted to ground to minimize feed-through. The External Bypass input is zener protected against over-voltage.

4.1.2 FILTERS

PRIME TIME employs precision 5-pole elliptical low pass filters in the input and output signal paths. Filters are necessary on the input to eliminate high frequency components which could cause aliasing in the sampling process. Output filters eliminate sampling frequency components in the audio output.

The filters are programmed by the Delay Multiply switch for four different cutoff frequencies (12kHz at 1x, 6kHz at 2x, 3kHz at 4x, and 1.5kHz at 8x). Switching is done by adding capacitors in parallel (e.g. C78,79 and 80 are successively paralleled with C77 in the first stage of the input filter). Reduced bandwidth is necessary to eliminate aliasing components as the Delay Multiply programs lower sampling rates.

The elliptical filters are based on frequency dependent negative resistance (FDNR) elements; U18 and associated components comprises one such element. The FDNR sections have the characteristic that their impedence is inversely proportional to the square of the frequency. The FDNR elements enable the construction of elliptical filters without the use of inductors. The FDNR elements are fine tuned for optimum performance of the filters. See section 2.1 for calibration details.

The output of the input low pass filter is followed by a high impedance buffer (1/2 U13). An active pre-emphasis stage (1/2 U16) provides a shelving high frequency boost, up 3dB at 2.2kHz, and shelving to about +11dB at 10kHz. This is followed by an aperture correction stage (1/2 U13) which provides a slight boost at 12kHz to compensate for high frequency loss inherent in the sampling process. The bandwidth of the aperture correction filter is programmed by the Delay Muliply switch.

4.1.3 FLOATING POINT CONVERSION

The signal is next routed to the Analog Daughter Board, where gain ranging takes place in the programmable gain amplifier (PGA). Before describing the PGA a brief discussion of the Floating Point Conversion process will be helpful.

NOTE: Reference numbers for Rev. 1 Analog Daughter Boards are different from those for Rev. 3 boards. Reference numbers in parentheses refer to Rev. 3 PC boards.

Lexicon's technique of encoding analog data into a digital format allows dynamic range in excess of 90dB to be represented by the use of a 12 bit word. Had straight binary coding been used, 15 bits would be required to encode an equivalent dynamic range. The general rule of thumb for a straight binary encoding of analog data is about 6dB of dynamic range per bit of encoded data. The above figure of about 6dB/bit is improved through the use of gain ranging.

Lexicon's technique is to use ten bit straight binary encoded data and append a 2 bit exponent which expresses one of 4 possible gain settings of a programmable gain stage incorporated just ahead of the analog-to-digital converter. The gain ranges selected for the Model 93 are spaced 10dB apart, i.e., 0, 10,20 and 30dB of gain programmed by the 2 bit exponent.

After each analog-to-digital conversion cycle, gain selection logic checks the resultant 10 bit data word to see if it ranges between 1/4 and 7/8th's of full scale. If the converted word exceeds 7/8ths of the ADC's dynamic range the programmable gain stage will drop its gain by 10dB prior to the next data conversion. If the converted word is less than 1/4 of full scale, a 25ms time-out is initiated. If at any time during the time-out a converted word exceeds 1/4 full scale, the time-out is re-started. Upon completion of the 25ms time-out the input gain will be increased by 10dB. The adaptive action of the gain selection logic maintains the analog data presented to the ADC in a range which preserves a high signal to noise ratio despite wide fluctuation of input signal amplitude.

The PGA is implemented with a fast op-amp U6 (U1) and a CMOS switch U9 (U7) selecting the feedback network. The feedback network consists of four precision resistors sized to provide gain steps of exactly 10dB. A 4051 CMOS analog multiplexer/demultiplexer is used as a single pole, 4 position selector switch to select the desired gain setting. Capacitor C15 (C7) provides constant DC gain in all four gain ranges to eliminate the possibility of an offset pedestal degrading performance during rapid gain changes. The PGA stage is also AC coupled to the preceeding stage to prevent accumulated DC offsets from affecting the PGA stage. Diodes CR10 (CR8) and CR11 (CR9) protect the CMOS switch against voltage inputs exceeding its VDD (Pin 16) and VSS (Pin 8) bias voltages.

The programming of the PGA stage is done with logic signals HLNG0/ and HLNG1/. These logic signals, as well as all other logic signals in the Model 93 prefixed "HL", denote High Level logic swings of 0 to +7 volts as opposed to the 0 to +4 volt LSTTL signals used throughout the rest of the Model 93. The gain steps of the PGA stage are defined in the following table:

U9(U7) PIN 1Ø	U9(U7) PIN 11	GAIN dB	GAIN (Vo/Vin)
HLNG1/	HLNGØ/		
Ø	Ø	Ø	1.Ø
Ø	1	1Ø	3.16
1	Ø	2Ø	1Ø.Ø
1	1	3Ø	31.6

4.1.4 ANALOG-TO-DIGITAL / DIGITAL-TO-ANALOG CONVERTER

Refer to Analog Daughter Board Schematic (Fig. 6.2.4)

The Model 93 uses an integrated circuit Digital-to-Analog Converter (DAC) in a time-shared mode, allowing a single DAC to serve as both an input converter and an output converter for each of the two outputs.

The input converter or Analog-to-Digital Converter (ADC) converts analog signals in the range of -5 to +5 volts to a 1Ø bit binary representation. Figure 4.2 illustrates this process. Limiting occurs when the analog signal presented to the ADC exceeds +5 volts. When this happens, the converted binary representation will be all ones or all zeros and no 1Ø bit binary representation is available to express a greater magnitude. This is why amplitudes greater than limit flat-top abruptly. The actual process of conversion uses a technique of sucessive approximation through a process of 1Ø tests. By setting and resetting register bits based upon the test outcomes, the input analog signal is quantized to an accuracy of one part in 1Ø24.

Figure 4.2 illustrates a good analogy to explain the method of successive approximation Analog-to-Digital (A/D) conversion, that of a balanced scale and a set of binarily related weights.

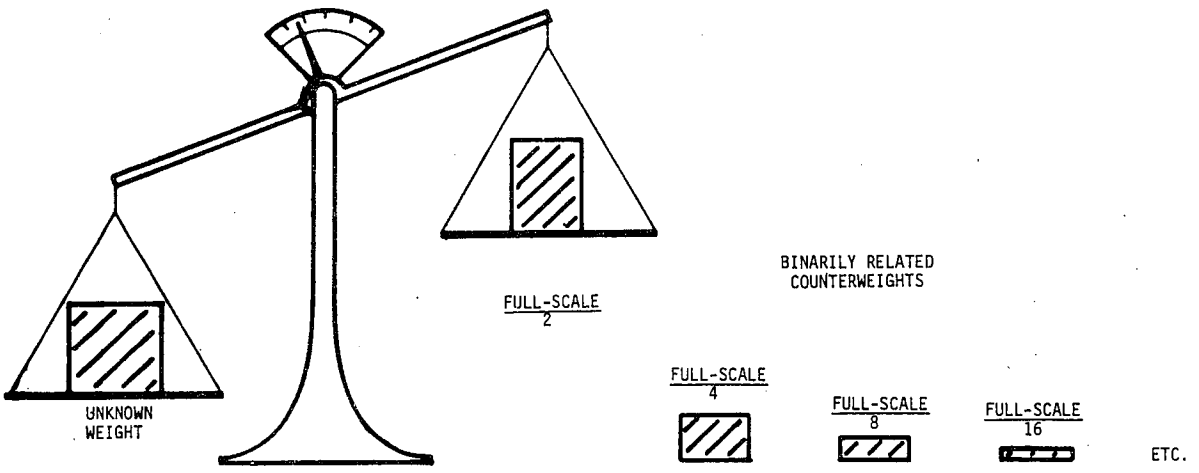


FIG. 4.2 SUCCESSIVE APPROXIMATION OF UNKNOWN WEIGHT

To measure the unknown weight, place the unknown in one balance pan and the heaviest weight, full-scale/2 in the other pan. If the full-scale/2 weight is too heavy, it will have to be removed before trying the next heaviest weight (full-scale/4). If the full-scale/2 weight is not too heavy it will be left on the balance and the full-scale/4 weight added to it. If this process is repeated for each weight, after n trials (Where n equals the number of binarily related weights) we will have a determination of the unknown weight accurate to one part in 2 to the nth power or 1/1Ø24 for 1Ø weights.

The Model 93 simulates this process electrically by sequentially comparing binarily related current outputs of the DAC U7(U5) to the unknown current set up by the analog input flowing through R28 and R37(R9 and R11), the comparator input resistors. The comparator U1Ø(U4) has the ability to distinguish which signal is greater and represents the outcome with a 2 state output i.e., ground or +5 volts out. In the Model 93 an analog signal more negative than the DAC output will result in a logic zero or ground level out of the comparator.

Upon receipt of a start conversion command by the Successive Approximation Upon receipt of a start conversion command by the Successive Approximation Register (SAR), the SAR output lines are set to Ø1111111111 - this causes the DAC to output a full-scale/2 output of zero volts where the full scale is -5V to +5V. If the comparator output goes to high, this means that the sampled audio signal is above zero volts or above the zero crossing axis. Under these conditions, the SAR would then reset the Most Significant Bit (MSB) to one and set the next bit to Ø, i.e. 1Ø111111111. This will cause the DAC to output a +2.5 volts or full-scale x3/4 output and the comparator will determine if the analog signal is between Ø and 2.5 volts or between 2.5 Volts and 5 Volts. This process continues for each of the 1Ø bits. At the end of 1Ø test cycles the SAR output lines will have stepped the DAC output to within 1ØmV of the true analog amplitude. The SAR outputs a 1Ø bit word which is combined with an additional 2 bits of gain information and stored in memory. Figure 4.3 is a simplified diagram of the successive approximation process used in the Model 93.

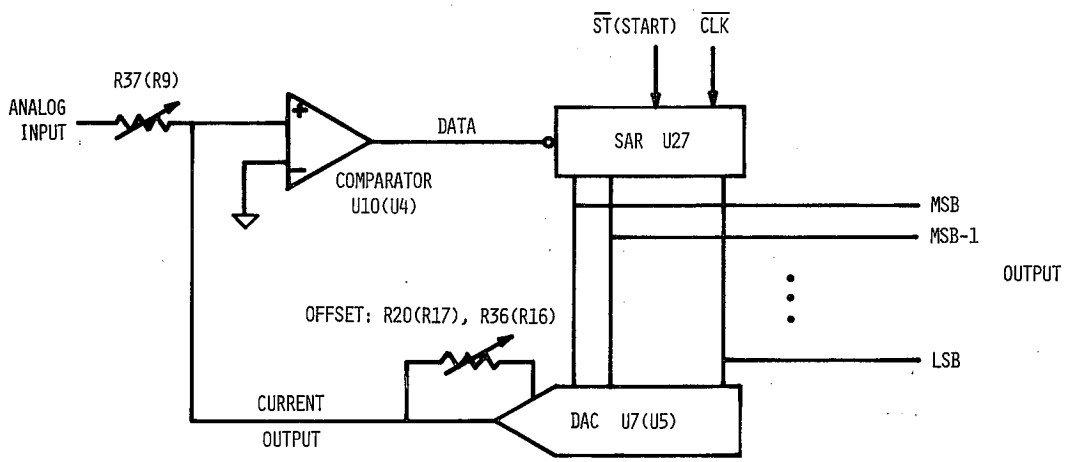


FIG. 4.3

Figure 4.4 shows a flow chart of the successive approximation process. Each of the decision steps is diagrammed as a diamond with two possible outcomes. The tree structure that evolves represents all possible paths that could evolve with a range of analog inputs.

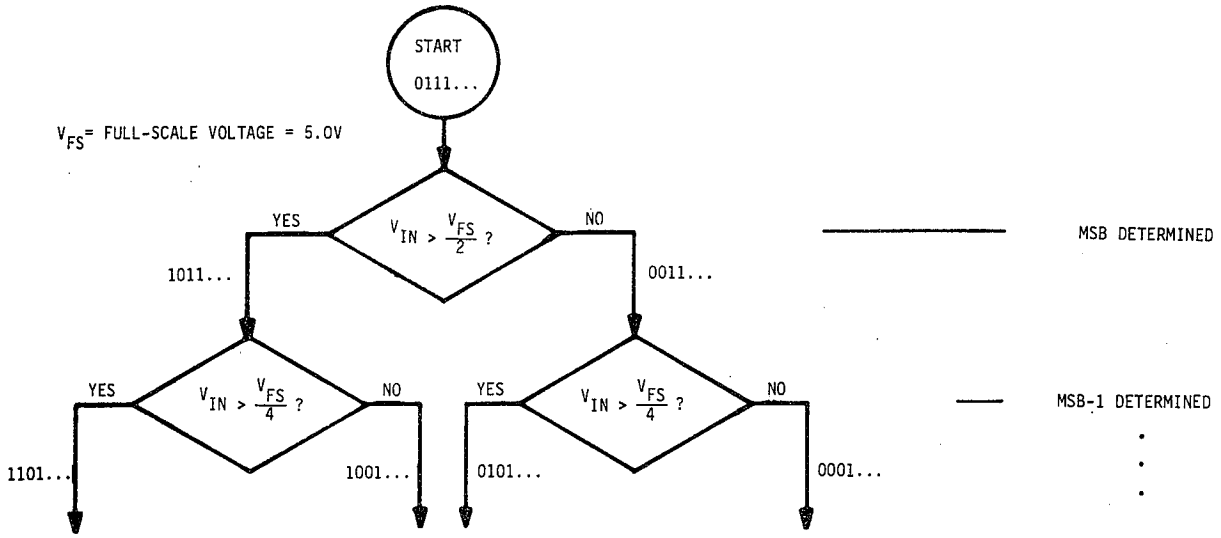


FIG. 4.4 SUCCESSIVE APPROXIMATION DECISION PROCESS

In the trouble-shooting section of this manual, a series of waveforms are presented which show the action of each bit line as it is tested and then either left the same or reset depending on the response of the comparator. Time sharing is achieved by passing output data through the DAC in addition to data for the input successive approximation process. Data retrieved from memory is sent to the DAC and to the appropriate output Programmable Gain Amplifier "PGA". The DAC output current re-routed to OP-AMP U5(U6) by switch U8(U3) is converted to a voltage, and then stored on a holding capacitor C3(C25) or C2(C23) until updated again during the next output cycle.

4.1.5 ADC/DAC INPLEMENTATION

Refer to Analog Daughter Board Schematic (Fig. 6.2.4).

Gain Conditioned and filtered analog information is sampled at 32.000kHz rate by U11(U2), a monolithic sample-and-hold amplifier. The purpose of the sample-and-hold is to provide accurate periodic sampling of analog data and to stabilize or freeze that data so that it does not change during the actual analog-to-digital conversion process. The sample-and-hold output is summed through R28 and R37(R9 and R11) with the DAC output current. This DAC output current is commutated from the DAC to the comparator input through switch U8 (U3) during the input conversion cycle. During input conversion, sample-and-hold control N will be at logic zero and HLN/ will be

high. The input conversion cycle is completed after the least significant (LSB) or tenth bit has been converted. At this time the 1Ø data bits are held in the SAR U27 (Motherboard) and the two gain bits, GØ and G1, are held in registers U53 (Motherboard).

When the output cycle commences, Signal N goes high returning the sample-and-hold circuit to the track or acquire mode. Signal HLN/ goes low, thus rerouting the DAC output current to the input of a fast settling op-amp U5(U6) which converts the DAC output current to a voltage with a 5 volt/ma sensitivity. U5(U6), an LM3Ø1, is not in itself a super-fast op-amp but the compensation arrangement used (feed-forward) provides good response and accurate settling. The voltage output of U5(U6) is re-connected back through additional sections of switch U8(U3) so that it may be first switched into sample-and-hold capacitor C3(C25) during output-1 cycle and then switched to C2(C23) during output-2 cycle. This switching action provides the combined action of demultiplexing and output sample-and-hold. Read-out of the capacitors is performed by a CA324Ø high input impedance dual op-amp connected as unity gain voltage followers. The output voltage samples are next gain conditioned by PGA's which provide Ø, -1Ø, -2Ø, or -3ØdB gain.

The Model 93 is designed to use either a Motorola MC341Ø or an Analog Devices AD561 monolithic 1Ø bit current output DAC. Since the MC341Ø and AD561 are electrically different, a dual set of device pads are provided on the circuit board. These chip positions are offset to allow use of both devices. The MC341Ø has no internal reference and, to provide a full scale current of 2ma, R31(R15) in series with R3Ø(R14) sets up approximiately 1ma of reference current flowing into Pin 16 of the device. R36(R16) is adjustable to trim the offset for symmetrical clipping.

The AD561 has a precision internal reference which when connected to the DAC output through a 1Ø ohm resistor exactly offsets the DAC's output to within one least significant bit (LSB) of the center of its output range. On Model 93's fitted with AD561 DAC's in position U7(U5) of the Analog Daughter Board, there is no offset adjustment ever required and R36(R16) is not installed. Since the 561 does have a full scale output range variation of 1.5 to 2.4ma (a typical value of 2.Øma), resistors R37(R9) and R38(R18) are trimmed to match the AD561's actual full output. In the event that a new AD561 is installed it will be necessary to recalibrate the converter. See section 2.2 for calibration procedure. The value of these resistors influence only the maximum input for limit and the maximum output at limit levels. The Analog Board schematic indicates both DAC interconnections.

The following truth table lists the gain for each combination of control signals.

HLGZ1/	HLGZØ/	GAIN dBm	GAIN Vo / Vin
Ø	Ø	Ø	1
Ø	1	-1Ø	Ø.316
1	Ø	-2Ø	Ø.1Ø
1	1	-3Ø	.ØØ316

4.1.6 OUTPUT SIGNAL CONDITIONING

On the Rev 3 Analog Daughter Board the gain corrected output is again sampled-and-held after the PGA has had ample time to settle. This eliminates gain switch transients which were present under some conditions in the earlier version. Analog switch U12 routes the signal to sample and hold capacitors C35 and C37. U13 provides a high impedance buffer for the sample and holds.

The output signals are next routed back down to the motherboard, where they pass through the de-emphasis stage. This serves to reduce high frequency output noise while exactly correcting the audio signal for the pre-emphasis in the input stage. Next the signal is low-pass filtered by the 5-pole elliptical filter. The actual response curves for all of the various filtering and correction networks are contained in the service data section of this manual.

The two delayed outputs are then routed through switch selectable inverters U15 to the output mixer. They are also routed through U5 to the Delay A and B output jacks on the rear panel. Pots R13 and R14 vary the output level from +8dBm to +18dBm when the delay line is at limit.

The Output Mixer output is routed through a unity gain power amplifier stage (U14). This is a class AB amplifier and is used to drive the primary of the output transformer. The secondary of the output transformer is routed to the Master Output on the rear panel. Ferrite beads FB1 and FB2 and capacitors C7 and C8 serve to reduce any high frequency digital noise on the output lines.

4.1.7 +/-7 VOLT SUPPLIES

The +/-7 volt CMOS bias and clamp voltages are derived from zener diodes CR8 and CR9 on the Motherboard and CR3 (CR14) and CR9 (CR15) on the Analog Daughter Board. A number of diodes are used as clamps on various signal lines. This is a precaution against excessive analog voltage swings causing damage to the CMOS analog switches. The +7 volt supply also serves the function of pull-up voltage to establish Ø to +7 volt logic swings for the "HL" control inputs of the CMOS switches.

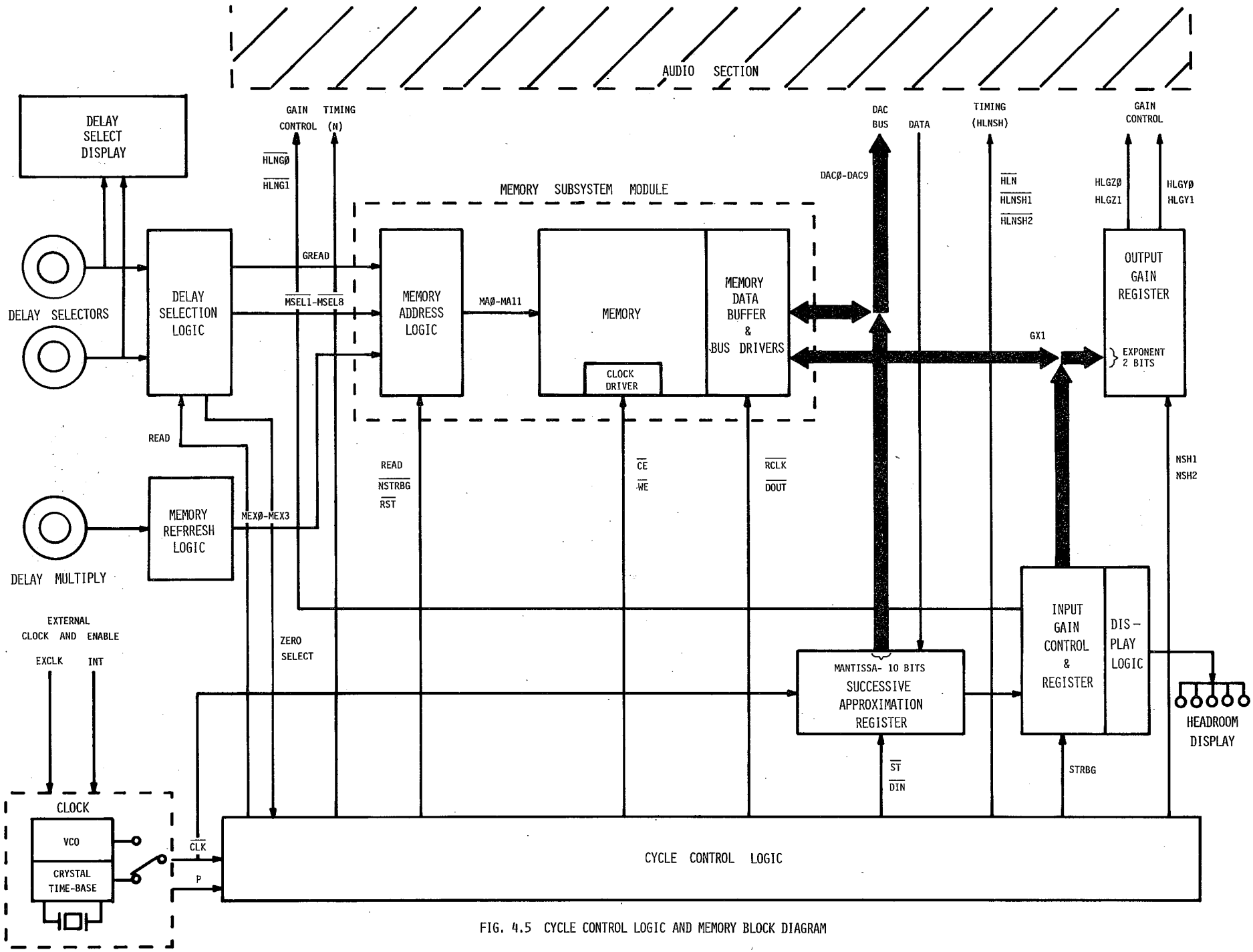


FIG. 4.5 CYCLE CONTROL LOGIC AND MEMORY BLOCK DIAGRAM

4.2 DIGITAL CONTROL LOGIC

The control logic section is located on the left half of the Motherboard, underneath the memory module. Refer to Figure 4.5, Systems Block Diagram, and Figures 6.2.1, 6.2.3, 6.2.6 and 6.2.7, Motherboard logic schematic, Motherboard VCO schematic, Memory schematic, and Memory Extension schematic as an aid to understanding the following description. The diagrams are partitioned into functional blocks to aid understanding. The following description will proceed on a block by block basis.

4.2.1 CLOCK GENERATOR / VCO

The PRIME TIME clock generator is built around the 74S124 dual voltage controlled oscillator. Refer to Figure 6.5, Motherboard schematic part 3. One half of the 74S124 functions as a stable crystal controlled oscillator in the "cal" mode. Nominal clock frequency is 4.992 MHz.

Turning the Delay Adjust control clockwise closes switch S2 on the front panel board. This illuminates the "uncal" indicator and disables the crystal oscillator half of the 74S124. The other half of the 74S124 functions as a high frequency Voltage Controlled Oscillator. Control voltage developed at the output of U64 (pin 1) varies the VCO frequency between 4.992 MHz and 9.984 MHz.

A dc control voltage is developed by U66. A 1ØV reference is set up at pin 1 U66. The control voltage is developed at the wiper of the Delay Adjust pot (R4 on front panel board). The other half of U66 acts as a high impedance buffer to avoid loading the wiper of R4. For external delay adjust, the wiper of the Delay Adjust pot is disabled and a Ø-1ØV control signal is injected in its place. Alternatively, a 5ØK ohm pot can be connected to the external jack. Q3 acts as a constant current source of about .2ma. In conjuction with the 5ØK ohm variable resistor, this produces the Ø-1ØV control signal.

A low frequency triangle wave is generated by U63, 64, 65, and 67. U65 acts as an integrator. FREQ control R161 programs the current into the integrator, which together with R152 controls the charging rate of capacitor C197. 1/2 U64 is a comparator; when the voltage at pin 6 U65 exceeds 1ØV the output of U64 goes negative. This causes pin 3 of CMOS inverter U63 to go to +1ØV, which causes the integrator output to decrease. Pin 4 U63 goes to ground and comparator U64 triggers again when the integrator output goes below ground. Use of CMOS gates in the hysteresis section ensures accurate Ø-1ØV swings. Frequency is variable from .1Hz to 2ØHz.

The dc control voltage and the Ø-1ØV triangle wave are summed through Depth control R16Ø. 1/2 U64 scales the voltages to control the 74S124. R159 is the high frequency trim and C188 is the low frequency trim. See section 2.3 for VCO calibration procedure.

used and the internal / external clock selection signal INT must be grounded.

The master clock (MC) is available on pin 8 U44, and is the crystal clock in "cal" mode or the VCO clock in "uncal" mode. This is divided down by U30 to give a bit clock CLK/ frequency of 832.00KHz, or a bit time of 1.2019us. Signal P, which is present for the second half of each clock period, is used to generate the chip enable signal CE for the dynamic RAM.

4.2.2 CYCLE CONTROL

Refer to Motherboard Schematic, Part 1, (Fig. 6.2.1).

U25 and half of U29 form the basic cycle counter which provides 26 bit-clock intervals in each cycle. An input conversion and two output conversions are performed during each cycle and the memory is written into once to store a new sample and read twice for output purposes. The sampling frequency is 32.000kHz with an interval of 31.25us. Since the memory holds 4096 samples, a maximum delay time of 128 milliseconds may be obtained (with extension memory, the memory holds 8192 samples for 256 milliseconds maximum delay in 1x mode). The cycle counter drives a ROM, U24 which provides the control signals for the operation of the entire system. These signals are shown in Figure 6.3.1 and are described below:

a. WE/: This signal enables memory write operation, which writes the last converted digital sample value, both the exponent and fraction bits, into memory.

b. ST/: This initializes the Successive Approximation Register (SAR) U27 to 0111111111 for two bit-times to allow the DAC extra settling time for the MSB.

c. STRBG: This signal (strobe gain) deglitched by 1/2 U29 to give NSTRBG, is used to strobe the new gain into NG0, NG1 (1/2 U53). The gain associated with the present conversion is transferred into G0, G1 (1/2 U53) to be written into the memory at the next WE/ time. NSTRBG occurs after SAR bits 9, 8, 7 and 6 have been settled to their final values. The new gain setting is immediately passed on to the input gain amplifier which is isolated from what the input comparator sees by the input sample-and-hold circuit.

d. PN: This signal after a delay of one bit-time gives signal N which forms the high order bit of the next ROM address. N is also used as the input sample-and-hold control signal.

e. READ/: This signal occurs twice per cycle. The first time is immediately after the LSB of the SAR has settled to its final value. The two occurrences of READ/,in conjunction with N, are used for delay selection. WE/ and READ/ are logically "ORed" to give the memory clock CE.

f&g. SH1/ & SH2/: These two signals are deglitched by U35 to give

output signals for sampling the DAC output and for strobing output gain into the two output gain registers U31 and U36.

h. CLR/: This signal is used for shortening the ROM address-counter counts to 14 during N=Ø and 12 during N=1.

4.2.3 A-D CONTROL

The SAR, U27, is initialized by ST/, clocked by CLK/ and steered by the comparator output DATA. The outputs of the SAR are connected through tri-state gates U22 and U26 to the data bus which drives the DAC. The seven high order bits of the SAR are connected directly to the Input Gain Control and Display Logic.

4.2.4 INPUT GAIN CONTROL AND DISPLAY

During an input conversion, the input sample-and-hold circuit is in the "hold" state, effectively isolating the input gain-switching amplifier from the comparator. The input gain-switching amplifier is controlled by gain register signals NGØ, NG1 (1/2 U53). When NSTRBG makes the Ø-1 transition, a sufficient number of bits of the input conversion have settled to determine whether the input gain-switching amplifier should take on a new gain setting. If the SAR shows 1111XXXXXX or ØØØØXXXXXX (X denotes "don't care"), the ADC is using at least seven eighths of its dynamic range and the input gain-switching amplifier should switch to a lower gain setting so as not to exceed the ADC dynamic range. Signal D denotes gain down. When the SAR shows 1ØØXXXXXXX or Ø11XXXXXXX we know that the ADC is using no more than one-fourth its dynamic range. To improve the system signal-to-noise ratio, we must increase the input amplifier gain so more of the DAC dynamic range will be utilized. This leads to the generation of the U signal, which denotes gain up. The one-shot 1/2 U38 is used to delay the gain up action until the DAC dynamic range has been less than one-quarter utilized for at least 25 milliseconds. This prevents the unnecessary and excessive gain switchings due to the normal alternating current nature of the input signal. U46, 47, 57 and 61 limit the Gain changing to ØØ-Ø1-1Ø-11 only. U46 is socket mounted to permit a test fixture to be plugged in for external control of the gain setting. Since the current gain setting associated with the conversion is needed for writing the memory, the old gain setting is transferred into GØ, G1 at the same time the new values of NGØ, NG1 are stored. At the end of the input conversion, when signal N makes the Ø-1 transition, if GØ, G1 is 11 (for lowest gain or maximum input signal level) and the SAR is 1111111XXX or ØØØØØØØXXX, a 4ØØms one shot, 1/2 U38, is fired to indicate that DAC limiting is at best only Ø.12dB away. GØ and G1 are connected to the data bus via U26 in the A-D Control Section and U51, 52, 56, 58 decode the gain setting and limit conditions to provide the five signals driving the LED level and limit indicators.

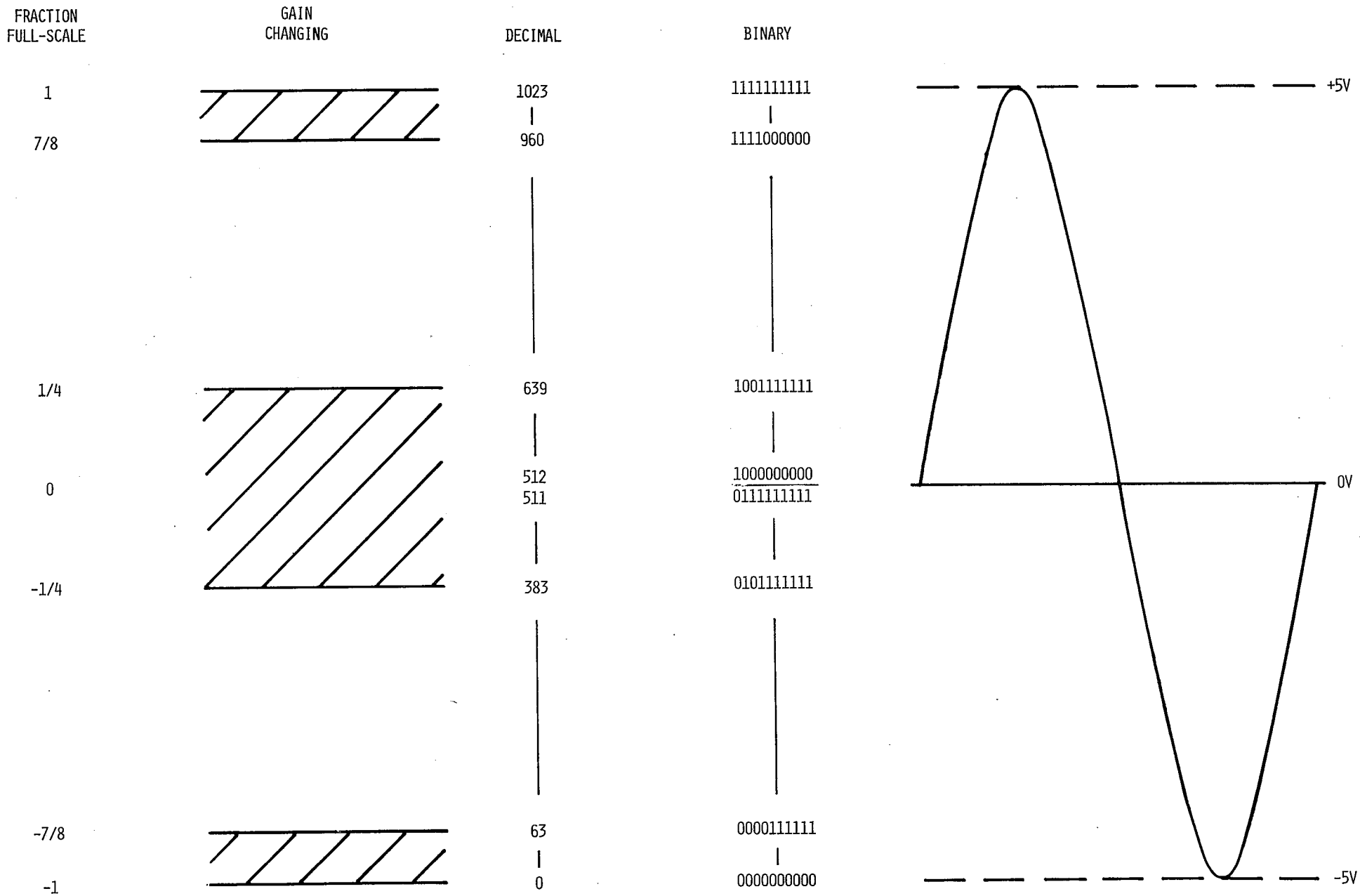


FIG. 4.6 SIGNAL ENCODING DIAGRAM

4.2.5 DELAY SELECTION LOGIC

Sixty position switches for Delay Select A and B (SW5 and SW4) are programmed with a nine bit memory address offset for each delay selection, which is processed and added to the current memory address. In addition, each switch is programmed to directly drive the LED delay time displays.

Multiplexers U59 and U60 route the correct offset to the Memory Board at the appropriate time. Signal N is used to select channel A or B.

In machines without the memory extension option, signal GREAD is jumpered to the strobe terminal of the multiplexers (pin 15 U59 and U60). In case of selection of a delay greater than 128ms, signal GREAD is forced high, which causes the multiplexer to output all 0's. Offset of all 0's corresponds to maximum delay, in this case 128ms in 1x mode (note that for any given memory address, the two Read operations are performed before the Write operation).

Zero delay is accomplished by pulling DIN/ low, enabling the SAR and Input Gain Register tri-state buffers (U22 and U26) and by forcing DOUT/ high, disabling the memory output tri-state buffers (U2 and U4), thus bypassing the memory, and using the SAR and G0, G1 outputs directly.

4.2.6 OUTPUT GAIN REGISTERS

U31 and U36 store the gain part of the data bus at times NSH1 and NSH2. U31 and U36 store the gain part of the data bus at times NSH1 and NSH2. Since NSH1 and NSH2 is delayed from SH1 and SH2 by Clock P, the DAC output has had one half bit-time for settling before the output sample-and-hold and gain-switching amplifier receive their commands.

4.2.7 MEMORY ADDRESS LOGIC

Refer to Memory Schematic, Fig. 6.2.6, and Memory Extention Schematic, Fig 6.2.7.

The memory is organized as a 4096 x 12 bit storage expandable to 8192 x 12 bits. The 8 high order address bits are used to select delay when only the basic memory is installed. The 8 high order bits allow division of the 128ms memory into 256 1/2ms sectors.

The memory addresses can be represented as a closed circle on which the end address is adjacent to the beginning address.

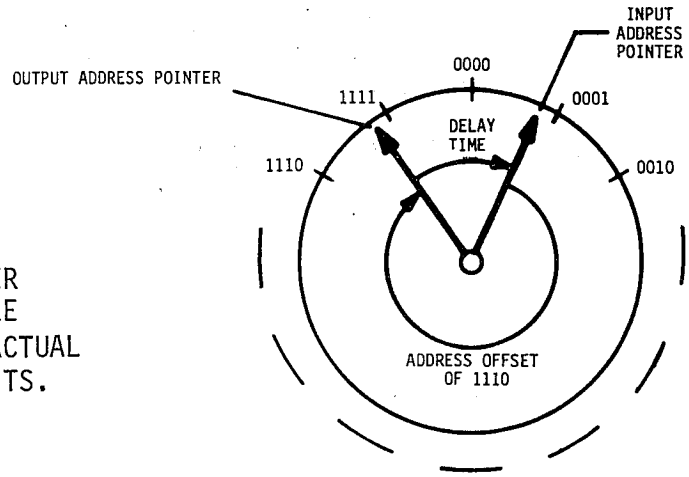


FIG. 4.7 MEMORY MAP SHOWING FOUR HIGH ORDER ADDRESS BITS AND SAMPLE DELAY CONFIGURATION. ACTUAL ADDRESS OFFSET IS 8 BITS.

During each machine cycle a read time slot is provided for each channel prior to the write operation.

Since the location about to be written contains the oldest data we obtain a 128ms delay by simply reading at the input address during each machine cycle.

Shorter delays are obtained by adding an offset to the current input address. If we offset or add all ones to the 8 higher order address bits the output pointer will follow the input pointer by Ø.5ms thus providing Ø.5ms of audio delay. The actual address bits are programmed by the two Delay Selector switches. U59 and U6Ø are data selectors which select the appropriate switch bits for input to adders U23 and U24 on the memory card.

During any given read cycle the Delay A Select Switch (SW5) and then the Delay B Select Switch (SW4) is selected through U59 and U6Ø by signal "N". During the third portion of the cycle the data selectors are disabled by GREAD//READ/ going high causing all logic zeros to be read out of the selectors. The all zero condition results in no offset added to the address counters. A memory write is then executed at the current input address.

Prior to the next read cycle signal NSTRBG increments the address counter. If a greater than 128ms delay is selected but no memory extension is added the closure of SEL A9 or SEL B9 switch bits prevent the memory read pulse U4Ø pin 4 (motherboard) from appearing at U45 pin 8.

It should be noted here that signal GREAD/ is jumpered as the

memory read pulse. This memory read pulse is then fed to the data selectors U59 and U60. The absence of the memory GREAD//READ/ pulse keeps the data selectors disabled thus forcing a read with no offset resulting in maximum delay (128ms).

4.2.7.1 MEMORY EXTENSION

Memory extension is accomplished by adding an additional bit to the address counter, an additional adder stage and 12 additional memory chips. Signal READ/ is jumpered through to the data selectors.

The chip select input to the memories is used as a high order address bit. Chip select CS2/ and CS1 allow connections of the primary and expansion memories in parallel, thus doubling the address range.

Since the RAM's are Tri-State devices only the selected memory will place data on the output bus or write data from the data bus.

Address range is expanded to 8192 and delay selection is provided by the 9 high order address bits, thus providing 512 1/2ms memory sectors.

In all modes of operation memory output data is latched into the output buffer by RCLK/. Write is enabled by signal WEG/ going to ground. High level memory clock CEL1 and CEL2 is present during both read and write cycles.

4.2.7.2 Memory Operation in Delay Multiply Modes

In Delay Multiply modes it is required to provide dummy cycles to insure memory refresh. Counter U49 (Motherboard) is preset as follows.

DELAY MULTIPLY	COUNTER PRESET	FUNCTION
1x	1111	Divide by 1
2x	111Ø	Divide by 2
4x	11ØØ	Divide by 4
8x	1ØØØ	Divide by 8

The carry output of counter U49 is control signal DMCY/. This is gated with memory address clock NSTRG (U19 Memory Board) to pass 1 of every 2 clock pulses in 2x, 1 of 4 in 4x, and 1 of 8 in 8x. This effectively reduces the memory clock rate in Delay Multiply modes. In addition DMCY/ is gated with the chip select signals (U19 Memory Board) to inhibit memory operation at the appropriate time. To ensure accepting memory data only at valid times in the Delay Multiply mode,

DMCY/ is also used on the preset inputs of U35, (Motherboard) to inhibit signals NSH1 and NSH2, the output sample and hold signals.

Use of slower clock rates in Delay Multiply modes requires special consideration for the memory refresh requirements of the dynamic RAMS. Refresh is accomplished by cycling through row addresses while providing memory clock (CEL). Counter U49, (Motherboard) provides appropriate count sequences which are added to the current memory address by adder U25 (Memory Board).

4.2.8 MEMORY AND MEMORY OUTPUT DATA BUFFER

U6 through U17 on the main Memory Board, and U1 through U12 on the Memory Extension Board are 4K bit dynamic RAM's for storing the input signal sample values.

U5 provides the chip enable clock whenever memory write or read operations take place. Writing is done at the beginning of each cycle, storing into memory the sample which was converted during the last cycle. Memory outputs are strobed into the output data buffer register U1 and U3, which are connected to the data bus through tri-state inverters U2 and U4, which are controlled by signal DOUT/.

4.2.9 REPEAT HOLD LOGIC

Refer to Motherboard Schematic, Part 1 (Fig. 6.2.1)

One shot U55 serves to debounce the repeat hold push-button. The resulting single pulse at pin 8 U48 clocks flip-flop U54. In normal operation, signal WE/ is gated with a high level from pin 9 U54. On power-up R133 and C184 hold the preset input of U54 low long enough to ensure that the machine turns on in normal operation. Pressing Repeat Hold causes pin 5 U54 to go low. Pin 9 U54 then goes low synchronized with RCLK/, which inhibits the WEG/ signal. This inhibits memory write, and the data in memory is continuously repeated without writing any more data into memory. Pressing Repeat Hold again restores normal operation.

4.3 POWER SUPPLY

The power transformer is wound with a dual primary and wired with a voltage change-over switch to allow selection of 115 or 230 Volt operation. Both sides of the mains voltage are switched for safety considerations. A single SLO-BLO type fuse is installed in the primary circuit of the power transformer. Consistent with good practice, a 3 wire IEC connector is provided to facilitate installation of a variety of power cords to match local mains recepticles. The third wire or ground is connected directly to the chassis of the instrument. The power supply develops +5 Volts at one amp and +/-15 Volts at 200ma each. The 5 Volt logic supply is derived from a seperate secondary. This supply is protected by a seperate 2 1/2 amp fuse. Additional protection is provided against

short circuiting, over voltage and excessive temperature rise.

The over-voltage protection is of the "crowbar" type. If an over-voltage condition is sensed a silicon control rectifier is triggered into conduction and shorts the 5 Volt supply to ground. Under these circumstances the 5 Volt monolithic regulator will limit the short circuit current to less than 2 amps and the protection fuse will not be blown. If the over-voltage was a result of regulator failure, it is conceivable that current limiting will not take place and under this set of circumstances the fuse will protect by blowing. Re-setting of the crowbar occurs when power is shut off momentarily.

The +/-15 Volt supplies are derived from a single secondary. Both positive and negative supplies are regulated by monolithic 3 terminal regulators which provide both short circuit and over temperature protection. All of the 3 terminal regulators are fitted with sockets to facilitate service should it ever be required. If replacement is required, it is desirable to use new thermal compound and mica insulators to insure reliability and low junction temperatures. A continuity check to insure against a chassis short is a good practice when installing these devices. Maximum screw torque applied should be 8 inch-pounds.

4.3.1 VOLTAGE LIMITS

A convenient location to probe the power supply voltages is at J4 (memory connector). The following table indicates appropriate voltage limits.

J4 PIN NO.	VOLTAGE	LIMITS min	LIMITS max
6	-15V	-14.25	-15.75
7	ANG GND (+/-15V)	--	
8	+15V	14.25	15.75
9	DIG GND (+5V)	--	
10	+5V	4.75	5.25

5.Ø MAINTENANCE AND TROUBLE-SHOOTING

If field service is required, it is always good practice to verify proper operation of all power supplies. In addition to the +5, +15 and -15 volt supplies, the +12V regulated supply on the Memory Board and the +7 and -7 Volt Analog Board and Motherboard supplies should be verified. Power supply voltage limits are as follows:

+/-15	-	14.25 to 15.75V
+5	-	4.75 to 5.25V
+12	-	11.4 to 12.6V
+/-7	-	6.12 to 7.48V

The unregulated 5V supply (approx. 8.5V) is used on the front panel to drive the displays. Failure of the displays to illuminate on power-up indicates malfunction of this supply.

Note: +5 Volt gnd. is isolated from all other voltage grounds if both Memory and Analog Daughter Board modules are removed from the Motherboard.

WARNING

All servicing of the Model 93 should be performed by qualified service personnel. There are hazardous voltages located under both the top and bottom covers of the Model 93. To avoid electrical shock remove power cord from unit prior to removing covers. Servicing procedures consistant with good safety practice should be used at all times.

5.Ø.1 MODULE REMOVAL

Should module removal be required proceed as follows:

Modules may be held in place by either nylon standoff retainers or threaded spacers secured with nylon screws. If the module is held in place by the spacers with nylon screws, remove the four screws and carefully lift the module straight up to avoid bending pins on the connectors. Installation of circuit boards requires alignment of all connector pins with their mating receptacles.

If the module is held in place by four nylon standoff retainers proceed as follows. Each retainer has a small locking barb which must

be depressed with needle nose pliers or screwdriver while carefully lifting the circuit board at the nearest corner. Release one corner at a time and then lift the entire module from the Motherboard. Installation of circuit boards requires alignment of all connector pins with their mating receptacles. After positioning board, firmly press each corner until all locking barbs are engaged.

Should a situation arise that requires removal of the Front Panel Board, proceed as follows.

To remove the front panel it is necessary to remove all knobs. To remove the knobs, pry off the colored caps with a thin knife blade (Delay Select, Delay Multiply, Delay Adjust, Depth). Use the proper size nut-driver or screw-driver to loosen the knobs. After the knobs have been removed, pull off all the rubber boots on the pots and toggle switches. Remove the hex nuts on the Delay Mulitply, Delay Adjust and Depth controls, taking care not to scratch the front panel. Remove the four screws securing the front panel to the chassis and carefully pull the front panel away from the machine.

To remove the front panel board, first remove the two angle brackets to which the front panel was secured. Remove the bushing extender on the Delay Multiply switch and the hex nuts on the Delay Select switches. Remove the two screws holding the front panel board in place and carefully pull the assembly away from the machine.

To reinstall the front panel board, make sure that all pins on the right angle Molex connector are properly aligned with the mating recepticle on the front panel board. Push the front panel board into place, taking care that none of the pins is bent. Reverse the above procedure to complete the front panel assembly.

To repair the Delay Multiply switch, see section 5.1

5.Ø.2 UNIT WILL NOT POWER UP

If the unit will not power up check mains cord and service outlet. Next check power fuses F1 and F2. If fuses are good next check individual power supply voltages with the aid of a good general purpose VOM. Refer to Fig. 6.Ø.1 and Fig. 6.6 (pin connection chart) to aid in locating test points.

5.Ø.3 UNIT FUNCTIONS ONLY AT ZERO DELAY SETTING

If it is determined that zero delay setting works but all higher delay settings are malfunctioning, the memory module is suspect. Check for proper installation of the memory card -- the connector pins should be carefully engaged and the nylon locking standoffs should be firmly in place.

5.Ø.4 PROBLEMS WITH ONLY ONE DELAY TAP

This is a good indication that the problem is on the analog daughter board only or in the output signal path after the analog daughter board. Check for proper seating of the analog daughter board.

5.Ø.5 HEADROOM INDICATOR ACTS ERRATICALLY

This problem often indicates defects in the control logic. It should be noted that it is normal for all 5 Headroom LED's to light when the analog daughter module is not installed. Improper analog daughter module installation can also cause erratic headroom indicator operation.

5.Ø.6 COMPONENT LEVEL TROUBLE-SHOOTING

We recognize that for many PRIME TIME owners lack of test equipment or familiarity with Digital techniques will prevent them from being able to efficiently trouble-shoot to the component level. For these individuals Lexicon provides a module exchange program and fast turn-around factory service.

5.1 LOGIC SECTION MAINTENANCE

The Model 93 is designed to allow testing of all logic subsystems with the exception of memory timing and delay selection with only the analog daughter board installed. The memory module may be removed for easy access to the digital logic.

Both Delay Select switches should be placed at the zero delay setting. In this mode the Model 93 will digitize audio and output zero delayed audio.

For most service problems, direct comparison of observed waveforms with the timing charts and photographs will indicate defective subsystems.

IC's U21 and U41 (Motherboard) are open collector 7406 TTL hex-inverters. Since the pull-up resistors for a number of these device outputs are on the analog daughter board it is necessary to have this module installed to verify proper device operation. With the pull-up the logic swing on the output of these devices will be either Ø to +5 Volts or Ø to +/-7 Volts dependent on the pull-up voltage supply used. All signals prefixed with "HL" are Ø to +/-7 Volts signals and are used to control the CMOS analog switches on the Analog Daughter Board.

5.2 MEMORY MAINTENANCE

For suspected memory problems, first verify the existence of +12, +5, and -5 Volts bias on all memory devices. Next check for the chip-enable clock CEL. This signal should be a Ø to +12V signal with fast rise and fall times (<1ØØ ns). U29, U28, U27, U26 comprise a 13-bit straight binary counter which provides the current memory write address. Check for functioning of all counter stages. U24, U23 and U22 form a 9-bit adder which generates an address offset during each read cycle. MA6-11 should follow U27 and U28 outputs except when signal READ/ goes low. U25 is a 4-bit adder which generates memory refresh addresses in 2x, 4x and 8x modes. Latched data from U1 and U3 should be available on the data bus (U2 and U4 outputs) only when DOUT/ is low.

On Memories with Memory Extension Option, if data is available only half the time check the chip select (CS) signals and make sure the Memory Extension Board is properly seated in its sockets.

For suspected memory bit error problems, direct substitution of memory chips with a known good part is sometimes a reasonable procedure for field servicing.

5.2.1 MEMORY OPTION INSTALLATION INSTRUCTIONS

This option increases the maximum delay time of the PRIME TIME Model 93 from 128ms to 256ms in x1 mode. It involves installing an additional Memory board and changing a few jumpers on the Main Memory Board.

PARTS LIST

QTY.	DESCRIPTION	PART NUMBER
1	P.C. Board, Memory Expansion	71Ø-Ø1122
1	Wire, Jumper, .5"	
1	Product Bulletin, MEO-93 Instr.	Ø7Ø-Ø1452
4	Standoffs, nylon	63Ø-Ø118Ø
1	I.C., 74LS74	3Ø3-ØØ7Ø3
1	I.C., 74LS283	3Ø3-ØØ716

INSTALLATION INSTRUCTIONS:

1. Unplug the PRIME TIME Model 93.
2. Remove top cover of PRIME TIME (seven screws).
3. Each module may be held in place by four nylon standoff retainers or four threaded spacers with nylon screws. Refer to section 5.Ø.1 for module removal instructions.

4. Locate jumber wires W1, W3, W4 on the silkscreen. Clip out jumper wires W1, W3, W4 using wire clippers (de-soldering is not necessary).
5. Insert jumper wire W2 and neatly solder in place
6. Install U22 (74LS283) and U26 (74LS74), being sure to orient the chips properly in the sockets. (All chips U18 through U29 should be oriented in the same direction).
7. Insert the four standoffs or spacers on the main memory board in the larger holes. (Refer to the motherboard for standoff installation technique).
8. Insert the memory extension board on the main memory board, making sure that all connectors seat properly.
9. Install the expanded memory module in the motherboard, making sure all connectors seat properly
10. Replace top cover

In case of difficulty, contact Lexicon, Inc.

5.3 AUDIO SECTION MAINTENANCE

NOTE: Reference numbers for REV 3 Analog Daughter Boards are different from those for REV 1 Boards. Reference numbers in parentheses refer to REV 3 boards.

5.3.1 DAC REPLACEMENT

In the event that the DAC requires replacement, it should be replaced with an identical Part No. MC3510 or AD561 depending on the original factory installation.

If the MC3510 is replaced the offset adjustment R36(R16) should be set for symmetrical clipping at the limit level. It is best to inject a 400Hz signal and adjust the generator amplitude until clipping is observed on both positive and negitive waveform peaks. Adjust R36(R16) for exactly symmetrical clipping. Use a generator level very close to clipping for the most accurate adjustment.

Replacement of either DAC will require recalibration of conversion levels. See section 2.3 for calibration procedure.

5.3.2 BYPASS OF DIGITIZING SUBSYSTEMS

In instances where it is uncertain if a problem is associated with the analog or digital systems, it is possible to bypass the analog daughter board and pass audio directly through the entire analog signal chain. This procedure will also be necessary to troubleshoot the output signal chains.

Procedure: Remove the analog daughter board. Connect a small jumper wire from pin 4 of J7 to pin 6 of J7 to test Delay A and to pin 8 of J7 to test Delay B. This bypasses the gain changing and converter stages normally in the signal path.

It is also possible to bypass just the ADC/DAC subsystem. Remove U8(U3) on the analog daughter board. Connect a small jumper wire directly from the U11(U2) sample-and-hold output at R28 (R9) to pin 12 of the U8(U3) socket for Delay A or to pin 2 of the U8(U8) socket for Delay B.

5.3.3 SUSPECTED DIGITAL PROBLEMS

For suspected digital problems first verify that all digital signals reach the analog board. Compare these signals with the waveform charts and photographs.

Also verify that the signal DATA from U1Ø(U4) reaches the motherboard. Substitution of a known good analog daughter board is also a powerful technique to localize a problem.

5.3.4 FILTER PROBLEMS

Signal tracing in the audio input and output stages should be straight forward. A problem in a single filter section could be due to a number of causes. A good first try is op amp replacement. Polypropylene capacitors in the large switching array are good suspects. Beware of tabs on the Delay Multiply switch wafers shorting to adjacent wafers. Component replacement in a filter section will necessitate re-calibration of the filter. Refer to section 2.1 for calibration procedure.

Should a problem arise which requires replacement of the Delay Multiply switch, it may not be necessary to remove the whole switch. It is possible to remove one wafer at a time by using the following procedure:

1. Remove the front panel board. See section 5.Ø.1 for proper procedure.
2. Remove the two long screws which run the length of the Delay Multiply witch. Be careful not to lose the nut, split lock washer, phenolic spacer or any of the three metal spacers associated with each screw.
3. Pull the shaft forward and remove it from the switch.
4. Desolder and remove only the suspected bad wafers.
5. To reassemble, place the wafer in position and replace the shaft and long screws before soldering the wafer in place. When tightening the long screws, do not over-torque: the phenolic spacers are extremely fragile. Hand tightening the nuts on the rear wafer is sufficient.

For sticky problems, refer the unit to the factory for repair.

5.3.5 ANALOG DAUGHTER BOARD REPAIR

Should component replacement on the analog daughter board become necessary, it may be necessary to remove the shield covering part of the daughter board. The shield is held in place by four beads of silicone cement. To remove the shield simply pull it off. To replace the shield, reglue it with an appropriate silicone compound (such as Dow Corning Silicone Rubber Sealant). Shield replacement is recommended for optimum noise performance.

5.4 VCO MAINTENANCE

The VCO section is located on the front left-center of the Motherboard. Trouble-Shooting in this area of the Motherboard is tricky due to high component density. Care should be taken to avoid accidental shorts while probing.

Component replacement in the VCO section may necessitate recalibration. To check calibration, refer to section 2.2.

M93 ANALOG DAUGHTER BOARD ASSY

PART NO.	QTY	DESCRIPTION	REF.
TRIM RESISTORS			
201-00432	2	RES,TRM,ST,PC,5K,SA,CER	R9,18
CARBON FLM RES			
202-00502	2	RES,CF,10%,1/2W,270 OHM	R40,41
202-00505	1	RES,CF,5%,1/4W,10 OHM	R17
202-00520	2	RES,CF,5%,1/4W,270 OHM	R8,21
202-00524	2	RES,CF,5%,1/4W,470 OHM	R36,37
202-00542	6	RES,CF,5%,1/4W,4.7K OHM	R22,23,34,35,38,39
202-00543	2	RES,CF,5%,1/4W,5.1K OHM	R12,20
202-00549	4	RES,CF,5%,1/4W,10K OHM	R1,2,28,29
METAL FLM RES			
203-00446	3	RES,MF,1/2%,1/8W,316 OHM	R3,27,33
203-00447	3	RES,MF,1/2%,1/8W,681 OHM	R5,24,30
203-00448	3	RES,MF,1/2%,1/8W,2.15K OHM	R4,25,31
203-00449	3	RES,MF,1/2%,1/8W,6.81K OHM	R6,26,32
203-00463	2	RES,MF,1%,1/8W,3.24K OHM	R11,19
NETWORK RES			
205-00330	1	RES,NET,SIP,2%,3.3KX9	RP1
ELECTROLYT CAP			
240-00608	1	CAP,ELEC,2.2uF,50V,RAD	C1
240-00614	3	CAP,ELEC,47uF,16V,RAD	C7,28,31
TANTALUM CAP			
241-00652	5	CAP,TANT,4.7uF,25V,RAD	C2,13,40-42
PCRB/PP CAP			
244-01151	1	CAP,PP,1000pF,2.5%	C45
244-01167	4	CAP,PP,750pF,2.5%	C23,25,35,37
CERAMIC CAP			
245-00587	1	CAP,CER,82pF,1000V,10%	C5
245-00590	1	CAP,CER,150pF,500V,10%	C19
245-00599	24	CAP,CER,.02uF,20V,80/20%	C3,4,6,8,10,12,14-17,21,22,24 C26,27,29,30,C32-34,36,38,39,43
245-00602	2	CAP,CER,.05uF,25V,80/20%	C9,18
245-00607	1	CAP,CER,39pF,1000V,10%	C20
DIODES			
300-01027	2	DIODE,1N754	CR14,15

M93 ANALOG DAUGHTER BOARD ASSY

PART NO.	QTY	DESCRIPTION	REF.
DIODES (CON'T)			
300-01029	12	DIODE,1N914 AND 4148	CR1,2,4-13
LINEAR IC			
340-00722	1	IC,LINEAR,LM301	U6
340-00725	1	IC,LINEAR,LM311	U4
340-00727	1	IC,LINEAR,LF398	U2
340-00737	1	IC,LINEAR,CA 3140S	U1
340-01566	3	IC,LINEAR,LF353,DUAL OP AMP	U8,11,13
SS SW IC			
346-00769	3	IC,SS SWITCH,4051	U7,9,10
346-00770	1	IC,SS SWITCH,4053	U12
346-02073	1	IC,SS SWITCH,MC14053 (SELECT)	U3
CONVERTER IC			
355-00773	1	DAC,AD 561J	U5
PC MNT CONN			
510-01067	2	CONN,POST,100X025,HDR,12MCG	J6
510-03088	1	CONN,POST,100X025,HDR,10MCG	J7
SOCKETS			
520-00941	6	IC SCKT,8 PIN,PC,LO-PRO	U1,4,6,8,11,13
520-00943	6	IC SCKT,16 PIN,PC,LO-PRO	U3,5,7,9,10,12
PC BOARDS			
710-01045	1	PC BD,ANLG,M93	

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M93 MEMORY BOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
CARBON FLM RES			
202-00502	1	RES,CF,10%,1/2W,270 OHM	R1
202-00505	2	RES,CF,5%,1/4W,10 OHM	R2,3
202-00529	1	RES,CF,5%,1/4W,1K OHM	R4
NETWORK RES			
205-00330	2	RES,NET,SIP,2%,3.3KX9	RP1,2
205-01155	2	RES,NET,DIP,2%,68X7	RP3,4
TANTALUM CAP			
241-00652	3	CAP,TANT,4.7uF,25V,RAD	C3,16,18
241-00654	1	CAP,TANT,22uF,16V,RAD	C17
241-00655	1	CAP,TANT,22uF,25V,RAD	C1
CERAMIC CAP			
245-00590	1	CAP,CER,150pF,500V,10%	C34
245-00599	28	CAP,CER,.02uF,20V,80/20%	C2,4-15,19-33
INDUCTORS			
270-00779	1	FERRITE,BEAD	FB2
270-01215	1	INDUCTOR,100uH	L1
DIODES			
300-01154	1	DIODE,1N751,ZENER,5.1V	CR1
DIGITAL/CMOS IC			
330-00695	1	IC,DIGITAL,74LS04	U18
330-00697	1	IC,DIGITAL,74LS10	U19
330-00703	1	IC,DIGITAL,74LS74	U26
330-00713	2	IC,DIGITAL,74LS174	U1,3
330-00716	4	IC,DIGITAL,74LS283	U22-25
330-00717	3	IC,DIGITAL,74LS293	U27-29
330-00719	2	IC,DIGITAL,74LS368	U2,4
LINEAR IC			
340-00746	1	IC,LINEAR,78L 12 ACZ	U30
340-00750	1	IC,LINEAR,DS 3672	U5
MEMORY IC			
350-00754	12	IC,DRAM 4060 OR 2680,4K RAM	U6-17
PC MNT CONN			
510-01062	4	CONN,POST,100X025,PC,12FCG,TOP	J19-22

M93 MEMORY BOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
PC MNT CONN (CON'T)			
510-01067	1	CONN,POST,100X025,HDR,12MCG	J5
510-01068	1	CONN,POST,100X025,HDR,18MCG	J3
510-03088	1	CONN,POST,100X025,HDR,10MCG	J4
SOCKETS			
520-00941	1	IC SCKT,8 PIN,PC,LO-PRO	U5
520-00942	6	IC SCKT,14 PIN,PC,LO-PRO	U18,19,26-29
520-00943	8	IC SCKT,16 PIN,PC,LO-PRO	U1-4,22-25
520-00944	12	IC SCKT,22 PIN,PC,LO-PRO	U6-17
BULK WIRE			
670-01768	1	WIRE,JMP,22AWG,0.5",TEF,WHT	W2
PC BOARDS			
710-01044	1	PC BD,MEM,M93	

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M93 FRONT PANEL BOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
POTENTIOMETERS			
200-01046	12	POT,SLD,PC,20K-A,15MM X 30MM	R6-10,17-23
200-01078	1	POT,RTY,SL,10K-U/10K-U/SW	R4/S2
CARBON FLM RES			
202-00503	1	RES,CF,5%,1/2W,1.5K OHM	R24
202-00515	1	RES,CF,5%,1/4W,150 OHM	R1
202-00524	1	RES,CF,5%,1/4W,470 OHM	R3
202-00529	4	RES,CF,5%,1/4W,1K OHM	R2,5,12,16
202-00542	2	RES,CF,5%,1/4W,4.7K OHM	R11,14
202-00580	2	RES,CF,5%,1/4W,1M OHM	R13,15
NETWORK RES			
205-00331	1	RES,NET,SIP,2%,150X5	RP7
205-01076	6	RES,NET,DIP,2%,820X8	RP1-6
TANTALUM CAP			
241-00652	3	CAP,TANT,4.7uF,25V,RAD	C1,6,7
PCRB/PP CAP			
244-00660	2	CAP,MYL,.01uF,100V,10%,RAD	C2,3
CERAMIC CAP			
245-00599	2	CAP,CER,.02uF,20V,80/20%	C4,5
TRANSISTORS			
310-01007	2	TRANSISTOR,2N3904	Q1,2
LINEAR IC			
340-00740	1	IC,LINEAR,4558	U2
INTERFACE IC			
345-00751	1	IC,INTER,D8877,75492 LED DRVR	U1
DSPLY/IND/LED			
430-00904	7	LED,HP #5082-4850	CR1,3-8
430-01072	6	LED,DSPLY,7-SEG,HP#5082-7730	D1A,D2A,D3A,D1B,D2B,D3B
430-01212	1	LED,HP #5082-4480	CR2
TOGGLE SWITCH			
450-01073	4	SW,TGL,1P2T,BLK BUSH,PC,GOLD C	S3-6

M93 FRONT PANEL BOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
PSH BUT SWITCH			
453-01074	1	SW,PBM,1P2T,PC,4A	S1,ALL C&K SWITCHES MARKED ON LEFT FOR POLARITY. C&K GOING FORWARD.
PC MNT CONN			
510-01064	1	CONN,POST,100X025,PC,10FCG,BOT	J8
510-01219	4	CONN,POST,100X025,PC,18FCG,BOT	J1,2,8
SOCKETS			
520-00941	1	IC SCKT,8 PIN,PC,LO-PRO	U2
520-00942	1	IC SCKT,14 PIN,PC,LO-PRO	U1
520-01075	6	IC SCKT.14PIN,PC	(DISPLAY SOCKET)
SPCR,NON-INSUL			
635-01224	1	BUSHING EXTENDER,3/8-32X5/8	(FOR R4/S2)
MACHINE SCREWS			
640-02747	12	SCRW,2-M2X.4X3/16L,PNH,PH,ZN	R6-10,17-23 GND
BULK WIRE			
670-01771	17	WIRE,24AWG,7/32,YEL	R4/S2,CUT FIVE 2.5" LENGTHS R4/S2,CUT ONE 4" LENGTH
PC BOARDS			
710-01071	1	PC BD,FRONT PANEL,M93	

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M93 MOTHERBOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
SLIDE SWITCH (CON'T)			
451-00971	1	SW,SL,2P2T,V-CHNG,PC	S6
ROTARY SWITCH			
452-00777	2	SW,RTY,60 POS,GRIGSBY	S4,5
452-01079	1	SW,RTY,12P4T,GRIGSBY	S3
PSH BUT SWITCH			
453-00966	1	SW,PBPP,2P2T,WINK,BLU,PCRA	S7
TRANSFORMERS			
470-00261	1	XFORMER,OTPT,M92	T1
PC MNT CONN			
510-00892	6	1/4" PHONE JACK,PCRA	J9-14
510-01061	2	CONN,POST,100X025,PC,10FCG,TOP	J4,7
510-01062	3	CONN,POST,100X025,PC,12FCG,TOP	J5,6
510-01063	1	CONN,POST,100X025,PC,18FCG,TOP	J3
510-01069	1	CONN,POST,100X025,HDR,RA,10MCG	J8
510-01218	4	CONN,POST,100X025,HDR,RA,18MCG	J1,2,8
SOCKETS			
520-00831	2	CONN,XISTOR,TO-220/202	U69,70
520-00941	22	IC SCKT,8 PIN,PC,LO-PRO	
520-00942	30	IC SCKT,14 PIN,PC,LO-PRO	
520-00943	13	IC SCKT,16 PIN,PC,LO-PRO	
520-00945	1	IC SCKT,24 PIN,PC,LO-PRO	
ELECTRONIC HDWR			
600-00871	4	FUSE CLIP,1/4",PC	F1,2
INSUL/SPACRS			
630-01182	3	SPCR,PCB,PUSHON/PUSHON,1"	
630-01894	1	INSUL,SEMI,TO-5 SPCR	U67
MACHINE SCREWS			
640-01714	1	SCRW,6-32X3/8,PNH,PH,SS	
640-01716	2	SCRW,6-32X3/8,PNH,PH,ZN	
640-01841	2	SCRW,2-56X1/4,PNH,PH,ZN	
NUTS			
643-01730	1	NUT,6-32,KEP,SMALL,ZN	

M93 MOTHERBOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
NUTS (CON'T)			
643-01731	2	NUT,6-32,SPEED,SLF RETAIN	
643-01855	2	NUT,2-56,HEX,SMALL,ZN	
WASHERS			
644-01740	2	WSHR,LOCK,SPLIT,#6	
644-01854	2	WSHR,LOCK,SPLIT,#2	
BULK WIRE			
670-01768	1	WIRE,JMP,22AWG,0.5",TEF,WHT	CR25
670-01974	2	WIRE,JMP,22AWG,0.1",NON-INSUL	
PRE-CUT WIRE			
675-02852	1	WIRE,16G,GRN,4",ST1/4XST&T1/4	
675-02864	3	WIRE,18G,BLK,18",ST&T1/4X0	
PANELS			
702-01132	1	COVER,PROTECTIVE	
HEAT SINKS			
704-00262	1	HEAT SINK,DIP	U62
704-01895	1	HEAT SINK,TO-5	
PC BOARDS			
710-01125	1	PC BD,MOTHERBD,M93	

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M93 MOTHERBOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
PCRB/PP CAP (CON'T)			
244-01169	17	CAP,PP,2200pF,2.5%	C79,83,87,91,95,99,101,102,111 C115,119,123,C127,131,135,139 143
244-01170	3	CAP,PP,2400pF,2.5%	C17,38,59
244-01171	15	CAP,PP,5100pF,2.5%	C80,84,88,92,96,100,112,116 C120,124,128,C132,136,140,144
244-01172	1	CAP,PP,6800pF,2.5%	C103
244-01174	1	CAP,PP,16000pF,2.5%	C104
CERAMIC CAP			
245-00590	9	CAP,CER,150pF,500V,10%	C5-10,20,22,39
245-00596	2	CAP,CER,.005uF,1.6KV,Z5U	C204,205
245-00598	3	CAP,CER,.01uF,16V,80/20%	C56,185,U55(PIN 9 TO PIN 8)
245-00600	76	CAP,CER,.02uF,35V,80/20%	C3,4,11,12,15,16,18,19,21 C23-25,28,29,C32,33,36,37,40,42 44-47,50-52,C54,57,58,60,61,64 65,68,69,73,C75,76,154-182 191-196,206
245-00604	2	CAP,CER,.1uF,12V,80/20%	C184,202
245-01164	14	CAP,CER,10pF	C26,27,30,31,34,35,48,49,55,62 C63,66,67,C187
VARIABLE CAP			
246-01146	1	CAP,TRIM,5-40pF,VAR	C188
INDUCTORS			
270-00779	5	FERRITE,BEAD	FB1-5
DIODES			
300-01026	1	DIODE,1N753	CR22
300-01027	3	DIODE,1N754	CR8,9,33
300-01029	9	DIODE,1N914 AND 4148	CR1-3,26-31
300-01030	10	DIODE,1N4004 AND 4005	CR10-17,23,24
300-01032	4	DIODE,1N5404	CR18-21
TRANSISTORS			
310-01008	1	TRANSISTOR,2N3906	Q3
310-01014	1	TRANSISTOR,C122F1,SCR	Q4
310-01237	1	TRANSISTOR,MJE-170,PNP	Q2
310-01238	1	TRANSISTOR,MJE-180,NPN	Q1
DIGITAL/CMOS IC			
330-00169	1	IC,DIGITAL,TI,SN74S124,VCO	U62

M93 MOTHERBOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
DIGITAL/CMOS IC(CON'T)			
330-00668	2	IC,DIGITAL,7406	R21,41
330-00685	2	IC,DIGITAL,74123	U38,55
330-00692	7	IC,DIGITAL,74LS00	U23,39,44,47,48,51,52
330-00693	2	IC,DIGITAL,74LS02	U43,58
330-00695	5	IC,DIGITAL,74LS04	U28,32,40,50,56
330-00697	5	IC,DIGITAL,74LS10	U33,42,45,57,61
330-00699	2	IC,DIGITAL,74LS20	U37,46
330-00703	5	IC,DIGITAL,74LS74	U31,34-36,54
330-00711	2	IC,DIGITAL,74LS157	U59,60
330-00712	3	IC,DIGITAL,74LS163	U25,30,49
330-00714	1	IC,DIGITAL,74LS175	U53
330-00718	2	IC,DIGITAL,74LS367	U22,26
330-00766	1	IC,DIGITAL,4011,CMOS	U63
330-02074	1	IC,DIGITAL,SN74LS74A (SELECT)	U29
330-02085	1	IC,DIGITAL,AM25L04	U27
LINEAR IC			
340-00740	13	IC,LINEAR,4558	U6-8,10-12,15-18,20,64,66
340-00742	1	IC,LINEAR,7805 (LM 340 T-5)	U68
340-00745	1	IC,LINEAR,7815 (LM 340 T-15)	U69
340-00747	1	IC,LINEAR,7915 (LM 320 T-15)	U70
340-01183	2	IC,LINEAR,LF 356	U14,65
340-01546	1	IC,LINEAR,LM309H,5V REG	U67
340-01566	7	IC,LINEAR,LF353,DUAL OP AMP	U1-5,9,13
SS SW IC			
346-00770	1	IC,SS SWITCH,4053	U19
MEMORY IC			
350-00720	1	IC,PROM,82S123	U24
CRYSTALS			
390-01147	1	CRYSTAL,4.992MHz,GP,01%	
DSPLY/IND/LED			
430-00904	1	LED,HP #5082-4850	CR32
FUSES			
440-00868	1	FUSE,3AG,FAST,2.5AMP	F1
SLIDE SWITCH			
451-00970	2	SW.SL,2P2T,PCRA,GOLD C	S1,2

M93 MOTHERBOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
POTENTIOMETERS			
200-01080	1	POT,RTY,PC,500K-A/5K-U	R160,161
200-01208	2	POT,RTY,PC,10K-U,FLUSH SHAFT	R13,14
TRIM RESISTORS			
201-00432	1	RES,TRM,ST,PC,5K,SA,CER	R159
201-00433	6	RES,TRM,ST,PC,5K,SA,CC	R24,33,37,61,93,102
CARBON FLM RES			
202-00502	2	RES,CF,10%,1/2W,270 OHM	R115,116
202-00510	1	RES,CF,5%,1/4W,51 OHM	R165
202-00514	3	RES,CF,5%,1/4W,100 OHM	R12,19,53
202-00517	2	RES,CF,5%,1/4W,200 OHM	R79,164
202-00521	1	RES,CF,5%,1/4W,330 OHM	R131
202-00523	1	RES,CF,5%,1/4W,390 OHM	R132
202-00524	1	RES,CF,5%,1/4W,470 OHM	R124
202-00525	1	RES,CF,5%,1/4W,510 OHM	R162
202-00526	1	RES,CF,5%,1/4W,680 OHM	R103
202-00529	1	RES,CF,5%,1/4W,1K OHM	R51
202-00533	3	RES,CF,5%,1/4W,2K OHM	R123,147,153
202-00535	1	RES,CF,5%,1/4W,2.4K OHM	R146
202-00538	10	RES,CF,5%,1/4W,3.3K OHM	R122,125,127-129,134,137-140
202-00539	2	RES,CF,5%,1/4W,3.6K OHM	R11,20
202-00541	2	RES,CF,5%,1/4W,4.3K OHM	R104,105
202-00542	17	RES,CF,5%,1/4W,4.7K OHM	R18,22,23,47,52,60,77,84-87 R120,121,144,R157,158,170
202-00545	3	RES,CF,5%,1/4W,6.8K OHM	R10,21,136
202-00549	16	RES,CF,5%,1/4W,10K OHM	R17,44,54,55,57,67,80-83,118 R119,135,145,R171,172
202-00550	2	RES,CF,5%,1/4W,11K OHM	R110,111
202-00552	1	RES,CF,5%,1/4W,13K OHM	R56
202-00555	2	RES,CF,5%,1/4W,20K OHM	R78,108
202-00556	5	RES,CF,5%,1/4W,22K OHM	R15,46,70,106,107
202-00559	1	RES,CF,5%,1/4W,30K OHM	R130
202-00564	1	RES,CF,5%,1/4W,51K OHM	R149
202-00565	2	RES,CF,5%,1/4W,56K OHM	R112,113
202-00566	2	RES,CF,5%,1/4W,62K OHM	R109,148
202-00571	2	RES,CF,5%,1/4W,110K OHM	R117,133
202-00578	1	RES,CF,5%,1/4W,360K OHM	R150
202-00579	1	RES,CF,5%,1/4W,470K OHM	R59
202-01157	2	RES,CF,5%,1/2W,33 OHM	R75,76
202-01159	2	RES,CF,5%,1/4W,18K OHM	R114,126
202-01160	1	RES,CF,5%,1/4W,43K OHM	R151
202-01245	2	RES,CF,5%,1/4W,1.6K OHM	R73,74
202-01252	1	RES,CF,5%,1/4W,270K OHM	R58
METAL FLM RES			
203-00460	2	RES,MF,1%,1/8W,2.15K OHM	R3,4

M93 MOTHERBOARD ASSEMBLY

PART NO.	QTY	DESCRIPTION	REF.
METAL FLM RES (CON'T)			
203-00464	1	RES,MF,1%,1/8W,4.99K OHM	R155
203-00469	3	RES,MF,1%,1/8W,7.87K OHM	R8,49,90
203-00471	13	RES,MF,1%,1/8W,10.0K OHM	R26,27,34,35,39,40,63,64,91,92 R97,98,163
203-00477	3	RES,MF,1%,1/8W,12.7K OHM	R25,38,99
203-00482	4	RES,MF,1%,1/8W,20.0K OHM	R166-169
203-01141	3	RES,MF,1%,1/8W,31.6K OHM	R9,50,88
203-01142	3	RES,MF,1%,1/8W,39.2K OHM	R7,48,89
203-01143	1	RES,MF,1%,1/8W,2.49K OHM	R154
203-01144	1	RES,MF,1%,1/8W,19.6K OHM	R156
203-01145	1	RES,MF,1%,1/8W,1.24M OHM	R152
203-01162	2	RES,MF,1%,1/8W,9.31K OHM	R71,72
203-01246	3	RES,MF,1%,1/8W,17.4K OHM	R29,41,101
203-01247	3	RES,MF,1%,1/8W,12.4K OHM	R28,42,100
203-01248	3	RES,MF,1%,1/8W,19.1K OHM	R30,43,95
203-01249	3	RES,MF,1%,1/8W,5.23K OHM	R31,65,96
203-01250	3	RES,MF,1%,1/8W,15.4K OHM	R36,62,94
203-01251	3	RES,MF,1%,1/8W,8.06K OHM	R32,66,69
NETWORK RES			
205-00330	2	RES,NET,SIP,2%,3.3KX9	RP3,4
205-01133	2	RES,NET,DIP,1%,10KX8	RP1,2
ELECTROLYT CAP			
240-00609	1	CAP,ELEC,10uF,16V,RAD	C186
240-00614	1	CAP,ELEC,47uF,16V,RAD	C200
240-00620	2	CAP,ELEC,1000uF,35V,RAD	C149,150
240-00622	1	CAP,ELEC,4700uF,16V,AX	C152
240-01262	2	CAP,ELEC,330uF,25V,RAD	C147,148
TANTALUM CAP			
241-00652	10	CAP,TANT,4.7uF,25V,RAD	C70,71,145,146,153,183,198,199 C203,207
241-00654	3	CAP,TANT,22uF,16V,RAD	C72,74,151
PCRB/PP CAP			
244-00662	1	CAP,MYL,.1uF,5%,RAD	C43
244-01150	1	CAP,PCARB,.01uF,+-5%,B32548	C197
244-01166	2	CAP,PP,240pF,2.5%	C105,106
244-01167	31	CAP,PP,750pF,2.5%	C77,78,81,82,85,86,89,90,93,94 C97,98,107,C109,110,113,114,117 118,121,C122,125,126,129,130 133,134,C137,138,141,142
244-01168	1	CAP,PP,1600pF,2.5%	C108

FIG. 6.6 PIN CONNECTION CHART Con't

PIN#	MEMORY J3	MEMORY J4	MEMORY J5
1	GREAD//READ/	RLCK/	GXØ
2	MSEL 5	PRES	DAC9
3	MSEL 6	CE/	GX1
4	MSEL 7	WEG/	DAC6
5	MSEL 8	RESET	DAC7
6	MSEL 2	-15V	DAC8
7	MSEL 1	AN GND	DAC5
8	MSEL 3	+15V	DAC4
9	MSEL 4	DIG GND	DACØ
10	MEX 1	5V	DAC1
11	MEX Ø	----	DAC2
12	MEX 2	----	DAC3
13	MEX 3	----	----
14	DMCY/	----	----
15	NSTRBG/	----	----
16	GREAD	----	----
17	READ/	----	----
18	DOUT/	----	----

Figure 6.6 PIN CONNECTION CHART

PIN #	FRONT PANEL J1	FRONT PANEL J2	FRONT PANEL AUDIO J8	ANALOG DAUGHTER J6	ANALOG DAUGHTER J7
1	8.5V	DISPL B 3G	----	HLNG1/	AN GND
2	PRES	DISPL B 3A	----	HLNGØ/	+15V
3	DISPLA 3D	DISPL B 3C	MSTR WPR/HI	HLGYO/	-15V
4	DISPLA 2A	DISPL B 3B	MSTR LO	HLGZ1/	IN FIL
5	DISPLA 2D	DISPL B 1B	IN WPR INMIX	HLGY1/	IN FIL GND
6	DISPLA 2C	DISPL B 3P	AUX WPR INMIX	HLOZØ/	A FIL
7	DISPLA 3E	RPT HLD	A WPR INMIX	HLN/	DLY FIL GND
8	DISPLA 2B	RPT HLD LED	B WPR INMIX	HLNSH2/	B FIL
9	DISPLA 1C	-4Ø dB	MSTR WPR OUTMIX	HLNSH1/	----
1Ø	DISPLA 3F	MAN DLY TOP	----	DAC 9	----
11	MSEL A9	DIG GND	IN WPR OUTMIX	DAC 6	----
12	DISPLA 3A	XTAL/VCO	AUX WPR OUTMIX	DAC 7	----
13	DISPLA 3G	5 VOLTS	A WPR OUTMIX	DAC 8	----
14	DISPLA 1A,D,E,G	MAN DLY WPR	B WPR OUTMIX	DAC 5	----
15	DISPLA 2R	-3ØdB	BYPASS	DAC 4	----
16	DISPLA 2E	-2ØdB	OVERLOAD	DAC Ø	----
17	DISPLA 2F	-1ØdB	OUT MSTR/HI	DAC 1	----
18	DISPLA 3B	ØdB	AN GND	DAC 2	----
19	DISPLA 2G	----	-15V	DAC 3	----
2Ø	DISPLA 1B	----	+15V	DATA	----
21	DISPLA 3C	----	IN INV	DIG GND	----
22	DISPLA 3P	----	A INV	+5V	----
23	DISPLB 2A	----	B INV	----	----
24	DISPLB 2C	----	B OUTMIX	N	----
25	DISPLB 3D	----	A OUTMIX	----	----
26	DISPLB 2D	----	AUX HI INMIX	----	----
27	DISPLB 2B	----	IN HI INMIX	----	----
28	DISPLB 1C	----	IN GND INMIX	----	----
29	DISPLB 3E	----	----	----	----
3Ø	DISPLB 3F	----	----	----	----
31	MSEL B9	----	----	----	----
32	DISPLB 2R	----	----	----	----
33	DISPLB 1A	----	----	----	----
34	DISPLB 2E	----	----	----	----
35	DISPLB 2F	----	----	----	----
36	DISPLB 2G	----	----	----	----

Fig 6.6 PIN CONNECTION CHART Con't

PIN #	MEMORY EXTENSION J19	J20	MEMORY EXTENSION J21	J22
1	MA2	GXO	-5V	ODAC9
2	CEL2	DAC9	GND	ODAC8
3	MA1	GX1	MA3	ODAC7
4	MA4	DAC6	+12V	ODAC6
5	MAO	DAC7	----	ODAC5
6	MA5	DAC8	----	ODAC4
7	MA11	DAC5	GND	ODAC1
8	MA6	DAC4	----	ODAC2
9	MA1Ø	DACØ	CS2/	ODAC3
1Ø	MA7	DAC1	+5V	ODACØ
11	MA9	DAC2	----	OGXØ
12	MA8	DAC3	WE/	OGX1

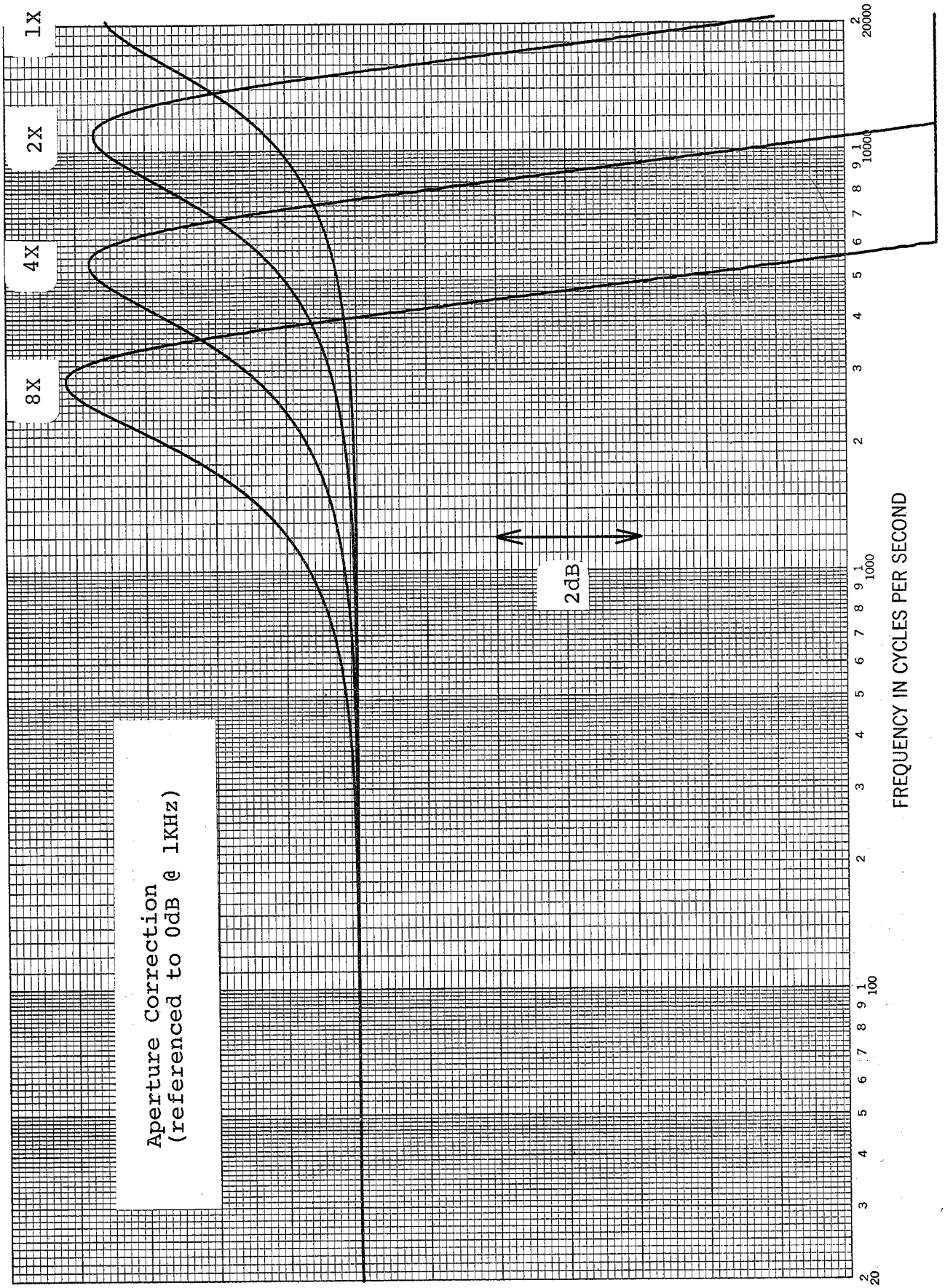


FIG. 6.5.3 APERTURE CORRECTION FREQUENCY RESPONSE

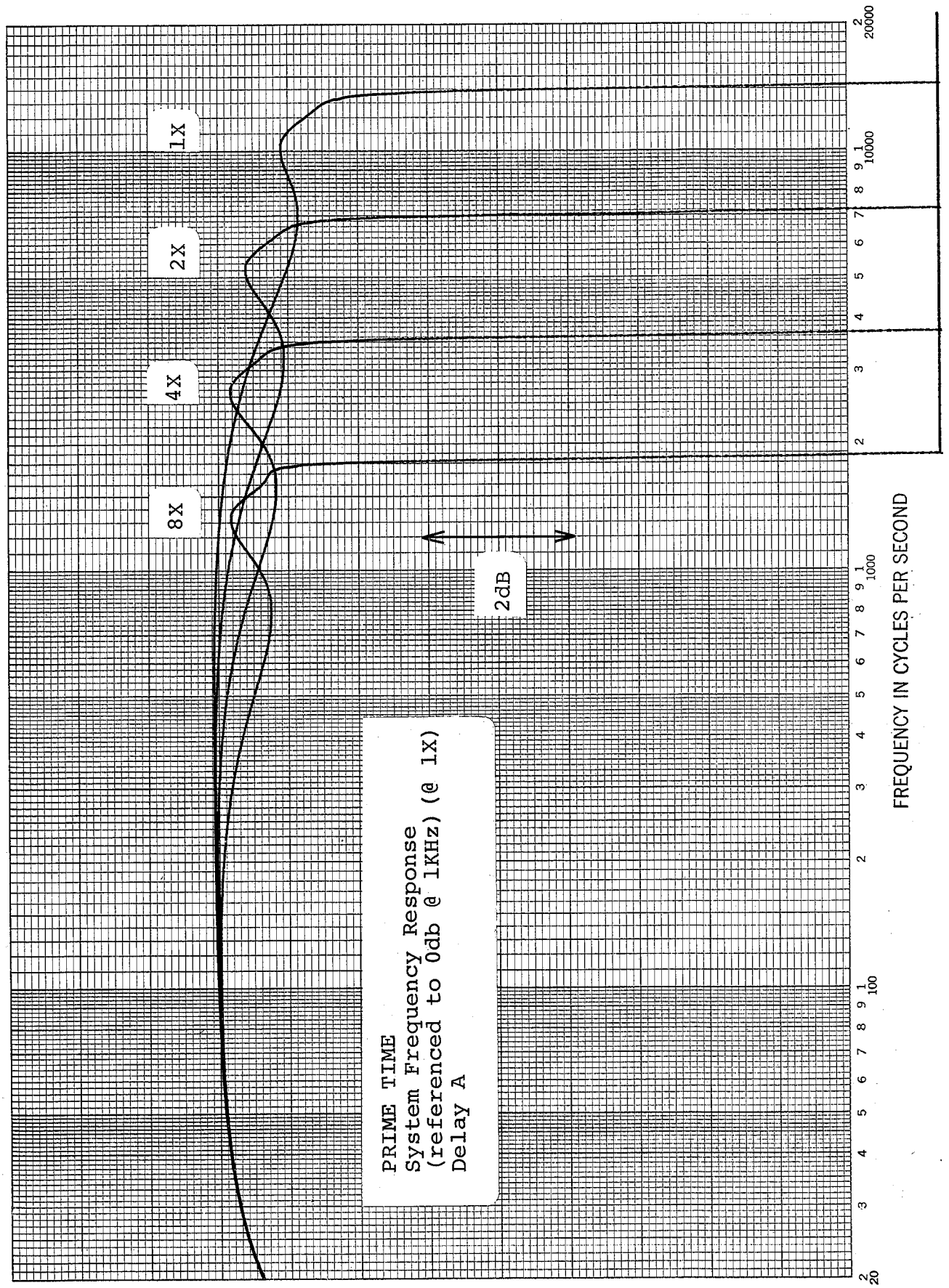


FIG. 6.5.4 SYSTEM FREQUENCY RESPONSE

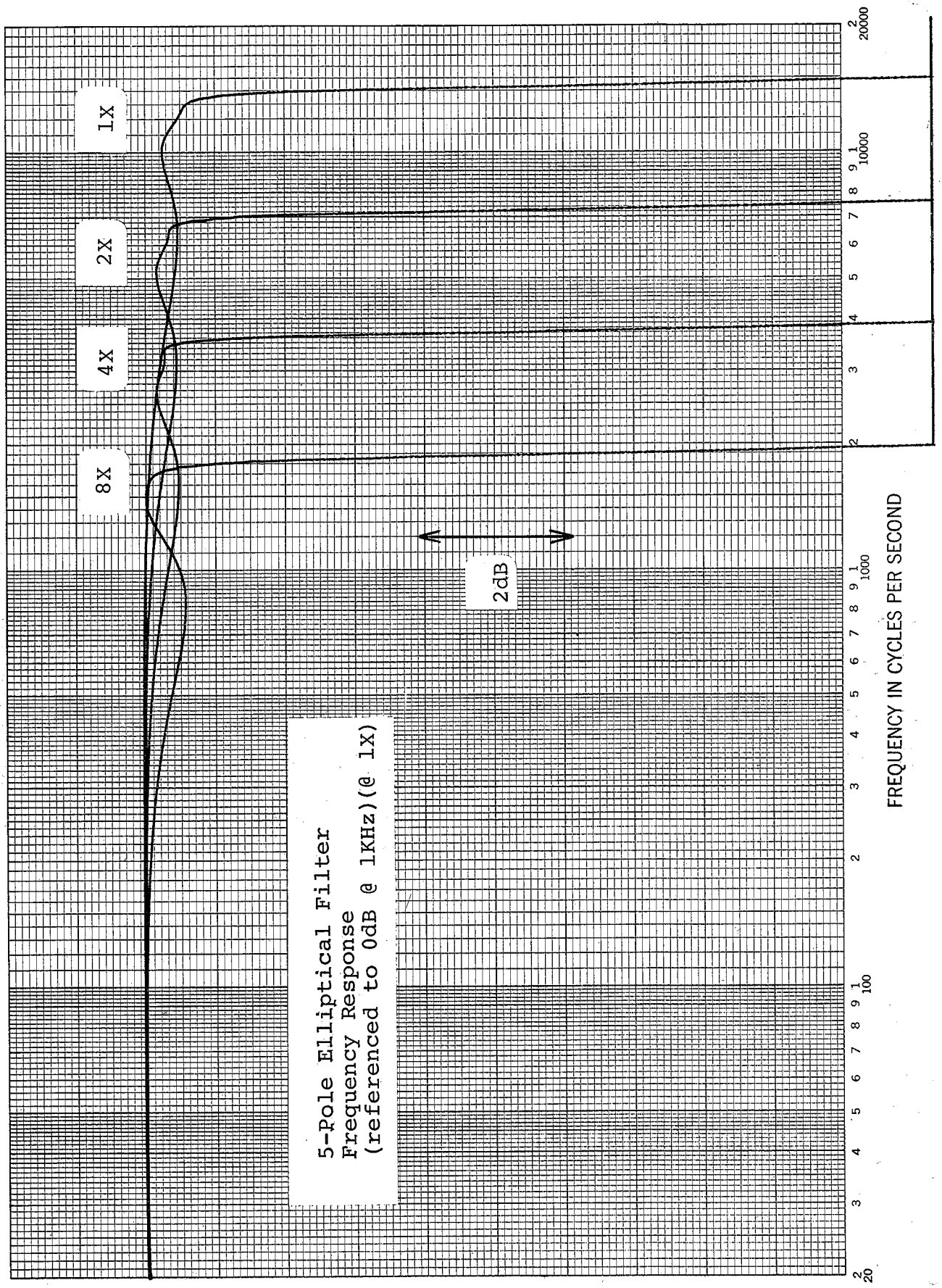


FIG. 6.5.1 5 POLE ELLIPTICAL FILTER FREQUENCY RESPONSE

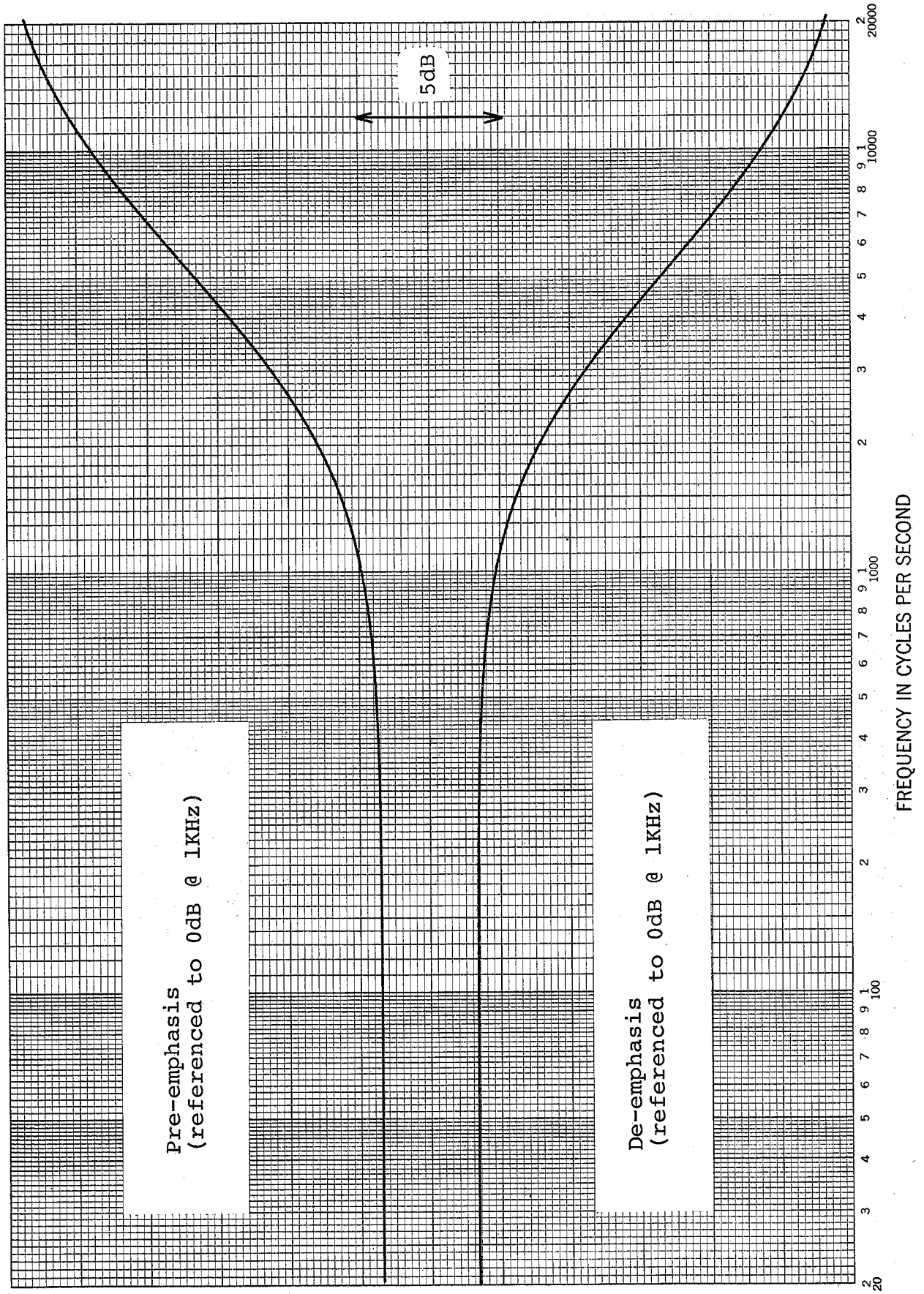


FIG. 6.5.2 PRE-EMPHASIS/ DE-EMPHASIS CURVES

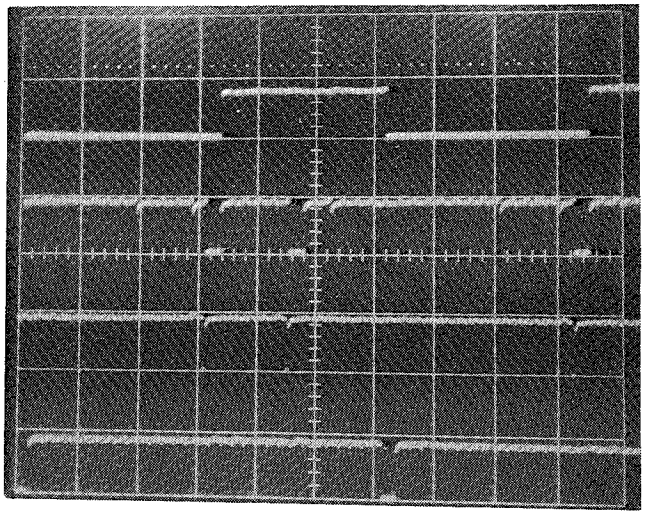
SYNC N 5V/DIV 5μS/DIV

27 N

25 $\overline{\text{READ}}$

44 $\overline{\text{RCLK}}$

28 $\overline{\text{WEG}}$



SYNC N 5V/DIV 5μS/DIV

27 N

29 CEL2

30 MSEL3 DELAY A=110MS

DELAY B=.5MS

31 MSEL4 DELAY A=110MS

DELAY B=.5MS

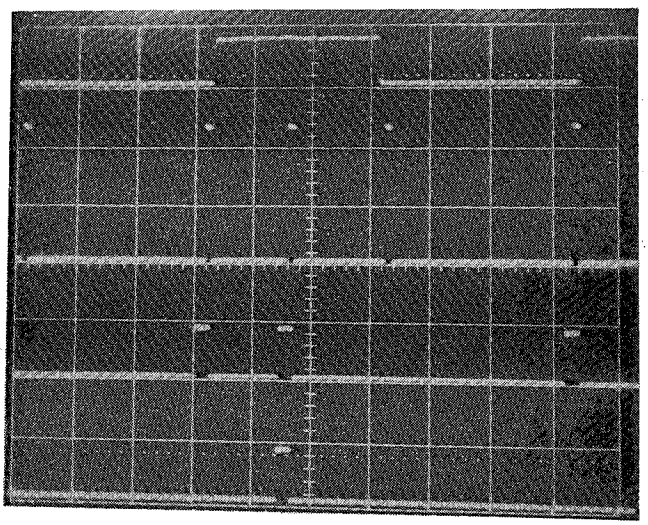
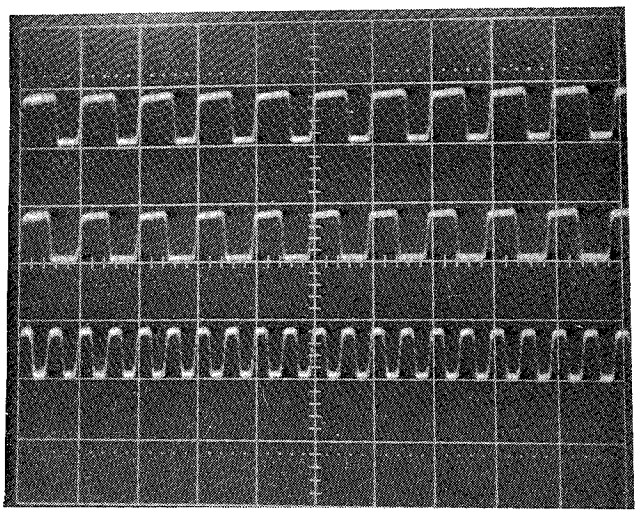
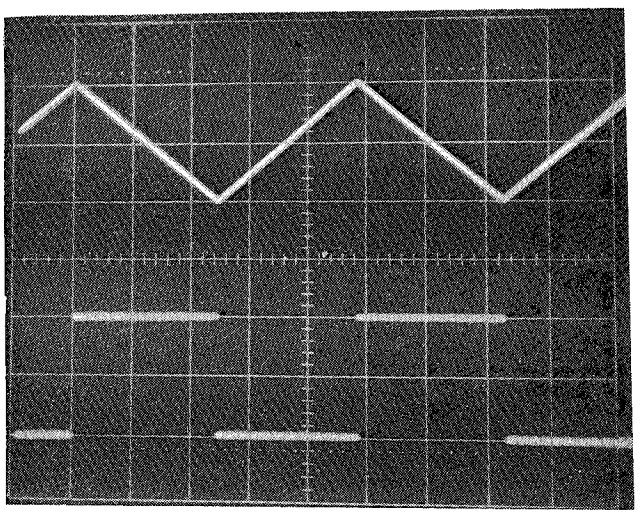


FIG. 6.4.5 MEMORY WAVEFORMS

SYNC MC 5V/DIV .2μS/DIV
DEPTH=FULL CCW
1 MC PIN 8 U44 CRYSTAL MODE
(DELAY ADJUST IN "CAL" POSITION)
1 MC VCO MODE
(DELAY ADJUST FULL CCW "UNCAL")
1 MC VCO MODE
(DELAY ADJUST FULL CW "UNCAL")



SYNC U65 PIN 6 5V/DIV 10μS/DIV
FREQ= FULL CW(~20 Hz)
33 U65 PIN 6
34 U63 PIN 3



SYNC U63 PIN 3 5V/DIV 10MS/DIV
FREQ= FULL CCW (20 Hz)
ALL WAVEFORMS AT WIPER OF DEPTH POT
(SOUTH END OF R151)
35 (1) DEPTH FULL CCW
(DELAY ADJUST SET SO V=2V)
35 (2) DEPTH AT 12 O'CLOCK
35 (3) DEPTH AT 3 O'CLOCK
35 (4) DEPTH FULL CW

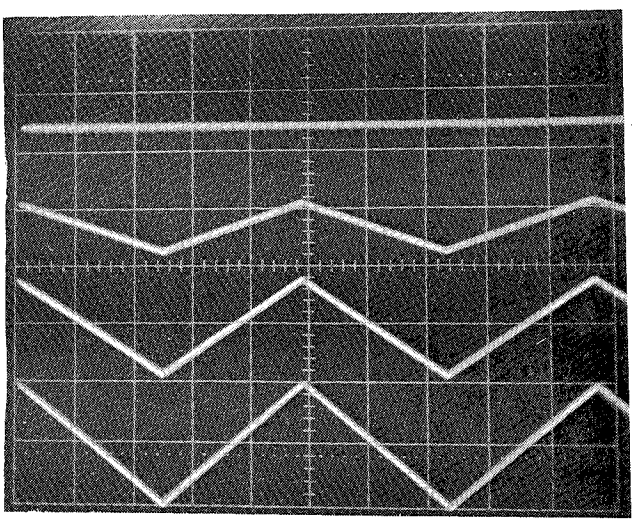
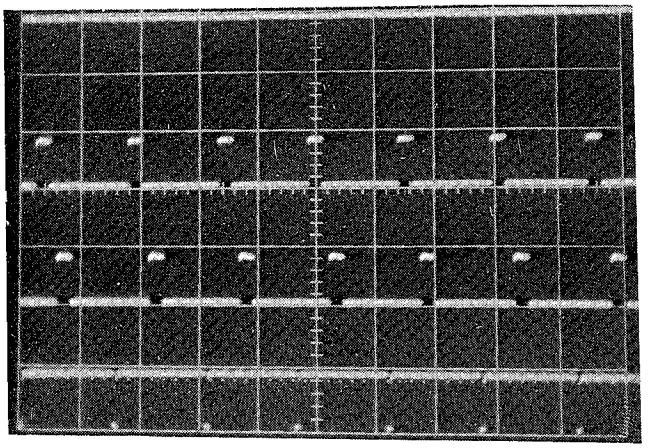
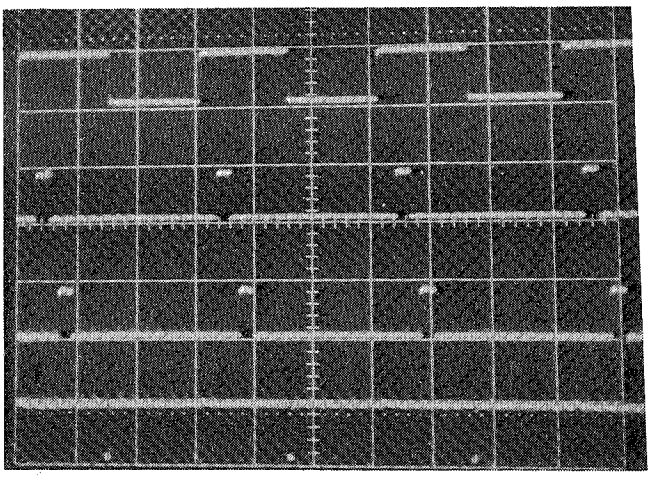


FIG. 6.4.6 VCO WAVEFORMS

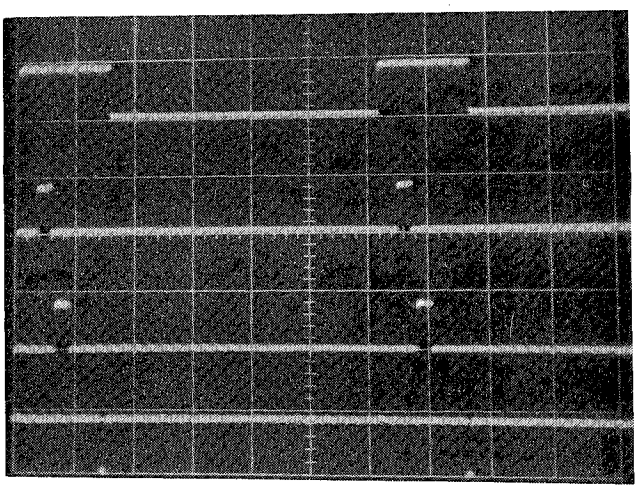
SYNC DMCY 5V/DIV 20 μS/DIV
DELAY MULTIPLY ON 1X
19 $\overline{\text{DMCY}}$ (AT HIGH LOGIC LEVEL)
20 NSH1
21 NSH2
22 PIN 3 U19 MEM



SYNC $\overline{\text{DMCY}}$ 5V/DIV, 20 μS/DIV
DELAY MULTIPLY ON 2X
19 $\overline{\text{DMCY}}$
20 NSH1
21 NSH2
22 PIN 3 U19 MEM



SYNC $\overline{\text{DMCY}}$ 5V/DIV 20 μS/DIV
DELAY MULTIPLY ON 4X
19 $\overline{\text{DMCY}}$
20 NSH1
21 NSH2
22 PIN 3 U19 MEM



SYNC $\overline{\text{DMCY}}$ 5V/DIV 20 μS/DIV
DELAY MULTIPLY ON 8X
19 $\overline{\text{DMCY}}$
20 NSH1
21 NSH2
22 PIN 3 U19 MEM

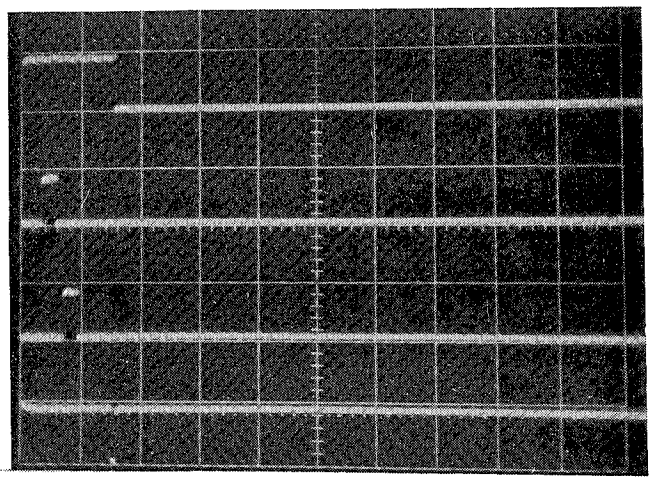


FIG. 6.4.3 DELAY MULTIPLY WAVEFORMS

SYNC N 5V/DIV 10μS/DIV

BOTH DELAYS ANY VALUE EXCEPT ZERO

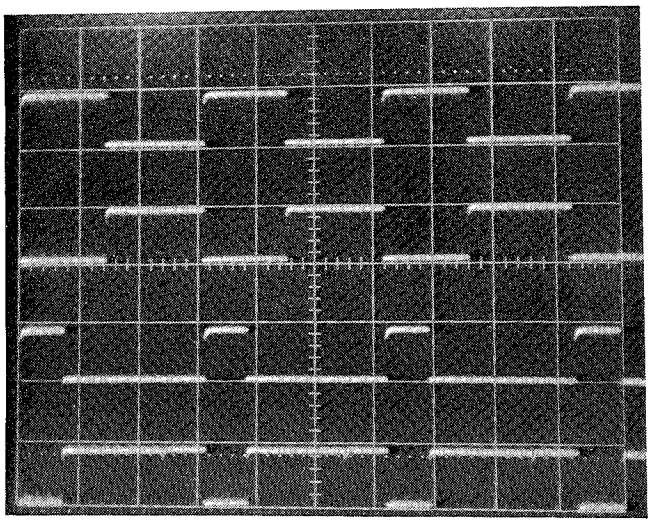
23 $\overline{\text{DIN}}$

24 $\overline{\text{DOUT}}$

DELAY B = ZERO MS

23 $\overline{\text{DIN}}$

24 $\overline{\text{DOUT}}$



SYNC N 5V/DIV 10μS/DIV

DELAY A = ZERO MS

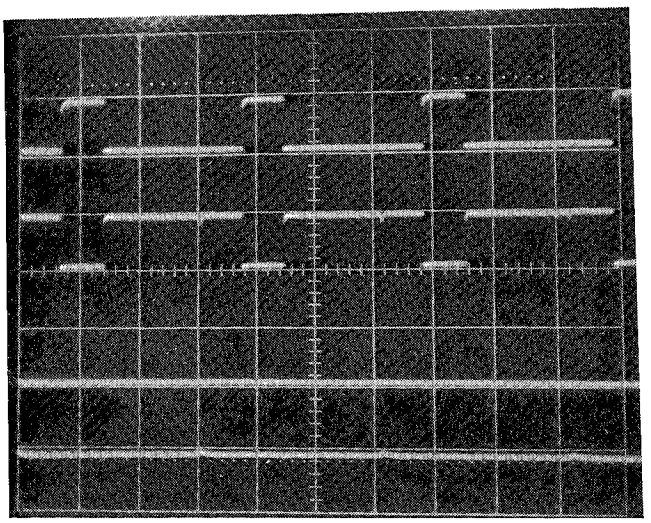
23 $\overline{\text{DIN}}$

24 $\overline{\text{DOUT}}$

BOTH DELAYS = ZERO MS

23 $\overline{\text{DIN}}$

24 $\overline{\text{DOUT}}$



SYNC $\overline{\text{READ}}$ 5V/DIV 5μS/DIV

25 $\overline{\text{READ}}$

26 GREAD - BOTH DELAYS≤128MS

26 GREAD - DELAY A>128MS
DELAY B≤128MS

26 GREAD - DELAY B>128MS
DELAY A≤128MS

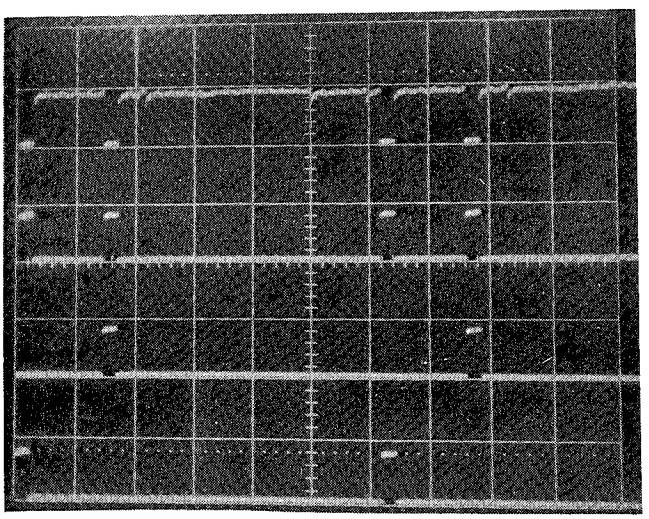


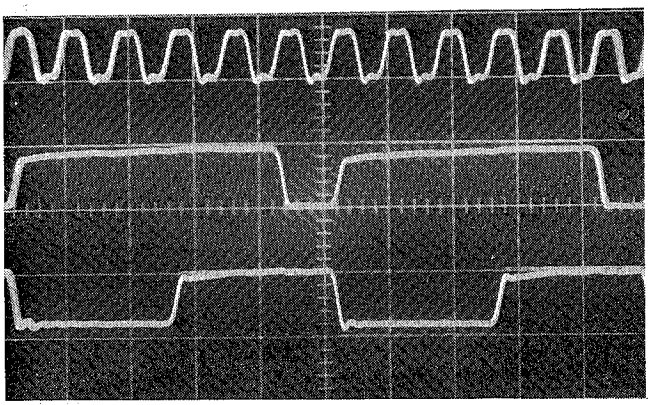
FIG. 6.4.4 DELAY SELECTION WAVEFORMS

PRIME TIME WAVEFORMS

1 0.2μS, 5V/DIV
MC U44, PIN8

2 $\overline{\text{CLK}}$
U23, PIN8

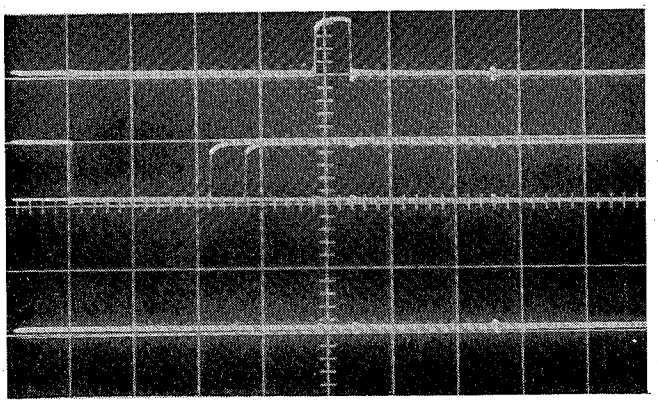
3 P
U30, PIN 11



4 SYNC ON $\overline{\text{N}}$
2μS, 5V/DIV
NSTRBG

5 D

6 U (AT GND LEVEL)
(INPUT 1KHZ @ LIMIT LEVEL)



4 NSTRBG

5 D

6 U
(NO INPUT SIGNAL)

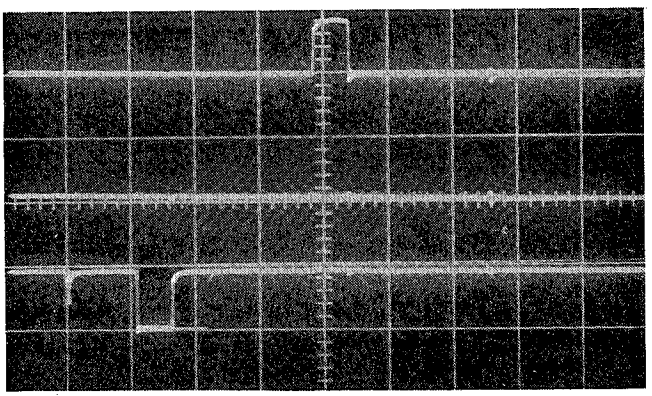


FIG. 6.4.1 MOTHERBOARD WAVEFORMS

SYNC ON $\overline{\text{HLN}}$

2μs, 5V/DIV

36 $\overline{\text{HLN}}$

8 DAC 9

9 DAC 8

10 DAC 7

11 DAC 6

12 DAC 5

13 DAC 4

14 DAC 3

15 DAC 2

16 DAC 1

17 DAC 0

18 DATA

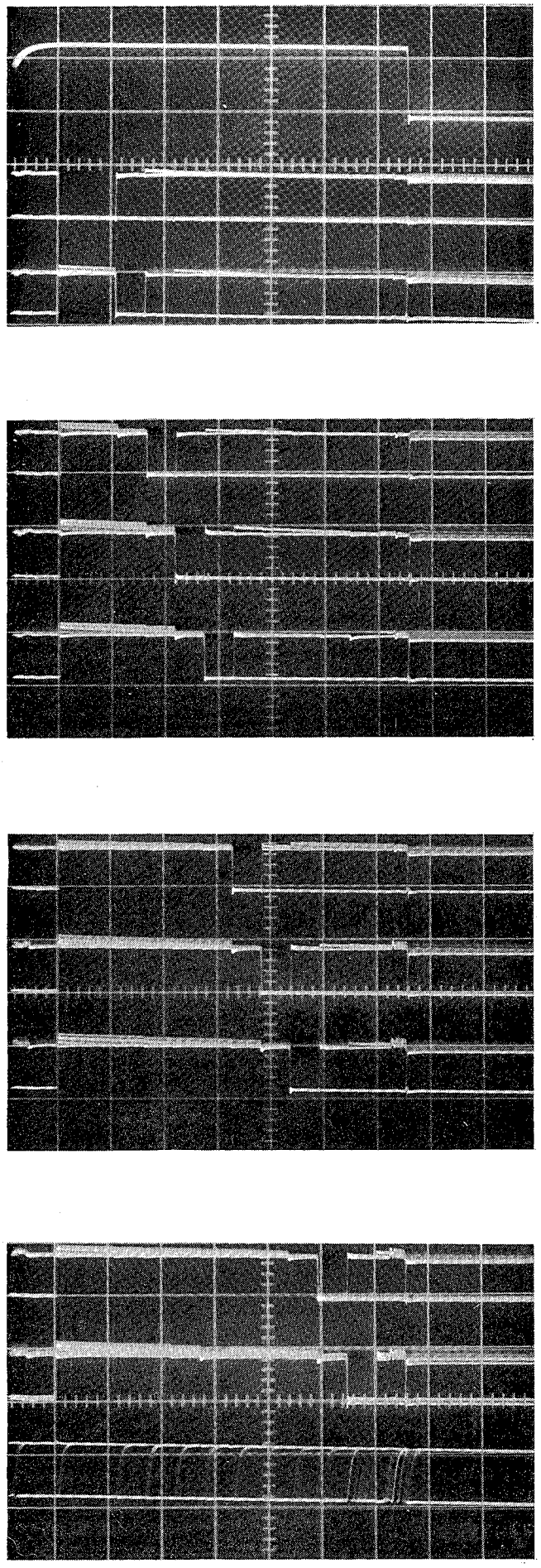


FIG. 6.4.2 ANALOG-DIGITAL CONVERSION WAVEFORMS

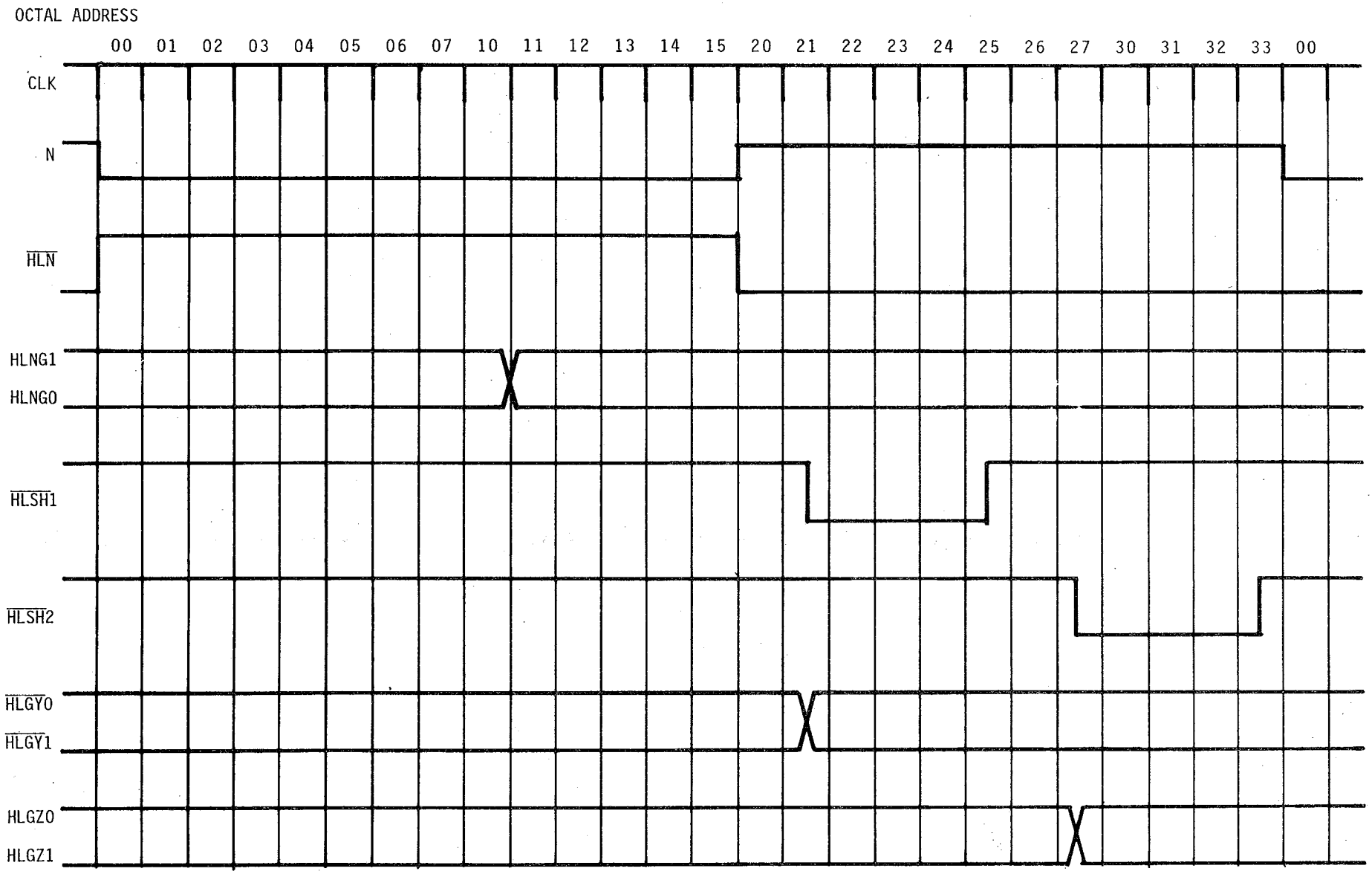


FIG. 6.3.4 ANALOG DAUGHTERBOARD TIMING

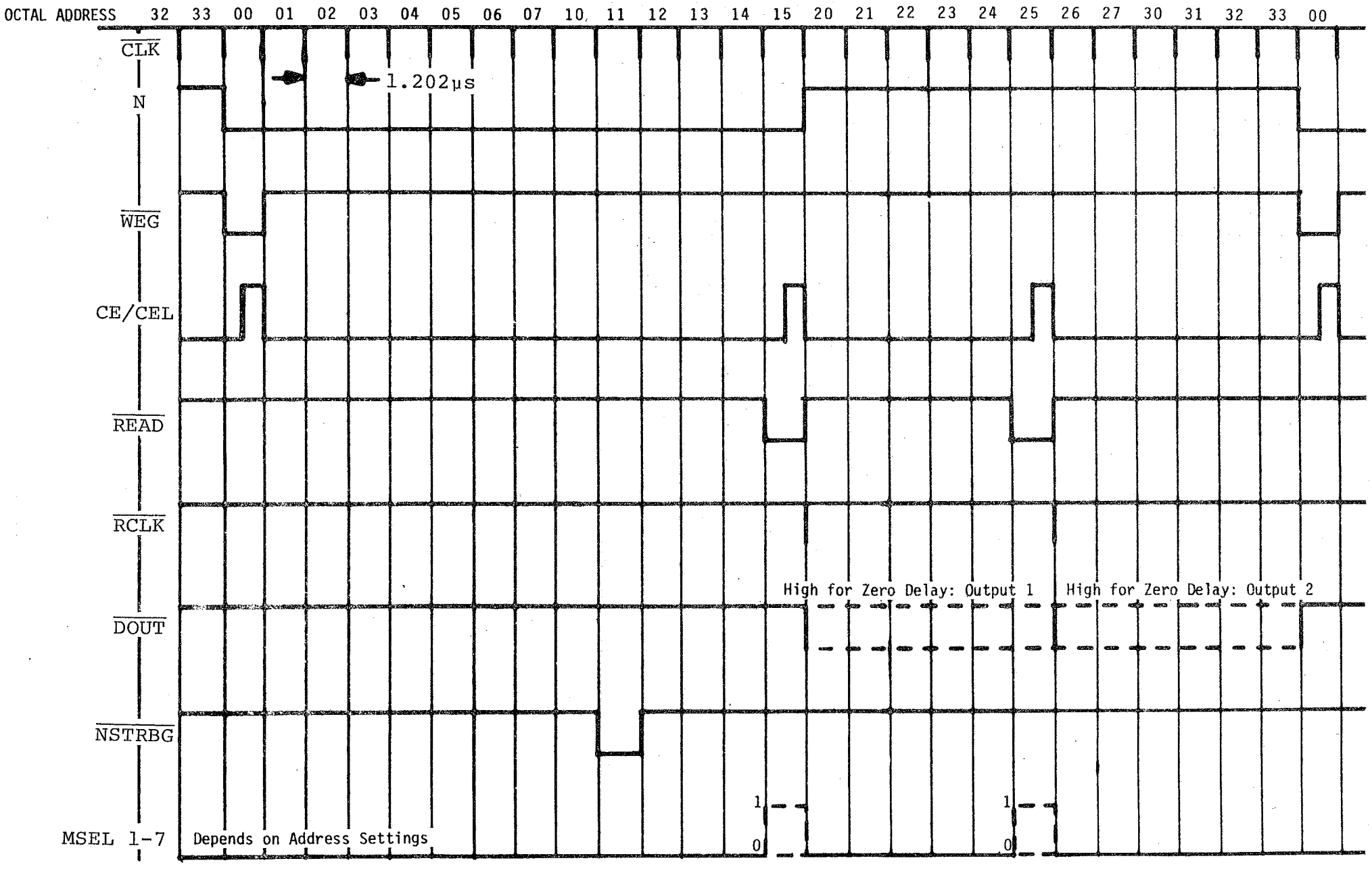


FIG. 6.3.3 MEMORY MODULE TIMING

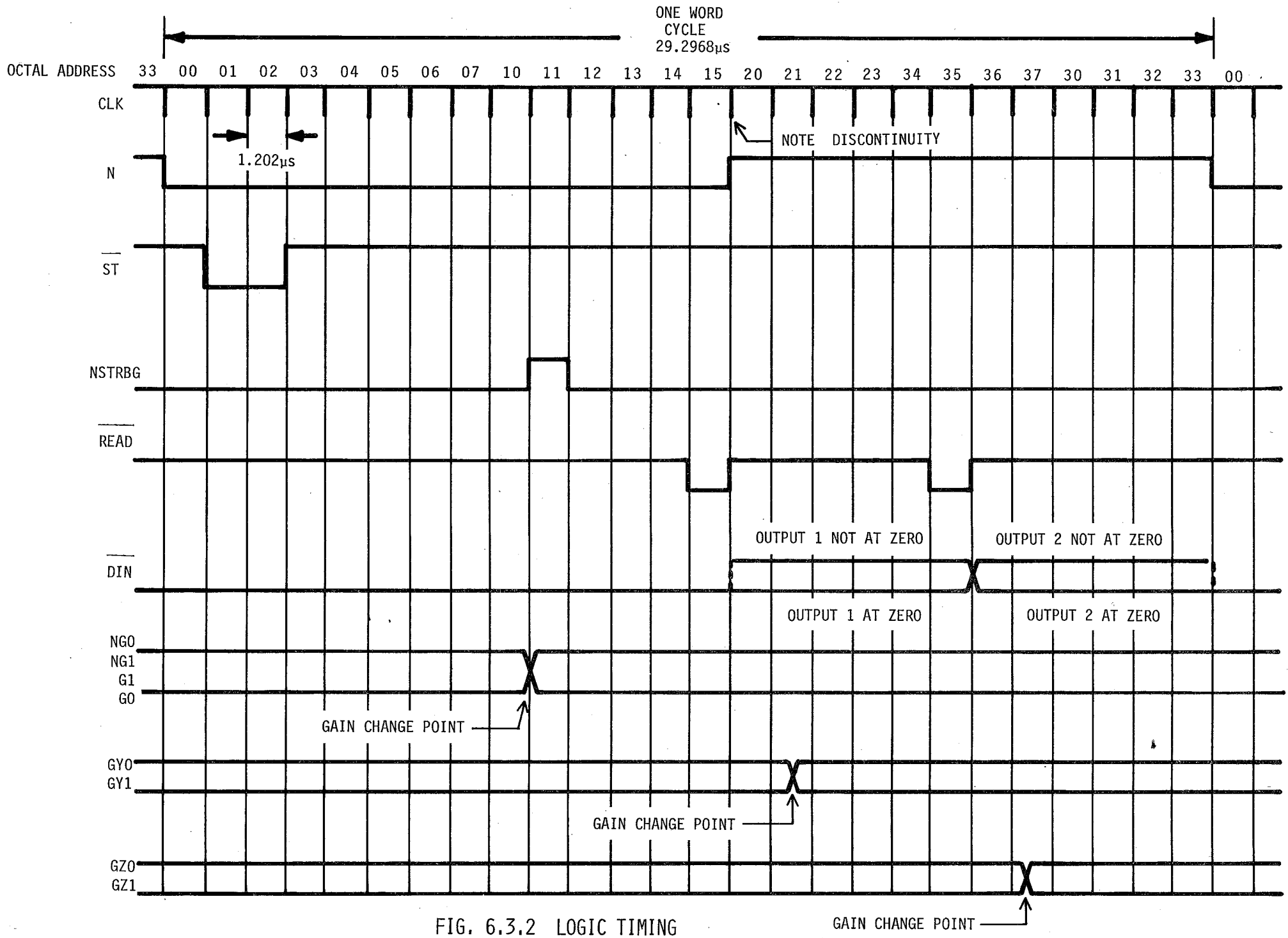
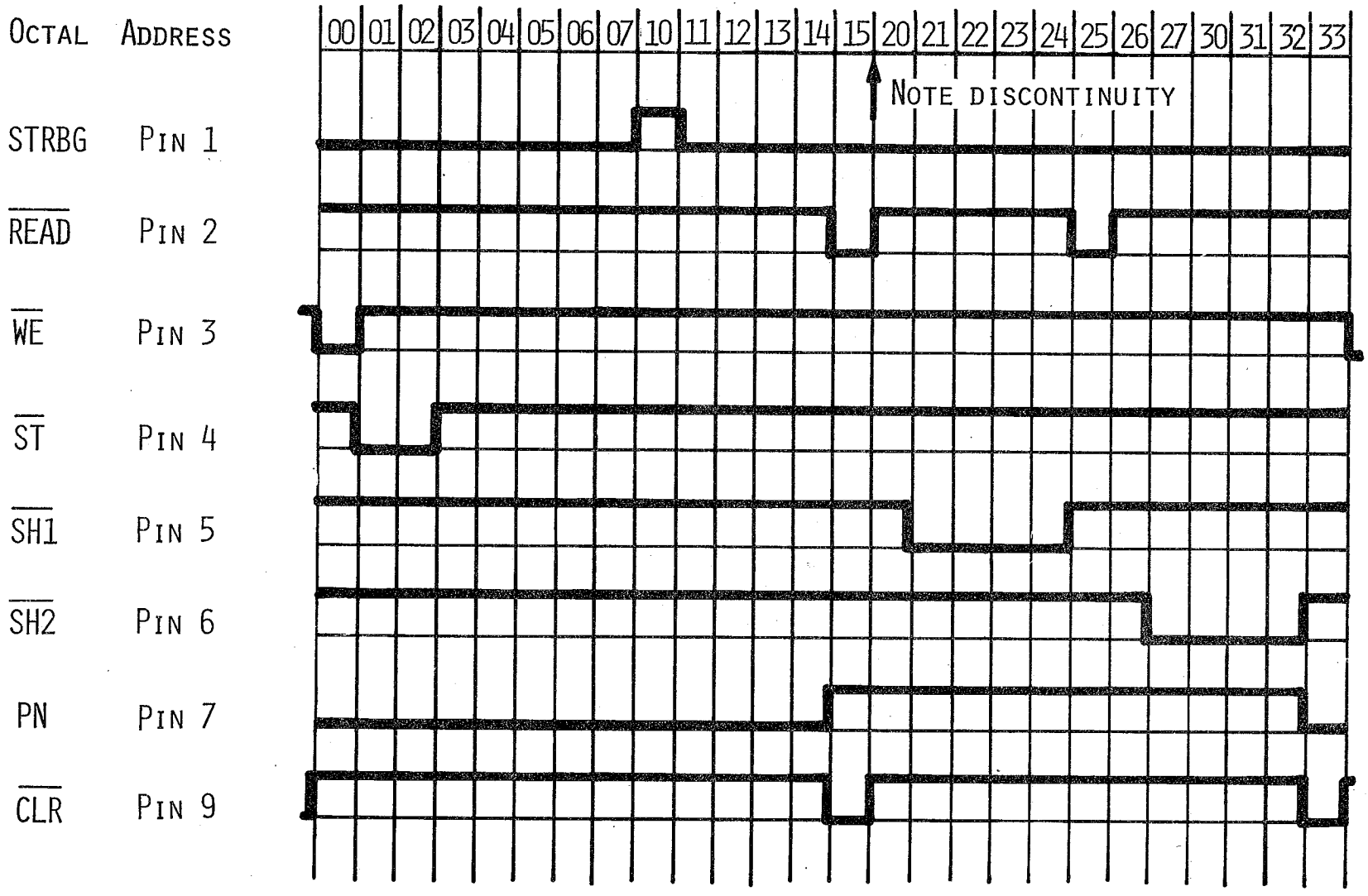


FIG. 6.3.2 LOGIC TIMING



ROM TYPE: 82S123 OR MANY EQUIVALENT TYPES

FIG. 6.3.1 CONTROL ROM TIMING

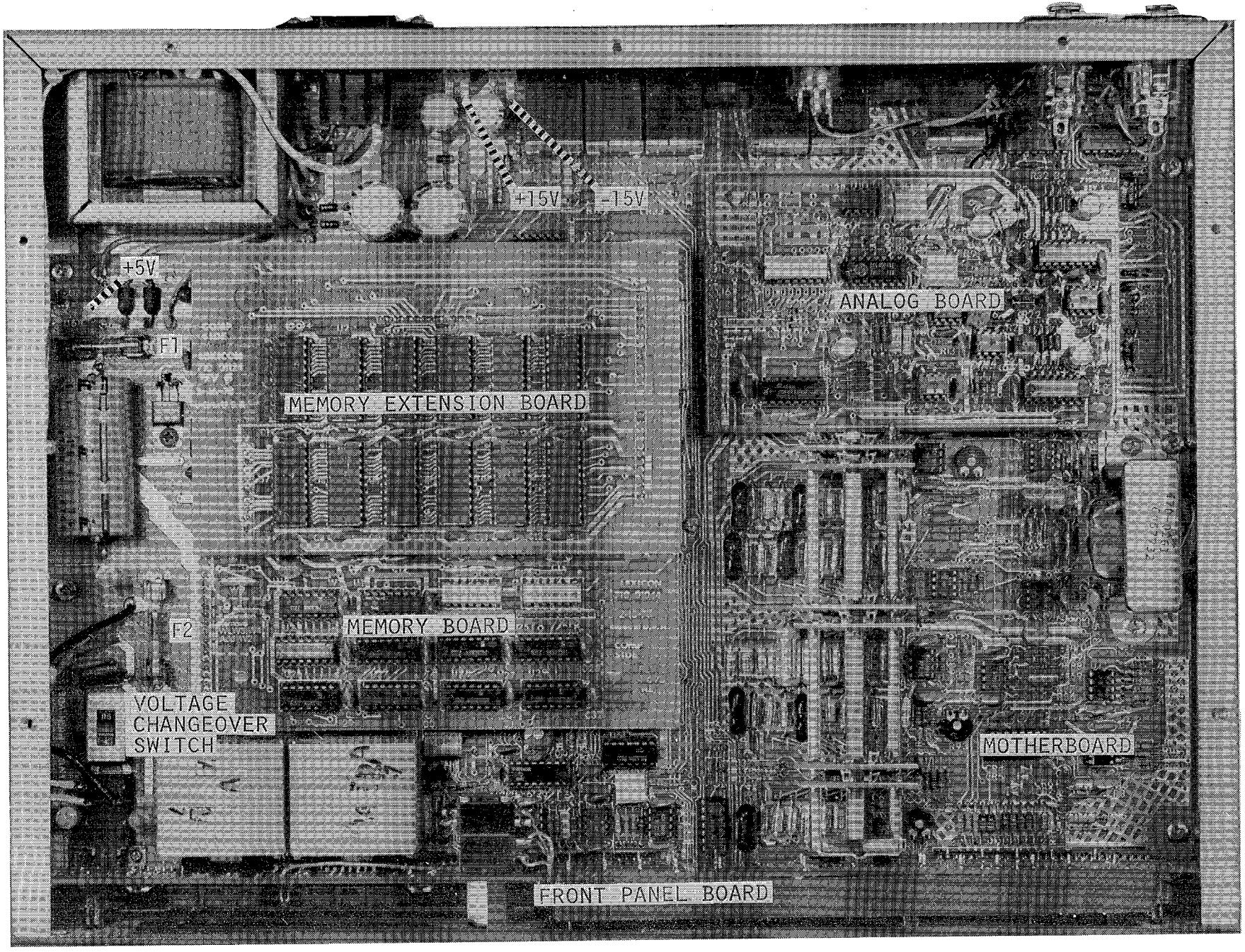
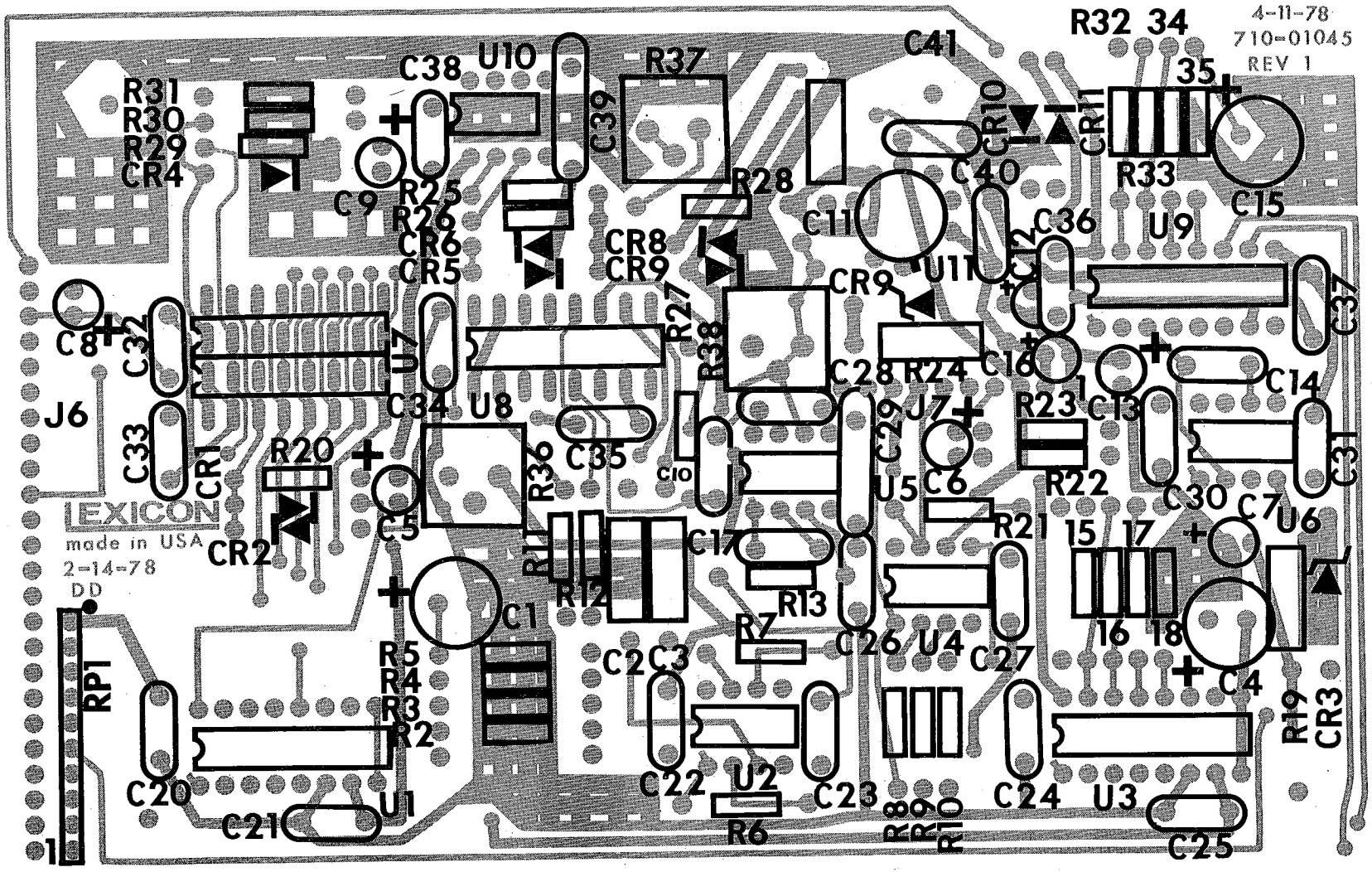


FIG. 6.0.1 INTERIOR VIEW



ANALOG
DAUGHTERBOARD LAYOUT

FIG. 6.1.2a

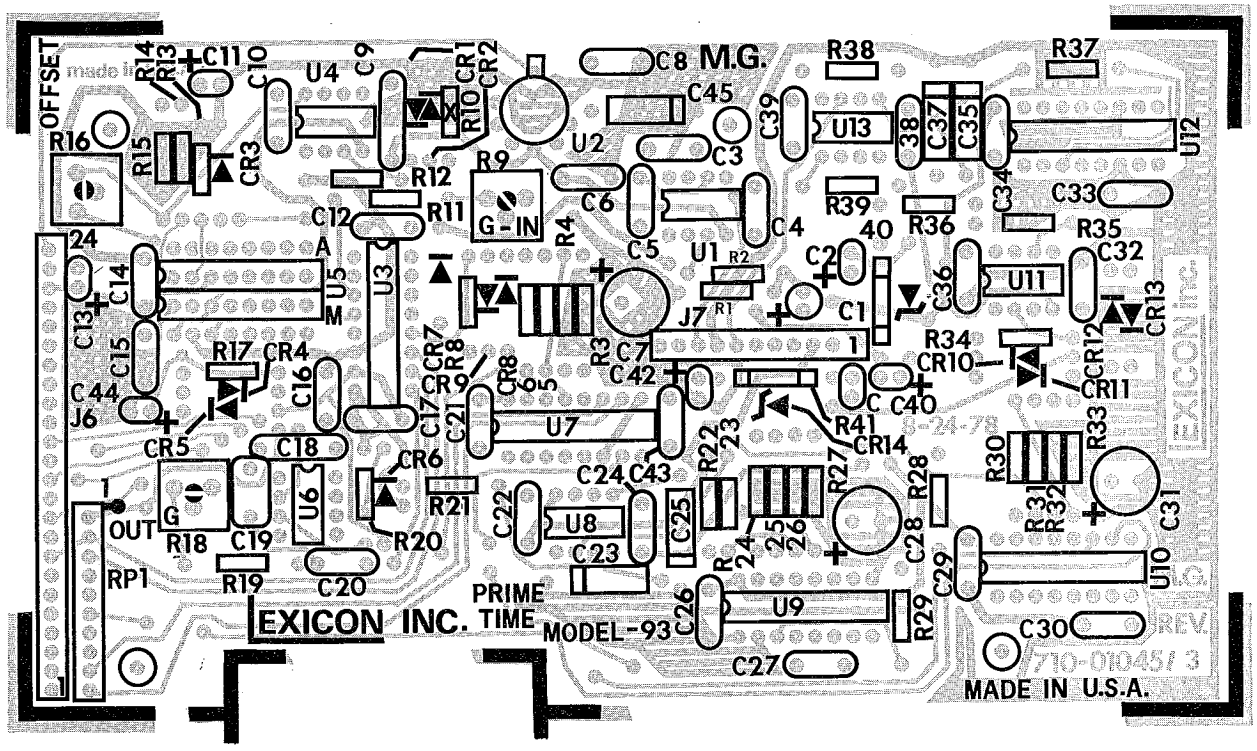
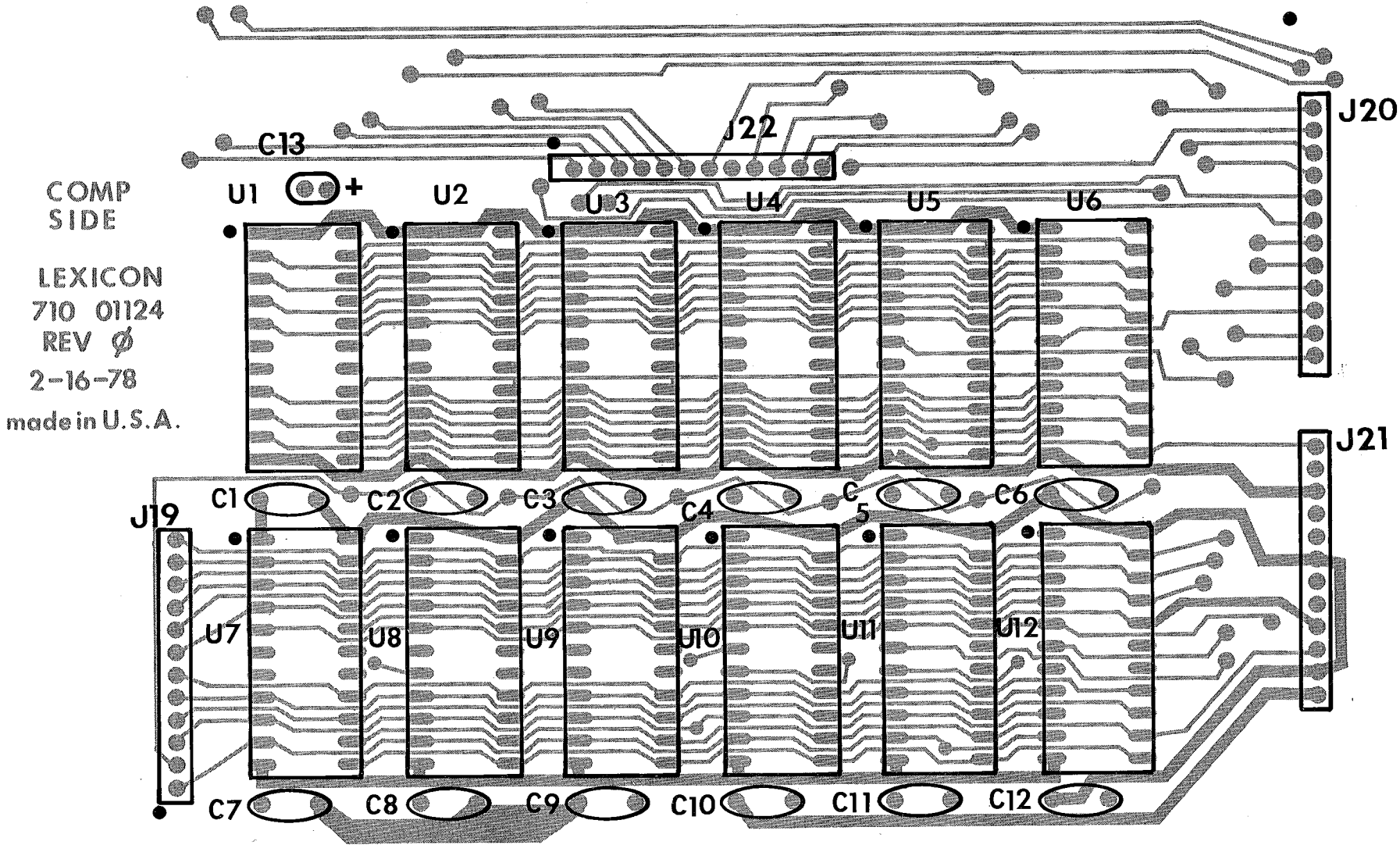


FIG. 6.1.2b ANALOG DAUGHTERBOARD/REV 3 LAYOUT



MEMORY
EXTENSION LAYOUT

FIG. 6.1.4

7.0 RETURNING UNITS FOR REPAIR

If it becomes necessary to return a module or mainframe for service, bear in mind that Lexicon assumes no responsibility for units in shipment from customer to factory, whether in or out of warranty. It is important, therefore that shipments be well packed, properly insured, and consigned to a reliable agent, such as UPS or Federal Air Express. Be sure to include (in the carton) a note explaining the nature of the problem, referencing any conversation with Lexicon personnel, detailing the preferred shipping method, and indicting a date when the unit is needed again. It is also important to provide us with the name and telephone number of a person we may contact should any questions arise.

7.1 MODULE RETURN

In the event that a defective module is clearly identified, Lexicon can usually provide a repair/exchange module in advance of receipt of the defective module. For warranty repairs, Lexicon will ship prepaid by UPS, UPS Blue Label, or US Air Mail. If faster turn-around is needed, Lexicon can ship by Federal Air Express or other expedited air service, usually resulting in 24 hour delivery if the customer is near a major airport. In the case of an expedited shipment, however, the customer is expected to pay shipping.

This service is available both for warranty and out-of-warranty repairs and in all cases of advance repair/exchange, Lexicon will invoice the customer for the card or module sent. The invoice is cancelled by issue of credit upon receipt of the defective module.

7.2 REPLACEMENT PARTS

Replacement Parts may be ordered from:

Lexicon, Inc.
60 Turner Street
Waltham, MA 02154
U.S.A.
Attn: Parts Dept.

Parts will be shipped FOB Waltham.

Price charges will be that price in effect at the time the order is received. Lexicon may be consulted at any time for a parts quotation.

When ordering parts refer to the appropriate parts list in the Model 93 Service Manual or order by complete description and give the following information.

A. Assembly - Motherboard, Analog Daughter Board, Memory, Memory Extension or Front Panel

B. Part No. and I.D. if available.

C. Item Description

D. Quantity Desired

E. Model 93 Serial No., if available

7.3 LIMITED WARRANTY

Lexicon warrants each PRIME TIME to be free from defects in material and workmanship under normal use and service for one year. This warranty begins on the date of delivery to the purchaser or his authorized agent or carrier. During the warranty period Lexicon will repair, or at its option, replace at no charge, components that prove to be defective provided the equipment is returned, shipping prepaid, to Lexicon's factory or designated service facility.

This warranty is null and void under any of the following conditions:

A. Abuse, neglect, alteration, or repair by unauthorized personnel.

B. Damage caused by improper use, or operation from an incorrect power source.

C. Damage caused by accident, act of God, war, or civil insurrection.

Lexicon shall not be responsible for any loss or damage direct or consequential resulting from machine failure or the inability of the product to perform. Lexicon shall not be responsible for any damage or loss during shipment to or from the factory or its designated service facility.

This warranty is in lieu of all other warranties, express, or implied , and of any other liabilities on Lexicon's part, and Lexicon does not assume nor authorize anyone to make any warranty or assume any liability not strictly in accordance with the above.

No equipment may be returned under this warranty without prior authorization from Lexicon. Authorized return shipments must be prepaid and should be insured. System modules being returned for repair/exchange should be wrapped or packed in soft packing material and shipped in an appropriate small protective box. In the case of returning the system mainframe, it should be carefully packed in the

original carton and packing material. If this is not available, new ones may be procured from Lexicon.

M93 MEMORY EXTENSION OPTION

PART NO.	QTY	DESCRIPTION	REF.
CERAMIC CAP			
245-00599	12	CAP,CER,.02uF,20V,80/20%	C1-12
MEMORY IC			
350-00754	12	IC,DRAM 4060 OR 2680,4K RAM	U1-12
PC MNT CONN			
510-01067	4	CONN,POST,100X025,HDR,12MCG	J4-7
SOCKETS			
520-00944	12	IC SCKT,22 PIN,PC,LO-PRO	U1-12
INSUL/SPACRS			
630-00953	8	WSHR,FL,#6CLX3/80DX1/16,FBR	MEM EXT MTG
630-01623	4	SPCR,6-32X7/16,1/4RD,PHEN	MEM EXT MTG
MACHINE SCREWS			
640-01713	8	SCRW,6-32X5/16,PNH,PH,ZN	MEM EXT MTG
PC BOARDS			
710-01124	1	PC BD,MEM EXPAN,M93	

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M93 CONNECTOR OPTIONS - CHOOSE ONE

M93 XLR CONNECTOR OPTION

PART NO.	QTY	DESCRIPTION	REF.
CABLE CONN			
490-00799	1	CONN,XLF,3MC,SDR	
490-00800	2	CONN,XLR,3FC,SDR	
MACHINE SCREWS			
640-01704	6	SCRW,4-40X5/16,FH,PH,ZN	

M93 PHONE JACK OPTION

PART NO.	QTY	DESCRIPTION	REF.
CABLE CONN			
490-01149	3	CONN,PHONE,JACK,3CF,CHASSIS	
INSUL/SPACRS			
630-00890	3	WSHR,SHLDR,1/2SHNK,3/8CL,FBR	
630-00891	3	WSHR,FL,3/8CLX5/80DX1/32,NYL	
MACHINE SCREWS			
640-01706	6	SCRW,4-40X3/8,PNH,PH,ZN	
WASHERS			
644-01737	6	WSHR,LOCK,SPLIT,#4	
PANELS			
702-01148	1	PLATE,PHONE JACK OPTION	

M93 FUSE OPTIONS - CHOOSE ONE

M93 N.AMER.FUSE OPTION(NO RFI)

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-01177	1	FUSE,3AG,FAST,.750AMP,115V	F2,PICK AND ADD TO MTHBD ASSY #022-01118
TRANSFORMERS			
470-00778	1	XFORMER,POWER,M93	PICK AND ADD TO CHAS HDWR KIT #022-01123
CABLE CONN			
490-00832	1	CONN,AC,HSG,3M,CRIMP	PICK AND ADD TO CHAS HDWR KIT #022-01123
TERM/PINS			
525-00833	3	CONN,AC,CRIMP PIN	PICK AND ADD TO CHAS HDWR KIT #022-01123

M93 N.AMER.FUSE OPTION(W/RFI)

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-01177	1	FUSE,3AG,FAST,.750AMP,115V	F2,PICK AND ADD TO MTHBD ASSY #022-01118
TRANSFORMERS			
470-00778	1	XFORMER,POWER,M93	PICK AND ADD TO CHAS HDWR KIT #022-01123
CABLE CONN			
490-00396	1	CONN,AC AND RFI FILTER	PICK AND ADD TO CHAS HDWR KIT #022-01123

M93 FUSE OPTIONS - CONTINUED

M93 EUROPEAN FUSE OPTION

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-01184	1	FUSE,3AG,FAST,.375AMP,230V	F2,PICK AND ADD TO MTHBD ASSY #022-01118
TRANSFORMERS			
470-00778	1	XFORMER,POWER,M93	PICK AND ADD TO CHAS HDWR KIT #022-01123
CABLE CONN			
490-00396	1	CONN,AC AND RFI FILTER	PICK AND ADD TO CHAS HDWR KIT #022-01123

M93 JAPANESE FUSE OPTION

PART NO.	QTY	DESCRIPTION	REF.
FUSES			
440-01177	1	FUSE,3AG,FAST,.750AMP,115V	F2,PICK AND ADD TO MTHBD ASSY #022-01118
TRANSFORMERS			
470-01243	1	XFORMER,POWER,M93(JAPAN)	PICK AND ADD TO CHAS HDWR KIT #022-01123
CABLE CONN			
490-00396	1	CONN,AC AND RFI FILTER	PICK AND ADD TO CHAS HDWR KIT #022-01123

M93 HARDWARE KIT

PART NO.	QTY	DESCRIPTION	REF.
CHASSIS/MECH (CON'T)			
700-01042	1	CHASSIS,M93	
		702-01132 PROTECTIVE SHIELD	
BRACKETS			
701-00299	8	BRACKET,KEYSTONE #617	SUPPLY TO CHASSIS VENDOR (8 QT) ADDED FOR PLANNING
PANELS			
702-00270	1	PANEL,COVER,TOP/BOTTOM,M92	
702-01033	1	PANEL,FRONT,M93	
702-01211	1	PANEL,COVER,TOP,M93	
702-01255	1	SHIELD,EPXY GL W/CU CTR,2X2.4"	
LENS/PLATE/PANL			
703-01043	1	PANEL,DISPLAY,M93	
SHIPPING MAT			
730-02820	1	BAG,CLEAR,19.5X28X.004	
730-03085	1	BOX,OUT,23X18.5X7.5	
LABEL/NAMEPLTS			
740-02253	1	LABEL,WRNG,3/4A-125V FU REPL	
740-02730	1	LABEL,FCC NON-COMPLIANCE	
740-02773	1	LABEL,CLA APPROVAL	

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M93 HARDWARE KIT

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-01060	1	MANUAL,OWNER'S,M93	
070-02813	1	CARD,WARRANTY,LEXICON	
GROMMETS			
540-01130	1	GUARD,DUST,M93	
FEET			
541-00780	4	BUMPER,FEET,3-M #SJ5023	
KNOBS/CAPS			
550-01047	3	KNOB,21MM,1/4SHFT,WING,GRY	DLY SEL
550-01048	1	KNOB,14.5MM,1/4SHFT,GRY/BLK LN	DLY ADJ
550-01049	1	KNOB,14.5MM,1/8SHFT,GRY	VCO DEPTH
550-01050	1	KNOB,21MM,1/4SHFT,GRY/BLK LN	VCO FREQUENCY
550-01051	1	KNOB CAP,21MM,RED	DLY SELECT "A"
550-01052	1	KNOB CAP,21MM,BLU	DLY MULT
550-01053	1	KNOB CAP,21MM,YEL	DLY SEL "B"
550-01054	2	KNOB CAP,14.5MM,BLU	DLY ADJUST; VCO DPH
550-01055	3	TGL CAP,GRN,ALCO C10	MAIN INPUT
550-01056	2	TGL CAP,WHT,ALCO C10	AUX INPUT
550-01057	4	TGL CAP,RED,ALCO C10	DLY "A" RECIR;OFF"A";OT MX DLY "A"
550-01058	4	TGL CAP,YEL,ALCO C10	DLY "B" RECIR;OFF"B";OT MX DLY "B"
550-01059	3	TGL CAP,BLU,ALCO C10	MASTERS
550-01117	1	PB CAP,BLU,C&K 7089	(FOR SW1)
550-01207	1	KNOB,14.5MM,NUT CVR,GRY/BLK LN	DLY ADJUST
LUGS			
620-01999	1	LUG,SOLDER,LCKNG,11/16,.020TH	GRNDING LUG
INSUL/SPACRS			
630-00889	3	INSUL,SEMI,MICA,TO-220	REG MTG
630-00890	6	WSHR,SHLDR,1/2SHNK,3/BCL,FBR	PHONE JACK MTG
630-00891	8	WSHR,FL,3/8CLX5/80DX1/32,NYL	PHONE JACK MTG
630-00952	3	INSUL,SEMI,BUSHING,TO-220	REG MTG
630-00953	16	WSHR,FL,#6CLX3/80DX1/16,FBR	MEM MTG,ANLG DAUGHTER MTG
630-01623	8	SPCR,6-32X7/16,1/4RD,PHEN	MEM MTG,ANLG DAUGHTER MTG
SPCR,NON-INSUL			
635-01224	1	BUSHING EXTENDER,3/8-32X5/8	FP BD MTG
MACHINE SCREWS			
640-01706	5	SCRW,4-40X3/8,PNH,PH,ZN	REG MTG,A/C CONN MTG

M93 HARDWARE KIT

PART NO.	QTY	DESCRIPTION	REF.
MACHINE SCREWS (CON'T)			
640-01710	26	SCRW,6-32X1/4,PNH,PH,ZN	MOTHERBD MTG,FP BRACK MTG FP BD MTG
640-01713	17	SCRW,6-32X5/16,PNH,PH,ZN	MEM MTG,ANLG DAUGHTER MTG GRND LUG
640-01721	2	SCRW,8-32X3/8,PNH,PH,ZN	PWR XFORMER MTG
640-01800	4	SCRW,6-32X1/4,FH SCKT,BLK	FP MTG
NUTS			
643-01179	2	NUT,3/8-32,SHLDR,BRASS/NI	FP BD MTG
643-01725	9	NUT,3/8-32,HEX,BRASS/NI	FP MTG
643-01729	1	NUT,6-32,HEX,SMALL,ZN	GRND LUG MTG
643-01733	3	NUT,4-40,HEX,SMALL,ZN	REG MTG
643-01734	2	NUT,8-32,KEP,ZN	PWR XFORMER MTG
WASHERS			
644-01253	2	WSHR,INT STAR,3/8CLX.500DX.016	FP,FP BD
644-01736	2	WSHR,FL,#4CLX.218ODX.032THK	A/C CONN MTG
644-01737	3	WSHR,LOCK,SPLIT,#4	REG MTG
644-01739	23	WSHR,INT STAR,#6	GRND LUG MTG,MOTHERBD MTG FP BD MTG
BULK WIRE			
670-01683	18	WIRE,18AWG,16/30,WHT	CUT ONE 18" LENGTH
670-01684	16	WIRE,18AWG,16/30,BLK	CUT ONE 16" LENGTH
670-01694	4	WIRE,24AWG,7/32,BRN	OUTPUT XLR WIRING CUT ONE 4" LENGTH
670-01695	4	WIRE,24AWG,7/32,RED	OUTPUT XLR WIRING CUT ONE 4" LENGTH
670-01696	4	WIRE,24AWG,7/32,ORN	OUTPUT XLR WIRING CUT ONE 4" LENGTH
PRE-CUT WIRE			
675-02881	2	WIRE,24G,BRN,3",ST&T1/4X1/4	INPUT XLR WIRING
675-02882	2	WIRE,24G,RED,3",ST&T1/4X1/4	INPUT XLR WIRING
675-02883	2	WIRE,24G,ORN,3",ST&T1/4X1/4	INPUT XLR WIRING
CABLES/CORDS			
680-00841	1	CORD,POWER,PHILLIP #13E37-1	
SLEEVING			
690-02060	5	SLEEVING,SHRINK,3/16"	AC CONN,1/2" LENGTHS
CHASSIS/MECH			
700-00094	2	BRACKET,FP,PRO BLACK BOX	

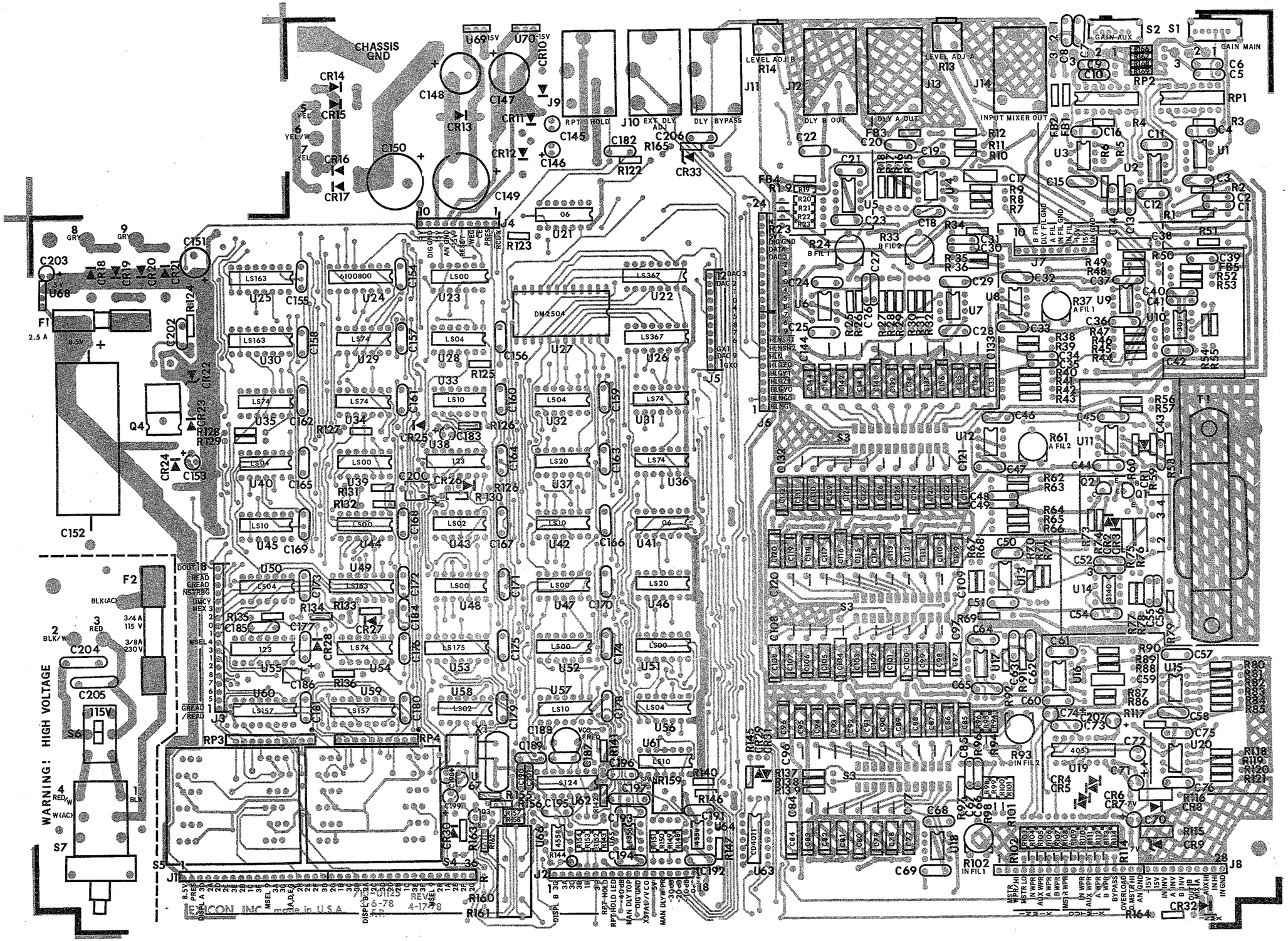
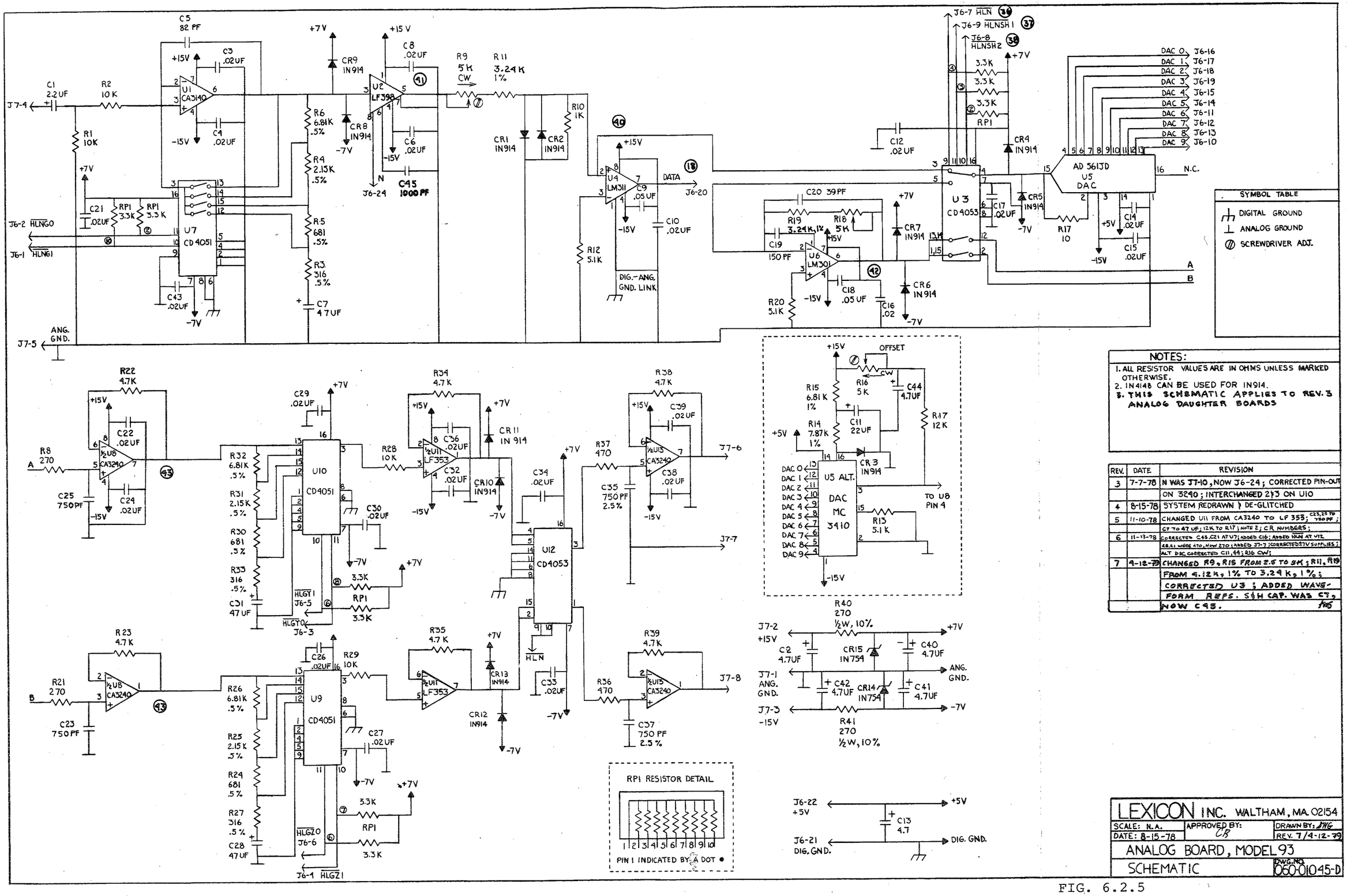


FIG. 6.1.1 MOTHERBOARD LAYOUT



REV.	DATE	REVISION
3	7-7-78	N WAS J7-10, NOW J6-24; CORRECTED PIN-OUT
		ON 3240; INTERCHANGED 2 & 3 ON U10
4	8-15-78	SYSTEM REDRAWN & DE-GLITCHED
5	11-10-78	CHANGED U11 FROM CA3240 TO LF 353; C23,25 TO 750 PF; C7 TO 47 UF; 12K TO R17; NOTE 2; CR NUMBERS;
6	11-13-78	CORRECTED C45, C21 AT U7; ADDED C16; ADDED HLN AT U12; R8,21 WERE 470, NOW 270; ADDED J7-7; CORRECTED -7V SUPPLIES; ALT DAC CORRECTED C11, 44; R16 CW;
7	4-12-79	CHANGED R9, R16 FROM 2.5 TO 5K; R11, R19 FROM 4.12K, 1% TO 3.24K, 1%; CORRECTED U3; ADDED WAVEFORM REFS. S&H CAP. WAS C7, NOW C45.

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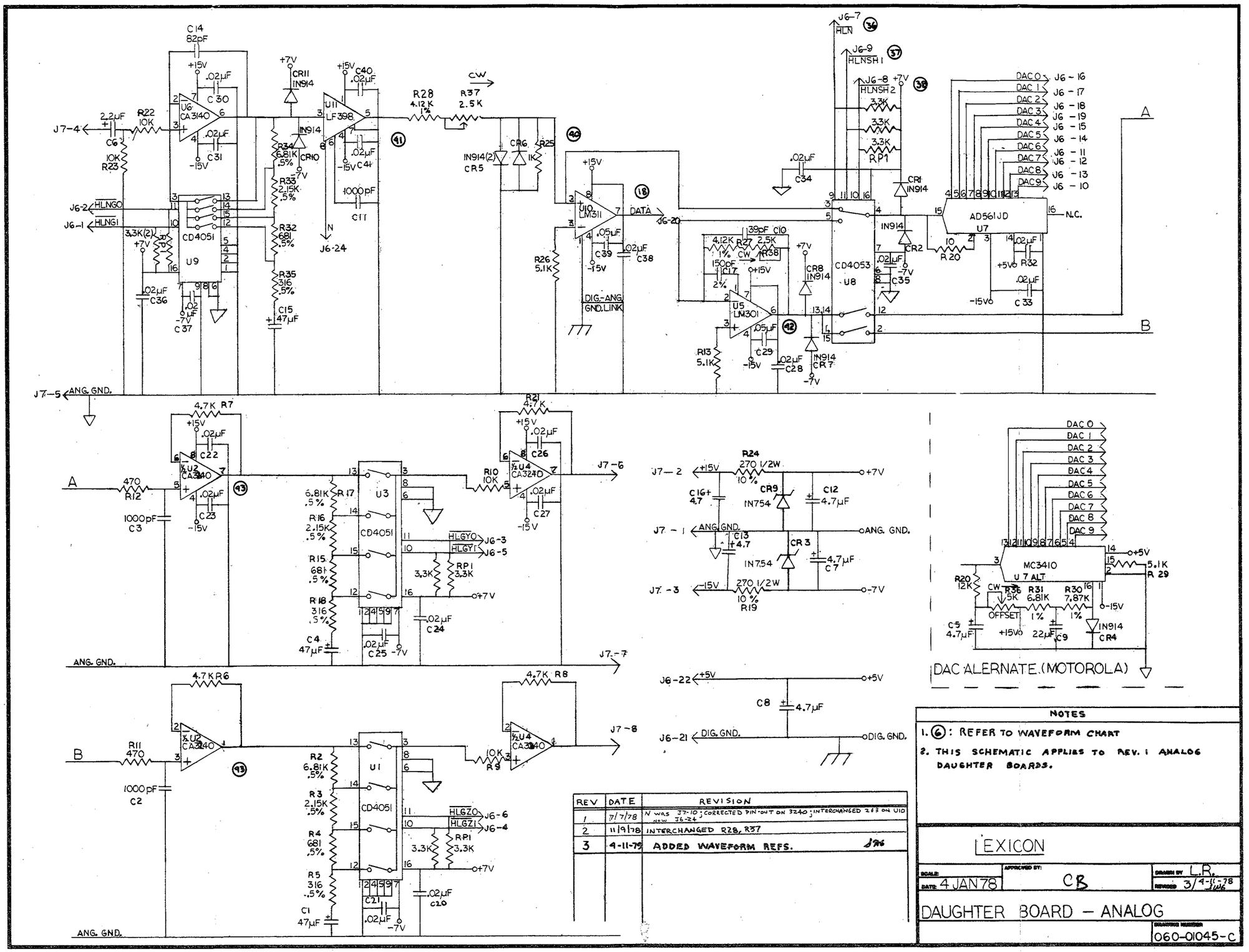
SCALE: N.A.	APPROVED BY: CB	DRAWN BY: PMG
DATE: 8-15-78		REV. 7/4-12-79

ANALOG BOARD, MODEL 93

SCHEMATIC — DWG. NO. 060-01045-D

FIG. 6.2.5
ANALOG DAUGHTERBOARD/ REV 3 SCHEMATIC



REV	DATE	REVISION
1	7/7/78	N WAS J7-10; CORRECTED PIN-OUT ON 3240; INTERCHANGED 2&3 ON U10 NOW J6-24
2	11/9/78	INTERCHANGED R28, R37
3	4-11-79	ADDED WAVEFORM REFS. JPG

NOTES

1. (6): REFER TO WAVEFORM CHART
2. THIS SCHEMATIC APPLIES TO REV. 1 ANALOG DAUGHTER BOARDS.

LEXICON

SCALE:	APPROVED BY:	DRAWN BY
DATE 4 JAN 78	CB	L.R.
		REVISED 3/4-11-78 JPG

DAUGHTER BOARD – ANALOG

DRAWING NUMBER 060-01045-C

FIG. 6.2.4
ANALOG DAUGHTERBOARD/REV 1 SCHEMATIC

P/S

REV.	DATE	REVISION
1	11/9/78	LABELED R161
2	11/15/78	ADDED GND U67; R149, C204; U70 CASE; CR13
3	11/14/78	INTERCHANGED C149, 150 ; ADDED CR21
4	12/14/78	U67 WAS 78L05; NOW LM309
5	9-12-79	ADDED: NOTE 1, WAVEFORM REFS., PINS 4&8 TO U66; DELETED: 10V REFS., CONN. BETWEEN CR30 AND DELAY ADJUST GND.; SWAPPED LOCATIONS OF C189 & XTAL; SWAPPED PINS 12 & 13 OF U62. JW
6	8-29-80	DELETE C189, C190, RELOCATE XTAL; DELETE R141, 142, 143; C151 WAS 470 uF, NOW 22 uF; CORRECT CONN'S AT CR16, F1.
7	12-29-81	U65 WAS LF156, NOW LF356. JW

NOTES

1. LM309 FOOTPRINT BOTTOM VIEW : INPUT, OUTPUT, GND (CASE)

SYMBOL TABLE

- (6) REFER TO WAVEFORM CHART
- SCREWDRIVER ADJ.
- DIGITAL GROUND
- ANALOG GROUND

EXICON INC. WALTHAM MA 02154

SCALE N.A.	APPROVED BY:	DRAWN BY JWG
DATE: 8-14-78		REV. 7 : 12-29-81

MOTHER BOARD, MODEL 93
SCHEMATIC PART 3
DWG NO. 060-01095

FIG. 6.2.3 MOTHERBOARD SCHEMATIC, PART 3

DISPLAY A

DISPLAY B

HIGHEST NUMBERED COMPONENTS

R24
C7
CR8
Q2
U2
RP7
D3A
D3B
S6

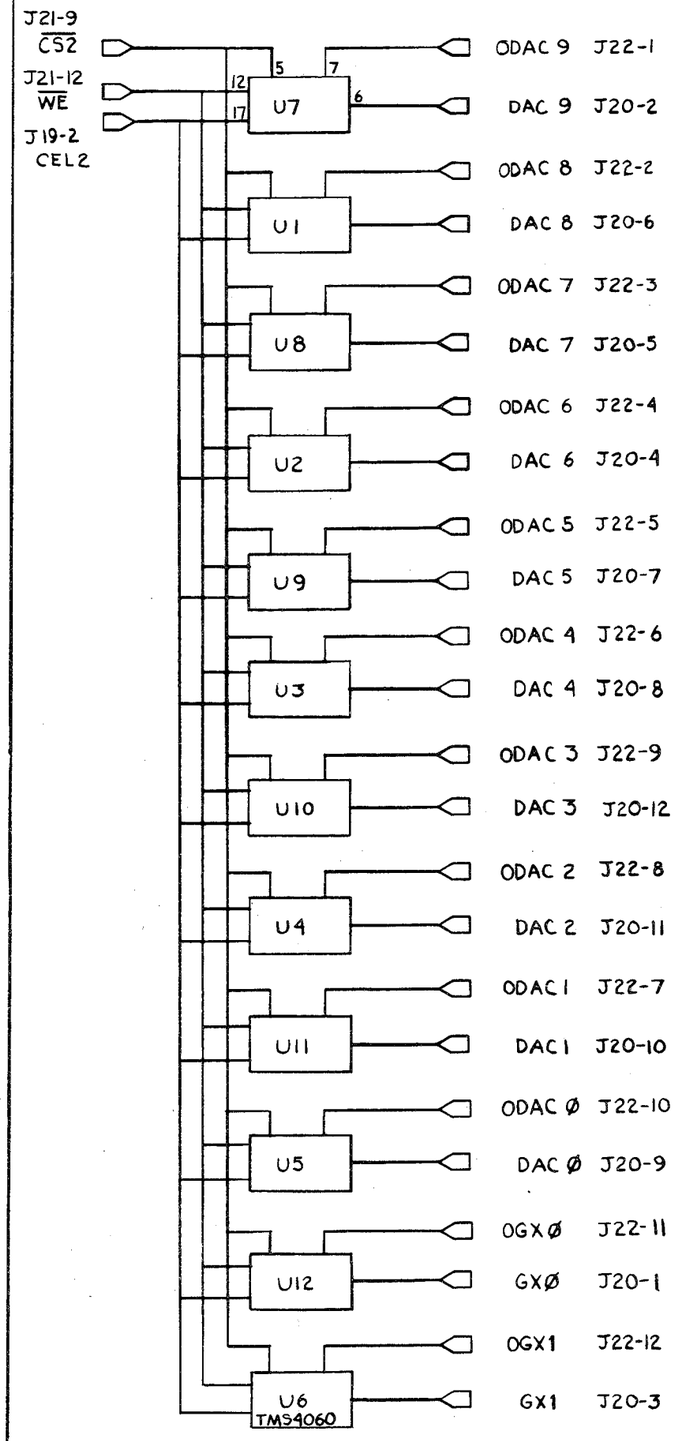
REV	DATE	REVISION
1	11/9/78	R3 WAS 150; NOW 470 ; R24 WAS 1K, NOW 1.5K ½W ; J1, J2 LABELED

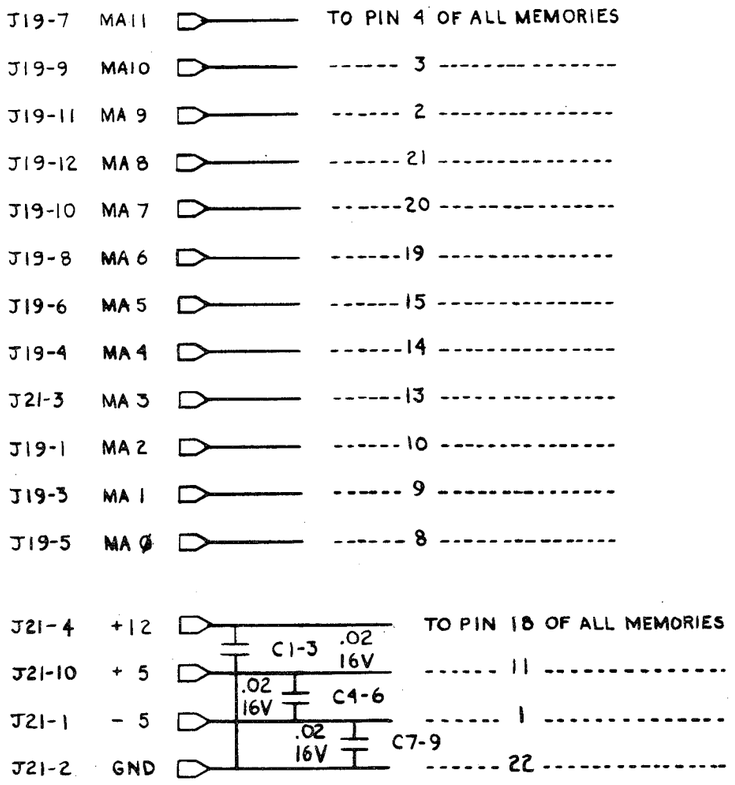
SCALE:	APPROVED BY: CB	DRAWN BY LR
DATE: 28 MAR78		REVISED 1

PRIME TIME FRONT PANEL BOARD

DRAWING NUMBER 060-01102

FIG. 6.2.8 FRONT PANEL BOARD SCHEMATIC





REV. #	DATE	REVISION	INIT.
1	8/18/78	REDRAWN	JMS
2	8/29/78	CHANGED J21-3 TO J21-4; J21-11 TO J19-2; GXØ TO GX-1; GX-1 TO GX-Ø; J19-2 TO J21-3	DR
3	4/24/79	DWG. TITLE WAS MEMORY MODULE, NOW MEMORY EXTENSION SCHEMATIC; DWG. NO. WAS 760-01044, NOW 060-01044	

EXICON INC. WALTHAM, MA 02154			
SCALE: NA	APPROVED BY: C.B.		DRAWN BY JTG
DATE: 8-18-78			REV. 3
MEMORY EXTENSION SCHEM.			
MODEL 93			060-01044

FIG. 6.2.7 MEMORY EXTENSION SCHEMATIC

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1	REDRAWN JM6	1-11-79	
2	CORRECTED PINS 2,11 ON U25; ADDED WAVEFORM REFS.	9-12-79 JM6	
3	U19 WAS 74LS00, NOW 74LS10; ADD R4 & C34; CHANGE CAP. REF. NO'S.	11-28-79 JM6	
4	U19 WAS 74LS10, NOW 74LS132. ADD NOTE 10.	8-21-80	

TYPICAL CONNECTIONS 12 POSITIONS
RAM PIN 6 TO DATA BUS

NOTES

1. CONNECTION TO MOTHER BOARD
2. CONNECTION TO PIGGY-BACK BOARD
3. ANALOG GND.
4. DIGITAL GND.
5. MEMORIES ARE TMS4060 OR EQUIV.
6. MEMORY ADDRESS LINES AND POWER SUPPLY LINES GO TO INDICATED PIN ON ALL MEMORIES
7. RP1, RP2 ARE 3.3K X 9 NETWORKS 10 PIN SIP
8. RP3, RP4 ARE 68Ω X 7 NETWORKS 14 PIN DIP LDP-14-01-68-K
9. BY-PASS CAPACITORS:
   C6, C9, C12, C15 TO +12V
   C5, C8, C11, C14, C19-C32 TO +5V
   C4, C7, C10, C13 TO -5V
10. SCHEMATIC REV'S 3&4 APPLY TO PC BOARD REV 2 & ABOVE ONLY.

SYMBOL TABLE

- DIGITAL GND
- ANALOG GND
- (5) REFER TO WAVEFORM CHART

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

	MODEL 93		
NEXT ASSY	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
XX NA
.XXX NA
MATERIAL NA
FINISH NA
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN JM6	1-11-79
CHECKED	
ISSUED	

lexicon

MEMORY, MODULE (MAIN)

SIZE | FSCM NO. | DWG. NO. 060-01083-D | REV. 4

SCALE | SHEET 1 OF 1

FIG. 6.2.6 MEMORY BOARD SCHEMATIC

REV.	DATE	REVISIONS
2	6-17-78	RP3,4 PINOUT ADDED TO SCHEMATICS.
3	6-18-78	REDRAWN + RELEASED.
4	11-10-78	CORRECTED U49,SW 3, U53, U43, U52, U21, U55, U46, U25
5	4-11-79	CORRECTED RP3,4 ; ADDED WAVEFORM REFERENCES
6	5-4-79	ADDED 82 pF, 10%, 1000V CAP. ACROSS NSTRBG (U25)
7	9-20-79	DELETED CR25
8	8-29-80	R126 WAS 17K, NOW 18K ; R139 WAS 13.3K, NOW 3.3 K
9	12-29-81	ADD NOTE 5. ADD DESTINATIONS ON "N" SIGNAL. ADD CAP AT PIN 9 OF U55.

NOTES
1. ALL RESISTOR VALUES ARE IN OHMS UNLESS MARKED OTHERWISE.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS MARKED OTHERWISE.
3. DELAY SWITCHES SW4,5 SHOWN IN 256MS POSITION
4. ALL RESISTORS ARE 5% CF TOL.
5. U29: ONLY TI IS APP'V'D FOR 74LS74

CYCLE CONTROL

INPUT GAIN CONTROL

DELAY SELECTION LOGIC

AD CONTROL

DUMMY CYCLE MEMORY REFRESH COUNTER

OUTPUT GAIN REGISTER

DELAY MULTIPLY

DISPLAY CONTROL

REPEAT HOLD LOGIC

SYMBOL TABLE
- DIGITAL GND
- TEST POINT
- (5) REFER TO WAVE FORM CHART
- +5V SUPPLY VOLTAGE BUSS CONNECT.
- CONNECTOR FEM.

EXICON Inc., Waltham, MA. 02154

SCALE: N.A.	APPROVED BY: C.B.	DWG. BY: TMG.
DATE: 7-18-78		REV.9: 12/29/81

MOTHER BOARD, MODEL 93

SCHEMATICS, PART-2 — DWG.NO. 060-01095

FIG. 6.2.2 MOTHERBOARD SCHEMATIC, PART 2

INPUT
J15
AUX INPUT
J16
0dB 20dB
GAIN SWITCHES: S1, S2
ROLLOFF A
FROM DLY A
ROLLOFF B
FROM DLY B
DLY A
DLY B
FROM DELAY BYPASS SWITCH
IN
AUX
RP 1,2
1 2 3 4 5 6 7 8
S3 SECTION TYP.
4X⊖ CW 1X⊖
4X⊖ 2X⊖
17 PLACES
CAPACITOR ARRAY TYP.
510Ω 1200Ω 750Ω 750Ω 1pF 2.5%
15 PLACES
INPUT MIX MASTER
LOW PASS FILTER
DEEMPHASIS
LOW PASS FILTER
INVERT IN
AUX
TO ROLLOFF A DLY A
TO ROLLOFF B DLY B
OUTPUT MIX MASTER
DELAY BYPASS
J11 EXTERNAL DELAY BYPASS
PREEMPHASIS
APERTURE CORRECTION
J7-4
J7-5
J7-6
J7-7
J7-8
J14 INPUT MIXER OUT
REV.1,2 MOTHERBOARDS, U10=LM301A AND POINT A IS CONNECTED TO POINT B. REV.3-CURRENT MOTHERBOARDS, U10=4558 AS SHOWN IN INSET→
OVERLOAD
J16
MASTER OUTPUT J17
J13 DELAY A OUT
J12 DELAY B OUT
LEVEL ADJUST A
LEVEL ADJUST B
+47V
AN GND
-7V

NOTES

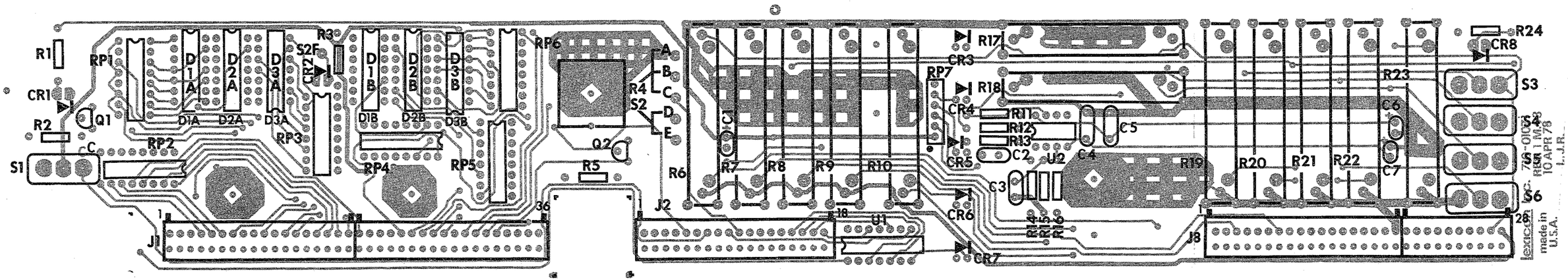
1. COMPONENTS WITHIN DOTTED LINES APPEAR ON FRONT PANEL BOARD.
2. U1-U5,U9,U13 ARE LF353. (CONT. NOTE 6)
3. CR32 LED:HP NO. 5082-4850
4. CAPACITOR VALUES IN μF UNLESS OTHERWISE MARKED.
5. RESISTOR VALUES IN Ω.
6. ALL OTHER OP AMPS ARE 4558 UNLESS OTHERWISE SPECIFIED.

REV	DATE	REVISION DATA
1	7-31-78	REDRAWN
2	8-31-78	R101, 41, 29 FROM 20K TO 17.4K; R96, 65, 31 FROM 4.12K TO 5.23K; R100, 42, 28 " 9.53K " 12.4K; R94, 62, 36 " 15.8 K " 15.4K; R99, 38, 25 " 15K " 12.7K; R69, 66, 32 " 9.53K " 8.06K; R95, 43, 30 " 22.1K " 19.1K; R73, 74 " 3.3 K " 1.6K; R58 " 47K " 270K; R56 " 18K " 13K; C72, 74 " 4.7 " 22; U14 FROM CA3140 TO LF356N; Q1 FROM TIP31A TO MJE180; Q2 FROM TIP32A TO MJE170
3	11-14-78	CHANGED DOCUMENT NUMBER: WAS 060-01039, NOW 060-01095
4	4-12-79	CHANGED R102 TO R108; DELETED C53; ALTERED U10 (SEE INSET).
5	8-29-80	R165 WAS 510, NOW 51; LABEL 5.6K RES. "R105". SG.
6	6-26-81	U1-5, U9, U13 WERE 4558 NOW LF353. SG.
7	10-16-81	C43 WAS .05/50, NOW .1, 5%; R59 WAS 1M, NOW 470K.
8	12-29-81	R106, 107 WERE 24K, NOW 22K; R104, 105 WERE 5.6K, NOW 4.3K.

EXICON INC. WALTHAM, MA. 02154

SCALE: N.A. DATE: 7-31-78	APPROVED BY: CB.	DRAWN: LJR REV: 8
MOTHERBOARD: ANALOG		M.93
PART 1		DWG. NO. 060-01095

FIG. 6.2.1 MOTHERBOARD SCHEMATIC, PART 1



FRONT
PANEL BOARD LAYOUT

FIG. 6.1.5

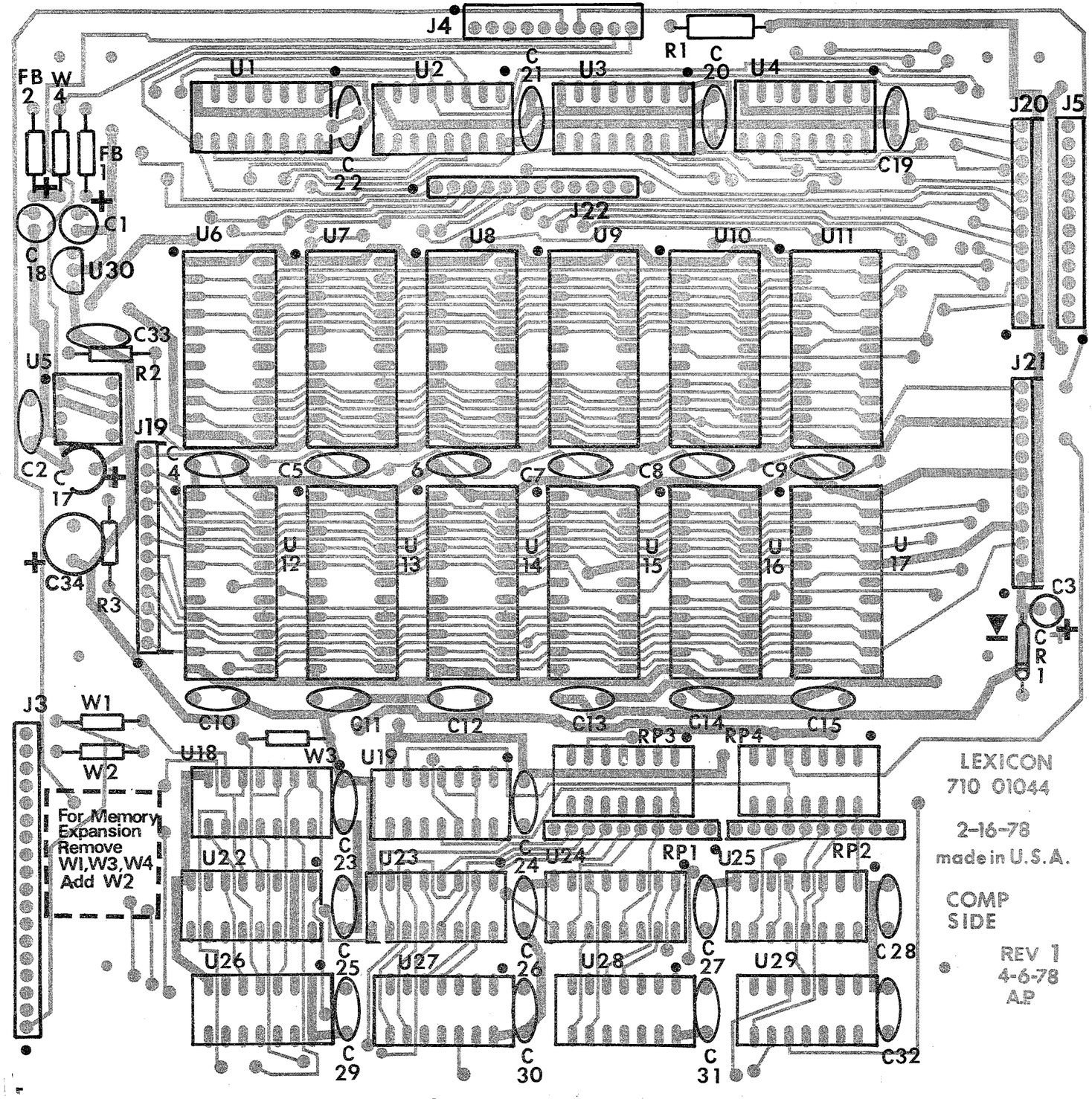


FIG. 6.1.3 MEMORYBOARD LAYOUT