Service Manual

LXP-1

Digital Effects Processor

Lexicon

Precautions

The LXP-1 is a rugged device with extensive electronic protection. However, you should observe the same reasonable precautions that apply to any piece of audio equipment:

- Always use the correct line voltage and power pack.
- Don't install the LXP-1 in a closed, unventilated rack, or directly above heat-producing equipment such as power amplifiers.
- Never attach audio power amplifier outputs (speaker outputs) directly to any of the LXP-1's connectors.
- To prevent fire or shock hazard, do not expose the LXP-1 to rain or moisture.

FCC Notice

Class A Computing Device

This equipment generates, uses, and can radiate radio frequency energy. If not installed and used in accordance with the instruction manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J, Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area may cause interference, in which case the user at his/her own expense will be required to take whatever measures are needed to correct the interference.

The Federal Communications has prepared a booklet which you may find useful:

"How to Identify and Resolve Radio-TV Interference Problems"

This booklet is available from the US Government Printing Office, Washington, DC 20402, Stock No. 004-000-0345-4.

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LXP-1
Service Manual
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1

Controls and Connectors

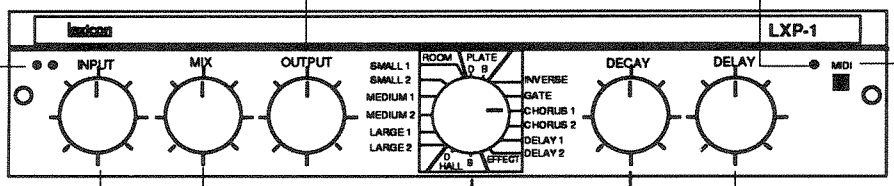
Front Panel

Level Indicators.
The left LED indicates signal present; the right flashes red when the signal is -3 dB from peak overload.

OUTPUT.
Controls the signal level sent to the LXP-1's outputs.

MEM LED.
Flashes to indicate that the system is under external control. Used also to indicate results of diagnostic tests or performance of internal memory functions.

MIDI button and status indicator.
The MIDI button is used with an external MIDI device to select a MIDI channel, store registers and learn patches. The status indicator confirms that power is on, and blinks at different rates to inform you of the LXP-1's status.



INPUT.
Sets the audio input level.

MIX.
Controls the ratio of dry (source) vs. wet (effect) signal present at the LXP-1 outputs. Turn the control all the way to the left for 100% dry, 0% wet. Straight up is 50% dry, 50% wet. All the way to the right is 0% dry, 100% effect.

Program Selector. Selects any one of sixteen preset programs for immediate use. 128 user registers can also be stored and recalled via MIDI.

Parameter Controls. Allow adjustment of two variable parameters in the currently running preset program or register.

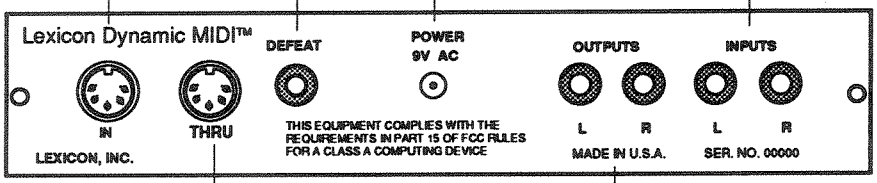
Rear Panel

MIDI IN.
Receives MIDI information from other MIDI equipment, such as master keyboard controllers, MIDI foot controllers, sequencers, and synthesizers.

DEFEAT.
Connect a push-on/push-off (toggle) footswitch here to turn effects on and off .

POWER.
Accepts power from the supplied power pack.

INPUTS (L and R).
Single-ended (unbalanced) inputs accept levels from -20 to +15 dBV. Input impedance is 50 kilohms in stereo, and 25 kilohms in mono.



MIDI THRU.
Any data received at the MIDI IN connector is sent here without change. An internal jumper can be set to change this into a MIDI OUT connector.

OUTPUTS (L and R).
Single-ended (unbalanced) stereo outputs provide up to +4dBV output into 600 ohms.

Power

Connect the LXP-1 power pack to an appropriate AC wall socket, and the cable end to the LXP-1 power connector. The LXP-1 must be used only with the supplied power pack. Voltage requirements are printed on the power pack. The LXP-1 has no power switch—it can be left on all the time. To keep the power plug from working loose from the rear of the unit during travel, you may wish to apply a small amount of silicone sealer to the plug after inserting it.

Periodic Maintenance

Under normal conditions the LXP-1 requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and a mild detergent to clean the exterior surfaces of the unit. **Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners.** Avoid using abrasive materials such as steel wool or metal polish. If the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the LXP-1 exterior.

2

Performance Verification

Performance Verification

Inspect the unit for any obvious signs of physical damage. Verify that all pots, the MIDI momentary push button and the 16-position rotary switches operate smoothly and correctly.

Verify that all screws and rear panel jacks are secure.

Inspect the external AC power transformer for any signs of physical damage. Make sure that it is rated for 9VAC at 2 Amps and that the proper 5mm/ 2.5mm barrel connector is attatched.

Front Panel Diagnostics

Power on the LXP-1 while pressing the MIDI button on the front panel of the unit. When the MIDI button is released, the LXP-1 will enter Diagnostic Mode and will be awaiting the selection of a diagnostic test.

Diagnostic test programs are selected by adjusting the Program Select knob (the third knob from the right on the front panel) to one of its 15 assigned positions, then pressing and releasing the MIDI button. As the MIDI button is released, the selected test is initiated.

Generally, the test action is performed once and the results are displayed immediately. In the case of tests marked by an asterisk (*) the action is performed continuously; the results are displayed when the MIDI button is pressed and released.

If the selected test is successful, the red MEM LED (located on the far right side of the front panel) will flash at a rate of approximately 6 Hz. If the test fails, the MEM LED and the OVLD LED (the red LED on the left side of the front panel) will flash at a rate of approximately 2 Hz.

Position "0" is selected when the Program Select knob is positioned at 6 o'clock (HALL B). Turning the knob clockwise will increment the position number by one.

Diagnostic Test Programs

Program Select Knob Position		Diagnostic Test Program Names
0	(HALL B)	Blink both LEDs in unison
1	(HALL D)	* ROM test
2	(LARGE 2)	* RAM test
3	(LARGE 1)	*WCS test
4	(MEDIUM 2)	* Interrupt test
5	(MEDIUM 1)	MIDI wrap around test
6	(SMALL 2)	DRAM test
7	(SMALL 1)	Switch test
8	(PLATE D)	Non-volatility test
9	(PLATE B)	Clear RAM (special proceedure required)
10	(INVERSE)	Blink MEM LED
11	(GATE)	Blink OVLD LED
12	(CHORUS 1)	Blink both LEDs alternately
13	(CHORUS 2)	Enter Audio Test Mode
14	(DELAY 1)	Exit to system
15	Not Assigned	NA

Test Programs

Position 0 (HALL B)
Blink both LEDs in unison

Indicates the position Zero location. When selected, both red LEDs will blink in unison at a rate of approximately 2 Hz until the next test selection is made.

Position 1 (HALL D)
ROM test

Calculates the ROM checksum and compares it to the stored value.

Position 2 (LARGE 2)
RAM test

Performs a RAM test on the stack area of RAM (since non-volatile data is not stored there). The test consists of storing and reading 55's, AA's, 00's and FF's, as well as an address test.

Position 3 (LARGE 1)
WCS test

Performs a RAM test on the WCS portion of the Lexichip. It operates identically to the RAM test on Position 2.

Position 4 (MEDIUM 2)
Interrupt test

Checks the interrupt timing by comparing it to coded timing loops.

Position 5 (MEDIUM 1)
MIDI wraparound test
(MIDI cable required)

Checks the MIDI serial port transmit and receive functions. This test requires internal jumpering to allow a MIDI OUT function to be performed instead of the factory-set MIDI THRU function. To prepare the LXP-1 for this test, perform the the following:

1. Open the unit and locate internal jumper pins W2 & W3 on the pc board near MIDI jacks.
2. Move internal jumper location at W3 to W2.
3. Connect a MIDI cable from the jack labeled: MIDI IN to the jack labeled: MIDI THRU.

When this procedure has been completed the test may be executed. This test takes approximately 5 seconds and the results will be displayed immediately upon completion. Remove the internal jumper from W2 and reset to W3 to restore the LXP-1 MIDI THRU function.

Position 6 (SMALL 2)
DRAM test

Performs a complete test of the audio DRAM in the Lexichip address area. This test takes approximately 30 seconds and the results will be displayed immediately upon completion.

Position 7 (SMALL 1)
Switch test

Compares the positions of the control knobs labeled DELAY and DECAY located on the far right of the front panel. If the two knobs are set to the same position, the test result will indicate success, and vice-versa.

Position 8 (PLATE B)
Non-Volatility test

Compares a character string stored in ROM to a character string stored at a specific address in RAM. If the two differ, a failure will result, indicating that a RAM storage failure may have occurred. If the MIDI button is pressed again without changing the Program Select knob setting, the character string is copied from ROM to RAM and the test will be performed again. If the test does not succeed when repeated, there may be a RAM hardware malfunction.

Note: This test will fail if the *Clear RAM* test has been performed since the last copy of the character string from ROM to RAM.

Test Programs, cont'd.

Position 9 (PLATE B)
Clear RAM

This operation should not be taken lightly.
This program actually consists of a data-destructive RAM test of the entire SRAM area. The last operation is the storage of zeros in all locations. The success signal indicates that the RAM passed the diagnostic test and that zeros have been stored in all memory locations. Since this test will destroy any user registers that may have been stored, a combination of Program Select knob settings are required to activate this operation. The combination is as follows:

Position "0" refers to a 6 o'clock knob position.

STEP	PGM	DECAY	DELAY	MIDI BUTTON	LED STATUS
1	9	0	0	press & release	one MEM LED flash
2	0	0	1	press & release	one MEM LED flash
3	1	1	1	press & release	one MEM LED flash
4	-	-	-	press & release	MEM LED /2 Hz

After the successful completion of each combination step, the MEM LED will flash once. If any step is performed incorrectly, a failure signal (alternately flashing red LEDs) will be activated and the procedure must be repeated from the beginning. After Step 3. is performed successfully, knob position becomes irrelevant. The final MIDI button press and release serves to distinguish the LED failure signal due to procedural errors from an actual *Clear RAM* test failure.

Position 10 (INVERSE)
Blink MEM LED

Tests the MEM LED by causing it to flash once after the MIDI button is pressed and released.

Position 11 (GATE)
Blink OVLD LED

Tests the red OVLD LED (located to the right of the green SIGNAL LED on the front panel) by causing it to flash once after the MIDI button is pressed and released.

Position 12 (CHORUS 1)
Blink both LEDs

Causes both the MEM and OVLD LEDs to flash once alternately after the MIDI button is pressed and released.

Position 13 (CHORUS 2)
Audio Test mode

Loads a program which tests the specifications of the converter circuitry by producing a digitally processed output signal which is identical to the input signal. When the MIDI button is pressed and released, a successful program load is indicated by the flashing of the MEM LED at a rate of 6 Hz. This test program will run continuously until another function is selected.

Position 14 (DELAY 1)
Exit to system

Exits the diagnostic mode and returns the LXP-1 to its normal operating mode.

Position 15 (DELAY 2)

No operation assigned.

Remove the two screws from the LXP-1 front panel. Remove the 5 hex nuts from the 1/4" connectors on the rear panel. The pc board should now slide out towards the front of its case, allowing easy access to the circuitry.

Clocks and Power Supply Measurements

Equipment Required

Variac
DMM
Frequency Counter (50MHz)
50 MHz Oscilloscope

1. Set the DMM to measure VAC. Apply power and measure the voltage across C22; it should measure > 9 VAC.

2. Plug the LXP-1 into the Variac and set output for 117 VAC.

3. Set the DMM to measure VDC and check the regulated voltages for proper levels:

Location: Power/Ground	Allowable voltage range
U19 pin 3/U19 pin 2	11.40 to 12.60 VDC
U13 pin 1/U13 pin 3	-11.40 to -12.60 VDC
U11 pin 3/U11 pin 2	4.75 to 5.25 VDC

4. Switch the DMM to VAC and check regulated voltages for minimum 60 Hz AC ripple.

Location: Power/Ground	Allowable voltage range
U19 pin 3/U19 pin 2	<1mVAC
U13 pin 1/U13 pin 3	<1mVAC
U11 pin 3/U11 pin 2	<1mVAC

Brown Out / Power Down Test.

1. Set oscilloscope for 2.5v/div (w/X10 probe) and a 1 mSec/div time base.

2. Connect scope probe to U1 pin 4. The Logic condition should be high.

3. Reduce the Variac output level to 104VAC.

4. Scope reading on U1 pin 4 should continue to be a logical high condition
.

5. Measure unregulated VDC level on U11 pin 1 (gnd on U11 pin 2) with DMM. This should read: > 7.2 VDC

6. Continue to monitor U1 pin 4 with oscilloscope and slowly reduce Variac output to 88 VAC. Pin 4 signal level should go to a logical low condition when the Variac output passes through the 100 - 88 VAC range . If this test fails, make certain that transformer AC output (across C22) is between 9.3-9.9VAC with 117VAC input. If AC transformer is OK, suspect LXP-1 power down reset circuitry failure.

Clock Measurements

Using the frequency counter, measure the clock frequencies at the following points:

Signal Name	Location	Meas	Tolerance
ZCLK	U2 /pin 6	4MHz	±0.5%(3980000-4020000 Hz)
MIDICLK	U8 /pin 9	500kHz	±0.8% (497500 -502500 Hz)

Peformance Tests

Equipment Required

Low Distortion Oscillator
with single-ended 600 ohm output
THD+N Distortion Analyzer/Level Meter
with switchable 30Khz or audio bandpass input band-pass filtering
Audio input cable
single-ended, shielded audio cable with 1/4" plug on one end and proper connector on other end to connect to Low Distortion Oscillator output
Audio output cable
single-ended, shielded audio cable w/ 1/4" plug on one end and the proper connectors on other ends to connect to THD+N Distortion Analyzer
Audio terminator plug
1/4" plug with a 100K ohm resistor attatched between tip and sleeve
1/4" Shorting plug
with tip and sleeve shorted inside shielded casing

Setups A, B and C, described below, are front panel settings used in the LXP-1 performance tests. CW refers to a clockwise knob setting and CCW refers to a counter-clockwise setting. See Front Panel Diagnostics (Page 2-2) for instructions on putting the LXP-1 into Audio Test mode.

A

Control Knob	Setting
Input Level:	Fully CW to Maximum Level
Output Level:	Fully CW to Maximum Level
Mix:	Fully CCW to 100% Dry (un-processed)
Delay/Decay:	-
Program:	Audio Test Mode (See page 2-2)

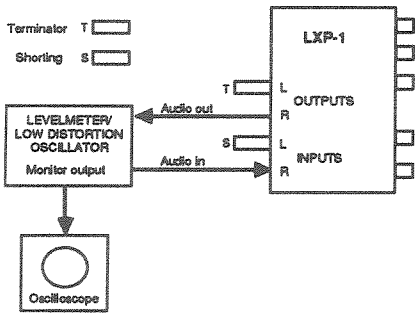
B

Control Knob	Setting
Input Level:	Fully CW to Maximum Level
Output Level:	Fully CW to Maximum Level
Mix:	Fully CW to 100% Wet (processed)
Delay/Decay:	-
Program:	Audio Test Mode (See page 2-2)

C

Control Knob	Setting
Input Level:	Fully CW to Maximum Level
Output Level:	Fully CW to Maximum Level
Mix:	Fully CW to 100% Wet (processed)
Program:	SMALL ROOM-2
Delay/Decay:	Set to 12 o'clock, then move to 6 o'clock while SMALL ROOM 2 is running.

Overall Gain Measurement



Setup A

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator plug to left channel output

Procedure

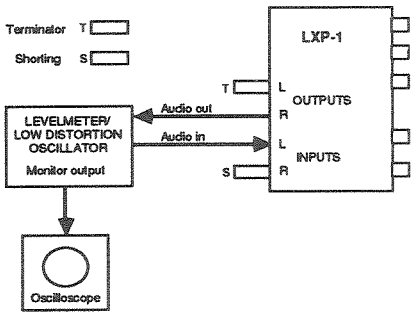
1. Apply a 1Khz signal at -15dBV (178 Vrms) to right channel input.
2. Measure output level on right channel output. Acceptable output level should measure between 13.5 and 15.5 dBV (4.75 to 5.95 Vrms)
3. Swap all right and left channel audio connections and repeat steps 1. and 2. on left channel.

Inter-Channel Crosstalk Measurement

Setup A

Audio connections

1. Audio input cable from Low Distortion Oscillator output to left channel input
2. 1/4" shorting plug to right channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator plug to left channel output



Procedure

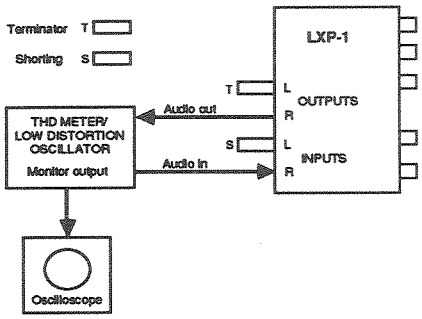
1. Apply a 1 kHz signal at -20dBV (100mVrms) to left channel input.
2. Measure Right channel output level . Acceptable level < -50dBV (3.2 mVrms).
3. Swap all right and left channel audio connections and repeat steps 1. and 2. on left channel .

Dry (unprocessed) THD Measurement

Setup A

Audio connections

1. Audio input cable from Low Distortion Oscillator output toright channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to THD+N Analyzer input
4. Audio terminator plug to left channel output



Procedure

1. Apply a 1 kHz signal at -15dBV (178mVrms) to right channel input.
2. Measure Thd+N at right channel output. Acceptable reading will be <.05%.
3. Swap all right and left channel audio connections and repeat steps 1. and 2. on left channel.

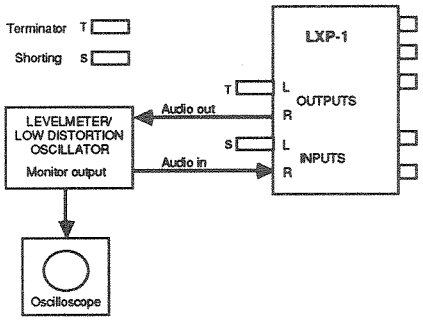
Dry (unprocessed) Frequency Response

Setup A

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator plug to left channel output

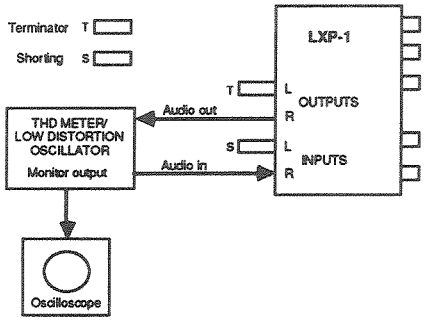
Dry (unprocessed) Frequency Response, cont'd.



Procedure

1. Apply a 1 kHz signal at -15dBV (178mVrms) to right channel input. Set Level Meter to measure right channel output as the 0 dB reference.
2. Sweep from 20 Hz to 20kHz.
3. Right channel output should measure within ±.5 dB (referenced to 1kHz output) over the range.
4. Swap right and left channel audio connections and repeat steps 1.-3. on left channel.

Wet (processed) THD Measurement



Setup B

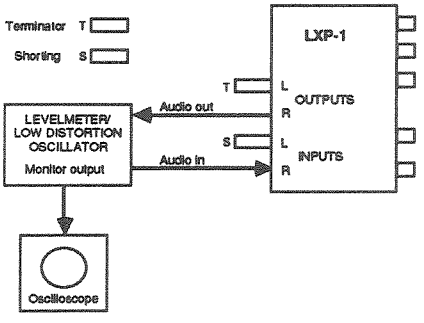
Audio Connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to THD+N Analyzer input
4. Audio terminator plug to left channel output

Procedure

1. Apply a 1 kHz signal at -20dBV (100mVrms) to right channel input.
2. Measure THD+N at right channel output. Acceptable reading will be < than .07%.
3. Swap all right and left channel audio connections and repeat steps 1. and 2. on left channel.

Wet (processed) Frequency Response Measurement



Setup B

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator plug to left channel output

Procedure

1. Apply a 1 kHz signal at -25dBV (56mVrms) to right channel input. Set Level Meter to measure the right channel output as the 0 dB reference.
2. Sweep from 20 Hz to 15kHz.

3. Right channel output should measure within +1.5 to -.5 dB (referenced to1kHz output) over the range.

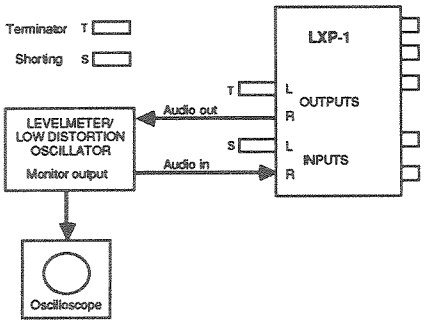
4. Swap right and left channel audio connections and repeat steps 1.-3. on left channel.

Dynamic Range/ Signal to Noise

Setup B

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to Level Meter input
4. Audio terminator plug to left chanel output



Procedure

1. Apply a 1 kHz signal at -20dBV (100mVrms) to right channel input. Set Level Meter to measure right channel output as the 0 dB reference.

2. Unplug input to right channel. This will short out both right and left channel inputs.

3. Measure level on right channel output. Acceptable reading will be $\leq$ -75 dB (referenced to 1kHz output level).

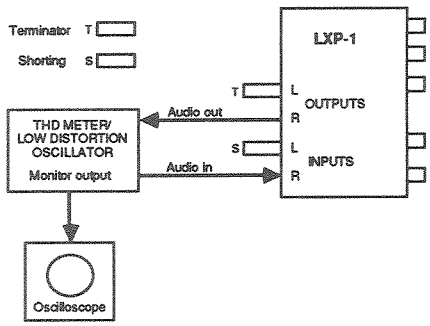
4. Swap right and left channel audio connections and repeat steps 1.-3. on left channel.

Reverb Processed THD Measurement

Setup C

Audio connections

1. Audio input cable from Low Distortion Oscillator output to right channel input
2. 1/4" shorting plug to left channel input
3. Audio output cable from right channel output to THD Meter input
4. Audio terminator plug to left channel output



Procedure

1. Apply a 1 kHz signal at -30dBV (32mVrms) to right channel input.

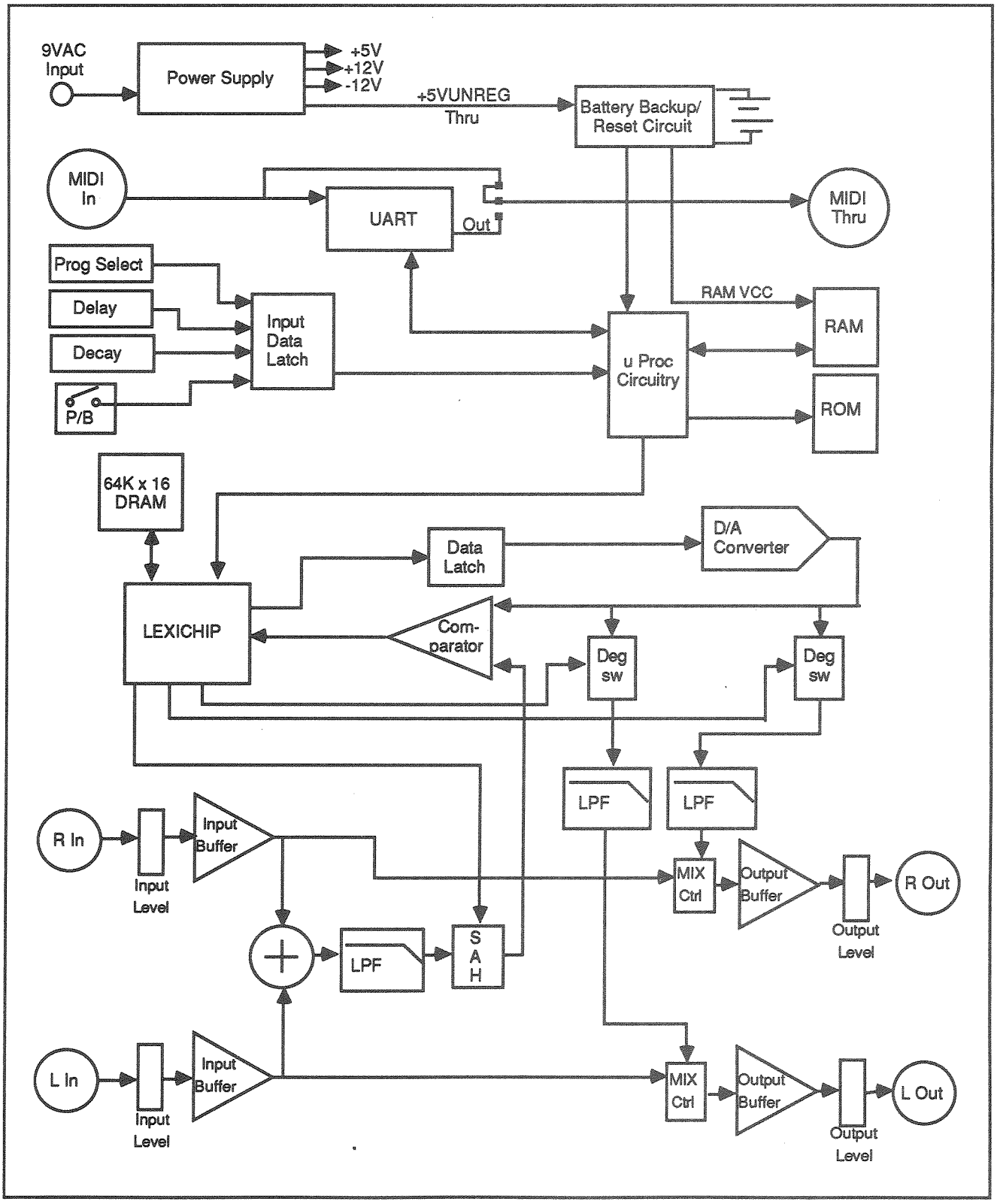
2. Measure THD+N on right channel output. Acceptable reading will be < .1%.

3. Swap right and left channel audio connections and repeat steps 1.-2. on left channel.

3

Circuit Description

Circuit Description



Power Supply

The LXP-1 power supply provides three regulated DC output voltages:

+5VDC
+12VDC
-12VDC

AC power is provided by an external transformer rated at 9VAC @ 1A. A 5mm/2.5mm input jack is provided for this power connection. A .01uF capacitor is connected across the AC input to reduce noise spikes from the line voltage input. Ferrite beads FB4 + 5 and filter capacitor C19/C22 help prevent circuit-generated RF from radiating out onto the power line.

Two sets of voltage doubler rectifier circuits develop the unregulated DC levels for the ±12 Volt supplies. C20 and C28 store the peak level of AC input voltage during one half of the AC input cycle. This stored charge adds with the next AC input half cycle to produce approximately twice the Peak input AC level across C23 and C27. CR14 and CR15 are polarized to produce the unregulated +12 Volt supply (+20 to 22VDC) across C27. CR11 and CR12 produce the unregulated -12 Volt dc supply (-20 to 22Vdc) across C23.

A single diode, half wave rectifier (CR7), in conjunction with two 1000uF capacitors, produces the unregulated +5V supply. This +5VUNREG is applied to the LXP-1 Reset and Battery Backup circuits to insure proper handling of Non-Volatile memory in power up and power down conditions.

Voltage regulation is performed by three TO220 packaged DC voltage regulator ICs.

+5V regulation is performed by U11 (7805)
+12V regulation is performed by U19 (7812)
-12V regulation is performed by U13 (7912)

Current limiting and short circuit protection is provided by the internal circuitry of these three ICs.

Reset Circuitry

The processor Reset signaling is controlled by the state of the +5VUNREG level. A voltage divider circuit incorporating CR4, R13 and R11, divides down the unregulated supply level to be used as a monitor voltage on the Schmidt inverter input of U1 pin 5. FB3 and C11 provide filtering from noise spikes emanating from the AC line. A low voltage range between 88-100VAC on the AC line should cause U1 pin 6 to go high resulting in processor reset. A normal AC input of 100-120 VAC will maintain a DC level above the inverter input threshold level and pin 6 will remain low.

An R-C circuit provides a delay in the removal of Reset during power up to allow regulated supply levels to stabilize before enabling the processor circuitry. R2 and C4 provide this power up Reset delay. A protection diode (CR2) allows an added discharge path for C4 during power down conditions. Q1, which is driven by U1 pin 6 output, is the R-C delay circuit driver. It produces a fast C4 discharge time for Reset enable and goes to a high impedence state producing the R-C delay on Reset disable.

The R-C Reset delay circuit is applied to the Schmidt inverter pin 1 input. This inverter pin 2 output (ZRST) drives three separate reset circuits:

1. Z80 Reset which requires an inverter to produce an active low Reset for the Z80. CR3, C1, and R9 produces an R-C delay when the ZRST goes to its low inactive state. This insures that the Z80 is the last device enabled and that all other devices will be in an active known state after Z80 Reset is removed.

2. ZRST is applied directly to the UART (U8) Reset input, which requires an active high signal.

3. ZRST is inverted to produce ZRST/, an active low signal which is required by the Lexichip (U17) and the SRAM Battery Backup circuit.

Battery Backup

Battery Backup is required in the LXP-1 to maintain the Non-Volatile function of processor SRAM. A 3V lithium battery maintains the minimum power requirement of the SRAM IC, U9 after power is disconnected from the unit.

When +5VCC is present, Q4 turns on, forward biasing CR13. +5Volts is then applied to VCC input of U9 allowing normal power up operation of SRAM. CR8 will be reverse-biased, preventing the +5V level from reaching BAT1. The removal of VCC causes Q4 to shut off. The BAT1 will then forward-bias CR8 and will provide a 3V level to RAM VCC input.

Q5 controls U9 CE2 pin (26). Under normal power on conditions, Q5 will conduct, maintaining an active high on CE2. If ZRST/ activates due to AC power failure, or if the regulated +5V supply fails, Q5 will shut off, disabling CE2 with a low condition. This chip select disable, in conjunction with the Battery Backup, puts U9 into an idle state and prevents stored data from being destroyed in power down and power failure situations.

Analog Circuitry

Input

Two separate left and right input signals can be applied to the two 1/4", unbalanced input jacks (J7 and J8). Both jack inputs are shorted together, allowing a single input source to be applied to left and right input circuitry. This permits the summing circuit R56, 57 and 58 to function properly for single-ended input signals. 1/4" plugs installed in both input jacks will remove this short, allowing separate left and right input signals to be applied to the LXP-1 circuitry.

Inputs are DC isolated by 10uF non-polarized coupling capacitors. R52, a dual 50K potentiometer located on the input, functions as an input gain control by controling the input signal level to the preamp stage. A dual op amp (U30) performs this preamp function by providing the initial gain and buffering for the Left and Right input signals.

Left and Right preamp outputs are applied to the dual Mix control (described later) and are also summed by a resistive summing matrix comprised of R56,57 and 58. This summed L+R signal is converted to digital data for processing. First, however, it is coupled into U32, a 15kHz low pass filter. Pre-Emphasis of higher audio frequencies is performed by the first 1/2 of U31. The pin 1 output of U31 is applied to the converter Sample and Hold circuit described below.

Pin 1 of U31 is also coupled through a 10K ohm resistor (R63) into the signal detect circuit. A diode clipper (CR20) removes the negative portion of audio AC and develops an average +DC level across C67 which is proportional to audio input level. An input signal level of -20dBV or greater will create sufficient +DC across C67 to turn on Q10, which results in the visible lighting of the green signal LED (LED3) located on the front panel of the unit.

Converter Circutry

SAH

The remaining half of U31, together with SPDT FET switch (U28), functions as the input Sample and Hold. The SAH switch is controlled by the SAMP signal output from the Lexichip. When SAMP is high, U28 pins 13 and 14 are shorted. The audio output current from the Pre-Emphasis circuit develops a voltage across storage capacitor C63. The Hold function is performed when SAMP, in it's low state connects U28 pin 14 to pin 12. C63 will then hold its sample of the audio input while the Analog to Digital conversion is performed.

DAC

U22 is a PCM54 16 Bit DAC. It converts 16 Bit data latched into it from the Lexichip into an analog voltage level (see Data to Voltage chart below). The output voltage from U22 is either deglitched and applied to audio output circuitry, or compared to sampled input level by the comparator U23 for analog to digital conversion. A full description and timing diagram of DAC control circuitry is explained in the Lexichip section of this manual.

Digital Input code	Analog Output
0000h	+2.99991V
7FFFh	0.0000V
8000h	-91.6uV
FFFFh	-3.0000V

DAC Data To Voltage

Comparator

An LM311 (U23) aids in the analog to digital conversion by comparing the input sample level to the DAC output. The DATA output signal on U23 pin 7 is applied to the Lexichip. The internal successive approximation register (SAR) of the Lexichip performs the logic function in the A/D conversion. This determines if the current DAC output is equal to the sampled input, if not, a new data value is latched out to the DAC for comparison.

Deglitch Circuitry

The remaining two FET switches in U28 are used to deglitch DAC outputs to the Right and Left output circuitry. The DAC inputs to deglitch hold amplifiers (U24) are connected to ground by a low condition on DEG0 (for left output) and DEG1 (for right channel). When the DAC is ready to output a sample to a specific channel, the Lexichip brings that channel's DEG(0 or 1) signal to a high state. This charges storage capacitor C41 or 52 (depending on the channel being output) to the DAC output level. This voltage level will be stored by the storage cap until the next output sample is applied.

Output

Output Low Pass Filters

Left and Right channel outputs from deglitch amplifiers are filtered by 15kHz low pass filter modules U25 and U29. Filter outputs are applied to de-emphasis circuits (C48,R43 for left, C56,R44 for right) to compensate for the pre-emphasis of U31, and are amplified by a dual op amp U27.

Mix and Output Level Controls

U27 outputs are applied to one end of one of the ganged linear 50k ohm pots R39. The opposite end of the dual pot is connected to the Right and Left preamp stage outputs. The user control varies the wiper position of R39 in order to control the percentage of Wet (processed) and Dry (unprocessed) signals on LXP-1 outputs.

The two outputs from R39 are applied to the ganged output level pot R31. This user control determines the signal level applied to the final output Buffer stage (U26).

Output Buffer and Mute Circuitry

The dual op amp U26 provides unity gain and buffers the Mix and output level pots from the unit output. Two series resistors on outputs of U26 (R21 &24, R26 &32) develop the approximate 600 Ohm output impedence for the unit's line level outputs.

Two discrete FET transistors, Q6 and Q7 provide an output muting function by shorting U26 outputs to ground after the 560 ohm resistors in series with the outputs. Muting is controlled by the ZRST/ signal described in the Reset Circuitry section of this manual. When ZRST/ becomes an active low, Q8 shorts C39 to ground, which turns on muting FETs. When ZRST/ is released, the charge time of C39 by R30 produces an approximate delay of 1 second in the release of output muting after ZRST/.

Since ZRST/ is activated at power up and power down, its control over output muting will prevent noise which can cause speaker damage if the LXP-1 is powered up or down while connected to an amplifier.

The 1/4" output jacks (J5 and J6) will short left and right output signal lines together when only one output plug is connected. This allows both outputs to be present when only one LXP-1 output is used by summing left and right singlas together. This short is disconnected when plugs are connected to both outputs allowing for the full stereo effect to be utilized.

Digital Circuitry

Z80 Microprocessor Circuitry

A 4MHz Z80 microprocessor (U2) is utilized as the Host Processor for the LXP-1. It performs the following functions:

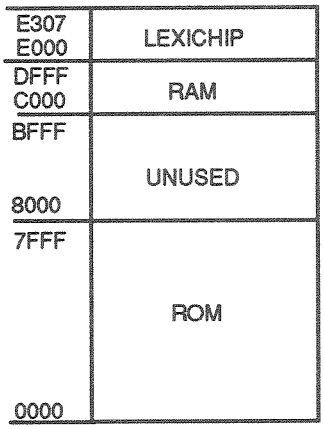
1. Processing of data and instructions to and from the UART
2. Processing of data and instructions to and from the LEXICHIP
3. Handling of user data input from digital user controls
4. Maintenance of non-volatile, user-controlled registers

Memory

The 32K bytes of ROM space is contained in a single 27C256 PROM (U6). Audio effects programs, diagnostics, I/O and housekeeping subroutines are contained in this memory space.

A CMOS 4364C SRAM provides 8K bytes of RAM space which is kept non-volatile by the battery backup circuit described earlier in this section.

The LEXICHIP contains it's own on-board program RAM and I/O registers which are addressable by the Z80 Host processor. This memory storage space is mapped into the Z80's 64K of addressable memory space as shown below.



Memory Map

PAL Decoding

A single PAL IC (U10) performs the I/O and memory decoding for the Z80 Host processor. An internal flip-flop circuit is also programmed to divide down the 4MHz ZCLK to a 2MHz UCLK output. The chart below displays the PAL decoding scheme.

MEMORY DECODING (MREQ/ = 0)						
M1/	SADR:	15	14	13	HEX ADDR.	Active Sel. Line
0		0	0	0	0000h through	ROM/
0		0	1	1	7FFFh	ROM/
1		1	1	0	C000h-DFFFh	RAM/
1		1	1	1	E000h-FFFFh	LEX/

I/O DECODING (IORQ/ = 0)				
SADR:	7	6	HEX ADDR.	Active Sel. Line
	0	0	00h -01h	UART/
	1	0	80h	IO1/
	1	1	C0h	IO2/

Audio Processor Circuitry

LEXICHIP: Z80 Interface

The LEXICHIP (U17) performs all the digital effects processing calculations for the LXP-1. It receives instructions from its internal program RAM, referred to as the Writeable Control Store (WCS). Address, data and control lines for the WCS, as well as various LEXICHIP control and status registers are shared with the Z80 bus. This allows the Z80 Host processor to load audio effects programs into the LEXICHIP, monitor status of audio data, and synchronously change program parameter values in audio programs. The Z80 treats this memory as RAM-mapped in its memory space between addresses E000 to E307 HEX.

Clocks

An internal crystal oscillator driver circuit drives a 16MHz crystal mounted across pins 75 and 76 on the LEXICHIP. Internal LEXICHIP circuitry divides this clock frequency down to provide the 4MHz ZCLK which is used by the Z80 processor.

PCLK1 (pin 73) output is programmed to divide down 16MHz clock to the 500kHz MIDICLK signal which is utilized by the UART IC to set up serial communications baud rate.

Word Clock (pin 59) is used as a clock reference by the LXP-1. It operates at a 31. 25kHz rate and is utilized by the UART interrupt timing circuitry, as explained in the UART, I/O section (Page 3-9).

LEXICHIP: Audio Memory

Four 64K by 4 bit dynamic RAM ICs (U14,15,18,21) provide the 64K by 16 bit RAM space used by the LEXICHIP for audio data storage. DRAM read, write, and refresh functions are performed by a dedicated set of address and control lines, and a 16 bit data bus provided by LEXICHIP.

LEXICHIP: DAC/ADC Control Logic and Data Port

Internal control logic circuitry enables the LEXICHIP to command complete control over external DAC functionality with minimal external circuitry.

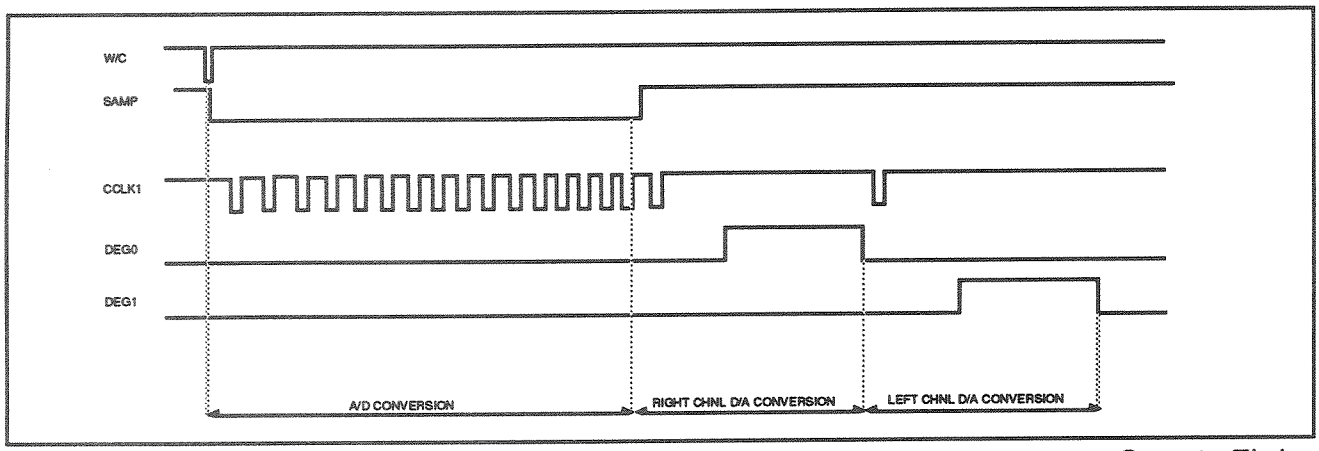
Two 8 bit latches (U16,U20) are used to latch 16 bit data out to DAC via the DRAM data bus. LEXICHIP output CCLK1 clocks DAC data into these DAC conversion latches.

An internal Successive Approximation Register (SAR) allows the DAC, in conjunction with an external comparator, to perform analog to digital conversions. A data value is latched into conversion latch. DAC output is compared to analog input by the comparator. The comparator's resulting output (DATA) is applied to LEXICHIP input SI1, and the SAR logic circuitry determines either the next DAC output value or an end of conversion. Converted data is then processed by the LEXICHIP with instructions from its RAM resident digital effects program.

DAC logic signals are provided by the LEXICHIP to control the SAH and deglitch functions and conversion data latching. A Word Clock signal (WC) is used as a clock reference (see CLOCKS section) and indicates the beginning of a conversion cycle.

On the falling edge of WC/, SAMP goes low in order to hold input sample on SAH for an A/D conversion. The internal SAR then applies a DAC data output to DAB0-15. This data is latched into conversion latches on the positive edge of the CCLK1 signal. The DATA signal from comparator is then compared by LEXICHIP to determine the next SAR output value. Sixteen SAR output samples are required to perform an analog conversion. Since the later samples produce smaller voltage changes on DAC output, less time is required for DAC to settle, therefore, the time duration between CCLK1 pulses towards the end of the A/D conversion is reduced.

The 17th CCLK1 pulse after WC/ latches left channel data out to DAC. After sufficient DAC settling time, the left channel deglitch switch is disabled by the high state of DEG0, applying a DAC sample to left channel output circuitry. The last CCLK1 pulse in the WC/ cycle latches right channel data to DAC and DEG1 goes high to output DAC output to right channel.



Converter Timing

UART, I/O

UART IC

Serial MIDI communications are handled by U8, an 82C51A UART IC. U8 is mapped into the Z80's I/O space at locations 00h (data register) and 01h (instruction register). The PAL decoder IC provides it with a 2MHz clock (UCLK) required by the internal logic of U8. The MIDICLK input from the LEXICHIP is a 500kHz baud rate clock which is frequency divided by U8 internally to produce the 31.25kHz baud rate used in MIDI serial communications.

The transmit and receive data connections (TXD,RXD) are applied to the MIDI standard I/O hardware. The unused handshake signals DTR and RTS drive two separate LED driver circuits.

DTR, in a high state, will turn on Q9 and thereby light the OVERLOAD LED signal (LED2). The Z80 will set this bit high when the LEXICHIP indicates that the audio signal is about to exceed, or has exceeded, the digital clipping level.

RTS bit is controlled by Z80 insrtuctions in order to light the MEMORY LED (LED1) for various system status indicators, as described in the Owner's manual.

The 31.25kHz WC/ signal is applied to the digital counter U3. Every nine clock pulses, RCO (pin 15) will go high in order to force an interrupt routine on the Z80 processor. The processor will then access the UART to examine the RXD port for any MIDI input data received. This is the heartbeat interrupt for the software operating system.

MIDI I/O Hardware

The MIDI hardware utilized by the LXP-1 complies with the MIDI 1.0 specs. It incorporates 5 pin, female DIN connectors for input and output/thru connections. MIDI IN is optocoupled into UART RxD line for ground isolation purposes. Two jumpers,W2 and W3, allow the user to select MIDI THRU or MIDI OUT function. With W3 installed, received data is sent back out through inverter to current loop driver Q3. W2 installed will connect TxD out to Q3, allowing for user register dumps and other MIDI output functions. Ferrite beads FB1 and FB2, are connected in series with MIDI THRU/OUT lines to reduce RFI.

User Data Input Hardware

Two tri-state® buffers, U4 and U7, provide an input port to the Z80 for the three 16-position Panel switches (S2,3 and4), the on/off Defeat switch input (J3) and the momentary push button (S1).

S2 (DECAY control), S3 (DELAY control) and S4 (Program Select) are 16-position switches which produce a 4 bit binary output. RP1 and 1/2 of RP2 act as pullup resistors for these data lines. The status of S2 and S3 is checked by the Z80 when it selects the IO1/ address.

S1 is connected to a pullup resistor in RP2. When pressed, a low state is produced on pin 11 of U7. An external on/off switch connected to the DEFEAT input will control the logic state of DEF/ signal applied to U7 pin 15. DEF/ is normally high due to it's connection to a pullup resistor (RP2). R5 and C10 on DEFEAT input act as an RFI filter. CR5 and CR6 provide overvoltage protection for DEF/ input .

The status of S2, DEF/ and S1 is made available to the Z80 when IO2/ is addressed.

4

Troubleshooting

Troubleshooting

Please read the previous sections of this manual before consulting this section for guidance.

Overview

The Performance Verification section (section 2) contains instructions on running the Diagnostic programs on the LXP-1. Many of these programs will identify specific hardware failures within the unit and will be referred to in this section. A familiarization with block diagram and descriptions in the Circuit Description section will also be helpful in isolating specific problems.

Preliminary Inspection

The LXP-1 can be opened for visual inspection by removing the two front panel screws and the five hex nuts on the rear panel 1/4" jacks. The circuit board slides out of the box with the front panel attached.

A thorough visual inspection of a malfunctioning unit once opened is good troubleshooting practice. Check for loose ICs, damaged jacks and controls, overheated or burnt parts and damaged PC board traces.

Observe whether the malfunction is intermittent, heat related or shock related.

Using Diagnostics in Troubleshooting

Processor hardware tests such as ROM, RAM and DRAM tests can be run to isolate processor circuitry problems.

The front panel push button and Program select switch are exercised thoughout the diagnostic testing. If diagnostics cannot be selected and executed properly with these two controls, their proper functioning is suspect. The panel switch test will check the functionality of the DELAY and DECAY controls.

Overload and Memory LEDs and driver functionality can be tested with the three LED flashing tests.

The analog signal can be traced though the converter circutry by running the Audio Test Loop program.

The MIDI wraparound test will give a pass/fail result, however, it will not be useful for troubleshooting hardware since data is only transmitted for a brief time while the test is being performed. (See MIDI I/O, page 4-3.)

Symptom Troubleshooting

No Audio output (Wet signal)

Check all power rails with a scope or multimeter. Verify that the RESET signals are not active due to power supply or circuit malfunction. Clock circuitry can be checked initially by checking ZCLK signal on pin 6 of the Z80. No clock signal present indicates a possible LEXICHIP clock oscillator failure. This will cause all converter logic curcuitry to freeze, resulting in no wet output signal.

Note: An X10 attenuator probe should be used when probing the 16MHz crystal for an oscilloscope reading. Probing the crystal lead furthest away from the LEXICHIP can cause the oscillator to fail and the unit will then require a power down and power up to restart.

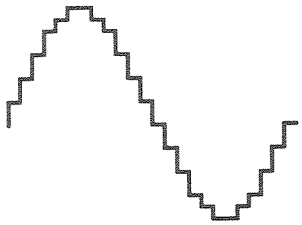
in early units, C21 was left unpopulated. Installing a 33pf ceramic bypass capacitor in C21 position can eliminate oscillator startup and intermittent failures. Units in the field should have his capacitor populated if they exhibit the following symptoms:

1. Unit is occasionally dead on power up.

2. Occasional crashes during operation.

3. Occasional oscillations and noise appear on output, even while sitting idle, and disappear when a new program is selected.

The SAMP, DEG0, DEG1 and WC/ signals can be checked and compared to the DAC timing chart in the Circuit Description section of this manual (Section 3). A 1kHz-25dB audio signal can be applied to inputs, and the signal can be traced into and out of the converter . A sampled sinewave staircase signal as shown below should appear on A/D input (U31 pin 7) and D/A outputs (U24 pins 1 &7).



No Audio output (Wet and Dry)

±12 volt supply rails should be checked for failure and the signal should be traced though the analog input to the output circuitry. A defective 1/4" connector could result in no output on one or both channels, depending on input and output connections used.

Noisy output (Wet signal)

Faulty DRAM can cause data errors in the effects processing circuitry. If the DRAM diagnostic does not indicate a failure, check the noise and distortion levels of the wet signal while the Audio Test Loop diagnostic is running. If distortion is only prevalent on certain effects programs, such as reverb, then the LEXICHIP processing circuitry is suspect. A noisy wet signal under all conditions could be the result of either converter or LEXICHIP failure. Perform shock testing while monitoring the wet audio output to determine if a loose IC in the converter /audio processing circutry is causing the problem. If noise is present on both wet and dry signals check the supply rails and trace the audio signal through the analog circuitry .

MIDI I/O

If the MIDI wraparound diagnostic test indicates a failure, place the LXP-1 into normal operating mode. With W2 in place, connect a MIDI cable from IN to OUT. When the DELAY or DECAY panel control is turned, MIDI data should be sent from the LXP-1 MIDI output to the input. The red MEMORY LED should flash when MIDI data is pulsed into the MIDI input port. If this does not occur, the MIDI signal can be traced through the MIDI IN/OUT hardware to find the malfunction.

If no MIDI data is being generated from UART TxD output, perform the following checks :

Check the MIDICLK and UCLK inputs and verify that the UART/ select line is being selected at regular intervals.

Check U3 pin 2 for the WC/ pulse which occurs at 32uSec intervals. This should cause U3 to generate an interrupt to the Z80 every 288uSec to scan UART input status. Trace this input pulse out from U3 pin 15 to the U1 inverter (pin 8 and 9).

If all the above-mentioned UART inputs and controls are functional but no MIDI data can be output or received, then the UART is suspect. This problem could also cause improper MEMORY and OVERLOAD LED operation.

5

Specifications

Specifications

Frequency Response:	20 Hz - 15 kHz, ± 1.0 dB (Wet) 20 Hz - 20 kHz, ± 0.5 dB (Dry)
Dynamic Range:	85 dB, typical
Minimum Input Signal:	-20 dB
Total Harmonic Distortion: (THD):	< 0.07% @ 1 kHz (Wet) < 0.05% @ 1 kHz (Dry)
Input Impedance:	50 kilohm (Stereo) 25 kilohm (Mono)
Output Impedance:	600 ohm
Signal Level Indication:	Signal Detect (Green) Processed Signal Overload (Red)
Defeat:	1/4" tip/sleeve phone jack for connection to any on/off toggle switch. Closed condition enables defeat mode.
Connections:	Inputs: 1/4" tip/sleeve phone jack Outputs: 1/4" tip/sleeve phone jack Defeat:: 1/4" tip/sleeve phone jack Power: 5.00 mm/2.5mm MIDI In: 5-pin DIN MIDI Thru: 5-pin DIN
Power:	9 VAC, 1 A AC wall transformer (supplied)
Dimensions:	8" W x 1.7" H x 8" D (203.2 x 43.2 x 203.2 mm)
Weight:	3.5 lb (1.59 kg)
Environment:	0 - 35°C (32 - 95°F)

Specifications subject to change without notice

6

Parts List

Parts List

PC BOARD

PART NO.	QTY	DESCRIPTION	REF.
POTENTIOMETERS			
200-06034	1	POT,RTY,PC,50KBX2,6MM/FLT,16MM	R39
200-06035	2	POT,RTY,PC,50KAX2,6MM/FLT,16MM	R31,52
CARBON FLM RES			
202-00514	4	RES,CF,5%,1/4W,100 OHM	R12,14,21,32
202-00518	3	RES,CF,5%,1/4W,220 OHM	R1,6,7
202-00520	1	RES,CF,5%,1/4W,270 OHM	R10
202-00521	3	RES,CF,5%,1/4W,330 OHM	R5,71,72
202-00529	2	RES,CF,5%,1/4W,1K OHM	R17,27
202-00530	1	RES,CF,5%,1/4W,1.2K OHM	R15
202-00533	5	RES,CF,5%,1/4W,2K OHM	R33-35,40,65
202-00534	1	RES,CF,5%,1/4W,2.2K OHM	R8
202-00536	1	RES,CF,5%,1/4W,2.7K OHM	R3
202-00545	3	RES,CF,5%,1/4W,6.8K OHM	R43,44,61
202-00549	6	RES,CF,5%,1/4W,10K OHM	R2,4,9,16,63,70
202-00579	5	RES,CF,5%,1/4W,470K OHM	R23,25,28-30
202-01077	2	RES,CF,5%,1/4W,560 OHM	R24,26
202-01228	2	RES,CF,5%,1/4W,620 OHM	R59,60
202-01245	2	RES,CF,5%,1/4W,1.6K OHM	R11,13
METAL FLM RES			
203-00455	2	RES,MF,1%,1/8W,681 OHM	R51,69
203-00457	4	RES,MF,1%,1/8W,1.50K OHM	R38,41,55,67
203-00459	1	RES,MF,1%,1/8W,2.00K OHM	R54
203-00471	2	RES,MF,1%,1/8W,10.0K OHM	R47,49
203-00482	2	RES,MF,1%,1/8W,20.0K OHM	R50,68
203-01251	1	RES,MF,1%,1/8W,8.06K OHM	R53
203-01490	1	RES,MF,1%,1/8W,3.09K OHM	R64
203-01673	3	RES,MF,1%,1/8W,16.5K OHM	R56-58
203-02611	5	RES,MF,1%,1/8W,5.62K OHM	R36,37,42,45,66
203-02655	2	RES,MF,1%,1/8W,6.04K OHM	R46,48
NETWORK RES			
205-05638	3	RES,NET,SIP,2%,10KX9 RP1-3	
ELECTROLYT CAP			
240-06096	6	CAP,ELEC,10uF,25V,RAD,NON-POL	C50,55,61,65,66,C68(@R62)
240-06611	6	CAP,ELEC,1000uF,25V,RAD	C15,16,20,23,27,28
TANTALUM CAP			
241-00652	3	CAP,TANT,4.7uF,25V,RAD	C4,40,51
PCRB/PP CAP			
244-00660	2	CAP,MYL,.01uF,100V,10%,RAD	C48,56
244-02342	1	CAP,MYL,.68uF,50V,10%,RAD	C39
244-04901	1	CAP,MYL,.022uF,100V,10%,RAD	C57
244-04960	3	CAP,MYL,1uF,5%,RAD	C17,35,36

CERAMIC CAP			
245-00592	2	CAP,CER,510pF,50V,10%	C41,52
245-01651	1	CAP,CER,.1uF,50V,80/20%	C1
245-03609	33	CAP,CER,.1uF,50V,Z5U,AX	C2,3,5-9,11-14,18,25,26, C29-33 C37,38,42-47,53,54,58,59, C62,64
245-03610	4	CAP,CER,.01uF,100V,Z5U,AX	C19,22,34,67
245-03868	1	CAP,CER,33pF,100V,COG,10%,AX	C21
245-03869	3	CAP,CER,100pF,100V,COG,10%,AX	C10,49,60
245-03871	1	CAP,CER,1000pF,100V,X7R,10%,AX	C63
INDUCTORS			
270-00779	5	FERRITE,BEAD	FB1-5
DIODES			
300-01024	1	DIODE,1N746	CR10
300-01029	9	DIODE,1N914 AND 4148	CR1,5,6,9,16-20
300-01030	5	DIODE,1N4004 AND 4005	CR7,11,12,14,15
300-01154	1	DIODE,1N751,ZENER,5.1V	CR4
300-02401	4	DIODE,BAR 35,SCHOTTKY,LOW VF	CR2,3,8,13
TRANSISTORS			
310-01007	4	TRANSISTOR,2N3904	Q1,2,9,10
310-01008	2	TRANSISTOR,2N3906	Q4,5
310-01646	1	TRANSISTOR,2N4403	Q8
310-01647	1	TRANSISTOR,2N4401	Q3
310-06612	2	TRANSISTOR,J108	Q6,7
DIGITAL/CMOS IC			
330-03586	2	IC,DIGITAL,74HCT244	U4,7
330-04271	2	IC,DIGITAL,74HCT273	U16,20
330-04272	1	IC,DIGITAL,74HCT163	U3
330-04589	1	IC,DIGITAL,74HCT14	U1
330-04675	1	IC,DIGITAL,74F08	U12
330-06204	1	IC,DIGITAL,LEXICHIP 1	U17
LINEAR IC			
340-00725	1	IC,LINEAR,LM311	U23
340-00742	1	IC,LINEAR,7805 (LM 340 T-5)	U11
340-00743	1	IC,LINEAR,7812 (LM 340 T-12)	U19
340-01463	1	IC,LINEAR,7912 U13	
340-01566	1	IC,LINEAR,LF353,DUAL OP AMP	U31
340-06036	4	IC,LINEAR,uPC4570,DUAL OP AMP	U24,26,27,30
INTERFACE IC			
345-06037	1	IC,INTER,82C51A	U8
SS SW IC			
346-00770	1	IC,SS SWITCH,4053	U28
MEMORY IC			
350-04282	1	IC,SRAM,4364,8KX8,150NS,LPS	U9
350-04434	4	IC,DRAM,64KX4,12ONS	U14,15,18,21
→ 350-06700	1	IC,ROM,27C256,LXP-1,V1.0 6 ⟷	U6
350-06701	1	IC,PAL,16R4A,LXP-1,V1.00	U10

CONVERTER IC			
355-06038	1	DAC,PCM54HP	U22
MICROPROC IC			
365-04284	1	IC,uPROC,Z80,CMOS,4MHz	U2
OPTO ISLTOR IC			
375-02247	1	IC,OPTO-ISOLATOR,6N 138	U5
MODULES			
380-06039	3	MOD,LPF,LC,7P,15KHz	U25,29,32
CRYSTALS			
390-06647	1	CRYSTAL,16.000 MHZ,.01%	Y1
DSPLY/IND/LED			
430-05484	2	LED,RED,T1	LED1,2
430-05485	1	LED,GRN,T1	LED3
ROTARY SWITCH			
452-06045	3	SW,RTY,BCD,16 POS	S2-4
PSH BUT SWITCH			
453-06040	1	SW,PBM,2P2T,PCRA,2MM TRAV	S1
BATTERIES			
460-04285	1	BAT,LITH,3V@160mAh,VERT COIN	BAT1
CABLE CONN			
490-02356	1	CONN,JUMPER,.1X025,2FCG	W2,3
PC MNT CONN			
510-04836	1	CONN,POST,.100X.025,HDR,4MCG	W2/3
510-06041	2	CONN,DIN,5FC@180DEG,PCRA,DJ006	J1,2
510-06042	1	CONN,DC POWER,PC,DJ005,2.5MM	J4
510-06043	5	1/4" PHONE JACK,PCRA,2C,SWITCH	J3,5-8
SOCKETS			
520-00946	1	IC SCKT,40 PIN,PC,LO-PRO	U2
520-01361	1	IC SCKT,20 PIN,PC,LO-PRO	U10
520-01458	4	IC SCKT,28 PIN,PC,LO-PRO	U6,8,9,22
520-02177	4	IC SCKT,18 PIN,PC,LO-PRO	U14,15,18,21
520-06184	1	IC SCKT,84 PIN PLCC	U17
KNOBS/CAPS			
550-06044	1	BUTTON,5MMSQ,2.8MM TANG,BLK	S1
LUGS			
620-06653	2	LUG,SOLDER,LCKING,.448"	J3,5
MACHINE SCREWS			
640-01706	3	SCRW,4-40X3/8,PNH,PH,ZN	U11,13,19
NUTS			
643-01732	3	NUT,4-40,KEP,ZN	U11,13,19

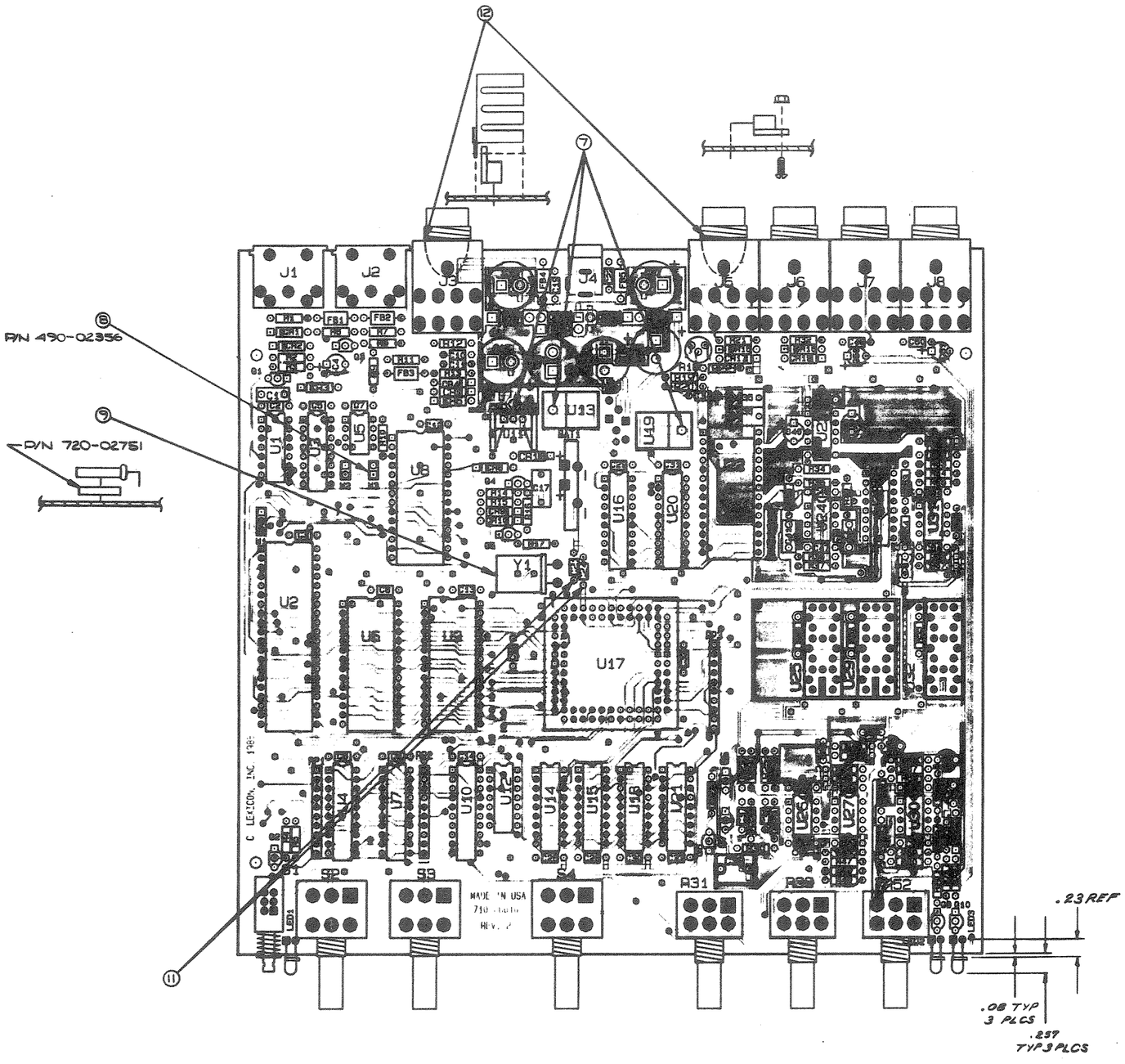
HEAT SINKS			
704-06165	1	HEAT SINK,TO-220,AAVID 5968B	U11
PC BOARDS			
710-06010	1	PC BD,LXP-1	
PLASTICS			
720-02751	1	TAPE,FOAM,DBL-STK,1/8THX3/4W	Y1

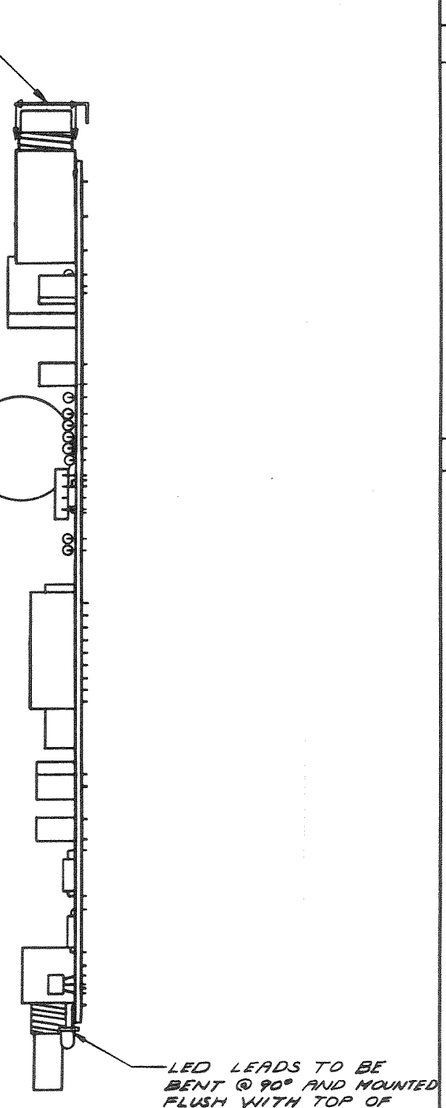
MECHANICAL PARTS

PART NO.	QTY	DESCRIPTION	REF.
CUST LITERATURE			
070-06023	1	MANUAL,OWNER'S,LXP-1	
TRANSFORMERS			
470-06048	1	XFORMER,PLUG-IN,120V,9VAC,9VA	
GROMMETS			
540-06032	2	BUMPER,GUIDE,PCB,5.75"	
FEET			
541-06033	2	BUMPER,FEET,STRIP,7.0"	
KNOBS/CAPS			
550-06031	6	KNOB,.73",6MM/FLAT,SKT,BLK/BLU	
THRD-FORM SCRW			
641-06575	2	SCRW,TAP,C,6-32X1/4,THG,PH,BLK	REAR PANEL
641-06757	2	SCRW,TAP,SW,6-32X1/2,PNH,PH,BK	FRONT PANEL
CHASSIS/MECH			
700-06614	1	ENCLOSURE,BOTTOM,LXP-1	
700-06630	1	ENCLOSURE,TOP,LXP-1	
PANELS			
702-06020	1	PANEL,REAR,LXP-1	
702-06027	1	PANEL,FRONT,LXP-1	
SHIPPING MAT			
730-02813	1	CARD,REGISTRATION,LEXICON	
730-04346	1	CARD,WARRANTY,LEXICON,8.5X11	
730-06709	1	INSERT,FOAM,TOP,LXP-1	
730-06710	1	INSERT,FOAM,BOTTOM,LXP-1	
730-06741	1	BOX,14-3/8X10-7/8X3-1/4	
730-06760	1	BAG,CLEAR,12X12X.004	
LABEL/NAMEPLTS			
740-06422	1	LABEL,PRODUCT ID,UNIVERSAL	

7

Schematics and Assembly Drawings





REV.	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH
0	RELEASE FOR PRODUCTION	J.V. 8/4/88 DWG 8/18/88	[illegible]
1	REMOVE C21 & C24 PER ECO#880324-00. REMOVE U11 HEATSINK SCREW & NUT	J.V. 4/14/88 DWG 4/21/88	LVK 4/26/88 DWG 4/26/88
2	LED DIMs ADDED ECO#880427-00	LDR 4/29/88 DWG 4/29/88	LDR 6/27/88 DWG 6/29/88
3	ADDED GROUND LUGS PER ECO#880527-00	J.V. 6/16/88 DWG 6/24/88	LVK 6/17/88 DWG 6/24/88

NOTES

1. REFER TO LEXICON BOM NO. 025-06008, 024-06007
2. ALL COMPONENTS TO BE INSTALLED FROM COMPONENT SIDE OF P.C.B.
3. MASKING FOR POST-SOLDER ASSEMBLY IS INDICATED BY SOLID AREAS ■ ●
4. COMPONENT HEIGHT .900" MAXIMUM
5. LEAD PROTRUSIONS .060" MAXIMUM FROM CIRCUIT SIDE OF P.C.B.
6. SOCKET IC POSITIONS: U2, 5, 6-10, 14, 15, 17, 18, 21, AND 22
7. USE PN 640-01706, ⌀ 4-40X3/8" PNH SCREW AND PN 643-01732, ⌀4X40 KEPNUT FOR MOUNTING U11, 13, AND U19
8. PLACE JUMPER BLOCK PN 490-02356 OVER POSTS OF W3.
9. PLACE DOUBLE STICK FOAM TAPE PN 720-02751 UNDER Y1 AS SHOWN.
10. BE SURE ALL SOCKETS, BATTERY, AND ELECTRO-MECHANICAL PARTS ARE SEATED PROPERLY.
11. DO NOT INSTALL C21 & C24.
12. BEND SOLDER LUGS UNDER PCB AND SOLDER TO J18 & J5 CENTER PIN.

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO.
		MATERIAL	APPROVALS / DATE
	710-06010		DRAWN J.V. 2/16/88
NEXT ASSY	USED ON	FINISH	CHECKED DWG 2/16/88
APPLICATION		DO NOT SCALE DRAWING	Q.C. LDR 2-17-88
			ISSUED DWG 2-17-88

lexicon

PC BD, LXP-1

ASSEMBLY DRAWING

SIZE D | FSCM NO. | DWG. NO. 080-06015 | REV 3

SCALE 1.5: 1 | SHEET 1 OF 1

ANALOG DOUBLERS

DIGITAL POWER

REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	G.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	TM 12/14/87	DS 12/14/87
		DS 12/14/87	BH 12/14/87
1	PRODUCTION RELEASE	TM 2/12/88	DS 2/12/88
		DS 2/12/88	BH 2/12/88
2	CHANGED TITLE	J.V. 4/14/88	DS 4/26/88
		JV 4/26/88	BH 4/26/88

C19 .01UF
C28 1000UF
C20 1000UF
CR7 1N4004
FB5
9VAC IN
J4
C22 .01UF
CR15 1N4004
U19 7812 VIN VOUT ADJ +12V
CR12 1N4004
U13 7912 VIN VOUT ADJ -12V
+5VUNREG
U11 7805 VIN VOUT ADJ +5V
FB4
CR14 1N4004
C27 1000UF
CR11 1N4004
C23 1000UF
C16 1000UF
C15 1000UF

+5V
U12 7408 10 N/C
U12 7408 13 N/C
SPARES

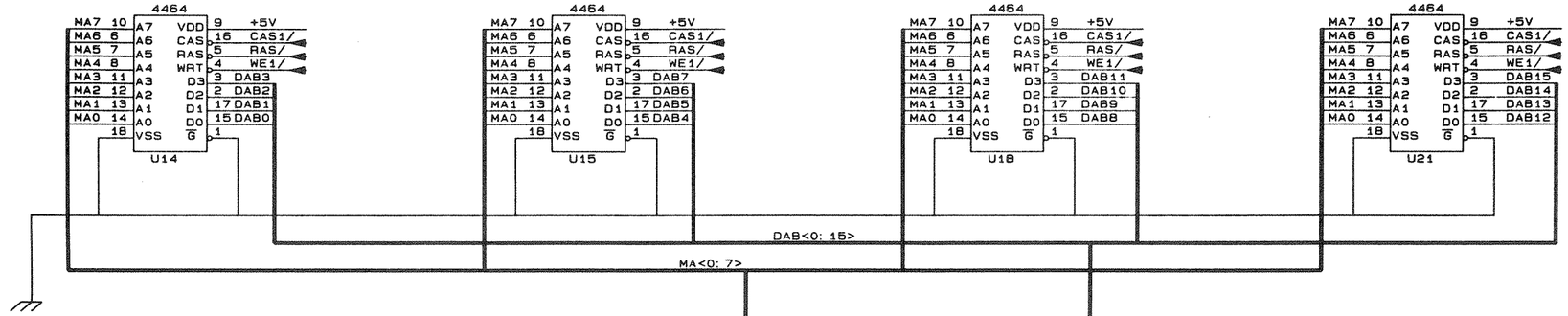
+5V: C2 0.1UF, C5 0.1UF, C3 0.1UF, C7 0.1UF, C8 0.1UF, C6 0.1UF, C9 0.1UF, C12 0.1UF, C14 0.1UF, C18 0.1UF, C25 0.1UF, C29 0.1UF, C26 0.1UF, C30 0.1UF, C31 0.1UF, C32 0.1UF, C33 0.1UF

+12V: C58 0.1UF, C62 0.1UF, C46 0.1UF, C53 0.1UF, C42 0.1UF, C44 0.1UF

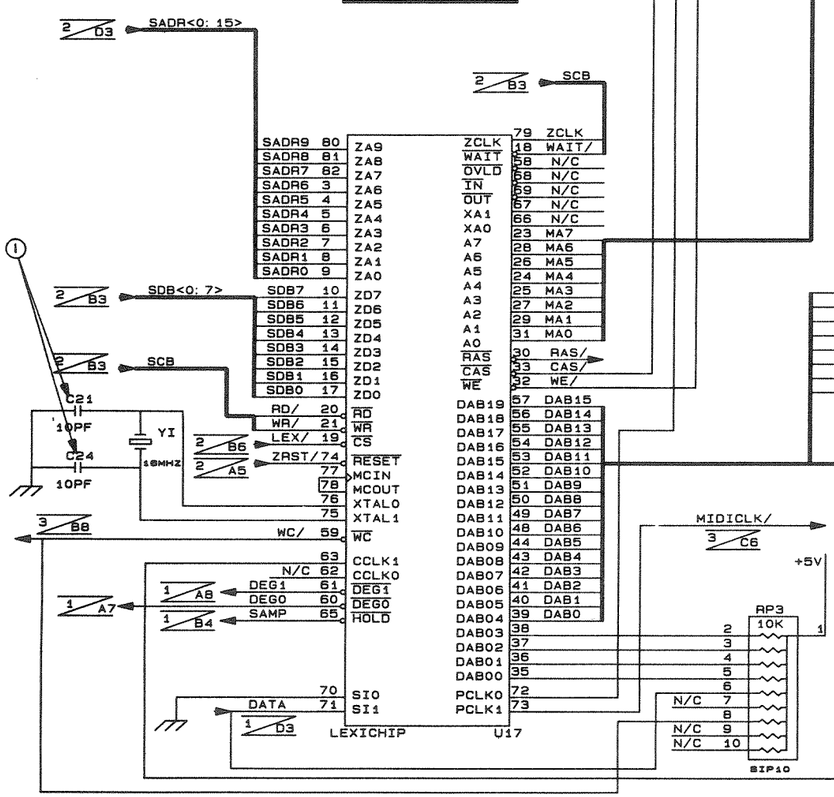
-12V: C59 0.1UF, C64 0.1UF, C47 0.1UF, C54 0.1UF, C43 0.1UF, C45 0.1UF

CONTRACT NO.	Lexicon 100 BEAVER ST. WALTHAM, MA 02154			
APPROVALS	DATE	TITLE: SCHEMATIC, LXP - 1 POWER SUPPLY		
DRAWN TM	10/27/87			
CHECKED DS	10/27/87	SIZE: D	CODE:	NUMBER: 060-06016 REV. 2
ISSUED DS	10/27/87			
Q.C. BH	10/27/87			SHEET 5 OF 5

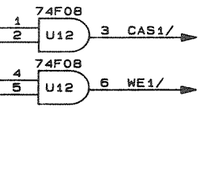
AUDIO MEMORY



AUDIO PROCESSOR



CONVERSION LATCH

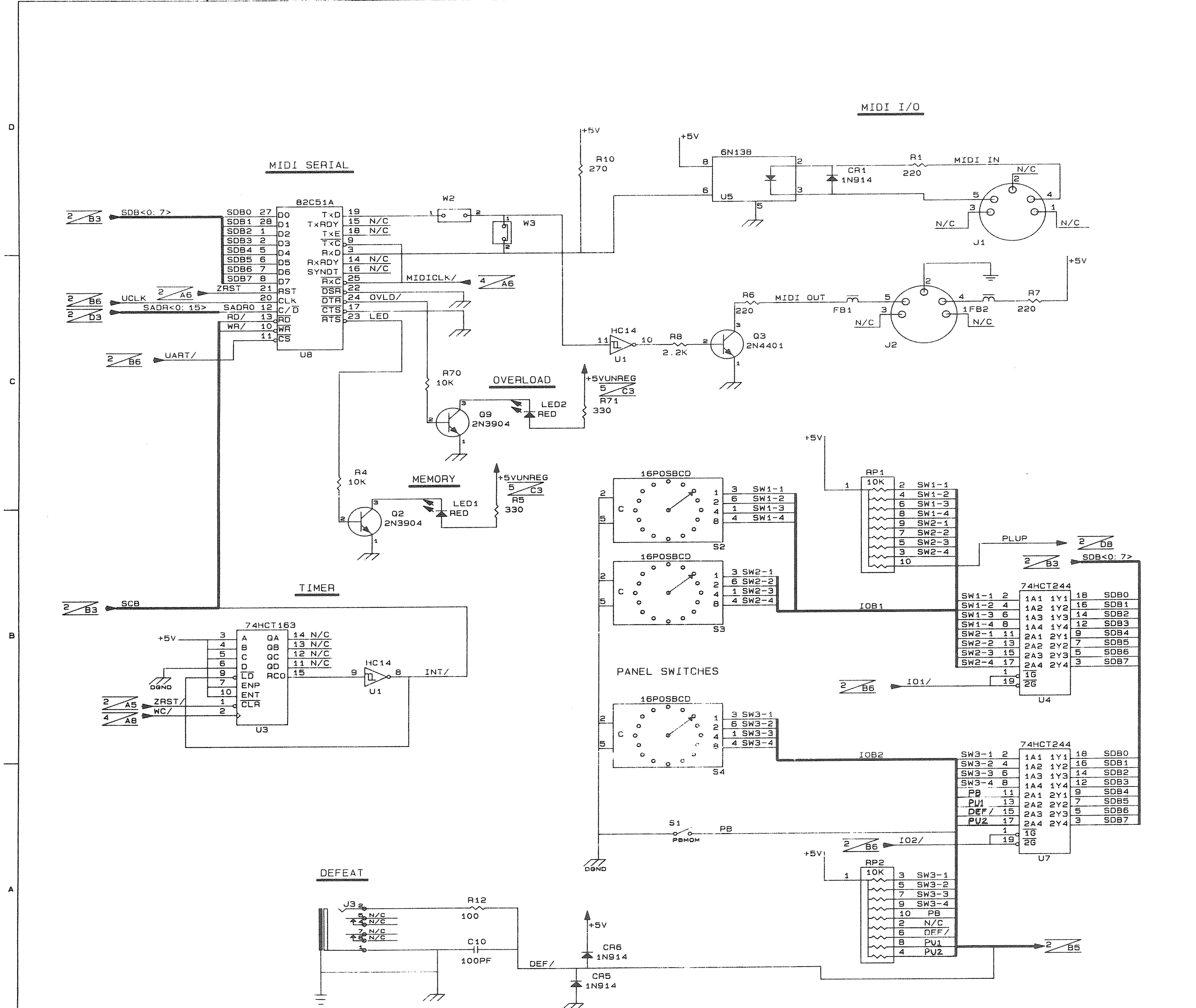


REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	TM 12/14/87 DS 12/14/87	DB 12/14/87 BH 12/14/87
1	PRODUCTION RELEASE	2/17/88 8-17-88	2/17/88 8-17-88
2	ADDED NOTE (1) PER ECO# 880324-00. CHANGED TITLE	JV 4/14/88 4/20/88	4/20/88 4/26/88

NOTES

(1) DO NOT INSTALL C21 & C24.

CONTRACT NO.	lexicon 100 BEAVER ST. WALTHAM, MA 02154		
APPROVALS	DATE	TITLE: SCHEMATIC, LXP - 1 LEXICHIP, DRAM	
DRAWN TM	10/27/87		
CHECKED DS	10/27/87	SIZE: D	CODE:
ISSUED DS	10/27/87	NUMBER: 060-06016	REV.: 2
Q.C. BH	10/27/87	SHEET 4 OF 5	



REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	TM 12/14/87 DS 12/14/87	DB 12/14/87 BH 12/14/87
1	PRODUCTION RELEASE	2-17-88	2-17-88
2	CHANGE PER ECO NO. 880223-00 CONNECTED RP2.8 AND RP2.4 TO U7.13 AND U7.17	[illegible]	[illegible] 3/28/88
3	CHANGED TITLE	J.V. 4/4/88	[illegible]
4	CHANGED SHEET [illegible] ECO # [illegible]	JV 6/24/88	[illegible] 6/24/88

CONTRACT NO.

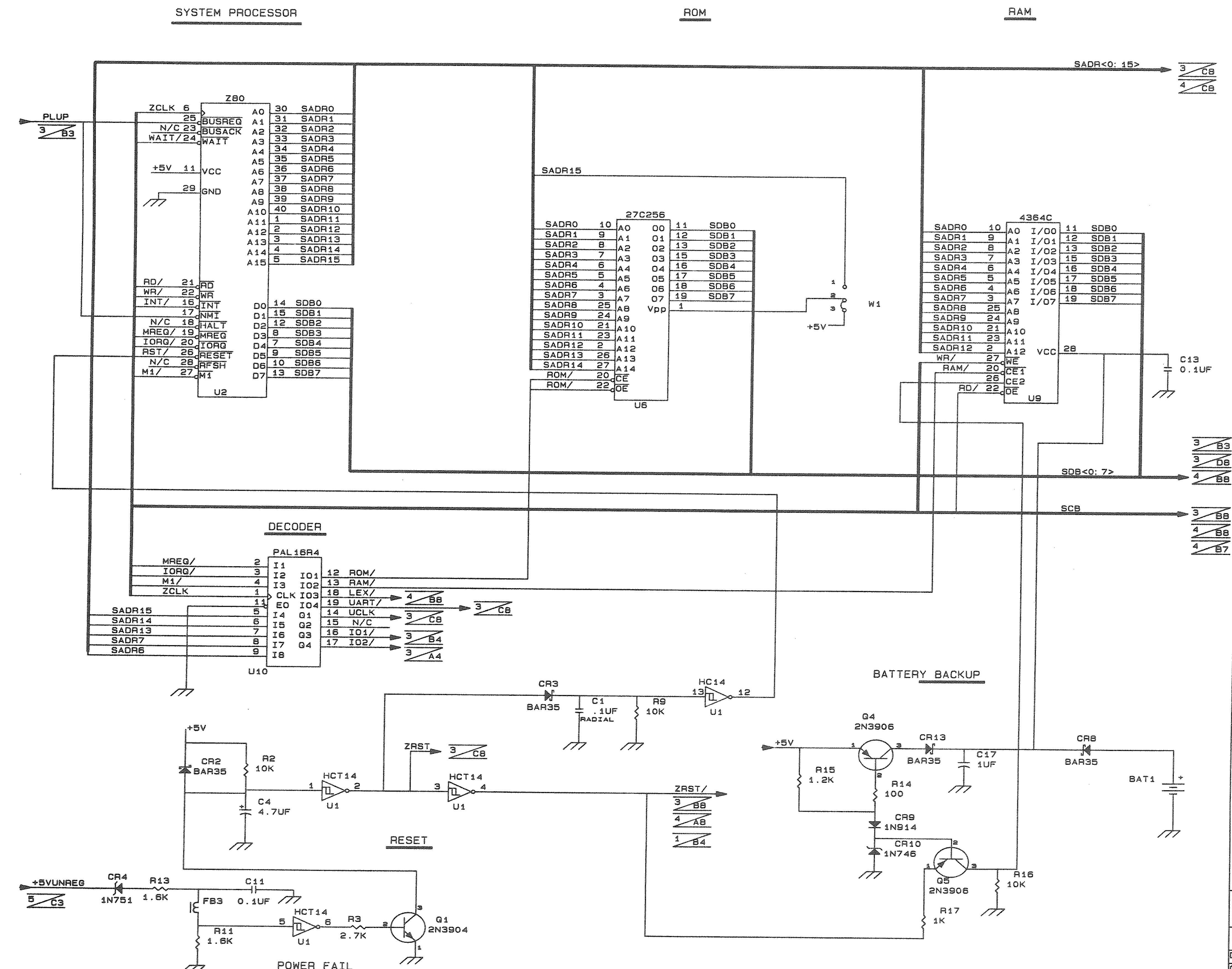
lexicon
100 BEAVER ST. WALTHAM, MA 02154

TITLE: SCHEMATIC, LXP - 1 I/O, MIDI, COUNTER

APPROVALS	DATE
DRAWN TM	10/27/87
CHECKED DS	10/27/87
ISSUED DS	10/27/87
Q.C. BH	10/27/87

SIZE	CODE	NUMBER	REV.
D		060-06016	4

SHEET 3 OF 5



REVISIONS			
REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	TM 12/14/87 / DS 12/14/87	DS 12/14/87 / BH 12/14/87
1	PRODUCTION RELEASE	MH 4/17/88 / DMF 2-12-88	KLH 4/17/88 / DMF 2-11-88
2	CHANGED TITLE	JV 4/14/88	KLH 4/26/88 / DMF 4/26/88

CONTRACT NO.

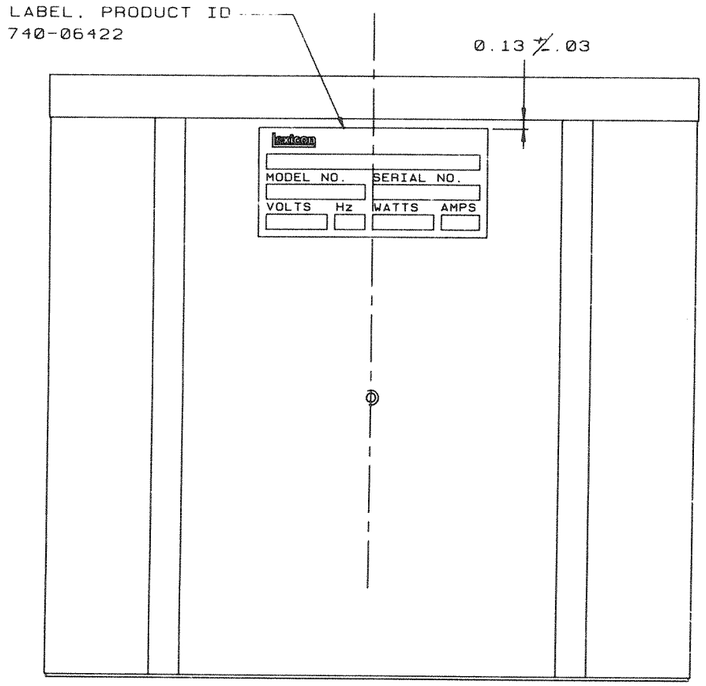
lexicon
100 BEAVER ST. WALTHAM, MA 02154

APPROVALS		DATE
DRAWN	TM	10/27/87
CHECKED	DS	10/27/87
ISSUED	DS	10/27/87
Q.C.	BH	10/27/87

TITLE SCHEMATIC, LXP - 1 PROCESSOR

SIZE	CODE	NUMBER	REV.
D		060-06016	2

SHEET 2 OF 5



BOTTOM VIEW

PARTS NOT SHOWN

PART #	DESCRIPTION
700-06543	RACK MOUNTING TRAY
070-06023	OWNER'S MANUAL
730-02813	REGISTRATION CARD
730-04346	WARRANTY CARD
730-06709	FOAM INSERT, TOP
730-06710	FOAM INSERT, BOTTOM
730-06741	SHIPPING BOX
730-06760	CLEAR SHIPPING BAG
470-06048	TRANSFORMER, 120V, 9VAC, 9VA

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
2	THIS SHT ADDED ECO# 880510-06		

NOTES

1. FRONT POT NUTS TO BE TIGHTENED TO 6-8 IN-LBS. FRONT SWITCH NUTS TO BE TIGHTENED TO 4 IN-LBS MAX. REAR PHONE JACK NUTS TO BE TIGHTENED TO 4-6 IN-LBS.

NEXT ASSY	USED ON		
APPLICATION		DO NOT SCALE DRAWING	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX +/-.010
.XXX +/-.005
MATERIAL
FINISH

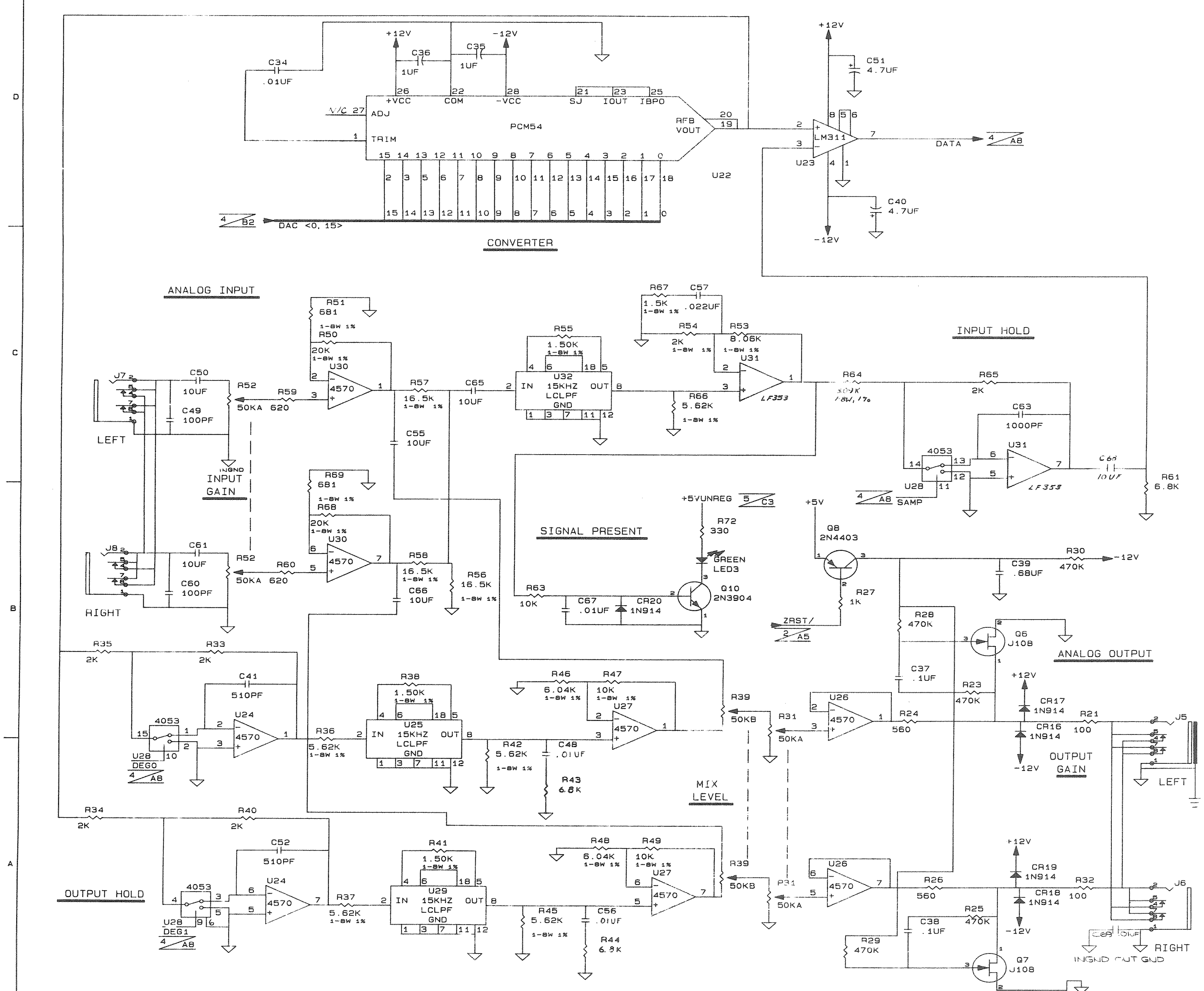
FILE NAME		
06613		
APPROVALS	DATE	
DRAWN		
CHECKED		
Q.C.		
ISSUED		

lexicon

TITLE ASSY DWG CHASSIS, LXP-1

SIZE	FSCM NO.	DWG. NO.	REV.
D		080-06613	2

SCALE 1/1 SHEET 2 OF 2



REVISIONS

REV	DESCRIPTION	DRAFTER/ CHECKER	Q.C./ AUTHORIZED
0	RELEASE FOR PROTOTYPE	TM 12/14/87 DS 12/14/87	DS 12/14/87 BH 12/14/87
1	PRODUCTION RELEASE	2-16-88	2-17-88
2	CHANGE PER ECO NO. 880225-00 SEE SHT NO. 3	3/16/88	3/28/88
3	CHANGE PER ECO NO. [illegible] CHANGE R62 TO C68, R64 [illegible] AND U31	3/16/88	[illegible]
4	CHANGE SHEET 4, [illegible] INSTALL C? & C24 PER ECO#880324-00, CHANGED DOC. CON. BLOCK. TITLES ON SHEETS 2-5 CHANGED.	J.V. 4/14/88	4/26/88
5	CHANGED SHEETS 1&3 PER ECO #880527-00	J.V. 6/24/88	6/27/88

NOTES

1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%, 1/4W.
2. UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V.
3. UNLESS OTHERWISE INDICATED, DIODES ARE 1N4148.
4. ANALOG GROUND, DIGITAL GROUND, CHASSIS GROUND, ANALOG PWR GND
5. A2 DENOTES SHEET NUMBER AND INTERSECT COORDINATE.
6. ON BOARD CONNECTION-TO; ON BOARD CONNECTION-FROM; SOLDER CONNECTION

DOCUMENT CONTROL BLOCK: #060-06016

SHEET NUMBER	REVISION NUMBER
1 OF 5	5
2 OF 5	2
3 OF 5	4
4 OF 5	2
5 OF 5	2

CONTRACT NO.

Lexicon
100 BEAVER ST. WALTHAM, MA 02154

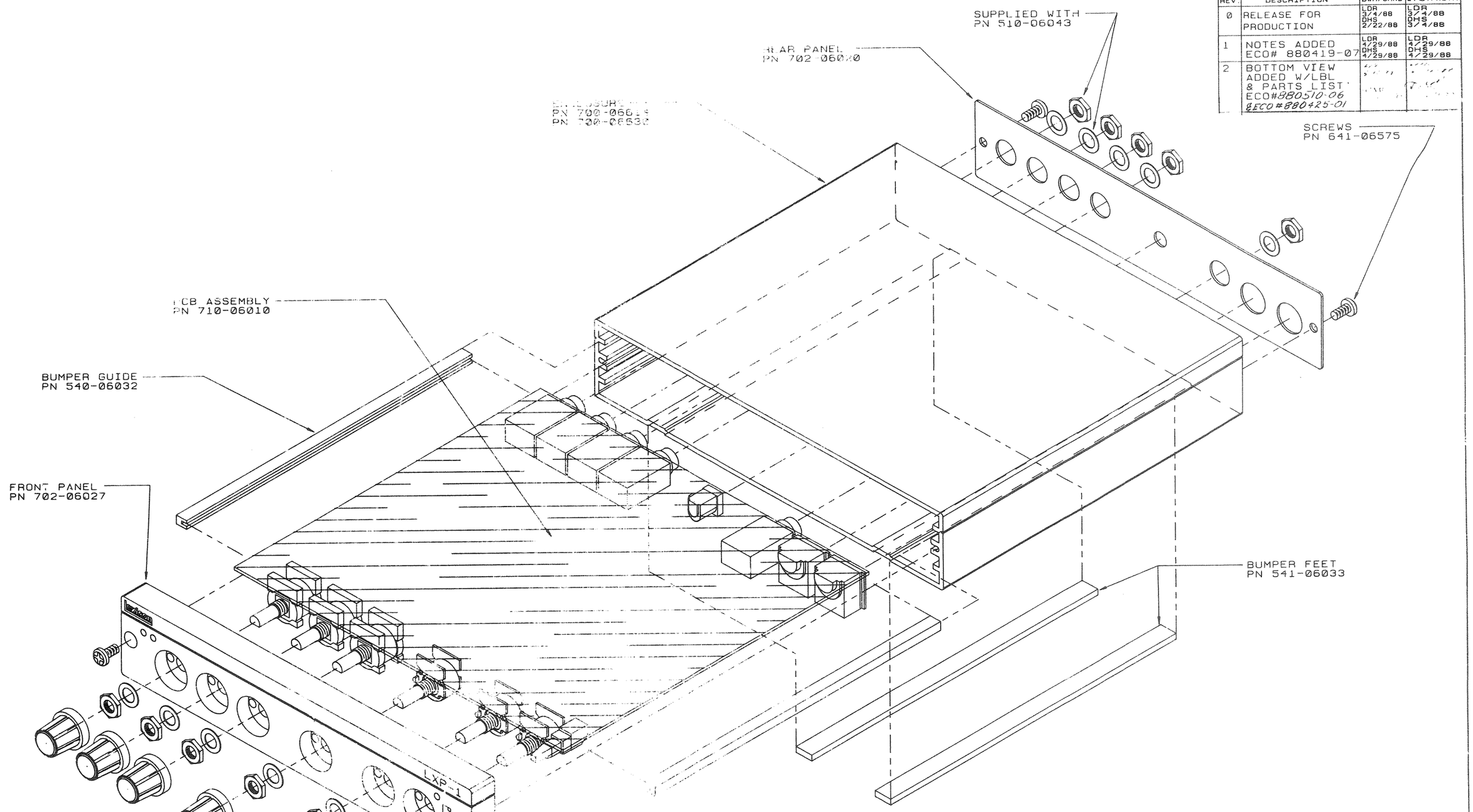
APPROVALS		DATE
DRAWN	TM	10/27/87
CHECKED	DS	10/27/87
ISSUED	DS	10/27/87
Q.C.	BH	10/27/87

TITLE: SCHEMATIC, LXP - 1 ANALOG AND CONVERTER

SIZE: D | CODE: | NUMBER: 060-06016 | REV. 5

SHEET 1 OF 5

REVISIONS			
REV.	DESCRIPTION	DWN/CHKD	Q.C./AUTH
0	RELEASE FOR PRODUCTION	LDR 3/4/88 DHS 2/22/88	LDR 3/4/88 DHS 3/4/88
1	NOTES ADDED ECO# 880419-07	LDR 4/29/88 DHS 4/29/88	LDR 4/29/88 DHS 4/29/88
2	BOTTOM VIEW ADDED W/LBL & PARTS LIST ECO#880510-06 &ECO#880425-01		



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX +/-.010 .XXX +/-.005	FILE NAME 06613	lexicon	
			APPROVALS / DATE	TITLE ASSY DWG, CHASSIS, LXP-1	
		MATERIAL	DRAWN LDR 1-17-88		
			CHECKED DHS 3-4-88	SIZE D	FSCM NO.
NEXT ASSY	USED ON	FINISH	Q.C. LDR 1-4-88	DWG. NO. 080-06613	REV. 2
APPLICATION		DO NOT SCALE DRAWING	ISSUED DHS 3-4-88	SCALE 1/1	SHEET 1 OF 2