MPX 1

Multi Processor FX

Service Manual

Lexicon

Unpacking and Inspection

After unpacking the MPX 1, save all packing materials in case you ever need to ship the unit. Thoroughly inspect the unit and packing materials for signs of damage. Report any shipment damage to the carrier at once; report equipment malfunction to your dealer.

Precautions

Save these instructions for later use.

Follow all instructions and warnings marked on the unit.

Always use with the correct line voltage. Refer to the manufacturer's operating instructions for power requirements. Be advised that different operating voltages may require the use of a different line cord and/or attachment plug.

Do not install the unit in an unventilated rack, or directly above heat producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.

Slots and openings on the case are provided for ventilation; to ensure reliable operation and prevent it from overheating, these openings must not be blocked or covered. Never push objects of any kind through any of the ventilation slots. Never spill a liquid of any kind on the unit.

This product is equipped with a 3-wire grounding type plug. This is a safety feature and should not be defeated.

Never attach audio power amplifier outputs directly to any of the unit's connectors.

To prevent shock or fire hazard, do not expose the unit to rain or moisture, or operate it where it will be exposed to water.

Do not attempt to operate the unit if it has been dropped, damaged, exposed to liquids, or if it exhibits a distinct change in performance indicating the need for service.

This unit should only be opened by qualified service personnel. Removing covers will expose you to hazardous voltages.

This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure... voltage that may be sufficient to constitute a risk of shock.

This triangle, which appears on your component, alerts you to important operating and maintenance instructions in this accompanying literature.

Notice

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to identify and Resolve Radio/TV Interference Problems."

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

Acknowledgements

Cry Baby, Leslie, Moog, Mutron and Vox are trademarked by their respective companies.

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING — The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION — The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.

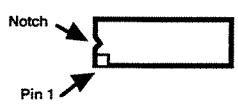
CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow to dry without rinsing.



CAUTION

ICs inserted backwards will be destroyed. Incorrect insertion of ICs is also likely to cause damage to the board.

Table of Contents

1

Product Overview

The Front Panel

Input/Output
Adjust analog input and output level.

Options
LED lights to indicate additional options exist for the displayed parameter. Press to access options. (LED will flash while options are displayed.) Press again to exit.

In Program mode, accesses database sorting selection.

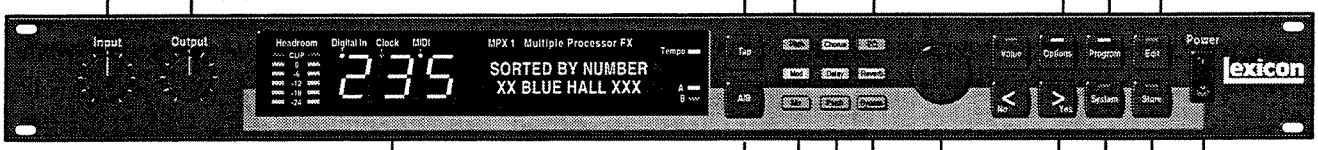
Program*
Activates Program Mode where you can select and load programs, see which effects are active in any program, and access a special set of soft parameters for the current program.

*In Autoload, displayed programs load automatically. In Manual mode, press Program to load any displayed program.

Effect Select: Pitch, Chorus, EQ, Mod, Delay, Reverb
Buttons light to indicate effect is active. In Program mode, pressing button turns off LED and bypasses effect. In Edit mode, pressing button selects effect parameters for editing.

Edit
Activates Edit mode, for access to all parameters of the currently loaded effect.

Tap
When Tempo LED is flashing, sets tempo. Press twice in rhythm to establish tempo rate. Press once to reset LFO.



Display
Digital In LED lights to indicate presence of digital input. The Clock LED lights to indicate digital signal lock. The MIDI LED lights to indicate incoming or outgoing MIDI data.

3-Digit Display indicates ID number of currently loaded program or patch.

6-position headroom indicator shows analog and digital signal levels and overload conditions.

Two rows of 16 characters display program and effect names, parameter names and values, and help and alert messages. An edit indicator shows edited effects.

Tempo LED flashes in time with current tempo rate when **Tap** is active.

A/B LEDs light to indicate A/B function is active.

A/B
Activates a variable glide between patched parameters.

Power
On/Off.

Store
Initiates program store function.

Patch
Accesses patch parameters.

System
Activates System mode parameters such as auto or manual load, MIDI dumps, I/O configuration, etc.

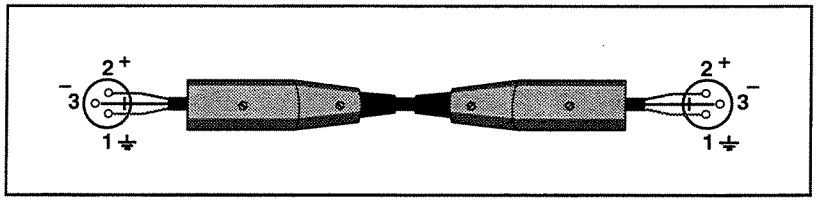
Mix
Instant access to mix and level parameters of any effect in the current program.

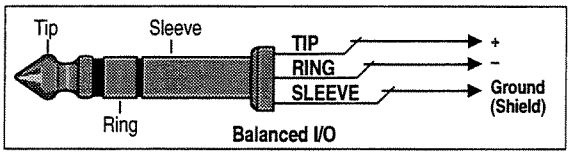
Bypass
Bypasses currently loaded program.

Value, **Knob** and < >
In Program mode, the knob selects programs, <and > jump through program categories. Pressing **Value** displays the Soft Row parameters of the currently loaded program. When **Value** is lit, the knob adjusts the value of the displayed parameter, < and > select other Soft Row parameters.

In Edit and System modes, **Value** assigns Select and Adjust functions to the knob or to the < > buttons. When **Value** is lit, the < > buttons select a parameter for modification and the knob adjusts the displayed parameter's value. When **Value** is off (unlit), the knob selects and the buttons adjust.

The Rear Panel



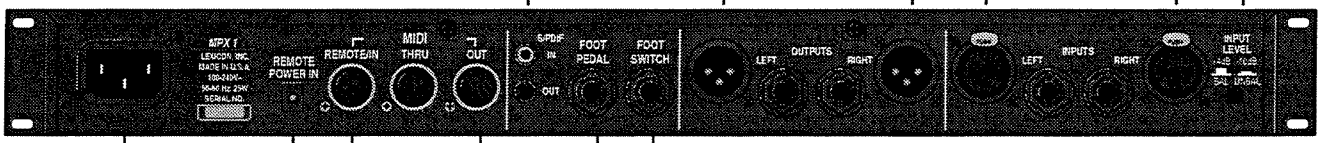


Balanced Inputs
Input impedance is 50kΩ unbalanced, and 100kΩ balanced. Inputs accept input levels from -14dBu to +20dBu. 1/4" phone connectors and XLRs provided.

Input Level
2-position (In/Out) switch for matching input gain to the source being used. The In position adds 12dB of input gain (unbalanced) to the input stages. Out position provides 0dB of gain (balanced).

Balanced Outputs
Output impedance is 600Ω, each side, balanced, and levels up to +18dBu maximum full scale. 1/4" phone connectors and XLRs provided.

S/PDIF
S/PDIF format digital connectors conform to CP-340 Type II consumer standards. (44.1kHz only)



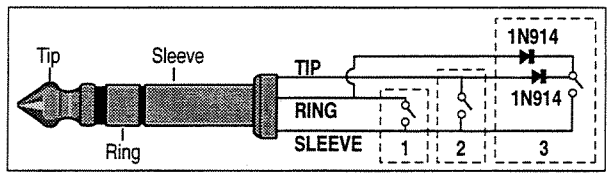
REMOTE POWER IN
2.5mm connector for 9 VAC MIDI remote power.

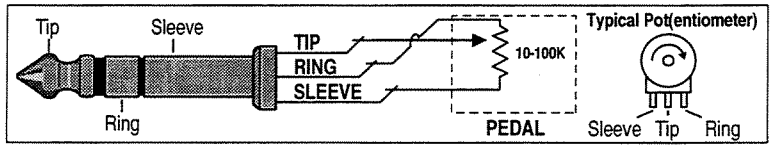
Foot Pedal
1/4" Tip/Ring/Sleeve phone jack provided for footpedal with 10kΩ to 100kΩ impedance.

AC Power
Standard 3-pin IEC power connector. 100-240V, 50-60Hz automatic switching to correct voltage range.

Foot Switch
1/4" Tip/Ring/Sleeve phone jack for three independent footswitches.

MIDI
IN
7-pin DIN connector for MIDI IN or powered bidirectional MIDI remote.
THRU
5-pin DIN connector passes any MIDI data received without change.
OUT
5-pin DIN connector transmits MIDI data to other equipment.





For control voltage input, use a 1/4" stereo plug with Sleeve connected to ground, Tip connected to the control voltage, and Ring unconnected.

Installation Notes

Mounting

The MPX 1 uses one EIA-standard rack space, and can be mounted on any level surface or in a standard 19 inch (483 mm) rack. If the unit is mounted in a rack or road case, support the rear of the chassis to prevent possible damage from mechanical shock and vibration.

The maximum ambient operating temperature is 104°F (40°C). Provide adequate ventilation if the unit is mounted in a closed rack with heat-producing equipment such as power amplifiers.

Power Requirements

The MPX 1 is equipped with a 3-pin IEC power connector and detachable cord. The unit will operate with power sources from 100 to 240 volts AC, 50-60Hz. Power switching to actual line voltage is automatic.

Audio Connections

Analog Audio

For best performance, maintain balanced connections, and use high-quality, low-capacitance, twisted-shielded pair cable.

When connecting MPX 1 outputs to single-ended, unbalanced devices, leave the low side floating and connect the grounds between the units.

Digital Audio

Connectors are provided for S/PDIF (CP-340 Type II) Consumer Digital Audio I/O. 75Ω coaxial cable suited for digital audio or video signals is required. Audio grade cable is *not* suitable. Only 44.1kHz signals are recognized.

Mono Applications: Using the MPX 1 Inputs with a Mono Source

Many of the programs in the MPX 1 are designed to process stereo input signals. These programs will also work and sound great with mono signals - but you need to configure the unit for mono. It will not automatically compensate for single-wire mono input connections.

There are two ways to use the MPX 1 in an installation where its inputs will be driven from a single, mono source:

- Use a Y-connector to send the signal to both inputs.
- Connect the mono signal to either the Left or Right input connector, then change the **System** mode **Audio Input Mode** parameter. If the Left input is connected, change the setting to **Mono (L only)**. If the Right input is connected, change it to **Mono (R only)**. The Mono settings of this parameter apply to the S/PDIF digital inputs as well. This allows you to select either the left or the right digital channel for processing.

NOTE

Individual programs can be optimized for mono input by simply inserting a mono effect, such as **Volume (M)**, into the first block of the routing map. See Chapter 3: *Editing* for more information on routing. See Chapter 7: *The Effects and Parameters* for more information on individual effects.

Internal Audio Data Paths	**Conversion:**	18 bit A/D, 20-bit D/A
	DSP:	32 bits
	S/PDIF I/O:	24 bits
Control Interface	**MIDI:**	7-pin DIN connector for MIDI IN/powered bidirectional remote 5-pin DIN connectors for MIDI THRU and OUT
	Footswitch:	1/4 inch T/R/S phone jack for 3 independent footswitches
	Foot pedal:	1/4 inch T/R/S phone jack (10kΩ min, 100kΩ max impedance)
	Remote Power In:	2.5mm barrel for 9VAC remote power
General	**Dimensions:**	19.0"W x 1.75"H x 9.0"D (483 x 45 x 289mm) 19 inch rack mount standard, 1U high
	Weight:	Net: 6lbs 2oz (2.8kg) Shipping: 9lbs 3oz (4.2kg)
	Power Requirements:	100-240VAC, 50-60Hz, 25W, 3-pin IEC power connector
	Environment:	Operating temperature: 32˚ to 104˚F (0˚ to 40˚C) Storage temperature: -22˚ to 160˚F (-30˚ to 70˚C) Humidity: maximum 95% without condensation
Electrical Approvals	**Safety Compliance:**	UL1419 and CSA 22.2 No. 1-94 (UL and C-UL marks) EN60065 (TUV-GS and CE marking per Directive 73/23/EEC)
	EMC Compliance:	FCC Class B EN55022 Class B and EN50082-1 (CE marking per Directive 89/336/EEC)

Specifications subject to change without notice.

3

Performance Verification

This section provides a procedure for quick verification of the normal operation of the MPX 1 internal processors and the integrity of the analog and digital audio signal paths. This procedure does not require removal of the MPX 1 covers.

Diagnostics

The MPX 1 contains three types of Diagnostics: Power On Diagnostics, Extended Diagnostics, and Emergency Diagnostics. Each of these is described fully in Chapter 4: Troubleshooting. When the MPX 1 is powered on, Power On Diagnostics run automatically to verify proper operation of its internal system. Power On Diagnostics consist of the following tests:

FPGA Test
Z80 CPU Test
ROM Checksum Test
Stack RAM Test
ADSP2115 Boot Ram Test
Lexichip-2 WCS Test
Hi SRAM Test (2115 SRAM Test)
Low SRAM (size) Test (Non destructive)
Lexichip 2/2115 Serial Audio Interface Test
Srate Test (Sample Rate Test)

Required Equipment

Low Distortion Oscillator with single-ended or balanced output, < 600Ω output impedance, <0.005% THD.

Distortion Analyzer and Level Meter with single-ended or balanced input, switchable 30kHz high pass filter or audio bandpass (20-20kHz) filter.

Oscilloscope

Footpedal with a 10-100kΩ range

Stereo footswitch T/R/S momentary closed style and cable

Cables:
Two shielded audio cables with 1/4" plugs on one end (T/S for single-ended, T/R/S for balanced) and appropriate connectors on the opposite ends for connection to Low Distortion Oscillator.

RCA male-to-male braided shield style cable

MIDI cable: 5 pin DIN, 3ft minimum

Analog Audio Performance

Setup

1. Turn on the MPX 1 and wait for the Power On Diagnostics cycle to finish.
2. Turn the front panel knob to select **200 Clean Slate**.
3. Press **Bypass** and verify that the button LED lights.
4. Connect an audio input cable between the Low Distortion Oscillator and the MPX 1 Left Input.
5. Set the rear panel BAL/UNBAL switch to UNBAL.
6. Connect an audio output cable between the MPX 1 Left Output and the Distortion Analyzer.
7. Set the Distortion Analyzer to measure VRMS.
8. Turn the MPX 1 front panel Input and Output knobs fully clockwise.

Check Signal Levels

1. Apply a 1kHz sinewave signal to the MPX 1 Left Input at .100VRMS. For Balanced, use .490VRMS input @ 1kHz, BAL switch set to +4dB (out).
2. Measure the Left output and verify a level between 2.06 to 3.0 VRMS. Balanced measurement is between 5.2 to 7.3VRMS.
3. Reconnect cables to the MPX 1 Right Input and Output and repeat steps 1 and 2.

Frequency Response Measurement

1. Disable all Filters on the Distortion Analyzer
2. Apply a 1kHz sinewave signal to the MPX 1 Left Input at .100VRMS. For Balanced, use .490VRMS input @ 1kHz, BAL switch set to +4dB (out).
3. Set the Analyzer for a 0dB reference (@ 1kHz).
4. Sweep the Oscillator from 20Hz to 20kHz and verify that the level stays within ±1dBr of the 0dB reference throughout the 20 to 20kHz sweep.
5. Reconnect the cables to the MPX 1 Right Input and Output and repeat steps 1-4.

THD+N Measurement

1. Apply a 1kHz sinewave signal to the MPX 1 Left Input at .100VRMS. For Balanced, use .490VRMS input @ 1kHz, BAL switch set to +4dB (out).
2. Set Analyzer to measure THD.
3. Set the MPX 1 rear panel BAL/UNBAL switch to +4dBu (out position).
4. Enable Low pass Filter (30kHz , 20kHz)
5. Measure and verify the Left Output THD+Noise level on the Analyzer, for a reading of < 0.010%.
6. Reconnect the cables to the MPX 1 Right Input and Output and repeat steps 1-4.
7. Return the MPX 1 rear panel BAL/UNBAL switch to UNBAL (in position).

Signal To Noise Ratio

1. Set Analyzer for a 0dB reference at 1kHz.
2. Remove phone plug from the MPX 1 input.
3. Enable the low pass filter (30 KHz , 20 KHz).
4. Measure noise at the left ouput and verify that the level is <-72dB.
5. Move the cable from the Left output to the Right output and verify a level of <-72dB.

Crosstalk Left

1. Enable the Lo pass filter (30kHz, 20kHz).
2. Apply a 1kHz sinewave signal to the MPX 1 Right Input at .100VRMS. For Balanced, use .490VRMS input @ 1kHz, BAL switch set to +4dB (out])
3. Connect the Left output to the Distortion Analyzer .
4. Set the Analyzer to measure level.
5. Sweep the Oscillator from 20Hz to 20kHz and verify that the level stays <.010 VRMS throughout the sweep range.

Crosstalk Right

1. Apply a 1kHz sinewave signal to the MPX 1 Left Input at .100VRMS. For Balanced, use .490VRMS input @ 1kHz, BAL switch set to +4dB (out).
2. Connect the MPX 1 Right Output to the Distortion Analyzer .
3. Set the Analyzer to measure level.
4. Sweep the Oscillator from 20Hz to 20kHz and verify that the level stays <.010 VRMS throughout the sweep range.

Digital I/O Functionality

This test verifies the MPX 1 S/PDIF input and output circuit by transmitting data out the S/PDIF output, then attempting to read the data coming back in through the S/PDIF input.

1. Connect the RCA cable between the MPX 1 S/PDIF Input and the S/PDIF Output.
2. Press and hold **Edit** while powering up the MPX 1.
3. Release **Edit** when **Lexicon** is displayed. After a few seconds, the display will show:

   Diags:Test
   Switch Test

4. Turn the front panel knob clockwise until the display shows:

   Diags:Test
   Dig Audio Test

5. Press the **Store** button (which should be flashing.)
6. If the test passes, the display will show:

   Dig Audio Test
   Passed

MIDI Functionality

This test will quickly verify that the MPX 1 MIDI circuitry transmits and receives MIDI data.

1. Connect one end of the MIDI cable to the MPX 1 MIDI OUT jack and the other end to the MPX 1 Remote/In jack.
2. Press and hold **Edit** while powering up the MPX 1.
3. Release **Edit** when **Lexicon** is displayed. After a few seconds, the display will show:

   Diags:Test
   Switch Test

4. Turn the front panel knob clockwise until the display shows:

   Diags:Test
   MIDI Test

5. Press the **Store** button (which should be flashing.)
6. If the test passes, the display will show:

   MIDI Test
   Passed

Footpedal Functionality

This test analyzes the data generated by the ADC circuitry during the sweep (0VDC to +5VDC) of a footpedal and confirms that the circuit is accurately reporting the voltage to the ASDP2115 Processor.

1. Connect the footpedal to the MPX 1 rear panel Foot Pedal jack and put the pedal to its up position.
2. Press and hold **Edit** while powering up the MPX 1.
3. Release **Edit** when **Lexicon** is displayed. After a few seconds, the display will show:

   Diags:Test
   Switch Test

4. Turn the front panel knob clockwise until the display shows:

   Diags:Test
   Footpedal Test

5. Press the **Store** button (which should be flashing.)
6. Within five seconds, move the pedal over its entire range (min to max).
7. If the test passes, the display will show:

   Footpedal Test
   Passed

Footswitch Functionality

This test will quickly verify that the MPX 1 footswitch circuitry is functional.

1. Connect the footswitch to the MPX 1 rear panel Footswitch jack.
2. Press and hold **Edit** while powering up the MPX 1.
3. Release **Edit** when **Lexicon** is displayed. After a few seconds, the display will show:

   Diags:Test
   Switch Test

4. Press the **Store** button (which should be flashing.) The display will show:

   Switch Test
   Hold < to exit

5. Press and hold one of the switches on the footswitch. Depending on which switch is depressed, one of the following messages will be displayed.

   Foot SW1 Tip **OR** **Foot SW2 Ring**
   Pressed **Pressed**

   When the switch is released, the lower line of the display will change from **Pressed** to **Released**.
6. Repeat step 5 for the remaining switch.

Listening/QC

Required Equipment

Clean, antistatic, well lighted work area

Low distortion sine wave oscillator

Headphone Amplifier

Two audio cables, shielded, with 1/4" (or XLR) plugs on one end and appropriate connectors on the opposite ends for connection to the Low Distortion Oscillator.

Two audio cables, shielded, with 1/4" (or XLR) plugs on one end and appropriate connectors on the opposite ends for connection to the headphone amplifier.

Stereo Headphones

Setup

1. Connect two audio cables between the outputs of the Low Distortion Amplifier and the MPX 1 Left and Right inputs.
2. Connect two audio cables between the headphone amplifier inputs and the MPX 1 Left and Right outputs.
3. Set the oscillator for 220Hz at .100VRMS.
4. Turn the volume control on the headphone amplifier completely counter-clockwise, and plug in the stereo headphones.
5. Power up the MPX 1. Turn the front panel knob to select and load **1 MPX Blue**.

Verify Clean Audio

1. Put headphones on.
2. Turn the MPX 1 front panel Input control fully clockwise.
3. Slowly increase the volume on the headphone amplifier to a comfortable listening level.
4. Adjust the Input knob over its entire range and verify that no pops, clicks or static noises are heard when turning the knob.
5. Adjust the MPX 1 Input so the 0 level LED just turns on.
6. Adjust the volume on the headphone amplifier to a comfortable listening level.
7. Mute and unmute the signal source at different frequencies. Listen carefully to the outputs for unusual noise, distortion or other irregularities through the entire decay time of the reverb.

Shock Test

1. Lift one corner of the MPX 1 four inches off the workbench and drop.
2. Verify that no audio or display intermittence are caused by this action.
3. Repeat for each of remaining three corners of the unit.

Keep one corner of the unit touching the bench at all times to prevent damage to the unit.

4

Troubleshooting

Diagnostics

The MPX 1 contains three types of diagnostics: Power On Diagnostics, Extended Diagnostics, and Emergency Diagnostics. Each of these is described in this chapter.

Power On Diagnostics

On normal power up, the MPX 1 will automatically execute a set of tests which comprise the Power On Diagnostics. As the test sequence begins, all LEDs and the top row of pixels in the display will turn on for approximately two seconds. On successful completion of the tests, the display will cycle to the state it was in when the MPX 1 was last powered off.

Error Indication

If any of the Power On Diagnostic tests fail, an error message will be displayed on the front panel as shown in the example below.

The left Headroom Clip LED will light to indicate an error condition. The remaining LEDs in the left Headroom column are used to display a binary error code.

The corresponding decimal error code may also be displayed on the numeric display.

The binary error code represented by the LEDs in our example is read as follows:

0dB	-6dB	-12dB	-18dB	-24dB		
0	0	1	0	0	=	Binary Code 4

The sequence of tests and their corresponding test codes are as follows:

Error #	Test
NA	FPGA
NA	Z80 CPU Test
1	ROM Checksum Test
2	Stack RAM Test
3	ADSP2115 Boot RAM Test
4	Lexichip-2 WCS Test
5	Hi SRAM Test (2115 SRAM)
6	Low SRAM Test (Non destructive)
7	Lexichip-2 2115 Serial Audio Test
8	SRATE Test (Sample Rate)

Test Descriptions

FPGA Test

This test verifies that the address and data lines are functional. If this test passes, the DONE signal line on U15 pin 55 will go high causing RESET1/ signal to go high, allowing the Z80 (U24) to boot.

In the event of failure, the CPU will not be able to display any messages. The MPX 1 will not function and service will be needed.

Z80 CPU

This test checks for stuck CPU register bits. The Z80 passes a value through its internal registers, then reads the value to verify that data sent matches data received.

In the event of failure, the CPU will not be able to display any messages. The MPX 1 will not function and service will be needed.

01 ROM Checksum Test

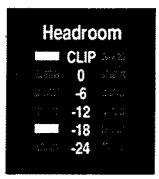
The ROM Checksum, which is a byte size value, is located in the last location of Bank 0. The test adds the entire ROM, including the Checksum byte, expecting 0 as a result.

Failure is displayed as follows:

02 Stack RAM Test

This test checks a portion of the volatile area of the Z80 High SRAM (U21 address 7E00-7FFF) and verifies that this portion of the SRAM is available as a temporary storage location for subsequent diagnostic tests.

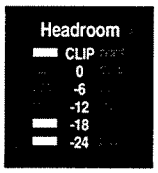
Failure is displayed as follows:



03 ADSP2115 Test

This test verifies that the Lexichip-2 crystal oscillator and Resonator are working. It also verifies that the frequencies are within their tolerances. (Lexichip-2=22.576942MHz to 22.581457MHz; Resonator=11.059403MHz to 11.224469MHz).

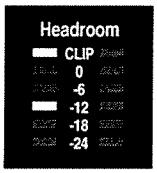
Failure is displayed as follows:



04 WCS Test (Writeable Control Store)

This test checks the program memory space (writeable control store) of the Lexichip-2 (U17). The RAM (memory space) is first filled with the value 55 hex (0101 0101 binary), then each memory location is read to see if it contains 55. If 55 is in the memory location, the location is then filled with AA hex (1010 1010 binary), and the next location is processed. The process is then repeated, checking for AAs, then storing 0s into the memory. On completion, an address test verifies that all address lines are active and the memory is checked for 0s.

Failure is displayed as follows:



05 Hi SRAM Test

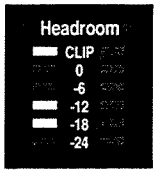
The Hi SRAM Test is performed by the ADSP2115 (U20). The tests performed on the SRAM are identical to those performed by the WCS Test on the RAM.

Failure is displayed as follows:

06 Lo SRAM Test

This test erases the memory on the lower half of the SRAM (U26) and does a non erasable test on the upper half (not touching the volatile SRAM area). The non erasable test checks one location at a time, saving the contents in register and then restoring the values.

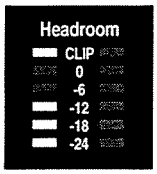
Failure is displayed as follows:



07 Lex-2115 Test (Serial Audio Test)

This test verifies serial audio communication between the ADSP2115 (U20) and Lexichip-2 (U17). The ADSP2115 sends a value to the Lexichip-2 and then reads the value back to verify that the data sent matches the data received. The Lexichip-2 is loaded with an I/O program that feeds the value it receives back to the ADSP2115 unprocessed.

Failure is displayed as follows:



08 Sample Rate Test

This test checks the relative frequencies (±100ppm) of the DSP (U20) master clock and the sample rate (44.1kHz). In this test, the DSP counts samples, and returns the average sample period in nanoseconds (22669–22681ns).

Failure is displayed as follows:

Extended Diagnostics

Extended Diagnostics are provided for to verify specific MPX 1 functions.

To enter Extended Diagnostics, power on the unit while pressing down the front panel **Edit** button. Continue holding **Edit** until **Lexicon** is displayed. Release **Edit**. Within approximately five seconds, the display will show:

Diags: Test
Switch Test

Turn the front panel knob to select any of the Extended Diagnostics tests listed below:

Switch
LED
LCD Char
LCD Block
Auto*
Burn In Loop
Footpedal*
MIDI*
Dig Audio
DRAM
Resonator
WCS
SRAM
ROM

* These tests are designed for Lexicon manufacturing use only. They require custom equipment which is not available for sale.

The display of any test selects it for execution, and causes the front panel **Store** button to flash. Pressing **Store** executes the displayed test.

To exit Extended Diagnostics without powering down the MPX 1:

1. Press the front panel button labeled **< No**. The display will show:

Diags: Top Level
Tests

2. Turn the knob clockwise until the display shows:

Diags: Top Level
Exit Diags

3. Press **> Yes** to exit Extended Diagnostics and return the MPX 1 to normal operating mode.

Test Descriptions

The first four Extended Diagnostics tests (Switch, LED, LCD Char and LCD Block) require operator interaction. These tests do not generate any error messages.

Enter **Extended Diagnostics** by powering on the unit while pressing down the front panel **Edit** button. Continue holding **Edit** until **Lexicon** is displayed. Release **Edit**. Within approximately five seconds, the display will show:

Diags: Test
Switch Test

Switch Test

This test allows you to check the front panel encoder and all front panel switches, as well as footswitches.

When a front panel switch is pressed, the upper line of the display will identify the switch (Encoder, Tap Button, etc.). The lower line will indicate **Pressed** or **Released** depending on the state of the switch.If the switch is held down for more than one second, the display will indicate **Held.**

Footswitches are verified in the same manner, but will only indicate **Pressed** or **Released** as appropriate.

Turning the front panel encoder clockwise or counterclockwise is verified on the display by the messages **Encoder <> CW** and **Encoder <> CCW**. Note that this test verifies only the direction of the encoder. The LED test is used to verify that the 36 encoder positions are working.

To exit, press and hold **< No** until the display shows:

Switch Test
Hold < to exit

LED Test

This test verifies that all 54 front panel LEDs and all 36 encoder positions are working.

Turning the front panel encoder clockwise will light each LED individually, beginning with the LED in the **Pitch** button and ending with the **MIDI** indicaotr in the numeric display. Turning the encoder clockwise beyond the last test will have no effect and no LEDs will light.

To exit, press and hold **< No** to return to the **LED Test** display.

LCD Character Test

This test verifies that all display segments are working.

Turning the front panel encoder clockwise will cause each display block to display a single character, then to step through the alphabet to numbers 0-9, and several ASCII characters.

To exit, press and hold **< No** to return to the **LCD Char Test** display.

LCD Block Test

This test turns on all the pixels of a single display block.

Turning the front panel encoder clockwise one step will cause a display block to appear at the top left corner of the LCD. The display block increments or decrements, effectively walking the block each time the encoder is turned. After the lower right display block is tested, turning the encoder once more position lights all of the display blocks. Turning the encoder clockwise another step turns all of the display blocks off.

To exit, press and hold **< No** to return to the **LCD Block Test** display.

Auto Test

This test is for Lexicon manufacturing use only. The test requires custom test fixtures which are not available for sale. Refer to Chapter 3 Performance Verification for equivalent testing without this equipment. Qualified distributors, contact Lexicon Customer Service for more information.

Required Equipment

- 1 MIDI Comparator Fixture (P/N 770-90096)
- 1 Remote Power In Power Supply Tester (P/N 770-90097)
- 1 Foot Controller Test Fixture (P/N 770-08508)
- 1 MIDI cable 5 pin male to 5 pin male, 3 ft minimum
- 1 MIDI cable 7 pin male to 7 pin male, 3 ft minimum
- 1 RCA cable male to male braided shield

Connections

1. Connect the 5 pin MIDI cable between the MPX 1 rear panel MIDI Out jack and the MIDI In jack of the MIDI Comparator Fixture.
2. Connect the 7 pin MIDI cable between the MIDI Comparator Fixture MIDI Out jack and the MPX 1 rear panel MIDI Remote/In jack.
3. Insert the single ended plug from the Remote Power Supply Tester into the MPX 1 rear panel Remote Power In jack.
4. Connect the RCA cable between the MPX 1 rear panel S/PDIF In and the S/PDIF Out jacks.
7. Connect the Foot Controller Test Fixture to the MPX 1 rear panel Foot Pedal jack.

Procedure

1. Enter **Extended Diagnostics** by powering on the unit while pressing down the front panel **Edit** button. Continue holding **Edit** until **Lexicon** is displayed. Release **Edit**. Within approximately five seconds, the display will show:

   Diags: Test
   Switch Test

2. Turn the front panel knob until **Auto Test** is displayed. The **Store** button will flash and the **Options** buttons will light.
3. Press **Store** to execute the following tests.

   Footpedal Test
   MIDI Test
   Dig Audio Test
   Resonator Test

On successful completion of all of the tests, the display will show:

Auto Tests
Passed

and automatically exit to the **Extended Diagnostics** menu.

If a failure occurs, the MPX 1 will halt on the test that failed, displaying the name of the test on the upper line of the display and **Failed** on the lower line.

Burn-In Loop Test

When Store is pressed, the following tests will run continuously.

ROM checksum test
Hi SRAM Test
Low SRAM Test
Lexichip-2 WCS Test
ADSP2115 Lexichip-2 Serial Audio Interface Test
Lexichip-2 DRAM Test

The display will show the name of each test as it cycles through the loop. The Left Headroom LEDs will flash during the DRAM test.

If a failure occurs, the MPX 1 will stop the test cycle and display the name of the failed test.

To exit the loop, press and hold **>Yes**. As the currently running test will be completed before the exit command takes effect, this may take as long as 37 seconds. On exiting, the display will indicate the number of times the cycle was successfully completed.

Footpedal Test

Required Equipment
1 Lexicon Custom Foot Controller Test Fixture (P/N 770-08508)

This test is for Lexicon manufacturing use only. The test requires custom test fixtures which are not available for sale. Refer to Chapter 3 Performance Verification for equivalent testing without this equipment. Qualified distributors, contact Lexicon Customer Service for more information.

The Foot Controller Test Fixture contains an LFO that will sweep the Controller input from its minimum value (0VDC) to its maximum voltage (+5VDC) then back to its minimum value. The test analyzes the data generated by the ADC circuitry during the sweep and confirms that the circuit is accurately reporting the voltage to the ASDP2115 Processor.

Procedure

1. Enter **Extended Diagnostics** by powering on the unit while pressing down the front panel **Edit** button. Continue holding **Edit** until **Lexicon** is displayed. Release **Edit**. Within approximately five seconds, the display will show:

   Diags: Test
   Switch Test

2. Turn the front panel knob until **Footpedal Test** is displayed.
3. Press the flashing **Store** button to execute the test. The display will indicate **Passed** or **Failed** when the test is completed.

To exit, press **< No**, then press **> Yes**.

MIDI Test

This test is for Lexicon manufacturing use only. The test requires custom test fixtures which are not available for sale. Refer to Chapter 3 Performance Verification for equivalent testing without this equipment. Qualified distributors, contact Lexicon Customer Service for more information.

Required Equipment

1 MIDI Comparator Fixture (P/N 770-90096)
1 Remote Power In Power Supply Tester (P/N 770-90097)
1 MIDI cable 5 pin male to male style, 3 ft minimum
1 MIDI cable 7 pin male to male style, 3 ft minimum

Connections

1. Connect the 5 pin MIDI cable between the MPX 1 rear panel MIDI Out jack and the MIDI In jack of the MIDI Comparator Fixture.
2. Connect the 7 pin MIDI cable between the MIDI Comparator Fixture MIDI Out jack and the MPX 1 rear panel MIDI Remote/In jack.
3. Insert the single ended plug from the Remote Power Supply Tester into the MPX 1 rear panel Remote Power In jack.

Procedure

1. Enter **Extended Diagnostics** by powering on the unit while pressing down the front panel **Edit** button. Continue holding **Edit** until **Lexicon** is displayed. Release **Edit**. Within approximately five seconds, the display will show:

   Diags: Test
   Switch Test

2. Turn the front panel knob until **MIDI Test** is displayed.
3. Press the flashing **Store** button to execute the test.. The display will indicate **Passed** or **Failed** when the test is completed.

To exit, press **< No**, then press **> Yes**.

Dig Audio Test

The test transmits data out of the S/PDIF output jack and reads the data coming back in through the S/PDIF input jack to verify functioning of the S/PDIF input output circuit.

To run this test, connect an RCA cable (male to male braided shield style) between the MPX 1 rear panel S/PDIF In and the Out jacks.

Select **Dig Audio Test** from the **Extended Diagnostics** menu and press **Store.** The display will indicate **Passed** or **Failed** when the test is completed.

To exit, press **< No**, then press **> Yes**.

DRAM Test

This test sets the Lexichip-2 (U17) into a mode that allows the Z80 (U24) to read and write to the 256K X 16 Dram (U25) and 256K X 4 Dram (U26) through the Lexichip-2 During this test the Z80 will write "AAAA" data into all the memory locations then read them back. It will repeat this test again by writing "5555" data. A second part of the test will check the address. The Z80 writes a count into the memory then reads it back. This test takes approximately 37 seconds to run, during which time the display will show:

DRAM Test
Running...

When the test is finished, the display will indicate **Passed** or **Failed**.

To exit, press < **No**, then press > **Yes**.

Resonator Test

This test checks the low to high range frequency of the resonator and verifies that it is within the sample rate tolerance of 44056-44144 Hz (±1000 ppm). It does this by setting the PHASE_DET low. This signal goes to the input of the Phase Detector circuit (PDC) and will cause the output (PLLV) of the (PDC) to go low (0 VDC), when it is in this state. The VCO frequency (11.3MHz) is measured by the ADSP2115 (U15) to verify it is within the rated tolerance. If the resonator is not within this tolerance, the CPU will report the test as failed.

When the test is finished, the display will indicate **Passed** or **Failed**.

To exit, press < **No**, then press > **Yes**.

WCS Test In Extended Diagnostics

This test checks the program memory space In the WCS of the Lexichip-2 (U17). RAM memory space is first filled with the value 55 hex (0101 0101 binary), then each memory location is read to see if it contains 55. If it is found in memory, it is then filled with AA hex (1010 1010 binary), and the next location is tested. Once the RAM has been checked for 55s and then filled with AAs, the process is then repeated checking for AAs, then storing 00s into memory. An address test verifies that all address lines are active. Finally the memory is checked for 0s.

When the test is finished, the display will indicate **Passed** or **Failed**.

To exit, press < **No**, then press > **Yes**.

Low SRAM Test In Extended Diagnostics
This test first clears the memory on the lower half of the SRAM (U22) and then does a non destructive test on the upper half, without touching the volatile SRAM. The nondestructive test checks one location at a time, saving the contents in a register and restoring the value when it is done.

When the test is finished, the display will indicate **Passed** or **Failed**.

To exit, press **< No**, then press **> Yes**.

ROM Checksum Test In Extended Diagnostics
In this test, the ROM checksum, which is a byte size value, is located in the last location of Bank 0. The test adds up the entire ROM including the checksum byte. The result should be zero (an 8 bit value).

When the test is finished, the display will indicate **Passed** or **Failed**.

To exit, press **< No**, then press **> Yes**.

Top Level Menu Utilities & Tools
The following utilities and tools provide more in-depth information on specific tests and help troubleshoot the MPX 1 during repair.

Exit Diags
Scope Loops
Test Results
View DRAM
View Err Log*
Clear Err Log*
2115 Tools*
MIDI Scope
Preset Dumps*

* These utilities are for factory use only.

When these Utilities and Tools are executed, the front panel **Options** button will light to indicate that it is active. Pressing **Options** allows the Test or loops in the MPX 1 to be run 1-254 times or continuously, making troubleshooting easier.

To enter the Top Level Menu, press and hold **Edit** while powering on the MPX 1. Release **Edit** when the display reads **Lexicon**.

Within 5 seconds the display will show:

Diags: Test
Switch Test

Press **< No.** The display will show :

Diags: Top Level
Tests

Turn the front panel encoder clockwise to select any of the available utilities and tools. Press **> Yes** to activate your selection.

Exit Diags
This utility provides a way to exit Extended Diagnostics without powering off the MPX 1. Press **> Yes** to exit and resume normal MPX 1 operation.

Scope Loops
This tool sets the MPX 1 into any of the following looping modes for troubleshooting.

Lexichip Scope
Z80-Lex Wr Test
LCD Read
LCD Write

Pressing **Options** in any of these Loops displays:

Repeat Test
1 times

Turn the front panel encoder once counterclockwise to select **Infinite Loops** or turn it clockwise to select **1-245.** As certain problems require time to troubleshoot, we recommend selecting **Infinite Loops.** Press **Options** to confirm your selection, then press **Store** to start the loop.

To exit a test which has been set to run more than once, press **> Yes.**

Lexichip Scope
Press **> Yes** to display the first Scope Loop selection: **Lexichip Scope**. Press **Store** to run the loop once. After one cycle, the display will show:

Diags: Scope Loop
Done...

Press **Options** and use the encoder to select **1-245**, or **Infinite Loops**.

Z80-Lex Wr
Press **Store** to run the loop once. Press **Options** and use the encoder to select **1-245**, or **Infinite Loops**.

LCD Read
Press **Store** to run the loop once. Press **Options** and use the encoder to select **1-245**, or **Infinite Loops**.

LCD Write
Press **Store** to run the loop once. Press **Options** and use the encoder to select **1-245**, or **Infinite Loops**.

Test Results
This utility will store the Pass/Fail status of the last test that was run. It will provide detailed information including data sent, data received, and the address.

This utility can be used for the following test. (Note that the test numbers are different than the ones assigned for Power On diagnostics.)

07	Footpedal
08	MIDI Wraparound
10	DRAM (U25& U26)
11	Resonator
12	WCS
14	ROM Checksum

As each of the six tests reports different information, an example of an instance of failure for each one is described below.

7 Footpedal Failure

When the test fails, the MPX 1 displays:

Last Test Failed
< > # times

The # indicates the number of times the test failed.

Pressing **> Yes** may call the following display:

Test #7 A: 13B7
S: 0000 R: 0000

Here the address field (A) contains the number 13B7. This is the last DC voltage the ADC (U2) and its associated circuitry read. The value is in hexadecimal form and must be converted to decimal notion, which can be performed on any scientific calculator with these functions. After the value has been converted to decimal it must be divided by 2500 to indicate the last read DC voltage.

13B7 (hex) = 5047 (dec)
5047/2500 = 2.0188 VDC

8 MIDI Wraparound Failure

When the test fails, the MPX 1 displays:

Last Test Failed
< > # times

The # indicates the number of times the test failed.

Pressing **> Yes** may call the following display:

Test #8 A: 0002
S: 00FF R:0000

In this test the address fields A: and data S: are used. In the above example, the MPX 1 has sent out 1 byte of information S: 00FF and has reported error 0002 in the A: field. Following is a list of the errors and their meaning .

#	Error	Suspect Components
1	Transmit Time-out	FPGA U15 and associated circuitry
2	Receive Time-out	FPGA U15 and associated circuitry
3	Frame Error	FPGA U15 and associated circuitry
4	Bad Data	FPGA U15 and associated circuitry

10 DRAM Failure

When the test fails, the MPX 1 displays:

Last Test Failed
< > # times

The # indicates the number of times the test failed.

Pressing > **Yes** may call the following display:

55 Test A: 0002
S: 55555 R:55551

In this test all 3 fields are used for display of information. In this example, data was sent as S: 55555 and received back as R: 55551. Because what was sent was not the same as received, a failure has been detected and the address that is bad is indicated by A: 40000 .

This information will point to which DRAM is at fault, U25 bits LD4–LD19 or U26 bits LD0–LD3 . The information is in Hex form that must be converted to Binary.

	Hex	Binary	bad nibble	
Data Sent S:	55555 =	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 1 01	
Data Received R:	55551 =	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0	0 1	LSB
		MSB LDbit 19	Bad LDbit 2	LDbit 0

The Data sent and received in the nibble as indicated are different. Bit 2 is bad because the level sent for bit 2 was 1 but the level received was 0. Therefore, the test indicates DRAM U26 or its associated circuitry may be faulty.

Following is a list of failures if one of the LABUS0– LABUS8 address lines are detected by the DRAM tests.

Address	Data Sent	Data Received	Cause
LABUS0	S: 0000F	R: FFFF0	Short to ground
LABUS1	S: 0000F	R: 0202F	Short to ground
LABUS2	S: 0000F	R: 0404F	Short to ground
LABUS3	S: 0000F	R: 0808F	Short to ground
LABUS4	S: 0000F	R: 1010E	Short to ground
LABUS5	S: 0000F	R: 2020D	Short to ground
LABUS6	S: 0000F	R: 4040B	Short to ground
LABUS7	S: 0000F	R: 80807	Short to ground
LABUS8	S: 40404	R: 10101	Short to ground

11 Resonator Failure

When the test fails, the MPX 1 displays:

Last Test Failed
< > # times

The # indicates the number of times the test failed.

Pressing > **Yes** may call the following display:

Test#11 A: 5916
S: 0132 R:0000

In this test, the address field A: will contain the information for the failure. The example shows the Resonator Frequency A:5916 as a Hexadecimal value which has to be converted to decimal notation. Using a scientific calculator that converts Hex to Decimal you will find Hex 5916=Decimal 22806.

This value is divided by 1000 to get the proper sample period in microseconds (22806/1000=22.806µs (sample rate). The sample rate is divided by 256 (22.806/256=0.089085937), then divided into 1 to get the frequency in MHz (1/ 0.089085937=11.2251162 MHz).

This is the Resonator frequency reported by the test.

12 WCS Failure

When the test fails, the MPX 1 displays:

Last Test Failed
< > # times

The # indicates the number of times the test failed.

Pressing **> Yes** may call the following display:

Test#12 A: 5000
S: 5000 R:5008

In this test all three fields are used for display of information. In our example, data was sent as S: 5000 and received back as R: 5008.

The information is in Hex form and must be converted to Binary.

	Hex	Binary	bad nibble
Data Sent S:	5000 =	0 1 0 1 0 0 0 0 0 0 0 0	0 0 0 0
Data Received R:	5008 =	0 1 0 1 0 0 0 0 0 0 0 0	1 0 0 0

MSB LDbit 15 — Bad LDbit 3 — LSB LDbit 0

This indicates WCS Address line LA3 of the Lexichip or the associated circuitry is suspect.

14 ROM Checksum Failure

When the test fails, the MPX 1 displays:

Last Test Failed
< > # times

The # indicates the number of times the test failed.

Pressing **> Yes** may call the following display:

Test#14 A: 5000
S: 5000 R:5001

This error message indicates ROM U23 is suspect.

View DRAM
Pressing > **Yes** will show:

Address: 000000
Data: 00000

The information in the display reports the data stored in the DRAMs (U25 and U26). Turning the front panel encoder clockwise displays all 256 memory address locations

As an example, if address LD2 were bad, the display would show:

Adress: 000000
Data: 55551

View Err Log
This utility is for factory use only.

Clear Err Log
This is used to Clear the Error log. This utility is for factory use only.

2115 Tools
This utility is for factory use only.

MIDI Scope
Pressing > **Yes** will show:

offset: -0 7800
34 69 C3 F3 00

This utility monitors incoming MIDI data. The display shows the following information:

offset: -0 7800	Scrolls through the data 0 - 256. Displays the last address sent to in.
32 6F C3 F3 00	MIDI Data received. Last byte entered is displayed here and moves to the left each time a byte is entered

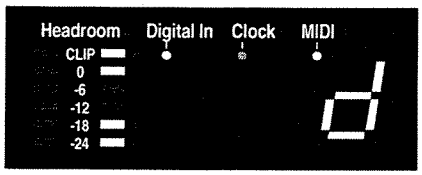
View Alg Nums
This utility is for factory use only.

Preset Dump
This utility is for factory use only.

Emergency Diagnostics

Emergency Diagnostics are used when the MPX 1 display fails to light on power up, is garbled or does not respond to the encoder being turned or buttons pushed.

To access Emergency Diagnostics, press and hold **Store** while powering up the MPX 1. The following display will appear.



The **d** on the display indicates that the unit is in Emergency Diagnostics mode. When this display appears, release the **Store** button.

The right column of the Headroom display will have the -24, -18, 0 and Clip LEDs lit. These LEDs provide an alternate method of feedback in the event the numeric display fails to function.

The Emergency Diagnostics allows you to perform the following functions:

	Numeric Display	Headroom LEDs Lit
LCD Read Scope Loop	0	None
LCD Write Scope Loop	1	-24dB
Initialize Operating System	2	-18dB

Press **Edit** to display the menu selections, turn the front panel encoder to select other manu items.

LCD Read Scope Loop

Press **Store** to start the Scope Read Loop running continuously.

LCD Write Scope Loop

Press **Store** to start the LCD Write Scope Loop running continuously.

Initialize Operating System

Press **Store** to reinitialize the system and then resume normal MPX 1 operation.

Troubleshooting

The following information aids testing of a non-functioning unit (no display, pegged input meters, load noises, popping, crashes, and/or no output). Test procedures are provided for checking power supplies, system clocks, battery, voltages, and both analog and digital signal paths.

WARNING **CAUTION**

As the following procedures require removal of the MPX 1 cover, it is imperative that these tests be performed with regard to all safety and ESD precautions.

Removing the Top Cover

Remove the eight (8) screws which attach the MPX 1 top cover to the chassis.

WARNING
THE POWER SUPPLY IN THIS UNIT HAS A LIVE HEAT SINK.
DO NOT TOUCH WHILE THE UNIT IS PLUGGED IN AND POWERED ON.

Power Supply

Required Equipment
1 DMM (Digital Multimeter)
1 Frequency Counter
1 100MHz oscilloscope (with 1X, 10X probes)
1 Bench power supply providing a variac voltage adjustment and transformer isolation

1. Plug in the MPX 1 and set the variac for nominal line voltage.
2. Set DMM to measure VDC and check the regulated voltages for proper levels using the chassis for ground.

Supplies	Location	Range
+5VD	Test point marked +5V in front of Battery Left side of board	+4.95 to +5.25
+15VA	Test point marked +15VA in front of C89 Left edge of board	+15.00 to +16.95
-15VA	Test point marked -15VA Left front corner of board next to J18 Left side	-14.25 to -15.75

Battery Voltage

1. Turn the MPX 1 off and detach the cord.
2. Set the DMM for a DC voltage on the 20 volts DC scale.
3. Place the negative probe (black) of the DMM on a chassis ground
4. Place the positive probe (red) of the DMM on pin 28 of U22.
5. The reading on the DMM should be 2.50 volts. If the voltage reading is below 2.50, volts replace the battery.

System Clocks

These procedures verify the major crystals and other clocks that are important to the operation of the MPX 1. A frequency counter and an oscilloscope are required for these tests. The oscilloscope's ground lead should be connected to the MPX 1's chassis — away from the power supply.

1. To measure the crystal, Y3, which runs the Lexichip, locate the Lexichip 2 (U17) on the right side of the main board and R189 which is just right of the lower right corner of the Lexichip. Measure each side and verify 22.579MHz.
2. Locate Y1 to the Right of U4 at the rear of the main board just in front of the Digital Input/Output jack , J11. To measure, place the probe on the lead of Y1 closest to you and verify 11.3MHz.
3. Locate Y2 in the center of the main board just to the Left of U15. Place the probe on the test point marked 10MHz and verify 10MHz.
4. Locate Y4 in the center of the main board just above the DAC U20. Place the probe on one of the leads of Y4 and verify 25MHz.

Analog Audio Signal Tracing

Required Equipment

1 Level meter with oscillator
1 Oscilloscope (to confirm audio signals)
2 1/4 shielded phone cables

Setup

1. Turn on the MPX 1 and wait for the Power On Diagnostics cycle to finish.
2. Turn the front panel encoder to display **Sorted by Number/200 Clean Slate.**
3. Press **Bypass** and verify that its LED is lit.
4. Connect an audio cable between the Low Distortion Oscillator and the MPX 1 rear panel left input.
5. Set the MPX 1 rear panel BAL/UNBAL switch to **UNBAL.**
6. Connect the audio output cable between the MPX 1 Left output and the level meter.
7. Set level meter to measure dBu.
8. Turn Input and Output knobs fully clockwise.
9. Apply a 1kHz sinewave signal to the Left input of the MPX 1 at .125 volts RMS.
10. Using the level meter and oscilloscope, measure and verify the signals listed on the following page.

Name	Measurement Point	Levels
Input Stage	U1 Pin 7 Left Input signal U1 Pin 1 Right signal	.485 -.505 volts RMS For left and Right input
Input Level Pot	U11 Pin 1 Left Non-Inverted Buffer	.858 -.912 volts RMS
To Buffer	U11 Pin 7 Left Inverted Buffer U10 Pin 1 Right Non-Inverted Buffer U10 Pin 7 Right Inverted Buffer	.850 -.921 volts RMS .858 -.912 volts RMS .850 -.921 volts RMS
ADC Inputs	U8 Pins 33+32 Left Inputs U8 Pins 23+24 Right Inputs	.858 -.912 volts RMS Left inputs .850 -.921 volts RMS Right input
ADC Output	U8 Pin 12	This is a Digital Audio Signal +5 volt CMOS Characteristics
DAC Inputs	U7 Pin 10	+5 volt Digital Audio Signal
DAC Outputs	U7 Pins 17+18 Left Outputs U7 Pins 13+14 Right Outputs	.685 -.905 volts RMS For Left and Right Outputs
Output Filters	U9 Pin 1 Left Output	1.99 - 2.69 volts RMS
To Output Level Pot	U9 Pin 7 Right Output	For Left and Right Outputs
Output Level Pot	U13 Pin 1 Left Non-Inverted Buffer	2.95 - 4.07 volts RMS
To Buffer	U13 Pin 7 Left Inverted Buffer U12 Pin 1 Right Non-Inverted Buffer U12 Pin 7 Right Inverted Buffer	2.95 - 4.07 volts RMS

Digital Audio Signal Tracing

This procedure verifies the critical clocks and control signals of the MPX 1 digital audio path.

Required Equipment

1 Level meter with oscillator
1 Oscilloscope (to confirm audio signals)
1 RCA cable male to male braided shield style

Setup

1. Connect the RCA cable between the MPX 1 rear panel S/PDIF In and Out jacks.
2. Press and hold **Edit** while powering up the MPX 1.
3. When **Lexicon** is displayed, release **Edit**. Within 5 seconds the display will show:

   Diags: Test
   Switch Test

4. Turn the front panel encoder clockwise until the display shows:

   Diags: Tests
   Dig Audio Test

   The **Options** button should be lit, and the **Store** button should be flashing.

5. Press **Options**. The display will show:

   Repeat test
   1 times

6. Turn the front panel encoder once counterclockwise. The **1** in the display should change to **infinite.** Press **Options** again to restore test mode.

7. Press **Store**. The display will show:

Dig Audio Test
Passed

The MPX 1 will now loop this test continuously and the circuit can tested.

9. Measure and verify the signals listed below.

Name	Measurement Point	Levels
Input Stage	U4 Pin 4 DIG_IN	+5 Volts Level
FPGA Input	U15 Pin 38 DIG_IN	+5 Volts Level
FPGA Output	U15 Pin 34 DIG_OUT	+5 Volts Level
Output Stage	U3 Pins 6/3 DIG_OUT	+5 Volts Level

System Signal Tracing

This procedure tests basic digital control signals in the MPX 1. For each of the following signals, load Program **200 Clean Slate.** Using an oscilloscope, probe at the indicated points listed below and check for the expected results.

Digital Audio Wordclocks

FS	Test point just above U15	44.1 KHz
4FS	U15 pin 49	176.4 KHz
8FS	Test point just Left of Y3	352.8 KHz
64FS	Test point above U15	2.8224 MHz
128FS/	Test point above Lexichip2 U17	5.6448 MHz
256FS	R172 just above U15	11.2896 MHz
10 MHz	Test point just Left of Y3	10 MHz

Reset Signals

RESET/	Test point just above U23	+5 Volts Level
RESET1/	Test point in front of U4	+5 Volts Level
RESET_DAC/	U18 pin 11	+5 Volts Level
RESET_DSP/	U18 pin 4	+5 Volts Level
RESET_LEX/	U18 pin 6	+5 Volts Level
RESET_PEDAL	U18 PIN 7	+5 Volts Level

Restoring Factory Settings

The following procedure restores the MPX 1 factory default settings. This may be necessary due to memory problems, or following internal battery replacement.

Note: This procedure will destroy any user settings or registers.

1. Turn on the MPX 1 and wait for the Power On Diagnostics cycle to finish.
2. Turn the front panel Input knob fully counterclockwise.
3. Press **System.** The display will show:

   System select:
   Audio

4. Turn the encoder until display shows:

   System select:
   Initialize

5. Press **>Yes.** The display will show:

   Initialize
   All

6. Press **Store.**The display will show:

   Are you sure?
   Yes or No

7. Press **Store** to verify the reinitialization request. The message **Sorting** will be displayed while the reinitialization is being performed. Once the procedure is completed, the message **Done** is displayed and the MPX 1 will return to its original factory set power on state.

Software Error Messages

If a software error occurs, an error message will be displayed on the upper left corner of the display. A list of these messages is provided below.

Please note that the software error messages (E1, E2, E3, etc..) have no relation to the error messages displayed for the Power On Diagnostics.

Please contact Technical Support at Lexicon Customer Service if you encounter any of these error messages.

E0 No error
E1 MIDI in overflow
E2 MIDI out overflow
E3 MIDI in frame error
E4 too many dump bytes
E5 incorrect num dump bytes
E6 dump buffer full
E7 lcd timeout
E8 MIDI handshake timeout error
E9 compact data error
E10 compact MIDI data error
E11 out of range program number
E12 prog ptr error getting prog name
E13 prog ptr error getting large prog
E14 prog ptr error getting small prog
E15 prog ptr error getting prog status
E16 prog ptr error clearing reg
E17 prog load error: reg unassigned
E18 prog load error: cleanup
E19 2115 DM overflow error
E20 2115 PM overflow error
E21 2115 INT overflow error
E22 2115 INT and PM overflow error
E23 2115 BK overflow error
E24 2115 INT steps overflow error
E25 2115 Already a FIRST error
E26 2115 effect order error
E27 2115 effect already assigned error
E28 2115 command clear timeout after load
E29 2115 command clear timeout after "prepare for load"
E30 audio param memory error in compact
E31 audio param memory error in "will_fit"
E32 extract param alg num error
E33 extract param size error
E34 compact param alg num error
E35 compact param size error
E36 "will fit" param size error
E37 "get size" param size error
E38 "get size" alg num error
E39 "get size" effect number error
E40 2115 resync: waiting for RESYNC command clear
E41 2115 resync: waiting for RESYNC command clear 2nd try
E42 2115 load: error count inc in external mode
E43 ran out of timers

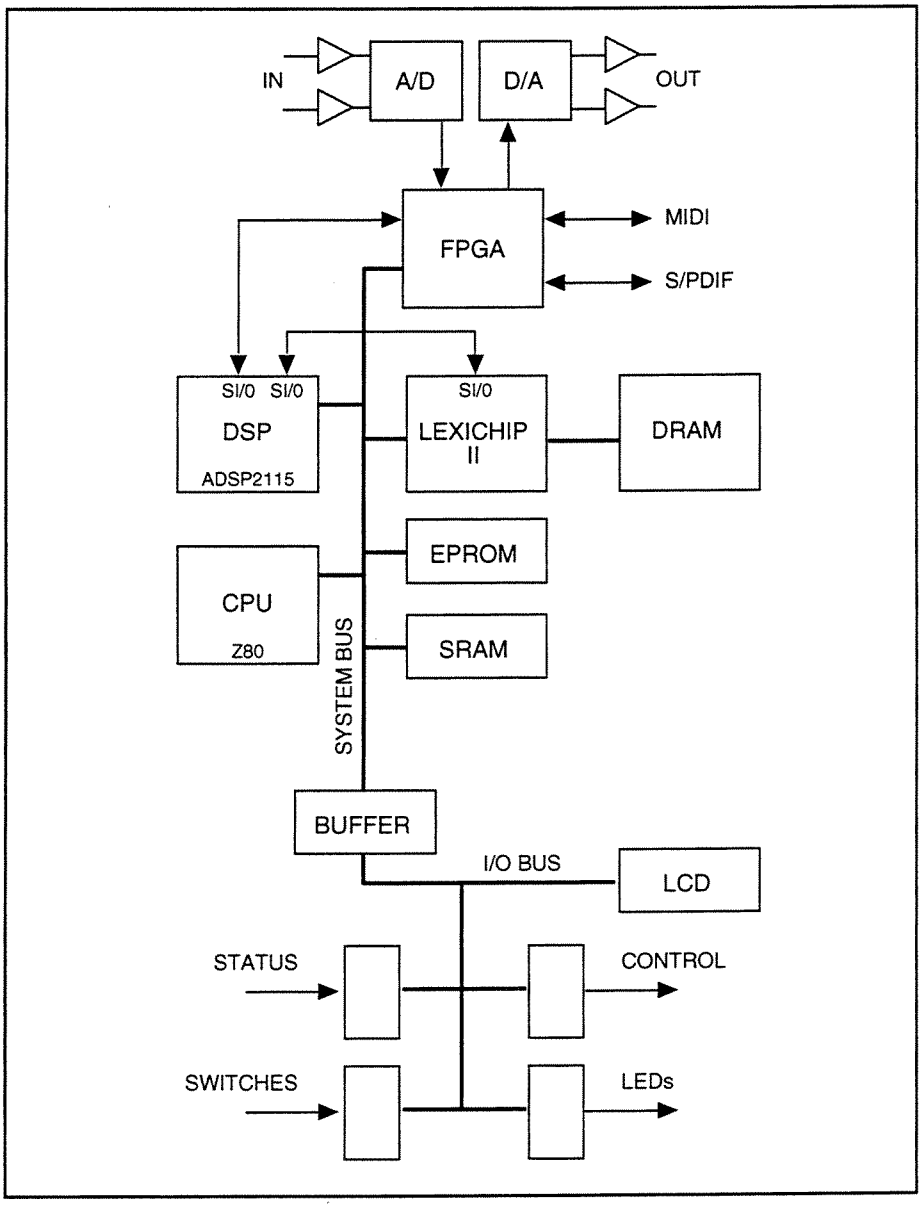
5

Theory of Operation

This section is divided into three sections: Architecture, which describes the basic structure of the MPX 1 hardware; a Schematic Walkthrough, which familiarizes the user with the components and Timing Issues, which also includes other operational details.

Architecture

Block Diagram



The Z80 handles the system software. The 2115 deals with signal routing and non-reverb DSP. The Lexichip performs the reverb. The FPGA performs most of the discrete logic, and includes an S/PDIF transceiver and MIDI UART. The EPROM holds the program information for the Z80 and the 2115, as well as configuration data for the FPGA. The SRAM holds variables for the Z80 and 2115, serves as a communication channel between the two processors, and provides a short audio buffer for the 2115.

As both the Z80 and 2115 have bus request/acknowledge features, they are able to share the system address and data busses. The Z80 owns the bus most of the time, but the 2115 takes over for the last part of every word clock.

This shared bus means that the 2115 is capable of accessing almost everything the Z80 can, including the Lexichip. The 2115 refreshes the LED displays, reads and debounces the switches, and transmits MIDI clock. All other system functions are left to the Z80.

The 2115 and Lexichip communicate through their respective serial ports, running at 128fs, allowing up to 8 16-bit channels of data to pass between the chips in both directions.

Z80-2115 Bus Sharing

The Z80 and 2115 share the system bus. The Z80 owns the bus for about 70% of the time, surrendering it to the 2115 for a few microseconds every sample period (22 µs). The Z80 stops executing when the 2115 owns the bus, so its effective speed is really its clock speed multiplied by the time on the bus, or approximately 7MHz. The 2115, however, runs even when it doesn't own the bus, stopping only when it has to make an external access.

The exact ratio of Z80 to 2115 time, as well as which section of the word clock belongs to which processor, is programmable. The Lexichip's DEG0 line goes high to tell the Z80 to give the bus to the 2115. When the 2115 is finished, it gives the bus back to the Z80. This flexibility allows the 2115's time on the bus to be fine tuned to a resolution of 128th of a word clock. In order not to interfere with the Z80's access of the Lexichip, the 2115 is given access roughly half-way through the word clock, and always surrenders it before the end of the word clock.

When syncing the Z80 to the Lexichip's first instruction, the Lexichip's _WAIT line is sent into the Z80's _BUSREQ input.

Memory Map

The EPROM is divided into eight 32K banks. The Z80 selects the bank by writing to the I register, whose contents are placed on the high address bus during refresh. The three extended address lines (P15-P17) are mapped into the I register as follows:

D7	D6	D5	D4	D3	D2 P17	D1 P16	D0 P15

ADDRESS	**BANK 0**	**BANK 1**	**BANK 2**	**BANK 3**
0x0000	COMMON ROM	COMMON ROM	COMMON ROM	COMMON ROM
0x4000	see below	see below	see below	see below
0x8000	COMMON ROM	ROM BANK 1	ROM BANK 2	ROM BANK 3
0xC000	ROM BANK 0			

ADDRESS	**BANK 4**	**BANK 5**	**BANK 6**	**BANK 7**
0x0000	COMMON ROM	COMMON ROM	COMMON ROM	COMMON ROM
0x4000	see below	see below	see below	see below
0x8000	ROM BANK 4	ROM BANK 5	ROM BANK 6	ROM BANK 7
0xC000	ROM BANK 4			

When A15 is low, the Z80 addresses either the common ROM, or the memory-mapped peripherals defined below. When A15 is high, the Z80 addresses the ROM bank selected by P15-P17.

The 2115 cannot drive A14 or A15. When it takes over the bus, A15 is pulled low and A14 is pulled high, allowing the 2115 to access memory-mapped peripherals in the 0x4000 block.

The 16K block between 0x4000 and 0x8000 contains the SRAM and memory-mapped peripherals. A bank-switching technique is used to fit a 32K SRAM into this area. The Z80 sets bit 4 of the I register, called RAM_A14, to determine which bank it will access. When the 2115 owns the bus, RAM_A14 is gated low.

This area is mapped as shown below.

ADDRESS	VIEW FROM Z80 RAM_A14=0	VIEW FROM Z80 RAM_A14=1	VIEW FROM 2115
0x4000	SRAM (used by 2115 during boot)	UPPER HALF OF SRAM (Used for preset storage)	DATA BUFFER SRAM (16 bits)
0x4400			
0x4800			
0x4C00			
0x5000	LEXICHIP		
0x5400	FPGA UART		
0x5800	FPGA REG 1		
0x5C00	FPGA REG 2		
0x6000	SRAM SHARED WITH 2115		SRAM SHARED WITH Z80
0x6400			
0x6800	SRAM		FPGA REG 1
0x6C00			FPGA REG 2
0x7000			LEXICHIP
0x7400			FPGA UART
0x7800			2215 INTERNAL RAM/REGISTERS
0x7C00			

The peripherals are mapped into different addresses for the Z80 and the 2115 to allow each processor to maximize SRAM usage. The lowest 8K of the SRAM is used by the 2115 to store audio data. This section is 16 bits wide; U21 provides the high byte. The 2115 boots from the low 4K of the SRAM. As the Z80 does not need to access the upper half of the 2115 data buffer, the memory-mapped peripherals are here.

The 8K section of SRAM starting at 0x6000 is used by the Z80 for general storage. The lowest 2K of this section is visible to both the Z80 and the 2115. The Z80 keeps variables which must be visible to the 2115 in this area.

When the RAM bank select line (RAM_A14) is high, the entire 16K block from 0x4000 to 0x7FFF is mapped to the upper half of SRAM, which the Z80 will use to store user preset data. Because the Z80 stack is invisible when RAM_A14 is high, the Z80 disables interrupts when accessing upper RAM.

The FPGA has two internal 8-bit registers (reg1 and reg2).

Register 1 (write only):

bit 0	SAVE_SRAM	When 1, prevents the DSP from writing to the low byte of the SRAM. The Z80 asserts this bit when preparing to load a new program into the DSP to prevent the DSP from overwriting the program with audio data.
bit 1	ENABLE_DIGOUT	Gates DIG_OUT. When 1, DIG_OUT is enabled.
bit 2	THRU_MODE	When 1, sends input S/PDIF channel status and user bits to output channel status and user bits. When 0, output channel status is forced to consumer mode and output user bits are set to 0.
bit 3	RESET_UART	When 1, resets the MIDI UART. (Must be set for at least 1µs after power-up.)
bit 4	ENABLE_BUSREQ	Gates DEG0. When 1, allows DSP_ON_BUS to go high after DEG0. When 0, keeps DSP_ON_BUS at 0.
bit 5	EXT_SYNC_MODE	When 0, sample rate source is Lexichip's master clock. When 1, sample rate source is S/PDIF in.
bit 6	_RELOCK	When 0, PHASE_DET is forced low to allow the PLL filter cap to discharge.
bit 7	SELECT_DIG_IN	When 0, audio data source is the A/D. When 1, audio data source is the S/PDIF input.

Register 2 Write:

bit 0	undefined	
bit 1	undefined	
bit 2	undefined	
bit 3	RESET_COUNTER	When 1, resets the word clock counter, turning off FC and its multiples. The Z80 sets RESET_COUNTER to resync the 2115.
bit 4	BLUE_BOX	Keep set to 0.
bit 5	undefined	
bit 6	undefined	
bit 7	undefined	

When the DSP has finished its time on the bus, it gives it back to the Z80 by writing 00 to the Reg2 location. The FPGA interprets a write to register 2 as a command to return the bus to the Z80.

Register 2 Read:

bit 0	TXRDY	UART transmit ready. 0=busy. The processor will not write to the UART when this line is low. A write to the UART will set TXRDY within 1µs.
bit 1	RXRDY	UART receive ready. 1=receive data is ready. Reading from the UART address clears this bit. On power-up, the Z80 reads the UART address to pre-clear RXRDY.
bit 2	FRAMING ERROR	When set, indicates a UART receive framing error. This bit is updated every time a serial byte is received in the UART. It is not valid unless RXRDY is also set.
bit 3	DIGIN_PRESENT	When 1, indicates that the S/PDIF receiver detected a preamble. Once set, it stays set until _RELOCK is set.

I/O Map

To reduce the load on the system data bus, the I/O bus is isolated from the main bus with a transceiver. (See Sheet 4 description in the Schematic Walkthrough section.) The direction of the transceiver is controlled by the A0 line. Thus, all odd I/O addresses must be writes and all even addresses must be reads.

ADDRESS	READ	WRITE
0x00	STATUS 1	
0x01		CONTROL
0x10	STATUS 2	
0x41		DISPLAY 1
0x61		DISPLAY 2
0x81		LCD CONTROL
0xC0	LCD	
0xC1		LCD

STATUS 1 (U32, sheet 5)

BIT 0 SWITCH_ROW 0
BIT 1 SWITCH_ROW 1
BIT 2 SWITCH_ROW 2
BIT 3 SWITCH_ROW 3

STATUS 2 (U32, sheet 5)

BIT 0 ENC1 (phase A of the rotary encoder)
BIT 1 ENC2 (phase B of the rotary encoder)
BIT 2 footswitch tip
BIT 3 footswitch ring

CONTROL (U18, sheet 4)

This is an addressable latch. A1 determines whether a bit is set or reset, and A2-A4 determine the bit to change.

Address	01, 03	RESET_DSP
	04, 07	MUTE
	09, 0B	_RESET_LEX
	0D, 0F	RESET_PEDAL
	11, 13	SOFT_SAT
	15, 17	DISCHARGE
	19, 1B	_RESET_DAC

These signals are described in sheet 4 of the Schematic Walkthrough. They are initialized to 0 by _RESET.

DISPLAY 1 (U31, sheet 3)	bit 0	column address 0
	bit 1	column address 1
	bit 2	column address 2
	bit 3	RIGHT_ROW0
	bit 4	RIGHT_ROW1
	bit 5	RIGHT_ROW2
	bit 6	RIGHT_ROW3

These signals are initialized to 0 by _RESET1. There are five columns of LED's, starting at address 1 and ending at address 6. Address 0 is unused. The RIGHT_ROW bits are active high, unlike the left row bits.

DISPLAY 2 (U27, sheet 3)	bit 0	left row 0
	bit 1	left row 1
	bit 2	left row 2
	bit 3	left row 3
	bit 4	left row 4
	bit 5	left row 5
	bit 6	left row 6
	bit 7	left row 7

These bits are active low.

LCD CONTROL (U29, sheet 3)	bit 0	CONTRAST0
	bit 1	CONTRAST1
	bit 2	CONTRAST2
	bit 3	CONTRAST3
	bit 4	LCD_READ
	bit 5	LCD_ADDR1

These signals are described in sheet 3 of the Schematic Walkthrough.

Schematic Walkthrough

Sheet 1

This sheet shows the Z80 and 2115 wire-ORed onto the data and address busses. As the 2115 does not drive A14 and A15, these lines are pulled high and low, respectively, when the 2115 owns the bus.

The low byte of SRAM (U22) is made non-volatile by battery BAT1 and associated components (sheet 8). The second SRAM (U21) is used exclusively by the 2115 as the high byte of the audio buffer.

Sheet 2

Sheet 2 contains the Lexichip and 256K x 20 bits of audio DRAM. J17 is unpopulated, as is a corresponding jumper location (W2).

Sheet 3

This sheet contains the display drivers.

The LEDs on the front panel are physically divided into those on the left of the LCD and those on the right. On the left are two columns of discrete LED's for level meters and three 7-segment displays. These naturally organize themselves as 5 columns of 8 rows. On the right are 19 discrete LED's, organized as 5 columns of 4 rows.

Octal D-flop U31 clocks the IO_DATA bus (a buffered version of the system data bus) on the trailing edge of _DISPLAY_WR1. U31's low three bits are decoded by U33, to create five active-low column select lines. These are buffered and inverted by switching transistors Q34-Q38. When a selected COL line is driven high and a ROW line is driven low, the LED at the crosspoint of the col and row will light. Also, if one of the front panel switches in the selected column is pressed, the SWITCH_ROW signal corresponding it its row will go high.

Resistors R251, R253, R255, R257 and R259 pull non-selected columns to ground for proper detection of the switches.

U31 directly drives the right row lines. Eight row drivers for the left display use discrete transistors Q26-Q33. The 100Ω resistors (R217, etc) limit the row current to about 28mA.

Writing to octal D-flop U29 sets the LCD access mode. The Z80 sets LCD_READ if the next LCD access will be a read, and clears it if the next access will be a write. The Z80 also sets LCD_ADDR_1 if the next access will be data transfer, and clears it if the next access will be command or status.

The four LSB's of U29, together with resistors R231-R236, form a DAC which controls the LCD contrast voltage.

Sheet 4 Octal transceiver U30 decouples the system data bus from the IO data bus in order to reduce loading on the system bus. _IOREQ enables the transceiver, and ADDR0 controls the direction. Thus, all odd IO addresses must be writes, and all even ones reads.

Addressable latch U18 generates the following control lines:

_RESET_DSP	resets the 2115 when low.
_MUTE	mutes the analog outputs when low.
_RESET_LEX	resets the Lexichip when low.
RESET_PEDAL	discharges the pedal ADC's capacitor when high.
SOFT_SAT	enables soft saturation of the ADC when high.
DISCHARGE	discharges the S/PDIF receiver's VCO capacitor in preparation for relock.
_RESET_DAC	resets the DAC when low.

U15, a Xilinx Field-Programmable Gate Array (FPGA) consists of a collection of 144 Configurable Logic Blocks (CLBs), each of which resembles a small PAL. The configuration of these CLBs, as well as the inter-CLB routing, is held in the FPGA's internal SRAM, which is loaded during power-up from the upper 4Kbytes of the EPROM. On power-up, U15 reads the EPROM by driving ADDR0-ADDR15 and _ROM_EN. Once it is configured, it stops driving the address lines, then brings DONE high, which unresets the Z80 and gives it control of the bus. The power-up sequence is described in the Timing Issues section.

U15 performs the following tasks:

Address Decoding U15 does all of the address decoding and chip select generation described previously. It creates:

P15-P17	upper bank addresses for the EPROM
RAM_A14	upper address for the SRAM
_ROM_EN	EPROM chip select
_HI_RAM_EN	chip select for the high byte of SRAM
_LO_RAM_RD	read strobe for the low byte of SRAM
_LO_RAM_WR	write strobe for the low byte of SRAM
_DISPLAY_WR1	clocks the data bus into U31 (sheet 3)
_DISPLAY_WR2	clocks the data bus into U27 (sheet 3)
_LCD_WR	clocks the data bus into U29 (sheet 3)
_LEX_WR	Lexichip write strobe
_LEX_EN	Lexichip chip select
LCD_EN	LCD strobe
_RD_STATUS	gates the status registers (U28 and U32, sheet 5) onto the data bus
_CONTROL_WR	clocks the addressable latch U18

Clock Generation

U15 selects _MC (512 FS) from the Lexichip or VCO (256 FS) from the digital input circuit, depending on whether the unit is in internal or external sync, and divides it down to make 256FS, 64FS, 8FS, 4FS, and FS, which are used by the A/D and D/A converters and the serial link between the 2115 and the Lexichip.

Synchronized Word Clock

U15 synchronizes its internally generated word clock (FS) to the Lexichip master clock (_MC), to create _LEX_WC.

S/PDIF Clock Recovery

U15 includes a phase detector which produces a pulse on PHASE_DET whose width is proportional to how far the DIG_IN signal leads the VCO signal. This is used by the clock recovery circuit on page 7 to help the VCO lock to the S/PDIF input frequency.

S/PDIF Encoder/Decoder

U15 demodulates the S/PDIF data from DIG_IN, and sends the decoded data to the 2115 over DSP_IN_DATA. If the ADC is selected as a data source, U15 routes ADC_IN to DSP_IN_DATA. U15 also modulates data from DSP_OUT_DATA to create S/PDIF data on DIG_OUT.

MIDI UART

U15 contains a stripped-down UART capable of sending and receiving asynchronous data at 31.25 Kbaud. When it receives a byte, it asserts _INT, which interrupts the Z80.

Wait State Generator

U15 decodes Z80 accesses to the Lexichip and LCD, adding two wait states for Lexichip accesses and four for LCD accesses.

Lexichip Synchronization

U15 uses LEXPHSAB from the Lexichip to make sure that write accesses to the Lexichip remain stable during the Lexichip "A" phase. It also generates LEXPHSDA, which clocks the address bus into U16 and U19 to meet Lexichip address setup and hold requirements.

Bus Arbitration

When U15 sees a high DEG0 from the Lexichip, which happens about half-way through the Lexichip word clock cycle, it asserts _ZBUSREQ. The Z80 gets off the bus and asserts _ZBUSACK. When U15 sees this, it asserts DSP_ON_BUS, which gives the 2115 access to the system bus. Once the 2115 has finished, it writes to an internal register in U15, which clears DSP_ON_BUS, giving the bus back to the Z80. When the Z80 wants to sync to the first Lexichip instruction, it writes to a special register in the Lexichip, which asserts _LEX_WAIT. U15 OR's this signal into the _ZBUSREQ signal. This halts the Z80 until the Lexichip reaches the top of its instruction list.

Sheet 5 Sheet 5 includes the inputs, the LCD interface, and the pedal A/D converter.

U32 reads the multiplexed switches from the right front panel, the encoder, and the footswitches. R246-R249, C154 and C156 help to debounce the encoder.

The pedal A/D converter is the integrating type made from current source Q1 and a 16-bit timer in the 2115. To start the conversion, the 2115 brings RESET_PEDAL high, which brings U2 pin 7 low, which discharges capacitor C32 to less than 0.2V. The 2115 then starts its timer and brings RESET_PEDAL low. C32 starts to charge from the current source. Once the capacitor voltage exceeds the footpedal voltage, PEDAL_ADC goes low. This produces a high-level interrupt on the 2115, which disables the timer. At its convenience, the 2115 reads the timer and derives the voltage on the pedal. This technique allows 14-bit resolution. The input voltage range is 0-10V. R42 puts the 5V excitation voltage on the pedal ring, while preventing excessive current draw from the 5V supply.

Sheet 6 The MIDI in connector (J14) does double duty as the interface to the MIDI remote. In addition to the standard MIDI input signals on pins 4 and 5, it sends a copy of MIDI out to pins 1 and 3, and also routes power from the remote power jack (J15) to pins 6 and 7.

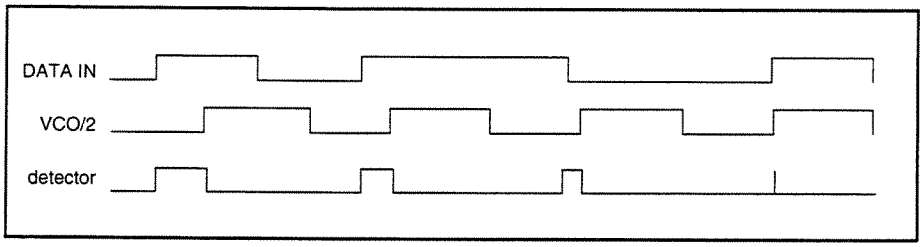
Opto isolator U5 provides the necessary MIDI input isolation. U3 and Q7 create a copy of the MIDI input signal, and send it to the MIDI thru jack (J13). Q6 and Q11 buffer the MIDI_OUT data from the FPGA, and send it out J12 and J14.

Sheet 7 Although the FPGA does most of the work of demodulating the incoming S/PDIF data, it still requires a clock that is 256 times the S/PDIF sample rate. This clock is provided by a Voltage-Controlled Oscillator (VCO) created from ceramic resonator Y1, unbuffered inverter U4, and associated components.

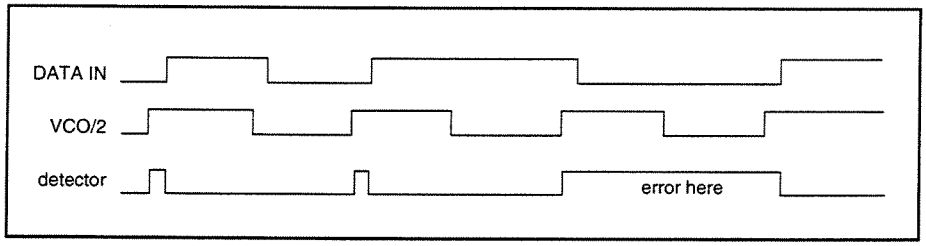
A quick review: S/PDIF data is transmitted as frames. Each frame contains two subframes. Each subframe contains one audio sample. The two subframes represent the left and right channels of a stereo pair. Each subframe is divided into 32 time slots. With the exception of time slots 0-3 (the preamble) each time slot carries one bit of information. Each time slot contains two states. The first state of a time slot is always different from the last state of the previous time slot. If the time slot represents a logical "0", the second state is the same as the first state. If the time slot represents a "1", the second state is different from the first state.

At a 44.1 KHz sample rate, the state rate or baud of the S/PDIF link is 128fs, or 5.6448 MHz. In the encoding scheme mentioned above, no more than two states will go by without a transition in the data line, except during a preamble. Preambles occur at the beginning of each subframe.

We use two complementary techniques to lock the VCO to the incoming data rate. The first is half of a classical phase detector (located in the FPGA), which compares the rising edge of VCO/2 with the rising edges in the data stream. If the VCO lags behind the data stream, the phase detector creates a correction pulse which increases the VCO's voltage, causing the VCO to increase its frequency and catch up with the data stream. This is shown below:



If the VCO leads the data in, this technique will not work, because the data stream doesn't have all of the edges the detector needs:



In other words, the "lag" half of the phase detector works, but the "lead" half doesn't. A pull-down resistor (R66) supplies some correction, but any jitter in the incoming signal sends the VCO to the top of its range. Injecting some of the S/PDIF input signal into the VCO forces the VCO into lockstep with the S/PDIF input as long as the VCO frequency is close to the S/PDIF frequency. Therefore, it is the job of the phase detector to get the VCO to within the pulse injector's capture range, and the pulse injector's job to stay locked in the presence of jitter.

This technique is reasonably robust, but fails in the presence of large amounts of jitter, or during a sudden downward shift in the frequency of the S/PDIF signal. In these cases, the phase detector pulls the VCO to the top of its range. When the Z80 detects this condition, it pulls the VCO back to the bottom of its range, then releases it and gives the phase detector another try.

The core of the VCO is ceramic resonator Y1, which forms an 11.3MHz oscillator with unbuffered inverter U4. R58 biases U4 into its linear region. The operating frequency of the VCO is determined by the capacitance on the legs of Y1. This capacitance is created by varactors D15-D17. The higher the voltage across the varactors, the lower the capacitance, and the higher the operating frequency. The anodes of the varactors are biased to ground with R63 and R64, while the cathodes are tied to PLLV, the VCO's control voltage. C45 and C46 are DC blocking caps. They allow the varactors to be biased to ground while the resonator is biased to VCC/2.

R59 increases the pullability, or frequency range, of the VCO, which is roughly +-1%. Although the S/PDIF spec only requires a 1000 PPM of lock range, the tolerance of the resonator requires a much larger range.

D14, R60, and C43 detect the rising edges from the S/PDIF input, and couple them into the VCO to enhance its stability.

High-speed transistors Q8 and Q9 convert the positive pulses on PHASE_DET into pulses of current from the 15V supply into loop filter cap C51. Q10 discharges C51 at the start of a lock acquisition cycle.

The S/PDIF receiver is an unbuffered inverter (U4) biased into its linear region. A pair of 74HC00s generate the S/PDIF output signal. Each gate has to source about 6.25mA. The voltage across R51 is 0.5Vpp, assuming a 75Ω load resistor across the S/PDIF connector and a Voh out of the gates of 4.7V, which is the typical Voh at 6mA.

C35 and C39 are not populated.

Sheet 8 This sheet includes the reset circuit and SRAM battery backup.

During power-up, U6 pin 1 pulls _RESET to ground until the voltage at pin 2 rises above approximately 4.3V. R93 and C70 form a power-on delay. R93 charges C70, which keeps Q14 turned on until its base reaches Vcc-1.2V. At that point, Q10 turns off, and U6 pin 1 goes to Vcc. This causes _RESET to go high.

D20 allows quick response to loss of Vcc. When Vcc slips below 4.3V, D20 is back-biased. D21 provides a quick discharge path for C70 to allow long resets in the event of short losses of Vcc.

Jumper W1 provides a manual reset.

When Vcc is absent, Q13 is off, and the SRAM supply voltage (VRAM) comes from the lithium battery. In order for the SRAM to go into power-down mode, its chip enable pin (WRITE_PROTECT) must be high. R86 ties WRITE_PROTECT to VRAM.

When Vcc is present, but _RESET is active, Q13 will be off, which keeps Q12 off as well. This keeps WRITE_PROTECT high, protecting the SRAM contents until the system is stable.

When Vcc is present and _RESET is off, Q13 is on, which brings WRITE_PROTECT low and turns on Q12, which couples Vcc to VRAM. D19 keeps Vcc from charging the battery, and R87 adds extra protection to the battery, as required by some regulating agencies.

Power resistors R81-84 are included to meet the power supply's minimum current specs.

Sheet 9

In the analog input stage, when SW1 is set to "BAL", U1 is configured as a differential amplifier with a gain of unity. When SW1 is set to "UNBAL", U1 is a single-ended amp with a gain of 4 (12 dB). The buffered input signals then go to 10K input pots through connector J18. The wipers of the input pots are RINPOT and LINPOT, which go to the next sheet.

Sheet 10

From the input pots, the signals go to non-inverting buffers U10 and U11, which add a gain of 1.78 (5dB). The other half of U10 and U11 invert this signal. The resulting differential signal goes to U8, the Philips SAA7360 A/D converter. Blocking caps C102, C106, C108, C112 and biasing resistors R97, R98, R102, and R103 shift the zero point to VREFL and VREFR from U8, which is roughly Vcc/2.

The transistors at the bottom of the page solve several problems. It is important to keep the inputs between 0 and 5V in order to keep U8 from latching up, and to compensate for a bug in the SAA7360 which resembles "foldback" distortion when the input gets above about 4.5 V or below about 0.5V. This also allows "softening" of the harsh digital clipping of the A/D converter.

Aa an example, assume that Q19 and Q20 are turned off. R132, R131, and R134 create a voltage divider which places 3.4V at the bases of Q21 and Q23. When the voltage from the op-amps exceeds 4.0V, The transistors turn on, clamping the voltage to 4V. R130 and R122 soften the clamping action, allowing the voltage at the converter to get up to 4.5V when the inputs are seriously overdriven. This clamp point is above the full-scale input of the A/D, but below the point where foldback distortion kicks in.

R128, R127, and R134 form an identical voltage divider for Q15 and Q17. Using separate voltage dividers reduces crosstalk between the audio channels.

Similarly, Q24, Q22, Q16, and Q18 protect against negative excursions. The voltage dividers bias the bases at about 1.6V. This puts the bases at about 1V, which keeps the input signals above 0.5V.

In soft saturation mode, Q19 and Q20 turn on, changing the base voltages to 3.0V and 2.0V. In this mode, clamping begins at roughly -3dBfs.

The softness of the clamping is determined by the relative values of R130, R122, etc., and R146-147, R151-152, etc. Increasing R130 softens the saturation in soft saturation mode, but also increases the voltage excursions at U8, even in non-soft saturation mode, to the point where foldback distortion starts.

Sheet 11

U7 is a 20-bit sigma-delta D/A, the Crystal Semiconductor CS4329. U9 is a combination differential to single-ended converter and 3-pole low-pass filter. The filter attenuates ultrasonic noise created by the D/A. From the filter, the signal goes to the J18 on sheet 9, then to the output level control pots, then to sheet 12.

Sheet 12

From the output pots, the output signal goes into non-inverting buffers U12 and U13, which add a gain of 1.5 (3.5dB). The outputs are inverted by the other halves of U12 and U13, to form a pseudo-differential driver.

There is no auto-balancing; if you short out the ring signal, the tip signal's level does not increase to compensate. Note that you can ONLY short the ring signal. If you short the tip signal, the ring signal's distortion will rise dramatically.

Q25 on sheet 9 shifts the level of the _MUTE signal to create MUTE, which is close to 5V when active and -15V when inactive. This signal drives FET's Q1-Q4 (sheet 12). When the gate voltage is at 5V, the FET's turn on, pulling the outputs of the differential drivers to ground.

Capacitors C19, C22, C25, and C28 are not populated.

Timing Issues

Power-On Sequence

When +5V comes on from a cold start, it charges C70, and roughly 100ms later (the timing is not critical), _RESET goes high. Refer to sheet 8 of the Schematic Walkthrough for a description of the reset circuit.

The first thing to come out of reset is U15, the FPGA (sheet 4). It has an internal low-voltage detector, so it starts its initialization phase when Vcc rises above about 2.8V AND _RESET goes high. When the FPGA enters its initialization phase, it drives ADDR0-ADDR15 and _ROM_EN, and reads roughly 4 Kbytes of configuration data from the ROM's upper memory. It then performs an error check on the data. If the check fails, it keeps retrying to reload the data. If there are problems with the EPROM, data, or address busses, the FPGA will load forever. This is a handy feature, because the FPGA will toggle the address lines, making it possible to check for shorts and opens in the bus.

During the initialization phase, the FPGA pulls all IO pins to 5V through high-impedance resistors. During the initialization phase, a roughly 1MHz clock will appear on pin 74 of U15. If this clock never appears, and U15 pin 55 (DONE) stays low, replace U15.

NOTE: Manually pulling _RESET low (e.g. by shorting W1 on sheet 4) does NOT put the FPGA into initialization phase. It only resets the states of the flip-flops inside of it. The only way to put the FPGA into initialization phase is to cycle power.

When the initialization phase finishes, DONE goes high, which brings _RESET1 high, which unresets the Z80. The Z80 performs power-on diagnostics of the system. If nothing happens, check the 1 MHz test point near U14. If it's there, look for activity on _RD (U24 pin 23). Also make sure that DSP_ON_BUS (to the left of U15) is low.

Once the Z80 passes its diagnostics, it gives the bus to the 2115 so that it can perform its own diagnostics. (Bus sharing is described in the Architecture section.). The two processors pass the bus back and forth until all of the diagnostics are completed. Then the Z80 performs a synchronization (described above). When this is completed, the 2115 will own the bus about 30% of time, starting just after the rising edge of FS (located above U15). Power-up is complete.

If the system crashes during power-up, it is often useful to look at DSP_ON_BUS. If it is stuck high, then the 2115 died while on the bus. Make sure U20 pin 43 has a 25 MHz clock. Make sure U20 pin 20 (_RESET_DSP) is high, and pins 47, 48, 51, 53, 54, and 56 have clocks.

If DSP_ON_BUS is low, then the Z80 owns the bus. It is still possible that it is waiting for the 2115. As described earlier, DSP_ON_BUS is set when DEG0 goes high. Check to make sure positive DEG0 pulses (U15 pin 35) are happening near the rising edge of FS.

Synchronizing and Locking to S/PDIF

All serial communications to and from the 2115 are timed by the 44.1KHz word clock, also called the sample clock or FS (Frequency of Sample). In internal sync mode, FS is derived by dividing the Lexichip's master clock (MC) by 512. All of the other FS clocks (8FS, 128FS, etc.) are derived from the same counter. In external sync mode, FS is derived from the VCO, which, when locked to an incoming S/PDIF signal, should be at exactly 256*FS, or 11.2896 MHz.

In order to synchronize the 2115 to MC, the Z80 first shuts down the word clock, then tells the 2115 to get ready for a resync, then turns the clock back on. If all goes well, the 2115 will end up on the bus approximately 30% of every word clock, starting at the rising edge of FS.

Synchronizing to the S/PDIF is more complicated. The S/PDIF clock recovery circuit is described in Sheet 7 of the Schematic Walkthrough.

To synchronize to the S/PDIF input, the Z80 shuts down the word clock and notifies the 2115. It then discharges the phase-locked loop capacitor (C51, sheet 7). The PLLV test point is in the upper right corner of the board, just below and to the left of the horizontal electrolytic cap (C51). The Z80 then allows the cap to recharge. As PLLV rises, it sweeps the VCO (Y1, U4, sheet 7) over its range, typically 11.15MHz to 11.4MHz. When the VCO reaches the frequency of the S/PDIF input, it locks on, and PLLV stabilizes, typically at 3-5V. Once the VCO has locked, the FPGA examines the DIG_IN data stream to look for a preamble (which marks the beginning of a word clock). If it finds one, it turns the word clock back on. The 2115 synchronizes to the word clock, and as before, it takes over the bus every rising edge of FS.

If the synchronization fails after several attempts, the Z80 reports a "resync failed". If this happens, retry the synchronization while monitoring PLLV. It should sweep from ground to roughly +12V three or four times. If PLLV doesn't go to ground, make sure DISCHARGE pulses high for a few msec every few seconds.

If PLLV doesn't rise, then something is wrong with the phase detector. Check the PHASE_DET signal. It should have positive pulses every few hundred nsec. If it is stuck at ground, then make sure there is a signal at DIG_IN (U15 pin 38) and that the box is in external sync mode.

If PHASE_DET is pulsing, but PLLV refuses to rise, follow the pulses through Q8 and Q9.

If PLLV appears to be sweeping correctly, double-check that the S/PDIF source is at 44.1KHz sampling rate. Then double-check the DIG_IN signal (U4 pin 4, sheet 7). It should show clean transitions from 0-5V.

Next, wait for the Z80 to give up locking (it stops periodically shorting PLLV to ground), then short PLLV to +5V and measure the frequency at U4 pin 10 with a frequency counter. It should be between 11.25 MHz and 11.35 MHz. If the Z80 is functional, you can test the VCO's frequency by running the resonator test in the diagnostic page. If the resonator frequency is too high, there could be a problem with one or more of the varactors (D15-D17). Check for open solder joints around C45-46, R63-64, and the varactors.

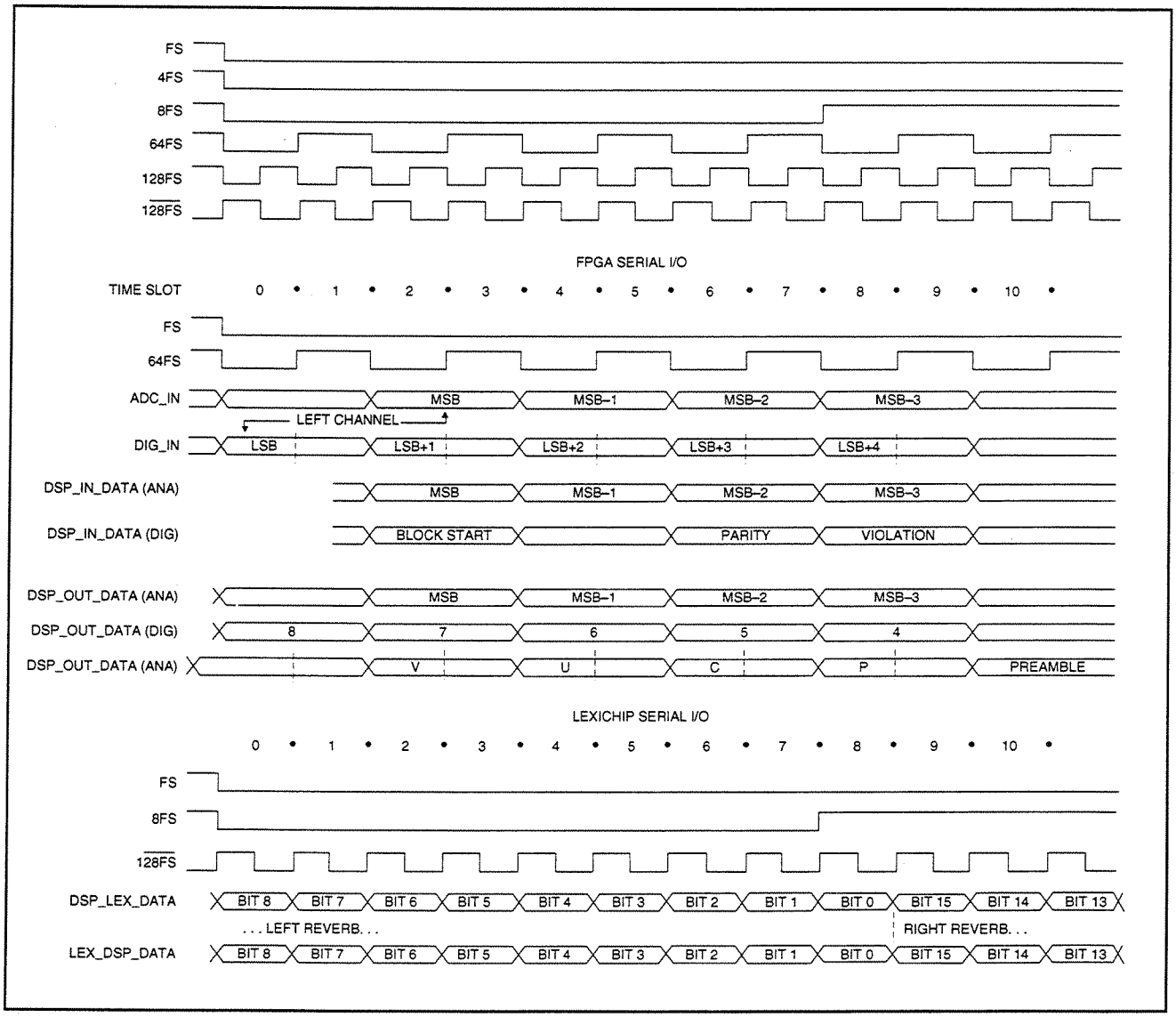
IF PLLV seems to pause during its sweep, then continue to 12V, it means that the VCO barely managed to lock, but couldn't hold the lock. Look for problems around R66, R67, C51, D14, R60, and C43. It is also possible that the S/PDIF source is so jittery that the MPX 1 can't maintain a lock. Make sure that DIG_IN looks clean.

Occasionally, even a perfectly working system will fail at its first resync attempt. This happens when PLLV sweeps past the correct lock voltage at the precise time that the phase detector detects a preamble, about 1% of the time.

If PLLV seems to settle on a voltage below 12V, but the resync still fails, check for the presence of FS. FS won't appear until the FPGA reads a valid preamble. If DIG_IN is noisy or corrupted, FS will stay low.

The following diagram shows the phase relationships of the serial signals to and from the FPGA.

FPGA Serial Communications



Each word clock is broken into 64 time slots, with time slot 0 starting at the falling edge of FS. All serial signals except DIG_IN and DIG_OUT have cell boundaries which line up with time slot boundaries. DIG_OUT's boundaries are skewed 1/4 time slot early. In addition, DIG_IN and DIG_OUT are modulated S/PDIF signals, so those cells which represent a logical "1" will have an additional logic transition in the middle. See the first few paragraphs under Sheet 7 of the Schematic Walkthrough for a brief description of the S/PDIF signal.

The FPGA selects between the A/D data (ADC_IN) and the S/PDIF data (DIG_IN), and sends the selected source to the DSP over DSP_IN_DATA, formatted as follows:

TIME SLOT	ADC_IN	DIG_IN	DSP_IN_DATA	
			ANALOG	DIGITAL
0		L BIT 0	BLK START	BLK START
1	L MSB	L BIT 1	L MSB	
2	L MSB-1	L BIT 2	L MSB-1	PARITY ERR
3	L MSB-2	L BIT 3	L MSB-2	BIPHASE VIOL.
4	L MSB-3	L BIT 4	L MSB-3	R PARITY
5	L MSB-4	L BIT 5	L MSB-4	R CHAN STAT
6	L MSB-5	L BIT 6	L MSB-5	R USER DATA
7	L MSB-6	L BIT 7	L MSB-6	R VALIDITY
8	L MSB-7	L BIT 8	L MSB-7	L BIT 7
9	L MSB-8	L BIT 9	L MSB-8	L BIT 6
10	L MSB-9	L BIT 10	L MSB-9	L BIT 5
11	L MSB-10	L BIT 11	L MSB-10	L BIT 4
12	L MSB-11	L BIT 12	L MSB-11	L BIT 3
13	L MSB-12	L BIT 13	L MSB-12	L BIT 2
14	L MSB-13	L BIT 14	L MSB-13	L BIT 1
15	L MSB-14	L BIT 15	L MSB-14	L BIT 0
16	L MSB-15	L BIT 16	L MSB-15	L BIT 15
17	L MSB-16	L BIT 17	L MSB-16	L BIT 14
18	L MSB-17	L BIT 18	L MSB-17	L BIT 13
19		L BIT 19		L BIT 12
20		L BIT 20		L BIT 11
21		L BIT 21		L BIT 10
22		L BIT 22		L BIT 9
23		L BIT 23		L BIT 8
24		L VALIDITY		L BIT 23
25		L USER		L BIT 22
26		L CHAN STAT		L BIT 21
27		L PARITY		L BIT 20
28		PREAMBLE		L BIT 19
29		PREAMBLE	BIPHASE VIOL.	L BIT 18
30		PREAMBLE	PARITY ERR.	L BIT 17
31		PREAMBLE		L BIT 16
32		R BIT 0	BLOCK START	
33	R MSB	R BIT 1	R MSB	
34	R MSB-1	R BIT 2	R MSB-1	PARITY ERR
35	R MSB-2	R BIT 3	R MSB-2	BIPHASE VIOL
36	R MSB-3	R BIT 4	R MSB-3	L PARITY
37	R MSB-4	R BIT 5	R MSB-4	L CHAN STAT
38	R MSB-5	R BIT 6	R MSB-5	L USER DATA
39	R MSB-6	R BIT 7	R MSB-6	L VALIDITY
40	R MSB-7	R BIT 8	R MSB-7	R BIT 7
41	R MSB-8	R BIT 9	R MSB-8	R BIT 6
42	R MSB-9	R BIT 10	R MSB-9	R BIT 5
43	R MSB-10	R BIT 11	R MSB-10	R BIT 4
44	R MSB-11	R BIT 12	R MSB-11	R BIT 3
45	R MSB-12	R BIT 13	R MSB-12	R BIT 2
46	R MSB-13	R BIT 14	R MSB-13	R BIT 1
47	R MSB-14	R BIT 15	R MSB-14	R BIT 0
48	R MSB-15	R BIT 16	R MSB-15	R BIT 15
49	R MSB-16	R BIT 17	R MSB-16	R BIT 14
50	R MSB-17	R BIT 18	R MSB-17	R BIT 13
51		R BIT 19		R BIT 12
52		R BIT 20		R BIT 11
53		R BIT 21		R BIT 10
54		R BIT 22		R BIT 9
55		R BIT 23		R BIT 8
56		R VALIDITY		R BIT 23

57	R USER		R BIT 22
58	R CHAN STAT		R BIT 21
59	R PARITY		R BIT 20
60	PREAMBLE		R BIT 19
61	PREAMBLE	BIPHASE VIOL.	R BIT 18
62	PREAMBLE	PARITY ERR.	R BIT 17
63	PREAMBLE		R BIT 16

Note that the A/D data is in I²S format, meaning that it is left-justified, MSB-first, starting one cell after the rising and falling edges of FS. When the A/D is selected as a source, the FPGA passes ADC_IN with little processing, except to add some digital status data (biphase violation, parity error). The DSP uses this status data when the user has selected analog data as a source, but frequency-locked to the S/PDIF in. By monitoring these status lines, the DSP can determine whether the clock recovery circuit is locked to the S/PDIF signal.

DIG_IN data is bit-reversed in addition to being modulated. The FPGA buffers 8 bits of demodulated S/PDIF data, reverses them, and sends them to the DSP.

Going in the other direction, DSP_OUT_DATA gets bit-swapped and modulated in the FPGA to become DIG_OUT. In analog out mode, DSP_OUT_DATA is fed directly to the DAC without passing through the FPGA.

TIME SLOT	DSP_OUT_DATA		DIG_OUT
	ANALOG	DIGITAL	
0		R VALIDITY	R BIT 23
1	L MSB	L BIT 7	R VALIDITY
2	L MSB-1	L BIT 6	R USER
3	L MSB-2	L BIT 5	R CHAN STAT
4	L MSB-3	L BIT 4	R PARITY
5	L MSB-4	L BIT 3	PREAMBLE
6	L MSB-5	L BIT 2	PREAMBLE
7	L MSB-6	L BIT 1	PREAMBLE
8	L MSB-7	L BIT 0	PREAMBLE
9	L MSB-8	L BIT 15	L BIT 0
10	L MSB-9	L BIT 14	L BIT 1
11	L MSB-10	L BIT 13	L BIT 2
12	L MSB-11	L BIT 12	L BIT 3
13	L MSB-12	L BIT 11	L BIT 4
14	L MSB-13	L BIT 10	L BIT 5
15	L MSB-14	L BIT 9	L BIT 6
16	L MSB-15	L BIT 8	L BIT 7
17	L MSB-16	L BIT 23	L BIT 8
18	L MSB-17	L BIT 22	L BIT 9
19	L MSB-18	L BIT 21	L BIT 10
20	L MSB-19	L BIT 20	L BIT 11
21		L BIT 19	L BIT 12
22		L BIT 18	L BIT 13
23		L BIT 17	L BIT 14
24		L BIT 16	L BIT 15
25		0	L BIT 16
26		0	L BIT 17
27		0	L BIT 18
28		0	L BIT 19
29		L PARITY	L BIT 20
30		L CHAN STA	L BIT 21
31		L USER DATA	L BIT 22
32		L VALIDITY	L BIT 23
33	R MSB	R BIT 7	L VALIDITY
34	R MSB-1	R BIT 6	L USER
35	R MSB-2	R BIT 5	L CHAN STAT

36	R MSB-3	R BIT 4	L PARITY
37	R MSB-4	R BIT 3	PREAMBLE
38	R MSB-5	R BIT 2	PREAMBLE
39	R MSB-6	R BIT 1	PREAMBLE
40	R MSB-7	R BIT 0	PREAMBLE
41	R MSB-8	R BIT 15	R BIT 0
42	R MSB-9	R BIT 14	R BIT 1
43	R MSB-10	R BIT 13	R BIT 2
44	R MSB-11	R BIT 12	R BIT 3
45	R MSB-12	R BIT 11	R BIT 4
46	R MSB-13	R BIT 10	R BIT 5
47	R MSB-14	R BIT 9	R BIT 6
48	R MSB-15	R BIT 8	R BIT 7
49	R MSB-16	R BIT 23	R BIT 8
50	R MSB-17	R BIT 22	R BIT 9
51	R MSB-18	R BIT 21	R BIT 10
52	R MSB-19	R BIT 20	R BIT 11
53		R BIT 19	R BIT 12
54		R BIT 18	R BIT 13
55		R BIT 17	R BIT 14
56		R BIT 16	R BIT 15
57		BLOCK START	R BIT 16
58		BLOCK START	R BIT 17
59		BLOCK START	R BIT 18
60		BLOCK START	R BIT 19
61		L PARITY	R BIT 20
62		L CHAN STAT	R BIT 21
63		L USER DATA	R BIT 22

2115-Lexichip Communication

The serial link between the 2115 and the Lexichip is broken into 128 time slots organized as 8 bidirectional channels of 16-bit data:

TIME SLOT	DSP_LEX_DATA	LEX_DSP_DATA
9-24	RIGHT REVERB	RIGHT REVERB
25-40	LEFT DELAY	LEFT DELAY 1
41-56	RIGHT DELAY	LEFT DELAY 2
57-72		LEFT DELAY 3
73-88		RIGHT DELAY 1
89-104		RIGHT DELAY 2
105-120		RIGHT DELAY 3
121-8	LEFT REVERB	LEFT REVERB

Signal Names

FS	Digital audio wordclock
4FS	4 x wordclock
8FS	8 x wordclock
10MHZ	10 MHz Z80 master clock
64FS	64 x wordclock
128FS/	128 x wordclock (inverted)
256FS	256 x wordclock
+5VD	+5 Volts Digital
+15VA	+15 Volts Analog
-15VA	-15 Volts Analog
ADC_IN	Serial audio from ADC
ADDR<0:15>	System address bus
BDSP_OUT_DATA	DSP_OUT_DATA, isolated by a resistor
COL<1:5>	LED matrix column drivers
CONTRAST	LCD contrast voltage
CONTRAST<0:3>	LCD contrast voltage control
CONTROL_WR/	System control register write strobe
DATA<0:15>	System data bus
DEG0	Deglitch 0, triggers ZBUSREQ/
DIG_IN	Buffered S/PDIF input signal
DIG_OUT	S/PDIF output signal
DISCHARGE	Sets PLL VCO to bottom of range
DISPLAY_WR1/	LED display write strobe 1
DISPLAY_WR2/	LED display write strobe 2
DONE	FPGA finished initialization
DSP_IN_DATA	Serial audio from ADC or S/PDIF to DSP
DSP_LEX_DATA	Serial audio from 2115 to Lexichip
DSP_BMS/	2115 Boot Memory Select
DSP_DMS/	2115 Data Memory Select
DSP_ON_BUS	Tells ADSP2115 to take over system bus
DSP_OUT_DATA	Serial audio from 2115 to DAC or S/PDIF
ENC<1:2>	Front panel encoder lines
HI_RAM_EN/	SRAM chip select, high byte
INT/	MIDI UART receive interrupt
IO_DATA<0:7>	I/O data bus
IOREQ/	I/O request, shared by Z80 and 2115
LA<0:15>	Lexichip WCS address bus
LABUS<0:9>	Lexichip audio address bus
LAXCA	Lexichip expansion memory Column Address
LAXRA	Lexichip expansion memory Row Address
LCAS/	Lexichip audio Column Address Strobe
LCASX/	Version of LCAS/ for memory expansion
LCD_ADDR1	LCD control/data selector
LCD_EN	LCD read/write strobe
LCD_READ	LCD read/write direction selector
LCD_WR/	LCD control register write strobe
LD<0:19>	Lexichip audio data bus
LEXPHSAB	Asserted during Lexichip phase A and B
LEX_DSP_DATA	Serial audio from Lexichip to 2115
LEX_EN/	Lexichip chip select
LEX_WAIT/	Triggers ZBUSREQ/ in FPGA

LEX_WC/	FS synchronised to Lexichip
LEX_WR/	Lexichip write strobe
LIN	Left analog in from buffer to pot
LINPOT	Left analog in from pot to ADC
LRAS/	Lexichip audio Row Address Strobe
LRASX/	Version of LRAS/ for memory expansion
LOUT	Left analog out from DAC to pot
LOUTPOT	Left analog out from pot to buffer
LO_RAM_RD/	SRAM read strobe, low byte
LO_RAM_WR/	SRAM write strobe, low byte
LWE/	Lexichip audio memory Write Enable
LWEX/	Version of LWE/ for memory expansion
MC/	512 x FS master clock made by Lexichip
MEMX_STAT	Memory expansion present indicator
MIDI_IN	MIDI input signal
MIDI_OUT	MIDI output signal
MOUTSIG<0:5>	Buffered version of MIDI OUT
MTHSIG<0:5>	Buffered versions of MIDI IN to THRU
MUTE/	Mutes analog outputs
MUTE	Level-shifted version of MUTE/
P<15:17>	EPROM bank select address
PEDAL_ADC	Footpedal comparator output
PHASE_DET	S/PDIF clock recovery phase detect
PLLV	Phase-Locked Loop control voltage
PTLRAS/	Pre-termination version of LRAS/
PTLCAS/	Pre-termination version of LCAS/
PTLWE/	Pre-termination version of LWE/
RAM_A14	SRAM bank select
RD/	Read strobe, shared by Z80 and 2115
RD_STATUS	System status read strobe
RESET/	Pre-reset, resets FPGA
RESET1/	System reset generated by FPGA
RESET_DAC	Mutes DAC output
RESET_DSP/	Resets the ADSP2115
RESET_LEX/	Resets the Lexichip
RESET_PEDAL	Starts Footpedal ADC cycle
RIGHT_ROW<0:3>	Right LED matrix row drivers
RIN	Right analog in from buffer to pot
RINPOT	Right analog in from pot to ADC
ROM_EN/	EPROM output enable
ROUT	Right analog out from DAC to pot
ROUTPOT	Right analog out from POT to buffer
SOFT_SAT	Soft saturation enable
SWITCH_ROW<0:3>	LED matrix switch sense lines
WR/	Write strobe, shared by Z80 and 2115
WRITE_PROTECT	Low SRAM write protect
VCO	256FS clock recovered from S/PDIF
VRAM	Battery-backed SRAM power supply
ZBUSACK/	Z80 asserts to release system bus to DSP
ZBUSREQ/	Requests system bus from Z80
ZMREQ/	Z80 memory request strobe
ZRFSH/	Z80 refresh, used to latch P<17:15> in FPGA
ZWAIT/	Z80 wait state request

MAIN BOARD

Parts List

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
RESISTORS				
202-00499	RES,CF,5%,1/2W,27 OHM	2		R83,84
202-07964	RES,MO,5%,1W,330 OHM	2		R81,82
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	13		R57,65,75,80,89 R181,182,184,233,238-241
202-09871	RESSM,RO,5%,1/10W,1K OHM	21	•05/06/96	R44,59,60,74,85-87 R92,218,220,222,224,226-229, R251,253 R255,257,259
202-09871	RESSM,RO,5%,1/10W,1K OHM	22	05/06/96•	R44,59,60,74,85-87,92,218,220, R222,224,226-229,251,253 R255,257,259,260
202-09873	RESSM,RO,5%,1/10W,10K OHM	12		R49-51,90,91,163,178,203,230, R235,247,248
202-09894	RESSM,RO,5%,1/10W,1M OHM	10		R15,17,21,23,27,29,33,35,58,189
202-09897	RESSM,RO,5%,1/10W,470 0HM	2		R166,231
202-09899	RESSM,RO,5%,1/10W,47 OHM	35		R167-177,179,180,183,185-188, R190-198,200-202,204-207,212
202-10466	RESSM,RO,5%,1/10W,20K OHM	1		R236
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	13		R39,41,42,67,69,88,135,137, R208-211,234
202-10558	RESSM,RO,5%,1/10W,47K OHM	11	•04/19/96	R19,25,31,37,40,43,56,66,93, R162,164
202-10558	RESSM,RO,5%,1/10W,47K OHM	7	04/19/96•	R40,43,56,66,93,162,164
202-10569	RESSM,RO,5%,1/10W,10 OHM	5		R94,118,122,126,130
202-10573	RESSM,RO,5%,1/10W,470K OHM	4		R97,98,102,103
202-10574	RESSM,RO,5%,1/10W,10M OHM	1		R165
202-10585	RESSM,RO,5%,1/4W,51 OHM	8		R18,20,24,26,30,32,36,38
202-10586	RESSM,RO,5%,1/4W,100 OHM	18		R48,68,134,136,214-217,219, R221,223,225,242-246,249
202-10834	RESSM,RO,5%,1/4W,5.1 OHM	2		R95,96
202-10891	RESSM,RO,5%,1/10W,270 OHM	2		R99,101
202-11041	RESSM,RO,5%,1/10W,680 OHM	5		R250,252,254,256,258
202-11042	RESSM,RO,5%,1/10W,6.8K OHM	2		R72,73
202-11043	RESSM,RO,5%,1/10W,24K OHM	1		R45
202-11070	RESSM,RO,5%,1/4W,56 OHM	4		R119,120,123,124
202-11071	RESSM,RO,5%,1/4W,75 OHM	9		R55,138,139,143,144,146,147, R151,152
202-11072	RESSM,RO,5%,1/4W,220 0HM	8		R61,62,70,71,76,77,79,213
202-11073	RESSM,RO,5%,1/4W,270 OHM	1		R78
202-11074	RESSM,RO,5%,1/4W,510 OHM	6	•09/05/96	R1,12,16,22,28,34
202-11491	RESSM,RO,5%,1/4W,16 OHM	1		R237
202-11797	RESSM,RO,5%,1/10W,510 OHM	6	09/05/96•	R1,12,16,22,28,34
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	10	•04/19/96	R104,107,111,115,142,145,150, R153,154,158
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	6	•04/19/96	R142,145,150,153,154,158
203-10425	RESSM,RO,1%,1/10W,7.50K OHM	4	04/19/96•	R105,109,112,116
203-10579	RESSM,RO,1%,1/10W,2.49K OHM	1		R47
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	9	04/19/96•	R46,140,148,155-157,159-161

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	13	•04/19/96	R46,104,107,111,115,140,148, R155-157,159-161
203-10584	RESSM,RO,1%,1/10W,12.7K OHM	2		R141,149
203-11075	RESSM,RO,1%,1/10W,95.3 OHM	1		R52
203-11078	RESSM,RO,1%,1/10W,422 OHM	4		R127,129,131,133
203-11079	RESSM,RO,1%,1/10W,715 OHM	2		R53,54
203-11080	RESSM,RO,1%,1/10W,1.15K OHM	2	•04/19/96	R110,117
203-11081	RESSM,RO,1%,1/10W,1.21K OHM	2		R4,9
203-11082	RESSM,RO,1%,1/10W,15.0K OHM	3		R63,64,100
203-11083	RESSM,RO,1%,1/10W,49.9K OHM	8		R2,3,6,7,10,11,13,14
203-11492	RESSM,RO,1%,1/10W,287 OHM	4		R121,125,128,132
203-11493	RESSM,RO,1%,1/10W,3.92K OHM	2		R5,8
203-11494	RESSM,RO,1%,1/10W,8.06K OHM	4	04/19/96•	R106,108,113,114
203-11697	RESSM,RO,1%,1/10W,909 OHM	2	04/19/96•	R110,117
203-11698	RESSM,RO,1%,1/10W,2.61K OHM	4	04/19/96•	R106,108,113,114
203-11699	RESSM,RO,1%,1/10W,14.7K OHM	4	•04/19/96	R105,109,112,116
CAPACITORS				
240-00608	CAP,ELEC,2.2uF,50V,RAD	1		C70
240-00609	CAP,ELEC,10uF,16V,RAD	6		C71,74,76,78,81,83
240-00614	CAP,ELEC,47uF,16V,RAD	1		C86
240-06096	CAP,ELEC,10uF,25V,RAD,NON-POL	12		C1,2,7,10,11,14,92,101,102,106, C108,112
240-06886	CAP,ELEC,4.7uF,25V,AX	1		C51
240-07335	CAP,ELEC,47uF,25V,RAD,NON-POL	4	•04/19/96	C19,22,25,28
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	3		C57,58,65
241-11799	CAPSM,TANT,4.7uF,6.3V,20%	1	08/15/96•	C123
244-06173	CAP,MYL,4700pF,5%,RAD	4		C88,91,97,100
244-06883	CAP,MYL,.01uF,5%,RAD	3		C32,95,96
244-10423	CAP,MYL,.22UF,10,RAD	5		C55,60,61,63,67
245-09291	CAPSM,CER,470pF,50V,NPO,5%	3		C69,84,87
245-09875	CAPSM,CER,.1uF,50V,Z5U,20%	64	•08/15/96	C5,6,18,21,24,27,33,34,36,38,40,42 C45,46,48,53,68,72,73,75,77,79,80, C82,85,93,94,104,105,110,111, C115,116,119,120,122-125,128,129 C132-153,155
245-09875	CAPSM,CER,.1uF,50V,Z5U,20%	63	08/15/96•	C5,6,18,21,24,27,33,34,36,38,40,42 C45,46,48,53,68,72,73,75,77,79,80 C82,85,93,94,104,105,110,111,115, C116,119,120,122,124,125,128 C129,132-153,155
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	4		C37,41,154,156
245-09895	CAPSM,CER,10pF,50V,COG,10%	10		C3,4,8,9,114,117,118,121,130,131
245-10544	CAPSM,CER,220pF,50V,NPO,5%	4	04/19/96•	C89,90,98,99
245-10561	CAPSM,CER,100pF,50V,COG,5%	6		C44,47,49,50,52,54
245-10562	CAPSM,CER,150pF,50V,10%	20	•04/19/96	C12,13,15-17,20,23,26,29-31,56,59, C62,64,66,89,90,98,99
245-10562	CAPSM,CER,150pF,50V,10%	16	04/19/96•	C12,13,15-17,20,23,26,29-31,56,59, C62,64,66
245-10587	CAPSM,CER,18pF,50V,COG,10%	4		C126,127,157,158
245-10588	CAPSM,CER,33pF,50V,COG,10%	5		C43,103,107,109,113
FERRITE BEAD				
270-00779	FERRITE,BEAD	14		FB1-14
270-06671	FERRITE CHOKE,2.5 TURN	3		FB15-17

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
DIODES				
300-10414	DIODE,VARACTOR,BB911	3		D15-17
300-10509	DIODESM,1N914,SOT23	6		D14,18-22
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	13		D1-13
TRANSISTORS				
310-01003	TRANSISTOR,MPS2369	1		Q8
310-06612	TRANSISTOR,J108	4		Q1-4
310-10422	TRANSISTORSM,2N4403,SOT23	9		Q15,17,21,23,34-38
310-10510	TRANSISTORSM,2N3904,SOT23	6		Q6,7,10,11,13,19
310-10565	TRANSISTORSM,2N3906,SOT23	5		Q5,12,14,20,25
310-10566	TRANSISTORSM,2N4401,SOT23	12		Q16,18,22,24,26-33
310-11365	TRANSISTOR,PN5910,PNP,HI SPEED	1		Q9
ICs				
330-09350	IC,DIGITAL,LEXICHIP 2A	1		U17
330-09877	ICSM,DIGITAL,74HC174,SOIC	2		U16,19
330-10417	ICSM,DIGITAL,74HC00,SOIC	1		U3
330-10523	ICSM,DIGITAL,74HCU04,SOIC	2		U4,14
330-10527	ICSM,DIGITAL,74HC138,SOIC	1		U33
330-10533	ICSM,DIGITAL,74HC245,SOIC	1		U30
330-10534	ICSM,DIGITAL,74HC259,SOIC	1		U18
330-10535	ICSM,DIGITAL,74AC273,SOIC	1		U31
330-10536	ICSM,DIGITAL,74HC273,SOIC	2		U27,29
330-11094	ICSM,DIGITAL,74HC257,SOIC	1		U32
340-10552	ICSM,LIN,MC33078,DU OPAMP,SOIC	6		U1,9-13
340-10567	ICSM,LIN,MC34164,+5V MON,SOIC	1		U6
340-11045	ICSM,LIN,LM393,DUAL COMP,SOIC	1		U2
350-10373	ICSM,DRAM,256KX16,80NS,SOJ	1		U25
350-10374	ICSM,DRAM,256KX4,80NS,SOJ	1		U26
350-10545	ICSM,SRAM,8KX8,80NS,SOP,50uA	1		U21
350-11046	ICSM,SRAM,32KX8,85NS,SOP,20UA	1		U22
350-11084	ICSM,FPGA,3042A,10X10,7NS,PLCC	1		U15
350-11478	IC,ROM,27C020,MPX 1,V1.00	1		U23
355-11085	ICSM,DAC,CS4329,20BIT,SSOP	1		U7
355-11091	ICSM,ADC,SAA7360,18BIT,QFP	1		U8
365-11047	ICSM,UPROC,ADSP2115,PLCC	1		U20
365-11092	ICSM,UPROC,Z80,CMOS,10MHZ,PLCC	1		U24
375-02247	IC,OPTO-ISOLATOR,6N138	1		U5
CRYSTALS				
390-09075	RESONATOR,CER,11.3MHz	1		Y1
390-10515	CRYSTAL,10.0MHz,PAR	1		Y2
390-11048	CRYSTAL,22.5792MHZ,.005%,PAR	1		Y3
390-11468	CRYSTAL,25.0000MHz,.005%,PAR	1		Y4
RELAYS/SWITCHES				
453-11090	SW,PBM,4P2T,5MMDIA,PCRA,BLK	1		SW1
BATTERIES				
460-04598	BATTERY,LITH,3V,FLAT	1		BAT1

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
CONNECTORS				
510-06042	CONN,DC POWER,PC,DJ005,2.5MM	1		J15
510-07785	CONN,RCA,PCRA,1FCGX2,VERT	1		J11
510-09790	CONN,DIN,5FC@180DEG,PCRA,SHLD	2		J12,13
510-10881	CONN,XLR,3MC,PCRA,PLASTIC CMPT	2		J5,8
510-10984	CONN,JMP,.6X2.5MM,16FC,TRAP	1		J20
510-11049	CONN,DIN,7FC@270DEG,PCRA,SHLD	1		J14
510-11086	CONN,XLR,3FC,PCRA,LATCH,SMALL	2		J1,4
510-11087	1/4"PH JACK,PCRA,3C,SW-TR,G,FT	6		J2,3,6,7,9,10
510-11390	CONN,POST,079,HDR,16MC,LC	1		J21
510-11391	CONN,POST,079,HDR,15MC,LC	2		J18,19
SOCKETS				
520-09736	IC,SCKT,32 PIN,PC,TIN,LO-PRO	1		U23
LUGS/SPACERS				
620-10413	LUG,#2,INT STAR,RCA GND	1		J11 RCA CONN
CABLES				
680-11067	CABLE,.156,HSG/ST&T,6C,9.5"	1		J16

FRONT PANEL LEVEL POT BOARD

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
POTENTIOMETERS				
200-11293	POT,RTY,PC,10KAX2,6MMFL,16,30L	2		R7,8
CABLES				
680-11296	CABLE,079,SCKT/SCKTRA,15C,2.5"	1		J2 TO MAIN BD (J18)

FRONT PANEL HEADROOM/DISPLAY BOARD

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
DISPLAYS/INDICATORS				
430-03896	LED,GRN,RECT,.197X.079	10		D2-6,8-12
430-03898	LED,RED,RECT,.197X.079	2		D1,7
430-11088	LED,DSPLY,7-SEG,GRN,3DIG,.56	1		DISP1
CABLES				
680-11296	CABLE,079,SCKT/SCKTRA,15C,2.5"	1		J1 TO MAIN BD (J19)

MECHANICAL/MISC

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
DISPLAYS/INDICATORS				
430-11089	DISP,LCD,16X2,NEG,LED,GN	1		TO MAIN BD (J20)
RELAYS/SWITCHES				
454-11095	SW,ROCKER,1P2T,6A@250,VERTSLIM	1		PWR SWITCH
KNOBS				
550-11063	KNOB,.84,6MM/FL,BLK	1		ENCODER
550-11064	KNOB,.61,6MM/FL,BLK,LINE	2		LEVEL POTS
GASKETS				
630-11484	GASKET,KEYPAD,3X3,MPX 1	1		SW ASSY
SCREWS				
640-10467	SCRW,M3X6MM,FH,PH,BZ	4		FP ASSY TO CHASSIS INSERT
640-10498	SCRW,M3X6MM,PNH,PH,BZ	14		MAIN BD TO CHAS (2) PWR SUP TO CHAS (4) CVR TO CHAS REAR (4) BRKT TO CVR/CHAS/INS(4)
641-09699	SCRW,TAP,AB,#2X5/16,PNH,PH,ZN	5	•12/04/96	DIN CONN TO CHAS (3) DISPLAY TO INSERT(2)
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	9		RCA CONN TO CHAS (1) XLR CONN TO CHAS (8)
641-11834	SCRW,TAP,AB,#2X1/4,PNH,PH,ZN	5	12/04/96•	DIN CONN TO CHAS (3) DISPLAY TO INSERT(2)
NUTS				
643-10492	NUT,M4X.7MM,KEP,ZN	1		CHASSIS GND
WASHERS/RIVETS				
644-01747	WSHR,INT STAR,#4	1		PWR SUP GND
644-08899	WSHR,FL,#2CLX.186ODX.03THK,NYL	1		DISPLAY TO INSERT
644-10494	WSHR,FL,M4CLX9ODX.8MM THK	1		CHASSIS GND
650-10427	RVT,SNAP-IN,.12DIA,NYL	5		SW ASSY (3) & HDRM BD (2) TO INSERT
CABLES				
680-11068	CABLE,AC PWR,2C,SHLD,10"	1		PS TO AC CONN & PWR SW
680-11295	CABLE,079,SCKT/SCKT,16C,2.5"	1		SW ASSY TO MAIN(J21)
MECHANICALS				
541-00781	BUMPER,FEET,3-M #SJ5018	4		
700-11056	CHASSIS,1UX9,MPX 1	1		
700-11059	COVER,1UX9	1		
700-11060	CHASSIS,INSERT,FP,MPX 1	1		
701-11061	BRACKET,MTG,RACK,1U,MPX 1	2		
702-11050	PANEL,FRONT,MPX 1	1		
702-11490	COVER,PROT,PS,2.9X5.7	1		INSIDE TOP COVER
703-11054	LENS,6.2X1.25,MPX 1	1		
750-11028	ASSY,PCB/SW/CAP,9SM/10LG,MPX 1	1		
POWER SUPPLIES				
750-11062	PWR SUP,+5V@2A,+-15@1.5/.2,25W	1		

PART NO.	DESCRIPTION	QTY	EFF•INACT	REFERENCE
POWER CORDS				
680-09149	CORD,POWER,NA/IEC,SVT,VW-1,10A	1		N.AMER
680-08830	CORD,POWER,IEC,6A,2M,EURO	1		EURO
680-10093	CORD,POWER,IEC,5A,2M,UK	1		UK
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1		ITALY
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1		SWITZERLAND
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1		AUSTRALIA
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1		JAPAN
680-10098	CORD,POWER,IEC,6A,2M,UNIVERSAL	1		UNIVERSAL

7

Schematics and Assembly Drawings

060-11018	Schematic, Main Board
	Main Bd Component Layout
060-11027	Schematic, FP Boards
	PC Bds FP Component Layout
060-11031	Schematic, Sw Bd Assy
080-11069	Assy Chassis

Lexicon, Inc.
3 Oak Park
Bedford MA
01730-1441
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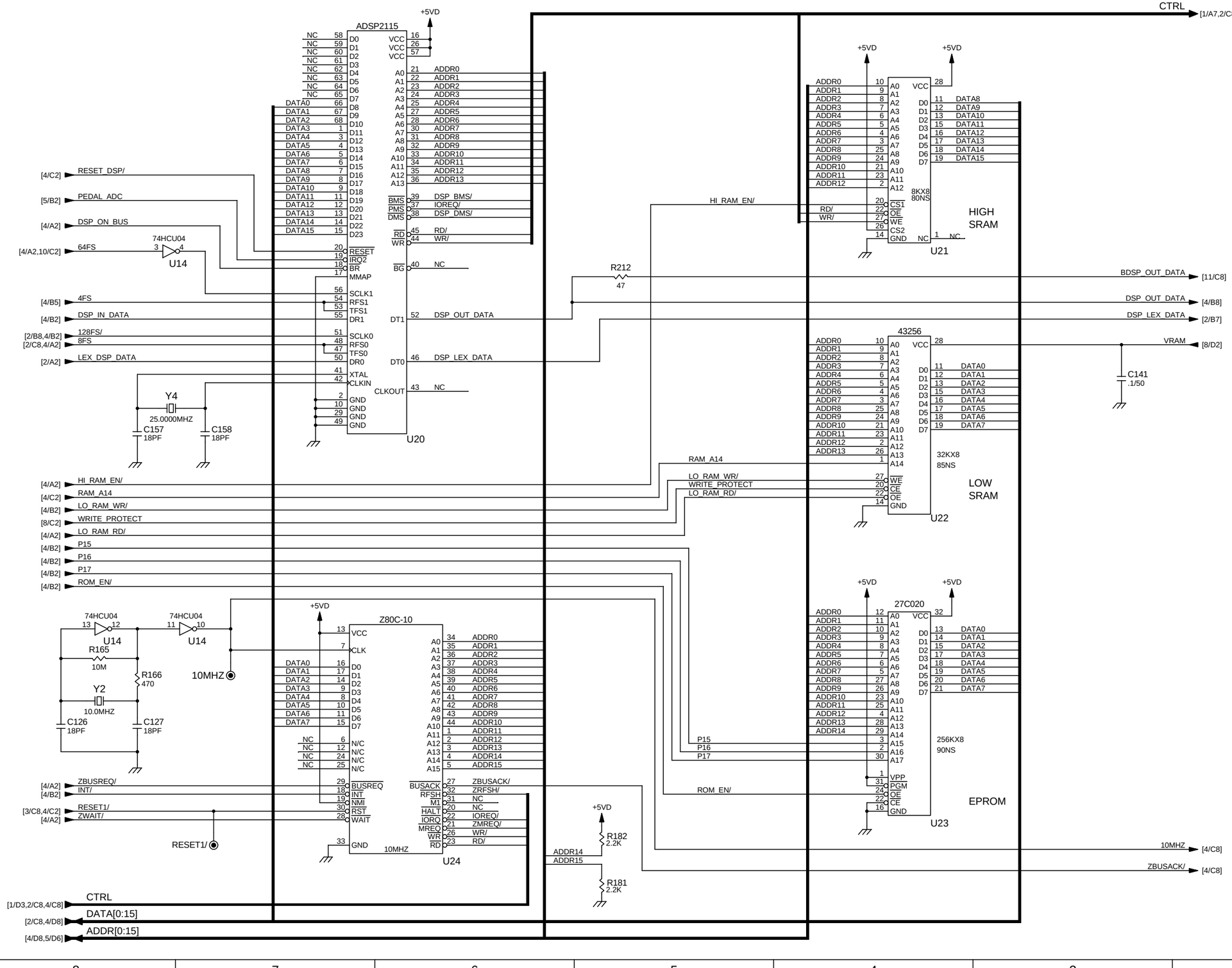
Lexicon Part No. 070-12180

Printed in U.S.A.



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN; ADDED Y4, C157, & C158 PER ECO 960314-00	RWH 3/18/96 JM'A 4/1/96	CW 4/2/96 BAC 4/2/96
2	CHANGED U23 SYMBOL AND SHEETS 11 & 12 PER ECO 960418-00	RWH 4/19/96 JM'A 4/22/96	CW 4/22/96 BAC 4/19/96
3	CHANGED NOTE 6 AND SHEETS 6 & 9 PER ECO 960502-00	RWH 5/2/96 JM'A 5/2/96	CW 5/2/96 BAC 5/2/96
4	CHANGED SHEET 11 PER ECO 960626-00	RWH 7/23/96 BAC 7/24/96	CW 7/24/96 JM'A 7/24/96
5	CHANGED SHEET 9 PER ECO 960812-00. CHANGED SHEETS 9 & 12 PER ECO 960827-00	RWH 9/10/96 BAC 9/11/96	CW 9/11/96 BAC 9/11/96
6	CHANGED SHEET 7 PER ECO 970922-01 UPDATED ADDRESS ON ALL PAGES	MTC 9/30/97 JJF 10/8/97	CW 10/16/97 BAC 10/16/97
7	CHANGED SHEET 6 PER ECO 980601-00	RWH 6/4/98 BAC 6/4/98	CW 6/5/98 BAC 6/5/98
8	CHANGED PER DCR 000414-00	RWH 4/17/00 ECM 4/18/00	CW 5/19/00 ECM 5/22/00
9	CHANGED SHT. 10 PER ECO 000517-00	RWH 5/18/00 ECM 5/18/00	CW 5/22/00 ECM 5/22/00
10	CHANGED SHT. 10 PER ECO 000517-00-A	RWH 5/26/00 ECM 5/26/00	CW 5/26/00 ECM 5/26/00

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: BAT1, C158, D22, FB19, J21, Q38, R261, SW1, U33, W2, Y4

7 COMPONENTS MARKED WITH * ARE NOT INSTALLED.

DOCUMENT CONTROL BLOCK: #060-11018	
SHEET NUMBER	REVISION NUMBER
1 OF 13	10
2 OF 13	3
3 OF 13	3
4 OF 13	3
5 OF 13	3
6 OF 13	5
7 OF 13	3
8 OF 13	3
9 OF 13	5
10 OF 13	5
11 OF 13	5
12 OF 13	5
13 OF 13	3

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

TITLE: SCHEM, MAIN BD, MPX 1 Z80, DSP

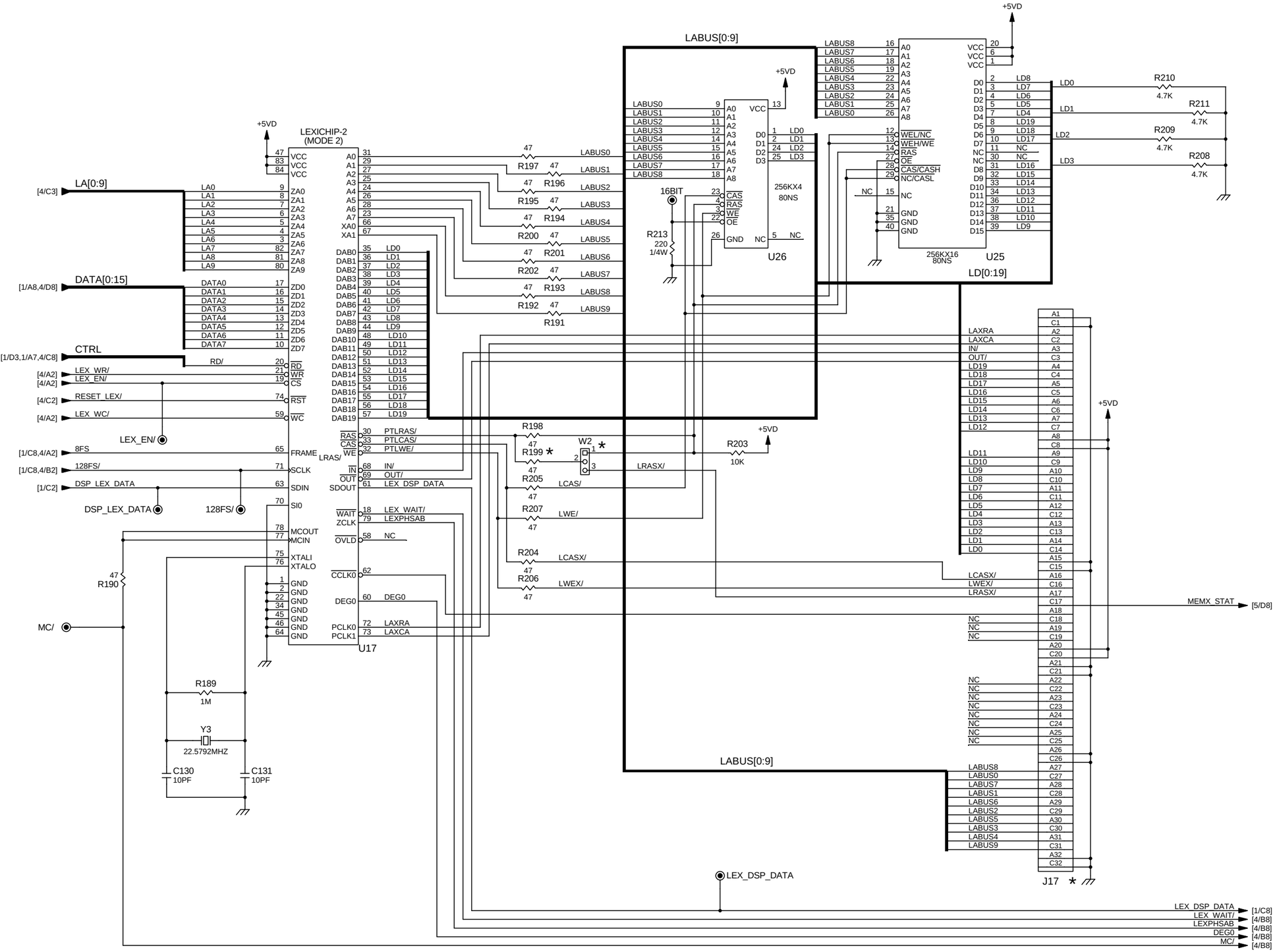
SIZE	CODE	NUMBER	REV
B		060-11018	10

FILE NAME: 11018-10.1

SHEET 1 OF 13

5-26-2000_11:59

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	SCHEM, MAIN BD, MPX 1 LEXICHIP
DRAWN BAC	1/15/96	SIZE B	CODE / NUMBER 060-11018 / REV 3
CHECKED JM'A	1/26/96		
Q.C. CW	4/2/96	FILE NAME 11018-8.2	SHEET 2 OF 13
ISSUED BAC	4/2/96		

5-22-2000_10:53

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00

COLUMN DRIVERS

+5VD

RIGHT_ROW[0:3]

RIGHT DISPLAY

IO_DATA[0:7]

[4/D4,5/D8]

74AC273

U31

DISPLAY_WR1/

[4/B2]

RESET1/

[1/A8,4/C2]

74HC138

U33

R258 680 2N4403 Q38

R256 680 2N4403 Q37

R254 680 2N4403 Q36

R252 680 2N4403 Q35

R250 680 2N4403 Q34

R251 1K

R253 1K

R259 1K

R255 1K

R257 1K

R245 100 1/4W

R244 100 1/4W

R243 100 1/4W

R242 100 1/4W

RIGHT_ROW0

RIGHT_ROW1

RIGHT_ROW2

RIGHT_ROW3

RIGHT ROW DRIVERS

J21

SWITCH_ROW[0:3] [5/C8]

ENC1 [5/B8]

ENC3 [5/C5]

LEFT DISPLAY

J19

LEFT ROW DRIVERS

R224 1K 2N4401 Q29

R222 1K 2N4401 Q28

R220 1K 2N4401 Q27

R218 1K 2N4401 Q26

R229 1K 2N4401 Q33

R228 1K 2N4401 Q32

R227 1K 2N4401 Q31

R226 1K 2N4401 Q30

R217 100 1/4W

R216 100 1/4W

R215 100 1/4W

R214 100 1/4W

R225 100 1/4W

R223 100 1/4W

R221 100 1/4W

R219 100 1/4W

74HC273

U27

DISPLAY_WR2/

74HC273

U29

LCD_WR/

RESET/

R236 20K

R235 10K

R234 4.7K

R233 2.2K

R232 UNKNOWN *

-15VA

R231 470

CONTRAST [5/A8]

LCD_READ [5/A8]

LCD_ADDR1 [5/A8]

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

TITLE: SCHEM, MAIN BD, MPX 1 DISPLAY DRIVER

SIZE	CODE	NUMBER	REV
B		060-11018	3

FILE NAME: 11018-8.3 SHEET 3 OF 13

5-22-2000_10:52

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00

IO_DATA[0:7] [3/D8,5/D8]

ADDR[0:15] [1/A7,5/D6]

LA[0:9] [2/D8]

DATA[0:15] [1/A8,2/C8]

CTRL [1/D3,1/A7,2/C8]

74HC245 U30

74HC174 U16 — LEXICHIP ADDRESS LATCH

74HC174 U19

LEXPHSDA

XC3042 MODE 6 U15

74HC259 U18

74HC00 U3

74HCU04 U4

R178 10K, R184 2.2K

R169 47

R177 47

R175 47

R180 47

R179 47

R171 47

R170 47

R168 47

R167 47

R172 47

R173 47

R174 47

R183 47, R187 47, R185 47, R176 47, R188 47, R186 47

RESET/ [3/A8,8/C2] [1/B5]

VCO [7/B2] ZBUSACK/ [1/A2]

LEXPHSAB [2/A2]

DSP_OUT_DATA [1/C2]
MC/ [2/A2]
DEG0 [2/A2]
LEX_WAIT/ [2/A2]
DIG_IN [7/C2]

ADC_IN [10/C2]
MIDI_IN [6/C2]

RESET_DSP/ [1/D8,10/C2]
MUTE/ [9/A8]
RESET_LEX/ [2/C8]
RESET_PEDAL [5/A8]
SOFT_SAT [10/B7]
DISCHARGE [7/A8]
RESET_DAC/ [11/C7]

RESET1/ [1/A8,3/C8]
RAM_A14 [1/B8]
DIG_OUT [7/D8]
ROM_EN/ [1/B8]
128FS/ [1/C8,2/B8]
DSP_IN_DATA [1/C8]
P15 [1/B8]
P16 [1/B8]
P17 [1/B8]
LO_RAM_WR/ [1/B8]
DISPLAY_WR1/ [3/C8]
DISPLAY_WR2/ [3/B8]
INT/ [1/A8]
MIDI_OUT [6/B8]
4FS [1/C8]
256FS [10/C2,11/B8]
LCD_WR/ [3/A8]
FS [10/C2,11/B8]
8FS [1/C8,2/C8]
64FS [1/C8,10/C2,11/B8]

PHASE_DET [7/B8]
LEX_WR/ [2/C8]
LEX_WC/ [2/C8]
LCD_EN [5/A8]
ZWAIT/ [1/A8]
LEX_EN/ [2/C8]
RD_STATUS/ [5/D8]
HI_RAM_EN/ [1/B8]
LO_RAM_RD/ [1/B8]
ZBUSREQ/ [1/A8]
DSP_ON_BUS [1/C8]

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

TITLE: SCHEM, MAIN BD, MPX 1 FPGA

SIZE	CODE	NUMBER	REV
B		060-11018	3

FILE NAME 11018-8.4 SHEET 4 OF 13

5-22-2000_10:51

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00

ADDR[0:15]
[1/A7,4/D8]

IO_DATA[7]
[3/D8,4/D4]

[2/B2] MEMX_STAT
[4/A2] RD_STATUS/

74HC257 U28
IO_DATA4, IO_DATA5, IO_DATA6, IO_DATA7
RD_STATUS/
ADDR4

R230 10K

+5VD

R40 47K
R43 47K

[3/C3] SWITCH_ROW[0:3]
SWITCH_ROW0
SWITCH_ROW1
SWITCH_ROW2
SWITCH_ROW3

74HC257 U32
IO_DATA0, IO_DATA1, IO_DATA2, IO_DATA3
RD_STATUS/
ADDR4

R238 2.2K
R239 2.2K
R241 2.2K
R240 2.2K

FOOTSWITCHES
J9
R41 4.7K
R39 4.7K
D10 BAV99
D9 BAV99
C29 150PF
C30 150PF

ENCODER
R247 10K
R248 10K
[3/D2] ENC1
[3/C2] ENC3
R246 100 1/4W
R249 100 1/4W
C154 .01/50
C156 .01/50

PEDAL
J10
R44 1K
R42 4.7K
D11 BAV99
C31 150PF
C33 .1/50
LM393 U2
R49 10K
PEDAL_ADC
[1/D8]

LCD
J20
[3/A2] CONTRAST
[3/A2] LCD_ADDR1
[3/A2] LCD_READ
[4/A2] LCD_EN
IO_DATA0
IO_DATA1
IO_DATA2
IO_DATA3
IO_DATA4
IO_DATA5
IO_DATA6
IO_DATA7
R237 16 1/4W

FOOTPEDAL A/D
R47 2.49K 1%
R45 24K
2N3906 Q5
12V
R46 10.0K 1%
R48 100 1/4W
.1MA
C32 .01/250
R50 10K
R51 10K
LM393 U2
[4/C2] RESET_PEDAL
RESET_PEDAL

CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

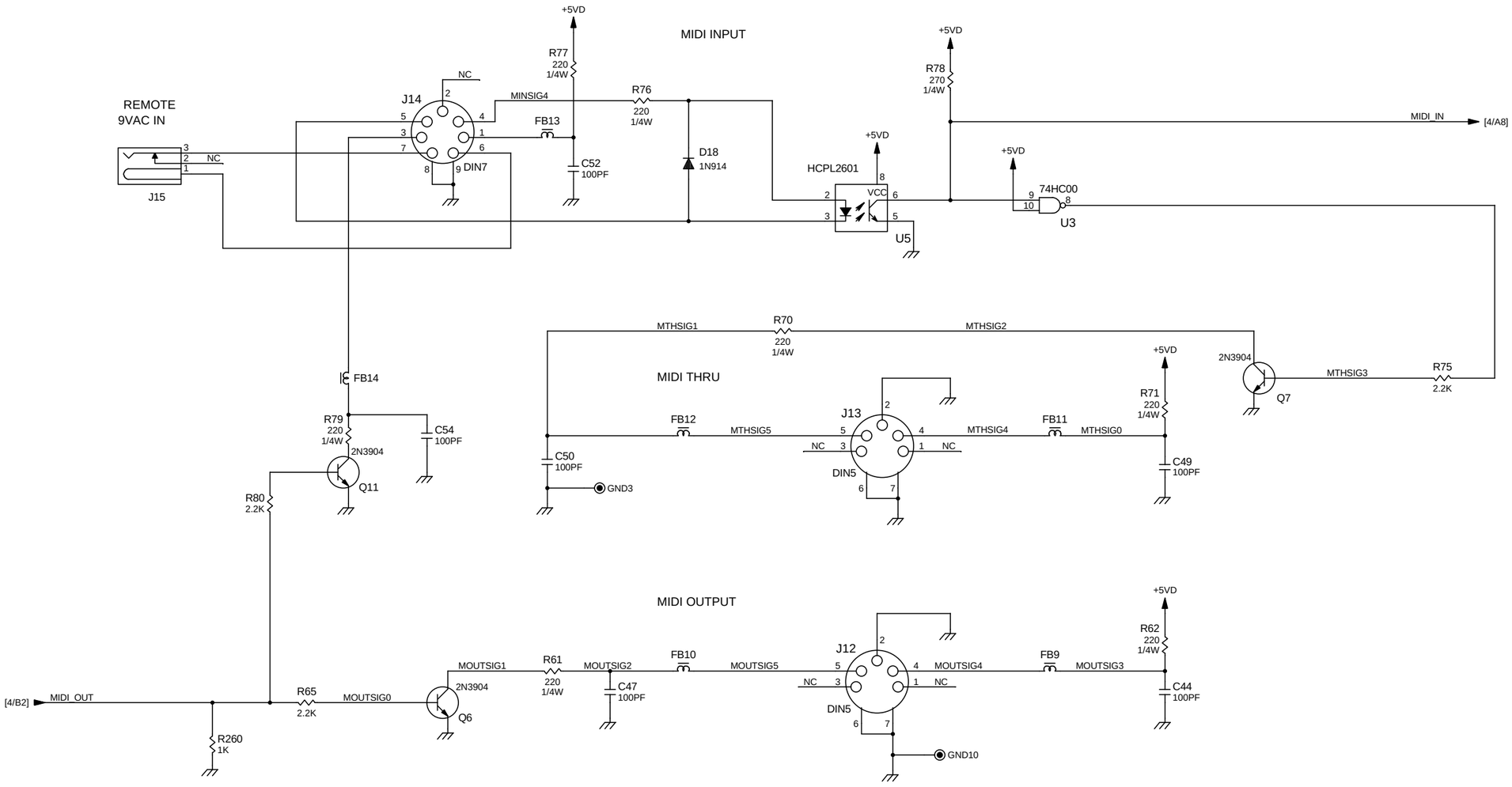
TITLE: SCHEM, MAIN BD, MPX 1 INPUTS

SIZE	CODE	NUMBER	REV
B		060-11018	3

FILE NAME: 11018-8.5
SHEET 5 OF 13

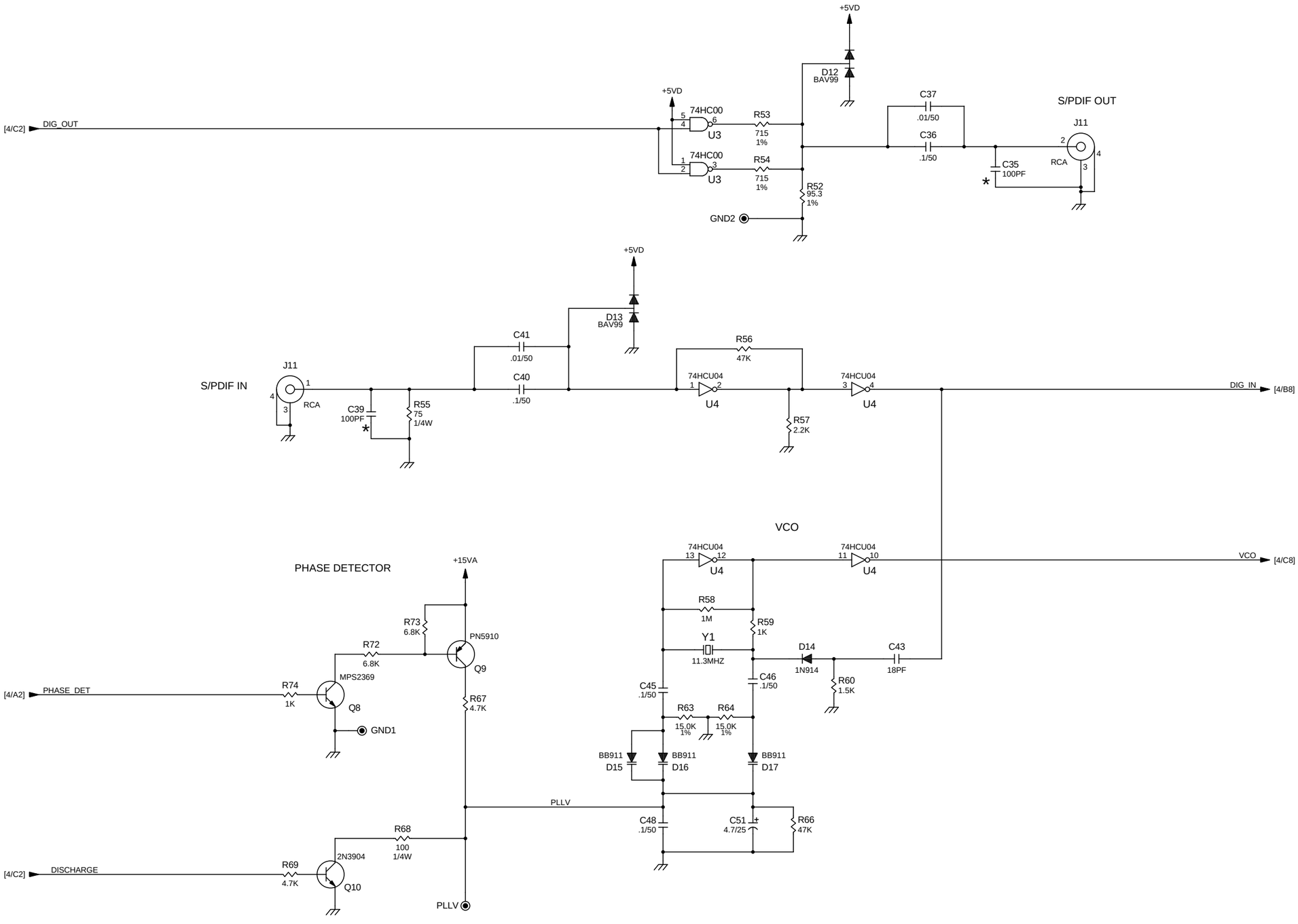
5-22-2000_10:51

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	ADDED R260 PER ECO 960502-00	RWH 5/2/96	CW 5/2/96
		JM'A 5/2/96	BAC 5/2/96
3	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
4	CHANGED U5 PER ECO 980601-00	RWH 6/4/98	CW 6/5/98
		BAC 6/4/98	BAC 6/5/98
5	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE	
DRAWN BAC	1/15/96	SCHEM, MAIN BD, MPX 1 MIDI	
CHECKED JM'A	1/26/96	SIZE B / CODE / NUMBER 060-11018 / REV 5	
Q.C. CW	4/2/96	FILE NAME 11018-8.6	SHEET 6 OF 13
ISSUED BAC	4/2/96		

5-22-2000_10:51



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	CHANGED R60 + C43 VALUES PER ECO #970922-01 UPDATED ADDRESS	MTC 9/30/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

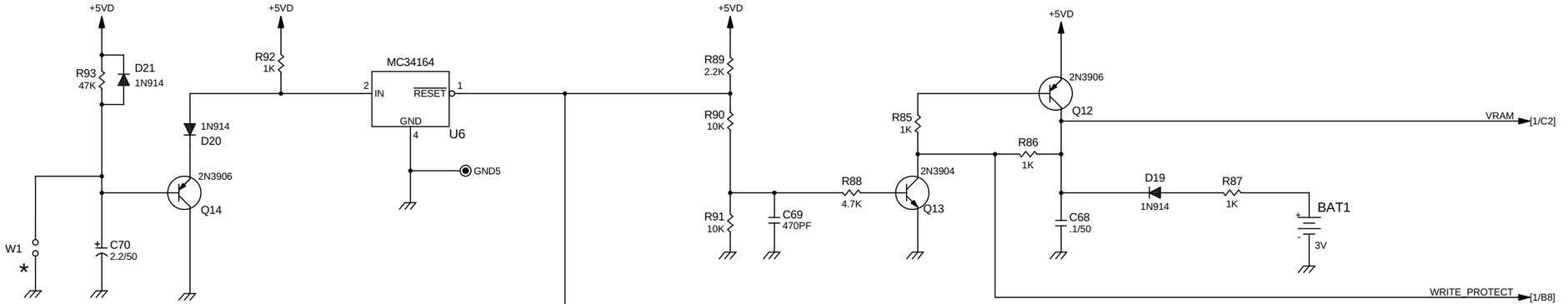
TITLE: SCHEM, MAIN BD, MPX 1 S/PDIF I/O

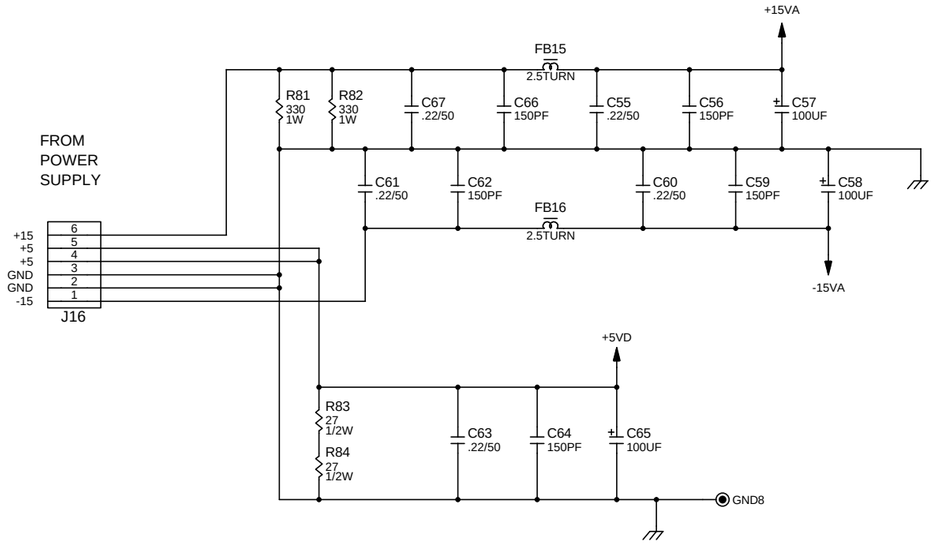
SIZE	CODE	NUMBER	REV
B		060-11018	3

FILE NAME: 11018-8.7

SHEET 7 OF 13

5-22-2000_10:51





REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

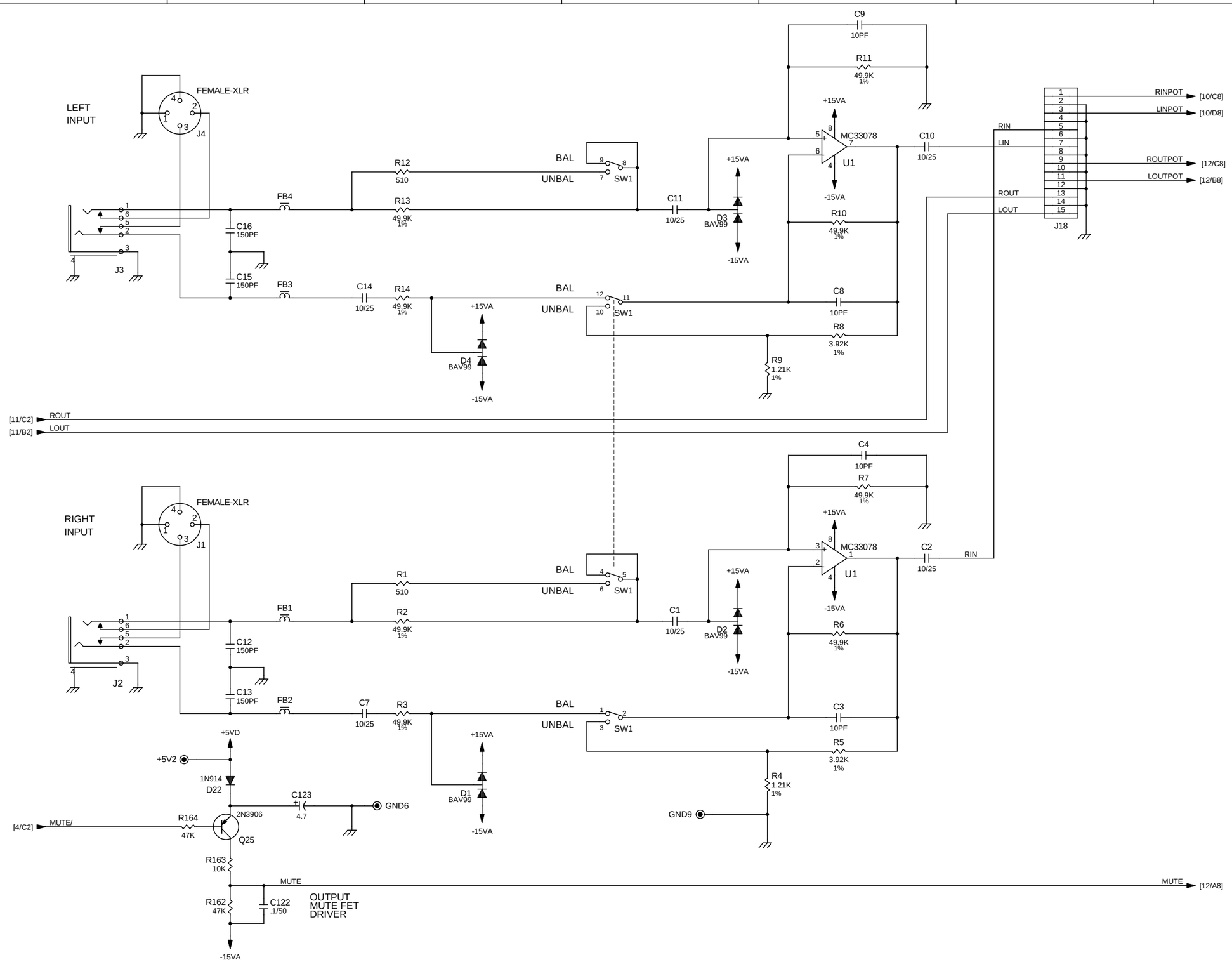
TITLE: SCHEM, MAIN BD, MPX 1 RESET,PS

SIZE	CODE	NUMBER	REV
B		060-11018	3

FILE NAME: 11018-8.8

SHEET 8 OF 13

5-22-2000_10:50



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	REVISED XLR WIRING PER ECO 960502-00	RWH 5/2/96	CW 5/2/96
		JM'A 5/2/96	BAC 5/2/96
3	CHANGED C123 PER ECO 960812-00. CHANGED R1,12 PER ECO 960827-00	RWH 9/10/96	CW 9/11/96
		BAC 9/11/96	BAC 9/11/96
4	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
5	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

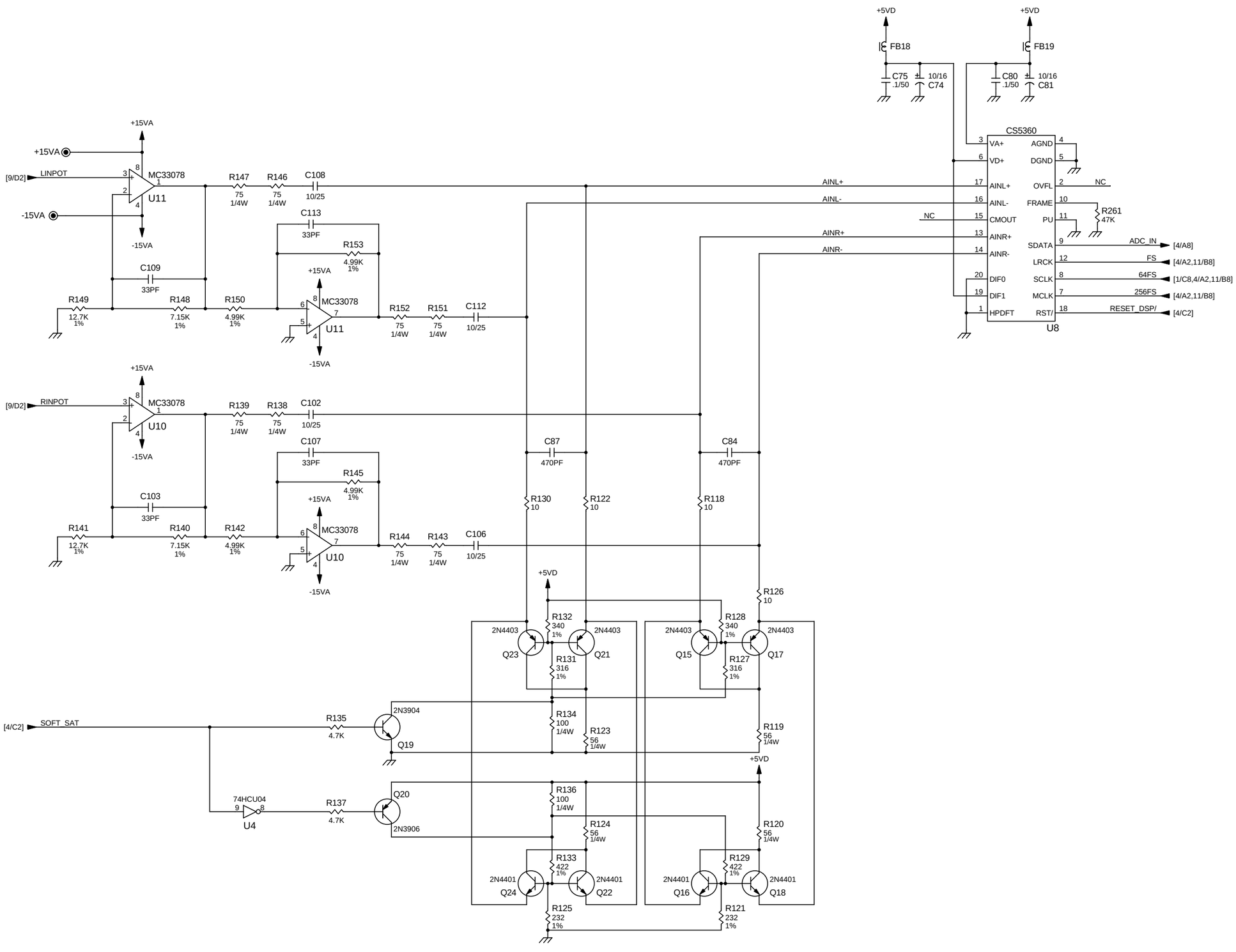
TITLE: SCHEM, MAIN BD, MPX 1 ANALOG INPUTS

SIZE	CODE	NUMBER	REV
B		060-11018	5

FILE NAME: 11018-8.9

SHEET 9 OF 13

5-22-2000_10:49



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00
4	CHANGED PER ECO 000517-00	RWH 5/18/00	CW 5/22/00
		ECM 5/18/00	ECM 5/22/00
5	CHANGED PER ECO 000517-00-A	RWH 5/26/00	CW 5/26/00
		ECM 5/26/00	ECM 5/26/00

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

TITLE: SCHEM, MAIN BD, MPX 1 A/D

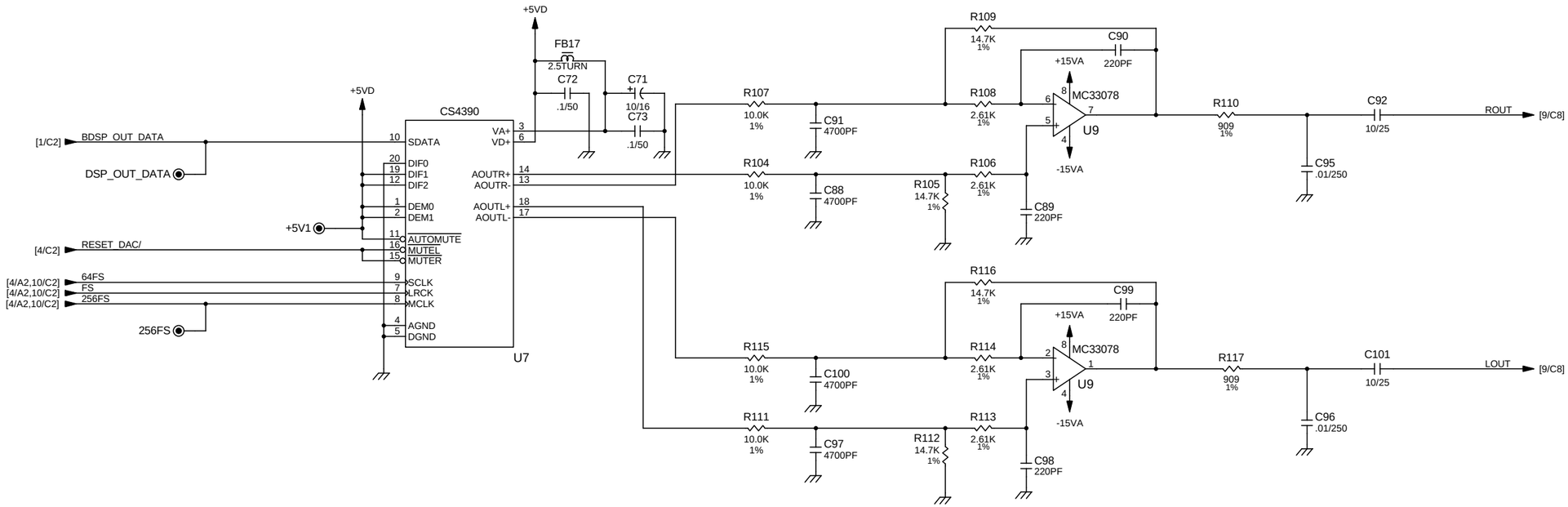
SIZE	CODE	NUMBER	REV
B		060-11018	5

FILE NAME: 11018-10.10

SHEET 10 OF 13

5-26-2000_11:59

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	CHANGED DAC OUTPUT FILTER RC VALUES PER ECO 960418-00	RWH 4/19/96	CW 4/22/96
		JM'A 4/22/96	BAC 4/19/96
3	TIED AUTOMUTE HIGH PER ECO 960626-00	RWH 7/23/96	CW 7/24/96
		BAC 7/24/96	JM'A 7/24/96
4	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
5	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00



CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	BAC	1/15/96
CHECKED	JM'A	1/26/96
Q.C.	CW	4/2/96
ISSUED	BAC	4/2/96

TITLE: SCHEM, MAIN BD, MPX 1 D/A

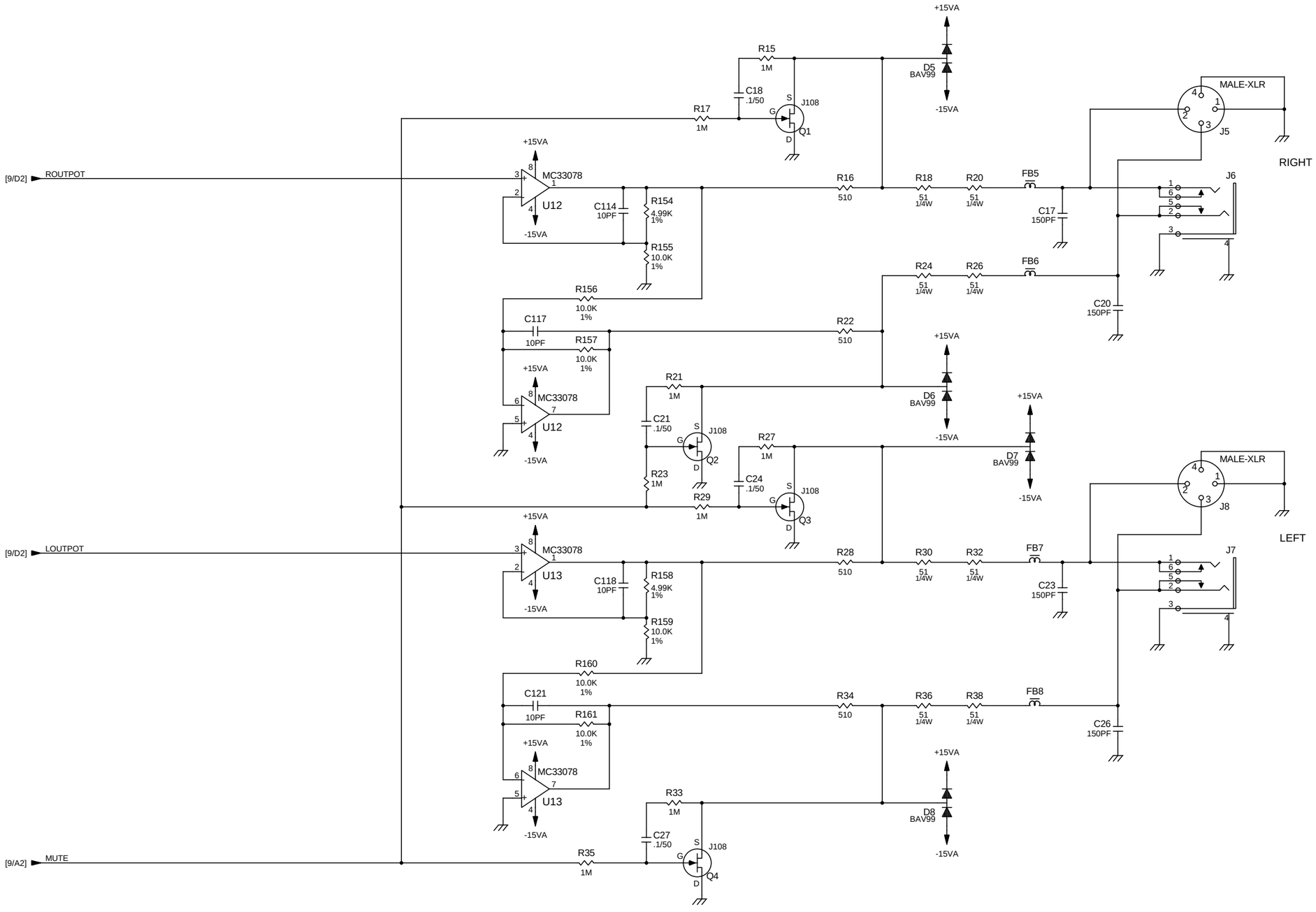
SIZE	CODE	NUMBER	REV
B		060-11018	5

FILE NAME: 11018-8.11

SHEET 11 OF 13

5-22-2000_10:54

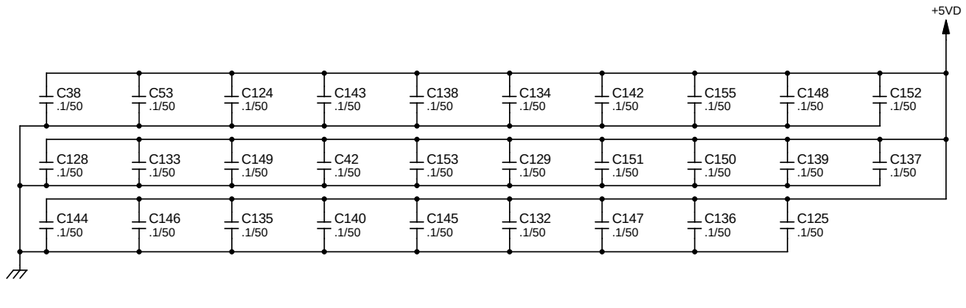
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	DELETE C19, C22, C25, C28, R19, R25, R31, & R37 PER ECO 960418-00	RWH 4/19/96	CW 4/22/96
		JM'A 4/22/96	BAC 4/19/96
3	CHANGED R16,22,28,34 PER ECO 960827-00	RWH 9/10/96	CW 9/11/96
		BAC 9/11/96	BAC 9/11/96
4	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
5	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00

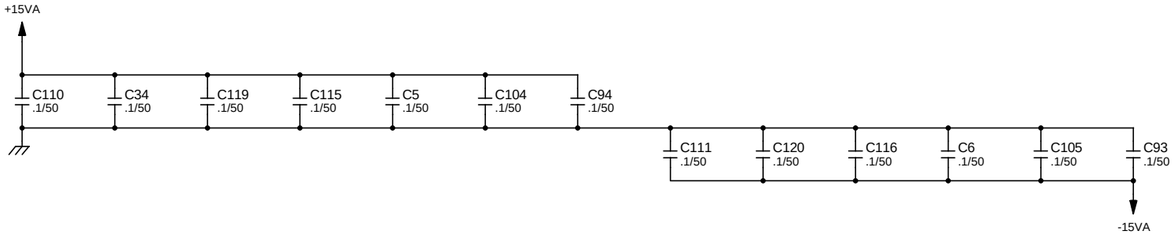


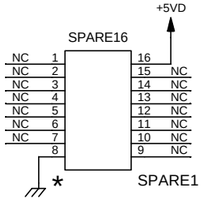
CONTRACT NO.	Lexicon 3 OAK PARK BEDFORD, MA 01730		
APPROVALS	DATE	TITLE: SCHEM, MAIN BD, MPX 1 ANALOG OUT	
DRAWN BAC	1/15/96	SIZE B	CODE
CHECKED JM'A	1/26/96	NUMBER 060-11018	REV 5
Q.C. CW	4/2/96	FILE NAME 11018-8.12	SHEET 12 OF 13
ISSUED BAC	4/2/96		

5-22-2000_10:50

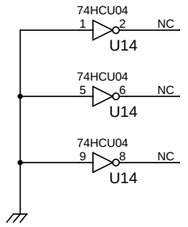
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	REDRAWN	RWH 3/18/96	CW 4/2/96
		JM'A 4/1/96	BAC 4/2/96
2	UPDATED ADDRESS	MTC 10/14/97	CW 10/16/97
		JJF 10/8/97	BAC 10/16/97
3	CHANGED PER DCR 000414-00	RWH 4/17/00	CW 5/19/00
		ECM 4/18/00	ECM 5/22/00





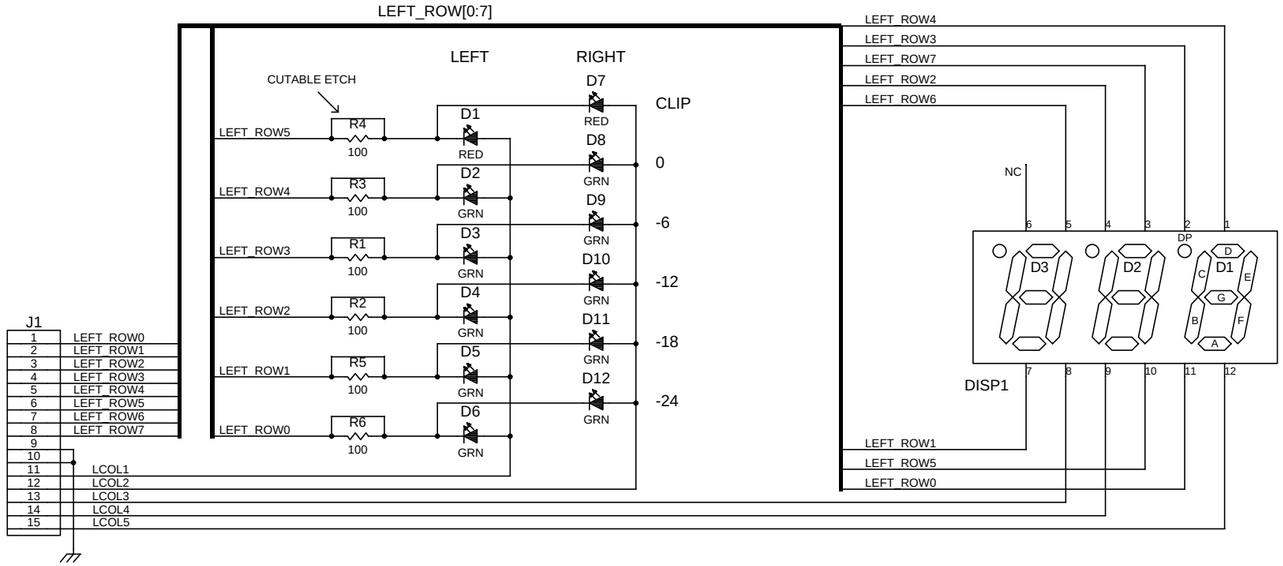


SPARES



CONTRACT NO.	Lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE: SCHEM, MAIN BD, MPX 1 BYPASS,SPARES	
DRAWN BAC	1/15/96	SIZE B / CODE / NUMBER 060-11018 / REV 3	
CHECKED JM'A	1/26/96		
Q.C. CW	4/2/96	FILE NAME 11018-8.13	SHEET 13 OF 13
ISSUED BAC	4/2/96		

5-22-2000_10:50



7-SEGMENT DISPLAY PIN CONNECTION

PIN	FUNCTION
1	CATHODE E
2	CATHODE D
3	CATHODE DP
4	CATHODE C
5	CATHODE G
6	NO CONNECTION
7	CATHODE B
8	D3 COMMON ANODE
9	D2 COMMON ANODE
10	CATHODE F
11	CATHODE A
12	D1 COMMON ANODE

REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHG. PROD. NAME PER DCR 960328-00	RWH 3/29/96	CW 3/29/96
		CW 3/29/96	BAC 4/1/96
2	ADD 7-SEGMENT DISPLAY PIN CONNECTIONS PER DCR 960628-00	CW 7/26/96	RWH 7/26/96
		JJF 7/26/96	BAC 7/26/96

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/4W
2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%
3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND
5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]
6 LAST REFERENCE DESIGNATORS USED: D12, DISP1, J2, R8

DOCUMENT CONTROL BLOCK: #060-11027

SHEET NUMBER	REVISION NUMBER
1 OF 2	2
2 OF 2	1

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

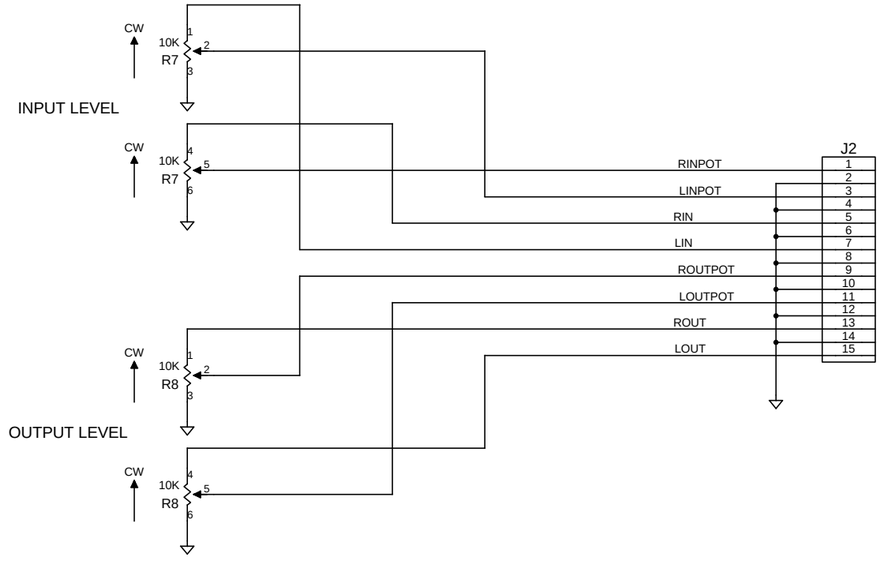
APPROVALS		DATE
DRAWN	CW/BAC	9/22/95
CHECKED	JM'A	10/10/95
Q.C.	CW	10/11/95
ISSUED	BAC	10/6/95

TITLE: SCHEM,FP BDS, MPX 1
HDRM / DSPLY

SIZE	CODE	NUMBER	REV
B		060-11027	2

FILE NAME: 11027-2.1
SHEET 1 OF 2

7-26-1996_14:47



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHG. PROD. NAME PER DCR 960328-00	RWH 3/29/96	CW 3/29/96
		CW 3/29/96	BAC 4/1/96

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

APPROVALS		DATE
DRAWN	CW/BAC	10/4/95
CHECKED	JM'A	10/10/95
Q.C.	CW	10/11/95
ISSUED	BAC	10/6/95

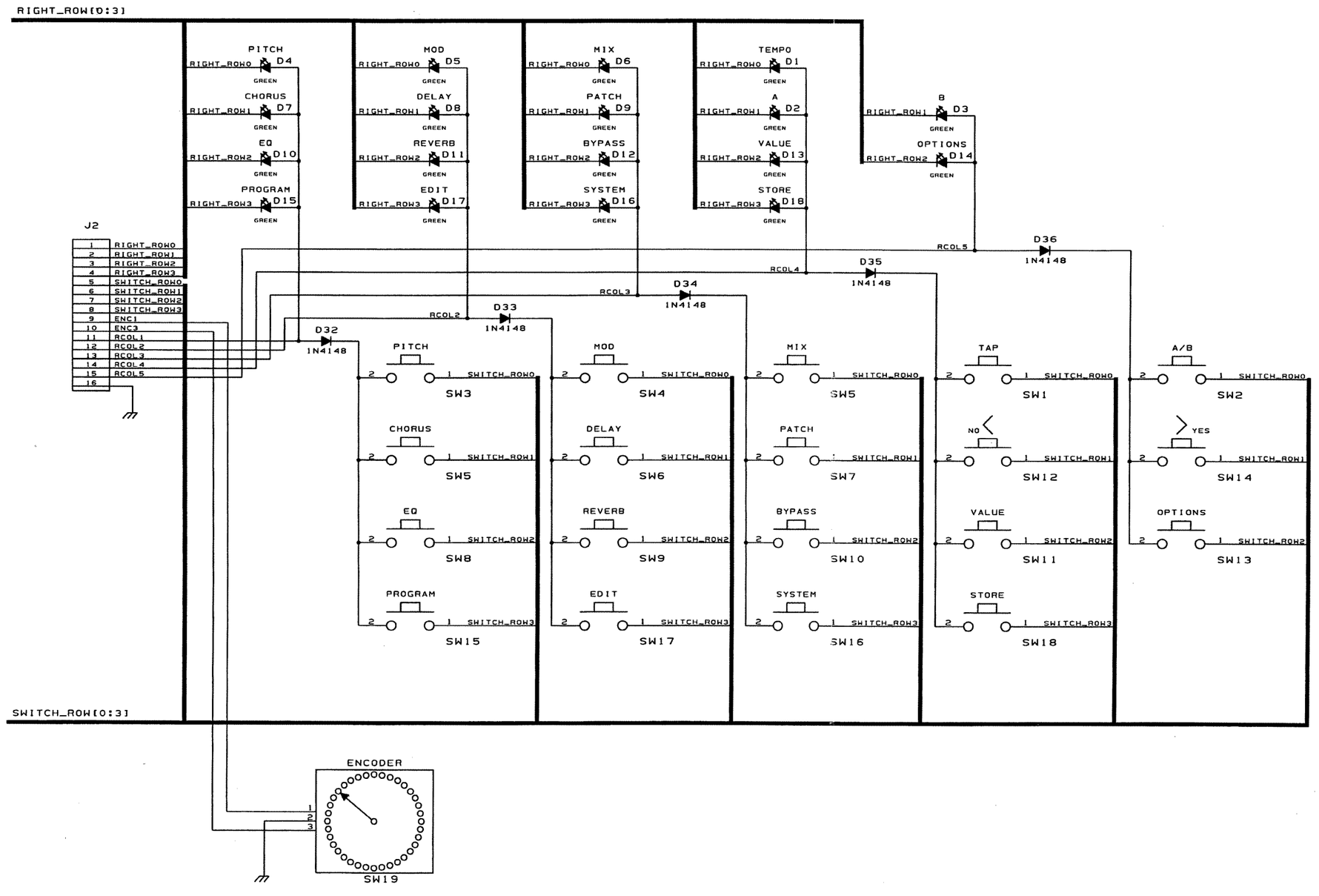
TITLE
SCHEM,FP BDS, MXP 1
LEVEL POTS

SIZE	CODE	NUMBER	REV
B		060-11027	1

FILE NAME 11027-2.2

SHEET 2 OF 2

7-26-1996_12:53



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGE DESCRIPTION, UPDATE PER DCR 960329-01	BAC 3/29/96 CW 3/29/96	CW 3/29/96 BAC 4/1/96

NOTES:

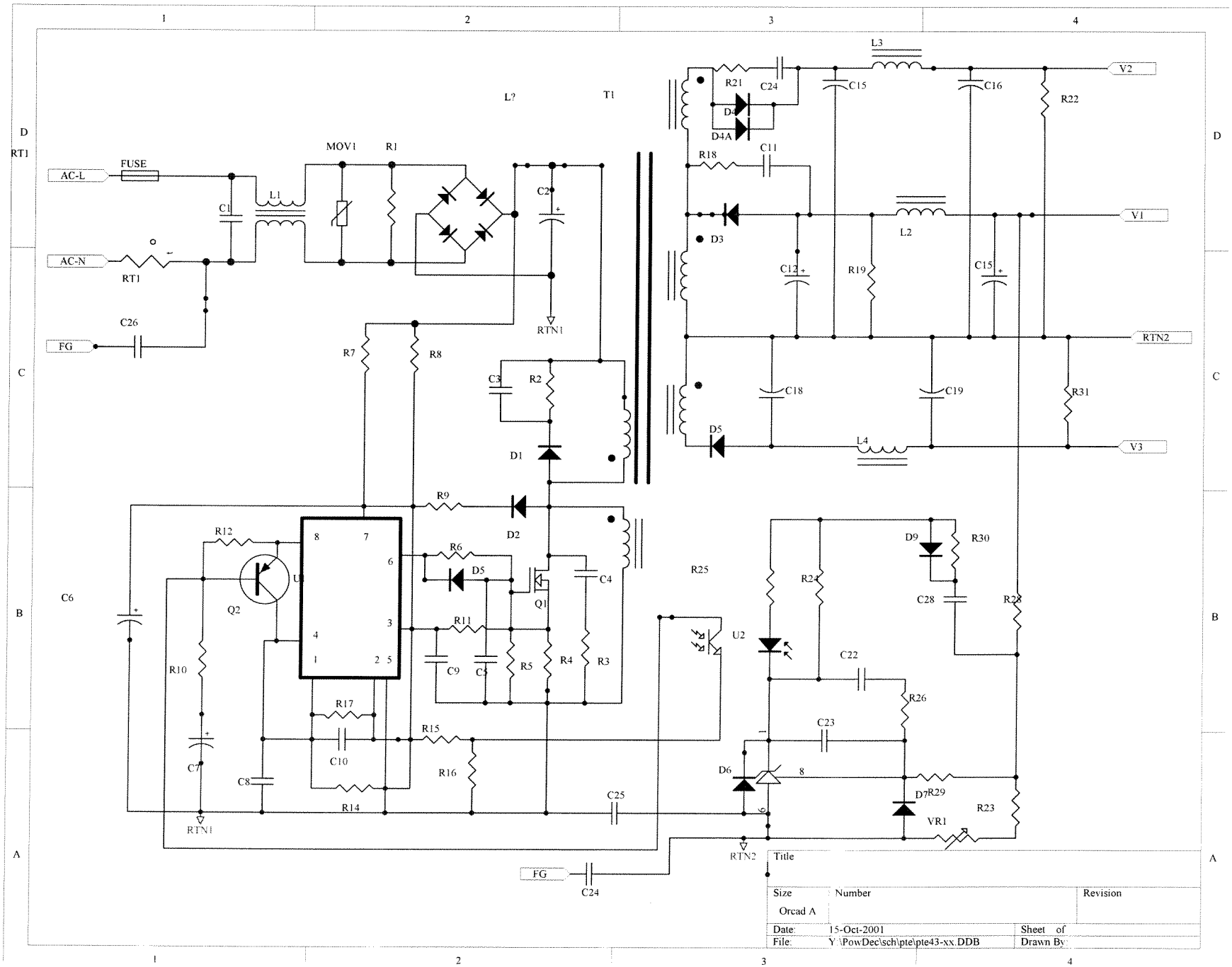
1 DIGITAL GROUND

2 LAST REFERENCE DESIGNATORS USED: D36, J2, SW19

JUN 20 2003

CONTRACT NO.	Lexicon 100 BEAVER STREET, WALTHAM, MA 02154				
APPROVALS	DATE	TITLE SCHEM, SWITCH ASSY, MPX 1			
DRAWN BAC	2/28/96				
CHECKED CW	3/29/96	SIZE B	CODE	NUMBER 060-11031	REV 1
Q.C. CW	3/29/96				
ISSUED BAC	4/1/96	FILE NAME 11031-1.1		SHEET 1 OF 1	

5-1-1996_18:07


L?
T1
L3
V2
R21
C24
C15
C16
R22
D4
D4A
R18
C11
V1
L2
D3
C12
R19
C15
RTN2
C18
C19
R31
D5
L4
V3
MOV1
R1
FUSE
AC-L
AC-N
RT1
C1
L1
C2
RTN1
C26
FG
R7
R8
C3
R2
D1
R9
D2
R12
U1
R6
D5
Q1
C4
R25
C6
Q2
R11
U2
C9
C5
R5
R4
R3
R10
R17
R15
C10
R16
C7
C8
R14
C25
RTN1
D9
R30
R24
C28
R27
C22
R26
C23
D6
D7
R29
R23
VR1
RTN2
FG
C24
Title
Size
Orcad A
Number
Revision
Date:
15-Oct-2001
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File:
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Drawn By:

	PowDec Technologies Inc.								
	PTE43-34 Part list								
Parts No	Descriptions	Parts Name	Q'ty	VendorA		VendorB		VendorC	
04.00431.020	IC KSE431AZ TAPING	U3	1	KSE	KSE431	TI	TL431		
04.03842.030	IC PWM KA3842B/UC3842AN	U1	1	FAIRCHILD	KA3842B	MOTOROLA	UC3842B		
05.PC123.010	PC123C/PS2561/SFH615A3 C:1-300	U2	1	INFENEON	SFH615A	NEC	KS2651	SHARP	PC817/PC113
06.04148.040	DIODE SW 1N4148	D6,7,8,9	4	HITACHI	1N4148	T.F.	1N4148		
06.10020.010	DIO. YG902C2R,BYQ28X-200	D3	1	FUJI	YG902C2R	PHILIP	BYQ28X-200		
06.1R020.010	U-FAST 1A 200V UF1003,HER103	D5	1	LITEON	UF1003	GS	UF1003		
06.1R020.040	DIODE 1A 600V 1N4937	D2	1	LITEON	1N4937				
06.1R0A0.020	DIO ULTRA FAST 1A 1KV BYV26E	D1	1	PHILIP	BYV26E	GS	BYV26E		
06.2N390.600	TR.PNP 200mA/40V 2N3906 T092	Q2,Q3	2	MOTOROLA	2N3906	NS	2N3906		
06.2R060.150	.IODE BRIDGE 2A 600V KBP206G	BD1	1	LITEON	KBP206G	GS	KBP206G		
06.3R020H011	DIO. FAST 3A 200V UF3003 E □	D4,D4A	2	LITEON	UF3003	GS	UF3003		
06.FS10T.010	MOS 10A 600V FS10KM-12/2SK2761	Q1	1	FUJI	2SK2761	TOSHIBA	2SK2843		
08.47216.263	Y1CAP TDK/MURA 472PF M 250V KX	C25 (RTN1-RTN2)	1	TDK	CD	SAMSUNG	AD	MATSUSHITA	AH

08.1031A.13C	C.CER 0.01UF M 1KV F-TYPE LL	C3	1	HOSONIC	C.CER				
08.2211A.13C	C.CER 220pF M 1KV Y5P 5mm SL	C4	1	HOSONIC	C.CER				
08.2211A.13C	C.CER 220pF M 1KV Y5P 5mm SL	C4	1	HOSONIC	C.CER				
08.10216.263	Y1CAP TDK/MURA 102PF M 250V KO	C26	1	TDK	CS	MURATA	KX	MATSUSHITA	NS-A
08.2221A.13C	C.CER 2200P M 1KV Y5P SL	C11,C14,C24	3	HOSONIC	Y5P				
09.10414.083	C.C M0N0 0.1uF 50V X7R +/-20%	C23,C28	2	HOSONIC	X7R				
09.10614R083	CE 10UF 50V SH/ 50MHA10 5*11	C7	1	CHEMICON	KME	RUBYCON	MHA		
09.10712R083	CE 100U 25V YXF 105C	C6,C19	2	CHEMICON	KMF	RUBYCON	YXF		
09.10717.T83	C.E 100uF 400V 85 C 25*25 LXK	C2	1	TEAPO	LXK	CHEMICON	KMG		
09.22713'083	C.E 220UF 35V SXE 8*20 □□	C18	1	CHEMICON	SXE	RUBYCON	YXA		
09.22819T093	C.E 2200UF 16V SD 13*25	C12	1	TEAPO	SD	CHEMICON	LXJ	RUBYCON	YXA
09.47712.T83	C.E 470UF 25V SX 10*20	C13,C15,C16	3	TEAPO	SX	CHEMICON	LXJ	RUBYCON	YXA
11.00000.033	JUMPER	J2,3,4,5,6,7,8.	7						
11.00000.033	JUMPER	J9,10,VR.	3						
11.10224.033	PEI 1000P 50V +/-20%	C8,C22	2	HOSONIC	PEI				
11.10314.033	PEI 0.01uF 50V +/-20%	C5	1	HOSONIC	PEI				
11.22314.033	PEI 0.022uF 50V +/-20%	C9,C10.	2	HOSONIC	PEI				
11.471KD.083	VARISTOR 300VAC/385DC,40J,7mm	M0V	1	JOYIN	JVR7N471	SAS	471KD07	CENTRA	CNR-07D471K
11.47416.033	C.MPE X 0.47UF 250V M SL	C1	1	RIFA	PHE	TEAPO	XG	UTX	HQX

13.10031.012	R.CF 10 1/8W +/-5% TAPING	R8	1	SAC	R.CF	BI IH	R.CF		
13.10033.012	R.CF 10- 1/2W +/-5% TAPING	R18,R21	2	SAC	R.CF	BI IH	R.CF		
13.10231.012	R.CF 1K 1/8W +/-5% TAPING	R10,R16.	2	SAC	R.CF	BI IH	R.CF		
13.10331.012	R.CF 10K 1/8W +/-5% TAPING	R5,R29,R30	3	SAC	R.CF	BI IH	R.CF		
13.10435.032	R.MOF 100K 2W "F" □	R2.	1	SAC	R.CF	BI IH	R.CF		
13.10436.034	R.MOF 100K3WS MINI SIZE FKK □	R7	1	SAC	R.MOF	BI IH	R.MOF		
13.20331.012	R.CF 20K 1/8W +/-5% TAPING	R26	1	SAC	R.CF	BI IH	R.CF		
13.22035.032	R.MOF 22- 2W "F"□	R3	1	SAC	R.MOF	BI IH	R.MOF		
13.22131.012	R.CF 220- 1/8W +/-5% TAPING	R24,R25	2	SAC	R.CF	BI IH	R.CF		
13.27231.012	R.CF 2.7K 1/8W +/-5% TAPING	R15	1	SAC	R.CF	BI IH	R.CF		
13.30031.012	R.CF 30 1/8W +/-5% TAPING	R6	1	SAC	R.CF	BI IH	R.CF		
13.30435.032	R.MOF 0.3 2W "F" FORM	R4	1	SAC	R.MOF	BI IH	R.MOF		
13.47135.032	R.MOF 470- 2W "F" FORM	R22,R31	2	SAC	R.MOF	BI IH	R.MOF		
13.51035.032	R.MOF 51- 2W "F" FORM	R19	1	SAC	R.MOF	BI IH	R.MOF		
13.51231.012	R.CF 5.1K 1/8W +/-5% TAPING	R17	1	SAC	R.CF	BI IH	R.CF		
13.51331.012	R.CF 51K 1/8W +/-5% TAPING	R12	1	SAC	R.CF	BI IH	R.CF		
13.56231.012	R.CF 5.6K 1/8W +/-5% TAPING	R14	1	SAC	R.CF	BI IH	R.CF		
13.56432.012	R.CF 560K 1/4W +/-5% TAPING	R1	1	SAC	R.CF	BI IH	R.CF		
13.82131.012	R.CF 820- 1/8W +/-5% TAPING	R11,R13	2	SAC	R.CF	BI IH	R.CF		
13.82432.012	R.CF 820K 1/4W +/-5% TAPING	R9	1	SAC	R.CF	BI IH	R.CF		
14.10025.012	R.MF 10K 1/8W +/-1% TAPING	R23	1	SAC	R.MF	BI IH	R.MF		
14.10225.012	R.MF 10.2K 1/8W +/-1% TAPING	R28	1	SAC	R.MF	BI IH	R.MF		

17.65R4A.5R0	NTC THERMISTER N10SP005M-Y1C	RT1	1	UPPERMOST	N10SP005M-Y1C				
19.28043.030	X'FORM ERL-28H PTE43-23/34	T1	1	CHU YANG	ERL-28H				
19.40008.002	CHK 4uH(R6*20)0.9*12.5T+UL TUB	L2,L3	2	CHU YANG	R6*20	JION	R6*20		
19.415.7.401	IND. COM. UU15.7*4SEC 17mH	L1	1	CHU YANG	UU15.7*4SEC	JION	UU15.7*4SEC		
19.4R6*8.001	CHOKE 10uH DR6*8 0.4*18.5T	L4	1	CHU YANG	DR6*8	JION	DR6*8		
20.60009.100	CONNECTOR 3.96mm 3PIN-1	CN1 REVERSED INSERTED	1	C S	3.96mm 3PIN-1				
20.60010.101	CONNECTOR 3.96mm 6PIN	CN2	1	C S	3.96mm 6PIN				
26.12001.802	FUSE 4A 250V 5ST4/218004	FUSE	1	LITTLE FUSE	2E+05				
34.00004.001	FUSE CLIP 5*20mm FH1206	FUSE CLIP	2	LITTLE FUSE	FH1206	BEL	5ST4	TRIAD	50T
34.03*05.011	HEATSINK H=25mm ALUM. HS910	HS1.HS2	2	WEI DING	HEATSINK				
34.PTE01.002	P.C.B.TERMINAL PC817(0.8)	GND	1	KANG YANG	TERMINAL				
42.00005.006	SHRINK TUBE 1*15 m/m (D*L)	FOR D4,D4A	4	LCELC	SHRINK TUBE				
42.T0220.002	TO-220 WASHER TW4 TR PAD	D3	1	LCELC	TO-220				

					WASHER				
42.T0220.003	TO-220 SILICONE INSULATED PAD	D3	1	LCELC	INSULATED PAD				
44.WP05X.007	CARTON , 200*130mm	PACK	1	LOCAL	CARTON				
48.03*05.012	PCB CEM1 2OZ 82*127mm CME07038	PCB	1	SKYCHIA	CEM1 2OZ				
86.00030.000	SCREW TMS 3*6B ROUND	FOR HS1,HS2	2	KOLING	TMS 3*6B				
86.00040.240	SCREW PMS 3*8N	FOR Q1,D3	2	KOLING	PMS 3*8N				
***** End *****									