Section 6
Technical Data

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Specifications

Performance

Performance meets or exceeds all specifications for the BTSC system, as defined by FCC *OET-60A* and EIA *Multichannel Television Sound: BTSC System Recommended Practices.* All measurements made with signal applied directly to 8185A audio inputs; dbx N/R IN unless otherwise noted.

Frequency response: ±0.5dB, 30–14,000Hz; <1dB down at 15kHz.

Noise: <–82dB, referenced to 100% modulation.

Total system distortion — BTSC mode (N/R in): <0.1% THD, 50–10,000Hz; <0.2% THD, 10–15kHz. <0.2% SMPTE IMD; 0.08% typical.

System BTSC separation — tone (10% 75μs equivalent-input modulation N/R in): >35dB, 50–10,000Hz; >30dB, 10–14kHz; >40dB, 50–10,000Hz typical.

BTSC separation of monitor decoder alone — tone (10% 75μs equivalent-input modulation, N/R in): >40dB, 50–10,000Hz; >35dB, 10-14kHz.

System group delay — 75μs equivalent mode: Constant ±5%, 50–12,000Hz.

Installation

Location

Immediately below 8182A OPTIMOD-TV Audio Processor, if used.

External Audio Input

For audio processors other than Orban 8182A OPTIMOD-TV.

Configuration: Left and right, flat or pre-emphasized.

Impedance: >10KΩ load impedance, electronically balanced by means of true instrumentation amplifier. Requires balanced source ≤600Ω. Common mode rejection >60dB at 60Hz.

Sensitivity: +10dBm at 100Hz applied in-phase to both inputs produces ±25kHz main channel deviation (100% modulation).

Connector: Barrier strip (#5 screw), EMI suppressed.

Interconnect to 8182A OPTIMOD-TV Audio Processor

Signals: Left and right 8182A compressor output to 8185A six-pole filter input; 8185A left and right six-pole filter output to 8182A HF limiter input; 8182A left and right pre-emphasized output to 8185A input.

Connector: 14 pin connector to mate with shielded jumper cable supplied with 8185A.

Sync Reference Input

Impedance: 20KΩ, balanced. Switchable 75Ω termination.

Level: Composite video or sync, 0.6 to 1.6Vp-p; 1V nominal.

Connector: Two BNC connectors, looped-thru, shell insulated from chassis.

SAP Subcarrier Input

Impedance: 10KΩ, unbalanced.

Sensitivity: 1.5Vp (3.0Vp-p) produced ±15kHz carrier deviation (100% modulation).

Connector: BNC; shell floating over chassis ground, capacitively coupled to chassis through approximately 500pF for EMI suppression.

Composite Output

Impedance: Voltage source (0Ω) or 75Ω source impedance (selectable with internal jumper), single-ended, impedance independent of OUTPUT LEVEL setting.

Level: Adjustable from 0 to 2.2Vp (4.4Vp-p) at 73kHz total deviation. 18-turn TOTAL BASEBAND OUTPUT LEVEL control.

Load: When jumpered for voltage source, will drive *two* 75Ω loads in parallel. Maximum permissible load capacitance 0.047uF.

Connector: BNC, floating over chassis ground. EMI suppressed.

Monitor Output

Configuration: Left and right, N/R decoded (or 75μs de-emphasized, depending on setting of internal MONITOR N/R IN/OUT switch).

Impedance: 600Ω source impedance, single ended.

Level: Fixed; 5V peak into open circuit corresponds to 100% modulation.

Connector: Barrier strip (#5 screw), EMI suppressed.

Remote Control

Function: Selects MONO LEFT/MONO RIGHT/STEREO, Pro Channel ON/OFF.

Voltage: 6 to 24V AC or DC, momentary or continuous, optically isolated. 22VDC supplied to facilitate use with contact closure.

Connector: Barrier strip (#5 screw).

Sync Lock Indicator

Configuration: Relay-controlled contact closure to indicate successful lock to sync or composite video. Limit applied voltage to 50V, total load to 10VA non-reactive, current to 0.5A.

Connector: Barrier strip (#5 screw).

Power

115/230VAC (switch-selectable), ±15%, 50–60Hz; 35VA. IEC mains connector with detachable 3-wire power cord supplied. Leakage to chassis <0.5mA. AC is EMI suppressed.

Ground: Circuit ground is independent of chassis ground; both appear on terminal strip on rear panel for strapping as required.

Weight

24 lbs (10.4kg) net; 34 lbs (15.4kg) shipping.

Environmental

Operating temperature range 0–50°C (32–122°F). Humidity 0–95% RH, non-condensing.

Circuitry

Filters

Filtering exceeds BTSC specifications, as stated in Section 2.4.1.1. and Section 2.4.1.2 of the EIA *Multichannel Television Sound: BTSC System Recommended Practices.*

Left and Right Low-pass Filters

Type: Six-pole filters with two high-Q notches.

Rejection: >–50dB at 15,734Hz.

Sum and Difference Low-pass Filters

Type: Eleven-pole elliptical filter.

Passband response: Typically +0.05, −0.1dB to 15,000Hz.

Stopband rejection: >60dB at 15,734Hz and above.

Stereo Baseband Encoder

Equivalent stereo separation: >55dB, 50–15,000Hz.

Crosstalk — Linear: <−70dB, 50–15,000Hz, main channel to subchannel, or subchannel to main channel, referenced to ±55kHz deviation.

Suppression of other spurious components: <−75dB, referenced to ±55kHz deviation.

Warranty

One year, parts and labor. Subject to limitations stated in our Standard Warranty.

All specifications subject to change without notice.

Circuit Description

On the following pages, a detailed description of each circuit's function is accompanied by a component-by-component description of that circuit. Keywords are highlighted throughout the circuit descriptions to help you quickly locate the information you need.

Each card is numbered. There is no Card #1. The Card #9 and Card #10 slots are reserved for the optional Pro Channel Cards described in a manual supplement supplied with those Cards. The number of the card containing the described circuitry is provided with its description.

Where circuitry is duplicated between the left and right, or between the L+R and L–R channels, we will only describe the L or L+R circuitry.

REFER ALSO TO THE MORE DETAILED BLOCK DIAGRAM (page 6-57).

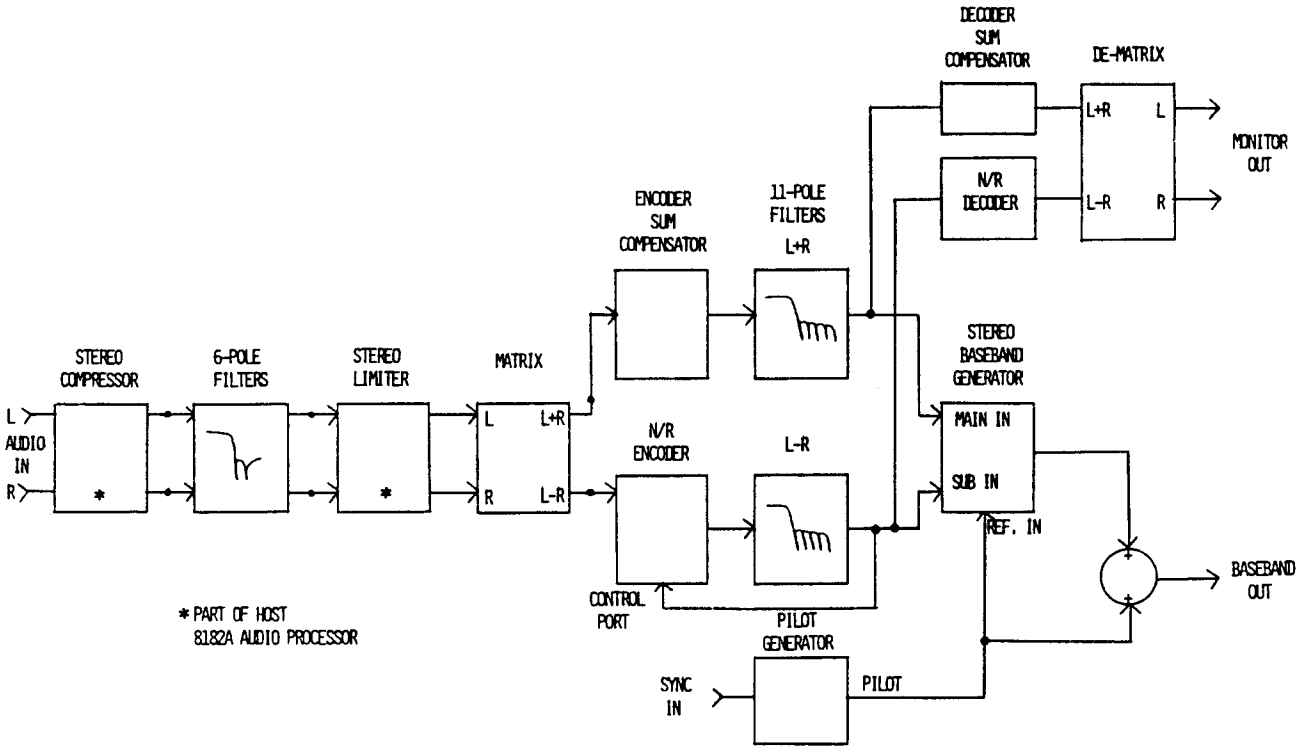


Fig. 6-1: Simplified Stereo Generator Block Diagram

1. Differential Input Amplifiers

Located on Card #2

The left and right input signals are applied to differential input amplifiers, which act like "active transformers": they respond with unity gain to the difference between the signals present at their + and − inputs, but reject signals that appear identically on these inputs, thus rejecting common-mode noise and hum.

Component-level description:

The differential amplifier is realized with the classic 3-amplifier "instrumentation amplifier" topology, configured for unity gain. R1, R2 provide bias current for buffers IC1a, IC1b. IC1a, IC1b drive differential amplifier IC2a, which provides high common-mode rejection because R3a-d are matched ±0.1%.

2. Pre-Emphasis Networks

Located on Card #2

IC3a provides 75μs pre-emphasis for external audio processors that can only provide a "flat" output. Pre-emphasis can be defeated with the pre-emphasis out/in jumper.

Component-level description:

IC3a and associated components create pre-emphasis by reducing the amount of feedback at high frequencies with C3. C4 causes a supersonic rolloff to prevent the pre-emphasis from increasing indefinitely with frequency.

The circuit is inverting. Its normal gain at 50Hz is −2.92dB. It is up 3dB (i.e., its gain is +0.09dB) at 2.12kHz.

3. Group Delay Correctors

Located on Card #2

The group-delay correctors are one or more cascaded allpass filters. The frequency response of these filters is very flat, but their phase response changes with frequency. The phase response is chosen to add frequency-dependent group delay to the signal such that the overall group delay of the allpass filter and the low-pass filter being equalized is more constant with frequency.

There are two group delay correctors. The first consists of one second-order allpass filter to equalize the six-pole filters on Card #3. The second consists of three cascaded second-order allpass filter to equalize the 11-pole filters on Card #5.

Component-level description:

IC2b and associated components are a second-order all-pass filter that equalizes the group delay of the six-pole filter on Card #6. The interaction of the components is complicated and best explained mathematically.

The frequency response of the filter is normally very flat (better than ±0.1dB, 50-15,000Hz). Faulty opamps may be replaced freely. If the filter becomes unflat due to a fault, first check the matching of R3f,g, since the flatness is very sensitive to this matching. Other faults due to component drift or failure are difficult to repair in the field, and should be repaired at the Orban factory. (See **Section 5, page 5-13** in this manual for details on how to obtain factory service.)

IC3b, IC4a, IC4b and associated components are a sixth-order all-pass filter that equalizes the group delay of the 11th-order low-pass filter on Card #5. Their topology is identical to IC2b's, and the troubleshooting comments above apply.

4. Matrix

Located on Card #2

From the L and R signals the matrix creates sum-and-difference signals for use by subsequent circuitry.

Component-level description:

The matrix is inverting. IC9a creates a very accurate −(L+R) signal by summing L and R with a high-precision (±0.1%) resistor array in an inverting amplifier. Similarly, IC9b creates a very accurate −(L−R) signal by subtracting L from R.

5. Six-Pole Filter

Located on Card #3

If the Orban Model 8182A Optimod-TV Audio Processor is used, the Six-Pole Filter and its associated stereo/mono switching and phase-matching functions are inserted between the output of the 8182A's Dual-Band Compressor and the input of its High-Frequency limiter.

If external processing is used, the Six-Pole Filter and its associated circuitry are inserted immediately after the differential input amplifiers in the 8185A.

The Six-Pole Filter's bandwidth is 15.0kHz. Its ideal frequency response in the passband and stopband is shown in Fig. 6-2. Note that the small (0.4dB) passband ripples are specifically designed to complement similar small ripples in the response of the 8182A OPTIMOD-TV Audio Processor to achieve flatter overall system response.

Because all parts of the filter interact, failures which cannot be cured merely by replacing opamps are best left to factory service, since special tight-tolerance tight-temperature-coefficient parts are used in certain places. (The circuitry has been designed to be insensitive to normal unit-to-unit variations in opamps.)

Instructions on field alignment of the filters is provided in **Section 4: Maintenance** of this manual.

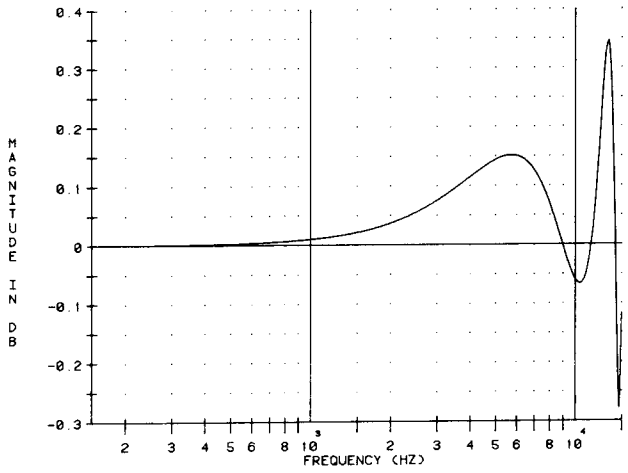
Component-level description:

The Six-Pole Filter is an active-RC analog of a passive LC ladder filter. It is realized by means of resistors, capacitors, and Frequency-Dependent Negative Resistors (FDNR's). An FDNR is realized by a dual opamp, three resistors, and two capacitors. When the passive LC filter is transformed into an active RC filter, inductors become resistors, resistors become capacitors, and capacitors become FDNR's.

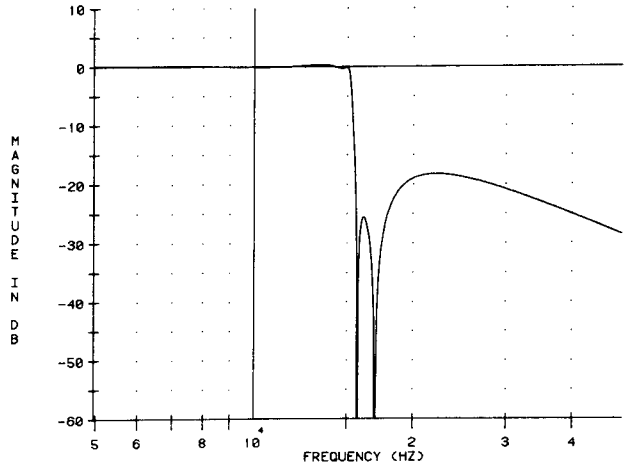
The first two FDNR's each resonate with a series resistor to create a notch in the frequency response of the filters. (This is analogous to a series L-C circuit to ground.) The third FDNR (IC3) serves as a transformed capacitor and does not produce a notch. The notches are located in the "stopband" (beyond approximately 15.7kHz). The circuit associated with IC1 produces a notch at 17.000kHz ±4%. The circuit associated with IC2 is tuned by means of R13 to produce a notch at precisely 15.734kHz to remove any H component in the audio.

Measuring the frequency of these notches and their depth provides the best way of diagnosing problems with such filters, since problems with a given notch can be associated with a given FDNR in most cases.

To avoid possible clipping, the signal is attenuated by 20dB by means of voltage divider R1, R2 before being applied to the filter. This gain is made up by IC5b to restore unity gain at low frequencies.



Response of Six-Pole Filter in Passband



Response of Six-Pole Filter in Passband and Stopband

Fig. 6-2: Response of Six-Pole Filter

6. Stereo/Mono Switching

Located on Card #3

A pair of JFET switches following the Six-Pole Filters accept the Left and Right signals. The gates of these JFET's are driven by logic signals generated on Card #7. In STEREO mode, the output of each filter is passed to the respective Left and Right output of the card. In MONO LEFT mode, the output of the Left Six-Pole Filter drives both the Left and Right outputs of the card. The MONO RIGHT mode is analogous.

Component-level description:

JFET switch Q6 determines whether unity-gain follower IC5a will receive its input from the output of the Left or Right Six-Pole Filter. If Q6 is ON (gate pulled to the same voltage as its source through R45 because Q2 is OFF), then the left channel contribution from R20 will be swamped out by the low impedance drive from IC10b and the output of IC5a will contain the right channel. Conversely, if Q6 is OFF (gate at −15VDC because Q2 is ON), it looks like a very high impedance and the left channel will be applied to IC5a through R20.

Logic signals are supplied from Card #7. Refer to Fig. 6-4 on page 6-21 for a logic truth table.

7. Phase-Balance Circuit

Located on Card #3

The two signal paths of the 8182A Audio Processor are complex and contain large frequency-dependent phase shifts. Although the 8182A is manufactured with high-precision parts, it is possible that differences between the phase shifts of the Left and Right channels could cause as much as 1dB frequency response error in the mono sum due to phase cancellation. Other external audio processors could be similarly sensitive. For this reason, a Phase-Balance circuit is provided in the Stereo Generator chassis. This circuit introduces a variable phase shift in the Left Channel path which can be adjusted to be less than, identical to, or more than a fixed phase shift which is introduced in the Right Channel. Thus relative phase shift can either be added to or subtracted from the Left Channel as necessary to make the overall difference between the phase responses of the two channels in the system as small as possible.

Component Level Description:

IC4b and associated components form a first-order all-pass network: its magnitude response is flat, but its phase shift changes from 0°to 180°as a function of frequency. With R24 centered, it is normally 90°at 100kHz, and is equal to the phase shift produced by IC9b and associated components in the L−R channel. Adjustment of R24 changes the frequency at which 90°of phase shift is produced, without changing the (flat) magnitude response.

8. Eleven-Pole Filters

Located on Card #5

The Eleven-Pole Filters provide essentially flat frequency response to 15kHz (typically ±0.1dB), and rejection exceeding 60dB above 15.734kHz. Ideal response is shown in Fig. 6-3 below .

The comments on page 6-7 regarding field repair of the Six-Pole Filter also apply to the Eleven-Pole Filters. The circuitry is designed to be insensitive to normal unit-to-unit variations in opamps. But if the filters cannot be repaired simply by replacing opamps, then they should be repaired by Orban Factory Service. Instructions for field alignment of the filters is provided in Part 4 of this manual. The Eleven-Pole Filters are realized using FDNR technology. The reader should refer to page 6-7 for a discussion.

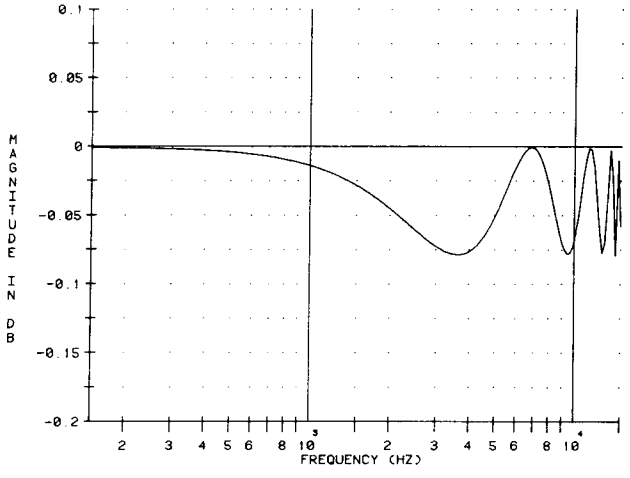
Unlike the Six-Pole Filters, all FDNR's in the eleven-pole filters create notches. There are five notches in the stopband. Trimmers are provided to tune the two notches closest to the passband to their correct frequencies, achieving highest filter accuracy. The notch frequencies are as follows:

IC5	34.60kHz
IC1	17.27kHz
IC2	15.77kHz
IC6	16.14kHz
IC11	20.74kHz

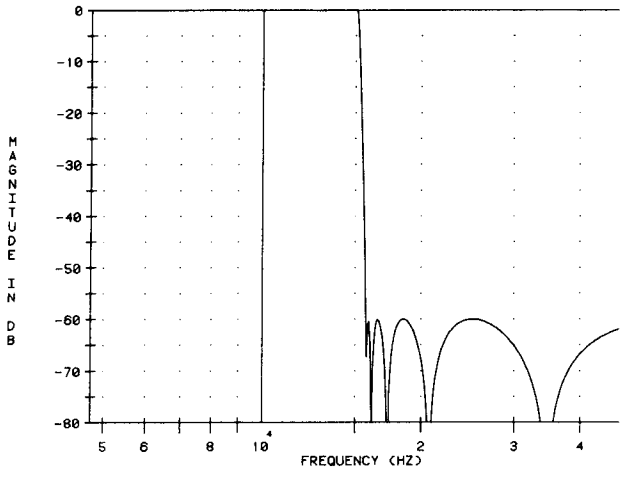
Component-level description:

R1 and R2 introduce about 20dB attenuation to avoid clipping within the filter. This gain is made up in IC10B.

Please note the comments regarding troubleshooting and factory service of the filters in **5. Six-Pole Filter on page 6-7** above.



Response of Eleven-Pole Filter in Passband



Response of Eleven-Pole Filter in Passband and Stopband

Fig. 6-3: Response of Eleven-Pole Filter

9. Sum Compensator

Located on Card #5

The Sum Compensator is a low-pass filter whose amplitude and phase response matches the excess amplitude and phase of the dbx N/R Encoder. (The "excess" amplitude and phase is the difference between the amplitude and phase specified in the "ideal companding tables" of OET-60a and the actual amplitude and phase produced by the real-world dbx circuit.) The Sum Compensator is switched into the Sum circuit path whenever the dbx N/R Encoder is switched into the Difference-Channel circuit path.

In the 8185A, Cards #4, #5, and #6 are a matched set. Please be aware of this, and work closely with Orban customer service if you wish to order backup cards or to return either Card #4, #5 or Card #6 to the factory for service.

Component-level description:

The sum compensator consists of IC9 and associated circuitry. Depending on the vintage of dbx N/R Encoder employed, either IC9B alone, or both parts of IC9 are used to realize the Sum Compensator. Each opamp can realize a wide variety of different filters depending on how the card is stuffed with components. The particular circuit to be used is chosen on factory test to best match the given dbx encoder card (on Card #4). Therefore, a given Card #4 (containing the dbx N/R Encoder) must be matched by a complementary Card #5 with the correct Sum Compensator. If spare cards or service of either Card #4 or Card #5 is required, please consult Orban Customer Service.

10. Stereo/Mono Filter Bypass

Located on Card #5

Whenever the system is in MONO mode (either MONO LEFT or MONO RIGHT), the Sum-Channel Eleven-Pole Filter and the Sum Compensator are both bypassed by a JFET switch driven from logic circuitry on Card #7. This prevents the Eleven-Pole Filter from introducing unnecessary overshoots and ringing in MONO mode.

Component-level description:

In MONO mode, the L+R Eleven-Pole Filter and N/R Encoder Sum Compensator should be bypassed. Q2, a JFET switch, does this. When Q2 is ON (gate pulled up to the voltage at its source through R35 by virtue of Q1's being OFF), then the contribution from R36 at IC10A's "+" input is swamped out, and the output of IC10A is substantially identical to the Eleven-Pole Filter's input signal (which appears at pin H of the card edge connector).

When Q2 is OFF (gate pulled to -15VDC by virtue of Q1's being ON), Q2 is a very high impedance, and the filter output appears at IC10A's "+" input through R36.

The logic signal to drive Q1 is generated on Card #7 (Stereo Baseband Generator).

11. Noise Reduction Encoder

Located on Card #4

Card #4 is devoted almost entirely to the dbx-manufactured N/R Encoder card. This card is described in the **Appendix** on page 6-26.

The N/R Encoder is fed by a precision 75μs de-emphasis network. This cancels the pre-emphasis produced by the 8182A audio processor (or by the pre-emphasis networks on Card #2 if other audio processing is used) so that a "flat" signal is applied to the N/R Encoder's input port. The N/R Encoder's input-referenced overload level closely follows the 75μs de-emphasis curve as a function of frequency, and the audio processor must provide high-frequency limiting to compensate for the 75μs curve.

When the N/R ENCODER IN/OUT switch on Card #5 is switched OUT, all circuitry on Card #4 (including the 75μs de-emphasis network) is bypassed, and pre-emphasized audio is applied to the Difference-Channel Eleven-Pole Filter.

The N/R circuitry can itself produce substantial noise, some of which will extend beyond 15kHz. For this reason, when the N/R ENCODER IN/OUT switch is IN, the very sharp Difference-Channel Eleven-Pole Filter (on Card #5) is inserted between the output of the N/R Encoder and the input of its sidechain. The output of the N/R Encoder is taken after the Eleven-Pole Filter to prevent N/R Encoder-induced noise from aliasing from the stereo Subchannel into the Main Channel, and to ensure that the sidechain of the N/R Decoder in the receiver sees the same signal as the sidechain of the N/R Encoder. (Any N/R Encoder-induced noise in the stereo Subchannel is essentially eliminated by the complementary action of the N/R Decoder in the receiver.)

The dbx card is not field-repairable or field-alignable due to the extremely tight tolerances involved in its manufacture and adjustment. In case of failure of the card, it should be returned to Orban Customer Service for repair or exchange. Please note that it is matched to its Sum Compensator circuit (on Card #5), and that Cards #4 and #5 must therefore be treated as a set. See **Sum Compensator** on page 6-11.

Component-level description:

Because the noise reduction cannot be repaired or aligned in the field, it should be treated as a component. No further component-level description is appropriate.

12. Sync Card–General Principles

Located on Card #8

The Sync circuitry extracts the horizontal line frequency from incoming composite video or sync signals, and outputs two signals. The first is a square wave at 16H which is used to drive the Stereo Baseband Generator; the second is a pulse waveform at 1H which is used to drive the Professional Channel Generator.

The sync is extracted in a Sync Separator circuit. The output of the Sync Separator serves as a reference for a Phase-Locked-Loop whose output is 16H. This output is divided by 16 to drive the Professional Channel Generator, and divided by 32 to drive the Bessel Null tone calibrator.

13. Sync Separator

Located on Card #8

The sync or composite video is tapped-off and amplified by a balanced differential amplifier with a high-impedance input and a gain of 4. The output of this amplifier drives a comparator and a negative peak detector. The negative peak detector detects the DC level of the sync tips. The output of the peak detector is offset by a positive voltage. This output (as offset) is applied to the comparator and provides a reference voltage which tracks changes in average DC level of the video.

The comparator output is a pulse train timed identically to the sync pulses in the incoming sync or composite video. The comparator output is applied to a non-retriggerable one-shot which stretches the pulses so that equalizing pulses cannot produce double-frequency output. The output of the one-shot is applied to the Phase-Locked-Loop and is also available for use by the Professional Channel Generator.

Component-level description:

Sync or composite video is picked off the input line by IC7 and associated circuitry, which form a differential amplifier with a gain of 4 and a high-impedance balanced-bridging input.

The output of IC7 is applied to comparator IC6 through two paths. The top path applies the signal to IC6's "+" input through level-shifting and temperature-compensation diode CR1 which is biased "ON" by means of current supplied through R41. The amount of DC level-shift is temperature-sensitive and compensates for temperature effects in CR2 in the bottom path.

The bottom path is a negative peak-detector which charges C2 to the peak voltage of the negative sync tips through CR2. (The voltage on C2 in fact contains a positive DC offset because of CR2's turn-on voltage.)

The voltage across C2 is applied to the "–" input of IC6. In addition, a positive DC level-shift is added to this voltage by virtue of the voltage drop across R5 due to current injected through R7. This DC level-shift causes the comparator reference voltage (on the "–" input of IC6) to track the negative sync tips (on the "+" input of IC6) with a positive offset of approximately 300mV DC, forcing the comparator output to switch reliably on each edge of the sync waveform despite changes in the average DC level of the composite video.

The output of comparator IC6 is applied to non-retriggerable one-shot IC5, which is a CMOS version of the familiar 555 timer. IC5 is triggered by negative-going edges. The output of IC5 is a series of 15,734Hz pulses whose positive-going edges are equally-spaced.

14. Phase-Locked-Loop (PLL)

Located on Card #8

The Phase-Locked-Loop employs a commercial CMOS PLL chip consisting of a digital phase detector and a Voltage-Controlled Oscillator (VCO). The VCO operates at a frequency of 16H. This is divided down to 1H in a binary divider chip. The 1H output of the Binary Divider is used as one input to the phase detector; the other input is the 1H pulse train from the Sync Separator.

The output of the phase detector (consisting of pulses at 1H whose width is proportional to the phase difference between the inputs of the phase detector) is filtered and applied to the control-voltage input of the VCO, closing the loop.

The phase detector is equipped with an output which is HIGH (+15V) when the loop is locked, and which produces pulses which go LOW (ground) when the loop is unlocked. This output is averaged and applied to the Lock Detector comparator whose output is saturated positive when the loop is locked and which is saturated negative when the loop is unlocked. The output of this comparator drives the SYNC LOCK LED on the front panel, and also provides a logic input to force the Stereo Baseband Generator out of stereo mode when sync lock is lost.

Component-level description:

The 1H pulses from IC5 provide a phase reference for the phase detector within IC9, which is triggered on positive-going edges. The output pulses of IC9a are integrated by IC8b and associated circuitry. When the loop is closed (by returning the 1H output of IC4 to phase detector IC9a), a second-order PLL is formed. R15 and C6 provide extra filtering of the high-frequency "garbage" which passes through IC8b.

IC9b and associated components form a Voltage-Controlled Oscillator (VCO). Its output is a square wave at 16H, which can be considered the output of the PLL.

If the loop loses lock (even very momentarily), pin 1 of IC9a (which is ordinarily at +15V) will produce pulses which go to ground. Ordinarily when lock is achieved, C9 is charged to +15V through R18 and this voltage is applied to IC8a's "+" input. IC8a operates as a comparator. A +14.0V reference voltage is applied to IC8a's "–" input through voltage divider R19, R20. If the voltage on IC8a's "+" input is +15V, IC8a turns ON (saturates to the positive power supply rail), lighting the SYNC LOCK lamp on the front panel, activating the REMOTE SYNC LOCK circuit, and forcing the BSYNC line (which goes to logic on the stereo generator) to ground because of the level-shifting performed by R21 and R22.

If lock is lost for any significant fraction of one field, the voltage across C9 will drop below +14V. IC8a's output will then saturate to the negative power supply rail, turning off the SYNC LOCK lamp, deactivating the REMOTE SYNC LOCK circuit, and forcing the BSYNC line to approximately –15V.

15. Bessel Null Calibrator

Located on Card #8

The Bessel Null calibrator circuit generates a sinewave at 1/2 H (7.867kHz). It does so by dividing the 1H squarewave by 2, and then filtering the resulting 1/2 H squarewave to turn it into a very low-distortion sinewave (THD<0.025%). Most of the filtering is done by the L+R 11-pole low-pass filter (on Card #5). A servo closes an amplitude-sensing feedback loop around the filter to ensure that the output level of the calibration tone is very stable.

The tone's level is calibrated so that it produces a level at the input to the Stereo Baseband Generator of 1.3377Vrms. This is equivalent to ±18.918kHz carrier deviation, or 75.673% modulation with reference to 100% modulation=±25kHz deviation. When the tone produces this level of modulation (indicated by the RF aural carrier's nulling for the first time as the output level control is advanced from its fully counterclockwise position), then the ratio between carrier deviation and noise reduction encoder output level is set correctly. (See **page 2-18 in Section 2 – Installation** of this manual for detailed instructions on how to perform the Bessel null.)

When the BESSEL NULL CAL switch is in TONE, the following things happen: 1) the tone generator is turned on; 2) the L+R signal is disconnected from the input of the L+R 11-pole low-pass filter; 3) the output of the tone generator is connected to the input of the L+R 11-pole low-pass filter; 4) the Stereo Baseband Generator is forced into mono mode; and, 5) the 11-pole low-pass filter is forced to remain in the circuit path despite the system's being in mono mode.

Component-level description:

The 1H tone is divided by 2 in IC10b which produces a square wave. The square wave is applied to second-order low-pass filter IC11a and associated components, where it is preliminarily filtered prior to its being routed through the L+R 11-pole low-pass filter for final filtering.

The amplitude control servo works as follows. The peak output level of the L+R ll-pole low-pass filter is monitored by IC11b, acting as a comparator. If the peak level at pin 6 of IC11b exceeds the precisely-controlled reference voltage on pin 5, then the output of IC11b goes negative, and charges C19 negatively through CR9 and R45. Emitter follower Q3 follows the voltage on C19 and clamps the square wave input to IC11a to a voltage just sufficient to create the desired 1.3377Vrms level at the output of the L+R ll-pole low-pass filter.

16. Pilot Generator

Located on Card #8

(NOTE: The output of this circuit is not used in the 8185A Stereo Generator; it is only used when this card is used in the older 8182A/SG Stereo Generator.)

The Binary Divider is configured to produce pulse trains at 1H and 3H. These are buffered by a pair of Exclusive-OR gates, one of which acts as an inverter and one of which acts as a non-inverter. The outputs of the two gates (at 1H and 3H) are summed in proper proportion to cancel all lower-order harmonics of H. Higher-order harmonics are eliminated in a third-order low-pass filter. The resulting output of the low-pass filter is a sinewave at 1H with approximately 0.025% THD. This is used as the stereo pilot tone and also as a reference for the Stereo Baseband Generator.

Component-level description:

The output of the PLL's VCO (at 16H) is applied to binary divider IC4. IC3a and associated components are a power-up startup circuit for IC4. IC4 is gated by IC3b and IC3c such that a 1H pulse of controlled duty-cycle appears at pin 5, and a 3H pulse of controlled duty-cycle appears at pin 11. The signal at pin 11 is inverted by IC2a, while the signal at pin 5 is passed without inversion through IC2b. The outputs of IC2a and IC2b are summed in R30 and R31 such that all lower harmonics of H are cancelled. Remaining harmonics are filtered-out in third-order inverting low-pass filter IC1a and associated components. The output of IC1a is a 1H sinewave with about 0.025% THD.

17. Pilot AGC

Located on Card #8

(NOTE: The output of this circuit is not used in the 8185A Stereo Generator; it is only used when this card is used in the older 8182A/SG Stereo Generator.)

To ensure that the pilot level remains stable, an AGC loop is employed. The peak level of the pilot is detected with a comparator which is referenced to the stable positive power supply. If the pilot level attempts to exceed the comparator reference, the comparator produces error pulses which reduce the voltage on an integrating capacitor. The voltage on this capacitor is coupled to the positive supply voltage terminal of the gates which buffer the Binary Divider. The output level of the gates changes in proportion to the positive supply voltage on the chip, closing the AGC loop.

Component-level description:

IC1b serves as a comparator. When the peak level of the 1H sinewave at the output of IC1a goes more positive than the voltage at the junction of R39 and R40 (i.e., +2.72V pk; 1.92Vrms), a negative-going pulse appears at the output of IC1b. Ordinarily, voltage divider R36, R37 holds C15 at approximately +7.5VDC. Output pulses from IC1b pass through CR6 and R38 and discharge C15 towards ground. This reduces the output level of IC1a until comparator IC1b is almost fully off.

The voltage on C15 affects the output level of IC1a as follows: C15 is buffered by emitter-follower Q2, which in turn supplies the power supply voltage for IC2. The amplitude of the output pulses of IC2a and IC2b vary in proportion to IC2's power supply voltage. Thus the drive to filter IC1a is varied, varying its output level and closing the AGC loop.

In stereo mode, the voltage on the GSTER line from the stereo generator is approximately 0VDC and the comparator reference divider R39, R40 operates normally, producing +2.72V at IC1b's "+" input. In any mono mode, the voltage on the GSTER line becomes −15VDC. This forces the "+" input of IC1b below ground and forces the output of IC1b to saturate to the negative rail. CR5 turns ON, clamping the control voltage output at the emitter of Q2 to approximately 0VDC. This removes power supply voltage from IC2, suppressing the stereo pilot tone.

18. Stereo Baseband Generator — General Principles

Located on Card #7

In the BTSC system, the L+R signal is passed through to the baseband output directly, while the L−R signal is multiplied by 2H, creating a double-sideband suppressed-carrier subchannel. The 8185A's Hadamard-Transform Stereo Baseband Generator™ closely approximates an ideal multiplier by a switching technique.

The L−R signal is passed through two analog switches whose outputs are summed together. These switches are driven by individual pulse trains, both synchronized to 2H, and shaped so that all harmonics of 2H prior to the 7th harmonic are cancelled. By comparison to a conventional switching modulator, performance requirements of the output low-pass filter (to remove harmonics above 7H) are greatly eased, and excellent separation and spurious rejection can be obtained from a relatively modest filter.

The stereo pilot tone is generated by multiplying a DC voltage by three individual pulse trains in three analog switches. Harmonics up to the 14th are canceled. The resulting waveform is passed through the same low-pass filter as the stereo subchannel, ensuring correct phasing between the pilot tone and stereo subcarrier.

Stereo/mono mode switching is provided by JFET switches driven by CMOS logic. In addition, there are three special "test" modes available. Each accepts the L+R signal from the preceding processing. The first grounds the L−R input port and applies signal to the L+R input port to test main-channel-to-subchannel crosstalk. The second grounds the L+R input port and applies signal to the L−R input port to test subchannel-to-main-channel crosstalk. The third applies equal signals to the L+R and L−R input ports to produce a "flat baseline" FM-stereo-style signal which permits separation to be optimized using only an oscilloscope.

The block diagram shows the major subsystems in the Stereo Baseband Generator and should help clarify the discussion below.

19. Stereo Modulator

Located on Card #7

The L–R signal is applied to a buffer amplifier. This amplifier has a DC servo that eliminates virtually all the DC offset that might have accumulated in earlier circuitry. (DC offset must be eliminated because it otherwise translates into loss of subcarrier suppression after modulation.) The output of the buffer amplifier is applied to a pair of analog switches which perform the modulation of the L–R signal by the subcarrier.

Equal + and - DC voltages are applied in parallel to three pairs of analog switches to generate the pilot tone. The amplitude of the pilot tone is determined by the DC voltage level. The pilot tone is turned off by reducing the DC voltage to zero.

The L+R signal is applied to a buffer amplifier with DC servo. This servo forces the DC at the outputs of the analog switches to be equal to zero, further reducing any subcarrier leakage. The output of this amplifier is summed with the outputs of the various analog switches prior to the low-pass filter. A separation control adjusts the amplitude of the L+R signal, permitting the L+R and L–R to be mixed with exactly equal gains, thus maximizing separation.

The analog switches effectively multiply their inputs by either +1 or 0, depending on whether the switches are on or off respectively. Thus the L–R signal is multiplied not only by the stereo subcarrier, but also by an average DC voltage. Therefore, a substantial undesired baseband L–R component appears at the output of the analog switches. This is cancelled by mixing a precise amount of out-of-phase L–R audio into the output of the switches. Cancellation is maximized with the sub-to-main crosstalk trimmer.

High-order harmonics generated in the switching process are eliminated in a fifth-order passive elliptical filter followed by a group delay corrector. The group delay of the corrector can be adjusted with the 15kHz separation trimmer to minimize variations in the overall group delay as a function of frequency, thus maximizing overall separation. Equivalent 75µs separation of >70dB is theoretically possible with this filter design.

The output of the filter is applied to a power buffer capable of driving two 75Ω loads in parallel. The Professional Channel subcarrier (if used) is mixed into this buffer. There is also an input for an external SAP generator.

Component-level description:

The L–R signal is buffered by IC22a, which has gain of 0.713x. IC21a is a DC servo to remove DC offsets. CR1-CR6 are clamping diodes to protect the analog switches IC7 and IC8 from being driven beyond their ±5V input range.

IC9a and IC9b provide +0.943VDC and −0.943VDC reference voltages for the pilot tone generator. These voltages are applied to analog switches within IC7 and IC8. When mono mode is selected, the +5VDC voltage at the high side of R7 is reduced to 0V, removing the DC pilot reference voltages and suppressing the pilot generator. (The pilot switching waveforms applied to IC7 and IC8 are also removed in mono mode.)

The L–R signal is applied through the sub-to-main crosstalk null trimmer R12 and through switching FET Q1 to IC22b. The signal is inverted by IC22b and is then applied to the output of the analog switches to cancel crosstalk.

In mono mode, switching waveforms are removed from analog switch IC7, and Q1 is turned off (by applying -15VDC to its gate), preventing L-R from being applied to the generator's output.

The L+R signal is applied to IC22b through separation control R14. IC21b is a DC servo that essentially prevents any DC from appearing at the outputs of the analog switches IC7, IC8.

L1, L2, and C3-C9 form a passive fifth-order elliptical filter with a cutoff frequency of approximately 70kHz. This is buffered by non-inverting amplifier IC16 and applied to all-pass group-delay corrector IC17 (see **Group Delay Correctors** on page 6-6 for a general description of this circuit topology).

The output of the Stereo Modulator, along with the SAP, and Pro signals, are summed into composite opamp IC19, IC20, and associated components. IC20 is a special high-slew-rate power buffer which is located within the overall opamp feedback loop. It isolates IC19 from the destabilizing effects of capacitive loads and also permits 75Ω loads to be driven without degradation. This line driver will drive up 1.5V pk into 0.047μF in parallel with 37.5 ohms before significant non-linear errors (increases in spurious components as observed on a baseband spectrum analyzer) or linear errors (noticeable deterioration of baseline flatness at 15kHz in the separation test mode) are apparent.

Output level is adjusted by varying the feedback resistor in the overall feedback loop of IC19, IC20 by means of R42, thus varying the gain to all baseband components, including the SAP and Pro subcarriers.

IC15 is an auxiliary summing amplifier to provide a reference signal, unaffected by the output level control, for the composite peak-reading meter.

20. Switching Waveform Generator

Located on Card #7

Switching waveforms for the analog switches IC7, IC8 are stored in a Read-Only Memory (ROM), and are clocked out in synchronism with the horizontal line frequency 1H.

Component-level description:

IC4 is a dual binary counter that is clocked from the 16H output of Card #8 to create a four-bit address word for ROM IC5. This word, which appears on pins 11-14 of IC4, constantly counts up until it reaches 1111B, at which point is resets to 0000B.

The counter only drives half of the bits in the ROM's address word. The other half of the bits in the ROM address are used to statically switch between various bit patterns stored in the ROM. For example, switching IC5 (address inputs A6 and A7) low causes the output waveform that drives the pilot switches in IC7, IC8 to become "0" at all times, suppressing the pilot. Similarly, driving IC5 (address input A4) low suppresses the stereo switching waveforms.

The output of IC5 is latched by octal D-flip-flop IC6. IC6 is clocked by the 16H signal to ensure that all switching waveforms change simultaneously and cleanly.

21. Mode Switching Logic

Located on Card #7

The 8185A Stereo Baseband Generator has four switch-selected modes of operation. Three are special test modes, and are used only when making stereo performance verification measurements.

The first of these facilitates measurement of main-to-sub crosstalk by applying the Stereo Baseband Generator's L+R input signal into its L+R input port (as is normal), and suppressing the input into its L–R input port.

The second mode facilitates the measurement of sub-to-main crosstalk by injecting the signal on the L+R input line into the Stereo Baseband Generator's L–R input port. This test mode in useful in adjusting the Stereo Baseband Generator's internal sub-to-main crosstalk null trimmer.

The third test mode allows separation to be optimized by connecting the L+R input line to both L+R and L–R inputs, producing an FM-stereo-style "flat baseline" oscilloscope waveform. This works because the L+R and L–R inputs of the Stereo Baseband Generator have been designed to have equal gain. The doubling of the stereo subchannel amplitude is achieved by doubling the audio input to the Stereo Baseband Generator's L–R input port.

The normal mode is OPERATE. In this mode, three sub-modes are available by remote control or by switching the front-panel stereo/mono switch.

The first is STEREO. It simply generates a normal stereo baseband output from the signals on the L+R and L–R Stereo Baseband Generator input lines.

The second and third sub-modes are MONO LEFT and MONO RIGHT. A given mono mode uses the signal at the output of the Left or Right Six-Pole Filter (depending on whether MONO LEFT or MONO RIGHT is selected), and applies this signal to both the Left and Right channels of subsequent processing. The Pilot Generator and **Stereo Modulator** are suppressed (see **19. Stereo Modulator on page 6-18** above).

A CMOS three-state latch using three NAND gates "remembers" the logic state. Note that the three manually-switched test modes are not directly integrated into the logic system. It is therefore necessary to manually enter stereo mode before making crosstalk and separation measurements.

The truth table below shows the state of each JFET switch in the system under various conditions. Further understanding of the operation of the logic and switching system in the 8185A may be obtained by studying this table.

Component-level description:

The three basic logic states – STEREO, MONO LEFT, and MONO RIGHT – are "remembered" by three CMOS NAND gates in IC13. The output of each gate is connected to an "output bus" through a 47K isolation resistor R51, R52, R53 to permit pulling a given output bus down without damaging its associated gate. A sub-mode is ON when its output bus is at -15V, and OFF when its output bus is at ground. The two inputs of each gate are connected to the two output busses of the other two gates. Thus, if either of the other gates is ON, the gate in question is held OFF. However, if the output bus associated with the gate in question is externally pulled ON, the

other two gates are pulled OFF; thus the gate in question is latched ON. Logic switching is effected by momentarily switching any of the gate output busses to -15V; this is done by forcing the transistors in optoisolators IC10, IC11, IC12 to conduct by passing current through their LED's (remote control), by operating the momentary front-panel STEREO/MONO switch, or by the power-up circuit, which uses R56, C16, and CR8 to hold a selected output line at -15 for a fraction of a second after power-up.

Failures in the mode-switching logic will almost certainly be due to failures of IC13, IC14, IC10, IC11, or IC12, or to failures in the JFET switching transistors. All of these components can be freely replaced as necessary without readjustments.

Note that the phototransistors in IC10-IC12 have had their base leads (pin 6) cut off flush with the IC package. This is because the base lead is extremely sensitive to leakage currents, and condensing moisture is quite sufficient to cause false switching. It is therefore extremely important that the base lead be cut off if any of these optoisolators are ever replaced.

Essentially no further circuit description is required, as most of the circuitry is integrated onto the CMOS logic chips. The discussion of operational principles supplied above, plus examination of the truth table (Fig. 6-4 below), should suffice to permit full understanding of the operation of the logic. (Some readers may be unfamiliar with the Exclusive-OR gate, IC14. This logic element operates such that its output is at -15 volts when its inputs are the same, and at 0 volts when its inputs are different.)

INPUTS				OUTPUTS				MODE
STEREO	MONOR	MONOL	BSYNC	LMONOL	LMONOR	GSTER	STEREO LIGHT	
0	1	1	1	0	0	1	ON	STEREO
1	0	1	1	1	0	0	OFF	MONO RIGHT - SYNC
1	1	0	1	0	1	0	OFF	MONO LEFT - LOCKED
1	1	1	1	NC	NC	NC	NC	PREVIOUS MODE
0	1	1	0	0	0	1	OFF	STEREO
1	0	1	0	1	0	0	OFF	MONO RIGHT - SYNC
1	1	0	0	0	1	0	OFF	MONO LEFT - UNLOCKED
1	1	1	0	NC	NC	NC	OFF	PREVIOUS MODE

NOTES: 1) 0=-15V, 1=GND, NC=no change from previous status

2) The response of the logic to the remote control inputs, the STEREO MONO switch and the power-on circuit is identical, and the inputs are taken to be the 3 lines labeled STEREO, MONO R and MONO L on the schematic.

Fig. 6-4: System Logic Truth Table

22. Monitor Circuit

Located on Card #6

The purpose of the monitor circuit is to accurately decode the Left and Right channels from the dbx-encoded sum-and-difference audio signal, thus aiding adjustment and verification of stereo generator operation independent of the aural exciter, transmitter, diplexer, antenna, and modulation monitor.

The monitor circuit consists of a pair of 75µs de-emphasis networks, a dbx N/R Decoder card, a decoder sum compensator, and a precision de-matrix which uses a resistor array with resistors matched to ±0.1%.

When the MONITOR N/R DECODER switch is OUT, de-emphasis is applied to both L+R and L–R inputs by precision-matched 75µs de-emphasis networks. The decoder sum compensator is switched out of the circuit.

When the MONITOR N/R DECODER switch is IN, L–R de-emphasis is replaced with the dbx Decoder Card, and the decoder sum compensator is switched into the L+R signal path.

The Monitor Circuit has been designed to serve as a reference for testing and adjustment of the rest of the 8185A system. There are no alignment controls, and the accuracy of the Card exceeds that of the rest of the system. When the MONITOR N/R DECODER switch is OUT (requiring the N/R ENCODER switch to also be OUT), then the "equivalent stereo separation" of the monitor card alone exceeds 45dB, 30-15,000Hz. When the MONITOR N/R DECODER switch is IN (requiring the N/R ENCODER to also be IN), then monitor card swept sinewave separation is limited by the performance of the dbx Decoder Card, and exceeds 40dB, 50-10,000Hz, at 10% equivalent input modulation.

Component-level description:

The L+R is applied to the card with a nominal level of 1.768Vrms for 100% modulation. The L–R is applied with a nominal level of 3.536Vrms for 100% modulation. The de-matrix exhibits unity gain to the L–R signal and 2x gain to the L+R signal. At low frequencies unaffected by de-emphasis, the nominal output level produced by equal Left and Right levels (@100% Main Channel modulation) is 3.536Vrms (+8.751dBu) +1% at both Left and Right Monitor Outputs when loaded by 100K or greater. Output impedance is 600Ω unbalanced.

The dbx N/R Decoder Card is described in an **Appendix** on page 6-26.

23. Meter Peak Detector

Located on Meter Resistor Card

The VU meter on the front panel is electronically conditioned to be peak-reading. Jumper "A" selects an integration time that shows the true instantaneous maximum of every peak, no matter how low its energy ("0ms"), or an integration time that ignores most inconsequential, low-energy peaks while still clearly indicating the peak level of program energy ("1.5ms").

Component-level description:

The signal to be metered is applied to buffer amplifier IC1a, whose gain is switchable by the meter gain switch between 0dB and 20dB. The output of IC1a is applied to full-wave rectifier IC1b. R17 and DS1 clip the half-wave AC output of IC1b to avoid overloading the meter. The rectified signal is then applied to peak detector with delayed release IC2 (and associated circuitry).

The peak detector uses feedback around the peak-detector hold capacitors C1, C2 and buffer amplifier IC2b to accurately capture and hold peaks. The DC output of the peak detector appearing at pin 1 of IC2a is fed back to the "–" input of IC2b. If the voltage on the "+" input of IC2b exceeds the voltage on its "–" input, then IC2b charges C1 and C2 through diode- connected transistors Q1, Q4 until the peak detector's DC output is equal to the voltage on the "+" input of IC2b.

The R21, R22, R23 network is a bootstrapped release time circuit which interacts with a delayed release circuit. When C1, C2 are not being charged, C2 discharges through R21. However, C1 cannot discharge until C2 has fallen about 1.2VDC below C1 so that diode-connected transistors Q2 and Q3 can turn on. This provides a hold time – a delayed release – that allows the meter to reach the full value of the peak despite its mechanical inertia.

The output of IC2a is at the same voltage as C1. Thus the junction of R22 and R23 is held approximately 0.8V below the voltage on C1 by virtue of the negative current flow through R22, R23. This provides an approximation to a constant current flow through R21, and thus a constant-slope release of approximately 3.6V/sec for C2. (The presence of the delayed release circuit substantially complicates this simplistic explanation and causes the release to diverge from constant slope. Nevertheless, the essential bootstrap principle still applies.)

Diode-connected transistor Q5 prevents saturation of IC2b by actively clamping the output of IC2b to 0.7V below the output voltage of IC2a when IC2b is not charging C1, C2.

C7 and R16 are frequency-compensation components to prevent overshoot and oscillation of the circuit.

24. Power Supplies

Mostly located on Card #PS

Most power for 8185A circuitry comes from a highly regulated ±15-volt power supply. The main supply is +15 volts, created by a 723C IC regulator with current-boosted output, current limiting, and over-voltage protection using a zener diode and fast-blow fuse.

The −15-volt supply is essentially a current-boosted opamp in a unity-gain inverting configuration which "amplifies" and inverts the +15V supply, thus tracking it. The −15V supply is also current-limited and protected against overvoltage. Both +15V and −15V supplies are located on a circuit board mounted on the inside of the rear chassis apron. This apron is also used as a heat sink for the regulator power transistors.

Component-level description:

The unregulated power supply (mounted inside the chassis, but outside of the RF-tight enclosure) is wholly conventional. It consists of dual-primary transformer T101, two full-wave rectifiers (CR101, CR102 and CR103, CR104), and two energy storage capacitors (C101 and C102).

T101's primary can be configured for 115-volt operation by paralleling its two primaries, or for 230-volt operation by connecting its two primaries in series (with a switch). RF filtering is provided on the AC line by FL101. In addition, C103, C104, C105, C106, C107, L101, L102 filter RF from the unregulated DC supply lines as they enter the chassis. The chassis is divided into three major sections to facilitate RF suppression. The section to the left (unregulated power supply chamber) contains the AC wiring and the unregulated power supply, and is assumed to contain some RF. The card cage, to the right, uses RF suppression on each line entering or leaving the area, and is thus free from RF. The RF shielding box on the rear panel, which interfaces the audio input and output lines with the outside world, contains the input pads — its connections to the main RF-tight compartment are all RF-filtered.

The +15-volt regulator (located on Card #PS) is the main reference for all other voltages in the 8185A. It employs 723C IC voltage regulator IC101 in conjunction with external series-pass transistor Q101. This transistor is mounted on the rear apron of the chassis, which serves as a heat sink.

IC101 contains a reference voltage source, an opamp (externally compensated by C109 to prevent oscillation), and a current-limiting transistor. The reference voltage (nominally +7.15V) is developed at pin 6. C108 filters high-frequency noise from the reference voltage, which is directly connected to the non-inverting input (pin 5) of the internal opamp. Voltage divider R105, R106, R107 develops a precise fraction of the output voltage of the regulator at the wiper of +15V ADJUST trimmer R106. The wiper of R106 is connected to the inverting input of IC101's internal opamp. Negative feedback forces the voltage at R106's wiper to be equal to the reference voltage, so the output voltage of the regulator is always the reference voltage divided by the voltage divider gain.

The output current flowing through Q101 develops a voltage drop across R103. When the current exceeds approximately ¾-amp, the voltage drop is sufficient to turn on the current-limiting transistor inside IC101. Since this transistor's base-emitter junction is connected to pins 2 and 3 of IC101, it then shunts base drive current from the external series-pass transistor Q101 and prevents damage due to overheating.

If a catastrophic failure in the +15-volt regulator causes it to lose control over its output voltage, the rest of the circuitry must be protected against the full unregulated voltage, or the entire system will be severely damaged. This protection is provided by zener diode VR101, CR105, and 1-amp fast-blow fuse F102. If the regulator loses control of the output voltage, VR101 will conduct and limit the output voltage to approximately 16.5 volts (which will not damage the system). Extremely large amounts of current will flow in VR101. Ordinarily, this current will blow F102 and disconnect the circuitry from the unregulated supply before VR101 is damaged. VR101's clamping action will also prevent the negative tracking supply from exceeding −16.5 volts. When the regulator is operating properly, the current-limiting circuitry will prevent F102 from blowing even if the regulator output is short-circuited. (In certain unusual circumstances, the current-limiting circuit may still work, even though the regulator has lost control of its output voltage. If this occurs,

F102 will not blow, and VR101 will overheat and burn out. Because its failure mode is a short-circuit, VR101 will still protect the 8185A circuitry even in this exceptional circumstance.)

The −15-volt regulator (located on Card #PS) is an opamp that contains a discrete power-booster output stage with current-limiting. It "amplifies" the output of the +15-volt regulator by −1 to produce a −15-volt tracking supply. Shutdown of the +15-volt supply (due to current-limiting conditions or to a fault which blows F102) will also result in shutdown of the −15-volt supply. The basic opamp is IC102. Its input resistor R109 and feedback resistor R108 are of equal valued, resulting in a gain of −1 ±2%. IC102's negative supply comes from the *unregulated* −22-volt supply. The common-mode range of IC102 includes its positive power supply, which permits operation with the chip's positive supply at ground. In normal operating conditions, the IC102's + input of IC102 is grounded, and its − input is within 10mV of ground.

Q103 and Q102 form a conjugate emitter-follower which can boost the output current of IC102 to more than ¾-amp. The basic emitter-follower is Q103. Q102 is connected in a 100% negative feedback configuration to boost the current output capability of Q103.

Q104 is a current-limiting transistor. If the −15-volt supply is called upon to deliver more than ¾-amp, a sufficient voltage drop (approximately 0.6 volts) will occur across R104 to turn on Q104, thus shunting drive current away from Q103 into the load and protecting Q102,Q103 from burn-out (IC102 is protected by internal current-limiting circuitry). C113 frequency-compensates the −15-volt supply to protect it against high-frequency oscillations. R102 increases the circuit's immunity to leakage in Q103.

Zener clamp VR102, CR106, and fuse F103 protect the rest of the circuitry from a catastrophic failure of the −15-volt regulator. The operation of this circuit is identical to the operation of the corresponding circuit in the +15-volt regulator.

This concludes the Circuit Description.

APPENDIX: dbx Noise Reduction Cards

The following data sheets were supplied by dbx, and describe the noise reduction encoder on Card #4 and the noise reduction decoder on Card #6.

525 Series
dbx-TV
Noise-Reduction Cards

DESCRIPTION

The dbx-TV noise-reduction system is designed to preserve the quality of audio signals transmitted using the Zenith multichannel-television-sound transmission standard. The series comprises two units: a high-spec compressor (525CH), for encoding the audio signal before transmission, and a complementary high-spec expander (525EH), for decoding the signal after transmission. With a bandwidth of 50 Hz-15 kHz, the system operates on both the stereo difference channel and the second-audio-program (SAP) channel, where dynamic range may be as low as 26 dB. An improvement of more than 50 dB in S/N ratio in the transmission channel is possible, yet the user need not extend his present efforts to prevent overmodulation.

The 525CH encoder will be used for broadcasting and for production-line testing of television sets. The 525EH decoder will be used for professional broadcast monitoring and as a reference on television production lines. Each unit complies with the recommendations of the FCC's Office of Science and Technology (Bulletin 60) on separation when used in the stereo difference channel.

Each 525 unit is a circuit board that requires an external power supply. In order to allow flexibility in transmission implementations, an external lowpass filter is required to prevent out-of-band signals from causing interference and/or crosstalk into other channels.

FEATURES

-- Unique spectral-companding system

-- Reduces noise from transmission channels by up to 50 dB

-- Can be used with channels having as little as 26 dB of dynamic range

-- Flat response 50 Hz-15 kHz

-- High performance: 0.1%-tolerance resistors and capacitors

-- Typically better than 35-dB midband separation (stereo-difference-channel applications).

SPECIFICATIONS	525CH (Compressor)	525EH (Expander)
INPUT IMPEDANCE	20 k-ohms	same
OUTPUT IMPEDANCE	Less than 1 ohm	same
INPUT LEVEL		
100% modulation at 300 Hz	+13.2 dBm (3.54 V)	+4.7 dBm (1.33 V)
Nominal at 300 Hz	-3.8 dBm (500 mV)	-3.8 dBm (500 mV)
OUTPUT LEVEL		
Maximum at 300 Hz	+4.7 dBm (1.33 V)	+13.2 dBm (3.54 V)
Nominal at 300 Hz	-3.8 dBm (500 mV)	-3.8 dBm (500 mV)
FREQUENCY RESPONSE*		
Sine-wave sweep		
20-100 Hz	±0.15 dB	±0.3 dB
100-8k Hz	±0.07 dB	±0.2 dB
8-14 kHz	±0.2 dB	±0.6 dB
TOTAL HARMONIC DISTORTION (THD) (at 300 mV, enc/dec, broadcast bandwidth)		
Maximum	0.2%	
Typical	0.1%	
OUTPUT NOISE	not applicable	greater than 85 dB below 100% modulation
UNITY-GAIN INPUT LEVEL (level-match point)	-3.8 dBm (500 mV) at 300 Hz	same
MINIMUM CHANNEL DYNAMIC RANGE (DR)	26 dB	
EFFECTIVE INCREASE IN DR	greater than 40 dB, depending on transmission medium	
POWER-SUPPLY REQUIREMENTS		
Voltages	±12 V	same
Tolerances	±50 mV	same
Current	less than 70 mA	same
DIMENSIONS		
PC board	approx. 4" x 5.5" (10.2 x 14 cm)	same same
COMPONENT HEIGHT		
above PCB	0.7" maximum	same
below PCB	0.25" maximum	same
CONNECTORS (optional)	4-pin right-angle (Molex part 22-05-1042, dbx part 280200); 6-pin right-angle (Molex part 22-05-1062, dbx part 280199)	
TEMPERATURE RANGE	10-40° C	same

*Frequency response is within the stated tolerance of the standard encode/decode response curves at 10% 75-us equivalent-input modulation, with the response of the accompanying sum-channel-compensation circuits taken into account.

dbx 525EH
Operating Guide

The dbx 525EH is a broadcast-quality printed circuit board which can be used to decode the dbx-TV noise-reduction characteristic of the BTSC format for multi-channel television-sound transmission. The 525EH card has been aligned at the factory using NBS-traceable measurement equipment to meet FCC recommended practices; no user adjustments are necessary. This guide is intended to allow the user to operate the 525EH card to decode dbx-TV noise reduction with minimum difficulty.

The operating information on the following pages has been separated into six categories:

1. Connections
2. Supply Voltages
3. Input/Output Levels
4. Filtering (optional)
5. Sum-Channel Processing
6. Operating Characteristics

Further information is available in the 525 Series spec sheet.

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525EHG011185

1. Connections

The input, output, rms-detector input, and power-supply connectors are 4- and 6-pin Molex right-angle connectors as shown in the attached 525EH top view. The connector part numbers are:

4-pin	Molex part 22-05-1042	dbx part 280200
6-pin	Molex part 22-05-1062	dbx part 280199

As you can see from the pinout, redundancy -- doubling the pins for each connection -- ensures high reliability for all connections.

2. Supply Voltages

The 525EH is designed to operate from a bipolar supply of ±12 VDC, capable of 70 mA current. Tolerances on the ±12-V supply are not critical, but caution should be applied to ensure that noise and hum are kept to a minimum.

3. Input/Output Levels

The 525EH is calibrated for operation where 100% modulation of the difference (L-R) channel corresponds to 10.000 VP-P. Operation at other levels is not recommended. Input levels up to 10 VP-P are allowed at low frequencies, but typically will not reach this level -- even in the extreme case of left- or right-only program material.

The 525EH is capable of handling inputs of 10 VP-P, and can therefore accept a 50-kHz deviation of the difference channel (100% modulation). Note, however, that the 525CH compressor will keep average levels well below 100% modulation. Only brief transients will cause the compressor output (and the expander input) to reach 10 VP-P.

The card's input impedance is 20 kΩ, while its output impedance is <1Ω (an op-amp output). It is important to consider these impedances since designs should compensate for any resistive attenuation. Capacitive loading is not recommended.

4. Filtering

Some form of filtering must be used if out-of-band signals interfere with the rms detectors in the 525EH. If signal-path filtering is used, a matched filter must be placed in the sum-channel path to maintain separation. Beginning with the Phase-4 version of the 525EH, the cards

offer an rms-detector input to allow filtering of the signal which is fed to the detectors. The benefit of this feature is that mistracking due to out-of-band interference may be eliminated without the need for critical matching of filters. Since the rms detectors are not phase sensitive, the phase response of an external rms-path filter is inconsequential. Furthermore, if the amplitude response of the filter is flat within ±0.1 dB to 15 kHz, separation will not be degraded. It is not necessary to use as complex a filter in the decoder as in the encoder; a fourth-order filter should be adequate.

5. Sum-Channel Processing

The noise-reduction encoders and decoders for dbx-TV are designed to be fully complementary. However, ac-coupling components, finite-bandwidth opamps and the like will cause phase shifts and/or amplitude errors that could affect stereo separation. Such errors in the difference channel can be rendered inconsequential by precisely duplicating them in the sum channel.

Attached is a schematic for a sum-channel-processor circuit that compensates for bandwidth limitations in the 525EH itself. The location of this circuit in the sum channel is not critical, but it must be included somewhere in the sum channel of the receiver. When building this circuit, it is important to keep its overall gain at precisely unity so that stereo separation will not suffer. Low impedances should be used to minimize capacitive effects of the opamps.

6. Operating Characteristics

All 525EHs are aligned and burned-in. Each is ready to be plugged into broadcast-monitoring or test equipment and used with no further adjustment. Following is a brief discussion to answer the question: "Is my card operating correctly?"

A few simple concepts can be presented that generally describe the card's operation. With no input signal, the wideband expander will attenuate greatly, and the spectral expander will exhibit maximum demphasis. The resulting output of the card should be vanishingly small.

A low-frequency single-tone input will capture the attention of the wideband rms-level detector and will be processed with a 1:2 expansion factor (i.e., a 1-dB input-level change will cause a 2-dB output change). The spectral expander, which will attenuate high frequencies (and noise), will not be greatly affected by low-frequency single tones, and will not generally affect these either. As the input frequency increases, the 525EH will behave more like a 1:3 expander.

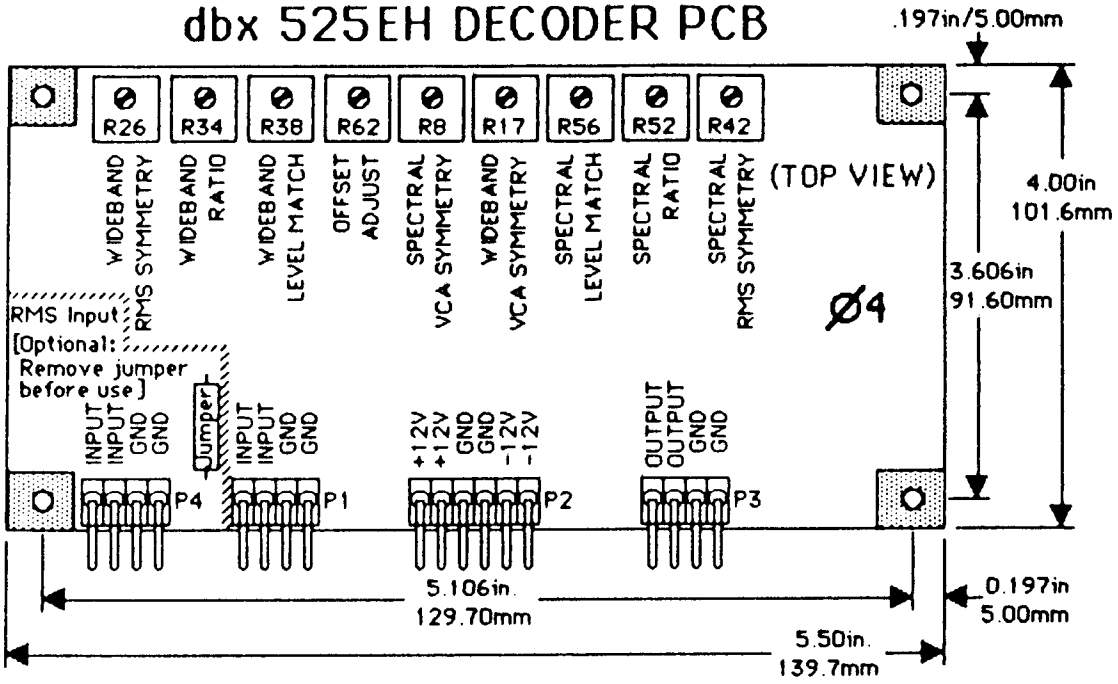
A consequence of the 525EH's deemphasis and the finite amount of time required by its rms detectors to respond to sharp increases in input level is that input signals with transient information will often cause the expander to undershoot. Transients will actually become dulled. Of course, since the compressor causes transient overshoots, the expander will restore transients to their original characteristics.

Two approximate alignment points can be used to make a rough check of the expander:

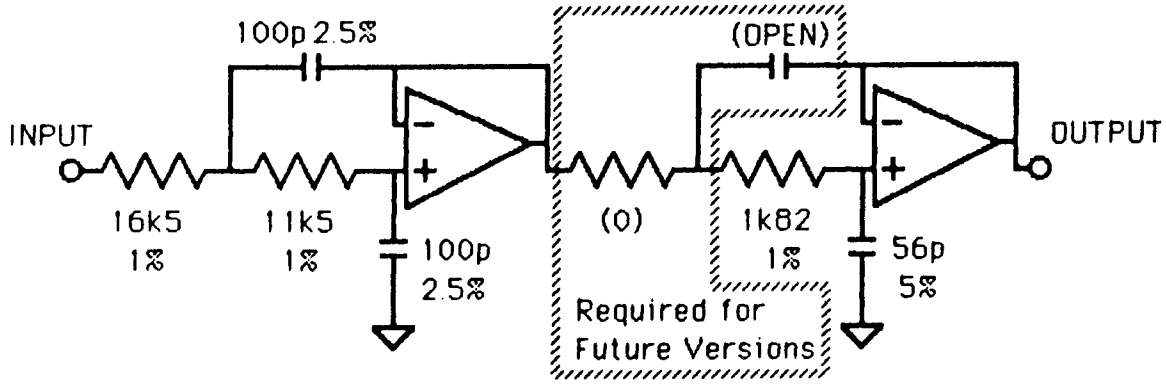
Input Frequency	Input Level	Desired Output Level
300 Hz	500 mVRMS	500 mVRMS
8 kHz	1.13 VRMS	136 mVRMS

For further information about the dbx 525EH card, please contact dbx OEM Products Division.

dbx 525EH DECODER PCB



dbx 525EH DECODER SUM-CHANNEL PROCESSOR



Phase 3 & Phase 4 Compensation

[FOR USE WITH 260584-00 AND 260584-01 PC-BOARDS]

Separation: >36dB, 50Hz to 8kHz; 30dB @ 15kHz

NOTE: OPAMPS ARE NE5532 OR EQUIVALENT

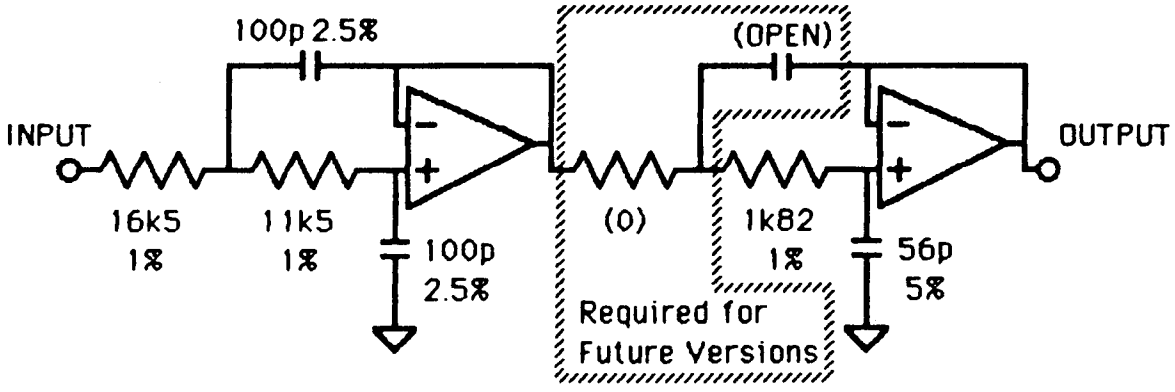
Operating Level:

100% Modulation = 10.000 V_{p-p}

525EH4 013185

525EH dbx-TV Decoder Sum-Channel Processors

[PHASE 3 AND PHASE 4]



Phase 3 & Phase 4 Compensation

[FOR USE WITH 260584-00 AND 260584-01 PC-BOARDS]

Separation: >36dB, 50Hz to 8kHz; 30dB @ 15kHz

NOTE: OPAMPS ARE NE5532 OR EQUIVALENT

The circuit shown above is for compensating Phase 3 & 4 525EH cards. Because dbx may revise the 525 cards periodically for improved performance, the component values shown are subject to change. As improvements are made, dbx will endeavor to maintain this sum-channel processor topology. Please be aware that changes may be required.

525EH3/4 120384

dbx 525CH
Operating Guide

The dbx 525CH is a broadcast-quality printed circuit board which can be used to implement the dbx-TV noise-reduction characteristic of the BTSC format for multi-channel television-sound transmission. The 525CH card has been aligned at the factory using NBS-traceable measurement equipment to meet FCC recommended practices; no user adjustments are necessary. This guide is intended to allow the user to operate the 525CH card to implement dbx-TV noise reduction with minimum difficulty.

The operating information on the following pages has been separated into six categories:

1. Connections
2. Supply Voltages
3. Input/Output Levels
4. Filtering
5. Sum-Channel Processing
6. Operating Characteristics

Further information is available in the 525 Series spec sheet.

525CH6011185

1. Connections

The input, output, filter, and power-supply connectors are 4- and 6-pin Molex right-angle connectors as shown in the attached 525CH top view. The connector part numbers are:

4-pin	Molex part 22-05-1042	dbx part 280200
6-pin	Molex part 22-05-1062	dbx part 280199

As you can see from the pinout, redundancy -- doubling the pins for each connection -- ensures high reliability for all connections.

2. Supply Voltages

The 525CH is designed to operate from a bipolar supply of ±12 VDC, capable of 70 mA current. Tolerances on the ±12-V supply are not critical, but caution should be applied to ensure that noise and hum are kept to a minimum.

3. Input/Output Levels

The 525CH is calibrated for operation where 100% modulation of the difference (L-R) channel corresponds to 10.000 VP-P. Operation at other levels is not recommended. Input levels up to 10 VP-P are allowed at low frequencies, but typically will not reach this level -- even in the extreme case of left- or right-only program material. At higher frequencies, the situation is more complex. Since the sum (L+R) channel is preemphasized at 75 µs and constrained to a maximum of 100% modulation, the maximum sum-channel signal will follow a 75-µs deemphasis curve. As a result, the difference channel is unlikely to see 10 VP-P at higher frequencies. Rather, the difference channel's maximum signal level will also follow a 75-µs deemphasized curve, and the 525CH will easily accept signals at this level.

Since the 525CH compresses large signals downward in amplitude, typical outputs will be well below 100% modulation. However, transient material may reach this level occasionally. The 525CH is capable of reaching 10 VP-P, and can therefore drive the difference channel to 50-kHz deviation (100% modulation).

Signal and filter input impedances are 20 kΩ, while signal and filter output impedances are <1Ω (opamp outputs). It is important to consider these impedances since designs should compensate for any resistive attenuation. Capacitive loading is not recommended.

4. Filtering

Lowpass filtering is part of the BTSC standard. Each of the stereo sum- and difference-channels must not contain spectral information beyond 15 kHz, which might interfere with the 15.734 kHz pilot tone or which might spill into the other channel. The SAP channel, too, has a bandwidth constraint, though at a lower frequency: 10 kHz. The 525CH has ports to connect a 15-kHz or 10-kHz lowpass filter within the compressor loop. This topology is preferred, since it does not induce decoder mistracking or stereo-separation errors. For proper operation, the 15-kHz lowpass filter in the stereo difference-channel compressor loop must have a companion 15-kHz LPF in the sum-channel signal path. This 15-kHz LPF pair must be closely matched to maintain stereo separation. Since the SAP channel is not stereo, matching in the 10-kHz SAP LPF is not applicable.

For proper encode/decode tracking, filters in the compressor loop must yield precisely unity gain in their passbands. Recommended filter designs for both stereo and SAP are available from Zenith (contact Pieter Fockens at [312] 391-8430).

5. Sum-Channel Processing

The noise-reduction encoders and decoders for dbx-TV are designed to be fully complementary. However, ac-coupling components, finite-bandwidth opamps and the like will cause phase shifts and/or amplitude errors that could affect stereo separation. These errors in the difference channel can be rendered inconsequential by precisely duplicating them in the sum channel.

Attached is a schematic for a sum-channel-processor circuit that compensates for bandwidth limitations in the 525CH itself. The location of this circuit in the sum channel is not critical, but it must be included somewhere in the sum channel before transmission. When building this circuit, it is important to keep its overall gain at precisely unity so that stereo separation will not suffer. Low impedances should be used to minimize capacitive effects of the op-amps.

6. Operating Characteristics

All 525CHs are aligned and burned-in. Each is ready to be plugged into broadcast or test equipment and used with no further adjustment. Following is a brief discussion to answer the question: "Is my card operating correctly?"

A few simple concepts can be presented that generally describe the card's operation. With no input signal, the wideband compressor will boost the equivalent input noise while the spectral compressor and fixed preemphasis will selectively boost the high frequencies. The resulting output of the card will look quite noisy, with the greatest spectral content at approximately the cutoff frequency of the 10- or 15-kHz LPF.

A low-frequency single-tone input will capture the attention of the wideband rms-level detector and will be processed with a 2:1 compression factor (i.e., a 2-dB input change will cause a 1-dB output change). The spectral compressor, which will boost high frequencies (and noise), will not be greatly affected by low-frequency single tones, and so the output will be a noisy low-frequency tone. In fact, a noisy input sinewave or one that has significant amounts of distortion components (often the case with digital function generators) will look noisier and more distorted at the 525CH output because of the drastic amounts of preemphasis. The decoder, of course, will restore this "strange" signal to its original condition, whether clean, noisy, or distorted.

As the input frequency is increased, the output will begin to look less and less noisy, as the spectral-compressor rms detector begins to see more and more of the high-frequency signal and reduces the amount of variable preemphasis. By 2 to 3 kHz, the output will become cleaner.

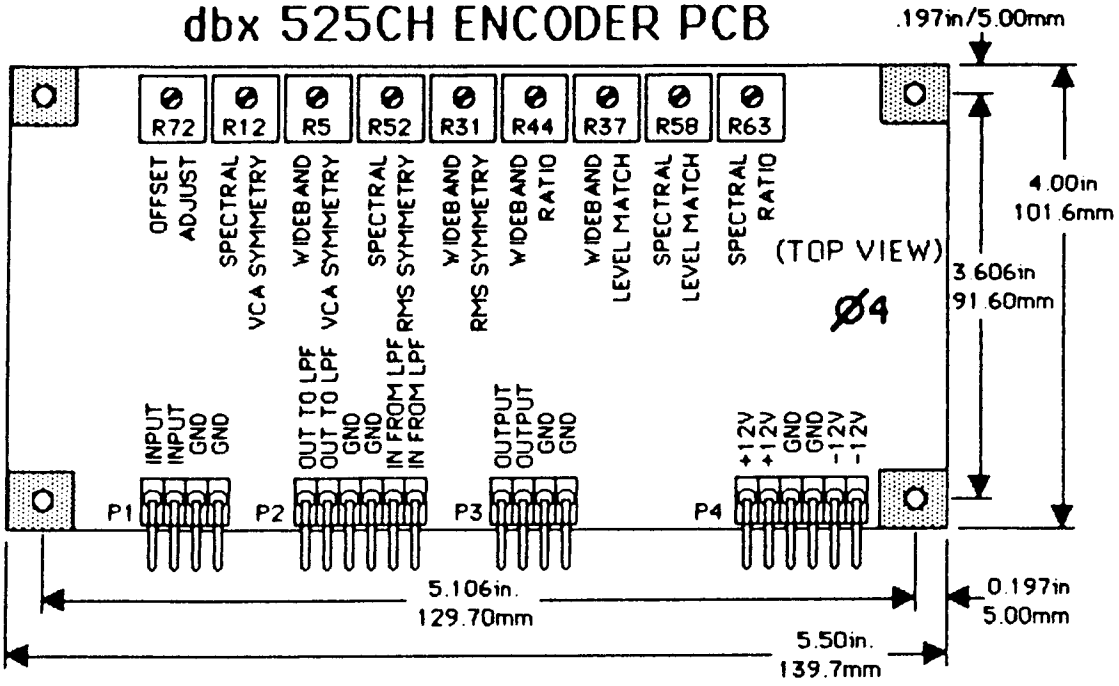
A consequence of the 525CH's preemphasis and the finite amount of time required by its rms detectors to respond to sharp increases in input level is that input signals with transient information will often cause the compressor to overshoot (though usually well below 100% modulation). Transients will actually become sharper and briefer, so that if there is any clipping action, less energy will be removed from the processed signal than would be removed from the original signal.

Two approximate alignment points can be used to make a rough check of the compressor:

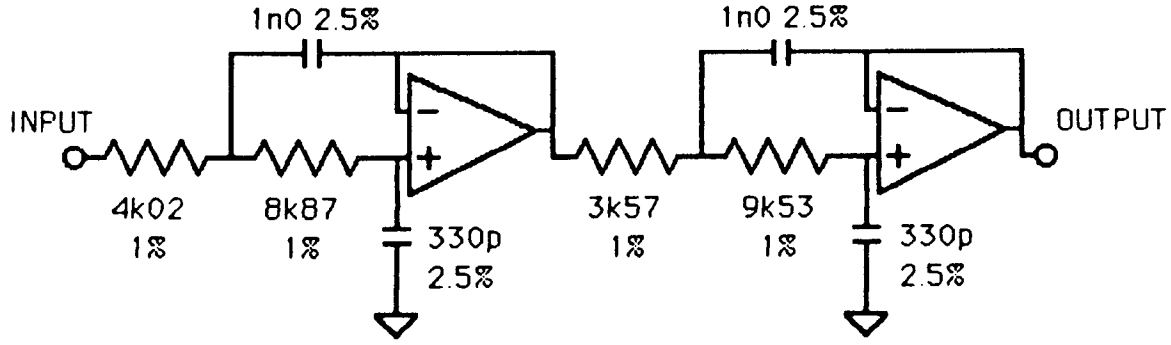
Input Frequency	Input Level	Desired Output Level
300 Hz	500 mVRMS	500 mVRMS
8 kHz	136 mVRMS	1.13 VRMS

For further information about the dbx 525CH card, please contact dbx OEM Products Division.

dbx 525CH ENCODER PCB



dbx 525CH ENCODER SUM-CHANNEL PROCESSOR



Phase-4 Compensation

[FOR USE WITH 260585-01 PC-BOARDS]

Seperation: >36dB, 50Hz to 8kHz, 30dB @ 15kHz

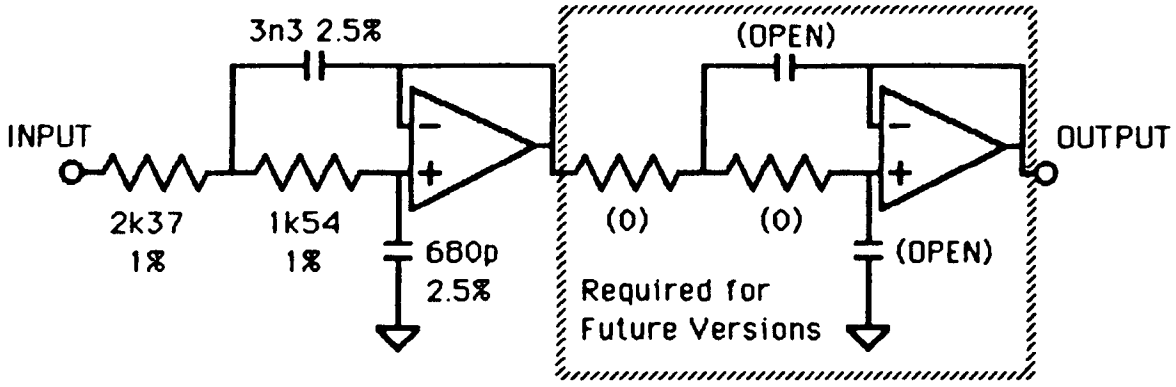
NOTE: OPAMPS ARE NE5532 OR EQUIVALENT

Operating Level:

100% Modulation = 10.000 V_{p-p}

525CH4 013185

525CH dbx-TV Encoder
Sum-Channel Processors
[PHASE 3M & PHASE 4]

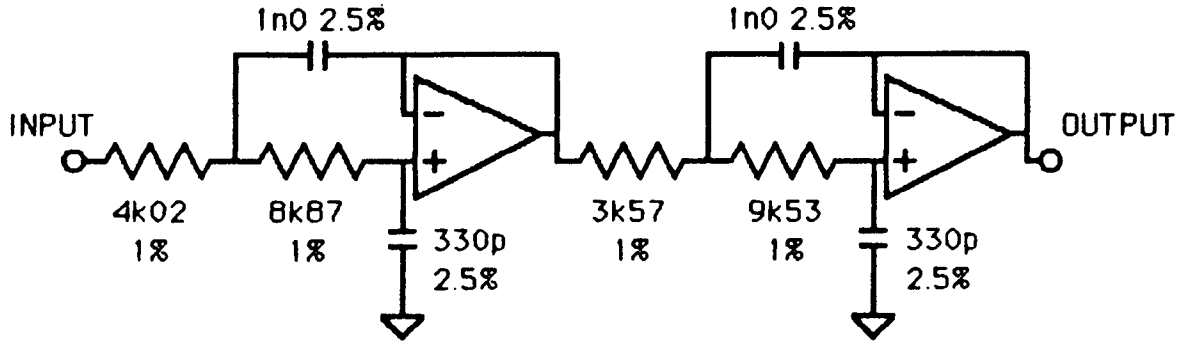


Phase-3M Compensation

[FOR USE WITH 260585-00 PC-BOARDS]

Separation: >36dB, 50Hz to 8kHz; 30dB @ 15kHz

NOTE: OPAMPS ARE NE5532 OR EQUIVALENT



Phase-4 Compensation

[FOR USE WITH 260585-01 PC-BOARDS]

Separation: >36dB, 50Hz to 8kHz; 30dB @ 15kHz

NOTE: OPAMPS ARE NE5532 OR EQUIVALENT

Most cards shipped to the U.S. are Phase 3M. Phase 4 cards will ship beginning January 1985. Because dbx may revise the 525 cards periodically for improved performance, the component values shown are subject to change. As improvements are made, dbx will endeavor to maintain this sum-channel processor topology. Please be aware that changes may be required.

525CH3M/4 120384

Parts List

Because special or subtle characteristics of certain components have been exploited to produce an elegant design at a reasonable cost, *it is unwise to make substitutions for listed parts.* Consult with Orban Customer Service (see page 5-13) if the parts list indicates that a part is specially selected, or that realignment is required when the part is replaced.

Orban maintains an inventory of tested, exact replacement parts that can be supplied quickly at nominal cost. Spare parts kits are also available. When ordering parts from Orban, please be ready to supply the following information:

Orban part number
Reference designator (e.g., C3, R78, IC14)
Description of part
Model, serial, and M number of unit — see rear-panel label
(not all units have M numbers)

Parts are listed by card or assembly (except for widely used common parts, which are described on the following page), and the parts on each card are grouped by type. See the assembly drawings for locations of components.

To facilitate future maintenance, we have used components from well-established manufacturers with worldwide distribution whenever possible. The abbreviations used for manufacturers are listed on page 6-54, along with their USA headquarters addresses.

Widely used common parts:

Diodes: Unless specified by reference designator in the following, all signal diodes are 1N4148 (Orban part number 22101-000). This is a silicon, small-signal diode with ultra-fast recovery and high conductance. It may also be replaced with 1N914 (BAY-61 in Europe). (BV: 75V min. @ I_r = 5V, I_r: 25nA max. @ V_r = 20V, V_f: 1.0V max. @ I_f = 100mA t_{rr}: 4ns max.)

Resistors: Resistors should only be replaced with the same style and with the *exact* value marked on the resistor body. If the value marking is not legible, check the schematic or contact Orban Customer Service (see page 5-13). Performance and stability will be compromised if you do not use exact replacements.

Unless specified by reference designator in the following, the resistors in this unit are:

Metal film resistors with conformally-coated bodies, value identified with five color bands or printed on body; rated 1/8-watt @ 70°C, with a ±1% tolerance, and with a temperature coefficient of 100 PPM/°C; Orban part numbers 20038-xxx through 20045-xxx, USA Military Specification MIL-R-10509 style RN55D, manufactured by R-Ohm (CRB-1/4FX), TRW/IRC, Beyschlag, Dale, Corning, Matsushita.

Carbon film resistors with conformally-coated bodies, value identified with four color bands; rated 1/4-watt @ 70°C, with a tolerance of ±5%; Orban part numbers 20001-xxx, manufactured by R-Ohm (R-25), Piher, Beyschlag, Dale, Phillips, Spectrol, Matsushita.

Carbon composition resistors with molded phenolic bodies, value identified with four color bands; rated 1/4-watt for the 0.09 × 0.25-inch (2.3 × 6.4mm) size, and rated 1/8 watt for the 0.14 × 0.375-inch (3.6 × 9.5mm) size @ 70° C, with a tolerance of ±5%; Orban part numbers 2001x-xxx, USA Military Specification MIL-R-11 style RC-07 or RC-20, manufactured by Allen-Bradley, TRW/IRC, Matsushita.

Cermet trimmer resistors with 3/8-inch (9mm) square bodies, value printed on side; rated 1/2-watt @ 70°C, with a tolerance of ±10%, and a temperature coefficient of 100 PPM/°C; Orban part numbers 20510-xxx and 20511-xxx, manufactured by Beckman (72P, 68W-series), Spectrol, Matsushita.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
CARD #2						
Capacitors						
C1,11	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C2,12	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C3,13	Capacitor Pair, Polypro.; 0.022uF	28602-002	ORB			3
C4,14	Capacitor Pair, Mica; 33pF	28603-001	ORB			3
C5,15	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C6,16	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C7,17	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C8,18	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C9,19	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C10,20	Capacitor Pair, Polypro.; 0.01uF	28602-001	ORB			3
C21,22	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C23-32	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Integrated Circuits						
IC1-9	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
Resistors						
R3	Resistor Network, 8 POS., 2K	20201-503	BEK	698-3-R2KD		
R4,25	Resistor Pair, MF; 4.32K	28521-020	ORB			3
R5,30	Resistor Pair, MF; 1.18K	28521-010	ORB			3
R6,31	Resistor Pair, MF; 2.15K	28521-015	ORB			3
R7,32	Resistor Pair, MF; 16.9K	28521-013	ORB			3
R8,33	Resistor Pair, MF; 6.04K	28521-009	ORB			3
R9,34	Resistor Pair, MF; 348 OHM	28521-012	ORB			3
R10,35	Resistor Pair, MF; 6.04K	28521-009	ORB			3
R11	Resistor Network, 8 POS., 2K	20201-503	BEK	698-3-R2KD		
R12,37	Resistor Pair, MF; 10.20K	28521-022	ORB			3
R13,38	Resistor Pair, MF; 2.61K	28521-018	ORB			3
R14,39	Resistor Pair, MF; 5.11K	28521-021	ORB			3
R15,40	Resistor Pair, MF; 4.22K	28521-019	ORB			3
R16,41	Resistor Pair, MF; 2.43K	28521-016	ORB			3
R17,42	Resistor Pair, MF; 2.10K	28521-014	ORB			3
R18,43	Resistor Pair, MF; 2.55K	28521-017	ORB			3
R19,44	Resistor Pair, MF; 2.43K	28521-016	ORB			3
R20,45	Resistor Pair, MF; 1.27K	28521-011	ORB			3
R21	Resistor Network, 8 POS., 20K	20201-501	BEK	698-3-R20KD		
R24	Resistor Network, 8 POS., 2K	20201-503	BEK	698-3-R2KD		
R26-29	Not Used	---				
R36	Resistor Network, 8 POS., 2K	20201-503	BEK	698-3-R2KD		

FOOTNOTES:
(1) See last page for abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A
Card 2 - Capacitors, IC's, Resistors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
	Integrated Circuits					
IC1-8	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
IC9	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC10-13	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
	Resistors					
R5	Resistor Set, MF; 2.00K	28520-002	ORB			3
R9	Resistor Set, MF; 2.00K	28520-002	ORB			3
R12	Resistor, MF, 1/2W, 25ppM, 4.64K; 1%	20071-464	ROHM	CRB-14		
R13	Resistor Set, MF; 2.00K	28520-002	ORB			3
R16	Resistor, MF, 1/2W, 25ppM, 931 OHM; 1%	20070-931	ROHM	CRB-14		
R19	Resistor, MF, 1/2W, 25ppM, 3.74K; 1%	20071-374	ROHM	CRB-14		
R20	Resistor Set, MF; 2.00K	28520-002	ORB			3
R21	Resistor, MF, 1/2W, 25ppM, 1.10K; 1%	20071-110	ROHM	CRB-14		
R25	Resistor Set, MF; 2.00K	28520-002	ORB			3
R40-50	Not Used	---				
R55	Resistor Set, MF; 2.00K	28520-002	ORB			3
R59	Resistor Set, MF; 2.00K	28520-002	ORB			3
R62	Resistor, MF, 1/2W, 25ppM, 4.64K; 1%	20071-464	ROHM	CRB-14		
R63	Resistor Set, MF; 2.00K	28520-002	ORB			3
R66	Resistor, MF, 1/2W, 25ppM, 931 OHM; 1%	20070-931	ROHM	CRB-14		
R69	Resistor, MF, 1/2W, 25ppM, 3.74K; 1%	20071-374	ROHM	CRB-14		
R70	Resistor Set, MF; 2.00K	28520-002	ORB			3
R71	Resistor, MF, 1/2W, 25ppM, 1.10K; 1%	20071-110	ROHM	CRB-14		
R75	Resistor Set, MF; 2.00K	28520-002	ORB			3
	Selected Components					
C13-18	To be determined during test	---	ORB			3
	Switches					
S1	Switch, Toggle, Min., DPDT	26041-202	CK	7201SYA		
	Transistors					
Q1	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	
Q2	Transistor, JFET/N	23406-101	NAT	J113	SIL	

FOOTNOTES:
(1) See last page for abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A
Card 2 - IC's, Resistors, Selected Components, Switches, Transistors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
CARD #3						
Capacitors						
C1	Polypropylene, 50V, 1%; 0.015uF	21701-315	NOB	CQ15P1H153FPP	WES	
C2	Mica, 500V, 5%; 2700pF	21024-227	CD	CD19-FD272J03	SAN	
C3,4	Polypropylene, 50V, 1%; 0.01uF	21701-310	NOB	CQ15P1H103FPP	WES	
C5,6	Polystyrene, 100V, 1%; 0.0047uF	21510-247	ORB			Special Tolerance
C7-9	Polypropylene, 50V, 1%; 0.01uF	21701-310	NOB	CQ15P1H103FPP	WES	
C10	Mica, 500V, 1%; 160pF	21018-116	CD	CD15-FD161F03	SAN	
C11	Polypropylene, 50V, 1%; 0.015uF	21701-315	NOB	CQ15P1H153FPP	WES	
C12	Mica, 500V, 5%; 2700pF	21024-227	CD	CD19-FD272J03	SAN	
C13,14	Polypropylene, 50V, 1%; 0.01uF	21701-310	NOB	CQ15P1H103FPP	WES	
C15,16	Polystyrene, 100V, 1%; 0.0047uF	21510-247	ORB			Special Tolerance
C17-19	Polypropylene, 50V, 1%; 0.01uF	21701-310	NOB	CQ15P1H103FPP	WES	
C20	Mica, 500V, 1%; 160pF	21018-116	CD	CD15-FD161F03	SAN	
C21,22	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C23-30	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Integrated Circuits						
IC1-10	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
Resistors						
R7	Resistor Set, MF; 2.00K	28520-002	ORB			3
R10	Resistor, MF, 1/2W, 25ppM, 1.37K; 1%	20071-137	ROHM	CRB-14		
R11	Resistor Set, MF; 2.00K	28520-002	ORB			3
R12	Resistor, MF, 1/2W, 25ppM, 3.16K; 1%	20071-316	ROHM	CRB-14		
R15	Resistor Set, MF; 2.00K	28520-002	ORB			3
R32	Resistor Set, MF; 2.00K	28520-002	ORB			3
R35	Resistor, MF, 1/2W, 25ppM, 1.37K; 1%	20071-137	ROHM	CRB-14		
R36	Resistor Set, MF; 2.00K	28520-002	ORB			3
R37	Resistor, MF, 1/2W, 25ppM, 3.16K; 1%	20071-316	ROHM	CRB-14		
R40	Resistor Set, MF; 2.00K	28520-002	ORB			3
Transistors						
Q1,2	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	
Q3	Transistor, JFET/N	23406-101	NAT	J113	SIL	
Q4,5	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	
Q6	Transistor, JFET/N	23406-101	NAT	J113	SIL	

FOOTNOTES:
(1) See last page for abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A
Card 3 - Capacitors, IC's, Resistors, Transistors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
CARD #4						
Capacitors						
C1	See Selected Components	---				
C2,3	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C4,5	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C6,7	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C8,9	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Integrated Circuits						
IC1	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
IC2	D.C. Regulator, 12V Positive	24309-901	MOT	MC78M12CT		
IC3	D.C. Regulator, 12V Negative	24310-901	MOT	MC79M12CT		
Miscellaneous						
A1	Encoder Card, DBX, Phase IV	30925-000-xx*	ORB			*Add suffix printed on part
Resistors						
R1	See Selected Components	---				
Selected Components						
C1/R1	Matched Set, Capacitor/Resistor	28701-000	ORB			3
CARD #5						
Capacitors						
C1-5	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C6-9	Polystyrene, 100V, 1%; 0.0047uF	21510-247	ORB			Special Tolerance
C10-12	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C13-18	See Selected Components	---				
C19-50	Not Used	---				
C51-55	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C56-59	Polystyrene, 100V, 1%; 0.0047uF	21510-247	ORB			Special Tolerance
C60-62	Polypropylene, 50V, 1%; 4700pF	21701-247	NOB	CQ15P1H472FPP	WES	
C63,64	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C65-82	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	

FOOTNOTES:
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(2) No Alternate Vendors known at publication
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(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS
OPTMOD-TV Model 8185A
Card 4 - Capacitors, IC's, Misc., Resistors, Selected Components
Card 5 - Capacitors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
CARD #6						
Capacitors						
C1-5	See Selected Components	---				
C6,7	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C8-11	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C12,13	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C14,15	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Integrated Circuits						
IC1	Linear, Dual Opamp	24206-202	TI	TL072CP	MOT	
IC2,3	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
IC4	D.C. Regulator, 12V Positive	24309-901	MOT	MC78M12CT		
IC5	D.C. Regulator, 12V Negative	24310-901	MOT	MC79M12CT		
Miscellaneous						
A1	Decoder Card, DBX, Phase IV	30930-000-xx*	ORB			*Add suffix printed on part
Resistors						
R1	See Selected Components	---				
R5	Resistor Network, 8 POS., 20K	20201-501	BEK	698-3-R20KD		
R8	Not Used	---				
R9	See Selected Components	---				
Selected Components						
C1/R1	Matched Set, Capacitor/Resistor	28701-000	ORB			3
C2-4	To be determined during test	---	ORB			3
C5/R9	Matched Set, Capacitor/Resistor	28701-000	ORB			3
Switches						
S1	Switch, Toggle, Min., DPDT	26041-202	CK	7201SYA		

FOOTNOTES:
(1) See last page for abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A
Card 6 - Capacitors, IC's, Misc., Resistors, Selected Components, Switches

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
CARD #7						
Capacitors						
C1	Not Used	---				
C2	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE	
C3	Mica, 500V, 1%; 680pF	21022-168	CD	CD19-FD681F03	SAN	
C4	Mica, 500V, +1/2pF -1/2pF; 22pF	21017-022	CD	CD15-CD220D03	SAN	
C5	Mica, 500V, 1%; 1000pF	21022-210	CD	CD19-FD102F03	SAN	
C6	Mica, 500V, 1%; 390pF	21018-139	CD	CD15-FD391F03	SAN	
C7	Mica, 500V, 1%; 51pF	21018-051	CD	CD15-ED510F03	SAN	
C8	Mica, 500V, 1%; 560pF	21022-156	CD	CD19-FD561F03	SAN	
C9	Mica, 500V, 1%; 82pF	21018-082	CD	CD15-ED820F03	SAN	
C10,11	Mica, 500V, 1%; 1000pF	21022-210	CD	CD19-FD102F03	SAN	
C12	Mica, 500V, +1/2pF -1/2pF; 22pF	21017-022	CD	CD15-CD220D03	SAN	
C13	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE	
C14,15	Not Used	---				
C16	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C17,18	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C19,20	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C21	Polypropylene, 50V, 2.5%; 0.01uF	21702-310	NOB	CQ15P1H103GPP	WES	
C22,23	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C24-47	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Diodes						
CR1-6	Diode, Signal, Hot Carrier	22102-001	HP	HP5082-2800		
Inductors						
L1	Variable Inductor	29705-006	ORB			
L2	Variable Inductor	29705-007	ORB			

FOOTNOTES:
(1) See last page for abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A
Card 7 - Capacitors, Diodes, Inductors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS(1)	NOTES
Integrated Circuits						
IC1	D.C. Regulator, 5V Negative	24308-901	NAT	LM79M05CP		
IC2	D.C. Regulator, 5V Positive	24307-901	NAT	LM78M05CP		
IC3	Digital, NAND Gate	24501-302	RCA	CD4011BE	MOT	
IC4	Digital, Up-Counter	24508-302	RCA	CD4520BE		
IC5	Digital, PROM	44001-000-01	ORB			
IC6	Digital, Flip-Flop	24553-302	NAT	74HC374	TI,RCA	
IC7,8	Triple 2-Channel Analog Multiplexer	24562-302	NAT	MM74HC4053		
IC9	Linear, Dual Opamp	24202-202	RAY	RC4558NB	MOT,FSC	
IC10-12	Optoisolator, NPN	25003-000	SIE	SFH-601-1		
IC13	Digital, NAND Gate	24501-302	RCA	CD4011BE	MOT	
IC14	Digital, XOR Gate	24504-302	RCA	CD4030BE	SIG	
IC15	Linear, Single Opamp	24013-202	TI	TL071CP		
IC16,17	Linear, Single Opamp	24008-202	TI	LM318N	NAT	
IC18	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC19	Linear, Single Opamp	24008-202	TI	LM318N	NAT	
IC20	Power Buffer	24707-102	LT	LT1010CH		
IC21	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC22	Linear, Dual Opamp	24207-202	SIG	NE5532N	TI,EXR	
Resistors						
R9	Not Used	---				
R10a,b	Resistor Pair, MF; 10.0K	28520-004	ORB			3
R11	Not Used	---				
R14	Trimpot, Cermet, 20 Turn; 1K	20512-210	BEK	89PR1K	BRN	
R30a,b	Resistor Pair, MF; 2.00K	28520-002	ORB			3
R31	Not Used	---				
R42	Trimpot, Cermet, 20 Turn; 25K	20512-325	BEK	89PR25K	BRN	
Switches						
S1	Switch, Rotary, Min., 2P4T	26203-000	ELSW	73-9005		
S2	Switch, Toggle, Min., SPDT	26041-102	CK	7101SYA		
Transistors						
Q1	Transistor, JFET/N	23403-101	NAT	J111	INS	
Q2,3	Not Used	---				
Q4	Transistor, Signal, PNP	23002-101	MOT	2N4402	FSC	
Q5	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A
Card 7 - IC's, Resistors, Switches, Transistors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
CARD #8						
Capacitors						
C1	Mica, 500V, +1/2pF -1/2pF; 3pF	21017-003	CD	CD15-CD030D03	SAN	
C2	Polypropylene, 50V, 2.5%; 0.01uF	21702-310	NOB	CQ15P1H103GPP	WES	
C3	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE	
C4	Mica, 500V, +1/2pF -1/2 pF; 33pF	21017-033	CD	CD15-CD330D03	SAN	
C5	Met. Polyester, 100V, 10%; 0.47uF	21441-447	WES	60F474K100	WIM,SIE	
C6	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE	
C7	Ceramic Disc, 50V, 20%; 0.01uF	21107-310	CRL	UK50-103	MUR	
C8	Mica, 500V, 5%; 470pF	21024-147	CD	CD19-FD471J03	SAN	
C9	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE	
C10	Met. Polyester, 100V, 10%; 0.47uF	21441-447	WES	60F474K100	WIM,SIE	
C11	Polypropylene, 50V, 2.5%; 0.01uF	21702-310	NOB	CQ15P1H103GPP	WES	
C12	Alum., Radial, 50V; 47uF	21208-647	SPR	502D 476G050CD1C	PAN	
C13	Polypropylene, 50V, 2.5%; 0.01uF	21702-310	NOB	CQ15P1H103GPP	WES	
C14	Mica, 500V, 5%; 100pF	21020-110	CD	CD15-FD101J03	SAN	
C15	Tantalum, 35V, 10%; 4.7uF	21307-547	SPR	196D 475X9035JA1	MANY	
C16	Met. Polyester, 100V, 10%; 0.1uF	21441-410	WIM	MKS-4100V5.0.1	WES,SIE	
C17	Mica, 500V, 1%; 1000pF	21022-210	CD	CD19-FD102F03	SAN	
C18	Mica, 500V, 1%; 150pF	21018-115	CD	CD15-FD151F03	SAN	
C19	Tantalum, 35V, 10%; 0.22uF	21307-422	SPR	196D 224X9035HA1	MANY	
C20	Met. Polyester, 100V, 5%; 0.047uF	21440-347	WES	60C 473J250	SIE,WIM	
C21,22	Alum., Radial, 25V; 100uF	21206-710	PAN	ECE-A1EV101S		
C23-32	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
Diodes						
CR1,2	Diode, Signal, Hot Carrier	22102-001	HP	HP5082-2800		
CR8	Diode, Volt. Reference, -1.2V	22081-112	NAT	LM385		
Integrated Circuits						
IC1	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC2	Digital, XOR Gate	24504-302	RCA	CD4030BE	SIG	
IC3	Digital, Quad 2-Input NAND	24509-302	RCA	CD4093BE		
IC4	Digital, Up-Counter	24508-302	RCA	CD4520BE		
IC5	Digital, Timer	24706-202	INS	ICM7555IPA		
IC6	Linear, Single Opamp	24011-205	RCA	CA3080E		
IC7	Linear, Single Opamp	24009-202	NAT	LF356N		
IC8	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC9	Digital, Phase Locked Loop	24507-302	RCA	CD4046BE		
IC10	Digital, Dual Flip-Flop	24502-302	RCA	CD4013BE		
IC11	Linear, Dual Opamp	24209-202	NAT	LF412CN		

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A
Card 8 - Capacitors, Diodes, IC's

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS(1)	NOTES
	Miscellaneous					
K1	Relay, Dip, 15V, 1xA	28022-011	PB	JWD-107-7		
	Resistors					
R48	Trimpot, Cermet, 20 Turn; 1K	20512-210	BEK	89PR1K	BRN	
	Switches					
S1	Switch, Toggle, Min., DPDT	26041-202	CK	7201SYA		
	Transistors					
Q1	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	
Q2	Transistor, Signal, PNP	23002-101	MOT	2N4402	FSC	
Q3,4	Transistor, Signal, PNP	23001-101	MOT	2N4125	FSC	
	CHASSIS (FRONT PANEL)					
	Diodes					
DS1-4	LED, Green	25104-000	GI	MV-5253		
	Meters					
M1	Meter, VU, Brown/Buff	28002-007	DIX	330T	HOYT	
	Switches					
S1	Switch, Toggle, Min., SPDT	26044-101	CK	7105P3		
S2	Switch, Toggle, Min., SPDT	26041-103	CK	7101		
	CHASSIS (POWER SUPPLY)					
	Capacitors					
C101,102	Alum., Electrolytic, 40V; 5000uF	21250-850	CD	FAH-5000-40-A2	MAL	
C103,104	Ceramic Disc, 50V, 20%; 0.05uF	21107-350	CRL	UK50-503	MUR	
C105-107	Ceramic, Feed-thru, 1000pF	21118-210	ERE	2404-000	MUR	
	Diodes					
CR101-104	Diode, Rectifier, 400V, 3A	22203-400	MOT	MR504		

FOOTNOTES:
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SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS
OPTIMOD-TV Model 8185A
Card 8 - Misc., Resistors, Switches, Transistors
Chassis Front Panel
Chassis Power Supply - Capacitors, Diodes

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
	Inductors					
L101,102	Inductor, RF Choke, 7uH	29501-004	OHM	Z-50	(2)	
	Miscellaneous					
F101	Fuse, 3AG, Slo-Blo, 1/2A	28004-150	LFE	313.500	BUS	
T101	Transformer, Power; 38VCT, 46VA	55002-000	ORB			
	Switches					
S101	Switch, Rocker, Power, DPST	26003-001	MAR	1802-0111		
S102	Switch, Slide, Mains voltage selector	26140-000	SW	EPSI-SLI		
CHASSIS (REAR PANEL)						
	Capacitors					
C1-18	Ceramic, Feed-thru, 1000pF	21118-210	ERE	2404-000	MUR	
C19	Ceramic Disc, 1KV, 10%; 0.001uF	21112-210	CRL	DD-102	MUR	
	Inductors					
L1-6	Inductor, RF Choke, 7uH	29501-004	OHM	Z-50	(2)	
	Miscellaneous					
NONE	Filter, Line, 3 Amp.	28015-000	COR	3EF1		
	Switches					
NONE	Switch, Slide, DPDT (Gold)	26106-000	CW	GF326-0149		Special Plating
INPUT FILTER ASSEMBLY						
	Inductors					
L1-6	Inductor, RF Choke, 1.2mH	29503-000	MIL	73F123AF		
L7	Inductor, RF Choke, 7uH	29501-004	OHM	Z-50	(2)	

FOOTNOTES:
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(2) No Alternate Vendors known at publication
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(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS
OPTIMOD-TV Model 8185A
Chassis Power Supply - Inductors, Misc., Switches
Chassis Rear Panel
Imput Filter Assembly - Inductors

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
METER RESISTOR BOARD						
Capacitors						
C1,2	Polypropylene, 50V, 1%; 0.01uF	21701-310	NOB	CQ15P1H103FPP	WES	
C3-6	Monolythic Ceramic, 50V, 20%; 0.1uF	21123-410	SPR	1C25 Z5U104M050B	KEM	
C7	Mica, 500V, +1/2pF -1/2pF; 22pF	21017-022	CD	CD15-CD220D03	SAN	
Diodes						
DS1	LED, Green	25104-000	GI	MV-5253		
Integrated Circuits						
IC1	Linear, Dual Opamp	24209-202	NAT	LF412CN		
IC2	Linear, Dual Opamp	24211-202	MOT	MC34082P		
Resistors						
R24	Trimpot, Cermet; 1K	20509-210	BEK	72XR1K	BRN	
Switches						
S1	Switch, Rotary, 1P12T	26078-306	CTS	212-Series		
Transistors						
Q1-5	Transistor, Signal, NPN	23202-101	MOT	2N4400	FSC	
OTHER						
Miscellaneous						
NONE	Line Cord, CEE	28102-002	BEL	17500	MANY	
NONE	PCB Extender Board Assy	30705-000	ORB			

FOOTNOTES:
(1) See last page for abbreviations
(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A

Meter Risistor - Capacitors, Diodes, IC's, Resistors, Switches, Transistors, Misc.

REF DES	DESCRIPTION	ORBAN P/N	VEN (1)	VENDOR P/N	ALTERNATE VENDORS (1)	NOTES
POWER SUPPLY BOARD						
Capacitors						
C108	Tantalum, 10V, 10%; 33uF	21303-633	SPR	196D 336X9010KE3	MANY	
C109	Mica, 500V, 5%; 470pF	21024-147	CD	CD19-FD471J03	SAN	
C110	Not Used	---				
C111,112	Alum., Radial, 50V; 47uF	21208-647	SPR	502D 476G050CD1C	PAN	
C113	Mica, 500V, 5%; 100pF	21020-110	CD	CD15-FD101J03	SAN	
C114	Met. Polyester, 100V, 10%; 0.01uF	21441-310	WES	60C 103K630	SIE, WIM	
C114	Polyester, 100V, 10%; 0.01uF	21401-310	SPR	225P 10391WD3	PAN,PAK	
Diodes						
CR105,106	Diode, Rectifier, 400V, 1A	22201-400	MOT	1N4004	MANY	
VR101,102	Diode, Zener, 5W; 16V, 5%	22005-160	MOT	1N5353B	MANY	
Integrated Circuits						
IC101	D.C. Regulator	24301-302	NAT	LM723CN		
IC102	Linear, Single Opamp	24003-202	NAT	LM301AN	TI,RCA	
Miscellaneous						
F102,103	Fuse, Pico, 1A, Axial	28011-210	LFE	275.001	BUS	
Resistors						
R103,104	Resistor, Wirewound, 2W, 0.62 OHM; 5%	20028-862	IRC	BWF Series		
R106	Trimpot, Cermet, 18 Turn; 500 OHM	20508-150	BEK	68XR500	BRN	
R108,109	Resistor Set, MF; 20.5K	28521-008	ORB			3
Transistors						
Q101,102	Transistor, Power, NPN; TO-204MA	23601-501	RCA	2N3055	FSC	Located on Chassis Rear Panel
Q103,104	Transistor, Signal, PNP	23002-101	MOT	2N4402	FSC	

FOOTNOTES:
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(2) No Alternate Vendors known at publication
(3) Actual part is specially selected from part listed, consult Factory
(4) Realignment may be required if replaced, see Circuit Description and/or Alignment Instructions

SPECIFICATIONS AND SOURCES FOR REPLACEMENT PARTS

OPTIMOD-TV Model 8185A

Power Supply - Capacitors, Diodes, IC's, Misc., Resistors, Transistors

Vendor Codes

AB Allen-Bradley Co., Inc.
1201 South Second Street
Milwaukee, WI 53204

AD Analog Devices, Inc.
One Technology Way
PO BOX 9106
Norwood, MA 02062-9106

AM Amphenol Corporation
358 Fall Avenue
Wallingford, CT 06492

BEK Beckman Industrial Corporation
4141 Palm Street.
Fullerton, CA 92635-1025

BEL Belden Electronic Wire & Cable
PO BOX 1980
Richmond, IN 47374

BRN Bourns, Inc.
Resistive Components Group
1200 Columbia Avenue
Riverside, CA 92507

BUS Bussmann Division
Cooper Industries
PO BOX 14460
St. Louis, MO 63178

CD Cornell-Dubilier Elec.
Wayne Interchange Plaza 1
Wayne, NJ 07470

CH Cutler-Hammer
4201 N. 27th Street
Milwaukee, WI 53216

CK C & K Components, Inc.
15 Riverdale Avenue
Newton, MA 02158-1082

COR Corcom, Inc.
1600 Winchester Road
Libertyville, IL 60048

CRL See Mepco/Centralab

CTS CTS Corporation
905 North West Blvd.
Elkhart, IN 46514

CW CW Industries
130 James Way
Southampton, PA 18966

DIX Dixson, Inc.
PO BOX 1449
Grand Junction, CO 81502

ECI Electrocube
1710 South Del Mar Avenue
San Gabriel, CA 91776

ELSW Electroswitch
180 King Avenue
Weymouth, MA 02188

EMI Emico Inc.
123 North Main Street
Dublin, PA 18917

ERE Murata Erie North America
2200 Lake Park Drive
Smyrna, GA 30080

EXR Exar Corporation
750 Palomar Ave
PO BOX 3575
Sunnyvale, CA 94088

FSC Fairchild Camera & Instr. Corp.
464 Ellis Street
Mountain View, CA 94042

GI General Instruments
Optoelectronics Division
3400 Hillview Avenue
Palo Alto, CA 94304

HP Hewlett-Packard Co.
640 Page Mill Road
Palo Alto, CA 94304

INS Intersil, Inc.
10600 Ridgeview Court
Cupertino, CA 95014

IRC International Resistive Co., Inc.
PO BOX 1860
Boone, NC 28607

JEN Jensen Transformers, Inc.
10735 Burbank Blvd.
North Hollywood, CA 91601

KEY Keystone Electronics Corp.
49 Bleecker Street
New York, NY 10012

LFE Littelfuse
A Subsidiary of Tracor, Inc.
800 E. Northwest Hwy
Des Plaines, IL 60016

LT Linear Technology Corp.
1630 McCarthy Blvd.
Milpitas, CA 95035

LUMX Lumex Opto/Components Inc.
292 E. Hellen Road
Palatine, IL 60067

MAL Mallory Capacitor Co.
Emhart Electrical/Electronic Gr.
3029 East Washington Street
Indianapolis, IN 46206

MAR Marquardt Switches, Inc.
67 Albany Street
Cazenovia, NY 13035

ME Mepco/Centralab
A North American Philips Corp.
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404

MID Midland-Ross Corporation
NEL Unit/Midtex Division
357 Beloit Street
Burlington, WI 53105

MIL J.W. Miller Division
Bell Industries
19070 Reyes Avenue
Rancho Dominguez, CA 90224-5825

MOT Motorola Semiconductor
PO BOX 20912
Phoenix, AZ 85036

NAT National Semiconductor Corp.
2900 Semiconductor Drive
PO BOX 58090
Santa Clara, CA 95052-8090

NOB Noble U.S.A., Incorporated
5450 Meadowbrook Ct.
Rolling Meadows, IL 60008

OHM Ohmite Manufacturing Company
A North American Philips Corp.
3601 Howard Street
Skokie, IL 60076

ORB Orban
a division of AKG Acoustics, Inc.
645 Bryant Street
San Francisco, CA 94107

PAN Panasonic Industrial Company
One Panasonic Way
PO BOX 1503
Seacaucus, NJ 07094

PB Potter & Brumfield Division
A Siemens Co.
200 S. Richland Creek Dr.
Princeton, IN 47671-0001

RCA RCA Solid State Division
Route 202
Somerville, NJ 08876

ROHM Rohm Corporation
8 Whatney
Irvine, CA 92718

SAE Stanford Applied Engineering, Inc
340 Martin Avenue
Santa Clara, CA 95050

SAN Sangamo Weston Inc.
Capacitor Division
PO BOX 48400
Atlanta, GA 30362

SCH ITT Schadow
8081 Wallace Road
Eden Prairie, MN 55344

SIE Siemens Components Inc.
186 Wood Avenue South
Iselin, NJ 08830

SIG Signetics Corporation
A Sub. of US Philips Corp.
811 E. Arques
PO BOX 3409
Sunnyvale, CA 94088-3409

SPR Sprague Electric Co.
41 Hampden Road
PO BOX 9102
Mansfield, MA 02048-9102

SW Switchcraft
A Raytheon Company
5555 N. Elston Avenue
Chicago, IL 60630

TI Texas Instruments
PO BOX 655012
Dallas, TX 75265

TOS Toshiba America, Inc.
2441 Michelle Drive
Tustin, CA 92680

TRW TRW Electronic Components
Connector Division
1501 Morse Avenue
Elk Grove Village, IL 60007-57

VARO Varo Quality Semiconductor, Inc.
1000 North Shiloh Road
PO BOX 469013
Garland, TX 75046-9013

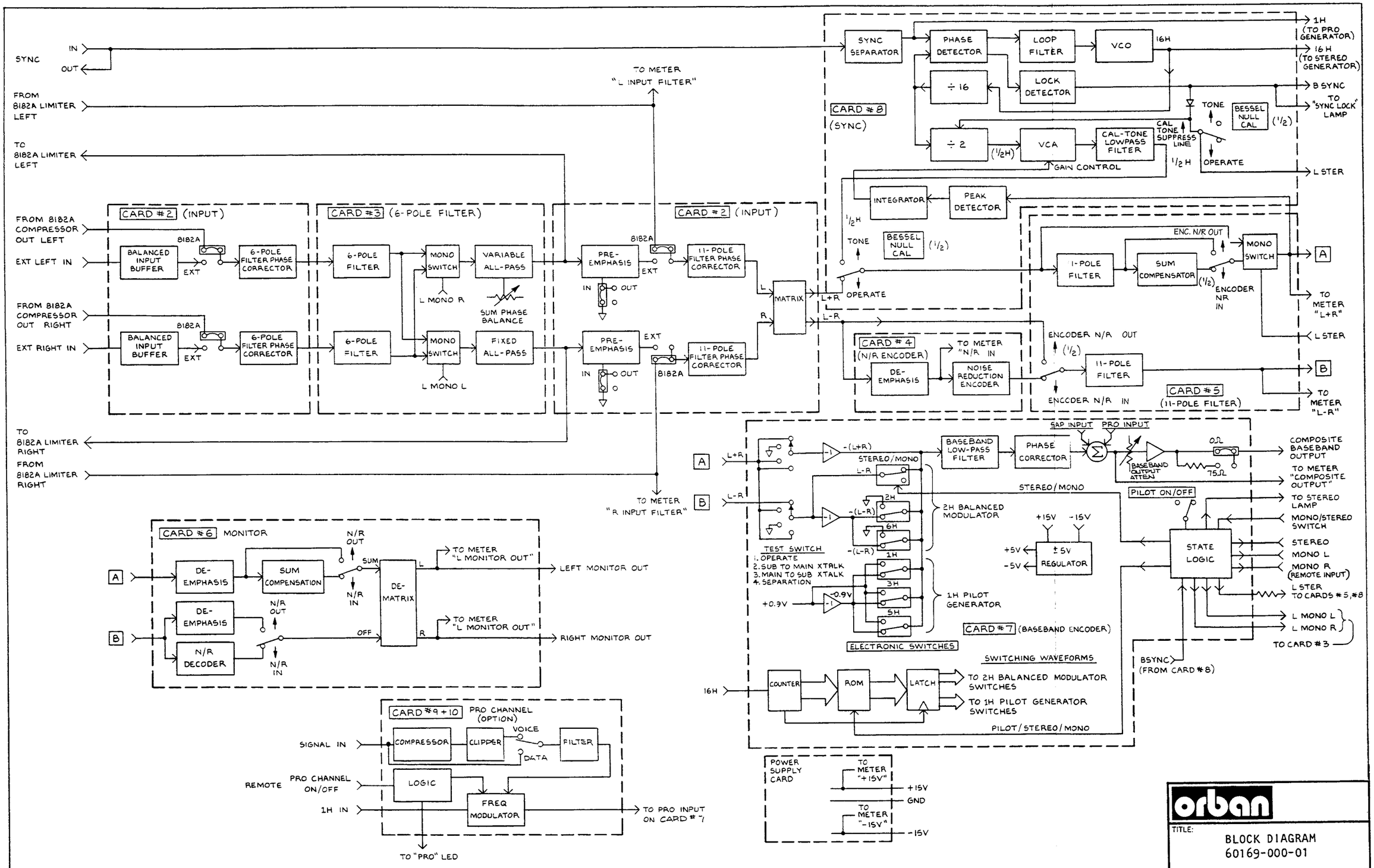
WES Westlake
5334 Sterling Ctr Drive
Westlake Village, CA 91361

WIM The Inter-Technical Group Inc.
Wima Division
PO BOX 23
Irvington, NY 10533

Schematics, Assembly Drawings

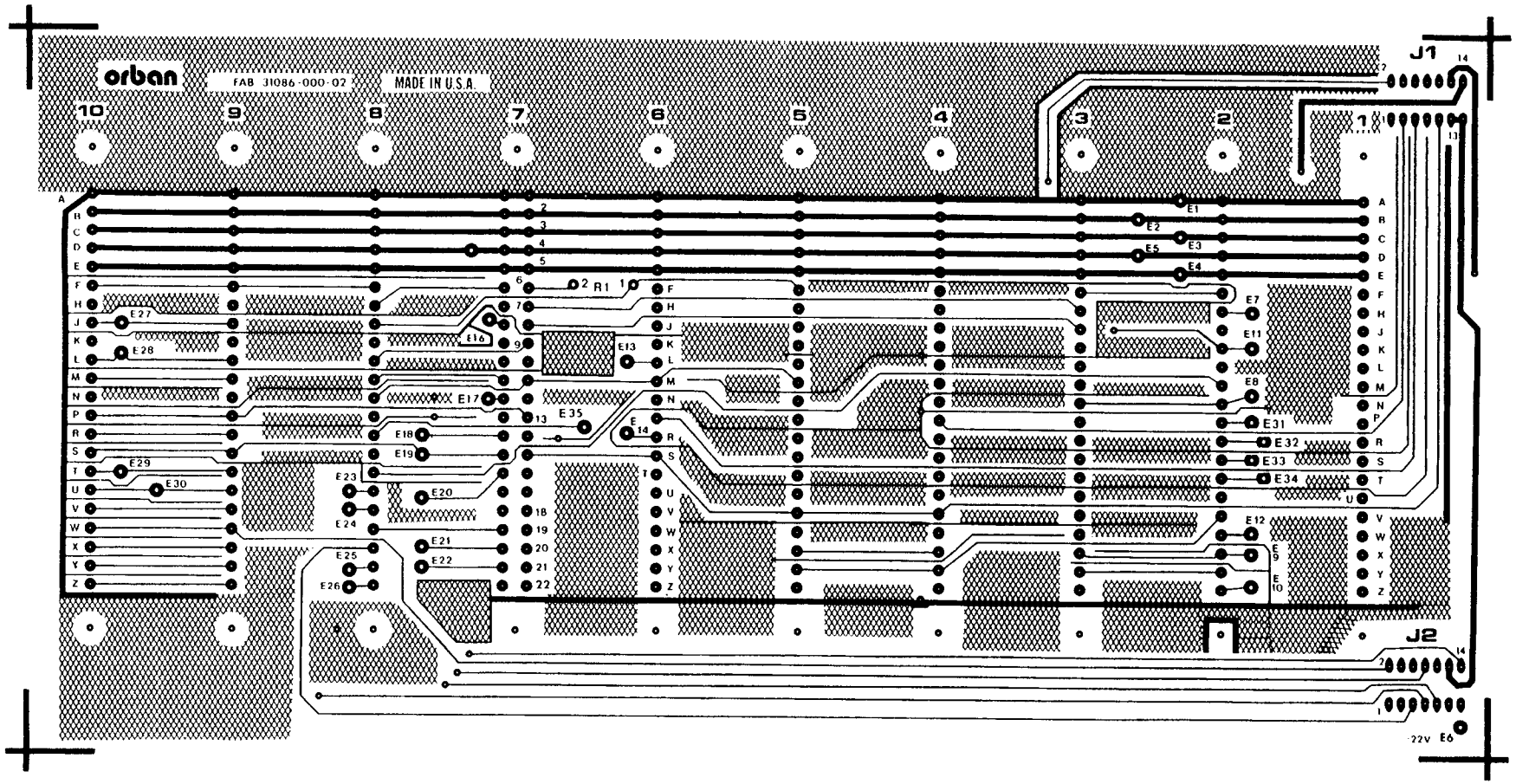
The following drawings are included in this manual:

These drawings reflect the actual construction of your unit as accurately as possible. Any differences between the drawings and your unit are almost undoubtedly due to product improvements or production changes since the publication of this manual. Major changes are described in addenda located at the front of this manual. If you intend to replace parts, please read page 6-41.

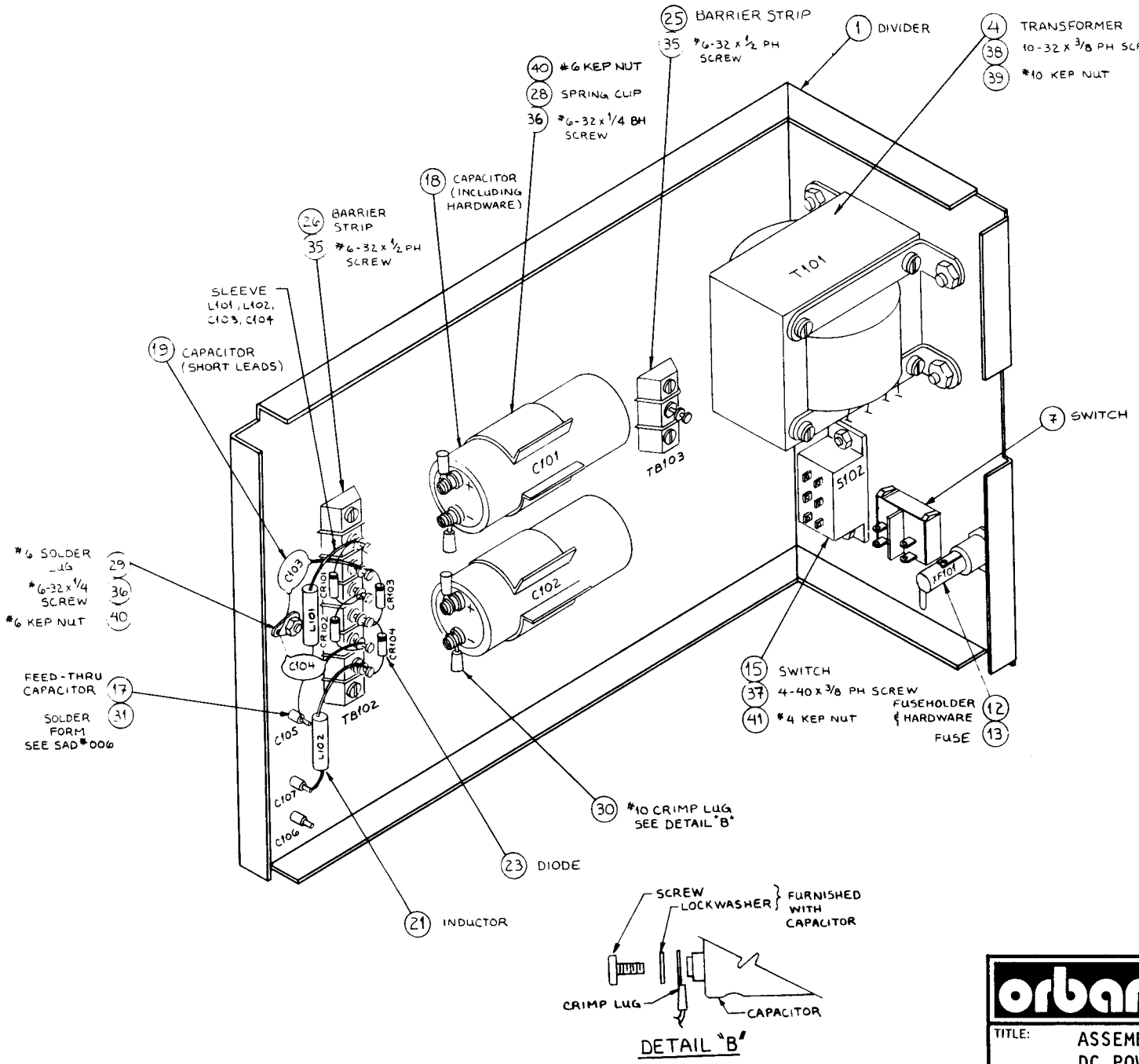


orban

TITLE:
BLOCK DIAGRAM
60169-000-01



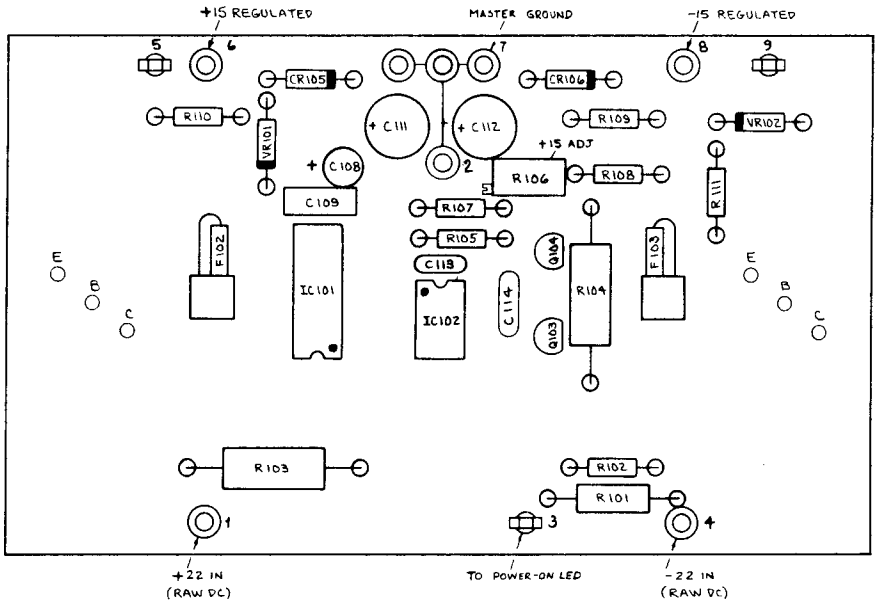
orban	
TITLE:	MOTHERBOARD 31087-000-02



DETAIL "B"

orban

TITLE: ASSEMBLY DRAWING
DC POWER SECTION
40017-000-07

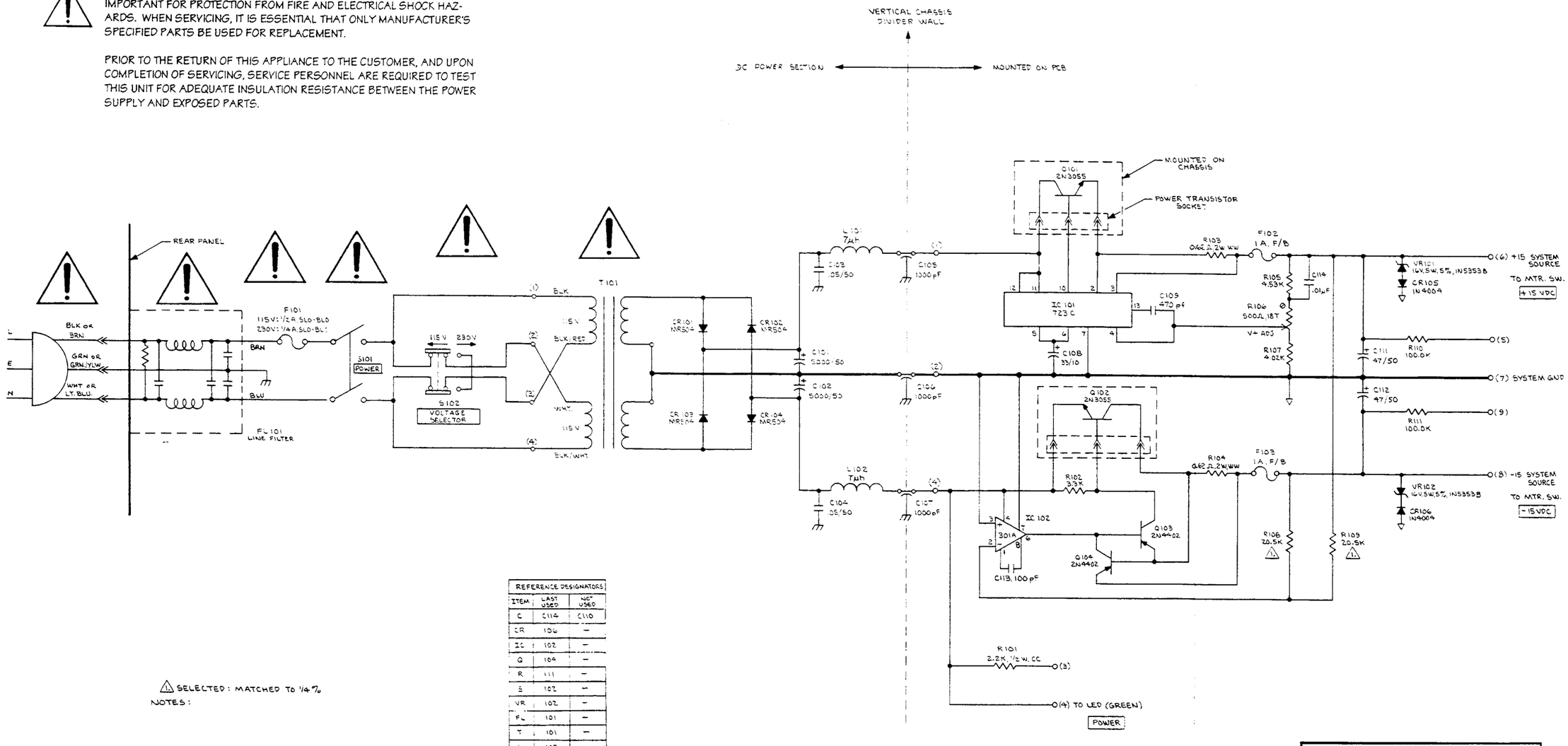


orban

TITLE: ASSEMBLY DRAWING
POWER SUPPLY
30310-000-07

⚠ COMPONENTS MARKED WITH THIS SYMBOL HAVE CRITICAL SPECIFICATIONS IMPORTANT FOR PROTECTION FROM FIRE AND ELECTRICAL SHOCK HAZARDS. WHEN SERVICING, IT IS ESSENTIAL THAT ONLY MANUFACTURER'S SPECIFIED PARTS BE USED FOR REPLACEMENT.

PRIOR TO THE RETURN OF THIS APPLIANCE TO THE CUSTOMER, AND UPON COMPLETION OF SERVICING, SERVICE PERSONNEL ARE REQUIRED TO TEST THIS UNIT FOR ADEQUATE INSULATION RESISTANCE BETWEEN THE POWER SUPPLY AND EXPOSED PARTS.



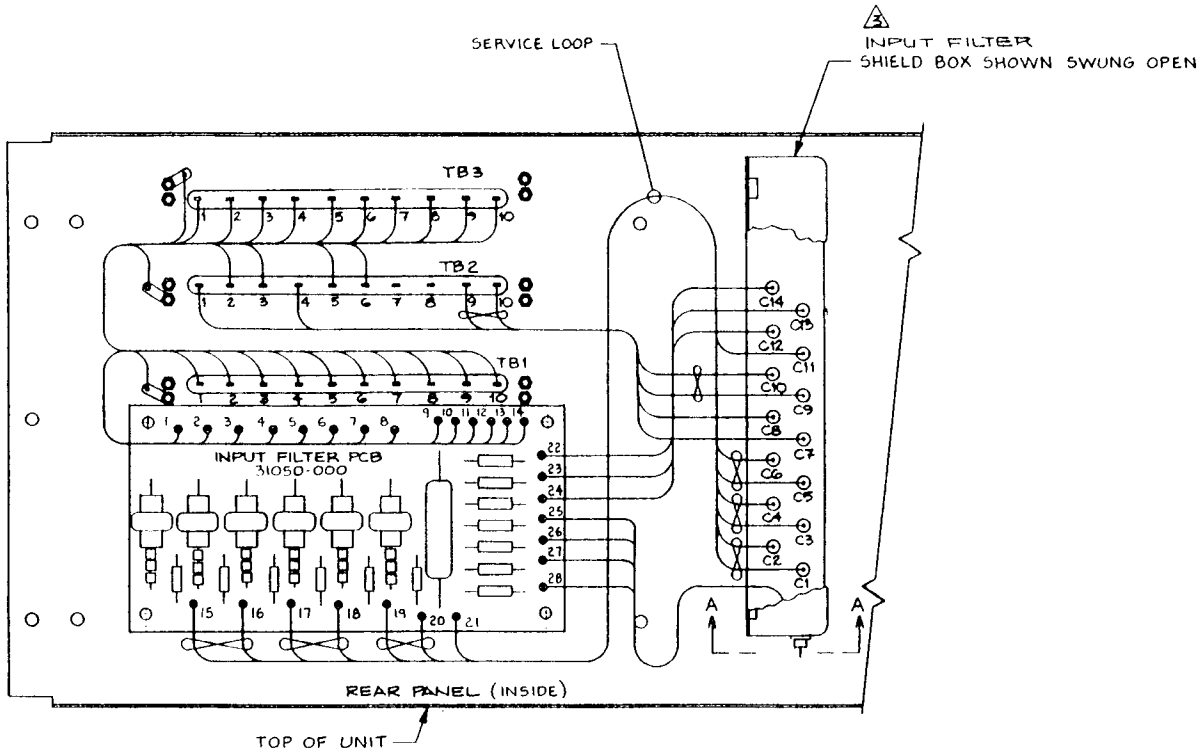
REFERENCE DESIGNATORS		
ITEM	LAST USED	NOT USED
C	C114	C110
CR	106	—
IC	102	—
Q	104	—
R	111	—
S	102	—
VR	102	—
FL	101	—
T	101	—
L	102	—
F	103	—

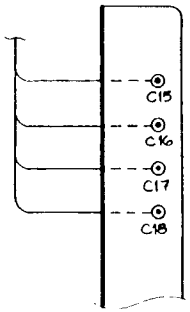
⚠1 SELECTED: MATCHED TO ¼%

NOTES:

orban

TITLE: SCHEMATIC
POWER SUPPLY
60021-000-08





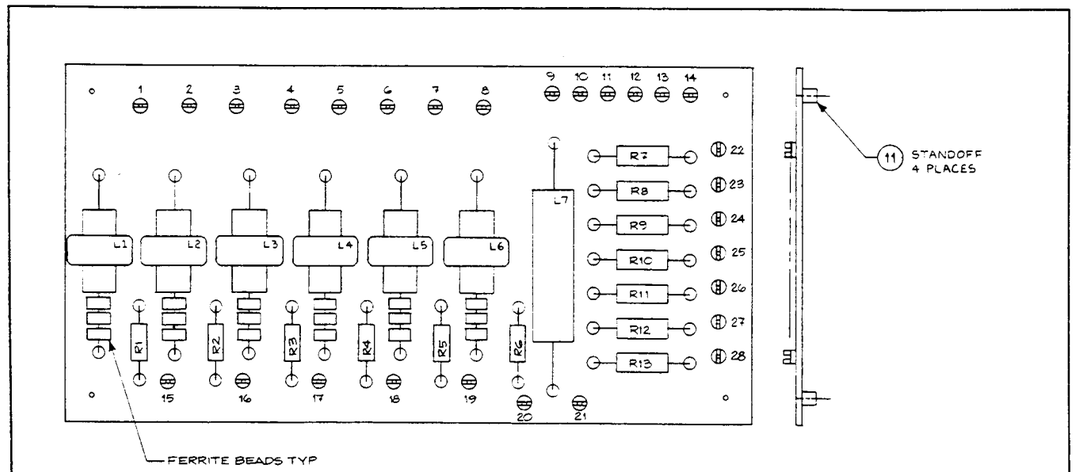
VIEW A-A

NOTES:

1. REF WIRE LIST 64030-000
2. ∞ MEANS TWISTED PAIR OF WIRES.
3. INPUT FILTER IS SHOWN ON ITS SIDE WITH A CUT-AWAY TO SHOW FEED THRU CAPACITORS AS THEY APPEAR ON INSIDE OF BOX.

orban

TITLE: WIRING DIAGRAM
INPUT FILTER
60163-000-01

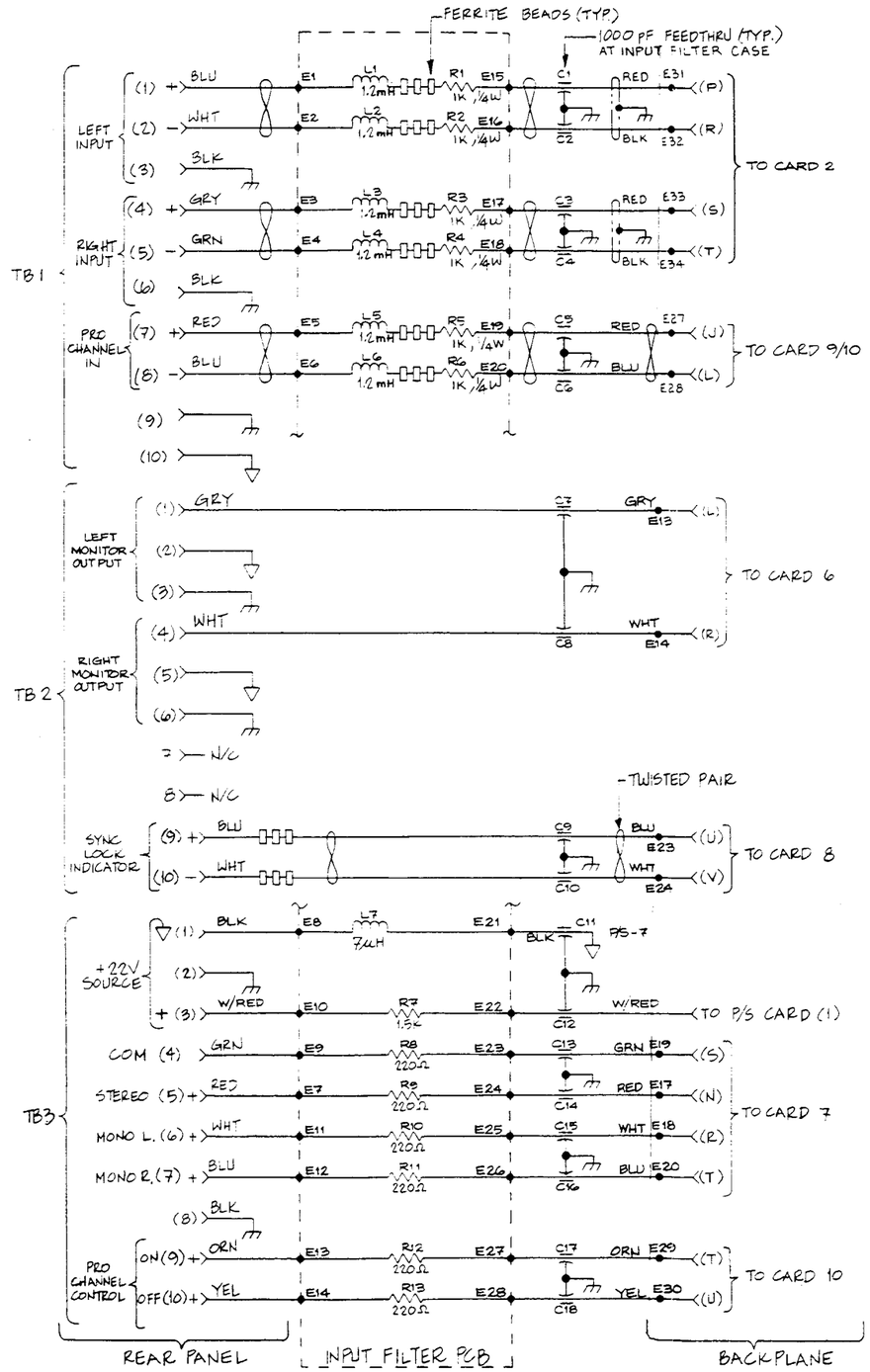


2. SOLDER ALL TERMINALS ON SOLDER SIDE BEFORE INSTALLING COMPONENTS (28 PLACES).
1. REFERENCE SCHEMATIC 61019-000

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban A Division of AKG Acoustics Inc.

TITLE: ASSEMBLY DRAWING
INPUT FILTER
31050-000-01



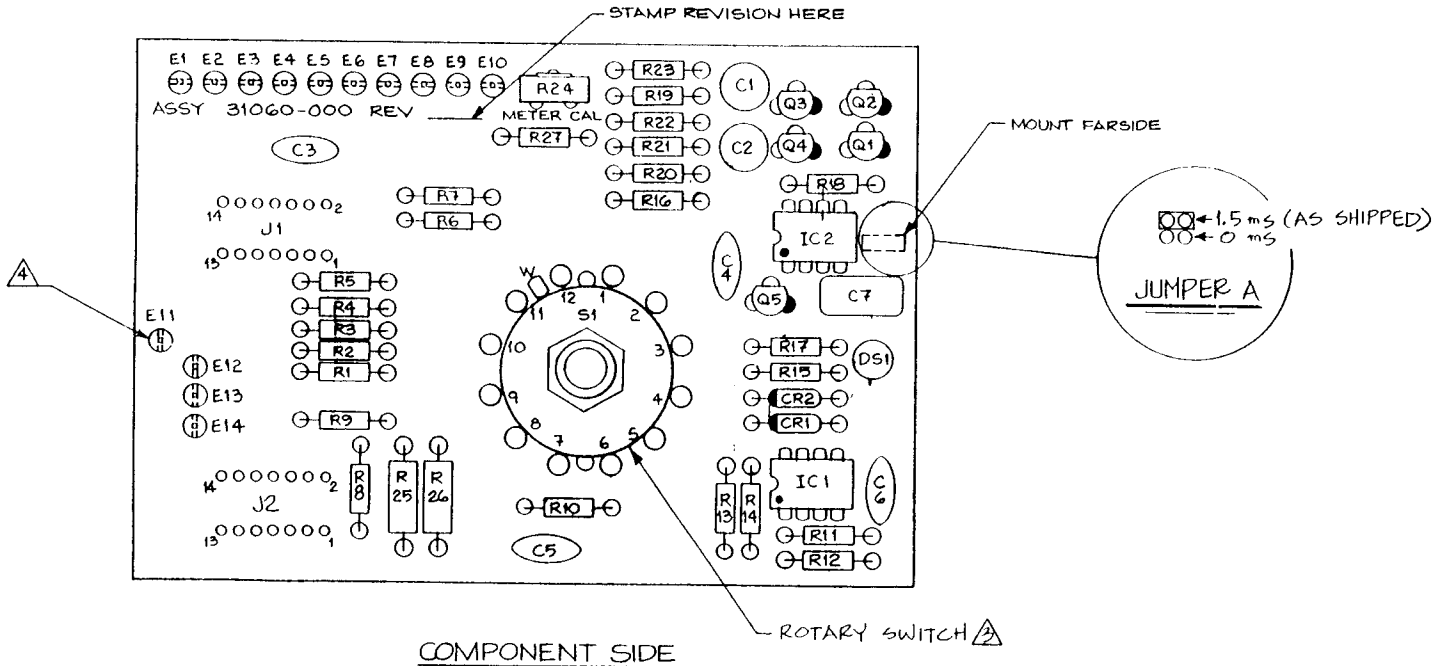
2. ALL CAPS ARE 1000pF FEEDTHRU SOLDERED TO CASE OF ASSEMBLY.
1. ALL RESISTORS ARE 1/2W, CC

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: SCHEMATIC
INPUT FILTER
61019-000-01

REF. DESIGNATORS		
ITEM	LAST USED	NOT USED
C	18	
R	13	
L	7	



COMPONENT SIDE

4 SOLDER ALL TERMINALS TO TRACES, 14 PLACES, FARSIDE

3 HAND INSTALL - DO NOT WASH MECHANISM.

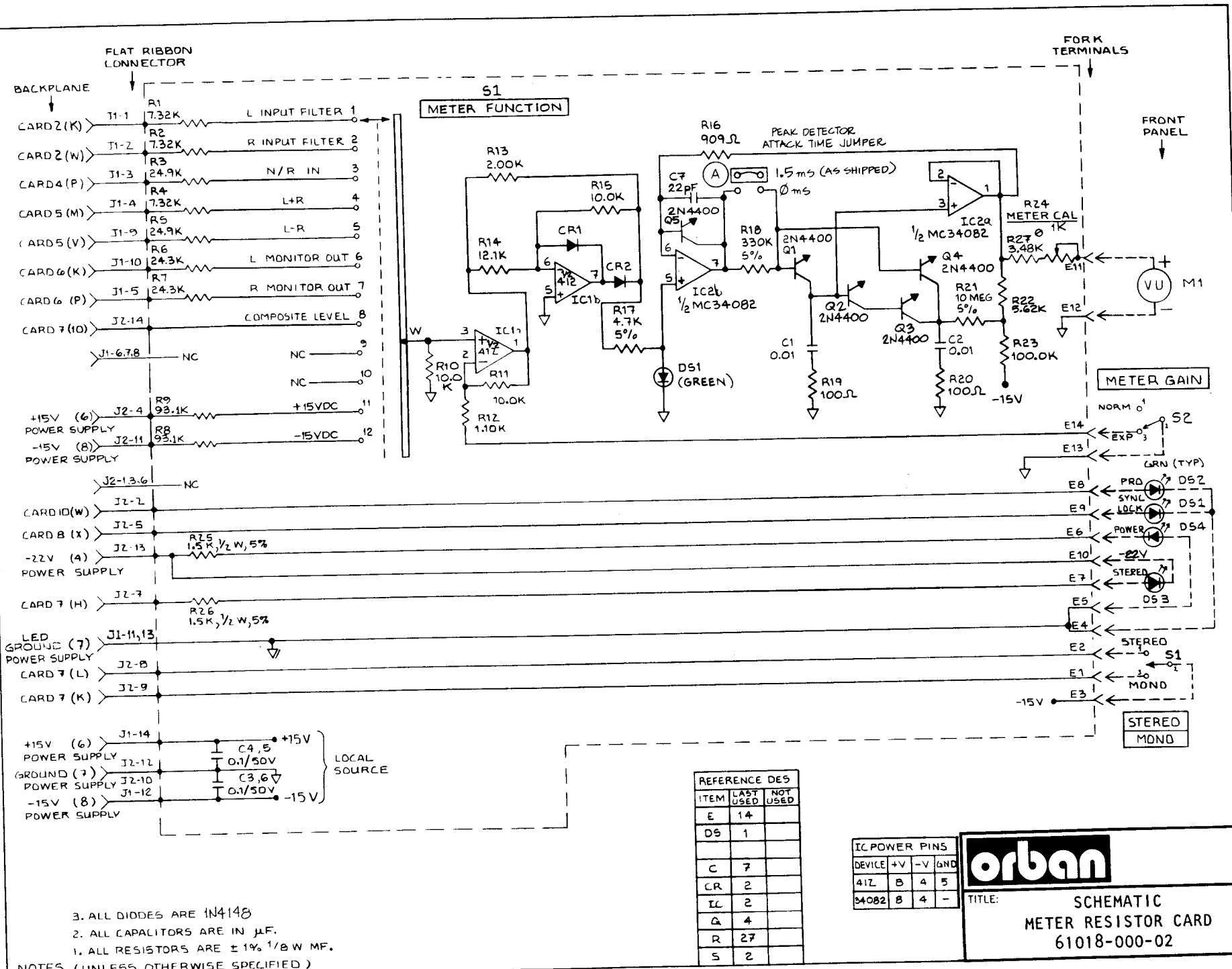
2. TIC MARKS INDICATE PIN #1 OF IC'S, PIN #1 OF CONNECTORS, CATHODE OF DIODES, EMITTER OF TRANSISTORS, PIN #1 OF SWITCH.

1. REFERENCE SCHEMATIC 61018-000

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: ASSEMBLY DRAWING
METER RESISTOR
31060-000-03

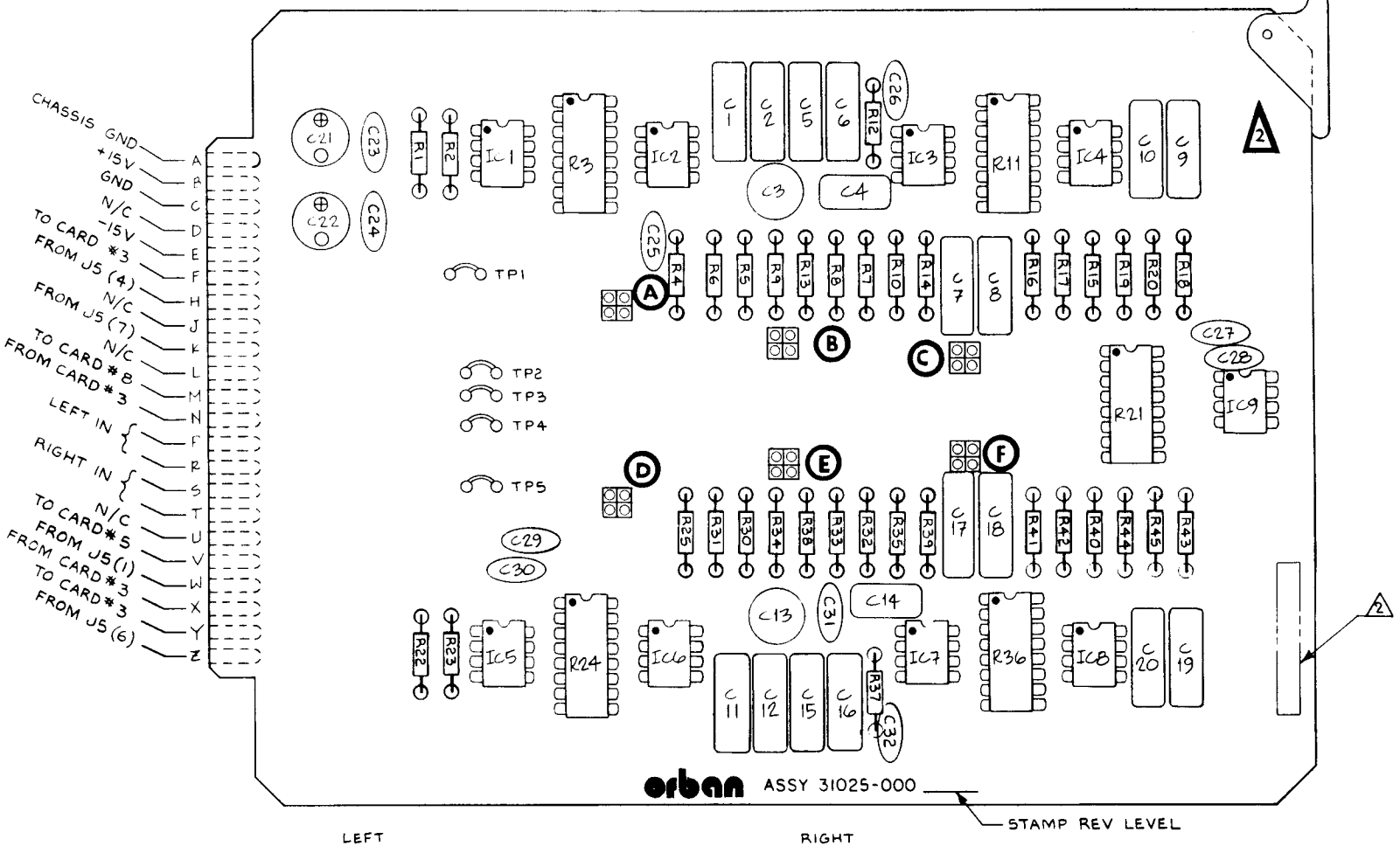


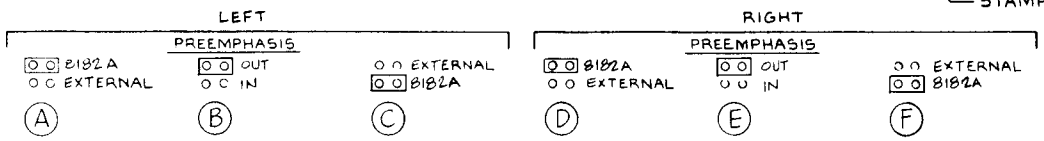
REFERENCE DES		
ITEM	LAST USED	NOT USED
E	14	
DS	1	
C	7	
CR	2	
IC	2	
Q	4	
R	27	
S	2	

IC POWER PINS			
DEVICE	+V	-V	GND
417	8	4	5
34082	8	4	-

orban

TITLE: SCHEMATIC
METER RESISTOR CARD
61018-000-02





PROCESSOR JUMPERS

(SHOWN AS SHIPPED)

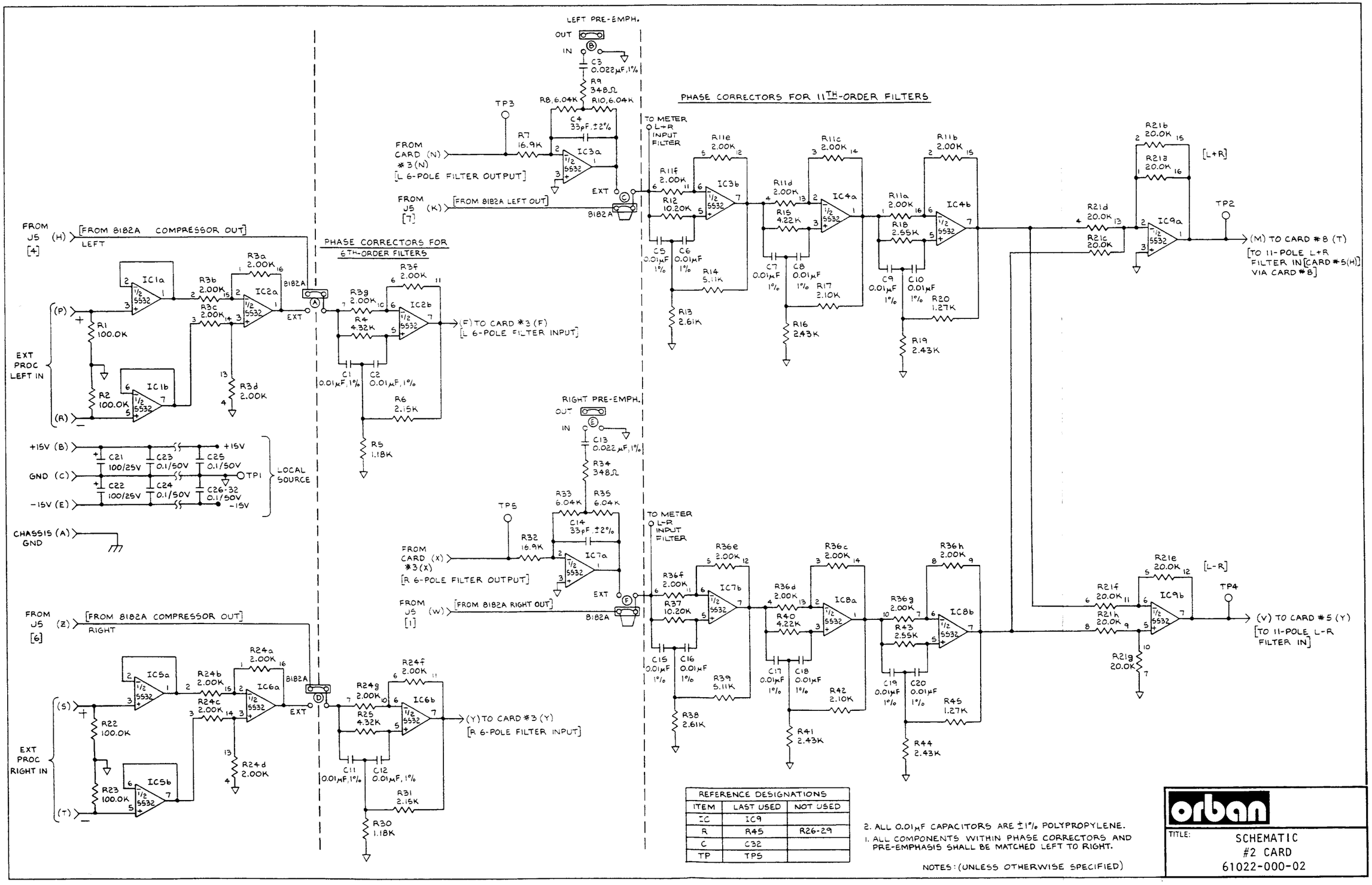
2 ADD SERIAL NUMBER PER SAD 014.

1. TIC MARKS INDICATE PIN 1 OF IC'S & RESISTOR NETWORKS

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: ASSEMBLY DRAWING
#2 CARD
31025-000-02



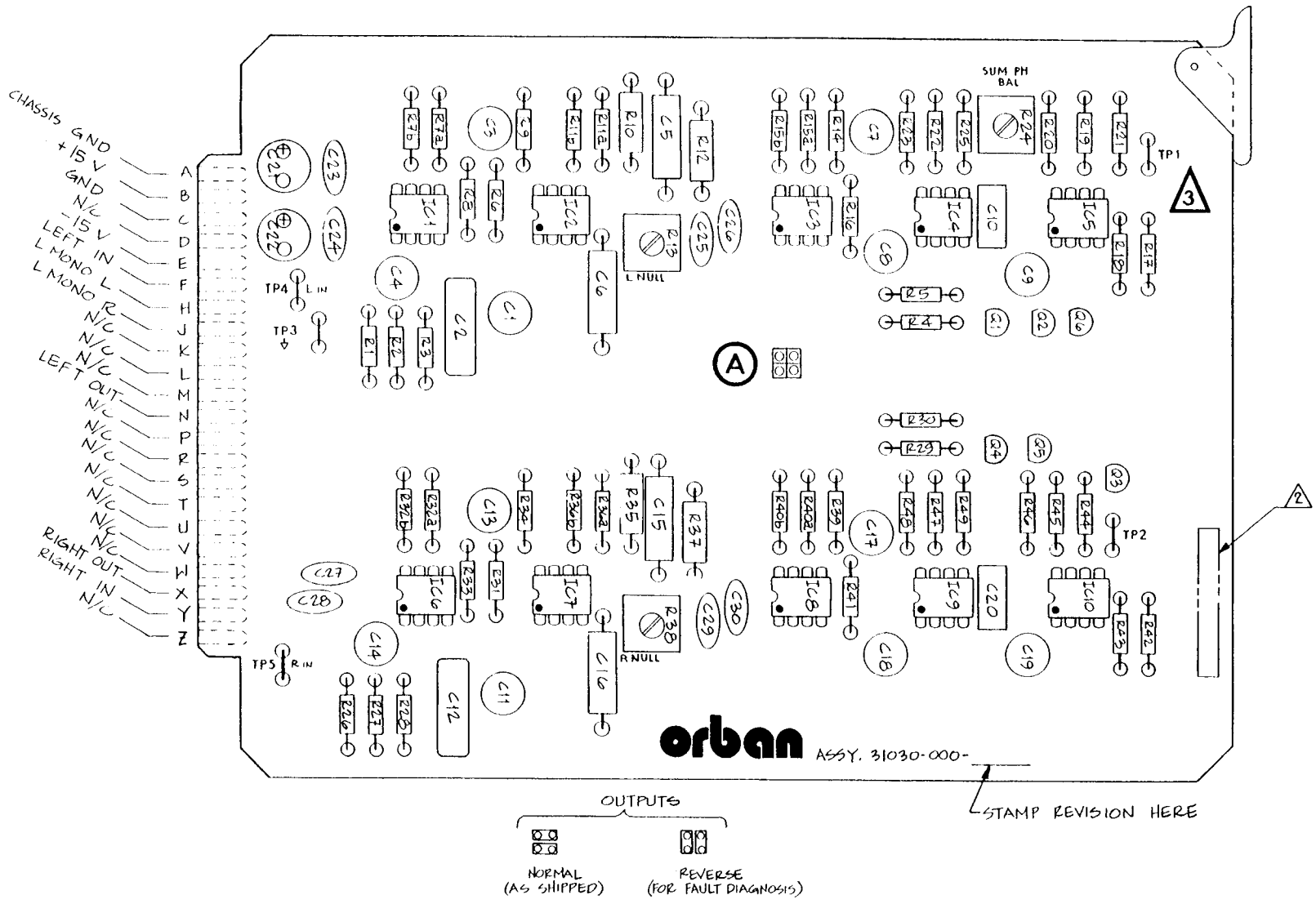
REFERENCE DESIGNATIONS		
ITEM	LAST USED	NOT USED
IC	IC9	
R	R45	R26-29
C	C32	
TP	TP5	

2. ALL 0.01µF CAPACITORS ARE ±1% POLYPROPYLENE.
1. ALL COMPONENTS WITHIN PHASE CORRECTORS AND PRE-EMPHASIS SHALL BE MATCHED LEFT TO RIGHT.

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: SCHEMATIC #2 CARD 61022-000-02



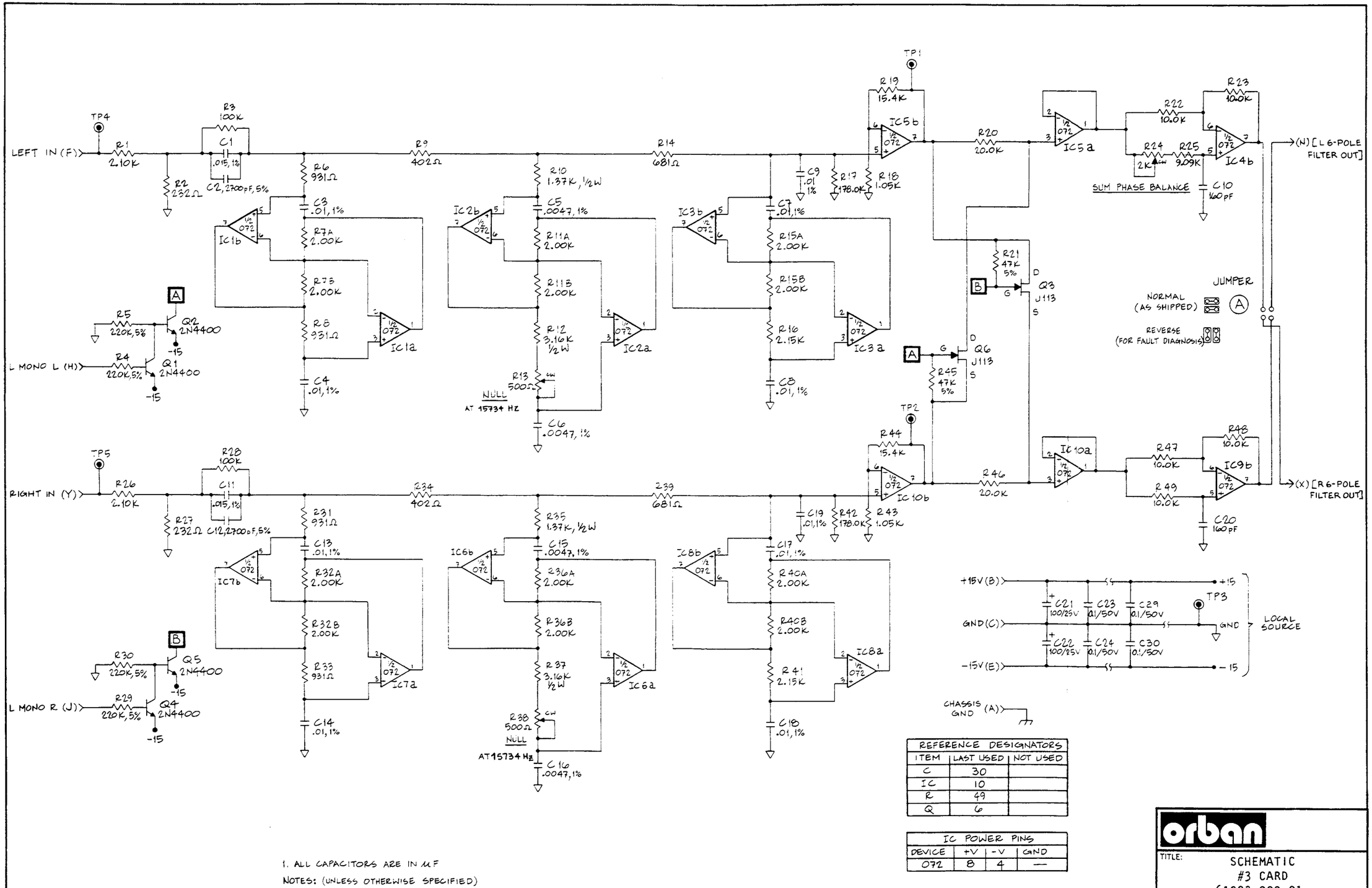
2 ADD SERIAL NUMBER PER SAD 014.

1. TIC MARKS INDICATE PIN 1 OF IC'S & POS. SIDE OF CAPS

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: ASSEMBLY DRAWING
#3 CARD
31030-000-02



REFERENCE DESIGNATORS		
ITEM	LAST USED	NOT USED
C	30	
IC	10	
R	49	
Q	6	

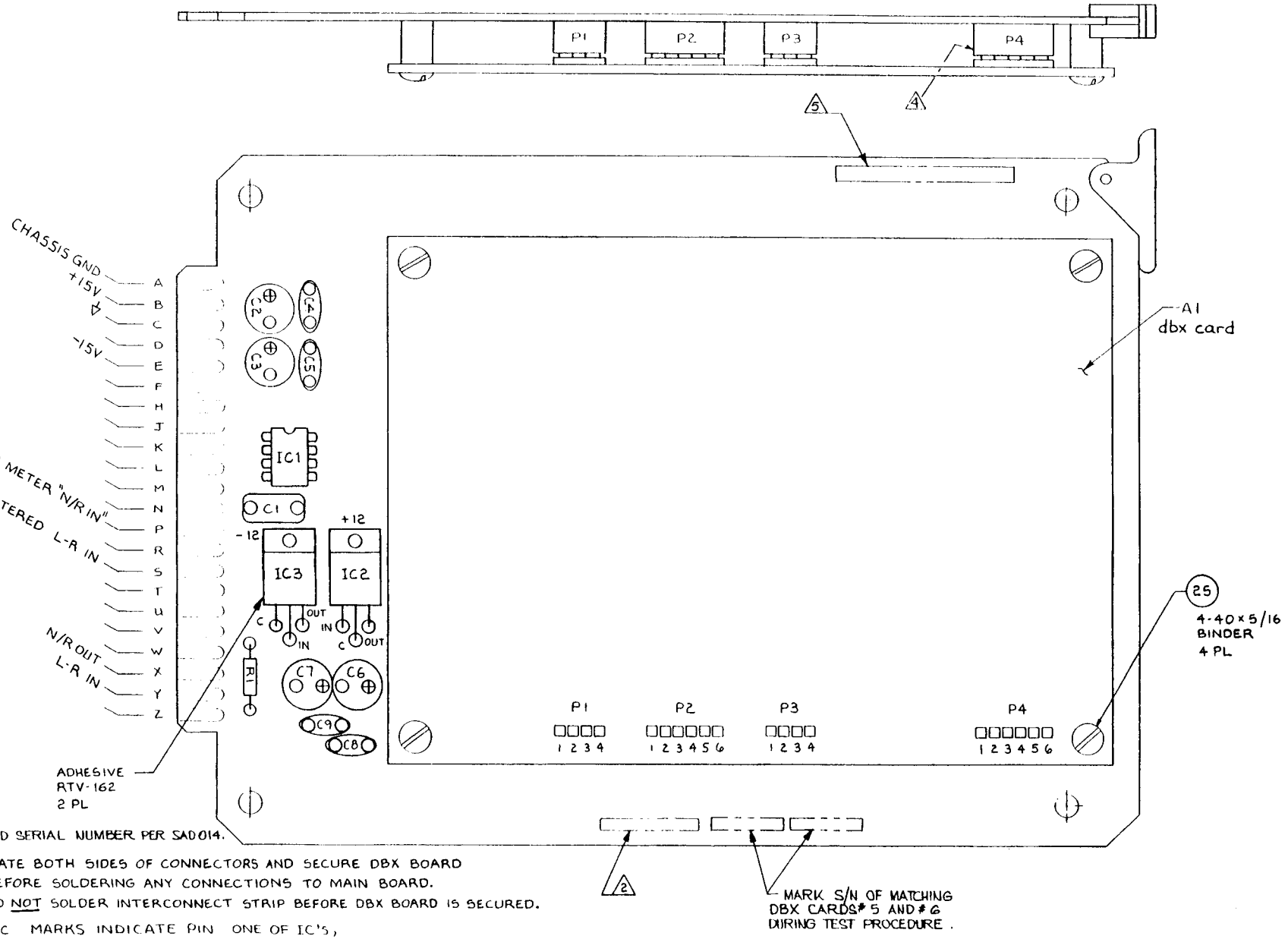
IC POWER PINS			
DEVICE	+V	-V	GND
072	8	4	—

1. ALL CAPACITORS ARE IN μF

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: SCHEMATIC #3 CARD 61023-000-01



5. ADD SERIAL NUMBER PER SAD014.

4. MATE BOTH SIDES OF CONNECTORS AND SECURE DBX BOARD BEFORE SOLDERING ANY CONNECTIONS TO MAIN BOARD. DO NOT SOLDER INTERCONNECT STRIP BEFORE DBX BOARD IS SECURED.

3. TIC MARKS INDICATE PIN ONE OF IC'S, CATHODE OF DIODES, POSITIVE SIDES OF CAPACITORS, EMITTER OF TRANSISTORS.

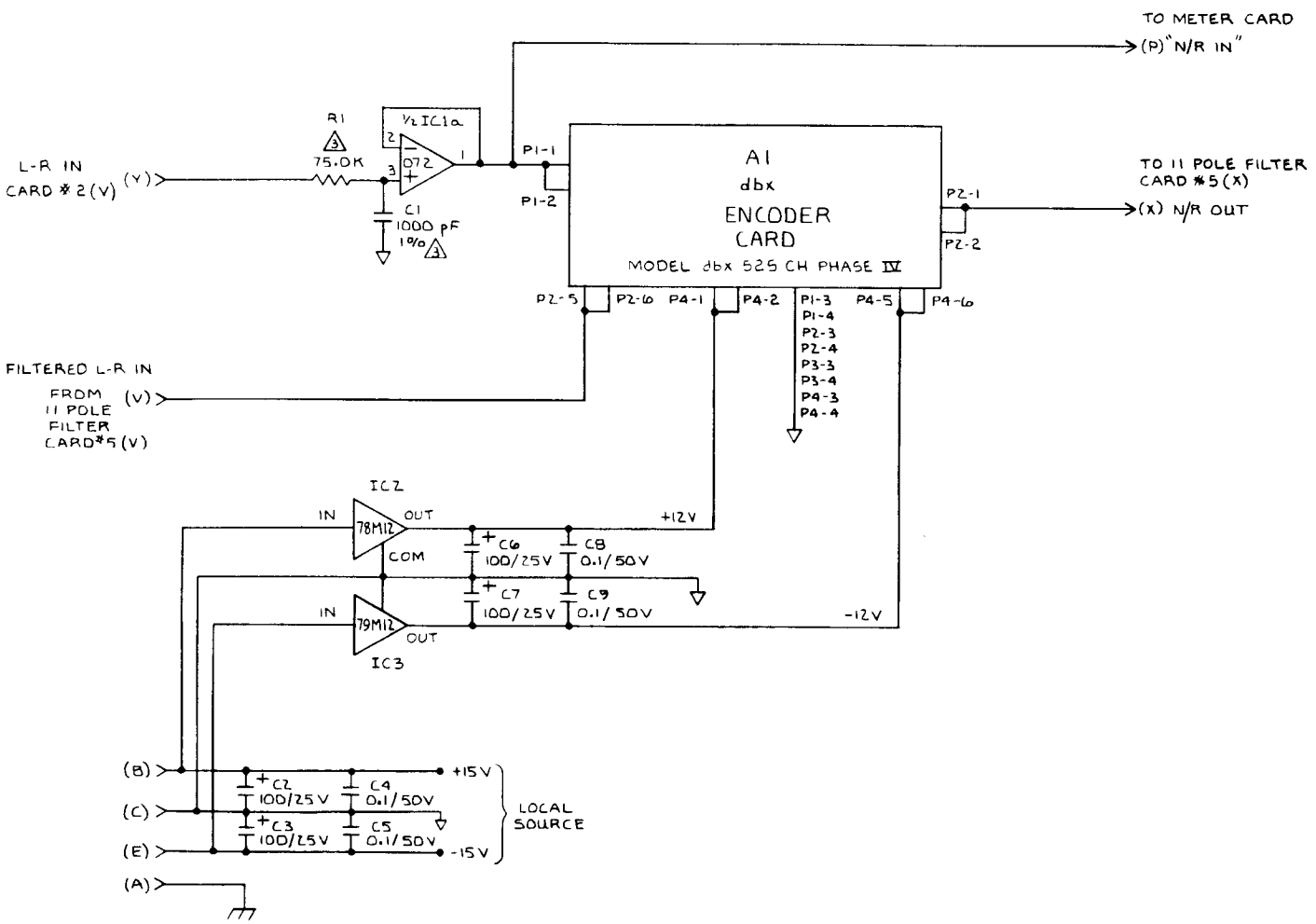
2. MARK PHASE NUMBER OF MOUNTED dbx CARD IN WHITE.

1. REFERENCE SCHEMATIC P/N 61024-000.

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: ASSEMBLY DRAWING
#4 CARD
31035-000-02



NOTES (UNLESS OTHERWISE SPECIFIED)

1- ALL RESISTORS ARE 1/8 W ± 1% MF.

2- ALL CAPACITORS ARE IN MICROFARADS.

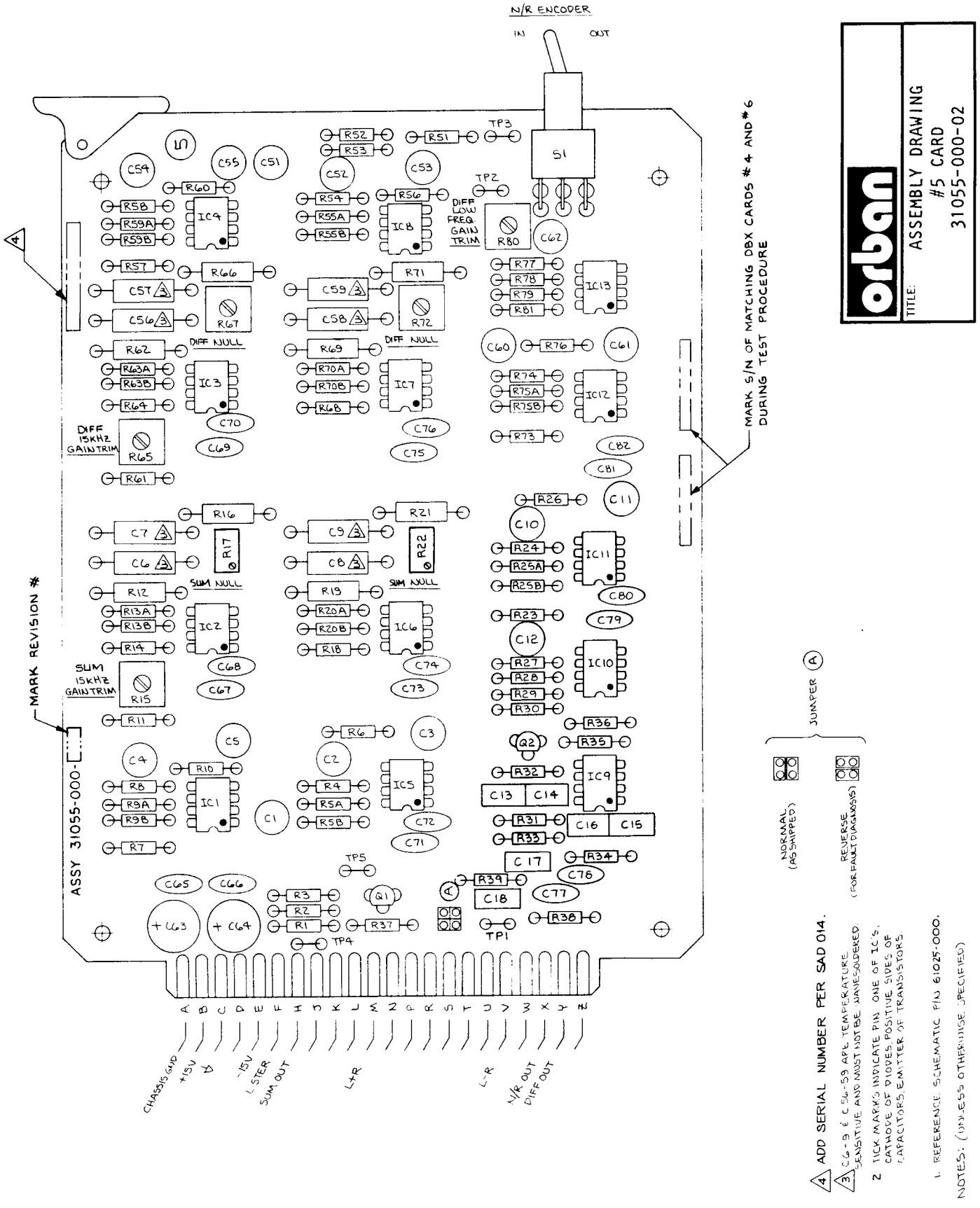
3 - MATCHED SET (75 µS).

REFERENCE DES		
ITEM	LAST USED	NOT USED
A	1	
C	9	
IC	3	16
R	1	

IC POWER PINS			
DEVICE	+V	-V	GND
072	8	4	-

orban

TITLE: SCHEMATIC
#4 CARD
61024-000-01



orban

TITLE: ASSEMBLY DRAWING #5 CARD 31055-000-02

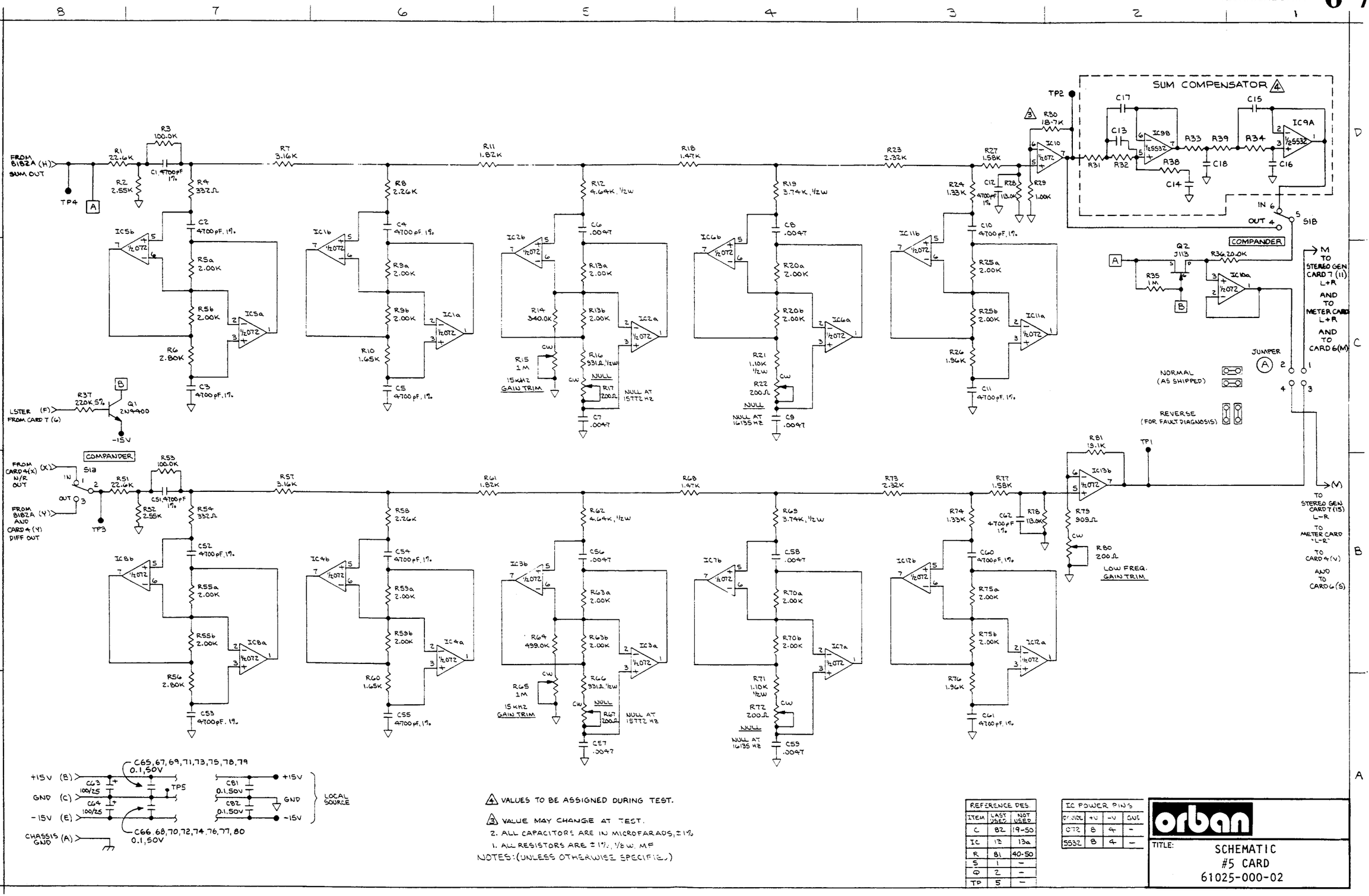
4 ADD SERIAL NUMBER PER SAD 014.

3 C6-9 & C56-59 ARE TEMPERATURE SENSITIVE AND MUST NOT BE WAVESOLDERED.

2 TICK MARKS INDICATE PIN ONE OF IC'S, CATHODE OF DIODES, POSITIVE SIDES OF CAPACITORS, EMITTER OF TRANSISTORS.

1. REFERENCE SCHEMATIC FIN 61025-000.

NOTES: (UNLESS OTHERWISE SPECIFIED)

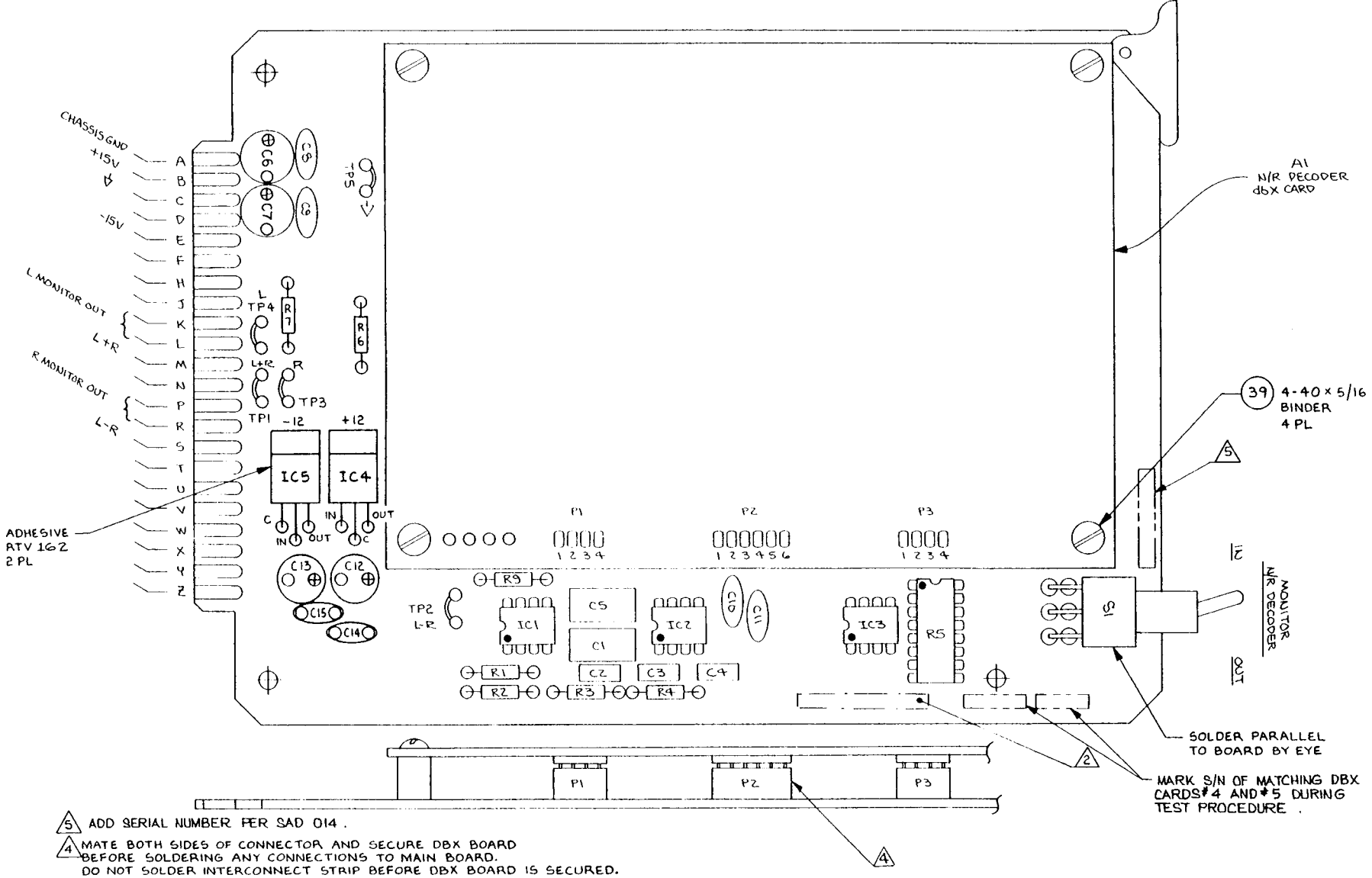


REFERENCE DES		
ITEM	LAST USED	NOT USED
C	82	19-50
IC	13	13a
R	81	40-50
S	1	–
Q	2	–
TP	5	–

IC POWER PINS			
DEVICE	+V	-V	GND
072	8	4	–
5532	8	4	–

orban

TITLE: SCHEMATIC #5 CARD 61025-000-02



5 ADD SERIAL NUMBER PER SAD 014 .

4 MATE BOTH SIDES OF CONNECTOR AND SECURE DBX BOARD BEFORE SOLDERING ANY CONNECTIONS TO MAIN BOARD. DO NOT SOLDER INTERCONNECT STRIP BEFORE DBX BOARD IS SECURED.

3. TIC MARKS INDICATE PIN ONE OF IC'S, CATHODE OF DIODES, POSITIVE SIDES OF CAPACITORS, EMITTER OF TRANSISTORS.

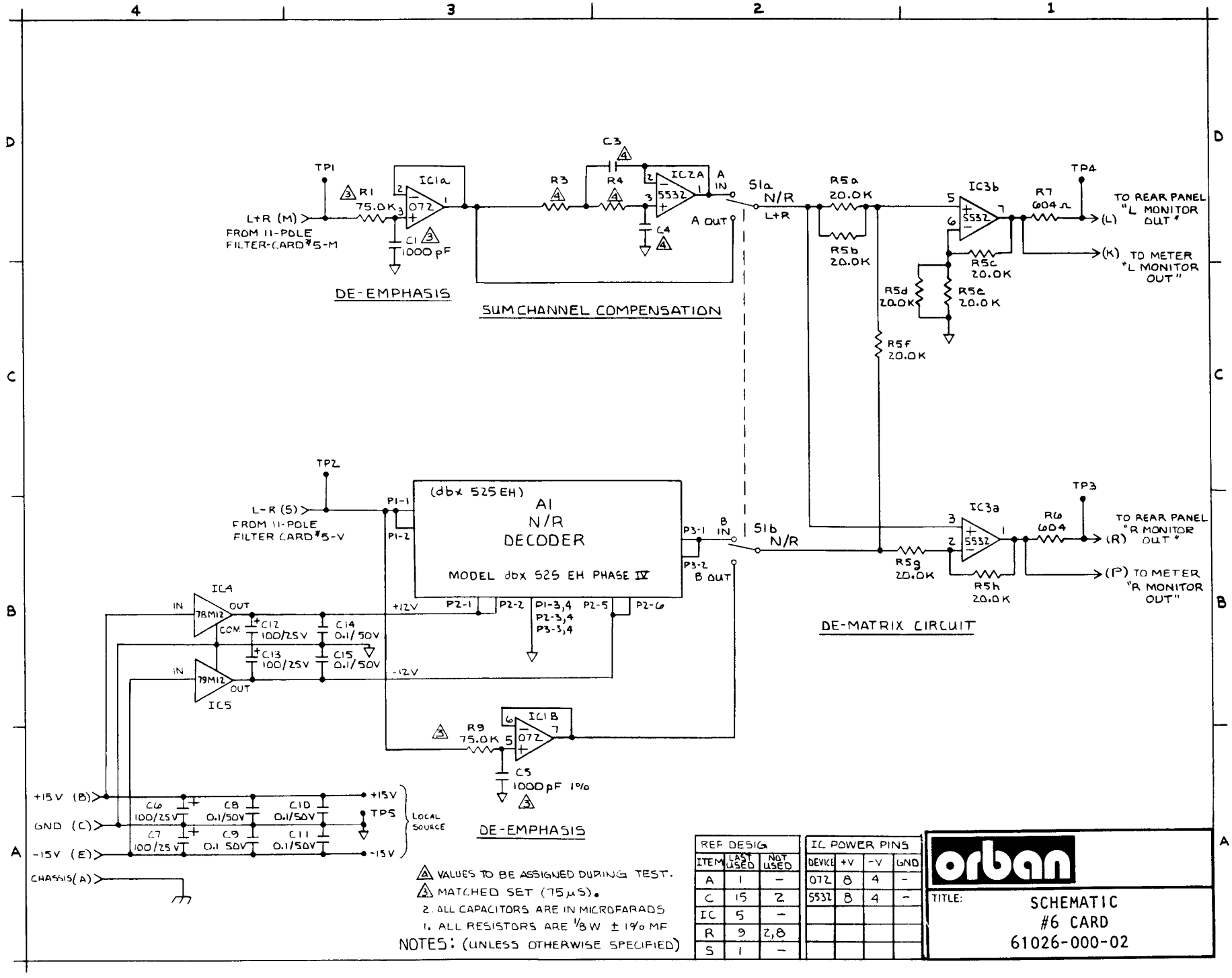
2 MARK PHASE NUMBER OF MOUNTED dbx CARD IN WHITE.

1. REFERENCE SCHEMATIC P/N 61026-000.

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: ASSEMBLY DRAWING
#6 CARD
31045-000-02



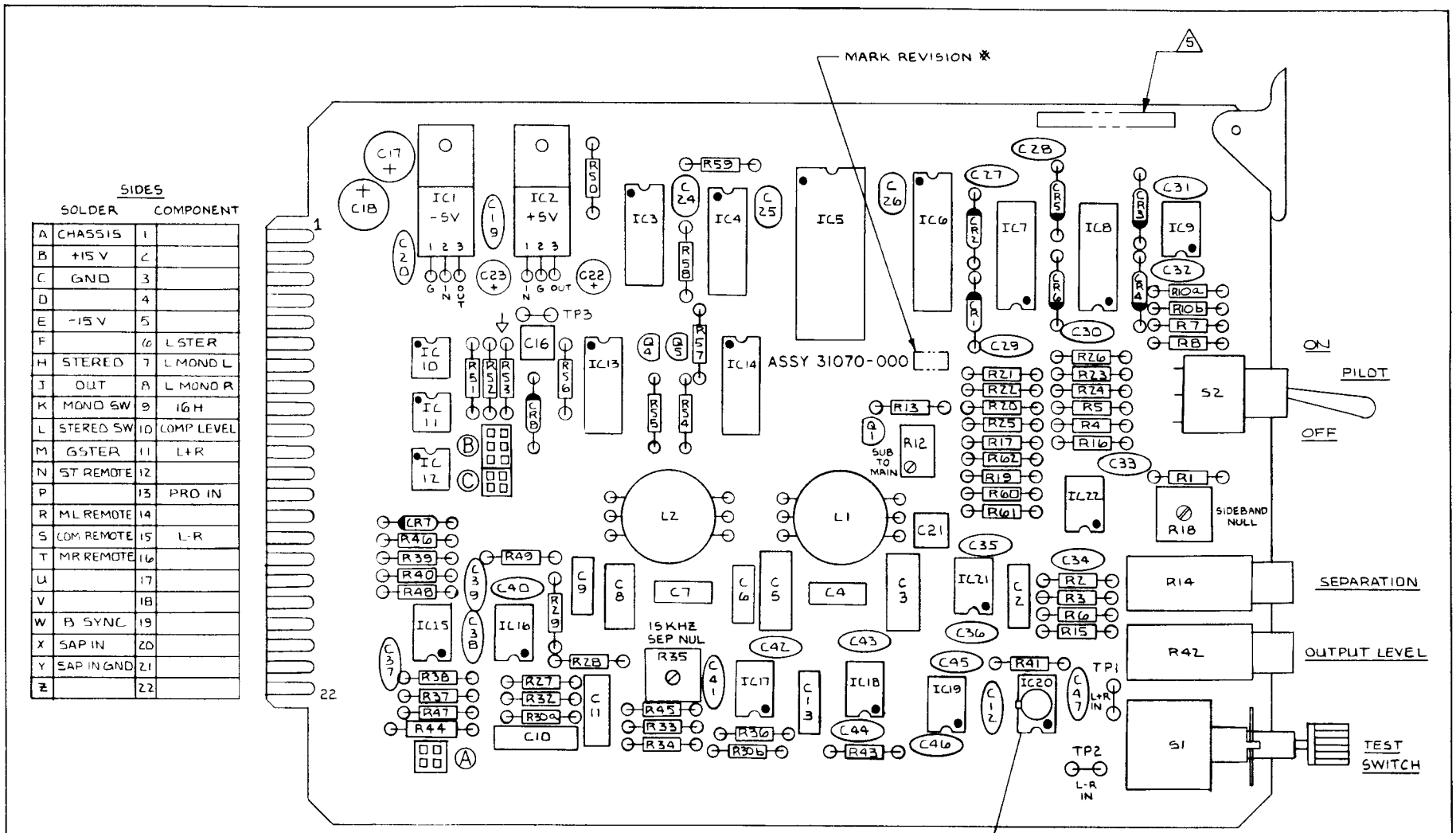
REF DESIG		
ITEM	LAST USED	NOT USED
A	1	–
C	15	2
IC	5	–
R	9	2,8
S	1	–

IC POWER PINS			
DEVICE	+V	-V	GND
1072	8	4	–
5532	8	4	–

orban

TITLE: SCHEMATIC #6 CARD 61026-000-02

4 VALUES TO BE ASSIGNED DURING TEST.
3 MATCHED SET (75 μS).
2. ALL CAPACITORS ARE IN MICROFARADS
1. ALL RESISTORS ARE 1/8 W ± 1% MF
NOTES: (UNLESS OTHERWISE SPECIFIED)



5 ADD SERIAL NUMBER PER SAD 014.

4. CLIP PIN 6 ON IC10, 11 AND 12.

3. REF SCHEMATIC 61027-000-01.

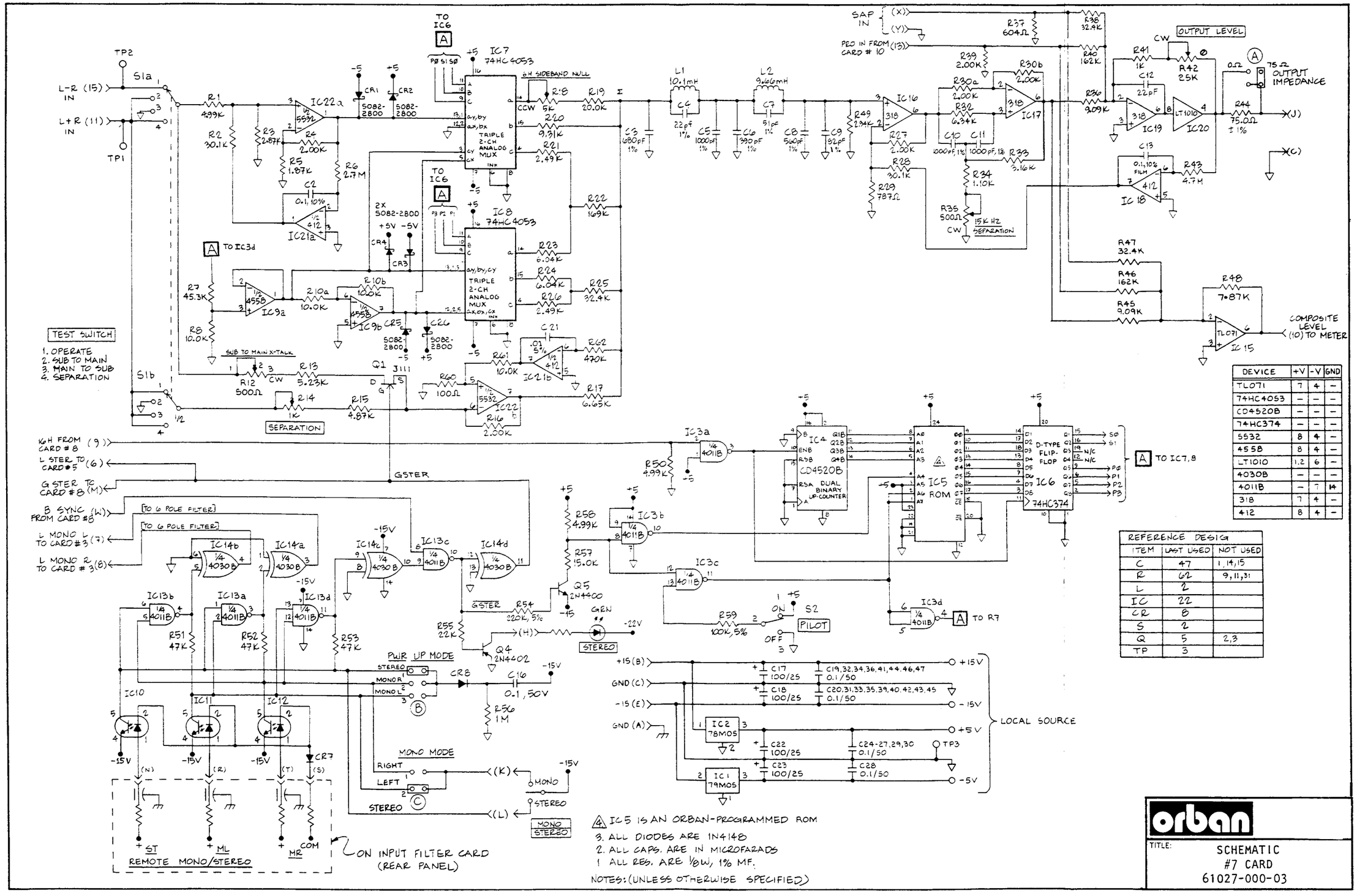
2. TIC MARKS INDICATE PIN ONE OF ICS, CATHODE OF DIODES, POS SIDE OF CAPACITORS, EMITTER OF TRANSISTORS.

1. USE COMPONENT MTG. PADS P/N 15051-000 FOR C21, C22.

NOTES: (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: ASSEMBLY DRAWING
#7 CARD
31070-000-02



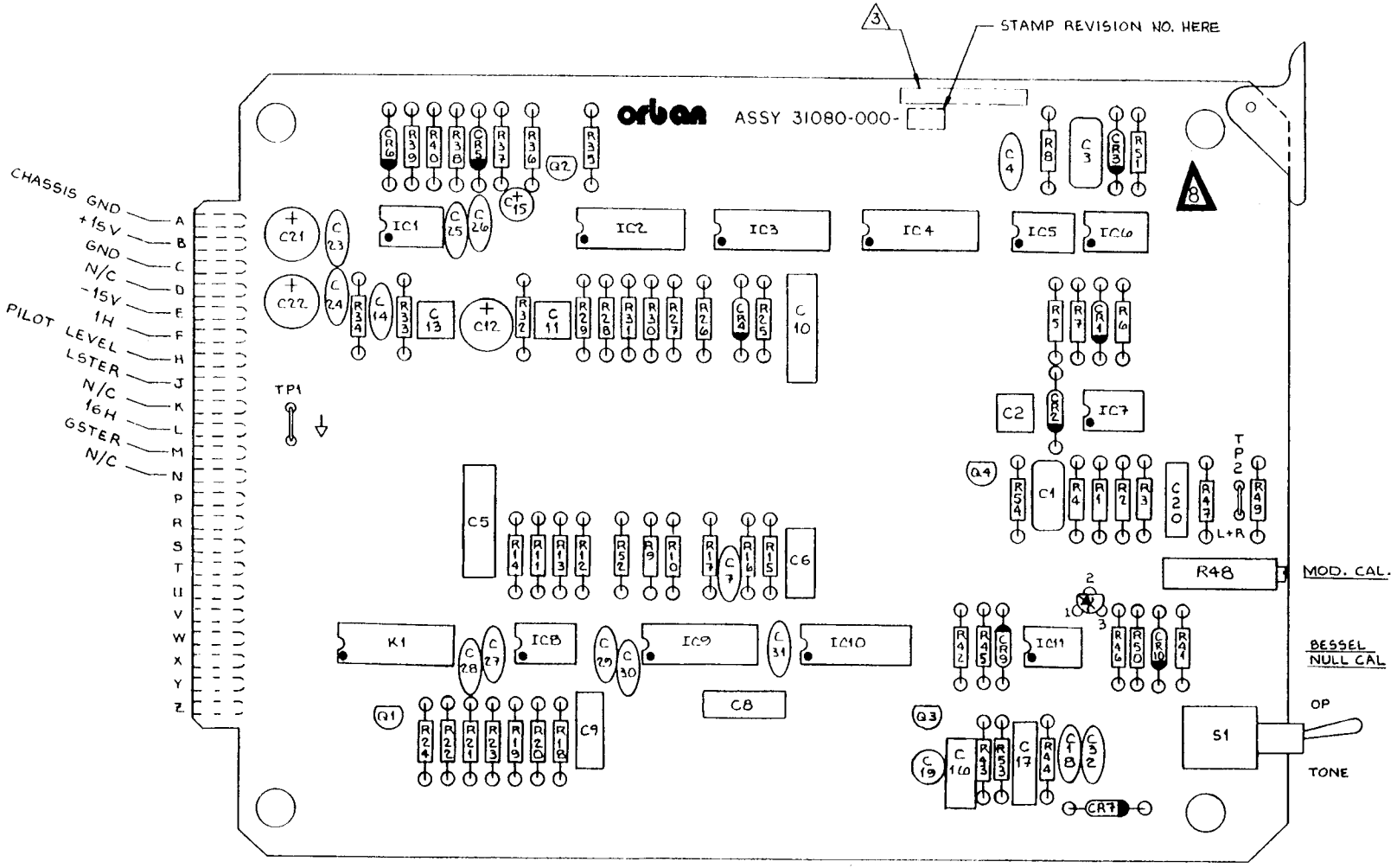
DEVICE	+V	-V	GND
TL071	7	4	–
74HC4053	–	–	–
CD4520B	–	–	–
74HC374	–	–	–
5532	8	4	–
4558	8	4	–
LT1010	1,2	6	–
4030B	–	–	–
4011B	–	7	14
318	7	4	–
412	8	4	–

REFERENCE DESIG

ITEM	LAST USED	NOT USED
C	47	1, 14, 15
R	62	9, 11, 31
L	2	
IC	22	
CR	8	
S	2	
Q	5	2, 3
TP	3	

orban

TITLE: SCHEMATIC
#7 CARD
61027-000-03



3 ADD SERIAL NUMBER PER SAD 014

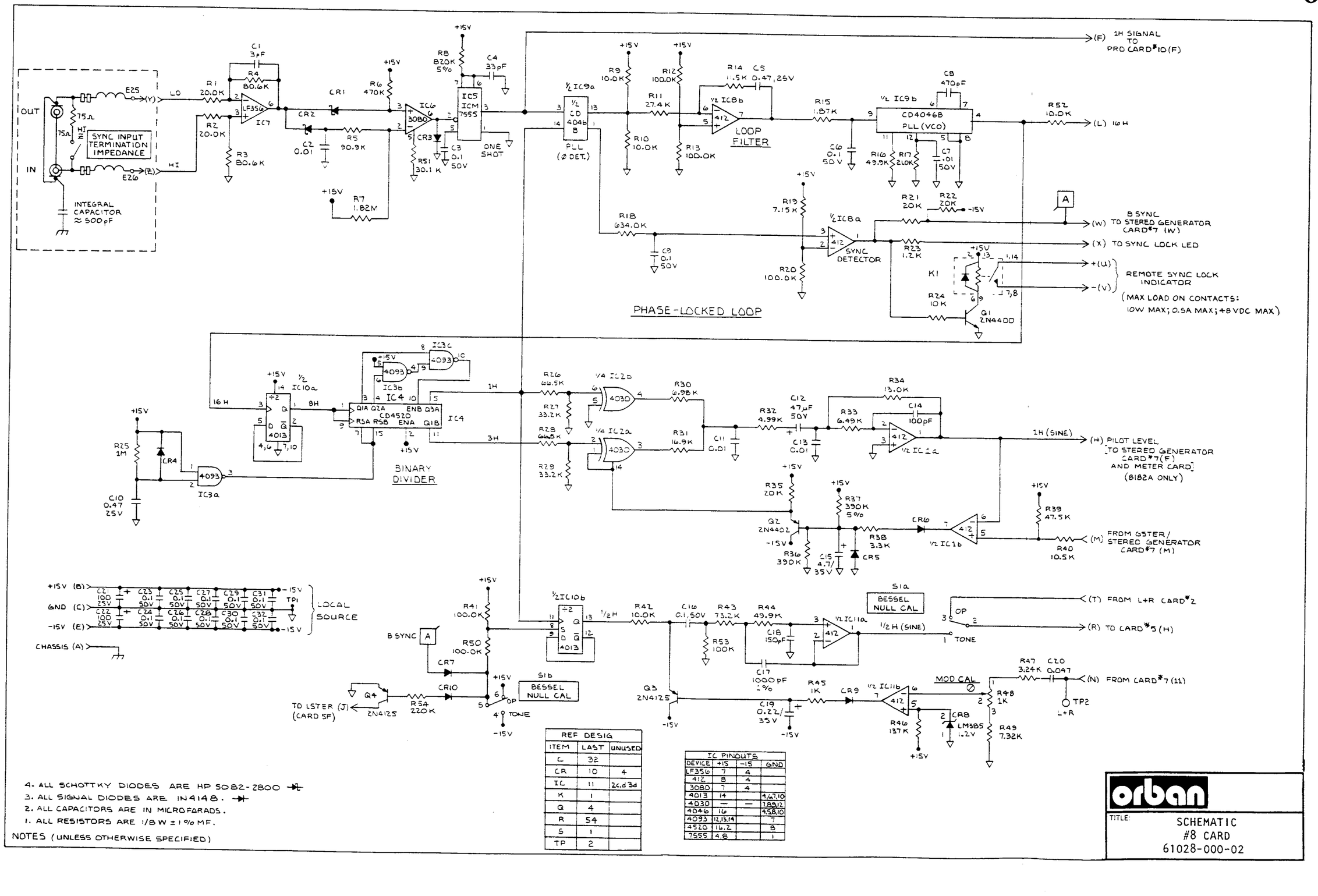
2. REF SCHEMATIC @1028-000

1. TIC MARKS INDICATE PIN ONE OF IC'S, CATHODE OF DIODES, POS SIDE OF CAPACITORS, EMITTER OF TRANSISTORS.

NOTES:(UNLESS OTHERWISE SPECIFIED)

orban

TITLE: ASSEMBLY DRAWING
#8 SYNC CARD
31080-000-03



REF DESIG		
ITEM	LAST	UNUSED
C	32	
CR	10	4
IC	11	2c,d 3d
K	1	
Q	4	
R	54	
S	1	
TP	2	

IC PINOUTS			
DEVICE	+15	-15	GND
LF356	7	4	
412	8	4	
3080	7	4	
4013	14		4,6,7,10
4030	—	—	7,8,9,12
4046	16		4,5,8,10
4093	12,13,14		7
4520	16,2		8
7555	4,8		1

4. ALL SCHOTTKY DIODES ARE HP 5082-2800
3. ALL SIGNAL DIODES ARE IN4148.
2. ALL CAPACITORS ARE IN MICROFARADS.
1. ALL RESISTORS ARE 1/8W ±1% MF.

NOTES (UNLESS OTHERWISE SPECIFIED)

orban

TITLE: SCHEMATIC #8 CARD 61028-000-02

Abbreviations

Some of the abbreviations used in this manual may not be familiar to all readers:

AGC	automatic gain control
CCIF	International Telephone Consultative Committee
CD	Compact disc
DAC	digital-to-analog converter
dBu	0dBu = 0.775Vrms. For this application, the dBm into 600Ω scale on voltmeters can be read as if it were calibrated in dBu.
DJ	disk jockey, an announcer who plays records in a club or on the air
EBS	Emergency Broadcasting System
EBU	European Broadcasting Union
EMI	electromagnetic interference
FCC	Federal Communications Commission (USA)
FET	field-effect transistor
G/R	gain reduction
HF	high-frequency
IC	integrated circuit
IEC	International Electrotechnical Commission
IF	intermediate frequency
IM	intermodulation (or "intermodulation distortion")
ips	inches per second
JFET	junction field-effect transistor
LED	light-emitting diode
LF	low-frequency
NAB	National Association of Broadcasters (USA)
N&D	noise and distortion
NRSC	National Radio Systems Committee
PM	pulse modulation
PPM	peak program meter
RF	radio frequency
RFI	radio-frequency interference
SCA	subsidiary communications authorization (FCC)
SID	slew-induced distortion
SMPTE	Society of Motion Picture and Television Engineers
S/N	signal-to-noise ratio
STL	studio-transmitter link
THD	total harmonic distortion
VCA	voltage-controlled amplifier

Warranty

United States Warranty

Limited Warranty

Valid only in the United States. We warrant Orban products against defects in material or workmanship for a period of one year from the date of original purchase for use, and agree to repair or, at our option, replace any defective item without charge for either parts or labor.

IMPORTANT: This warranty does not cover damage resulting from accident, misuse or abuse, lack of reasonable care, the affixing of any attachment not provided with the product, loss of parts, or connecting the product to any but the specified receptacles. This warranty is void unless service or repairs are performed by an authorized service center. No responsibility is assumed for any special, incidental or consequential damages. However, the limitation of any right or remedy shall not be effective where such is prohibited or restricted by law.

Simply take or ship your Orban product prepaid to our service department. Be sure to include your sales slip as proof of purchase date. (We will not repair transit damage under the no-charge terms of this warranty). Orban will pay return shipping.

NOTE: No other warranty, written or oral is authorized for Orban products.

This warranty gives you specific legal rights, and you may also have other rights which vary from state to state. Some states do not allow the exclusion of limitations of incidental or consequential damages or limitations on how long an implied warranty lasts, so the above exclusion and limitations may not apply to you.

International Warranty

Bedingungen

Orban gewährt 1 Jahr Garantie ab Verkaufsdatum auf nachweisbare Material- und Fabrikationsfehler. Der Garantieanspruch erlischt bei unsachgemäßer Handhabung, elecktrischer oder mechanischer Beschhädigung durch mißbräuchliche Anwendung sowie bei unsachgemäßer Reparatur durch nichtautorisierte Werkstätten. Voraussetzung für die Garantieleistung ist die Vorlage der ordnungsgemäß durch den Fachhändler ausgefüllten Garantiekarte sowie der Kaufrechnung. Transport- und Portospesen, welche aus der Einsendung des Gerätes zur Garantiereparatur erwachsen, können von Orban nicht übernommen werden, das Risiko der Zusendung trägt der Kunde. Die Garantie wird ausschließblich für den ursprünglichen Käufer geleistet.

Warranty Conditions

Orban warrants Orban products against evident defects in material and workmanship for a period of one year from the date of original purchase for use. This warranty does not cover damage resulting from misuse or abuse, or lack of reasonable care, and inadequate repairs performed by unauthorized service centers. Performance of repairs or replacements under this warranty is subject to submission of this Warranty/Registration Card, completed and signed by the dealer on the day of purchase, and the sales slip. Shipment of the defective item for repair under this warranty will be at the customer's own risk and expense. This warranty is valid for the original purchaser only.

Conditions de garantie

Pour toute mise en œvre de garantie ou de service après-vente, vous devez vous adresser à votre revendeur. Notre société assure au revendeur le remplacement gratuit des pièces détachées nécessaires à la réparation pendant un an, à partir de la date de votre facture, sauf en cas de non respect des prescritions d'utilsation ou lorsqu' une cause étrangère à l'appareil est responsable de la défaillance. Les dispositions stipulées ci-dessus ne sont pas exclusives du bénéfice au profit de l'acheteur de la garantie légale pour défaut et vice cachés qui s'applique, en tout état de cause, dans les conditions des articles 1641 et suivants du Code Civil.

Condizioni di garanzia

L'Orban presta garanzia per un anne dalla data della vendita per difetti di materiale e fabbriccazione che possono essere provati. Il diritto di garanzia cessa in caso di manipolazione impropria, danneggiamento electtrico o meccanico attraverso i'uso non approriato e riparazione inesperta eseguita da officine non autorizzate. E' indispensabile, per la prestazione della garanzia, presentare la carta di garanzia debitamente riempita dal rivenditore autorizzato e la fattura di vendita. Spese di trasporto che risultano dall'invio dell'impianto per la riparazione in garanzia, non possono essere assunte dall'Orban i'invio è a rischio e pericolo del cliente. La garanzia verrà data solo al primo acquirente.

Condiciones de garantia

Orban concede 1 añe de garantia por defectos comprobables de material o de fabricación a partir de la fecha de venta. El derecho de garantia caduca en caso de procederse a uno manipulación inadecuada en caso de producirse daño electrico o mecánico por uso indebido, así como también en caso de reparaciones inadecuados por parte de talleres no autorizados. La prestación de la garantia está sujeta a la presentación de la Tarjeta de Garantia rellenada correctamente por el vendedor autorizado, y de la factura de compra. Orban no assume ningún gasto de transporte o correo incurrido por el envio del aparato defectuoso para la reparación bajo garantia; el riesgo del envio ha de ser asumido por el cliente. La garantia se concede única y exclusivamente al comprador original.