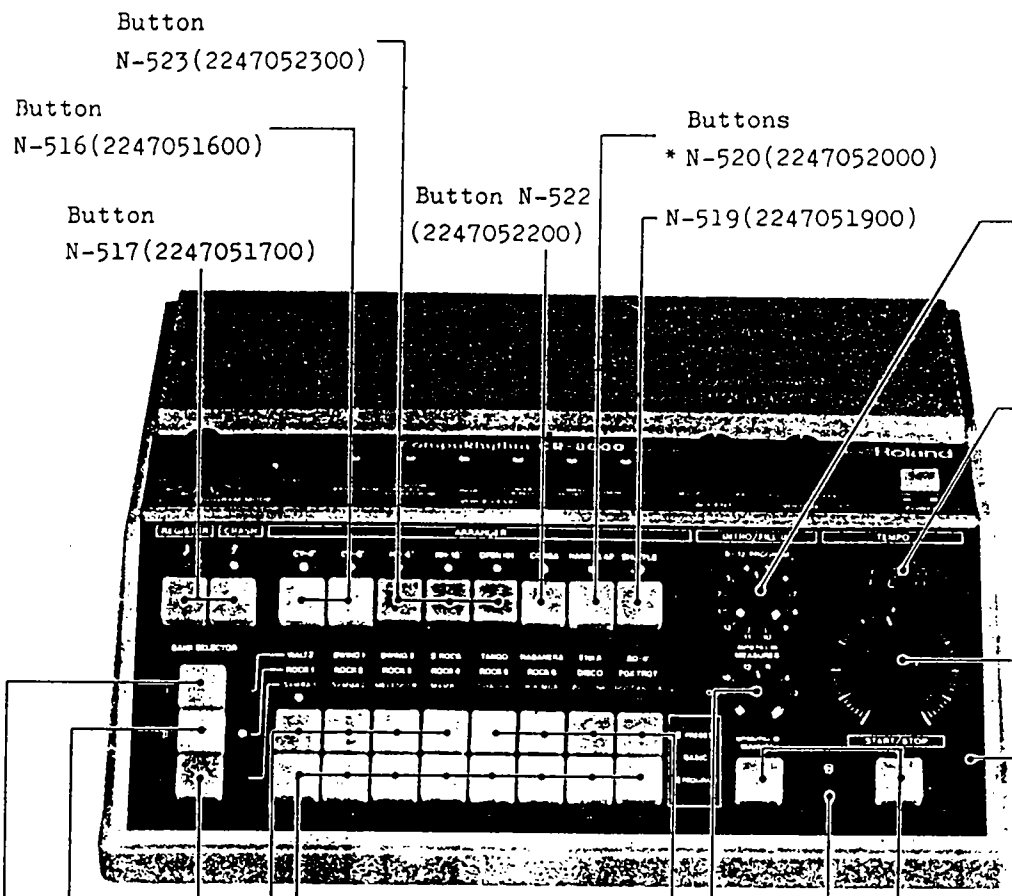
CR-5000/8000 SERVICE NOTES

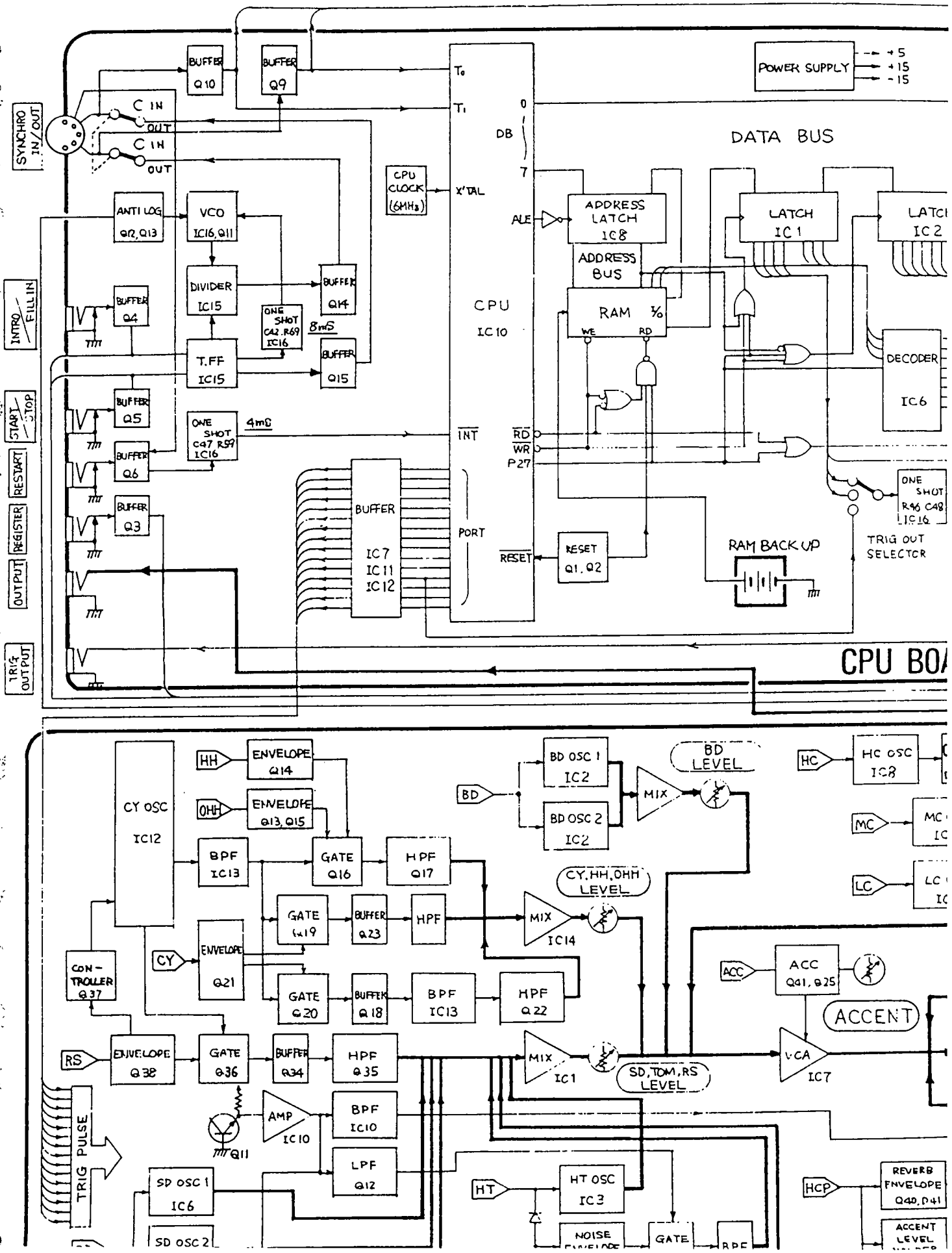
SPECIFICATIONS

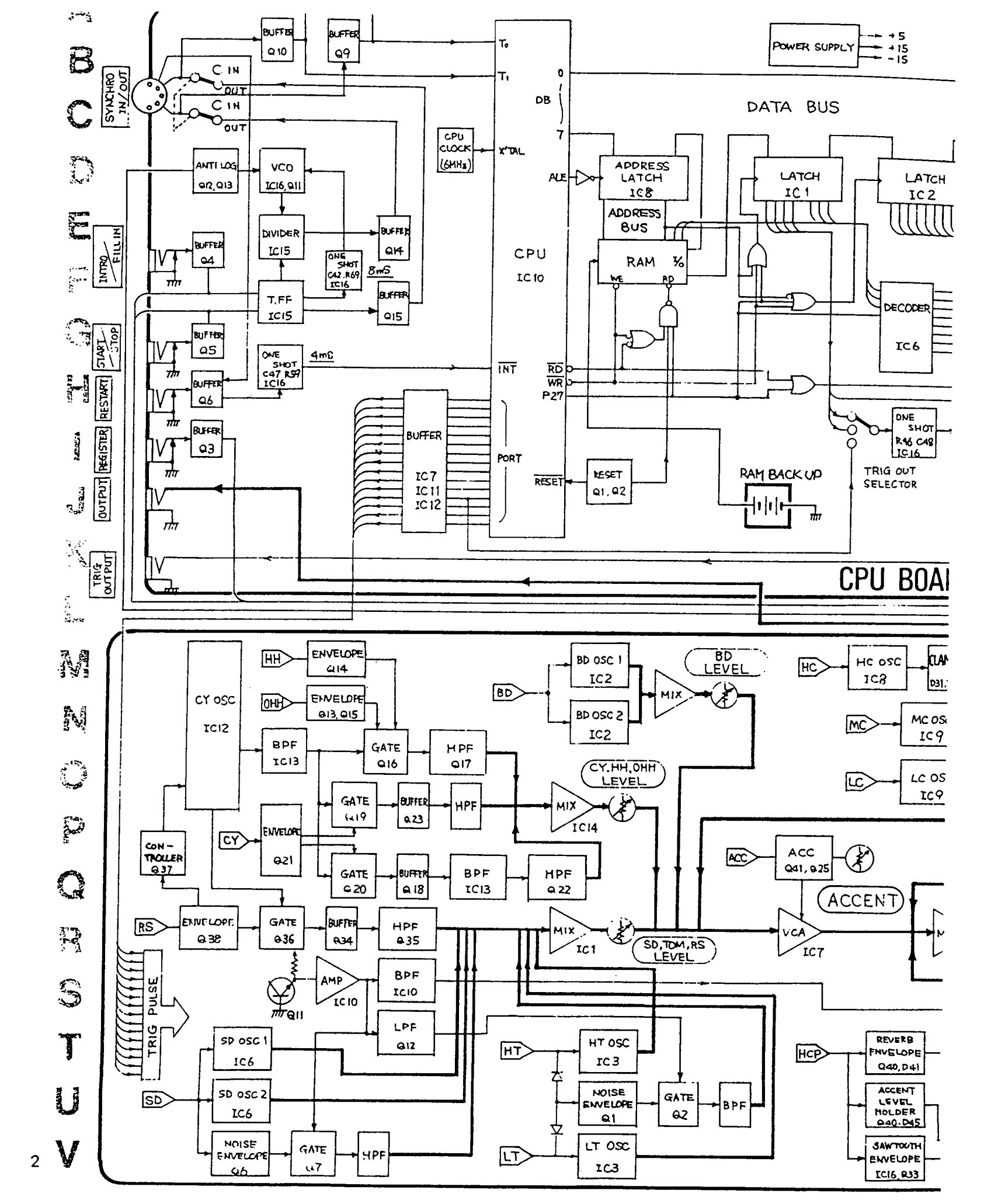
First Edition

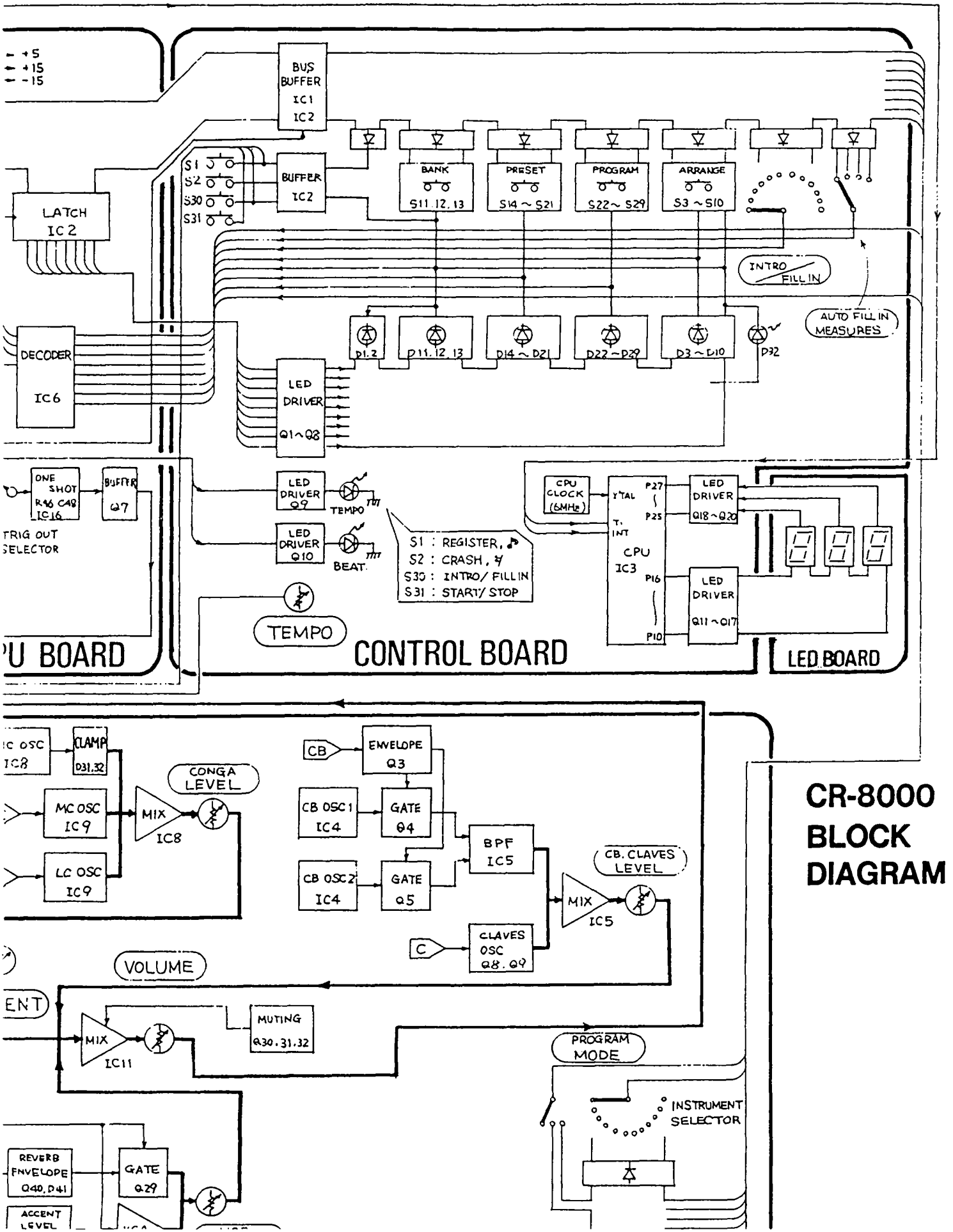
Second Printing (July 12, 1983 E2)

OUTPUT IMPEDANCE	Less than 6KΩ or less than 25KΩ (Serial No. CR5000 091100–, CR8000 090900–)
TRIGGER OUT	Level: +5 positive edge
	Width: 44ms (typ) @ TEMPO min./12ms (typ) @ TEMPO max.
OUTPUT (max.)	4V p-p @ VOICE LEVEL max./VOLUME max./ACCENT min. (16V p-p @ ACCENT max.)
(into 100KΩ)	2.5V p-p @ VOICE LEVEL mid./VOLUME mid./ACCENT mid.
(CR8000)	
SYNC IN	+15V (max.)
SYNC OUT	+15V (Tempo clock – 6.7ms-71ms)
POWER CONSUMPTION ...	CR5000: 10W, CR8000: 12W
DIMENSIONS	331(W) x 278(D) x 108(H)mm
WEIGHT	3.7kg
NOISE	0.3mV rms (–68dB) (0dB = 0.775V)
(load 100kΩ)	(DIN 45405 wtd)

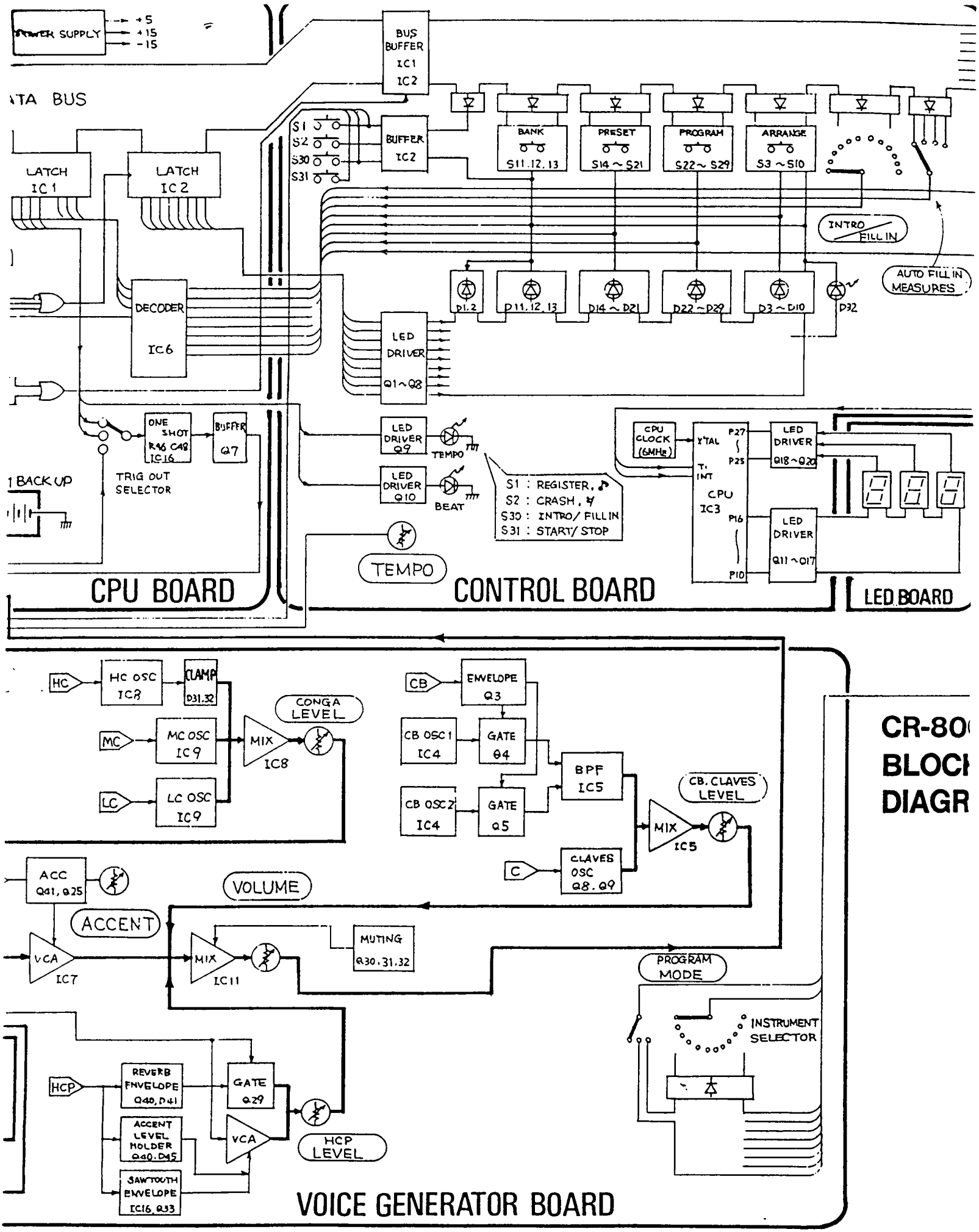



POWER SUPPLY
+5
+15
-15
DATA BUS
CPU BOA
BUFFER Q10
BUFFER Q9
SYNCHRO IN/OUT
C IN
OUT
C IN
OUT
CPU CLOCK (6MHz)
ANTI LOG Q12,Q13
VCO IC16,Q11
DIVIDER IC15
BUFFER Q14
ONE SHOT CR2,R69 IC16
8mS
T.FF IC15
BUFFER Q15
INTRO FILL IN
BUFFER Q4
START STOP
BUFFER Q5
ONE SHOT CR7 R59 IC16
4mS
RESTART
BUFFER Q6
REGISTER
BUFFER Q3
OUTPUT
TRIG OUTPUT
CPU IC10
ADDRESS LATCH IC8
ADDRESS BUS
RAM
WE
RD
LATCH IC1
LATCH IC2
DECODER IC6
ONE SHOT R46 C48 IC16
TRIG OUT SELECTOR
RAM BACK UP
RESET Q1, Q2
BUFFER IC7 IC11 IC12
PORT
CY OSC IC12
HH
ENVELOPE Q14
OHH
ENVELOPE Q13, Q15
BPF IC13
GATE Q16
HPF Q17
BD
BD OSC 1 IC2
BD OSC 2 IC2
MIX
BD LEVEL
HC
HC OSC IC8
MC
LC
CY, HH, OHH LEVEL
GATE Q19
BUFFER Q23
HPF
MIX IC14
CY
ENVELOPE Q21
CONTROLLER Q37
GATE Q20
BUFFER Q18
BPF IC13
HPF Q22
ACC
ACC Q41, Q25
ACCENT
RS
ENVELOPE Q38
GATE Q36
BUFFER Q34
HPF Q35
MIX IC1
SD, TOM, RS LEVEL
VCA IC7
TRIG PULSE
Q11
AMP IC10
BPF IC10
LPF Q12
SD OSC 1 IC6
SD OSC 2
HT
HT OSC IC3
NOISE
GATE
HCP
REVERB ENVELOPE Q40, Q41
ACCENT LEVEL

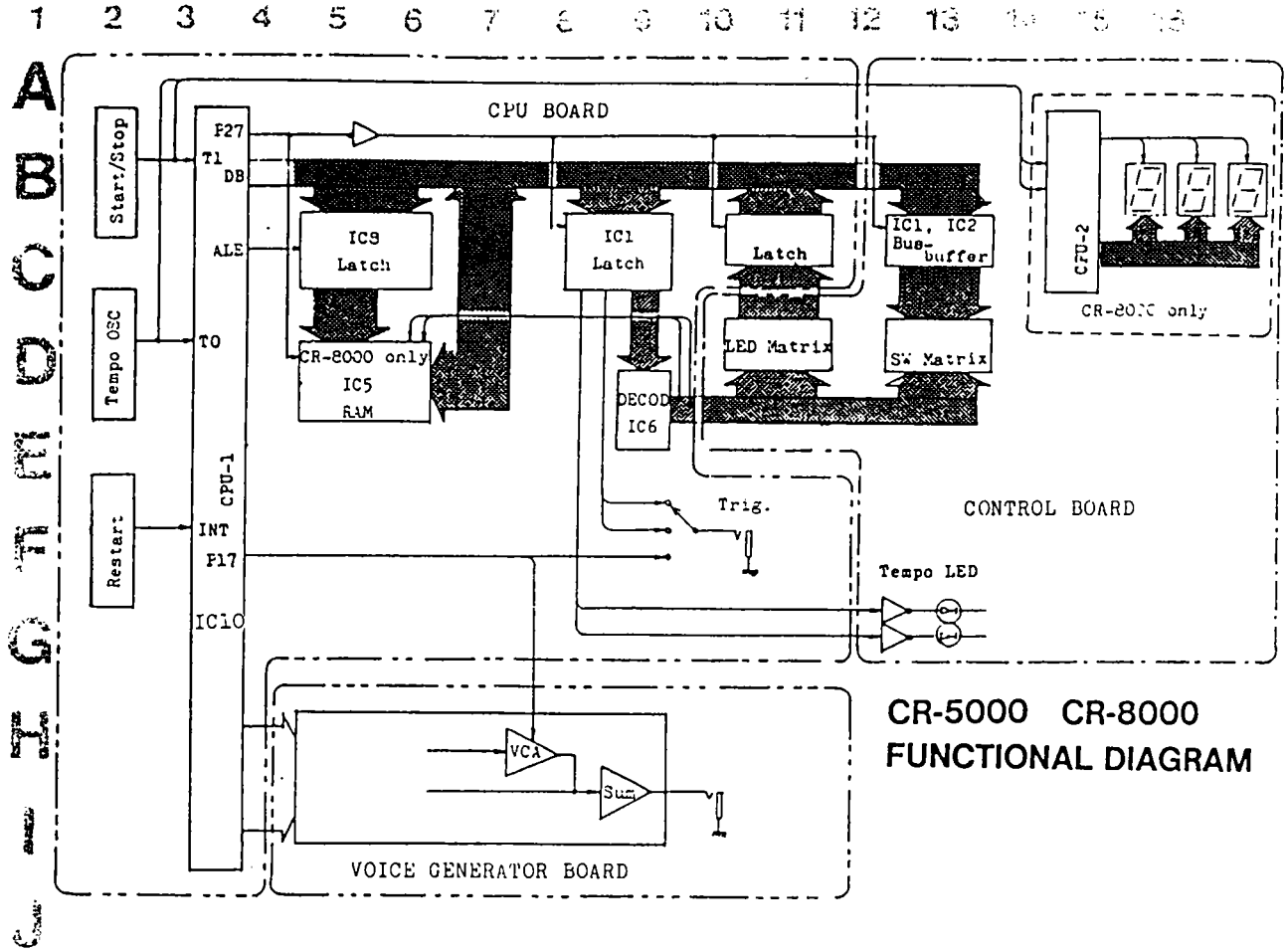

BUFFER Q10
BUFFER Q9
SYNCHRO IN/OUT
C IN
OUT
C IN
OUT
ANTI LOG Q12, Q13
VCO IC16, Q11
DIVIDER IC15
BUFFER Q14
ONE SHOT C42, R69 IC16
8mS
BUFFER Q4
INTRO/FILL IN
T.FF IC15
BUFFER Q15
BUFFER Q5
START/STOP
ONE SHOT C47 R59 IC16
4mS
BUFFER Q6
RESTART
BUFFER Q3
REGISTER
OUTPUT
TRIG OUTPUT
BUFFER IC7 IC11 IC12
To
T1
DB
7
X'TAL
CPU CLOCK (6MHz)
CPU IC10
PORT
INT
RD
WR
P27
RESET
RESET Q1, Q2
ALE
ADDRESS LATCH IC8
ADDRESS BUS
RAM 1/0
WE
RD
LATCH IC1
LATCH IC2
DECODER IC6
DATA BUS
POWER SUPPLY
+5
+15
-15
ONE SHOT R46 C48 IC16
TRIG OUT SELECTOR
RAM BACK UP
CPU BOAI
CY OSC IC12
HH
ENVELOPE Q14
OHH
ENVELOPE Q13, Q15
BPF IC13
GATE Q16
HPF Q17
GATE Q19
BUFFER Q23
HPF
CY
ENVELOPE Q21
GATE Q20
BUFFER Q18
BPF IC13
HPF Q22
CON-TROLLER Q37
RS
ENVELOPE Q38
GATE Q36
BUFFER Q34
HPF Q35
TRIG PULSE
Q11
AMP IC10
BPF IC10
LPF Q12
SD OSC 1 IC6
SD
SD OSC 2 IC6
NOISE ENVELOPE Q6
GATE Q7
HPF
BD
BD OSC 1 IC2
BD OSC 2 IC2
MIX
BD LEVEL
CY, HH, OHH LEVEL
MIX IC14
MIX IC1
SD, TOM, RS LEVEL
ACC
ACC Q41, Q25
ACCENT
VCA IC7
HC
HC OSC IC8
MC
MC OSC IC9
LC
LC OSC IC9
HT
HT OSC IC3
NOISE ENVELOPE Q1
GATE Q2
BPF
LT
LT OSC IC3
HCP
REVERB ENVELOPE Q40, D41
ACCENT LEVEL HOLDER Q40, D45
SAWTOOTH ENVELOPE IC16, Q33



CR-8000 BLOCK DIAGRAM



CR-80
BLOCK
DIAGR



CR-5000 CR-8000
FUNCTIONAL DIAGRAM

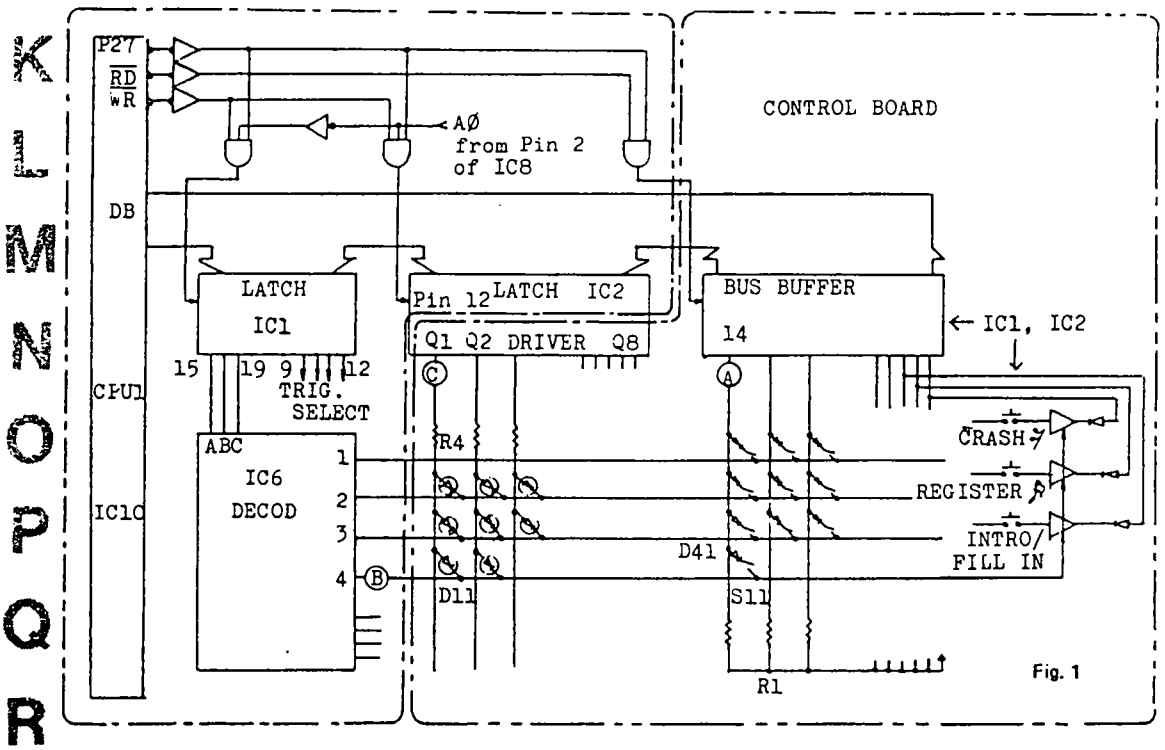
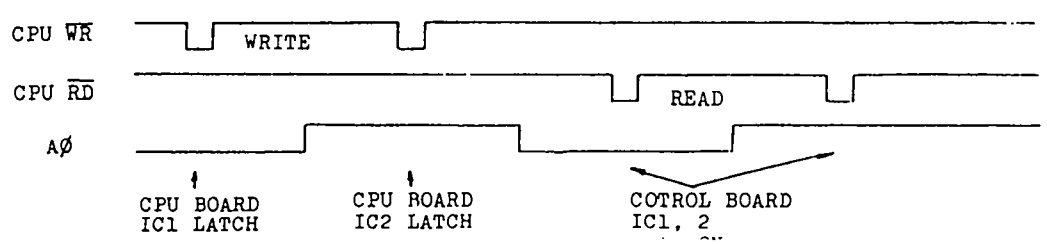


Fig. 1



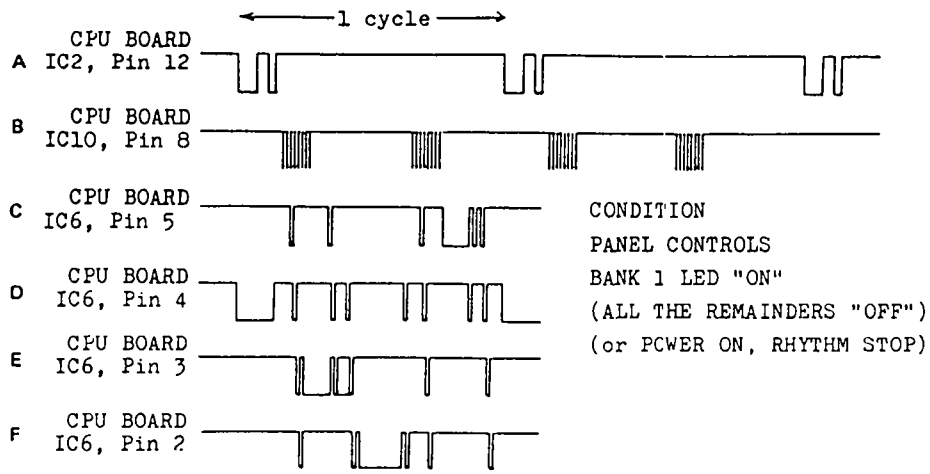


Fig. 2

CIRCUIT DESCRIPTION

SWITCH SCANNING

CPU holds one of switch matrix rows low through LATCH IC1 and DECODER IC6.
Exp. When S11 closes while pin 4 of IC6 (B in Fig. 1) is held low, pin 14 of BUFFER IC1 (A in Fig. 1) which is pulled up via R1, becomes low. This low is read by CPU through data bus.
CPU continues this sequence for the remaining 7 matrix rows (Ⓑ, Fig.2).
Once rhythm starts, time interval between switch scanning varies to Tempo Clock rate.

LED DINAMIC SCANNING

To light LED that is on, CPU selects matrix row and column where the LED is connected diagonally.
In the above example D11 has been on, CPU fires LED driver Q1 through LATCH IC2 in sympathy with low at B in Fig. 1 (Ⓐ and Ⓓ in Fig. 2.)

Lengths of lows and intervals between lows in Fig. 2 also vary greatly with controls setting and rhythm tempo.

VOICE TRIGGER SIGNAL

CPU delivers trigger signals (negative going) to individual VOICE Generators.
Trigger signal goes negative at the falling edge of tempo clock and stays low until the next falling edge of the tempo clock. That is,width of trigger signal is equal to period of one clock signal. The maximum trigger signal rate is $\frac{24 \text{ clocks}}{4}$:(♪).

EXT TRIGGER Derived from LATCH IC1 on CPU board. They are also negative going and the pulse width is equal to that of tempo clock.

RESTART

CPU reads INT terminal (not in use for interrupt application) every 3ms and , when INT is high, resets internal counter to revert to onset of a measure.
If monostable (1/6IC6. C47 and R59) output is high for a period shorter than 3ms or

:E GENERATORS

t voice generators are designed based on a fashion
ilar to those detailed in the circuit description
the TR-808 Service Notes which is expected to be
erenced to as necessary. Exceptions are Cymbal and
Shot. Below brief comments on individual voices.

circuit consists of two bridged-T networks.

) has two bridged-T filters for drum sound, in
ition, noise generator for snare sound.

1T:

lged-T networks in these stage include two diodes
heir RC constant loop. The diode changes con-
ing rate in proportion to sound amplitude passing
)ugh the network, changing filter characteristic,
; shifts filter response curve (frequency) along
id contour. Pink noise is combined with this out-
to simulate reverbration.

1C. HC

) based on Bridged-T. HC output is clamped on D31
D32 to have multiple harmonics to emphasis highs.

)HH. CY

combined square waves from Shmitt triggers
are gated at choppers with the contour
)ed by respective envelop generator outputs.

1g six Schmitt triggers, two are used which
reset by an RS trig fed through Q37. The
;t rising edge of two outputs are synchro-
:d to each other to eliminate unsavory sound
:he very first of RS note.

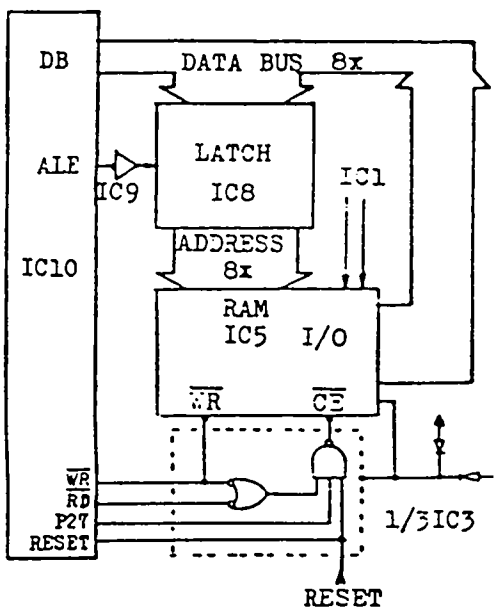
CB

Two oscillator outputs of
frequency are summed at B
gated at choppers.

HCP

HCP sound is accomplished
lating white noise with sa
waves derived from IC6.

RAM
CR-8000 only



NOTES:
P27 - high during RAM accessin
$\overline{CE}$ - high during power off

outputs of different
summed at BPF after
ers.

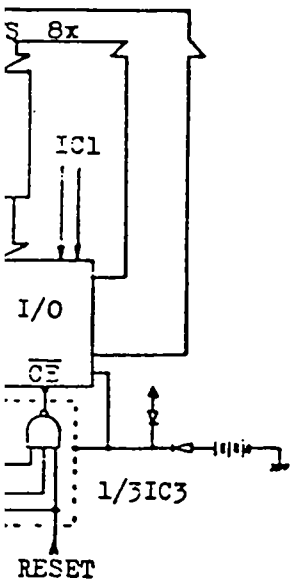
complished by modu-
ise with sawthooth
rom IC6.

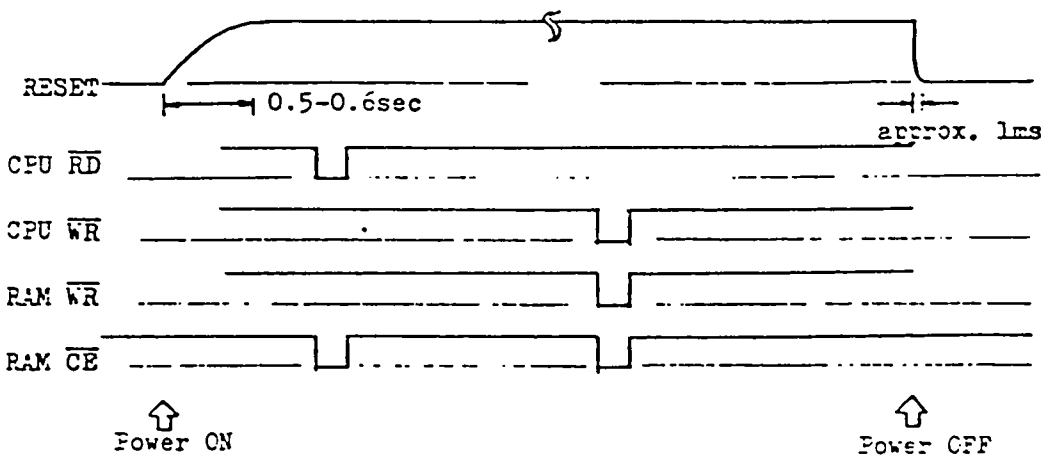
ACCENT

Sounds passing through VCA IC7 are accentuated simaltenously when an accent pulse is applied to Q41 with its amplitude determined by VR8 setting.

C (CLAVES)

The circuit is designed based on conventional R-C phase oscillator.





RAM accessing
power off

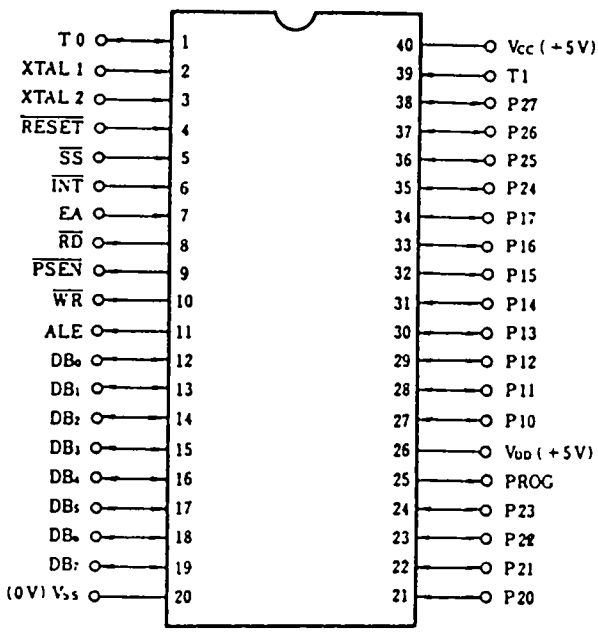
Storage for programmed rhythm patterns are provided for the CR-8000. The memories are maintained by backup batteries (three 1.5V dry cells).
The ten address bits are required to access to a memory location on 1024 words by 4 bit RAM uPD444; 8 bits are latched into IC8 by ALE and 2 bits into IC1 (also used for switch scanning).

DEC.8,1981

μPD8049C/μPD8048C

SINGLE COMPONENT 8-BIT MICROCOMPUTER

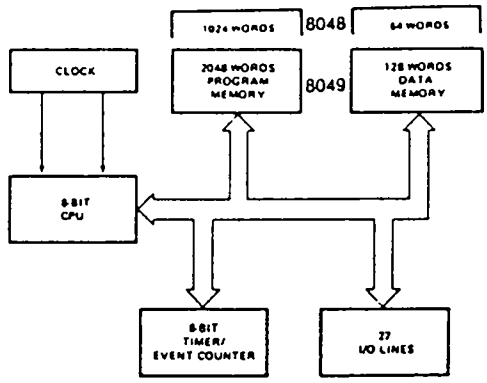
(Top View)



8049
2K x 8 ROM
128 x 8 RAM

8048
1K x 8 ROM/EPROM
64 x 8 RAM

BLOCK DIAGRAM



μPD8049C

PIN NAME	PIN NO.	FUNCTION
TØ	1	TEMPO CLOCK IN
T1	39	START/STOP SIGNAL IN
INT	6	RESTART SIGNAL IN
DATA BUS	12-19	SWITCH SCANNING OUT/IN LEDs LIGHT OUT TEMPO LED, TRIG OUT MEMORY READ/WRITE (CR-8000 only)
PORT 1		TRIGGER OUT FOR VOICE GENERATOR
P10	27	CYMBAL
P11	28	HI TOM
P12	29	OPEN HI-HAT
P13	30	LOW TOM
P14	31	HI-HAT
P15	32	SNARE DRUM
P16	33	BASS DRUM
P17	34	ACCENT
PORT 2		TRIGGER OUT FOR VOICE GENERATOR
P20	21	HI CONGA
P21	22	MIDDLE CONGA
P22	23	LOW CONGA
P23	24	COWBELL
P24	35	CLAVES
P25	36	RIM SHOT
P26	37	HAND CLAP

uPD8049C-159
uPD8049C-232 (improved version)

The following program bug is eliminated in the -232 version.

Condition
SHUFFLE ON with alternate rhythm patterns selected.
INTRO/FILL IN is pushed after the termination of first measure pattern.

When INTRO/FILL IN part ends, CPU delivers rhythm pattern data for the first measure but replaces the first step data only with the one for the second measure.
This is perceptive in RHUMBA, BEGUINE or

μPD8048C CR-8000 only

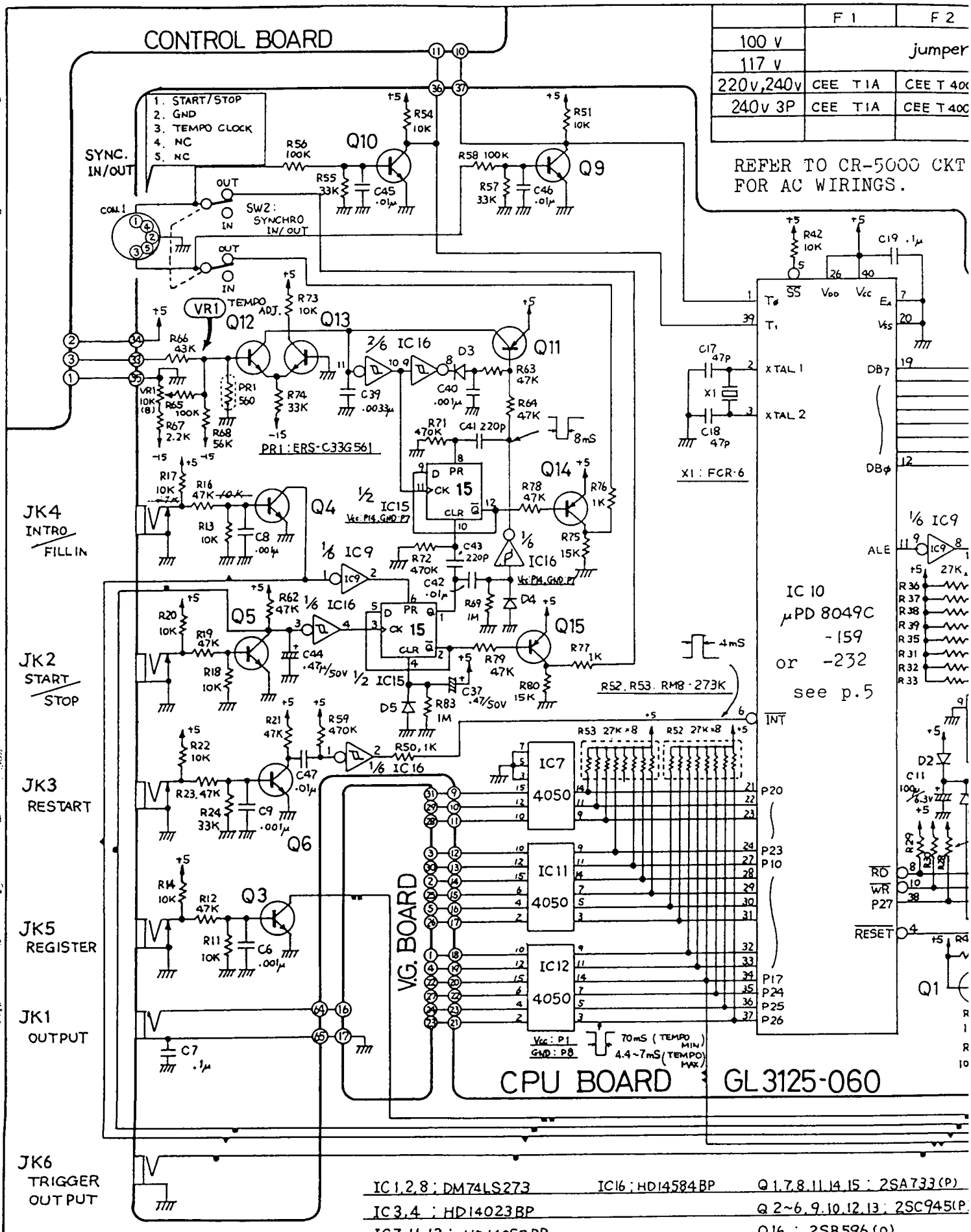
PIN NAME	PIN NO.	FUNCTION
TØ	1	NO APPLICATION (KEPT LOW)
T1	39	TEMPO CLOCK IN
INT	6	START/STOP SIGNAL IN
DATA BUS	12	KEPT HIGH
	13	KEPT LOW
	14	KEPT LOW
	15	KEPT LOW
	16-19	NO CONNECTION
		for Internal program initialization
PORT 1		
P10	27	7-SEGMENT LED LIGHT SIGNAL OUTPUTS
P11	28	
P12	29	
P13	30	
P14	31	
P15	32	
P16	33	
P17	34	NO CONNECTION
PORT 2		
P20-P23	21-24	NO CONNECTION
P24	35	(NOT IN USE)
P25	36	7-SEGMENT LED CONTROL SIGNAL OUTPUT
P26	37	
P27	38	

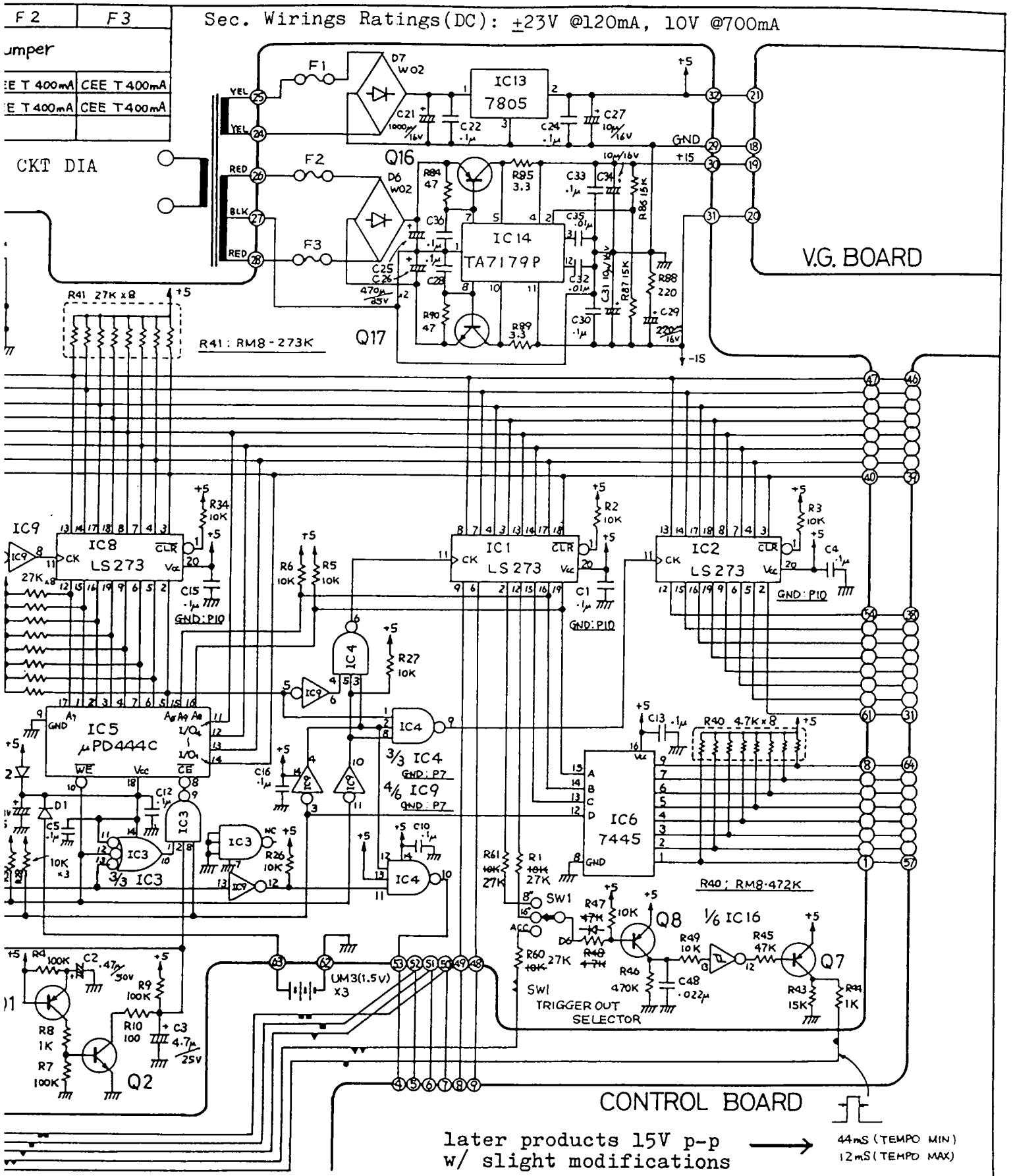
TEMPO DISPLAY (CR-8000 only)

uPD8048C IC3 on Control Brd counts Tempo Clocks derived from Q9 on CPU Brd whenever power is being fed to the CR-8000.
Since 24 tempo clocks are made equal to one ♩, actual tempo displayed is

$$\frac{\text{clocks per minute}}{24}$$

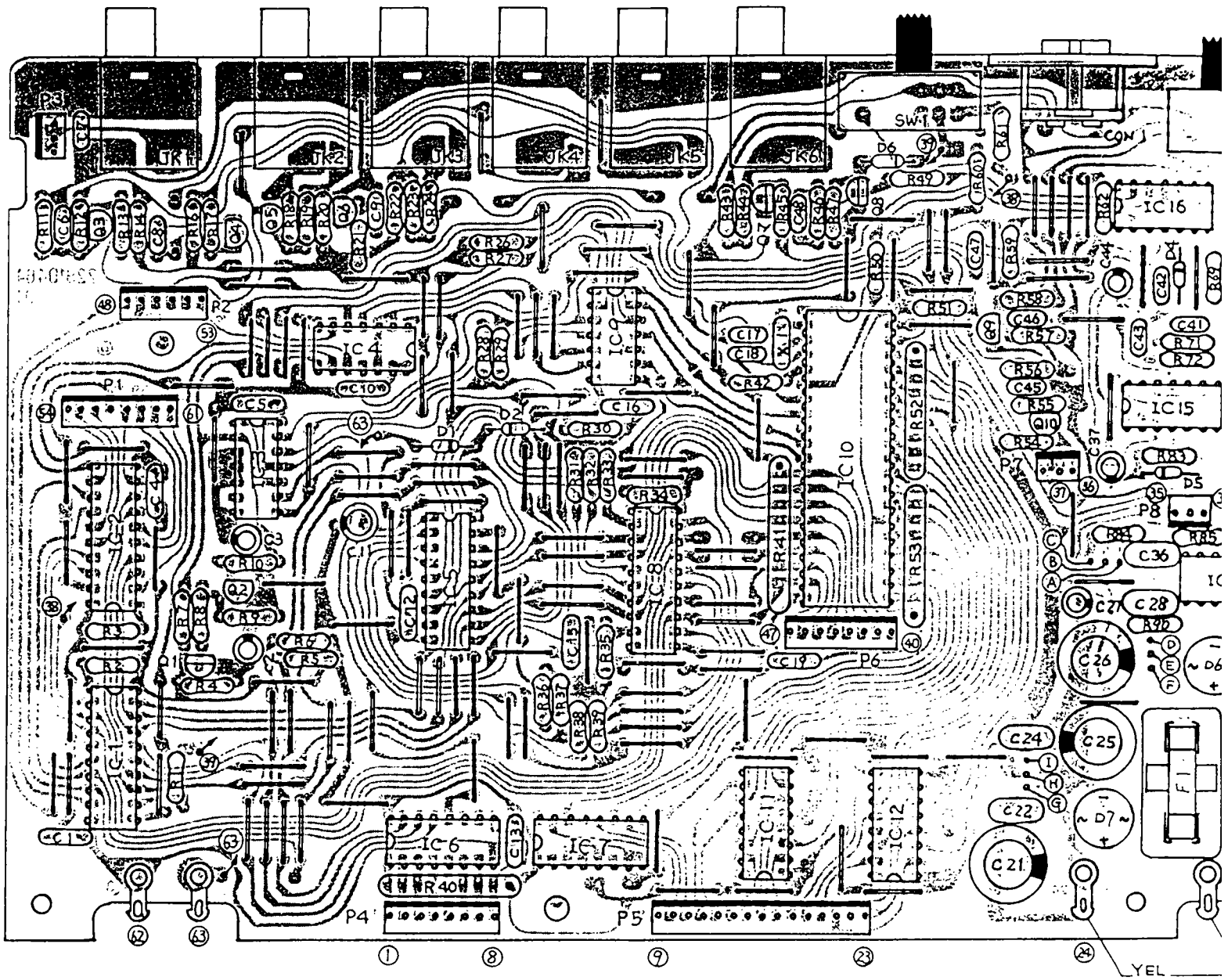
CPU performs an equivalent eq. in a short period and drives Q18-Q20 on Control Brd in synchronous with drive signals for 7 segments of display LEDs.
Upon rhythm running INT of CPU IC3 goes and stays negative with which CPU's internal count gate is disabled, then re-started at the first falling edge of the next tempo clock. This count break allows CPU to skip transitional tempo clock that is reset by a start signal.
If INT remains high after rhythm running, tempo display varies temporarily.


CONTROL BOARD
1. START/STOP
2. GND
3. TEMPO CLOCK
4. NC
5. NC
SYNC. IN/OUT
SW2: SYNCHRO IN/OUT
VR1 TEMPO ADJ.
PR1: ERS-C33G561
JK4 INTRO / FILL IN
JK2 START / STOP
JK3 RESTART
JK5 REGISTER
JK1 OUTPUT
JK6 TRIGGER OUT PUT
IC 10 μPD 8049C -159 or -232
see p.5
X1 : FCR-6
V.G. BOARD
CPU BOARD GL3125-060
REFER TO CR-5000 CKT FOR AC WIRINGS.
100 V
117 V
220v,240v
240v 3P
CEE T1A
CEE T40
jumper
IC 1,2,8 ; DM74LS273
IC3,4 ; HD14023BP
IC7,11,12 ; HD14050BP
IC16 ; HD14584BP
Q1,7,8,11,14,15 ; 2SA733(P)
Q2~6,9,10,12,13 ; 2SC945(P)
Q16 ; 2SB596(O)

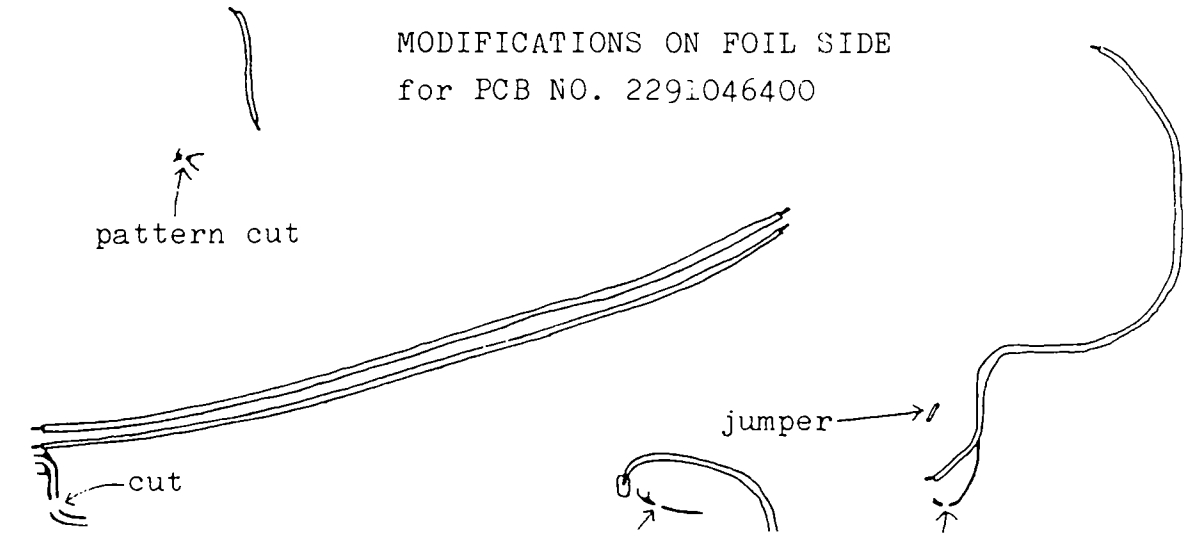

F2
F3
Jumper
CEE T400mA
CEE T400mA
CKT DIA
Sec. Wirings Ratings(DC): ±23V @120mA, 10V @700mA
F1
F2
F3
D7 W02
D6 W02
IC13 7805
IC14 TA7179P
Q16
Q17
V.G. BOARD
R41 27K x8
R41 : RM8-273K
IC8 LS273
IC1 LS273
IC2 LS273
IC5 μPD444C
IC6 7445
3/3 IC4
4/6 IC9
3/3 IC3
1/6 IC16
Q8
Q7
Q2
SW1
SW1 TRIGGER OUT SELECTOR
R40 4.7K x8
R40 : RM8-472K
UM3(1.5V) x3
CONTROL BOARD
later products 15V p-p
w/ slight modifications
44mS (TEMPO MIN)
12mS (TEMPO MAX)

CR-8000 CPU

TEMPO

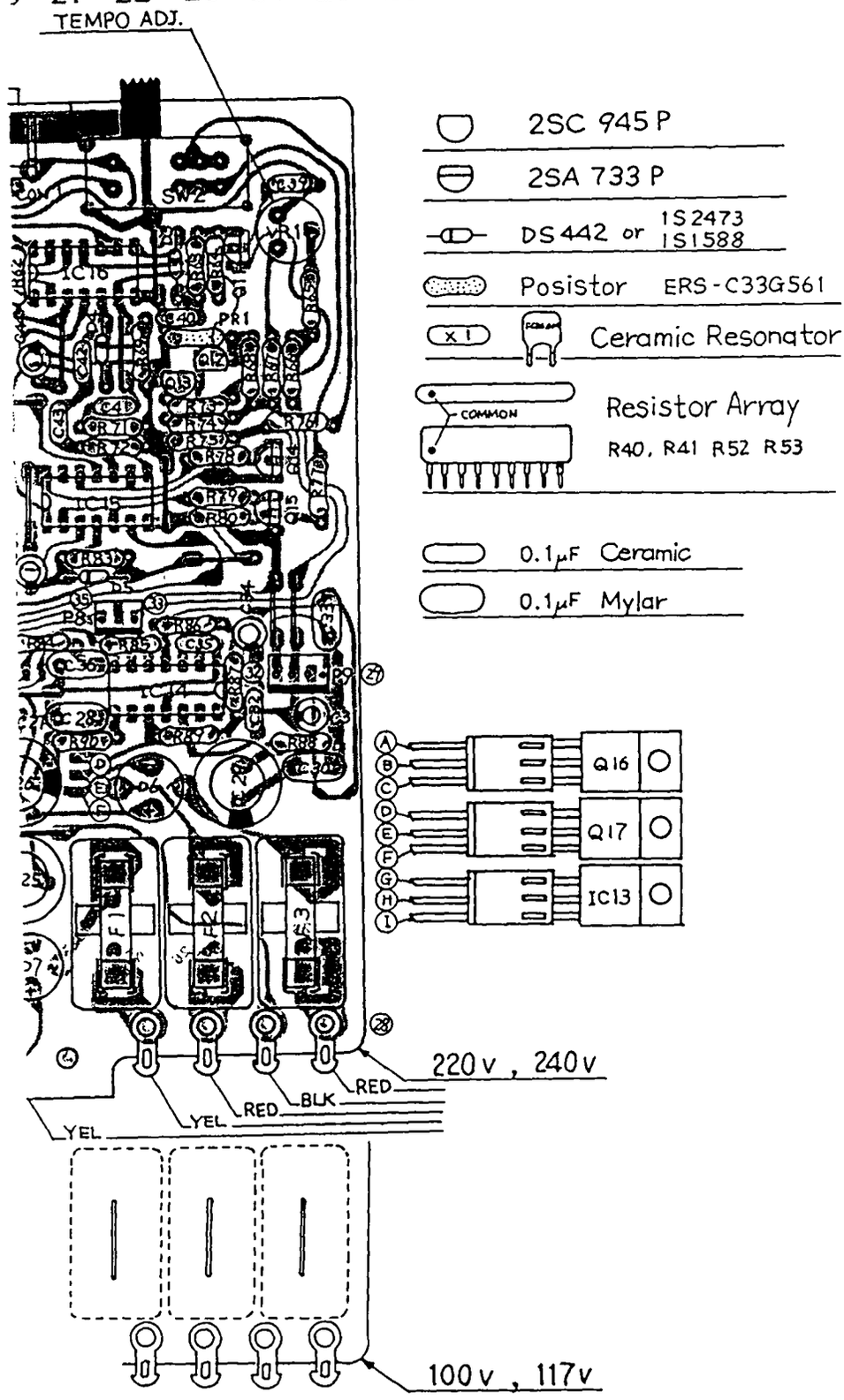


MODIFICATIONS ON FOIL SIDE
for PCB NO. 2291046400



CR-8000
CPU BOARD

GL3125-060
(731250600)
(pcb 2291046401)



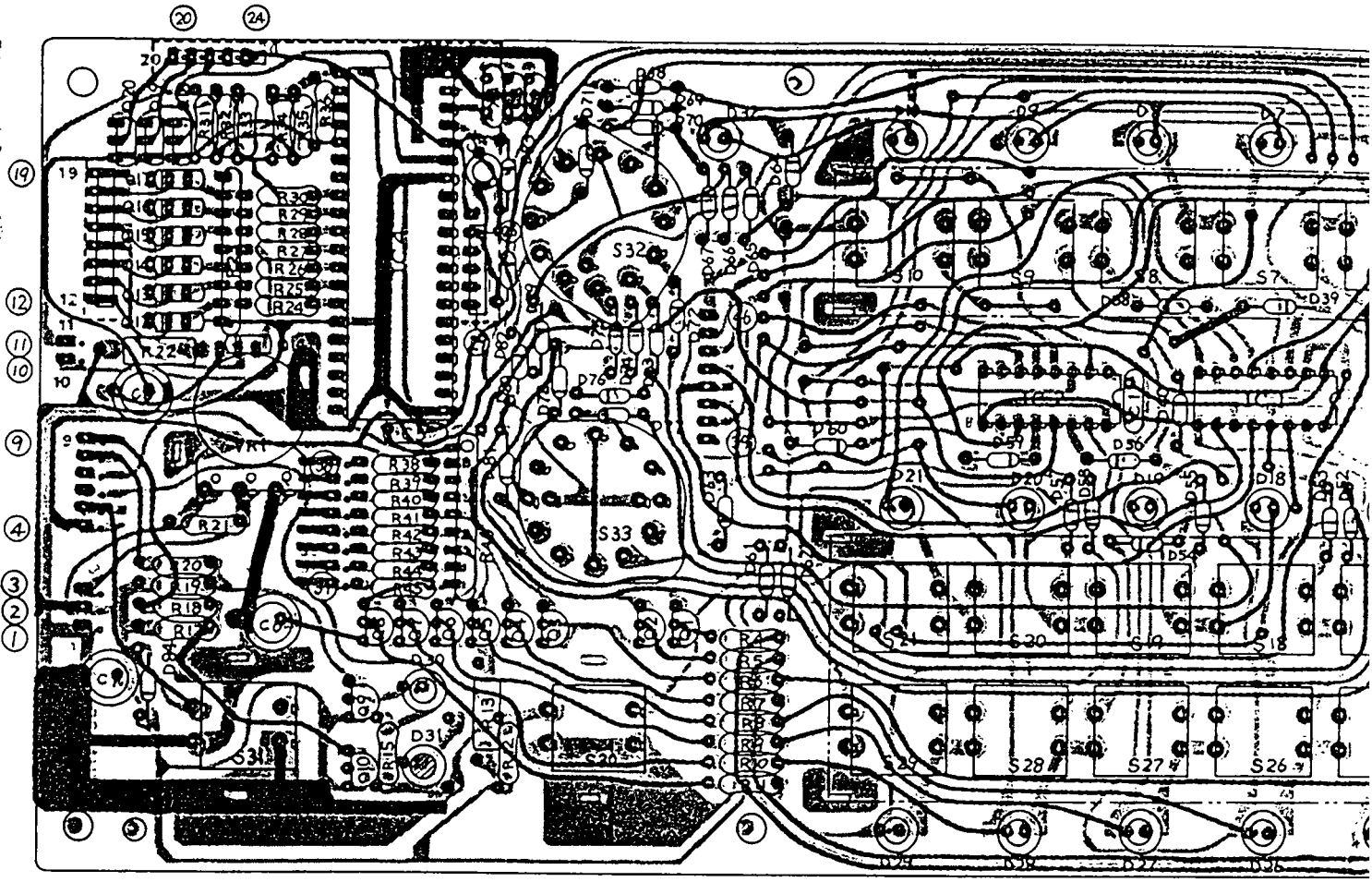
CHANGES IN COMPONENTS

Ensure trigger outputs at IC1 when low V_{OH}

LS273 is used.

R47	47k to 10k
R48	47k to D6
R1	10k to 27k
R61	10k to 27k
R60	10k to 27k

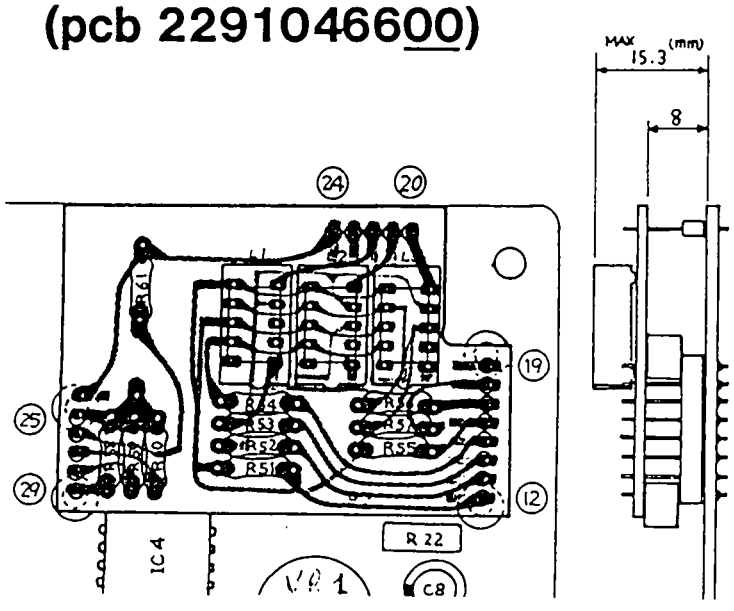
CONTROL BOARD GL3125-090 (7312509008) (pcb 2291



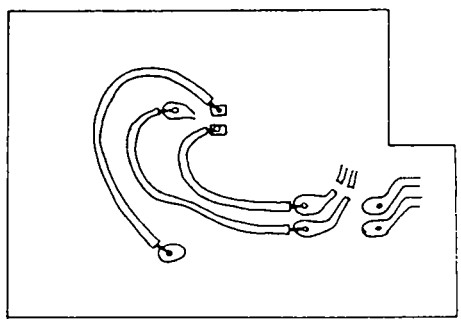
LED BOARD

(7312511001)

(pcb 2291046600)



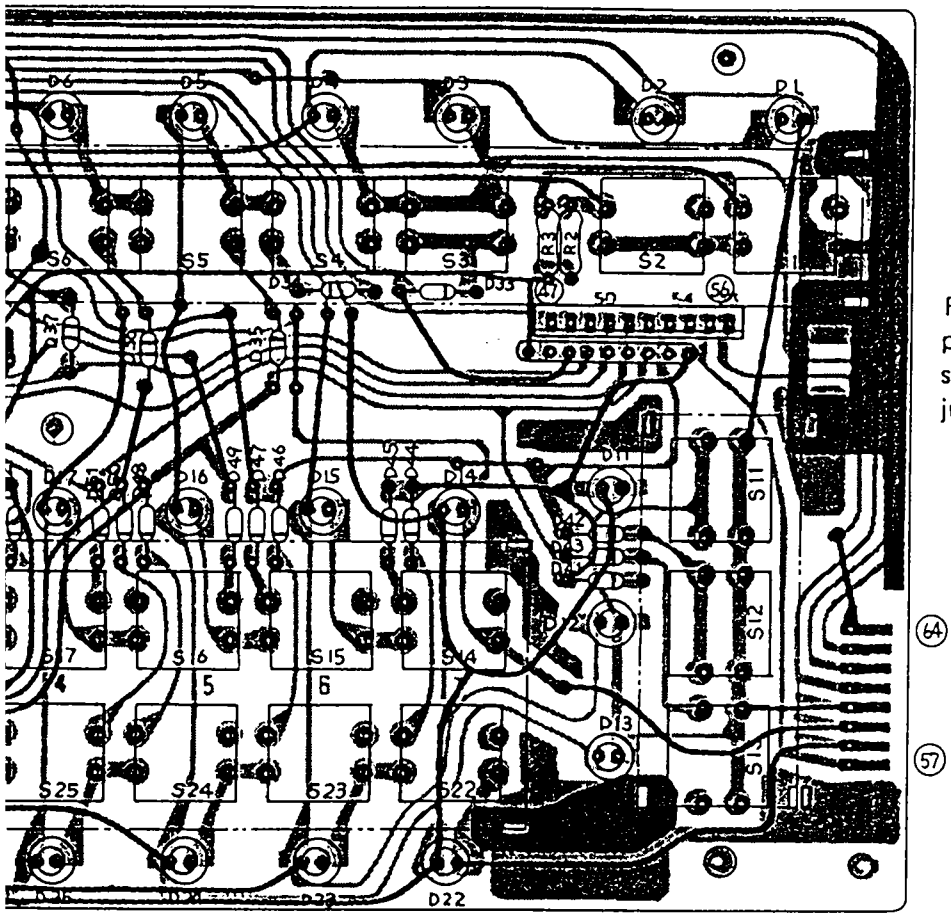
LED BOARD
on early products
pcb 2291046600
↑
without underscore
Pattern cuts, Jumpers



21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

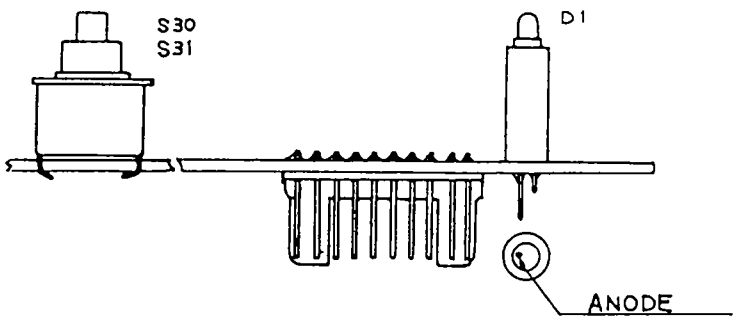
1046501) Serial Number 142650 and higher

(Viewed from the rear)

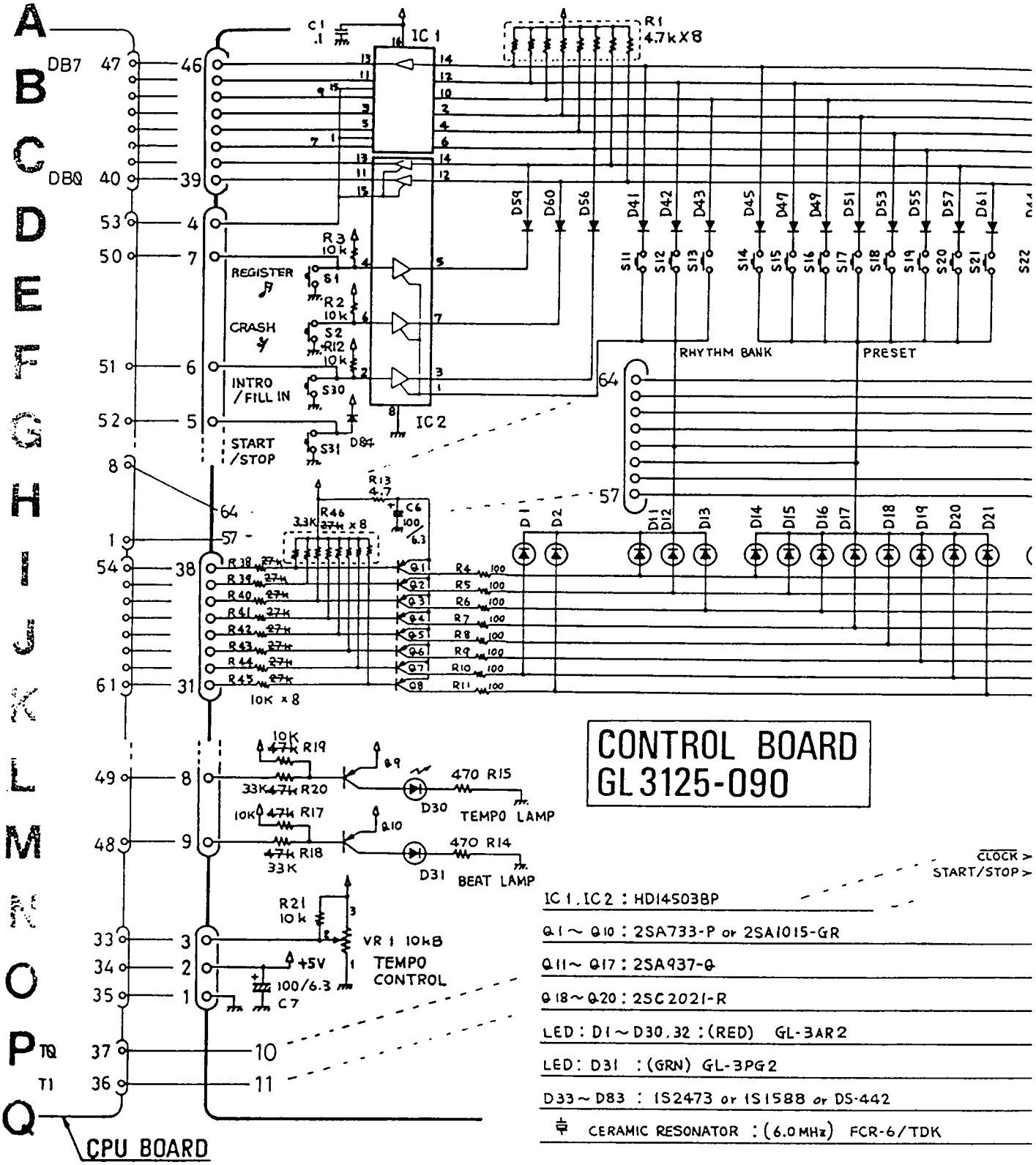


Refoer to p.16 for pcb 2291046500: surface mounting jumper wire.

CR-8000



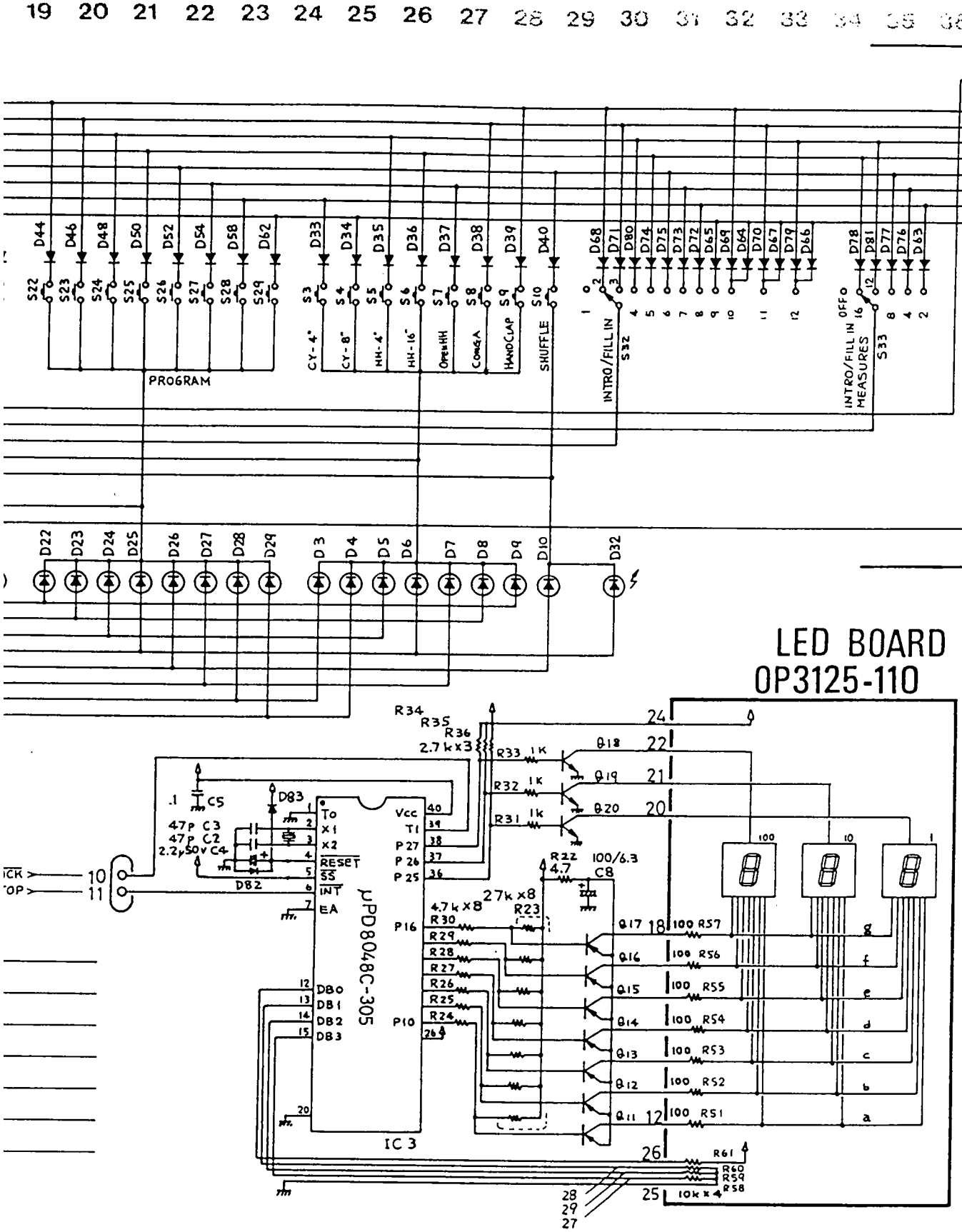
: DS442 or 1S1588, 1S2473	
: 2SA733P or 2SA1015GR	
: 2SA937Q	
: 2SC2021R	
X1 : CERAMIC RESONATOR (6.0MHz) FCR-6	
: LED GL-3PR2 (RED)	
: LED GL-3PG2 (GRN)	



CHANGES IN RESISTANCE With Serial Number 090900 and up

The changes eliminates possible dim lighting of LEDs due to insuffi at IC1 or IC2 on CPU board:

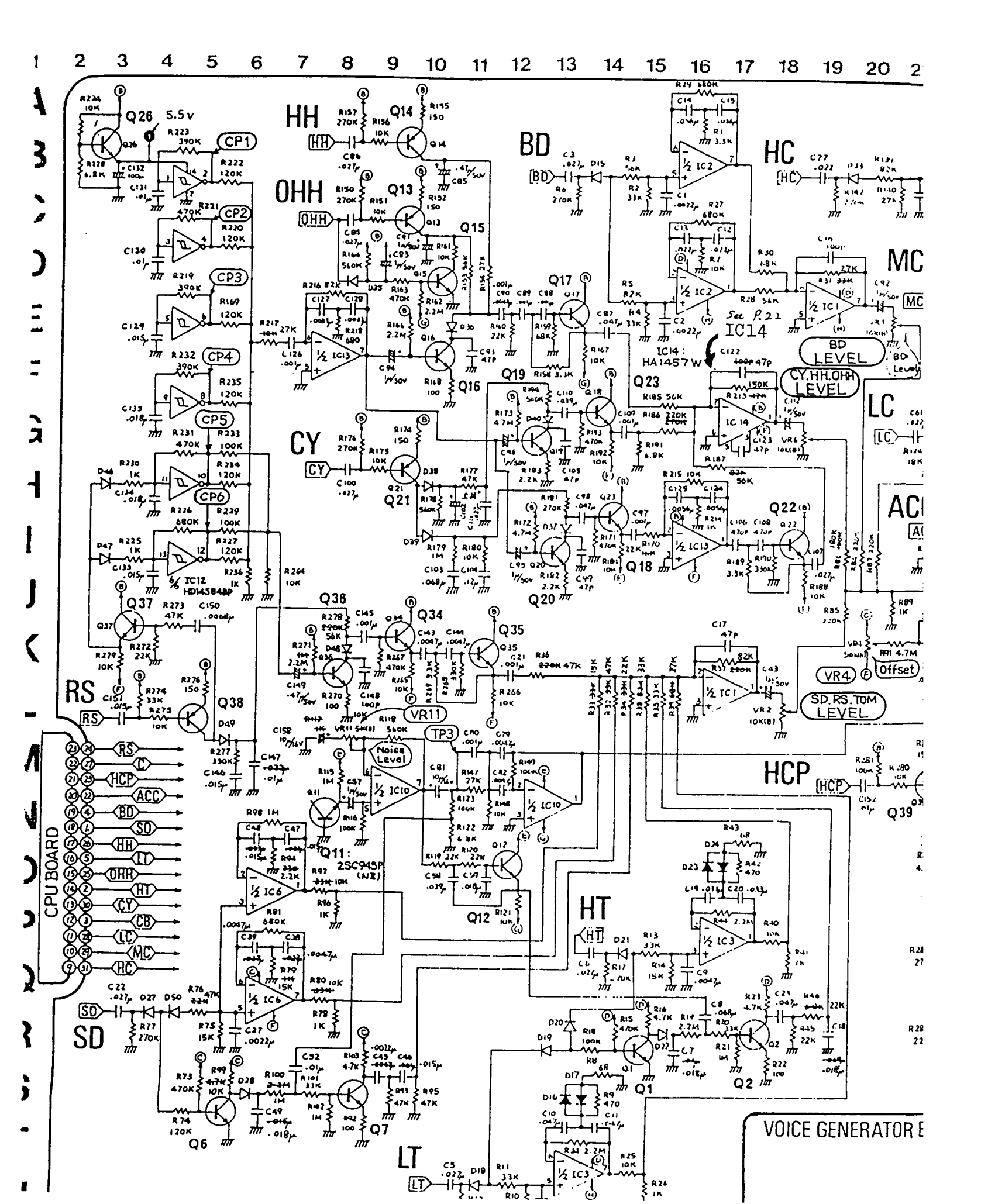
R38-R45: 27k to 10k R17, R19: 47k to 10k R18, R20: 47k to 3
Resistor Array R46: 27k to 3.3k

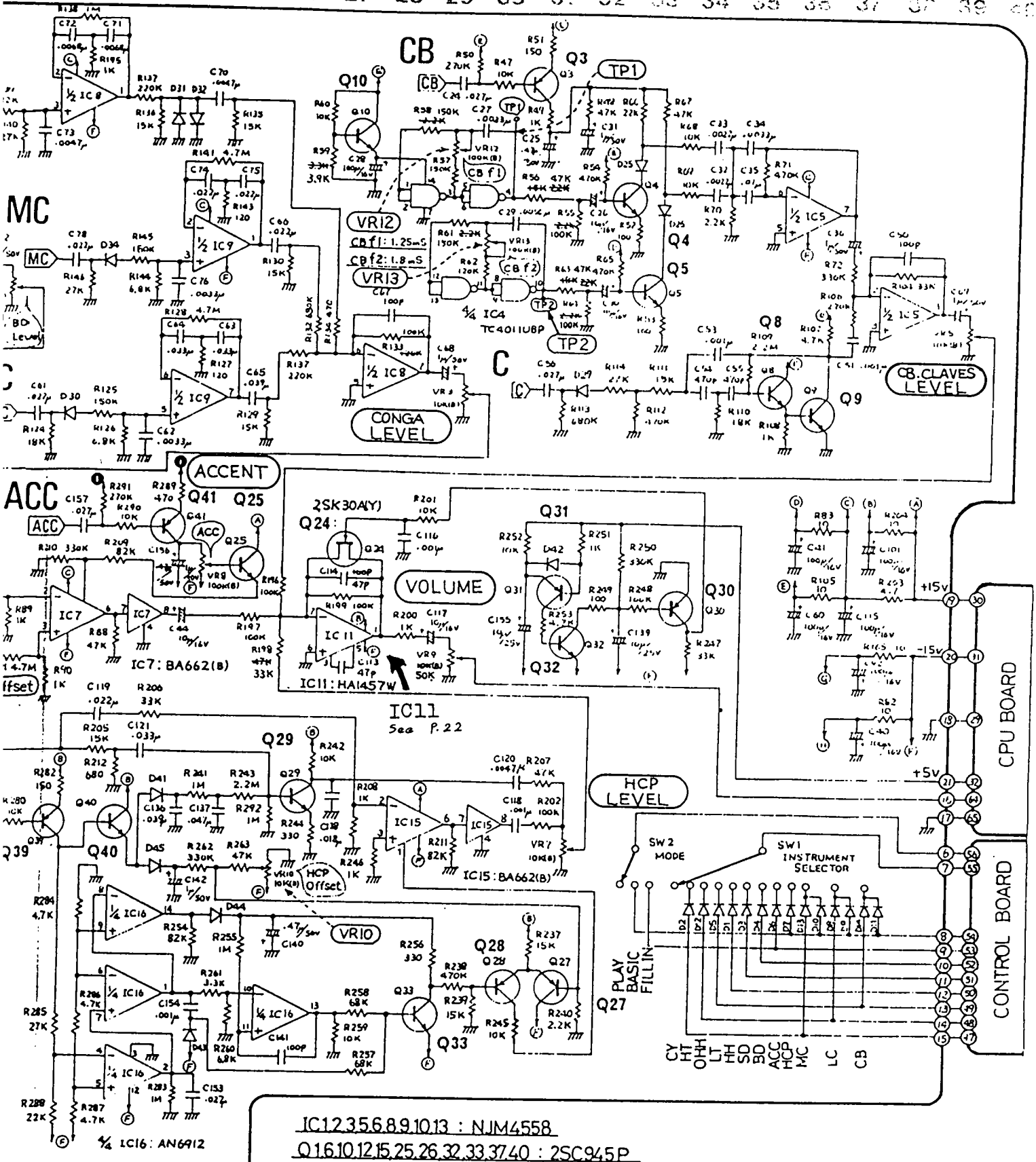


'ficient H level output

33k

CR-8000 CONTROL


HH
OHH
BD
HC
MC
CY
LC
RS
HCP
HT
SD
LT
Q26 5.5v
Q14
Q13
Q15
Q17
Q16
Q19
Q18
Q23
Q21
Q20
Q22
Q37
Q38
Q34
Q35
Q36
Q11 : 2SC945P (NEC)
Q12
Q39
Q1
Q2
Q6
Q7
IC14 : HA1457W
See P.22
BD LEVEL
CY.HH.OHH LEVEL
SD.RS.TOM LEVEL
VR4
Offset
Noise Level
VR11
TP3
CPU BOARD
RS
C
HCP
ACC
BD
SD
HH
LT
OHH
HT
CY
CB
LC
MC
HC
VOICE GENERATOR



IC1.2.3.5.6.8.9.10.13 : NJM4558

Q1.6.10.12.15.25.26.32.33.37.40 : 2SC945P

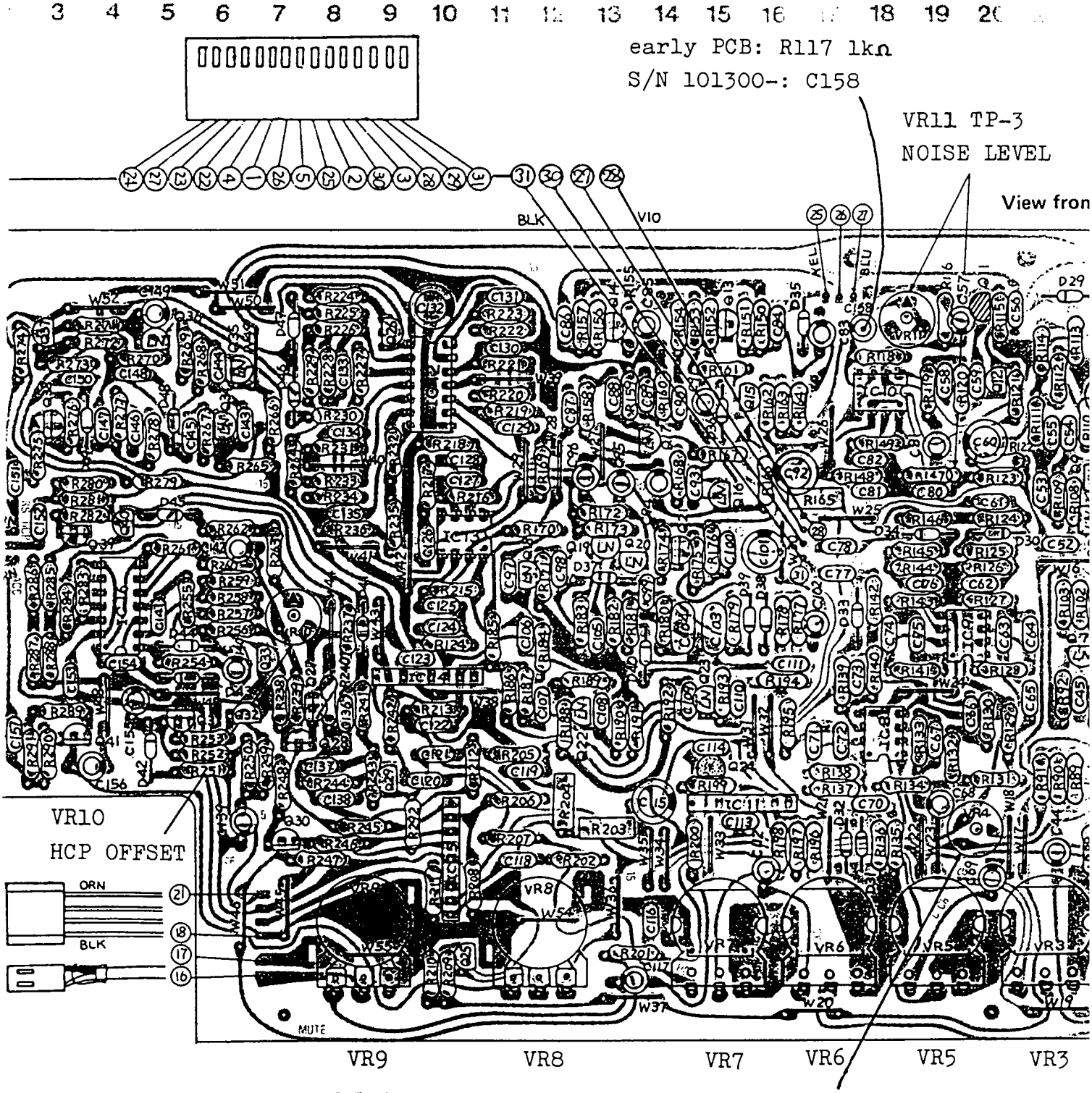
Q2.4.5.7~9.16~20.22.23.29.34~36 : 2SC 732 TM GR

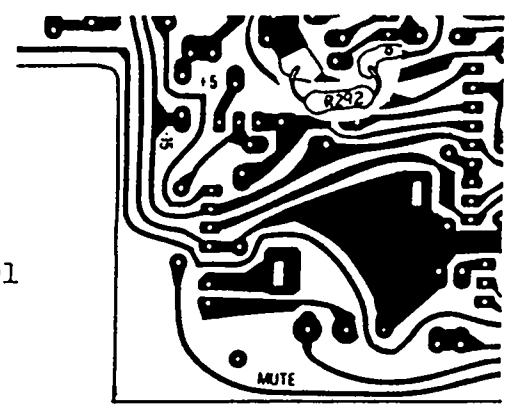
Q3.13.14.21.27.28.30.31.38.39.41 : 2SA733P

D16.17.23.24 : 1S188FM

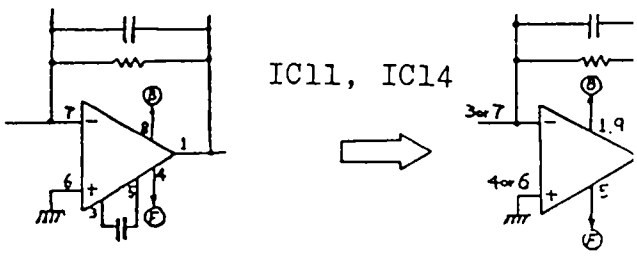
D1~15.18~22.25~50 : DS442 , 1S2473 or 1S1588

OR BOARD VG3125-120





surface
mounting
on PCB
2291046301



IC11, IC14

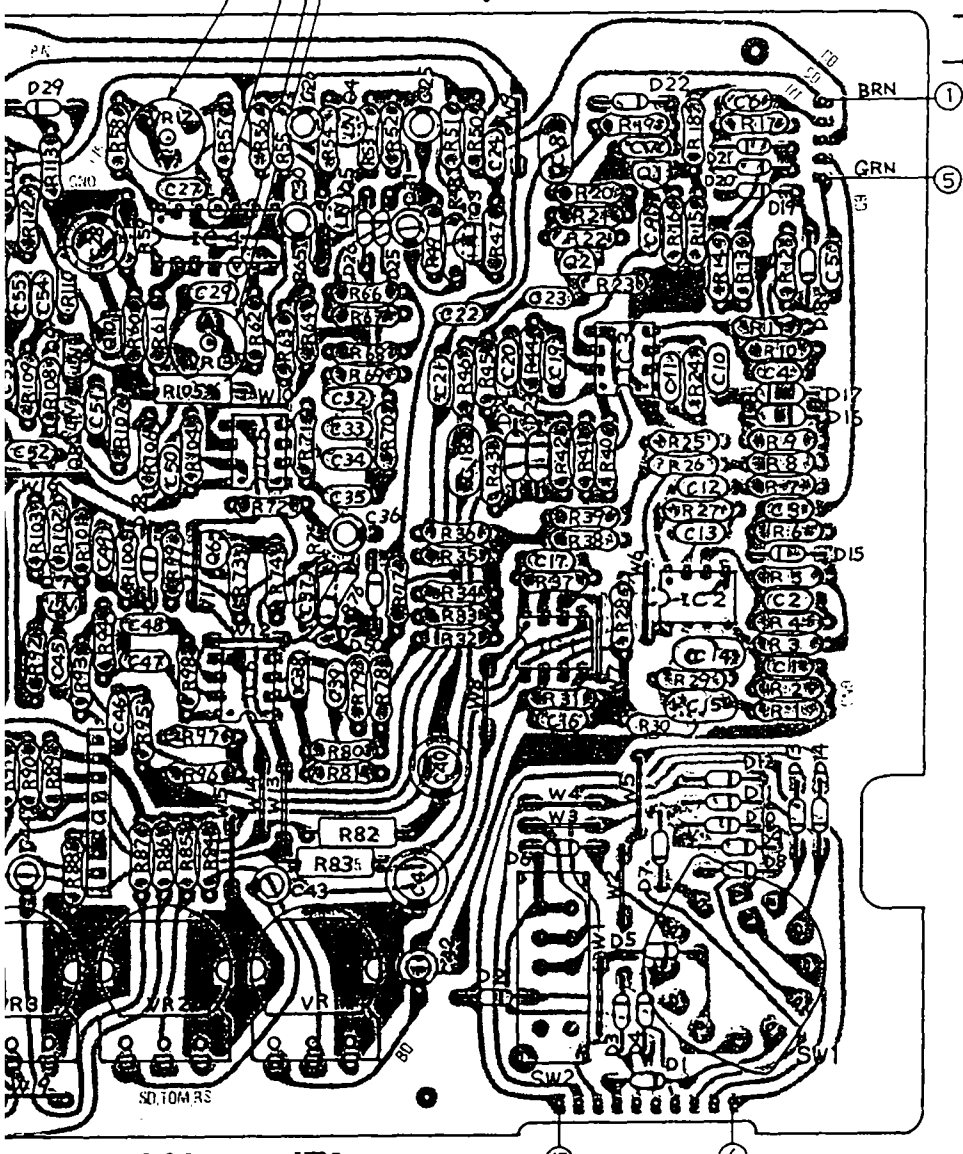
HA1457W (8 pins) or NJM4558S (

1 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

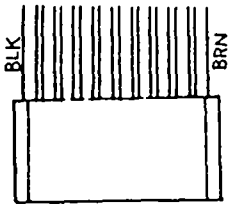
VR12 TP-1
CB FREQ

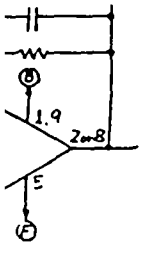
VR13 TP-2
CB FREQ

from foil side



R3 VR2 VR1 ⑮ ⑥





3S (9 pins) (See p. 22 for detail.)

2SC945-P
2SC732TM-GR
2SA733-P
2SC945-P(NZ)
2SK30A-Y
DS442, 1S2473 or 1S1588
1S188FM

CR-8000
VOICING BOARD
VG3125-120
(7312512007)
(pcb 2291046302)

CHANGES IN COMPONENTS

with S/N 090900
VR9 from 10k to 50k
Eliminates whizz sound upon power off.

with S/N 101300
R198(HCP) 47k to 33k

with S/N 111700
R55,56,58,61,63,64 resistances are increased to limit currents into IC4. This modification is mandatory when replacing defective IC4.

ALSO SEE CR-5000 VG BRD LAYOUT FOR OTHER MODIFICATIONS.

ADJUSTMENTS

CPU BOARD

RAM BACK UP BATTERIES (CR-8000 only)
Power switch must be turned OFF.
Connect 100 ohms across pins 18 (Vcc) and 9 (GND) of RAM IC5 or shunt meter (scope or voltmeter) inputs with 100 ohms. Confirm approx. 4V at pin 18.

TEMPO CLOCK

Allow at least 10 minutes for circuit thermal stabilization.

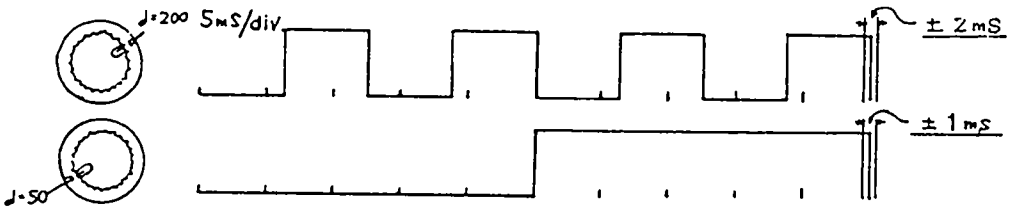
CR-5000

Connect scope to pin 1 of CPU (TP-1). Set scope time base to 5ms/div.
With TEMPO set at 200 adjust VR1 for 12.5ms/cycle (50ms/4 cycles).
Reset TEMPO to 50 and confirm that 1 cycle is 50m±1ms. If exceeds this limit, readjust VR1 for 1ms at the sacrifice of ±2ms error at TEMPO 200.

CR-8000

Turning TEMPO across its travel, confirm TEMPO DISPLAY; factory set ranges from 33±2 to 375±5%. Adjust VR1 as required.

NOTE: $\text{TEMPO} = \dfrac{2500}{\text{period of one tempo clock cycle (ms)}}$



VOICE BOARD

NOISE

Connect scope (1V/div, time base relatively slow) to TP-3.
Adjust VR11 for 2V p-p when measured at rather dense peaks.

CB

Connect scope to TP-1. Adjust VR12 for 1.25ms/cycle.
Connect scope to TP-2. Adjust VR13 for 1.8ms/cycle.

CY

See table right. Probing CP1-CP6 of oscillators IC6, confirm frequency ratios between adjacent two; they should be in 1.1-1.4 steps. Note that two oscillators generating on too close frequency will sound beating cymbal which can be eliminated by tailoring R and C listing on the table.

OFFSET

Controls set up - All VOICE LEVELs: FCCW; VOLUME, ACCENT: MAX; RYTHM: DISCO
Start the ryhthm. Monitoring through OUTPUT jack (scope or amp), adjust VR4 for minimum thump.

HCP (CR-8000 only)

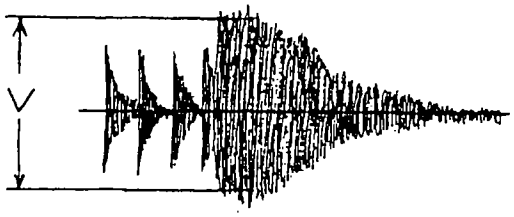
Controls set up - HCP VOICE LEVEL: FCW; VOLUME: MAX; ARRANGER: HAND CLAP

Connect scope V IN to OUTPUT jack and H (EXT) to HCP trig terminal 23.

Adjust VR10 for the below:

Serial number up to 101299 1V p-p

Serial number 101300 and up 2V p-p



		CHECK POINT	FREQUENCY (mS)(Hz) MIN	TYP	MAX	AMPLITUDE (V_{p-p}) MIN	TYP	MAX	DECAY TIME (mS) MIN	TYP	MAX	VOICE LEVEL CONTROL AT HOT TERMINAL: AMPLITUDE (V_{p-p}) MIN	TYP	MAX	DECAY TIME (mS) MIN	TYP	MAX	OUTPUT JACK AMPLITUDE (V_{p-p})
BD	H	IC2 PIN1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	6.7	8.0	9.6	77	96	115	1.2
	L	IC2 PIN7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110							
SD	H	IC6 PIN1	3.5 (286)	3.0 (333)	2.5 (400)	4.7	5.6	6.5	8	10	12	10.8	13.0	15.6	58	72	86	1.7
	L	IC6 PIN7	5.1 (196)	4.4 (227)	3.8 (266)	16.8	20.0	23.2	28	34	40							
LT		IC3 PIN7	10.9 (91.7)	9.4 (106)	8.0 (124)	24	27	28				7.0	8.8	10.6	160	200	240	1.3
HT		IC3 PIN1	7.6 (132)	6.6 (152)	5.6 (177)	24	27	28				4.6	6.0	7.4	120	150	180	1.0
LC		IC9 PIN7	5.8 (172)	5.0 (200)	4.3 (234)	24	27	28				6.4	8.0	9.6	136	170	200	1.3
MC		IC9 PIN1	3.9 (256)	3.4 (294)	2.9 (343)	24	27	28				2.2	2.8	3.4	80	100	120	0.4
HC		IC8 PIN1	1.67 (599)	1.45 (690)	1.24 (807)	24	27	28				3.4	4.3	5.1	12	15	18	0.6
CB		TP1.VR12 / TP2.VR13		1.25 (800)	1.80 (555)							1.1	1.3	1.6	29	36	43	1.3
C		Q9 COLLECTOR	0.49(2.01K)	0.43(2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5
HCP		VR10										0.4	0.6	0.8	72	90	108	2.0
RS												18.4	23	27.6	24	30	36	2.6
CY												6.3	7.6	9.1	300	380	450	1.2
HH												5.8	7.0	8.4	59	74	87	1.1
OHH												5.8	7.0	8.4	240	300	360	1.1

	CHECK POINT	R (KΩ)	C (μF)	FREQUENCY (mS)(Hz) MIN	TYP	MAX
RS CY HH OHH	CP 1	R233 390	C131 0.01	1.58 (631)	1.26 (794)	
	CP 2	R221 470	C130 0.01		1.54 (649)	
	CP 3	R219 390	C129 0.015		1.91 (524)	
	CP 4	R232 390	C135 0.018		2.25 (444)	
	CP 5	R231 470	C134 0.018		2.72 (368)	
	CP 6	R226 680	C133 0.015	4.20 (238)	3.53 (283)	

CR-5000 S/N with 101400 -

CR-8000 S/N with 101300 -

Ref. set up

VOICE LEVEL, VOLUME: MAX

ACCENT : MIN

(@ MAX, add 12dB to each: four times MIN.)

		CHECK POINT	FREQUENCY (mS)(Hz) MIN	TYP	MAX	AMPLITUDE (V_{p-p}) MIN	TYP	MAX	DECAY TIME (mS) MIN	TYP	MAX	VOICE LEVEL CONTROL AT HOT TERMINAL: AMPLITUDE (V_{p-p}) MIN	TYP	MAX	DECAY TIME (mS) MIN	TYP	MAX	OUTPUT JACK AMPLITUDE (V_{p-p})
BD	H	IC2 PIN1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	7.2	9.0	10.8	77	96	115	1.5
	L	IC2 PIN7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110							
SD	H	IC6 PIN1	4.4 (227)	3.8 (263)	3.2 (308)	24	27	28	54	64	74	9.6	12.0	14.4	58	72	86	1.7
	L	IC6 PIN7	5.1 (196)	4.4 (227)	3.8 (266)				30	40	50							
LT		IC3 PIN7	10.9 (91.7)	9.4 (106)	8.0 (124)							7.2	9.0	10.8	160	200	240	1.5
HT		IC3 PIN1	7.6 (132)	6.6 (152)	5.6 (177)							5.6	7.0	8.4	120	150	180	1.0
LC		IC9 PIN7	5.8 (172)	5.0 (200)	4.3 (234)							6.4	8.0	9.6	136	170	200	1.3
MC		IC9 PIN1	3.9 (256)	3.4 (294)	2.9 (343)							2.4	3.0	3.6	80	100	120	0.5
HC		IC8 PIN1	1.67 (599)	1.45 (690)	1.24 (807)							3.4	4.3	5.1	12	15	18	0.6
CB		TP1.VR12 / TP2.VR13		1.25 (800)	1.80 (555)							1.1	1.3	1.6	29	36	43	1.3
C		Q9 COLLECTOR	0.49(2.01K)	0.43(2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5
HCP		VR10										0.4	0.6	0.8	72	90	108	1.0
RS												10	13	16	24	30	36	1.5
CY												4.6	6.0	7.4	180	225	270	1.2
HH												3.4	4.3	5.1	47	59	71	1.1
OHH												3.4	4.3	5.1	140	180	220	1.1

CR-5000 S/N up to 101399

Controls set up - HCP VOICE LEVEL: FCW; VOLUME: MAX; ARRANGER: HAND CLAP
Connect scope V IN to OUTPUT jack and H (EXT) to HCP trig terminal 23.
Adjust VR10 for the below:

Serial number up to 101299 1V p-p
Serial number 101300 and up 2V p-p

			FREQUENCY (mS)(Hz)			AMPLITUDE (V_{p-p})			DECAY TIME (mS)			VOICE LEVEL CONTROL AT HOT TERMINAL: AMPLITUDE (V_{p-p})			VOICE LEVEL CONTROL AT HOT TERMINAL: DECAY TIME (mS)			OUTPUT JACK
		CHECK POINT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	AMPLITUDE (V_{p-p})
BD	H	IC2 PIN1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	6.7	8.0	9.6	77	96	115	1.2
	L	IC2 PIN7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110							
SD	H	IC6 PIN1	3.5 (286)	3.0 (333)	2.5 (400)	4.7	5.6	6.5	8	10	12	10.8	13.0	15.6	58	72	86	1.7
	L	IC6 PIN7	5.1 (196)	4.4 (227)	3.8 (266)	16.8	20.0	23.2	28	34	40							
LT		IC3 PIN7	10.9 (91.7)	9.4 (106)	8.0 (124)	24	27	28				7.0	8.8	10.6	160	200	240	1.3
HT		IC3 PIN1	7.6 (132)	6.6 (152)	5.6 (177)	24	27	28				4.6	6.0	7.4	120	150	180	1.0
LC		IC9 PIN7	5.8 (172)	5.0 (200)	4.3 (234)	24	27	28				6.4	8.0	9.6	136	170	200	1.3
MC		IC9 PIN1	3.9 (256)	3.4 (294)	2.9 (343)	24	27	28				2.2	2.8	3.4	80	100	120	0.4
HC		IC8 PIN1	1.67 (599)	1.45 (690)	1.24 (807)	24	27	28				3.4	4.3	5.1	12	15	18	0.6
CB		TP1.VR12 / TP2.VR13		1.25 (800) / 1.80 (555)								1.1	1.3	1.6	29	36	43	1.3
C		Q9 COLLECTOR	0.49 (2.01K)	0.43 (2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5
HCP		VR10										0.4	0.6	0.8	72	90	108	2.0
RS												18.4	23	27.6	24	30	36	2.6
CY												6.3	7.6	9.1	300	380	450	1.2
HH												5.8	7.0	8.4	59	74	89	1.1
OHH												5.2	7.0	8.4	240	300	360	1.1

	CHECK POINT	R (KΩ)	C (μF)	FREQUENCY (mS)(Hz) MIN	TYP	MAX
RS	CP 1	R223 390	C131 0.01	1.58 (631)	1.26 (794)	
	CP 2	R221 470	C130 0.01		1.54 (647)	
CY	CP 3	R224 390	C129 0.015		1.91 (524)	
HH	CP 4	R232 390	C135 0.018		2.25 (444)	
OHH	CP 5	R231 470	C134 0.018		2.72 (368)	
	CP 6	R226 680	C133 0.015	4.20 (238)	3.53 (283)	

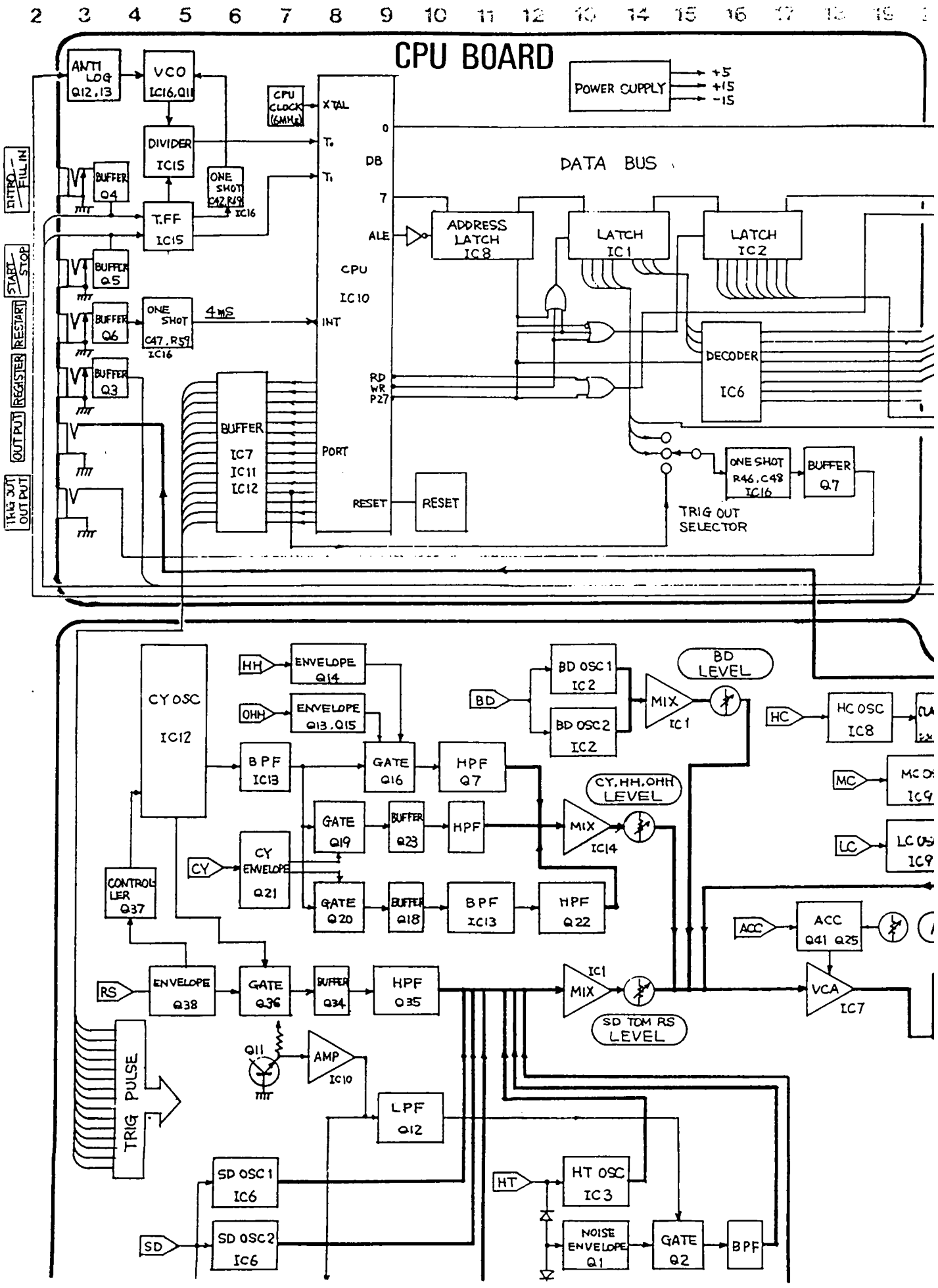
CR-5000 S/N with 101400 -
CR-8000 S/N with 101300 -

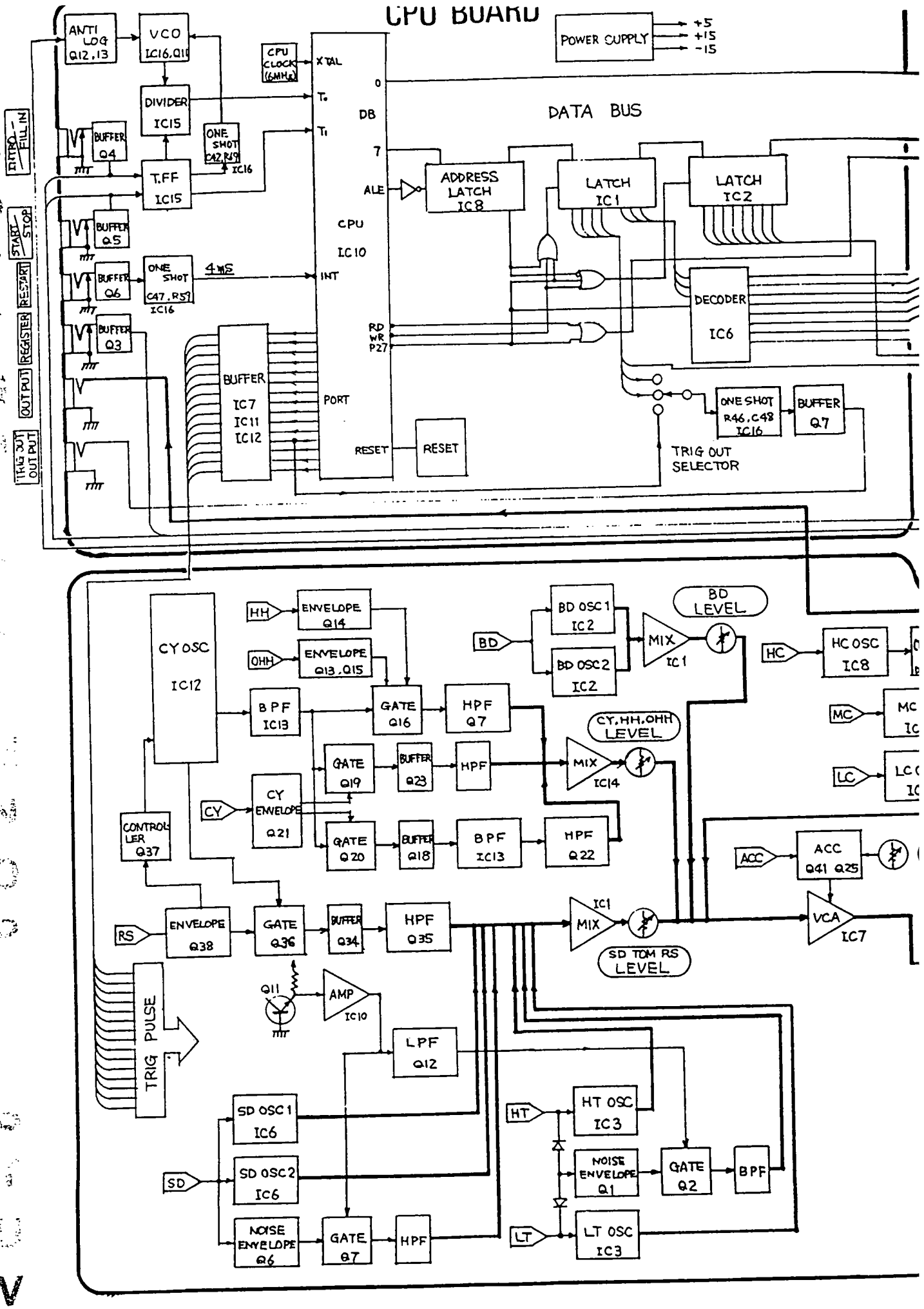
Ref. set up
VOICE LEVEL, VOLUME: MAX
ACCENT : MIN
(@ MAX, add 12dB to each: four times MIN.)

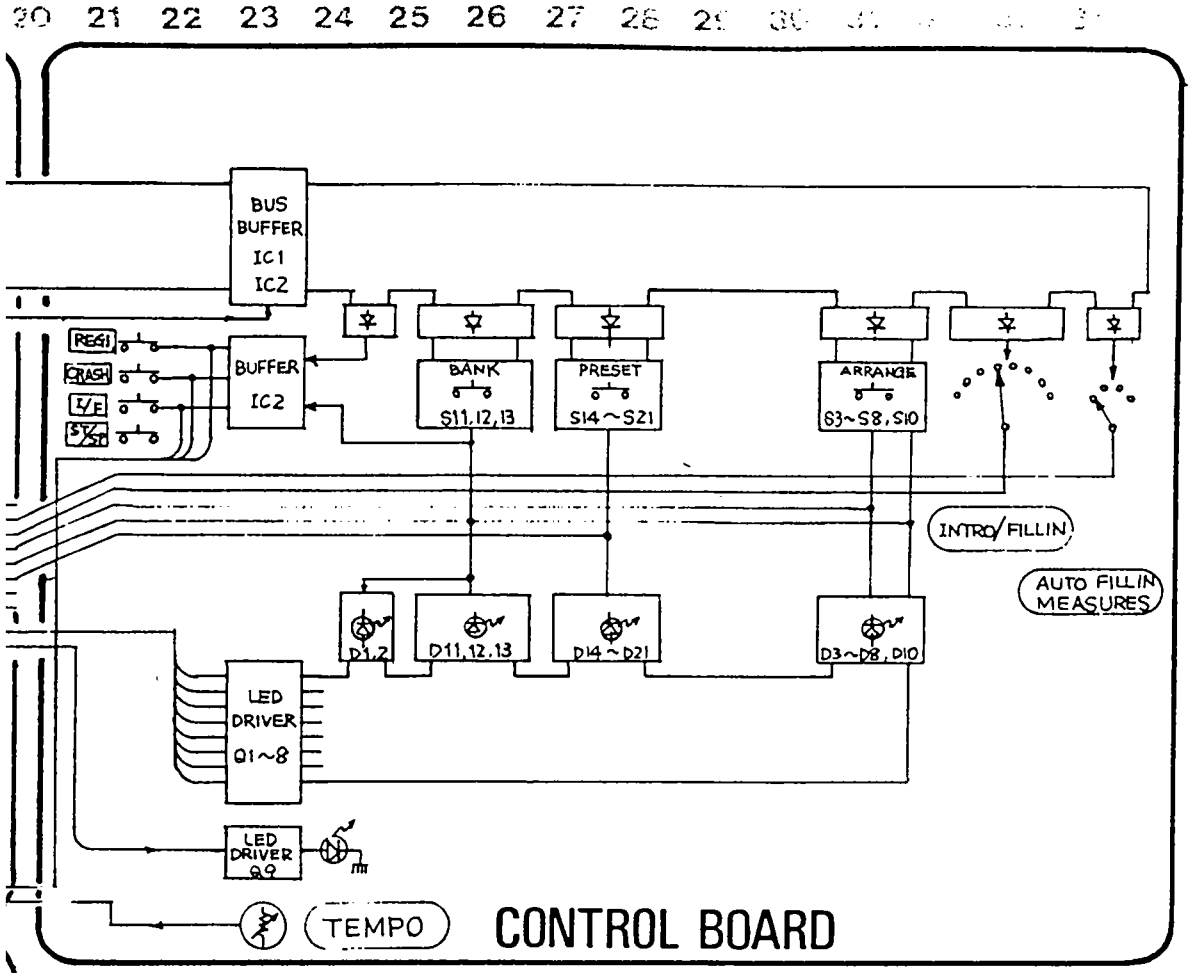
			FREQUENCY (mS)(Hz)			AMPLITUDE (V_{p-p})			DECAY TIME (mS)			VOICE LEVEL CONTROL AT HOT TERMINAL: AMPLITUDE (V_{p-p})			VOICE LEVEL CONTROL AT HOT TERMINAL: DECAY TIME (mS)			OUTPUT JACK
		CHECK POINT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	AMPLITUDE (V_{p-p})
BD	H	IC2 PIN1	13.2 (76)	11.4 (88)	9.7 (103)	6.8	7.6	8.4	30	40	50	7.2	9.0	10.8	77	96	115	1.5
	L	IC2 PIN7	20.2 (50)	17.5 (57)	15.0 (67)	11.9	13.2	14.5	90	100	110							
SD	H	IC6 PIN1	4.4 (227)	3.8 (263)	3.2 (308)	24	27	28	54	64	74	9.6	12.0	14.4	58	72	86	1.7
	L	IC6 PIN7	5.1 (196)	4.4 (227)	3.8 (266)				30	40	50							
LT		IC3 PIN7	10.9 (91.7)	9.4 (106)	8.0 (124)							7.2	9.0	10.8	160	200	240	1.5
HT		IC3 PIN1	7.6 (132)	6.6 (152)	5.6 (177)							5.6	7.0	8.4	120	150	180	1.0
LC		IC9 PIN7	5.8 (172)	5.0 (200)	4.3 (234)							6.4	8.0	9.6	136	170	200	1.3
MC		IC9 PIN1	3.9 (256)	3.4 (294)	2.9 (343)							2.4	3.0	3.6	80	100	120	0.5
HC		IC8 PIN1	1.67 (599)	1.45 (690)	1.24 (807)							3.4	4.3	5.1	12	15	18	0.6
CB		TP1.VR12 / TP2.VR13		1.25 (800) / 1.80 (555)								1.1	1.3	1.6	29	36	43	1.3
C		Q9 COLLECTOR	0.49 (2.01K)	0.43 (2.33K)	0.37 (2.72K)							1.3	1.6	1.9	11	14	17	1.5
HCP		VR10										0.4	0.6	0.8	72	90	108	1.0
RS												10	13	16	24	30	36	1.5
CY												2.5	3.5	4.5	300	380	450	1.0
HH												3.0	4.0	5.0	59	74	89	1.0
OHH												3.0	4.0	5.0	240	300	360	1.0

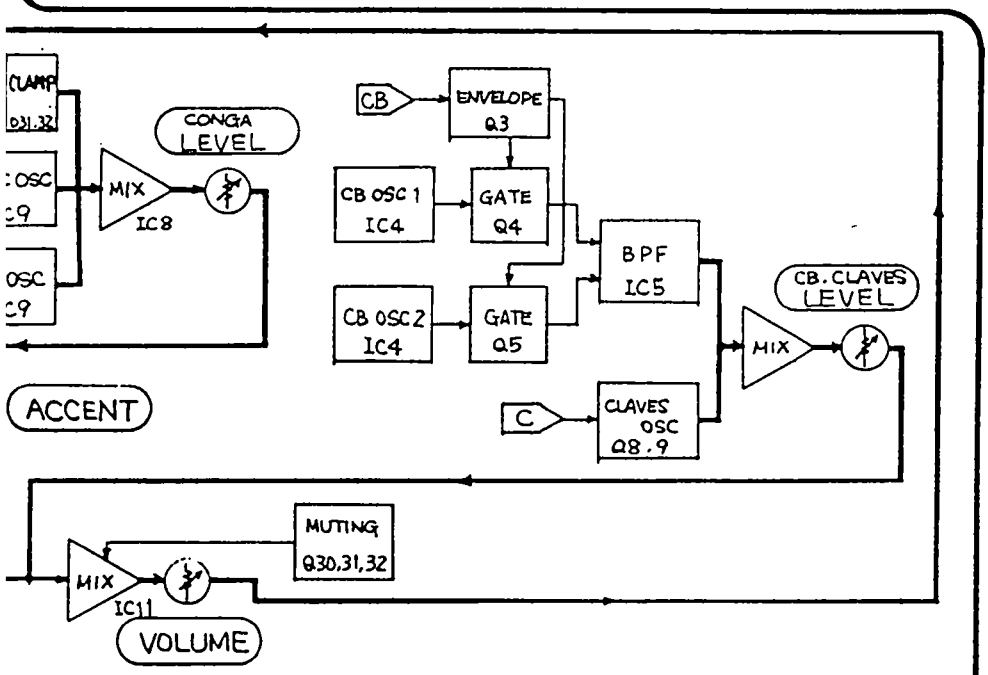
CR-5000 S/N up to 101399
CR-8000 S/N up to 101299

See table above for RS, CY, HH and OHH frequencies.

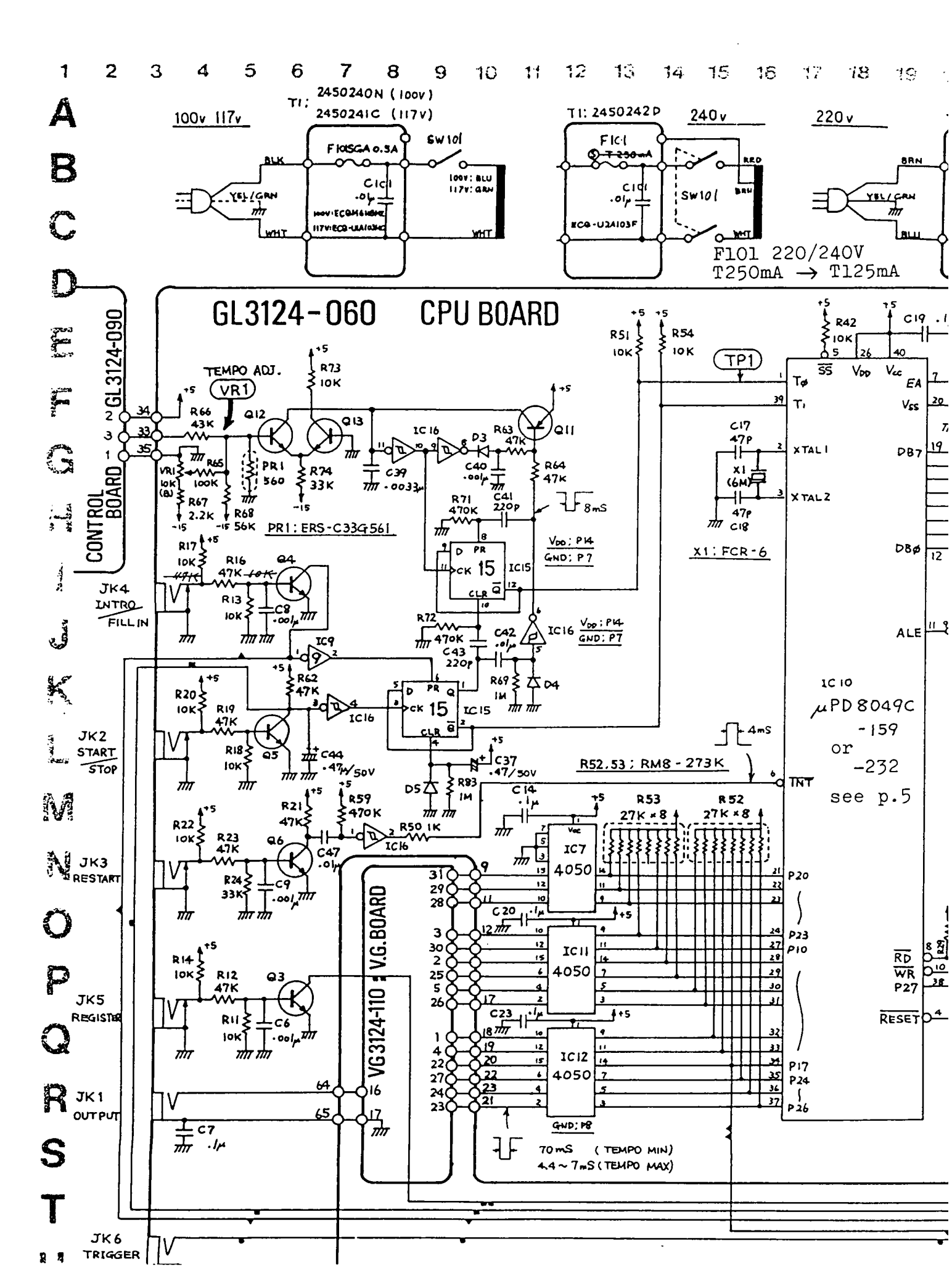

CPU BOARD
POWER SUPPLY
+5
+15
-15
DATA BUS
ANTI LOG Q12,13
VCO IC16,Q11
DIVIDER IC15
CPU CLOCK (6MHz)
XTAL
T0
T1
DB
7
ALE
ADDRESS LATCH IC8
LATCH IC1
LATCH IC2
BUFFER Q4
ONE SHOT C42,R49 IC16
T.FF IC15
BUFFER Q5
BUFFER Q6
ONE SHOT C47,R59 IC16
4mS
INT
CPU IC10
RD
WR
P27
DECODER IC6
BUFFER Q3
BUFFER IC7 IC11 IC12
PORT
RESET
RESET
ONE SHOT R46,C48 IC16
BUFFER Q7
TRIG OUT SELECTOR
INTRO-FILL IN
START STOP
RESTART
REGISTER
OUT PUT
TRIG OUT OUT PUT
CY OSC IC12
HH
ENVELOPE Q14
OHH
ENVELOPE Q13,Q15
BPF IC13
GATE Q16
HPF Q7
GATE Q19
BUFFER Q23
HPF
CY
CY ENVELOPE Q21
GATE Q20
BUFFER Q18
BPF IC13
HPF Q22
CONTROL LER Q37
BD
BD OSC1 IC2
BD OSC2 IC2
MIX IC1
BD LEVEL
CY,HH,OHH LEVEL
MIX IC14
HC
HC OSC IC8
MC
LC
ACC
ACC Q41 Q25
VCA IC7
RS
ENVELOPE Q38
GATE Q36
BUFFER Q34
HPF Q35
IC1 MIX
SD TOM RS LEVEL
Q11
AMP IC10
TRIG PULSE
LPF Q12
SD OSC1 IC6
SD OSC2 IC6
SD
HT
HT OSC IC3
NOISE ENVELOPE Q1
GATE Q2
BPF


CPU BOARD
POWER SUPPLY
+5
+15
-15
ANTI LOG Q12,13
VCO IC16,Q15
CPU CLOCK (6MHz)
XTAL
DIVIDER IC15
T0
T1
DB
DATA BUS
7
ALE
ADDRESS LATCH IC8
LATCH IC1
LATCH IC2
BUFFER Q4
ONE SHOT C42,R59 IC16
T.FF IC15
INTRO-FILL IN
START-STOP
RESTART
REGISTER
OUT PUT
TRIG OUT OUT PUT
BUFFER Q5
BUFFER Q6
ONE SHOT C47,R57 IC16
4mS
CPU IC10
INT
DECODER IC6
RD
WR
P27
BUFFER Q3
BUFFER IC7 IC11 IC12
PORT
RESET
RESET
ONE SHOT R46,C48 IC16
BUFFER Q7
TRIG OUT SELECTOR
CY OSC IC12
HH
ENVELOPE Q14
OHH
ENVELOPE Q13,Q15
BD
BD OSC1 IC2
BD OSC2 IC2
MIX IC1
BD LEVEL
HC
HC OSC IC8
MC
LC
BPF IC13
GATE Q16
HPF Q7
GATE Q19
BUFFER Q23
HPF
CY,HH,OHH LEVEL
MIX IC14
CY
CY ENVELOPE Q21
CONTROLLER Q37
GATE Q20
BUFFER Q18
BPF IC13
HPF Q22
ACC
ACC Q41 Q25
RS
ENVELOPE Q38
GATE Q36
BUFFER Q34
HPF Q35
IC1
MIX
VCA IC7
SD TOM RS LEVEL
TRIG PULSE
Q11
AMP IC10
LPF Q12
SD OSC1 IC6
SD OSC2 IC6
NOISE ENVELOPE Q6
GATE Q7
HPF
SD
HT
HT OSC IC3
NOISE ENVELOPE Q1
GATE Q2
BPF
LT
LT OSC IC3





CR-5000 BLOCK DIAGRAM

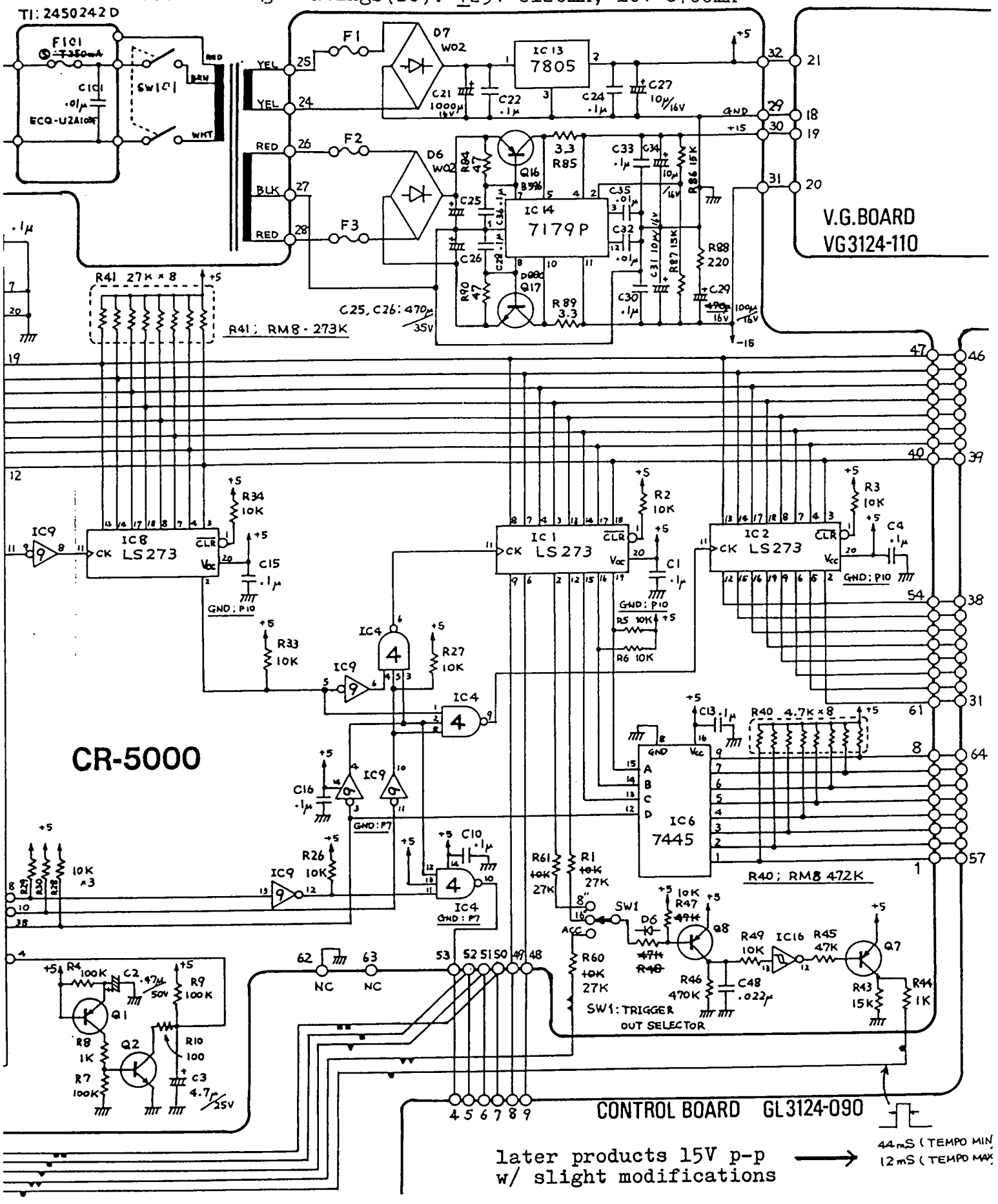

T1: 2450240N (100v)
2450241C (117v)
100v 117v
F1(0.5A
SW101
C101
.01μ
100v: BLU
117v: GRN
BLK
YEL/GRN
WHT
T1: 2450242P
240v
F101
T250mA
C101
.01μ
ECQ-U2A103F
SW101
RED
BRN
WHT
220v
BRN
YEL/GRN
BLU
F101 220/240V
T250mA → T125mA
GL3124-060 CPU BOARD
GL3124-090
CONTROL BOARD
TEMPO ADJ.
VR1
PR1: ERS-C33G561
JK4 INTRO FILL IN
JK2 START STOP
JK3 RESTART
JK5 REGISTER
JK1 OUTPUT
JK6 TRIGGER
VG3124-110
V.G.BOARD
VDD: P14
GND: P7
X1: FCR-6
IC10
μPD8049C
-159
or
-232
see p.5
R52.53: RM8-273K
GND: P8
70mS (TEMPO MIN)
4.4~7mS (TEMPO MAX)
8mS
4mS
TP1
IC7 4050
IC11 4050
IC12 4050
IC15
IC16
R53 27K×8
R52 27K×8
P20
P23
P10
P17
P24
P26
P27
RD
WR
RESET
INT
XTAL1
XTAL2
DB7
DB0
ALE
EA
VSS
VDD
VCC
SS

CR-5000/8000

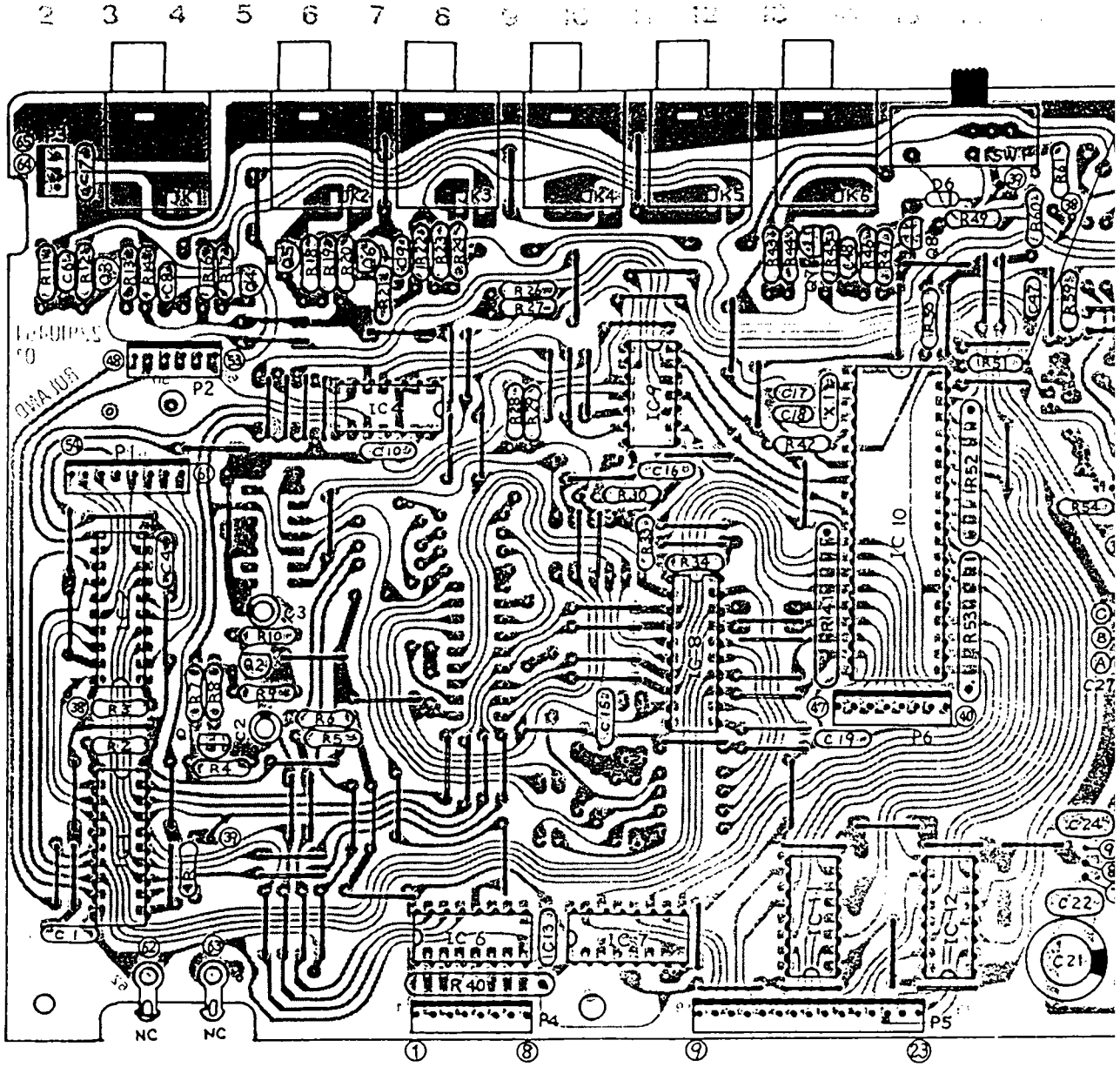
DEC.8,1981

20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

Sec. Wirings Ratings(DC): ±23V @120mA, 10V @700mA



C.8,1981



240v

SOME MODIFICATIONS
FOR PCB 2291046400
AT FOIL SIDE
SEE CR-8000 LAYOUT

	F1	F2	F3
100V	jumper	jumper	jumper
117V	jumper	jumper	jumper
220V, 240V	CEE T1A	CEE T400mA	CEE T400mA
240V 3P	CEE T1A	CEE T400mA	CEE T400mA

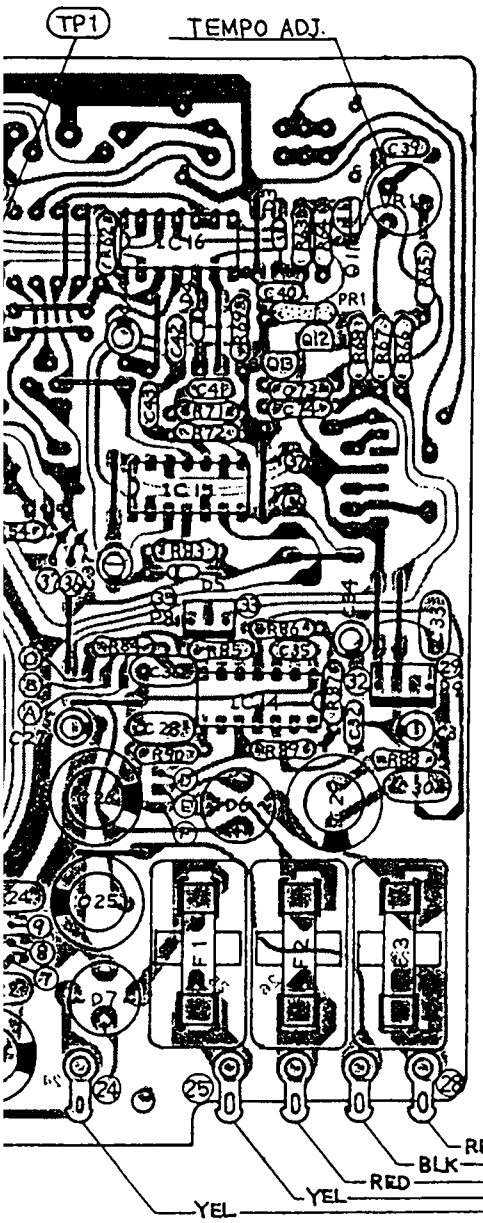
BLU—

BRN—

YEL/GRN—

IC1,2,8 : DM74LS273
IC4 : HD14023BP
IC6 : HD7445
IC7 : HD14050BP
IC15 : HD14013BP
IC9 : HD74LS04P
D3~5 : DS442 or IS2473 IS1598
IC13 : μA7805UC
IC14 : TA7179P
IC16 : HD14584BP
Q1,7,8,11 : 2SA733(P)
Q2~6,12,13 : 2SC945(P)
Q16 : 2SB596(O)
Q17 : 2SD880(Y)

18 19 20 21 22 23 24 25 26 27 28 29 30



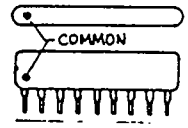
2SC 945 P

2SA 733 P

DS442 or 1S2473 1S1588

Posistor ERS-C33G561

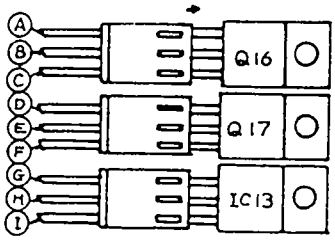
X1 Ceramic Resonator



Resistor Array
R40, R41, R52, R53

0.1μF Ceramic

0.1μF Mylar



G = 7
H = 8
I = 9

CR-5000
CPU BOARD
GL-3124-060
(7312406008)
(pcb 2291046401)

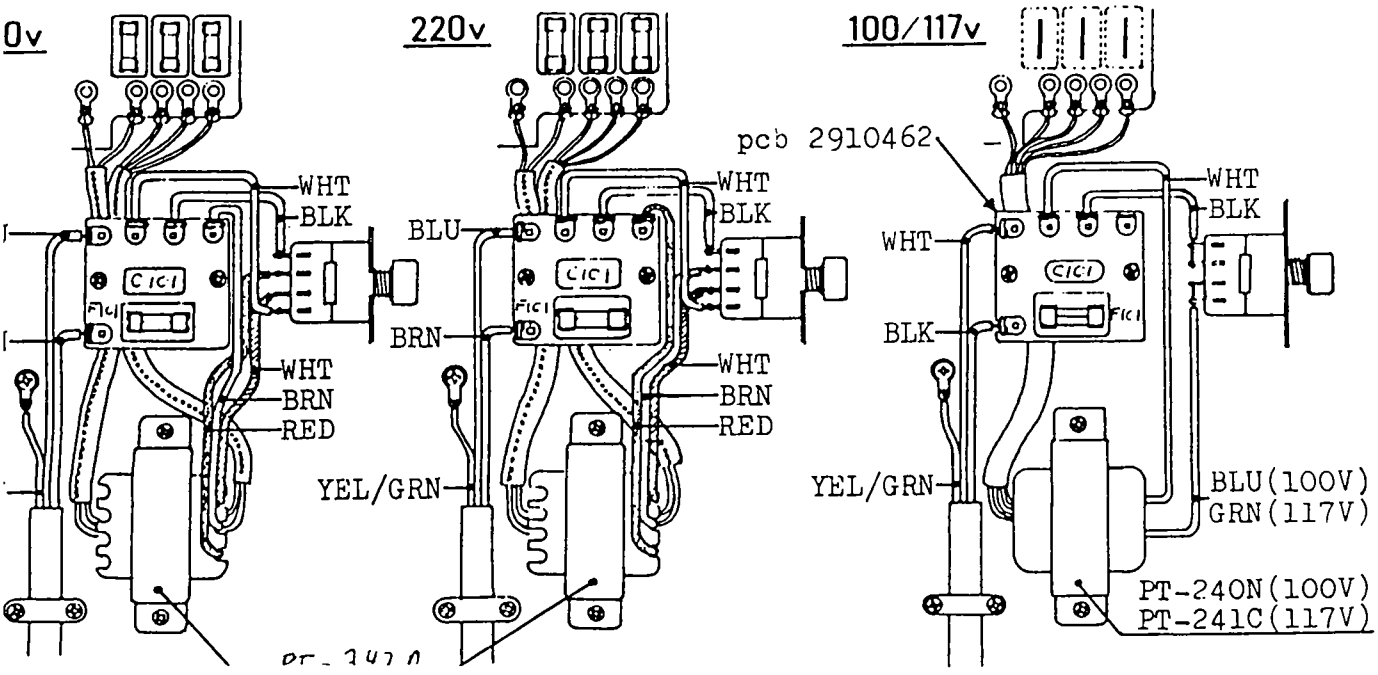
CHANGES IN COMPONENTS

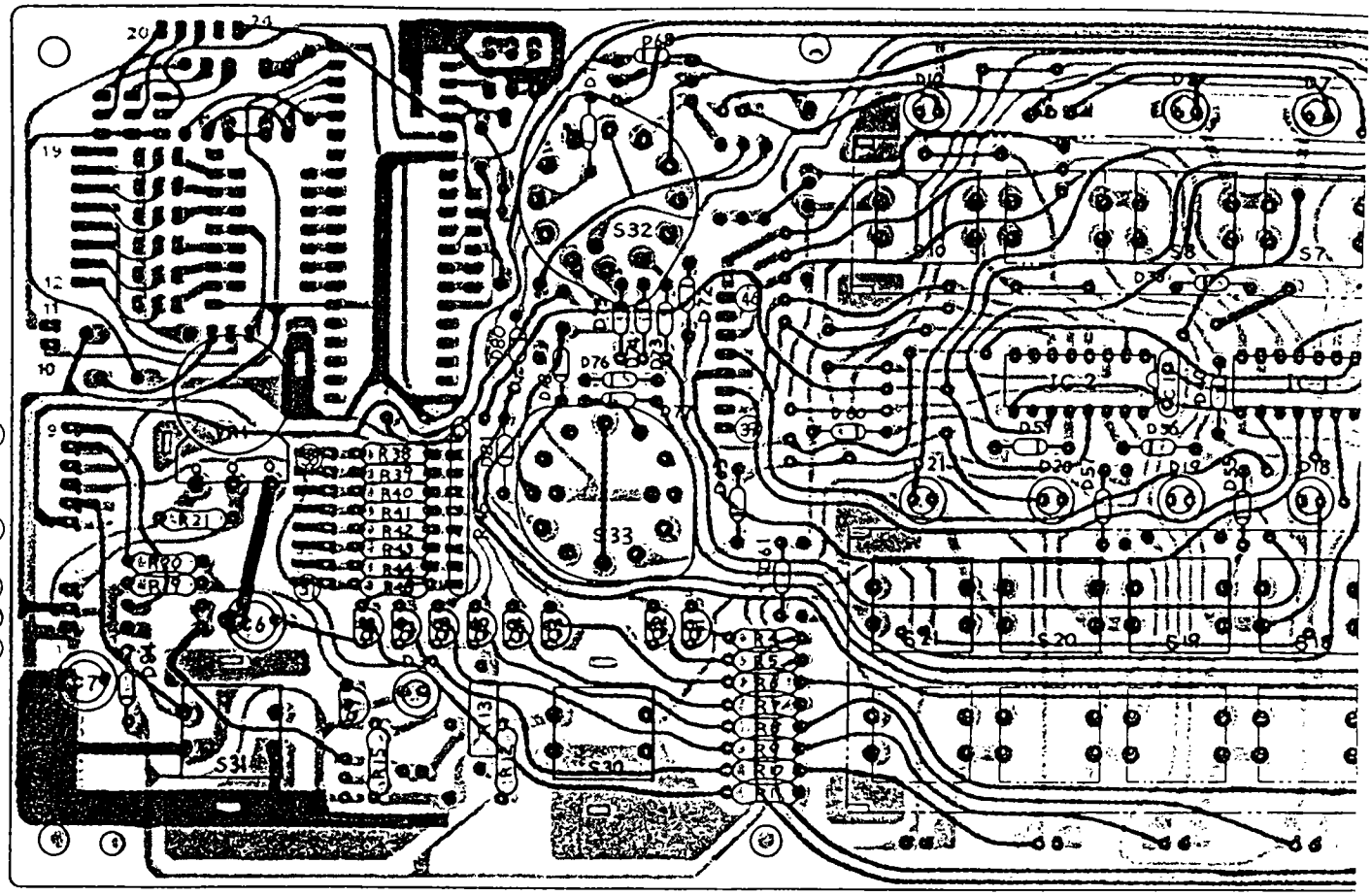
Ensure trigger outputs at IC1 when low V_{OH} LS273 is used.

R47 47k to 10k
R48 47k to D6
R1 10k to 27k
R61 10k to 27k
R60 10k to 27k

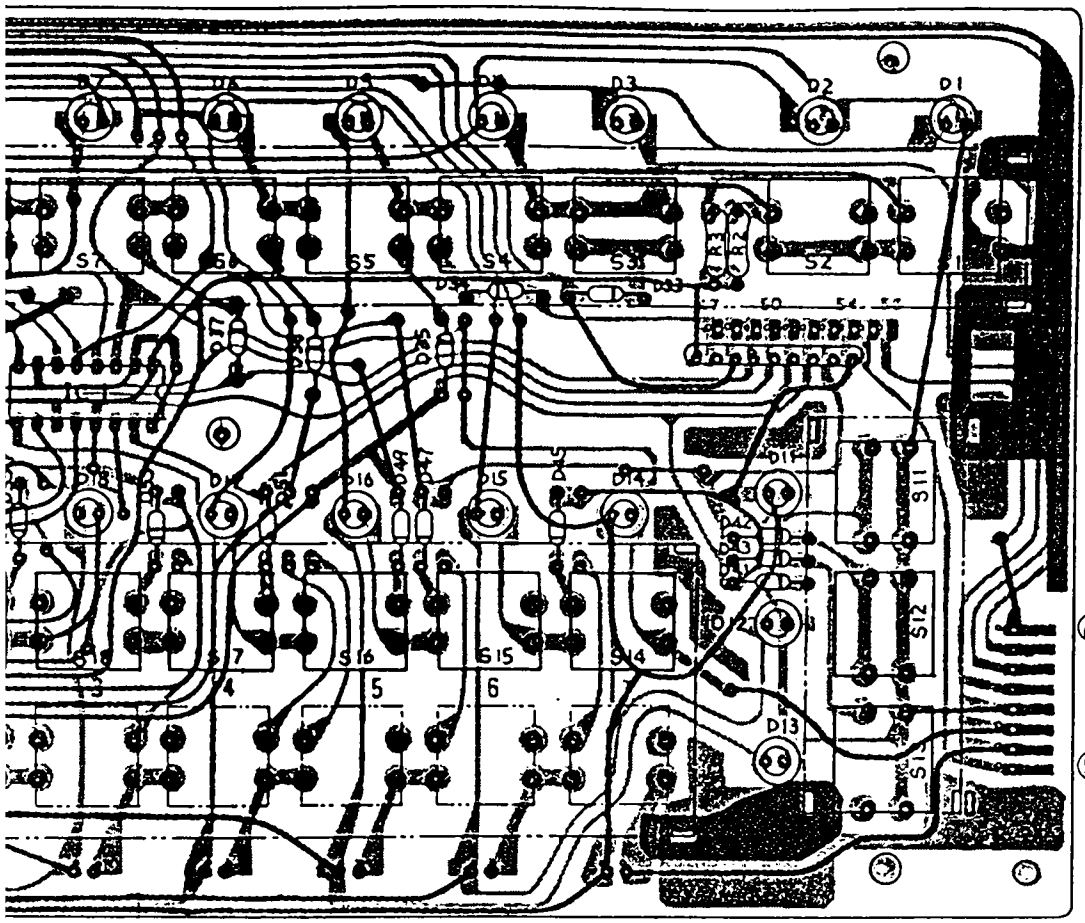
Prevents possible oscillation at final amp upon power off

C29: 470uF to 100uF



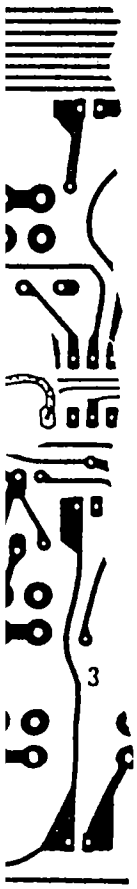

S32
S33
S31
S30
S21
S20
S19
IC-2
D76
D83
R46

19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35



CR-5000
CONTROL BOARD
GL3124-090
(7312409010)
(pcb 2291046501)

with serial number 152650
(Viewed from the rear)



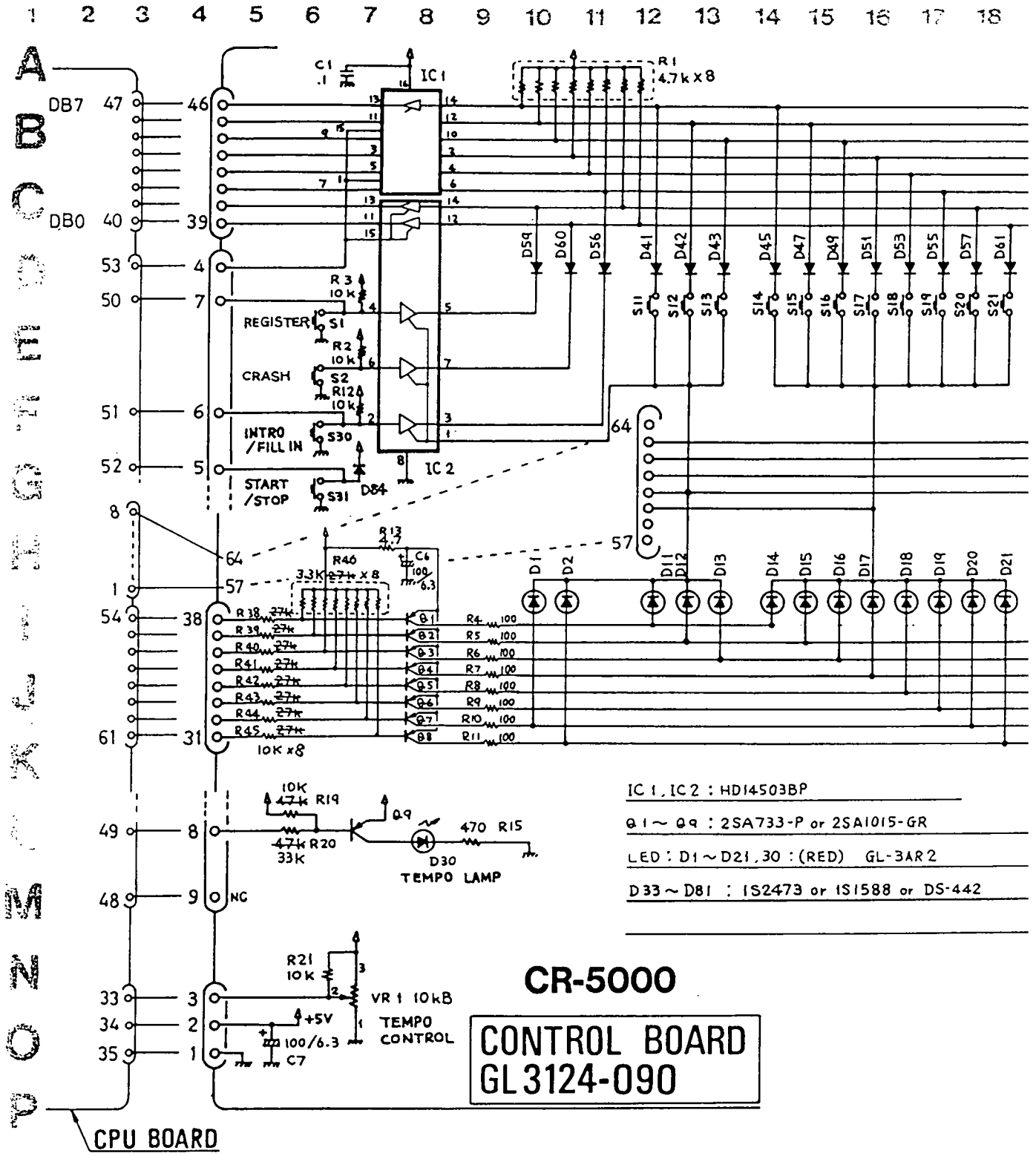
: DS442 or 1S1588, 1S2473

: 2SA733P or 2SA1015-GR

: LED GL-3PR2 (RED)

(pcb 2291046500)

surface mounting
D83 - CR-8000 only



IC 1, IC 2 : HD14503BP

Q 1 ~ Q 9 : 2SA733-P or 2SA1015-GR

LED : D1 ~ D21, 30 : (RED) GL-3AR2

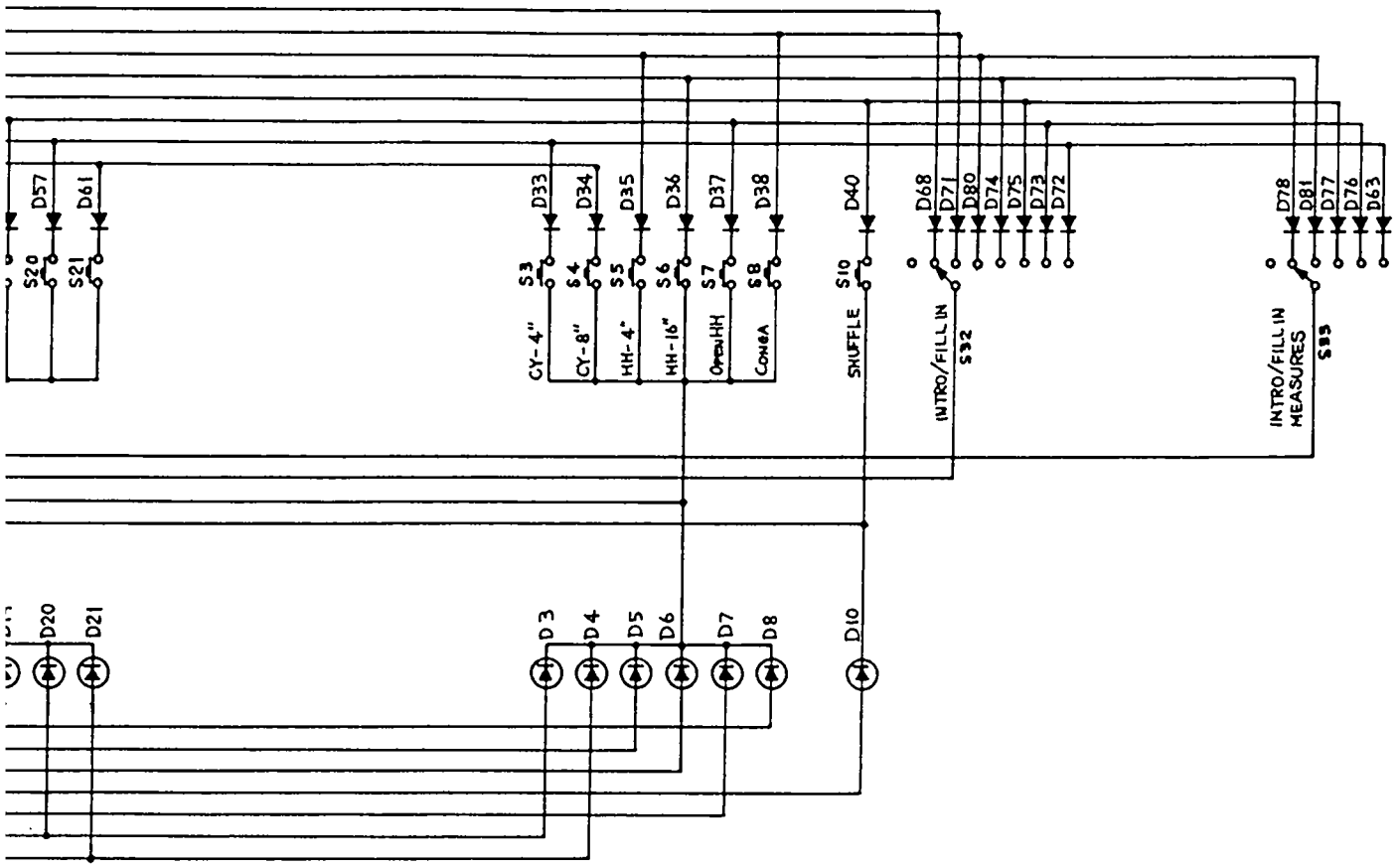
D33 ~ D81 : 1S2473 or 1S1588 or DS-442

CHANGES IN RESISTANCE With Serial Number 091100 and up

The changes eliminates possible dim lighting of LEDs due to insuffic at IC1 or IC2 on CPU board:

R38-R45: 27k to 10k R19: 47k to 10k R20: 47k to 33k
Resistor Array R46: 27k to 3.3k

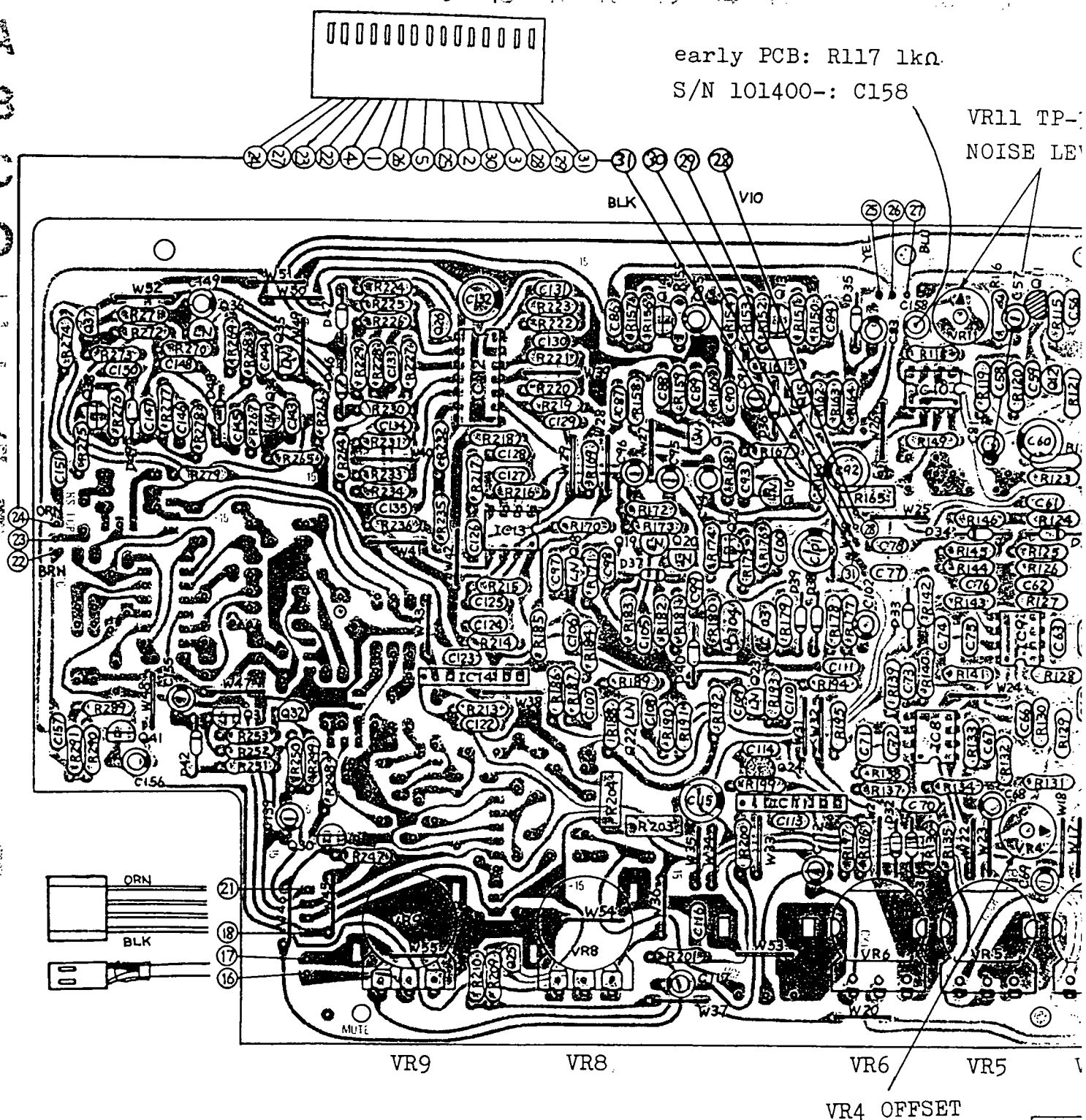
18 19 20 21 22 23 24 25 26 [illegible] 30



—

-442

sufficient H level output



2SC945-P
2SC732TM-GR
2SA733-P
2SC945-P(NZ)
2SK30A-Y
DS442, 1S2473 or 1S1588
1S188FM

VR9
with S/N 091100
From 10k to 50k

CR-5000
VOICING BOARD
VG3124-110 (7312411009)

HA1457

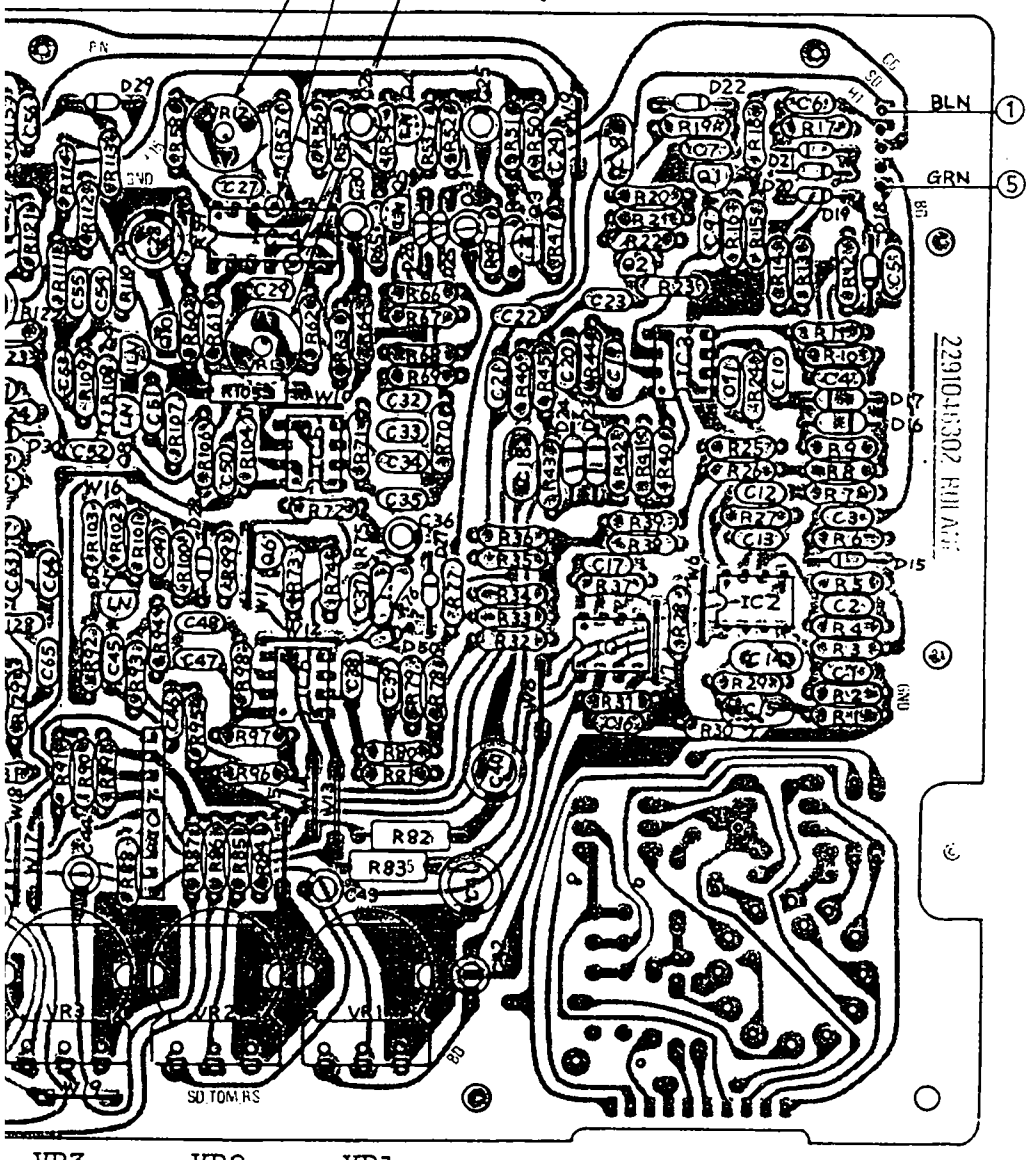
21 22 23 24 25 26 27 28 38 39

VR12 TP-1
CB FREQ

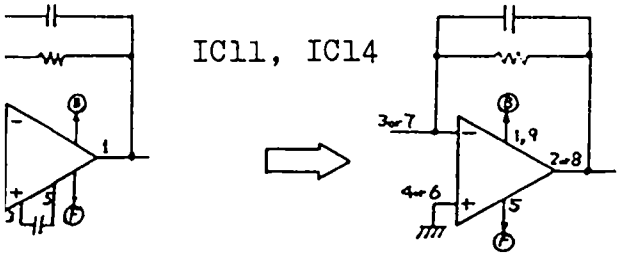
VR13 TP-2
CB FREQ

-3
LEVEL

WITH S/N 111700
R55,56,58,61,63,64
Resistances are increased to limit currents into IC4. This modification is mandatory when replacing defective IC4.



VR3 VR2 VR1



IC11, IC14

57W(8-pin) or NJM4558S (9-pin)
See p. 22 for detail.

CHANGES IN COMPONENT WITH SERIAL NUMBERS:

CR-5000 101400
CR-8000 101300

- **SD**

R94	330	→	2.2k
R97	33k	→	10k
R79	1k	→	15k
R80	33k	→	10k
R76	22k	→	47k
R99	4.7k	→	10k
R33	33k	→	15k
R32	33k	→	47k
R34	33k	→	22k
R100	2.2M	→	1M
C48, 47	.033μF	→	.015μF
C39, C38	.027μF	→	.0047μF
C49	.015μF	→	.018μF
C45	.0047μF	→	.0022μF
C46	.001μF	→	.015μF

- **NOISE**

VR11	5k(B)	→	10k(B)
R117	1k	→	open
C158	0	→	10μF/16

- **TOM TOM**

R46	6.8k	→	22k
R38	82k	→	33k
R39	68k	→	27k
R37	220k	→	82k
C18	.068μF	→	.018μF
C7	.01μF	→	.018μF

- **CONGA**

R133	120k	→	100k

- **CB**

R59	3.3k	→	3.9k
R56	18k	→	22k
R63	18k	→	22k

- **OUTPUT**

C114	100pF	→	47pF

- **ACC**

C156	0.47μF	→	1μF

- **CY, HH, OHH**

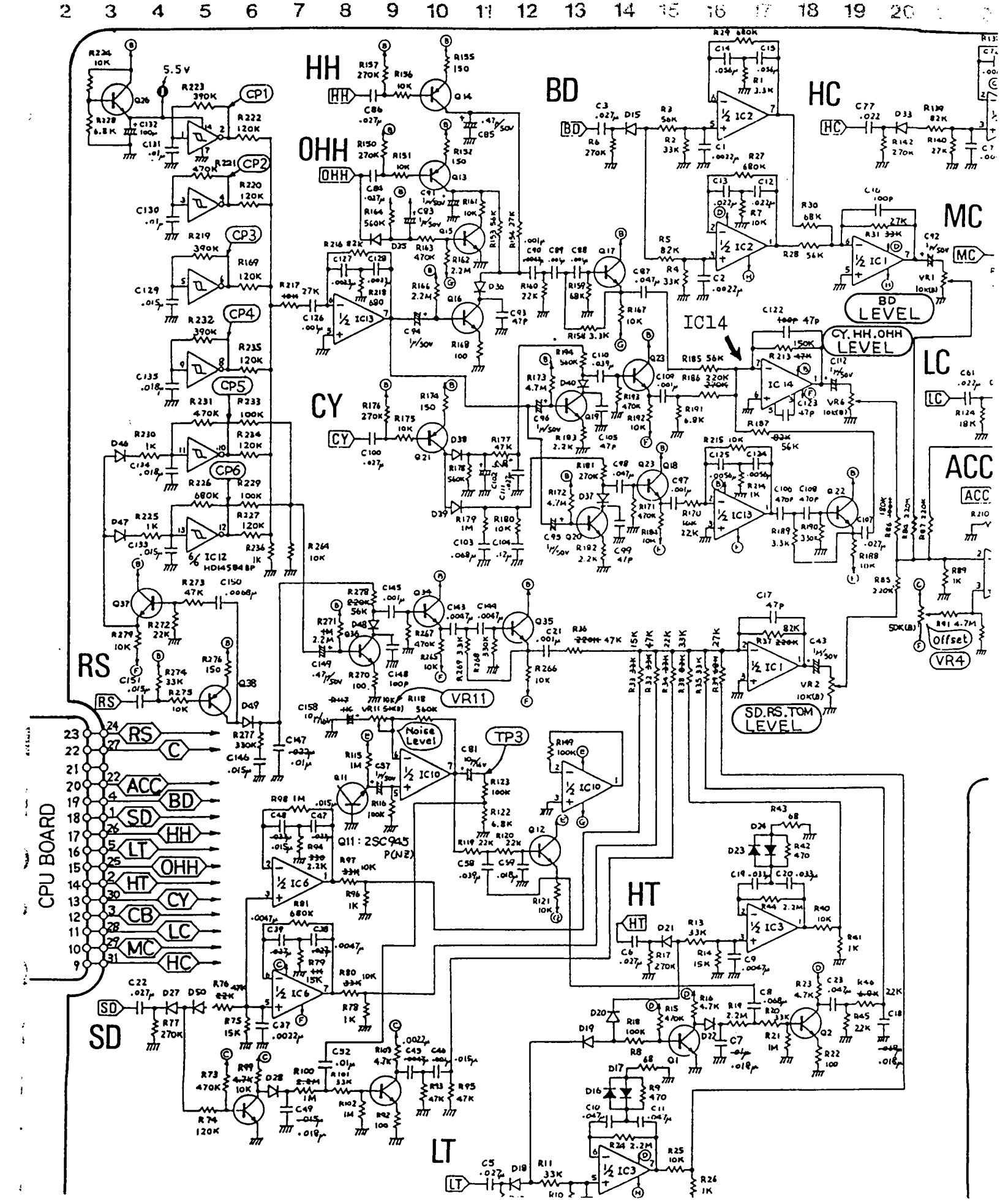
R217	10k	→	27k
R170	10k	→	22k
R187	82k	→	56k
R186	270k	→	220k
R213	47k	→	150k
R86	100k	→	180k
C90	.0047μF	→	.001μF
C122	100pF	→	47pF

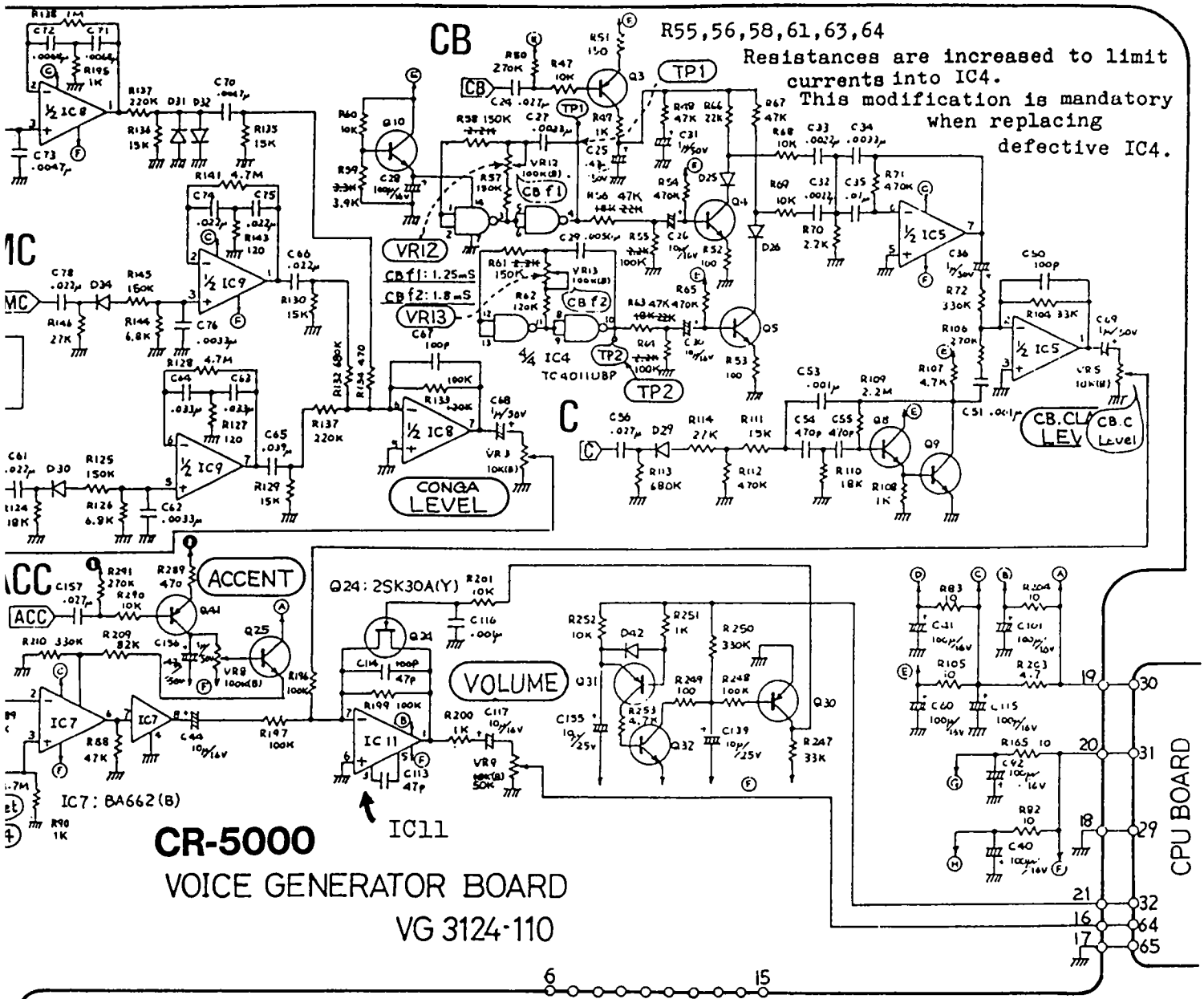
- **RS**

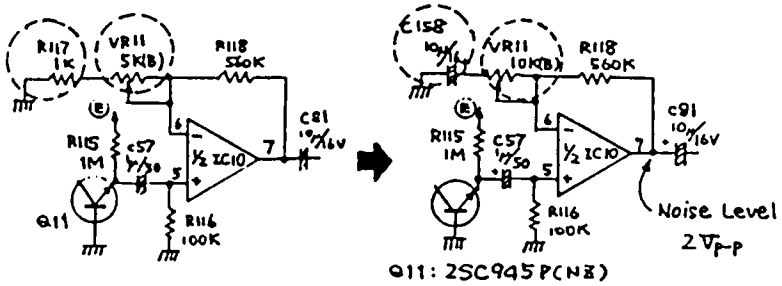
R271	1M	→	2.2M
R278	220k	→	56k
R36	220k	→	47k
C147	.002μF	→	.01μF

- BD

R31 33k


HH
OHH
CY
RS
SD
BD
HT
LT
HC
MC
LC
ACC
IC14
BD LEVEL
CY.HH.OHH LEVEL
SD.RS.TOM LEVEL
Noise Level
Offset
VR4
VR11
TP3
CPU BOARD
Q11 : 2SC945 P(NZ)
HD14584BP





NOISE GENERATOR

LEFT

When ½IC10 bias current is high, it heavily DC biases output waveform, narrowing headroom. (Flatened one peak at relarively small input signal.)

RIGHT

Decoupling capacitor makes DC gain of the IC unity.

IC1,2,3,5,6,8,9,10,13 : NJM4558DP
IC11,14 : HA1457W or NJM4558S
Q1,6,10,12,15,25,26,32,37 : 2SC945P
Q24,5,7,8,9,16~20,22,23,34~36 : 2SC732TM GR
Q3,13,14,21,30,31,38,41 : 2SA733P

PARTS LIST

* CR-8000 ** CR-5000

2201061100	Case N-611	
*2281028102	Chassis(bottom plate) N-281	
*22020159	Battery cover	
*12199525	Battery holder	
*2219024802	Holder	
*2226031000	Cushion	
**2281027302	Chassis(bottom plate) N-273	
2235010100	Rubber foot	
2281027201	Chassis N-272 power trans.	
*2221027100	Panel(upper) N-271	
**2221025900	Panel(upper) N-259	
*2221027200	Panel(lower) N-272	
**2221026000	Panel(lower) N-260	
*2222030200	Escutcheon(LED window)N-302	

KNOB. BUTTON

2247012800	Knob N-128 rotary small	
2247016500	Knob N-165 rotary large	
2247050900	Button N-509 wht p.sw.	
2247051600	Button N-516	
2247051700	Button N-517	
2247051800	Button N-518	
2247051900	Button N-519	
2247052000	Button N-520	
2247052100	Button N-521	
2247052200	Button N-522	
2247052300	Button N-523	

POWER TRANSFORMER

22450240N1	PT-N-240N	100V
22450241C1	PT-N-241C	117V
22450242D0	PT-N-242D	220/240V

POTENTIOMETER

13219229	EVHRRA361B14 TEMPO, VOLUME on early units	
13219312	EVHLWAD25B14 Voice level	
13219238	EVHRRA361B15 ACCENT	
13219245	EVHRRA361B54 VOLUME not on eary products	
13299106	EVTR4AA00B53 5kB trim	
13299101	EVTR4AA00B14 10kB trim	
13299107	EVTR4AA00B54 50kB trim	
13299102	EVTR4AA00B15 100kB trim	

SWITCH

13129117	SDK1P power	100V
13129118	SDK1P w/CSA UL	117V
13129110	ESB-70294	220/240V
13159316	HSW-0372-01-030 slide TRIG OUT select. SYNC IN/OUT	
13129714	KEH10903 RHYTHM SELECT	
13119508	SRM1026K15 FILL IN MEASURE	
*13119806	SRM101CY15 FILIN SELT.INSTMNT	
*13159304	SSB02335 PROGRAM MODE	
**13119704	SRM1018K15 FILL IN SELECT	

PCB

*7312506009	CPU (pcb 2291046401)
**7312406008	CPU (pcb 2291046401)
*7312509008	CONTROL (pcb 2291046500)
**7312409010	CONTROL (pcb 2291046500)
*7312512007	VOICING (pcb 2291046302)
**7312411009	VOICING (pcb 2291046302)
*7312511001	LED (pcb 2291046600)
2291046200	FUSE

JACK. SOCKET

13449106	SG7622#8
*13429607	DIN socket TCS0707-01-010

FUSE

12559104	SGA 0.500	100/117V
12559505	CEE T125mA(s)	220/240V
12559510	T400mA CEE(s) ±15V	220/240V
12559513	CEE T1A(s) +5V	220/240V
12199519	Fuse clip TF-758	

RESISTOR ARRAY

13910107	RM8-332K	3.3K x 8
13910101	RM8-472K	4.7K x 8
13910102	RM8-273K	27K x 8

SEMICONDUCTORS

IC

1517911700	µPD8049C-159	CPU
or		(See Page 5 for difference.)
1517913000	µPD8049C-323	
*15179118	µPD8048C-305	CPU display
15159105H0	HD14013BP	
15159126H0	HD14023BP	
15159128H0	HD14050BP	
15159303H0	HD14584BP	
15169304H0	HD74LS04P	
15169325C0	DM74LS273N	octal D FF
15169115H0	HD7445	BCD-TO-DECIMAL DEC
*15179305	µPD444C	RAM
15199110T0	TA7179P	±15V regulator1519
15199106F0	µA7805UC	+5V regulator
15159306HC	HD14503BP	
15159103T0	TC4011UBP	
15189103	NJM4558DP	
*15189113	AN6912	
15189502	HA1457W	(pin incompatible,
or		see p. 22)
15189135	NJM4558S	
15229803	BA662B	VCA

TRANSISTOR

15119105	2SA733P
15129108	2SC945-P
15129108A	2SC945-P(NZ) noise
15129104	2SC732TM-GR
*15119121	2SA937-Q
*15129121	2SC2021-R
15139101	2SK30ATM-Y
15119806	2SB596-0 or Y
15129816	2SD880-0 or Y

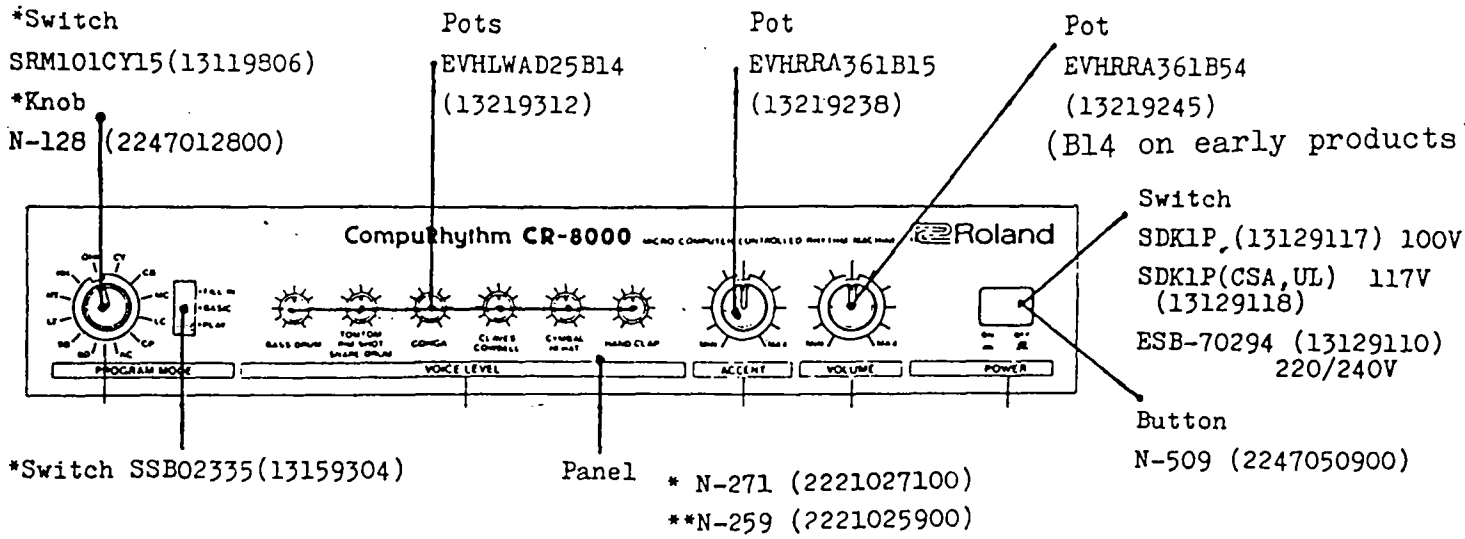
LED

15029109	GL-3AR2 red
*15029112	GL-3PG2 green BEAT
*15029125	TLR312 DISPLAY

Diode

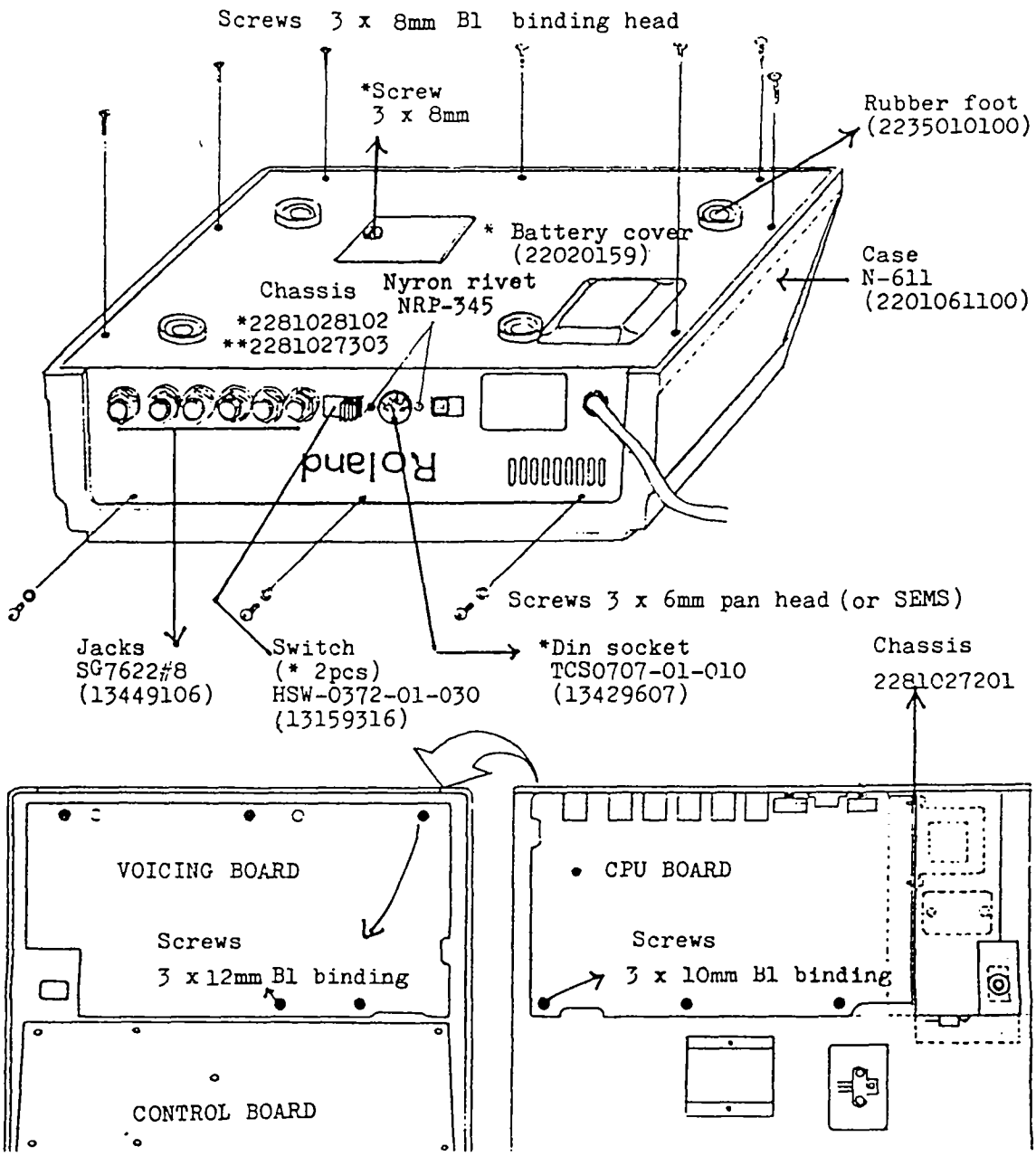
15019107	DS442 or 1S1588 or 1S2473
15019122	1S188FM
15019236	W02 bridge rectifier

12389708	FCR-6 (6.0MHz) ceramic resonator



DISASSEMBLY

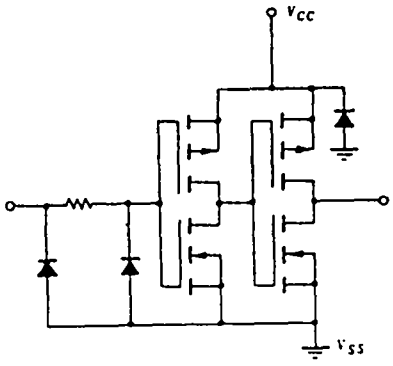
Remove ten (10) screws indicated below.

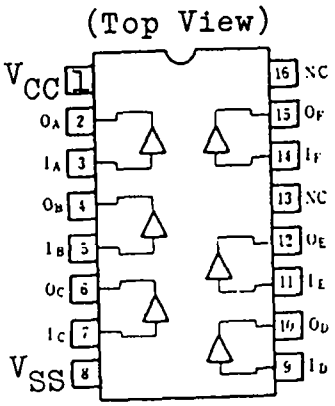


(13129714)

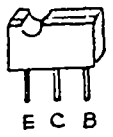
HD14050B

Hex Buffers





2SA937
2SC2021



MC14503B

HEX NON-INVERTING 3-STATE BU

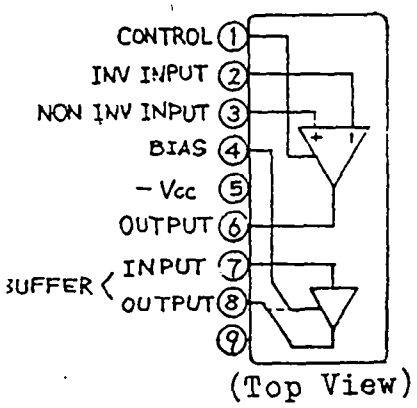
TRUTH TABLE		
In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

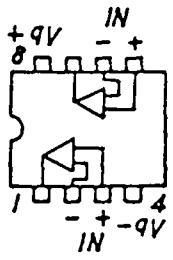
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BA662

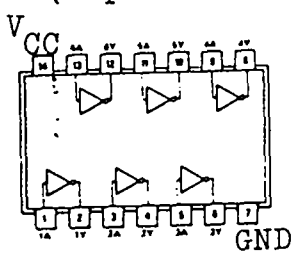


μPC4558C

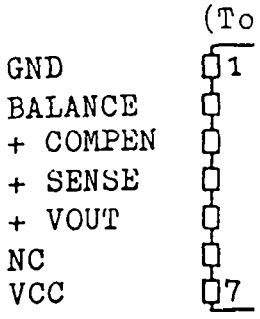


TA717

74LS04
HEX INVERTER



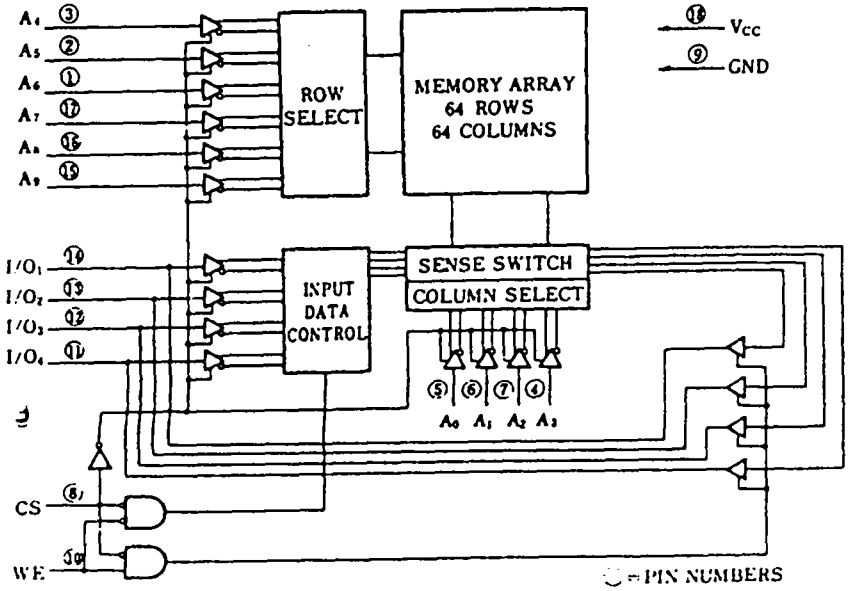
DUAL ±15V TRAC



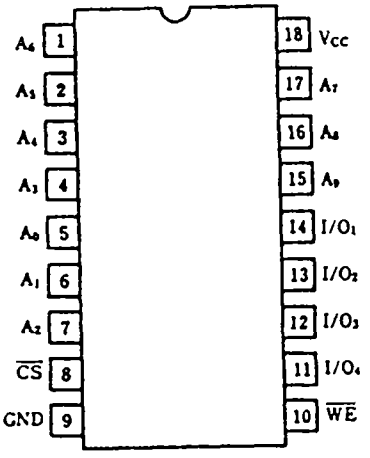
HM4334P-4

μPD444C

4096 BIT STATIC CMOS RAM



(Top View)

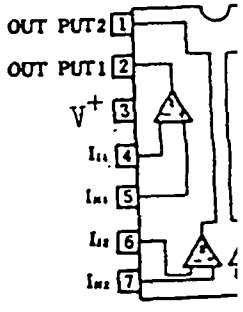


Reg.IN = 5
Reg.OUT= 5
Ripple rej
Output cur

μPC177C

Quad C

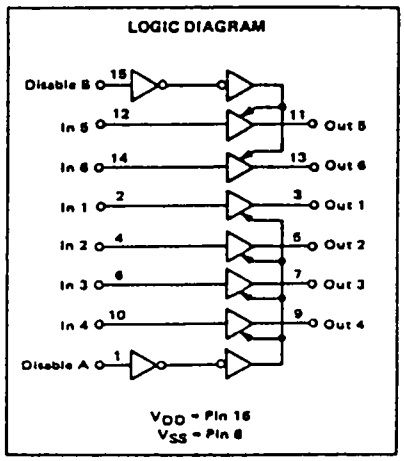
Connectio



503B

3-STATE BUFFER

	Unit
	Vdc
0.5	Vdc
	mAdc
	mAdc
	°C
	°C

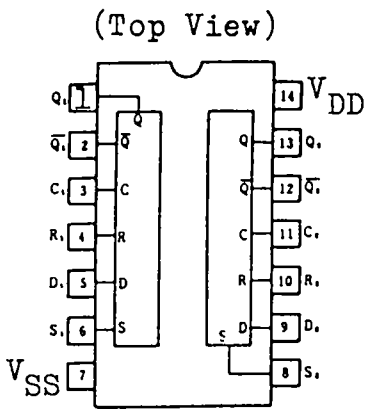


HD14013B

Dual Type D Flip Flop

INPUT				OUTPUT	
Clock*	Data	Reset	Set	Q	$\overline{Q}$
↗	0	0	0	0	1
↗	1	0	0	1	0
↘	×	0	0	Q	$\overline{Q}$
×	×	1	0	0	1
×	×	0	1	1	0
×	×	1	1	1	1

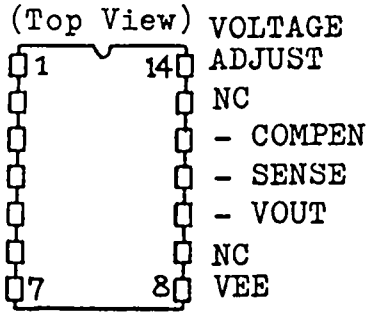
(Top View)



TA7179P

15V TRACKING RAGULATOR

(Top View)



VOLTAGE ADJUST
NC
- COMPEN
- SENSE
- VOUT
NC
VEE

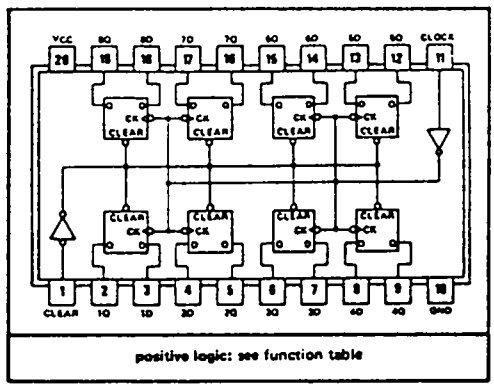
E
EN
E

g.IN = 5mV(typ)(VIN=18-30V)
g.OUT= 5mV(typ)(IOUT=0-50mA)
pple rejection ratio = 75dB
tput current = 100mA (max)

N74LS273

OCTAL D-TYPE FLIP-FLOP WITH CLEAR

(Top View)



FUNCTION TABLE
(EACH FLIP-FLOP)

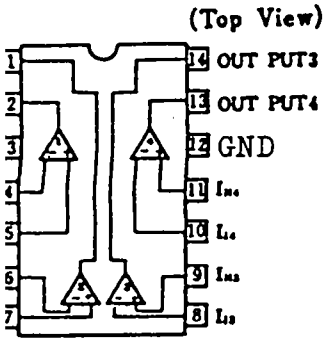
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

PC177C, AN6912

Quad Comparator

Connection Diagram

(Top View)

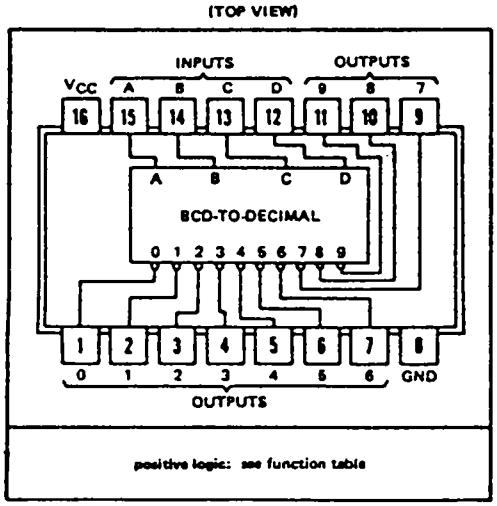


OUT PUT3
OUT PUT4
GND

N7445

BCD-TO-DECIMAL DECODERS/DRIVERS

(TOP VIEW)



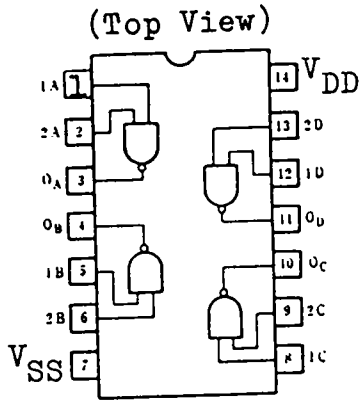
FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

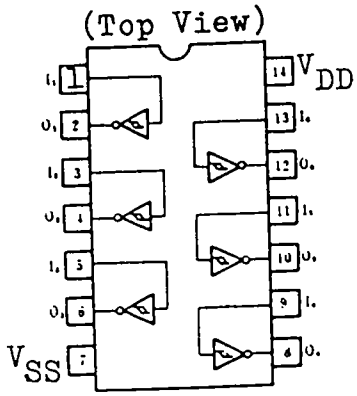
HD14011B

Quadruple 2-input NAND Gate



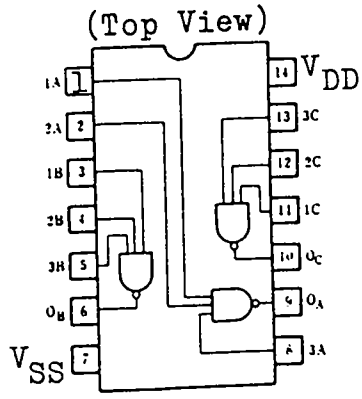
HD14584B

Hex Schmitt Trigger

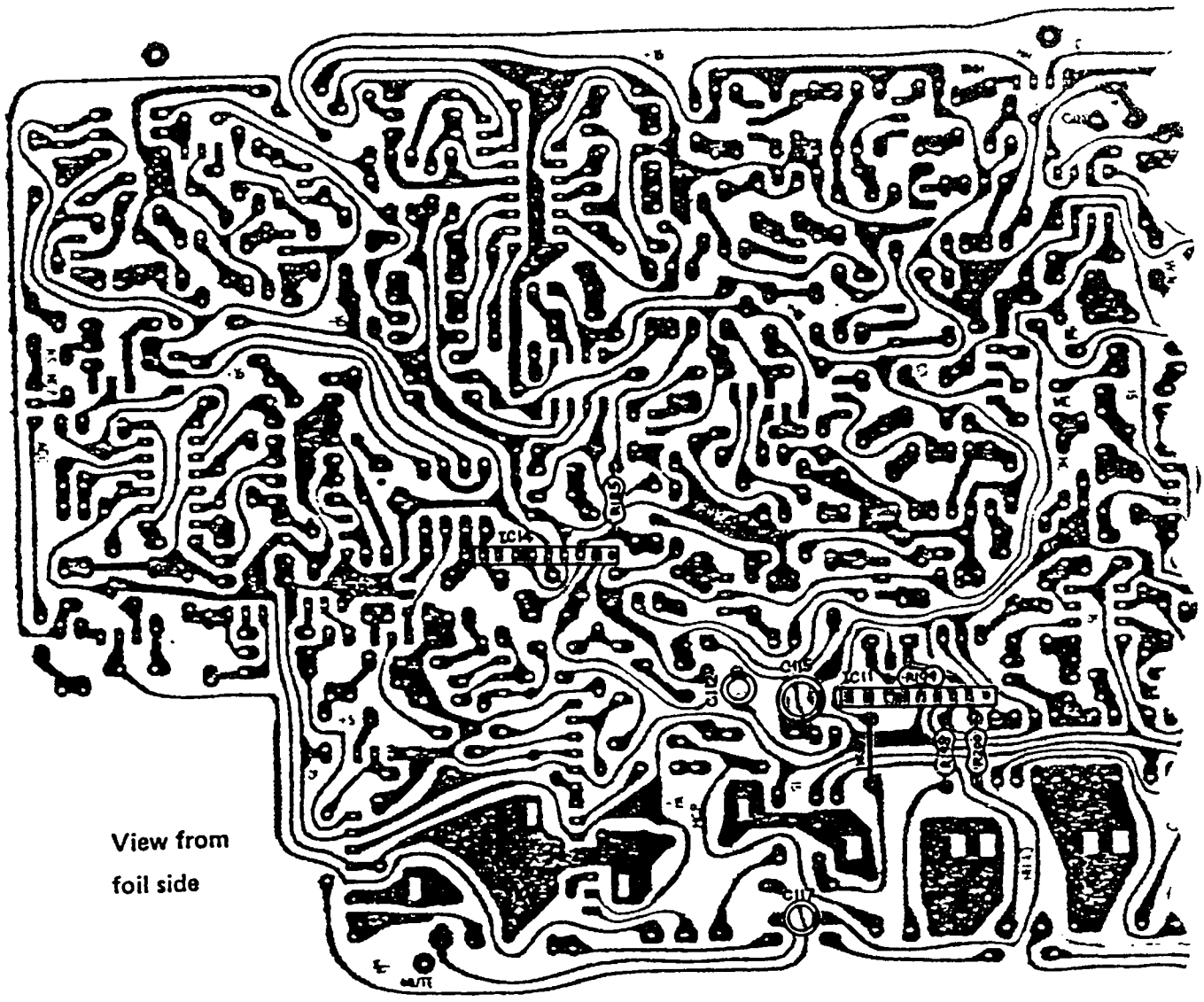


HD14023B

Triple 3-input NAND Gate



VOICING BOARD CHANGES



View from foil side

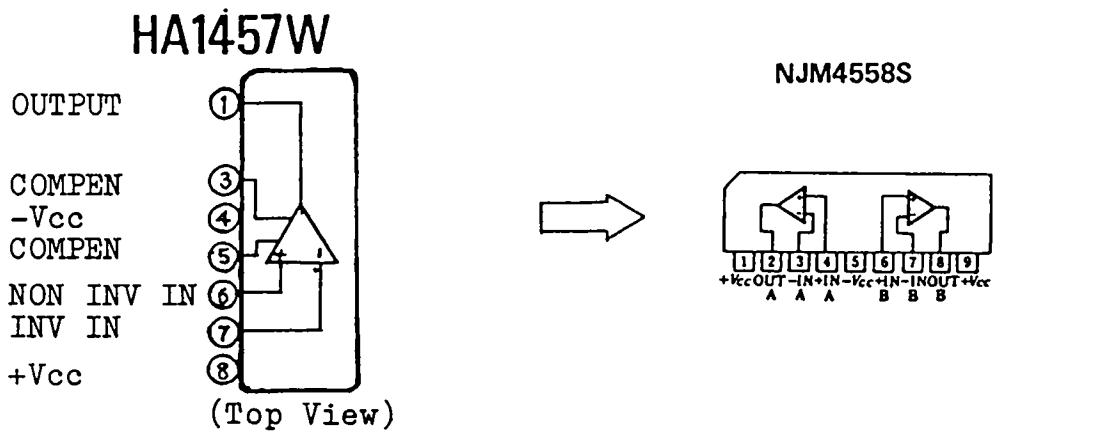
CHANGING OPERATIONAL AMPLIFIERS

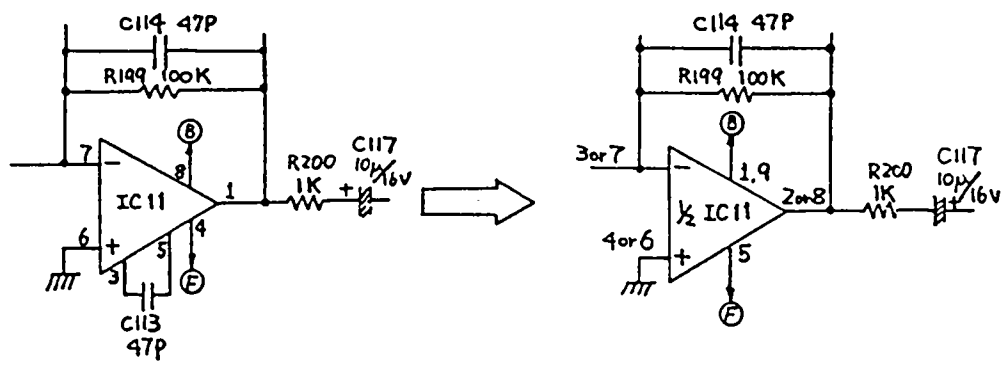
On CR-5000/8000 VG Boards as well as in other Roland products, the IC NJM4558S replaces HA1457W which is discontinued at the semiconductor manufacturer.

Incompatible pin arrangement leads to minor PCB re-layout as shown below, which is due to put into practical production.

Serial Numbers with which the change is effective on the CR-5000/8000 are not fixed as of the date this edition is closed.

NOTE: Although two OP AMPs are contained in new IC, one is left redundant in this application.





HA1457W NJM4558S