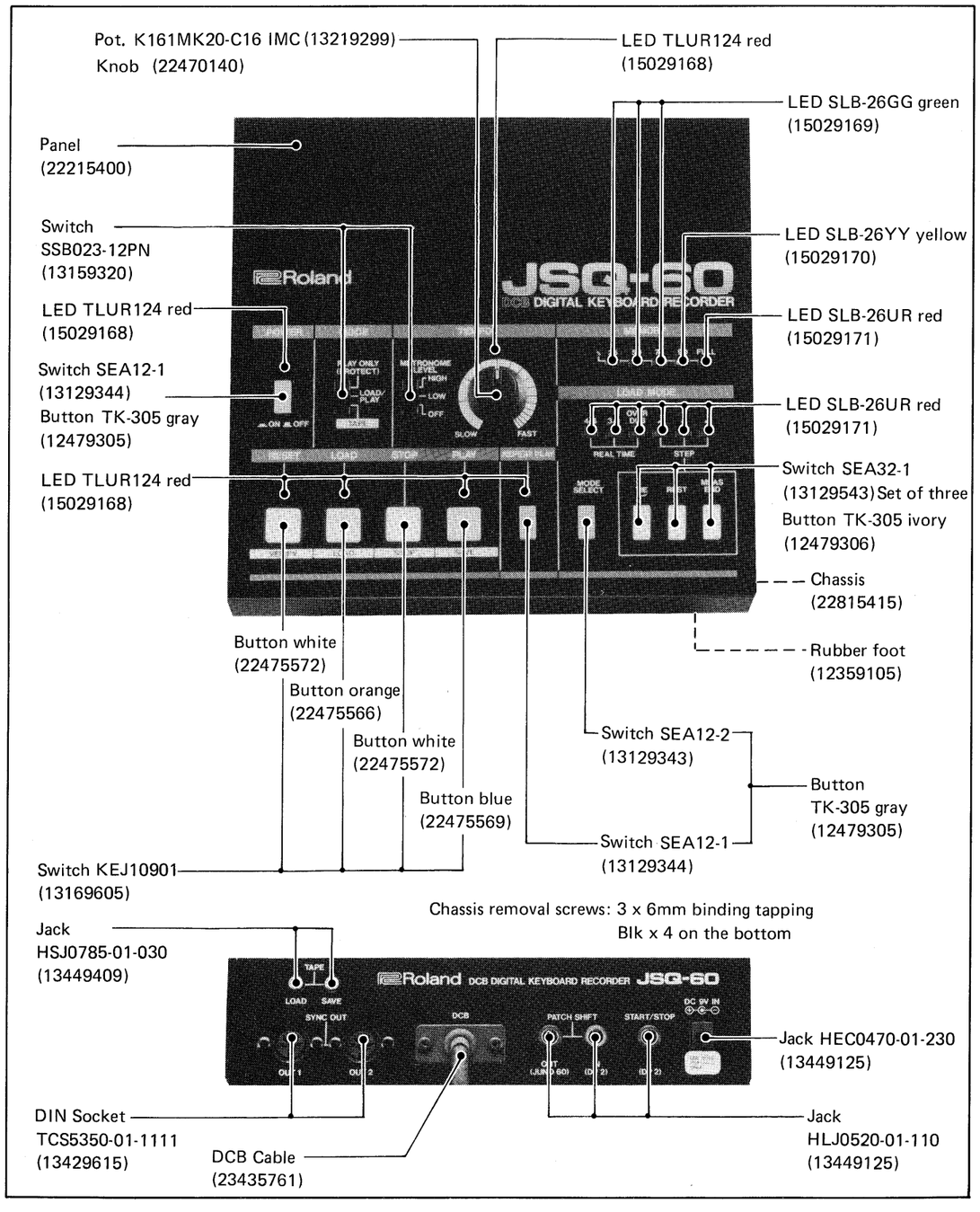
JSQ-60 SERVICE NOTES *First Edition*

SPECIFICATIONS

Memory Capacity : Approx. 2000 steps (a note/step)
Tape Interface : 2700 baud
Current Draw : 70mA @9VDC
Power Consumption : 3W
Dimensions : 226(W) x 223(D) x 57(H) mm
8 7/8(W) x 8 3/4(D) x 2 1/4(H) in
Weight : 1.5 kg / 3 lb. 5 oz.



PARTS LIST

CASE

22215400	Panel	
22815415	Chassis	
12359105	Rubber foot	

KNOB, BUTTON

22470140		knob
22475566	(orange)	button
22475572	(white)	button
22475569	(blue)	button
12479306	TK-305 (ivory)	button
12479305	TK-305 (gray)	button

PCB

79318120	SEQUENCER BOARD (pcb 22915869)	

IC

15179338	TMP80C50AP-6-9511	CPU
15179335	HM6264LP-15	Static RAM
15179337	MSM82C51A	SIO
15159503	TC40H000P	Quad 2-input NAND gate
15159505	TC40H004P	Hex inverter
15159514	TC40H032P	Quad 2-input OR gate
15159506	TC40H138P	3-to-8-Line decoder/demultiplexer
15159511	TC40H174P	Hex D-type flip flop
15159508	TC40H373P	Octal D-type latch
15159509	TC40H393P	Dual 4-bit binary counter
15159116TO	TC4069UBP	Hex inverter
15169341	74LS14	Hex schmitt trigger inverter
15189119	TL062CP	Dual low power bi FET OP amp
15149114	M54527P	Hex sink-type darlington transistor array

TRANSISTOR

15119113	2SA1015-GR (or 15119112 2SA1015-Y)	
15129114	2SC1815-GR (or 15119115 2SC1815-Y)	
15129815	2SD880-0 (or 15129816 2SD880-Y)	

DIODE

15019120	1S2473	
15019208	1SR35-200	
150196120X	05Z5.6X	zener
15029168	TLUR124 (red)	LED
15029171	SLB-26UR (red)	LED
15029169	SLB-26GG (green)	LED
15029170	SLB-26YY (yellow)	LED

POTENTIOMETER

13219299	K161MK20-C16 1MC	
13299137	RVF8P01-104 100KB	trimmer

SWITCH

13169605	KEJ10901	light touch
13129343	SEA12-2	push (momentary action)
13129344	SEA12-1	push (lock)
13129543	SEA32-1	Set of three SEA12-2 in one frame
13159320	SSB023-12PN	slide

JACK

13449125	HLJ0520-01-110	6.5mm dia.
13449409	HSJ0785-01-030	3.5mm dia.
13429615	TCS5350-01-1111	5-pin DIN
13449706	HEC0470-01-230	DC 9V IN

CERAMIC RESONATOR

12389725	CSA4.00MT	4MHz
12389726	KMFC1081T	9MHz (with CSC300)

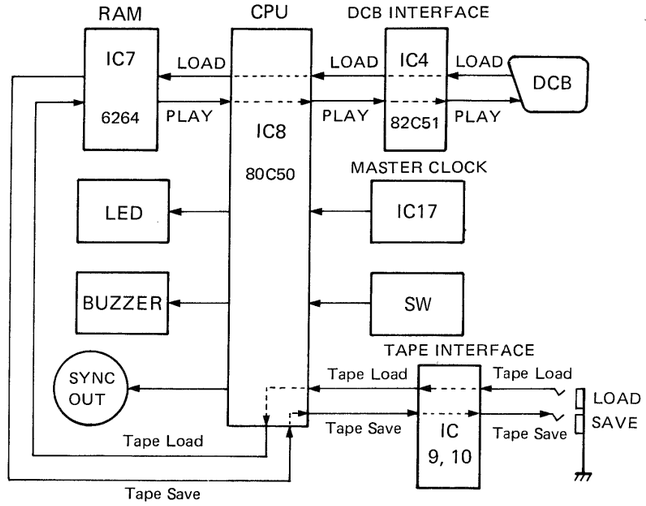
OTHERS

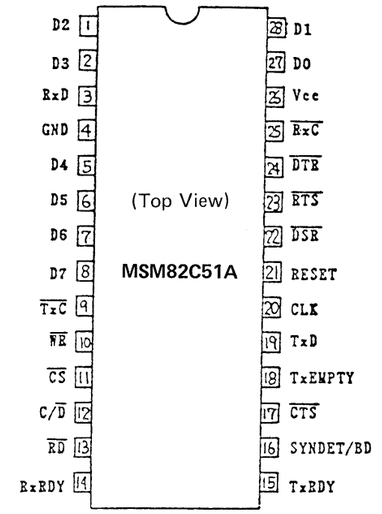
12389723	PKM37-3A0	piezoelectric buzzer
13589501	FZ0H473Z	0.047F/5.5V high-capacitance, low-leakage, high-impedance, non-polarized, miniature capacitor for RAM back up
13919320	RM6 333J	resistor array 33K x 6
12449243	ELE-A120KA	coil
22195439	LED Holder	
2224010200	Mask	slide switch
23435761	DCB Cable	W/DCB Plug

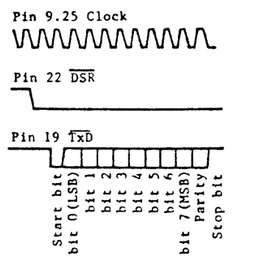
AC ADAPTOR (Commercially available. Only for reference.)

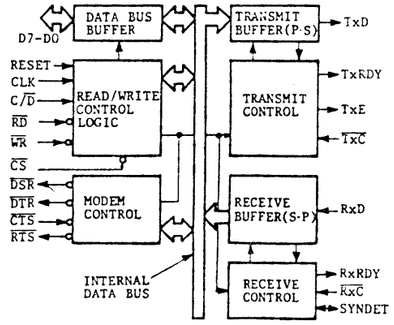
1244950900	PSA-100	100V
1244951000	PSA-120	117V
1244951100	PSA-220	220V
1244951200	PSA-240	240V

CIRCUIT DESCRIPTIONS









D7-D0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Recover Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{cc}	+5 Volt Supply
GND	Ground

JSQ-60 receives or transmits data (Key ON/OFF, Patch Change) from or to the external equipment such as JP-8 or JUNO-60 through the DCB.
Since the data flowing through DCB is a serial bit stream of 31.25 Kbaud, a USART (Universal Synchronous/Asynchronous Receiver/Transmitter) M82C51 is employed. The M82C51 converts the external serial input into parallel format to allow the CPU to process the data. At the same time it converts parallel data from the CPU to serial bit stream for use by the external DCB unit.
Data format and connection of DCB are detailed on OP-8, JUNO-60 and JP-8 Service Notes.

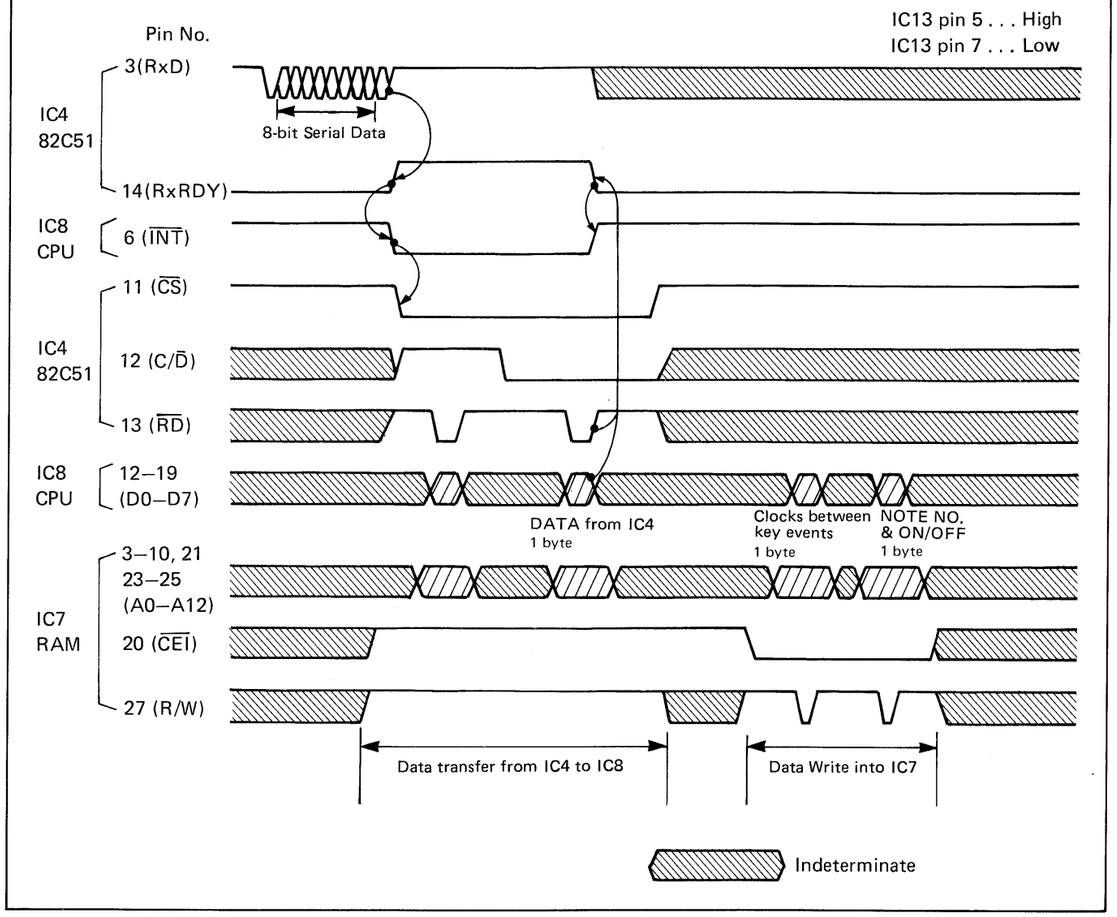
SWITCH SCANNING

The CPU places successive scanning pulses on pins 12 (Y-3) thru 14 (Y-0) of IC15 and reads output from switches through pins 31-34 respectively.

LOAD/PLAY

In LOAD or PLAY mode, key data and patch data (if any on the DCB) are transmitted in parallel format between the CPU IC8 and DCB Interface IC4. The CPU reads the status of IC4 through INT terminal.

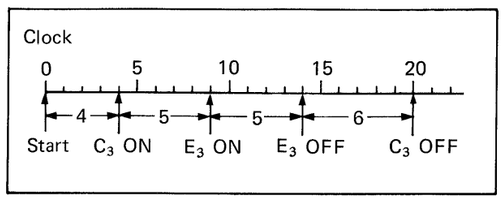
LOAD TIMING



LOAD

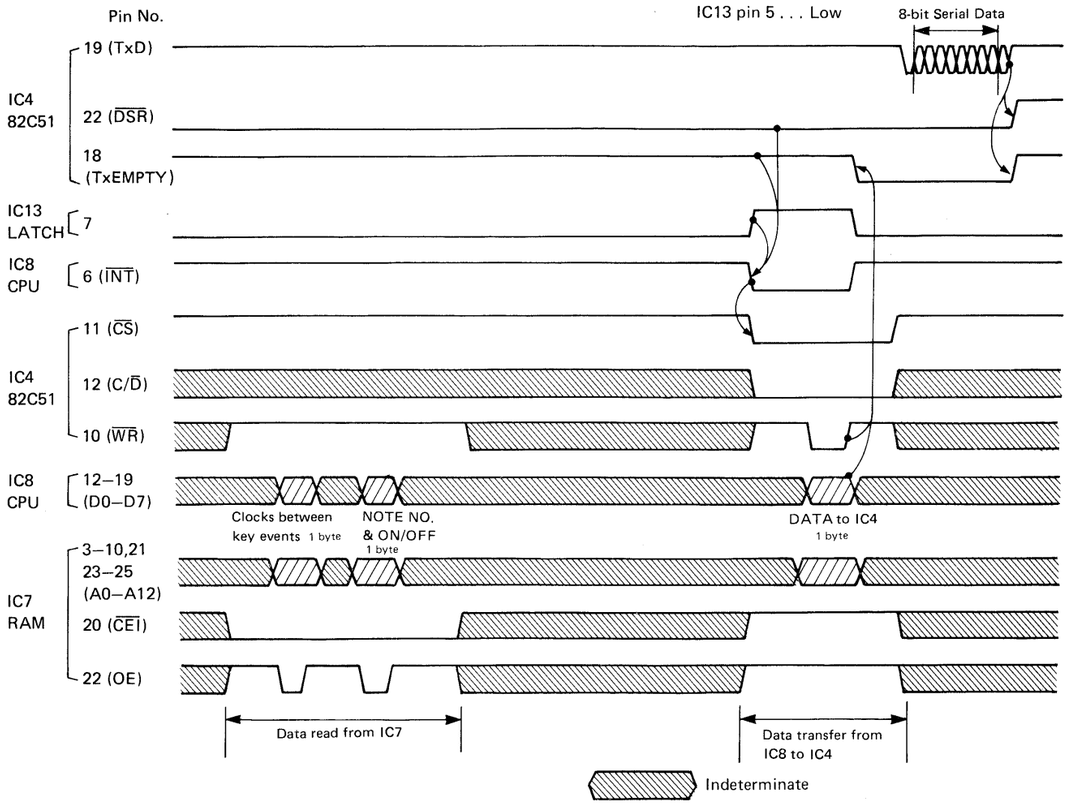
The CPU puts IC13 pin 5 (IC3 pin 10) high to allow INT control logic IC3 to pass the level on RxRDY of IC4 which turns RxRDY high when it has stored 1 byte of external data (via RxD) into RECEIVE buffer. The high RxRDY causes INT to go low and signals the external DCB unit of its BUSSY status.
Recognizing low INT, the CPU proceeds with some steps to read the data on the CPU data bus. Then the IC4 sets RxRDY low to prepare itself for the next data.
The CPU stores the data into RAM IC7 in the following way.

REAL TIME One byte for elapse time between the preceding key event, represented by clocks (divided-by-10 of T1 input, TEMPO).
One byte for the key number (note) with information on PRESSED or RELEASED.



STEP LOAD The length of a note is predetermined by the program according to set position of LOAD MODE on the front panel.

PLAY TIMING



PLAY

The CPU reads two bytes of RAM stored data (one for the number of clocks from the preceding key data; one for the key number and ON or OFF). An elapse corresponding to the clocks prompts the CPU to interrogate the IC4. The CPU pulls IC13 pin 7 (IC3 pin 5) high (while keeping IC13 pin 5 low). When IC4 has no data to be transmitted (high TxEMPTY) to DCB and when the external receiver is not BUSSY (low DSR), low INT is resulted, which enables the CPU to place the key data (note and ON or OFF) on D0-D7. IC4 stores the data into TRANSMIT BUFFER, removes off high on TxEMPTY, then sends it to DCB and turns TxEMPTY to high again, preparing for receiving the next data from the CPU.

OVER DUB

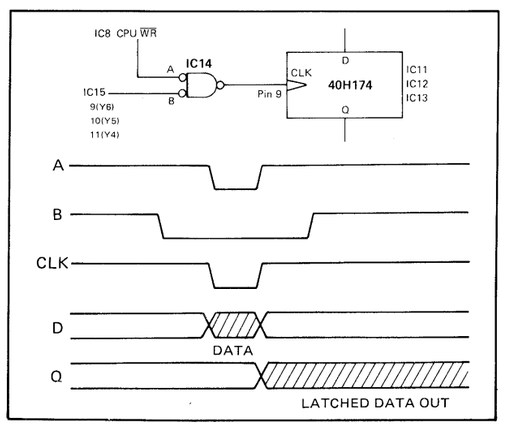
The Real Time Load and Play routines are executed alternately.

MASTER CLOCK (TEMPO)

The outputs of the master oscillator IC17 (approx. 0.7 – 4.4kHz, 5Vpp) are divided by 10 in the CPU and are used to determine the tempo of notes in both Real Time Load and Play modes. The clocks are also used as the timebase of the metronome.

LATCH

ICs 11, 12 and 13 latch LED driving signals. In addition, IC13 controls other signals.



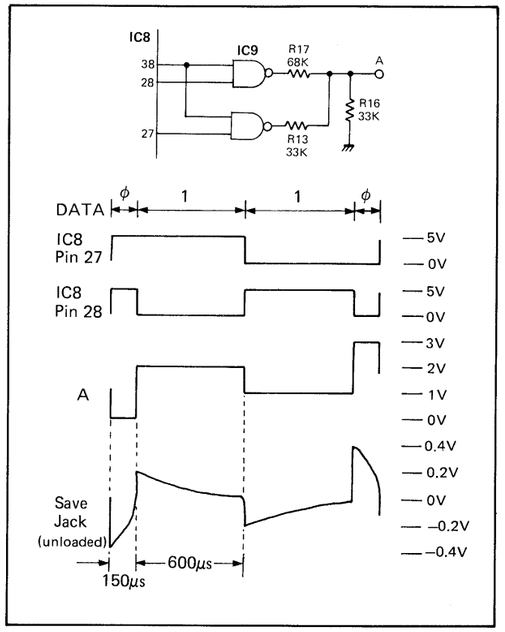
LATCH	pin7	pin5	pin2	pin15	pin12	pin10
IC11	REAL TIME 4/4	REAL TIME 3/4	OVER DUB	STEP 8	STEP 12	STEP 16
IC12	MEMORY INDICATE					RESET / VERIFY
	25%	50%	75%	90%	full	
IC13	TX INTERRUPT MASK H=PLAY L=LOAD	RX INTERRUPT MASK H=LOAD L=STOP, PLAY	SYNC str/stp H (@ STOP)=STOP L (@ PLAY, LOAD)=START	PLAY / SAVE	PATCH SHIFT	LOAD / LOAD

TAPE INTERFACE

When in TAPE mode, the tape interface consisting of IC9, TR1, TR2 and IC10 processes data from/to cassette tape recorder at a 2700 baud rate, while the DCB interface IC4 is made inactive. Also, EXT SYNC clock is blocked in the TR19 which is reverse biased by a high from pin 38 of the CPU.

SAVE

The CPU first converts RAM stored data to serial bit stream and puts out them from port 1, in combination of pin 27 and pin 28 while keeping pin 38 high, to provide two kind of pulses for each 1 and 0 so that they can be made more distinguishable from adjacent bits (when D/Aed with weight) as shown in Fig.
As a leader a pulse train of 1's are produced.

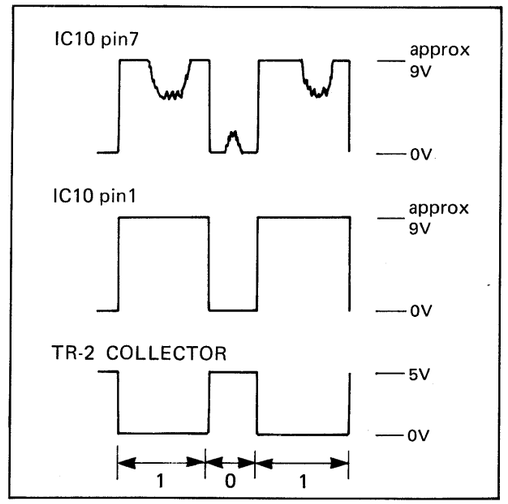


LOAD/VERIFY

Tape data from LOAD jack is first smoothed, amplified to a sufficient level at the first IC10, shaped up by the second IC10 comparator and stepped down to 5Vpp by TR2 before fed to the CPU via T0. The CPU can meaure the length of each incoming half-period. Depending upon the length, it stores into memory either a "0" or a "1" (in LOAD mode), or compares each bit with that stored in RAM (in VERIFY mode).

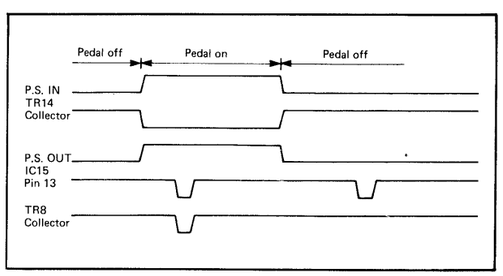
The CPU interprets the signals as follow:
More than 256 train of "1" -- leader
Half period is under 256 μsec. -- "0"
Half period is 256 μsec. – 1msec -- "1"
Over 1 msec. -- invalid or error

If the program runs away when JSQ-60 is operated in conjunction with JUNO-60, this can be curred by connecting a 0.1 μF ceramic capacitor between pin 21 (RESET) of IC24 on JUNO-60 Panel Board B and the ground point.



PATCH SHIFT

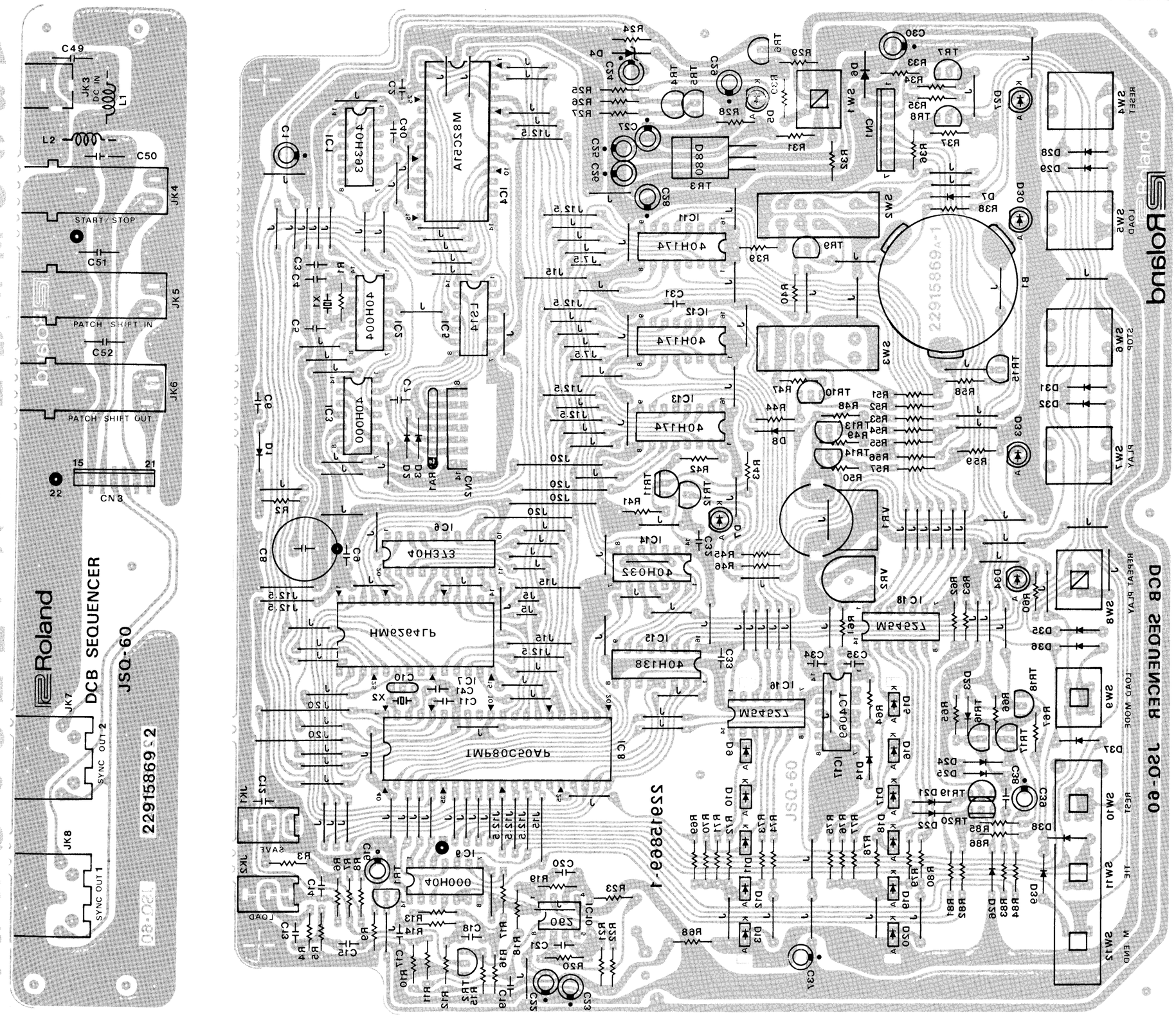
A signal coming from PATCH SHIFT IN jack is routed to PATCH SHIFT OUT jack through TR14 and through TR13 where the signal is also sent to TR8 which passes it on to CPU pin 33 on negative going of IC15 pin 13. When outputting this data in PLAY mode, the CPU pulls IC13 pin 12 (TR14 Collector) low for approx. (20ms with TMEPO set at FAST).



SEQUENCER BOARD

79318120 (pcb 22915869)

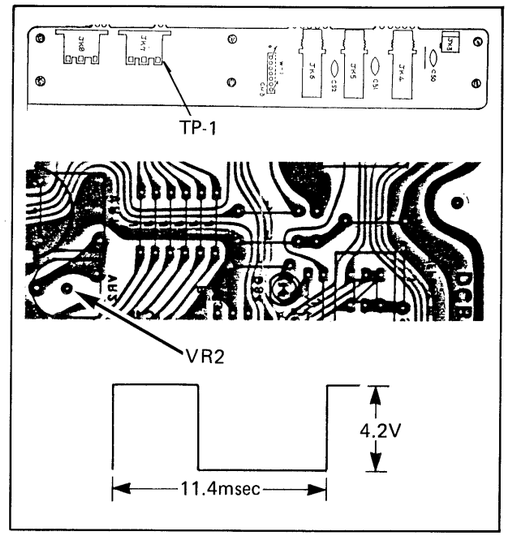
View from foil side



ADJUSTMENT

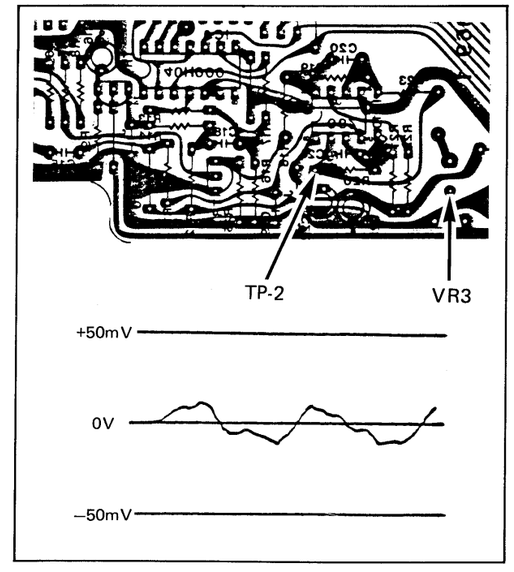
TEMPO

1. Set TEMPO to FAST. 2. Connect the oscilloscope to TP-1 SYNC CLK. 3 Adjust the VR 2 so that 1 clock period is 11 msecs. (88Hz, 220 beat/min.). 4. Set TEMPO at SLOW. Check if the clock is within 62-83 msecs.



TAPE INTERFACE OFFSET

1. Connect the oscilloscope to TP-2 (R20) as shown in the figure.
2. Leave LOAD jack unconnected.
3. Adjust the VR-3 so that the voltage is less than 5 mVp-p.



CIRCUIT DIAGRAM

TMP80C50AP

IC8

IC9

IC10 062

IC1

IC2

IC3

IC4

IC5

IC6

IC7 HM6264LP

IC11

IC12

IC13

IC14

IC15

IC16

IC17

IC18

M82C51

M54527

40H373

40H174

40H138

40H004

40H000

74LS14

40H032

40H089U8

TP-1

TP-2

SAVE

LOAD

DCB

AMPHENOL DDK 57-30140

MEMORY BACK UP CAP.

POWER SW1

SW2 MODE

SW3 METRONOME LEVEL

BUZZER

TEMPO

MAIN BOARD

NOTES

UNLESS OTHERWISE SPECIFIED:

1) ALL PNP TRANSISTORS — 2SA1015 (GR or Y)
2) ALL NPN TRANSISTORS — 2SC1815 (GR or Y)
3) ALL DIODES — 1S2473
LED: TLUR 124
SLB 26 UR, GG, YY

SYNC OUT

For synchronization with the instrument(s) being linked, START/STOP is supplied to SYNC OUT socket from IC13 pin 2 via TR11 which inverts the signal. While SYNC clocks are generated on pin 28 of the CPU at a 24 clocks/quater note. In the TAPE mode, CPU pin 38 goes high, canceling bias on TR19 base, blocking the clocks.

BUZZER

BUZZER transistor TR15 is associated with TRs 16, 17, 18 and 20 to create various tones.

BEEP

When the CPU detects an error (see "ERROR" of the Owner's manual) it forward biases (pin 27 low) base-emitter junction of TR20, activating TR15 by the grounding TR18.

METORONOME

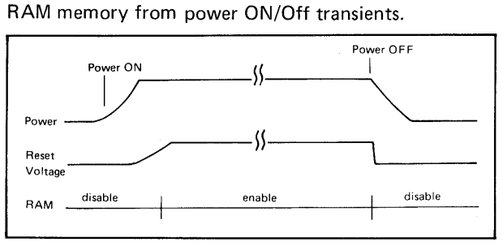
CLICK Pin 30 of the CPU turns to high. TR15 emitter feels a ground via TR16.

ACCENT Both pins 29 and 30 go high. In this case TR17 drives TR20, connecting TR18 in parallel with TR16.

MEMORY PROTECTION

RESET

TRs 3, 4, 5 and surrunding RC time constants protect RAM memory from power ON/Off transients.



RAM BACK-UP

During Power Off As long as JSQ-60 is fed with power through an AC adaptor, VDD is maintained by the TR6 irrespective of POWER SW1 position.

With AC Adaptor Disconnected C8, a high capacitance, low leakage capacitor can retain the memory for one day.

C8 should not be replaced by ordinary capacitor.

RAM CHECK

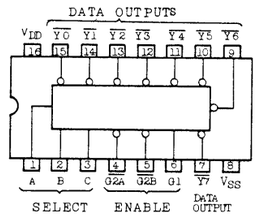
The RAM diagnostic program is contained in JSQ-60. RAM check procedures are as follows;

1. Set MODE SW to LOAD/PLAY or TAPE mode and REPEAT PLAY to OFF.
2. Turn the power ON while pressing simultaneously the LOAD, PLAY and REST buttons. While the above three buttons are held down, the RAM check program is executed.
3. If RAM is normal, 25% and 5% Memory Indicators light up and the buzzer beeps continuously. If it is abnormal, the Memory Indicators flash and the buzzer sounds intermittently.
   To exit RAM check either release one of the three LOAD PLAY or REST buttons, or turn the power OFF.

IC DATA

TC40H138P

Pin Configuration (Top View)



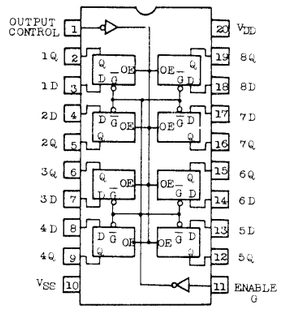
Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	A	B	C	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
L	※	※	※	※	※	H	H	H	H	H	H	H	H
※	H	※	※	※	※	H	H	H	H	H	H	H	H
※	※	H	※	※	※	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

※ : Don't care

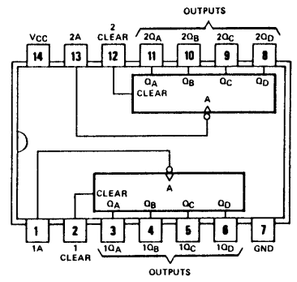
TC40H373P

Pin Configuration (Top View)



TC40H393P

Pin Configuration (Top View)



Count Sequence

COUNT	OUTPUT			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

HM6264LP

Pin Configuration (Top View)