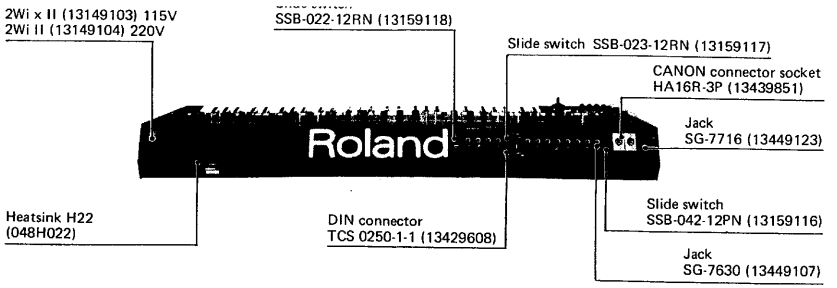
JP-8 SERVICE NOTES

Second Edition
December.1982

This Notes makes First Edition obsolete and consists of two parts:

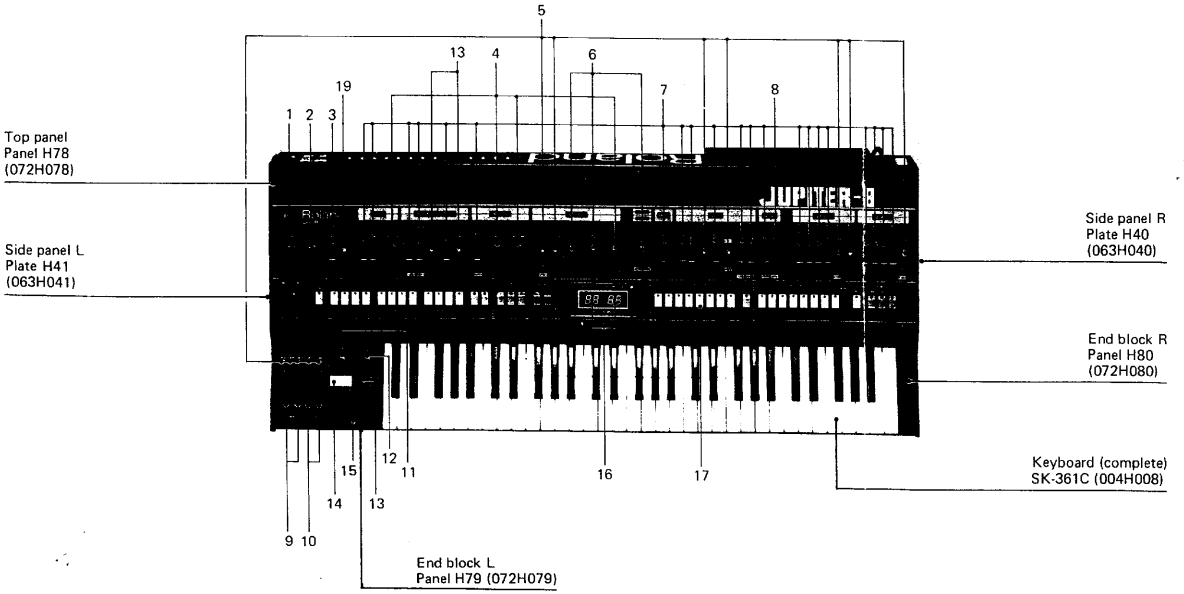
BEFORE READING

PLEASE CHECK FOR CHANGE INFORMATION AND CONTENTS AT PAGES 32 AND 33 OF THIS NOTES.



SPECIFICATIONS

Keyboard:	61 Note, 5 Octaves
VCO	
VCO-2 Fine Tune Range:	±50 Cents
VCF	
Slope:	12/Octave, 24/Octave
Key Follow:	0 – 120%
ENV	
ENV-1, 2	
Attack Time:	1ms – 5s
Decay Time:	1ms – 10s
Sustain Level:	0 – 100%
Release Time:	1ms – 10s
LFO	
Rate:	0.05 – 40Hz
Delay Time:	0 – 4s
Master Tunable Range:	±50%
Arpeggio	
Rate:	1 – 20Hz
Audio Outputs	
Upper:	0dBm, 600 Ohm, Balanced 0dBm/–20dBm, 1k Ohm, Unbalanced
Lower:	0dBm, 600 Ohm, Balanced 0dBm/–20dBm, 1k Ohm, Unbalanced
Highest Note Output	
CV:	0 – 5V
Gate:	Off – 0V, On – +15V
Dimensions:	1063(W) x 485(D) x 120(H)mm
Weight:	22kg
Power Consumption:	90W

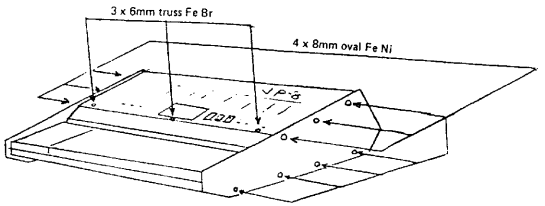


JP-8 PANEL PARTS LIST

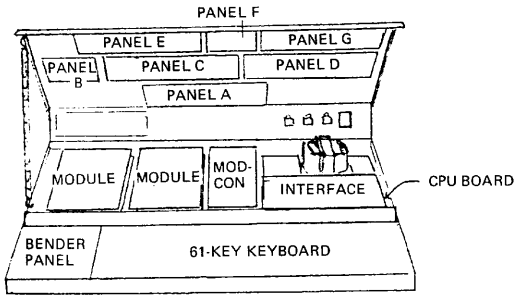
1	Pot.	GM70R-K20B54 (50KB x 2) (13219812)
2	Pot.	GM70R-K20AC54 (50KA, C) (13219811)
3	Pot.	LFE9R-C16A55 (500KA) (13339414)
4	Switch	SRM1034-K15 (13119301)
5	Switch	SLE622-18PS (13139137)
6	Pot.	VM10R-K20B14 (10KB) (13219225)
7	Pot.	LFE9R-C16B14 (10KB) (13339415)
8	Switch	SQPR-24-12P (13159503)
9	Pot.	LFE9R-C16B54 (50KB) (13339413)
10	Pot.	MFE9R-C16B54 (50KB x 2) (13359302)
11	Pot.	VM10R-K20A55 (500KA) (13219231)
12	Pot.	VM10R-K20C54 (50KC) (13219243)
13	Switch	SLE623-18P (13139135)
14	Switch w/key top KEH10003 (13129717) See Parts List for Key top and Switch	
15	Bender assy	PB-4 (029-022)
16	Cover LED	H80 (065H080) LN526RA (15029404)
17	Switch	KHC11901 (13169601)
	Buttons	
	No.1, 38	RED (016H018)
	No.2-5, No.34-37	ORANGE (016H012)
	No.6-9, No.30-33	YELLOW (016H017)
	No.10-13, No.21-28	WHITE (016H010)
	No.14, 15, 29	GREEN (016H014)
	No.16-18, No.39-41	BLUE (016H013)
	No.19, 20	DARK BLUE (016H011)
18	Pot.	VM10A-K15B54 (50KB CT) (13229131)
19	Switch	SLE-622-18P (13139136)
	All rotary knobs	No.68 (016-078)
	All slider knobs	H4 (016H004)

DISASSEMBLY

Remove screws ①, ② and ③.

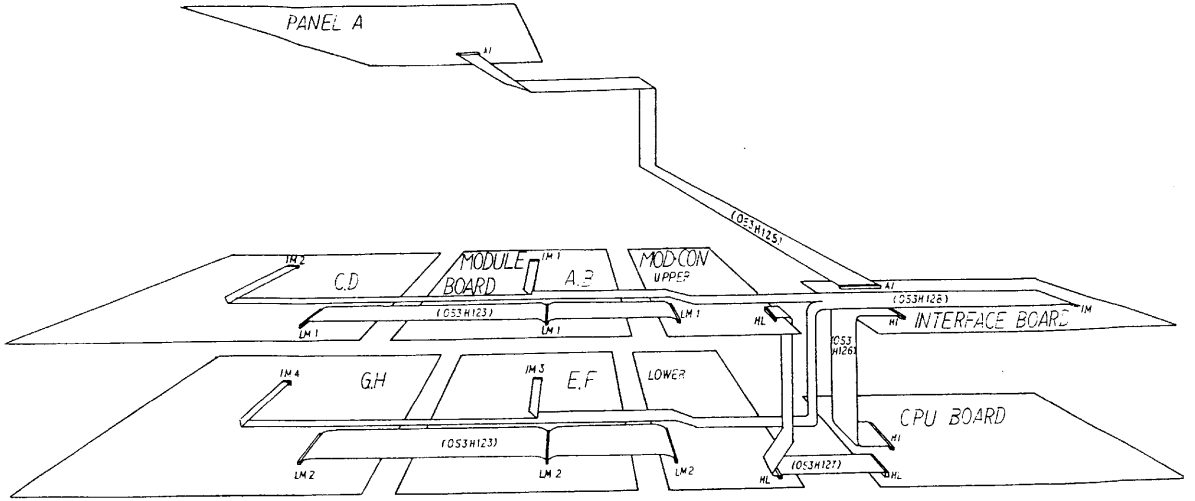


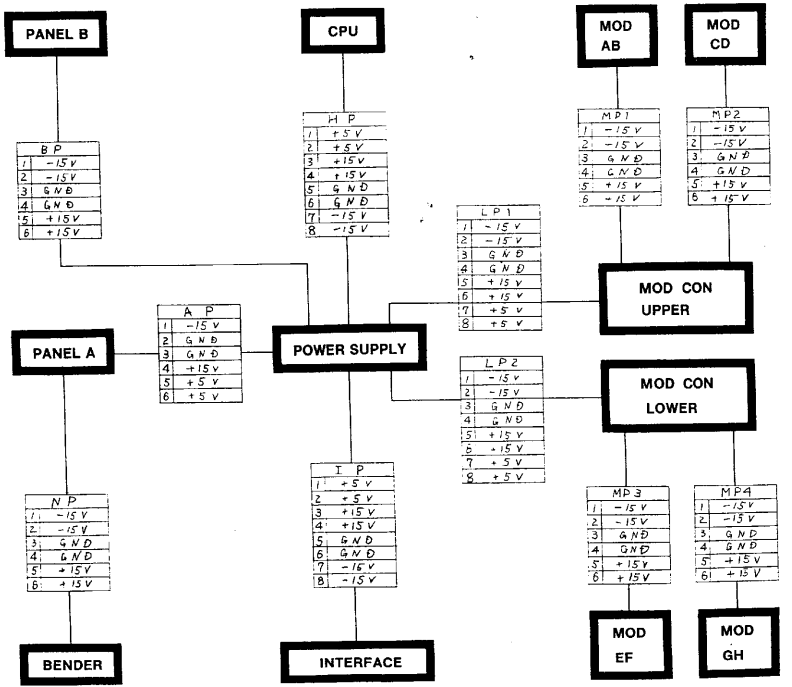
NOTE:
Preparation of a stay and a prop is recommended for a stable top panel rest.

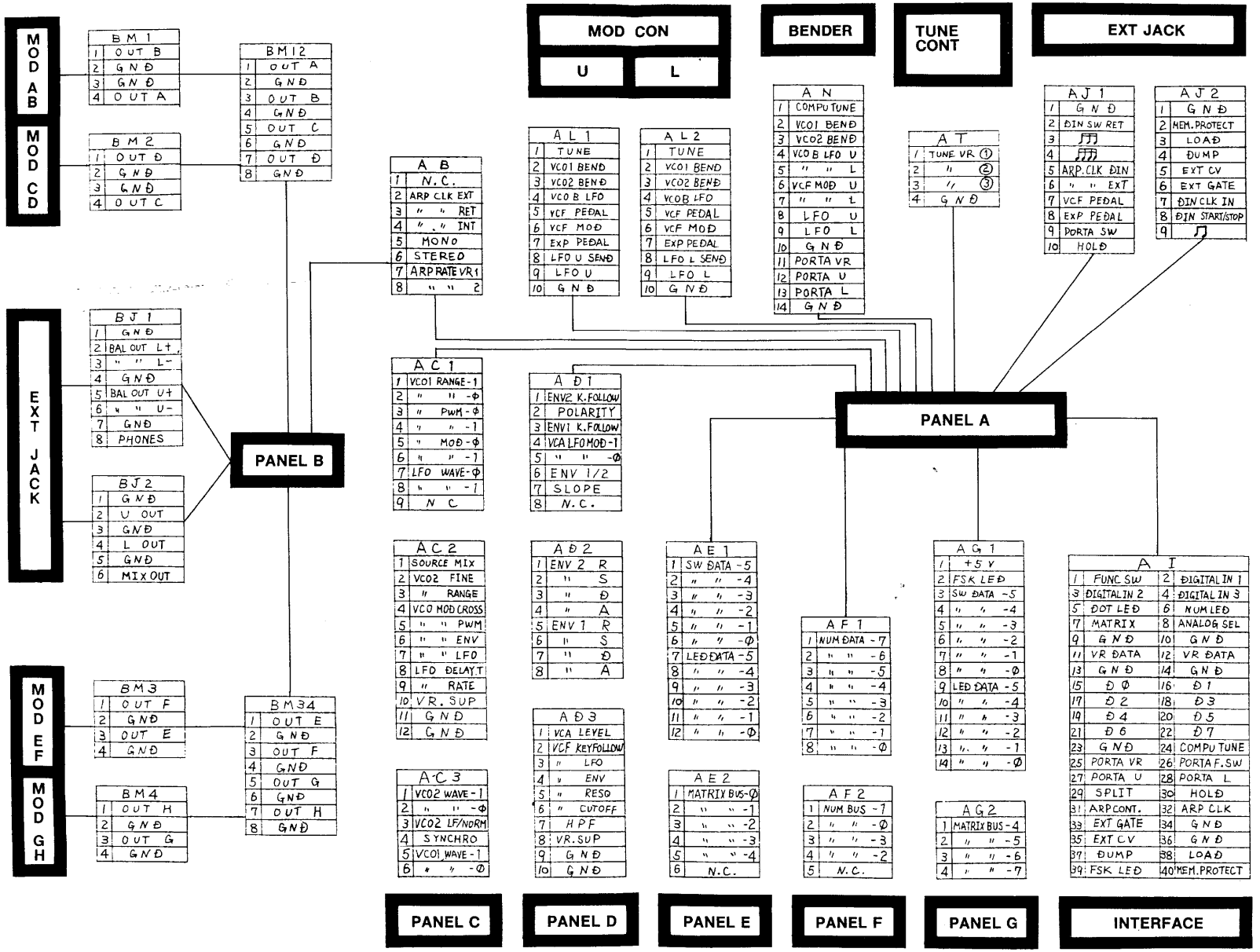


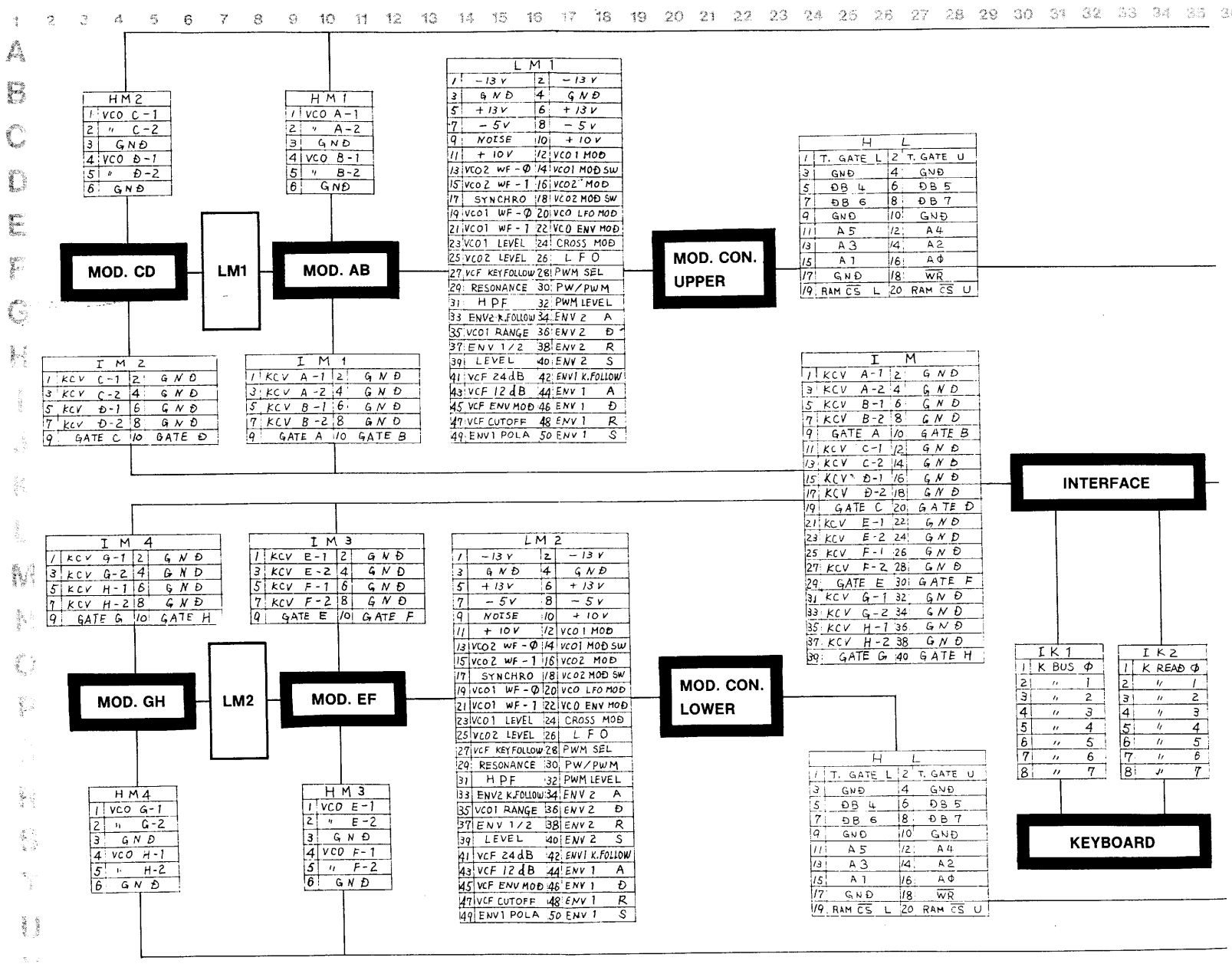
PRECAUTIONS

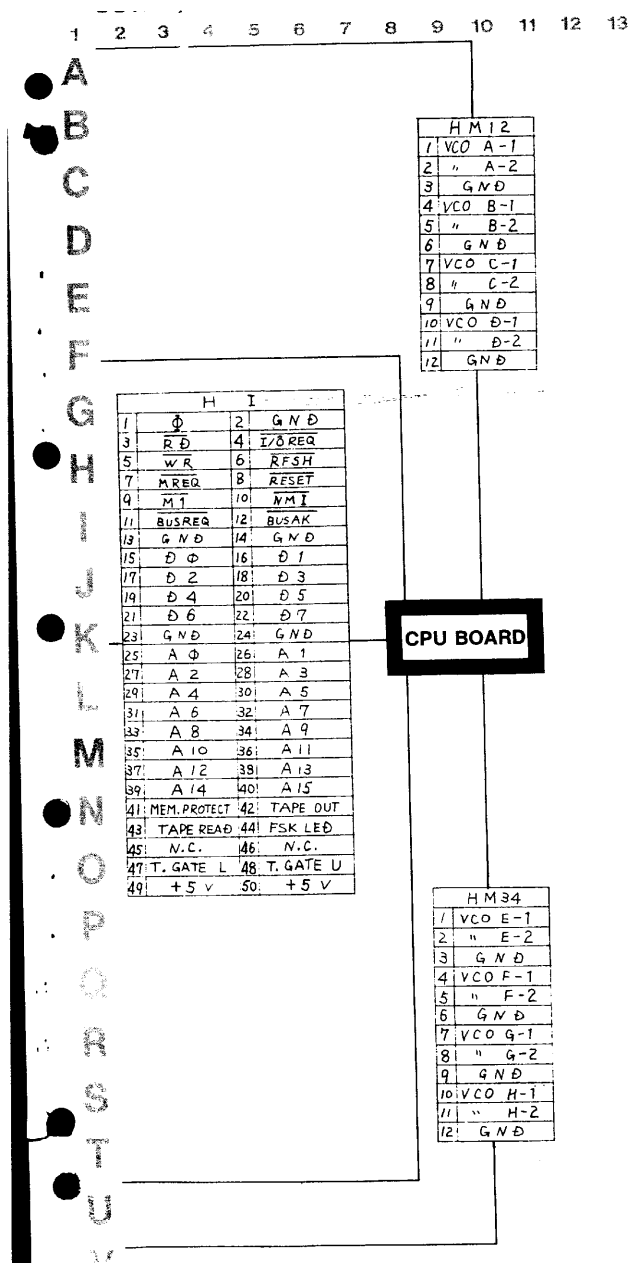
1. Do not pinch flat cables in the pcbs when closing panel assemblies. Prongs on PCBs will pierce humped cable, causing circuits to malfunction. Stretch rolling cable out.
2. Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, PCBs are temperature-sensitive.






MOD AB
MOD CD
BM1
1 OUT B
2 GND
3 GND
4 OUT A
BM2
1 OUT D
2 GND
3 GND
4 OUT C
BM12
1 OUT A
2 GND
3 OUT B
4 GND
5 OUT C
6 GND
7 OUT D
8 GND
MOD CON
U
L
BENDER
TUNE CONT
EXT JACK
AN
1 COMPU TUNE
2 VCO1 BEND
3 VCO2 BEND
4 VCO B LFO U
5 " " L
6 VCF MOD U
7 " " L
8 LFO U
9 LFO L
10 GND
11 PORTA VR
12 PORTA U
13 PORTA L
14 GND
AT
1 TUNE VR ①
2 " ②
3 " ③
4 GND
AJ1
1 GND
2 DIN SW RET
3
4
5 ARP.CLK DIN
6 " " EXT
7 VCF PEDAL
8 EXP PEDAL
9 PORTA SW
10 HOLD
AJ2
1 GND
2 MEM.PROTECT
3 LOAD
4 DUMP
5 EXT CV
6 EXT GATE
7 DIN CLK IN
8 DIN START/STOP
9
AL1
1 TUNE
2 VCO1 BEND
3 VCO2 BEND
4 VCO B LFO
5 VCF PEDAL
6 VCF MOD
7 EXP PEDAL
8 LFO U SEND
9 LFO U
10 GND
AL2
1 TUNE
2 VCO1 BEND
3 VCO2 BEND
4 VCOB LFO
5 VCF PEDAL
6 VCF MOD
7 EXP PEDAL
8 LFO L SEND
9 LFO L
10 GND
AB
1 N.C.
2 ARP CLK EXT
3 " " RET
4 " " INT
5 MONO
6 STEREO
7 ARP RATE VR1
8 " " 2
EXT JACK
BJ1
1 GND
2 BAL OUT L+
3 " " L-
4 GND
5 BAL OUT U+
6 " " U-
7 GND
8 PHONES
BJ2
1 GND
2 U OUT
3 GND
4 L OUT
5 GND
6 MIX OUT
PANEL B
PANEL A
AC1
1 VCO1 RANGE-1
2 " " -Φ
3 " PWM-Φ
4 " " -1
5 " MOD-Φ
6 " " -1
7 LFO WAVE-Φ
8 " " -1
9 N C
AD1
1 ENV2 K.FOLLOW
2 POLARITY
3 ENV1 K.FOLLOW
4 VCA LFO MOD-1
5 " " -Φ
6 ENV 1/2
7 SLOPE
8 N.C.
AC2
1 SOURCE MIX
2 VCO2 FINE
3 " RANGE
4 VCO MOD CROSS
5 " " PWM
6 " " ENV
7 " " LFO
8 LFO DELAY T
9 " RATE
10 VR. SUP
11 GND
12 GND
AD2
1 ENV 2 R
2 " S
3 " Ð
4 " A
5 ENV 1 R
6 " S
7 " Ð
8 " A
AE1
1 SW DATA -5
2 " " -4
3 " " -3
4 " " -2
5 " " -1
6 " " -Φ
7 LED DATA -5
8 " " -4
9 " " -3
10 " " -2
11 " " -1
12 " " -Φ
AF1
1 NUM DATA -7
2 " " -6
3 " " -5
4 " " -4
5 " " -3
6 " " -2
7 " " -1
8 " " -Φ
AG1
1 +5 V
2 FSK LED
3 SW DATA -5
4 " " -4
5 " " -3
6 " " -2
7 " " -1
8 " " -Φ
9 LED DATA -5
10 " " -4
11 " " -3
12 " " -2
13 " " -1
14 " " -Φ
AI
1 FUNC SW
2 DIGITAL IN 1
3 DIGITAL IN 2
4 DIGITAL IN 3
5 DOT LED
6 NUM LED
7 MATRIX
8 ANALOG SEL
9 GND
10 GND
11 VR DATA
12 VR DATA
13 GND
14 GND
15 D0
16 D1
17 D2
18 D3
19 D4
20 D5
21 D6
22 D7
23 GND
24 COMPU TUNE
25 PORTA VR
26 PORTA F.SW
27 PORTA U
28 PORTA L
29 SPLIT
30 HOLD
31 ARP CONT.
32 ARP CLK
33 EXT GATE
34 GND
35 EXT CV
36 GND
37 DUMP
38 LOAD
39 FSK LED
40 MEM.PROTECT
MOD EF
MOD GH
BM3
1 OUT F
2 GND
3 OUT E
4 GND
BM4
1 OUT H
2 GND
3 OUT G
4 GND
BM34
1 OUT E
2 GND
3 OUT F
4 GND
5 OUT G
6 GND
7 OUT H
8 GND
AC3
1 VCO2 WAVE-1
2 " " -Φ
3 VCO2 LF/NORM
4 SYNCHRO
5 VCO1 WAVE-1
6 " " -Φ
AD3
1 VCA LEVEL
2 VCF KEYFOLLOW
3 " LFO
4 " ENV
5 " RESO
6 " CUTOFF
7 HPF
8 VR.SUP
9 GND
10 GND
AE2
1 MATRIX BUS-Φ
2 " " -1
3 " " -2
4 " " -3
5 " " -4
6 N.C.
AF2
1 NUM BUS -1
2 " " -Φ
3 " " -3
4 " " -2
5 N.C.
AG2
1 MATRIX BUS -4
2 " " -5
3 " " -6
4 " " -7
PANEL C
PANEL D
PANEL E
PANEL F
PANEL G
INTERFACE

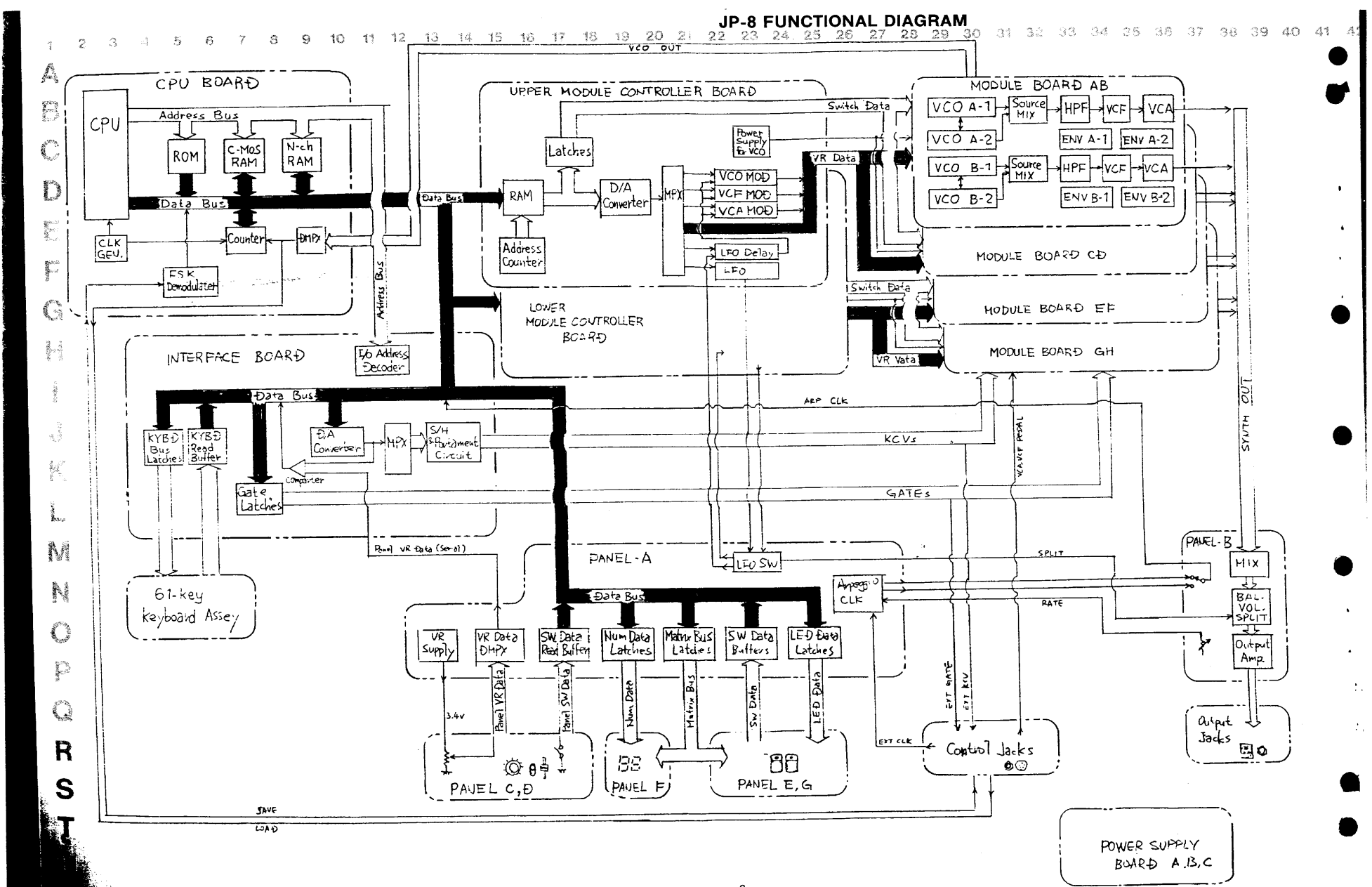

MOD. CD
LM1
MOD. AB
MOD. CON. UPPER
MOD. GH
LM2
MOD. EF
MOD. CON. LOWER
INTERFACE
KEYBOARD
HM2
1 VCO C-1
2 " C-2
3 GND
4 VCO D-1
5 " D-2
6 GND
HM1
1 VCO A-1
2 " A-2
3 GND
4 VCO B-1
5 " B-2
6 GND
LM1
1 -13V 2 -13V
3 GND 4 GND
5 +13V 6 +13V
7 -5V 8 -5V
9 NOISE 10 +10V
11 +10V 12 VCO1 MOD
13 VCO2 WF-Φ 14 VCO1 MOD SW
15 VCO2 WF-1 16 VCO2 MOD
17 SYNCHRO 18 VCO2 MOD SW
19 VCO1 WF-Φ 20 VCO LFO MOD
21 VCO1 WF-1 22 VCO ENV MOD
23 VCO1 LEVEL 24 CROSS MOD
25 VCO2 LEVEL 26 LFO
27 VCF KEYFOLLOW 28 PWM SEL
29 RESONANCE 30 PW/PWM
31 HPF 32 PWM LEVEL
33 ENV2 K.FOLLOW 34 ENV 2 A
35 VCO1 RANGE 36 ENV 2 D
37 ENV 1/2 38 ENV 2 R
39 LEVEL 40 ENV 2 S
41 VCF 24dB 42 ENV1 K.FOLLOW
43 VCF 12dB 44 ENV 1 A
45 VCF ENV MOD 46 ENV 1 D
47 VCF CUTOFF 48 ENV 1 R
49 ENV1 POLA 50 ENV 1 S
H L
1 T. GATE L 2 T. GATE U
3 GND 4 GND
5 DB 4 6 DB 5
7 DB 6 8 DB 7
9 GND 10 GND
11 A5 12 A4
13 A3 14 A2
15 A1 16 AΦ
17 GND 18 WR
19 RAM CS L 20 RAM CS U
IM2
1 KCV C-1 2 GND
3 KCV C-2 4 GND
5 KCV D-1 6 GND
7 KCV D-2 8 GND
9 GATE C 10 GATE D
IM1
1 KCV A-1 2 GND
3 KCV A-2 4 GND
5 KCV B-1 6 GND
7 KCV B-2 8 GND
9 GATE A 10 GATE B
IM
1 KCV A-1 2 GND
3 KCV A-2 4 GND
5 KCV B-1 6 GND
7 KCV B-2 8 GND
9 GATE A 10 GATE B
11 KCV C-1 12 GND
13 KCV C-2 14 GND
15 KCV D-1 16 GND
17 KCV D-2 18 GND
19 GATE C 20 GATE D
21 KCV E-1 22 GND
23 KCV E-2 24 GND
25 KCV F-1 26 GND
27 KCV F-2 28 GND
29 GATE E 30 GATE F
31 KCV G-1 32 GND
33 KCV G-2 34 GND
35 KCV H-1 36 GND
37 KCV H-2 38 GND
39 GATE G 40 GATE H
IM4
1 KCV G-1 2 GND
3 KCV G-2 4 GND
5 KCV H-1 6 GND
7 KCV H-2 8 GND
9 GATE G 10 GATE H
IM3
1 KCV E-1 2 GND
3 KCV E-2 4 GND
5 KCV F-1 6 GND
7 KCV F-2 8 GND
9 GATE E 10 GATE F
LM2
1 -13V 2 -13V
3 GND 4 GND
5 +13V 6 +13V
7 -5V 8 -5V
9 NOISE 10 +10V
11 +10V 12 VCO1 MOD
13 VCO2 WF-Φ 14 VCO1 MOD SW
15 VCO2 WF-1 16 VCO2 MOD
17 SYNCHRO 18 VCO2 MOD SW
19 VCO1 WF-Φ 20 VCO LFO MOD
21 VCO1 WF-1 22 VCO ENV MOD
23 VCO1 LEVEL 24 CROSS MOD
25 VCO2 LEVEL 26 LFO
27 VCF KEYFOLLOW 28 PWM SEL
29 RESONANCE 30 PW/PWM
31 HPF 32 PWM LEVEL
33 ENV2 K.FOLLOW 34 ENV 2 A
35 VCO1 RANGE 36 ENV 2 D
37 ENV 1/2 38 ENV 2 R
39 LEVEL 40 ENV 2 S
41 VCF 24dB 42 ENV1 K.FOLLOW
43 VCF 12dB 44 ENV 1 A
45 VCF ENV MOD 46 ENV 1 D
47 VCF CUTOFF 48 ENV 1 R
49 ENV1 POLA 50 ENV 1 S
HM4
1 VCO G-1
2 " G-2
3 GND
4 VCO H-1
5 " H-2
6 GND
HM3
1 VCO E-1
2 " E-2
3 GND
4 VCO F-1
5 " F-2
6 GND
H L
1 T. GATE L 2 T. GATE U
3 GND 4 GND
5 DB 4 6 DB 5
7 DB 6 8 DB 7
9 GND 10 GND
11 A5 12 A4
13 A3 14 A2
15 A1 16 AΦ
17 GND 18 WR
19 RAM CS L 20 RAM CS U
IK1
1 K BUS Φ
2 " 1
3 " 2
4 " 3
5 " 4
6 " 5
7 " 6
8 " 7
IK2
1 K READ Φ
2 " 1
3 " 2
4 " 3
5 " 4
6 " 5
7 " 6
8 " 7

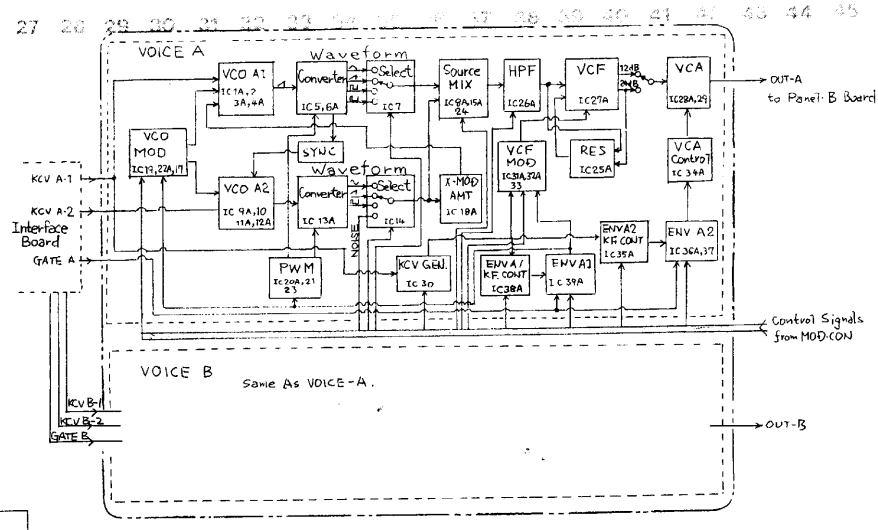


WIRING DATA TABLE

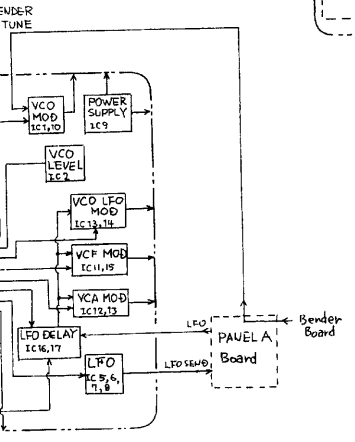
CONNECTOR	PINS	PCB from	PCB to
AB	8	PANEL A	PANEL B
AC1	9	"	PANEL C
AC2	12	"	"
AC3	6	"	"
AD1	8	"	PANEL D
AD2	8	"	"
AD3	10	"	"
AE1	12	"	PANEL E
AE2	6	"	"
AF1	8	"	PANEL F
AF2	5	"	"
AG1	14	"	PANEL G
AG2	4	"	"
AI	40J	"	INTERFACE
AJ1	10	"	EXT JACK
AJ2	9	"	"
AL1	10	"	MOD CON U
AL2	10	"	MOD CON L
AN	14	"	BENDER
AP	6	"	POWER
BJ1	8	PANEL B	EXT JACK
BJ2	6	"	"
BM12 [BM1, BM2]	8 [4, 4]	PANEL B	MODULE AB
			" CD
BM34 [BM3, BM4]	8 [4, 4]	PANEL B	" EF
			" GH
BP	6	PANEL B	PANEL A
HI	50J	CPU	INTERFACE
HL	20J	"	MOD CON
HM12 [HM1, HM2]	12 [6, 6]	CPU	MODULE AB
			" CD
HM34 [HM3, HM4]	12 [6, 6]	CPU	" EF
			" GH
HP	8	CPU	POWER
IK1	8	INTERFACE	KEYBOARD
IK2	8	"	"
IM [IM1, IM2, IM3, IM4]	40J [10J, 10J, 10J, 10J]	INTERFACE	MODULE AB
			" CD
			" EF
			" GH
IP	8	INTERFACE	POWER
LM1	50J	MOD CON U	MODULE ABCD
LM2	50J	" L	MODULE EFGH
LP1	8	" U	POWER
LP2	8	" L	"
MP1	6	MODULE AB	MOD CON U
MP2	6	" CD	"
MP3	6	" EF	MOD CON L
MP4	6	" GH	"
NP	6	BENDER	PANEL A
AT	4	PANEL A	TUNE VR

JP-8 FUNCTIONAL DIAGRAM



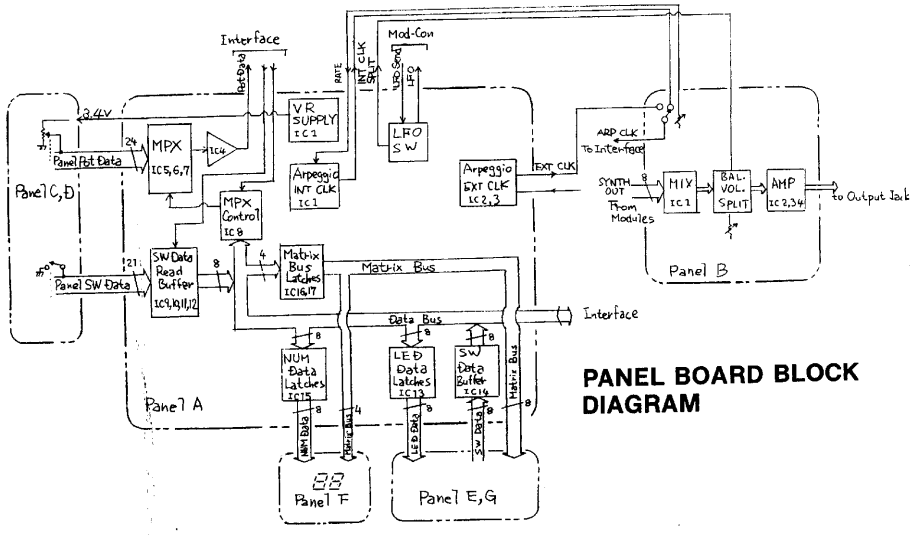


MODULE BOARD BLOCK DIAGRAM

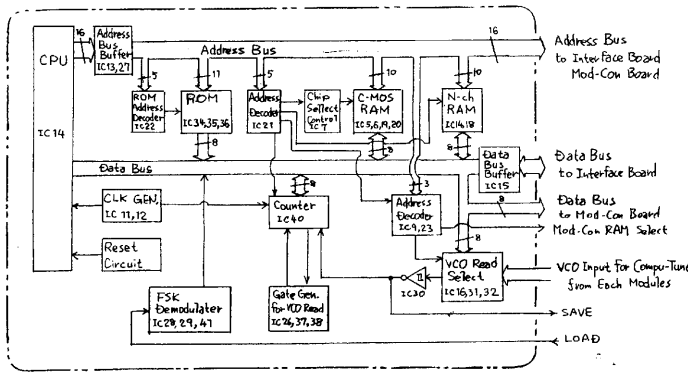


D BLOCK DIAGRAM

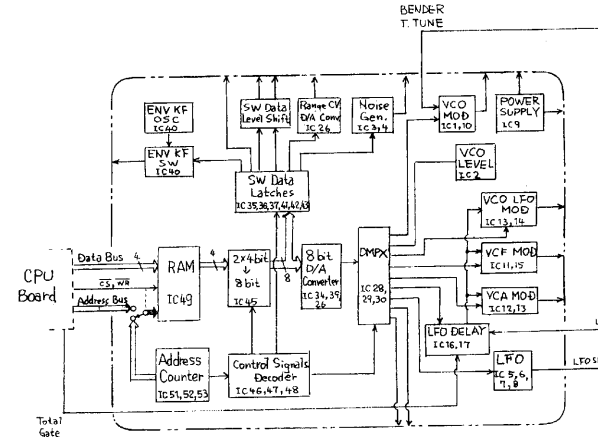
DESTINATION
MODULE BOARD.



PANEL BOARD BLOCK DIAGRAM

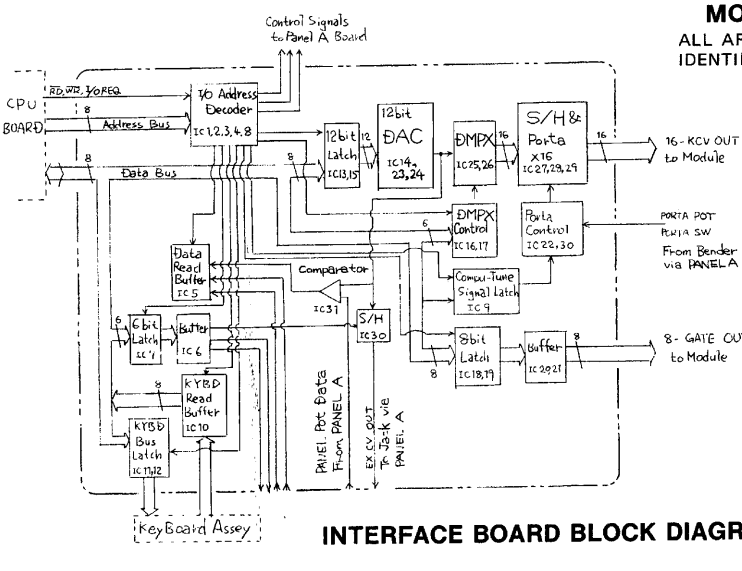


CPU BOARD BLOCK DIAGRAM

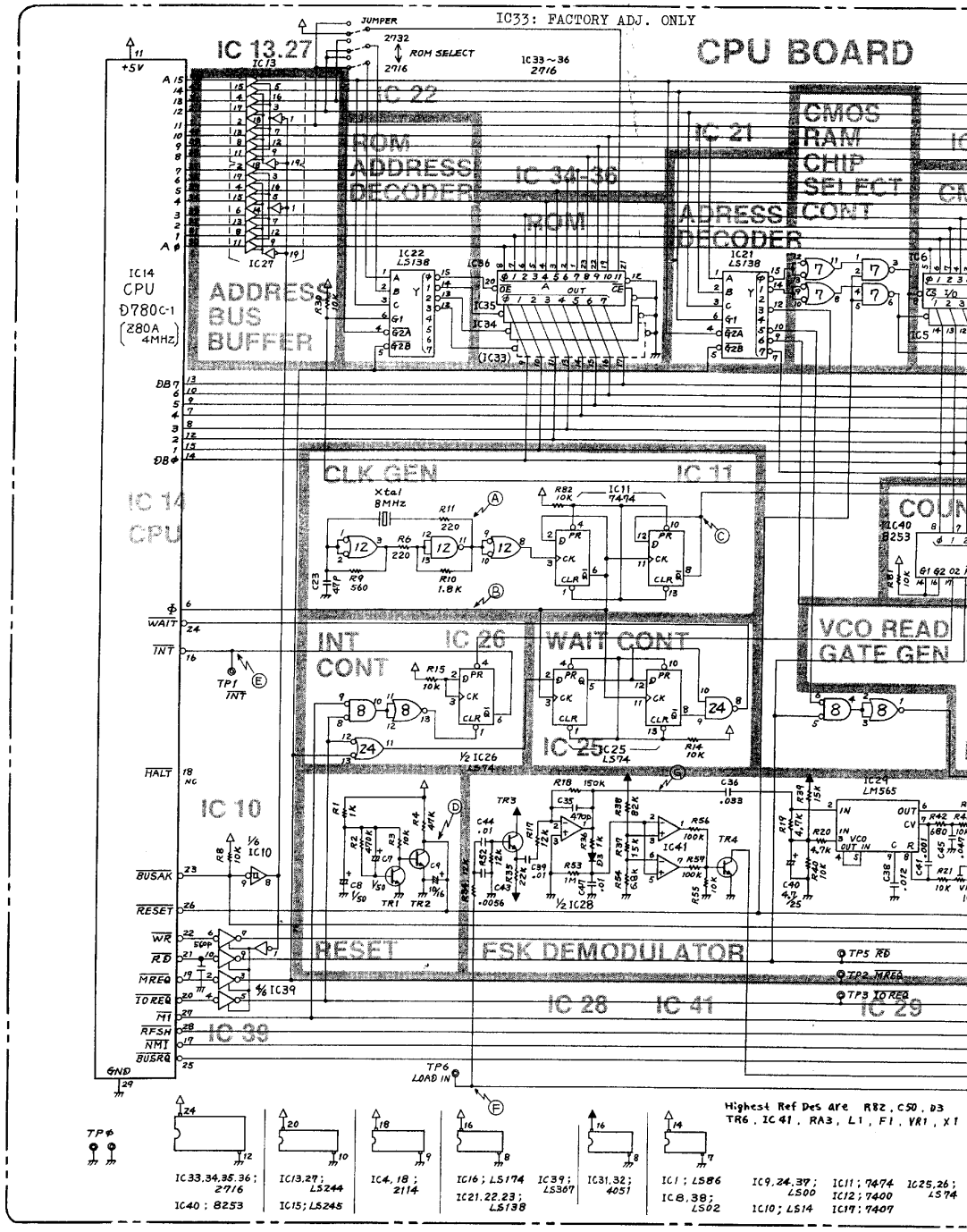


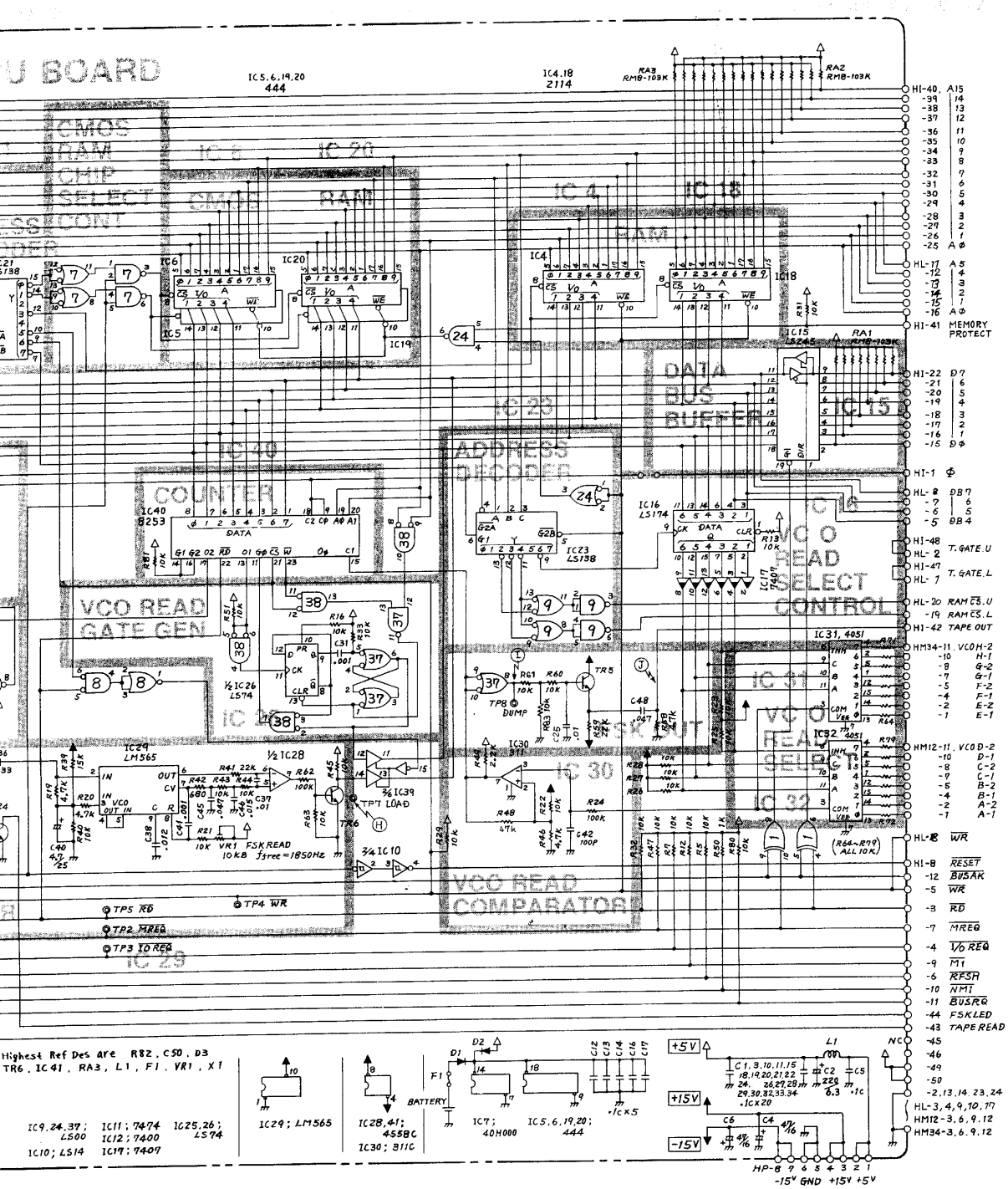
MOD-CON BOARD BLOCK DIAGRA

ALL ARROWS HAVING NO DESTINATION IDENTIFIER CONNECT TO MODULE BOARD.

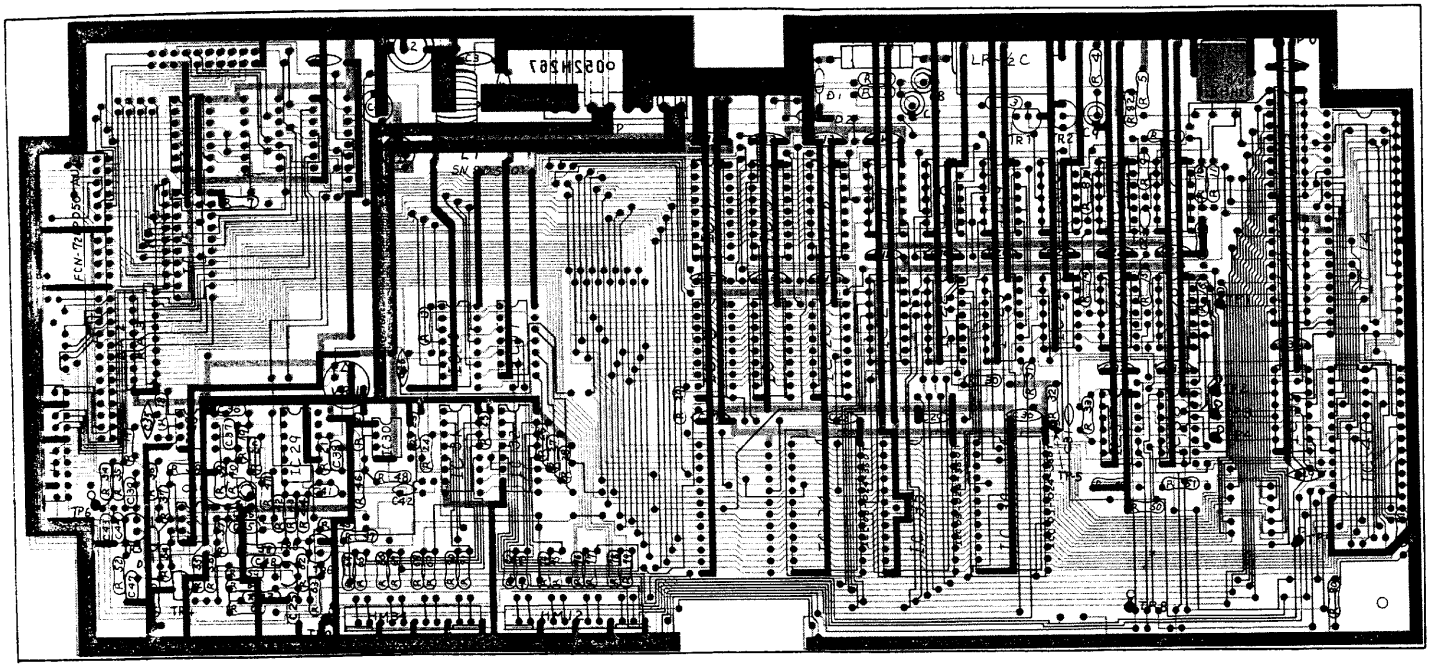


INTERFACE BOARD BLOCK DIAGRAM


IC33: FACTORY ADJ. ONLY
CPU BOARD
IC 13.27
JUMPER
2732
ROM SELECT
2716
IC33~36
2716
IC 22
ROM ADDRESS DECODER
IC 34-36
ROM
IC 21
CMOS RAM CHIP SELECT CONT
ADDRESS DECODER
IC14 CPU D780C-1 (Z80A 4MHz)
ADDRESS BUS BUFFER
CLK GEN
IC 11
Xtal 8MHz
IC 14 CPU
INT CONT
IC 26
WAIT CONT
IC 25
VCO READ GATE GEN
IC 10
RESET
FSK DEMODULATOR
IC 28
IC 41
IC 29
IC 39
TP1 INT
TP6 LOAD IN
TP5 RD
TP2 MREQ
TP3 IOREQ
Highest Ref Des are R82, C50, D3 TR6, IC 41, RA3, L1, F1, VR1, X1
IC33,34,35,36; 2716
IC40; 8253
IC13,27; LS244
IC15; LS245
IC4,18; 2114
IC16; LS174
IC21,22,23; LS138
IC39; LS367
IC31,32; 4051
IC1; LS86
IC8,38; LS02
IC9,24,37; LS00
IC10; LS14
IC11; 7474
IC12; 7400
IC17; 7407
IC25,26; LS74
125ns
250ns
500ns
Power On
Power Off
1ms.
min 1.5V PP
max 4V PP
on "SAVE" mode
on "LOAD" mode
FSK Freq. "H"=2100Hz
"L"=1300Hz


U BOARD
IC5,6,19,20
444
IC4,18
2114
RA3
RMB-103K
RA2
RMB-103K
CMOS RAM CHIP SELECT CONT
IC 6
IC 20
CMOS RAM
IC 4
IC 18
RAM
IC6
IC20
IC5
IC19
IC4
IC18
IC15
LS245
RA1
RMB-103K
DATA BUS BUFFER
IC 15
IC 40
IC 25
ADDRESS DECODER
IC 16
COUNTER
IC40
8253
DATA
IC23
LS138
IC16
LS174
VCO READ SELECT CONTROL
VCO READ GATE GEN
IC 26
IC 31
IC 32
IC31, 4051
IC32, 4051
IC29
LM565
½ IC28
IC30
311
IC 30
VCO READ COMPARATOR
¾ IC10
TP7 LOAD
TP8 DUMP
TR5
TR6
FSK READ
10kB fFree=1850Hz
TP5 RD
TP4 WR
TP2 MREQ
TP3 IO REQ
IC 29
HI-40, A15
-39 14
-38 13
-37 12
-36 11
-35 10
-34 9
-33 8
-32 7
-31 6
-30 5
-29 4
-28 3
-27 2
-26 1
-25 A0
HL-17 A5
-12 4
-13 3
-14 2
-15 1
-16 A0
HI-41 MEMORY PROTECT
HI-22 D7
-21 6
-20 5
-19 4
-18 3
-17 2
-16 1
-15 D0
HI-1 Φ
HL-8 DB7
-7 6
-6 5
-5 DB4
HI-48 T. GATE.U
HL-2 T. GATE.L
HI-47 T. GATE.L
HL-7
HL-20 RAM CS.U
-19 RAM CS.L
HI-42 TAPE OUT
HM34-11, VCO H-2
-10 H-1
-8 G-2
-7 G-1
-5 F-2
-4 F-1
-2 E-2
-1 E-1
HM12-11, VCO D-2
-10 D-1
-8 C-2
-7 C-1
-5 B-2
-4 B-1
-2 A-2
-1 A-1
HL-18 WR
HI-8 RESET
-12 BUSAK
-5 WR
-3 RD
-7 MREQ
-4 IO REQ
-9 M1
-6 REFSH
-10 NMI
-11 BUSRQ
-44 FSKLED
-43 TAPE READ
-45
-46
-49
-50
-2,13,14,23,24
HL-3,4,9,10,17
HM12-3,6,9,12
HM34-3,6,9,12
(R64~R79 ALL 10K)
Highest Ref Des are R82, C50, D3
TR6, IC41, RA3, L1, F1, VR1, X1
IC9,24,37; LS00
IC11; 7474
IC12; 7400
IC25,26; LS74
IC10; LS14
IC19; 7407
IC29; LM565
IC28,41; 4558C
IC30; 311C
IC7; 40H000
IC5,6,19,20; 444
BATTERY
+5V
+15V
-15V
C1,3,10,11,15 18,19,20,21,22 24,26,27,28 29,30,32,33,34 .1cx20
C2 220
6.3 .1c
C5
C6 4.7/16
C4 4.7/16
L1
NC
HP-8 7 6 5 4 3 2 1
-15V GND +15V +5V

CPU BOARD OPH121(149H121)(pcb 052H267)



R25J

2SC1815-GR

LC-2S

SR19R

152473

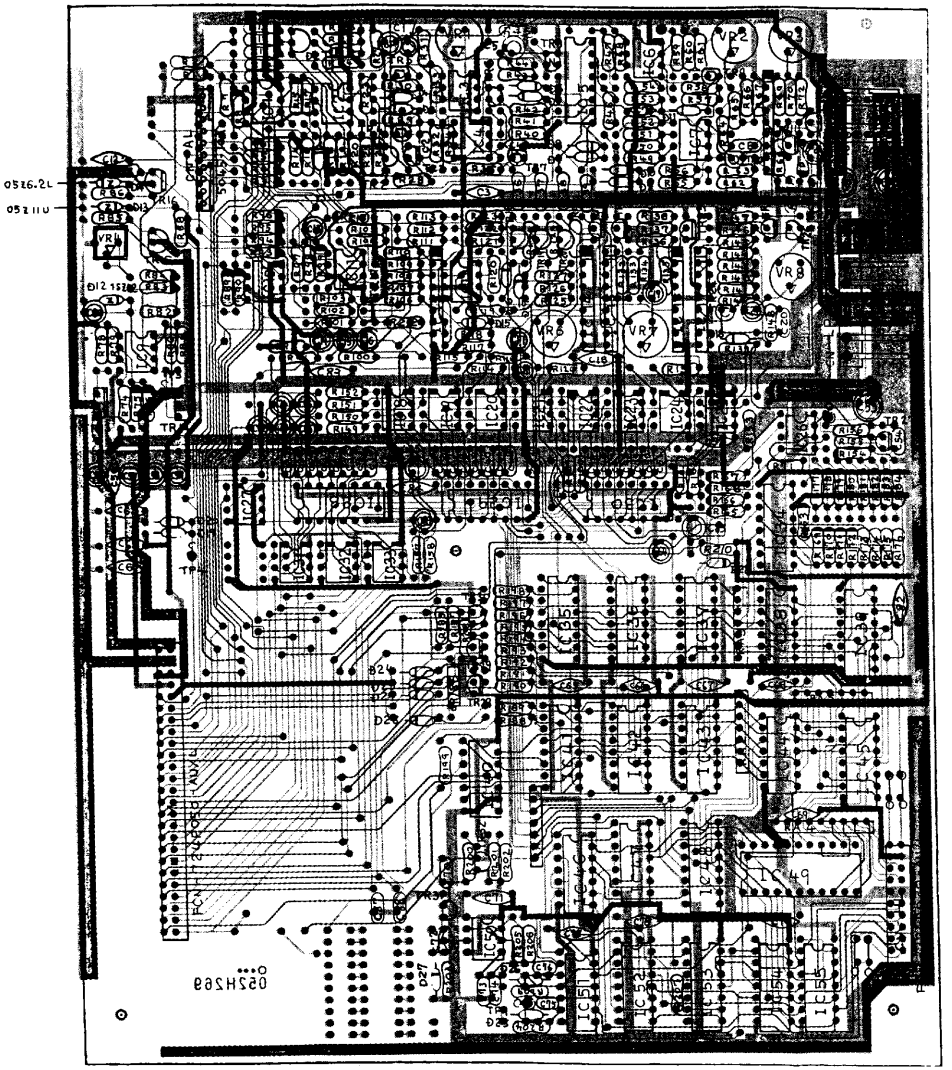
RM8-103K

Refer to Page 38 for:

CPU CHANGE INFORMATION

CAUTIONS ON MODULE CONTROLLER BOARD REPLACEMENT
RAM (MOD CON BOARD) REPLACEMENT

CPU BOARD WILL BE AFFECTED BY THESE REPLACEMENTS



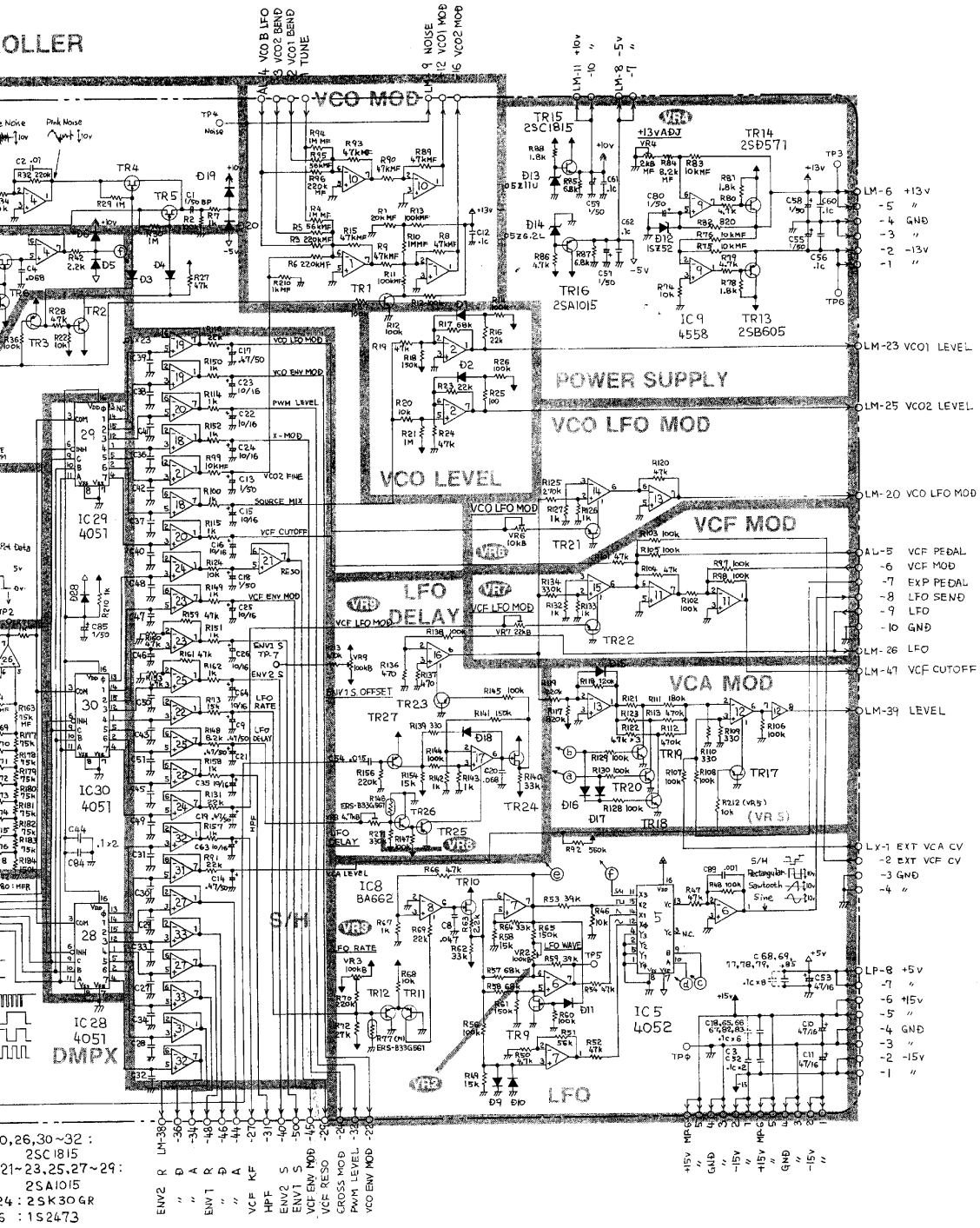
MODULE CONTROLLER

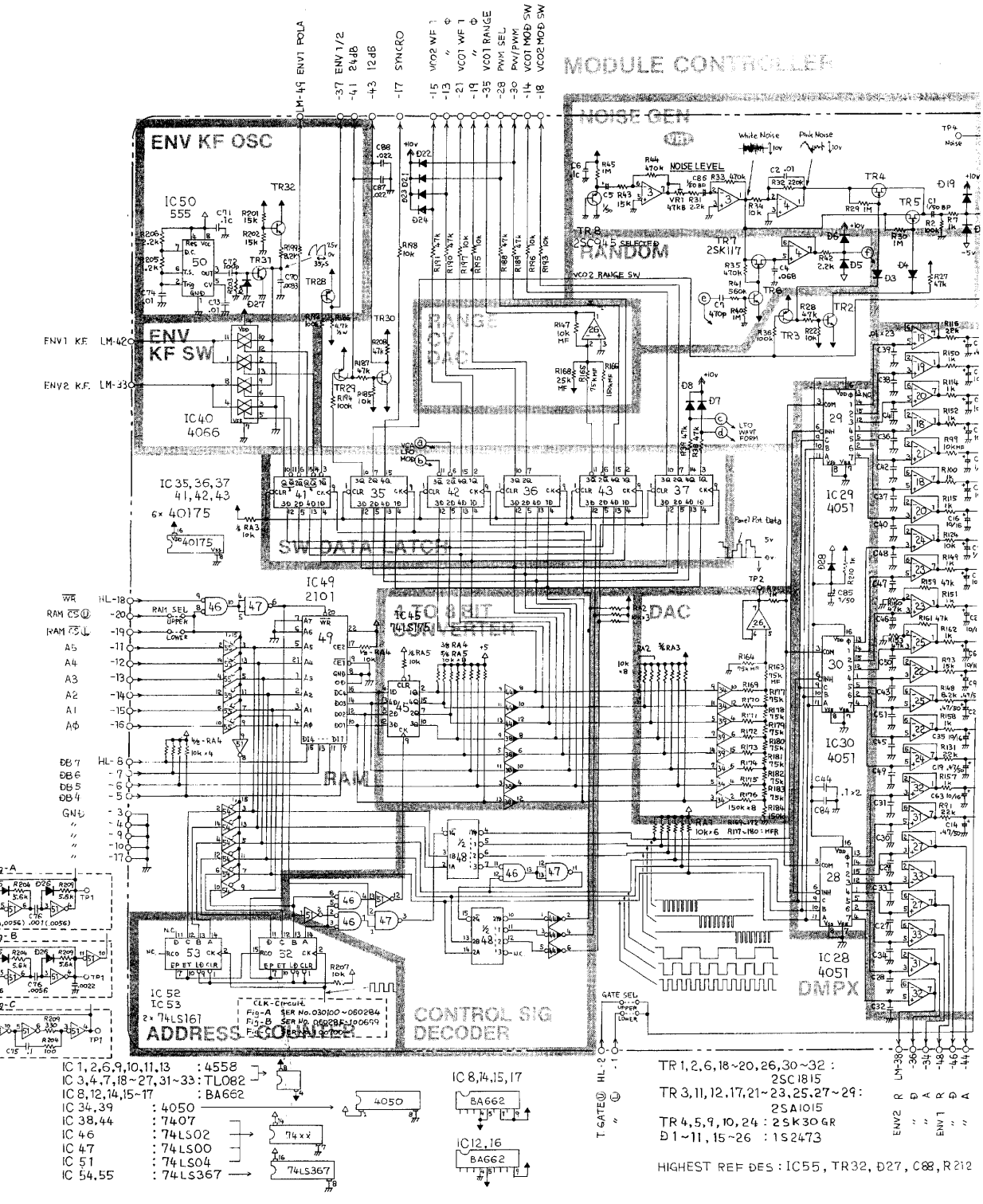
OPH123(149H123) (pcb 052H269)

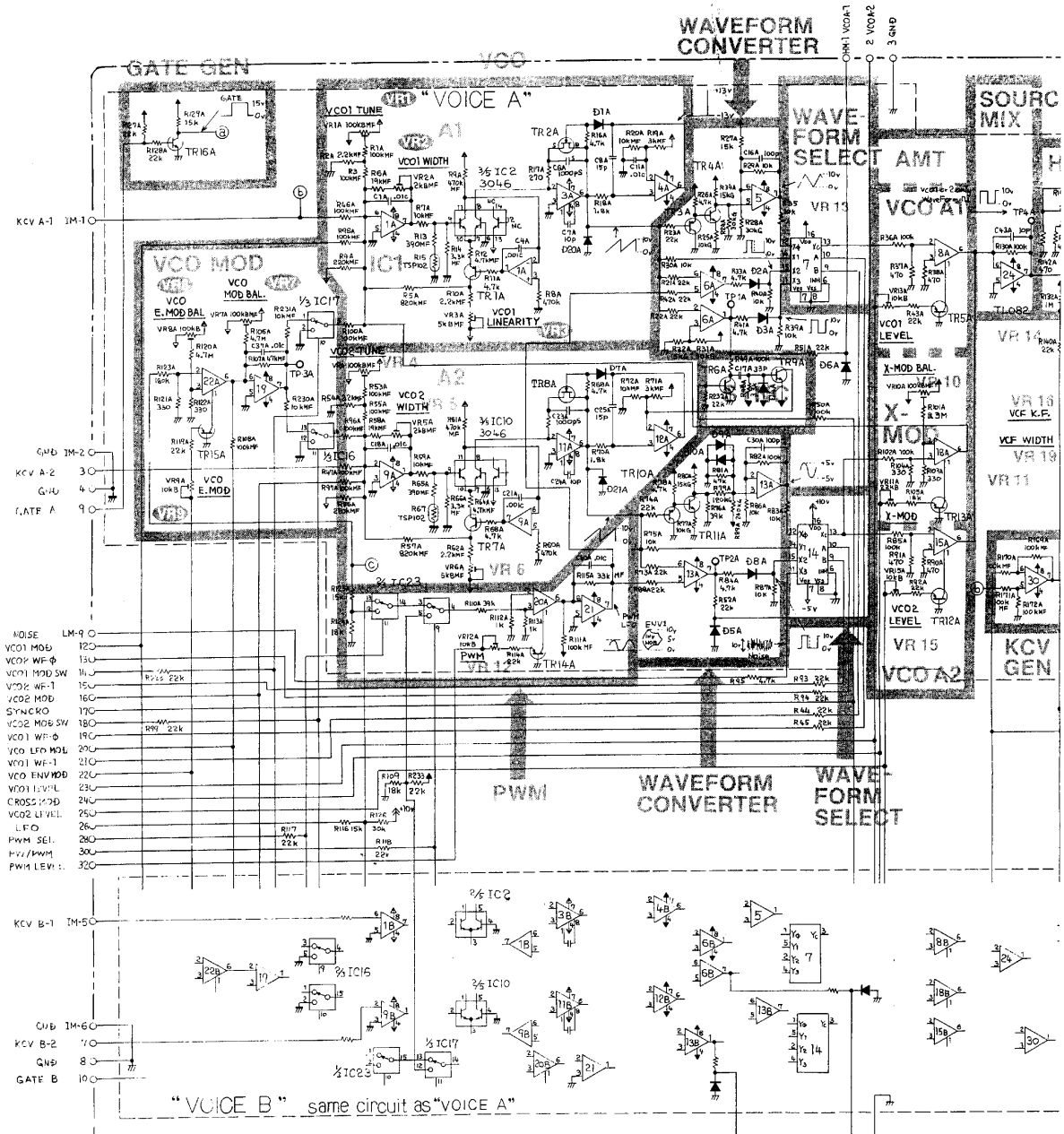
SN 090600-192099

REFER TO PAGES
49–50 for SN up to 090599
36–37 for SN 202100-up
37–38 for PCB or RAM REPLACEMENT

selected on current leakage white dot
R 50J
¼w carbon R25
¼w metal film CRB25FX
posister ERS-C33G561
1S2473
zener diode
5R19R
ET-6P
2SA1015-GR
2SC1815-GR
2SC945 selected for Noise
2SK30A-GR
2SK117-GR
2SB605
2SD571
BA662
Resistor array
BA662A selected on offset
bi-polar
test point LC-2-S


OLLER
VCO MOD
VCO B LFO
VCO2 BEND
VCO1 BEND
TUNE
NOISE
VCO1 MOD
VCO2 MOD
POWER SUPPLY
VCO LFO MOD
VCO LEVEL
VCF MOD
LFO DELAY
VCA MOD
S/H
LFO
DMPX
IC29 4051
IC30 4051
IC28 4051
IC8 BA662
IC5 4052
IC9 4558
TR15 2SC1815
TR14 2SD571
TR16 2SA1015
TR13 2SB605
LM-6 +13v
-5 "
-4 GND
-3 "
-2 -13v
-1 "
LM-23 VCO1 LEVEL
LM-25 VCO2 LEVEL
LM-20 VCO LFO MOD
AL-5 VCF PEDAL
-6 VCF MOD
-7 EXP PEDAL
-8 LFO SEND
-9 LFO
-10 GND
LM-26 LFO
LM-47 VCF CUTOFF
LM-39 LEVEL
LX-1 EXT VCA CV
-2 EXT VCF CV
-3 GND
-4 "
LP-8 +5v
-7 "
-6 +15v
-5 "
-4 GND
-3 "
-2 -15v
-1 "
ENV2 R LM-38
ENV2 S -45
ENV1 R -46
ENV1 S -50
VCF KF -27
HPF -31
VCF ENV. MOD -40
VCF RESO -45
CROSS MOD -20
PWM LEVEL -33
VCO ENV MOD -22
0,26,30~32 : 2SC1815
21~23,25,27~29 : 2SA1015
24 : 2SK30GR
5 : 1S2473
DES : IC55, TR32, D27, C88, R212, RA5, VR9


MODULE CONTROLLER
ENV KF OSC
NOISE GEN
RANDOM
RANGE CV DAC
ENV KF SW
SW DATA LATCH
RAM
8 TO 8 BIT MULTIPLEXER
DAC
CONTROL SIG DECODER
ADDRESS COUNTER
IC 1,2,6,9,10,11,13 : 4558
IC 3,4,7,18~27,31~33 : TL082
IC 8,12,14,15~17 : BA662
IC 34,39 : 4050
IC 38,44 : 7407
IC 46 : 74LS02
IC 47 : 74LS00
IC 51 : 74LS04
IC 54,55 : 74LS367
IC 8,14,15,17 BA662
IC12,16 BA662
TR 1,2,6,18~20,26,30~32 : 2SC1815
TR 3,11,12,17,21~23,25,27~29 : 2SA1015
TR 4,5,9,10,24 : 2SK30GR
D 1~11, 15~26 : 1S2473
HIGHEST REF DES : IC55, TR32, D27, C88, R212

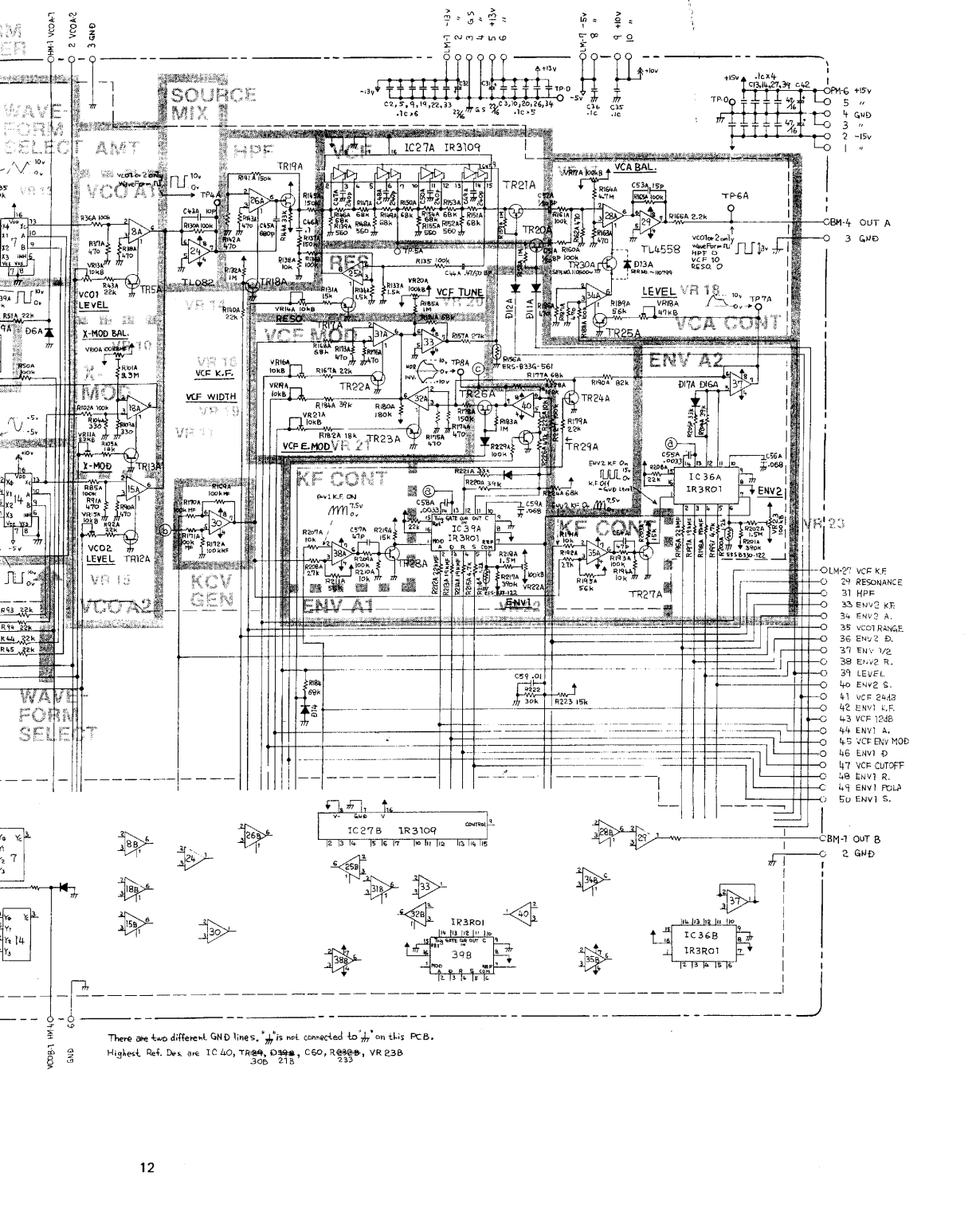


IC 1A, 1B, 5, 9A, 9B, 19, 21, 30, 33, 37, 40 : 4558
IC 2, 10 : RC3046
IC 3A, 3B, 4A, 4B, 11A, 11B, 12A, 12B, 35A, 35B, 38A, 38B : TL080
IC 6A, 6B, 13A, 13B, 24 : TL082
IC 7, 14 : 4052
IC 8A, 8B, 15A, 15B, 18A, 18B, 20A, 20B, 22A, 22B, 25A, 25B, 26A, 26B, 28A, 28B, 31A, 31B, 32A, 32B, 34A, 34B : BA662
IC 16, 17, 23 : 4053
IC 27A, 27B : IR3109
IC 29 : TL455B or NJM4559DD
IC 36A, 36B, 39A, 39B : IR3R01

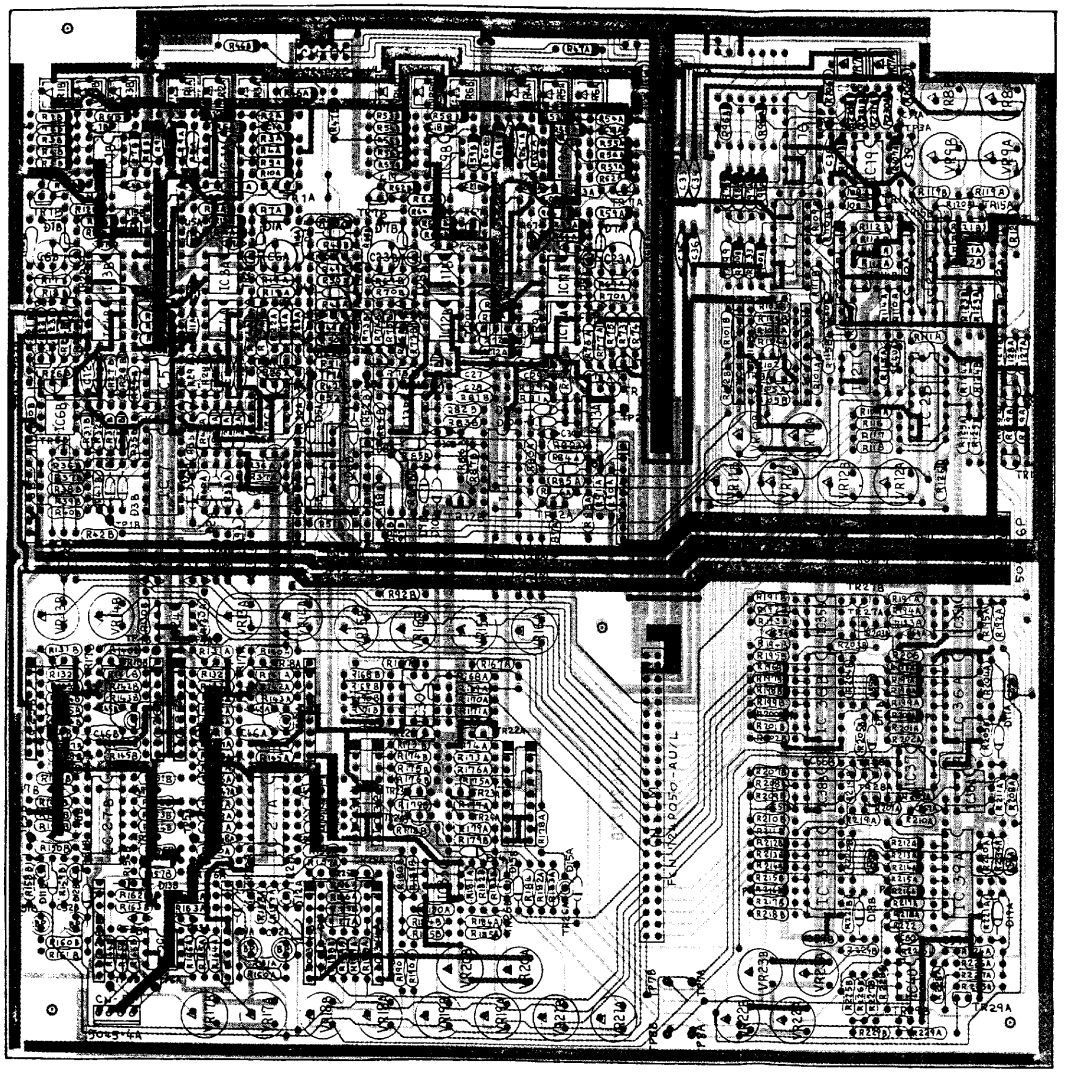
All PNP TR : 2SA1015-GR
TR 4A, 4B, 9A, 9B, 11A, 11B : 2SC752-Y
Other NPN TR : 2SC1815-GR
TR 24, 28, 8A, 8B Other FET : NF510
All Diode : 2SK30A-GR
: 1S2473

There are two different GND l
Highest Ref. Des are IC 40,

MODULE BOARD CIRCUIT DIAGRUM



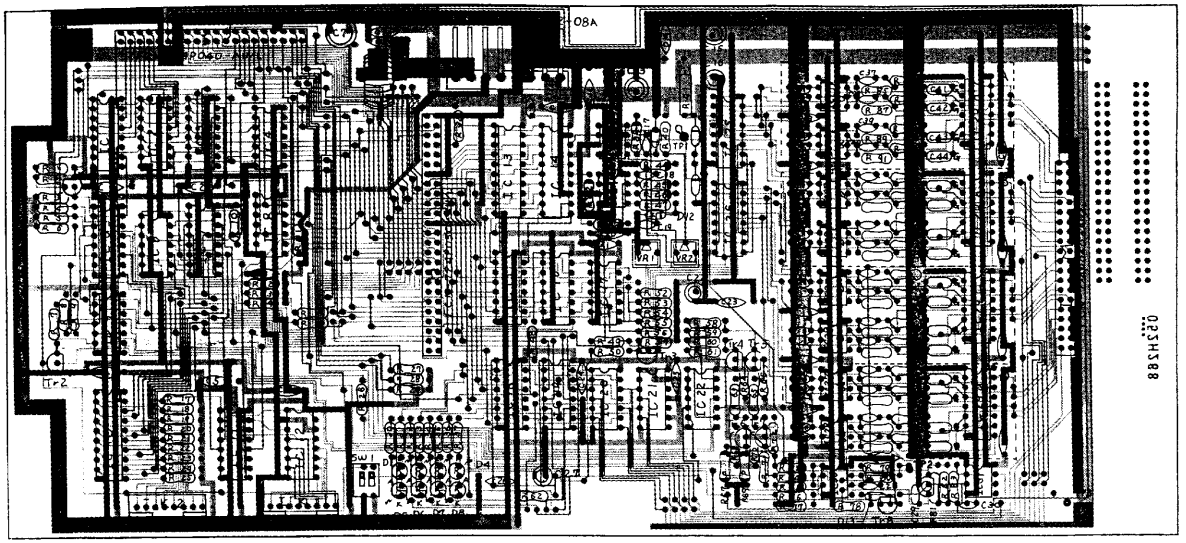
There are two different GND lines. "//" is not connected to "//" on this PCB.
Highest Ref. Des. are IC 40, TR~~39~~ 30b, D~~38~~ 21B, C60, R~~232~~ 233, VR 23B



MODULE BOARD
OPH124(149H124)
(pcb 052H270)

SEE PAGE 48
For SN up to 090599

R25G
selected on slew rate
TL08C 8pcs
C82 5pcs
carbon R25
metal film RB25FX
POS. STEPERS-C33G561
P posistor TSP102
2SA1015-GR
2SC1815-GR
2SC1752-Y
2SK30A-GR
NE510
1S2473
BA662
ET-6P
A or B
selected on VF(gm)
replacement should be
of the existing
Selected on offset
10 pcs
white dot
SR19
test point LC-2S (TP-G: GND)
polystylem film
bi-polar

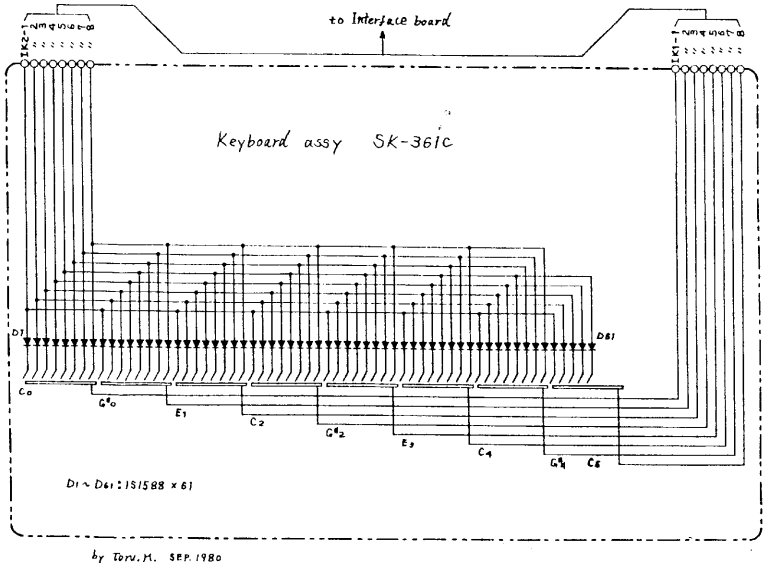


See pp. 34–35 for SN171700 and up

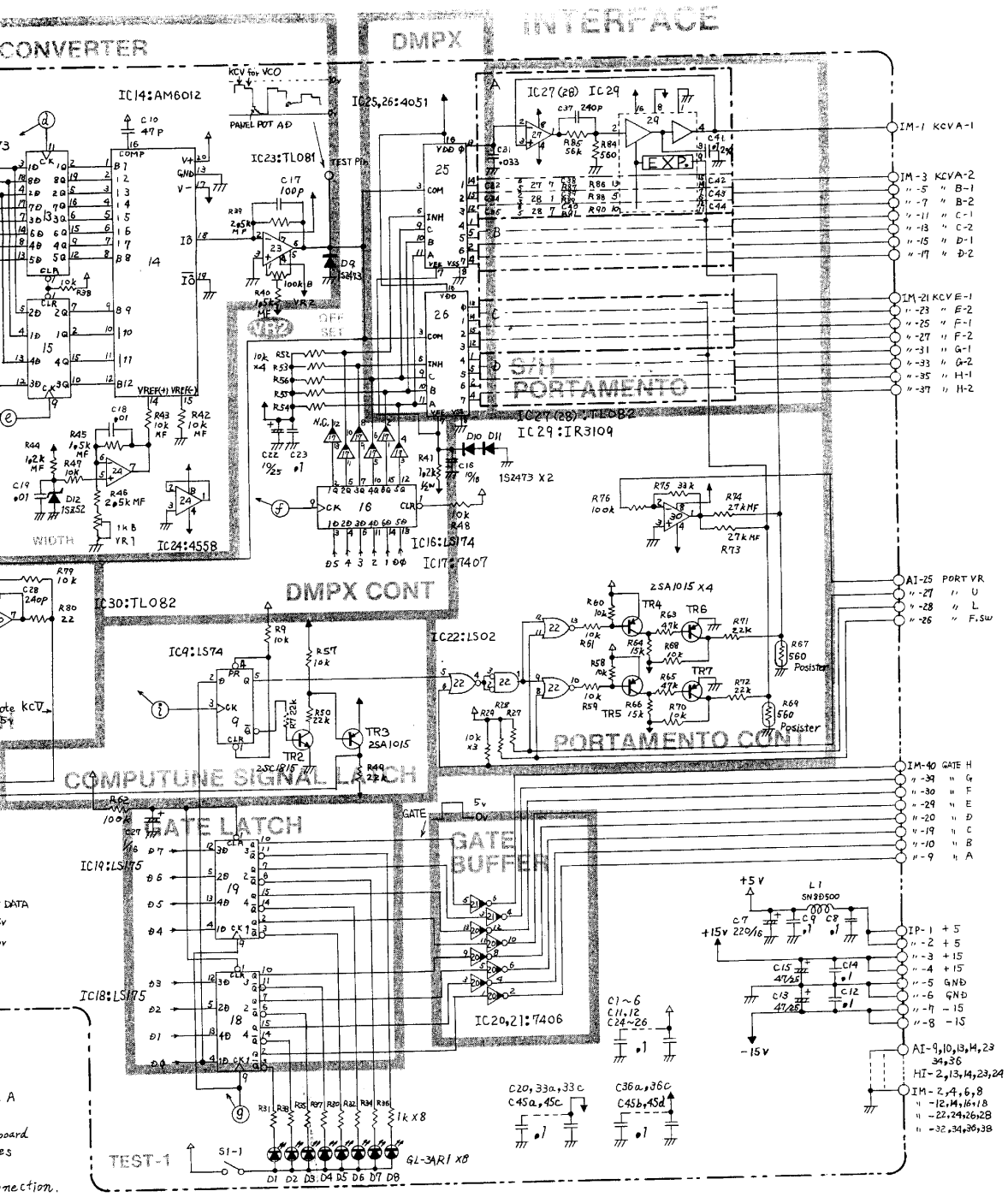
CAUTION

When replacing Interface board bearing edition no. 052H268 (and below) with PCB of 052H268 (and above), refer to pp. 34 and 35 for PROMs versions of CPU borad.

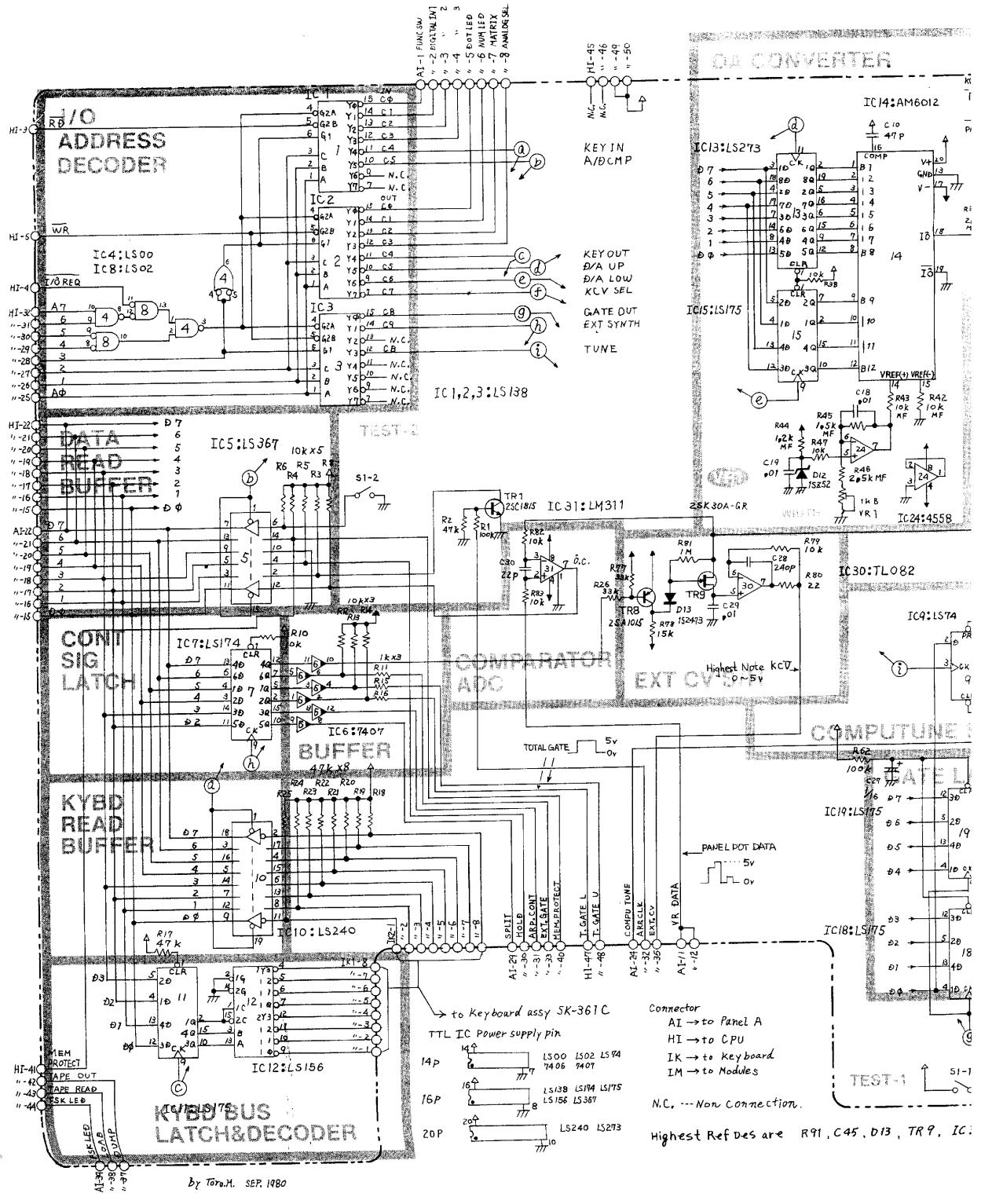
R25J
CRB25FX
POSISTOR
ERS-C33G561
R50J
ET-6P
TL082
Selected on current leakage
2SC1815-GR
2SA1015-GR
2SK30A-GR
1S2473
1S1588
LED GL-3ARI

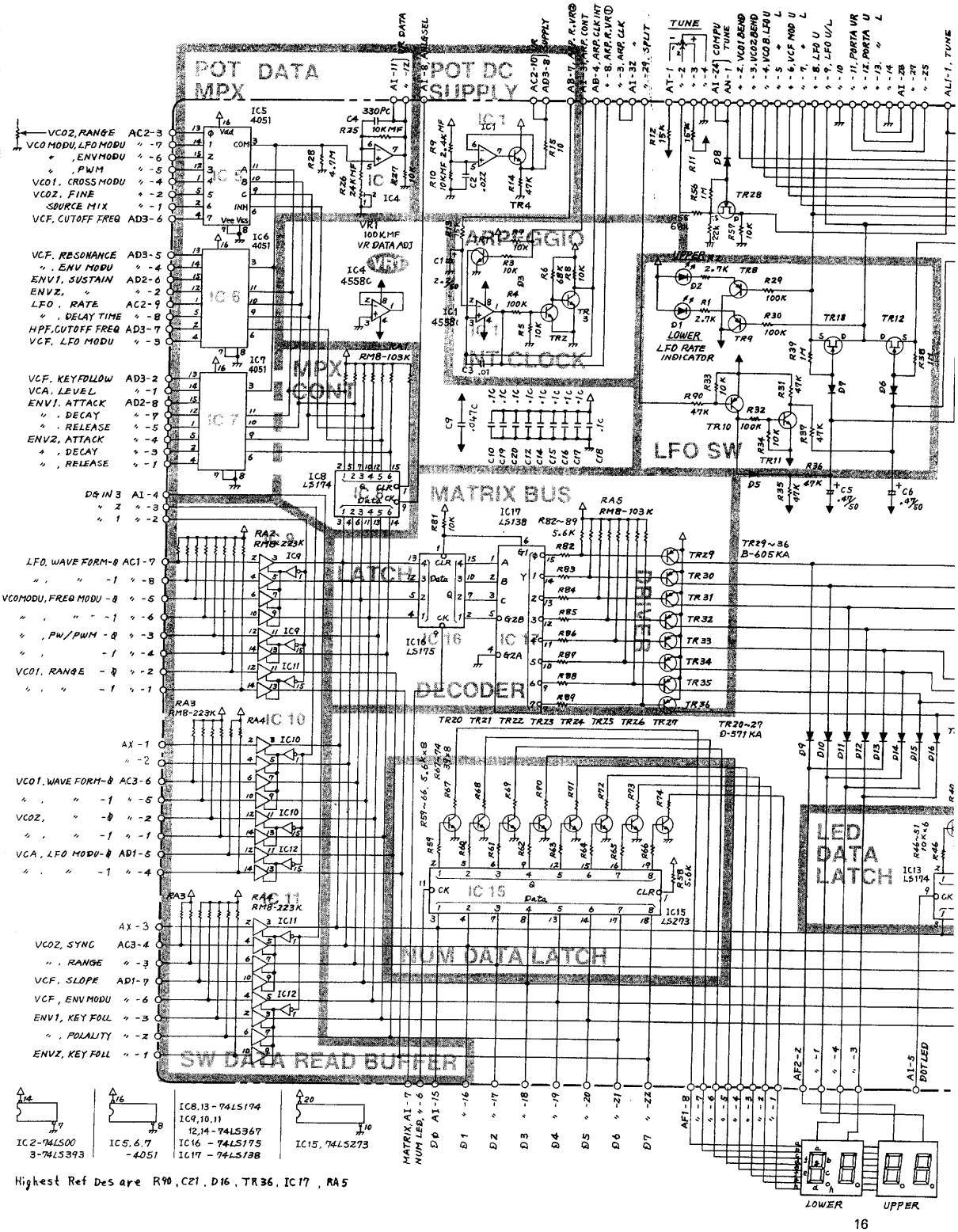


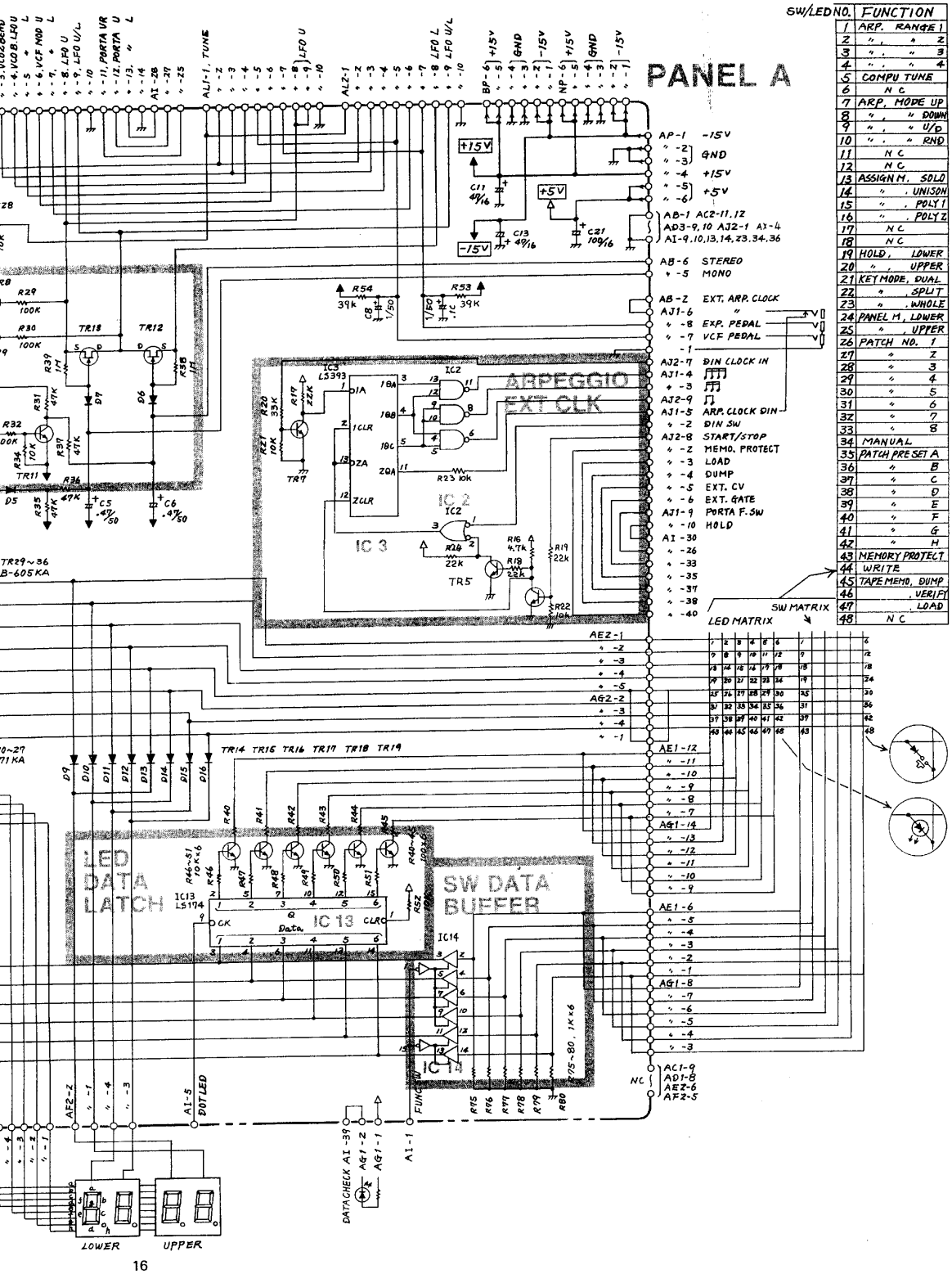
by Toru.M. SEP. 1980



are R91, C45, D13, TR9, IC31, VR2, L1, SW1


I/O ADDRESS DECODER
IC1,2,3:LS138
IC4:LS00
IC8:LS02
KEY IN A/D CMP
KEY OUT D/A UP D/A LOW KCV SEL
GATE OUT EXT SYNTH
TUNE
D/A CONVERTER
IC14:AM6012
IC13:LS273
IC15:LS175
IC24:4558
DATA READ BUFFER
IC5:LS367
CONT SIG LATCH
IC7:LS174
BUFFER
IC6:7407
COMPARATOR ADC
EXT CV
IC31:LM311
IC30:TL082
Highest Note KCV
KYBD READ BUFFER
IC10:LS240
IC12:LS156
KYBD BUS LATCH&DECODER
IC9:LS74
IC19:LS175
IC18:LS175
TOTAL GATE
PANEL POT DATA
to Keyboard assy SK-361C
TTL IC Power supply pin
14P LS00 LS02 LS74 74C06 74C07
16P LS138 LS174 LS175 LS156 LS367
20P LS240 LS273
Connector
AI → to Panel A
HI → to CPU
IK → to Keyboard
IM → to Modules
N.C. --- Non Connection.
Highest Ref Des are R91, C45, D13, TR9, IC
TEST-1
TEST-2
by Toru.M. SEP. 1980

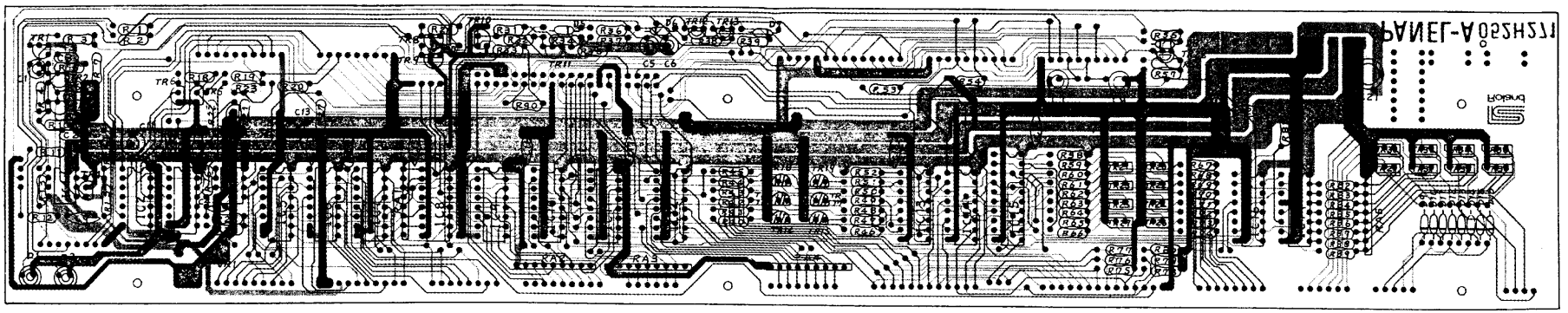

POT DATA MPX
POT DC SUPPLY
MPX CONT
ARPEGGIO
INT CLOCK
LFO SW
MATRIX BUS
DECODER
LATCH
LED DATA LATCH
NUM DATA LATCH
SW DATA READ BUFFER
TUNE
VCO2, RANGE AC2-3
VCO MODU, LFO MODU
, ENV MODU
, PWM
VCO1, CROSS MODU
VCO2, FINE
SOURCE MIX
VCF, CUTOFF FREQ AD3-6
VCF, RESONANCE AD3-5
, ENV MODU
ENV1, SUSTAIN AD2-6
ENV2, AD2-2
LFO, RATE AC2-9
, DELAY TIME
HPF, CUTOFF FREQ AD3-7
VCF, LFO MODU
VCF, KEY FOLLOW AD3-2
VCA, LEVEL
ENV1, ATTACK AD2-8
, DECAY
, RELEASE
ENV2, ATTACK
, DECAY
, RELEASE
D0 IN 3 AI-4
LFO, WAVE FORM-0 AC1-7
VCO MODU, FREQ MODU -0
, PW/PWM -0
VCO1, RANGE -0
VCO1, WAVE FORM-0 AC3-6
VCO2, -0
VCA, LFO MODU-0 AD1-5
VCO2, SYNC AC3-4
, RANGE
VCF, SLOPE AD1-7
VCF, ENV MODU
ENV1, KEY FOLL
, POLARITY
ENV2, KEY FOLL
LOWER
UPPER
IC2-74LS00 3-74LS393
IC5,6,7 - 4051
IC8,13 - 74LS174
IC9,10,11 12,14 - 74LS367
IC16 - 74LS175
IC17 - 74LS138
IC15, 74LS273
Highest Ref Des are R90, C21, D16, TR36, IC17, RA5


PANEL A
SW/LED NO. FUNCTION
1 ARP. RANGE 1
2 " " 2
3 " " 3
4 " " 4
5 COMPU TUNE
6 N C
7 ARP. MODE UP
8 " " DOWN
9 " " U/D
10 " " RND
11 N C
12 N C
13 ASSIGN M. SOLO
14 " " UNISON
15 " " POLY 1
16 " " POLY 2
17 N C
18 N C
19 HOLD, LOWER
20 " " UPPER
21 KEY MODE, DUAL
22 " " SPLIT
23 " " WHOLE
24 PANEL M, LOWER
25 " " UPPER
26 PATCH NO. 1
27 " " 2
28 " " 3
29 " " 4
30 " " 5
31 " " 6
32 " " 7
33 " " 8
34 MANUAL
35 PATCH PRESET A
36 " " B
37 " " C
38 " " D
39 " " E
40 " " F
41 " " G
42 " " H
43 MEMORY PROTECT
44 WRITE
45 TAPE MEMO. DUMP
46 " VERIFY
47 " LOAD
48 N C
ARPEGGIO EXT CLK
IC 3
IC 2
LED DATA LATCH
IC13 LS174
IC 13
SW DATA BUFFER
IC14
IC 14
SW MATRIX
LED MATRIX
LOWER
UPPER
DOT LED
DATACHECK
FUNC
+15V
+5V
-15V
GND

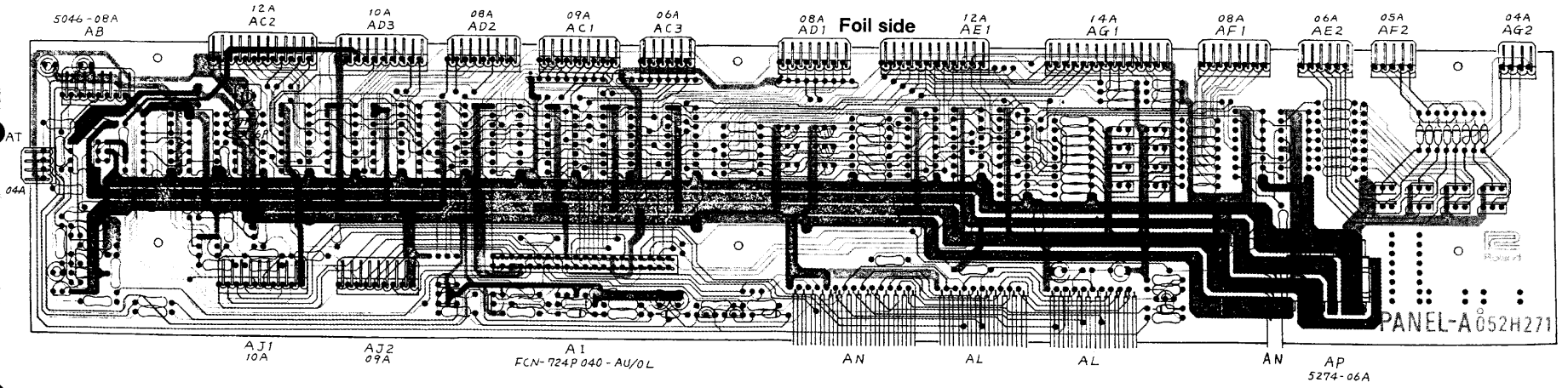
PANEL BOARD A OPH125(149H125) (pcb 052H271)

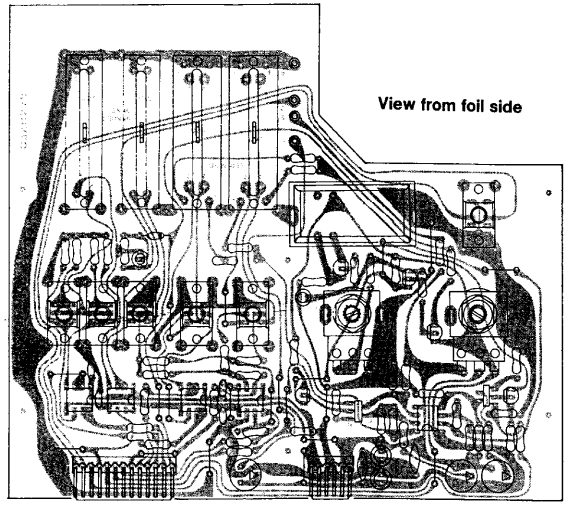
A1015 Y or GR
C1815 Y or GR
C1815 GR
B605 KA
D571 KA
K30A GR
152473
R25J
CR02SFX
Resistor array

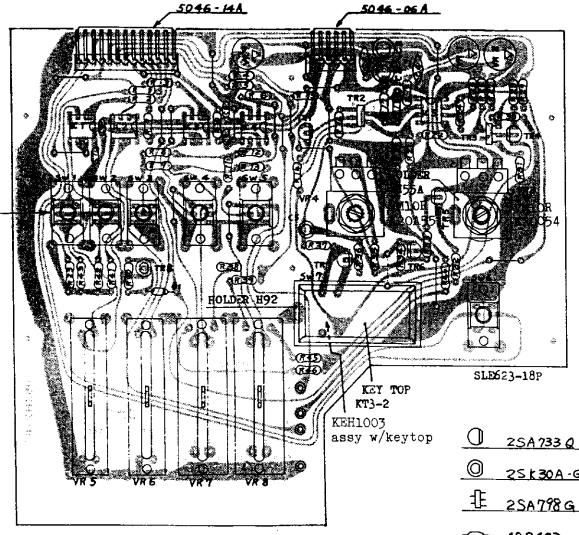
Component side

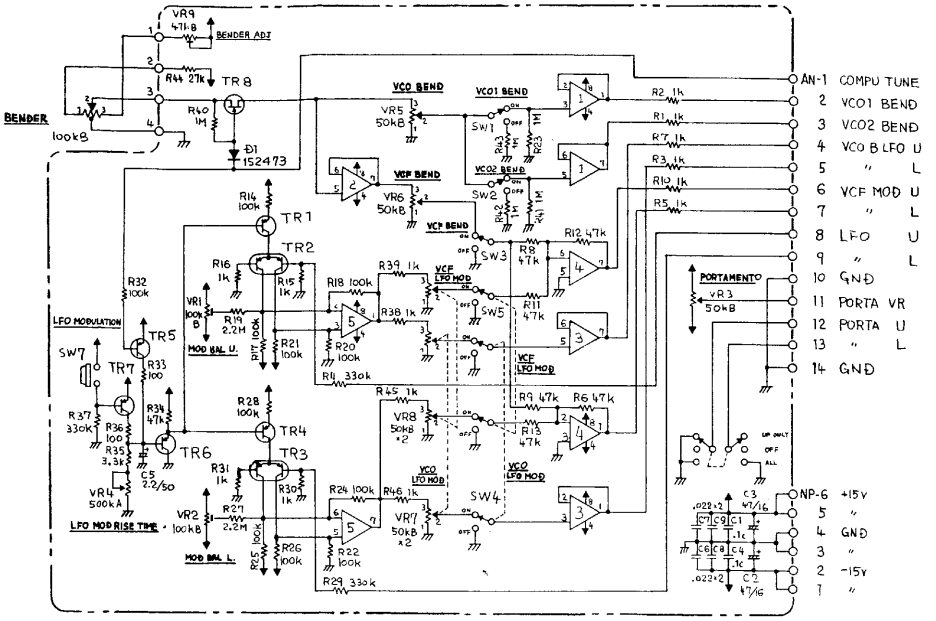


Foil side







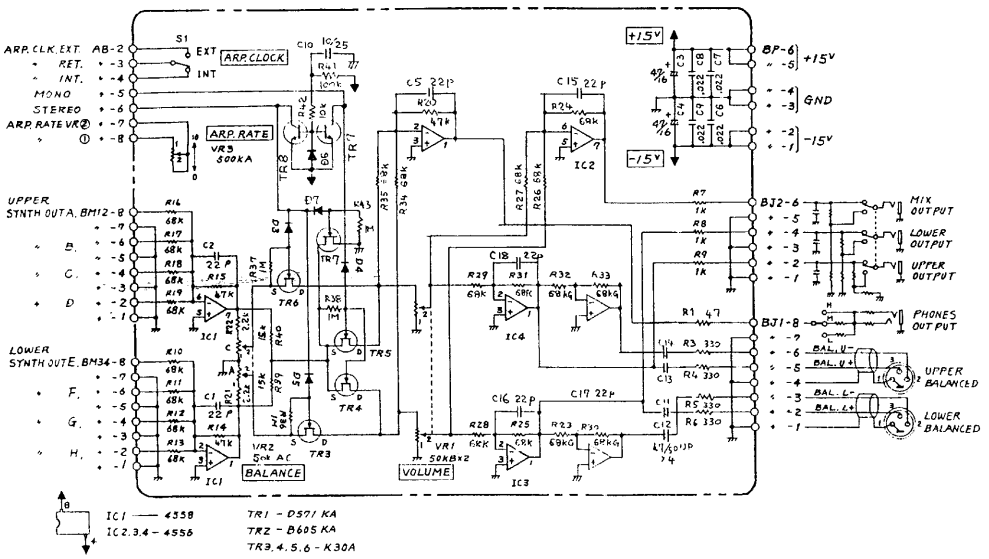


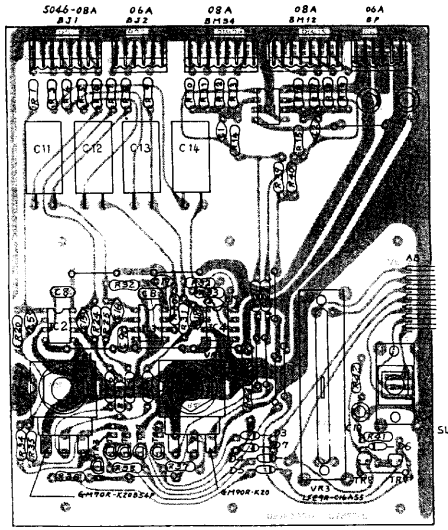
Note: IC 1,3 TL082 IC 2,4,5 4558
TR1,4~7 2SA1015-GR
TR 2,3 2SA798G
TR 8 2SK30A-GR

Highest Ref. Des : IC5, TR8, D1, C5, R43, VR8, SW7

BENDER BOARD
OPH132(149H132)
(pcb 052H278)

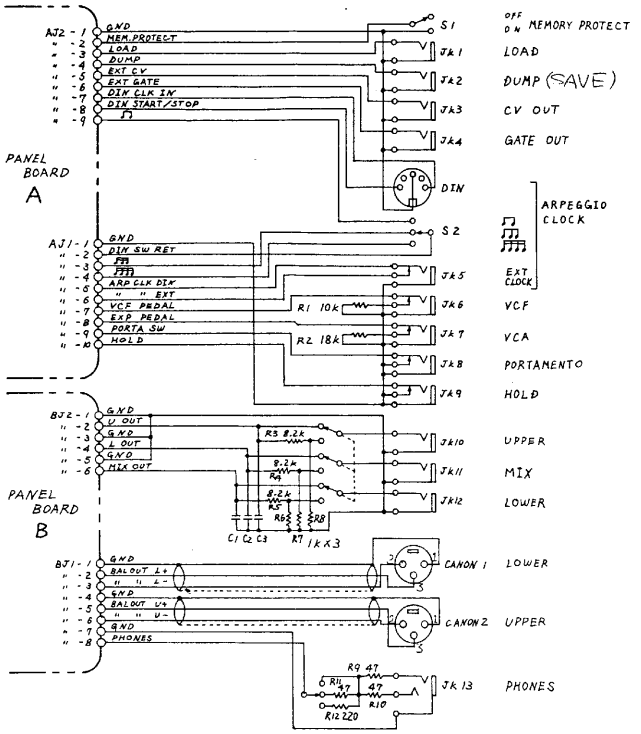
2SA733 Q . P . K
2SK30A-GR . Y
2SA798G
1S2473
SR19R
R25-J



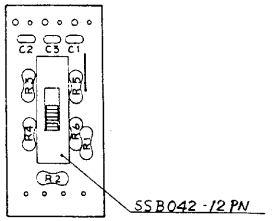


PANEL BOARD B
OPH126(149H126)
(pcb 052H272)

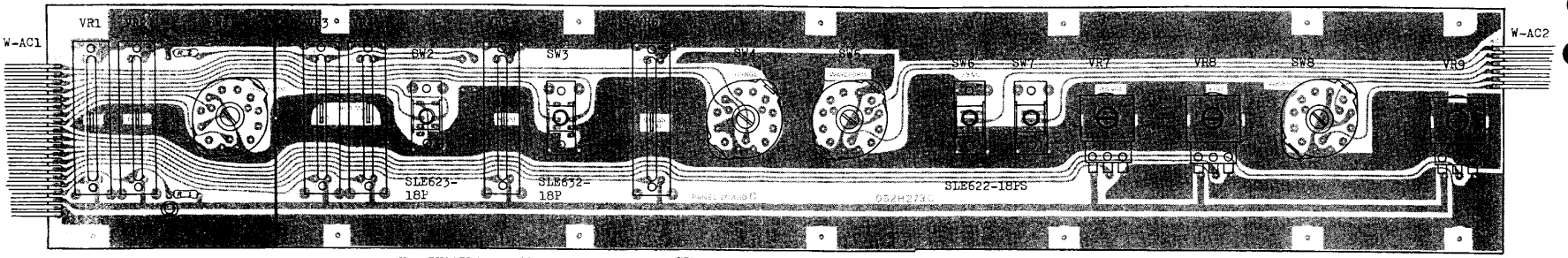
R25J
1S2473
2SK30A
2SC1815 GR



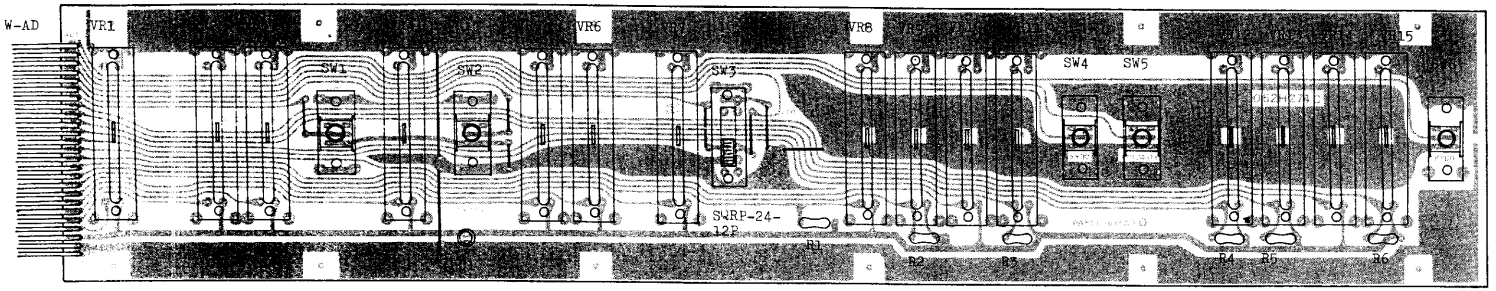
LEVEL SELECT BOARD
OPH139(149H139)
(pcb 052H330)



PANEL BOARD C OPH127(149H127)(pcb 052H273) View from foil side

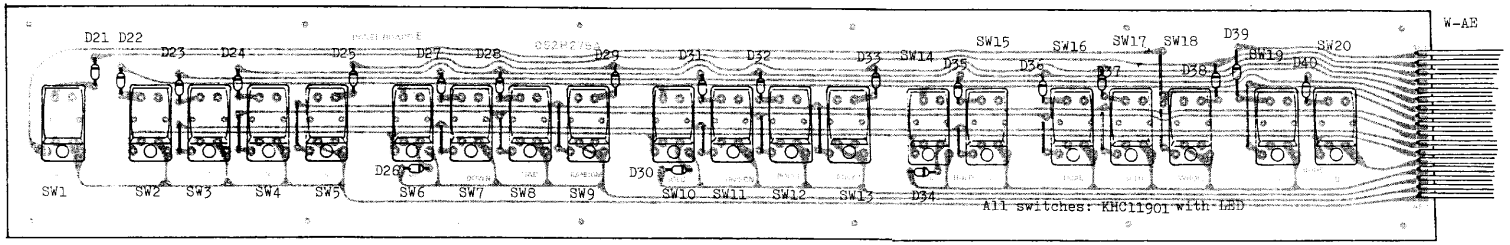


All sliders: LFE9RC16B14 All rotary pots: VM10RK20B14 All rotary switches: SRM1034-K15

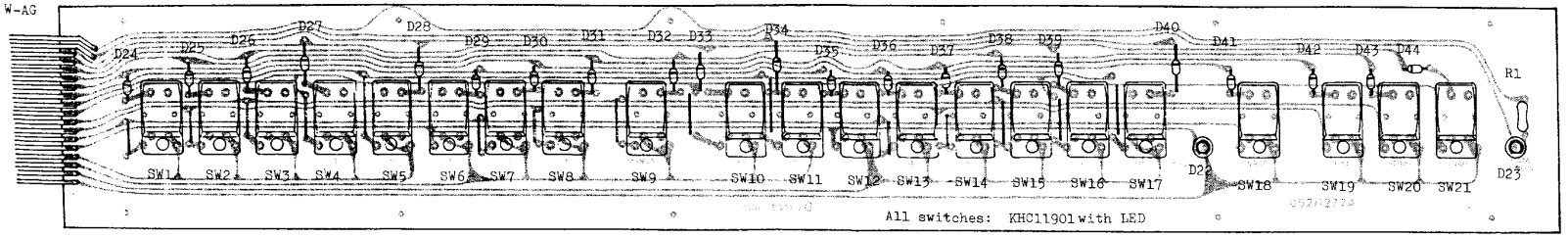


All sliders: LFE9RC16B14 All lever switches: SLE622-18PS

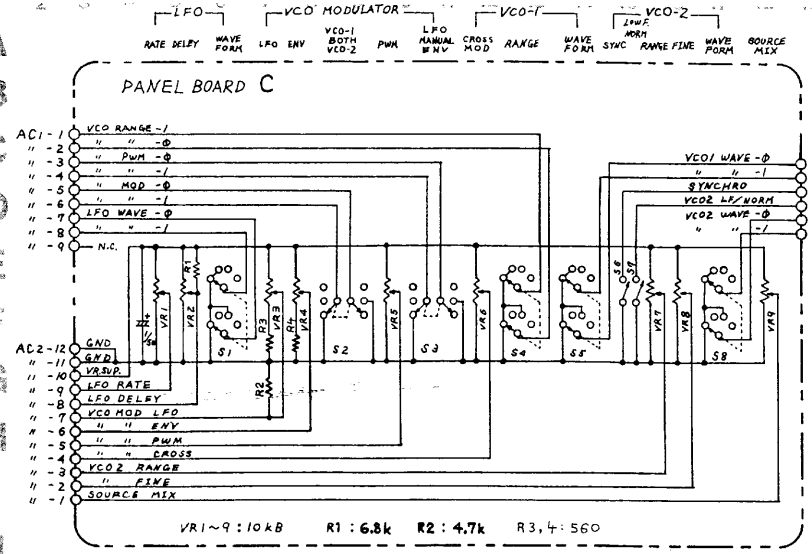
PANEL BOARD D OPH128(149H128) (pcb 052H274) View from foil side

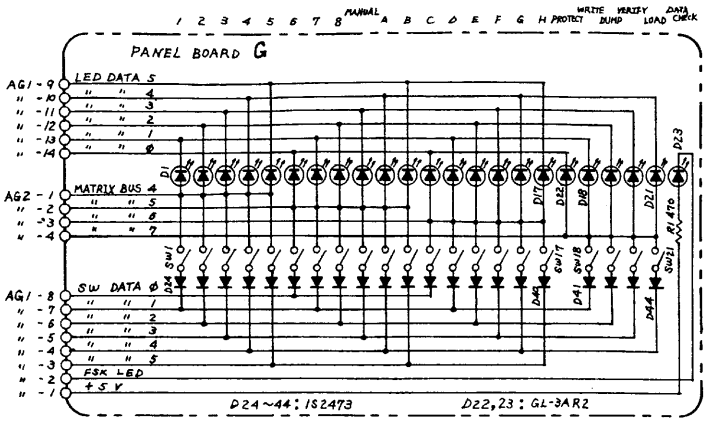


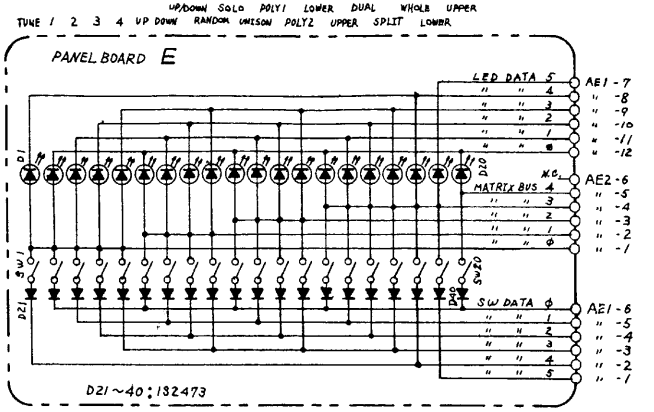
PANEL BOARD E OPH129(149H129) (pcb 052H275) View from foil side

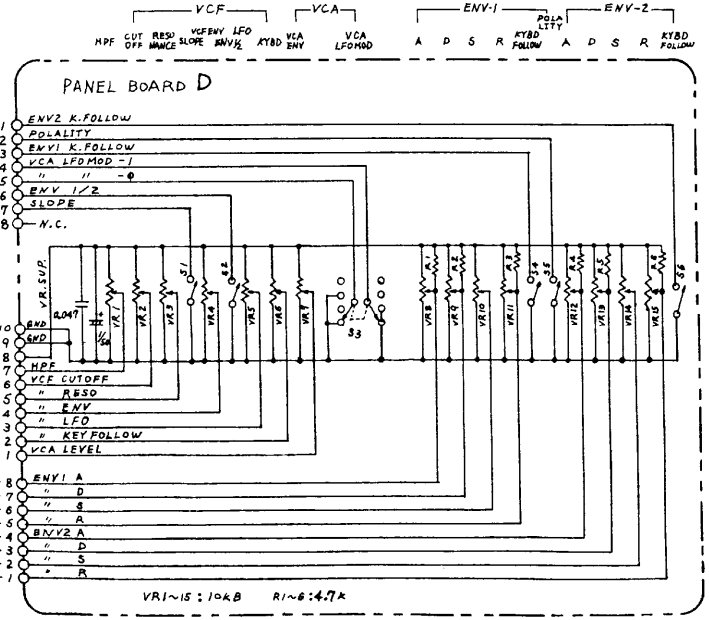


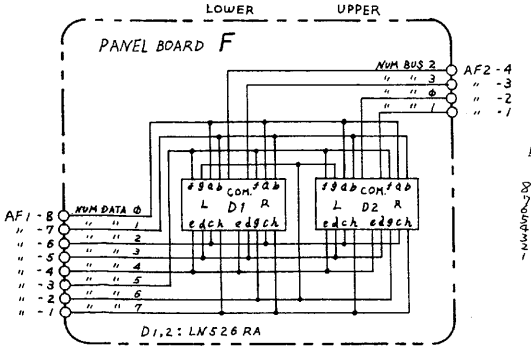
PANEL BOARD G OPH131(149H131) (pcb 052H277) View from foil side



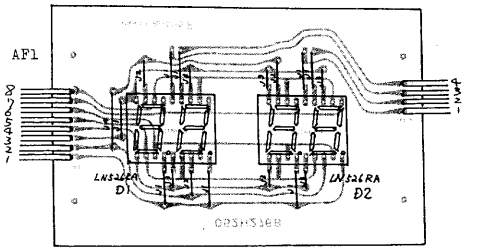




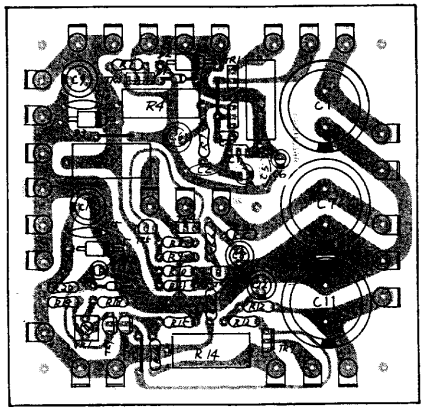




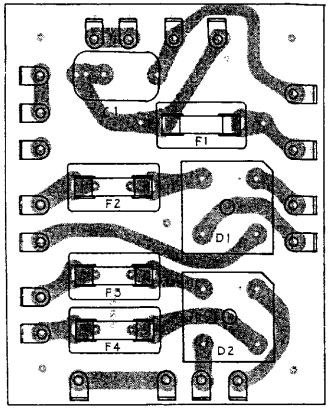
PANEL BOARD F
OPH130 (149H130) (pcb 052H276B)



POWER SUPPLY BOARD A
PSH059(146H059)(pcb 052H279)



POWER SUPPLY BOARD B
PSH061(146H061) 100/117 V
PSH062(146H062) 220/240 V

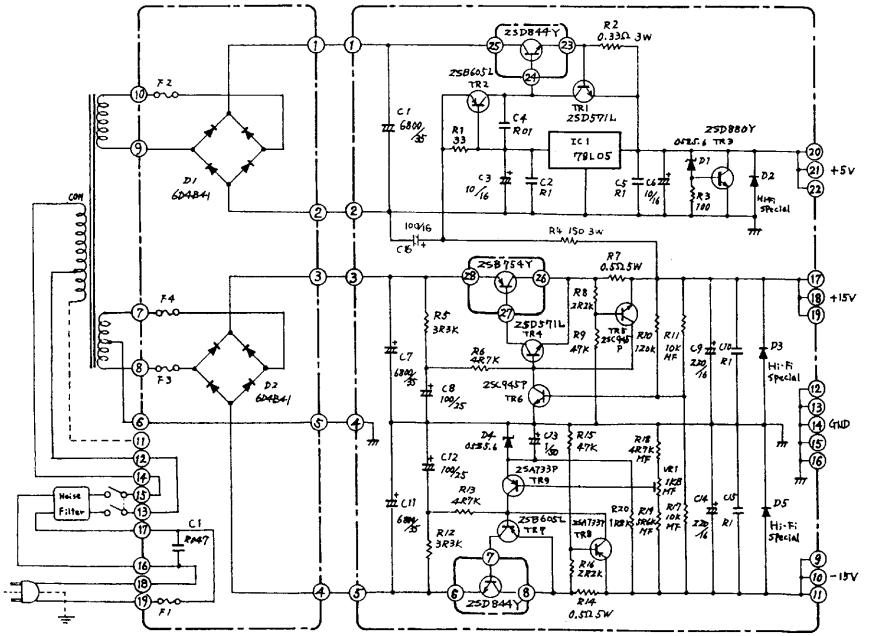


POWER TRANSFORMER SECONDARY RATINGS

±20.5VDC @ 1.3A 4700mfd IN

+8.5VDC @ 1.3A 4700mfd IN

	100/117V	220/240V
F1	MGP0003 (3.0A)	CEE T1.6A
F2		
F3	none	CEE T5.0A
F4		



μPD780 C/D-1
8 BIT MICROPROCESSOR

This is an 8 bit parallel CPU and is compatible with Z-80A and LH0080A.

* Instruction sets: 158
* Instruction cycle: 1.0μs (4.0MHz)
* Internal registers: 17
* address bus 16 bit
* Data bus: 8 bit

PIN FUNCTIONS

ADDRESS BUS Transfers 16 bits to memory address decoders (CPU board- IC21, 22 and 23) for controlling the followings:
on CPU board - ROM, CMOS, RAM, N-ch RAM, TAPE and TUNE reading.
on MOD CON board - RAM, UP, LO and VCO select.

Lower 8 bits are transferred to I/O Address decoders (Interface board - IC1, 2, 3, 4 and 8) for controlling the followings:
IN - Function sws, Digital IN (1, 2 and 3), Key IN, A/D.
OUT - Dot LED, Num LED, Matrix, Analog sel, Key out, D/A Up/Lo, KCV sel, Gate out, EXT synth, Tune.

DATA BUS Used to transfer 8 bit instructions and data between CPU and memories or I/O device.

Ø Square wave, 4 MHz. Derived from X-tal oscillator's 8 MHz, divided-by-two through frequency divider.

$\overline{MREQ}$ (Memory Request) Indicates that Address bus holds a valid memory address for a memory read and memory write.

$\overline{IORQ}$ (I/O Request) Indicates the presence of I/O Device number at pins A0-A7 during I/O write/read cycle.

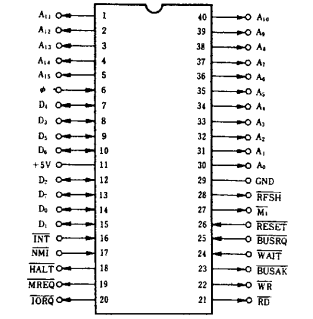
$\overline{RD}$ (Memory read) Indicates that CPU wants to read data from memory or I/O device. The addressed memory or I/O device outputs data onto the CPU data bus at positive transition of RD.

$\overline{WR}$ (Memory write) Indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device which latches the data off of the bus at positive transition of $\overline{WR}$.

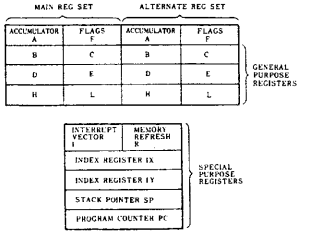
$\overline{INT}$ (Interrupt Request) Whenever $\overline{INT}$ (Ø, frequency divided by Counter-2, IC40) is fed to CPU every 1ms via ‡IC26, it accepts $\overline{INT}$ upon finishing processing job then starts executing Panel LED lighting program, generating INT Acknowledge as an $\overline{IORQ}$ in M1 cycle.

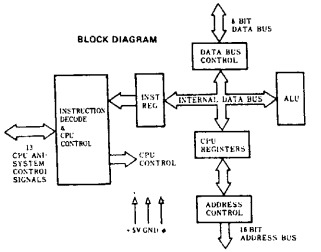
$\overline{WAIT}$ Lengthens read or write cycle until data on the data bus becomes valid during the presence of address signal for timing CPU access time to memory or I/O device.

$\overline{RESET}$ Initializes CPU circuits upon power on for the JP-8 or when DC voltages drop below specified value.



REGISTERS

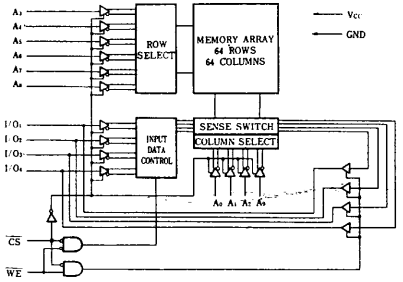




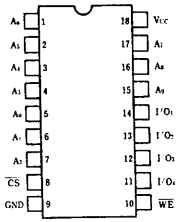
μPD444C

1024 X 4 BIT STATIC RAM CMOS RAM

BLOCK DIAGRAM



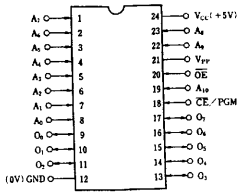
(Top View)



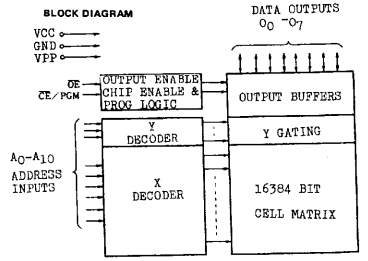
μPD2716D

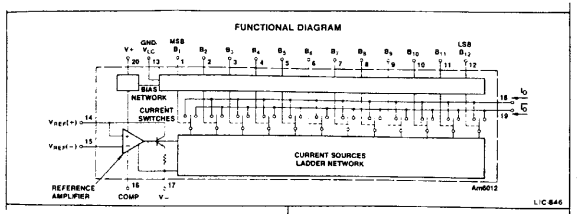
16K (2K × 8) UV ERASABLE PROM

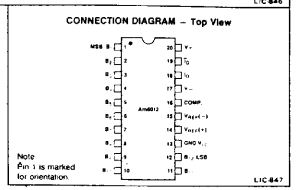
(Top View)



BLOCK DIAGRAM





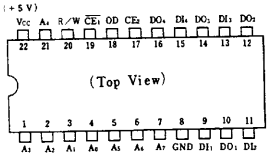


Am6012

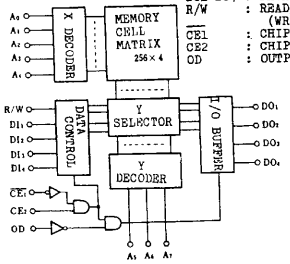
12-Bit High-Speed Multiplying D/A Converter

μPD2101ALC

1024 BIT (256x4) STATIC MOS RAM

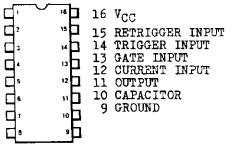


BLOCK DIAGRAM



A0–A7 : ADDRESS
DI1–DI4 : DATA INPUT
DO1–DO4 : DATA OUTPUT
R/W : READ/WRITE (WRITE "0")
CE1 : CHIP ENABLE 1
CE2 : CHIP NEABLE 2
OD : OUTPUT DISABLE

IR3R01

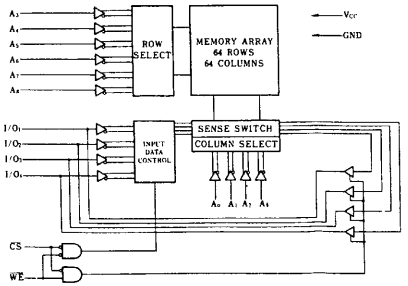


1 MODE INPUT
2 ATTACK TIME INPUT
3 DECAY TIME INPUT
4 RELEASE TIME INPUT
5 SUSTAIN VOLTAGE INPUT
6 COMMON INPUT 0.3V
7 REFERENCE VOLTAGE
8 V_{EE}
16 V_{CC}
15 RETRIGGER INPUT
14 TRIGGER INPUT
13 GATE INPUT
12 CURRENT INPUT
11 OUTPUT
10 CAPACITOR
9 GROUND

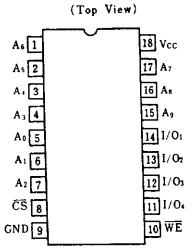
μPD2114LC/D

1024 X 4 BIT STATIC RAM

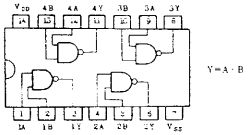
BLOCK DIAGRAM



(Top View)



TC40H000P QUAD 2-INPUT NAND GATE



ADJUSTMENTS

DISASSEMBLY

Follow procedure on page 2. Preparation of a STAY (chain or string) and prop is advisable for a stable top panel rest.

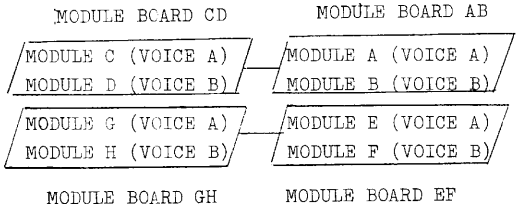
PRECAUTIONS

Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, most circuits are temperature-sensitive.

The adjustments on the JP-8 should not be done more than necessary. Adjustments merely attempted on a particular module (VOICE) might cause sound balance away from entire VOICEs and can, in an extreme case, require the same procedures to be done fifteen times for the remainder.

DESIGNATION – TEST POINT, TRIMMER, PCB –

For PCBs that are identical in circuit configuration, most adjustment steps, test points and trimmers do not refer to a particular PCB or module (VOICE), they may be read as ones on a PCB to be adjusted.



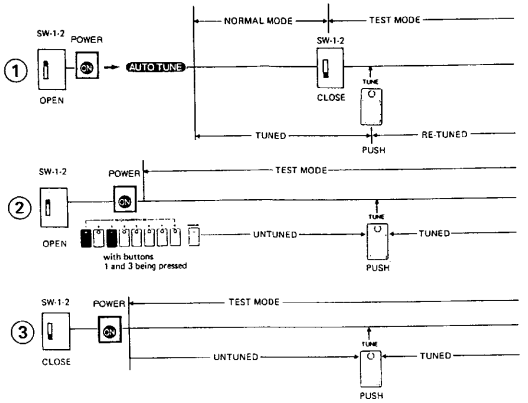
Four module boards, each consisting of two voices, are identical in all aspects, having the same designators with A or B suffix for the same components of two VOICEs, e.g. VR1A (VOICE A) and VR1B (VOICE B). Note that each voice contains two VCOs, VCO-1 and VCO-2.

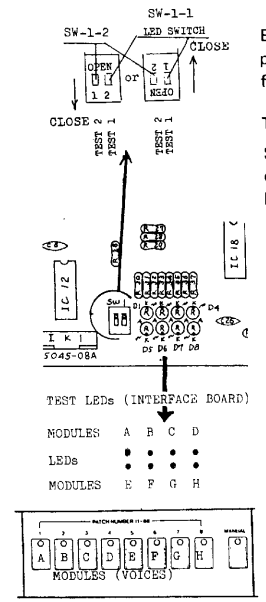
ADJUSTING ORDER

The adjustments proceed from paragraph 1, DC Supply assuming that the JP-8 is completely unadjusted. When adjusting a specific section, begin with lower numbered para. in the relative adjustment section, e.g. first No. 7 BAL, then, No. 8 DEPTH, as directed.

TEST MODES

Adjustments on the JP-8 proceed in TEST MODEs. Although three TEST MODEs are available for the adjustments, TEST MODE (3) is chosen in this manual unless otherwise specified. (For more details refer to TEST MODE in Circuit Description – separate copy.)





Below confines description to the point inevitably necessary for performing the adjustments.

To put the JP-8 into TEST MODE 3

See figure above 3. With power off, throw SW-1-2 on Interface board from OPEN to TEST-1 or -2 (on some early models the switch is oriented opposite, so are labels TEST-1/2 on PCB, left hand one is always SW-1-2 and OPEN position is at label "OPEN" on the SW).

In the TEST MODE 3

The JP-8 has the following functions that are different from those in NORMAL MODE:

All VCOs are uncompu-tuned, i.e. their pitches are left deviated slightly until "TUNE" is pressed.

* Among key assignments, POLY-1 only changes assigning order – tapping single key (same key) will assign modules from A to H one by one, repeating the order. This is convenient in comparing 8 modules sounds (timbre, pitch, etc.) sequentially at a note.
* Computer provides FSK adjustment (para. 26) program and outputs test signal at SAVE (DUMP) jack when VERIFY is pressed.
* Integrated PATCH NUMBER LEDs serve as module (VCO) indicator for visible checking, identifying VCO(s) being directed by key(s) has been depressed or being held down.

SW-1-1, LED switch, in close position, allows LEDs (TEST LED) located right to it to be energized regardless of MODE (NORMAL or TEST) when gate signals are fed to them individually. The LEDs function as assignment indicator just as Patch Number LEDs do. Test LEDs find extended application for learning and checking the assignments varying to MODEs (KEY, PANEL and ASSIGN) in Normal mode.

Patch Number LEDs are lit automatically in sequence immediately after TUNE is touched, representing module A VCO-1 (leftmost LED), A VCO-2 (No.2 LED) and so on; the first cycle for Upper modules' and the second for Lower. Their lighting period is proportional to degree of VCO detune from standard pitches. An LED staying on and won't pass illumination to the next one claims checking of its mated VCO having been far out of computer controllable range.

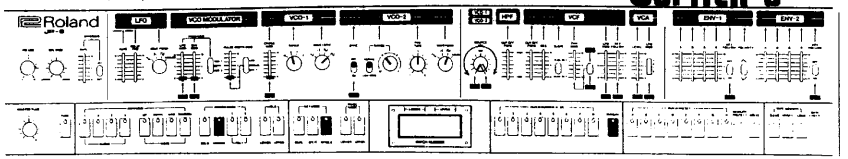
TEST MODEs 2 and 3 are identical to each other in function, but any panel disassembly is required for mode 2 if the purpose is only to check Key Assignment or VCO detune.

FOR SATISFACTORY SERVICE WORK

1. Dump user's preset memory on tape before attempting adjustments and troubleshooting.
2. If TUNE was pressed in previous adjustments, be sure to power off and on the JP-8 before making adjustment which must be done without compu-tune.
3. Plural keying and miskeying will disorder key assignment sequence. Push HOLD or ASSIGN MODE to off and again to on, as appropriate, to restore the order.
   Use monitor amp to detect erroneous key assignmanet that LED does not distinguish.
4. Make a practice of pushing MANUAL after changing PANEL MODEs.
5. Restore SW-1-1 and SW-1-2 to OPEN and load back the data on tape before return the unit to the customer.

12. VCO LEVEL

MODULE (MOD)



See appendices for adjustment locations and glossary.

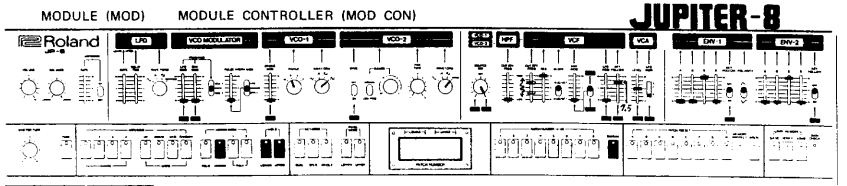
1. Connect scope to MOD TP-4.

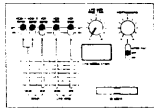
CAUTION On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

2. Press A2 key, adjust VR13 for 10V p-p reading.
3. Rotate SOURCE MIX to VCO-2 and adjust VR15 for 10V p-p.

13. VCF KEY FOLLOWER

MODULE (MOD) MODULE CONTROLLER (MOD CON)





See appendices for adjustment locations and glossary.

This adjustment must be followed by para. 14-17.

CAUTION

On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

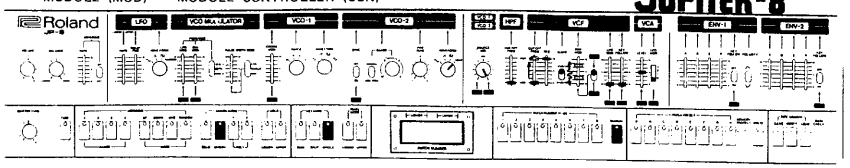
1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166 lead.
3. Turn MOD VR14 fully clockwise. The VCFs resonate.
4. Press C2 key, adjust scope timebase and VCF FREQ to display one complete cycle. (across the graticules, same for the rest para.) MOD VR20 may be used for fine adjustment.
5. Press C4 key, adjust VR16 to display 4 complete cycles.

NOTE:

VR14 and VR20 will be readjusted in later para.

14. VCF WIDTH

MODULE (MOD) MODULE CONTROLLER (CON)



Para. 13-17 must be performed in sequence.

On JP-8's S/N **0600 and subsequent, read figures in parentheses.

1. With scope to MOD TP-6 set timebase to 1ms (2ms)/div.
2. press C2 key, adjust VCF ENV MOD and MOD VR20 to display one complete cycle.
3. Set CO FREQ to 10, scope timebase to 5μs/div (20μs/div). Adjust VR19 to display one complete cycle (5 cycles).

Steps 2 and 3 interact, repeat steps as required.

15. VCF ENV MOD

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change para. 14 setup: VCF ENV MOD to 0, scope timebase to 0.2ms/div.

1. Press C2 key, adjust CO FREQ and MOD VR20 to display exactly one complete cycle.
2. Reset VCF ENV MOD to 10, timebase to 50μs/div. Adjust VR21 to display 16 complete cycles.

16. VCF TUNE

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change setup in para. 15 step 2: ENV MODE to 0; CO FREQ to 5 (S/N **0600 – 4); scope to MOD TP-6 with A-442 reference fed to H IN.

1. Press a key, adjust VR20 for 1:1 Lissajous.

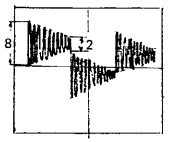
17. RESONANCE LEVEL

MODULE (MOD)

Para. 13-17 must be performed in sequence.

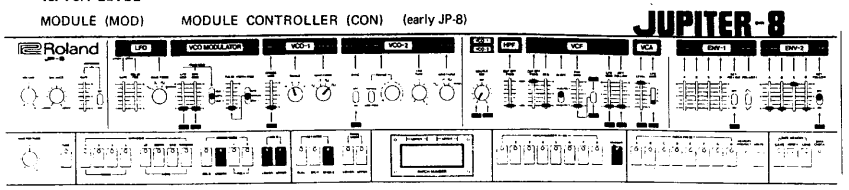
Change setup in para. 16: SOURCE MIX to VCO-1; CO FREQ to 10; Scope to INT TRIG.

1. Press A2 key (S/N **0600 – E3 key), adjust VR14 for the figure:



18. VCA LEVEL

MODULE (MOD) MODULE CONTROLLER (CON) (early JP-8)



See appendices for adjustment locations and glossary.

Although CON VR5 is included in part 1, the trimpot is replaced by 10k resistor on later products.
When adjusting MOD replacement, ignore VR5 trimming, following Part 2.

Connect scope to TP-6 or R166 lead.

PART 1

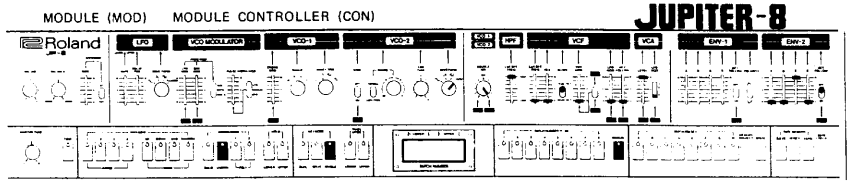
1. Set MOD VR18 wiper to midpoint.
2. Press C2 key and adjust CON VR5 for 3V p-p.
3. Adjust VR18 of the remainder Voices for 3V p-p.

PART 2

1. Press C2 key and adjust VR18 for 3V p-p.

19. VCA BALANCE

MODULE (MOD) MODULE CONTROLLER (CON)

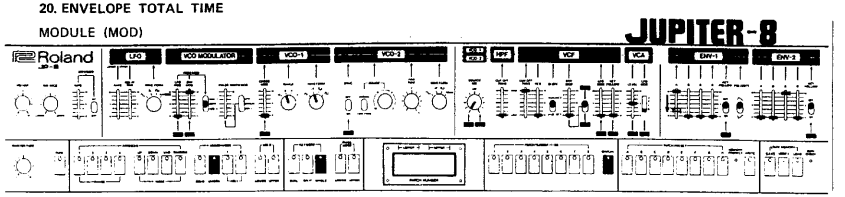


See appendices for adjustment locations and glossary.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166. Switch scope to DC coupling, vertical range to 20mV/div.
3. While tapping a key, adjust VR17 so that DC variations are minimized.

20. ENVELOPE TOTAL TIME

MODULE (MOD)

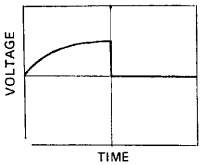


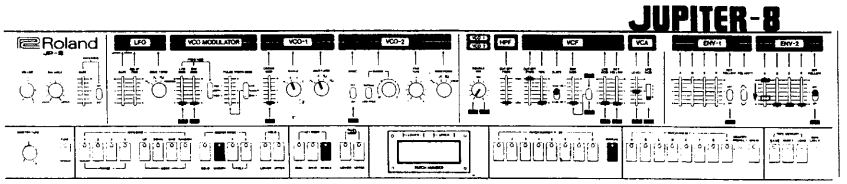
See appendices for adjustment locations and glossary.

This adjustment proceeds on the assumption that all VOICEs' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope V IN connected to TP-8 of well calibrated module.

ENV-1

1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
3. Switch scope timebase to 20ms/div. Trigger scope from TR16 collector of any module.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4-5) and timebase VARI or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.





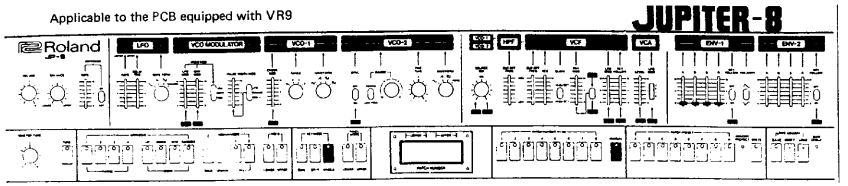
ENV-2

The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.

7-1. ENV-1 S OFFSET

MODULE CONTROLLER (CON)

Applicable to the PCB equipped with VR9



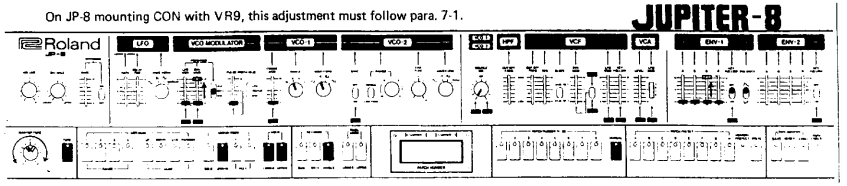
This adjustment must be followed by para. 7. See appendices for adjustment locations and glossary.

1. Connect scope to CON TP-7.
   Set scope V to 20mV/div.
2. Adjust CON VR9 for 0V reading.

7. VCO ENV MOD BAL

MODULE (MOD)

On JP-8 mounting CON with VR9, this adjustment must follow para. 7-1.



See appendices for adjustment locations and glossary.

1. Push TUNE.
2. Connect scope to MOD TP-4 with A-442 reference to H IN.
3. Press A2 key, adjust MASTER TUNE for still Lissajous.
4. Slide MOD ENV up to 10. Without additional keying, adjust MOD VR8 for still Lissajous. (Frequency is same as in step 3.)

8. VCO ENV MOD DEPTH

MODULE (MOD)

This adjustment must follow para. 7. See appendices for adjustment locations and glossary.

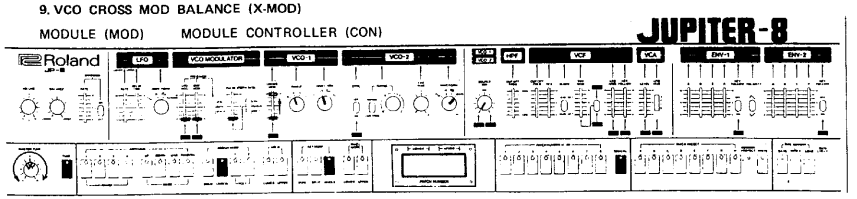
Change from para. 7 setup: ENV-1 S to 10; VCO-1 to 2'; VCO MOD ENV to 0.

The adjustment sets maximum voltage of modulating waveform to the value by which VCO's can be shifted within a 3-octave range.

1. Press A0 key, adjust MASTER TUNE for motionless Lissajous.
2. Set VCO-1 to 16'; VCO MOD ENV to 10. Leaving A0 key open, adjust MOD VR9 for the same waveform as in step 1.

9. VCO CROSS MOD BALANCE (X-MOD)

MODULE (MOD) MODULE CONTROLLER (CON)



This adjustment must be followed by para. 10. See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 with A-442 reference fed to H IN. Place a ground to CON TP-4 or D-20. Push TUNE.
2. Press A2 key, adjust MASTER TUNE for still Lissajous.
3. Leaving A2 key open, set VCO-1 CROSS MOD to 10. Adjust MOD VR10 for the same Lissajous displayed in step 2.

10. VCO CROSS MOD DEPTH (X-MOD LEVEL)

MODULE (MOD) MODULE CONTROLLER (CON)

This adjustment must follow para. 9. See appendices for adjustment locations and glossary.

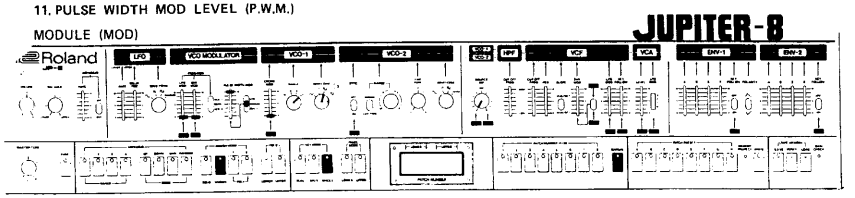
The adjustment sets modulating voltage to the value by which VCO-1 frequency is shifted by 3 octaves when CROSS MOD is set at 5, and VCO-1 RANGE at 2'.

Change from para. 9 setup: VCO-1 CROSS MOD to 5; VCO-2 SYNC to on; VCO-2 RANGE to LOW FREQ.

1. Press A0 key, adjust MASTER TUNE so that Lissajous is 1:1.
2. Switch VCO-2 WAVE to square; VCO-1 to 16'. Adjust MOD VR11 to display Lissajous observed in step 1.

11. PULSE WIDTH MOD LEVEL (P.W.M.)

MODULE (MOD)



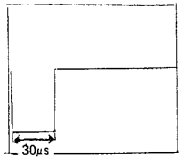
On JP-8's S/N **0600 and subsequent, waveform is up side down.

See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 or R130 lead. Trigger on the negative edge (positive S/N **0600).
2. Press C2 key, adjust MOD VR12 for 30μs space width.

NOTE:

VR12's interact to each other. Check other voices for mark/space ratio. Readjust as necessary.



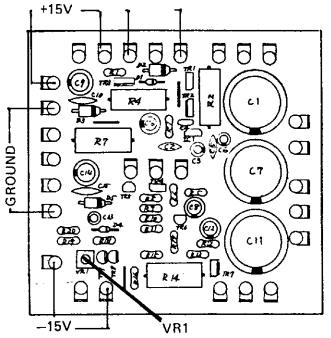
BEFORE STARTING ADJUSTMENTS

ALLOW AT LEAST 30 MINUTES FOR WARUP PERIOD

1. DC SUPPLY

POWER SUPPLY BOARD

1. Connect Digital voltmeter (DVM) to −15V (terminal 9, 10, 11).
2. Adjust VR1 for −15V±10mV reading.
3. +15V should be +15V±500mV.
4. +5V should be 5V±400mV.



2. DC SUPPLY (VCO)

MODULE. MODULE CONTROLLER

See appendices for adjustment locations and glossary.

MODs A, B, C and D

1. Connect DVM to MOD AB IC1 pin 4 (−VDD).
2. Adjust upper CON VR4 for −13V±5mV.
3. IC1 pin 8 should read +13V±200mV.

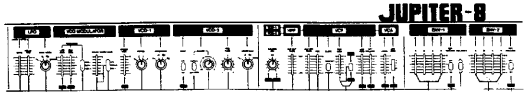
MODs E, F, G and H

1. Disconnect flatcables at upper CON LM1 and HL. Observe the note in CON Layout, appendix.
2. Perform step 1-3 above for lower PCBs.

3. PANEL POTs VOLTAGES

INTERFACE (INT) PANEL BOARD A

See appendices for locations and glossary.



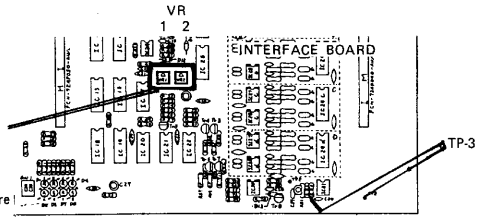
1. Connect DVM to INT TP-3 or R83 (10k) lead facing outside. (See Fig. below right.)
2. Depress MANUAL.
3. Turn all the pots on the panel illustrated fully cw, or to 10. Incomplete settings result in a fluctuating reading or dips on a screen if observed with scope.
4. Set VR1 (Panel board A) for +5V±2mV.

4. DAC

INTERFACE (INT)

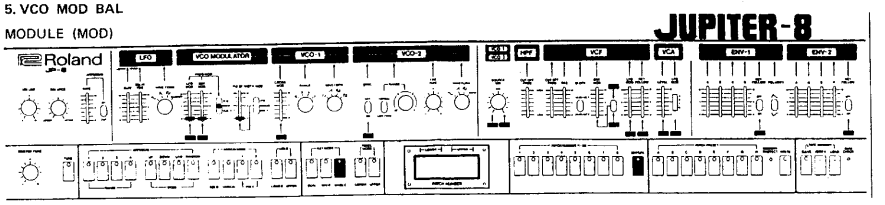
See appendix for glossary.

1. Connect DVM to OUTPUT CV jack.
2. Press KEY MODE WHOLE.
3. Press C0 key, adjust VR2 for 0.000V reading.
4. Press C5 key, adjust VR1 for 5.000V reading.
5. Check C0-C5 keys for scaling, that those voltages are 1V/oct increments ±2mV.



5. VCO MOD BAL

MODULE (MOD)

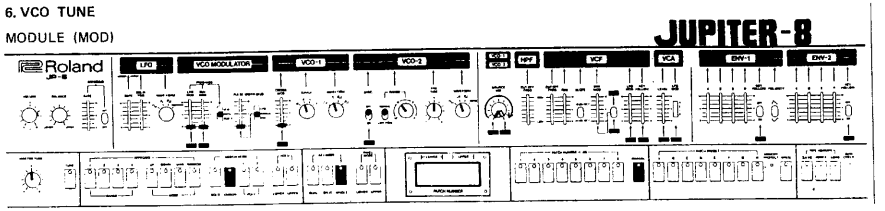


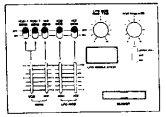
See appendices for adjustment locations and glossary.

1. Connect DVM to MOD TP-3 or R107 lead.
2. Adjust MOD VR7 for 0.000V reading.

6. VCO TUNE

MODULE (MOD)





See appendices for adjustment locations and glossary.

Compu-tuned VCO needs to be re-calibrated only if it or associated components have been replaced. If a VCO is excessively out of tune right after compu-tune, first check MOD BAL, para. 5 and KCV OUT (INT terminals IM-1, IM-3, etc.) for voltage. Seconds, isolate possible causes before attempting VCO adjustments.

As is usual with tuning, several instruments may be used for determining frequency. The calibration proceeds by Lissajous figures with A-442 reference fed to scope's horizontal input.

1. Connect scope to MOD TP-4 or R130 lead.
2. Turn SOURCE MIX fully to VCO-1 or 2 accordingly.

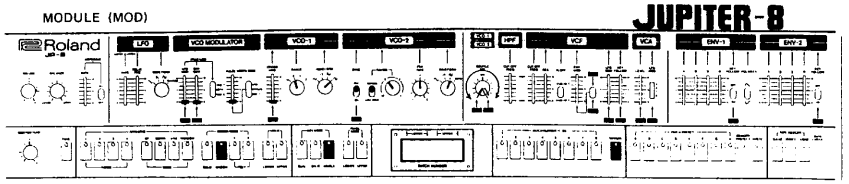
NOTE:

Make sure that the JP-8 is in the test mode without initially compu-tuned upon power on. To ensure this, turn power off and on. Then, push UNISON, etc. See "TEST MODE" on the first page of this section.

3. Press A3 key, adjust trimpot T for 884Hz.
4. Press A1 key, adjust trimpot W for 221Hz.
5. Repeat steps 3-4 until waveforms are stationary on both keys.
6. With RANGE set in 2', press A3 key and adjust L for 3536Hz.
7. These trims interact to each other, repeat steps 3-6 until three notes are on the right frequency.

12. VCO LEVEL

MODULE (MOD)



See appendices for adjustment locations and glossary.

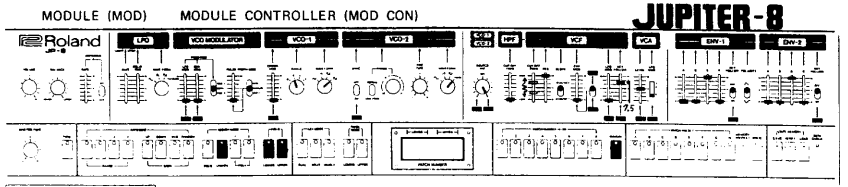
1. Connect scope to MOD TP-4.

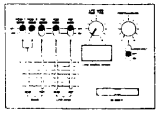
CAUTION On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

2. Press A2 key, adjust VR13 for 10V p-p reading.
3. Rotate SOURCE MIX to VCO-2 and adjust VR15 for 10V p-p.

13. VCF KEY FOLLOWER

MODULE (MOD) MODULE CONTROLLER (MOD CON)





See appendices for adjustment locations and glossary.

This adjustment must be followed by para. 14-17.

CAUTION

On early product, legends for some VR's are incorrect. Refer to PCB layout in appendix.

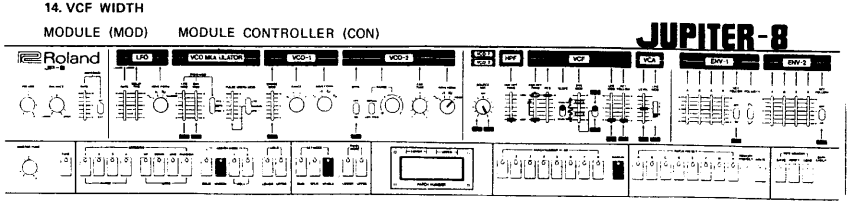
1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166 lead.
3. Turn MOD VR14 fully clockwise. The VCFs resonate.
4. Press C2 key, adjust scope timebase and VCF FREQ to display one complete cycle. (across the graticules, same for the rest para.) MOD VR20 may be used for fine adjustment.
5. Press C4 key, adjust VR16 to display 4 complete cycles.

NOTE:

VR14 and VR20 will be readjusted in later para.

14. VCF WIDTH

MODULE (MOD) MODULE CONTROLLER (CON)



Para. 13-17 must be performed in sequence.

On JP-8's S/N **0600 and subsequent, read figures in parentheses.

1. With scope to MOD TP-6 set timebase to 1ms (2ms)/div.
2. press C2 key, adjust VCF ENV MOD and MOD VR20 to display one complete cycle.
3. Set CO FREQ to 10, scope timebase to 5μs/div (20μs/div). Adjust VR19 to display one complete cycle (5 cycles).

Steps 2 and 3 interact, repeat steps as required.

15. VCF ENV MOD

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change para. 14 setup: VCF ENV MOD to 0, scope timebase to 0.2ms/div.

1. Press C2 key, adjust CO FREQ and MOD VR20 to display exactly one complete cycle.
2. Reset VCF ENV MOD to 10, timebase to 50μs/div. Adjust VR21 to display 16 complete cycles.

16. VCF TUNE

MODULE (MOD) MODULE CONTROLLER (CON)

Para. 13-17 must be performed in sequence.

Change setup in para. 15 step 2: ENV MODE to 0; CO FREQ to 5 (S/N **0600 – 4); scope to MOD TP-6 with A-442 reference fed to H IN.

1. Press a key, adjust VR20 for 1:1 Lissajous.

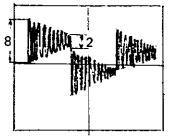
17. RESONANCE LEVEL

MODULE (MOD)

Para. 13-17 must be performed in sequence.

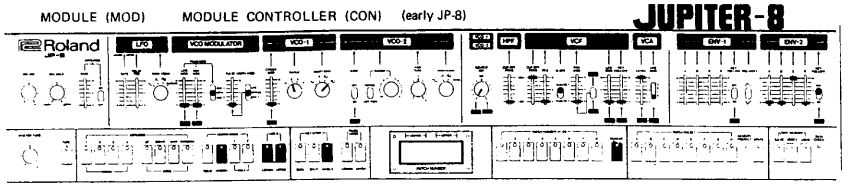
Change setup in para. 16: SOURCE MIX to VCO-1; CO FREQ to 10; Scope to INT TRIG.

1. Press A2 key (S/N **0600 – E3 key), adjust VR14 for the figure:



18. VCA LEVEL

MODULE (MOD) MODULE CONTROLLER (CON) (early JP-8)



See appendices for adjustment locations and glossary.

Although CON VR5 is included in part 1, the trimpot is replaced by 10k resistor on later products.
When adjusting MOD replacement, ignore VR5 trimming, following Part 2.

Connect scope to TP-6 or R166 lead.

PART 1

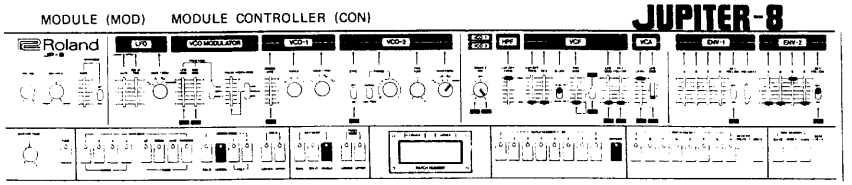
1. Set MOD VR18 wiper to midpoint.
2. Press C2 key and adjust CON VR5 for 3V p-p.
3. Adjust VR18 of the remainder Voices for 3V p-p.

PART 2

1. Press C2 key and adjust VR18 for 3V p-p.

19. VCA BALANCE

MODULE (MOD) MODULE CONTROLLER (CON)

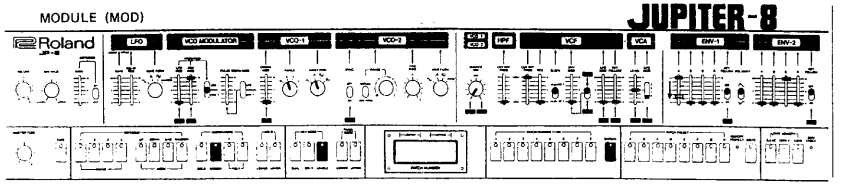


See appendices for adjustment locations and glossary.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R166. Switch scope to DC coupling, vertical range to 20mV/div.
3. While tapping a key, adjust VR17 so that DC variations are minimized.

20. ENVELOPE TOTAL TIME

MODULE (MOD)

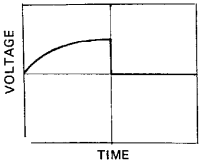


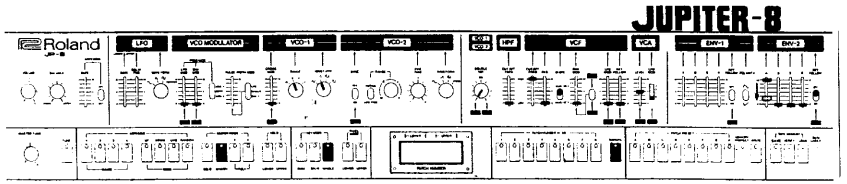
See appendices for adjustment locations and glossary.

This adjustment proceeds on the assumption that all VOICEs' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope V IN connected to TP-8 of well calibrated module.

ENV-1

1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
3. Switch scope timebase to 20ms/div. Trigger scope from TR16 collector of any module.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4-5) and timebase VARI or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.



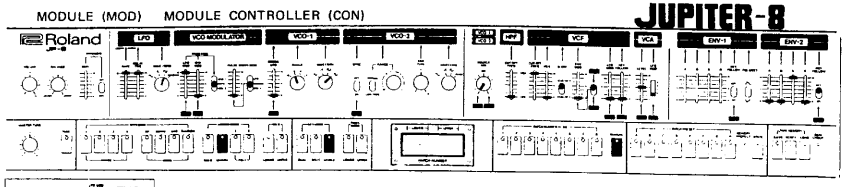


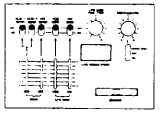
ENV-2

The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.

21. LFO MODULATION

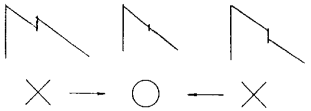
MODULE (MOD) MODULE CONTROLLER (CON)





See appendices for adjustment locations and glossary.

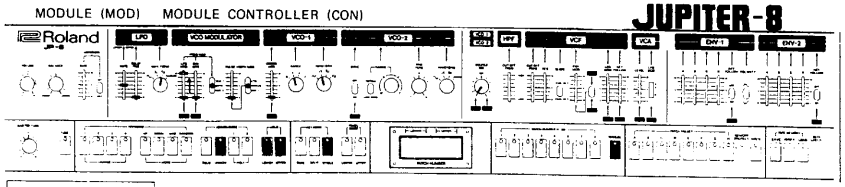
1. Connect scope to CON TP-5 Or R59 lead. Set timebase to 10ms/div.
2. Adjust CON VR3 to display exactly 3 complete cycles on the scope.

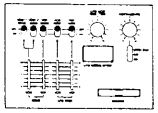


3. Adjust CON VR2 for slope straightness as shown in Fig. right.
4. Shift scope to TP-4 of (Upper – MOD A; Lower – MOD E). Repeatedly holding a key, adjust CON VR8 so that VCO becomes being modulated approx. 4 sec after the key first depressed.

22. VCO LEO MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)



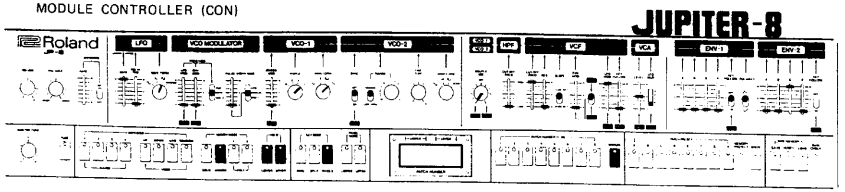


See appendices for adjustment locations and glossary.

1. Connect scope (with A-442 into H IN) to TP-4 of (Upper-MOD A; Lower – MOD E).
2. Press A2 key, adjust MASTER TUNE for 1:1 Lissajous.
3. Set VCO LFO MOD to 10. Lissajous ratio is now changing up and down in sympathy with LFO rate. Adjust CON VR6 so that Lissajous becomes 2:1 at the highest pitch. Note that LFO modulated VCO swing equals 2 oct's.

23. VCF LFO MOD LEVEL

MODULE CONTROLLER (CON)

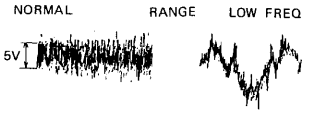


See appendices for adjustment locations and glossary.

1. Connect scope to TP-6 of (Upper – MOD A; Lower – MOD E).
2. Press C2 key (S/N **0600— C4 key), adjust CON VR7 for 50 percentage modulation.

24. NOISE

MODULE CONTROLLER (CON)

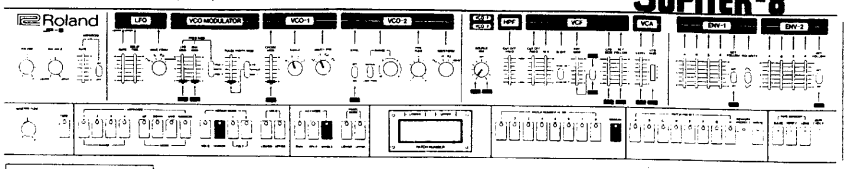


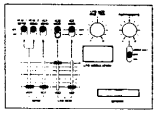
See appendices for adjustment locations and glossary.

1. Switch VCO-2 RANGE to NORMAL. Connect scope to CON TP-4.
2. Adjust CON VR1 so that dense signal peaks are appeox. 5V p-p.
3. Switch RANGE to LOW FREQ, check peaks for clip.

25. BENDER OFFSET

BENDER MODULE (MOD)





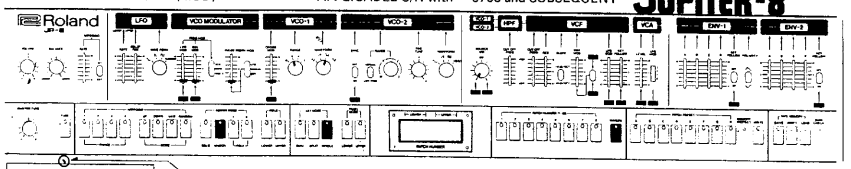
See appendices for adjustment locations and glossary.

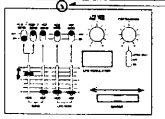
1. Connect scope to TP-4 of (Upper – MOD A; Lower – MOD E) with A-442 reference to H IN.
2. Press A2 key, adjust MASTER TUNE for stationary Lissajous.
3. Set VCO MOD switch to on, adjust VR1 (Upper) or VR2 (Lower) for stationary Lissajous.

NOTE: On JP-8 S/N **0700—, next comes para. 25-1, BENDER LEVEL.

25-1. BENDER LEVEL

BENDER MODULE (MOD) APPLICABLE S/N with **0700 and SUBSEQUENT





VR3 BENDER ADJ

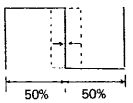
1. Connect scope to TP-4 of any MOD. Press A2 key, adjust timebase and vernier (VARI) to display one complete cycle.
2. Press A3 key. Sway and hold BENDER Lever at extreme left, adjust VCO BEND to display 1 cycle.
3. Press A1 key. Sway and hold BENDER at extreme right, set VR3 for complete 1 cycle.

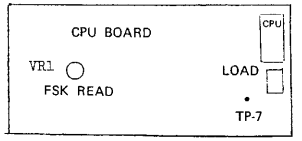
26. FSK

CPU

See appendices for glossary.

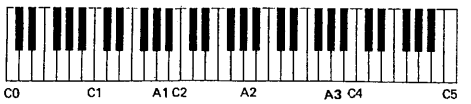
1. Join TAPE MEMORY LOAD and DUMP jacks via cable.
   NOTE: DUMP is renamed as SAVE on later products.
2. Connect scope to CPU TP-7.
3. Push VERIFY. Be sure that the JP-8 is in test mode, this is displayed in PATCH NUMBER window as –|–|–|–|.
4. Set CPU VR1 for 50% duty cycle.
5. Push VERIFY again at the end of adjustment.



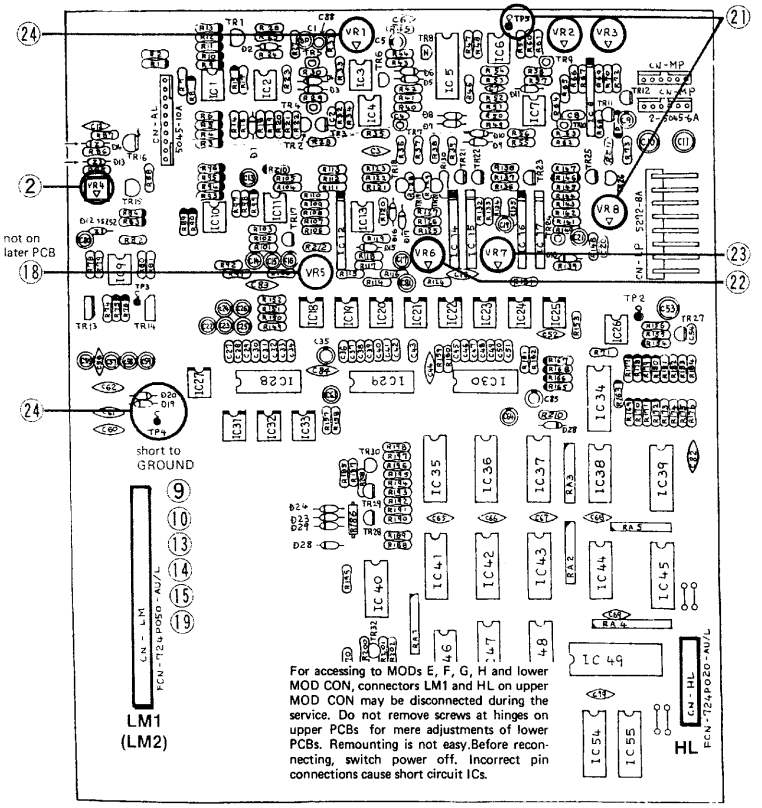


APPENDIX I

CIRCLED NUMBERS AROUND PCB LAYOUT CORRESPOND TO PARAGRAPH NUMBERS



MODULE CONTROLLER BOARD



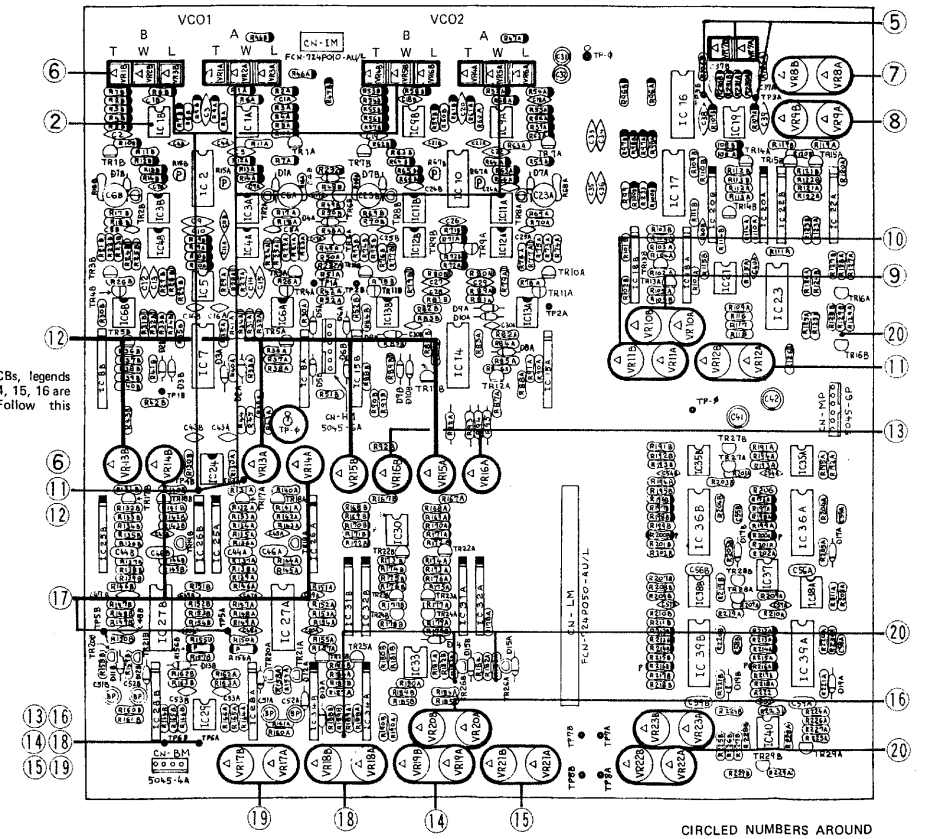
For accessing to MODs E, F, G, H and lower MOD CON, connectors LM1 and HL on upper MOD CON may be disconnected during the service. Do not remove screws at hinges on upper PCBs for mere adjustments of lower PCBs. Remounting is not easy. Before reconnecting, switch power off. Incorrect pin connections cause short circuit ICs.

APPENDIX II

MODULE BOARD

GLOSSARY

DVM	Digital Voltmeter
SCOPE	Oscilloscope
CPU	CPU Board
MOD	Module Board Module (VOICE)
CON	Module Controller Board
INT	Interface Board



On early PCBs, legends for VR13, 14, 15, 16 are incorrect. Follow this arrangement.

CIRCLED NUMBERS AROUND PCB LAYOUT CORRESPOND TO PARAGRAPH NUMBERS

PARTS LIST

CHASSIS

061H117	Chassis H117 (main)
061H118	Chassis H118 (power trans)
061H116	Chassis H116 (jack)
063H040	Plate (side panel) H40 (right)
063H041	Plate (side panel) H41 (left)

PANEL

072H078	Panel H78 (upper)
072H079	Panel H79 (bender)
072H080	Panel H80 (right end block)

HOLDER

064H055B	Holder H55B (pot-pcb)
064H092	Holder H92 (key sw)
064H100	Holder H100
064H101	Holder H101
064H094	Holder H94

KEYBOARD

004H008	SK-361C

KNOB

016-078	Knob NO. 78
016H004	Knob H4
12479703	KT3-2 (key top) (ivory)

SWITCH

13149103	2Wi XII (115V) power sw
13149104	2Wi II (220V) power sw

SLIDE SWITCH

13159118	SSB 022-12RN
13159117	SSB 023-12RN
13159116	SSB 042-12PN
13159503	SQPR-24-12P

DIP SWITCH

13169606	J-S8719-02

LEVER SWITCH

13139136	SLE-622-18P
13139137	SLE-622-18PS
13139135	SLE-623-18P

ROTARY SWITCH

13119301	SRM1034-K15

PUSH SWITCH

13169601	KHC 11901 w/LED

KEY SWITCH UNIT

13129717	KEH 10003 w/key top KT3-2
13129714	KEH10903 switch proper
13129719	Guide pin CHC32801A
2226920800	Cushion rubber CK42602A

BUTTON

016H010	white
016H011	dark blue
016H012	orange
016H013	blue
016H014	green
016H017	yellow
016H018	red

PCB

149H121	CPU board OPH121 (etch mask 052H267)
149H122	INTERFACE board OPH122 (etch mask 052H268)
149H123	MODULE CONTROLLER OPH123 (etch mask 052H269)
149H124	MODULE board OPH124 (etch mask 052H270)
149H125	PANEL board A OPH125 (etch mask 052H271)
149H126	PANEL board B OPH126 (etch mask 052H272)
149H127	PANEL board C OPH127 (etch mask 052H273)
149H128	PANEL board D OPH128 (etch mask 052H274)
149H129	PANEL board E OPH129 (etch mask 052H275)
149H130	PANEL board F OPH130 (etch mask 052H276)
149H131	PANEL board G OPH131 (etch mask 052H277)
149H132	BENDER board OPH132 (etch mask 052H278)
149H139	LEVEL SELECT board OPH139 (etch mask 052H330)
146H059	POWER SUPPLY board A PSH059 (etch mask 052H279)
146H061	POWER SUPPLY board B (100/117) PSH061 (etch mask 052H302)
146H062	POWER SUPPLY board B (220/240) PSH062 (etch mask 052H302)
146H060	POWER SUPPLY board C PSH060 (etch mask 052H303) power Tr

JACK

13449107	S-G7630 (mono)
13449123	S-G7716 (stereo)

FUSE

	GHS 1/4A (CPU board)
12559137	MGP0003 (3.0A) prim. 100/117V
12559521	CEE T1.6A prim. 220/240V
12559518	CEE T5.0A sec. 220/240V

SEMICONDUCTOR

IC (* CMOS)

15159114HO	* TC4052BP	Dual 4-channel multiplexer
15159131	* TC4053BP	Triple 2-channel multiplexer
15159128TO	* TC4050BP	Hex buffer non-inverting type
15159113HO	* TC4051BP	Single 8-channel multiplexer
15159115HO	* TC4066BP	Quadruple bilateral switch
15159132	* TC40175BP	Quadruple D-type flip-flop
15179308	uPD2101ALC	1024 bit static RAM
15179111	uPD780C-1	CPU
15179605NO	uPD2716D	16384 bit erasable PROM
15179305	uPD444C	4096 bit static RAM
15179309	uPD2114C	4096 bit static RAM
15179110NO	uPD8253C	Triple programable interval timers
15149106	CA3046	Transistor arrays
15199109NO	uPC78L05	Three terminal voltage regulator
15189111NO	uPC311C	Comparator
15189105	uPC4558C	OP amp
15189132JO	NJM4556C	OP amp
15189105XO	TL4558C	OP amp
15189116	TL080CP	OP amp
15189160A	TL080CP (selected)	OP amp
15189117	TL081CP	OP amp
15189118OA	TL082CP (selected)	OP amp
15229801	IR3109	VCF
15229807	IR3R01	ADSR
15229802	BA662A or B	VCA
152298020A	BA662A (VF selected) white dot only	
152298020B	BA662A (Offset selected) color dot	
15169301HO	74LS00	Quadruple 2-input NAND gates
15169303HO	74LS02	Quadruple 2-input NOR gates
15169304HO	74LS04	Hex inverters
15169341	74LS14	Hex schmitt-trigger inverters
15169311HO	74LS74	Dual D-type flip-flops
15169313HO	74LS86	Quadruple 2-input exclusive-OR gates
15169318HO	74LS138	3-line to 8-line decoders
15169319HO	74LS139	Dual 2-line to 4-line decoders
15169342	74LS156	Dual 2-line to 4-line decoders
15169321HO	74LS161	Synchronous 4 bit binary counters
15169322HO	74LS174	Hex D-type flop-flops
15169323HO	74LS175	Quadruple D-type flip-flops
15169343	74LS240	Octalbuffers/line drivers with 3-state outputs
15169331XO	74LS244	Octalbuffers/line drivers with 3-state outputs
15169324CO	74LS245	Octal bus transceivers with 3-state outputs
15169325CO	74LS273	Octal D-type flip-flop
15169327HO	74LS367	Hex bus drivers
15169329HO	74LS393	Dual 4-bit binary counters
15169101XO	7400	Quadruple 2-input NAND gates
15169116	7474	Dual D-type flip-flops
15169102XO	7406	Hex inverters with open-collector
15169117	7407	Hex buffers/drivers with open-collector
15219109HO	HA-17555C	Precision timer
15159503	* TC40H000P	Quad 2-input NAND gate
15219105	LM565	Phase locked loop
15219118	Am6012A	12-bit multiplying D/A converter

TRANSISTOR

15119113	2SA1015-GR
15119108	2SA798-G
15119105	2SA733-Q or P, K
15119601	2SB605-L
017-163	2SB605-KA
15119813	2SB754-Y
15129114	2SC1815-GR
15129128	2SC752-Y
15129108	2SC945-P
151291080A	2SC945 (Selected)
15129600	2SD571-L
017-164	2SD571-KA
15129606	2SD844-Y
15129816	2SD880-Y
15139106	2SK117-GR
15139103	2SK30A-GR
15139110	NF510 or 2N4392

DIODE

15019103	1S2473
15019628	05Z-5.6U
15019629	05Z-6.2L
15012626	05Z-11U
15019624	1SZ-52
15029110	GL-3AR1 or TLR124, SLP-135 (LED)
15029103	TLR124 (LED)
15029404	LN526RA (LED)
15019248	6D4841 (6A 200V)
15019247	GP-30G (Hi-Fi special)

POTENTIOMETER

SLIDER

13339414	LFE9R-C16A55 (500KA)
13339415	LFE9R-C16B14 (10KB)
13339413	LFE9R-C16B54 (50KB)
13359302	MFE9R-C16B54 (50KB x 2)

ROTARY

13219811	GM70R-K20AC54P (50KAC)
13219812	GM70R-K20B54P (50KB x 2)
13219225	VM10R-K20B14 (10KB)
13219243	VM10R-K20C54 (50KC)
13219231	VM10R-K20A55 (500KA)
13229131	VM10A-K15B54 (50KB CT)

TRIMMER

	SR19R
13299114	10K
13299116	47K
13299117	100K
	CR44R
329-601	100K
	ET-6P
13299551	1K
13299550	2K
13299549	5K
13299552	100K
	EVTR4SA00B15
13299102	100K

BENDER UNIT

029-022	PB-4

RESISTOR

	CRB25FX (1%)
13769138DO	390 Ohm
13769151DO	1.2K
13769153DO	1.5K
13769158DO	2.4K
13769252DO	2.5K
13769159DO	2.7K
13769160DO	3K
13769161DO	3.3K
13769163DO	3.9K
13769165DO	4.7K
13769167DO	5.6K
13769171DO	8.2K
13769173DO	10K
13769255DO	19K
13769181DO	22K
13769182DO	24K
13769254DO	25K
13769183DO	27K
13769189DO	47K
13769191DO	56K
13769194DO	75K
13769197DO	100K
13769201DO	150K
13769205DO	220K
13769213DO	470K
13769219DO	820K
13769221DO	1M
13769253DO	2.2M
	MO-4S
13839143FO	0.33 3W
13839144FO	150 3W
13839188FO	0.5 5W
	POSISTOR
15229909	560 ERS-B33G561
15229910	1.2K ERS-B33G122
15229911	1K TSP102J
	ARRAY
13910106	10K x 6 RM6-103K
13829821	10K x 8 RM8-103K
13910105	22K x 8 RM8-223K

CAPASITOR

13639942MO	ECEA-1HN010S	1μ 50V bi-polar
13569575FO	CQ09S-1H-10000-J5	1000PF styrol

POWER TRANSFORMER

022H039J	100V
022H039C-A	117V
022H039D	220/240V

COIL

244021500	SN8D500

IC SOCKET

13429511	IC-49-2406#2 (24P)

CONNECTOR

13429608	TCS0250-1-1 (DIN)
13439120	5045-04A
13439122	5045-06A
13439124	5045-08A
13439126	5045-10A
13439155	5045-12A
13439131	5046-04A
13439132	5046-06A
13439133	5046-06A
13439169	5046-08A
13439135	5046-09A
13439136	5046-10A
13439171	5046-12A
13439172	5046-14A
13439173	5274-06A
13439106	5272-08A
13439174	FCN-724P010-AU/0.L 10pin
13439175	FCN-724P020-AU/0.L 20pin
13439176	FCN-724P040-AU/0.L 40pin
13439177	FCN-724P050-AU/0.L 50pin
13439851	HA16R-3P (canon)

FLAT CABLE

053H125	Flat cable H125
053H126	Flat cable H126
053H127	Flat cable H127
053H128	Flat cable H128
053H129	Flat cable H129

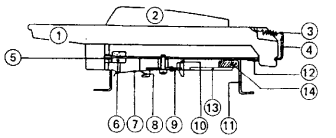
NOISE FILTER

12449219	ZGB1201-11 (100/117V)
12449220	ZMB2201-13 (220/240V)

OTHERS

048H022	Heat sink H22
2215050100	Long nut #1 10mm
2215050300	Long nut #3 18mm
2215051100	Long nut #13 22mm

SEE PP. 40 and 47
For Parts Change
INFORMATION



KEYBOARD PARTS

JP-8 SK-361C (004H008)

NO	PART NO	DESCRIPTION	
1	106H026	Natural key	C F
1	106H027	Natural key	D
1	106H028	Natural key	E B
1	106H029	Natural key	G
1	106H030	Natural key	A
1	106H031	Natural key	C' F'
2	106H032	Sharp key	black
3	070H029	Key spring	H29
4	061H086A	Chassis	H86A
5	068H004	Guide bushing	H4
6	101H141	Level felt	H141
7	071H044	Contact leaf	H44
8	071H051	Busbar 8P	H51
	071H054	Busbar 5P	H54
9	043H007	Switch unit 12P	H7
	043H008	Switch unit 13P	H8
10	104H029	Busbar holder	H29
11	062H024	Chassis bracket	H24
12	098H006	Key stopper	H6
13	052H283-5	Matrix board	H283-5
14	107H059	Cushion	H59

NOTE:
Although Roland has employed 8-10 digit coding, old ones (6 digit and 6 digit with H) are still applied to some parts.

JP-8 SERVICE NOTES

PART 2

The following pages cover the information of Engineering changes and various aspects of JP-8 affected by the changes.

DESIGNE CHANGES THAT CHANGE FEATURE OF THE JP-8

DAC

To have JP-8 more stable in pitch, DAC for KCVs is changed from 12-bit to 14-bit version.

KEY SPLIT POINT

To make JP-8 more convenient for the user to play on, key split point becomes under the control of the player.

DIGITAL COMMUNICATION INTERFACE OC-8 & DCB

To have JP-8 externally controlled through Digital Data Bus connecting either to digitally operating "musical instrument" or to Analog/Digital Interface Unit (e.g. OP-8 that accepts analog CVs in parallel), Digital Communication Interface Board (DCIB) is built in.

OC-8: First, DCIB is named OC-8 and sold as an optional kit.

DCB: Second, another version of DCIB, called DCB is incorporated in the later JP-8 as a standard feature.

The above-mentioned changes and other significant changes not found on the First Edition of JP-8 Service Notes are listed on the table right.

PARTS LIST CHANGE

SEE P. 47

APPENDIX

SEE PP. 48~50

PCB LAYOUTS FOR EARLY 500 JP-8's
MODULE BOARD
MODULE CONTROLLER BOARD

Not published previously, these drawings will help to trace signal paths on old PCBs.

CHANGE INFORMATION

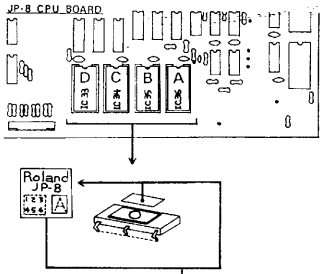
EFFECTIVE SERIAL NUMBER	MAJOR CHANGE	PART INVOLVED	REMARKS
Below 171700	OC-8 (OPTION): TEST PRODUCTION built into JP-8 with programmable KEY SPLIT feature	PROM Program (CUP board): IC34–IC36 Version from 1.0 to 2.1	made only on a few JP-8's see table on the next page
171700 ⋮ 181899	D/A CONVERTER . . . from 12-bit to 14-bit format	INTERFACE BOARD: PCB 052H268 to 052H268 DAC (IC14) from Am6012 to ITS80141 Some ICs and circuits CPU BOARD: PROM programs (IC34–IC36) Version 1.0 to 3.1	14-bit INTERFACE BOARD is compatible with the 12-bit pcb only when PROMs of CPU BOARD are replaced with of version 3.1 or 3.2 see P. 34 for detail
	OC-8 (OPTION): made as a commercially available kit for both 12- and 14-bit versions	ROMs IC34–IC36 of CPU BOARD to be replaced upon installing OC-8	IC34–IC36 must be 3.2 version and are supplied in an OC-8 kit together with PROM IC33 containing communication program
181900	PROMs PROGRAM . . . revised to be compatible with those stored in OC-8 kit PROMs	CPU BOARD: IC34–IC36 from 3.1 to 3.2 version	additional PROM 3.4D (IC33) only is necessary upon installing OC-8 see table on the next page for detail
202100	MODULATION CIRCUITS: To have U and L sounds kept balanced	MODULE CONTROLLER BOARD: PCB from 052H269 to 052H269 some circuits	when U or L board is replaced with new one, the remainder should be slightly modified. see pp. 36–38 for detail
202210	RAM (MODULE CONTROLLER BOARD IC 49): make equivalent RAM usable	CPU BOARD: IC23	short pin 5 of IC23 to ground see p. 38 for modification
242750	LED DISPLAY: adopt brighter LED	PANEL BOARD F: from LN526RA to LN562OA	new and old LEDs are different in color and brightness mix use should be avoided for uniformity
272850	FUNCTION SWITCH: LED to diffusive, brighter type	PANEL BOARD E: PANEL BOARD G: function switch from KHC11901 to KHC11026 (LED from AR3432S to SEL2210R)	
282880	DCB BOARD (similar to OC-8): built into JP-8 as a standard feature	CPU BOARD MODULE CONTROLLER BOARD PANEL BOARD A	drawings related to this change begin at p. 40

HOW TO IDENTIFY PROM VERSION

CPU BOARD

Version is indicated by hand written number or marking on the label as shown below.
Version can be displayed in PATCH NUMBER window (LOWER). Turn the JP-8 on while pressing PATCH NUMBER buttons 1 and 3.

NOTES:
In 0.7 or 1.0 version, displayed number will change quickly from 07 (10) to 13.
In 3.2 (A, B, C) and 3.3D (3.4) arrangement, number 33 (34) will change to 32 if PROM D is removed.



PROM VERSION	PROGRAM
0.7 1.0	12-BIT DAC FIXED KEY SPLIT POINT
2.0 [1]	12-BIT DAC VERIABLE KEY SPLIT POINT
2.1D	DIGITAL COMMUNICATION INTERFACE
3.1	14-BIT DAC VARIABLE KEY SPLIT POINT
3.2 [2]	14-BIT DAC VARIABLE KEY SPLIT POINT
3.3D (3.4D)	DIGITAL COMMUNICATION INTERFACE

1) This is a special version. Replace each with the same one, or replace all four with a set of 3.2 and 3.4D version.
2) Co-operates with 3.3D or 3.4D for Digital Communication Interface.

PROM REPLACEMENT

When replacing PROMs A, B and C with different version, replace them in a set.

Version 3.2 can replace 3.1, 1.0 and 0.7
Version 3.1 can replace 1.0 and 0.7
The reverse does not hold true.

ROM 3.4 can replace 3.3D and vice versa.

NOTES:
PROM D is required only when OC-8 or DCB BOARD is present.
PROM D must be used together with A, B, C of 3.2 version and up.
PROM D contains diagnostic programs.
Refer to P.46 for test procedure.
Difference between 3.3D and 3.4D is that the latter has debugged diagnostic program.

When need arises to modify the JP-8 or to replace parts:
First consult the table below, then refer to the right as necessary.

SERIAL NUMBER	PROM VERSION A B C	PROM VERSION D	DISPLAY	The JP-8 may be or may have	Features of the JP-8	When new feature is required, replace existing part(s) with the one indicated by ●. Addable new feature	PROM A, B, C 3.2	VERSION D 3.3 or 3.4	INTERFACE BOARD w/14-bit DAC	by-product
PROTOTYPE	0.7		07	as produced	DAC ..... 12-bit KEY SPLIT POINT .... Fix OC-8 ..... less	DA 14-bit	●		●	Variable Split point
						SPLIT POINT ..... Valiable	●			
030100	1.0		10	as produced		OC-8 ..... built in	●	●		Variable Split point
171699		JP-8 2.1D	21	OC-8: installed at the factory	DAC ..... 12-bit KEY SPLIT POINT .... Variable OC-8 ..... built in	DA 14-bit	●	●	●	
	(3.2)	3.3D or 3.4D	3334 or	OC-8: built in as option					●	
171700 181899			31	as produced	DA ..... 14-bit KEY SPLIT POINT .... Variable OC-8 ..... less	OC-8 ..... built in	●	●		
181900 282879			32	as produced				●		
171700–272829			34	OC-8: built in as option	DA ..... 14-bit KEY SPLIT POINT .... Variable OC-8 (DCB) ..... built in					
2828800	(3.2)	3.4D		DCB: built in as a standard feature						

INTERFACE BOARD OPH122A

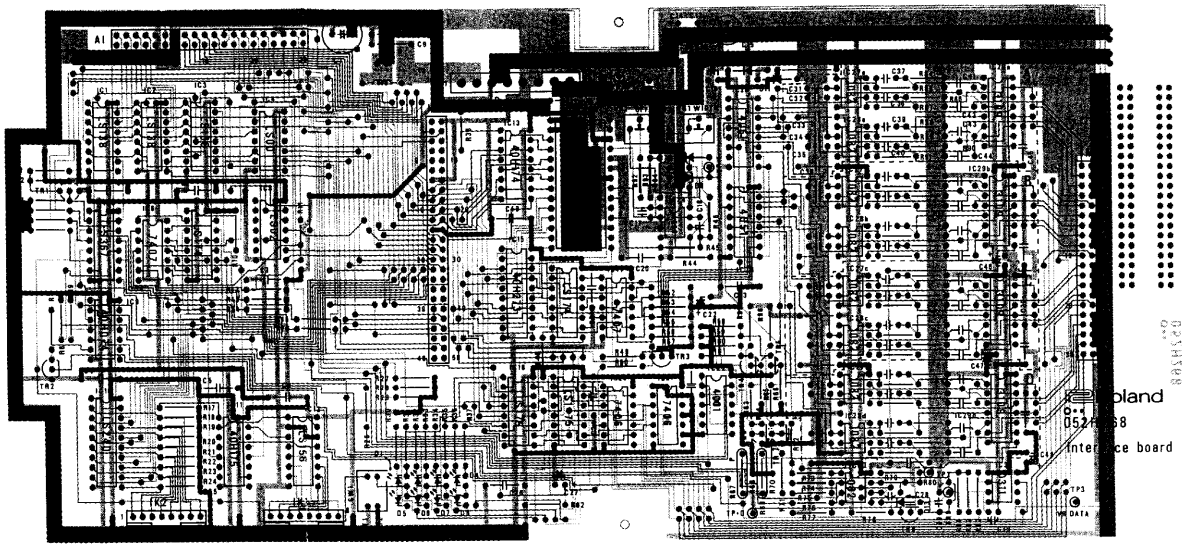
(149H122A) (pcb ○•••052H268)

SN 171700 and higher

MAJOR CHANGES

D/A CONVERTER 14BIT

KEY SPLIT POINT ..... PROGRAMMABLE



This board can replace 12-bit INTERFACE BOARD when PROMs of CPU board are of correct version. See right below.

Besides suffix (A, B, etc.), the PCBs occasionally bear marks "●" and/or "○" above its code number to show the edition.

● stands for 1, and ○ for 5.

Example: ○••• = 8th edition

The D/A Converter IC14 is changed from 12-bit Am6012 to 14-bit ITS80141 with this PCB version. Along with the change the following parts are also changed.

PART	From	To
Latch	LS273 (TTL, IC13)	40H273 (CMOS, IC15)
	LS175 (TTL, IC15)	40H174 (CMOS, IC13)
Multiplexer	LS175 (TTL, IC11)	40H175 (CMOS)
Multiplexer	4051 (IC25, IC26)	HD14051 (Hitachi only)
Flip-flop	74LS74 (IC9)	TC4013 (SN212330-UP TC40H74)
Gate	LS02 (IC22)	TC4001

SUBSTITUTING THIS BOARD FOR 12-BIT DAC BOARD

Prepare PROMs for CPU board:

A, B, C

3.1 version

or

3.2 version (inevitable when OC-8 exists)

for IC34-IC36

D (when OC-8 is built in)

3.3 or 3.4 version for IC33

Replace existing PROMs with these PROMs.

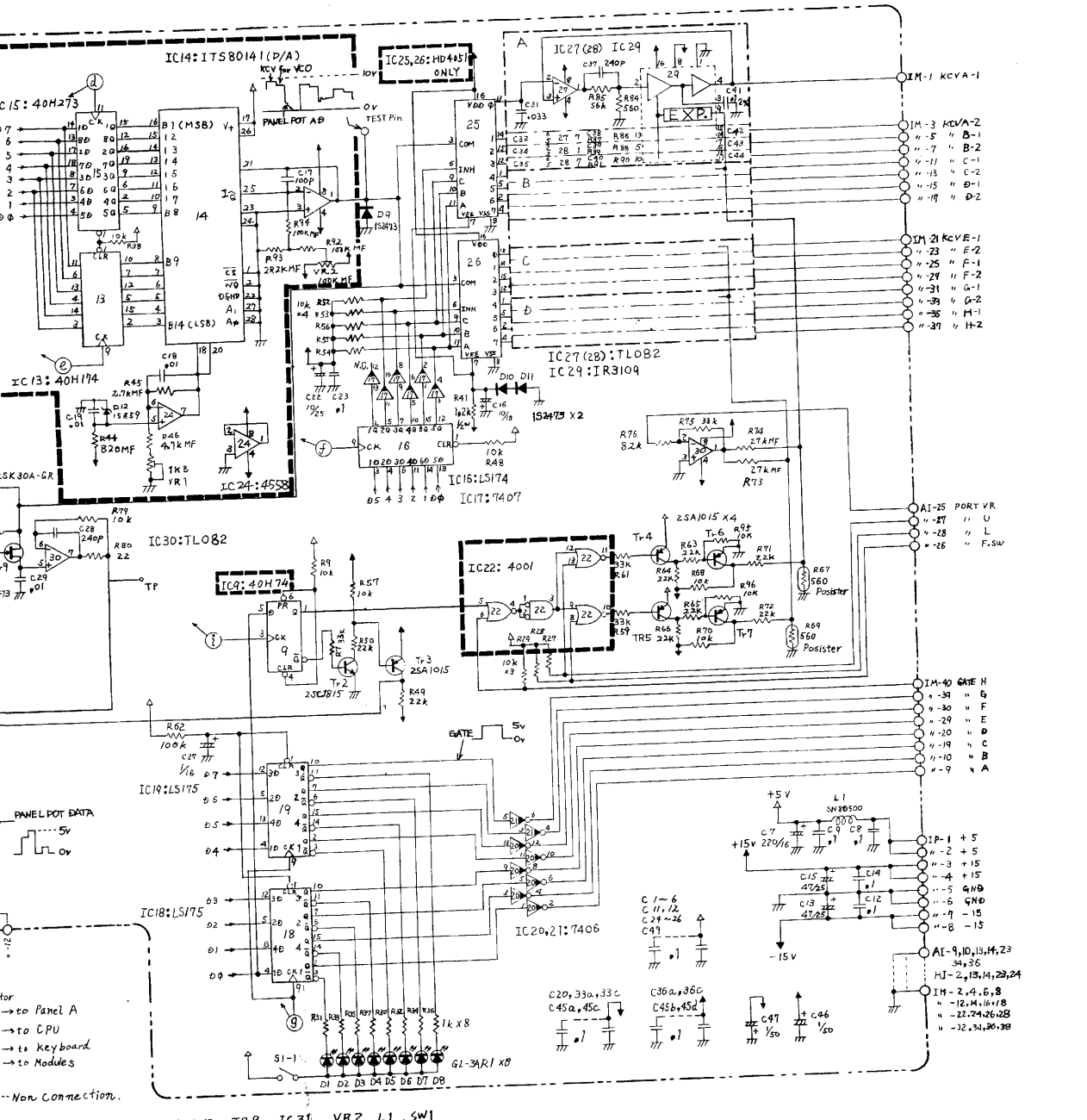
Adjust DAC circuit, referring to "4. DAC" on p.25 of this book.

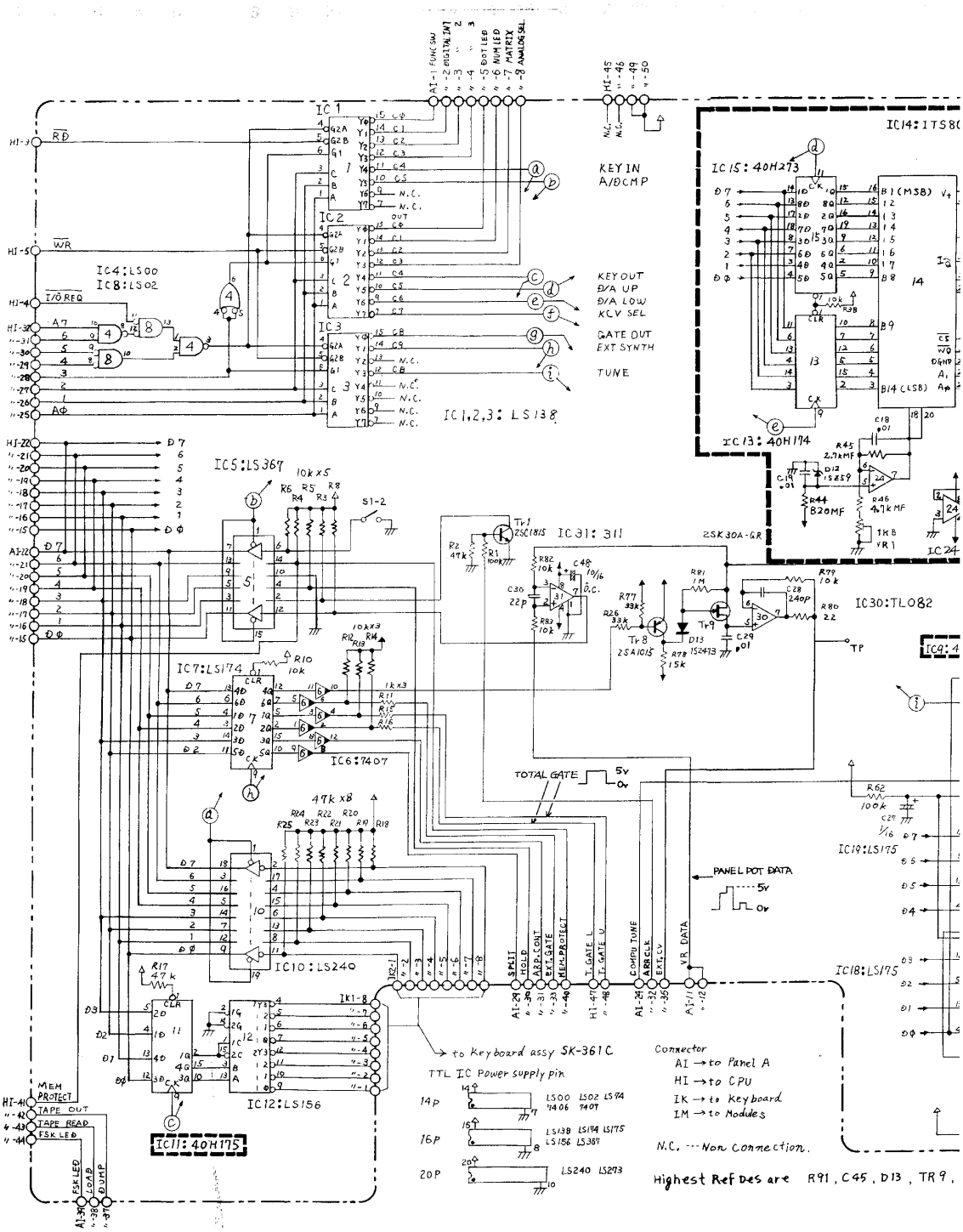
NOTES:

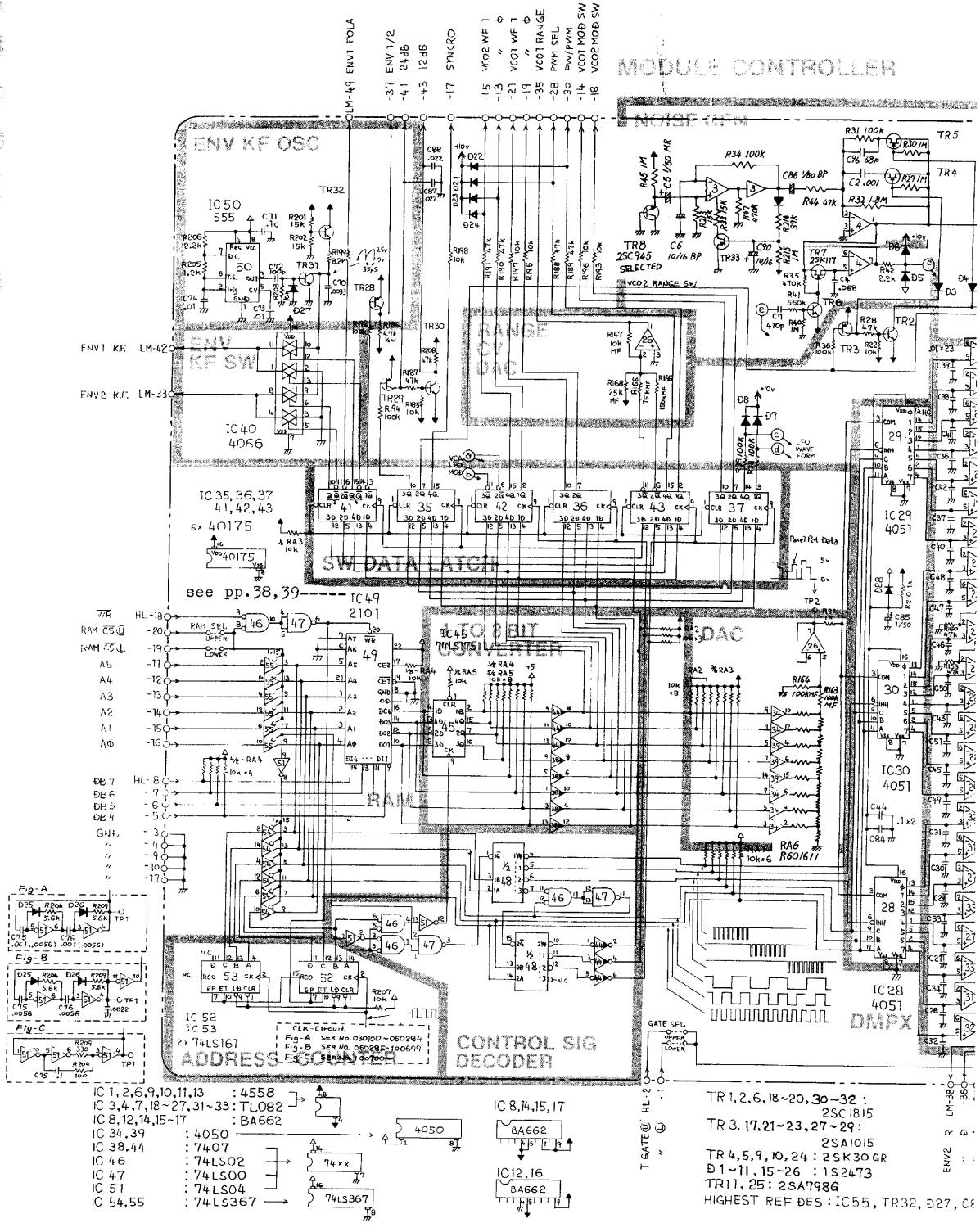
This interchange does not affect adjustment procedures except that the letter "PLL" are displayed in PATCH NUMBER window after —I—I—I during FSK adjustment steps.

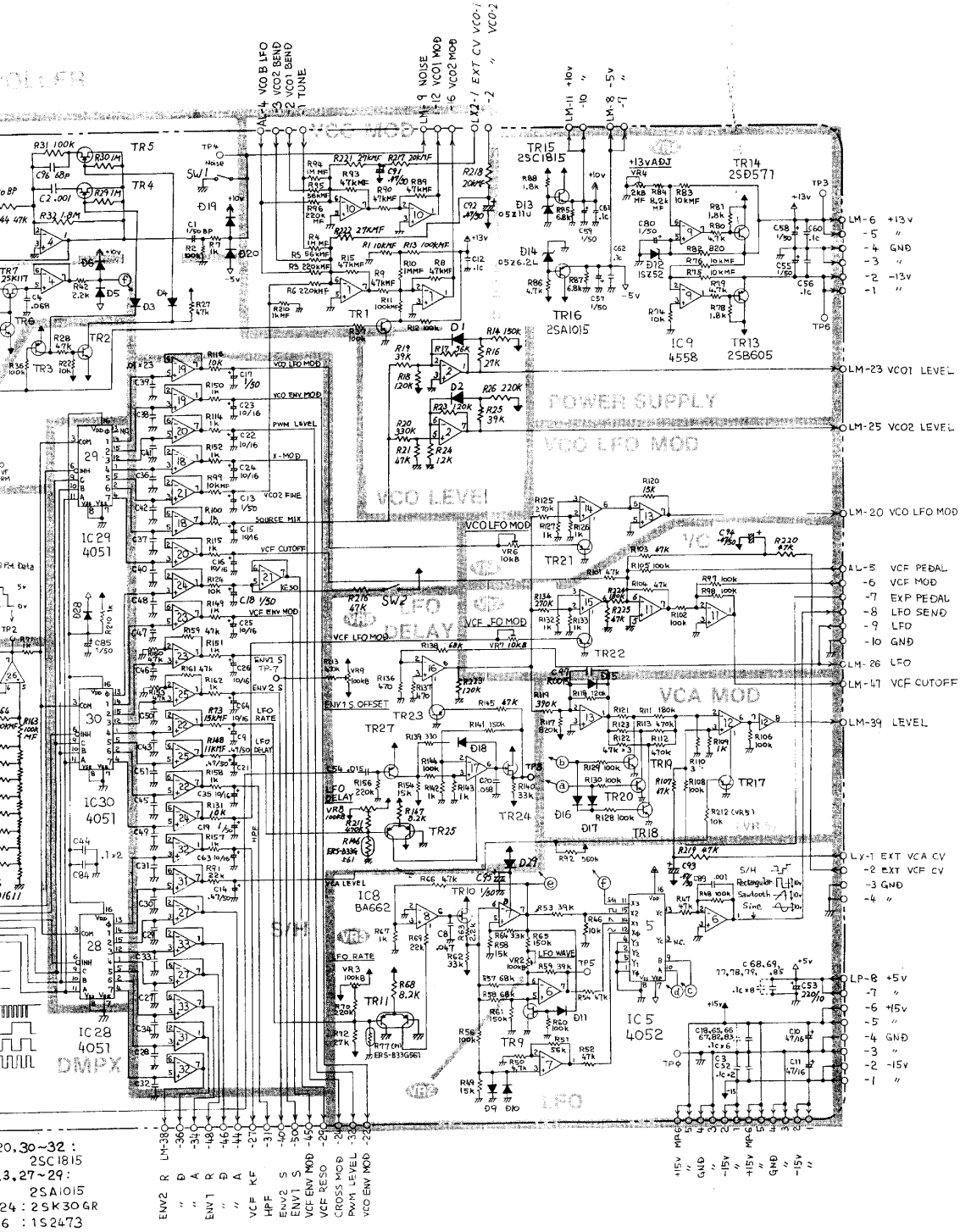
At the end of Computune cycle(s), defective VCO that has not "tuned-in" is indicated in MANUAL and PATCH- NUMBER or PRESET buttons.

See p.39 for indicators and difference in computuning between 12-bit and 14-bit systems.


IC14: ITS80141 (D/A)
IC25,26: HD4851 ONLY
IC27(28) IC29
IC27(28): TL082
IC29: IR3109
IC15: 40H273
IC13: 40H174
IC24: 4558
IC16: LS174
IC17: 7407
IC30: TL082
IC9: 40H74
IC22: 4001
IC19: LS175
IC18: LS175
IC20,21: 7406
PANEL POT DATA
PANEL POT AD
TEST Pin
KCV for VCO
EXP.
Tr4
Tr5
Tr6
Tr7
Tr2
Tr3
2SA1015 X4
2SC1815
152473 X2
GATE
IM-1 KCV A-1
IM-3 KCV A-2
IM-21 KCV E-1
IM-40 GATE H
AI-25 PORT VR
AI-9,10,13,14,23 34,36
IM-2,4,6,8
IP-1 +5
IP-2 +5
IP-3 +15
IP-4 +15
IP-5 GND
IP-6 GND
IP-7 -15
IP-8 -15
1k x8
G1-3AR1 X8
→to Panel A
→to CPU
→to keyboard
→to Modules
--Non Connection.
st Ref Des are R91, C45, D13, TR9, IC31, VR2, L1, SW1


IC1,2,3: LS138
IC4: LS00
IC8: LS02
IC5: LS367
IC7: LS174
IC6: 7407
IC10: LS240
IC12: LS156
IC11: 40H175
IC15: 40H273
IC13: 40H174
IC14: I7S8(
IC31: 311
IC30: TL082
IC19: LS175
IC18: LS175
KEY IN A/D CMP
KEY OUT D/A UP D/A LOW KCV SEL
GATE OUT EXT SYNTH
TUNE
TOTAL GATE
PANEL POT DATA
to Keyboard assy SK-361C
TTL IC Power supply pin
Connector
AI → to Panel A
HI → to CPU
IK → to Keyboard
IM → to Modules
N.C. ··· Non Connection.
Highest Ref Des are R91, C45, D13, TR9,


MODULE CONTROLLER
ENV KF OSC
ENV KF SW
RANGE CV DAC
SW DATA LATCH
10 BIT D/A CONVERTER
CONTROL SIG DECODER
ADDRESS COUNTER
RAM
DMPX
IC50 555
IC40 4066
IC35,36,37 41,42,43 6× 40175
IC45 74LS541
IC49 2101
IC52 IC53 2× 74LS161
IC28 4051
IC29 4051
IC30 4051
TR32
TR31
TR28
TR30
TR29
TR8 2SC945 SELECTED
TR33
TR5
TR4
TR7 2SK117
TR6
TR3
TR2
ENV1 KF LM-42
ENV2 KF LM-33
ENV1 POLA LM-49
-37 ENV 1/2
-41 24dB
-43 12dB
-17 SYNCRO
-15 VCO2 WF 1
-13 〃 Φ
-21 VCO1 WF 1
-19 〃 Φ
-35 VCO1 RANGE
-28 PWM SEL
-30 PW/PWM
-14 VCO1 MOD SW
-18 VCO2 MOD SW
VCO2 RANGE SW
LFO WAVE FORM
Panel Pot Data
see pp.38,39
GATE SEL
Fig-A
Fig-B
Fig-C
IC 1,2,6,9,10,11,13 : 4558
IC 3,4,7,18~27,31~33 : TL082
IC 8,12,14,15~17 : BA662
IC 34,39 : 4050
IC 38,44 : 7407
IC 46 : 74LS02
IC 47 : 74LS00
IC 51 : 74LS04
IC 54,55 : 74LS367
IC 8,14,15,17 8A662
IC12,16 8A662
TR 1,2,6,18~20,30~32 : 2SC1815
TR 3,17,21~23,27~29 : 2SA1015
TR 4,5,9,10,24 : 2SK30 GR
D1~11,15~26 : 1S2473
TR11,25 : 2SA798G
HIGHEST REF DES : IC55, TR32, D27, C8



20,30~32 : 2SC1815
3,27~29 : 2SA1015
24 : 2SK30GR
6 : 1S2473
SA798G
DES : IC55, TR32, D27, C88, R212, RA5, VR9

GUIDES ON REPLACEMENT

MODULE CONTROLLER BOARD

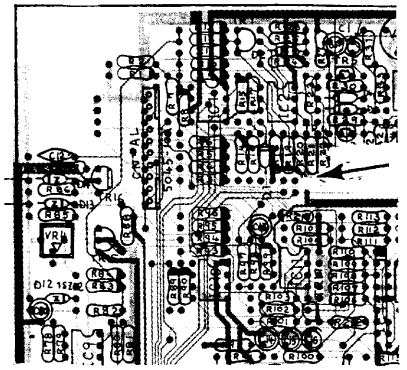
(For early 500 units, see p.48)

When replacing OPH123 with OPH123A, be sure to proceed the following.

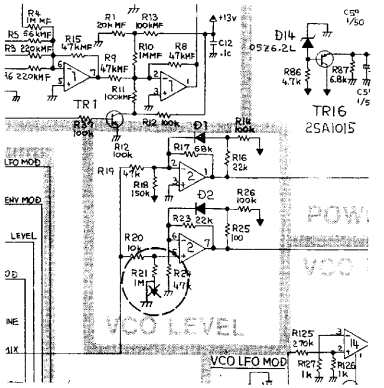
Check IC49 on the both PCBs (being replaced and replacement) for name. If 2101 is on the existing PCB and 5101 on the replacement, take the modification illustrated below.

When replacing Upper board or Lower only:

Adjust VR1 (NOISE LEVEL) of unchanged MOD CON board to match the noise level of new board which omits the adjustment. Reconnect R21 of unchanged MOD CON, referring to drawing to the right. This will eliminate possible loudness differences between U and L voices.



Disconnect R21 lead at negative end and solder it to the nearist ground foil.



IC49 OF MOD CON BOARD (MODIFICATION ON CPU BOARD)

(RAMs 2101 and 5101)

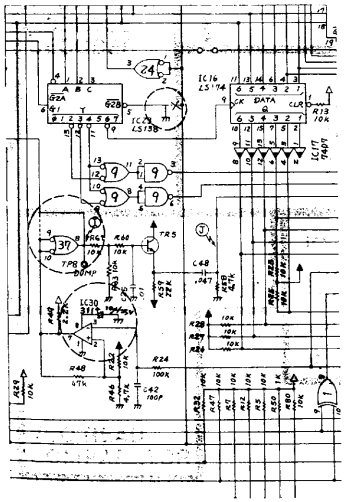
Factory modification SN 202210-UP

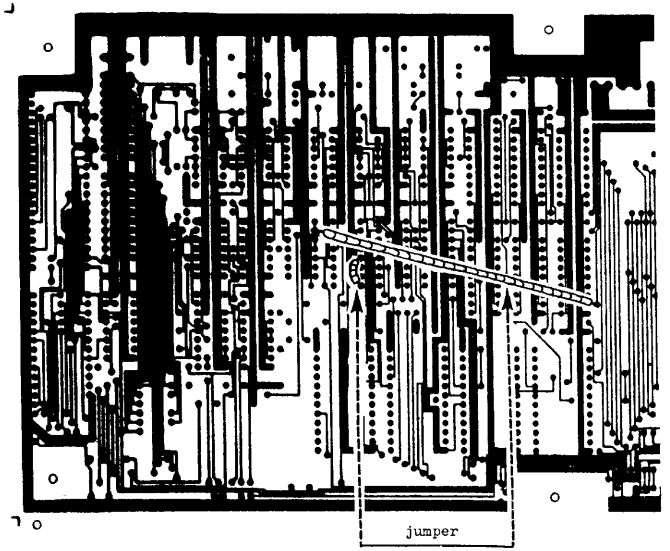
Below, two minor modifications (independent of RAM change) are also indicated:

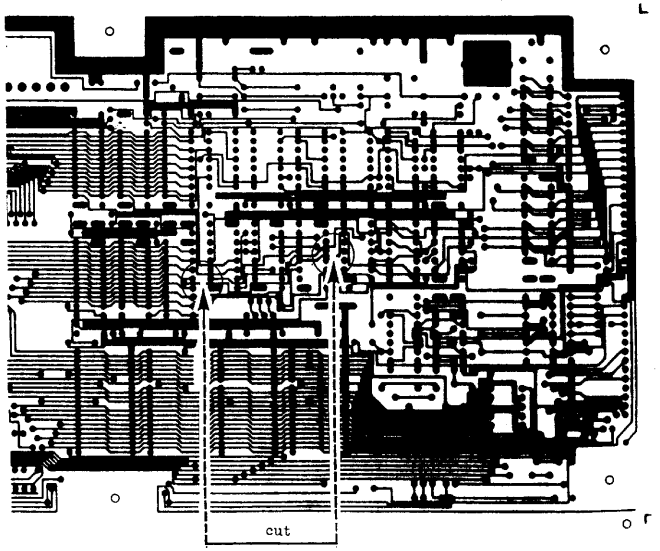
Reconnection of IC37 and addition of 10UF at IC30 pin 8

Insertion of 5101 into a place previously occupied by 2101 requires pin 5 of IC23 on CPU board to be grounded. This reconnection as illustrated is to protect the data on panel control from garbled — while a control is being reset, some of other controls are also detected as moving; in extreme case no voice would sound. This is due to the fact that two RAMs differently respond to the same timing signal.

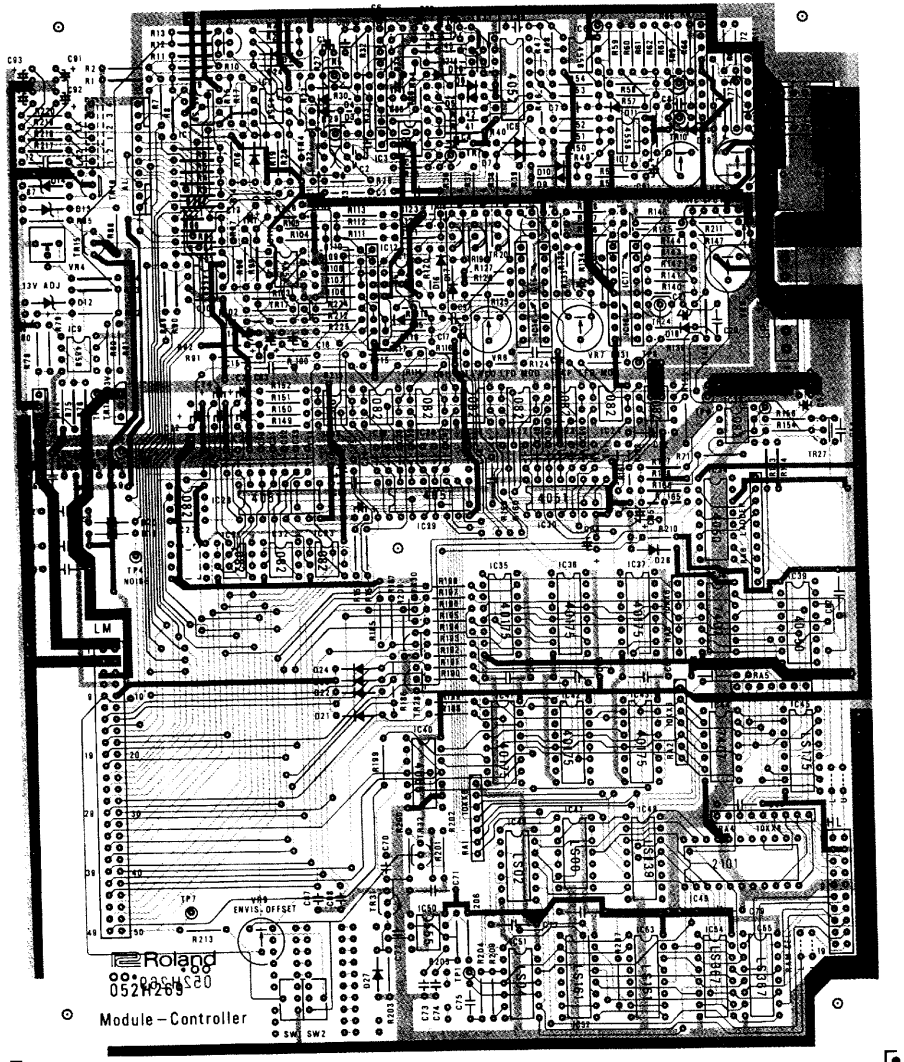
This modification has no adverse effect on 2101.







MODULE CONTROLLER BOARD SN 202100 and UP
OPH123A (149H123A) (pcb 052H269)



IMPORTANT
When replacing MOD CON BOARD or RAM IC49,
SEE PAGE 38 (P.48 for early 500 units).

CHANGE INFORMATION

(Each heading is followed by address to the circuit diagram.)

1. NOISE GENERATOR (D-H, 18-27)

IC3: from TL082 to BA662 having AGC.
NOISE LEVEL VR1: omitted

SAMPLING SIGNAL
Previous circuit:
Only white noise is routed to S/H circuit regardless of VCO-2 RANGE position.
New circuit:
Pink noise is selected for S/H when RANGE is in LOW position.

2. D/A CONVERTER (O-R, 23)

Ladder Resistors: from discrete to resistor array

3. NOISE KILLER SWITCH (D-E, 28)

Newly attached for cutting off noise signlas. Used in particular adjustments. Close this switch when step states "Place a ground to MOD CON TP-4".

4. RESONANCE SWITCH (M,33)

To emphasis regeneration to the point of oscillation. Used for factory adjustment only.

5. LFO DELAY CONTROL (R, 33)

From TR25 and TR26 to single paired-transistor TR25 to have U and L delay times synchronize with each other.

6. LFO RATE (V,33)

From TR11 and TR12 to single paired-transistor TR11. To minimize speed difference between U and L LFOs.

7. Add D29 and C95 to +B pin of IC7 (S, 36) to stabilize the supply voltage

8. Add RC filters on EXT CV lines (L, 43; S, 41; E, 35; D, 33)

To filter out noise induced into EXT CV.

9. VCO LEVEL (J, 33-34)

Apply a ground to pin 5 of IC2 through R21, previously −15V. Change resistors values in this section
To set VCO-1 and VCO-2 audio levels to an equal amount when SOURCE MIX is set at 12 o'clock position.
To have the same volume changes in VCO-1 and VCO-2 sounds, that is, the change in volume of VCO-1 when SOURCE MIX is being rotated toward VCO-1 is the same as that of VCO-2 when S.M. being toward VCO2.

10. VCA MOD (O, 38-39)

Add C97 across pins 1 and 2 of IC13
To eliminate click noises at positive or negative going transient.

11. Add TP-8 (Q, 36-37)

For factory adjustment only.

IC49, RAM 2101 and 5101
SN 202210-UP

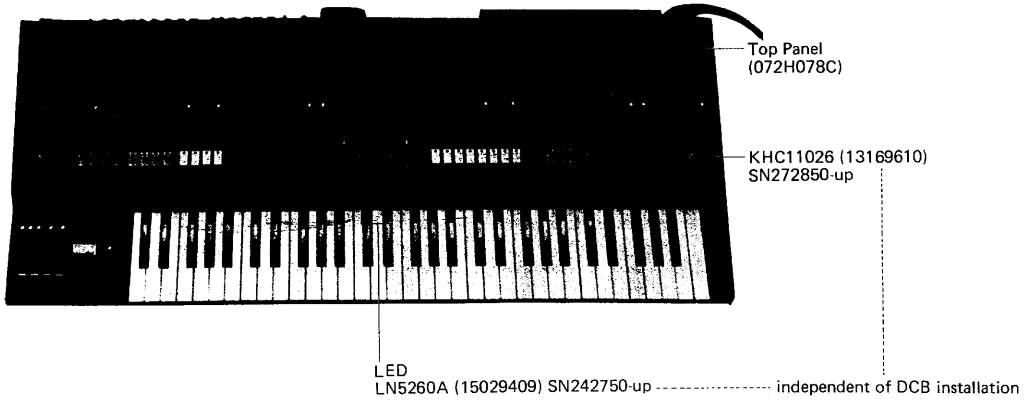
Often, RAM 2101 is substituted by 5101 upon manufacturing or shipping replacement because of procurement problem.
RAMs of these models have different characteristics in timing response.
To make both RAMs compatible, factory modification on CPU board started with above Serial number. (See p.38 for detail.)

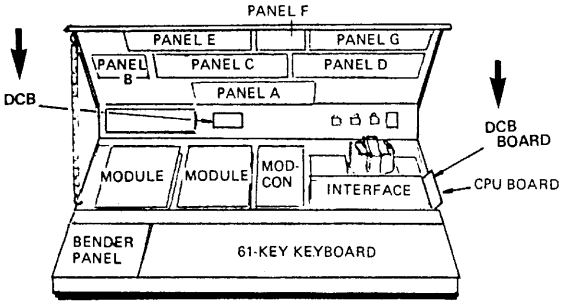
NOTE:
Beside suffix (A, B, etc.), the PCBs occasionally bear marks "●" and/or "o" above its code number to show the edition● stands for 1, and o for 5. example: o●●● 8th edition.

CHANGES,MODIFICATIONS,ADDITIONS

INVOLVED IN IMPLEMENTING DCB (Digital Communication Bus) BOARD

pp.40-47

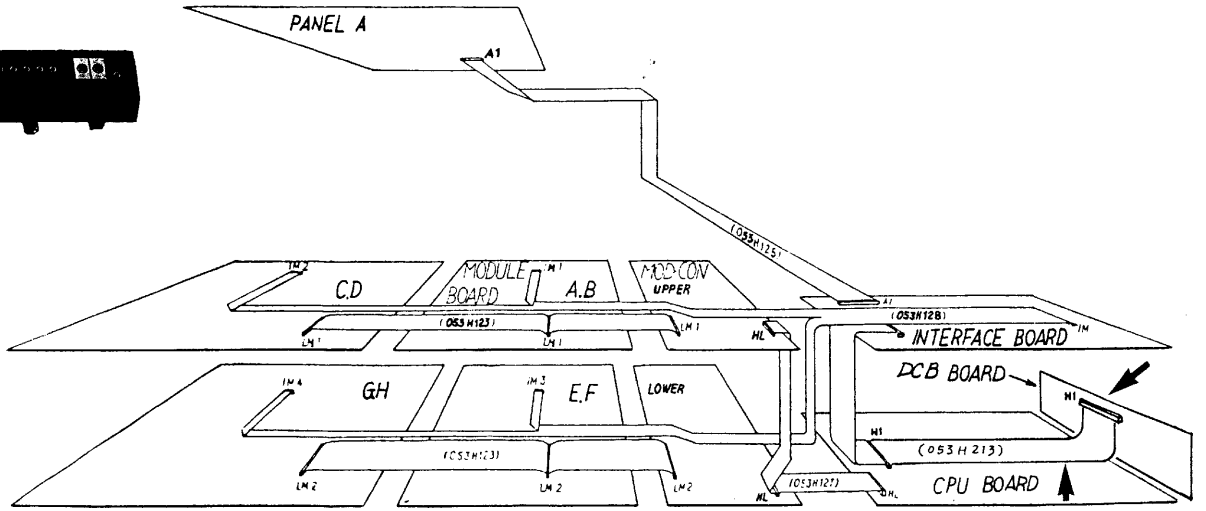




Holder (064H184)

DCB Connector
57-40140R (13429611)
Holder (064H153A)

Slide Switch
SSB-022-12RN (13159118)



CIRCUIT DESCRIPTION

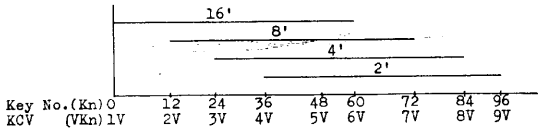
This circuit description applies to the JP-8 with serial numbers 171700 and up where DAC changed from 12- to 14-bit version, and concentrates on computune program which is revised in line with the change.

This description makes reference to pages 6 and 7 "WIDTH" and "KCV" of the Circuit Description of First Edition issued separately.

WIDTH

P. 6 Change title to WIDTH & TUNE

The coverage of the JP-8 keyboard is expansible to 96 keys using footage selector (RANGE SWITCH). In the following, KCV and key designation are defined as below.



In this mutual arrangement any KCV (VKnx) at a key (Knx) is obtained from the equations:

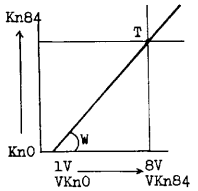
VKnx = VKno + W(WIDTH) x Knx (1)

or VKnx = T(TUNE) − W(84 − Knx) (2)

where, W = 1/12(V)

—— voltage steps per half tone

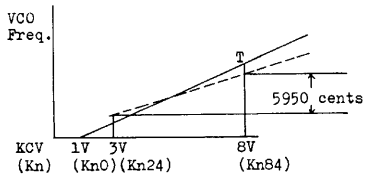
T = VKn84



In the following computuning, T is a reference voltage in calculating every KCVs to the equation (2) above.

Upon power on for the JP-8, computune program starts frequency measurements at two points with MOD.A VCO-1 by applying KCV of Kn24(3V) and VKn84(8V) to it. If the VCO output is 20 cents higher than expected pitch at 3V KCV, and 30 cents lower at 8V as shown in the figure right, the factor W is given by:

$$\frac{8-3\,(V)}{9570-3620\,(cent)} = 0.084$$



Substituting 0.084 for W in equation (2) above would provide the VCO with KCVs for every keys, and the VCO will oscillate in 1V/oct steps with most of pitches slightly out of tune.

To bring each note in tune, the program first adds fine tune voltage (bias) ... $0.084 \times \frac{30}{100}$(cent) = 0.0252V − to T. Then, finds KCVs for every notes by applying equation (2).

Example: VKn24 = 8.025(T) − 0.084(W) x (84 − 24) = 2.985V.

When compare this WIDTH with the WIDTH determined by previous 12-bit system, the new system provides more precise resultant because of wider measurement range.

INITIAL TUNING UPON POWER ON

When the power is first turned on for the JP-8, thermally unstalbe VCO tends to oscillate on frequencies which are greatly deviating from the expected frequency so that computune circuitry will not be able to determine exact pitch error at a time. If a program encounters such a VCO, the program ceases measurement for that VCO but retains the data, then proceeds to the next VCO. After all the VCOs have been measured, the program ressumes operation from the first VCO, depending on the previous data. However, the process is repeated only two times per oscillator, regardless of the frequency deviation. Properly functioning VCOs will be brought into tolerance at the second time.

Most VCOs outside tolerances after completion of the second execution might be brought closer and closer to desired pitches if the computune program is forced to repeat the operation by manual triggering of TUNE button. (See next paragraph.)

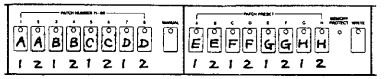
Tuning sequence is visually comfirmed on flashing LEDs in the PATCH buttons.

VCO BEING MEASURED

	1st cycle		2nd cycle	
PATCH NO.	MODULE	VCO	MODULE	VCO
1	A	1	E	1
2	A	2	E	2
3	B	1	F	1
. . .	. . .	. . .	. . .	. . .
8	D	2	H	2

However, when one PATCH LED stays on while MANUAL LED is flashing, they are indicating failure in that VCO. The computune program cannot correct such a VCO as is indicated by a PATCH button as below, and does not proceed to the next VCO unless one of function switches is touched.

MODULE
VCO



COMPUTUNE WITH TUNE BUTTON

When the computune program is triggered manually with TUNE button (after power-on-tune), it runs only once for each VCO since the program already had data on fine tune, and drastical change in VCO frequencies is likely to occur. If the program fails to compensate frequency drift, iterative tapping of "TUNE" will bring VCO closer to correct pitch. Relying on this method is prefarable only in an emergency; the cause of out of tune must be eliminated as early as possible.

KCV (INTERFACE BOARD)

P. 7 Lines 9 and 10: Delete

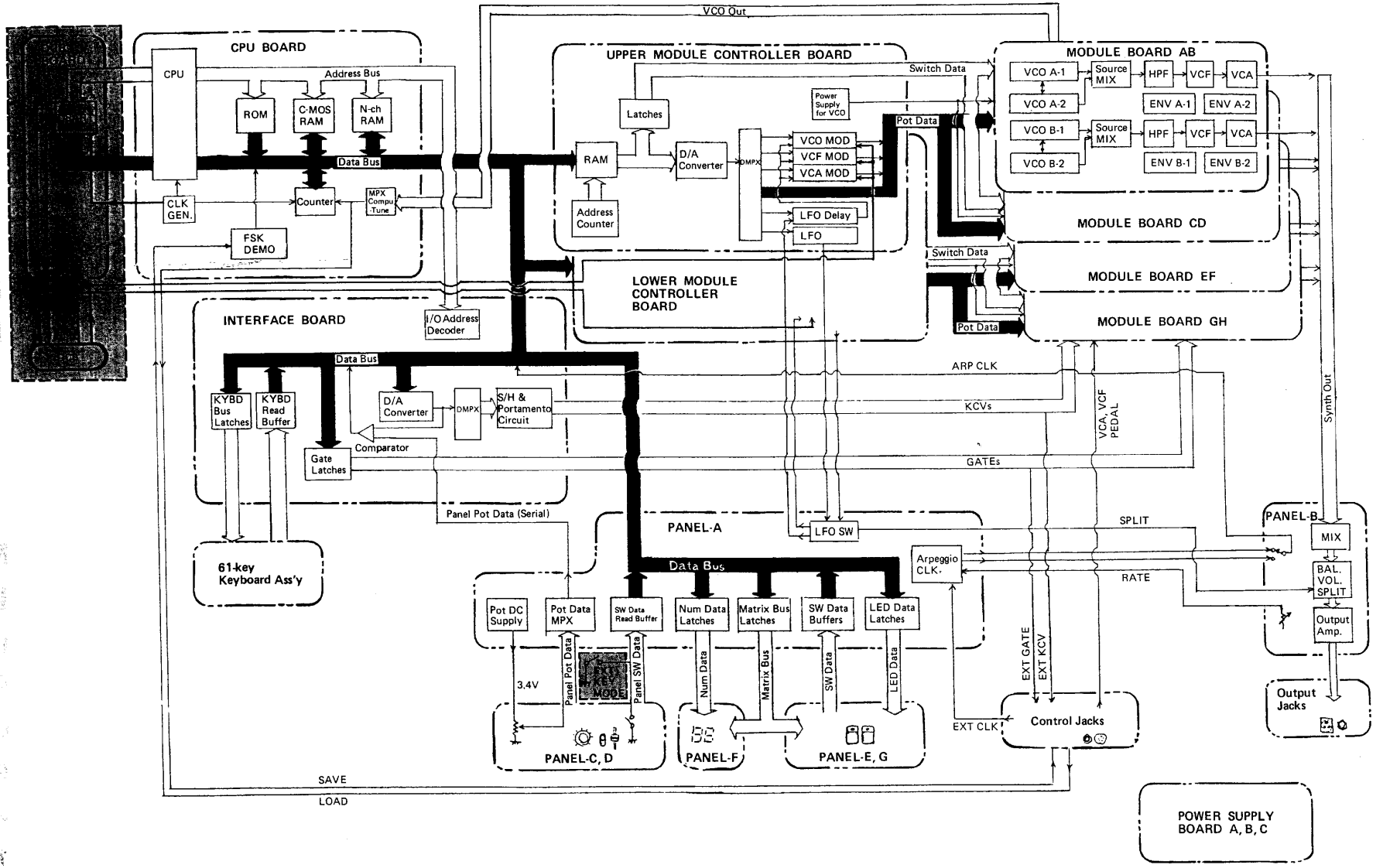
Lines 11-17: Reads as follows.

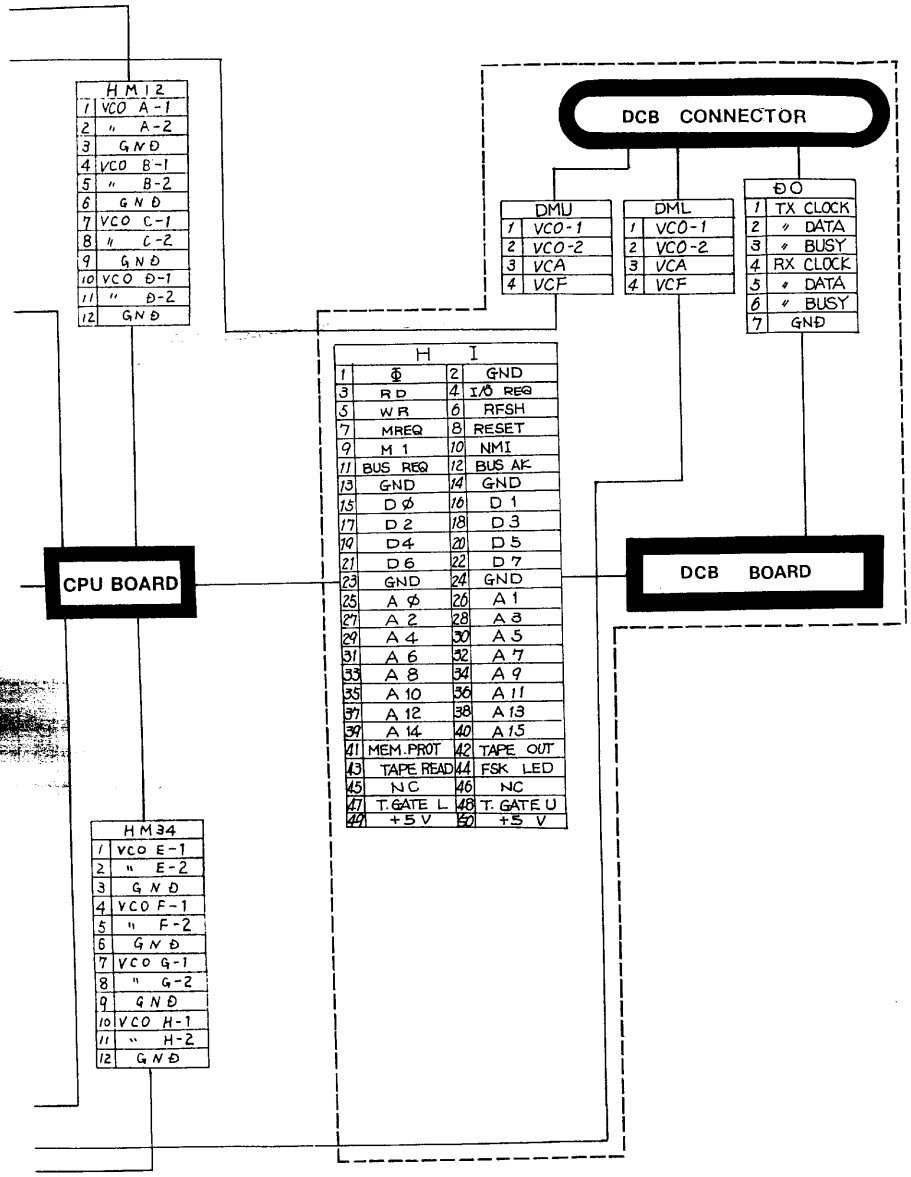
Each KCV data is represented in 14-bit format and is divided into two pieces—MS (most significant) 8-bit is latched by IC15 followed by LS 6-bit into IC13. DAC output has a range of 0-10V against 14 bits, thus resolution is $10V \div 2^{14}$ (bit) = 0.6mV, nearly equals 0.7 cents in pitch. Durig I/V conversion in ½IC24, CV for EXT. jack is scaled 1V/oct.

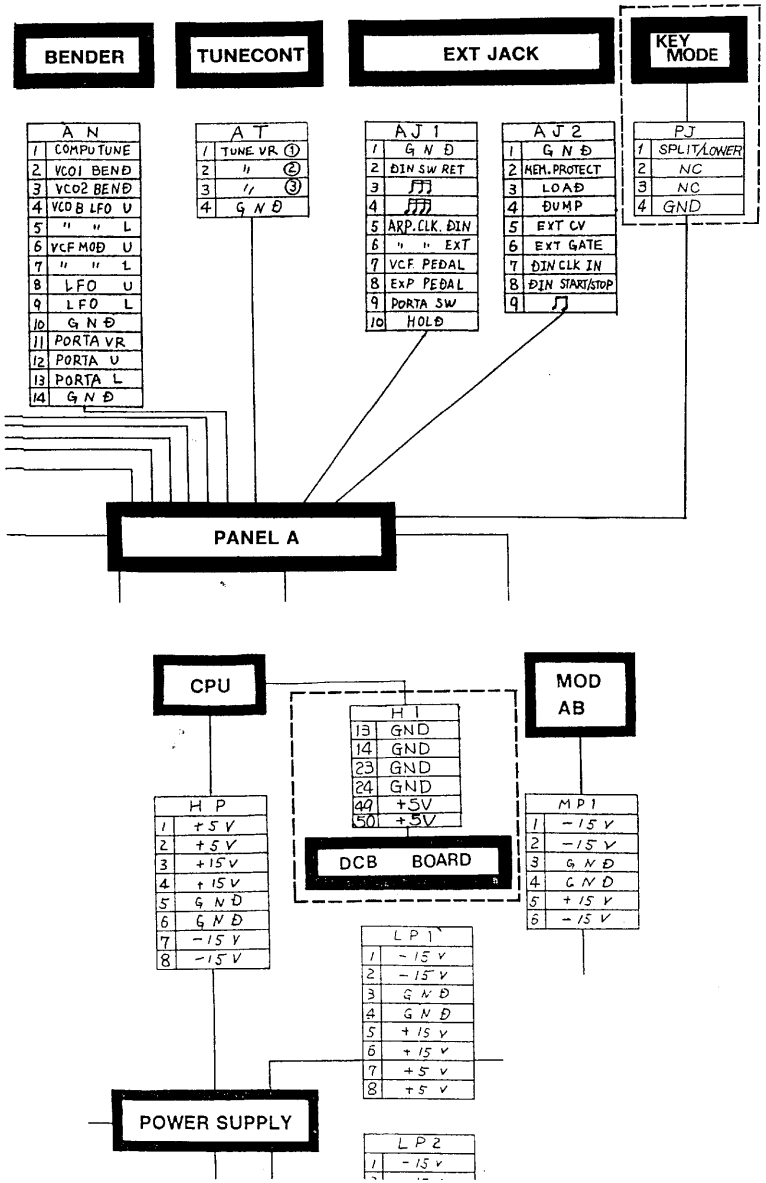
CORRECTION
CIRCUIT DESCRIPTION

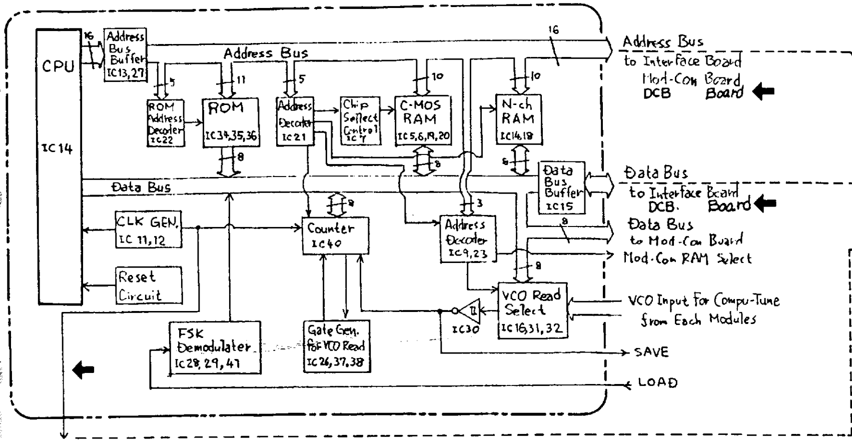
P. 11: PUSH SWITCH SCANNING

Push switches (function switches with LED) are read every approximately 25ms (not 1ms). See timing chart on page 3 of the Circuit Description. LEDs are lit every 1ms when INT signal is applied from IC26 which in turn is timed by the signal generated at pin 17 of IC40. Failure of INT signal causes no LED driving signal, but has no relation to the switch reading performance.


CPU BOARD
CPU
Address Bus
ROM
C-MOS RAM
N-ch RAM
Data Bus
CLK GEN.
Counter
MPX Compu-Tune
FSK DEMO
VCO Out
UPPER MODULE CONTROLLER BOARD
Switch Data
Latches
Power Supply for VCO
Pot Data
RAM
D/A Converter
DMPX
VCO MOD
VCF MOD
VCA MOD
Address Counter
LFO Delay
LFO
MODULE BOARD AB
VCO A-1
VCO A-2
VCO B-1
VCO B-2
Source MIX
HPF
VCF
VCA
ENV A-1
ENV A-2
ENV B-1
ENV B-2
MODULE BOARD CD
Switch Data
MODULE BOARD EF
Pot Data
MODULE BOARD GH
LOWER MODULE CONTROLLER BOARD
INTERFACE BOARD
I/O Address Decoder
Data Bus
KYBD Bus Latches
KYBD Read Buffer
D/A Converter
DMPX
S/H & Portamento Circuit
Comparator
Gate Latches
ARP CLK
KCVs
VCA, VCF PEDAL
GATEs
Synth Out
Panel Pot Data (Serial)
PANEL-A
LFO SW
SPLIT
PANEL-B
MIX
BAL. VOL. SPLIT
Output Amp.
61-key Keyboard Ass'y
Arpeggio CLK.
RATE
Data Bus
Pot DC Supply
Pot Data MPX
SW Data Read Buffer
Num Data Latches
Matrix Bus Latches
SW Data Buffers
LED Data Latches
3.4V
Panel Pot Data
Panel SW Data
Num Data
Matrix Bus
SW Data
LED Data
EXT GATE
EXT KCV
EXT CLK
Control Jacks
Output Jacks
PANEL-C, D
PANEL-F
PANEL-E, G
SAVE
LOAD
POWER SUPPLY BOARD A, B, C

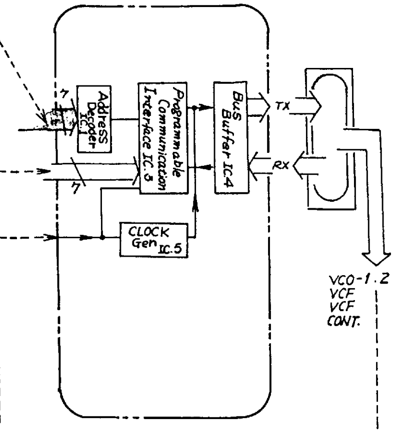

HM12
1 VCO A-1
2 " A-2
3 GND
4 VCO B-1
5 " B-2
6 GND
7 VCO C-1
8 " C-2
9 GND
10 VCO D-1
11 " D-2
12 GND
DCB CONNECTOR
DMU
1 VCO-1
2 VCO-2
3 VCA
4 VCF
DML
1 VCO-1
2 VCO-2
3 VCA
4 VCF
DO
1 TX CLOCK
2 " DATA
3 " BUSY
4 RX CLOCK
5 " DATA
6 " BUSY
7 GND
H I
1 Φ 2 GND
3 RD 4 I/O REQ
5 WR 6 RFSH
7 MREQ 8 RESET
9 M1 10 NMI
11 BUS REQ 12 BUS AK
13 GND 14 GND
15 DØ 16 D1
17 D2 18 D3
19 D4 20 D5
21 D6 22 D7
23 GND 24 GND
25 AØ 26 A1
27 A2 28 A3
29 A4 30 A5
31 A6 32 A7
33 A8 34 A9
35 A10 36 A11
37 A12 38 A13
39 A14 40 A15
41 MEM.PROT 42 TAPE OUT
43 TAPE READ 44 FSK LED
45 NC 46 NC
47 T.GATE L 48 T.GATE U
49 +5V 50 +5V
CPU BOARD
DCB BOARD
HM34
1 VCO E-1
2 " E-2
3 GND
4 VCO F-1
5 " F-2
6 GND
7 VCO G-1
8 " G-2
9 GND
10 VCO H-1
11 " H-2
12 GND


BENDER
TUNECONT
EXT JACK
KEY MODE
AN
1 COMPUTUNE
2 VCO1 BENØ
3 VCO2 BENØ
4 VCO B LFO U
5 " " L
6 VCF MOØ U
7 " " L
8 LFO U
9 LFO L
10 GNØ
11 PORTA VR
12 PORTA U
13 PORTA L
14 GNØ
AT
1 TUNE VR ①
2 " ②
3 " ③
4 GNØ
AJ1
1 GNØ
2 DIN SW RET
3
4
5 ARP.CLK. DIN
6 " " EXT
7 VCF PEDAL
8 EXP PEDAL
9 PORTA SW
10 HOLØ
AJ2
1 GNØ
2 KEM. PROTECT
3 LOAØ
4 ØUMP
5 EXT CV
6 EXT GATE
7 ØIN CLK IN
8 ØIN START/STOP
9
PJ
1 SPLIT/LOWER
2 NC
3 NC
4 GND
PANEL A
CPU
MOD AB
H1
13 GND
14 GND
23 GND
24 GND
49 +5V
50 +5V
DCB BOARD
HP
1 +5V
2 +5V
3 +15V
4 +15V
5 GNØ
6 GNØ
7 -15V
8 -15V
MP1
1 -15V
2 -15V
3 GNØ
4 GNØ
5 +15V
6 -15V
LP1
1 -15V
2 -15V
3 GNØ
4 GNØ
5 +15V
6 +15V
7 +5V
8 +5V
POWER SUPPLY
LP2
1 -15V

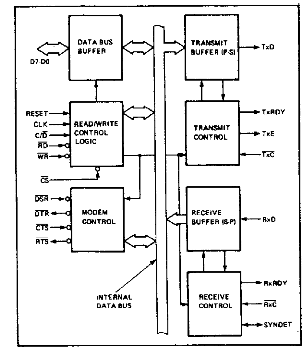


CPU
IC14
Address Bus Buffer IC13,27
Address Bus
ROM Address Decoder IC22
ROM IC34,35,36
Address Decoder IC21
Chip Select Control IC7
C-MOS RAM IC5,6,19,20
N-ch RAM IC14,18
Data Bus
Data Bus Buffer IC15
CLK GEN. IC 11,12
Counter IC40
Address Decoder IC9,23
Reset Circuit
VCO Read Select IC16,31,32
IC30
FSK Demodulater IC28,29,41
Gate Gen. for VCO Read IC26,37,38
Address Bus to Interface Board Mod-Con Board DCB Board
Data Bus to Interface Board DCB Board
Data Bus to Mod-Con Board
Mod-Con RAM Select
VCO Input For Compu-Tune from Each Modules
SAVE
LOAD
PCB BOARD

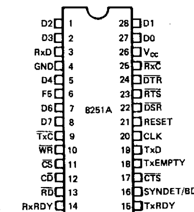
CPU BOARD BLOCK DIAGRAM

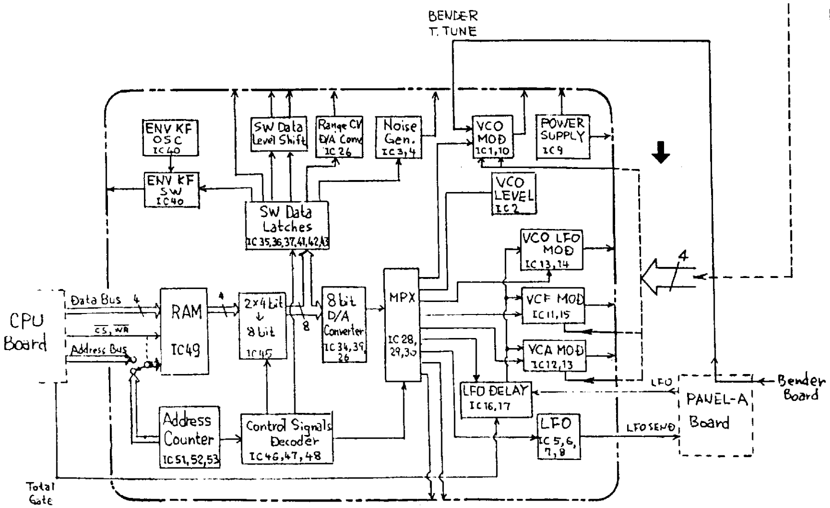


DCB BOARD



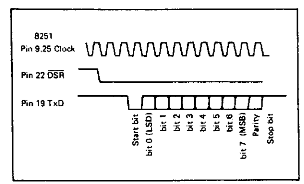
8251 (Top View)





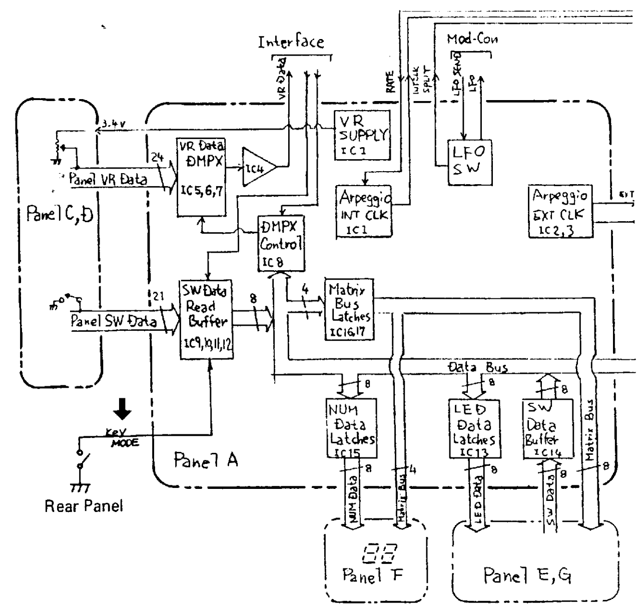
BENDER T. TUNE
ENV KF OSC IC40
ENV KF SW IC40
SW Data Level Shift
Range CV D/A Conv IC26
Noise Gen. IC3,4
VCO MOD IC1,10
POWER SUPPLY IC9
VCO LEVEL IC2
SW Data Latches IC35,36,37,41,42,43
VCO LFO MOD IC13,14
CPU Board
Data Bus
CS, WR
Address Bus
RAM IC49
2×4 bit ↓ 8 bit IC45
8 bit D/A Converter IC34,39 26
MPX IC28, 29,30
VCF MOD IC11,15
VCA MOD IC12,13
LFO DELAY IC16,17
LFO IC5,6,7,8
Address Counter IC51,52,53
Control Signals Decoder IC46,47,48
PANEL-A Board
Bender Board
LFO
LFO SEND
Total Gate

MOD-CON BOARD BLOCK DIAGRUM



8251

D7-D0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Recover Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

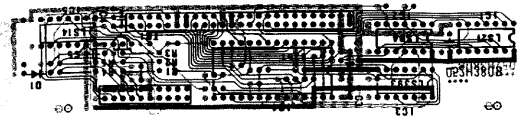


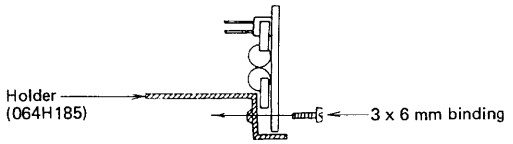
Interface
Mod-Con
VR Data
RATE
LFO SEND
LFO
3.4v
Panel VR Data
VR Data DMPX IC5,6,7
IC4
VR SUPPLY IC2
LFO SW
Arpeggio INT CLK IC1
Arpeggio EXT CLK IC2,3
Panel C,D
DMPX Control IC8
Panel SW Data
SW Data Read Buffer IC9,10,11,12
Matrix Bus Latches IC16,17
Data Bus
KEY MODE
Rear Panel
Panel A
NUM Data Latches IC15
LED Data Latches IC13
SW Data Buffer IC14
Matrix Bus
NUM Data
LED Data
SW Data
Panel F
Panel E,G

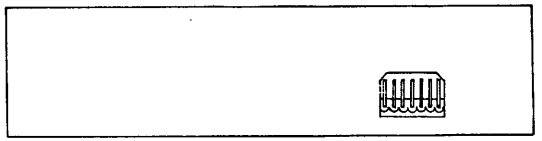
DCB BOARD

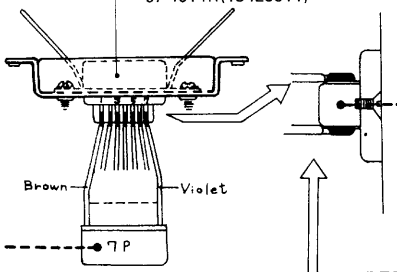
OPH220 (149H220) (pcb 052H380B)

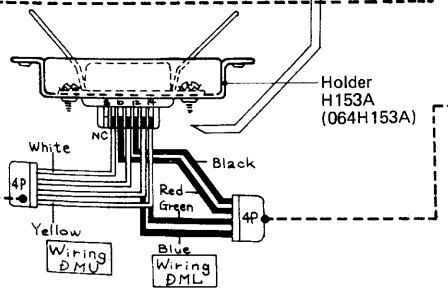
FCN724PC50-AU/L



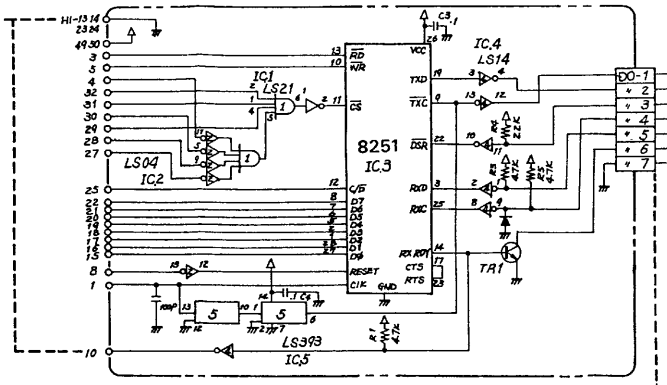




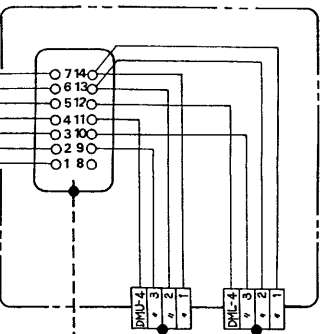




DCB BOARD



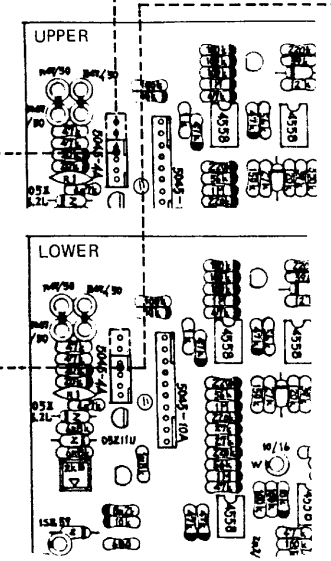
DCB CONNECTOR ASS'Y



DCB PIN ASSIGNMENT

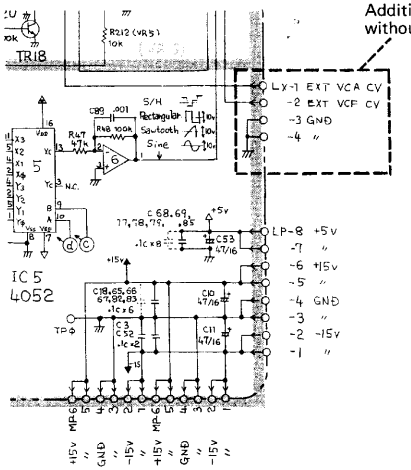
PIN	DESCRIPTION	PIN	DESCRIPTION
1	RX BUSY	8	NC
2	" DATA	9	VCA UPPER
3	" CLOCK	10	LOWER
4	GND	11	VCF UPPER
5	TX BUSY	12	LOWER
6	" DATA	13	VCO-2
7	" CLOCK	14	VCO-1

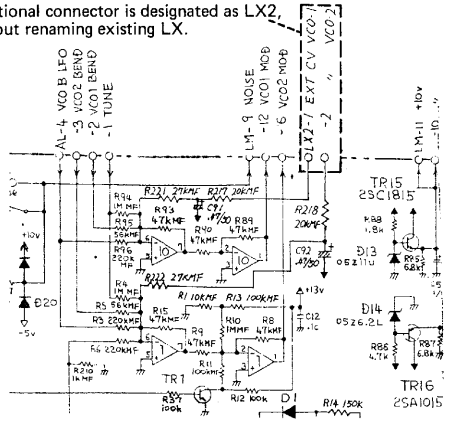
DCB (Digital Communication Bus)



MODULE CONTROLLER BOARD

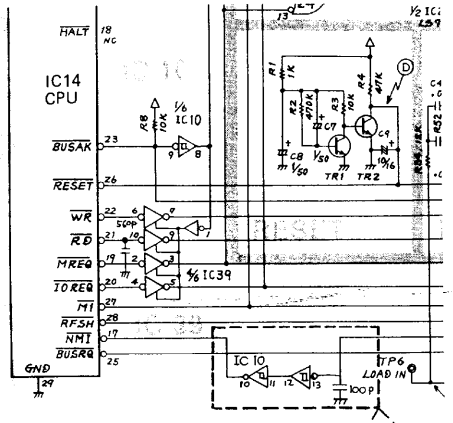
Additional connector is designated as LX2, without renaming existing LX.

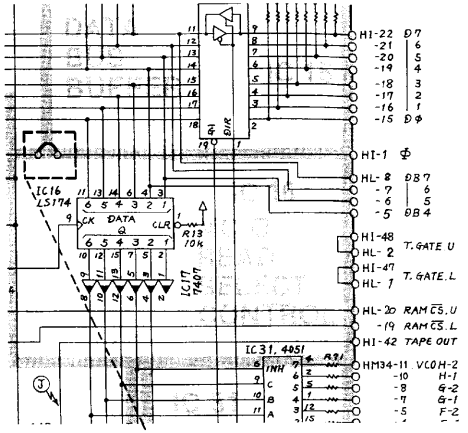




Circuits Changes related to DCB Board Installation

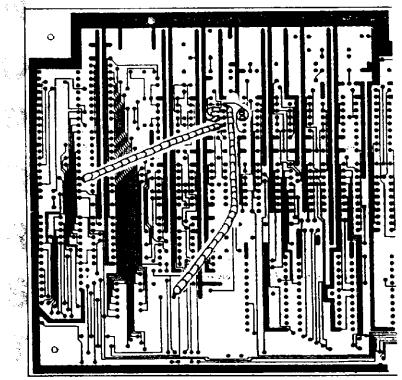
CPU BOARD



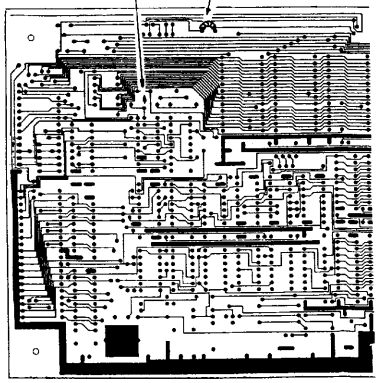


JUMPER ——— 3
CAPACITOR (100P) - 1

CUT JUMPER

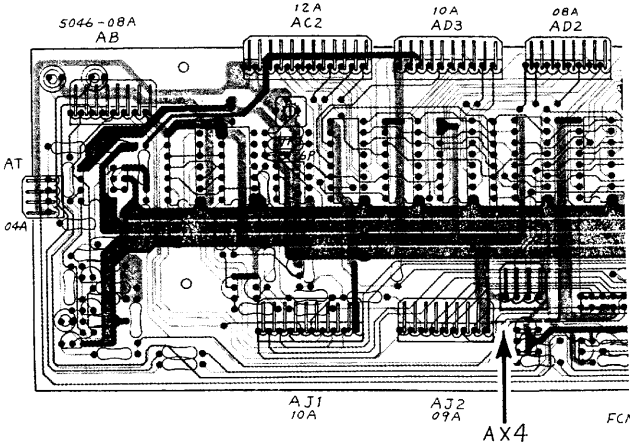


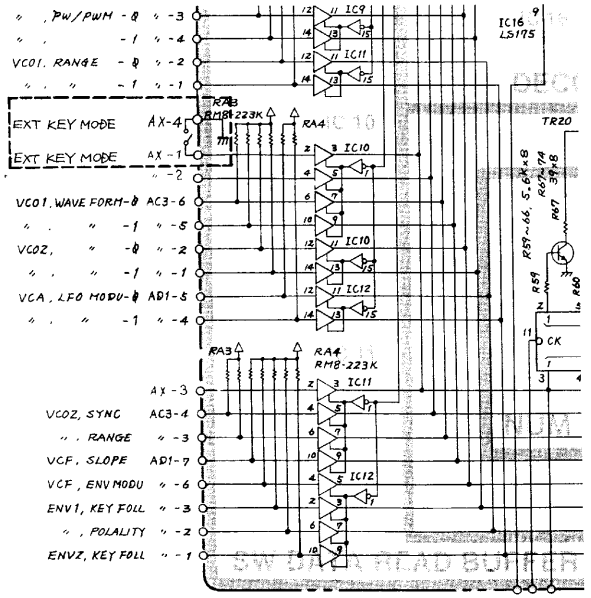
Foil Side



Component Side

PANEL BOARD A





DIAGNOSTIC PROGRAM IN PROM D

On the CPU board (of JP-8 furnished with the OC-8 or DCB board) located is IC33 (3.3D or 3.4D) which contains not only digital communication program, but also disgnostic program. The program, when executed in the TEST mode, simplifies testing and fault isolation of some of the ICs and their associated circuits listing to the right. For this program to run, the remaining PROMs (IC34–IC36) of CPU board must be of 3.2 version.

PRECAUTIONS

Allow plenty of time for warm-up (approx. 30 minutes).
If the CPU, PROMs or other circuits fail to perform their basic functions, the program will not start.

STEPS

1. Turn the JP-8 OFF.
2. To put the JP-8 into the TEST mode, either;
   a) Turn the power ON while pressing PATCH NUMBER buttons 1 and 3.
      or
   b) Set SI-1 and SI-2 of the Interface board to TEST, then turn the power ON.

The test program is executed in the order listed and is stopped wherever it encounters a defective IC (or a problem pertaining to a particular IC), and displays the suspected IC number in the window.
To resume the program, press any touch button. (For example, MANUAL.)

At the end of program, the window displays both the PROM D version and the DAC's bit format, for example;

33 12 -- 3.3D, 12-bit DAC
34 14 -- 3.4D, 14-bit DAC

	IC 36	IC36	PROM A
	IC 35	IC35	PROM B
	IC 34	IC34	PROM C
	IC 33	IC33	PROM D
①	IC 06	IC 6	RAM
	IC 05	IC 5	RAM
②	IC 20	IC20	RAM
	IC 19	IC19	RAM
	IC 04	IC 4	RAM
	IC 18	IC18	RAM
③	dA 00	Module A VCO-1, KCV=0, etc.	
④	dA 01	IC14, IC15	D/A MSB
	dA 02	IC14, IC15	D/A B2
	dA 03	IC14, IC15	D/A B3
	dA 04	IC14, IC15	D/A B4
	dA 05	IC14, IC15	D/A B5
	dA 06	IC14, IC15	D/A B6
	dA 07	IC14, IC15	D/A B7
	dA 08	IC14, IC15	D/A B8
	dA 09	IC14, IC13	D/A B9
	dA 10	IC14, IC13	D/A B10
	dA 11	IC14, IC13	D/A B11
	dA 12	IC14, IC13	D/A B12
⑤	dA 13	IC14, IC13	D/A B13
	dA 14	IC14, IC13	D/A LSB

NOTES FOR TABLE

1. 3.3D doesn't check IC5 and IC6.
2. Because of misprogramming, 3.3D will display these IC numbers in reverse order. If displayed, read;
   IC20 as IC19, and IC19 as IC20.
3. Output from Module A VCO-1 is applied to the DAC Check. Consequently, if this VCO fails, all the remaining tests will not be performed.
   Push any button, and the version with 00 is displayed.
4. IC13 and IC15 on the 12-bit interface board are inversely numbered.
   Read; IC13 as IC15, and IC15 as IC13.
5. If the 13-bit line malfunctions in the 14-bit D/A, the CPU concludes that the D/A is 12-bit, and skips the 13th and 14th bits.

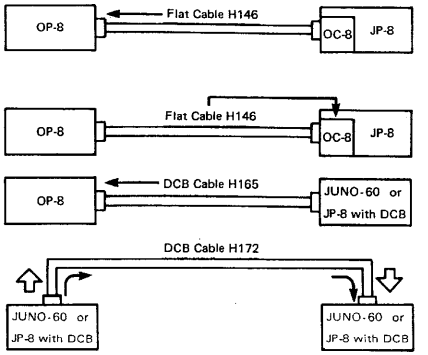
DESCRIPTION OF CONNECTION CABLES

In the below, SN refers to Serial Number of OP-8.

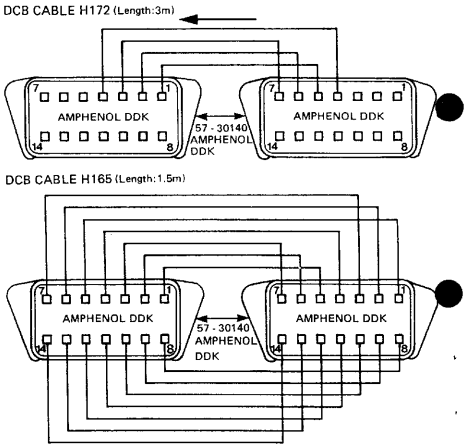
- For serial numbers up to and including SN220269, the OP-8 was provided with Flat Cable H146 for connecting the OP-8 to the JP-8.

- Effective from serial number SN230270, the OP-8 unit can be connected to the JP-8 through the Flat Cable H146 provided with the OC-8 unit, or to the JUNO-60 through the DCB Cable H165 provided with the OP-8 unit.

- Roland provides not only DCB Cable H165 but also DCB Cable H172 for interconnecting JP-8 or JUNO-60 as shown here.

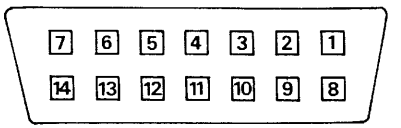


- DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector.
  When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled.
  Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60.
  Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.
  On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.



1. BUSY) RX
2. DATA
3. CLOCK)
4. GND
5. BUSY) TX
6. DATA
7. CLOCK)
8. UNREG
9. VCA LOWER
10. VCA UPPER
11. VCF LOWER
12. VCF UPPER
13. VCO-2
14. VCO-1

DCB Pin Configurations



(View from Rear Panel)

APPENDIX

PCB EDITION

Dot and circle above PCB code are indicative of edition; "•" stands for 1, and "○" for 5. Example: ○• = 6th edition.

Illustrated on pp. 48-50 is information on MODULE and MODULE CONRTOLLER Boards mounted on the JP-8 models with serial numbers up to 090599. For circuit diagram, refer to p.11 or p.12 although some small discrepancies may exist.

CAUTION ON REPLACEMENT OF PCBs IN THIS SECTION

Although terminal for terminal compatible, when mix used, new and old PCBs process signals in slightly different way, reproducing voices that are distinguishable form each other. Therefore, when replacing MODULE or MOD CON board in this section, use a set of PCBs of the same edition group as described below.

NOTE: Replacement of MODULE board can be made independently of MOD CON board, and vice versa.

MODULE CONTROLLER BOARD		MODULE BOAD	
group A	group B		When replacements for MOD CON are of group B, check IC49 (RAM) for name. If it is 5101, see p.38 for necessary modification.
○••• 052H269 or ○••• 052H269	○•••• 052H269-up	○ 052H270-up	

Listing below are descriptions of surface mounting, jumper wire, and conductive foil cut made on the MOD COM boards up to the abovementioned serial numbers, shown on the next page.

ABBREVIATIONS

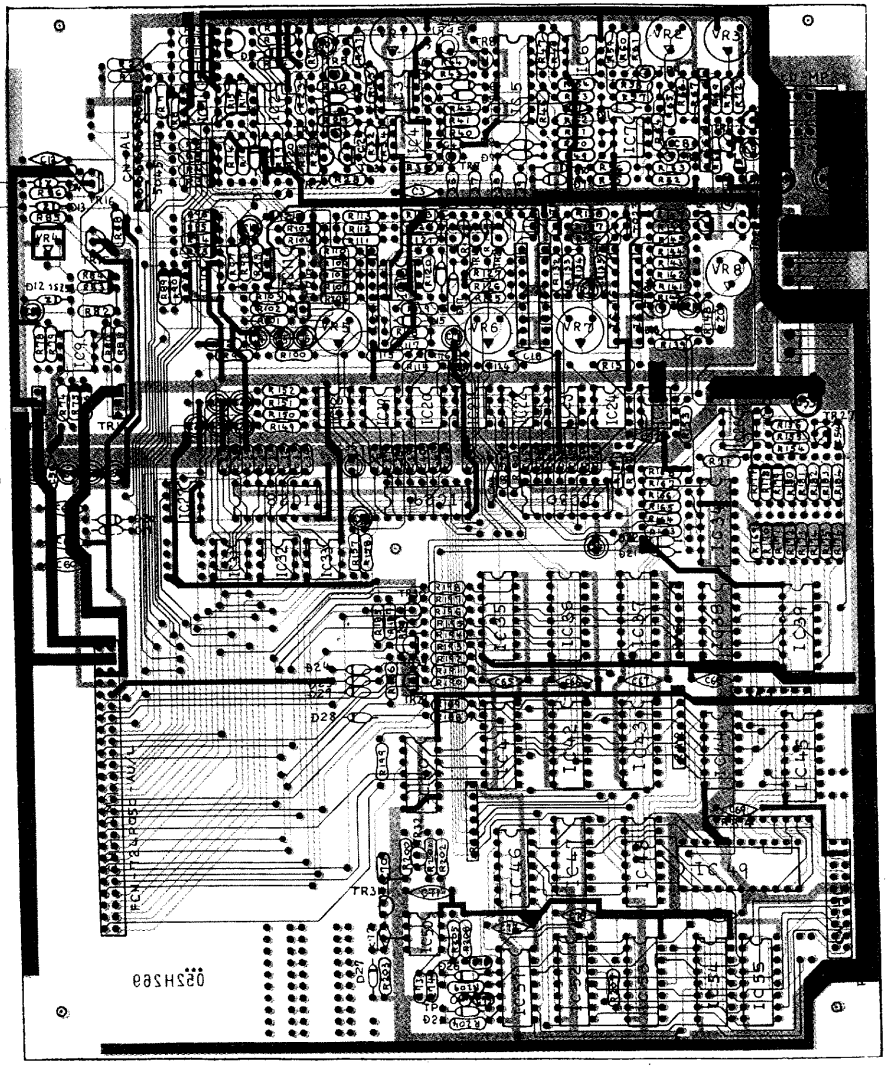
C-pattern cut Di-diode R-resistor J-jumper M-mylar cap

Serial numbers

1B-050199 2A-050200 2B-060299 3A-060300 4A-070400 5A-080500 5B-090599

No.	Part	SN	No.	Part	SN
1	C	up to 2B	10	R	5A-up
2	C	3A-5B	11	R	3A-5B
3	C				
4	D	up to 1B	12	D 2xC	3A-5B
5	R	3A-5B	13	M.R.C	2A-up
6	J	up to 2B	14	J.C	4A-5B
7	J.C	4A-5B	15	M	4A-5B
8	J	5A-up	16	J.C	2A-5B
9	R	up to 2B	17	M	3A-5B

MODULE CONTROLLER BOARD
(PCB ○••• 052H269, ○•••• 052H269, ○ 052H269, ○• 052H269)



PARTS LIST CHANGE

PART. SERIAL NO.	FROM	TO	PART NO.
INTERFACE BOARD			
SN 171700			
PCB Ass'y	OPH122	OPH122A	149H122A
PCB	052H268	052H268	
D/A Converter (IC14)	Am6012	ITS80141	15219127
Latches	LS273	TC40H273 (IC15, CMOS)	15159507
	LS175	TC40H174 (IC13, CMOS)	15159511
	LS175	TC40H175 (IC11, CMOS)	15159512
IC25, IC26	TC4051	HD14051 (CMOS) (Hitachi only)	15159113H0
IC22	LS02	TC4001	15159101T0
IC9	74LS74	4013BP (CMOS)	15159105T1
SN 212330			
IC9	4013	TC40H74P	15159510
	ICs: ALL INCOMPATIBLE		
CPU BOARD			
SN 171700			
IC34-IC36	μPD2716 (version 1.0)	μPD2716-JP8-A (IC36) μPD2716-JP8-B (IC35) μPD2716-JP8-C (IC34)	15179609 (version 3.x) 15179610 (version 3.x) 15179611 (version 3.x) (version 3.x = 3.1 or 3.2)
MODULE CONTROLLER BOARD			
SN 202100			
PCB Ass'y	OPH123	OPH123A	149H123A
PCB	052H269	052H269	
IC3	TL082	BA662A	15229802
Ladder Resistor	Discrete	R601611 (RA6)	
TRs, 11, 12, 25	2SA1015	2SA798-G (TR11)	15119108
TR26	2SC1815	2SA798-G (TR25)	15119108
Switches	.....	SSB212 (SWs 1, 2)	13159123
SN 202210			
IC49 RAM	2101 only	2101 or 5101	15179303
	(Compatible with minor modification. See pp. 37. 38.)		
PANEL BOARD F			
LED (display)			
SN 242750	LN526RA	LN526OA	15029409
	(Compatible but different in brightness and color; mix use should be avoided.)		
PANEL BOARD E			
PANEL BOARD G			
SN 272850			
Switches	KHC11901	KHC11026	13169610
(LEDs)	(AR3432S)	(SEL2210R)	
	(Switch proper remains unchanged. The new LED has better off-axis luminous density. Mix use should be avoided.)		

SN 282880-UP JP-8 WITH DCB BOARD

PART NAME	FROM	TO	PART NO.
Top Panel	Panel H78B	Panel H78C	072H078C
Chassis (jack)	Chassis H116	Chassis H116A	061H116A
Holder (rear)	.....	Holder H184	064H184
DCB BOARD			
PCB Ass'y	.....	OPH220	149H220 (pcb 052H380B)
Holder	.....	Holder H185	064H185
IC1	.....	74LS21	15169350
IC3	.....	μPD8251AC	15179112
Flat Cable	Flat Cable H126 (INTFCE-CPU)	Flat Cable H213 (INTERFACE-CPU-DCB)	053H213
DCB Connector	.....	57-40140R	13429611
Holder	.....	Holder H153	064H153
Slide Switch	.....	SSB-022-12RN	13159118
CPU BOARD			
IC33	.....	μPD2716-JP8-D	15179612 (version 3.4)

In order to expedite delivery of products or because of procurent problem, the factory is occasionally forced to make minor substitution of ICs.
Such substitutions will work satisfactorily and compatible with the initial IC unless otherwise noted in related sections (circuit diagram, parts list, etc.).

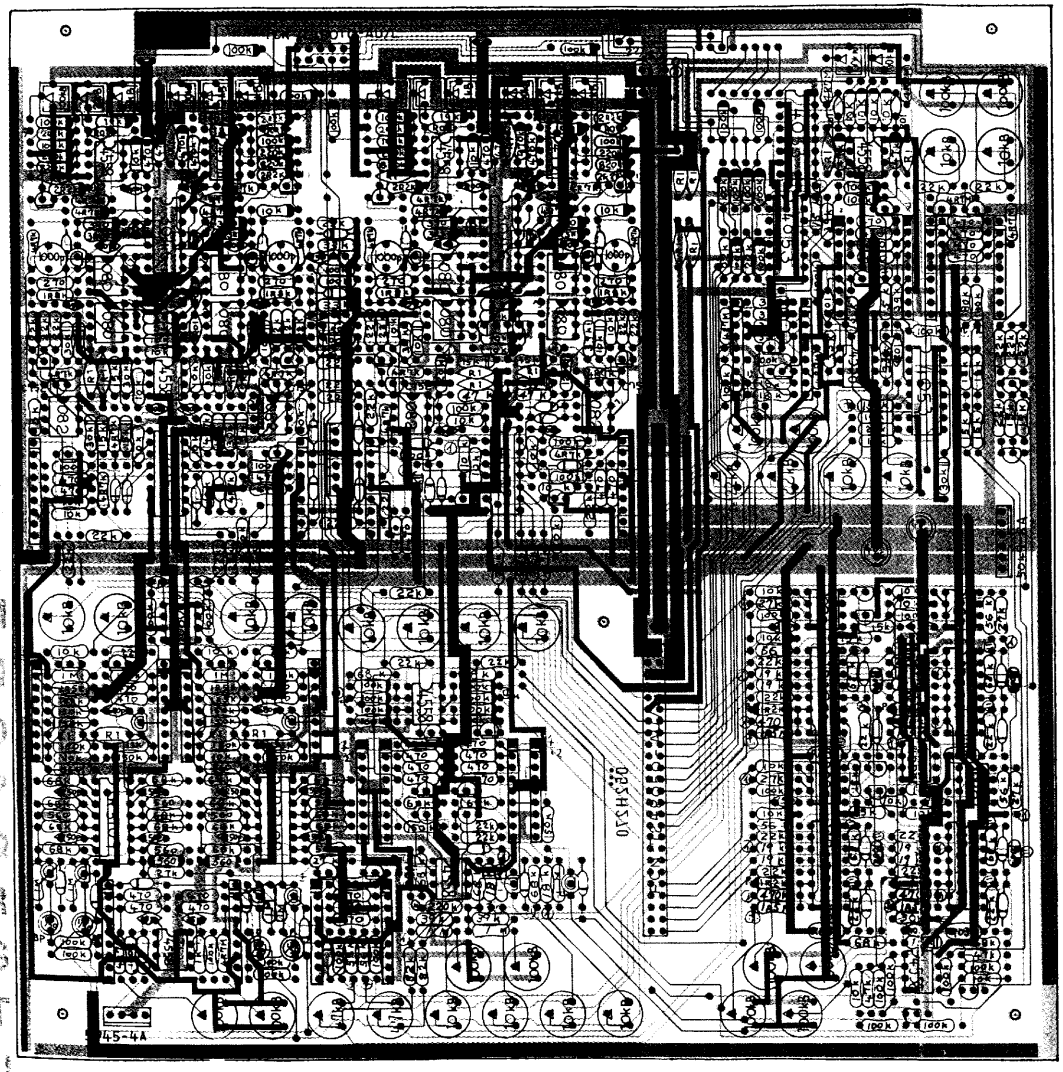
PART NUMBER

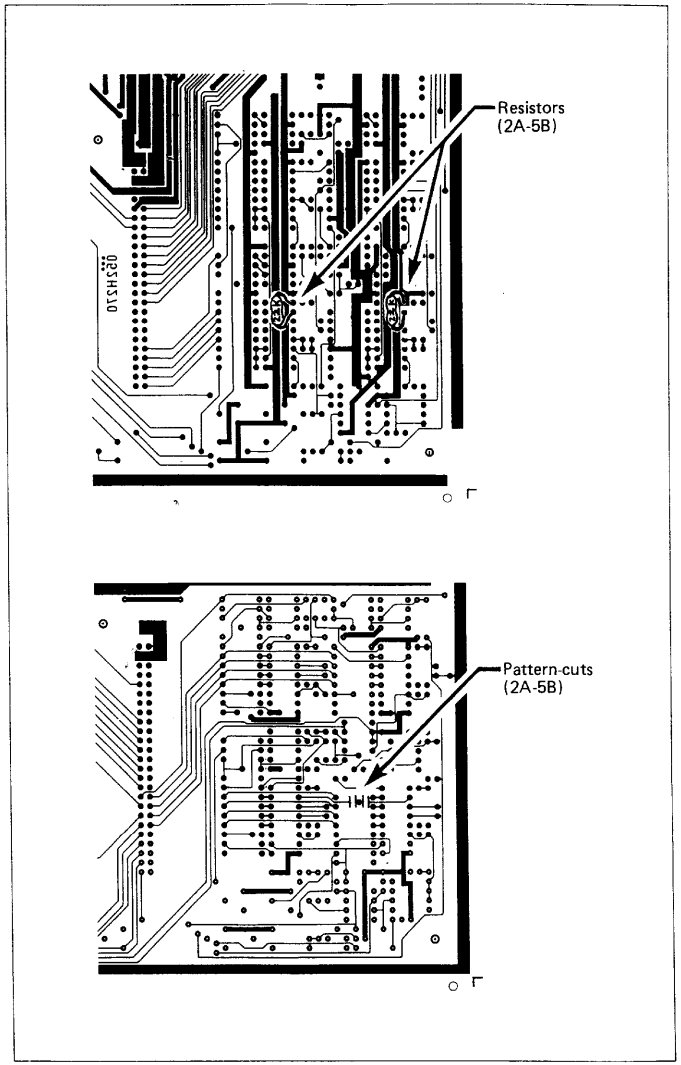
Usually, equivalent semiconductors are assigned to the same part number as initial component with two-letter suffix identifying the manufacturer. For example, TO – Toshiba, ZO – Motorola.
In ordering such ICs, uncertain suffix can be omitted from the part number, and the factory will supply suitable ones with notes or cautions, as necessary.

Parts on the PARTS LIST	Equivalent
TC4052BP	HD14052BP
TC4051BP	HD14051BP
TC40175BP	μPD4175BC
μPD2101ALC	M5L2101AP-4 μPD5101LC M5L5101LP-1
μPD780C-1	LH0080A
μPD2716D	M5L2716K MB8516
μPD444C	M58981P-45
μPD2114C	M5L2114LP
μPD8253C	M5L8253P-5
TL082CP	NJM082DR μPC4082C
74LS Series	M74LS series
74 . . Series (exp. 7406	M532 . . series M53206)

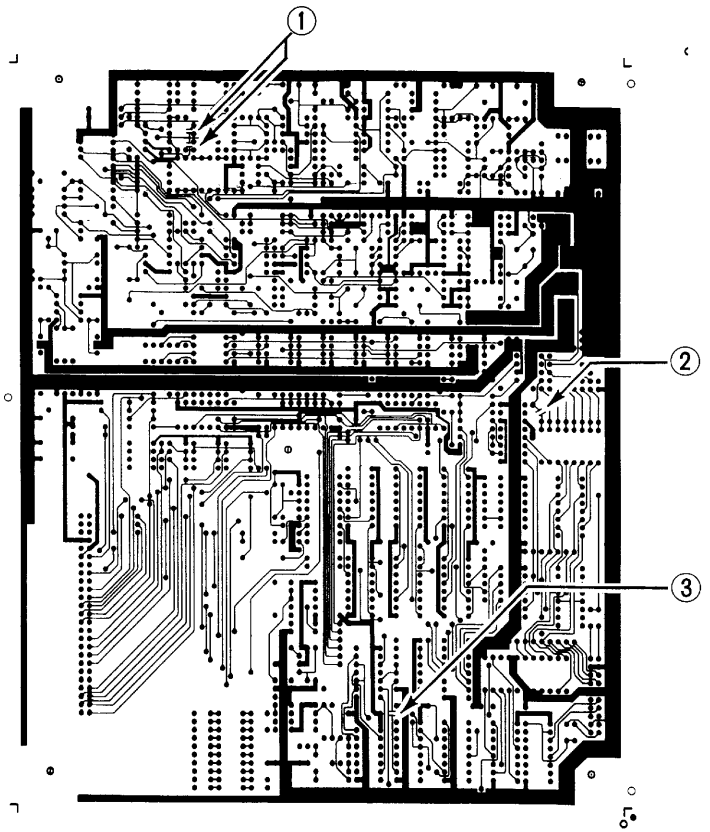
MODULE BOARD OPH124

SN 030100-090599 (pcb 052H270 or 052H270)





PATTERN-CUTS ON MOD CON



PATTERN-CUTS & SURFACE-MOUNTINGS ON MOD CON