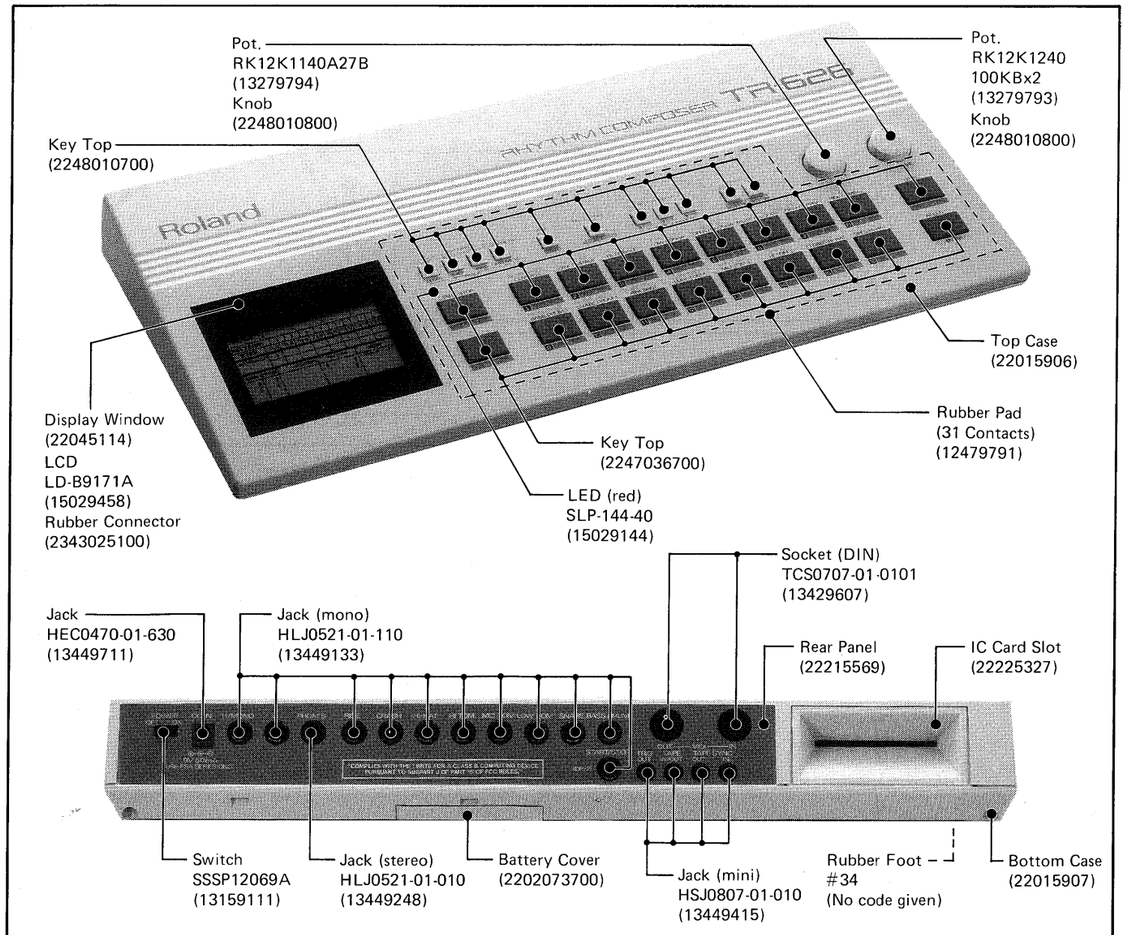
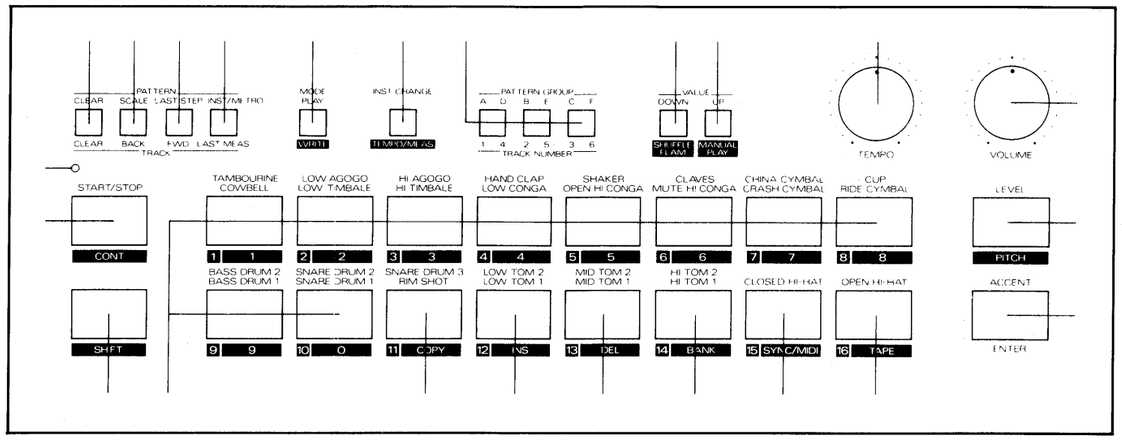
TR-626 SERVICE NOTES *First Edition*

SPECIFICATIONS

Memory Capacity	: 48 Preset Rhythm Patterns (Pattern Group A, B & C, each 16 patterns) 48 User's Programmable Rhythm Patterns (Pattern Group D, E & F, each 16 patterns)
Track	: 6 (999 measures max. in total)
Step	: 1 to 16 / measure
Tempo	: ♩=40–240
Output	: 6.0Vpp max. (Mono OUT) 2.0Vpp max. (Individual OUT)
Noise Level	: Less than –78dBm IHF-A
Trigger Out	: +5V, Approx. 18ms pulse (Rim Shot)
Tape In/Out	: 600 baud
Tape Sync Out	: –7dBm
Power Source	: 9V DC dry cell (UM-3) 6 pcs or AC Adapter BOSS PSA series
Current Draw	: 50mA DC at 9V
Power Consumption	: 450mW
Battery Life Expectancy	: Approx. 16 hours (UM-3)
Dimensions	: 400 (W) x 194 (D) x 56 (H) mm 15-3/4 x 7-5/8 x 2-3/16 in.
Weight	: 1.3 kg/2 lb. 14 oz. (including dry cells)
Accessories	: Connection Cable II-250 Dry cell SUM-3 6 pcs.
Options	: AC Adapter BOSS PSA series Pedal Switch DP-2 Memory Card M-128D (RAM 16K bytes)





CHANGE INFORMATION

CPU IC5 Main Board

Three CPU's as of the date of this manual
Differences among them are as listed below

Since the updated newest CPU is upward compatible from the predecessors, it is a preferable replacement.

	Name	Part No.	Serial No.	Type	Change
1	HD63701Y0P	15179270	up to 800199	w/internal one time PROM	
2		15179268	820200-823199		Program:See description below.
3	HD6301Y0D09P	15179271	823200-up	w/internal MASK ROM	Type of internal ROM (program is the same as in 15179268) (プログラムは15179268と同じ)

Improvements On The CPU Program
(2 and 3 in the above list)

* Decrease flickering in tempo indication on the LCD.

* Implement the following features.

  Transmit/receive MIDI Exclusive message.

  Transmit a song position pointer when a measure in the ongoing track is directly specified from the main key.

変更案内

ＣＰＵ ＩＣ５ メインボード

本サービスノート発行時点で、下表の通り３種類のＣＰＵが使用されています。

表中３のＣＰＵは、上位コンパチブルなので、補修用には３のＣＰＵを使用して下さい。

プログラム改良点
（上記２および３）

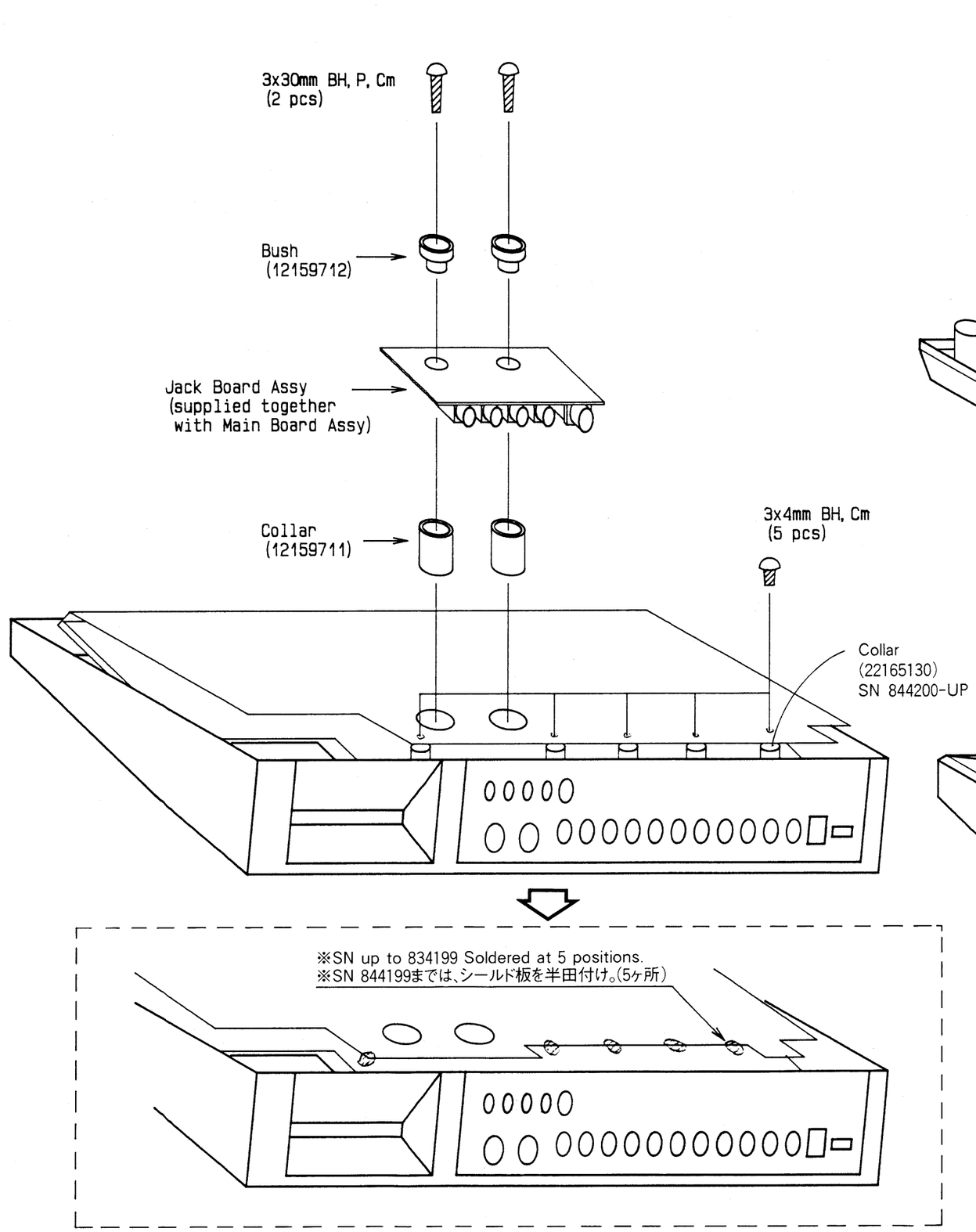
＊ ＬＣＤ上のテンポ表示のチラツキ軽減。

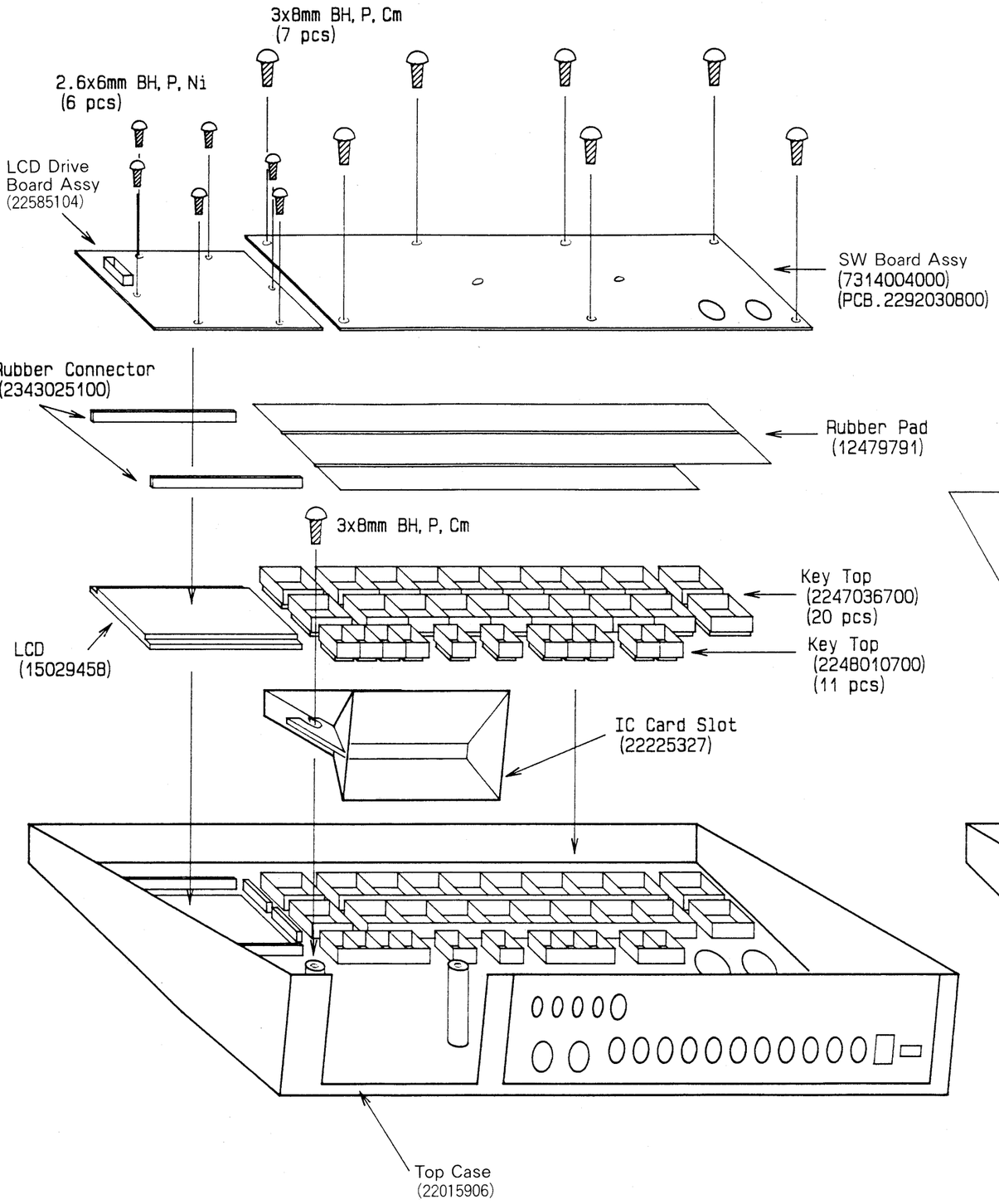
＊ 下記の機能を追加

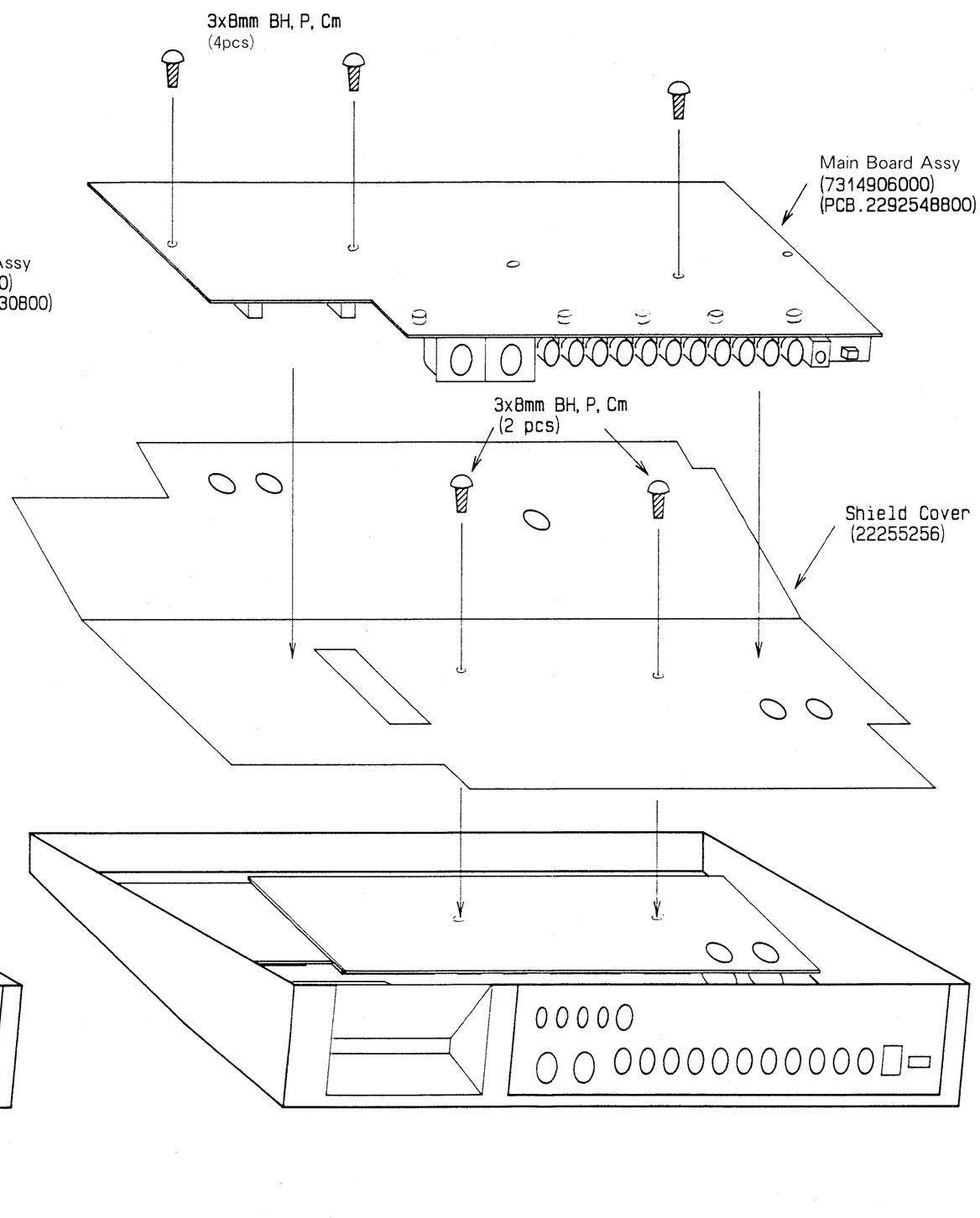
MIDI Exclusive メッセージを送受信する。

トラック中の小節がメインキーにより直接指定された場合、ソングポジションポインタを送信する。

EXPLODED VIEW 分解図




3x8mm BH, P, Cm
(7 pcs)
2.6x6mm BH, P, Ni
(6 pcs)
LCD Drive
Board Assy
(22585104)
SW Board Assy
(7314004000)
(PCB.2292030800)
Rubber Connector
(2343025100)
Rubber Pad
(12479791)
3x8mm BH, P, Cm
Key Top
(2247036700)
(20 pcs)
Key Top
(2248010700)
(11 pcs)
LCD
(15029458)
IC Card Slot
(22225327)
Top Case
(22015906)


3x8mm BH, P, Cm
(4pcs)
Main Board Assy
(7314906000)
(PCB.2292548800)
3x8mm BH, P, Cm
(2 pcs)
Shield Cover
(22255256)

PARTS LIST パーツ・リスト

CASING ケース

22015906	Top Case	トップケース
22015907	Bottom Case	ボトムケース
2202073700	Battery Cover	電池カバー
23425811	Battery Compartment Assy (including the following 4 parts)	電池ボックス完成品 (下記4点を含む)
2202073900	Compartment	電池ボックス
2345015500	Terminal Plate (+)	端子板
2345015600	Terminal Spring (-)	端子板
----------	Connector 4p w/leads	リード付コネクタ
22215569	Rear Panel	リアパネル
22225327	IC Card Slot	ICカード エスカッション
22045114	Display Window	LCD窓

KNOB, BUTTON シャツ,ボタン

2247036700	Key Top (large)	モールド ツマミ(大)
2248010700	Key Top (small)	モールド ツマミ(小)
2248010800	Knob	丸ツマミ

PCB ASSY 基板完成品

7314906000	Main Board (pcb 22925488 1/2)	メイン基板
	Including Jack Board	ジャック基板を含む
7314905000	Jack Board (pcb 22925488 2/2)	ジャック基板
7314004000	Switch Board (pcb 22920308) (Common to TR-505)	スイッチ基板
22585104	LCD Drive Board Assy	LCDドライブ基板

No replacement for individual parts on LCD Drive Board, including pcb and IC.
LCDドライブ基板の単独部品(IC,基板等)に対する補修品は用意されておりません。

JACK ジャック

13429607	TCS0707-01-0101	DIN	MIDI IN, MIDI OUT
13449711	HEC0470-01-630		DC IN
13449415	HSJ0807-01-010	mini	TRIG OUT, TAPE IN/OUT TAPE SYNCHRO IN/OUT
13449248	HLJ0521-01-010	stereo	PHONES
13449133	HLJ0521-01-110	monaural	START/STOP, R/MONO, L RIDE, CRASH, HI-HAT HI TOM, MID TOM, LOW TOM SNARE, BASS DRUM

POTENTIOMETER ボリューム

13279793	RK12K1240 100KBx2	VOLUME
13279794	RK12K1140A27B	TEMPO

SWITCH スイッチ

12479791	Rubber Pad		ゴムスイッチ
13159111	SSSP12069A	slide	スライドスイッチ

CONNECTOR コネクター

13439402	IL-S-4P-S2UX2-E	4p	Main Board
13439351	IL-S-6P-S2L2-EF	6p	Jack Board
13439297	IL-S-8P-S2T2-EF	8p	Switch Board
13439321	MOLEX 5124-03BHPB	3p	Switch Board
13429191	75080920	34p	Memory Card
2343025100	Rubber Connector		LCD

CERAMIC RESONATOR 発振子

12389729	CSA4.00MG	4.0MHz
12389809	CST6.40MT	6.4MHz

LCD 液晶表示器

15029458	LD-B9171A

IC

15179268 or (15179270)			
	HD63701Y0P	ZTAT CPU (w/one time PROM)	
or			
15179271	HD6301Y0D09P	(w/MASK ROM)	
	Containing the same program, (exclusive to TR-626), 15179268 and 271 are compatible with each other. See "CHANGE INFORMATION". Replacement CPU will be 271 only.		
	プログラムバージョンが同じなので、15179268と271は互換性 があります。「変更案内」参照。補修品は271が供給されます。		
15179846	μPD23C2001C	MASK ROM (SOUND)	IC15
15179378	MB8464A-15LL-SK	CMOS S-RAM	IC2
15229825	MB63H114PF	gate array multiple address counter	IC14
15229880	MB671189PF	gate array	IC13
15229881	μPD65006GF-198	gate array	IC1
15229867	BU3904S R11-0001	custom IC FSK MOD/DEMOD	IC10
15159113T0	TC4051BP	CMOS single 8-channel multiplexer	
15159116B0	M4069UBP	CMOS hex inverter	
15159129H0	HD14053BP	CMOS triple 2-channel multiplexer	
15169512X0	SN74HCU04	H-CMOS hex inverter	
15169515X0	SN74HC00	H-CMOS quad 2-input NAND gate	
15169571X0	SN74HC238	H-CMOS 3-to-8 line decoder	
15189136	M5218L	Op amp	
15189194	BA6993	comparator	
15219187	M51958AL	reset IC	
15229712	PC-900	optoisolator	

TRANSISTOR トランジスタ

15129602	2SD-667C	NPN
15129612	2SD-1469R	NPN
15129154	DTA-144EA	
15129181	DTC-144TF	

DIODE ダイオード

15019125	1SS-133		
15019209T0	S-5500G	rectifier	整流器
15019413D0	MTZ5.1B-T77	5.1V zener	ツェナー
15019509	MTZ5.6C	5.6V zener	ツェナー
15029144	SLP-144-40	LED red	赤

INDUCTOR コイル

12449272	GM50510152	filter bead inductor
12449266	BL01RN1-A62	ferrite bead inductor

RESISTOR ARRAY 抵抗アレイ

13919118	RGSD16L104G	ladder network	DAC
13910107	RGLD 8x332J		

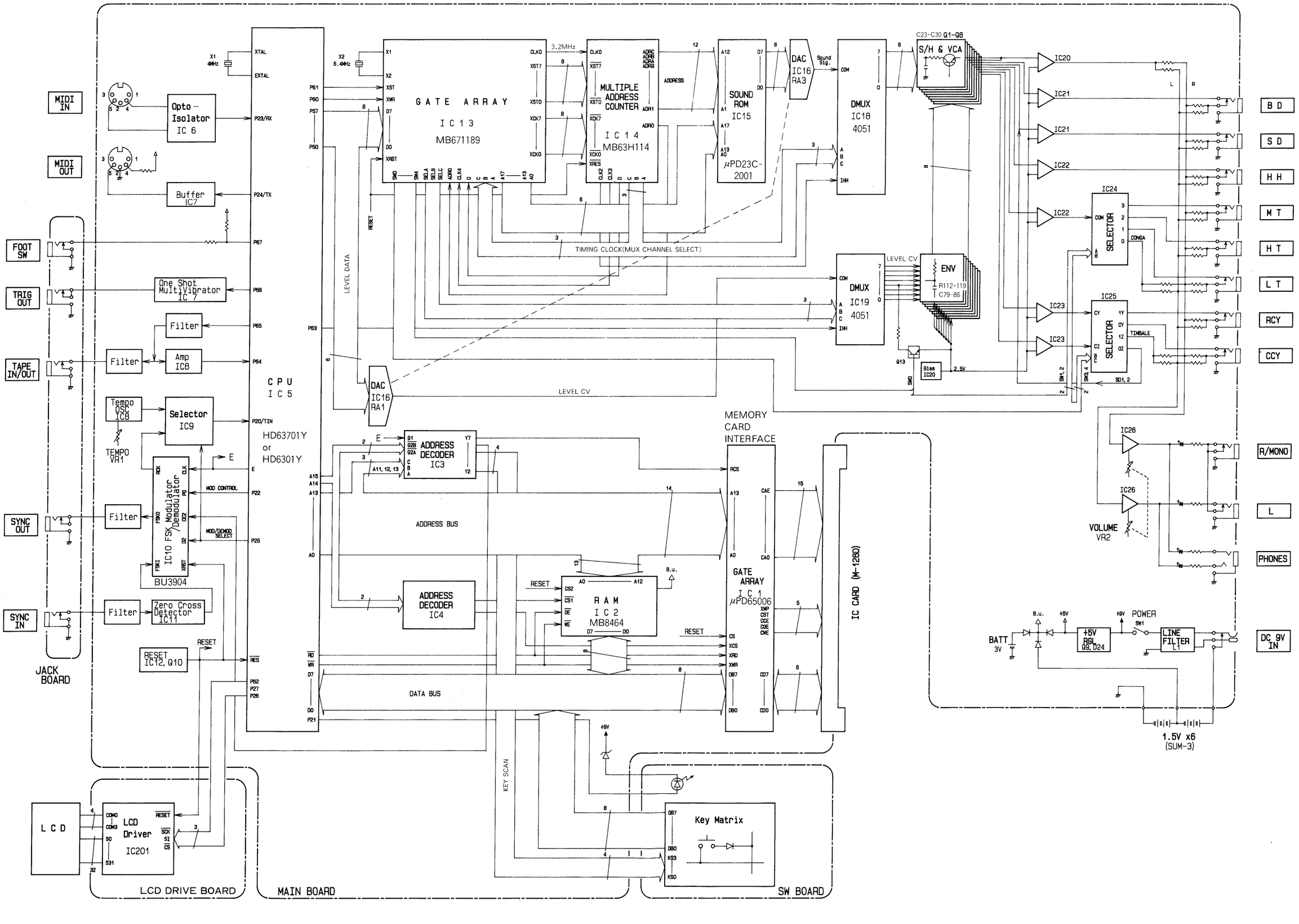
WIRING ASSY ワイアリング完

23495604	6P, 7P, 8P	main board

MISCELLANEOUS その他

13629141	Capacitor	Philips 122.5109 10μF 16V		
13549128	Capacitor	0.082μF 50vj ±5% Mylar		
12569255	Lithium Battery	M2B-C200 3V	リチウム電池	
12569105	Dry Cell	SUM-3S 1.5V	単三乾電池	
--------	Rubber Foot #34		ゴム足	
22255256	Shield Cover		シールド板	
22165130	Collar	PB-1-S	カラー(スペーサ)	shield cover
12159711	Collar	NA-315	カラー(スペーサ)	jack board
12159712	Bushing	NB-300	ブッシュ	jack board

BLOCK DIAGRAM



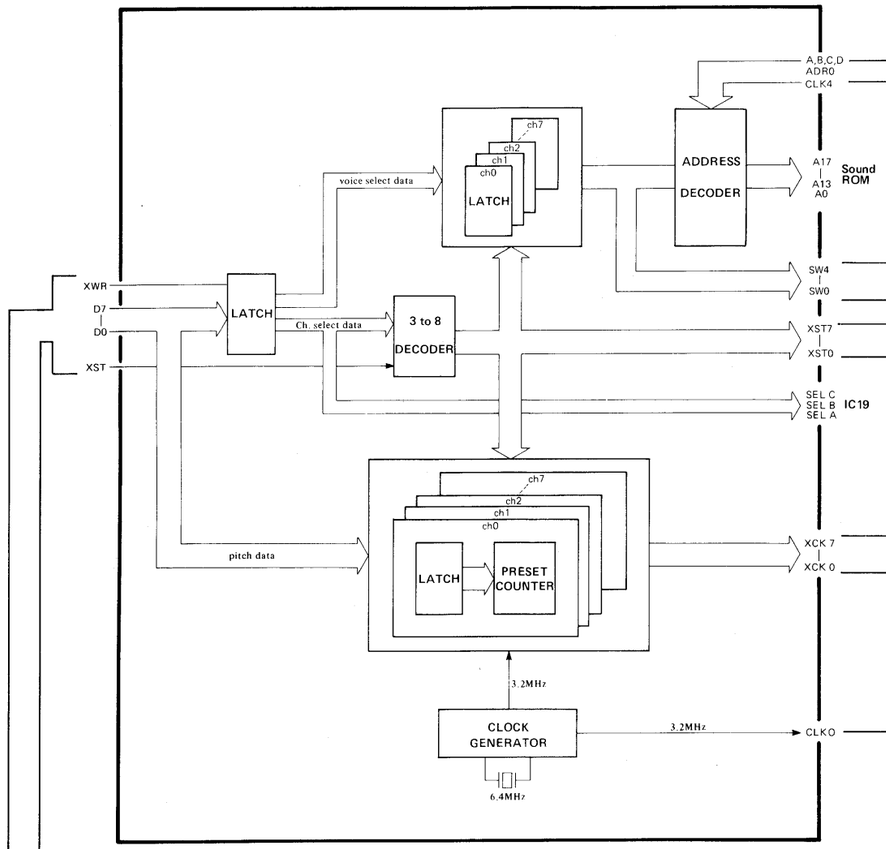


Fig. 1 IC13 MB671189 BLOCK DIAGRAM

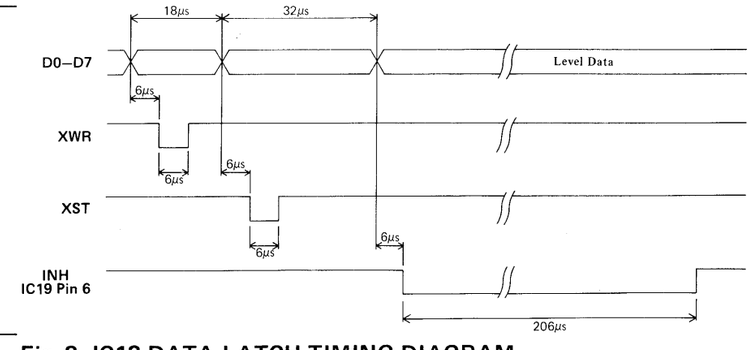


Fig. 2 IC13 DATA LATCH TIMING DIAGRAM

(CLK3)

SW	"L"	"H"
0	Open Hi-Hat	Closed Hi-Hat
1	Hi Tom 1, 2 Low Conga, Open Hi Conga	Low Tom 1, 2 Mid Tom 1, 2
2	Low Tom 1, 2 Low Conga, Open Hi Conga	Hi Tom 1, 2 Mid Tom 1, 2
3	Crash Cymbal China Cymbal	Ride Cymbal Cup
4	Snare Dram 1, 2	Low Timbale, Hi Timbale

Fig. 3 OUTPUT CHANNEL SELECT

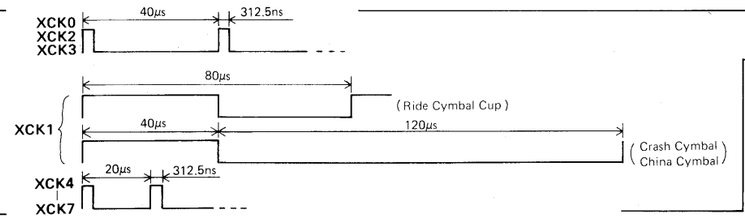
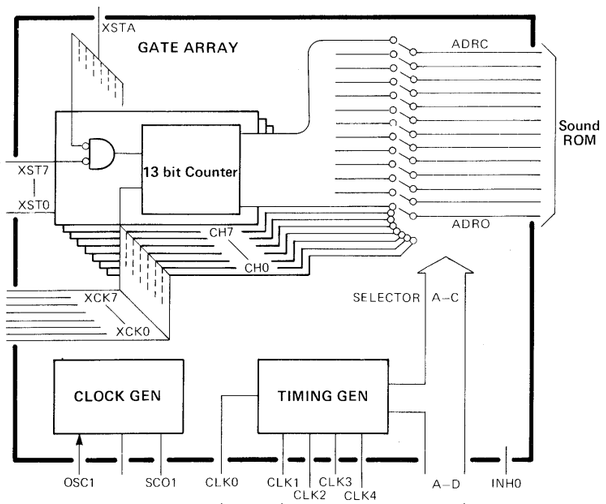


Fig. 4 ADDRESS COUNTER CLOCK PULSES (Pitch at zero)

Fig. 5 GATE ARRAY MB63H114 Multiple Address Counter



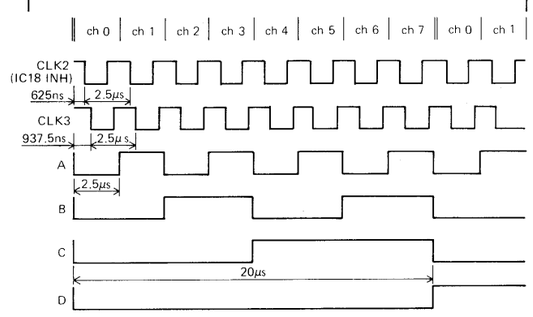


Fig. 6 MULTIPLEXING TIMING DIAGRAM

Table 2 SOUND ROM ADDRESS MAP

ch	voice	A0	A1 – A12	A13	A14	A15	A16	A17	Bytes
0	SD1	AD0	AD1 – AD12	0	1	1	1	0	8K
	SD2	AD0	AD1 – AD12	1	1	1	1	0	8K
	LTB	AD0	AD1 – AD12	0	1	1	1	1	8K
	HTB	AD0	AD1 – AD12	1	1	1	1	1	8K
1	CCY	AD0	AD1 – AD12	AD(-2)	AD(-1)	0	1	0	32K
	RCY	AD0	AD1 – AD12	AD(-1)	0	1	1	0	16K
	CHY	AD0	AD1 – AD12	AD(-2)	AD(-1)	0	1	1	32K
	CUP	AD0	AD1 – AD12	AD(-1)	0	1	1	1	16K
2	O.HCG	AD0	AD1 – AD12	0	0	0	0	0	8K
	LT1	AD0	AD1 – AD12	1	0	0	0	0	8K
	HT1	AD0	AD1 – AD12	0	1	0	0	0	8K
	MT1	AD0	AD1 – AD12	1	1	0	0	0	8K
	LCG	AD0	AD1 – AD12	0	0	0	0	1	8K
	LT2	AD0	AD1 – AD12	1	0	0	0	1	8K
	HT2	AD0	AD1 – AD12	0	1	0	0	1	8K
	MT2	AD0	AD1 – AD12	1	1	0	0	1	8K
3	OHH	AD0	AD1 – AD12	1	1	1	0	0	8K
	CHH	AD0	AD1 – AD12	1	1	1	0	1	8K
4	RIM	0	AD1 – AD12	0	1	1	0	0	4K
	SD3	0	AD1 – AD12	0	1	1	0	1	4K
5	BD1	1	AD1 – AD12	0	1	1	0	0	4K
	BD2	1	AD1 – AD12	0	1	1	0	1	4K
6	HCP	0	AD1 – AD12	0	0	1	0	0	4K
	CLAVES	0	AD1 – AD12	1	0	1	0	0	4K
	M.HCG	0	AD1 – AD12	0	0	1	0	1	4K
	SHAKER	0	AD1 – AD12	1	0	1	0	1	4K
7	CB	1	AD1 – AD12	0	0	1	0	0	4K
	TA MB.	1	AD1 – AD12	1	0	1	0	0	4K
	L AGOGO	1	AD1 – AD12	0	0	1	0	1	4K
	H AGOGO	1	AD1 – AD12	1	0	1	0	1	4K

Table 1 SOUND LOCATION

ch	Voice		Bytes
0	Snare Drum 1 Snare Drum 2	Low Timbale Hi Timbale	8K
1	Crash Cymbal Ride Cymbal	China Cymbal Cup	32K 16K
2	Open Hi Conga Low Tom 1 Mid Tom 1 Hi Tom 1	Low Conga Low Tom 2 Mid Tom 2 Hi Tom 2	8K
3	Open Hi-Hat	Closed Hi-Hat	8K
4	Rim Shot	Snare Drum 3	4K
5	Bass Drum 1	Bass Drum 2	4K
6	Hand Clap Claves	Mute Hi Conga Shaker	4K
7	Cowbell Tambourine	Low Agogo Hi Agogo	4K

CIRCUIT DESCRIPTIONS

GENERAL

The TR-626 is a multiple-sound rhythm machine that reproduces up to 8 rhythm voices simultaneously by reading multi sound (waveform) data, in time-division format, stoted in the sound ROM.

These sound data in the sound ROM (IC15) are called by addresses generated in the 8-channel address counter (IC14) in sequence; converted into analog equivalent at DAC (IC16, RA3) output; delivered to S/H circuits through demultiplexing and then given the suitable contour at VCA by envelope generator outputs.
With the TR-626 the pitch of a rhythm sound can be shifted by changing addressing speed, i.e. time interval of a counter clock (XCK0–XCK7) to the multi-address counter IC14. The new Roland custom gate array MB671189PF (IC13) generates variable counter clocks as well as upper address bits needed to access a 2 Mbyte ROM.
The very basic circuit concept of multi-addressing system already apeared in Roland TR-707 and TR-505. Those discrete circuit components generating upper address bits are incorporated in one chip (MB671189PF) on the TR-626.
Since this section of the description skips some basic functions of the multi-address counter (only shows block diagram and pin configuration), readers not familiar with multi-address counter are encouraged to read the detailed description on the TR-707 and TR-505 service notes.

DETAIL

1. Gate Array MB671189PF (IC13, Main Board)

The gate array features the following three major functions:

. Generates address counter (IC14) start pulses (XST0–XST7)
. Decodes sound ROM (IC15) addresses
. Generates address counter (IC14) clocks (XCK0–XCK7)

When a rhythm starts, the CPU IC5 places on P50 – P57 the data specifying sound channel to be activated and a sound in the channel. The data are latched into the gate array IC13 on an L to H transition of XWR and sent to DMUX IC19 as a channel select code (SELs A, B and C). The IC19, in turn, passes a level CV onto the envelope generator in the correct channel. The next data from the CPU determines the pitch of the sound and is held by the CPU until latched by a counter start pulse (XST0 – XST7) described below.

回路解説

概要

ＴＲ－６２６はマルチプル音源方式のリズムマシンです。音源ＲＯＭ（ＩＣ１５）に記憶されている複数の音源（波形）データを８チャンネルのアドレスカウンタ（ＩＣ１４）で順次読み出し（時分割）、ＤＡＣ（ＩＣ１６，ＲＡ３）でアナログ電圧に変換、デマルチプレクス回路で指定のＳ／Ｈ回路に入力し、サンプル／ホールドし、これに楽器の種類に応じたエンベロープを与えます。
ＴＲ－６２６では音源データの読み出しスピード（アドレス）を変えることにより、ピッチを変化させることが出来ます。このためにはマルチアドレスカウンタ（ＩＣ１４）のカウンタクロック（ＸＣＫ０～ＸＣＫ７）の周期を可変にする必要があります。ゲートアレイ ＩＣ１３ （ＭＢ６７１１８９ＰＦ）は、可変周期のクロックを生成するとともに、２Ｍビットの音源データを読み出すための上位アドレスも生成します。
マルチプル音源方式はＴＲ－７０７、ＴＲ－５０５等で採用されているものと基本的には同じですが、ディスクリートで組まれていた上位アドレス生成回路がＴＲ－６２６ではゲートアレイ ＩＣ１３ に内蔵されています。したがって、本解説で不明な点についてはＴＲ－５０５のサービスノートも参照して下さい。（アドレスカウンタ ＩＣ１４ の詳細は本解説では省略していますが、ＴＲ－５０５では詳しく説明されています。）

詳細

1.ゲートアレイ MB671189PF (IC13, メインボード)

主な機能は次の三つです。

・アドレスカウンタ（ＩＣ１４）スタート用パルスの発生（ＸＳＴ０～ＸＳＴ７）
・音源ＲＯＭ（ＩＣ１５）用のアドレスデコーダ（Ａ０，Ａ１３～Ａ１７）
・アドレスカウンタ用のカウンタクロッグの発生（ＸＣＫ０～ＸＣＫ７）

ＣＰＵ（ＩＣ５）から発音すべき音源チャンネルおよび、そのチャンネル内の音源を指定するデータがＰ５０～Ｐ５７を通じてＤ０～Ｄ７へ送られて来ます。
これらのデータは、ＸＷＲのＬからＨへの立上りでラッチされ、このうち音源チャンネルを指定するコードはチャンネルセレクト信号（ＳＥＬＡ，Ｂ，Ｃ）としてＤＭＵＸＩＣ１９へ送られます。ＩＣ１９は、このコードに応じて、レベルＣＶを指定のチャンネルのエンベロープ発生回路へ出力します。
次に発生させる音源のピッチを指定するデータがＣＰＵから送られて来ますが、このデータは後述のカウンタスタートパルス（ＸＳＴ０～ＸＳＴ７）によってラッチされるので、それ迄はＣＰＵが出力し続けます。

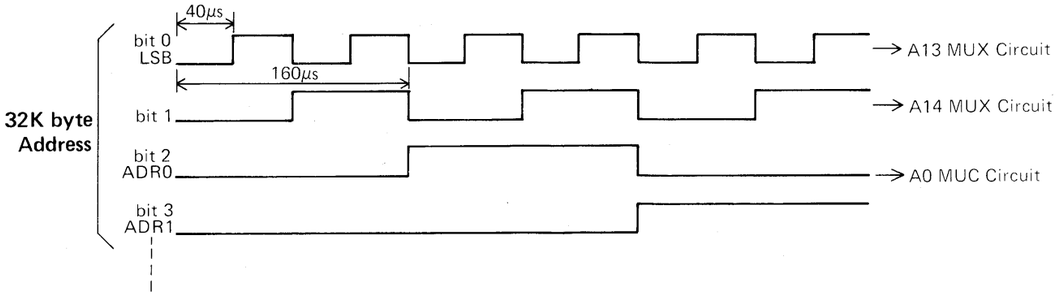
On an L to H transition of XST, the channel select signal being latched is made become a counter start pulse (XST0–XST7) of the selected channel by the 3-to-8 decoder. The counter start pulse also latches the pitch data and sound source select data into the correct channel.

2. Sound ROM (IC15) Address

The address bits A13 and A14 of channel 1 in Table 2 are somewhat defferent from those in other channels. The following description takes Crash Cymbal (CCY) address as an example.
To gain access to CCY's 32 kbyte memory location, 15 (2^{15} = 32K) address bits are required. The address must proceed at 40μs steps (when pitch shift is set at zero). The total bits the address counter can furnish are 13 bits: the remaining 2 bits must keep pace with the 13 bits.
Because the address counters are configured as non-free-running, they stop upon counting up all 1's which are equivalent to the address of the end location of an 8 kbyte memory space. To prolong the counter running time to cover all the 32 kbyte locations, the highest bit (ADRC) from the counter must be the 15th bit. That is, all counts (ADR0 – ADRC) are to be shifted up by 2 orders with respect to other channels. On the contrary, A13 and A14 address signals are shifted down to LSB (bit 0 and bit 1, respectively). The gate array IC13 generates bits 0 and 1 and applies them to the sound ROM IC15 as A13 and A14 when channel 1 is selected (Fig. 7).
The IC13 also feeds a clock whose interval is equal to bit 1 (160 μs with pitch set at 0) to channel 1 counter as the XCK1 (Fig. 4). Triggered on this XCK1, the channel 1 counter will deliver the count ADR0 as shown in Fig. 7, which is considered as bit 2 of the address system whose LSB (bit 0) steps at 40 μs interval.

NOTE:
ADR0 output from IC14 is indirectly applied to the sound ROM via IC13. The A0 column in Table 2 indicates that ADR0 must be at fixed level, 1 or 0 for channels 4–7. The IC13 selects a level according to channel selected before sending ADR0 to the sound ROM.

Fig. 7 CCY ADDRESS



ＸＳＴが“Ｌ”から“Ｈ”になると、それ迄ラッチされていたチャンネルセレクト信号が３ to ８ デコーダによってデコードされ、該当するチャンネルのカウンタスタートパルス（ＸＳＴ０～ＸＳＴ７のうちのいずれか）となります。このスタートパルスは同時に、ピッチデータおよび既にラッチされている音源セレクトデータを該当チャンネルへラッチします。

2.サウンドROM (IC15) のアドレス

Ｔａｂｌｅ２のアドレスマップを見ると、チャンネル１のＡ１３，Ａ１４のアドレス信号が他のチャンネルと異なっています。これについてＣｒａｓｈ Ｃｙｍｂａｌ（ＣＣＹ）を例にとって説明します。
ＣＣＹの３２Ｋｂｙｔｅのメモリロケーションにアクセスするには、１５ビット（2^{15}＝３２Ｋ）のアドレスが４０μｓ 毎に（ピッチゼロの場合）順次進行せねばなりません。
一方アドレスカウンタの出力は１３ ビットですから、残り２ビットをカウンタに同期して生成せねばなりません。アドレスカウンタはフリーランニング方式ではないので、８Ｋｂｙｔｅ目でオール１となり停止してしまいます。カウンタのラン時間を拡張して３２Ｋｂｙｔｅ のメモリにアクセス出来るようにするには、カウンタの最上位ビットが１５ビット目となるよう各ビットを２桁シフトアップする必要があります。（代りにＡ１３，Ａ１４ アドレスを最下位ビットへ移行させる。）
ＴＲ－６２６ではビット０、ビット１をゲートアレイＩＣ１３で生成し、ＣＨ１のＡ１３，Ａ１４として音源ＲＯＭへ加えます。またＩＣ１３はビット１と同一周期のクロックをＸＣＫとしてアドレスカウンタのＣＨ１へ加えます（Ｆｉｇ４）。このクロックによるアドレスカウンタのＡＤＲ０出力はＦｉｇ７に示す如く１６０μｓ 毎に変化し（ピッチゼロの場合）、これはＬＳＢが４０μｓ 毎に変化するアドレス構成の３ビット目に相当します。

注. ＩＣ１４ のＡＤＲ０出力は直接ＲＯＭへ加えられず、ＩＣ１３を経由しています。これはＴａｂｌｅ ２のＡ０欄を見ると判る如く、チャンネル４～７では“０”または“１”に固定する必要があります。ＩＣ１３は、チャンネルに応じてＡ０ の状態を変えてからＲＯＭへ送り出します。

3. FSK MOD/DEMOD BU3904S (IC10, Main Board)

BU3904S is a Roland custom IC designed to function as an FSK modulator/demodulator. The function mode of IC10 is generally determined by a command applied to D0–D3. With the TR-626 only D2 is changed its status while D0, D1 and D3 are held at fixed level.

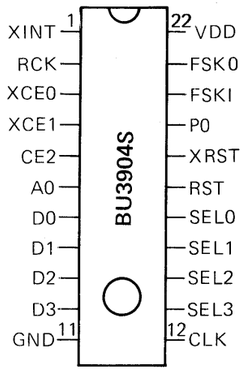
MOD = D2 "L" DEMOD = D2 "H"

During Modulation

Modulation is controlled by P0 input: FSK0 outputs 1.3 kHz at "L" P0 and 2.1kHz at "H" P0.

During Demodulation

RCK output changes the level according to signal frequency on FSKI. IC9 selects the RCK pulse instead of the tempo clock, as desired, and sends it to P20/TIN of the CPU.



Top View

Table 3 BU3904S FSK MOD/DEMOD

Name	Pin No.	I/O	Description
XINT	1	O	demodulation output (for interrupt), active low (NC)
RCK	2	O	demodulation clock output
XCE0	3	I	chip select, active low pulled down
XCE1	4	I	chip select, active low pulled down
CE2	5	I	chip select, active high
A0	6	I	data/command select "L" = command "H"= data pulled down
D0	7	I	data/command input pulled down
1	8	I	pulled down
2	9	I	L = MOD H = DEMOD
3	10	I	pulled up
GND	11	-	GND
CLK	12	I	clock input 1MHz
SEL3	13	I	clock select (1-8,10,12,14,16MHz) pulled up
2	14	I	pulled up
1	15	I	pulled up
0	16	I	pulled up
RST	17	I	reset, active high pulled down
XRST	18	I	reset, active low
P0	19	I	modulation control
FSKI	20	I	FSK signal input
FSKO	21	O	FSK signal output
V_{DD}	22	-	power supply +5V

3.FSK変調・復調 BU3904SCIC10, メインボード)

ＢＵ３９０４Ｓは、ＦＳＫ変調／復調用のカスタム ＩＣです。モード設定はＤ０～Ｄ３へ加えられるコマンドによって決まりますが、ＴＲ－６２６ではＤ０，Ｄ１，Ｄ３は固定とし、Ｄ２のみでコントロールします。

Ｄ２“Ｌ”＝変調、Ｄ２“Ｈ”＝復調

変調時

変調制御はＰ０入力によって行なわれＦＳＫ０の出力信号はＰ０“Ｌ”で1.3ＫＨｚ、“Ｈ”で2.1ＫＨｚとなります。

復調時

復調時には、ＦＳＫＩに入力されるＦＳＫ信号によって、ＲＣＫの出力が変化します。復調時ＩＣ９はテンポクロックの代わりにこのＲＣＫパルスをＣＰＵのＰ２０／ＴＩＮへ加えます。

4. Memory Card Interface μPD65006GF-198 (IC1, Main Board)

The gate array contains 3-state buffers. Inserting the memory card into the card socket pulls CST high.

When CST is high:

A0–A14 are transferred to CA0–CAE, respectively,
XWR (low active) to CWE (low active),
XRD (low active) to COE (low active) and
XCS (low active) to CCE (high active).

High CCE activates bidirectional buffers DB0–DB7 and CD0– CD7. Read/write is selected by XRD. Two chip select inputs are provided: XCS (low active) and CS (high active), but XCS only used in the TR-626. RCS (high active) and XRCS (low active) are used to detect the status of memory card. When they are made active, inputs are transferred:

XWP input (set position of protect switch – L = protect) to DB0
CST input to DB1
BATT input to DB2 (unused in the TR-626)

Switching to external bank enables the CPU to use RCS to read the status of the memory card.

During access to external memory (banks 2 and 3) the CPU checks the card at constant intervals.

4.メモリーカード・インターフェイス μPD65006GF-198 (IC1, メインボード)

本ゲートアレイには３ステートのバッファが内蔵されています。

メモリカードがソケットに挿入されると、ＣＳＴ端子が“Ｈ”となります。

ＣＳＴが“Ｈ”になると

ＡＯ～Ａ１４がＣＡＯ～ＣＡＥへ
ＸＷＲ（ローアクチブ）がＣＷＥ（ローアクチブ）へ
ＸＲＤ（ローアクチブ）がＣＯＥ（ローアクチブ）へ
ＸＣＳ（ローアクチブ）がＣＣＥ（ハイアクチブ）へ
それぞれ出力されます。

ＣＣＥが“Ｈ”になると双方向性のバッファＤＢ０～ＤＢ７およびＣＤ０～ＣＤ７がアクチブとなり、ＸＲＤの状態に応じてメモリカードへの書込みまたは、読み出しが可能となります。なお、チップセレクト入力には、ＸＣＳ（ローアクチブ）とＣＳ（ハイアクチブ）の２つがありますが、ＴＲ－６２６ではＸＣＳのみ使用しています。

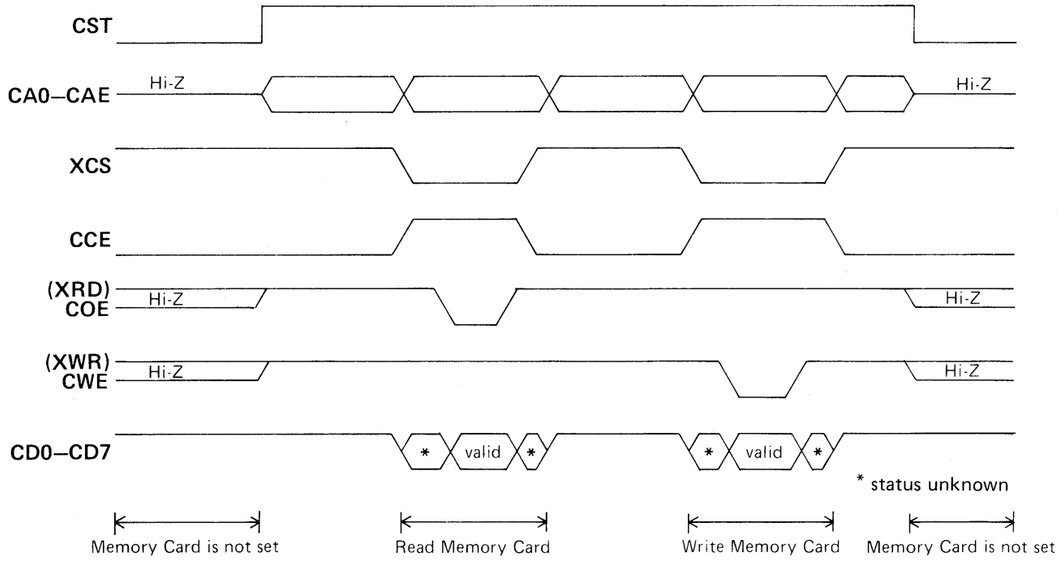
ＲＣＳ（ハイアクチブ）およびＸＲＣＳ（ローアクチブ）はメモリカードの状態検出用端子です。これらの端子がアクチブになると、

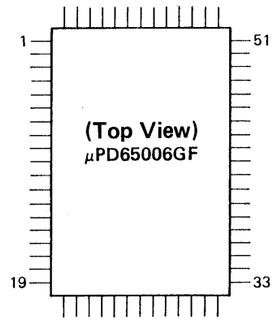
ＤＢ０にＸＷＰ（プロテクトＳＷの状態・・・・“Ｌ”プロテクト）
ＤＢ１にＣＳＴ
ＤＢ２にＢＡＴＴ（ＴＲ－６２６では使用していない）

の入力がそれぞれ出力されます。

メモリが外部バンクに切替えられると、ＣＰＵはＲＣＳを使ってメモリカードの状態を読み込みチェックします。また外部メモリ（バンク２，３）がアクセスされている時は、一定の間隔でカードの状態をくり返しチェックします。

Fig. 8 Memory Card Access Timing Chart





Gate Array μPD65006GF-198 IC1 Memory Card Interface

Name	Pin No.	I/O	Description
A0	40	I	address bus
1	42	I	
2	44	I	
3	46	I	
4	48	I	
5	50	I	
6	52	I	
7	53	I	
8	51	I	
9	49	I	
10	43	I	
11	47	I	
12	55	I	
13	29	I	
14	28	I	pulled down
RCS	31	I	read card status,active high
XRCS	32	I	read card status,active low (not used) pulled down
CS	57	I	chip select,active high
XCS	30	I	chip select,active low
XRD	45	I	read (or output enable),active low
XWR	54	I	write enable,active low
CST	2	I	CST (memory card)
XWP	15	I	WPOUT (memory card) memory card status
BATT	56	I	battery voltage detector pulled down
CA0	25	O	address bus
1	60	O	
2	61	O	
3	62	O	
4	63	O	
5	64	O	
6	24	O	
7	23	O	
8	22	O	
9	21	O	
A	20	O	
B	19	O	
C	18	O	
D	17	O	
E	16	O	
CCE	13	O	chip enable,active high
COE	12	O	output enable,active low
CWE	14	O	write enable,active low
DB0	41	I/O	data bus (to CPU)
1	39	I/O	
2	37	I/O	
3	35	I/O	
4	33	I/O	
5	34	I/O	
6	36	I/O	
7	38	I/O	
CD0	10	I/O	data bus (to memory card)
1	9	I/O	
2	8	I/O	
3	7	I/O	
4	6	I/O	
5	5	I/O	
6	4	I/O	
7	3	I/O	
GND	11	-	GND
GND	26	-	
GND	58	-	
V_{DD}	27	-	power supply,+5V
V_{DD}	59	-	
(NC)	1	-	(NC)

Memory Card M-128D (RAM 16K bytes)

Name	Pin No.	I/O	Description
Vcc	1	-	power supply, +5V
A0	2	I	address bus
1	3	I	
2	4	I	
3	5	I	
4	6	I	
5	7	I	
6	8	I	
7	9	I	
8	10	I	
9	11	I	
10	12	I	
11	13	I	
12	14	I	
13	15	I	
(NC)	16	-	(NC)
(NC)	17	-	
(NC)	18	-	
(NC)	19	-	
WPOUT	20	O	write protect switch status "L" = protect
WE	21	I	write enable active low
CE	22	I	chip enable active high
OE	23	I	output enable,active low
D0	24	I/O	data bus
1	25	I/O	
2	26	I/O	
3	27	I/O	
4	28	I/O	
5	29	I/O	
6	30	I/O	
7	31	I/O	
GND	32	-	GND
V_{BB}	33	O	back-up battery voltage output
CST	34	O	card status output, "H" = card enable

NOTES:

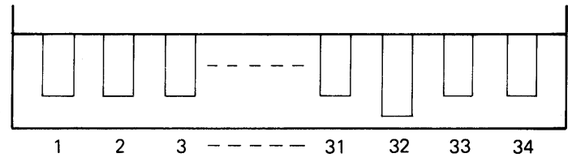
Pin 16 to which M-128D has no connection. However, the pin on the socket connects to CAE of IC1 and is pulled low. This provision is to make it possible to use another memory card M-256D for which pin 16 serves as A14.

Pin 33 The TR-626 does not check the voltage (VBB) on this pin.

CAUTION

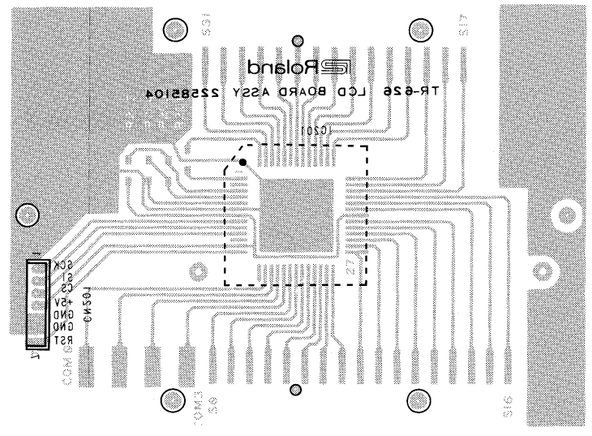
Pin 33 must be left open. Otherwise, the life expectancy of the battery in the memory card will be shortened.

注. 16番ピンはM－128Dでは（NC）ですが、M－256DではA14となります。そのためTR－626では、16番ピンをゲートアレイμPD65006GF－198に接続し、16番ピンが常に“L”になるようにしています。33番ピンV_{BB}はTR－626では使用していません。（PCB上のコネクタの33番ピンは（NC）になっています。）



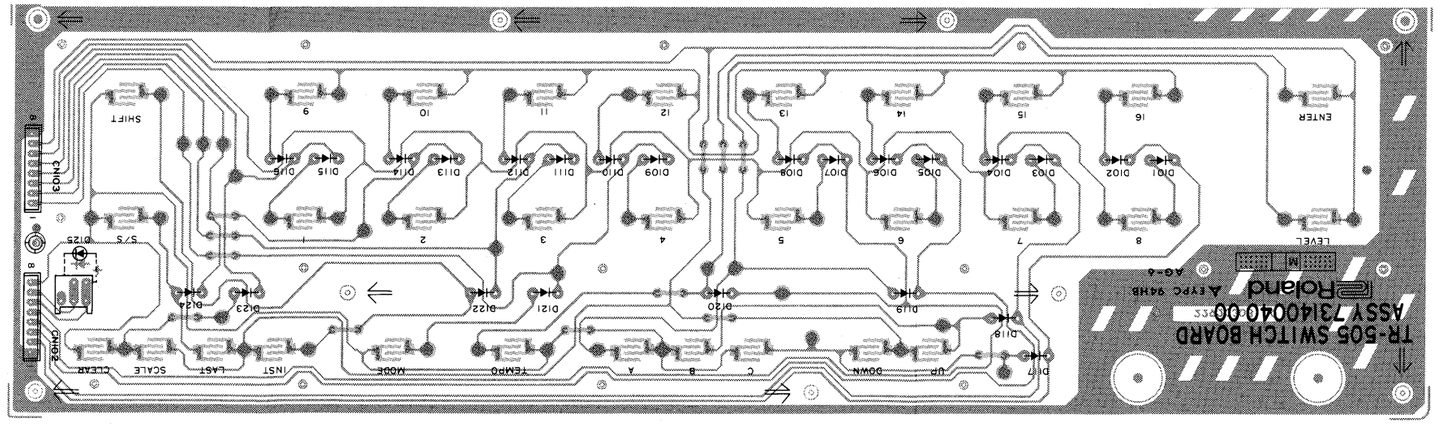
LCD Drive Board Assy 22585104

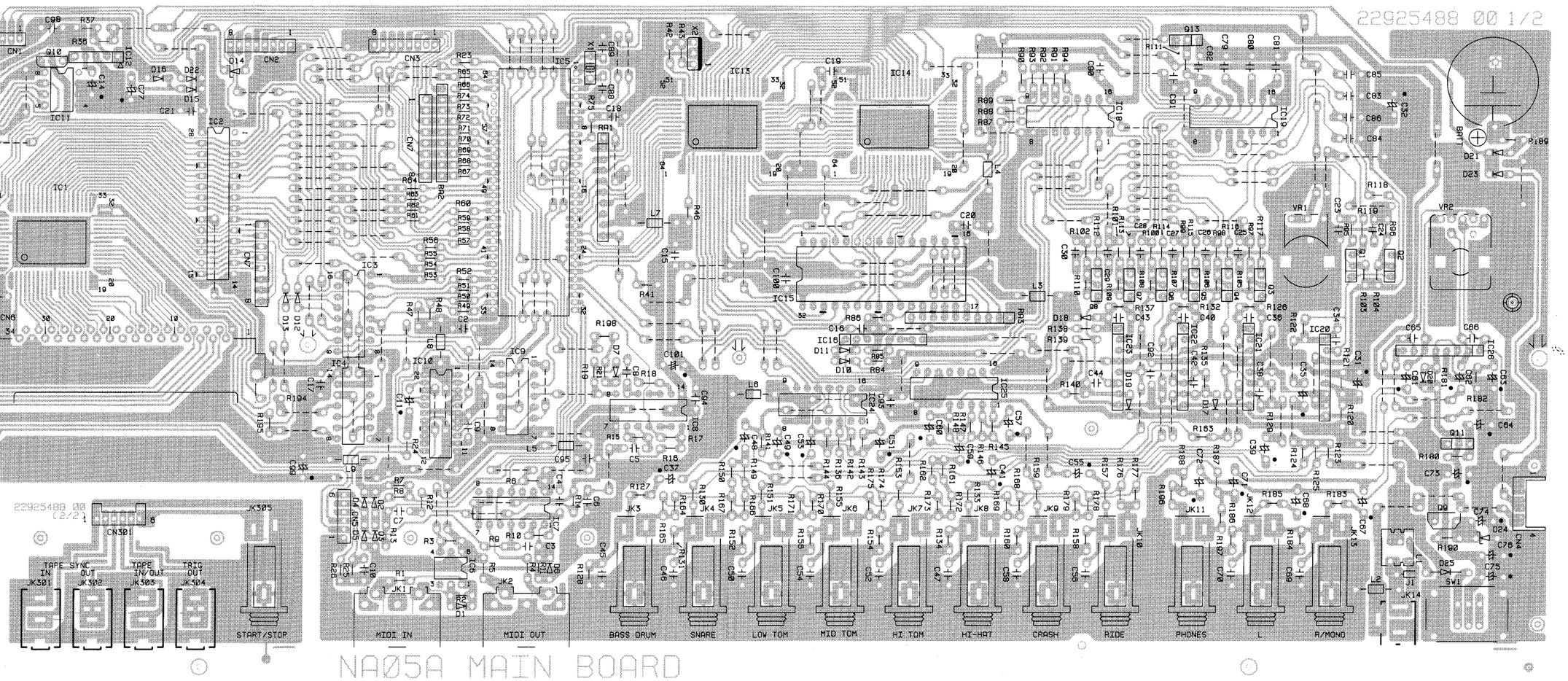
View from Foil side



Switch Board Assy 7314004000 (pcb 22920308)

Identical to switch board for TR-505
TR-505のスイッチ基板と同一





Jack Board
Assy 7314905000
(pcb 22925488 2/2)

Main board and Jack board Supplied in a set with Main board made representative.

メインボードとジャックボードは
セットで供給されます。
(メインボードが代表となります)

Main Board
Assy 7314906000
(pcb 22925488 1/2)

ADVARSEL!
Lithiumbatteri. Eksplosionsfare.
Udskiftning må kun foretages af en sagkyndig, og som beskrevet i servicemanual.

Lithium batteri må kun udskiftes med samme type og fabrikat.

VARNING!
Lithiumbatteri. Explosionsrisk.
Får endast bytas av behörig servicetekniker.
Se instruktioner i servicemanualen.

Lithium batteri för endast ersättes med samme typ och fabrikat.

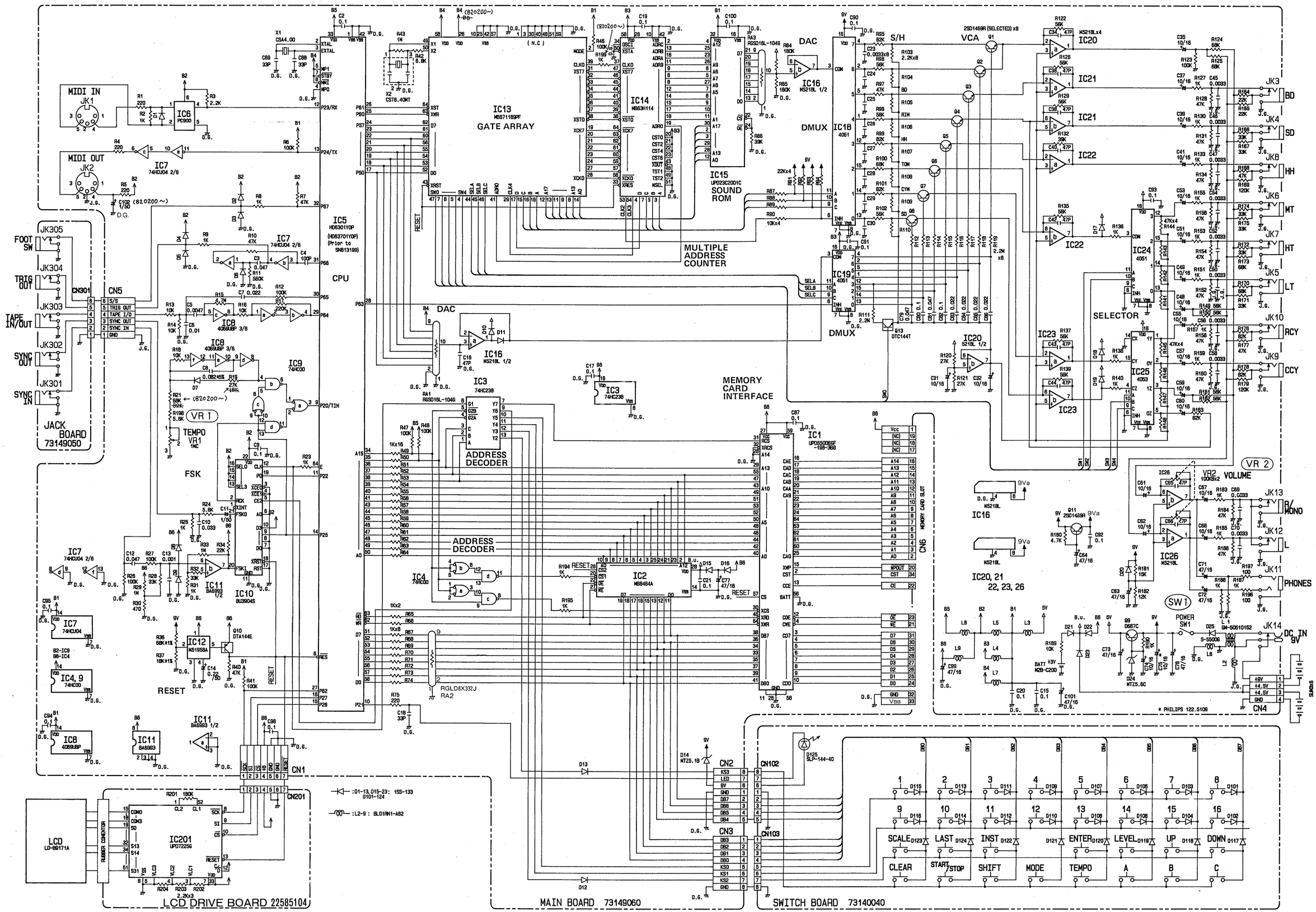
ADVARSEL!
Lithiumbatteri. Fare for eksplotion.
Må bare skiftes av kvalifisert tekniker som beskrevet i servicemanualen.

Lithium batteri må kun utskiftes med samme type og fabrikat.

VAROITUS!
Lithiumparisto. Räjähdysvaara.
Pariston saa vaihtaa ainoastaan alan ammottimies.

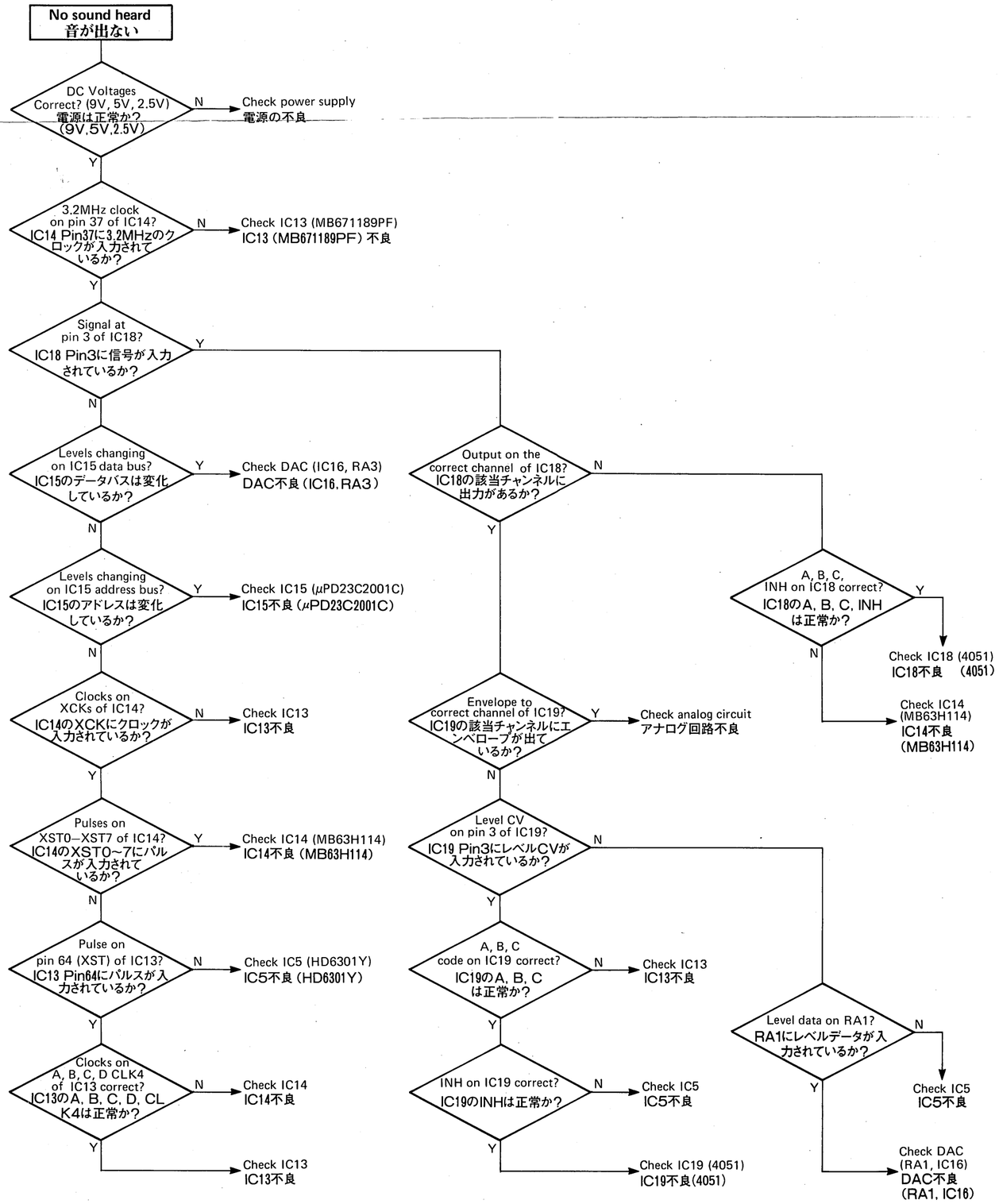
Kun vaihat lithium pariston KÄYTÄ saman valmistajan samaa tyyppiä.

CIRCUIT DIAGRAM

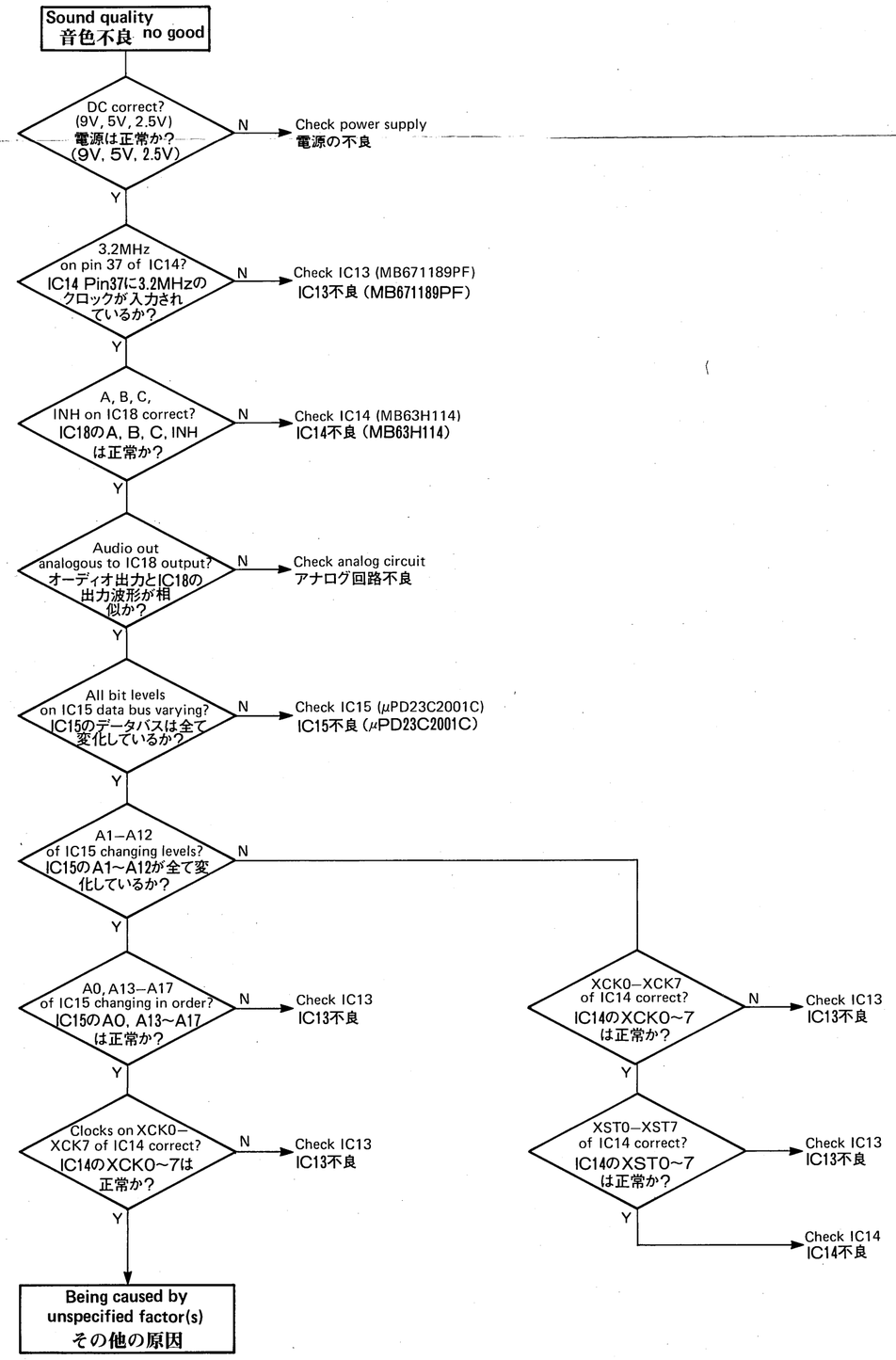


TROUBLESHOOTING LOGIC TREE トラブルシューティング例

ex.1)



ex.2)

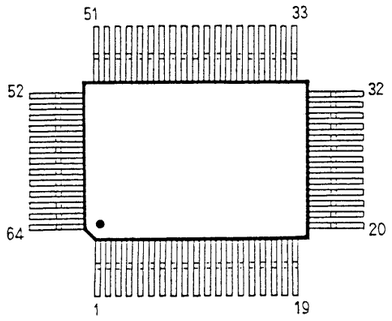


IC DATA

Gate Array MB63H114

Name	Pin No.	I/O	Description
CST0	20	I	continue start counter 0 — pulled up
2	21	I	continue start counter 2 — pulled up
4	22	I	continue start counter 4 — pulled up
6	23	I	continue start counter 6 — pulled up
XSTA	50	I	XST0 - XST7 enable — active low — pulled down
XST0	38	I	counter start counter 0 active low
1	39	I	counter start counter 1 active low
2	40	I	counter start counter 2 active low
3	41	I	counter start counter 3 active low
4	44	I	counter start counter 4 active low
5	45	I	counter start counter 5 active low
6	46	I	counter start counter 6 active low
7	47	I	counter start counter 7 active low
XCK0	56	I	counter clock input counter 0
1	57	I	counter clock input counter 1
2	59	I	counter clock input counter 2
3	60	I	counter clock input counter 3
4	61	I	counter clock input counter 4
5	62	I	counter clock input counter 5
6	63	I	counter clock input counter 6
7	64	I	counter clock input counter 7
XOUT	43	I	ADR0 - ADRC out enable — active low — pulled down
ADR0	19	O	ROM address
1	18	O	
2	17	O	
3	15	O	
4	14	O	
5	12	O	
6	8	O	
7	6	O	
8	9	O	
9	11	O	
A	16	O	
B	13	O	
C	2	O	
A	3	O	timing clock 200kHz (MUX DMUX channel select)
B	5	O	timing clock 100kHz
C	7	O	timing clock 50kHz
D	4	O	timing clock 25kHz
INH0	1	O	DMUX inhibit — (NC)
OSCI	34	I	X'tal terminals for — pulled down
SCO0	35	O	internal clock generator — (NC)
SC01	36	O	internal clock generator output — (NC)
CLK0	37	I	master clock input , 3.2MHz
CLK1	52	O	system clock 400kHz — (NC)
2	53	O	system clock 400kHz DMUX inhibit
3	54	O	system clock 400kHz timing clock for MB671189
4	55	O	system clock 400kHz — (NC)
XRES	33	I	reset,active low
MSEL	51	I	counter 12/13 bit select — pulled down
TST1	48	I	IC test — pulled down
TST2	49	I	IC test — pulled down
Vss	10	-	GND
Vss	42	-	GND
V_{DD}	26	-	power supply, +5V
V_{DD}	58	-	power supply, +5V
GAT0	32	O	counter gate output, "H" = counter running — (NC)
1	31	O	(NC)
2	30	O	(NC)
3	29	O	(NC)
4	28	O	(NC)
5	27	O	(NC)
6	25	O	(NC)
7	24	O	(NC)

Pin Configuration (Top View) **MB63H114 MB671189PF**



CHECKING IC14 MB63H114

The gate out pins GAT0 – GAT7 of IC14 will indicate the status of mated counter.
While a counter is running, its GAT pin stays high.

ゲートアレイ(IC14,MB63H114)良否判定のヒント

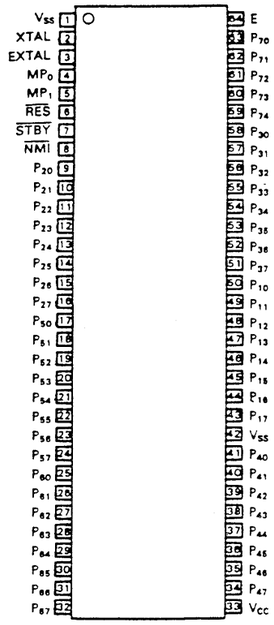
故障診断の際、ゲートアレイの良否を以下の方法で判定する事が出来ます。ゲートアレイのゲート（ＧＡＴ０－ＧＡＴ７）は対応したカウンタが走っている間、ハイとなります。

Gate Array MB671189PF

Name	Pin No.	I/O	Description
XWR	63	I	data latch pulse (for sound select) — active Low
XST	64	I	data latch pulse (for pitch) & counter start — active Low
D0	52	I	date input
1	53	I	
2	54	I	
3	55	I	
4	56	I	
5	60	I	
6	61	I	
7	62	I	
CLK4	29	I	timing clock
A	18	I	timing clock (MUX channel select)
B	16	I	timing clock
C	15	I	timing clock
D	17	I	timing clock
ADR0	41	I	multiple address counter bit 0 — to ROM address decoder
XCK0	38	O	counter start pulse counter 0
1	37	O	counter start pulse counter 1
2	36	O	counter start pulse counter 2
3	35	O	counter start pulse counter 3
4	34	O	counter start pulse counter 4
5	33	O	counter start pulse counter 5
6	32	O	counter start pulse counter 6
7	31	O	counter start pulse counter 7
XCK0	28	O	counter clock counter 0
1	27	O	counter clock counter 1
2	24	O	counter clock counter 2
3	23	O	counter clock counter 3
4	22	O	counter clock counter 4
5	21	O	counter clock counter 5
6	20	O	counter clock counter 6
7	19	O	counter clock counter 7
A 0	14	O	ROM address
A13	8	O	
14	9	O	
15	11	O	
16	13	O	
17	12	O	
SELA	44	O	level CV channel select
B	45	O	
C	46	O	
SW0	47	O	sound select "H" = Closed Hi-Hat "L" = Open Hi-Hat
1	7	O	sound select "H" = L.TOM, M.TOM "L" = H.TOM, Congas
2	6	O	sound select "H" = M.TOM, H.TOM "H" = L.TOM, Congas
3	5	O	sound select "H" = Ride,Cup "L" = Crash, China
4	4	O	sound select "H" = Timbales "L" = Snare Drum 1,2
MODE	2	I	mode select "H" = variable pitch "L" = fixed pitch — pulled up
XRST	43	I	reset,active low
X 1	49	I	X'tal terminals for internal clock generator, 6.4MHz
X 2	50	O	
CLKO	39	O	system clock output, 3.2MHz
Vss	10	-	GND
Vss	25	-	GND
Vss	42	-	GND
Vss	57	-	GND
V_{DD}	26	-	power supply,+5V
V_{DD}	58	-	power supply,+5V
(NC)	1	-	(NC) — pulled down
(NC)	3	-	(NC) — pulled down
(NC)	30	-	(NC) — pulled down
(NC)	40	-	(NC) — pulled down
(NC)	48	-	(NC) — pulled down
(NC)	51	-	(NC) — pulled down
(NC)	59	-	(NC) — pulled down

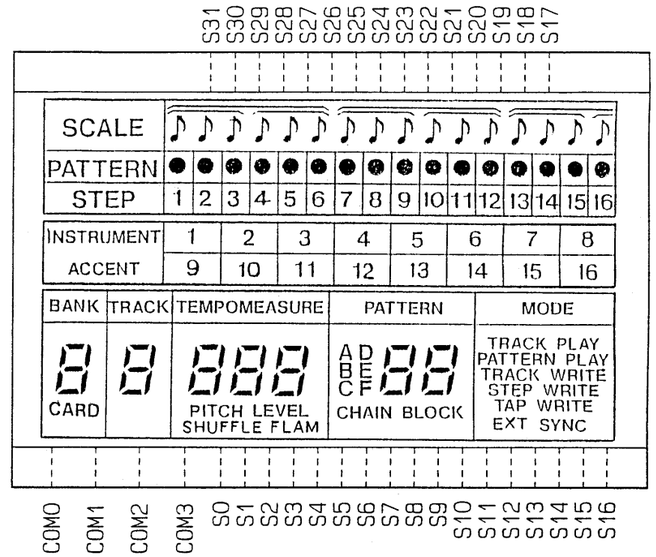
CPU HD6301Y0A99P
HD63701Y0P

Pin Configuration
(Top View)

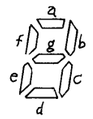


PIN NO.	PORT NAME	DESCRIPTION	
1	Vss	GND	
2	XTAL	terminal, Xtal	
3	EXTAL	terminal, Xtal	
4	MP0	input, Mode Setting, pulled down	
5	MP1	input, Mode Setting, pulled up +5V	
6	RES	input, Reset (active low)	
7	STBY	unused, pulled up +5V (active low)	
8	NMI	unused, pulled up +5V (active low)	
9	P20	input, TEMPO CLOCK	
10	P21	output, LED	
11	P22	output, FSK P0	
12	P23	input, MIDI IN	
13	P24	output, MIDI OUT	
14	P25	output, FSK D2	
15	P26	output, LCD CS	
16	P27	output, LCD SI	
17	P50	output, Sound Select Pitch Data	Level Data
18	P51		
19	P52		
20	P53		
21	P54		
22	P55		
23	P56		
24	P57		
25	P60	output, $\overline{XWR}$	
26	P61	output, $\overline{XST}$	
27	P62	output, LCD SCK	
28	P63	output, Level CV DMUX, INH	
29	P64	input, LOAD (TAPE)	
30	P65	output, SAVE (TAPE)	
31	P66	output, TRIG OUT	
32	P67	input, START/STOP	
33	Vcc	+5V power supply	
34	P47	output, Address Bus	A15
35	P46		A14
36	P45		A13
37	P44		A12
38	P43		A11
39	P42		A10
40	P41		A9
41	P40		A8
42	Vss	GND	
43	P17	output, Address Bus	A7
44	P16		A6
45	P15		A5
46	P14		A4
47	P13		A3
48	P12		A2
49	P11		A1
50	P10		A0
51	P37	input/output, Data Bus	D7
52	P36		D6
53	P35		D5
54	P34		D4
55	P33		D3
56	P32		D2
57	P31		D1
58	P30		D0
59	P74	unused	
60	P73	unused	
61	P72	unused	
62	P71	output, $\overline{WE}$	
63	P70	output, $\overline{RD}$	
64	E	output, system clock, 1MHz	

LCD LDB9171A



	COM 0	COM 1	COM 2	COM 3
S 0	7 seg #1 a	f	g	e
S 1	CARD	b	c	d
S 2	7 seg #2 a	f	g	e
S 3	TEMPO	b	c	d
S 4	7 seg #3 a	f	g	e
S 5	MEASURE	b	c	d
S 6	7 seg #4 a	f	g	e
S 7	PITCH	b	c	d
S 8	FLAM	---	---	SHUFFLE
S 9	7 seg #5 a	f	g	e
S10	LEVEL	b	c	d
S11	CHAIN	A	B	C
S12	PATTERN	D	E	F
S13	7 seg #6 a	f	g	e
S14	BLOCK	b	c	d
S15	7 seg #7 a	f	g	e
S16	PATTERN PLAY	b	c	d
S17	TRACK WRITE	STEP WRITE	TAP WRITE	EXT SYNC
S18	TRACK PLAY	(INST) 14	(INST) 15	(INST) 16
S19	(INST) 5	(INST) 6	(INST) 7	(INST) 8
S20	(STEP) 9	(STEP) 11	(STEP) 13	(STEP) 15
S21	(STEP) 10	(STEP) 12	(STEP) 14	(STEP) 16
S22	(DOT) 9	(DOT) 11	(DOT) 13	(DOT) 15
S23	(DOT) 10	(DOT) 12	(DOT) 14	(DOT) 16
S24	♩	♩	♪ ♪ ♪ ♪	♬ ♬ ♬ ♬
S25	(DOT) 7	(DOT) 5	(DOT) 3	(DOT) 1
S26	(DOT) 8	(DOT) 6	(DOT) 4	(DOT) 2
S27	(STEP) 7	(STEP) 5	(STEP) 3	(STEP) 1
S28	(STEP) 8	(STEP) 6	(STEP) 4	(STEP) 2
S29	(INST) 4	(INST) 3	(INST) 2	(INST) 1
S30	(INST) 12	(INST) 11	(INST) 10	(INST) 9
S31	(INST) 13	♩ ♩	ACCENT	INSTRUMENT



7 seg #* Arrangement 7segパターン配列
7 seg #1 : leftmost 7seg#1……左端
7 seg #7 : rightmost 7seg#7……右端

MIDI IMPLEMENTATION

[RHYTHM MACHINE] Date : Jul.23.1987
MODEL TR-626 MIDI Implementation Chart Version : 1.0

Function ...		Transmitted	Recognized	Remarks
Basic	Default	1-16	1-16	memorized
Channel	Changed	1-16	1-16	(non-volatile)
Mode	Default	Mode 3	Mode 1 OMNI ON/OFF	memorized (non-volatile)
	Messages			
	Altered	**********		
Note Number		25-99 *1	25-99 *1	assignable to each voice
	True voice	**********		
Velocity	Note ON	o 9n v=18-127	o 9b v=1-127	n=Inst CH *2 b=Basic CH
	Note OFF	x 9n v=0	x	
After Touch	Key's	x	x	
	Ch's	x	x	
Pitch Bender		x	x	
Control Change		x	x	
Prog Change		x	x	
	True #	**********		
System Exclusive		o	o	
System Common	Song Pos	o	o SYNC = MIDI	
	Song Sel	o	o SYNC = MIDI	
	Tune	x	x	
System Real Time	Clock	o	o SYNC = MIDI	
	Commands	o	o SYNC = MIDI	
Aux Mes-sages	Local ON/OFF	x	x	
	All Notes OFF	x	x	
	Active Sense	x	x	
	Reset	x	x	
Notes		*1 Can be changed by panel operation. *2 Transmit channel number of each voice can be changed to 1 to 16 by panel operation.		

Mode 1 : OMNI ON, POLY Mode 2 : OMNI ON, MONO o : Yes
Mode 3 : OMNI OFF, POLY Mode 4 : OMNI OFF, MONO x : No

RHYTHM MACHINE
MODEL TR-626 MIDI IMPLEMENTATION Version 1.0 Jul.24.1987

1. TRANSMITTED DATA

■ Note event

Note off

Status	Second	Third
9nH	kkH	00H

n = Transmit channel : 0H - FH (1 - 16)
kk = Note number :19H - 63H (25 - 99)

Note on

Status	Second	Third
9nH	kkH	vvH

kk = Note number :19H - 63H (25 - 99)
vv = Velocity :12H - 7FH (18 - 127)
Determined by Accent value: -3 to +3

Transmit channel for each voice can be set to any of 1 to 16 by panel operation.
Note number of each voice can be assigned to one of 25 to 99.
The above settings can be made by panel operation and are non-volatile.
The accent value (-3 to +3) written in a pattern determines the note velocity, overriding the volume level set internally.

Accent	Velocity
-3	12H
-2	19H
-1	23H
0	30H
+1	42H
+2	5BH
+3	7FH

■ System exclusive

Status

F0H :System Exclusive
F7H :EOX(End of Exclusive)

Refer to 3.EXCLUSIVE COMMUNICATIONS.

■ System common

Song Position Pointer

Status	Second	Third
F2H	llH	hhH

ll = Least significant :00H - 7FH (0 - 127)
hh = Most significant :00H - 7FH (0 - 127)

Sent whenever MEASURE FORWARD or MEASURE BACK is pressed, or a measure number is specified.

Song Select

Status	Second
F3H	ssH

ss = song select :00H - 05H (0 - 5)

Sent whenever the track is set to new track from the panel.
One each of the track numbers 1 to 6 corresponds to the song selects 0 to 5 in that order.

■ System Real Time

Timing Clock

Status

F8H

Sent even if the rythm is not running.

Start

Status

FAH

Sent upon pressing START for playing.

Continue

Status

FBH

Sent upon pressing CONTINUE START for re-running the rhythm.

Stop

Status

FCH

Sent whenever the rhythm is stopped.

When Sync mode is set at MIDI, the TR-626 sends(software through) the real time messages received from MIDI IN.

2. RECOGNIZED RECEIVE DATA

■ Channel mode message

OMNI OFF

Status	Second	Third
BbH	7CH	00H

OMNI ON

Status	Second	Third
BbH	7DH	00H

b = Basic channel : 0H - FH (1 - 16)

■ Note event

Note on

Status	Second	Third
9bH	kkH	vvH

b = Basic channel : 0H - FH (1 - 16)
kk = Note number :19H - 63H (25 - 99)
vv = Velocity :01H - 7FH (1 - 127)

The basic channel (receive channel) can be changed to 1-16 by panel operation. The Basic channel is non-volatile.
Assignment of a Note number to a voice is common to MIDI IN and MIDI OUT. Assignment can be independent of the remaining voices.
A MIDI IN note number will sound the voice to which it is assigned. The associated Velocity determines the volume of the voice, defeating the internal level setting.

■ System exclusive

Status	
F0H	:System Exclusive
F7H	:EOX(End of Exclusive)

Refer to 3.EXCLUSIVE COMMUNICATIONS.

■ System common

Recognized only when the TR-626 is in 'STOP' status in the Track Play mode.

Song Position Pointer

Status	Second	Third
F2H	llH	hhH

ll = Least significant :00H - 7FH (0 - 127)
hh = Most significant :00H - 7FH (0 - 127)

Song Select

Status	Second
F3H	ssH

ss = song select :00H - 05H (0 - 5)
06H - 7FH ignored

One each of track numbers 1 to 6 corresponds to the song selects 0 to 5 in that order, regardless of memory bank being currently selected (internal or external memory card).

■ System Real Time

Recognized only when the Sync mode is set at MIDI.

Timing Clock

Status
F8H

When Sync mode is set at MIDI, the TR-626 keeps rhythm timing to this clock.

Start

Status
FAH

When Sync mode is set at MIDI, the TR-626 starts running on the Start message.

Continue

Status
FBH

When Sync mode is set at MIDI, the TR-626 starts continue play upon receiving this message.

Stop

Status
FCH

When Sync mode is set at MIDI, the TR-626 stops upon receipt of this message.

3.EXCLUSIVE COMMUNICATIONS

See the TR-626 Owner's Manual for send/receive procedures of the exclusive messages.

One way communication

■ Data set

When recognized, the following messages are stored internally.

Byte	Description
F0H	Exclusive status
41H	Roland - ID
0bH	Device - ID = MIDI Basic channel
1DH	Model - ID (TR-626)
12H	Command - ID (DT1)
aaH	Address (MSB)
bbH	Address (LSB)
ddH	Data dd = 00H - 7FH
:	:
ddH	Data
ssH	Sum ss:aaH + bbH + ddH + ... + ddH + ssH = 0
F7H	EOX (End of Exclusive)

■ Address mapping of data

With the TR-626 the following data for memory bank 1 are available for send/receive of exclusive messages.

Pattern, track, and the level and pitch of each voice

Address		Description
aaH(MSB)	bbH(LSB)	
00H	20H	data start address
		data
2DH	10H	data end address