3. MX900 FADER CIRCUIT DESCRIPTION

3.1 Logarithmic amplifier.

The circuitry around the transistor array CA3046 and half the LM348 comprises a logarithmic amplifier. This amplifier takes the voltage tapped off the wiper of the fader track (which has the +15 volt supply across it in 'auto') and coverts it into a current using R55. This current is then compared with a reference current passing through R32 and VR3 taken from the same voltage (+15V supply).

The difference between the two currents appears as an offset at the output of the first section of the LM348. However, for each side of this bridge (made up of R55 and its transistor on one side and R32/VR3 and its transistor on the other) to be balanced, all the current entering by the collectors must leave by the common emitters.

Also, the left hand side transistor has its base grounded. When the two currents entering the inverting inputs are made equal, the output of the left hand ampifier becomes zero. This is the condition which corresponds to fader full up. Since there are minor differences in the geometry of the two transistor chips, the right hand resistor R32, is arranged to be variable (VR3) to compensate for the inequality and give the balanced condition referred to above.

As the fader is moved down the scale, the left hand input current reduces but the right hand current, being fixed, must still be drawn away through the common emitter connection. Since the emitters are commoned, and the left hand transistor is only having to pass the now smaller input current, the right hand transistor must be kept in the same conductivity as in the original case when both transistors were conducting the same currents.

Thus the base of the right hand device must rise above the level of the left hand device. Since the current through a transistor is proportional to the exponent of the base-emitter voltage, the base emitter voltage of the transistor must rise in an anti-exponential or logarithmic manner. If the voltage required by the base is attenuated from a larger source, then this source can be made to be logarithmic over a scale determined purely by the attenuator value.

The output of the left hand amplifier is the logarithm of its input current with a value of zero when the current is maximum and rising to the limit of the amplifiers swing for reducing currents. If an audio taper fader (whose output is in fact an exponent, not a log), is applied to the input of the logarithmic amplifier, the voltage at the output will become a more or less linear function of the fader position. ('More or less' because the exponential taper is further bent to give finer control over the upper half of the scale and ensure good shutoff at the bottom of the travel).

The only other point to note is that the log of zero is indeterminate, so when the fader is at the bottom of its scale, a small amount of current is stolen from the input by R36 to make sure that the amplifier saturates before the bottom stop of the fader is reached.

3.2 Switching

In the MasterMix Automation System, the fader does not itself control any audio at all. The output of the Logamp signals to the Digitiser via pin 19 of the interface what level is required and this is echoed back to drive the VCA via pin 20 on the interface.

If the MX700 Interface develops a fault, or the faders are installed without the MX700 Interface, there is a CMOS changeover switch (IC1 pins 1, 2, 3, 4, 5 & 15) whose control inputs (9 & 10) are driven from the MX700 Interface power supply via R63. When the MX700 Interface power is interrupted, or not present, the output of the log amp is sent directly to the VCA driver stage so that control is re-established.

The summing input of the third section of the LM348 carries the wipers of this switch together with some offset components (R56 & R57), so that control current can be taken either through R41 from the Logamp or via R43 from the MX700 Interface when power is present.

The gain of the control path and hence the tracking between fader scale value and attenuation is controlled by VR6 in the feedback loop of the third amplifier.

The offset component R57 can inject a small current into the inverting input of the stage for applications when the fader does not have unity gain with the wiper at full up.

3.3 Muting

The other section of the 4053 is activated by the computer's mute line so that when interface pin 12 goes high, the non-inverting input of the amplifier is taken to about -6.2 volts through a 330K resistor.

The rate of change is controlled by R38 and C30 which cause the amplifier output to rise quite slowly. The attack time of the mute is thus fairly long (about 33mS).

When the mute input goes false, the timing capacitor is discharged through 3.3K giving a very short (330 microS) recovery time which is, in practice, limited by the slew rate of the amplifier feedback loop.

The reason for the imbalance in the timeconstants is to compensate for the VCA gain characteristic, which is exponential (dB/Volt, not volt/volt). With attenuation, the exponential charge of the capacitor gives an almost linear dB/second attack time characteristic. However when recovering, the characteristic is doubly exponential giving a very long recovery time for the original gain to be achieved.

R56 gives the amplifier a gain of about three as far as the non-inverting input is concerned so that the muting voltage source is one that can be handled by the CMOS switch.

The CMOS switch itself has its supply built out with 1K resistors in both legs so that any tendency to go into 4 layer breakdown mode will merely result in temporary malfunction. If, owing to a fault, any of the pins of the 4053 do go below the voltage on pin 7, breakdown will occur and the chip will appear to be faulty with a short accross its supply pins. Removal of the source of negative voltage should effect a cure unless excessive currents have been passed.

3.4 Push pull driver stage.

The output of the third section of the LM348 (pin 8) sits at about zero volts when the fader is wide open. It swings negative at about 1 volt per 10 dB of fader movement. The ´catching´ circuit in the logamp cuts in at about -65 to -70dB on the fader scale and forces the output stage to saturate at this point.

Similarly, the last section of the LM348 (pin 7) inverts this characteristic giving a voltage which starts about zero volts and rises to saturation at about 12.5 volts positive.

3.5 VCA section.

The VCA section itself consists of an inverting NE5532 and an inverting NE 5534 with the Allison EGC 101 transistor array between. The audio input is coupled from the bypass switch via C34 which removes any small DC offsets which would be modulated by the VCA to produce ´thumps´ on the output when the control voltage moves quickly. The audio is then converted into current by R53 which is chosen to give a peak current of 3.2mA (15 volts peak signal accross 4.7K input resistor). This current flows into the feedback loop, which for positive excursions is formed by the left hand NPN transistor (R14) and part of VR1. For negative excursions, the path is the left hand PNP, R12 and part of VR1.

When the control current is zero (no drive from the LM348) the impedance of the feedback loop depends on the instantaneous difference between the base and emitter voltage of the NPN or PNP transistor in the loop.

For example, for a large positive excursion at the input, the amplifier output will swing negative and pull the left hand NPN emitter negative. The transistor´s base is tied to 0V with a low value resistor and so the action of pulling the emitter negative switches on the transistor allowing the impedance of the feedback loop to reduce strongly. Strongly enough to make sure that exactly the right amount of current is bypassed from the input to prevent its moving away from the voltage at the non-inverting amplifier and causing the amplifier to saturate.

The non-inverting input is tied to 0V which thus means that the collectors are tied to a virtual earth. This means that the instantaneous impedance of the feedback loop is almost entirely dependant on the level of the signal at the input. The larger the signal, the greater the feedback.

Since it is the input current which has to be diverted, and the current through a transistor´s collector is directly proportional to the exponent of the base emitter voltage, once again, the input side of the VCA circuit constitutes a logarithmic amplifier. However, because it has both NPN and PNP transistors in the feedback loop, it can handle both positive and negative signals at the input. In order to make sure that neither device tries to take the logarithm of zero or a negative quantity (by switching completely off) a static bias current is passed through both devices coming from the positive rail, through R13, through both the PNP then the NPN and finally via R15 to the negative rail. Across the transistors is a second identical pair of devices and the input amplifier´s drive potentiometer (R12, VR1 & R14).

Since the two pairs of devices have been selected to be very closely matched, NPN to NPN & PNP to PNP, the current through the bias chain should divide equally between the two parallel paths presented. Neglecting, for a moment, the presence of R48 and the FET (which will be described below) the voltage across the array (pin 9 to pin 1) is 4 Vbe´s or about 2.5 volts which allows the bias current in the chain to be determined. The total voltage across the chain is set at 30V. The centre section of 4 junctions keeps 2.5V accross it (4 Vbe´s) so there is 27.5 volts across two 3K´s in series. This gives a current of 4.48 mA through R13 & R15.

At the centre section, we have a voltage of 2.5V across a total resistance of 2.11K giving a current of 1.18 mA not passing through the junctions. The bias current is thus 3.3 mA which splits equally between the two halves of the array (assuming the two sides are exactly matched).

As we have seen, the peak input signal to be handled is 3.2 mA which has to flow through the right hand pair of transistors and the bias chain into the input amplifier´s output. The input amplifier will also accept the current flowing from the output amplifier´s output, via its feedback resistor and the left hand pair of transistors. The theoretically correct level of bias current would be thus twice the peak input current with a margin for error, half of which current would flow in each NPN/PNP pair assuming close matching between the two sides.

With no control drive present, all the audio current from the input amplifier will flow through the right hand set of transistors, through the output amplifiers feedback resistor and into the output of the output amplifier. However, as we have seen, the current that passes through the collector of a transistor is proportional to the exponent of the base-emitter voltage so that for small signal excursions, where the base-emitter differential is small, the collector current is very small indeed. For larger excursions, the current becomes exponentially larger. Thus, the input impedance of the right hand section of the VCA is large for small signals and very small for large signals. Since the right hand section is another inverting stage, the gain of the stage is directly proportional to this input impedance value.

The stage is thus behaving as the mirror image of the input section, and constitutes an anti-logarithmic amplifier.

Assuming once again that the two sections are perfectly matched, the log taken of the input signal should be perfectly anti-logged by the output section and the gain only determined by the values of the input and output resistors. For small input signals, this is found to be the case.

Having now built a log/anti-log amplifier, the interesting property of adding fixed quantities to the signal in its logged state can be investigated.

Adding a D.C. quantity to the signal in its logged state is the same as multiplication of the signal in its linear state. Multiplication of an audio signal is more normally referred to as gain for multiplication values greater than unity or attenuation for multiplication by values less tham unity (division).

Electronically speaking, if an offset is added to the base emitter voltages of the transistors, it will change the impedance of the collector-emitter path and affect the performance of the feedback loops in which the device is placed.

This is can be seen in the changes that occur in the output half of the VCA. Suppose an offset is introduced to the NPN and PNP devices which has the effect of turning the transistors on, the antilogging property of the junctions will still occur but the signal passed into the output amplifier will be greater. If this same offset is also arranged to increase the impedance in the feedback loop of the input amplifier, the signal passed into the anti-log stage will be greater.

This is the situation which results if the control circuit is arranged to bias the input NPN and output PNP bases slightly positive and the input PNP and output NPN bases slightly negative.

Such bias control introduces gain to the stage as a whole, so if the drive polarities are reversed, attenuation will result.

It is also interesting to look at the effect the control drive has on the bias current flowing through the two halves of the transistor array.

As the drive is increased in the attenuation direction (EGC 101 pins 7 & 16 negative and pins 3 & 12 positive) the input devices can be seen to be being switched further on and the output devices switched further off. This means that the bias current will no longer be shared equally and increasingly the input side will 'hog' the current. This is fortunate because attenuation normally takes place when the input signal is large and the need for bias is greatest.

The opposite is true when the input signal is small and gain is required. The input stage no longer needs the full bias available and can pass the surplus over to the output devices where it is needed.

This situation allows the VCA when used as a volume control to handle signals which are effectively twice as large as would be expected from a theoretically correct bias current of twice the expected peak input current.

In the MX500 (N-Option) version of the fader, with R53 as 2K4, R47 & R66 as 1K, there is a further increase in input current and an output attenuator is fitted (R47 & R66) because, with only a 24 V rail in the console, the nominal input signal level is some 6 dB lower than would be the case for a 20 Volt bipolar supply to the console electronics which is normal for more modern designs.

It is found that the noise level at the output decreases by about 6 dB for each 10 dB increase in attenuation so manipulation of the VCA gain structure gives worse noise tradeoff than straight output attenuation where both parameters go down in sympathy.

The other major benefit of using log/anti-log technology is found when overload does occur. When the signal current does exceed the bias, distortion rises rapidly but not in the same manner as straight clipping at the signal peaks where it rises almost vertically. This is because the log/antilog properties of the transistors still function but only after the delay while each device swithes back on after being switched off by a signal peak.

As might be expected, this delay time causes the distortion to be strongly frequency dependent under overload conditions being greater the higher the frequency. We can now turn to the effects of the FET and resistor R48. As we have seen above, for small input signals, the amount of bias through the VCA need only be small. This is important because, the output noise is directly related to the bias current. The greater the required signal handling, the greater the bias and vice versa. This means that all VCA's of this type have a fixed signal to noise ratio.

For a peak signal of +20 dB, the output noise is found to be -90dB (band limited to 20Hz to 20 KHz). Bearing in mind that there will always be a following amplifier of 10 to 12 dB gain, this means that the fader itself will provide a noise floor of about -78 to -80 dB.

Although on the face of it this is respectable, with digital recording or efficient noise reduction techniques removing a great deal of the input noise, the fader noise is now found to be a strong contributor to the overall noise of the system.

The fader noise will of course only be noticeable when there is no signal present and we therefore need a means of reducing the bias current when there is no need for it.

This is the function of the FET. With no gate bias, the device conducts according to its Idss parameter which is chosen here to be greater than the current to be stolen from the VCA's transistors. The stealing is proportional to the effective channel resistance and the build out resistor R48. The channel itself has a resistance of about 300 ohms and with R48, this gives a load of about 860 ohms.

As we have seen, there is about 2.5 volts across pins 9 and 1 of the VCA, largely independant of the current through the network. Thus our extra load takes around 2.9 of the 3.3 mA available bias, cutting this from 3.3 mA to 400 microamp when the FET is hard on.

When the peak input signal rises above 400 microamp, i.e. when the peak input voltage rises to 1.88 volts across 4.7K, the FET must start to turn off. This is an input signal of about +4 dBm at the input to the fader. Now +4dBm is in fact a very loud signal compared to our previous noise floor of -78 to -80dB which means that we can safely start turning the FET off much earlier. In fact the point where the FET starts to release current to the VCA is chosen to be around -6 dB and the gain in the rectifier driver stage is arranged to be enough to switch the FET entirely off by the time zero level is reached.

As with all peak rectifier circuits, there has to be an attack and decay times and these are usually crucial to the operation of the circuit. The attack time must be short enough so that isolated peaks are tolerated and is chosen to be about 200microS by R51 and C25 (1K and 0.1microF in a voltage doubler). The decay time is more difficult. To make sure that low frequencies do not allow significant discharge between pulses, especially as the rectifier is a simple voltage doubler, there has to be a smoothing network after the main reservoir capacitor C25. An ordinary smoothing network would put up the attack time unacceptably and so the swinging diodes D5 and D6 are used instead. For sharp transients D5 will conduct almost immediately and charge its small load capacitor C23. As soon as the transient is over, C25 starts to discharge slowly through R50 (2M2) giving a basic time constant of 220 mS. But because C25 is discharging slowly, it takes a significant time to start D6 conducting.

The rate at which D6 conducts is low because it is only just being kept in conduction. Therefore, D6 appears to be a high value resistor with an initial time constant with C23 of about 10 mS but a final time constant of a couple of seconds as C25 discharges exponentially through R50.

The time constant values are thus chosen to be those which give no appreciable bias modulation by a 20Hz input signal and barely perceptable modulation on a 10 Hz signal. This modulation can only be seen on the recovered distortion waveform and are completely inaudible in use.

3.6 Distortion trimming

The function of each of the distortion trims is as follows:

To correct for any differences between the NPN and PNP sides of the array, when there is no control drive, a small amount of the output signal is injected into the control circuitry. The level of this signal is selected by R10 and R11 and balanced by VR4. When the VCA is giving heavy attenuation, this function is taken over by VR1. It should also be noted that the two balance pots (VR1 and VR4) interact when the fader is open but VR4 has only a very small effect when the fader is well down. For this reason, the alignment method should be followed. Otherwise, a distortion null all the way from fader open to almost closed cannot be obtained.

When the input frequency rises, it will be found that the unequal handling of the two sides of the VCA resulting from differences in the HF hfe of the NPN and PNP sides requires that some extra balancing is provided especially when the fader is above its scale zero. The frequency where this starts to occur is selected by C9/R9 and is around 2KHz. The extra balance is set by VR5.

Unequal handling of the control current by the NPN and PNP sides is compensated for by VR2 which introduces a static bias to the output pair and thus lowers the unbalanced current which might flow into or out of pin 14 of the EGC 101 as the control drive changes.

The actual balance between the two polarities of the array is heavily temperature gradient dependent so that any temperature difference between the devices causes the unbalanced current to flow into the output amplifier and hence cause a shift at the output. Such temerature differences can only occur slowly owing to the thermal mass of the device. However, the offset is directly modulated by the control signal and appears as a 'thump' at the output whenever the control drive changes.

Bearing in mind that the Automation Grouping function of MasterMix is to move many faders at once, it is very important to prevent such control movements from causing even small shifts in each fader which, when mixed together, would produce unacceptable 'thumps' in the console output.

For this reason, the pot VR2 must always be reset when the faders have been installed and have reached their operating temperature.

VR2 does have an effect on the distortion especially at high levels of input signal and so it must be set before any of the other distortion trims are done and should be checked if difficulty is found in trimming a VCA which has been switched on for a while.

One other point to note is that MasterMix cannot convert negative signals from the logamp and so the swing of the output on pin 19 of the interface should be checked when the fader is full open. If there is a wrong value somewhere in the circuitry, the auto and bypass positions can often be made to track with near full scale settings of VR3 and VR6 but this may leave the interface drive swinging either heavily negative or not to a few millivolts above ground when the fader is open.

4. MX900 ALIGNMENT

4.1 Test Equipment Required

Bench PSU giving $\pm$20V DC and better than 1 mV Ripple noise peak to peak 50Hz to 100KHz.

Distortion measuring set, for example , Hewlett-Packard type 339A.

High sensitivity audio noisemeter (true RMS reading), for example, RADFORD type ANM2.

Fader Test Jig. (See Figure 4.1)

4.2 Preliminary Setting

Set all pots to midscale

4.3 Power Rail Checks

Monitor the power rails into the fader. With the fader in active and +18 dBm at 1 kHz on the input, the currents should be not greater than 42 mA on the +ve rail and 35 mA on the -ve rail at any position of the fader.

4.4 Gain/law adjustment:

Set an Input of 1kHz at +10dBm

Press Bypass on the Fader

Check that scale follows fader law at top, -10dB & -30 by setting fader knob at these points and measuring the output.

Press Auto

a) Set the fader knob to the top of the scale, adjust VR3 so that the auto/bypass levels are the same. (+10dBm out).

b) Set the fader knob to -20dB on scale, adjust VR6 for the same levels in auto and bypass. (-20 dBm out).

c) Repeat a) and b), then check fader at zero on its scale, there should be only about 0.5dB difference between auto/bypass levels. If the error is greater, then repeat a) and b) again sharing errors.

d) Check that the DC output on pin 19 of the signal connector is zero or slightly positive when the fader is at the top of its travel and rises to at least 11 volts when the fader knob is about 5mm from the bottom stop. Check also that the voltage begins to drop sharply when the knob is about 1 cm from the bottom stop.

4.5 DC Offset

Set for no input, by switching the oscillator off.

Connect a DC millivoltmeter between ground and pin 6 of IC 1. With the fader knob fully down, the output should be about 5mV and should not move relative to this offset by more than 5mV when the fader is moved from end to end of its travel slowly. If the offset is more than 5mV, adjust VR2 to null out the DC shift.

NB the offset with the fader open is thermally sensitive and care is needed not to upset the thermal balance of the EGC 101 whilst the adjustment is carried out. (Don´t touch the IC etc).

REMOVE DC MILLIVOLTMETER.

4.6 Distortion

Lowpass and highpass filters active (in).

a) Input 1KHz at +18 dBm, set the fader knob at -20dB. Adjust VR1 for minimum distortion.

b) Input 1KHz at +8dBm, set the fader knob at the top, remove the second harmonic with VR4.

c) Repeat a) and b) until the second harmonic component that occurs at each fader setting is minimised.

Limits: distortion should be better than 0.01% in each case.

Highpass filter inactive (out). Lowpass still active (in).

d) Input 20Hz at +18dBm, set the fader knob at zero, distortion should be better than 0.01%.

4.7 Frequency/distortion

"30 KHz" Low pass & High pass filters active (in).

a) Input 10Khz at +8dBm set the fader knob at +10dB, adjust VR5 to balance out any second harmonic. Limit better than 0.01%.

b) Input 10KHz at +18dBm, set the fader knob at zero, check distortion is less than 0.015%, if greater, bring into spec with VR5 and check that result does not put distortion under a) conditions above 0.01%.

Check the following limits with the "80KHz" filter active and "30KHz" inactive for 20KHz measurements only and High pass active throughout. For measurements below 20KHz, the "30KHz" should be active as well.

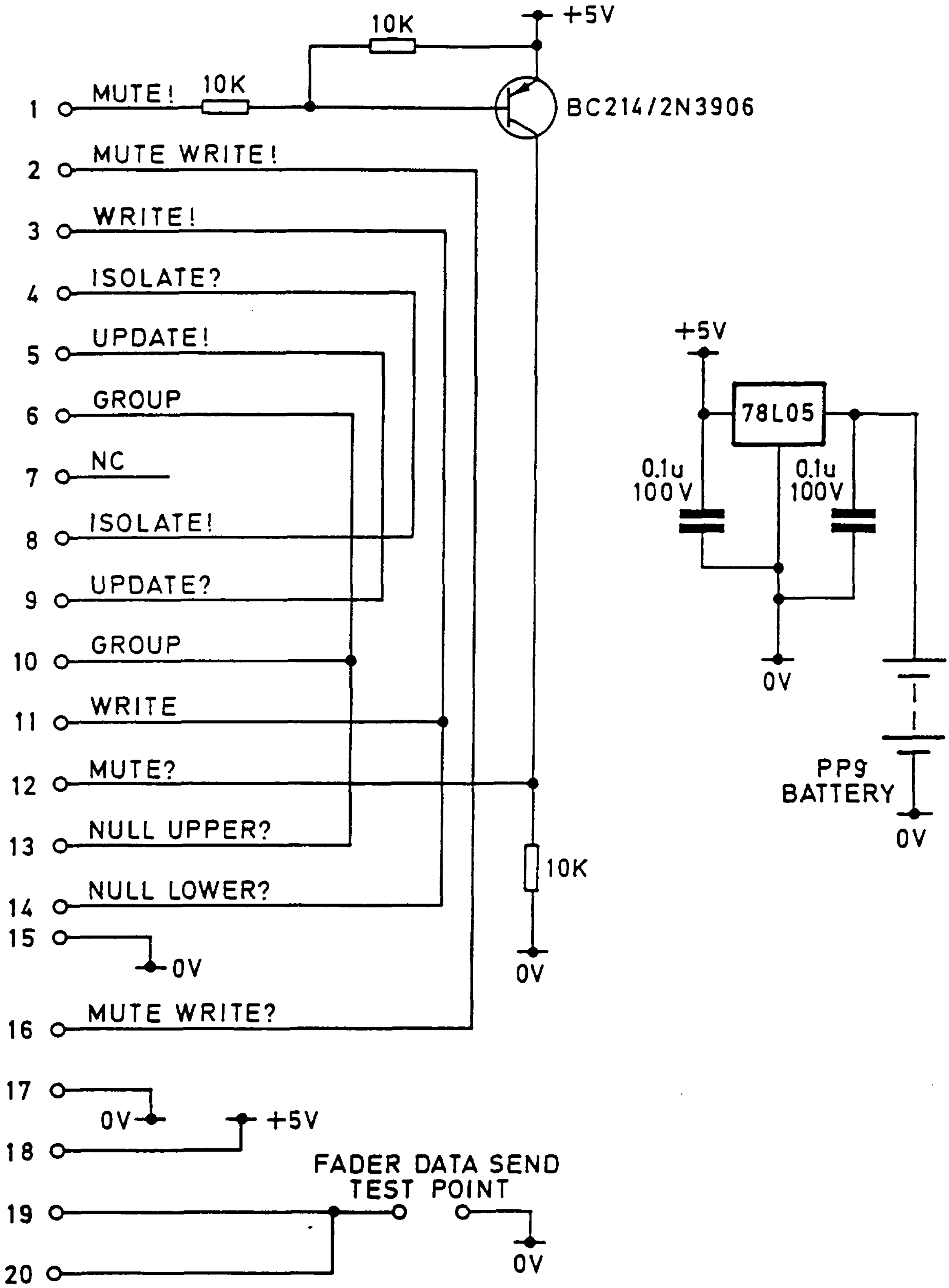
Input +8dBm, set the fader knob at top:
20kHz max=0.015%, 10kHz max=0.01%, 3kHz max=0.008%, 1KHz max=0.006%.

Input +18dBm, set the fader knob at zero:

20kHz max=0.02%, 10kHz max=0.015%, 3kHz max=0.008%, 1KHz max=0.006%.

Input +18dBm, set the fader knob at -10:

20kHz max=0.018%, 10kHz max=0.012%, 3kHz max=0.01%, 1KHz max=0.008%.7.



IDC FEMALE CONNECTOR

USED ON : PSM200, PSM210, PSM900

Figure 4.1

MODIFICATION	ISSUE	DATE	DRAWN	CHECKED	DRAWING NO.
	2	4.10.84	JMW		A4/PM/PSM200/4.1

AUDIO KINETICS (UK) LIMITED
Kinetic Centre
Theobald Street
Borehamwood
Hertfordshire
England
Telephone Number

AUDIO KINETICS

TITLE

MX200/500/900 FADER TEST JIG

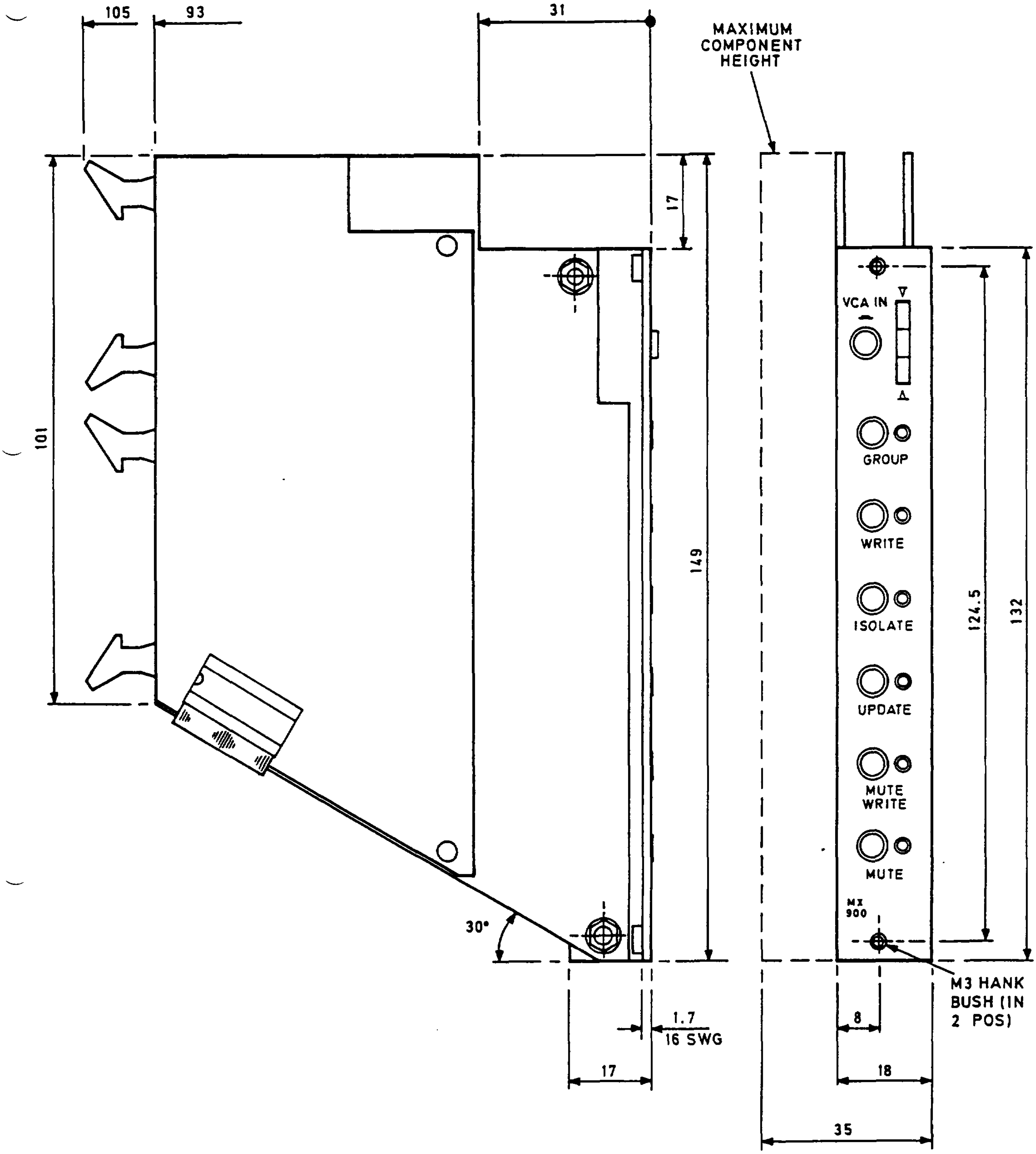


Figure 4.1

MODIFICATION	ISSUE	DATE	DRAWN	CHECKED	DRAWING NO.
	1	4.1.85	JMW		A3/PM/PSM900/4.1

TITLE

OVERALL PHYSICAL DIMENSIONS MX900 SERIES FADER

AUDIO KINETICS

AUDIO KINETICS (UK) LIMITED
Kinetic Centre
Theobald Street
Borehamwood
Hertfordshire WD6 4PJ
England
Telephone Number 01 953 8118

4.8 Noise measurments:

Using RADFORD millivoltmeter, indicated maximum values are:

	Wideband	Din audio band
Fader at top	-85dBv	-100dBv
Fader at zero	-90dBv	-105dBv
Fader at -10	-92dBv	-109dBv
Fader at -20	-93dBv	-111dBv
Fader at bottom	-94dBv	-114dBv

NB the Radford is scaled in dBv not dBm and so to get dBm s/n ratios the above are reduced by 2.5dB.

4.9 DC Offset Check

Recheck the DC offset as in 4.3 above and reset if necessary.

4.10 Switch and LED Check

Connect the MX700 Interface plug, check each switch on the front panel and make sure that it echoes the correct LED:

The "group" button should echo its LED and no other.

The "write" button should echo its LED and the top "null" LED and turn off the centre "null" LED.

The "Isolate" button should echo its LED and no other.

The "update" button should echo its own LED and the lower "null" LED and turn off the centre "null" LED.

The "mute write" button should echo its own LED and no other.The "mute" button should echo its own LED and also mute the audio signal (fader not in bypass). The muting should be at least 95 dB at 10KHz and 10dB better at 1KHz.

The audio level difference between 5V present and 5V switched off should be not measurable (fader not in bypass). If it is, check on the power pins (8 and 16) of the 4053. If less than 12V is present between them switch off the main supply and switch it back on again. If the voltage on the supply pins of the 4053 is now correct, check that none of the chip voltages are unusual with 5V present and absent.

(The 4053 can often be triggered into abnormal conduction by a probe slipping and causing a short circuit in some part of the circuitry.

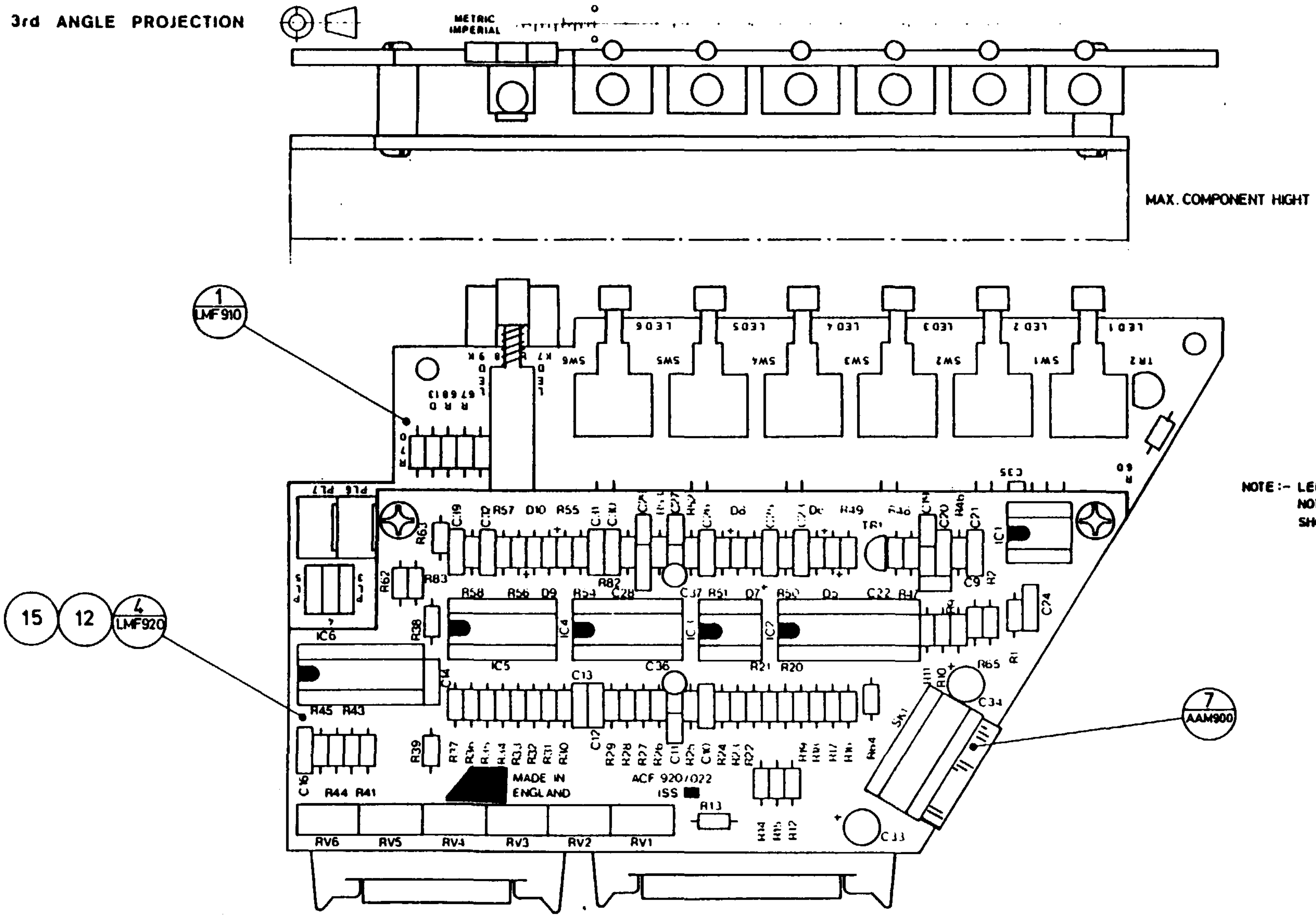
If this event causes one of the high voltage supplies to be connected directly to one of the 4053's pins, the circuit may be destroyed. It usually signals this by trying to take heavy supply current. If the short circuiting probe did not pass large currents into the device,the fault is nearly always cleared by switching off and back on again. However, if the circuit will not support 12V via the two 1K resistors, when power is reapplied, it should be replaced.)

If the link between interface pins 19 and 20 is broken with the 5V present and the fader not in bypass, the fader should appear to be almost closed irrespective of the position of the knob. Switching the 5V off should then cause the fader to function normally again.

5. MX900 FADER DIAGRAMS

5.1	Circuit Diagram	A2/PM/ACF900/001
5.2	Fader Assembly	A2/PM/MMF900/022
	Fader PCB Assembly	A2/PM/ACF900/022
5.3	Fader Switch Board PCB Assembly	A2/PM/ACF910/022
	Fader Audio Board PCB Assembly	A2/PM/ACF920/022
5.4	Interface Connector	
5.5	Power Connector	
5.6	Audio Connector	A4/PM/PSM200/5.6

3rd ANGLE PROJECTION



NOTE :- LED.S AND BUTTON CAPS ARE NOT FITTED AT THIS STAGE SHOWN FOR REFERANCE ONLY

MATERIAL	TOLERANCE
SEE PARTS LIST	
FINISH	SURFACE ROUGHNESS
DIMS IN	SCALE TWICE SCALE

AUDIO KINETICS

TITLE

AK FADER P.C.B ASSEMBLY

DRAWING NUMBER

A2 / PM / ACF 900 / 022

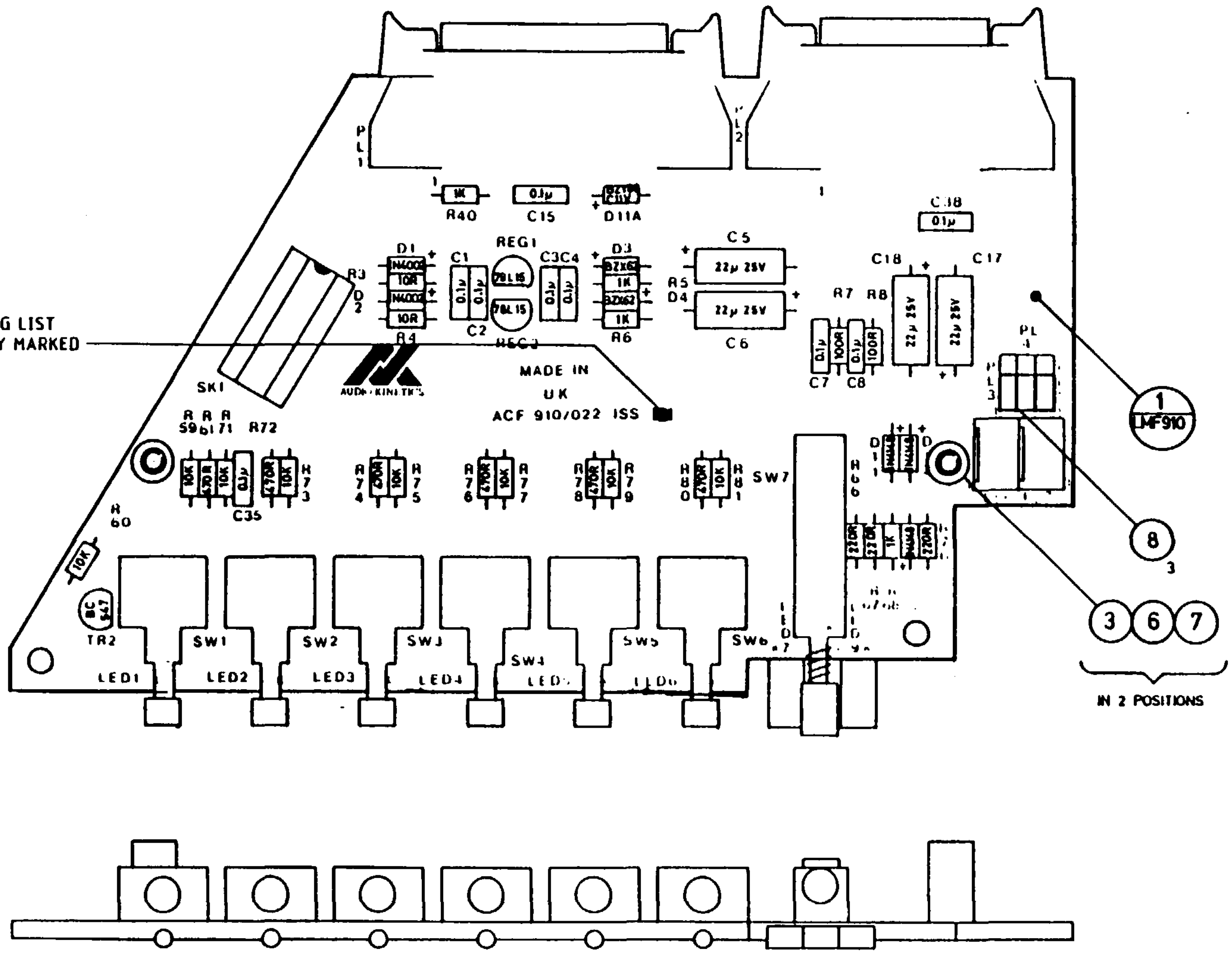
AR No	ISSUE	DATE	AR No	ISSUE	DATE	AR No	ISSUE	DATE
	1	26.8.86						

DRAWN VDS

USED ON MX900

3. ANGLE PROJECTION

METRIC
IMPERIAL



CERT'D.	MATERIAL	TOLERANCE
CHECKED	REFER TO PARTS LIST	
DRAWN WJS	FINISH	SURFACE ROUGHNESS
	DIMS IN	SCALE TWICE SIZE

AUDIO KINETICS

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AR. No.	ISSUE	DATE	AR. No.	ISSUE	DATE	AR. No.	ISSUE	DATE
	1	17.8.84						

TITLE
AK FADER SWITCH BOARD
P.C.B. ASSEMBLY

DRAWING NUMBER
A2/PM/ACF 910/022

5.4 Interface Connector

1	MUTE!	Switch
2	MUTE WRITE!	Switch
3	WRITE!	Switch
4	ISOLATE?	LED
5	UPDATE!	Switch
6	GROUP!	Switch
7	Not Connected	
8	ISOLATE!	Switch
9	UPDATE?	LED
10	GROUP?	LED
11	WRITE?	LED
12	MUTE?	LED and MUTE command to Fader
13	Above NULL?	LED
14	Below NULL?	LED
15	Logic Ground	
16	MUTE WRITE?	LED
17	MX700	Analogue Ground (Audio Common)
18	MX700	+5V
19	Data FROM FADER TO MX700 INTERFACE(ENCODE)	
20	Data TO FADER FROM MX700 INTERFACE(DECODE)	

20 way ribbon socket, closed end and polarised.

All signals except Encode/Decode are TTL compatible and LOW for true except the MUTE? which is HIGH for true.

6. MX190 FADER CONTROL SWITCHES AND LEDS

The switches and LEDs present on the front panel of the MX190 Fader Control are illustrated in Figure 6.1.

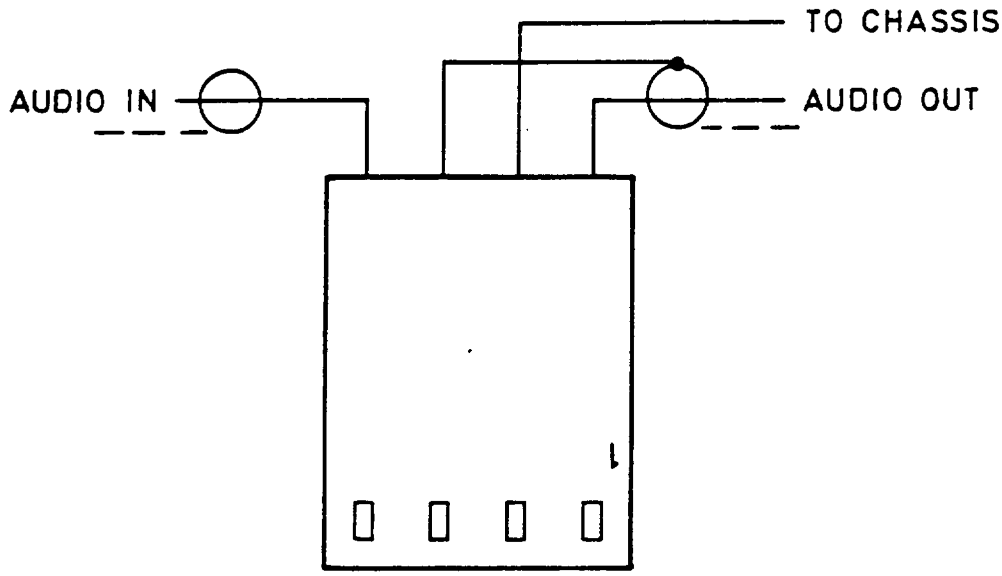
The MX190 module is used to select all faders' functions with single key entries.

It consists of an array of single pole single throw switches with 10K pullups to MasterMix +5V supply rail (interface pins 19 and 20) which all make to ground (interface pins 13 and 14). There is also an array of LED tallies each of which has a 470 ohm dropper to their individual pins.

The only active element in the module is the opto-coupler/buffer circuit (IC2/1) which allows an isolated logic input to be sent to the interface. At present this input is not used and should be left unconnected.

There is no active logic in the module as such, all the intelligence being provided by the interface software.

Plugging the module onto a fader interface connector or vice versa will not damage either but the fault should be rectified immediately because pressing certain keys on the master module can short out the 5V supply and damage the ribbon link to the interface.



4 WAY MOLEX SHELL AND PINS VIEWED FROM CONTACT LOCKING SLOTS SIDE. SOCKETS DOWNWARDS.

FADER ANALOGUE GROUND IS CARRIED THROUGH SCREEN ON CABLE TO INPUT STAGE OF POST-FADER BUFFER AMPLIFIER IN CONSOLE MODULE.

CHASSIS CONNECTION IS TAKEN TO THE FADER ELEMENT METALWORK ONLY. THE FRONT PANEL IS GROUNDED VIA ITS FIXING SCREWS.

Figure 5.6

MODIFICATION	ISSUE	DATE	DRAWN	CHECKED	DRAWING NO.
	1	20.7.84	JMW		A4/PM/PSM200/5.6

AUDIO KINETICS
AUDIO KINETICS (UK) LIMITED
Kinetic Centre
Theobald Street
Borehamwood
Hertfordshire WD6 4PJ
England
Telephone Number 01 953 8118

TITLE

AUDIO CONNECTIONS TO MX200/500/900 FADER SERIES

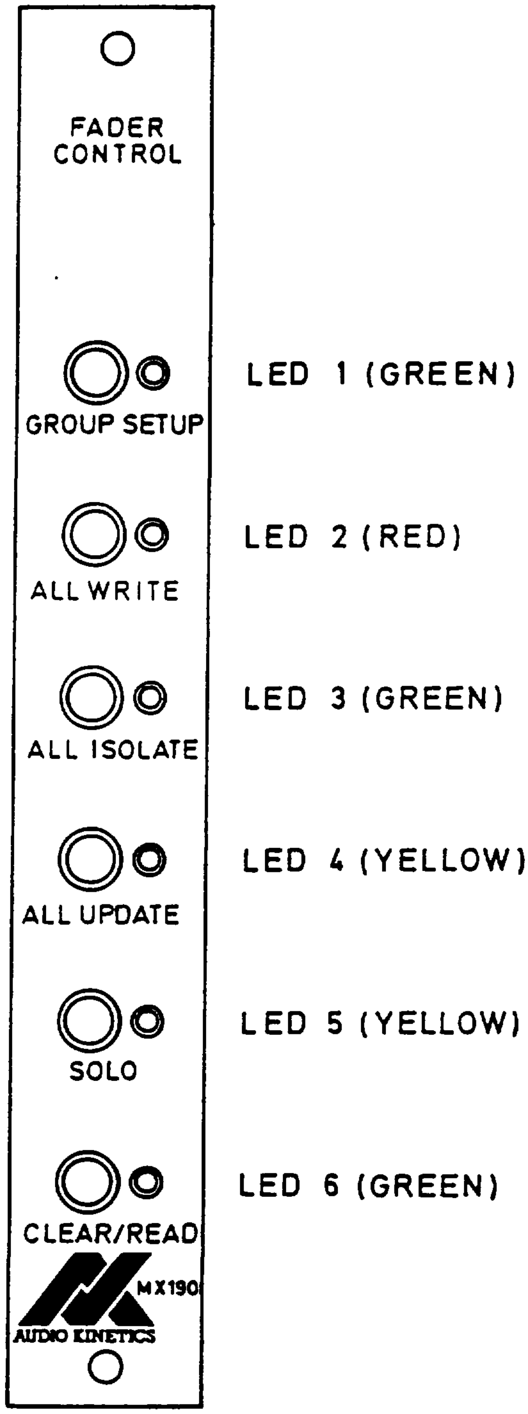


Figure 6.1

MODIFICATION	ISSUE	DATE	DRAWN	CHECKED	DRAWING NO.
	A	4.10.84	JMW		A4/PM/PSM900/6.1

AUDIO KINETICS
AUDIO KINETICS (UK) LIMITED
Kinetic Centre
Theobald Street
Borehamwood
Hertfordshire WD6 4PJ
England
Telephone Number 01 953 8118

TITLE

MX190 FADER CONTROL

5.5 Power Connector

1	Console Audio Common
2	Console Audio Common
3	Console Audio Common
4	Console Audio Common
5	Console Audio Common
6	Console Audio Common
7	Console Audio Common
8	+20V
9	+20V
10	+20V
11	-20V
12	-20V
13	-20V
14	-20V
15	-20V
16	-20V
17	+20V
18	+20V
19	+20V
20	Power Supply Common
21	Power Supply Common
22	Power Supply Common
23	Power Supply Common
24	Power Supply Common
25	Power Supply Common
26	Power Supply Common

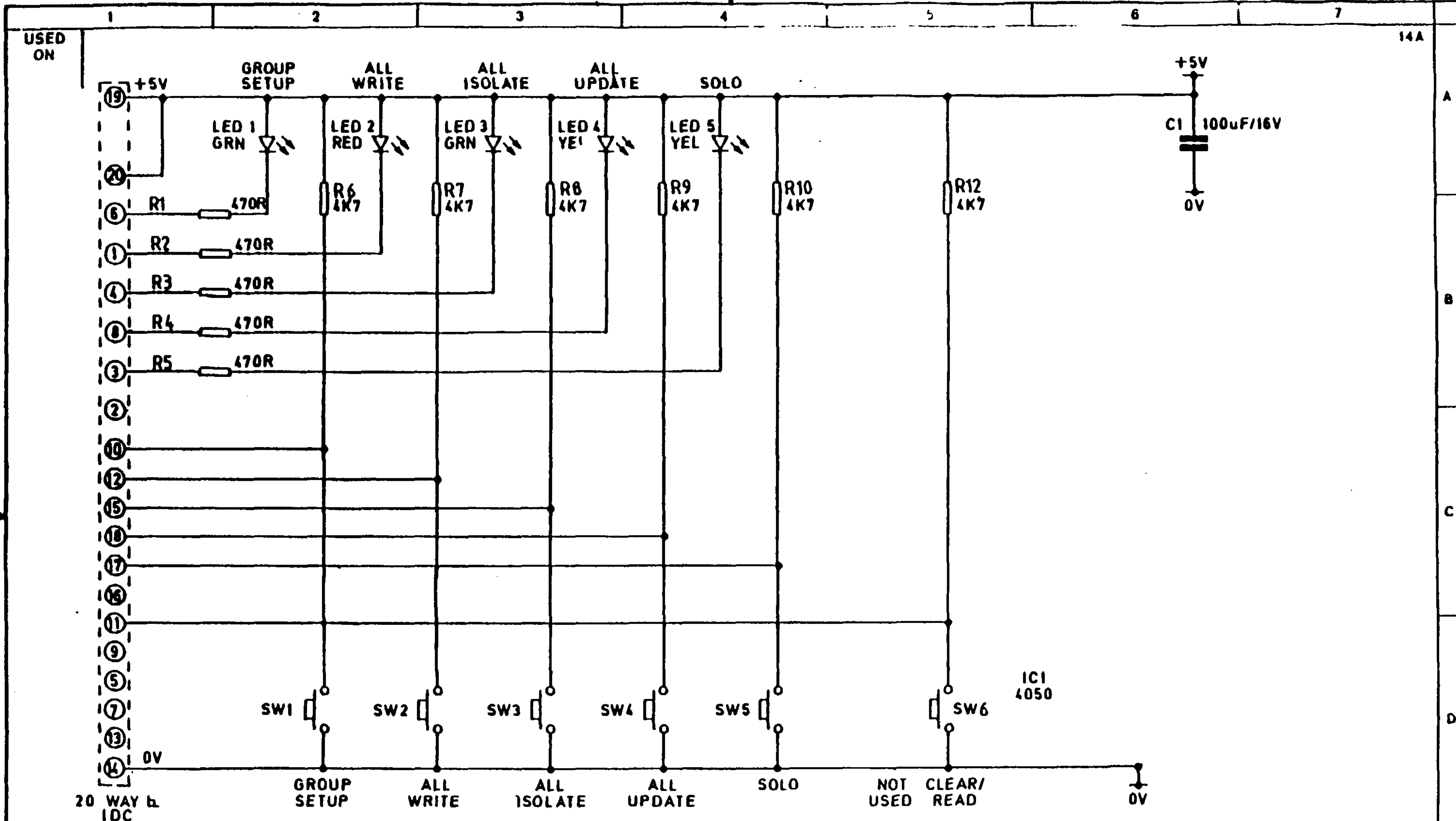
26 Way ribbon socket open ended.

7. MX190 FADER CONTROL DIAGRAM

7.1 Circuit Diagram A3/PM/ACF020/001

7.2 Fader Control PCB and AssemblyA3/PM/MMF020/022

7.3 Signal Connector



CERT'D.	MATERIAL	TOLERANCE
CHECKED	FINISH	SURFACE ROUGHNESS
DRAWN JMW	DIMS.IN	SCALE

AUDIO KINETICS

AUDIO KINETICS (UK) LIMITED

AR. No.	ISSUE	DATE	AR. No	ISSUE	DATE	AR. No.	ISSUE	DATE
						NA	1	17·9·84

TITLE

FADER CONTROL CIRCUIT

DRAWING NUMBER

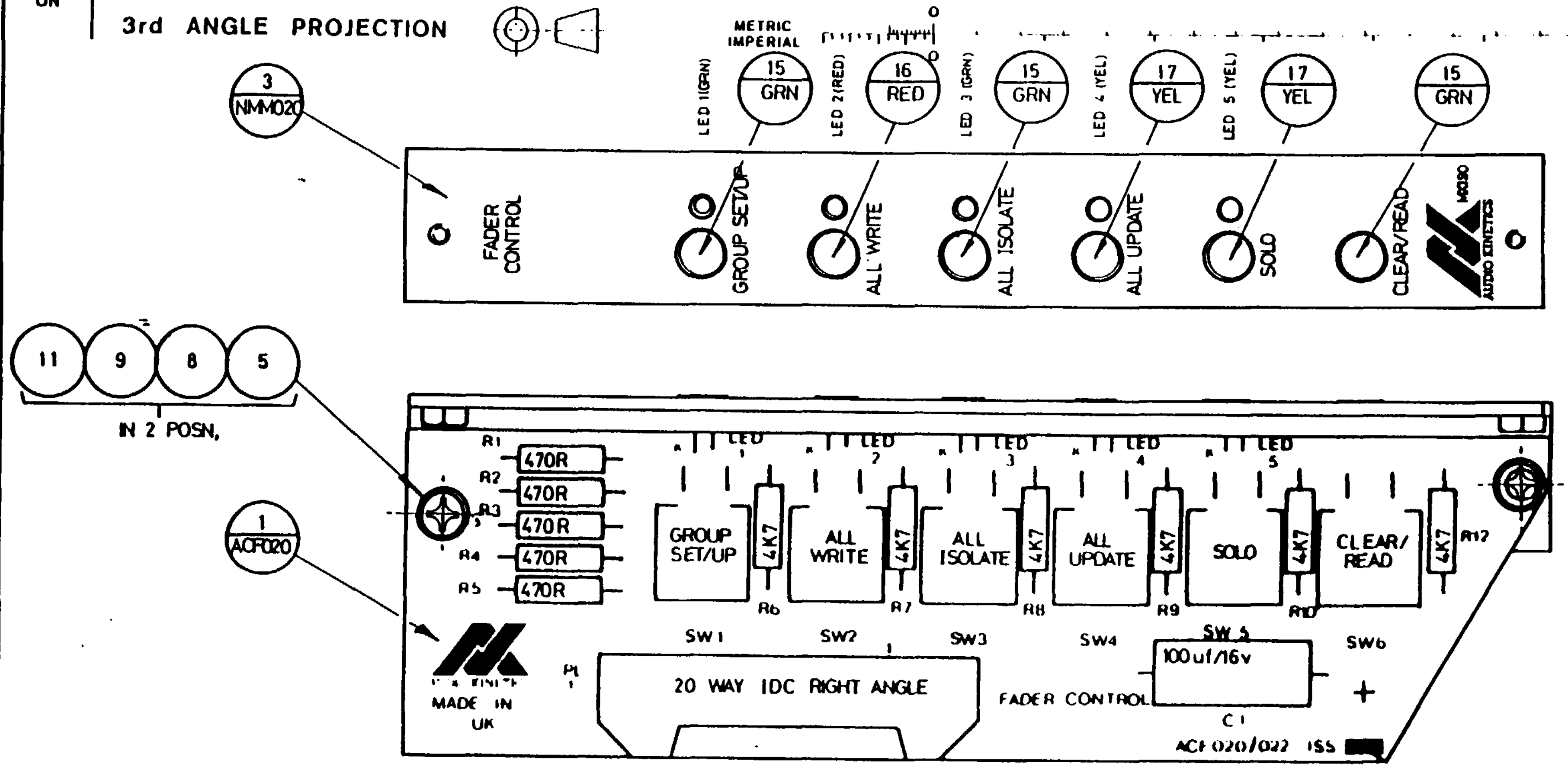
A3/PM/ACF020/001

A3

LONSDALE TECH 3100/84

USED ON

3rd ANGLE PROJECTION



14 A

CERT'D.	MATERIAL	TOLERANCE
CHECKED	FINISH	SURFACE ROUGHNESS
DRAWN	DIMS.IN	SCALE 2 1

AUDIO KINETICS

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Kinetic Centre
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Borehamwood
Hertfordshire WD6 4PJ
England
Telephone Number 01 953 8118

AR. No.	ISSUE	DATE	AR. No.	ISSUE	DATE	AR. No.	ISSUE	DATE
						—	A	24.8.84

TITLE
FADER CONTROL ASSY

DRAWING NUMBER
A3/PM/MMF020/022

A3

7.3 Signal Connector

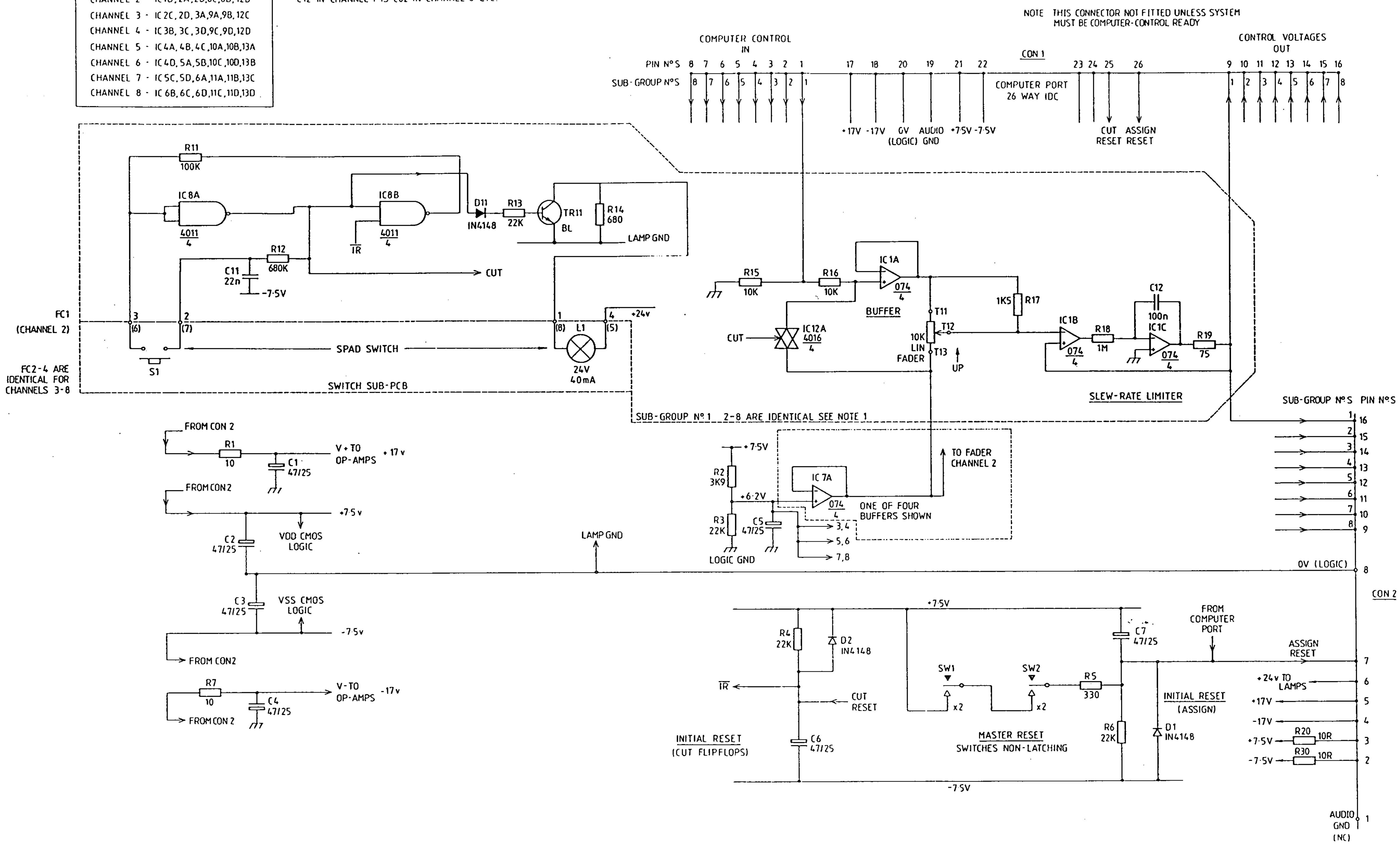
1	ALL WRITE LED
2	UnassignedLED
3	SOLO LED
4	ALL ISOLATELED
5	Unassigned
6	GROUP SETUPLED
7	Unassigned
8	ALL UPDATELED
9	PLAY TALLY
10	GROUP SETUPSwitch
11	CLEAR/READSwitch
12	ALL WRITE Switch
13	OV
14	OV
15	ALL ISOLATESwitch
16	Unassigned
17	SOLO Switch
18	ALL UPDATESwitch
19	+5V
20	+5V

DRG No. ED 2211

Initl	Issue
	Issue 1 21-11-84
	ISSUE 2 20 - 6 - 85
	ISSUE 3 14 - 8 - 85
	ISSUE 4 D2 TYPE NO. ADDED(IN4148) 28-5-87

CHANNEL 1	IC1A, 1B, 1C, 8A, 8B, 12A
CHANNEL 2	IC1D, 2A, 2B, 8C, 8D, 12B
CHANNEL 3	IC2C, 2D, 3A, 9A, 9B, 12C
CHANNEL 4	IC3B, 3C, 3D, 9C, 9D, 12D
CHANNEL 5	IC4A, 4B, 4C, 10A, 10B, 13A
CHANNEL 6	IC4D, 5A, 5B, 10C, 10D, 13B
CHANNEL 7	IC5C, 5D, 6A, 11A, 11B, 13C
CHANNEL 8	IC6B, 6C, 6D, 11C, 11D, 13D

NOTE 1
R15 IN CHANNEL 1 IS R25 IN CHANNEL 2 ETC.
C12 IN CHANNEL 1 IS C82 IN CHANNEL 8 ETC.



NOTES.

HOLE INDEX.

TOLERANCE
All imperial dimensions ±0.010
All metric dimensions ±0.25mm
All angles ±0.50°
Unless otherwise stated.

THIRD ANGLE PROJECTION

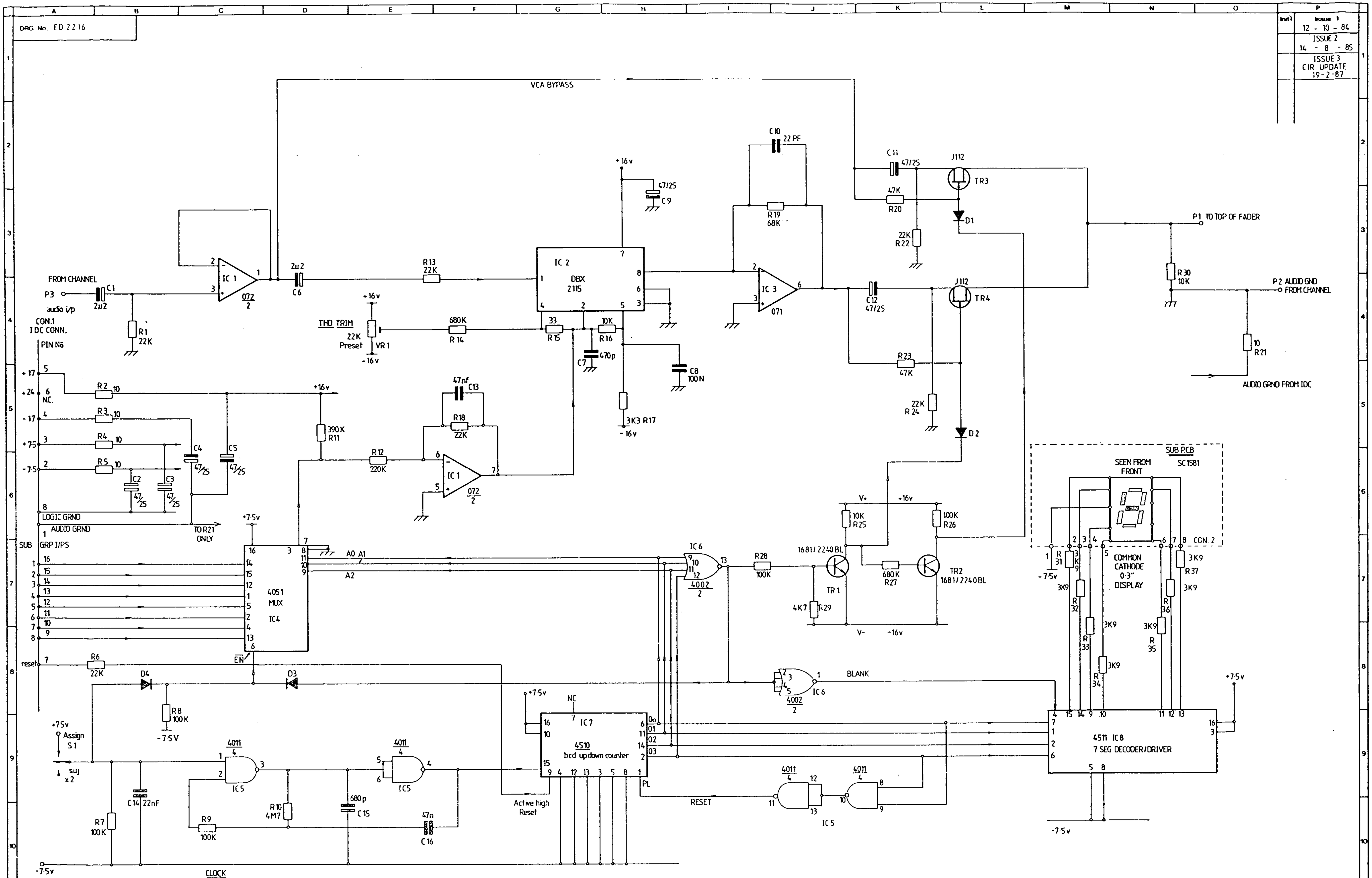
MATL.
FINISH.
SCALE.

DRG.
TRCD.
CHKD.

SOUNDCRAFT ELECTRONICS LTD.
5-8 GREAT SUTTON STREET
LONDON EC1V 0BX.
TELEPHONE 01-251-3631/2/3
TELEGRAMS SOUNDCRAFT LDN. EC1
TELEX, UK No. 21198 USA No. 01-2203

TITLE
TS24
VCA MASTER
CIRCUIT DIAGRAM

DRG No. ED2211



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NOTES.

HOLE INDEX.

ALL DIODES 1N4148
ALL RESISTORS 1/4 W

TOLERANCE.
All imperial dimensions ±0·010
All metric dimensions ±0·25mm
All angles ±0·50°
Unless otherwise stated.

THIRD ANGLE PROJECTION

MATL.
FINISH.
SCALE.

DRG. DS
TRCD. CHRIS
CHKD.

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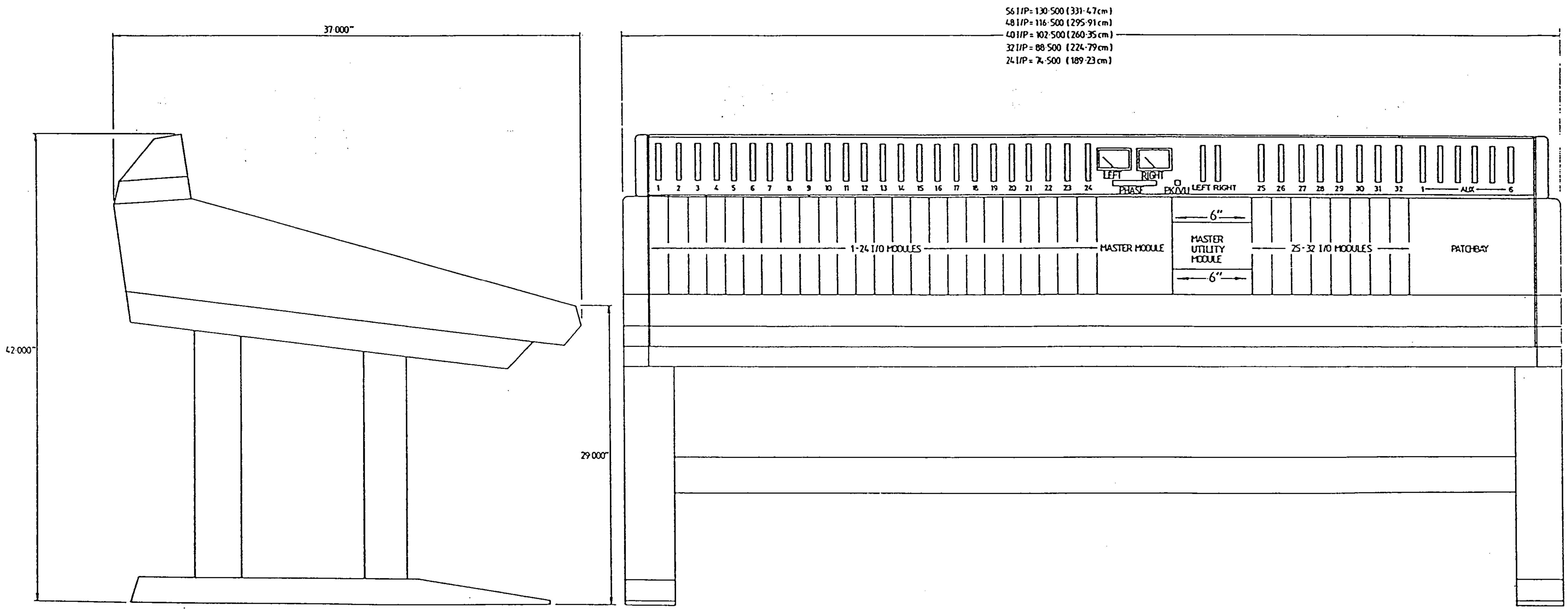
TELEPHONE. 01-251-3631/2/3
TELEGRAMS. SOUNDCRAFT LDN. EC1
TELEX. UK No. 21198. USA No. 01-2203

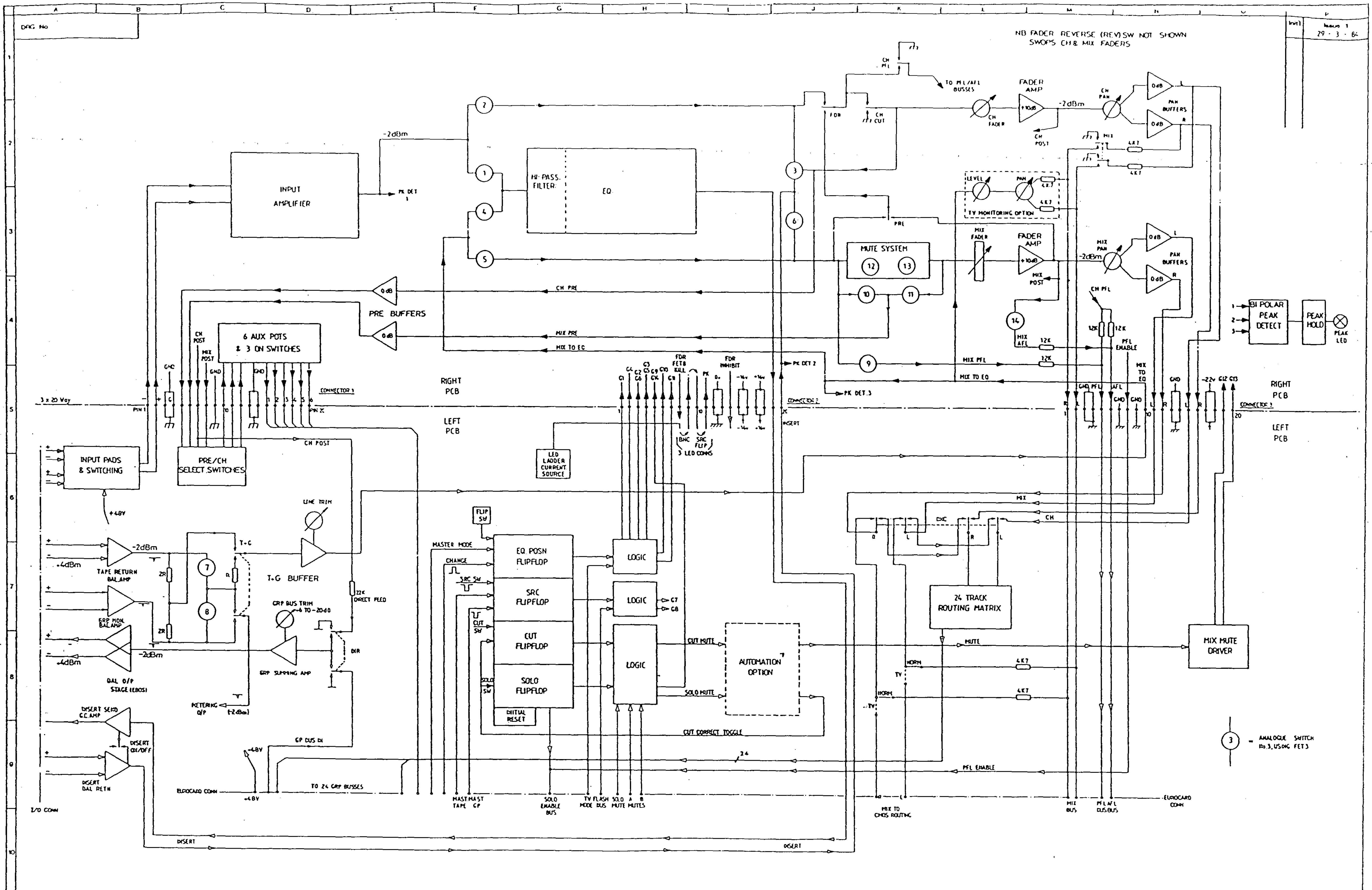
TITLE. TS 24
VCA SUB GROUP
CHANNEL PCB

DRG No. ED 2216

DRG No. MI 2371



NOTES.	HOLE INDEX.	TOLERANCE.	THIRD ANGLE PROJECTION	MATL.	DRG. CHRIS	SOUNDCRAFT ELECTRONICS LTD.	TITLE TS 24 CONSOLE LAYOUT
		All imperial dimensions ±0.010 All metric dimensions ±0.25mm All angles ±0.50° Unless otherwise stated.		FINISH.	TRCD.	5-8 GREAT SUTTON STREET LONDON, EC1V. 0BX. TELEPHONE. 01-251-3631/2/3	
				SCALE. NOT TO SCALE	CHKD.	TELEGRAMS. SOUNDCRAFT LDN. EC1 TELEX. UK No. 21198, USA No. 01-2203	DRG No. MI 2371



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NOTES. 1) G REFERS TO GATE OF THAT NUMBER FET. IE G4 = GATE OF FET4
2) ALL SIGNALS IN PHASE (+) UNLESS SHOWN OTHERWISE BY SYMBOL

HOLE INDEX.

TOLERANCE.
All imperial dimensions ±0·010
All metric dimensions ±0·25mm
All angles ±0·50°
Unless otherwise stated.

THIRD ANGLE PROJECTION

MATL.	—	DRG.	D S
FINISH.	—	TRCD.	
SCALE.	—	CHKD.	

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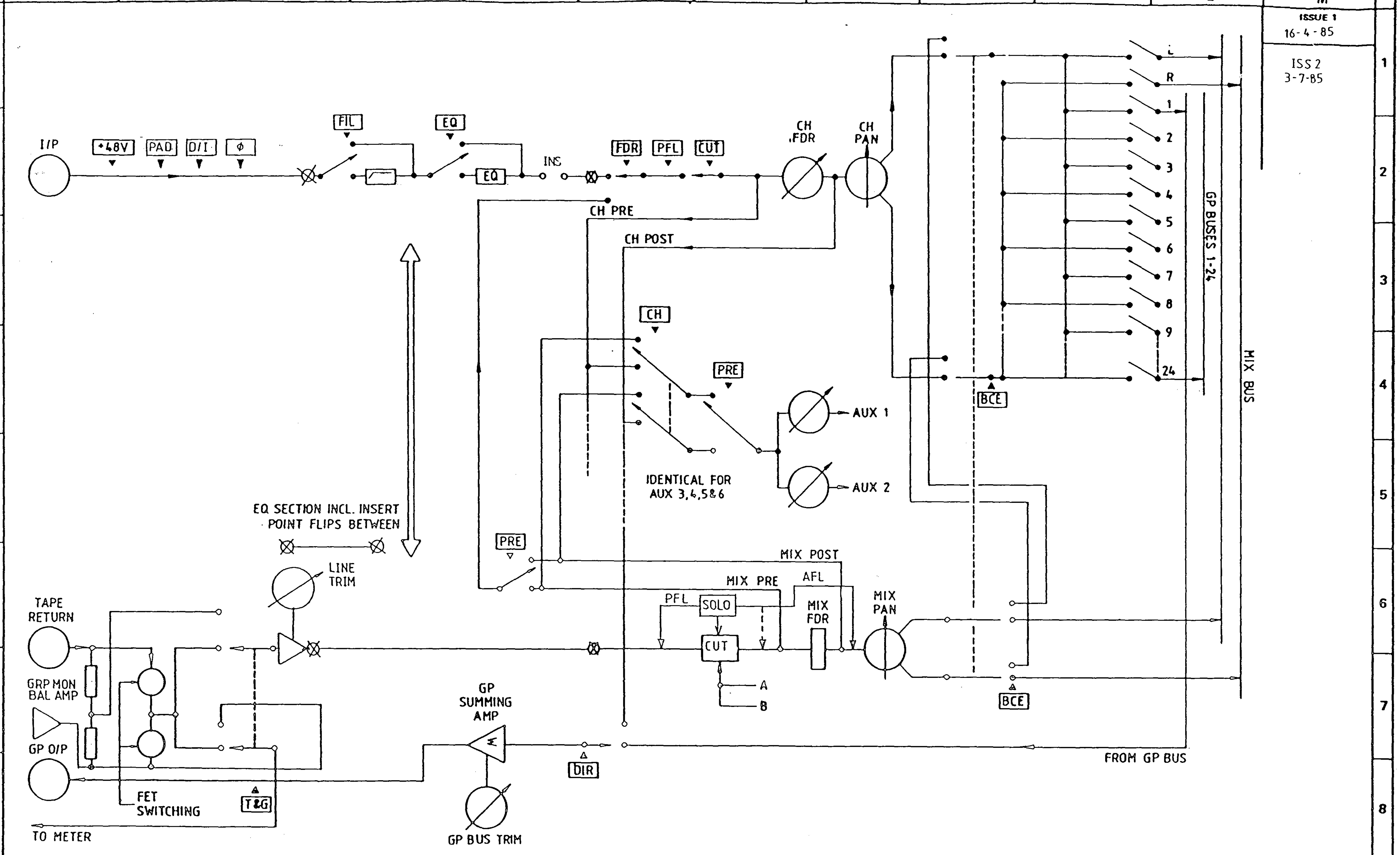
TELEPHONE. 01-251-3631/2/3
TELEGRAMS. SOUNDCRAFT LDN. EC1
TELEX. UK No. 21198. USA No. 01-2203

TITLE. TS24 I/O MODULE LINE TRIM BLOCK DIAGRAM

DRG No. ED2258



THIRD ANGLE PROJECTION	TOLERANCE	HOLE INDEX	MATL	DRN	
	All imperial dimensions ± 0·010 All metric dimensions ± 0·25mm All angles ± 0·60° Unless otherwise stated		FINISH	TRCD	
			SCALE	CHKD	

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TELEGRAMS. SOUNDCRAFT LDN EC1
TELEX. UK. No. 21198. USA. No. 224408

TITLE TS24 I/O (LINE TRIM) MODULE SIGNAL FLOW DIAG SHOWING BOUNCE

DRG. No. ED 2256

UDO 30910