

## APPENDIX C. BLOCK DIAGRAMS AND SCHEMATICS

These schematics are, of course, crucial if you are trying to service an 8X32. A word about the conventions used in drawing the schematics is in order. On every schematic, a timing signal that leaves that sheet and goes elsewhere is indicated with an arrow for the connector, which is represented by the little triangle-shaped symbol. If the signal is sourced on the module schematic you are looking at, then the arrowhead of the connector symbol points away from the head, indicating that the circuitry on that sheet is the source for the timing signal or other piece of data. If the arrow is coming into the sheet, then the source of the signal is external.

The following are additional notes about the ANA-2 schematics:

### ANA-2, I/O (sheet 1)

Note 1: RV11 and associated components added in REV 3 version to allow DC offset adjustment of signal MTIN. Earlier units need not have this feature.

Note 2: Only REV 3 version has the 7 pin output connector. Earlier versions used discrete wires, soldered to the PC connector J20.

### ANA-2, ADA, (sheet 2)

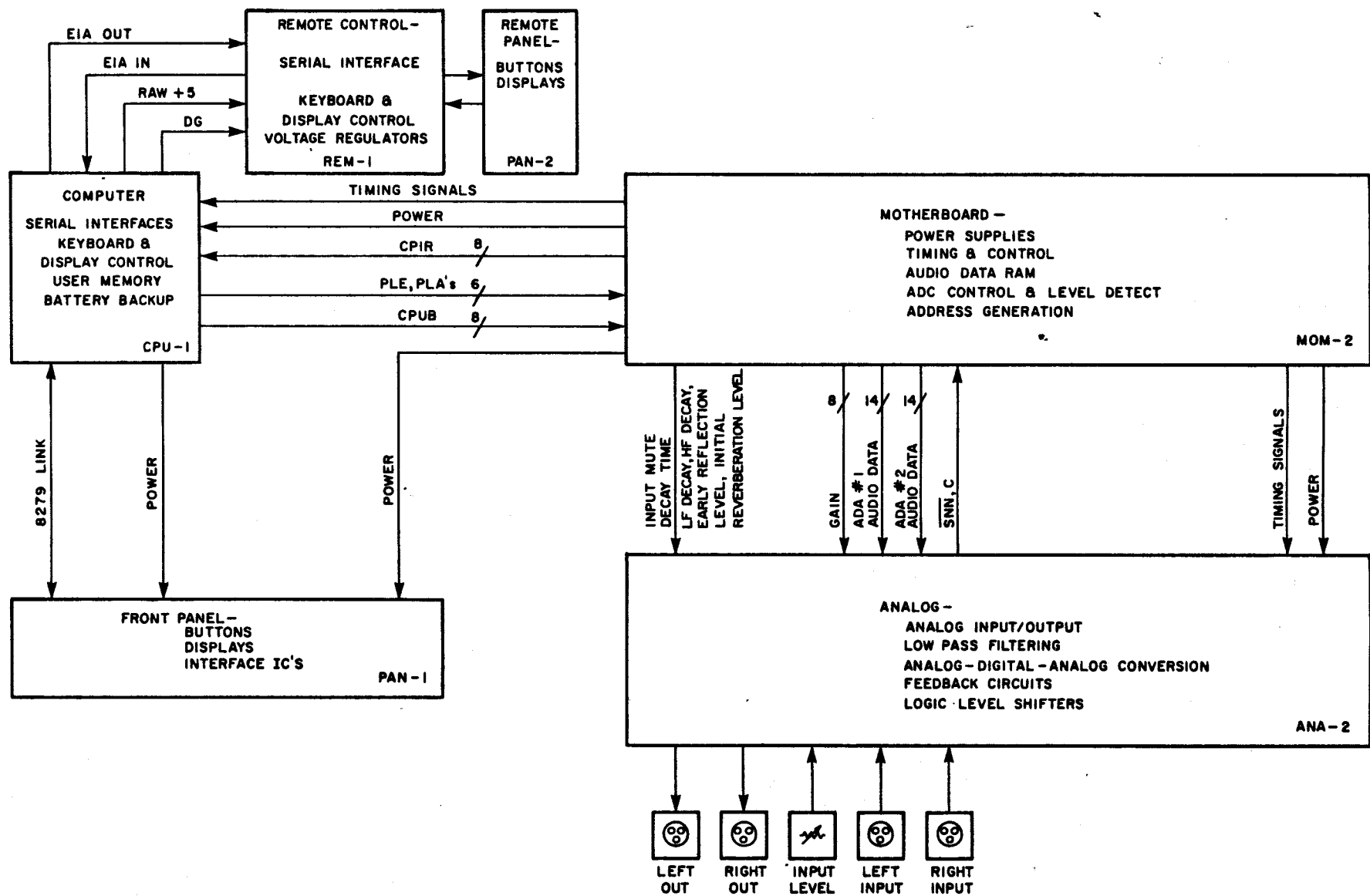
Note 1: Signal M1 forced to zero, and signal CFD ignored due to changes in program software of Program Edition E4-1. M1 set to zero in software, while CFD cancelled by deleting resistors R38 and R40.

Note 2: When FSB #10 ("Reducing the Noise") is carried out, two .0039 capacitors are added, and R68 is changed to 3.09K. See other notes, or FSB #10 for other details.

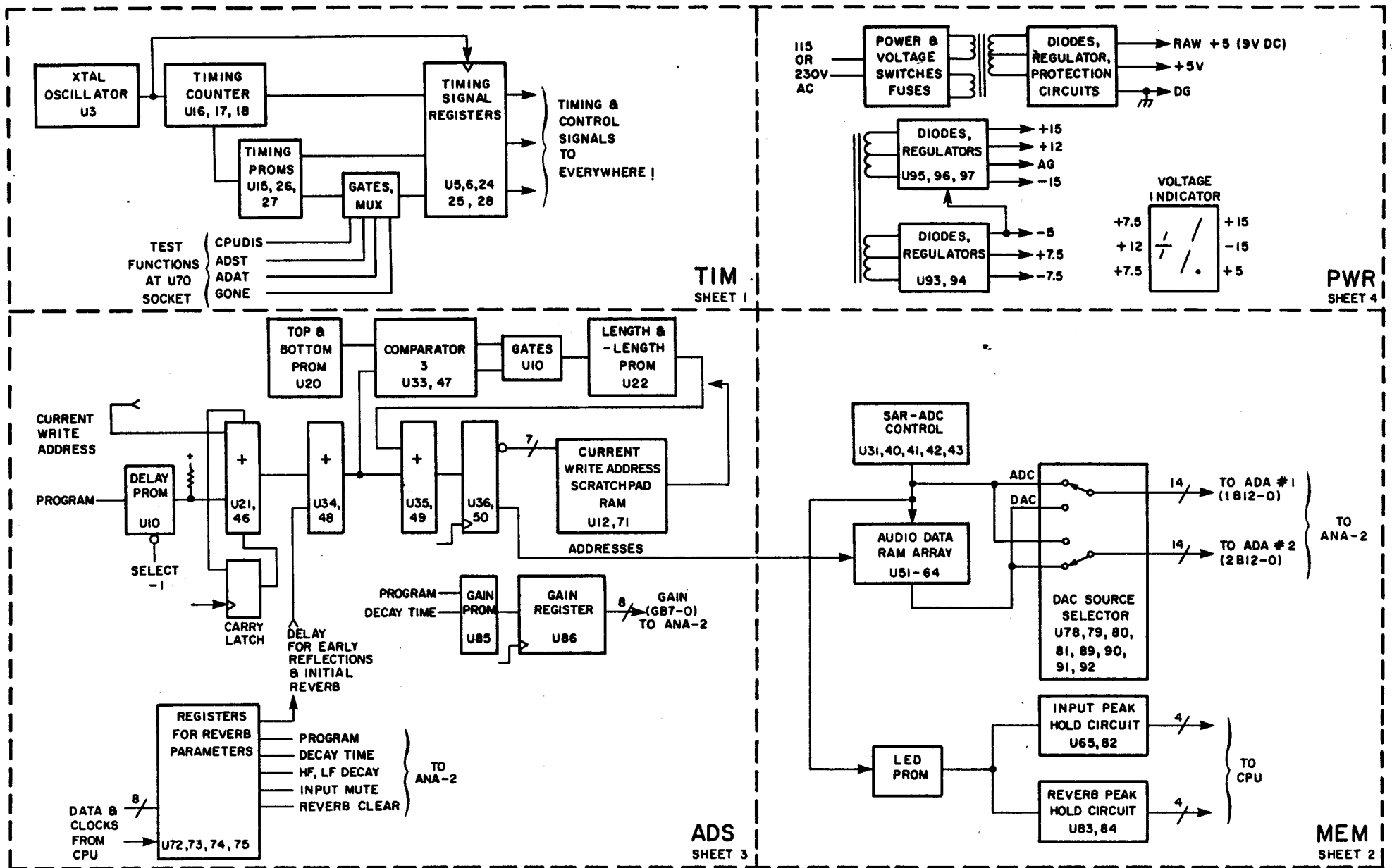
### ANA-2, FBC, (sheet 3)

Note 1: RV10 added to allow DC offset adjustment of signal APIN, in REV 3 boards. Earlier units had changes according to FSB #7 ("Buzz Saw Noise") so that RV4, offset adjust for C5IN, could also adjust APIN offset.

Note 2: R98 changed to 4.99K with .018 capacitor in parallel, and R9, 10 changed to 10.0K as part of FSB #10, "Reducing the Noise".

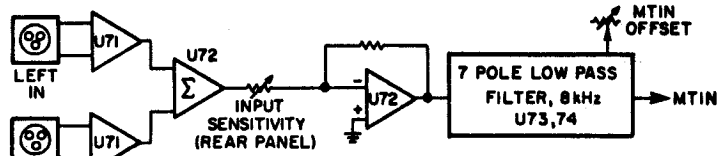


**8X32 DIGITAL REVERBERATOR  
 System Block Diagram**

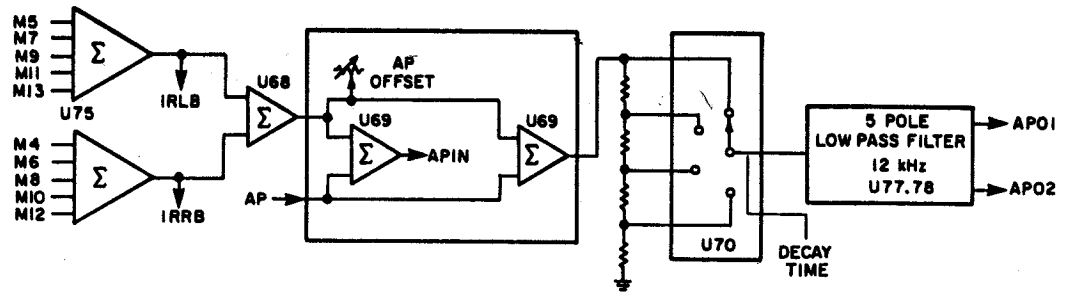


8X32 DIGITAL REVERBERATOR  
Motherboard (MOM-2) Block Diagram

### INPUT CIRCUITS

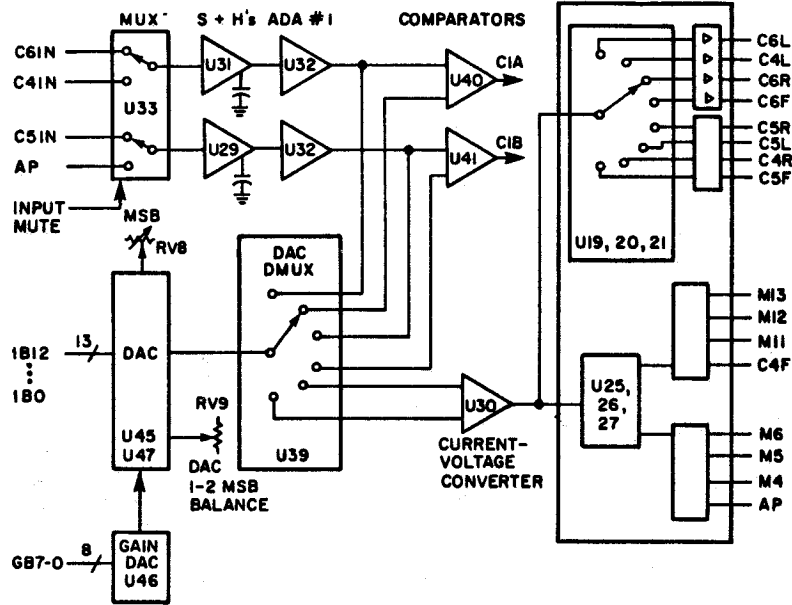


### ALL PASS CIRCUITS

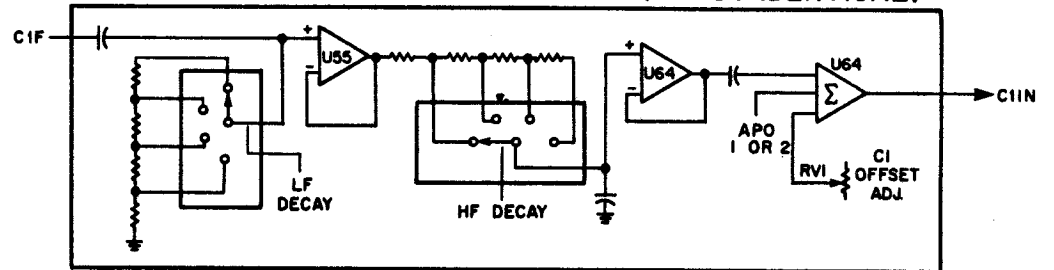


### AD & DA CONVERTERS

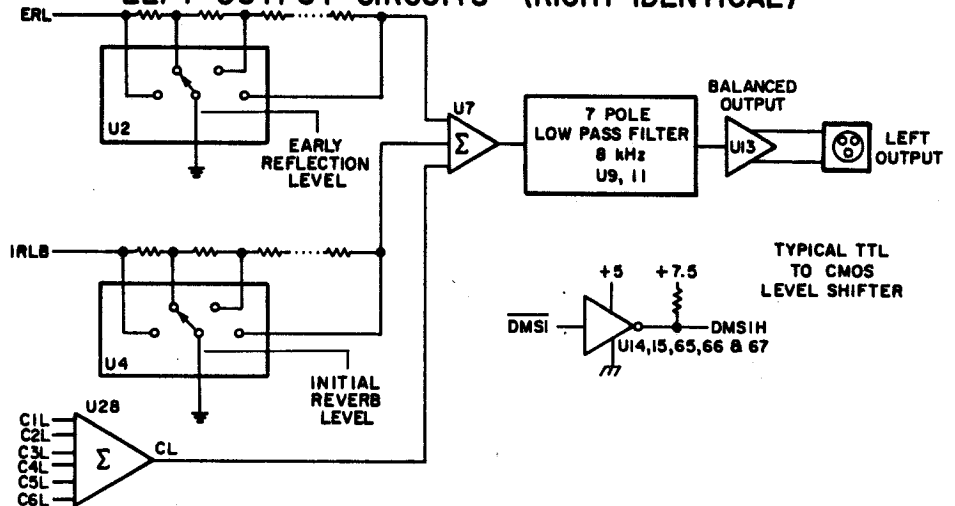
### DA SAMPLE & HOLDS



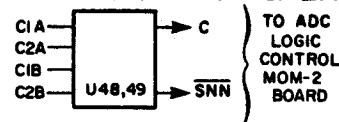
### CF FEEDBACK CIRCUIT-C1 ONLY DRAWN (C2-C6 IDENTICAL)



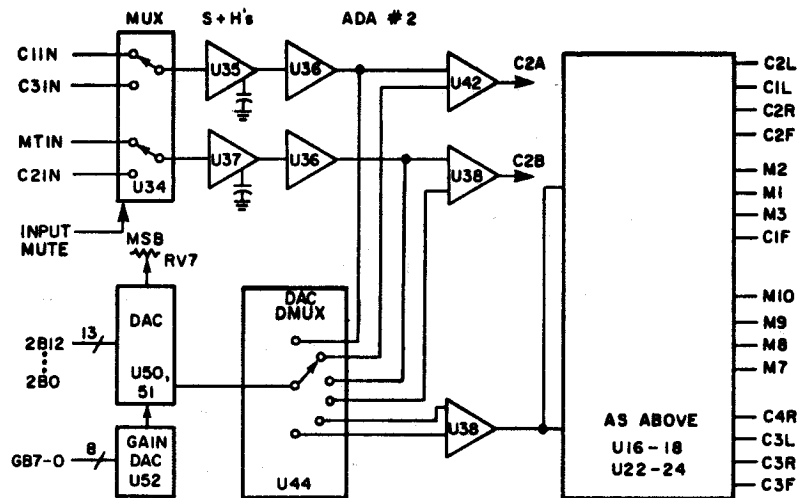
### LEFT OUTPUT CIRCUITS - (RIGHT IDENTICAL)

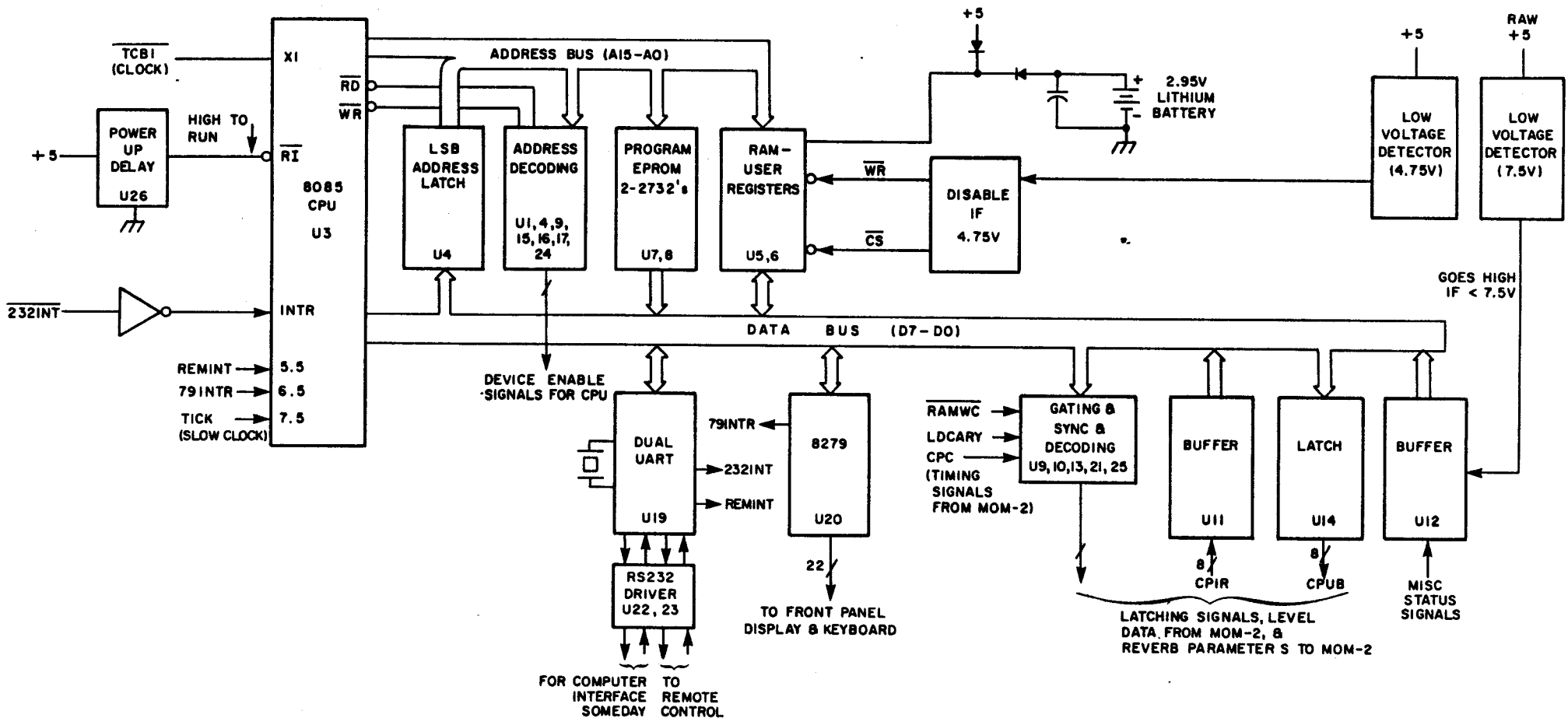


### COMPARATOR MUX & LATCH

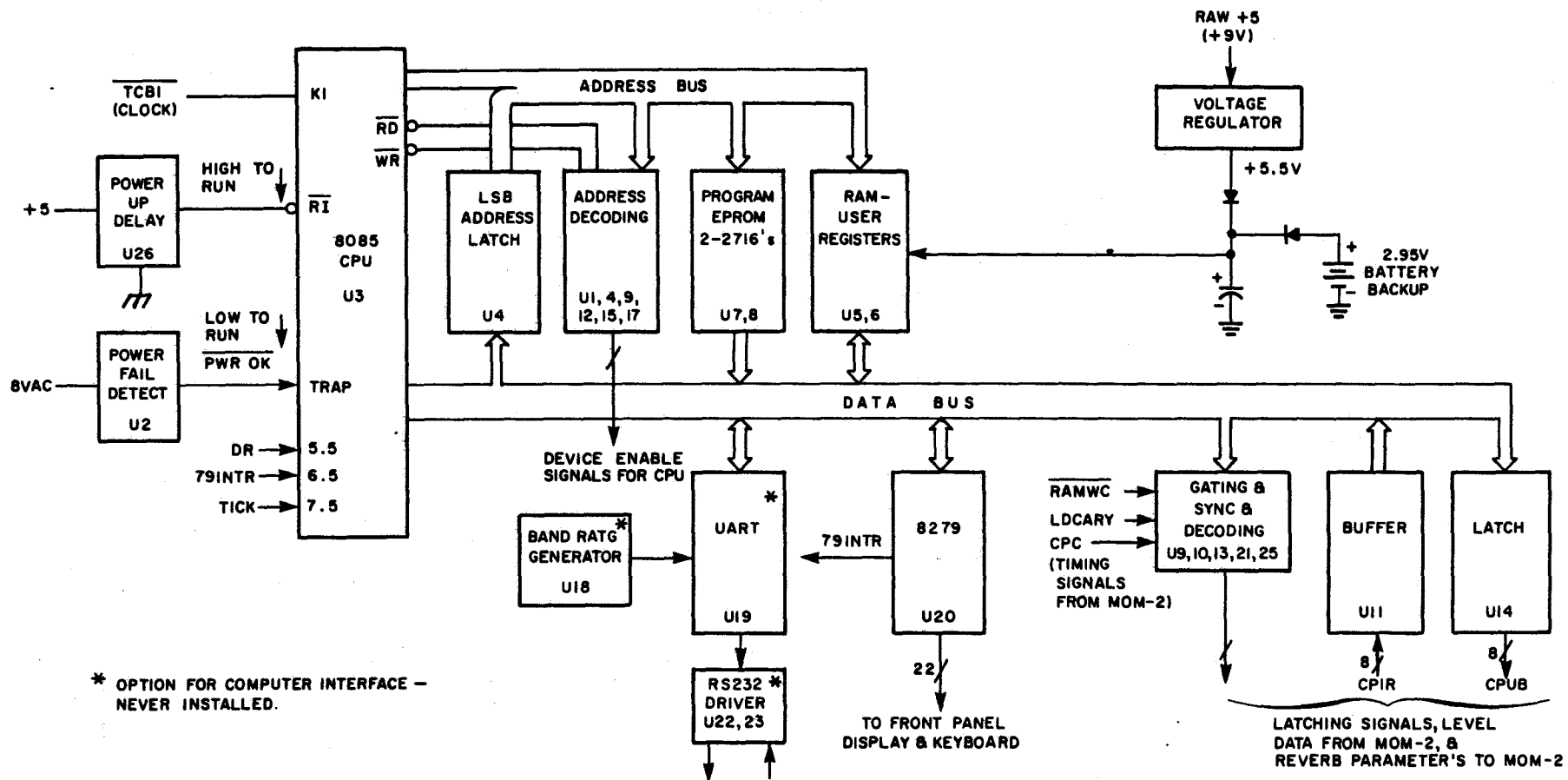


### 8X32 DIGITAL REVERBERATOR ANA-2 Block Diagram



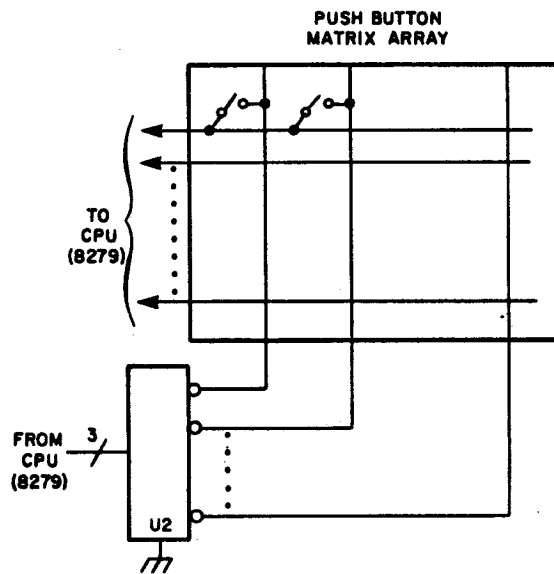


**8X32 DIGITAL REVERBERATOR**  
**CPU-1 Block Diagram**  
 REV 2 (LATER REV)  
 OK FOR USE WITH REMOTE

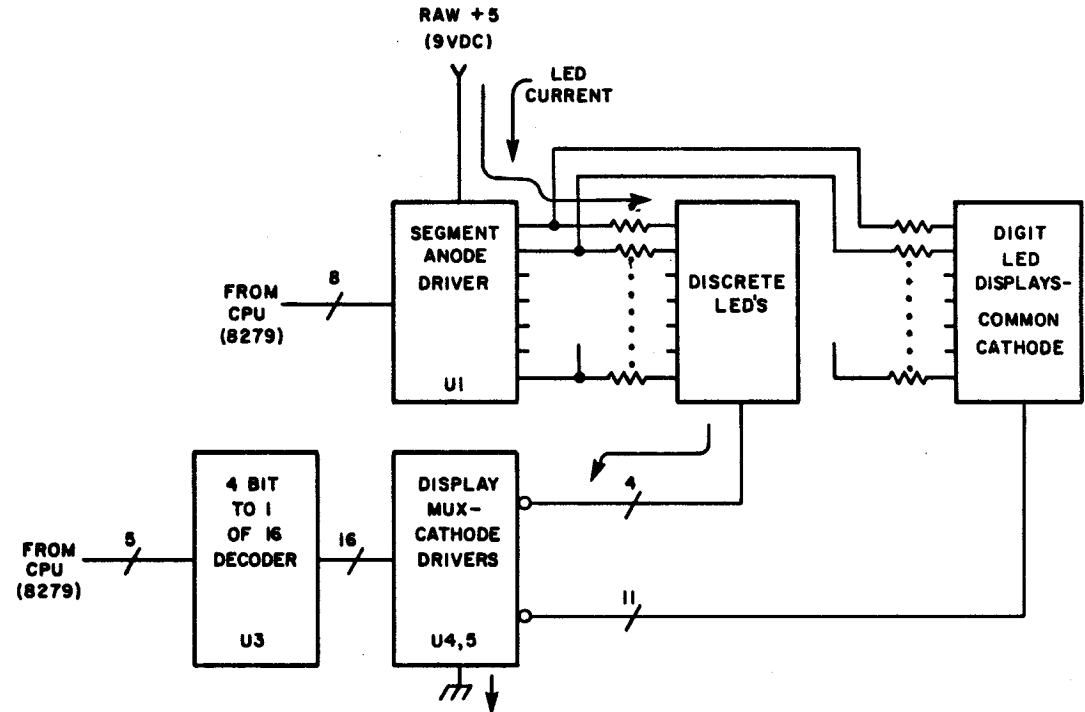


8X32 DIGITAL REVERBERATOR  
CPU-1 Block Diagram  
REV.1 (EARLY REV.)

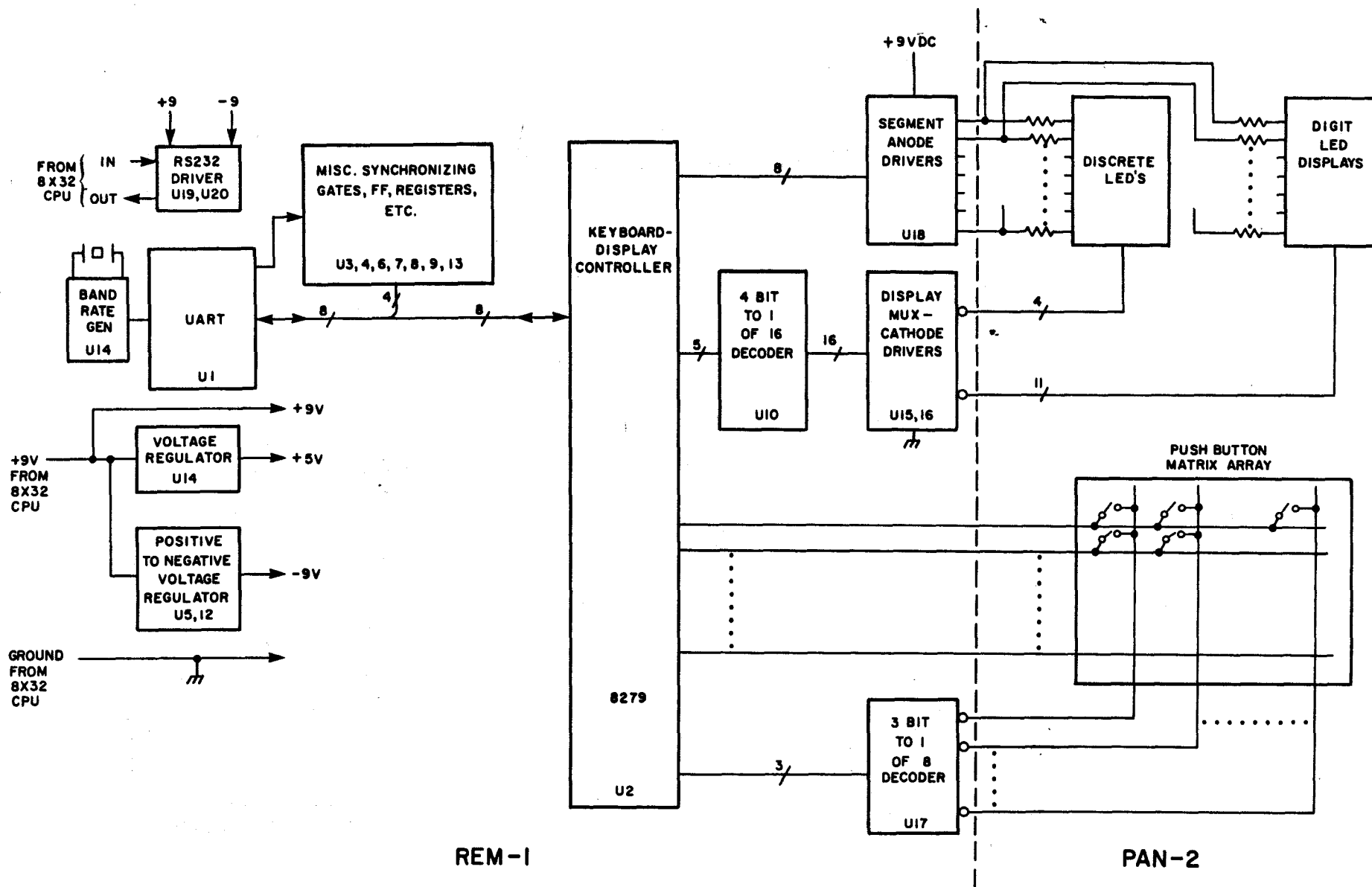
**SCANNED KEYBOARD  
MATRIX ARRAY**



**MULTIPLEXED  
DISPLAY & DRIVERS**



**8X32 DIGITAL REVERBERATOR  
PAN-1 Block Diagram**

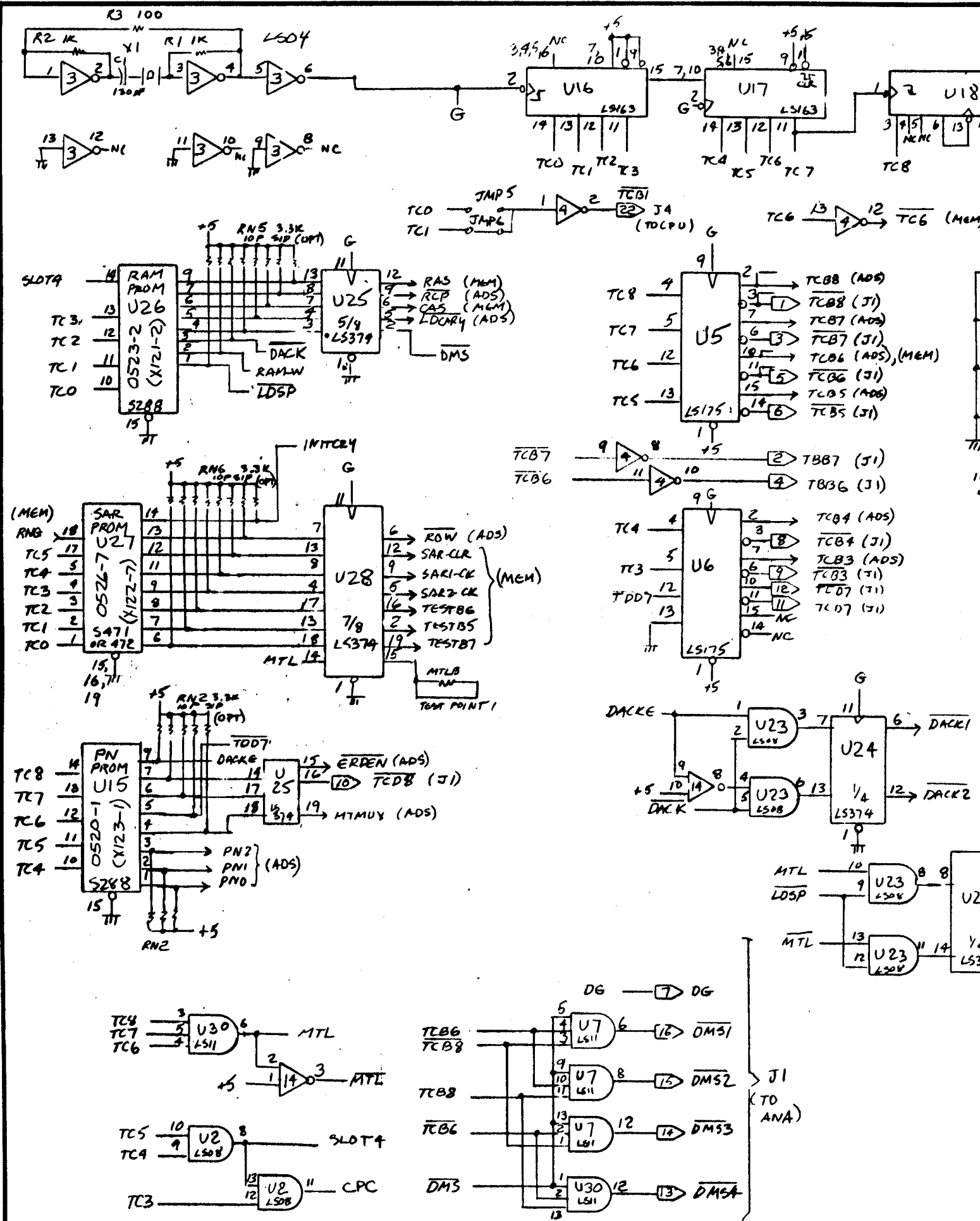


REM-1

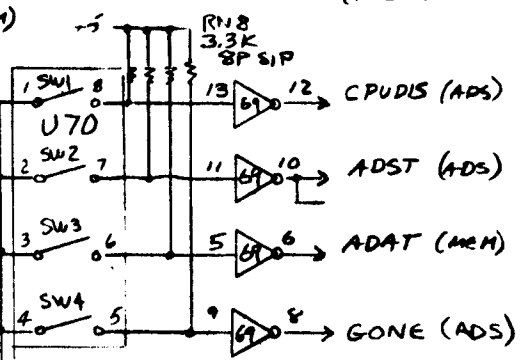
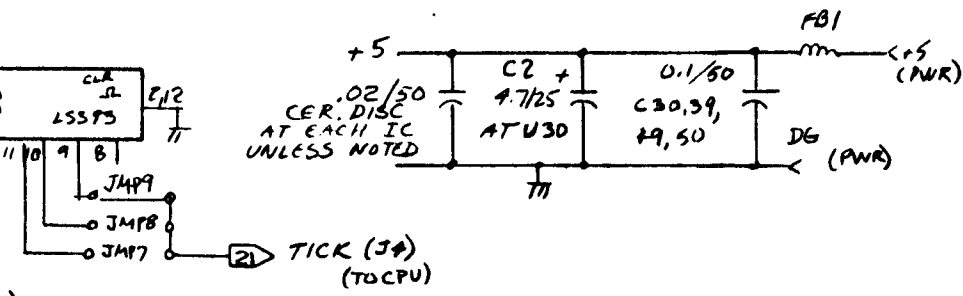
PAN-2

8X32 DIGITAL REVERBERATION SYSTEM  
Remote Block Diagram

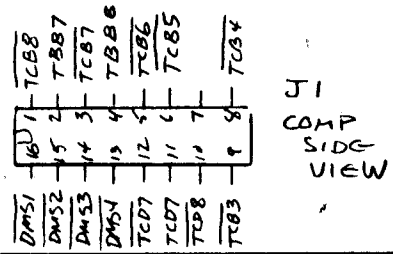
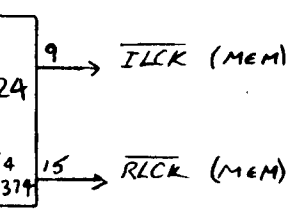
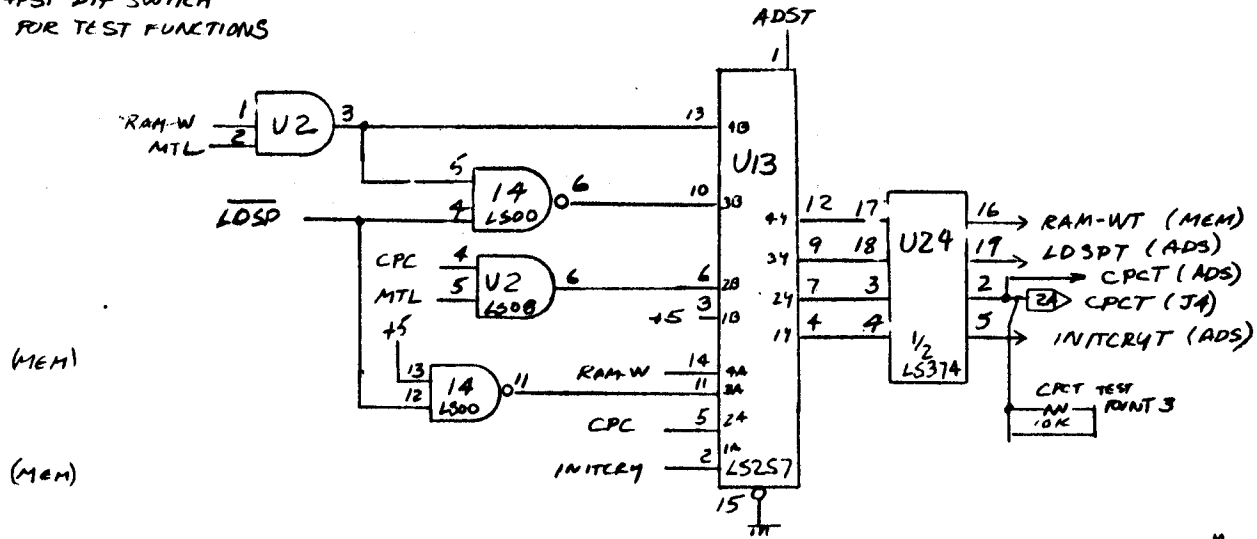




SEPT. 28, 83

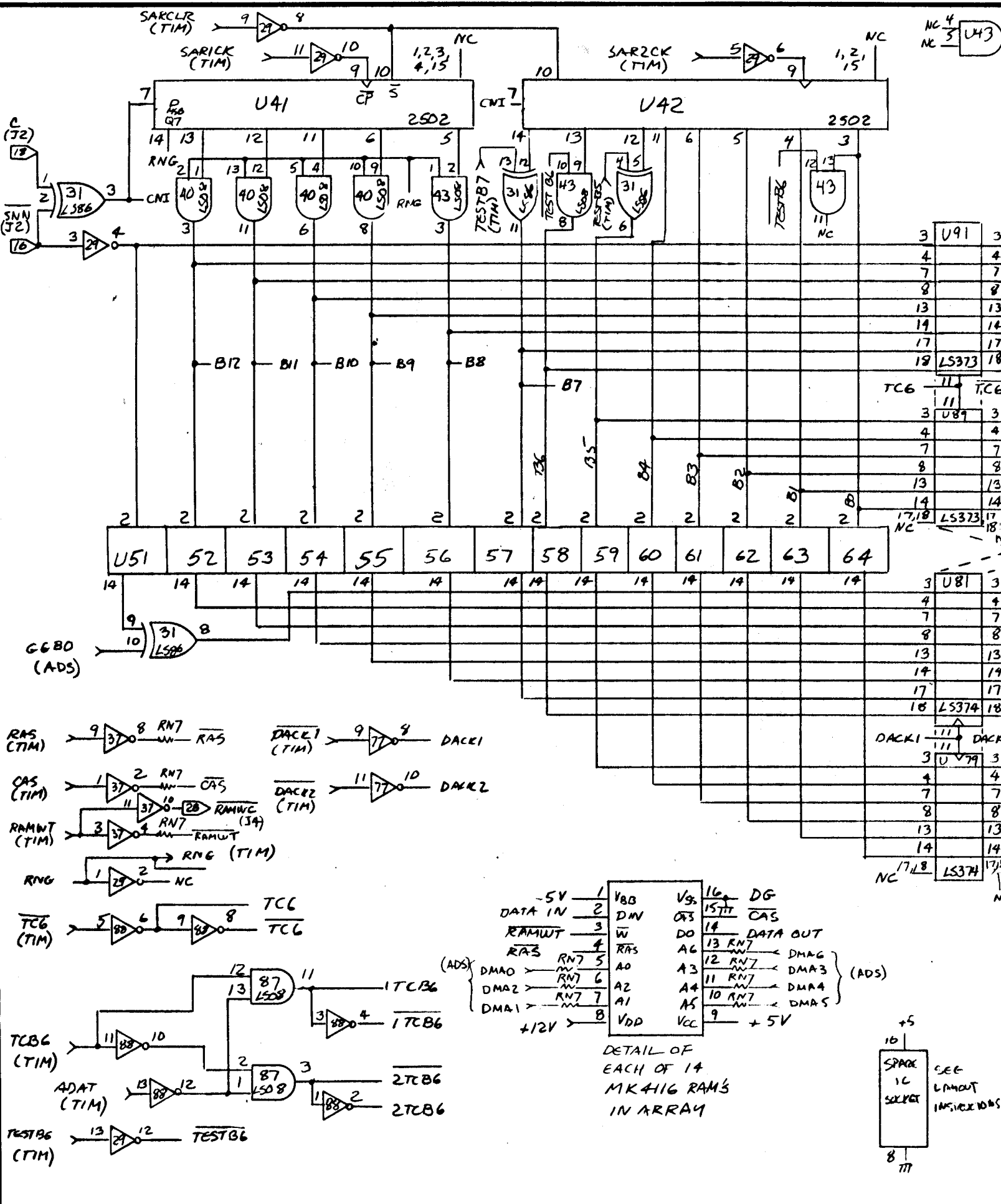


9 PIN IC SOCKET  
INSTALL 8 PIN, 4PST DIP SWITCH FOR TEST FUNCTIONS



3	LS374	20V
2	LS175	16
2	LS00	14
2	LS08	14
2	LS11	14
2	S288	16
2	S471	20
2	LS163	16
1	LS373	14
2	LS04	14
1	309	14
1	LS257	16

<b>8 x 32</b>		
SCALE: —	APPROVED BY	DRAWN BY CM
DATE: 27 JAN 81	LAST REV: SEPT. 28, 1983	
<b>MOM-2, TIM (SHEET 1 OF 4)</b>		
VRSMA MAJOR, INC BOX 18 BELMONT MA 02178 USA		DRAWING NUMBER <b>0366</b>

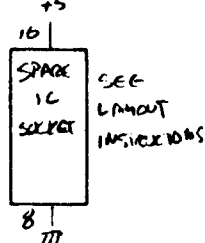


NC 4  
5 U43  
NC

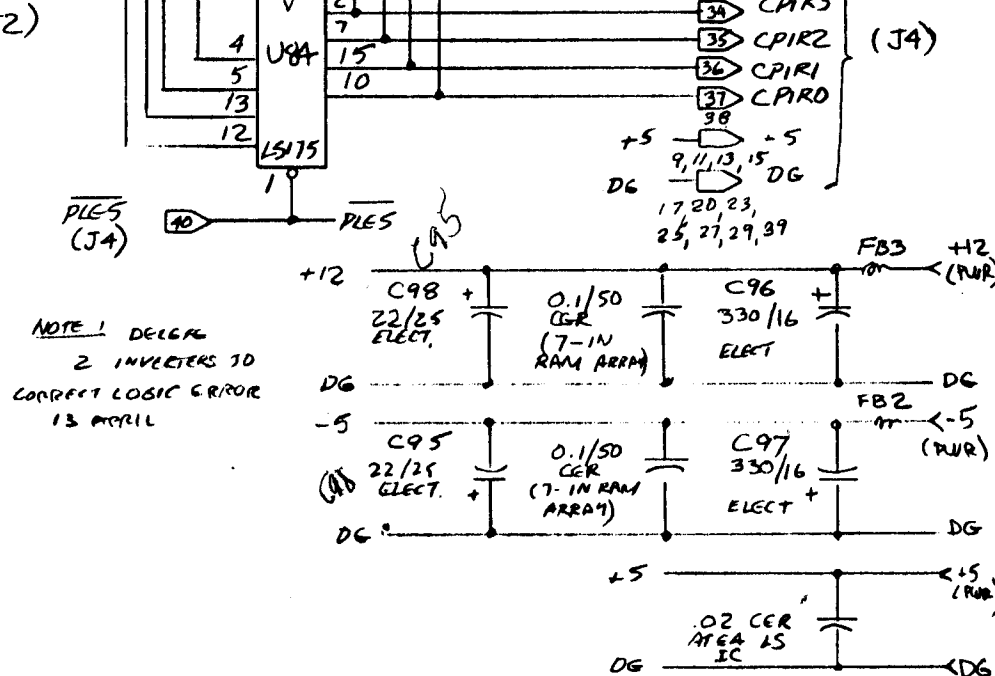
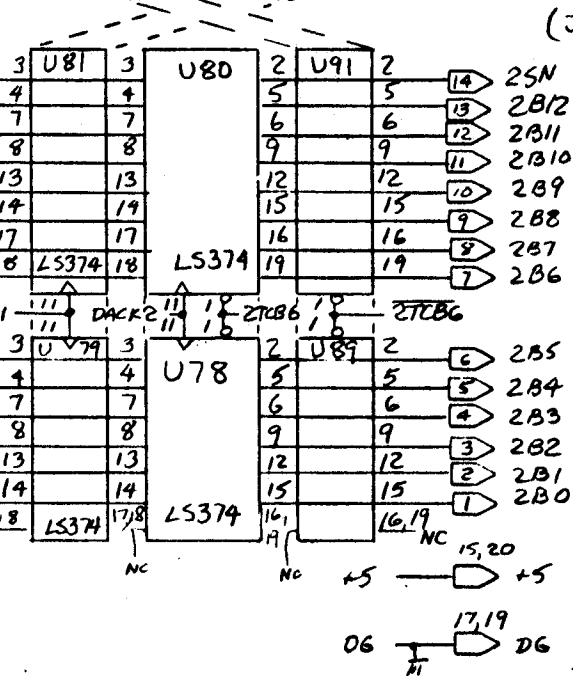
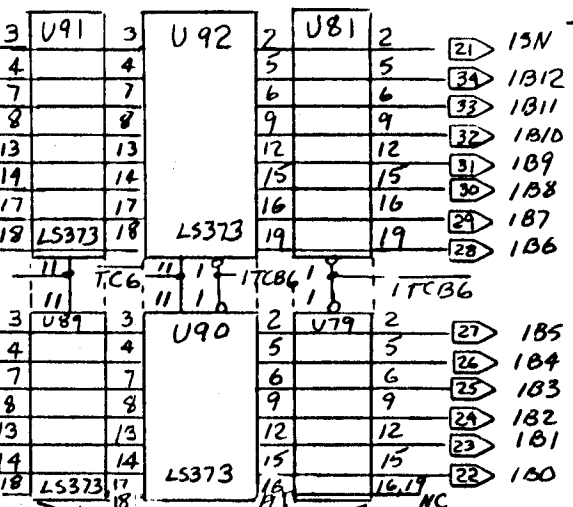
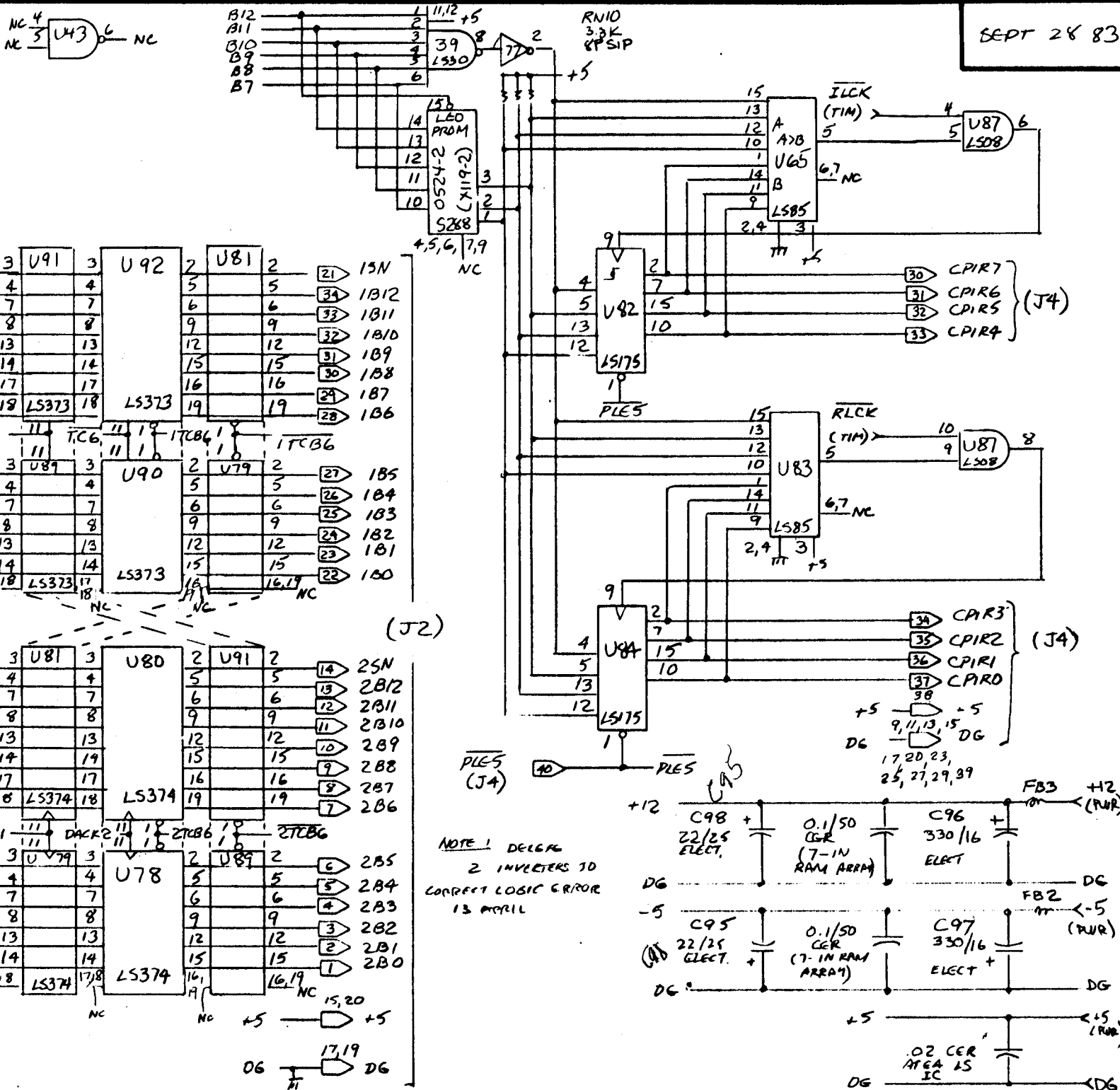
3	U41	3
4		4
7		7
8		8
13		13
14		14
17		17
18	LS373	18
TC6	11	TC6
3	U89	3
4		4
7		7
8		8
13		13
14		14
17,18	LS373	17,18
NC		NC
3	U81	3
4		4
7		7
8		8
13		13
14		14
17		17
18	LS374	18
DAK1	111	DAK1
3	U79	3
4		4
7		7
8		8
13		13
14		14
NC	17,18	LS374
		17,18
		NC

-5V	1	V <sub>B0</sub>	16	DG
DATA IN	2	D <sub>IN</sub>	15	TT CAS
RAMWT	3	W	14	DATA OUT
RAS	4	RAS	13	RN7 < DMA0
DMA0	RN7	A0	12	RN7 < DMA3
DMA2	RN7	A2	11	RN7 < DMA4
DMA1	RN7	A1	10	RN7 < DMA5
+12V	8	V <sub>DD</sub>	9	+5V

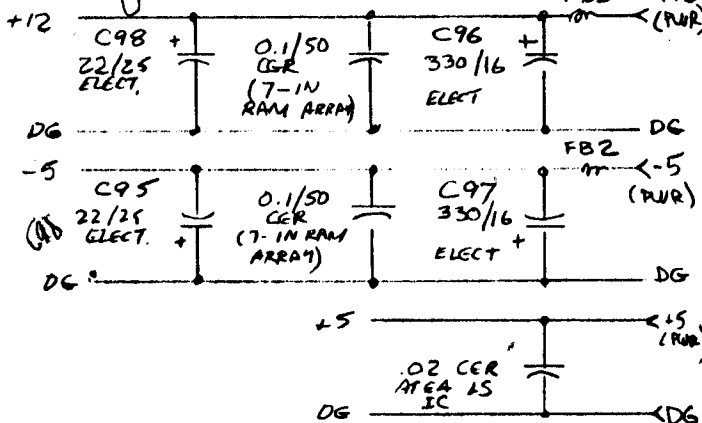
DETAIL OF EACH OF 14 MK416 RAM'S IN ARRAY



SEPT 28 83



NOTE 1 DELGK  
2 INVERTERS TO  
CORRECT LOGIC ERROR  
13 APRIL

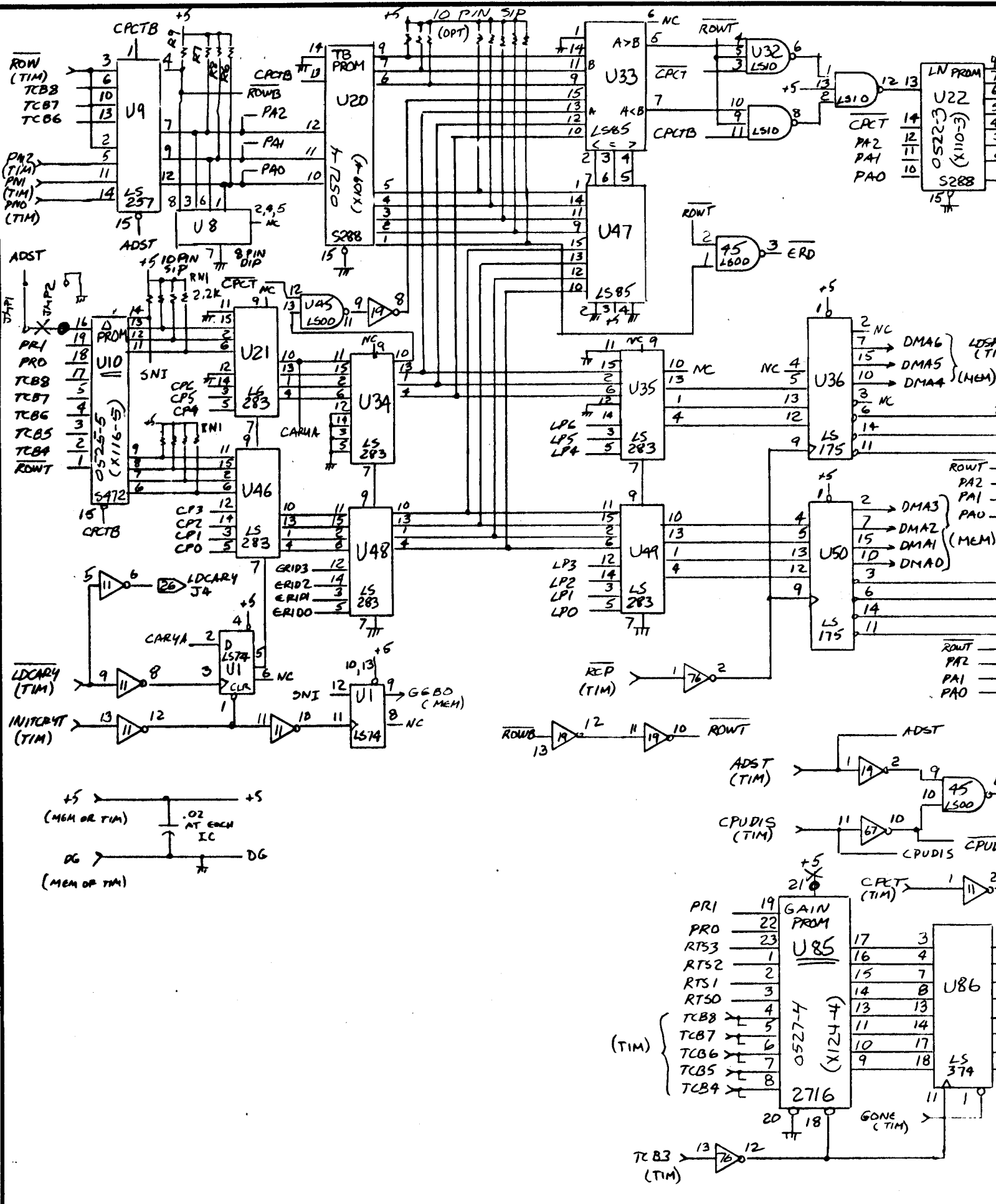


- 14-MK4116 16F
- 4-LS04 14P
- 3-LS08 14P
- 2-LS85 16P
- 2-LS175 16P
- 4-LS373 20P
- 4-LS374 20P
- 2-2502 16P
- 1-LS86 14P
- 1-LS288 16P
- 1-LS30 14P

8 X 32

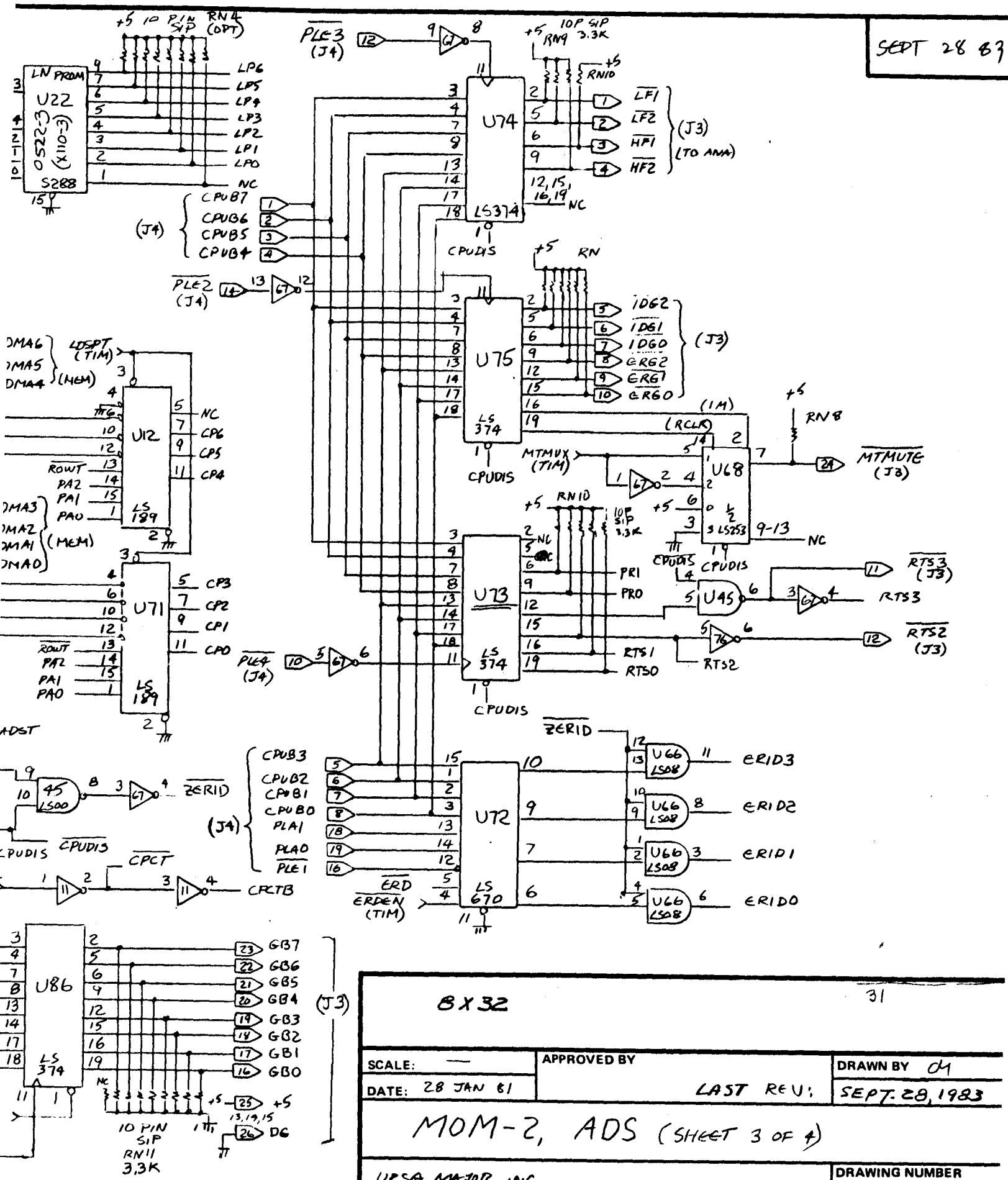
SCALE: —	APPROVED BY	DRAWN BY CM
DATE: 27 JAN 81	LAST REV: SEPT. 28, 1983	
MOM-2, MEM (SHEET 2 OF 4)		
URSA MAJOR, INC BOX 18 BELMONT MA 02178 USA		DRAWING NUMBER <span style="font-size: 24pt; font-weight: bold;">0367</span>

SEE LAYOUT  
INSTRUCTIONS



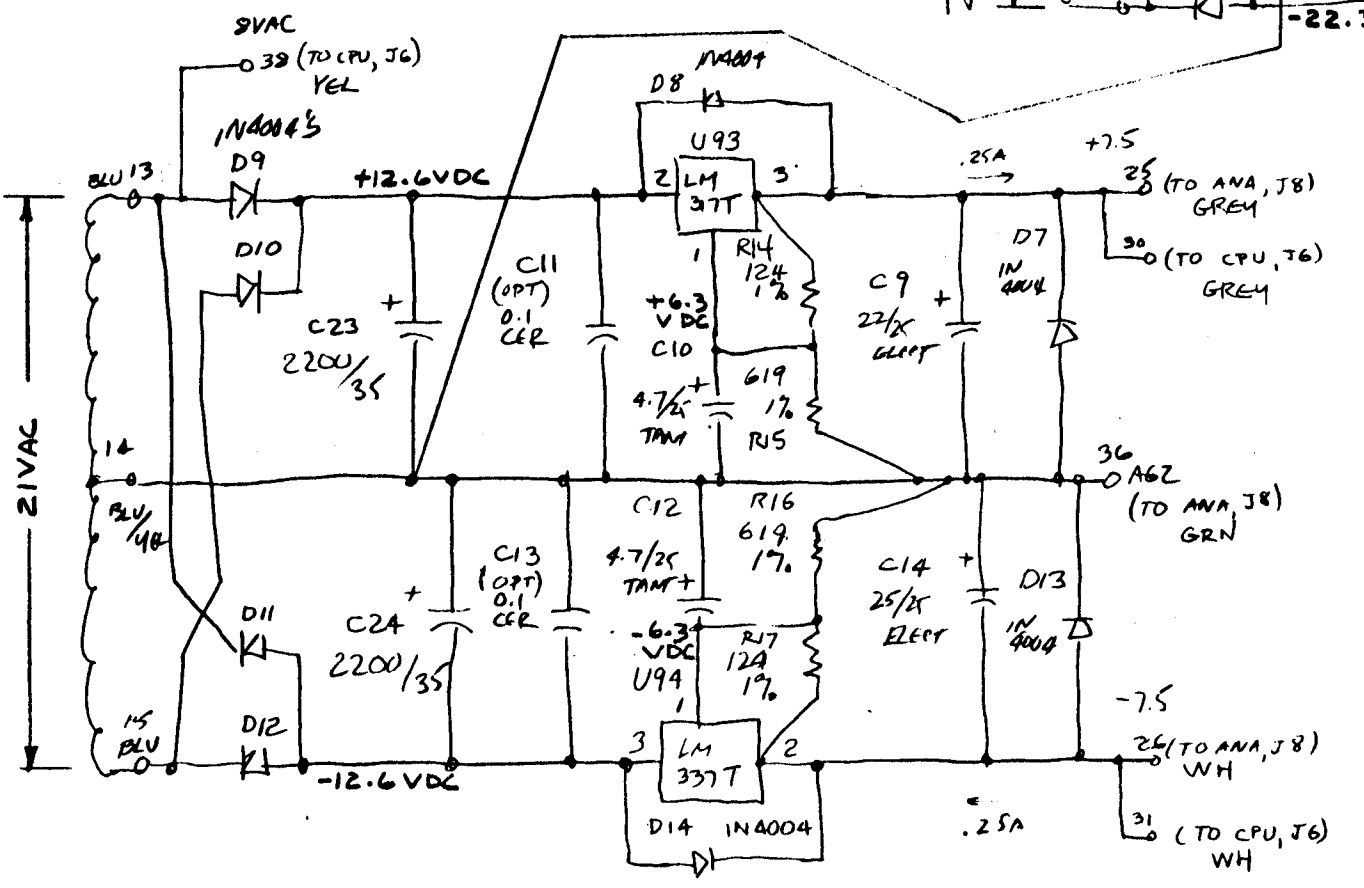
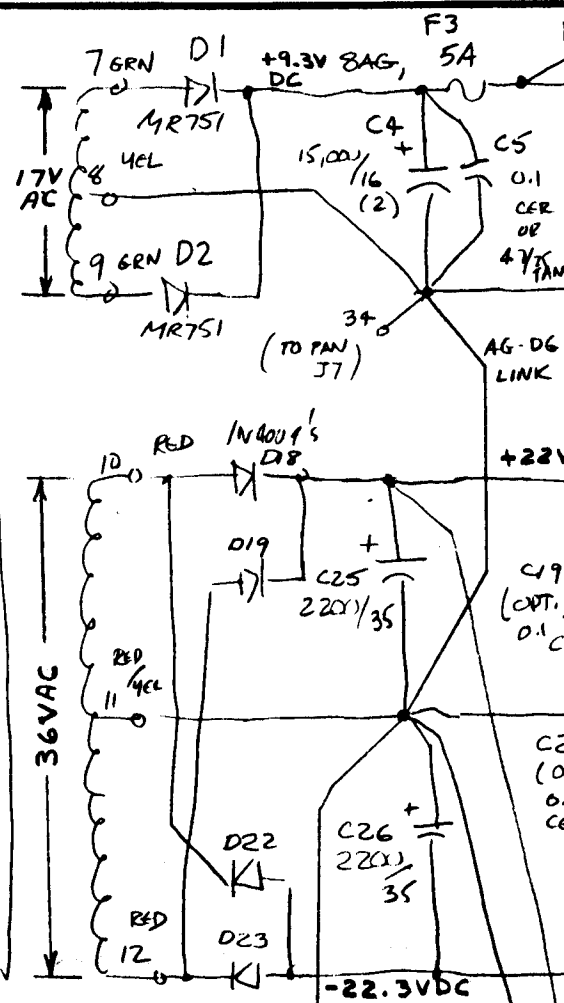
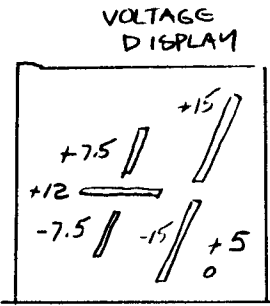
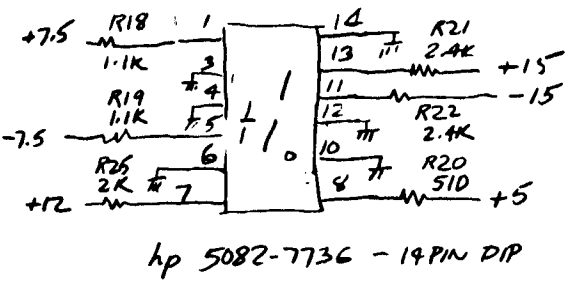
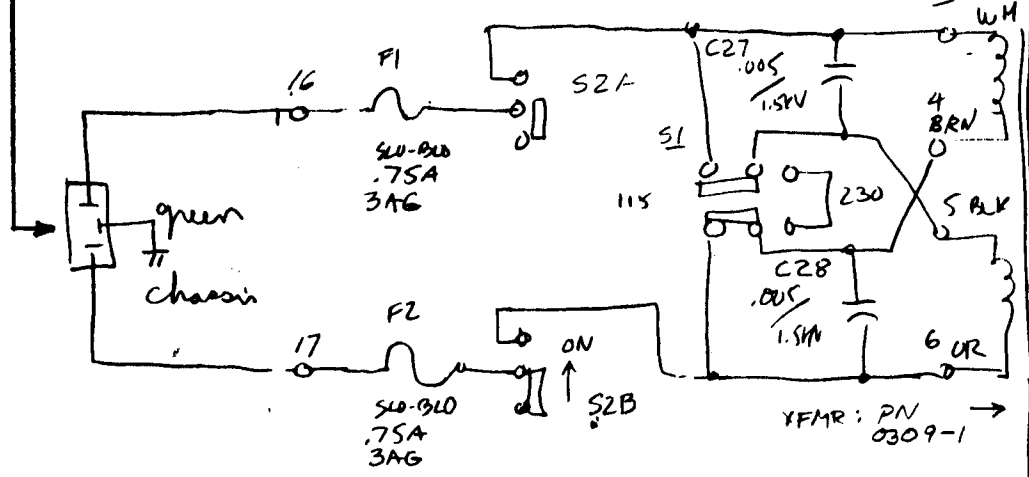
DIETZGEN MASTER FORM 198MF

SEPT 28 83



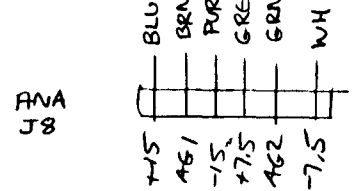
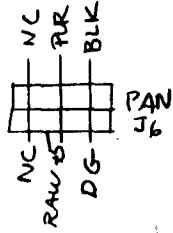
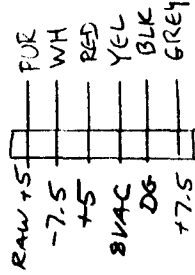
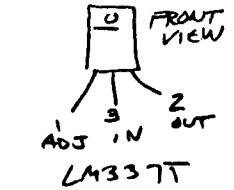
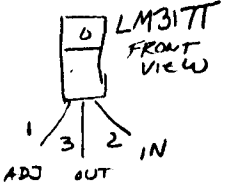
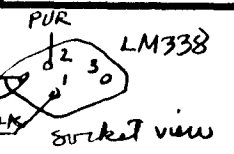
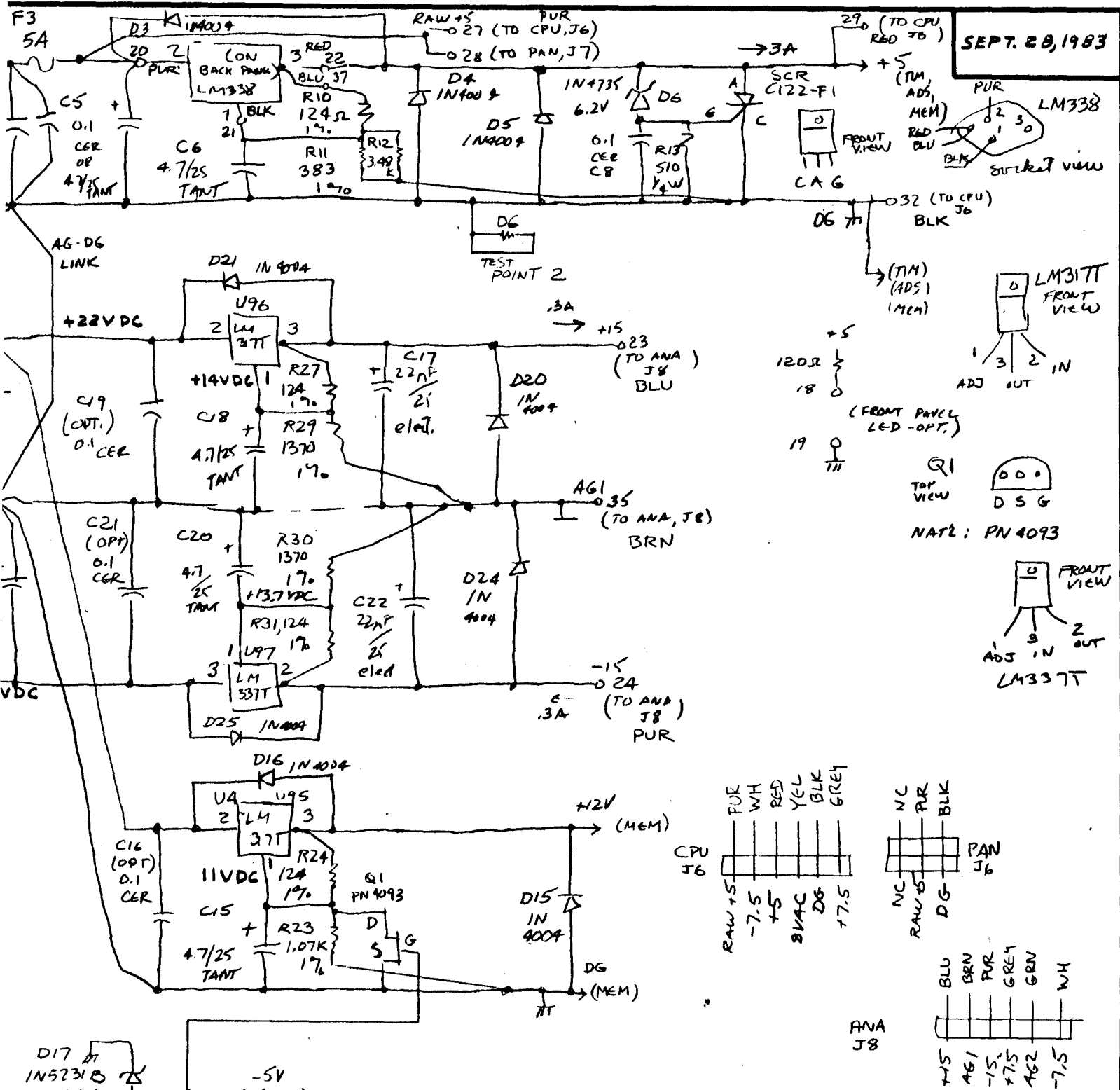
<b>8x32</b>		31
SCALE: —	APPROVED BY	DRAWN BY <i>cl</i>
DATE: 28 JAN 81	LAST REV:	SEPT. 28, 1983
<b>MOM-2, ADS (SHEET 3 OF 4)</b>		
URSA MAJOR INC Box 18 BELMONT MA 02178 USA		DRAWING NUMBER <b>0368</b>

DC RESISTANCE, COLD:  
 115 V SETTING: 5.27Ω  
 230V SETTING: 15.7Ω



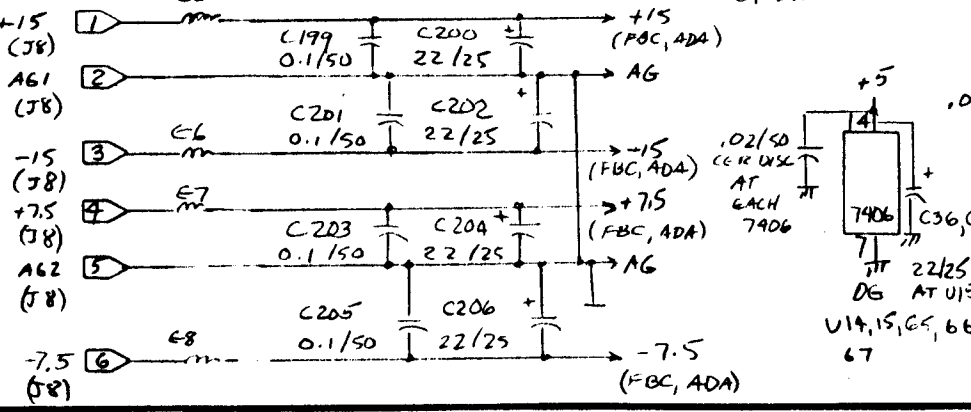
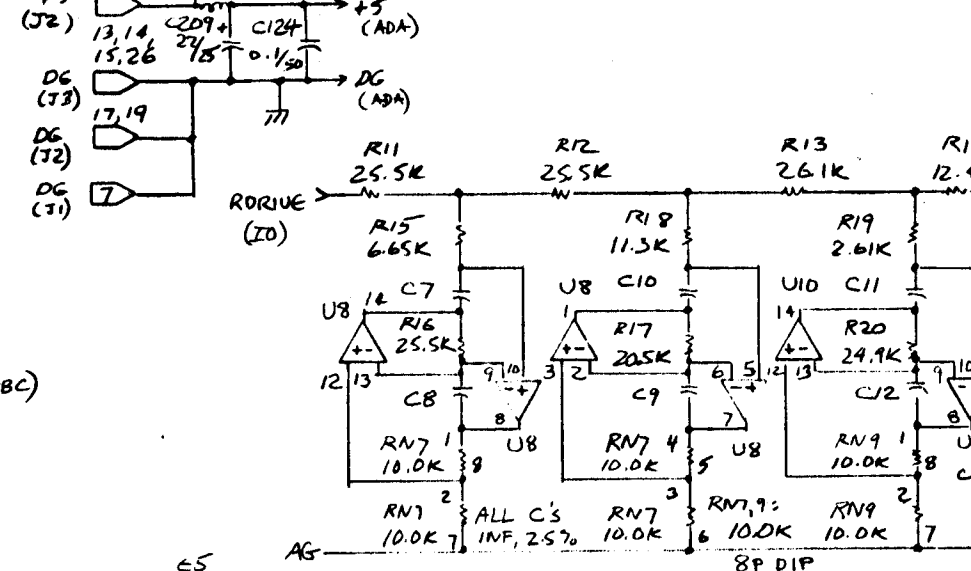
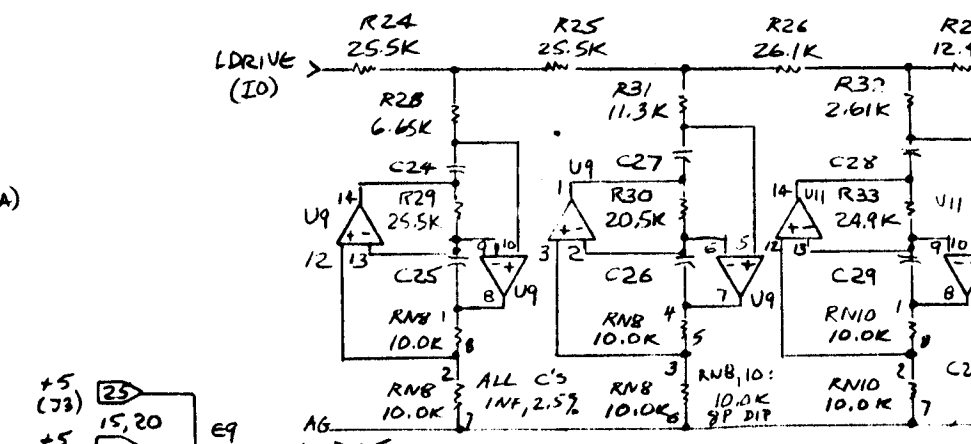
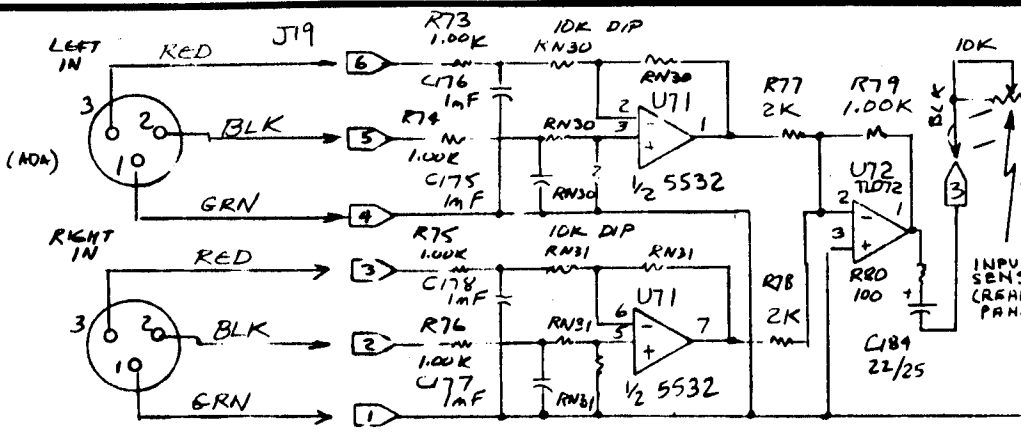
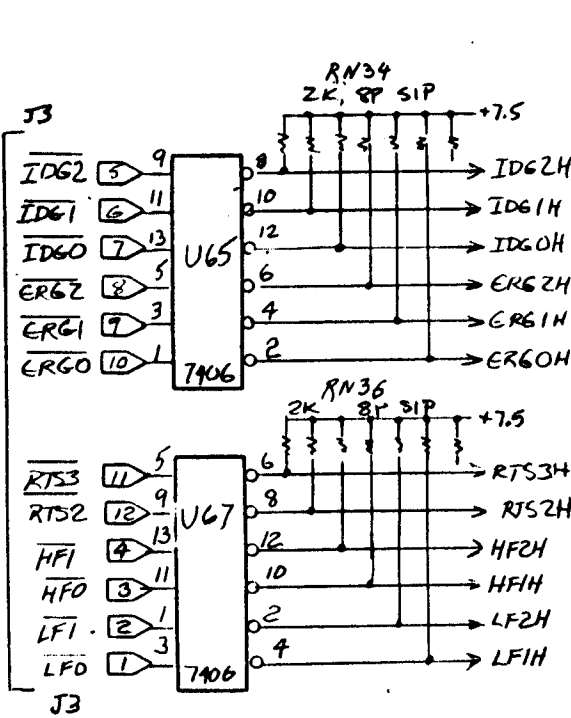
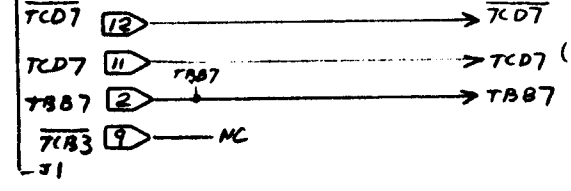
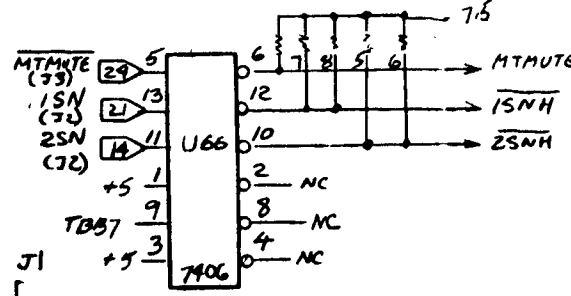
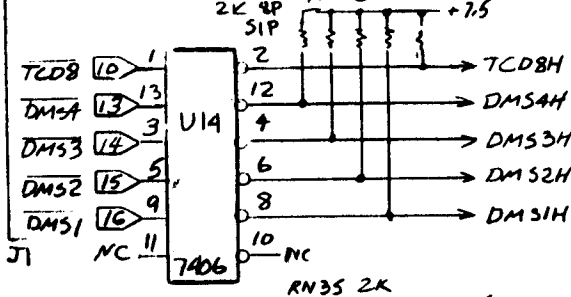
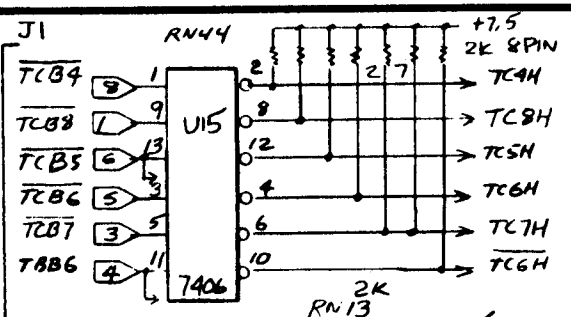
D17 1N5231R  
 5.1V  
 R21 270Ω  
 57

SEPT. 28, 1983

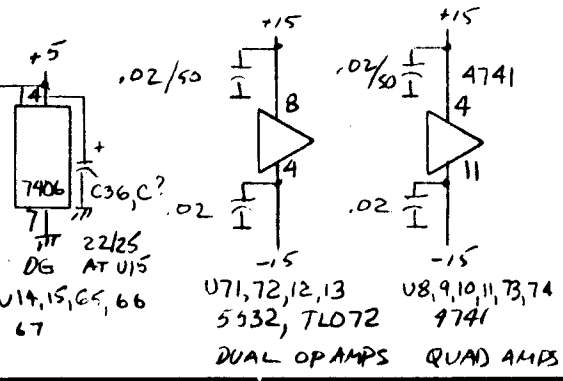
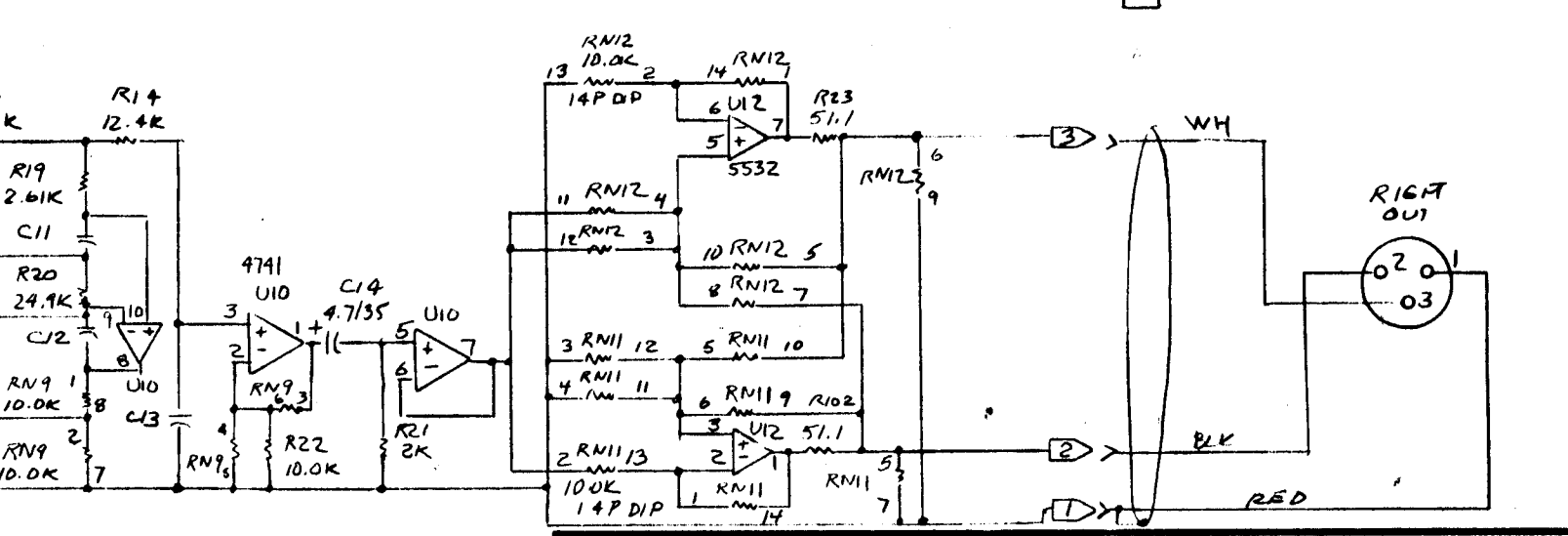
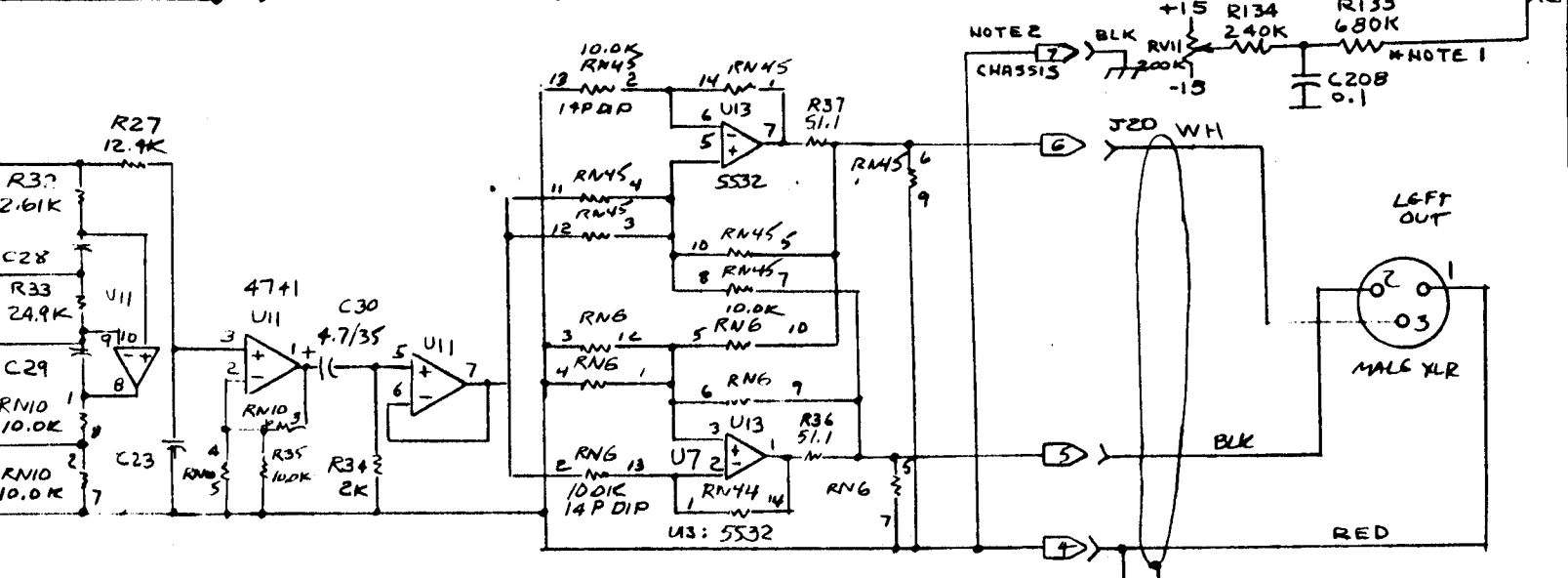
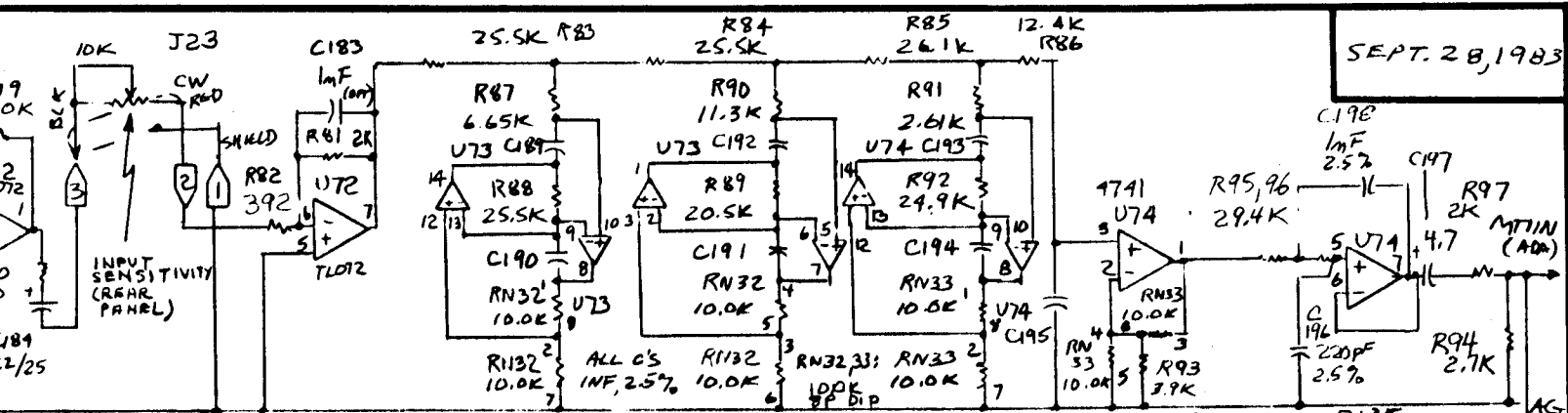


8 x 32		
SCALE: —	APPROVED BY	DRAWN BY <i>CM</i>
DATE: 25 Dec 80	LAST REV:	SEPT. 28, 1983
MOM-2, PWR (SHEET 4 OF 4)		
URSA MAJOR INC BOX 18 BELMONT MA 02178 USA		DRAWING NUMBER <b>0369</b>



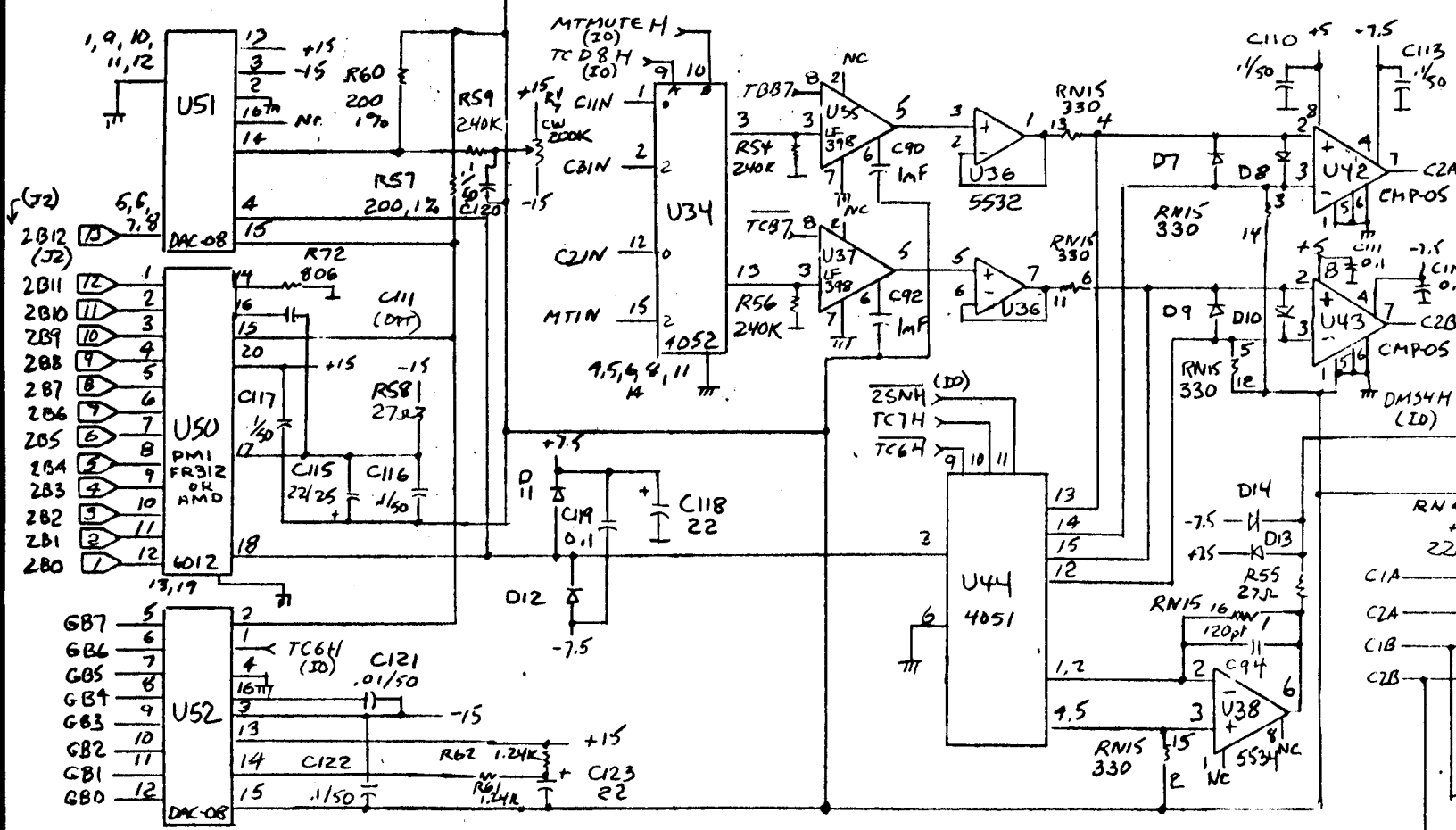
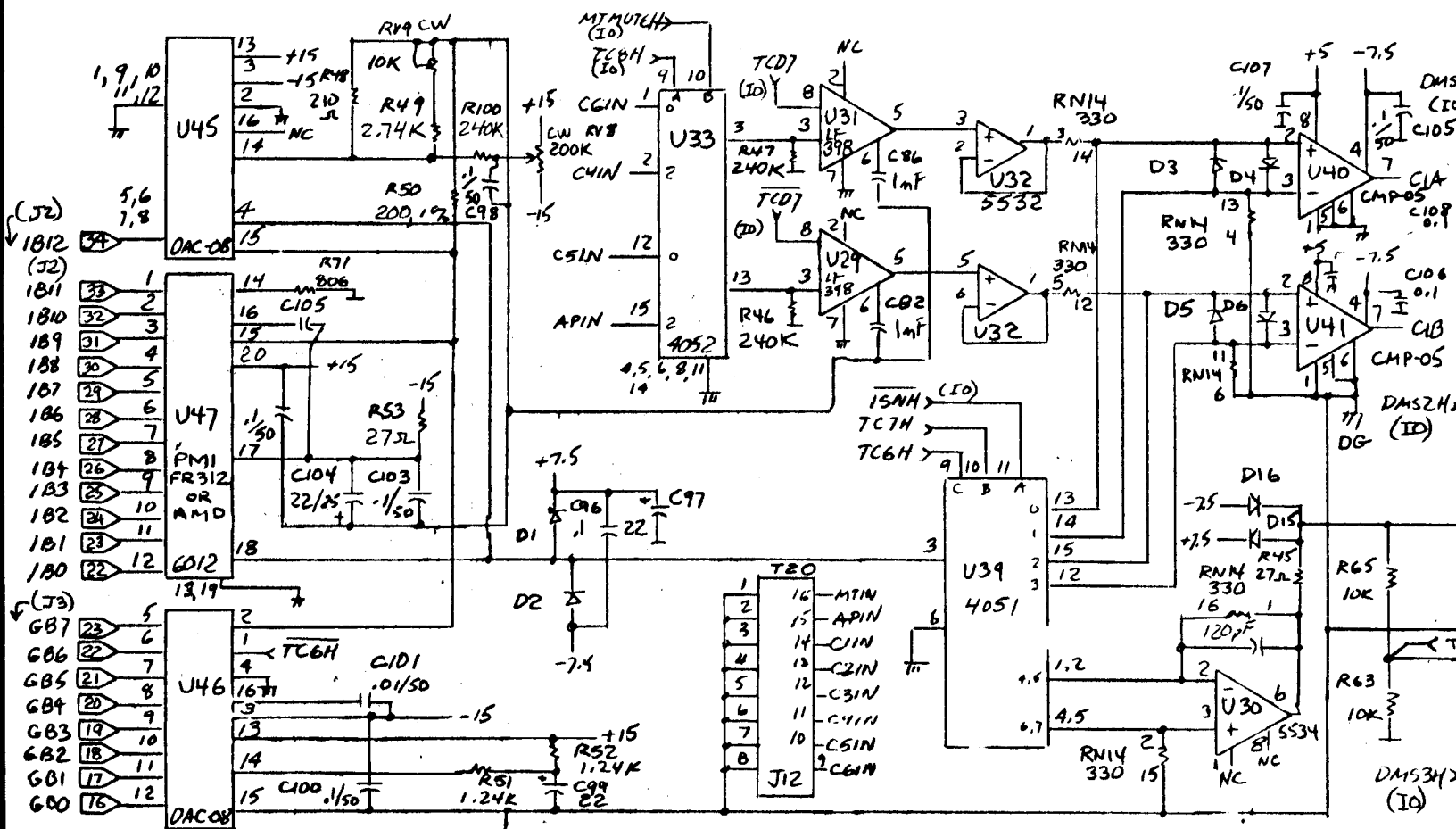


SEPT. 28, 1983

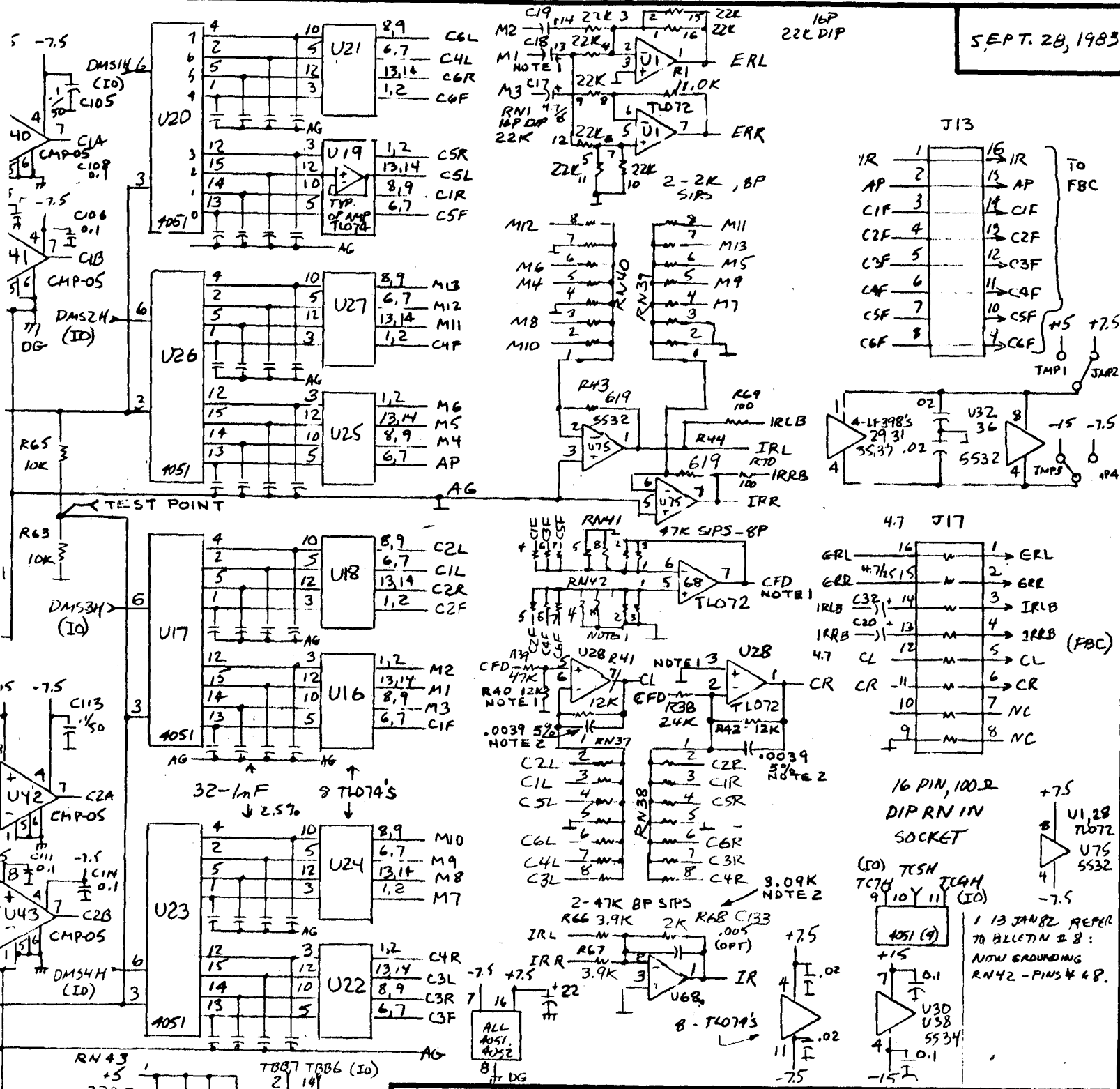


**8X32**

SCALE: ~	APPROVED BY	DRAWN BY CM
DATE: 17 FEB 81		REV: SEPT. 28, 1983
<b>ANA-2, IO, (SHEET 1 OF 3)</b>		
URSA MAJOR, Inc BOX 18 BELMONT MA 02178 USA		DRAWING NUMBER <b>0397</b>

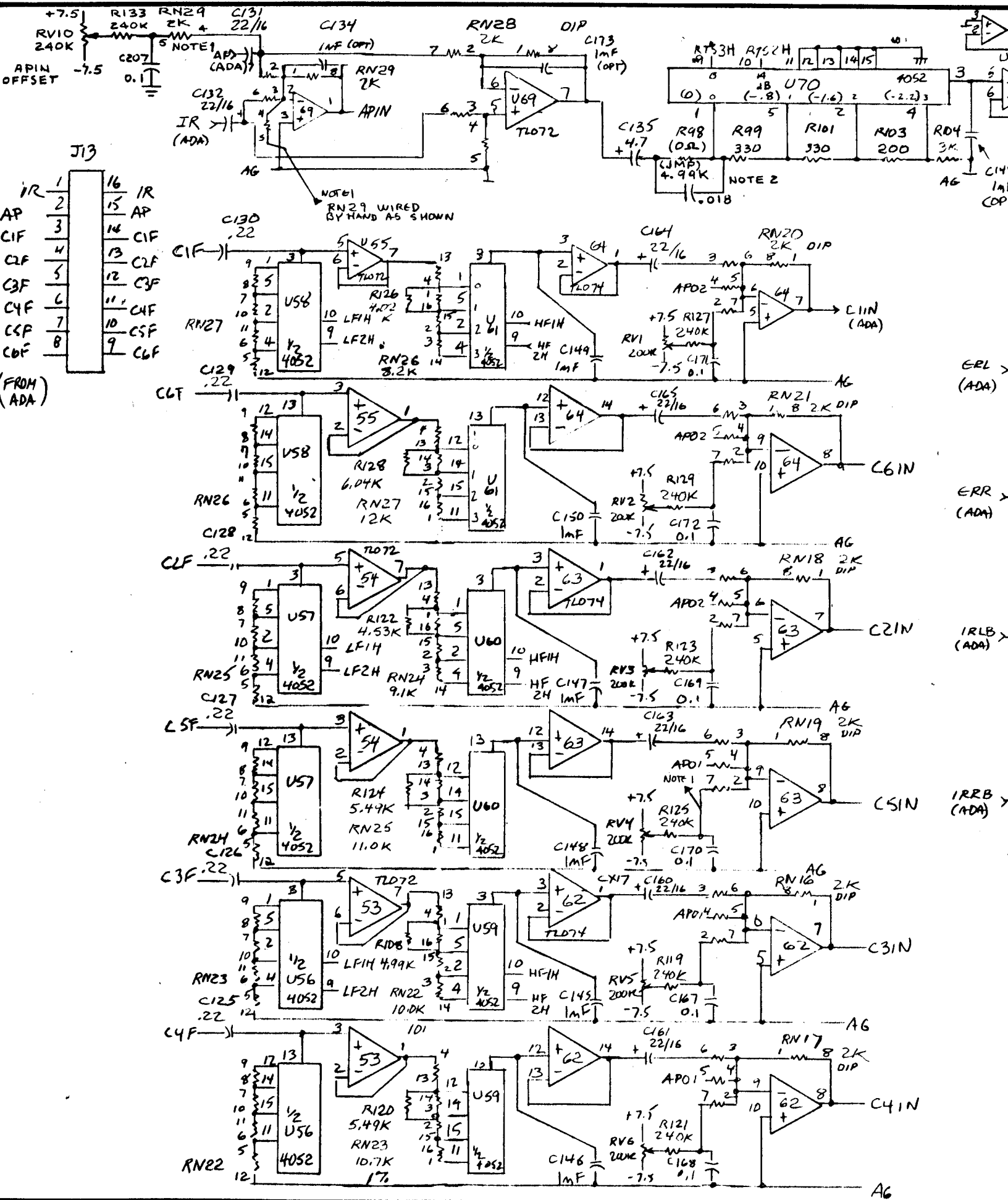


SEPT. 28, 1983



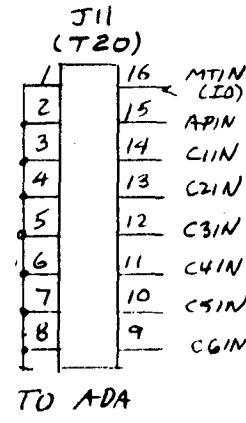
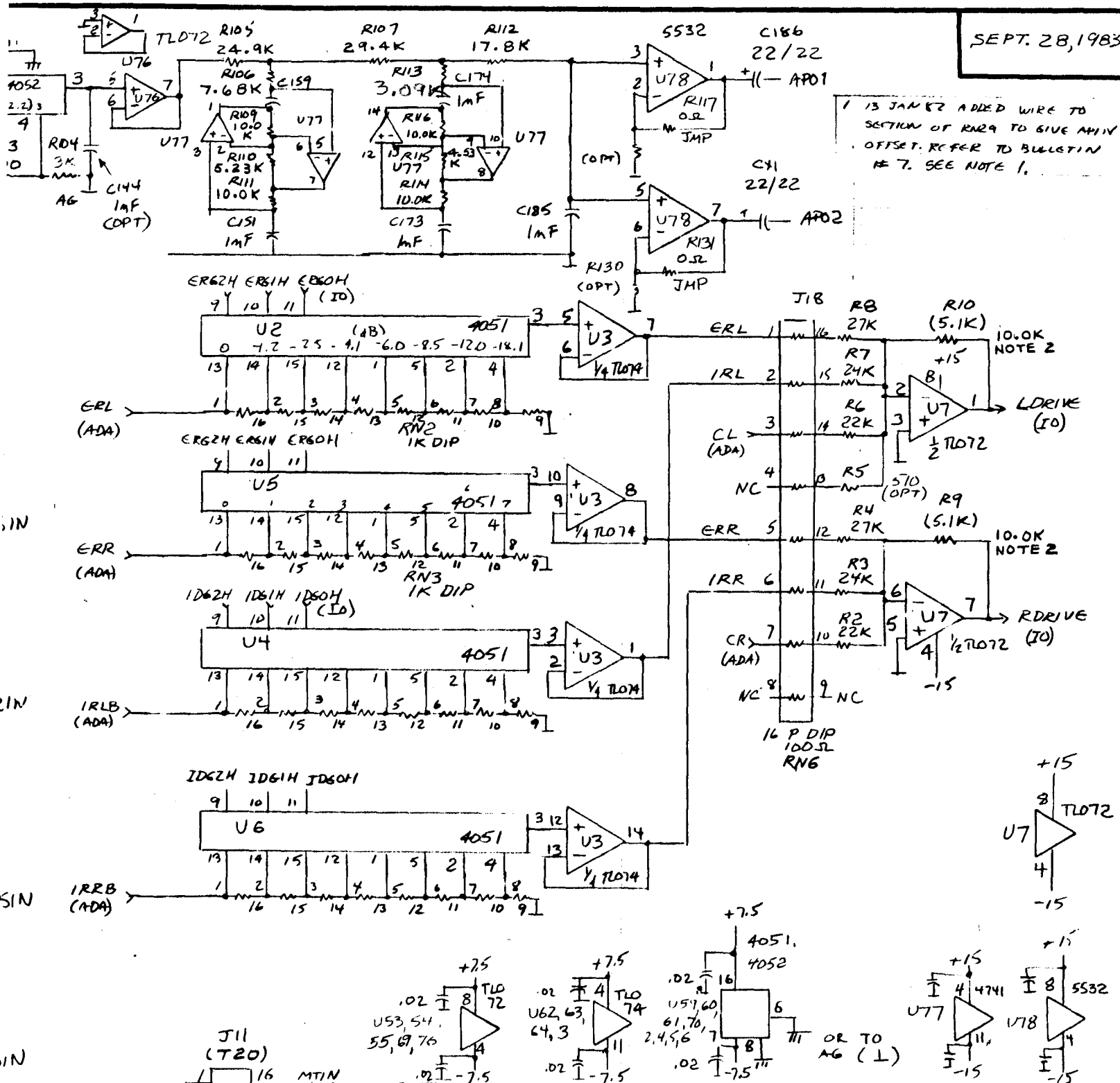
8X32

SCALE: ~	APPROVED BY	DRAWN BY CM
DATE: 18 FEB 81	LAST REV: SEPT. 28, 1983	
ANA-2, ADA (SHEET 2 OF 3)		
URSA MAJOR, Inc BOX 8 BELMONT MA 02178 USA		DRAWING NUMBER <span style="font-size: 1.5em; font-weight: bold;">0398</span>



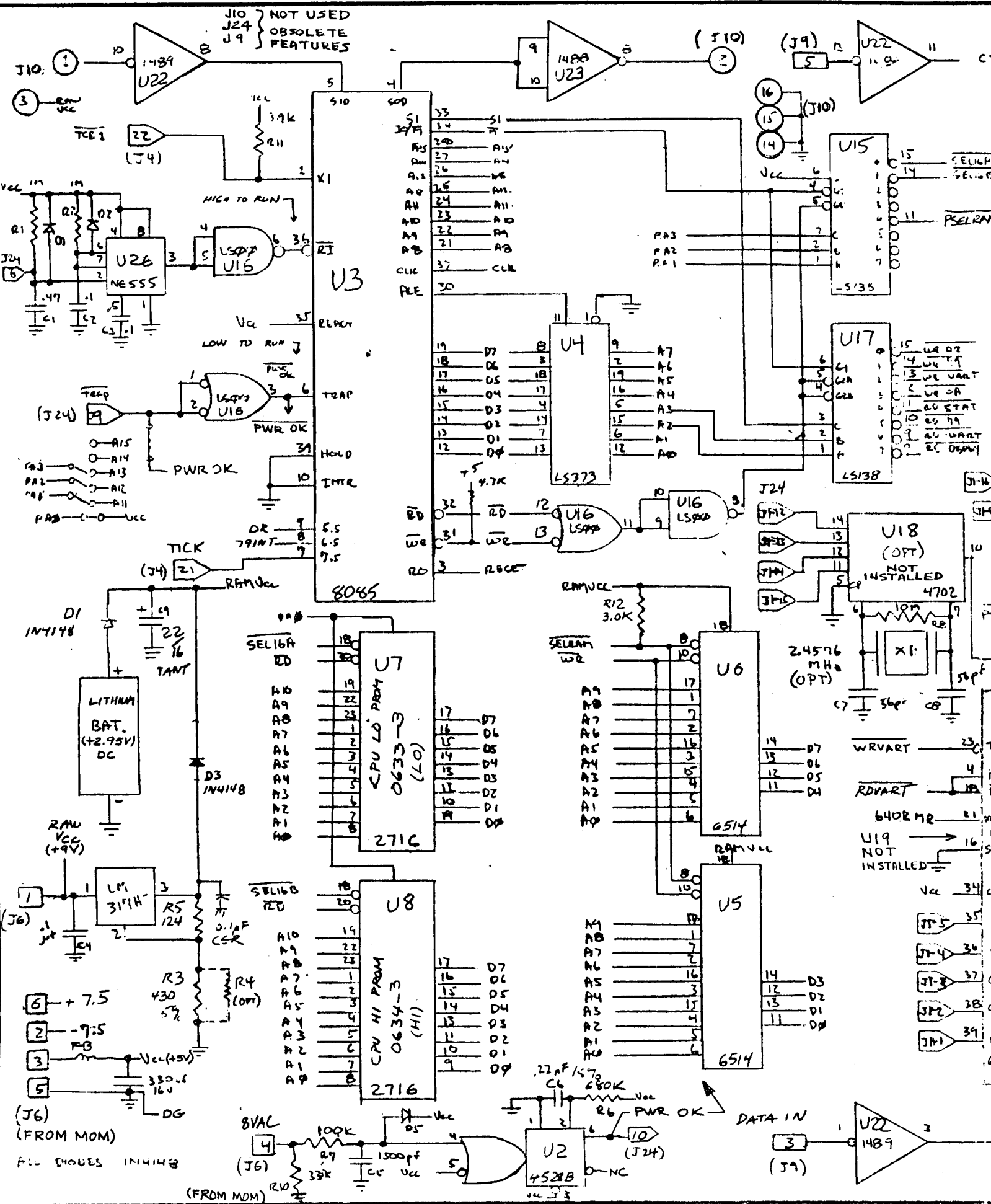
SEPT. 28, 1983

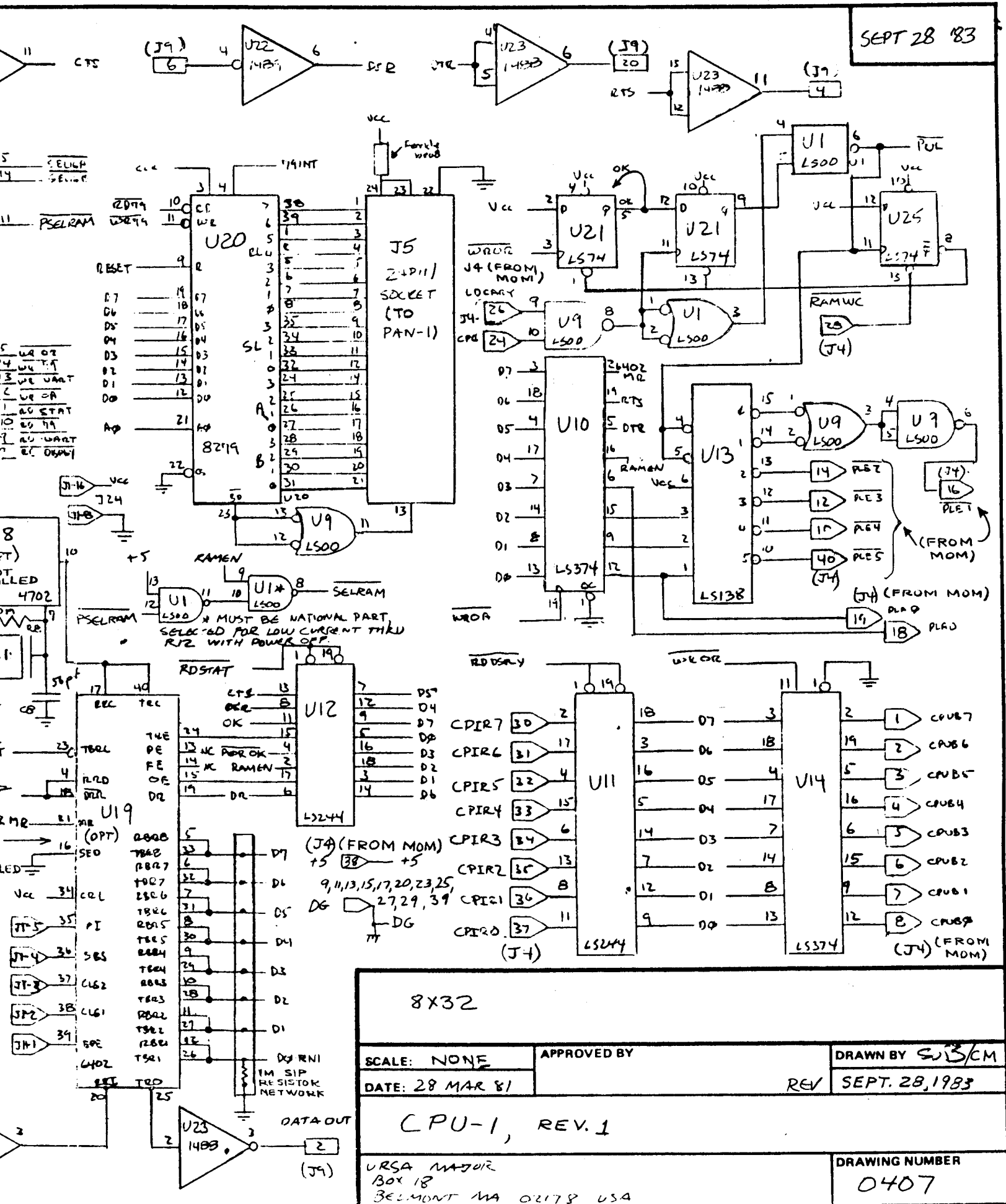
1 13 JAN 82 ADDED WIRE TO SECTION OF R29 TO GIVE MINV OFFSET. REFER TO BULLETIN # 7. SEE NOTE 1.



8X32

SCALE: —	APPROVED BY	DRAWN BY CM
DATE: 19 FEB 81	LAST REV: SEPT. 28, 1983	
ANA-2, FBC (SHEET 3 OF 3)		
URSA MAJOR, INC BOX 18 BELMONT MA 02178 USA		DRAWING NUMBER <span style="font-size: 1.5em;">0399</span>





MUST BE NATIONAL PART, SELECTED FOR LOW CURRENT THRU R12 WITH POWER OFF.

8X32

SCALE: NONE      APPROVED BY

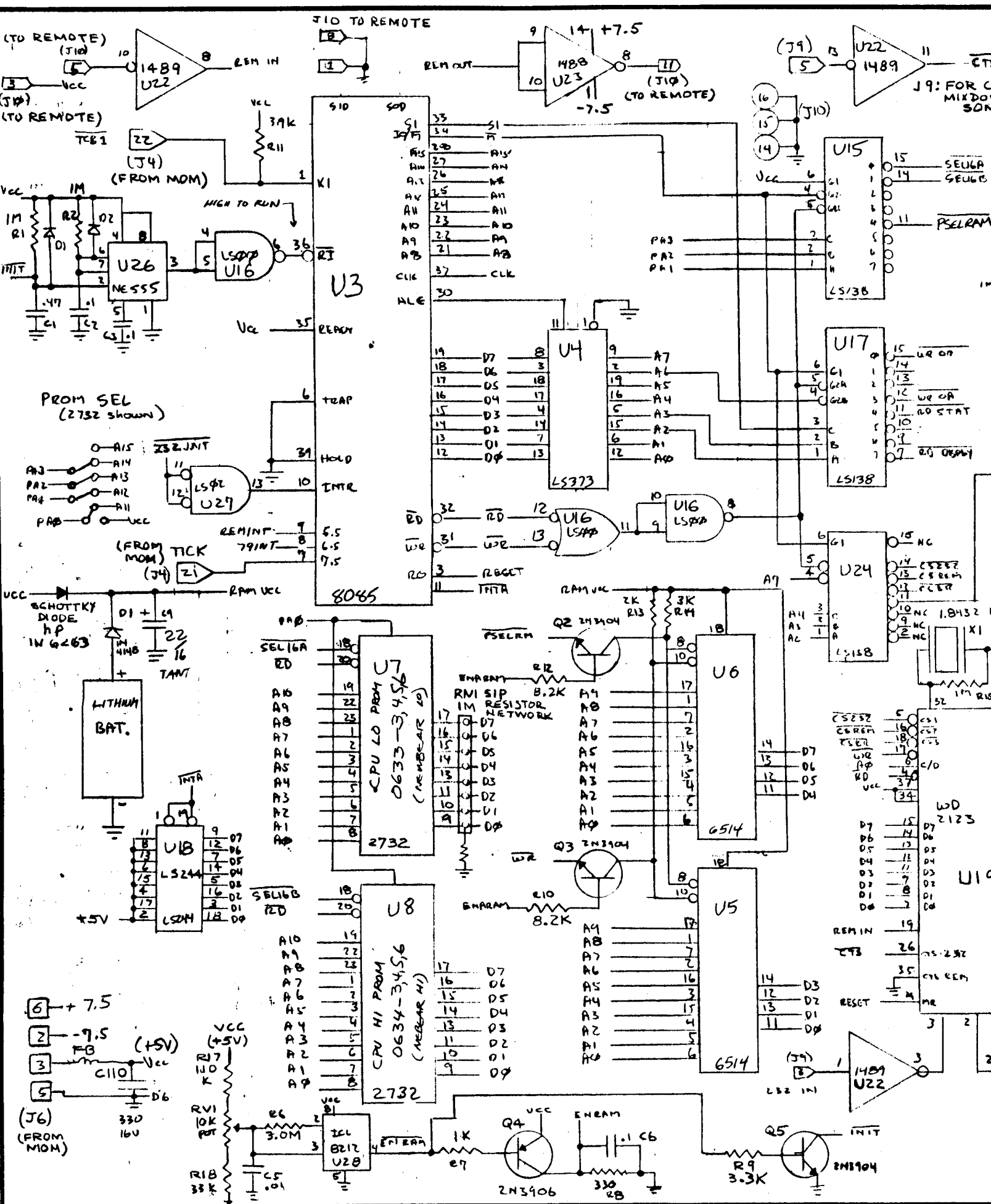
DATE: 28 MAR 81      REV      DRAWN BY SJS/CM

CPU-1, REV. 1      SEPT. 28, 1983

URSA MAJOR  
Box 18  
BELMONT MA 02178 USA

DRAWING NUMBER  
0407





SEPT. 28, 1983

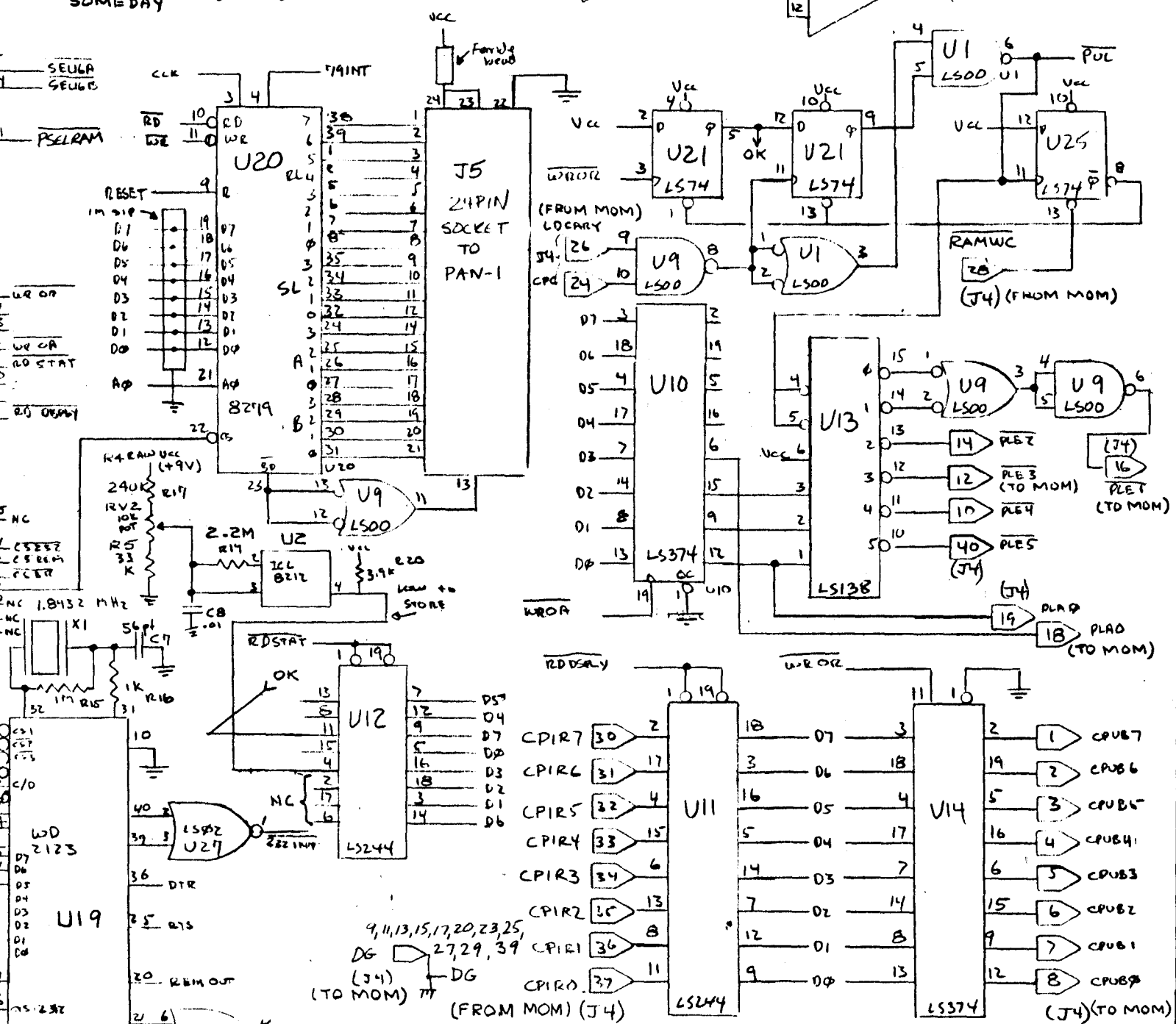
J9: FOR COMPUTER MIXDOWN R5232C, SOMEDAY

SEUGA SEUGE  
PSEL RAM  
RD WR  
D7 D6 D5 D4 D3 D2 D1 D0  
A7 A6 A5 A4 A3 A2 A1 A0

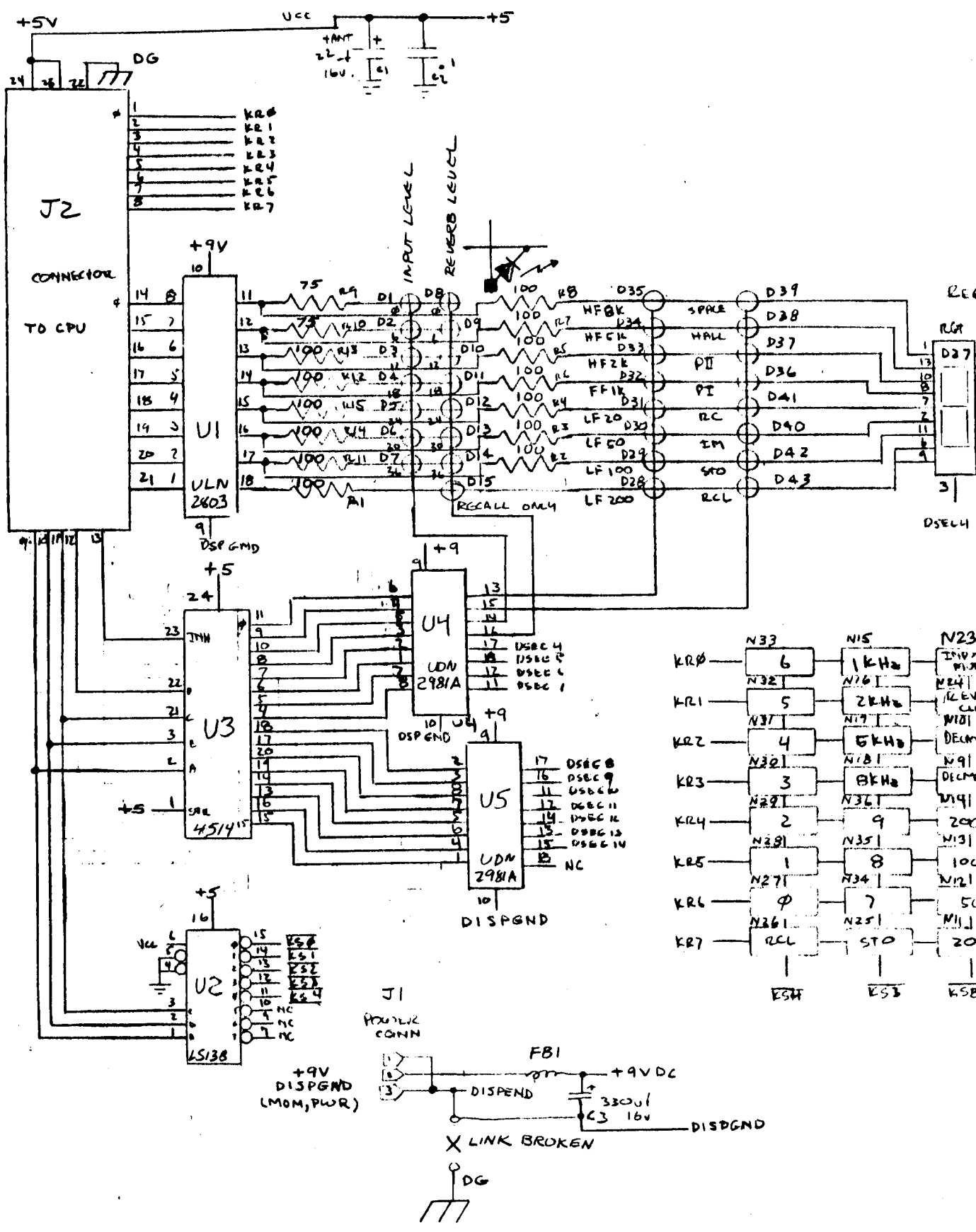
15 NC  
14 C5257  
13 C5258  
12 C5259  
11 C5260  
10 NC  
9 NC  
8 NC  
7 NC  
6 NC  
5 NC  
4 NC  
3 NC  
2 NC  
1 NC

WD 2123  
D7 D6 D5 D4 D3 D2 D1 D0  
A7 A6 A5 A4 A3 A2 A1 A0  
C51 C52 C53  
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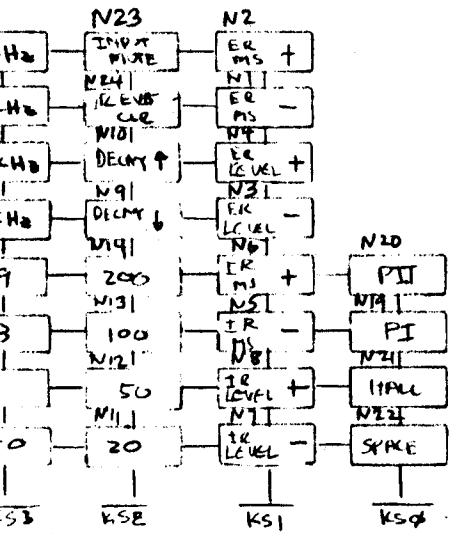
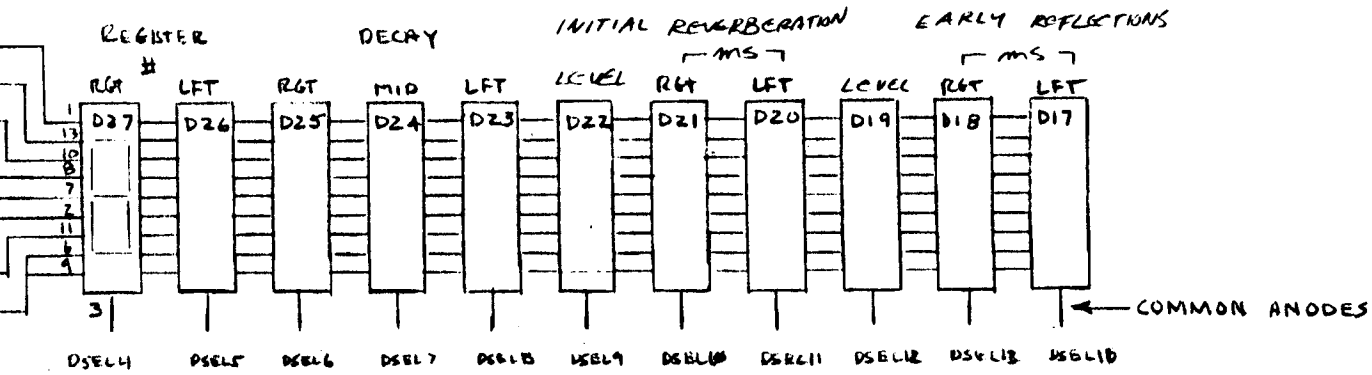
J9: FOR COMPUTER MIXDOWN R5232C INTERFACE, SOMEDAY



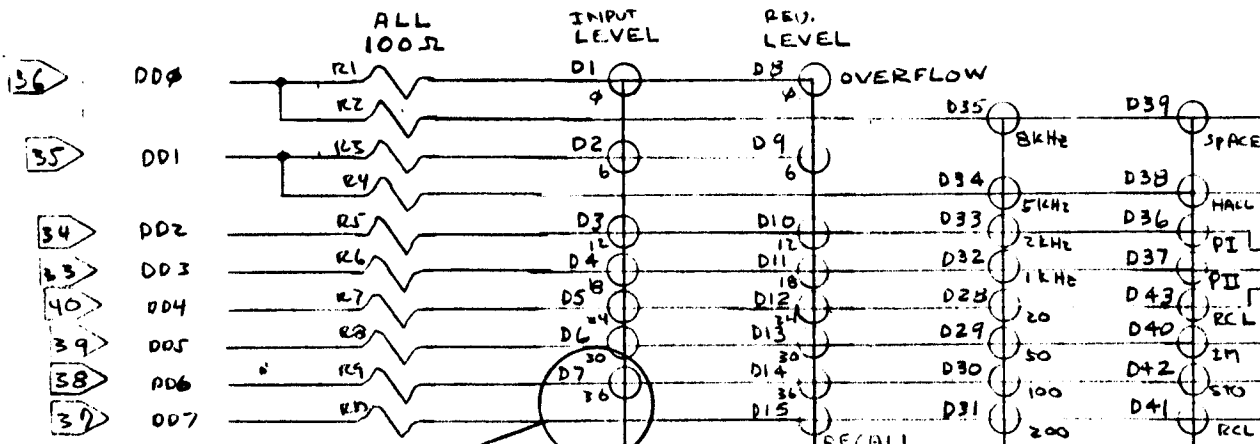
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SCALE: NONE	APPROVED BY	DRAWN BY SJS/CM
DATE: 28 MAR 81		REV SEPT 28 83
CPU-1, REV. 2		
URSA MAJOR BOX 18 BELMONT MA 02178 USA		DRAWING NUMBER 0407



SEPT. 28, 1983

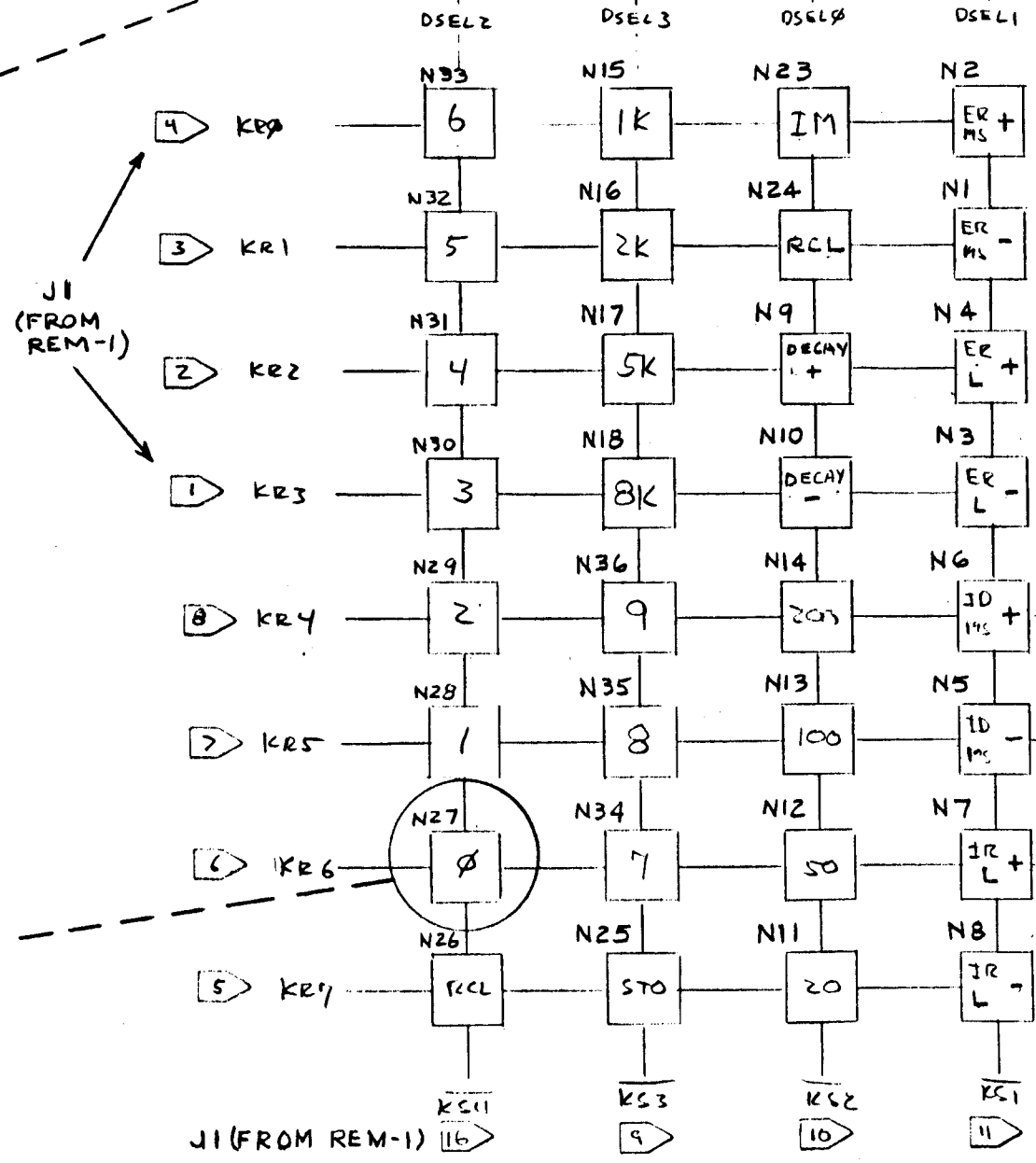
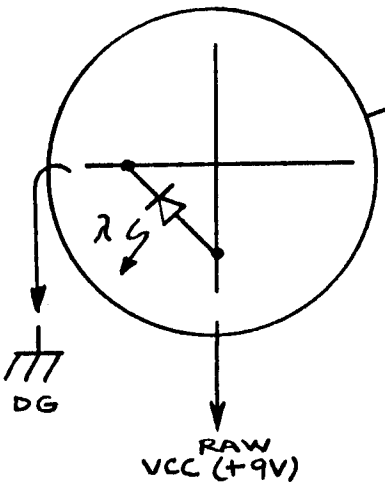


8X32		
SCALE: —	APPROVED BY	DRAWN BY SOB/CM
DATE: 28 MAY 81	REV	SEPT. 28, 1983
PAN-1 - FRONT PANEL BOARD, 8X32		
VRSR MAJDR BOX 18 BELMONT MA 02178 USA		DRAWING NUMBER 0414



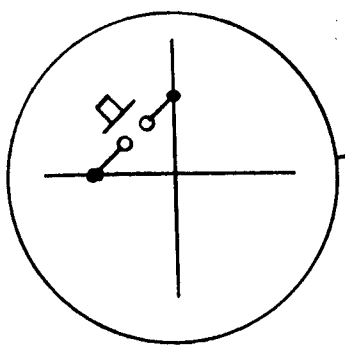
J1  
(FROM  
REM-1)

TYP LED  
IN MATRIX



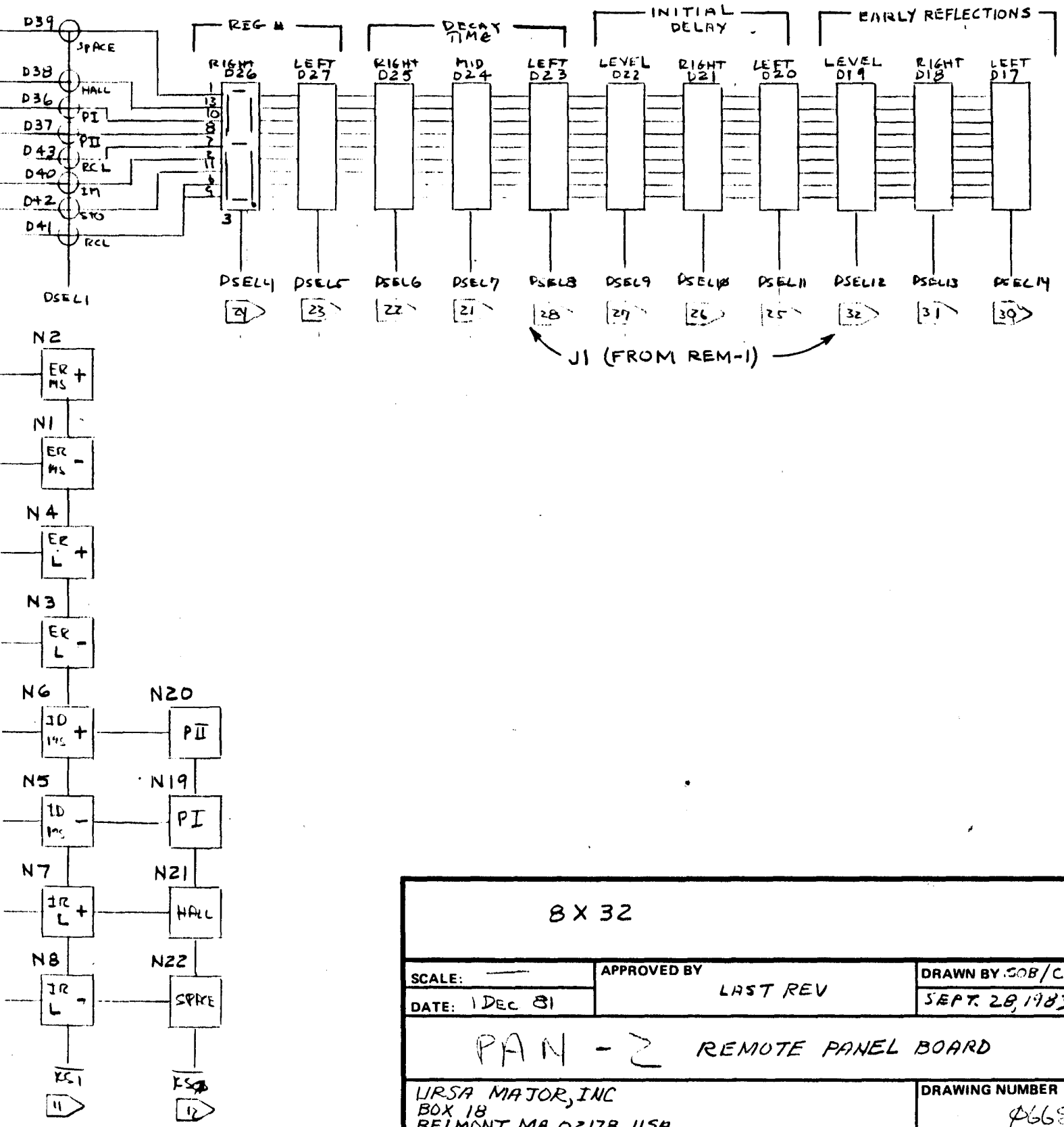
J1  
(FROM  
REM-1)

TYP SWITCH  
IN MATRIX

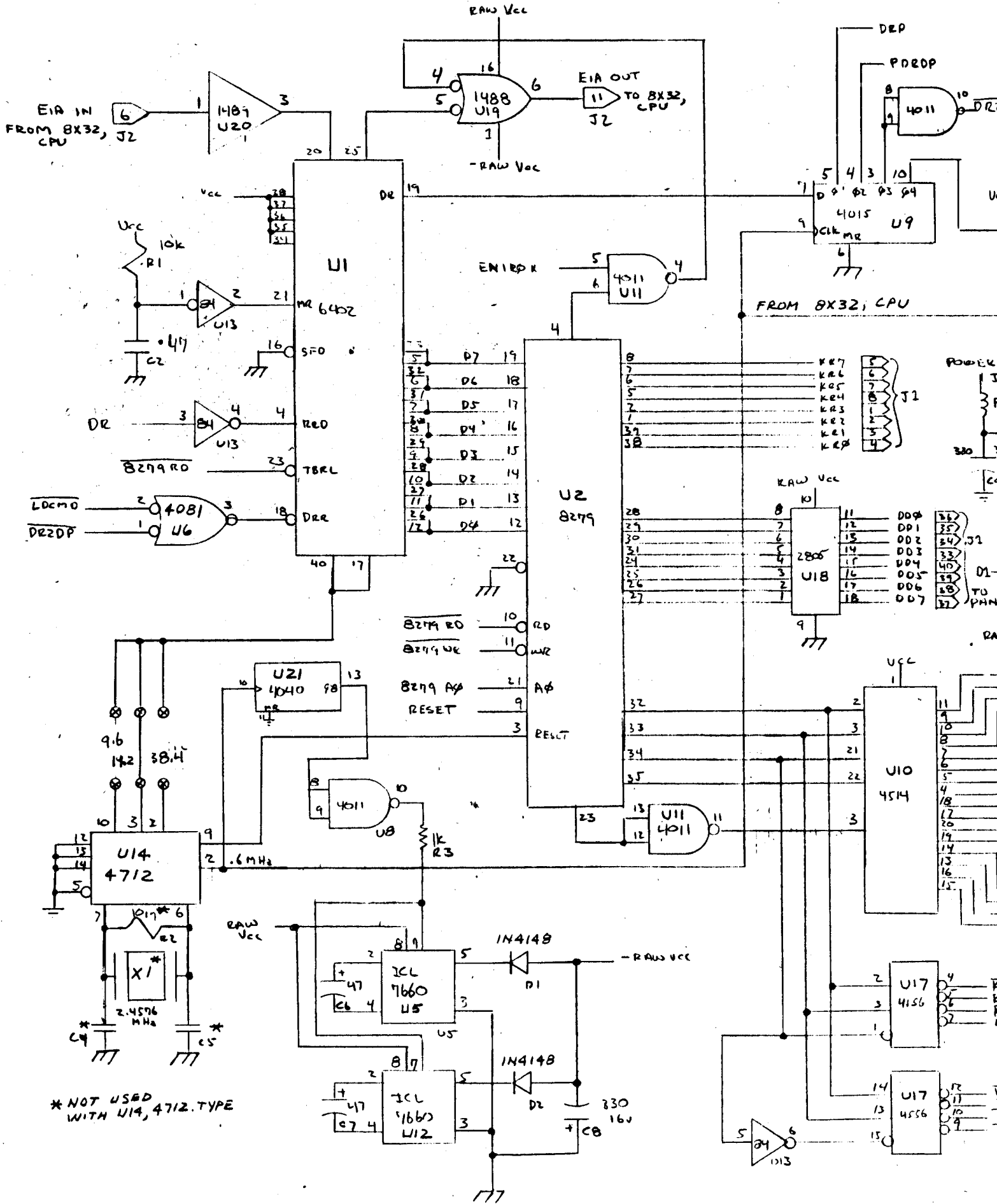


J1 (FROM REM-1)

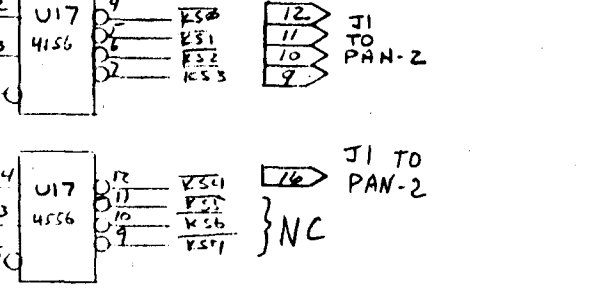
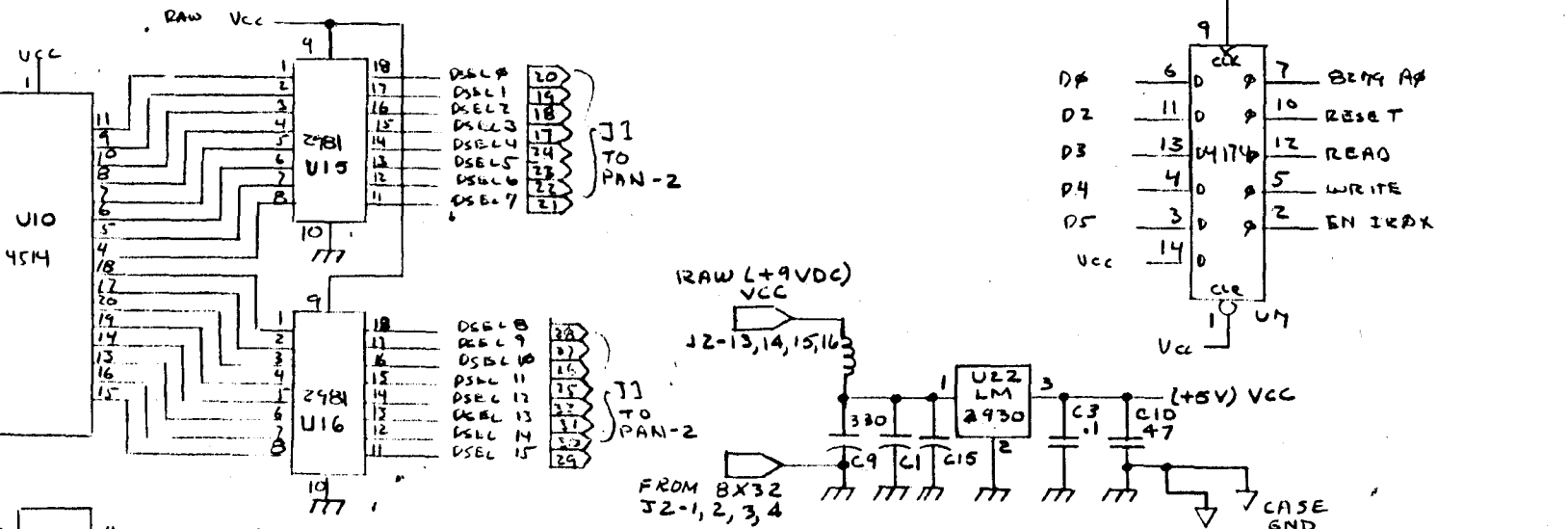
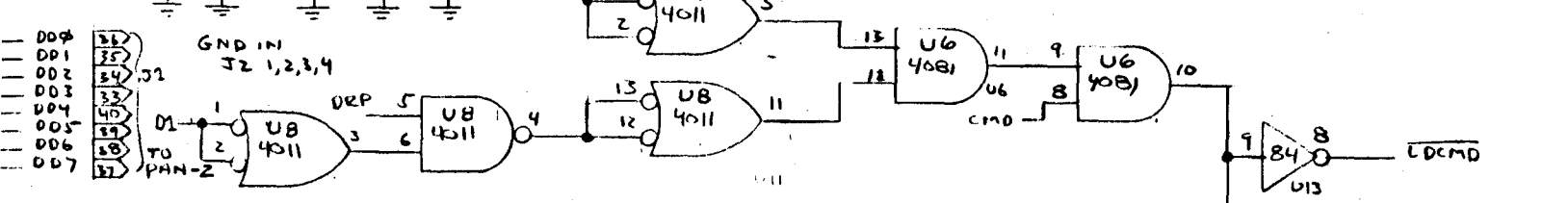
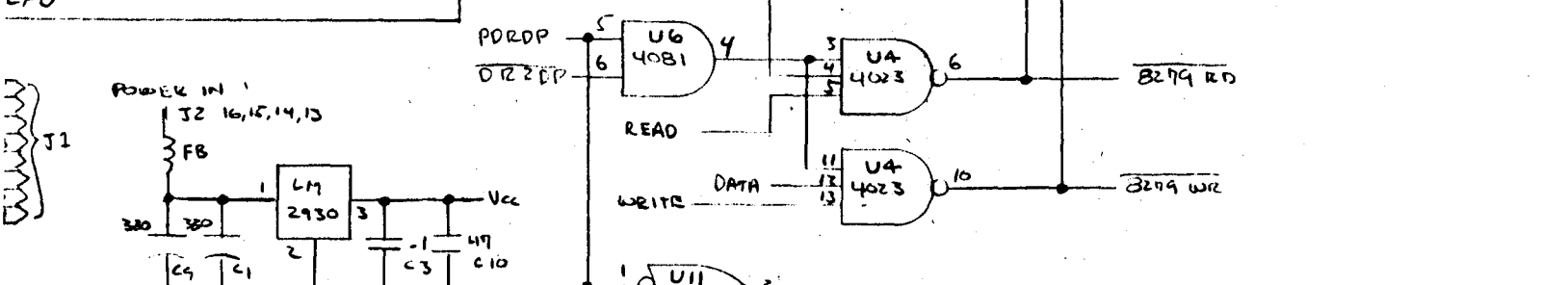
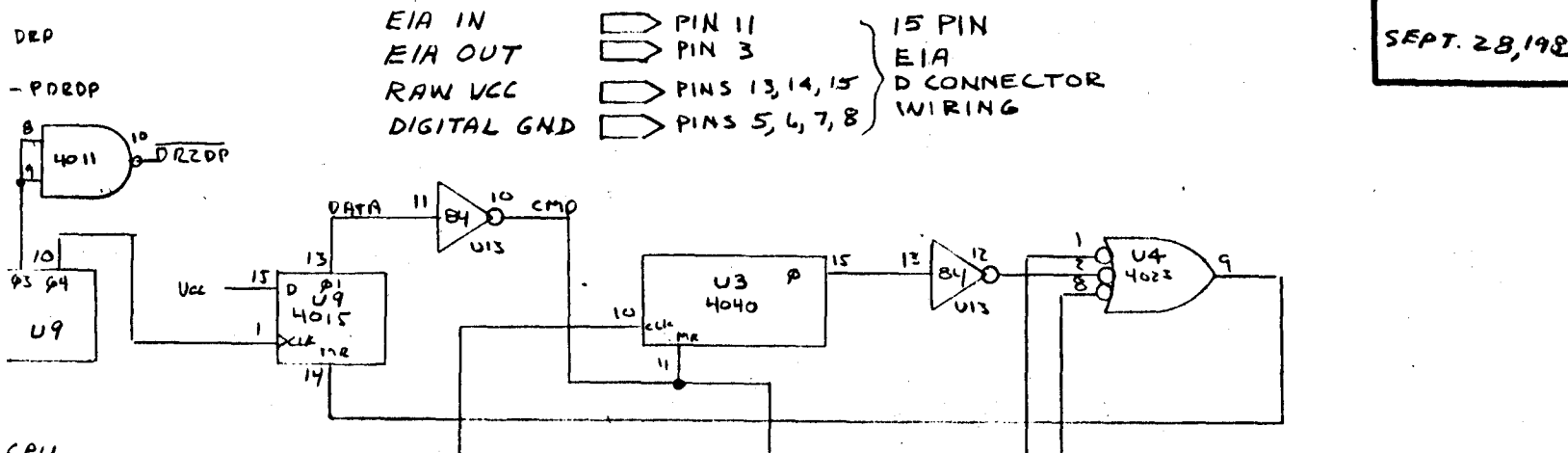
SEPT 28 8.



8 X 32		
SCALE: —	APPROVED BY LAST REV	DRAWN BY: SOB/CM
DATE: 1 DEC 81		SEPT. 28, 1983
PAN - 2 REMOTE PANEL BOARD		
URSA MAJOR, INC BOX 18 BELMONT, MA 02178 USA		DRAWING NUMBER 4663



SEPT. 28, 1983



8 X 32

SCALE:	APPROVED BY	DRAWN BY SDH/CM
DATE: 2 Dec 81	LAST REV.	SEPT. 28, 1983
<b>REM-1 REMOTE CIRCUIT BOARD</b>		
URSA MAJOR, INC. BOX 18 BELMONT, MA. 02178 USA		DRAWING NUMBER 0669