YAMAHA

PROGRAMMABLE MEMORY SYNTHESIZER
CS SERIES

20M/40M

●HARDWARE MANUAL

CONTENTS

Although this manual describes the circuit structure centering around the CS-40M, the same description applies to the circuitry of CS-20M too, As the latter is only a minor model of the CS-40M and is basically the same.

FEATURES

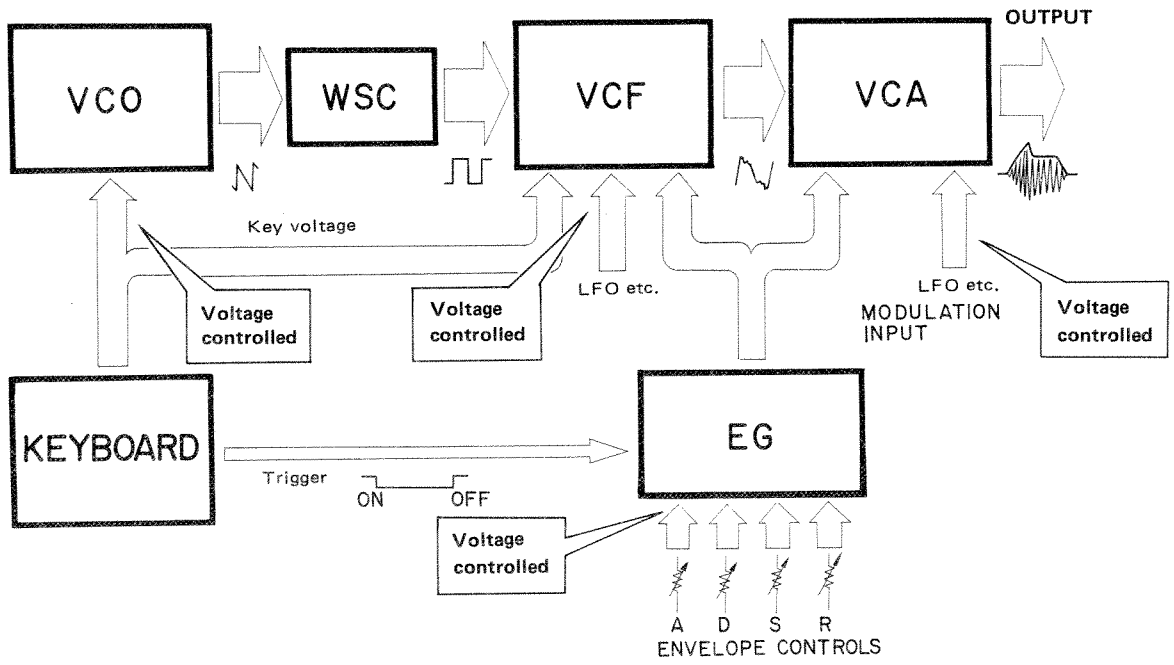
The CS-20M and CS-40M not only enables operation with 5-mode functions, but adopts methods departing from those of conventional synthesizers in connections with hardware.

OPERATIONAL FEATURES: 5-Mode Functions

1. **PANEL Mode**
   Similar to conventional synthesizers, the controls provided on the panel enable sound-creating manupulation.
2. **VOICE WRITE Mode**
   By one touch operation, it is possible to have the synthesizer memorize a plural number of voices created at the panel. This is achieved by having the parameters (voltage data) of the panel controls memorized into the IC memory.
3. **VOICE Mode**
   By depressing the push button, the voices can be recalled for play.
4. **STORE Mode**
   In this mode, parameters that have been memorized into the IC memory can be recorded on a cassette tape.
5. **LOAD Mode**
   When necessary, voice parameters memorized on the cassette tape can be recalled into the IC memory.

Voltage controlled

In order to realize these functions, the CS-20M and CS-40M are equipped with hardware (circuitry) that has several features hitherto unfound in conventional synthesizers. However, the process in which voices are created is exactly the same with conventional analog synthesizers.
The basic composition of an analog synthesizer is as shown in the following diagram. Every type of control is effected using the voltage values as parameters.

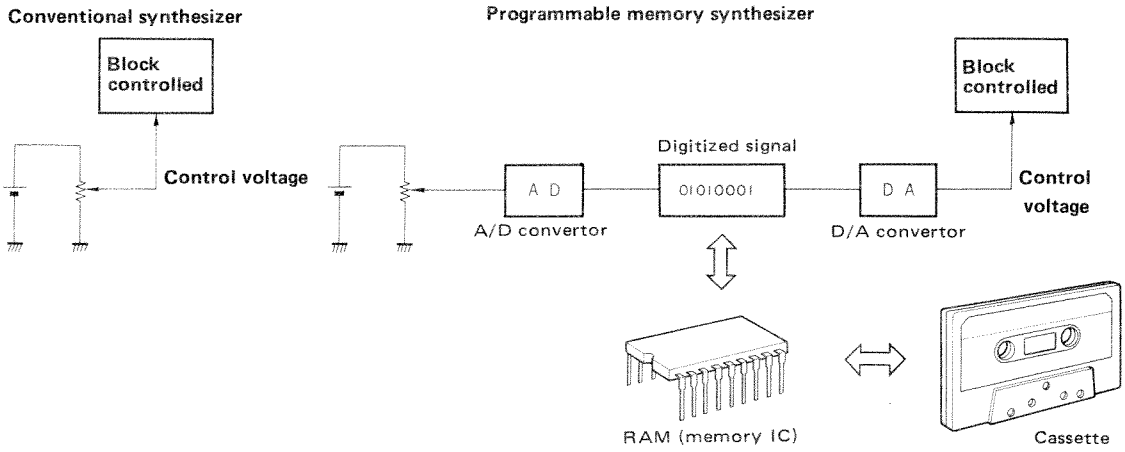


In other words, the actions of the respective blocks are determined by the size of the voltage applied to the cirtain block. This holds true for both the CS-20M and CS-40M.

TECHNICAL FEATURES : Digital parameters

To memorize

Analog voltages cannot be memorized over a long period of time*. Accordingly, the various control voltages are converted once into digital signals. (A/D conversion) These digital signals can be readily memorized by a semiconductor memory. When such blocks as the VCO, VCF and VCA are to be controlled, the digital voltage is converted into an analog voltage and applied to the particular block. (D/A conversion) This constitutes a large difference between a conventional synthesizer and programmable synthesizer in terms of hardware.

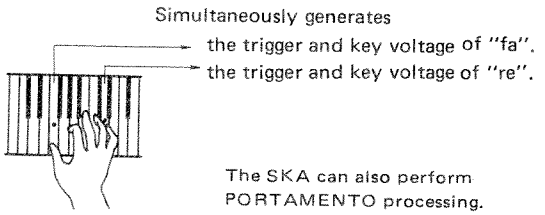


Newly employed

The major portions of the actual circuit composition that differ from conventional synthesizers are shown in outline below. Composition of other sections practically remain unchanged.

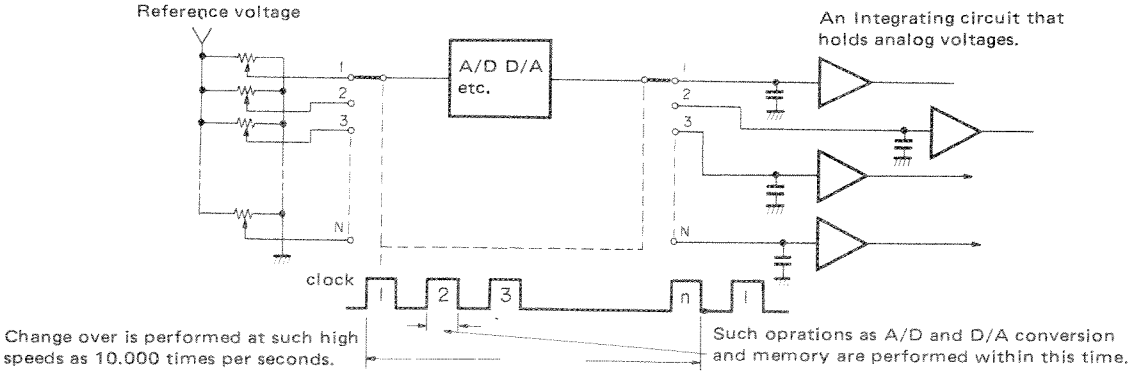
1. Key Assigner Section (SK Circuit Board)

To generate two tones, that is the highest and lowest tones, simultaneously, a special LSI (YM-615) has been newly developed and employed. This LSI not only inherits the philosophy that underlies such polyphonic synthesizers as the CS-50 and CS-60 and etc, but has also developed it further.



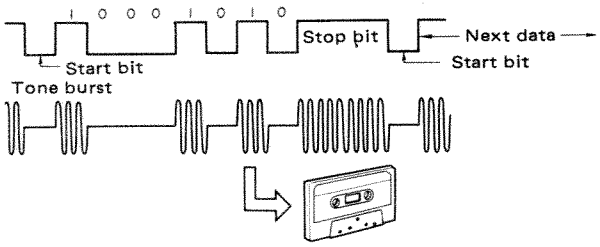
2. Programming Section

This block performs A/D conversion and D/A conversion by effecting centralized control for the voltages (0 ~ 4V) that have been obtained by means of the respective controls provided on the panel. Since an enormous number of circuits will be needed to carry out parallel processing of a large number of parameters simultaneously, this is performed instead by scanning a large number of parameters by time-sharing processing that is synchronized with the clock.



3. Cassette Interface Section (PGM C. board)

This block serves to record on a cassette tape data of digital signals, tha is, "8 bits (referred to as one word) x Number of controls x Number of voices", that have been memorized into the memory IC, or to recall the data into the memory IC. The data is recorded by the Tone Burst Method, after adding such bits as the START bit and STOP bit to the 8-bit data.

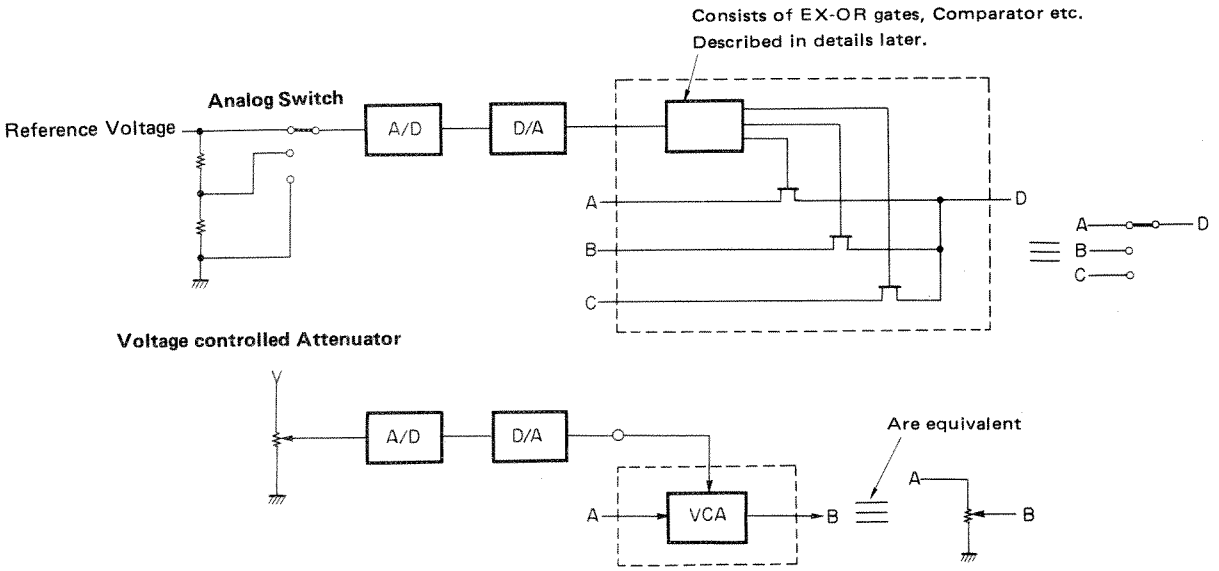


4. Mode Control Section (PGM C. board)

After the 5-mode functions are detected by means of the push button on the panel, this block functions to effect such control as WRITING the data into the IC memory, READING the data from the IC memory, storing, or loading them onto the cassette tape.

5. Analog Switch and Control Circuit

Instead of using mechanical switches and controls to perform the functions the of switch to change the flow of signals of the VCO→VCF→VCA line, or those of the controls in mixing operations, this circuit employs electrical elements to do the same job. The setting condition of the switches and controls are expressed in DC voltages and after being digitized as parameters are memorized. For this reason, it calls for switch circuits and controls that are activated by the differnce in DC voltages. The circuit that has such functions is the analog switch & control circuits which are provided at key points of circuits.



Signal flow

The circuits that have been described constitute the major circuits employed in a programmable synthesizer. Circuit operation shall be described in each corresponding section. But by keeping the points that have been described in mind, it should be possible to understand the rough idea when you look at a circuit diagram.

A block diagram that shows the general flow of signals is given the next page.

2. CIRCUIT COMPOSITION OF PROGRAMMER

Function Mode Control Section: The function mode is specified with the programmer's operating button. Simultaneously, the specified function mode is displayed.

a. Mode Selection

Function — Generates function codes selected according to mode selection.

ICs used
- TC4532BP . . . . . 8-bit encoder
- TC40175BP . . . . . D-type Flip-Flop
- YM617 . . . . . Parallel → Serial conversion

b. Mode Indicating Circuit

Function — Indicates the specified function mode.

ICs used
- YM617 . . . . . Serial → Parallel conversion
- TC4028BP . . . . . Decoder
- M54516P . . . . . LED driver (Buffer)

Program Controller: Controls all data of the programmer

IC used
- YM616 . . . . . LSI for central processor control

Function Mode Executing Section: According to the selected function mode, performs signal transmission.

a. Control Voltage Parameter Generator

Functions — According to the panel setting, generates voltage parameters to control the respective blocks.

b. Multiplexer

Functions — Performs multiplexing of the control voltage parameters of the panel. Parallel-In, Serial-Out.

IC used
- YM617 . . . . . Multiplexer

c. A/D & D/A converter

Functions — Performs A/D and D/A conversion for the control voltage parameters following multiplexing.

d. Demultiplexer

Functions — Performs demultiplexing of the control voltage parameters following A/D and D/A conversions. Serial-In, Parallel-Out.

IC used
- YM617 . . . . . Demultiplexer

e. RAM (Random Access Memory)

Functions — Memorizes digital voice data of the 20 voices and 50 parameters.

IC used
- M58981S-45 . . . . . RAM (1024 words x 4 bits)

f. Cassette Interface

Functions — STORE and LOAD modes

3. MULTIPLEXER

3-1 Control Voltage Parameter Generator

50 parameters

The generator for the 50 different block control parameters on the PA and PB circuit boards (on the control panel) generate control voltages (0V to 4.00V) selected by the controls that have programming functions. The table lists the output voltages of the controls of the CS-40M have programming functions.

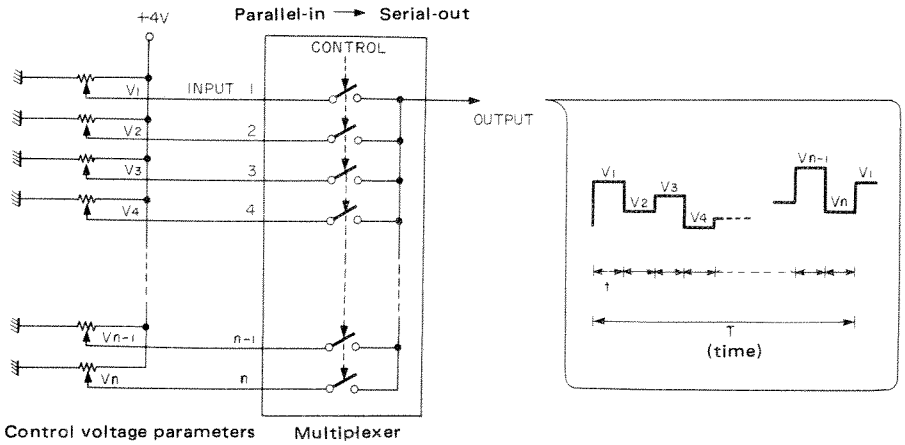
CONTROL VOLTAGE PARAMETERS

Board	BLOCK	FUNCTION	POSITION	VOLTAGE	REMARKS
PA	VCO 1,2	FEET	64' 32' 16' 8' 4' 2'	0 0.67 1.33 2.00 2.67 3.33	
		WAVE	∧ ◸ ⊓	0 1.33 2.67	
		MODULATION FUNCTION	∿ ◸ ⩗ ⊓ S/H E+ E−	0 0.57 1.14 1.71 2.29 2.86 3.43	
		MODULATION DEPTH	0 - 10	0 - 4	VR-A
		PW(PULSE WIDTH)	50 - 90%	0 - 4	VR-B
		PWM FUNCTION	∿ E+ E−	0 1.33 2.67	
		PWM DEPTH	0 - 10	0 - 4	VR-B
	LFO	SPEED	S - F	0 - 4	VR-B
		SPEED DEPTH	0 - 10	0 - 4	VR-B
		EG-VCO	∧ ⩗	4 0	
	EG-VCO	TIME EXPAND	NOR x5	4 0	
		ATTACK TIME	S - L	4 - 0	VR-C
		DECAY TIME	S - L	4 - 0	VR-C
	RMO	ON - OFF	ON OFF	4 0	
		SPEED	S - F	0 - 4	VR-B
		SPEED DEPTH	0 -10	0 - 4	VR-B
		EG - VCO	∧ ⩗	4 0	
PB	MIXER	VCO 1	0 - 10	0 - 4	VR-A
		VCO 2	0 - 10	0 - 4	VR-A
		NOISE	0 - 10	0 - 4	VR-A
	VCF	CUT OFF FREQ	L - H	0 - 4	VR-B
		RESONANCE	L - H	4 - 0	VR-B
		FILTER MODE	LP BP HP	0 1.33 2.67	
		MODULATION FUNCTION	∿ ◸ ⩗ ⊓ S/H	0 0.8 1.6 2.4 3.2	
		MODULATION DEPTH	0 - 10	0 - 4	VR-B
		EG DEPTH	0 - 10	0 - 4	VR-B

Board	BLOCK	FUNCTION	POSITION	VOLTAGE	REMARKS
PB	VCF	KCV	ON OFF	4 0	
	EG-VCF	POLE	⌒ ⌣	0 4	
		TIME EXPAND	NOR x5	0 4	
		ATTACK TIME	S - L	4 - 0	VR-C
		DECAY TIME	S - L	4 - 0	VR-C
		SUSTAIN LEVEL	0 - 10	0 - 3.4	VR-B
		RELEASE TIME	S - L	4 - 0	VR-C
	VCA	∿ 1	0 - 10	0 - 4	VR-A
		∿ 2	0 - 10	0 - 4	VR-A
		MODULATION FUNCTION	∿ ⊓ ⩗ ⊓	0 1 2 3	
		MODULATION DEPTH	0 - 10	0 - 4	VR-A
	EG-VCA	TIME EXPAND	NOR x5	0 4	
		ATTACK TIME	S - L	4 - 0	VR-C
		DECAY TIME	S - L	4 - 0	VR-C
		SUSTAIN LEVEL	0 - 10	0 - 3.4	VR-B
		RELEASE TIME	S - L	4 - 0	VR-C
	OUTPUT	POA	ON OFF	4 0	

3-2 Multipexer

The 50 different control voltages that can be obtained from the control voltage parameter generator, are applied to the input terminals (1) through (50) of the multiplexer. By subjecting these voltages to parallel and serial conversions, output voltages that vary at a fixed timing are fed out from the COM terminal.
The figure shown below gives the basic ptinciple diagram of the multiplexer.

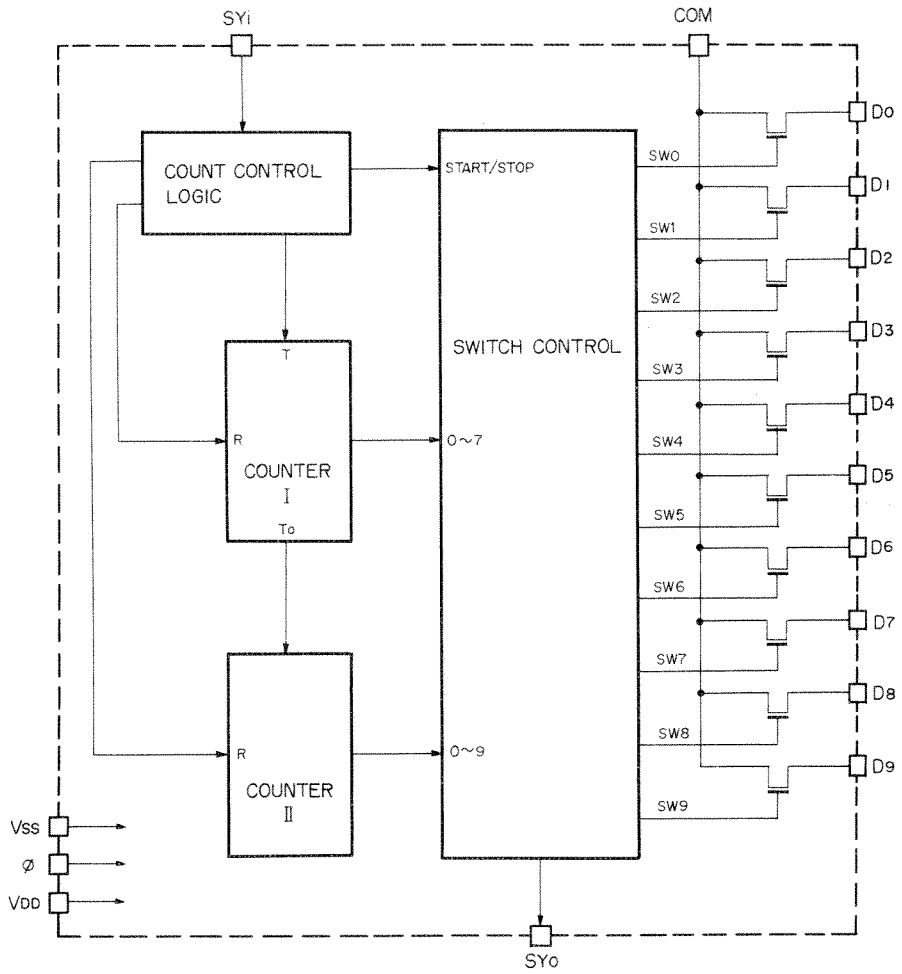


Parallel-In, Serial-Out

The term "parallel to serial conversions" as used here refers to the opereation of turning ON and OFF n pieces of switches (having a common output) in sequence at a fixed timing. Thus n pieces of data are fed out one after another.

10 in 1 out

The YM617 employed as the multiplexer is an LSI called as a SMD (Synthesizer Mult/Demultiplexer). Provided with 10 analog switches, it can multiplex 10 pcs. of data. The block diagram of the YM617 is shown below. In the CS-40M, which empolys five YM617s, 50 parameters are fed out one by one from the COM terminal at a 100μs timing.

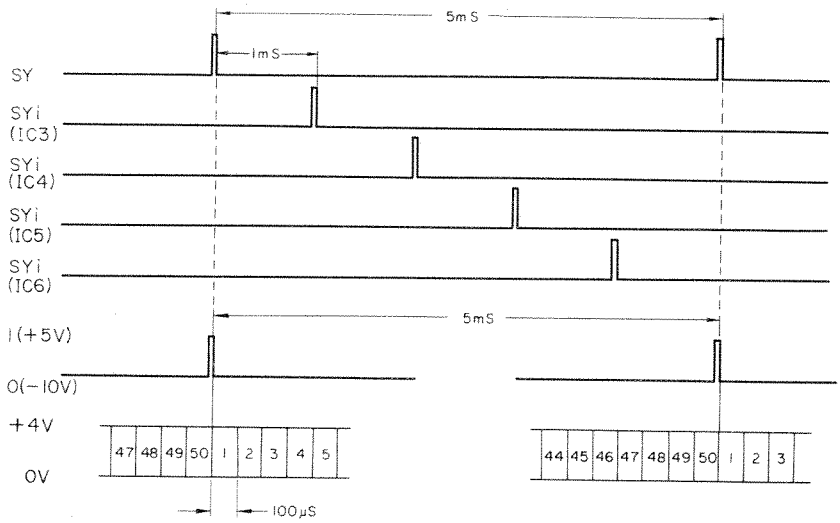


PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	D_4	Switch Input/Output	16	COM	Switch Common
2	D_3		15	D_5	Switch Input/Output
3	D_2		14	D_6	
4	D_1		13	D_7	
5	D_0		12	D_8	
6	SYi	Synchro-pulse Input	11	D_9	
7	SYo	Synchro-pulse Output	10	V_{DD}	−10 volt power supply
8	Vss	+5 volt power supply	9	ϕ	Clock pulse Input

■ OPERATING PRINCIPLE OF YM617

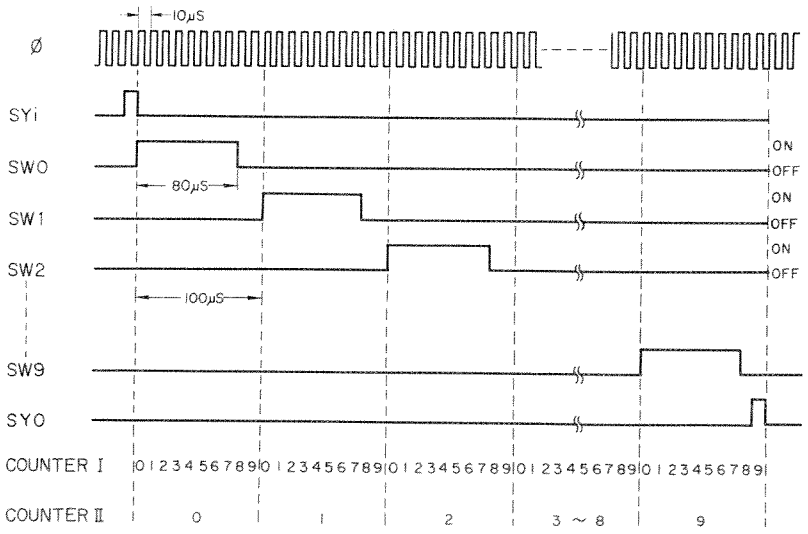
Analog switch

When "1" (Vss) is set for the SYi terminal, counters 1 and 2 will start counting. Counter I is a decimal counter that counts the pulses of Clock ϕ, while Counter II is a counter that further counts To (Trigger OUT) pulses of Counter I. The analog switches will turn ON and OFF one after another, corresponding to the count of Counter II. The duration of "ON" is synchronized with Counter I's count of 0 through 7. After SYi = "1" is fed in, SYo will become "1" after 100 bits following ϕ. This data is transmitted to the terminal SYi of the next YM617, In the same manner, it is possible to switch the ten analog switches ON and OFF. The timing chart for this operation is given below.



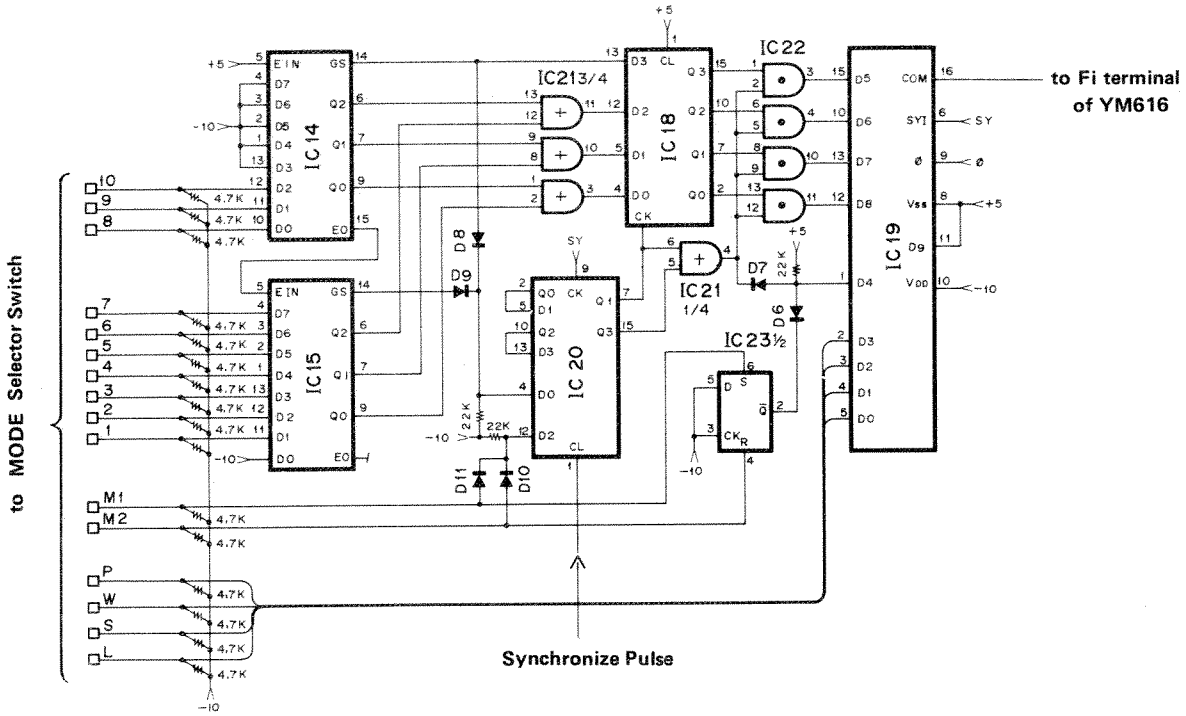
5m seconds

As the programmer's master clock ϕ counts at 100KHz, the 1-bit count of Counter I is performed at 10μs. Consequently, the analog switches which correspond to Counter II turns ON and OFF at a timing of 100μs. The ON-duration will be the time it takes Counter I to count from 0 up to 7, that is, 80μs. Since SYO outputs pulse data after a 1ms delay following the input from SYi, it means that from 1 up to 50 control voltage parameters are multiplexed in a duration as short as 5ms in the case of the CS-40M.



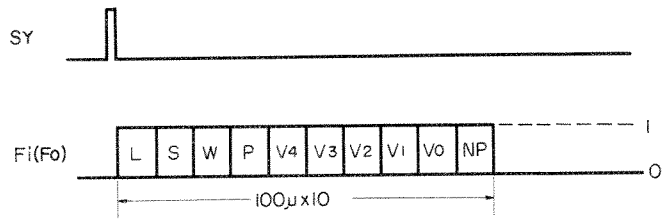
4. FUNCTION MODE CONTROL SECTION

4-1 Mode Selecting Circuit



Encoding

By operating the program operating buttons on the control panel, the circuit supplies the timing data that are needed for selecting the mode into the Fi terminal of the program controller (YM616). The following drawing shows the layout of the function data that appears at the COM terminal of the IC19 (YM617). YM616 will select the respective function modes in compliance with these data.



Function code

As shown in the drawing, the respective bits of the encoded 10-bit function data have the following meanings.

L : LOAD . . . . . When "1", "Transfer data recorded (in STORE mode) on cassette tape to RAM."

S : STORE . . . . . When "1", "Transfer data from RAM to cassette tape."

W : WRITE . . . . . "Write A/D-converted data into RAM."

P : PANEL . . . . . "After A/D- and D/A-converting voltage parameters produced with the panel control, add them to each block."

$V_4 \sim V_0$: VOICE . "After reading data written into RAM, according to the selected voice, subject it to D/A conversion." Voices are selected by binary data*, $V_0 \sim V_4$.

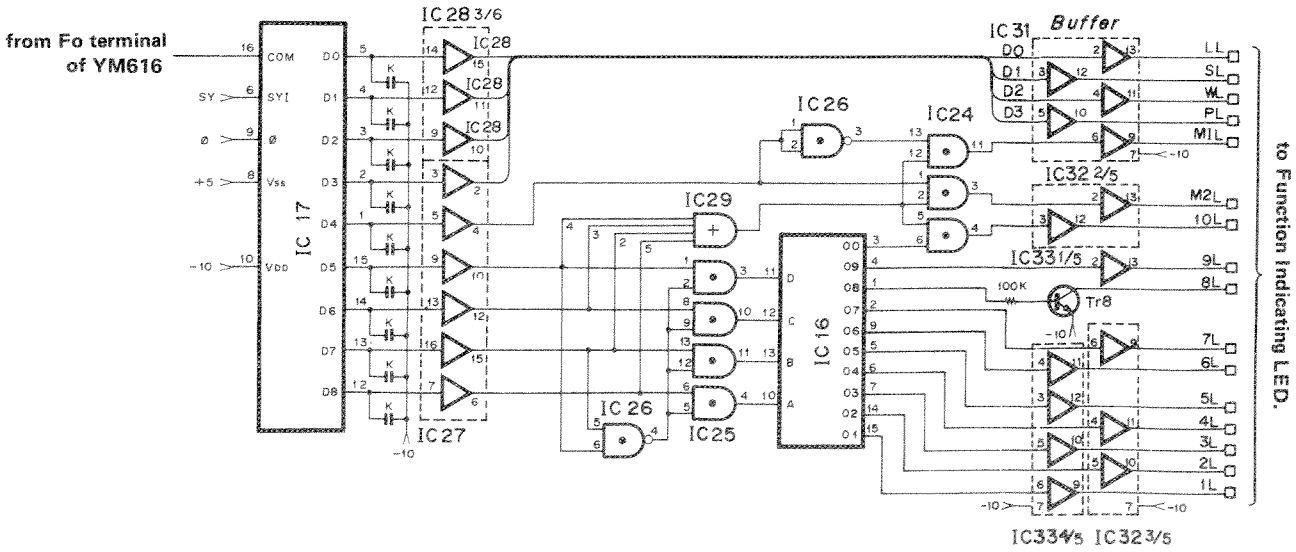
NP : . . . . . Selects the number of voices and parameters.
1 : 20 voices and 50 parameters (CS-40M)
0 : 8 voices and 32 parameters (CS-20M)
* Voice selection ($V_0 \sim V_4$) is performed as shown in the following chart.

VOICE	V_4	V_3	V_2	V_1	V_0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	1	0	0	0	1
12	1	0	0	1	0
13	1	0	0	1	1
14	1	0	1	0	0
15	1	0	1	0	1
16	1	0	1	1	0
17	1	0	1	1	1
18	1	1	0	0	0
19	1	1	0	0	1
20	1	1	0	1	0

4-2 Mode Indicating Circuit

Decording

Function data fed in from the Fi terminal of the YM616 is fed out from the Fo terminal and applied to the mode indicator circuit. According to these data, the circuit will turn on the respective LEDs which light up corresponding to the operation of the program operating button.



5. PROGRAM CONTROLLER AND ITS PERIPHERAL

■ Major Functions of Program Controller (YM616)

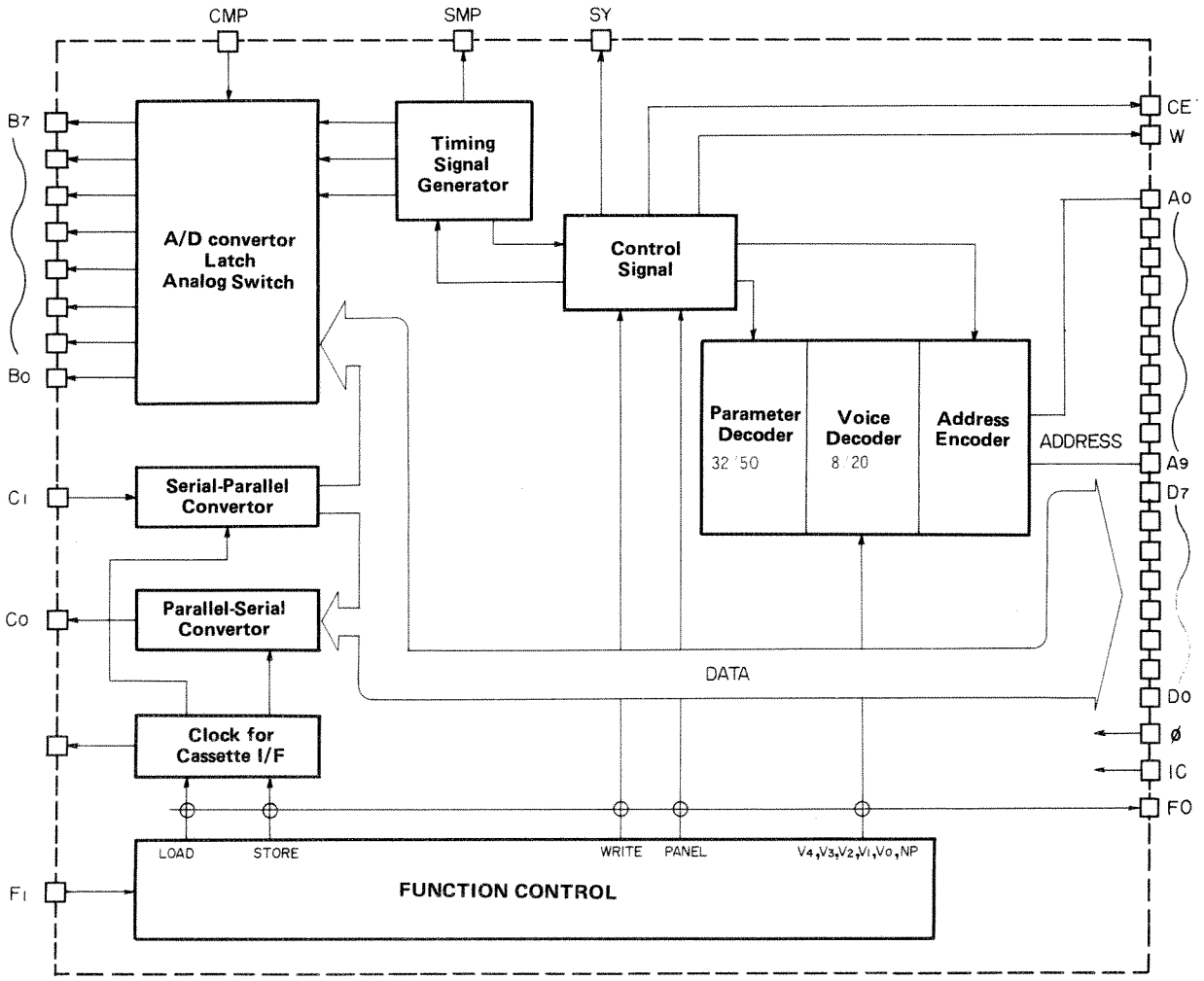
1) Function Mode Control . . . . . Determines the function mode of the programmer in accordance with the 10-bit function code that have been fed into Fi from the mode selecting circuit.

2) Function Mode Execution . . . . . According to the selected function code, performs exchange communicate of data with peripheral circuits and also controls them.

- ○ PANEL Mode → A/D and D/A conversions, generates Sample and Hold data.
- ○ VOICE WRITE Mode → A/D conversion, writing into RAM, (address selection and data output).
- ○ VOICE Mode → Reading from RAM, D/A conversion and Sanple and Hold.
- ○ STORE Mode → Transfer from RAM to tape.
- ○ LOAD Mode → Transfer from tape to RAM.

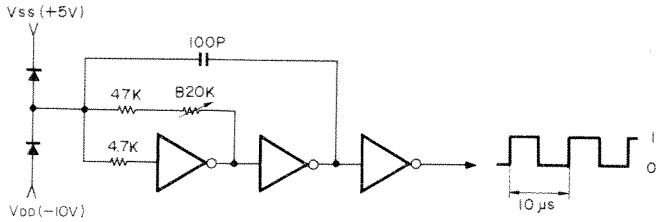
■ Outline of Operations of YM616

The block diagram for the YM616 and a description of the terminals are given below.



Master clock ϕ

All operations of the programmer block are synchronized with the master clock ϕ and the synchronizing pulse SY. As for ϕ, the master clock frequency of 100KHz is given to the entire circuit by means of the clock oscillator. Therefore, the programmer's operating bit is 10μs.

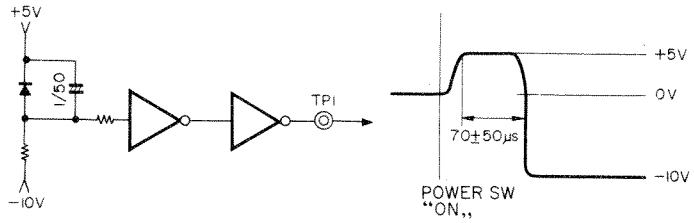


Synchro pulse · SY

Syncho-pulse SY is fed out from the SY terminal (Pin (38)) of the YM616 in synchronism with ϕ. The programmer starts operating following the timing at which these SY data are generated. The timing of SY is 5ms pitches.

Initial clock : IC

The IC terminal (Pin (6)) of the YM616 will be activated simultaneously with switch-on of power, setting the programmer to the PANEL mode.



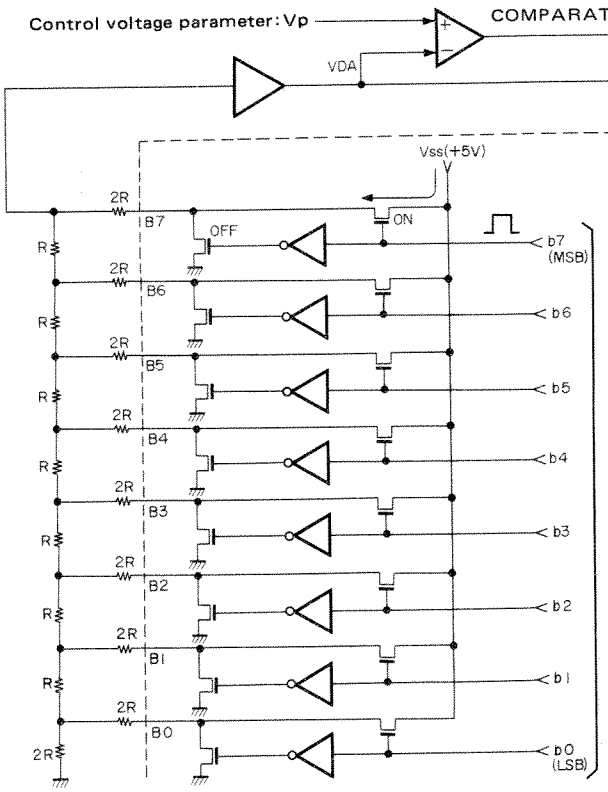
PIN	NAME	DESCRIPTION
1	Vss	+5 volt power supply
2	F_0	Function Data Output
3	CMP	Input for A/D Convert
4	Fi	Function Data Input
5	SMP	Sample and Hold control
6	IC	Initial clear Input
7	B_7	(MSB) } Bit Data Output
8	B_6	
9	B_5	
10	B_4	
11	B_3	
12	B_2	
13	B_1	
14	B_0	(LSB)
15	− 5 V	−5 volt power suplly
16	C_0	STORE Data Output
17	$\overline{D_0}$	※
18	$\overline{D_1}$	
19	$\overline{D_2}$	
20	$\overline{D_3}$	
21	$\overline{D_4}$	※ Memory Data Input/Output
22	$\overline{D_5}$	
23	$\overline{D_6}$	
24	$\overline{D_7}$	
25	Ci	LOAD Data Input
26	W	R/W Control
27	CE	Chip Select Output
28	$\overline{A_0}$	Address Data Output
29	$\overline{A_1}$	
30	$\overline{A_2}$	
31	$\overline{A_3}$	
32	$\overline{A_4}$	
33	$\overline{A_5}$	
34	$\overline{A_6}$	
35	$\overline{A_7}$	
36	$\overline{A_8}$	
37	$\overline{A_9}$	
38	SY	Synchronize Pulse Input
39	V_{DD}	−10 volt power suplly
40	ϕ	Master Clock Input

FUNCTION I/O : Fi, Fo

By receiving the function data encoded by the mode selecting circuit into the Fi terminal (Pin ⑥), the function modes of the YM616 are specified. At the same timing, function data are fed out from the Fo terminal (Pin ②) to the indicator circuit.

6. A/D, D/A CONVERSION CIRCUIT

The ladder resistor connected to YM616's $B_7 \sim B_0$ terminals (Pins ⑦ ~ ⑭) and terminals CMP (Pin ③) and SMP (Pin ②), together with such periphery circuits as ICs 7, 8, 9 and 10, make up the A/D and D/A conversion circuit. When in the PANEL mode, A/D and D/A conversions are performed, while in the VOICE mode D/A conversion alone is performed. The basic circuit diagram is shown below.



HOW TO CONVERTE

This state can be compared to the following example. 8 bits (0 - 255) are used for expressing voltage from 0 to 5 volt (Vss). Let us assume for example that 2.00 volts is fed in as Vp.

Since $\frac{2.00}{5.00} \times 255 = 102$, we shall consider it as 102

102 < 128	RESET	" 0 "	b_7 (MSB)
102 > 64	SET	" 1 "	b_6
102 > 64+32		" 1 "	b_5
102 < 64+32+16		" 0 "	b_4
102 < 64+32	+ 8	" 0 "	b_3
102 > 64+32	+ 4	" 1 "	b_2
102 = 64+32	+ 4 + 2	" 1 "	b_1
102 < 64+32	+ 4 + 2 + 1	" 0 "	b_0 (LSB)

MSB LSB

As a result, 8 bits such as "0 1 1 0 0 1 1 0" is obtained.

A/D Procedures

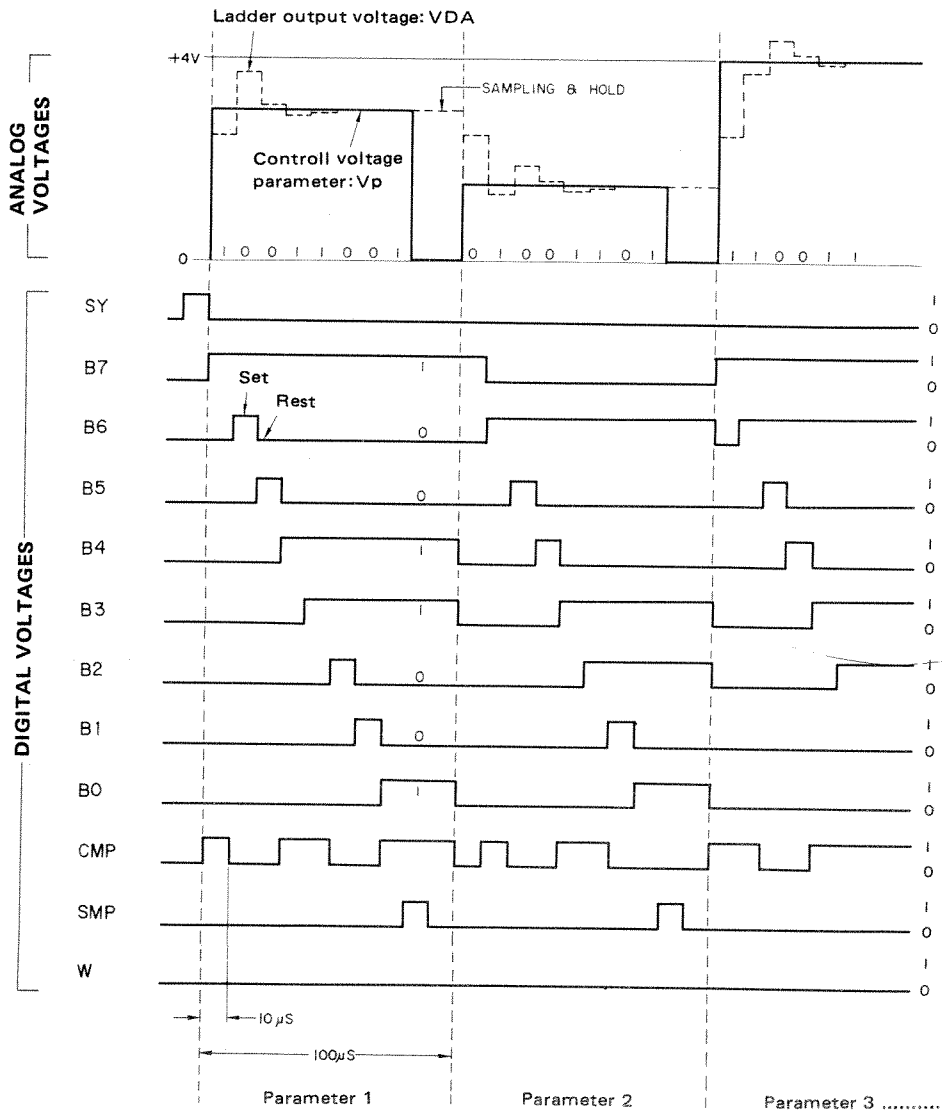
In the A/D and D/A conversion circuit, A/D and D/A conversion processing is performed by comparing the voltage parameters that are sent in from the multiplexer with the output voltages of the ladder network connected to the $B_7 \sim B_0$ terminals of the program controller (YM616). A converting system such as this known as a method of successive comparison. The operations proceed in the following sequence.

1. Synchronizing with the master clock ϕ, the program controller (YM616) sets the B-terminals (from B_7 downard) to "1" to generate the ladder output voltage. (D/A conversion)
2. After comparing the parameter control voltage with the ladder output voltage by means of the A/D converter (Voltage comparator), the compared results are fed into the CMP terminal.

$V_p > V_{DA}$ CMP terminal is "1" V_p : Parameter control voltage

$V_p < V_{DA}$ CMP terminal is "0" V_{DA} : Ladder's output voltage

3. When "1" is returned to the CMP terminal, it will cause the corresponding Bn terminal to be held in the condition of "1" and "1" is set into the next Bn−1 terminal as a result. When "0" is returned to the CMP terminal, the corresponding Bn terminal will be reset ("0").
4. As for the output voltage of the R-2R type ladder network, Vss/2 (2.5V) will generate when "1" is set in B_7. When B_6 is "1", the output voltage will decrease at a 1/2-fold rate (2.5 V/2). As a result, the output voltage (V_{DA}) that has become "1" is added.
5. The parameter control voltages will be compared sequentially in the order from B_7 down to B_0, the terminal at which, A/D and D/A conversion will be completed. At this point, $V_p = V_{DA}$.
6. After A/D and D/A conversions have been completed, the SMP terminal will be set to "1", causing the ladder output voltage to be "sample-held".
7. The above operations will be performed for all the 50 parameters, after which, the process will be repeated again from Parameter 1.



7. MEMORY CIRCUIT, AND ITS PERIPHERAL

To enable writing into RAM (VOICE WRITE & LOAD Mode), and reading from RAM (VOICE & STORE Mode), the program controller YM616 is provided with the following 4 types of terminals, which are either directly connected to RAM, or connected by way of a gate ICs.

Addressing : $A_0 \sim A_9$

Terminals $A_0 \sim A_9$ (Pins (28) ~ (37)) select addresses to enable data communication with RAM.
In the case of the CS-40M, which has a total of 50 parameters and 20 voices with one parameter corresponding to one address, a toral of 1,000 addresses consisting of 0 ~ 999 is required. The following chart shows the starting address of each voice.

STARTING ADDRESS

Address / Voices	NP=1, 20 Voices, 50 parameters										Address in Decimal
	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	L	L	L	L	L	L	L	L	L	L	0 - 49
2	L	L	L	L	H	H	L	L	H	L	50 - 99
3	L	L	L	H	H	L	L	H	L	L	100 - 149
4	L	L	H	L	L	H	L	H	H	L	150 - 199
5	L	L	H	H	L	L	H	L	L	L	200 - 249
6	L	L	H	H	H	H	H	L	H	L	250 - 299
7	L	H	L	L	H	L	H	H	L	L	300 - 349
8	L	H	L	H	L	H	H	H	H	L	350 - 399
9	L	H	H	L	L	H	L	L	L	L	400 - 449
10	L	H	H	H	L	L	L	L	H	L	450 - 499
11	L	H	H	H	H	H	L	H	L	L	500 - 549
12	H	L	L	L	H	L	L	H	H	L	550 - 599
13	H	L	L	H	L	H	H	L	L	L	600 - 649
14	H	L	H	L	L	L	H	L	H	L	650 - 699
15	H	L	H	L	H	H	H	H	L	L	700 - 749
16	H	L	H	H	H	L	H	H	H	L	750 - 799
17	H	H	L	L	H	L	L	L	L	L	800 - 849
18	H	H	L	H	L	H	L	L	H	L	850 - 899
19	H	H	H	L	L	L	L	H	L	L	900 - 949
20	H	H	H	L	H	H	L	H	H	L	950 - 999

Function code

The address is determined by the state of $V_4 \sim V_0$ and L and S of the function code. For example, when the function mode is VOICE/WRITE, the corresponding address is selected at the same time the voice address to be memorized is selected. This will cause data to be written into that address one after another. By contrast, when the VOICE mode is selected, the address that corresponds to that VOICE No. will be selected, and data will be read into that certain address.

Data I/O : $D_0 \sim D_7$

Terminals $D_0 \sim D_7$ (Pins ((17) ~ (24)) are terminals used both for input and output when data are communicated between RAM and terminals $D_0 \sim D_7$, according to the function code.

When, in the VOICE/WRITE mode, A/D-converted voice data will be fed out to RAM. However, in the VOICE mode, the data of a selected address inside the RAM will be fed in, and by being D/A-converted, will control the certain blocks.

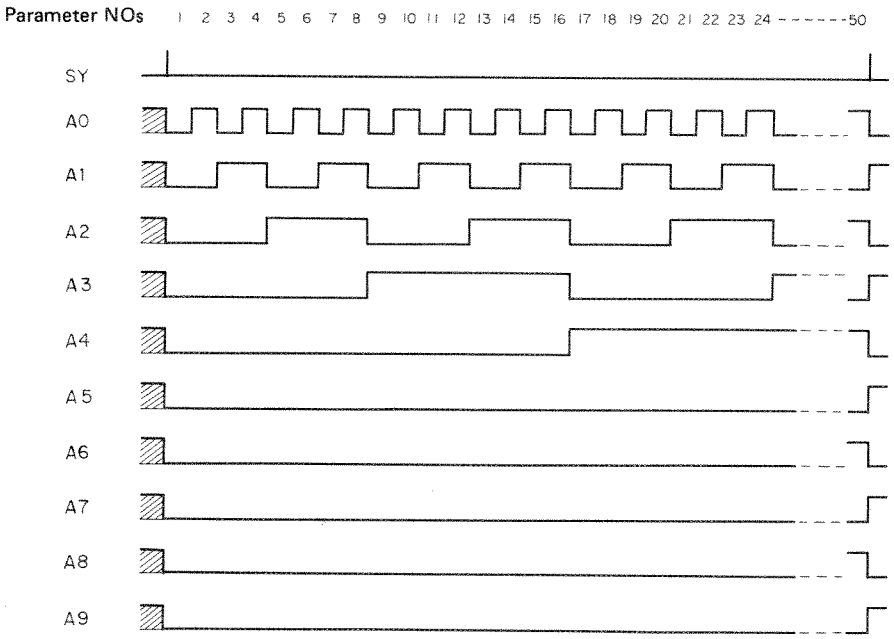
W (Write)

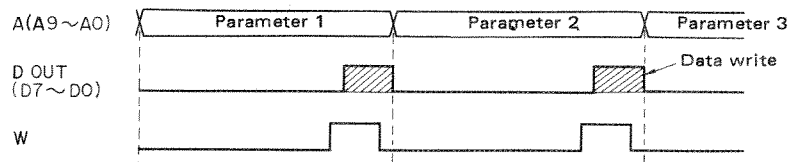
The W terminal (Pin (26)) is an output terminal used for specifying whether WRITE ("1"), or READ ("0") is to be performed for RAM.

CE (Chip Enable)

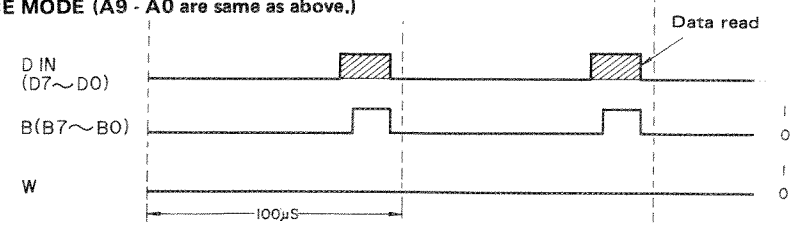
The CE terminal (Pin (27)) outputs data needed for determining the state of RAM. When in the "1" state, the RAM will be activated.
Shown below is a timing chart for these terminals.

2. VOICE WRITE MODE (B7 - B0 and CMP timing are same as PANEL mode.)
Parameter Nos.





3. VOICE MODE (A9 - A0 are same as above.)



■ RAM (RANDOM ACCESS MEMORY)

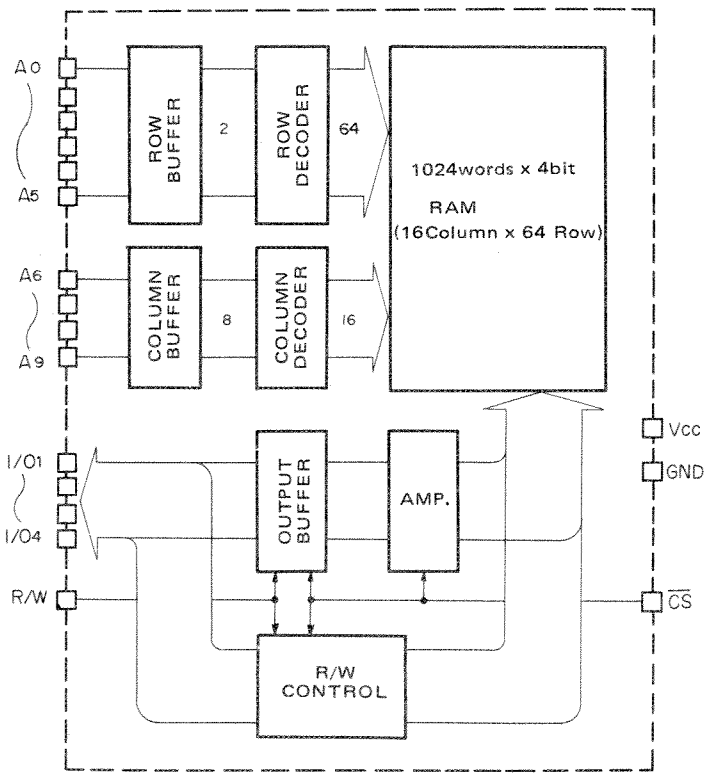
RAM, which stands for Random Access Memory is an IC used for memory and can READ or WRITE freely into any desired adress of the large number of addresses. Here, we shall describe the RAM employed in the CS-40M, that is, the M58981S45, which has a memory capacity of 1024 words x 4 bits.

1. Memory capacity required for the CS-40M

1. The number of voices that can be memorized: 20 voices
2. The number of parameters that can be used for composing one voice: 50 parameters
3. The parameter control voltage is memorized into the RAM, after being A/D-converted into an 8-bit digital data.
4. The memory capacity required for memorizing CS-40M's 20 voices will be "8 x 50 x 20 = 8,000 bit = 8 Kbit = 2 x 4Kbit, meaning that two RAMs, each having a memory capacity of 4Kbits are needed.
5. Similarly, in the case of the CS-20M, to memorize the 8 voices and 32 parameters, a memory capacity of 8 x 32 x 8 = 2,048 bit = 2Kbits = 2 x 1 Kbits are needed, or two RAMS, each having 1Kbit, are needed.

2. Address Selction and Take-in of Data

The following figure gives the block diagram of the M58981S-45.



PIN	NAME	DESCRIPTION
1	A_6	Address Data Input
2	A_5	
3	A_4	
4	A_3	
5	A_0	
6	A_1	
7	A_2	
8	$\overline{CS}$	Chip Select Input
9	GND	0 Volt
10	$R/\overline{W}$	R/W Command Input
11	I/O_4	Data Input/Output
12	I/O_3	
13	I/O_2	
14	I/O_1	
15	A_9	Address Data Input
16	A_8	
17	A_7	
18	Vcc	+5 Volt Power supply

Address selection is performed by using the binary data fed in from the 10 address selecting terminals (A0 ~ A9) of the YM616. That is, since it is a binary number of 10 bits, the 10 address inputs may be divided into six row inputs and 4 column inputs, that is, into a matrix consisting of 2^6 = 64 rows and 2^4 = 16 columns. This matrix will determine which of the addresses from 0 through 1.023 is to be selected.

With regard to data, it is possible to memorize a 4-bit data for one address, since there are 4 data input/output terminals (I/O 1 ~ 4). As it incorporates two M58981-45s, the CS-40M can memorize data of 20 voices x 50 opera-

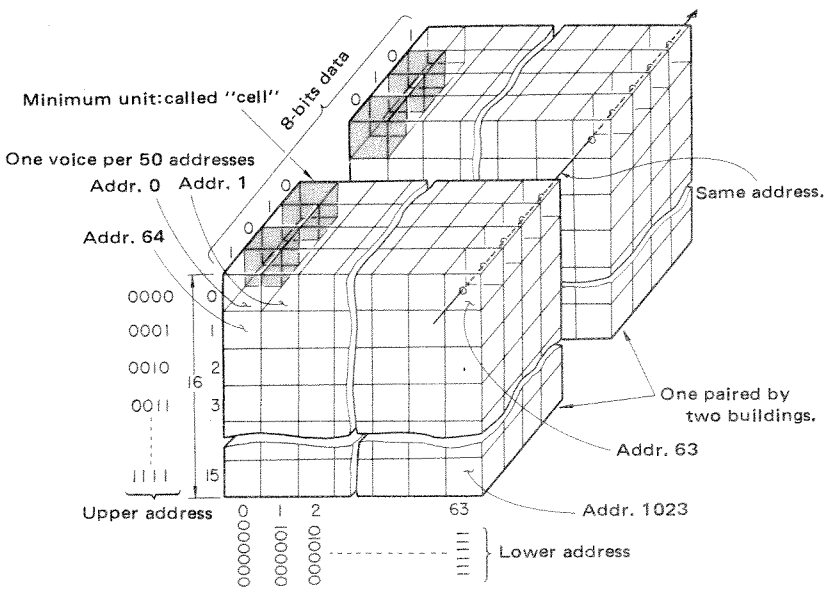
meters. Address data A0 though A9 that are sent in from the program controller will select the same addresses for the two RAMs. The 8-bit data from D0 to D7 will be divided into two groups, one consisting of the higher-order data, D7 through D4, and the other of the lower-order data, D3 through D0, and will be fed into the two RAMs. In other words, by using two "1,024 words x 4 bits" RAMs, a RAM of "1,024 words x 8 bits (8-bit data can be memorized into 1.024 addresses)" can be formed.

3. Operation of M68981-45

In the M58981-45, the data terminals are used both for input and output.
In the R/W terminal state, R (READ) and W (WRITE) controls are effected. During WRITE, the address is selected by address data A0 through A9. When the R/W terminal is brought to the "L" level, it will cause data of the I/O terminal of that certain time to be written in. On the other hand, during READ, the desired address will be selected by address data A0 through A9 and by bringing the R/W teminal to the "H" level, the data of the selected address will be be called out to the I/O terminal.
CS (Chip Select) is an input terminal that determines whether to bring the RAM to an active state or to an inactive state. When this terminal is brought to the "H" level. it will put the RAM in the inactive (stop) state where it will be impedance state. The R/W terminals are controlled from the W terminal of the programmer controller, and CS (Chip Select), which will be set to the "H" level when the voltage becomes in stable during switch-on and switch-off of power, serve to prevent erroneous operations from taking place by disabling operation.

Hints

This state of the RAM may be likened to two massive, 16-storied buildings such as shown in the drawing. Each floor will have a number of "4 rooms x 64", with 8 rooms forming a compartment. Each compartment is given an address such as 0, 1, 2 . . . . . starting from the left end. If we decide to have "1" indicate the state in which each room will be lighted, and have "0" indicate that in which all the lights will be out, it will be possible to express the state of address "0", for example, as "10100101". In this way, every address can be selected by specifying how many doors down from the left end and on what floor it is to be found. The RAM is a memory element that can turn on or turn out (WRITE) the lights of the 8 rooms of whatever address, and can examine (READ) the condition of lighting. Naturally, if the power supply to the building is interrupted a blackout cannot be avoided. But RAM is prepared for this situation too, as it has a battery to keep power supply uninterrupted.



8. CASSETTE INTERFACE

8-1 STORE Mode

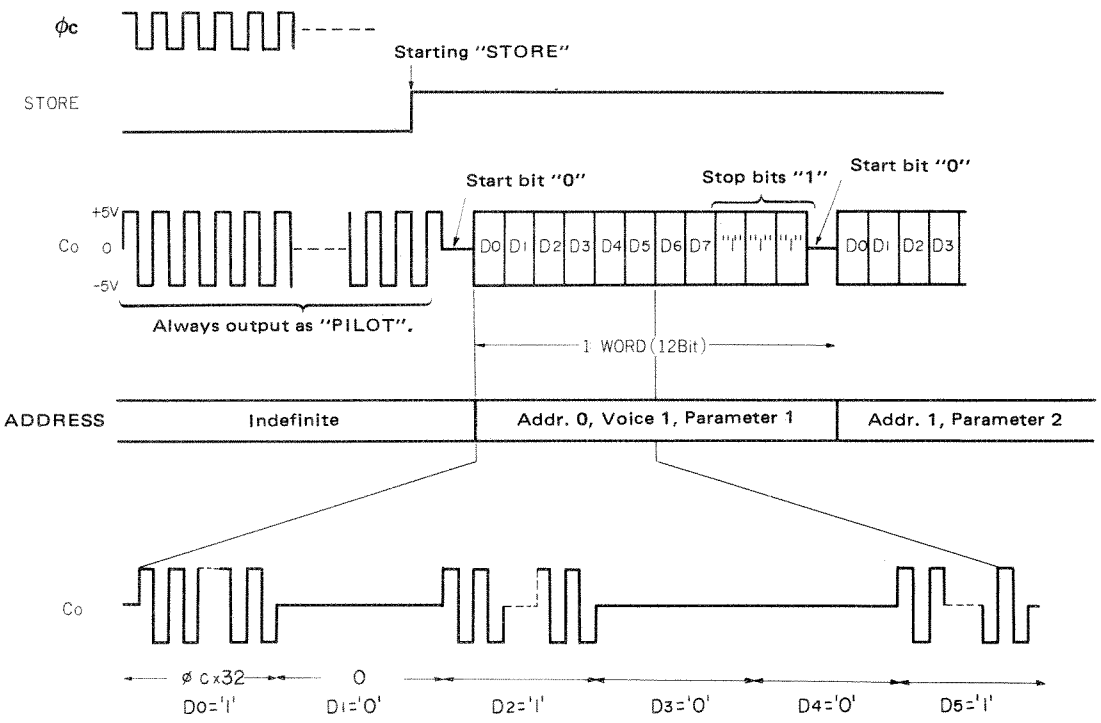
3KHz tone burst

A clock ϕc (f = 3.125KHz) whose frequency is 1/12 of that of the master clock ϕ is constantly fed out from the Co terminal (Pin ⑯) of YM616. When the STORE bit of the function code is set to "1", the data memorized into RAM will be fed out from the Co terminal in the form of TONE BURST. Fig. 1 shows the output timing of STORE data.

(Conception of bit in the STORE mode)

Basic clock $\phi c = 320\mu s$
1 Bit = ϕc x 32 clock
1 word = 12 bit (Interval needed to STORE data for a parameter)

When all voice data have been stored, the function mode is restored to PANEL, and with this, STORE operations are completed.
The following chart is the STORE data timing chart.



Time for STORE & LOAD

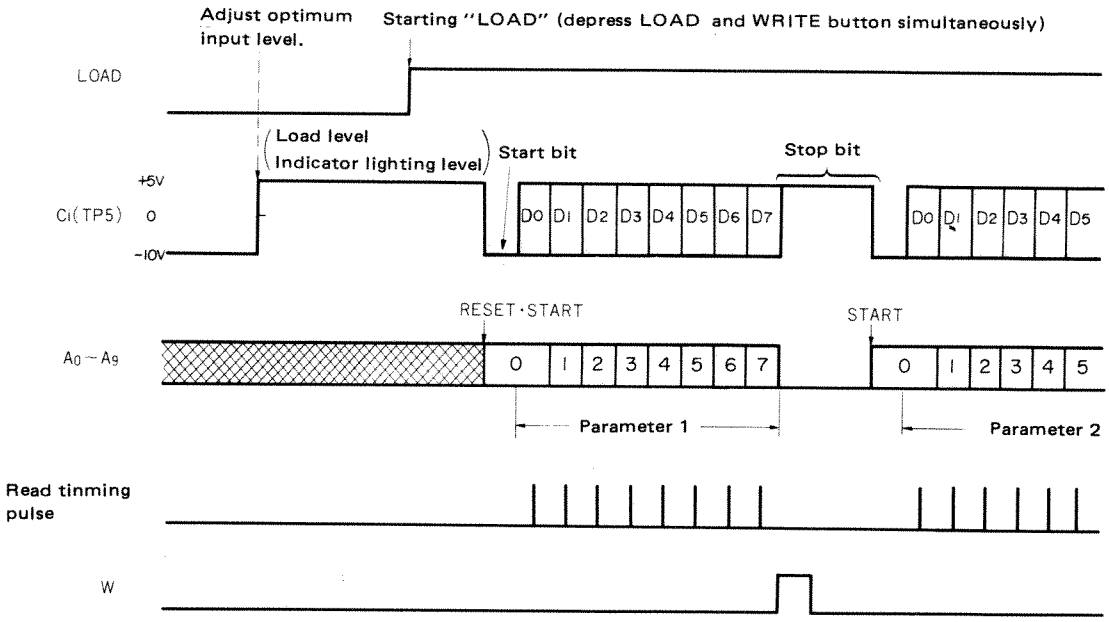
(Time required for STORE)

1 bit = ϕc x 32 clocks = 320μs x 32 = 10.24ms
1 word = 12 bit x 10.24ms = 122.88ms
For 20 voices and 50 parameters . . . . . Slightly more than 2 minutes
For 8 voices and 32 parameters . . . . . 32 seconds

8-2 LOAD Mode

Into pulse

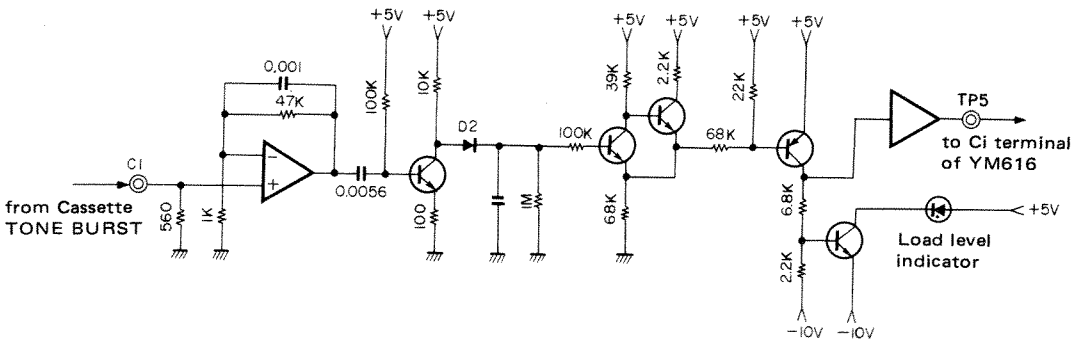
Data recorded on a tape in the STORE mode, after being fed in from the C1 terminal (C2-1) of the PGM c. board, pass through the waveform shaping circuit, and then are fed into the C1 terminal (Pin (25)) of the YM616.
The following chart shows the timing of LOAD data input.



Start bit

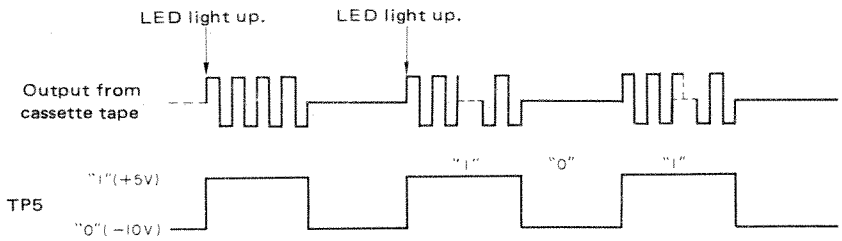
When the function mode is changed over to the LOAD mode, the START bit will cause the address to be reset to address "0" (The location to memorize data of parameter 1 of Voice 1, in other words, the FEET of VCO 1.). In this way, loading begins, starting from Parameter 1 of Voice 1. When LOAD for Parameter 1 is completed, the address counter will stop for the duration of the STOP bit. LOAD will be restarted with the next START bit. In this way, LOAD operations are performed for each voice. When LOAD for all the voices are completed, the function mode is restored to PANEL to complete LOAD operations. The time required for LOAD is the same as that required for STORE.

■ WAVEFORM SHAPING CIRCUIT



Waveform shaping

The signals recorded on a tape are, as mentioned earlier, tone burst signals of 3.125KHz. That is, burst signals will appear when the data is "1". When it is "0", which is a NO SIGNAL state, recording will take place. At the waveform shaping circuit, this signal will be converted into digital data.



TP5

When the output of the taperecorder is adjusted while the pilot signal is being reproduced and when the optimum input level that permits LOAD is reached, TP5 will become "1" (+5V), causing the LED to illuminate. In other words, it will be "1" when the clock is being generated, and will be "0" during NO SIGNAL, the state which permits data to be loaded.

8-3 Input/Output Characteristics Of STORE And LOAD

The characteristics of the "TO TAPE" and "FROM TAPE" terminals on the rear panel are shown below.

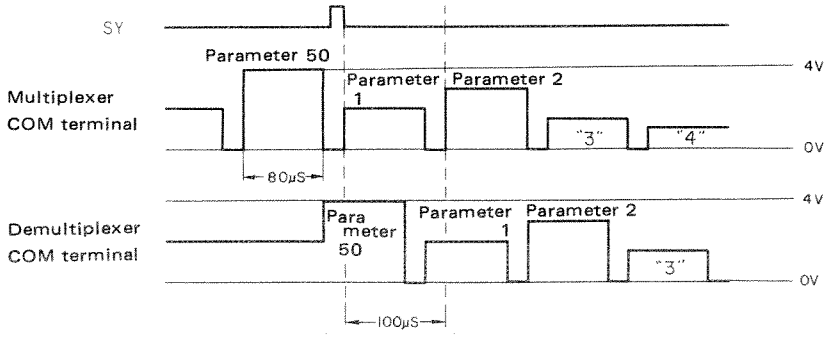
TO TAPE	Output impedance	560 Ω
	Output level	100 ± 10m$V_{p\text{-}p}$
FROM TAPE	Input impedance	560 Ω
	Optimum input level	0.5$V_{p\text{-}p}$ (Should permit LOAD at 100mV ~ 1$V_{p\text{-}p}$.)

9. DEMULTIPLEXER

Serial-in parallel-out

The demultiplexer may be considered as being a unit for which the input-output relationship of the multiplexer is reversed. While the multiplexer performs PARALLEL-IN and SERIAL-OUT operations, which consist of feeding out a plural number of voltages that generate simultaneously, after arranging them in sequence at a certain timing, the demultipexer performs SERIAL-IN and PARALLEL-OUT operations which consist of converting the input signals (arranged sequentially at a certain timing) into a plural number of output voltages.

The following chart is a timing chart of the parameter control voltages that are obtained at the COM (output) terminal of the multiplexer and the COM (input) terminal of the demultiplexer.



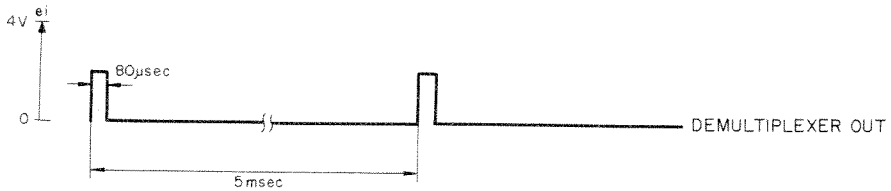
As will be seen from the timing chart just given, the control voltage parameter obtained at the COM terminal of the demultiplexer has a delay of 80μs compared with that obtained at the COM terminal of the multiplexer. This arrangement has been taken because 8 bits are needed for performing successive comparison at the A/D, D/A converter, so that the S/H gate opens at the 9th bit.

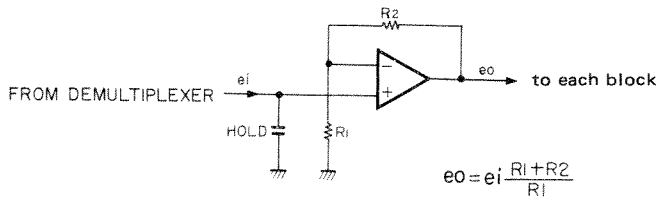
■ S/H, Output Amplifier

Hold

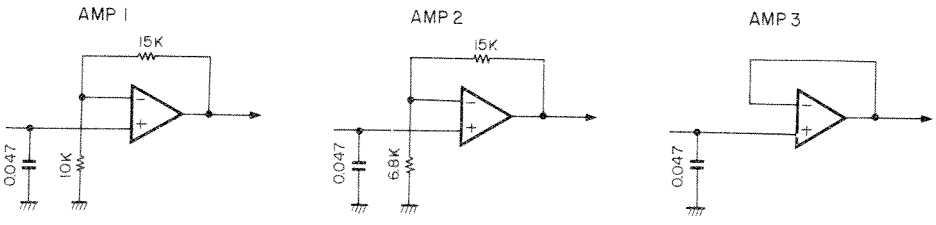
In the demultiplexer, a voltage parameter having a width of 80μsec is fed at a timing of once every 5msec to each output terminal. Therefore, it will be necessary to hold this pulse and convert it into direct current in order to apply this control voltage to the respective blocks. To achieve this, high-impedance buffers, or amplifiers are connected to the output terminal of the demultiplexer to have the capacitor perform HOLD (smoothening) operations. These amplifier comprise 3 types, two of which, function as DC amplifiers.

Demultiplexer Output Waveform





Integrated Waveform

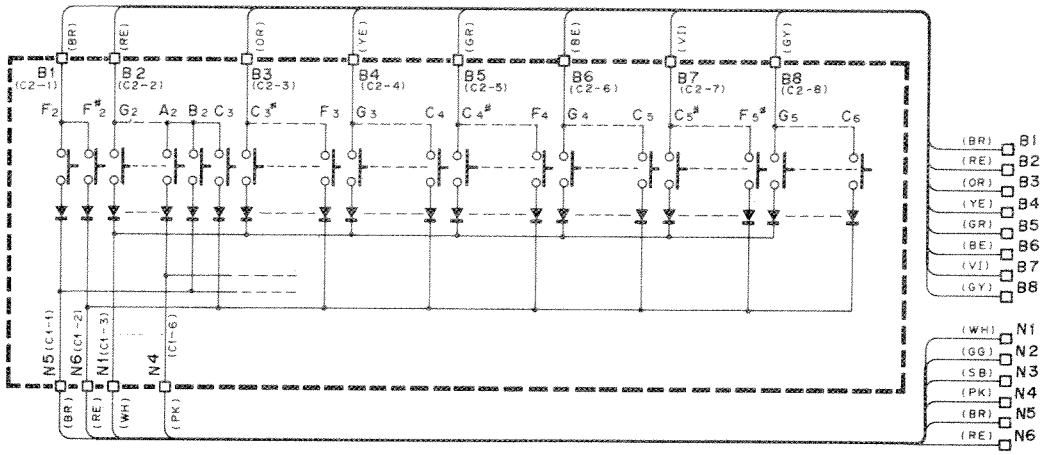


MEMO

KEYBOARD BLOCK

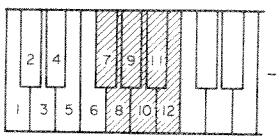
Circuit

The CS20M is composed of 37 keys and the CS-40M of 44. We shall explain the keyboard, taking the CS-40M as the example.

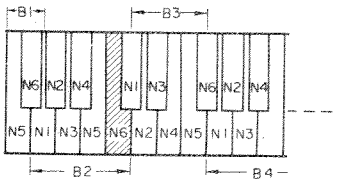


Octave & note

As will be seen from Figure, in the keyboard circuit, the key switches are divided into semi-octave blocks ($B_1 \sim B_8$) and "Semitone x 6" note blocks ($N_1 \sim N_6$) in order to detect the key that has been depressed.
When a key is depressed, it causes one of the semi-octave blocks to be connected with one of the note blocks by way of a diode. As a result, it is possible to know which key on the keyboard has been depressed.



One octave consists of "A seminote x 12". Here, one octave is divided into semi-octaves, that is, "A seminote x 6"



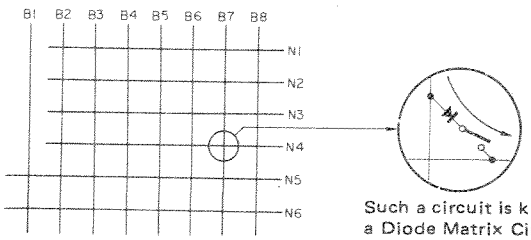
In the CS-40M, semi-octave and note blocks are allocated as shown in the drawing.

For example, when the key ▒ is depressed, B2 and N6 will become conductive.

Diode matrix

Such a circuit is known as a "Diode Matrix Circuit".

The circuit may be also written in the graphic expression as given below.

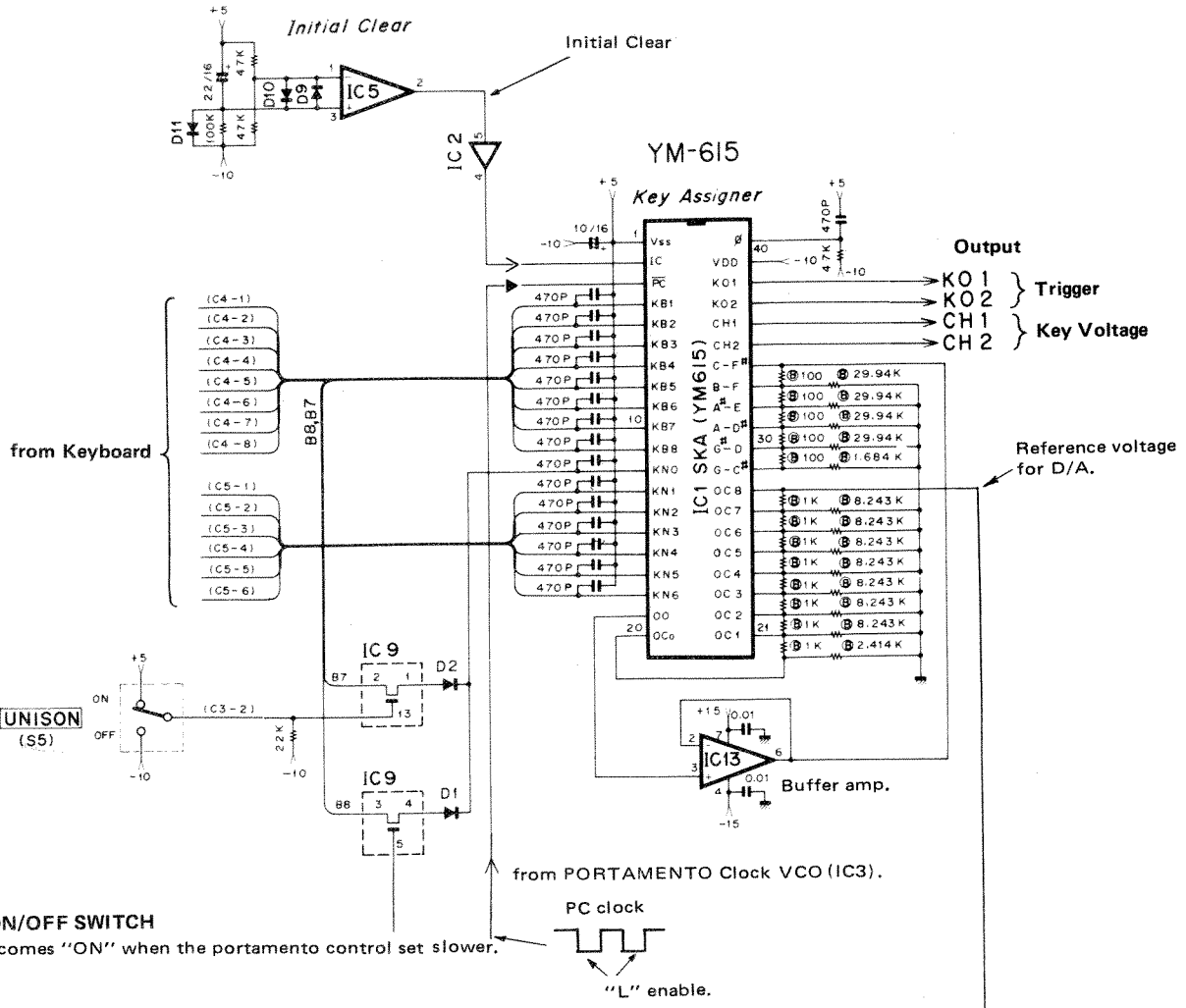


Such a circuit is known as a Diode Matrix Circuit.

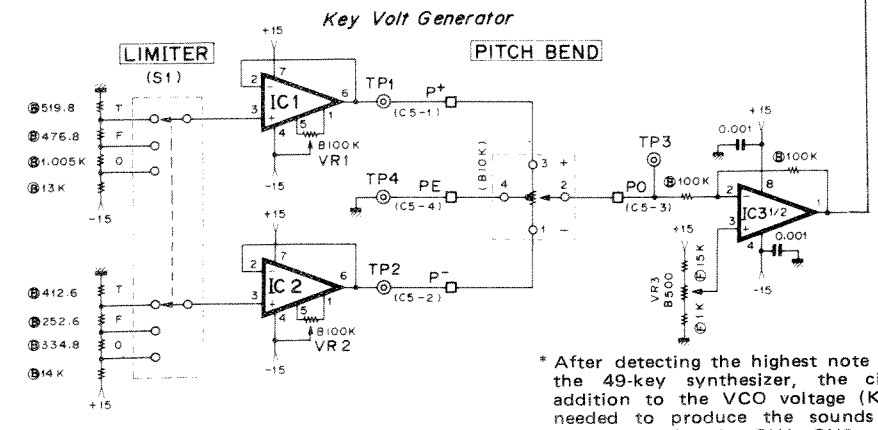
KEY ASSIGNER BLOCK: SK BOARD

Circuitry

The key assigner circuit is composed of the LSI (YM615) located on the SK c. board and the its periphery circuits. The YM615 is capable of controlling inputs of 49 keys. Of this controlling capacity, the CS-20M uses only a portion for 37 keys, and the CS-40M a portion for 44 keys. This being the case, it should be understood that there will be some difference between the actual circuit and what is explained here.



Generates Refernce voltage to apply D/A ladder network.



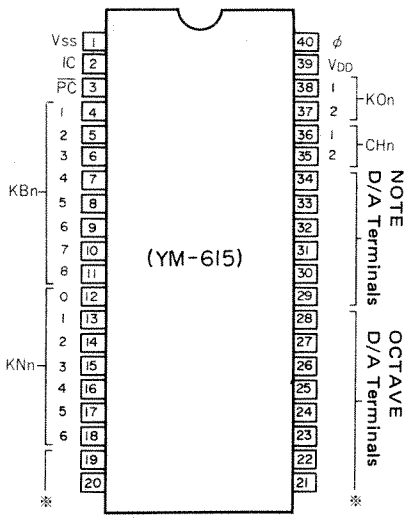
* After detecting the highest note and lowest note o the 49-key synthesizer, the circuit generates in addition to the VCO voltage (Key voltage) that is needed to produce the sounds of the two notes simultaneously, the CH1, CH2 and KEY ON signals (Trigger), KO1 and KO2.

* As functions, it has Portamento effect (PC) and Polyphonic/Monophonic (MP) function.

Major Functions of Synthesizer Key Assigner (YM615)

1) After detecting the highest note and lowest note of the 49-key synthesizer, the circuit generates, in addition to the VCO voltages (Key Voltage) there are needed to produce the sounds of the two notes simultaneously, the CH1, CH2 and KEY ON signals (trigger signals), KO1 and KO2.
2) As functions, it has Portamento treatment (PC) functions and Duophonic/Monophonic, 2 channel selecting (UNISON) functions.

1-1 Pin Connections And Basic Circuit Composition



PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	V_{SS}	+15 volt power supply	21	OC_1	※ Octave D/A Terminals
2	I C	Initial Clear Input	22	OC_2	
3	$\overline{PC}$	Glissand Clock Input	23	OC_3	
4	KB_1	Semi Octave Code Input	24	OC_4	
5	KB_2		25	OC_5	
6	KB_3		26	OC_6	
7	KB_4		27	OC_7	
8	KB_5		28	OC_8	
9	KB_6		29	G-C#	NOTE D/A Terminals
10	KB_7		30	G#-D	
11	KB_8		31	A-D#	
12	KN_0	Note Code Input	32	A#-E	
13	KN_1		33	B-F	
14	KN_2		34	C-F#	
15	KN_3		35	CH_2	KV (Key voltage) Output
16	KN_4		36	CH_1	
17	KN_5		37	KO_2	KON (Trigger) Output
18	KN_6		38	KO_1	
19	OO	※	39	V_{DD}	−10 volt power supply
20	OC_0		40	φ	Master Clock Input

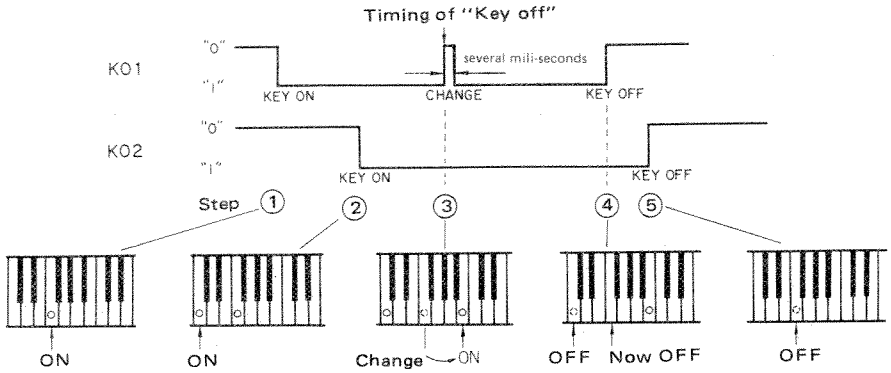
Key Voltage

As for channel assignment, the KV signals are assigned in the order of key-off. However, when the next depressed Key is of the same pitch (key on again) of the key whose key-off has just taken place, the KV will be assigned to the same channel.
When a new key has been depressed and if the mode differs from that of the other channel, the KV is fed out. At key-off, the last data that has been fed out will be held. And UNISON switch is on or single key is depressed, KV will assigned to both CH1 and CH2.

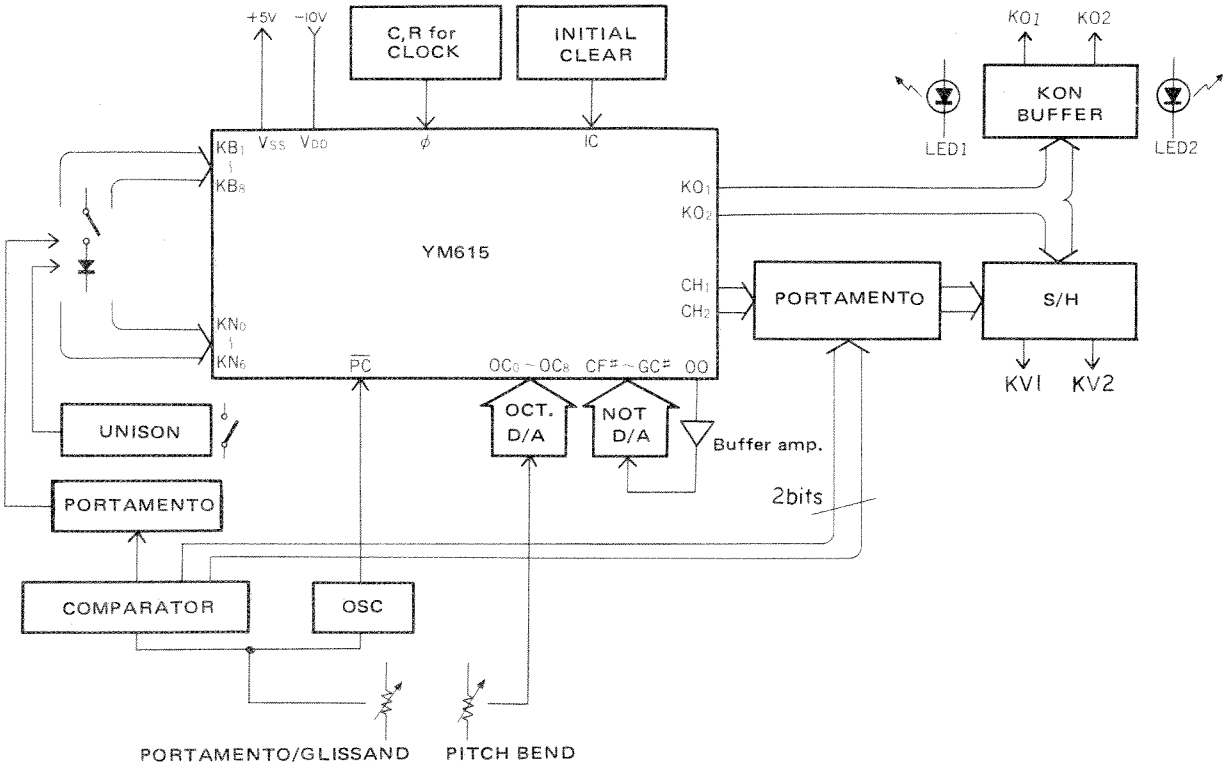
Trigger

When two notes are depressed at UNISON switch is off, both KO1 and KO2 will become "L" , whereas when only one note has been depressed, "L" will be fed out to either CH1 or CH2. When the key data has changed, as when a key of a pitch higher than that of the two previously depressed keys, the

output will once become "H" and then after several mili-seconds will change to "L".
When the key is released, the output will change to "H".

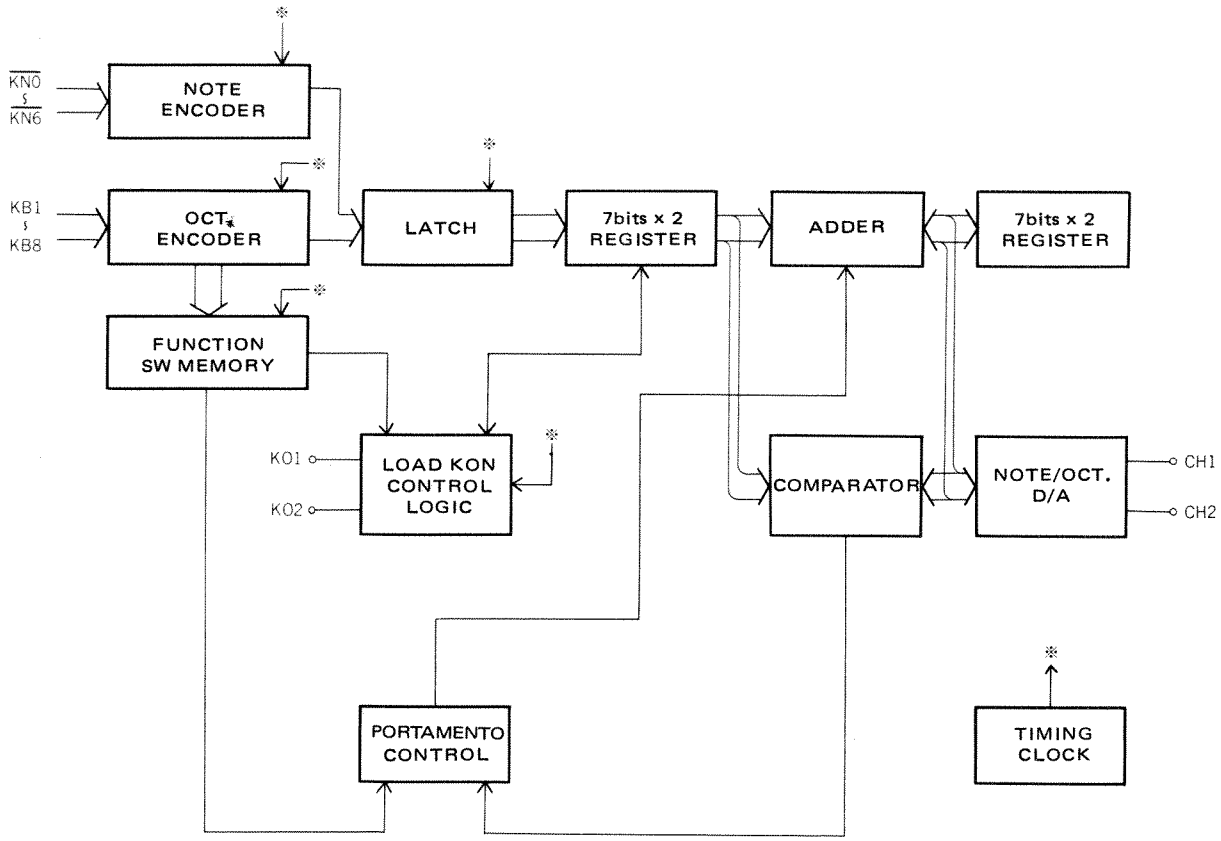


1-2 Block Diagram of Key Assigner Block



OPERATING PRINCIPLE

The Inside block diagram of the YM615 is shown below.



SKA Functions

Inside the SKA, all processings are performed in synchronism with the period of the timing clock generator. The substance of processing can be largely divided into the following 4 groups:

1. Encoding of key data
2. D/A conversion
3. Grissando (Portamento) Processing
4. Function Control

1. ENCODING OF KEY DATA

Encoder

Semioctave data inputs, KB1 ~ KB8 and note data inputs, KN1 ~ KN6 that are fed out from the keyboard circuit are encoded, by encoders into 4-bit and 3-bit binary numbers, respectively. After being encoded, the total 7bit data (4bits plus 3bits) are sent to the latch*, where they are descriminated by the LOAD and KEY ON control logic as to whether they are pitch data of the highest note and lowest note, or not. If they are descriminated as necessary data, they are sent to the register** of Ch1 or Ch2. At the same time, the Key On Trigger signal is fed out to KO1, or KO2.

These operations are all performed in an orderly manner at high speed, synchronizing with the timing clock.

* Latch: A place where digital data is held temporarily.

** Register: Similar to the IC memory, it is a place where data is memorized.

Coding List

Key data that have been encoded into a 7-bit binary number is processed inside the SKA in the following manner. When KN0 and KB8, or KN0 and KB7 become conductive when the FET switch is operated, the lower 3bits will become "000", so that the key data will become a code that represents the function, that is POR (Portamento processing), or MP (Mono-phonic 2 channel). This data will be processed in a different way from which the code denoting the pitch is. When the lower 3 bits of the note code data are not "000", such correspondence as shown in the Note Code Data Chart will be established between the data and pitch.

Semi-octave data

BLOCK	B_4	B_3	B_2	B_1
KB8	1	0	0	0
KB7	0	1	1	1
KB6	0	1	1	0
KB5	0	1	0	1
KB4	0	1	0	0
KB3	0	0	1	1
KB2	0	0	1	0
KB1	0	0	0	1

Semi-note data

NOTE		N_3	N_2	N_1	Decimal
KN6	C - $F^{\#}$	1	1	1	7
KN5	B - F	1	1	0	6
KN4	$A^{\#}$ - E	1	0	1	5
KN3	A - $D^{\#}$	0	1	1	3
KN2	$G^{\#}$ - D	0	1	0	2
KN1	G - $C^{\#}$	0	0	1	1
KN0	Por,MP	0	0	0	0

KN0

In the case of CL (Lowermost Key: C2, KN0 and KB1 conducts), the lower 3 bits will be made "111" (as with the C-$F^{\#}$ channel) to descriminate it from POR and MP. The CS-20M and CS-40M, however, do not include the CL.

Key Data

Key data and functions obtained from matix KN0 – KN6 and KB1 – KB6 are as listed in the following table.

C2	$C2^{\#}$	D2	$D2^{\#}$	E2	F2	$F2^{\#}$	KB1
	G2	$G2^{\#}$	A2	$A2^{\#}$	B2	C3	KB2
	$C3^{\#}$	D3	$D3^{\#}$	E3	F3	$F3^{\#}$	KB3
	G3	$G3^{\#}$	A3	$A3^{\#}$	B3	C4	KB4
	$C4^{\#}$	D4	$D4^{\#}$	E4	F4	$F4^{\#}$	KB5
	G4	$G4^{\#}$	A4	$A4^{\#}$	B4	C5	KB6
MP	$C5^{\#}$	D5	$D5^{\#}$	E5 F	F5	$F5^{\#}$	KB7
POR	G5	$G5^{\#}$	A5	$A5^{\#}$	B5	C6	KB8
KN0	KN1	KN2	KN3	KN4	KN5	KN6	KB / KN

▒ marked notes are not used in the CS-40M. Further, ▒ marked notes are not used in the CS-20M.

Function Data

The 7-bit coding just described can be summarized as follows:
In the note data, the semitone between A and $A^{\#}$ ($D^{\#}$ and E) are denoted by "011 (3)" and "101 (5)", respectively: "100 (4)" is not used. In other words, when considered in relation to POR and MP function codes, it means that the 7-bit data whose lower 2 bits are "00" are not pitch data. A 3-bit binary number can express 8 numbers of from 0 through 7. The 6 notes of semi-octave are expressed by excluding two of them, that is "000" and "00", and using just six. It can be processed as a continuous 7-bit number by adding, or subtracting "2" right before, or after, the point where the lower two bits become "00", and using this together with the upper 4 bits. This point is an important point in Glissand (Portamento) processing.

2. D/A CONVERTER

This is a digital-to-analog converter circuit that genetates the key voltage that corresponds to the encoded key signal. Together with changes in the pitch, the frequency will change in the manner of an exponential coefficient. In this way, the converter is composed so that voltages that are proportional to the frequency variations can be obtained. It consists of a D/A converting section for semioctave data and that for note data.

Ladder network

The voltage sent in from the PITCH BEND control is divided in the manner of an exponential coefficient by means of the ladder network, after which, it is applied to the INPUT terminal of each gate.
This will cause the gate corresponding to the key code signal to open and select the required voltage. This semioctave voltage is applied to the ladder resistor for note data by way of a buffer amplifier, and voltage selection is performed in the same manner to obtain the required key voltage.
If, for example, 4.00V is applied from the PITCH BEND section, voltages such as shown below are obtained.

Terminals	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1
Voltages	4.000	2.828	2.000	1.414	1.000	0.707	0.500	0.354

As will be seen, an octave relationship (x 0.5) is established between every-other two voltages. Here, let us consider the case when 1,000V has been selected and applied to the ladder resistor for note data.

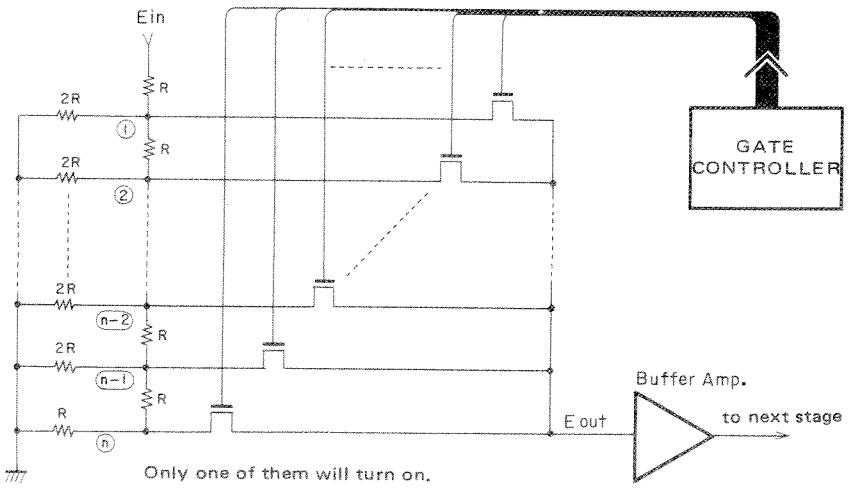
*

Terminals	C-F#	B-F	A#-E	A-D#	G#-D	G-C#
Voltages	1.000	0.9439	0.8910	0.8410	0.7938	0.7493

Let us take C-F# to B-F# where only one step of the steps of the ladder resistor has been passed. For example, the voltage has become 0.9439 times the former voltage.* Since one octave can be divided into twelve semitones, if we assume the voltage will become $0.9439^{12} = 0.500$ after 12 steps have been passed, we can see that the 0.5 (times) octave relationship is indeed established.

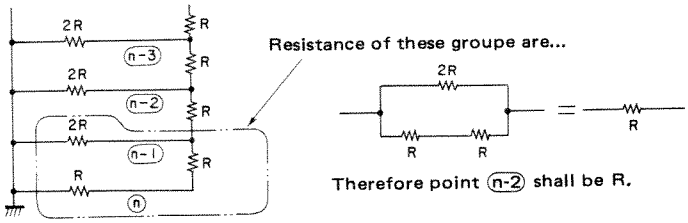
R-2R D/A mothod

Although it differs from the actual circuit, let us suppose a D/A converter in which an R-2R relationship is established as shown below.



n = 1/2 (n-1)

- As the voltage at Point (n−1) is divided by R and R, the voltage at Point (n) will be one half of that of Point (n−1) .
- Further, the synthetic resistance (2R and (R + R)) of the 3 lines grounded from Point (n−1) shall be R. Consequently, the voltage at Point (n−1) will be one half of that of Point (n−2).
- Similarly, as the synthetic resistance of the 5 lines grounded from Point (n−2) shall be "R", the voltage at Point (n−2) will also become one half of the voltage at Point (n−3) .



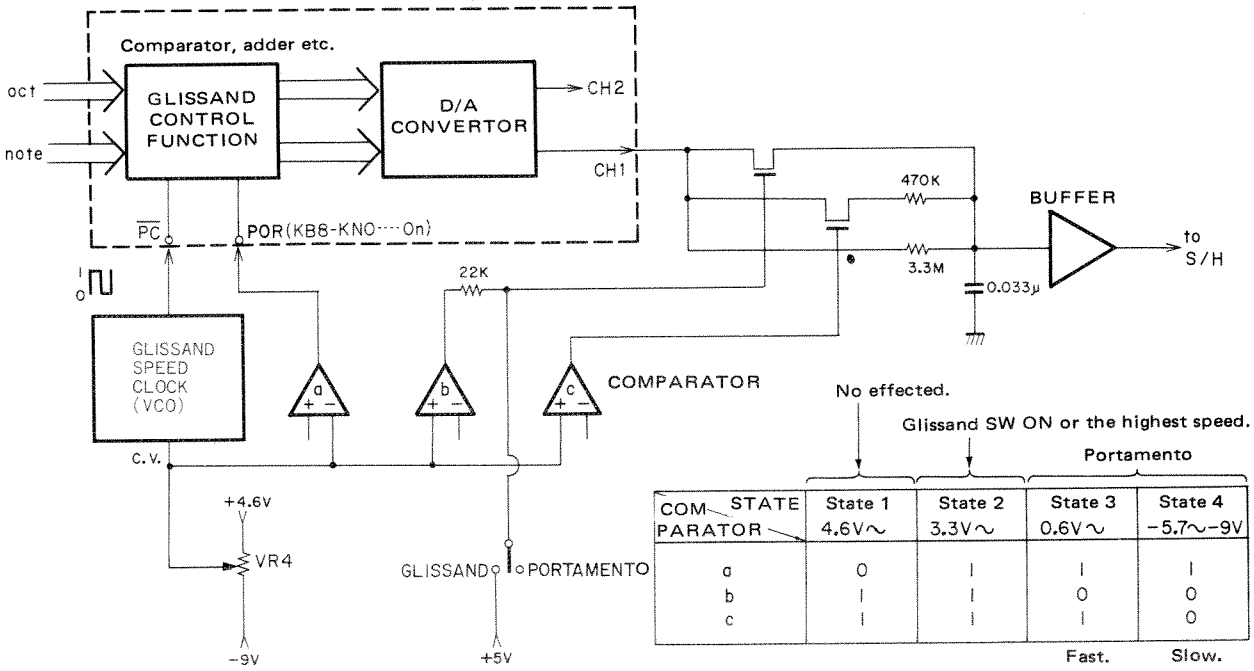
In this way, we can see that the resistance grounded from (n) , (n−1) , (n−2) . . . . . (1) are all "R" and is one half of the voltage of the previous step. In other words, for a ladder resistor having a R-2R relationship, no matter how many steps may be added, the relationship will be always established. This means that a D/A converter having an octave relationship where the voltage will be 1/2 has been established.

The D/A converter employed in this synthesizer, is set to a resistance that will enable a $1/\sqrt{2}$ and $1/2^{12}$ relationship to be established, instead of a 1/2 relationship. But the operating principle is exactly the same.

Meanwhile, as the resistors to be used for the ladder resistor are components that assume great importance in determining the accuracy, Class B (0. 1 %) metallic film resistors should be used.

3. GLISSAND (PORTAMENTO Processing)

GLISSAND processing is performed inside the YM615, while PORTAMENTO is by the integrating gate. The basic circuit is shown below.



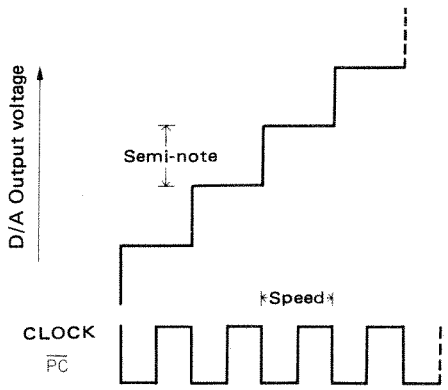
COMPARATOR \ STATE	State 1 4.6V∼	State 2 3.3V∼	State 3 0.6V∼	State 4 −5.7∼−9V
a	0	1	1	1
b	1	1	0	0
c	1	1	1	0

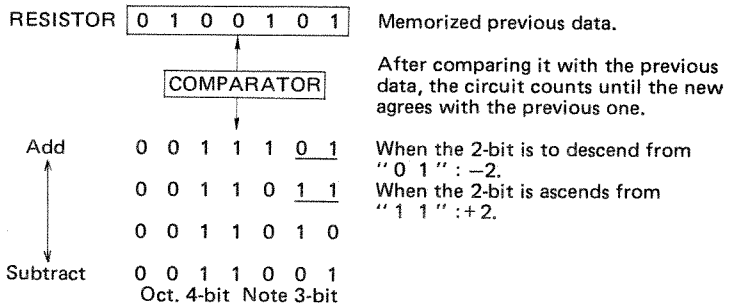
Glissand

When KB9 and KNO become conductive, it causes the GLISSAND circuit to be activated. Glissando is the effect achieved by varying the tone's semi-tone steps when moving from one pitch to the next. This pitch movement is performed by performing digital operation and processing which consists of adding or subtracting "1", or "2" to the 7-bit data that has been encoded inside the YM615 (Refer to Page 34).

The GLISSAND circuit compares the new tone with the previous one and if the two are of different pitches, it detemines whether to produce an UP or DOWN Glissando effect, depending on the relative level of the two pitches. When the voltage that is equivalent to the data is fed in from the D/A converter, the circuit counts (adds or subtracts) the 7 bit data one after another until the old data agrees with the data of the new pitch. The circuit stops counting at this point. This means that Glissando operation has been completed.

As the speed of the count, or in other words, the GLISSAND speed is set in accordance with the speed (frequency) of the clock ((PC), it is determined by the relative level of the DC voltage that is applied to the VCO for the Clock.





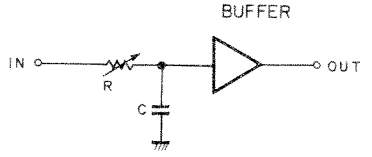
The clock frequency is determined by voltage control effected by the VCO (IC3).

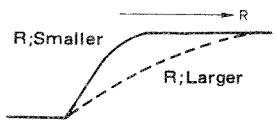
Integration

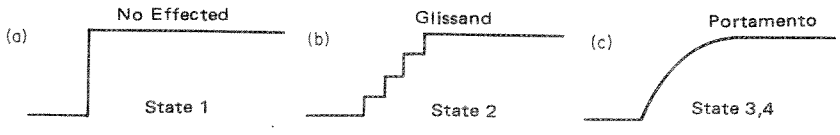
This circuit is used for producing the PORTAMENTO effect. The PORTAMENTO effect is the smooth gliding effect that is produced when moving from one pitch to another. Generally, this circuit is realized by making use of the time constant of C and R. Set the time it will take the note to change over completely to the next note to a value that suits your taste. This is acieved by making "R" variable. As a result, the time constant will change.

For this synthesizer, it may be thought that the movement is smoothened by applying the Glissand effect first to remove the corners using the time constant, For this reason, time constants are selected in stepped succession in accordance with the GLISSAND speed.

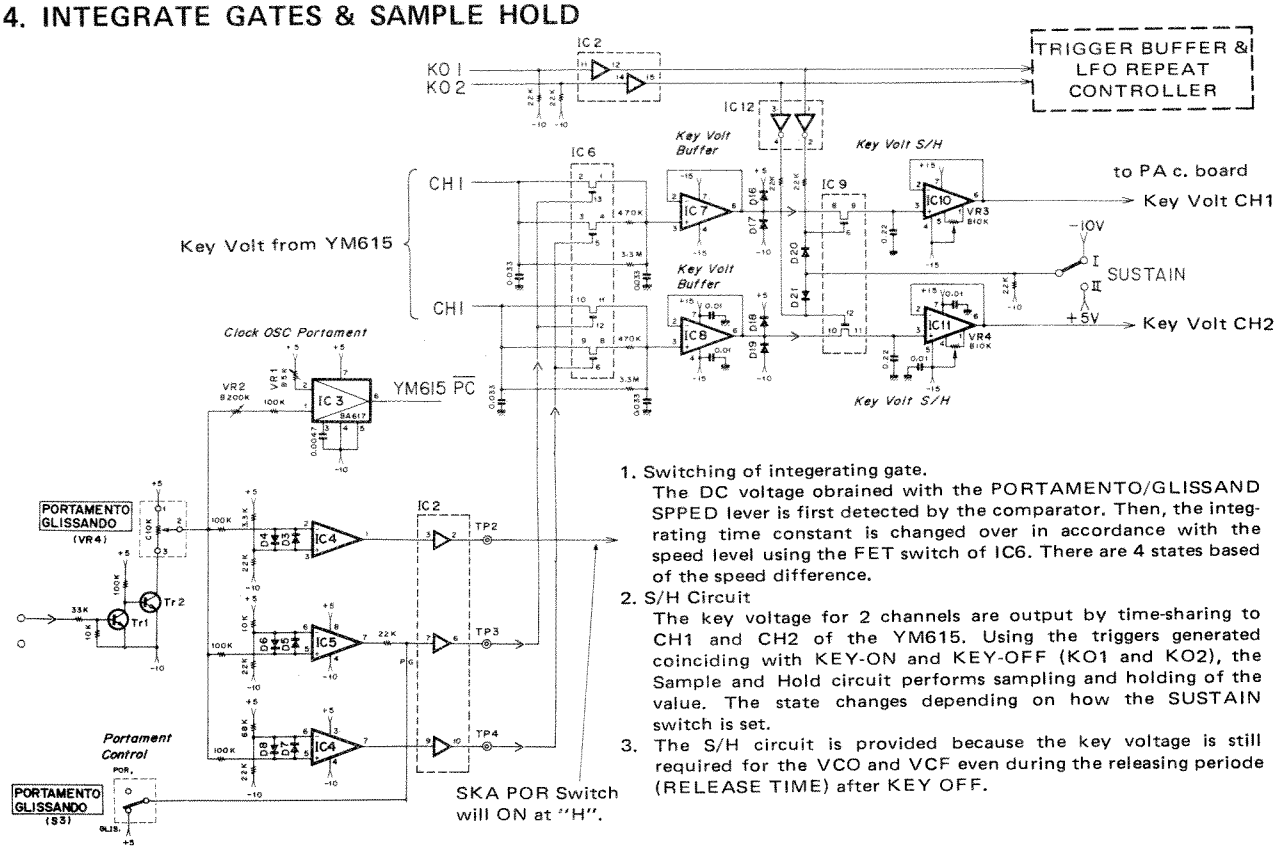
This selection is performed by first detecting the GLISSAND voltage (voltage selected with the PORTAMENTO SPEED control) with the compartor and then switching the FET gates On or Off.







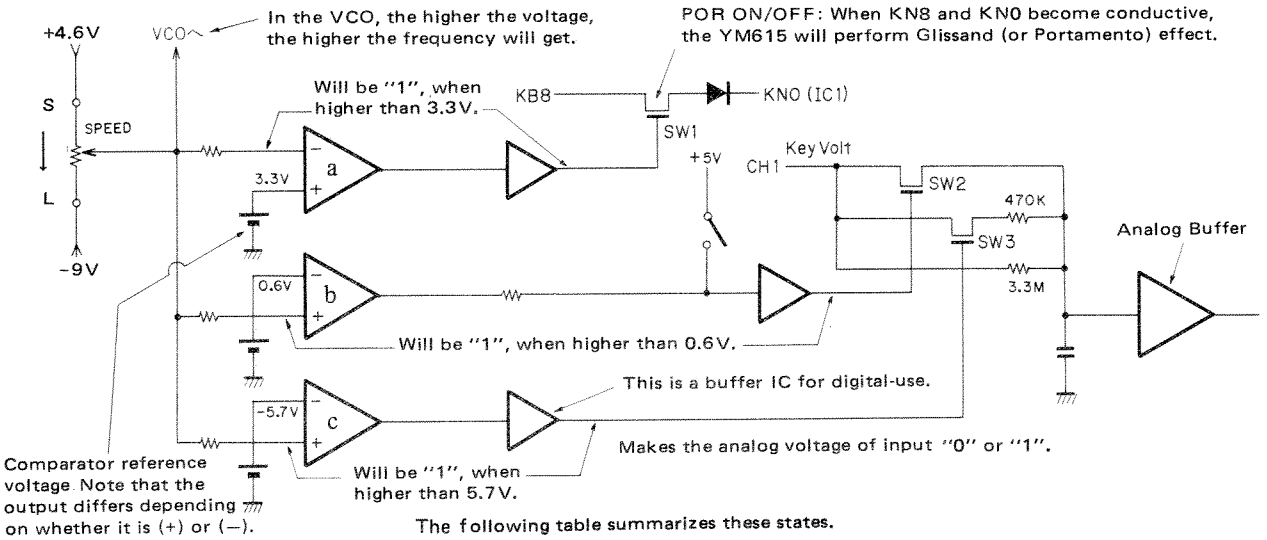
4. INTEGRATE GATES & SAMPLE HOLD



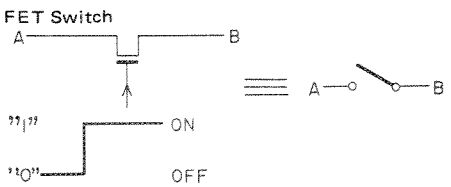
1. Switching of integerating gate.
   The DC voltage obrained with the PORTAMENTO/GLISSAND SPPED lever is first detected by the comparator. Then, the integrating time constant is changed over in accordance with the speed level using the FET switch of IC6. There are 4 states based of the speed difference.
2. S/H Circuit
   The key voltage for 2 channels are output by time-sharing to CH1 and CH2 of the YM615. Using the triggers generated coinciding with KEY-ON and KEY-OFF (KO1 and KO2), the Sample and Hold circuit performs sampling and holding of the value. The state changes depending on how the SUSTAIN switch is set.
3. The S/H circuit is provided because the key voltage is still required for the VCO and VCF even during the releasing periode (RELEASE TIME) after KEY OFF.

Comparison

The following describes the status in which ON/OFF switching of the FET gate is performed with the DC voltage (voltage obtained with the SPEED lever: +4.6V ~ –9V) that controls the VCO for the clock.



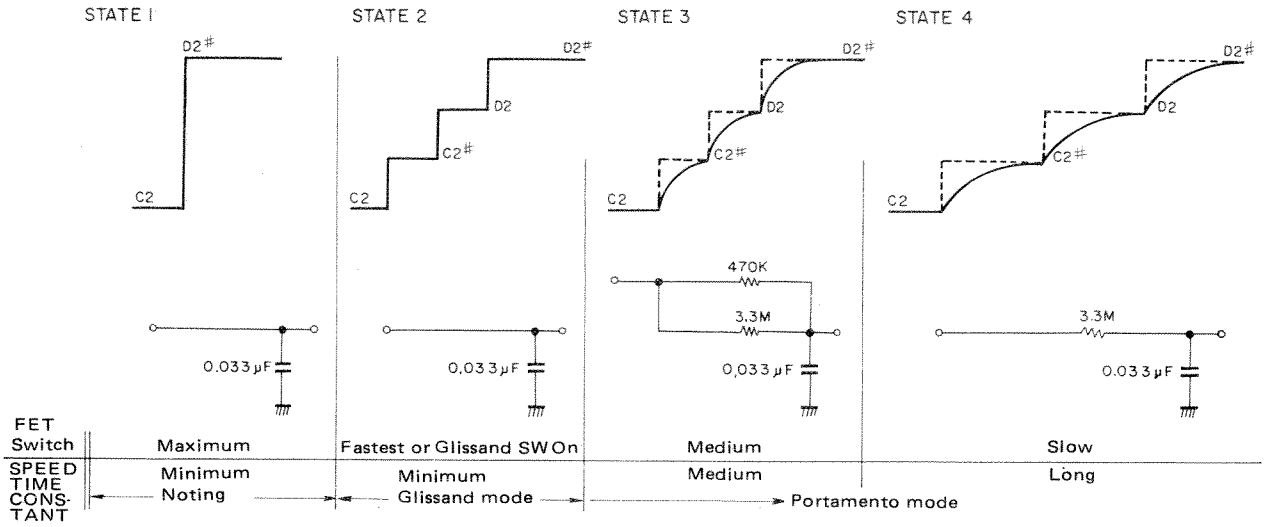
The following table summarizes these states.



Comparator \ State	State 1 4.6V ~	State 2 3.3V ~	State 3 0.6V ~	State 4 –5.7V~–9V
a SW1	0 OFF	1 ON	1 ON	1 ON
b SW2	1 ON	1 ON	0 OFF	0 OFF
c SW3	1 ON	1 ON	1 ON	0 OFF
	No Glissand(Portamento) effect.	Glissand	Fast portamento	Slow portamento

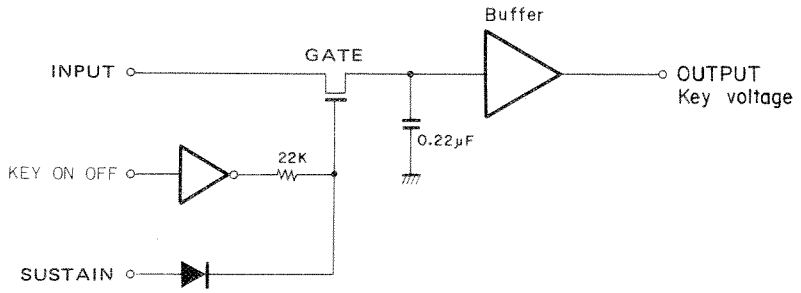
State

Depending on the difference in the integrating gate, the integrating time constant and variation will differ as shown below.



Sample & hold

Up to this point, processing that gives priority to the highest tone and processing giving priority to the lowest tone have both been carried out by time-sharing processing inside the YM615. At this stage, the two outputs are smoothened. This circuit, which is provided for CH1 and CH2, functions to hold the respective voltages by storing them inside 0.22μF capacitors.



Will ON, when FET gate voltage is "H".

Hi-impedance

The gate opens when the gate control voltage is "1", and the input key voltage is stored into the capacitor. However, when the gate control voltage becomes "0", the gate closes, causing the impedance to get high, so that the charge of the capacitor will be prevented from flowing out from the gate. Meanwhile, since the input of the buffer amplifier is also of the high impedance type, it makes it hard for the charge to flow. Consequently, charge leakage from this system will be extremely little. In this way, it is possible to hold a constant voltage for a sufficiently long duration with regard to the performing speed.

When the gate opens midway of a performance, one would think that the charge would leak out. But, actually, no serious voltage drop occurs as the previous stage integrating circuit not only has a time constant of 3.3M x 0.033μ but also has a buffer amplifier that incorporates a high-impedance type input circuit.

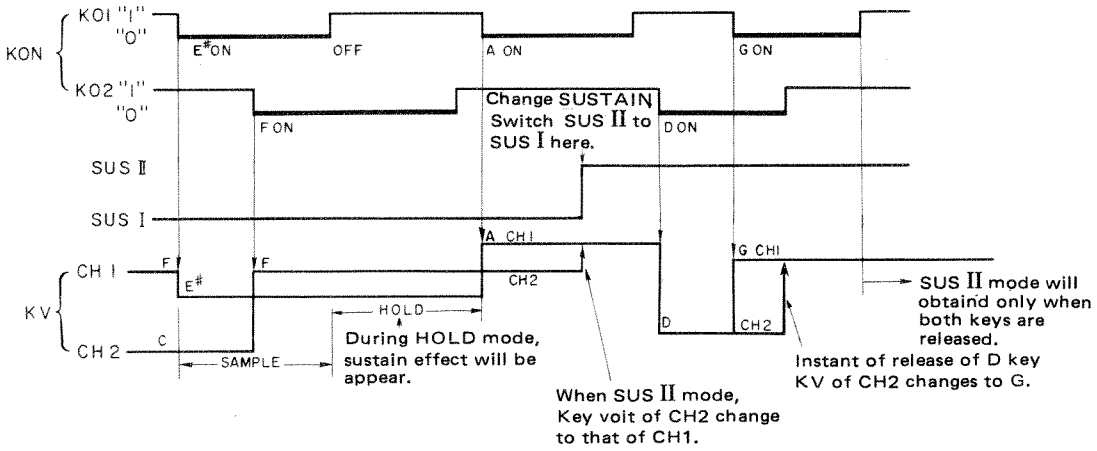
■ **SUSTAIN – Selection between I/II**

(a) During SUS I

Since the gate opens only during Key-On, the sustain effect will be obtained for the pitches of the respective notes.

(b) During SUS II

As the gate will be always open regardless of whether there is a Key-On signal or not, the key voltage that has been charged into the capacitor of the S/H circuit will change to the key voltage of the next key that has been depressed. As a result, the attenuating sound of the former note will be changed into a new sound. (When the keys are depressed one at a time.) Sustain effect will obtained only when all keys are released.

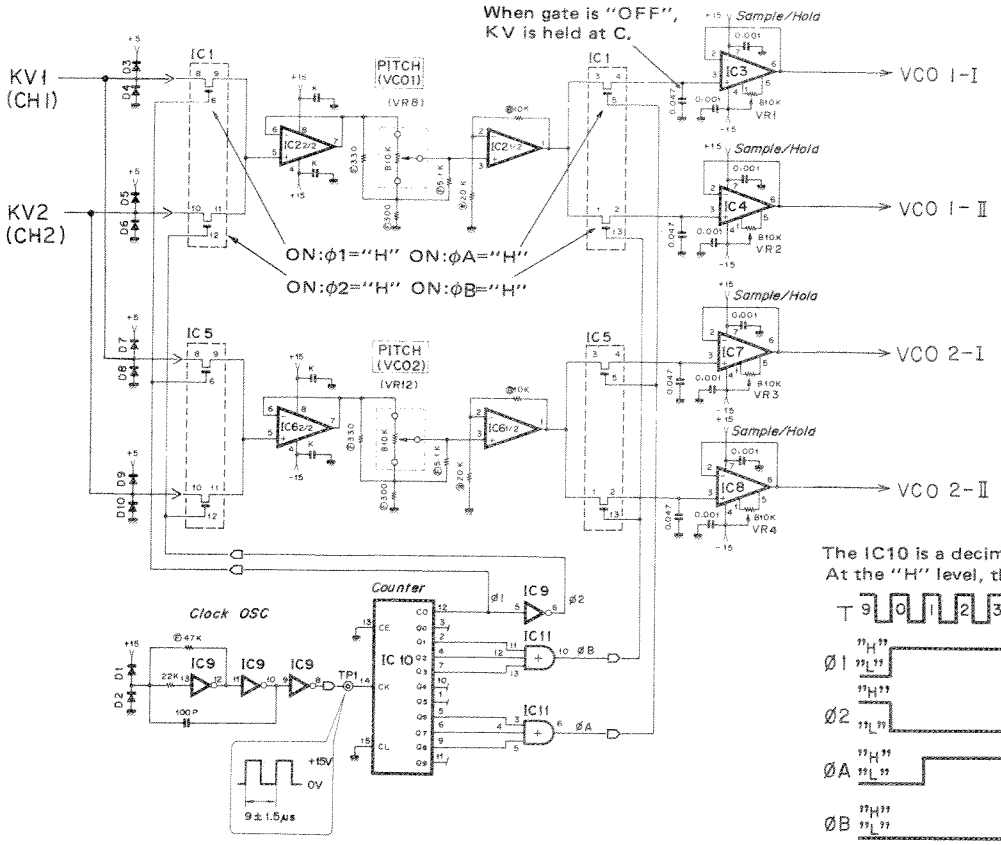


KEY VOLTAGE DISTRIBUTOR: PA BOARD

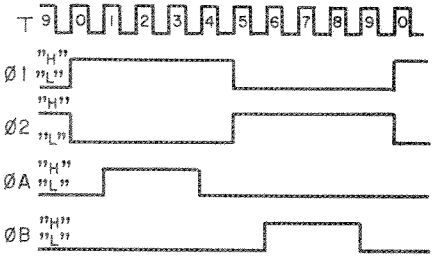
In addition to assigning the key voltage outputs CH1 and CH2 of two systems to VCOs of 4 systems, the PA unit controls the pitch.

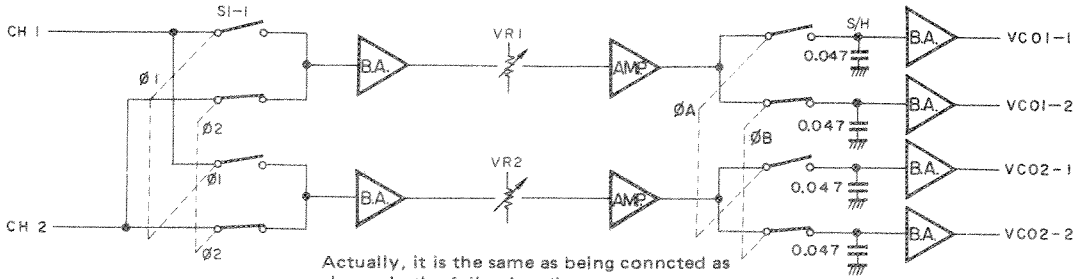
Switching

The PA unit actually functions to perform switching at high speed. And since the key voltage is held by the 0.047μF even when the switch is "OFF", the functions are exactly the same as those gained when the KV of CH1 is connected to VCO1-I and VCO2-I, and the KV of CH2 to VCO1-II and VCO2-II.



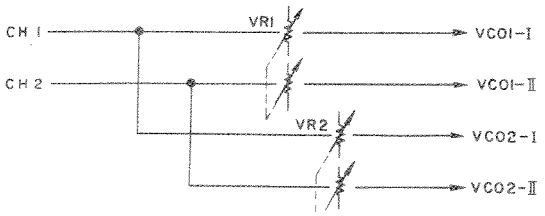
The IC10 is a decimal system counter.
At the "H" level, the gate will be switched on.





Actually, it is the same as being connected as shown in the following diagram.

Has the function of holding the KV during switch off.



However, since the VR can be used in common, it has the advantage of being free of errors that are caused because of the irregularity in the VRs.

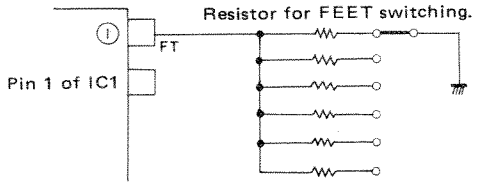
VOLTAGE CONTROLLED OSCILLATOR: VCO BOARD

In terms of basic operation, the VCO is exactly the same as that of a conventional synthesizer. First, the FET switch and analog switch that serves to changeover the FEET switch electrically shall be explained.

1. FEET SELECTOR CIRCUIT

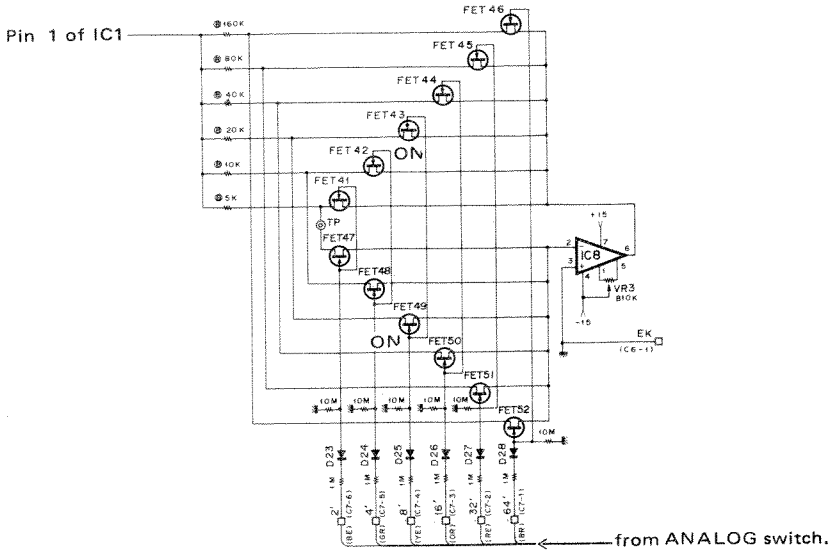
RFT

As shown in the figure, this section functions to change over the FEET resistor which is connected to Pin 1 of IC1.



FET switch

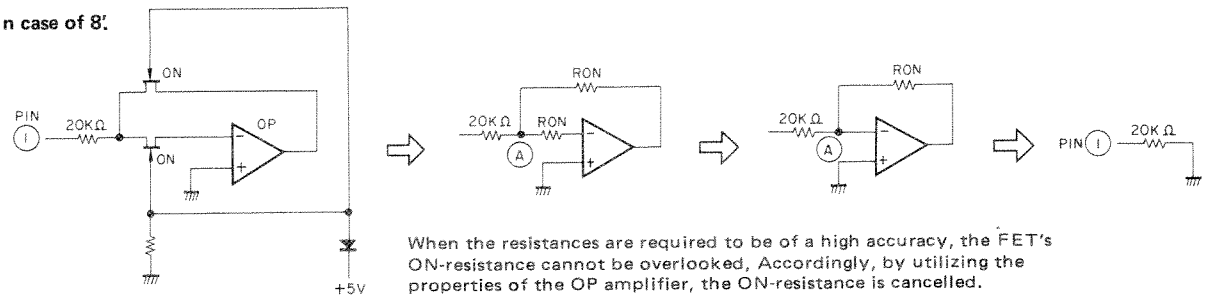
The following drawing shows how this is performed electrically.
This FET switch operates so that it will be "ON" when the control input terminal is +5V, and will be "OFF" when the terminal is −10V. Here the 8' control terminal alone will be +5V: the others will be −10V.



Ron resistance

To make it easier to understand, the following drawing shows elements that are in the 'ON" condition. In this circuit, one end (FET-side) of the 20kΩ is of a potential equivalent to that of the earth.
When the resistances are required to be of a high accuracy, the FEET's ON-resistance cannot be overlooked. Accordingly, by utilizing the properties of the OP amplifiers, the ON-resistance is cancelled.

In case of 8'



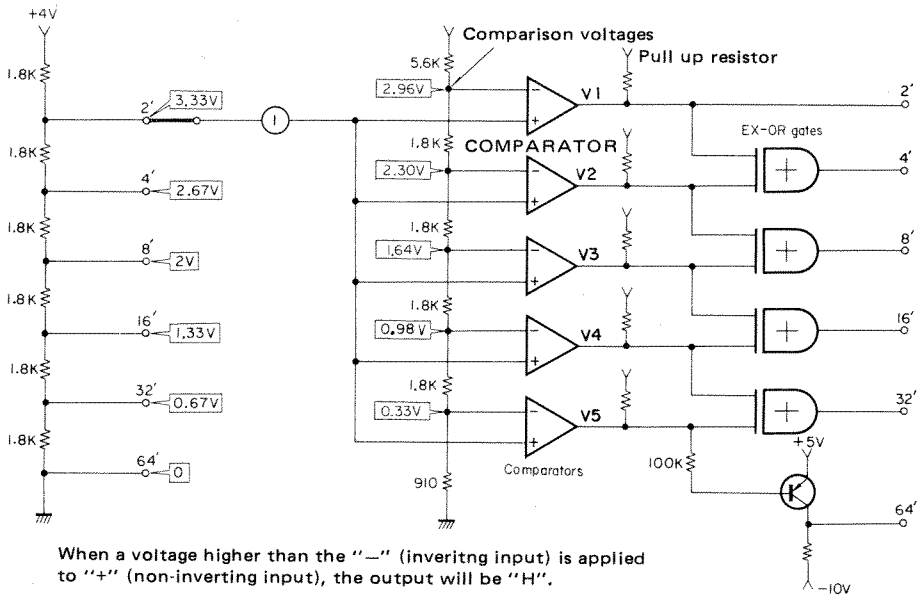
When the resistances are required to be of a high accuracy, the FET's ON-resistance cannot be overlooked, Accordingly, by utilizing the properties of the OP amplifier, the ON-resistance is cancelled.

That is, the resistance component of the input terminal of the feedback loop, when the OP amplifier forms one, will be overlooked, and Point A will be of a potential equivalent to that of the earth. When this phenomenon is viewed from the side of 20kΩ, it means nothing other than that the potential has dropped to that of the earth. In other words, changeover with this FET switch will be equivalent to changing over with a mechanical switch.

Now, we shall explain the LOGIC section which controls the FET switch. The IF 1/4 c. board performs this control function. This circuit is identical to the circuit used for such c. boards as the MOD c. board.

2. ANALOG SWITCH LOGIC SECTION

This circuit is composed of a DC comparator, EX-OR gate and transistors. The control voltage is applied from the demultiplexer. When we exclude D/A and A/D conversion, the circuit may be expressed in an equivalent manner as illustrated below.

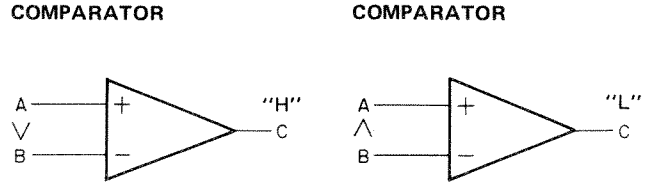


When a voltage higher than the "—" (inveritng input) is applied to "+" (non-inverting input), the output will be "H".

Comparator

Together with the changeover of FEET (or data of memory), a DC voltage as shown in the drawing will be impressed on "+" (non-inverting input) of the comparator.

When an input voltage as that shown below is applied to the DC comparator, a positive, or negative, potential will appear in acordance with the potential difference.



If A > B, then C will be "H" (positive). If A < B, then C will be "L" (negative).

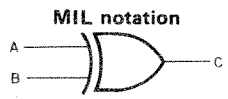
Comparator output

That is, when a potential higher than the comparing potention (shown in the drawing) is applied to "—" (inverting input) of the comparator, the output will be of the H-level. The following drawing summarizes this status.

Comparator output (V) / V^+_{in}	V1 (2.96)	V2 (2.30)	V3 (1.64)	V4 (0.98)	V5 (0.33)
3.33V	H	H	H	H	H
2.67V	L	H	H	H	H
2.00V	L	L	H	H	H
1.33V	L	L	L	H	H
0.67V	L	L	L	L	H
0.00V	L	L	L	L	L

EX-OR

When several comparators have become "H", and when the required data alone are to be made "H", the EX-OR (exclusive OR: Exclusive logical sum) gate functions to achieve this. As for the truth table of EX-OR, it is "H" when the two input conditions are incoherent, and is "L" for other cases.



A	B	C
L	L	L
L	H	H
H	L	H
H	H	L

8' was selected

Let us, therefore, consider a case in which 2V (8') is applied to the analog switch as the control input. The outputs of the comparator will be "H", up to the third one from the first one, so that the following levels will be applied to EX-OR.

That is, the output of IC3 alone will change to the H-level, causing the 8' FEET switch to turn on, and 20kΩ to be grounded.

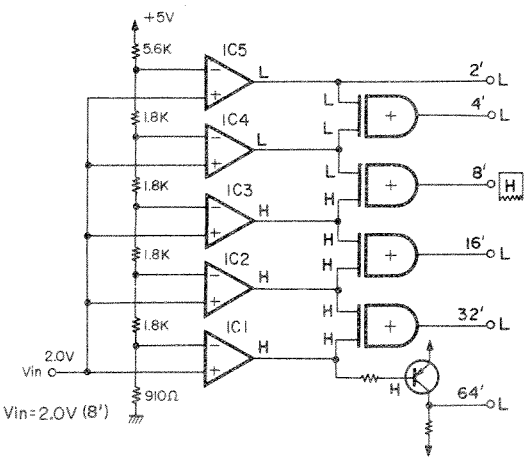
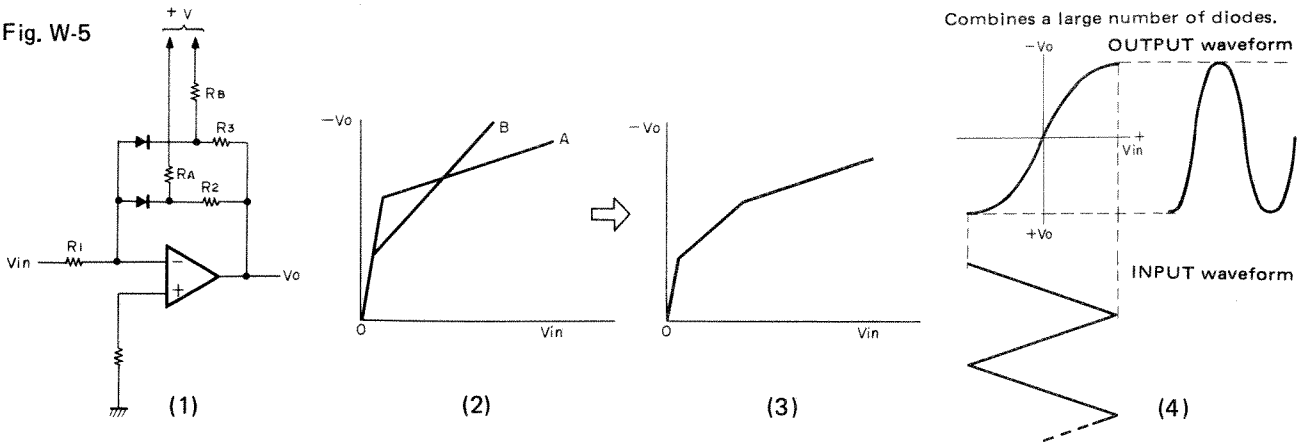


Fig.W-5 (1) forms into a single circuit these two circuits having different characteristics. The output characteristics gained as a result of this combination has bends at two points as can be seen in Fig. W-5 (3). The basic operation, naturally, is the same as that shown in Fug. W-4. Fig W-5 (4) shows the result of combining a large number of such circuits, by matching the plus and minus polarities. It may seem sonewhat complex, but it is just a combination of such circuits as shown in Fig W-4.

Fig. W-5



Sawtooth Wave/Square Wave Conversion

Fig. W-6 shows the circuit structure. To convert sawtooth waves into square waves, the comparetor is employed. Fig. W-7 shows the principal diagram. As will be seen from this diagram, when the voltage fed into A becomes larger than that fed into B, the output will be "H", whereas, when it becomes smaller, the output will be "L". When the voltage fed into B is varied, H to L ratio (called the duty cycle) of the output waveform will vary as illustrated, changing the waveform as a result. The output, if unmodified, will be too large for the comparator. It is, therefore, adjusted to an adequate level by letting it pass through the clamper circuit. In this way, sawtooth waves are converted into square waves.

Fig. W-6

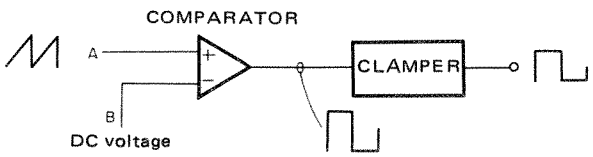
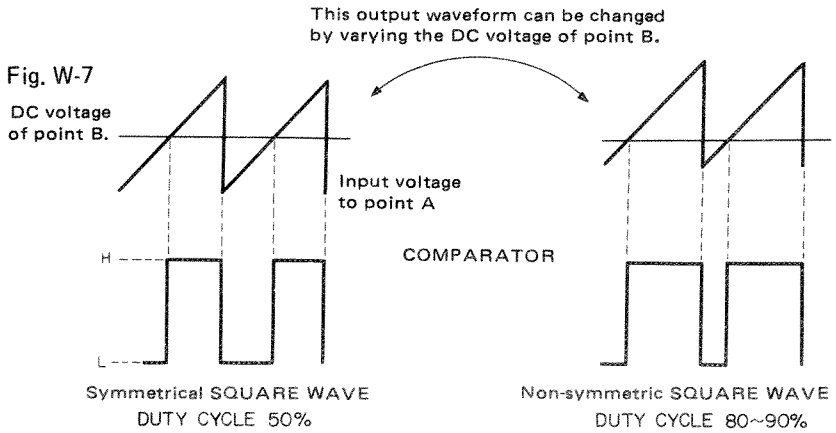
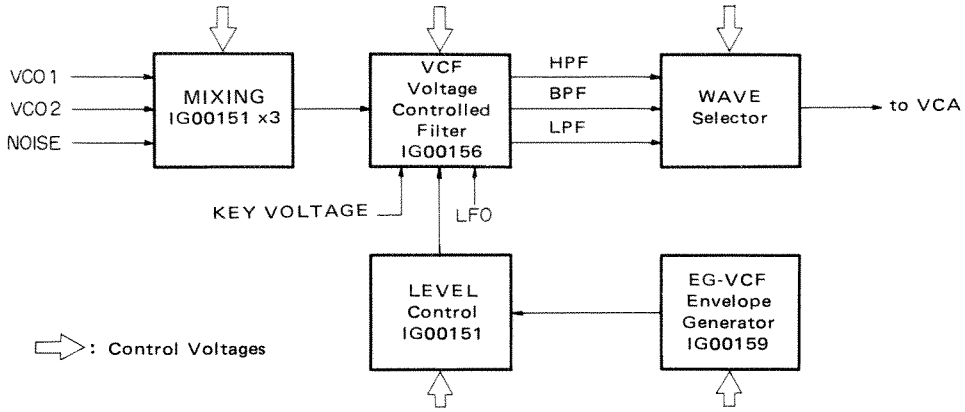


Fig. W-7



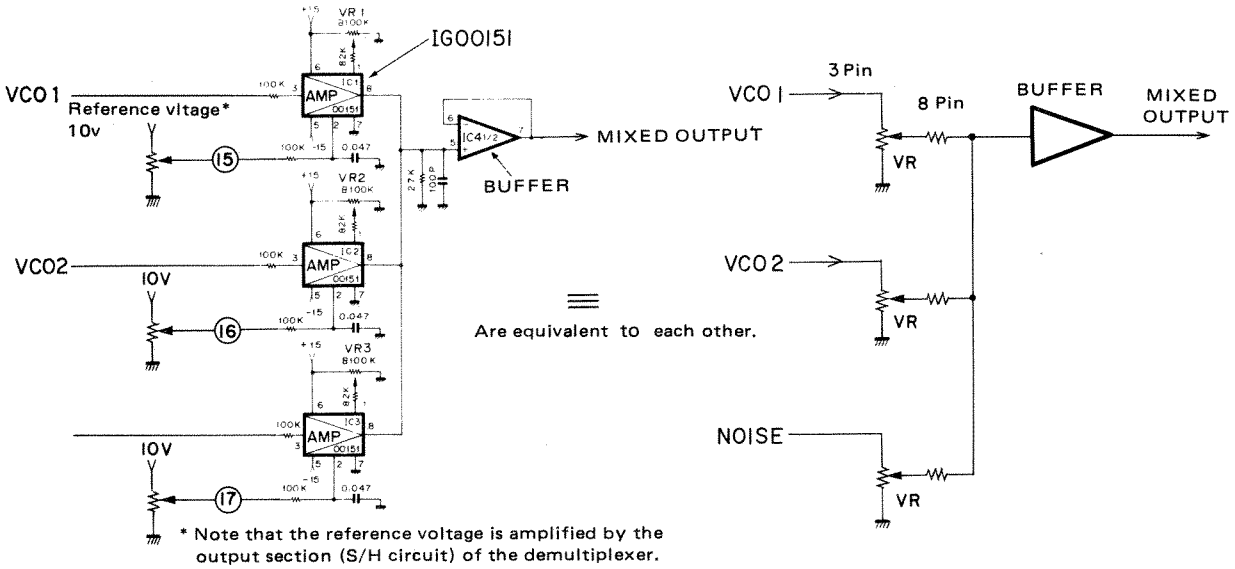
VOLTAGE CONTROLLED FILTER: FA BOARD

As shown in the following figure, the VCF section is composed of such components as the input mixing section, VCF section, EG section and envelope generator section.



1. MIXING BLOCK

First, let us take a look at the electronic controls based on the use of the IG00151 which is employed as a mixer. The operations of the envelope generator will be discussed in the section dealing with the VCA block.



The IG00151 functions as a special OP amplifier that controls the mutual conductance Gm by using the voltage (in fact, the current that is proportional to the voltage) that is applied to its control input terminal (Pin ②). The higher the voltage gets, the higher the Gm will be (resistance will decrease). Conversely, the lower the voltage gets, the smaller the Gm will become (resistance will decrease). For this reason, the IG00151 functions as a voltage controlled function which uses Pin 3 as its INPUT terminal and Pin 8 as its OUTPUT. (It may also be referred to as a VCA (voltage controlled amplifier) used for changing the amplification degree.) Therefore, this circuit is exactly equivalent to the circuit shown on the right side of the above drawing.

2. VCF BLOCK (PERIPHERY OF IG00156)

The VCF block is composed of the IG00156 (an IC exclusively used for this block) and its peripheral circuits. The input is fed into Pin ①, the cut-off frequency control voltage into Pin ④ and the key voltage into Pin ②

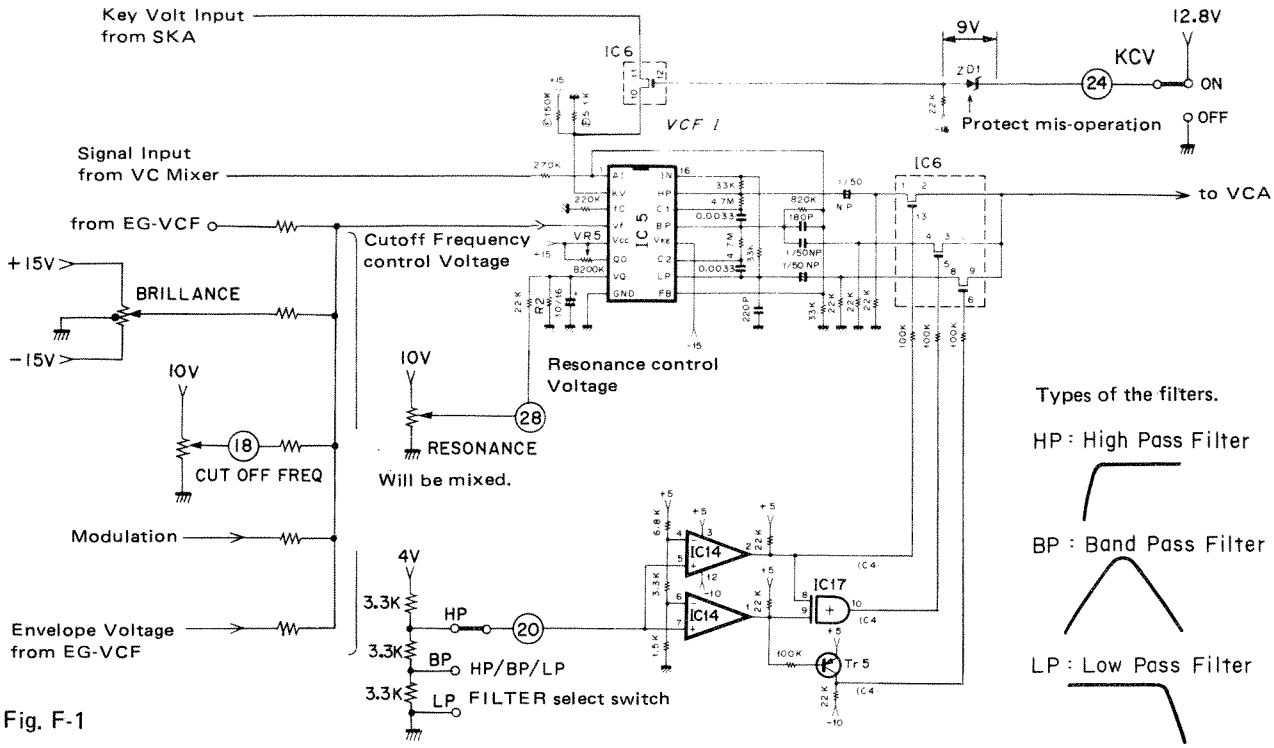
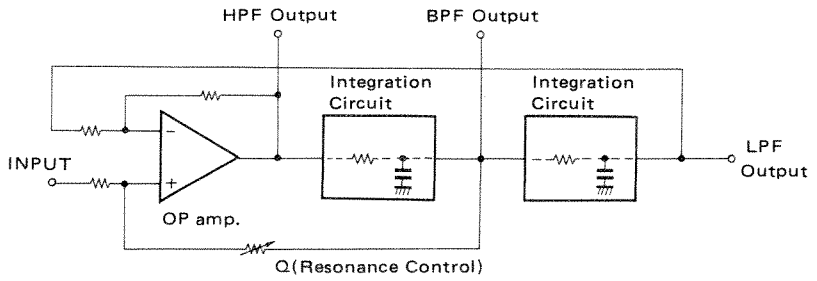


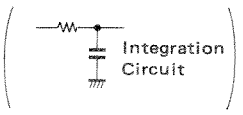
Fig. F-1

■ Operating Principles of IG00156

This circuit is composed of state-variable filters in the manner shown in Fig. F-2. Two stages of integrating circuits are connected in series, and at a point midway between these two circuits, feedback is applied by way of an OP amplifier. By this arrangement, the circuit composition becomes equivalent to that by which the transfer functions of a filter is indicated. As a result, the respective filters, i.e., the high-pass, band-pass and low-pass filters are obtained.

(As the principle underlying the transfer function and filter is extremgly complicated and difficult, please read specialized books for reference if you should wish to know more.)





The filter characteristics shall be 12dB/oct.

Fig. F-2

Using OP amp as C

To ensure accurate operation of the circuit, a circuit as shown in Fig. F-3 is composed by employing an integrating circuit. The cut-off frequency of the filter is determined by R and C with which the integrating circuit is formed. In other words, by changing R to a variable resistor as shown in Fig. F-3, it is possible to change the cut-off frequencies of the filter freely. Further, by changing R', it is possible to control resonance (Q) also in a free manner.

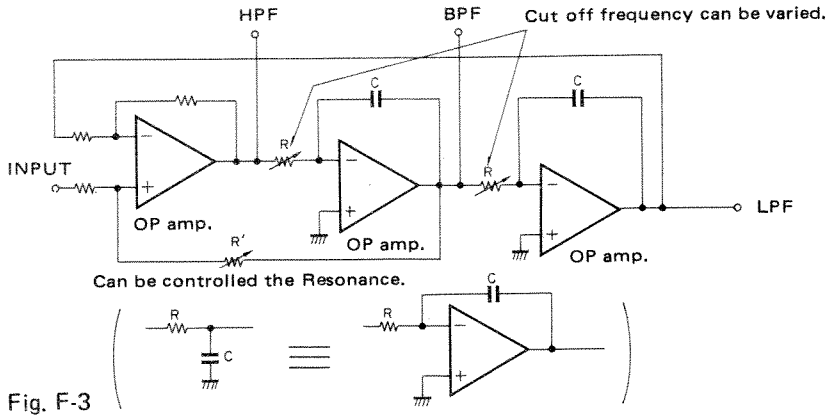


Fig. F-3

Using IG00151 as VR

The cut-off frequencies of this filter can be obtained from the following formula.

$$fc = \frac{1}{2\pi CR}$$

Now, by replacing this variable resistor by the Gm converting circuit (IG00151), it is possible to control the cut-off frequency and resonance with the voltage. In other words, this will form a VCF. Fig. F-4 shows the VCF formed in this manner. Since the voltage will be converted in various manners, the cut-off frequency is given finally by the following formula.

$$fc = 125 \cdot Kv \cdot 2^{Vfc}$$

where, Kv : Key voltage

Vfc : Cut off frequency control voltage

As regards the filter characteristics, the output both for the high-pass and low-pass filters will be 12dB/OCT as the integrating circuit is composed of 2 stages.

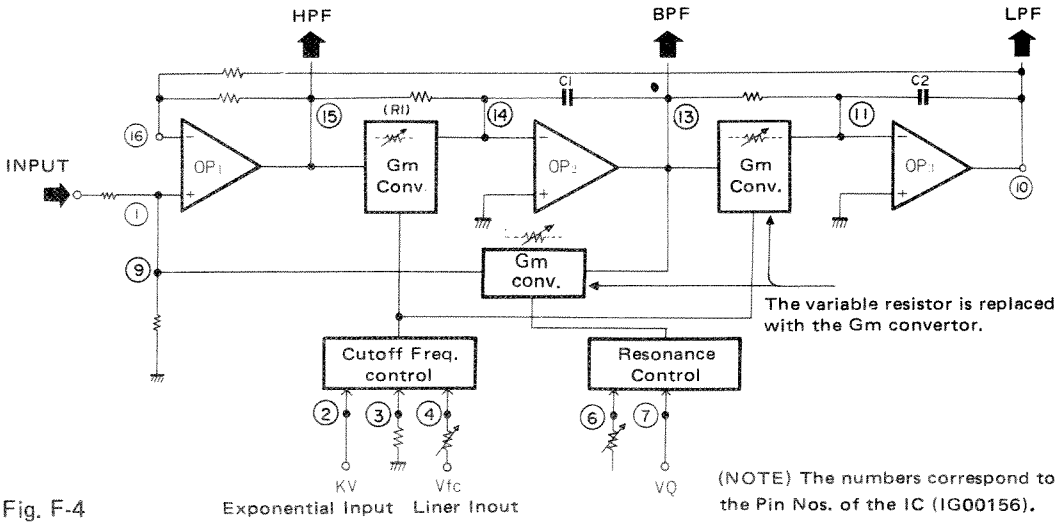
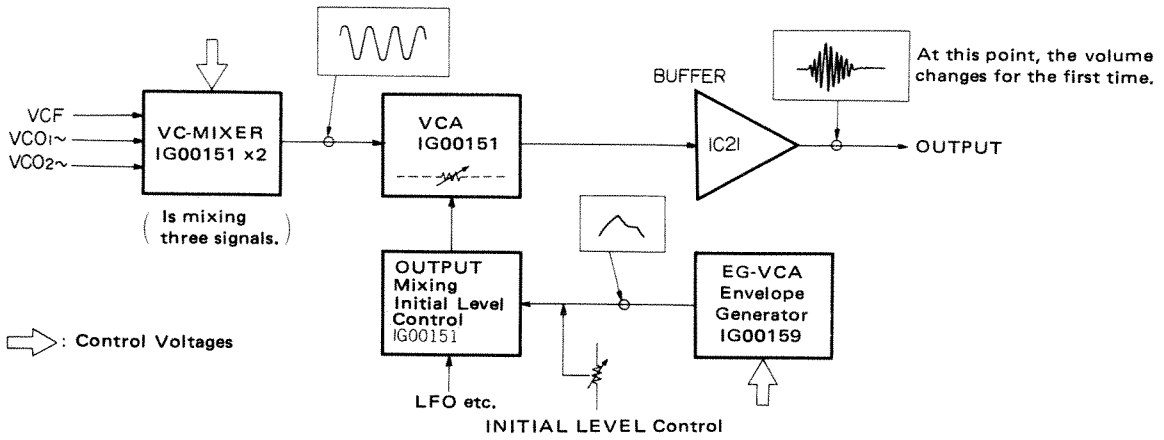


Fig. F-4

(NOTE) The numbers correspond to the Pin Nos. of the IC (IG00156).

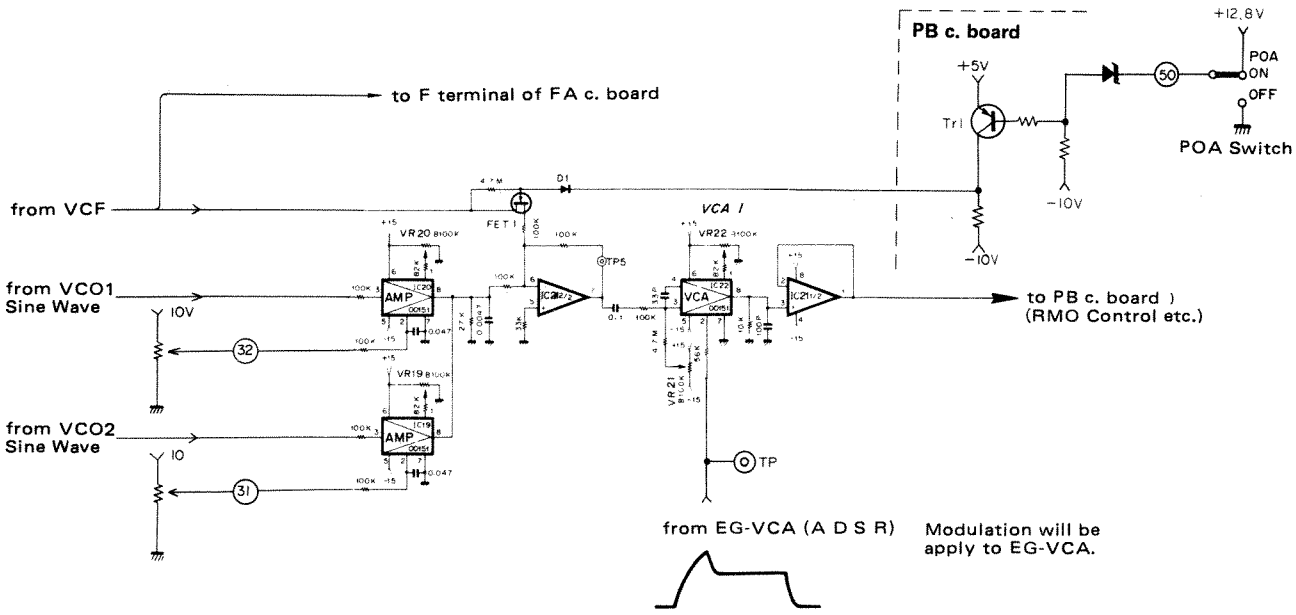
VOLTAGE CONTROLLED AMPLIFIER: FA BOARD

The circuit compostion of the VCA section consits of the mixing section, VCA, and envelope generator.



Circuitry

Sine waves are fed in from the VCO blocks, and signal from VCF is applied to VCA block when POA switch is set to OFF position.

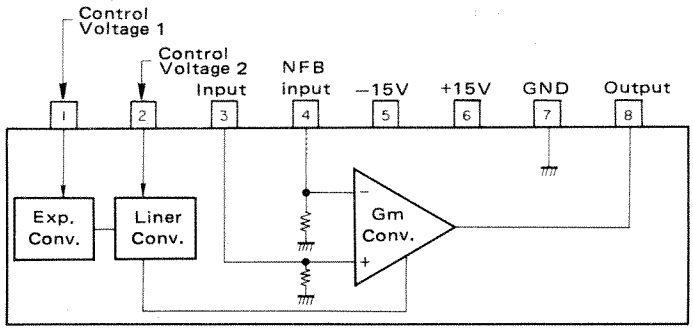


1. MIXING BLOCK

Basically, the functions are the same as those of the mixer of the VCF.
In this case, sine-wave outputs, VC01 and VC02, are fed into the two IG00151s and are mixed by IC21. Further, instead of being passed through the IG00151, the output signals of the VCF are passed through the FET switch, after which, they are mixed by the IC21. This FET switch will be ON when the gate is OV and will be OFF when it is −10V. This FET switch is provided for the purpose of preventing the signals of the VCF from entering into the VCA, when the switch of the POA (Pass Over VCA) is turned on.

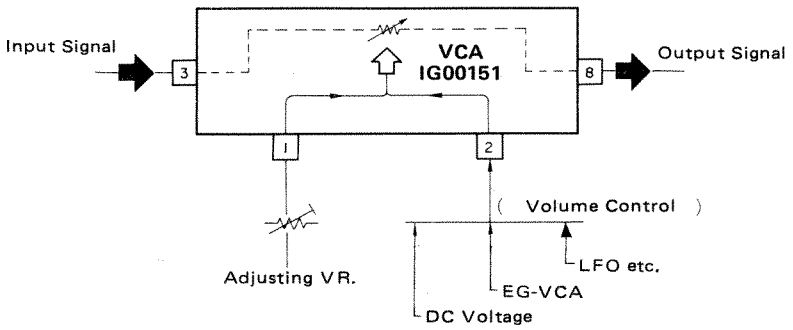
2. VCA BLOCK (PERIPHERY OF IG00151)

As this has been described in details in the section in which the VCF has been discussed. The following shows the inner block diagram of the IG00151.

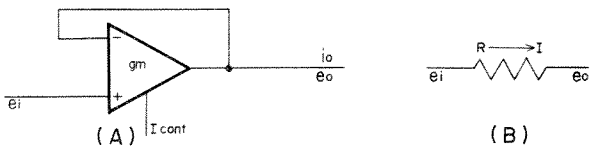


0v ⩽ Vcont ⩽ 10v

The IC (IG00151) is so controlled by the semifixed variable resistor so that the output will be "0" when the voltage applied to Pin 2 is "OV", and will be of the same level (that is, of the same volume) as that of the input voltage, when the voltage applied to Pin 2 is 10V.



Conversion of Gm (1/R) is performed inside for the IC, by using the current Icont which is proportional to the control voltage.



The Gm of this IC is variable by the use of Icont.

Therefore, $Gm = K \cdot I_{CONT}$ (K : Constant)

Its characteristics as shown in Fig. A are: $Io = K \cdot I_{CONT}(ei - eo)$

and in Fig. B are: $I = \frac{1}{R}(ei - eo)$

Here, Gm can be obtained in an equivalent manner as $Gm \equiv 1/R$

By comparing Fig. A with Fig. B, we get $\therefore R \equiv \frac{1}{Gm} = \frac{1}{K \cdot I_{CONT}}$

It follows, therefore, that the larger the control voltage, the smaller the resistance will get, and the level-down of the input signals will become less as a result.

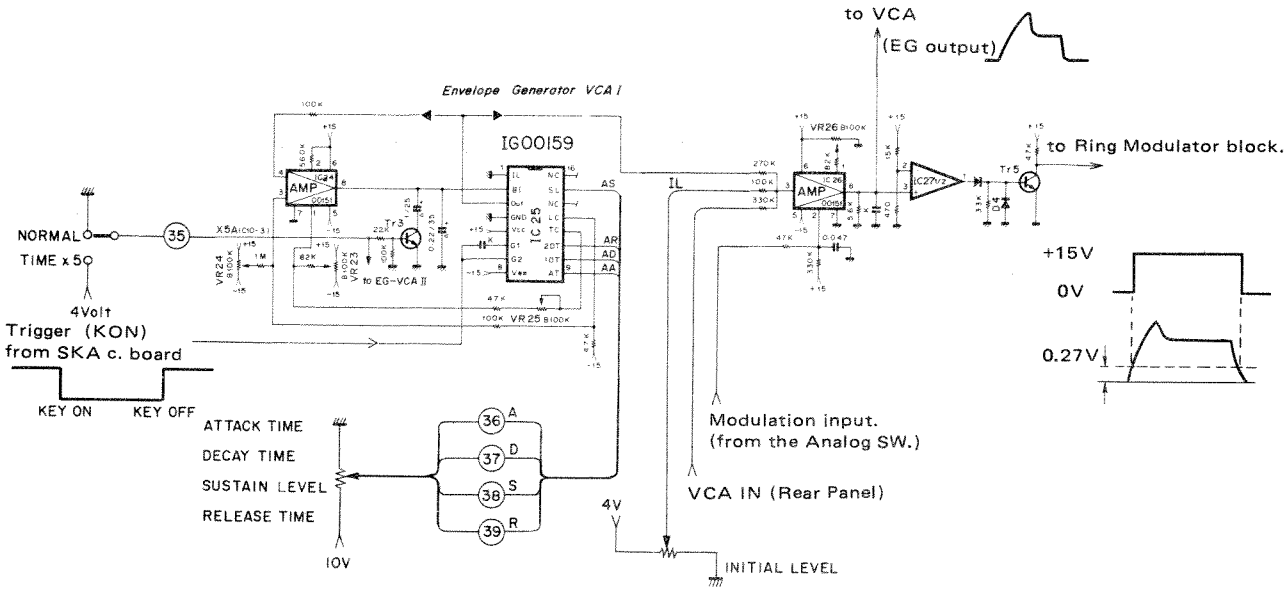
ENVELOPE GENERATOR: FA, PA BOARDS

This is a DC voltage time function generator. This circuit, which starts operating upon receiving a Key-On signal, generates an envelope voltage corresponding to the time the note starts up to the time it fades away. Largely divided, this envelope generator can be grouped into three types, those for VCO, those for VCF and those for VCA. (The EG for VCO is only provided for the CS-40M.)

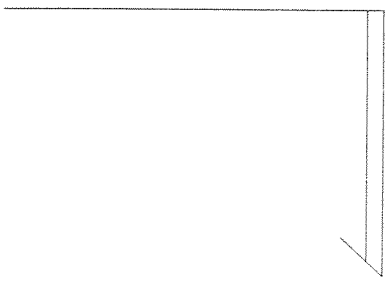
VCO-EG is used as the oscillating frequency control voltage of the VCO.
VCF-EG is used as the cut-off frequency control voltage of the VCF.
VCA-EG is used as the volume control voltage of the VCA.

1. EG-VCA CIRCUIT

EG-VCA, EG-VCF and EG-VCO are practically the same in terms of circuit composition.
First, the EG-VCA will be explained, and then we shall go into discussing the difference between the EG-VCA and EG-VCF. The major section of the EG consists of the IG00159 and its periphery.



■ **Operating Principles of the IG00159**



The hardware of the envelope generator (referred to as EG hereafter) is basically composed as shown in Fig. A. The circuit that forms the basis of the EG is an integrating circuit such as shown in Fig.B.
This integrating circuit makes use of the fact that such output characteristics as those shown in the figure are gained when a DC current is applied as the input. This, in other words, means that the time it takes for the output voltage to reach the same level as the input voltage is determined by the product of R and C. This further means that an EG can be obtained by combining the integrating circuits with switches in a clever manner.

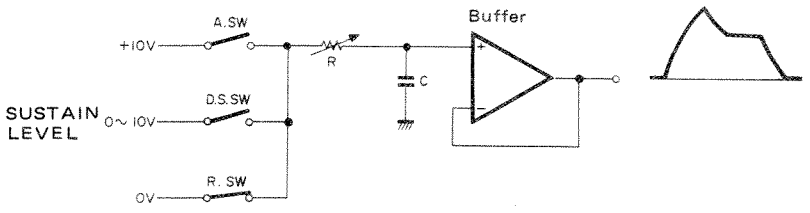


Fig. A

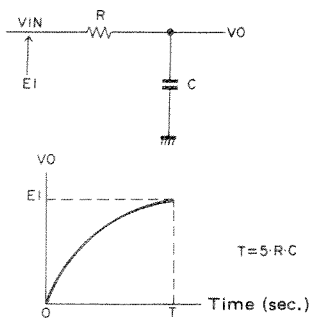
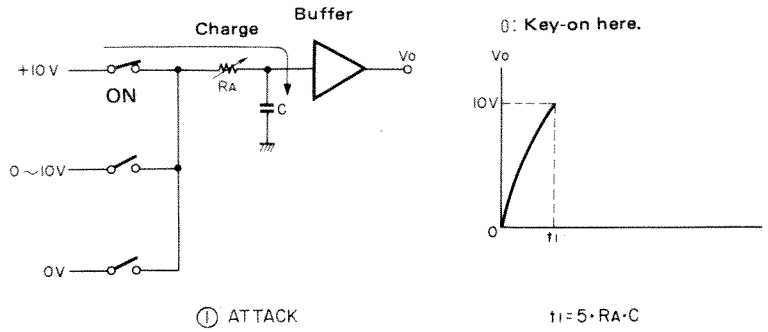


Fig. B

① Attack time

Upon Key-On, the A.SW will close, causing +10V to be applied to the integrating circuit. The output voltage will gradually rise from OV to 10V.

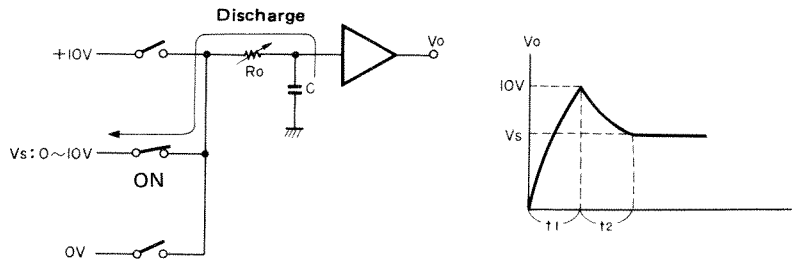


① ATTACK

$t_1 = 5 \cdot R_A \cdot C$

② Decay time
③ Sustain level

When the output voltage reaches 10V, the A. SW will open, causing the D and S SWs to close. This, in turn, will cause the output voltage to drop to a predetermined voltage (SUSTAIN level: 0 ~ 10V).
During Key-On, the voltage will be sustained at the predetermined level.

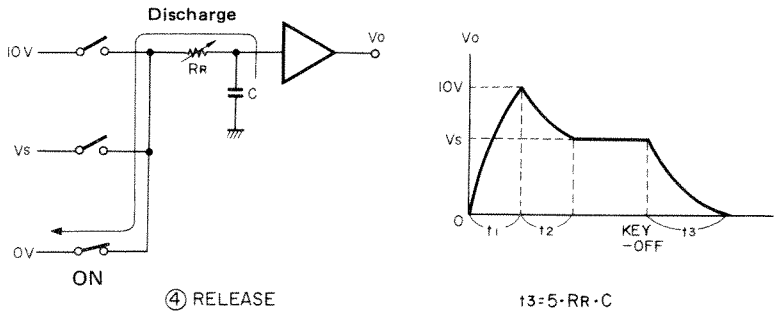


②③ DECAY, SUSTAIN

$t_2 = 5 \cdot R_O \cdot C$

④ Release time

Upon Key-Off, the R. SW alone will close, and the output voltage will stop dropping toward 0V.
By passing through this process, the EG voltage is formed.

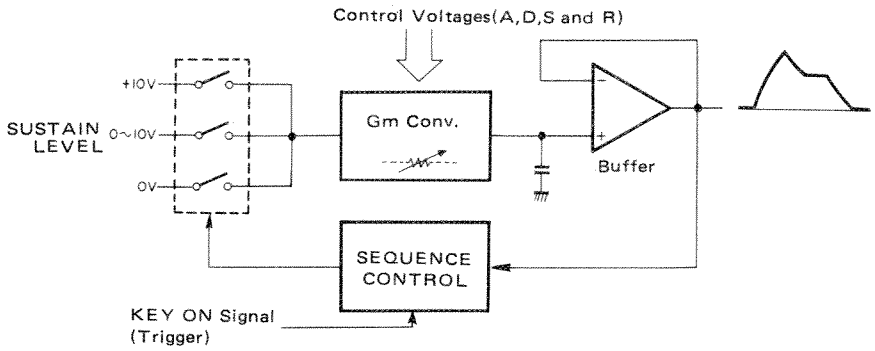


④ RELEASE

$t_3 = 5 \cdot R_R \cdot C$

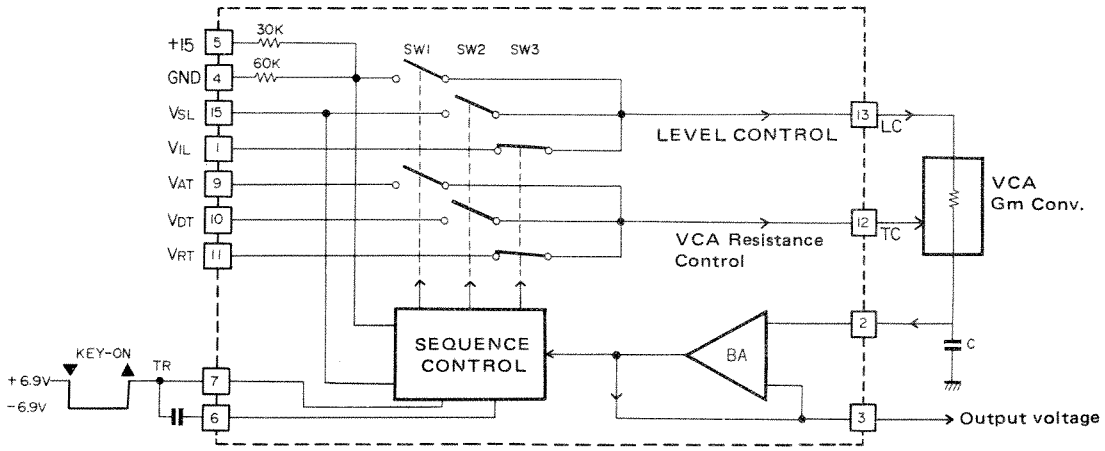
Using Gm comvertor

Now, by replacing the variable resistor R with the Gm converting circuit and the switch with the analog switch, and by adding a sequence control circuit that functions to effect automatic control of the condition of the various switches, it is possible to control each parameter with voltages. Furthermore, the EG can be activated any time when Key-On signals are applied.



Brock diagram

The integrated circuit (IC) with which the composition shown in the Figure above has been realized is the IG00159. The composition of the IC is given in concrete details in the Figure below. Although it is rather complex, the basic operations remain the same as those in the past. Compare this carefully to understand the operation fully.



Time expand

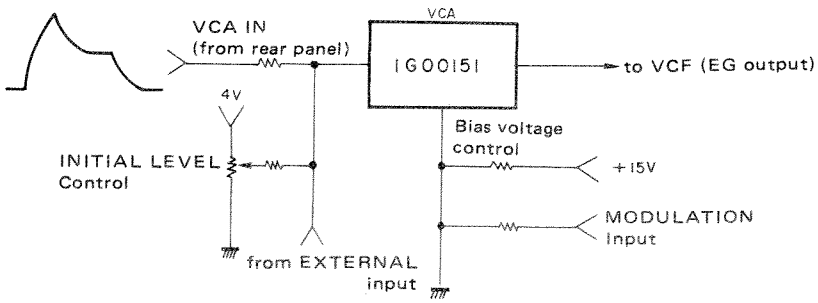
Tr3 and its periphery circuit turns on and grounds the 1μF capacitor when the TIME x 5/NORMAL switch is changed over to "x5". As a result, the 1μF capacitor and the 0.022μF capacitor will be arranged in parallel and the time constant will increase by 5-folds.

Initial level

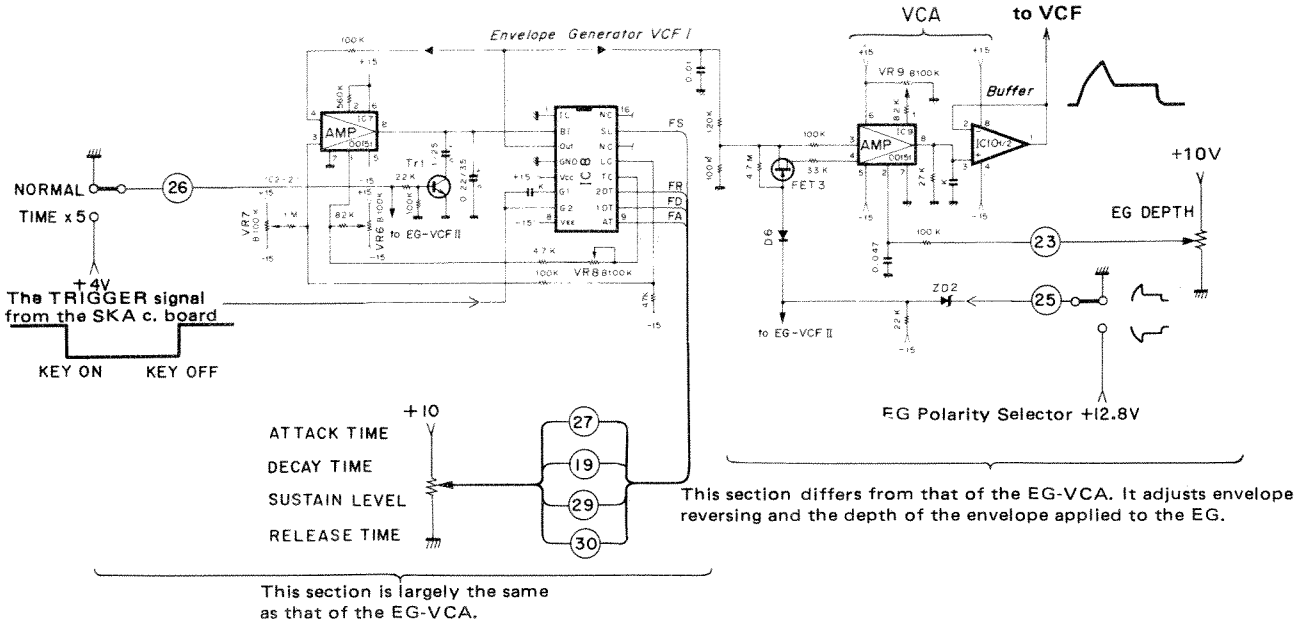
This is a circuit that functions to control the VCA output level when the keys are not being depressed. The EG voltage and DC voltage are mixed at the input section of the IG00151.
This circuit is provided only for the EG-VCA and not for the EG-VCF. This section is not programmed.

Modulation

For the EG-VCA, modulation is performed at the EG block. However, for the VCF, modulation is performed at the VCF block, since it is necessary to apply modulation even when the EG-VCF level is zero.



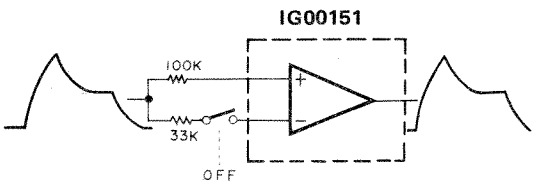
2. EG-VCF CIRCUIT



Switching polarity

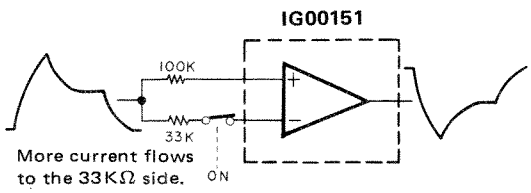
The EG-VCF circuit also employs the IG00159 and are the same as those of the EG-VCA in terms of basic operation. However, it differs in one point. While the EG-VCA uses the IG00151 as a mixer, the EG-VCF uses it to reverse polarities and to control the EG depth.
The polarity reversing circuit operates as illustrated below.
The FET switch turns on when a + voltage is applied to the gate.

Non-inverting amplifier



IG00151 is of the positive polarity.

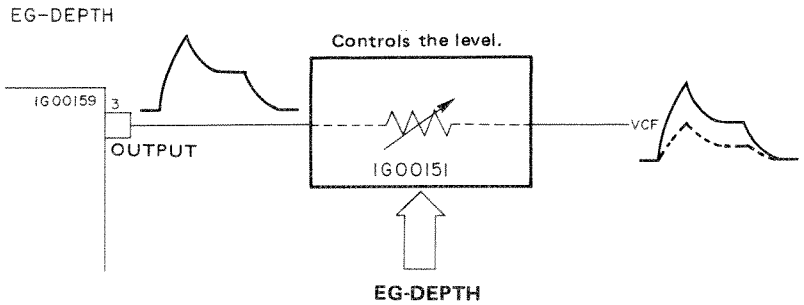
Inverting amplifier



IG00151 is of the negative polarity.

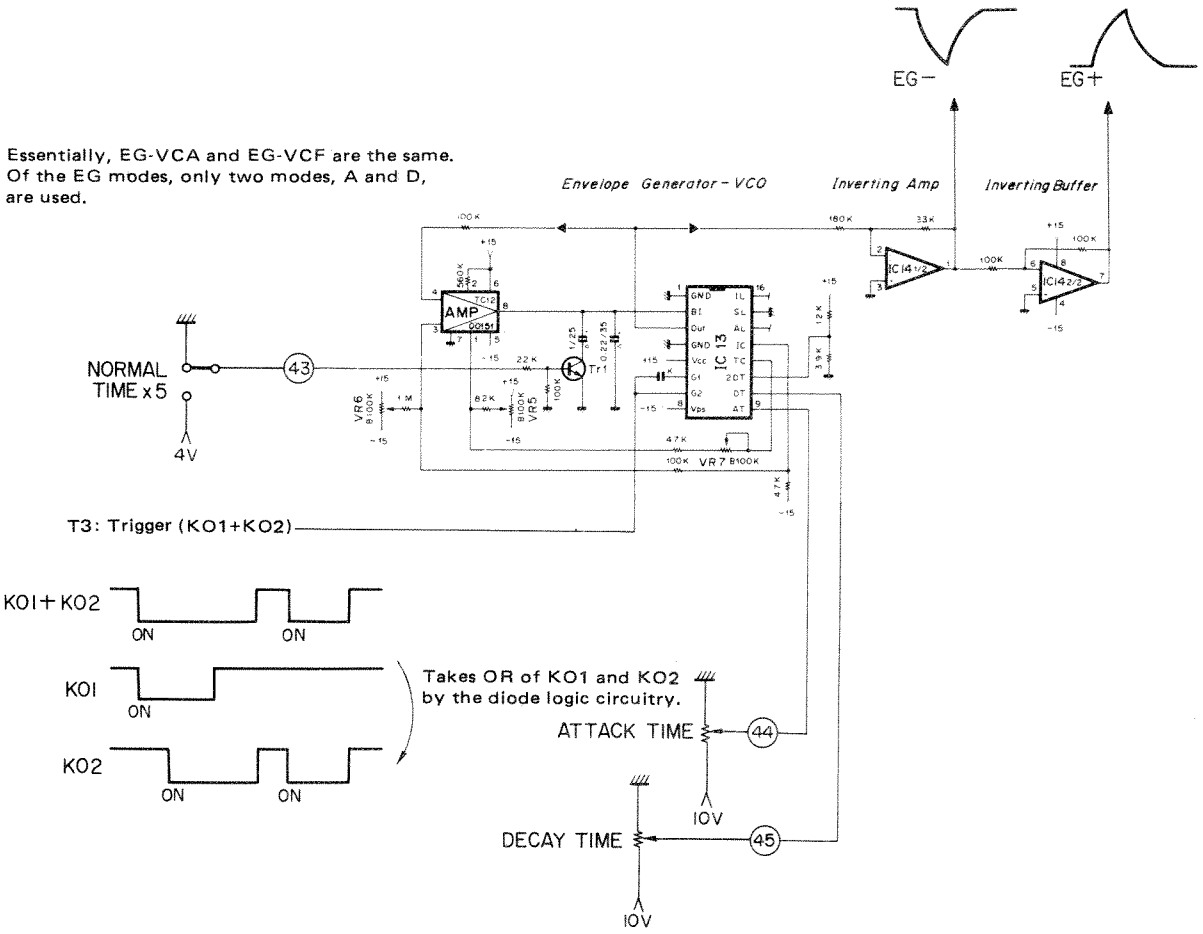
EG depth

At the same time, the IG00151 will function as a VCA, varying the output with the control voltage applied to Pin 2.



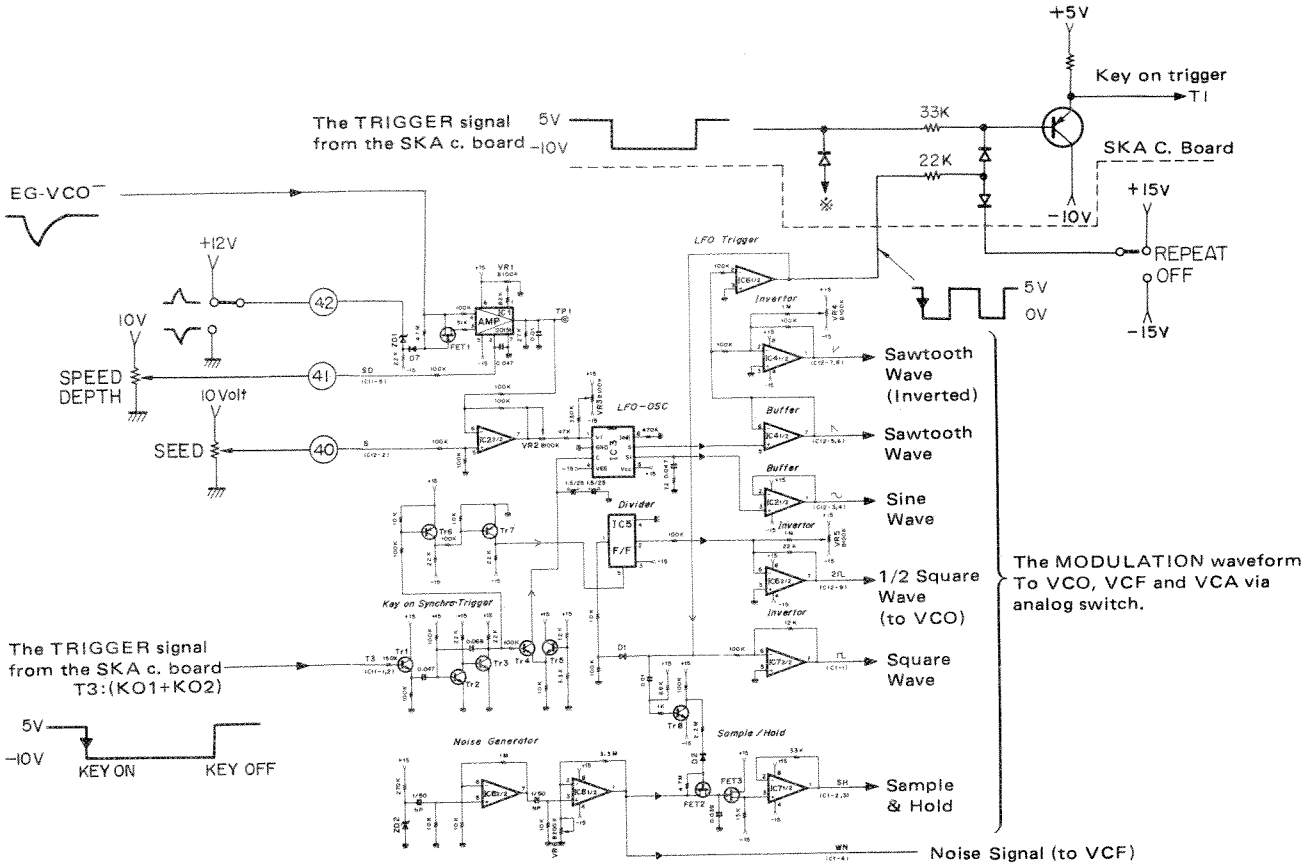
3. EG-VCO CIRCUIT

The EG-VCO circuit also employs the IG00159 and adopts a circuit system similar to the EG-VCA, etc. However, with the SUSTAIN level terminal grounded, it only uses 2 modes, A and D. As output, the EG voltage for reversing and non-reversing are constantly fed out.



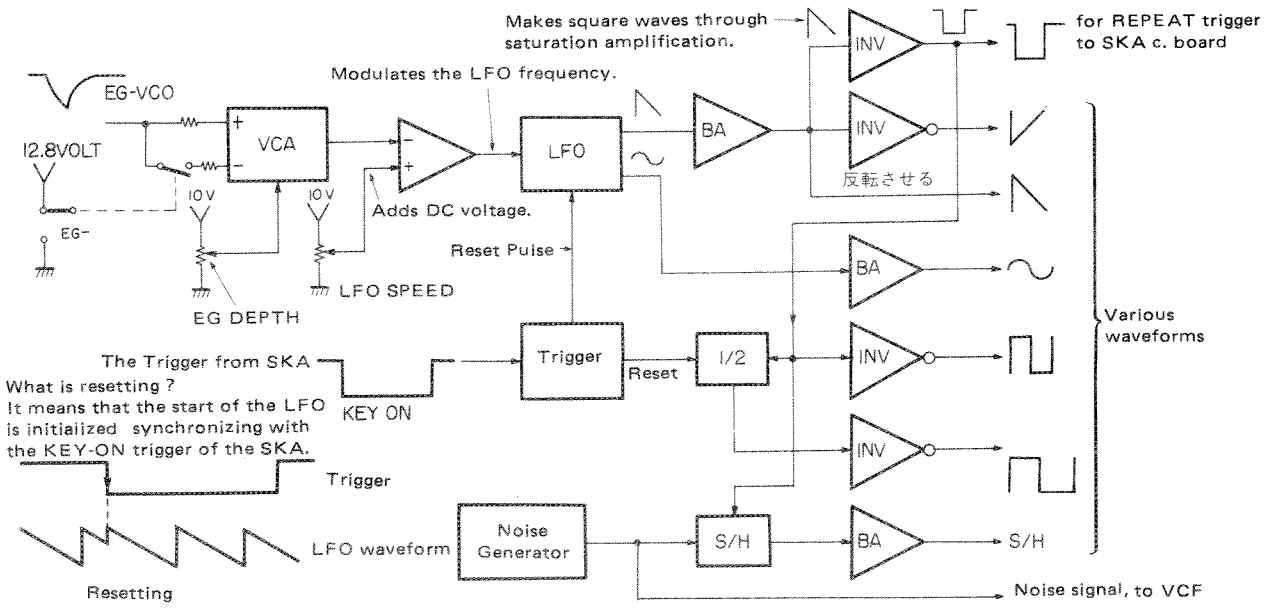
LFO AND PERIPHERAL: MOD, FA BOARD

This section, which is built centering around the IG00150 (a LFO IC used exclusively for the LFO) also includes the peripheral circuits.



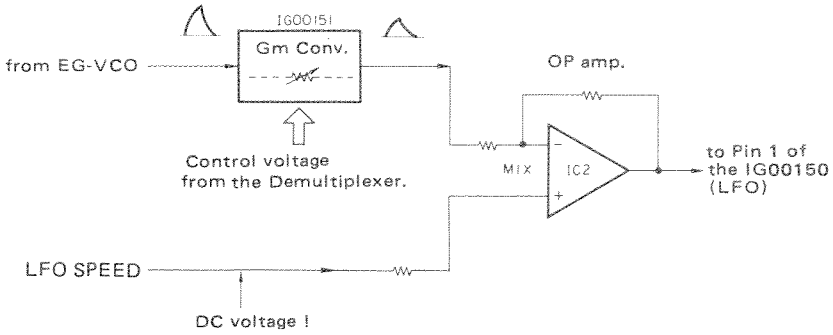
FUNCTIONS OF LFO

This block functions to oscillate ultra-low frequencies used for the modulation of VCO, VCF and VCA, using the various LFO waveforms.



1. VCA (Voltage Controlled Amplifier)

The VCA is operated by IC1 (IG00151). Its operating principles are exactly the same as that explained for the VCA. It is a voltage controlled amplifier that controls the VCO-EG's output voltage, which is used for varying the oscillating frequency of the LFO. Accordingly, the input signals of this VCA are the output voltages of the VCO-EG. VCA's control voltage is sent in from the demultiplexer.

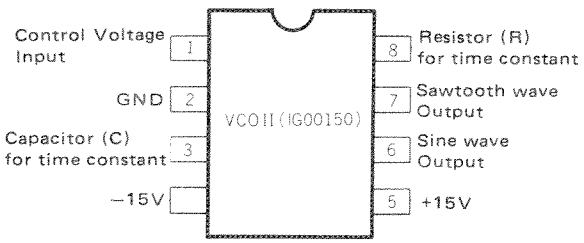


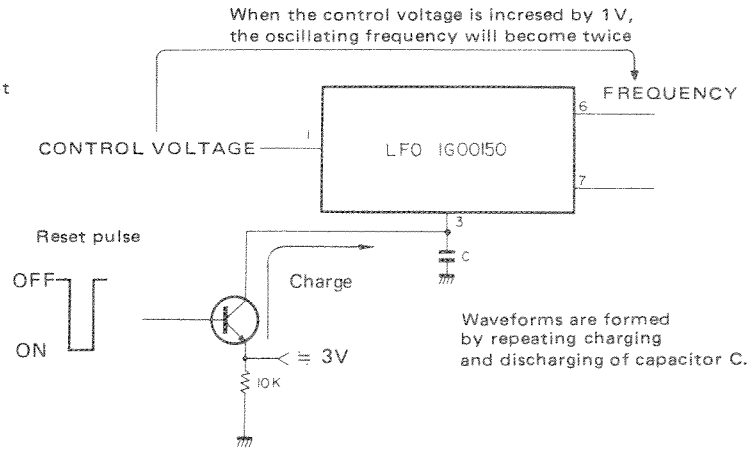
Polarity

After being mixed with the oscillating frequency control voltage of the LFO, the VCF output is sent to the LFO. FET 1 operates as a polarity changing switch for IC 1.

2. LFO OSCILLATOR CIRCUIT

The LFO uses the IG00150, whose operating principles are the same as those of the IG00153. However, this LFO incorporates a logarithmic conversion circuit inside the IC so that frequencies twice or one and half as large may be obtained with regard to a 1V variation of the input control voltage. Further, it incorporates two wave shaping circuits, one for the sine wave and the other for the sawtooth wave. When the capacitance of the capacitor connected to Pin 3 is increased, the frequency will be lowered.





LFO reset

The transistor switch is connected to Pin 3. When this transistor turns on, it causes C to rapidly charge its voltage. As a result, the LFO is reset to the initial state.

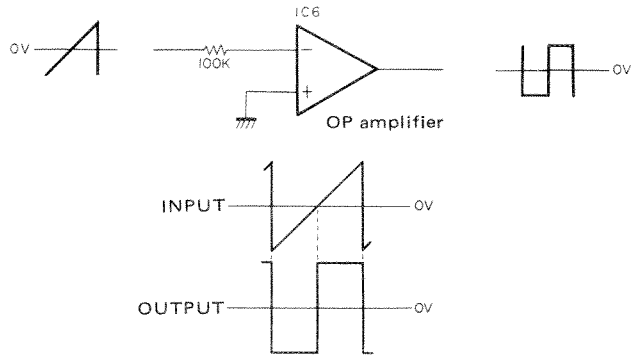
3. LFO WAVEFORM SHAPING

■ **Sine Wave, Sawtooth Wave and Inverted Sawtooth Wave**

These waveforms are fed out, respectively, from the output terminals of the IG00150 passing through a buffer, another buffer and inverter.

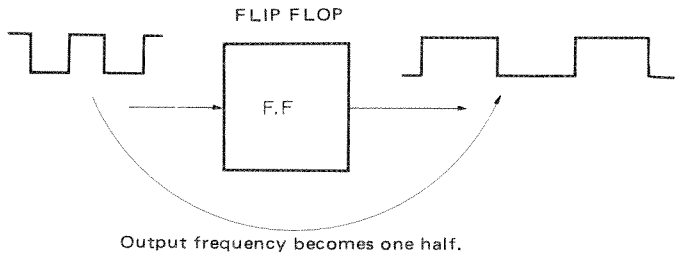
■ **Square waves**

Square waves are obtained by feeding in sawtooth waves into the clipper circuit of IC6, where the sawtooth waves will be subjected to saturation amplification and converted into square waves. (For VCF and VCA circuits)



■ **1/2 Square Wave**

This waveform is used for the VCO circuit to prevent VCO's tremolo from synchronizing with VCO's pitch variation.
Square waves are fed into the flip-flop of IC5 from the output terminal of IC6's clipper by way of a diode. This will cause square waves to be divided into one half and to be fed out through the inverter of IC6.



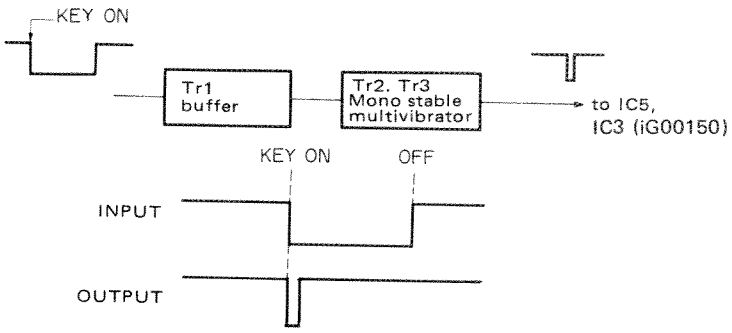
★ Since the flip-flop cannot be reset even when the input is changed midway of operation, it is to be reset with the RESET terminal set to "0".

4. KEYED TRIGGER TIMING CIRCUIT

This circuit, which is formed with $Tr_1 \sim Tr_5$, feeds out a short-duration pulse which is generated corresponding to the fall in pulse that takes place when a Key-On trigger is applied. It is used for resetting the IC5 (BA634) and IG00150.

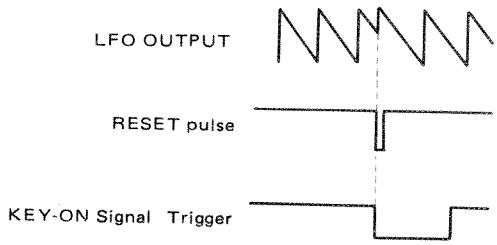
Reset pulse

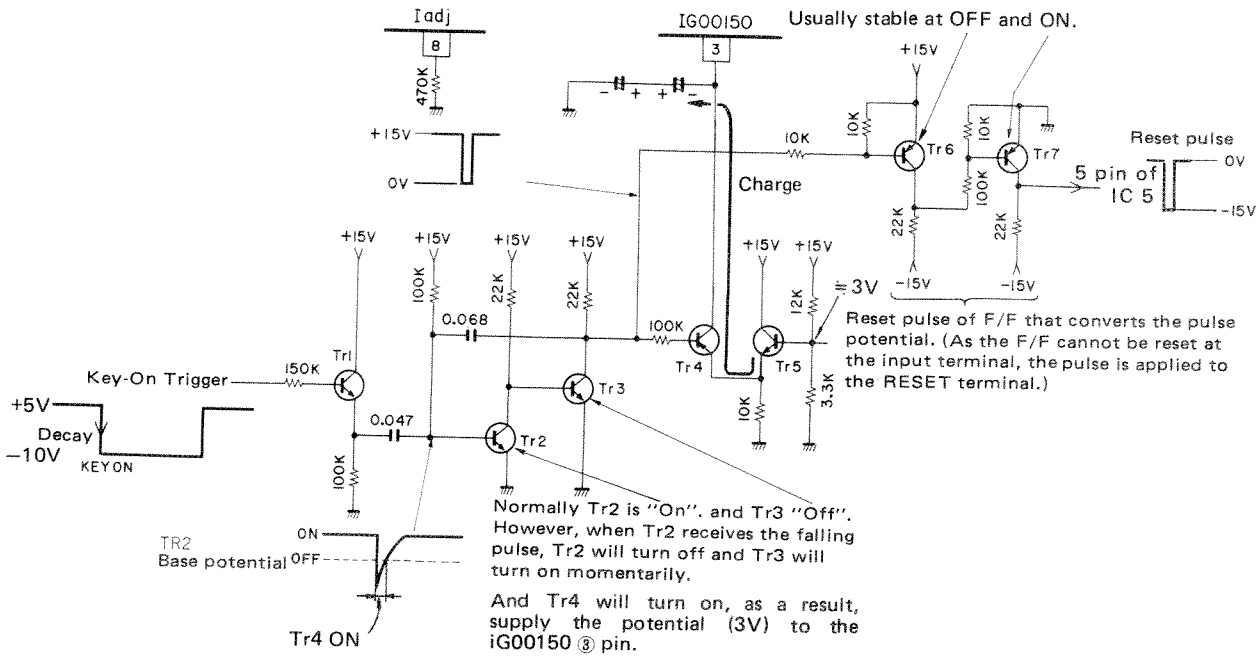
Tr_1 serves as a buffer that transmits the Key-On trigger to Tr_2. Tr_2 and Tr_3 together form a mono-stable multivibrator, feeding out short-duration pulses when a Key-On trigger has been applied. This pulse is transmitted to IC5 by way of Tr_6 and Tr_7, as well as to IC3 by way of Tr_4, to reset the respective ICs.



Synchronize

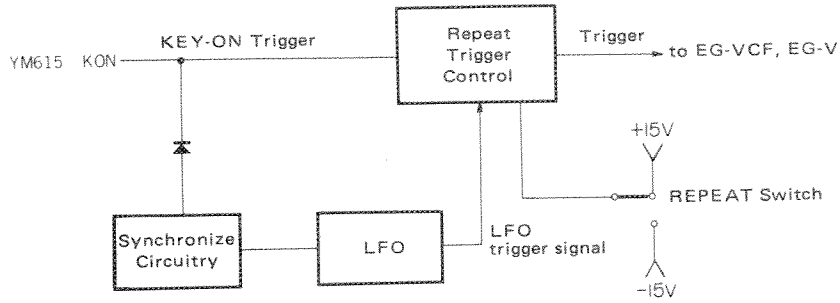
This arrangement is taken to synchronize the tone (VCF), volume (VCA) and LFO effects when a trigger is effected at the LFO speed, and at the same time, to prevent the tone and volume from changing at Key-On.





5. REPEAT TRIGGER CIRCUIT

The trigger signals from the SKA that accompanies Key-On and Key-Off are used as the triggers to start the EG's VCA, VCF. This trigger can be controlled at the LFO with the REPEAT switch.



When the REPEAT switch is set to "REPEAT", the trigger that controls such selection as the EG-VCA, is effected not only by Key-On and Key-Off signal but also by the LFO's square wave.

Diode OR Logic

Repeat operations are controlled chiefly by diodes. With reference fo Fig. 1, when the potential at Point (A), or Point (B) drops, it will cause current to flow from Point (C) to Point (A), or to Point (B), so that the pontential at Point (C) will drop. In this case, the voltage at Point (C) will be higher than that of Point (A) and Point (B), by a degree equivalent to the diode's forward voltage.

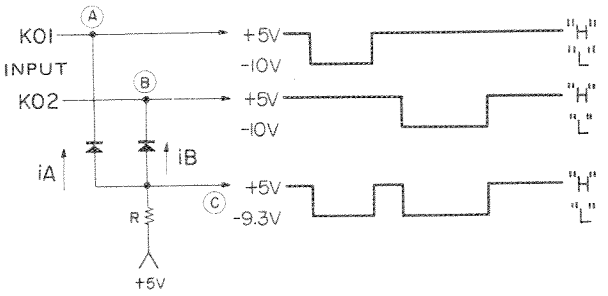


Fig. 1

Repeat off

With reference to Fig. 2, the potential at Point (E) will become −14.3V. The voltage variation at Point (G) will not appear at Point (C).

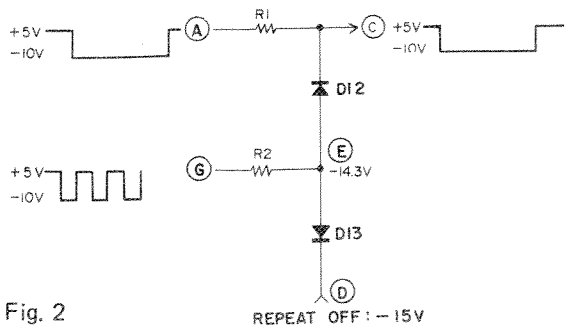


Fig. 2

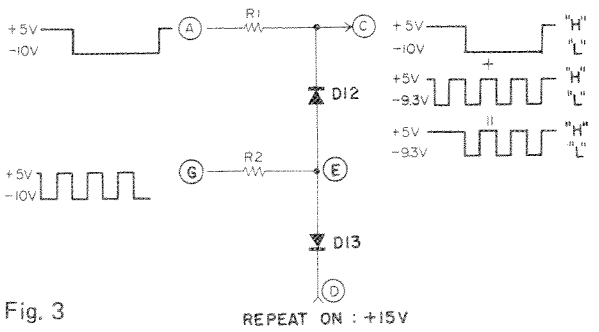
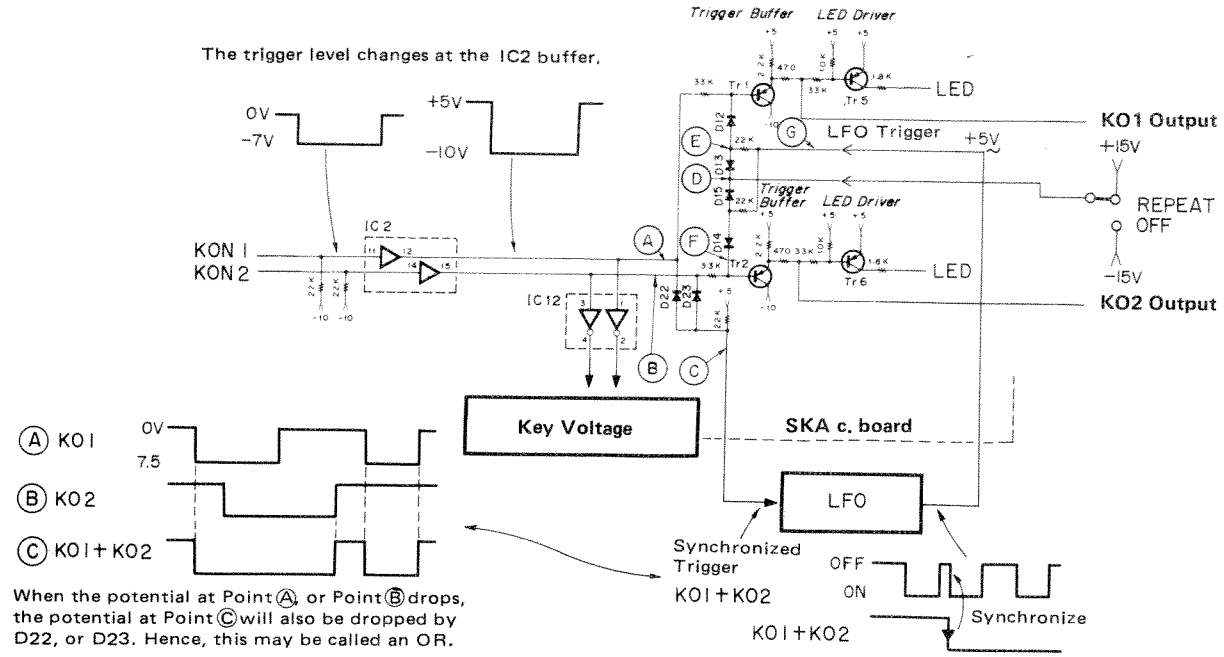


Fig. 3

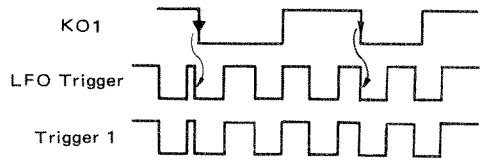
Repeat on

Now, with reference to Fig. 3, no current will flow as the potential of Point (G) will be lower than that at Point (D). As a result, the voltage of Point (G) appears at Point (E). The voltage of Point (G) will appear at Point (C), with its value reduced by a degree equivalent to the forward voltage of D12. Consequently, the variations of (A) and (G) will be mixed at Point (C). This circuit functions as positive enabled OR logic.

The actual circuit is more complicated, but if you follow the logical sequence, bit by bit, it will not be too difficult to understand.



At REPEAT the trigger will be as shown below.



DESCRIPTION OF OPERATION

When −15V is applied to Point Ⓓ, Points Ⓔ and Ⓕ will retain its voltage of −14.3 V, even when a trigger from LFO is fed into Point Ⓖ.

Meanwhile, when +15V (REPEAT) is applied to D, the variation of Point Ⓖ will appear at Points E and F, contributing to turning Tr1 an Tr2 On and Off.

Tr1 turns on when Point Ⓐ or Point Ⓖ is "On", while Tr2 will turn on when Point Ⓑ of Ⓖ turns "On".

6. SAMPLE & HOLD CIRCUIT AND NOISE GENERATOR

Noise

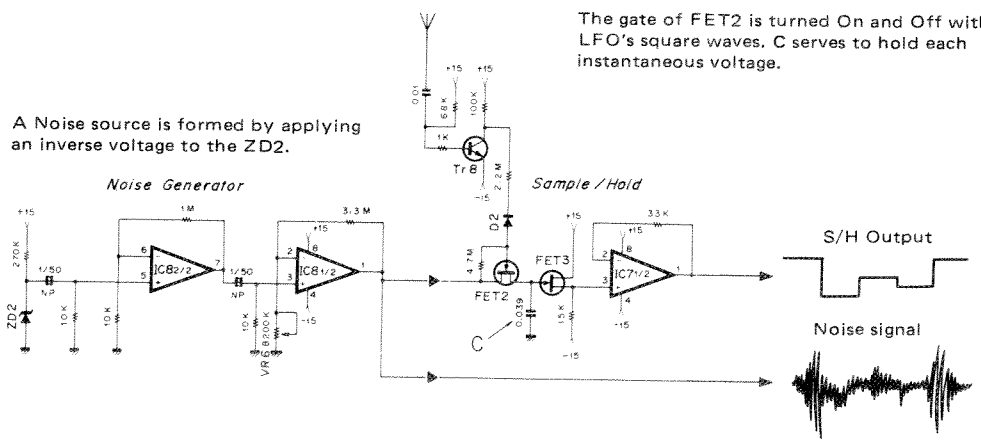
An inverse voltage is applied to a zenner diode for use as a noise source. This voltage is amplified by the OP amplifier and used as noise. In this point, the circuit is absolutately the same as conventional circuits.

S/H

In terms of operating principles, this circuit is exactly the same as the Sampling-and-Hold circuit that has been described in the section where the Key Voltage has been explained.

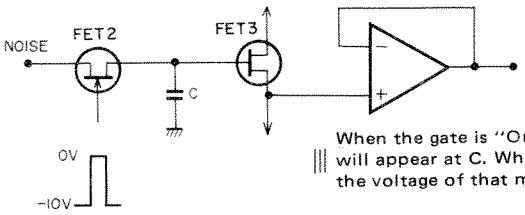
The gate of FET2 is turned On and Off with LFO's square waves. C serves to hold each instantaneous voltage.

A Noise source is formed by applying an inverse voltage to the ZD2.

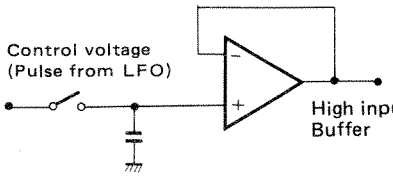


R = ∞

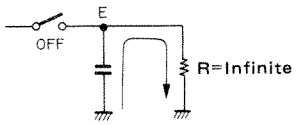
In other words, the square waves from LFO are applied to the base of Tr_2 by way of a capacitor, which differentiates the square waves to generate pulse. This pulse, after passing through Tr_8 and D2, is applied to FET2, causing FET2 to turn on only for the duration a short pulse is applied. Consequently, the noise voltage when FET2 is "ON" will be held by the 0.039μF capacitor. FET3 and IC3, which are high-input-impedance buffers, function to hold that certain voltage until the next pulse comes in.



When the gate is "On", the noise voltage will appear at C. When the gate turns "Off" the voltage of that moment will be held by C.



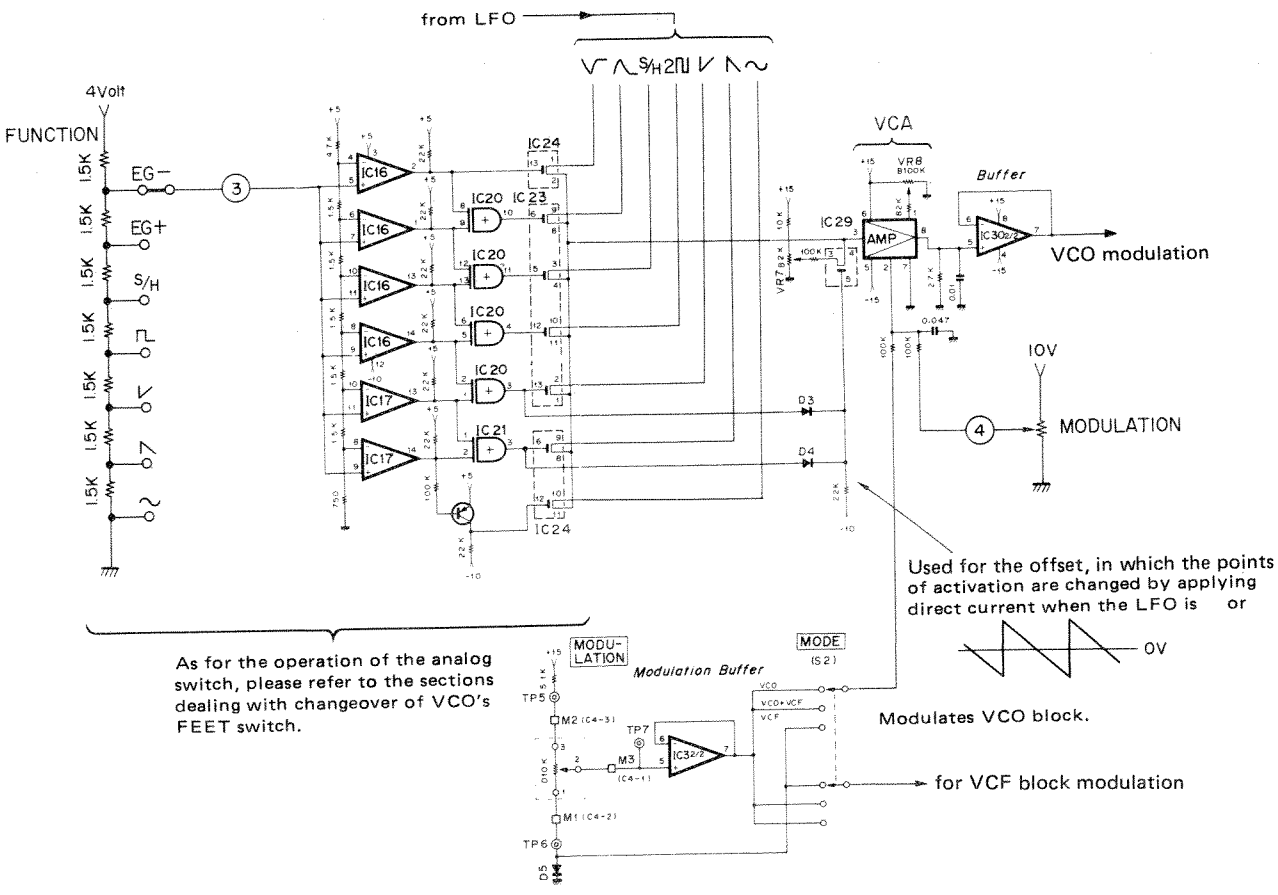
High input impedance Buffer



As there will be practically no current flow, the voltage of E does not drop.

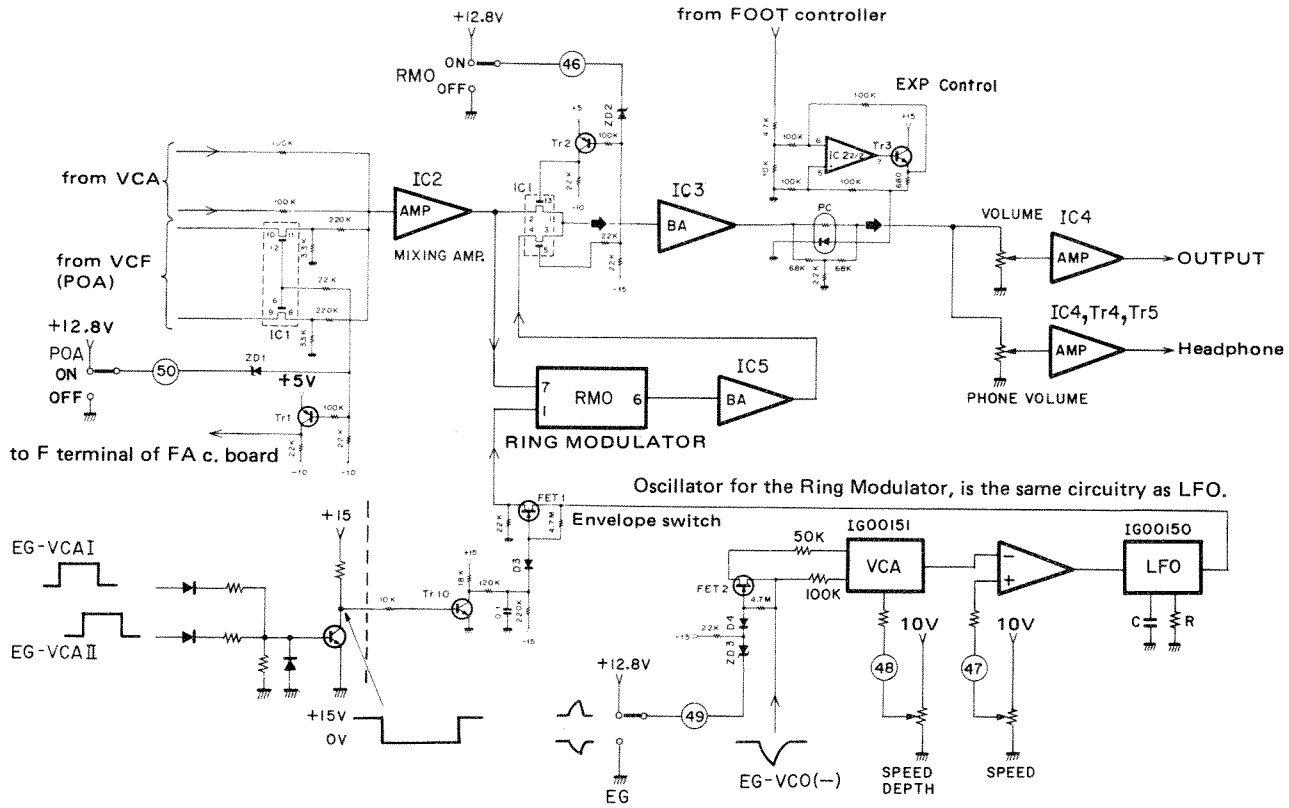
7. MODULATION SIGNAL SELECTOR CIRCUIT

This circuit is similar to the circuit used for changing over, the FEET switch of the VCO section, for exanple. The circuit diagram is given below but no description will be given here.



RING MODULATOR: PB BOARD

The PB Unit is that section interposed between the VCA (or VCF) and output jacks. It is composed of such sections as 1) the POA switch section that functions to changeover the VCF (POA) input and VCA input for the block that applies RING MODULATION, and 2) the output amplifying section. The block diagram of this unit centering around the switch section is shown below.



■ Outline of Circuits

POA switch

Outputs from the VCA circuit are mixed at IC2. Signals from the VCF circuit are sent in directly to the analog switch. Therefore, when the POA switch is turned on, the analog switch will also turn on. The outputs of the analog switch are mixed at IC2.

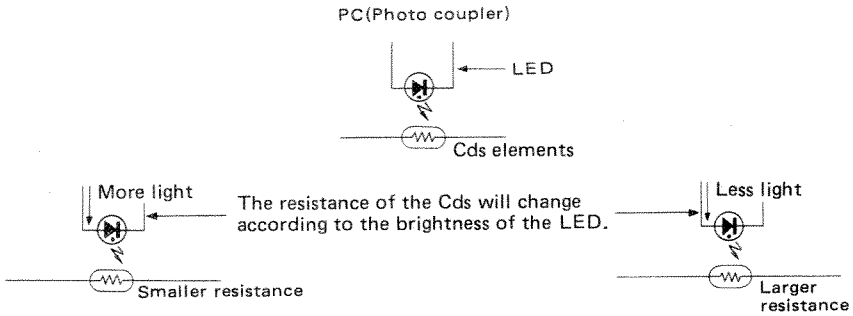
PMO switch

The outputs of IC2 are divided into those that go to the analog switch and those that go to the ring modulator (to be referred to as RMO hereafter). When the RMO switch is "OFF", the analog switch will be "ON" for the section from IC2 to IC3, and when the RMO switch is "ON", the analog switch will be "ON" for the sections from RMO up to IC3.

Foot control

Signals that have passed through the IC3 buffer are further passed through the photocoupler (PC). As shown in next figure, the photocoupler is an element that controls the resistance corresponding to the size of the current that is flown to the light emitting diode. This is a pedal control. When the pedal is stepped on, the action causes the IC2 (EXP-Control) to convert the current, which is then flown to the light emitting diode in the PC. The Cds of the PC are controlled by this light. In other words, when the pedal is depressed deeply, more current will flow and more light will be emitted. This will cause the resistance of the Cds to drop, and the volume will increase as a result. The output fed out from PC will be divided into two,

one going to the output jack after passing through the VOLUME and output amplifier, and the other to HEADPHONES after passing through the phones volume and phones amplifier.



■ Ring Modulation

Multiplier

The function of the RMO (ring modulator) is to produce the sum and difference between the frequencies that have been fed in.
This is a multiplier, or in other words an applied circuit of a balanced modulator. The product of two inputs X and Y appear at the OUTPUT. Here, we shall assume that X and Y are such AC signals as shown below.

$X = \sin x$ (Frequency : x)

$Y = \sin y$ (Frequency : y)

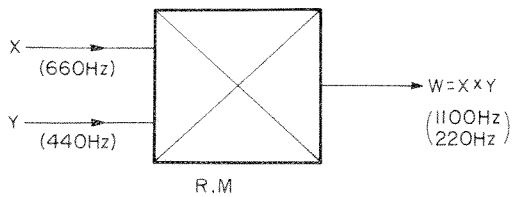
Hence, the output W will be

$$W = X \times Y = \sin x \times \sin y = -\frac{1}{2}\cos(x+y) + \frac{1}{2}\cos(x-y)$$

(The Product and Sum Formula)

Discord

When, for example, 660Hz (E) is fed into X and 440Hz (A) into Y, the note of 220Hz (660—440) (A) and 1100Hz (660+440) (= $C^{\#}$) will appear at the output. Since these rates have no direct relation to the input pitch, it will result in producing a discord.



Product Sum Subtract

$$\sin x \times \sin y = -\frac{1}{2}\cos(x+y) + \frac{1}{2}\cos(x-y)$$

Although the output from the oscillator (LFO) for the RMO will be fed into Pin ① of IC5, the FET switch which is located inbetween is designed so as to turn ON and OFF depending on the presence of an envelope from the EG-VCA. This arrangement is taken to prevent the LFO output from being fed out when the key is not being depressed. Since this LFO adopts a circuit conposition exactly the same as that adopted for the MOD block, description shall be omitted here.

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