■ LSI PIN DESCRIPTION

● **HD6435208A00P** (XK278A00) CPU <H8/520>

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	EXT	I	Clock	33	A7	O	
2	EXTAL	I		34	A8	O	
3	/WAIT	I	Bus cycle wait	35	A9	O	
4	/IRQ0	O	Interrupt request	36	A10	O	
5	A18	O		37	A11	O	Address bus
6	A17	O	Address bus	38	A12	O	
7	A16	O		39	A13	O	
8	/AS	O	Address strobe	40	A14	O	
9	/RD	O	Read strobe	41	A15	O	
10	/WR	O	Write strobe	42	AVCC		Analog power supply
11	VCC		Power supply	43	P50	O	
12	MD0	I		44	P51	O	
13	MD1	I	Mode select	45	P52	O	
14	MD2	I		46	P53	O	Port 5
15	/RES	I	Reset	47	P54	O	
16	NMI	I	Non-maskable interrupt request	48	P55	O	
17	VSS		Ground	49	P56	O	
18	D0	I/O		50	P57	O	
19	D1	I/O		51	VSS		Ground
20	D2	I/O		52	AVSS		Analog ground
21	D3	I/O	Data bus	53	AN0	I	
22	D4	I/O		54	AN1	I	Analog data input
23	D5	I/O		55	AN2	I	
24	D6	I/O		56	AN3	I	
25	D7	I/O		57	AVCC		Analog power supply
26	A0	O		58	TXD2	O	Transmit data
27	A1	O		59	RXD2	I	Receive data
28	A2	O		60	A19	O	Address bus
29	A3	O	Address bus	61	TXD1	O	Transmit data
30	A4	O		62	RXD1	I	Receive data
31	A5	O		63	SCLK	I	Clock for serial operation
32	A6	O		64	VSS		Ground

● **AK4320-VM-E1** (XR361A00) DAC

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	CKS	I	Clock select	13	DEM1	I	De-emphasis mode
2	DVDD		Digital VDD	14	DIF0	I	Input format
3	DVSS		Digital GND	15	DIF1	I	
4	XTO	O	Xtal out	16	VCNT	I	Mute Control
5	XTI	I	Xtal in	17	AOUTR	O	Analog output R
6	/PD	I	Power down	18	AOUTL	O	Analog output L
7	BICK	I	Serial bit clock	19	VCOM	O	Common
8	SDATA	I	Serial data input	20	AVDD		Analog VDD
9	LRCK	I	L/R clock	21	AVSS		Analog VSS
10	SMUTE	I	Soft mute	22	VREF	I	V reference
11	HOLD	I	Soft mute hold	23	DZF	O	Zero input
12	DEM0	I	De-emphasis mode	24	ZMUTE	I	Zero mute

● **LZ95300** (XP451A00) Gate Array

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	INC	O	INPUT CUE ON/OFF	15	/CSW	I	CUE switch input
2	CPR	O	VCA CUE PRE PAN ON/OFF	16	VCA8	I	
3	CPST	O	VCA CUE POST PAN ON/OFF	17	VCA7	I	
4	COFF	O	All CUE OFF	18	VCA6	I	
5	CPU	I	H: CPU mode, L: Local mode	19	VCA5	I	VCA GROUP switch input
6	C0	I		20	VCA4	I	
7	C1	I	CPU address bus	21	VCA3	I	
8	C2	I		22	VCA2	I	
9	C3	I		23	VCA1	I	
10	/RES	I	Reset	24	/SLSF	I	SOLO SAFE switch input
11	DATA	I/O	Data input/output	25	/CHK	I	CHECK LED ON/OFF
12	IRQ	O	When /ONSW and /CSW change; H. When CPU reads data; L.	26	/ONSW	I	ON switch input
13	/CS	I	Chip select	27	/ONRY	O	ON relay & LED ON/OFF
14	GND		Digital ground	28	VDD		Digital power supply

● Function of DATA

C3	C2	C1	C0	R/W	MODE	FUNCTION	DATA 0	DATA 1
0	0	0	0	W	ON RELAY SET	Sets /ONRY	OFF	ON
0	0	0	1	R	ON SW READ	Reads /ONSW	OFF	ON
0	0	1	0	W	CUE RELAY SET	Sets INC ON	OFF	ON
0	0	1	1	R	CUE SW READ	Reads /CSW	OFF	ON
0	1	0	0	W	CHECK LED SET	Sets /CHK	OFF	ON
0	1	0	1	W	VCA PRE/POST SET	Sets CVCA CUE PRE/POST PAN	POST	PRE
0	1	1	0	W	SOLO SET	Sets SOLO When SOLO is set, CUE or SOLO SAFE is not ON, /ONRY is set to OFF.	OFF	SOLO
0	1	1	1	W	VCA1 CUE SET	Sets VCA1 CUE	OFF	ON
1	0	0	0	W	VCA1 CUE SET	Sets VCA1 CUE	OFF	ON
1	0	0	1	W	VCA2 CUE SET	Sets VCA2 CUE	OFF	ON
:	:	:	:	:	:	:	:	:
1	1	1	1	W	VCA8 CUE SET	Sets VCA8 CUE	OFF	ON

● **YSP99 LZ95XD59** (XM047A00) Gate Array

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	NC			41	A9	I	CPU address bus
2	MCLK	O	Master clock	42	A8	I	
3	DESYN	O	Sync for DEQIC	43	CD2	I	CARD page select
4	CD04	I	Control data input	44	CD1	I	
5	CD03	I		45	CDROM	I	CARD/ROM select
6	CD02	I		46	ROM4	I	ROM page control
7	CD01	I		47	ROM3	I	
8	CDI4	O	Control data output (DSP2)	48	ROM2	I	
9	CDI3	O	Control data output (MOD)	49	ROM1	I	
10	CDI2	O	Control data output (DEQ IC17)	50	YY2	I	Dividing select
11	CDI1	O	Control data output (DEQ IC19)	51	YY1	I	
12	+Vdd			52	GND		
13	GND			53	+Vdd		
14	L4	O	LED scan pulse	54	SEL2	I	Control data select
15	L3	O		55	SEL1	I	
16	L2	O		56	XX2	I	LED scan data
17	L1	O		57	XX1	I	
18	LCD	O	LCD enable	58	MDCK	O	MIDI clock
19	KEYN	O	KEY enable	59	TRG0	O	Trigger out
20	LED	O	LED enable	60	E	I	
21	CDA14	O	CARD address	61	RWN	I	Read write pulse
22	CDA13	O		62	ICN	I	Initial clear
23	CARDN	O	CARD enable	63	ACIA	O	ACIA enable
24	GND			64	GND		
25	RAWN	O	RAM write enable	65	TXD	I	DSP control data input
26	RAON	O	RAM read enable	66	RXD	O	DSP control data output
27	RMA16	O	ROM address back select	67	XCLK	O	Transfer clock
28	RMA15	O		68	WCLK	O	Word clock
29	RMA14	O		69	SCLK	O	Serial data transfer clock 64fs
30	RMA13	O		70	FSYNC	O	NC
31	+Vdd			71	ADLR	O	NC
32	GND			72	GND		
33	ROMN	O	ROM read enable	73	+Vdd		
34	A15	I	CPU address bus	74	SCLKN	O	Serial data sift clock
35	A14	I		75	DCLK	O	256fs clock
36	A13	I		76	XI	I	Clock input/(Xtal)
37	A12	I		77	XO	O	output/(Xtal)
38	A11	I		78	GND		
39	A10	I		79	TRIG	I	Trigger input
40	NC			80	SYNCN	O	Sync clock

● **YSS228E-F** (XQ962D00) DSP3 (Digital Signal Processor)

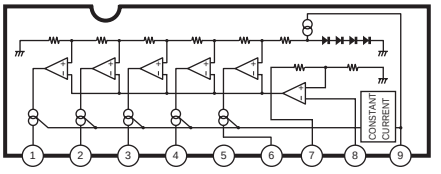
DM : IC2, 3

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	VSS		Ground	81	VSS	I/O	Ground
2	XI	I	System master clock input (60 M or30 MHz)	82	DB13	I/O	
3	XO		System master clock input (60 M or30 MHz)	83	DB14	I/O	
4	VDD		Power supply	84	DB15	I/O	
5	/SYNCI	I	System synch. input	85	DB16	I/O	
6	/SYNCO	O	System synch. output	86	DB17	I/O	
7	CKI	I	System clock input (30 MHz)	87	DB18	I/O	
8	CKO	O	System clock output (30 MHz)	88	DB19	I/O	
9	CKSL	I	System master clock select (0:60 M,1:30 MHz)	89	DB20	I/O	
10	VSS		Ground	90	DB21	I/O	
11	MCKS	I	Master clock for serial I/O(128 xFs)	91	DB22	I/O	Parallel data bus
12	/SSYNC	I	Synch. signal for serial I/O	92	DB23	I/O	
13	/IC	I	Initial clear	93	DB24	I/O	
14	/TEST	I	Test mode setting	94	DB25	I/O	
15	BTYP	I	CPU data bus 8/16 bit select(0:8,1:16)	95	DB26	I/O	
16	/IRQ	O	Interrupt request	96	DB27	I/O	
17	TRIG	I/O	Trigger signal	97	DB28	I/O	
18	VDD		Power supply	98	DB29	I/O	
19	VSS		Ground	99	DB30	I/O	
20	/CS	I	Chip select	100	DB31	I/O	
21	/DS	I	Data strobe	101	TIMO/DBOE	I/O	Timing signal/Parallel data bus control
22	R/W	I	Read/Write select	102	VSS		Ground
23	CA7	I		103	VDD		Power supply
24	CA6	I		104	DA00	I/O	
25	CA5	I		105	DA01	I/O	
26	CA4	I	CPU address bus	106	DA02	I/O	
27	CA3	I		107	DA03	I/O	
28	CA2	I		108	DA04	I/O	
29	CA1	I		109	DA05	I/O	
30	CA0/CD15	I/O	CPU address/data bus	110	DA06	I/O	
31	CD14	I/O		111	DA07	I/O	
32	CD13	I/O		112	DA08	I/O	External memory data bus
33	CD12	I/O		113	DA09	I/O	
34	CD11	I/O		114	DA10	I/O	
35	CD10	I/O	CPU data bus	115	DA11	I/O	
36	CD09	I/O		116	DA12	I/O	
37	CD08	I/O		117	DA13	I/O	
38	CD07	I/O		118	DA14	I/O	
39	CD06	I/O		119	DA15	I/O	
40	VSS		Ground	120	VSS		Ground
41	VDD		Power supply	121	VDD		Power supply
42	CD05	I/O		122	DA16	I/O	
43	CD04	I/O		123	DA17	I/O	
44	CD03	I/O	CPU data bus	124	DA18	I/O	
45	CD02	I/O		125	DA19	I/O	
46	CD01	I/O		126	DA20	I/O	
47	CD00	I/O		127	DA21	I/O	
48	/DTACK	O	DTACK signal output	128	DA22	I/O	
49	SI0	I		129	DA23	I/O	
50	SI1	I		130	DA24	I/O	External memory data bus
51	SI2	I		131	DA25	I/O	
52	SI3	I	Serial data input	132	DA26	I/O	
53	SI4	I		133	DA27	I/O	
54	SI5	I		134	DA28	I/O	
55	SI6	I		135	DA29	I/O	
56	SI7	I		136	DA30	I/O	
57	VSS		Ground	137	DA31	I/O	
58	VDD		Power supply	138	VDD		Power supply
59	SO0	O		139	VSS		Ground
60	SO1	O		140	A00	O	
61	SO2	O		141	A01	O	
62	SO3	O	Serial data output	142	A02	O	
63	SO4	O		143	A03	O	
64	SO5	O		144	A04	O	
65	SO6	O		145	A05	O	
66	SO7	O		146	A06	O	
67	DB00	I/O		147	A07	O	External memory address bus
68	DB01	I/O		148	A08	O	
69	DB02	I/O		149	A09	O	
70	DB03	I/O		150	A10	O	
71	DB04	I/O		151	A11	O	
72	DB05	I/O		152	A12	O	
73	DB06	I/O	Parallel data bus	153	A13	O	
74	DB07	I/O		154	A14	O	
75	DB08	I/O		155	A15/RAS	O	External memory address bus/Row address strobe
76	DB09	I/O		156	A16/CAS	O	External memory address bus/Column address strobe
77	DB10	I/O		157	A17/CE	O	External memory address bus/Chip enable
78	DB11	I/O		158	/WE	O	External memory write enable
79	DB12	I/O		159	/OE	O	External memory output enable
80	VDD		Power supply	160	VDD		Power supply

IC BLOCK DIAGRAM

● **BA6144** (XA552A00)
ST4: IC121,IC221,IC321,IC421
IN3: IC103,IC203,IC303,IC403,
IC503,IC603,IC703,IC803

METER DRIVER

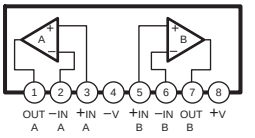


● **NJM2068-D**(XM356A00)
ST1: IC101~106,IC201~204,
IC301~305,IC401~404
MAS3: IC952,IC953
MAS2: IC101,IC151,IC301,IC351,IC501,
IC551,IC751,IC901~903
MAS1: IC101~103,IC301~303,IC501~503,
IC701~703
ISRT: IC101~104,IC111~115,IC121~124,
IC201~217
IN1: IC103~107,IC303~307,IC503~507,
IC703~707

● **NJM2082M(T1)**(XN797A00)
CTRL: IC108

● **NJM4558L-D**(XQ212A00)
METER1: IC102
METER2: IC102

OP AMP

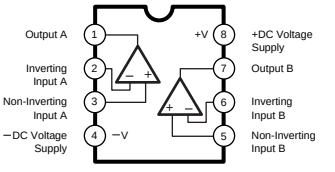


● **NJM4556AL**(XP844A00)
MAS: IC951

● **NJM4580L**(XF195A00)
ST2: IC101~103,IC301~303
ST3: IC101,IC201,IC301,IC401
MASOUT3: IC101,IC201,IC301
MSOUT1,2: IC301,IC201,IC301,IC401
MAS3: IC101,IC301,IC501,IC701,
IC901,IC902
MAS1: IC901
IN3: IC101,IC102,IC301,IC501,IC502,
IC701,IC702
IN1: IC101,IC102,IC301,IC501,IC502,
IC701,IC702

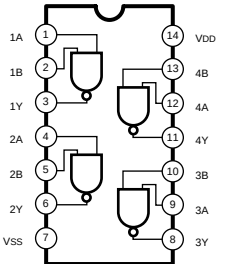
● **M5238AP**(XM085A00)
DC: IC101,IC201,IC202

OP AMP



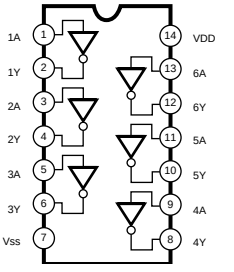
● **SN74HC00NSR** (XE165A00)
CTRL: IC113

NAND



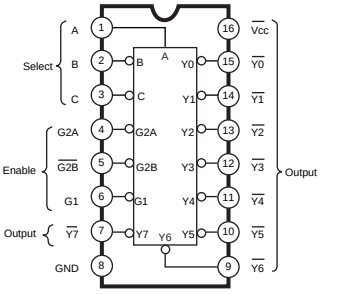
● **SN74HC04NSR** (XD830A00)
CTRL: IC109

INVERTER



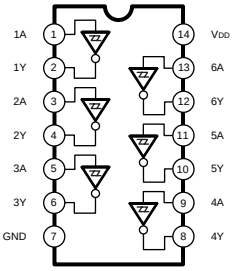
● **SN74HC138NSR** (XD835A00)
CTRL: IC124

DECODER



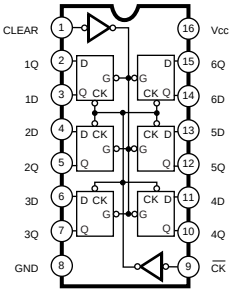
● **SN74HC14NSR** (XC725A00)
CTRL: IC110,IC302

INVERTER



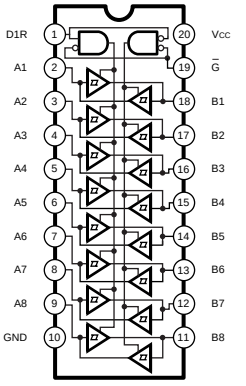
● **SN74HC174NSR** (XD836A00)
CTRL: IC123

D-FF



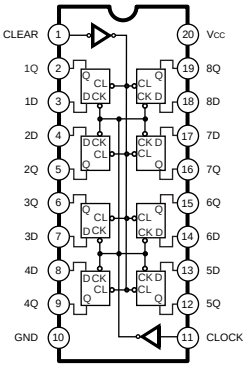
● **SN74HC245NSR** (XD838A00)
CTRL: IC121,IC125,IC131

BUFFER



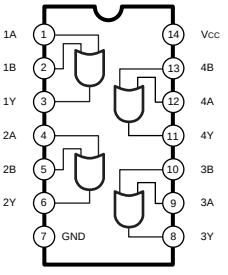
● **SN74HC273NSR** (XH223A00)
CTRL: IC132

D-FF



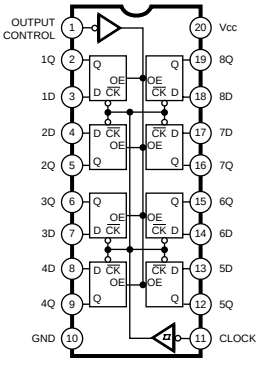
● **SN74HC32NSR** (XD833A00)
CTRL: IC112

OR



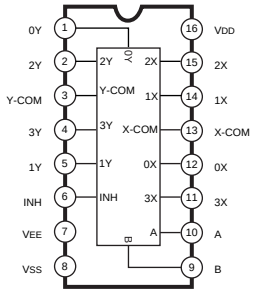
● **SN74HC374ANSR** (XQ042A00)
CTRL: IC122

D-FF



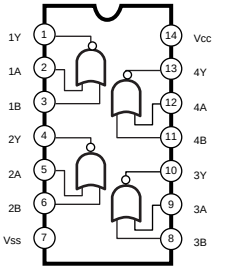
● **TC4052BP** (XA053A00)
METER1: IC101
METER2: IC101

MULTIPLEXER



● **SN74HC02AP** (IR000200)
ST4: IC102 MAS4: IC102,502,902
IN4: IC102,IC302

NOR



● **SN74HC139AP** (IR013900)
MAS2: IC910

DECODER