# ■ INSPECTION

## 1. Range of Application

These specifications apply to the DSP1D and DSP1D-EX.

## 2. Preparations

### 2-1. Conditions

◇ For details on the connection method, refer to the Test Program Specifications KES-92651.

◇ The function generator used for inspection must be the Sony Tektronix AFG310 or equivalent. When using the AFG310, the settings are as follows.

FUNC :PULS
MODE :CONT
MODUL :OFF
AMPL :1.800
OFFSET :0.900

◇ Unless otherwise specified, the conditions are as follows.

· The function generator BNC output is connected to WORD CLOCK IN (BNC).

· Set WORD CLOCK IN to 75 Ω.

### 2-2. Loading the Firmware

The firmware used must be the "CS1D Firmware" (managed with the already drawn CD-R assembly drawing (3JL-XY714A0) of the FMID System Software matching the version on the cover sheet. For details on the firmware writing method, refer to the Test Program Specifications KES-92651.

### 2-3. Test Program

For details on the starting method etc., refer to the Test Program Specifications KES-92651.

### 2-4. Jigs

The altered jigs and cable circuit diagram are shown from Page 47 of the Test Program Specifications KES-92651.

## 3. Inspection

### 3-1. Inspection with Test Program

· Inspect based on the Test Program Specifications KES-92651.

### 3-2. Jitter Measurement

· Connect the jitter meter to the WORD CLOCK OUT terminal.

· Set the function generator to 48 kHz and 44.1 kHz, connect to WORD CLOCK IN, and measure the jitter with the jitter meter.

| | Range of tolerance |
|---|---|
| 48 kHz | 6 ns max. |
| 44.1 kHz | 5 ns max. |

### 3-3. Fan Operation Check

· Check that the fan rotates while the power is on.

### 3-4. Sound

· For the connections and settings, refer to the Test Program Specifications.

**(1) Fs = 51.12 kHz (48 kHz + 6.5 %)**

· Set the function generator to 51.12 kHz.

· Test listen for 30 seconds and verify that there is no noise.

**(2) Fs = 39.69 kHz (44.1 kHz -10 %)**

· Set the function generator to 39.69 kHz.

· Test listen for 30 seconds and verify that there is no noise.

## 4. Factory Settings

· Rear panel.

WORD CLOCK IN 75 Ω: ON

# TEST PROGRAM

## A. Preparations for Inspection

This equipment requires firmware. When there are changes to the manufacturing processes and program for this equipment, it is necessary to write the new firmware to FlashRom from a PC. The software used and firmware used and their version numbers and concrete details of the writing method are shown below.

### •PM1DLOAD installation

First, it is necessary to install in the PC the dedicated software for writing the firmware. For the installation method, refer to the CS1D Test Program Specifications.

| | |
|---|---|
| Software used: | PM1DLOAD within PM1D system software |
| Version used: | PM1D system software component files with the version number listed on the cover sheet. (Managed with the already drawn CD-R assembly drawing (3JL-XY714A0.) |

### •Writing the firmware

The sheets that require firmware downloading are CIB (the 2CPU portion of E_TUC/E_HIF), EMB (the 2CPU portion of EMU/UIF), PDB, GDB, IDB (the 2CPU portion of DSP1D-EX), and EDB.
Below is the firmware used. Detailed procedures are on the following pages.

| | |
|---|---|
| Firmware used: | DSP1D firmware in PM1D system software |
| Version used: | PM1D system software component files with the version number listed on the cover sheet. (Managed with the already drawn CD-R assembly drawing (3JL-XY714A0.) |

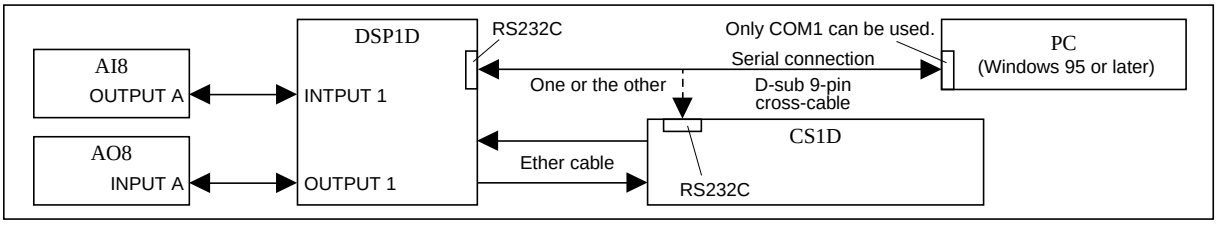
* If PM1DLOAD has been installed according to the instructions in the CS1D Test Program Specifications, the version for the firmware above is taken care of and there is no need to worry about it.

| | Firmware name | Sheet name | Connection number for writing firmware independently |
|---|---|---|---|
| **1** | EMU | EMB | CN104 |
| **2** | E_TCU | CIB | CN105 |
| **3** | E_HIF | | CN107 |
| **4** | UIF | EMB | CN105 |
| **5** | PDB | PDB | CN100 |
| **6** | GDB | GDB | CN100 |
| **7** | IDB1 | IDB (1st sheet) | CN100 |
| **8** | IDB2 | IDB (2nd sheet) | CN100 |
| **9** | EDB | EDB | CN100 |

"Firmware" and "subject sheet and subject connector" correspondence table

### •Method for writing firmware using the CS1D or DSP1D RS232C port

* It is possible to write the CPU firmware from the PC via the RS232C port. This is the method normally used.




1. Install and set PM1DLOAD with the method given in the CS1D Test Program Specifications.
2. Connect as in the figure above. Do not connect any other signal lines. However, to write firmware just to this equipment for a manufacturing process with this equipment, the only configuration required is DSP1D and the PC.
3. Write the firmware to all the units listed in the CS1D Test Program Specifications. You can check the status of the LEDs on each sheet. After the firmware has been written, check that the versions for all the units are the desired versions.

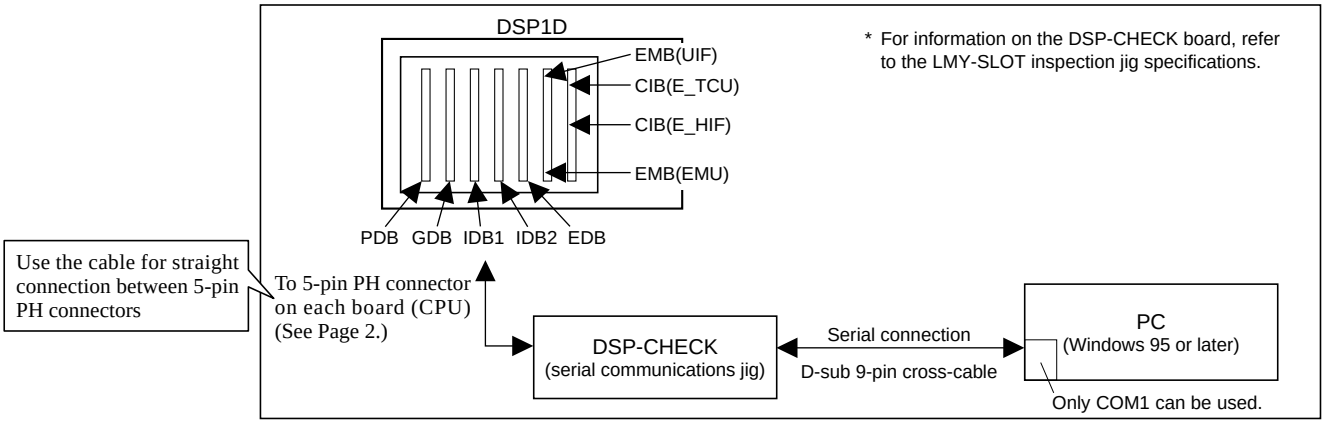
| For PDB, GDB, IDB1, IDB2, and EDB | |
|---|---|
| MONI-4 flashing | Program not yet written |
| MONI-4 lit up | Program writing complete<br>Program writing enabled |
| LED other than MONI-4 flashing or lit up | Program writing complete<br>Program writing inhibited |
| All LEDs out | Board defect possible |

| For CIB, EMB | |
|---|---|
| LED flashing | Program not yet written |
| LED lit up | Program writing complete<br>Ready for program writing |
| LED off | Program writing complete<br>Not ready for program writing |

Corresponding LEDs { CIB (E_TCU: LD101, E_HIF: LD102)
EMB (EMU: LD101, UIF: LD102)

**•Method for writing firmware directly to each sheet**

* When there is some kind of problem and the firmware can not be written with the method on the previous page, use the method below.




**1.** Install and set PM1DLOAD with the method given in the CS1D Test Program Specifications.
**2.** Remove the DSP1D front panel.
**3.** Remove all the CPU boards except the one on which you want to write PDB. (When writing to PDB, leave only that board.)
**4.** Connect the D-sub 9-pin serial cables (cross) and DSP-CHECK board between the 5-pin connector for the target board and the PC. At this time, do not connect other signal lines.

• For PDB, GDB, IDB1, IDB2, and EDB

**5.** Short Pin 1 of the target CPU directly to ground.
**6.** With the connections still as in 4., switch on the power for the DSP1D. If the LED darkens momentarily, you can remove the short.
**7.** Check that the LED on the board is lit or flashing, indicating that the system is ready for writing. (See the previous page.)
**8.** After starting PM1DLOAD, select CardDirect with MODE SELECT, then press OK.
**9.** Press the Update button on the DSP1D.
**10.** Select the desired firmware, then press the Write button. (See Page 45.)
**11.** After writing ends, end PM1DLOAD.
**12.** Switch off DSP1D. Remove the PH connector, then switch the power for DSP1D on again and check that it starts up normally.

• For EMB, CIB

**5.** Switch on the power for the DSP1D.
**6.** Check that the LED on the board is lit or flashing, indicating that the system is ready for writing. (See the previous page.)
**7.** After starting PM1DLOAD, select CardDirect with MODE SELECT, then press OK.
**8.** Press the Update button on the DSP1D.
**9.** Select the desired firmware, then press the Write button. (See Page 45.)
**10.** After writing ends, end PM1DLOAD.
**11.** Switch off DSP1D. Remove the PH connector, then switch the power for DSP1D on again and check that it starts up normally.

**•PM1D inspection PC software preparation**

Inspection with this device uses special PC software for inspection.
The version of the software used is shown below.

| | |
|---|---|
| Firmware used: | PM1D inspection PC software in PM1D system software |
| Version used: | PM1D system software component files with the version number listed on the cover sheet. (Managed with the already drawn CD-R assembly drawing (3JL-XY714A0.) |

* The operating systems supported are Windows 95/98.
* USB inspection is only supported in Windows 98. (Windows 98 Second Edition is not supported yet.)

For details of the preparation method and execution method, refer to the CS1D Test Program Specifications.
Refer to version.txt in the same directory as the firmware on Page 2 and input the version character string exactly as given there.
(For details on the input positions, refer to the "PM1D Inspection PC Software Summary" given later in this document.)

**•Installing the USB driver for inspection**

This equipment has a USB terminal. Therefore, it is necessary to install the USB driver for inspection in the inspection PC. The files used are included in the above PM1D inspection PC software, so install with the following procedure.

1. For the PM1D inspection PC software, start 16. DSP1D-JK6, LED2 Test.
2. When the pop-up box for connecting the USB cable is displayed, connect the USB cable.
3. After a short while, the system asks you to specify the driver. Specify the directory containing the PM1D inspection PC software.
4. The installation proceeds as indicated by the OS.
5. After installation is complete, press the OK button on the pop-up box that came up in 2.
6. If inspection is OK, the installation has completed normally.

* The only operating system supported is Windows98. The USB driver can not be used with Windows 98 Second Edition.
* The USB port is only activated in the state in 2. Beware. If you insert the USB cable in any other state, it is not correctly recognized by the PCS1De and the wrong driver is installed.
* Once the driver has been installed, the above procedure is not necessary for USB tests.
* This driver is only for inspection. It does not add the DSP1D USB function.
* The CS1D inspection USB driver must be installed separately.

## B. Inspection Method

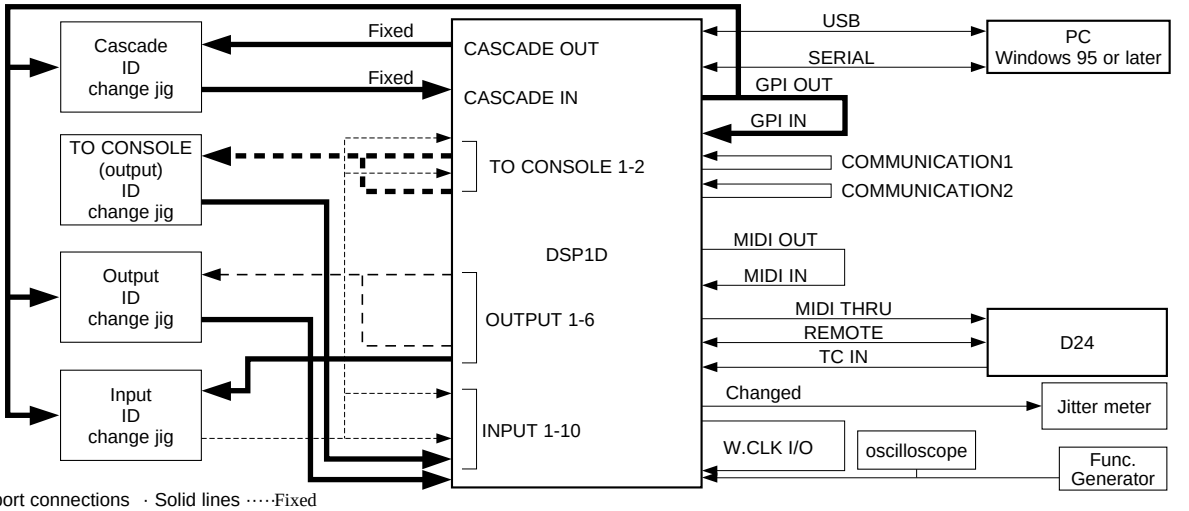
The inspection items are given below. Except for 17., these items are inspected using the PM1D inspection PC software. For details on each item, see from Page 51 on.

| No. | Items | |
|---|---|---|
| 1 | CIB Test | 1-1. TCU<br>1-2. HIF<br>1-3. CIF |
| 2 | EMB Test | 2-1. EMU<br>2-2. UIF |
| 3 | IFC Test | |
| 4 | PDB Test | 4-1. CPU<br>4-2. DSP6<br>4-3. DSP5 |
| 5 | GDB Test | 5-1. CPU<br>5-2. DSP6<br>5-3. DSP5 |
| 6 | IDB1 Test | 6-1. CPU<br>6-2. DSP6<br>6-3. DSP5 |
| 7 | IDB2 Test | 7-1. CPU<br>7-2. DSP6<br>7-3. DSP5 |
| 8 | EDB Test | 8-1. CPU<br>8-2. DSP6 |

| No. | Items | |
|---|---|---|
| 9 | Connection test | 9-1. PDB<br>9-2. GDB<br>9-3. IDB1<br>9-4. IDB2<br>9-5. EDB |
| 10 | JK1 (INPUT x) Test | 10-1. INPUT 1<br>:<br>10-10. INPUT 10 |
| 11 | JK4 (TO CONSOLE x) INPUT Test | 11-1. TO CONSOLE 1<br>11-2. TO CONSOLE 2 |
| 12 | JK2 (OUTPUT x) Test | 12-1. OUTPUT 1<br>:<br>12-6. OUTPUT 6 |
| 13 | JK4(TO CONSOLE x) OUTPUT Test | 13-1. TO CONSOLE 1<br>13-2. TO CONSOLE 2 |
| 14 | JK3 (CASCADE) Test | |
| 15 | JK5 Test | |
| 16 | JK6 , LED2 Test | |
| 17 | All-group sound inspection<br>(Inspects using DSP1D sound inspection data. See Page 49.) | |

## C. Inspection Using PM1D Inspection PC Software

Except for the all-group sound test, the inspections use the PM1D inspection PC software to control the DSP1D and the inspection is carried out autonomously. The inspection configuration diagram is as follows.




68-pin port connections · Solid lines ·····Fixed
· Dotted lines···Changed

For details on inspecting with this software, see from Page 51 on.
Locations with instructions for changes have instructions for that inspection item in the PC software, so change the connections according to the instructions.
(* Even if the system is the DSP1D not the DSP1D-EX, inspect with IDB2 inserted for the bus check.)

### D24 setting method

For time code output, insert an MO disc (song data or the like) that can idle as long as possible. Also, switch On MMC Receive on the Utility menu and set TC Select to Serial IN on the Setup menu.

### W. CLK connection method

In the 16 JK6 inspection, it is necessary to change the BNC cable. The connection method is as follows.

| JK6-W.CLK inspection sub-item | Connection method |
|---|---|
| IN 48 kHz + 6 %<br>IN 44.1kHz - 10 % | W.CLK In ····· Connect the function generator and output the clocks.<br>W.CLK Out ····· No need to connect |
| Jitter 48 kHz<br>Jitter 44.1 kHz | W.CLK In ····· Connect the function generator and output the clocks.<br>W.CLK Out ····· Connect the jitter meter and measure. |
| IN/OUT | Loopback connection between W.CLK Out and W.CLK In |

### 68-pin port connection method table

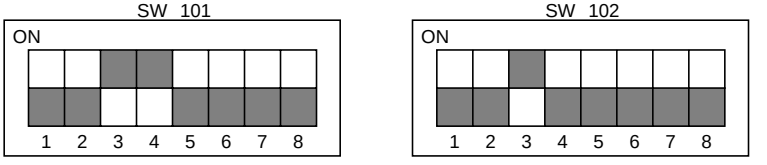
* Since the input and output functions are inspected separately for TO CONSOLE, there are two connection methods.

| Inspection item | Necessary jig | ID change jig connection method | |
|---|---|---|---|
| | | From left side (CN103) | From right side (CN102) |
| 10. INPUT 1-10 | Input ID change jig | To INPUT 1-10 | To OUTPUT x |
| 11. TO CONSOLE (INPUT) 1-2 | | To Console 1-2 | |
| 12. OUTPUT 1-6 | Output ID change jig | To INPUT x | To OUTPUT 1-6 |
| 13. TO CONSOLE (OUTPUT) 1-2 | Altered ID change jig just for TO CONSOLE (OUTPUT) | Connected TO CONSOLE 1-2 and INPUT; no polarity. | |
| 14. CASCADE IN/OUT | Cascade ID change jig | To CASCADE IN | To CASCADE OUT |

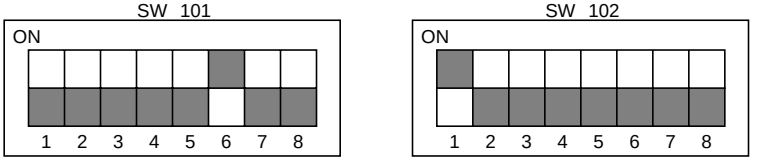
### ID change jig DIP switch settings

* There are three special 68-pin port ID change jigs (for INPUT, OUTPUT, and CASCADE) but these are the same jig with just the DIP switch settings changed. In other words, you can work with just one ID change inspection jig by changing the DIP switch settings appropriately. For information on the ID change jig, refer to the LMY-SLOT inspection jig specifications.

Input ID change jig
[INPUT 1-10]
[TO CONSOLE (INPUT)]



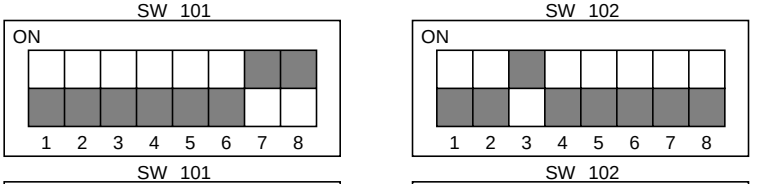

Output ID change jig
[OUTPUT 1-6]



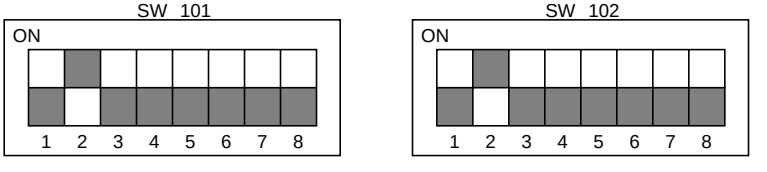

TO CONSOLE (OUTPUT) ID change jig
[TO CONSOLE (OUTPUT)]

The ID is not inspected at TO CONSOLE (OUTPUT), so the DIP switch settings do not matter. Connect the altered ID change jig just for TO CONSOLE (OUTPUT). (For details on the alteration, refer to the DSIP Overall Inspection Specifications.)

Cascade ID change jig
[for CASCADE IN check]



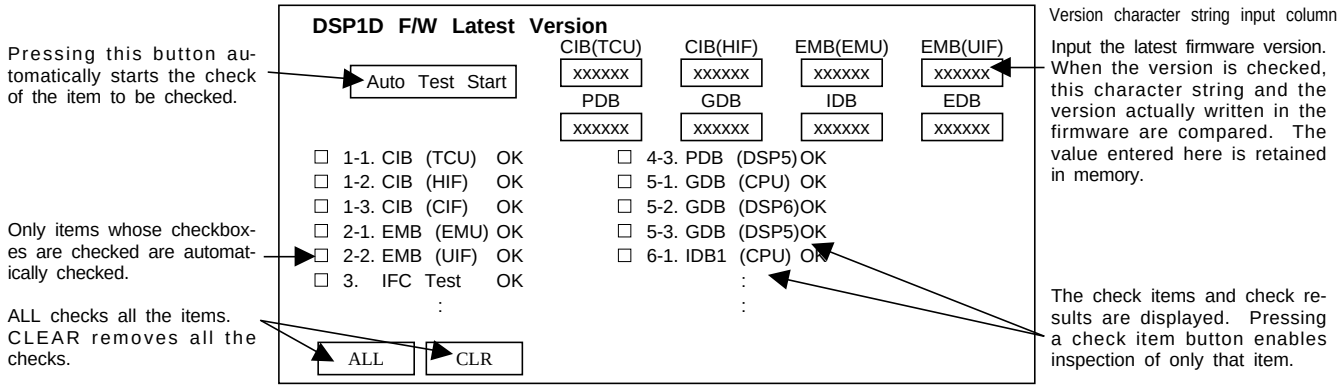

Cascade ID change jig
[for CASCADE OUT check]



**PM1D inspection PC software summary**

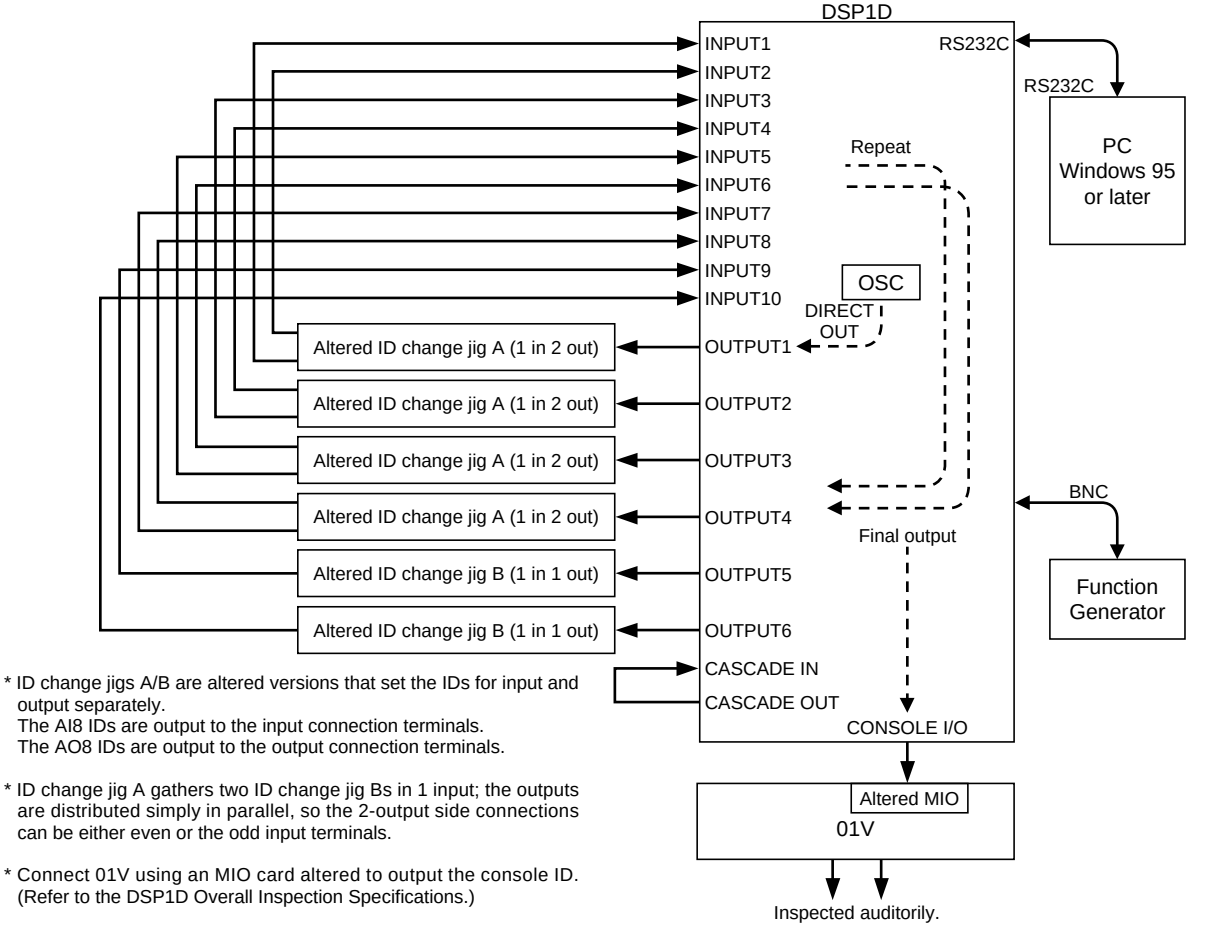
Except for Item 17., the PM1D is inspected using PC inspection software. This inspection software is common for AI8/AO8/DSP1D/CS1D.
For details on the basic operation methods, menu screen specifications, etc., refer to the CS1D Test Program Specifications.

The DSP test menus are shown below.
Before the inspection, the latest version of each piece of DSP1D software must be input. (This is necessary for the version check.)
For the version character string to be input, refer to version.txt in the same directory as the DSP1D firmware.
The following pages give details on each check item and how the PC software handles it.




## D. All-Group Sound Inspection

After all the inspections were carried out with the PM1D inspection PC software, the sound inspection is carried out.
After making the connections as in the diagram below, inspect with the procedure given from the next page on. Note that the altered ID change jigs A/B are separate from the dedicated TO CONSOLE (OUTPUT) altered ID change jig. (If multiple ID change jigs can be not be made available, substitute with the method given later in this document.)




* ID change jigs A/B are altered versions that set the IDs for input and output separately.
  The AI8 IDs are output to the input connection terminals.
  The AO8 IDs are output to the output connection terminals.

* ID change jig A gathers two ID change jig Bs in 1 input; the outputs are distributed simply in parallel, so the 2-output side connections can be either even or the odd input terminals.

* Connect 01V using an MIO card altered to output the console ID. (Refer to the DSP1D Overall Inspection Specifications.)

**• Method using six altered ID change jigs (This is the method normally used.)**

1. Connect according to the connection diagram. Supply a 48kHz clock from the function generator.
2. Execute the PM1D Manager for Windows from the PC. From Utility - LOAD/SAVE, execute the DSP1D sound and LOAD the inspection data. (For the version, installation method, usage method, etc., see below.)

| | |
|---|---|
| Software used: | PM1D Manager for Windows within PM1D system software |
| Version used: | PM1D system software component files with the version number listed on the cover sheet. (Managed with the already drawn CD-R assembly drawing (3JL-XY714A0.) |

* The installation method is the same. Refer to install.txt in the PM1D system software.

| | |
|---|---|
| Data used: | DSP1D sound inspection software within PM1D system software |
| Version used: | PM1D system software component files with the version number listed on the cover sheet. (Managed with the already drawn CD-R assembly drawing (3JL-XY714A0.) |

* Start the installed PM1D Manager for Windows, then read with UTILITY - LOAD/SAVE.

3. Set ENGINE A to W.CLOCK IN with SYS/W.CLOCK - WORD CLOCK.
4. Set OSC OUT to 1AO8:1-1 with MON/CUE - OSCILLATOR, set ON. OSC to IN, then adjust the level.
5. Recall SCENE 00.1: SOUND THRU1 with SCENE - MEMORY.
6. Set the switch for the altered MIO connected to 01V to ST.
7. Check the audio through 01V.
8. Set the switch for the altered MIO connected to 01V to ST.
9. Check the audio through 01V.

**• Method using only one altered ID change jig**

1. Connect according to the connection diagram. Supply a 48kHz clock from the function generator.
2. Connect an altered ID change jig to INPUT 1 and 2 and OUTPUT 1.
3. Execute the PM1D Manager for Windows from the PC. From Utility - LOAD/SAVE, execute the DSP1D sound and LOAD the inspection data. (For the version, installation method, usage method, etc., see the previous page.)
4. Set ENGINE A to W.CLOCK IN with SYS/W.CLOCK - WORD CLOCK.
5. Set OSC OUT to 1AO8:1-1 with MON/CUE - OSCILLATOR, set ON. OSC to IN, then adjust the level.
6. Recall SCENE 00.1: SOUND THRU1 with SCENE - MEMORY.

*1 {
7. Set the switch for the altered MIO to ST and check the audio through 01V.
8. Set the switch for the altered MIO to MON and check the audio through 01V.

9. Recall SCENE 00.2: SOUND THRU2 with SCENE - MEMORY. Check that the audio goes off.
10. Change the input side connections only to INPUT 3 and 4.
11. Repeat *1.
12. Recall SCENE 00.3: SOUND THRU3 with SCENE - MEMORY. Check that the audio goes off.
13. Change the input side connections only to INPUT 5 and 6.
14. Repeat *1.
15. Recall SCENE 00.4: SOUND THRU4 with SCENE - MEMORY. Check that the audio goes off.
16. Change the input side connections only to INPUT 7 and 8.
17. Repeat *1.
18. Recall SCENE 00.5: SOUND THRU5 with SCENE - MEMORY. Check that the audio goes off.
19. Change the input side connections only to INPUT 9 and 10.
20. Repeat *1.
21. Set OSC OUT to 2AO8:1-1.
22. Change the output side connection only to OUTPUT 2. (The INPUT remains 9 and 10 and the scene 00.5.)
23. Repeat *1.
24. Set OSC OUT to 3AO8:1-1.
25. Change the output side connection only to OUTPUT 3.
26. Repeat *1.
27. Set OSC OUT to 4AO8:1-1.
28. Change the output side connection only to OUTPUT 4.
29. Repeat *1.
30. Set OSC OUT to 5AO8:1-1.
31. Change the output side connection only to OUTPUT 5.
32. Repeat *1.

**33.** Set OSC OUT to 6AO8:1-1.
**34.** Change the output side connection only to OUTPUT 3.
**35.** Repeat *1.

## 1. DSP1D-CIB Test

This test checks the DSP1D-CIB. It checks the following items. Those items for which there are figures display the results in binary. Detailed screen output specifications are given on the following pages.
The details for 1-2. are omitted because they are the same as for 1-1.

* For the DPM (dual port RAM) item, EM BUS <-> TC BUS R etc. is written. This indicates which of the DPM buses is inspected. For example, for EM BUS <-> TC BUS R, this indicates the check of the TC BUS side seen from the DPM (right side for the DPS BUS <-> CM BUS notation).

**1-1. DSP1D-CIB (TCU-IC129) Test**

This test checks around the CIB TCU.

Check item
- ☐ ID TCU [11h]
- ☐ RAM
  - • Data Bus 16bit(15-0)
  - • Address Bus 20bit(19-0)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • EM BUS<->TC BUS R

**1-2. DSP1D-CIB (TCU-IC129) Test**

This test checks around the CIB HIF.

Check item
- ☐ ID TCU [12h]
- ☐ RAM
  - • Data Bus 16bit(15-0)
  - • Address Bus 20bit(19-0)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • HI BUS<->EM BUS L

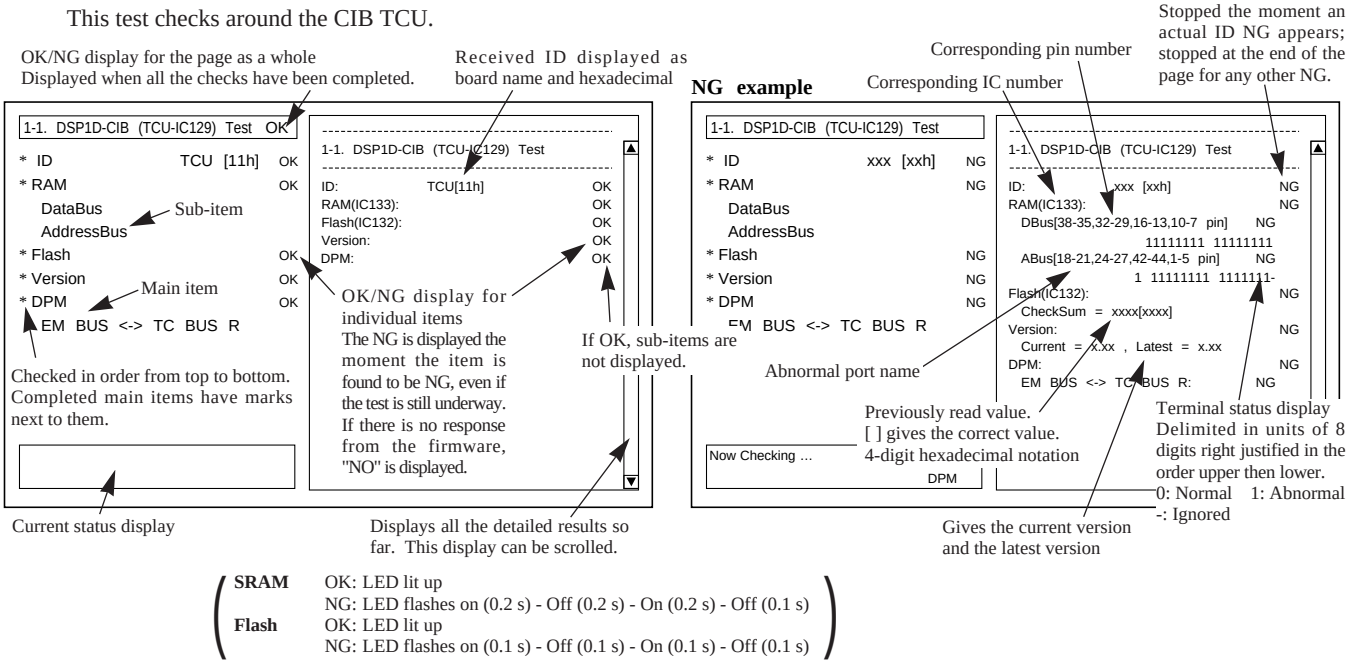
**1-3. DSP1D-CIB (ETC)Test**

This test makes other checks of the CIB.

Check item
- ☐ FPGA HIF [02h]
- ☐ DPM
  - • EMU<->CONS L
- ☐ FIFO
- ☐ TC IC

## 1-1. DSP1D-CIB (TCU) Test

This test checks around the CIB TCU.

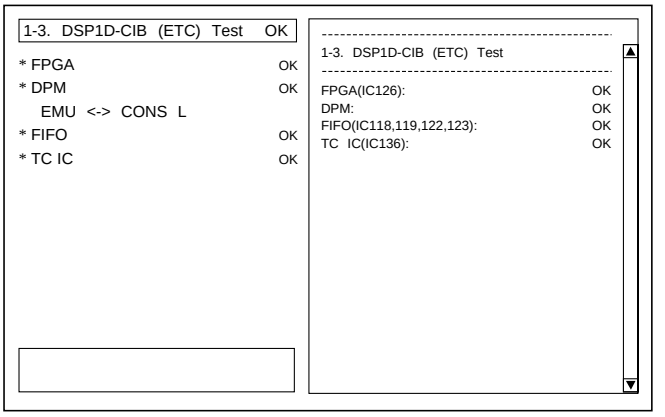



**SRAM** OK: LED lit up
NG: LED flashes on (0.2 s) - Off (0.2 s) - On (0.2 s) - Off (0.1 s)

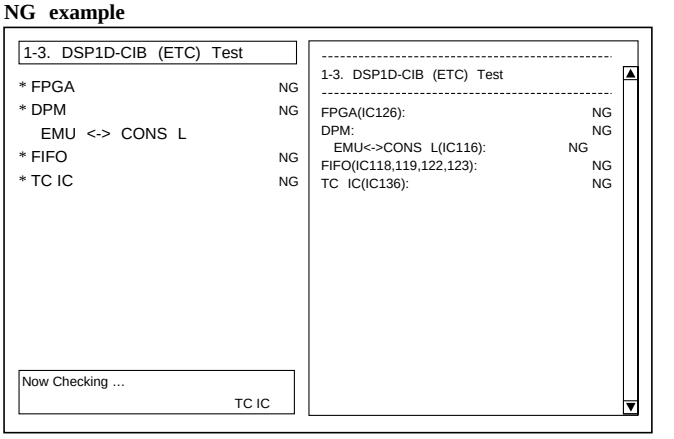
**Flash** OK: LED lit up
NG: LED flashes on (0.1 s) - Off (0.1 s) - On (0.1 s) - Off (0.1 s)

## 1-3. DSP1D-CIB (ETC) Test

This test checks around the CIB ETC.




**NG example**



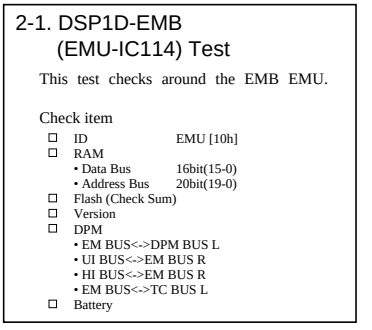

**SRAM** OK: LED lit up
NG: LED flashes on (0.2 s) - Off (0.2 s) - On (0.2 s) - Off (0.1 s)

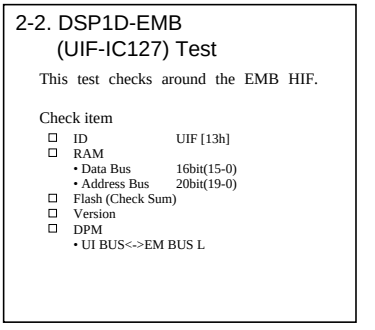
**Flash** OK: LED lit up
NG: LED flashes on (0.1 s) - Off (0.1 s) - On (0.1 s) - Off (0.1 s)

## 2. DSP1D-EMB Test

This test checks the EMB. It checks the following items. Those items for which there are figures display the results in binary. Detailed screen output specifications are given on the following pages.

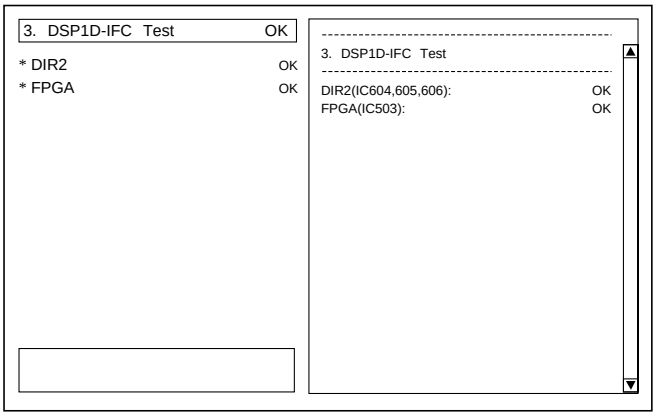
The battery check item is only for 2-1. Here the voltage is checked and if it is within the correct range, OK is displayed. If it is NG, how far it deviates from the correct value is displayed.



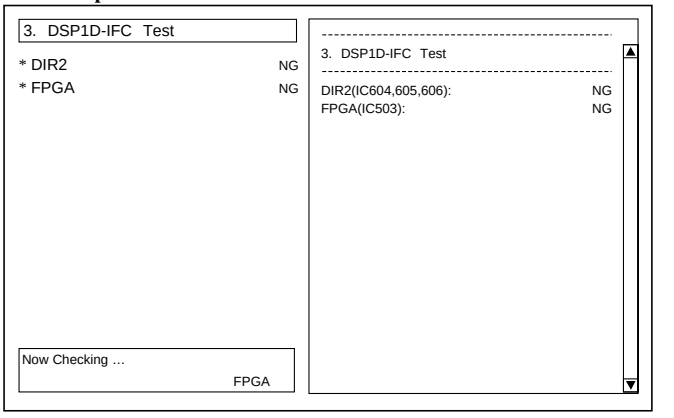




## 3. DSP1D-IFC (TCU) Test

This test checks the IFC board.




**NG example**




## 4. DSP1D-PDB Test

This test checks the DSP1D-PDB. It checks the following items. Those items for which there are figures display the results in binary. Detailed screen output specifications are given on the following pages.

DSP6 total count ···· 9
DSP5 total count ···· 11

4-1. DSP1D-PDB (CPU-IC101) Test

This test checks around the PDB CPU.

Check item
- ☐ ID PDB [14h]
- ☐ RAM
  - • Data Bus 16bit(15-0)
  - • Address Bus 16bit(16-1)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • Data Bus 16bit(15-0)
  - • Address Bus 15bit(15-1)

4-2. DSP1D-PDB (DSP6) Test

This test checks around PDB DSP6.

Check item
- ☐ Chip Select
- ☐ DSP6 <--> CPU
  - • Data Bus 16bit(15-0)
  - • Address Bus 7bit( 7-1)
- ☐ DSP6 <--> DRAM
  - • Data Bus 32bit(31-0)
  - • Address Bus 10bit( 9-0)
- ☐ DSP6 -> DSP6
  - • Serial I/O

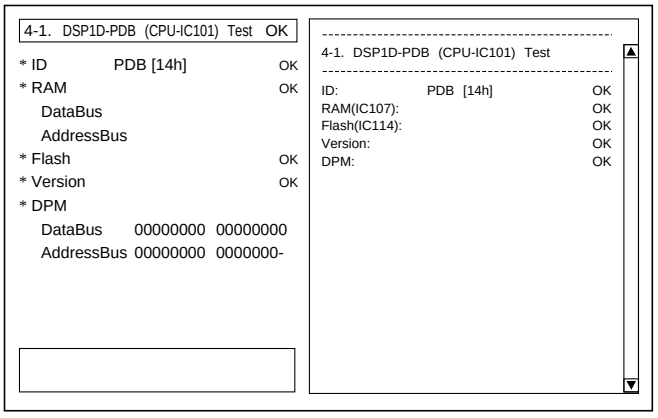
4-3. DSP1D-PDB (DSP5) Test

This test checks around PDB DSP5.

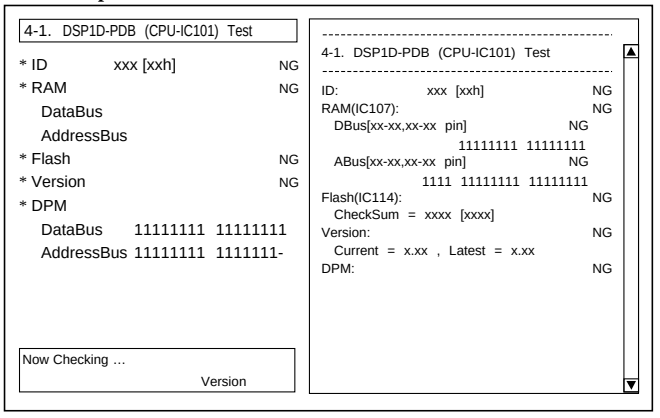
Check item
- ☐ Chip Select
- ☐ DSP5 <--> CPU
  - • Data Bus 16bit(15-0)
  - • Address Bus
- ☐ DSP6 -> DSP5
  - • Serial I/O
- ☐ DSP5 -> DSP6
  - • Serial I/O
- ☐ DPM
  - • Serial I/O
  - • ParallelI/O 32bit(31-0)

## 4-1. DSP1D-PDB (CPU-IC101) Test

This test checks around the PDB CPU.




**NG example**




( **SRAM** OK: LED lit up
NG: LED flashes on (0.2 s) - Off (0.2 s) - On (0.2 s) - Off (0.1 s)
**Flash** OK: LED lit up
NG: LED flashes on (0.1 s) - Off (0.1 s) - On (0.1 s) - Off (0.1 s) )

## 4-2. DSP1D-PDB (DSP6) Test

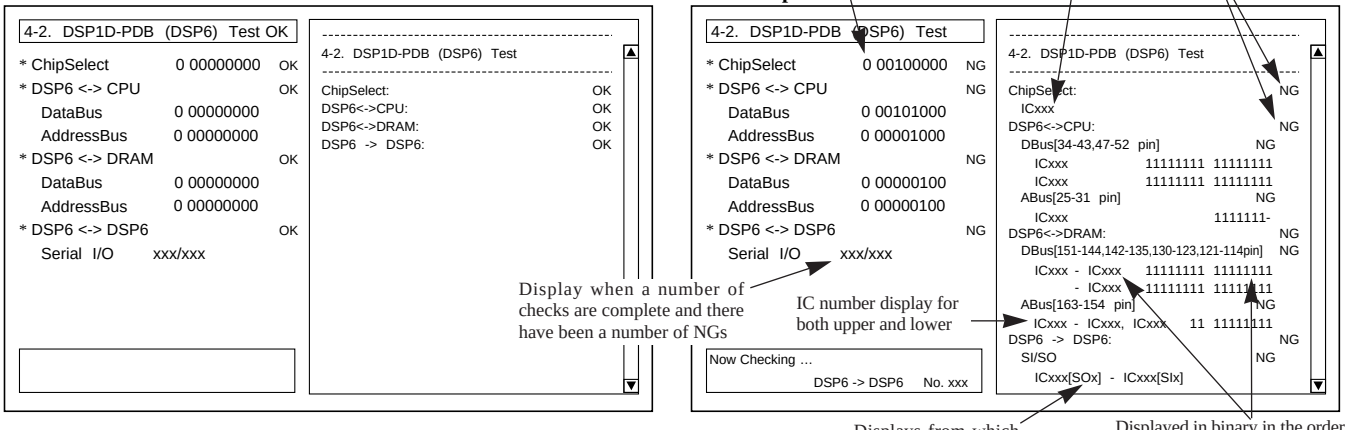
This test checks around PDB DSP6.

The DSP check results are displayed for each DSP. The DSPs are displayed in order from the right of the ChipSelect signals on the circuit diagram.
(Blank: Not yet checked; 0: Normal; 1: Abnormal; N: No response)

Stopped the moment an actual Chip Select or TxB NG appears; stopped at the end of the page for any other NG.

Gives the abnormal DSP IC number.

**NG example**




Display when a number of checks are complete and there have been a number of NGs

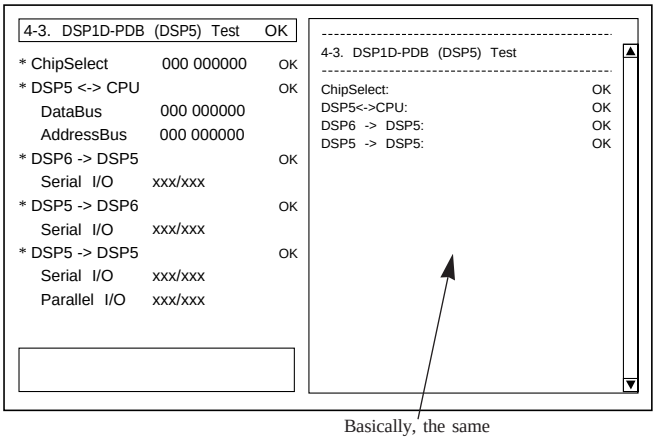
IC number display for both upper and lower

Displays from which SO to which SI is NG.

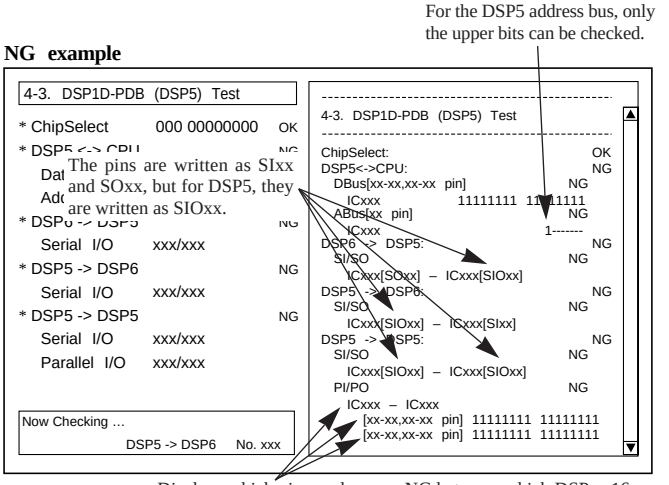
Displayed in binary in the order Upper: 16 bits, Lower: 16 bits
The corresponding DRAM IC number is also displayed.

## 4-3. DSP1D-PDB (DSP5) Test

This test checks around PDB DSP6.




**NG example**




## 5. DSP1D-GDB Test

This test checks the GDB. It checks the following items. The specifications are basically the same as for 4-1. through 4-3.

DSP6 total count ···· 13

DSP5 total count ···· 7

### 5-1. DSP1D-GDB (CPU-IC100) Test

This test checks around the GDB CPU.

Check item

- ☐ ID GDB [15h]
- ☐ RAM
  - • Data Bus 16bit(15-0)
  - • Address Bus 16bit(16-1)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • Data Bus 16bit(15-0)
  - • Address Bus 15bit(15-1)

### 5-2. DSP1D-GDB (DSP6) Test

This test checks around GDB DSP6.

Check item

- ☐ Chip Select
- ☐ DSP6 <-> CPU
  - • Data Bus 16bit(15-0)
  - • Address Bus 7bit( 7-1)
- ☐ DSP6 <-> DRAM
  - • Data Bus 32bit(31-0)
  - • Address Bus 10bit( 9-0)
- ☐ DSP6 -> DSP6
  - • Serial I/O

### 5-3. DSP1D-GDB (DSP5) Test

This test checks around GDB DSP5.

Check item

- ☐ Chip Select
- ☐ DSP5 <-> CPU
  - • Data Bus 16bit(15-0)
  - • Address Bus
- ☐ DSP6 -> DSP5
  - • Serial I/O
- ☐ DSP5 -> DSP6
  - • Serial I/O
- ☐ DSP5 -> DSP5
  - • Serial I/O
  - • Parallel I/O 32bit(31-0)

## 6. DSP1D-IDB1 Test

This test checks the IDB1. It checks the following items. The specifications are basically the same as for 4-1. through 4-3.

DSP6 total count ···· 16

DSP5 total count ···· 8

### 6-1. DSP1D-IDB1 (CPU-IC100) Test

This test checks around the IDB1 CPU.

Check item

- ☐ ID IDB1 [16h]
- ☐ RAM
  - • Data Bus 16bit(15-0)
  - • Address Bus 16bit(16-1)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • Data Bus 16bit(15-0)
  - • Address Bus 15bit(15-1)

### 6-2. DSP1D-IDB1 (DSP6) Test

This test checks around IDB1 DSP6.

Check item

- ☐ Chip Select
- ☐ DSP6 <-> CPU
  - • Data Bus 16bit(15-0)
  - • Address Bus 7bit( 7-1)
- ☐ DSP6 <-> DRAM
  - • Data Bus 32bit(31-0)
  - • Address Bus 10bit( 9-0)
- ☐ DSP6 -> DSP6
  - • Serial I/O

### 6-3. DSP1D-IDB1 (DSP5) Test

This test checks around IDB1 DSP5.

Check item

- ☐ Chip Select
- ☐ DSP5 <-> CPU
  - • Data Bus 16bit(15-0)
  - • Address Bus
- ☐ DSP6 -> DSP5
  - • Serial I/O
- ☐ DSP5 -> DSP5
  - • Serial I/O

## 7. DSP1D-IDB2 Test

This test checks the IDB2. It checks the following items. The specifications are basically the same as for 4-1. through 4-3.

DSP6 total count ···· 16

DSP5 total count ···· 8

### 7-1. DSP1D-IDB2 (CPU-IC100) Test

This test checks around the IDB2 CPU.

Check item

- ☐ ID — IDB2 [16h]
- ☐ RAM
  - • Data Bus — 16bit(15-0)
  - • Address Bus — 16bit(16-1)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • Data Bus — 16bit(15-0)
  - • Address Bus — 15bit(15-1)

### 7-2. DSP1D-IDB2 (DSP6) Test

This test checks around IDB2 DSP6.

Check item

- ☐ Chip Select
- ☐ DSP6 <-> CPU
  - • Data Bus — 16bit(15-0)
  - • Address Bus — 7bit( 7-1)
- ☐ DSP6 <-> DRAM
  - • Data Bus — 32bit(31-0)
  - • Address Bus — 10bit( 9-0)
- ☐ DSP6 -> DSP6
  - • Serial I/O

### 7-3. DSP1D-IDB2 (DSP5) Test

This test checks around IDB2 DSP5.

Check item

- ☐ Chip Select
- ☐ DSP5 <-> CPU
  - • Data Bus — 16bit(15-0)
  - • Address Bus
- ☐ DSP6 -> DSP5
  - • Serial I/O
- ☐ DSP5 -> DSP5
  - • Serial I/O

## 8. DSP1D-EDB Test

This test checks the EDB. It checks the following items. The specifications are basically the same as for 4-1. through 4-2.

DSP6 total count ···· 12

### 2-1. DSP1D-EMB (EMU-IC114) Test

This test checks around the EMB EMU.

Check item

- ☐ ID — EMU [10h]
- ☐ RAM
  - • Data Bus — 16bit(15-0)
  - • Address Bus — 20bit(19-0)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • EM BUS<->DPM BUS L
  - • UI BUS<->EM BUS R
  - • HI BUS<->EM BUS R
  - • EM BUS<->TC BUS L
- ☐ Battery

### 2-2. DSP1D-EMB (UIF-IC127) Test

This test checks around the EMB HIF.

Check item

- ☐ ID — UIF [13h]
- ☐ RAM
  - • Data Bus — 16bit(15-0)
  - • Address Bus — 20bit(19-0)
- ☐ Flash (Check Sum)
- ☐ Version
- ☐ DPM
  - • UI BUS<->EM BUS L

## 9. DSP1D Connection Test

This test checks the connections among the PDB, GDB, IDB1, IDB2, and EDB. It checks the following items. Detailed screen output specifications are given on the following pages.

* There are duplicate checks, but for checking just specific boards, these checks are not omitted.

### 9-1. DSP1D-Connection (PDB) Test

Checks the connections between the PDB and the other boards.

Check item

- ☐ PDB -> IDB1
- ☐ PDB -> IDB2
- ☐ PDB -> GDB
- ☐ PDB -> EDB
- ☐ IDB1 -> PDB
- ☐ IDB2 -> PDB
- ☐ GDB -> PDB
- ☐ EDB -> PDB

### 9-2. DSP1D-Connection (GDB) Test

Checks the connections between the GDB and the other boards.

Check item

- ☐ GDB -> PDB
- ☐ IDB1 -> GDB
- ☐ IDB2 -> GDB
- ☐ PDB -> GDB
- ☐ EDB -> GDB

### 9-3. DSP1D-Connection (IDB1) Test

Checks the connections between the IDB1 and the other boards.

Check item

- ☐ IDB1 -> GDB
- ☐ IDB1 -> PDB
- ☐ IDB1 -> IDB2
- ☐ PDB->IDB1

### 9-4. DSP1D-Connection (IDB2) Test

Checks the connections between the IDB2 and the other boards.

Check item

- ☐ IDB2 -> GDB
- ☐ IDB2 -> PDB
- ☐ IDB1 -> IDB2
- ☐ PDB->IDB2

### 9-5. DSP1D-Connection (EDB) Test

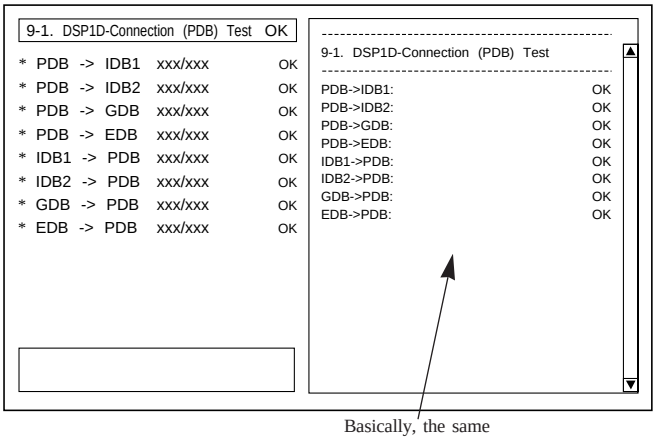
Checks the connections between the EDB and the other boards.

Check item

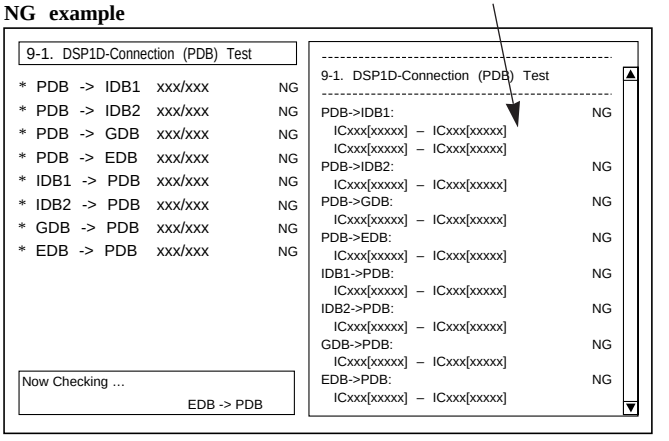
- ☐ EDB -> GDB
- ☐ EDB -> PDB
- ☐ PDB -> EDB

## 9-1. DSP1D-Connection (PDB) Test

Checks the connections between the PDB and the other boards.

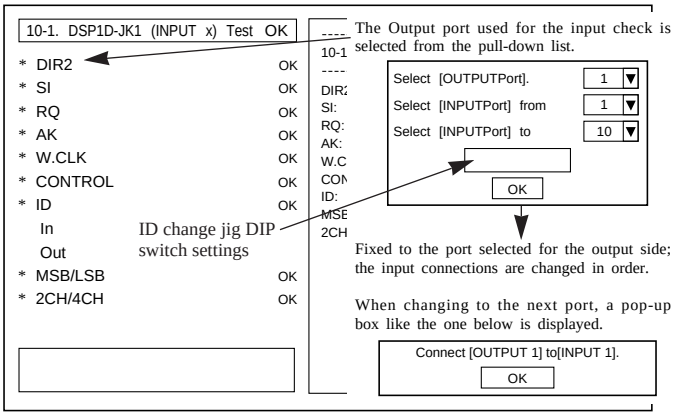



**NG example**

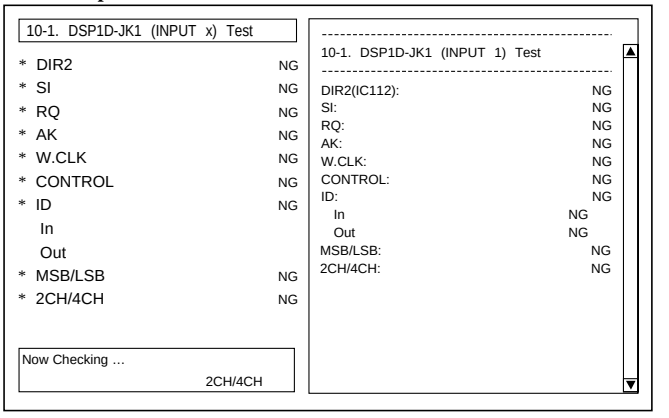



## 10. DSP1D-JK1 (INPUT x) TEST

This test checks the JK1 board with loopback connections. These items are repeated for just the specified range of Inputs 1-10. The input ID change jig is used for Items 10 and 11.

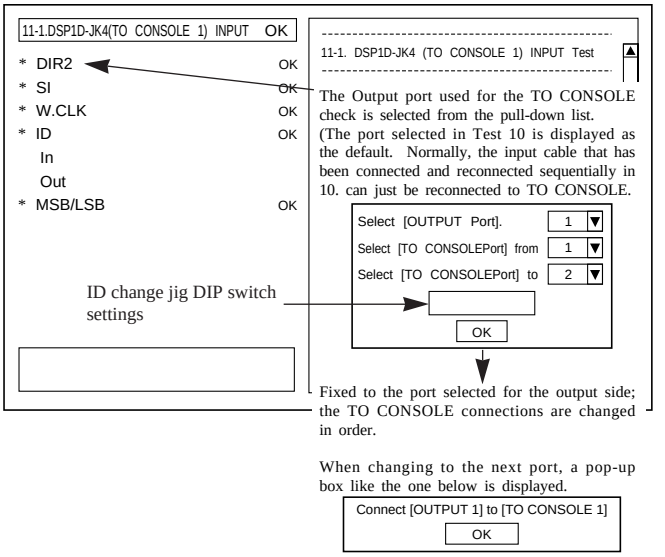



**NG example**

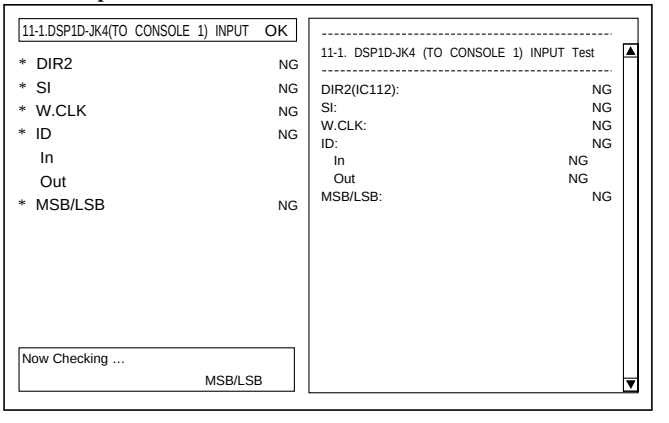



## 11. DSP1D-JK4 (TO CONSOLE x) Input Test

This test checks the JK4 port input direction communications. These items are repeated for the specified range of TO CONSOLE 1-2.

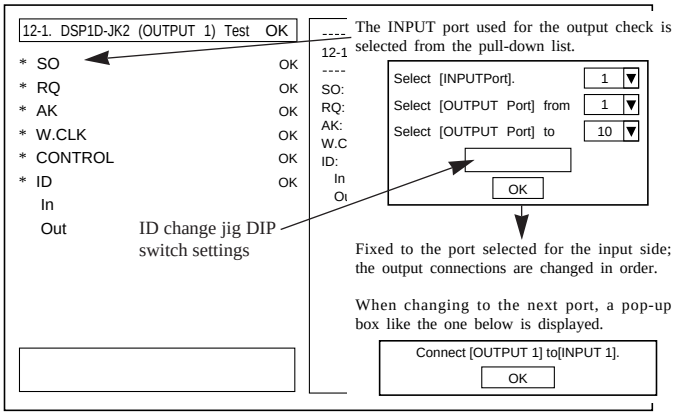



**NG example**

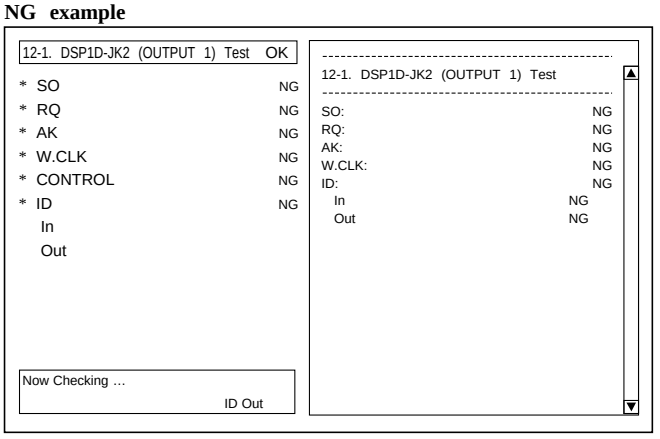


## 12. DSP1D-JK2 (OUTPUT x) Test

This test checks the JK2 port with loopback connections. These items are repeated only for INPUT1-10. The output ID change jig is used for Item 12.

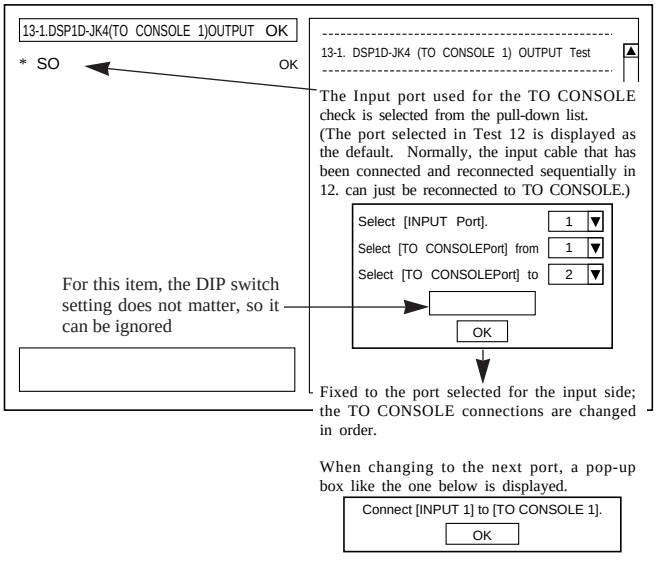



**NG example**

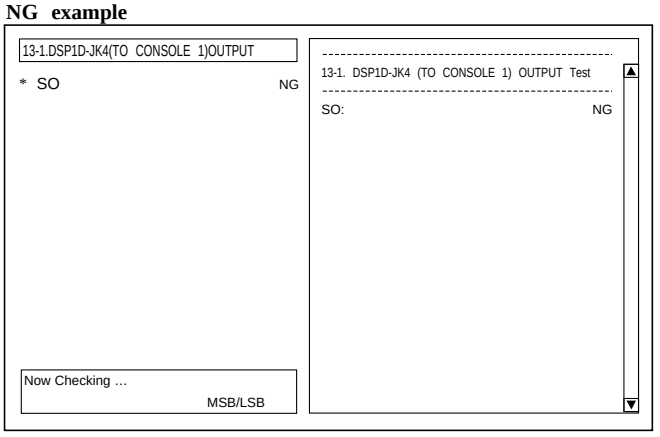



## 13. DSP1D-JK4 (TO CONSOLE x) Output Test

This test checks the JK4 port output direction communications. For this item, use either the altered TO CONSOLE (OUTPUT) ID change jig or the altered special cable.

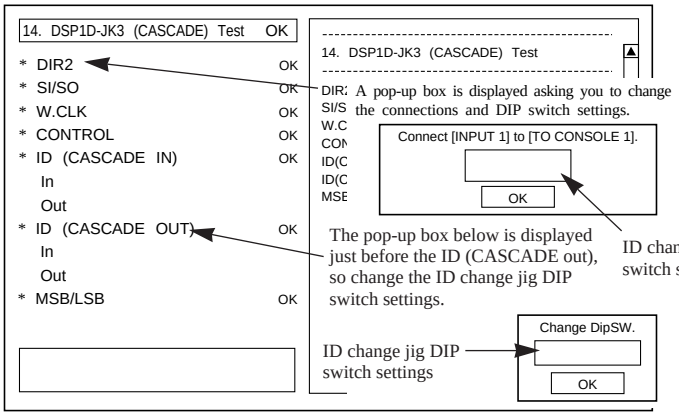



**NG example**

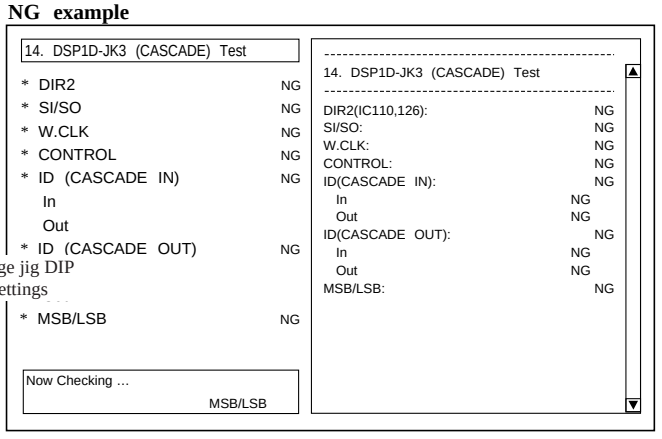



## 14. DSP1D-JK3 (CASCADE) Test

This test checks the JK3 port with loopback connections. For this test, use either the Cascade ID change jig.

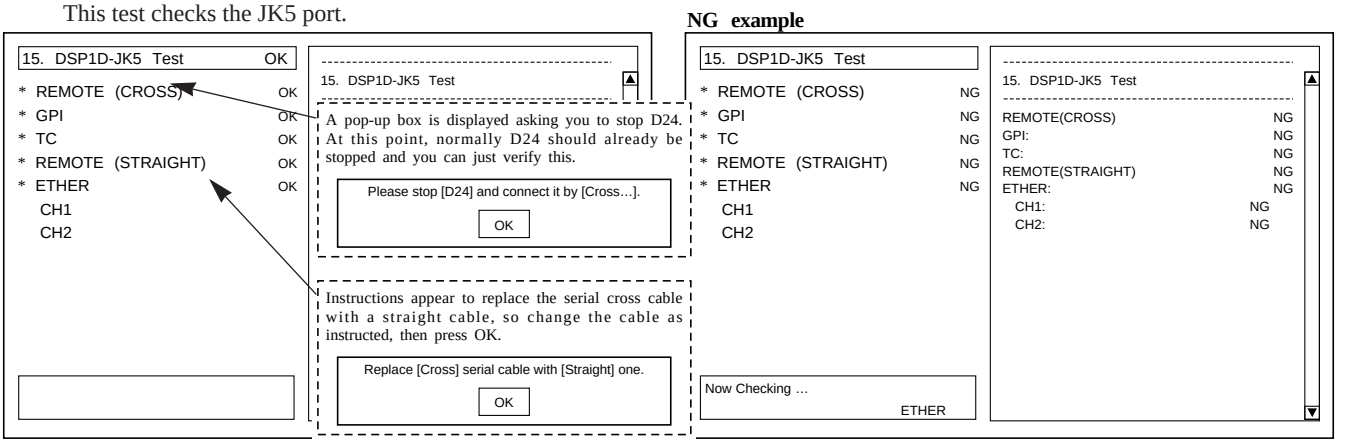



**NG example**



## 15. DSP1D-JK5 Test

This test checks the JK5 port.

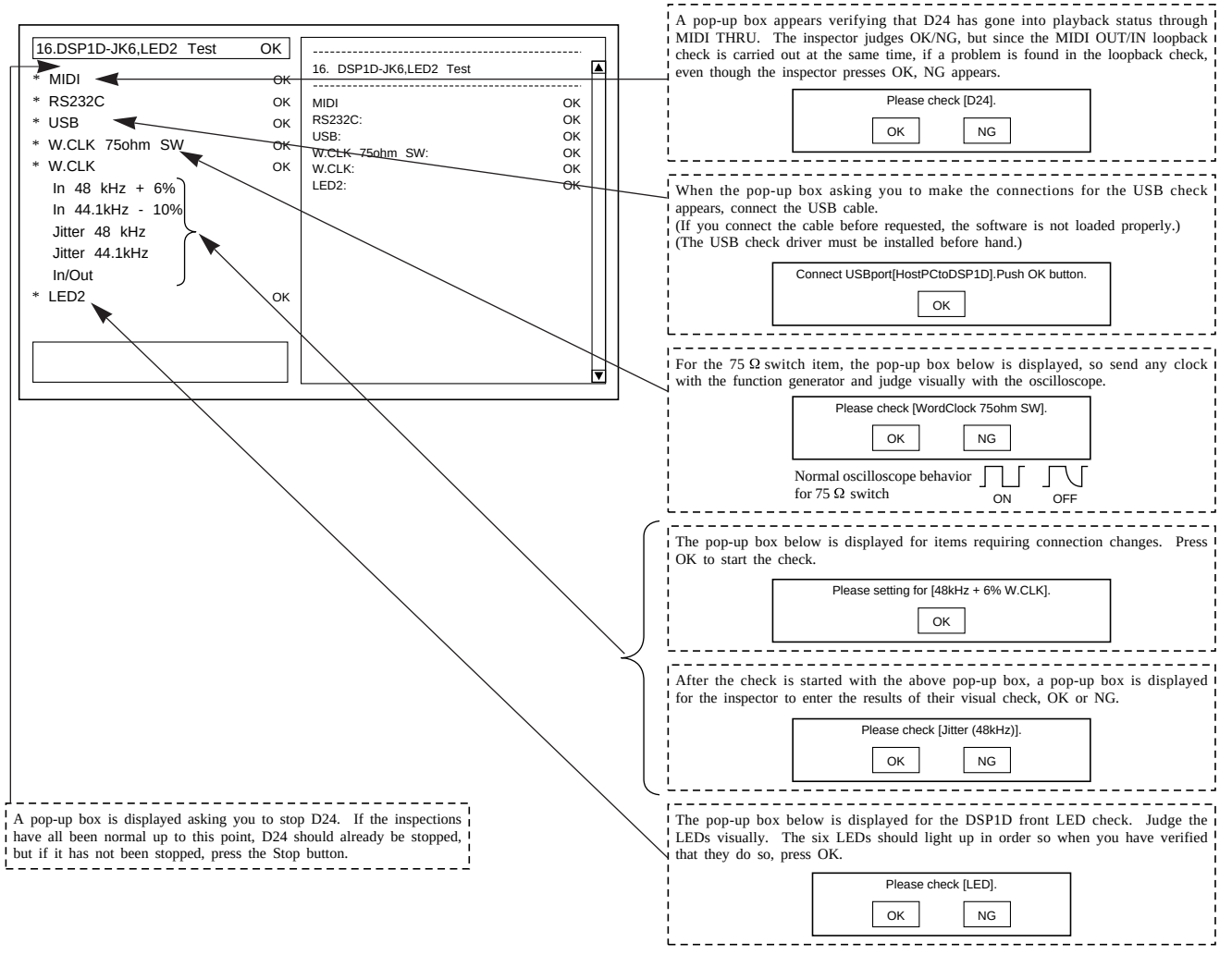



• Normal behavior for each inspection item

REMOTE (CROSS) ····· D24 playback (TC send)
TC ····· TC check from D24
REMOTE (STRAIGHT) ····· D24 stop

## 16. DSP1D-JK6 Test

This test checks the JK6 port and LED2. For details on how to change the connections, see Page 7.



# ■ ERROR MESSAGES

**• If both ENGINE ID A and B indicators are flash-ing:**

→ There is a malfunction in the internal board (PDB, GDB, IDB1/2, EDB, EMB, or CIB). Or the necessary board does not exist.

**• If either ENGINE ID A or B indicator is flashing:**

→ During the Mirror mode operation, the ENGINE ID indicator for the unused DSP1D/DSP1D-EX flashes, indicating that the unit is in standby mode.

→ If Indicator A is flashing, unit A is in standby mode. If Indicator B is flashing, unit B is in standby mode.

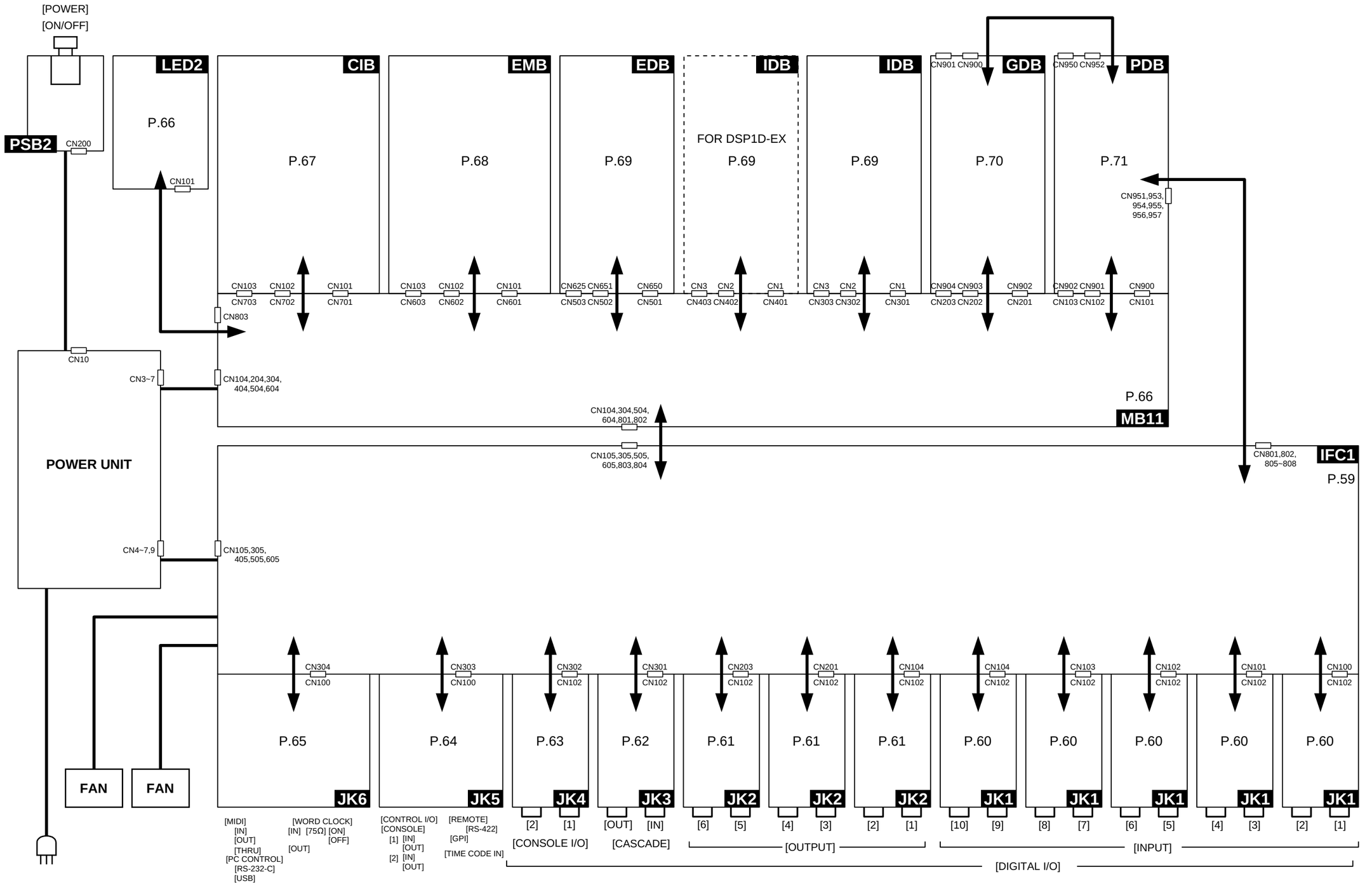
**• If the CONTROL I/O 1 indicator is flashing:**

→ Communication between the CS1D control surface and the DSP1D is not established.The CONSOLE 1, 2 IN OUT jacks or the PC CON-TROL port is not connected correctly.

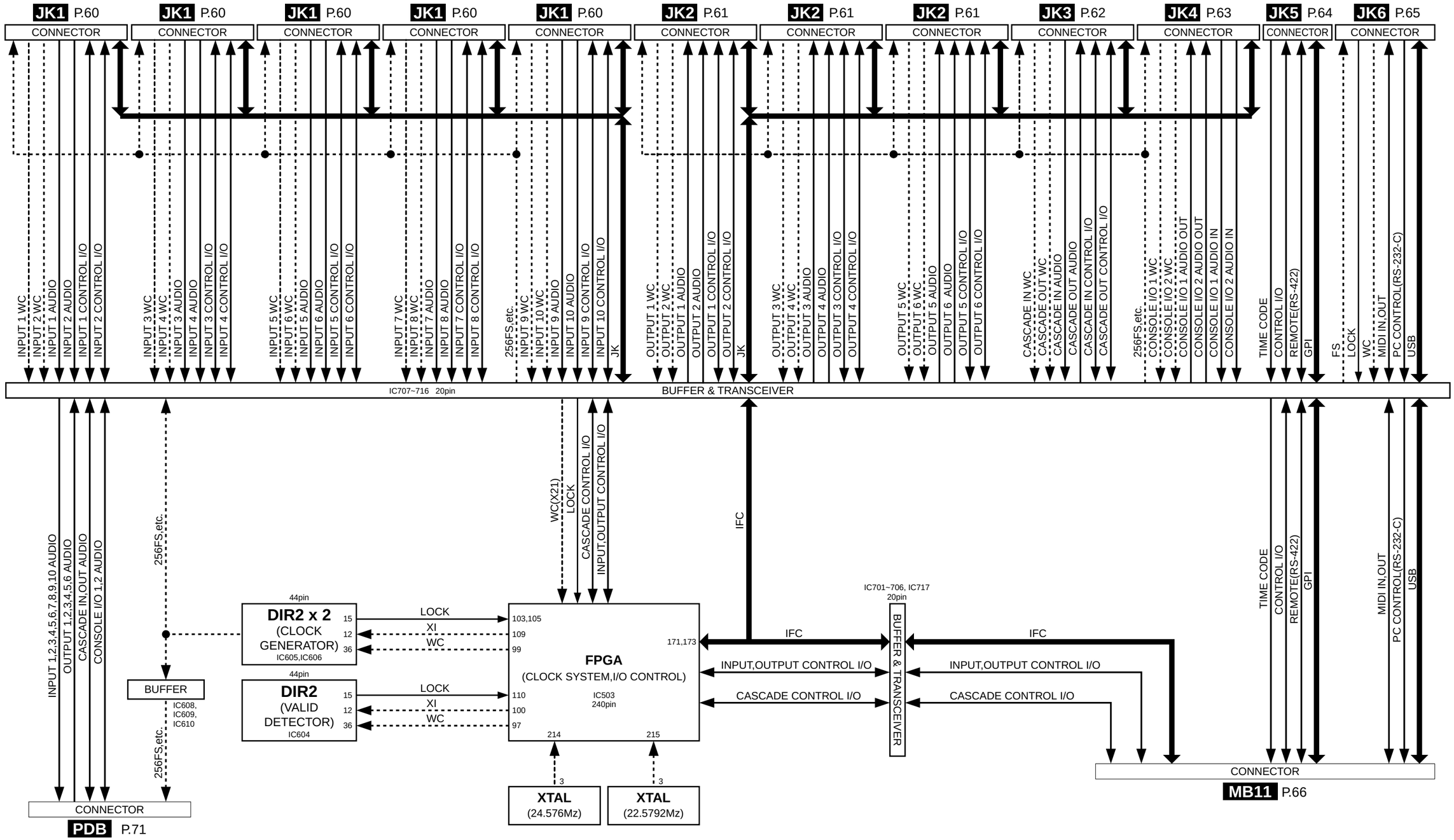
**• If the INPUT CONFIGURATION 48CH is flashing:**

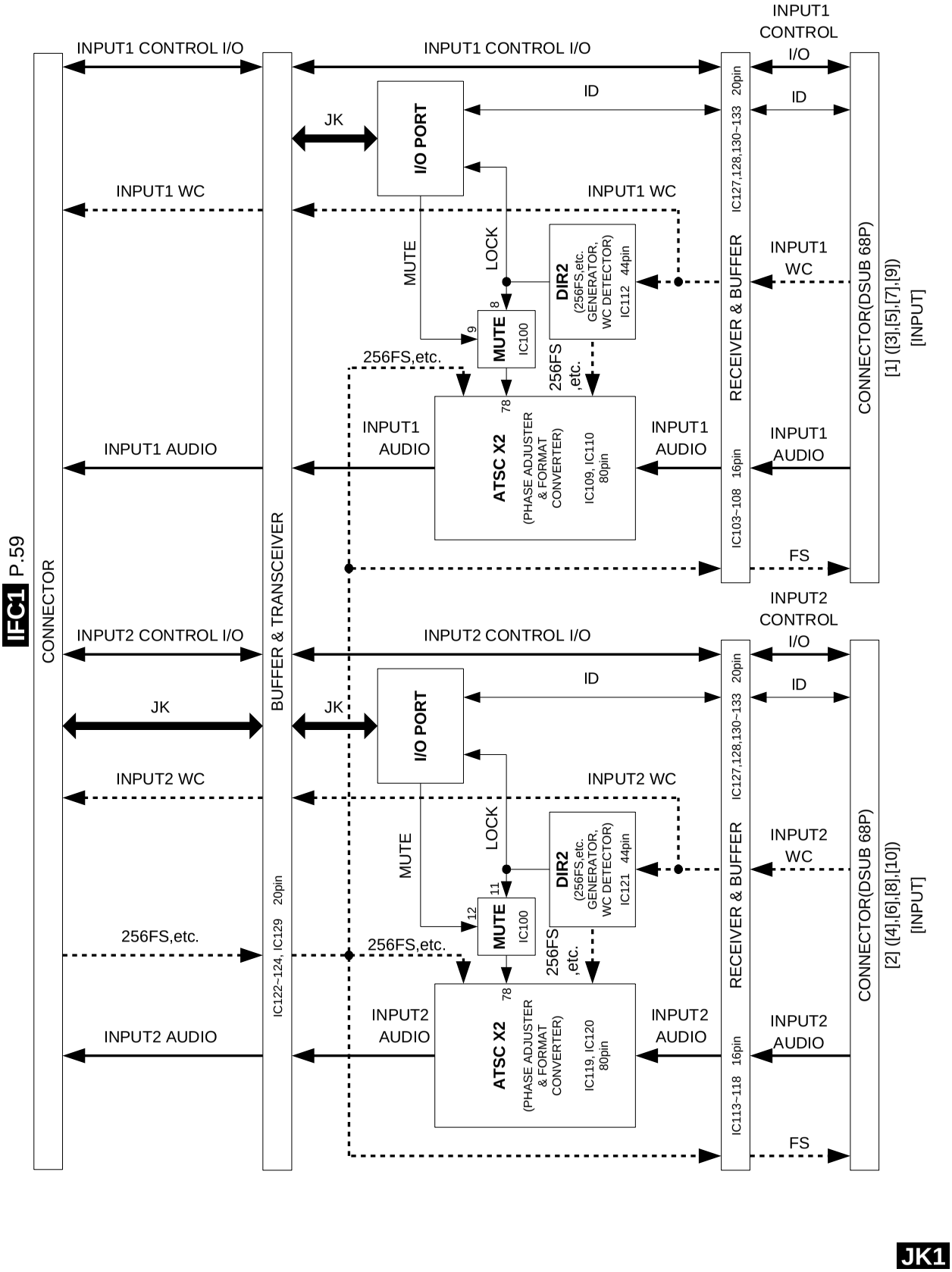
→ The signal is not locking to the word clock.

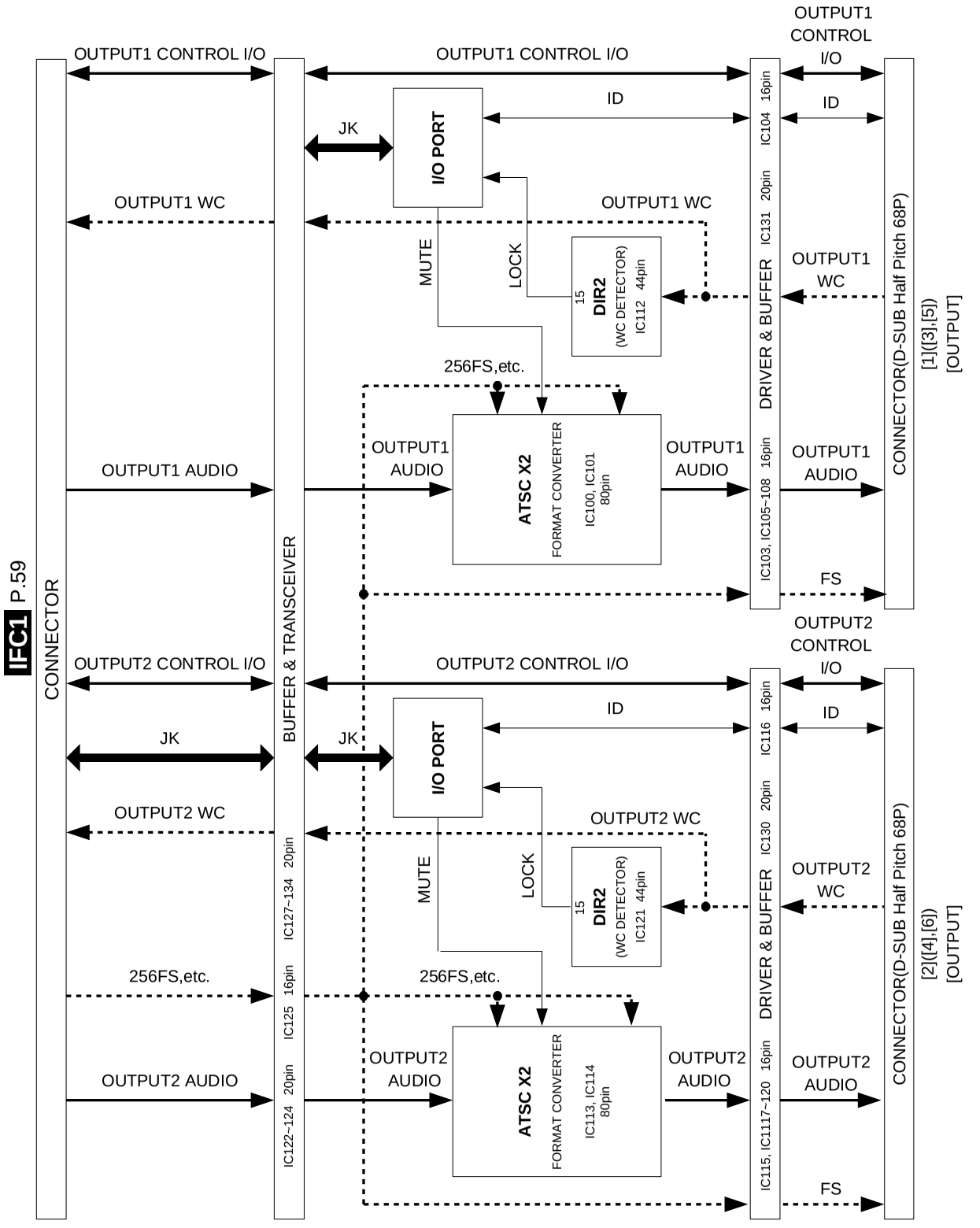
## BLOCK DIAGRAM

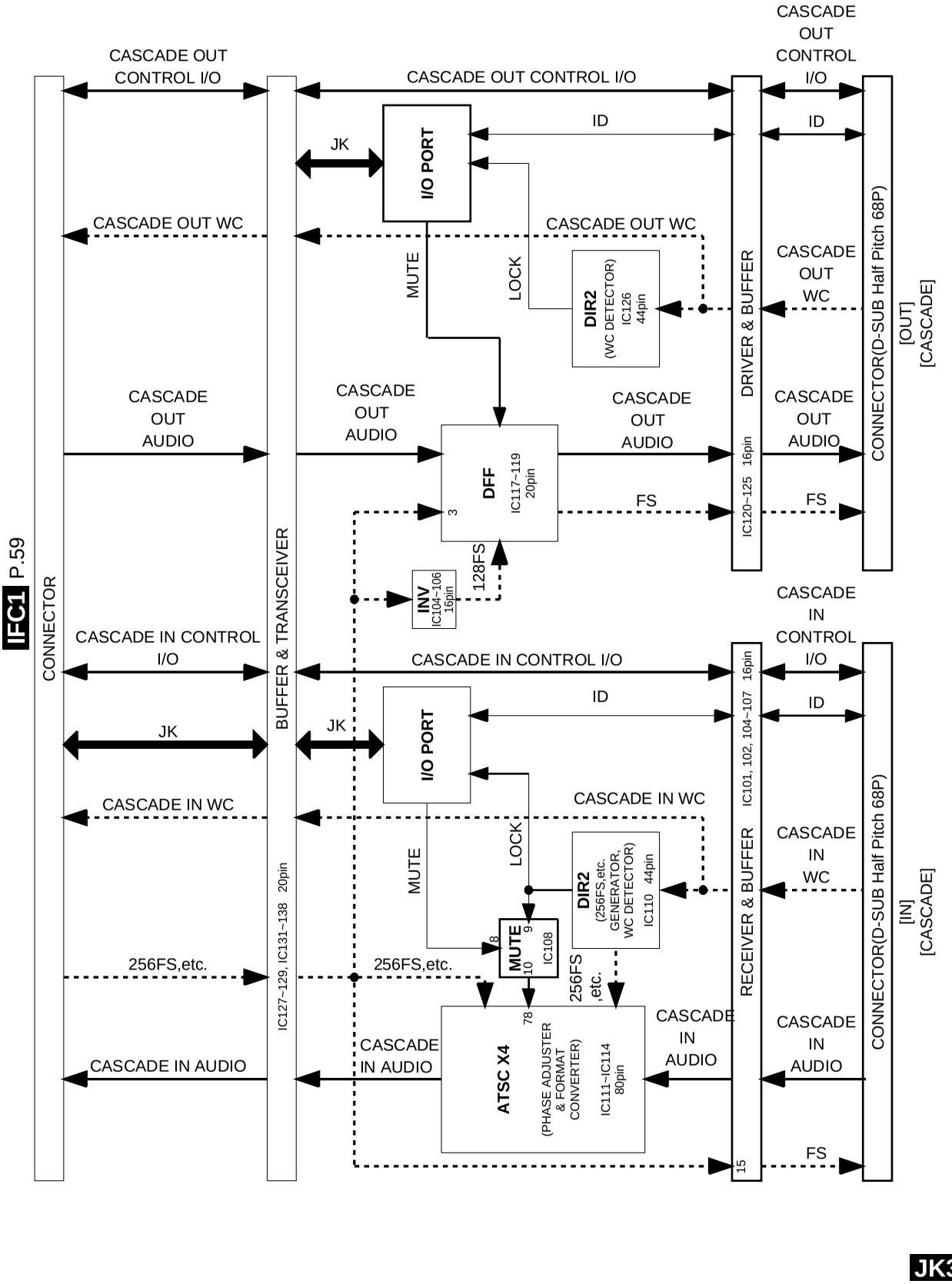


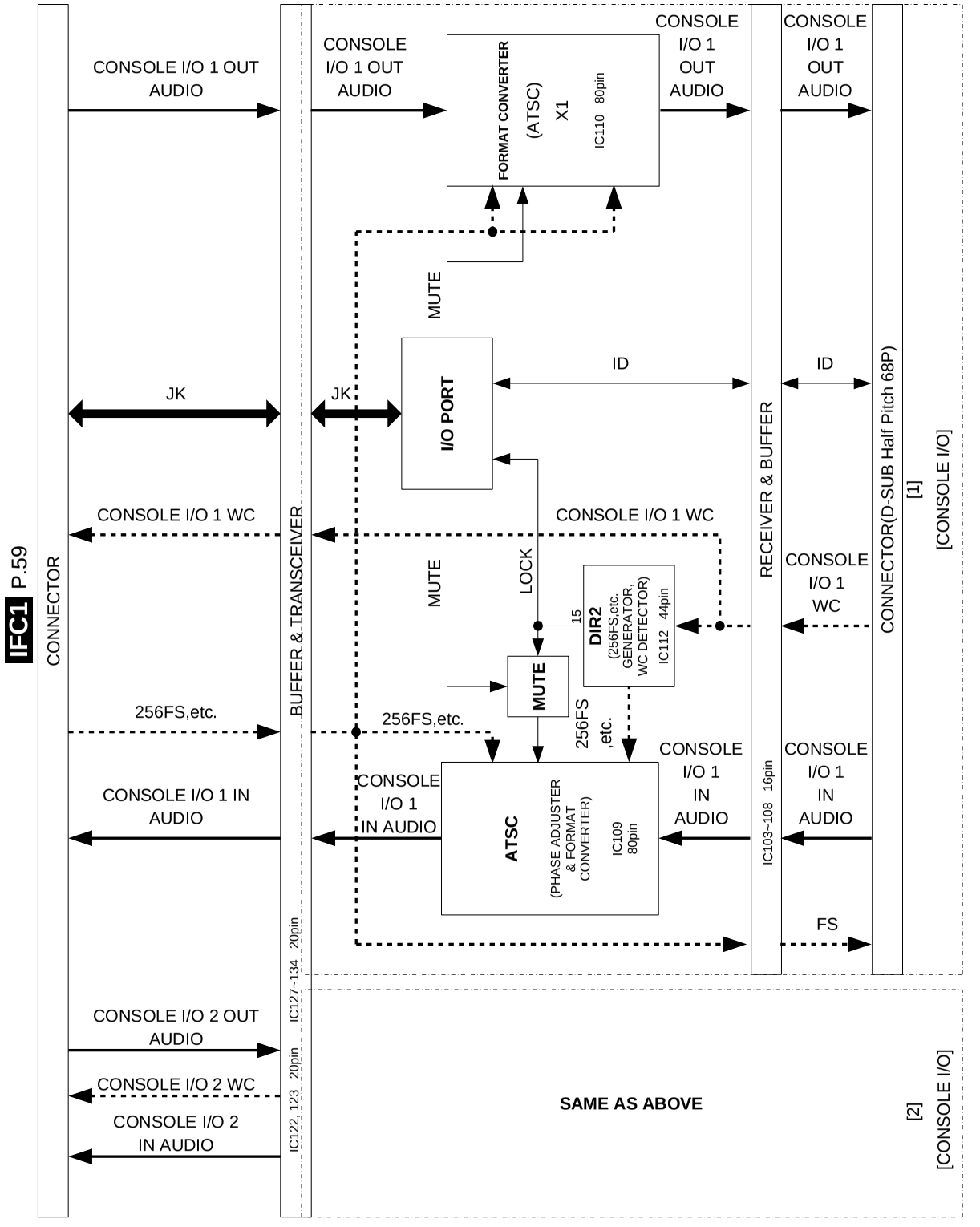

KEC-92538-2

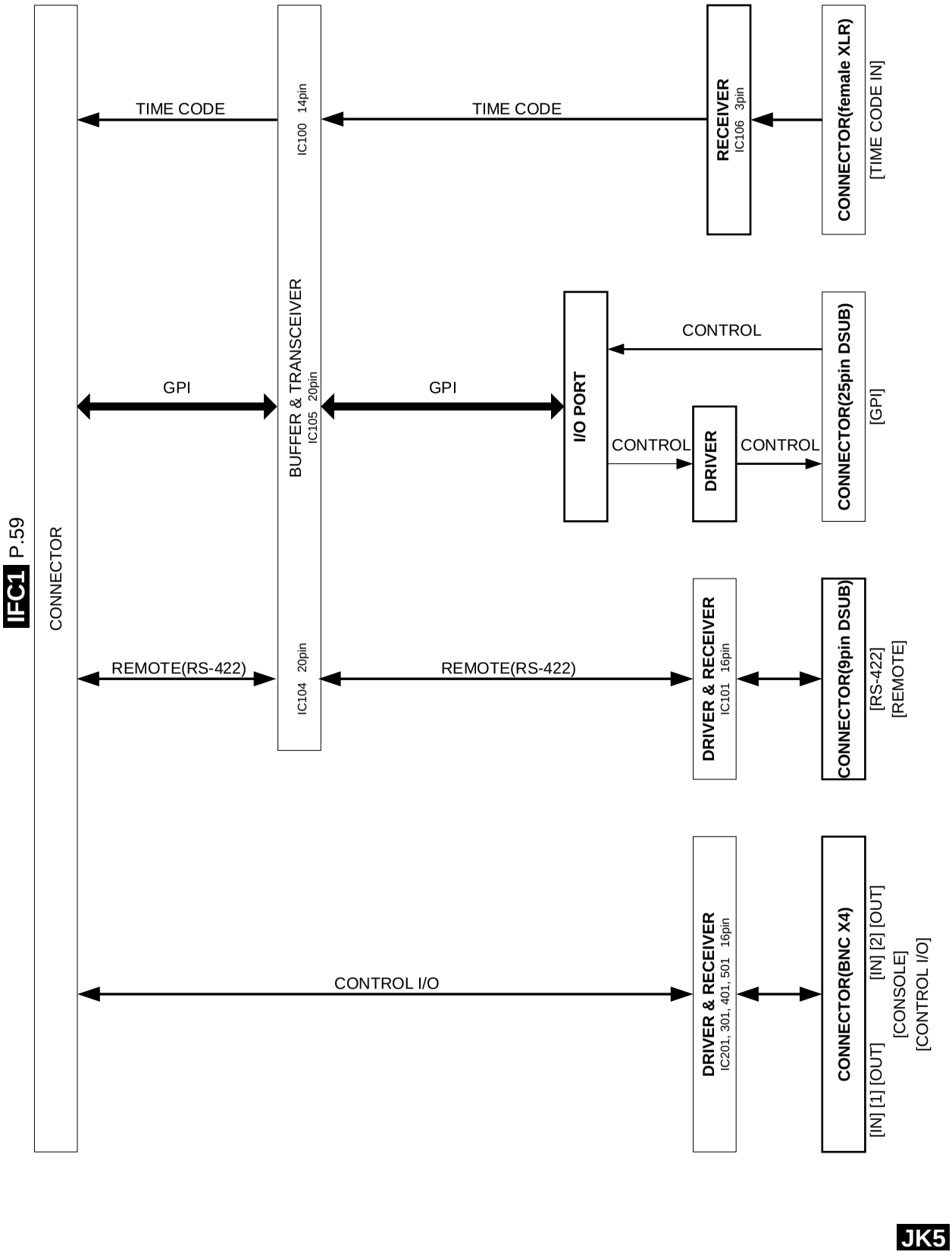

JK1 P.60
JK2 P.61
JK3 P.62
JK4 P.63
JK5 P.64
JK6 P.65
CONNECTOR
INPUT 1 WC
INPUT 2 WC
INPUT 1 AUDIO
INPUT 2 AUDIO
INPUT 1 CONTROL I/O
INPUT 2 CONTROL I/O
INPUT 3 WC
INPUT 4 WC
INPUT 3 AUDIO
INPUT 4 AUDIO
INPUT 3 CONTROL I/O
INPUT 4 CONTROL I/O
INPUT 5 WC
INPUT 6 WC
INPUT 5 AUDIO
INPUT 6 AUDIO
INPUT 5 CONTROL I/O
INPUT 6 CONTROL I/O
INPUT 7 WC
INPUT 8 WC
INPUT 7 AUDIO
INPUT 8 AUDIO
INPUT 7 CONTROL I/O
INPUT 8 CONTROL I/O
256FS,etc.
INPUT 9 WC
INPUT 10 WC
INPUT 9 AUDIO
INPUT 10 AUDIO
INPUT 9 CONTROL I/O
INPUT 10 CONTROL I/O
JK
OUTPUT 1 WC
OUTPUT 2 WC
OUTPUT 1 AUDIO
OUTPUT 2 AUDIO
OUTPUT 1 CONTROL I/O
OUTPUT 2 CONTROL I/O
JK
OUTPUT 3 WC
OUTPUT 4 WC
OUTPUT 3 AUDIO
OUTPUT 4 AUDIO
OUTPUT 3 CONTROL I/O
OUTPUT 4 CONTROL I/O
OUTPUT 5 WC
OUTPUT 6 WC
OUTPUT 5 AUDIO
OUTPUT 6 AUDIO
OUTPUT 5 CONTROL I/O
OUTPUT 6 CONTROL I/O
CASCADE IN WC
CASCADE OUT WC
CASCADE IN AUDIO
CASCADE OUT AUDIO
CASCADE IN CONTROL I/O
CASCADE OUT CONTROL I/O
256FS,etc.
CONSOLE I/O 1 WC
CONSOLE I/O 2 WC
CONSOLE I/O 1 AUDIO OUT
CONSOLE I/O 2 AUDIO OUT
CONSOLE I/O 1 AUDIO IN
CONSOLE I/O 2 AUDIO IN
TIME CODE
CONTROL I/O
REMOTE(RS-422)
GPI
FS
LOCK
WC
MIDI IN,OUT
PC CONTROL(RS-232-C)
USB
IC707~716 20pin
BUFFER & TRANSCEIVER
INPUT 1,2,3,4,5,6,7,8,9,10 AUDIO
OUTPUT 1,2,3,4,5,6 AUDIO
CASCADE IN,OUT AUDIO
CONSOLE I/O 1,2 AUDIO
256FS,etc.
WC(X21)
LOCK
CASCADE CONTROL I/O
INPUT,OUTPUT CONTROL I/O
IFC
TIME CODE
CONTROL I/O
REMOTE(RS-422)
GPI
MIDI IN,OUT
PC CONTROL(RS-232-C)
USB
44pin
DIR2 x 2
(CLOCK GENERATOR)
IC605,IC606
LOCK
XI
WC
15
12
36
103,105
109
99
FPGA
(CLOCK SYSTEM,I/O CONTROL)
171,173
IC503
240pin
110
100
97
214
215
3
XTAL
(24.576Mz)
XTAL
(22.5792Mz)
IC701~706, IC717
20pin
BUFFER & TRANSCEIVER
IFC
INPUT,OUTPUT CONTROL I/O
CASCADE CONTROL I/O
BUFFER
IC608,
IC609,
IC610
CONNECTOR
PDB P.71
MB11 P.66
IFC1

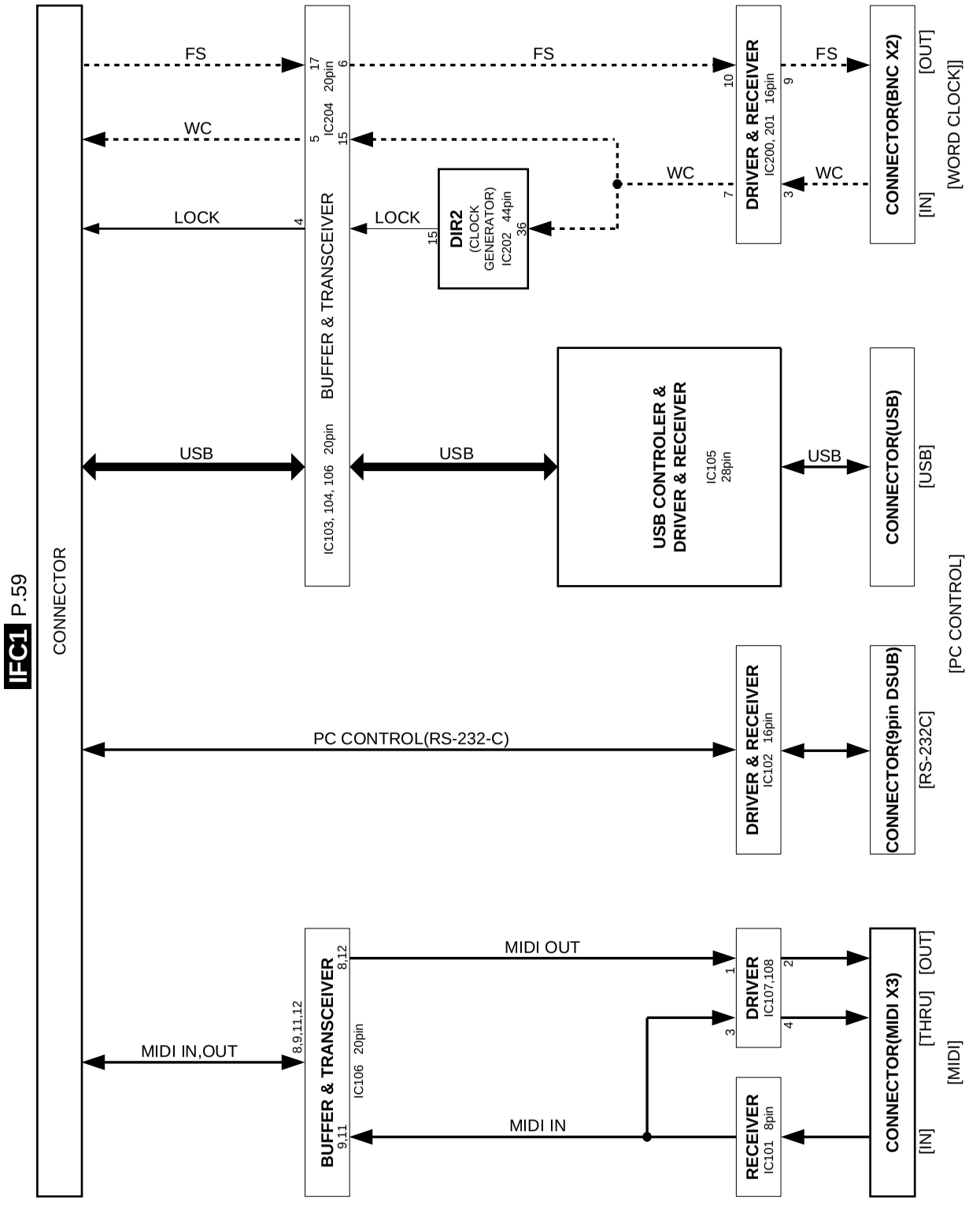

IFC1 P.59
CONNECTOR
BUFFER & TRANSCEIVER
IC122~124, IC129 20pin
INPUT1 CONTROL I/O
INPUT1 WC
INPUT1 AUDIO
INPUT2 CONTROL I/O
INPUT2 WC
INPUT2 AUDIO
256FS,etc.
JK
I/O PORT
ID
MUTE
LOCK
DIR2 (256FS,etc. GENERATOR, WC DETECTOR) IC112 44pin
DIR2 (256FS,etc. GENERATOR, WC DETECTOR) IC121 44pin
MUTE IC100
ATSC X2 (PHASE ADJUSTER & FORMAT CONVERTER) IC109, IC110 80pin
ATSC X2 (PHASE ADJUSTER & FORMAT CONVERTER) IC119, IC120 80pin
RECEIVER & BUFFER
IC127,128,130~133 20pin
IC103~108 16pin
IC113~118 16pin
FS
CONNECTOR(DSUB 68P)
[1] ([3],[5],[7],[9])
[2] ([4],[6],[8],[10])
[INPUT]
JK1

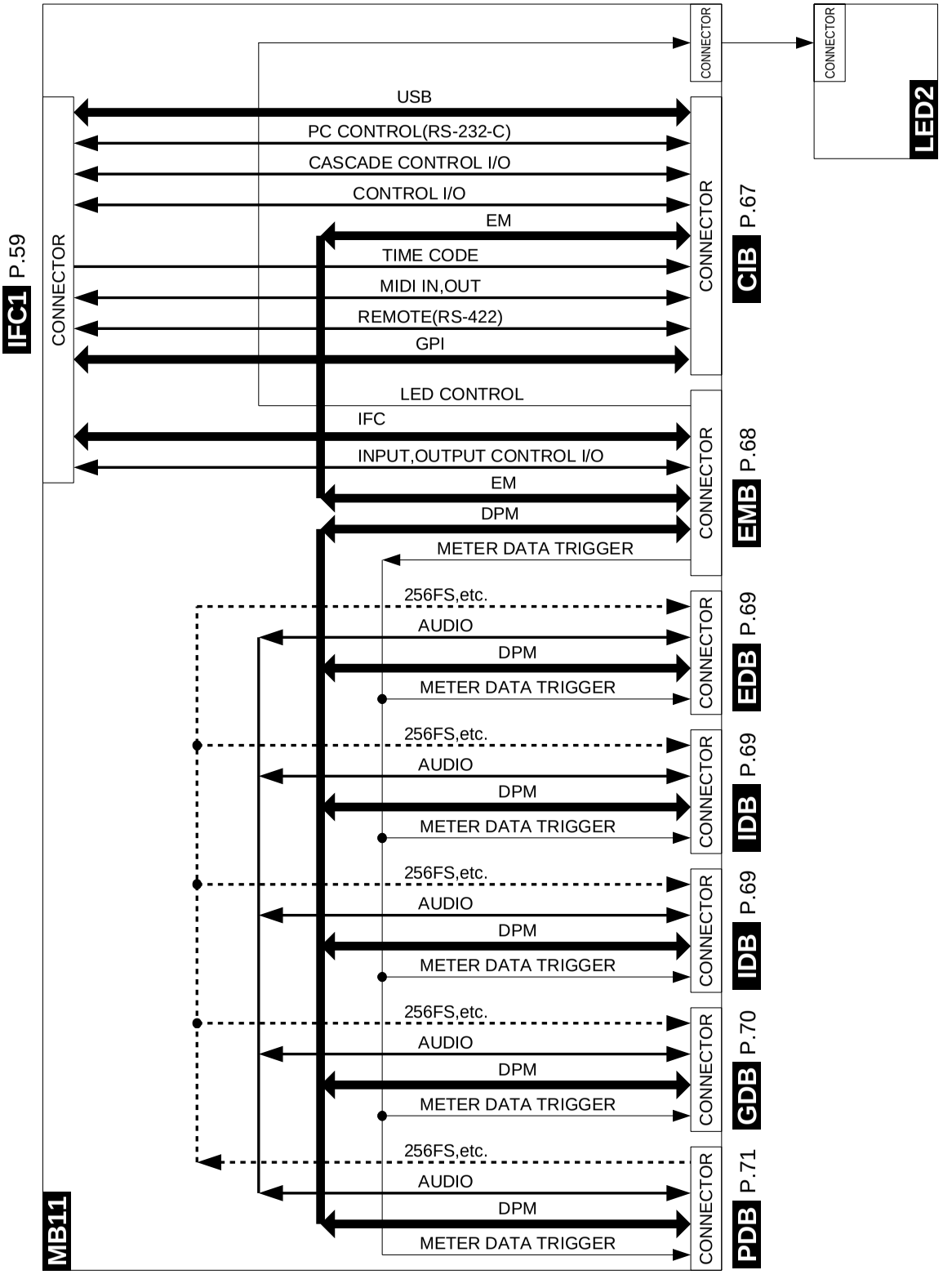

IFC1 P.59
CONNECTOR
BUFFER & TRANSCEIVER
IC122~124 20pin
IC125 16pin
IC127~134 20pin
OUTPUT1 CONTROL I/O
OUTPUT1 WC
OUTPUT1 AUDIO
OUTPUT2 CONTROL I/O
JK
OUTPUT2 WC
256FS,etc.
OUTPUT2 AUDIO
I/O PORT
ID
MUTE
LOCK
15 DIR2 (WC DETECTOR) IC112 44pin
15 DIR2 (WC DETECTOR) IC121 44pin
256FS,etc.
ATSC X2
FORMAT CONVERTER
IC100, IC101 80pin
IC113, IC114 80pin
OUTPUT1 AUDIO
OUTPUT2 AUDIO
DRIVER & BUFFER
IC103, IC105~108 16pin
IC115, IC1117~120 16pin
IC131 20pin
IC104 16pin
IC130 20pin
IC116 16pin
OUTPUT1 CONTROL I/O
OUTPUT1 WC
OUTPUT1 AUDIO
FS
OUTPUT2 CONTROL I/O
OUTPUT2 WC
OUTPUT2 AUDIO
FS
CONNECTOR(D-SUB Half Pitch 68P)
[1]([3],[5])
[OUTPUT]
[2]([4],[6])
[OUTPUT]
JK2


IFC1 P.59
CONNECTOR
CASCADE OUT CONTROL I/O
CASCADE OUT WC
CASCADE OUT AUDIO
CASCADE IN CONTROL I/O
CASCADE IN WC
CASCADE IN AUDIO
256FS,etc.
BUFFER & TRANSCEIVER
IC127~129, IC131~138 20pin
JK
I/O PORT
ID
MUTE
LOCK
DIR2
(WC DETECTOR)
IC126
44pin
DFF
IC117~119
20pin
3
128FS
INV
IC104~106
16pin
ATSC X4
(PHASE ADJUSTER & FORMAT CONVERTER)
IC111~IC114
80pin
78
MUTE
IC108
8
9
10
DIR2
(256FS,etc. GENERATOR, WC DETECTOR)
IC110 44pin
DRIVER & BUFFER
IC120~125 16pin
RECEIVER & BUFFER
IC101, 102, 104~107 16pin
15
FS
CONNECTOR(D-SUB Half Pitch 68P)
[OUT]
[CASCADE]
[IN]
[CASCADE]
JK3

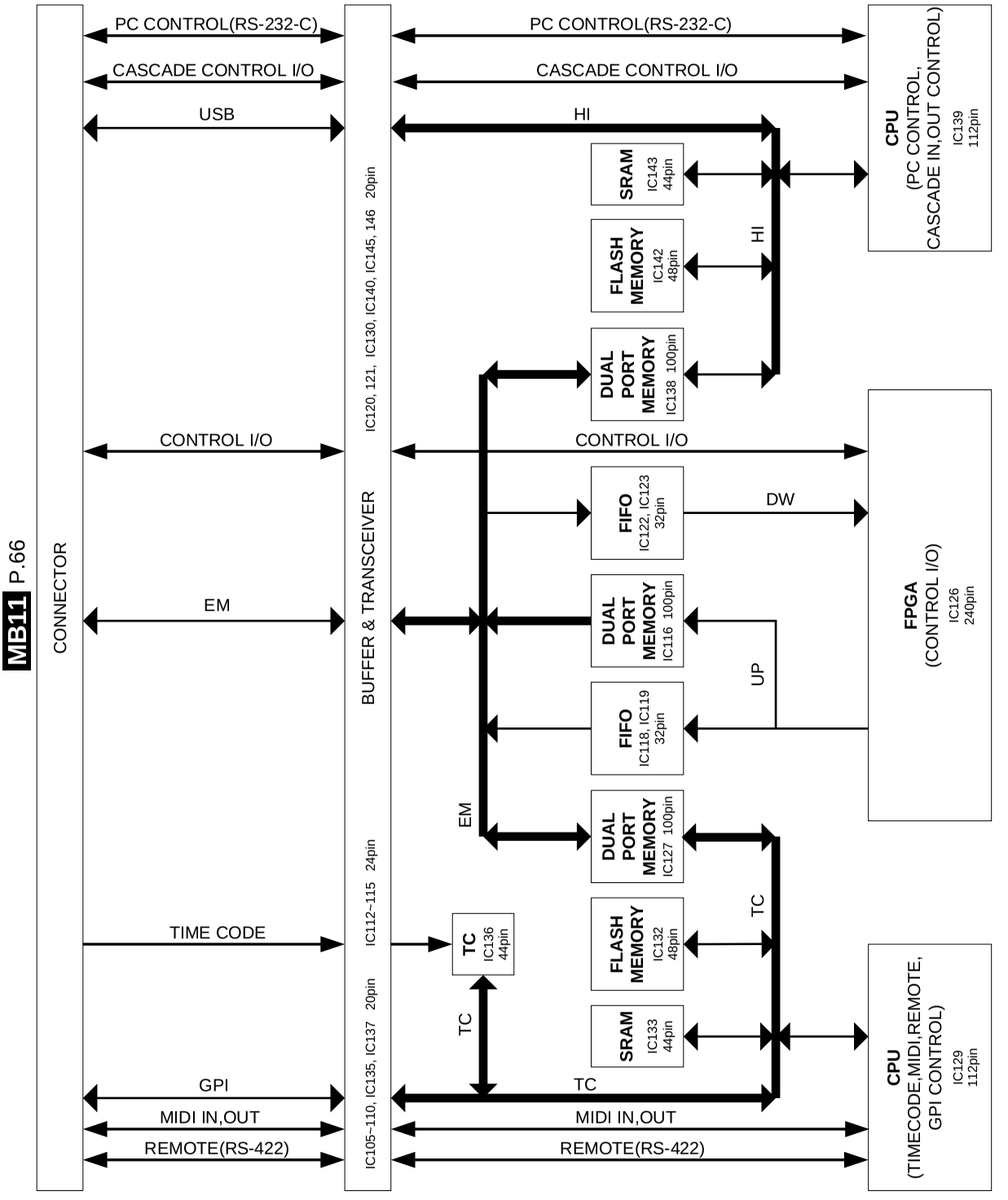

IFC1 P.59
CONNECTOR
CONSOLE I/O 1 OUT AUDIO
JK
CONSOLE I/O 1 WC
256FS,etc.
CONSOLE I/O 1 IN AUDIO
CONSOLE I/O 2 OUT AUDIO
CONSOLE I/O 2 WC
CONSOLE I/O 2 IN AUDIO
BUFFER & TRANSCEIVER
IC127~134 20pin
IC122, 123 20pin
CONSOLE I/O 1 OUT AUDIO
JK
CONSOLE I/O 1 WC
MUTE
LOCK
15
DIR2
(256FS,etc. GENERATOR, WC DETECTOR)
IC112 44pin
MUTE
256FS,etc.
CONSOLE I/O 1 IN AUDIO
FORMAT CONVERTER
(ATSC)
X1
IC110 80pin
MUTE
I/O PORT
ID
ATSC
(PHASE ADJUSTER & FORMAT CONVERTER)
IC109 80pin
256FS ,etc.
CONSOLE I/O 1 OUT AUDIO
ID
CONSOLE I/O 1 IN AUDIO
RECEIVER & BUFFER
IC103~108 16pin
FS
CONSOLE I/O 1 OUT AUDIO
CONSOLE I/O 1 WC
CONSOLE I/O 1 IN AUDIO
ID
CONNECTOR(D-SUB Half Pitch 68P)
[1]
[CONSOLE I/O]
SAME AS ABOVE
[2]
[CONSOLE I/O]
JK4


IFC1 P.59
CONNECTOR
TIME CODE
TIME CODE
BUFFER & TRANSCEIVER
IC100 14pin
IC105 20pin
IC104 20pin
RECEIVER
IC106 3pin
CONNECTOR(female XLR)
[TIME CODE IN]
GPI
GPI
I/O PORT
CONTROL
CONTROL
DRIVER
CONTROL
CONNECTOR(25pin DSUB)
[GPI]
REMOTE(RS-422)
REMOTE(RS-422)
DRIVER & RECEIVER
IC101 16pin
CONNECTOR(9pin DSUB)
[RS-422]
[REMOTE]
CONTROL I/O
DRIVER & RECEIVER
IC201, 301, 401, 501 16pin
CONNECTOR(BNC X4)
[IN] [1] [OUT]
[IN] [2] [OUT]
[CONSOLE]
[CONTROL I/O]
JK5

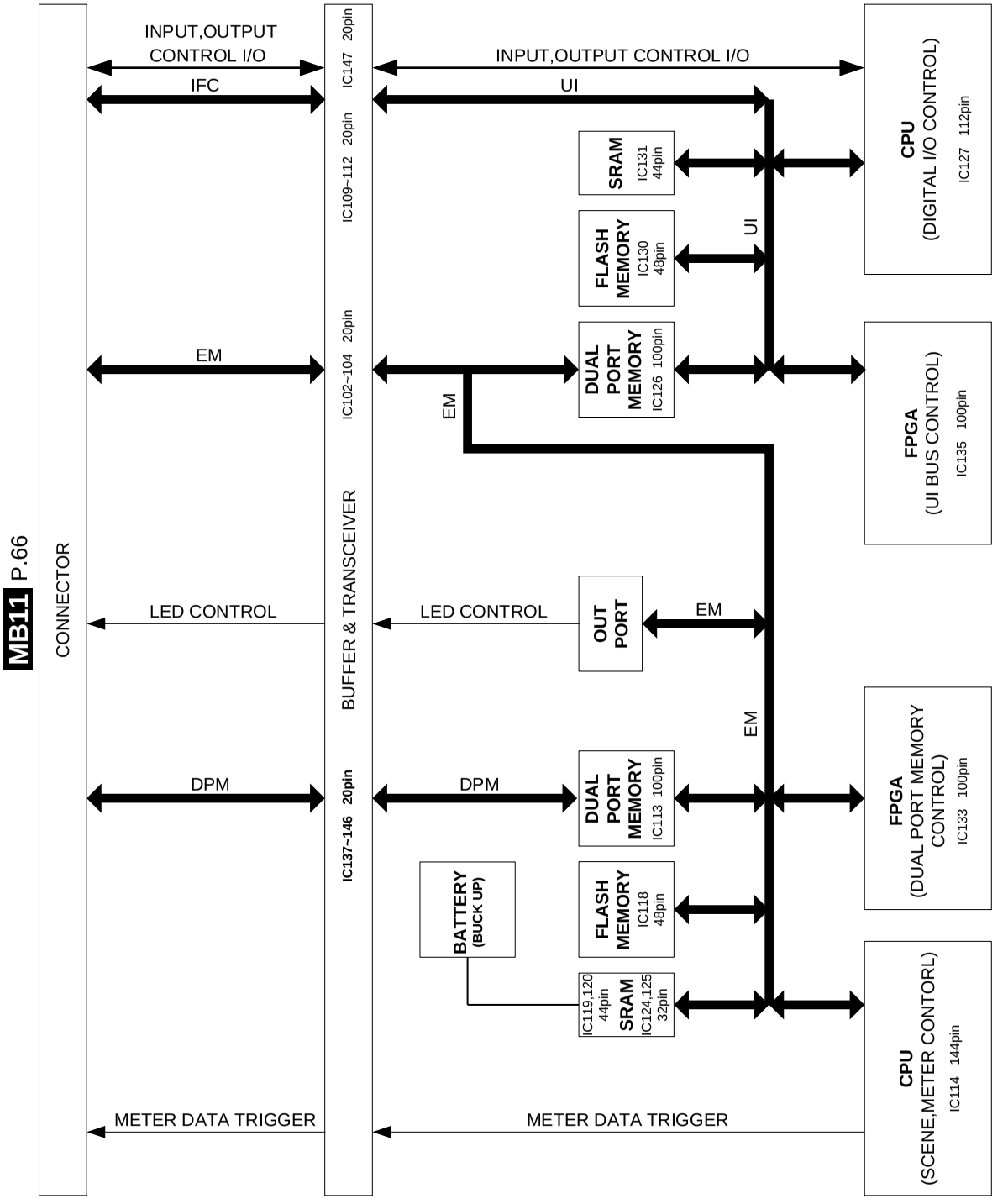

IFC1 P.59
CONNECTOR
FS
WC
LOCK
USB
PC CONTROL(RS-232-C)
MIDI IN,OUT
BUFFER & TRANSCEIVER
IC103, 104, 106 20pin
17
20pin
6
IC204
5
15
4
DIR2
(CLOCK GENERATOR)
IC202 44pin
15
36
DRIVER & RECEIVER
IC200, 201 16pin
10
9
7
3
CONNECTOR(BNC X2)
[IN]
[OUT]
[WORD CLOCK]
USB CONTROLER & DRIVER & RECEIVER
IC105
28pin
CONNECTOR(USB)
[USB]
DRIVER & RECEIVER
IC102 16pin
CONNECTOR(9pin DSUB)
[RS-232C]
[PC CONTROL]
BUFFER & TRANSCEIVER
9,11
8,12
8,9,11,12
IC106 20pin
MIDI OUT
MIDI IN
DRIVER
IC107,108
1
2
3
4
RECEIVER
IC101 8pin
CONNECTOR(MIDI X3)
[IN]
[THRU]
[OUT]
[MIDI]
JK6


MB11
CONNECTOR
IFC1 P.59
USB
PC CONTROL(RS-232-C)
CASCADE CONTROL I/O
CONTROL I/O
EM
TIME CODE
MIDI IN,OUT
REMOTE(RS-422)
GPI
CIB P.67
LED CONTROL
IFC
INPUT,OUTPUT CONTROL I/O
EM
DPM
METER DATA TRIGGER
EMB P.68
256FS,etc.
AUDIO
DPM
METER DATA TRIGGER
EDB P.69
256FS,etc.
AUDIO
DPM
METER DATA TRIGGER
IDB P.69
256FS,etc.
AUDIO
DPM
METER DATA TRIGGER
IDB P.69
256FS,etc.
AUDIO
DPM
METER DATA TRIGGER
GDB P.70
256FS,etc.
AUDIO
DPM
METER DATA TRIGGER
PDB P.71
CONNECTOR
LED2

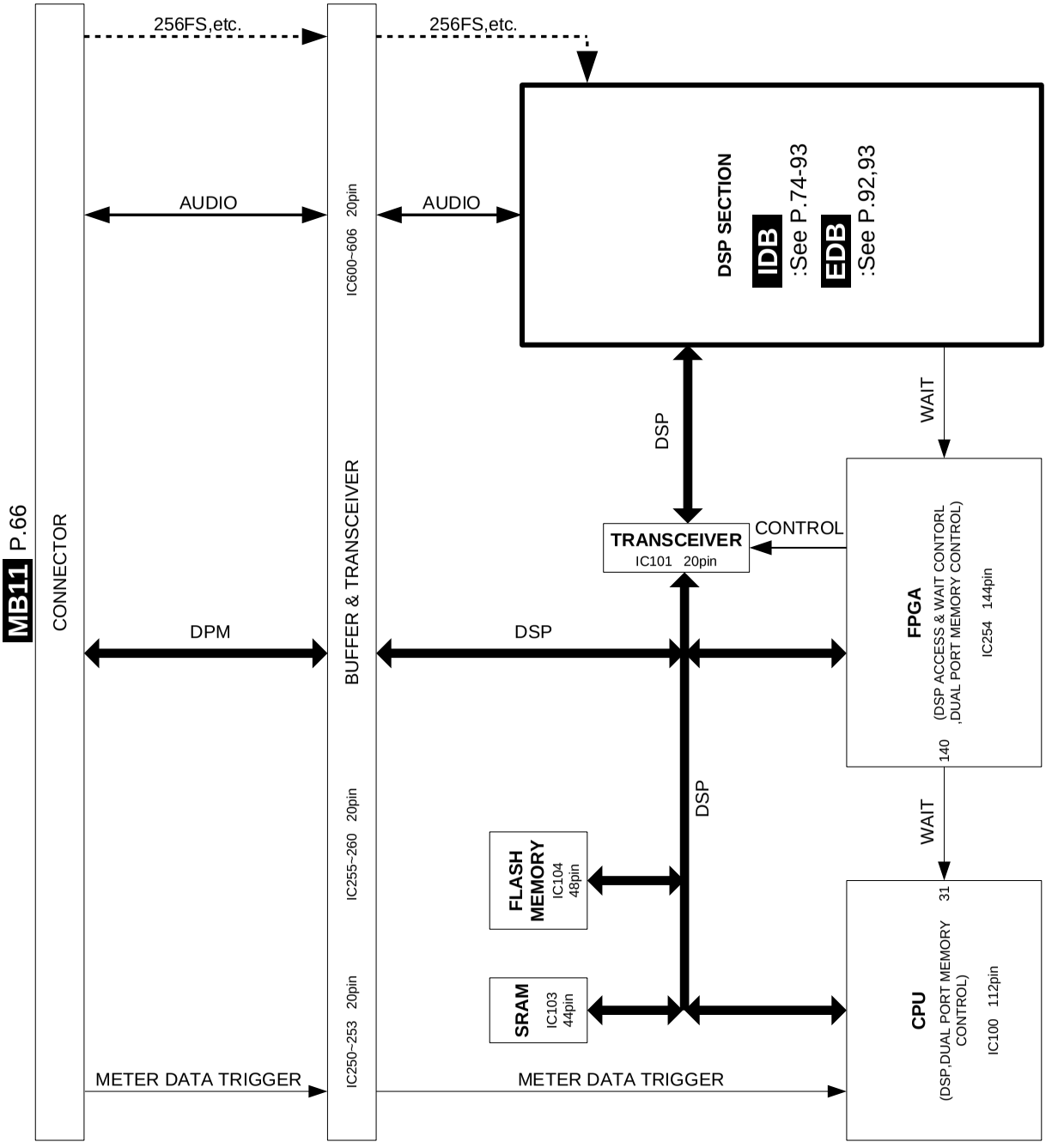
MB11 LED2


MB11 P.66
CONNECTOR
PC CONTROL(RS-232-C)
CASCADE CONTROL I/O
USB
CONTROL I/O
EM
TIME CODE
GPI
MIDI IN,OUT
REMOTE(RS-422)
BUFFER & TRANSCEIVER
IC105~110, IC135, IC137 20pin
IC112~115 24pin
IC120, 121, IC130, IC140, IC145, 146 20pin
PC CONTROL(RS-232-C)
CASCADE CONTROL I/O
HI
CONTROL I/O
DW
EM
UP
TC
TC
TC
MIDI IN,OUT
REMOTE(RS-422)
CPU
(PC CONTROL, CASCADE IN,OUT CONTROL)
IC139 112pin
SRAM IC143 44pin
FLASH MEMORY IC142 48pin
DUAL PORT MEMORY IC138 100pin
FIFO IC122, IC123 32pin
DUAL PORT MEMORY IC116 100pin
FIFO IC118, IC119 32pin
DUAL PORT MEMORY IC127 100pin
FLASH MEMORY IC132 48pin
SRAM IC133 44pin
TC IC136 44pin
FPGA
(CONTROL I/O)
IC126 240pin
CPU
(TIMECODE,MIDI,REMOTE, GPI CONTROL)
IC129 112pin

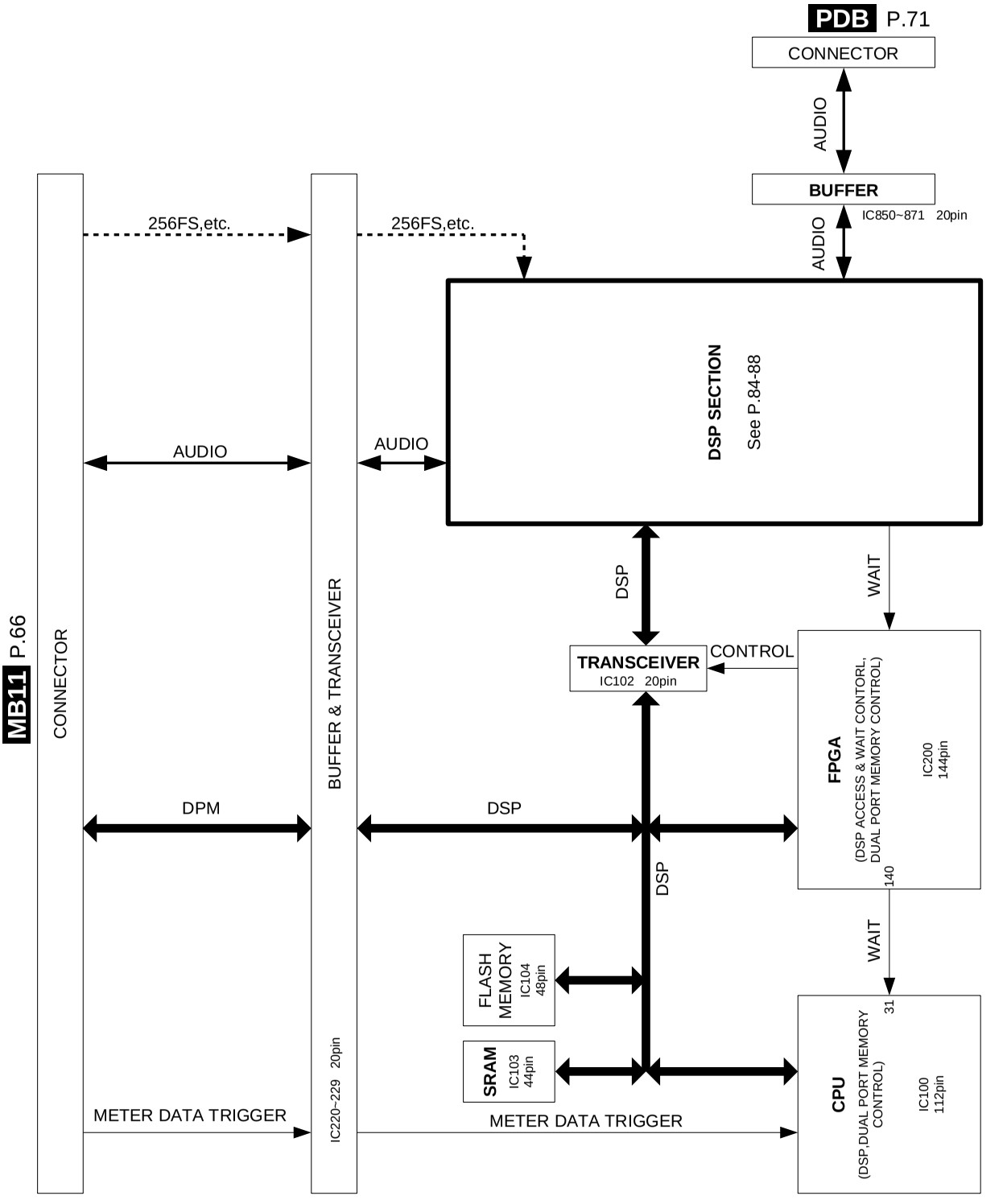
CIB


MB11 P.66
CONNECTOR
INPUT,OUTPUT CONTROL I/O
IFC
EM
LED CONTROL
DPM
METER DATA TRIGGER
BUFFER & TRANSCEIVER
IC147 20pin
IC109~112 20pin
IC102~104 20pin
IC137~146 20pin
INPUT,OUTPUT CONTROL I/O
UI
EM
LED CONTROL
DPM
METER DATA TRIGGER
SRAM IC131 44pin
FLASH MEMORY IC130 48pin
DUAL PORT MEMORY IC126 100pin
OUT PORT
DUAL PORT MEMORY IC113 100pin
BATTERY (BUCK UP)
FLASH MEMORY IC118 48pin
IC119,120 44pin SRAM IC124,125 32pin
CPU (DIGITAL I/O CONTROL) IC127 112pin
FPGA (UI BUS CONTROL) IC135 100pin
FPGA (DUAL PORT MEMORY CONTROL) IC133 100pin
CPU (SCENE,METER CONTORL) IC114 144pin

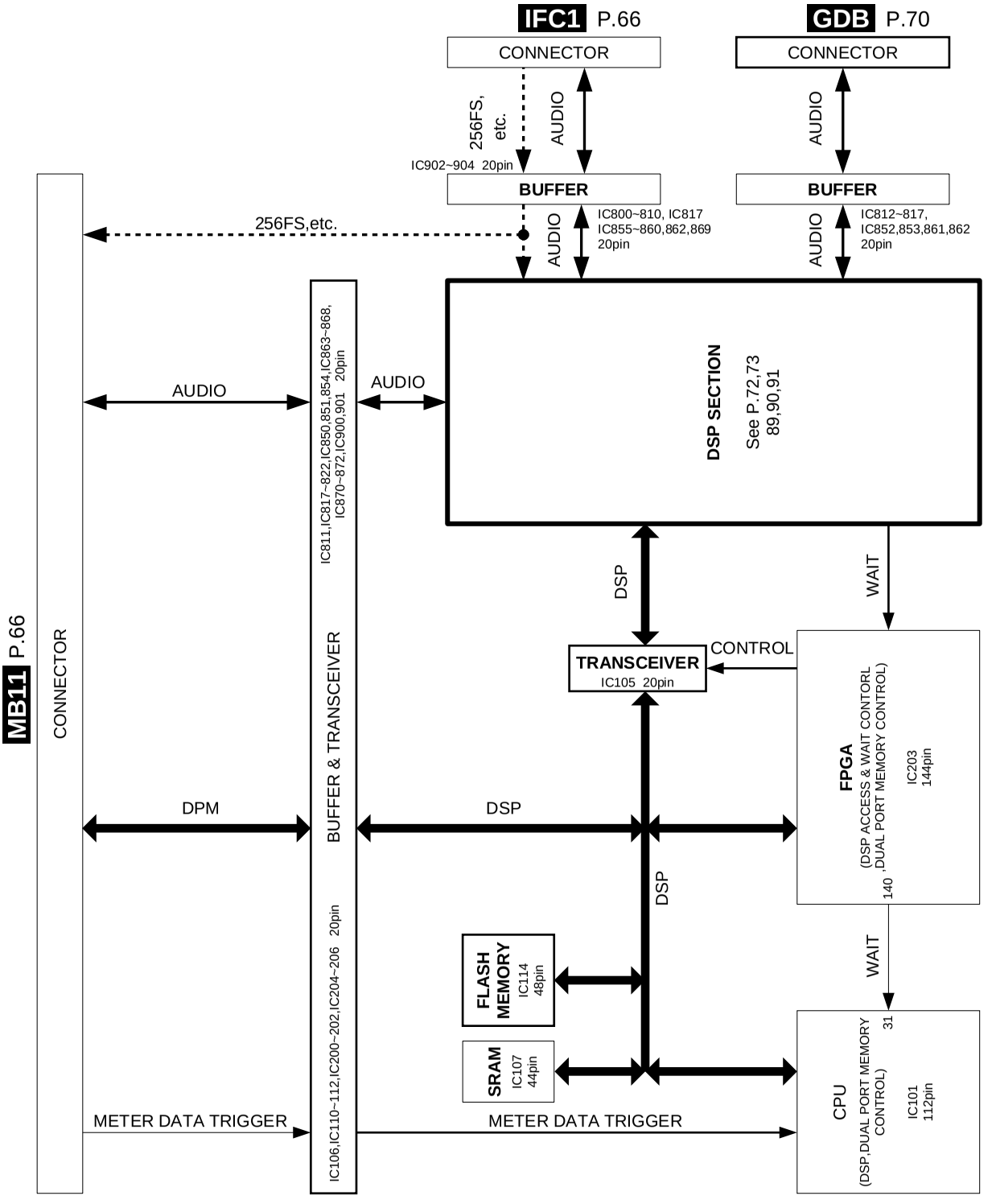
EMB


MB11 P.66
CONNECTOR
256FS,etc.
AUDIO
DPM
METER DATA TRIGGER
BUFFER & TRANSCEIVER
IC600~606 20pin
IC255~260 20pin
IC250~253 20pin
256FS,etc.
AUDIO
DSP SECTION
IDB :See P.74-93
EDB :See P.92,93
DSP
TRANSCEIVER
IC101 20pin
CONTROL
DSP
DSP
FLASH MEMORY
IC104
48pin
SRAM
IC103
44pin
METER DATA TRIGGER
WAIT
FPGA
(DSP ACCESS & WAIT CONTORL
,DUAL PORT MEMORY CONTROL)
IC254 144pin
140
WAIT
CPU
(DSP,DUAL PORT MEMORY CONTROL)
IC100 112pin
31

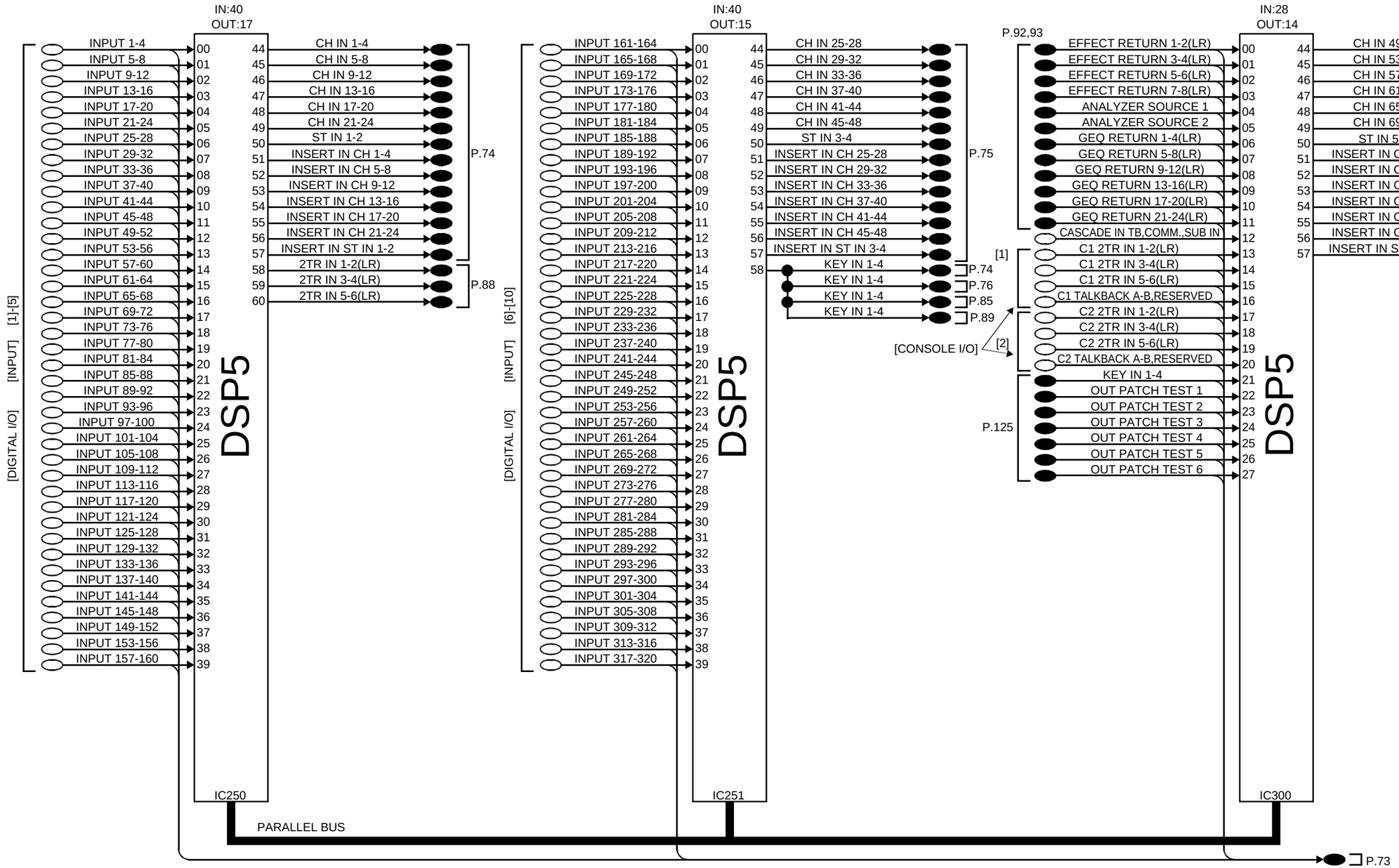
IDB EDB


PDB P.71
CONNECTOR
AUDIO
BUFFER
IC850~871 20pin
AUDIO
256FS,etc.
256FS,etc.
DSP SECTION
See P.84-88
AUDIO
AUDIO
MB11 P.66
CONNECTOR
BUFFER & TRANSCEIVER
IC220~229 20pin
DSP
WAIT
TRANSCEIVER
IC102 20pin
CONTROL
FPGA
(DSP ACCESS & WAIT CONTORL, DUAL PORT MEMORY CONTROL)
IC200
144pin
140
DPM
DSP
DSP
FLASH MEMORY
IC104
48pin
WAIT
SRAM
IC103
44pin
CPU
(DSP,DUAL PORT MEMORY CONTROL)
IC100
112pin
31
METER DATA TRIGGER
METER DATA TRIGGER

GDB

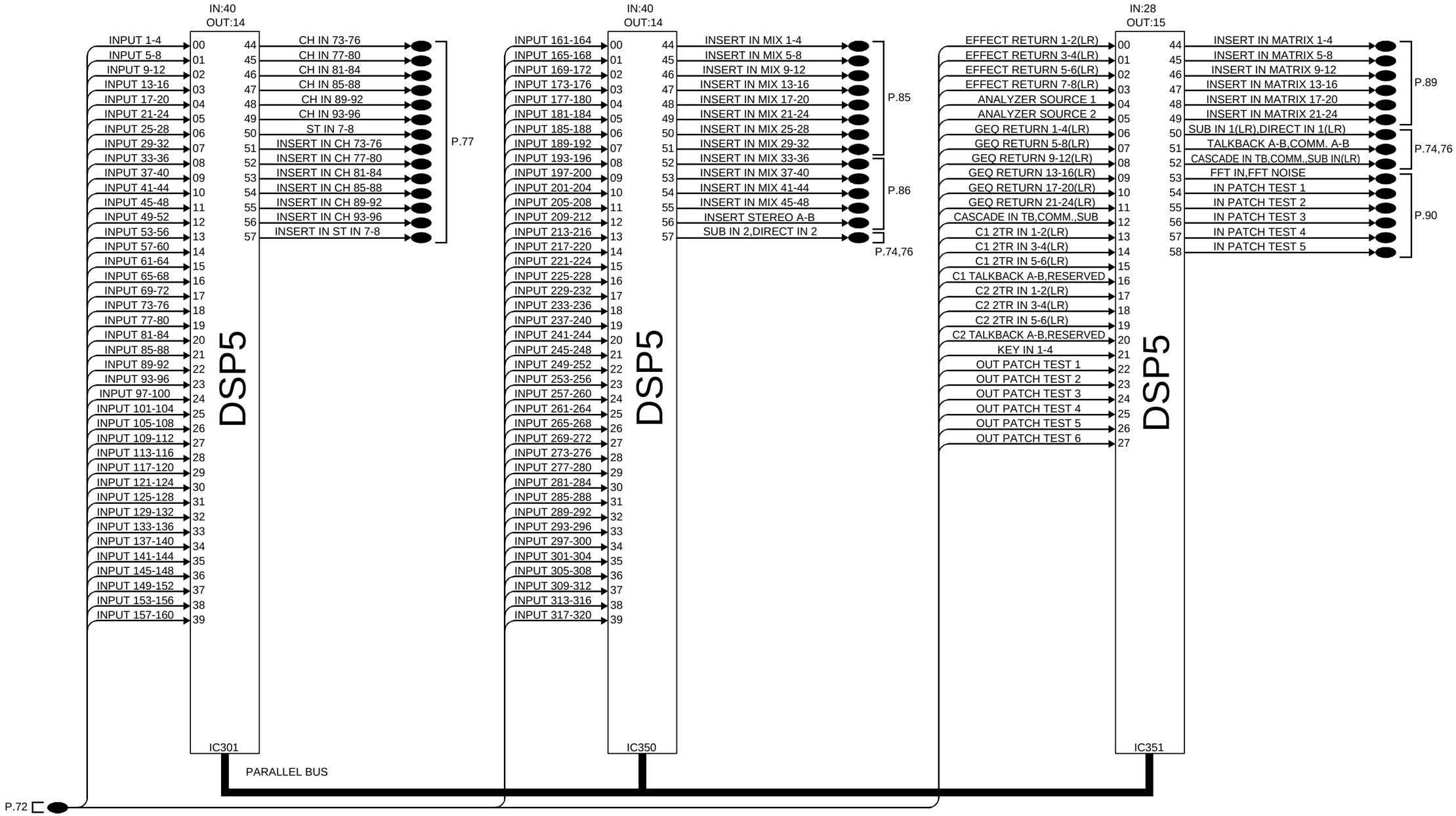

IFC1 P.66
GDB P.70
CONNECTOR
CONNECTOR
256FS, etc.
AUDIO
AUDIO
IC902~904 20pin
BUFFER
BUFFER
256FS,etc.
AUDIO
IC800~810, IC817
IC855~860,862,869
20pin
AUDIO
IC812~817,
IC852,853,861,862
20pin
DSP SECTION
See P.72,73
89,90,91
AUDIO
AUDIO
IC811,IC817~822,IC850,851,854,IC863~868,
IC870~872,IC900,901 20pin
DSP
WAIT
TRANSCEIVER
IC105 20pin
CONTROL
MB11 P.66
CONNECTOR
BUFFER & TRANSCEIVER
FPGA
(DSP ACCESS & WAIT CONTORL
,DUAL PORT MEMORY CONTROL)
140
IC203
144pin
DPM
DSP
DSP
FLASH MEMORY
IC114
48pin
WAIT
SRAM
IC107
44pin
IC106,IC110~112,IC200~202,IC204~206 20pin
CPU
(DSP,DUAL PORT MEMORY
CONTROL)
31
IC101
112pin
METER DATA TRIGGER
METER DATA TRIGGER

PDB




FUNCTION: INPUT PATCH, PEAK METER

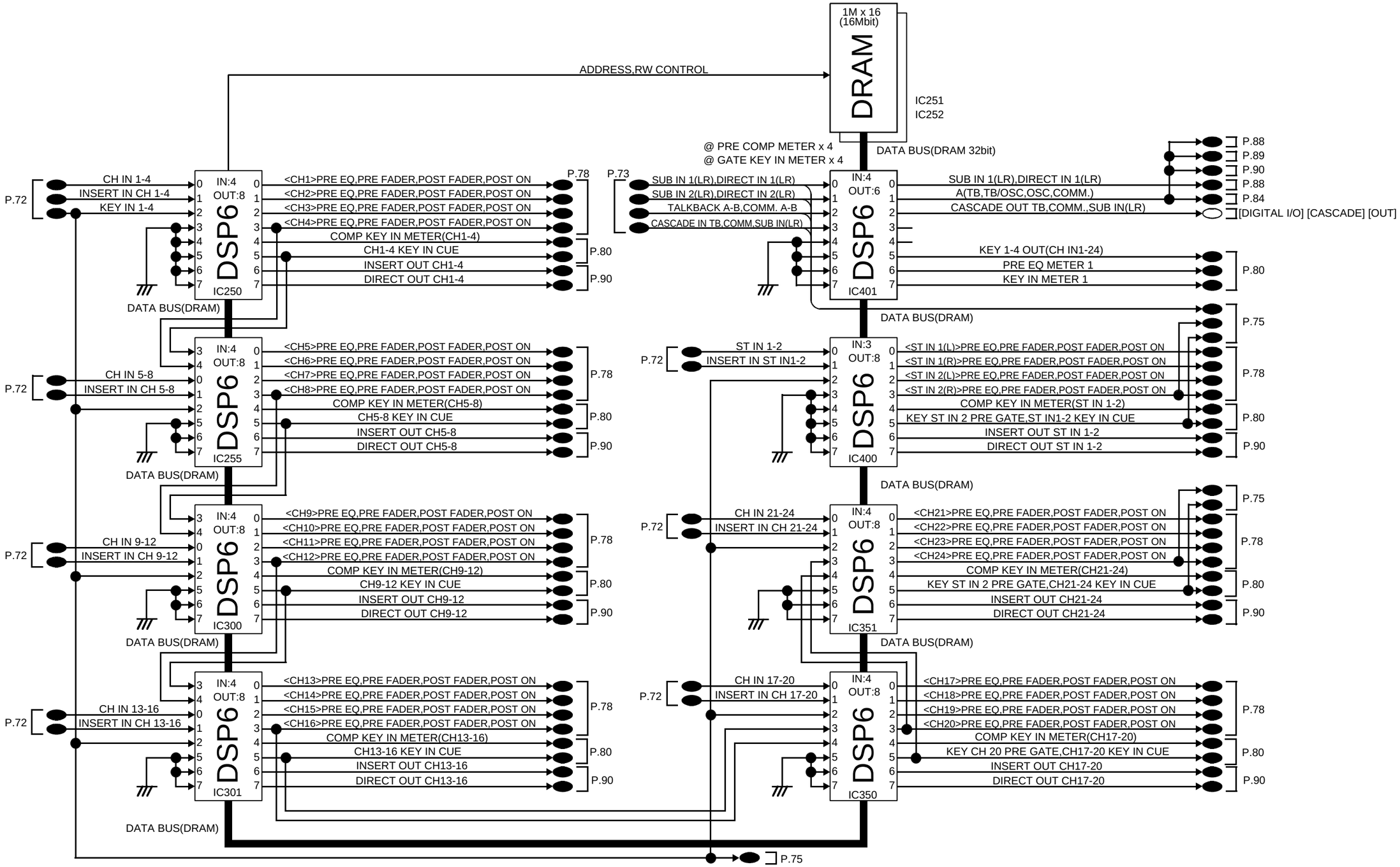
PDB



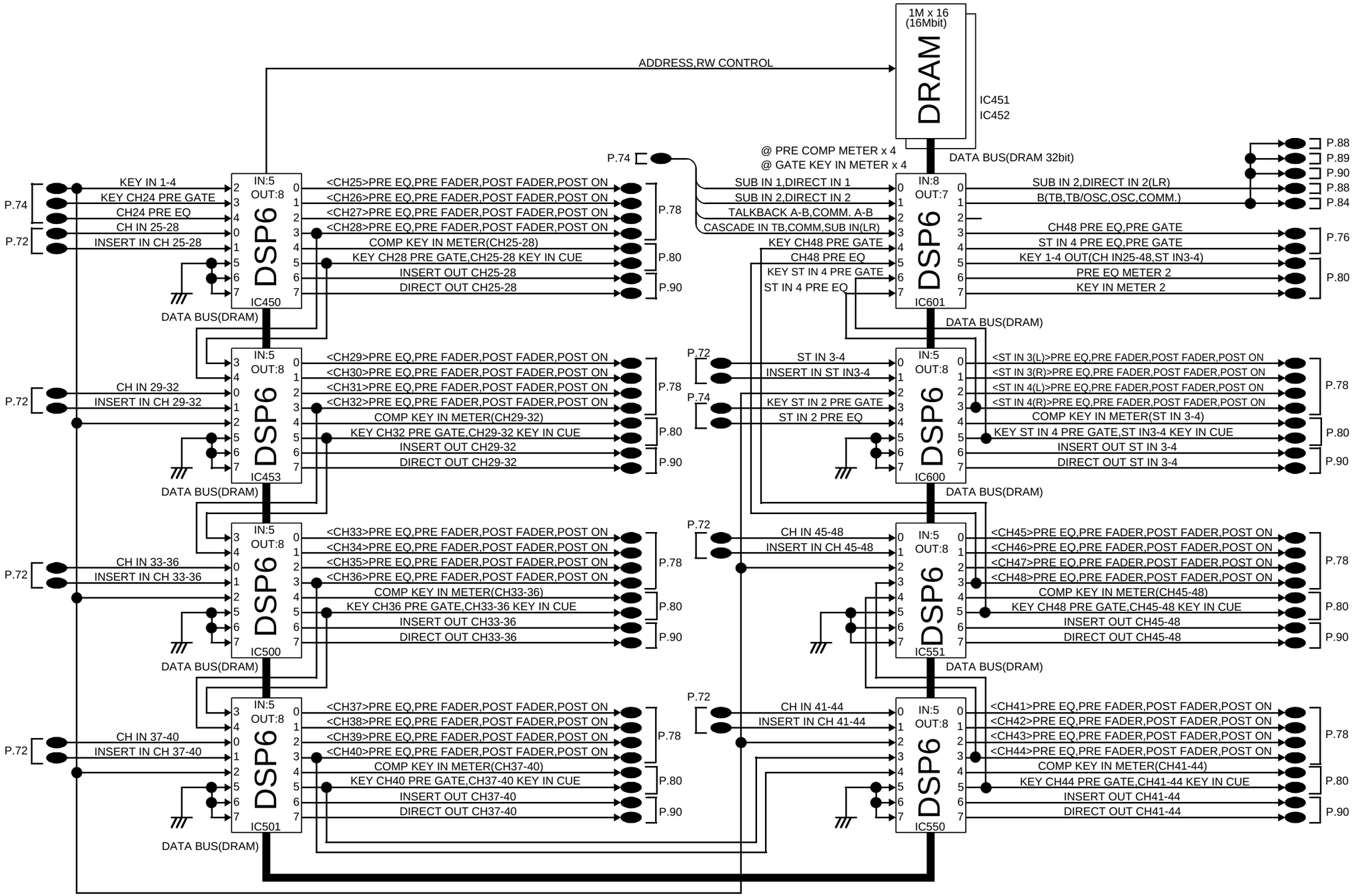

FUNCTION: INPUT PATCH, PEAK METER

PDB

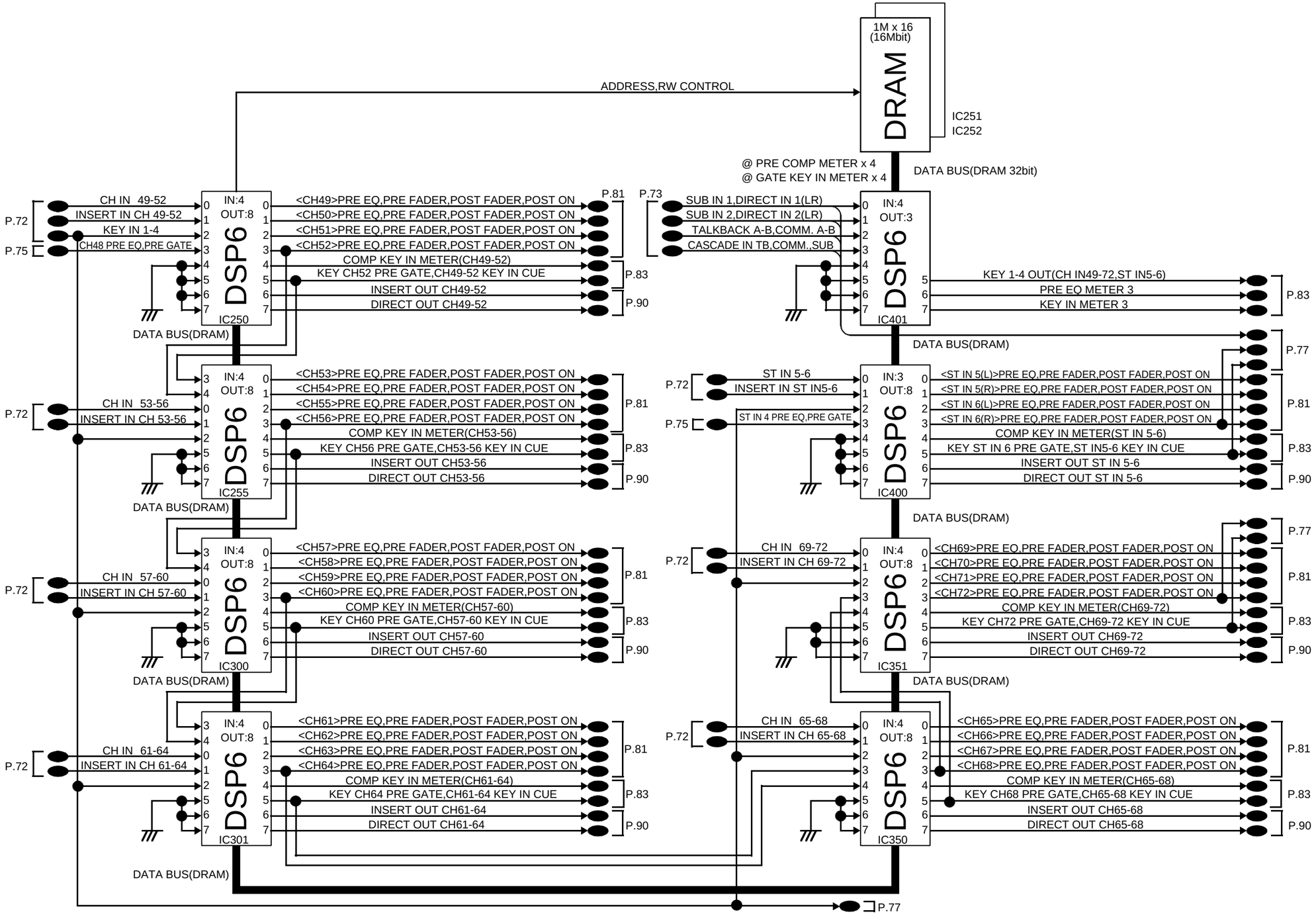
KEC-92538-17




FUNCTION: INPUT EQ/GATE/COMP/DELAY/FADER ON



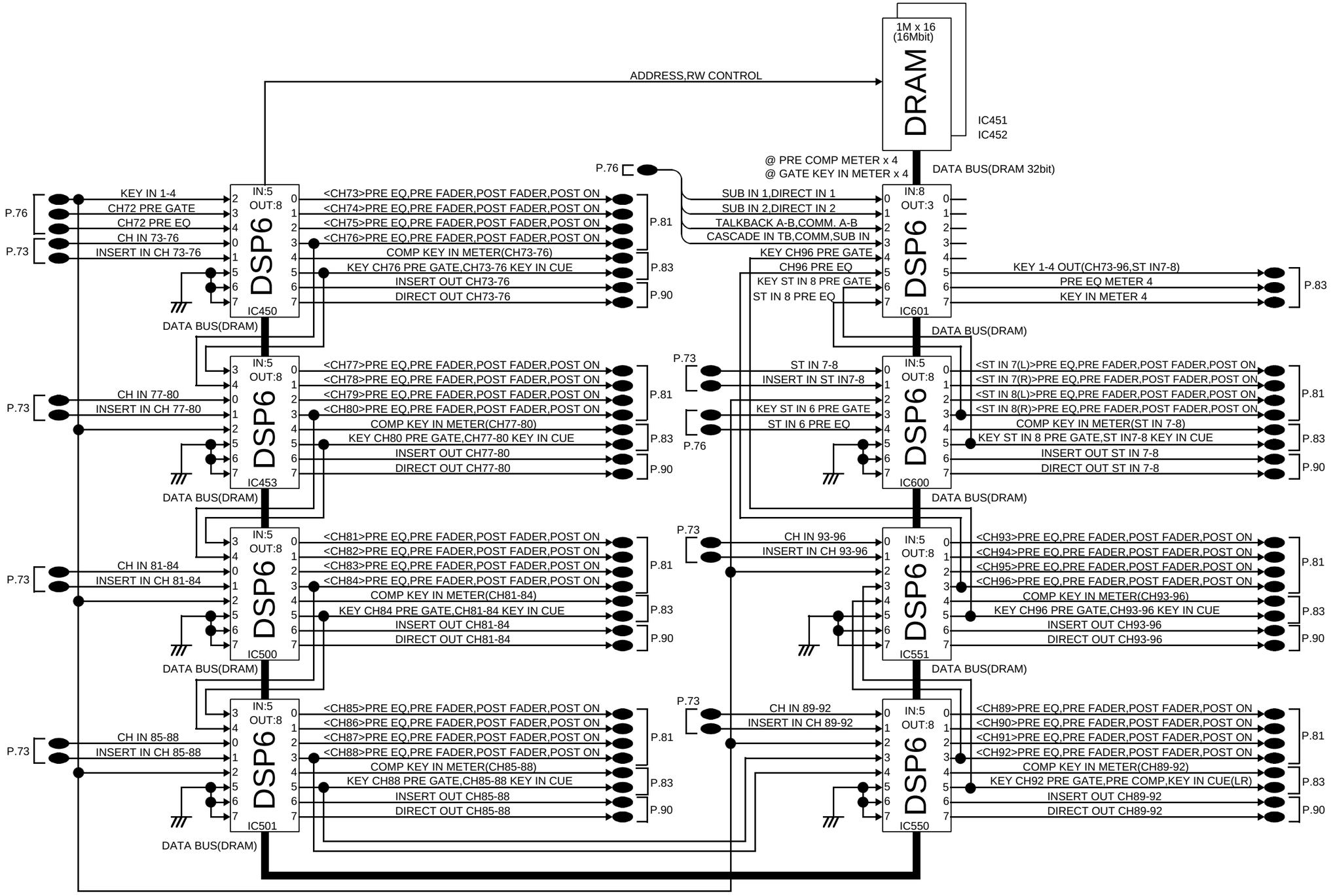

FUNCTION: INPUT EQ/GATE/COMP/DELAY/FADER ON




FUNCTION: INPUT EQ/GATE/COMP/DELAY/FADER ON

(FOR DSP1D-EX)

**IDB (49–96)**

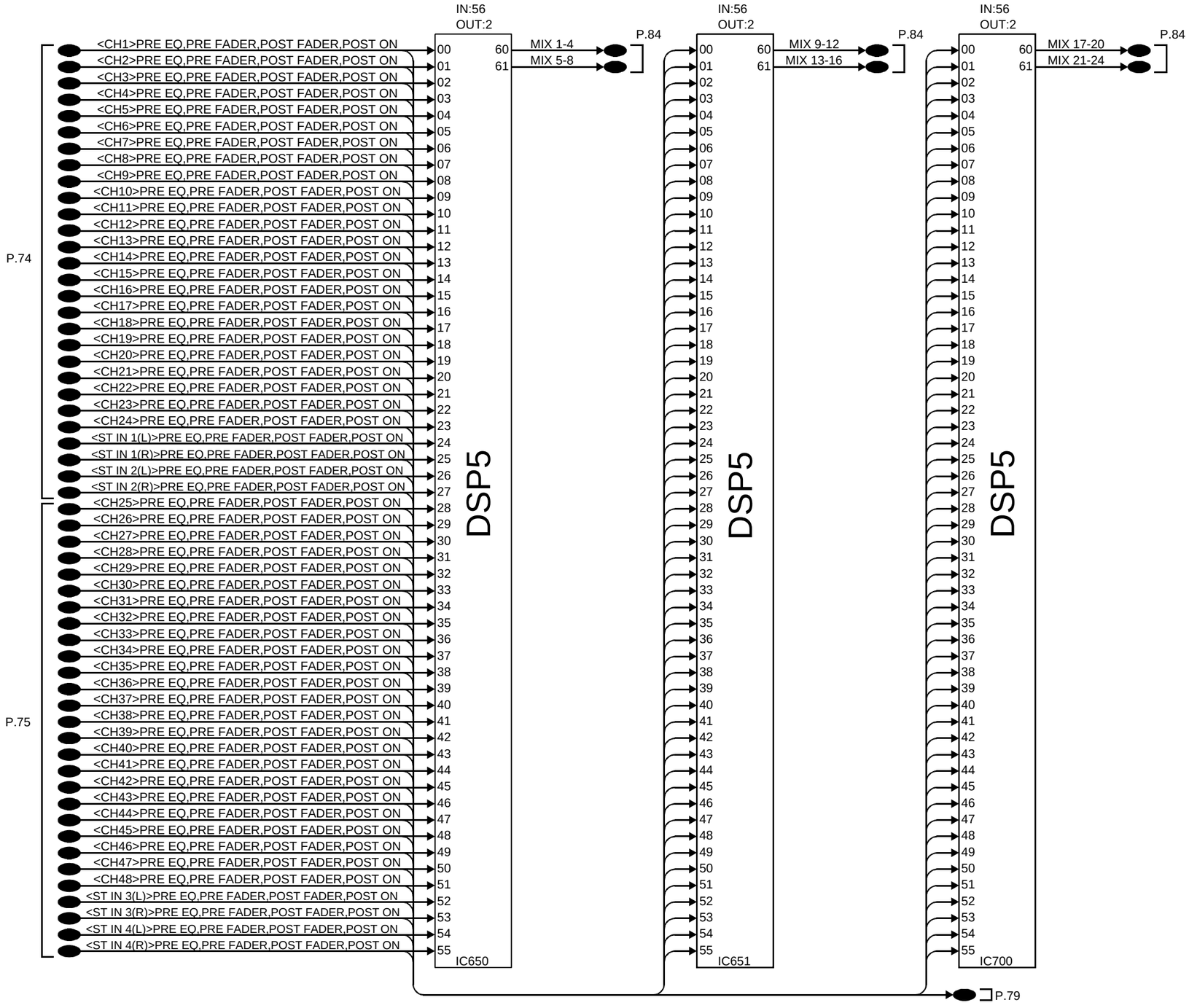



FUNCTION: INPUT EQ/GATE/COMP/DELAY/FADER ON

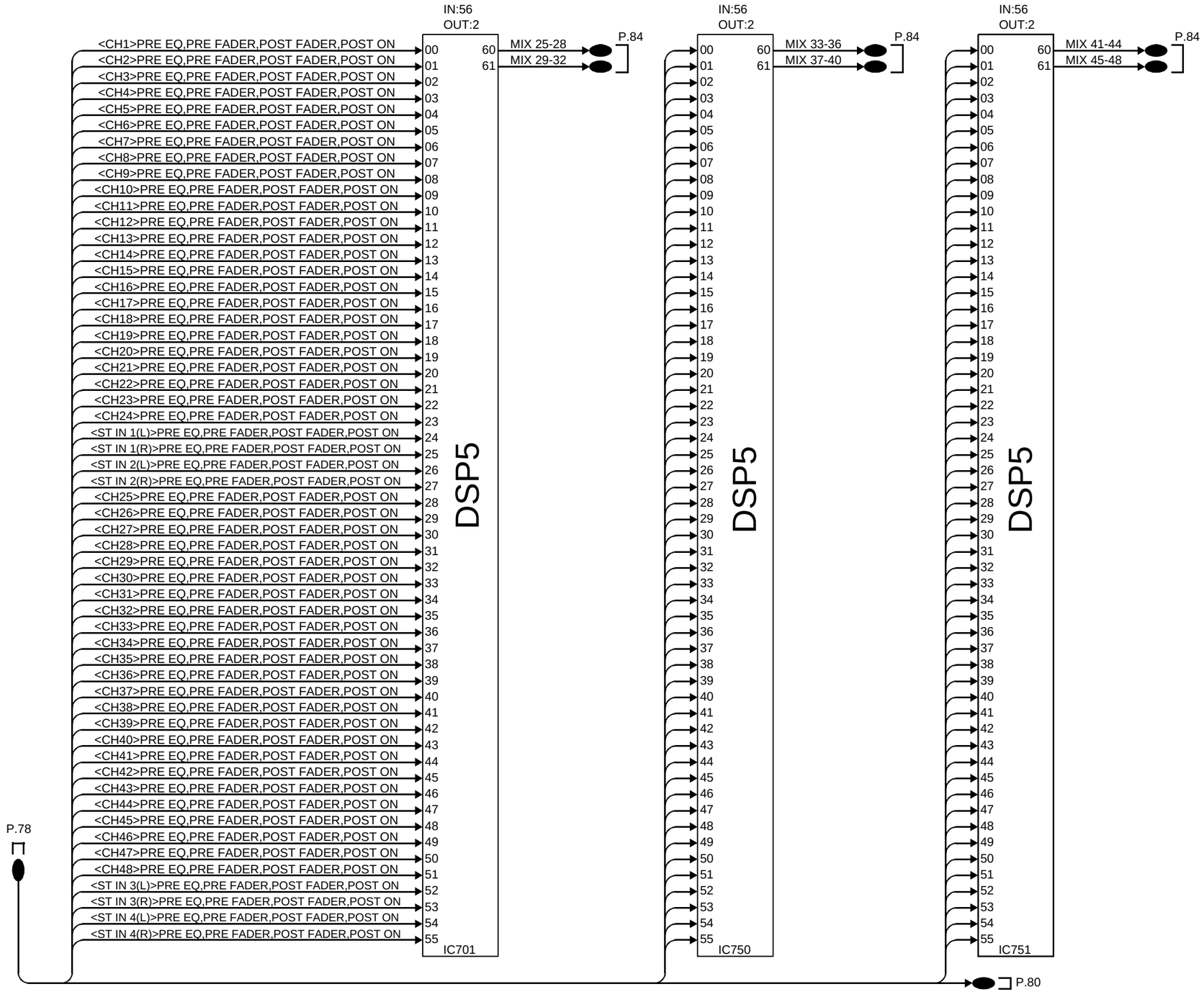
(FOR DSP1D-EX)

**IDB (49–96)**

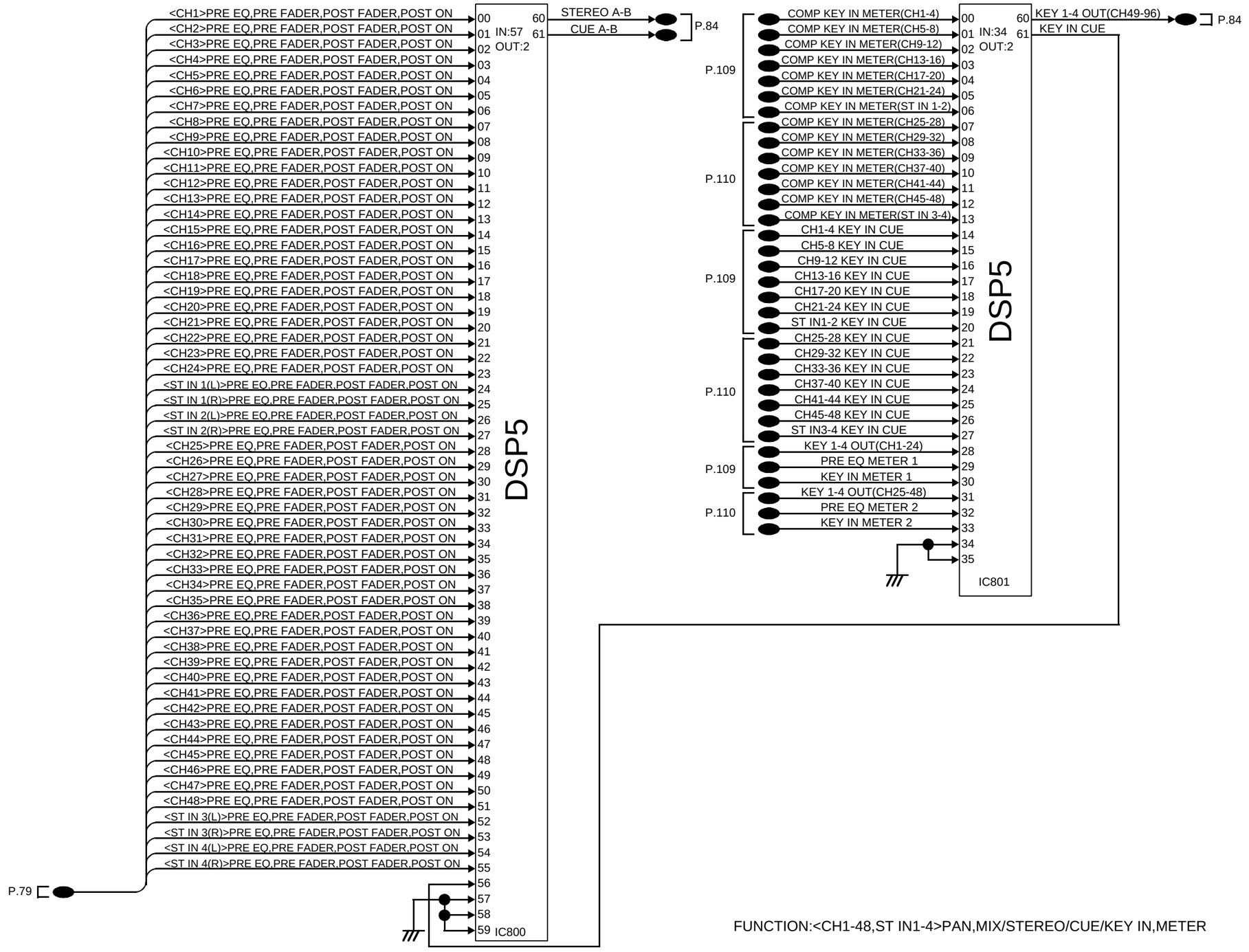
KEC-92538-21



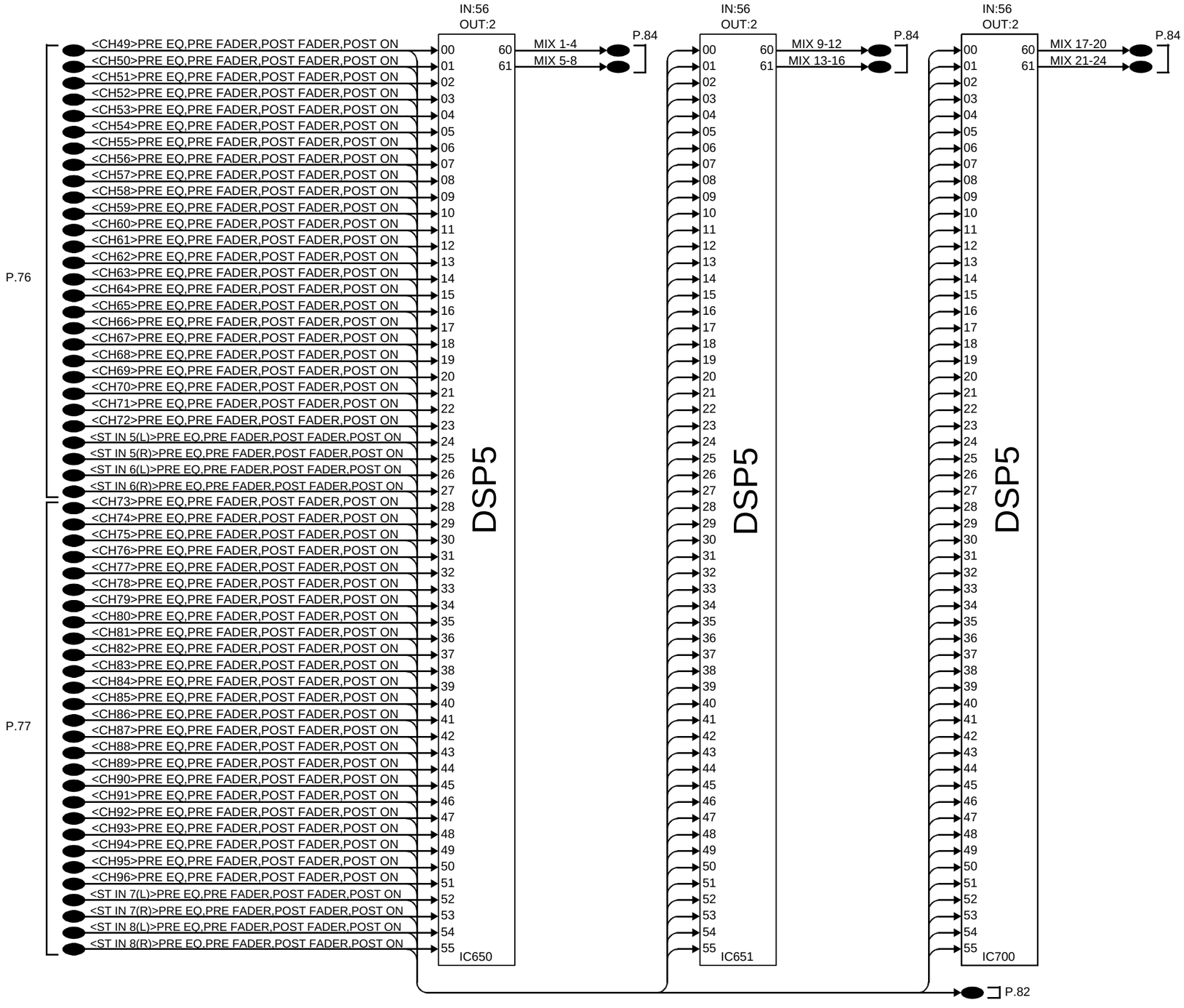

FUNCTION: <CH1-48,ST IN1-4>PAN,MIX/STEREO/CUE/KEY IN,METER




FUNCTION: <CH1-48,ST IN1-4>PAN,MIX/STEREO/CUE/KEY IN,METER




FUNCTION:<CH1-48,ST IN1-4>PAN,MIX/STEREO/CUE/KEY IN,METER

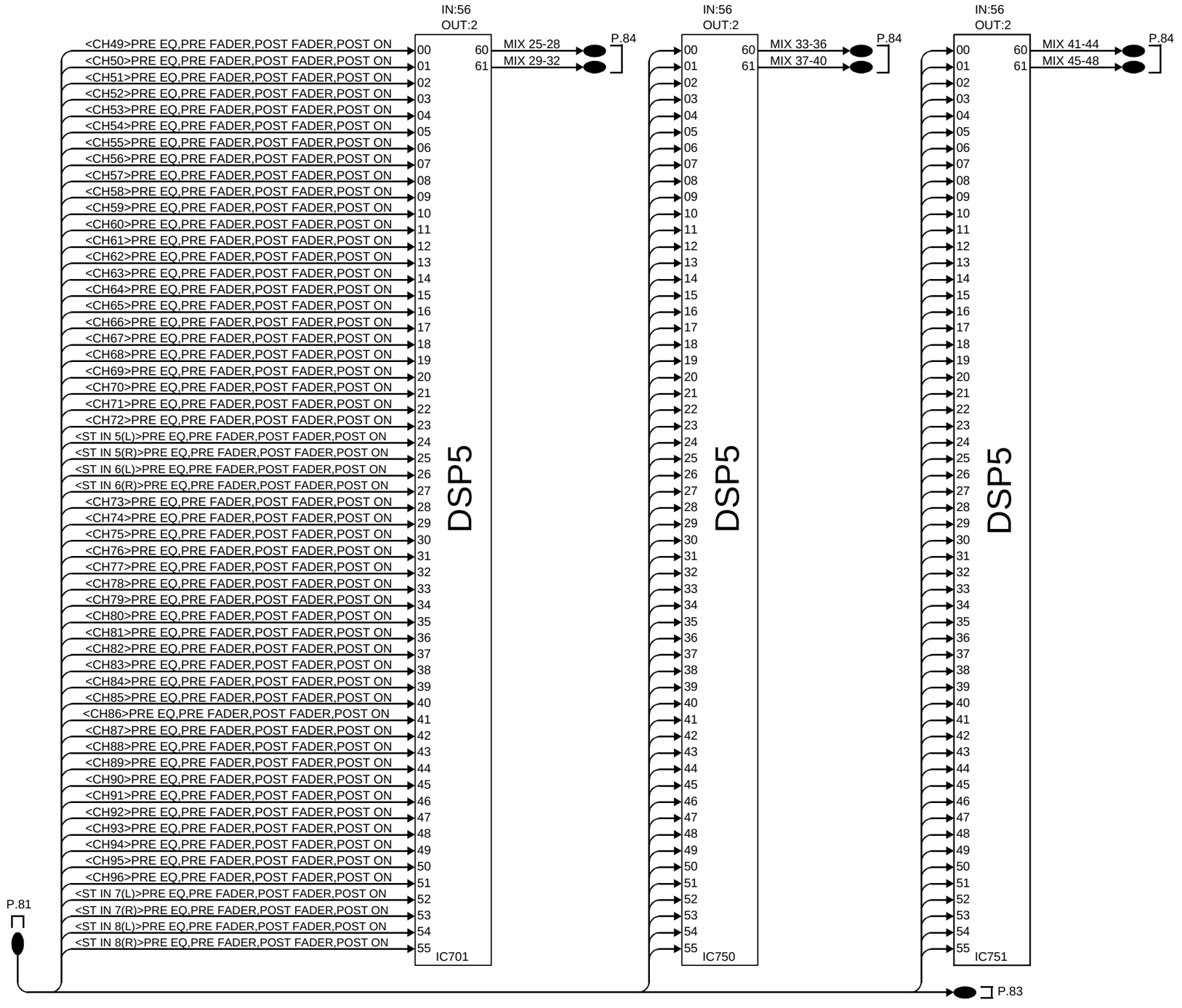



FUNCTION: <CH49-96,ST IN5-8>PAN,MIX/STEREO/CUE/KEY IN,METER

(FOR DSP1D-EX)

**IDB (49–96)**

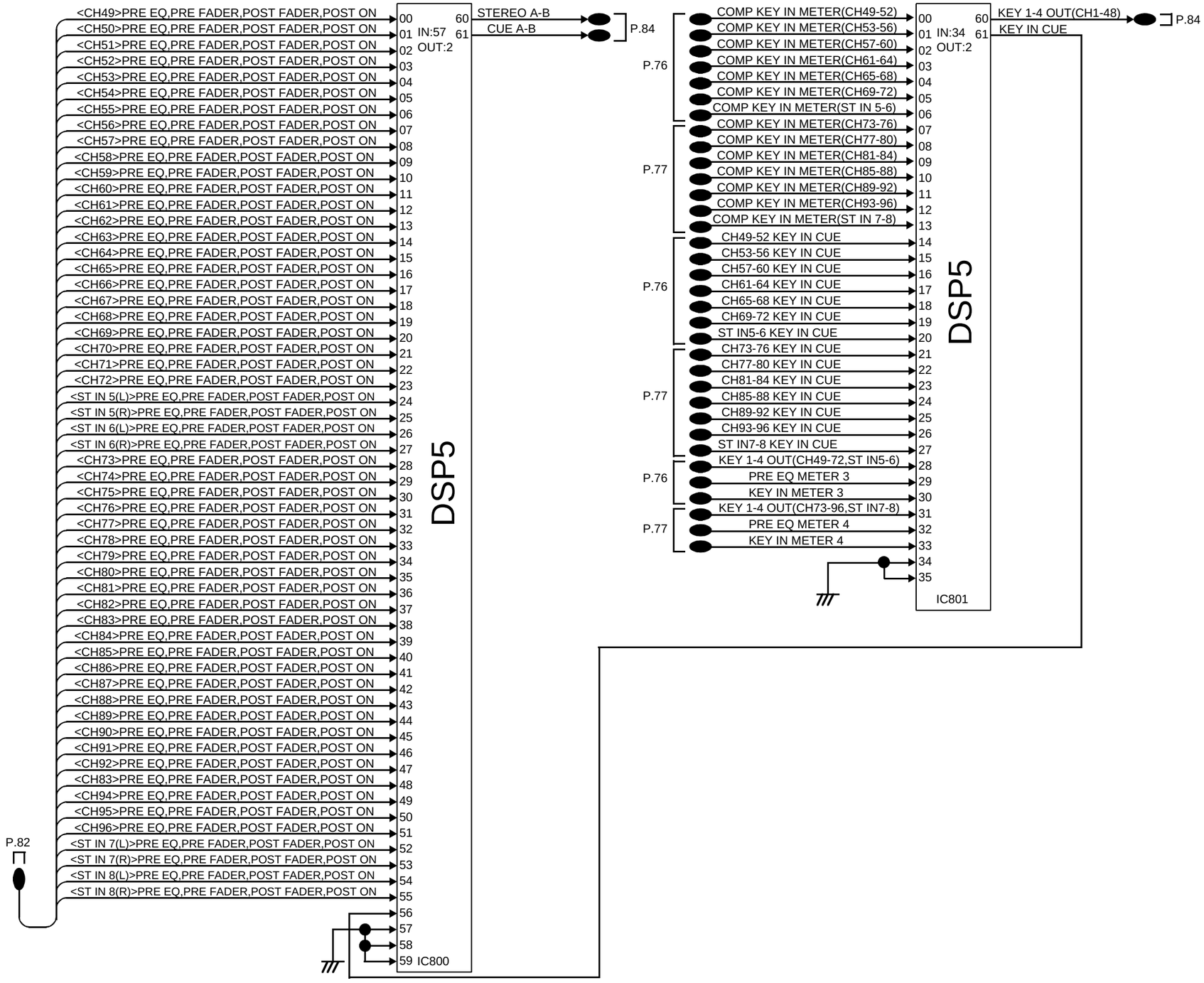
KEC-92538-25




FUNCTION: <CH49-96,ST IN5-8>PAN,MIX/STEREO/CUE/KEY IN,METER

(FOR DSP1D-EX)

**IDB (49–96)**

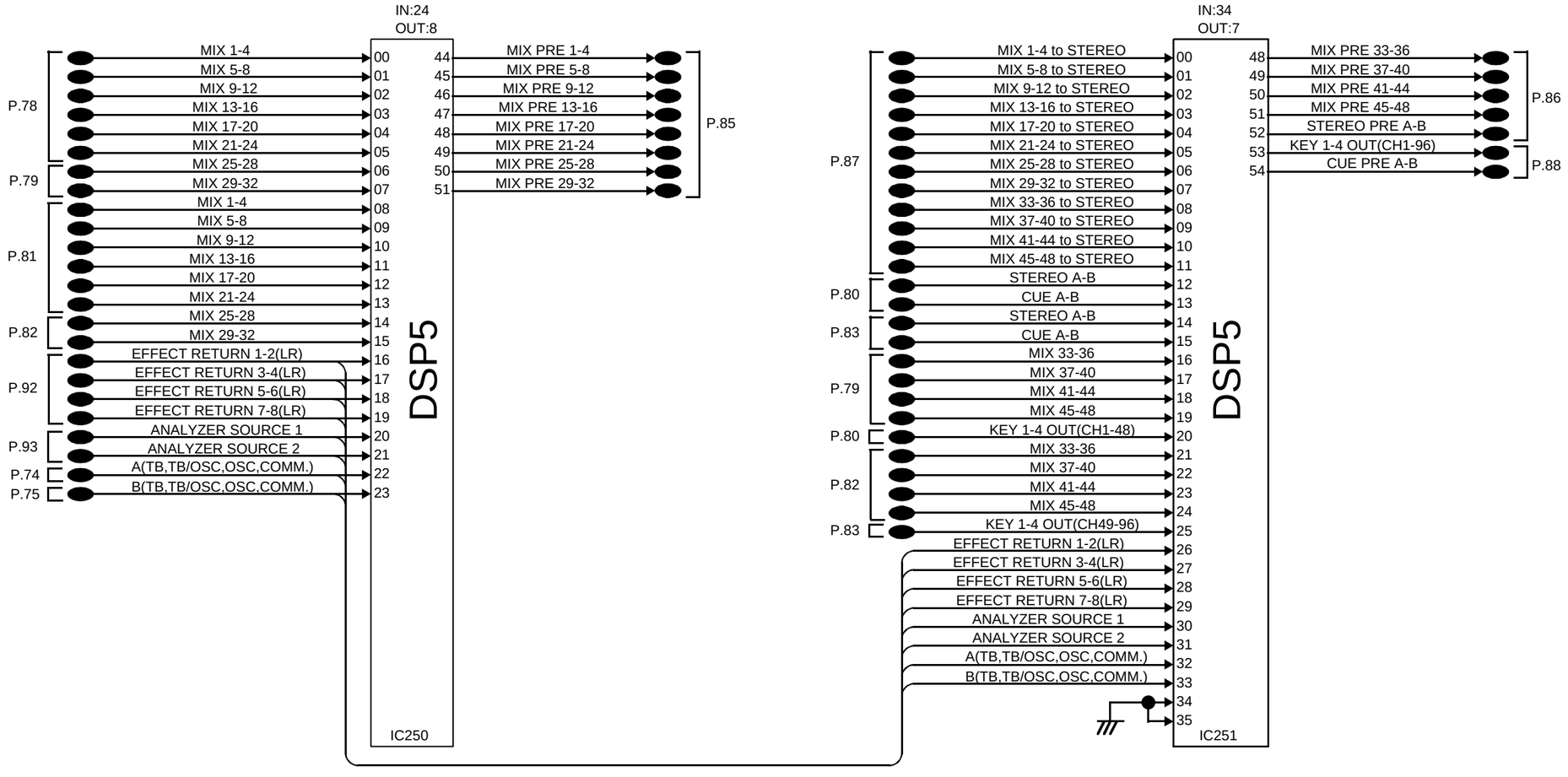



FUNCTION: <CH49-96,ST IN5-8>PAN,MIX/STEREO/CUE/KEY IN,METER

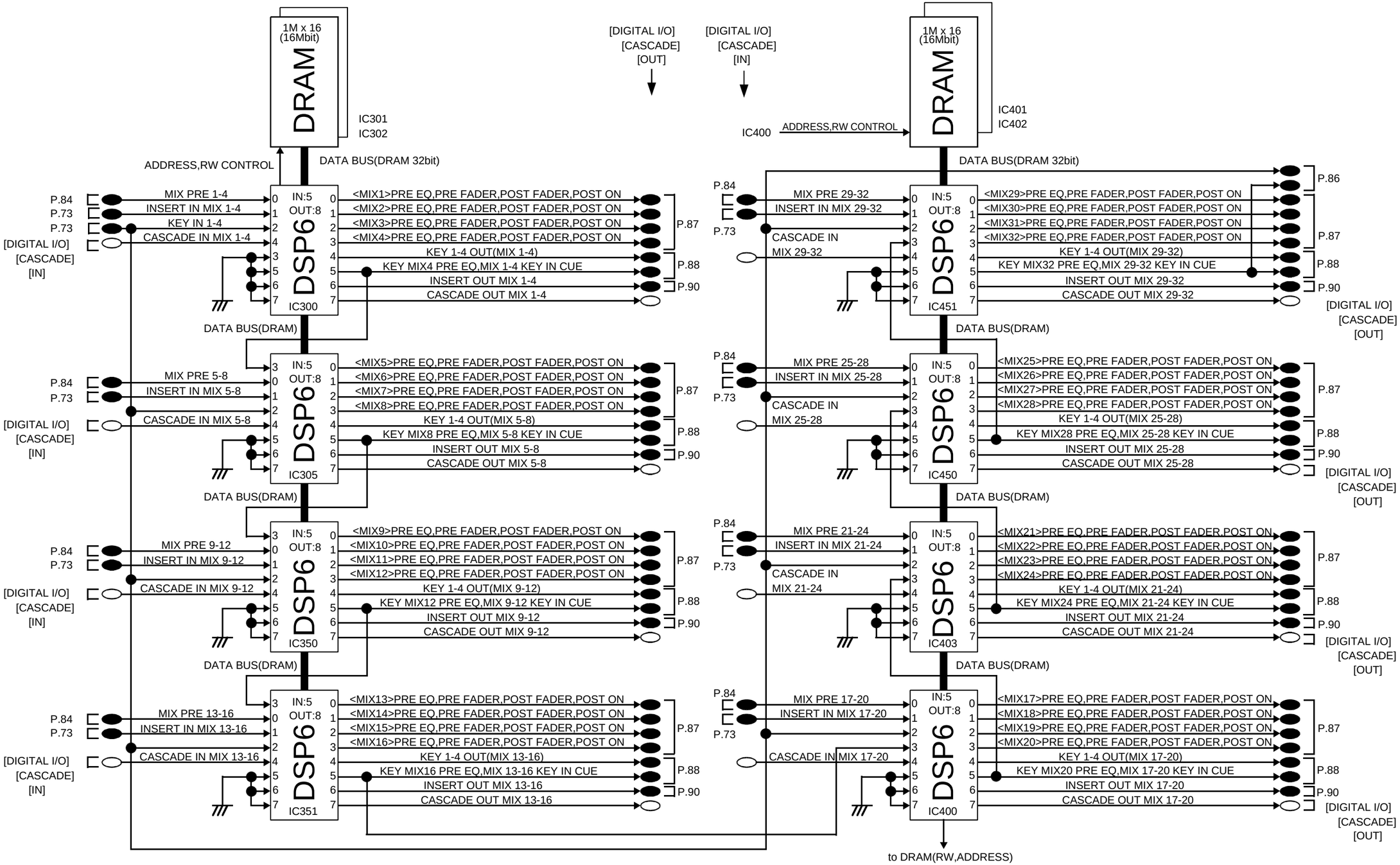
(FOR DSP1D-EX)

**IDB (49–96)**

KEC-92538-27



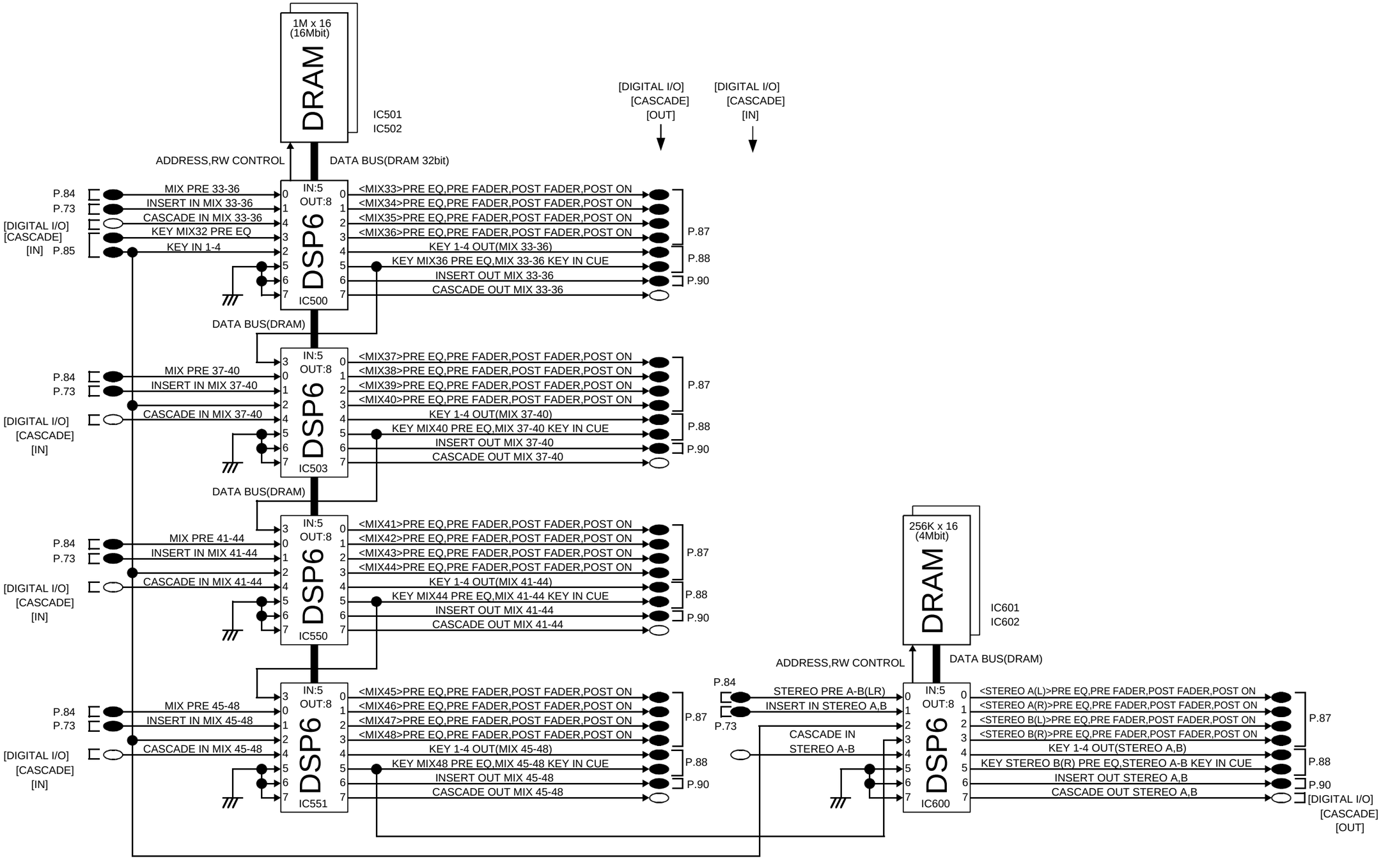

FUNCTION: MIX/STEREO/CUE/KEY IN




FUNCTION: MIX EQ/COMP/DELAY/FADER ON

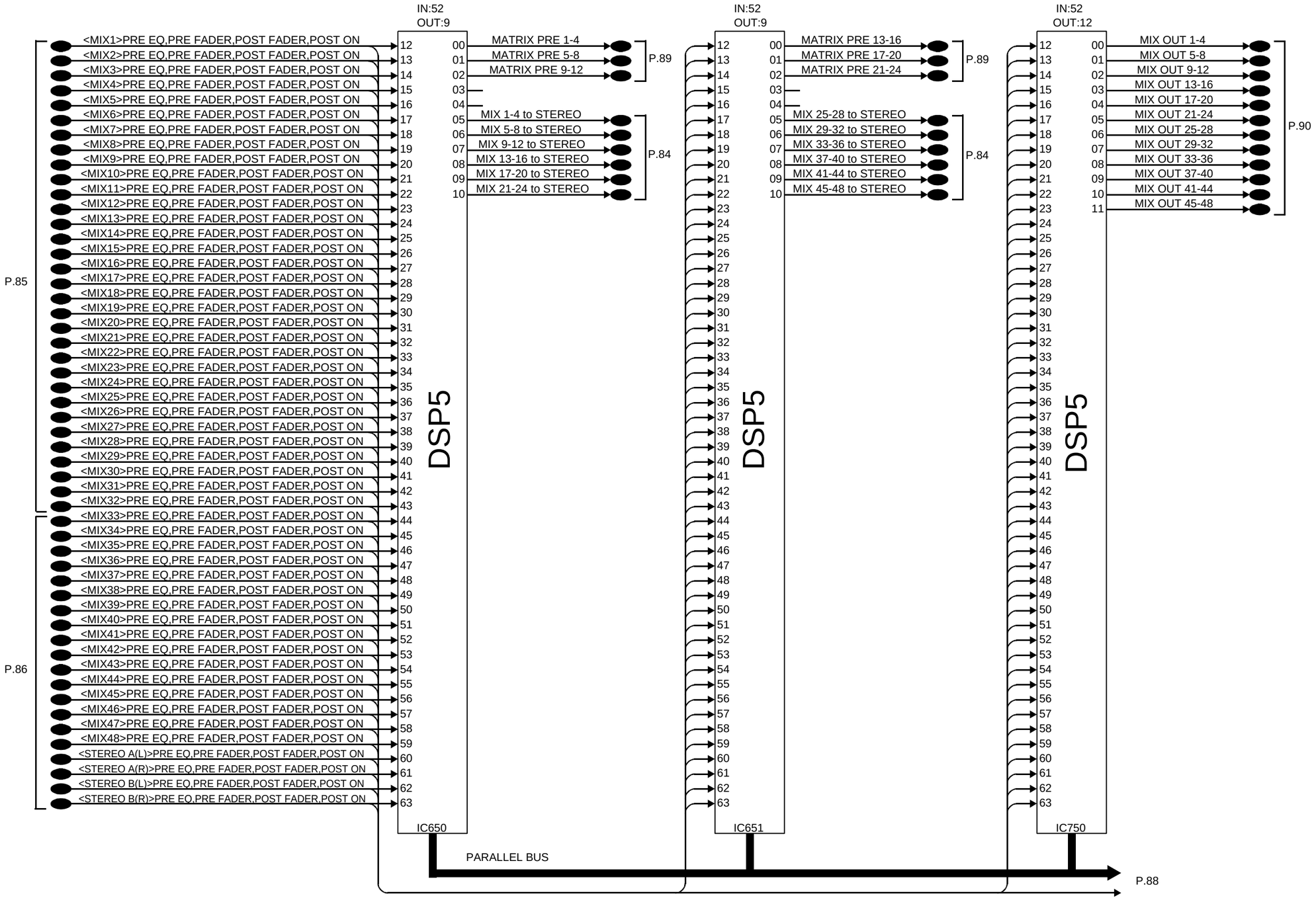
GDB

KEC-92538-29

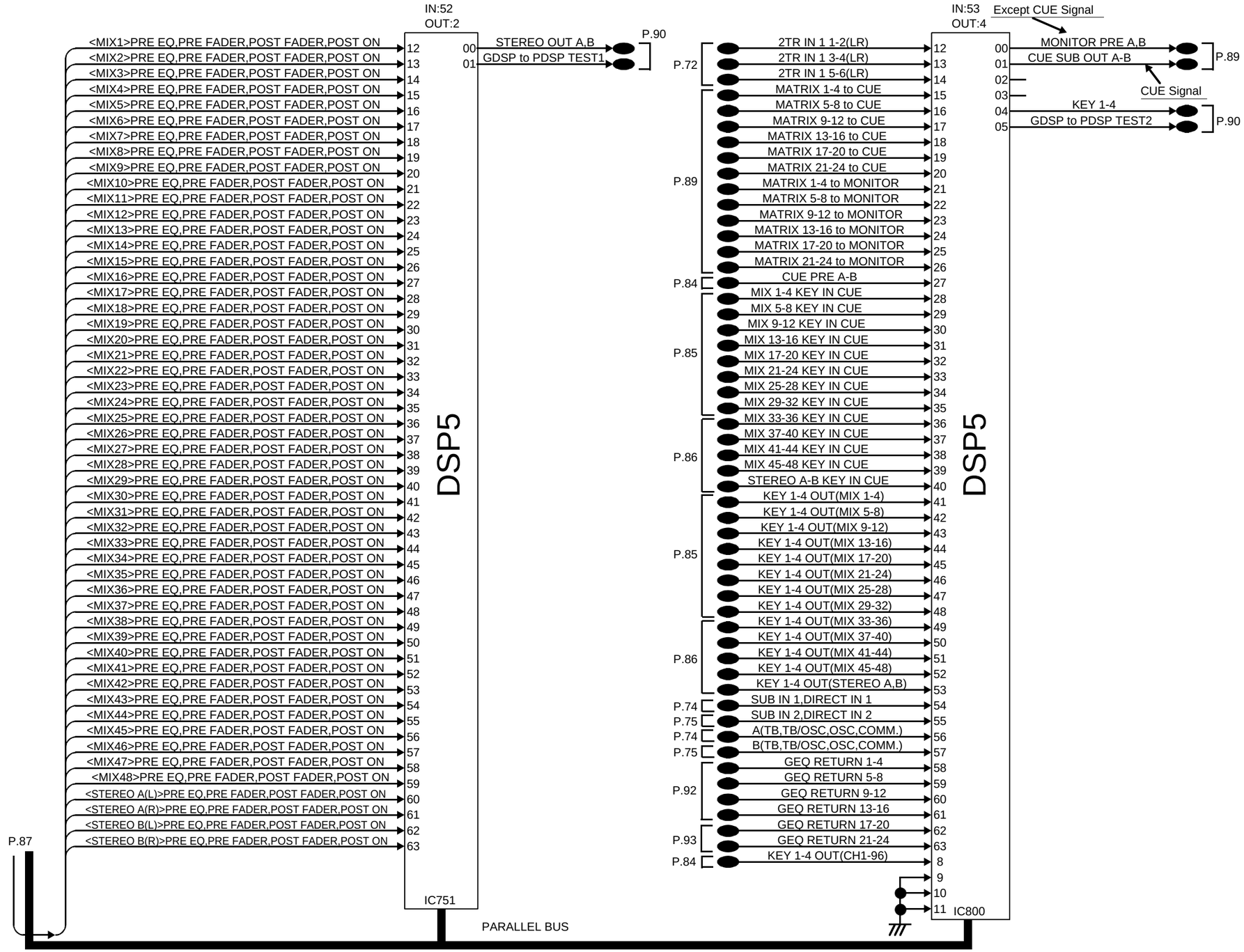



FUNCTION: MIX EQ/COMP/DELAY/FADER ON

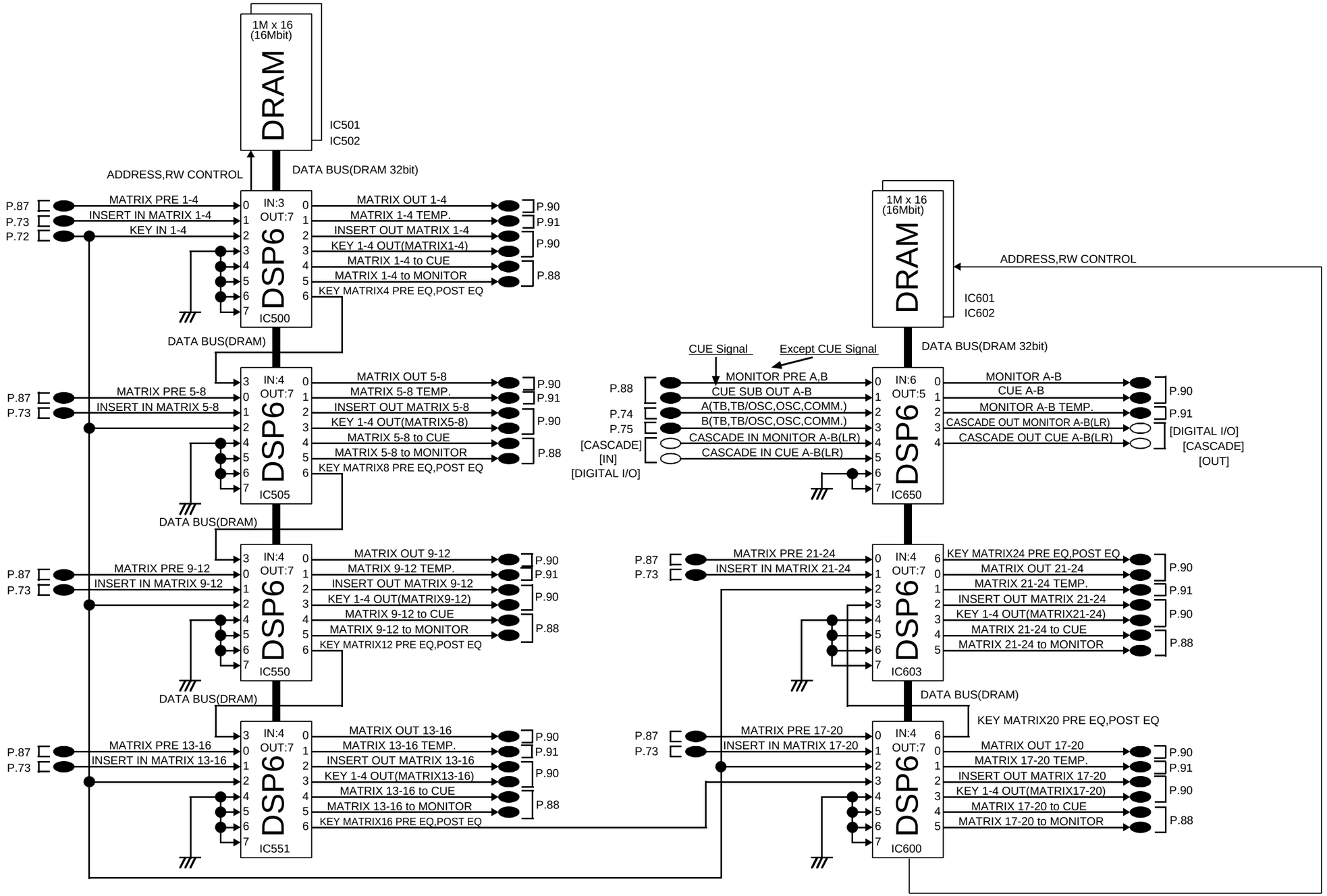
GDB




FUNCTION: MATRIX,CUE/MONITOR ADD.,KEY IN



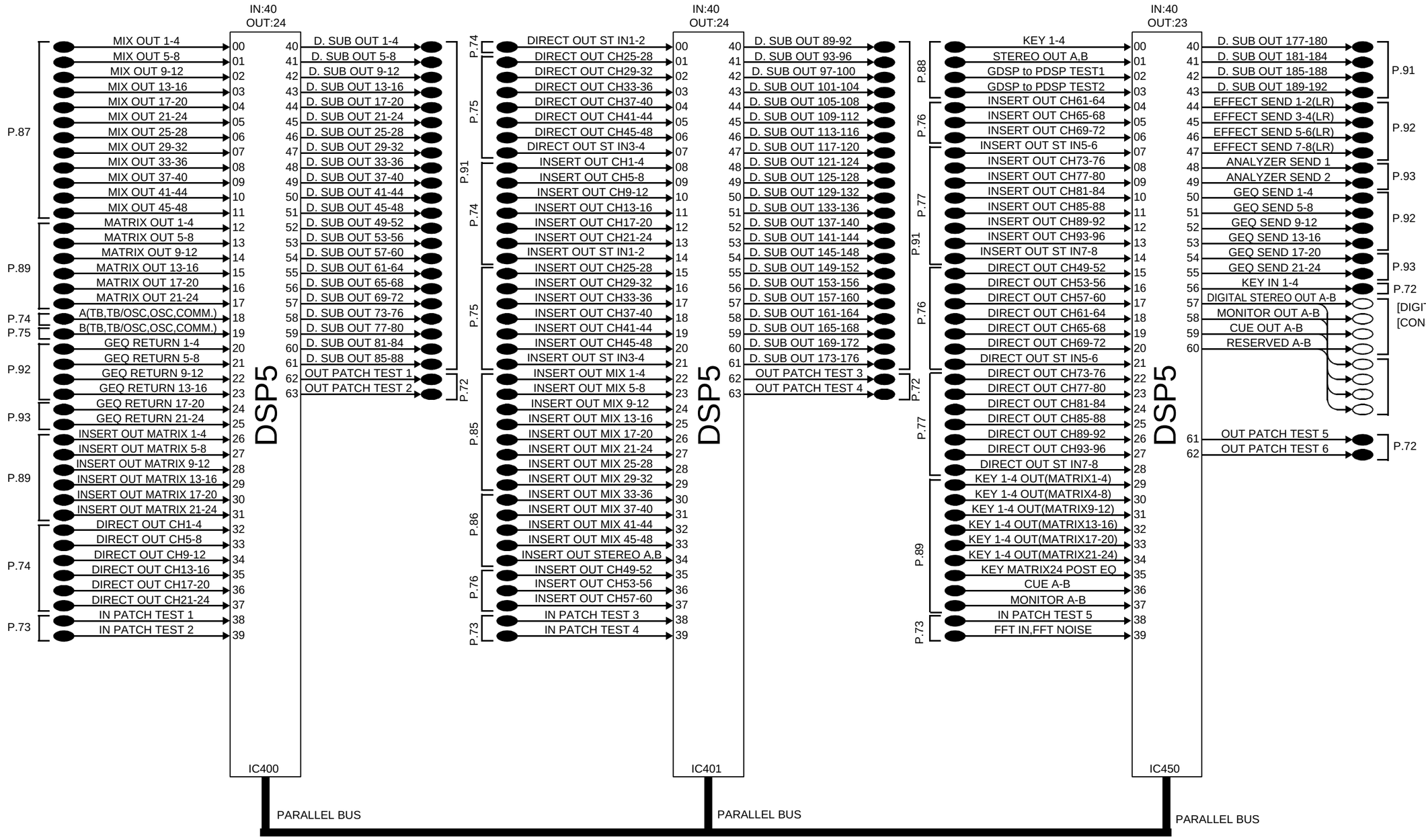

FUNCTION: MATRIX,CUE/MONITOR ADD.,KEY IN




FUNCTION: MATRIX EQ/COMP/DELAY/FADER ON,MONITOR DELAY

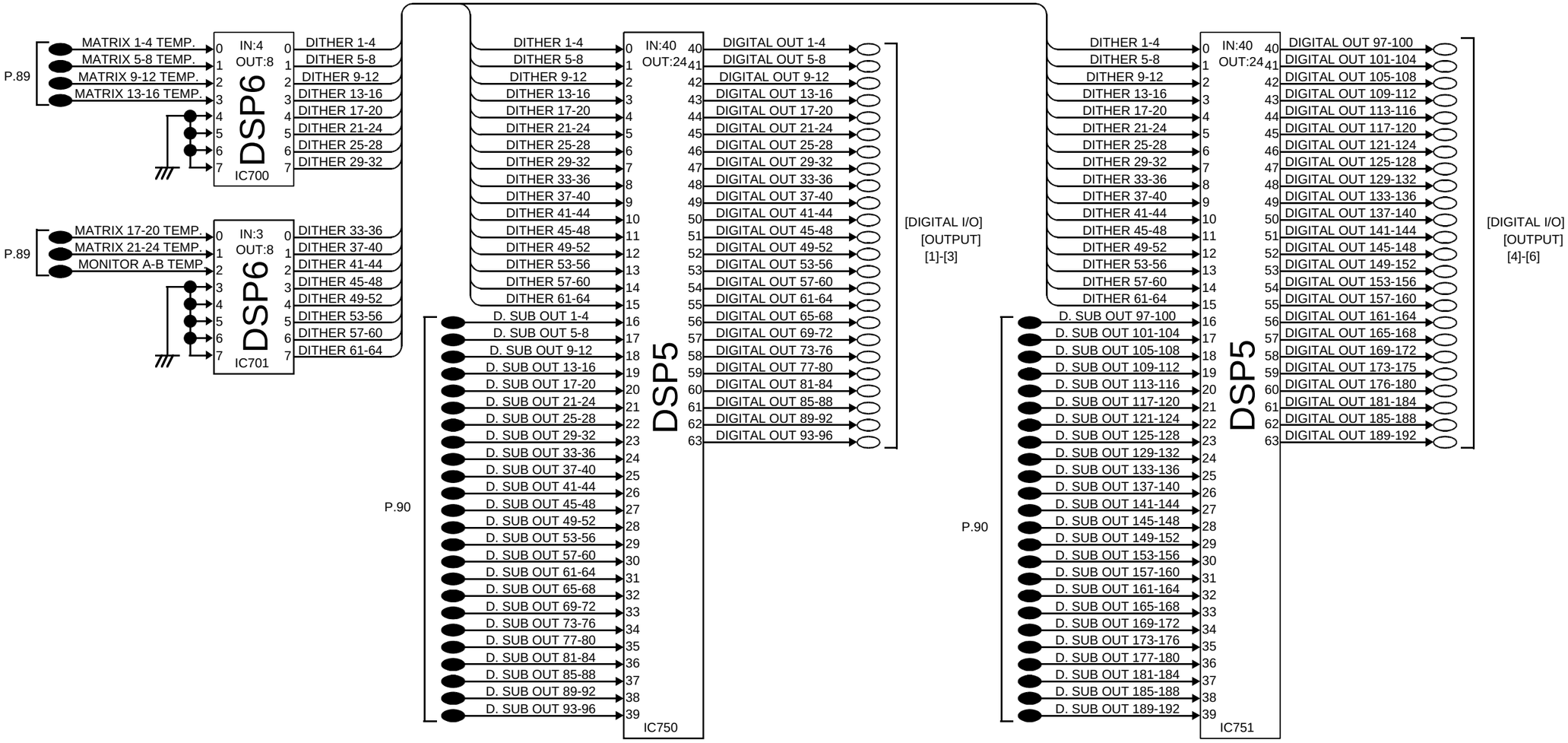
PDB

KEC-92538-33

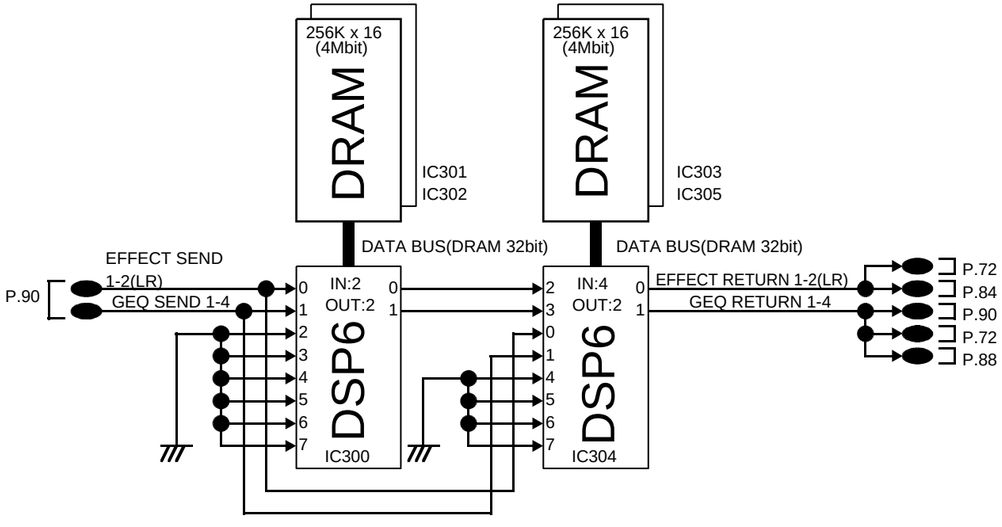


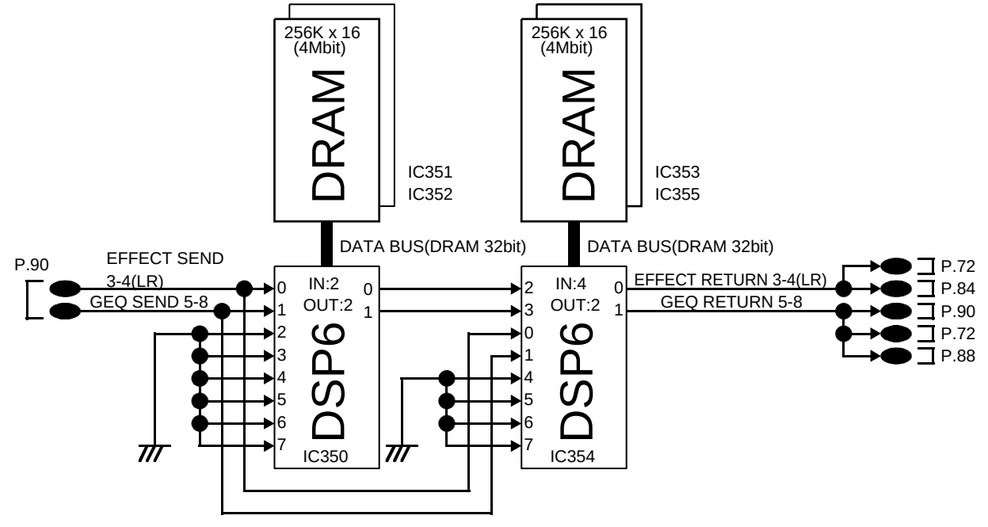

FUNCTION: OUTPUT PATCH, PEAK METER

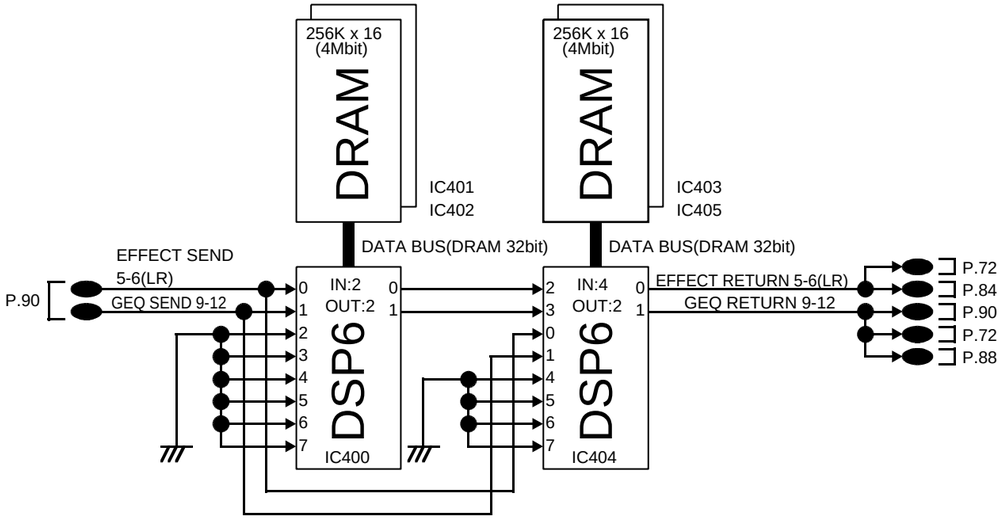
PDB

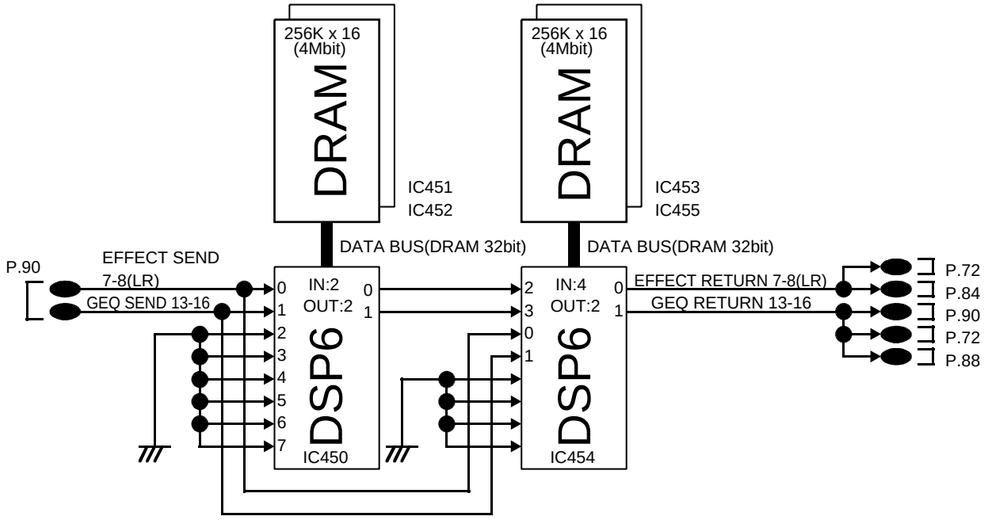



FUNCTION: DITHER

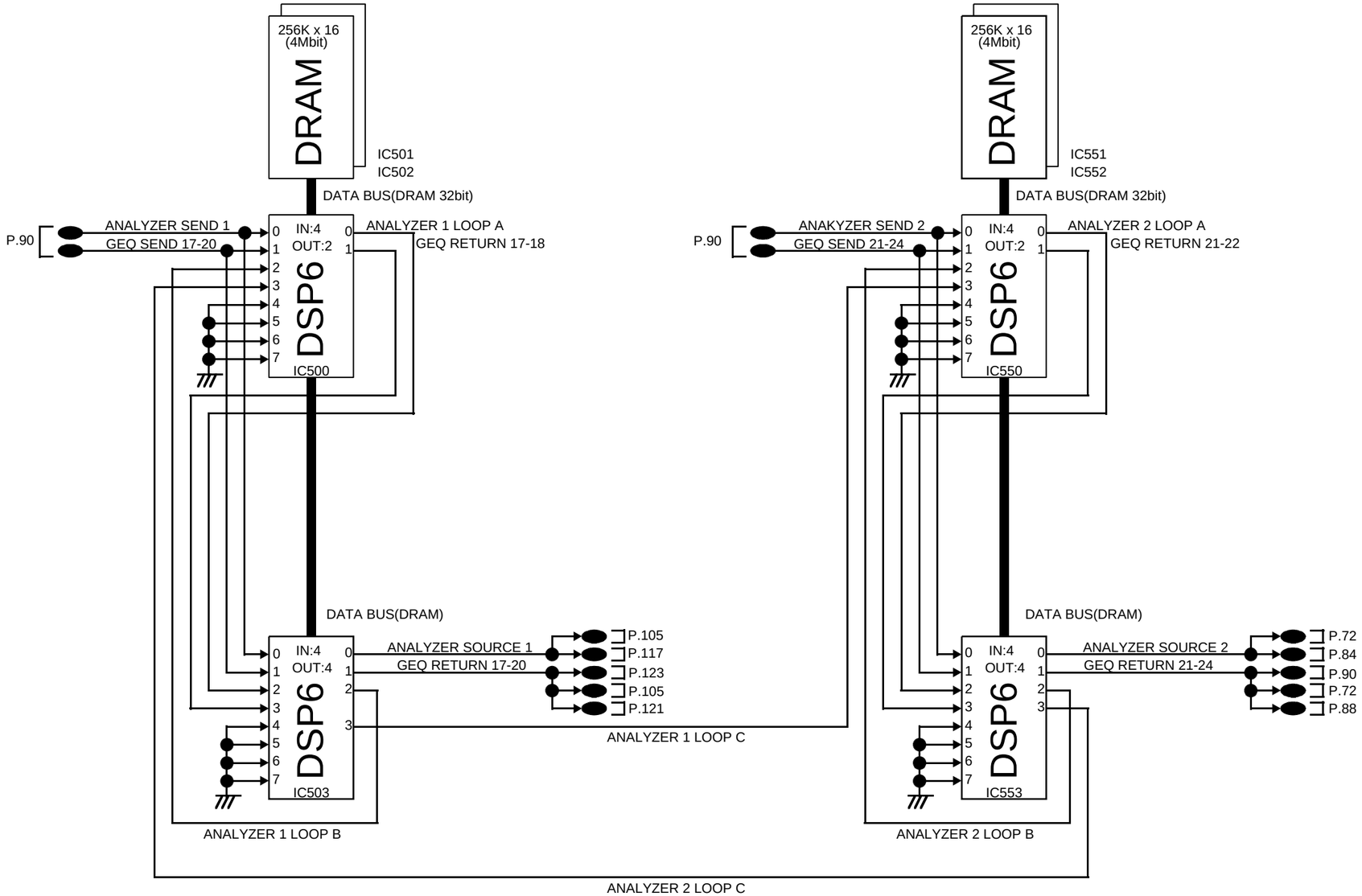



FUNCTION: EFFECT,GEQ


256K x 16
(4Mbit)
DRAM
IC501
IC502
DATA BUS(DRAM 32bit)
P.90
ANALYZER SEND 1
GEQ SEND 17-20
IN:4
OUT:2
DSP6
IC500
ANALYZER 1 LOOP A
GEQ RETURN 17-18
DATA BUS(DRAM)
IN:4
OUT:4
DSP6
IC503
ANALYZER SOURCE 1
GEQ RETURN 17-20
P.105
P.117
P.123
P.105
P.121
ANALYZER 1 LOOP C
ANALYZER 1 LOOP B
256K x 16
(4Mbit)
DRAM
IC551
IC552
DATA BUS(DRAM 32bit)
P.90
ANAKYZER SEND 2
GEQ SEND 21-24
IN:4
OUT:2
DSP6
IC550
ANALYZER 2 LOOP A
GEQ RETURN 21-22
DATA BUS(DRAM)
IN:4
OUT:4
DSP6
IC553
ANALYZER SOURCE 2
GEQ RETURN 21-24
P.72
P.84
P.90
P.72
P.88
ANALYZER 2 LOOP B
ANALYZER 2 LOOP C