

DSP UNIT


DSP *LD*

CIRCUIT DIAGRAM

■ CONTENTS

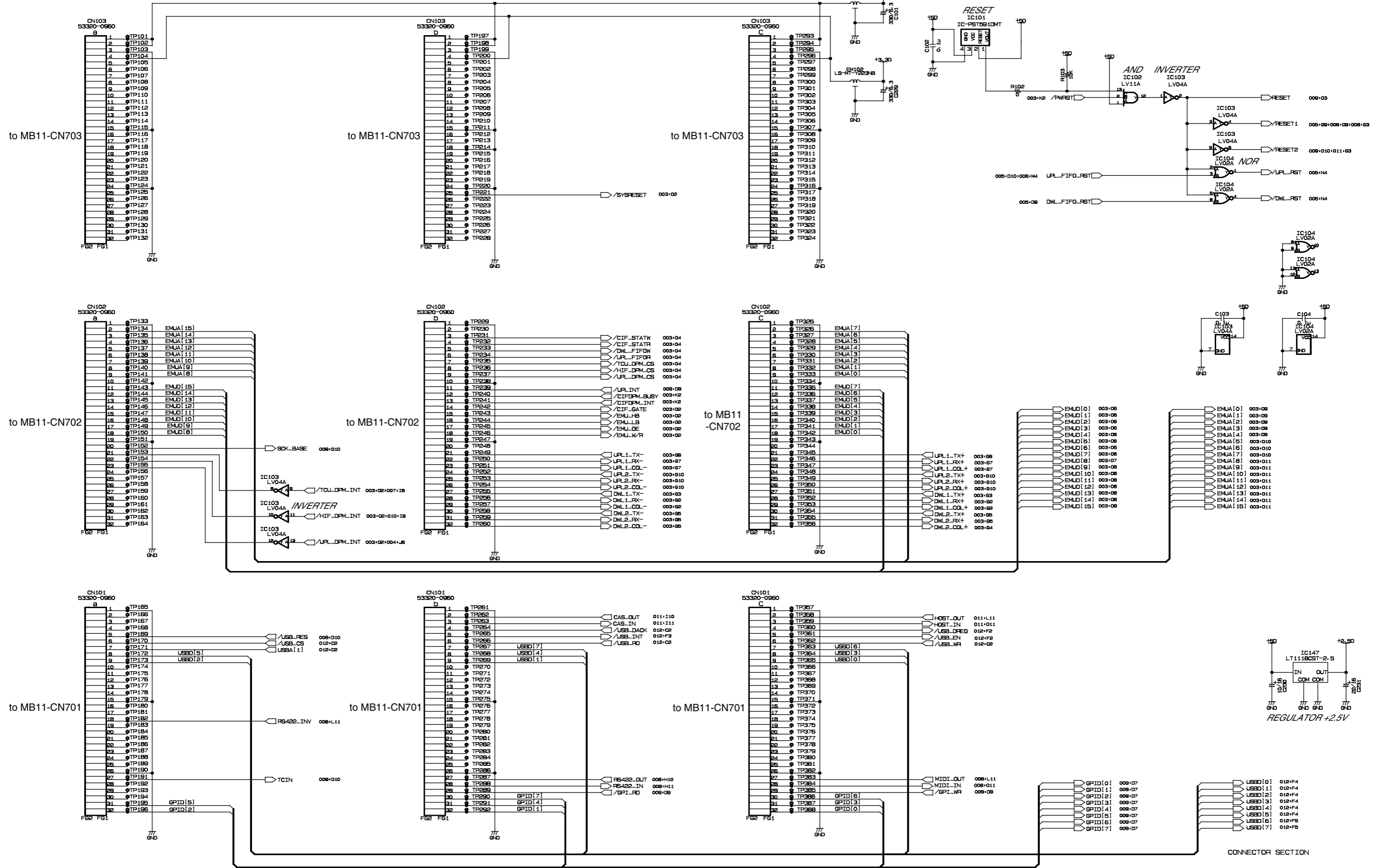
CIB.....	3
EDB.....	14
EMB.....	25
GDB.....	35
IDB.....	51
IFC1.....	69
JK1.....	76
JK2.....	79
JK3.....	82
JK4.....	86
JK5.....	89
JK6.....	91
LED2.....	93
MB11.....	94
PDB.....	97
PSB.....	116
DSP-DC CONNECTOR DIAGRAM.....	117

■ WARNING

Components having special characteristics are marked  and must be replaced with parts having specification equal to those originally installed.

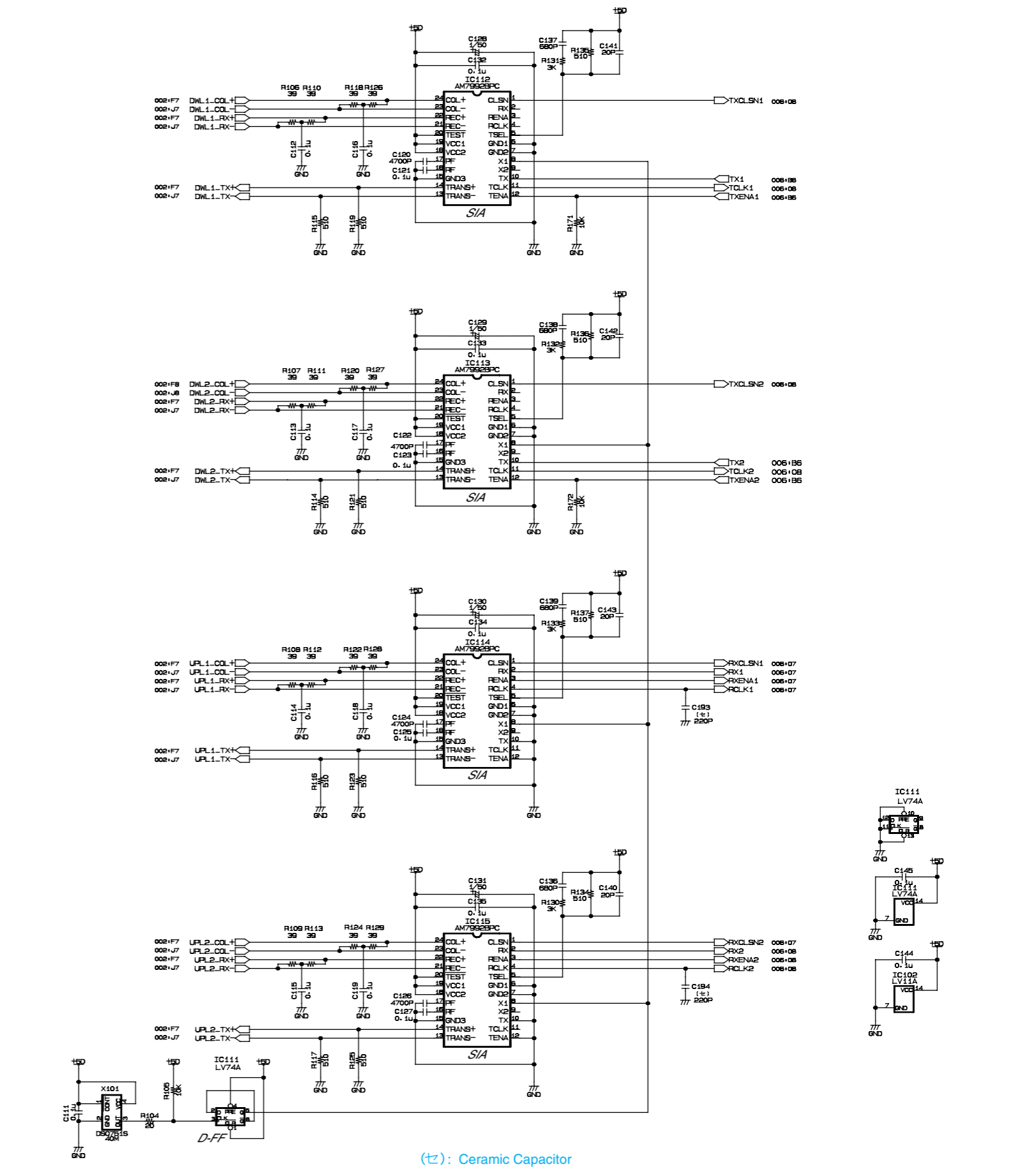
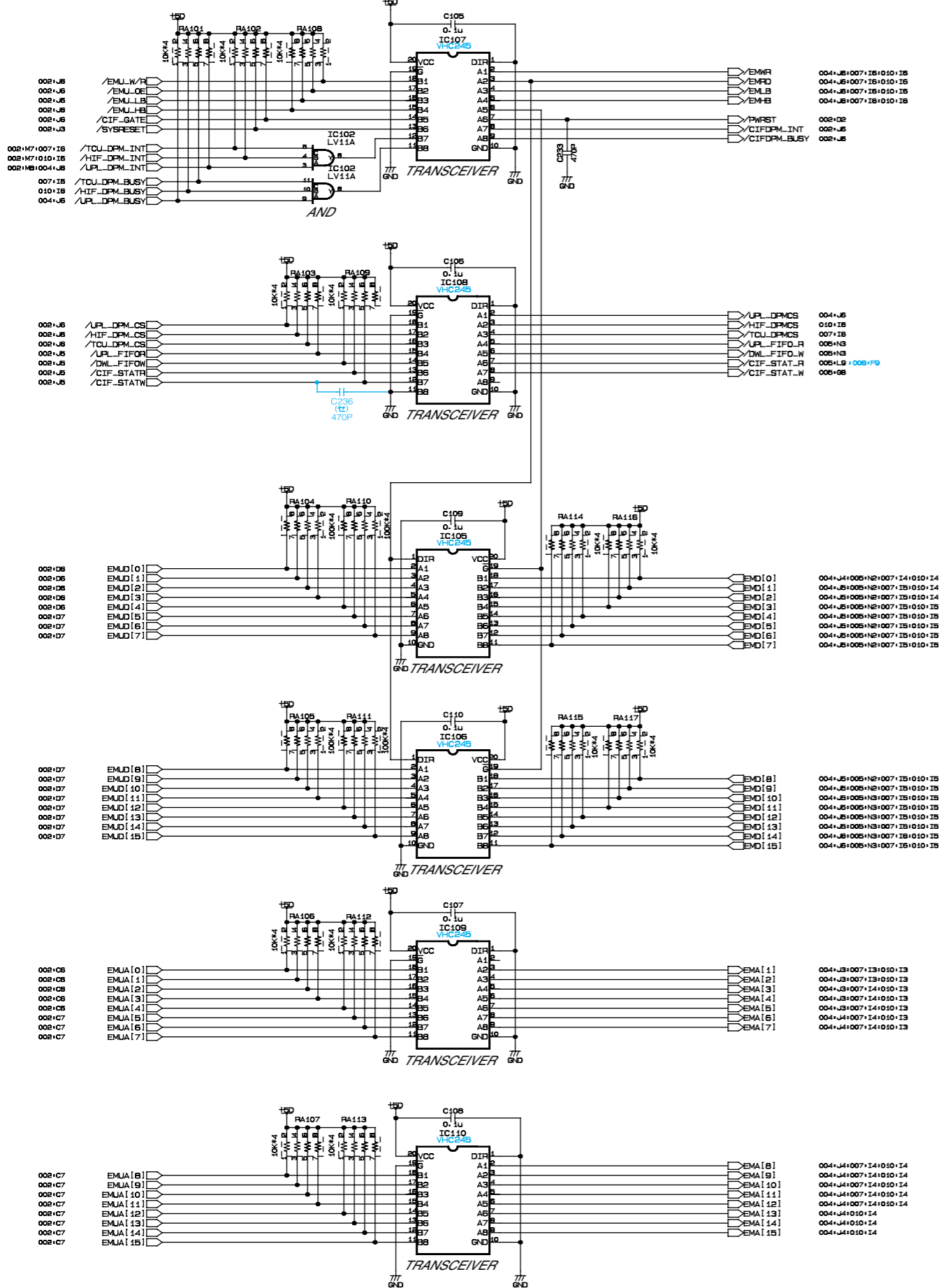
CIB CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D



CIB CIRCUIT DIAGRAM 003 (DSP1D)

DSP1D

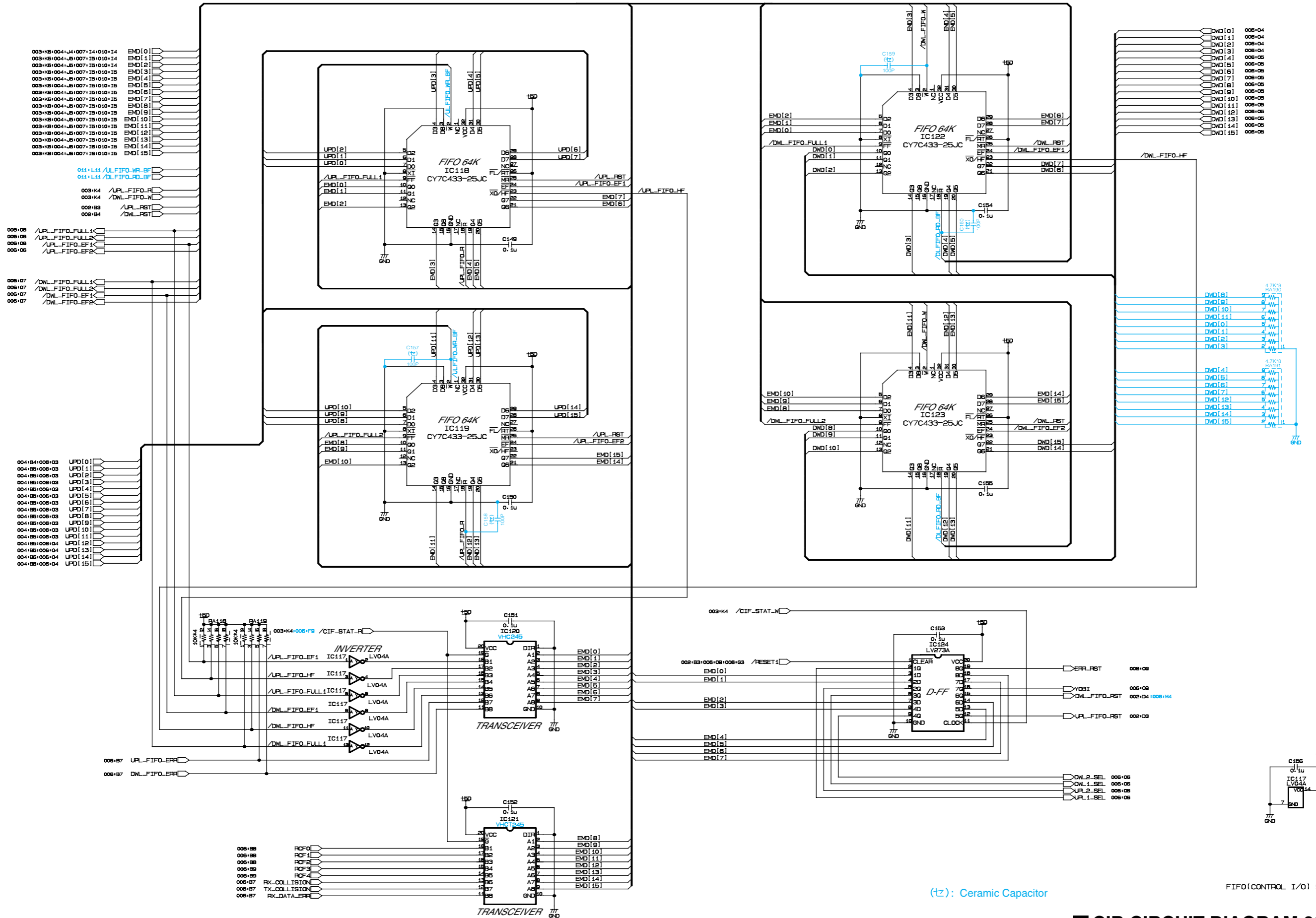


(C): Ceramic Capacitor

CIB CIRCUIT DIAGRAM 003 (DSP1D)

■ CIB CIRCUIT DIAGRAM 005 (DSP1D)

DSP1D

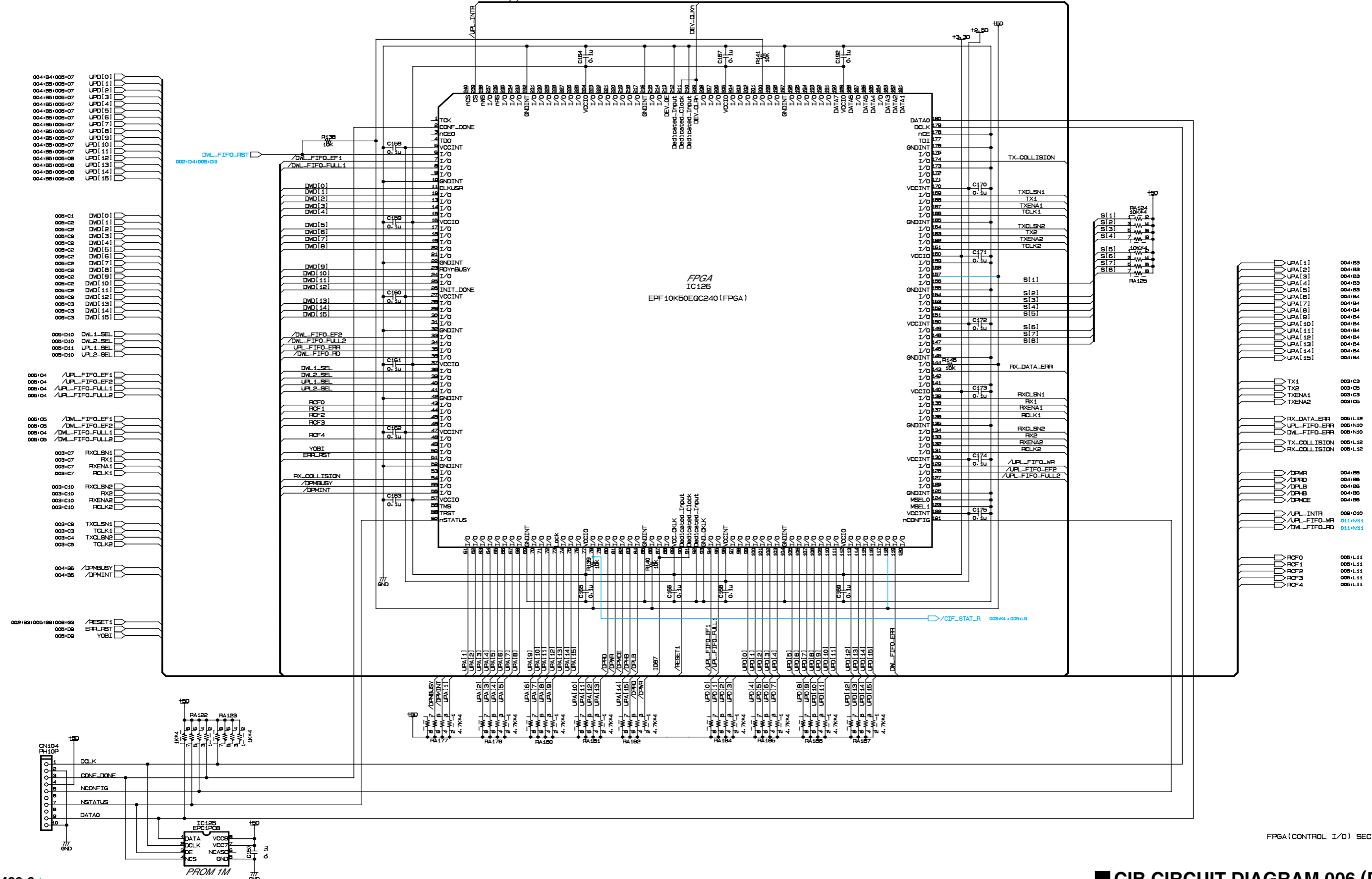


(t): Ceramic Capacitor

FIFO (CONTROL I/O) SECTION

■ CIB CIRCUIT DIAGRAM 006 (DSP1D)

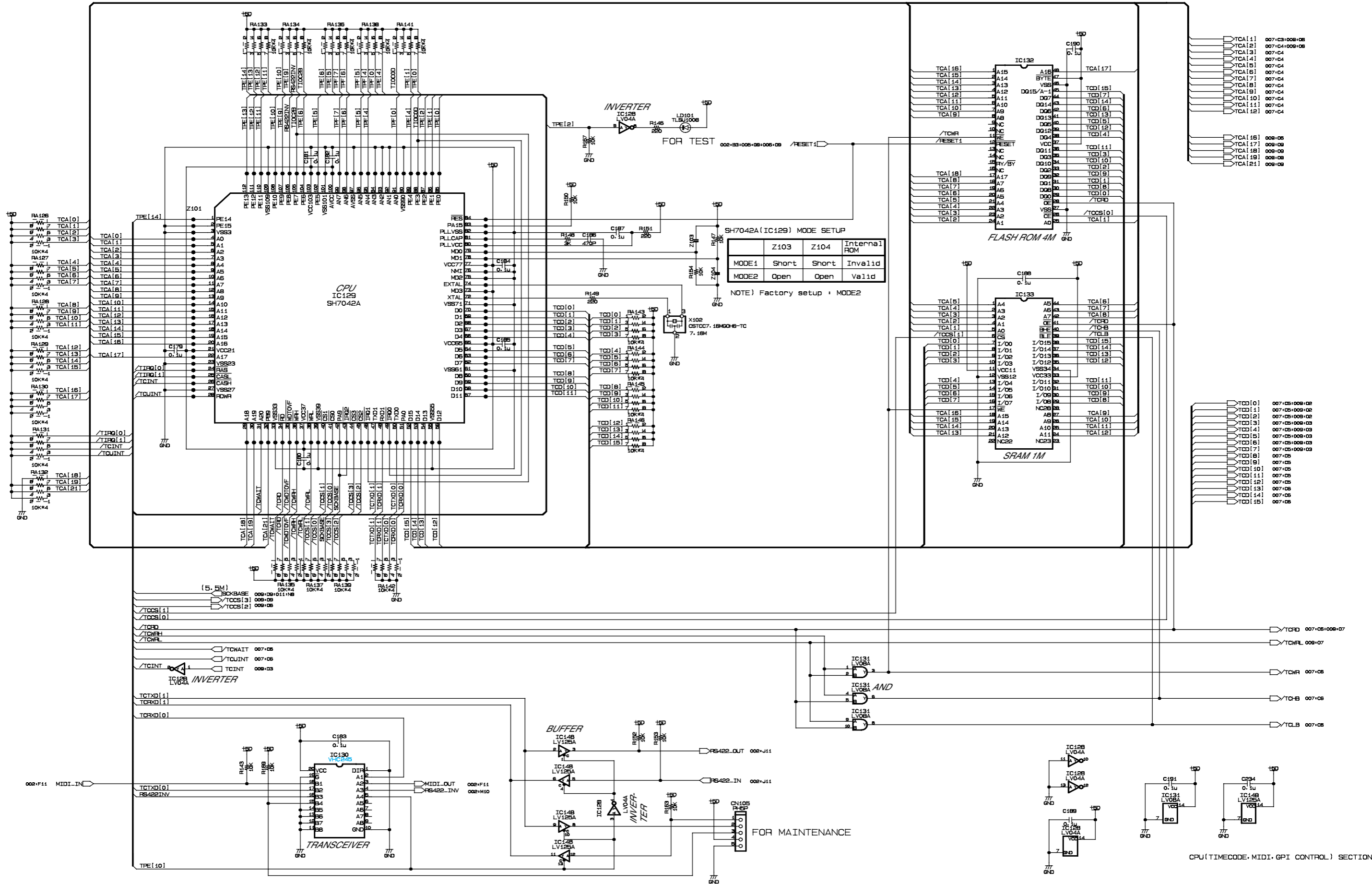
DSP1D



FPGA (CONTROL I/O) SECTION

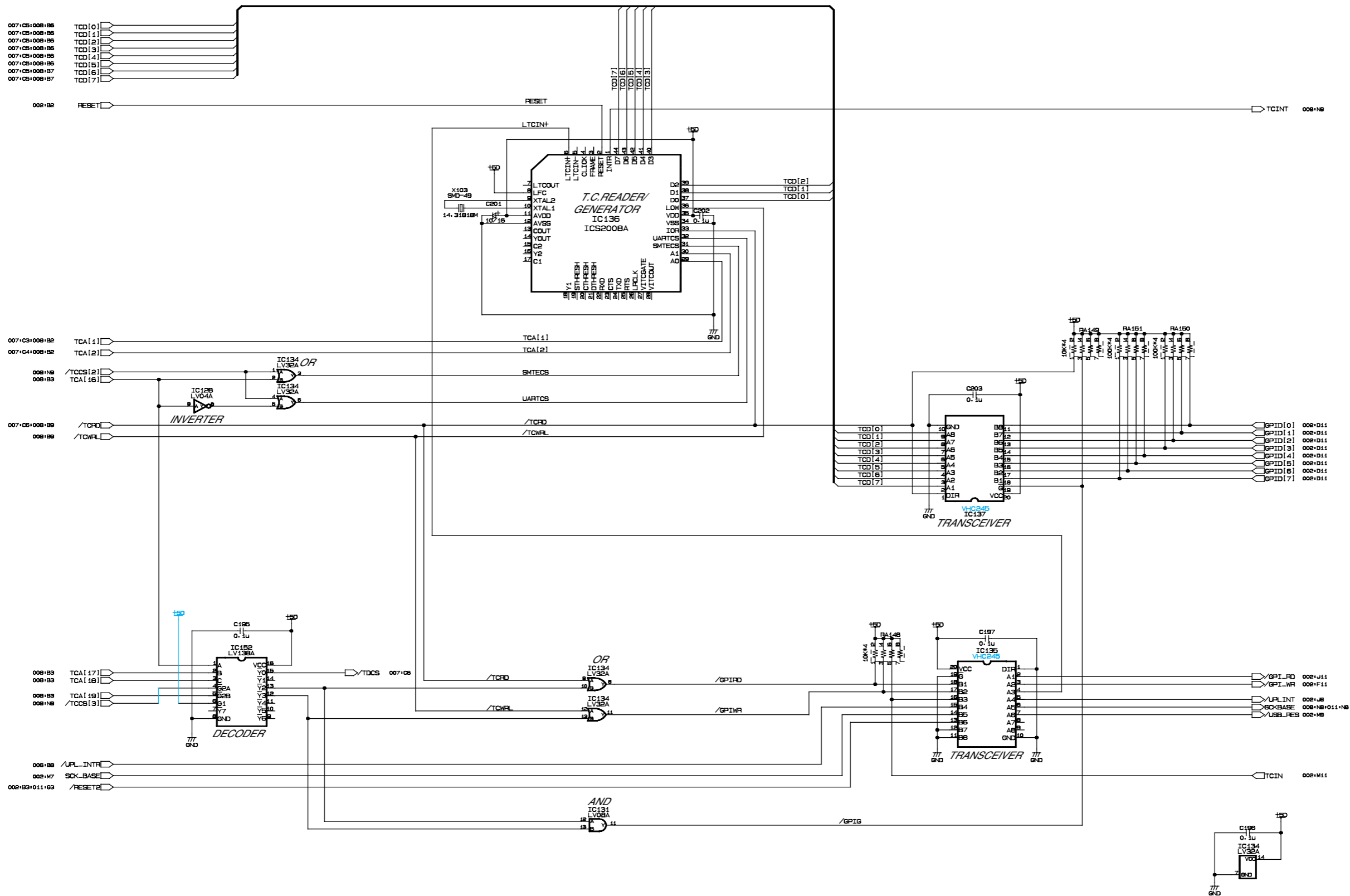
■ CIB CIRCUIT DIAGRAM 008 (DSP1D)

DSP1D

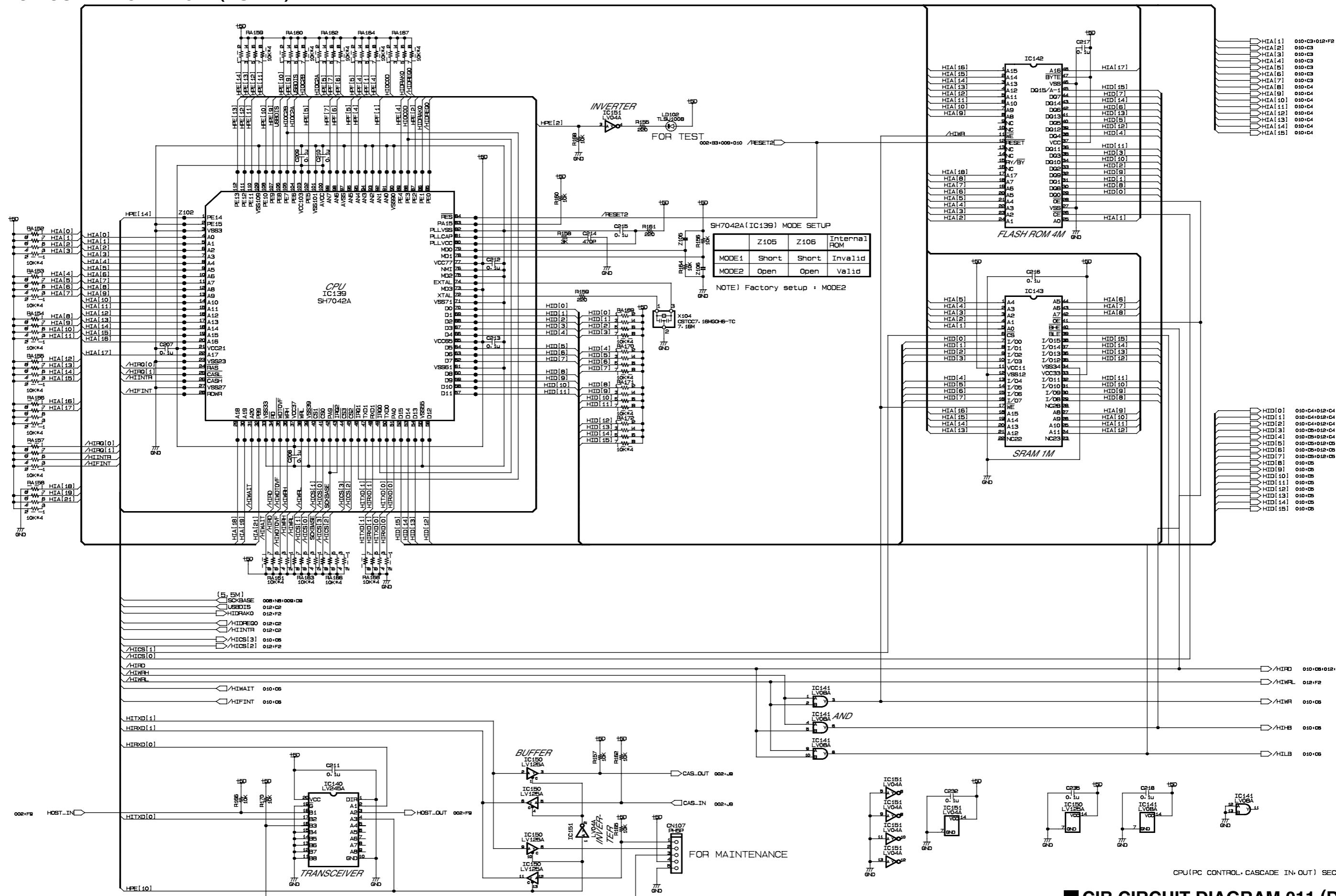


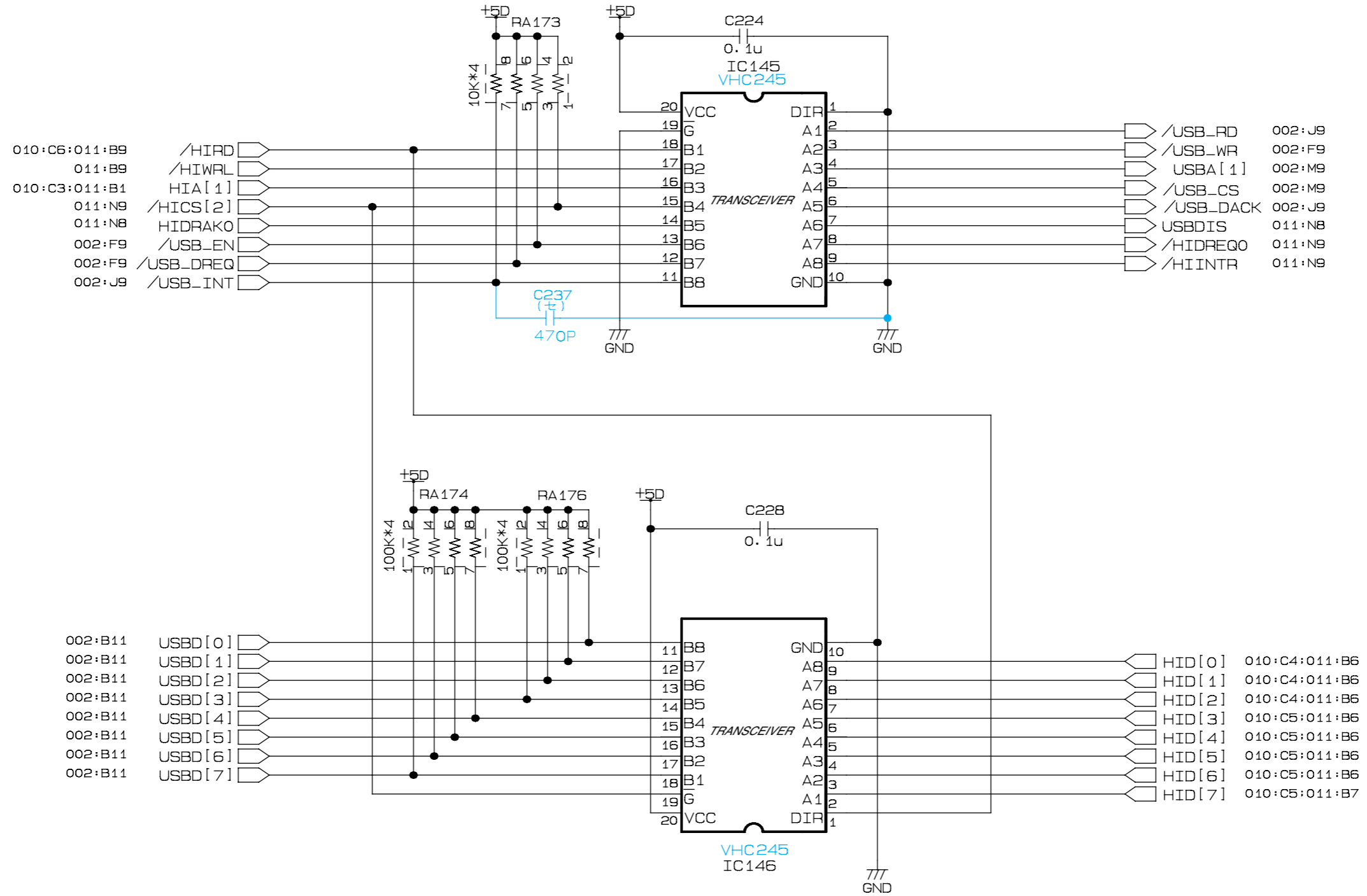
CIB CIRCUIT DIAGRAM 009 (DSP1D)

DSP1D



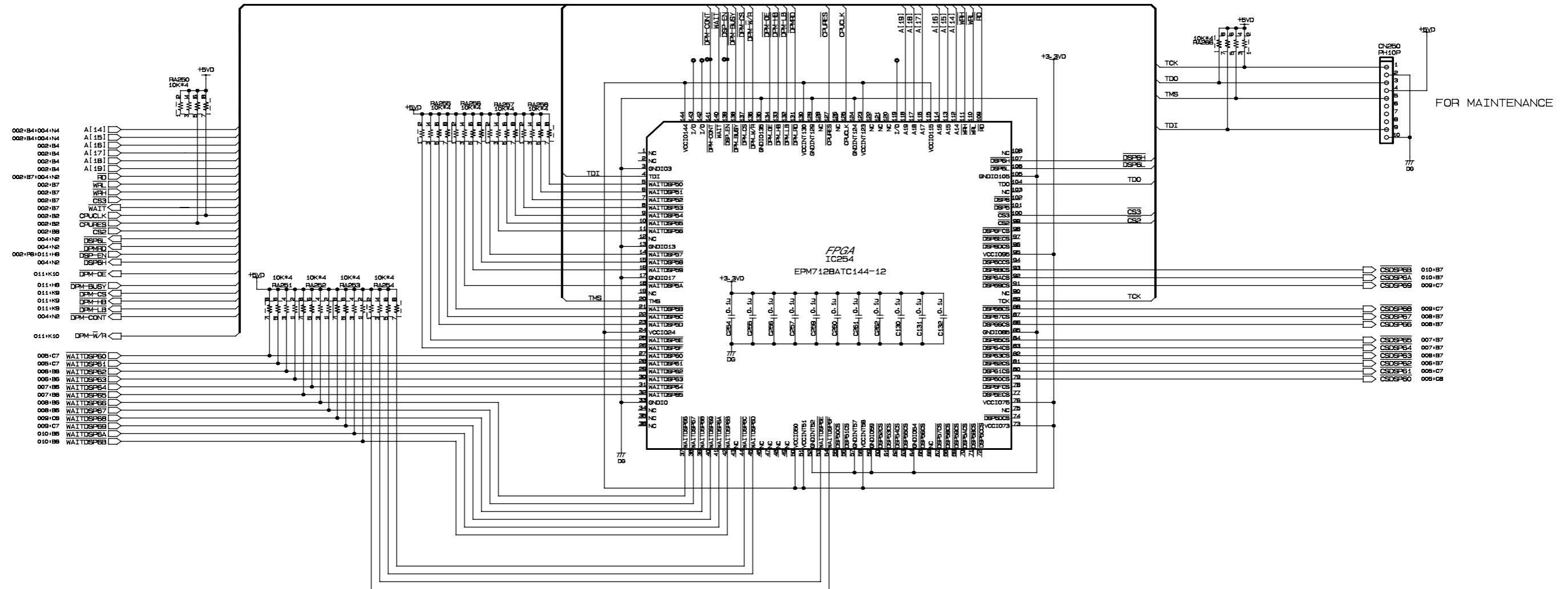
TIMECODE CONTROL SECTION





(t): Ceramic Capacitor

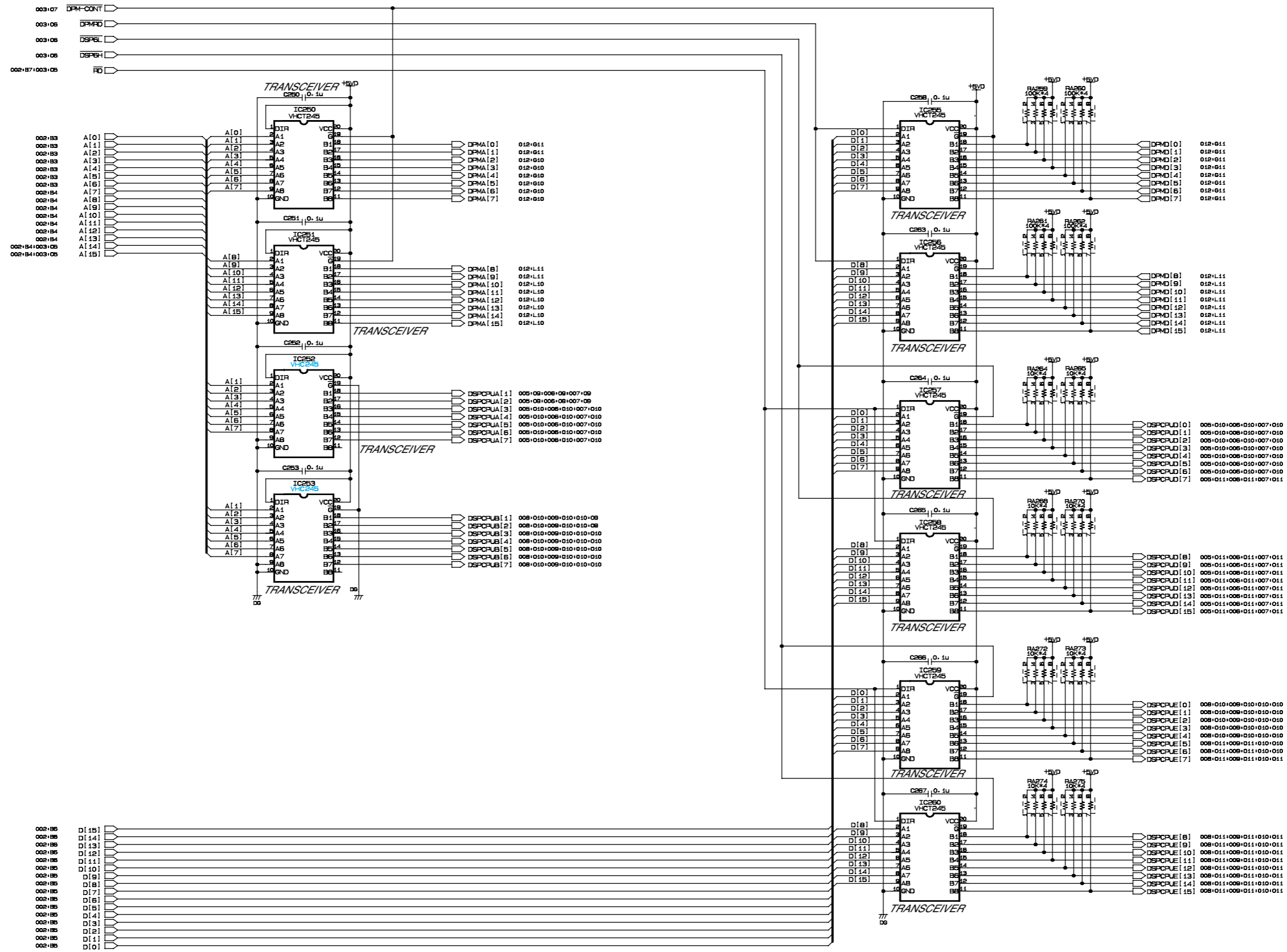
BUFFER & TRANCEIVER(USB BUS <-> HI BUS) SECTION



ADDRESS DECODE & WAIT CONTROL SECTION

EDB CIRCUIT DIAGRAM 004 (DSP1D)

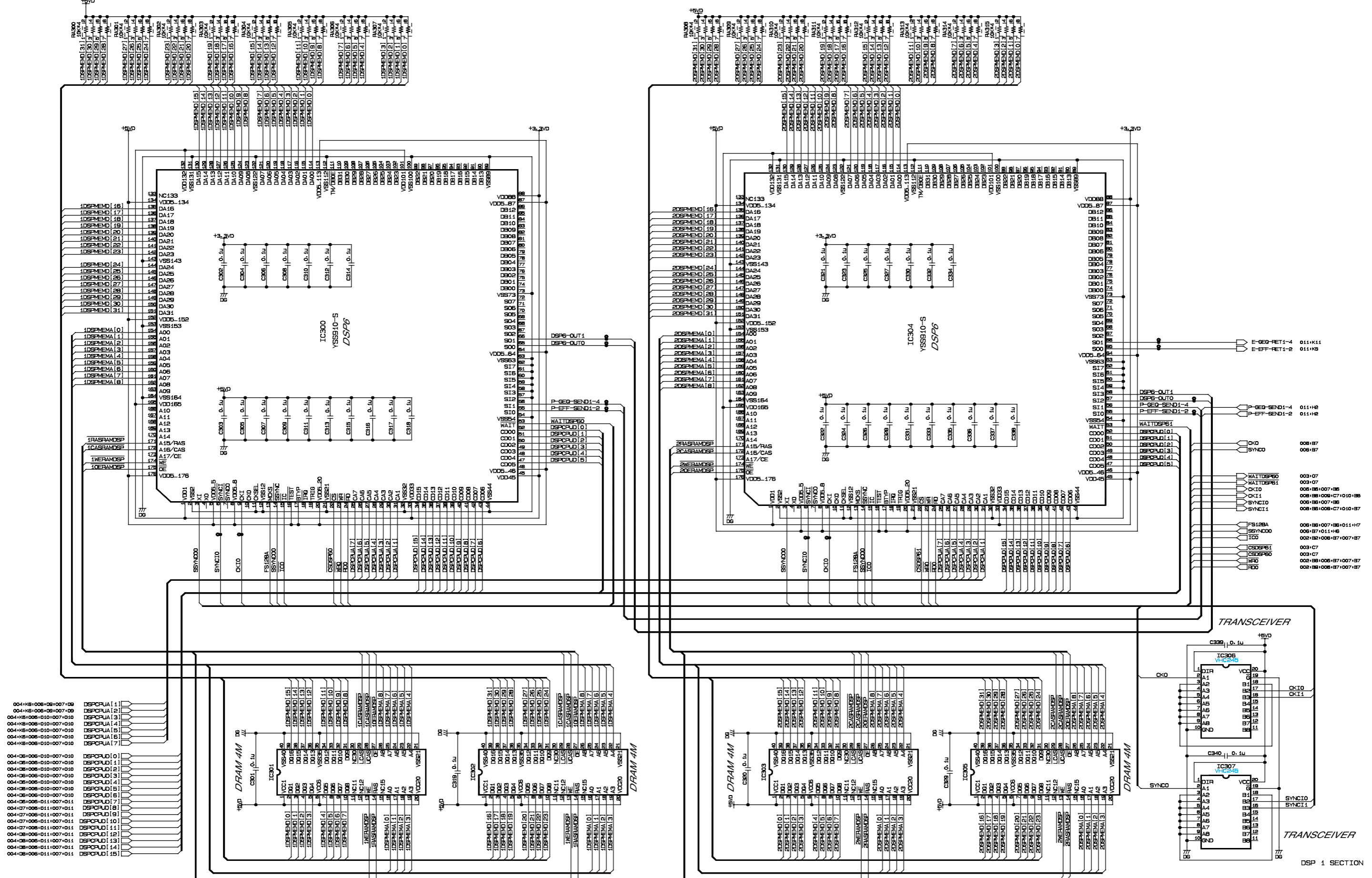
DSP1D



ADDRESS & DATA BUFFER SECTION

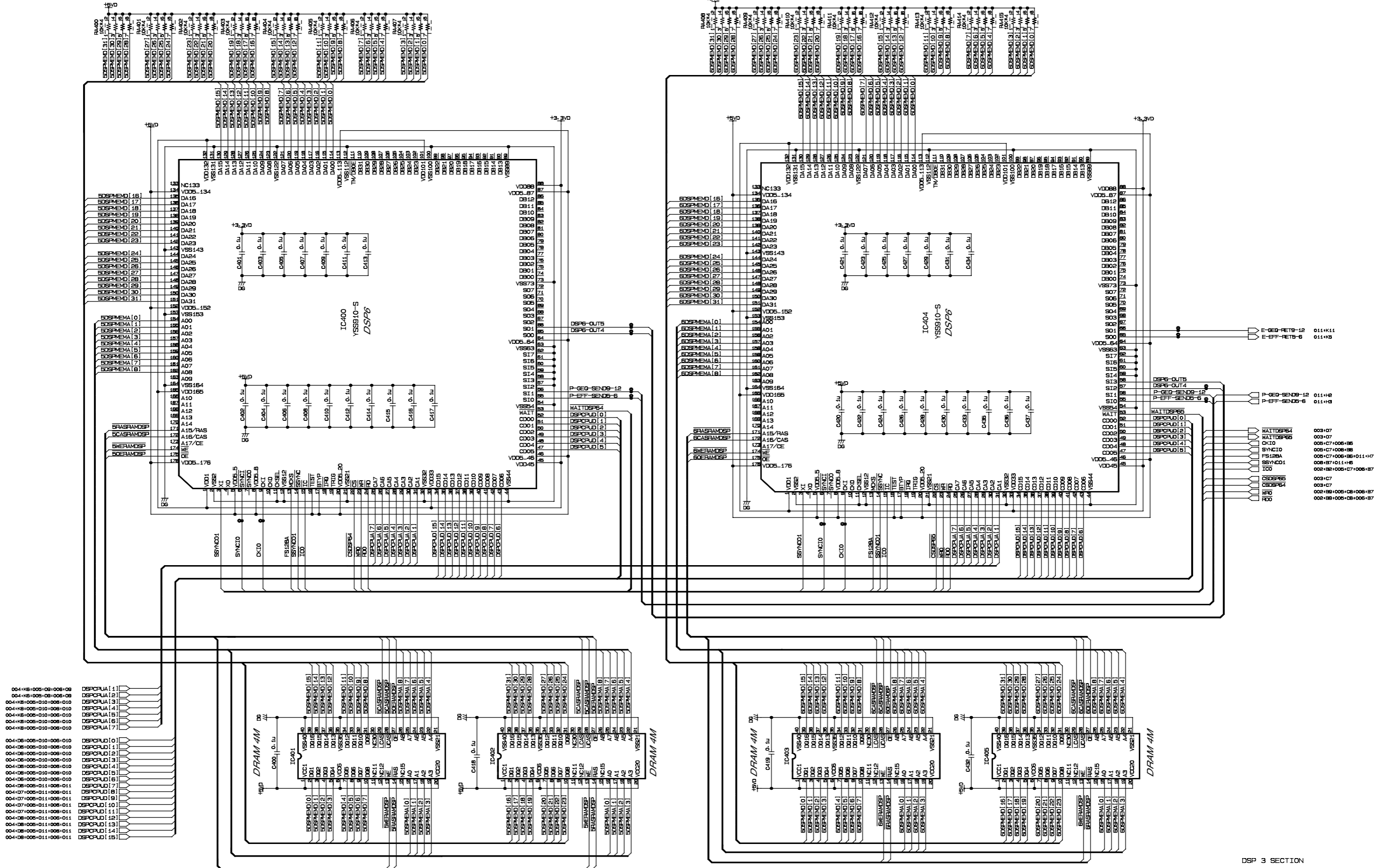
EDB CIRCUIT DIAGRAM 005 (DSP1D)

DSP1D



EDB CIRCUIT DIAGRAM 007 (DSP1D)

DSP1D

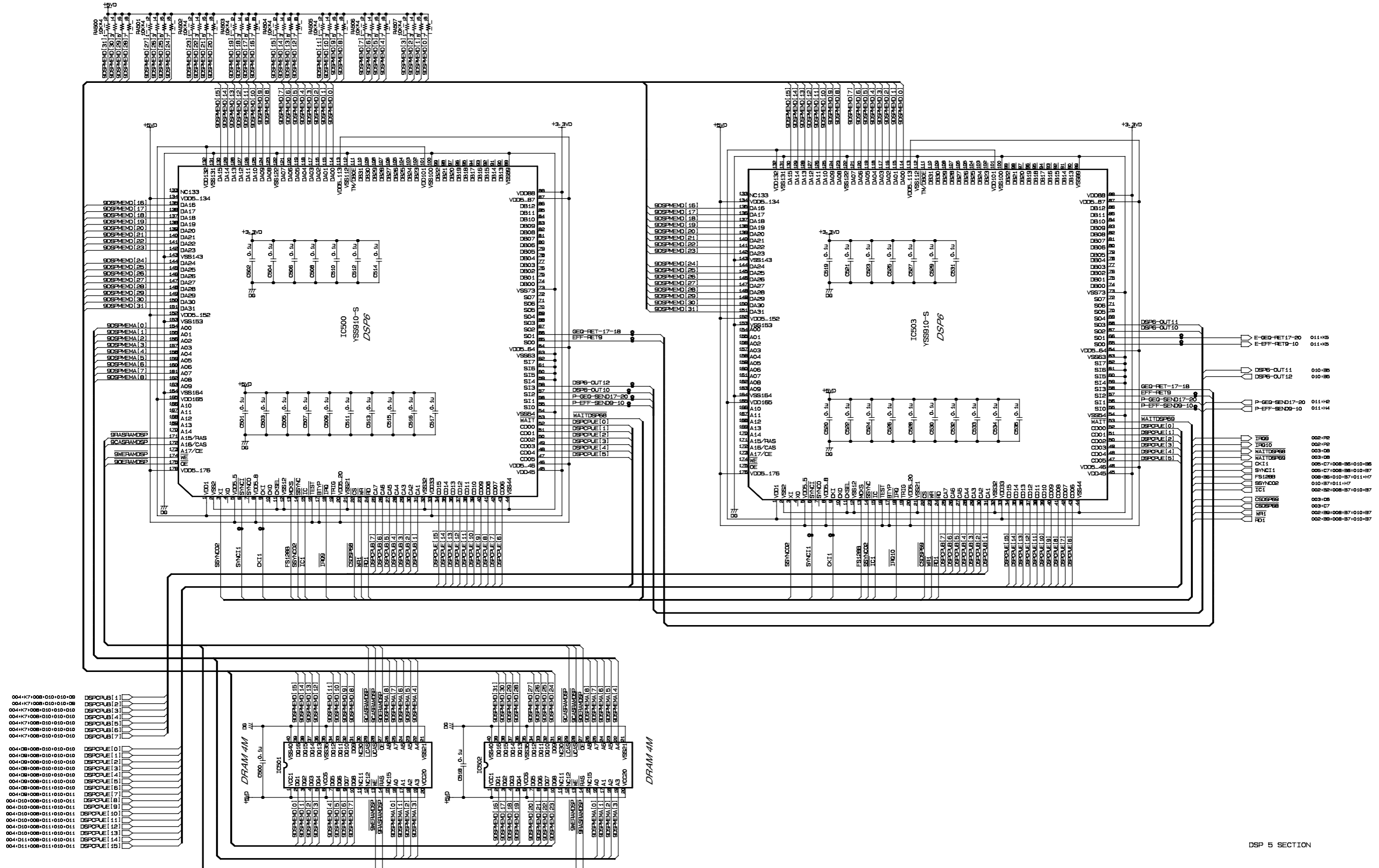


DSP 3 SECTION

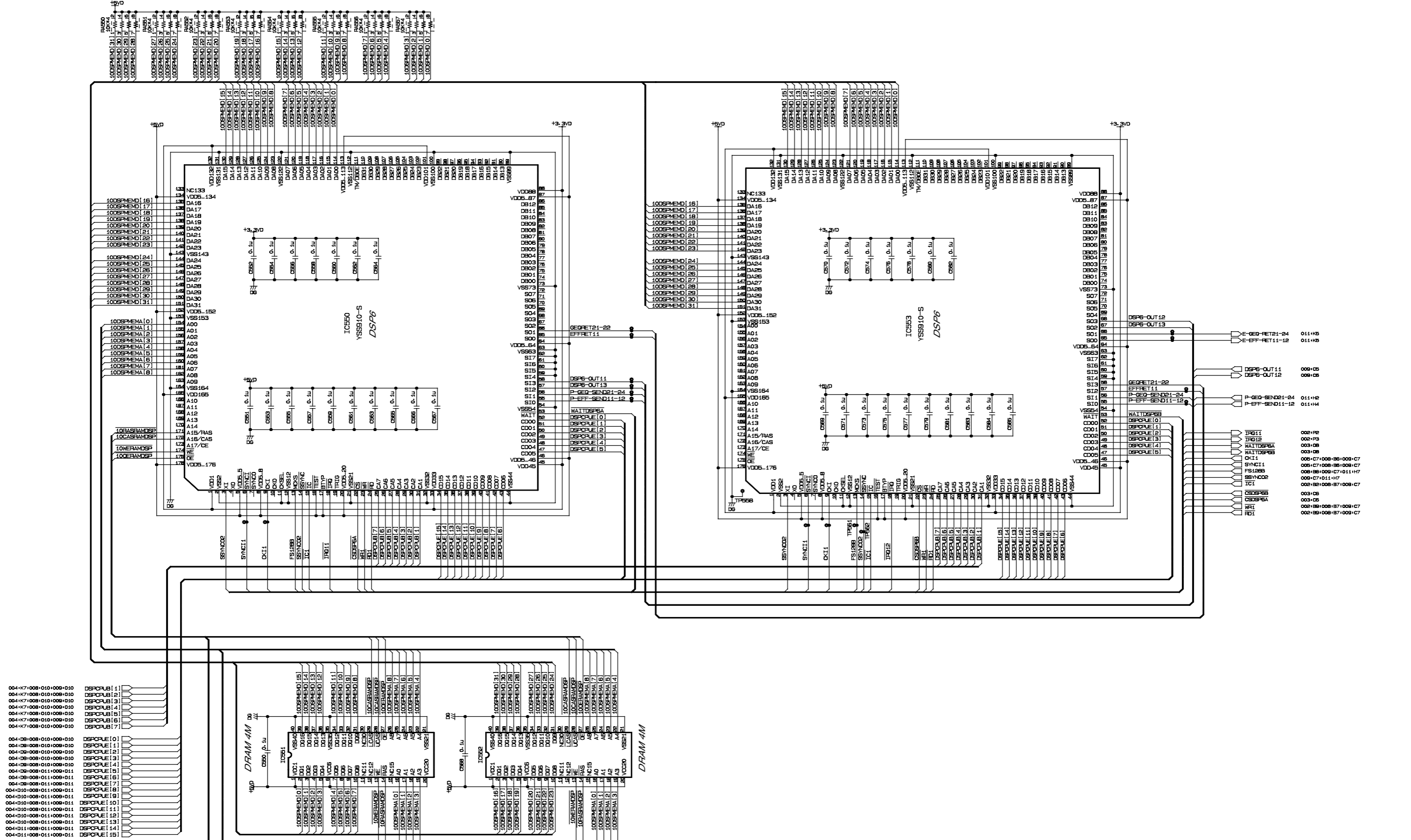
EDB CIRCUIT DIAGRAM 007 (DSP1D)

EDB CIRCUIT DIAGRAM 009 (DSP1D)

DSP1D



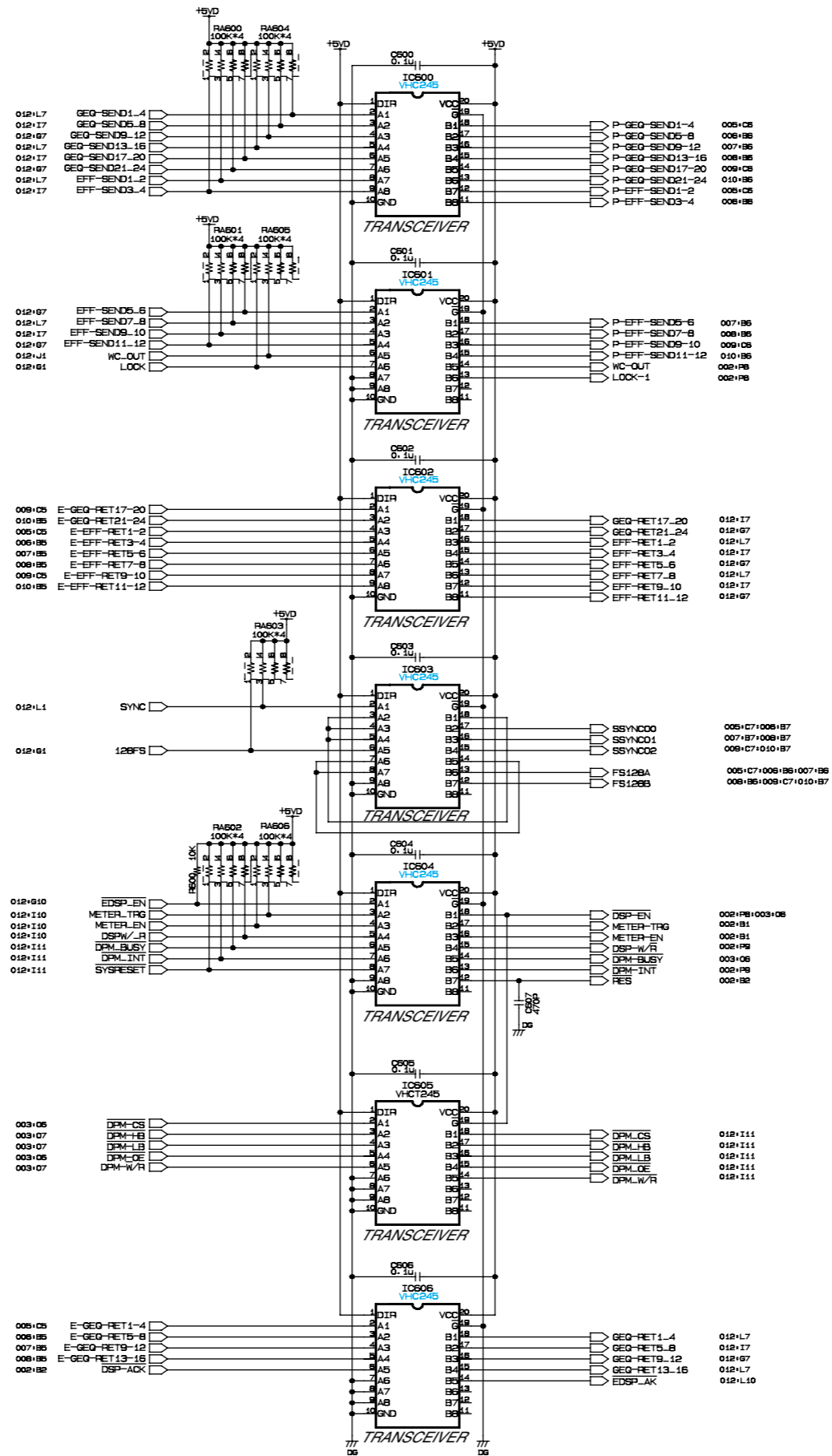
DSP 5 SECTION



1
2
3
4
5
6
7
8
9
10
11
12

EDB CIRCUIT DIAGRAM 011 (DSP1D)

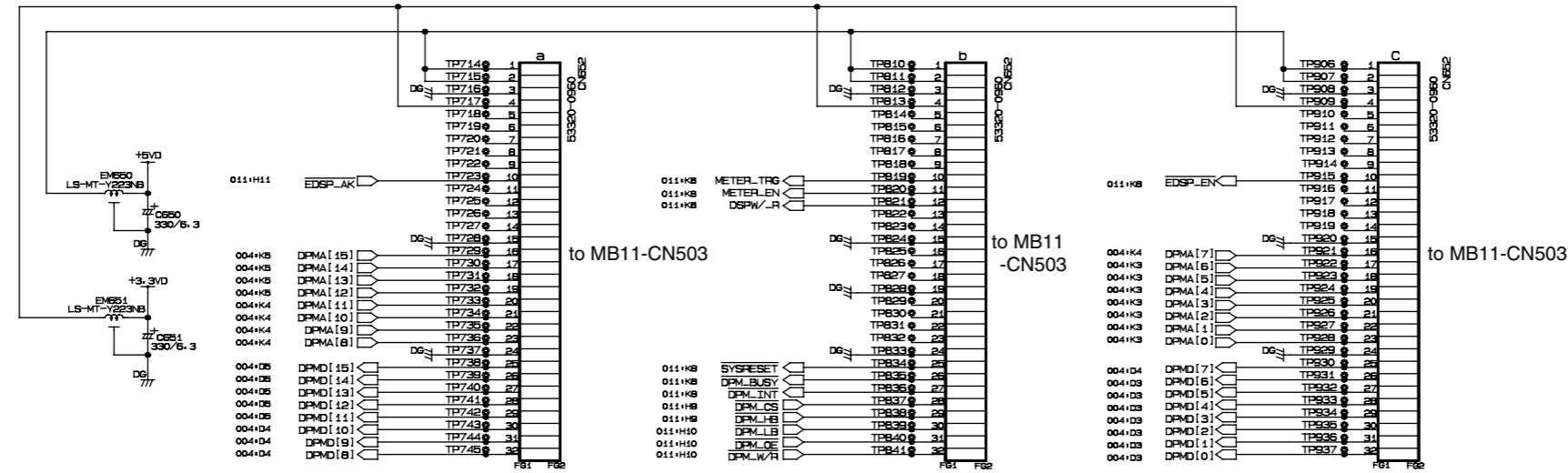
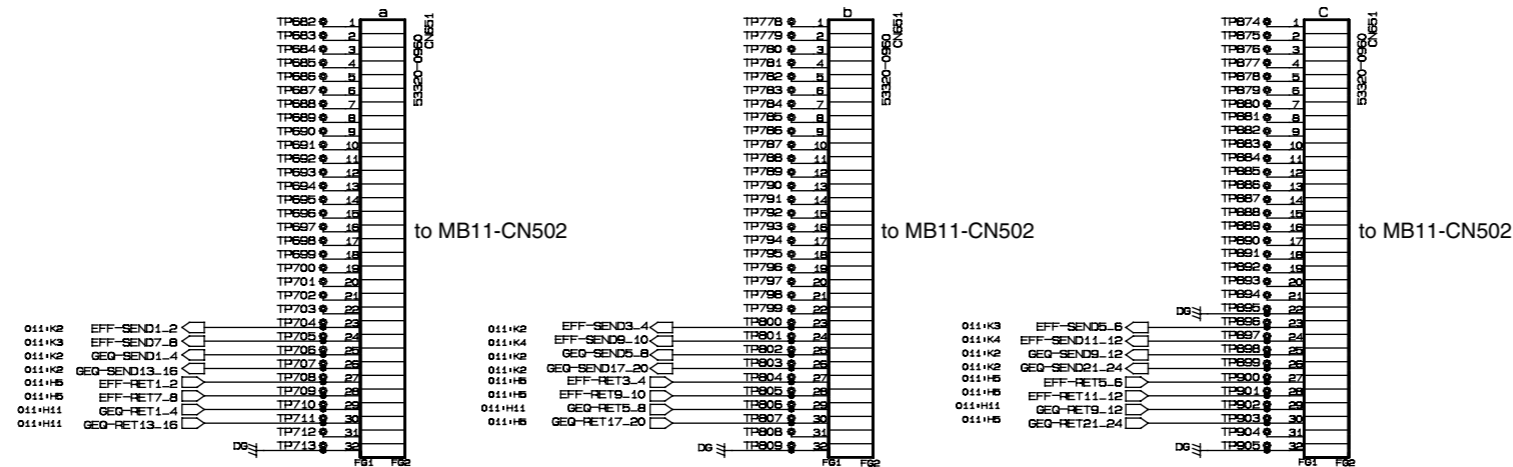
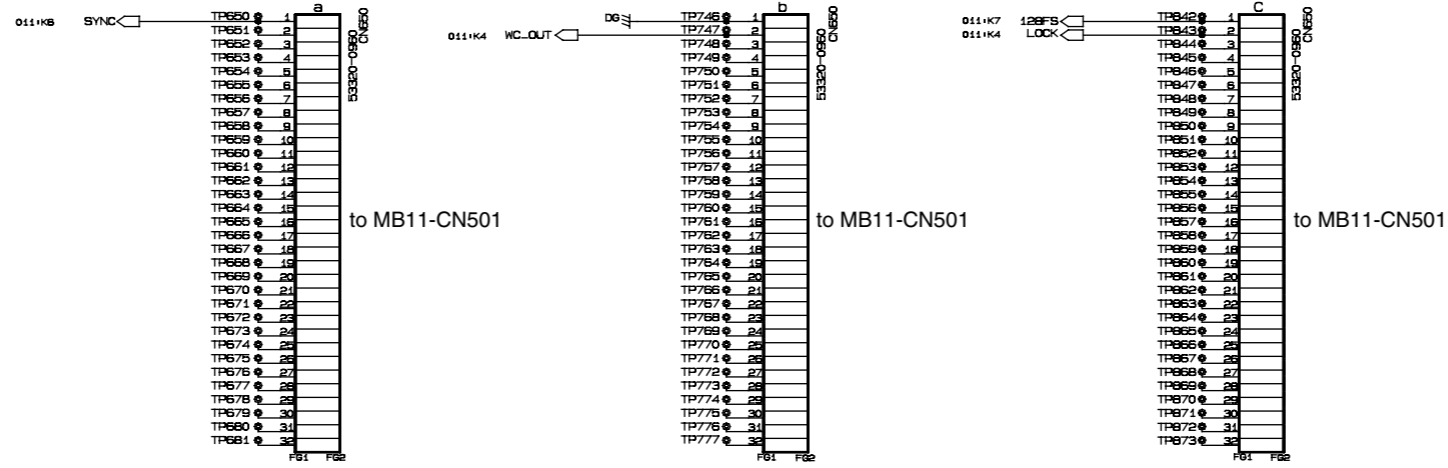
DSP1D



AUDIO DATA BUFFER SECTION

EDB CIRCUIT DIAGRAM 012 (DSP1D)

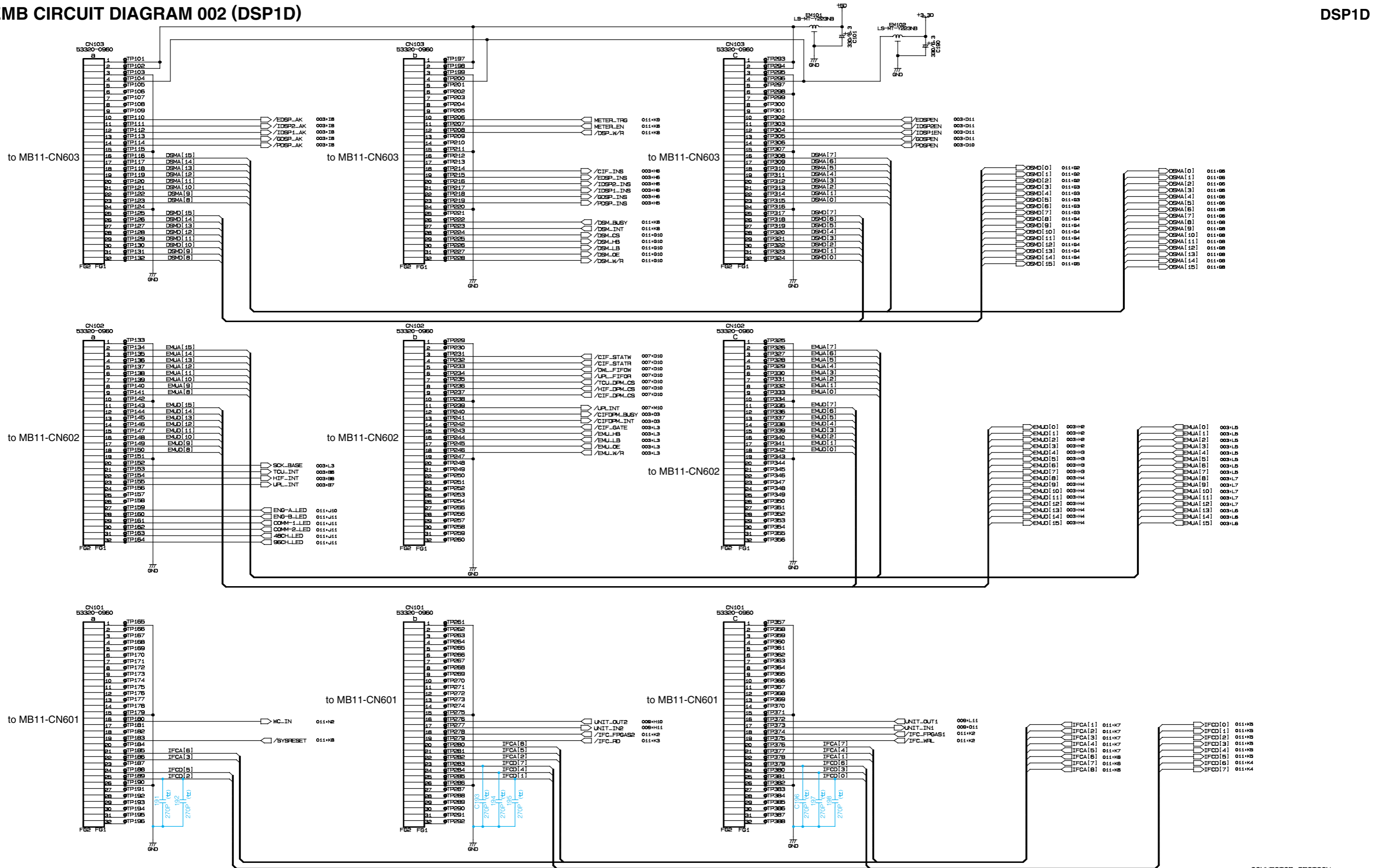
DSP1D



CONNECTOR SECTION

EMB CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D

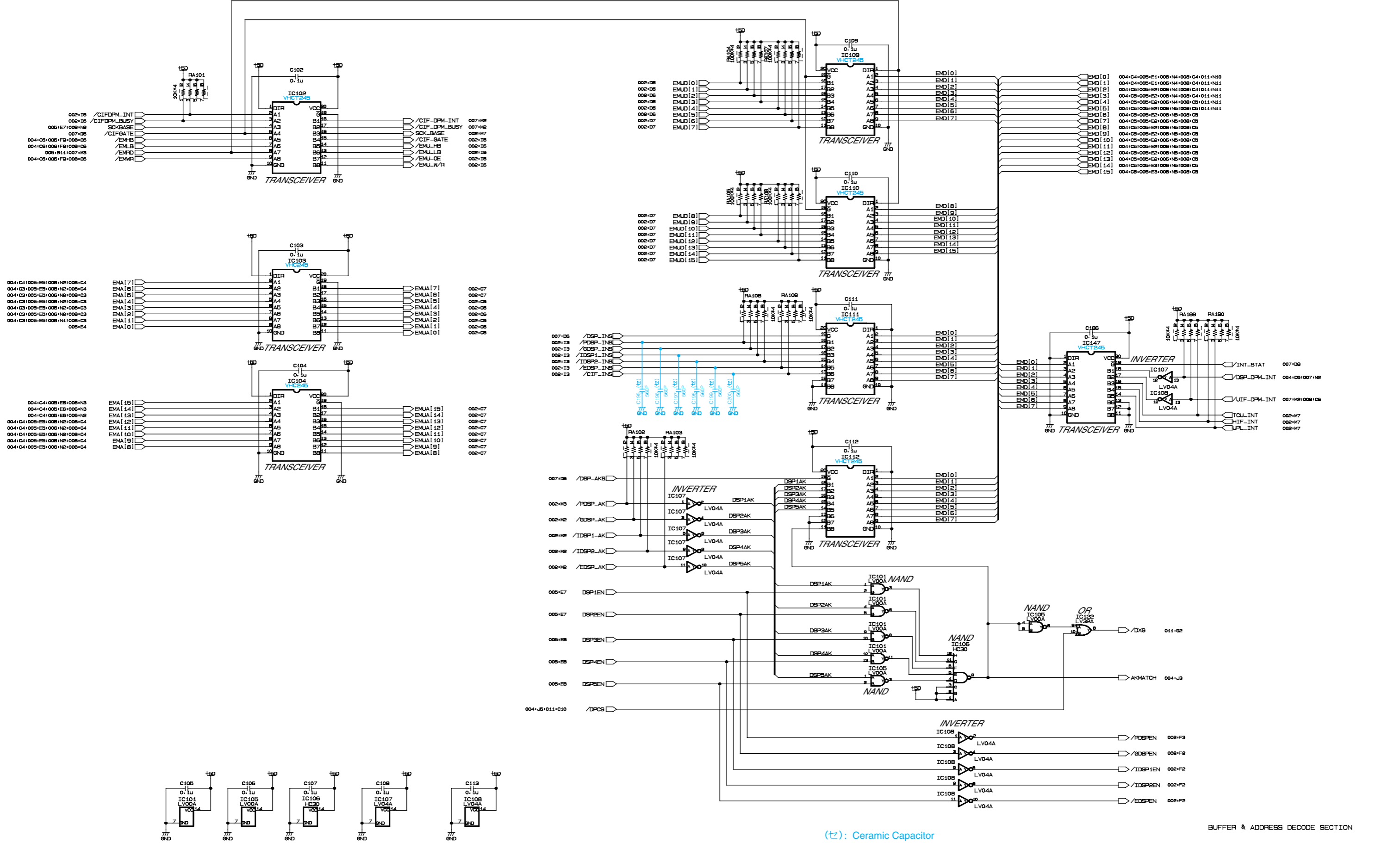


CONNECTOR SECTION

(t): Ceramic Capacitor

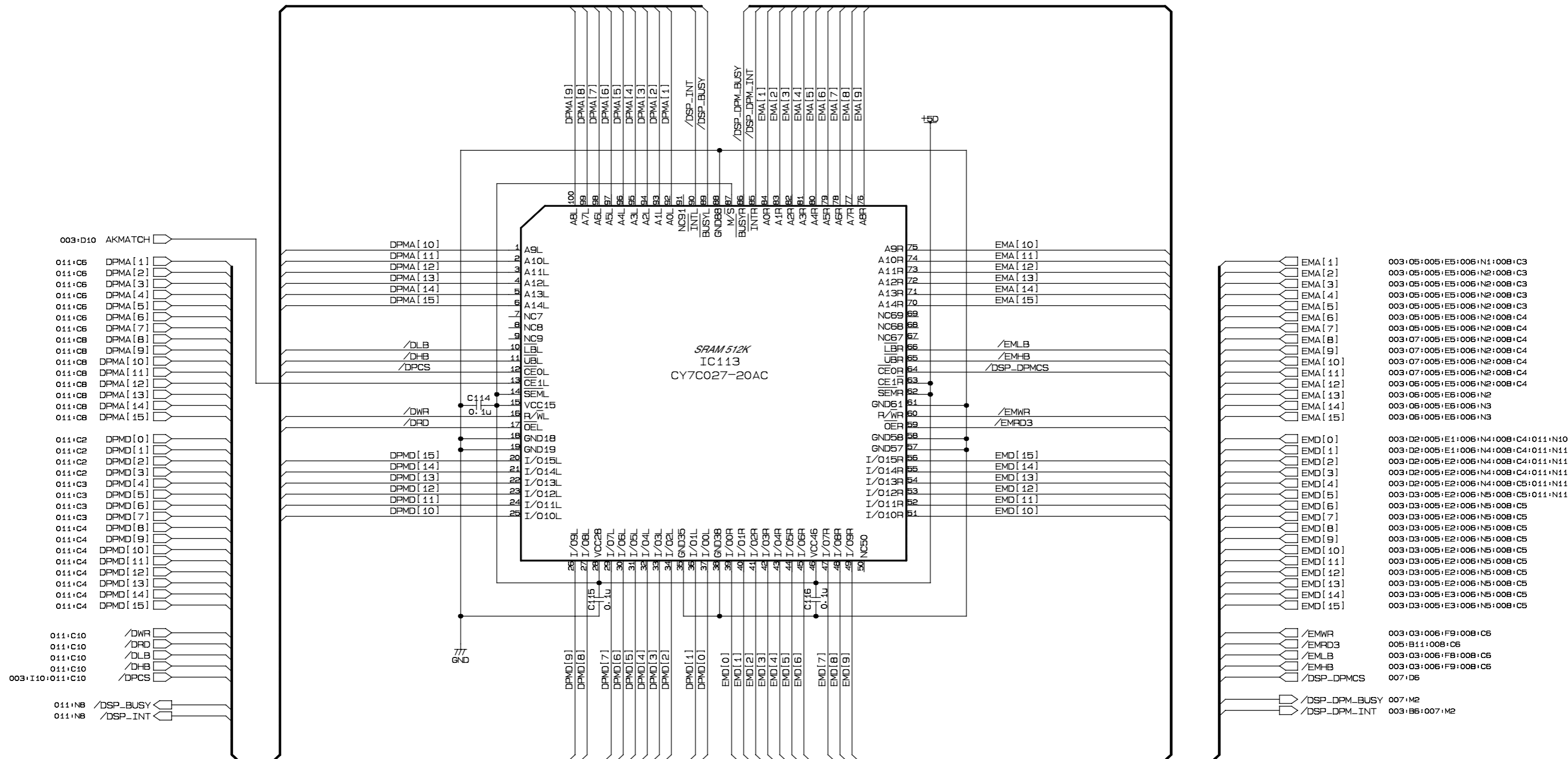
EMB CIRCUIT DIAGRAM 003 (DSP1D)

DSP1D



(tz): Ceramic Capacitor

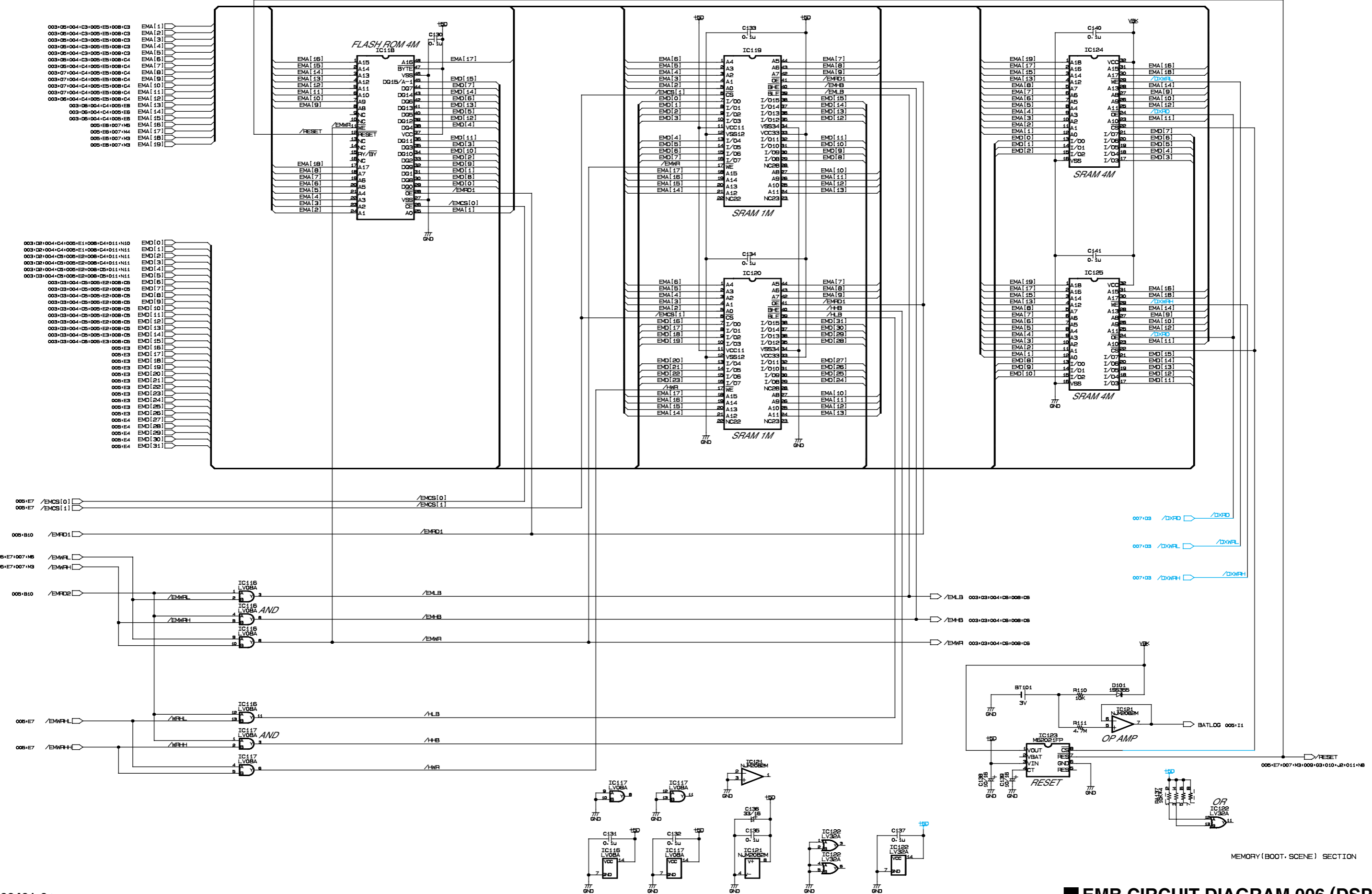
BUFFER & ADDRESS DECODE SECTION



DUAL PORT MEMORY (DPM BUS <-> EM BUS) SECTION

EMB CIRCUIT DIAGRAM 006 (DSP1D)

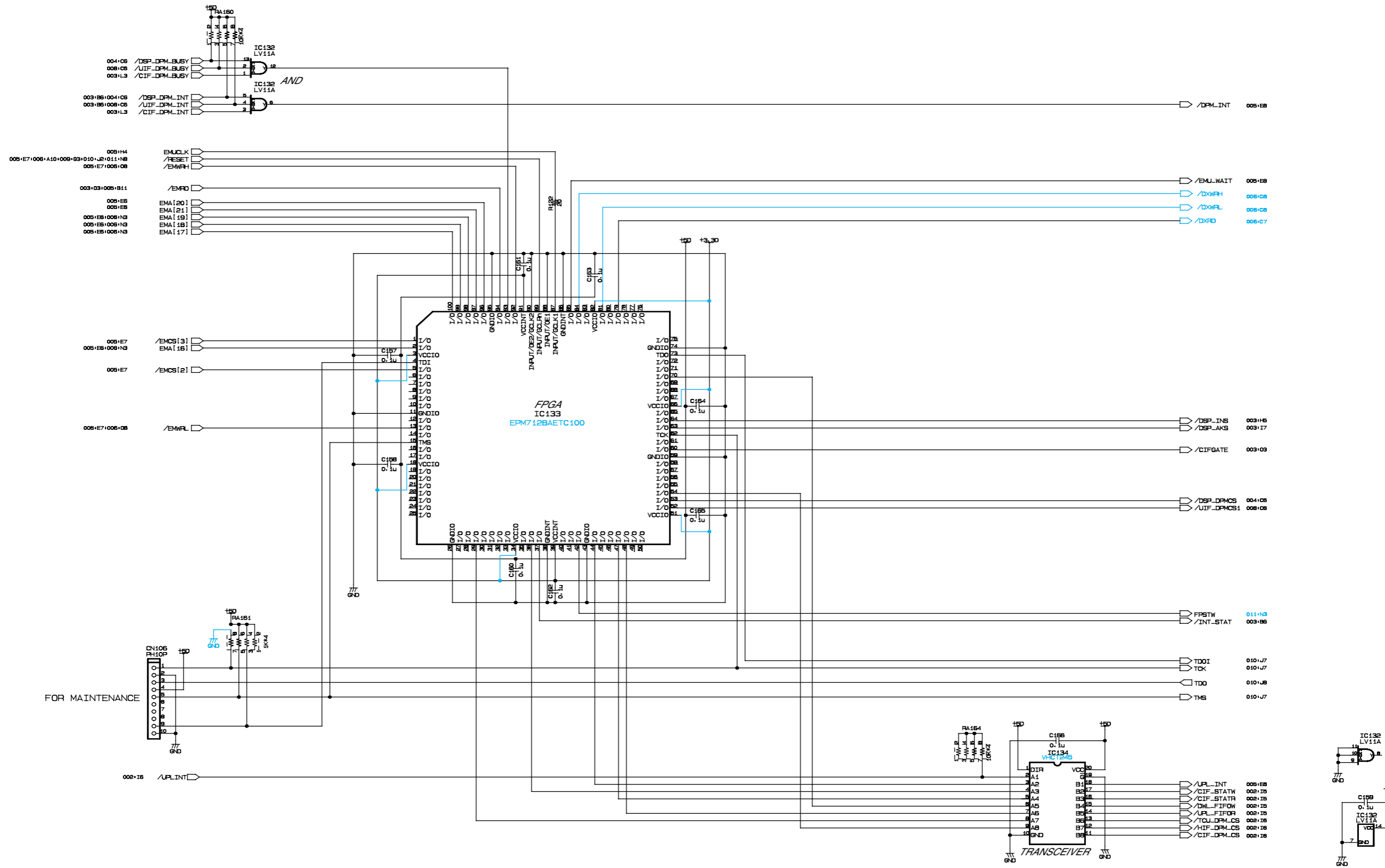
DSP1D



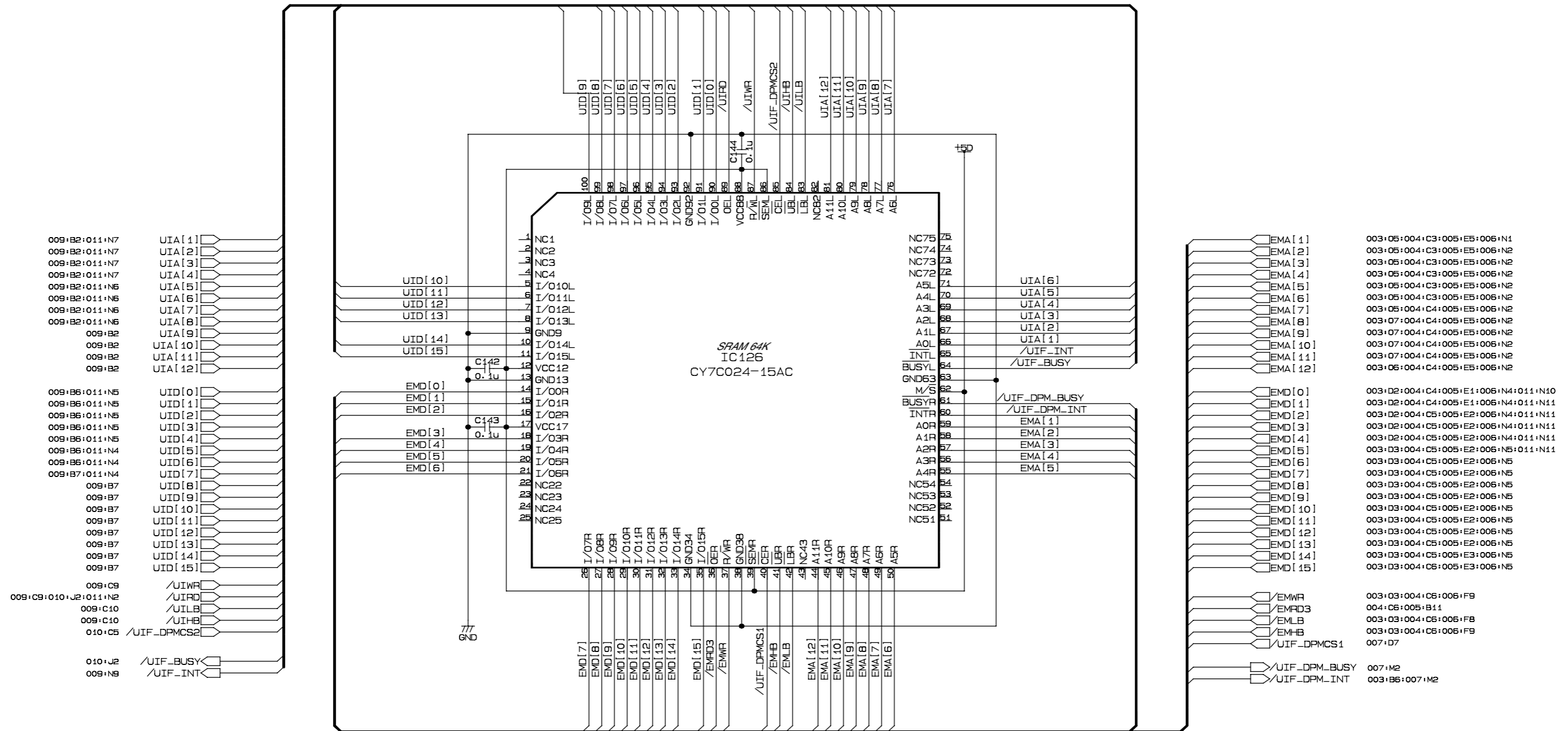
MEMORY (BOOT- SCENE) SECTION

EMB CIRCUIT DIAGRAM 007 (DSP1D)

DSP1D



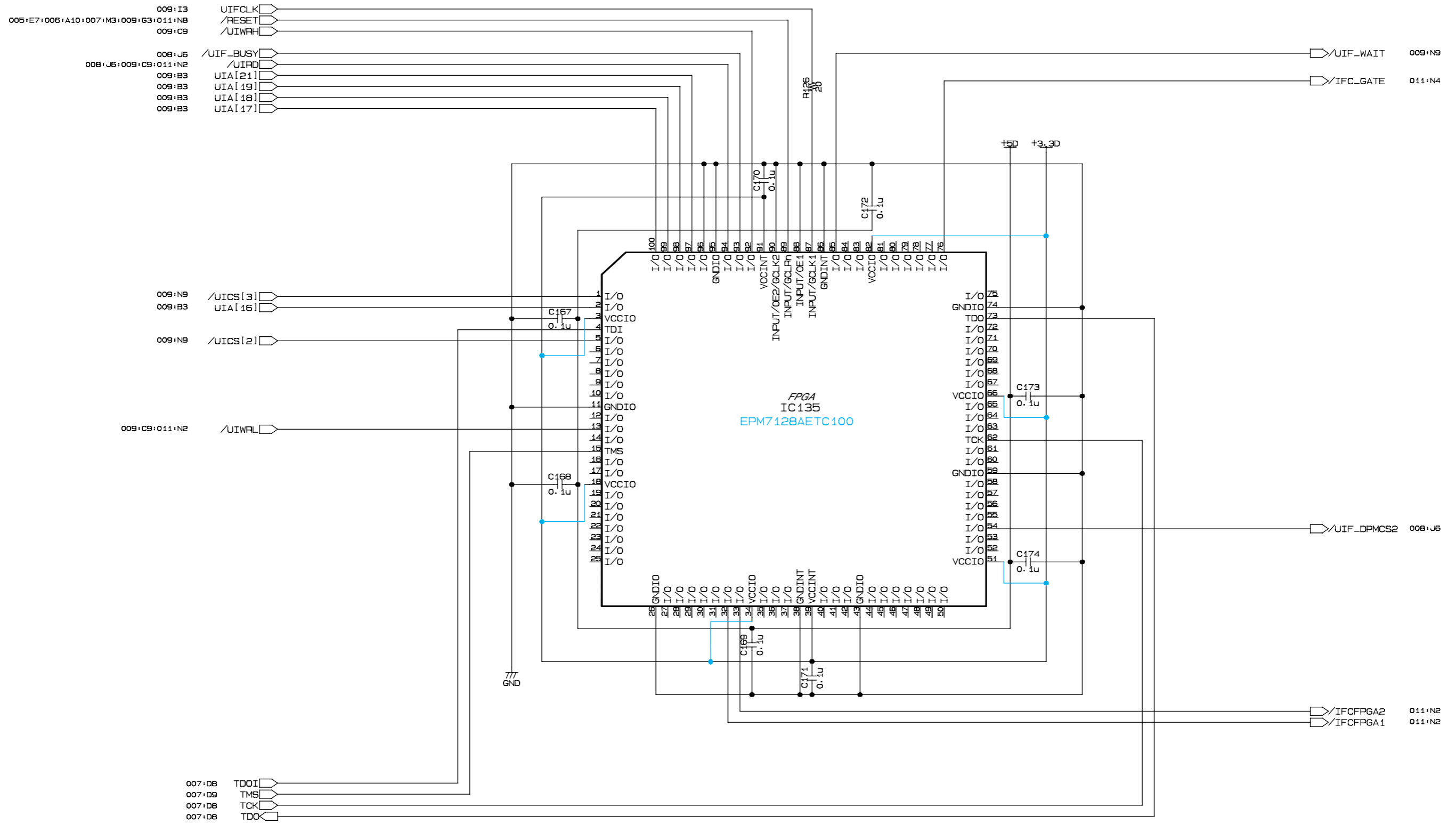
FPGA (DUAL PORT MEMORY CONTROL) SECTION



DUAL PORT MEMORY (UI BUS <-> EM BUS) SECTION

EMB CIRCUIT DIAGRAM 010 (DSP1D)

DSP1D



FPGA(UI BUS CONTROL) SECTION

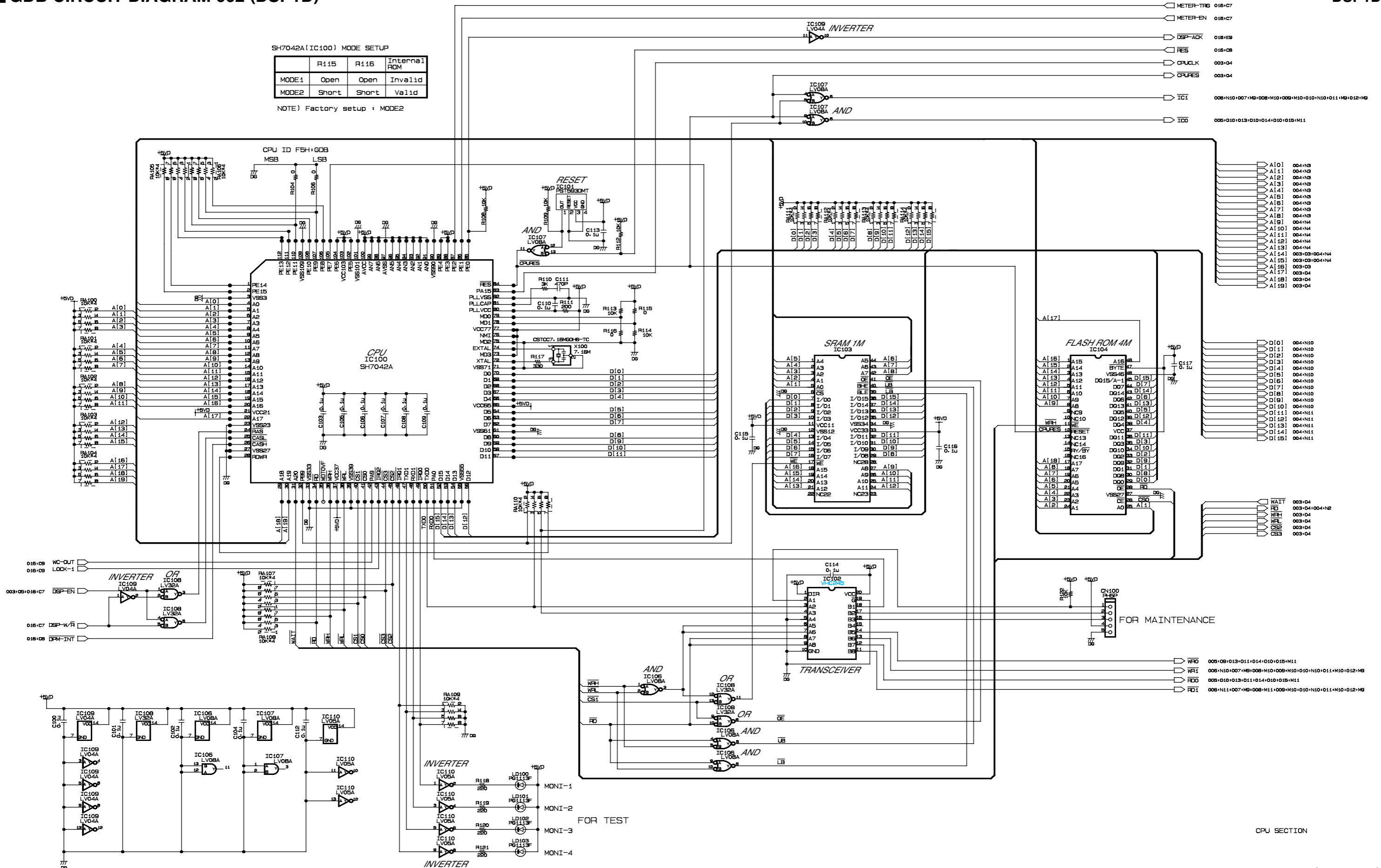
GDB CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D

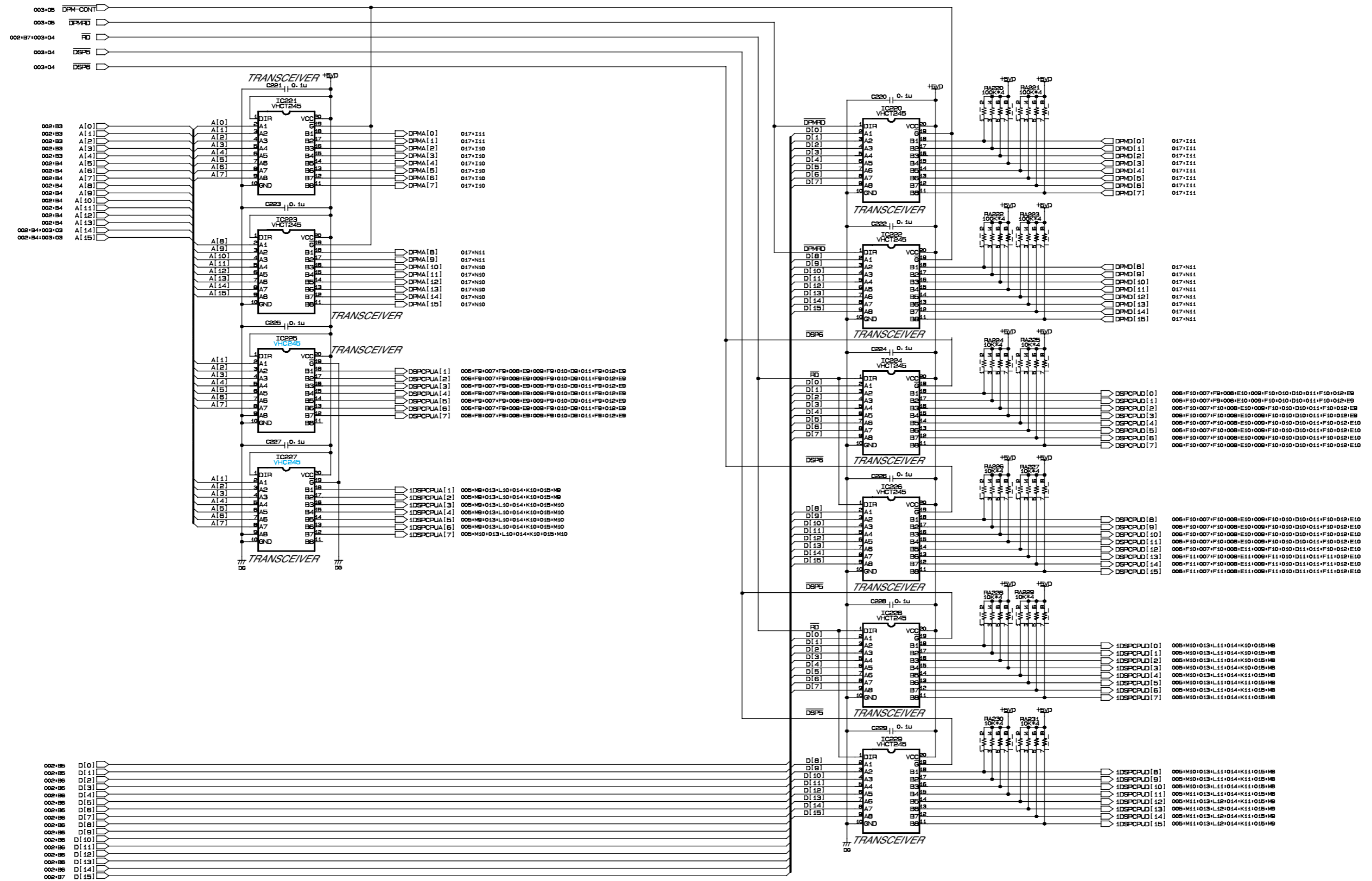
SH7042A(IC100) MODE SETUP

	R115	R116	Internal ROM
MODE1	Open	Open	Invalid
MODE2	Short	Short	Valid

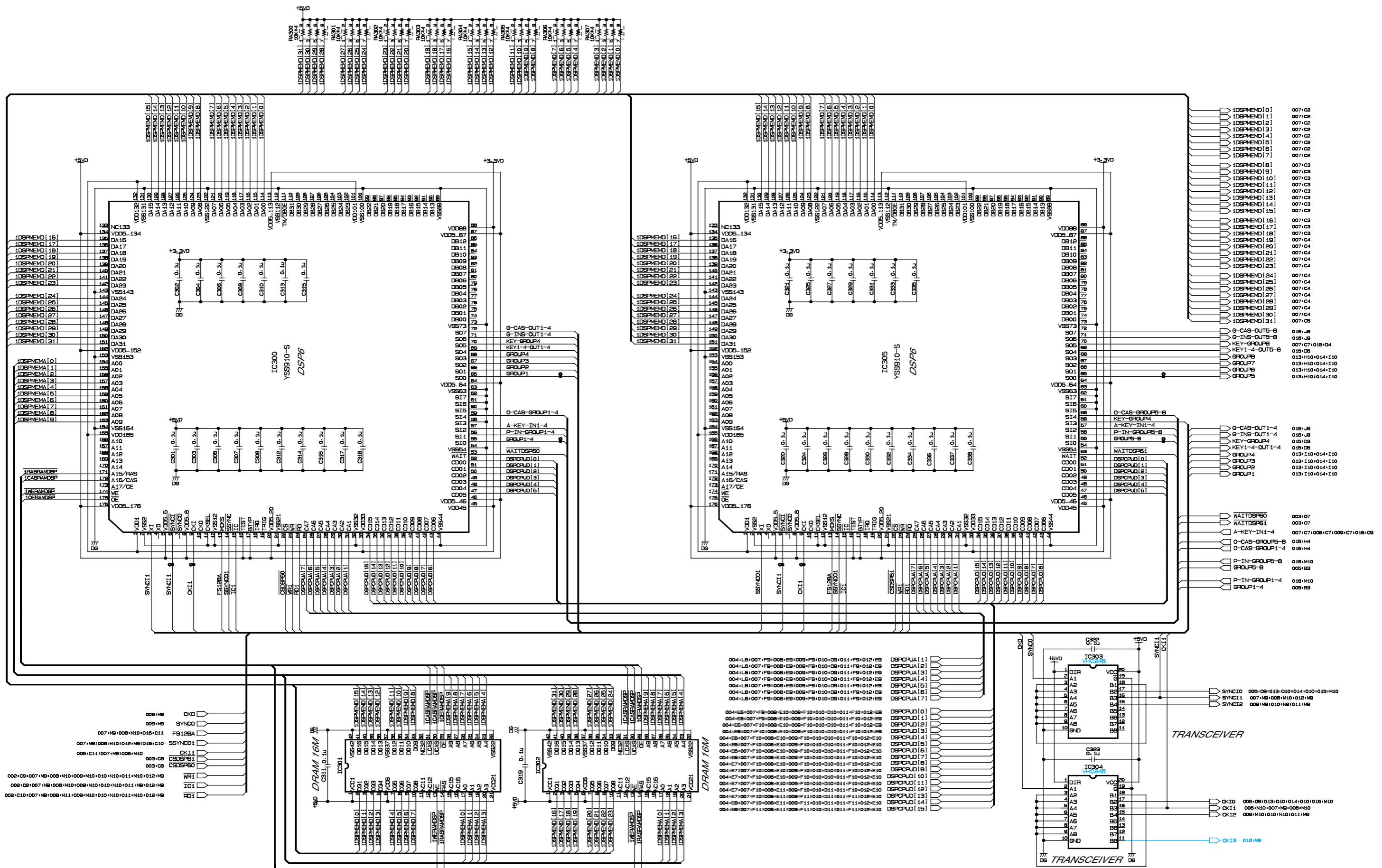
NOTE) Factory setup : MODE2

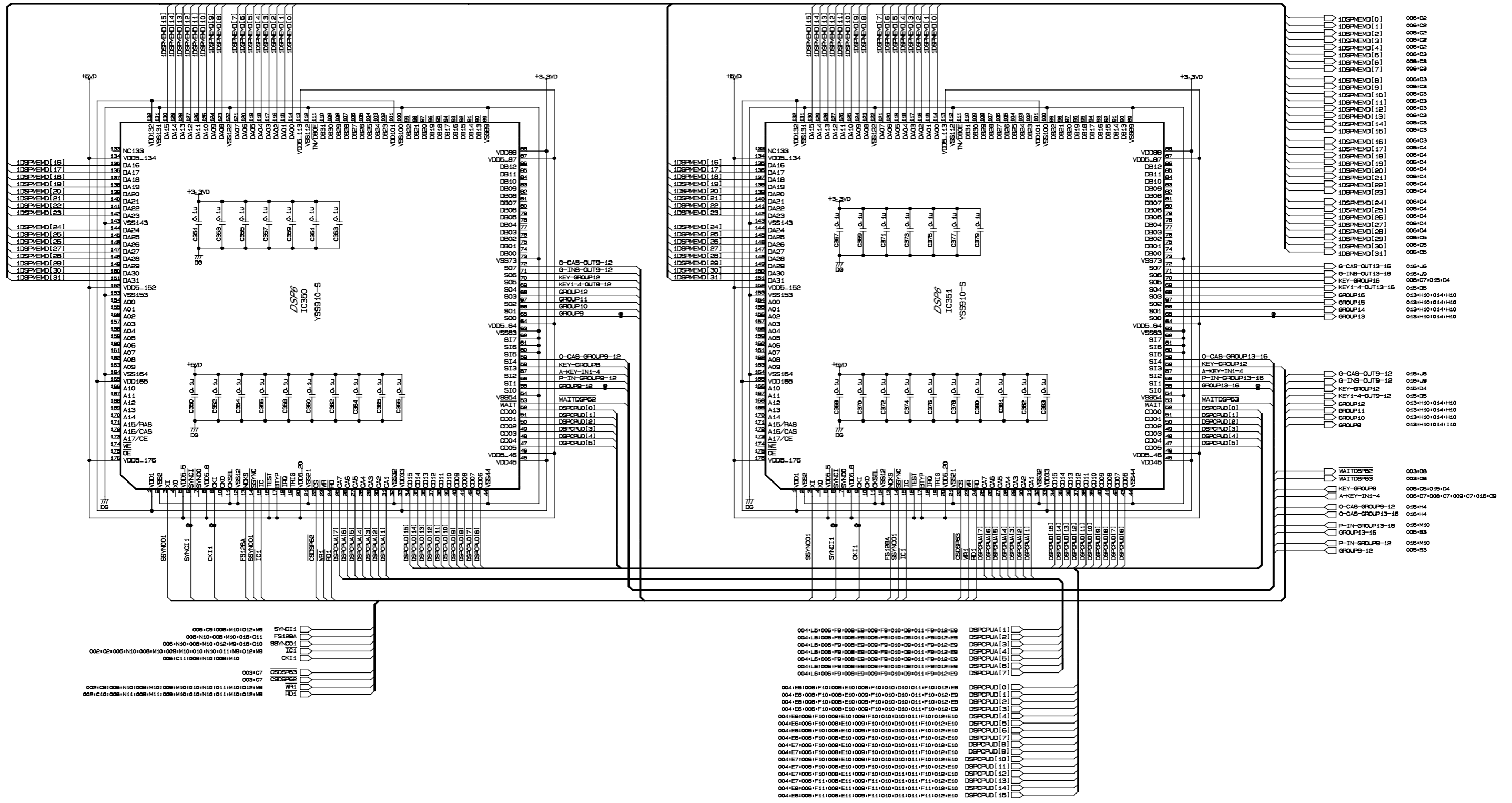


CPU SECTION

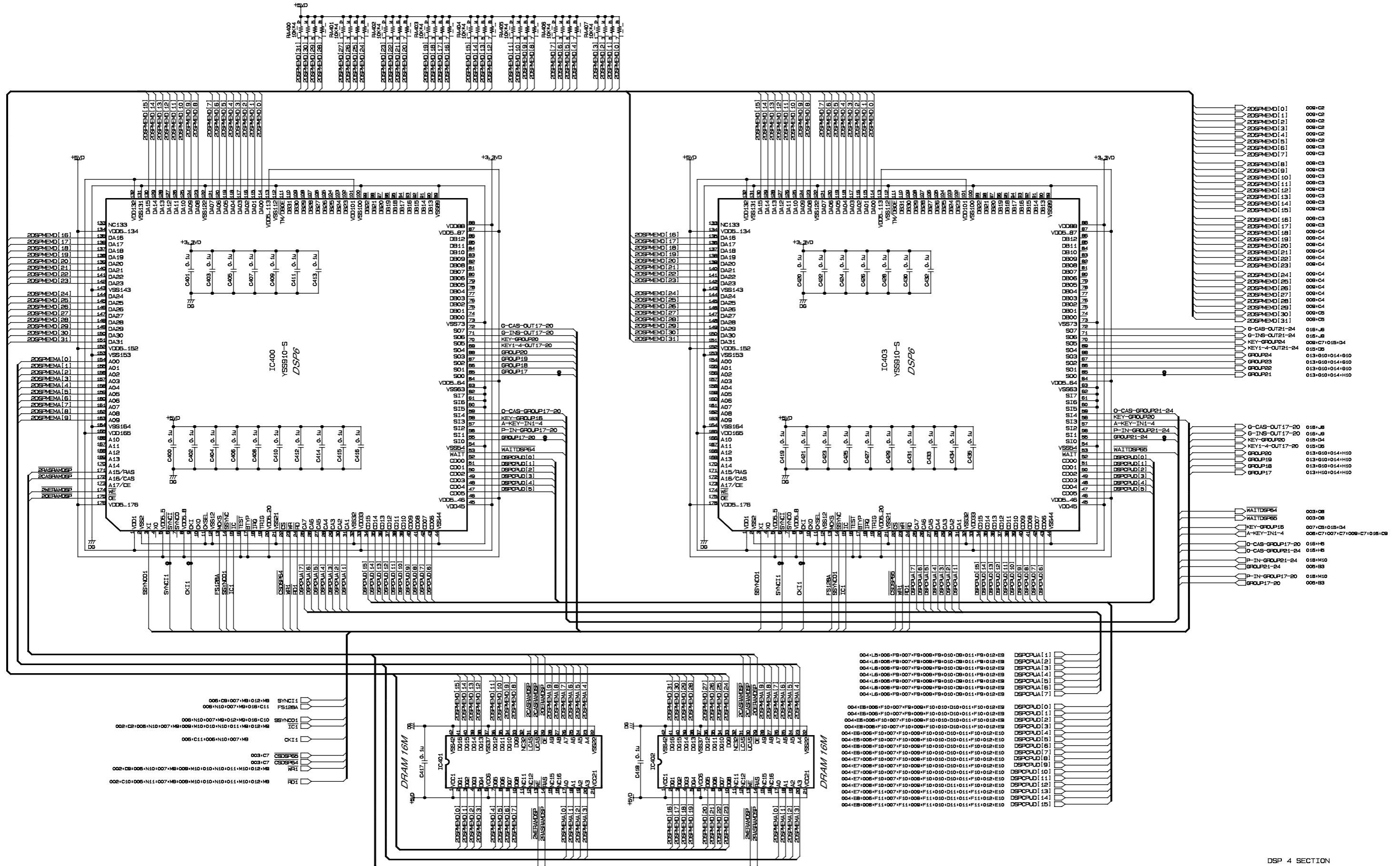


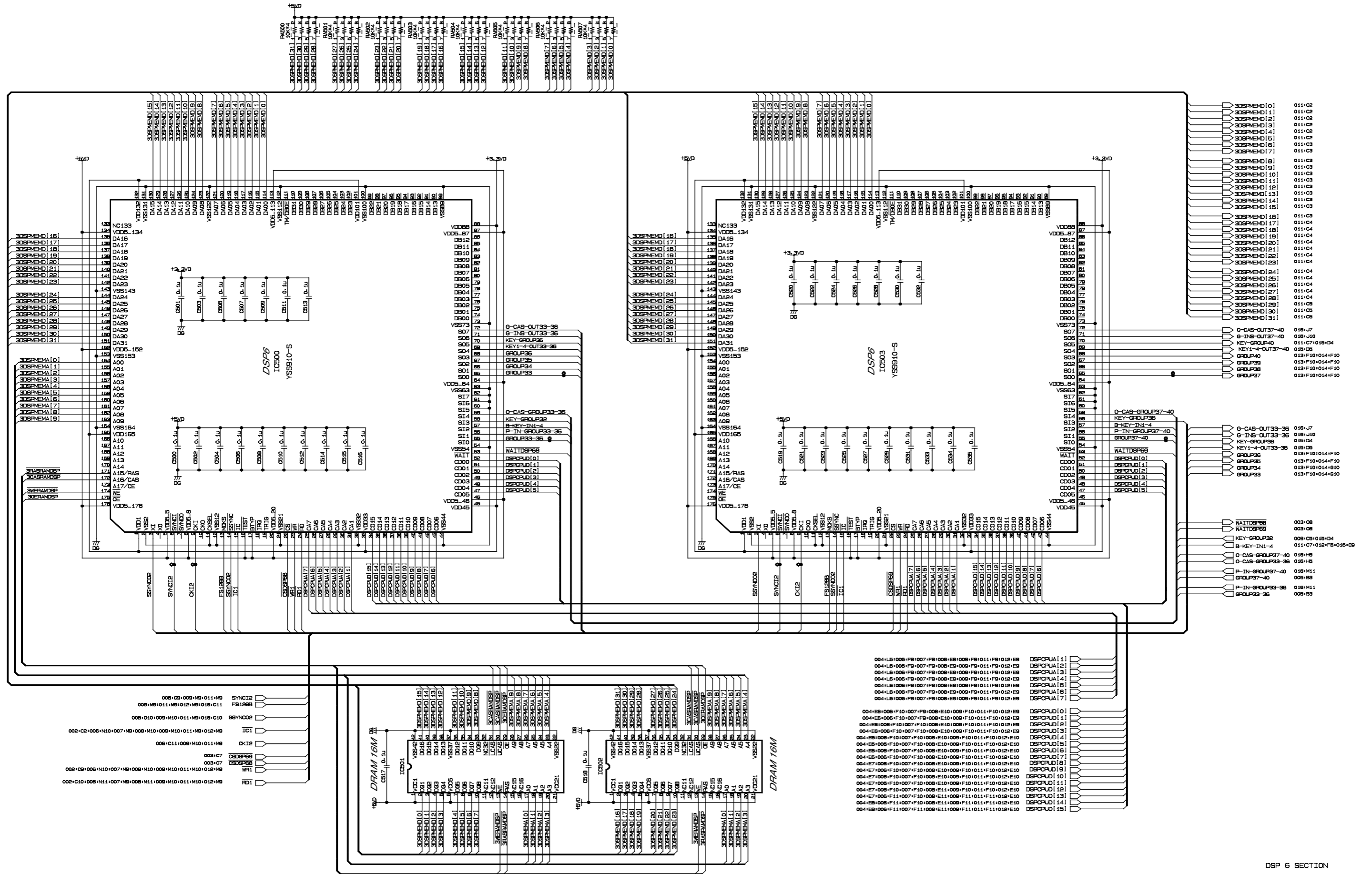
BUFFER SECTION



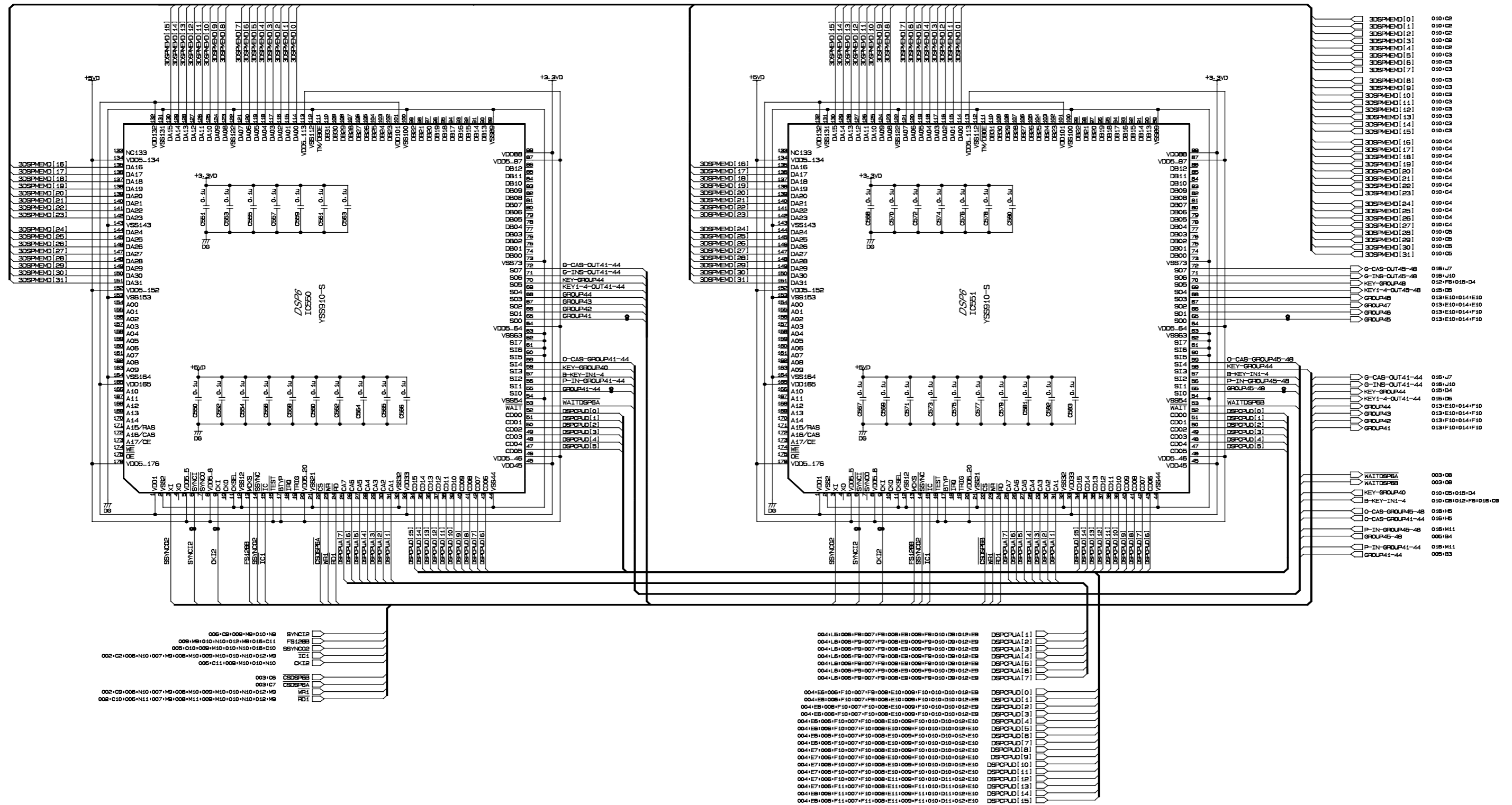


DSP 3 SECTION





DSP 6 SECTION

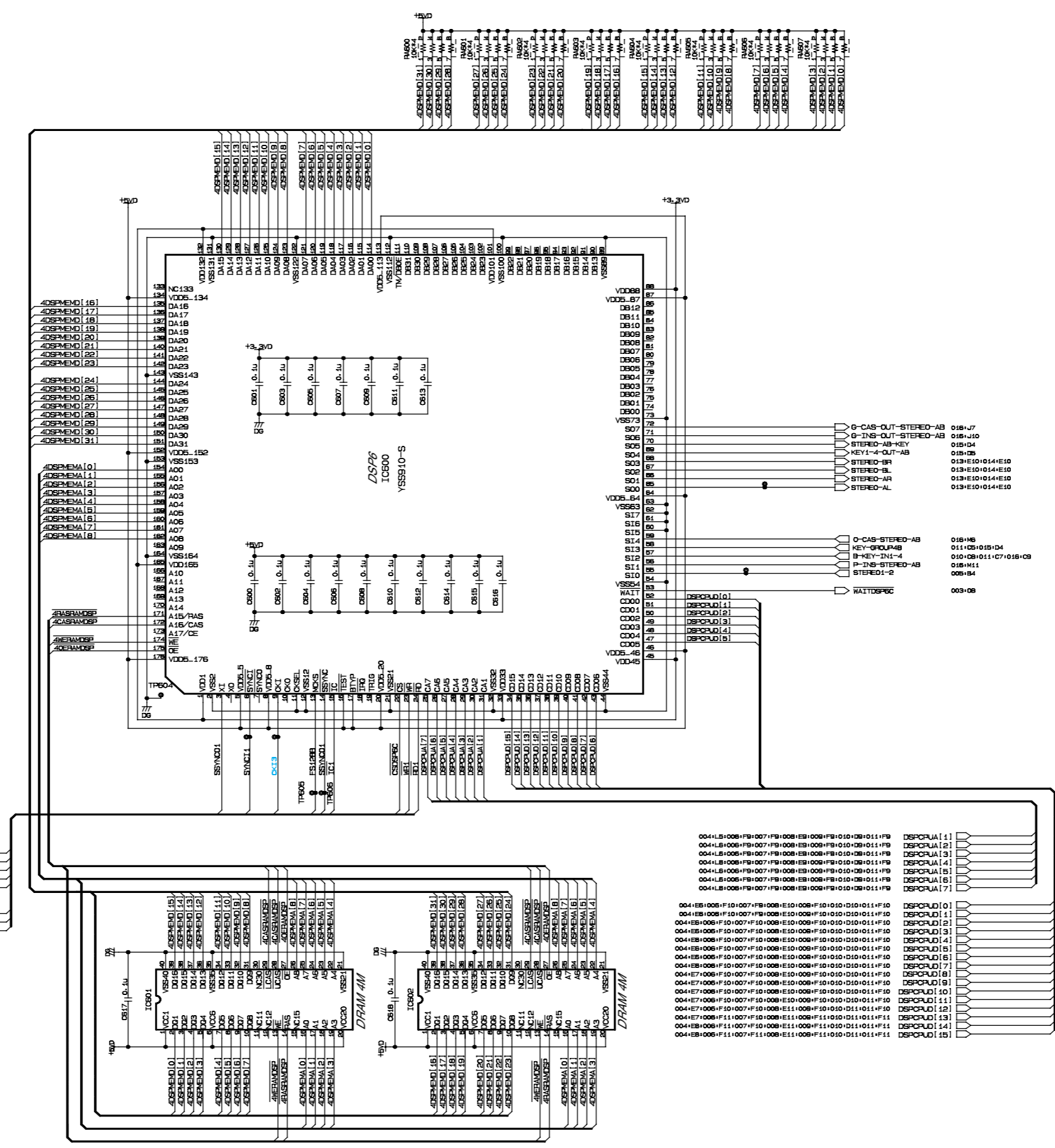


DSP 7 SECTION

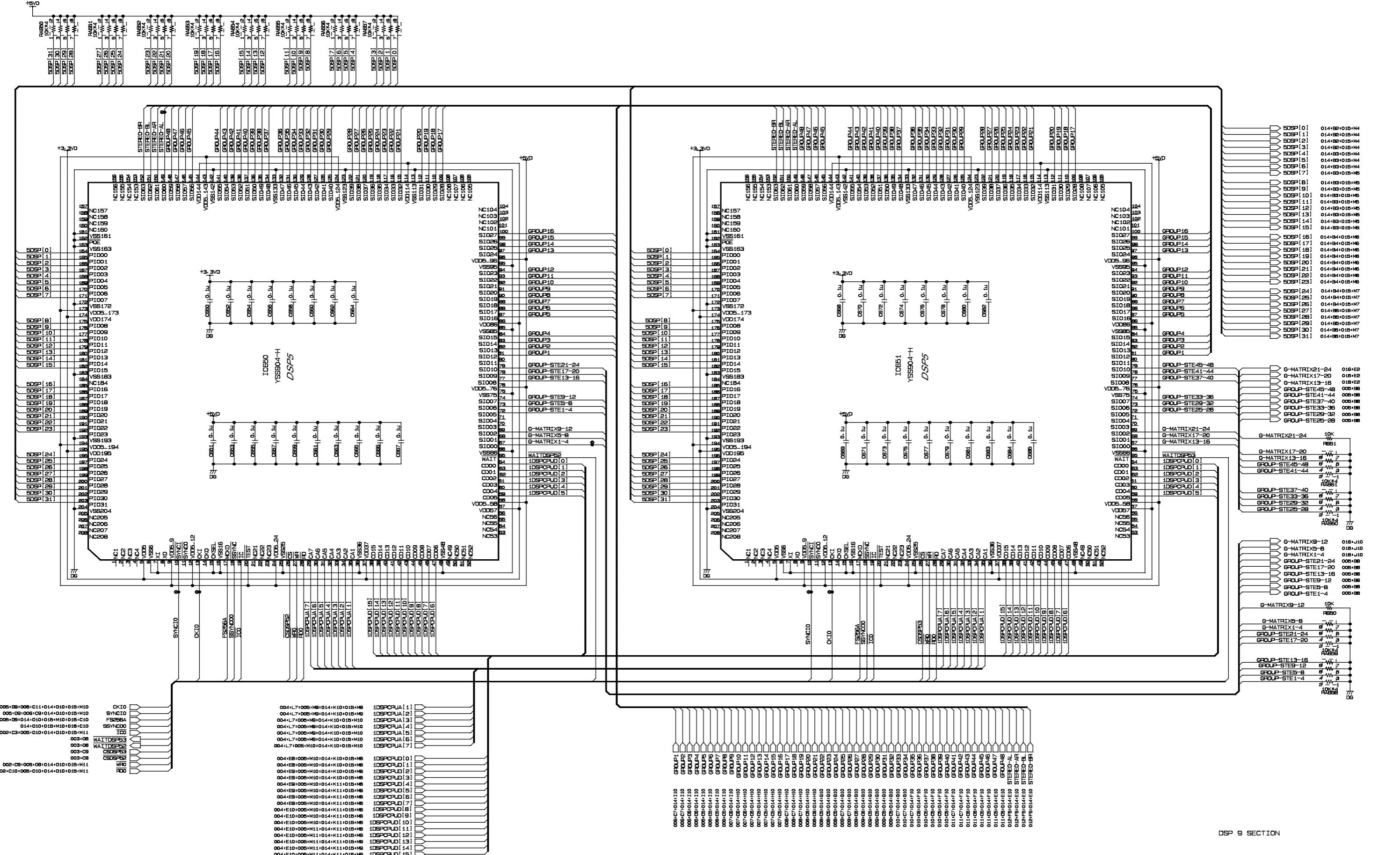
005+C9+007+M8+008+M10
 008+M8+010+N10+011+M8+018+C11
 008+N10+007+M8+008+M10+018+C10
 002+C2+006+N10+007+M8+008+M10+010+010+011+M8
 008+C11

003+C5
 CS0SPRC
 WFI1
 RD1

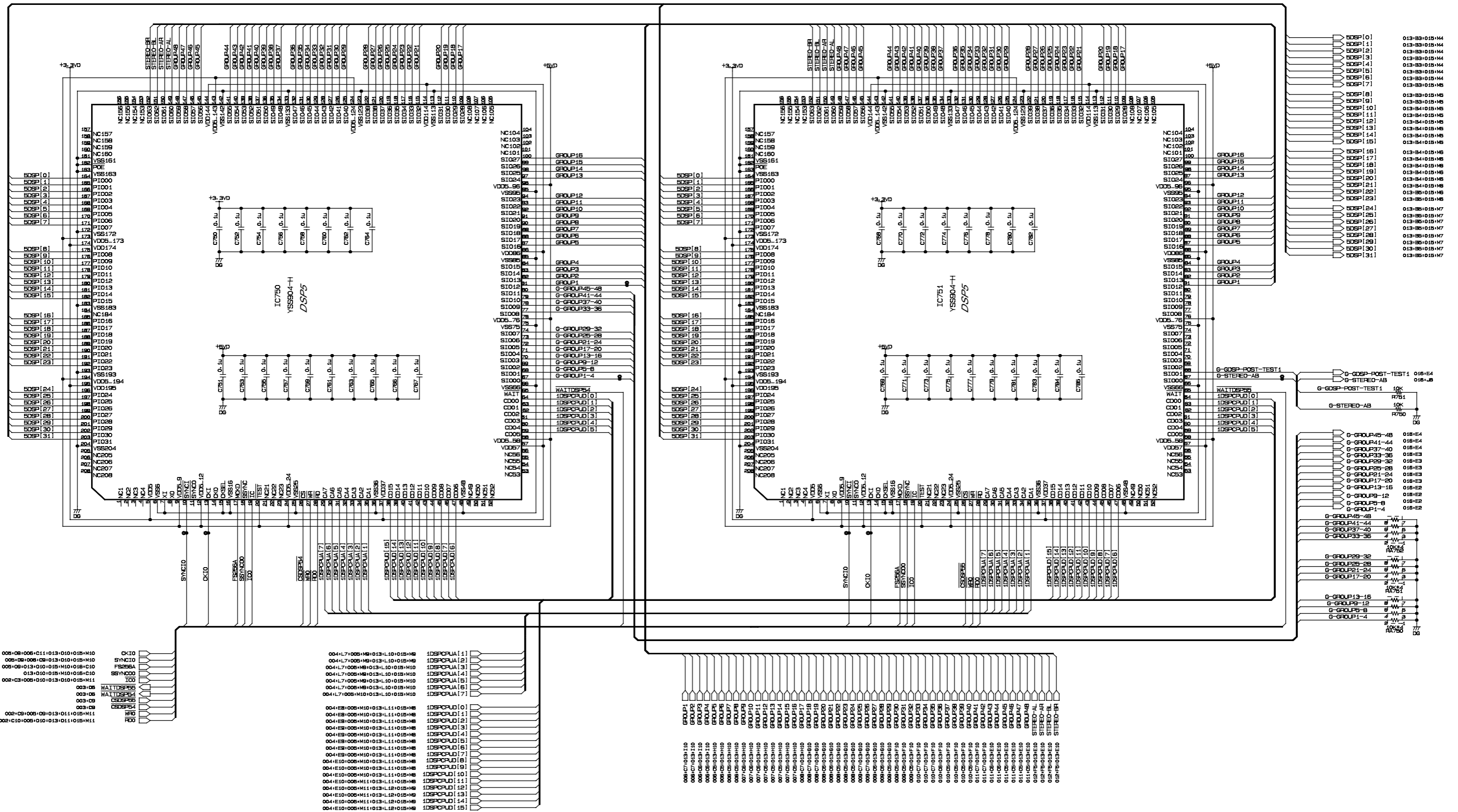
SYNCT1
 FS12B8
 SYNCD1
 TC1
 CK13

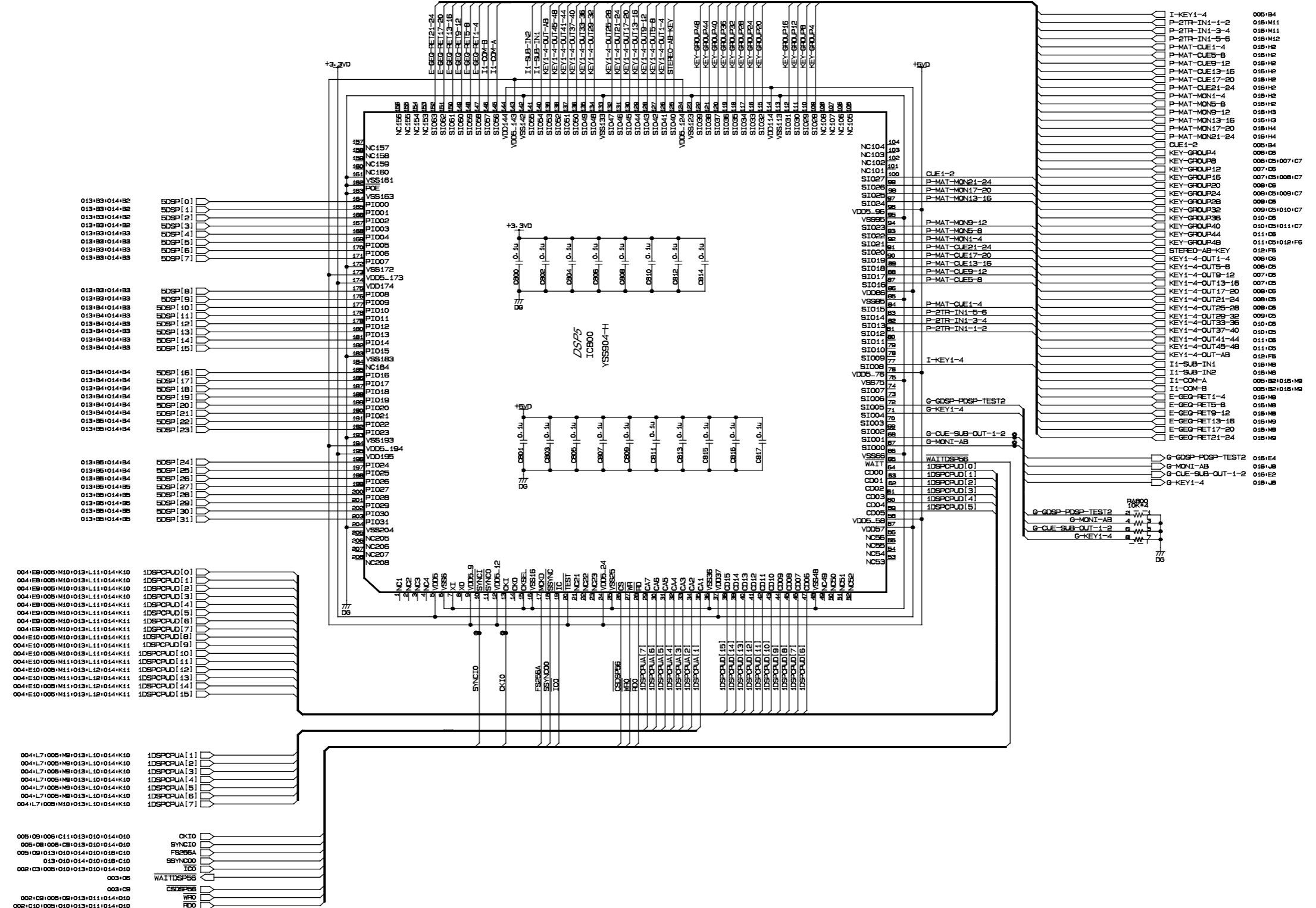


DSP B SECTION



DSP 9 SECTION

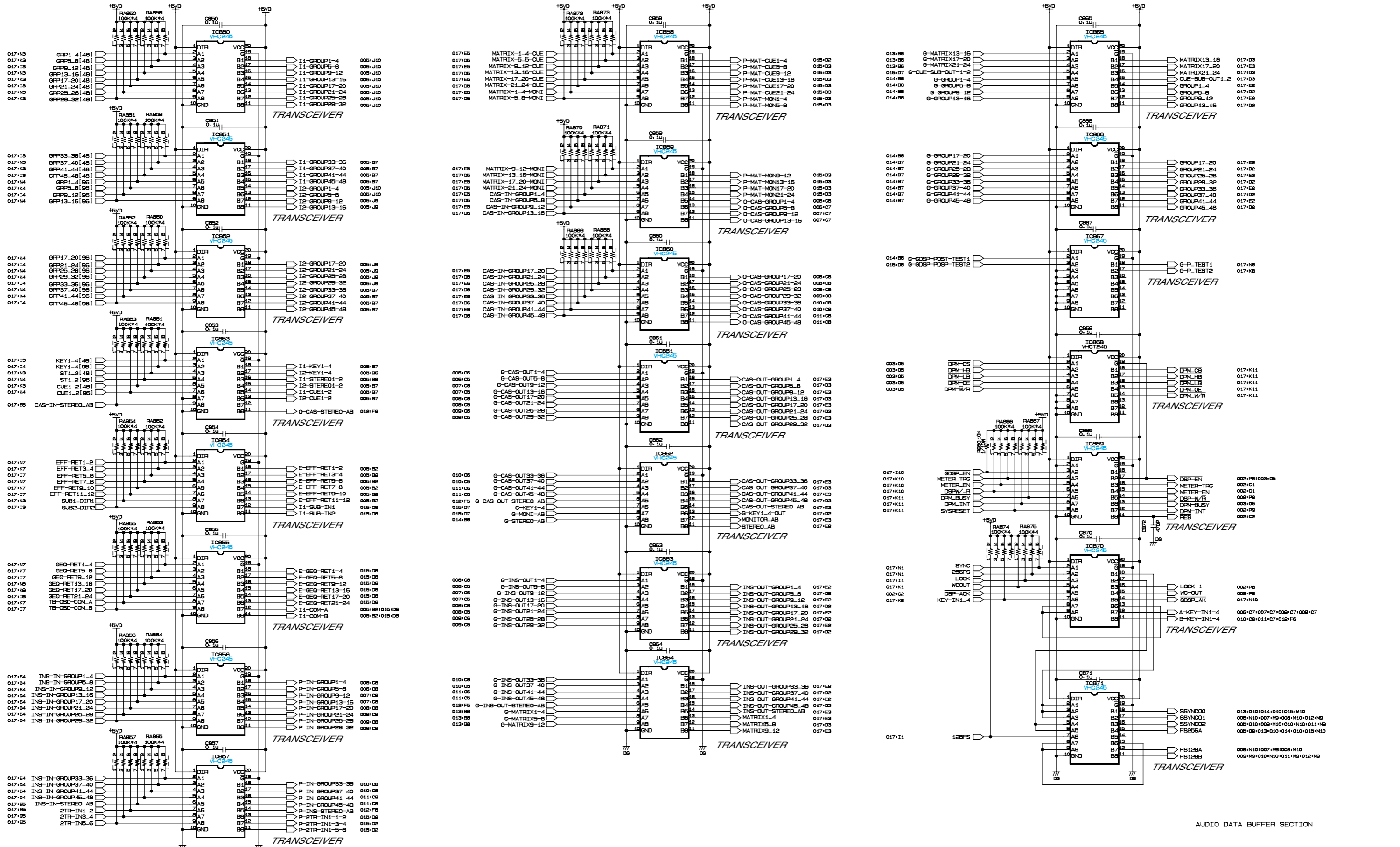




DSP 11 SECTION

GDB CIRCUIT DIAGRAM 016 (DSP1D)

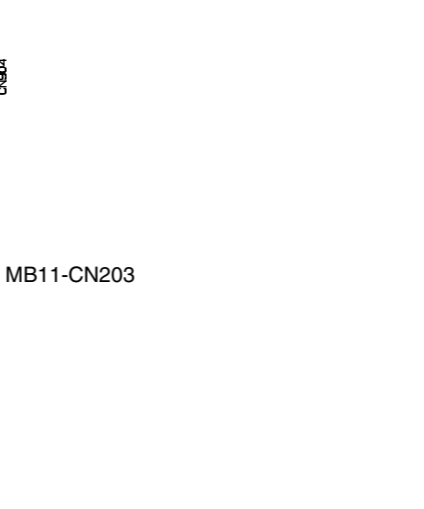
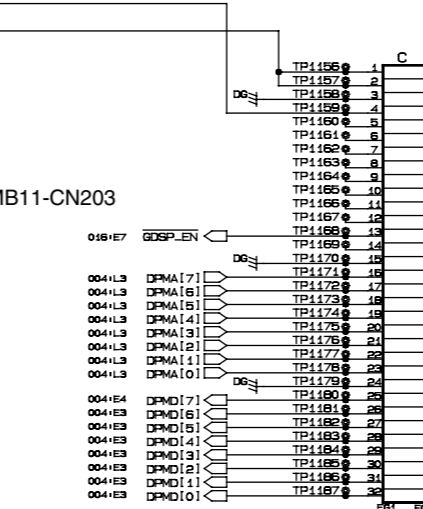
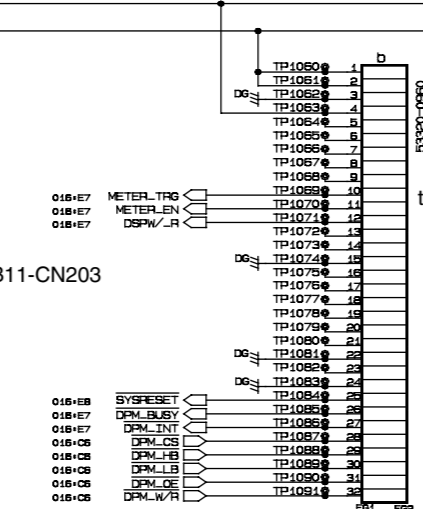
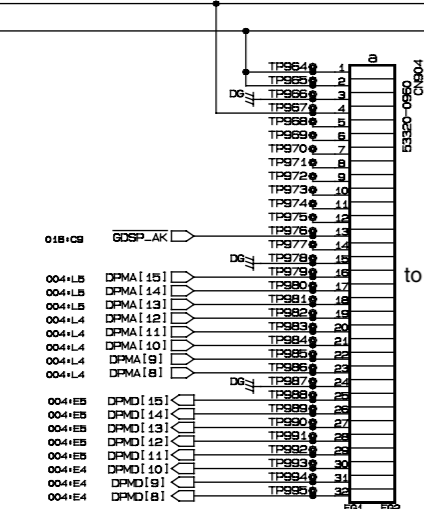
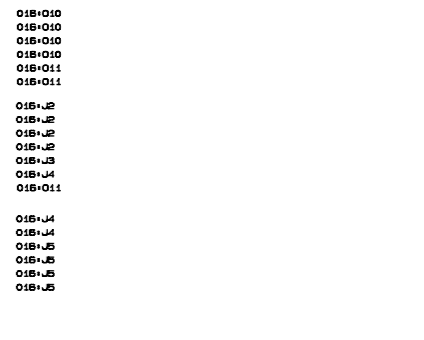
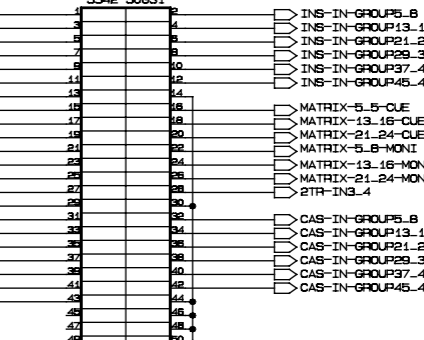
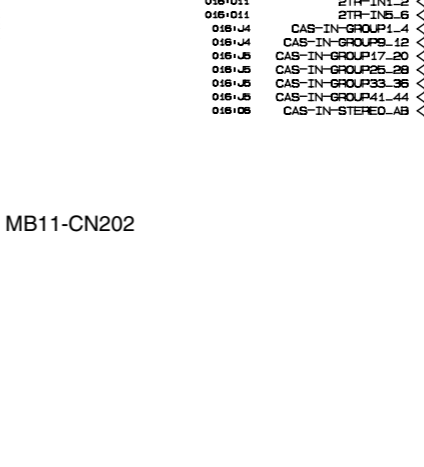
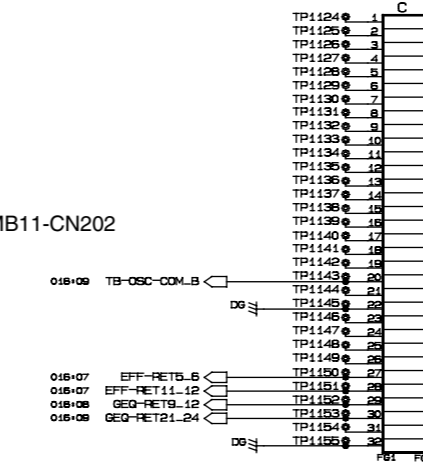
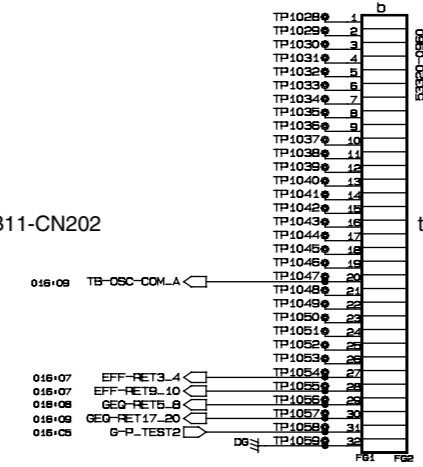
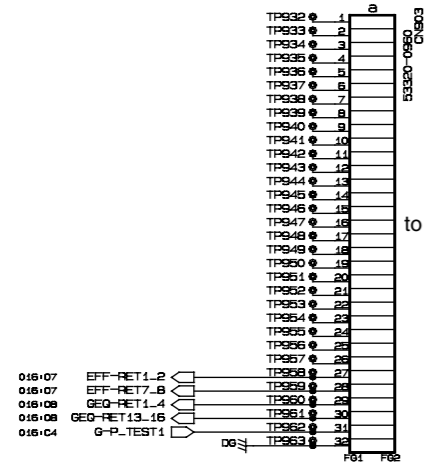
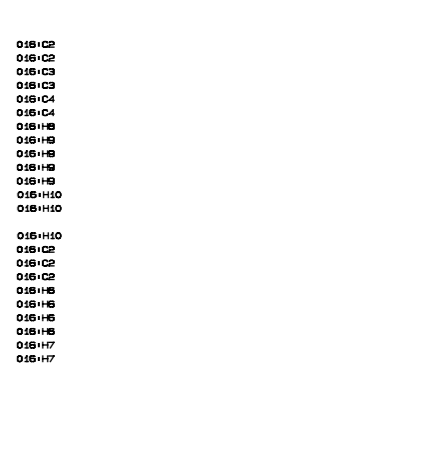
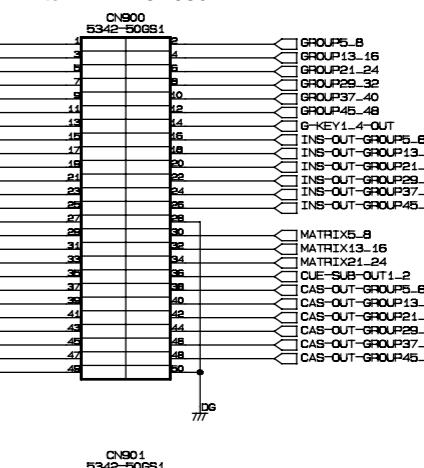
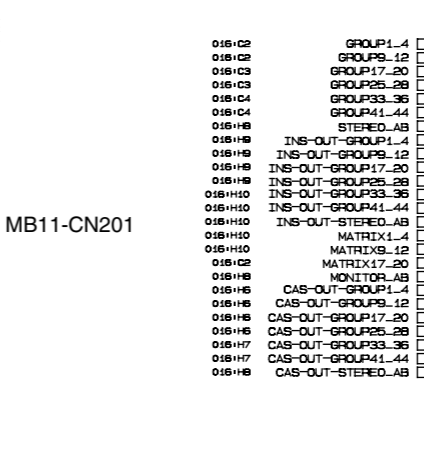
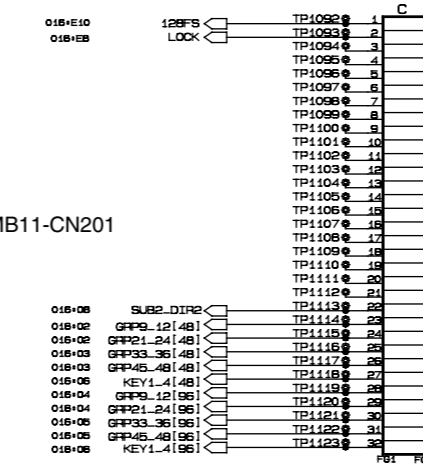
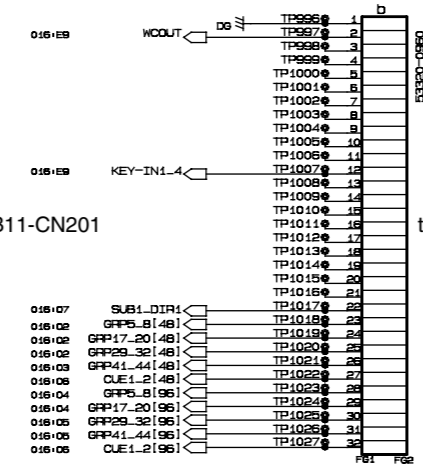
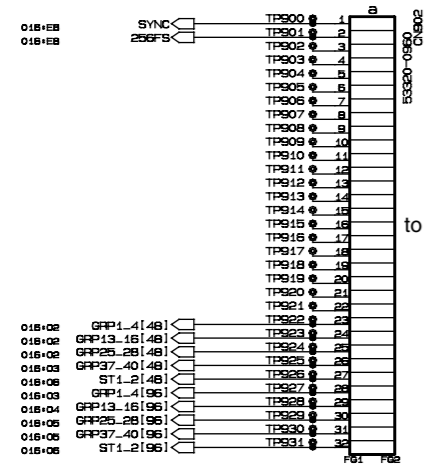
DSP1D



AUDIO DATA BUFFER SECTION

GDB CIRCUIT DIAGRAM 017 (DSP1D)

DSP1D



CONNECTOR SECTION

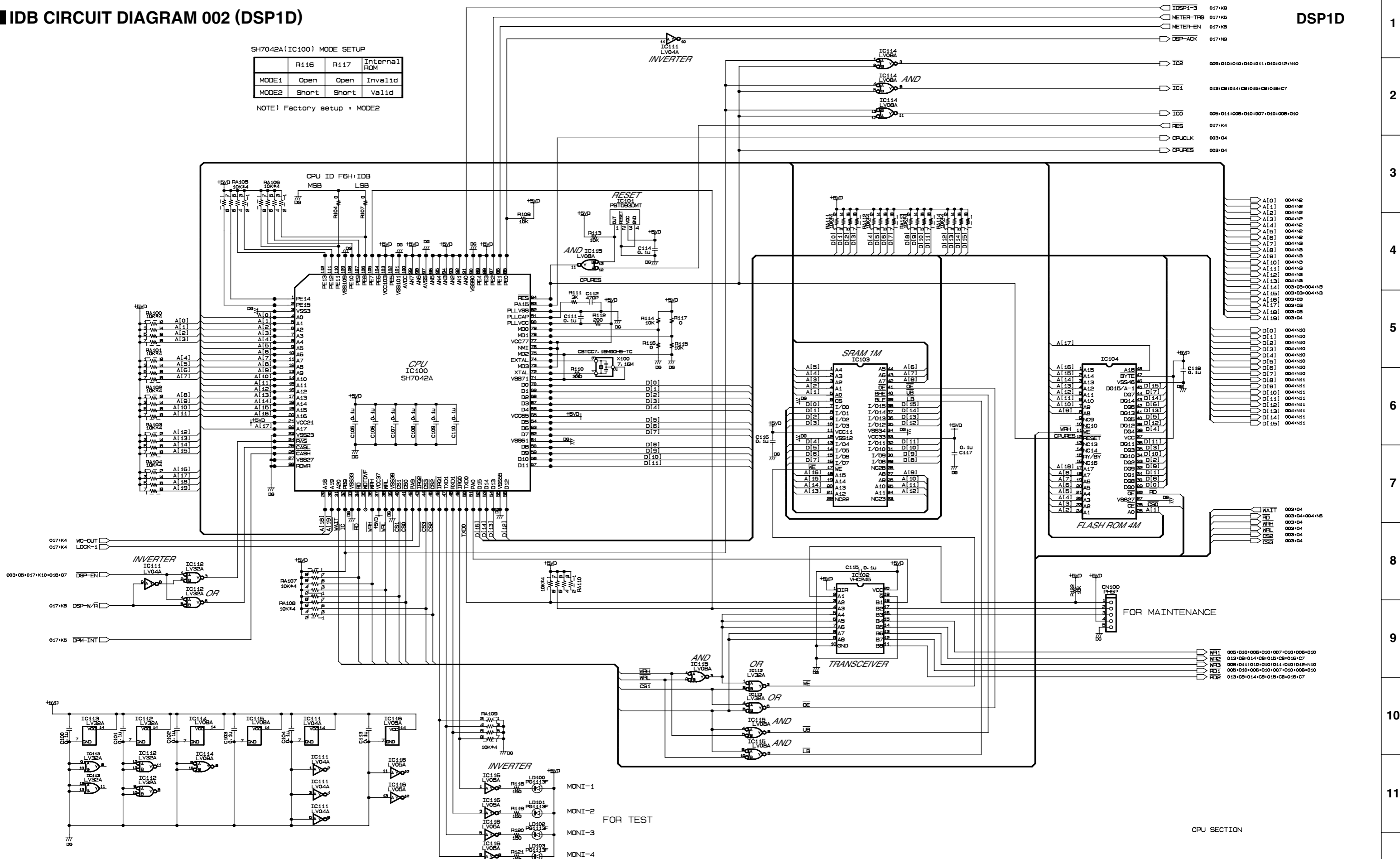
■ IDB CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D

SH7042A(IC100) MODE SETUP

	R116	R117	Internal ROM
MODE1	Open	Open	Invalid
MODE2	Short	Short	Valid

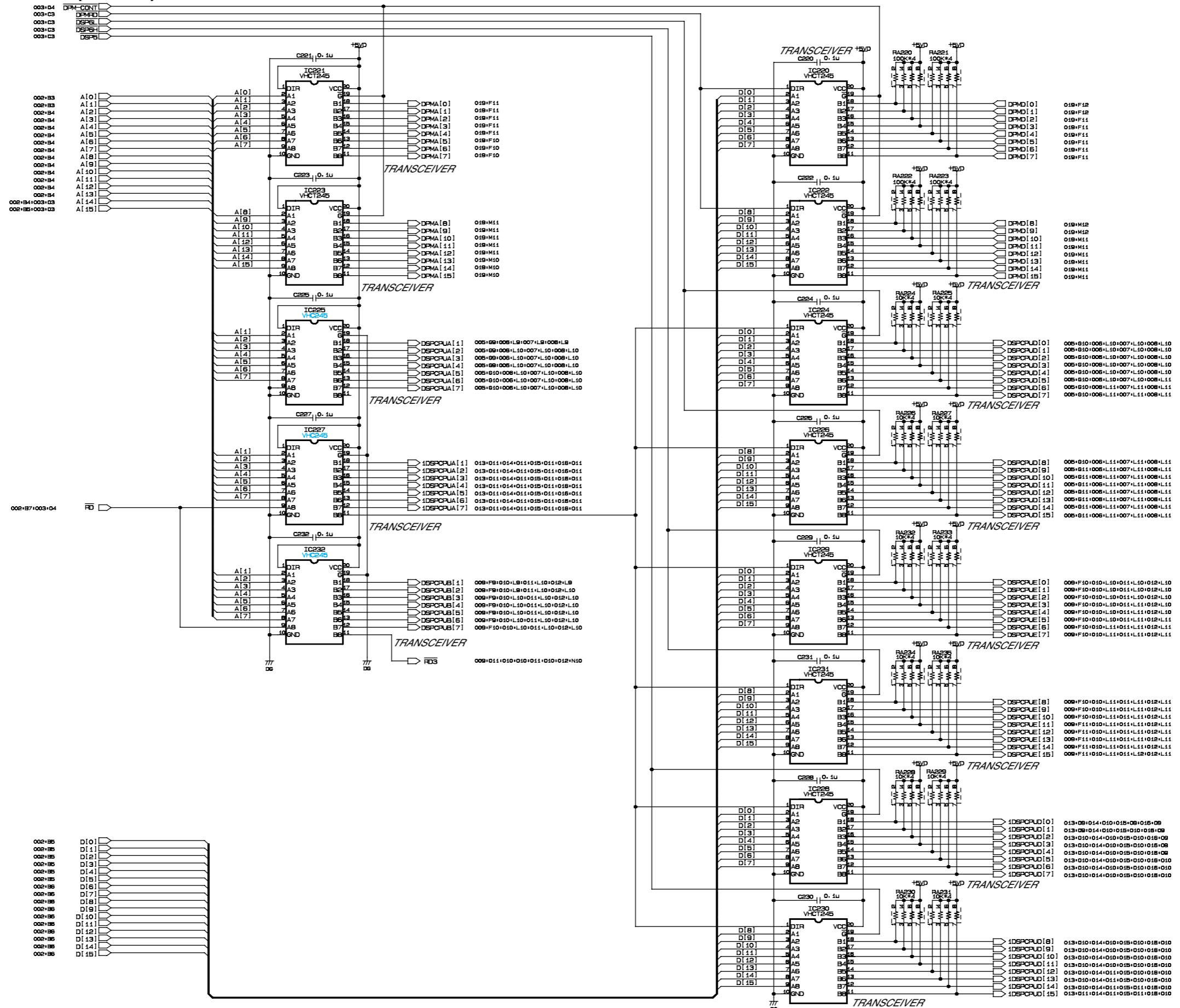
NOTE) Factory setup : MODE2

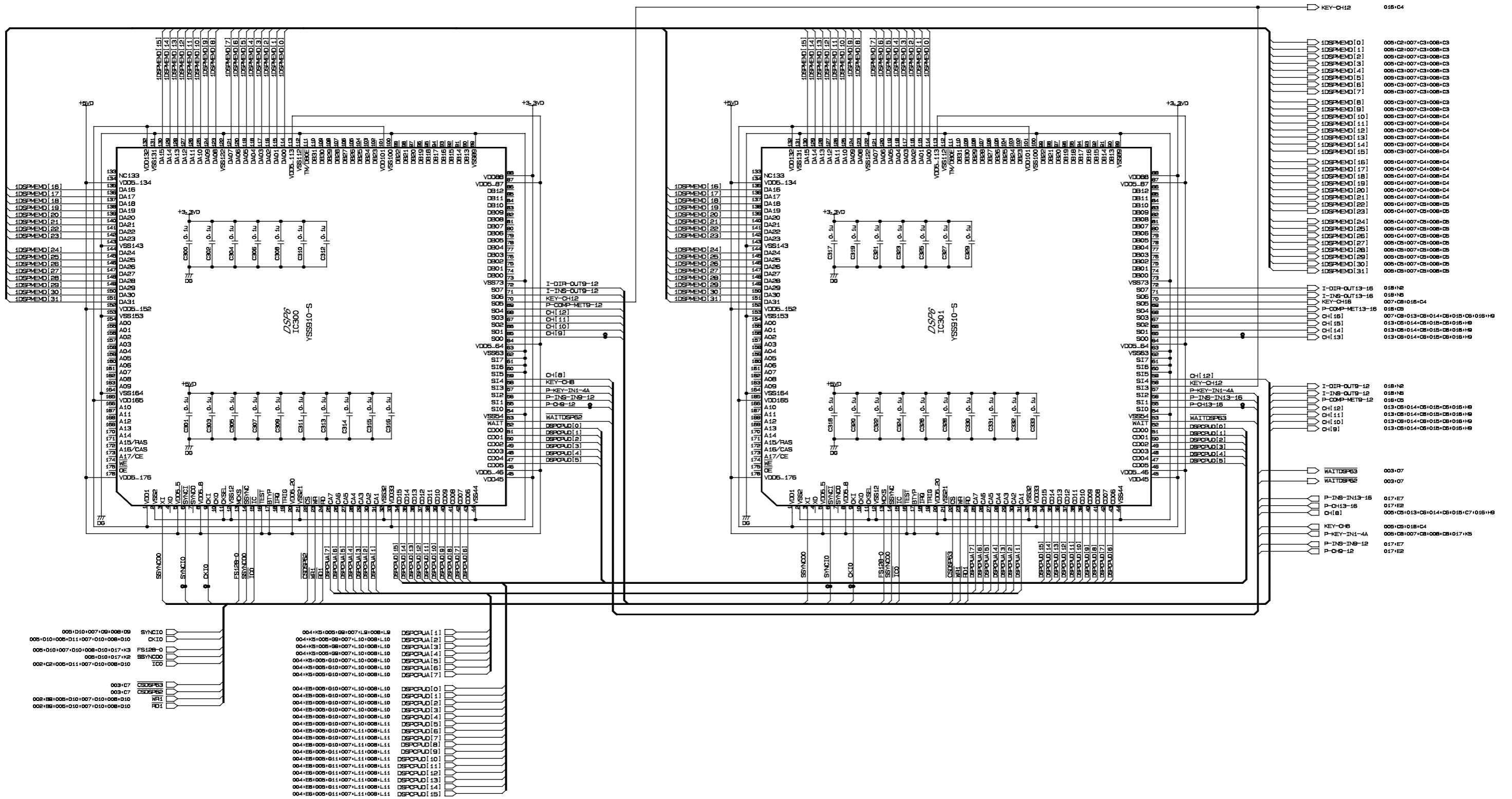


CPU SECTION

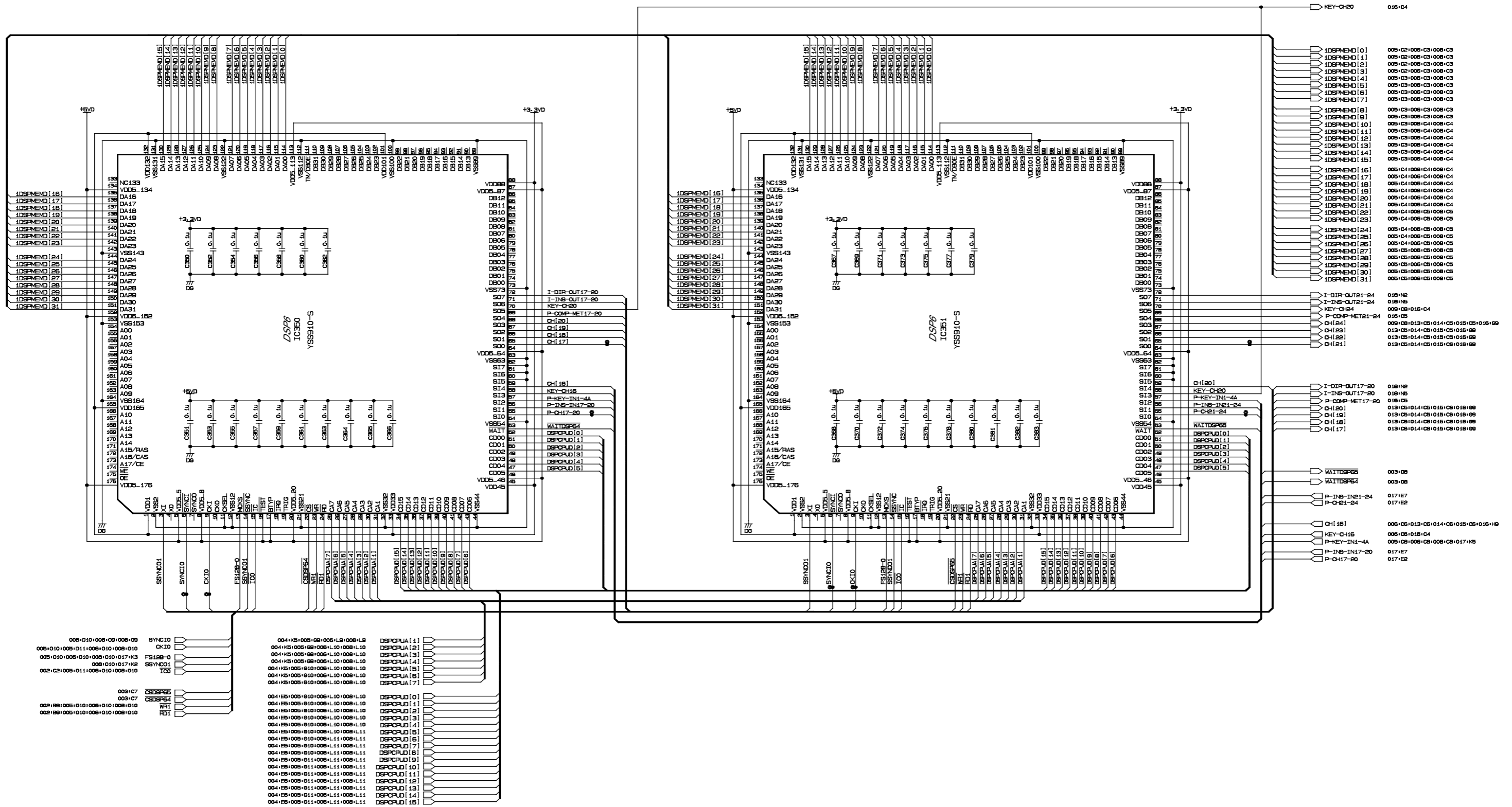
IBD CIRCUIT DIAGRAM 004 (DSP1D)

DSP1D

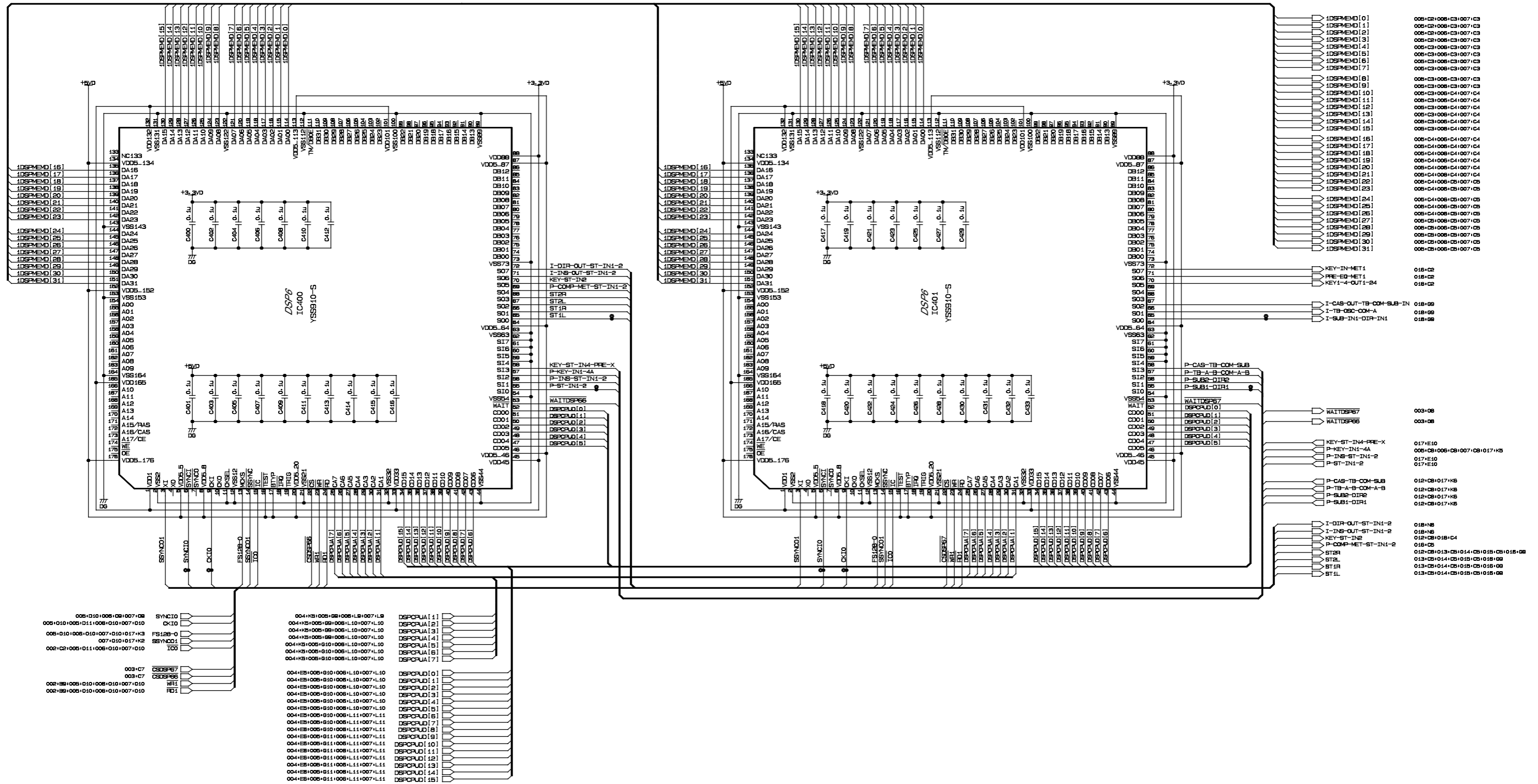




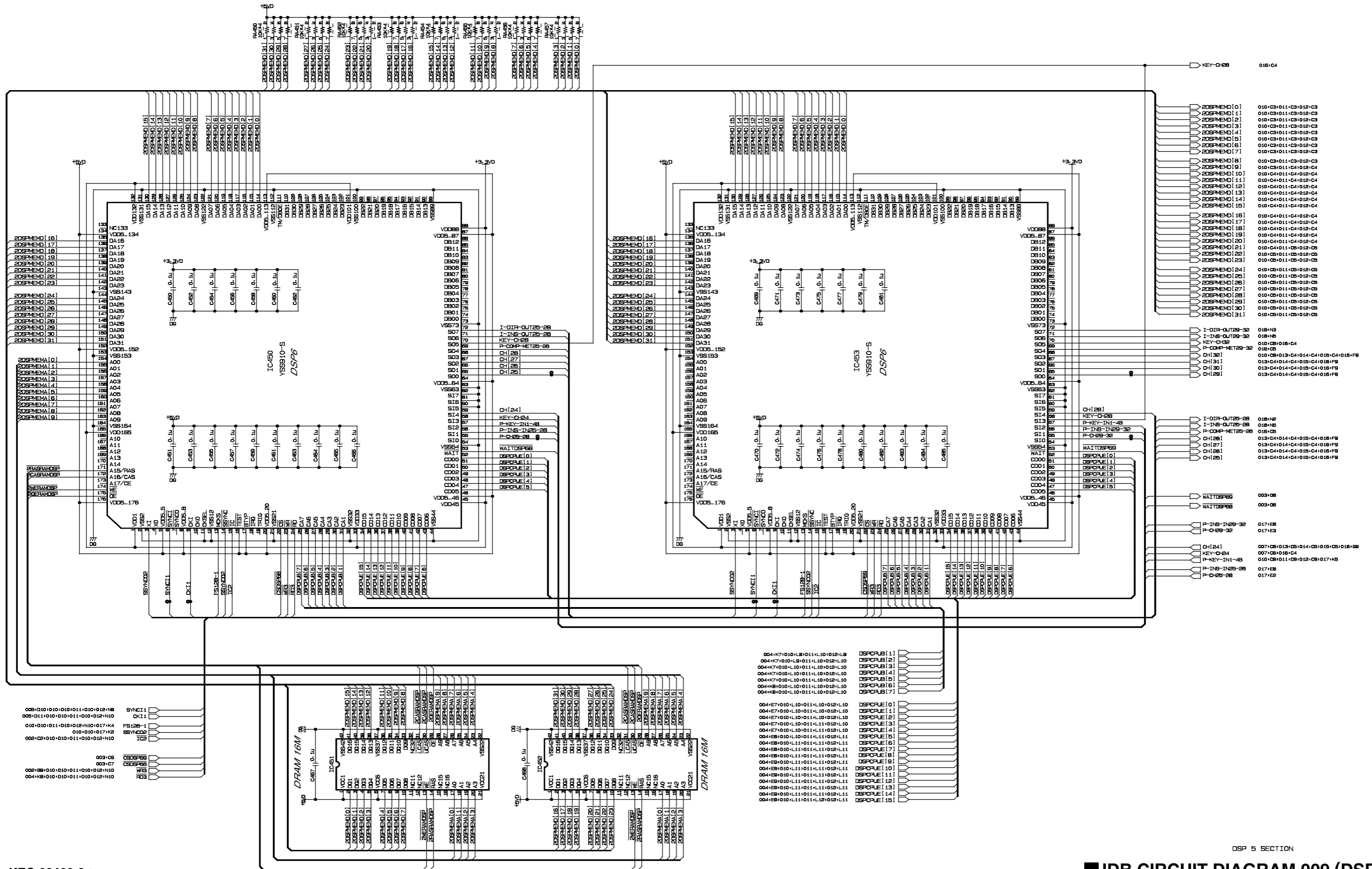
DSP 2 SECTION



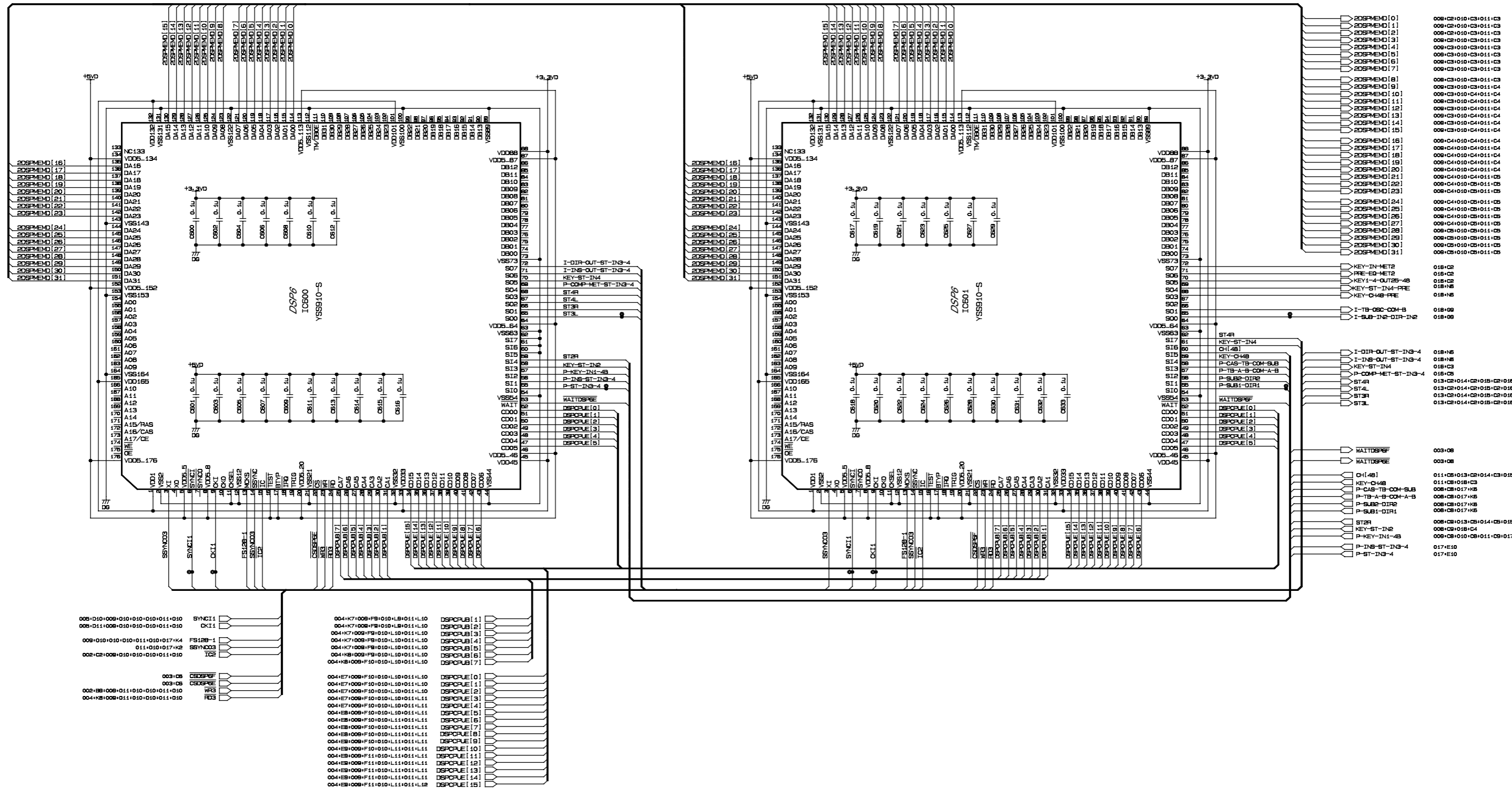
DSP 3 SECTION



DSP 4 SECTION



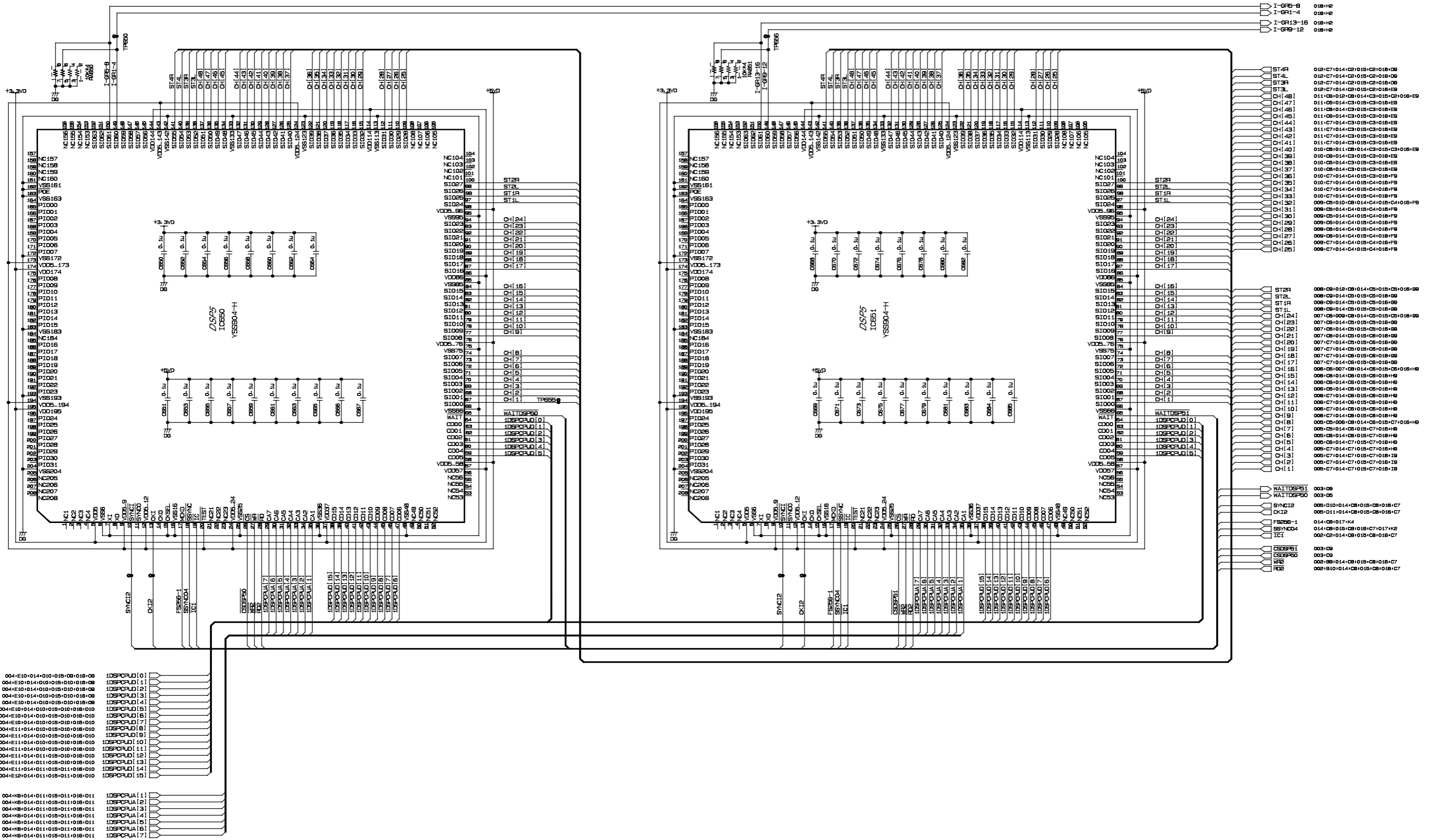
DSP 5 SECTION



DSP B SECTION

IDB CIRCUIT DIAGRAM 013 (DSP1D)

DSP1D



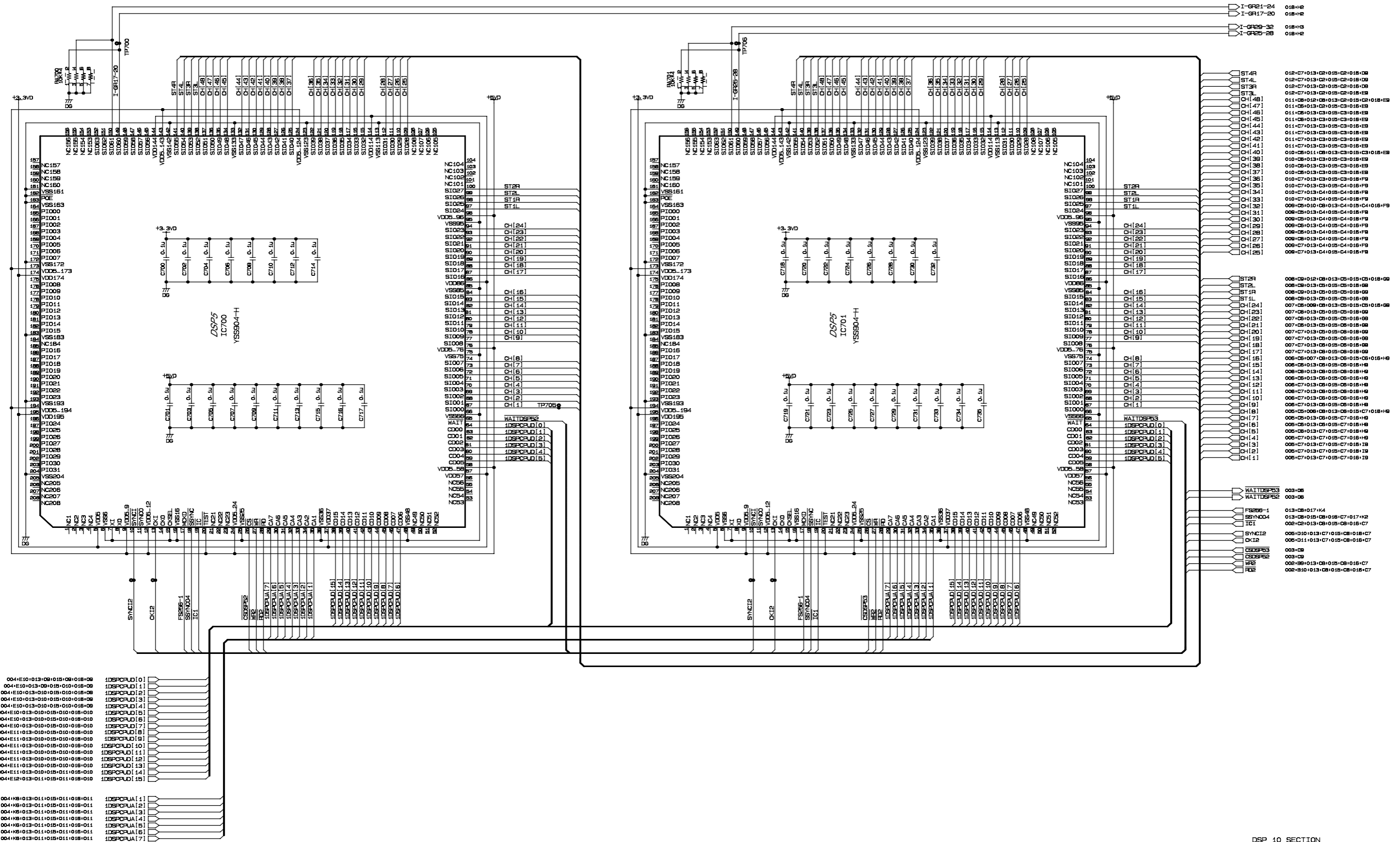
- 004+E10+014+010+015+09+016+08 1DSPCPUD[0]
- 004+E10+014+010+015+010+016+08 1DSPCPUD[1]
- 004+E10+014+010+015+010+016+08 1DSPCPUD[2]
- 004+E10+014+010+015+010+016+08 1DSPCPUD[3]
- 004+E10+014+010+015+010+016+08 1DSPCPUD[4]
- 004+E10+014+010+015+010+016+08 1DSPCPUD[5]
- 004+E10+014+010+015+010+016+08 1DSPCPUD[6]
- 004+E10+014+010+015+010+016+08 1DSPCPUD[7]
- 004+E11+014+010+015+010+016+08 1DSPCPUD[8]
- 004+E11+014+010+015+010+016+08 1DSPCPUD[9]
- 004+E11+014+010+015+010+016+08 1DSPCPUD[10]
- 004+E11+014+010+015+010+016+08 1DSPCPUD[11]
- 004+E11+014+010+015+010+016+08 1DSPCPUD[12]
- 004+E11+014+010+015+010+016+08 1DSPCPUD[13]
- 004+E11+014+010+015+010+016+08 1DSPCPUD[14]
- 004+E12+014+011+015+011+016+08 1DSPCPUD[15]

DSP 9 SECTION

IDB CIRCUIT DIAGRAM 013 (DSP1D)

IDB CIRCUIT DIAGRAM 014 (DSP1D)

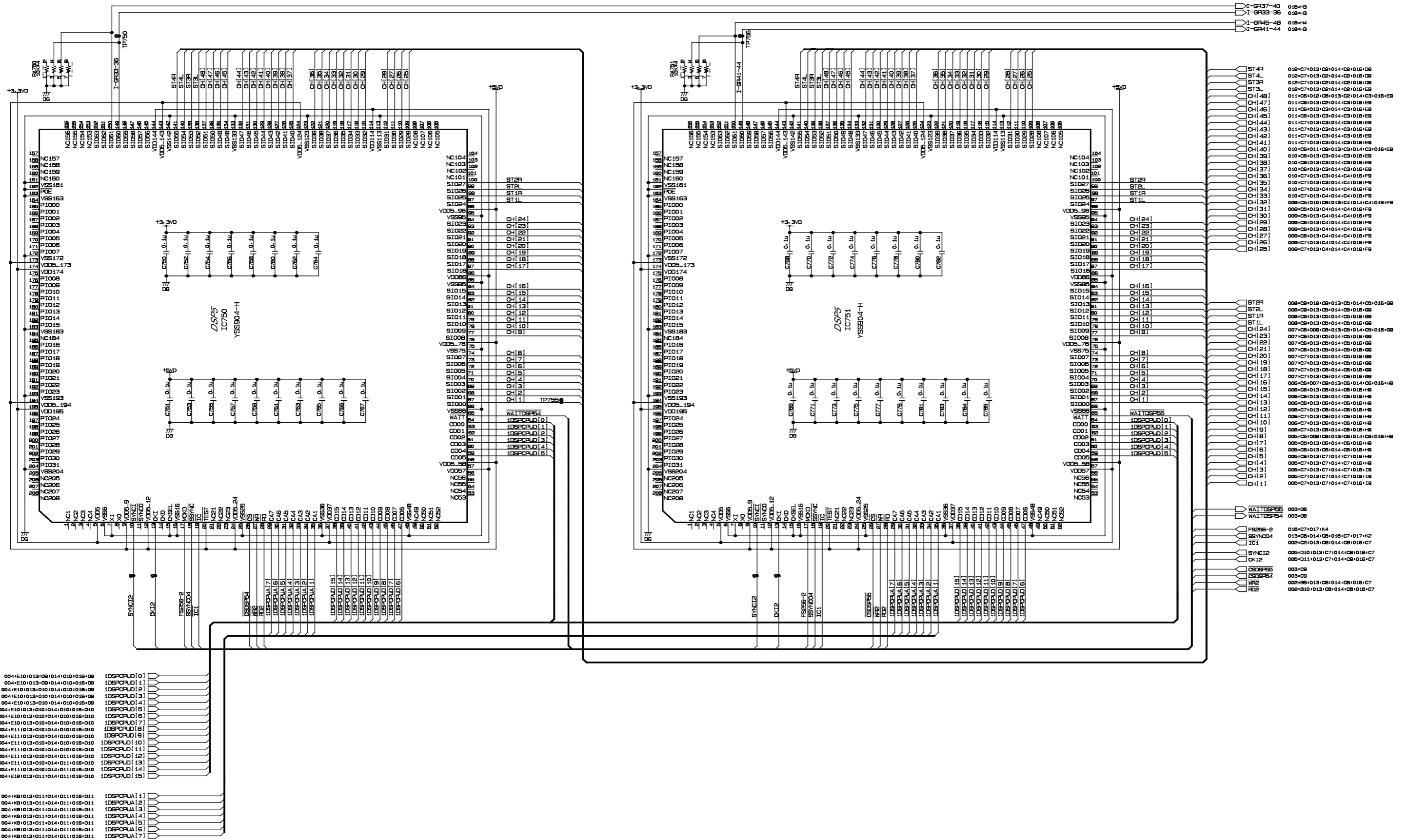
DSP1D



DSP 10 SECTION

IDB CIRCUIT DIAGRAM 015 (DSP1D)

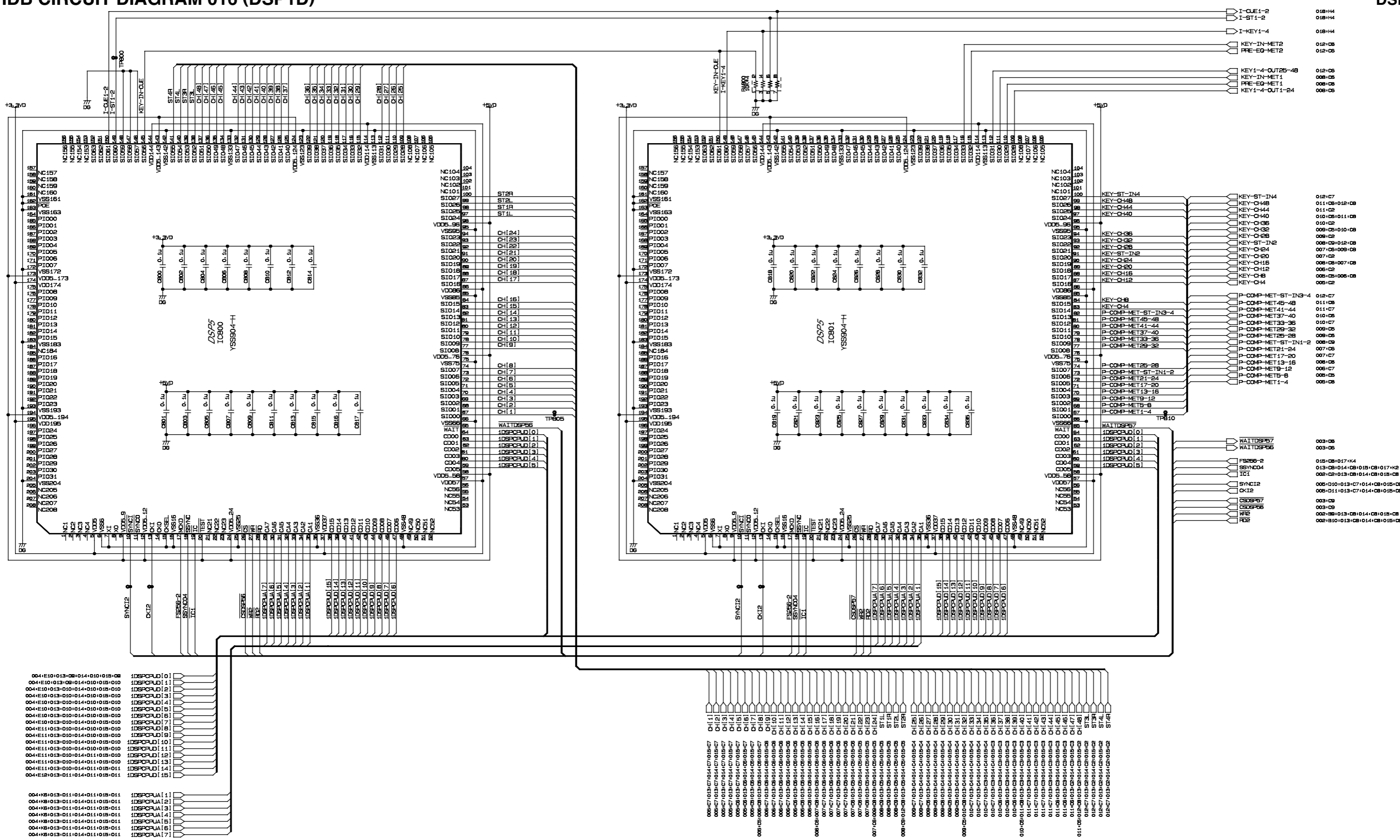
DSP1D



DSP 11 SECTION

IDB CIRCUIT DIAGRAM 016 (DSP1D)

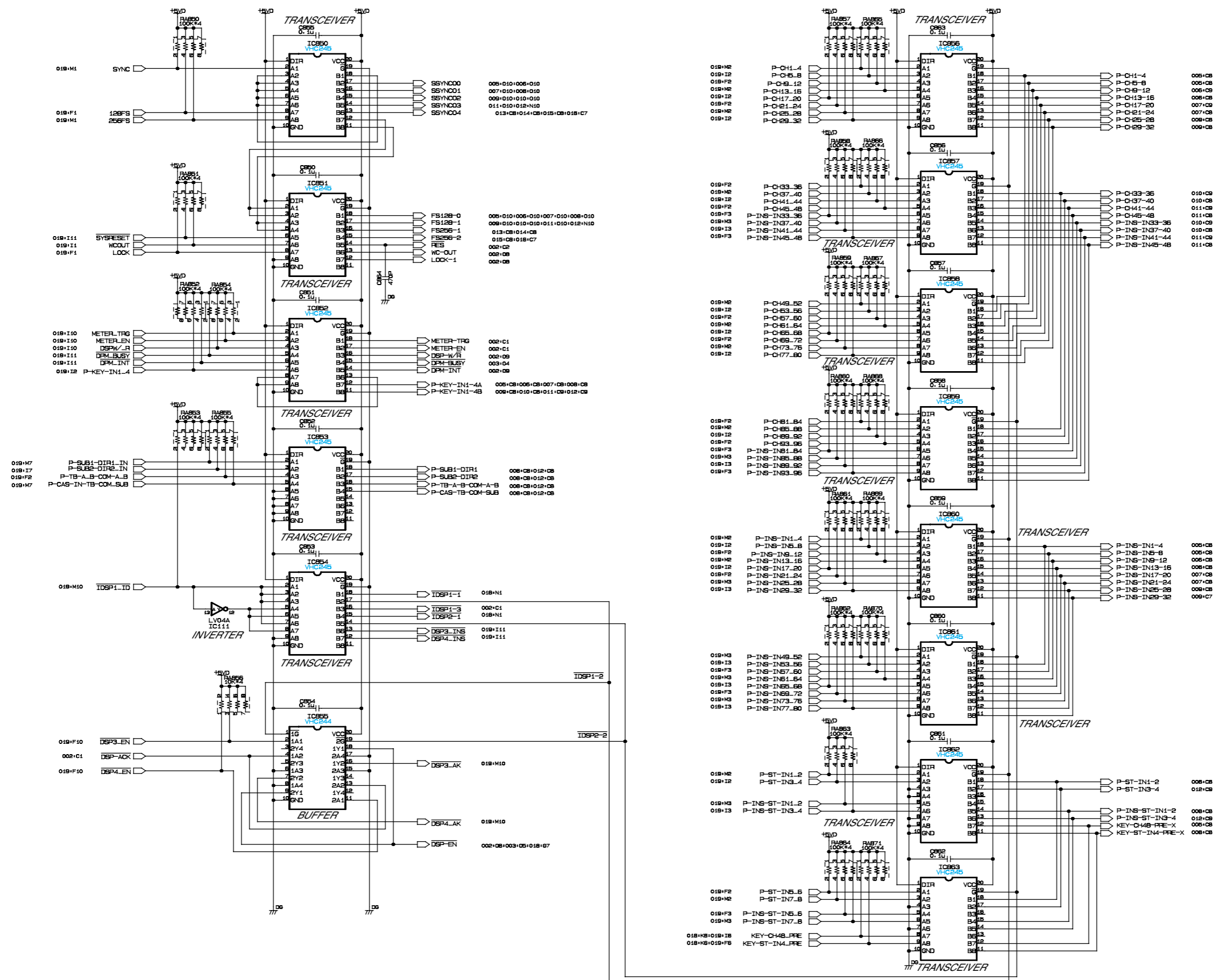
DSP1D



DSP 12 SECTION

1D B CIRCUIT DIAGRAM 017 (DSP1D)

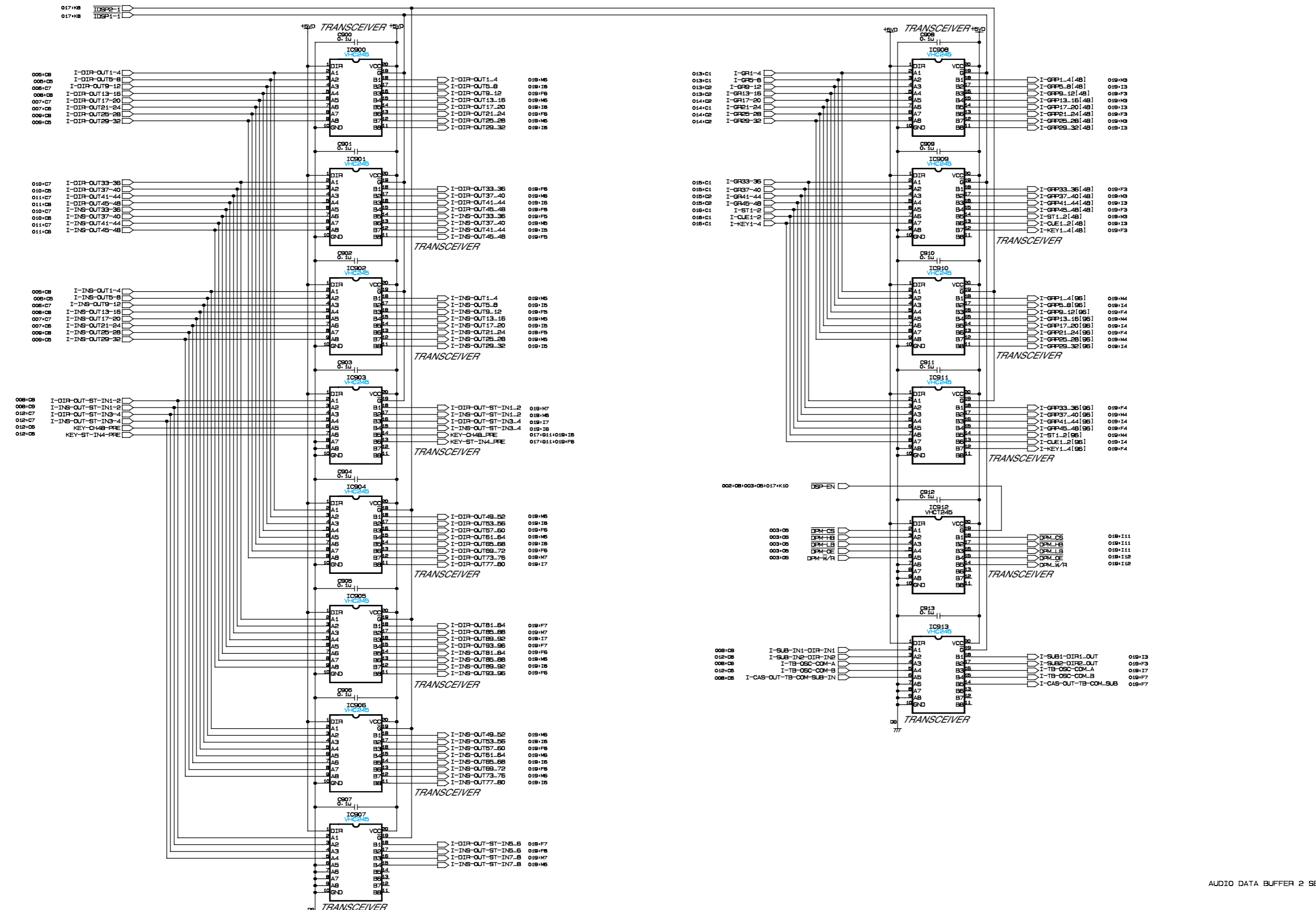
DSP1D



AUDIO DATA BUFFER 1 SECTION

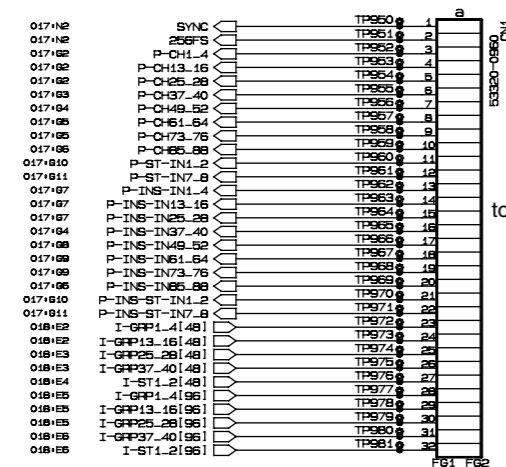
IDB CIRCUIT DIAGRAM 018 (DSP1D)

DSP1D

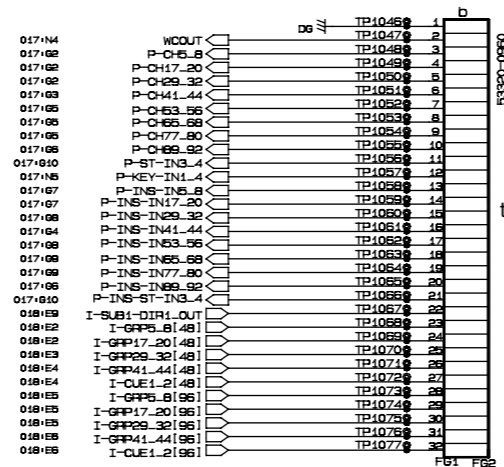


■ IDB CIRCUIT DIAGRAM 019 (DSP1D)

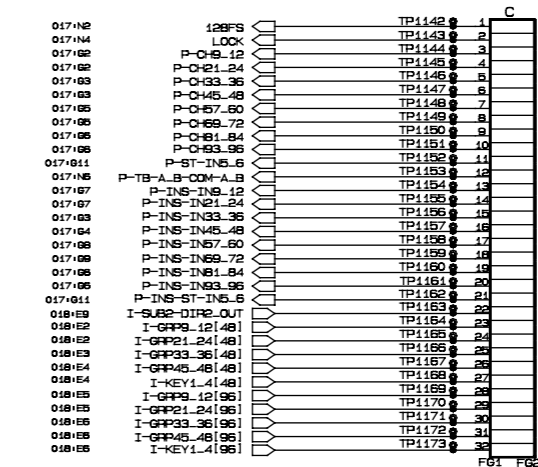
DSP1D



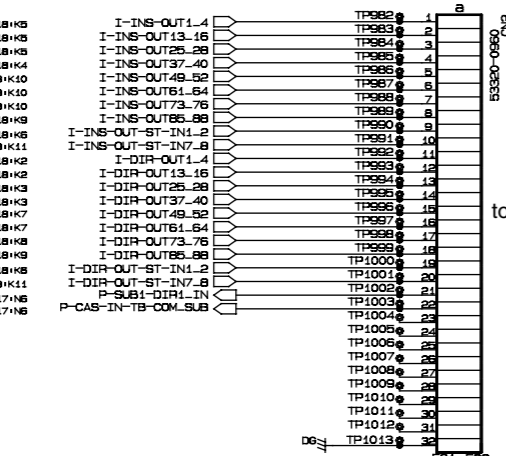
to MB11-CN301 (CN401)



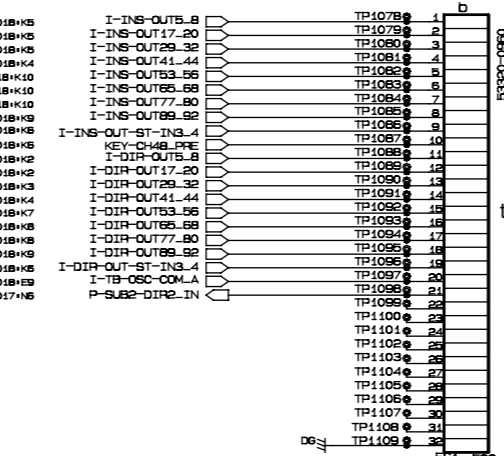
to MB11-CN301 (CN401)



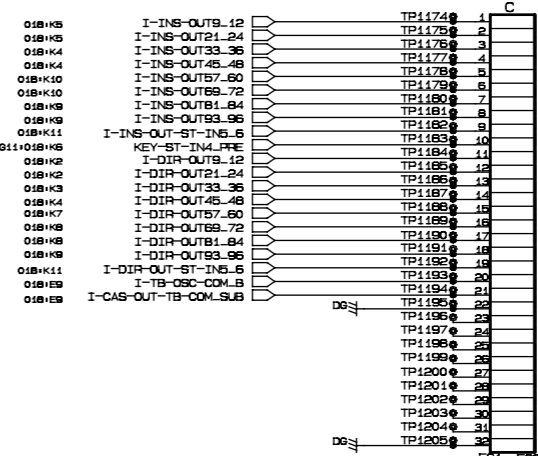
to MB11-CN301 (CN401)



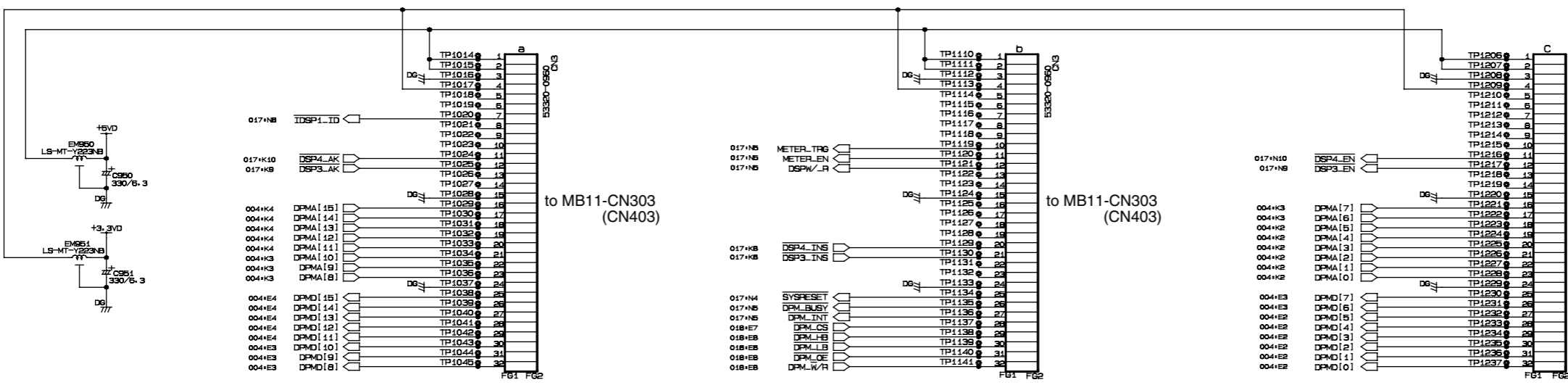
to MB11-CN302 (CN402)



to MB11-CN302 (CN402)



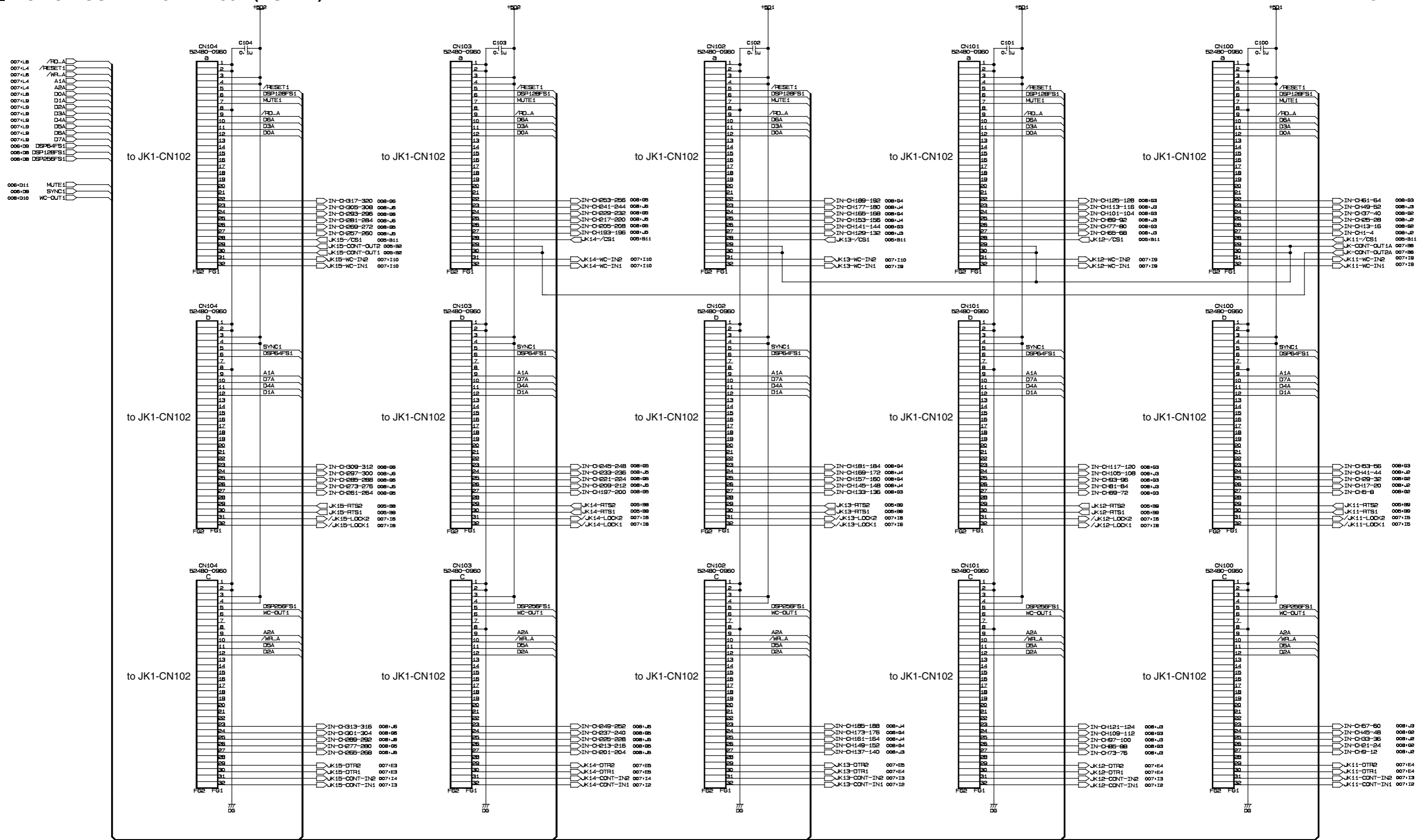
to MB11-CN302 (CN402)



(): DSP1D-EX CONNECTOR SECTION

IFC1 CIRCUIT DIAGRAM 002 (DSP1D)

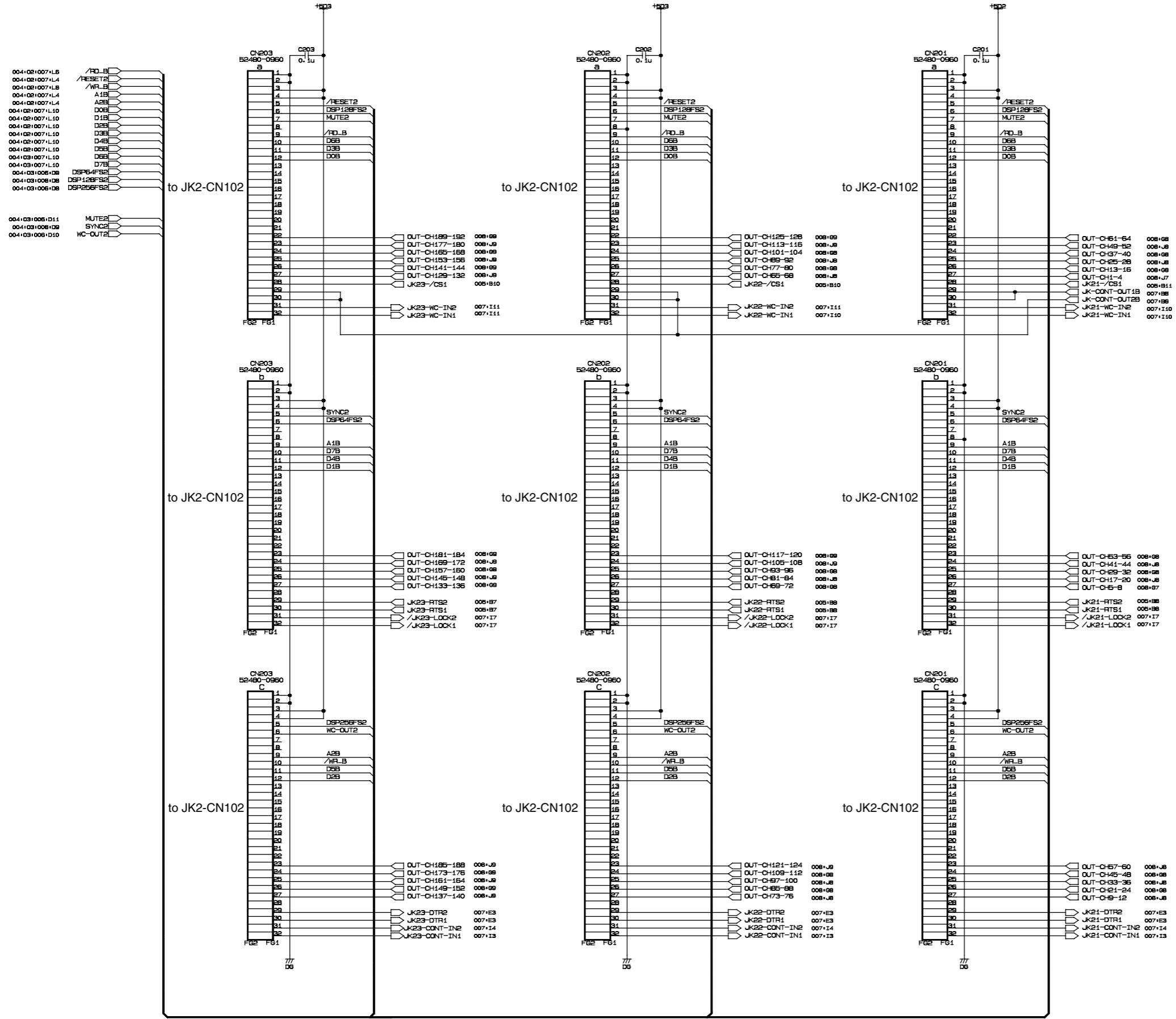
DSP1D



CONNECTOR 1 SECTION

IFC1 CIRCUIT DIAGRAM 003 (DSP1D)

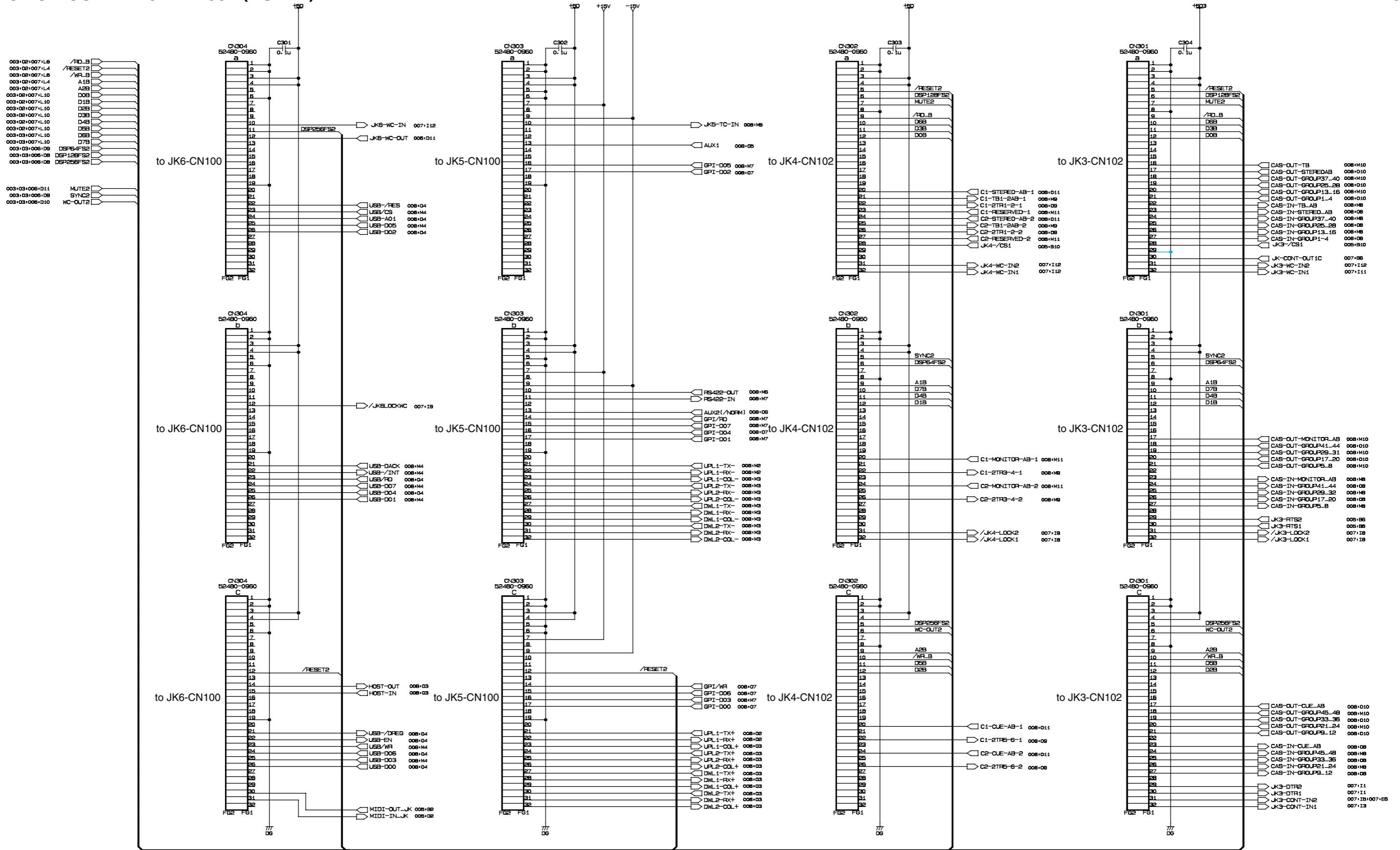
DSP1D



CONNECTOR 2 SECTION

IFC1 CIRCUIT DIAGRAM 004 (DSP1D)

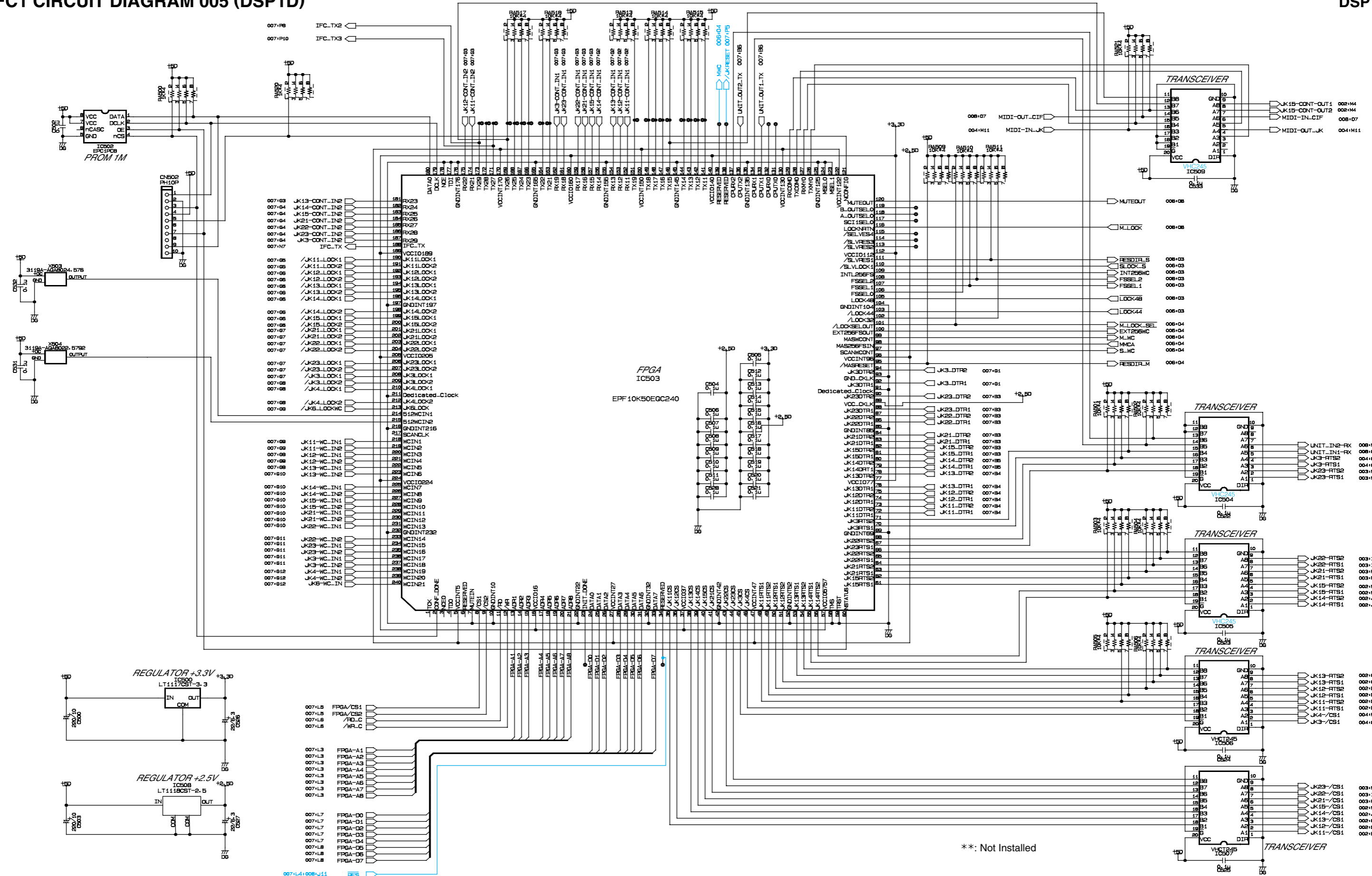
DSP1D



CONNECTOR 3 SECTION

IFC1 CIRCUIT DIAGRAM 005 (DSP1D)

DSP1D

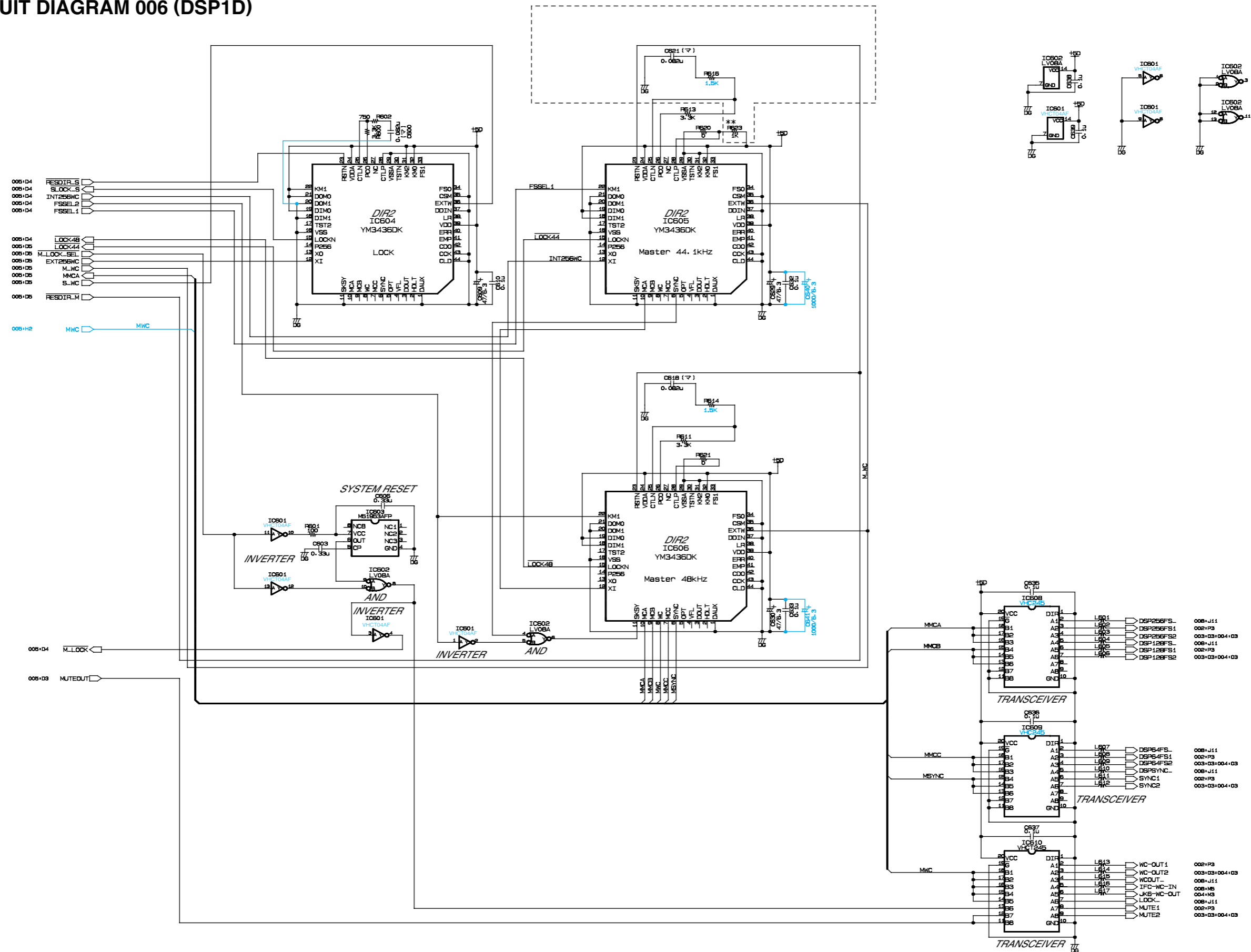


CLOCK SYSTEM & EMB I/F SECTION

IFC1 CIRCUIT DIAGRAM 005 (DSP1D)

IFC1 CIRCUIT DIAGRAM 006 (DSP1D)

DSP1D

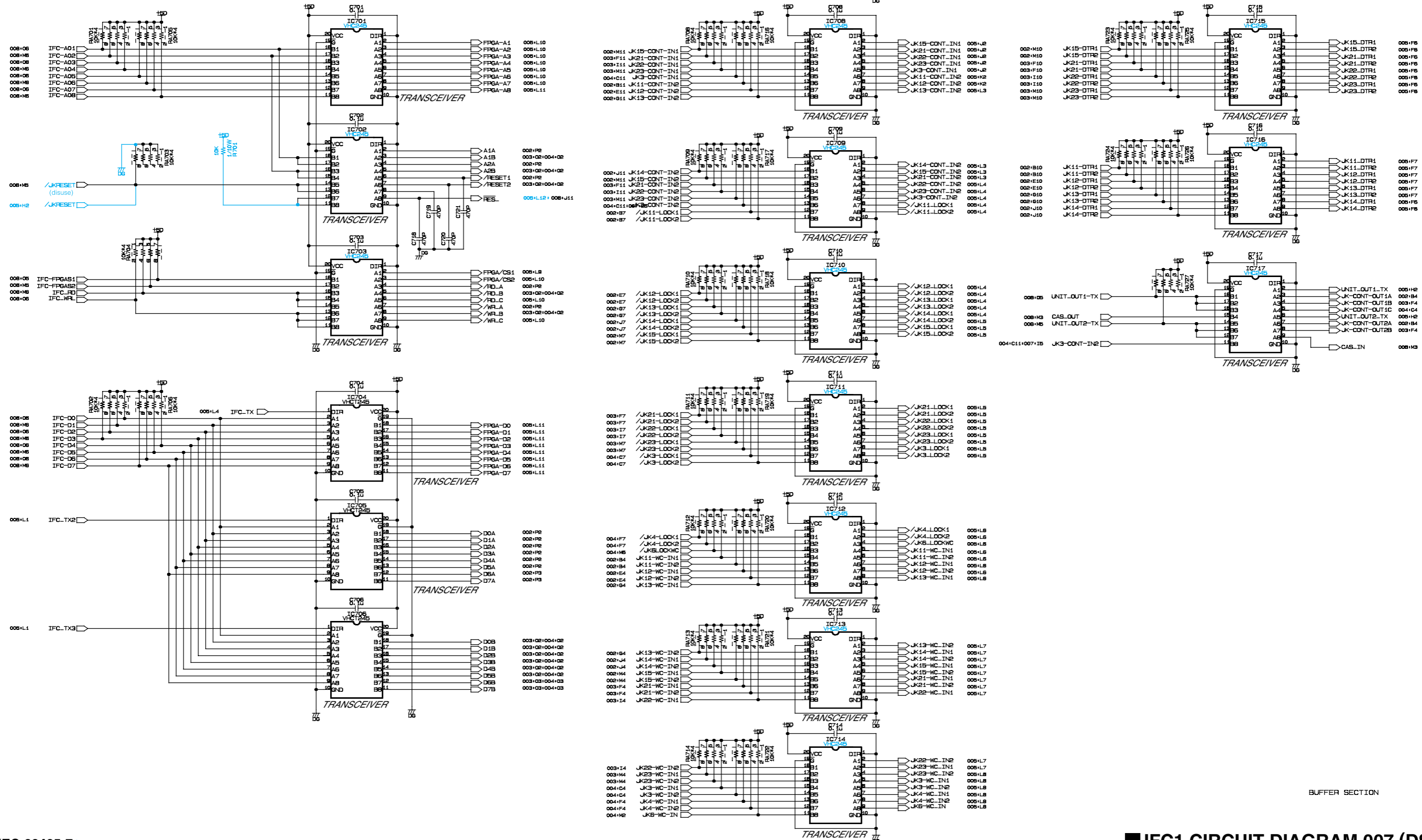


** : Not Installed
 (∇) : Mylar Capacitor

PLL SECTION

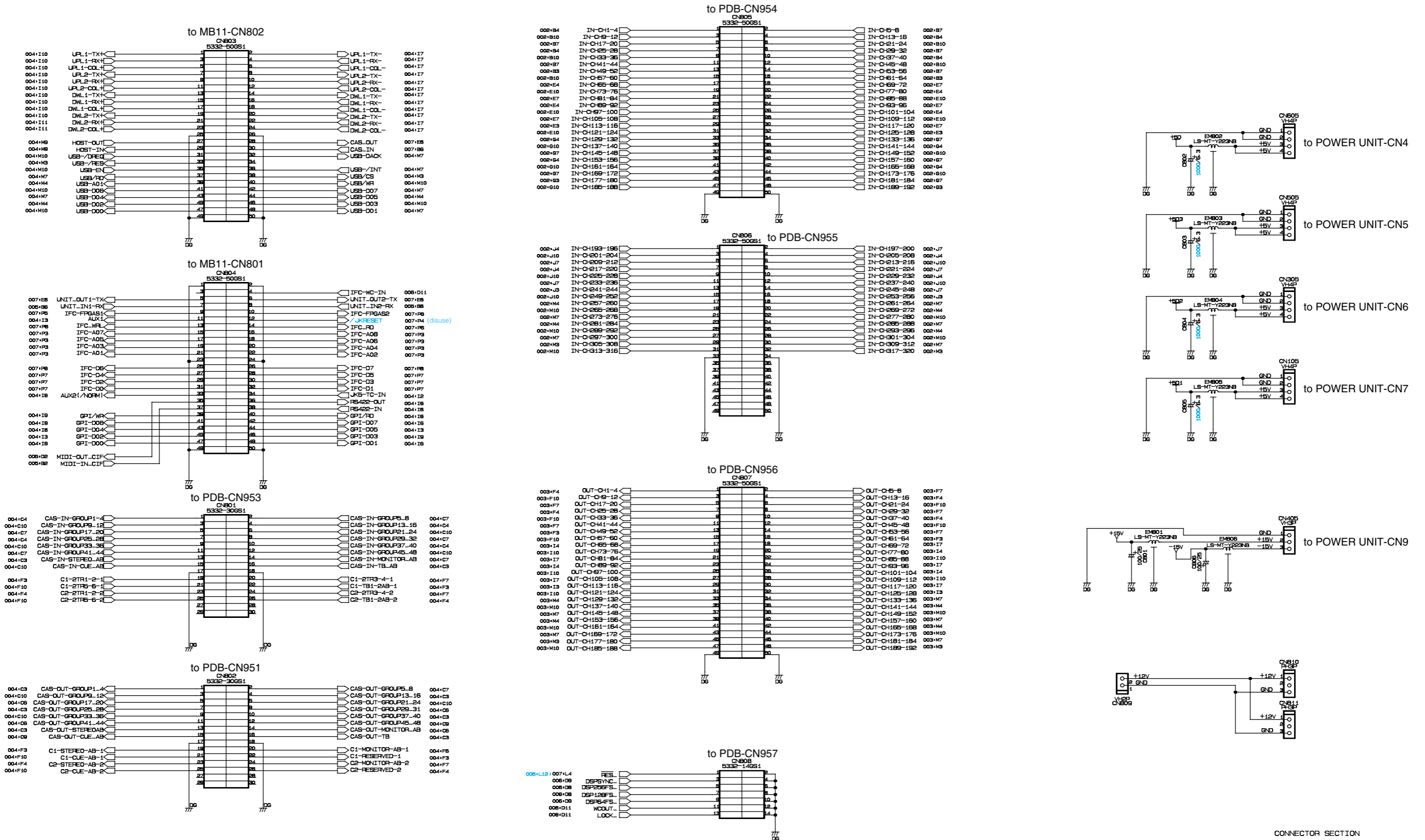
IFC1 CIRCUIT DIAGRAM 007 (DSP1D)

DSP1D



IFC1 CIRCUIT DIAGRAM 008 (DSP1D)

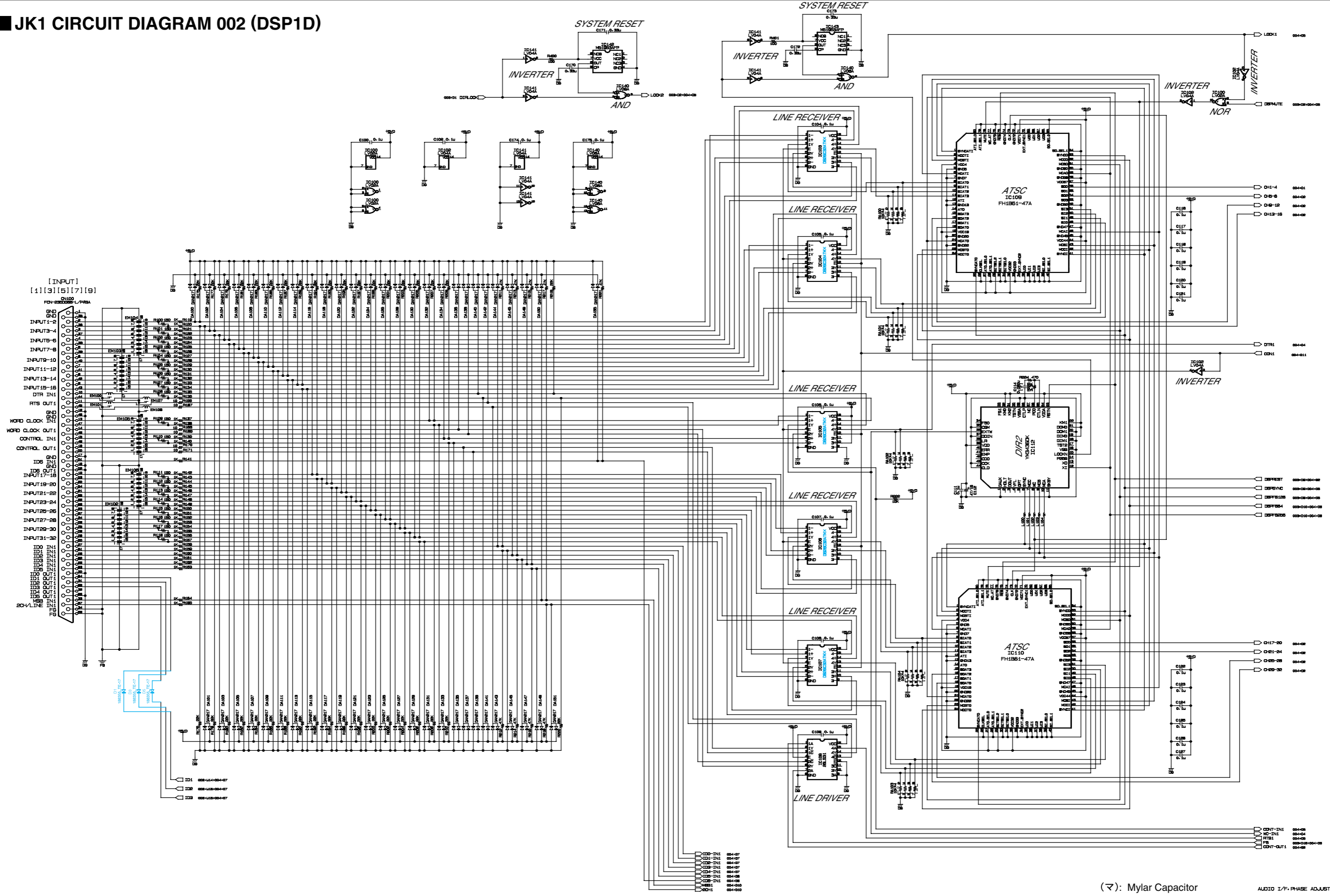
DSP1D



CONNECTOR SECTION

JK1 CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D

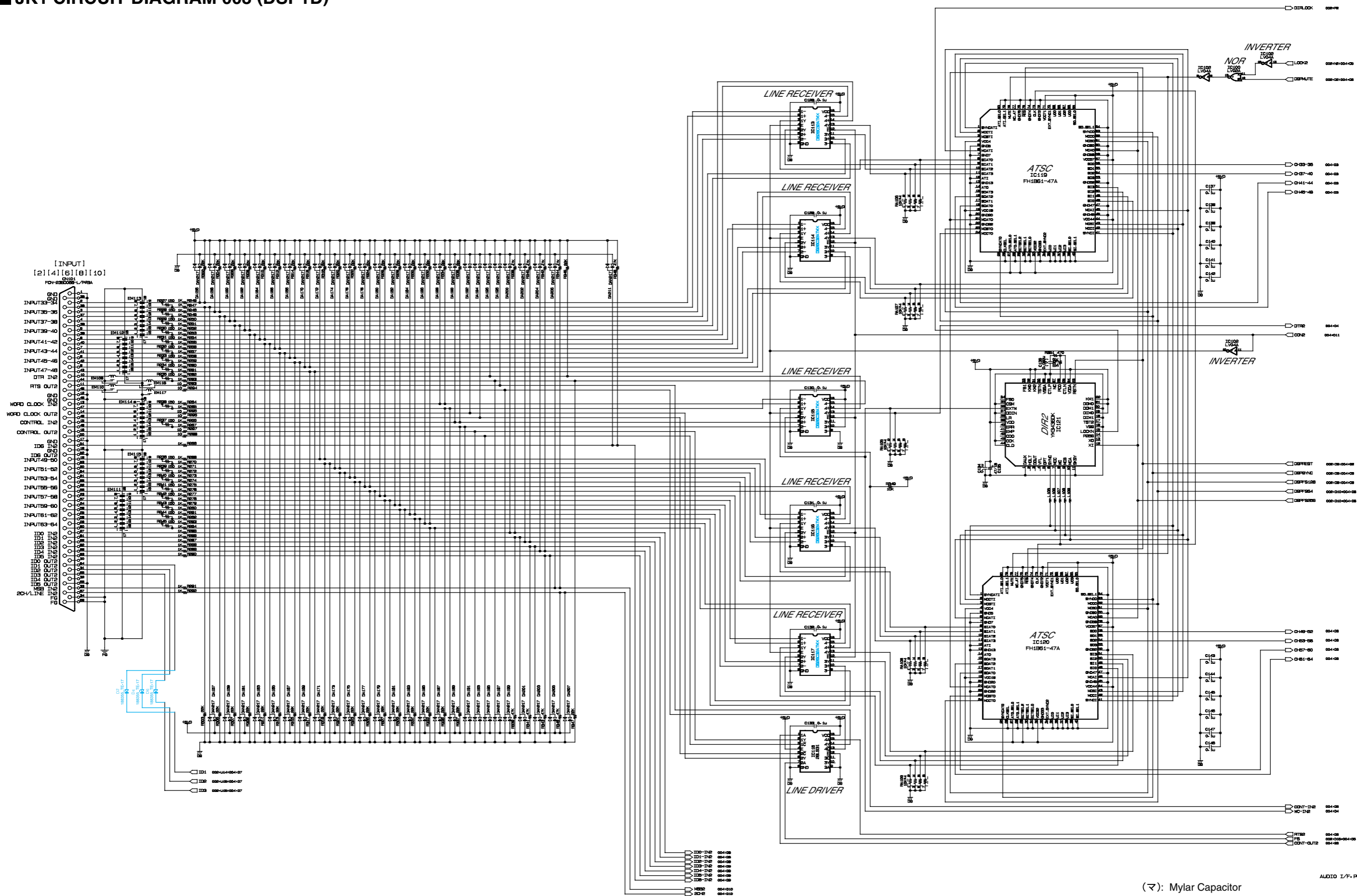


(M): Mylar Capacitor AUDIO I/F PHASE ADJUST SECTION

JK1 CIRCUIT DIAGRAM 002 (DSP1D)

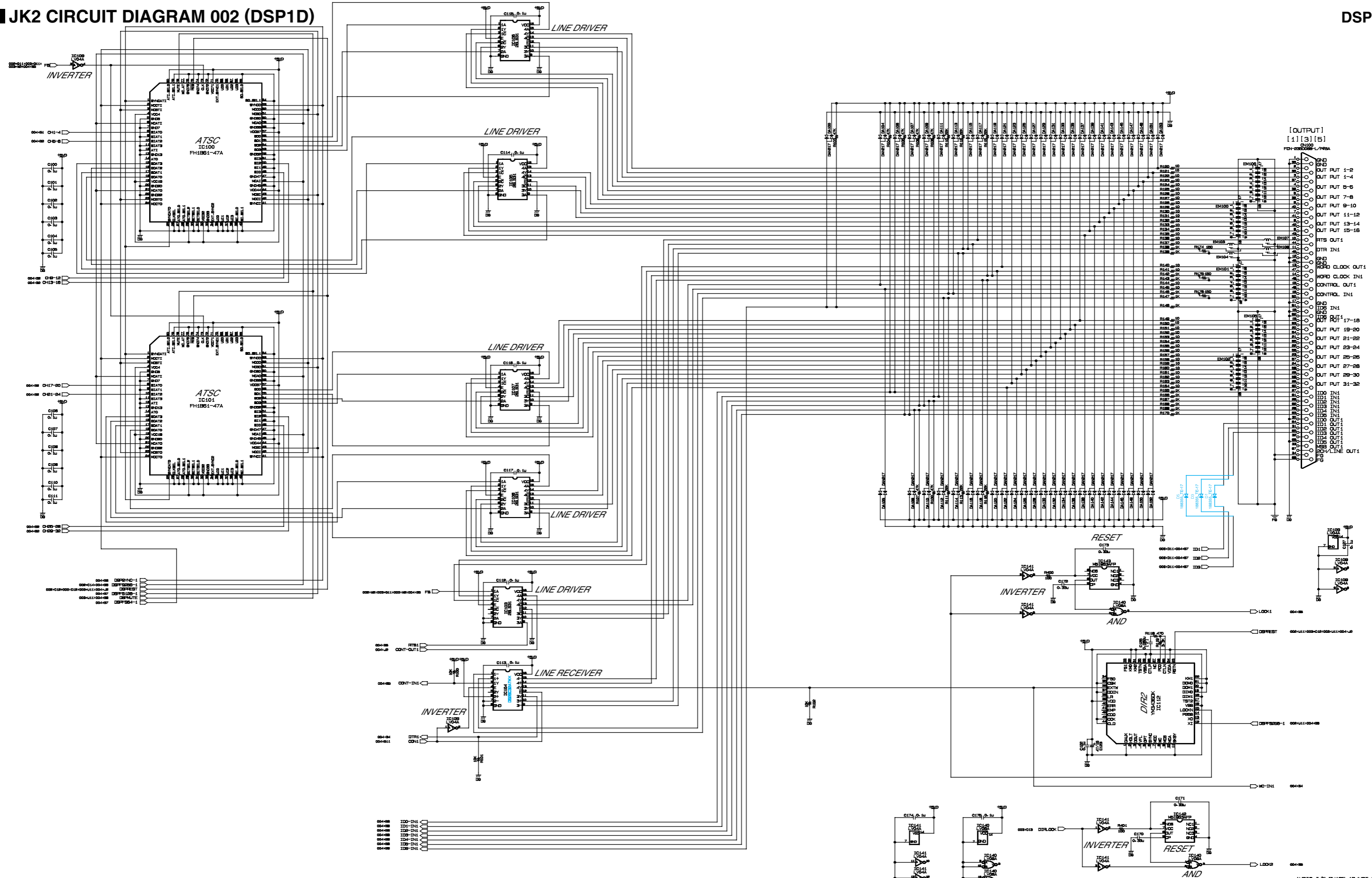
JK1 CIRCUIT DIAGRAM 003 (DSP1D)

DSP1D



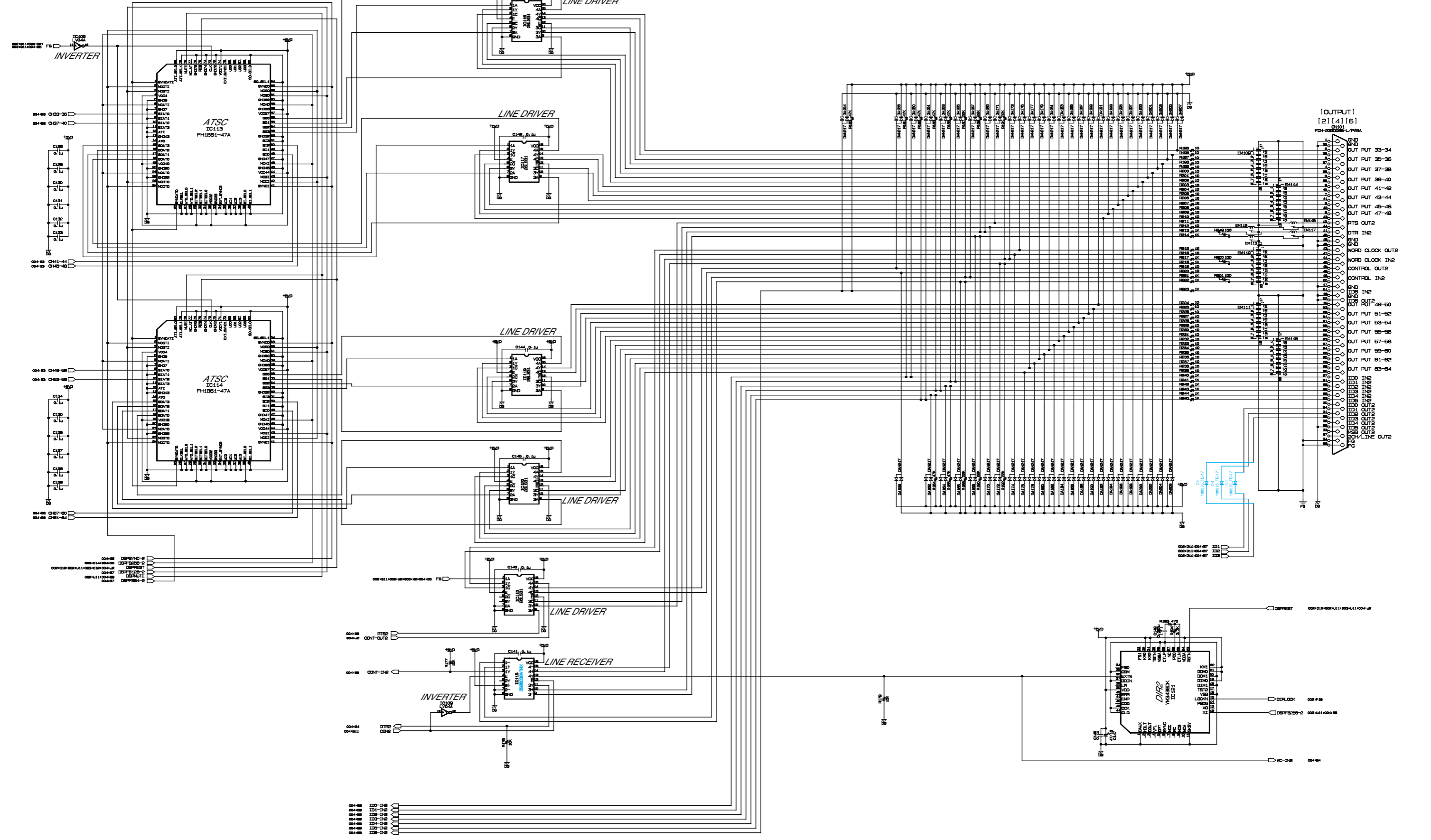
JK2 CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D



JK2 CIRCUIT DIAGRAM 003 (DSP1D)

DSP1D



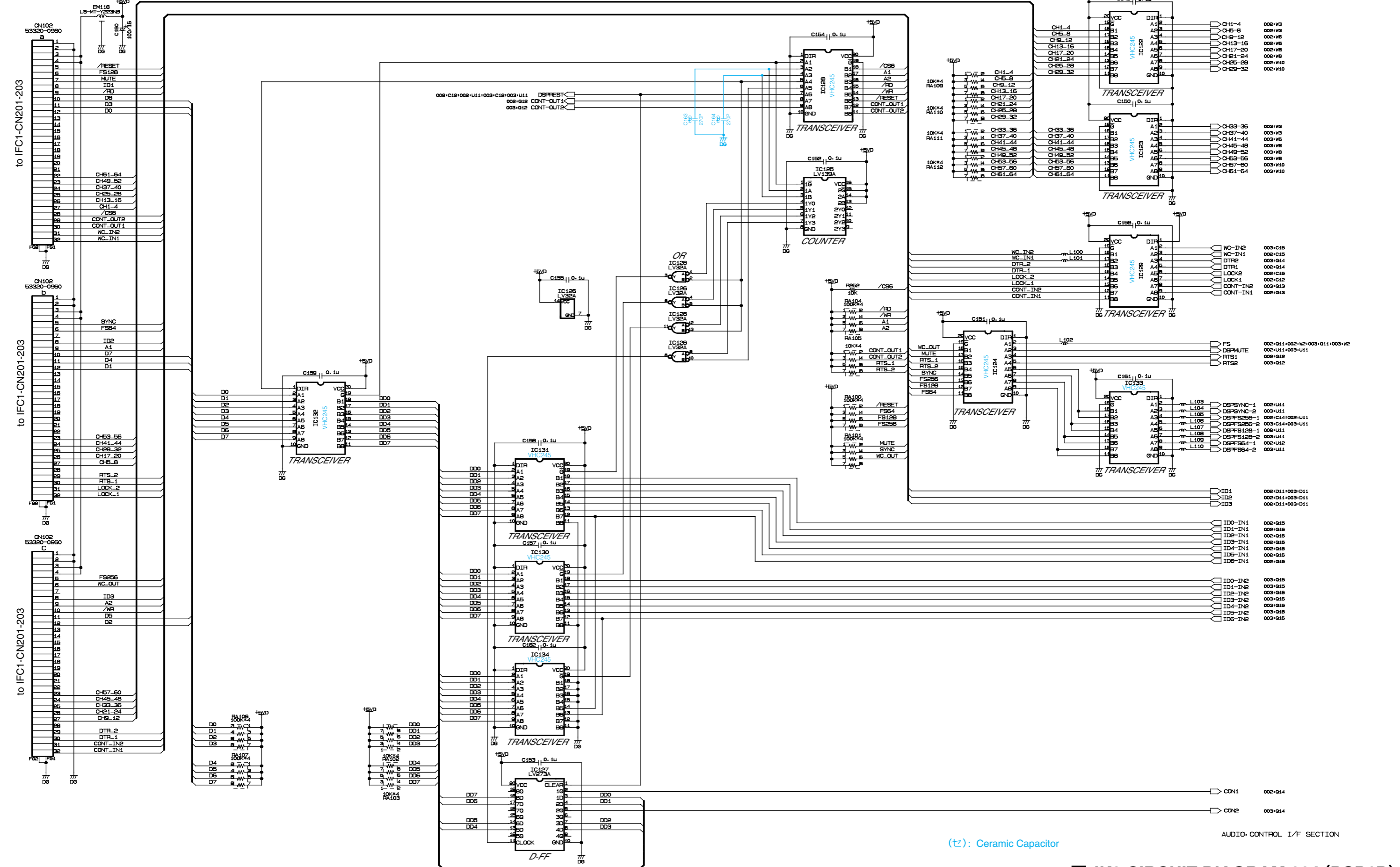
(M): Mylar Capacitor

AUDIO I/F-PHASE ADJUST SECTION

JK2 CIRCUIT DIAGRAM 003 (DSP1D)

JK2 CIRCUIT DIAGRAM 004 (DSP1D)

DSP1D

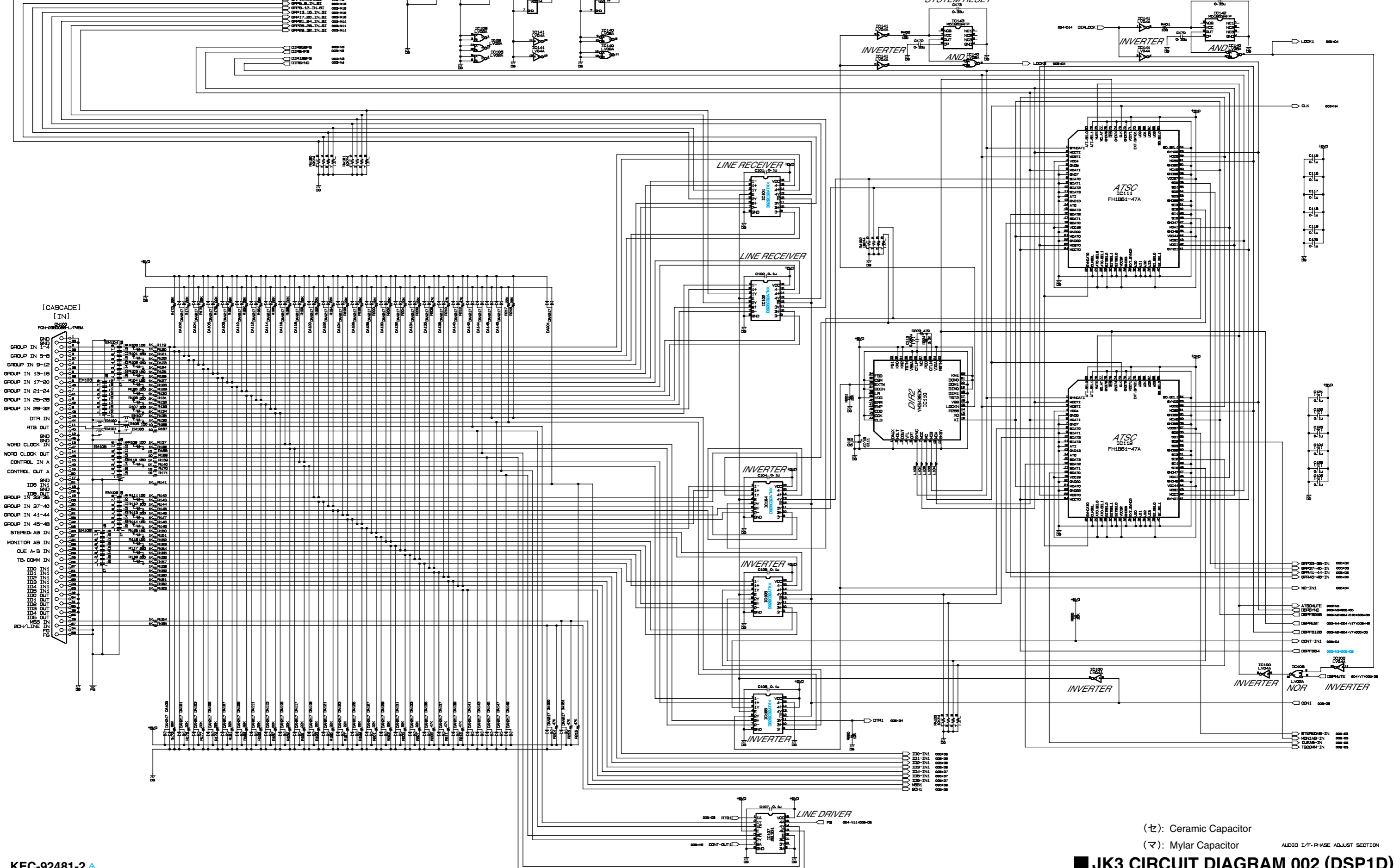


AUDIO CONTROL I/F SECTION

(τ): Ceramic Capacitor

JK3 CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D



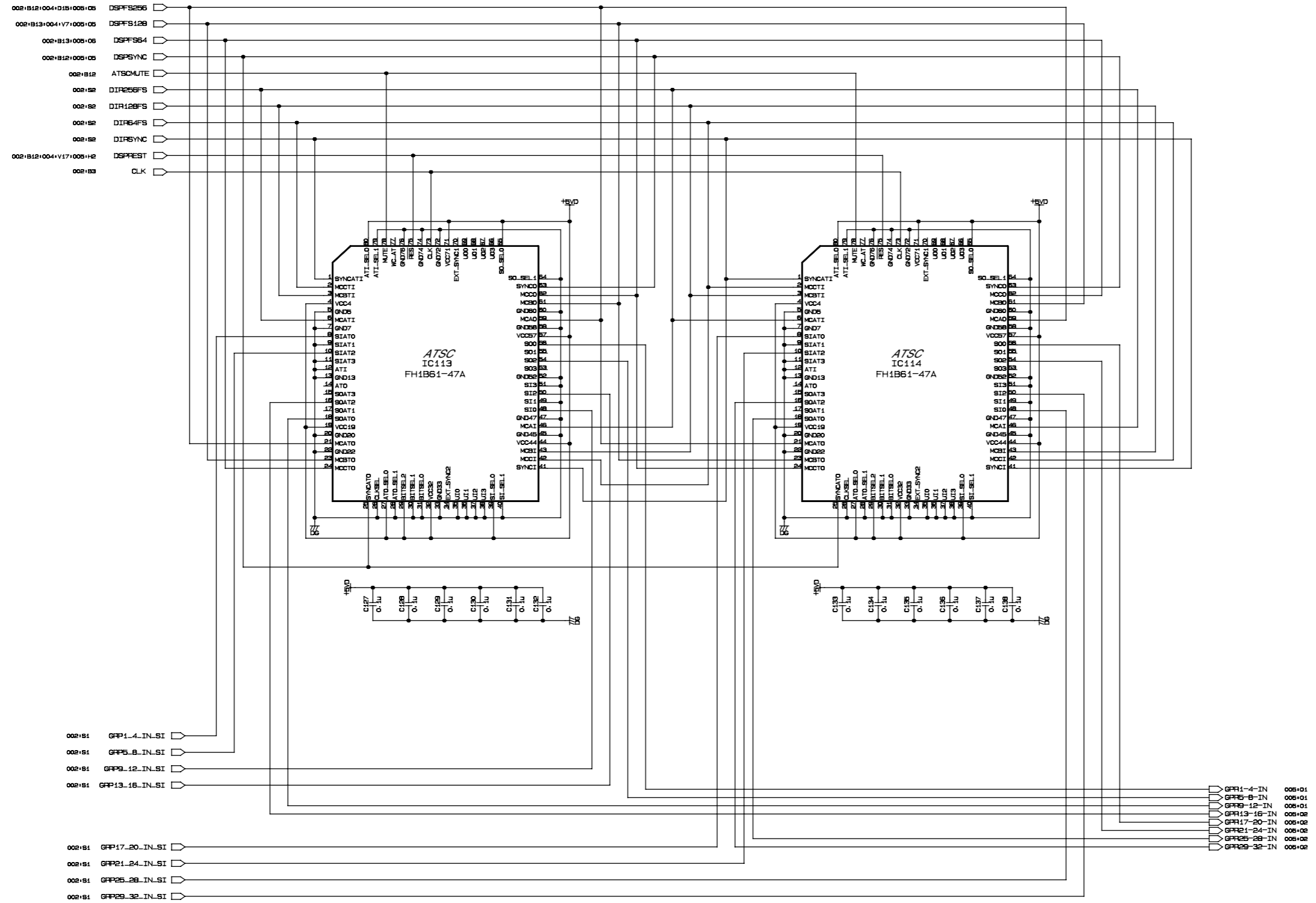
(㊦): Ceramic Capacitor
(マ): Mylar Capacitor

AUDIO I/F-PHASE ADJUST SECTION

JK3 CIRCUIT DIAGRAM 002 (DSP1D)

JK3 CIRCUIT DIAGRAM 003 (DSP1D)

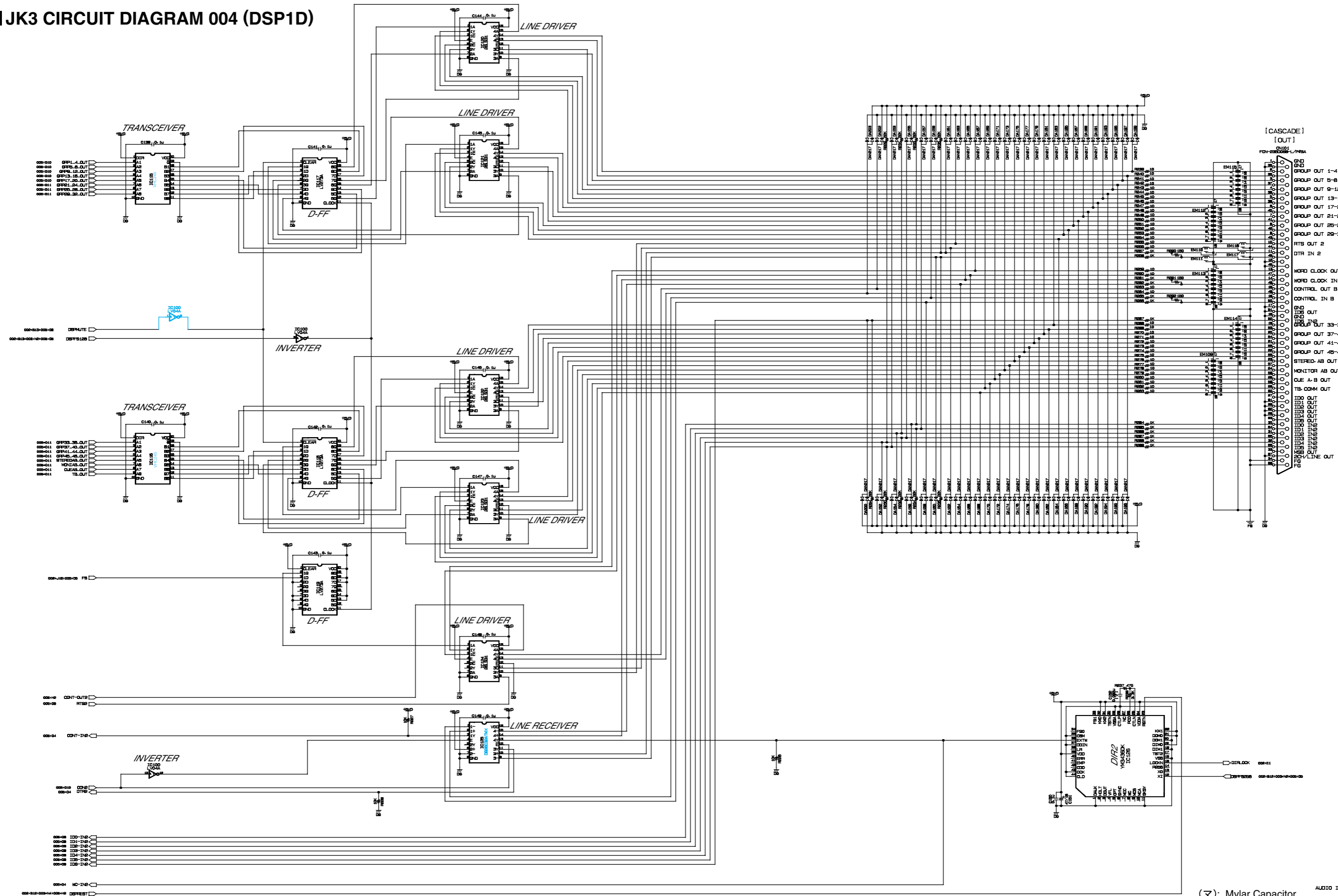
DSP1D



AUDIO I/F. PHASE ADJUST SECTION

JK3 CIRCUIT DIAGRAM 004 (DSP1D)

DSP1D

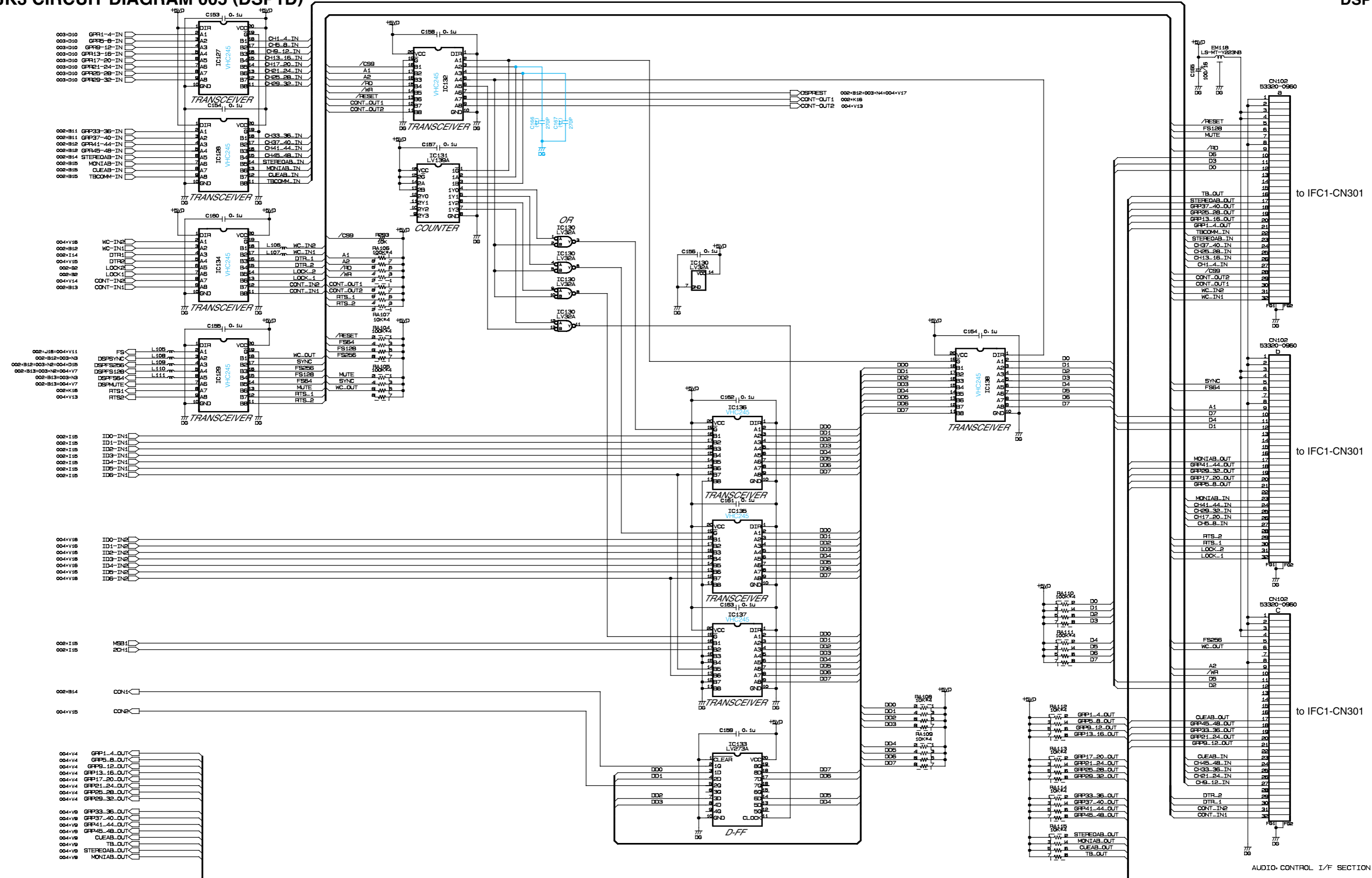


(マ): Mylar Capacitor AUDIO I/F SECTION

JK3 CIRCUIT DIAGRAM 004 (DSP1D)

JK3 CIRCUIT DIAGRAM 005 (DSP1D)

DSP1D

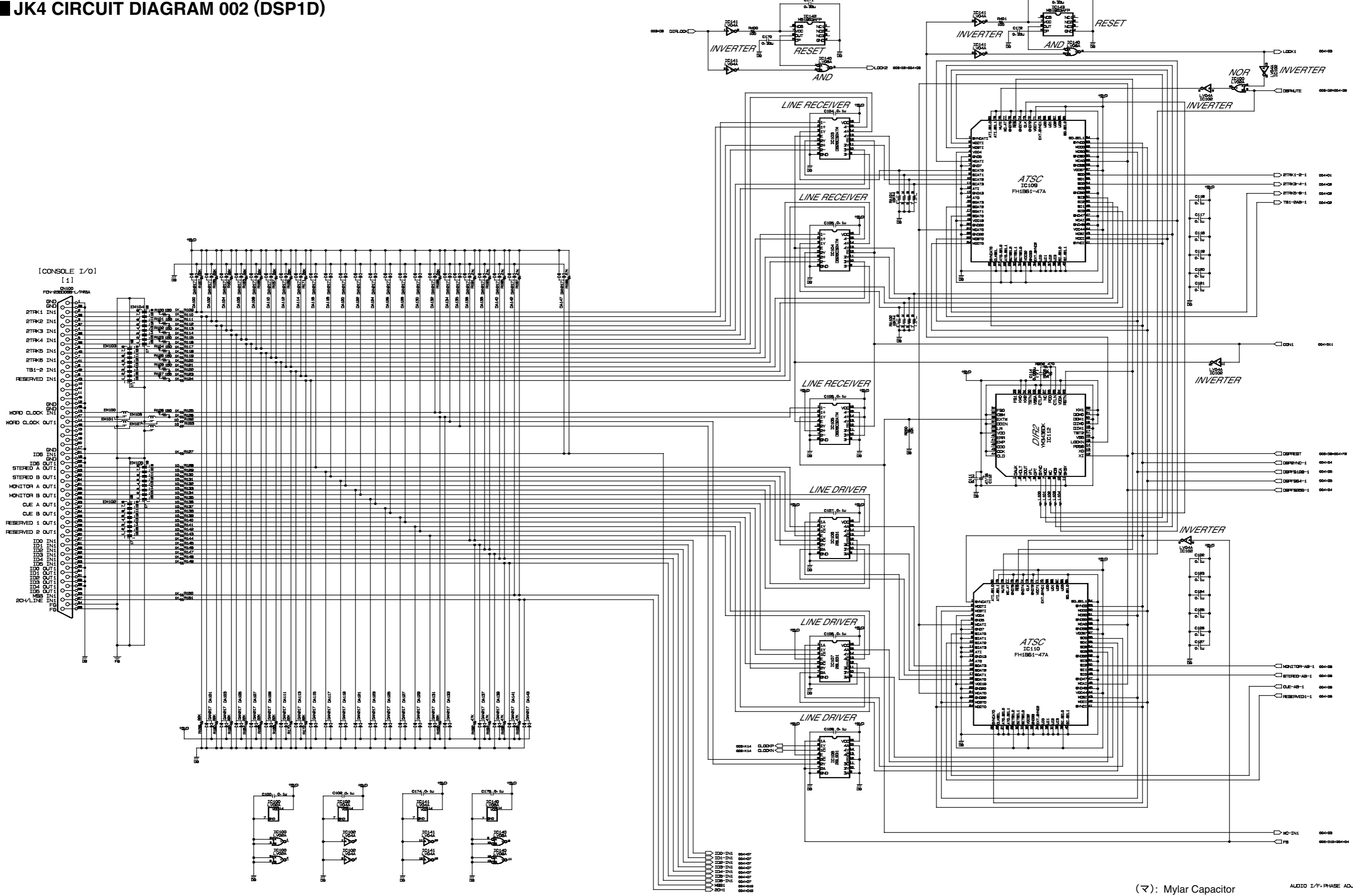


AUDIO-CONTROL I/F SECTION

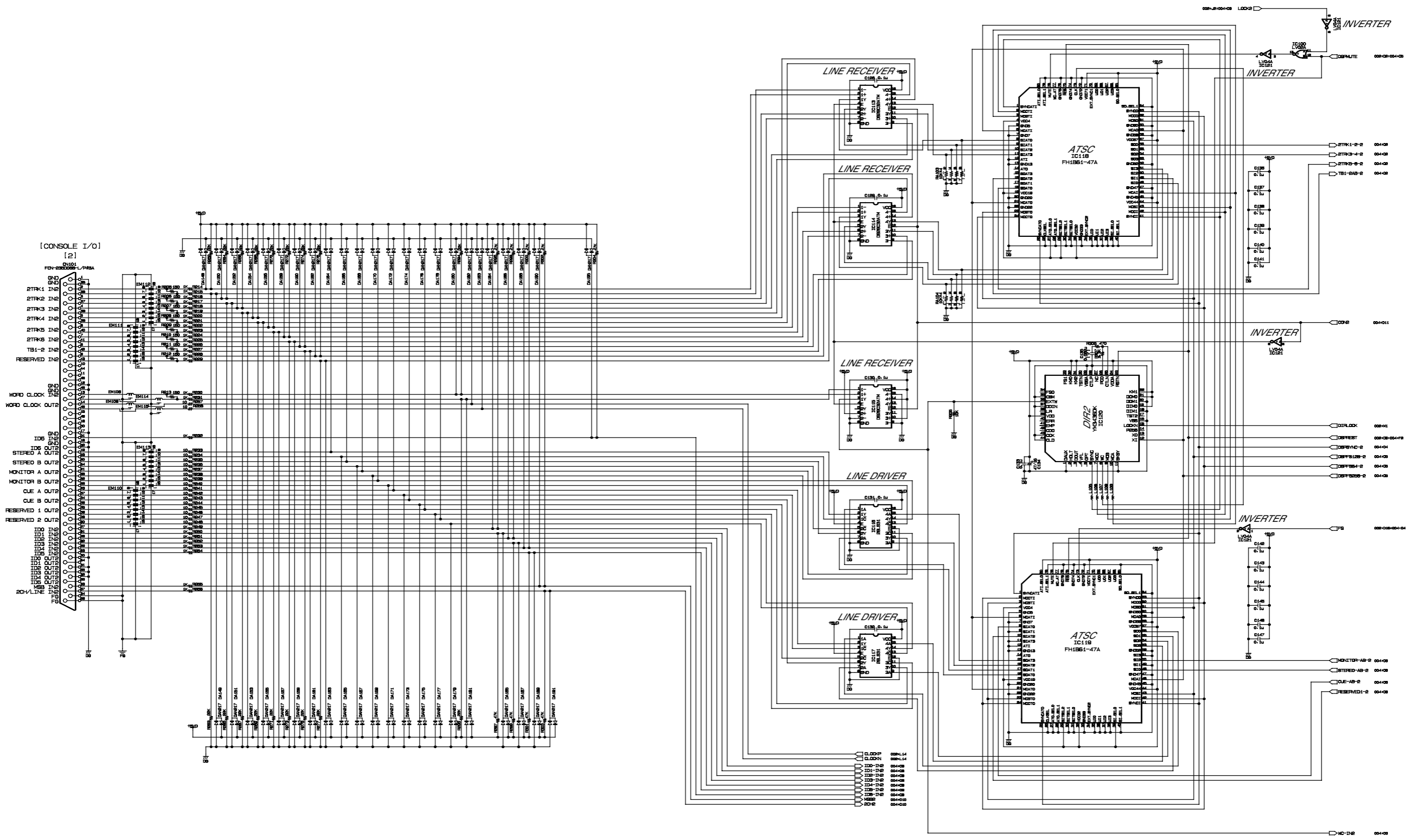
JK4 CIRCUIT DIAGRAM 002 (DSP1D)

DSP1D

[CONSOLE I/O]
[1]
FDN-2300000-778BA



(M): Mylar Capacitor AUDIO 1/F-PHASE ADJUST SECTION

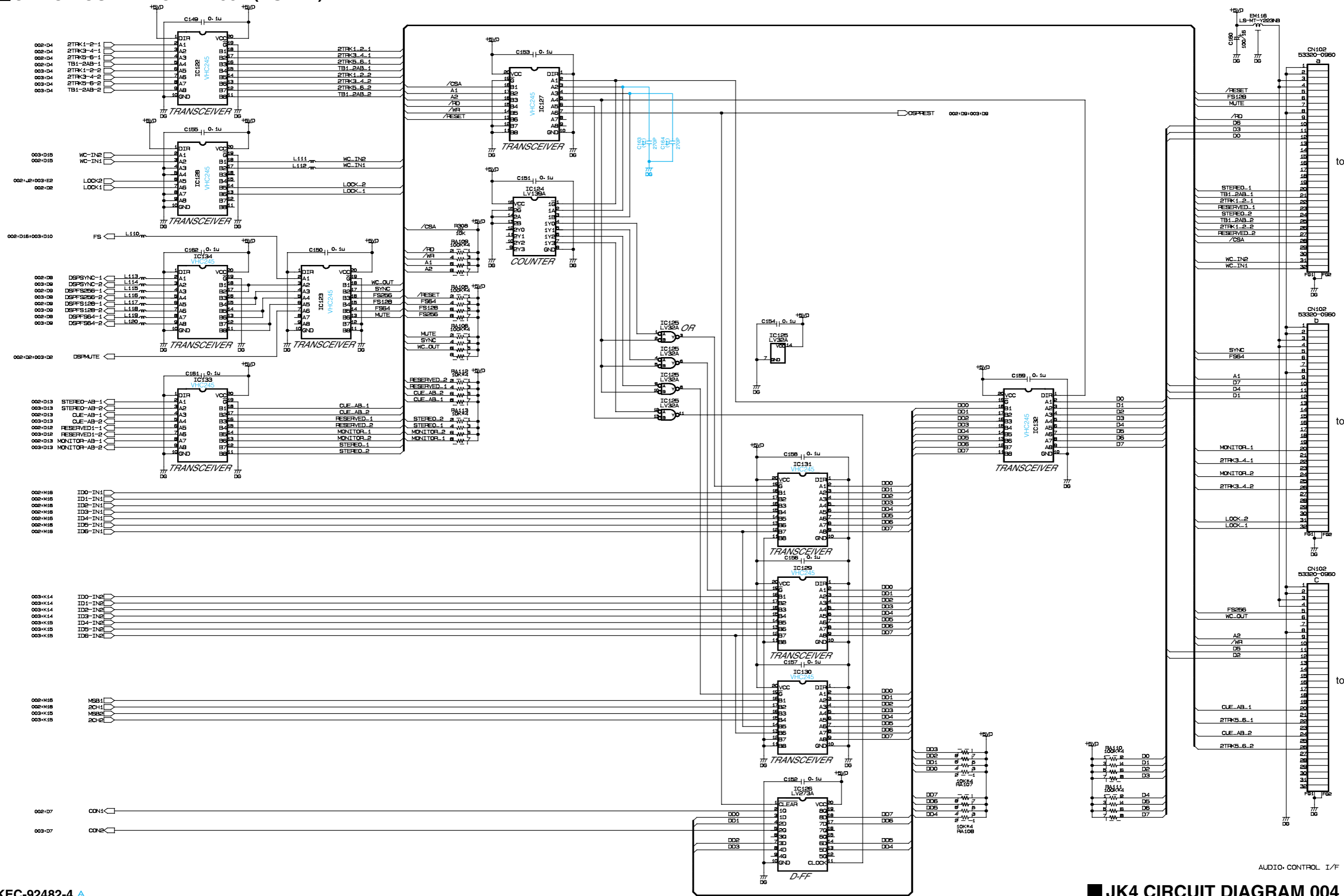


(M): Mylar Capacitor

AUDIO 1/F-PHASE ADJUST SECTION

JK4 CIRCUIT DIAGRAM 004 (DSP1D)

DSP1D



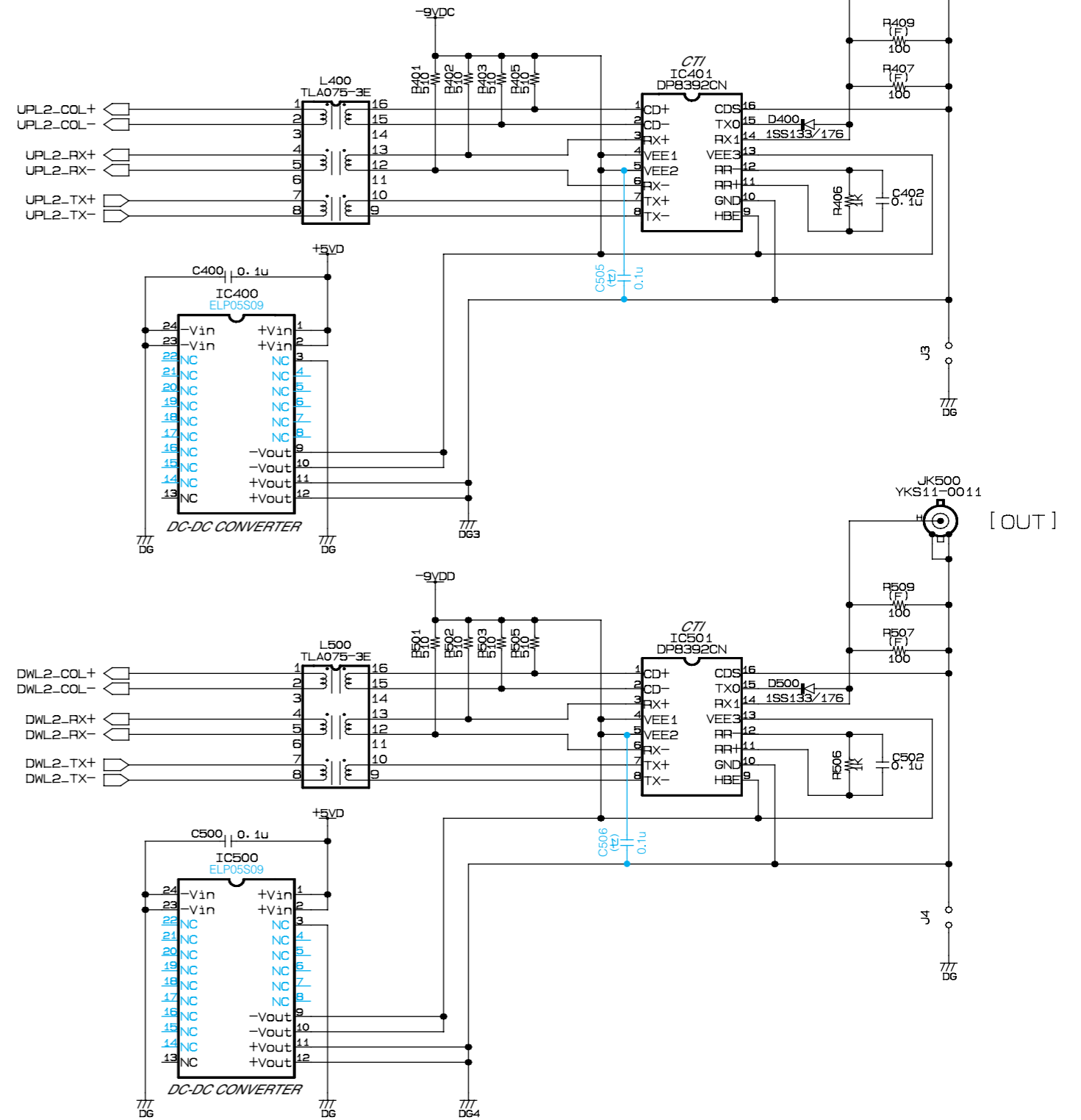
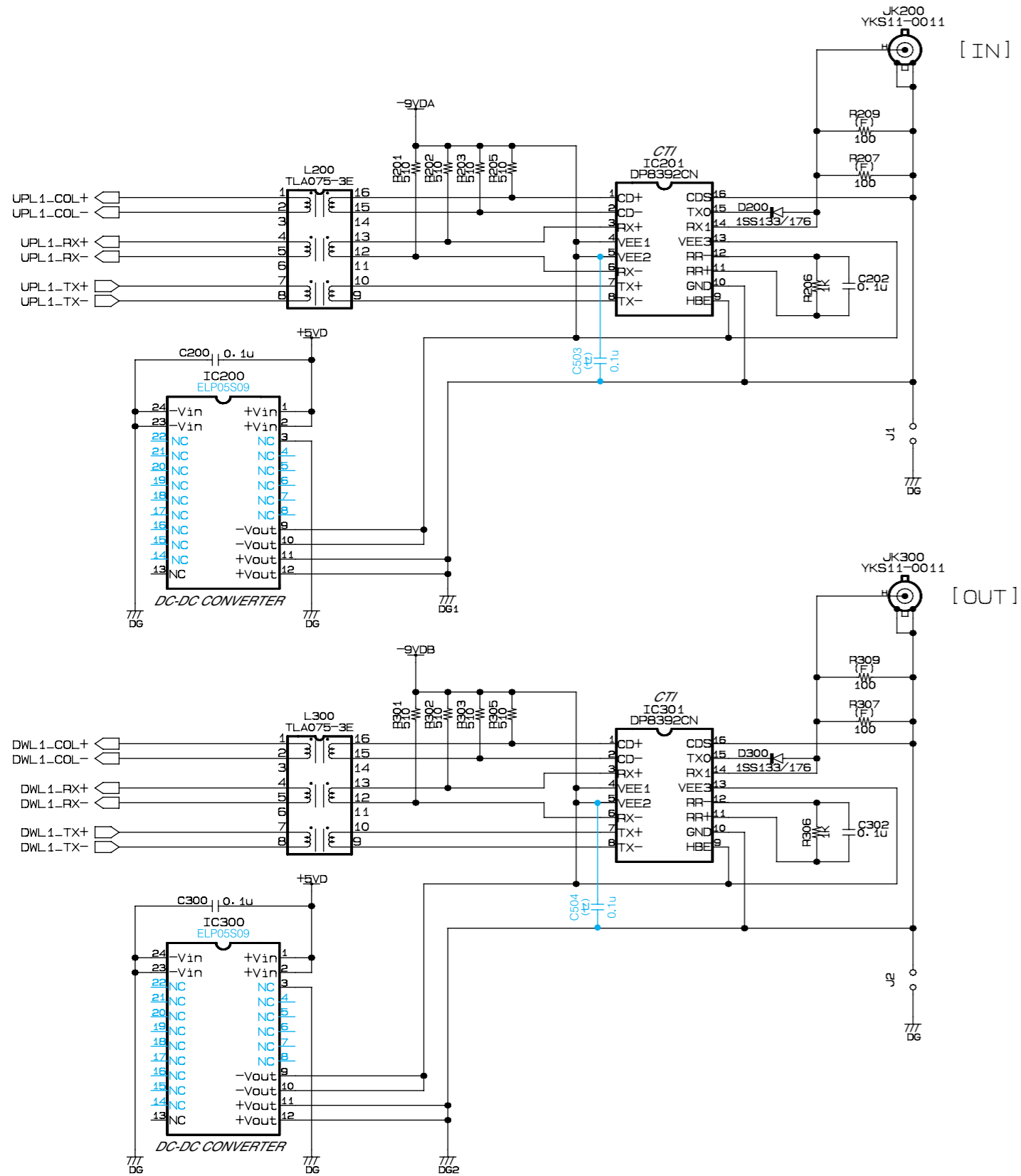
AUDIO CONTROL I/F SECTION

JK4 CIRCUIT DIAGRAM 004 (DSP1D)

JK5 CIRCUIT DIAGRAM 2/2 (DSP1D)

[CONTROL I/O]
[CONSOLE]
[1]
[IN]

[CONTROL I/O]
[CONSOLE]
[2]
[IN]



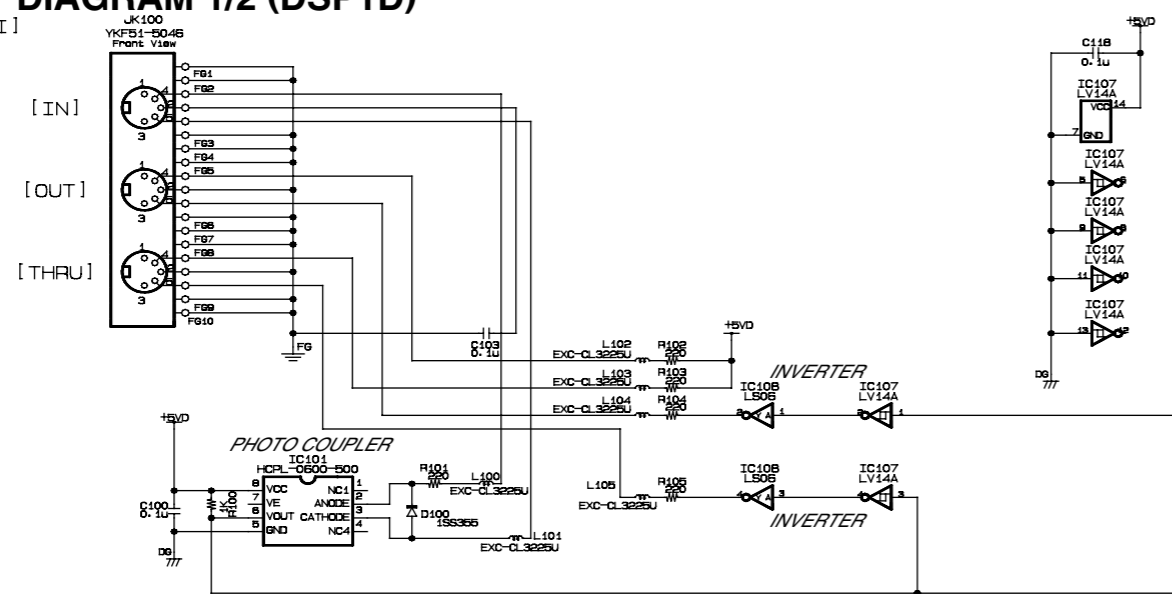
(F): Metal Film Resistor

Ethernet I/F SECTION

JK6 CIRCUIT DIAGRAM 1/2 (DSP1D)

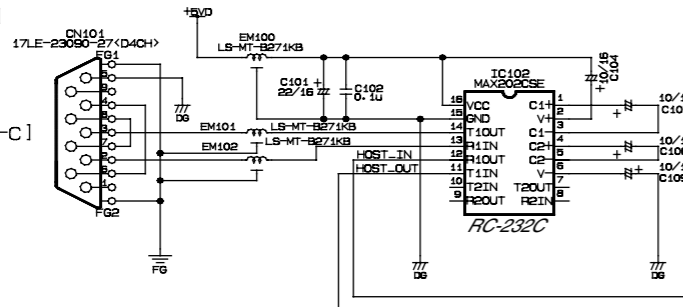
DSP1D

[MIDI]

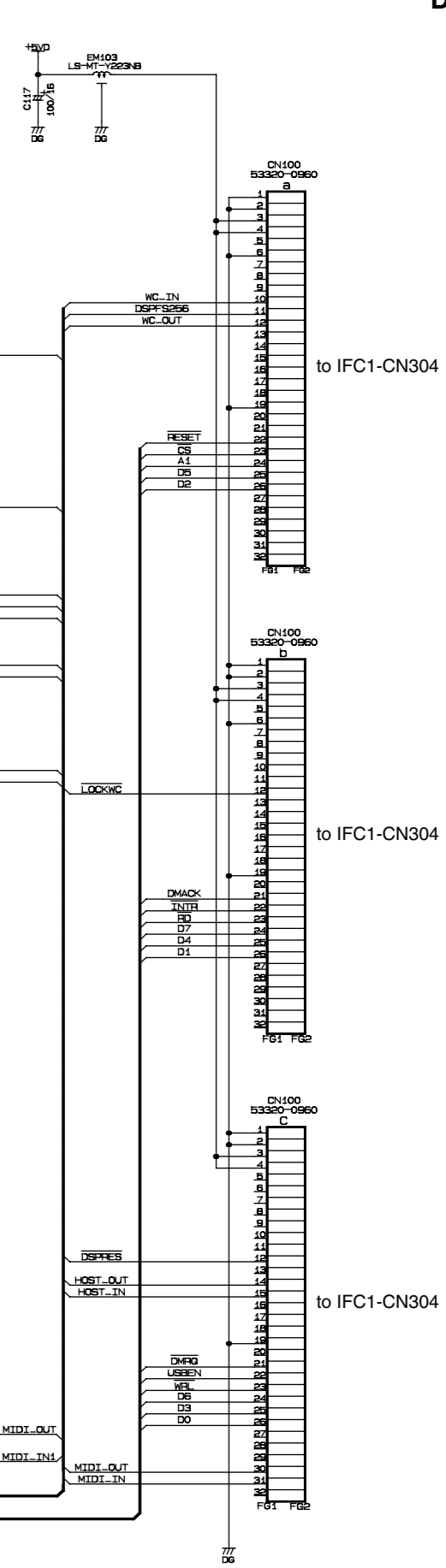
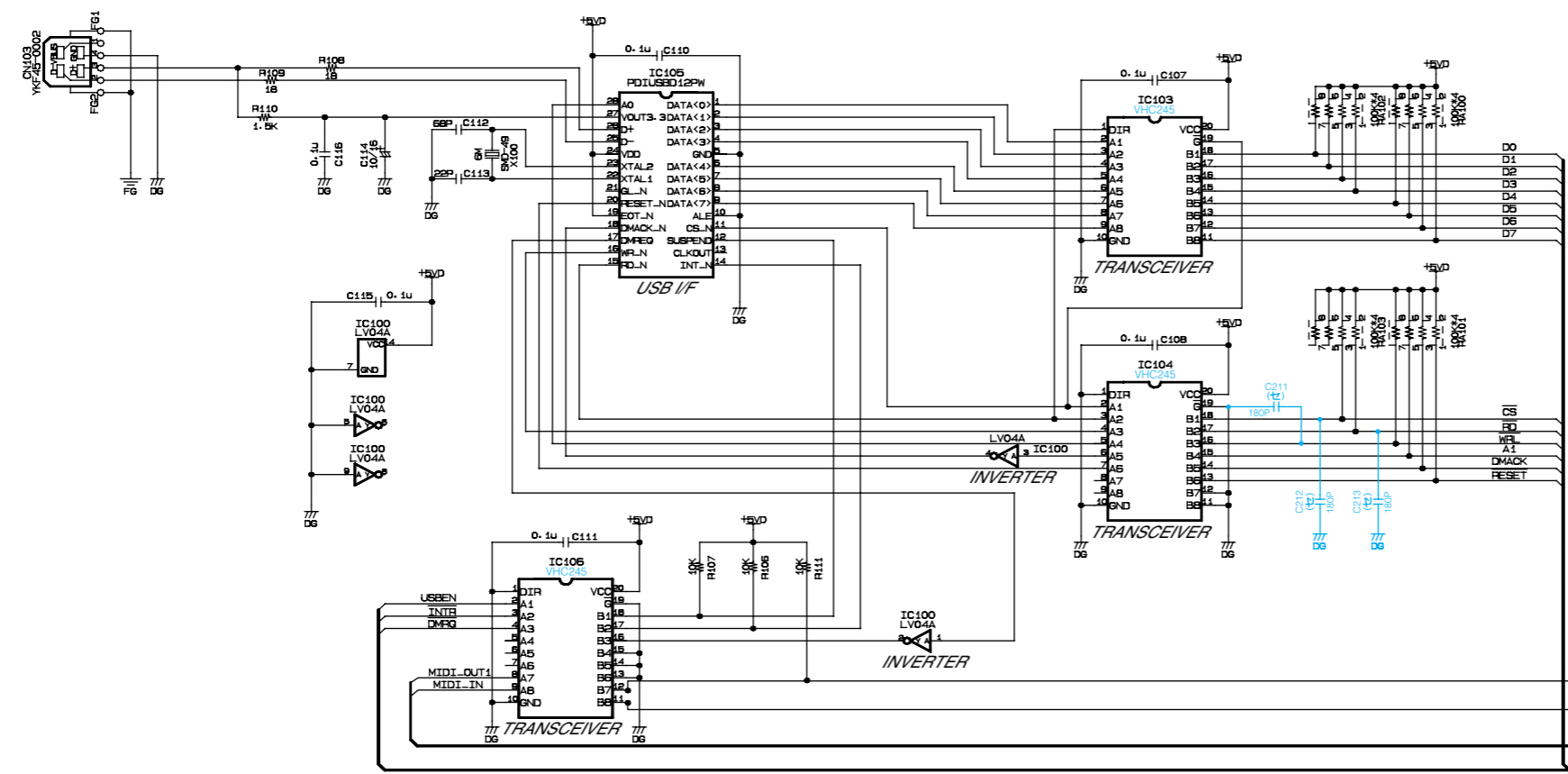


[PC CONTROL]

[RS-232-C]



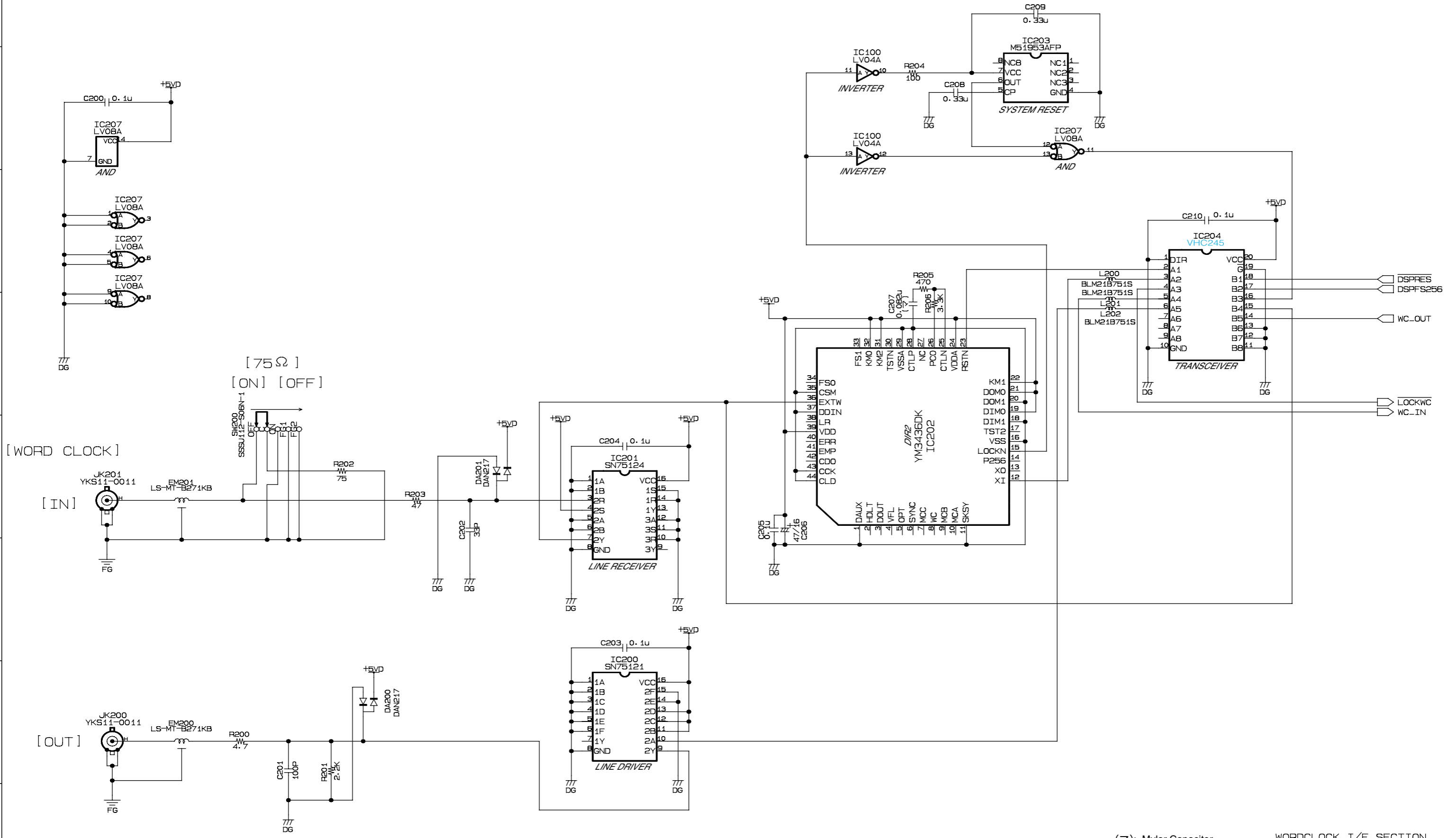
[USB]



MIDI, RS-232C, USB I/F SECTION

JK6 CIRCUIT DIAGRAM 2/2 (DSP1D)

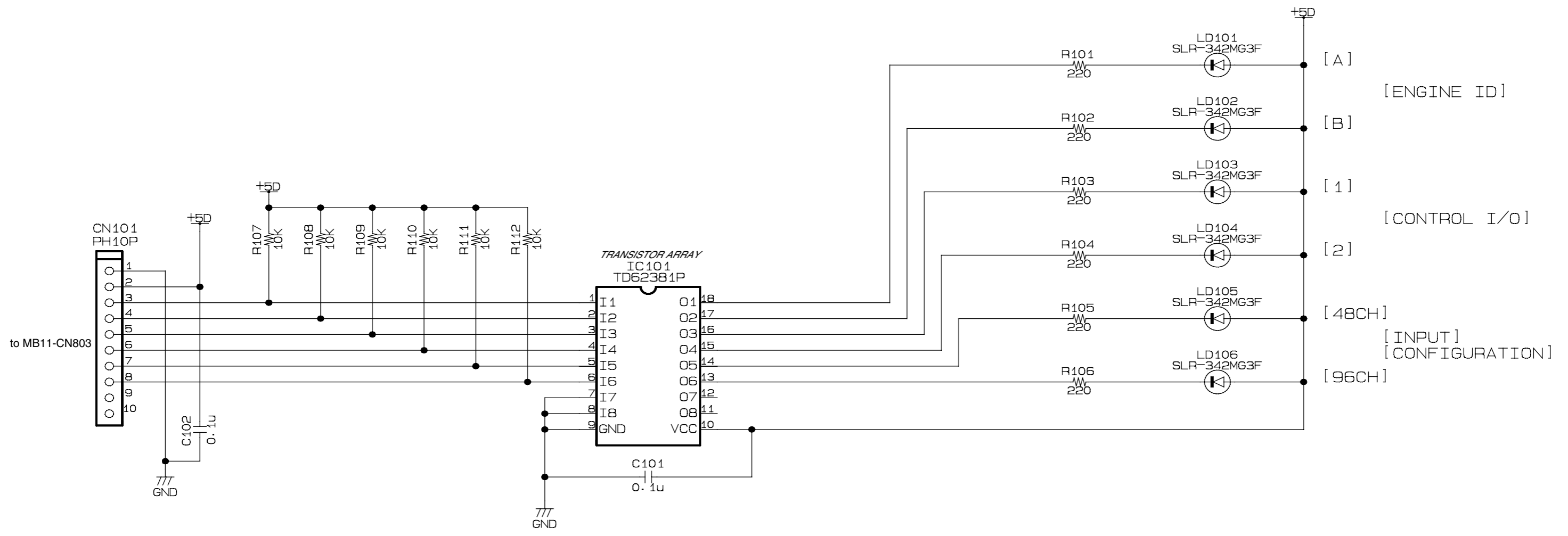
DSP1D



(M): Mylar Capacitor WORDCLOCK I/F SECTION

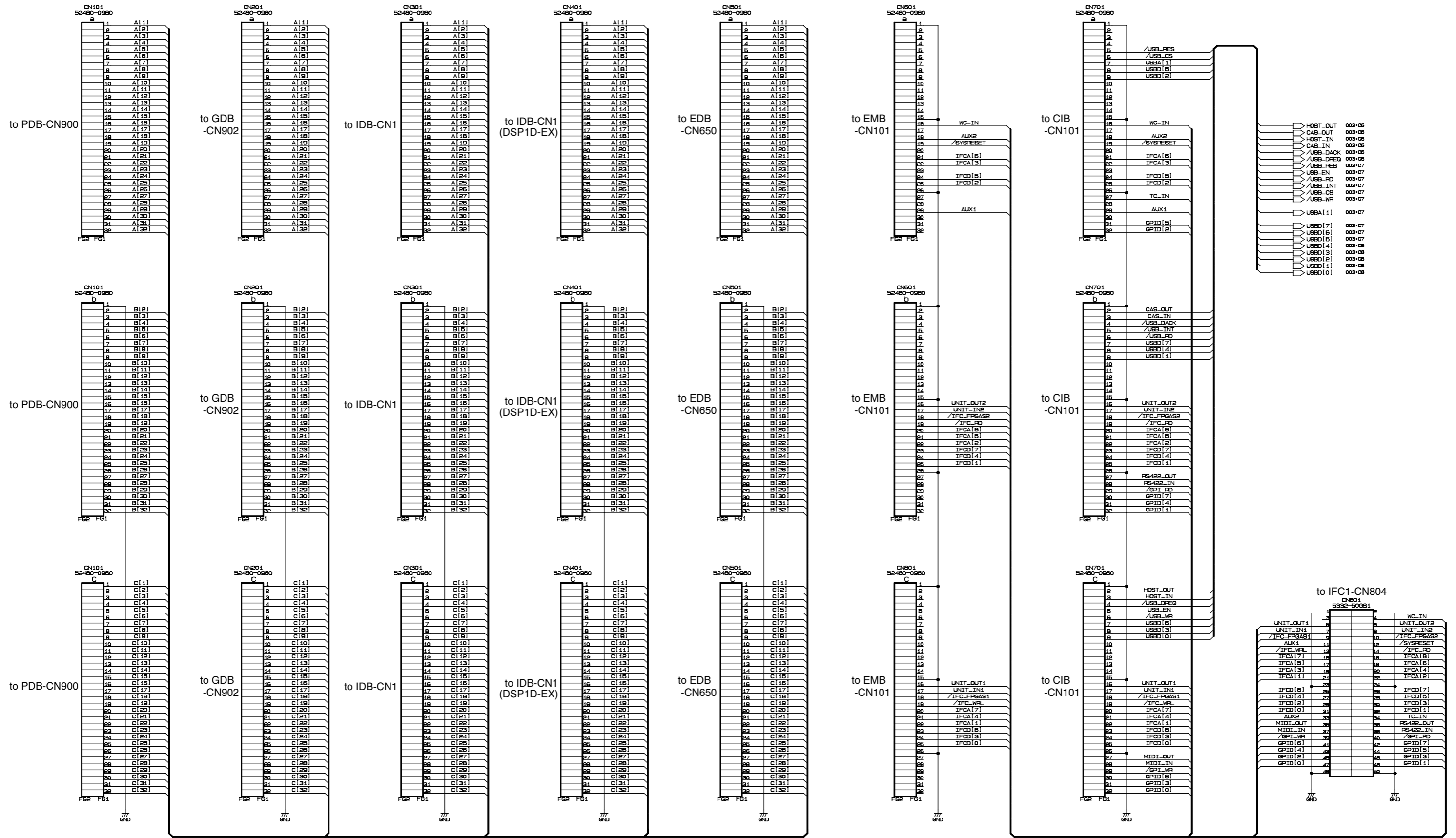
LED2 CIRCUIT DIAGRAM (DSP1D)

DSP1D



MB11 CIRCUIT DIAGRAM 002 (DSP1D)

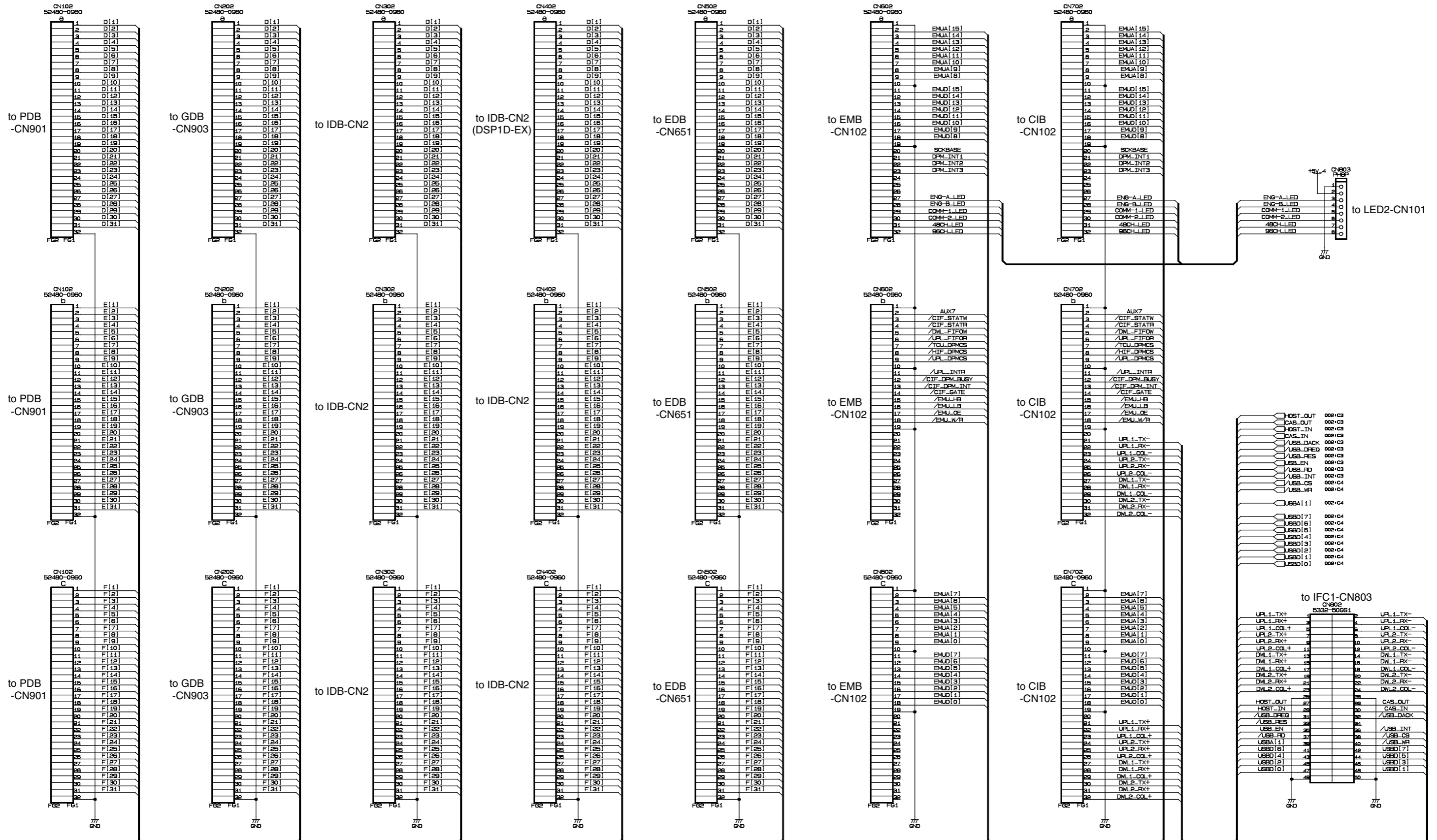
DSP1D



CONNECTOR 1 SECTION

MB11 CIRCUIT DIAGRAM 003 (DSP1D)

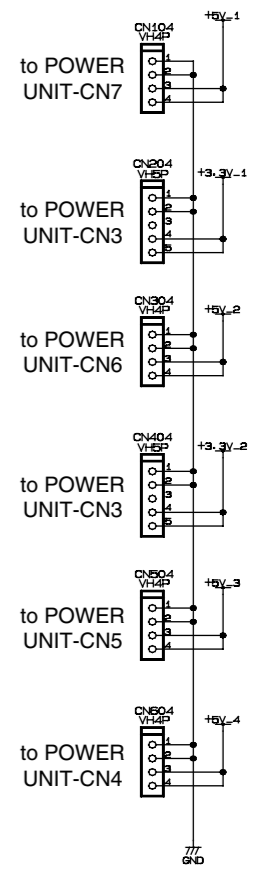
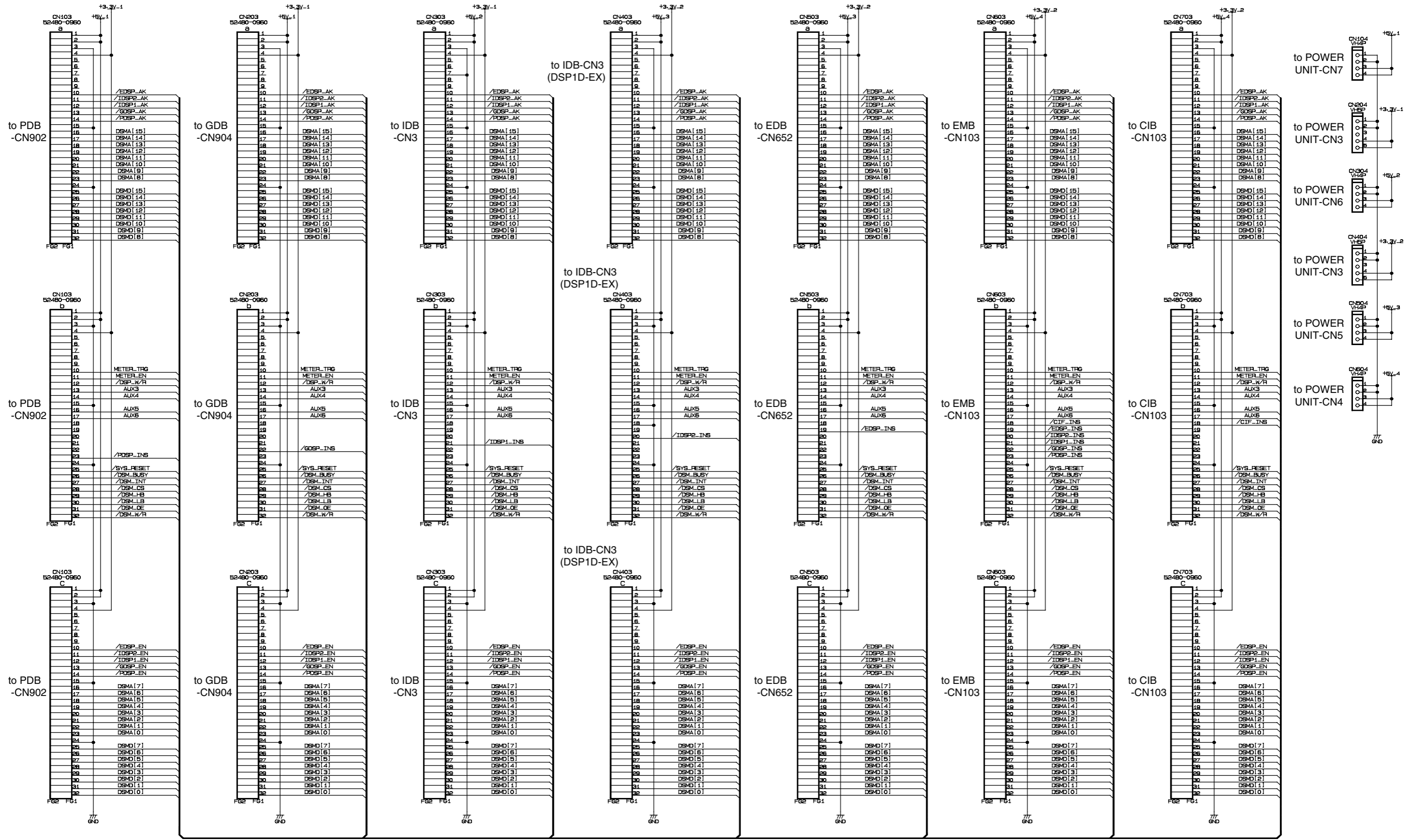
DSP1D



CONNECTOR 2 SECTION

MB11 CIRCUIT DIAGRAM 004 (DSP1D)

DSP1D



CONNECTOR 3 SECTION

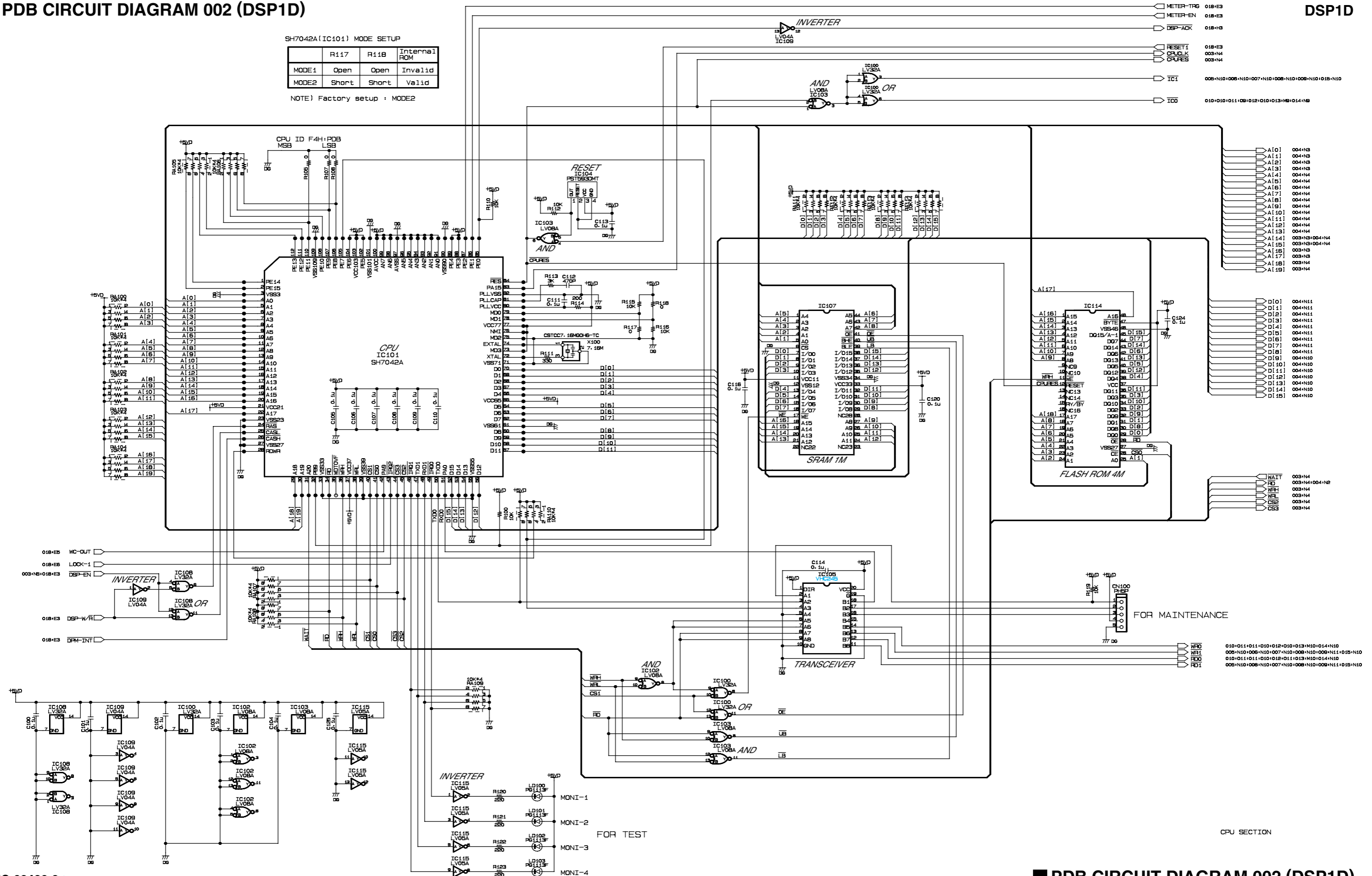
PDB CIRCUIT DIAGRAM 002 (DSP1D)

SH7042A(IC101) MODE SETUP

	R117	R118	Internal ROM
MODE1	Open	Open	Invalid
MODE2	Short	Short	Valid

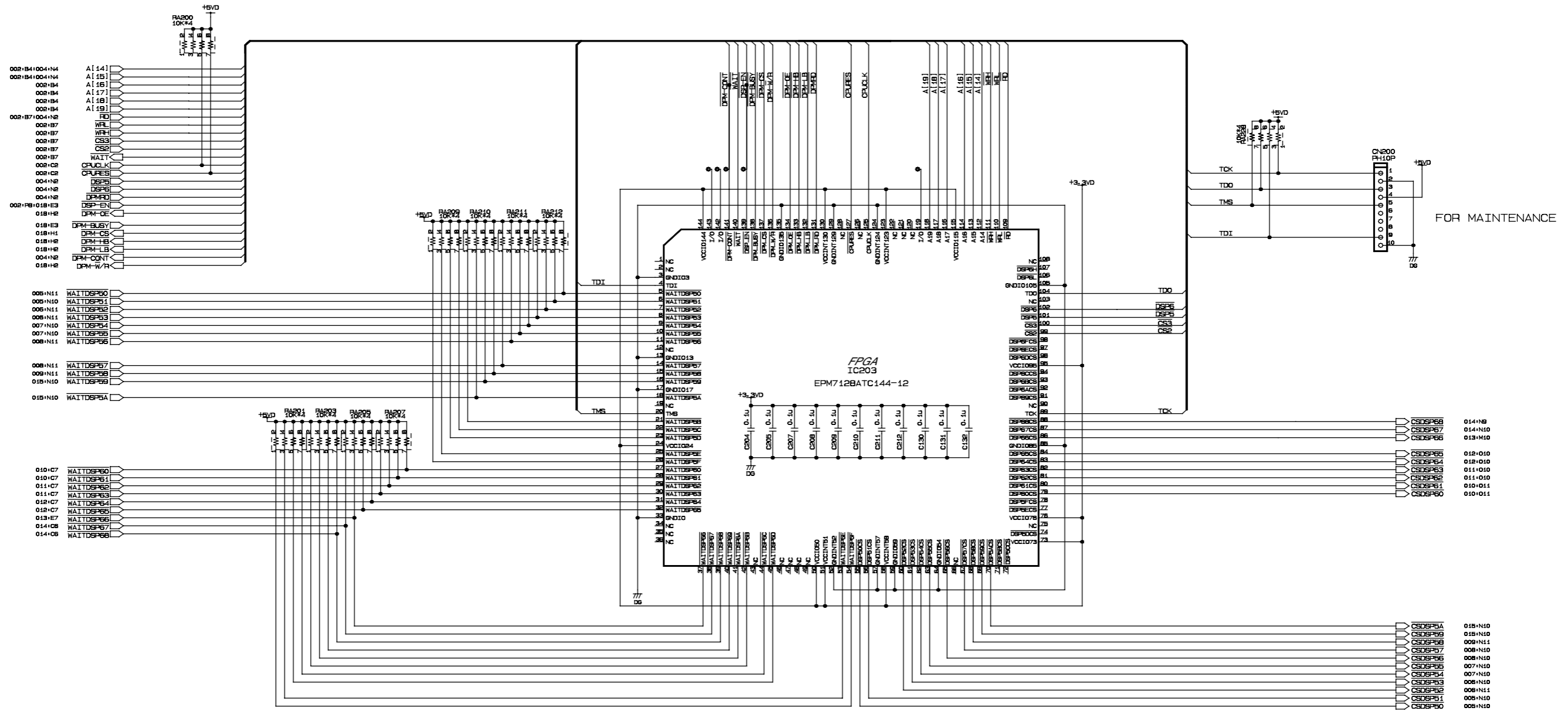
NOTE) Factory setup : MODE2

DSP1D



CPU SECTION

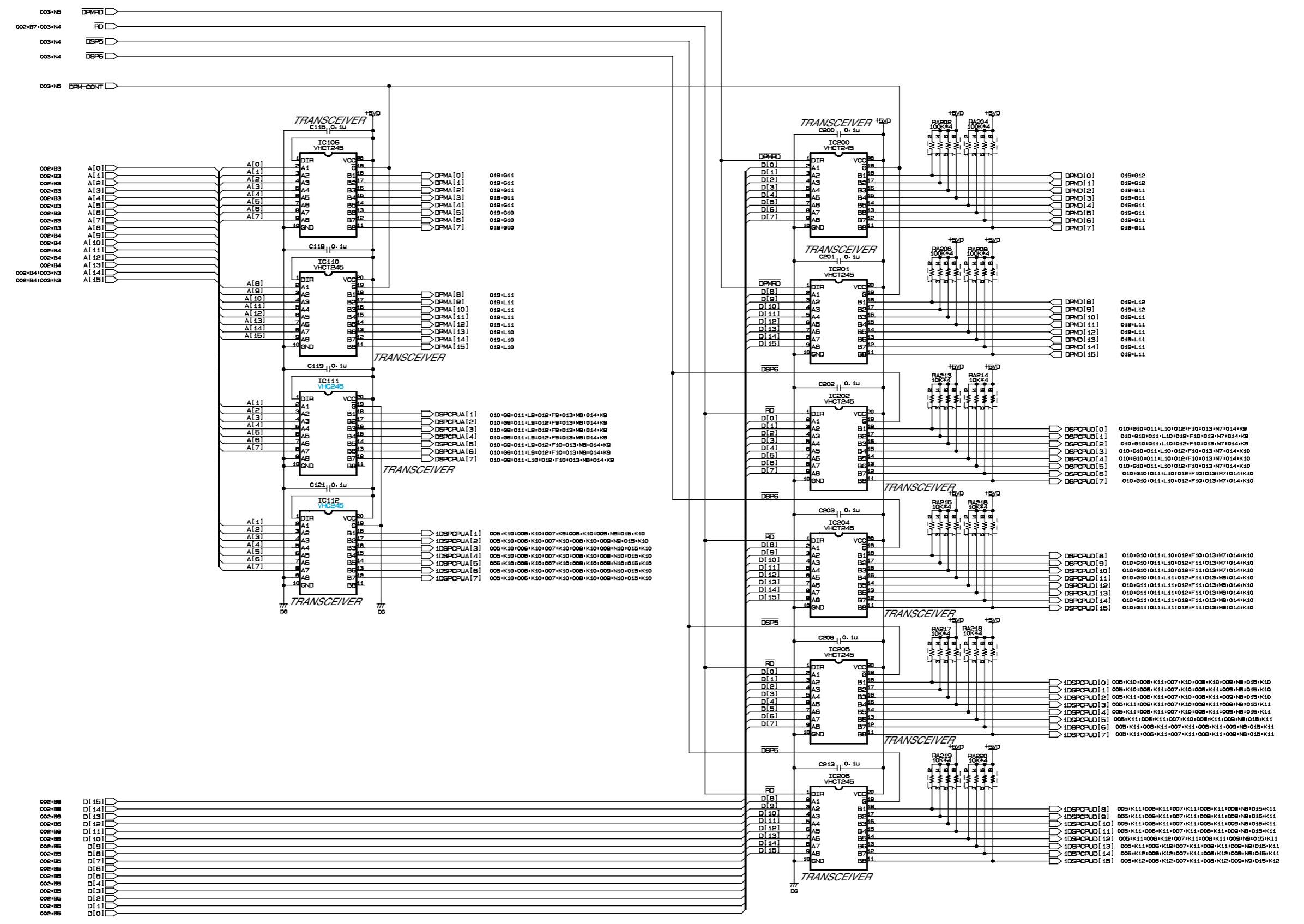
PDB CIRCUIT DIAGRAM 002 (DSP1D)



ADDRESS DECODE & WAIT CONTROL SECTION

PDB CIRCUIT DIAGRAM 004 (DSP1D)

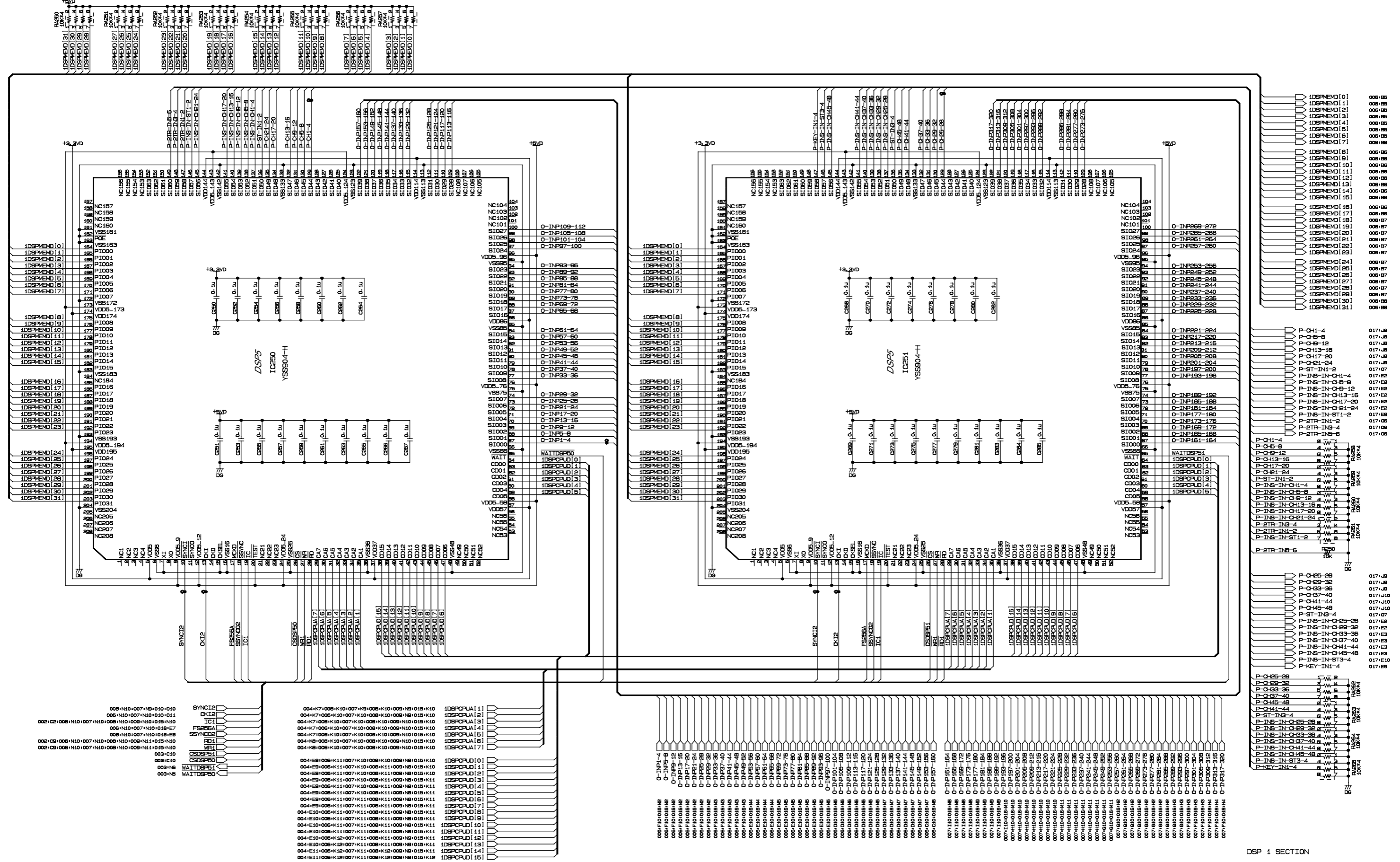
DSP1D



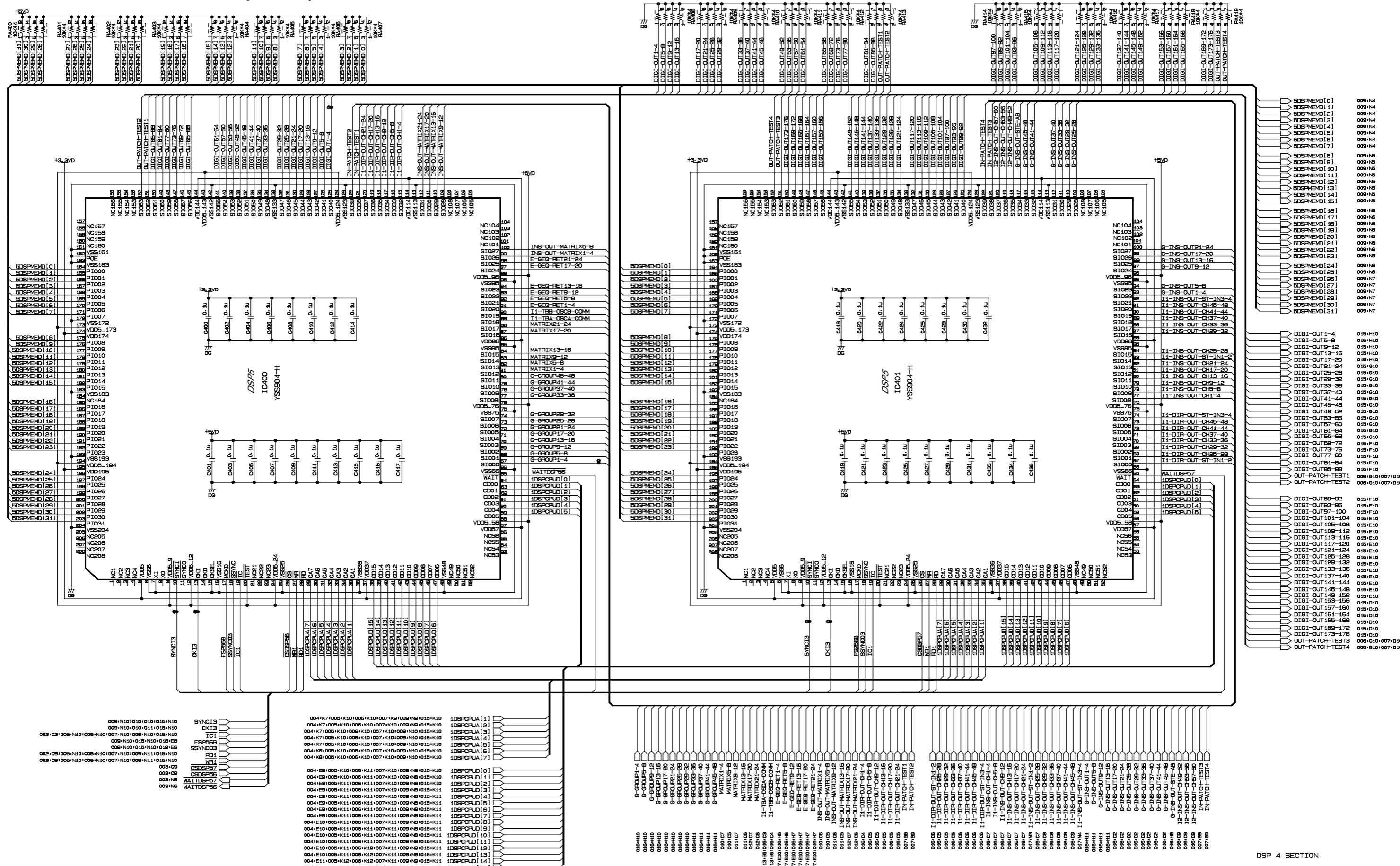
ADDRESS DATA BUFFER SECTION

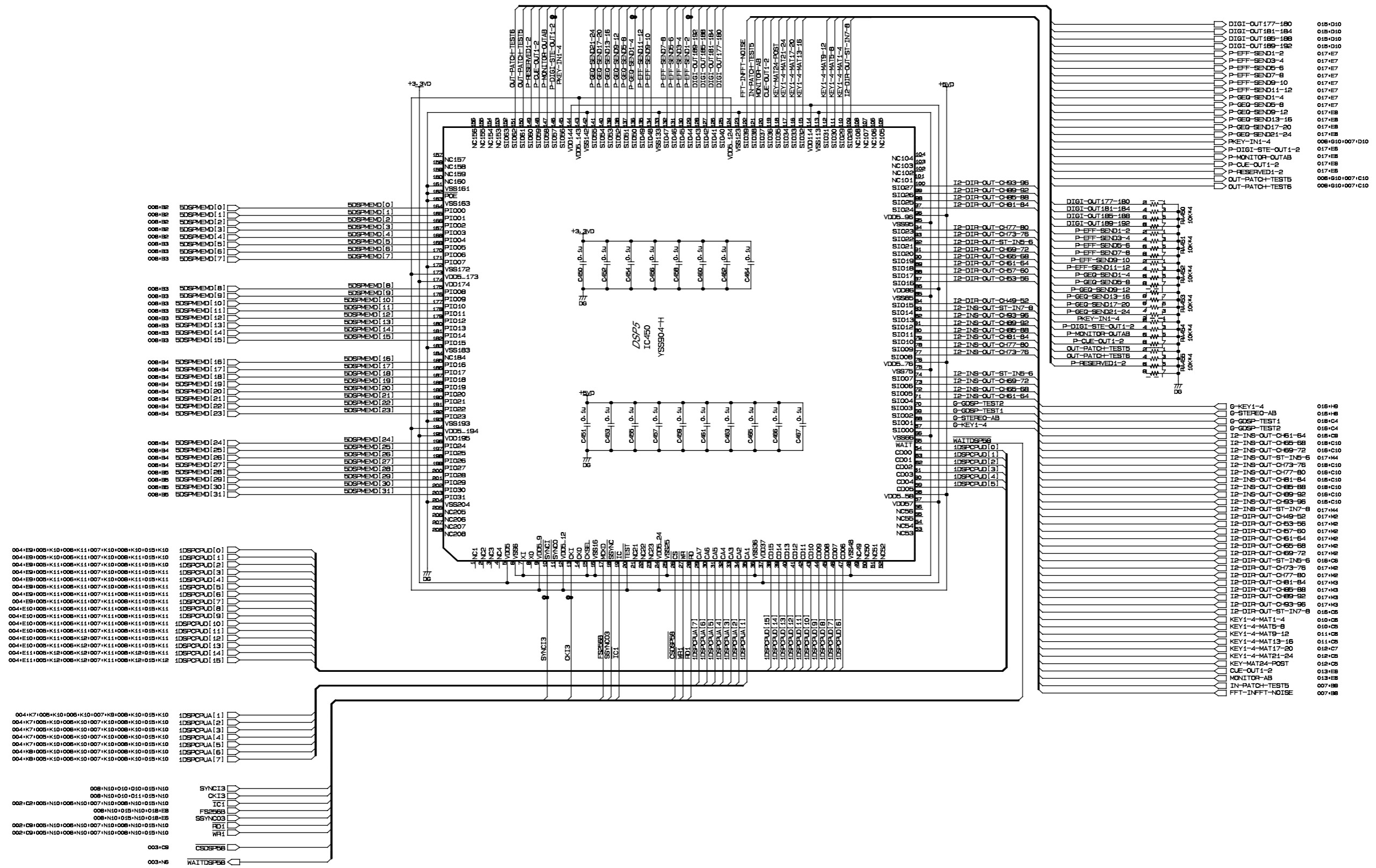
PDB CIRCUIT DIAGRAM 005 (DSP1D)

DSP1D



DSP 1 SECTION

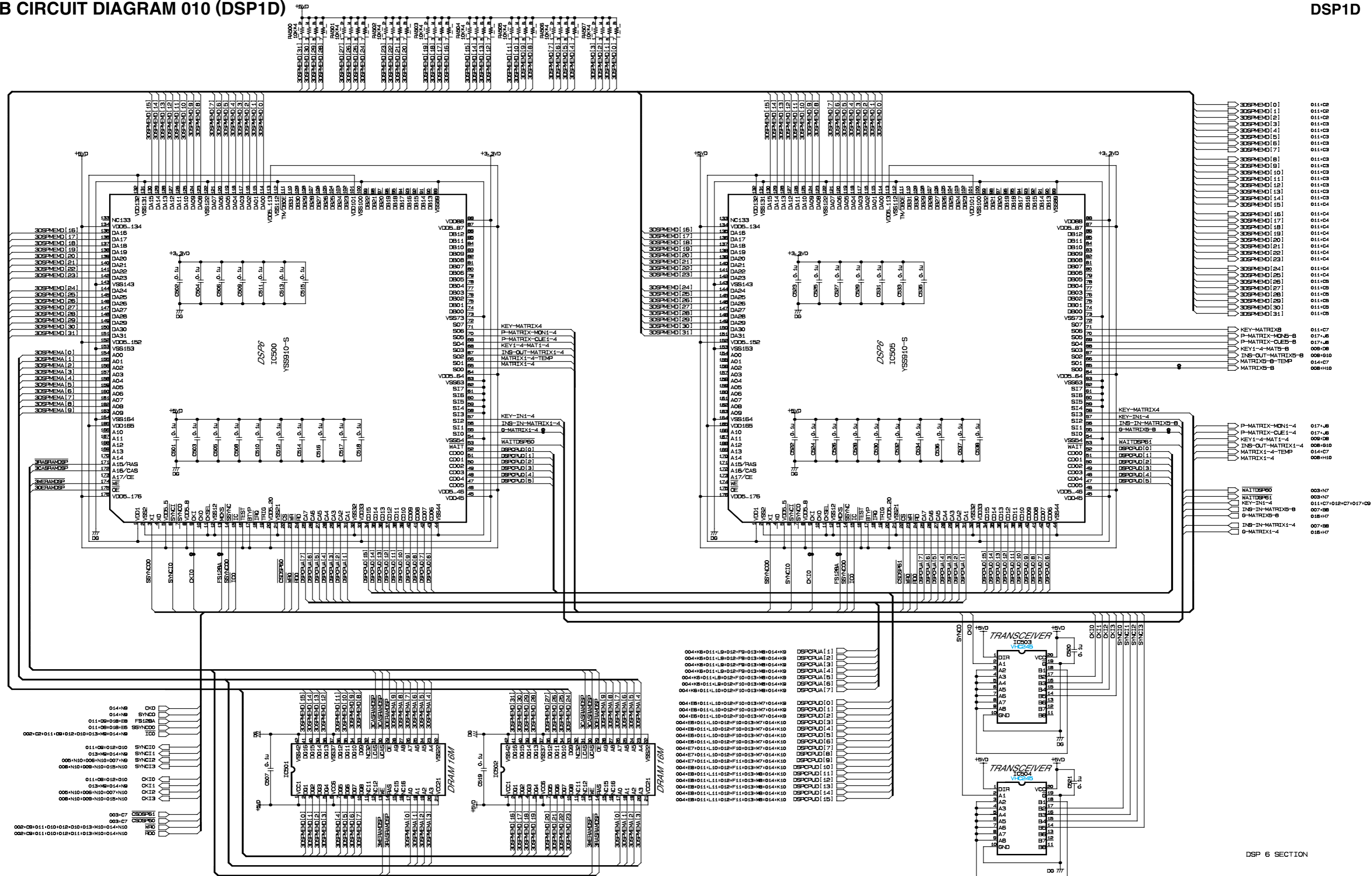


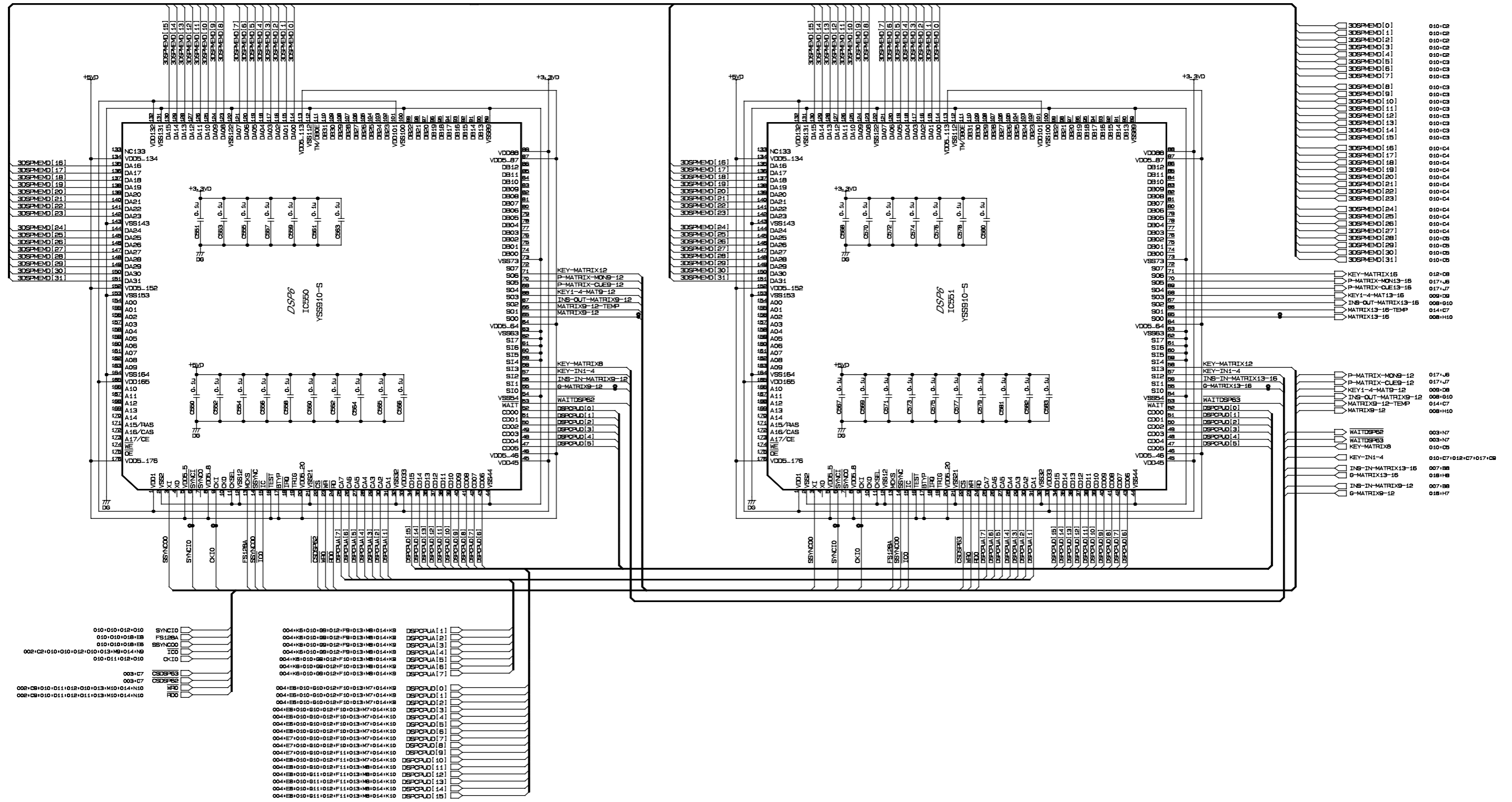


DSP 5 SECTION

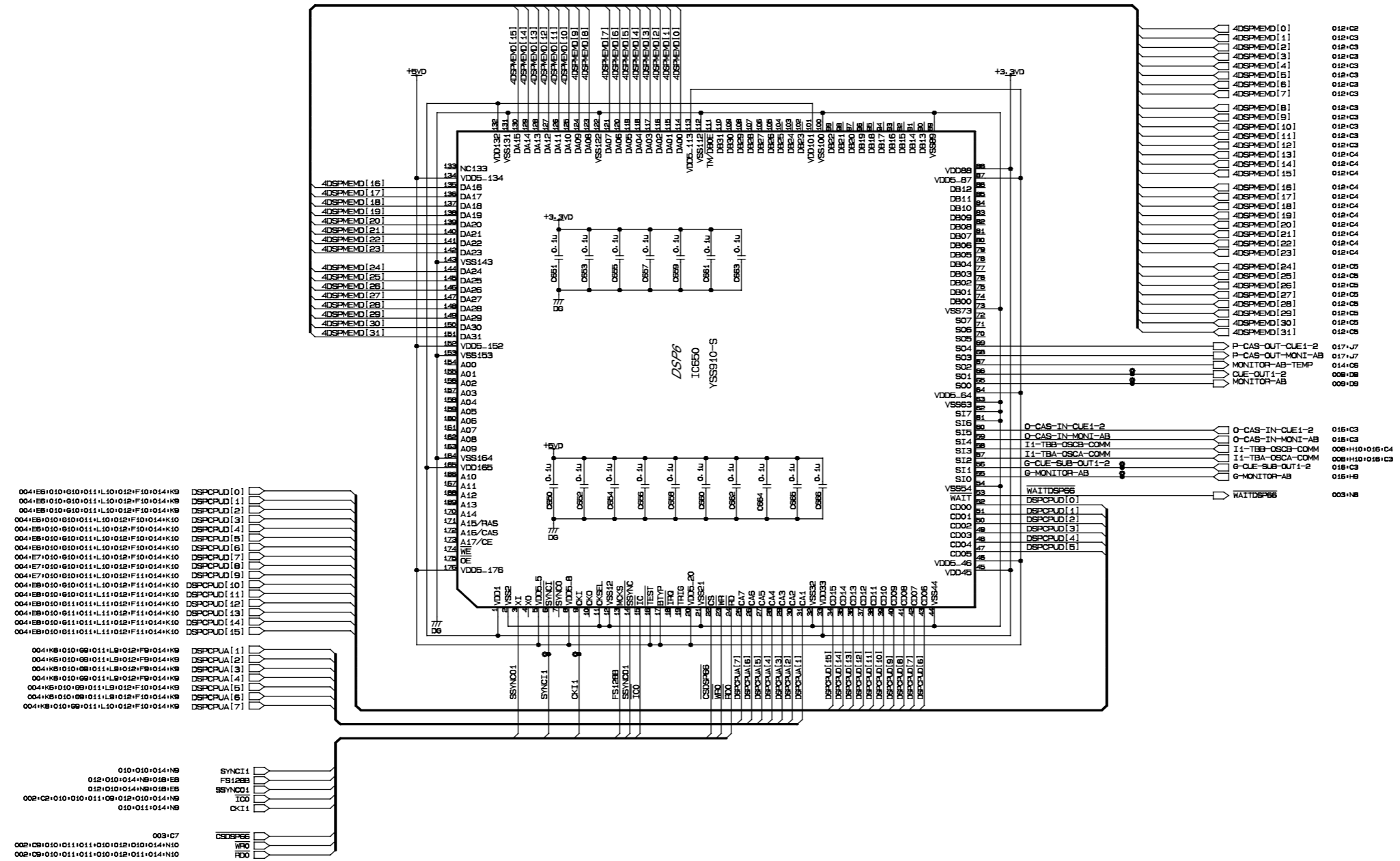
PDB CIRCUIT DIAGRAM 010 (DSP1D)

DSP1D

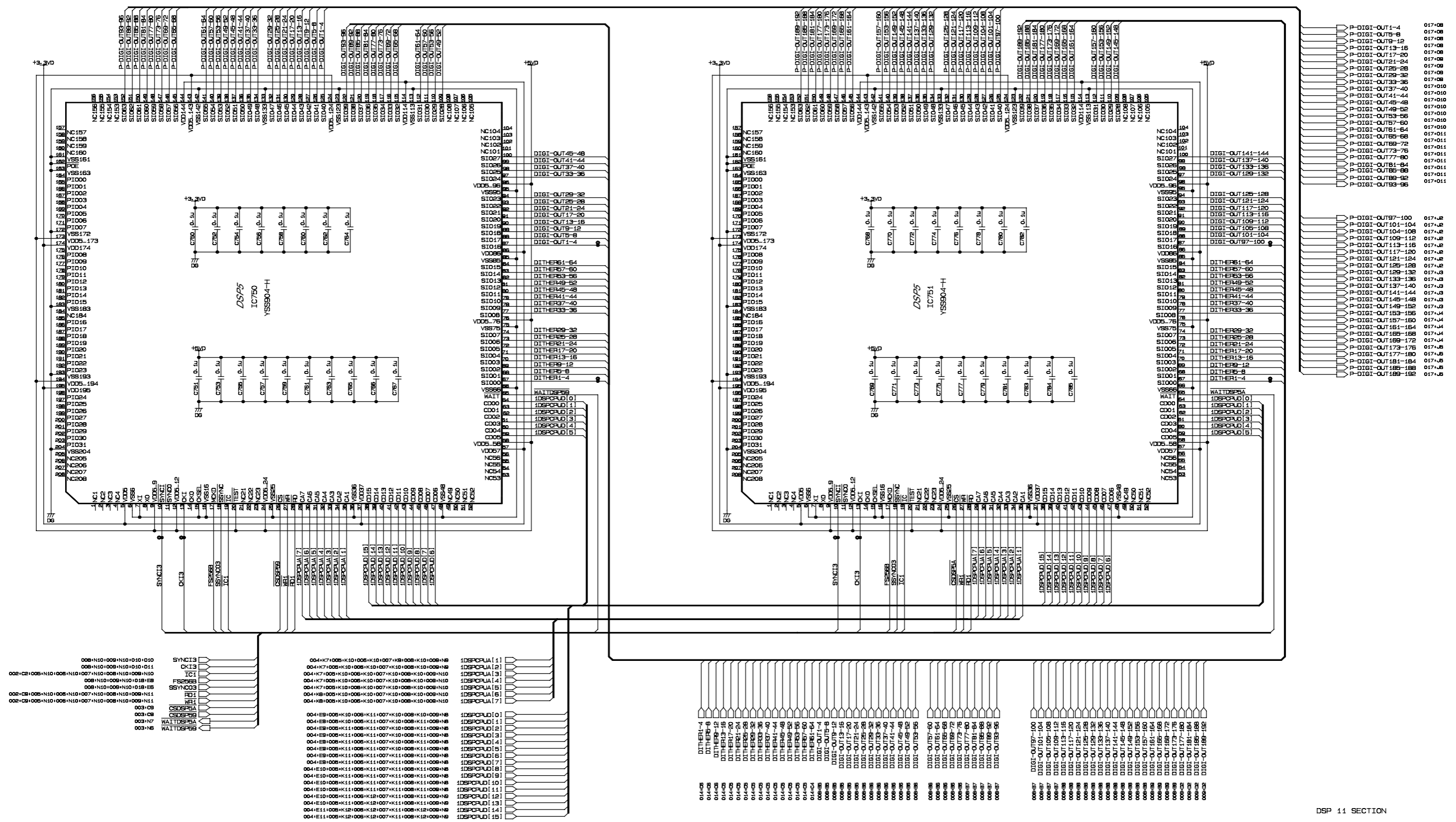




DSP 7 SECTION



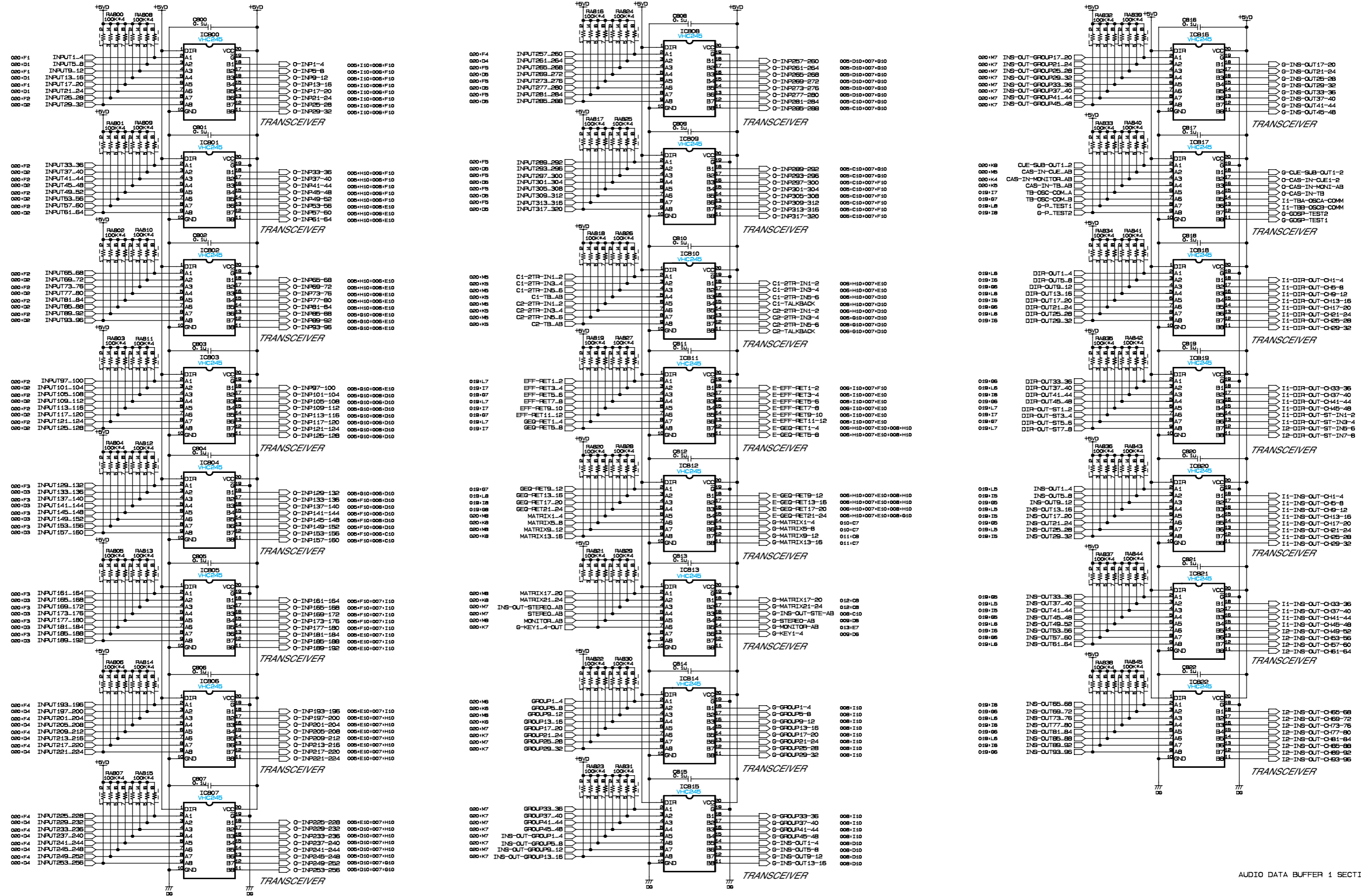
DSP 9 SECTION



DSP 11 SECTION

PDB CIRCUIT DIAGRAM 016 (DSP1D)

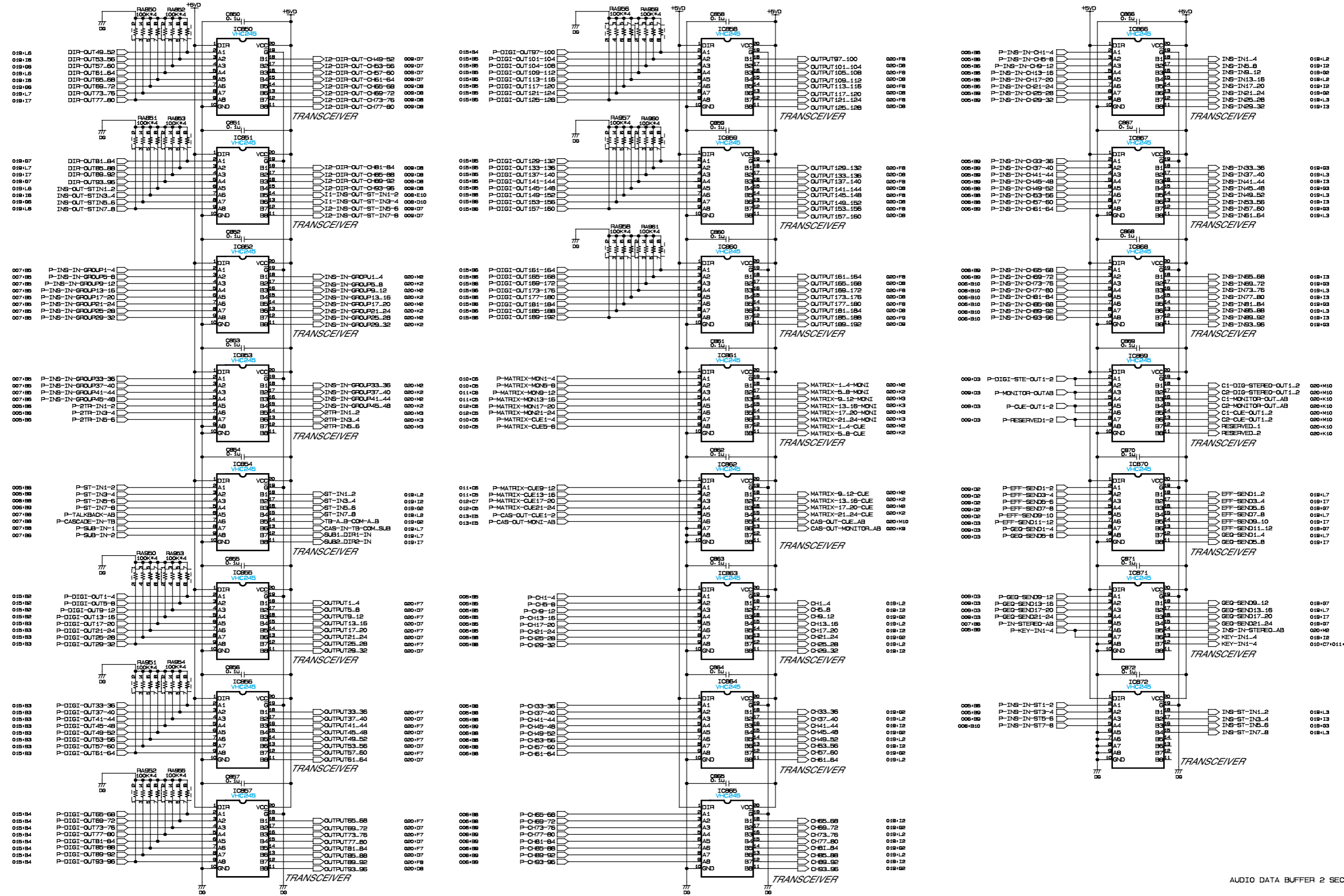
DSP1D



AUDIO DATA BUFFER 1 SECTION

PDB CIRCUIT DIAGRAM 017 (DSP1D)

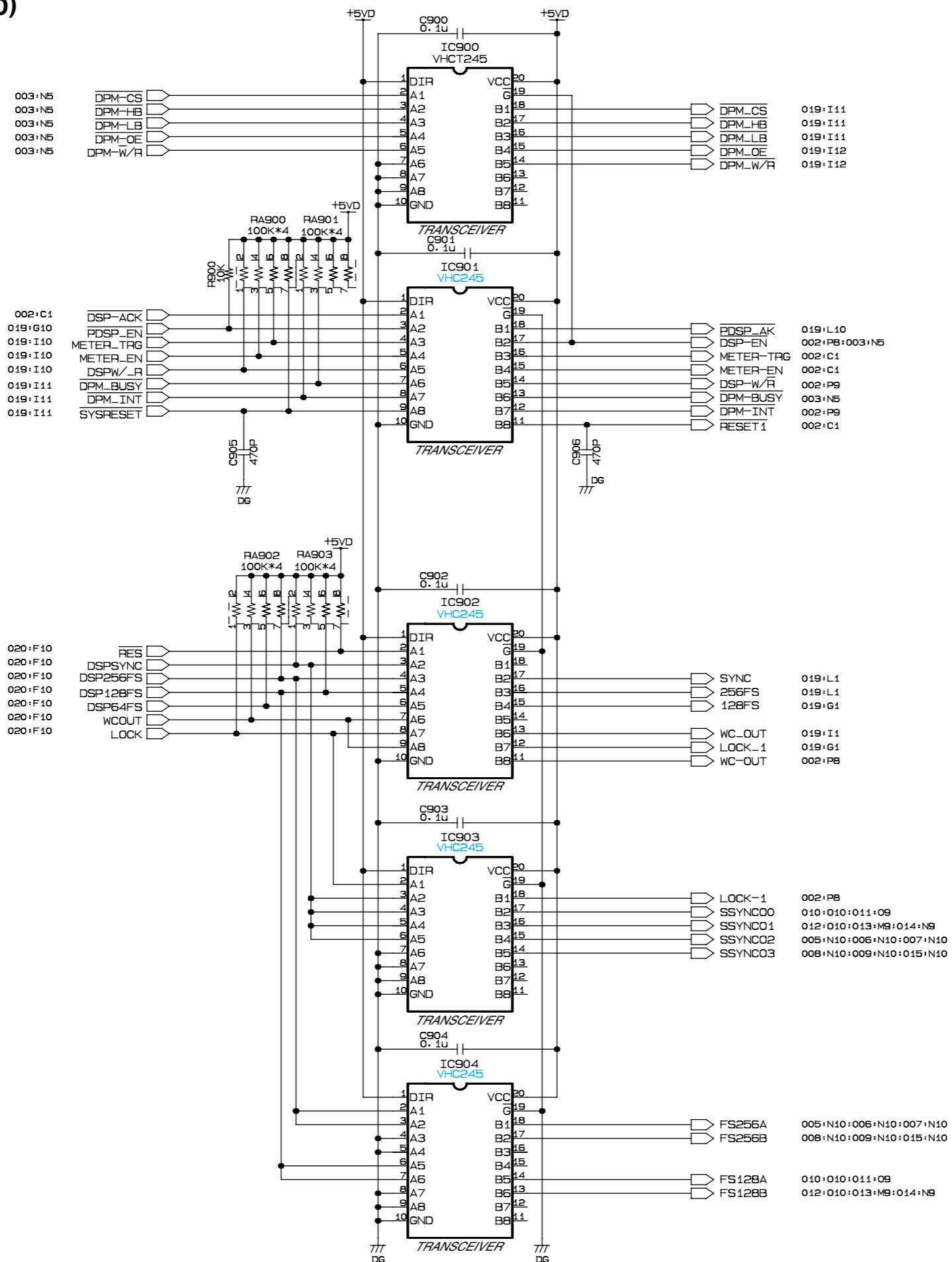
DSP1D



AUDIO DATA BUFFER 2 SECTION

■ PDB CIRCUIT DIAGRAM 018 (DSP1D)

DSP1D

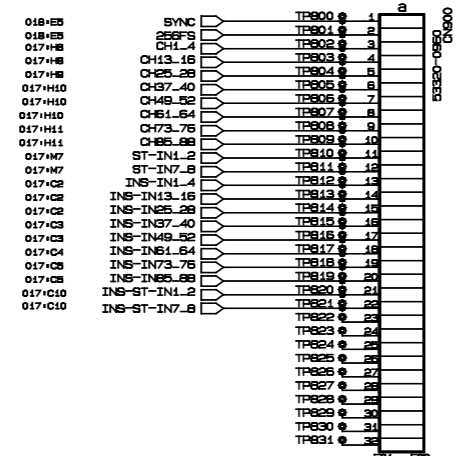


CONTROL & CLOCK BUFFER SECTION

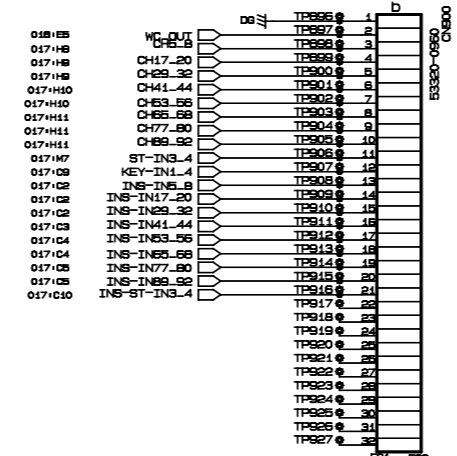
■ PDB CIRCUIT DIAGRAM 018 (DSP1D)

PDB CIRCUIT DIAGRAM 019 (DSP1D)

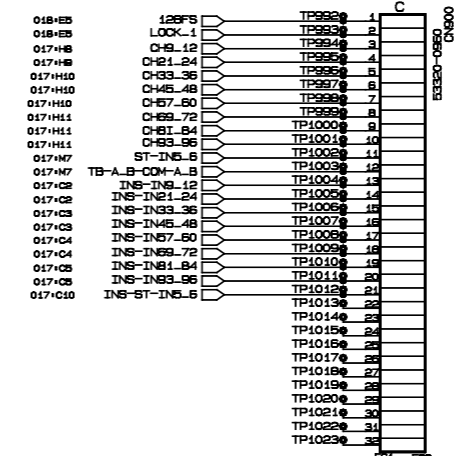
DSP1D



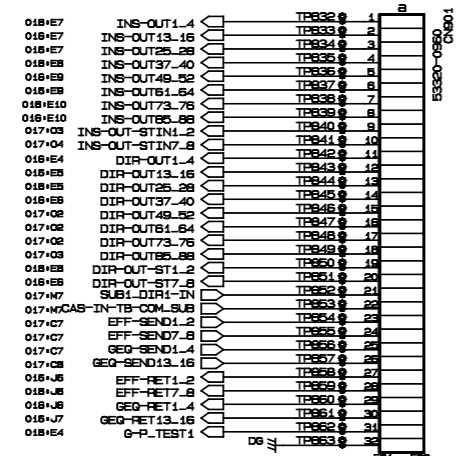
to MB11-CN101



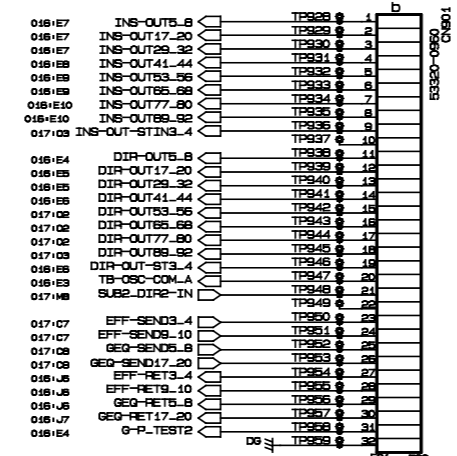
to MB11-CN101



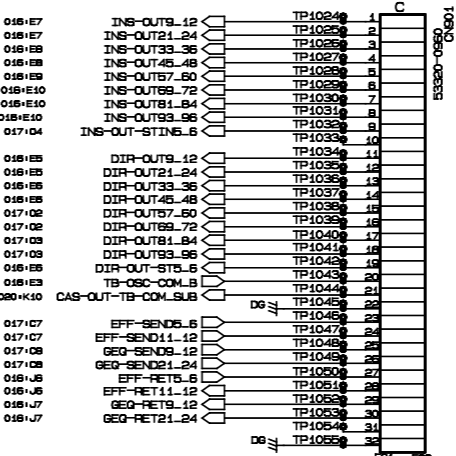
to MB11-CN101



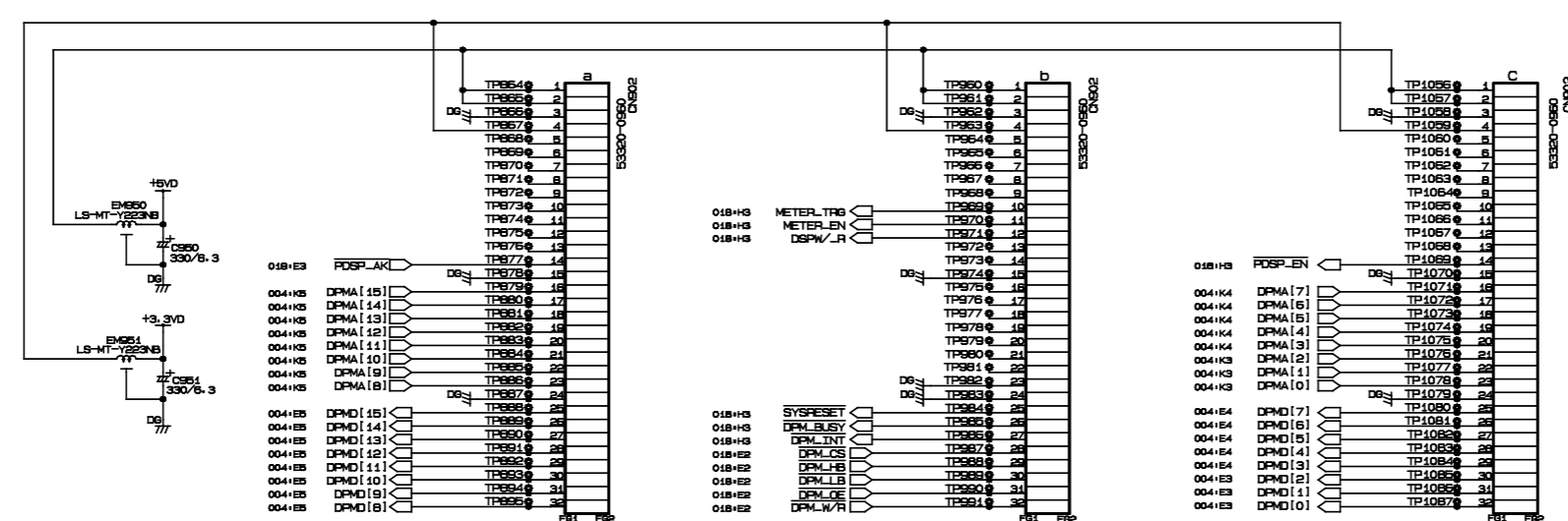
to MB11-CN102



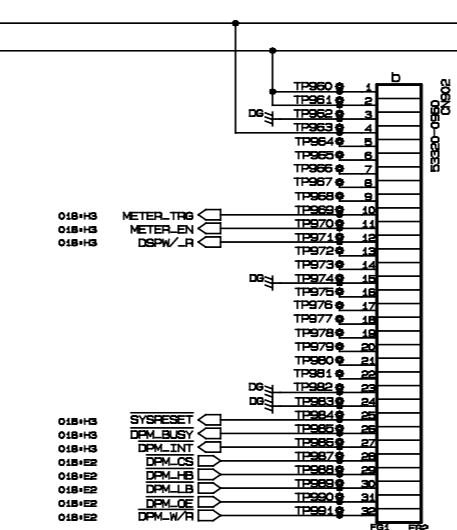
to MB11-CN102



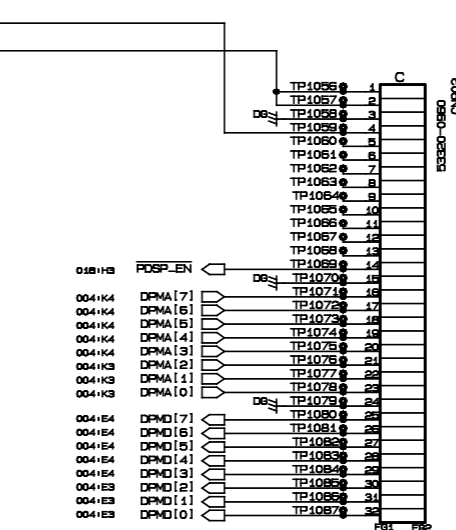
to MB11-CN102



to MB11-CN103



to MB11-CN103

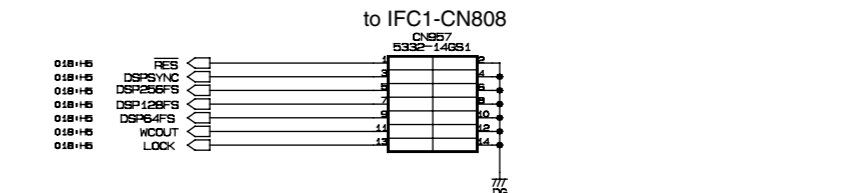
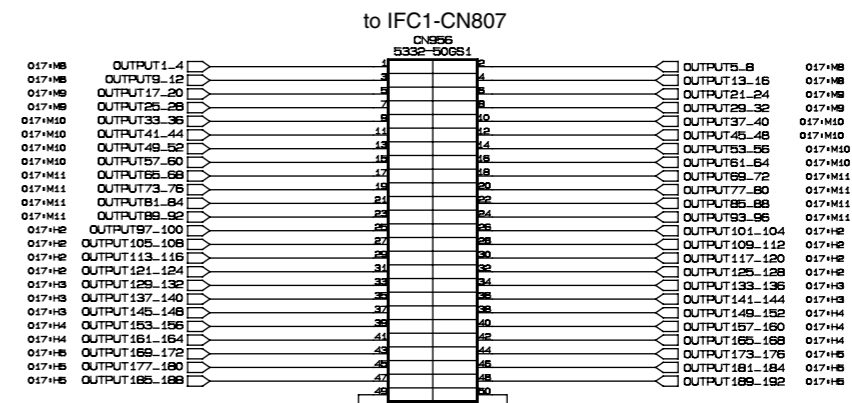
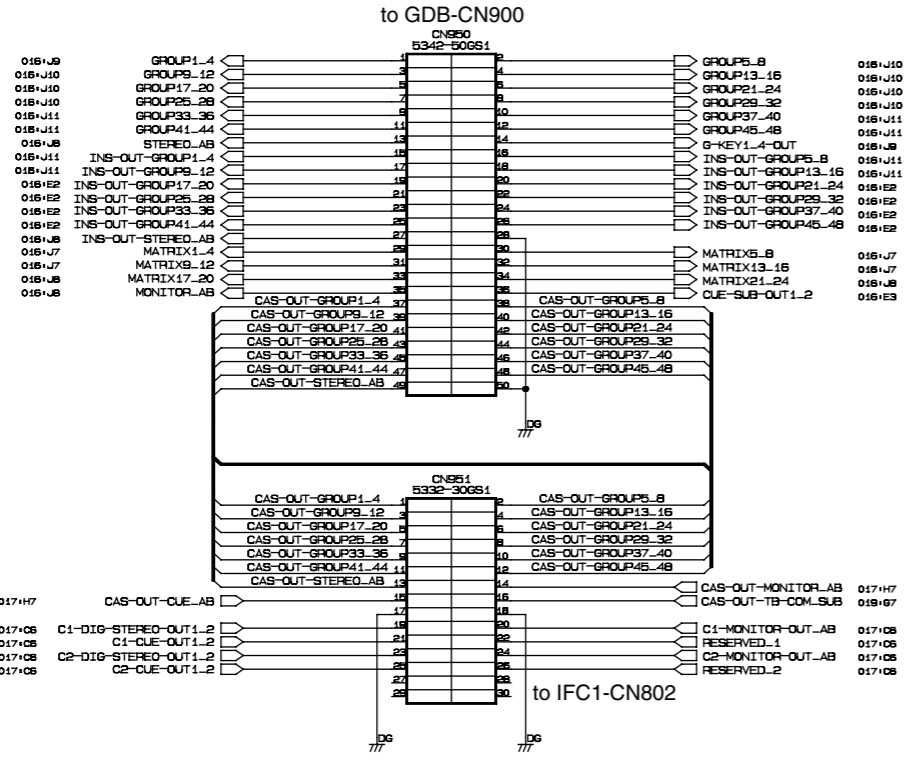
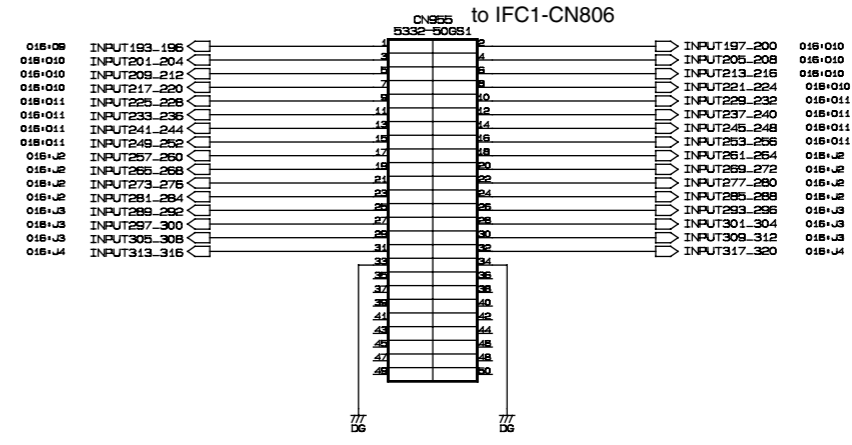
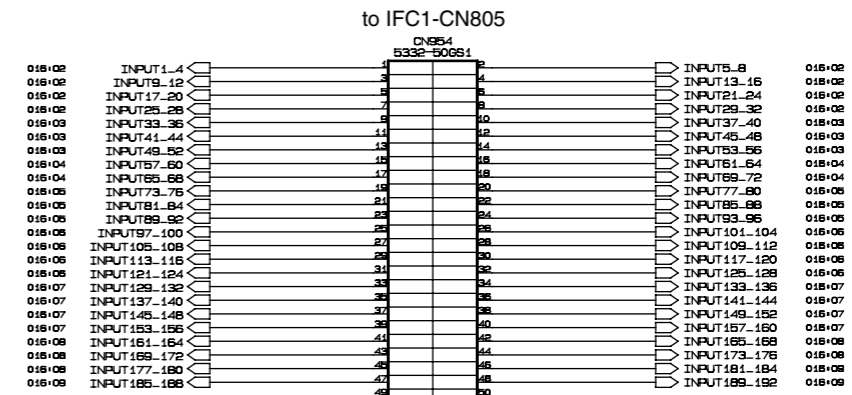
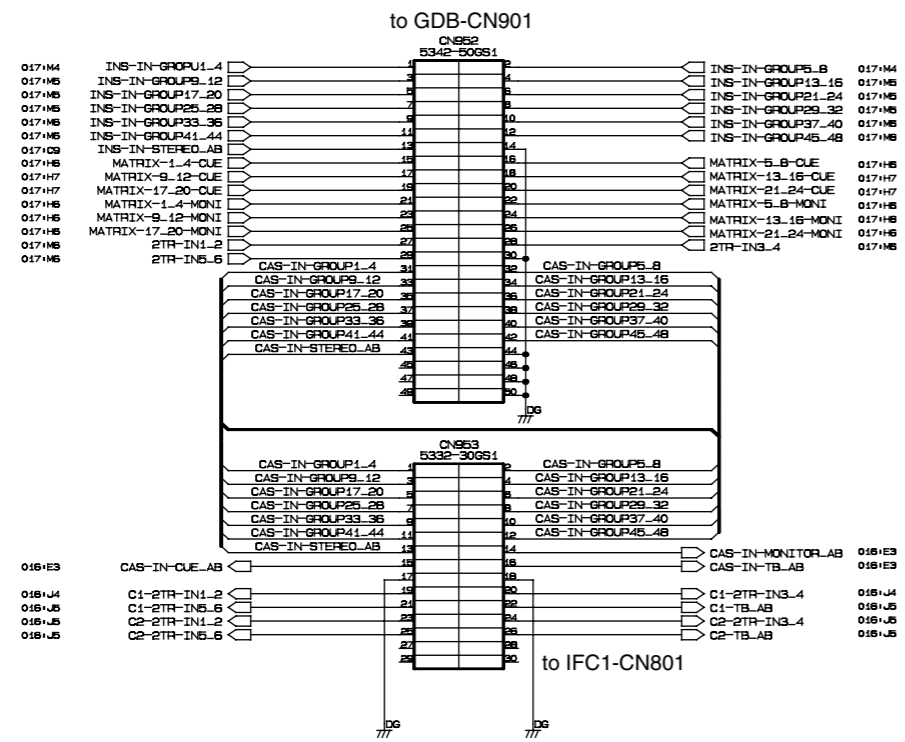


to MB11-CN103

CONNECTOR 1 SECTION

PDB CIRCUIT DIAGRAM 020 (DSP1D)

DSP1D



CONNECTOR 2 SECTION

PSB CIRCUIT DIAGRAM (DSP1D)

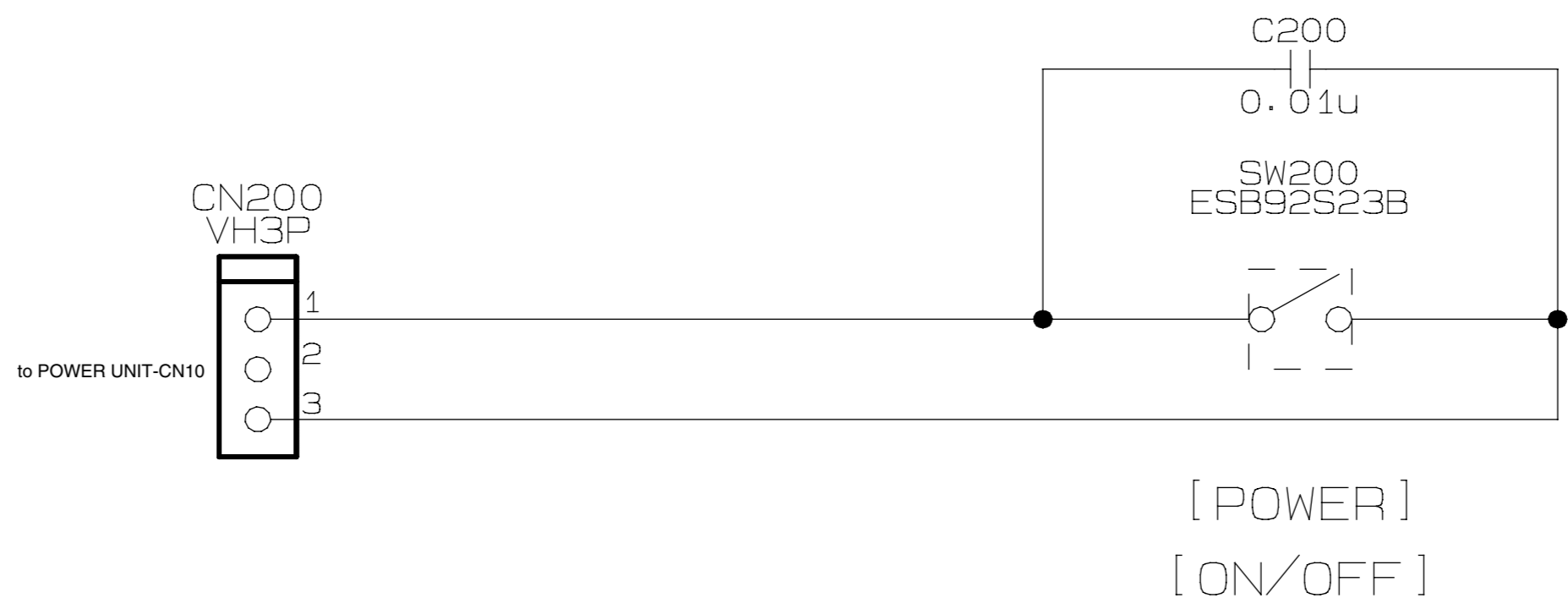
DSP1D

1

2

3

4



DSP-DC CONNECTOR DIAGRAM (DSP1D)

DSP1D

