SECTION 9

CIRCUIT SCHEMATICS & DESCRIPTIONS

COMPONENT LOCATORS

9-1. GENERAL

9-2. Schematics and Component Locators are arranged by Assembly number (A101, A102, etc.). Circuit descriptions and circuit theory are shown on the same or adjacent pages. All assembly related drawings and diagrams have the same figure number, but have different suffix letters (9-6A, 9-6B, etc.).

9-3. Parts Lists and Ordering Information will be found in Section 8.

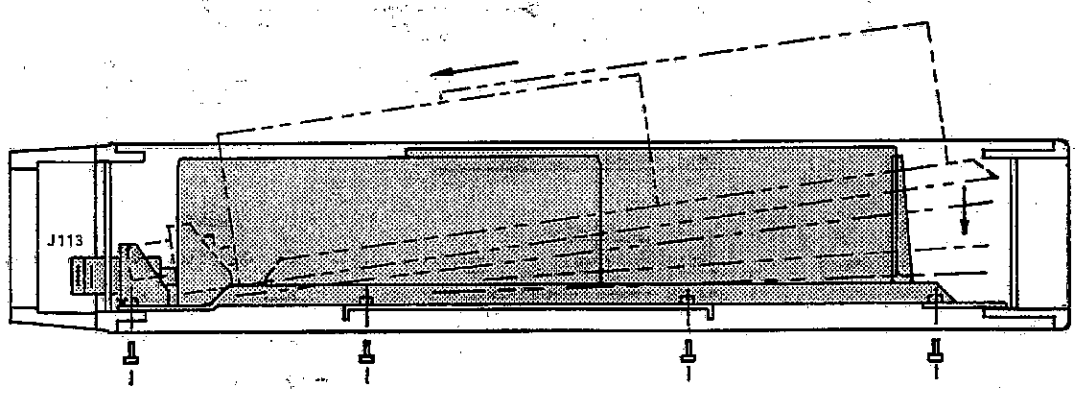
9-4. Unless otherwise specified, the following notes apply to all figures in this section.

a. Resistance values in ohms.

b. Capacitance values in microfarads ("pf" values in picofarads).

c. Connector reference numbers may not appear on part.

d. SAT = Selected at Test. Nominal value shown; part may not be installed. MP = Matched Pair.

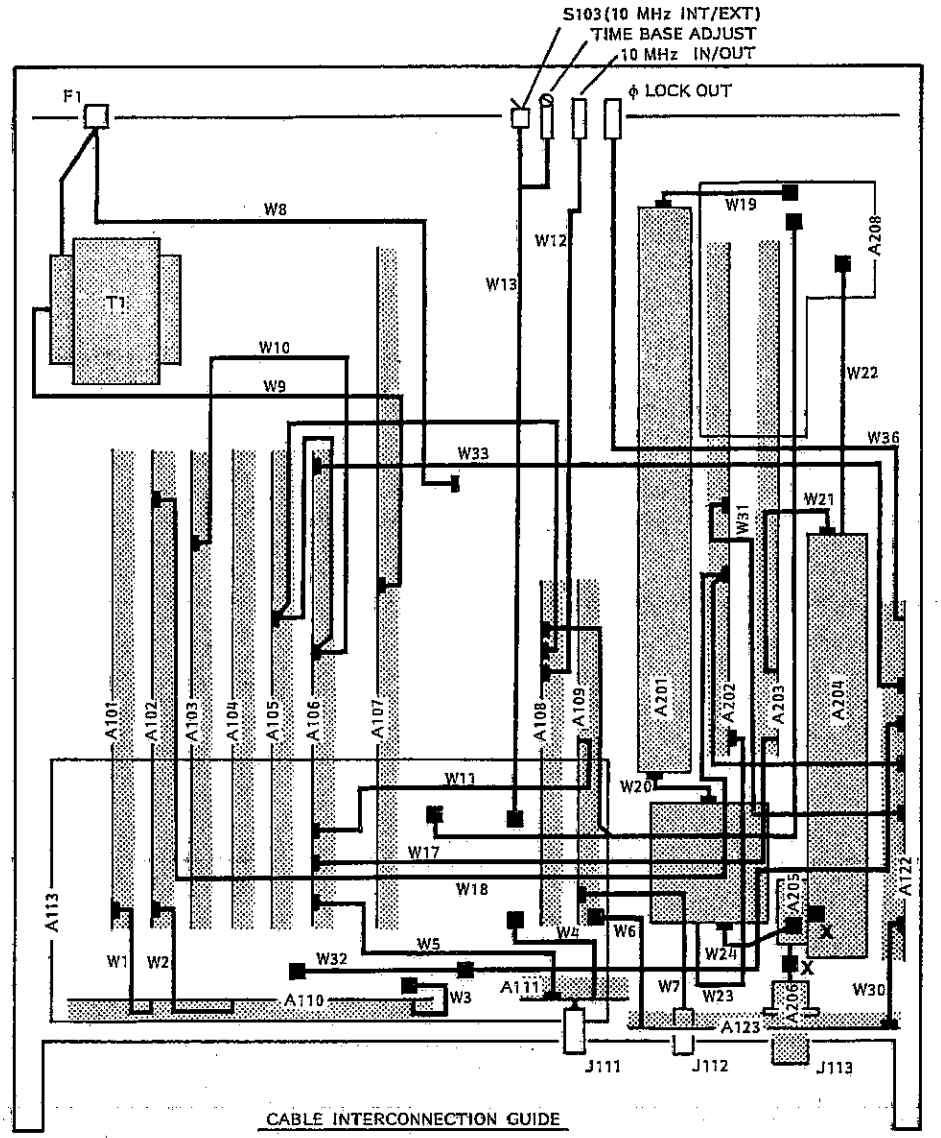


FIELD INSTALLATION OF CONVERTER ASSEMBLY

1. WITH TOP AND BOTTOM COVERS REMOVED FROM BASIC COUNTER, LOWER CONVERTER INTO POSITION AS SHOWN IN DIAGRAM. TILT J113 DOWN AND FORWARD THROUGH HOLE IN FRONT PANEL.
2. INSTALL SIX 6-32 SCREWS FROM BOTTOM SIDE OF COUNTER INTO CAPTIVE NUTS ON CONVERTER. ALIGN J113 CONCENTRICALLY WITH FRONT PANEL HOLE; TIGHTEN SCREWS.
3. PLUG CABLES W16, W17, AND W18 INTO MATING CONNECTORS ON BASIC COUNTER (SEE CABLE INTERCONNECTION GUIDE); REPLACE COVERS. REVERSE ABOVE PROCEDURE TO REMOVE CONVERTER.

FIELD INSTALLATION OF PRESCALER ASSEMBLY

1. WITH TOP COVER REMOVED, PLUG PRESCALER (A109) INTO A113-XA109. MOUNT J112 IN FRONT PANEL HOLE.
2. PLUG CABLES W7 AND W11 INTO MATING CONNECTORS PROVIDED ON MODULES (SEE CABLE INTERCONNECTION GUIDE); REPLACE COVER.



CABLE INTERCONNECTION GUIDE

BASIC COUNTER

FROM	CABLE	TO
A110J1	W1	A101J1
A110J2	W2	A102J1
A110P1	W3	A113J2
A111P1	W4	A113J4
J111	X	A111J1
A111J2	W5	A106J1
A123P1	W6	A113J6
J112	W7	A109J1
REAR PNL	W8	J101
P102(T1)	W9	A107J1
A108J1	W10	A105J1
A106J3		A103J2
A109P2	W11	A106J2
P104	W12	A108J2
P103	W13	A113J5
A122J1	W30	A123J1
A122J4	W32	A113J7
A113J8		
A122J5	W33	A106J5
A206P2	W34	A204J4
A206P1	W35	A204J3
A122P1	W36	P105(REAR PNL)

CONVERTER

FROM	CABLE	TO
A208J2	W16	A113J3
		A108J4
A203P3	W17	A106J4
A202J2	W18	A102J4
		A122J3
A201P1	W19	A208J1
A201J1	W20	A207J2
A203P2	W21	A204J2
A204P1	W22	A208J3
A202J3	W23	A207J3
		A2Q1
A205P1	W24	A207J1
A205P2	X	A204J1
A205J1	X	A206P1
A202J1	W31	A122J2

LEGEND:

X Direct-coupled (No cable assy)

Cable - to - Assembly

Cable - to - Assembly

Cable - to - Cable

CAUTION: Use care when unplugging ribbon cable connectors. Use removal tool for extraction (EIP P/N: 5000094).

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047A

FIGURE 9-1
ASSEMBLY LOCATOR
CABLE INTERCONNECTIONS

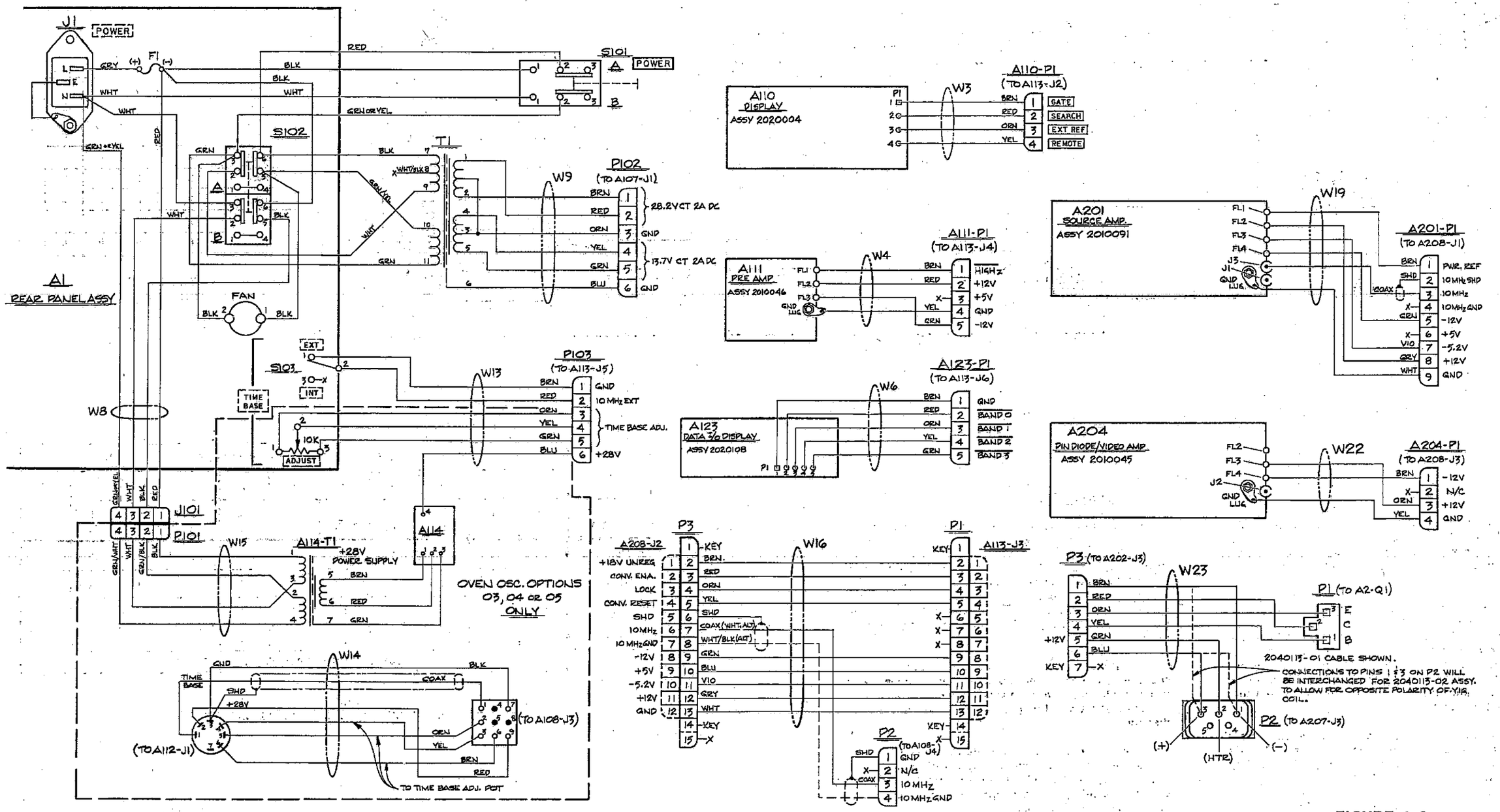
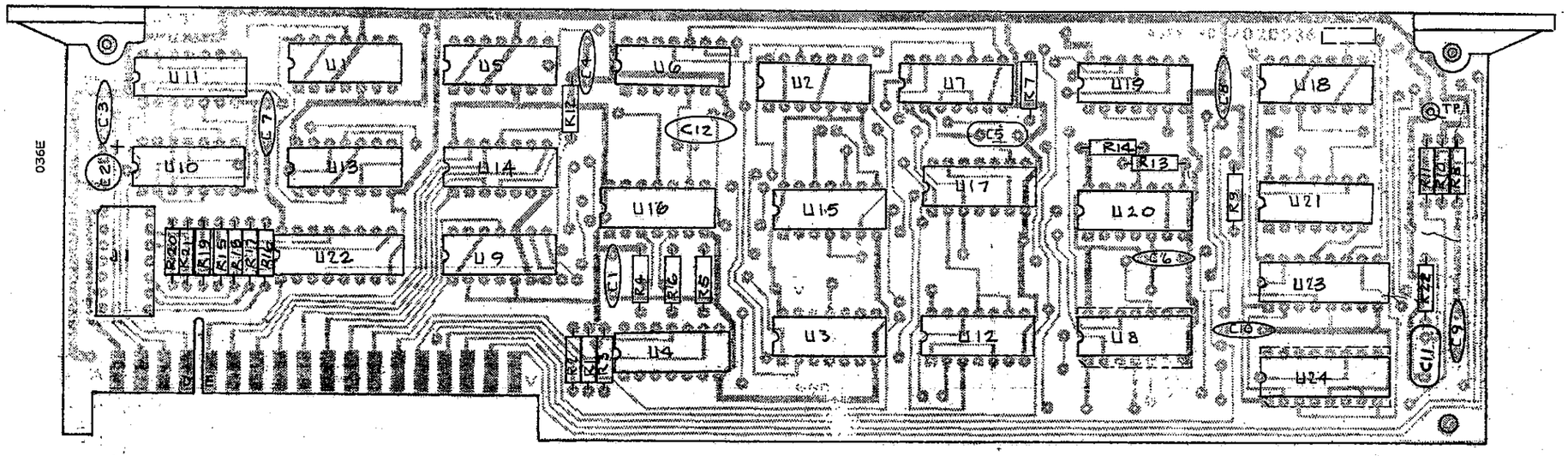


FIGURE 9-2
INTERCONNECTION
DIAGRAM
371 COUNTER

007A



GATE TIME	÷5 COUNT	B	C	D
1 sec.	5	0	0	0
100 ms.	4	0	0	1
10 ms.	3	1	1	0
1 ms.	2	0	1	0
	1	1	0	0
	0	0	0	0

TABLE 9-3B
U15 PRESETS

COUNT CHAIN 1, 2, AND 3

Count Chain Boards 1, 2, and 3 (A101, A102, and A103) perform most of the actual frequency counting functions of the direct counter. The main components are: (1) a counting chain, (2) a storage unit, and (3) the display multiplexer.

The counting chain consists of a string of ten cascaded decimal counting units (DCUs), preceded by a quinary (÷5) counting unit. The quinary counter is sufficiently fast to follow the output of the binary (÷2) counter in the High Frequency Board, forming the first DCU. The remaining DCUs are each a standard integrated circuit having four output lines to indicate the state of the counter at any given time.

The storage unit is a string of quad latches, one for each of the eleven DCUs of the counting chain. An enable signal to the storage unit causes it to load the information from the DCUs.

The display multiplexer processes the information held in the eleven elements of the storage unit. The output of the storage unit is converted to the seven line code needed to drive the seven segments of each display digit. Power is applied to each digit sequentially for 25% of the time.

Physical Organization

The Count Chain is divided among three PC Boards: A101, A102, and A103, as follows:

Board A103 contains the first quinary unit, the following four DCUs, quad latches to load the information in the DCUs, and a multiplexer to place the information in proper time sequence for the front panel display. A variable +5 VDC supply for display brightness is also provided.

Board A102 includes the six remaining DCU's of the counting chain, a set of associated quad latches, and two multiplexers. Two decoders convert the multiplexer outputs to the seven line code which drives the visual display.

Board A101 includes the third decoder-driver, buffer circuits for the front panel RESOLUTION switches, timing circuits for the multiplexer and display. A101 also contains circuitry which suppresses zeros to the left of the first significant digit.

	LATCH - DISPLAY DIGIT POSITION										
	1	2	3	4	5	6	7	8	9	10	11
GATE TIME	10 GHz	1 GHz	100 MHz	10 MHz	1 MHz	100 kHz	10 kHz	1 kHz	100 Hz	10 Hz	1 Hz
1 sec.	1	2	3	4	5	6	7	8	9	10	11
100 ms.	1	2	3	4	5	6	7	8	10	11	-
10 ms.	1	2	3	4	5	6	7	10	11	-	-
1 ms.	1	2	3	4	5	6	10	11	-	-	-
	NUMBER OF DCU SUPPLYING DATA TO LATCH										

TABLE 9-3A
DISPLAY DIGIT POSITION vs. SUPPLYING DCU

FIGURE 9-3A
COMPONENT LOCATOR
COUNT CHAIN 1 (A101)

COUNT CHAIN 1 (A101)

Count Chain 1 (A101) generates the correct timing sequence and control commands for the multiplex system, provides leading zero blanking of the display, and controls shifting of data from DCU to DCU in the counting chain in response to changes in gate time length.

In addition, A101 accepts the inputs from the front panel RESOLUTION switches, and processes them into control signals for the multiplex system and the Time Base Generator on Control 1 (A105). A101 also contains the third decoder driver for the display.

Multiplex System Operation

The multiplex system is composed of three individual multiplex channels designated MUX 1, MUX 2, and MUX 3. Each MUX channel includes a four-to-seven line decoder-driver which drives directly segments of the front panel display. MUX 1 controls the four most-significant digits of the display (10 GHz, 1 GHz, 100 MHz and 10 MHz). MUX 2 controls the middle three digits and MUX 3 the four least-significant digits. The input information for MUX 1, 2, and 3 is obtained from the eleven quad-latch units on Count Chains 2 and 3 (A102 and A103).

In order for each multiplex circuit and decoder to drive four digits, the multiplex timing sequence is broken down into four intervals designated Time Frames 1 through 4 (TF1 - TF4). Only one display digit in each channel is illuminated in a given Time Frame, as determined by the display digit selectors. The actual number displayed by the selected digit is determined by segment drive from the decoder-driver which drives all corresponding segments in that channel in parallel. If one of the selected digits is not to be illuminated, its segment drive is canceled by a blanking signal to the appropriate decoder-driver. Table 9-3C shows, for each channel and for each of the gate times, the relationship of the Time Frames to MUX address, the DCU addressed, the display digit selected by the MUX, and whether the drive is enabled.

For each available gate time, Table 9-3A shows the resulting position in the display at which the information from each DCU is presented. The DCUs not displayed in shorter gate times are those removed from the counting chain, as described in the paragraphs on Count Chain 3 (A103).

In addition to blanking digits 9, 10, and 11 of the display (as shown in Table 9-3A), three more digits may be blanked by depressing the appropriate RESOLUTION switches. The gate time remains at 1 ms. in these positions.

The MUX timing sequence is actually three groups of four time frames. The first two groups occur at a rate of 2.5 MHz, the last at 25 kHz. The fast groups are used only to gather zero suppression information; display occurs only during the slow group.

Multiplex Sequence Generator

Clock pulses for the multiplexer are obtained from a 2.5 MHz clock signal derived from the 10 MHz Time Base Oscillator (A116 or A112). This signal is processed through a circuit composed of DCUs U1 and U5, ÷16 U2, the inverters of U6, and the gates of U11. The "SET 9" inputs of the DCUs are tied together, so that applying a high level to this input causes the 2.5 MHz clock to be fed through the gates to U2 at a 2.5 MHz rate.

With a low "SET 9" the input to U2 is one-hundredth the 2.5 MHz rate, or 25 kHz. The "SET 9" inputs to U1 and U5 are the inverted D output from U2, which is high when U2 is reset. The clock to U2 is then at a 2.5 MHz rate for eight pulses after reset. The D output then switches, and the clock rate drops to 25 kHz for the next four pulses. The A and B outputs of U2, plus their complements, are combined in the four NOR gates of U7 to produce the four MUX timing signals TF1, TF2, TF3, and TF4. The output TF4 is combined with U2 output D, and applied to the J input of flip-flop U23B. The clock to U23 and U24 is the same as the input to U2. The end of the fourth slow clock pulse then triggers U23B which resets U2. The clock pulses then return to the 2.5 MHz rate. The next pulse resets U23B and returns U1, U2, and U5 to their initial states.

The result is to produce a frame consisting of eight MUX time intervals at the 2.5 MHz rate, followed by four at the 25 kHz rate. One extra clock pulse resets the generator. The drive to the front panel display from U10 is gated off by the D output of U2 during the eight fast pulses in this train.

Count Chain Data Shift Controls

As the length of the Gate Time is varied by changing the front panel RESOLUTION switches, the counting chain on A103 is also modified by removing DCUs from the string. This is described in the Circuit Description of Count Chain 3 (A103). In the 1 Hz RESOLUTION setting (1 sec. Gate Time), all eleven DCUs are in the counting chain. With 10 Hz RESOLUTION (100 ms. Gate Time), the seventh (10 kHz position) DCU is bypassed. With 100 Hz RESOLUTION the seventh and eighth DCUs are bypassed, and with 1 kHz RESOLUTION the seventh through ninth DCUs are bypassed.

As indicated in Table 9-3A, with shorter gate times, the information in the eighth through eleventh DCUs must be shifted into lower numbered latches (7 through 10) to read out and be displayed in the proper front panel position. The data shift controls which accomplish this function are produced in ICs U9, U13, U14, U15, and U16.

To allow the data shift to take place on A103, presettable DCUs are used in the counting chain. The output lines of the eleventh DCU feed the data input lines of the tenth DCU. The tenth DCU feeds data to the ninth DCU, the ninth feeds data to the eight, and the eighth feeds data to the seventh. When a LOAD DATA command is applied to one of these DCUs, it then loads data from and assumes the same state as the higher numbered DCU to its right. To shift data one place left in the highest five DCUs of the counting chain (DCUs 7 through 11), it is necessary to apply the data LOAD pulses in sequence to DCUs 7, 8, 9, 10, and then a reset pulse to DCU 11 (load zero). If the load pulses were applied simultaneously to all DCUs, they

would all go immediately to zero. The necessary sequence of pulses is produced by a 4-10 line decoder on A103 which is driven by a DCU on A101. The DCU is stepped through states 0 to 9 by a clock input, with the 1, 3, 5, 7, and 9 outputs of the decoder activating the load inputs of DCUs 7, 8, 9, 10, and 11 respectively. Every ten inputs to the data shift DCU on A101 cause the data in the DCUs on A103 to shift left one position.

To place the counting chain data in the proper position after the end of each gate time interval, clock pulses must be applied to the data shift DCU. With 1 second gate time, no pulses are required; with 100 ms. gate time, ten pulses are required; with 10 ms. gate time, 20 pulses; and with 1 ms. gate time, 30 pulses. The number of clock pulses is regulated by presettable DCU U15 and associated gates in U13, U14, and U16.

The ÷5 part of U15 is preset during the gate time to the states shown in Table 9-3B. Data inputs to produce them are the four gate control lines. The ÷2 part of U15 directly controls the gate through which the 2.5 MHz clock is applied to data shift DCU U9. With 1 second gate time, the binary is not preset, and no data shift clock pulses occur. With shorter gate time settings, the ÷2 is set during gate time, with data shift clock pulses occuring after gate time is complete. Every ninth pulse to the data shift DCU (U9) produces an output through AND gate U13 which is applied to the ÷5 input of U15. The input to U15 is combined with the D output in another AND gate, and applied to the ÷2 input. When the ÷5 count reaches zero state, the ÷2 state is also zero, and the data shift clock turns off. Depending upon the ÷5 preset state, either 0, 10, 20, or 30 clock pulses have occured, and the counting chain data has shifted 0, 1, 2, or 3 places to the left.

Additional gates inhibit the Sequence Generator during data shift. Update Data is also inhibited during this time.

Display Selector Drive Generator

This drive is actually the same as the MUX Time Frame signals during the slow scan. The signals TF1 - TF4 provide one input to each of the four NAND gates of U10. The other four inputs are tied together with the D output of U2. This D output is high only after the first eight fast scan signals (first two groups of TF1 - TF4) have occurred, and the slow scan (third group of TF1-TF4) is taking place. The NAND gate outputs are the inputs to the digit selector drivers on Display Board (A110).

Signal Generators for Blanking and Gate Time Controls

These generators operate on the inputs from the six front panel RESOLUTION switches. They are processed in the inverters of U4 and U8, and the NOR gates of U3 and U12, to produce nine output control signals. Five of these are used on A101 principally to control display blanking. The remaining four are used externally, as well as on A101. The four lines, one of which is high for each gate time, are fed to the gate generator on A105, which then determines the gate time. The signals are also fed to Count Chain 3 (A103) where they control the length of the counting chain as the gate time is changed. One of these four signals, plus the remaining five, are used on A101 to control least significant digit blanking by the RESOLUTION switches. Three outputs of U20 produce blanking signals in Display Driver 2, by combining MUX timing outputs TF2, TF3, and TF4 with the RESOLUTION switch signals from U4 and U8. This produces blanking in readout digit 7 (as indicated in Table 9-3C), plus blanking of digits 5 and 6 in resolution settings for 100 kHz and 1 MHz. U17 produces the blanking signals in Display Drive 3 (as indicated in Table 9-3C), plus complete blanking (TF1 - TF4) in the 100 kHz and 1 MHz resolution settings.

Leading Zero Suppression Circuitry

The portion of A101 related to leading zero suppression is detailed in Figure 9-3C. This function is accomplished in two steps. Initially, the circuit determines if any of the three channels contains non-zero data. If all data is zero, it disables the blanking and displays all zeros. If there is non-zero data, it locates the first channel containing this data.

The most vital portion of the zero suppression circuitry is contained within the decoder-drivers themselves. This is a zero detection circuit which is enabled by the ripple blanking input (RBI). If RBI is enabled (low), the presence of zero data causes the ripple blanking output (RBO) to be energized (low). The decoder-driver also contains a blanking input (BI) which blanks the digit when energized (low). BI and RBO are internally tied together so that the pin designated BI/RBO serves both as an input and an output. Thus, if RBI is enabled, zero data will energize RBO, which is equivalent to energizing BI, and the digit is blanked. Thus, a digit may be blanked either by applying a low-level to BI/RBO, or by the presence of zero data when RBI is enabled.

The first circuit function is to determine if any of the three channels contain non-zero data. All flip-flops are reset enabling the RBI on all decoder-drivers. As the multiplex system rapidly scans through its first four Time Frames, any non-zero data in a decoder-driver will be indicated by the RBO going high. This in turn enables the J input of the corresponding flip-flop. The next timing pulse sets that flip-flop and disables the RBI of that decoder-driver. At the end of the first multiplex group, the presence of any non-zero data is indicated by a set flip-flop. A set flip-flop enables the J input of the following flip-flop. This insures that non-zero data in any decoder-driver causes all flip-flops further down the chain to be set within two additional Time Frames.

If all data is zero, then the gating is such as to allow the eight clock pulse (TF4 of the second fast group) to set the first two flip-flops and enable the third. The ninth clock pulse then sets the third flip-flop. This then disables all ripple blanking inputs so no blanking will occur with all zero data.

The remaining task is to determine the first channel with non-zero data. Gates are arranged so that the ninth clock pulse will reset the first flip-flop which is in the "set" state via the K input, and thus enable the corresponding RBI, prior to the start of the slow scan. The internal ripple blanking circuitry will then blank all zeros until the first non-zero data is present.

Gate Time	Sequence Time Frame in MUX Sequence	MUX Address a	MUX Address b	CHANNEL 1 DCU Addressed	CHANNEL 1 Display Digit Selected	CHANNEL 1 Drive Enable	CHANNEL 2 DCU Addressed	CHANNEL 2 Display Digit Selected	CHANNEL 2 Drive Enable	CHANNEL 3 DCU Addressed	CHANNEL 3 Display Digit Selected	CHANNEL 3 Drive Enable
1 sec.	TF-1	0	0	1	1	+	5	5	+	8	8	+
	TF-2	1	0	2	2	+	6	6	+	9	9	+
	TF-3	0	1	3	3	+	7	7	+	10	10	+
	TF-4	1	1	4	4	+	11	7	−	11	11	+
100 ms.	TF-1	0	0	1	1	+	5	5	+	9	8	+
	TF-2	1	0	2	2	+	6	6	+	10	9	+
	TF-3	0	1	3	3	+	7	7	−	11	10	+
	TF-4	1	1	4	4	+	8	7	+	8	11	−
10 ms.	TF-1	0	0	1	1	+	5	5	+	10	8	+
	TF-2	1	0	2	2	+	6	6	+	11	9	+
	TF-3	0	1	3	3	+	7	7	−	8	10	−
	TF-4	1	1	4	4	+	9	7	+	9	11	−
1 ms.	TF-1	0	0	1	1	+	5	5	+	11	8	+
	TF-2	1	0	2	2	+	6	6	+	8	9	−
	TF-3	0	1	3	3	+	7	7	−	9	10	−
	TF-4	1	1	4	4	+	10	7	+	10	11	−

TABLE 9-3C
GATE TIME vs. SEQUENCE TIME FRAME and DCU ADDRESSED

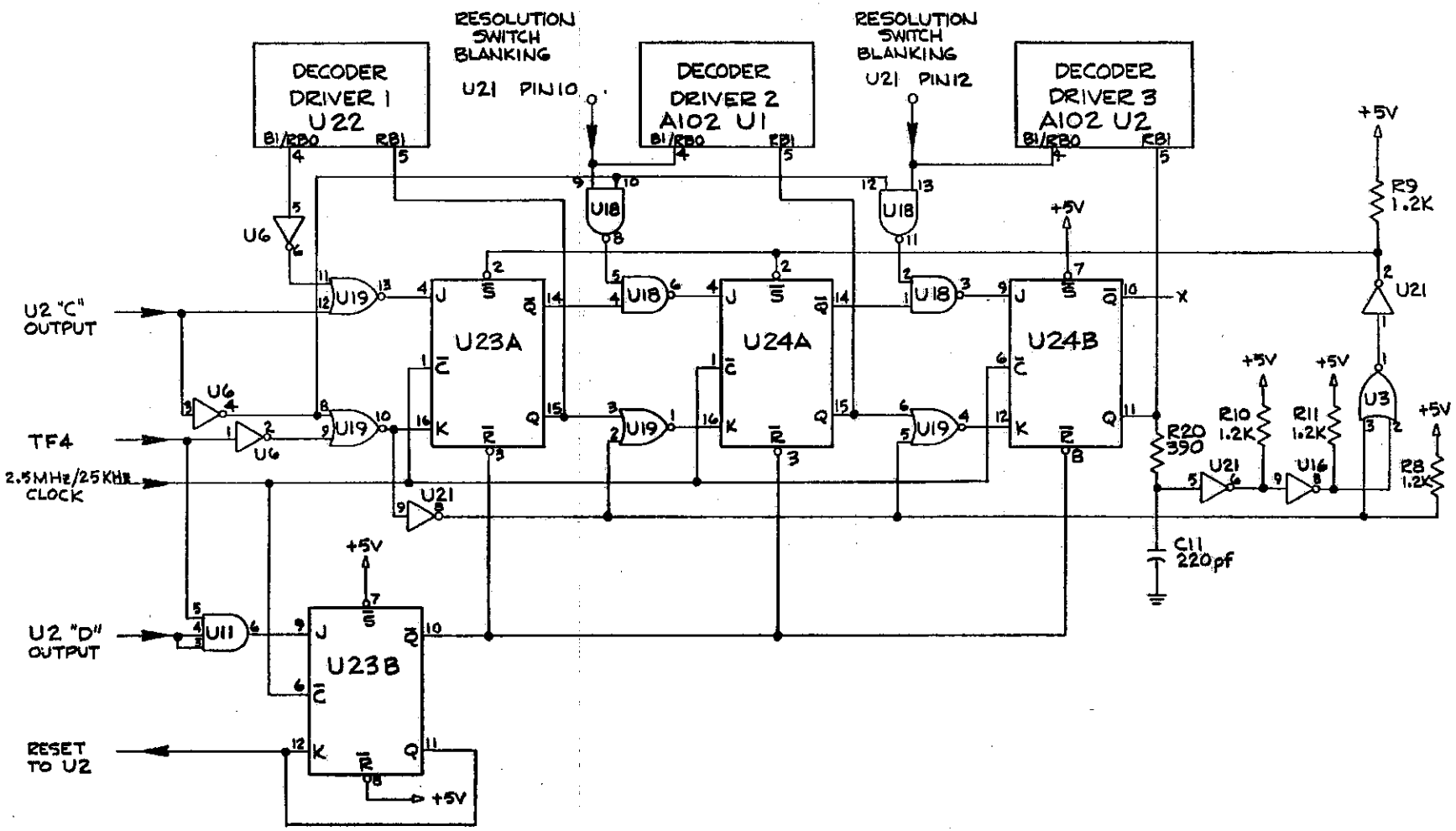
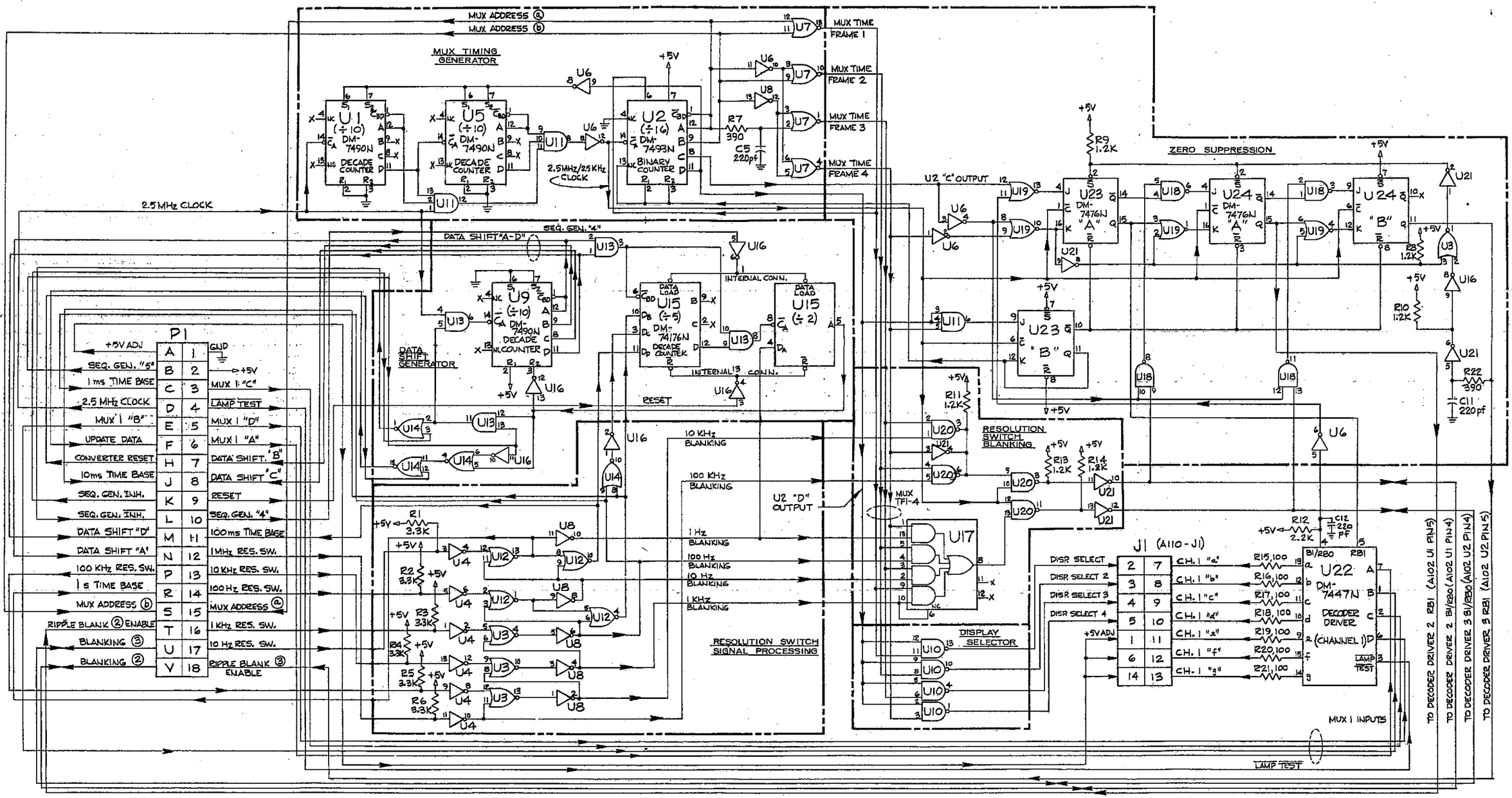
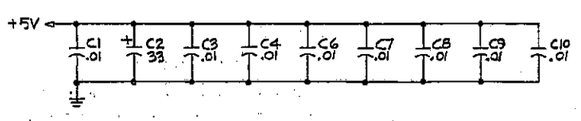


FIGURE 9-3C
PARTIAL SCHEMATIC
LEADING ZERO SUPPRESSION

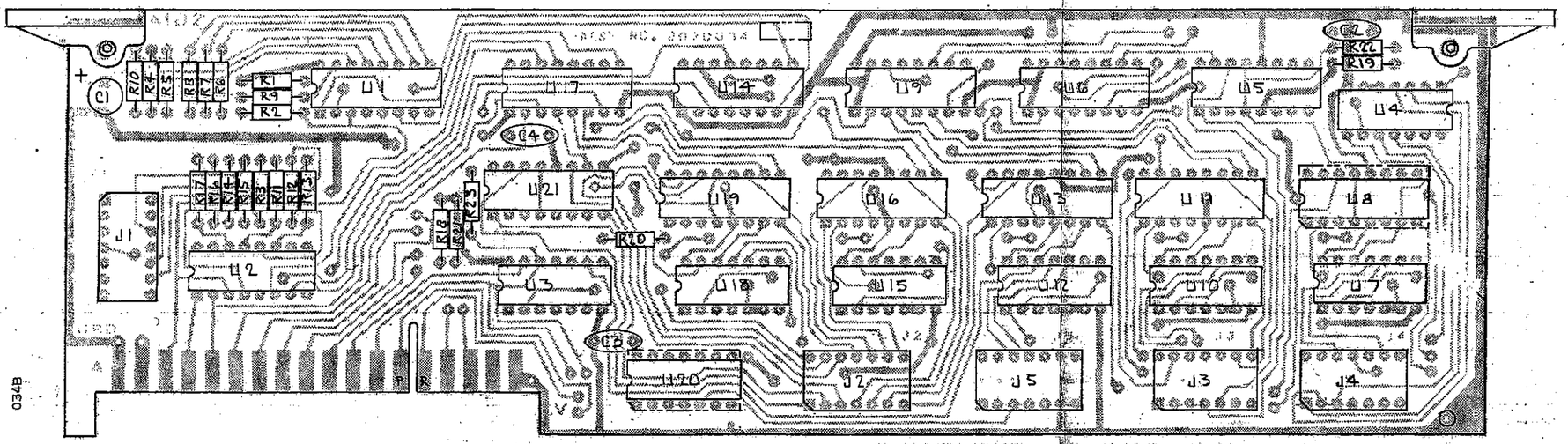




I.C. NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1, U5, U9	DM7490N	10	5
U2	DM7493N	10	5
U3, U7, U12, U14, U19	DM7402N	7	14
U4, U6, U8, U16	DM7404N	7	14
U10	DM7401N	7	14
U11	DM7411N	7	14
U13	DM7408N	7	14
U15	DM74176N	7	14
U17	DM7454N	7	14
U18, U20	DM7400N	7	14
U21	DM7405N	7	14
U22	DM7447N	8	16
U23, U24	DM7476N	13	5

FIGURE 9-3B
SCHEMATIC DIAGRAM
COUNT CHAIN 1 (A101)

036C



COUNT CHAIN 2 (A102)

A102 is similar to A103, being simply a continuation of the counting chain that begins on A103. Six DCUs on A102 (U4, U7, U10, U12, U15, and U18) combine with the five DCUs on A103 for a total of eleven in the counter. Each of these six are presettable. They are programmed by data lines either from the Converter (when it is being used), or from external inputs when IF Offset Option 06 is used.

Each of the six DCUs has an associated quad-latch (U5, U8, U11, U13, U16, and U19) to store the DCU information. An additional latch (U21) stores the information from the last DCU on A103 (U1), which does not have a quad-latch on that board. Two sets of multiplexers (U6 and U9, and U14 and U17) transfer the information from the latches to the display drivers. Two decoder-drivers (U1 and U2) convert the four line BCD information from the two multiplexers into the seven-line code necessary to drive the segments of the front panel display. Separate inputs to these decoders allow the display to be blanked, or to display all eights in the Visual Display Test. (A more detailed description will be found in the paragraphs titled "Leading Zero Suppression Circuity".)

FIGURE 9-4A
COMPONENT LOCATOR
COUNT CHAIN 2 (A102)