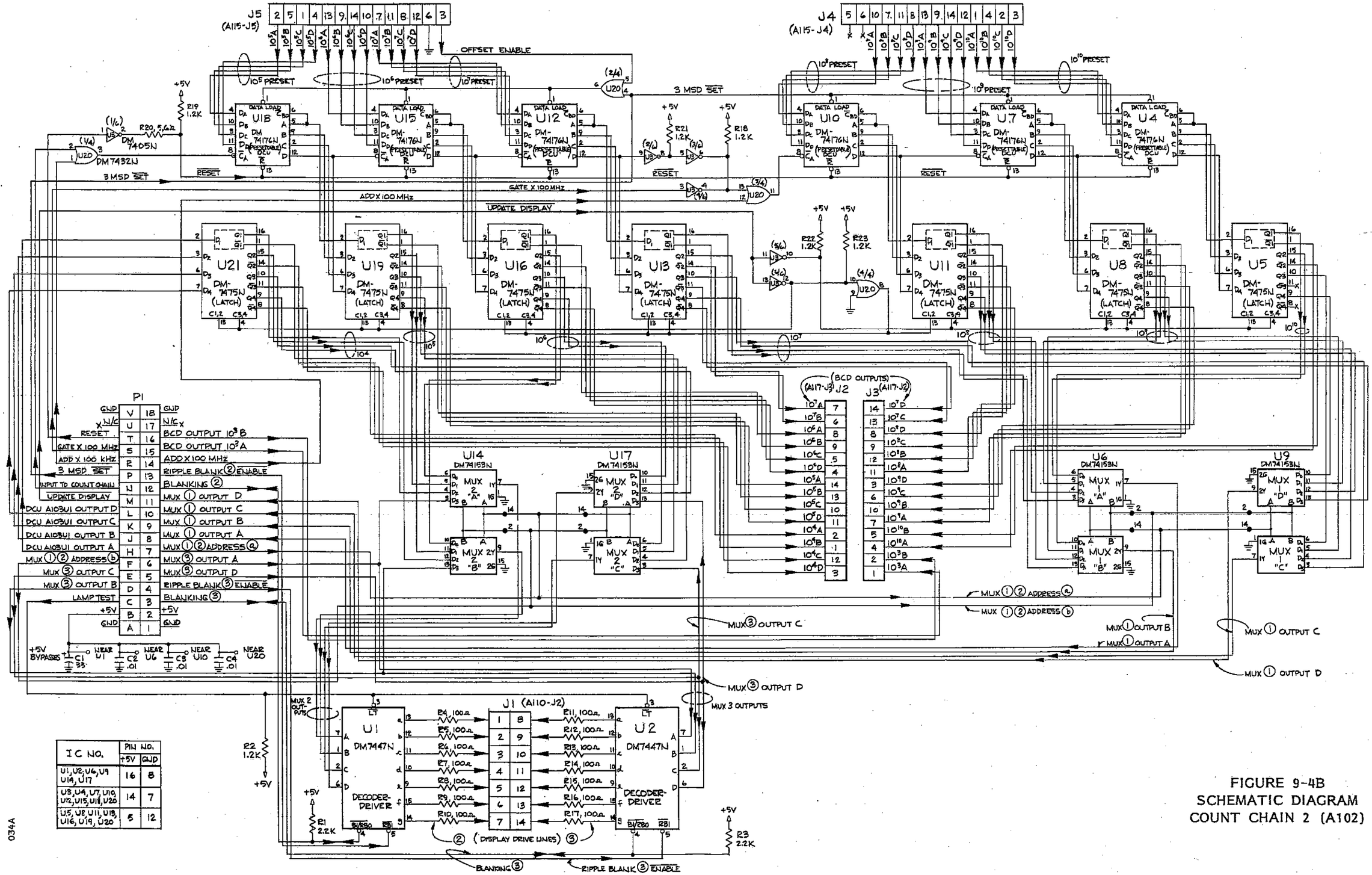
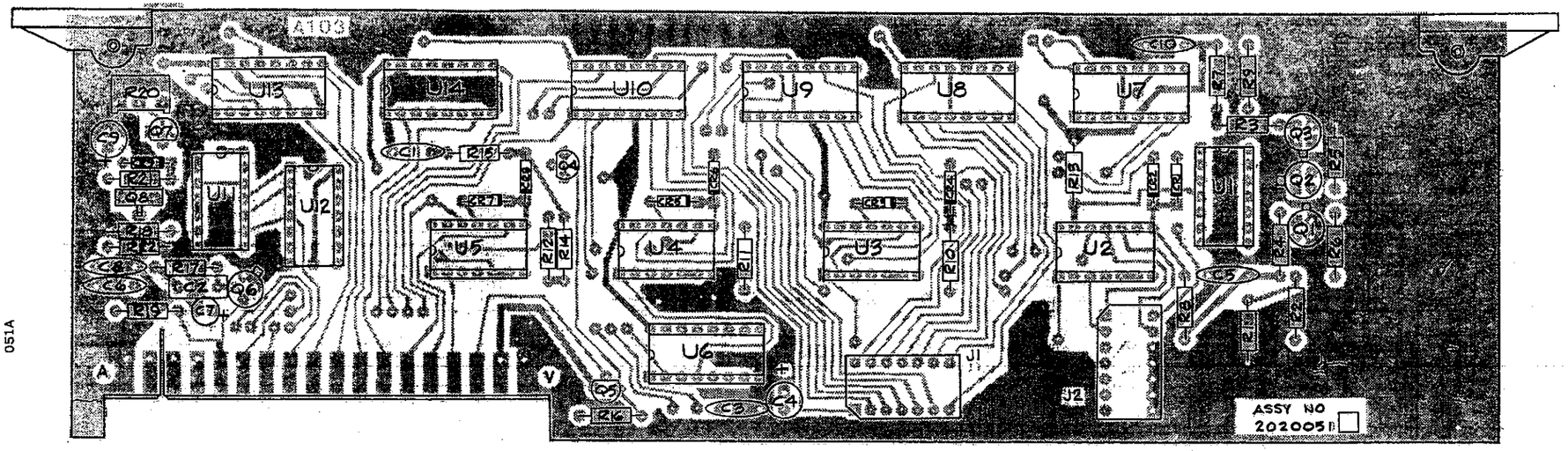


IC NO.	PIN NO.	
	+5V	GND
U1, U2, U6, U9 U14, U17	16	8
U3, U4, U7, U10, U12, U15, U18, U20	14	7
U5, U8, U11, U13, U16, U19, U20	5	12

FIGURE 9-4B
SCHEMATIC DIAGRAM
COUNT CHAIN 2 (A102)



051A

COUNT CHAIN 3 (A103)

A103 receives BCD and carry signals from the High Frequency Board (A106). The carry signal is processed thru one to four decade dividers (U2-U5), with the carry output at P1 pin E sent to the Count Chain 2 Board (A102). Gate width commands from the RESOLUTION switches, control data routing and shifting to place the data in proper position for display. Display data for 1 Hz thru 1 kHz information is stored on this board, with mux commands from the Count Chain 1 Board (A101) controlling the transfer of this data to the front panel display.

Data from the first DCU on A106 enters at J2. The data consists of four TTL logic bits giving the BCD information from the first decade, and a 60% duty cycle ECL logic signal which is the carry output from the first decade.

The ECL carry signal enters the ECL-to-TTL converter on the base of Q1. R1 and R2 provide a 95 ohm termination to -1.4 V (open circuit voltage at J2 pin 3). R5 and R6 provide a reference voltage of -1.5 V at the base of Q2. Q1, Q2, and Q3, form a differential cascode amplifier operating in the over-driven mode as a level translator. R3 prevents the TTL output signal from going negative.

The TTL carry signal enters a cascade of four DCU's (U2-U5). The carry output from A103 can be selected from any one of the four DCU's by a 4-wide, 2-input AND-OR-INVERT gate (U12). The selection of the carry output is determined by the RESOLUTION switches. For 1 second gate times, the output comes from U5; for a 0.1 sec gate time, from U4, etc.

There are four latches on A103 (U7-U10) which contain the information to be displayed by the 1 Hz thru 1 kHz digits. The input to these latches comes from the first four decade dividers: input to U7 comes from the decade divider on the High Frequency Board (A106), input to U8 from A103U2, to U9 from A103U3, and to U10 from A103U4.

When the counter is operated in shorter gate time than one second, the decade dividers contain correspondingly higher digit information. For example: For a 0.1 second gate, the first DCU (on A106) contains the 10 Hz information; for a .01 second gate, 100 Hz information, and for a 1 ms gate, 1 kHz information. In order for this information to be displayed properly, BCD information in the DCU's is shifted to the right before it is transferred to the storage latches. The data shift occurs in sequence from right to left; that is, the data moves from U4 to U5, then from U3 to U4, from U2 to U3, and finally from J2 to U2. This shift sequence is controlled by the four command signals: Data Shift A thru Data Shift D, generated on A101. This series occurs once for 10 Hz resolution (100 ms gate), twice for 100 Hz resolution (10 ms gate), and three times for 1 kHz resolution and above (1 ms gate). During the data shift process, the normal clock inputs to the DCU's must be inhibited. This is accomplished by one third of U11, and the four diode gates (CR1, CR4, CR6, and CR8). These gates are held off during sequence 5 when the data is being shifted.

Reset of the four DCU's is controlled by the counter reset line, and occurs after the data is read into the latches and before the next counter gate period. The inverted BCD information from the latches goes to J1 for use with the BCD Output option.

The non-inverted BCD data from the four latches goes to a 4-by-4 mux consisting of U13 and U14. This data is then sent four bits at a time, to the Count Chain 2 Board (A102), where it is converted into 7-segment display information to drive the front panel LED display. The control signals for the mux switch come from A101 and are comprised of two signals: mux address a, and mux address b. These two signals form a binary code to give four addresses: 0, 1, 2, and 3, as shown in Table 9-5A.

SELECTED INPUT	ADDRESS	
	A	B
0	0	0
1	1	0
2	0	1
3	1	1

TABLE 9-5A
MULTIPLEX ADDRESS

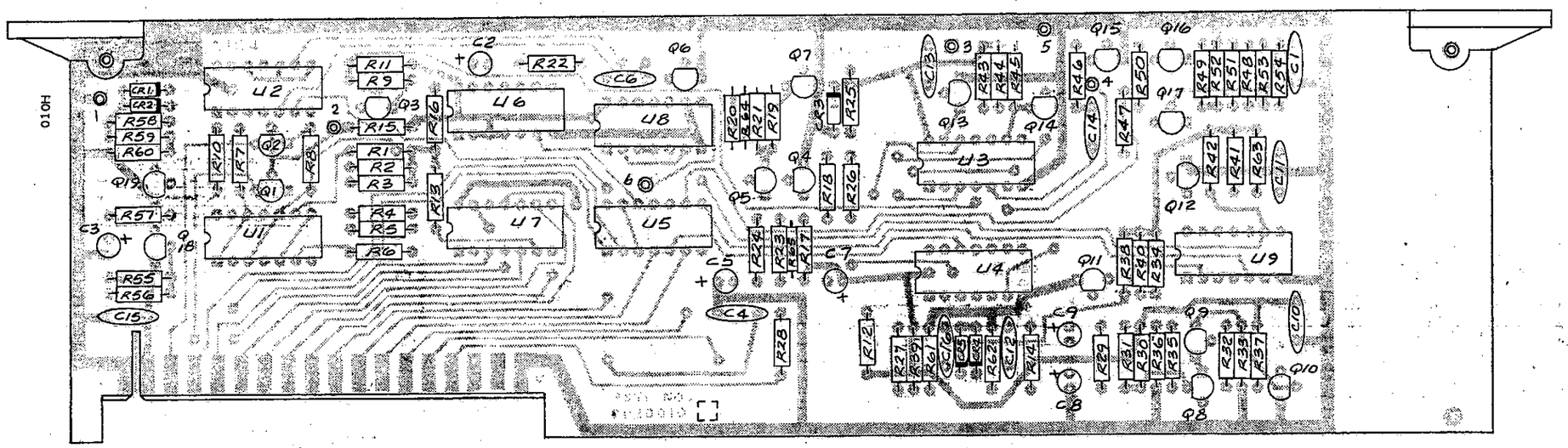
FIGURE 9-5A
COMPONENT LOCATOR
COUNT CHAIN 3 (A103)

NOT USED

U1

I.C. NO	TYPE	GND	+5V
U1	DM7405N	7	14
U2	DM74196N	7	14
U3, U4, U5	DM74176N	7	14
U6	DM7442N	8	16
U7, U8 U9, U10	DM7475N	12	5
U11	DM7427N	7	14
U12	DM7454N	7	14
U13, U14	DM74153N	8	16

FIGURE 9-5B
SCHEMATIC DIAGRAM
COUNT CHAIN 3 (A103)



CONTROL 2 (A104)

This unit accepts commands from the front panel controls, programming inputs and internal control inputs. Front panel controls include RESET, TEST, and BAND SELECT. Internal control inputs to this unit are: SEQUENCE GENERATOR "0", SEQUENCE GENERATOR "5", SEQUENCE GENERATOR "8", PRINT command, and Converter LOCK. The outputs of A104 consist of counter control signals and a front panel SEARCH indicator.

Circuit Description

The three Band Select input lines from P1 pins 6, 7 and 8, each drive an inverter in U1 when one particular line is grounded. The outputs drive the emitters of transistor switches Q1, Q2, and Q3. Their collectors connect directly to the Band Selection inputs on the High Frequency Board, and energize the appropriate input channel amplifier for that band. In Band III, however, the Q3 drive signal is combined with two other inputs via three inverters with open-collector outputs. The three inputs are: the BAND III SELECT (low in Band III), the LOCK signal (low when Converter is locked), and the TEST signal (low except in the TEST mode). The counter must then be in Band III, with the Converter locked and the unit not in the TEST mode for the Band III input to be enabled.

If all the BAND SELECT commands are disabled (as when switching bands), a RESET is generated. This is accomplished by combining the inputs to drive U5 pin 10. This OR gate then drives the RESET trigger U9 pin 5.

Manual Reset and Test inputs come from front panel RESET and TEST switches, and are fed through resistor-capacitor networks to Schmitt triggers composed of Q15, -16, -17, and Q8, -9, -10 respectively. These circuits are used to eliminate the effects of switch contact bounce.

The output of the TEST trigger generates the TEST command for A105, and the TEST signal. These signals are differentiated and fed to the base of Q11, which then triggers the RESET command at both start and finish of the TEST cycle. The TEST signal also drives the bases of Q1-Q3, disabling the input channels of A106 during the TEST cycle. The TEST signal also removes BAND II ENABLE, returning gate time to normal. Finally it combines with the Manual Reset to produce the Visual Display Test function of U7 pin 11.

The Manual Reset also drives the RESET trigger through C11 and Q12. This trigger drives the one shot U8 to produce the RESET pulse.

The CONVERTER RECYCLE command is generated at U7 pin 3, and is generated by either a Manual Reset, a band switching RESET, or after initial instrument turn on. At turn on, the circuit composed of Q4, Q5, and Q6 holds U8 in the triggered state for several seconds. This output sets the Sequence Generator on A105 to "9" and is equivalent to resetting the counter.

In Band III, a LOCK command is received from the Converter when a signal is acquired. This signal generates a Reset through Q14. It is also combined with the Band III SELECT command to drive the SEARCH indicator (U4 pin 8) on the front panel. In the event that the Converter loses LOCK, the one shot U6 is triggered. The output of U6 inhibits the Sequence Generator to allow the Converter to reacquire the signal without displaying zeros on the readout. If a LOCK command is not obtained within the one shot period, a RESET is generated via Q13. If a LOCK signal is reacquired, the delay time is reduced to a few milliseconds by Q18 and Q19.

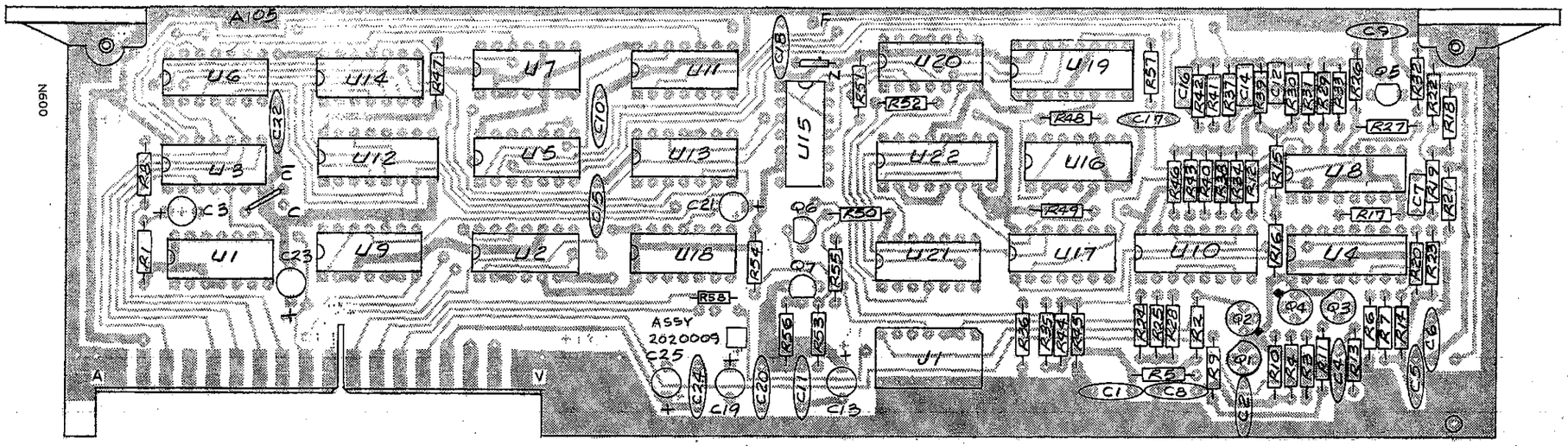
In the event that the Sequence Generator is in the PRINT or memory update portion of the cycle when LOCK is lost, the sequence is allowed to continue to the Display period where it is held. This is accomplished by combining in an OR gate, the PRINT command and SEQUENCE GENERATOR "5", and then combining these with the output of U6 at U5 pin 11. When LOCK is reacquired, the counter is immediately reset.

FIGURE 9-6A
COMPONENT LOCATOR
CONTROL 2 (A104)

TABLE I			
I.C. NO	TYPE	PIN NO.	
		GND	+5V
1,4	DM7404N	7	14
2,9	DM7405N	7	14
3	DM7408N	7	14
5	DM7432N	7	14
6,8	DM8601N	7	14
7	DM7400N	7	14

ALL DIODES ARE P/N: 2704154.

FIGURE 9-6B
SCHEMATIC DIAGRAM
CONTROL 2 (A104)



CONTROL 1 (A105)

This unit contains the circuitry to generate the counter control sequence and the gate time interval. These functions are derived from the 10 MHz Time Base Oscillator.

Clock Generator

Transistors Q1 through Q4 form a Schmitt Trigger to convert the 10 MHz time base signal to a square wave suitable to drive the ECL gates of U4. These outputs are further gated and translated to TTL levels in U8.

Sequence Generator

This circuit produces the main control cycle of the counter by generating a sequence of commands. It consists primarily of an address generator U9, and a decoder U12.

Clocking is performed at a 100 kHz rate by dividing the 10 MHz TTL clock in DCU's U2 and U7. An output of 2.5 MHz is also obtained at U7 pin 12 for the multiplexer clock on Count Chain 1 (A101). The gates of U5 are arranged so that both the 100 kHz and the 2.5 MHz signals are trains of 50 ns wide pulses.

The 100 kHz pulse train drives address generator U9, which produces a four line BCD code. The A and B outputs of U9 address U12, while the C output selects which of the two decoders is active. This generates sequential control signals, one on each of eight lines. Two more signals are obtained using the D output of U9 by itself, or combined with the A output. The gate inputs to U12 (pins 2 and 14) are turned off during switching and when not required, by an OR gate in U13. This eliminates any outputs due to switching transients.

Several internal counter operations inhibit the sequence generator. In addition, Digital Output Option 09, and Remote Programming Option 07, allow the sequence to be externally inhibited.

Gate Generator

The Gate Generator provides the correct gate time interval as required by the front panel RESOLUTION switch settings. The time interval is controlled by selecting an integral number of cycles of the 10 MHz Time Base Oscillator. This then turns the Gate Binary U10 on and off appropriately.

The major element of the Gate Generator is a programmable multi-decade divider, U19. By applying the proper address as shown in Table 9-7B, division ratios from 10^3 to 10^6 can be obtained. A 1 MHz input is then used to generate intervals from 1 ms to 1 second. DCU U16 divides the 10 MHz clock signal to provide the 1 MHz input for U19. The address is obtained by processing the four gate control signals from A101.

For operation in Band II, it is necessary to expand the gate time by a factor of four, since the incoming frequency is divided by four. This is accomplished by disabling Q5. The 2.5 MHz signal from U2 and U7 then appears at U8 pin 15 during the gate time and is combined with the 10 MHz signal to produce a 2.5 MHz pulse train at U17 pin 3. If Q5 is enabled, then the 10 MHz pulse train will appear there.

The Q_B output of U22 is combined in U17 with the 10 MHz clock and the A and D outputs of U16 to produce the Time Base Gate Level at U17 pin 6. This arrangement guarantees that the gate time interval is precisely determined by the 10 MHz signal itself.

It is necessary that the Q_B output be no more than one microsecond duration. The two flip-flops of U22 are interconnected in such a manner as to produce a single one microsecond pulse every time the output of U19 goes low.

Display Time Generator

This generator consists of U18, U15, Q6, Q7 and associated circuitry. Triggering the multivibrator U18 generates a pulse whose width is determined by C21 and the resistance of the front panel SAMPLE RATE potentiometer. Q6 is a current amplifier to increase the available range, while DCU U15 is used to scale the range by a factor of ten. The result is a display time period variable from approximately 60 ms to 40 seconds. U18 is triggered by the SEQUENCE GENERATOR "8" appearing at pin 2. Once turned on, feedback from Q7 to pin 4 holds the unit in its free running state until pin 3 goes low. Pin 3 input is derived from the output of DCU U15. The Display Time Generator output (U3 pin 12) is then used as one of the Sequence Generator Inhibit inputs.

The Display Time cycle begins with SEQUENCE GENERATOR "9" setting U15 (pin 7) to the "9" state which inhibits U18 (pin 3) from triggering. When SEQUENCE GENERATOR "7" begins, U15 is reset (pin 3), thus enabling U18. Period "8" triggers U18 (pin 2) and the Sequence Generator is then held in period "8" until U15 counts to 9, at which time the display period ends.

Application of the front panel HOLD command at U13 pin 8, holds U15 in the reset position so that the Sequence Generator is permanently inhibited in period 8.

To assist troubleshooting of the Sequence Generator, a Cycle Speed jumper is provided. If this jumper is moved from +5 (Normal) to ground (Fast), the R(1) input (U15 pin 2) is brought low, and the Display Generator is inhibited, thus reducing the display time to 10 microseconds.

CONTROL LINE			DIVISION RATIO
2^0	2^1	2^2	
1	1	0	10^3
0	0	1	10^4
1	0	1	10^5
0	1	1	10^6

TABLE 9-7B
PROGRAMMABLE DIVIDER

FIGURE 9-7A
COMPONENT LOCATOR
CONTROL 1 (A105)

PERIOD	FUNCTION	DURATION	LOCATION
9	COUNTER RESET	10 µs	-
0	3 MSD $\overline{\text{SET}}$	10 µs	U12 pin 9
1	OFFSET ENABLE	10 µs	U12 pin 10
2	GATE GENERATOR SET	10 µs	U12 pin 11
3	GATE GENERATOR ENABLE	10 µs	U12 pin 12
4	GATE PERIOD	GATE + 10 µs	U12 pin 7
5	$\overline{\text{DATA UPDATE}}$	10 µs	U3 pin 10
6/7	PRINT	20 µs	U14 pin 6
8	DISPLAY PERIOD	Variable	U9 pin 11

TABLE 9-7A

SEQUENCE GENERATOR COMMANDS

Commands are generated as shown in Table 9-7A. (Period numbering is determined by the output state of U9.) The sequence proceeds as follows:

Period 9: The starting point in the cycle. All counting chain DCU's are reset.

Period 0: In Band III, the YIG/Comb Generator frequency is preset.

Period 1: Used to preset counter in conjunction with Offset Option 06.

Period 2: The Gate Generator is set.

Period 3: The Latch Binary (U10B) is reset, enabling the Gate Binary (U10A). The 10 MHz clock (U8 pin 7) is applied to the Gate Generator.

Period 4: The Gate Generator is enabled and inhibits the Sequence Generator (U13 pin 8) for the duration of the gate time. The incoming signal to the counter is counted during this period.

Period 5: The accumulated data in the counting chain DCU's is loaded into the latches.

Period 6/7: The PRINT command is generated indicating the presence of data on units equipped with Digital Output Option 08.

Period 8: The Display Period. The Display Generator is turned on and inhibits the Sequence Generator during this time. The duration of the period is determined by the front panel SAMPLE RATE control.

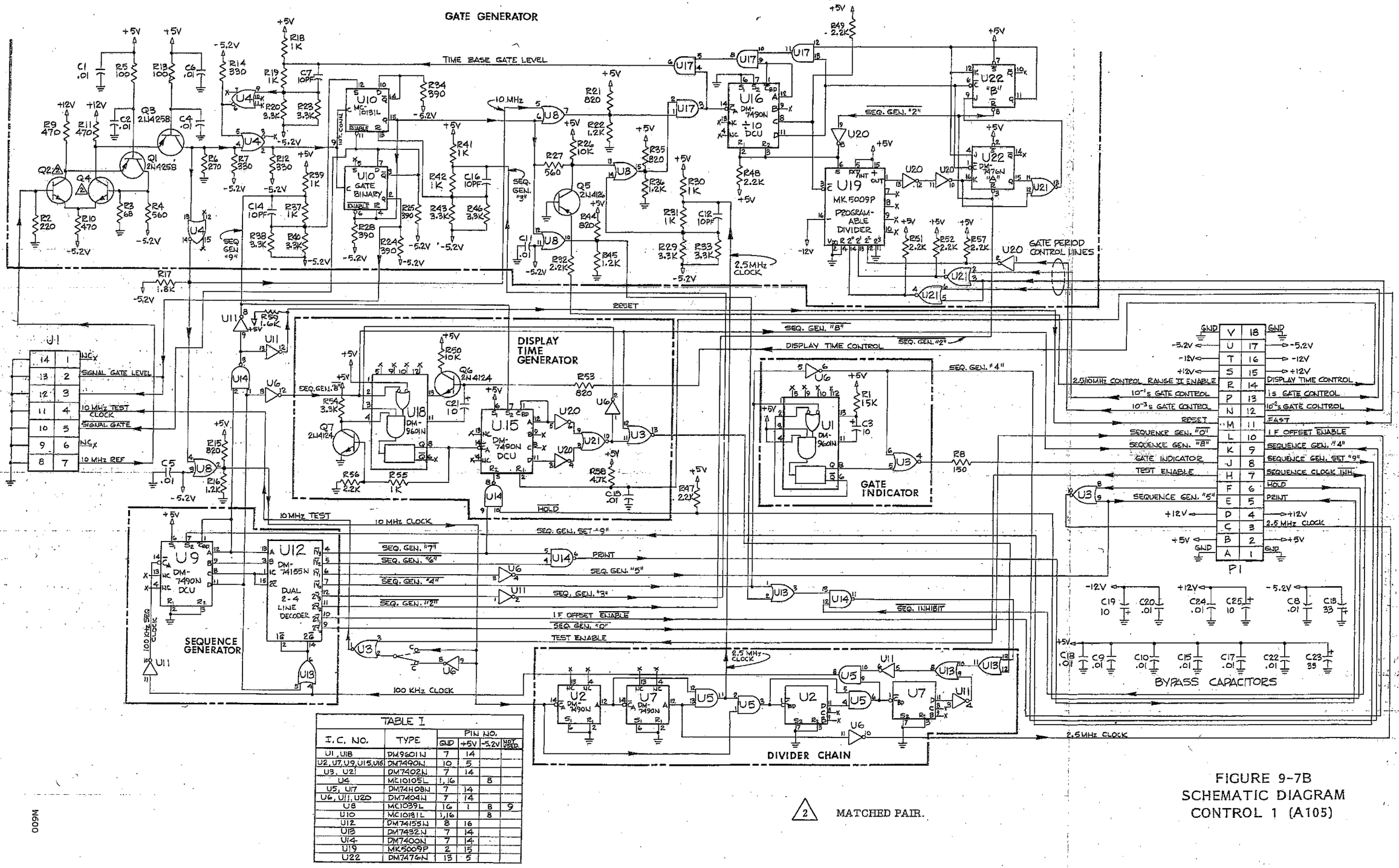
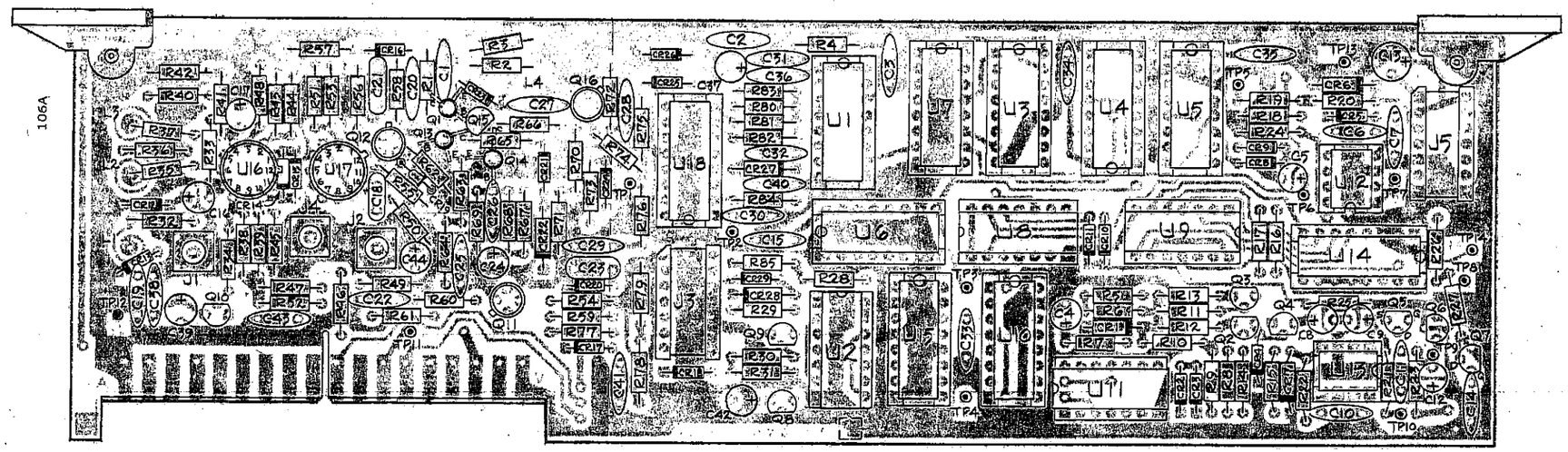


TABLE I					
I.C. NO.	TYPE	PIN NO. GND	+5V	-5.2V	NOT USED
U1, U18	DM9601N	7	14		
U2, U7, U9, U15, U16	DM7490N	10	5		
U3, U21	DM7402N	7	14		
U4	MC10105L	1, 16		8	
U5, U17	DM74H08N	7	14		
U6, U11, U20	DM7404N	7	14		
U8	MC1039L	16	1	8	9
U10	MC10181L	1, 16		8	
U12	DM74155N	8	16		
U13	DM7432N	7	14		
U14	DM7400N	7	14		
U19	MK5009P	2	15		
U22	DM7476N	13	5		

2 MATCHED PAIR.

FIGURE 9-7B
SCHEMATIC DIAGRAM
CONTROL 1 (A105)

M600



HIGH FREQUENCY (A106)

The High Frequency board accepts RF signals from the Preamplifier (A111), Prescaler (A109), Converter (A2), gate and 10 MHz Test signals from Control 1 (A105). Range signals from Control 2 (A104) select the appropriate input which is processed, gated, and counted in the first decade counting unit (DCU). The outputs from A106 are the Carry (f/10) signal, and the first decade of BCD information. These signals go to Count Chain 3 (A103) for further processing.

High Frequency board A106 also provides programming, frequency division, phase comparison, integration, and part of the video signal amplification, for the source locking phase lock loop (PLL). All signals for the PLL portion of A106 enter or leave via J1, which connect to Microprocessor board A122.

Input Selector

A106 accepts three input signals (on J1, J2, and J4), and a 10 MHz Test signal (J3 pin 4). One of the three inputs is selected by a command signal entering on P1 pins 12, 13, or 14. Each command line sits at approximately -12 V until it is selected, at which time it is pulled up to about + 0.7 V. These command signals turn on an appropriate differential amplifier, which selects the input signal to be processed. The signal into each gated amplifier is terminated with a 51 ohm resistor.

If the input to J1 is selected, an additional amplifier stage (U16A) is also turned on by the control signal. This signal is ac-coupled into the preamplifier stage to allow the input to be biased at approximately -6 V. The collectors of U16A are operated against ground to minimize parasitics. L2 and L3 in series with load resistors R35 and R37, are high frequency peaking coils used to flatten the response of the amplifier. R36 is used partly as a damping resistor for L2 and L3, and partly to establish a -2 V level at the output of U16A for direct coupling to U16B. CR14 and CR15 prevent large signals from overloading U16B.

Squaring Circuits

The input selector differentially drives squaring circuit Q12 and Q19. Q12 is a current mirror which is used as a voltage-to-current converter. The current from Q12's collector is used to drive tunnel diode CR19. The action of a tunnel diode under a current driving signal is that of a Schmitt trigger; that is, the voltage across the diode changes abruptly between two states (approximately 0.1 and 0.5 V), and therefore changes a low frequency sine wave into a low frequency square wave, with rise and fall times on the order of half a nanosecond.

The voltage signal across the tunnel diode is used to drive the pulse forming network. The network input is a wide-band high speed differential amplifier (Q13/Q14), to increase the amplitude of the tunnel diode signal, and improve the rise and fall times. The output of Q13/Q14 drives current mirror Q15, used here as a current switch. Essentially, Q15 is either on or off, but the output is the current from the collector, and not a voltage signal. The switched current signal drives differentiator L4. The output of a differentiator with a square wave input is a series of pulses — positive when Q15 turns on, and negative when Q15 turns off. The negative pulses (wider than the positive pulses due to transistor storage time) are removed by CR23. Shorting out the negative pulses also provides a damping effect on L4, improving its response to the positive pulses at high frequencies.

Pulse Inverter

These positive pulses are then coupled to pulse inverter Q7, which has two functions: to invert the pulse, and to deliver the negative output pulses at the right dc reference level for decade divider U18. A temperature compensated stable dc reference is provided by voltage divider R75-77 and CR25-26. The inverter is kept from disturbing this reference by being biased just at cut-off. This is accomplished by developing a forward bias for the transistor from the voltage drop across CR14, whose voltage matches the base-emitter voltage of Q16, keeping Q16 just at the edge of conduction. Basically, Q16 is a pulse amplifier, since it only conducts during a signal pulse. The load resistor for Q16 is the net equivalent of the bias network R75-77.

Q16 output drives the input of decade divider U18. The divide-by-ten output of U16 is a 60/40% duty cycle ECL level signal, and is called the "DCU CARRY" signal (J3 pin 3); the load resistor for this signal is on A103.

The gate signal to the DCU is an inverted ECL signal. It enters on J3 pin 5, and goes directly to U18 pin 16. The BCD output information is available at J3 pins 1, 2, 13, and 14. During a count cycle at high frequencies, this information is slew rate limited, and actual output level cannot be seen until the circuit comes to rest. After the circuit is finished counting, TTL level signals are present at these outputs. U18 is reset after the counting cycle is complete by a TTL reset signal at pin 3.

Phase Lock Loop

The PLL generates a 50 kHz reference signal by dividing the counter's 10 MHz time base in the reference divider (U2B, U15A/B, Q8, Q9). The incoming 10 MHz signal is converted to a TTL signal by Q8 and Q9. The signal is then divided by two in U2, by ten in U15A, and by ten in in U15B, resulting in a total division of 200. The 50 kHz reference retains the same stability as the time base oscillator (A108). This reference signal is applied to phase detector U11 through phase reversing switch U10.

The second input to the phase detector circuitry comes from the frequency divider chain. The divider chain takes the IF frequency and divides it by the number programmed into it by frequency program registers U8 and U9. With the exception of two bits, the program number consists of four 4-bit numbers (in standard positive logic format), which correspond to the IF lock frequency.

The numbers are programmed serially into U8 and U9, with the parallel outputs programming the frequency divider chain (U3-U6) sequentially from the least significant digit to the most significant digit. Since the counter can never be programmed above 319.9 MHz, only two bits are required to program U5 (pins 5 and 11); the other two bits (pins 2 and 14) are hard-wired low. The two remaining bits from U9 are used for other programming functions: one bit (pin 10) is used to control the reversing of the reference and divided IF signals to change the polarity of the video signal; the other bit (pin 11) goes through J4 pin 1 to the Microprocessor board (A122) to select the narrow bandwidth mode of locking. (These last two functions, generated by the microprocessor on A122, have no correlation to the frequency being programmed.)

Phase Detector

The phase detector compares the phase of the two incoming signals by measuring the time difference between their leading edges. The output of phase comparator U11 consists of negative voltage pulses from pin 2 or pin 13, with the width of the pulses proportional to the phase error between the two signals. The advantage of this type of detector is significant when the two signals being compared are not the same frequency. When this occurs, the error pulses lengthen into a nearly dc signal, and the phase detector becomes a frequency comparator, indicating whether the divided signal is above or below the reference frequency. The only condition under which this type of phase detector can lock up, is when the two incoming frequencies are identical.

FIGURE 9-8A
COMPONENT LOCATOR
HIGH FREQUENCY (A106)

Charge Pump

The remaining part of the phase detector circuitry (Q2 - Q4) is called the charge pump. This circuitry takes the voltage pulses from the phase comparator and converts them to current pulses. Q3 takes the negative voltage pulse from U11 (pin 13), and converts it to a 4.6 mA collector current pulse, at about the same width as the voltage pulse from U11. Q2 is an inverter which drives Q4, generating a 4.6 mA current pulse of opposite polarity to that of Q3. The current output pulses "pump" the charge across C8 and C9 in the loop filter up and down, to correct for the phase error between the two frequencies entering the phase comparator.

Loop Filter

The loop filter (Q5, Q6) is an integrating type, which has a dc gain equal to the open loop gain of amplifier U13. The gain of U13 decreases as a function of frequency, until the impedance of C8 and C9 is less than R21. Above this frequency, the output is equal to the input current times the value of R21. Since this is an integrating filter, capacitors C8 and C9 store a charge. At times during the lock up procedure, it becomes desirable to "dump" this charge. Q5 is held at cut-off by -12 volts applied to its gate. When current flows into Q6's emitter, Q6 saturates, and its collector and the gate of Q5, go to +0.2 volts. This turns on Q5, and dumps the charge on C8 and C9.

The output of the loop filter drives the loop amplifier, consisting of a DAC (U14) and an op amp (U12A). The DAC is a CMOS switching type that is used as a digital gain control. The gain in Bands IA, IB, and III, from TP10 to TP7, can be calculated from the equation: Frequency in MHz, divided by 70.

In Band II, the divide-by-four Prescaler requires that the gain of the loop amplifier be multiplied by four. This is accomplished by the Band II command signal turning on Q7, which switches R27 into the circuit. R27 essentially bypasses 3/4 of the feedback current, resulting in an increased stage gain of four. The output of U12A goes to A121 for further processing before being used to control the frequency of the source being phase locked.