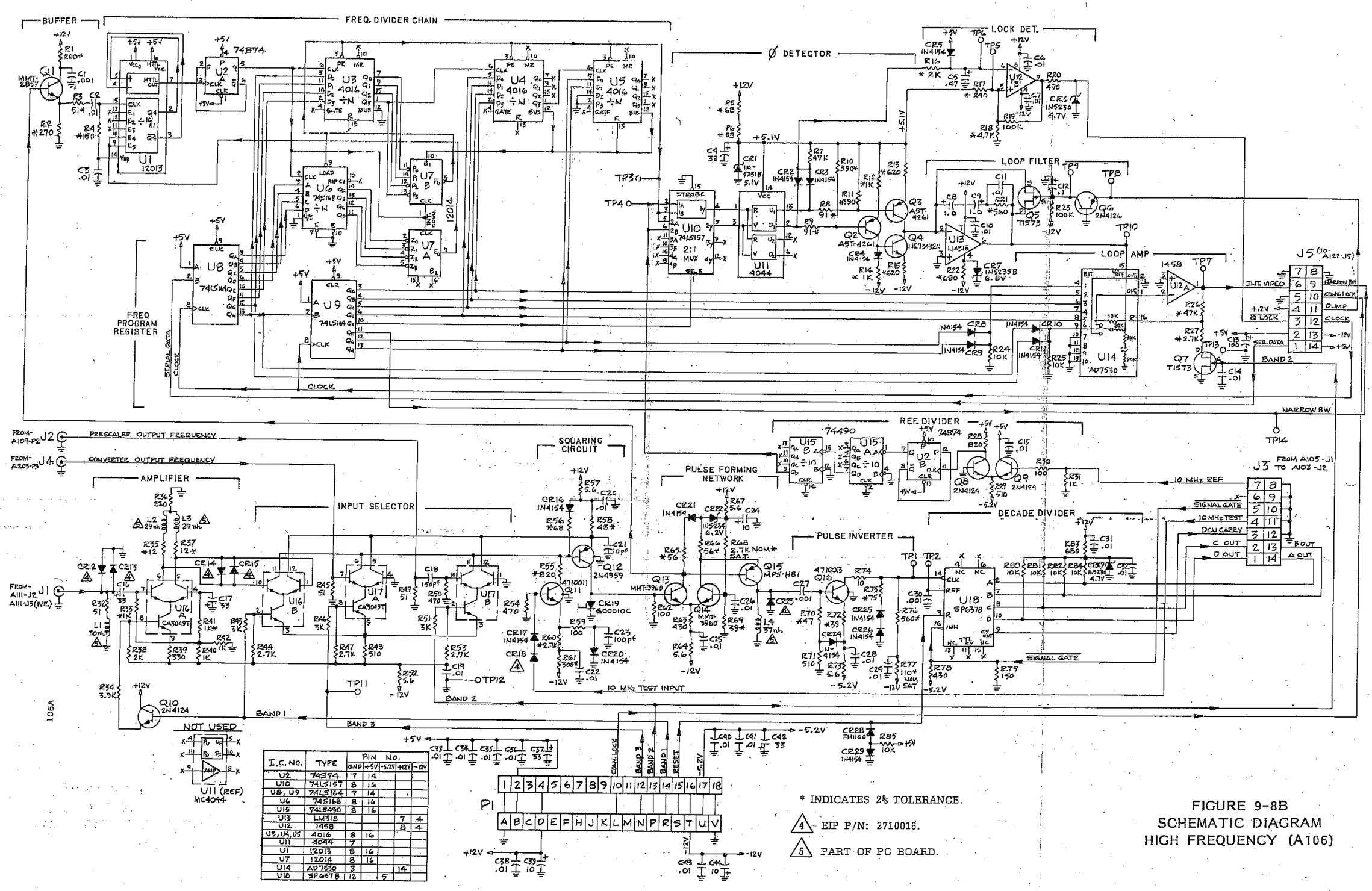
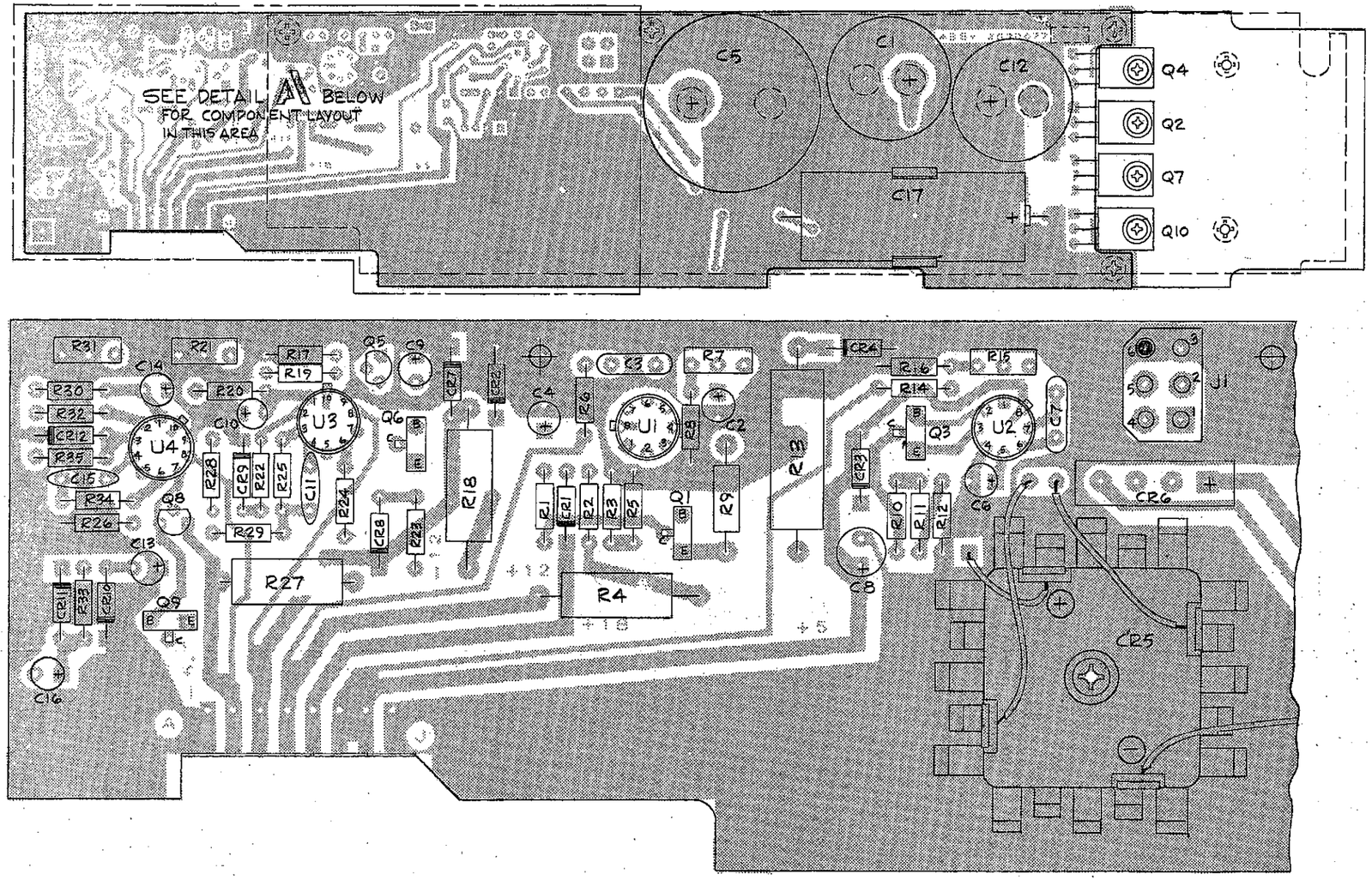


I.C. NO.	TYPE	PIN NO. GND	+5V	-5.2V	+12V	-12V
U2	74S74	7	14			
U10	74LS157	8	16			
U8, U9	74LS164	7	14			
U6	74S168	8	16			
U15	74LS490	8	16			
U13	LM318				7	4
U12	1458				8	4
U3, U4, U5	4016	8	16			
U11	4044	7				
U1	12013	8	16			
U7	12014	8	16			
U14	AD7530	3			14	
U18	SP6378	12		5		

FIGURE 9-8B
SCHEMATIC DIAGRAM
HIGH FREQUENCY (A106)



DETAIL A

FIGURE 9-9A
COMPONENT LOCATOR
POWER SUPPLY (A107)

POWER SUPPLY (A1/A107)

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two assembly groups:

(1) PC Board A107 contains the rectifiers, filter capacitors, and regulator circuitry.

(2) Chassis mounted components (A1-) consist of the power transformer (T1), primary wiring, fuse (F1), 115/230 power switch (S102), and the front panel POWER On/Off switch (S101).

Circuit Description

The basic voltages that are required by the counter are: unregulated +18 V, regulated +12 V, -12 V, +5 V and -5.2 V.

All the regulated voltages are produced by full wave rectifier and series regulator circuits. The +18 V unregulated voltage is also the input voltage for the +12 V regulator.

Each of the four regulator circuits contains an integrated circuit voltage regulator with current foldback capability, protective diodes, and provision for adjustment of the required output voltage.

The type of IC used in both the +12 V and +5 V regulators is an LM305. This IC contains an internal temperature compensated voltage reference, as well as the necessary circuits to provide gain and current foldback limiting. The foldback current limit control resistors in the +5 V supply (for example) are R11, R12, and R13.

The negative supplies utilize an LM304 as the basic IC regulator. This IC also contains an internal temperature compensated reference. To implement this reference an external pre-regulator is required. In the -12 V circuit (for example), the pre-regulator includes R22, R25, and CR9. Current foldback limiting uses internal IC circuitry in addition to R17, R18, R19 and Q5.

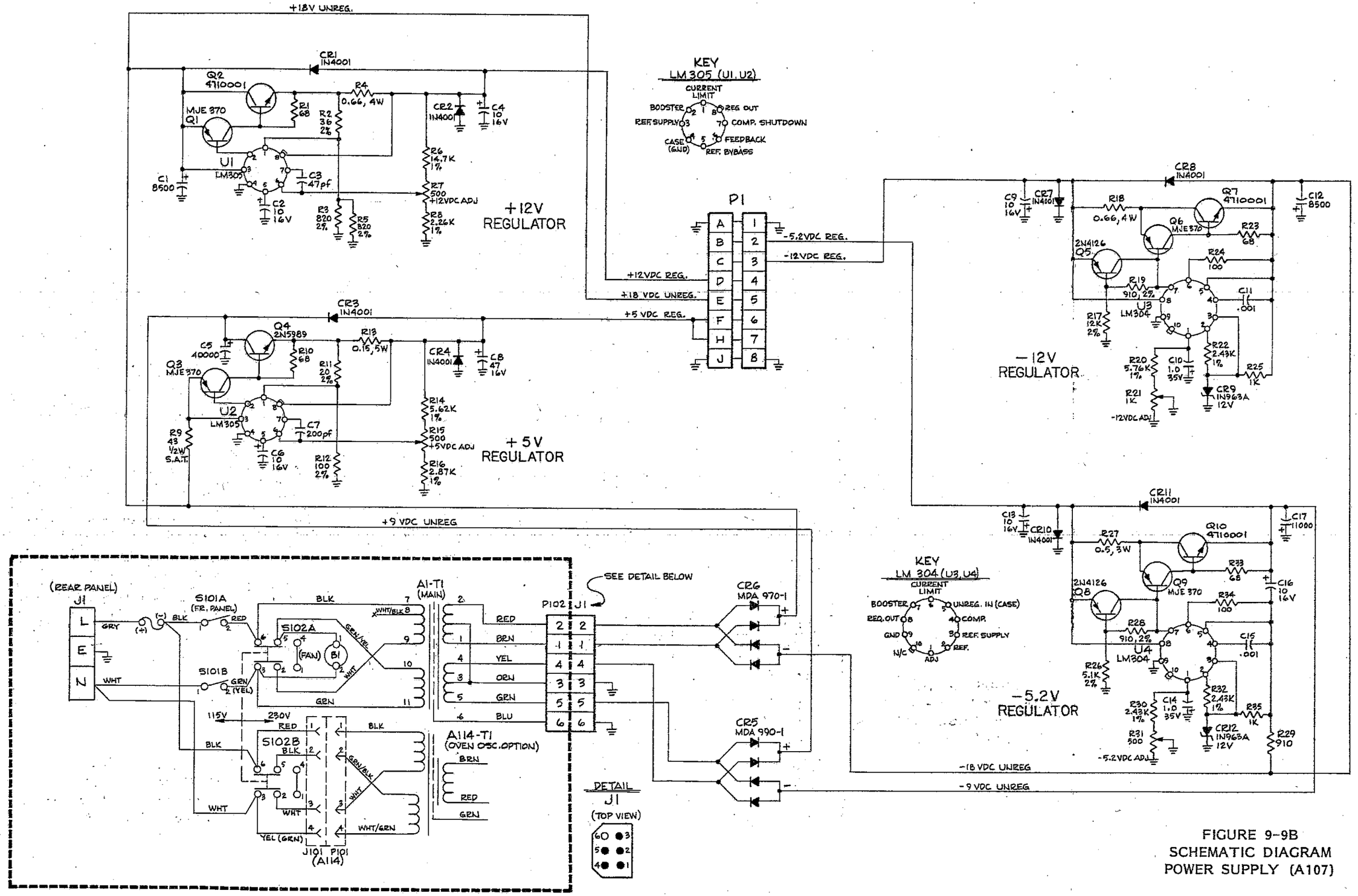
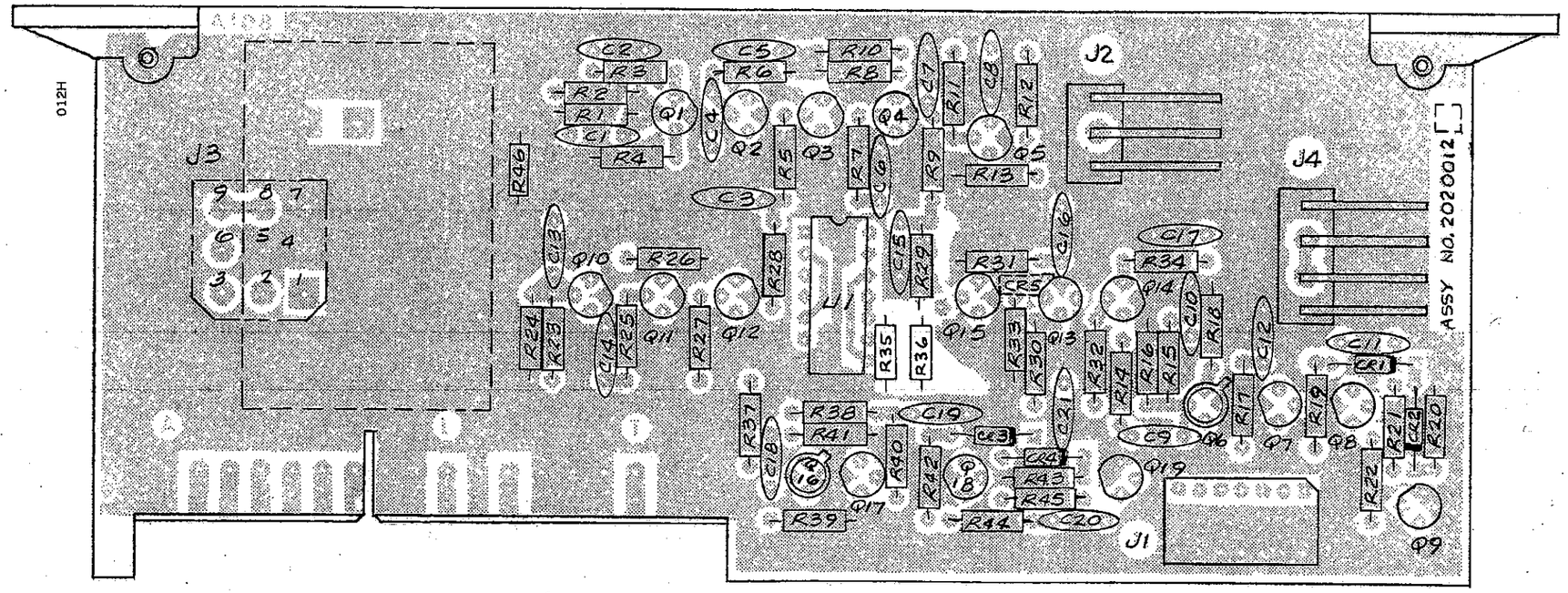


FIGURE 9-9B
SCHEMATIC DIAGRAM
POWER SUPPLY (A107)



REFERENCE OSCILLATOR BUFFER (A108)

An internal temperature-compensated crystal oscillator — TCXO (A116), is used as the basic reference against which all input signals are compared. Additional time base options are available (see Section O - Options), which allow the user to select a level of precision compatible with measurement requirements. Specifications of the TCXO are listed in Section 3.

The counter may be operated from either the internal time base oscillator (TCXO or oven option), or from an external time base reference generator. Internal or external selection is made by means of a rear panel switch (A1S103). A rear panel BNC connector (A1J4) connects to A108J2 to furnish a 10 MHz square wave output signal, or accept a 10 MHz sine or square wave input signal (1 to 3 V p-p into 300 ohms). The method of switching between internal and external oscillators is shown in the Functional Diagram of Figure 9-10C. The power to the TCXO is switched on and off with the main counter power supply, while the power to any of the oven oscillator options remains on as long as the counter is plugged into an active power line, irrespective of the setting of the POWER On/Off switch.

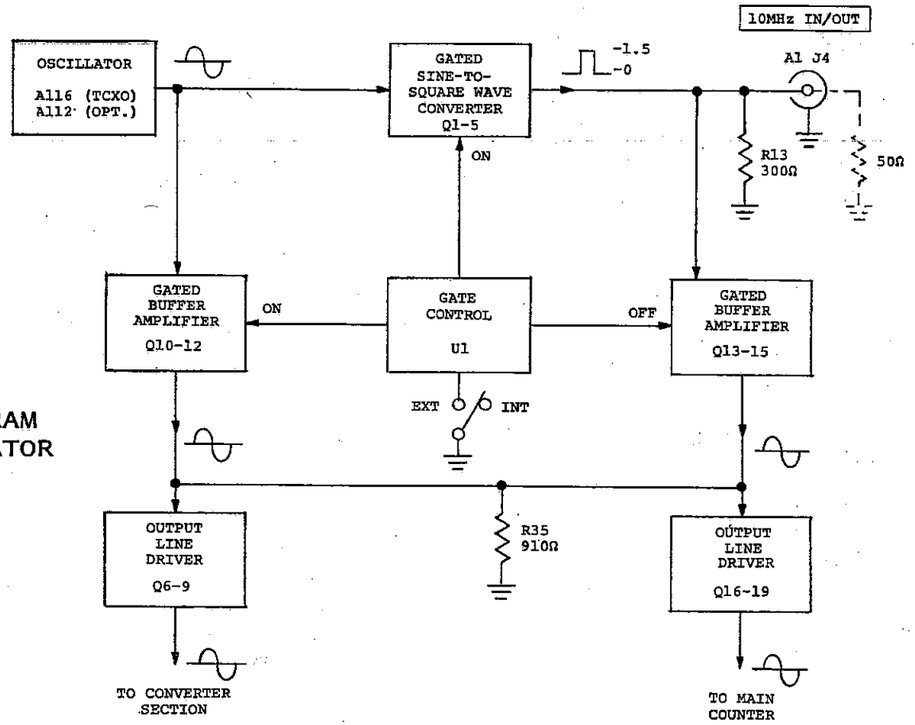
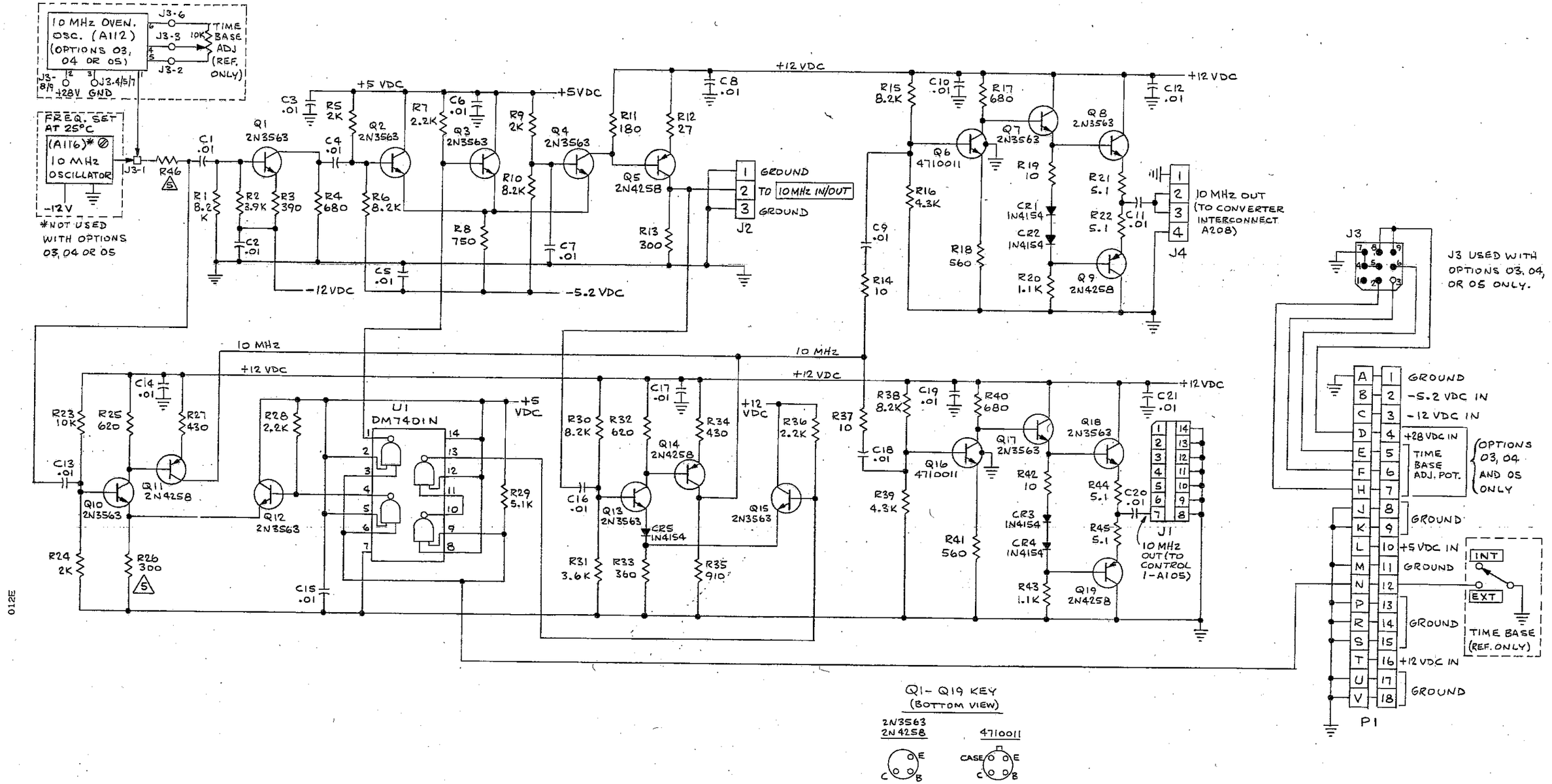


FIGURE 9-10C
FUNCTIONAL DIAGRAM
REFERENCE OSCILLATOR
BUFFER

Circuit Description

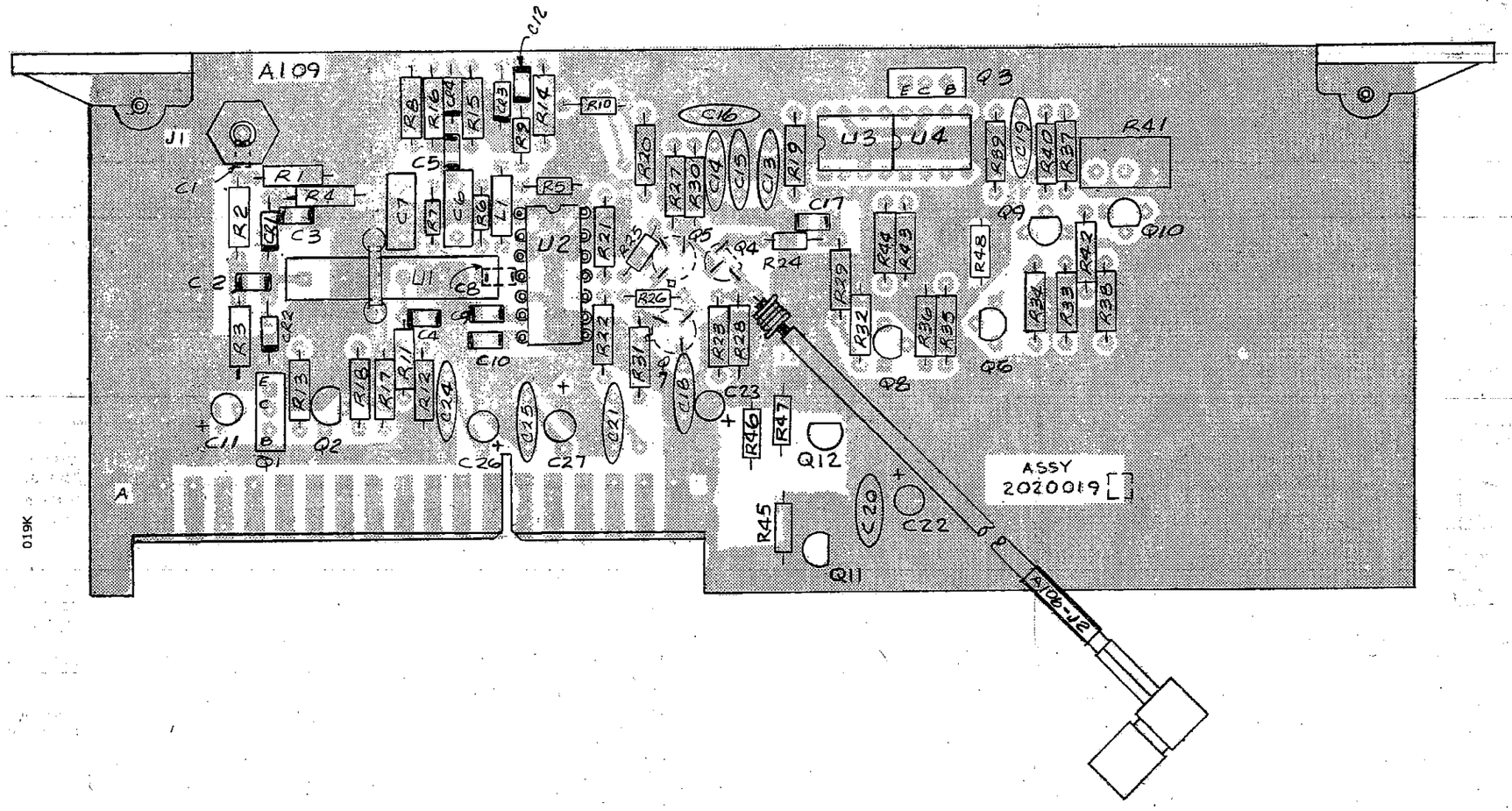
The TCXO sine wave is gated and converted to a TTL level in the circuit consisting of: a linear, low-gain isolation amplifier Q1; a differential sine-to-square wave amplifier Q2 and Q4; and an output current driver Q5. The gate function is accomplished by switching Q3 on and off through U1. Transistors Q10 - Q12, and Q13 - Q15, are identical sets of gated buffer amplifiers. Buffered gain is obtained in each set by the low-gain NPN/PNP pairs Q10/Q11, and Q13/Q14. The gating function is performed by switching Q12 and Q15 on and off through U1. Q6 -Q9, and Q16 - Q19, are identical sets of output line drivers. Low-gain, common emitter input stages Q6 and Q16 are followed by emitter followers Q7 and Q17, which drive push-pull emitter follower output pairs Q8/Q9, and Q18/Q19.

FIGURE 9-10A
COMPONENT LOCATOR
REFERENCE OSCILLATOR
BUFFER (A108 + A116)



5 VALUE SELECTED AT TEST. PART MAY NOT BE USED.

FIGURE 9-10B
SCHEMATIC DIAGRAM
REFERENCE OSCILLATOR
BUFFER (A108 + A116)



PRESCALER (A109)

This assembly permits the measurement of frequencies in the range of 100 MHz to 850 MHz, dividing the input frequency by a factor of four prior to counting. The counter then counts this scaled frequency with a gate time which has been expanded by four, thus yielding a direct frequency readout.

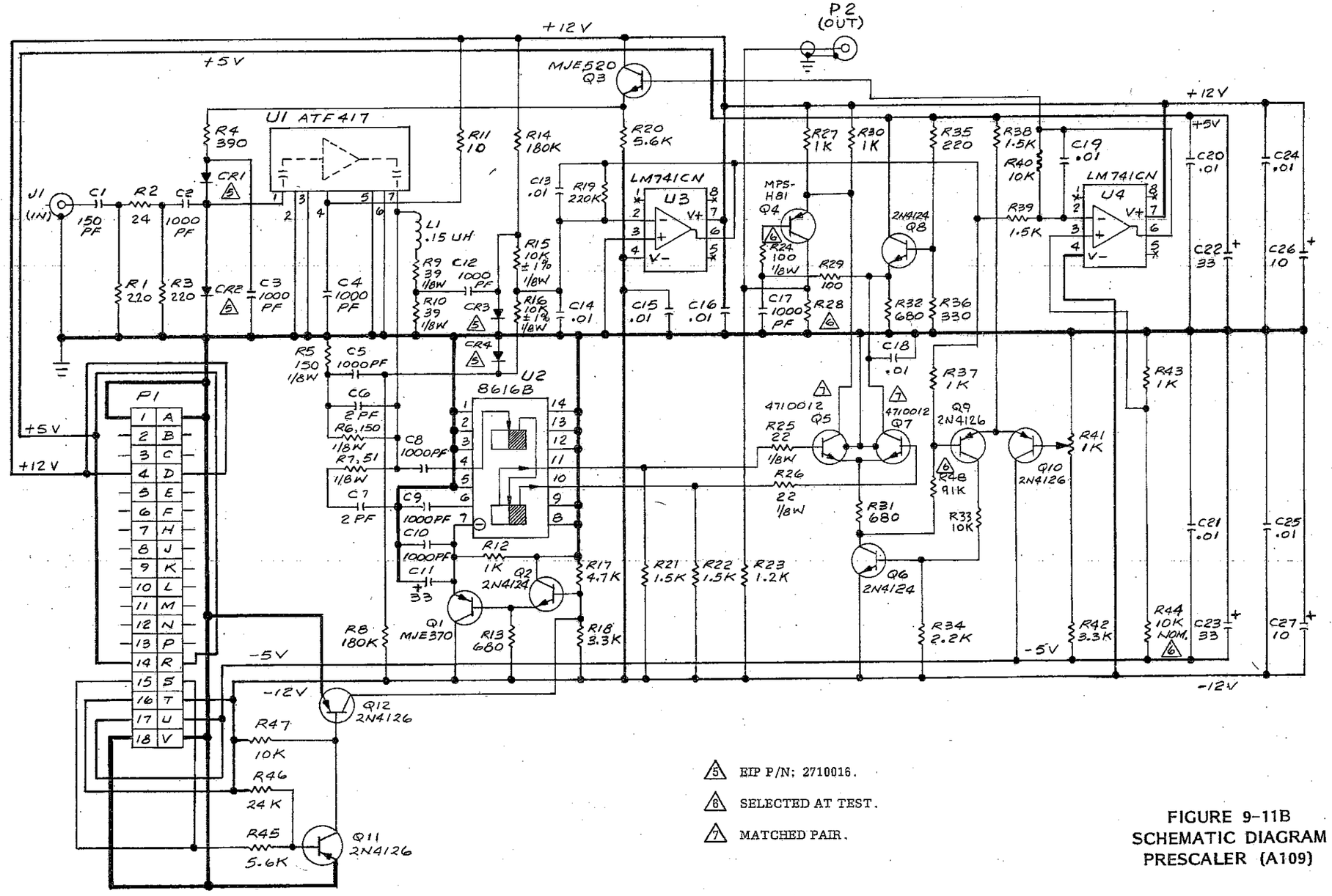
The major element of A109 is a ÷4 integrated circuit (U2). Sufficient drive level for this IC is provided by an integrated broad band amplifier U1. The output of U2 is amplified by the circuit consisting of Q4 through Q8.

Due to the tendency of U2 to free run with no input signal, it is necessary to disable the output if an input signal of sufficient amplitude is not present. This is accomplished with a threshold circuit consisting of a detector (CR3, CR4 and associated components), amplifier (U3), and differential trigger (Q9 and Q10). When the amplifier output applied to the base of Q9 exceeds the threshold level set by R41, Q9 turns on Q6 and thus enables the output amplifier.

In order to prevent U1 from overloading, automatic gain control is provided by comparing the amplified detector output to a preset level in U4 and feeding the output level back via Q3 to a pair of diodes CR1 and CR2. These diodes, when conducting, act to attenuate the input signal.

Transistors Q1 and Q2 form a -7 volt power source for U2.

FIGURE 9-11A
COMPONENT LOCATOR
PRESCALER (A109)



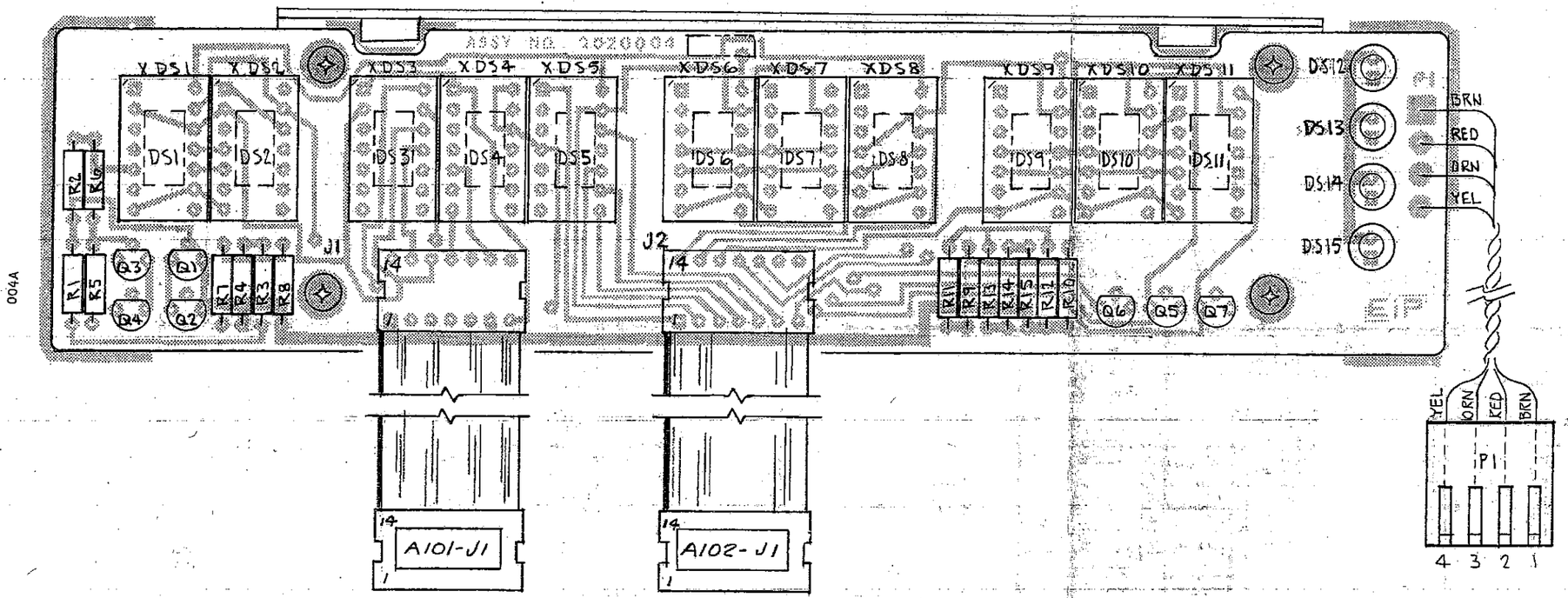
H610

△5 EIP P/N; 2710016.

△6 SELECTED AT TEST.

△7 MATCHED PAIR.

FIGURE 9-11B
SCHEMATIC DIAGRAM
PRESCALER (A109)



DISPLAY (A110)

The Display Board (A110) contains eleven LED numerical display units mounted side-by-side, with spaces between each third digit from the right. The entire assembly is mounted behind a front panel window with the digits grouped to distinctly show GHz, MHz, kHz, and Hz. All drive signals for the Display are obtained from the Count Chain Boards (A101 and A102).

The digit displays are 7-segment LED's, with the anodes of each segment tied together. When the anode is at a positive voltage, grounding any cathode through its resistor illuminates that segment.

In this multiplexed system, the anode supply is applied in pulses (through anode drivers), which are synchronized with the cathode data to determine which segment shall light.

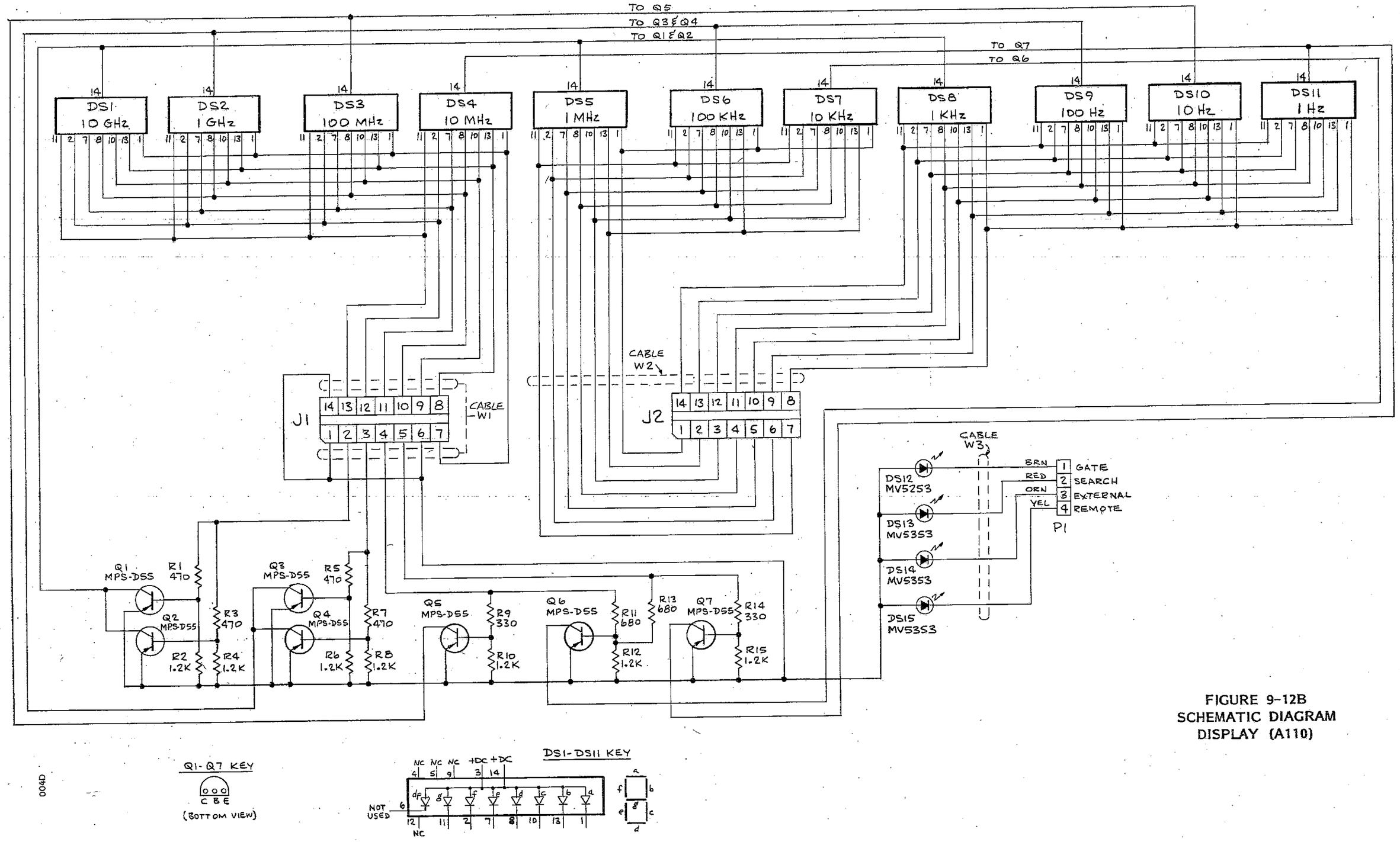
The segment drive is applied directly to the display digits. DS1-4, DS5-7, and DS8-11 have their corresponding cathode segments tied together within each group.

The selector drive to groups DS1, -5, -8, and DS2, -6, -9, are each driven by two transistors in parallel to meet the higher current requirements.

The remaining LED's use single transistor drivers. The drivers saturate when turned on, applying a voltage almost equal to the supply voltage for the display. This voltage is variable (by A103R22) for display brightness adjustment.

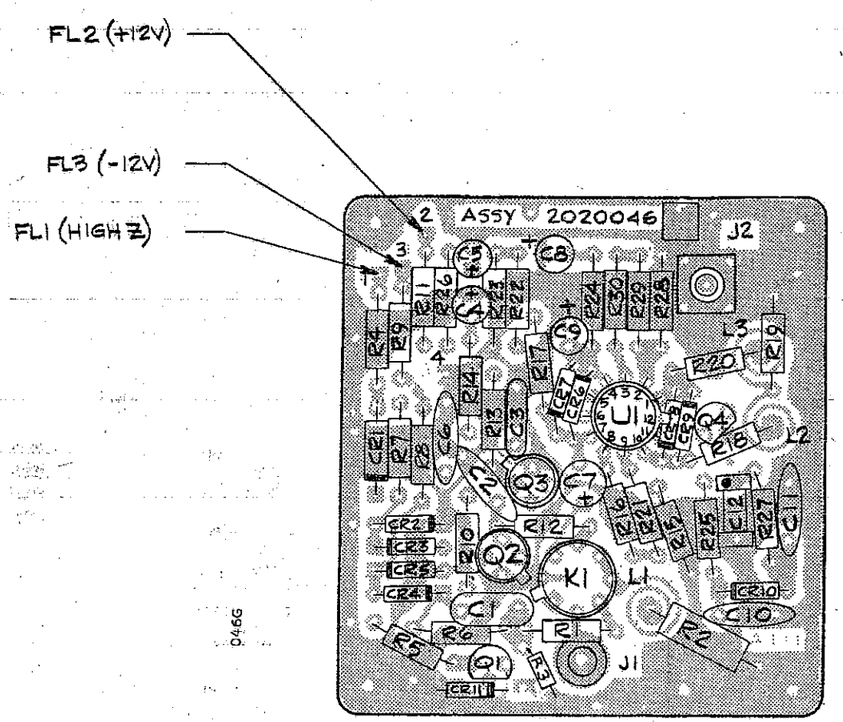
Four display lamps are included on this assembly, which illuminate to indicate GATE operation, Converter SEARCH, EXTernal REFerence, and REMOTE operation (Option 07).

FIGURE 9-12A
COMPONENT LOCATOR
DISPLAY (A110)



004D

FIGURE 9-12B
SCHEMATIC DIAGRAM
DISPLAY (A110)



PREAMPLIFIER (A111)

The Preamplifier accepts Band I input signals at J1. The BAND SELECT switch controls relay K1 which selects either the Band IA high impedance (1 meg/20 pf) circuitry, or the Band IB low impedance (50 ohm) circuitry. The output of the Preamplifier (at J2) drives the High Frequency Board (A106).

When K1 is de-energized, the amplifier operates in the 50 ohm mode. The terminating impedance is the parallel product of a 51 ohm resistor (R2) in series with a small inductance (L1), and the input impedance of the first amplifier stage (U1A). This combination keeps input VSWR below 1.5:1 up to 400 MHz. The signal is ac-coupled thru C7 to amplifier U1A, which is biased at approximately -6 Vdc. The collectors of U1A are operated against ground to minimize parasitic problems. Inductors L2 and L3 in series with load resistors R18 and R20, are high frequency peaking coils to flatten the response of the amplifier. R19 is used primarily to establish a dc voltage sufficiently negative to allow direct coupling to the second stage (U1B).

The output of the second stage is also operated against a ground reference. U1B pin 11 output is fed into current mirror Q4, whose output is then summed with the current of U1B pin 12, at J2. In this way, the two currents cancel, and only a small error component is left to generate an off-offset at the load.

When K1 is energized, the amplifier operates in the high impedance mode, with the relay routing the input signal to the impedance converter. The input impedance of the converter is essentially R3 in parallel with a network of components, and the gate of FET Q2. The net impedance of this combination is 1 megohm shunted by about 20 pf. The signal enters the gate of Q2 through diodes CR3 and CR4, which provide protective limiting for Q2. The limiter diodes are back-biased at about 0.7 V by networks R7/CR2 and R8/CR5. This back-biasing improves the frequency response by reducing the capacitance of CR3/CR4. The limiter is adequate to protect against an accidental connection of a 115 V, 60 Hz power line to the input, however, due to frequency compensating capacitor C1, this high voltage tolerance decreases as the frequency increases (see Specifications).

Q2 operates as a source follower to transform the impedance down to several hundred ohms. Q3 is a buffer amplifier with a gain of about 1.5; its purpose is to match the output of Q2 to the input of amplifier U1A, and to recover the loss of Q2 gain. The net gain through the Preamplifier is approximately equal for both high and low impedance inputs.

FIGURE 9-13A
COMPONENT LOCATOR
PREAMPLIFIER (A111)