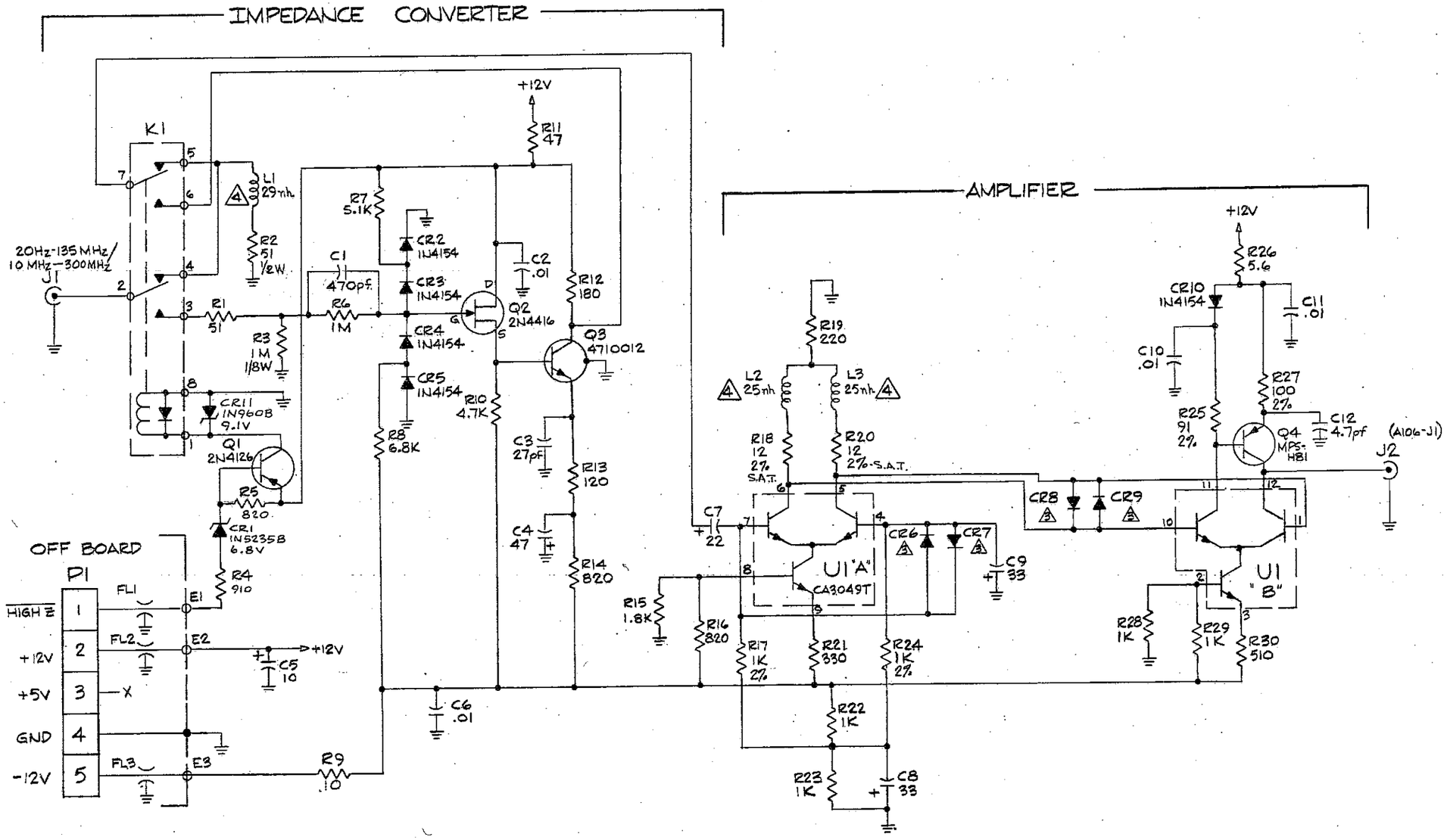
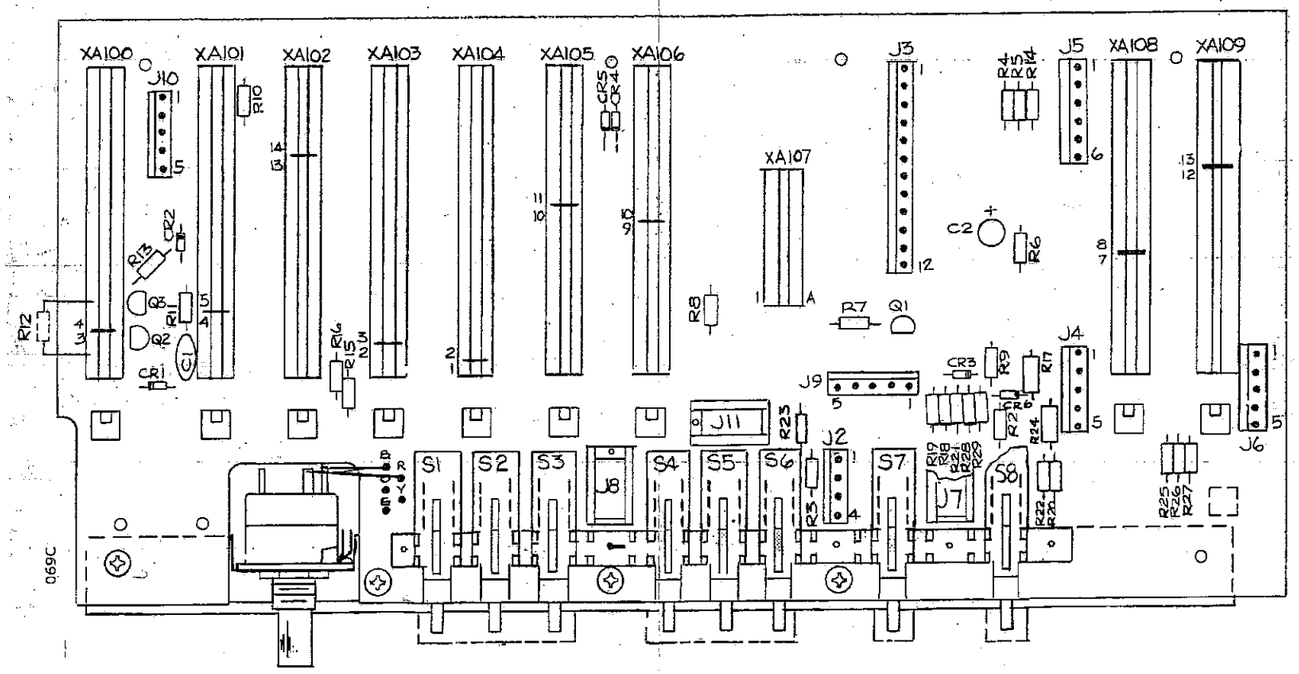


3 P/N: 2710016.

4 INDUCTOR PART OF PC BOARD.

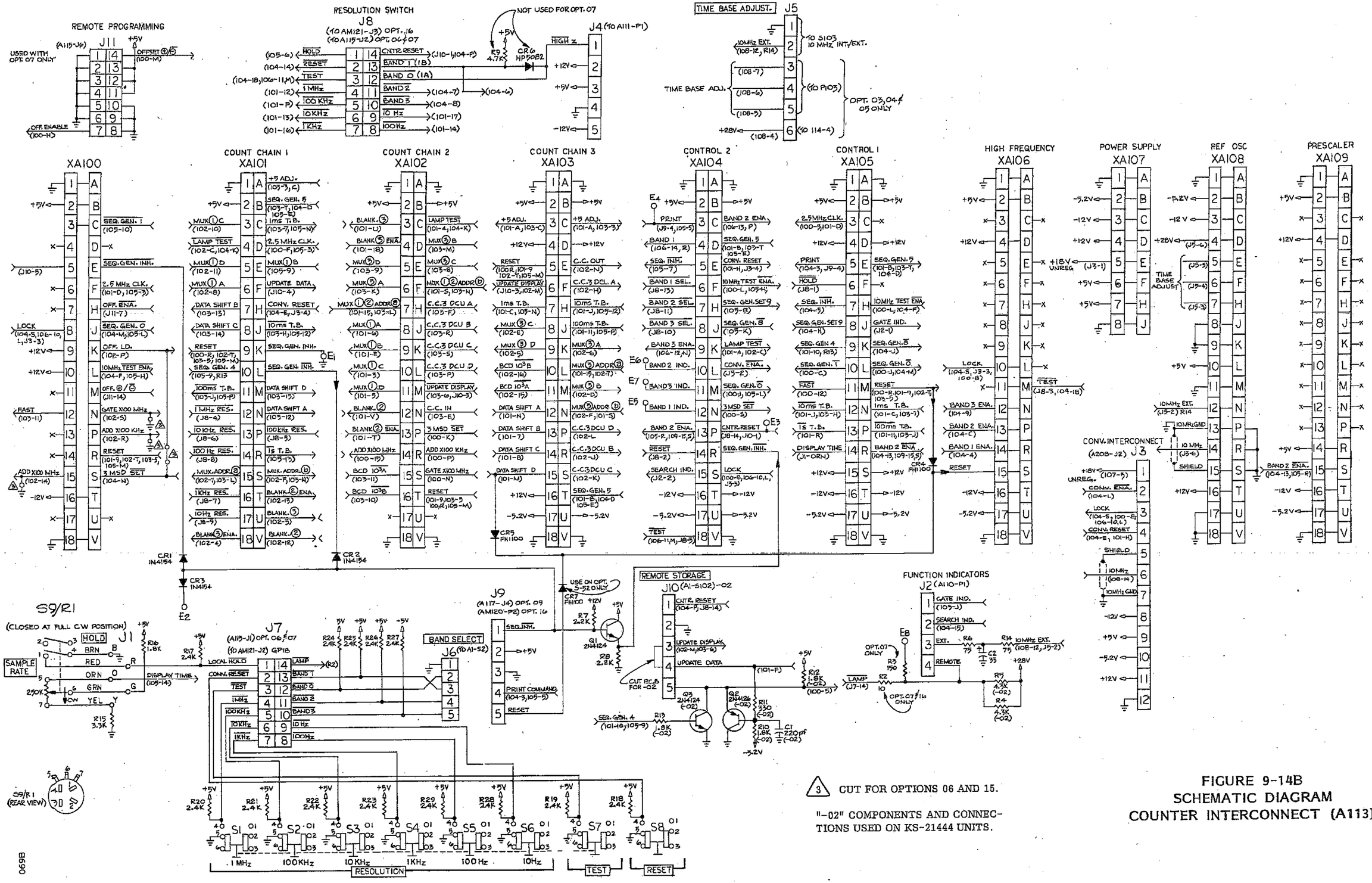
FIGURE 9-13B
SCHEMATIC DIAGRAM
PREAMPLIFIER (A111)

046F



NOTE: COMPOSITE PCB ASSEMBLY.
CERTAIN COMPONENTS USED ONLY
FOR SPECIFIC OPTIONS AND MODELS.

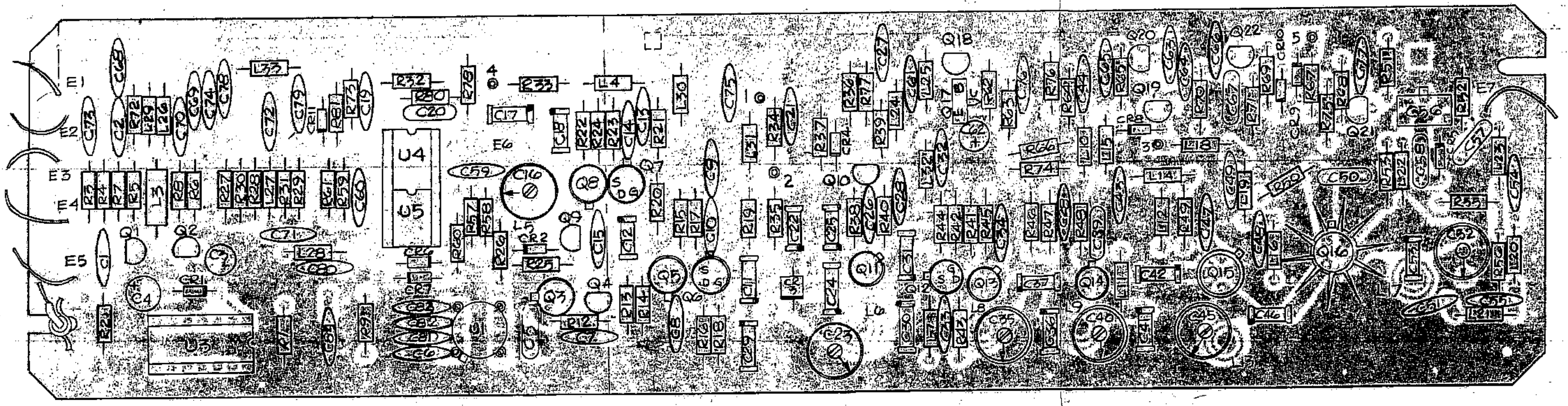
FIGURE 9-14A
COMPONENT LOCATOR
COUNTER INTERCONNECT (A113)



3 CUT FOR OPTIONS 06 AND 15.

"-02" COMPONENTS AND CONNECTIONS USED ON KS-21444 UNITS.

FIGURE 9-14B
SCHEMATIC DIAGRAM
COUNTER INTERCONNECT (A113)



SOURCE AMPLIFIER (A201)

General

A source of up to one watt of power at 200 MHz is required to drive the step recovery diode Comb Generator in YIG module A207. The 200 MHz must be both stable and coherent with the master oscillator in the counter. Stability is required to provide an IF spectrum that is dependent only upon the input signal spectrum. Coherence with the master oscillator is required to make counting accuracy dependent only upon the accuracy of the master oscillator.

The requirements of stability and coherence are satisfied by using a phase locked loop to lock a 200 MHz LC oscillator to the 10 MHz Time Base oscillator. The required output power is generated by a class C amplifier that contains a leveling loop to set the power output at any desired level from 1 mw to 1.1W.

Circuit Description

The phase lock loop is a standard second order loop, implemented by using digital phase lock loop components. The 200 MHz LC oscillator is a modified Colpitts circuit with bias stabilization supplied by Q10. The output frequency of the 200 MHz oscillator is divided by 20 in U1 to produce a 10 MHz square wave. This signal is compared to the processed 10 MHz reference by phase detector U3. Phase error is amplified by active filter U4 and applied to voltage variable capacitor CR3. This holds the 200 MHz oscillator "locked" in phase to the 10 MHz reference signal. C23 sets the open loop center frequency of the oscillator.

The main power amplifier consists of four stages: Buffer amplifier Q12 and Q13, linear amplifier Q14, and two Class C stages Q15 and Q16. Output power level is controlled by adjusting the value of the negative voltage supplied by Q17 and Q18 to the linear amplifier and the Class C stages.

The power leveling loop operates by sampling the peak value of the output signal with CR5, and comparing this value to the Power Reference. The comparison is made by differential amplifier Q19 and Q20, which then controls Q17 and Q18.

FIGURE 9-15A
COMPONENT LOCATOR
SOURCE/AMPLIFIER (A201)

FREQUENCY DIVIDER

BUFFER

BUFFER

PHASE DETECTOR

10 MHz AMP

OFF OF BOARD
PART OF MODULE ASSY (2010091)

POWER AMPLIFIER

OSCILLATOR

AMPLIFIER

OUT OF LOCK CONTROL

LEVELING LOOP

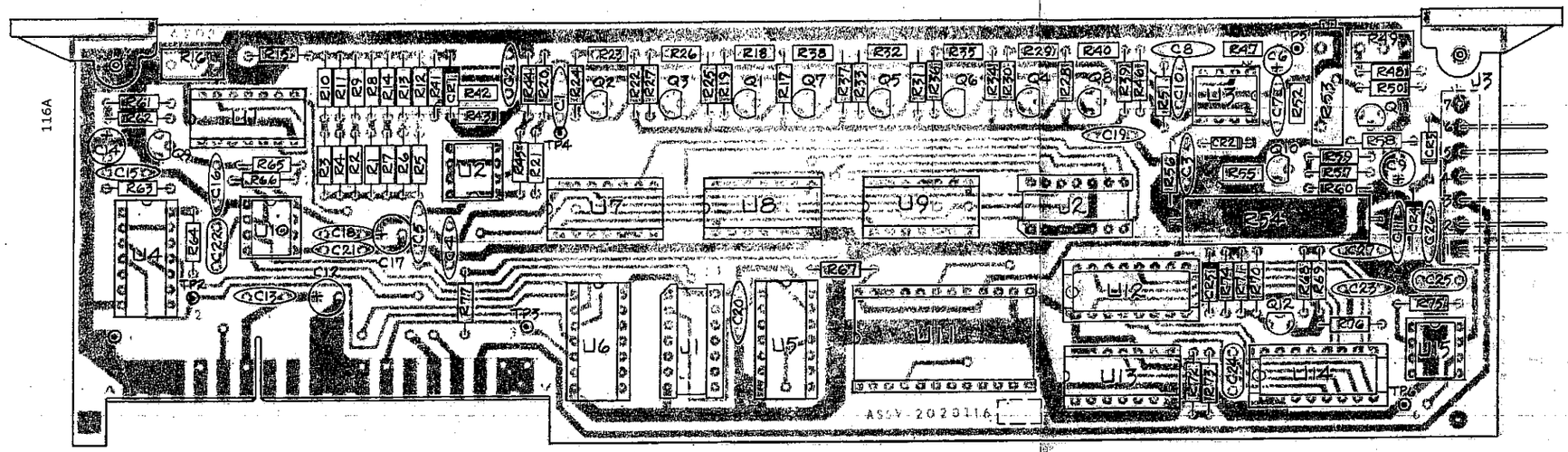
OFF BOARD
PART OF MODULE ASSY (2010091)

NOT USED

△3 PART OF PC BOARD.

FIGURE 9-15B
SCHEMATIC DIAGRAM
SOURCE/AMPLIFIER (A201)

091P



CONVERTER CONTROL 2 (A202)

Converter Control 2, utilizing enable and reset commands from Converter Control 1 (A203), creates the signals required to tune the frequency of the YIG Comb Generator, and control its output power. A202 consists of three principal circuits: DAC 1 and DAC 2, which provide a linear control voltage for the YIG sweep; the YIG Driver, which converts the linear outputs of the DACs to the proper drive currents for the YIG; and the Power Leveler, which controls the YIG output current.

Digital-to-Analog Converter Section

This section consists of a clock generator, DAC 1 (the main DAC), DAC 2 (the fine DAC), and the DAC control circuitry. U10 generates pulses at a 500 microsecond rate. These pulses drive either DAC 1 or DAC 2. If DAC 1 is enabled, the clock drives U7-9, whose outputs go to transistors Q1-8. When the appropriate output goes high it saturates the transistor, effectively connecting the collector resistor to the temperature compensated 3.1 V reference. This sums current into U3A causing the output to step up in voltage. The linear step function is achieved by properly selecting the values of the collector resistors for Q1-8. The high precision of these resistors, and the stability of the 3.1 V reference, provides the needed accuracy. Because the A output of U7 does not drive the sum line, the speed of DAC 1 is effectively divided-by-two, giving it a rate of 1 ms/step. The amplitude of the DAC is equivalent in YIG current to 200 MHz/step. The outputs of U7-9 are also connected to J2, providing the 3MSD information to the Count Chain.

In DAC 2, the clock drives U1 whose outputs are connected directly through resistors to the sum line. Because of the small size of DAC 2 (1.5 MHz/step), the accuracy of DAC 1 is not needed. Q9 provides a backward step at the beginning of DAC 2 to compensate for eddy current delays within the YIG Comb Generator.

Sweep Driver Section

The Sweep Driver section consists of an operational amplifier, a voltage translator, and two cascaded output transistors. The second output transistor (A2Q1) is located on the Converter chassis.

The ramp from the DACs drives the inverting input of U3B; R49 sets the ramp offset, and R53 determines the slope of the ramp. Feedback voltage is obtained across sense resistor R54, forcing an extremely linear relationship between the sweep voltage and the YIG filter current. CR3 limits the voltage developed across the YIG filter tuning coil during flyback, to protect Q11 and A2Q1.

Power Control Section

The Power Control section consists of an E PROM (U11), and a binary DAC (U14, U15). The 3MSD lines drive the address inputs of U11, which generates, for each address, the proper buffered 8-bit output which feeds the input of the 8-bit DAC. The analog output of the DAC is the signal which controls the YIG comb power by adjusting the output power of the Source Amplifier (A201).

During Reset, or when the Converter is not enabled, Q12 and U13B effectively cut the reference current in U14 to zero, thus shutting down the power level output.

FIGURE 9-16A
COMPONENT LOCATOR
CONVERTER CONTROL 2 (A202)

I.C. NO.	TYPE	GND	+5V	+12V	-12V
U4	7400	7	14	—	—
U5-U6	7404	7	14	—	—
U13	7408	7	14	—	—
U11	1702A	AS SHOWN			
U12	MC14050	8	1		
U7-U8-U9	74176	7	14	—	—
U1	74393	7	14	—	—
U15	LM741	—	—	7	4
U14	MC1408 L-6	AS SHOWN			
U2-U3	MC1458	—	—	8	4
U10	NE555	1	8	—	—

NOT USED

7404 U5C

7408 U13A

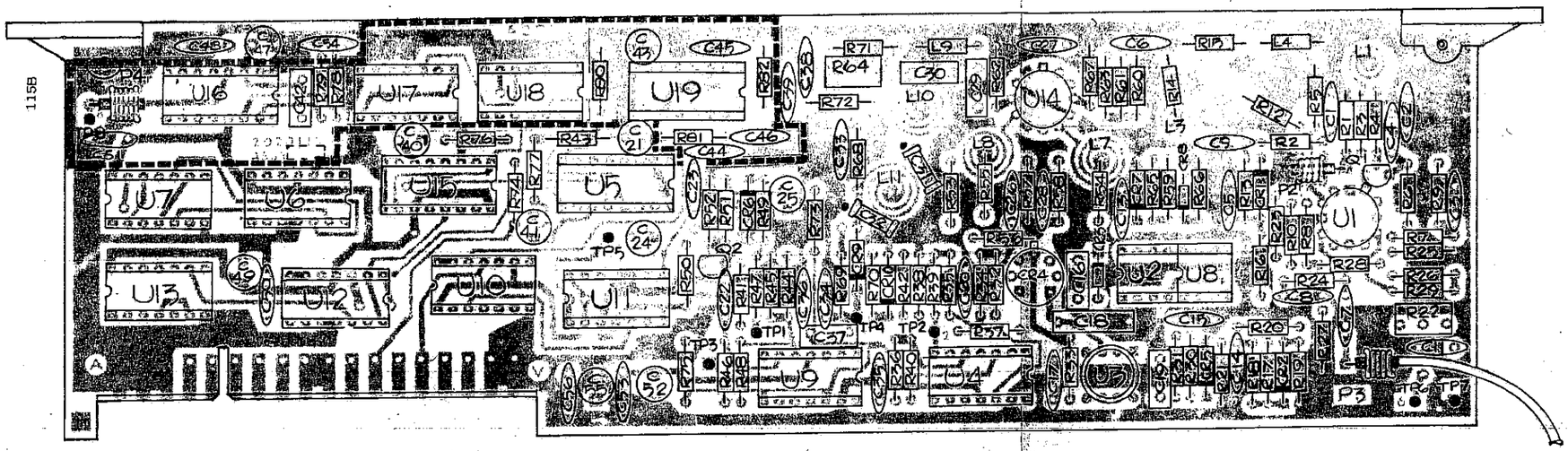
3 J1, J2 NOT USED ON 371 COUNTER.

4 P1-D/4 CONNECTS TO A208P1-14.

FIGURE 9-16B
SCHEMATIC DIAGRAM
CONVERTER CONTROL 2 (A202)

116A

371



CONVERTER CONTROL 1 (A203)

Converter Control 1 performs all the control functions necessary to lock the microwave Converter to the correct YIG/Comb Generator (A207) output frequency, and provide appropriate signals to the direct counter.

Converter Control 1 consists of five basic functional sections: a Video Limiter, a Video Detector, an In-Band Detector, an Analog Processor, and Signal Acquisition Logic. The Video Limiter processes the signal from A204 to provide a constant amplitude signal to the High Frequency board (A106). The Video Detector converts the incoming video signal from A204 to a level proportional to the incoming power. This signal is then compared to a number of preset levels in the Analog Processor circuits, and converted into digital signals for further processing. The In-Band Detector is used to determine whether or not the video frequency falls within the desired passband, and to enable the Analog Processor circuits. The Signal Acquisition Logic provides the digital commands to control the sweep circuits and to lock the Converter on the appropriate comb line.

Figure 9-17C shows the operating sequence of the Converter. In the absence of an input signal to the Converter, a 200 MHz/ms sweep is continuously generated (DAC 1 ENABLE and CLOCK ENABLE are high). At the end of each sweep, a CONVERTER RESET command is generated (point A to point B on waveform). When a signal is applied, a Video Detector output will be generated when the YIG filter is tuned through the correct harmonic (point C). When this signal appears, a CONVERTER RESET command is again generated (point C to point D), and the sweep is reset to zero. A new sweep is initiated (point D) and eventually the Video Detector again produces an output (point E). At this point, a small backward step will be taken, followed by a 3 millisecond delay (point E to point F). At the end of this time, DAC 2 turns on, and a considerably slower sweep (3 MHz/msec) begins. At point G, the Video Detector output has reached 90% of the value stored in the Peak Detector, and the sweep is stopped. Three milliseconds later (point H), a LOCK command is given, which will allow the counter to read the frequency applied to the High Frequency board (A106). If the sweep is inhibited from stopping at point G (by grounding A203TP2), the Video Detector output will appear as shown by the dotted line on the waveform.

Video Limiter and Video Detector Sections

The incoming signal from the Video Amplifier (A204) enters at connector P2, passes through an isolation buffer U1B, and is limited by amplifier U1A. This provides a fixed output of approximately -5 dBm to A106. U1B also drives Video Detector diode CR1. Diode CR2 (matched to CR1) is used for temperature compensation of CR1 bias. The rectified signal is then amplified by U8, whose gain is set by Video Detector Gain Control R22. The setting of R22 determines the minimum required lock signal from the Video Amplifier. As such, its setting plays an important part in determining the sensitivity of the Converter. Refer to Section 6 for the proper adjustment procedure.

In-Band Detector

The buffer also provides the drive for a two-stage limiter U14, which drives, in turn, a bandpass filter whose output is then detected by CR9. (Matched diode CR10 provides temperature compensation for CR9.) The output level of CR9 is thus a function of frequency only. When the output of CR9 exceeds the DC level set by R64, the In-Band Detector triggers, generating a TTL compatible output signal. Trigger level hysteresis prevents the In-Band Detector from turning off until the signal is reduced considerably in power. R64 is set to turn on the In-Band Detector at 250 MHz. Once turned on, it will not turn off until the frequency is increased to approximately 275 MHz. It is this difference in turn-on and turn-off frequency which determines the FM tolerance of the heterodyne Converter at the edge of the video passband.

During Reset time the YIG/Comb Generator has no output, so no in-band should be generated. If one is generated, it is an indication that the input to the Converter contains spurious signals of sufficient amplitude to interfere with the operation of the in-band. The Noise Control circuit senses this in-band and generates a ramp to increase attenuation of the input signal via the PIN Diode Attenuator (A206) until in-band goes away, at which point the spurious inputs no longer create a problem. After Reset, A206 remains preset to that amount of attenuation, and the Converter can function with no interference from spurious signals.

Analog Processor

The Analog Processor contains a DC-coupled comparator, and a Peak Detector. The purpose of this section is to convert the analog output of the Video Detector into digital commands which can be used to lock the Converter to the correct comb line. U9A compares the Video Detector output to preset levels, and is used to determine that there is sufficient power level from the Video Amplifier. This comparator is enabled by the In-Band Detector output.

Operational amplifiers U2, U3, and associated circuitry, form a Peak Detector which stores the maximum Video Detector output (limited to 500 mV by CR11) during a particular sweep period. U4A compares the stored output of the Peak Detector with the instantaneous value of the Video Detector output. Switching occurs when that output reaches 90% of the stored peak.

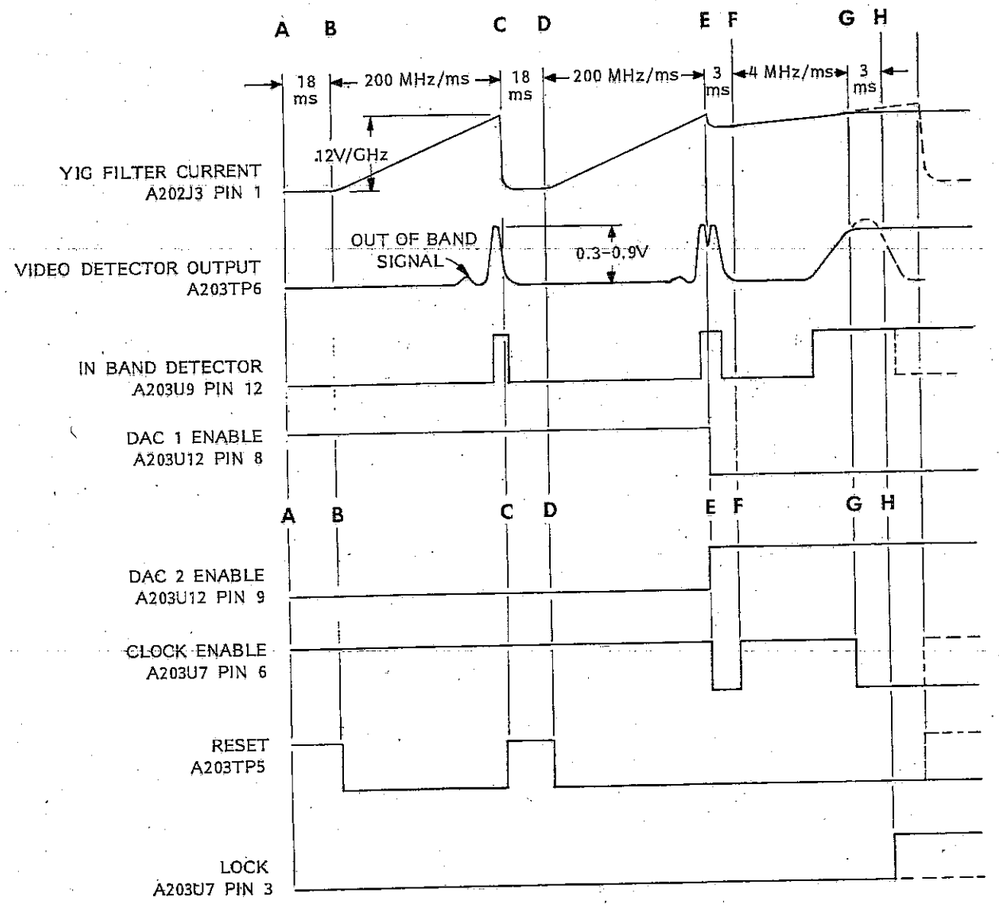
The Peak Detector is discharged by U4B. A CONVERTER RESET command, or lack of the In-Band Detector signal, will activate U4B. The circuit is inhibited from discharging by the presence of the DAC 2 ENABLE command.

The outputs of the two comparators (U4A and U9A), then form input commands to the Signal Acquisition Logic.

Signal Acquisition Logic

There are five commands generated by the Signal Acquisition Logic: CONVERTER RESET, DAC 1 ENABLE, DAC 2 ENABLE, CLOCK ENABLE, and LOCK. The CONVERTER RESET command is an 18 millisecond pulse used to reset the digital logic on both this board and Converter Control 2 (A202), and to enable the Noise Control circuit. The three enable commands determine which DAC (if any) will control the sweep current applied to the YIG filter. If the CLOCK ENABLE is low, no sweep will occur, and the current to the YIG will remain constant. If the CLOCK ENABLE is high, either DAC 1 or DAC 2 (on A202) will generate a current sweep. The appropriate DAC is selected by the DAC ENABLE commands.

FIGURE 9-17A
COMPONENT LOCATOR
CONVERTER CONTROL 1 (A203)



The following description is keyed to the corresponding lettered points on the waveforms shown in Figure 9-17C.

A. Initiation of CONVERTER RESET: A CONVERTER RESET will occur in the digital logic whenever any one of the following occur: (1) CONVERTER RECYCLE command from A104. (2) Either DAC reaching the end of its range. (3) Loss of sufficient video level (U9A input drops below threshold). (4) Image Rejection circuit operating (see later paragraph). When this occurs, U5 pin 1 goes low, causing it to generate an 18 millisecond CONVERTER RESET pulse. This pulse will reset DAC 1, DAC 2, U11B, and U7A.

B. Start Sweep: CONVERTER RESET goes low and enables DAC 1.

C. Presence of Sweep Related Signal: An In-Band signal of sufficient amplitude triggers U9A. When the signal drops below the threshold value, the negative transition triggers flip-flop U11A. This action generates a CONVERTER RESET. All circuits *except* U11A are reset; U11B is enabled.

D. Start of Second Sweep: End of CONVERTER RESET triggers U11B which, in turn, enables U12A. The purpose of the second sweep is to guarantee that after the signal has been applied to the Converter, a sweep is begun from zero frequency. This prevents locking to a harmonic of the input frequency.

E. Presence of Sweep Related Signal: The negative transition of U9A, as described in paragraph C, triggers U12A. This turns on DAC 2 ENABLE. In addition, multivibrator U5A is triggered, which generates a 3 millisecond pulse. The CLOCK ENABLE is turned off during this pulse, and U6A is triggered. The output of U6A enables U6B. The loss of DAC 1 ENABLE also results in a negative current step (generated on Converter Control 2) such that the YIG/Comb Generator is tuned back through the frequency that initiated the trigger. This action causes the twin peaks in the Video Detector output. During this period, the Peak Detector has stored the peak detected signal level; the voltage at U4 pin 6 is 90% of that peak.

F. Start of DAC 2 Sweep: The CLOCK ENABLE command goes high at the end of the pulse from U5A.

G. Stop Sweep: When the Video Detector output reaches 90% of the stored peak U4A is triggered, which again causes a 3 millisecond pulse to be generated by U5A. This pulse triggers U6B which disables the CLOCK ENABLE.

H. Lock: At the end of the 3 millisecond pulse, the LOCK command is obtained at U7 pin 3 (this allows the counter to display the input frequency). If at any time after LOCK command occurs, the output of the Video Detector should drop below the threshold set at U9 pin 5, a CONVERTER RESET command will be initiated when U9 pin 10 goes high.

Image Rejection

At input levels below the specified sensitivity, it is possible that although the video level is insufficient to trigger U9A on the correct comb line, the next higher line *is* sufficient. If the counter should lock to this line, called the image, an erroneous reading would result. To prevent this, an image rejection circuit consisting of U12B and U15 is provided.

If the In-Band Detector turns on, then off, without U9A triggering, multivibrator U15B enables flip-flop U12B for 3 milliseconds. If during this period, U9A is triggered, resulting in DAC 1 ENABLE going low, U12B will be triggered, resulting in a CONVERTER RESET. The Converter is thus prevented from locking on the image.

FIGURE 9-17C
OPERATING SEQUENCE
CONVERTER CONTROL 1 (A203)