LIMITER

PEAK DETECTOR

LOCK CONTROL

ISOLATION AMP

VIDEO DETECTOR

VIDEO THRESH COMPARATOR

SWEEP CONTROL

RESET GENERATOR

IN-BAND CIRCUIT

IMAGE REJECTION

NOISE CONTROL CIRCUIT

NOT USED U13

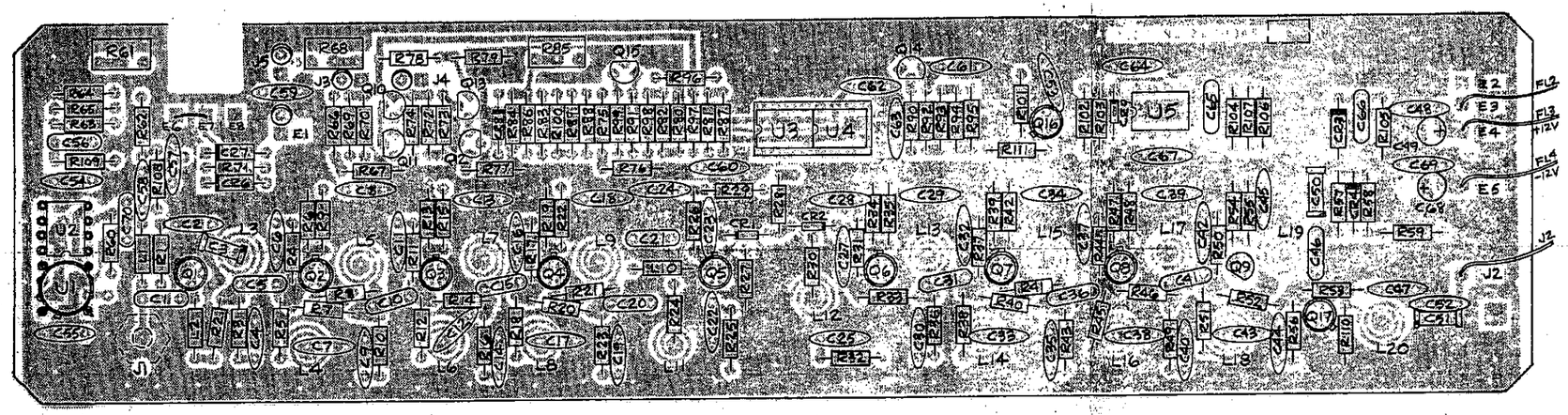
I.C. NO.	TYPE	PIN NO. GND	+5V	+12V	-5.2V	-12V
U10	DM7400	7	14			
U13	DM7405	7	14			
U7	DM7408	7	14			
U18	DM7420	7	14			
U6 U11 U12	DM7473	11	4			
U5 U15 U19	DM74123	6	1	9		
U17	DM74393	8	16			
U1 U14	CA3049					
U3	CA3130			4	7	
U2	LM741C				7	4
U8	LM1415				7	4
U16	MC14081-C	12	13			3 4
U9	72506			4	11	
U4						

3 PART OF PCB.

4 MATCHED PAIR.

FIGURE 9-17B
SCHEMATIC DIAGRAM
CONVERTER CONTROL 1 (A203)

115B



045S

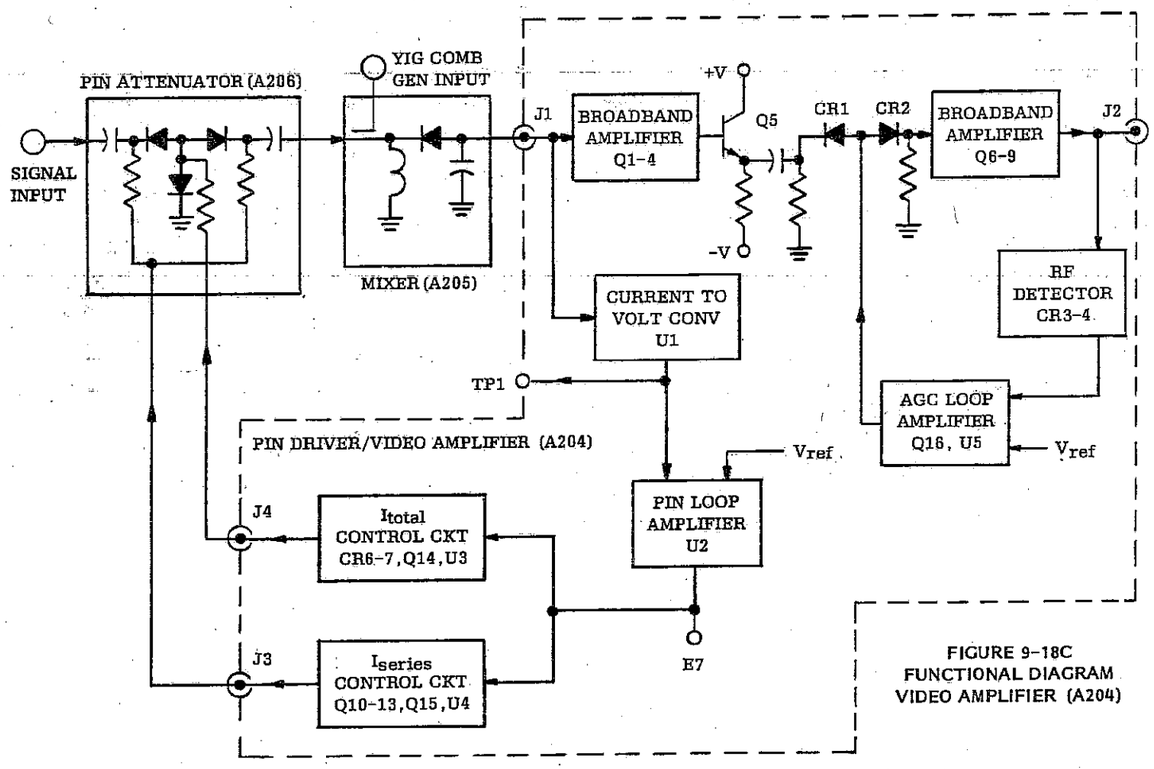


FIGURE 9-18C
FUNCTIONAL DIAGRAM
VIDEO AMPLIFIER (A204)

PIN DRIVER/VIDEO AMPLIFIER (A204)

Refer to Functional Diagram — Figure 9-18C.

The PIN Driver/Video Amplifier module (A204) consists of two distinct sections: the PIN Diode Attenuator Control Loop, and the Video Amplifier.

Components of the PIN Driver include:

a. PIN Diode Attenuator (A206).
b. Mixer (A205).
c. Current-to-Voltage Converter (A204U1).
d. Loop Amplifier (A204U2).
e. I_{series} Control Circuit (A204Q10-13,Q15,U4).
f. I_{total} Control Circuit (A204CR6,CR7, Q14,U3).

Components of the Video Amplifier include:

a. Four-stage Broadband Amplifier (A204Q1-4).
b. PIN Attenuator Section (A204CR1, CR2,Q5).
c. Four-stage Broadband Amplifier (A204Q6-9).
d. RF Detector (A204CR3, CR4).
e. AGC Loop Amplifier (A204Q16,U5).

The PIN Diode Attenuator Control section is a simple feedback loop. DC current from the Mixer diode is converted to a voltage by U1. This voltage is compared to reference voltage (V_{ref}) at the input of U2. The difference in the two voltages is amplified by U2, and appears at E7. This voltage causes the proper currents to flow from the current generators: I_{series} and I_{total}. These currents determine the magnitude of signal attenuation in the PIN Diode Attenuator (A206).

The I_{series} and I_{total} current generators contain shaping networks that control the ratio of the currents through the series and shunt diodes in the attenuator to provide a fairly constant 50 ohm terminal impedance.

The current shaping network for I_{total} consists of CR6, CR7, R68, and R71. CR6 and CR7 produce an approximately exponential curve, while R68 and R71 produce a linear curve. Their sum determines the shape of the current into the summing node at R75.

In operation, an increase in signal power at the attenuator input results in an increase in the magnitude of DC current from the Mixer diode. The increased current causes the outputs from U1 and U2 to tend positive, increasing I_{total} while decreasing I_{series}. This produces an increase in the current through the shunt diode, and a decrease in the current through the series diodes, in a ratio which maintains a 50 ohm terminal impedance. This action decreases the magnitude of change in signal power which appears at the Mixer diode.

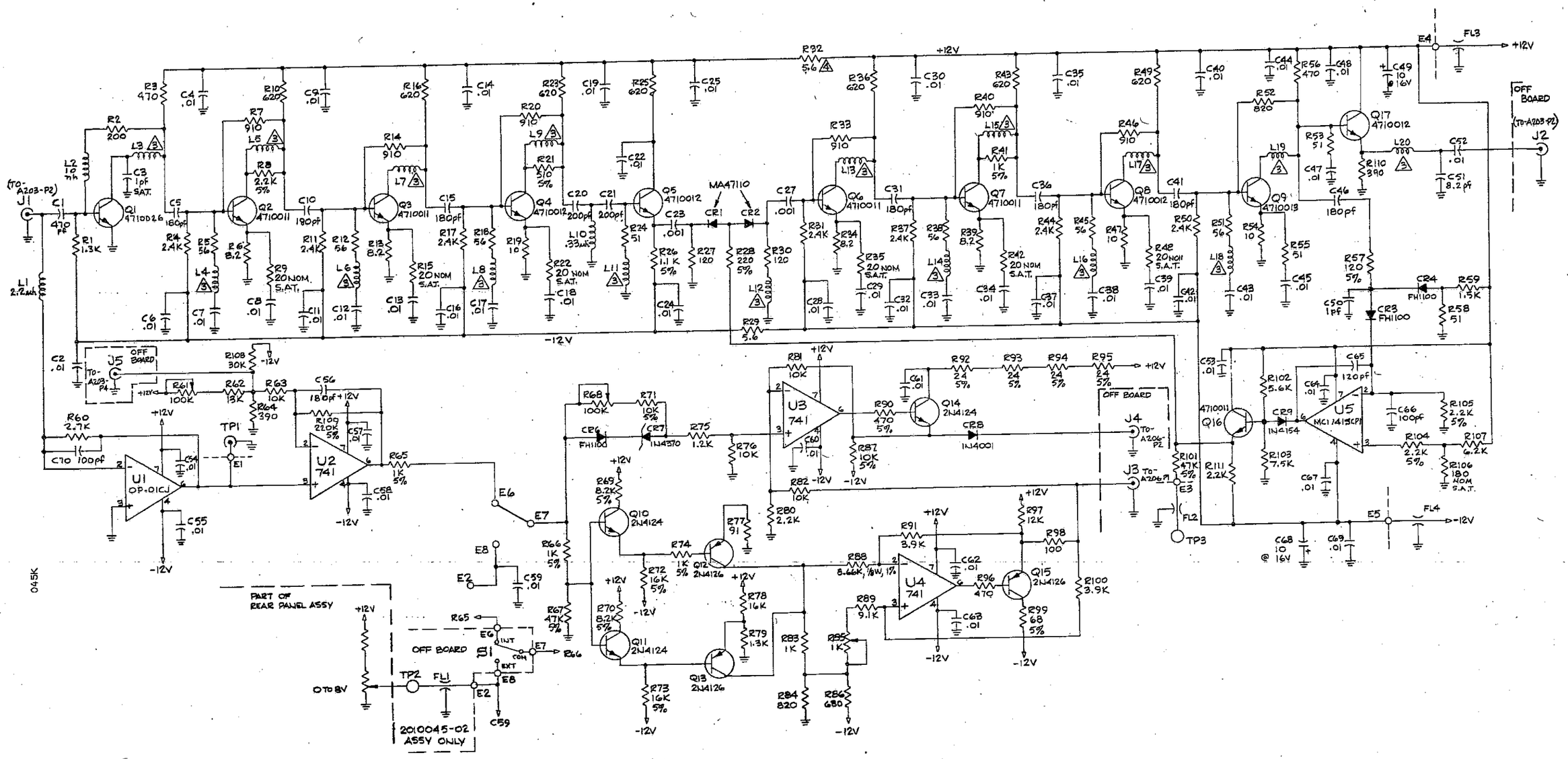
The Video Amplifier section amplifies the difference frequency produced by the Mixer, and applies it to Converter Control 1 (A203).

The circuit consists of eight essentially identical gain blocks and an automatic gain control. Overall gain of the Video Amplifier is nominally 56 dB, with a frequency range of 25 MHz to 275 MHz.

A typical gain block includes a single broadband transistor amplifier stabilized by series and shunt feedback, and an output matching inductor.

The AGC portion of the amplifier consists of RF level detector CR3 and CR4, loop amplifier U5, PIN Diode current driver Q16, emitter follower Q5, and PIN Attenuator diodes CR1 and CR2. The reference voltage in the AGC loop sets the maximum output power level for the Video Amplifier at 0 to +1 dBm.

FIGURE 9-18A
COMPONENT LOCATOR
VIDEO AMPLIFIER (A204)



3 PART OF PC BOARD.

FIGURE 9-18B
SCHEMATIC DIAGRAM
VIDEO AMPLIFIER (A204)

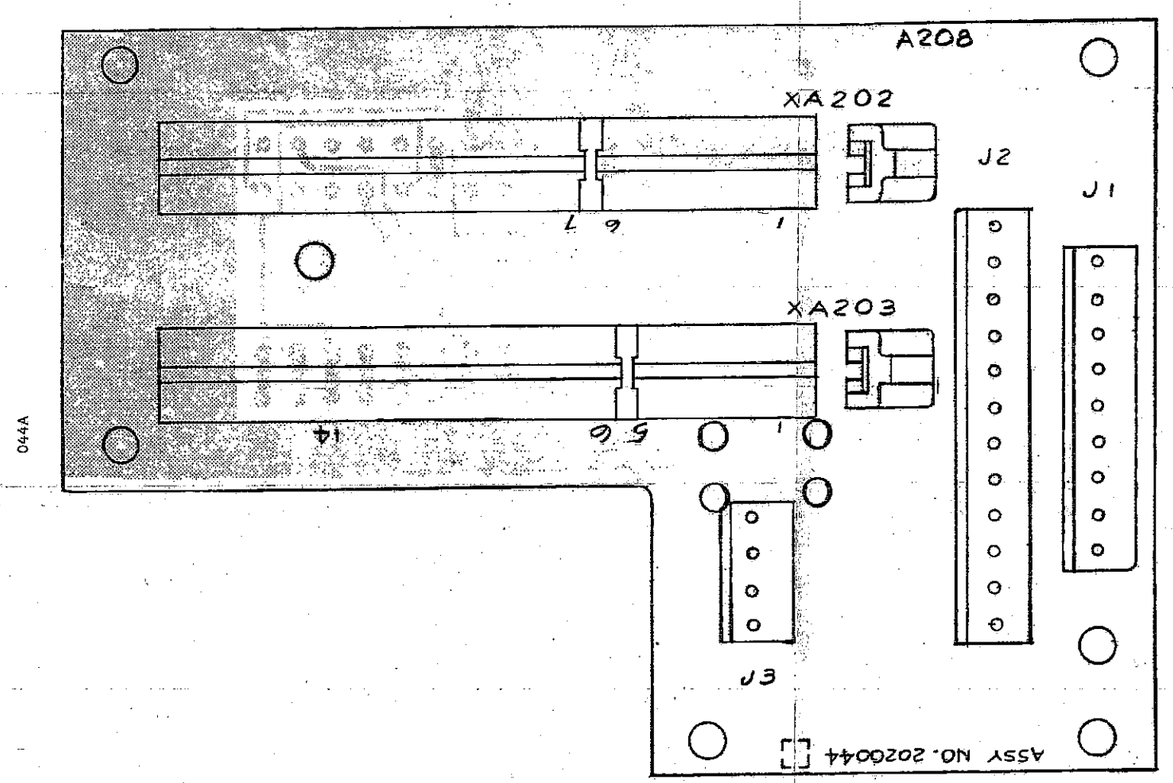


FIGURE 9-19A
COMPONENT LOCATOR
CONVERTER INTERCONNECT (A208)

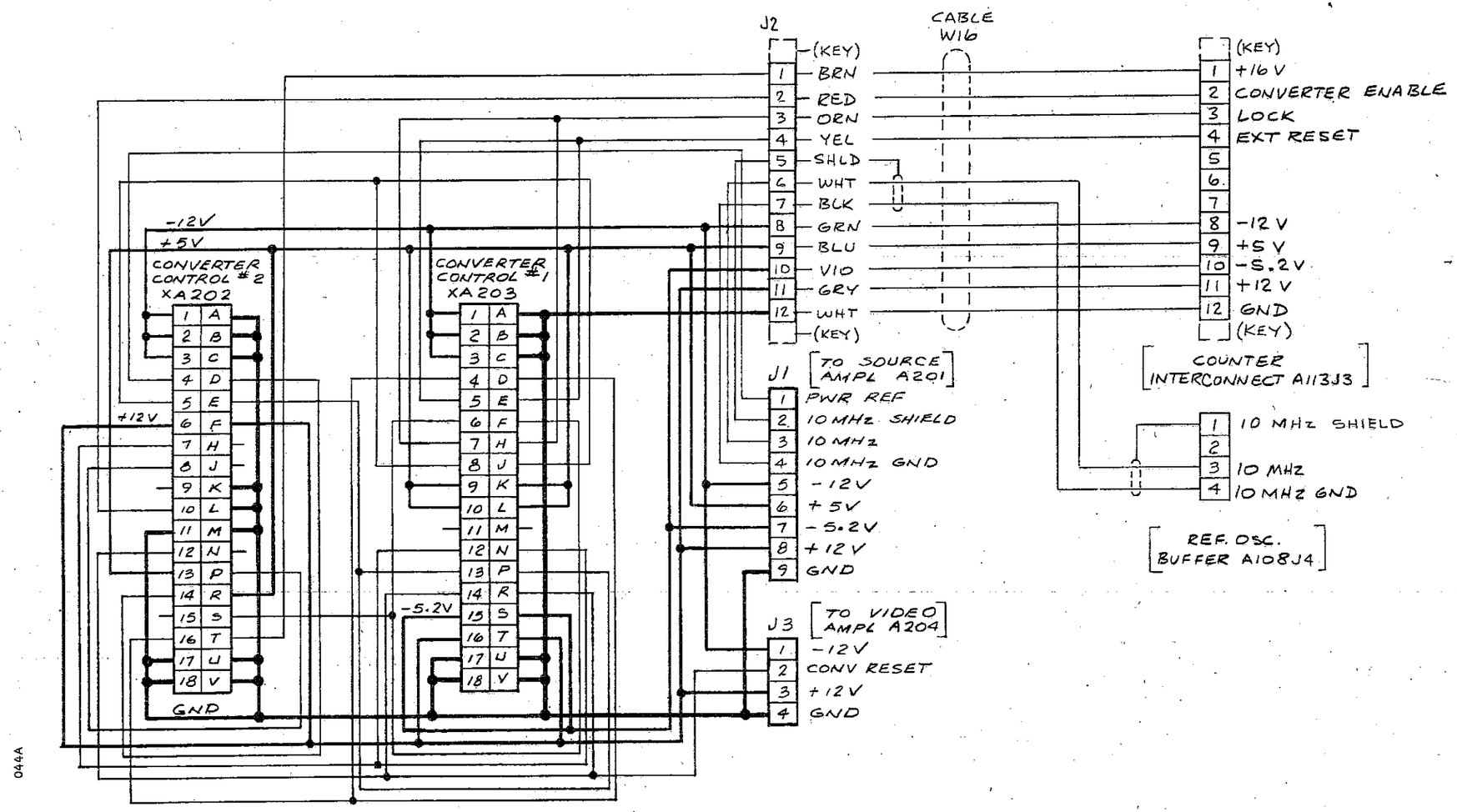
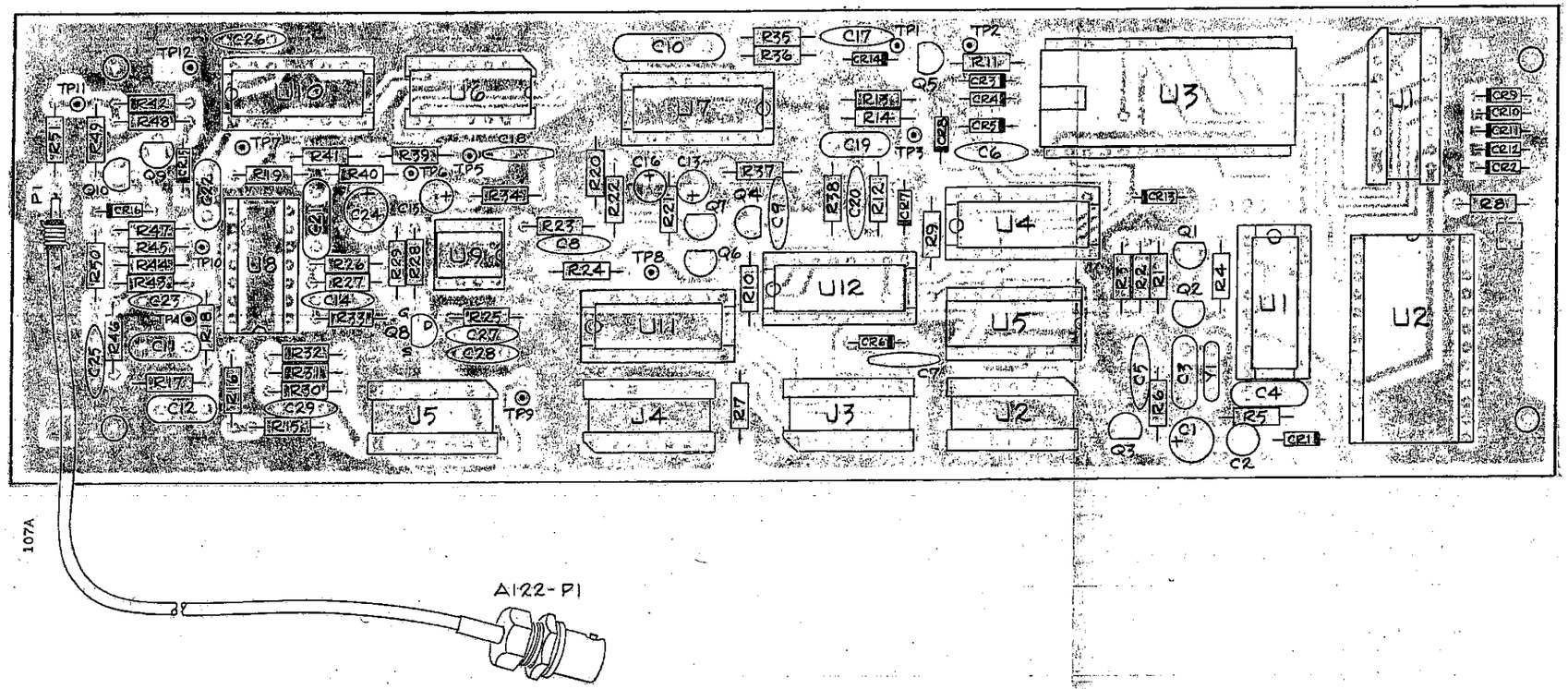


FIGURE 9-19B
SCHEMATIC DIAGRAM
CONVERTER INTERCONNECT (A208)



MICROPROCESSOR (A122)

A122 contains the microprocessor (μP) which controls all of the data manipulation and mathematical computation to perform the YIG Preset, Phase Lock, and Band Change functions.

The heart of the μP board is the 4040 Microprocessor (U2). U2 requires two clock signals and a Power On Reset signal which are supplied by clock generator U1. All the signals for data to and from the μP, are carried on the 1-bit Test input, the 1-bit Carry output line, or the 4-bit bi-directional data lines ($D_0 - D_3$).

The 4-bit data lines are connected between U2 and U3. U3 is a combination ROM (read only memory), and I/O (input/-output) IC. The ROM contains the program steps that control the programming of U2. The four I/O ports are 4-bits each, resulting in 16 data I/O lines. These lines are set up as four input lines, and twelve output lines. These 16 lines, plus the Test input and Carry output on U2, control all the data manipulation in the system.

Data Input

Data input to the μP follows one of two basic methods: Serial data input, or parallel data input. Parallel input is the simplest method, but it requires one input port for each data bit. It is, therefore, used in only one place in the system: the input from the keyboard (KEY 0 - KEY 2).

The remainder of the input data is read by a serial input data process. Two 8-bit shift registers (U11, U12), are used to input appropriate data. The process begins with a series of commands which load U11 and U12 with the 16 bits of data on their inputs. After the Load command, the first piece of data (Converter Lock) is available on the Test input to U2. For each subsequent piece of data, a clock pulse shifts register data up one bit. To read any piece of data requires N-1 clock pulses, where N equals the number of bits down on the shift register where the data is located.

Data Output

Data output also occurs in both serial and parallel modes. The parallel mode is used only for the 4-bit BCD number which lights the numerical display (MUX A - MUX D). All other data is sent out in the serial mode. In this mode, the data is presented one bit at a time, on the Carry Output of U2. While the data is present, a clock pulse is sent to clock the data into an appropriate shift register. For the serial output routine, one clock pulse is required for each bit of data to be read out. Data which is to be sent out by this process includes YIG Preset, PLL Program, Gain Adjust, and Band Select.

Loop Amplifier

The Loop Amplifier has essentially three stages of gain (U8A, B, and C). U8A is a 2-pole low pass filter. It has a DC gain of two, and a corner frequency of 16 kHz. Above the corner frequency, the gain drops off at the rate of 12 dB per octave.

U8B is a summing amplifier used to combine the signal from the oscillator (U7) with the video from U8A, and also with an external input (TP6) for introducing signals for loop test purposes. U8C, in combination with U10, is a digitally controlled gain stage. U10 is designed to be used with a summing amplifier and an internal 10 K ohm feedback resistor, to give a gain that is proportional to the binary number programmed. (The gain of this stage would normally be .0078 to .999 using the internal 10 K feedback resistor. However, resistor R42 has been added to increase the gain by a factor of 1.3, resulting in a .01 to 1.3 gain range.) The gain of U10 is programmed by the μP through U6. The program is written such that the gain can be stepped in approximately 3 dB steps.

Bandwidth Adjust Oscillator

U7 is a dual frequency monolithic waveform generator. The frequency of the oscillator is determined by the Select line (FSK) on U7 pin 9. When pin 9 is low, the frequency is determined by C10/R14. When pin 9 is high, the frequency is determined by C10/R13. A sine wave is obtained by first generating a triangular wave, then driving a triangle-to-sine wave converter. The purity of the resulting waveform is a function of how hard the converter is driven. R37 controls the drive to the converter, with its value selected for best signal purity.

Bandwidth Detector

The bandwidth detector (Q6-8, U8D, U9A/B), consists of three circuits: a DC restorer, a synchronous detector, and a Schmitt trigger. The DC restorer (U8D) functions by having a simultaneous DC gain of +10 and -10. This results in an output level close to zero volts for any DC input. The positive gain however, is bypassed for high frequencies, with the resulting gain for AC signals being -10. This stage drives synchronous detector U8A/B.

The synchronous detector functions by changing the gain of an amplifier from +1 to -1 in accordance with the polarity of the signal to be detected — that is, the gain is +1 when the signal is positive, and -1 when the signal is negative. The detector output essentially resembles that of a full wave rectifier. The amplifier output is passed through an integrator (R24/C13), whose output is a DC voltage proportional to the amplitude of the incoming signal. All signals not synchronous with the switching rate of the amplifier, have equal positive and negative gains, resulting in an average DC value of zero volts. The output of the synchronous detector drives a Schmitt trigger (Q8, Q7), which has about 250 mV of hysteresis. The output switches to a high at an input threshold of 1.33 volts, and to a low at an input threshold of 1.08 volts.

The automatic bandwidth adjustment process begins with the loop at its lowest gain (narrowest bandwidth). Oscillator U7 is turned on, with its output driving U8B; the output from U8B drives the synchronous detector. At narrow bandwidths, the peak detector sees the signal and sends out a high, indicating that the bandwidth is too narrow. The automatic programming increases the gain of the loop by stepping U10 in 3 dB increments. As the bandwidth increases, the frequency generated by U7 becomes a frequency inside the loop bandwidth. When this happens, the loop feeds back some signal at the output of U8A which is out of phase with that from U7. This feedback cancels some of the signal from the oscillator, and at the appropriate bandwidth, the output of U8B is small enough that the synchronous detector output goes low, indicating sufficient bandwidth.

FIGURE 9-20A
COMPONENT LOCATOR
MICROPROCESSOR (A122)

I.C. NO.	TYPE	PIN NO. GND	+5V	+12V	-12V	-10V	N/C
U1	4201		15			4	
U2	4040		9			14	
U3	4308		1			28	
U4	CD4010AE	8	1,16				13
U5, U6	74LS164	7	14				
U7	X2220G	12		4			
U8	UA4136			11	7		
U9	MC1458			8	4		
U10	AD7530	3		14			
U11, U12	CD4014AE	8	16				

* INDICATES 2% TOLERANCE.

ALL DIODES ARE EIP P/N: 2704154.

FIGURE 9-20B
SCHEMATIC DIAGRAM
MICROPROCESSOR (A122)

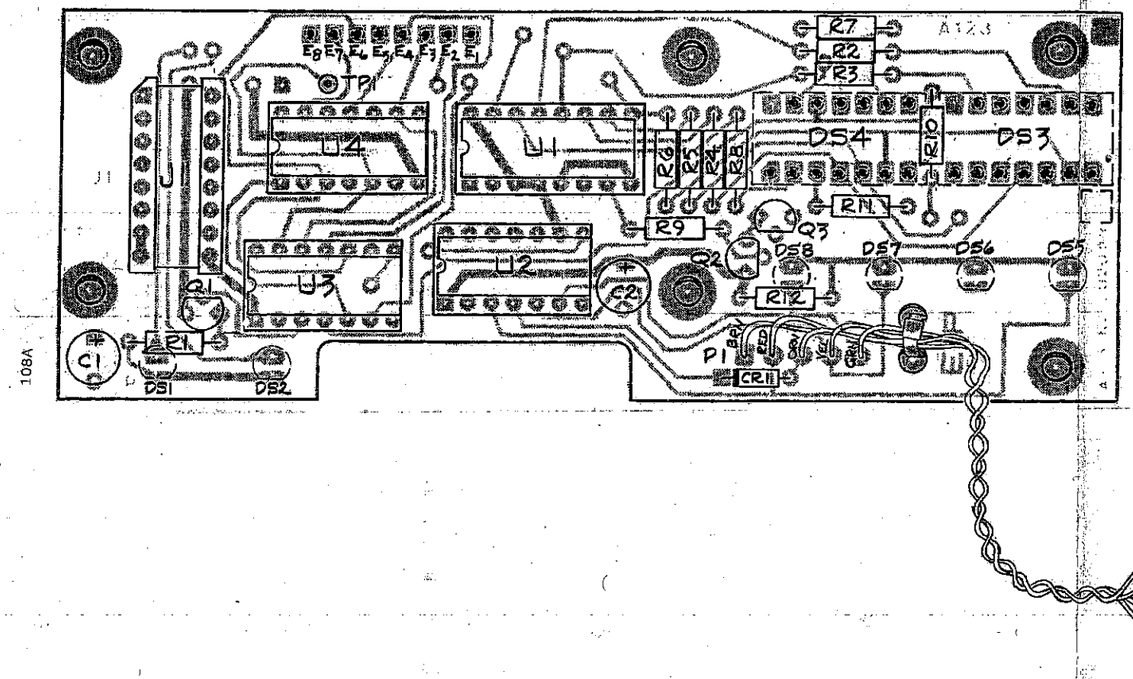


FIGURE 9-21A
COMPONENT LOCATOR
AUXILIARY DISPLAY (A123)

AUXILIARY DISPLAY (A123)

The Auxiliary Display board (A123) has three functions: to display the data entry digits for YIG Preset, and Phase Lock frequency; to light the BAND SELECT, PRESET, and LOCK status indicators; and to scan the keyboard for data entry. All signals to and from A123 are fed through J1, with the exception of local Band Select (on P1).

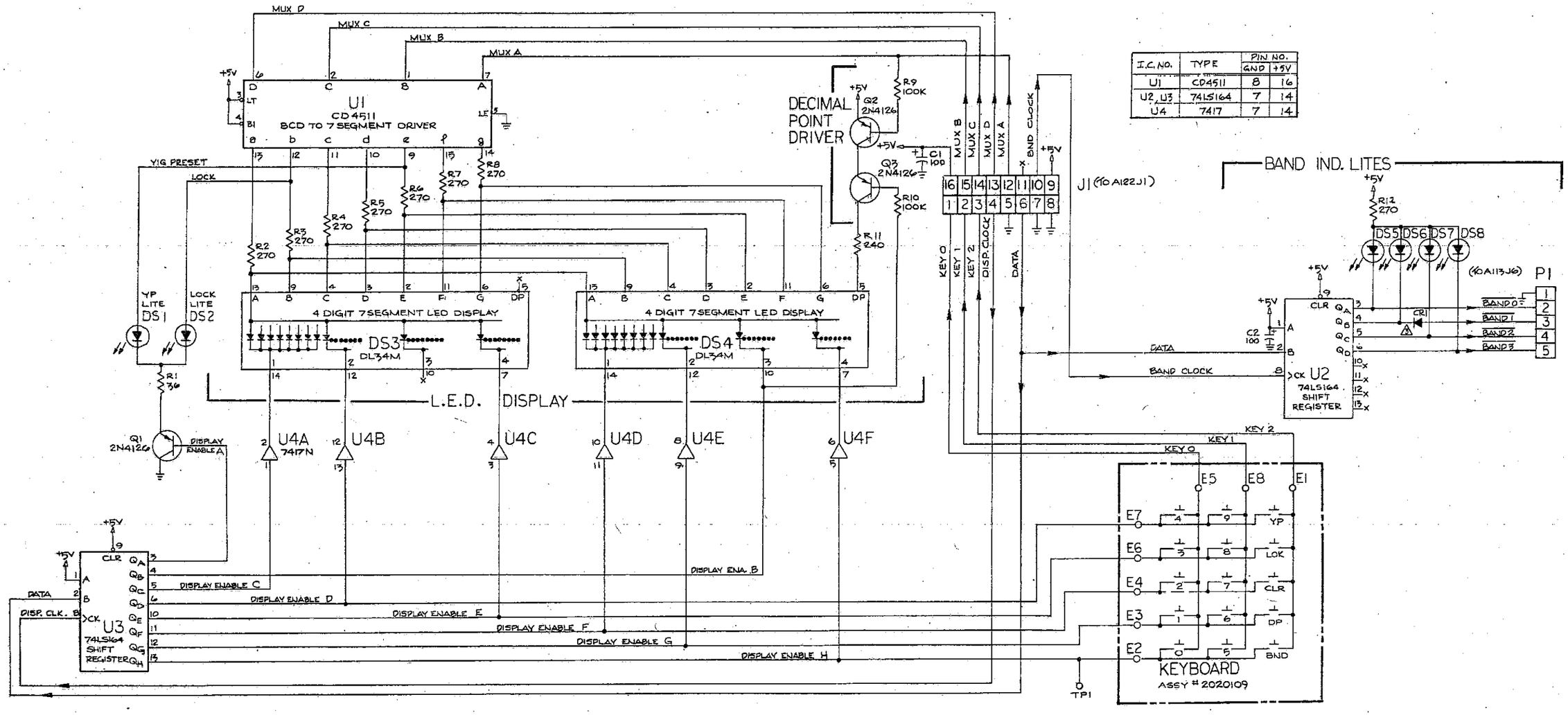
The keyboard display scan consists of a set of clock and data pulse pairs generated by the microprocessor on A122. The clock and data signals enter via J1, and drive U3 pins 8 and 2 respectively. Each scan sequence consists of eight clock pulses, with the data input being low for the first pulse, and high for all other pulses. The data low is shifted down the shift register from Q(A) to Q(H), sequentially enabling eight components of display. The first step, which enables either the YIG PRESET or LOCK indicator, is about three times longer than that for the remaining display digits, to equalize the apparent brightness of the different types of displays.

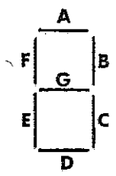
Each display digit is lit by the MUX A through MUX D information. The MUX data is changed from a blank display character to the desired display character shortly after the enable is turned on, and changed back to a blank character shortly before shifting the enable to the next desired character. For those digits which are to be blanked, the blank character is simply left on the MUX line during the enable time.

The keyboard data entry is examined at each of the enable times. Since all three key lines have pull up resistors internal to the ROM input port, they are all high unless a key is pressed. When a key is pressed, the low level from the scan shift register (U3) is connected through the keyboard to one of the key lines. The status of U3 is compared to the key line input data, and the selected key is decoded. If two or more keys are pressed simultaneously, the keyboard data is decoded as invalid, and is ignored.

Band select data is sent out each time the BAND SELECT key is pressed. The local band select is programmed by four clock and four data pulses. The band select data is is negative logic data — that is, a low on the appropriate band select line lights the BAND SELECT indicator, and selects the local band. Since a remote band selection could be different than a local band selection, the band select data is sent out twice each time the band is changed. Local band data is sent out, then the existing band select data is read and sent out. If the counter is in the local mode, the two band selects will be the same. If the counter is in the Remote mode, the second band select data will match the remote band selected.

I.C. NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1	CD4511	8	16
U2, U3	74LS164	7	14
U4	7417	7	14





△3 EIP P/N: 2710016.

FIGURE 9-21B
SCHEMATIC DIAGRAM
AUXILIARY DISPLAY (A123)

108A