If the STORE button is pressed, the control logic is locked at the next 'store full' signal and the effect of further trigger pulses is inhibited. If the STORE button is again pressed the control logic allows one single triggered write sweep but if the RELEASE button is pressed, the trigger inhibition is removed completely. Typical operation is shown in Fig.8 for the 200μs/cm range. The increasing count in the address counters is represented as a ramp. The read/write interlace applies for time base ranges 100μs/cm to 20s/cm. Alternate clock pulses are used for read, leaving the remaining alternate periods available for write entry if called for by the range divider. Fig.9 shows this sequence for range 8.(200μs/cm). The initial addresses for this diagram are chosen at random but the subsequent sequence is relevant.

On range 6 and faster, the maximum writing speed of the store is used (550μs per address), and the control of the store address lines is passed to the write address counter for the time required to enter the 1024 new data words. The read system then holds-off trigger pulses until two reading sweeps have taken place.

4.5.2 OPERATION IN THE ROLL MODE

A block diagram of the system in the Roll mode is shown in Fig.10. The read and write counters are clocked as for the refreshed mode, and the 'data in' latch, store, data and latch, and address selectors function in exactly the same way as for the Refreshed mode. The essential differences are:

a) The display sweep is started from parity between the read and write address rather than from zero read address. This gives the effect of a moving display.

b) Data is entered continuously and trigger pulses have no effect until operation of the STORE button enables a trigger pulse to initiate a STOP sequence.

To generate the concidence signal which initiates the display sweep, the 10 address lines of the write and read address counters are connected to an eight bit and two bit comparator whose outputs are taken to a two input NAND gate. When the same address is present on the counters the gate output goes low and after a short delay the display ramp is started. As can be seen

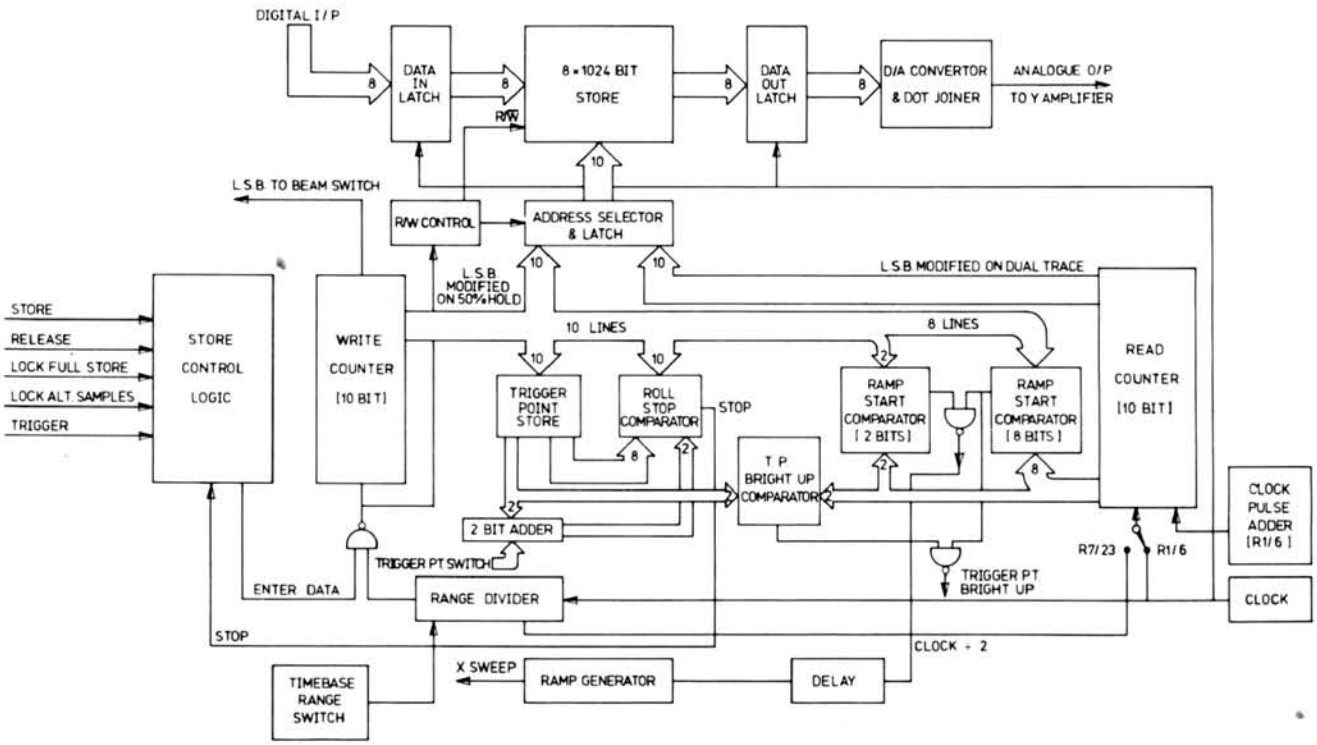

Fig.10 Logic Block Diagram: Roll Mode

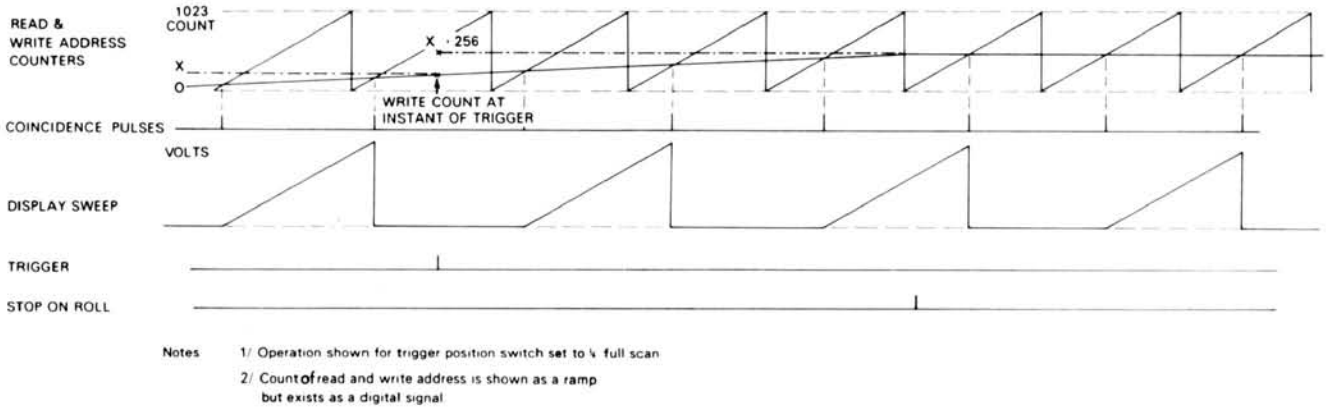

Fig.11 Timing Diagram: Roll Mode

from Fig.11, the write address counter is stepped-on at a slow rate determined by the range divider while the read address counter is stepped at a fixed fast rate. The comparator output occurs at the address where new information is being written into the store, and the displaying sweep started at this point (after a short delay) will display the oldest information first (left hand side of display) and the newest last (R.H.S.) When the Roll mode is selected while released, the store control logic drives the 'enter data' line high, trigger pulses have no effect on the operation of the system and the display follows the incoming data. If the STORE button is now pressed, the store control logic can accept a trigger signal and the address present in the write address counter at the instant of trigger, is held in the ten bit Trigger Point Store latch. The eight least significant bits in the latch are compared with the eight least significant bits of the write address counter. The two most significant bits held in the latch are added in a 2 bit binary adder to a two bit number set up by the Stored Trigger Point switch, before being passed to a two bit comparator to be compared with the most significant two bits of the write address counter.

If the number set up by the switch is 00 the comparator gives an output immediately after Trigger, which acting on the store control logic, drives the enter data line low, stopping any further information being written into the store. If the number set up by the switch is 01 (¼ full count), 10 (½ full count) or 11 (¾ full count), the write address counter must count on this amount before the comparator will generate an output and stop the entry of information. As the write address counter is now stable, every display sweep will be started at the same store address, and therefore the displayed waveform will be stationary.

4.5.3 CLOCK GENERATOR

The clock oscillator consists of TR602–TR603 connected as an emitter coupled oscillator, C601 being adjusted to set the frequency to 9.09MHz. TR601 is a buffer enabling the oscillator to drive the clock lines of the two dual bistables, IC's 610, 602. These are connected as a four stage shift register, but with the first input (pin 2, IC610) controlled from the output of a four input NAND gate, IC603 b, whose inputs are connected to all four bistables. Therefore the input to the shift register cannot go high until all Q outputs are low, and will go and remain low while a single high state is propagated down the shift register. The outputs from the bistables are inverted by IC611, and called P1, 2, 3, 4. P5 is taken directly from pin 8 IC603. The width of a P pulse is 110ns and the period is 550ns.

4.5.4 READ AND WRITE COUNTERS

The write counter consists of two four bit binary counter integrated circuits, IC655, 647 and a dual J.K. bistable package, IC639, connected as a two bit divider. Outputs are labelled B1 (least significant bit) to B10 (most significant bit) on the circuit diagram.

The read address counter consists of two four bit binary dividers, IC's 656, 648, and the dual bistable, IC640, connected as a two bit binary divider. The clock pulse for this counter comes from IC707c, which together with IC707d, a, and IC720b select the P1 pulse on ranges 50μs/cm and above, or the output from the first stage of the range divider on the lower ranges. The least significant bit of this counter (C1) is applied to the selector, IC719, whose output (C1') is connected to the store address selector. If a single trace mode is chosen the $\overline{\text{DUAL TRACE}}$ line operating on IC719 allows C1 to pass to the output. In the dual trace mode, C1 is blocked and the output of gate, IC719a, is determined by bistable, IC723a. This bistable is clocked by the display ramp bistable, such that on alternate sweeps odd and even read addresses are selected.

4.5.5 STORE, INPUT, OUTPUT AND ADDRESS LATCHES

The timing diagram Fig.9 includes details of the events in the 1.1μs period taken by a write and read cycle in the store. First, the ten address lines for the store must

be set and held at a new number, then new input data is set and held on the 'data in' lines. To write in data at this address the R/$\overline{W}$ line is taken low after 110ns for 330ns. True 'data out' is available 500ns after a new read address in set up.
The 'data in' latches consist of IC's 618, 619, which are clocked by the $\overline{P1}$. The address latches (IC's 652, 644, 636) are controlled by a pulse which is positive-going during the last half of the P5 period.
If a write cycle is to take place (Q of IC620a is high) the store R/W line is taken low from the beginning of P2 to the end of P4 period by the P2 and P5 pulses acting on the bistable formed by IC625 c, d. Output data appearing on pin 12 of the R.A.M.'s is held in the 8 bit 'data out' latch consisting of IC650, 659, by the leading edge of a positive-going pulse which is the address latch pulse inverted by IC625.

4.5.6 COMPARATORS

Three comparators are required. These are for 'stop on roll', 'trigger point bright-up' and 'display ramp start'. The circuits used are all quad exclusive NOR two input gates (8242 or equiv.) with open collector outputs. By connecting outputs together, two n bit binary numbers may be compared, and when they are equal the output will go high. These comparators function only in the roll mode.
The 'display ramp start' pulse is generated by exclusive NOR gates, IC654 a, b, c, d, IC646 a, b, c, d, which compare the eight least significant bits of the read and write counter, R618 is the common load resistor and IC638 c, d, compares the two most significant read and write address bits, with R617 as the load. The two outputs are then applied to two inputs of the 3 input NAND gate, IC632C, together with the $\overline{P4}$ pulse which acts as a strobe, allowing the state of the read and write counter to settle before the result of the comparison can pass to the output of IC632C.
The 'stop on roll' output is generated either immediately on receipt of trigger or after the write address counter has counted another quarter, half or three quarters of its full count. This is controlled by the front panel lever switch STORED TRIGGER PT. S602. When a trigger signal is received, the P5 pulse immediately following the trigger signal is gated by IC605d, and acts as a clock pulse on the ten bit latch, IC613, 621, 629, the inputs of which are connected to the write address counter. Therefore the write address set up at the instant of trigger is held in this latch.
The eight least significant bits held in the latch (outputs IC613, 621) are compared with the eight least significant write address bits, by IC614, a, b, c, d, IC622, a, b, c, d, whose common load is R627. The two most significant bits stored in the latch are applied to the two bit binary full adder, IC631, together with a two bit binary number derived from the front panel switch, S602. The result of this addition is applied to the comparators, IC623, a, b, and compared with the two most significant bits of the write address register. IC623d which compares the P1 pulse with 0V is also connected to the common output load R627. If the number set up by S602 is 00 there will be an immediate equality between the write address number and the latch number, so that during P1 period the comparator output will go high. If S601 sets up 01 so that the number held in the latch is increased by one quarter of the full count before being applied to the comparators, the write address counter will have to count on for a quarter of its full count to generate an output. Similarly the output is delayed by half or three quarters full count for the other positions of S602.
The number set up by S602 can be reduced to zero by gates IC606, b, c, when their inputs are driven high. This is done during the trigger enable sequence described in section 4.6.3.
To generate the 'trigger point bright-up' the read counter is compared with the number held in the trigger point store. The eight least significant bits are already compared in IC654, a, b, c, d, and IC646, a, b, c, d. The two most significant bits are compared by IC638, a, b, with R619 as the common load. The output of IC654, 646, and the output of IC638, a, b, are taken to two inputs of a three input NAND gate, IC632b, the third input of which goes high when both inputs of IC630a are high. The trigger point is only marked when the roll mode is selected and the STORE l.e.d. is illuminated.

4.5.7 RANGE DIVIDER

The divider consists of a multi-decade divider package, IC711 (Mostek 5009), and a dual distable, IC722, connected as a $\div 2 \div 4$ stage. P1 and P4 pulses applied to the cross-connected gates IC728 a, b, cause the output of 728a to go high from the beginning of P1 to the beginning of P4. The output of 728b is complementary. Output 728a is used to clock 722a, a J.K. bistable with J. and K. high, changing its output on the negative going edge. The Q output of 722a is used to clock 722b where J. and K. input are also high. Therefore the Q output of 722a is a square wave of half the P pulse frequency (0.909MHz) and the Q output of 722b is a square wave of one quarter the P pulse frequency (0.455MHz). The outputs from 728b, 722a, 722b, are applied to the selector, IC717c, IC706 a, b, c, which is driven from the timebase range switch via the inverters, IC705d, e, f.
The state of the three control lines, 9L, 12L, 15L, for all ranges is shown in the following table. For example when the timebase switch shorts 9L to ground, output 705d goes high enabling the output from 722a (0.909MHz) to pass to IC717. Only one line out of three is shorted on any range, the other two being high. In this particular case, outputs 705f, e, will be low and will drive the output of 706b, c, high. Therefore only the 0.909MHz signal will appear at output IC717c. This output is used to clock the decade divider, IC711. This is an M.O.S. device and requires a −12V line which is derived from the −20V line via R795 and D711. The division ratio of this IC is set by the three lines controlled by the timebase switch, (16L, 10L, 6L) as shown in table overleaf.

Range	Range No.	Range Divider Ratio	Range Divider Control Lines L16	L10	L6	L15	L9	L12
1μs/cm	1	1	0	0	0	0	1	1
2μs/cm	2	1	0	0	0	0	1	1
5μs/cm	3	1	0	0	0	0	1	1
10μs/cm	4	1	0	0	0	0	1	1
20μs/cm	5	1	0	0	0	0	1	1
50μs/cm	6	1	0	0	0	0	1	1
100μs/cm	7	2	0	0	0	1	0	1
200μs/cm	8	4	0	0	0	1	1	0
500μs/cm	9	10	1	0	0	0	1	1
1ms/cm	10	20	1	0	0	1	0	1
2ms/cm	11	40	1	0	0	1	1	0
5ms/cm	12	100	0	1	0	0	1	1
10ms/cm	13	200	0	1	0	1	0	1
20ms/cm	14	400	0	1	0	1	1	0
50ms/cm	15	1000	1	1	0	0	1	1
100ms/cm	16	2000	1	1	0	1	0	1
200ms/cm	17	4000	1	1	0	1	1	0
500ms/cm	18	10,000	0	0	1	0	1	1
1s/cm	19	20,000	0	0	1	1	0	1
2s/cm	20	40,000	0	0	1	1	1	0
5s/cm	21	100,000	1	0	1	0	1	1
10s/cm	22	200,000	1	0	1	1	0	1
20s/cm	23	400,000	1	0	1	1	1	0

The output from the decade divider is taken via the buffering inverters, IC705, a, b, to the clock input of the bistable, IC718a. The output of the range divider takes various positions relative to the system clock depending on the division ratio selected. IC718, a, b, is used to re-clock the divider output pulse at P2. The decade divider output makes IC718a Q go high, driving high the J. and K. inputs of IC718b. The next P2 pulse allowed through the gate IC706d, will set Q IC718b high, $\overline{Q}$ IC718b low thus clearing IC718a. IC718b is cleared by the P3 clock pulse. Therefore IC718b Q is high for the P2 time after an output pulse from the range divider. These pulses are applied through gate, IC732c to the write address counter.

4.5.8 DISPLAY RAMP START AND STOP

Ramp Start Selection

The ramp start pulse is generated either by the most significant read address bit (Refreshed Mode) or by the ramp start comparators, IC654, 646, 638 acting on IC632c (Roll Mode). One of these two signals is selected by the selector, IC740, a, b, c, d, and appears at the output of IC740d. Selection is controlled by IC728c and IC717a. In the refreshed mode the ROLL line is low, driving the output of IC728 high and passing the most significant read address bit through the gate, IC740. The other input to IC728 controlled by IC717, can have no effect. In the Roll mode, for the output of IC728c to go low and select the signal from the ramp start comparators, the output of IC717a must also be high. It can be seen from the input connections of IC717a that on the fastest ranges (1/7) if the STORE l.e.d. is not lit and the 100% HOLD button not pressed, the output of IC717a will be low, forcing IC728c output high, resulting in the ramp start being derived from the read counter. This is necessary since on the fastest ranges the read and write counters are being clocked at the same frequency and therefore would never become coincident. When the STORE l.e.d. is lit or the Lock Full Store button pressed, the write address counter is not counting and coincidence pulses will again occur and can be used to start the displaying ramp.

Ramp Start Delay

The selected output is used as the clock input to the monostable pulse generator circuit consisting of a J.K. flip flop, IC741a, TR715, R771/772 and C718. In the quiescent state, Q of IC741a is low, TR715 is off and its collector load, R772, pulls the 'clear' input of IC741a high. Conditions around IC741a are:- Clear and 'preset' are high, J is high and K is low. A negative transistion on the clock input will cause the Q output to go high and the $\overline{Q}$ output to go low. This negative step is transmitted via C718 to the base of TR715, driving it negative by about 3V w.r.t. ground, but the current through R771 charges C718 eventually pulling the base of TR715 above ground potential and turning on TR715. The delay time is therefore set by R771 and C718. The collector of TR715 goes low, applying a 'clear' input to IC714a to drive $\overline{Q}$ high and Q low. C718 is rapidly charged via the base-emitter junction of TR715, but as the charging current falls to zero, TR715 again turns off, thus returning the circuit to its original condition.
Monostable, IC741a, does not perform a delaying function. In the ROLL mode, because the result of the comparison between read and write counters is strobed by P4 to allow for settling times, but the read counter is being clocked on most ranges at one half the clock frequency, the ramp start output consists of a pair of pulses. The delay set by IC741a is sufficient to ensure that the second pulse of the pair is ignored.
The negative transistion at $\overline{Q}$ IC741a caused by the first ramp start pulse, is used as the clock input to an identical circuit, IC739a, TR717, R794, R793, C714, which generates a pulse width of approximately 2μs.

Ramp Stop

The Q output of IC739a acting through IC717b and IC728d turns on TR718 for this period, driving the 'clear' input of the display ramp bistable on the timebase p.c.b. (IC903b) low, thus ending the displaying ramp if it is running at that time.

Ramp Start

The negative transition at Q–IC739a when it returns to the quiescent state, clocks IC739b, a J.K. flip flop connected as a divide by two. Assume that the clock pulse drives Q–IC739b from low to high. The 'clear' inputs to IC741b and IC742b are now removed and IC742b can respond to pulses on its clock input. These are the gated P4 pulses used as sample-and-hold pulses for the dot joiner circuit, and can be at full clock rate, half clock rate or quarter clock rate depending on timebase range and single/dual trace operation. The first P4 pulse incident on the clock input of IC742b after the clear input has been removed, will drive Q–742b high, and the second will drive Q–742b low, $\overline{Q}$–742 high $\overline{Q}$–741b low, which makes the J & K inputs of IC742b

both low, preventing further clock pulses having any effect. The low/high transition of $\overline{Q}$–IC742b acts as the ramp start pulse through connection N/M16 and gate, IC904d, on the clock input of the ramp start bistable, IC903b.
The next ramp start pulse from the read counter or comparator system will, via monostable, IC741a, drive IC739a to the opposite state, i.e. Q high to low. Thus $\overline{Q}$–IC741b is returned to the high state, $\overline{Q}$–IC742b is held in its high state and cannot generate a ramp start signal. Therefore the ramp start signals are divided by two, but the ramp stop signals are not. The generated sequence of signals is:- STOP START – STOP – STOP START – STOP – STOP START, etc. The STOP signal immediately prior to the START signal has no effect as the displaying ramp is not running at that time.

Read Counter Clock Pulse Adder
On ranges 1/6 in the Roll mode before the STORED condition is reached, the write address counter is in control of the store address lines and the read address counter does not determine the address of the information read out into the 'data out' latch. The information held in this latch is that which has just been written into the store. If the front panel controls have been set to call for dual trace operation (CH1 and CH2 operation or LOCK ALT. SAMPLES) the dot joining circuit will receive a sample-and-hold pulse at one half the clock rate (the least significant bit of the read address counter acts on gates, IC725a, b, and IC732a, to allow only every other P4 pulse through to drive the dot joiner sample-and-hold cct). To prevent this pulse from sampling the information in the same set of alternate addresses on every displaying sweep, an extra clock pulse is inserted into the read address counter input after every other full count. This ensures that the sample-and-hold pulse samples even address information on one displaying sweep, and odd address information on the next sweep and so on. This extra pulse is generated by IC721, and IC720.
Bistable, IC721a, is connected as a binary divider, with the clock input taken from the most significant read address bit. On every other full count output from the read address counter, Q–IC721a goes low clocking the binary divider, IC721b, driving its Q output high, and allowing the next P3 pulse via IC720a to pass gates, IC720c, IC720b and IC707c, to appear as a clock pulse at the input of the read address counter. The following P5 pulse acts on the 'clear' input of IC721b to return its Q output to ground and close gate, IC720c.

4.6 MODE CONTROL

4.6.1 DISPLAY MODE LOGIC

The switch, S601, has three positions, Normal, Refreshed and Roll. When the timebase range switch is set between the 500ms/cm and the 1μs/cm range the pole of S101a is connected to ground via S6, so that in the up position the l.e.d. indicating normal operation, D601, is lit, the centre position illuminates D602 (Refresh indicator) and the bottom position illuminates the roll indicator, D603.
When the timebase is set between ranges 1s/cm to 20s/cm the pole of S601b is grounded so that in the up position, D602 is illuminated indicating that the refreshed mode is operating. Outputs from this switch to the control logic are on 7H ($\overline{NORM}$) and 5H ($\overline{ROLL}$).
One of the l.e.d.'s, D601, 602, 603, is always lit unless the STORE l.e.d., D717, is on, in which case the base drive to the p.n.p. transistor, TR701, is removed and no current can flow through R609 to these l.e.d.'s.

4.6.2 HOLD

Output pulses from the range divider must pass through the three input gate, IC732c, to the input of the write address counter. The Lock Full Store push button, S703a, drives a slave bistable, IC702a, d, for switch de-bouncing. When the button is pressed the input of invertor, IC727d, goes high, putting a low on one input of IC732c, cutting off this gate.
The LOCK ALT. SAMPLES button, S704a, driving a similar bistable, IC701a and d, puts a low on IC707c, blocking the signal from the least significant write address bit (B1) and driving the least significant write address line ($\overline{B1}$) permanently high. Half the contents of the store cannot now be addressed by the write counter, but will continue to be displayed. Action of the dot joiner requires that if single channel operation is in progress, two display traces must be established, one the held information and the other the current information.
IC701a and d, drives high both inputs of the open collector gates IC735, so that the DUAL TRACE line is pulled low. This causes the least significant bit of the read address to come under the control of the display ramp bistable such that alternate sweeps display odd and even store locations as for any dual trace display.

4.6.3 STORE AND RELEASE

Fig.12 shows a simplified section of this part of the complete circuit of Fig.23.

Operation in the Refreshed Mode
Assume that the RELEASE button has been pressed. Bistable, IC708a and IC726a, are cleared, $\overline{Q}$–IC726a is high so that the ARMED l.e.d., D716, is off, and Q–IC708a is low applying a low input to the two gates, IC733a and IC732b, driving their outputs high, so that the TRIGGERED and STORED l.e.d.'s are off. The output of IC732b (high) drives on TR701 via IC702b so that l.e.d., D602, controlled by the mode switch, S601, is lit. The gate, IC731c, has two high inputs, $\overline{Q}$–IC708a and the $\overline{ROLL}$ line, so that its output is low. This turns off IC713b so that its output will rise if the "wired or" gate, IC713c, is also off. This gate is controlled by the two sweep hold off system, IC723a, b (described later) and may be assumed to be off in this section. Consequently the trigger enable line is always high after the RELEASE button has been pressed.
When the STORE button is pressed bistable, IC726a, is clocked such that $\overline{Q}$ goes low turning on the ARMED l.e.d. Gate, IC731b, now has two high inputs, Q–IC726a and Q–IC726b (this bistable is held preset by the ROLL

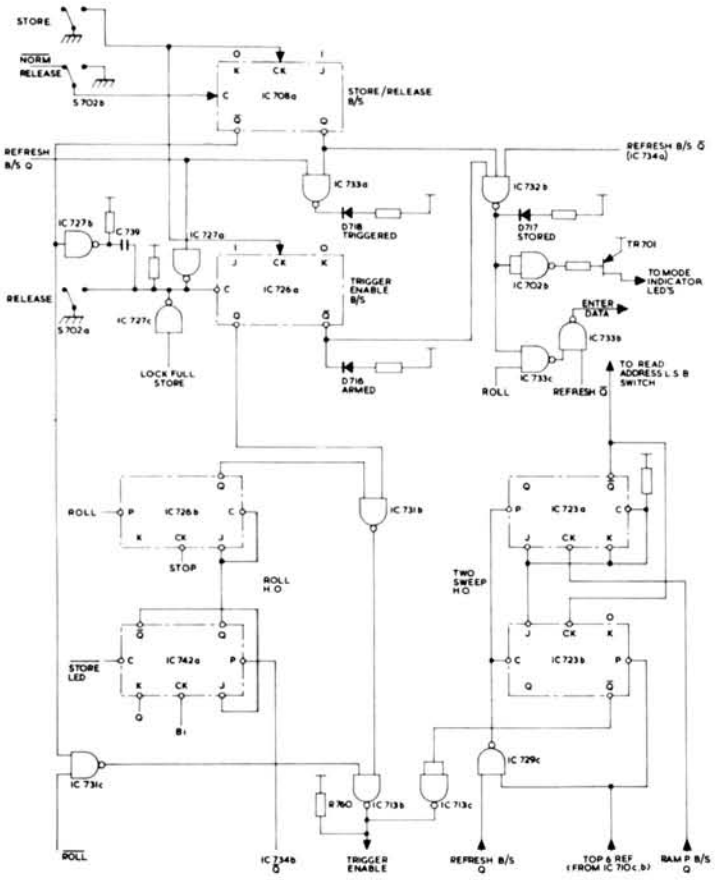

Fig.12 Simplified Control Logic

line being low), and so its output is low. This, acting on IC713b, holds its output high as before. The action of pressing the STORE button also clocks bistable, IC708a, such that the $\overline{Q}$ goes low driving high the other input to IC713b via IC713b. The result is that the trigger enable line is still high but this is now conditional on the state of the trigger enable bistable, IC726a. The gate controlling the TRIGGERED l.e.d. now has one high input (Q–IC708a) and one low input (Refresh B/S–Q) so that this l.e.d. is still off. The gate controlling the STORED l.e.d. has two high inputs (Refresh B/S–$\overline{Q}$ and Q–IC708a) and one low input ($\overline{Q}$–IC726a) so this l.e.d. is also off.

When a trigger signal occurs, the refresh B/S–Q goes high and this operating through invertor, IC727a, on the 'clear' input of IC726a, resets it, turning off the ARMED l.e.d., D716. The gate controlling D718 now has two high inputs so this l.e.d. (TRIGGERED) is lit. The gate controlling the STORE l.e.d., IC732b, now has two high inputs (Q–IC708a and $\overline{Q}$–IC726a) and one low input ($\overline{Q}$–Refresh B/S), so the l.e.d. is off.

On completion of a writing sequence the RefreshQ output will go low, turning off D718 and turning on D717, the STORED l.e.d. It also turns off TR701 and extinguishes the Refreshed Mode indicator l.e.d. D602. Q of IC726a going low, drives the trigger enable line low via the two invertors, IC731b and IC713b.

Pushing the STORE button again will clock Q–IC726a to the high state, so driving the trigger enable line high until another trigger signal is accepted. Pushing the release button sets $\overline{Q}$–IC708a high, driving the trigger enable line permanently high via gates, IC731b and IC713b.

Two Sweep Hold-Off Circuit

This circuit only operates in the refreshed mode on the timebase ranges 50μs/cm to 1μs/cm.

On these timebase ranges it is necessary that the writing sequence interrupts the reading sequence (this is described in section 4.5.1). If the system were allowed to respond to rapid trigger pulses, no full reading of the store would occur resulting in a blanked display. To prevent this, after every writing sequence the trigger enable line is held low until two reading sweeps have taken place.

Under all other conditions the line, TOP6 REF, will be low, presetting bistable, IC723b, and applying a permanent low to IC713c turning off this half of the "wired or" gate, so that the state of the trigger enable line is controlled only by IC713b.

When the TOP6 REF line is high, the preset input is removed from IC723b. When the refresh B/S–Q is set high by a trigger signal at the start of a writing sequence, the output of gate, IC729c, will now go low setting the $\overline{Q}$ output of IC723b high and the Q output of IC723a high. IC713c is now turned on and the trigger enable line pulled low. The display ramp B/S–Q will go low on the completion of the current reading sweep, but this cannot clock IC723a because of its preset input.

No more display ramp sweeps take place until the end of the writing sequence. When the refreshed Q goes low, displaying sweeps can again occur. The output of IC723a will change at the end of every display sweep (this output is used to generate the l.s.b. of the read address when dual trace operation is called for), and after two sweeps, the $\overline{Q}$ output of IC723a going negative acts as a clock pulse on IC723b setting $\overline{Q}$ low and therefore making the trigger enable line high by turning off IC713c.

Operation In The Roll Mode

Operation of the ARMED, TRIGGER, and stored l.e.d.'s is the same as for the refreshed mode previously described. The action of the trigger enable is as follows:-

Assume the RELEASE button has been pressed so that $\overline{Q}$–IC708a is high, $\overline{Q}$–IC726a is low, and also that the output of the roll hold-off circuit, $\overline{Q}$–IC726b, is high (this is described later). The $\overline{\text{ROLL}}$ line being low drives high the output of gate, IC731c, and Q of IC726a acting through inverter, IC731b, also applies a high input to IC713b, turning on this gate and driving low the trigger enable line. As the STORE l.e.d. is off, IC733c has two high inputs thereby applying a low input to the 'enter data' gate, IC733b, forcing its output high so that data is written into the store continuously. Trigger signals will have no effect until the STORE button is pressed. This sets Q–IC726a high, and via the two inverters, IC731b and IC713b, sets the trigger enable line high. The ARMED l.e.d. is also illuminated. When a trigger signal sets the refreshed B/S–Q high bistable, IC726a, is reset