OS4001
OUTPUT UNIT

Instruction Manual

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Contents

Introduction

Section 1

The 4001 option is designed to be added to a standard OS4000 Digital Storage Oscilloscope to enable the information in store to be retransmitted in both analogue and digital form. Two analogue outputs are provided, and these are intended primarily to drive strip chart and X-Y recorders. Channel 1 and 2 signals are available simultaneously at a read-out rate which can be varied to suit the chart recorder, with a slowest time of 200 seconds representing the 10 division display. In addition, a corresponding X-ramp signal is provided for X-Y recorder use. The unit also incorporates relay contacts for pen lift or chart motor control. There is a variable delay between the closing of these contacts and the start of read out which can be preset to allow a chart drive motor to accelerate.

A socket on the rear panel presents the output information in digital form as two eight bit parallel signals for Y and one ten bit parallel signal for the X ramp. Control facilities for remote start and continuous readout are also provided. The latter can be used for continuous generation of a recorded transient or frequency shift of recorded waveforms.

Specification

ANALOGUE OUTPUTS Via B.N.C. connectors

Channels 1 and 2

Amplitude	100mV per cm of screen height. Bipolar with 0V corresponding to middle of screen
Accuracy	Output voltage per cm of display ± 3% Output to input voltage (cal) ± 3%

X Ramp

Amplitude	100mV per cm of screen width. Positive ramp resetting to 0V
Accuracy	Output voltage/cm of display ± 3% Output voltage/unit time recorded ± 3%

Time output accuracy of Y Channel outputs ± 1%
(Record to replay ratio)

Output Impedance CH1, CH2 and X-ramp 100Ω/0.1μF
Continuous short circuit protected

DIGITAL OUTPUTS Via back panel socket

All outputs true binary from open collector T.T.L. buffers

Channels 1 and 2		8 bit parallel, negative logic
X Ramp		10 bit parallel, negative logic
Accuracy	Y Channel	full scale = 9cm of display ± 5%
	X Ramp	full scale = 11.3cm of display ± 5%

READ OUT RATE
Set on OS4000 timebase range switch
Range 20sec/cm to 200μs/cm
Read-out bandwidth D.C. – 16kHz (–3dB)

CONTROLS
Front panel start button to initiate single read-out cycle.
Remote start by T.T.L. low or contact closure to ground.

Remote continuous read-out by T.T.L. low or contact closure to ground.

Delay	Delay between start command and initiation of read-out cycle set by front panel preset control from < 20msec to > 1 sec. (10μsec. to 10sec. by internal component change)
Contacts	Front panel access via 4mm sockets to isolated single pole contact which closes from start command to end of read-out cycle Contact rating 200V D.C. 0.5 A D.C. 10W D.C. Isolation 400V max.

OUTPUTS

Clocks 1 and 2	Negative T.T.L. pulses, 100nsec. duration marking the change of each digital word.
Read-out Marker	T.T.L. low, commencing at the end of delay, for the duration of the read-out cycle.

TEMPERATURE RANGE as OS4000

SUPPLY derived from OS4000

DIMENSIONS 3.75cm extra height to OS4000

WEIGHT 570gm extra (1¼ lb) to OS4000 approx.

ACCESSORIES 36 way plug Amphenol 57–30360
2 x 4mm plugs
Handbook PN 36896

3.1 ANALOGUE OUTPUTS

The 4001 may be used to drive strip-chart, T-Y or X-Y recorders. Both Y channels are available simultaneously for chart recorders with two pens. Alternatively, the two channels may be reproduced sequentially on single pen recorders. A synchronised X-ramp is available to drive X-Y recorders as Y-t. Alternatively, the CH1 and CH2 outputs can drive an X-Y display directly.

The internal contacts can be used to control chart motor and/or pen lift if required.

3.2 CHART RECORDER SPEED

The 4001 offers a very wide range of read-out rates to suit the recorder being used. The rate should be chosen by considering the following:

1) A slow read-out rate, while faithfully reproducing the stored signal, will also show the discrete levels in the output waveform, (there is no dot-joining on the 4001 outputs). A faster read-out rate and chart recorder speed will tend to smooth the output waveform.
2) If too high a read-out rate is chosen, the chart recorder may be unable to follow any large amplitude fast change of the signal. This is slew-rate limitation of the recorder.
   The optimum read out speed for any particular stored waveform is thus the maximum at which the chart recorder is capable of tracking the signal. This may be determined by increasing the readout/chart recorder speed each sweep until waveform degradation can be observed.
   The bandwidth of the output amplifier is d.c. to 16kHz (−3dB) which is well above the limitation of most chart recorders. However this limitation may be reached if the output is required for other purposes when the replay frequency is a function of recorded waveform and replay rate.
   (See Function Generator)

3.3 DRIVING A CHART RECORDER

1) Connect to the CH1, CH2 and X-ramp sockets as required. In single trace operation, the same signal will be present at CH1 and CH2 outputs.
   Set the sensitivity of the chart recorder inputs to accommodate ± 400mV f.s. on CH1 and CH2 and 0 to 1V on the X-ramp.
   When the 4001 is not reading out, the CH1 and 2 and the X-ramp outputs return to 0V. Ov on the Y-channel output corresponds to mid-screen on the OS4000 display and thus the chart recorder pen should be set to mid-scale unless specifically required otherwise.
   The X-ramp moves positive from 0V and thus the pen should be positioned to allow at least 1V positive travel.
2) Connect, if required for remote start/pen lift.
   NOTE: The relay contacts are unprotected and inductive loads should be suppressed to stay within the contact rating.
3) The delay time (from closing of relay contacts to start of read-out) is set by a front panel screwdriver preset. The minimum delay time of < 20ms is sufficiently short for recorders for which no delay is required. The preset control range allows the delay time to be set to a maximum of 1 second but this can be increased to approx. 10 sec. by increasing the internal capacitor C801 to 15μF.
4) Obtain the required trace on the OS4000 and STORE or LOCK it. If the 50% hold facility is being used, the trace stored by the 50% hold will appear at the CH2 output, the other trace appearing at CH1.
5) Set the required read-out rate on the timebase range switch.
6) Press the start switch to initiate the read-out cycle. Note the display is inhibited during read-out. At slow read-out rates, this will result in a blank screen for considerable periods. Similarly the OS4000 is prevented from accepting new data into the store during this period.
7) At the end of the read-out cycle, reset the timebase range switch as required to record subsequent data.

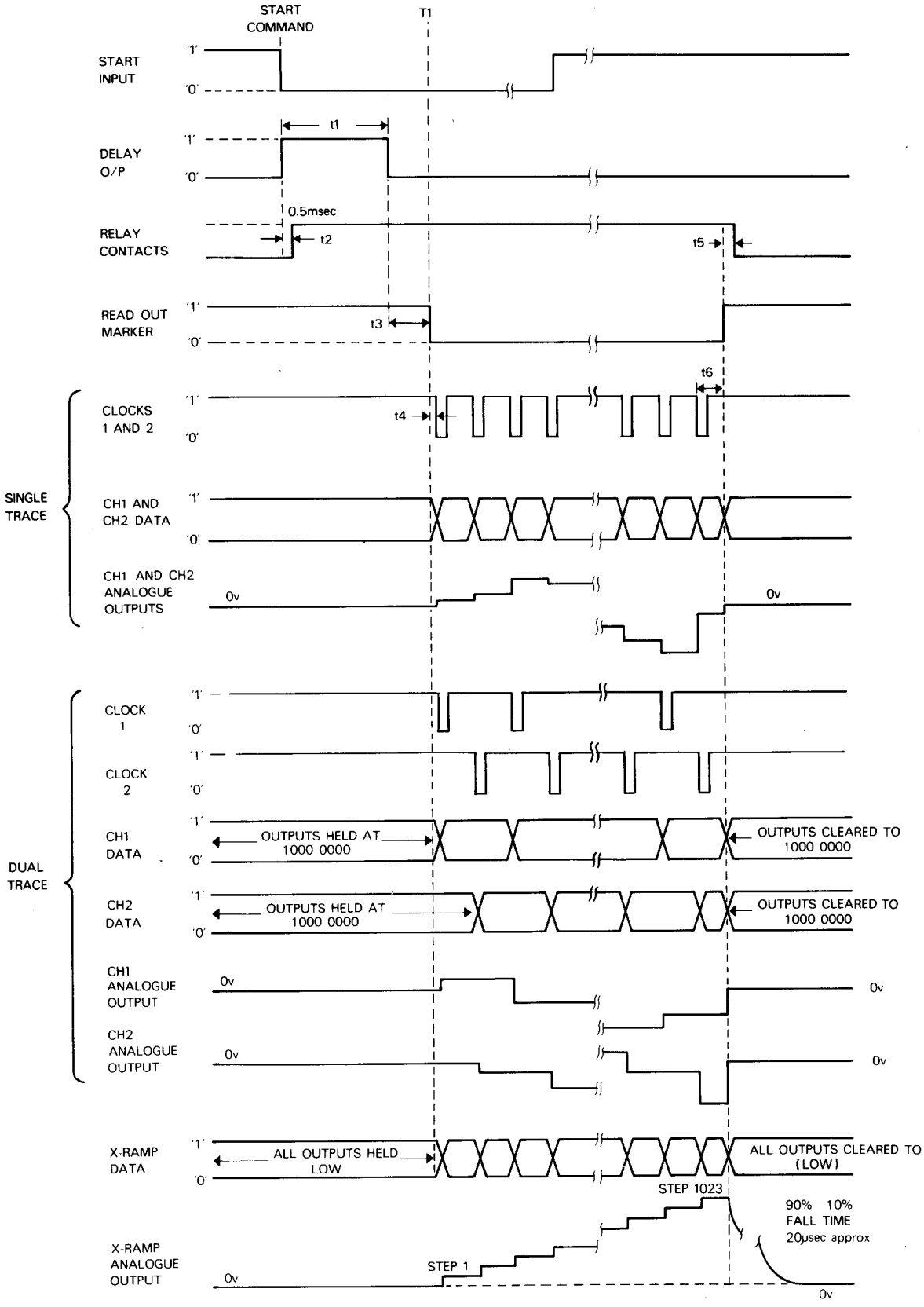
3.4 THE READ-OUT CYCLE

Fig. 1 shows a typical read-out cycle. The cycle is initiated by a negative edge on the start input produced by the push button or by remote start (see section 3.5). The relay contacts close within 0.5msec. of the start command and the preset delay period is started. At the end of this delay, the read-out is primed to start at T1 the end of the current display sweep on the OS4000.

Period t3 has any value from 0 to 1.2msec. depending on when the button was pushed but is unlikely to be a significant delay at chart recorder speeds. If required, the read-out marker, available at the back panel socket SK A.C. pin 2, can be connected to the chart recorder event marker to indicate the exact start of read-out. At the end of read-out, the relay contacts open again within 0.5ms and all analogue outputs return to 0V.

3.5 REMOTE START

The remote start input appears on contact 3 on the back panel socket SK AC. Read-outs may be initiated by a T.T.L. low on this contact or by connecting it to contact 4 which is logic earth. This action has the identical effect to pushing the front panel button.


START COMMAND
T1
START INPUT
'1'
'0'
t1
DELAY O/P
0.5msec
RELAY CONTACTS
t2
t5
READ OUT MARKER
t3
t6
CLOCKS 1 AND 2
t4
SINGLE TRACE
CH1 AND CH2 DATA
CH1 AND CH2 ANALOGUE OUTPUTS
0v
CLOCK 1
CLOCK 2
DUAL TRACE
CH1 DATA
OUTPUTS HELD AT 1000 0000
OUTPUTS CLEARED TO 1000 0000
CH2 DATA
CH1 ANALOGUE OUTPUT
CH2 ANALOGUE OUTPUT
X-RAMP DATA
ALL OUTPUTS HELD LOW
ALL OUTPUTS CLEARED TO (LOW)
STEP 1023
90% – 10% FALL TIME 20µsec approx
X-RAMP ANALOGUE OUTPUT
STEP 1

3.6 FUNCTION GENERATION

Although primarily intended to be used to drive chart recorders, the analogue outputs can be used for other applications. In the continuous run mode, the 4001 acts as a function generator, continuously repeating the one or two waveforms stored.

Thus a single transient can be recorded at one speed and regenerated continuously at another faster or slower speed, within the available stepped range of timebase sweep speeds. (20 sec/cm to 200μs/cm.) As the scan length is approx. 11.5 cm, this range is equivalent to 230 seconds to 2.3ms for a full cycle. For example a slow stimulus into a servo system could be recorded and replayed faster for analysis in an electrical analogue of the servo.

Alternatively functions can be "written" manually on the screen of the OS4000 by use of the shift control or externally controlled input during a very slow scan in the refreshed mode.

Such a single scan can be started by operation of the trigger level control and frozen at any point by the 'Lock Store' button. The latter is necessary at some point during a scan for operation of the X shift control so that the end of scan can be brought on screen. When the 'Lock Store' button is released the scan continues from the point at which it was frozen. To write a second trace in this mode, the Lock Alt. Samples button should be pressed and the writing process repeated. The two patterns will be generated simultaneously from the CH1 and CH2 outputs. Such outputs could be used for XY display on another oscilloscope or chart recorder.

Continuous readout is obtained by shorting Pin 1 on the rear panel socket to Pin 4 (ground).

3.7 DIGITAL OUTPUTS

The chart in Fig.2 shows the digital outputs and controlling inputs available at back panel socket SKAC. These outputs come from open collector T.T.L. buffers without pull-up resistors.

Fig.1 shows a typical read-out cycle. The read-out cycle is initiated by a negative edge on the start input, which triggers the delay period tl. This delay may be set in the range 20ms to 1 sec. by the front panel control or if required it can be reduced to less than 50μsec.by changing C801 to 1000pF.

Read-out will commence at T1, the end of the current display sweep on the OS4000. Thus there will be a period t3, after the end of the initial delay, of 0 to 1.2msec. approx. according to the relative timing of the start command and the OS4000 sweep before the read-out is enabled.

There will be a further delay, t4, between the read-out enable and the first clock pulse, where t4 is dependent upon the read-out rate chosen. For a read-out rate of N sec./cm, t4 will be in the range 0 to N x 11 x 10^{-3} sec,

The problems due to the uncertainty of these delays are reduced (or removed) by clocks 1 and 2, whose negative edges indicate when the data is updated in channels 1 and 2 respectively. These clocks may be used to latch the data at the receiving digital equipment.

CH1 data is shown as changing first when in dual channel operation. This is only in the case when the OS4000 is in the 'Refreshed' mode. In the 'Roll' mode, each sweep does not start at the beginning of store (see OS4000 handbook). This results in an uncertainty as to which channel output will appear first. Again, recourse should be made to clocks 1 and 2.

Pin No.	Connection	
1	Continuous read-out input	
2	Read-out marker	
3	Remote start input	
4	Logic earth (0V)	
5	Clock 1	
6	Clock 2	
7	D1 (Most significant)	X-ramp output
8	D2	
9	D3	
10	D4	
11	D5	
12	D6	
13	D7	
14	D8	
15	D9	
16	D10 (Least significant)	
17	Not connected	
18	Not connected	
19	D1 (Most significant)	Channel 1 output
20	D2	
21	D3	
22	D4	
23	D5	
24	D6	
25	D7	
26	D8 (Least significant)	
27	D1 (Most significant)	Channel 2 output
28	D2	
29	D3	
30	D4	
31	D5	
32	D6	
33	D7	
34	D8 (Least significant)	
35	Not connected	
36	Not connected	

Fig. 2 Connection to Back Panel Socket

4.1 GENERAL

Fig.8 shows the full circuit detail of the 4001.
References of components on the P.C.B. are in the range 800 to 899.
Components in the range 80 to 89 are on the front panel of the 4001.
Interconnection between the OS4000 and the 4001 is obtained by breaking the direct links SKK to SKD and SKA to SKH in the OS4000 and reconnecting SKA to SKAA, SKD to SKDD etc. (see Fig.26 of OS4000 handbook). This provides access to the Y-Channel data and permits OS4000 control signals to be modified by the 4001.

Fig.3 shows a simplified block diagram.

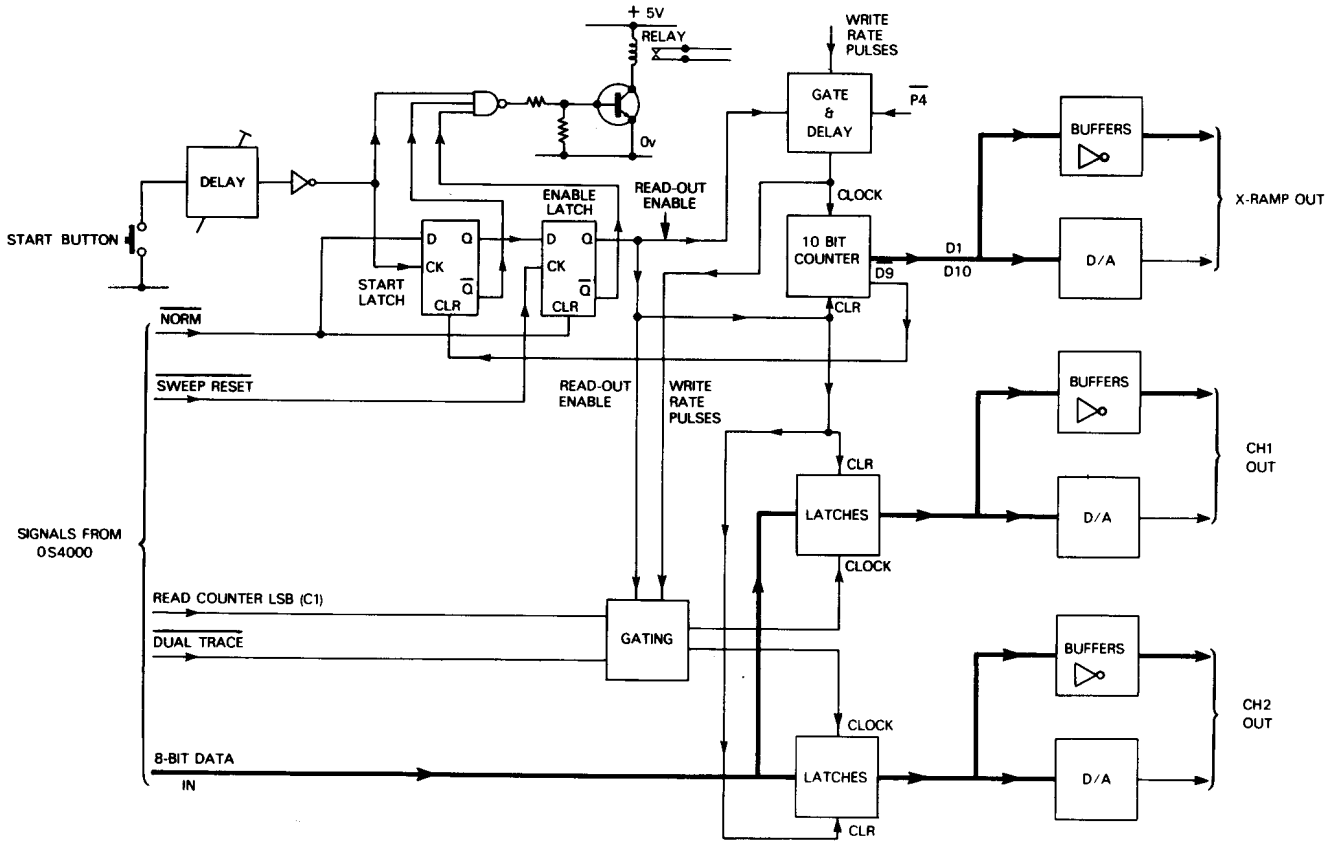


Fig. 3 Block Diagram

In essence, operation of the start button initiates the delay period. At the end of this period the control circuitry is primed to start a read-out at the end of the current display sweep of the OS4000. During read-out, the clock to the OS4000 read address counter is changed to the slower rate determined by the timebase range switch. At the end of the slow read-out scan, the control circuit is reset and the OS4000 returns to normal operation.

(a) CH1 and CH2

Y channel data is obtained from the OS4000 in the form of an 8 bit word as read out from the stores.

Consider the circuit when operating in dual trace mode. Channel 1 information is contained in odd store locations and Channel 2 information in even locations. In order to separate the two channels and present them simultaneously, the incoming data is held in two sets of latches, one clocked on even addresses, the other on odd. The latched information is then passed on to the digital to analogue converters (D to A) and also to the buffers, which protect the internal data from external effects such as short circuits or line reflections. At the end of read-out, the latches are cleared to binary 1000,0000 which produces 0V (mid range) at the analogue outputs.

(b) X Ramp

The X-ramp is produced digitally by a 10 bit counter clocked at each change of data input. The counter is cleared to all zeros at the end of read-out. The output of this counter feeds a third D to A and is buffered as is the Y data for the digital output.

(c) Timing

The start of read-out is initiated by triggering the delay. This immediately energises the relay. At the end of the delay period, the start latch is set, holding the relay and putting a '1' on the D of the enable latch. The next sweep reset from the OS4000 clocks this '1' to the output and enables the read-out.

The start latch is cleared after two clock pulses putting a '0' on the D of the enable latch. The relay is now held on by the $\overline{Q}$ of the enable latch. When the next 'sweep reset' pulse arrives at the end of the slow scan, this '0' is clocked to the output and the read-out enable goes low clearing the Y channel latches and resetting the X-ramp, thus terminating read-out.

The $\overline{\text{NORM}}$ input inhibits read-out when the OS4000 is in the normal mode, by putting a '0' on the D input of the start latch and on the clear input of the enable latch.

4.2 D/A CONVERTERS

The D/A converters, IC821, 822, 823, are similar to those used in the OS4000. The output current produced at Pin 4 is converted into an output voltage by the following operational amplifiers, IC 824, 825, 826. The current injected into Pin 14 of the D to A defines the output scaling, and the external current injected into Pin 4 of the D to A, sets the zero. Each has a preset control to compensate for component tolerances. Both pins are virtual earth points and so the currents can be completely defined by a reference voltage and a series resistor. The reference voltage is provided by regulator, IC827. The resistor and capacitor on the output remove any high frequency pick up. Each channel has a half scale offset current introduced by R848, 849 and R841, 842 such that mid-screen on the display produces 0V out.

The X-ramp operates on 10 bits. The least significant eight are converted to an analogue current by IC821. The two most significant bits are generated separately for current summation at the input of IC824.

These additional binary weighted currents are provided by R822, R823 and R824 representing bit D1, and R832, R833 and R834 representing bit D2.

Transistors, TR802 and TR803, when switched on, reverse bias diodes, D807 and D805/D806 respectively, diverting the current from the summing junction. D804 is included in series with R854 to ensure thermal tracking between the current from IC821 and the two additional currents. IC821 draws a current toward −6V from the summing junction, proportional to the digital input. Correspondingly the two additional currents are normally on when their digital inputs are zero and their total current is balanced by that through R825 and R827.

R824 and R834 adjust the currents representing D2 and D1 respectively. R829 adjusts the overall scaling without changing the matching between the three currents.

4.3 LATCHES AND LATCH CONTROL

Refer to the circuit diagram, Fig.8.

The incoming data stream enters two 4-bit latches in each Channel, IC819, 815 and IC814, 818. The Q outputs are used for all but the most significant bit, which arrives inverted by IC804 (d) and is taken out from the $\overline{Q}$ output. This ensures that at the end of read-out when the clear is taken low and all the latches cleared, the digital information presented to the D/A is binary 1000,0000 which is half full scale (0V at the analogue output).

IC807 gates the clock pulses such that:-

(a) In dual trace or 'Lock alternate samples' mode, information from odd and even locations is clocked into CH1 and CH2 latches respectively.

(b) Information from all store locations is clocked into both channels when in single trace operation.

The operation is as follows:-

The signal arriving at Pins 13 and 2 of IC807 is the clock to be gated. The signal arriving at Pins 5 and 9 is the read-out enable. When low it inhibits clocks to both latches and clears them. When high, it enables clocks.

The input '$\overline{\text{dual trace}}$' is inverted by IC802 (b). In single trace operation it puts a '0' on IC805 Pins 13 and 9 which in turn puts a '1' on IC807 Pins 12 and 1. This allows clocks to reach both Y Channel latches simultaneously, fulfilling condition (b) above.

In dual trace operation or 'lock alt. samples', IC802 Pin 4 is high, enabling the read address LSB to arrive at IC807 Pin 1 and its inverse at Pin 12. Thus when the LSB is High, the CH1 latches receive clocks, when it is low CH2 receive clocks. This fulfils conditions (a).

4.4 X RAMP COUNTER

IC817 and IC820 are each four bit synchronous binary counters and with IC816 are cascaded to form a 10 bit divider. They are cleared to zero at the end of each sweep and stepped with each change of Y Channel data, i.e. following the read address through the read-out cycle.

4.5 DATA SELECTOR

Switches shown with '0' on select.

The data selector, IC808 functions as 4 changeover switches as shown in Fig.4.

The OS4000 normally reads out from the stores at a fixed

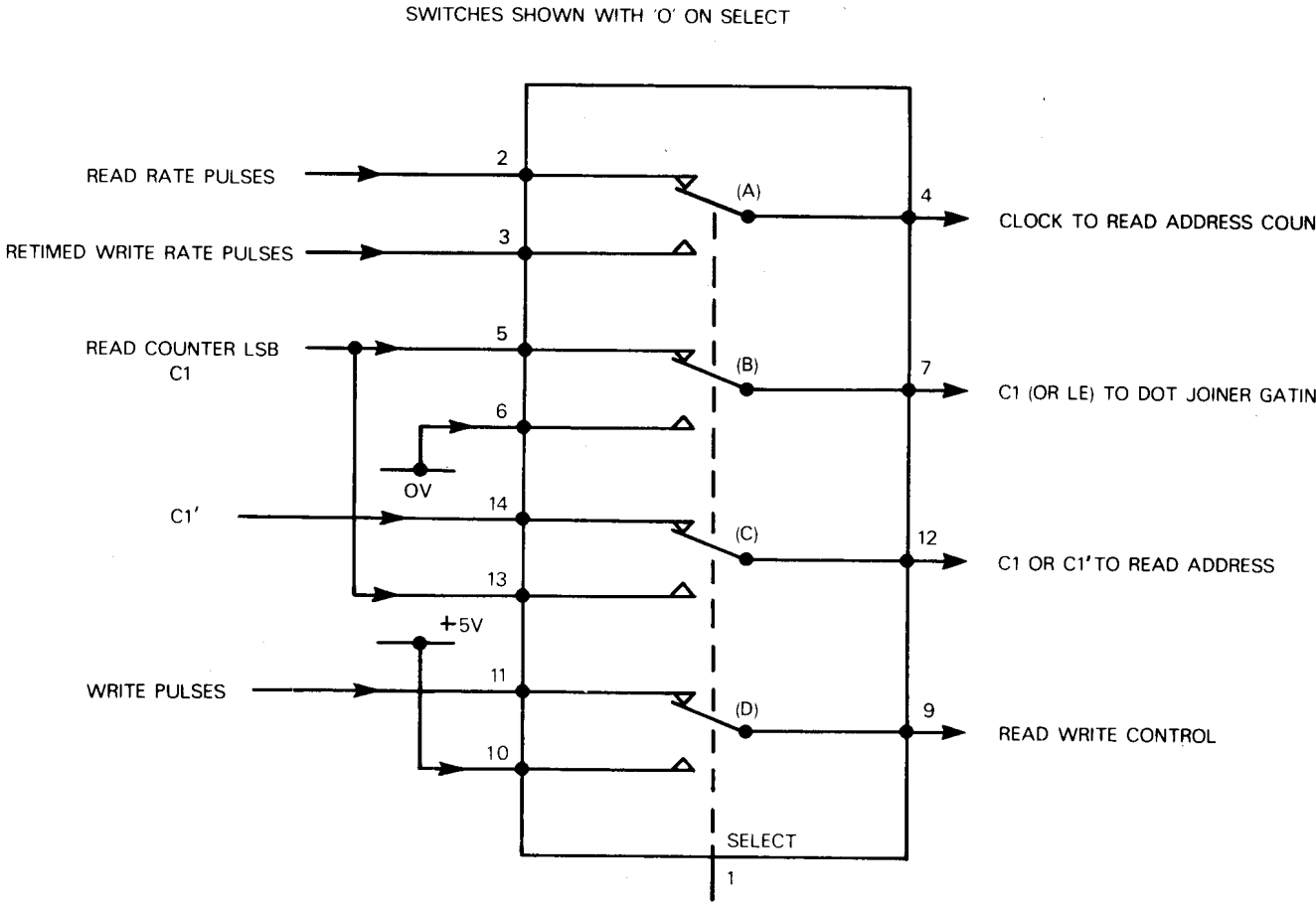


Fig. 4 Data Selector – Mechanical Equivalent

rate. Switch (a) changes this rate to one set by the Time-base switch, i.e. the write-rate pulses. The flip-flop, IC805 (a) and (b), retimes the write-rate pulses from P2 to P1 to drive the read address counter. (See Fig.5.)

In dual trace operation, the OS4000 normally reads even store locations only on one sweep and odd only on the next. (See section 4.5.4 of OS4000 handbook.)

In the read-out mode, switch (c) ensures that the LSB address is taken from C1 rather than C1', retaining read-out from all the store location. Switch (b) sends logic '0' to the dot-joiner gating circuitry of the OS4000 in place of C1 during read-out, while (d) sends logic to the read/write control to inhibit writing into store.

4.6 CLOCK DELAY

Fig.5 shows the retimed write rate pulses which arrive at IC803 Pin 3. These are sent to step the read address counter but there is an inherent delay within the OS4000 before the data changes. Because of this delay of data it is necessary to delay the start of clock pulses to the X-ramp counter and to the Y-Channel latches by three P4 pulses.

The write-rate pulses are entered at the serial input of the shift register, IC812, and clocked through by $\overline{P4}$. Using the output from the third stage of the register produces the required delay. At the end of read-out, the shift register is cleared to zero by parallel loading.

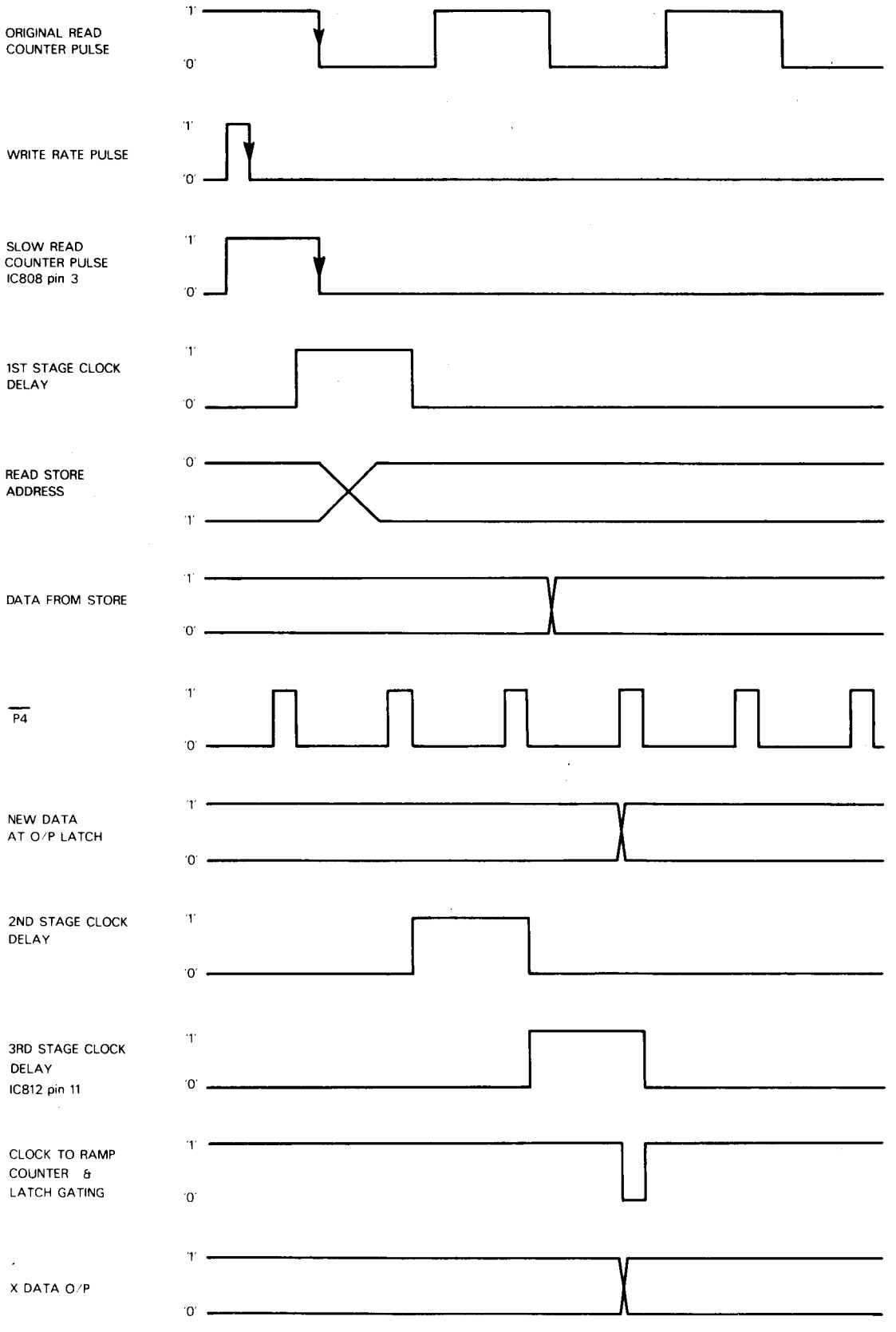


Fig. 5 Clock Delay – Timing Diagram

5.1 FITTING THE 4001 TO THE OS4000

The 4001 kit to be fitted to an OS4000 comprises:

		Part Number
1	4001 assembly	
2	Cable and plug assy 'A'	A3/36892
2	Cable and plug assy 'B'	A3/36893
4	Nut special	A4/36827
4	Pillar clamping	A4/36826
10	Washer 4–40 'Wavey'	4591
1	Cover Bottom	A2/36823
6	Screws 4–40 x ¼" Pan Head Taptite	22694

Fitting procedure

(1) Disconnect the OS4000 from the supply and stand it on the back cover.

(2) Remove both covers of the OS4000, plus 4 feet.

(3) Unplug the ribbon cables connecting SKA to SKH and SKK to SKD and plug in the four ribbon cables supplied to each of the above sockets as shown in Figs. 6 and 7b. (Long cables to sockets A and H, short to K and D.) It is possible to achieve this without removing the store and timing logic boards, but if any difficulty is encountered refer to the OS4000 handbook section 5.2.2 to remove these boards.

(4) Place the special nuts on the OS4000 frame extrusion, with the threaded hole inside as shown in Fig.7a.

(5) Place the 4001 chassis in position and insert the threaded pillars.

(6) Connect the power supplies as shown in Fig.7c. The connectors are a push fit onto the supply pins.

(7) Plug in the four ribbon cables to the sockets on the 4001, connecting

SK A to SK AA
SK D to SK DD
SK H to SK HH
SK K to SK KK

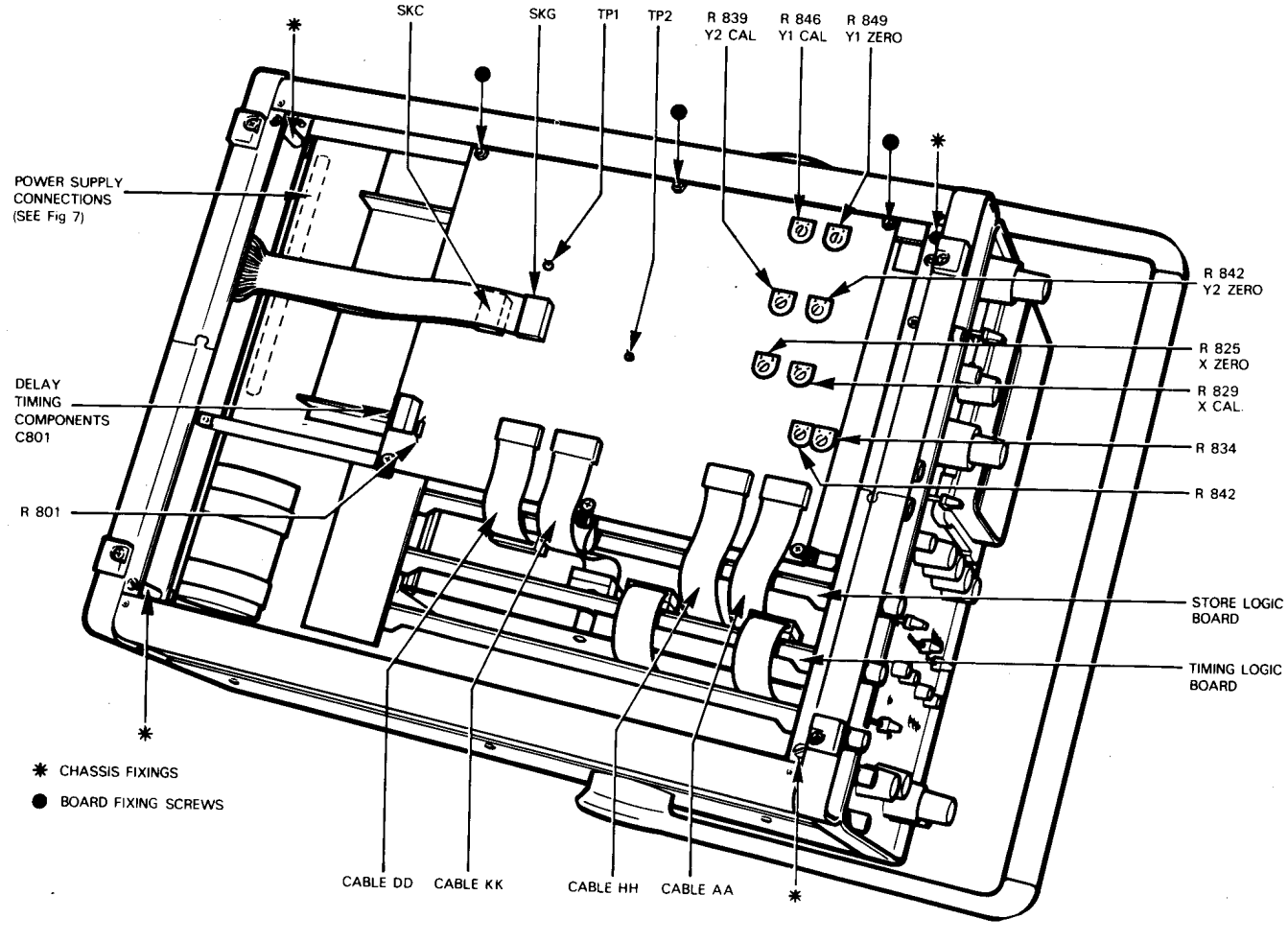


Fig. 6 Internal View of 4001

(8) The 4001 is now ready for setting up as detailed in section 5.4. It should not be necessary to make any adjustment to the OS4000.
(9) Fit the bottom cover to the 4001 with the ventilation holes at the rear. The original bottom cover of the OS4000 is not required when the 4001 is fitted.
(10) Fit 4 feet to the 4001.

5;2 ACCESS

Access to the 4001 is obtained by unscrewing the six retaining screws and removing the bottom cover. Fig.6 shows the location of the preset controls and test points.

Access to both sides of the board and to the preset controls in the OS4000 may be obtained in the following manner.

(1) Unplug PLC and PLG.
(2) Remove the three screws marked (•) in Fig.6.

The board is now free to hinge about the central bar.

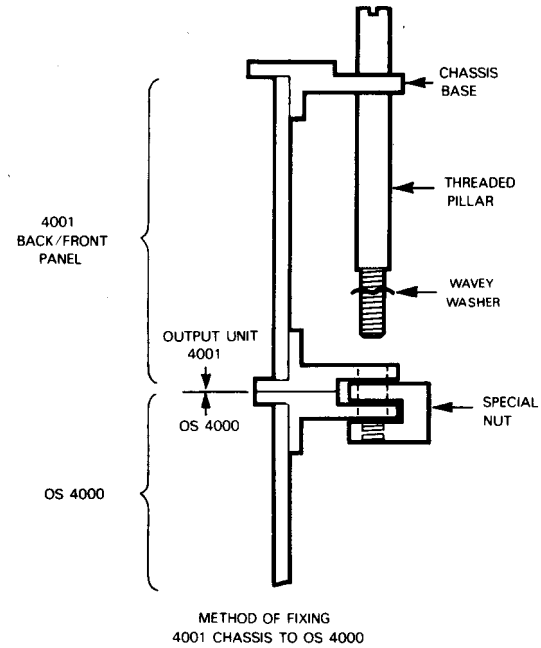
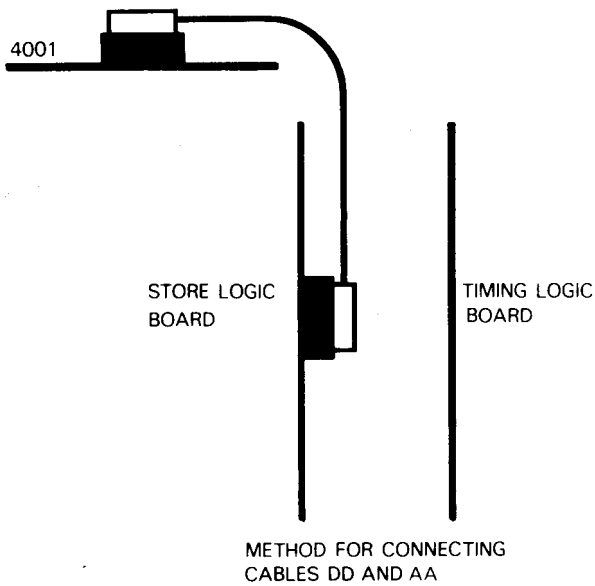
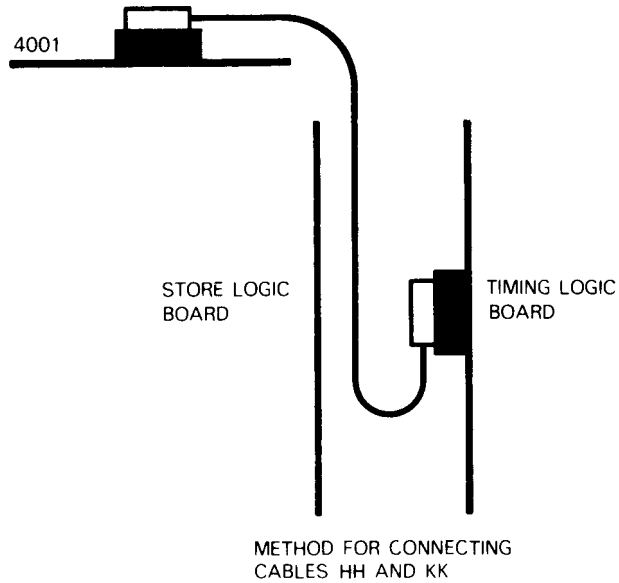


Fig. 7a

Fig. 7b





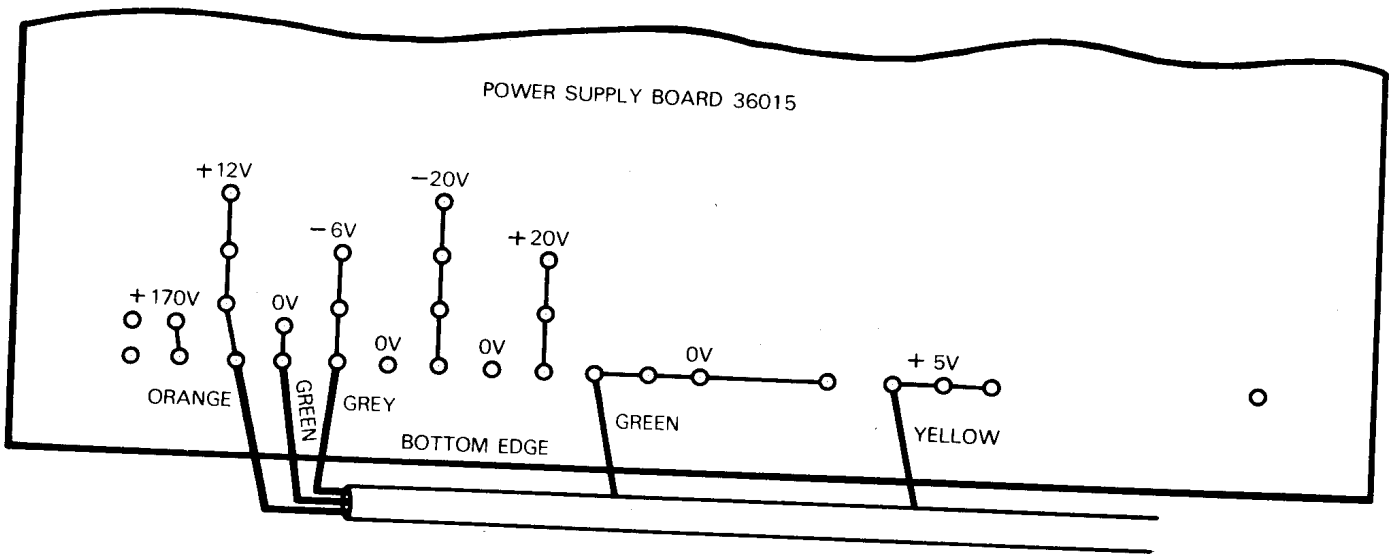


Fig. 7c

5.3 FAULT FINDING

(a) All voltage measured with respect to 0V as in Table 1

Table 1

Supply	Measured Voltage	Location
+5.V	+4.8 to +5.2V	Pin 1 with respect to Pin 2
+12V	11.5 to 12.5V	Pin 12 w.r.t. Pin 13
−6V	5.75 to 6.25V	Pin 11 w.r.t. Pin 13
6.2V ref.	5.9 to 6.5V	Wiper of R834 w.r.t. Pin 13

With the exception of the 6.2V reference, the supplies are derived from the OS4000. If any disagreement with Table 1 is encountered, disconnect the supplies at Pins 1, 2 and 11, 12 and 13 and check the incoming supplies. If the fault lies with the main frame, refer to section 5 of the OS4000 manual.

(b) **Logic Levels**

IC's with the exception of IC's 802, 809, 810, 811, 813.
Logic '1', 2 to 4.5V
Logic '0', 0.15 to 0.7V
IC's 802, 809, 810, 811, 813 have open collector outputs which require a pull-up resistor to +5V to attain the levels indicated above.

(c) **Fault Location**

The following guide assumes that there is no fault in the OS4000. This can be checked by by-passing the 4001 completely as follows:-

(a) Disconnect the four ribbon cables between the 4001 and the OS4000.
(b) Use two of these cables to connect SK A directly to SK H and SK K directly to SK D.

First check the supplies, then set the delay period to maximum.

The following chart offers guidance on fault localisation:-

(i) Digital read-out but one or more analogue outputs inoperative.	(1) +12V and −6V supplies. (2) D/A convertors. (3) Operational Amplifiers.
(ii) No read-out cycle (OS4000 display not interrupted) but the L.E.D. comes on for the delay period.	(1) Sweep reset pulse on SKDD/KK Pin 16 and IC806 Pin 11. (2) Clear inputs of IC808.
(iii) L.E.D. permanently on, no OS4000 display.	(1) $\overline{P4}$ clock pulses on SKDD/KK Pin 1. (2) Write rate pulses (related to timebase switch setting) on input Pin 3 and output Pin 4 of IC808. (3) Check clocks to ramp counter and ensure count. Read-out cannot terminate until $\overline{Q}$ of IC816 (b) clears IC806 (a).

(iv)	Both CH1 and CH2 outputs chopping between CH1 and CH2 signals at approx. 100 cycles per displayed cm.	(1) SKDD/KK Pin 3 is LO in dual trace mode.
(v)	Discontinuities in the X-ramp.	(1) Data bits missing. (2) Mis-match between IC821 current and additional currents see 5.4d.

5.4 SETTING UP PROCEDURE

(a) **Test Equipment**

1. Calibrated dual trace oscilloscope.
2. Square wave generator.

(b) **Channels 1 and 2**

Set the square-wave generator to 1kHz and the OS4000 to CH1, 0.2ms/div. X expansion X1. Adjust the generator frequency and amplitude display an 8 div peak to peak waveform with two cycles occupying 10 div. Press "Full Store Lock". Connect the 4001 CH1 output to an oscilloscope via the front panel BNC connector. Set the OS4000 timebase switch to 2ms/div. Connect TP1 or its remote on SK AC Pin 3, to logic earth to produce a continuous read-out. Adjust R846 to produce an 800mV pk-pk output. Remove the earth on TP1 and adjust R849 to produce 0V d.c. out. Connect the oscilloscope to the CH2 output and repeat adjusting R839 and R842.

(c) **X-ramp**

With the same stored display as in 5.4(b) connect an oscilloscope to the X-ramp output. Earth TP1 to produce continuous read-out. Connect the second channel of the oscilloscope to the Channel 1 output. One cycle of the stored square wave, representing 5 Div. of displayed trace, should also correspond to 500mV of X ramp. Adjust R829 to this effect.
Remove the earth on TP1 and adjust R825 to produce 0V d.c. out.

(d) **X-ramp current matching**

If any discontinuity is visible at the ¼ and/or ½ and ¾ way points of the ramp, this means that the two additional currents are no longer matched to the current from IC821.
On one channel of an oscilloscope, display the X-ramp in continuous read-out as in 5.4(c). Connect the other channel to R812.
R824 should be used to remove any step at the quarter way point (coincident with the first positive edge of D2) expanding the trace to view it if possible. Adjust R834 to remove any step at the half way point (negative edge of D2). When these two are correctly adjusted there should be no discontinuity at the three-quarter way point (coincident with the second positive edge of D2). Repeat (c) above.

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	1/2W	10%	unless otherwise stated
CF	Carbon Film	1/8W	5%	unless otherwise stated
MO	Metal Oxide	1/2W	2%	unless otherwise stated
MF	Metal Film	1/4W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potentiometer		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+ 80% - 25%	
CE(2)	Ceramic	500V	± 10%	unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		± 10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		± 10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (aluminium)		+ 50% - 10%	
T	Tantalum		+ 50% - 10%	

OUTPUT UNIT 4001

Ref	Value	Description	Tol % ±	Part No.
RESISTORS				
R81	1M	CP		A4/37898
R801	6k8	CF		21807
R802	4k7	CF		21805
R803	10k	CF		21809
R804	1M	CF		31840
R805	10k	CF		21809
R806	4k7	CF		21805
R807	4k7	CF		21805
R808	470	CF		21797
R809	4k7	CF		21805
R810				
R811	4k7	CF		21805
R812	8k2	CF		21808
R813	8k2	CF		21808
R814	10	CF		21793
R815	2k7	CF		28726
R816	3k3	CF		21803
R817	10	CF		21793
R818	3k3	CF		21803
R819	10	CF		21793
R820	3k3	CF		21803
R821	10	CF		21793
R822	180	CF		21795
R823	3k	MO		26727
R824	220	PCP		35881
R825	220	PCP		35881
R826	4k7	CF		21805
R827	1k1	MO		28791
R828	120	CF		28718
R829	100	PCP		36958
R830	100	CF		21794
R831	2k7	CF		28726
R832	100	CF		21794
R833	1k5	MO		26733
R834	100	PCP		36958
R835	680	CF		28723
R836	560	CF		21798
R837	560	CF		21798
R838	100	CF		21794
R839	1k	CP		35880
R840	3k3	CF		21803
R841	6k8	CF		21807
R842	2k2	PCP		36868
R843	560	CF		21798
R844	560	CF		21798
R845	100	CF		21794
R846	1k	PCP		35880
R847	3k3	CF		21803
R848	6k8	CF		21807
R849	2k2	PCP		36868
R850				
R851				
R852	4k7	CF		21805
R853	180	CF		21795
R854	3k3	MO		26726

Ref	Value	Description	Tol % ±	Part No.
CAPACITORS				
C81	.1μF	CE(2)	25V	36709
C82	.1μF	CE(2)	25V	36709
C83	.1μF	CE(2)	25V	36709
C801	1.5μF	PE	63V	31365
C802	.68μF	E	63V	32162
C803	10nF	CE(2)	250V	22395
C804	2n2F	CE(2)	500V	22389
C805	10nF	CE(2)	250V	22395
C806	10nF	CE(2)	250V	22395
C807	1nF	CE(2)	500V	22387
C808	10nF	CE(2)	250V	22395
C809	10nF	CE(2)	250V	22395
C810	33μF	E	16V	32173
C811	10nF	CE(2)	250V	22395
C812	33μF	E	16V	32173
C813	10nF	CE(2)	250V	22395
C814	10nF	CE(2)	250V	22395
C815	10nF	CE(2)	250V	22395
C816	10nF	CE(2)	250V	22395
C817	10nF	CE(2)	250V	22395
C818	10nF	CE(2)	250V	22395
C819	10nF	CE(2)	250V	22395
C820	100nF	CE(2)		36709
C821	100nF	CE(2)		36709
C822	100nF	CE(2)		36709

INTEGRATED CIRCUITS		
IC801	555V	36813
IC802	74LS05	36879
IC803	74LS10	36867
IC804	74LS04	36731
IC805	74LS00	36730
IC806	74LS74	36732
IC807	74LS00	36730
IC808	74S157	36735
IC809	74LS05	36879
IC810	74LS05	36879
IC811	74LS05	36879
IC812	74LS95	36734
IC813	74LS05	36879
IC814	74LS175	36728
IC815	74LS175	36728
IC816	74LS76	36733
IC817	74LS161	36727
IC818	74LS175	36728
IC819	74LS175	36728
IC820	74LS161	36727
IC821	1408-8	35683
IC822	1408-8	35683
IC823	1408-8	35683
IC824	741	36736
IC825	741	36736
IC826	741	36736
IC827	78L06	36959

OUTPUT UNIT 4001 (Contd.)

Ref	Value	Description	Tol % ±	Part No.
TRANSISTORS				
TR801		BC182B		33205
TR802		2N2369		23307
TR803		2N2369		23307
DIODES				
D81		L.E.D. TIL209A		35202
D801		IN4148		23802
D802		IN4148		23802
D803				
D804		IN4148		23802
D805		IN4148		23802
D806		IN4148		23802
D807		IN4148		23802
D808		IN4148		23802

Ref	Value	Description	Tol % ±	Part No.
MISCELLANEOUS				
S81				A4/35341
RL801		REED RELAY		26755
SKAC		Amphenol 57–40360		27513
SKAD				26587
SKAE				26587
SKAF				26587
SKAG				36946
SKAH				36946

Guarantee and Service Facilities

Section 7

This instrument is guaranteed for a period of two years from its delivery to the purchaser, covering faulty workmanship and replacement of defective parts other than cathode ray tubes and batteries (where fitted). Cathode ray tubes are subject to the manufacturers guarantee. This assumes fair wear and tear and usage in the specified environment and does not cover routine recalibrations and mechanical adjustments.

We maintain comprehensive after sales facilities and the instrument should be returned to our factory for servicing if this is necessary. The type and serial number of the instrument should always be quoted, together with full details of any fault and service required.

Equipment returned for servicing must be adequately packed, preferably in the box in which the instrument was supplied and shipped with transportation charges prepaid. We accept no responsibility for instruments arriving damaged. Should the cause of failure during the guarantee period be due to misuse or abuse of the instrument, or if the guarantee has expired the repair will be put in hand without delay and charged unless other instructions are received.

Our Sales, Service and Engineering Departments are ready to assist you at all times.

The Service Department can provide maintenance and repair information by telephone or letter, if required.

Note: Please check fuses before returning instruments for service.

Service Dept.,
Roebuck Road,
Hainault,
Essex,
IG6 3UE

Tel: 01-500 1000
Telex: 263785
Telegrams: Attenuate Ilford