Errata

Title & Document Type: **1980A Oscilloscope Measurement System Operating and Service Manual**

Manual Part Number: **01980-90907**

Revision Date: **February 1982**

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Agilent Technologies

OPERATING AND SERVICE MANUAL

MODEL 1980A
OSCILLOSCOPE MEASUREMENT SYSTEM

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **2205A.**

For additional important information about serial numbers see INSTRUMENTS COVERED BY MANUAL in SECTION I.

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Manual Part No. 01980-90907
Microfiche Part No. 01980-90807
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PRINTED: FEBRUARY 1982

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

The cathode-ray tube (CRT) in the instrument and any replacement CRT purchased from HP are also warranted against electrical failure for a period of one year from the date of shipment from Colorado Springs. BROKEN TUBES AND TUBES WITH PHOSPHOR OR MESH BURNS, HOWEVER, ARE NOT INCLUDED UNDER THIS WARRANTY.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

S C W & A 9/78 (CRT)

X-RAY RADIATION NOTICE

ACHTUNG

Model 1980A/B

WARNING

Während des Betriebs erzeugt dieses Gerät Röntgenstrahlung. Das Gerät ist so abgeschirmt, daß die Dosisleistung weniger als 36 pA/kg (0,5 mR/h) in 5cm Abstand von der Oberfläche der Katodenstrahlröhre beträgt. Somit sind die Sicherheitsbestimmungen verschiedener Länder, u.A. der deutschen Röntgenverordnung eingehalten.

Die Stärke der Röntgenstrahlung hängt im Wesentlichen von der Bauart der Katodenstrahlröhre ab, sowie von den Spannungen, welche an dieser anliegen. Um einen sicheren Betrieb zu gewährleisten, dürfen die Einstellungen der Niederspannungs- und des Hochspannungsnetzteils nur nach der Anleitung in Kapitel V des Handbuches vorgenommen werden.

Die Katodenstrahlröhre darf nur durch die gleiche Type ersetzt werden. (Siehe Kapitel VI für HP — Ersatzteile).

Das Gerät ist in Deutschland zugelassen unter

der Nummer: BW/71/80/Rö

When operating, this instrument emits x-rays; however, it is well shielded and meets safety and health requirements of various countries, such as the X-ray Radiation Act of Germany.

Radiation emitted by this instrument is less than 0.5 mR/hr at a distance of five (5) centimeters from the surface of the cathode-ray tube. The x-ray radiation primarily depends on the characteristics of the cathode-ray tube and its associated low-voltage and high-voltage circuitry. To ensure safe operation of the instrument, adjust both the low-voltage and high-voltage power supplies as outlined in Section V of this manual (if applicable).

Replace the cathode-ray tube with an identical CRT only. Refer to Section VI for proper HP part number.

Number of German License: BW/71/80/Rö

LITHIUM BATTERY SAFETY INFORMATION

To prevent explosion or exposure to hazardous materials, the Lithium battery contained in this instrument must be handled in the following manner:

Do not crush, puncture, or mutilate battery.
Do not incinerate battery.
Do not short battery terminals.

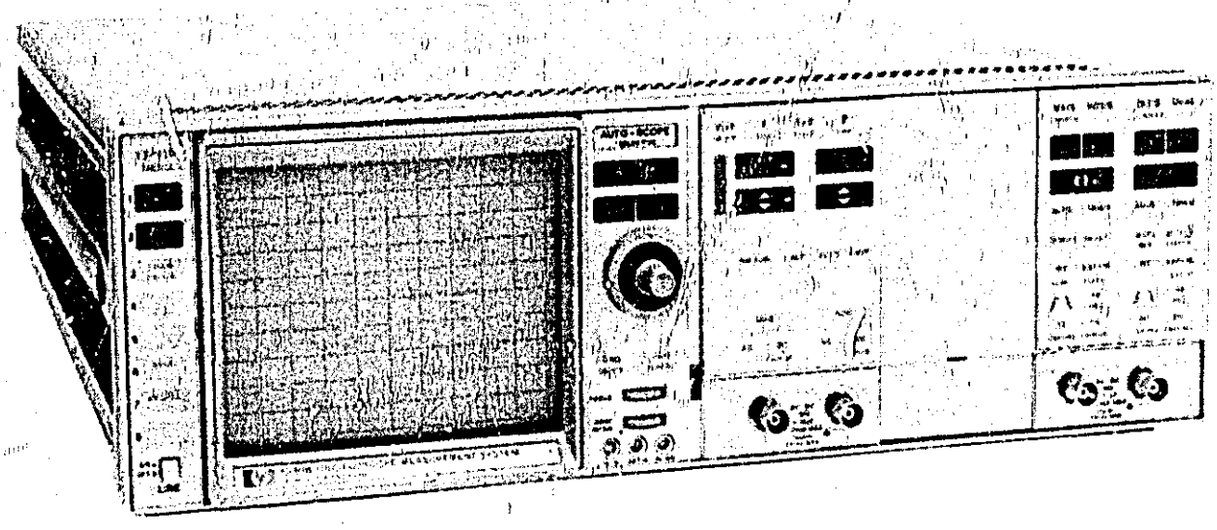
Dispose of battery in a controlled, hazardous waste land fill as designated by your state.

If proper disposal methods are not available or unknown, place insulating, electrical tape over terminals and return to your nearest HP Sales and Service office.

SS-3-9/80

OPERATING AND PROGRAMMING MANUAL

1980A/B OSCILLOSCOPE MEASUREMENT SYSTEM



HEWLETT PACKARD

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

The cathode-ray tube (CRT) in the instrument and any replacement CRT purchased from HP are also warranted against electrical failure for a period of one year from the date of shipment from Colorado Springs. BROKEN TUBES AND TUBES WITH PHOSPHOR OR MESH BURNS, HOWEVER, ARE NOT INCLUDED UNDER THIS WARRANTY.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement, and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

S C W & A 9/78 (CRT)

OPERATING AND PROGRAMMING MANUAL

1980 A/B
OSCILLOSCOPE MEASUREMENT SYSTEM

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed as noted on the title page of the 1980A or 1980B (as applicable) Operating and Service Manual. For a brief history of operational changes, refer to Appendix 1 at the end of Section III. For additional information about serial numbers, refer to INSTRUMENTS COVERED BY MANUAL in Section I.

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OPERATING AND PROGRAMMING MANUAL PART NO. 01980-90905
Operating and Programming Microfiche Part No. 01980-90805

PRINTED NOVEMBER 1981

SAFETY CONSIDERATIONS

GENERAL — This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION — BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNINGS

Servicing instructions are for use by service-trained personnel only. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.

BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two conductor outlet is not sufficient protection.

If this instrument is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Do not install substitute parts or perform any unauthorized modification to the instrument.

Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.



Indicates hazardous voltages.



Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

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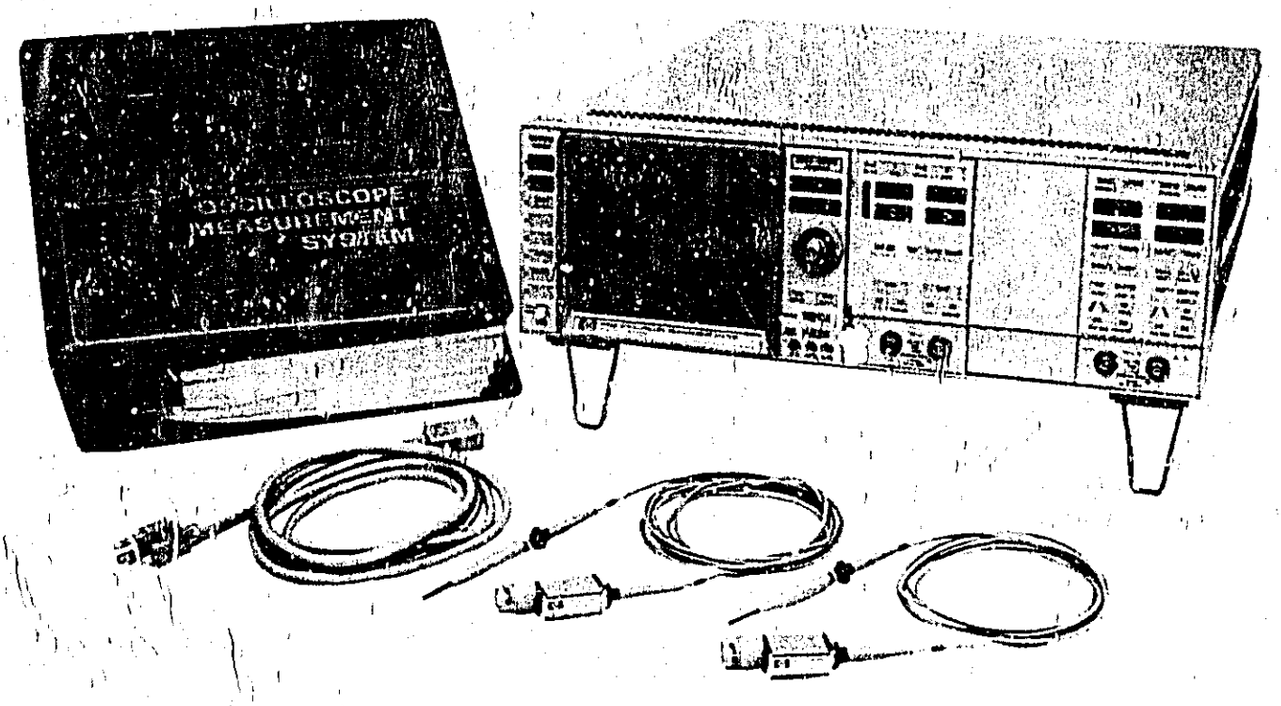


Figure 1-1. HP Model 1980B Oscilloscope Measurement System and Supplied Accessories

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

From the standpoint of operation, the Model 1980A and Model 1980B Oscilloscope Measurement Systems are virtually identical; the major difference is in physical configuration. The 1980A is a cabinet model for bench operation. The 1980B is configured for either rack mounted or bench operation. In this manual, the two models are referred to collectively as the 1980A/B. Where distinction is necessary, the two models are referred to separately.

The 1980A/B Operating and Service Manual has eight major sections. The manual contains the following information:

Section I, General Information: describes the instruments documented by this manual. It also provides a basic description of the Measurement System which includes options, accessories, and specifications.

Section II, Installation: provides information about initial inspection, preparation for use (including HP-IB address selection for remote operation), and storage and shipment.

Section III, Operation: provides detailed operating information for the instrument, including remote (HP-IB) operation and operator's checks and maintenance. Also included is a front-panel description and a "getting acquainted" exercise to familiarize the first time user with the basic Measurement System operating procedures.

Section IV, Performance Tests: presents the procedures required to check the performance of the instrument against the critical specifications in table 1-1.

Section V, Adjustments: provides instructions for properly adjusting the instrument.

Section VI, Replaceable Parts: provides ordering information for all replaceable parts and assemblies.

Section VII, Manual Changes: contains manual change information necessary to document all serial prefixes listed on the title page of this manual. In addition, this section also contains recommended modifications for earlier instrument configurations.

Section VIII, Service: provides the information required to repair the instrument.

This Operating and Programming Manual contains Sections I, II, and III only. The Service Manual contains the remaining sections. A second copy of the Operating and Programming Manual is included in the manual set; it should be kept with the instrument for operator reference. Additional copies may be ordered separately through your nearest Hewlett-Packard Sales and Service office. The part numbers for the complete Operating and Service Manual and for the Operating and Programming Manual alone are listed on the title page of this manual.

Also listed on the title page is the part number for a microfiche version of the complete Operating and Service Manual. The microfiche are 100 × 150 mm (4 × 6 inch) microfilm transparencies of the manuals. Each microfiche contains up to 96 photo duplicates of manual pages. The microfiche package also includes the latest Manual Changes supplement.

1-2. SPECIFICATIONS.

Specifications and supplemental characteristics of the 1980A/B Oscilloscope Measurement System are listed in table 1-1. This instrument will meet the electrical characteristics listed following complete calibration as given in the Adjustments section of the manual. These electrical characteristics apply over the ambient temperature range of 0 to 55°C except as otherwise noted. Warm-up time for given accuracy is 30 minutes.

1-3. SAFETY CONSIDERATIONS.

WARNING

To prevent ...urs... injury, observe all safety precautions and warnings stated on the instrument and in the manual.

This product is a Safety Class I instrument (provided with a protective earth terminal). The 1980A/B and all related documentation must be reviewed for familiarization with safety markings and instructions before operation. Refer to the Safety Considerations page found at the beginning of this manual for a summary of general safety information. Safety precautions for installation, operation, and servicing are found in appropriate locations throughout the Operating and Service Manual. These precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in the manual violates safety standards of design, manufacture, and intended use of this instrument. Hewlett-Packard assumes no liability for failure to comply with these requirements.

1-4. INSTRUMENTS COVERED BY MANUAL.

Attached to the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is in two parts: the first four digits and the letter are the serial number prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The letter in the prefix designates the country in which the instrument was manufactured. (A=USA; G=West Germany; J=Japan; S=Singapore.) The suffix, however, is assigned sequentially and is unique to each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. Manuals accompanying these newer instruments include a Manual Changes supplement. The supplement contains change instructions for the entire Operating and Service Manual.

In addition to change information, the supplements may contain information for correcting errors in the manuals. To keep your manuals as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. These supplements are identified with the print date and part number that appears on the title page of this manual. Complimentary copies of these supplements are available from Hewlett-Packard.

For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales and Service office.

1-5. DESCRIPTION.

The 1980A/B Oscilloscope Measurement System is a complete two channel 100 MHz oscilloscope. It features 2 mV/div deflection factor, two independent 5 nsec/div sweeps, main and delayed trigger view, and both delta time and delta voltage functions. Measurement capabilities can be extended by adding internal options and plug-in Expansion Modules.

In addition, the 1980A/B has these special features:

- All functions are programmable via HP-IB (HP's implementation of IEEE Std 488) for automatic or semi-automatic measurement applications.
- Autoscope function presets the 1980A/B, then autoranges trigger level, deflection factor, and sweep speed. It provides a one keystroke setup for most input signals.
- Save/Recall registers can be used to save as many as eight complete instrument states for recall in repetitive measurement procedures.
- Calibration can be performed on-site, without removing covers and requires little or no test equipment. Internal reference signals are provided and complete, step by step instructions are displayed on the CRT.

1-6. OPTIONS.

1-7. Electrical Options.

Option 080: Supplies two, 10080A 10:1, 1 M (3.3 ft) probes instead of two 10081A probes.

Option 082: Supplies two, 10082A 10:1, 3 M (10 ft) probes instead of two 10081A probes.

Option 083: Supplies two, 10083A 1:1, 1 M (3.3 ft) probes instead of two 10081A probes.

Option 084: Supplies two, 10084A 1:1, 2 M (6.5 ft) probes instead of two 10081A probes.

Option 090: Deletes probes.

Option 150: Supplies HP Model 1950A Two Channel Vertical Plug-in installed.

Option 810: Supplies HP Model 19810A Key Sequence ROM installed.

Option 811: Supplies HP Model 19811A Plot/Sequence ROM installed.

Option 860: Supplies HP Model 19860A Digital Waveform Storage installed.

1-8. Mechanical Options.

The following options are available for rack mounting the 1980B. The rack mounting kits can be ordered separately from the nearest Hewlett-Packard Sales office using the part numbers given in the descriptions.

Front Handle Kit (Option 907). This kit contains front handles and mounting hardware. Order HP part number 5061-0089.

Rack Flange Kit (Option 908). This kit contains flanges and hardware for mounting the Measurement System in a standard rack of 482.5 mm (19 inches). Order HP part number 5061-0077.

Rack Flange and Front Handle Combination Kit (Option 909). This kit contains flanges, handles and mounting hardware (the flanges are different than the Option 908 flanges). Order HP part number 5061-0083.

Standard Slide Kit (Option 009). This kit contains rack mounting slides and hardware for mounting the Measurement System into HP rack enclosures. Order HP part number 1494-0017.

1-9. HEWLETT-PACKARD INTERFACE BUS (HP-IB). HP-IB

1-10. Compatibility.

The standard 1980A/B Oscilloscope Measurement System has an HP-IB interface and can be used in automatic system applications driven by an HP-IB equipped controller or computer. The instrument is fully programmable via the HP Interface

Bus. The instrument's compatibility with HP-IB is defined by the following list of interface functions: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP0, DC0, DT1, C0, E2. For an explanation of the compatibility codes, refer to IEEE Std 488 "IEEE Standard and Digital Interface for Programmable Instrumentation" or the identical ANSI Standard MC1.1.

For more detailed information relating to remote operation of the Measurement System, refer to Remote Operation, Hewlett-Packard Interface Bus in Section III of this manual.

1-11. HP-IB Address.

The HP-IB address "7" is preset at the factory before the instrument is shipped. This address may be displayed or changed from the front-panel when the HP-IB ADDRESS MODE menu is selected. This procedure is described in Section II. The "HP-IB Address" Detailed Operating Instruction (Section III) provides a more complete description of addressing considerations.

1-12. ACCESSORIES SUPPLIED.

Accessories supplied with the Measurement System are in figure 1-1. Included with the instrument are: One blue light filter, one 2.3 M (7.5 ft) power cordset, one Expansion Module Panel Cover, and one complete Operating and Service Manual. A second copy of the Operating and Programming Manual (sections I-III) is also included.

The power cable and line fuse are selected at the factory according to the voltage available in the country of destination. For the part numbers of the available power cables, refer to paragraph 2-6, AC Power Cable, in Section II.

1-13. EQUIPMENT AVAILABLE.

The following accessories are available for servicing the Measurement System:

64 Pin Hybrid Extender. Aids troubleshooting circuits containing 64 pin hybrids. Order HP part number 5081-7663.

Plug-in Extender. Required to service plug-in Expansion Modules. Order HP part number 01980-63901.

1-14. RECOMMENDED TEST EQUIPMENT.

Table 1-2 lists equipment required for maintaining the 1980A/B. The Critical Specifications column describes the essential requirements for each piece of test equipment. Other equipment can be substituted if it meets or exceeds these critical specifications.

The Suggested Model column may suggest more than one model. The first model shown is usually the least expensive, single purpose model. Alternate models are suggested for additional features that would make them a better choice in some applications. For example, reasons for recommending an alternative model might be:

- HP-IB programmability

  -- or --

- Multi-function capability (that is, one model can replace two or more single purpose models)

Table 1-4 presents the advantages of the alternate suggestions.

Table 1-1. Specifications (Page 1 of 4)

OPERATING MODES

Voltage vs time (V vs T); channel 1 vs 2 (1 vs 2); monitor mode for logic state display with HP Model 1607A (X-Y-Z).

VERTICAL DISPLAY MODES (V vs T)

Channel 1; channel 2; channels 1 and 2 displayed on alternate sweeps (ALT); channels 1 and 2 displayed by switching between channels at approx 400 kHz rate with blanking during switching (CHOP); automatic selection of alternate for sweep speeds >1 ms/div and chop for sweep speeds ≤1 ms/div (AUTO-CHOP/ALT); channel 1 plus 2 algebraic addition (1+2), channel 1 and/or 2 may be inverted; and either main or delayed trigger signal.

VERTICAL AMPLIFIERS (2)

BANDWIDTH: 3 dB down from a 5 div reference signal (0 to +40° C).

DC-Coupled: dc to 100 MHz in 50Ω and 1 MΩ input modes.

AC-Coupled: <10 Hz to ≥100 MHz.

BANDWIDTH LIMIT: limits upper bandwidth to approx 20 MHz.

INPUT COUPLING: AC, DC, 50Ω (DC), Ground. Ground position disconnects input connector and grounds amplifier input.

INPUT RC

AC or DC: 1 MΩ ±2% shunted by approx 16 pF.

50 Ohm (DC): 50Ω ±3%.

MAXIMUM INPUT VOLTAGE

50 Ohm: 5V rms.

1 Megohm: ac or dc coupled, 250V (dc + peak ac) at ≤1 kHz.

DEFLECTION FACTOR

Range: 2 mV/div to 10 V/div.

Resolution: 3 digits.

Adjustment: coarse stepping is in a 100, 150, 200, 300 . . . 900 sequence; fine stepping is a change of 1 in the least significant digit.

Accuracy: ±3%.

VERTICAL POSITION

Range: baseline can be adjusted ±15 major div from center graticule line (possible 10 div off screen).

Resolution: 0.02 major division.

Adjustment: coarse or fine slew rates.

Accuracy: ±(2% of reading +0.3 major div).

ΔV (CHANNEL 1 OR 2)

Range: ±15 times the deflection factor selected for that channel.

Resolution: 0.02 times the deflection factor for that channel.

Adjustment: coarse or fine slew rates.

Accuracy: ±4% (for a Δ ≤ 10 major divisions).

CHANNEL 1 + 2

Amplifier: bandwidth and deflection factors are unchanged.

Differential (Channel 1-2 or Channel 2-1): CMR is at least 20 dB from dc to 20 MHz with common mode signal amplitude equivalent to 10 div and one channel adjusted for optimum rejection.

TRIGGER VIEW

Display: Internal or external trigger signal for either main or delayed sweep.

Deflection Factor: internal, approx deflection for selected channel; ext ÷ 10, 600 mV/div ±20%; ext ÷ 1, 60 mV/div ±20%.

External Trigger Signal Delay: ≤4 ns with identically timed signals to a vertical channel and either main or delayed trigger inputs.

Trigger Point: approx center horizontal graticule line.

Momentary: trigger signal is displayed while main or delayed trigger level is adjusted.

HORIZONTAL DISPLAY MODES (V vs T)

Main, Main Intensified, Delayed, and Dual. Dual simultaneously displays main intensified and delayed sweep for all displayed channels.

MAIN AND DELAYED TIME BASES

RANGE: 5 ns/div to 1 s/div.

RESOLUTION: 3 digits.

ADJUSTMENT: coarse stepping is in a 100, 150, 200, 300, . . . 900 sequence; fine stepping is a change of 1 in the least significant digit.

ACCURACY:

Speed	Accuracy*
5 ns/div to 9.99 ns/div (center 8 div)	±3%
10 ns/div to 9.99 ms/div (first 10 div)	±3%
10 ms/div to 1 s/div (first 10 div)	±4%

*Within ±10° C of the temperature at which the instrument was calibrated. For temperatures beyond the ±10° C range and within 0 to +55° C, add 1%, from 0.5 s/div to 1 s/div add 2%.

SWEEP DELAY

Delay can be measured by either time or a number of events.

TIME DELAY

RANGE: 0 to 9.9999 s.

Resolution: displayed, 5 digits; HP-IB, 100 ps at any delay, possible 11 digits.

Table 1-1. Specifications (Page 2 of 4)

Accuracy:*

Delay or Time Interval

Sweep Speed	<200 μs	≥200 μs
5 ns/div to 9.99 ns/div	±(2 ns + 0.1% of reading)	±(0.05% of reading)
≥10 ns/div	±(2 ns + 0.1% of reading + 1% of dly'd s/div × 10 div)	±(0.05% of reading + 1% of dly'd s/div × 10 div)

*Within one hour of a Delay Self Calibration and in constant ambient temperature.

Delay Jitter: 0.002% of delay time; at 10 MHz ± 10 kHz, 0.01% of delay time.

Adjustment: Numerical, step size is related to current delay value; Normal, step size is related to sweep speed.

TIME INTERVAL (ΔT)

In Intensified, Dual, or Delayed Horizontal Display Modes a zero time reference can be set anywhere in the delay range and a time interval measurement can be made from that point.

Resolution, Adjustment, Accuracy: same as Time Delay.

FREQUENCY (1/ΔT)

Calculates and displays reciprocal of time interval measurement.

Resolution: same as ΔT. As frequency increases insignificant digits are truncated.

Adjustment, Accuracy: same as Time Delay.

DIGITAL DELAY

Range: 0 to $10^8 - 1$ events.

Resolution: 1 event.

Adjustment: coarse stepping is in a 1, 2, 3, . . . 9, 10, 20, 30, . . . 90, etc. sequence; fine stepping is a change of 1 in least significant digit.

Maximum Rep Rate: 15 MHz with a 50% duty cycle.

TRIGGERING (Main and Delayed Time Bases)

MAIN SWEEP

Triggered: specified level and slope is required to generate a sweep.

Auto-Triggered: baseline displayed in absence of a trigger signal; triggering is same as triggered above approx 10 Hz.

Single: sweep occurs once with same triggering as Triggered mode; reset key rearms sweep.

DELAYED SWEEP

Auto Sweep After Delay: delayed sweep starts at end of delay time.

Triggered Sweep After Delay: delayed sweep can be triggered after delay time.

Digital Delay: delayed sweep starts a specified number of events after start of main sweep.

SOURCES

Selectable from Channel 1, Channel 2, Enhancement Module, or External. Line frequency triggering is also available for main sweep only. Main and delayed trigger sources are independently selectable.

INTERNAL TRIGGER LEVEL

Range: ±20 major divisions from center horizontal graticule line.

Resolution: 0.02 major divisions; coarse or fine slew rates.

Accuracy: ±(3% of reading + 0.4 major div).

EXTERNAL TRIGGER LEVEL

Range: ÷1, ± 1.2 V from ground reference; in ÷10, ± 12 V from ground reference.

Resolution: ÷1, 2 mV; in ÷10, 20 mV; coarse or fine slew rates.

Accuracy: ±(3% of reading + 40 mV); in ÷10 mode, ±(3% of reading +400 mV).

LINE TRIGGER LEVEL

Range: ±20 relative units.

Resolution: steps of 0.02; fine or coarse slew rates.

SLOPE: triggers on positive or negative slope within specified trigger signal range.

SENSITIVITY

Internal: for deflection factors <10 mV/div, at least 1.4 div of vertical deflection from dc to 25 MHz increasing to 3 div at 100 MHz; for deflection factors ≥10 mV/div at least 0.7 div of vertical deflection from dc to 25 MHz increasing to 1.5 div at 100 MHz.

External: in external ÷10, at least 500 mV p-p from dc to 25 MHz increasing to 1.2 V p-p at 100 MHz; in external ÷1, at least 50 mV p-p from dc to 25 MHz increasing to 120 mV p-p at 100 MHz.

COUPLING (Internal and External)

AC: attenuates signals <10 Hz.

DC: direct coupled.

HF Rej: attenuates signals above approx 35 kHz.

LF Rej: attenuates signals below approx 35 kHz.

EXTERNAL TRIGGER INPUTS (Main and Delayed)

Input RC: AC or DC, 1 MΩ ±2% shunted by approx 15 pF; 50Ω (DC), 50Ω ±3%

Maximum Input Voltage: 50Ω (DC), 5 V rms; 1 MΩ, ac or dc coupled, 250 V (dc + peak ac) at ≤1 kHz.

1 vs 2 OPERATION

BANDWIDTH

Y-Axis (Channel 1): same as channel 1 in V vs T.

X-Axis (Channel 2): dc to 4 MHz.

Phase Difference Between Channels: ≤3° dc to 100 kHz.

Deflection Factors: same as Vertical Amplifiers.

X·Y·Z OPERATION

Inputs are compatible with HP Model 1607A Logic State Analyzer or equivalent.

X AND Y INPUTS

Deflection Factors: 0.5 V/div ±20% for X; 0.4 V/div ±20% for Y.

Table 1-1. Specifications (Page 3 of 4)

Input Impedance approx 5 kΩ.
Maximum Input Voltage: ±10 V.

Z-INPUT
Sensitivity: pulse ≥50 ns wide and 4 V amplitude blanks any intensity display.
Input Impedance: low power Schottky TTL gate.
Bandwidth: approx 10 MHz.
Maximum Input Voltage: TTL level, 5 V.

CATHODE-RAY TUBE AND CONTROLS

TYPE: post accelerator, approx 22 kV accelerating potential, aluminized P31 phosphor.
GRATICULE: 10 × 10 div internal graticule; 0.2 subdivision markings on major horizontal and vertical axes; 10 × 12 cm display area.
TRACE INTENSITY: adjustable in relative steps of 1 from 0 to 99.
CHARACTER INTENSITY: adjustable in relative steps of 1 from 0 to 99.
FIND BEAM: returns trace to CRT screen regardless of setting of vertical, horizontal, or intensity controls.
GRATICULE ILLUMINATION: internal flood gun.
ALIGN: aligns baseline with horizontal graticule line.
ASTIG: controls roundness of beam.

OPERATING CHARACTERISTICS

AUTOSCOPE: seeks, scales, and displays input signals >20 mV and >50 Hz. Autoscope preselects V vs T operating mode, main sweep, assigns Control Knob to main sec/div, ac input coupling, character generator on, internal trigger source, positive slope, and trigger level to 0.5 div.
SELECTIVE AUTOSCOPE: seeks, scales, and displays selected channels in the same manner as autoscope except all setup functions below the variable function keys on the "VOLTAGE" and "TIME" panels are preserved.
PROBE RECOGNITION: deflection factor, ΔV, or external trigger level readout is automatically adjusted for division ratio of recommended 1:1 or 10:1 probes.
SAVE/RECALL REGISTERS: saves up to eight complete front panel setups in nonvolatile memory.
PRESET: sets front panel to V vs T, intensified sweep mode, 100 μs/div main sweep, 10 μs/div delayed sweep, channel 1 main trigger, channel 1 delayed trigger, 2 V/div on channels 1 and 2, and ac input coupling.
CRT DISPLAY READOUTS: displays selected trigger source and selected variable functions.
Trigger Source: time base, main or delayed for channels 1 and 2, external, and line.
Variable Functions: channels 1 and 2 volts/div and ΔV; main and delayed sweep speeds, time delay, normal, numerical, and digital; normal and numerical ΔT; and calculated frequency (reciprocal of ΔT) 1/ΔT.
LED DISPLAY READOUTS: all functions related to the Control Knob are displayed.

HORIZONTAL POSITION
Range: ±6 major div from center vertical graticule line.
Resolution: 0.02 major divisions.
Adjustment: coarse or fine slew rates.

DUAL SEPARATION
Range: delayed sweep waveform can be adjusted ±5 major vertical div from main sweep waveform.
Resolution: 0.02 major divisions.
Adjustment: coarse or fine slew rates.
PANEL INTENSITY: adjustable in relative steps of 1 from 0 to 99.

GENERAL

BUS COMPATIBILITY: as defined in IEEE Std 488-1978 is: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP0, DC0, DT1, C0, and E2.
SELF CALIBRATION ROUTINES: two self calibration routines can be performed at any time without altering front panel setup.
Balance Self Cal: DC balances vertical pre-amplifier inputs to minimize trace shift during deflection factor range changes.
Delay Self Cal: calibrates delay time oscillator to within 0.005% of the internal crystal reference accuracy.
FRONT PANEL CAL 1980A/B: Channel 1 and 2 position, dual separation, main and delayed trigger level, and delay time are calibrated to specified accuracy using internally generated calibration signals. Channel 1 and 2 deflection factors, and main and delayed sweep speeds are calibrated to specified accuracies with externally supplied calibration signals. Deflection factors and sweep speeds are also supplied with internal calibration signals as a performance verification with approx ±6% accuracy.

SIGNAL OUTPUTS
Calibrator Outputs: rear panel BNC and front panel post: source impedance, approx 150Ω; probe calibration, 1 V p-p ±1%, approx 1.86 kHz square wave, rise time ≤5 μs; programmable cal signals, 20 mV p-p ±2%, 100 mV p-p ±1%, 200 mV p-p ±1%, 1 V p-p ±1%, and 10 V p-p ±1%.
15 Volt Reference: source impedance, approx 1 kΩ; level, 15 V ±30 mV.
Main Gate: source impedance, ECL gate output; signal, high ECL logic level following main gate.
Delayed Gate: source impedance, ECL gate output; signal, high ECL logic level following delayed gate.
POWER: 100, 120, 220, 240 Vac, +5 to −10%, 48 to 440 Hz, 300 VA max with expansion module and plug-in ROMs, standard, 200 VA max.

OPERATING ENVIRONMENT
Temperature: 0 to +55° C.
Humidity: to 95% relative at +40° C.
Altitude: to 4600 m (15 000 ft).
Vibration: vibrated in three planes for 15 min. each with 0.38 mm (0.015 in.) excursion, 10 to 55 Hz.

Table 1-1. Specifications (Page 4 of 4)

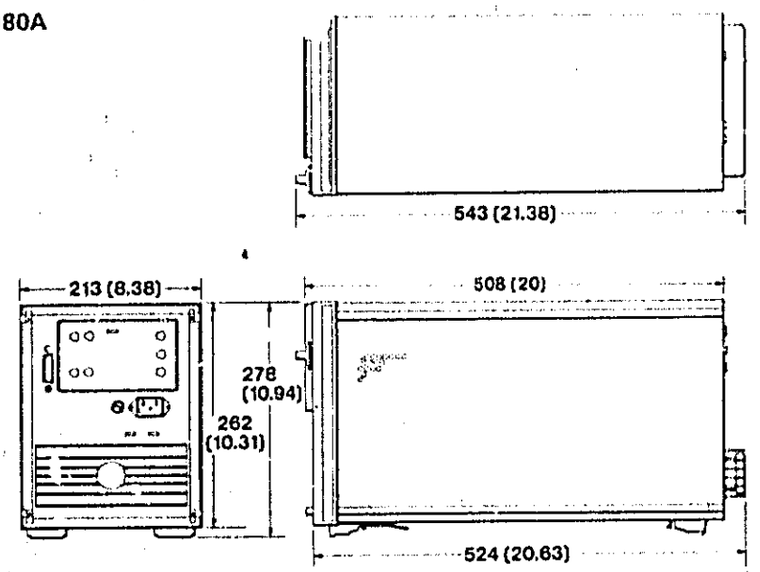
ACCESSORIES FURNISHED: one blue light filter HP P/N 01980-02701, one 2.3 m (7.5 ft) power cord, one Expansion Module Panel Cover HP P/N 01980-24106, two Operating/Programming Manuals, one Service Manual, one Binder with Divider tabs, two 10081A, 10:1, divider probes approx 2 m (6 ft) long.

WEIGHT: net, approx 18.2 kg (40 lb); shipping, approx 24.1 kg (53 lb).

DIMENSIONS:

in mm (in.)

1980A



1980B

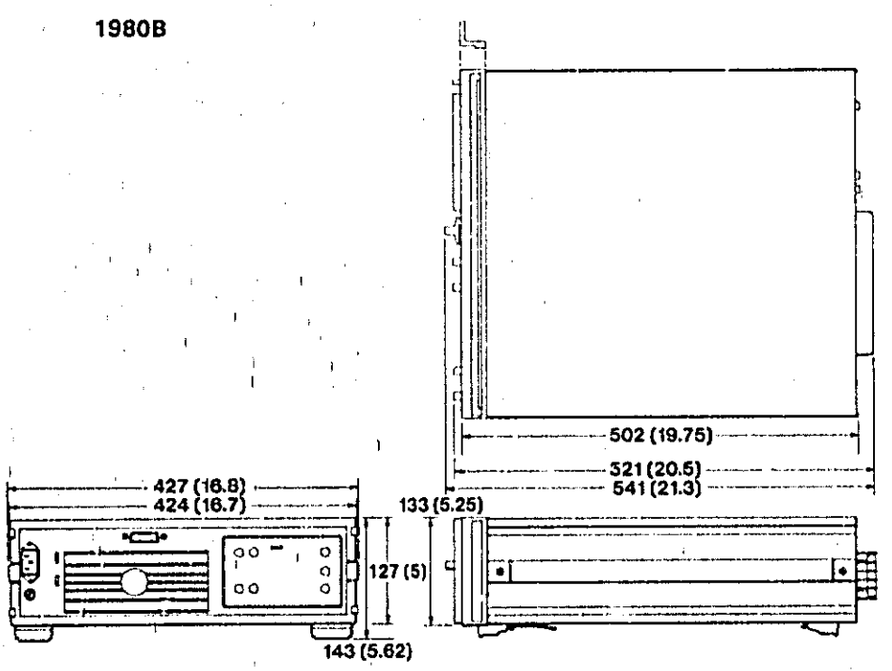


Table 1-2. Recommended Test Equipment

Instrument	Critical Specifications	Suggested Model	Use*
Cable Pair	50Ω BNC male to BNC male, approximately 9 inches long. Pair must be of equal length.	HP 10502A	P
Controller, HP-IB	HP-IB compatibility as defined by IEEE Std 488 and the identical ANSI Std MC1.1: SH1, AH1, T2, TE0, L2, LE0, SR0, PP0, DC0, DT0, and C1, 2, 3, 4, 5.	HP 9825B with 98213A and 98034A (revised) -or- HP 9835A with 98332A I/O ROM and 98034A (revised) -or- HP 85F	C,T
DC Source	level: 0 to 100 Vdc accuracy: ±0.25%	Ballantine 6125B	A,T
Digital Voltmeter (DVM)	range: 0 to 100 Vdc accuracy: ±0.1% input impedance: 10 MΩ	HP 3465A -or- HP 3438A	A,T
Electronic Counter	range: 0 to 10 MHz resolution: 8 digit accuracy: ±0.1 Hz	HP 5382A	A,T
Function Generator	range: 10 Hz to 100 kHz squarewave 2 kHz to 50 kHz sinewave level: 0 to 10 Vp-p	HP 3310A	A,T
LCR Meter	range: 3 pF to 20 pF accuracy: ±5%	HP 4332A	A
Oscilloscope	2 channels, delayed sweep sensitivity: 5 mV/div bandwidth: 100 MHz	HP 1740A	A,P,T
Peak to Peak Source	level: 20 mV to 100 V accuracy: ±0.25%	Ballantine 6125B	A,P,T
Power Divider	1- 50Ω input 2- 50Ω outputs	General Radio 874-TPDL	P
Probe	input R: 1MΩ shunt C: 12 pF division ratio: 10:1 compensation range: 20 to 26 pF	HP 10041A	A,P,T
Probe, High Voltage	division ratio: 1000:1 (into 10 Mohm DVM input)	HP 34111A	A,T
Sampling Voltmeter	bandwidth: 10 MHz to 100 MHz accuracy: ±3%	HP 3406A with HP 11063A Sampling Tee	P
Signal Generator	range: 10 MHz to 100 MHz	HP 3200B	P,T
Signature Analyzer	NO SUBSTITUTE	HP 5004A	T
Time Mark Generator	range: 5 nsec to 1 sec accuracy: ±0.01%	Ballantine 6125B	A,P,T

*A = Adjustments, C = Operator's Checks, P = Performance Testing, T = Troubleshooting

Table 1-3. Recommended Test Accessories

Accessory Type		Qty	Suggested Part
Adapter	GR874 to female BNC	2	HP 1250-0850
Adapter	GR874 to male BNC	1	HP 1250-0849
Attenuator	6 dB Attenuator	1	General Radio GR874 - G6
Tee	BNC, coaxial, one male, two female connectors	1	HP 1250-0781

Table 1-4. Alternate Test Equipment

Instrument Type	Suggested Alternate	Instrument Replaced	Advantages of Alternate
Controller, HP-IB	HP 9835A with 98332A and 98034A (revised)	HP 9825B with 98213A and 98034A (revised)	CRT Display HP Enhanced BASIC Larger Memory
	HP 85F	HP 9825B with 98034A and 98213A (revised)	CRT Display HP Extended BASIC Lower Cost
Digital Voltmeter (DVM)	HP 3438A	HP 3465A	HP-IB*

*HP-IB is Hewlett-Packard's implementation of IEEE Std 488 and the identical ANSI Std MC1.1.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

This section provides installation instructions for the Measurement System. Also included is information pertinent to initial inspection, preparation for use, storage, and shipment.

2-2. INITIAL INSPECTION.

WARNING

To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosure (covers and panels).

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked mechanically and electrically. The contents of the shipment should be as shown in figure 1-1. Procedures for checking electrical performance are given in the Operator's Checks in Section III and Performance Tests in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the electrical performance test, notify the nearest Hewlett-Packard Sales and Service office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection.

2-3. PREPARATION FOR USE.

2-4. Power Requirements.

The Measurement System requires a power source of 100, 120, 220, or 240 Vac +5/−10%; 48-440 Hz single phase. Power consumption is 200 VA maximum; with an expansion module and plug-in ROMs installed, power consumption is 300 VA maximum.

WARNING

This is a Safety Class I product (provided with a protective earth terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer for voltage reduction, make sure the comon terminal is connected to the earthed pole of the power source.

2-5. Line Voltage and Fuse Selection.

WARNING

For protection against fire hazard, the line fuse should only be replaced with 250 V, fast blow fuses with the correct current rating.

CAUTION

BEFORE CONNECTING THIS INSTRUMENT to line (Mains) voltage, be sure the line voltage switches are set correctly and that the proper fuse is installed.

If the line fuse burns out, do not replace it until the cause for failure has been determined and repaired by a qualified service person only. Replacing this fuse in a damaged instrument can cause additional damage.

The line voltage switch settings and line fuse are selected at the factory according to the line (Mains) voltage available in the country of destination. To operate the instrument from any other power source, proceed as follows:

a. Disconnect power cord.

b. Using a blade-type screwdriver, position rear-panel LINE voltage select switches for desired Vac input. (Figure 2-1 shows switches set for 120 Vac operation.)

c. Select and install proper line fuse. Fuse current ratings are printed on the LINE module on the instrument's rear panel and are listed with HP part numbers in table 2-1.

d. Reconnect power cord.

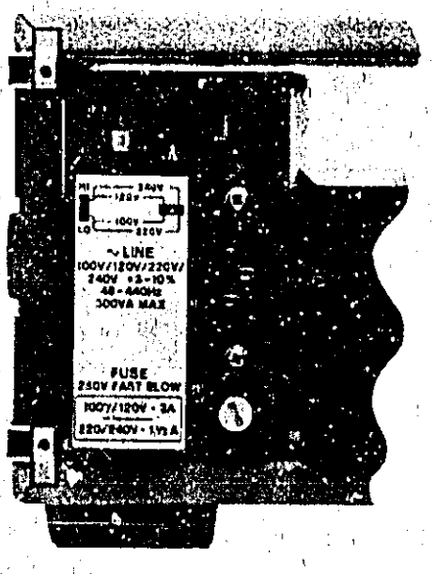


Figure 2-1. Line Voltage Selection Switches

Table 2-1. Line Fuse Part Numbers

Line Voltage	Fuse Rating	HP Part Number
100/120 Vac	250 V, 3 A Fast blow	2110-0003
220/240 Vac	250 V, 2 A Fast blow	2110-0002

2-6. AC Power Cable.

WARNING

BEFORE CONNECTING THIS INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (Mains) power cord. The Mains plug must be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two conductor outlet does not provide an instrument ground

This instrument is equipped with a three-wire power cable. When connected to an appropriate power receptacle this cable grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Figure 2-2 shows the part numbers (and associated Option numbers) for the power cables and plug configurations available.

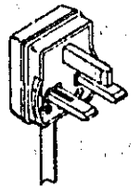
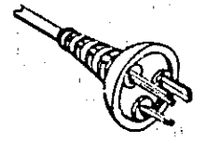
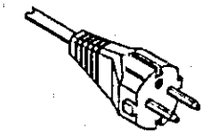
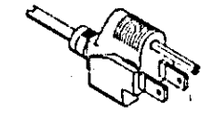
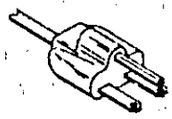
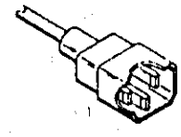
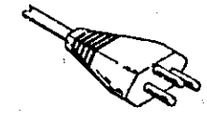
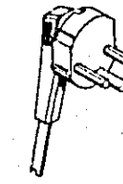
Option 900 United Kingdom 250 V  Plug: BS 1363A HP 8120-1703	Option 901 Australia/ New Zealand 250 V  Plug: NZSS 198/AS C112 HP 8120-0696	Option 902 European Continent 250 V  Plug: CEE7-VII HP 8120-1692	Option 903 USA/ Canada 125 V  Plug: NEMA 5-15P HP 8120-1521
Option 904 USA/ Canada 250 V  Plug: NEMA 6-15P HP 8120-0698	Option 905 Systems 250 V  Plug: CEE 22-VI HP 8120-2191	Option 906 Switzerland  Plug: SEV 1011.1959-24507 HP 8120-2296	Option 912 Denmark 220 V  Plug: DHCR 107 HP 8120-2956
NOTE: The number listed for the plug is the industry identifier for the plug only. The HP part number specifies a complete power cordset.			

Figure 2-2. Power Cable and Mains Plug Part Numbers

2-7. HP-IB Address Selection.

HP-IB

The HP-IB address is displayed or changed using the keys located on the left hand side of the CRT (refer to figure 2-3). To check the address setting, set the Measurement System LINE switch to ON and press OPTION MENU, then 9 1980A HP-IB.

This calls the HP-IB ADDRESS MODE menu (refer to figure 2-3). The current instrument address is on the second line of the display in decimal code. (Address "7" is preset at the factory.) Table 2-2 lists the decimal equivalents of the ASCII Talk and Listen codes. For a more complete listing of ASCII code equivalents, refer to table 3-30.

To change the HP-IB address, press:

3 INCREMENT or 4 DECREMENT

When the desired address is displayed, press OPTION MENU.

Note

The HP-IB address is stored in nonvolatile memory. Therefore, the address value is not affected by power-down. It can only be changed through the front-panel key sequence.

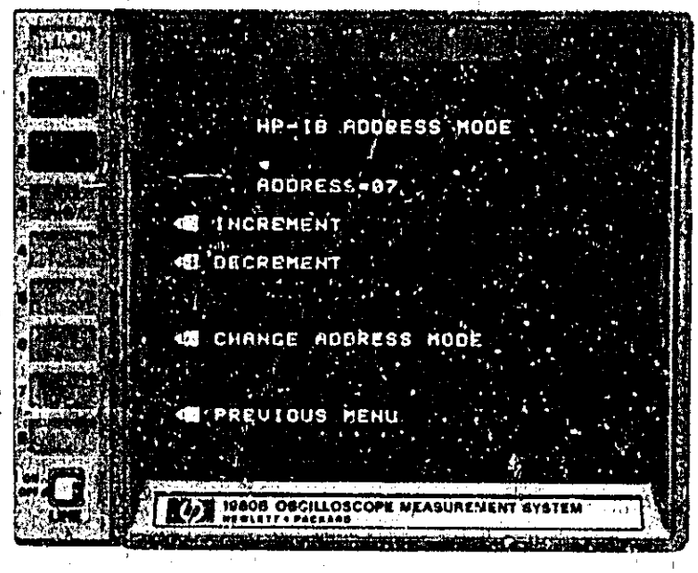


Figure 2-3. The Soft Keys and the HP-IB ADDRESS MODE *Menu*

2-8. Mating Connectors.

Coaxial Connectors. Coaxial mating connectors used with the Measurement System should be 50 ohm BNC male connectors.

HP-IB Interface Connector. Interconnection data for the Hewlett-Packard Interface Bus is provided in figure 2-4.

Chassis Ground. The front-panel chassis ground jack will accept a standard banana plug. The rear-panel chassis ground binding post accepts a standard banana plug or an 18 gauge wire.

2-9. Operating Environment

CAUTION

Do not block the instrument fan or ventilation holes. At minimum, 0.2 cm (1/16 inch) clearance should be provided around the top, bottom, and sides of the instrument.

Table 2-2. ASCII Address Codes to Decimal Equivalents

ASCII Address Codes		Decimal Equivalents
LISTEN	TALK	
<SP>	@	00
!	A	01
"	B	02
#	C	03
$	D	04
%	E	05
&	F	06
'	G	07
(	H	08
)	I	09
*	J	10
+	K	11
,	L	12
-	M	13
.	N	14
/	O	15
0	P	16
1	Q	17
2	R	18
3	S	19
4	T	20
5	U	21
6	V	22
7	W	23
8	X	24
9	Y	25
:	Z	26
;	[	27
<	\	28
=	]	29
>	^	30

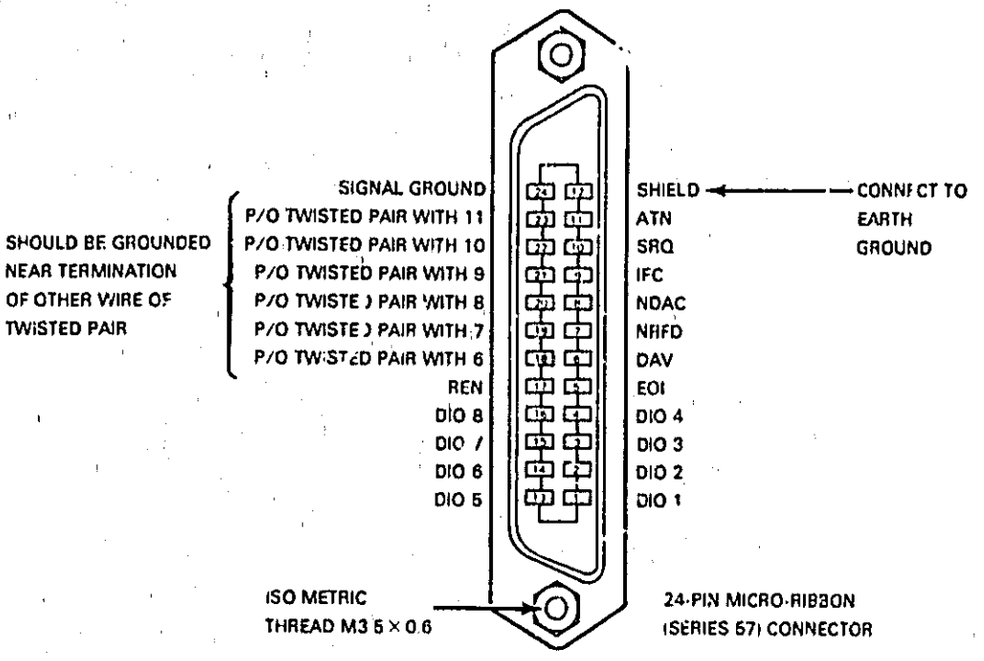
† Indicates factory set address.

The operating environment should be within the following limitations:

Temperature ..... 0°C to +55°C
Humidity ..... <95% relative at 40°C
Altitude ..... <4570 metres (15 000 feet)

2-10. Bench Operation.

The 1980A and 1980B cabinets have plastic feet and fold-away tilt stands for convenience in bench operation. The plastic feet are shaped to ensure positive alignment when the Measurement System is stacked with other instruments housed in Hewlett-Packard System I or System II enclosures. The tilt stands raise the front of the instrument for easier viewing of the front-panel.



Logic Levels
The Hewlett-Packard Interface Bus Logic Levels are TTL compatible, i.e., the true (1) state is 0.0 Vdc to +0.4 Vdc and the false (0) state is +2.5 Vdc to +5.0 Vdc.

Programming and Output Data Format
Refer to Section III, Operation.

Mating Connector
HP 1251-0293; Amphenol 57-30240.

Mating Cables Available
HP 10833A, 1 metre (3.3 ft)
HP 10833B, 2 metres (6.6 ft)
HP 10833C, 4 metres (13.2 Ft)
HP 10833D, 0.5 metres (1.6 ft)

Cabling Restrictions
1. A Hewlett-Packard Interface Bus system may contain no more than 2 metres (6 ft) of connecting cable per instrument.

2. The maximum accumulative length of connecting cable for any Hewlett-Packard Interface Bus system is 20.0 metres (65.6 ft).

Figure 2-4. Hewlett-Packard Interface Bus Connection

2-11. Rack Mounting.

Rack mounting information is provided with the rack mounting kits. If a kit was not ordered with the instrument as an option, it can be ordered through the nearest Hewlett-Packard Sales office. Refer to paragraph 1-8, Mechanical Options for the appropriate part numbers.

2-12. STORAGE AND SHIPMENT.

2-13. Environment.

The Measurement System may be stored or shipped in environments within the following limits:

Temperature	−65°C to +75°C
Humidity	<95% relative
Altitude	<15 300 metres (50 000 feet)

Protect the instrument from conditions which would cause internal condensation.

2-14. Packaging.

Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also mark the container FRAGILE to ensure careful handling. In correspondence, refer to the instrument by model number and full serial number.

Other Packaging. The following general instructions should be used for repackaging with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 2.4 MPa (350 psi) test material is adequate.

c. Use a layer of shock-absorbing material 75 to 100 mm (3- to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III

OPERATION

3-1. INTRODUCTION.

This section contains complete operating information for the 1980A/B Oscilloscope Measurement System. Included in this section are descriptions of all front and rear panel features, local and remote operation, operators checks, adjustments, and maintenance. Also included is a "Getting Acquainted" exercise which is designed to familiarize the first time user with front panel operation and features.

3-2. Operating Characteristics.

The 1980A/B Oscilloscope Measurement System is a two channel, 100 MHz oscilloscope which can be controlled via HP-IB. Complete instrument setups can be programmed and measurement results can be reported under remote control. Eight nonvolatile internal registers can be used for saving and recalling complete instrument setups during local or remote operation. Measurement System capabilities can be extended by adding various internal options and plug-in Expansion Modules.

Table 3-1 summarizes the major operating characteristics of the 1980A/B Oscilloscope Measurement System. For a complete description, refer to Table 1-1, Specifications. HP-IB capabilities are summarized in Table 3-3, Message Reference Table.

3-3. Local Operation.

Instructions for local (i.e., front panel) operation are described in the following paragraphs. To learn the basic operation of the instrument, begin with Simplified Operation and the Getting Acquainted exercise. Once familiar with the general operation, use the Detailed Operating Instructions for complete and in-depth information about operating the Measurement System.

Simplified Operation is an overview of front panel operation. It provides an introduction to basic operating procedures and front panel controls. An index to the Detailed Operating Instructions is opposite Simplified Operation to guide the operator to further information.

Getting Acquainted is an exercise for hands-on operation using the major instrument functions. Instrument operating procedures and some basic measurement techniques are explained. The exercise takes about 20 minutes to perform. The only equipment required is a 1980A/B and a probe.

Panel Features briefly describes all controls, connectors and indicators. Front panel features are discussed in figures 3-5 to 3-9. Rear panel features are in figure 3-10.

Detailed Operating Instructions provide a complete operating reference for the Measurement System user. They include information about the various measurements that can be made, as well as complete descriptions of all controls and menu functions. The instructions are arranged alphabetically by subject. They are indexed by function in table 3-2.

Each instruction contains a general description that covers signal levels, ranges, measurement limits, and other general information. Following the description, local operating procedures are explained and an example is given to illustrate the procedures. At the end of each instruction, any special considerations are listed that might aid the user. Also included are references to other instructions which contain related information.

3-4. Remote Operation.

Knowledge of local operation is essential for the remote operator to use the full capabilities of the Measurement System. Pages containing explanations of HP-IB related operations are noted with the HP-IB symbol. Instructions for HP-IB operation are in the following paragraphs:

Remote Operation, Hewlett-Packard Interface Bus presents a complete description of the instrument's bus implementation. It covers bus compatibility, HP-IB message response, general Data message (input and output) format rules, and many other basic bus considerations.

Detailed Operating Instructions explain how to program instrument functions and make bus controlled measurements. Specific format rules and any special programming considerations are described. Each instruction includes a programming example for reference. Table 3-2 indexes the Detailed Operating Instructions by function.

HP-IB Codes and Format Summary condenses the programming information for the instrument. It is a quick reference for the experienced remote operator. The summary lists all program codes by function and includes a complete description of parameter range and format.

Notation Conventions and Definitions explains the syntax conventions used in the manual.

3-5. Operator's Checks.

This section includes procedures that allow the operator to make a quick evaluation of instrument operation. The following checks are provided:

Confidence Test is a menu function that assures most of the instrument is operating properly. This procedure only requires a probe or BNC cable.

Memory Check is a menu function that verifies the content and operation of ROM and RAM memory. No additional equipment is required.

HP-IB I/O Check confirms that the Measurement System responds properly to all HP-IB messages. This check assumes that local operation has been verified with the Confidence Test and Memory Check procedures. An HP-IB controller, interface and connecting cable are required.

3-6. Operator's Calibration and Adjustment.

This section provides several procedures that should be used periodically to ensure measurement accuracy. Each procedure includes a brief description of the adjustment and the recommended calibration cycle. The following procedures are provided:

Delay Time Self-cal is a menu function that automatically nulls drift in the delay circuits. The Delay Self-cal routine should be executed before all critical measurements where the highest resolution and accuracy are required.

Vertical Balance Self-cal is a menu function that nulls the offsets within the vertical attenuators. Execute this routine if trace baselines shift as vertical deflection factor is changed.

CRT Display Adjustment explains how to set trace alignment, focus, and astigmatism.

Probe Compensation describes how to adjust the low frequency compensation of probes used with the Measurement System.

3-7. OPERATOR'S MAINTENANCE.

The only instrument maintenance an operator needs to perform is to occasionally clean the CRT contrast filter and the instrument front panels using a soft cloth and either a commercial glass cleaner, or a mild soap and water solution.

WARNING

Do not remove covers. Internal parts present an electrical shock hazard. Refer servicing to qualified service personnel.

CAUTION

Do not use chemical cleaning agents or abrasive cleaners that might damage the plastics in this instrument. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), or a solution of 1% mild detergent and 99% water.

3-8. GENERAL OPERATING INSTRUCTIONS.

WARNING

Before switching the instrument on, connect all protective earth terminals, extension cords, auto transformers, and devices to a protective earth grounded socket. Any interruption of protective earth grounding is a potential shock hazard that could result in personal injury or death.

Only use 250V fast blow fuses with the required current rating. Do not use repaired fuses or short circuited fuseholders. To do so could cause severe shock or fire hazard.

CAUTION

Before switching the instrument on, it must be set to the voltage of the power source, or damage to the instrument may result.

Do not operate the instrument with its enhancement slot uncovered. If there is no Expansion Module installed, the Expansion Module filler must be in place. Otherwise, damage to the instrument could result.

A stationary, high intensity spot (trace intensity level > 25) can cause CRT damage.

Excessive input voltage will damage the input attenuators and amplifiers. Observe the maximum input rating described in Table 1-1, Specifications.

Switch off instrument power before installing or removing Expansion Module. Otherwise, damage to the instrument or Expansion Module could result.

3-9. Power-on.

Power-on Procedure. Before turning the instrument on the first time, follow these instructions.

On the rear panel:

1. Check line voltage switches for correct voltage selection.
2. Check fuse for correct current rating. Current ratings are printed on the line module.
3. Plug in power cable.

Then set the front-panel LINE switch to ON.

Power-on Configuration. The Measurement System turns on with the same settings it had before it was switched off (that is, if line power was removed). The exceptions to this rule are described in the "Power-on Sequence and Default Conditions" Detailed Operating Instruction. The primary default conditions are:

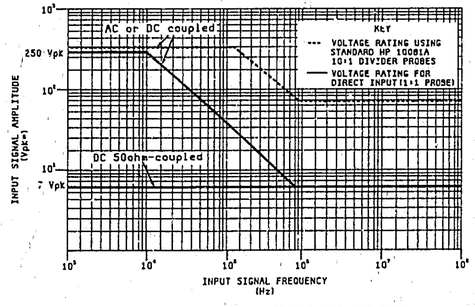
- Any DC 50 ohm vertical or trigger couplings are changed to DC.
- Menus are turned off.
- Advisory messages are enabled.
- All HP-IB conditions default except address and addressing mode selection.

Table 3-1. Operating Characteristics

Operating Parameter	Capability
Autoscope	Autoscope autoranges trigger level, deflection factor, and sweep speed for repetitive input signals >20 mV p-p and >50 Hz.
Calibrator Output	Frequency: 1.86 kHz Level: 1 V p-p, normal mode 20 mV p-p, 100 mV p-p, 200 mV p-p, and 10 V p-p can be programmed via HP-IB.
Delay Time	Range: 0.0 nsec to 9.999 sec
Digital Delay	Range: 0 to 99 999 999 trigger events
Delta Time	Range: (0-Tzero) sec to (9.999-Tzero) sec
Delta Volts (channel 1 and 2)	Range: ±15 times channel deflection factor
Horizontal Position	Range: ± 6 major divisions
Dual Separation	Range: ± 5 major divisions
Sweep Speed (main and delayed)	Range: 5 nsec/div to 1 sec/div
Trigger Level (main and delayed) internal source external source	 Range: ±20 major divisions Range: ÷1, ±1.2 V ÷10, ±12 V
Vertical Deflection (channel 1 and 2)	Range: 2 mV/div to 10 V/div
Vertical Position (channel 1 and 2)	Range: ± 15 major divisions

Operating Parameter	Capability
Implemented HP-IB Subsets	As defined in IEEE Std 488: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP0, DC0, DT1, C0, and E2.
Maximum Input Voltage (channel 1, 2, and external trigger inputs) DC 50 ohm-coupled DC or AC-coupled	 Level: 5 Vrms Level: 250 V (dc+peak ac) at ≤1 kHz

Maximum Input Voltage at Frequencies ≥1 kHz



*Vpk RATING BASED UPON CONTINUOUS SINE WAVE INPUT

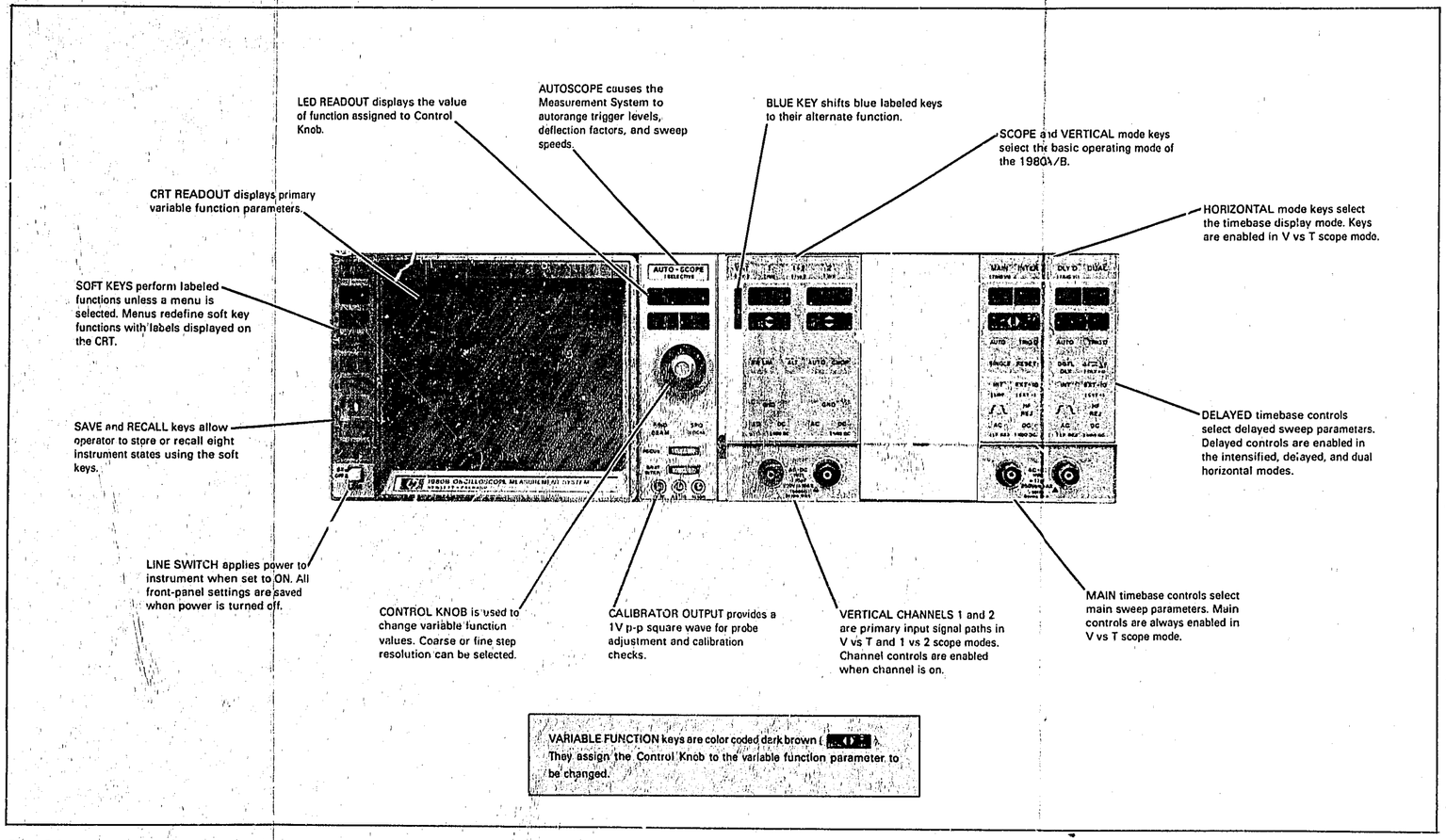


Figure 3-1.
Front Panel Features

SIMPLIFIED OPERATION

Obtaining a Basic Display

Use autoscope to quickly set up the 1980A/B for a basic, triggered display. Connect the signal to be viewed to channel 1 or 2, and press [AUTOSCOPE].

Indications

Active functions or operating modes are indicated by the lighted keys and the CRT readout.

Primary variable function values are displayed in the CRT readout for convenient reference.

Advisory messages are displayed on the CRT as an operator's aid. They are displayed momentarily when an illegal key entry is made or when other conditions occur that may require additional information.

Changing Values

Variable function values can be changed with the Control Knob.

Assign the Control Knob to a variable function by pressing the corresponding variable function key:

[INTEN TRACE]	trace intensity
[INTEN PANEL]	panel intensity
[CHAR INTEN]	character intensity
[VOLTS/DIV] (ch 1 or 2)	deflection factor
[POSITION] (ch 1 or 2)	vertical position
[SEC/DIV] (main or dly'd)	sweep speed
[TRIG LVL] (main or dly'd)	trigger level
[POSITION]	horizontal position
[DUAL SEP]	dual separation
[DELAY]	delay
[DELAY NUMERICAL]	delay, numerical entry mode

Then increment or decrement the function value by rotating the Control Knob.

The Control Knob is a stepping control. Coarse or fine step resolution can be selected with [FINE].

Soft Key Menus

The function of the soft keys is changed when a menu is called to the CRT. Menus redefine the soft keys with displayed labels such as:



The menus can be turned on and off by pressing [OPTION MENU].

Table 3-2. Detailed Operating Instructions Index

Instruction	Page
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Horizontal Mode	3-66
Horizontal Position	3-68
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Intensity, Trace	3-78
Scope Mode	3-88
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Instruction	Page
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Sweep Mode, Delayed	3-96
Sweep Mode, Main	3-98
Trigger, Delayed Sweep	3-107
Trigger, Main Sweep	3-112
Trigger Flag	3-117
Trigger View	3-120
Vertical Coupling	3-122
Vertical Deflection Factor	3-125
Variable Functions	
Control Knob	3-54
Delay	3-57
Delta Time	3-60
Delta Volts	3-62
Horizontal Position	3-68
Intensity, Characters and Lamps	3-77
Intensity, Trace	3-78
Reading Values Via HP-IB	3-84
Separation, Dual	3-90
Sweep Speed, Delayed	3-100
Sweep Speed, Main	3-102
Trigger, Delayed Sweep	3-107
Trigger, Main Sweep	3-112
Vertical Deflection Factor	3-125
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Vertical Functions	
Bandwidth Limit	3-49
Control Knob	3-54
Delta Volts	3-62
Vertical Coupling	3-122
Vertical Deflection Factor	3-125
Vertical Mode	3-127
Vertical Position	3-129

3-10. GETTING ACQUAINTED EXERCISE.

This exercise is designed to acquaint the user with front-panel operation of the Measurement System. It provides a demonstration of general operating features and many of the special functions. In addition, some basic measurement techniques are described. The exercise should take about 20 minutes to perform. The only equipment required is a 1980A/B and a probe.

CAUTION

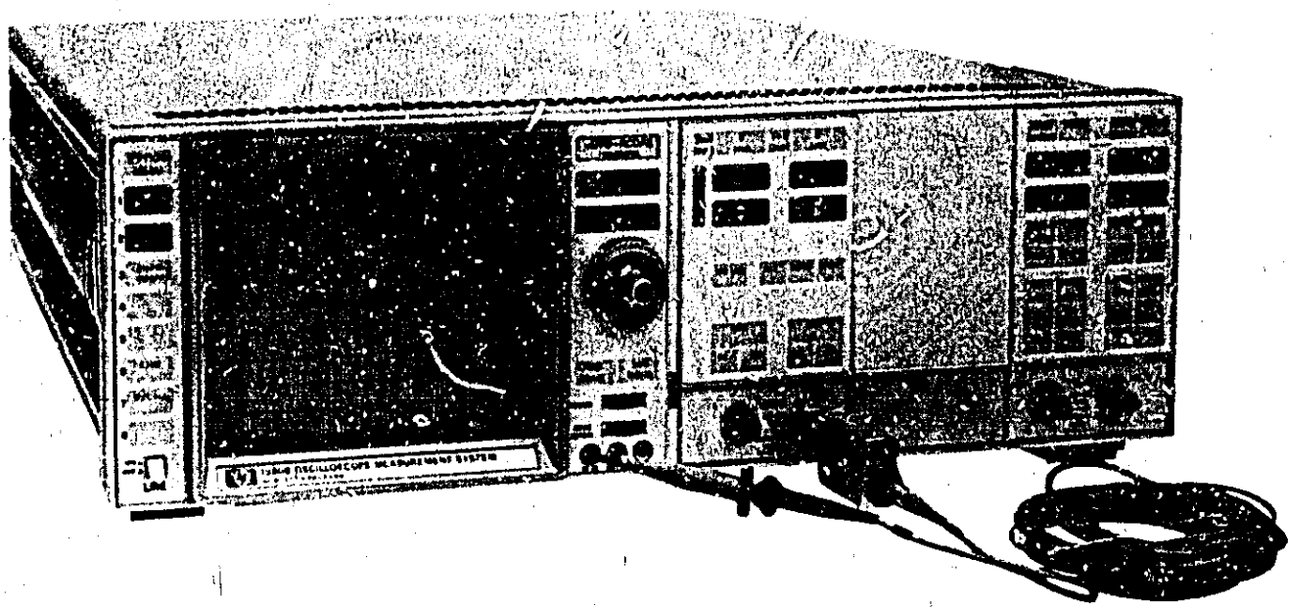
Before turning the instrument on the first time, follow these instructions.

On the rear panel:

1. *Check line voltage switches for correct voltage selection.*
2. *Check fuse for correct current rating. Current ratings are printed on the line module.*
3. *Connect power cable.*

Set the front-panel LINE switch to ON.

Set up the 1980A/B by connecting the calibrator signal to the channel 2 input (figure 3-2).



80-348

Figure 3-2. Getting Acquainted Exercise Setup

GETTING ACQUAINTED EXERCISE

INITIALIZE
Set LINE switch to OFF, then to ON.

3-11. Using Autoscope.

Autoscope is a convenient means of obtaining a basic display of an unknown signal. In executing autoscope, the 1980A/B scans the vertical inputs, selects trigger sources, and autoranges trigger levels, deflection factors and sweep speeds.

Execute autoscope, press AUTO-SCOPE.

After autoscope, the 1980A/B displays input signals plotted vs main sweep. Main sweep speed is selected to display ~2 cycles of the waveform. If only one signal is applied, deflection factor is selected so the displayed signal is ~3 divisions peak to peak.

For more information about the autoscope function, refer to the "Autoscope" Detailed Operating Instruction.

3-12. Keys and Indications.

Instead of conventional mechanical switches, the 1980A/B has membrane switch keys to control instrument operation. Instrument setup is stored in nonvolatile memory, so it is not lost when instrument power is cycled off and on. The keys are easy to operate, just press on the center of the key legend.

Active functions or operating modes are indicated by lighted keys. For example, press BW LIM to turn on vertical bandwidth limit. The key lights to indicate bandwidth limit is on.

SHIFT is used to select blue-labled shift functions. SHIFT shifts only the next key that is pressed. If the next key has no blue shift function, the normal function is performed. For example, to invert channel 2, first press SHIFT It lights to indicate that a blue function can be selected. Now press 2 INV to select inverted display. Invert is a toggling function, so press SHIFT 2 INV to restore noninverted display. Press SHIFT BW LIM. Because BW LIM has no blue function, the shift is ignored.

Advisory messages provide supplemental operating information. They are displayed momentarily on the CRT when invalid operations are attempted or when certain special conditions are in effect. For an example, press . The advisory KEY DISABLED is displayed to indicate the key has no function in the current operating mode. A description of all advisory messages (and suggested response) is contained in the "Advisory Messages" Detailed Operating Instruction.

Primary variable function parameters are displayed in the CRT readout. Figure 3-3 describes the readout display when channel 1 and 2, and both main and delayed timebases are on.

3-13. Changing Values.

Parameter values of variable functions are changed with the Control Knob. The Control Knob is a digital control with an "analog feel". Values set by the knob are stored in nonvolatile memory, so they are not lost when instrument power is cycled off and on.

GETTING ACQUAINTED EXERCISE

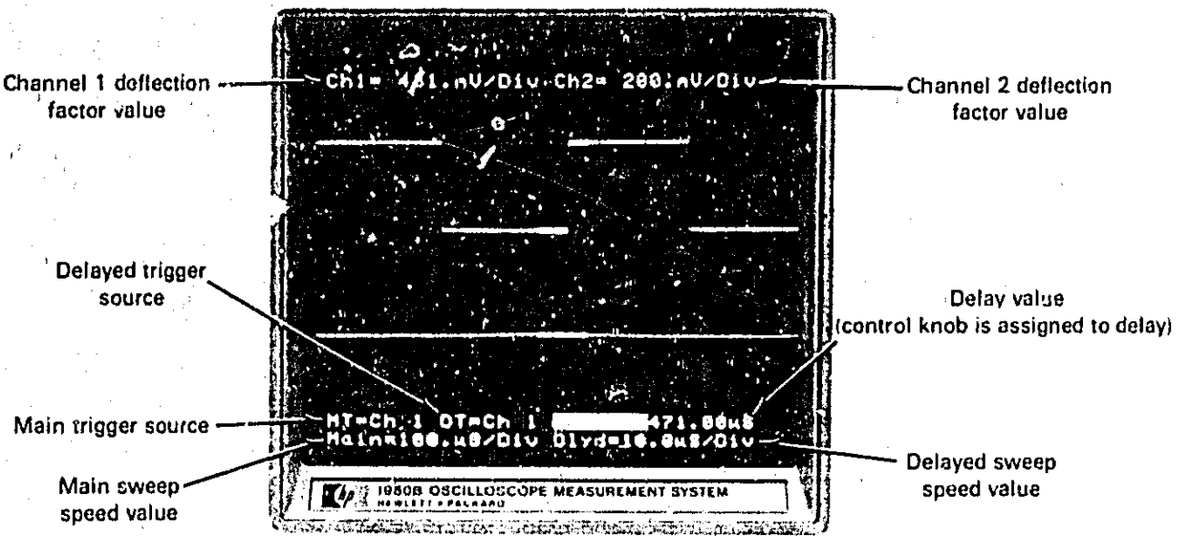


Figure 3-3. The CRT Readout

Executing autoscope assigns the Control Knob to main sweep speed. To indicate this selection, SECS/DIV (main) is lighted and the LED readout displays the main sweep speed value. Also, the CRT readout displays MAIN in inverse video to indicate that the Control Knob is assigned to main sweep speed.

Change the main sweep speed by rotating the Control Knob. Press FINE/COARSE to toggle between fine and coarse step resolution. When coarse is selected, sweep speed changes in relatively large steps. In contrast, fine provides a vernier-like adjustment that is continuously in calibration.

Now, change the deflection factor value for channel 2. Press VOLTS/DIV (ch 2) to assign the Control Knob. Notice the change in the CRT and LED readouts. Change the deflection factor by rotating the Control Knob. Again, try making both fine and coarse adjustments.

Accidental changes to values can be prevented by putting the Control Knob in hold mode. To select hold, press FINE/COARSE. To exit hold mode, press any enabled variable function key.

For more information about using the Control Knob, refer to the "Control Knob" Detailed Operating Instruction.

INITIALIZE
Press: OPTION MENU, AUTO, 1

3-14. Using the Trigger Controls.

With the 1980A/B, stable triggering is easy to establish using this general procedure:

Check that both the main and delayed sweeps are in auto sweep mode. AUTO and AUTO should both be lighted.

Select the signal source for the main sweep trigger. Since the calibrator signal is connected to channel 2, press INT 2. When INT is pressed, the advisory TO CHANGE INT SRC SEL CHAN is displayed. This is just a reminder to

GETTING ACQUAINTED EXERCISE

press either 1 or 2 to specify the source. Otherwise, the last internal trigger source is restored. The CRT readout displays the selected trigger source.

Press TRIG LEVEL (main) and adjust main trigger level with the Control Knob for a triggered display. As an adjustment aid, the trigger signal is displayed while the Control Knob is turned. The center horizontal graticule line represents the trigger threshold level with respect to the trigger signal.

When adjusting trigger controls, begin with the timebases in auto-sweep mode so there is a trace displayed. For example, press DLY'D (dly'd) to put delayed sweep in triggered mode. Because channel 1 is selected as the delayed trigger source and the trigger level is misadjusted, delayed sweep is not triggered. This inhibits main sweep and trigger view making it more difficult to correct the triggering problem. Notice that the delayed sweep NOT indicator is lighted. The NOT indicators show which sweep is not triggered. Press AUTO SWEEP A to return delayed to auto-sweep mode.

Now select the trigger source and level for delayed sweep. Press INT 2 TRIG LEVEL (dly'd) and rotate the Control Knob until trigger signal overlaps the center horizontal graticule line.

In some cases, it is desireable to display the trigger signal continuously. Press MAIN to display main trigger view.

The trigger circuits are both level and edge sensitive. Press ∫ ∖ (main) to toggle the main trigger point between positive and negative slope.

For more information about triggering, refer to the "Trigger, Delayed Sweep", "Trigger, Main Sweep" and "Trigger View" Detailed Operating Instructions.

INITIALIZE
Press: AUTO-SCOPE

3-15. Using Delayed Sweep.

This procedure describes some basic features of delayed sweep operation. Press INTEN to display delayed sweep as a marker on the main sweep.

When the delayed sweep is in auto mode, marker position is determined solely by the delay time value. Press DELAY TIME and change delay time with the Control Knob until the marker overlaps the falling edge of the first pulse.

Press DLY'D to display the delayed sweep. This provides an expanded view of the pulse edge.

Select dual horizontal mode, press DUAL. Dual displays both the main and delayed sweep traces. The main sweep marker indicates the portion of the waveform displayed in delayed sweep. Press ↕ (ch 2) and center the main sweep trace in the upper half of the CRT using the Control Knob. Press ◁▷ and use the Control Knob to change the separation between sweeps for convenient viewing.

Press SEC/DIV (dly'd) and change the delayed sweep speed with the Control Knob. Try using both coarse and fine. Because the sweep rates of the two timebases are independent of each other, delayed sweep can actually be slower than main sweep.

GETTING ACQUAINTED EXERCISE

Delayed sweep can start after main sweep is completed. Press [redacted] and rotate the Control Knob until the marker goes off screen. The advisory INTEN'D TRACE OFF SCREEN is displayed as a reminder that delay time value is longer than main sweep.

To zero the delay value, press [redacted].

For more information about delayed sweep, refer to the "Sweep Mode, Delayed" and "Sweep Speed, Delayed" Detailed Operating Instructions.

INITIALIZE
Press: [redacted]

3-16. Using Delta Volts.

Voltage measurements are simplified with the ΔV function. Try this procedure for peak to peak measurements:

Position channel 2 so the bottom peak of the waveform is on the center horizontal graticule line. Press [redacted] (ch 2) and position with the Control Knob.

Press [redacted] to turn on and zero the ΔV function.

Now make the voltage measurement. Change channel 2 position with the Control Knob until the top peak is on the center horizontal graticule line.

Read the peak to peak voltage (expressed as ΔV) in either the LED or CRT readout.

For more information about voltage measurements, refer to the "Delta Volts" Detailed Operating Instruction.

INITIALIZE
Press: [redacted]

3-17. Using Delta Time.

Timing or frequency measurements can be made quickly with the 1980A/B by using the ΔT function. Try this basic procedure for measuring pulse risetime:

Change channel 2 deflection factor so that the input signal is displayed as 5 divisions peak to peak. Press [redacted] (ch 2) and adjust with Control Knob.

Change channel 2 vertical position, if necessary, to center waveform. Waveform peaks should just reach the 0 and 100% points marked on the right hand side of the CRT. Press [redacted] (ch 2) and center with Control Knob.

Press [redacted] to display delayed sweep as a marker on waveform.

Change delay time until marker starts at the beginning of the rising edge of the second pulse. Press [redacted] and move marker with the Control Knob.

GETTING ACQUAINTED EXERCISE

Decrease marker width by increasing delayed sweep speed until marker just overlaps the pulse rising edge. Press [DLY'D] (dly'd) and adjust with the Control Knob.

Display the delayed sweep trace only, press [DLY'D].

Change delay time until pulse edge intersects the center vertical graticule line at the 10% point. Press [DELAY TIME] and change with the Control Knob.

Press [ΔT/1/ΔV] to turn on and zero the ΔT function.

Increase delay time with the Control Knob until the pulse edge intersects the center vertical graticule line at the 90% point.

Read the pulse risetime (expressed as ΔT) in either the LED or CRT readout.

For more information about timing measurements, refer to the "Delta Time" Detailed Operating Instruction.

INITIALIZE
Set LINE switch to OFF, then to ON.

3-18. Using Soft Key Menus.

Soft key menus add many special measurement and utility functions to the instrument. Menus redefine the soft keys with labels displayed on the CRT. To call the first level menu, press [OPTION MENU]. Figure 3-4 contains an explanation of the soft key functions defined by OPTION MENU.

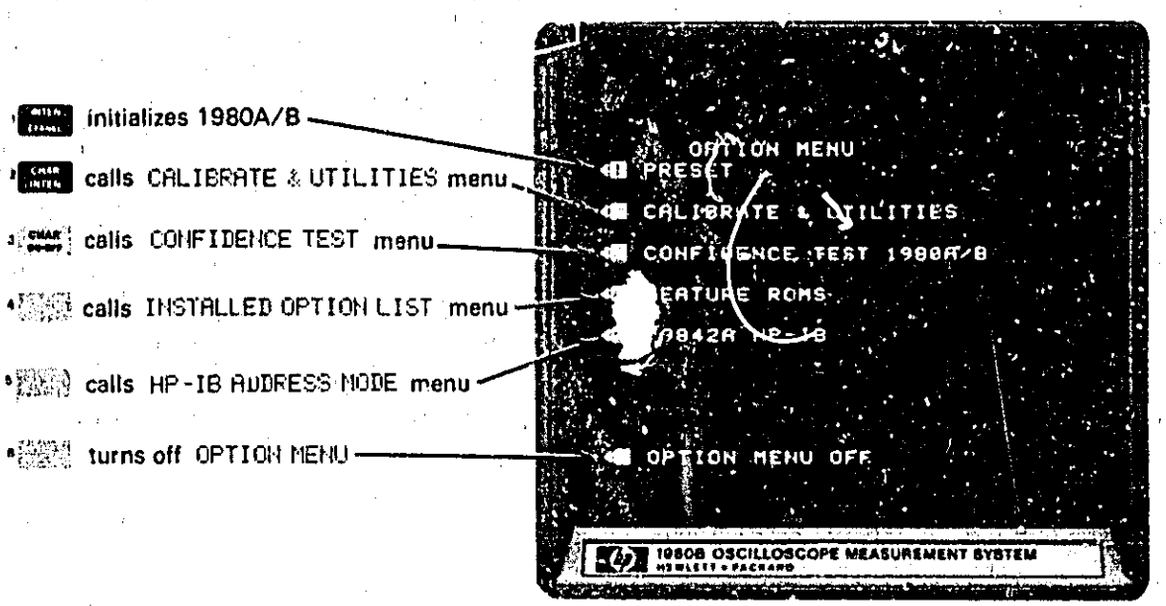


Figure 3-4. The OPTION MENU *Soft Key Definitions* 80-345

Press [CHAN] CONFIDENCE TEST 1980A/B. This calls CONFIDENCE TEST menu which contains instructions for the test. Press [CH2] to test channel 2.

GETTING ACQUAINTED EXERCISE

Confidence Test executes a series of autoscopes while changing the calibrator output level. It checks the vertical attenuators, and the vertical, horizontal, and trigger circuits. At the end of the test, an advisory is displayed to indicate whether the instrument passed or failed.

Now, call the UTILITIES menu by pressing:

OPTION MENU, CHAR ENTER CALIBRATE & UTILITIES
4 UTILITIES

Utility functions are primarily used for testing and servicing the instrument.

All menus (except OPTION MENU) provide backstep capability to allow returning to the previous menu. Return to the CALIBRATE & UTILITIES menu by pressing PREVIOUS MENU.

To return the soft keys to their normal functions, press OPTION MENU.

For more information about menu functions, refer to the "Soft Key Menus" Detailed Operating Instruction.

INITIALIZE
Set LINE switch to OFF, then to ON.

3-19. Using Save/Recall.

When a test sequence is used repetitively, instrument states can be stored in the Save/Recall registers for recall during the procedure. Up to eight instrument states can be stored. The registers are selected using the soft keys after the SAVE SETTINGS AT S[] menu is called.

Store the current instrument state in register S1, press SAVE, ENTER S1.

Change the instrument state, press OPTION MENU, ENTER PRESET.

Store this state in S2, press SAVE, CHAR ENTER S2.

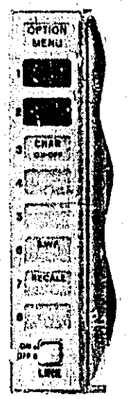
Recall S1, press RECALL, ENTER S1.

Recall S2, press RECALL, CHAR ENTER S2.

Refer to the "Save/Recall" Detailed Operating Instruction for more information.

3-20. PANEL FEATURES.

Soft Keys



OPTION MENU calls OPTION MENU which redefines the soft key functions with labels displayed on the CRT. When a menu is displayed, pressing OPTION MENU returns the soft keys to their normal functions.

INTEN assigns the Control Knob to trace intensity.

INTEN assigns the Control Knob to panel intensity.

CHAR INTEN assigns the Control Knob to character generator intensity.

CHAR toggles character generator on and off.

has no function except as defined by menus or options.

has no function except as defined by menus or options.

SAVE calls the SAVE SETTINGS AT SC] menu. The soft keys are then defined to store instrument state in the corresponding Save/Recall register. OPTION MENU turns off the SAVE SETTINGS AT SC] menu.

RECALL calls the RECALL SETTINGS AT SC] menu. The soft keys are then defined to recall the instrument state stored in the corresponding Save/Recall register. OPTION MENU turns off the RECALL SETTINGS AT SC] menu.

has no function except as defined by menus or options.

Figure 3-5. Display Panel Features

80-82

Channel 1 and 2 deflection factor is displayed if the channel is on or is selected as a trigger source. If ΔV mode is selected, Δ value is displayed instead of deflection factor.

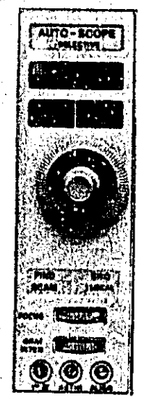
For 10 div measurements, 90% and 10% reference points are marked on the graticule.

For 5 div measurements, 100%, 90%, 80%, 20%, 10% and 0% reference points are marked on the graticule.

80-344

Main and delayed sweep speed, trigger source, and delay values are displayed if the timebase is on. If ΔT mode is selected, ΔT value is displayed instead of the delay value.

Figure 3-6. CRT Features



80-81

Autoscope

executes autoscope.

executes selective autoscope. Instrument autoranges deflection factor and sweep speed but preserves channel selection, coupling and trigger setups.

Delta Time and Delta Volts

selects ΔT mode if the Control Knob is assigned to delay ( ). If Control Knob is assigned to vertical position (ch 1 or 2), selects ΔV mode for the corresponding channel. If the Control Knob is assigned to a Δ function, pressing turns off that mode and restores normal delay time or vertical position control.

Control Knob

is used to change variable function parameter values. It is assigned to a function by pressing the corresponding variable function key. The function value is displayed in the LED readout.

toggles the Control Knob step resolution between fine and coarse.

puts the Control Knob in hold.

Beam Finder

changes the gain of the vertical and horizontal output amplifiers so that when the beam is off screen, it can be located.

Service Request

is used in remote operation to request service from the HP-IB controller.

Return to Local

switches the 1980A/B from remote to local mode unless local lockout is in effect.

CRT Adjustments

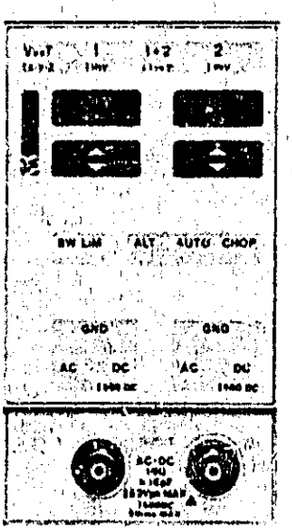
FOCUS adjusts spot size for sharp display.

GRAT INTEN illuminates the CRT graticule for photographing.

ASTIG adjusts spot shape for sharp display.

ALIGN adjusts the horizontal alignment of the sweeps with the CRT graticule.

Figure 3-7 Control Panel Features



80 81

Scope Mode

selects normal oscilloscope mode, input signals (Y-axis) plotted vs timebase signals (X-axis).

selects X-Y mode, channel 1 signal (Y-axis) plotted vs channel 2 signal (X-axis). Timebases are disabled.

selects display mode using rear-panel X, Y, and Z-blanking inputs. Disables channels 1 and 2, and timebases.

Blue Key

shifts blue labeled keys to their alternate function. applies only to the next key that is pressed. If the next key has no blue labeled function, the shift is ignored.

Vertical Mode

and toggle corresponding channels on and off. turns on channel 1 and 2, displays algebraic sum. Can be used for differential measurements when one channel is inverted with respect to the other. selects alternate or chop mode automatically.

and provide manual selection of alternate or chop mode.

Vertical Deflection Factor

(ch 1 or 2) asigns Control Knob to vertical deflection factor.

inverts channel 1.

inverts channel 2.

Vertical Position

(ch 1 or 2) assigns Control Knob to vertical position.

Vertical Coupling

, , and (ch 1 or 2) select the input signal coupling.

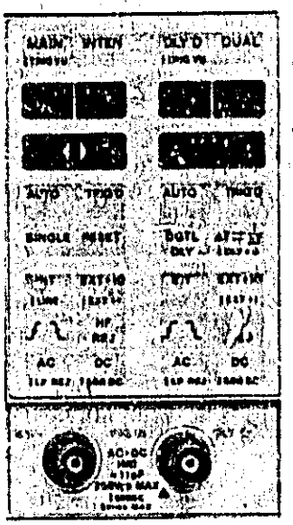
Bandwidth Limit

toggles bandwidth limit on or off. Can be used in V vs T or 1 vs 2 modes to limit vertical response.

Channel Inputs

Channel 1 and 2 inputs are female BNC connectors which have the special probe key contact. When the recommended HP probes are connected, channel deflection factor is displayed as the total value at the probe tip.

Figure 3-8. Voltage Panel Features



80-80

Horizontal Mode

MAIN enables and displays main timebase only.

INTEN enables main and delayed timebases. Displays delayed sweep as a marker on main sweep trace.

DLY'D enables main and delayed timebases. Displays delayed sweep only.

DUAL enables main and delayed timebases. Displays main and delayed sweeps in alternate or chop, depending on vertical display mode selection.

Trigger View

MAIN toggles the main trigger view on or off.

DLY'D toggles delayed trigger view on or off.

Horizontal Position

assigns Control Knob to horizontal position.

Dual Separation

assigns Control Knob to dual separation.

Sweep Mode

AUTO, TRIG'D, and SINGLE select the mode of main sweep operation.

AUTO, TRIG'D, and DLY'D select the mode of delayed sweep operation.

RESET resets both main and delayed sweeps.

Sweep Speed

SWEEP (main or dly'd) assigns the Control Knob to sweep speed.

Delay

DELAY assigns the Control Knob to delay, normal entry mode. If delayed sweep is in auto-sweep or triggered sweep modes, delay value is in units of time. In digital delay mode, delay is expressed as trigger events.

DELAY assigns the Control Knob to numerical time entry mode if delayed sweep is in auto-sweep or triggered sweep modes.

Trigger

TRIG LVL (main or dly'd) assigns the Control Knob to trigger level.

INT and INT select internal trigger source for main and delayed. Specify desired vertical channel by pressing 1 or 2.

EXT÷10 (main or dly'd) selects external÷10 trigger source.

EXT (main or dly'd) selects external÷1 trigger source.

LINE selects line trigger source for main sweep.

∫ (main or dly'd) toggles trigger slope between positive and negative edge.

HF REJ (main or dly'd) selects low pass filter on trigger signal.

AC (main or dly'd) selects high pass filter on trigger signal. Cannot be used in DC coupling.

AC, DC, and DC (main or dly'd) select the coupling for external trigger inputs.

External Trigger Inputs

Main and delayed inputs are female BNC connectors which have the special probe key contact. When the recommended HP probes are connected, external trigger level is displayed as the total value at the probe tip.

Figure 3-9. Time Panel Features

MAIN GATE OUTPUT: Provides ECL level (high = −0.8 V, low = −1.8 V) signal that is high during main sweep.

DLY'D GATE OUTPUT: Provides ECL level (high = −0.8 V, low = −1.8 V) signal that is high during delayed sweep.

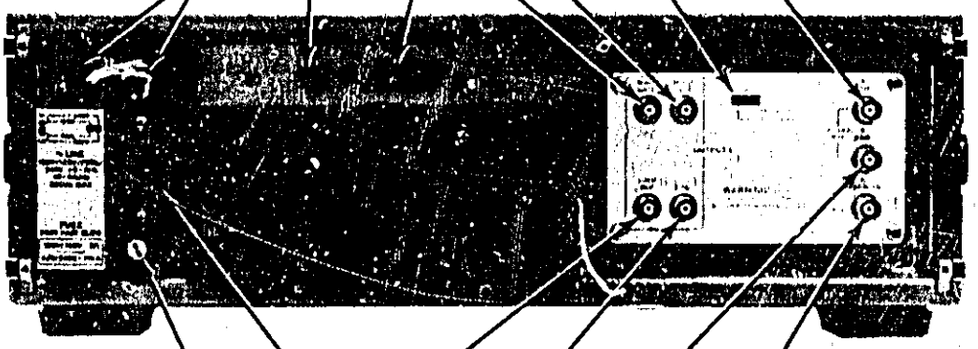
HP-IB: Connects the 1980A/B to the Hewlett-Packard Interface Bus for remote operation.

CHASSIS GROUND: Binding post accepts either a banana plug or 18 guage wire.

CAL SWITCH: Front-panel calibration is inhibited when the CAL switch is in the protected position. Refer to Section V of Service Manual.

VOLTAGE SELECTION: Switches must be set to voltage of applied power source. Refer to paragraph 2-5, Line Voltage and Fuse Selection for instructions about setting the line switches.

X AXIS INPUT: X-axis input from HP Model 1607A.



FUSE: Select fuse according to applied line voltage. Fuse part numbers are listed in table 2-1 of this manual. The 1980A/B is completely disabled if this fuse burns out. The line fuse should not be replaced until the cause of its failure has been determined.

Z BLANKING INPUT: Z-axis blanking signal from HP Model 1607A.

LINE: Receptacle provides a direct grounding connection to the 1980A/B chassis through the center contact. Available power cordsets are described in paragraph 2-6, AC Power Cable.

Y AXIS INPUT: Y-axis input from HP Model 1607A.

+15 V REF OUTPUT: Voltage reference for 1980A/B calibration. Source impedance is ~1kΩ; output level is 15 V±30 mV.

CAL OUTPUT: Frequency reference for 1980A/B calibration and calibration checks. Same as front-panel calibrator signal.

80-053

Figure 3-10. Rear-panel Features

HP-IB

3-21. REMOTE OPERATION, HEWLETT-PACKARD INTERFACE BUS.

The 1980A/B Oscilloscope Measurement System can be operated through the Hewlett-Packard Interface Bus (HP-IB). Menu functions, remote only functions, and all front panel functions (except those of FIND BEAM , LINE switch, and the CRT display adjustments) are programmable through the HP-IB. Bus compatibility, programming, and data format are described in the following paragraphs.

The notation used in this section to described bus communications is defined in paragraph 3-56, Notation Conventions and Definitions.

In this manual, the 1980A/B program codes are listed in ASCII code. Table 3-30, Commonly Used Code Conversions, includes a listing of ASCII characters and some commonly used equivalent codes.

A quick check of the instrument HP-IB functions is provided in the HP-IB I/O Check (paragraph 3-47). It verifies that the instrument can respond to or send each of the applicable HP-IB messages described in table 3-3.

For more information about HP-IB, refer to IEEE Std 488 (or the identical ANSI Standard MC1.1), "IEEE Standard Digital Interface for Programmable Instrumentation". The Hewlett-Packard catalog and the booklet "Improving Measurements in Engineering and Manufacturing" (HP part number 5952-0058) provide an overview of bus operation and useful information about HP-IB system applications.

3-22. HP-IB Compatibilty.

The Measurement System's complete bus compatibility as defined in IEEE Std 488 is presented in table 3-3.

The programming capability of the instrument is further described by the twelve HP-IB meta messages in the left hand column of table 3-3. Foremost among these is the Data message. Data messages contain the program codes that set the instrument's mode of operation.

Table 3-3. HP-IB Message Reference Table (1 of 2)

HP-IB Meta Message	Applicable	Instrument Response	Related Commands and Control Lines	Interface Functions
Data	Yes	All front panel, menu, and remote functions are bus programmable except LINE switch, FIND BEAM , and CRT adjustments. Also, all instrument settings may be read via the HP-IB.	DAB MLA EOI UNL EOS MTA UNT OTA	L3 T5
Trigger	Yes	Does not have device trigger capability, however, GET is decoded and available for use by internal or plug-in options.	GET MLA	DT1
Clear	Yes	Does respond to the Clear message.	DCL SDC	DC0

Table 3-3. HP-IB Message Reference Table (2 of 2)

HP-IB

HP-IB Meta Message	Applicable	Instrument Response	Related Commands and Control Lines	Interface Functions
Remote	Yes	Enabled to remote mode when the REN bus control line is true. However, it remains in local until it is addressed to listen the first time. Control Knob is put in hold on local to remote transition.	REN MLA	RL1
Local	Yes	Returns from remote to local when it receives the Local message or the key sequence [, SRQ LOCAL is pressed. Settings remain unchanged after the remote-to-local transition.	GTL MLA	RL1
Local	Yes	When in remote, and local lockout is in effect, the front panel is disabled. Only the system controller can return the instrument to local.	LLO	RL1
Clear Lockout/ Set Local	Yes	Returns to local and local lockout is cleared when the REN bus control line goes false.	REN	RL1
Pass/Take Control	No	The controller subset is not implemented.	TCT	C0
Require Service	Yes	Sets the SRQ line true when one of the service request conditions occur, if it has been enabled to send the RQS message for that condition.	SRQ	SR1
Status Byte	Yes	Responds to a Serial Poll Enable (SPE) bus command by sending an eight-bit byte when it is addressed to talk. Bit 7 (RQS bit) is true if the 1980A/B had set the SRQ bus control line true. The byte is cleared after it is read by the HP-IB controller.	SPE SPD STB	T5
Status Bit	No	Does not respond to a parallel poll.	PPE PPC PPD PPU	PP0
Abort	Yes	Is unaddressed to listen or talk.	IFC	T5 L3

1. Commands, Control Lines and Interface Functions are defined in IEEE Std 488-1978. Knowledge of these might not be necessary if your controller's manual described programming in terms of the twelve HP-IB Meta Messages shown in the left column.

2. The 1980A/B Oscilloscope Measurement System's complete bus capability as defined in IEEE Std 488-1978 is: SH1, AH1, T6, TE0, L3, LE0, SR1, RL1, PP0, DC0, DT1, C0, E2

3-23. HP-IB Status Display.

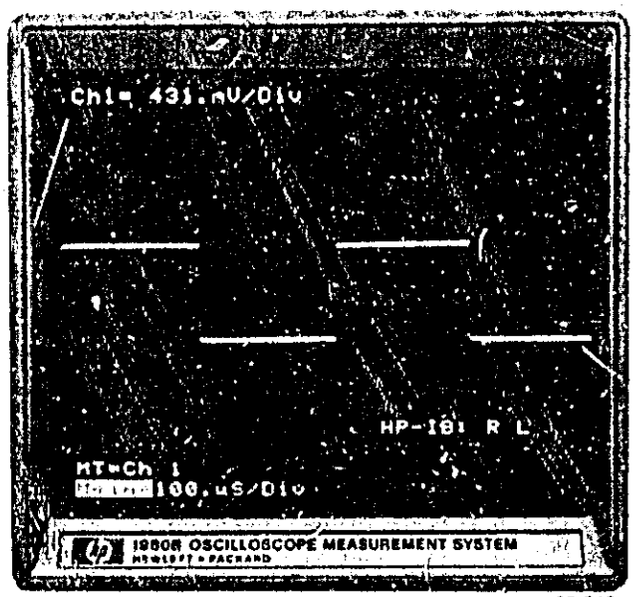
The status of the Measurement System on the HP-IB is annunciated on the CRT by a special HP-IB status advisory. For example, figure 3-11 shows the HP-IB status advisory displayed when the instrument is in remote mode and addressed to listen. The symbols displayed in the advisory and their indications are listed in table 3-4.

HP-IB

Table 3-4. Symbols Used in HP-IB Status Advisory

Advisory Symbol	HP-IB Status Indication
R	Switched to remote mode
L	Addressed to listen
T	Addressed to talk
S	Issued the Require Service message

The HP-IB status advisory is normally enabled. (It is enabled by default at power-on and when the HP-IB ADDRESS MODE menu is accessed.) The status advisory can be disabled by the remote operator; for further information, refer to the "HP-IB Status Advisory" Detailed Operating Instruction.



80-342

Figure 3-11. HP-IB Status Advisory

3-24. Remote Mode.

Remote Capability. The instrument communicates on the bus in both remote and local modes. In remote, all but a few of the front panel controls are disabled. The exceptions are the LINE switch, FIXED BEAM, |, SRQ LOCAL, and the CRT display adjustments. When Local Lockout is in effect, the return-to-local key sequence (| SRQ LOCAL) is also disabled.

The Control Knob can be enabled and assigned to specific functions while the instrument is in remote mode. This allows a local operator to make measurements or change settings under program direction. The procedure for this is described in the "Control Knob" Detailed Operating Instruction.

The Measurement System can be addressed to listen or talk while in remote mode. When addressed to listen, the instrument automatically stops talking and responds to Data messages. When addressed to talk, the instrument stops listening and sends either a Data message or the Status Byte. Whether addressed or not, the Measurement System responds to the Local, Local Lockout, Clear Lockout/Set Local, and Abort messages and, in addition, the Measurement System may issue the Require Service message. Although the 1980A/B does not respond to the Trigger message, this message is decoded and available for use by enhancement modules or internal options.

Local-to-remote Mode Changes. The Measurement System switches to remote upon receipt of the Remote message. The Remote message has two parts:

- Remote Enable (REN) bus control line true
- Device listen address (MLA) received once while REN is true

All instrument settings remain unchanged with the local-to-remote transition. However, the remote-to-local transition does put the Control Knob in hold. If the HP-IB status advisory is enabled, R is displayed in the status advisory to indicate remote mode.

If the Measurement System is set to listen-only or talk-only mode, the local-to-remote transition is inhibited.

3-25. Local Mode.

Local Capability. In local, the Measurement System's front panel controls are operational. Although it does not respond to input Data messages in local mode, if addressed to talk, the instrument can send Data messages and the Status Byte. Whether addressed or not, the instrument responds to the Remote, Local, Local Lockout, Clear Lockout/Set Local, and Abort messages. It also can issue the Require Service message in local mode.

Remote-to-local Mode Changes. The instrument always switches to local from remote whenever it receives the Local message (GTL) or the Clear Lockout/Set Local message. (The Clear Lockout/Set Local message sets the Remote Enable control line [REN] false.) If it is not in Local Lockout mode, the instrument also switches to local from remote when the key sequence [local] is pressed.

The instrument's settings remain unchanged during remote-to-local transitions. If the HP-IB status advisory is enabled, the remote indicator (R) turns off as the remote-to-local change is made.

3-26. Local Lockout.

When program control is interrupted, which can happen by returning the instrument to local via the front panel keystroke sequence, data or settings could be changed. This would leave the instrument in an unknown state. To prevent this, a local lockout is recommended. Local lockout allows return-to-local only under program control.

Note

Return-to-local can also be accomplished by turning the instrument off, then on again with the LINE switch. However, this technique has several potential disadvantages:

- It defeats the purpose of local lockout (that is, the system controller may lose control of the instrument).
- Other HP-IB conditions reset to default states at power-on.

3-27. Addressing.

The Measurement System interprets the byte on the eight bus data lines as an address or a bus command if the bus is in the command mode (Attention control line [ATN] true). In addressable mode, the instrument may be addressed to listen or to talk.

HP-IB

Once addressed to listen, the instrument remains configured to listen until it receives an Abort message (IFC), its own talk address (MTA), or a universal unlisten command (UNL) from the controller. Once addressed to talk, the instrument remains configured to talk until it receives an Abort message (IFC), another instrument's talk address (OTA), its own listen address (MLA), or a universal untalk command (UNT). If the status advisory is enabled, it indicates on the CRT when the instrument is addressed to talk (T) or addressed to listen (L).

The Measurement System is shipped from the factory in the addressable mode, with its talk and listen addresses set to "7" (ie, T7 and L7). Refer to table 3-30 for equivalent address codes. The instrument can also be configured in the talk-only or listen-only mode. These modes enable limited bus operation without an HP-IB system controller. The instrument's address and addressing mode may be displayed or changed from the front panel using the soft keys. Complete instructions for these procedures are in the "HP-IB Address" Detailed Operating Instruction.

Listen-only Mode. If the instrument is set to listen-only mode, it is always configured as a listener and responds to all Data messages sent on the HP-IB. However, it cannot output Data messages and it is inhibited from responding to the Remote, Local, Local Lockout, Clear Lockout/Set Local, or Abort messages. Also, it is disabled from issuing the Require Service message and cannot respond to a serial poll.

Note

In listen-only mode, the front panel is enabled (the instrument does not enter remote mode). Therefore, settings can be changed while a program is executing.

Talk-only Mode. If the Measurement System is set to talk-only mode, it is always configured as a talker and does not respond to any of the bus messages. Although the talk-only mode may be selected from the front panel, it is not supported by the 1980A/B standard firmware.

3-28. HP-IB Turn-on Default Conditions.

Several HP-IB parameters are reset at power-on. However, both the instrument's address and addressing mode are preserved in nonvolatile memory.

HP-IB parameter default conditions are:

- HP-IB local mode
- Local-lockout cleared
- Unaddressed (if in normal addressing mode)
- RQS mask cleared
- Service Request message cleared
- Status byte register cleared
- HP-IB status advisory enabled

3-29. Data Messages.

The Measurement System communicates on the HP-IB primarily with Data messages. The Measurement System interprets the byte on the eight bus data lines as a Data message when the bus is in the data mode (Attention control line [ATN] false)

The instrument can both receive and send Data messages. Input Data messages include the instrument's program codes (device-dependent commands) used to program front panel functions, menu functions, and all remote functions. Output Data messages include instrument status information and the settings of specific functions.

Of special consideration is the Learn String which can be sent and received by the instrument. It is a binary data string that contains a condensed coding of the entire instrument state. The Learn String is described in paragraph 3-32 and in the "Learn Mode" Detailed Operating Instruction.

The HP-IB Codes and Format Summary (paragraph 3-55) provides a list of all program codes for the 1980A/B. This summary includes a brief description of each code, specific format requirements, and a cross reference to further information in the Detailed Operating Instructions.

3-30. Receiving the Data Message.

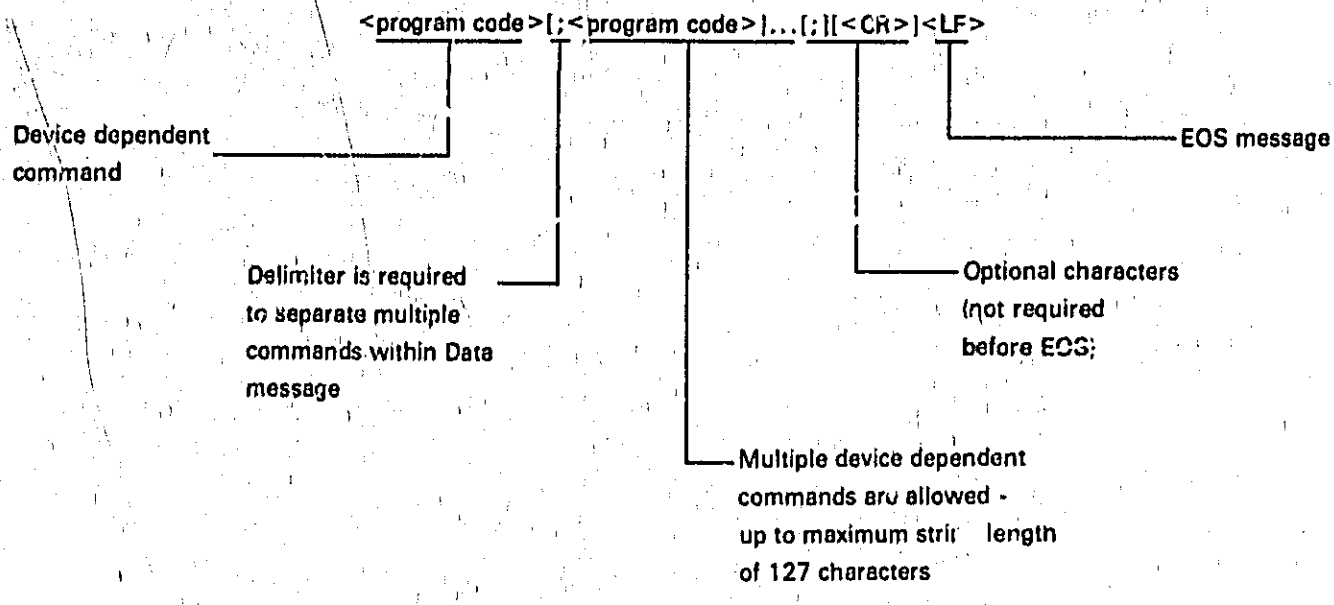
The Measurement System responds to Data messages when in remote mode (REN control line true) and is addressed to listen or when it is in listen-only mode.

Input Data Message Format. Input Data messages contain a string of device dependent commands (program codes) and an End-of-String (EOS) message. The program codes within a Data message are executed after the EOS message is received. The following format rules must be observed in all input Data messages:

- A linefeed (<LF>) is used as the End-of-String (EOS) message. Each Data message must be terminated by a (<LF>).
- Except during Learn String transfers, the carriage return character (<CR>) is not required before <LF>. Preceding <LF>, <CR> is treated as "no operation" and may be repeated as many times as permitted by the maximum string length limitation.
- When several program codes are sent in a Data message, a semicolon (;) must be used to delimit each program code except the last one in the string.
- Spaces (<SP>) are not allowed within input Data messages except as defined in the program code format description.
- The maximum length of a Data message string is 128 characters (including: semicolons, commas, <SP>, <CR>, and <LF>).

Errors in Data message syntax are trapped and can be reported via the HP-IB. For details about detecting and reporting format errors refer to the "HP-IB Syntax Errors" Detailed Operating Instruction.

General Input Data Message Format:



Program Order Considerations. Measurement System functions may be programmed in practically any order from the HP-IB. However, it is recommended that program code sequences should be in the same order used for front-panel operation. Generally, this requires that functions be set up starting with the most basic parameter to be changed. For example, before entering channel 2 deflection factor, turn on channel 2.

If an enhancement module or internal option for the instrument imposes any other order considerations, the manual for that option provides the necessary programming information.

Table 3-5 lists typical processing times for some sample Data messages. To minimize the processing time in a given application, use the learn string and save/recall registers to establish instrument configuration. When sending a series of program codes to the 1980A/B, processing time can be reduced by combining them into as few Data messages as possible. For example, note the execution time for the last two Data messages in table 3-5.

Program Code Format. Program codes consist of a two letter function identifier (i.e., prefix) and a parameter field. Suffixes are not used in 1980A/B program codes. The two letter identifier is a mnemonic that defines the major instrument function being addressed. Depending upon the identifier, the associated parameter field may contain zero, one, or multiple parameters. The general rules of program code format are:

- The 1980A/B sends and receives Data messages in standard ASCII code.
- The instrument responds equally to upper and lower case characters.
- Parameter fields containing multiple parameters require a comma (,) to delimit individual parameters.
- Program codes are space sensitive. Within program codes, spaces are accepted only immediately following function identifiers or parameter delimiters. (Exponential numeric entries use the character "E" or "e" as a delimiter between the mantissa and the exponent; spaces may follow "E", "e", or comma.)

Program code parameters are of five types, these are: integers, decimals, exponentials, ASCII character strings, and binary data. Integer, decimal, and exponential paremeters can be signed or unsigned. Specific format requirements for all program codes are given in the Detailed Operating Instructions section of this manual. They are also condensed in the HP-IB Codes and Format Summary.

Errors in program code format can be trapped and reported via the HP-IB. Refer to the "HP-IB Syntax Errors" Detailed Operating Instruction for a description of how to detect and report program code format errors.

Table 3-5. Typical Processing Times for Various Commands

Data Message	Execution Time* (Typical)	Function/Comments
SK7,1<CR><LF>	150 msec	Recall instrument state from register 1
SK6,1<CR><LF>	200 msec	Save instrument state in register 1.
IN<CR><LF>	380 msec	Execute initialize.
AS <CR><LF>	3.2 sec	Execute autoscope, calibrator connected to both channel 1 and 2.
SA<CR><LF>	2.7 sec	Execute selective autoscope one channel on with calibrator connected.
TX1,<any string>	20 msec	Write text on line 1 of the CRT text field.
RC1,1<CR><LF>	64 msec	Assign Control Knob to channel 1 deflection factor, fine resolution.
VM2<CR><LF>	70 msec	Turn on channel 2 only.
VS1,+2.00 E-3<CR><LF>	40 msec	Enter channel 1 deflection factor of 2 mV/div. If polarity change is made, add 54 msec.
VC1,2<CR><LF>	82 msec	Select DC coupling for channel 1.
HM2<CR><LF>	114 msec	Select intensified horizontal mode; time given is for change from main mode.
HM3<CR><LF>	70 msec	Select delayed horizontal mode, time given is for change from intensified mode.
MS50.0E-6<CR><LF>	55 msec	Enter main sweep speed of 50 µsec/div.
DY200E-3<CR><LF>	50 msec	Enter delay time of 200 msec.
DL200<CR><LF>	28 msec	Enter delayed trigger level of 2 div, internal source selected.
VM2;VC2,2;VS2,+2.00E-3 <CR><LF>	140 msec	Enter channel 2 coupling and sensitivity. Note the execution time improvement when several program codes are sent in a single Data message.
HM2;MS50.0E-6; MM1; MT+1,4; ML200<CR><LF>	260 msec	Select horizontal mode and main sweep speed, mode, trigger source, slope, level, and coupling.

*Execution time is measured from receipt of EOS message (<LF>). Maximum data input rate is 127 µsec/character

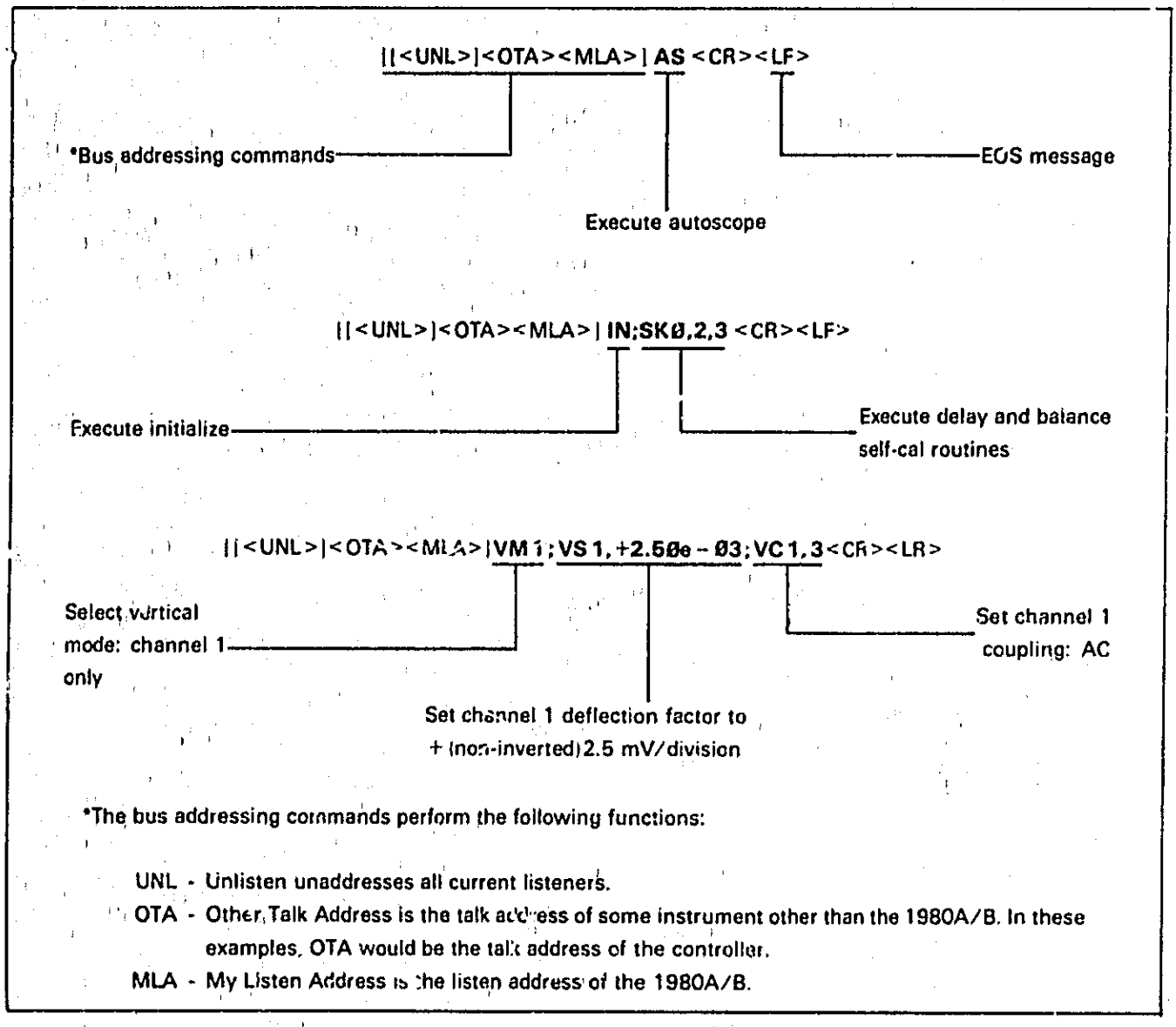


Figure 3-12. 1980A/B Input Data Message Examples

3-31. Sending the Data Message.

The instrument can send Data messages in local or remote mode, when it is addressed to talk or in the talk-only mode.

Note

Before the instrument is addressed to talk, the desired output data must be specified with the appropriate input Data message. Otherwise, the Measurement System outputs the ASCII character "E" by default to complete the bus transaction.

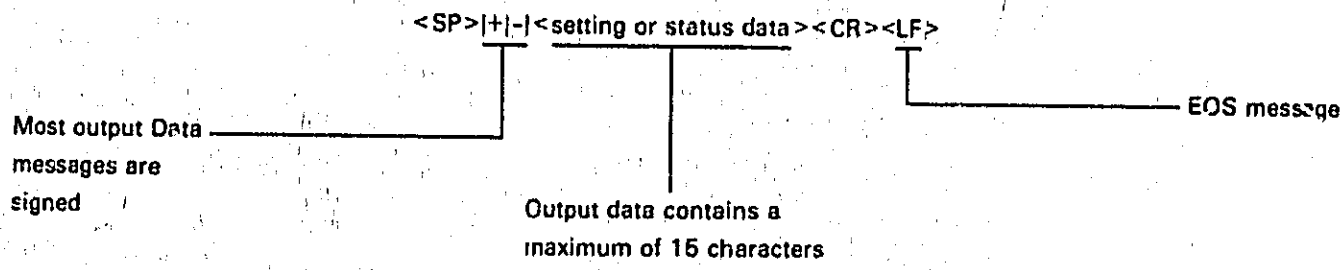
Output Data Message Format. Output Data messages include the settings of individual functions, instrument status information or binary Learn String data. Excluding the Learn String, there are three output data types: Integer, decimal, and exponential. All output Data messages contain a leading space (<SP>) followed by the function value or status data. <CR> and <LF> are sent as the EOS message for all output data except the Learn String. The Learn String uses the EOI bus control line to signal end-of-string.

For more information about output Data messages, refer to the "Reading Values Via HP-IB", "Instrument Status", and "Learn Mode" Detailed Operating Instructions.

Note

Exponential values are sent by the 1980A/B with the ASCII character "E" (uppercase) as the delimiter between the mantissa and the exponent.

General Output Data Message Format:



3-32. Learn Mode.

If the Measurement System receives a "TE" (Teach) program code and is then addressed to talk, it sends the Learn String. The Learn String consists of 80, 8-bit bytes containing information about front panel configuration. This binary data can be stored in the controller's memory for future use. The Learn String includes only those parameters that can be stored in the instrument's internal Save/Recall registers. The contents of the Save/Recall registers, however, are not included in the Learn String. Refer to the "Save/Recall" Detailed Operating Instruction for information about register limitations.

Note

The 80th byte of the Learn String is sent with the bus EOI line true, to indicate end-of-string.

When the Measurement System is addressed to listen, the binary data can be returned to it in a 80 byte string. The Measurement System interprets the first two bytes to determine that this is a Learn string. Following the 80th byte, the transfer must be terminated with <CR> and <LF>. When the <LF> is received, the instrument changes state according to the Learn String contents.

Note

During the transfer of the Learn String, the instrument can not be readdressed. If it is the transfer will be aborted. The 80 byte string should be sent or read by the controller using a technique that does not readdress bus devices.

For more information about using the Learn String, refer to the "Learn Mode" Detailed Operating Instruction.

3-33. Receiving the Clear Message.

Receiving the Clear Message sets all Soft Key menus to off, aborts a talk or listen, and clears all Service Requests.

3-34. Receiving the Trigger Message.

The 1980A/B does not respond to the Trigger message (GET bus command), although the message is received and available to internal and plug-in options.

3-35. Receiving the Remote Message.

The Remote message has two parts. First, the remote enable bus control line (REN) is held true, then the device listen address is sent by the controller. The Measurement System is enabled to go into remote when REN goes true but it does not actually switch into remote until addressed to listen the first time. No instrument settings are changed by the transition from local to remote, but the Control Knob is placed in hold. When actually in remote mode, the Measurement System displays R in the HP-IB status advisory to indicate remote mode.

3-36. Receiving the Local Message.

The Local message returns the Measurement System to front panel control. The Local message (GTL bus command) addresses the instrument to listen and then switches it from remote to local mode. If the HP-IB status advisory is enabled, the remote indicator (R) will turn off when the Local message is received. No instrument settings are changed by the remote-to-local transition.

Although the Local message returns front panel control, it does not clear local lockout. Unless the instrument receives the Clear Lockout/Set Local message, if local lockout is in effect, it will return to local lockout mode the next time it goes to remote.

3-37. Receiving the Local Lockout Message.

The Local Lockout message (LLO bus command) disables the Measurement System's front panel return-to-local keystroke sequence. Local Lockout is accepted when the instrument is in either remote or local mode. Afterwards, whenever the instrument is in remote mode, lockout is in effect. While the instrument is in local lockout, the remote-to-local transition can only be made from the system controller by sending the Clear Lockout/Set Local message or the Local message.

3-38. Receiving the Clear Lockout/Set Local Message.

The Clear Lockout/Set Local message (REN control line false) returns the Measurement System from remote to local mode and clears the local lockout condition. No instrument settings are changed by this message. It is accepted while the instrument is in either remote or local mode. If the instrument is in remote mode, the remote indicator (R) is blanked when the Clear Lockout/Set Local message is received.

3-39. Receiving the Pass Control Message.

The instrument does not implement the controller subset, therefore, it does not respond to the Pass Control message.

3-40. Sending the Require Service Message.

The Measurement System sends the Require Service message (by setting the SRQ bus control line and bit 7 of the status byte true) when a previously programmed condition occurs. The instrument can send the Require Service message in either local or remote mode. The Require Service message is cleared when a serial poll is executed by the system controller. During serial poll, the SRQ control line is reset immediately before the instrument places the Status Byte message on the bus. Figure 3-13

includes the conditions that can be selected to cause the Require Service message. If no conditions are selected, the Require Service message is disabled.

The Measurement System indicates having sent the Require Service message by displaying S in the HP-IB status advisory. This indicator is turned off during the serial poll when the SRQ control line is reset.

If the Measurement System is set to either listen-only or talk-only mode, it can not send the Require Service message.

For complete information about programming the condition that causes the Require Service message, refer to the "Service Request Condition" Detailed Operating Instruction.

Bit	8	7	6	5	4	3	2	1
Mask Weight	128	64	32	16	8	4	2	1
Service Request Condition	SRQ Key	RQS Bit	Plug-in Option Request	Internal Option Request	Advisory or Error	End of Sweep	Key Closure	HP-IB Syntax Error

Notes: 1. To set the RQS bit and SRQ bus control line true, the condition must be enabled in the RQS mask.

2. If no condition is enabled, the 1980A/B can not set the SRQ bus control line nor the RQS bit true. However, bits 1-6 and 8 of the status byte are set to indicate which conditions have occurred.

Figure 3-13. The Status Byte and the RQS Mask

3-41. Sending the Status Byte Message.

The Status Byte message consists of one 8-bit byte in which the bits are set according to the conditions described in figure 3-13. The Measurement System sends the Status Byte message when it is addressed to talk and it receives the Serial Poll Enable (SPE) bus command from the HP-IB system controller. After the message is transferred to the controller, all bits are cleared by the Serial Poll Disable (SPD) bus command, the Abort message, or if the instrument is unaddressed to talk.

If the instrument is set to either listen-only or talk-only mode, it does not respond to the SPE or SPD commands and can not send the Status Byte.

The Measurement System has two modes for transferring status information with the status byte:

If the Required Service message is not enabled (that is, if the RQS mask value is 0), a single status byte is available from the instrument. The bits in this byte are set to indicate all conditions that have occurred since the byte was last reset. In this mode, the RQS bit (bit 7 of the status byte) is always false. Figure 3-14 contains a typical flowchart for reading instrument status when the Require Service message is disabled.

If the Require Service message is enabled, as many as nine separate occurrences can be queued in a status byte register stack. Each byte in the stack has two bits set true: The RQS bit (bit 7) and the bit corresponding to the condition that occurred. The status register stack is read on a first-in, first-out basis by serial polling the Measurement System repetitively until it does not send the Require Service message. If there are more than nine occurrances before the register stack is read, the stack will contain the codes for the first eight conditions and for the last condition that occurred. Figure 3-15 contains a flowchart for reading instrument status using the Require Service message.

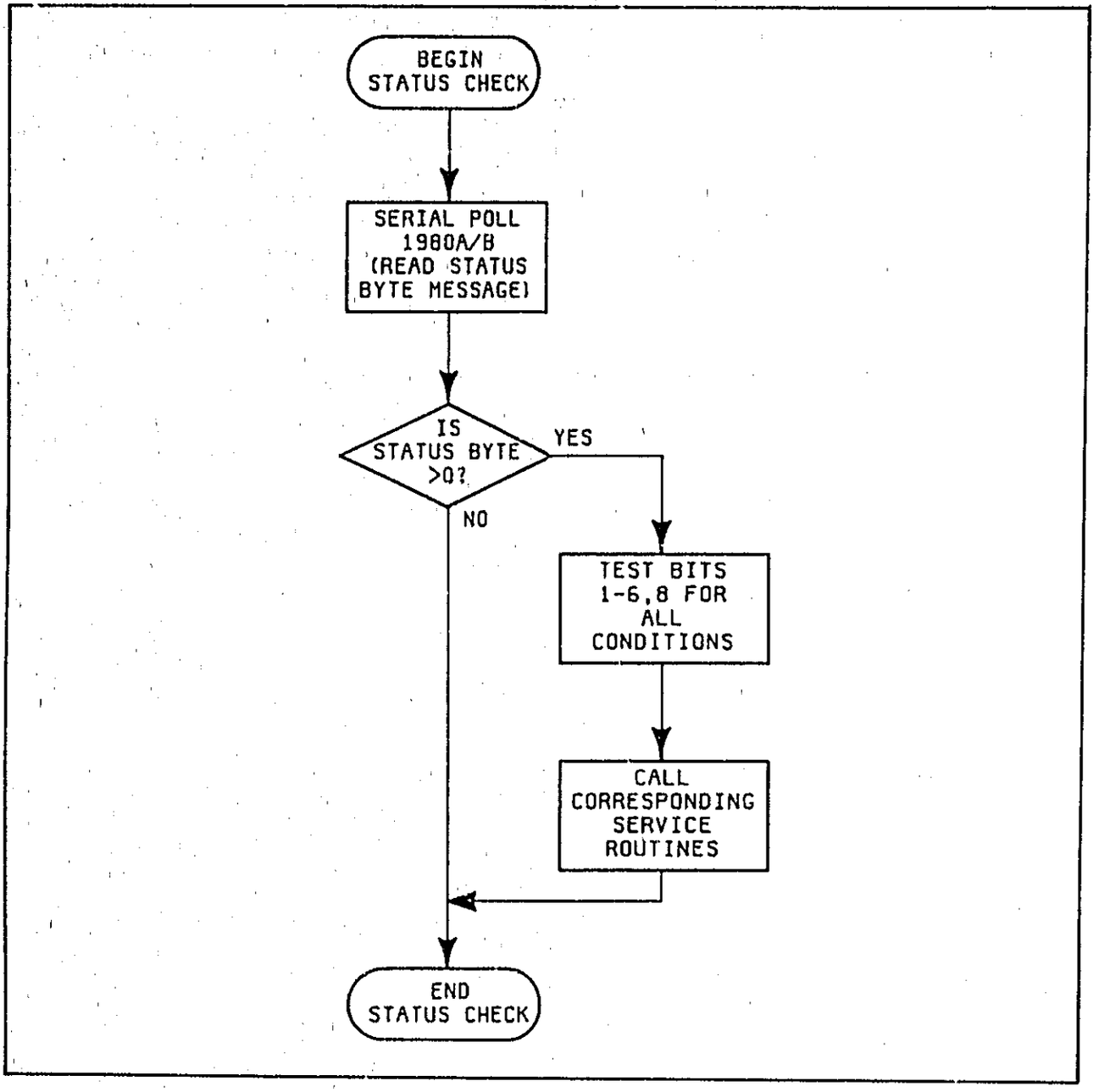


Figure 3-14. Serial Poll With Require Service Message Disabled (RQS Mask Value = 0)

To supplement the information in the Status Byte, there are status qualifier registers that can be read to determine which error occurred, which key was pressed, etc. For more information about using the status reporting features of the Measurement System, refer to the "Instrument Status" Detailed Operating Instruction.

3-42. Sending the Status Bit Message.

The Measurement System does not respond to a Parallel Poll Enable (PPE) bus command; it cannot send the Status Bit message.

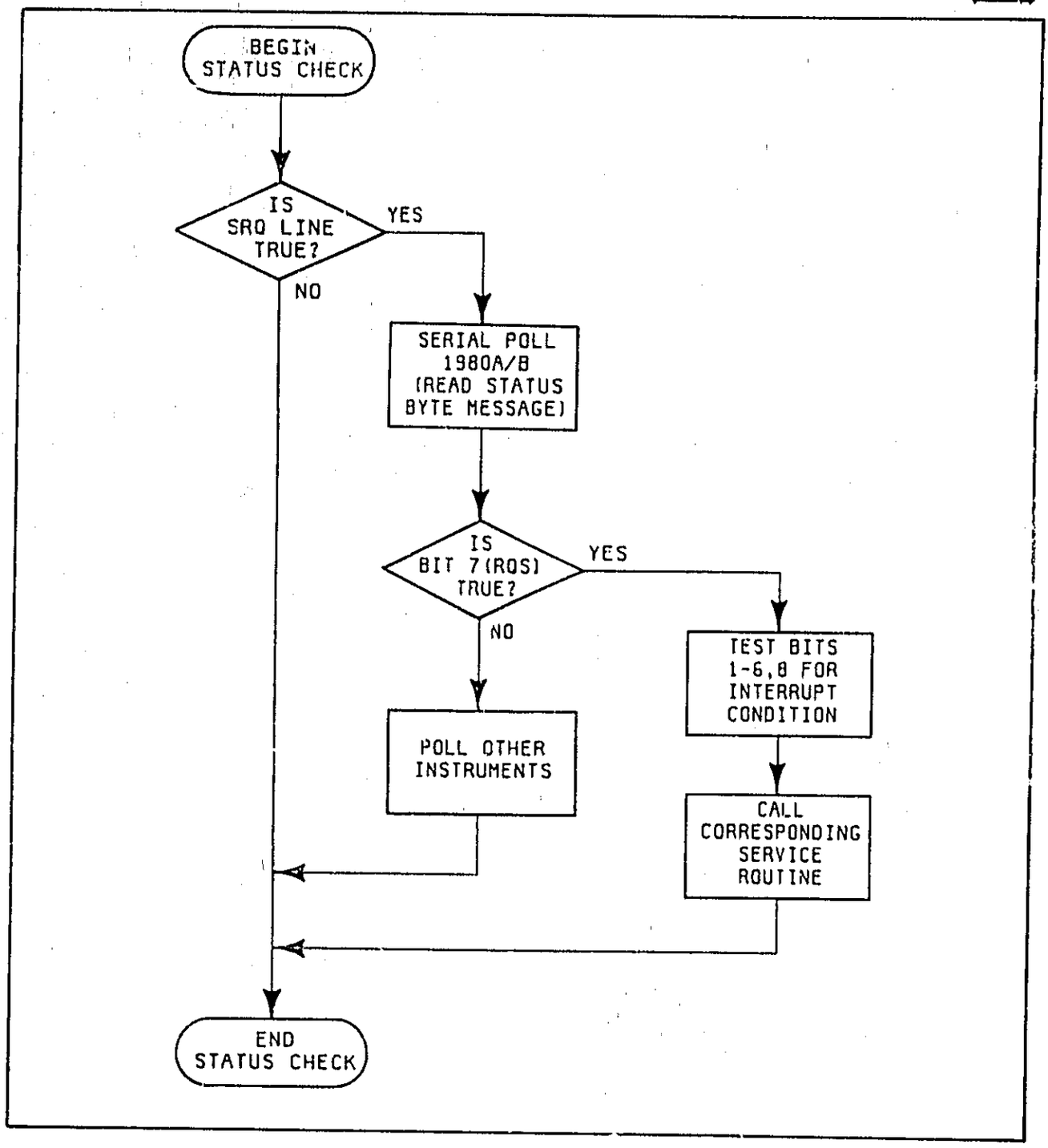


Figure 3-15. Serial Poll Using the Require Service Message (RQS Mask Value > 0)

3-43. Receiving the Abort Message.

The Abort message (IFC control line true) halts all bus activity. When the Measurement System receives the Abort message it becomes unaddressed and stops talking or listening. The Require Service message and the Status Byte are unaffected by the Abort message.

3-44. OPERATOR'S CHECKS.

3-45. Confidence Test.

Description Confidence Test can be executed from the front-panel to confirm that the internal 1980A/B hardware and software is functional. This test does not verify that the 1980A/B is operating to specifications. Only a 1:1 or 10:1 probe or a BNC cable is required to execute Confidence Test.

Procedure Select the CONFIDENCE TEST menu by pressing OPTION MENU > CHAR CONFIDENCE TEST 1980A/B.

Then, connect the calibrator signal to the vertical channel to be tested. To execute the test, press any key except , or FIND BEAM.

To exit the CONFIDENCE TEST menu without performing the test, press PREVIOUS MENU.

Indication If the instrument passes the Confidence Test, the PASSED TEST advisory message is displayed on the CRT.

If the instrument fails the Confidence Test, an error message is displayed in the LED Readout that indicates which failure was detected. The test is then aborted, the 1980A/B executes an autoscope to initialize itself, and the advisory FAILED TEST is displayed. The error messages that may be displayed during the Confidence Test are listed in table 3-6.

If no signal is applied to either input channel when the Confidence Test is executed, the advisory message SIGNAL NOT FOUND is displayed on the CRT in addition to the error message Err -31.

Table 3-6. Confidence Test Error Messages

Error Message	Error Description
Err -31	No signal found at channel 1 or 2.
Err -32	Horizontal range error
Err -33	10V range error
Err -34	1V range eror
Err -35	0.1V range error
Err -36	0.02V range error

Response If a failure is detected by the Confidence Test, the instrument might be useable but it does require servicing.

Comments At the end of the Confidence Test, the Measurement System executes an autoscope on the calibrator signal (at output level of 1 Vp-p). Previous front-panel settings are not preserved by this test. However, the Save/Recall registers and HP-IB status information are not changed.

The Confidence Test requires a front panel key closure to execute. The test cannot be executed via the HP-IB.

OPTION MENU can not be used to turn off the menus when the CONFIDENCE TEST 1980A/B menu is displayed.

3-46. Memory Check.

Description There are two memory checks: ROM Checksum and RAM Test. These checks assure that the 1980A/B memory is operating properly and that it contains valid data.

Procedure Both memory checks are in the UTILITIES menu which is called with the key sequence:

OPTION MENU › CHAR INTEN CALIBRATE & UTILITIES

4 UTILITIES

To execute ROM Checksum, select the UTILITIES menu, then press 6 ROM CHECKSUM. This routine can also be executed via the HP-IB by sending the Data message:

IN;SKØ,2,4,6 <CR><LF>

To execute the RAM Test routine, select the UTILITIES menu, then press 5 RAM TEST. This check can also be executed via the HP-IB by sending the Data message:

IN;SKØ,2,4,5 <CR><LF>

Indication When the instrument passes either the ROM Checksum or RAM Test, the advisory PASSED TEST is displayed on the CRT.

If the instrument fails a ROM Checksum or RAM Test, an error message is displayed in the LED readout that indicates where in memory the failure occurred. When the first error is detected, the routine is aborted and the advisory FAILED TEST is displayed.

Response If the instrument fails either the ROM Checksum or the RAM Test, it might be useable, but it does require servicing.

Comments Executing either the ROM Checksum or the RAM Test causes the advisory messages to be enabled. However, there are no other changes in instrument front-panel settings or status.

3-47. HP-IB I/O Check.

HP-IB

Description The following procedures check the Oscilloscope Measurement System's ability to process or send all of the applicable HP-IB messages described in table 3-3. In addition, the instrument's ability to recognize its HP-IB address is checked and all of the bus data, handshake, and control lines except DIO8 are set to both their true and false states. These procedures do not check whether or not all Measurement System program codes are being properly interpreted and executed by the instrument, however, if front panel operation is correct, the program codes, in all likelyhood are correctly implemented.

The validity of these checks is based upon the following assumptions:

- The instrument performs correctly when operated in local mode. This can be verified with the Contidence Test and the Memory Check (ROM Checksum and RAM Test) procedures in paragraphs 3-45 and 3-46 respectively.
- The bus controller properly executes HP-IB operations as defined by IEEE Std. 488.
- The bus controller's HP-IB interface properly executes the HP-IB operations.

HP-IB

If the Measurement System appears to fail any of these HP-IB checks, the validity of the above assumptions should be confirmed before attempting to service the instrument.

The controller's HP-IB interface select code is assumed to be "7". The Measurement System is assumed to be in the addressable mode with address "7" (T7/L7) selected. This select code-address combination (that is, 707) is not necessary for these checks to be valid. However, program lines in this procedure would have to be modified for any other combination.

These checks are intended to be as independent of each other as possible. Nevertheless, the first four checks should be performed in order before the other checks. Any special initialization or requirements for a check are described at its beginning.

Equipment

HP-IB Controller ..... HP 9825/98213A (General and Extended I/O ROM)
-or- HP 9835/98332A (I/O ROM)
-or- HP 9845 (with HP-IB I/O)

HP-IB interface ..... HP 98034A (revised)

Setup

Connect the Measurement System to the bus controller via the HP-IB Interface.

Procedure

Address Recognition. This check determines if the Measurement System recognizes when it is being addressed and when it is not. This check assumes only that the instrument can properly handshake on the bus. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON.

Description	HP 9825 (HPL)	HP 9835/45 (BASIC)
Set Remote Enable (REN) line false.	lcl 7	LOCAL 7
Send the 1980A/B listen address.	wrt 707	OUTPUT 707

The HP-IB status advisory should read: HP-IB: L

Unaddress 1980A/B by sending a different listen address.	wrt 721	OUTPUT 721

The HP-IB status advisory should turn off.

Remote and Local messages and | SRQ LOCAL |. This check determines if the Measurement System properly switches from local to remote control, from remote to local control, and whether the key sequence: | SRQ LOCAL | returns the instrument to local control. This check assumes that the Measurement System is able to both handshake and recognize its own address. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON.

Description	HP 9825 (HPL)	HP 9835/45 (BASIC)
Send Remote message by setting the REN line true and addressing 1980A/B to listen.	rem 707	REMOTE 707

The HP-IB status advisory should read: HP-IB: RL

Send Local message to 1980A/B.	lcl 707	LOCAL 707

The HP-IB status advisory should read: HP-IB: L

Send Remote message to 1980A/B.	rem 707	REMOTE 707

HP-IB status advisory should read: HP-IB: RL

Press | LOCAL | . The status advisory should change to read: HP-IB: L

Receiving the Data Message. This check determines if the Measurement System properly receives Data messages. This check assumes the instrument is able to handshake, recognize its own address, and properly make the remote/local transition. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON.

Description	HP 9825 (HPL)	HP 9835/45 (BASIC)
Set REN line true.	rem 7	REMOTE 7
Address 1980A/B to listen and send the Data message "execute autoscope".	wrt 707, "AS"	OUTPUT 707; "AS"

Check that the instrument executes an autoscope and that the HP-IB status advisory reads: HP-IB: RL

Sending the Data Message. This check determines if the Measurement System properly sends Data messages. It also verifies the 7 least significant HP-IB data lines can be sent and received in both their true and false states. This check assumes the instrument is able to handshake, recognize its own address, make remote/local transitions, and receive Data messages. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON and press OPTION MENU, PRESET.

Description	HP 9826 (HPL)	HP 9836/45 (BASIC)
Send Remote message to 1980A/B.	rem 707	REMOTE 707
Send a Data message to 1980A/B which instructs it to output the value of channel 2 deflection factor.	wrt 707, "OF2"	OUTPUT 707; "OF2"
Address 1980A/B to talk and store its output data in variable A.	red 707, A	ENTER 707; A
Display value of A	dsp A	DISP A

The HP-IB status advisory should read: HP-IB: RT
The controller's display should read 2.00 (9825) or 2 (9835/45)

Local Lockout and Clear Lockout/Set Local Messages. This check determines if the Measurement System properly receives the Local Lockout message and the Clear Lockout/Set Local message. This check assumes that the Measurement System is able to handshake, recognize its own address, and properly make the remote/local transitions. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON.

Description	HP 9826 (HPL)	HP 9836/45 (BASIC)
Send Remote message to 1980A/B.	rem 707	REMOTE 707
Send Local Lockout message.	llo 7	LOCAL LOCKOUT 7

The HP-IB status advisory should read: HP-IB: RL

Press: | SHIFT | LOCAL |. Advisory SCOPE UNDER REMOTE CONTROL should be displayed and the status advisory should remain unchanged.

Send the Clear Lockout/Set Local message.	lcl 7	LOCAL 7

HP-IB status advisory should read: HP-IB: L

Set REN line true.	rem 7	REMOTE 7
Address the 1980A/B to listen.	wrt 707	OUTPUT 707

Press: | SHIFT | LOCAL |. The HP-IB status advisory should read: HP-IB: L

Abort Message. This check determines if the Measurement System becomes unaddressed when it receives the Abort message. This check assumes that the instrument is able to handshake, recognize its own address, and make the remote/local transitions. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON.

Description	HP 9825 (HPL)	HP 9835/45 (BASIC)
Send the Remote message to 1980A/B.	rem 707	REMOTE 707

HP-IB status advisory should read: HP-IB: RL

Send the Abort message unaddressing 1980A/B.	cli 7	ABORTIO 7

If using a HP 9825, check that the HP-IB status advisory reads: HP-IB: R. If using a HP 9835 (or 9845), check that the HP-IB status advisory is turned off. (The 9835 and 9845 send the Local message and the Abort message with the ABORTIO command.)

Send Local message (HP 9825 only).	lcl 707	The Local message was sent with ABORTIO statement.
Address 1980A/B to talk.	red 707	ENTER 707
Send Abort message unaddressing 1980A/B.	cli 7	ABORTIO 7

Check that the HP-IB status advisory is off.

Require Service Message. This check determines if the Measurement System can issue the Require Service message (set the SRQ bus line true). This check assumes that the Measurement System is able to handshake, recognize its own address, make remote/local transitions, and receive Data messages. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON.

Description	HP 9825 (HPL)	HP 9835/45 (BASIC)
Set REN line true.	rem 7	REMOTE 7
Address 1980A/B to listen and send a Data message enabling a Require Service message to be sent if a key closure occurs.	wrt 707, "IM2"	OUTPUT 707; "IM2"

Press MAIN. HP-IB status advisory should read: HP-IB: RL

Read binary status of the controller's HP-IB interface and store data in variable A.	rds(7)→A	STATUS 7; A
Display value of SRQ bit.	dsp "SRQ=", bit (7,A)	DISP "SRQ="; BIT (A,7)

The SRQ value should be displayed as 1.00 (9825) or 1 (9835/45), indicating that the Measurement System issued the Require Service message.

Status Byte Message. This check determines if the Measurement System sends the Status Byte message in both local and remote modes. This check assumes that the Measurement System is able to handshake, recognize its own address, and make local/remote transitions. Before beginning this check, set the Measurement System LINE switch to OFF, then to ON.

Description	HP 9825 (HPL)	HP 9835/45 (BASIC)
Conduct a serial-poll and display Status Byte value.	rds (707)	STATUS 707; A DISP A

Check that the HP-IB status advisory remains off and the controller display reads 0.00 (HP 9825) or 0 (HP 9835 and 9845).

Press [RESET].

Send Remote message to 1980A/B.	rem 707	REMOTE 707
Conduct a serial-poll and display Status Byte value.	rds (707)	STATUS 707; A DISP A

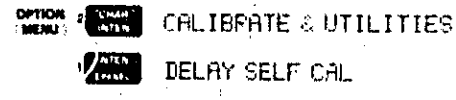
HP-IB status advisory should read: HP-IB: RL
Controller display should read 130.00 (HP 9825) or 130 (HP 9835/45).

3-48. OPERATOR'S CALIBRATION AND ADJUSTMENT.

3-49. Delay Time Self-cal.

Description To maintain the specified delay time performance, execute the following delay self-calibration procedure approximately once each hour.

Procedure The delay time self-cal can be executed with the key sequence:



It can also be executed via the HP-IB by sending the Data message:

IN; SKØ, 2, 1 <CR><LF>

Indication As the delay self-cal is executing, the LED readout displays a number which represents the relative delay drift. As the drift is nulled, this displayed number approaches zero. When the self-cal routine is finished, the Measurement System is restored to the settings it had before the self-cal was initiated.

If the drift cannot be corrected by the self-cal routine, the instrument executes the self-cal repetitively until a key is pressed or the LINE switch is cycled OFF and ON.

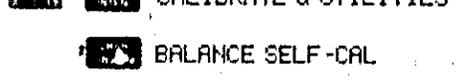
To express the delay drift in terms of percentage error, divide the value displayed in the LED readout by 1999.87. For example, if the value "30" is displayed, the drift is: 30/1999.87=0.015%

Response If the self-calibration routine cannot correct the drift entirely, internal adjustment is required. Although the Measurement System may still be functional, it does require servicing.

3-50. Vertical Balance Self-cal.

Description The vertical balance self-cal routine nulls gain dependent offsets in the vertical pre-amplifiers. The self-cal routine virtually eliminates baseline shift as vertical deflection factor is changed. The balance self-cal should be performed whenever there is noticeable shift of the vertical baseline as deflection factor is changed.

Procedure To execute the balance self-cal from the front panel of the 1980A/B, press the following key sequence:



The balance self-cal can be executed via HP-IB by sending the Data message.

IN;SKØ, 2, 2 <CR><LF>

Note

Do not apply any signals to channel 1 or 2 inputs while executing the balance self-cal procedure.

Indication While balance self-cal is executing, advisory message BALANCE SELF-CAL CH1 (or CH2) is displayed on the CRT. When the balance routine is finished, the Measurement System is restored to the same settings it had before the self-cal was initiated.

If the balance routine cannot calibrate one of the vertical channels, an error message is displayed in the LED readout to indicate which channel failed. The instrument can be programmed to issue the Require Service message to signal this failure, refer to the "Error Messages" and "Service Request Condition" Detailed Operating Instructions for further information.

Response Although a vertical balance self-cal failure indicates the Measurement System should be checked by qualified service personnel, the accuracy of measurements taken with the instrument are not impaired.

3-51. CRT Adjustments.

Description Controls are provided on the front-panel of the 1980A/B for operator adjustment of the CRT display. Because trace alignment with the graticule is affected by the orientation of the instrument with the ambient magnetic field, the display may have to be realigned after the instrument is installed or moved. The ASTIG and FOCUS controls may have to be periodically adjusted for optimum focus.

Procedure **Trace Alignment.** With no signal applied to either vertial channel input, press AUTO-SCOPE.

Using a small screwdriver or alignment tool, adjust the front-panel ALIGN control (on CONTROL panel) for best alignment of trace with horizontal graticule lines.

Astigmatism and Focus. Set trace intensity to level 22, press [illegible] and adjust with the Control Knob.

Select 1 vs 2 scope mode, press [illegible].

Ground channel 1 and 2 inputs, press [illegible] (ch 1), [illegible] (ch 2).

Adjust ASTIG control for best spot shape (i.e., most radically symmetric spot).

Adjust FOCUS control for smallest spot and for well defined characters.

3-52. Probe Compensation.

Description Probe compensation may be required because of variations in total input resistance and capacitance from one instrument or input to another. To compensate a probe, proceed as follows:

Procedure Connect probe to the input of vertical channel 1.

Connect the probe tip to the front-panel calibrator terminal.

Select DC coupling for channel 1, then execute a selective autoscope. Press DC (ch 1) | AUTO-SCOPE.

Adjust divider probe low frequency compensation for correct display (figure 3-16).

3-53. DETAILED OPERATING INSTRUCTIONS.

3-54. Using the Detailed Operating Instructions.

These Detailed Operating Instructions contain all the information needed to operate the 1980A/B. The instructions are arranged alphabetically; a functional index appears in table 3-2.

The following considerations should be remembered when using the Detailed Operating Instructions:

- Procedures and examples assume the instrument is in the initialized state (refer to the "Initialize" instruction).
- The procedures and examples for HP-IB operation include only the program codes (device dependent commands) needed for remote operation. The HP-IB command mode messages (such as REN, MLA, MTA, and UNL) that are

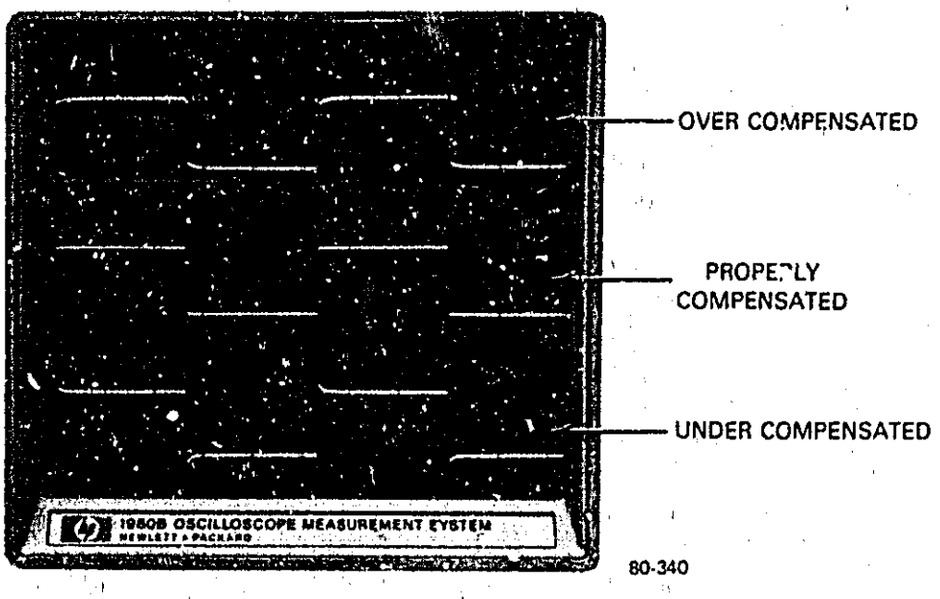


Figure 3-16. Divider Probe Adjustment Display

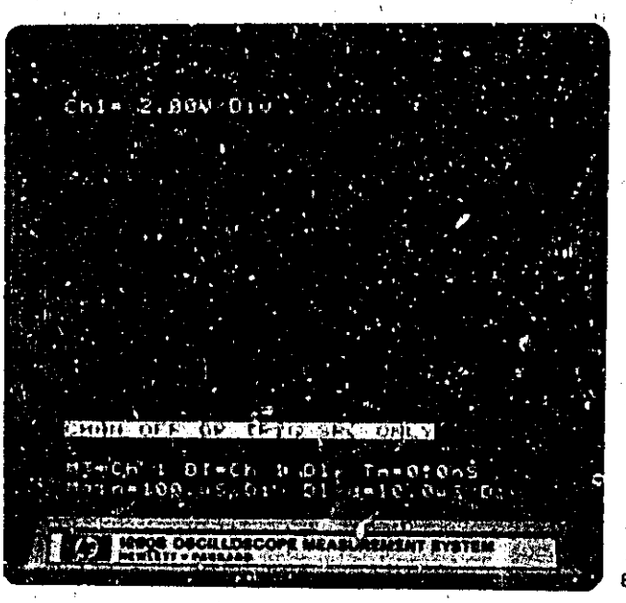
required in bus data transfers are not listed. General requirements for communicating with the 1980A/B are in paragraph 3-19, Remote operation, Hewlett-Packard Interface Bus.

- HP-IB program codes are listed in ASCII code. Table 3-30 contains conversions to other commonly used codes.
- The notation conventions used to describe HP-IB codes are defined in paragraph 3-56, Notation Conventions and Definitions.

Advisory Messages

Description The instrument generates advisory messages to indicate HP-IB syntax errors, incorrect key entries, and special operating information. The messages are displayed on the CRT in inverse video. They can also be reported via the HP-IB. The advisories can be disabled if desired.

Table 3-7 lists all advisory messages and describes the conditions which cause them. Figure 3-17 contains a typical advisory message display.



80-339

Figure 3-17. Typical Advisory Message Display

Procedure Disable advisory messages with the key sequence:

OPTION (MENU) 2 CHAR (INTEN) CALIBRATE & UTILITIES
4 UTILITIES
4 ADVISORIES OFF

Enable advisory messages with the key sequence:

OPTION (MENU) 2 CHAR (INTEN) CALIBRATE & UTILITIES
4 UTILITIES
3 CHAR (ON-OFF) ADVISORIES ON

HP-IB **Program Codes**

Enable or disable the advisory message display:

AV<state>

state ::= Ø disable advisories
1 enable advisories

Advisory Messages (Cont'd)

Example Disable the advisory message display.

LOCAL (keys)	(show MENU) CALIBRATE & UTILITIES UTILITIES ADVISORIES OFF
REMOTE (codes)	AVØ<CR><LF> identifier — state — EOS

Indication When the advisory display is enabled or disabled from the front-panel, the 1980A/B accepts the key entry and remains in the UTILITIES menu.

Comments At power-on, the advisories are enabled as a default condition.

In remote operation, advisory messages can be programmed to cause a service request. This capability is independent of whether the advisory display is enabled or disabled. For more information, refer to the "Service Request Condition" Detailed Operating Instruction.

The "Instrument Status" Detailed Operating Instruction explains how to read the advisory code via the HP-IB. Table 3-7 includes the HP-IB codes for the advisory messages.

The code for the HP-IB SYNTAX ERROR advisory can not be reported via HP-IB nor can this advisory cause a service request. HP-IB syntax errors are handled separately, refer to the "HP-IB Syntax Errors" Detailed Operating Instruction for more information.

Related Sections
Character Generator
Error Messages
HP-IB Status Advisory
HP-IB Syntax Errors
Instrument Status
Service Request Condition

HP-IB

Advisory Messages (Cont'd)

Table 3-7. Advisory Message Description (Page 1 of 2)

Advisory Message Description	HP-IB Code
OPTION INSTALLED HAS NO MENU — there is no menu display for the option selected. For more information, refer to the operating information supplied with the option.	1
CHANNEL IS OFF — the deflection factor, polarity, or coupling of a vertical channel cannot be changed from the front-panel while the channel is off.	2
DLY'D SWEEP IS OFF — the delayed sweep speed, trigger level, trigger qualifiers, sweep mode, and delay cannot be changed from the front-panel while the delayed sweep is off. Instrument must be in V vs T mode and in intensified, delayed, or dual horizontal mode.	3
DLY'D SWEEP IN AUTO — although the trigger qualifiers for the delayed sweep may be changed while it is in auto-sweep mode, this sweep mode does not require a trigger signal.	4
KEY DISABLED — the key pressed was not accepted, either the function is not allowed or there is no current function assignment.	5
CHARACTER GENERATOR OFF — character intensity cannot be changed when the characters are not displayed.	6
CHAN OFF OR TRIG SRC ONLY — the vertical position cannot be adjusted when the channel is off or only being used as a trigger source.	7
TO CHANGE INT SRC SEL CHAN1 — select the internal trigger source by pressing 1 or 2.	8
SCOPE UNDER REMOTE CONTROL — the instrument is in Remote mode; all keys except ▌, SRQ (LOCAL), and FIND (CLEAR) are disabled.	9
SCOPE NOT IN V VS T MODE — key pressed is enabled only when the instrument is in V vs T mode.	10
HP-IB SYNTAX ERROR — an HP-IB syntax error occurred.	*
SCOPE NOT IN DUAL MODE — dual separation can only be adjusted if the instrument is in dual horizontal mode.	12
CONTROL KNOB IN HOLD — Control Knob is not assigned to any function. Select the desired variable function by pressing the corresponding key.	13

* The HP-IB SYNTAX ERROR advisory is not reported via HP-IB. Refer to Comments section of this instruction.

Advisory Messages (Cont'd)

HP-IB

Table 3-7. Advisory Message Description (Page 2 of 2)

Advisory Message Description	HP-IB Code
SELECT VERT POSN OR DELAY — to enter ΔV or ΔT mode, first press [CH 1 POSITION] (channel 1 or 2) or [DELAY TIME], then press [Δ V/T].	14
SIGNAL NOT FOUND — no signal is detected within the frequency or amplitude range for autoscope.	15
CAL MEMORY PROTECTED — the rear-panel calibration protection switch is set to PROTECTED, calibration is not possible.	16
CAL MEMORY NOT PROTECTED — the rear-panel calibration protection switch is set to NOT PROTECTED. Set it to PROTECTED before using the 1980A/B.	17
ΔT ONLY IN AUTO SW AFTER DLY — ΔT measurements can only be made when delayed sweep is in auto-sweep mode.	18
LONG HOLDOFF BY SLOW MAIN SW — main sweep speed is much slower than delayed; may cause viewing problems.	19
LONG HOLDOFF BY SLOW DLY'D SW — delayed sweep speed is much slower than main; may cause viewing problems.	20
INTEN'D TRACE OFF SCREEN — the delay time is greater than ten times the main sweep speed. The intensified marker is beyond the main sweep window.	21
1/ΔT IN ΔT MODE ONLY — only a ΔT value can be expressed in terms of frequency. Select ΔT mode.	22
PASSED TEST — the Confidence Test, RAM Test, or ROM Checksum found no errors.	24
FAILED TEST — the Confidence Test, RAM Test or ROM Checksum found an error. The instrument should be checked by qualified service personnel.	25

Autoscope

Description Autoscope finds the amplitude and period of signal inputs and displays them on the CRT. For many waveforms, it provides a one keystroke setup of the 1980A/B. Autoscope is optimized for repetitive input waveforms with the following characteristics:

frequency ..... 50 Hz to 100 MHz
amplitude ..... 20 mV to maximum input rating

Autoscope executes the following general procedure:

Preset the conditions listed in table 3-8.

Test signal amplitude at each vertical input. If a signal is found, adjust channel delection factor for approximately 3 divisions of display. If no signals are found, display advisory and end routine.

Turn off channels with no signal input.

Select signal from lowest numbered channel as trigger source for main and delayed sweeps. Set trigger level to ±0.5 divisions.

Determine period of trigger source and set main sweep speed for approximately 2 cycles of display. Set delayed sweep speed to 0.1 of main value.

Display input waveforms and return control to front-panel or HP-IB operator.

With selective autoscope, the operator can define which channels are to be autoranged. In addition, selective autoscope preserves coupling, trigger source, and trigger level selec[illegible]. Table 3-8 describes which functions are preset and which are preserved by selective autoscope.

Procedure To execute autoscope, press [AUTO-SCOPE].

To execute selective autoscope, press [SHIFT] [AUTO-SCOPE].

HP-IB **Program Codes**

Execute autoscope:

AS

Execute selective autoscope:

SA

Autoscope (Cont'd)

Example Execute autoscope.

LOCAL (keys)	AUTO SCOPE
REMOTE (codes)	identifier — AS<CR><LF> — EOS

Indication As the 1980A/B is autoranging deflection factor and sweep speed for each input channel, the signal waveform is visible on the CRT. At completion of autoscope, all input signals greater than 10mV are displayed.

Comments Selective autoscope defaults to full autoscope execution if any of the following conditions are detected:

- 1980A/B not in V vs T mode
- No vertical channels on
- 1 + 2 vertical mode selected

If no input signals are found when autoscope is executed, these additional presets are made:

- Trigger source (main and delayed) = channel 1
- Main sweep speed = 50.0 μsec/div
- Delayed sweep speed = 5.00 μsec/div
- Vertical deflection factor (all channels) = 2.00 V/div

In remote operation, customized autoscope routines (controller driven) can be implemented using the trigger flag. Refer to the "Trigger Flag" Detailed Operating Instruction.

If external delayed trigger source is selected when selective autoscope is executed, the delayed trigger level is preset to the same numeric value as main trigger level. For main values > 12.00, delayed is set to 12.00 (÷10) or 1.200 (÷1). For main values <-12.00, delayed is set to -12.00 (÷10) or -1.200 (÷1).
frequency

Related Sections Reading Values Via HP-IB
Trigger Flag

Autoscope (Cont'd)

Table 3-8. Autoscope and Selective Autoscope Preset Conditions

Instrument Function	After Autoscope	After Selective Autoscope
Advisory Messages	no change	no change
Bandwidth Limit	off	no change
Calibrator Level	1 V p-p	1 V p-p
Control Knob Assignment	main sweep speed	main sweep speed
Character Generator	on	on
Delay	0 sec, coarse	0 sec, coarse
Delta Time	off	off
Delta Volts		
channel 1	off	off
channel 2	off	off
Horizontal Position	0.00 div, coarse	0.00 div, coarse
Horizontal Mode	main	main
HP-IB status advisory	no change	no change
Intensity, Characters	70%, coarse	no change
Intensity, Panel Lamps	90%, coarse	no change
Intensity, Trace	25%, coarse	no change
Scope Mode	V vs T	V vs T
Separation, Dual	-3.0 div	-3.0 div
Soft Key Menus	no change	no change
Sweep Mode, Delayed	auto-sweep	no change
Sweep Mode, Main	auto	no change
Sweep Speed, Delayed	autoranged	autoranged
Sweep Speed, Main	autoranged	autoranged
Text Display	no change	no change
Trigger, Delayed		
source	internal, selected	no change
slope	positive	no change
level, internal	0.5 div	set to main level
level, external (÷10 or ÷1)	0.5 V	refer to comments
coupling	AC	no change
Trigger, Main		
source	internal, selected	no change
slope	positive	no change
level, internal	0.5 div	no change
level, external (÷10 or ÷1)	0.5 V	no change
level, line	0.5 V	no change
coupling	AC	no change
Trigger View	off	no change
Vertical Coupling	AC	no change
Vertical Deflection	autoranged	autoranged
Vertical Mode	selected	no change
Vertical Position	selected	no change

Bandwidth Limit

Description Bandwidth limit changes the roll-off of the vertical signal path. It is used to filtar signals displayed on the vertical axis when the 1980A/B is in either V vs T or 1 vs 2 mode. Bandwidth limit does not affect internal trigger signals.

Vertical Bandwidth Characteristics

limit off ..... −3 dB at 100 MHz
limit on ..... −3 dB at 20 MHz

Procedure To toggle bandwidth limit on or off, press .

Program Codes

Turn bandwidth limit on or off:

BW<state>

state ::= **0** bandwidth limit off
1 bandwidth limit on

Example Turn on bandwidth limit.

LOCAL (keys)	
REMOTE (codes)	BW1<CR><LF> — identifier, state, EOS

Indication When bandwidth limit is on, is lighted.

Related Sections
Scope Mode
Trigger, Delayed Sweep
Trigger, Main Sweep
Vertical Coupling
Vertical Deflection Factor

HP-IB

Calibrator Level

Description A signal at the front-panel calibrator terminal for use when adjusting probe compensation. The calibrator signal is also available through a BNC connector on the rear-panel.

The normal calibrator output waveform is a 1 V p-p, square wave. Signal amplitude can be changed via the HP-IB for calibration checks at other levels.

Calibrator Characteristics

frequency	1.86 kHz square wave
rise time	≤ 5 μsec
amplitude	10 V p-p ±1% 1 V p-p ±1% 200 mV p-p ±1% 100 mV p-p ±1% 20 mV p-p ±2%
source impedence	50Ω

Procedure Calibrator output level can only be changed via the HP-IB.

HP-IB **Program Codes**

Select calibrator output level:

CL <level>

level ::=
1 20 mV p-p
2 100 mV p-p
3 200 mV p-p
4 1 V p-p
5 10 V p-p

Example Set calibrator output to 10 V p-p.

REMOTE (codes)	CL5<CR><LF> identifier — EOS level

Calibrator Level (Cont'd)

Comments The calibrator output amplitude is reset to its default value of 1V p-p by the following:

- Power-on
- Executing autoscope
- Executing preset (HP-IB "IN")
- ROM Checksum
- RAM Test
- Confidence Test

Calibrator level cannot be stored in the Save/Recall registers nor is it changed when an instrument state is recalled.

Related Sections Probe Compensation (paragraph 3-50)

Character Generator

Description The character generator displays the CRT readout, advisory messages, and soft key menus. It can also be programmed via HP-IB for special text displays. This instruction describes the CRT readout, and some general considerations about using the character generator.

Primary vertical and horizontal parameter values and the trigger source selections are displayed by the CRT readout. When the Control Knob is assigned to one of these functions, the function name is displayed in inverse video. Figure 3-18 contains a typical readout display.

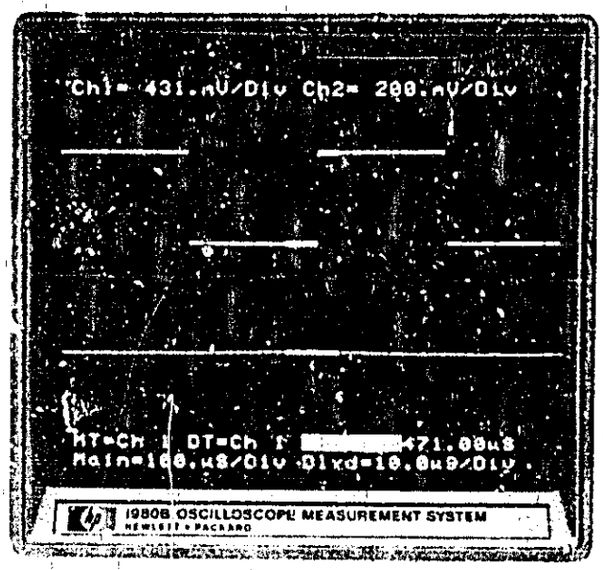


Figure 3-18. The 1980A/B CRT Readout

The character generator writes all characters during the main and delayed sweeps. In other words, characters are multiplexed with the traces. Although this technique provides a high quality character display, at some sweep speeds it may interfere with the trace display. For example, press the key sequence OPTION MENU and change main sweep speed to approximately 6 msec/div with the Control Knob. The "holes" in the traces are caused by the character generator. Press ³ CHAR, and the "holes" disappear.

The following steps can be taken if the character generator interferes with measurements:

- Reduce the number of displayed traces to fewest required for making the measurement.
- Select chop vertical display mode.
- Turn off the character generator, use only the LED readout for parameter value display.

Procedure To toggle the character generator on or off, press ³ CHAR. This key controls all characters displayed except the advisory messages.

Character Generator (Cont'd)

HP-IB **Program Codes**

Toggle the character generator on or off:

SK3

Turn only the CRT readout on or off:

CG <state>

state::= Ø CRT readout off
1 CRT readout on

Example Turn off the CRT readout.

LOCAL (keys)	3 CHAR ON-OFF
REMOTE (codes)	CGØ <CR><LF> identifier — Ø — EOS state

Comments In local or remote operation, if the CRT readout is turned off with 3 CHAR ON-OFF or the HP-IB program code "SK3", the following conditions turn the readout on again:

- Power-on
- Executing autoscope
- Executing selective autoscope
- Calling OPTION MENU

In local or remote operation, if the CRT readout is turned off with the HP-IB program code "CG0", calling OPTION MENU or cycling the LINE switch turns the readout on again.

If the CRT readout is disabled via HP-IB with the program code "CG0", 3 CHAR ON-OFF and the program code "SK3" only toggle the HP-IB text field on or off.

The state of the character generator can be established via the HP-IB by initializing the 1980A/B with the "IN" program code.

Related Sections
Advisory Messages
Control Knob
HP-IB Status Advisory
Initialize
Intensity, Characters and Lamps
Soft Key Menus
Text Display

Control Knob

Description The Control Knob is used to change the value of variable function parameters such as sweep speed, deflection factor, trigger level, and delay. The knob is assigned to a variable function by pressing the corresponding key. As the knob is rotated, the value is immediately changed.

The Control Knob is a stepping control; either coarse or fine step resolution can be selected. In coarse, the speed of knob rotation affects the step size so that changes can be quickly made. Fine provides vernier-like control where step size is set for maximum resolution.

Accidental changes to parameters can be prevented by selecting hold mode. In hold, the knob is not assigned to any variable function.

The Control Knob can also be assigned to variable functions via the HP-IB. In this special case, the knob is enabled for local operation, even if the 1980A/B is in remote mode. This allows the selected function to be adjusted from the front-panel, while all other keys and functions remain in remote.

Procedure To assign the Control Knob to a function, press the corresponding variable function key:

	trace intensity
	panel intensity
	character intensity
(ch 1 or 2)	deflection factor
(ch 1 or 2)	vertical position
(main or dly'd)	sweep speed
(main or dly'd)	trigger level
	horizontal position
	dual separation
	delay (time or digital)
	delay time, numerical

Toggle Control Knob between fine and coarse step resolution by pressing .

To select hold mode, press . Exit hold by assigning the Control Knob to a variable function.

Control Knob (Cont'd)

HP-IB **Program Codes**

Assign the Control Knob and set step resolution:

RC<code>[,<step>]

code::=	**Ø**	hold
	1	channel 1 deflection factor
	2	channel 2 deflection factor
	3	main sweep speed
	4	delayed sweep speed
	5	channel 1 position
	6	channel 2 position
	7	channel 1 position
	8	channel 2 position
	9	dual separation
	1Ø	horizontal position
	11	main trigger level
	12	delayed trigger level
	13	delay
	14	delay
	15	delay
	16	trace intensity
	17	character intensity
	18	panel intensity
step::=	**Ø**	coarse
	1	fine

To assign the Control Knob to delay in the numerical entry mode, first send the program code: **KY7,41** — then send **RC13,Ø** or **RC13,1** to select step resolution. Refer to the "Key" Detailed Operating Instruction for more information about the "KY" command.

The program codes for assigning the Control Knob to ΔT and ΔV are described in the "Delta Time" and "Delta Volts" Detailed Operating Instructions, respectively.

Example Assign Control Knob to channel 1 deflection factor, coarse step resolution.

LOCAL (keys)	[redacted] (ch 2) [redacted]
REMOTE (codes)	**RC7,Ø**<CR><LF> identifier assignment code EOS step resolution

Control Knob (Cont'd)

Indication Control Knob assignment is indicated by lighting the corresponding variable function key. Also, the LED readout displays the parameter value of the function.

The LED readout displays HoLd to indicate hold mode is selected. If the Control Knob is rotated while in hold, the advisory CONTROL KNOB IN HOLD is displayed.

When the Control Knob is assigned to a variable function displayed by the CRT readout, the function name is displayed in inverse video.

FINE lights to indicate that fine is selected.

Comments The Control Knob defaults to hold mode when the 1980A/B makes the remote-to-local transition.

Executing autoscope or selective autoscope assigns the Control Knob to main sweep speed. If the 1980A/B is in remote mode, the Control Knob is enabled as though the program code **RC3,Ø** was sent.

Executing preset (HP-IB "IN") in remote or local mode assigns the Control Knob to trace intensity. If the 1980A/B is in remote mode, the Control Knob is enabled as though the program code **RC16,Ø** was sent.

Control Knob step resolution for a variable function may also be changed by the following:

- Executing autoscope
- Executing selective autoscope
- Executing preset (HP-IB "IN")
- Recalling settings from Save/Recall registers

Related Sections

Delay
Delta Time
Delta Volts
Horizontal Position
Intensity, Character and Lamp
Intensiy, Trace
Reading Values Via HP-IB
Separation, Dual
Sweep Mode, Delayed
Sweep Mode, Main
Sweep Speed, Delayed
Sweep Speed, Main
Trigger, Delayed
Trigger, Main

Delay

Description The delay from the main sweep trigger until the start of the delayed sweep is expressed in terms of time or trigger events, depending upon which delayed sweep mode is in effect. This instruction explains how to set the delay factor for each of the delayed modes.

There are two basic modes for delay time entry from the front-panel of the 1980A/B. Normally the delay time parameter step resolution is determined by the sweep speed of the displayed timebases. This is usually the best mode of entry when making measurements on waveforms displayed on screen because the step resolution is proportioned to the displayed waveform. A second basis for delay time step resolution is provided by numerical entry mode. This mode allows specific delay values to be quickly entered. Table 3-9 describes the step resolutions available for delay time entry.

Delay Characteristics

delay time
- range ..... 0 to 9.999 999 999 9 sec
- resolution
  - front-panel ..... 5 digits, 100 psec minimum (refer to table 3-9)
  - HP-IB ..... 100 psec
- accuracy ..... delay time accuracy depends upon delayed sweep speed value and delay time as described in table 3-10.
- delay jitter ..... 0.002% of delay time

events delay
- range ..... 0 to 99 999 999 events
- resolution ..... 1 event
- maximum rep rate ..... 15 MHz with 50% duty cycle

Table 3-9. Delay Time Step Resolution (front-panel)

Entry Mode	Horizontal Mode	Coarse Step Resolution	Fine Step Resolution
Numerical	all modes	Second most sig. digit	Least sig. digit
Normal	intensified	0.03 × main sweep speed	0.0001 × main sweep speed
Normal	delayed	0.03 × delayed sweep speed	0.0001 × delayed sweep speed
Normal	dual	0.03 × main sweep speed	0.03 × delayed sweep speed

Delay (Cont'd)

*Table 3-10. Delay Time Accuracy**

Delay Value	Delayed Sweep Speed Value	
	5 to 9.99 nsec/div	≥10 nsec/div
<200 μsec	±(2 nsec + 0.1% of reading)	±(2 nsec + 0.1% of reading + 10% of dly'd s/div × 10 div)
≥200 μsec	±(0.05% of reading)	±(0.05% of reading + 1% of dly'd s/div × 10 div)

* Within one hour of a Delay Self Calibration and in constant ambient temperature.

Procedure To enter a delay value, press [key] and rotate the Control Knob.

To enter delay time values using the numerical entry mode, press | [key].

Press [key] to select step resolution for delay time (numerical or normal entry mode), or digital delay entries.

Zero the delay value by pressing | [key].

HP-IB **Program Codes**

Enter delay time value when the delayed sweep is in auto or triggered sweep mode:

DY <value>

value ::= exponential
{+}{d.dd|dd.d|ddd}{d...}{e|E}{-|d}d|+0}
100 psec to 9.999 999 999 9 sec
most significant digit must be ≤9sec

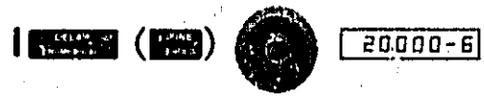
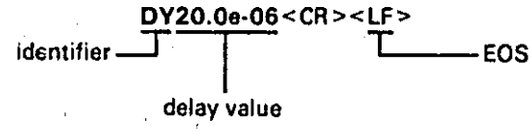
Enter events delay value when delayed sweep is in digital delay mode:

DD <value>

value::= integer
{d...}d
↑7 digits maximum
0 to 99 999 999 events

Delay (Cont'd)

Example Enter delay time value of 20 μsec using numeric entry mode.

LOCAL (keys)	
REMOTE (codes)	

Indication When the Control Knob is assigned to delay, [redacted] is lighted and the delay value is displayed in the LED readout. Delay time values are displayed by the readout as exponential numbers, digital delay values are displayed as integers.

Comments It is a syntax error if a time or events delay value is entered via HP-IB when the delayed sweep is not in the corresponding delay mode. This error, however, is not trapped. Always ensure the proper delay mode is selected before entering delay values. Refer to the "Sweep Mode, Delayed" Detailed Operating Instruction for more information about selecting delayed sweep mode.

If a delay time value is entered via HP-IB when numerical entry mode with coarse step resolution is selected, the 1980A/B only accepts two digits of the delay time value. If a delay time value with more than two digits is entered, the value is truncated to two digits. To avoid this condition, ensure the delay time function is either in normal entry mode or numerical entry mode, fine step resolution.

In triggered or digital delay delayed sweep modes, the setup time of the delayed trigger circuit must be taken into consideration if delayed sweep is to be triggered on the same pulse edge as main. Delayed trigger events cannot be detected until approximately 70 nsec after main trigger.

Related Sections
Control Knob
Delay Time Self-cal (paragraph 3-49)
Delta Time
Sweep Mode, Delayed
Sweep Mode, Main
Trigger Flag

Delta Time

Description ΔT provides a convenient means for making time interval or frequency measurements from the front-panel. It is an extension of the delay time function. ΔT allows a zero time reference to be set anywhere within the delay time range. Then as delay time is incremented or decremented, the 1980A/B displays a direct readout of the time interval between the zero reference and the present delay value.

Delta Time Characteristics

range	(0 – Tzero) sec to (9.999 – Tzero) sec
resolution	
front-panel	5 digits, 100 psec minimum (refer to table 3-9)
HP-IB	100 psec
accuracy	delta time accuracy is the same as delay time, it depends upon delayed sweep speed value and delay time as described in table 3-10.
delay jitter	0.002% of delay time

Procedure To select ΔT mode, press [ΔT] while the Control Knob is assigned to delay time. If numerical entry mode is selected, numerical ΔT mode is selected with [ΔT].

When the Control Knob is assigned to ΔT, the 0.0 nsec reference point is set by pressing [ΔT].

Select Control Knob step resolution with [FINE].

To toggle the ΔT display between units of time and units of frequency, press [1/Δ].

ΔT mode can be turned off by pressing [ΔT] while the Control Knob is assigned to ΔT.

HP-IB **Program Codes**

Turn ΔT mode on or off, set the zero reference point, and assign the Control Knob to ΔT:

DZ <mode>

mode::=	**0**	ΔT off
	1	ΔT on, zeroed, Control Knob assigned

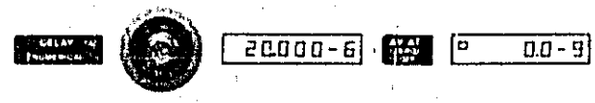
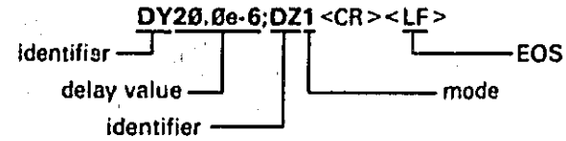
Select Control Knob resolution:

RC13, <step>

step::=	**0**	coarse
	1	fine

Delta Time (Cont'd)

Example Turn on ΔT and set the zero reference point at a delay value of 20 μsec from main sweep trigger.

LOCAL (keys)	
REMOTE (codes)	

Indication When ΔT mode is on, the LED and CRT readouts display the ΔT value instead of delay. The LED readout displays 0.0-9 when ΔT is zeroed.

Comments For specified accuracy, the Delay Time Self-cal should be executed within one hour before ΔT measurements are made.

Although the "DZ" command assigns the Control Knob to ΔT, it does not select numerical or normal entry mode. The last selected delay time entry mode determines the ΔT entry mode.

If sweep speeds, sweep modes, trigger levels, or main trigger conditions are changed (or the corresponding keys pressed), ΔT mode is turned off.

When ΔT is first turned on from the front-panel or via the HP-IB, ΔT is expressed in terms of time.

Related Sections
- Control Knob
- Delay
- Delay Time Self-cal (paragraph 3-49)
- Horizontal Mode
- Reading Values Via HP-IB
- Sweep Mode, Delayed
- Sweep Speed, Delayed
- Sweep Speed, Main
- Trigger Flag

Delta Volts

Description ΔV provides a convenient means of measuring voltage using the Control Knob. ΔV is a special operating mode of the vertical position variable function in which channel deflection factor is multiplied by change in vertical position. A zero vertical reference point can be set anywhere within the vertical position range. Then, as vertical position is incremented or decremented, the 1980A/B displays a direct reading of the voltage interval between the zero reference and the present trace position. ΔV measurements can be made with both channel 1 and 2 in either V vs T or 1 vs 2 scope modes.

Delta Volts Characteristics (Channel 1 or 2)

range	±15 times the channel deflection factor
resolution	0.02 times channel deflection factor
accuracy	±4% for a position change ≤ 10 div

Procedure Select ΔV mode for a given channel and set the zero reference point by pressing [redacted] while the Control Knob is assigned to that channel's vertical position variable function.

While the Control Knob is assigned to channel 1 or 2 ΔV, pressing [redacted] turns off ΔV mode for that channel.

Select step resolution by pressing [redacted].

HP-IB **Program Codes**

Turn on ΔV mode for channel 1 or 2 and assign Control Knob:

DV<channel>,<state>

channel::=	1	channel 1
	2	channel 2
state::=	Ø	ΔV off
	1	ΔV on,zeroed,Control Knob assigned

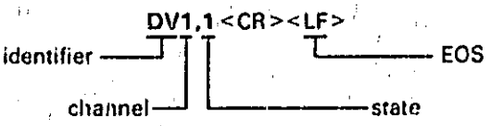
Select Control Knob step resolution:

RC<channel>[,<step>]

channel::=	5	channel 1
	6	channel 2
step::=	Ø	coarse
	1	fine

Delta Volts (Cont'd)

Example Turn on channel 1 ΔV.

LOCAL (keys)	
REMOTE (codes)	

Indication When ΔV is on for a channel, the LED and CRT readouts display the ΔV value instead of deflection factor. The LED readout displays 0.000 -6 when ΔV is zeroed.

Comments If channel deflection factor is changed after ΔV mode is selected, ΔV is turned off.

Related Sections
- Control Knob
- Reading Values Via HP-IB
- Scope Mode
- Vertical Mode
- Vertical Deflection Factor
- Vertical Position

Error Messages

Description If the 1980A/B detects an internal hardware error, an error message is displayed in the LED readout. The error message is primarily meant as a diagnostic aid; it indicates a failure that requires the attention of qualified service personnel. Table 3-11 lists the error conditions that can be detected.

The instrument can be programmed to send the Require Service message when an error condition is detected. The condition can also be read by the system controller, refer to the "Instrument Status" Detailed Operating Instruction. Table 3-11 includes the HP-IB codes for the various error conditions.

Indication When an error is detected, the LED readout displays an error message, such as: Err -34.

Comments If an error occurs during the balance self-cal, RAM test, ROM checksum, or Confidence Test, the error message is displayed briefly in the LED readout. Then the procedure terminates and displays FAILED TEST on the CRT.

If a cal factor or horizontal word output error occurs, the error message is displayed in the LED readout until any key except FIND BEAM is pressed.

The HP-IB code "25" is sent for many of the error conditions. It is the code for the advisory FAILED TEST, which is displayed on the CRT when an error is detected during any of the procedures described in paragraph 3-44, Operator's Checks.

NOTE

A set of Front Panel Calibration Error Codes are generated by the 1980A/B, and displayed on the CRT, when in the Front Panel Calibration Routine. These error codes are not reported to the controller via HP-IB. Refer to Section V of the Service Manual for Front Panel Calibration Error Codes.

Related Sections
- Instrument Status
- Remote Operation (paragraph 3-21)
- Operator's Checks (paragraph 3-44)
- Power-on Sequence and Default Conditions
- Service Request Condition

Error Messages (Cont'd)

Table 3-11. Hardware Error Codes

LED code	HP-IB Code	Error Description
Err -0	25	ROM 0 Failed checksum
Err -2	25	ROM 2 Failed checksum
Err -4	25	ROM 4 Failed checksum
Err -6	25	ROM 6 Failed checksum
Err -8	25	ROM 8 Failed checksum
Err -10	25	ROM 10 Failed checksum
Err -12	25	ROM 12 Failed checksum
Err -14	25	ROM 14 Failed checksum
Err -16	25	ROM 16 Failed checksum
Err -18	25	ROM 18 Failed checksum
Err -20	25	ROM 20 Failed checksum
Err -22	25	ROM 22 Failed checksum
Err -24	25	ROM 24 Failed checksum
Err -26	25	ROM 26 Failed checksum
Err -28	25	ROM 28 Failed checksum
Err -30	25	ROM 30 Failed checksum
Err -31	25	Confidence-test vertical channel error
Err -32	25	Confidence-test horizontal range error
Err -33	25	Confidence-test 10 V signal not found
Err -34	25	Confidence-test 1 V signal not found
Err -35	25	Confidence-test 0.1 V signal not found
Err -36	25	Confidence-test 0.02 V signal not found
Err 40	66	1980A/B cal factor checksum error
Err 51	77	Channel 1 failed autobalance
Err 52	78	Channel 2 failed autobalance
Err -60	25	Scratch RAM (U16) failed
Err -61	25	Nonvolatile RAM (U42, 43) failed
Err -62	25	Character RAM (U32, 33) failed
Err -64	25	Feature RAM (U34, 36) failed
Err -66	25	Save/Recall RAM (U35, 37) failed
Err 72	98	Horizontal Word output failed

Horizontal Mode

Description In V vs T scope mode, four horizontal modes are available. The modes are: Main, main intensified, delayed, and dual. Main displays vertical inputs with respect to the main timebase. Main intensified displays the vertical inputs with respect to the main timebase, and intensifies the portion of the trace that occurs during delayed sweep. Delayed displays the vertical inputs with respect to the delayed timebase. Dual displays both the main intensified and the delayed sweep traces using the selected vertical mode (alternate or chop).

In main mode, only the main timebase is on. The delayed timebase and trigger controls are not enabled.

In main intensified, delayed, and dual modes the main and delayed timebases are on. The main and delayed sweeps are dependent on each other in two ways:

- Delayed sweep cannot begin until main sweep has been triggered.
- Main sweep cannot repeat until delayed sweep is completed.

Unlike traditional scopes, the 1980A/B allows main and delayed sweep speeds to be set independently. Also, the delay until start of delayed sweep is totally independent of the main sweep speed. This allows considerable versatility in waveform measurement and viewing. For example, the first and last events of a block of serial data can be displayed simultaneously at any sweep speed by triggering main at the first event and delaying delayed sweep until the last event.

For more information about using the main and delayed sweeps, refer to the sections listed at the end of this instruction.

Procedure Select horizontal mode with the following keys:


main sweep


main sweep intensified by delayed


delayed sweep


dual sweep

HP-IB **Program codes**

Select horizontal mode:

HM <mode>

mode::= 1 main
2 main intensified
3 delayed
4 dual

Horizontal Mode (Cont'd)

Example Select dual sweep horizontal mode.

LOCAL (keys)	[DUAL]
REMOTE (codes)	HM 4 <CR><LF> identifier — mode — EOS

Indication Horizontal mode is indicated by lighting the corresponding key.

Related Sections

Delay
Delta Time
Scope Mode
Sweep Mode, Delayed
Sweep Mode, Main
Sweep Speed, Delayed
Sweep Speed, Main
Trigger, Delayed
Trigger, Main

Horizontal Position

Description In V vs T mode, the horizontal position of the displayed waveforms can be adjusted for viewing convenience. When horizontal position is zero, the sweeps begin at the leftmost vertical graticule line.

Horizontal Position Characteristics

range	±6.00 div
resolution	0.02 div

Procedure To change horizontal position, press [KNOB] and adjust with Control Knob. Resolution is the same in coarse and fine. In coarse, step size is a function of speed of rotation of the Control Knob.

HP-IB **Program Codes**

Enter horizontal position value:

HP<value>

value::= decimal
[+|-]<SP>]d.d[d]
-6.00 to +6.00 div
value must be multiple of 0.02 div

Example Change horizontal position setting to +2.44.

LOCAL (keys)	[KNOB]  POS 2.44
REMOTE (codes)	HP+2.44<CR><LF> identifier — value — EOS

Indication When Control Knob is assigned to horizontal position, [KNOB] is lighted and the position value is displayed in the LED readout.

Related Sections Control Knob
Reading Values Via HP-IB

HP-IB Address

Description The HP-IB addressing mode and address can be displayed and changed from the front-panel using soft key menus.

Procedure To check the current address or addressing mode, call the HP-IB ADDRESS MODE menu. Press OPTION MENU and HP-IB ADDRESS MODE.

Press CHANGE ADDRESS MODE to step the 1980A/B through the three addressing modes.

When the 1980A/B is set to addressable (ADDRESS: <dd>) mode, the address value can be changed by pressing INCREMENT or DECREMENT.

Press OPTION MENU to return the soft keys to their normal functions.

Example Check the HP-IB addressing mode and address.

LOCAL (keys)	OPTION MENU and HP-IB ADDRESS MODE then exit the menu with OPTION MENU

Indication The following information is displayed in the HP-IB ADDRESS MODE menu to indicate the current addressing mode and address:

ADDRESS: <dd> - indicates instrument is addressable. <dd> is the instrument talk and listen address.

LISTEN ONLY - indicates listen-only mode is selected.

TALK ONLY - indicates talk-only mode is selected.

When listen-only mode is selected, the HP-IB status advisory displays HP-IB: L .

When talk-only mode is selected, the HP-IB status advisory displays HP-IB: T .

Comments Talk-only mode is not supported by the standard 1980A/B.

Calling the HP-IB ADDRESS MODE menu resets all HP-IB parameters, except the address value and addressing mode, to the states described in the "Power-on Sequence and Default Conditions" Detailed Operating Instruction.

Related Sections
HP-IB Status Advisory
Power-on Sequence and Default Conditions
Remote Operation (paragraph 3-21)

HP-IB Status Advisory

Description The HP-IB status advisory displays basic HP-IB status information on the CRT. The advisory indicates when the instrument is in remote mode; is addressed to talk or listen; or if it has issued the Require Service message. If none of these conditions are in effect, the advisory is not displayed. The status advisory can be disabled via the HP-IB.

Table 3-12. Symbols Used in HP-IB Status Advisory

Advisory Symbol	*HP-IB Status Indication*
R	Switched to remote mode
L	Addressed to listen
T	Addressed to talk
S	Issued the Require Service message

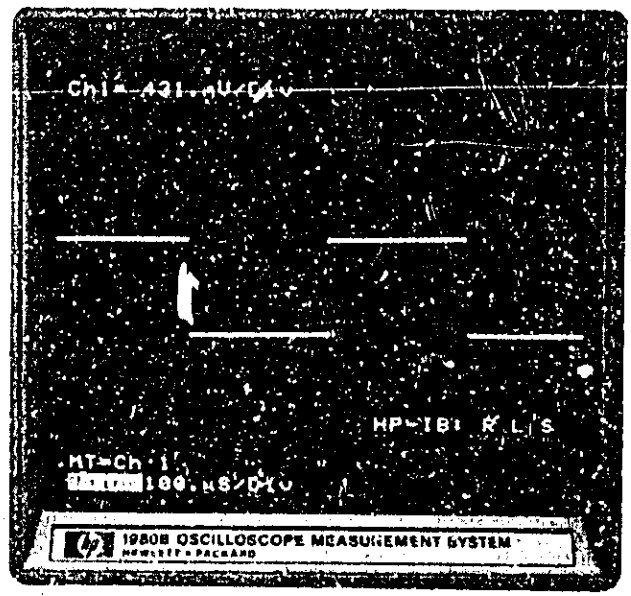


Figure 3-19. The HP-IB Status Advisory

HP-IB **Program Codes**

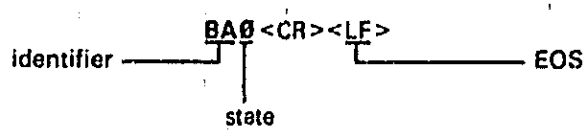
Enable or disable the HP-IB status advisory:

BA<state>

state::= **0** status advisory off
1 status advisory on

HP-IB Status Advisory (Cont'd)

Example Turn off the status advisory.

REMOTE (codes)	

Comments In listen-only or talk-only addressing modes, status advisory is enabled. HP-IB: and HP-IB: T are displayed, respectively.

Related Sections
Character Generator
HP-IB Address
Intensity, Characters and Lamps

HP-IB Syntax Errors

Description When an error in HP-IB message syntax is detected by the 1980A/B, it aborts the execution of the Data message. Program codes up to the error are executed, those following the error are ignored. For more specific information on message execution, refer to Receiving the Data Message, paragraph 3-30.

The instrument can be programmed to issue the Require Service message in response to syntax errors. The type of error can then be determined by reading the error code via the HP-IB. Table 3-13 lists the types of syntax errors the instrument detects, and their corresponding HP-IB codes. The "Service Request Condition" and "Instrument Status" Detailed Operating Instructions explain how to detect errors and read their codes.

Table 3-13. HP-IB Syntax Errors

HP-IB Code	Syntax Error Description
1	Parameter out of range
2	Command not recognized
3	Missing terminator
4	Unexpected character
5	Input buffer overflow
6	Data output not specified

Indication A syntax error causes HP-IB SYNTAX ERROR advisory to be displayed on the CRT if advisories are enabled.

Comments If the 1980A/B is addressed to talk before the output data is specified, it outputs ASCII character "E" to complete the bus transaction. This syntax error does not cause HP-IB SYNTAX ERROR advisory, and does not cause the Require Service message to be sent. However, if the status qualifier for HP-IB syntax is read, the 1980A/B outputs error code 6.

Related Sections
Advisory Messages
Instrument Status
Reading Values Via HP-IB
Remote Operation (paragraph 3-21)
Service Request Condition

Initialize

Description The 1980A/B can be initialized to a defined state using the soft keys or via the HP-IB. Table 3-14 contains a complete description of the initialized state.

Procedure To initialize the instrument, press OPTION MENU, then PRESET.

HP-IB **Program Codes**

Execute initialize:

IN

Example Initialize the 1980A/B.

LOCAL (keys)	OPTION MENU, then PRESET
REMOTE (codes)	identifier — IN<CR><LF> — EOS

Indication The instrument changes to the setup described in table 3-14.

Comments Initializing via the HP-IB turns off soft key menus. Therefore, it provides a known "starting point" for selecting menu functions via HP-IB.

Related Sections Soft Key Menus

Initialize (Cont'd)

Table 3-14. 1980A/B Initialized State

Instrument Function	Initialized State
Advisory Messages	no change
Bandwidth Limit	off
Calibrator Level	1 V p-p
Character Generator	on
Control Knob Assignment	trace intensity
Delay	0.0 nsec, coarse
Delta Time	off
Delta Volts	
channel 1	off
channel 2	off
Horizontal Position	0.00 div, coarse
Horizontal Mode	main-intensified
HP-IB Status Advisory	no change
Intensity, Characters	70%, coarse
Intensity, Lamps	90%, coarse
Intensity, Trace	25%, coarse
Scope Mode	V vs T
Separation, Dual	−3.00 div, coarse
Soft Key Menus	off
Sweep Mode, Delayed	auto-sweep
Sweep Mode, Main	auto-start
Sweep Speed, Delayed	10.0 µsec/div, fine
Sweep Speed, Main	100 µsec/div, coarse
Text Display	off
Trigger, Delayed	
source	channel 1
slope	positive
level, external ÷ 10	1 V, coarse
level, internal	1.00 div, coarse
coupling	AC
Trigger, Main	
source	channel 1
slope	positive
level, external ÷ 10	1 V, coarse
level, internal	1.00 div, coarse
coupling	AC
Trigger View	off
Vertical Coupling	
channel 1	AC
channel 2	AC
Vertical Deflection	
channel 1	2.00 V/div, fine
channel 2	2.00 V/div, fine
Vertical Mode	channel 1 and 2 on, auto-alt/chop selection
Vertical Position	
channel 1	0.00 div, coarse
channel 2	−2.00 div, coarse

Instrument Status

HP-IB

Description The 1980A/B can issue a Require Service message on the HP-IB under one or more operator selectable conditions. Whenever the enabled condition occurs, it sets both the bit corresponding to the condition and the RQS bit (bit 6) in the Status Byte. The bits set in the Status Byte are not cleared unless the LINE switch is cycled.

If more than one enabled condition occurs before the Status Byte is read, the 1980A/B queues them, each in a separate byte, in the order in which they happened. Up to 9 conditions (Status Bytes) can be stacked in this way. The stack must be read, byte by byte, using successive serial polls. Each byte contains an RQS bit so that the instrument will issue and reissue the Require Service message until the entire stack is cleared.

For applications where the RQS interrupt is inconvenient or unnecessary, the Require Service message can be inhibited. In this mode, a single Status Byte register in the 1980A/B traps the occurance of all of the 7 conditions. Although the instrument will not issue the Require Service message, the Status Byte may still be read by serial polling.

Supplemental information about status conditions that occur is contained in the status qualifier registers. These can be read to determine which error occurred, which key was pressed, etc. The qualifier registers can be read without reading the Status Byte message if desired.

Procedure The "Service Request Condition" Detailed Operating Instruction describes how to select the conditions for the Require Service message.

The Status Byte is read via the serial poll sequence described in figures 3-14 and 3-15.

HP-IB **Program Codes**

To read the status qualifiers, select the data to be output by the 1980A/B:

OQ<code>

code ::=
- 1 HP-IB syntax error code
- 2 last key code
- 3 trigger flag state
- 4 advisory or error code
- 5 internal option code
- 6 plug-in option code

Then, address the instrument to talk and read the data.

HP-IB

Instrument Status (Cont'd)

Example Command the 1980A/B to output trigger flag state.

REMOTE (codes)	identifier — OQ3 <CR><LF> — EOS qualifier code

Indication If the RQS mask is 70 and an enabled condition occurs, the HP-IB status advisory displays until the Status Byte message is cleared.

Comments The status qualifier registers contain information pertaining only to the last occurrance of the corresponding condition.

Sending the "OQ" command will clear the selected bit of the status byte if Service Requests are masked off.

Related Sections
- Advisory Messages
- Error Messages
- HP-IB Status Advisory
- HP-IB Syntax Errors
- Key
- Service Request Condition
- Soft Key Menus
- Trigger Flag

Intensity, Characters and Lamps

Description The brightness of the characters displayed on the CRT, and of the panel lamps (including the LED readout) can be adjusted from the front-panel or via the HP-IB. The intensities of both the characters and lamps are expressed as % of full intensity.

Procedure To change the brightness of the character display, press [CHAR INTEN] and adjust with the Control Knob.

To change the brightness of the panel lamps and the LED readout, press [LAMP INTEN] and adjust intensity with the Control Knob.

HP-IB **Program Codes**

Enter character and lamp intensity values:

FP<char>[,<lamp>]

char ::=	integer
	[d]d
	0 to 99
lamp ::=	integer
	[d]d
	0 to 99

Example Set the character intensity to "80" and the lamp intensity to "85".

LOCAL (keys)	[CHAR INTEN] [knob] CHAr 80 [LAMP INTEN] [knob] PNL 85
REMOTE (codes)	FP80, 85<CR><LF> identifier — EOS char intensity — lamp intensity

Comments If character generator is on and character intensity is set to value less than 35 when OPTION MENU is called, the character intensity is preset to level 35.

If the CRT readout is off, the character intensity level can not be changed from the front-panel.

Related Sections Character Generator
Control Knob
HP-IB Status Advisory

Intensity, Trace

Description The intensity level of displayed waveforms can be adjusted over a wide range with the trace intensity variable function. This is necessary because perceived trace intensity (brightness) depends upon ambient lighting, beam writing rate, and beam repetition rate.

As an operating convenience, two values of trace intensity can be entered. One value is used in main, intensified, or dual horizontal modes and in 1 vs 2 and X-Y-Z scope modes. The other value is used only in delayed horizontal mode.

Procedure To change trace intensity, press [INTEN], then adjust Control Knob for desired brightness. The trace intensity used in delayed horizontal mode ([DLY'D]), must be entered while that mode is selected.

HP-IB **Program Codes**

Enter trace intensity values:

CI<main>[,<delayed>]

main ::=	integer	
	[d]d	
	0 to 99	
delayed ::=	integer	
	[d]d	
	0 to 99	

Example Set the main trace intensity to "30" and the delayed trace intensity to "45".

LOCAL (keys)	[INTEN] [knob] 30 [DLY'D] [knob] 45
REMOTE (codes)	CI30,45<CR><LF> identifier — CI main intensity — 30 delayed intensity — 45 EOS — <CR><LF>

Indication When the Control Knob is assigned to trace intensity, [INTEN] is lighted and the LED readout displays the intensity value.

Comments For longest CRT life, use the lowest trace intensity value that provides a viewable waveform.

Related Sections Control Knob
Intensity, Characters and Lamps
Horizontal Mode

Key

HP-IB

Description The remote operator can simulate the pressing of front-panel keys using the key (KY) command. Although almost every function is addressable using the primary command set, the key command can be used as an alternative.

Procedure Send a series of key codes in the same order as keys would be pressed in local operation.

HP-IB **Program Codes**

Enter a key sequence:

KY<code>|,<code>|...
code ::= integer
|d|d
Key codes are listed in tables 3-15 and 3-16.

Example Execute the keystroke sequence [redacted] (ch 1) [redacted].

REMOTE (codes)	KY 6,62,13,7,47<CR><LF> identifier, key codes, EOS

Indication The KY command executes as front-panel keystrokes. The same indications result as in local operation.

Comments Although the KY command is interpreted as a keystroke, it does not affect the "last key code" instrument status qualifier.

If the last key code is read when no key has been pressed since power-on, the code "64" is output by the 1980A/B.

Related Sections
Control Knob
Delta Time
Instrument Status
Service Request Condition
Soft Key Menus

Key (Cont'd)

Table 3-15. Key to Keycode Conversion Table

Display Panel		Control Panel		Voltage Panel			
Key	Code	Key	Code	Key	Code	Key	Code
	49		63		55		21
	50		62		47		14
	51		61		39		22
	52		54		31	(ch 1)	29
	56		•		7	(ch 1)	37
	57			(ch 1)	6	(ch 1)	45
	58			(ch 2)	23	(ch 2)	30
	59			(ch 1)	5	(ch 2)	38
	60			(ch 2)	15	(ch 2)	46
					13		

Time Panel						Probe Keys	
Key	Code	Key	Code	Key	Code	Key	Code
	1		32	(main)	3	Channel 1	65
	9		40	(dly'd)	36	Channel 2	66
	17		16	(main)	35	Main Trigger	67
	25		24	(dly'd)	20	Dly'd Trigger	68
(main)	0		34	(main)	11		
(main)	8		42	(dly'd)	44		
(dly'd)	18		2	(main)	43		
(dly'd)	26		10	(dly'd)	28		
	33		19	(main)	27		
	41		4	(dly'd)	12		

* is not programmable, no code is assigned.

Key (Cont'd)

HP-IB

Table 3-16. Keycode to Key Conversion Table

Code	Key	Code	Key	Code	Key	Code	Key
0	(main)	18	(dly'd)	36	(dly'd)	54	
1		19		37	(ch 1)	55	
2		20	(dly'd)	38	(ch 2)	56	
3	(main)	21		39		57	
4		22		40		58	
5	(ch 1)	23	(ch 2)	41		59	
6	(ch 1)	24		42		60	
7		25		43	(main)	61	
8	(main)	26	(dly'd)	44	(dly'd)	62	
9		27	(main)	45	(ch 1)	63	
10		28	(dly'd)	46	(ch 2)	64	*
11	(main)	29	(ch 1)	47		65	Ch Probe
12	(dly'd)	30	(ch 2)	48	(Not Used)	66	Ch 2 Probe
13		31		49		67	Main Probe
14		32		50		68	Dly'd Probe
15	(ch 2)	33		51		69	(Not Used)
16		34		52			
17		35	(main)	53	(Not Used)		

*Code 64 means no key has been pressed since power-on.

HP-IB

Learn Mode

Description The 1980A/B has learn mode capability which uses the HP-IB controller memory to store instrument configurations. Learn mode provides a fast means of configuring the 1980A/B from an HP-IB controller, and also, a compact format in which instrument setups can be stored.

The learn string contains all of the information that is stored in the Save/Recall registers. In other words, it includes all variable function parameter values, and all state or mode selections.

Procedure The learn string is transferred as binary data between the 1980A/B and the HP-IB system controller.

HP-IB **Program Codes**

Command the 1980A/B to output a learn string:

TE

Then address the 1980A/B to talk. The learn string comprises 80, 8 bit bytes. End-of-String is indicated by setting the EOI bus control line true with the 80th byte.

To configure the 1980A/B using learn mode, send a previously acquired learn string as a Data message:

<80 byte string><CR><LF>

Comments The learn string must be transferred using a technique that does not send the unlisten (UNL) or untalk (UNT) bus commands. If the 1980A/B is unaddressed during Data message transfers, the transfer is aborted.

Related Sections Remote Operation (paragraph 3-21)
Save/Recall

Power-on Sequence and Default Conditions

HP-IB

Description When power is switched on, the 1980A/B performs a series of internal checks. These are transparent to the operator unless an error is found. The following conditions may be encountered at power-on:

Hardware error. If a hardware error is detected, an error message is displayed in the LED readout. Error codes and recommended responses are described in the "Error Messages" Detailed Operating Instruction. Pressing any key except [CLEAR] clears the error display.

CAL factor switch. If the calibration factor protection switch is in the NOT PROTECTED position, the advisory CAL MEMORY NOT PROTECTED is displayed. Put switch in the PROTECTED position or press any key except [CLEAR] to turn off the advisory.

At power-on, the instrument is configured in the state that existed when power was disconnected. However, the following default conditions occur:

- Soft key menus turned off
- Advisory messages enabled
- CRT readout enabled
- DC 50Ω vertical or trigger couplings changed to DC.
- HP-IB switched to local mode
- Local-lockout cleared
- Unaddressed (if in addressable mode)
- RQS mask cleared
- Require Service message cleared
- Status byte register cleared
- HP-IB status advisory enabled

Related Sections Error Messages

Reading Values Via HP-IB

Description All variable function parameter values can be read via the HP-IB. Output Data message format for each parameter is described in table 3-17.

Procedure Send a command to select the desired output data, then address the 1980A/B to talk.

Program Codes

Select parameter value to be output:

OF<code>

code::= **1** channel 1 deflection factor
2 channel 2 deflection factor
3 main sweep speed
4 delayed sweep speed
5 channel 1 ΔV value
6 channel 2 ΔV value
7 channel 1 position
8 channel 2 position
9 dual separation
10 horizontal position
11 main trigger level
12 delayed trigger level
13 delay time
14 ΔT value
15 digital delay

Example Select channel 1 position value as data output.

REMOTE (codes)	identifier — OF7<CR><LF> — EOS function code

Comments The 1980A/B outputs "E" (uppercase) as the delimiter between the mantissa and exponent in exponential values.

Related Sections Control Knob
Instrument Status
Service Request Condition
Trigger Flag

Reading Values Via HP-IB (Cont'd)

HP-IB

Table 3-17. Data Message Output Format

Variable Function	Units	Output Format
channel 1 deflection factor channel 2 deflection factor channel 1 ΔV channel 2 ΔV	V/div V/div Volts Volts	<SP>{+|-} d.ddE {+|-}dd<CR><LF>
main sweep speed delayed sweep speed	sec/div sec/div	<SP>d.ddE {+|-} dd<CR><LF>
channel 1 position channel 2 position horizontal position dual separation	div div div div	<SP> {+|-} dd.dd<CR><LF>
main trigger level delayed trigger level	 div Volts Volts Volts	Format and units depend upon the selected trigger source: LINE, INT: <SP> {+|-} dd.dd<CR><LF> EXT÷1: <SP> {+|-} d.ddd<CR><LF> EXT÷10: <SP> {+|-} dd.dd<CR><LF> EXT÷100: <SP> {+|-} ddd.d<CR><LF>
delay time	sec	<SP>d.d[d...]E-dd<CR><LF> ↑9 digits maximum
ΔT	sec	<SP>[+|-]d.d[d...]E-dd<CR>>LF> ↑9 digits maximum
digital delay	events	<SP>[d....]d<CR><LF> ↑ 7 digits maximum

Save/Recall

Description Eight Save/Recall registers are provided for storing instrument configurations. Instrument state can be saved or recalled from the front-panel or via the HP-IB.

Procedure To save a front-panel configuration, call the SAVE SETTINGS menu with [SAVE]. Then select the storage register by pressing the corresponding soft key.

To recall a front-panel configuration, call the RECALL SETTINGS menu with [RECALL]. Then select the storage register by pressing the corresponding soft key.

To exit either the SAVE SETTINGS or RECALL SETTINGS menu without saving or recalling an instrument state, press [OPTION MENU].

HP-IB **Program Codes**

Save settings with:

SK6,<register>

register ::=	integer	
	d	
	1 to 8	

Recall settings with:

SK7,<register>

register ::=	integer	
	d	
	1 to 8	

Example Save the current front-panel settings in register 8.

LOCAL (keys)	[SAVE] 8 [SELECT] SK
REMOTE (codes)	**SK6, 8**<CR><LF> identifier — SAVE EOS — register 8

Save/Recall (Cont'd)

Comments To quickly load the Save/Recall registers via HP-IB, configure the instrument with a learn string, then save the state in the desired register.

Related Sections Learn Mode

Table 3-17. Functions Stored in Save/Recall Registers

Instrument Function	Paramoters Stored
Advisory Messages	state
Bandwidth Limit	state
Character Generator	state
Control Knob	assignment
Delay	value, step resolution
Delta Time	state, value, step resolution
Delta Volts	state, value, step resolution
Horizontal Position	value, step resolution
Horizontal Mode	state
HP-IB Status Advisory	state
Intensity, Characters	value, step resolution
Intensity, Lamps	value, step resolution
Intensity, Trace	main and delayed value, step resolution
Scope Mode	state
Separation, Dual	value, step resolution
Sweep Mode, Delayed	state
Sweep Mode, Main	state
Sweep Speed, Delayed	value, step resolution
Sweep Speed, Main	value, step resolution
Trigger, Delayed	level value, source, slope, coupling
Trigger, Main	level value, source, slope, coupling
Trigger View	state
Vertical Coupling (ch 1 & 2)	state
Vertical Deflection Factor (ch 1 & 2)	value, step resolution
Vertical Mode	state
Vertical Position (ch 1 & 2)	value, step resolution

Scope Mode

Description The 1980A/B has 3 basic display modes: Volts vs time, channel 1 vs channel 2, and external X-Y-Z. This instruction provides a description of these modes and general advice on their use.

V vs T is the most commonly used scope mode. Channel 1 or 2 signal inputs (Y-axis) are plotted versus timebase signals (X-axis). In V vs T, vertical and horizontal modes can be selected to enable convenient voltage and timing measurements.

1 vs 2 selects an X-Y operating mode. Channel 1 signals are plotted versus channel 2 signals (X-axis). This mode turns on channel 1 and 2, and it enables their controls. The timebases are disabled.

X-Y-Z is a display operating mode using the rear-panel X,Y, and Z-blanking signals. It is designed to accept the output of an HP model 1607A for logic state analysis. This mode disables channels 1 and 2, and the timebases.

Scope Mode Charactersitics

V vs T Mode
- Y-axis
  - bandwidth ..... dc to 100 MHz (limit off)
  - deflection factor ..... 2 mV/div to 10 V/div
- X-axis
  - timebase range ..... 5 nsec/div to 1 sec/div

1 vs 2 Mode
- Y-axis (channel 1)
  - bandwidth ..... dc to 100 MHz (limit off)
  - deflection factor ..... 2 mV/div to 10 V/div
- X-axis (channel 2)
  - bandwidth ..... dc to 4 MHz
  - deflection factor ..... 2 mV/div to 10 V/div
- Phase difference ..... ≤3°, dc to 100 kHz

X-Y-Z Mode
- Y-axis
  - bandwidth ..... dc to ~50 MHz
  - deflection factor ..... 0.4 V/div ±20%
  - maximum input ..... ±10 Vrms
- X-axis
  - bandwidth ..... dc to ~5MHz
  - deflection factor ..... 0.5 V/div ±20%
  - maximum input ..... ±10 Vrms
- Z-axis
  - bandwidth ..... dc to 10 MHz
  - sensitivity ..... +4 V pulse ≥50 nsec wide blanks display
  - maximum input ..... +5 V peak ac + dc

Scope Mode (Cont'd)

Procedure To select the scope mode, press the corresponding key:

	V vs T mode
	1 vs 2 mode
	X·Y·Z mode

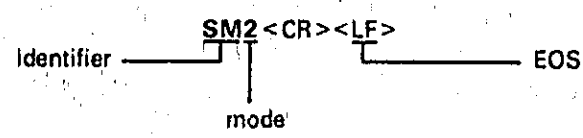
HP-IB **Program Codes**

Select scope mode:

SM<mode>

mode::=	**1**	V vs T
	2	1 vs 2
	3	X·Y·Z

Example Select 1 vs 2 mode.

LOCAL (keys)	
REMOTE (codes)	

Indication The selected scope mode is indicated by the lighted scope mode key.

If the CRT readout is on, scope mode is also indicated by the information that is displayed. In V vs T, both vertical channel and timebase information is displayed. In 1 vs 2 mode, only vertical channel information is displayed. In X·Y·Z mode, there is no CRT readout information displayed.

Comments In 1 vs 2 mode, channel 2 invert is not permitted.

When the instrument is switched from V vs T to 1 vs 2 mode, channel 2 is reset to noninverted display.

Related Sections Horizontal Mode
Vertical Mode

Separation, Dual

Description When the instrument is in dual sweep horizontal mode, the vertical separation of the main and delayed sweep traces may be adjusted to improve viewability.

Dual Separation Characteristics

range	−5.00 div to +5.00 div
resolution	0.02 div

Procedure To change dual separation, press | SEP | and adjust Control Knob for desired value. Separation can only be adjusted when dual horizontal mode is selected.

HP-IB **Program Codes**

Enter separation value:

SP<value>

value ::= decimal
[+|−][d]d.d[d]
−5.00 div to +5.00 div

Example Enter a dual separation value of +4.50 divisions.

LOCAL (keys)	| SEP 4.50
REMOTE (codes)	SP+4.5Ø<CR><LF> (identifier; separation value; EOS)

Indication When the Control Knob is assigned to dual separation, SEP is lighted and separation value is displayed by the LED readout.

Comments If an odd integer (to the nearest hundreth) is entered via the HP-IB, it will be rounded to the nearest even value; positive values are rounded down, negative values are rounded up.

Related Sections Control Knob
Horizontal Mode

Service Request Condition

HP-IB

Description This instruction explains how to set the interrupt mask (RQS mask) for the Require Service message. The related sections listed at the end of this instruction describe the instrument's serial poll capability and the status information that can be obtained.

Procedure The service request condition cannot be set or displayed from the front-panel of the instrument.

HP-IB **Program Codes**

Enter the RQS mask value:

IM<value>

value::=	integer
	ddd
	0≤value≤255
	(refer to table 3-19)

The mask value is the sum of the weights of the conditions that are to be enabled. The value 64 is assigned to the RQS bit, and does not affect the interrupt mask. If it is not added into the total mask value, it will be assumed by the instrument.

The mask value of "0" inhibits the Require Service message, but enables all conditions to be read in a single Status Byte message.

Table 3-19. RQS Mask Value for Service Request Conditions

Condition	Weight
HP-IB Syntax Error	1
Key Closure (except [illegible], [illegible])	2
End of Sweep (after SG command)	4
1980A/B Advisory or Error Message	8
Internal Option request	16
Plug-in Option request	32
[illegible]	128

Example Enable the Require Service message upon closure of [illegible] or detection of HP-IB syntax error.

REMOTE (codes)	IM129<CR><LF> identifier — mask value — EOS

HP-IB

Service Request Condition (Cont'd)

Indication

There is no indication of the mask value being entered. However, when an enabled service request condition occurs, the HP-IB status advisory displays S until the status byte message is read by the controller.

Comments

The interrupt mask is reset to "0" (no conditions enabled) at power-on and when the HP-IB ADDRESS MODE menu is displayed. When the RQS mask value is 0, closure of SRQ LOCAL is handled as both a weight "2" and weight "128" event. That is, SRQ LOCAL sets aboth bit 2 and 8 of the Status Byte time. For all RQS mask values > 0, SRQ LOCAL closures cause the Require Service message only if the RQS mask includes the value "128".

Sending the "IM" instruction clears any pending service requests.

Related Sections

Advisory Messages
Error Messages
Instrument Status
Key
Remote Operation (paragraph 3-21)
Trigger Flag

Soft Key Menus

Description The soft key menus provide many special functions for the remote and local operator by redefining the soft keys. Included in the menu selections are calibration routines, self test routines, and a directory of installed options. In addition, internal enhancement functions are accessed via the soft keys. Table 3-20 summarizes the menu "tree" in the standard 1980A/B (no options installed).

Procedure To call the first level menu (when the menus are off), press OPTION MENU.

Menus define the soft keys with labels displayed on the CRT, such as:



When menus are on, pressing OPTION MENU returns the soft keys to their normal functions.

HP-IB **Program Codes**

To use menu functions via the HP-IB, send a series of soft key codes in the same sequence as in front-panel operation:

SK<code>[,<code>]...

code ::=

Ø	OPTION MENU
1	
2	
3	
4	
5	
6	
7	
8	

Example Execute the balance and delay self-cal routines.

LOCAL (keys)	OPTION MENU, 2 CHAR ENTER: CALIBRATE & UTILITIES 4: BAL & DELAY SELF-CAL
REMOTE (codes)	SKØ,2,3<CR><LF> identifier — EOS menu selection

Soft Key Menus (Cont'd)

Indication When a menu is on or a menu function is executing, [MENU] is lighted.

Comments If character intensity is less than level 35, when the menus are called with [MENU], character intensity is preset to level 35.

Calling the soft key menus turns on the CRT readout. It also erases any text written on screen via HP-IB.

Related Sections
Advisory Messages
Character Generator
Confidence Test (paragraph 3-45)
Delay Time Self-cal (paragraph 3-49)
HP-IB Address
Initialize
Key
Memory Check (paragraph 3-46)
Save/Recall
Vertical Balance Self-cal (paragraph 3-50)

Soft Key Menus (Cont'd)

Table 3-20. Soft Key Menu Tree

level 1:

Soft Key #	
0	menu off
1	
2	
3	
4	
5	HP-IB ADDRESS MODE
6	disabled [1]
7	disabled [2]
8	

level 2:

Soft Key #			
0	menu off	menu off	menu off
1		execute test	disabled [3]
2		execute test	disabled [3]
3		execute test	disabled [3]
4		execute test	disabled [3]
5	disabled [1]	execute test	disabled [3]
6		execute test	disabled [3]
7	disabled [2]	execute test	disabled [3]
8			

	HP-IB ADDRESS MODE (addressable)	HP-IB ADDRESS MODE (listen only)	HP-IB ADDRESS MODE (talk only)
Soft Key #			
0	menu off	menu off	menu off
1	normal function	normal function	normal function
2	normal function	normal function	normal function
3		disabled	disabled
4		disabled	disabled
5	disabled	disabled	disabled
6			
7	disabled	disabled	disabled
8			

level 3:

Soft Key #	
0	menu off
1	normal function
2	normal function
3	
4	
5	
6	
7	
8	

NOTES: [1] reserved for internal enhancement menu
[2] reserved for plug-in enhancement menu
[3] reserved for feature ROM menu

Sweep Mode, Delayed

Description There are three modes of delayed sweep operation: Auto sweep after delay, triggered sweep after delay, and triggered sweep after digital (events) delay.

In auto sweep after delay (auto-sweep) mode, the delay value determines the time interval from the main sweep trigger until the delayed sweep begins. The delay time circuit is calibrated so that delayed sweep can start from 0 to 9.99 sec after the main sweep trigger.

In triggered sweep after delay (triggered) mode, the delay value determines the time interval from the main sweep trigger until the delayed sweep trigger circuit is armed. This mode provides a time-referenced trigger holdoff.

In digital delay mode, the delay value is expressed as trigger events. The delayed sweep begins after the specified number of delayed triggers have ocurred. This mode is useful when examining clocked serial data.

Procedure Select the delayed sweep mode with these keys:

- auto-sweep
- triggered sweep
- digital delay

Both main and delayed sweep can be reset by pressing .

HP-IB **Program Codes**

Select delayed sweep mode:

DM<mode>

mode ::= 1 triggered sweep
2 auto-sweep
3 digital delay

Example Select triggered delayed sweep mode.

LOCAL (keys)	
REMOTE (codes)	DM1<CR><LF> (identifier: DM; mode: 1; EOS: <CR><LF>)

Sweep Mode, Delayed (Cont'd)

Indication The delayed sweep mode is indicated by lighting the corresponding key.

In auto-sweep and triggered-sweep modes, the delay value is expressed in terms of time. The CRT readout displays `Dly Tm =<delay>`.

In digital delay mode, delay is expressed in terms of events and the CRT readout displays `Dig Dly =<delay>`.

The NOT indicator is lighted if main sweep is armed and not triggered.

Comments In digital delay mode, the NOT indicator is disabled.

Related Sections Delay
Sweep Mode, Main
Trigger, Delayed Sweep
Trigger, Main Sweep
Trigger Flag

Sweep Mode, Main

Description There are three basic modes of main sweep operation: Auto-start, triggered, and single. These sweep modes can be selected from the front-panel or via the HP-IB.

In auto-start, the main sweep is triggered by an internal oscillator (~10 Hz) if no trigger signal is present. This mode is convenient since it ensures a trace baseline if delayed sweep is off or in auto-sweep mode.

In triggered mode, main sweep only occurs after it is triggered. Triggered mode is recommended if the trigger repetition rate is less than 10 Hz.

In single mode, main sweep functions as in triggered. However, after one sweep, the sweep circuit must be reset from the front-panel or via HP-IB before the next sweep can occur.

Procedure Select main sweep mode with the following keys:

- auto-start
- triggered
- single

Reset main sweep in any mode by pressing RESET.

HP-IB **Program Codes**

Select main sweep mode:

MM<mode>

mode ::=
- **1** triggered
- **2** auto-start
- **3** single sweep (resets single sweep)

Example Select triggered main sweep mode.

LOCAL (KEYS)	
REMOTE (codes)	MM1<CR><LF> identifier — mode — EOS

Sweep Mode, Main (Cont'd)

Indication The main sweep mode is indicated by lighting the corresponding key.

The NOT indicator is lighted when the main sweep is armed and not triggered.

Related Sections

Delay
Sweep Mode, Delayed
Trigger, Main Sweep
Trigger, Delayed Sweep
Trigger Flag

Sweep Speed, Delayed

Description The sweep speed of the the delayed timebase is adjustable from the front-panel or vie the HP-IB. Delayed sweep speed is independent of main sweep speed, any value within the specified range can be entered.

Delayed Sweep Characteristics

range ..... 5.00 nsec/div to 1 sec/div
resolution ..... 3 digits
accuracy*
5 nsec/div to 9.99 nsec/div ..... ±3%
(center 8 div)
10 nsec/div to 9.99 msec/div ..... ±3%
(first 10 div)
10 msec/div to 1 sec/div ..... ±4%
(first 10 div)

* Within ± 10° C of calibration temperature. For temperature beyond ± 10° C and within 0 to 55°C add 1%, for sweep speeds from 500 msec/div to 1 sec/div add 2%.

Procedure Press [DLY'D] and adjust delayed sweep speed with the Control Knob.

Select fine or coarse step resolution with [STEP]. In coarse, steps are in a 100,150,200,300... 0 sequence. In fine, steps are change of 1 in least significant digit.

HP-IB **Program Codes**

DS<value>

value ::= exponential
[+][n.dd|nd.d|ndd]{E|e}[+|-|<SP>][d]d
5.00e-09 to 1.00e00 sec/div

Examplo Change delayed sweep speed to 10 µsec/div.

LOCAL (keys)	[DLY'D] (dly'd)  10.0 -6
REMOTE (codes)	DS+10.0e-06<CR><LF> identifier — sweep speed value — EOS

Sweep Speed, Delayed (Cont'd)

Indication Delayed sweep speed is displayed by the CRT readout. When the Control Knob is assigned to delayed sweep speed, [DLY SWP] is lighted and the parameter value is displayed by the LED readout. Also, the CRT readout indicates Control Knob assignment by displaying Dlyd = in inverse video.

Comments If delayed sweep speed is much less than main sweep speed, the 1980A/B displays the advisory LONG HOLDOFF BY SLOW DLY SW when [DLY SWP] is pressed and when the delayed sweep speed is changed.

When automatic vertical display mode selection is enabled ([Auto]), delayed sweep speeds less than 1 msec/div cause chop mode to be selected.

Related Sections

Control Knob
Delay
Intensity, Trace
Reading Values Via HP-IB
Sweep Mode, Delayed
Sweep Speed, Main
Vertical Mode

Sweep Speed, Main

Description The sweep speed of the main timebase can be entered from the front-panel or via the HP-IB. Main sweep speed is independent of delayed sweep speed, any value within the specified range can be entered.

Main Sweep Characteristics

range ..... 5.00 nsec/div to 1 sec/div
resolution ..... 3 digits
accuracy*
5 nsec/div to 9.99 nsec/div ..... ±3%
(center 8 div)
10 nsec/div to 9.99 msec/div ..... ±3%
(first 10 div)
10 msec/div to 1 sec/div ..... ±4%
(first 10 div)

* Within ±10°C of calibration temperature. For temperatures beyond ±10°C and within 0 to 55°C add 1%, for sweep speeds from 500 msec/div to 1 sec/div add 2%.

Procedure Press [MAIN DLY] (main) and adjust main sweep speed with the Control Knob.

Select fine or coarse step resolution with [CAL/FINE]. In coarse, steps are in a 100,150,200,300...900 sequence. In fine, steps are change of 1 in least significant digit.

HP-IB **Program Codes**

Enter the main sweep speed value:

MS<value>

value ::= exponential
[+]{n.dd|nd.d|ndd}{E|e}[+|-|<SP>][d]d
5.00e-09 to 1.00e00 sec/div

Sweep Speed, Main (Cont'd)

Example Change main sweep speed to 1 msec/div.

LOCAL (keys)	(main)  100 -3
REMOTE (codes)	MS+1.00e-03<CR><LF> identifier — MS+1.00e-03 — EOS sweep speed value

Indication Main sweep speed is displayed by the CRT readout. When the Control Knob is assigned to main sweep speed, is lighted and the parameter value is displayed by the LED readout. Also, the CRT readout indicates Control Knob assignment by displaying MAIN= in inverse video.

Comments If main sweep speed is much less than delayed sweep speed, the 1980A/B displays the advisory LONG HOLDOFF BY SLOW MAIN SW when is pressed and when the main or delayed sweep speed is changed.

When automatic vertical display mode selection is enabled (), main sweep speeds less than 1 msec/div cause chop mode to be selected.

Related Sections

Control Knob
Delay
Intensity, Trace
Reading Values Via HP-IB
Sweep Mode, Delayed
Sweep Speed, Main
Vertical Mode

HP-IB

Text Display

Description The 1980A/B character generator can be programmed via the HP-IB to write special messages on the CRT. The available display area is shown in figure 3-20.

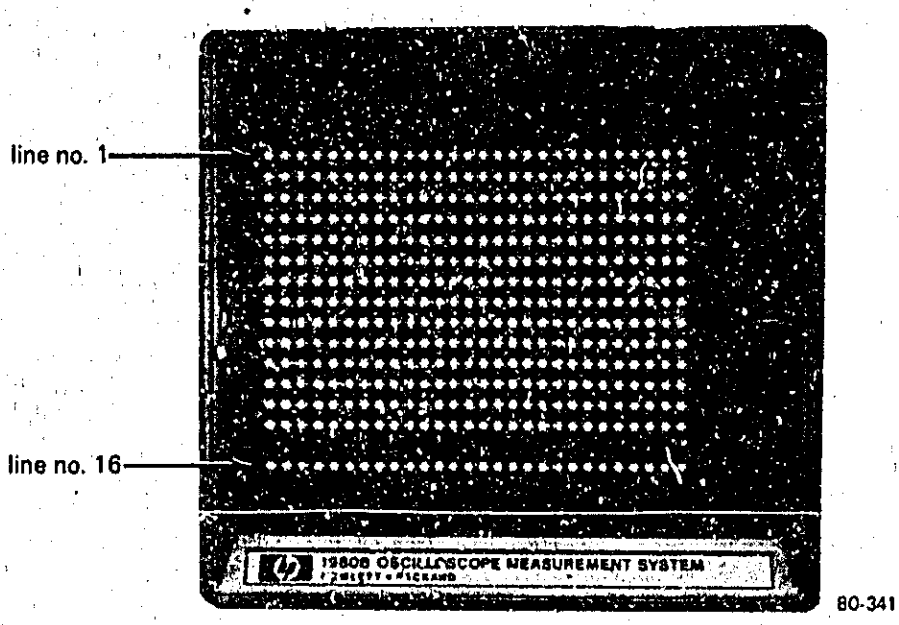


Figure 3-20. Text Field in the 1980A/B CRT Display

Procedure Text cannot be entered from the front-panel, however, the text field can be toggled on or off with [CHAR].

HP-IB **Program Codes**

Erase text field:

TX

Erase text line:

TX<line #>

line #::=	integer	
	dd	
	1-14, 16	

Text Display (Cont'd)

Write text line:

TX<line #>,<string>

line # ::=	integer dd 1-14, 16
string ::=	character string 1 to 28 characters 1980A/B character set, table 3-22

Write text with display attributes:

CH<line #>,<string>

line # ::=	integer dd 1-14, 16
string ::=	7 to 28 bytes, counting characters and attributes String must contain 4 attributes Attributes must be separated by at least one character First byte must be an attribute

Table 3-21. Special Text Attributes

Display Attribute	Octal Code	Decimal Code
normal	200	128
inverse	220	144
blinking	202	130
underline	240	160
blinking and inverse	222	146
inverse and underline	260	176
blinking and underline	242	162
inverse, blinking & underline	262	178

HP-IB

Text Display (Cont'd)

Comments If a soft key menu is called, all text programmed to the display is cleared.

Related Sections
Character Generator
Intensity, Characters and Lamps
Soft Key Menus

Table 3-22. 1980A/B Modified ASCII Character Set

decimal	character	decimal	character	decimal	character	decimal	character
0	¶	32	<SP>	64	@	96	'
1	☺	33	!	65	A	97	a
2	☻	34	"	66	B	98	b
3	♥	35	#	67	C	99	c
4	♦	36	$	68	D	100	d
5	♣	37	%	69	E	101	e
6	♠	38	&	70	F	102	f
7	•	39	'	71	G	103	g
8	◘	40	(	72	H	104	h
9	○	41	)	73	I	105	i
10 *	<LF>	42	*	74	J	106	j
11	♂	43	+	75	K	107	k
12	♀	44	,	76	L	108	l
13 *	<CR>	45	-	77	M	109	m
14	♪	46	.	78	N	110	n
15	☼	47	/	79	O	111	o
16	►	48	0	80	P	112	p
17	◄	49	1	81	Q	113	q
18	↕	50	2	82	R	114	r
19	‼	51	3	83	S	115	s
20	¶	52	4	84	T	116	t
21	§	53	5	85	U	117	u
22	▬	54	6	86	V	118	v
23	↨	55	7	87	W	119	w
24	↑	56	8	88	X	120	x
25	↓	57	9	89	Y	121	y
26	→	58	:	90	Z	122	z
27	←	59 *	;	91	[	123	{
28	∟	60	<	92	\	124	|
29	↔	61	=	93	]	125	}
30	▲	62	>	94	↑	126	~
31	▼	63	?	95	_	127	⌂

* <LF>, <CR>, and ";" are not permitted within text strings.

Trigger, Delayed Sweep

Description The trigger source, level, slope and coupling for delayed sweep may be selected from the front-panel or via the HP-IB.

Delayed Sweep Trigger Characteristics

internal
- sensitivity
  - channel deflection
    - factor < 10 mV/div ..... > 1.4 div, dc to 25 MHz increasing to 3 div at 100 MHz
  - channel deflection
    - factor ≥ 10 mV/div ..... >0.7 div, dc to 25 MHz; increasing to 1.5 div at 100 MHz
  - range ..... −20.00 div to + 20.00 div
  - resolution ..... 0.02 major division
  - accuracy ..... ±(3% of reading +0.4 major div)

external ÷ 10
- sensitivity ..... >500 mV p-p, dc to 25 MHz increasing to 1.2 V p-p at 100 MHz
- range ..... −12.0 V to + 12.0 V
- resolution ..... 20 mV
- accuracy ..... ±(3% of reading +400 mV)

external ÷ 1
- sensitivity ..... >50 mV p-p, dc to 25 MHz increasing to 120 mV p-p at 100 MHz
- range ..... −12.0 V to + 12.0 V
- resolution ..... 2 mV
- accuracy ..... ±(3% of reading +40 mV)

external input
- AC, DC-coupled
  - impedance ..... 1 MΩ ±2% shunted by ~15 pF
  - maximum input ..... refer to figure 3-21
- DC 50Ω coupled
  - impedance ..... 50Ω ±3% shunted by ~15 pF
  - maximum input ..... refer to figure 3-2

HF reject ..... −3 dB at ~35 kHz

LF reject ..... −3 dB at ~35 kHz

Trigger, Delayed Sweep (Cont'd)

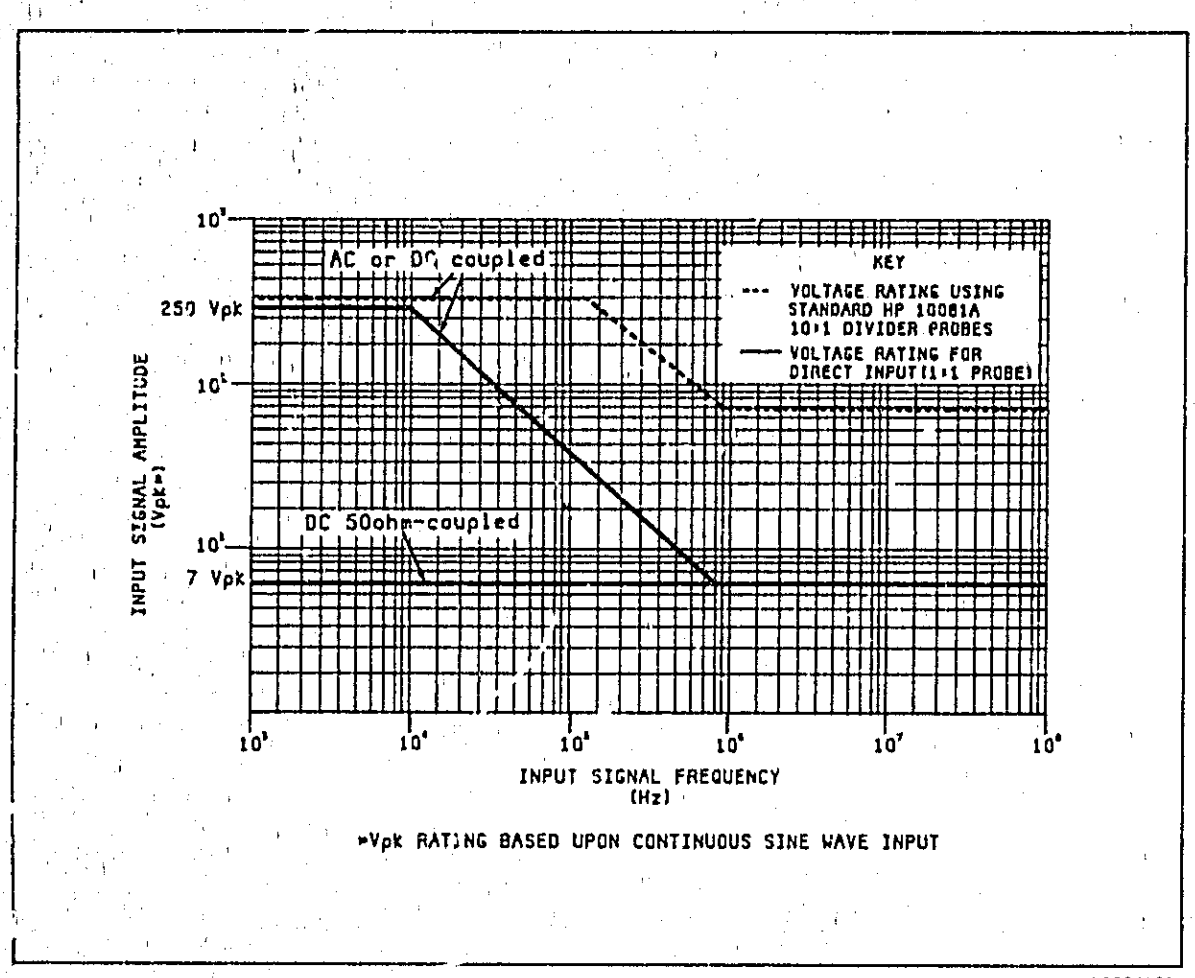


Figure 3-21. Maximum Signal Input vs Frequency ≥1 kHz

Procedure Select delayed trigger source with the following keys.

INT 1	internal, channel 1
INT 2	internal, channel 2
EXT÷10 (dly'd)	external, input ÷ 10
EXT÷1 (dly'd)	external, input ÷ 1

To select the internal or external source coupling, press:

AC (dly'd)	AC coupled
AC LF REJ (dly'd)	AC coupled, LF reject
DC (dly'd)	DC coupled
DC 50Ω (dly'd)	DC coupled, 50Ω (external source only)

Trigger, Delayed Sweep (Cont'd)

Select trigger slope by pressing ∫ \ (dly'd).

To set trigger level, press TRIG LVL (dly'd) and adjust with Control Knob. If main and delayed trigger views are off, delayed trigger view is displayed while the Control Knob is rotated. The trigger threshold is represented by the center horizontal graticule line.

HF reject for internal or external sources can be toggled on or off by pressing ≋ (dly'd).

HP-IB **Program Codes**

Select delayed trigger slope, source and coupling:

DT[<slope>][<source>,<coupling>]

slope ::=	+	low to high transition
	-	high to low transition
source ::=	0	previous source (no change)
	1	vertical channel 1
	2	vertical channel 2
	3	external ÷ 1
	4	external ÷ 10
coupling ::=	0	AC
	1	AC, LF reject
	2	AC, HF reject
	3	AC, LF and HF reject
	4	DC
	5	DC, HF reject
	6	DC 50Ω
	7	DC 50Ω, HF reject

Trigger, Delayed Sweep (Cont'd)

Enter delayed trigger level:

DL<value>

value::= integer
(+|−)dddd
leading zeroes may be omitted

Trigger level value is interpreted according to the selected trigger source:

internal: dd dd
↑assumed decimal point
−20.00 div to +20.00 div

external ÷ 1: d ddd
↑assumed decimal point
−1.200 V to +1.200 V

external ÷ 10: dd dd
↑assumed decimal point
−12.00 V to +12.00 V

external ÷ 100: ddd d
↑assumed decimal point
−120.0 V to +120.0 V

Example Select channel 2 as trigger source, negative slope, DC-coupled with HF reject.

LOCAL (keys)	[illegible]
REMOTE (codes)	DT−2,5<CR><LF> identifier, slope, source, coupling, EOS

Trigger, Delayed Sweep (Cont'd)

Enter delayed trigger level -1.60 div.

LOCAL (keys)	
REMOTE (codes)	DL -160 <CR> <LF> identifier — EOS value

Indication When the Control Knob is assigned to delayed trigger level, (dly'd) is lighted and the trigger source and level value are displayed by the LED readout.

Trigger source is displayed by the CRT readout and the corresponding source selection key is lighted.

Trigger slope and coupling are indicated by lighting the corresponding keys.

Comments At power-on, DC 50Ω coupling is changed to DC as a default condition.

In triggered or digital delay delayed sweep modes, the setup time of the delayed trigger circuit must be taken into consideration if delayed sweep is to be triggered on the same pulse edge as main. Delayed trigger events cannot be detected until approximately 70 nsec after main trigger.

The delayed external trigger input has a probe key contact. If an external trigger source is connected via a recommended HP 10080 series miniprobe, trigger level is displayed as measured at the probe tip (including the probe division ratio).

A probe key closure at the delayed trigger external input causes a momentary shift in delayed trigger level (any source selected) to identify the trigger view signal.

Related Sections

Sweep Mode, Delayed
Sweep Mode, Main
Trigger, Main Sweep
Trigger Flag
Trigger View
Vertical Deflection Factor
Vertical Coupling

Trigger, Main Sweep

Description The source, slope, level, and coupling of the trigger for main sweep can be selected from the front-panel or via the HP-IB.

Main Sweep Trigger Characteristics

internal
- sensitivity
  - channel deflection
    - factor < 10 mV/div ..... > 1.4 div, dc to 25 MHz increasing to 3 div at 100 MHz
  - channel deflection
    - factor ≥ 10 mV/div ..... >0.7 div, dc to 25 MHz; increasing to 1.5 div at 100 MHz
  - range ..... −20.00 div to + 20.00 div
  - resolution ..... 0.02 major division
  - accuracy ..... ±(3% of reading +0.4 major div)

external ÷ 10
- sensitivity ..... > 500 mV p-p, dc to 25 MHz increasing to 1.2 V p-p at 100 MHz
- range ..... −12.0 V to + 12.0 V
- resolution ..... 20 mV
- accuracy ..... ±(3% of reading +400 mV)

external ÷ 1
- sensitivity ..... > 50 mV p-p, dc to 25 MHz increasing to 120 mV p-p at 100 MHz
- range ..... −1.20 V to +1.20 V
- resolution ..... 2 mV
- accuracy ..... ±(3% of reading +40 mV)

line
- range ..... ± 20 relative units
- resolution ..... 0.02 unit

external input
- AC, DC-coupled
  - impedance ..... 1 MΩ ± 2% shunted by ~15 pF
  - maximum input ..... refer to figure 3-22
- DC 50Ω coupled
  - impedance ..... 50Ω ± 3% shunted by ~15 pF
  - maximum input ..... refer to figure 3-22

HF reject ..... −3 dB at ~35 kHz

LF reject ..... −3 dB at ~35 kHz

Trigger, Main Sweep (Cont'd)

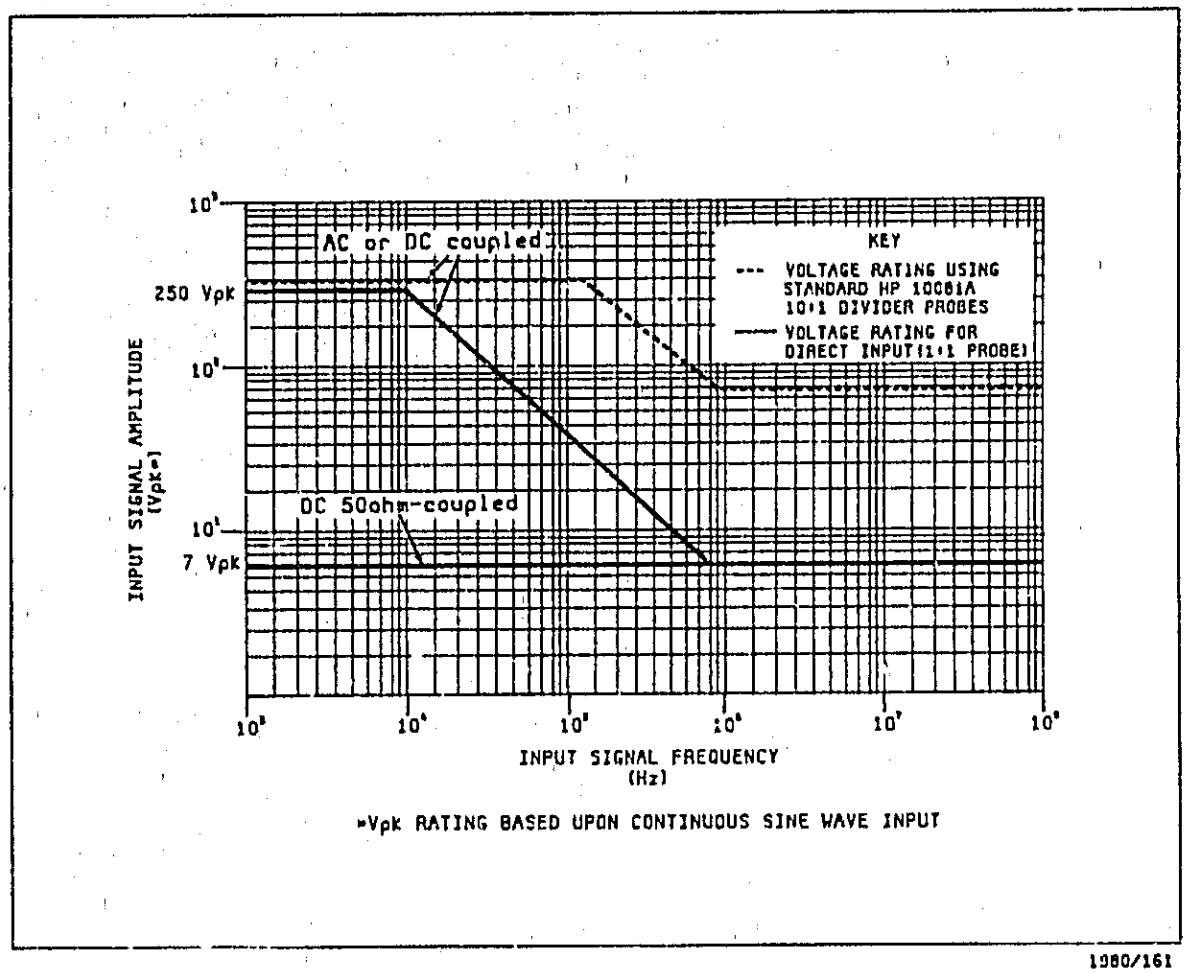


Figure 3-24. Maximum Signal Input vs Frequency ≥1 kHz

Procedure Select main trigger source with the following keys:

	internal, channel 1
	internal, channel 2
(main)	external, input ÷ 10
(main)	external, input ÷ 1
	line

To select the internal or external source coupling, press:

(main)	AC coupled
(main)	AC coupled, LF reject
(main)	DC coupled
(main)	DC coupled, 50Ω

Trigger, Main Sweep (Cont'd)

HF reject for internal or external sources can be toggled on or off by pressing [HF] (main).

Select trigger slope for internal, external or line sources by pressing [Slope] (main).

To set trigger level, press [Level] (main) and adjust with Control Knob. If main and delayed trigger views are off, the main trigger view is displayed while the Control Knob is rotated. The trigger threshold is represented by the center horizontal graticule line.

HP-IB Program Codes

Select main trigger slope, source, and coupling:

MT[<slope>][<source>,<coupling>

slope ::=	+	low to high transition
	-	high to low transition
source ::=	0	previous source (no change)
	1	vertical channel 1
	2	vertical channel 2
	3	external ÷ 1
	4	external ÷ 10
	5	line
coupling ::=	0	AC
	1	AC, LF reject
	2	AC, HF reject
	3	AC, LF and HF reject
	4	DC
	5	DC, HF reject
	6	DC 50Ω
	7	DC 50Ω, HF reject

Enter main trigger level:

ML<value>

value ::=	integer
	[+|-]dddd
	leading zeroes may be omitted

Trigger, Main Sweep (Cont'd)

Trigger level value is interpreted according to the selected trigger source:

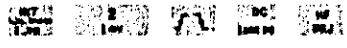
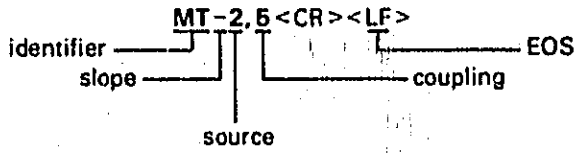
internal or line: dd dd
↑ assumed decimal point
−20.00 div to +20.00 div

external ÷ 1: d ddd
↑ assumed decimal point
−1.200 V to +1.200 V

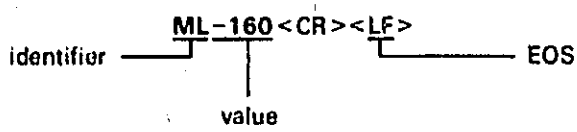
external ÷ 10: dd dd
↑ assumed decimal point
−12.00 V to +12.00 V

external ÷ 100: ddd d
↑ assumed decimal point
−120.0 V to +120.0 V

Example Select channel 2 as trigger source, negative slope, DC-coupled with HF reject.

LOCAL (keys)	
REMOTE (codes)	

Enter main trigger level of −1.60 divisions.

LOCAL (keys)	
REMOTE (codes)	

Trigger, Main Sweep (Cont'd)

Indication When the Control Knob is assigned to main trigger level, [MAIN] (main) is lighted and the trigger source and level value is displayed by the LED readout.

Trigger source is displayed by the CRT readout and the corresponding source selection key is lighted.

Trigger slope and coupling are indicated by lighting the corresponding keys.

Comments At power-on, DC 50Ω coupling is changed to DC as a default condition.

The main external trigger input has a probe key contact. If an external trigger source is connected via a recommended HP 10080 series miniprobe, trigger level is displayed as measured at the probe tip (including the probe division ratio).

A probe key closure at the main trigger external input causes a momentary shift in main trigger level (any source selected) to identify the trigger view signal.

Related Sections
Sweep Mode, Delayed
Sweep Mode, Main
Trigger, Delayed Sweep
Trigger View
Vertical Deflection Factor
Vertical Coupling

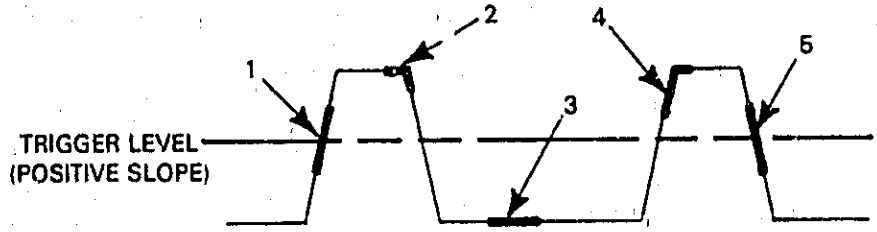
Trigger Flag

Description The trigger flag is a trigger circuit output that can be monitored via the HP-IB. It is used in remote operation to detect trigger events and to make voltage and timing measurements.

Trigger flag detects whether a valid trigger event occurred. Either the main or delayed trigger can be selected to set the flag. There are two basic modes of trigger flag operation, latched and dynamic:

In latched mode, the selected trigger signal must make a transition through the trigger threshold level, with the selected slope, during delayed sweep, to set the flag to "1". Figure 3-23 contains examples of latched mode trigger flag state as delay time is changed.

In dynamic mode, the flag "follows" the trigger signal. With positive trigger slope selected, the flag is "1" while the trigger signal is greater than the trigger level. With negative slope selected, the flag is "1" while the trigger signal is less than the trigger level. Figure 3-24 contains an example of trigger flag state in dynamic mode.



1) FLAG = 1
2) FLAG = 0
3) FLAG = 0
4) FLAG = 0
5) FLAG = 0

Figure 3-23. Latched Mode Trigger Flag State Examples

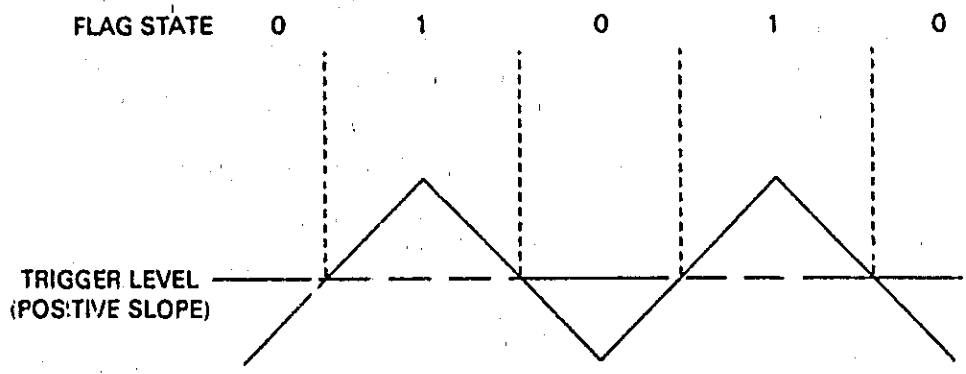


Figure 3-24. Dynamic Mode Trigger Flag State Example

HP-IB

Trigger Flag (Cont'd)

A special horizontal mode must be selected to use the trigger flag. This mode is enabled with the program code "SG". This command puts main sweep in single mode, resets the sweeps and initializes the trigger flag.

The "SG" command does not affect any of the variable function parameters.

The 1980A/B can be programmed to issue the Require Service message at the completion of "SG" enabled sweeps. Also, a timer can be set to cause Require Service after a maximum sweep wait time has expired. The procedure for enabling Require Service after "SG" enabled sweeps or timeout is described in the "Service Request Condition" Detailed Operating Instruction.

Procedure Follow this general procedure when making trigger flag measurements:

Preset horizontal and vertical functions for the measurement procedure.

Set the trigger flag mode and enter the sweep wait time.

Enter RQS mask value for end of sweep if SRQ interrupt is desired.

Start search with "SG" command and wait for end of sweep or timeout interrupt (or test status byte for these conditions).

Test trigger flag state.

HP-IB

Program Codes

Set trigger flag mode:

TF<mode>

mode ::=
- 1 delayed trigger source, latched
- 2 delayed trigger source, dynamic
- 3 main trigger source, latched
- 4 main trigger source, dynamic

Initialize trigger flag and enable sweep:

SG

Trigger Flag (Cont'd)

HP-IB

Enter maximum sweep wait time:

SW<factor 1>,<factor 2>,<factor 3>

factor 1 ::=	integer ddd 0 to 255 units of 23 μsec
factor 2 ::=	integer ddd 0 to 255 units of 5.84 msec
factor 3 ::=	integer ddd 0 to 255 units of 1.5 sec

Example Program the trigger flag to detect a trigger from the delayed trigger source during delayed sweep. Set maximum wait time = 40.6 msec and enable sweep.

REMOTE **(codes)**	**TF1;SW242.6.0;SG**<CR><LF> identifier flag mode identifier EOS enable sweep timeout value

Comments After the program code "SG" is sent to the 1980A/B, it is in a special state that is not indicated on the front panel. After executing a routine using "SG", proper instrument state can be restored by sending the program code "SM1" (selecting V vs T mode).

If the main trigger source-latched mode is selected, the delay value must be set to zero for proper operation. In latched mode, the duration of delayed sweep must be considered. Sweep length is not calibrated and can increase from the nominal 11 divisions to more than 40 divisions at fast sweep speeds.

Related Sections

Delay
Instrument Status
Horizontal Mode
Reading Values Via HP-IB
Service Request Condition
Sweep Mode, Delayed
Sweep Mode, Main
Trigger, Delayed Sweep
Trigger, Main Sweep

Trigger View

Description Trigger view displays the main or delayed trigger signal. This feature is a useful aid when configuring the trigger circuits. It can also be used as a "third channel" to display reference waveforms. However, trigger view should not be used as a measurement channel.

Trigger view has two operating modes. Normally, main or delayed trigger view is displayed only while the trigger level for that sweep is being changed with the Control Knob. If desired, trigger view can also be turned on continuously from the front-panel or via the HP-IB.

Procedure To toggle main trigger view on or off, press [Main Trigger View].

To toggle delayed trigger view on or off, press [Delayed Trigger View].

HP-IB **Program Codes**

Select trigger view mode:

TV<mode>

mode ::=	**0**	view off (momentary display)
	1	main trigger view
	2	delayed trigger view

Example Turn on delayed trigger view.

LOCAL (keys)	[Delayed Trigger View]
REMOTE (codes)	identifier — TV2 <CR><LF> — EOS; mode

Trigger View (Cont'd)

Indicator When main or delayed trigger view is on, the corresponding key is lighted.

Comments Only one trigger view (main or delayed) can be displayed at one time.

Delayed trigger view cannot be displayed when main horizontal mode is selected.

The center horizontal graticule line represents the trigger threshold level with respect to the trigger view waveform.

The timebase in which the trigger view waveform is displayed depends upon the horizontal mode selected (table 3-23).

Table 3-23. Trigger View Display Timebase

Horizontal Mode	Main Trigger View Timebase	Delayed Trigger View Timebase
Main	Main	Not enabled
Intensified	Intensified	Intensified
Delayed	Delayed	Delayed
Dual	Intensified	Delayed

Related Sections
Horizontal Mode
Trigger, Delayed Sweep
Trigger, Main Sweep
Vertical Mode

Vertical Coupling

Description Vertical input coupling can be selected from the front-panel or via the HP-IB. Four input configurations are provided: AC, DC, DC 50Ω, and Ground. The characteristics of each coupling are listed below. Figure 3-25 contains the maximum input voltage derating curve which must be observed for safe operation of the instrument.

Vertical Coupling Characteristics

AC-coupled
- bandwidth ..... ~10 Hz to 100 MHz
- impedance ..... 1 MΩ ±2% shunted by ~16 pF
- input voltage ..... refer to figure 3-25

DC-coupled
- bandwidth ..... dc to 100 MHz
- impedance ..... 1 MΩ ±2% shunted by ~16 pF
- input voltage ..... refer to figure 3-25

DC 50Ω-coupled
- bandwidth ..... dc to 100 MHz
- impedance ..... 50Ω ±3% shunted by 16 pF
- VSWR ..... typically less than 1.3:1
- input voltage ..... 5 V rms maximum

Ground ..... Input connector is disconnected from attenuator, attenuator is grounded through 50Ω.

Procedure Select the vertical coupling for channel 1 or 2 with the following keys:

AC	AC coupled
DC	DC coupled
DC 50Ω	DC 50Ω coupled
GND	Ground (decoupled)

The instrument accepts coupling key entries only if the channel is on or is a trigger source.

Vertical Coupling (Cont'd)

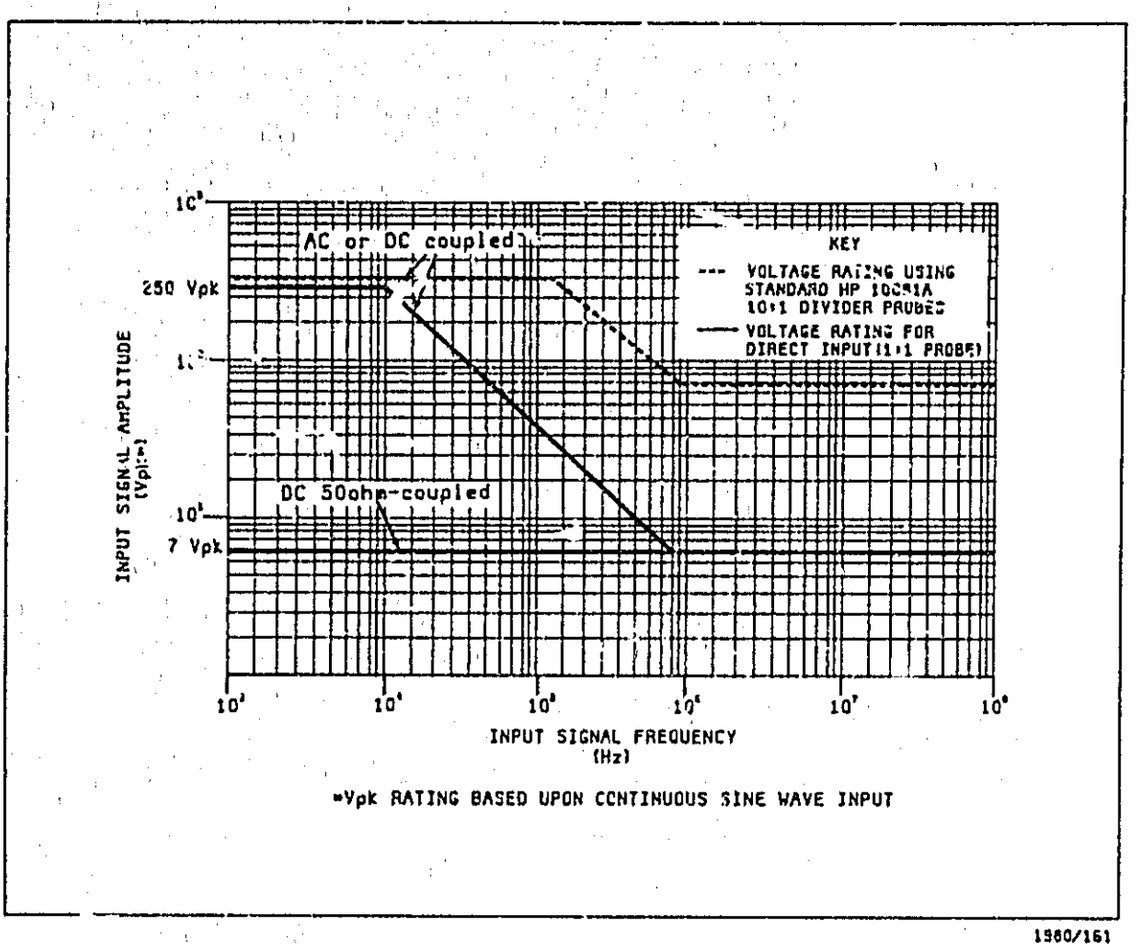


Figure 3-25. Maximum Input Voltage vs Frequency

HP-IB **Program Codes**

Select vertical coupling:

VC<channel>,<coupling>

channel ::=	1	channel 1
	2	channel 2
coupling ::=	0	Ground
	1	AC
	2	DC
	3	DC 50Ω

Vertical Coupling (Cont'd)

Example Select DC coupling for channel 1.

LOCAL (keys)	
REMOTE (codes)	VC1,2<CR><LF> identifier — channel — coupling — EOS

Indication Vertical coupling is indicated by the lighted coupling key.

Comments At power-on, DC 50Ω coupling is changed to DC as a default condition.

Related Sections Trigger, Delayed Sweep
Trigger, Main Sweep
Vertical Position

Vertical Deflection Factor

Description Vertical deflection factor (channel sensitivity) is adjustable from the front-panel or via the HP-IB. Because it is a continuouly calibrated function, waveforms can be accurately scaled for vertical axis measurement or reference.

Deflection Factor Characteristics

range ..... 2.00 mV/div to 10.0 V/div
resolution ..... 3 digits
accuracy ..... ±3%

Procedure Press VOLTS/DIV (channel 1 or 2) and change deflection factor with the Control Knob. Use FINE (ON) to select step resolution.

To toggle between inverted and noninverted display, press 1 or 2.

HP-IB **Program Codes**

Enter channel 1 or 2 sensitivity:

VS<channel>,[<polarity>]<setting>

channel ::= 1 vertical channel 1
2 vertical channel 2

polarity ::= + non-inverted display
- inverted display

value ::= exponential
{n.dd|nd.d|ndd}{e|E}{+|-|<SP>}{d|d
2.00e-03 to 1.00e+01 V/div

Example Change channel 1 deflection factor to −100 mV/div.

LOCAL (keys)	1 VOLTS/DIV -100 -3
REMOTE (codes)	VS1,-100e-3<CR><LF> identifier, channel, polarity, value, EOS

Vertical Deflection Factor (Cont'd)

Indication Deflection factor of enabled channels is displayed in the CRT readout.

When the Control Knob is assigned to channel deflection factor, the LED readout displays the parameter value and the corresponding key (channel 1 or 2 [volts/div]) is lighted. Also, the channel name is displayed by the CRT readout in inverse video.

Comments When a recommended HP 10080 series miniprobe with division ratio readout is connected, channel deflection factor is entered and displayed as the total deflection factor at the probe tip.

Vertical deflection factor can only be changed if the channel is on or is a trigger source.

Related Sections
Delta Volts
Trigger, Delayed S p
Trigger, Main Sweep
Vertical Mode
Vertical Position

Vertical Mode

Description In V vs T mode, the 1980A/B can display channel 1, channel 2, or both channels 1 and 2. Also, the algebraic sum of channels 1 and 2 can be displayed.

Multiple waveforms are displayed using alternate or chop display mode. In alternate, traces are displayed on alternate sweeps. Chop mode displays all traces during each sweep by switching between vertical (and horizontal) signal sources at a 400 kHz rate. The display is blanked during switching time. When automatic selection is enabled, multiple traces are displayed in alternate for sweep speeds slower than 1 msec/div and in chop for sweep speeds faster than 1 msec/div.

1+2 mode allows a composite waveform to be viewed. It provides a differential mode of operation when channel 1 or 2 is inverted.

Differential Mode Characteristics

bandwidth	dc to 20 MHz
CMR	20 dB with common mode signal amplitude equivalent to 10 div and one channel adjusted for optimum rejection

Procedure Press  to toggle channel 1 on or off.

Press  to toggle channel 2 on or off.

Press  to display the algebriac sum of channel 1 and 2. To return to normal channel display, press or  .

To select alternate or chop vertical display mode, press or respectively.

Press  for automatic alternate/chop selection.

HP-IB **Program Codes**

Select vertical mode:

VM<mode>

mode ::=	**0**	channels 1 and 2 off
	1	channel 1 only
	2	channel 2 only
	3	channel 1 + channel 2
	4	channels 1 and 2 on

Vertical Mode (Cont'd)

Select mode of display:

AC<mode>

mode ::= 1 alternate sweep
2 chop sweep
3 automatic selection

Example Select chop sweep vertical display mode.

LOCAL (keys)	CHOP
REMOTE (codes)	AC2<CR><LF> (identifier, mode, EOS)

Display channel 1 + channel 2.

LOCAL (keys)	1+2 DUAL
REMOTE (codes)	VM3<CR><LF> (identifier, mode, EOS)

Indication Vertical mode and vertical display mode selections are indicated by lighting the corresponding keys. Also, the CRT readout displays the deflection factor of the enabled channels.

Comments If the 1980A/B is in dual horizontal mode, chop mode is not permited for main or delayed sweep speeds greater than 1 μsec/div. The display mode will default to alternate mode (unlighted) when either sweep speed is faster than 1 μsec/div. If sweep speed is changed to 1 μsec/div or slower, the original vertical display mode is restored.

Related Sections Horizontal Mode
Trigger View

Vertical Position

Description The vertical position of channel 1 or 2 is adjustable from the front-panel and via the HP-IB. Trace baseline can be positioned as much as 10 divisions off screen.

Vertical Position Characteristics

position range	−15.00 to +15.00 div
resolution	0.02 major division
accuracy	±(2% of reading + 0.3 major division)

Procedure To adjust the vertical position of channel 1 or 2, press [channel 1 or 2], then adjust the Control Knob for desired setting.

HP-IB **Program Codes**

Set channel 1 or 2 vertical position:

VP<channel>,<value>

channel ::= 1 channel 1
2 channel 2

value ::= decimal
[+|−|<SP>][d][d.d[d]]
−15.00 to +15.00 divisions

Example Change channel 1 position to +3.5 divisions.

LOCAL (keys)	[channel 1] [5] POS 3.50
REMOTE (codes)	VP1,+3.5<CR><LF> identifier — channel; position value; EOS

Vertical Position (Cont'd)

Indication When the Control Knob is assigned to vertical position, [redacted] is lighted and the LED readout displays the parameter value.

Comments The vertical position of a channel cannot be changed if the channel is off or only used as a trigger source.

If an odd integer (to the nearest hundredth) is entered via the HP-IB, it will be rounded to the nearest even value; positive values are rounded down, negative values are rounded up.

A probe key closure at channel 1 or 2 causes a momentary shift in the vertical position of that channel's trace for trace identification.

Related Sections Delta Volts
Vertical Mode

3-55. HP-IB CODES AND FORMAT SUMMARY

HP-IB

HP-IB Capability:
As described in IEEE Std 488, and ANSI Std MC1.1, the instrument's complete capability is: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP0, DC0, DT1, C0, E2.

HP-IB Status Advisory:
The following instrument states are indicated on the CRT in the HP-IB status advisory:

R - Switched to remote mode
L - Addressed to listen
T - Addressed to talk
S - Sent the Require Service message

Address:
Set or displayed by calling the HP-IB ADDRESS MODE menu.

The address is preset at the factory to 7 decimal; 00111 binary.

General Input Data Message Format:

<program code>|;<program code>|...|;||<CR>|<LF>

format rules: The 1980A/B sends and receives Data messages in standard ASCII code.

<LF> is used as the End-of-String (EOS) message for all input Data messages.

If several program codes are sent in a Data message, all but the last must be delimited by a semicolon (;).

Program codes consist of a two character identifier (prefix) and a parameter field containing zero, one or several parameters.

Unsigned parameters are interpreted as positive values.

In integer parameters, leading zeroes may be omitted.

Multiple parameters within a program code are delimited by a comma (,).

The character "E" or "e" is used to delimit the mantissa of exponential parameters.

Exponential parameters may be entered in scientific or engineering notation.

In Data messages, spaces (<SP>) are permitted only following program code identifiers and parameter delimiters.

The maximum Data message length is 127 characters including: <CR>, <LF>, <SP>, comma and semicolon.

HP-IB The instrument cannot be unaddressed during input or output Data message transfers. If the instrument is unaddressed and then readdressed, the data transfer is aborted and a syntax error is reported.

All valid program codes for the Measurement System are listed in table 3-26. Specific format requirements and parameter descriptions are included.

General Output Data Message Format:

<SP><function value><CR><LF>

During Learn String outputs, the instrument sets the EOI bus control line true with the last character of the string to indicate end of string. All other output Data messages use <LF> for the EOS message.

Table 3-26 includes specific descriptions of output Data message format. Refer to the functions " 'EADING VALUES" and listed in table 3-26.

Return to Local:
Press [LOCAL] -if not in Local Lockout mode.

Default Conditions:
Several HP-IB parameters are reset at power-on and when the HP-IB ADDRESS MODE menu is selected. The instrument address and addressing mode, however, are preserved. The parameter default conditions are:

- HP-IB local mode
- Local-lockout cleared
- Unaddressed
- RQS mask cleared (mask=0)
- SRQ message cleared
- Status byte (register) cleared
- HP-IB status advisory enabled

Status Byte:
When no conditions are enabled to cause SRQ (mask value=0), a single status byte is available that indicates which conditions have occurred since the byte was reset.

When one or more of the conditions are enabled to cause the SRQ message (mask value>0), as many as 9 separate occurrences can be queued in a status byte register stack. The stack is read on a first-in, first-out basis by serial polling the instrument until bit 7 (the RQS bit) goes false. If there are more than nine occurrances before the register stack is read, the stack will contain the codes for the first eight events and for the last condition that occurred.

The status byte (status byte register stack) is cleared when it is read, at power-on and when the HP-IB ADDRESS MODE menu is selected.

HP-IB

Table 3-24. The Status Byte and RQS Mask

Bit	8	7	6	5	4	3	2	1
Mask Weight	128	64	32	16	8	4	2	1
Service Request Condition	SRQ Key	RQS Bit	Plug-in Option Request	Internal Option Request	Advisory or Error	End of Sweep	Key Closure	HP-IB Syntax Error

Notes: 1. To set the RQS bit and SRQ bus control line true, the condition must be enabled in the RQS mask.

2. If no condition is enabled, the 1980A/B can not set the SRQ bus control line nor the RQS bit true. However, bits 1-6 and 8 of the status byte are set to indicate which conditions have occurred.

Table 3-25. Program Code Prefix to Function Cross Reference

Program Code	Function
AC < mode >	Vertical Mode (alt-chop select)
AS	Autoscope
AV < state >	Advisory Messages
BA < state >	HP-IB Status Advisory
BW < state >	Bandwidth Limit
CG < state >	Character Generator
CI < value 1 > [, < value 2 >]	Intensity, Trace
CH < line # > [, < sting >]	Text Display (with attributes)
CL < mode >	Calibrator Level
DD < value >	Delay (digital delay)
DL < value >	Trigger, Delayed Sweep (level)
DM < mode >	Sweep Mode, Delayed
DS < value >	Sweep Speed, Delayed
DT [< slope >] < source >, < coupling >	Trigger, Delayed Sweep
DV < channel > , < state >	Delta Volts
DY < value >	Delay (delay time)
DZ < state >	Delta Time
FP < char > [, < lamps >]	Intensity, Readout
HM < mode >	Horizontal Mode
HP < value >	Horizontal Position
IM < value >	SRQ Condition (RQS mask)
IN	Initialize
KY < code > [, < code >]...	Key
ML < value >	Trigger, Main Sweep (level)
MM < mode >	Sweep Mode, Main
MS < value >	Sweep Speed, Main
MT [< slope >] < source >, < coupling >	Trigger, Main Sweep
OF < code >	Reading Values (output function)
OQ < code >	Instrument Status (output qualifier)
RC < code > [, < step >]	Control Knob
SA	Autoscope (selective)
SG	Trigger Flag (initialize flag)
SK < code > [, < code >]...	Soft Key
SM < mode >	Scope Mode
SP < value >	Separation, Dual
SW < value 1 >, < value 2 >, < value 3 >	Trigger Flag (sweep wait time)
TE	Teach (output learn string)
TF < mode >	Trigger Flag
TV < mode >	Trigger View
TX < line # > [, < string >]	Text Display
VC < channel > , < mode >	Vertical Coupling
VM < mode >	Vertical Mode
VP < channel > , < value >	Vertical Position
VS < channel > [, < polarity >] < value >	Vertical Deflection Factor

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Table 3-26. Program Codes and Format Summary

Function	Program Code
ADVISORY MESSAGES	AV<state>
off	state ::= 0
on	1
AUTOSCOPE	
Execute autoscope:	AS
Execute selective autoscope:	SA
BANDWIDTH LIMIT	BW<state>
off	state ::= 0
on	1
CALIBRATOR LEVEL	CL<level>
0.02 V p-p	level ::= 1
0.1 V p-p	2
0.2 V p-p	3
1 V p-p	4
10 V p-p	5
CHARACTER GENERATOR	CG<state>
readout off	state ::= 0
readout on	1
CONTROL KNOB	RC<entry>[,<mode>]
Assign control knob:	
hold	entry ::= 0
channel 1 deflection	1
channel 2 deflection	2
main sweep speed	3
delayed sweep speed	4
channel 1 position	5
channel 2 position	6
channel 1 position	7
channel 2 position	8
dual separation	9
horizontal position	10
main trigger level	11
delayed trigger level	12
delay	13
delay	14
delay	15
trace intensity	16
character intensity	17
panel intensity	18
Select step resolution:	
coarse steps	mode ::= 0
fine steps	1
DELAY	
Enter delay time: (seconds)	DY<value>
	value ::= exponential [+]d.d[d...][E/e][+/-][d]d up to 9 digits +0.00e-08 to +9.999 999 999 9e+00 sec min step = 100 psec
Enter digital delay: (delayed trigger events)	DD<value>
	value ::= integer[d...]d up to 7 digits 0 to 99 999 999 events
DELTA TIME	DZ<state>
ΔT mode off	state ::= 0
ΔT mode on (and zeroed)	1
DELTA VOLTS	DV<channel>,<mode>
vertical channel 1	channel ::= 1
vertical channel 2	2
ΔV off	mode ::= 0
ΔV on (and zeroed)	1
HORIZONTAL POSITION (divisions)	HP<value>
	value ::= decimal [+/-][d]d.d[d] -8.00 to +8.00 div minimum step = .02 div

Function	Program Code
HORIZONTAL MODE	HM<mode>
main	mode ::= 1
intensified	2
delayed	3
dual	4
HP-IB STATUS ADVISORY	SA<state>
off	state ::= 0
on	1
INITIALIZE	
Execute initialize:	IN
INSTRUMENT STATUS	
Specify data to be read:	OO<code>
HP-IB syntax error code	code ::= 1
last key code	2
trigger flag state	3
advisory or error code	4
internal option code	5
plug-in option code	6
	output format: <SP>ddd<CR><LF>
INTENSITY, READOUT	FP<char>[,<lamp>]
CRT Readout intensity: (% full character brightness)	char ::= integer[1] dd 0 to 99%
Lamp (and LED) intensity: (% full lamp brightness)	lamp ::= integer[1] dd 0 to 99%
INTENSITY, TRACE	CI<value 1>[,<value 2>]
Main intensity level: (% max intensity)	value 1 ::= integer[1] dd 0 to 99%
Delayed intensity level: (% max intensity)	value 2 ::= integer[1] dd 0 to 99%
KEY	KY<code>[,<code>]...
Valid keycodes are listed in table 3-27.	code ::= integer[1] dd
LEARN MODE	
Specify Learn String output:	TE
	output format: 80 eight bit bytes EOS = EOI bus control line true
Configure the 1980A/B using the Learn String:	<80 byte string><CR><LF>
	Note: The Learn String must be transferred without sending UNL or UNT.

READING VALUES			Format #
Select function to be read:	OF<code>		
channel 1 deflection factor	code ::=	1	F1
channel 2 deflection factor		2	F1
main sweep speed		3	F2
delayed sweep speed		4	F2
channel 1 ΔV		5	F1
channel 2 ΔV		6	F1
channel 1 position		7	F3
channel 2 position		8	F3
dual separation		9	F3
horizontal position		10	F3
main trigger level		11	F4
delayed trigger level		12	F4
delay time		13	F5
ΔT		14	F6
digital delay		15	F7

NOTE: [1] In integer parameters, leading zeroes may be omitted.

Table 3-26. Program Codes and Format Summary (Cont'd)

Function	Program Code
READING VALUES (Cont'd)	
	F# Output Format
	F1 <SP>{+|-}d.ddE{+|-}dd<CR><LF>
	F2 <SP>d.ddE{+|-}dd<CR><LF>
	F3 <SP>{+|-}dd.dd<CR><LF>
	F4 depends on trigger source: line, internal: <SP>{+|-}dd.dd<CR><LF> external+1: <SP>{+|-}d.ddd<CR><LF> external+10: <SP>{+|-}dd.dd<CR><LF> external+100: <SP>{+|-}ddd.d<CR><LF>
	F5 <SP>d.d[d...]E – dd<CR><LF> !up to 9 digits
	F6 <SP>{+|-}d.d[d...]E–dd<CR><LF> !up to 9 digits
	F7 <SP>[d...]d<CR><LF> !up to 7 digits
SCOPE MODE V vs T 1 vs 2 external X-Y-Z	SM<mode> mode ::= 1 2 3
SEPARATION, DUAL (divisions)	SP<value> value ::= decimal [+|-][d]d.d[d] –5.00 to +5.00 div
SRQ CONDITION *Mask value is the sum of the weights of the conditions to be enabled:*	IM<value> value ::= integer! ddd
Condition	Weight
HP-IB syntax error	1
Key (except [front panel], [end sweep])	2
End of sweep (after "SG")	4
Advisory or error message	8
Internal option request	16
Plug-in option request	32
[end sweep]	128
SOFT KEY MENUS	SK<code>[,<code>]...
[previous menu]	code ::= 0
[with trigger]	1
[main trigger]	2
[delay trigger]	3
[main time]	4
[delay time]	5
[save setup]	6
[recall setup]	7
[recall cal]	8
SWEEP MODE, DELAYED triggered sweep after delay auto-sweep after delay digital delay	DM<mode> mode ::= 1 2 3

Function	Program Code
SWEEP MODE, MAIN triggered auto-start single sweep reset	MM<mode> mode ::= 1 2 3 5
SWEEP SPEED, DELAYED (seconds/division)	DS<value> value ::= exponential [+]{n.dd|nd.d|ndd}[E|e][+|-][d]d 5.00e-09 to 9.99e+00 sec/div
SWEEP SPEED, MAIN (seconds/division)	MS<value> value ::= exponential [+]{n.dd|nd.d|ndd}[E|e][+|-][d]d 5.00e-09 to 9.99e+00 sec/div
TEXT DISPLAY Erase all text:	TX
Write character string:	TX<line #>[,<string>] line # ::= integer! dd 1-14,16
The 1980A/B modified ASCII character set is listed in table 3-28.	string ::= 1 to 28 characters If no string is entered, the specified line is cleared
Write character string with special display attributes:	CH<line#>[,<string>] line # ::= same as for TX
	string ::= 7 to 28 bytes long, counting attribute bytes and characters. String must contain four attributes. Attributes must be separated by at least one character. First byte must be an attribute.

Display Attribute	Octal	Decimal
normal	200	128
inverse	220	144
blinking	202	130
underline	240	160
blinking and inverse	222	146
inverse and underline	260	176
blinking and underline	242	162
inverse, blinking & underline	262	178

Function	Program Code
TRIGGER, DELAYED Enter delayed trigger level:	DL<value> value ::= integer! [+|-]dddd
The trigger level value is interpreted according to the current trigger source:	
internal trigger (divisions)	dd.dd !assumed decimal pt –20.00 to +20.00 div
external+1 (Volts)	d.ddd !assumed decimal pt –1.200 to +1.200 V
external+10 (Volts)	dd.dd !assumed decimal pt –12.00 to +12.00 V
external+100 (Volts)	ddd.d !assumed decimal pt –120.0 to +120.0 V

Table 3-26. Program Codes and Format Summary (Cont'd)

Function	Program Code
TRIGGER, DELAYED (Cont'd) Set delayed trigger conditions: triggers on positive slope triggers on negative slope	DT[<slope>]<source>,<coupling> slope ::= + –
previous source (no change) vertical channel 1 vertical channel 2 external+1 external+10	source ::= 0 1 2 3 4
AC AC, LF reject AC, HF reject AC, LF and HF reject DC DC, HF reject DC, 50Ω DC 50Ω, HF reject	coupling ::= 0 1 2 3 4 5 6 7
TRIGGER, MAIN Enter main trigger level:	ML<value> value ::= integer! [+|-]dddd
The trigger level value is interpreted according to the current trigger source:	
line & internal trigger (divisions)	dd.dd !assumed decimal pt –20.00 to +20.00 div
external+1 (Volts)	d.ddd !assumed decimal pt –1.200 to +1.200 V
external+10 (Volts)	dd.dd !assumed decimal pt –12.00 to +12.00 V
external+100 (Volts)	ddd.d !assumed decimal pt –120.0 to +120.0 V
Set main trigger conditions: triggers on positive slope triggers on negative slope	MT[<slope>]<source>,<coupling> slope ::= + –
previous source (no change) vertical channel 1 vertical channel 2 external+1 external+10 line	source ::= 0 1 2 3 4 5
AC AC, LF reject AC, HF reject AC, LF and HF reject DC DC, HF reject DC, 50Ω DC 50Ω, HF reject	coupling ::= 0 1 2 3 4 5 6 7
TRIGGER FLAG Set flag mode:	TF<mode> mode ::= 1
delayed trigger, latched delayed trigger, dynamic main trigger, latched main trigger, dynamic	2 3 4

Function	Program Code
TRIGGER FLAG (Cont'd) Initialize flag, enable single sweep:	SG
Set maximum sweep wait time: (expressed as total of three factors of delay)	SW<factor 1>,<factor 2>,<factor 3>
time in units of ~23 µsec	factor 1 ::= integer! ddd 0 to 255
time in units of ~5.84 msec	factor 2 ::= integer! ddd 0 to 255
time in units of ~1.5 sec	factor 3 ::= integer! ddd to 255
TRIGGER VIEW trigger view off main trigger view delayed trigger view	TV<mode> mode ::= 0 1 2
VERTICAL COUPLING channel 1 channel 2	VC<channel>,<coupling> channel ::= 1 2
GND AC DC DC 50Ω	coupling ::= 0 1 2 3
VERTICAL DEFLECTION channel 1 channel 2	VS<channel>,[<polarity>]<value> channel ::= 1 2
non-inverted display inverted display	polarity ::= + –
deflection factor (Volts/division)	value ::= exponential {n.dd|nc.d|ndd}[E|e][+|-][d]d 2.00e-03 to 1.00e+01 V/div
VERTICAL MODE Select input channels: channels 1 and 2 on channel 1 only channel 2 only channel 1 + channel 2 channel 1 and channel 2 on	VM<mode> mode ::= 0 1 2 3 4
Select alternate or chop: alternate sweep chop sweep automatic selection	AC<mode> mode ::= 1 2 3
VERTICAL POSITION channel 1 channel 2	VP<channel>,<value> channel ::= 1 2
position (divisions)	value ::= decimal [+|-][d]d.d[d] –15.00 to +15.00 div

Table 3-27. 1980A/B Keycodes

Code	Key	Code	Key	Code	Key	Code	Key
0	(main)	18	(dly'd)	36	(dly'd)	54	
1		19		37	(ch 1)	55	
2		20	(dly'd)	38	(ch 2)	56	
3	(main)	21		39		57	
4		22		40		58	
5	(ch 1)	23	(ch 2)	41		59	
6	(ch 1)	24		42		60	
7		25		43	(main)	61	
8	(main)	26	(dly'd)	44	(dly'd)	62	
9		27	(main)	45	(ch 1)	63	AUTO-SCOPE
10		28	(dly'd)	46	(ch 2)	64	*
11	(main)	29	(ch 1)	47		65	Ch 1 Probe
12	(dly'd)	30	(ch 2)	48	(Not Used)	66	Ch 2 Probe
13		31		49		67	Main Probe
14		32		50		68	Dly'd Probe
15	(ch 2)	33		51		69	(Not Used)
16		34		52			
17		35	(main)	53	(Not Used)		

*Code 64 means no key has been pressed since power-on.

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Table 3-28. 1980A/B Text Character Set (Modified ASCII)

decimal	char	decimal	char	decimal	char	decimal	char
0		32	<SP>	64	@	96	'
1		33	!	65	A	97	a
2		34	"	66	B	98	b
3		35	#	67	C	99	c
4		36	$	68	D	100	d
5		37	%	69	E	101	e
6		38	&	70	F	102	f
7		39	'	71	G	103	g
8		40	(	72	H	104	h
9		41	)	73	I	105	i
10*	<LF>	42	*	74	J	106	j
11		43	+	75	K	107	k
12		44	,	76	L	108	l
13*	<CR>	45	-	77	M	109	m
14		46	.	78	N	110	n
15		47	/	79	O	111	o
16		48	0	80	P	112	p
17		49	1	81	Q	113	q
18		50	2	82	R	114	r
19		51	3	83	S	115	s
20		52	4	84	T	116	t
21		53	5	85	U	117	u
22		54	6	86	V	118	v
23		55	7	87	W	119	w
24		56	8	88	X	120	x
25		57	9	89	Y	121	y
26		58	:	90	Z	122	z
27		59*	;	91		123	
28		60	<	92		124	
29		61	=	93		125	
30		62	>	94		126	
31		63	?	95		127	

* <LF>, <CR>, and ";" are not permitted within text strings.

Table 3-29. HP-IB Syntax Error Codes

HP-IB Code	Syntax Error Description
1	Parameter out of range
2	Command not recognized
3	Missing terminator
4	Unexpected character
5	Input buffer overflow
6	Data output not specified

3-56. NOTATION CONVENTIONS AND DEFINITIONS

The following conventions are used in this manual in descriptions of remote (HP-IB) operation:

< > Angular brackets enclose descriptive words that are used to symbolize a program code parameter or an HP-IB command.

::= "is defined as". For example, <A> ::= <B> indicates that <A> can be replaced by <B> in any statement containing <A>.

[ ] Square brackets indicate that the enclosed items are optional.

{ } When several items are enclosed by braces, one, and only one, of these elements must be selected.

| "or": Indicates a choice of exactly one element from a list. For example, <A>|<B> indicates <A> or <B> but not both.

. . . An ellipsis (trailing dots) is used to indicate that the preceding element may be repeated one or more times.

The following definitions are used:

d ::= A single ASCII numeric character, 0-9.

n ::= A single ASCII nonzero, numeric character, 1-9.

<LF>::= ASCII linefeed (decimal 10).

<CR>::= ASCII carriage return (decimal 13).

<SP>::= ASCII space (decimal 32).

Table 3-30. Commonly Used Code Conversions

HP-IB		ASCII	Decimal	Binary	Octal	Hexa-decimal	HP-IB		ASCII	Decimal	Binary	Octal	Hexa-decimal
Addressed Command Group (ACG)	GTL	NUL	0	00 000 000	000	00	Talk Address Group (TAG) Note 2	T0	@	64	01 000 000	100	40
		SOH	1	00 000 001	001	01		T1	A	65	01 000 001	101	41
		STX	2	00 000 010	002	02		T2	B	66	01 000 010	102	42
		ETX	3	00 000 011	003	03		T3	C	67	01 000 011	103	43
	SDC	EOT	4	00 000 100	004	04		T4	D	68	01 000 100	104	44
	PPC	ENQ	5	00 000 101	005	05		T5	E	69	01 000 101	105	45
		ACK	6	00 000 110	006	06		T6	F	70	01 000 110	106	46
		BEL	7	00 000 111	007	07		T7	G	71	01 000 111	107	47
	GET	BS	8	00 001 000	010	08		T8	H	72	01 001 000	110	48
	TCT	HT	9	00 001 001	011	09		T9	I	73	01 001 001	111	49
		LF	10	00 001 010	012	0A		T10	J	74	01 001 010	112	4A
		VT	11	00 001 011	013	0B		T11	K	75	01 001 011	113	4B
		FF	12	00 001 100	014	0C		T12	L	76	01 001 100	114	4C
		CR	13	00 001 101	015	0D		T13	M	77	01 001 101	115	4D
		SO	14	00 001 110	016	0E		T14	N	78	01 001 110	116	4E
		SI	15	00 001 111	017	0F		T15	O	79	01 001 111	117	4F
Universal Command Group (UCG)	LLO	DLE	16	00 010 000	020	10		T16	P	80	01 010 000	120	50
		DC1	17	00 010 001	021	11		T17	Q	81	01 010 001	121	51
		DC2	18	00 010 010	022	12		T18	R	82	01 010 010	122	52
		DC3	19	00 010 011	023	13		T19	S	83	01 010 011	123	53
	DCL	DC4	20	00 010 100	024	14		T20	T	84	01 010 100	124	54
	PPU	NAK	21	00 010 101	025	15		T21	U	85	01 010 101	125	55
		SYN	22	00 010 110	026	16		T22	V	86	01 010 110	126	56
		ETB	23	00 010 111	027	17		T23	W	87	01 010 111	127	57
	SPE	CAN	24	00 011 000	030	18		T24	X	88	01 011 000	130	58
	SPD	EM	25	00 011 001	031	19		T25	Y	89	01 011 001	131	59
		SUB	26	00 011 010	032	1A		T26	Z	90	01 011 010	132	5A
		ESC	27	00 011 011	033	1B		T27	[	91	01 011 011	133	5B
		FS	28	00 011 100	034	1C		T28	\	92	01 011 100	134	5C
		GS	29	00 011 101	035	1D		T29	]	93	01 011 101	135	5D
		RS	30	00 011 110	036	1E		T30	^	94	01 011 110	136	5E
		US	31	00 011 111	037	1F		UNT	_	95	01 011 111	137	5F
Listen Address Group (LAG) Note 1	L0	SP	32	00 100 000	040	20	Secondary Command Group (SCG) Note 3	S0	`	96	01 100 000	140	60
	L1	!	33	00 100 001	041	21		S1	a	97	01 100 001	141	61
	L2	"	34	00 100 010	042	22		S2	b	98	01 100 010	142	62
	L3	#	35	00 100 011	043	23		S3	c	99	01 100 011	143	63
	L4	$	36	00 100 100	044	24		S4	d	100	01 100 100	144	64
	L5	%	37	00 100 101	045	25		S5	e	101	01 100 101	145	65
	L6	&	38	00 100 110	046	26		S6	f	102	01 100 110	146	66
	L7	'	39	00 100 111	047	27		S7	g	103	01 100 111	147	67
	L8	(	40	00 101 000	050	28		S8	h	104	01 101 000	150	68
	L9	)	41	00 101 001	051	29		S9	i	105	01 101 001	151	69
	L10	*	42	00 101 010	052	2A		S10	j	106	01 101 010	152	6A
	L11	+	43	00 101 011	053	2B		S11	k	107	01 101 011	153	6B
	L12	,	44	00 101 100	054	2C		S12	l	108	01 101 100	154	6C
	L13	-	45	00 101 101	055	2D		S13	m	109	01 101 101	155	6D
	L14	.	46	00 101 110	056	2E		S14	n	110	01 101 110	156	6E
	L15	/	47	00 101 111	057	2F		S15	o	111	01 101 111	157	6F
	L16	0	48	00 110 000	060	30		S16	p	112	01 110 000	160	70
	L17	1	49	00 110 001	061	31		S17	q	113	01 110 001	161	71
	L18	2	50	00 110 010	062	32		S18	r	114	01 110 010	162	72
	L19	3	51	00 110 011	063	33		S19	s	115	01 110 011	163	73
	L20	4	52	00 110 100	064	34		S20	t	116	01 110 100	164	74
	L21	5	53	00 110 101	065	35		S21	u	117	01 110 101	165	75
	L22	6	54	00 110 110	066	36		S22	v	118	01 110 110	166	76
	L23	7	55	00 110 111	067	37		S23	w	119	01 110 111	167	77
	L24	8	56	00 111 000	070	38		S24	x	120	01 111 000	170	78
	L25	9	57	00 111 001	071	39		S25	y	121	01 111 001	171	79
	L26	:	58	00 111 010	072	3A		S26	z	122	01 111 010	172	7A
	L27	;	59	00 111 011	073	3B		S27	{	123	01 111 011	173	7B
	L28	<	60	00 111 100	074	3C		S28	|	124	01 111 100	174	7C
	L29	=	61	00 111 101	075	3D		S29	}	125	01 111 101	175	7D
	L30	>	62	00 111 110	076	3E		S30	~	126	01 111 110	176	7E
	UNL	?	63	00 111 111	077	3F		S31	DEL	127	01 111 111	177	7F

NOTES: 1. L<n> = MLA assigned to device number <n>.
2. T<n> = MTA assigned to device number <n>.
3. Meaning defined by Primary Command Group code.

APPENDIX I

The information in appendix I is for backdating of operational changes. This manual has been updated to include the most up-to-date operating information available. The following is a brief description of the changes in operation due to changes in firmware. This information is supplied to allow this manual to be used for operating older instruments.

Area	Serial Prefix 2131A and Below	Serial Prefix 2142A and Above
Soft Keys 4, 5, 8 (without 19860A installed)	If pressed, message notes "KEY DISABLED"	If pressed, message notes "OPTION NOT INSTALLED"
Soft Keys 4, 5, 8 (with 19860A installed)	If pressed, message notes "KEY DISABLED"	Soft Key 4 = STORE M1 Soft Key 5 = STORE M2 Soft Key 8 = VIEW OFF (should be accompanied with appropriately labeled display panel)
In Utilities Menu, ADVISORIES ON/OFF	When pressed, exited menu automatically	Does not exit menu automatically
OPTION MENU	SK4 labeled "INSTALLED OPTION LIST"	SK4 labeled "FEATURE ROMS"
SHIFT KEY	Could not toggle off if erroneously selected	Can now toggle off if not wanted
"Automatic" Trigger View when TRG LVL is adjusted	Short viewing period, looked like flicker	Longer viewing period
With no channels selected (all off)	If Rotary Control is moved bright spot may appear	No bright spot
SELECTIVE AUTOSCOPE	Preset the intensity to a fixed level	Preserves intensity level
CONFIDENCE TEST	Required BNC cable or 1:1 probe only	Will now accept 10:1 probe also (of the proper type)
UTILITIES MENU, RAM TEST ROM CHECKSUM	Automatically exited menu when pressed, cannot execute from HP-IB	Does not exit menu, can be executed from HP-IB
Auto sweep start-up with no signal input at turn on	Possible no auto sweep start-up (not due to malfunction of old ROM devices)	Software routine insures auto sweep start without an input at turn on

APPENDIX I (Cont'd)

Area	Serial Prefix 2131A and Below	Serial Prefix 2142A and Above
OPTION MENU	SK5 labeled "19842A HP-IB"	SK5 labeled "HP-IB MODE"
Sweep and Sensitivity	Accepted only 3 mantissa digits	Will accept more than 3 mantissa digits ignoring those after 3
Delay Time (DY)	If input contained digits representing less than 100 ps a syntax error was reported	Digits representing less than 100 ps are truncated and no syntax error reported
Input Mask (IM)	Did not clear pending service requests	Clears all pending service requests
Service Requests Masked Off	SRQ key prassed sets bit 8 and bit 2	Sets only bit 8
Service Requests Masked Off	Reading status byte cleared status byte	Reading status byte does not clear byte (executing OQn will clear bit n. OQ2 will also clear bit 8, SRQ.)
Rotary Control	When changed from one function to another instrument would properly set FINE/COARSE but it would not be apparent to the operator. Therefore operator would attempt to change and confusion resulted.	Now set automatically as it should be. e.g., RC is transferred from MS (coarse) to VOLTS/DIV, FINE is set and FINE light is lit.
ALT/CHOP Selection	If Main or Delayed sweeps were changed from <1 ms to >1 ms (or vice versa) program had to select ALT or CHOP	Proper selection of ALT/CHOP is automatically accomplished, but can be overridden as desired
Device Clear	No device clear	Added. Therefore after set, next poll from 1980 main loop causes HP-IB interface to: 1) abort a Talk or Listen 2) reset the menus 3) clear all pending SRQ's Does not function during CAL or digitize. Clears 1980 only. Plug in, Option or Feature ROMs not affected

SERVICE MANUAL

In order to have a complete eight section Operating and Service Manual this section must be preceeded by a copy of the Operating and Programming Manual.

A complete Table of Contents for the Service Section is included in this section.

For detailed operating instructions, power requirements and safety information refer to the Operating and Programming Manual sections I, II, and III.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION

The procedures in this section test the instrument's electrical performance using specifications of table 1-1 as performance standards. All tests can be performed without access to interior of the instrument. A simpler operational test is included in Section III under Operator's Checks.

4-2. EQUIPMENT REQUIRED.

Equipment required for performance tests is listed in the Recommended Test Equipment Table in Section I and in table 4-1. Any equipment that satisfies critical specifications given in the table may be substituted.

Table 4-1. Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model
Function Generator	range: 10 Hz to 100 kHz squarewave 2 kHz to 50 kHz sinewave level: 0 to 10 Vp-p	HP 3310A
Peak to Peak Source	level: 20 mV to 100 V accuracy: ±0.25%	Ballantine 6125B
Time Mark Generator	range: 5 nsec to 1 sec accuracy: ±0.01%	Ballantine 6125B
Signal Generator	range: 10 MHz to 100 MHz	HP 3200B
Cable Pair	50 ohm BNC male to BNC male, approximately 9 inches long. Pair must be of equal length.	HP 10502A
BNC Tee	1 male, 2 female	HP Part No. 1250-0781
Sampling Voltmeter	bandwidth: 10 MHz to 100 MHz accuracy: ±3%	HP 3406A with HP 11063A Sampling Tee
Pulse Generator	Fast Rise Time	Ballantine 6125B

Table 4-1. Recommended Test Equipment (Cont'd)

Instrument	Critical Specifications	Recommended Model
Adapter (4)	GR874 to female BNC	HP Part No. 1250-0850
Adapter	GR874 to male BNC	HP Part No. 1250-0849
Power Divider	1 - 50 ohm input 2 - 50 ohm outputs	General Radio 874-TPDL
Attenuator	6 dB Attenuator	General Radio GR874-G6
DC Source	± Ø V to 100 V	Ballantine 6125B

4-3. TEST RECORD.

Results of performance tests may be tabulated on the Performance Test Record (table 4-4) at the end of procedures. The Test Record lists all of the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

4-4. CALIBRATION CYCLE

This instrument requires periodic verification of performance. Depending on use and environmental conditions, the instrument should be checked using the following performance tests at least every six months.

4-5. PERFORMANCE TEST PROCEDURES.

Note

Allow instrument to warm up for at least 30 minutes prior to beginning performance tests.

PERFORMANCE TESTS

4-6. Deflection Factor Test.

Specifications:

Ranges: 2 mV/div to 10 V/div

Accuracy: ±3%

Description:

Apply a known peak to peak voltage and check each range for accuracy.

Equipment:

Peak to Peak Source ..... Ballantine 6125B

Procedure:

a. Set peak to peak source output to 20 mV P-P.

b. Apply output of peak to peak source to channel 1 input.

c. Press AUTO-SCOPE.

d. Select channel 1 volts/div and set to 2 mV/div by pressing [CH 1] (channel 1) and rotating the Control Knob for a reading of [2.00 -3] in LED display.

e. Displayed signal should be 10 divisions (limits 9.7 to 10.3 major divisions).

f. Set channel 1 volts/div to 10 mV by rotating the Control Knob for a reading of [10.0 -3] in LED display.

g. Increase peak to peak source output to 100 mV P-P.

h. Displayed signal should be 10 divisions (limits 9.7 to 10.3 major divisions).

i. Set channel 1 volts/div to 100 mV by rotating the Control Knob for a reading of [100. -3] in LED display.

j. Increase peak to peak source output to 1 V P-P.

k. Displayed signal should be 10 divisions (limits 9.7 to 10.3 major divisions).

l. Set channel 1 volts/div to 1 V by rotating the Control Knob for a reading of [1.00] in LED display.

m. Increase peak to peak source output to 10 V P-P.

n. Displayed signal should be 10 divisions (limits 9.7 to 10.3 major divisions).

o. Repeat steps a through n for channel 2.

PERFORMANCE TESTS

4-7. Vertical Position Test.

Specifications:

Range: A baseline can be adjusted ±15 major div from center graticule line (possible 10 div off screen).

Accuracy: ±(2% of reading +0.3 major div)

Description:

Set trace to 15 divisions above center graticule and apply a minus 15 Vdc input to deflect trace to center screen, then set trace to 15 divisions below center graticule and apply a 15 Vdc input to deflect trace to center screen.

Equipment:

DC Source ..... Ballantine 6125B

Procedure:

a. Press AUTO-SCOPE.

b. Select channel 1 DC coupling by pressing DC (channel 1).

c. Adjust channel 1 volts/div to 1 V by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of [1.00] in LED display.

d. Press POSITION (channel 1) and rotate the Control Knob for a reading of [POS 15.00] in LED display.

e. Apply −15 V from the DC source to channel 1 input.

f. Trace should be at center graticule (limits .6 major divisions above or below center graticule).

g. Rotate the Control Knob for a reading of [POS -15.00] in LED display.

h. Apply +15 V from DC source to channel 1 input.

i. Trace should be at center graticule (limits .6 major divisions above or below center graticule).

j. Repeat steps b through i for channel 2.

PERFORMANCE TESTS

4-8. Position ΔV (Channel 1 or Channel 2) Test

Specifications:

Range: ±15 times the deflection factor selected for that channel.

Accuracy: ±4% (for a Δ ≤10 major divisions)

Description:

Test ΔV by applying an accurate p-p signal and measuring signal in ΔV mode.

Equipment:

Peak to Peak Source ..... Ballantine 6125B

Procedure:

a. Set peak to peak source to 1 V.

b. Apply peak to peak source to channel 1 input.

c. Press AUTO-SCOPE.

d. Set channel 1 volts/div to 100 mV by pressing (channel 1) and rotating the Control Knob for a reading of 100. -3 in LED display.

e. Position top of waveform to center graticule by pressing (channel 1) and rotating the Control Knob

f. Press .

g. Position bottom of waveform to center graticule by rotating the Control Knob.

h. LED display should read ⏚ 1.00 (limits ⏚ 960. -3 to ⏚ 1.04).

i. Repeat steps a through h for channel 2.

PERFORMANCE TESTS

4-9. Internal Trigger Sensitivity Test.

Specifications:

For deflection factors <10 mV/div, at least 1.4 div of vertical deflection from dc to 25 MHz increasing to 3 div at 100 MHz; for deflection factors ≥10 mV/div at least .7 div of vertical deflection from dc to 25 MHz increasing to 1.5 div at 100 MHz.

Description:

Checks for proper trigger sensitivity at 25 MHz and 100 MHz.

Equipment:

Signal Generator ..... HP Model 3200B

Procedure:

a. Set signal generator to 25 MHz.

b. Apply signal generator output to channel 1 input.

c. Press AUTO-SCOPE.

d. Set channel 1 volts/div to 5 mV by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of 5.00 -3 in LED display.

e. Set signal generator level for 1.4 div display.

f. Set Main sweep for several cycles displayed by pressing SEC/DIV (main) and rotating the Control Knob.

g. Select Main Trigger Level by pressing TRIG LVL (main).

h. Rotate the Control Knob for stable display. Stable display confirms proper trigger.

i. Set signal generator to 100 MHz.

j. Increase signal generator level for a 3 div display.

k. Rotate the Control Knob for a stable display. Stable display confirms proper trigger.

l. Set channel 1 volts/div to 100 mV by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of 100. -3 in LED display.

m. Increase signal generator level for a 1.5 div display.

n. Select main trigger level by pressing TRIG LVL (main).

o. Rotate the Control Knob for a stable display. Stable display confirms proper trigger.

PERFORMANCE TESTS

p. Set signal generator for 25 MHz.

q. Decrease signal generator level for a .7 div display.

r. Rotate the Control Knob for a stable display. Stable display confirms proper trigger.

s. Repeat steps a through r using Delayed Sweep.

PERFORMANCE TESTS

4-10. External Trigger Sensitivity Test.

Specifications:

In external÷10 at least 500 mV p-p from dc to 25 MHz increasing to 1.2 V p-p at 100 MHz; in external÷1 at least 50 mV p-p from dc to 25 MHz increasing to 120 mV p-p at 100 MHz.

Description:

Checks for proper external trigger sensitivity at 25 MHz and 100 MHz.

Equipment:

Signal Generator	HP Model 3200B
Sampling Voltmeter	HP Model 3406A
Sampling Tee	HP Model 11063A
Power Divider	General Radio Model 874-TPD
Adapter, GR874 to female BNC (2)	HP Part No. 1250-0850
Adapter, GR874 to male BNC	HP Part No. 1250-0849

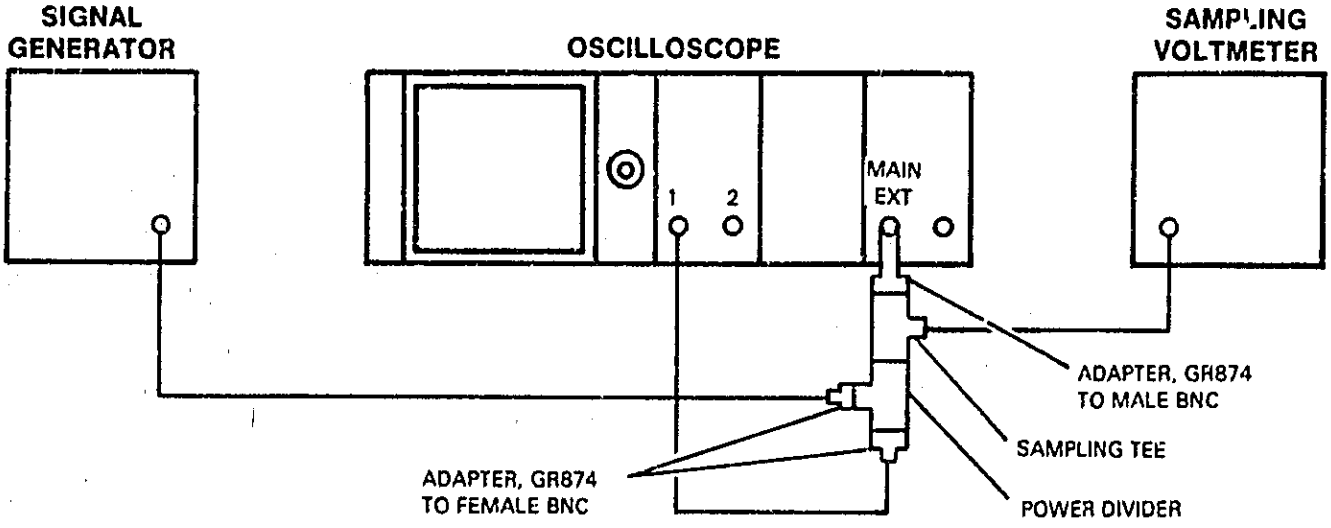


Figure 4-1. Equipment Setup For External Trigger Sensitivity Test

Procedure:

a. Select Main sweep by pressing MAIN.

b. Select external÷10 (main) by pressing EXT÷10.

c. Select main 50 ohms dc by pressing [redacted], then 50Ω (main).

d. Select channel 1 by pressing 1.

e. Select channel 1 50 ohms dc by pressing [redacted], then 50Ω (channel 1).

f. Connect signal generator to channel 1 and Ext Trigger input using 50 ohm power divider and sampling tee at EXT INPUT. Refer to figure 4-1 for equipment setup.

g. Set signal generator to 25 MHz.

PERFORMANCE TESTS

h. Set signal generator level to 175 mV rms as read on Sampling Voltmeter (approx 500 mV p-p signal).

i. Select channel 1 volts/div by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for approx 8 div signal displayed.

j. Select Main sec/div and display several cycles by pressing SEC/DIV (main) and rotating the Control Knob until several cycles are displayed.

k. Select main trigger level by pressing TRIG LEVEL (main).

l. Rotate the Control Knob for a stable display. Stable display confirms proper trigger.

m. Set signal generator to 100 MHz.

n. Set signal generator level to 420 mV rms (1.2 V p-p).

o. Select channel 1 volts/div by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for approx 8 div signal displayed.

p. Select main trigger level by pressing TRIG LEVEL (main).

q. Rotate the Control Knob for a stable display. Stable display confirms proper trigger.

r. Set signal generator level to 42 mV rms (120 mV p-p).

s. Select main external÷1 by pressing [redacted], then EXT÷10 (main).

t. Select channel 1 volts/div by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for approx 8 div signal displayed.

u. Select main trigger level by pressing TRIG LEVEL (main).

v. Rotate the Control Knob for a stable display. Stable display confirms proper trigger.

w. Set signal generator to 25 MHz.

x. Set signal generator level to 17.5 mV rms (50 mV p-p)

y. Select channel 1 volts/div by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for approx 8 div signal displayed.

z. Select main trigger level by pressing TRIG LEVEL (main).

aa. Rotate the Control Knob for a stable display. Stable display confirms proper trigger.

ab. Repeat steps a through aa for Delayed External.

PERFORMANCE TESTS

4-11. Internal Trigger Level Test.

Specifications:

Range: ±20 major divisions from the center horizontal graticule line.

Accuracy: ±(3% of reading +0.4 major div)

Description:

Check trigger level control accuracy on both positive and negative slopes.

Equipment:

Oscillator ..... HP Model 3310A

Procedure:

a. Set oscillator to approx 2 kHz and apply to channel 1 input.

b. Press AUTO-SCOPE.

c. Set channel 1 volts/div to 400 mV by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of [400. -3] in LED display.

d. Set oscillator output for a 10 division display. (Adjust trigger level as necessary for a stable display.)

e. Change channel 1 volts/div to 90 mV by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of [90.0 -3] in LED display.

f. Press ◆ (channel 1) and rotate the Control Knob for a reading of [POS -15.00] in LED display.

g. Set main trigger level to 20 by pressing ◆ (main) and rotating the Control Knob clockwise for a reading of [CH1 20.00] in LED display.

h. Waveform should be stable with trigger start point at top graticule (limits 1 major division above or below top graticule).

i. Press ◆ (channel 1) and rotate the Control Knob for a reading of [POS 15.00] in LED display.

j. Press ◆ (main) and rotate the Control Knob counterclockwise for a reading of [CH1 -20.00] in LED display.

k. Waveform should be stable with trigger start point at bottom graticule (limits 1 major division above or below bottom graticule).

l. Press AUTO-SCOPE.

m. Press DLY'D, then TRIG'D (delayed).

Note

Press ◆ (delayed) and rotate the Control Knob to view 2 or more cycles.

n. Repeat steps e through k for delayed internal trigger.

PERFORMANCE TESTS

4-12. External Trigger Level Test.

Specifications:

Range: ±1.2 V from ground reference; in Ext÷10 ±12 V from ground reference.

Accuracy: ±(3% of reading +40 mV); in Ext÷10 mode ±(3% of reading +400 mV)

Description:

Check trigger level control accuracy on both positive and negative slopes.

Equipment:

Oscillator ..... HP Model 3310A

BNC Tee ..... HP Part No. 1250-0781

Procedure:

a. Set oscillator to approx 2 kHz.

b. Apply oscillator output to channel 1 input and main external input

c. Press AUTO-SCOPE.

d. Set channel 1 volts/div to 1.2 V by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of [1.2] in LED display.

e. Set oscillator level for a 10 division display.

f. Select external÷10 (main) by pressing EXT÷10.

g. Select main trigger view by pressing ▮, then MAIN.

h. Select main trigger level by pressing TRIG LVL (main).

i. Rotate the Control Knob and note trigger level control of all positive slope.

j. Select negative slope by pressing ∫↘ (main).

k. Rotate the Control Knob and note trigger level control of all negative slope.

l. Change channel 1 volts/div to 120 mV by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of [120. -3] in LED display.

m. Decrease oscillator level for a 10 division display.

n. Select main external÷1 by pressing ▮, then EXT÷1 (main).

o. Select main trigger level by pressing TRIG LVL (main).

p. Rotate the Control Knob and note trigger level control of all negative slope.

q. Select positive slope by pressing ↗∫ (main).

r. Rotate the Control Knob and note trigger level control of all positive slope.

s. Repeat steps a through r for delayed external.

PERFORMANCE TESTS

4-13. Sweep Time Accuracy Test

Specifications:

Ranges: 5 ns/div to 1 s/div

Accuracy*: The following table gives the accuracy of the main and delayed time bases.

Sweep Time/Div	Accuracy*
5.00 ns/div to 9.99 ns/div (center 8 div only)	±3%
10.0 ns/div to 9.99 ms/div (first 10 div)	±3%
10.0 ms/div to 1.00 s/div (first 10 div)	±4%

*Within ±10°C of the temperature at which the instrument was calibrated. For temperatures beyond the ±10°C range and within 0 to +55°C, add 1%; for sweep speeds from .5 sec/div to 1 sec/div add 2%.

Description:

Tests Sweep Time Accuracy by checking sweep time of each range using a time mark generator.

Equipment:

Time Mark Generator ..... Ballantine 6125B

Procedure:

a. Connect time mark generator to Channel 1 input.

b. Select Main Sweep by pressing MAIN.

c. Select channel 1 50 ohms dc by pressing [redacted], then DC (channel 1).

d. Set time mark generator output and Main Sec/Div as shown in table 4-2 and check for accuracy as indicated.

PERFORMANCE TESTS

Table 4-2. Main Sweep Time Accuracy

Time Mark Generator Setting	Main Sec/Div		Accuracy (Major Div)
	Setting	LED Reading	
* 5 ns	5 ns	5.00 -9	8.7 - 9.3
10 ns	10 ns	10.0 -9	9.7 - 10.3
100 ns	100 ns	100. -9	9.7 - 10.3
1 µs	1 µs	1.00 -6	9.7 - 10.3
10 µs	10 µs	10.0 -6	9.7 - 10.3
100 µs	100 µs	100. -6	9.7 - 10.3
1 ms	1 ms	1.00 -3	9.7 - 10.3
10 ms	10 ms	10.0 -3	9.6 - 10.4
100 ms	100 ms	100. -3	9.6 - 10.4
1 sec	1 sec	1.00	9.6 - 10.4

*Check accuracy only over center 8 divisions (align 2nd time mark on 2nd graticule and observe 10th time mark.

e. Select delayed sweep by pressing DLY'D .

f. Set time mark generator output and Delayed Sec/Div as shown in table 4-3 and check for accuracy as indicated.

Table 4-3. Delayed Sweep Time Accuracy

Note

Set Main sec/div to 5 nsec for Delay Sweep Time Accuracy Test.

Time Mark Generator Setting	Delayed Sec/Div		Accuracy (Major Div)
	Setting	LED Reading	
* 5 ns	5 ns	5.00 -9	8.7 - 9.3
10 ns	10 ns	10.0 -9	9.7 - 10.3
100 ns	100 ns	100. -9	9.7 - 10.3
1 µs	1 µs	1.00 -6	9.7 - 10.3
10 µs	10 µs	10.0 -6	9.7 - 10.3
100 µs	100 µs	100. -6	9.7 - 10.3
1 ms	1 ms	1.00 -3	9.7 - 10.3
10 ms	10 ms	10.0 -3	9.6 - 10.4
100 ms	100 ms	100. -3	9.6 - 10.4
1 sec	1 sec	1.00	9.6 - 10.4

*Check accuracy only over center 8 divisions (align 2nd time mark on 2nd graticule and observe 10th time mark)

PERFORMANCE TESTS

4-14. Time Delay and Time Interval (ΔT) Accuracy Test.

Specifications:

Range: 0.0 nsec to 9.9999 sec

Accuracy:

Delayed Sweep Speed	Delay or Time Interval	
	<200 μsec	≥200 μsec
5 ns/div to 9.99 ns/div	±(2 ns + 0.1% of reading)	±(0.05% of reading)
≥10 ns/div	±(2 ns + 0.1% of reading + 1% of dly'd secs/div X 10 div)	±(0.05% of reading + 1% of dly'd secs/div X 10 div)

Description:

Using time marks, check accuracy of Time Delay and Time Interval (ΔT) by making measurement and checking LED display reading.

Equipment:

Time Mark Generator ..... Ballantine 6125B

Procedure:

a. Press OPTION (MENU).

b. Press soft keys in the following sequence:
   1. CALIBRATE & UTILITIES
   2. DELAY SELF CAL

Note

When Delay Self-Cal routine is complete procede to step c.

c. Apply 100 μsec time marks from time mark generator to channel 1 input.

d. Press AUTOSCALE (UNDO/REDO).

e. Select Dual mode by pressing DUAL.

f. Set main sec/div to 100 μsec by pressing SEC/DIV (main) and rotating the Control Knob for a reading of 100. -6 in LED display.

g. Set delayed sec/div to 1 μsec by pressing SEC/DIV (delayed), and rotating the Control Knob for a reading of 1.00 -6 in LED display.

h. Press DELAY and rotate the Control Knob until intensified portion of main sweep is under second time mark.

i. Select fine control by pressing FINE.

j. Observe delayed sweep and place displayed time mark on center graticule.

k. Note reading on LED display.

l. Select coarse control by pressing COARSE.

m. Rotate the Control Knob until intensified portion of main sweep is under the 10th time mark.

n. Select fine control by pressing FINE.

o. Observe delayed sweep and place displayed time mark on center graticule.

PERFORMANCE TESTS

p. Note reading on LED display.

q. Subtract reading obtained in step k from reading obtained in step p. Result should be between 799.45 µsec and 800.55 µsec.

r. Ensure time mark displayed on delayed trace is aligned with center graticule, then press .

s. Select coarse control by pressing .

t. Rotate the Control Knob until intensified portion of main sweep is under second time mark.

u. Select fine control by pressing .

v. Align time mark displayed on delayed trace with center graticule.

w. Note reading on LED display. Reading should be between 799.5 µsec and 800.5 µsec.

x. Apply 1 µsec time marks from time mark generator to channel 1 input.

y. Press .

z. Select Dual mode by pressing .

aa. Set main sec/div to 1 µsec by pressing (main) and rotating the Control Knob for a reading of 1.00 -6 in LED display.

ab. Set delayed sec/div to 10 nsec by pressing (delayed) and rotating the Control Knob for a reading of 10.0 -9 in LED display.

ac. Press and rotate the Control Knob until intensified portion of main sweep is under second time mark.

ad. Select fine control by pressing .

ae. Observe delayed sweep and place displayed time mark on center graticule.

af. Note reading on LED display.

ag. Select coarse control by pressing .

ah. Rotate the Control Knob until intensified portion of main sweep is under the 10th time mark.

ai. Select fine control by pressing .

aj. Observe delayed sweep and place displayed time mark on center graticule.

ak. Note reading on LED display.

al. Subtract reading obtained in step af from reading obtained in ak. Result should be between 7.988 µsec and 8.012 µsec.

am. Ensure time mark displayed on delayed trace is aligned with center graticule, then press .

an. Rotate the Control Knob until intensified portion of main sweep is under second time mark.

ao. Select fine by pressing .

ap. Align time mark displayed on delayed trace with center graticule.

aq. Note reading on LED display. Reading should be between 7.989 µsec and 8.011 µsec.

PERFORMANCE TESTS

4-15. Delay Jitter Test.

Specifications:

0.002% of the delay time; at 10 MHz ±10 kHz, 0.01% of the delay time.

Description:

Check delay jitter by observing a marker pulse edge at a delay time 50,000 times the sweep speed.

Equipment:

Time Mark Generator..... Ballantine 6125B

Procedure:

a. Set time mark generator to 1 μsec time marks and apply to channel 1 input.

b. Press AUTO SCOPE.

c. Set main sec/div to 5 nsec by rotating the Control Knob for a reading of 5.00 -9 in LED display.

d. Select delayed mode by pressing DLYD.

e. Set delayed sec/div to 5 nsec by pressing DLY'D (delayed) and rotating the Control Knob for a reading of 5.00 -9 in LED display.

f. Press ▌, then DELAY and rotate the Control Knob for a reading of 250.00-6 in LED display.

Note

Set intensity to maximum by pressing INTEN and rotating the Control Knob. Use a hood to shield CRT from ambient light to observe time mark.

g. Observe horizontal axis jitter of time mark rising edge. Jitter must be less than 1 major division.

PERFORMANCE TESTS

4-16. Bandwidth Test.

Specifications:

3dB down from a 5 div reference signal from 0 to +40°C.

DC-Coupled: dc to 100 MHz in 50Ω and 1 MΩ input modes.

AC-Coupled: <10 Hz to ≥100 MHz

Description:

Set a 10 MHz signal for 5 divisions amplitude then increase frequency to 100 MHz and check that amplitude is greater than 3.5 divisions.

Equipment:

Signal Generator	HP Model 3200B
Sampling Voltmeter	HP Model 3406A
Sampling Tee	HP Model 11063A
Adapter, GR874 to Male BNC	HP Part No. 1250-0849
Adapter, GR874 to Female BNC	HP Part No. 1250-0850
Attenuator, 6 dB	General Radio GR874-G6

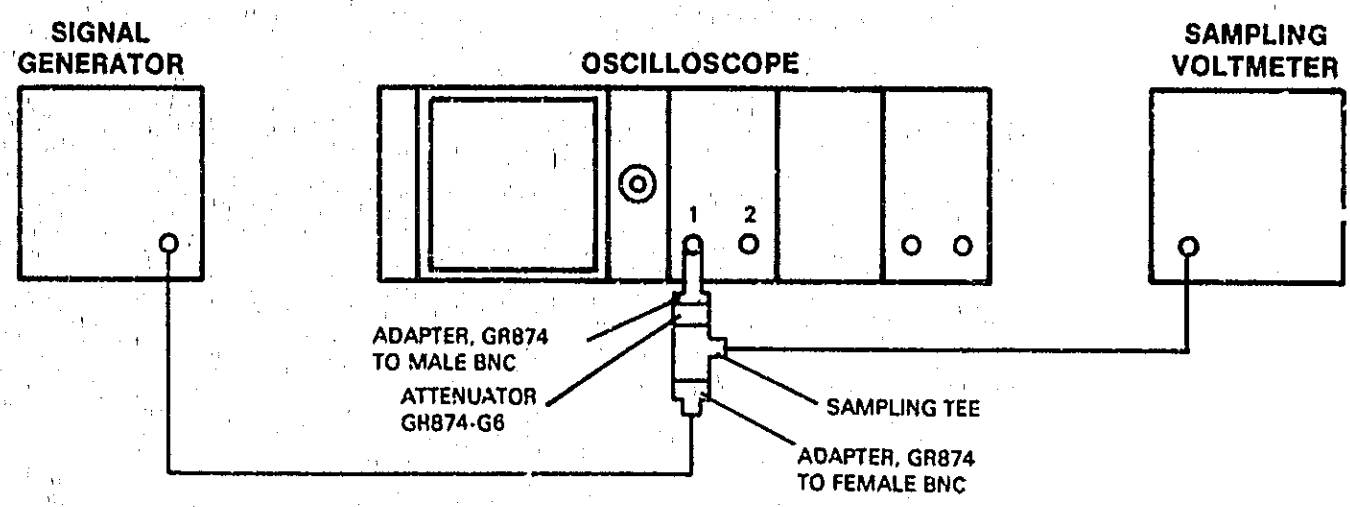


Figure 4-2. Equipment Setup for Bandwidth Test

PERFORMANCE TESTS

Procedure:

a. Connect signal generator to channel 1 input per figure 4-2.

b. Set channel 1 volts/div to 10 mV by pressing [redacted] (channel 1) and rotating the Control Knob for a reading of 10.0 -3 in LED display.

c. Set channel 1 to 50 ohms dc by pressing [redacted], then [redacted].

d. Set signal generator output for 10 MHz.

e. Set signal generator level for a 5 division display.

f. Note reading on sampling voltmeter.

g. Change signal generator to 100 MHz.

h. Reset signal generator level to reading noted in step f.

i. Display amplitude should be greater than 3.5 major divisions.

j. Repeat steps a through i for channel 2.

PERFORMANCE TESTS

4-17. Common Mode Rejection Ratio (CMRR) Test.

Specifications:

Differental (Channel 1 - Channel 2 or Channel 2 - Channel 1); CMRR is at least 20 dB from dc to 20 MHz with common mode signal amplitude equivalent to 10 div and one channel adjusted for optimum rejection.

Description:

Apply a 20 MHz signal (through equal length cables) to channel 1 and channel 2 inputs. After adjusting gain of either channel for minimum deflection remaining deflection shall be less than 1 division.

Equipment:

Signal Generator ..... HP Model 3200B
BNC Cables, 9 inch length (2) ..... HP Model 10502A
BNC Tee ..... HP Part No. 1250-0781

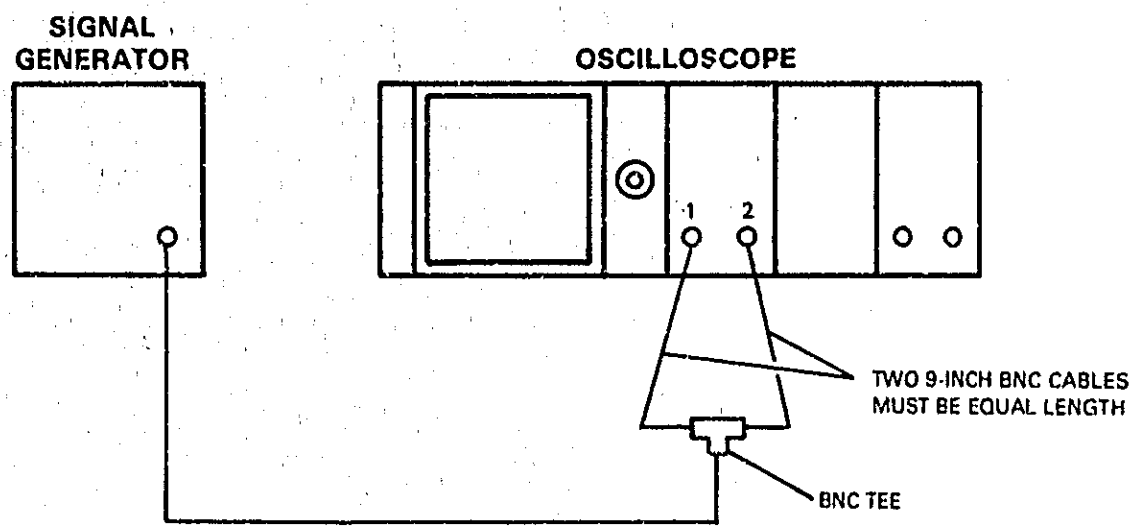


Figure 4-3. Equipment Setup for Common Mode Rejection Ratio (CMRR) Test

PERFORMANCE TESTS

Procedure:

a. Connect signal generator to channel 1 and channel 2 inputs as shown in figure 4-3

b. Set signal generator output to 20 MHz.

c. With channel 1 on and channel 2 off, set channel 1 volts/div to 100 mV by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of [100. -3] in LED display.

d. Set signal generator level for a 10 division display.

e. Turn channel 2 on and set channel 2 volts/div to 100 mV by pressing VOLTS/DIV (channel 2) and rotating the Control Knob for a reading of [100. -3] in LED display.

f. Select 1+2 mode by pressing 1+2.

g. Invert either channel by pressing ▮, then either 1 or 2 .

h. Adjust either channel volts/div for minimum amplitude displayed (difference in volts/div displayed on CRT readout denotes gain difference between channels.)

i. Display should be less than 1 major division.

PERFORMANCE TESTS

4-18. Calibrator Output Verification Test.

Specifications:

Programmable Cal Signals: The calibrator signal amplitude is programmable to 20 mV p-p ±2%, 100 mV p-p ±1%, 1 V p-p ±1%, and 10 V p-p ±1%.

Description:

Using a monitor oscilloscope, compares amplitude of calibrator output to a peak to peak source.

Equipment:

Oscilloscope ..... HP Model 1740A
Peak to Peak Source ..... Ballantine 6125B

Procedure:

a. Place rear panel Protected-Unprotected switch to the Unprotected position.

CAUTION

Do not rotate the Control Knob during this procedure or Calibration Factors will be changed.

b. Press OPTION MENU.

c. Press soft keys in the following sequence:
   1. CALIBRATE & UTILITIES
   2. FRONT PANEL CAL 1980A/B

d. After auto balance routine is completed (Menu reappears on CRT) press NEXT SEQUENCE three times until SENSITIVITY appears on CRT.

e. Set peak to peak source for a 1 kHz, 20 mV output and connect to channel A input of monitor oscilloscope.

f. Set monitor oscilloscope to 0.005 V/div, sweep speed to display two or more cycles (approx .2 μsec/div), and trigger for a stable display.

g. Adjust monitor oscilloscope channel A vernier to view a 4 division signal.

h. Disconnect peak to peak source from channel A of monitor oscilloscope. Connect rear panel Cal output to monitor oscilloscope channel A input.

i. Cal output waveform, observed on monitor oscilloscope, should be 4 divisions amplitude. Limits 4 major ±.4 minor divisions.

j. Disconnect rear panel Cal output from monitor oscilloscope and reconnect peak to peak source to channel A input of monitor oscilloscope.

PERFORMANCE TESTS

k. Set peak to peak source to 100 mV. Set monitor oscilloscope to 0.01 volts/division and adjust vernier for an 8 division display.

l. Disconnect peak to peak source from monitor oscilloscope and reconnect rear panel Cal output to channel A input of monitor oscilloscope.

m. Press AUTO-SCOPE once.

n. Cal output waveform, observed on monitor oscilloscope, should be 8 divisions amplitude. Limits 8 major ±.4 minor divisions.

o. Press AUTO-SCOPE once. Display on monitor oscilloscope should be same as in step n.

p. Disconnect rear panel Cal output from monitor oscilloscope and reconnect peak to peak source to channel A input of monitor oscilloscope.

q. Set peak to peak source to 1 V. Set monitor oscilloscope to 0.1 volts/division and adjust vernier for an 8 division display.

r. Disconnect peak to peak source from monitor oscilloscope and reconnect rear panel Cal output to channel A input of monitor oscilloscope.

s. Press AUTO-SCOPE once.

t. Cal output waveform, observed on monitor oscilloscope, should be 8 divisions amplitude. Limits 8 major ±.4 minor divisions.

u. Disconnect Cal output from monitor oscilloscope and reconnect Peak to Peak Source to channel A of monitor oscilloscope.

v. Set peak to peak source to 10 V. Set monitor oscilloscope to 1 volt/division and adjust vernier for an 8 division display.

w. Disconnect peak to peak source from monitor oscilloscope and reconnect rear panel Cal output to channel A of monitor oscilloscope.

x. Press AUTO-SCOPE once.

y. Cal output waveform, observed on monitor oscilloscope, should be 8 divisions amplitude. Limits 8 major ±.4 minor divisions.

z. Press AUTO-SCOPE once. Display on monitor oscilloscope should be same as step y.

aa. Press AUTO-SCOPE once. Display on montior oscilloscope should be same as step y.

ab. Exit front panel cal routine by pressing OPTION MENU.

ac. Set rear panel Protected-Unprotected switch to the Protected position.

Table 4-4. Performance Test Record (Page 1 of 6)

HEWLETT-PACKARD
MODEL 1980 OSCILLOSCOPE
MEASUREMENT SYSTEM

Tested by_____

Work Order No._____

SERIAL NO._____ Recommend Calibration Interval _____ Months

Date_____

Paragraph Number	Test			Results
4-6	DEFLECTION FACTOR TEST	Channel 1	Step e.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Step h.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Step k.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Step n.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
		Channel 2	Step e.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Step h.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Step k.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Step n.	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
4-7	VERTICAL POSITION TEST	Channel 1	Step f.	Minimum — 0.6 major divisions Above Center Actual — Maximum — 0.6 major divisions Below Center
			Step h.	Minimum — 0.6 major divisions Above Center Actual — Maximum — 0.6 major divisions Below Center

Table 4-4. Performance Test Record (Page 2 of 6)

Paragraph Number	Test			Results
4-7	VERTICAL POSITION TEST (Cont'd)	Channel 2	Step f.	Minimum — 0.6 major divisions Above Center Actual — Maximum — 0.6 major divisions Below Center
			Step h.	Minimum — 0.6 major divisions Above Center Actual — Maximum — 0.6 major divisions Below Center
4-8	POSITION ΔV (CHANNEL 1 OR CHANNEL 2) TEST			
		Channel 1		Minimum [-960. -3] Actual — Maximum [-1.04]
		Channel 2		Minimum [-960. -3] Actual — Maximum [-1.04]
4-9	INTERNAL TRIGGER SENSITIVITY TEST	MAIN	Step h.	Stable Display____
			Step k.	Stable Display____
			Step o.	Stable Display____
			Step r.	Stable Display____
		DELAYED	Step h.	Stable Display____
			Step k.	Stable Display____
			Step o.	Stable Display____
			Step r.	Stable Display____
4-10	EXTERNAL TRIGGER SENSITIVITY TEST	MAIN	Step l.	Stable Display____
			Step q.	Stable Display____
			Step v.	Stable Display____
			Step aa.	Stable Display____
		DELAYED	Step l.	Stable Display____
			Step q.	Stable Display____
			Step v.	Stable Display____
			Step aa.	Stable Display____

Table 4-4. Performance Test Record (Page 3 of 6)

SERIAL NO._____ Tested by_____

Paragraph Number	Test				Results
4-11	INTERNAL TRIGGER LEVEL TEST		MAIN	Step h.	Stable Display____ (top graticule ±1 major div)
				Step k.	Stable Display____ (bottom graticule ±1 major div)
			DELAYED	Step h.	Stable Display____ (top graticule ±1 major div)
				Step k.	Stable Display____ (bottom graticule ±1 major div)
4-12	EXTERNAL TRIGGER LEVEL TEST		MAIN	Step i.	Control of all positive slope____
				Step k.	Control of all negative slope____
				Step p.	Control of all negative slope____
				Step r.	Control of all positive slope____
			DELAYED	Step i.	Control of all positive slope____
				Step k.	Control of all negative slope____
				Step p.	Control of all negative slope____
				Step r.	Control of all positive slope____
4-13	SWEEP TIME ACCURACY TEST	MAIN	Sec/Div	5 nsec	Minimum — 8.7 major divisions Actual — Maximum — 9.3 major divisions
			Sec/Div	10 nsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	100 nsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	1 μsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions

Table 4-4. Performance Test Record (Page 4 of 6)

Paragraph Number	Test				Results
4-13	SWEEP TIME ACCURACY TEST	MAIN (Cont'd)	Sec/Div	10 μsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	100 μsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	1 msec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	10 msec	Minimum — 9.6 major divisions Actual — Maximum — 10.4 major divisions
			Sec/Div	100 msec	Minimum — 9.6 major divisions Actual — Maximum — 10.4 major divisions
			Sec/Div	1 sec	Minimum — 9.6 major divisions Actual — Maximum — 10.4 major divisions
		DELAYED	Sec/Div	5 nsec	Minimum — 8.7 major divisions Actual — Maximum — 9.3 major divisions
			Sec/Div	10 nsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	100 nsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	1 μsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	10 μsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
			Sec/Div	100 μsec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions

Table 4-4. Performance Test Record (Page 5 of 6)

SERIAL NO._____ Tested by_____

Paragraph Number	Test		Results
4-13	SWEEP TIME ACCURACY TEST (Cont'd)		
	DELAYED	Sec/Div 1 msec	Minimum — 9.7 major divisions Actual — Maximum — 10.3 major divisions
		Sec/Div 10 msec	Minimum — 9.6 major divisions Actual — Maximum — 10.4 major divisions
		Sec/Div 100 msec	Minimum — 9.6 major divisions Actual — Maximum — 10.4 major divisions
		Sec/Div 1 sec	Minimum — 9.6 major divisions Actual — Maximum — 10.4 major divisions
4-14	TIME DELAY AND TIME INTERVAL (ΔT) TEST	Step q.	Minimum — 799.45 μsec Actual — Maximum — 800.55 μsec
		Step w.	Minimum — 799.5 μsec Actual — Maximum — 800.5 μsec
		Step al.	Minimum — 7.988 μsec Actual — Maximum — 8.012 μsec
		Step aq.	Minimum — 7.989 μsec Actual — Maximum — 8.011 μsec
4-15	DELAY JITTER TEST		<1 major division_____
4-16	BANDWIDTH TEST	Channel 1	>3.5 major divisions_____
		Channel 2	>3.5 major divisions_____
4-17	COMMON MODE REJECTION RATIO (CMRR) TEST		<1 major division_____

Table 4-4. Performance Test Record (Page 6 of 6)

Paragraph Number	Test		Results
4-18	CALIBRATOR OUTPUT VERIFICATION TEST	Step i.	Minimum — 4 major divisions - .4 minor divisions Actual — Maximum — 4 major divisions + .4 minor divisions
		Step n.	Minimum — 8 major divisions - .4 minor divisions Actual — Maximum — 8 major divisions + .4 minor divisions
		Step o.	Minimum — 8 major divisions - .4 minor divisions Actual — Maximum — 8 major divisions + .4 minor divisions
		Step t.	Minimum — 8 major divisions - .4 minor divisions Actual — Maximum — 8 major divisions + .4 minor divisions
		Step y.	Minimum — 8 major divisions - .4 minor divisions Actual — Maximum — 8 major divisions + .4 minor divisions
		Step z.	Minimum — 8 major divisions - .4 minor divisions Actual — Maximum — 8 major divisions + .4 minor divisions
		Step aa.	Minimum — 8 major divisions - .4 minor divisions Actual — Maximum — 8 major divisions + .4 minor divisions

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

This section describes adjustments and checks required to return the instrument to peak operating capabilities after repairs have been made. Included in this section is a table of Recommended Test Equipment (table 5-1), two adjustment procedures (Normal Calibration and Complete Calibration), equipment setups, and a table of Required Adjustments After Repair (table 5-3).

5-2. NORMAL CALIBRATION.

Normal Calibration should be completed on a periodic basis. During a normal calibration only the Front Panel Calibration routine need be addressed. The period of the normal calibration cycle will depend on the user's environment and number of hours of operation. In a controlled laboratory environment one year periods may be sufficient. With normal rack mounted usage (based on 2000 hours/year operating time) six month cycles are recommended.

For best overall operation the Normal Calibration should be completed at the user's site, i.e., if the instrument is rack mounted, the Normal Calibration should be completed while instrument is installed in the rack.

5-3. COMPLETE CALIBRATION.

Complete Calibration is a listing of all adjustments in the 1960 and is intended for use after repairs have been made. Complete Calibration procedures do not need to be completed on a periodic basis. When repairs have been made, refer to table 5-3 (Required Adjustments) to determine which adjustments must be made after each repair. The Complete Calibration may be made at any time, if desired. All adjustments should be made in the order listed.

After a Complete Calibration has been completed, a Normal Calibration should be performed at the user's site.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures.

5-5. EQUIPMENT REQUIRED.

Test equipment is listed in the Recommended Test Equipment table in Section I of this manual and in table 5-1.

Table 5-1. Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model
Digital Voltmeter (DVM)	range: 0 to 100 Vdc accuracy: ±0.1% input impedance: 10 Mohm	HP 3465A - or - HP 3438A
Electronic Counter	range: 0 to 10 MHz resolution: 8 digit accuracy: ±0.1 Hz	HP 5382A
Probe, High Voltage	division ratio: 1000:1 (into 10 Mohm DVM input)	HP 34111A
Function Generator	range: 10 Hz to 100 kHz squarewave 2 kHz to 50 kHz sinewave level: 0 to 10 Vp-p	HP 3310A
Oscilloscope	2 channels, delayed sweep (sensitivity:) 5 mV/div Bandwidth: 100 MHz	HP 1740A
Probe	input R: 1 Mohm shunt C: 12 pF division ratio: 10:1 comp. range: 20 to 26 pF	HP 10041A
Peak to Peak Source	level: 20 mV to 100 V accuracy: ±0.25%	Ballentine 6125B
Time Mark Generator	range: 5 nsec to 1 sec accuracy: ±0.01%	Ballantine 6125B
LCR Meter	range: 3 pF to 20 pF accuracy: ±5%	HP 4332A
DC Source	level: 0 to 100 Vdc accuracy: ±0.25%	Ballantine 6126B

5-6. ADJUSTMENTS.

In order to achieve the optimum specifications from the 1980 an accurate external peak to peak voltage source and timing source should be used to set gain and sweep speeds. If accuracies between 4% and 6% are sufficient, the 1980 calibrator may be used for calibration.

Table 5-2. Required Adjustments After Repair

	5-8	5-9	5-10	5-11	5-12	5-13	5-14	5-15	5-16	5-17	5-18	5-19	5-20	5-21	5-22	5-23	5-24	5-25	5-26	5-27	5-28	5-29	5-30	5-31	5-32
A1 Board (LVPS)	X	X						X					X		X		X	X		X	X			X	
A1 LVPS components (IC's and pass devices)	X	X															X	X		X					
Vertical Output Hybrid																			X	X		X			X
Horizontal Output components													X		X						X				
A2 HV xfmr;multiplier;osc.		X	X		X	X		X	X	X	X									X		X			
A3 GATE board		X			X	X	X		X	X	X									X		X			
A4 PROCESSOR board																	X	X		X					
NV RAM's																				X					
A5 SCOPE board												X	X	X		X		X	X	X		X			X
Vertical Hybrid																			X	X		X			X
Trigger Hybrid																							X		
Horizontal Hybrid												X	X	X						X					
A10 Delay Line Assy																				X					X
A12 Battery (Low Voltage or Inst. off)																				X					
A13 Vertical Attenu. board																				X			X	X	
A14 Trigger Attenuator board																				X			X		
A19 RPG Assy																									
A20 CRT Assy	X	X	X	X	X	X	X	X	X	X	X		X		X	X					X	X			X

5-6. ADJUSTMENT PROCEDURES.

NORMAL CALIBRATION

5-7. Front Panel Calibration.

Reference:

None

Description:

Using operator setups, instrument automatically selects and stores in memory a number of calibration factors.

Equipment:

Peak - Peak Source ..... Ballantine 6125B
Time Mark Generator ..... Ballantine 6125B

Procedure:

a. Place rear panel "Cal" switch in the "Unprotected" position.

b. Press OPTION MENU.

c. Press Soft Keys in the following sequence:
   1. CALIBRATE & UTILITIES
   2. FRONT PANEL CAL 1980A/B

d. Proceed through the FRONT PANEL CALIBRATION routine as instructed by messages displayed on CRT.

Note

During the Front Panel Calibration routine error codes may be generated. The error codes are displayed on the CRT in inverse video and indicate what area of the Cal routine failed. Refer to table 5-4 for error codes and a brief description.

Note

If an external timing source is to be used for Main and Delayed Sweep calibration, EXT TIME MARK must be selected during the Front Panel Calibration routine. It may be necessary to adjust the volts/division, vertical position, and trigger level for a stable display.

e. When the FRONT PANEL CALIBRATION routine is complete, place rear panel "Cal" switch to "Protected" position.

Note

Calibration routine must be completed and the message CAL MEMORY NOT PROTECTED must be received prior to placing the Protected-Unprotected switch in the protected position. If the switch is placed in the protected position without receiving this message, the front panel will be locked out.

ADJUSTMENTS

COMPLETE CALIBRATION

Note

Disconnect Model 1980 power cord. Remove top and bottom covers. Reconnect power cord, apply power and allow to warm up for at least 30 minutes. If a complete PC board assembly has been replaced, mechanically center all adjustable resistors on that assembly before starting the Front Panel Calibration or Complete Calibration.

Note

If, upon instrument power up, the LED Display is flashing Err 40 the instrument Cal Factors have changed. At this time the user may desire to select the Front Panel Calibration routine and enter more meaningful Cal Factors. The first three calibration sequences, positioning, gain, and timing, could be considerably off and affect the ability to easily accomplish the Complete Calibration routine. The keyboard is free to use at all times in the calibration routine and it may be necessary to select and adjust , , , etc., to obtain a suitable display.

5-8. Power Supply Adjustment.

Reference:

Service Sheets 1,2,3,4.

Description:

The +15 Vdc Power Supply is adjusted for an output of +15 Vdc and all other supplies are checked.

Equipment:

Digital Voltmeter (DVM) ..... HP Model 3465A

Procedure:

a. Connect + input of DVM to "+15V REF" output on rear panel and – input of DVM to GND.

Note

If +15 V is measured on the LVPS Board Assembly (A1) the reading will be approximately 15 mV higher than measured on rear panel output.

b. Adjust LV ADJ (A1R7) until DVM indicates +15 V ±15 mV. Refer to figure 5-1 for adjustment location.

c. Monitor remaining supplies at test points labeled on the A1 (LVPS) board and verify performance within limits stated in table 5-2. Refer to figure 5-1 for test point locations.

ADJUSTMENTS

Table 5-3. LVPS Voltage Limits

Test Point	Low Limit	Nominal	High Limit
+100	+92.63	97.5	+102.38
+ 43	+40.7	+42.4	+ 44.1
+ 6	+ 5.98	+ 6.1	+ 6.22
+ 5	+ 5.07	+ 5.17	+ 5.27
- 3	- 3.23	- 3.3	- 3.37
- 5	- 5.0	- 5.1	- 5.2
- 12	-11.86	-12.1	- 12.34
- 24	-22.8	-24.15	- 25.2

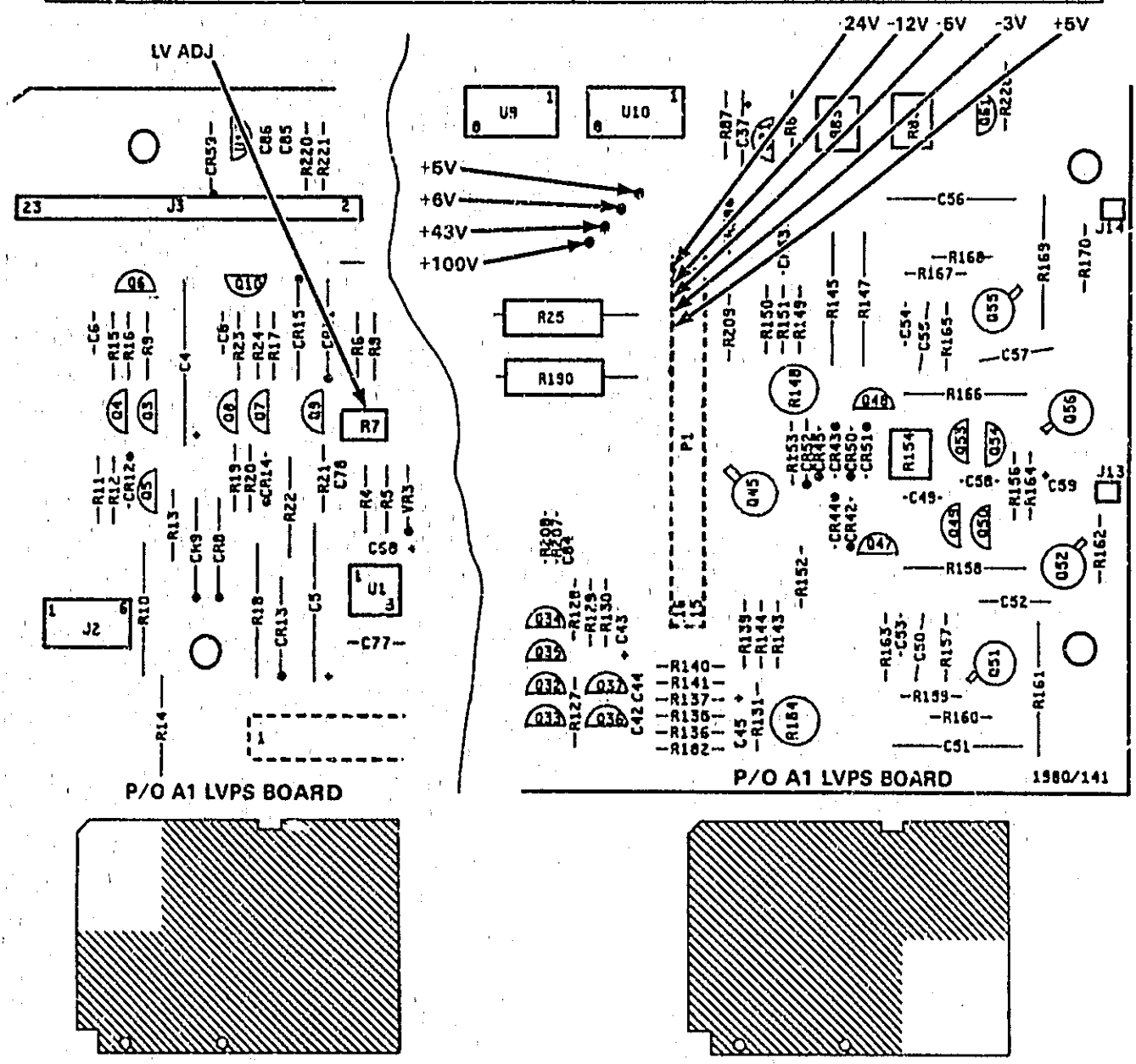


Figure 5-1. LVPS Test Point and Adjustment Location

ADJUSTMENTS

5-9. Thermal Shutdown Adjustment.

Reference:

Service Sheet 2.

Description:

A1R231 is adjusted for the same current flow through A9A2U1 and the newly installed U1. Adjustment is required at the initial installation of A1 and U1 and need not be repeated unless A1, A9A2U1, or U1 are subsequently replaced.

Equipment:

0-25 VDC External Power Supply ..... HP 6216A or equivalent
DVM ..... HP 3466A

Procedure:

a. Allow instrument to stabilize at ambient temperature for at least 2 hours with covers removed and power off

b. Connect + lead of power supply to A1TP1 and - lead to chassis ground.

c. Connect + lead of DVM to A1TP2 and - lead to chassis ground.

NOTE

Do not turn instrument power on.

d. Center A1R231 and turn external power supply on set to +15 ± .25 VDC.

e. DVM should read 2.98 ± .400 VDC.

f. Change + lead of DVM to A1TP3 and - lead to A1TP2 and adjust A1R231 for a reading of 0.00 ±.005 VDC.

g. Remove DVM and external power supply and proceed with normal instrument calibration.

ADJUSTMENTS

5-10. High Voltage Power Supply Adjustment.

Reference:

Service Sheet 5.

Description:

The high voltage power supply is adjusted for −2750 Vdc.

Equipment:

Digital Voltmeter (DVM) ..... HP Model 3465A
High Voltage Probe ..... HP Model 34111A
DC Source ..... Ballantine 6125B

Procedure:

a. Set DC source for a 100 V output.

b. With DVM and High Voltage Probe monitor 100 V output of DC source. Note reading.

c. Multiply reading obtained in step b by 27.5 and record result.

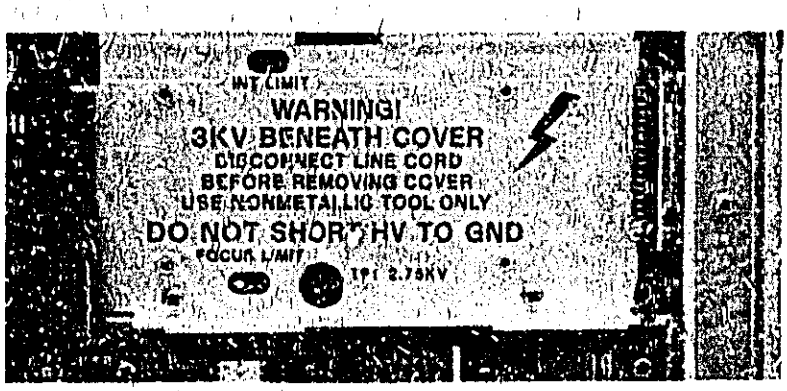
CAUTION

Extreme care must be taken not to arc the high voltage test point to chassis with the high voltage probe. Arcing the high voltage test point to ground may cause damage to some IC's.

d. Place High Voltage probe on HV test point A2TP1. Refer to figure 5-2 for test point location.

e. Adjust HV ADJ (A3R83) for result obtained in step c. (HV should be adjusted to −2750 V ±10V.) Refer to figure 5-2 for adjustment location.

ADJUSTMENTS



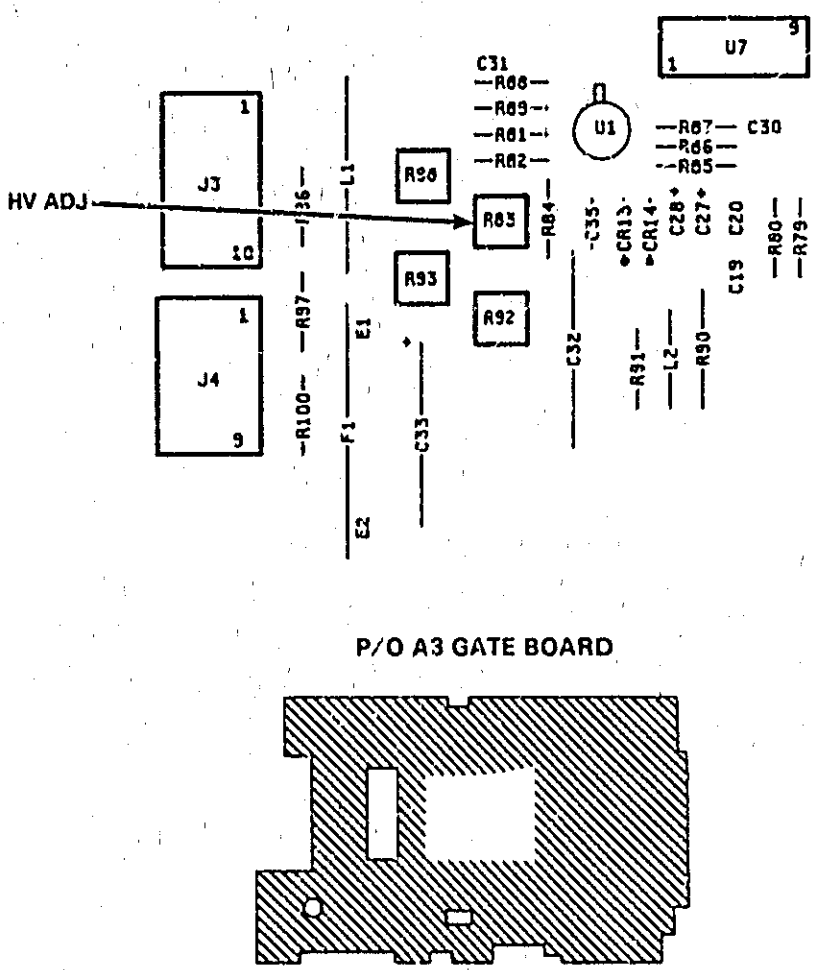


Figure 5-2. High Voltage Test Point and Adjustment Location

ADJUSTMENTS

5-11. Intensity Limit Adjustment.

Reference:

Service Sheet 5.

Description:

The Intensity Limit is adjusted for proper trace intensity limits. The Intensity Limit Adjustment varies with the cutoff value of the specific CRT installed.

Equipment:

Nonmetallic adjustment tool.

Procedure:

a. Obtain a main sweep auto trace by removing all signal inputs and pressing AUTO-SCOPE.

b. Set main sec/div to .1 msec/div by rotating the Control Knob for a reading of [100. -6] in LED display.

c. Press [ ].

d. Rotate the Control Knob for a reading of [18] in LED display.

e. Using nonmetallic adjustment tool adjust INT LIMIT (A2R14) until trace is just extinguished. (Shade CRT from ambient light to insure trace is off.) Adjustment should be made with H ' cover in place. Refer to figure 5-3 for adjustment location.

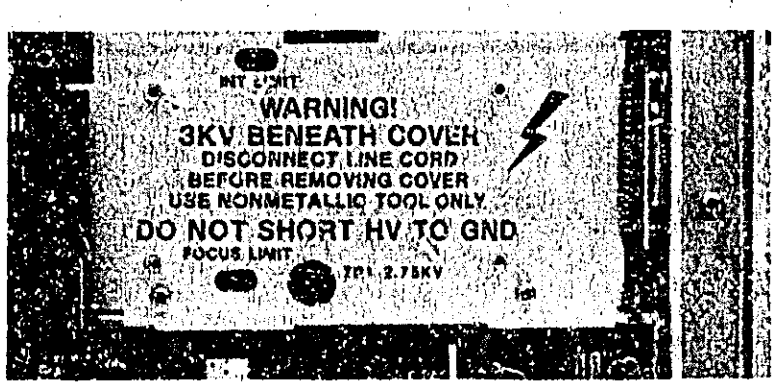


Figure 5-3. Intensity Limit Adjustment Location

ADJUSTMENTS

5-12. Trace Alignment Adjustment.

Reference:

Service Sheet 5.

Description:

The Align control is adjusted for best trace and CRT graticule alignment.

Equipment:

None

Procedure:

a. Obtain a main sweep auto trace by removing all signal inputs and pressing AUTO-SCOPE.

b. Set main sec/div to 100 µsec by rotating the Control Knob for a reading of [100. -6] in LED display.

c. Position trace on center graticule line of CRT.

d. Adjust front panel ALIGN control until trace is aligned with center CRT graticule.

e. Position trace to top graticule. Check alignment.

f. Position trace to bottom graticule. Check alignment.

g. Readjust alignment as necessary for optimum alignment at top, bottom, and center graticules. (Typical alignment with most CRT's will be quite good, however, a maximum deviation of 1/2 minor division is allowed.)

ADJUSTMENTS

5-13. Pattern Adjustment.

Reference:

Service Sheet 5.

Description:

Pattern is adjusted for best raster (minimum barreling and pincushioning).

Equipment:

Function Generator ..... HP Model 3310A

Procedure:

a. With function generator, apply a sine wave of approximately 50 kHz, and approximately 1 volt peak to peak to channel 1 input.

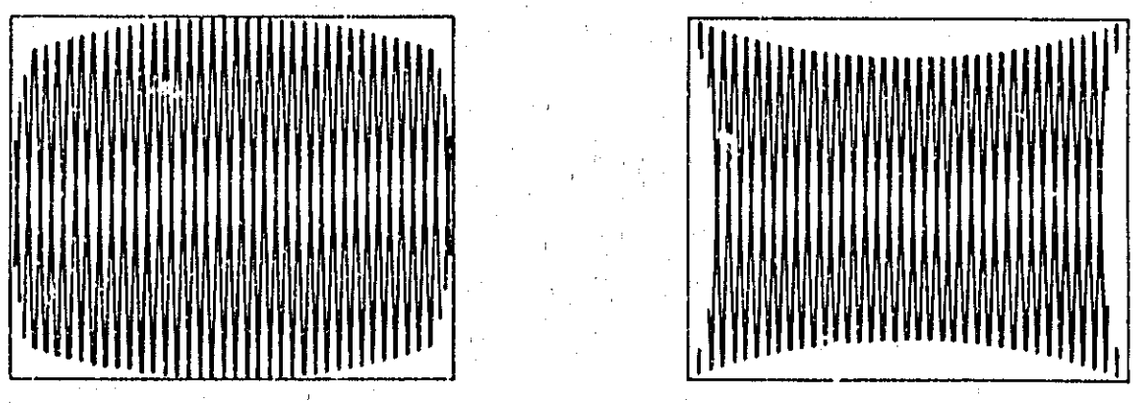
b. Press AUTO SCOPE.

c. Turn charecters off by pressing CHAR.

d. Set channel 1 volts/division for a 10 division display (centered) by pressing VOLTS (channel 1) and rotating the Control Knob.

e. Set main sec/div to 1 msec by pressing SEC (main) and rotating the Control Knob for a reading of 1.00 -3 in LED display.

f. Adjust PATTERN (A3R92) for best raster (minimum barreling and pincushioning) of displayed pattern. Refer to figure 5-4 for illustration of barreling and pincushioning. Refer to figure 5-5 for adjustment location.

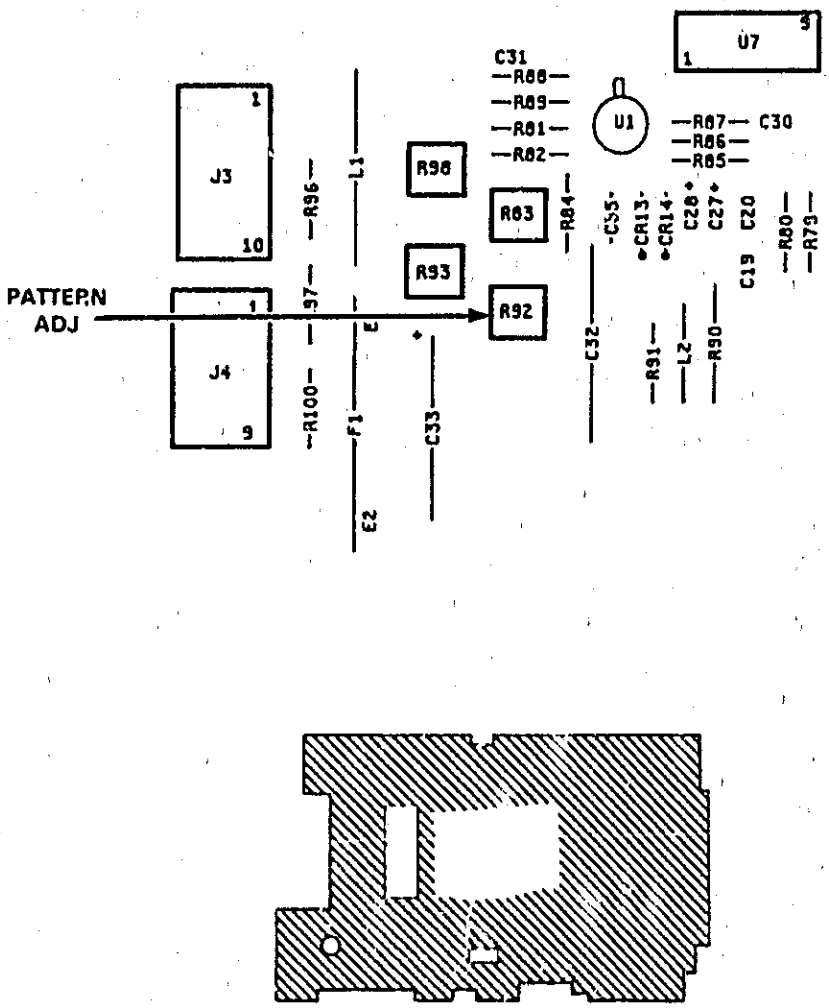


BARRELING PINCUSHIONING

Figure 5-4. Barreling and Pincushioning

ADJUSTMENTS

g. Remove input signal from channel 1.



P/O A3 GATE BOARD

Figure 5-5. Pattern Adjustment Location

ADJUSTMENTS

5-14. Orthogonality Adjustment.

Reference:
Service Sheet 5.

Description:
Aligns y-axis trace with vertical CRT graticule.

Equipment:
Function Generator ..... HP Model 3310A

Procedure:

a. With function generator, apply a sine wave of approximately 50 kHz, and approximately 1 volt peak to peak to channel 1 input.

b. Press AUTO-SCOPE.

c. Using [illegible] (channel 1) and [illegible] (channel 1), adjust for a signal amplitude of 10 div and centered vertically.

d. Select 1 vs 2 mode by pressing [illegible], then [illegible].

e. Press [illegible] (channel 2) and rotate the Control Knob until trace is over center vertical graticule.

f. Adjust ORTHO (A3R93) to align trace with center vertical graticule. Refer to figure 5-6 for adjustment location.

g. Rotate the Control Knob until trace is over left CRT graticule. Note alignment. Rotate the Control Knob until trace is over right CRT graticule. Note alignment.

h. Readjust ORTHO (A3R93) for optimum alignment at left, center and right vertical graticules. (A maximum deviation of 1/2 minor division is allowed.) Refer to figure 5-6 for adjustment location.

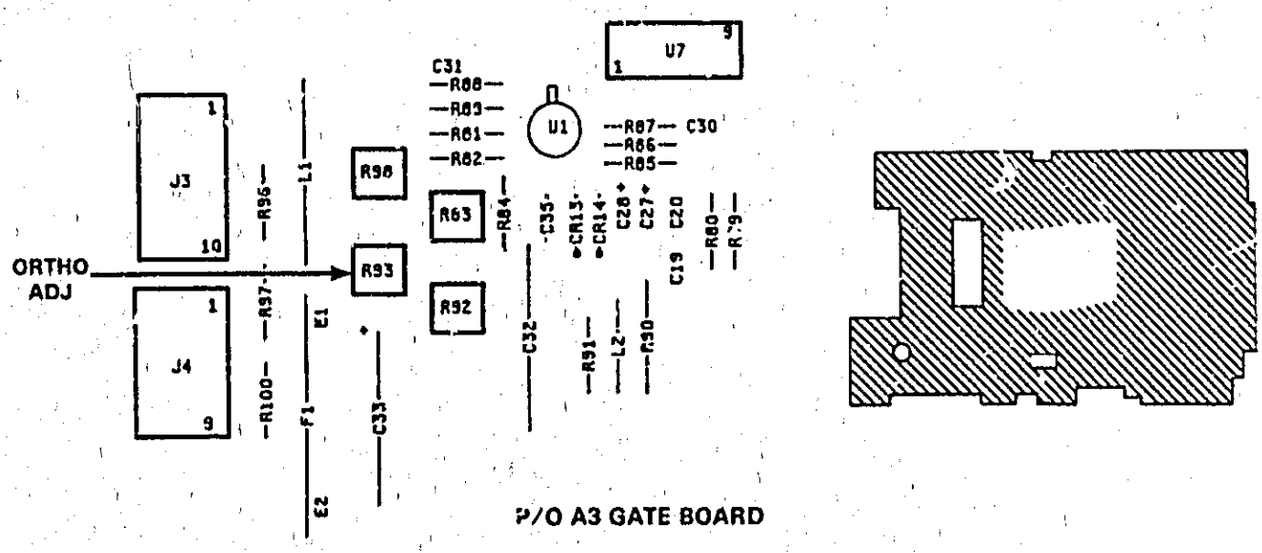


Figure 5-6. Orthogonality Adjustment Location

ADJUSTMENTS

5-15. Flood Gun Pattern Adjustment.

Reference:

Service Sheet 5.

Description:

Adjusts Floodgun for even background illumination.

Equipment:

None

Procedure:

a. Set trace intensity to Ob / pressing [WRITE THRU] and rotating the Control Knob for a reading of [0] in LED display.

b. Turn characters off by pressing [CHAR ON/OFF].

c. Turn front panel GRAT INTEN control to maximum (fully to the right).

d. Adjust FG PAT (A3R98) for maximum even illumination of CRT. Refer to figure 5-7 for adjustment location.

e. Rotate front panel GRAT INTEN control throughout its range and check that background illumination remains constant.

f. If uneven illumination occurs reduce background slightly by adjusting FG PAT (A3R98) and recheck GRAT INTEN range.

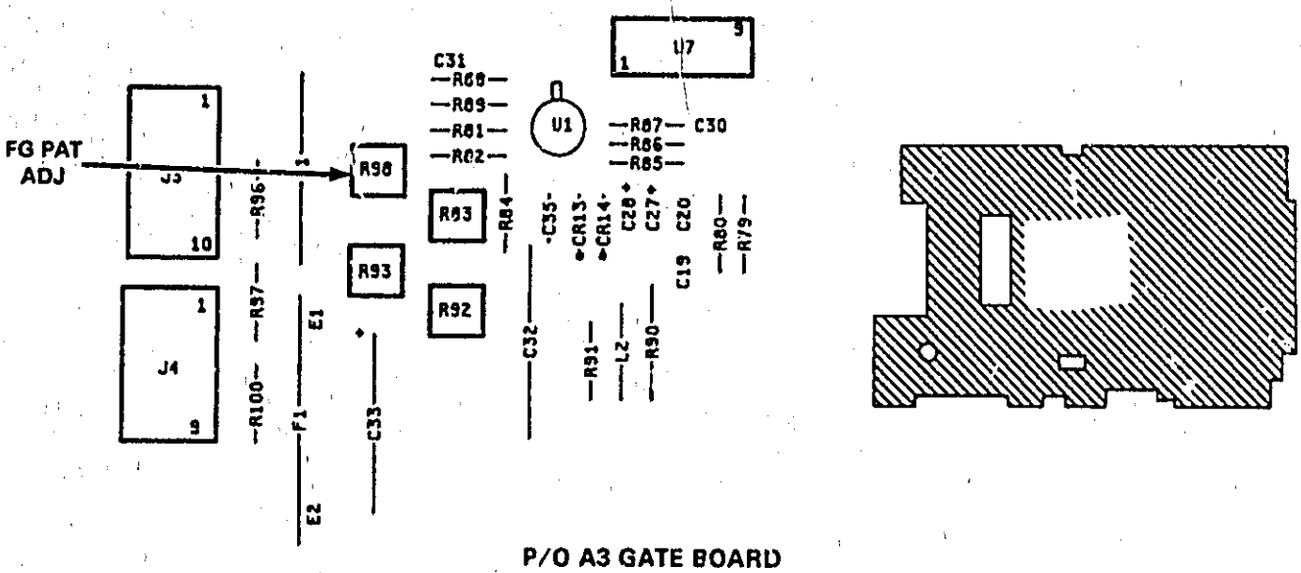


Figure 5-7. Floodgun Pattern Adjustment Location

5-16. Character Gain and Position Adjustments.

Reference:

Service Sheet 10, 13.

Description:

Adjusts characters for proper vertical and horizontal positioning.

Equipment:

None

Procedure:

a. Turn characters on by pressing [CHAR DISPLAY].

b. Press [CHAR GAIN] and rotate the Control Knob until characters are displayed at a comfortable viewing level (approximately [CHAr 70] in LED display).

c. Adjust CHAR POS (A1R85) to vertically center characters on CRT. Refer to figure 5-8 for adjustment location.

d. Adjust CHAR GAIN (A1R83) until top of first line of characters and bottom of last line of characters are just inside upper and lower CRT graticules. Refer to figure 5-8 for adjustment location.

e. Repeat steps c and d above until characters are properly positioned vertically.

f. Adjust A1R107 (Horiz Char Position) until CH1 and NT are approximately 1 minor division to right of far left vertical graticule. Refer to figure 5-8 for adjustment location.

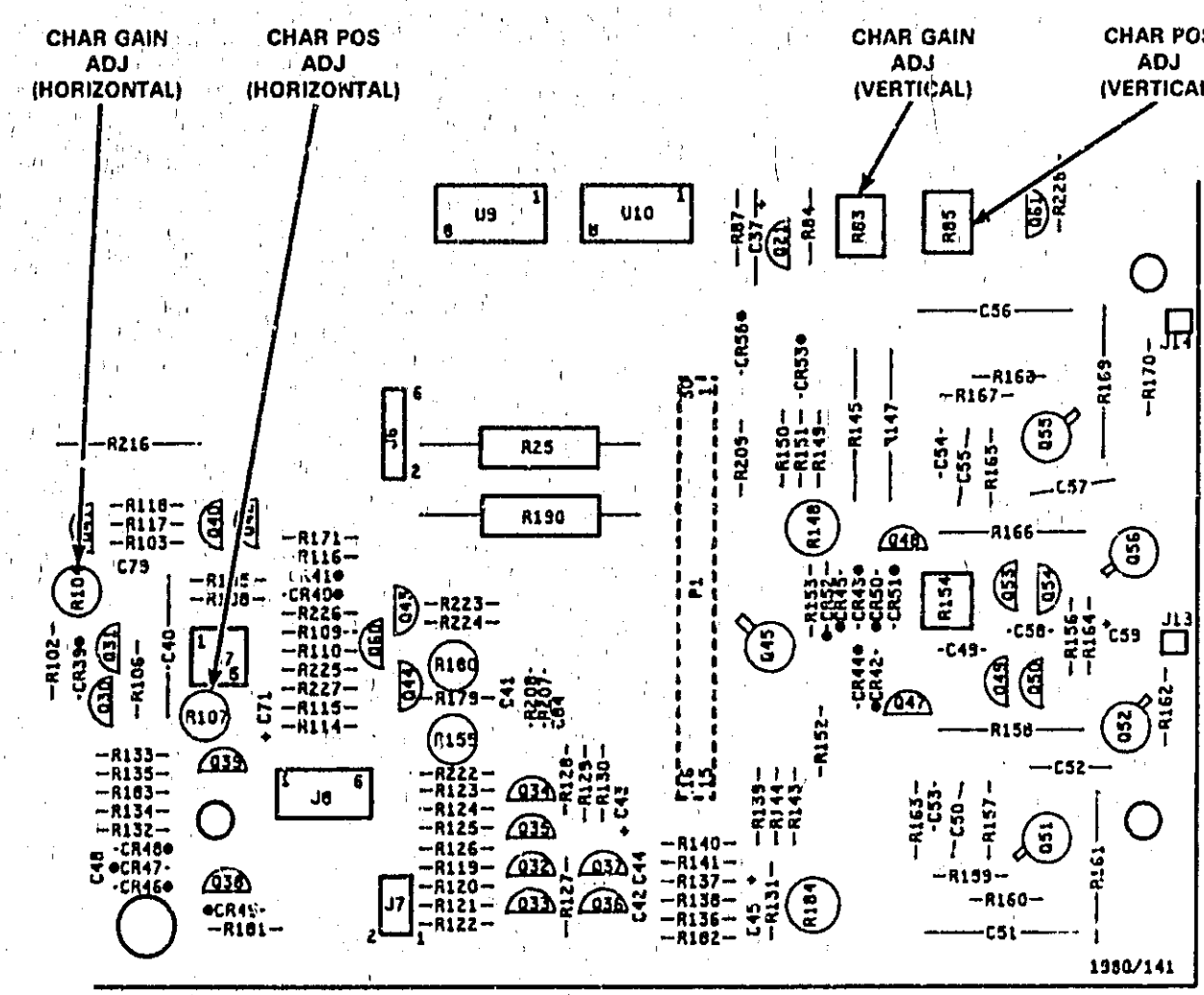
g. Press [2 INP] (channel 2), then press [INTEN ALT].

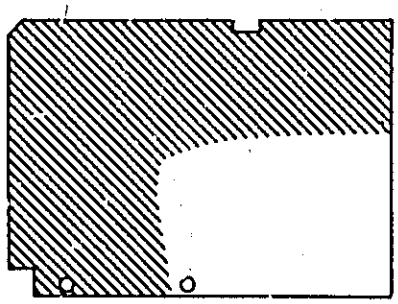
h. Adjust A1R104 (Horiz Char Gain) until CH2 and DLY are approximately 1 minor division to right of center vertical graticule. Refer to figure 5-8 for adjustment location.

i. Repeat steps f and h if necessary to obtain proper horizontal character positioning.

j. Turn characters off by pressing [CHAR DISPLAY].

ADJUSTMENTS





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Figure 5-8. Character Gain and Position Adjustment Locations

ADJUSTMENTS

5-17. Gate and Dynamic Focus Pulse Response Adjustments.

Reference:

Service Sheet 6.

Description:

Adjusts Gate pulse and the Dynamic Focus pulse for the best rise time and overshoot.

Equipment:

Oscilloscope ..... HP Model 1740A
Oscilloscope Probe ..... HP Model 10041A

Procedure:

a. Press AUTO-SCOPE, then set characters to off by pressing CHAR.

b. Set main sweep to 50 nsec/div by rotating the Control Knob for a reading of [50.0 -9] in LED display.

c. Connect monitor oscilloscope using a 10:1 probe to 95 wire of A3 board. Refer to figure 5-9 for wire location.

d. Press ENTER and rotate the Control Knob for approximately a 25 V peak to peak gate pulse.

e. Monitor Gate Pulse and alternately adjust HF1 (A3R63) and HF3 (A3C11) for fastest risetime and optimum corner of positive gate pulse. Overshoot on pulse should be less than 5%. Refer to figure 5-9 for adjustment location.

f. Move monitor oscilloscope probe to 93 wire of A3 board. Refer to figure 5-9 for wire location.

g. Monitor negative Dynamic Focus pulse and alternately adjust HF2 (A3C6) and HF4 (A3R23) for fastest risetime and less than 5% overshoot. Refer to figure 5-9 for adjustment location.

ADJUSTMENTS

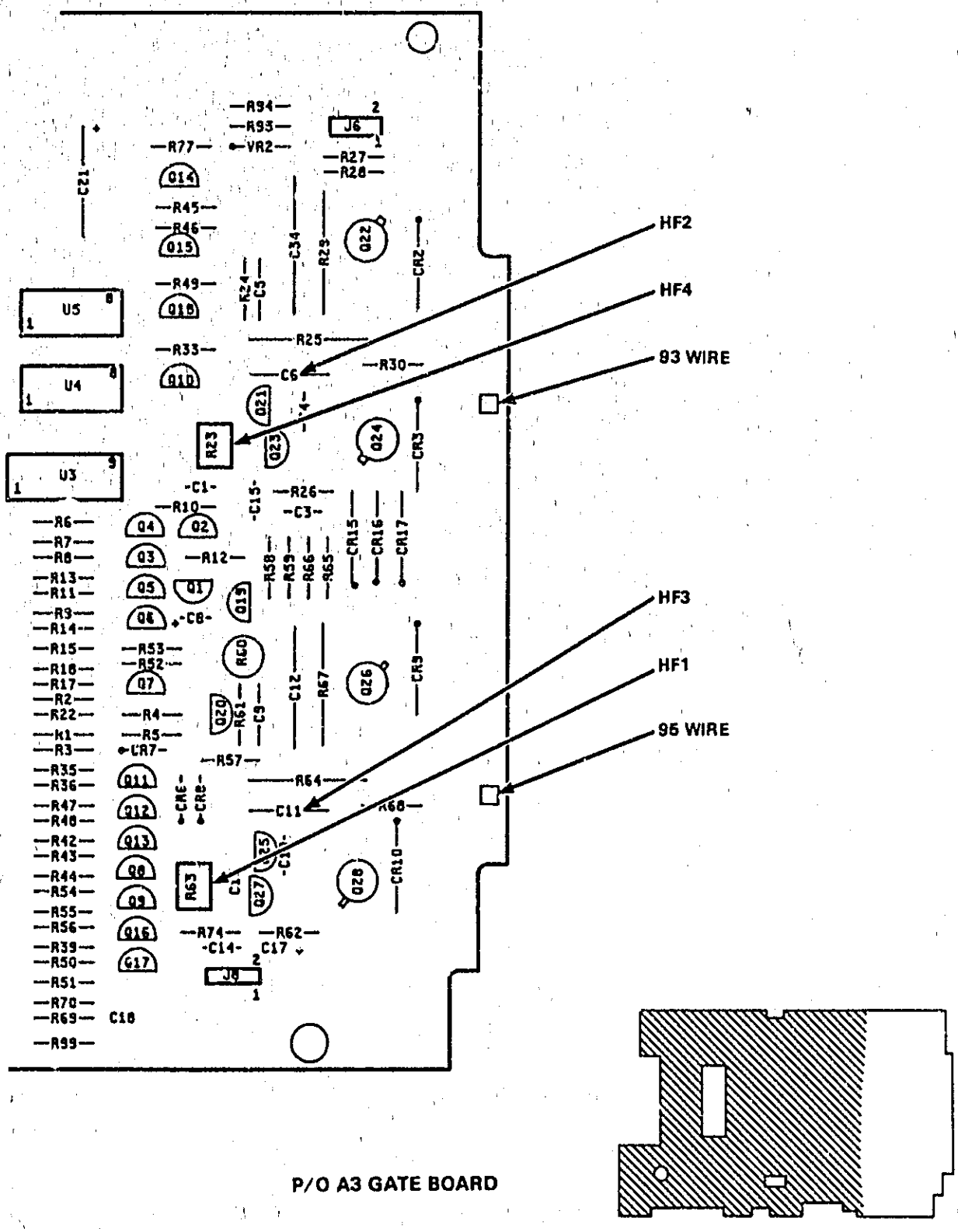


Figure 5-9. Gate and Dynamic Focus Pulse Adjustment and Wire Locations

ADJUSTMENTS

5-18. Focus Limit and Dynamic Focus Adjustments.

Reference:
Service Sheet 6.

Description:
Sets Focus Limit for optimum focus over entire CRT and sets range of dynamic focus for optimum at extreme deflection and high intensity drive.

Equipment:
None

Procedure:

a. Select 1 vs 2 mode by pressing [1], then [1vs2 MODE].

b. Select ground inputs for channels 1 and 2 by pressing both [GND] keys.

c. Select Bandwidth Limit by pressing [BW LIMIT].

d. Press [AUX CTRL] and rotate the Control Knob until a low intensity spot is visible (approximately `20` in LED display).

e. Alternately select [◄►1] (channel 1), then [◄►2] (channel 2) and rotate the Control Knob. Observe the spot in all four corners of display at least 1/2 major div inside outer graticule lines.

f. Move spot to quadrant where spot shape is most out of focus.

g. Set Front Panel Focus Control to center of its range.

h. Adjust FOCUS LIMIT (A2R24) and front panel ASTIG control for optimum focus of spot. Refer to figure 5-10 for adjustment location.

i. Press [CHAR ON-OFF] to turn characters on, then press [CHAR INTEN] and rotate the Control Knob for a reading of `CHAr 80` in LED display.

j. Adjust A3R60 (Dynamic Focus) for best possible focus of characters. Better focus will be obtained at lower CHAR INTEN levels. Refer to figure 5-10 for adjustment location.

ADJUSTMENTS

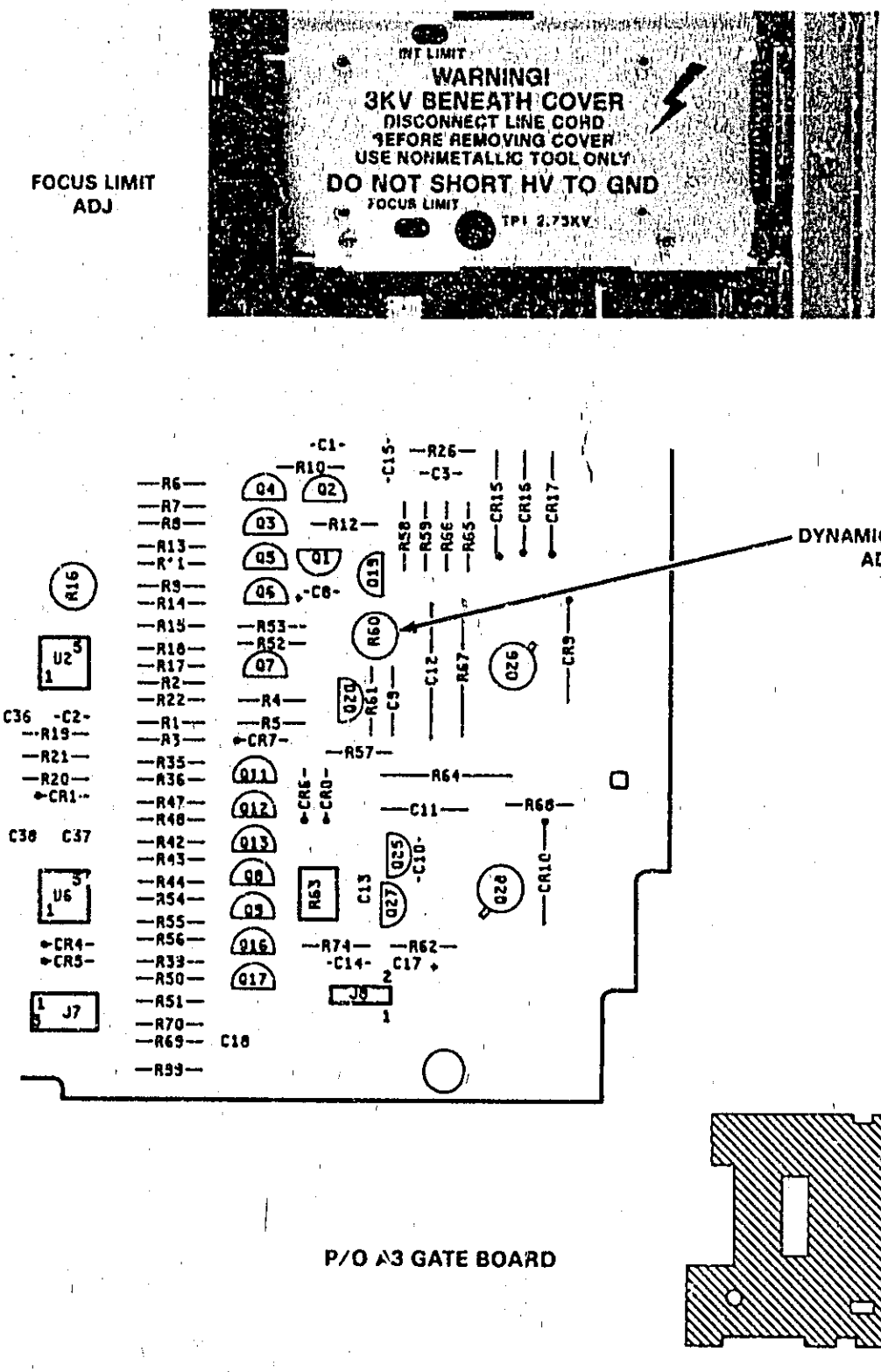


Figure 5-10. Focus Limit and Dynamic Focus Adjustment Locations

ADJUSTMENTS

5-19. Intensity Ratio Adjustment.

Reference:

Service Sheet 6.

Description:

Sets brightness of intensified portion of sweep.

Equipment:

None

Procedure:

a. Press AUTO-ECOPS.

b. Set main sweep speed to 500 nsec/div by rotating the Control Knob for a reading of 500. -9 in LED display.

c. Press INTEN.

d. Set delayed sweep speed to 50 nsec/div by pressing DELAY (delayed) and rotating the Control Knob for a reading of 50.0 -9 in LED display.

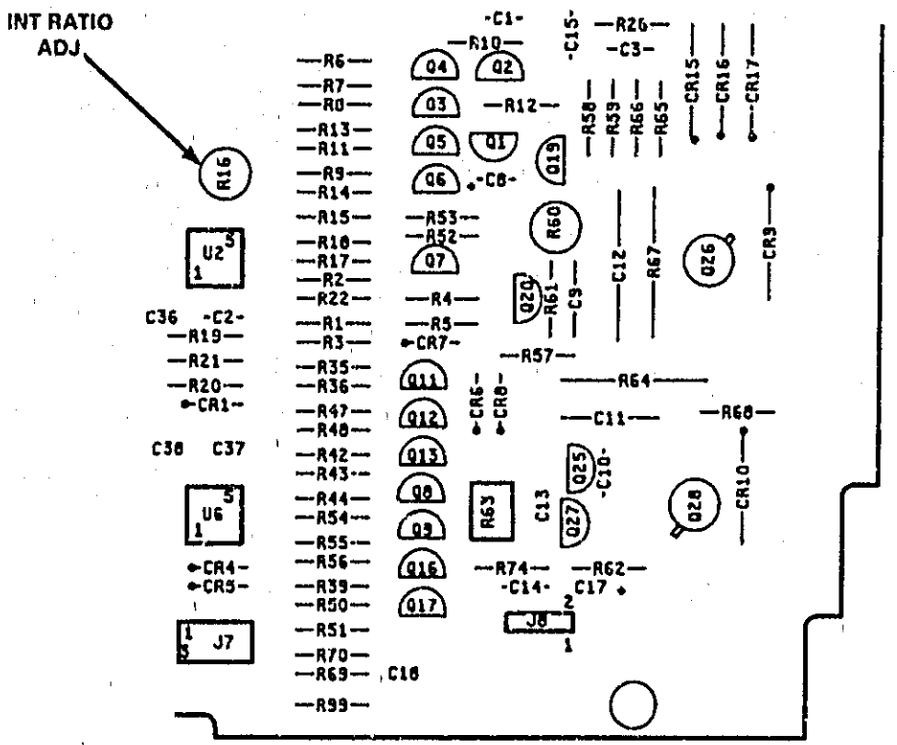
e. Set intensified portion of trace to approximately center screen by pressing DELAY key and rotating the Control Knob.

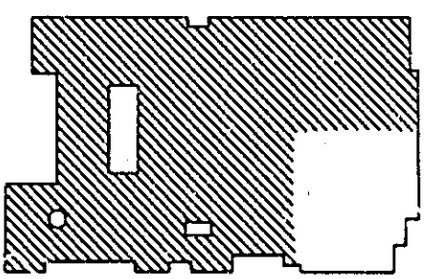
f. Set intensity for a reading of 15 in LED display by pressing and rotating the Control Knob.

g. Adjust INT RATIO (A3R16) to just extinguish intensified portion of trace. (This adjustment may be altered as desired for user preference or application.) Refer to figure 5-11 for adjustment location.

ADJUSTMENTS

5





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Figure 5-11. Intensity Ratio Adjustment Location

ADJUSTMENTS

5-20. Main and Delayed Sweep Gate Adjustments.

Reference:

Service Sheet 12.

Description:

Adjusts pulse width of Main and Delayed Sweep Gate pulses.

Equipment:

Oscilloscope ..... HP Model 1740A
Oscilloscope Probe ..... HP Model 10041A

Procedure:

a Press AUTO SCOPE.

b. Set main sweep speed to 20 nsec/div by rotating the Control Knob for a reading of 20.0 -9 in LED display.

c. Select intensified sweep mode by pressing INTEN.

d. Set delayed sweep speed to 20 nsec/div by pressing DSG (delayed) and rotating the Control Knob for a reading of 20.0 -9 in LED display.

e. Set monitor oscilloscope input to DC coupling and volts/division to 0.05 V.

f. Using monitor oscilloscope and probe, observe the waveform at A5U8 pin 10.

g. Adjust MSG (A5R100) for minimum width pulse and note level of baseline. Readjust MSG (A5R100) for maximum pulse width attainable while baseline shift does not exceed 100 mV. Refer to figure 5-12 for adjustment location.

h. Move monitor oscilloscope probe to observe waveform at A5U11 pin 10.

i. Adjust DSG (A5R111) for minimum width pulse and note baseline. Then adjust DSG (A5R111) for maximum pulse width with no more than 100 mV shift in baseline. Refer to figure 5-12 for adjustment location.

ADJUSTMENTS

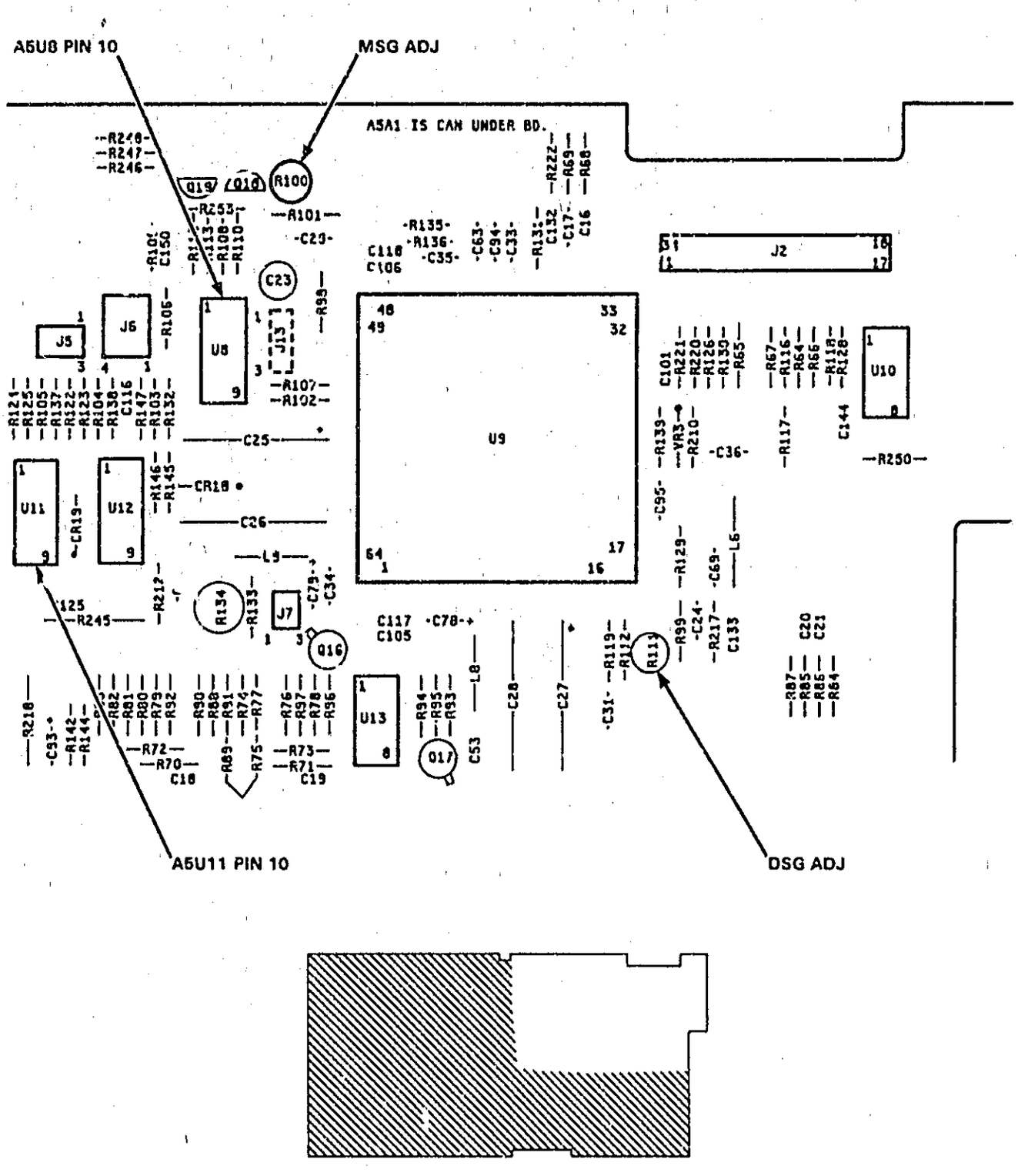


Figure 5-12. Main and Delayed Sweep Gate Adjustment Locations

ADJUSTMENTS

5-21. Sweep Length Adjustment.

Reference:

Service Sheet 13.

Description:

Adjusts length of sweep for 11 horizontal divisions.

Equipment:

None

Procedure:

a. Press AUTO-SCOPE.

b. Set sweep speed to 100 µsec/div by rotating the Control Knob for a reading of [100. -6] in LED display.

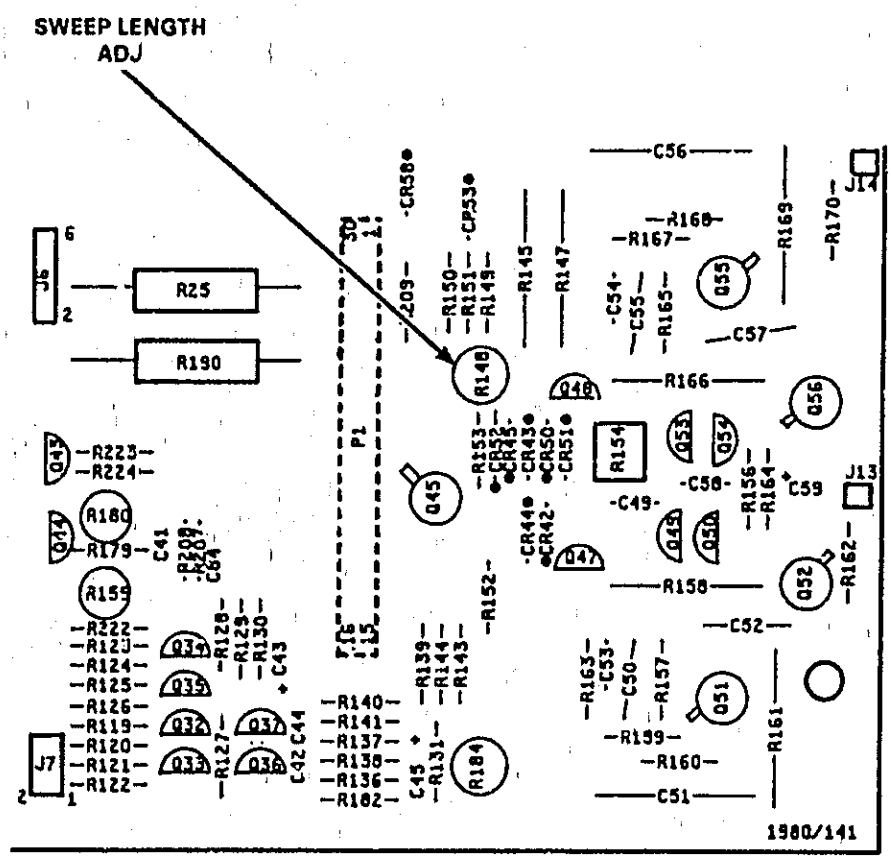
c. Select horizontal position by pressing ◄ ► key.

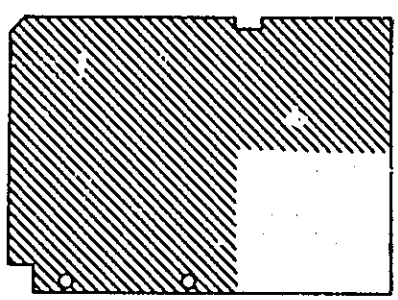
d. Adjust A1R148 (Sweep Length) for a sweep length of 10 divisions. (Rotate the Control Knob to position sweep.) Refer to figure 5-13 for adjustment location.

e. Position left end of sweep 1/2 major division to right of left graticule.

f. Readjust A1R148 (Sweep Length) to bring start of sweep back to left graticule.

ADJUSTMENTS





P/O A1 LVPS BOARD

Figure 5-13. Sweep Length Adjustment Location

ADJUSTMENTS

5-22. Sweep Start Adjustment.

Reference:

Service Sheet 12.

Description:

Adjusts Main sweep and Delayed sweep to start at same point.

Equipment:

None

Procedure:

a. Press AUTO-SCOPE.

b. Set main sweep speed to 10 µsec/div by rotating the Control Knob for a reading of [10.0 -6] in LED display.

c. Select Dual time mode by pressing DUAL.

d. Set delayed sweep speed to 10 µsec/div by pressing (delayed) and rotating the Control Knob for a reading of [10.0 -6] in LED display.

e. Separate sweeps vertically, if necessary, using dual separation. Press , then and rotate the Control Knob for desired separation.

f. Adjust SWP ST (A5R134) so both sweeps start at the same time. (Use a graticule line to aid adjustment.) Refer to figure 5-14 for adjustment location.

ADJUSTMENTS

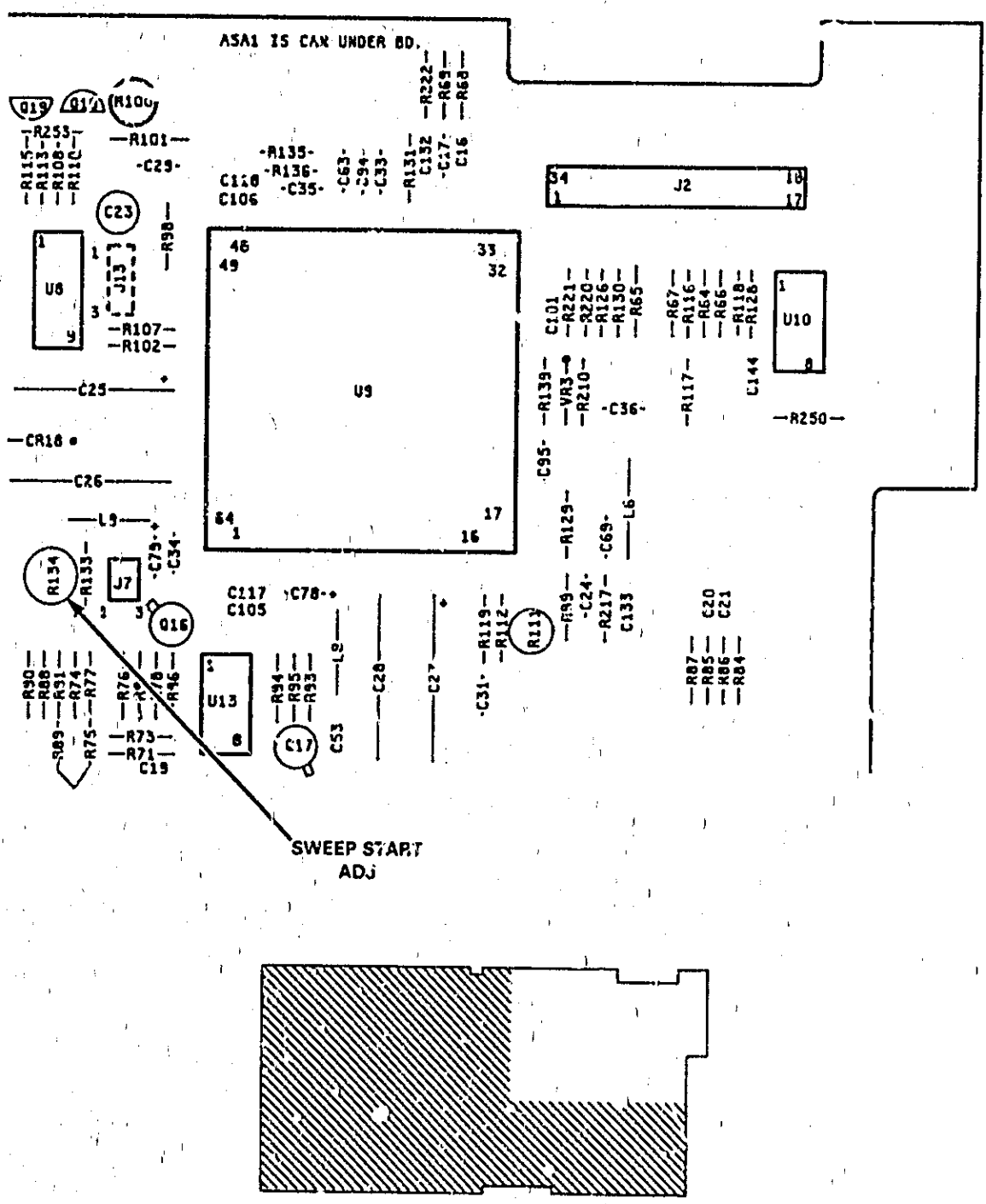


Figure 5-14. Sweep Start Adjustment Location

ADJUSTMENTS

5-23. Plate Average Adjustment.

Reference:

Service Sheet 13.

Description:

Adjusts average potential on horizontal deflection plates to +43 volts.

Equipment:

Digital Voltmeter (DVM) ..... HP Model 3465A

Procedure:

a. Select 1 vs 2 mode by pressing , then .

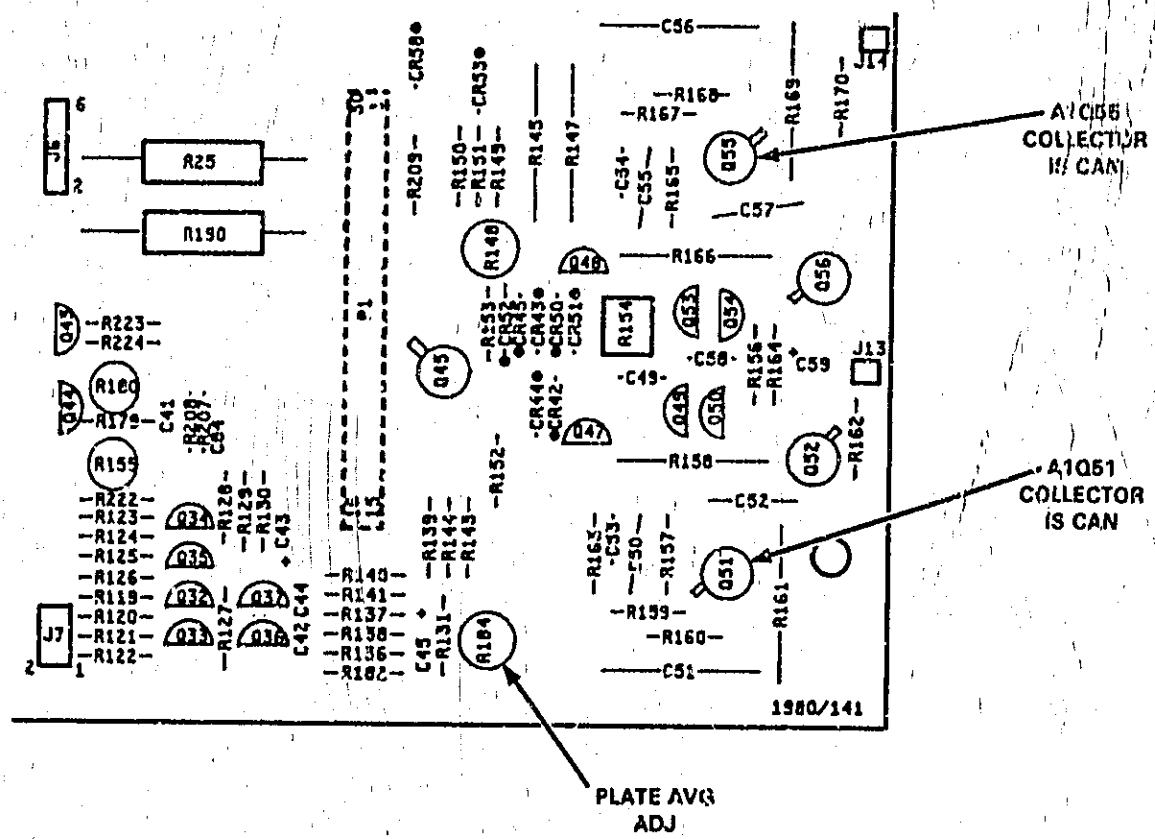
b. Center low intensity spot horizontally on CRT by pressing (channel 2) and rotating the Control Knob.

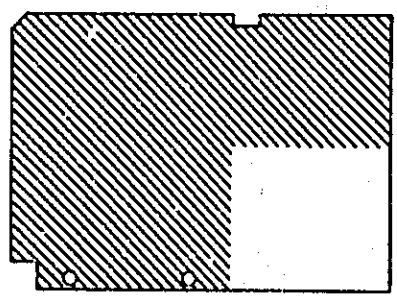
c. Set characters to off by pressing .

d. Using DVM, measure voltage at collectors of A1Q51 and A1Q55. Rotate the Control Knob until the voltages are approximately equal.

e. Adjust PLATE AVG (A1R184) so that the average of the two voltages is +43 V. Refer to figure 5-15 for adjustment location.

ADJUSTMENTS





P/O A1 LVPS BOARD

Figure 5-15. Plate Average Test Point and Adjustment Locations

ADJUSTMENTS

5-24. Vertical Gain Adjustment.

Reference:

Service Sheet 9.

Description:

Centers gain for a given amplifier/CRT combination. Gain will be refined for all ranges in the "Front Panel" calibration routine. This adjustment need only be made after the CRT or a major board assembly has been replaced.

Equipment:

Digital Voltmeter (DVM) ..... HP Model 3465A
Peak - Peak Source ..... Ballantine 6125B

Procedure:

a. Select V vs T mode and channel 1 by pressing [VIEW], then [CH 1].

b. Set channel 1 volts/division to 100 mV by pressing [CH 1] (channel 1) and rotating the Control Knob for a reading of [100. -3] in LED display.

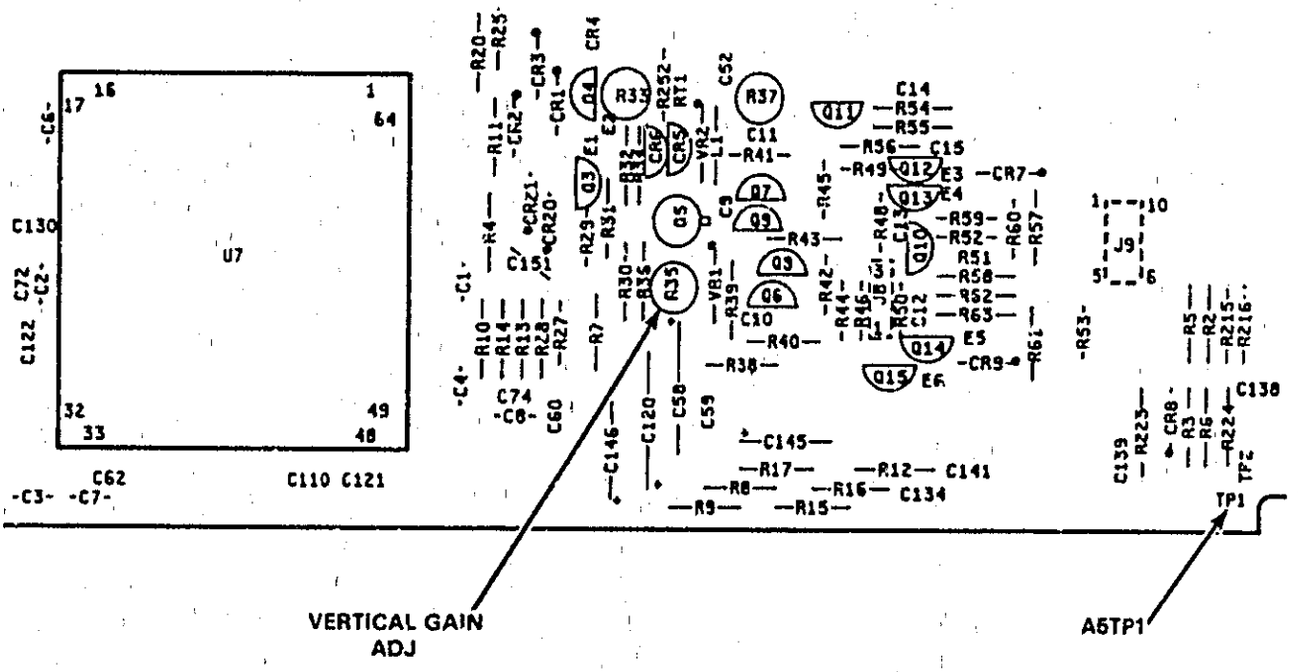
c. Monitor A5TP1 with DVM and rotate the Control Knob for a reading of 140 mV on DVM. Refer to figure 5-16 for test point location.

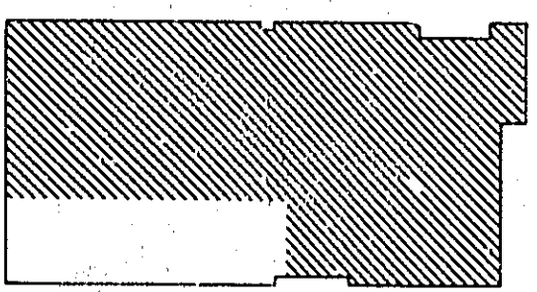
Note

If 140 mV cannot be attained at TP1, enter the Front Panel Cal routine and complete procedure as follows: Press [OPTION MENU], CALIBRATE & UTILITIES, FRONT PANEL CAL 1980A/B then NEXT SEQUENCE (three times) until CH1 SENSITIVITY is displayed. Press RANGE STEP (two times) until [100. -3] is displayed in LED display. Repeat step c of this procedure and complete steps d and e. After completion of step e, press [OPTION MENU] and continue calibration as necessary.

d. With signal source apply a 1 V peak-peak signal to channel 1 input.

e. Adjust GAIN (A5R35) for 10 cm of deflection. Refer to figure 5-16 for adjustment location.





P/O A5 SCOPE BOARD

Figure 5-16. Vertical Gain Test Point and Adjustment Location

ADJUSTMENTS

5-25. OSC Adjustment.

Reference:

Service Sheet 18.

Description:

The Osc adjustment on processor board is adjusted for a frequency of 3.333333 MHz.

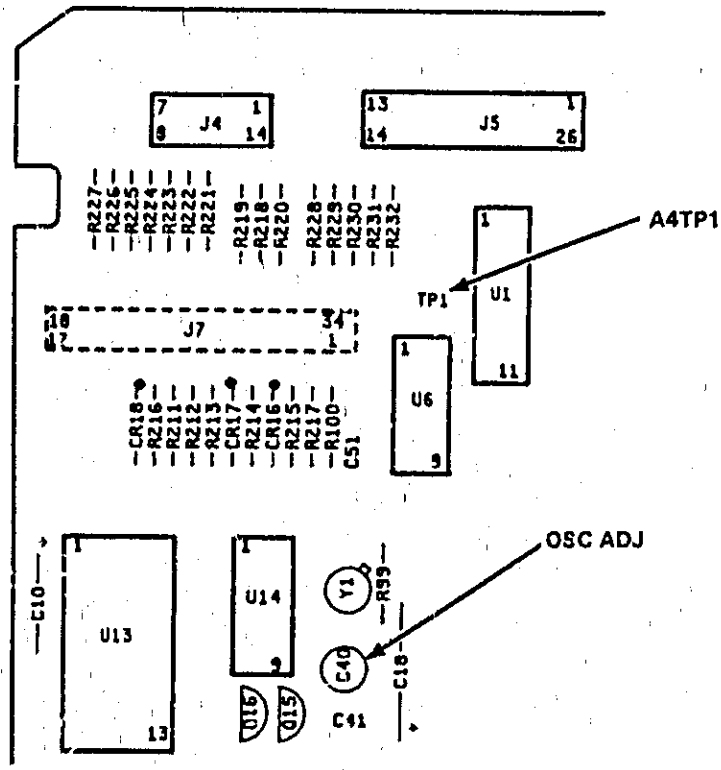
Equipment:

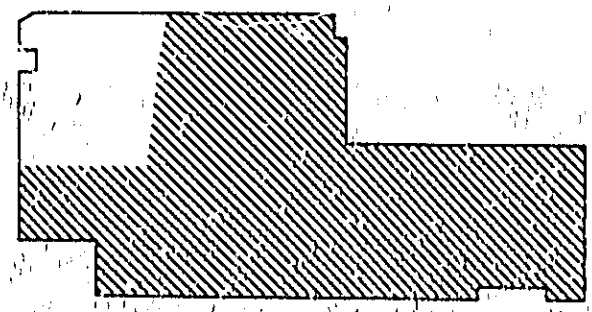
Frequency Counter ..... HP Model 5382A
Nonmetallic adjustment tool

Procedure:

a. Connect frequency counter input to A4TP1, Refer to figure 5-17 for test point location.

b. Using the nonmetallic adjustment tool, adjust OSC ADJ (A4C40) for a frequency of 3.333333 MHz ±10 Hz Refer to figure 5-17 for adjustment location.





P/O A4 PROCESSOR BOARD

Figure 5-17. OSC Test Point and Adjustment Location

ADJUSTMENTS

5-26. VCO Calibration Adjustment.

Reference:

Service Sheet 12.

Description:

The VCO is manually adjusted for minimum reading on LED display, then automatically adjusted under processor control.

Equipment:

Nonmetallic adjustment tool.

Procedure:

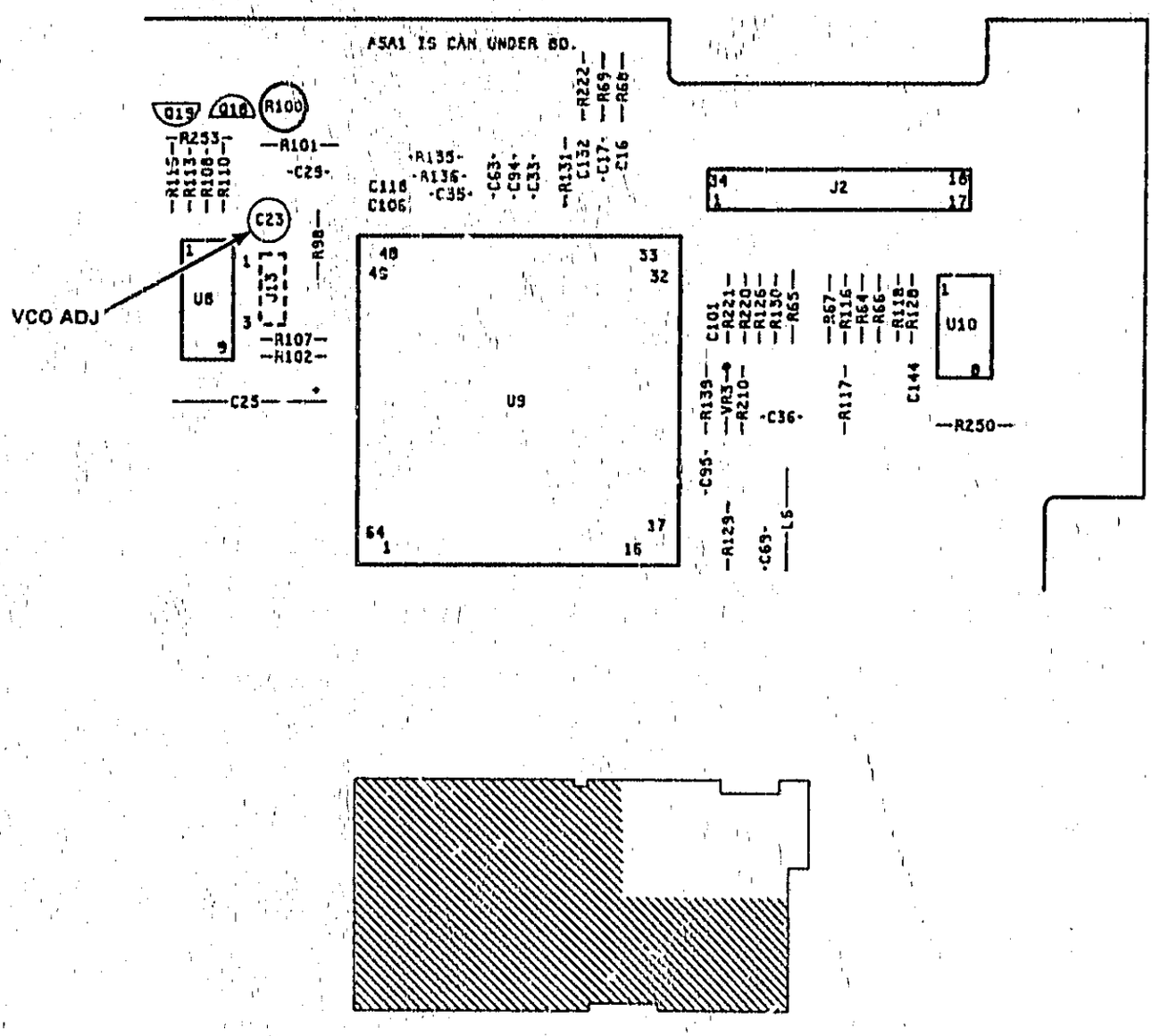
a. Press OPTION (MENU).

b. Press Soft Keys in the following sequence:
   1. CALIBRATE AND UTILITIES
   2. UTILITIES
   3. INT ADJ DELAY OSC RANGE

c. Adjust VCO ADJ (A5C23) for minimum reading on LED display. (Use nonmetallic tool. Reading must be adjusted to [200] or less.) Refer to figure 5-18 for adjustment location.

d. Press PREVIOUS MENU key. Internal VCO calibration will then be completed accurately and automatically.

ADJUSTMENTS



P/O A5 SCOPE BOARD

Figure 5-18. VCO Adjustment Location

ADJUSTMENTS

5-27. Sync, Main and Delayed Trigger View Adjustments.

Reference:

Service Sheet 15.

Description:

Adjusts Sync, Main and Delayed Trigger View signals to trigger on the center horizontal graticule.

Equipment:

Function Generator ..... HP Model 3310A

Procedure:

a. Press AUTO-SCOPE (MEASURE).

b. Position channel 1 trace to center graticule by pressing (channel 1) and rotating the Control Knob.

c. Select channel 1 + channel 2 operation by pressing key.

d. Position trace to center graticule by pressing (channel 2) and rotating the Control Knob.

e. Select channel 2 operation by pressing .

f. Adjust SYNC (A5R33) to position trace to center graticule.

g. Apply a 50 kHz, 10 volt peak to peak signal from oscillator to channel 1 input and press AUTO-SCOPE (MEASURE).

h. Set channel 1 volts/division to 1 v/div by pressing (channel 1) and rotating the Control Knob for a reading of 1.0 in LED display.

i. Select main trigger view by pressing , then (main).

j. Set channel 1 to off by pressing the .

k. Adjust MT VU ADJ (A5R171) to balance sweep starts between positive and negative slopes about center, horizontal graticule. Toggle . Refer to figure 5-19 for adjustment location.

l. Select delayed by pressing .

m. Select delayed trigger view by pressing , then (delayed).

n. Select triggered mode by pressing key.

o. Adjust DT VU ADJ (A5R187) to balance sweep starts between positive and negative slopes about center, horizontal graticule. Toggle . Refer to figure 5-19 for adjustment location. (User may desire to set SEC/DIV (DLY'D) to view 1 or more complete cycles.)

ADJUSTMENTS

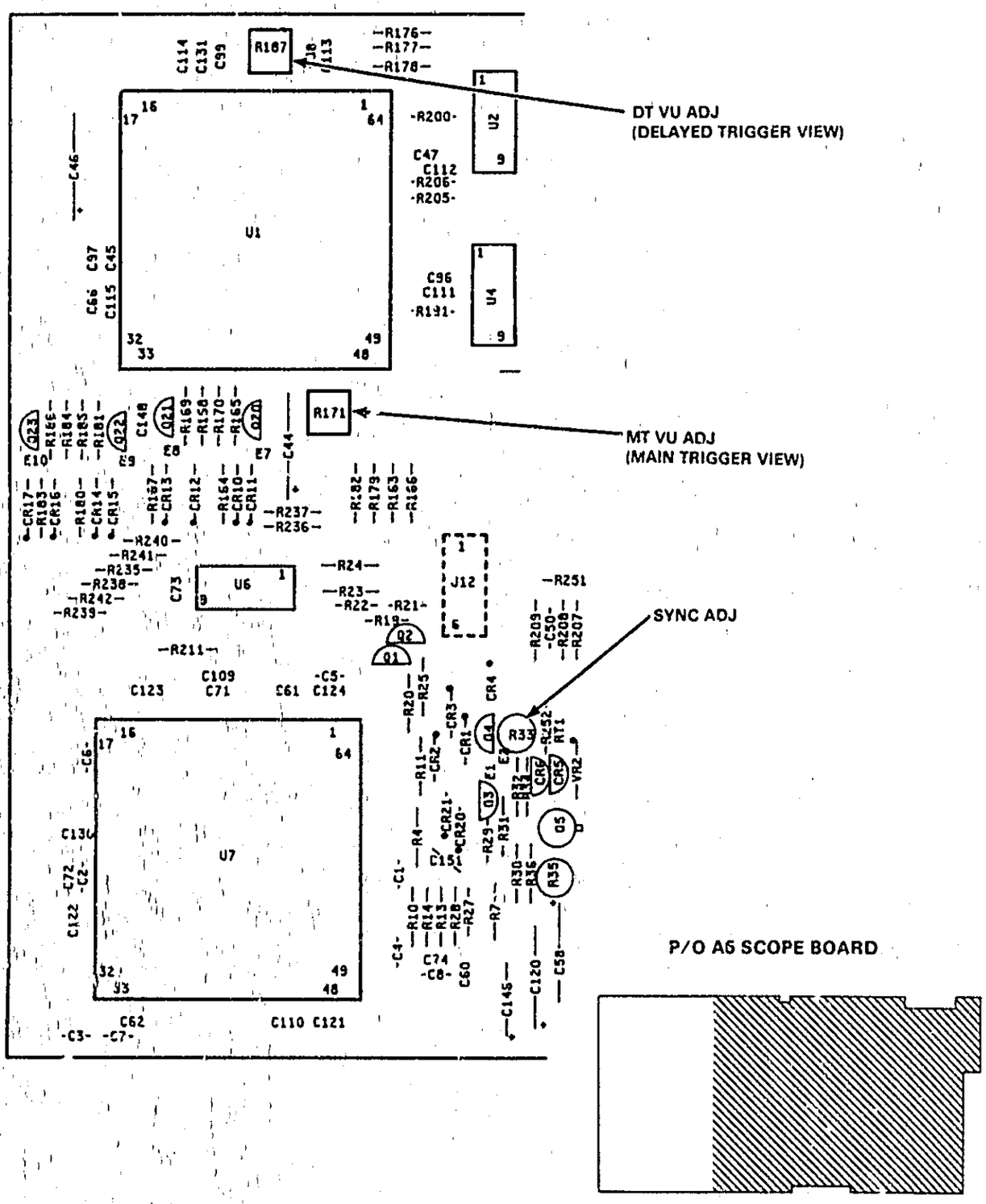


Figure 5-19. Sync, Main and Delayed Trigger View Adjustment Locations

5-28. Front Panel Calibration Without Sweep Linearity Adjustment.

Reference:

None

Description:

Using operator setups, instrument automatically selects and stores in memory a number of Calibration Factors.

Equipment:

None

Procedure:

a. Place rear panel "Cal" switch in "Unprotected" position.

b. Press OPTION MENU.

Note

Soft Key labels are displayed on CRT after OPTION MENU is pressed.

c. Press Soft Keys in the following sequence:
   1. CALIBRATE & UTILITIES
   2. FRONT PANEL CAL 1980A/B

d. Proceed through internal calibration routine as instructed by messages displayed on CRT.

Note

During the Front Panel Calibration routine error codes may be generated. The error codes are displayed on the CRT in inverse video and indicate what area of the Cal routine failed. Refer to table 5-4 for error codes and a brief description.

Note

If an external timing source is to be used for Main and Delayed Sweep calibration, EXT TIME MARK must be selected during the Front Panel Calibration routine. It may be necessary to adjust the volts/division, vertical position, and trigger level for a stable display.

e. When Front Panel Calibration routine is complete place rear panel "Cal" switch to the "Protected" position.

Note

Calibration routine must be completed and the message CAL MEMORY NOT PROTECTED must be received prior to placing the Protected-Unprotected switch in the protected position. If the switch is placed in the protected position without receiving this message, the front panel will be locked out.

ADJUSTMENTS

5-29. Front Panel Calibration With Sweep Linearity Adjustment.

Reference:

Service Sheet 13.

Description:

The sweep linearity adjustments match the horizontal output amplifier to a specific CRT load. Once they have been adjusted they need not be readjusted unless CRT or Scope Board Assembly (A5) has been replaced.

Equipment:

Time Mark Generator ..... Ballantine 61258

Procedure:

a. Place rear panel "Cal" switch in "Unprotected" position.

b. Press OPTION MENU.

Note

Soft key labels are displayed on CRT after OPTION MENU is pressed.

c. Press Soft Keys in the following sequence:
   1. CALIBRATE & UTILITIES
   2. FRONT PANEL CAL 1980A/B

d. Proceed through internal calibration routine as instructed by messages displayed on CRT up to beginning of Main Sweep Timing.

Note

During the Front Panel Calibration routine error codes may be generated. The error codes are displayed on the CRT in inverse video and indicate what area of the Cal routine failed. Refer to table 5-4 for error codes and a brief description.

e. Apply a 200 MHz (5 ns) signal, from time mark generator, to channel 1 input and select EXT source by pressing EXT INT TIME MARK.

f. Adjust channel 1 volts/division, trigger level, and intensity to obtain a suitable display.

g. Press MAIN DLY (main) and rotate the Control Knob to set timing as close as possible.

Note

Press DELAY TIME and rotate the Control Knob to align time marks on graticule lines as necessary.

h. Adjust HF8 (A1R154) 10 ns linearity adj for most even distribution over the full 10 divisions. Refer to figure 5-20 for adjustment location.

i. Adjust HF6 (A1C57) and HF7 (A1C52) 5 ns linearity adj in equal increments for best overall linearity. Refer to figure 5-20 for adjustment locations.

ADJUSTMENTS

Note

HF6 and HF7 slugs must be equally extented.

j. Refine timing and linearity adjustments for the best timing and linearity over full display. (Remember the specifications call for only 3% timing accuracy from the second to the tenth graticule.)

Note

It may be necessary to restart sequance in order to refine timing.

k. Place instrument cover tightly over horizontal amplifier and check effect on linearity. Remove cover and refine linearity adjustments to compensate for error introduced by instrument cover.

l. Complete remainder of Front Panel Calibration routine.

m. When Front Panel Calibration routine is complete place rear panel "Cal" switch to the "Protected" position.

Note

Calibration routine must be completed and the message CAL MEMORY NOT PROTECTED must be received prior to placing the Protected-Unprotected switch in the protected position. The switch is placed in the protected position without receiving this message, the front panel will be locked out.

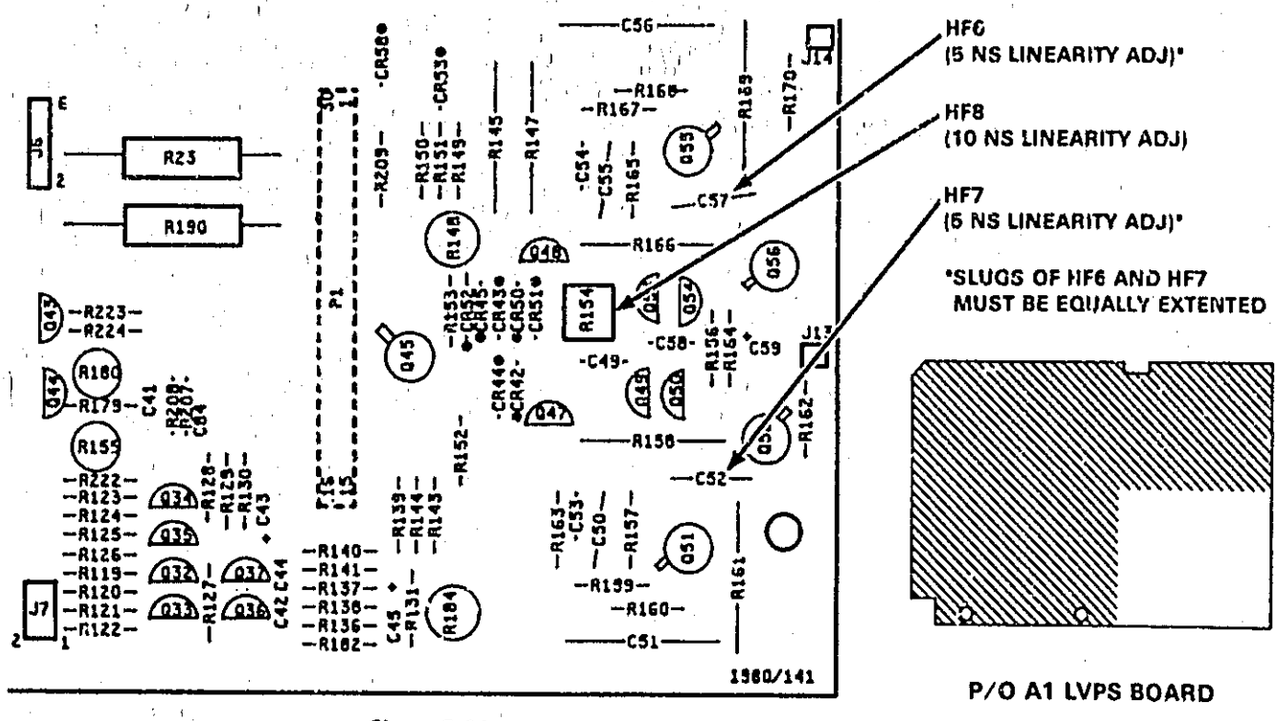


Figure 5-20. Sweep Linearity Adjustment Locations

ADJUSTMENTS

5-30. 1 vs 2 Gain Adjustment.

Reference:

Service Sheet 13.

Description:

Adjusts the 1 vs 2 Gain to cause a given signal amplitude to have the same divisions of deflection in the vertical and horizontal.

Equipment:

Peak to Peak Source ..... Ballatine 6126B

Procedure:

a. Apply a 1 V peak to peak signal from peak to peak source to channel 2 input.

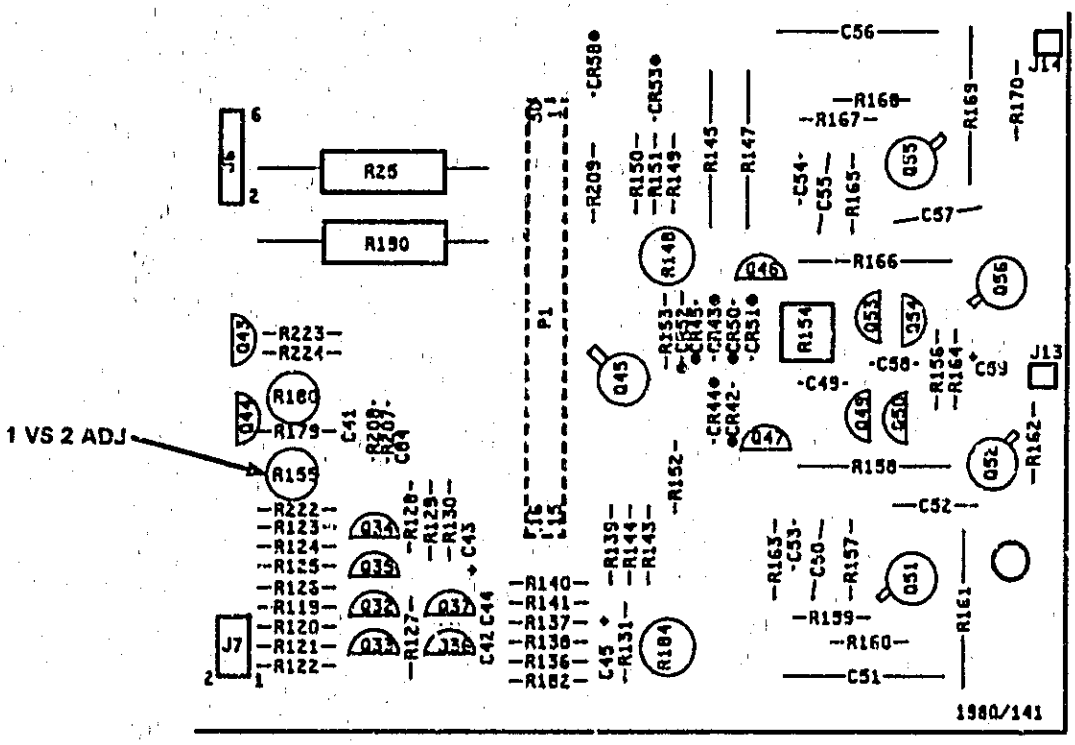
b. Press AUTO SCORE.

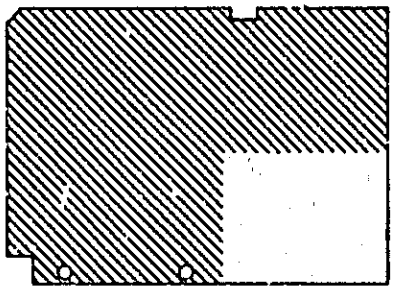
c. Set channel 2 volts/division to 100 mV by pressing V/div and rotating the Control Knob for a reading of [100. -3] in LED display.

d. Display should be 10 divisions.

e. Select 1 vs 2 mode by pressing [ ], then [ ].

f. Adjust 1vs2 (A1R155) for the deflection noted in step d. Refer to figure 5-21 for adjustment location.





P/O A1 LVPS BOARD

Figure 5-21. 1 vs 2 Adjustment Location

ADJUSTMENTS

5-31. Input Compensation Adjustments.

Reference:

Service Sheets 8, 14.

Equipment:

Square Wave Generator ..... Ballantine 6125B

Procedure:

a. Apply a 10 kHz square wave to channel 1 input and press AUTO • SCOPE.

b. Set channel 1 to 100 mV/div by pressing VOLTS/DIV (channel 1) key and rotating the Control Knob for a reading of 100. -3 in LED display.

c. Adjust square wave generator amplitude for approximately 9 divisions.

d. Set sweep speed for a display of 3 to 4 cycles by pressing SEC/DIV (main) and rotating the Control Knob.

e. Adjust 100 mV COMP (A13A1C4) for best square wave. Refer to figure 5-22 for adjustment location.

f. Change channel 1 sensitivity to 1 V/div by pressing VOLTS/DIV (channel 1) and rotating the Control Knob for a reading of 1.00 in LED display.

g. Increase square wave amplitude for 9 divisions of deflection.

h. Adjust 1 V COMP (CH1) (A13A1C5) for best square wave. Refer to figure 5-22 for adjustment location.

i. Select channel 2 by pressing 2 mV, and change internal trigger to channel 2 by pressing INT, then 2 mV.

j. Set channel 2 for 100 mV/div by pressing VOLTS/DIV (channel 2) and rotating the Control Knob for a reading of 100. -3 in LED display.

k. Apply a 10 kHz square wave to channel 2 input and adjust amplitude for approximately 9 divisions.

l. Adjust 100 mV COMP (A13A1C16) for best square wave. Refer to figure 5-22 for adjustment location.

m. Change channel 2 sensitivity to 1 V/div by pressing VOLTS/DIV (channel 2) and rotating the Control Knob for a reading of 1.00 in LED display.

n. Increase square wave amplitude for 9 divisions of deflection.

o. Adjust 1 V COMP (CH2) (A13A1C18) for best square wave.

p. Remove square wave input from channel 2 and apply it to Main EXT input.

q. Select EXT÷10 and Main Trigger View by pressing EXT÷10, then ▮, then MAIN (main).

ADJUSTMENTS

r. Set square wave generator for a signal amplitude of 9 divisions.

s. Adjust ÷10 COMP (MAIN) (A14A1C3) for best square wave. Refer to figure 5-22 for adjustment location.

t. Select EXT÷10 and Delayed by pressing (delayed) and .

u. Select delayed trigger view by pressing , then .

v. Remove signal from EXT (main) input and apply to EXT (delayed) input.

w. Set delayed sec/div to view 3 or 4 cycles by pressing (delayed) and rotating the Control Knob.

x Set function generator for a signal amplitude of 9 divisions.

y. Adjust ÷10 COMP (DLY'D) (A14A1C13) for best square wave. Refer to figure 5-22 for adjustment location.

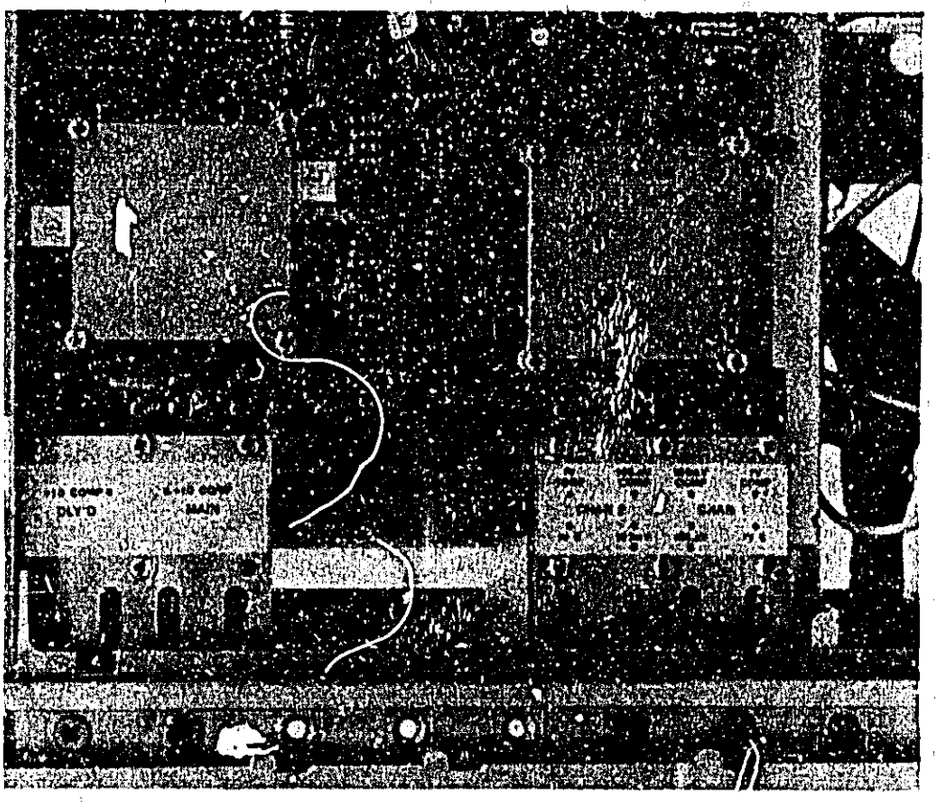


Figure 5-22. Input Comp Adjustment Locations

5-32. Input Capacitance Adjustments.

Reference:

Service Sheet 8.

Description:

Adjusts input capacitance of ÷10 and ÷100 attenuators to equal input capacitance of ÷1 range.

Equipment:

LCR Meter ..... HP Model 4332A

Procedure:

a. Select channel 1 by pressing [CH 1].

b. Set channel 1 volts/division to 10 mV by pressing [CH 1] (channel 1) key and rotating the Control Knob for a reading of [10.0 -3] in LED display.

c. Connect LCR Meter to channel 1 input and note reading.

d. Change channel 1 volts/division to 100 mV by rotating the Control Knob for a reading of [100. -3] in LED display.

e. Adjust 100 mV C (CH1) (A13A1C3) for same reading on LCR meter as noted in step c. Refer to figure 5-23 for adjustment location.

f. Change channel 1 volts/division to 1 V by rotating the Control Knob for a reading of [1.00] in LED display.

g. Adjust 1 V C (CH1) (A13A1C5) for same reading on LCR Meter noted in step c. Refer to figure 5-23 for adjustment location.

h. Recheck and readjust 100 mV C if necessary.

i. Select channel 2 by pressing [CH 2].

j. Set channel 2 volts/division to 10 mV by pressing [CH 2] (channel 2) key and rotating the Control Knob for a reading of [10.0 -3] in LED display.

k. Connect LCR Meter to channel 2 input and note reading.

l. Change channel 2 volts/division to 100 mV by rotating the Control Knob for a reading of [100. -3] in LED display.

m. Adjust 100 mV C (channel 2) (A13A1C15) for same reading on LCR meter as noted in step j. Refer to figure 5-23 for adjustment location.

ADJUSTMENTS

n. Change channel 2 volts/division to 1 V by rotating the Control Knob for a reading of 100 in LED display.

o. Adjust 1 V C (CH2) (A13A1C17) for same reading on LCR Meter noted in step j. Refer to figure 5-23 for adjustment location.

p. Recheck and readjust 100 mV C if required.

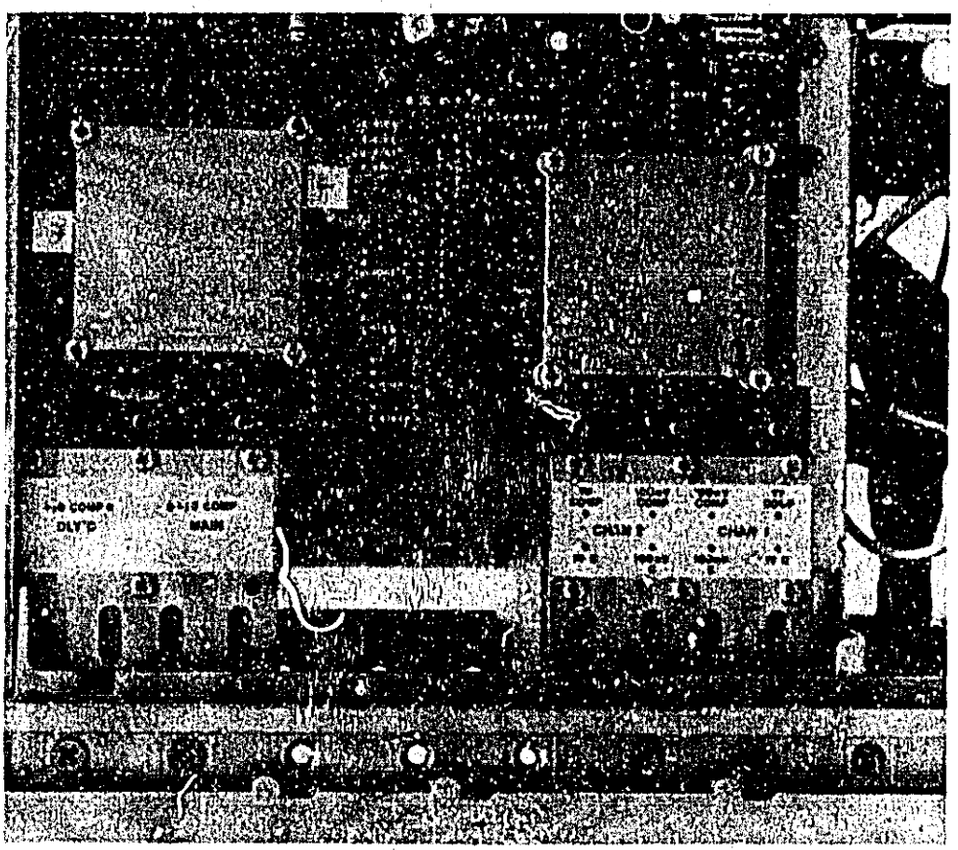


Figure 5-23. Input Capacitance Adjustments

ADJUSTMENTS

5-33. Risetime, Bandwidth, and Overshoot Adjustments.

Reference:

Service Sheets 9, 10.

Description:

Adjusts for a risetime of <3.5 nsec and overshoot of <4% to assure a bandwidth of >100 MHz consistent with proper amplifier response. These adjustments primarily match the vertical amplifier output to a specific CRT load, therefore they need only be made after the CRT has been replaced, however, should the bandwidth become marginal these adjustments may be made to correct for component aging.

Equipment:

Pulse Generator ..... Ballantine 6125B

Procedure:

a. Apply an approximate 100 kHz fast rise pulse from pulse generator to channel 1 input.

b. Press AUTO-SCOPE.

c. Select 50 ohm DC coupling by pressing CH 1, then DC (channel 1).

d. Press VOLTS/DIV (channel 1).

e. Adjust channel 1 volts/division and pulse amplitude for a 5 division display.

f. Adjust HF1 (A5R37) for best pulse shape. Refer to figure 5-24 for adjustment location.

g. Adjust HF1 (A1R55); HF2 (A1R50); HF3 (A1R49); HF4 (A1C27); and HF5 (A1R56) for fastest risetime, best corners, and flattest pulse top.

ADJUSTMENTS

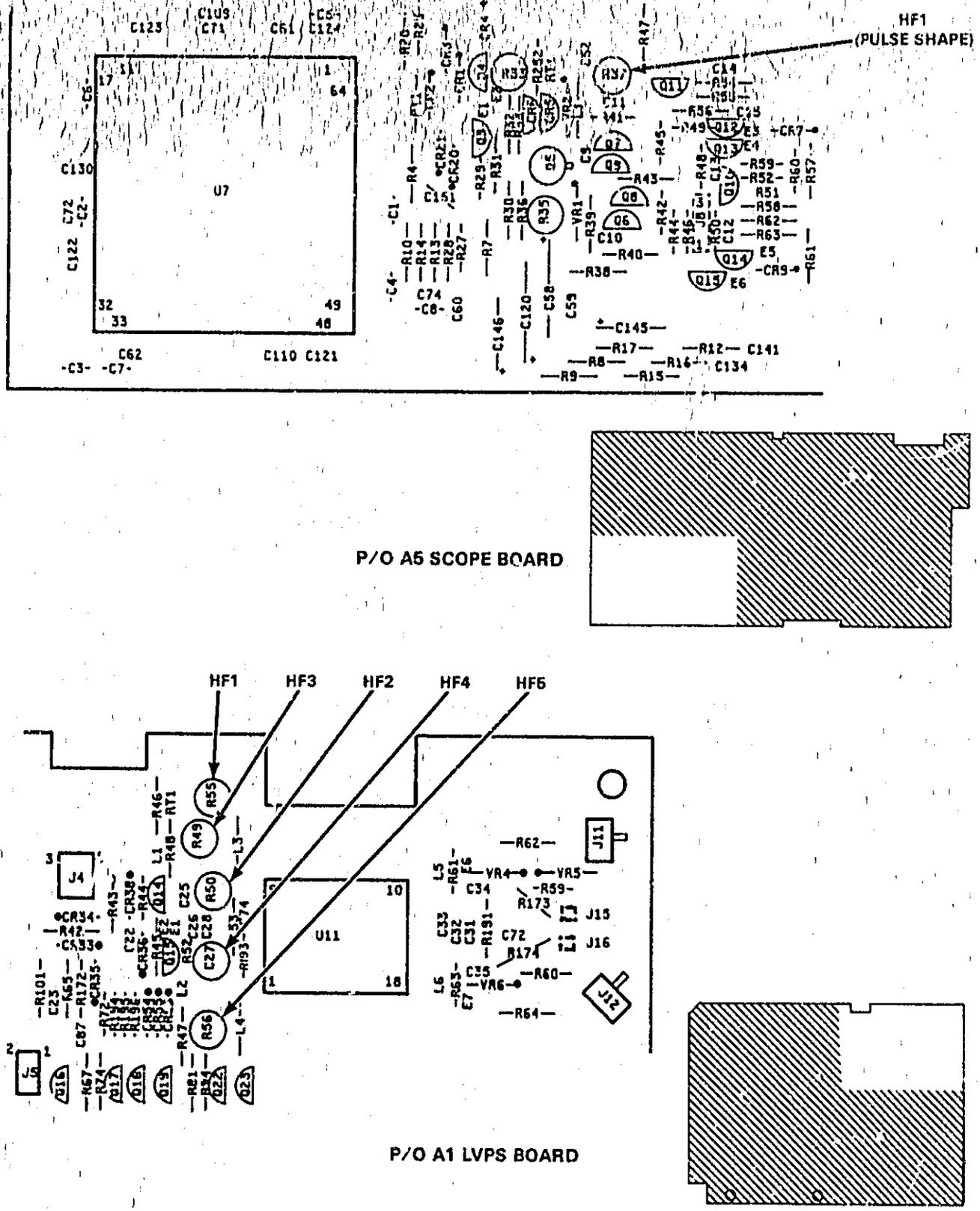


Figure 5-24. Risetime and Overshoot Adjustment Locations

Table 5-4. Front Panel Calibration Error Codes

Cal Factor Error	Error Description	Cal Factor Error	Error Description
10	Channel 1 Position Error	58	Delayed Sweep Error — 100 ms Range
11	Channel 1 Position Error	59	Delayed Sweep Error — 10 ms Range
12	Channel 1 Position Error	60	Delayed Sweep Error — 1 ms Range
13	Channel 2 Position Error	61	Delayed Sweep Error — 100 µs Range
14	Channel 2 Position Error	62	Delayed Sweep Error — 10 µs Range
15	Channel 2 Position Error	63	Delayed Sweep Error — 1 µs Range
16	Horizontal Position Error	64	Delayed Sweep Error — 100 ns Range
17	Horizontal Position Error	65	Delayed Sweep Error — 10 ns Range
		66	Delayed Sweep Error — 5 ns Range
20	Channel 1 Gain Error — 1 V Range	67	Delayed Sweep Error — 100 ms Range
21	Channel 1 Gain Error — 100 mV Range	68	Delayed Sweep Error — 10 ms Range
22	Channel 1 Gain Error — 10 mV Range	69	Delayed Sweep Error — 1 ms Range
23	Channel 1 Gain Error — 2 mV Range	70	Delayed Sweep Error — 100 µs Range
24	Channel 1 Gain Error — 1 V Range	71	Delayed Sweep Error — 10 µs Range
25	Channel 1 Gain Error — 100 mV Range	72	Delayed Sweep Error — 1 µs Range
26	Channel 1 Gain Error — 10 mV Range	73	Delayed Sweep Error — 100 ns Range
27	Channel 1 Gain Error — 2 mV Range	74	Delayed Sweep Error — 10 ns Range
		75	Delayed Sweep Error — 5 ns Range
28	Channel 2 Gain Error — 1 V Range		
29	Channel 2 Gain Error — 100 mV Range		
30	Channel 2 Gain Error — 10 mV Range	76	Main Trigger Level Error — AC
31	Channel 2 Gain Error — 2 mV Range	77	Main Trigger Level Error — EXT DC
32	Channel 2 Gain Error — 1 V Range	78	Main Trigger Level Error — CH1 DC
33	Channel 2 Gain Error — 100 mV Range	79	Main Trigger Level Error — CH2 DC
34	Channel 2 Gain Error — 10 mV Range	80	Main Trigger Level Error
35	Channel 2 Gain Error — 2 mV Range		
36	Delay Time Error	81	Delayed Trigger Level Error — AC
37	Delay Time Error	82	Delayed Trigger Level Error — EXT DC
		83	Delayed Trigger Level Error — CH1 DC
40	Main Sweep Error — 100 ms Range	84	Delayed Trigger Level Error — CH2 DC
41	Main Sweep Error — 10 ms Range	85	Delayed Trigger Level Error
42	Main Sweep Error — 1 ms Range		
43	Main Sweep Error — 100 µs Range		
44	Main Sweep Error — 10 µs Range	86	Main Trigger Level Error — CH1 or Line
45	Main Sweep Error — 1 µs Range	87	Main Trigger Level Error — CH2
46	Main Sweep Error — 100 ns Range	88	Main Trigger Level Error — EXT
47	Main Sweep Error — 10 ns Range		
48	Main Sweep Error — 5 ns Range		
49	Main Sweep Error — 100 ms Range	89	Delayed Trigger Level Error — CH1 or Line
50	Main Sweep Error — 10 ms Range	90	Delayed Trigger Level Error — CH2
51	Main Sweep Error — 1 ms Range	91	Delayed Trigger Level Error — EXT
52	Main Sweep Error — 100 µs Range		
53	Main Sweep Error — 10 µs Range		
54	Main Sweep Error — 1 µs Range	95	Separation Error
55	Main Sweep Error — 100 ns Range	96	Separation Error
56	Main Sweep Error — 10 ns Range		
57	Main Sweep Error — 5 ns Range		

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts lists. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacture's code numbers. Figure 6-1 shows the illustrated parts breakdown.

6-2. ABBREVIATIONS.

Table 6-1 lists abbreviations used in the parts lists, the schematics, and throughout this manual. The abbreviations in the parts list are always capital letters. However, in other parts of the manual abbreviations may be used with both lowercase and uppercase letters.

6-3. REPLACEABLE PARTS LIST.

Table 6-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Electrical assemblies and their components in alphanumerical order by reference designation.

The information given for each part consists of the following:

a. Reference designation.

b. Hewlett-Packard part number.

c. Part number Check Digit (CD).

d. Total quantity (QTY) in instrument (or on assembly). The total quantity is given only once at the first appearance of the part number in the list.

e. Description of part.

f. Typical manufacturer of part in an identifying five-digit code.

6-4. ORDERING INFORMATION.

To order a part listed in the material lists, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the material lists, include the instrument model number, instrument serial number, a description of the part (including its function), and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-5. DIRECT MAIL ORDER SYSTEM.

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

a. Direct ordering and shipment from the Hewlett-Packard Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local Hewlett-Packard office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices.

To provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information is available through your local Hewlett-Packard office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	F	= fuse	Q	= transistor; SCR, triode thyristor	U	= integrated circuit, microcircuit
B	= fan; motor	FL	= filter	R	= resistor	V	= electron tube, glow lamp
BT	= battery	H	= hardware	RT	= thermistor	VR	= voltage regulator, breakdown diode
C	= capacitor	J	= electrical connector (stationary portion); jack	S	= switch; jumper	W	= cable
CR	= diode; diode thyristor; varactor	L	= coil; inductor	T	= transformer	X	= socket
DL	= delay line	MP	= misc. mechanical part	TB	= terminal board	Y	= crystal unit (piezo-electric or quartz)
DS	= annunciator; lamp; LED	P	= electrical connector (movable portion); plug	TP	= test point		
E	= misc. electrical part						

ABBREVIATIONS

A	= amperes	DWL	= dowel	MFR	= manufacturer	RND	= round
A/D	= analog-to-digital	ECL	= emitter coupled logic	MICPROC	= microprocessor	ROM	= read-only memory
AC	= alternating current	ELAS	= elastomeric	MINTR	= miniature	RPG	= rotary pulse generator
ADJ	= adjustment)	EXT	= external	MISC	= miscellaneous	RX	= receiver
AL	= aluminum	F	= farads; metal film (resistor)	MLD	= molded	S	= Schottky-clamped, seconds (time)
AMPL	= amplifier	FC	= carbon film/ composition	MM	= millimeter	SCR	= screw; silicon controlled rectifier
ANLG	= analog	FD	= feed	MO	= metal oxide	SEC	= second (time); secondary
ANSI	= American National Standards Institute	FEM	= female	MTG	= mounting	SEG	= segment
ASSY	= assembly	FF	= flip-flop	MTLC	= metallic	SEL	= selector
ASTIG	= astigmatism	FL	= flat	MUX	= multiplexer	SGL	= single
ASYNCHRO	= asynchronous	FM	= foam,from	MW	= milliwatt	SHF	= shift
ATTEN	= attenuator	FR	= front	N	= nano (10-9)	SI	= silicon
AWG	= American wire gauge	FT	= gain bandwidth product	NC	= no connection	SIP	= single in-line package
BAL	= balance	FW	= full wave	NMOS	= n-channel metal-oxide semiconductor	SKT	= skirt
BCD	= binary-coded decimal	FXD	= fixed	NPN	= negative-positive-negative	SL	= slide
BD	= board	GEN	= generator	NPRN	= neoprene	SLDR	= solder
BFR	= buffer	GND	= grounded)	NRFR	= not recommended for field replacement	SLT	= slotted
BIN	= binary	GP	= general purpose	NSR	= not separately replaceable	SOLD	= solenoid
BRDG	= bridge	GRAT	= graticule	NUM	= numeric	SPCL	= special
BSHG	= bushing	GRV	= groove	OBD	= order by description	SQ	= square
BW	= bandwidth	H	= henries; high	OCTL	= octal	SREG	= shift register
C	= ceramic; cermet (resistor)	HD	= hardware	OD	= outside diameter	SRQ	= service request
CAL	= calibrate, calibration	HDND	= hardened	OP AMP	= operational amplifier	STAT	= static
CC	= carbon composition	HG	= mercury	OSC	= oscillator	STD	= standard
CCW	= counterclockwise	HGT	= height	P	= plastic	SYNCHRO	= synchronous
CER	= ceramic	HLCL	= helical	P/O	= part of	TA	= tantalum
CFM	= cubic feet/minute	HORIZ	= horizontal	PC	= printed circuit	TBAX	= tubeaxial
CH	= choke	HP	= Hewlett-Packard	PCB	= printed circuit board	TC	= temperature coefficient
CHAM	= chamfered	HP-IB	= Hewlett-Packard Interface Bus	PD	= power dissipation	TD	= time delay
CHAN	= channel	HR	= hour(s)	PF	= picofards	THD	= threaded
CHAR	= character	HV	= high voltage	PI	= plug in	THK	= thick
CM	= centimeter	HZ	= Hertz	PL	= plate(d)	THRU	= through
CMOS	= complementary metal-oxide-semiconductor	I/O	= input/output	PLA	= programmable logic array	TP	= test point
CMR	= common mode rejection	IC	= integrated circuit	PLST	= plastic	TPG	= tapping
CNDCT	= conductor	ID	= inside diameter	PNP	= positive-negative-positive	TPL	= triple
CNTR	= counter	IN	= inch	POLYE	= polyester	TRANS	= transformer
CON	= connector	INCL	= includes)	POS	= positive, position	TRIG	= trigger ed)
CONT	= contact	INCAND	= incandescent	POT	= potentiometer	TRMR	= trimmer
CRT	= cathode-ray tube	INP	= input	POZI	= pozidrive	TRN	= turns
CW	= clockwise	INTEN	= intensity	PP	= peak-to-peak	TTL	= transistor-transistor
D	= diameter	INTL	= internal	PPM	= parts per million	TX	= transmitter
D/A	= digital-to-analog	INV	= inverter	PRCN	= precision	U	= micro (10-6,
DAC	= digital-to-analog converter	JFET	= junction field-effect transistor	PREAMP	= preamplifier	UL	= Underwriters Laboratory
DARL	= darlington	JKT	= jacket	PRGMBL	= programmable	UNREG	= unregulated
DAT	= data	K	= kilo (103)	PRL	= parallel	VA	= voltampere
DBL	= double	L	= low	PROG	= programmable	VAC	= volt, ac
DBM	= decibel referenced to 1 mW	LB	= pound	PSTN	= position	VAR	= variable
DC	= direct current	LCH	= latch	PT	= point	VCO	= voltage controlled oscillator
DCDR	= decoder	LCL	= local	PW	= potted wirewound	VDC	= volt, dc
DEG	= degree	LED	= light-emitting diode	PWR	= power	VERT	= vertical
DEMUX	= demultiplexer	LG	= long	R-S	= reset-set	VF	= voltage, filtered
DET	= detector	LI	= lithium	RAM	= random-access memory	VS	= versus
DIA	= diameter	LK	= lock	RECT	= rectifier	W	= watts
DIP	= dual in-line package	LKWR	= lockwasher	RET	= retainer	W/	= with
DIV	= division	LS	= low power Schottky	RF	= radio frequency	W/O	= without
DMA	= direct memory access	LV	= low voltage	RGLTR	= regulator	WW	= wirewound
DPDT	= double-pole, double-throw	M	= mega (106), megohms; meter (distance)	RGTR	= register	XSTR	= transistor
DRC	= DAC refresh controller	MACH	= machine	RK	= rack	ZNR	= zener
DRVR	= driver	MAX	= maximum	RMS	= root-mean-square	°C	= degree Celsius (Centigrade)
						°F	= degree Fahrenheit
						°K	= degree Kelvin

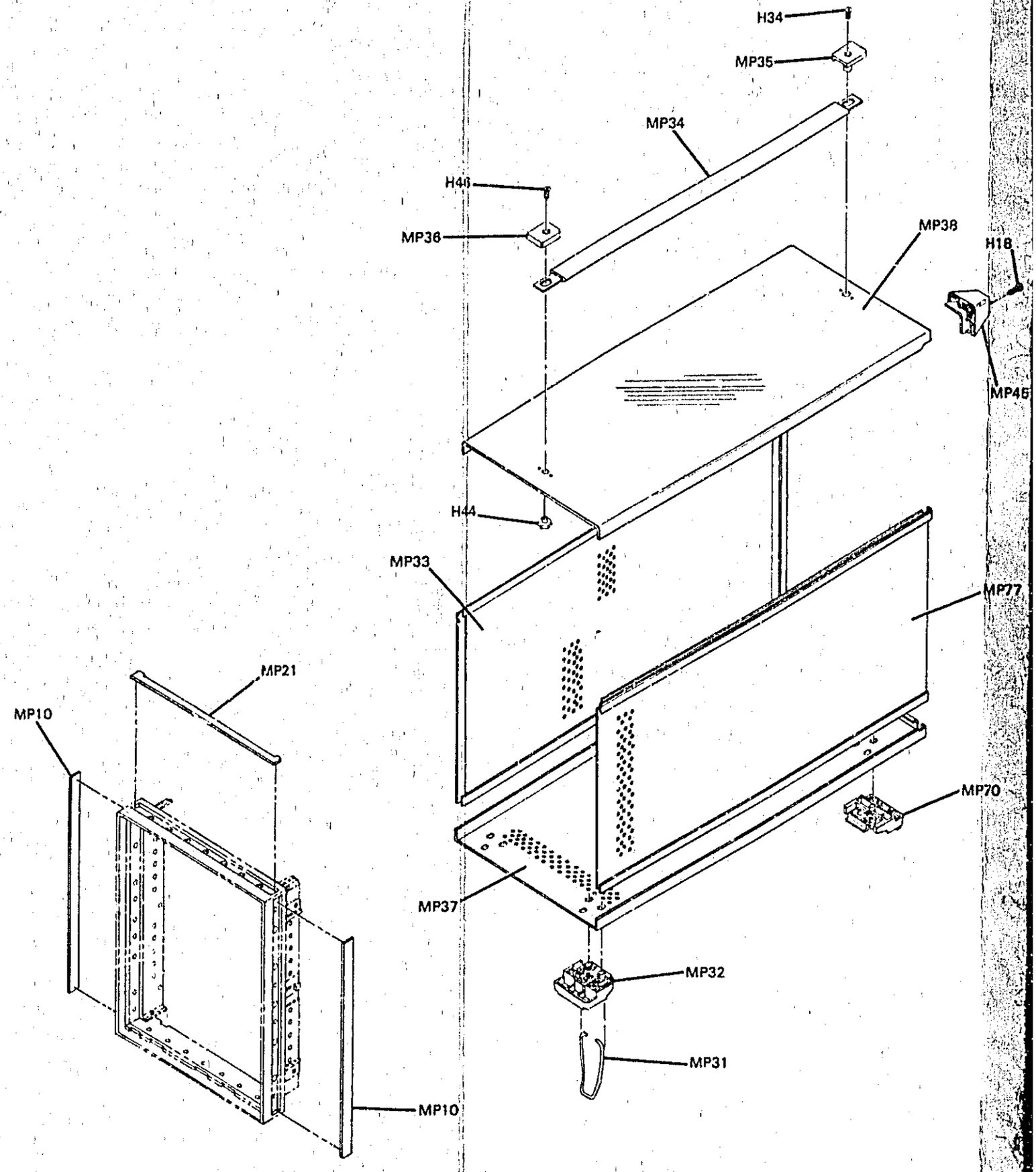


Figure 6-1.
Covers and Trim Parts Identification

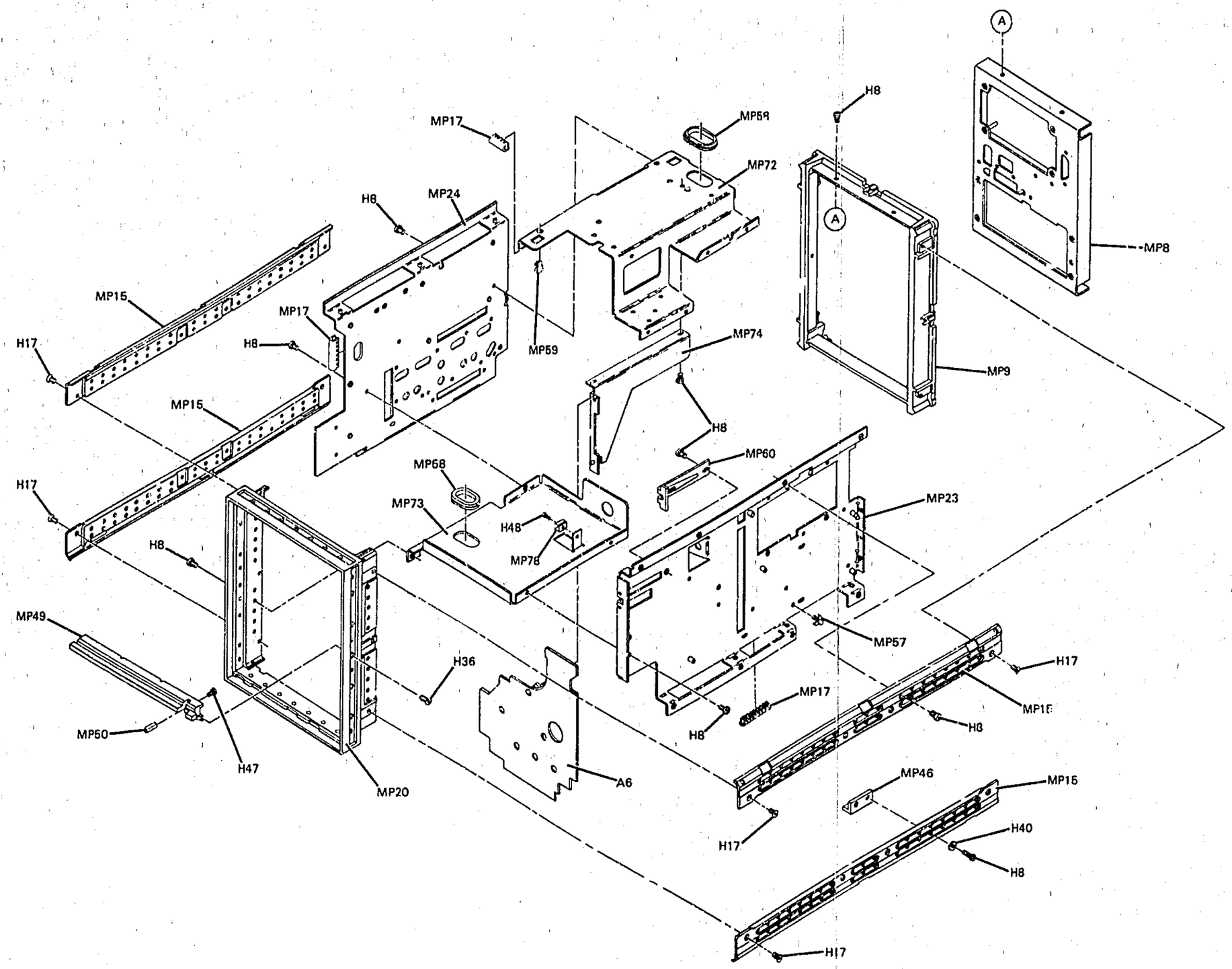


Figure 6-2.
Chassis Parts Identification

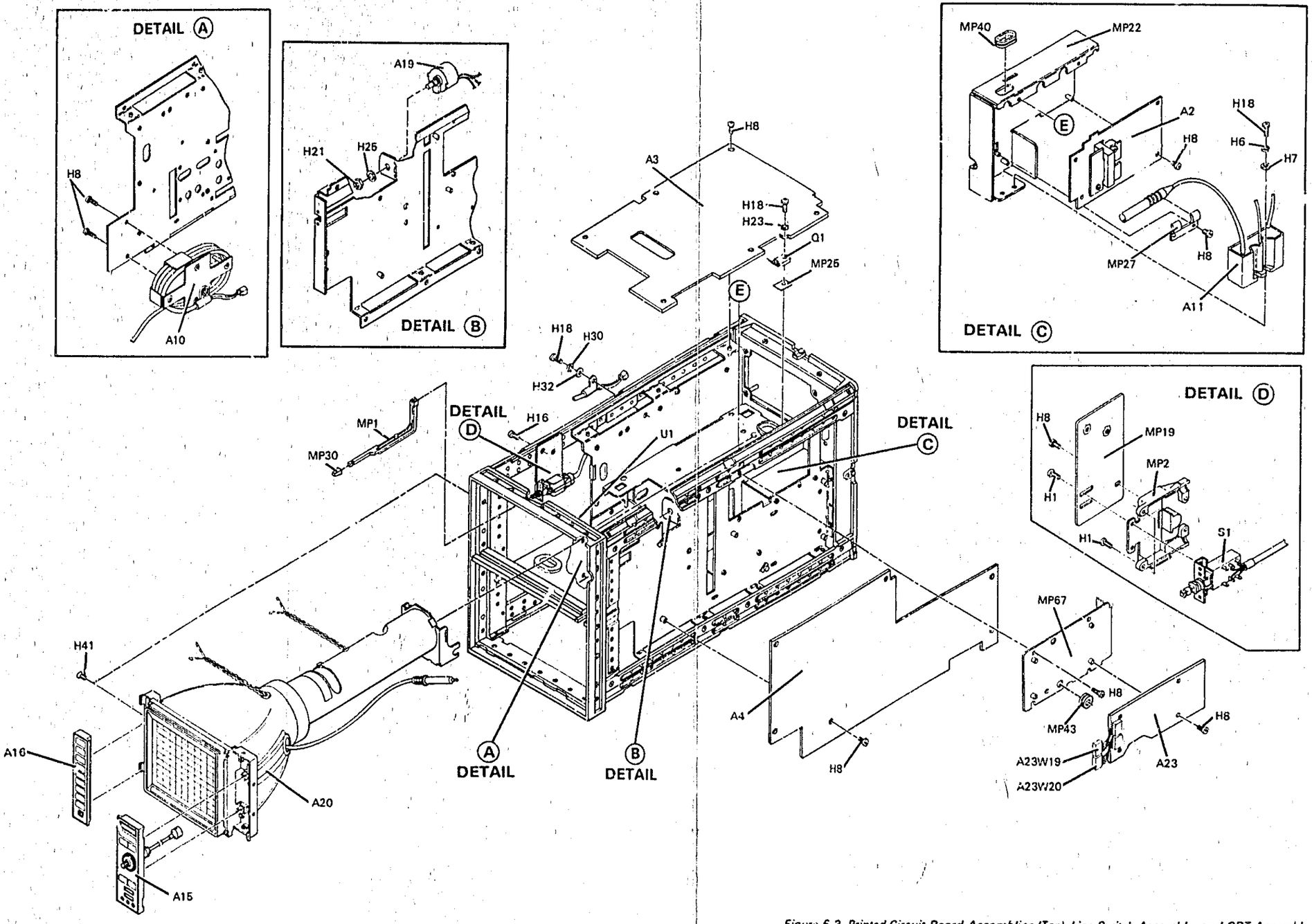


Figure 6-3. Printed Circuit Board Assemblies (Top), Line Switch Assembly, and CRT Assembly Identification

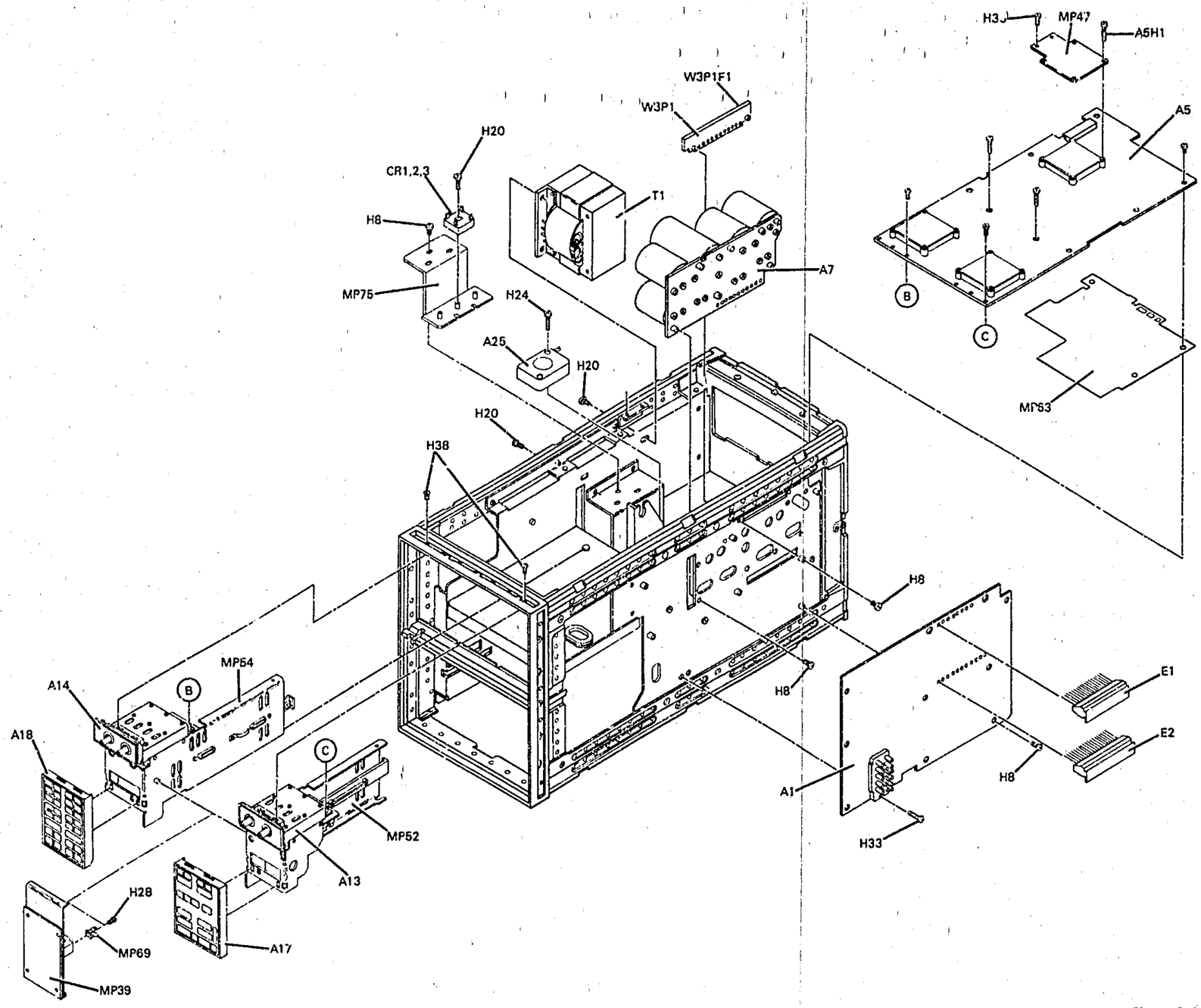


Figure 6-4.
Printed Circuit Board Assemblies (bottom), Time and Voltage Panel Assemblies and Attenuator Assemblies Identification

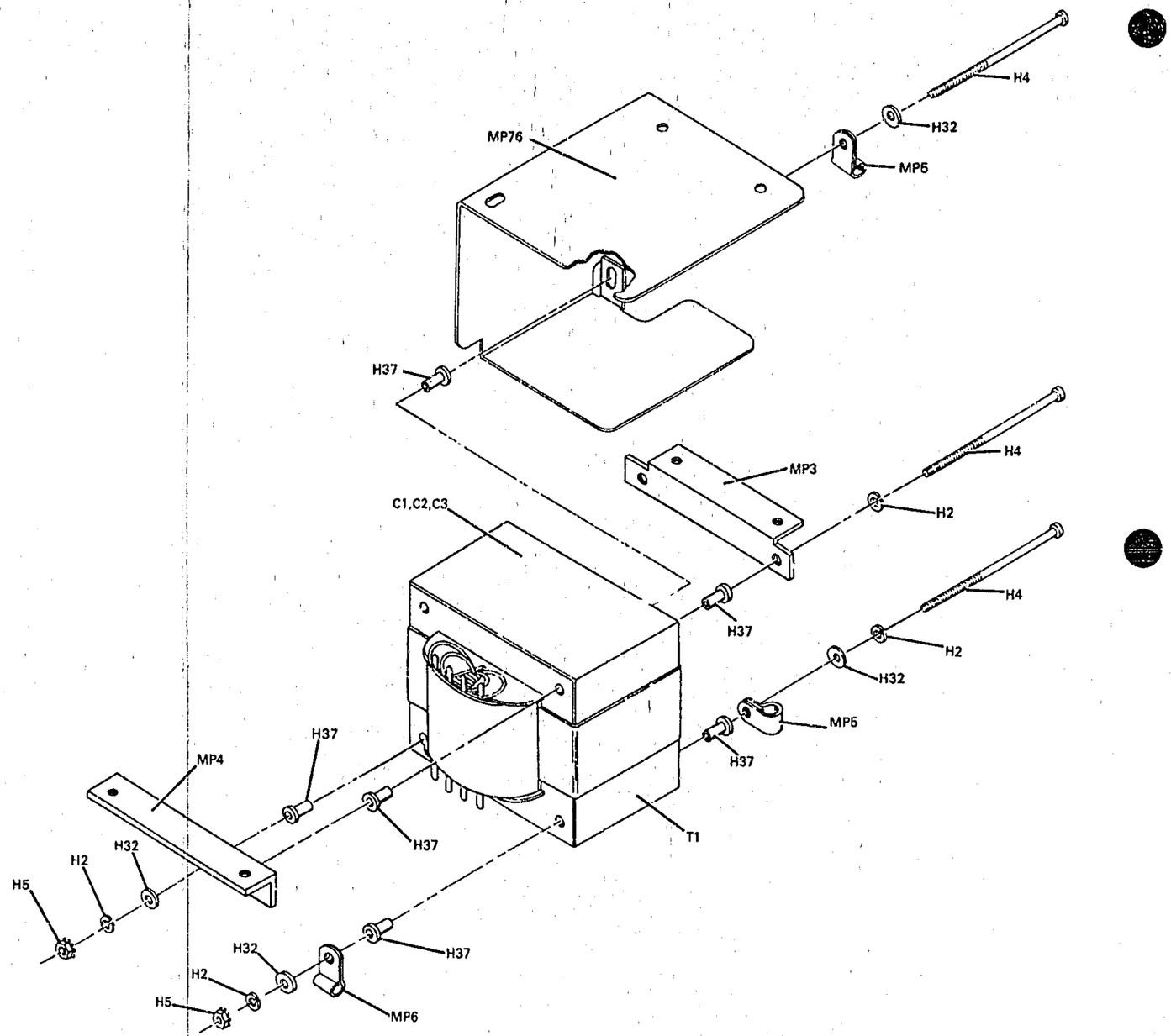
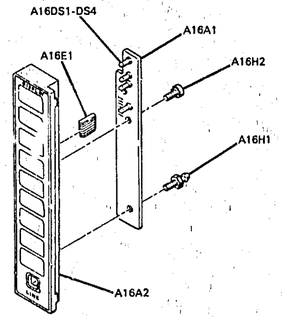
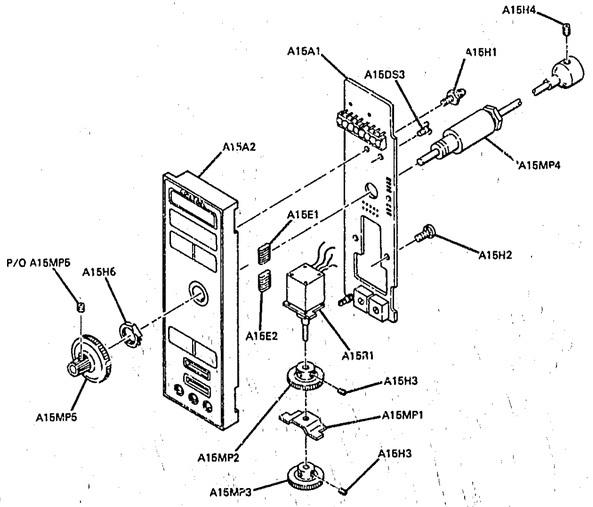


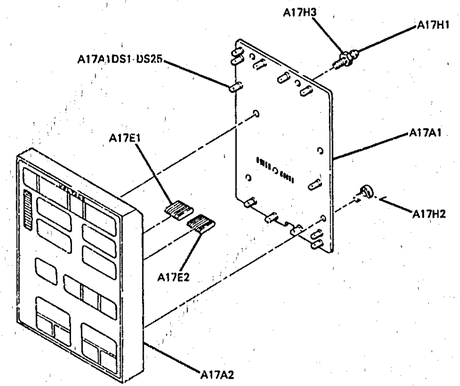
Figure 6-5. Transformer Assembly Mounting Parts Identification



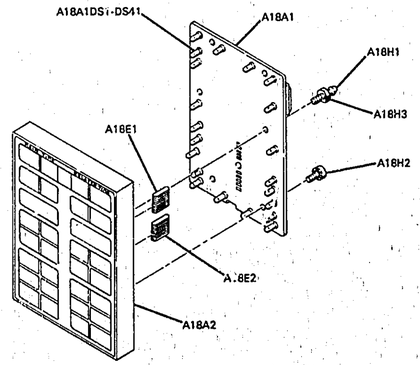
DISPLAY PANEL



CONTROL PANEL

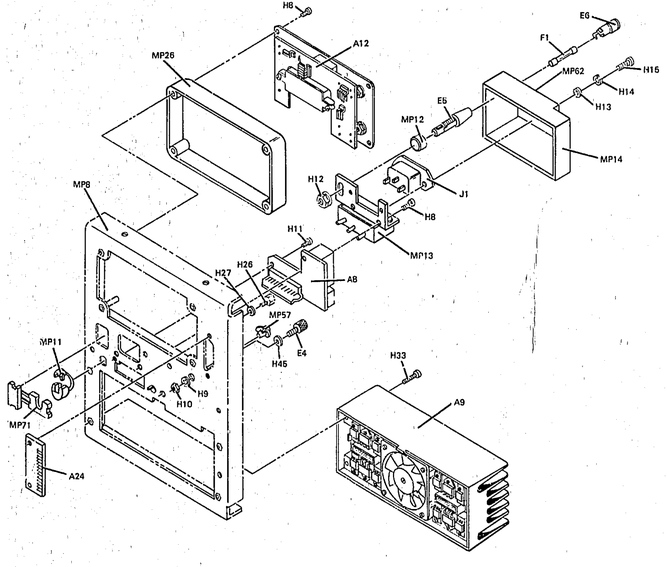


VOLTAGE PANEL

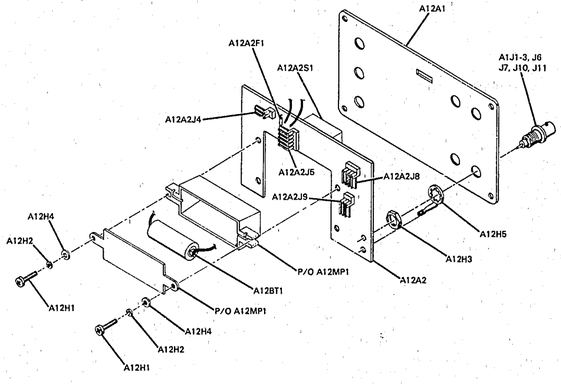


TIME PANEL

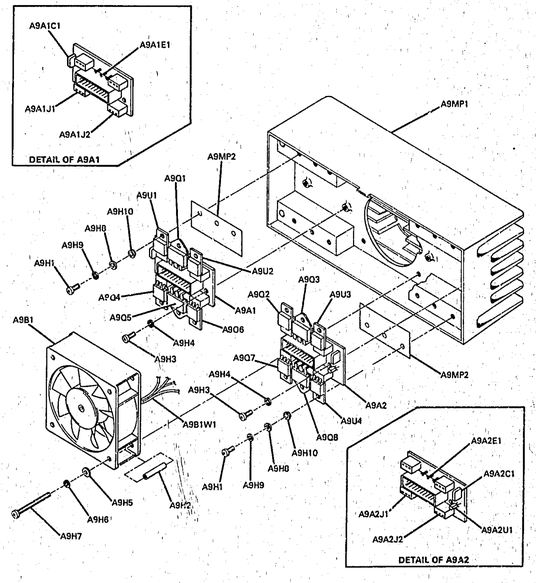
Figure 6-6.
Display Panel, Control Panel, Voltage Panel, and Time Panel Parts Identification



REAR PANEL



BNC PANEL



HEAT SINK

Figure 6-7. Rear Panel, BNC Panel (A12), and Heat Sink (A9) Parts Identification

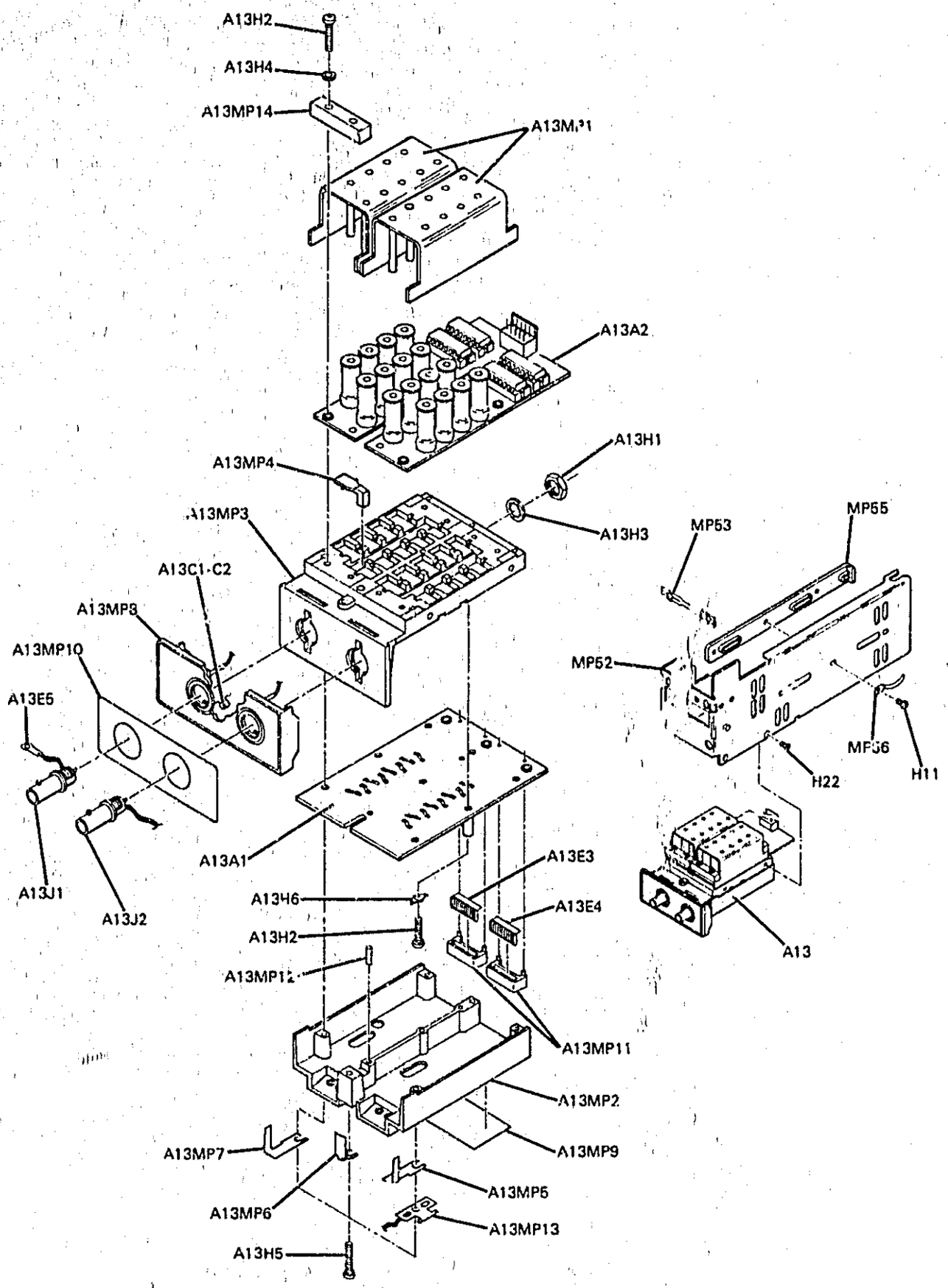


Figure 6-8. Vertical Attenuator Assembly (A13) Parts Identification

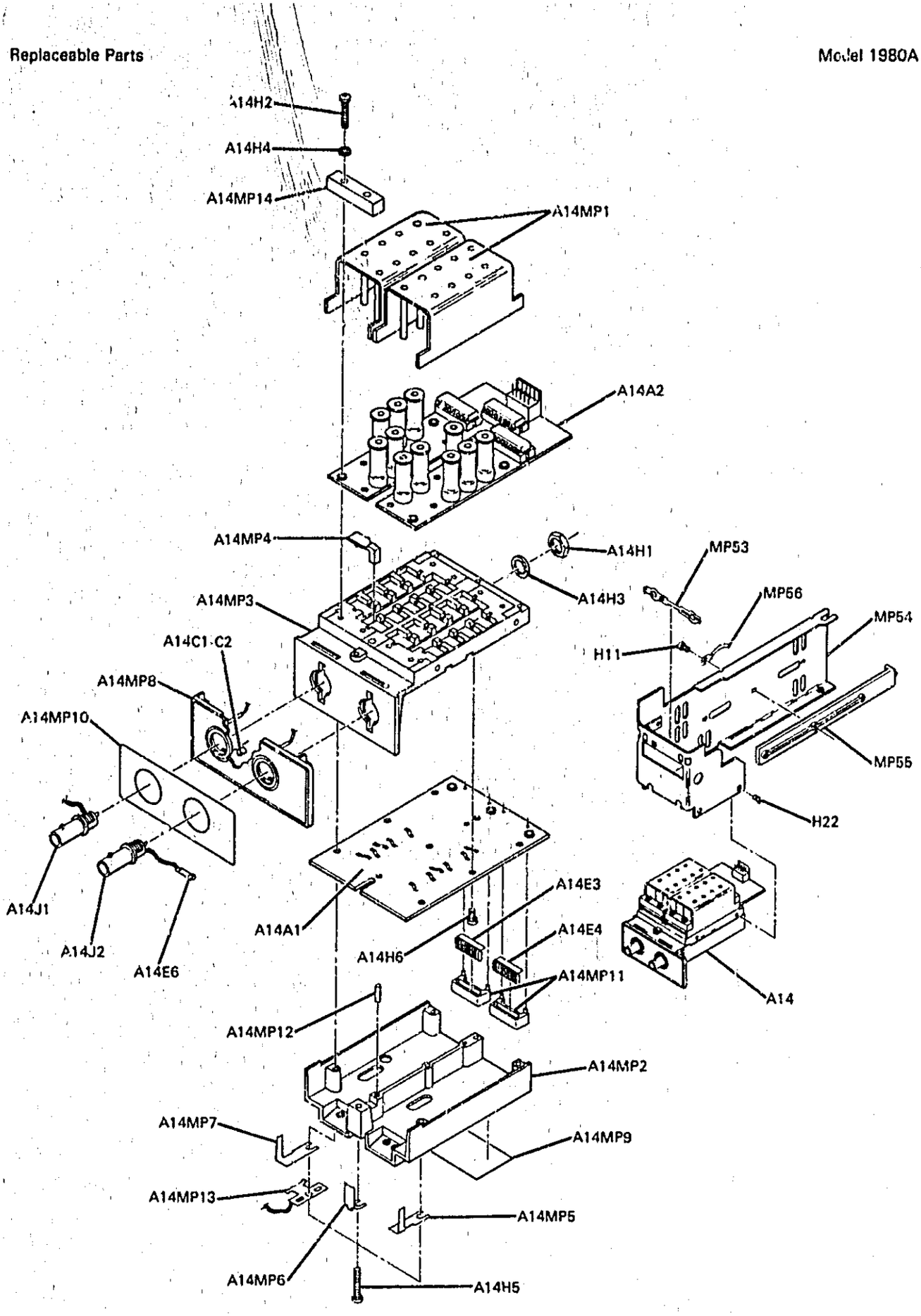


Figure 6-9. Trigger Attenuator Assembly (A14) Parts Identification

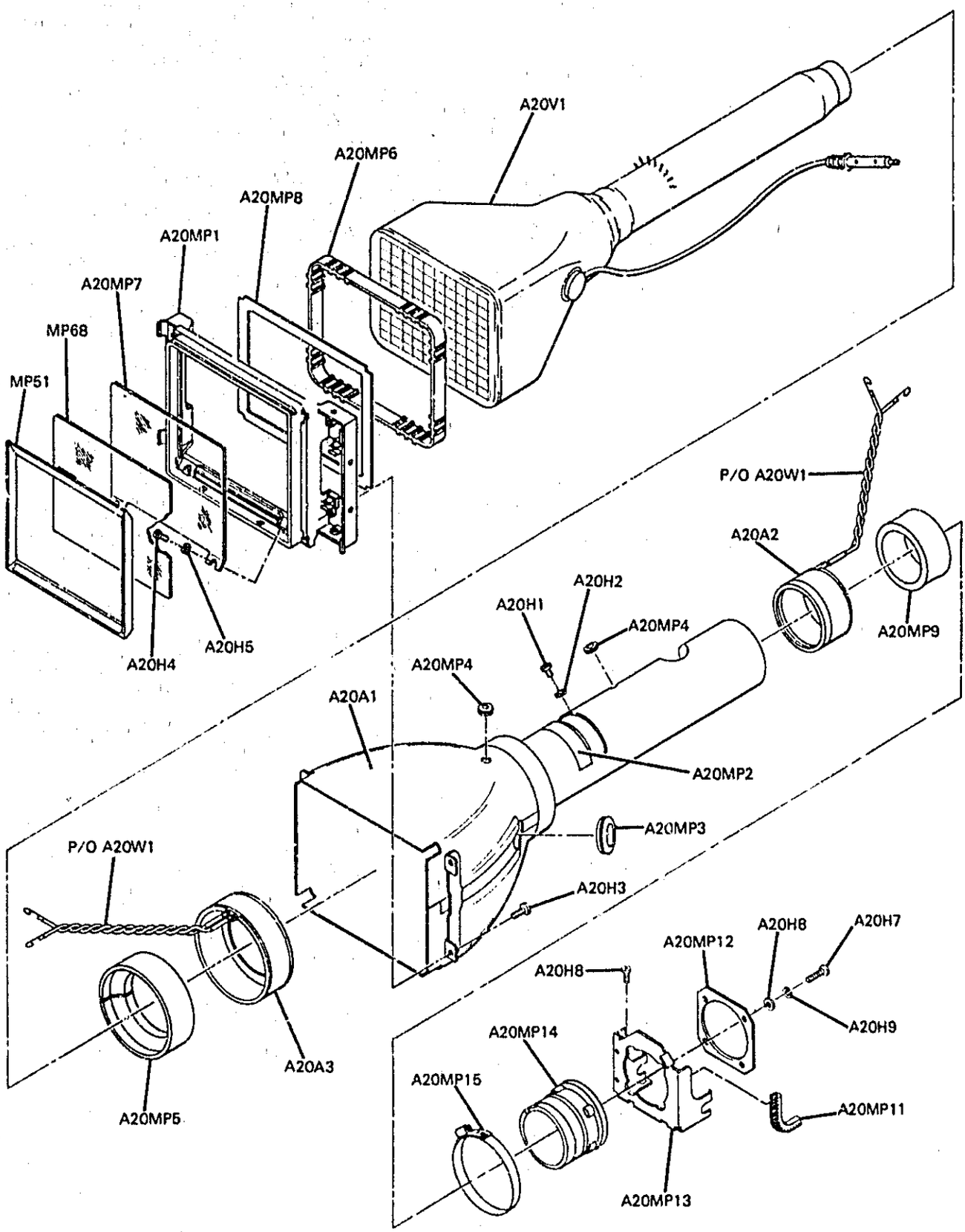


Figure 6-10. CRT Assembly (A20) Parts Identification

Table 6-2. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01980-66539	1	1	BOARD ASSY-L V SUPPLY	28480	01960-66539
A2	01980-66550	4	1	HIGH VOLTAGE BOARD	28480	01980-66550
A3	01980-66503	8	1	GATE OSCILLOSCOPE BOARD	28480	01960-66503
A4	01980-66547	1	1	PROCESSOR BOARD	28480	01980-66547
A5	01980-69508	0	1	BOARD ASSY-SCOPE	28480	01980-69508
A6	01980-66506	1	1	BOARD-INTERFACE	28480	01980-66506
A7	01980-66508	4	1	BOARD ASSY-CAPACITOR	28480	01980-66508
A8	01980-66514	2	1	LINE SELECT BOARD	28480	01980-66514
A9	01980-60604	9	1	HEAT SINK ASSY	28480	01980-60604
A10	01980-61628	9	1	DELAY LINE ASSY	28480	01980-61628
A11	0960-0651	2	1	MULTIPLIER-H V	28480	0960-0651
A12	01980-60209	0	1	BNC PANEL ASSY	28480	01980-60209
A13	01980-63401	0	1	VERT ATTEN ASSY	28480	01980-63401
A14	01980-63402	1	1	TRIG ATTEN ASSY	28480	01980-63402
A15	01980-60203	4	1	PANEL ASSY-CONTROL	28480	01980-60203
A16	01980-60204	5	1	PANEL ASSY-DISPLAY	28480	01980-60204
A16 (OPT 660)	01980-60214	7	1	PANEL ASSY-DISPLAY	28480	01980-60214
A17	01980-60202	3	1	PANEL ASSY-VOLT	28480	01980-60202
A18	01980-60201	2	1	PANEL ASSY-TIME	28480	01980-60201
A19	01980-61062	5	1	ASSY-RPG	28480	01980-61062
A20	01980-60602	7	1	CRT DISPLAY ASSY	28480	01980-60602
A23	19842-66503	2	1	BUS INTERFACE BOARD	28480	19842-66503
A24	19842-66502	6	1	HP-IB CONNECTOR BOARD	28480	19842-66502
A25	01980-66501	1	1	FAN DRIVE ASSY	28480	01980-66501
CR1	1901-0525	7	3	DIODE-FW BRDG 50V 25A	28480	1901-0525
CR2	1901-0525	7		DIODE-FW BRDG 50V 25A	28480	1901-0525
CR3	1901-0525	7		DIODE-FW BRDG 50V 25A	28480	1901-0525
E1	01980-47602	9	1	CONNECTOR HOLDER	28480	01980-47602
E2	01980-47601	8	1	CONNECTOR HOLDER	28480	01980-47601
E3	0362-0366	7	1	CONNECTOR SGL CONT SKT 1 14-MM BSC SZ	28480	0362-0366
E4	1510-0038	8	1	BINDING POST ASSY SGL THD STUD	28480	1510-0038
E5	2110-0664	8	1	FUSEHOLDER BODY 12A MAX FOR UL	H9027	031-1657
E6	2110-0665	9	1	FUSEHOLDER CAP 12A MAX FOR UL	28480	2110-0665
F1	2110-0003	0	1	FUSE 3A 250V NTD 1.25X.25 UL	75915	312003
F1	2110-0002	9	1	FUSE 2A 250V NTD 1.25X.25 UL	28480	2110-0002
FL1	NSR	4		FILTER (ORDER 01980-61214, MP13)	28480	NSR
H1	0624-0004	8	4	SCREW-TPG 4-24 .375-IN-LG PAN-HD-SLT	00000	ORDER BY DESCRIPTION
H2	2190-0017	4	4	WASHER-LK HLCL NO 8 .168 IN-ID	78420	2190-0017
H4	2510-0138	0	4	SCREW-MACH 8-32 3 IN LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H5	2680-0003	5	2	NUT-HEX W/LKWR 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H6	2190-0006	1	3	WASHER-LK HLCL NO 6 .141 IN-ID	28480	2190-0006
H7	3050-0010	2	2	WASHER-FL MTLC NO 6 .147-IN-ID	28480	3050-0010
H8	2360-0113	2	104	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H9	2190-0027	6	1	WASHER-LK INTL T 1/4 IN .266-IN-ID	28480	2190-0027
H10	2950-0006	3	1	NUT-HEX-DBL-CHAM 1/4-40-THD .062-IN-THK	00000	ORDER BY DESCRIPTION
H11	2200-0103	2	2	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H12	2110-0569	3	1	NUT-FUSEHOLDER	28180	2110-0569
H13	3050-0235	3	2	WASHER-FL MTLC NO 4 .117-IN-ID	28480	3050-0235
H14	2190-0019	6	2	WASHER-LK HLCL NO 4 .115-IN-ID	28480	2190-0019
H15	2200-0143	0	2	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H16	2510-0043	5	2	SCREW-MACH 8-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H17	2510-0192	6	16	SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
H18	2360-0197	2	8	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H19	2510-0049	2	4	SCREW-MACH 8-32 .5 IN LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H20	2360-0117	6	3	SCREW-MACH 6-32 .375 IN LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H21	2950-0043	8	2	NUT-HEX-DBL-CHAM 3/8 32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H22	2200-0164	5	8	SCREW-MACH 4-40 .188-IN-LG UNCT 82 DEG	00000	ORDER BY DESCRIPTION
H23	2190-0909	3	1	WASHER-LK INTL T NO 6 .146-IN-ID	28480	2190-0909
H24	2360-0236	0	6	SCREW-MACH 6-32 .812-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H25	2190-0016	3	1	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
H26	0360-0644	4	2	STANDOFF-HEX .327-IN LG 6-32 HD	00000	ORDER BY DESCRIPTION
H27	2190-0034	5	2	WASHER-LK HLCL NO 10 .194-IN-ID	28480	2190-0034
H28	0624-0268	6	2	TS 4-24 .250 LG	00000	ORDER BY DESCRIPTION
H29	2190-0046	9	3	WASHER-LK HLCL NO 6 .141 IN-ID	28480	2190-0046
H32	3050-0071	5	9	WASHER-FL MTLC NO 8 .169-IN-ID	28480	3050-0071
H33	2360-0125	6	8	SCREW-MACH 6-32 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H34	2680-0172	1	4	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H35	2200-0105	4	10	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H36	2360-0118	7	2	SCREW-MACH 6-32 .375 IN LG 82 DEG	00000	ORDER BY DESCRIPTION
H37	0390-0006	3	6	INSULATOR-FLG-BSHG NYLON	28480	0390-0006
H38	2510-0193	7	4	SCREW-MACH 8-32 .375-IN-LG PAN-HD-POZI	28480	2510-0193

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
H39	3050-0016	8	2	WASHER-FL MTLC NO 6 .147-IN ID	28480	3050-0016
H40	3050-0105	6	2	WASHER-FL MTLC NO 4 .125-IN ID	28480	3050-0105
H41	2510-0195	9	4	SCREW-MACH 8-32 .375-IN LG	28480	2510-0195
H42	2510-0044	7	4	SCREW MACHINE	28480	2510-0195
H43	2200-0115	6	4	SCREW-MACH 4-40 .750-IN LG	00000	ORDER BY DESCRIPTION
H44	01980-25702	4	1	NUT-FRONT HANDLE MOUNT	28480	01980-25702
H45	3050-0028	2	1	WFL .250 .473	00000	ORDER BY DESCRIPTION
H46	2680-0160	1	1	MACHINE SCREW	28480	2680-0106
H47	2200-0107	6	1	SCREW	28480	2200-0107
H48	2200-0107	6	1	SCREW	28480	2200-0107
J1	1251-2357	8	1	CONNECTOR-AC PWR HP-9 MALE FLG-MTG	28480	1251-2357
MP1	3131-0442	6	1	SWITCH EXTENDER	28480	3131-0442
MP2	5041-1686	2	1	SWITCH COVER	28480	5041-1686
MP3	01980-01210	9	1	BRACKET-TRANSFORMER, RIGHT	28480	01980-01210
MP4	01980-01211	0	1	BRACKET-TRANSFORMER, LEFT	28480	01980-01211
MP5	1400-0017	0	2	CLAMP-CABLE .312-DIA .375-WD NYL	28480	1400-0017
MP6	1400-0024	9	1	CLAMP CABLE .25-DIA .5-WD NYL	28480	1400-0024
MP7	01980-01201	8	1	BRACKET-MULTIPLIER, SMALL	28480	01980-01201
MP8	01980-00201	6	1	PANEL-REAR	28480	01980-00201
MP9	5020-8822	9	1	CASTING,REAR	28480	5020-8822
MP10	5001-0442	3	2	TRIM-FRONT SIDE	28480	5001-0442
MP11	0400-0013	5	1	GROMMET-STR RLF STR-THRU 1-IN-THK-PNL	28480	0400-0013
MP12	0380-1158	7	1	SPACER RND .25-IN LG .5 IN-ID .625-IN-OD	00000	ORDER BY DESCRIPTION
MP13	01980-01214	3	1	BRACKET LINE MODULL	28480	01980-01214
MP14	5041-2368	0	1	LINE COVER	28480	5041-2368
MP15	5020-8837	6	4	STRUT,CORNER	28480	5020-8837
MP16	01980-00106	0	1	RIB-CENTRAL BACK	28480	01980-00106
MP17	0400-0226	2	8	GROMMET-CHAN .062-IN-GRV WD	95987	CSG-06-NATURAL
MP19	01980-01203	0	1	BRACKET-POWER SWITCH	28480	01980-01203
MP20	5020-8821	8	1	CASTING, FRONT	28480	5020-8821
MP21	5040-7203	0	1	TRIM, TOP	28480	5040-7203
MP22	01980-05501	9	1	BOX-H V	28480	01980-05E01
MP23	01980-00114	0	1	DECK RIGHT	28480	01980-00114
MP24	01980-00102	6	1	DECK-LEFT	28480	01980-00102
MP25	0340-0664	3	1	INSULATOR-XSTR THRM-CNDCT	28480	0340-0664
MP26	5041-2373	7	1	BEZEL-BNC PANEL	28480	5041-2373
MP27	01980-01204	1	1	BRACKET-H.V LEAD	28480	01980-01204
MP29	01980-00401	8	5	MOUNT-P C BOARD	28480	01980-00401
MP30	0370-2802	1	1	PUSHBUTTON 0.230 IN SQ: 0.425 IN HGT	28480	0370-2802
MP31	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP32	5040-7201	8	2	FOOT,STANDARD	28480	5040-7201
MP33	5061-1966	8	2	COVER-SIDE, RIGHT	28480	5061-1966
MP34	5060-9804	3	2	HANDLE STRAP	28480	5060-9804
MP35	SEE NOTE 1		1	RETAINER-HANDLE STRAP REAR	28480	
MP36	SEE NOTE 2		1	RETAINER-HANDLE STRAP FRONT	28480	
				NOTE 1. ORDER 1 EA 01980-22302 (REAR RETAINER) AND 1 EA 5041-3047 (HANDLE CAP).		
				NOTE 2. ORDER 1 EA 01980-22303 (FRONT RETAINER) AND 1 EA 5041-3047 (HANDLE CAP).		
MP37	5061-1965	7	1	COVER ASSEMBLY-BOTTOM	28480	5061-1965
MP38	5061-1964	6	1	COVER ASSEMBLY-TOP	28480	5061-1964
MP39	01980-24106	0	1	PANEL-ENHANCE MOD COVER	28480	01980-24106
MP40	0400-0001	1	1	GROMMET-RND .062-IN-ID .75-IN-GRV-OD	28480	0400-0001
MP41	0400-0009	9	1	GROMMET-RND .125 IN-ID .25-IN-GRV-OD	28480	0400-0009
MP42	1400-1052	5	1	CABLE CLAMP	76853	C20744 017.4
MP43	0400-0010	2	2	GROMMET-RND .25-IN-ID .375-IN GRV-OD	28480	0400-0010
MP45	5040-7221	2	4	STANDOFF, REAR PANEL	28480	5040-7221
MP46	01980-01223	4	1	BRACKET-HEAT SINK	28480	01980-01223
MP47	01980-04105	7	1	COVER-HEAT SINK	28480	01980-04105
MP49	01980-63701	3	1	FILL STRIP	28480	01980-63701
MP50	1251-6199	4	1	JACK-BNA SCR-TERM	28480	1251-6199
MP51	01980-22201	2	1	RETAINER-FILTER	28480	01980-22201
MP52	01980-00111	7	1	HOUSING-VERTICAL ASSEMBLY	28480	01980-00111
MP53	1600-0662	7	2	SLIDEBAR, LATCH	28480	1600-0662
MP54	01980-00112	8	1	HOUSING-TRIGGER ASSEMBLY	28480	01980-00112
MP55	01980-43101	5	2	GUIDE-PLUG-IN	28480	01980-43101
MP56	01980-09104	6	1	CLIP-GROUND	28480	01980-09104
MP57	0380-1276	0	2	SPACER-SNAP-IN .188 IN LG, .280 IN OD	00000	ORDER BY DESCRIPTION
MP58	0400-0236	4	2	GROMMET, 1 1/8" DIAMETER	76385	2228
MP59	1400-0579	0	6	CLIP-CABLE 'U' SHP, PNL MTG TYPE	28480	1400-0679
MP60	5041-3059	8	1	GUIDE-SHAFT	28480	5041-3059
MP61	5041-3062	3	1	SUPPORT POST-CABLE	28480	5041-3062
MP62	7121-0298	3	1	LABEL-LINE MOD	28480	7121-0298
MP63	01980-24107	1	1	PLATE-COVER	28480	01980-24107

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP64	01980-24303	9	1	LABEL-TAG 1980A	28480	01980-24303
MP65	01980-24304	0	1	LABEL-WARNING 1980A	28480	01980-24304
MP66	1400-1069	2	1	CLAMP-CABLE	59730	TC68
MP67	01980-04101	3	1	H.V. COVER	28480	01980-04101
MP68	01980-02701	5	1	CONTRAST FILTER	28480	01980-02701
MP69	1400-0076	1	2	FUSE CLIP	28480	1400-0076
MP70	5040-7222	3	2	REAR FOOT, NONSKID	28480	5040-7222
MP71	5041-3119	1	1	COVER, LINE AC	28480	5041-3119
MP72	01980-00115	1	1	DECK, CENTER, REAR	28480	01980-00115
MP73	01980-00116	2	1	DECK, FRONT	28480	01980-00116
MP74	01980-01232	6	1	SUPPORT BRACKET	28480	01980-01232
MP75	01980-01231	4	1	RECTIFIER BRACKET	28480	01980-01231
MP76	01980-00606	5	1	TRANSFORMER SHIELD	28480	01980-00606
MP77	5061-1987	9	1	COVER, LEFT SIDE	28480	5061-1987
MP78			1	CLAMP, CABLE	28480	NEW PART HV WIRE
Q1	1854-0133	6	1	TRANSISTOR NPN SI PD=60W FT=2MHZ	28480	1854-0133
S1	3101-1720	2	1	SWITCH PB DPDT 4A 250VAC	28480	3101-1720
T1	9100-4243	4	1	TRANSFORMER-POWER 100/120/220/240V	28480	9100-4243
U1	1826-0760	2	1	IC, TEMPERATURE SENSOR	28480	1826-0760
W1	8120-1521	8	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT	28480	8120-1521
W2	01980-61607	4	1	CABLE-LINE SWITCH	28480	01980-61607
W3	01980-61641	6	1	CABLE-TRANSFORMER SEC	28480	01980-61641
W4	01980-61642	7	1	CABLE-POWER SUPPLY	28480	01980-61642
W6	01980-61615	4	1	CABLE-PROC-DAT/DAC	28480	01980-61615
W7	01980-61614	3	2	CABLE ASSEMBLY-VERTICAL T	28480	01980-61614
W8	01980-61614	3		CABLE ASSEMBLY-VERTICAL T	28480	01980-61614
W10	01980-61621	2	1	CABLE ASSEMBLY-VERTICAL OP	28480	01980-61621
W11	01980-61631	4	1	CABLE ASSEMBLY-H.V. TRANSFORMER	28480	01980-61631
W12	01980-61601	8	1	CABLE-CRT BASE	28480	01980-61601
W13	01980-61622	3	1	CABLE ASSEMBLY-HORIZ OP	28480	01980-61622
W14	01980-61642	7	1	CABLE ASSEMBLY-PANEL P	28480	01980-61642
W15	01740-61616	5	1	CABLE ASSEMBLY-TRANS CON	28480	01740-61616
W16	01980-61629	0	1	CABLE-ROM PROCESS	28480	01980-61629
W17	01980-61630	3	1	CABLE-ROM DATA	28480	01980-61630
W21	01980-61620	1	1	CABLE ASSEMBLY-DISPLAY PR/C	28480	01980-61620
W22	01980-61619	8	1	CABLE ASSEMBLY-CON PR/C	28480	01980-61619
W23	01980-31617	6	1	CABLE-TIME/VOLT PANEL	28480	01980-61617
W24	01980-61618	7		CABLE-TIME/VOLT PANEL	28480	01980-61618
W27	01980-61602	9	1	CABLE ASSEMBLY-15V/CAL	28480	01980-61602
W28	01980-61623	4	1	CABLE ASSEMBLY-MAIN DY	28480	01980-61623
W29	01980-61625	6	1	CABLE ASSEMBLY-X-INPUT	28480	01980-61625
W30	01980-61624	5	1	CABLE ASSEMBLY-Y-Z INPUT	28480	01980-61624
W33	01980-61612	1	1	CABLE ASSEMBLY-SWITCH AVSB	28480	01980-61612
W34	01980-61613	2	1	CABLE ASSEMBLY-Z-AXIS	28480	01980-61613

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01980-66539	1	1	LV POWER SUPPLY ASSEMBLY	28480	01980-66539
A1C1	0180-0229	7	1	CAPACITOR-FXD 33UF±10% 10VDC TA	56289	150D336X9010B2
A1C2	0160-3622	8	14	CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C3	0160-2065	R	13	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C4	0180-0058	0	2	CAPACITOR-FXD 50UF+75-10% 25VDC AL	56289	30D506G025CC2
A1C5	0180-2210	0	2	CAPACITOR-FXD 2UF+50-10% 150VDC AL	56289	30D205F150BB2
A1C6	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C7	0180-2210	0		CAPACITOR-FXD 2UF+50-10% 150VDC AL	56289	30D205F150BB2
A1C8	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C9	0160-3762	5	6	CAPACITOR-FXD 1000PF ±10% 50VDC CER	28480	0160-3762
A1C10	0160-3762	5		CAPACITOR-FXD 1000PF ±10% 50VDC CER	28480	0160-3762
A1C11	0180-2255	3	12	CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C12	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C14	0160-3762	5		CAPACITOR-FXD 1000PF ±10% 50VDC CER	28480	0160-3762
A1C15	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C16	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C17	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C18	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C19	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C20	0180-0161	6	1	CAPACITOR-FXD 3.3UF±10% 35VDC TA	00908	T110B335K035AS
A1C22	0160-3652	4	3	CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER	28480	0160-3652
A1C23	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C25	0160-3770	7	1	CAPACITOR-FXD 47PF ±5% 100VDC CER	51642	200-100-N150-470J
A1C26	0160-3799	0		CAPACITOR-FXD 18PF ±10% 100VDC CER	28480	0160-3799
A1C27	0121-0467	1	1	CAPACITOR-V TRMR-CER 2.5-8PF [illegible] PC-MTG	28480	0121-0467
A1C28	0160-3762	5		CAPACITOR-FXD 1000PF ±10% 50VDC CER	28480	0160-3762
A1C29	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C30	0180-0230	0	1	CAPACITOR-FXD 1UF±20% 50VDC TA	56289	150D105X0050A2
A1C31	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C32	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C33	0160-3799	0		CAPACITOR-FXD 18PF ±10% 100VDC CER	28480	0160-3799
A1C34	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C35	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C36	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C37	0160-3724	1	1	CAPACITOR-FXD 47UF±5% 40VDC TA	28480	0160-3724
A1C40	0160-0161	4	1	CAPACITOR-FXD .01UF ±10% 200VDC POLYE	28480	0160-0161
A1C41	0140-0198	5	1	CAPACITOR-FXD 200PF ±5% 300VDC MICA	28480	0140-0198
A1C42	0160-3652	4		CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER	28480	0160-3652
A1C43	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C44	0160-3652	4		CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER	28480	0160-3652
A1C45	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C48	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C49	0160-2198	1	1	CAPACITOR-FXD 20PF [illegible]% 300VDC MICA	28480	0160-2198
A1C50	0160-3665	9	3	CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A1C51	0160-0165	8	2	CAPACITOR-FXD .056UF ±10% 200VDC POLYE	28480	0160-0165
A1C52	0121-0474	0	2	CAPACITOR-V TRMR-PSTN 3-13PF 600V	28480	0121-0474
A1C53	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C54	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C55	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A1C56	0160-0165	8		CAPACITOR-FXD .056UF ±10% 200VDC POLYE	28480	0160-0165
A1C57	0121-0474	0		CAPACITOR-V TRMR-PSTN 3-13PF 600V	28480	0121-0474
A1C58	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C59	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C61	0180-0301	6	1	CAPACITOR-FXD 5UF+75-10% 50VDC AL	56289	30D505G050BB2
A1C62	0160-3622	8		CAPACITOR-FXD .1UF100VDC CER	28480	0160-3622
A1C63	0160-3622	8		CAPACITOR-FXD .1UF 100VDC CER	28480	0160-3622
A1C64	0180-0058	0		CAPACITOR-FXD 50UF+75-10% 25VDC AL	56289	30D506G025CC2
A1C65	0160-5211	5		CAPACITOR-FXD .1UF 250VDC CER	28480	0160-5211
A1C66	0160-3622	8		CAPACITOR-FXD .1UF 100VDC CER	28480	0160-3622
A1C67	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C68	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C69	0160-3622	8		CAPACITOR-FXD .1UF 100VDC CER	28480	0160-3622
A1C70	0160-2065	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2065
A1C71	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A1C72	0160-3318	9	1	CAPACITOR-FXD .047UF ±10% 100VDC CER	28480	0160-3318
A1C73	0140-0200	0	1	CAPACITOR-FXD 330PF ±5% 300VDC MICA	28480	0140-0200
A1C74	0160-3651	3	1	CAPACITOR-FXD 68PF ±10% 200VDC CER	28480	0160-3651
A1C75	0160-3654	6	2	CAPACITOR-FXD .4700PF ±20% 50VDC CER	28480	0160-3654
A1C76	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A1C77	0160-3508	9	2	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C78	0160-3762	5		CAPACITOR-FXD 1000PF ±10% 50VDC CER	28480	0160-3762

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1C79	0160-3647	7	1	CAPACITOR-FXD 22PF ±5% 100VDC CER 0±30	28480	0160-3647
A1C81	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	28480	2130Y5V100R104Z
A1C82	0160-3608	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3608
A1C83	0180-2287	3		CAPACITOR-FXD 2.2UF ±10% 20VDC TA	28480	0180-2287
A1C84	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	28654	2130Y5V100R104Z
A1C85	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	28654	2130Y5V100R104Z
A1C86	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	28654	2130Y5V100R104Z
A1C87	0160-3602	6	1	CAPACITOR-FXD 150PF ±10% 100VDC CER	28480	0160-3602
A1C88	0150-0028	2	1	CAPACITOR-FXD 1PF ±20% 500VDC CER	28480	0150-0028
A1C89	0160-0154	5	1	CAPACITOR-FXD 2 200PF 200VDC MYLAR	28480	0160-0154
A1CR2	1901-0662	3	4	DIODE-PWR RECT 100V 6A	04713	MR751
A1CR3	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A1CR4	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A1CR5	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A1CR6	1906-0061	0	2	DIODE-FW BRDG 200V 2A	28480	1906-0061
A1CR7	1906-0061	0		DIODE-FW BRDG 200V 2A	28480	1906-0061
A1CR8	1901-0731	7	12	DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR9	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR11	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR12	1901-0040	1	14	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR13	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR14	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR15	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR16	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR17	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR18	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR19	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR20	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR22	1906-0048	9	3	DIODE-FW BRDG 100V 5A	28480	1906-0048
A1CR23	1906-0048	9		DIODE-FW BRDG 100V 5A	28480	1906-0048
A1CR24	1906-0048	9		DIODE-FW BRDG 100V 5A	28480	1906-0048
A1CR25	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR26	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR27	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR29	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR30	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR31	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR32	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A1CR33	1901-0047	8	12	DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR34	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR35	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR36	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR38	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR39	1901-0535	9	1	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1CR40	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR41	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR42	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR43	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR44	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR45	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR46	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR47	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR48	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR49	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR50	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR51	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR52	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR53	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR54	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR55	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR56	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A1CR57	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR58	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR59	1901-0050	3	1	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR60	1901-0731	7		DIODE-PWR RECT 400V	28480	1901-0731
A1E1	9170-0029	3	9	CORE-SHIELDING BEAD	28480	9170-0029
A1E2	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A1E3	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A1E4	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A1E5	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A1E6	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A1E7	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A1E8	1251-5839	7	2	CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-5839
A1E9	1251-5839	7		CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-5839
A1E10	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1E11	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A1F1	2110-0274	7	4	FUSE 3A 125V 281X 093	28480	2110-0274
A1F2	2110-0274	7		FUSE 3A 125V 281X 093	28480	2110-0274
A1F3	2110-0438	6	4	FUSE 7A 125V 281X 093	28480	2110-0438
A1F4	2110-0456	7	1	FUSE 10A 125V 281X 093	28480	2110-0456
A1F5	2110-0438	6		FUSE 7A 125V 281X 093	28480	2110-0438
A1F6	2110-0438	6		FUSE 7A 125V 281X 093	28480	2110-0438
A1F7	2110-0274	7		FUSE 3A 125V 281X 093	28480	2110-0274
A1F8	2110-0274	7		FUSE 3A 125V 281X 093	28480	2110-0274
A1F9	2110-0438	6		FUSE 7A 125V 281X 093	28480	2110-0438
A1H1	2200-0109	8	2	SCREW MACH 4-40 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1J1	1251-5880	7	1	CONNECTOR 16-PIN F POST TYPE	28480	1251-5889
A1J2	1251-5656	8	2	CONNECTOR 8-PIN M METRIC POST TYPE	28480	1251-5656
A1J3	1251-6544	3	3	CONTACT-CONN U/W-POST-TYPE MALE DPSLDR	28480	1251-6544
A1J4	1251-5571	8	2	CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A1J5	1251-4836	2	3	CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251-4836
A1J6	1251-6544	3		CONNECTOR	28480	1251-6544
A1J7	1251-4836	2		CONNECTOR 2 PIN M METRIC POST TYPE	28480	1251-4836
A1J8	1251-5656	8		CONNECTOR 8 PIN M METRIC POST TYPE	28480	1251-5656
A1J9	1251-4836	2		CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251-4836
A1J10	1251-6544	3		CONNECTOR	28480	1251-6544
A1J11	1250-1368	7	2	CONNECTOR-RF SMB M PC 50-OHM	28480	1250-1368
A1J12	1250-1368	7		CONNECTOR-RF SMB M PC 50-OHM	28480	1250-1368
A1J13	0360-1653	5	4	CONNECTOR-SGL CONT PIN 1 14-MM-BSC-SZ SQ	28480	0360-1653
A1J14	0360-1653	5		CONNECTOR-SGL CONT PIN 1 14-MM-BSC-SZ SQ	28480	0360-1653
A1J15	0360-1653	5		CONNECTOR-SGL CONT PIN 1 14-MM-BSC-SZ SQ	28480	0360-1653
A1J16	0360-1653	5		CONNECTOR-SGL CONT PIN 1 14-MM-BSC-SZ SQ	28480	0360-1653
A1J17	1251-5971	8		CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A1L1	9100-2698	8	4	INDUCTOR 80NH 6.25% X 26LG Q=35	28480	9100-2698
A1L2	9100-2698	3		INDUCTOR 80NH 6.25% X 26LG Q=35	28480	9100-2698
A1L3	9100-2250	9	4	INDUCTOR RF-CH-MLD 180NH 10% .105DX 26LG	28480	9100-2250
A1L4	9100-2250	9		INDUCTOR RF-CH-MLD 180NH 10% .105DX 26LG	28480	9100-2250
A1L5	9100-2252	1	4	INDUCTOR RF-CH-MLD 270NH 10% .105DX 26LG	28480	9100-2252
A1L6	9100-2252	1		INDUCTOR RF-CH-MLD 270NH 10% .105DX 26LG	28480	9100-2252
A1L8	9100-2258	7	2	INDUCTOR RF-CH-MLD 1.2UH 10% .105DX 26LG	28480	9100-2258
A1MP1	5041-3062	3	3	SUPPORT POST-CABLE	28480	5041-3062
A1MP2	1200-0185	9	4	INSULATOR-XSTR NYLON	28480	1200-0185
A1MP3	1205-0095	0	4	HEAT SINK SGL TO-5/TO-39-CS	30161	32258
A1MP4	0050-2005	6	1	HEAT SINK-VERT	28480	0050-2005
A1MP5	4040-1556	5	1	CONNECTOR-ELAS RET	28480	4040-1556
	4330-0145	9		BEADS-INDIAN, GREEN	28480	4330-0145
A1P1	1251-1686	6	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	28480	1251-1686
A1Q1	1854-0215	1	24	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q2	1884-0217	6	1	THYRISTOR-TRIAC	04713	MAC-10-2
A1Q3	1853-0336	5	4	TRANSISTOR PNP SI PD=625MW FT=60MHZ	04713	MPSA92
A1Q4	1853-0336	5		TRANSISTOR PNP SI PD=625MW FT=60MHZ	04713	MPSA92
A1Q5	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q6	1854-0575	6	2	TRANSISTOR NPN SI PD=625MW FT=60MHZ	04713	MPS A42
A1Q7	1853-0336	5		TRANSISTOR PNP SI PD=625MW FT=60MHZ	04713	MPSA92
A1Q8	1853-0336	5		TRANSISTOR PNP SI PD=625MW FT=60MHZ	04713	MPSA92
A1Q9	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q10	1854-0575	6		TRANSISTOR NPN SI PD=625MW FT=60MHZ	04713	MPS-A42
A1Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q12	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q14	1853-0354	7	8	TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q15	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q16	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q17	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q18	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q19	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q21	1853-0036	2	5	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1Q22	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q23	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A1Q30	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q31	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1Q32	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q33	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q34	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q35	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q36	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q37	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q38	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1Q39	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q40	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q41	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q42	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q43	1854 0392	5	3	TRANSISTOR NPN SI PD=310MW FT=60MHZ	04713	2N5068
A1Q44	1854 0392	5		TRANSISTOR NPN SI PD=310MW FT=60MHZ	04713	2N5068
A1Q45	1853-0316	1	1	TRANSISTOR DUAL PNP PD=500MW	28480	1853-0316
A1Q47	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q48	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q49	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1Q50	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q51	1853-0232	C	2	TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0232
A1Q52	1854 0419	7	2	TRANSISTOR NPN SI TO-39 PD=1W FT=200MHZ	28480	1854-0419
A1Q53	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1Q54	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q55	1853-0232	0		TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0232
A1Q56	1854-0419	7		TRANSISTOR NPN SI TO-39 PD=1W FT=200MHZ	28480	1854-0419
A1Q57	1854 0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q58	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1Q59	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1Q60	1854-0392	5		TRANSISTOR NPN SI PD=310MW FT=60MHZ	04713	2N5068
A1Q61	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1R1	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0±100	24546	C4-1/8-T0-2002-F
A1R2	0683-1005	5	2	RESISTOR 10 5% .25W CC	28480	0683-1005
A1R3	0757-0280	3	16	RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R4	0698-3454	9	1	RESISTOR 6.65K 1% .125W F TC=0±100	24546	C4-1/8-T0-6651-F
A1R5	0698-3612	4	1	RESISTOR 1.18K 1% .125W F TC=0±100	24546	C4-1/8-T0-1181-F
A1R6	0698-8647	6	1	RESISTOR 14.7K 1% .125W F TC=0±25	28480	0698-8647
A1R7	2100-3091	1	1	RESISTOR-TRMR 2K 10% C TOP-ADJ 17-TRN	32997	3292W-1-202
A1R8	0698-6360	6	3	RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A1R9	0757-0442	9	7	RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A1R10	0757-0851	4	1	RESISTOR 43.2K 1% .5W F TC=0±100	28480	0757-0851
A1R11	0757-0463	4	1	RESISTOR 82.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-8252-F
A1R12	0698-6619	6	5	RESISTOR 15K .1% .125W F TC=0±25	28480	0698-6619
A1R13	0757-0401	0	15	RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R14	0698-0001	0	1	RESISTOR 4.7 5% .5W CC TC=0+612	01121	EJ47G5
A1R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A1R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A1R18	0757-0841	2	1	RESISTOR 12.1K 1% .5W F TC=0±100	28480	0757-0841
A1R19	0757-0452	1	2	RESISTOR 27.4K 1% .125W F TC=0±100	24546	C4-1/8-T0-2742-F
A1R20	0698-6619	6		RESISTOR 15K .1% .125W F TC=0±25	28480	0698-6619
A1R21	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R22	0698-6254	7	1	RESISTOR 1.8 5% .5W CC TC=0+612	01121	EB18C5
A1R23	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A1R24	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R25	0811-1072	8	2	RESISTOR 39 5% 5W PW TC=0±800	28480	0811-1072
A1R26	0757-0273	4	2	RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A1R27	0698-6360	6		RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A1R28	0696-8210	9	1	RESISTOR 5.26K .25% .125W F TC=0±25	19701	MF4C1/8-T9 5261-C
A1R29	0811-1662	3	1	RESISTOR .47 5% 2W PW TC=0±800	75042	BWH2-47/100-J
A1R30	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A1R31	0698-6360	6		RESISTOR 10K .1% .125W F TC=0±25	28480	0698-6360
A1R32	0757-0439	4	3	RESISTOR 6.81K 1% .125W F TC=0±100	24546	C4-1/8-T0-6811-F
A1R33	0757-0438	3	4	RESISTOR 6.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-6111-F
A1R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R35	0698-6619	8		RESISTOR 15K .1% .125W F TC=0±25	28480	0698-6619
A1R36	0757-0433	8	3	RESISTOR 3.32K 1% .125W F TC=0±100	24546	C4-1/8-T0-3321-F
A1R37	0698-6619	8		RESISTOR 15K .1% .125W F TC=0±25	28480	0698-6619
A1R38	0757-0438	3		RESISTOR 6.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-6111-F
A1R39	0698-6619	8		RESISTOR 15K .1% .125W F TC=0±25	28480	0698-6619
A1R40	0698-7934	2	1	RESISTOR 12.1K 1% .125W F TC=0±25	19701	MF4C1/8-T9-1212-B
A1R42	0698-4399	7	2	RESISTOR 88.7 1% .125W F TC=0±100	24546	C4-1/8-T0-88R7-F
A1R43	0698-4399	7		RESISTOR 88.7 1% .125W F TC=0±100	24546	C4-1/8-T0-88R7-F
A1R44	0698-7199	1	1	RESISTOR 28.7 1% .05W F TC=0±100	28480	0698-7199
A1R45	0683-1015	7	1	RESISTOR 100 5% .25W CC	28480	0683-1015
A1R46	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R47	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R48	0757-0411	2	1	RESISTOR 332 1% .125W F TC=0±100	24546	C4-1/8-T0-332R-F
A1R49	2100-2216	0	1	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	73138	82PR5K
A1R50	2100-1966	9	3	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	73138	82PR1K
A1R5.	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0±100	24546	C4-1/8-T0-6811-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R53	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R54	0683-1005	5		RESISTOR 10 5% .25W CC	28480	0683-1005
A1R55	2100-1788	8	2	RESISTOR-TRMR 500 10% C TOP-ADJ 1-TRN	73138	82PR500
A1R56	2100-1788	8		RESISTOR-TRMR 500 10% C TOP-ADJ 1-TRN	73138	82PR500
A1R57	0698-7660	1	1	RESISTOR 61.9 1% .25W F TC=0±100	19701	MF52C1/4-T0-61R9-F
A1R58	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R59	0757-0465	6	9	RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R60	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R61	0698-7187	9	2	RESISTOR 23.7 1% .05W F TC=0±100	24546	C3-1/8-T00-23R7-G
A1R62	0699-0623	4	2	RESISTOR 10K 1% .5W C TC=0±250	28480	0699-0623
A1R63	0698-7197	9		RESISTOR 23.7 1% .05W F TC=0±100	24546	C3-1/8-T00-23R7-G
A1R64	0699-0623	4		RESISTOR 10K 1% .5W C TC=0±250	28480	0699-0623
A1R65	0683-2735	0	1	RESISTOR 27K 5% .25W CC	28480	0683-2735
A1R66	0757-0283	6	8	RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R67	0757-0317	7	1	RESISTOR 1.33K 1% .125W F TC=0±100	24546	C4-1/8-T0-1331-F
A1R69	0698-3439	4	7	RESISTOR 178 1% .125W F TC=0±100	24546	C4-1/8-T0-178R-F
A1R70	0698-3439	4		RESISTOR 178 1% .125W F TC=0±100	24546	C4-1/8-T0-178R-F
A1R71	0757-0412	3	3	RESISTOR 365 1% .125W F TC=0±100	24546	C4-1/8-T0-365R-F
A1R72	0[illegible]-3-4073	4	4	RESISTOR 1M 10% .125W CC TC=-600/+1137	01121	BB1051
A1R73	0[illegible]-7-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R74	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R75	0757-0281	4	2	RESISTOR 2.74K 1% .125W F TC=0±100	24546	C4-1/8-T0-2741-F
A1R76	0698-3439	4		RESISTOR 178 1% .125W F TC=0±100	24546	C4-1/8-T0-178R-F
A1R77	0698-3439	4		RESISTOR 178 1% .125W F TC=0±100	24546	C4-1/8-T0-178R-F
A1R78	0757-0412	3		RESISTOR 365 1% .125W F TC=0±100	24546	C4-1/8-T0-365R-F
A1R79	0757-0406	5	1	RESISTOR 182 1% .125W F TC=0±100	24546	C4-1/8-T0-182R-F
A1R80	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R81	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R83	2100-0580	7	1	RESISTOR-TRMR 500K 10% C TOP-ADJ 1-TRN	28480	2100-0580
A1R84	0757-0477	0	1	RESISTOR 332K 1% .125W F TC=0±100	19701	MF4C1/8-T0-3323-F
A1R85	2100-3252	8	1	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A1R86	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-2152-F
A1R87	0757-0399	5	1	RESISTOR 82.5 1% .125W F TC=0±100	28480	0757-0399
A1R88	0757-0444	1	2	RESISTOR 12.1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1212-F
A1R89	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R90	0698-3439	4		RESISTOR 178 1% .125W F TC=0±100	24546	C4-1/8-T0-178R-F
A1R91	0698-3439	4		RESISTOR 178 1% .125W F TC=0±100	24546	C4-1/8-T0-178R-F
A1R92	0757-0412	3		RESISTOR 365 1% .125W F TC=0±100	24546	C4-1/8-T0-365R-F
A1R93	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R94	0757-0419	0	4	RESISTOR 681 1% .125W F TC=0±100	24546	C4-1/8-T0-681R-F
A1R101	0757-0419	0		RESISTOR 681 1% .125W F TC=0±100	24546	C4-1/8-T0-681R-F
A1R102	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R103	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R104	2100-1738	9	1	RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	73138	82PR10K
A1R105	0757-0446	3	1	RESISTOR 15K 1% .125W F TC=0±100	24546	C4-1/8-T0-1502-F
A1R106	0757-0389	3	1	RESISTOR 33.2 1% .125W F TC=0±100	24546	C4-1/8-T0-33R2-F
A1R107	2100-2497	9	2	RESISTOR-TRMR 2K 10% C TOP-ADJ 1-TRN	73138	82PR2K
A1R108	0757-0435	0	2	RESISTOR 3.92K 1% .125W F TC=0±100	24546	C4-1/8-T0-3921-F
A1R109	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R110	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R114	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R115	0757-0442	0		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A1R116	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R117	0757-0462	1		RESISTOR 27.4K 1% .125W F TC=0±100	24546	C4-1/8-T0-2742-F
A1R118	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R119	0757-0346	2	10	RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R120	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R121	0757-0398	4	2	RESISTOR 75 1% .125W F TC=0±100	24546	C4-1/8-T0-75R0-F
A1R122	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R123	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R124	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R125	0757-0398	4		RESISTOR 75 1% .125W F TC=0±100	24546	C4-1/8-T0-75R0-F
A1R126	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R127	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R128	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R129	0757-0435	0		RESISTOR 3.92K 1% .125W F TC=0±100	24546	C4-1/8-T0-3921-F
A1R130	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R131	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R132	0757-0290	5	2	RESISTOR 6.19K 1% .125W F TC=0±100	19701	MF4C1/8-T0-6191-F
A1R133	0757-0451	0	1	RESISTOR 24.3K 1% .125W F TC=0±100	24546	C4-1/8-T0-2432-F
A1R134	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-5111-F
A1R135	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0±100	19701	MF4C1/8-T0-6191-F
A1R136	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R137	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R138	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R139	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R140	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R141	0757-0433	8		RESISTOR 3.32K 1% .125W F TC=0±100	24546	C4-1/8-T0-3321-F
A1R143	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R144	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R145	0757-0193	7	2	RESISTOR 3.32K 1% .5W F TC=0±100	28480	0757-0193
A1R147	0757-0193	7		RESISTOR 3.32K 1% .5W F TC=0±100	28480	0757-0193
A1R148	2100-1984	7	2	RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	73138	82PR100
A1R149	0757-0282	6	1	RESISTOR 221 1% .125W F TC=0±100	24546	C4-1/8-T0-221R-F
A1R150	0757-0427	0	4	RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A1R151	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A1R152	0757-0410	0		RESISTOR 681 1% .125W F TC=0±100	24546	C4-1/8-T0-681R-F
A1R153	0757-0419	0		RESISTOR 681 1% .125W F TC=0±100	24546	C4-1/8-T0-681R-F
A1R154	2100-3211	7	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A1R155	2100-2497	9		RESISTOR-TRMR 2K 10% C TOP-ADJ 1-TRN	73138	82PR2K
A1R156	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R157	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R158	0761-0006	0	2	RESISTOR 10K 5% 1W MO TC=0±200	28480	0761-0006
A1R160	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A1R160	0757-0417	8	2	RESISTOR 562 1% .125W F TC=0±100	24546	C4-1/8-T0-562R-F
A1R161	0761-0028	6	2	RESISTOR 12K 5% 1W MO TC=0±200	28480	0761-0028
A1R162	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R163	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R164	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A1R165	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A1R166	0761-0006	0		RESISTOR 10K 5% 1W MO TC=0±200	28480	0761-0006
A1R167	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A1R168	0757-0417	8		RESISTOR 562 1% .125W F TC=0±100	24546	C4-1/8-T0-562R-F
A1R169	0761-0028	6		RESISTOR 12K 5% 1W MO TC=0±200	28480	0761-0028
A1R170	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R171	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A1R172	0698-3440	7	1	RESISTOR 196 1% .125W F TC=0±100	24546	C4-1/8-T0-196R-F
A1R173	0683-4705	8	2	RESISTOR 47 5% .25W CC	28480	0683-4705
A1R174	0683-4705	8		RESISTOR 47 5% .25W CC	28480	0683-4705
A1R175	2100-1988	9		RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	73138	82PR1K
A1R176	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A1R177	0757-0434	9	1	RESISTOR 3.65K 1% .125W F TC=0±100	24546	C4-1/8-T0-3651-F
A1R178	0757-0416	7	3	RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A1R179	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A1R180	2100-1986	9		RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	73138	82PR1K
A1R181	0757-0281	4		RESISTOR 2.74K 1% .125W F TC=0±100	24546	C4-1/8-T0-2741-F
A1R182	0757-0433	8		RESISTOR 3.32K 1% .125W F TC=0±100	24546	C4-1/8-T0-3321-F
A1R183	0757-0474	7	1	RESISTOR 243K 1% .125W F TC=0±100	24546	C4-1/8-T0-2433-F
A1R184	2100-1984	7		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	73138	82PR100
A1R185	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R187	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R190	0811-1072	9		RESISTOR 39 5% 5W PW TC=0±800	28480	0811-1072
A1R191	0698-3159	5	1	RESISTOR 26.1K 1% .125W F TC=0±100	24546	C4-1/8-T0-2612-F
A1R193	0698-7264	9	1	RESISTOR 6.62K 1% .05W F TC=0±100	24546	C3-1/8-T0-6621-G
A1R194	0698-4073	4		RESISTOR 1M 10% .125W CC TC=-600/+1137	01121	BB1051
A1R195	0698-4073	4		RESISTOR 1M 10% .125W CC TC=-600/+1137	01121	BB1051
A1R196	0698-4073	4		RESISTOR 1M 10% .125W CC TC=-600/+1137	01121	BB1051
A1R198	0683-2215	1	5	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A1R199	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A1R200	0683-2215	1		RESISTOR 200 5% .25W FC TC=-400/+600	01121	CB2215
A1R201	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A1R204	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-5111-F
A1R205	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A1R206	0757-0444	1		RESISTOR 12.1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1212-F
A1R207	0698-7235	6	2	RESISTOR 909 1% .05W F TC=0±100	24546	C3-1/8-T0-909R-G
A1R208	0698-7235	6		RESISTOR 909 1% .05W F TC=0±100	24546	C3-1/8-T0-909R-G
A1R209	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A1R210	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A1R211	0811-1746	4	2	RESISTOR 36 5% 2W PW TC=0±800	75042	BWH2-36/100-J
A1R212	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R213	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R214	0811-1746	4		RESISTOR 36 5% 2W PW TC=0±600	75042	BWH2-36/100-J
A1R215	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A1R216	0811-2771	7	1	RESISTOR 18.3% 2W PW TC=0±90	28480	0811-2771
A1R217	0683-3905	8	1	RESISTOR 39 5% .25W CC	28480	0683-3905
A1R218	0698-0084	9	1	RESISTOR 2.16K 1% .125W F TC=0±100	24546	C4-1/8-T0-2161-F
A1R219	0757-0417	8	1	RESISTOR 562 1% .125W F TC=0±100	24546	C4-1/8-T0-562R-F
A1R220	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A1R221	0698-3433	4	1	RESISTOR 178 1% .125W F TC=0±100	24546	C4-1/8-T0-178R-F
A1R222	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R223	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0±100	24546	C4-1/8-T0-2371-F
A1R224	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0±100	24546	C4-1/8-T0-1621-F
A1R225	0698-0082	7	1	RESISTOR 464 1% .125W F TC=0±100	24546	C4-1/8-T0-4640-F
A1R226	0698-3443	0	2	RESISTOR 287 1% .125W F TC=0±100	24546	C4-1/8-T0-287R-F
A1R227	0698-3443	0		RESISTOR 287 1% .125W F TC=0±100	24546	C4-1/8-T0-287R-F
A1R228	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0±100	24546	C4-1/8-T0-6811-F
A1R229	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	C3-1/8-T0-5111-F
A1R230	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0±100	24546	C3-1/8-T0-1501-F
A1R231	2100-2650	6	1	RESISTOR 200K RVCMT	28420	2100-2650
A1R232	0698-7203	8	2	RESISTOR 42.2 1% .05W F TC=0±100	24546	C3-1/8-T00-42R2-G
A1R233	0698-7203	8		RESISTOR 42.2 1% .05W F TC=0±100	24546	C4-1/8-T00-42R2-G
A1R234	0757-0464	3	1	RESISTOR 33.2K 1% .125W F	24564	C4-1/8-T0-3322
A1RT1	0837-0035	6	1	THERMISTOR DISC 5K-OHM TC=-4.4%/C-DEG	28480	0837-0035
A1RT2	0837-0089	4	2	THERMISTOR DISC 100-OHM TC=+4.4%/C-DEG	28480	0837-0089
A1RT3	0837-0089	4		THERMISTOR DISC 100-OHM TC=+4.4%/C-DEG	28480	0837-0089
A1RT4	0837-0215	4	1	THERMISTOR DISC 10 OHM	28480	0837-0215
A1U1	1826-0433	0	1	IC OP AMP GP 8-DIP-P PKG	03406	L5356BN
A1U2	1826-0271	0	6	IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U3	1826-0271	0		IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U4	1826-0271	0		IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U5	1826-0271	0		IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U6	1826-0271	0		IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A1U7	1826-0254	9	1	IC OP AMP H-SLEW-RATE 8 DIP-P PKG	04713	MC1741SCP1
A1U8	1826-0271	0		IC OP AMP GP 8 DIP-P PKG	01295	SN72741P
A1U9	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
A1U10	1820-1448	3	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S09N
A1U11	1NA9-0006	1	1	IC-OUTPUT AMPLIFIER	28480	1NA9-0006
A1U12	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P PKG	01295	SN72311P
A1VR1	1902-1350	0	2	DIODE-ZNR 1N5364B 33V PD=5W TC=±5%	28480	1902-1350
A1VR2	1902-1350	0		DIODE-ZNR 1N5364B 33V PD=5W TC=±5%	28480	1902-1350
A1VR3	1902-0680	7	1	DIODE-ZNR 1N827 6.2V 5% DO-7 PD=.4W	24046	1N827
A1VR4	1902-3256	9	2	DIODE-ZNR 23.7V 5% DO-35 PD=.4W	28480	1902-3256
A1VR5	1902-3070	5	1	DIODE-ZNR 4.22V 5% DO-35 PD=.4W	28480	1902-3070
A1VR6	1902-3256	9		DIODE-ZNR 23.7V 5% DO-35 PD=.4W	28480	1902-3256
A1VR7	1902-0049	2	2	DIODE-ZNR 6.19V 5% PD=.4W	28480	1902-0049
A1VR8	1902-0049	2	2	DIODE-ZNR 6.19V 5% PD=.4W	28480	1902-0049
A1XA7	1251-6988	6	1	CONNECTOR-20-CIRCUITS	28480	1251-6988
A1XU9	1200-0638	7	2	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU10	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	01980-66540	8	1	HIGH VOLTAGE BOARD ASSEMBLY	28480	01980-66540
A2C1	0160-0644	7	2	CAPACITOR-FXD .022UF ±20% 4KVDC	28480	0160-0644
A2C2	0160-0684	5	1	CAPACITOR-FXD .068UF ±20% 4KVDC	56289	430P683040
A2C3	0160-0684	6	3	CAPACITOR-FXD 1000PF ±20% 4KVDC	28480	0160-0684
A2C4	0160-4061	9	3	CAPACITOR-FXD .01UF ±20% 4KVDC	28480	0160-4061
A2C5	0160-4061	9		CAPACITOR-FXD .01UF ±20% 4KVDC	28480	0160-4061
A2C6	0160-3665	0	2	CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A2C7	0160-0684	6		CAPACITOR-FXD 1000PF ±20% 4KVDC	28480	0160-0684
A2C8	0160-0164	7	1	CAPACITOR-FXD .039UF ±10% 200VDC POLYE	28480	0160-0164
A2C9	0180-0269	6	1	CAPACITOR-FXD 1UF+50-10% 150VDC AL	56289	30D106G150DA2
A2C10	0160-3665	9		CAPACITOR-FXD .01UF +80-20% 500VDC CER	28480	0160-3665
A2C11	0160-0684	6		CAPACITOR-FXD 1000PF ±20% 4KVDC	28480	0160-0684
A2C12	0160-4061	9		CAPACITOR-FXD .01UF ±20% 4KVDC	28480	0160-4061
A2C13	0160-0644	7		CAPACITOR-FXD .022UF ±20% 4KVDC	28480	0160-0644
A2CR1	1901-0683	8	1	DIODE-HV RECT 10KV 5MA 230NS	28480	1901-0683
A2CR2	1901-0028	5	8	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR3	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR4	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR5	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR6	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR7	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR8	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2CR9	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A2H1	2360-0275	7	4	SCREW-MACH 6-32 .25-IN-LG BDG-HD-SLT	00000	ORDER BY DESCRIPTION
A2J1	1251-6000	6	1	CONNECTOR 5-PIN M METRIC POST TYPE	28480	1251-6000
A2MP1	0340-0007	9	2	STANDOFF-RND .5-IN-LG 6-32THD .5-IN-OD	00000	ORDER BY DESCRIPTION
A2R1	0683-1045	5	1	RESISTOR 100K 5% .25W FC TC=-400/+800	28480	0683-1045
A2R2	0686-4725	8	1	RESISTOR 4.7K 5% .5W CC TC=0+647	28480	0686-4725
A2R3	0684-1021	7	8	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R4	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R5	0683-2255	8	1	RESISTOR 2.2M 5% .25W FC TC=-900/+1100	28480	0683-2255
A2R6	0698-8016	5	1	RESISTOR 30M 1% .3W C TC=0+100	03883	PVC1/5-3 TO 3004 F
A2R7	0686-1065	3	2	RESISTOR 10M 5% .5W CC TC=0+1059	28480	0686-1065
A2R8	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R9	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R10	0686-1055	1	1	RESISTOR 1M 5% .5W CC TC=0+1000	28480	0686-1055
A2R11	0686-2225	8	1	RESISTOR 2.2K 5% .5W CC TC=0+647	28480	0686-2225
A2R12	0686-5605	5	2	RESISTOR 56 5% .5W CC TC=0+412	28480	0686-5605
A2R13	0686-1015	3	1	RESISTOR 100 5% .5W CC TC=0+529	28480	0686-1015
A2R14	2100-3253	7	1	RESISTOR-TRMR 50K 10% C TOP ADJ 1-TRN	28480	2100-3253
A2R15	0698-3152	0	1	RESISTOR 46.4K 1% .125W F TC=0+100	24546	C4-1/8-TO-4642-F
A2R16	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R17	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R18	0686-5605	5		RESISTOR 56 5% .5W CC TC=0+412	28480	0686-5605
A2R19	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R20	0686-1065	3		RESISTOR 10M 5% .5W CC TC=0+1059	28480	0686-1065
A2R21	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A2R22	0686-5665	5	1	RESISTOR 5.6M 5% .5W CC TC=0+1000	01121	EB5665
A2R23	0698-8995	7	1	RESISTOR 10M 5% 1W C TC=0+250	28480	0698-8995
A2R24	2100-3831	8	1	RESISTOR-TRMR 2M 20% C TOP ADJ 1-TRN	02111	83P206
A2R25	0699-0170	6	1	RESISTOR 13M 5% 1W C TC=0+250	28480	0699-0170
A2TP1	1251-7550	3	1	CONNECTOR-SGL CONT SKT .04 IN BSC-SZ RND	28480	1251-7550
A2TP2	1251-0206	2	2	CONNECTOR-SGL CONT SKT .04-IN-BSC-SZ RND	28480	1251-0206
A2TP3	1251-0206	2		CONNECTOR-SGL CONT SKT .04-IN-BSC-SZ RND	28480	1251-0206
A2V1	2140-0013	5	3	LAMP-GLOW 70VDC 300UA T-2 BULB	28480	2140-0013
A2V2	2140-0013	5		LAMP-GLOW 70VDC 300UA T-2 BULB	28480	2140-0013
A2V3	2140-0018	0	2	LAMP-GLOW A9A CT 90VDC 700UA T-2 BULB	0046G	A9A CT
A2V4	2140-0018	0		LAMP-GLOW A9A CT 90VDC 700UA T-2 BULB	0046G	A9A CT
A2VR5	2140-0013	5		LAMP-GLOW 70VDC 300UA T-2 BULB	28480	2140-0013
A2VR1	1902-0184	6	1	DIODE-ZNR 16.2V 5% DO-35 PD=.4W	28480	1902-0184
A2A1	01980-66529	9	1	TRANSFORMER ASSEMBLY HV	28480	01980-66529
A2A1C1	0160-2264	2	2	CAPACITOR-FXD 20PF ±5% 500VDC CER 0+30	28480	0160-2264
A2A1C2	0160-2264	2		CAPACITOR-FXD 20PF ±5% 500VDC CER 0+30	28480	0160-2264
A2A1R1	0687-3941	0	2	RESISTOR 390K 10% .5W CC TC=0+882	01121	EB3941
A2A1R2	0687-3941	0		RESISTOR 390K 10% .5W CC TC=0+882	01121	EB3941

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	01980-66503	9	1	GATE OSCILLOSCOPE BOARD ASSEMBLY	28480	01980 66503
A3A21	1251-7146	2	1	CONNECTOR-PC EDGE 36-CONT/ROW 2-ROWS	28480	1251-7146
A3A22	1251-7146	3	2	CONNECTOR-PC EDGE 20 CONT/ROW 2-ROWS	28480	1251-7146
A3C1	0160-3622	8	6	CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y6V100R104Z
A3C2	0160-3508	0	3	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160 3508
A3C3	0160-2307	4	2	CAPACITOR-FXD 47PF ±5% 300VDC MICA	28480	0160 2307
A3C4	0160-2055	0	4	CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160 2055
A3C5	0160-3665	9	2	CAPACITOR-FXD 01UF +80-20% 50VDC CER	28480	0160 3665
A3C6	0121-0474	0	2	CAPACITOR-V TRMR-PSTN 3-1 6PF 600V	28480	0121-0474
A3C7	0160-2197	0	1	CAPACITOR-FXD 10PF ±5% 300VDC MICA	28480	0160-2197
A3C8	0180-2255	3	8	CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180-2255
A3C9	0160-3665	9		CAPACITOR-FXD 01UF +80-20% 500VDC CER	28480	0160 3665
A3C10	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A3C11	0121-0474	0		CAPACITOR-V TRMR-PSTN 3-1 6PF 600V	28480	0121 0474
A3C12	0160-0166	8	2	CAPACITOR-FXD 066UF ±10% 200VDC POLYE	28480	0160-0166
A3C13	0160-2307	4		CAPACITOR-FXD 47PF ±5% 300VDC MICA	28480	0160 2307
A3C14	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A3C15	0160-2055	9		CAPACITOR-FXD 01UF +80-20% 100VDC CER	28480	0160-2055
A3C16	0180-2255	3		CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180-2255
A3C17	0180-2255	3		CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180-2255
A3C18	0160-3622	8		CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y6V100R104Z
A3C19	0160-3622	8		CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y6V100R104Z
A3C20	0160-3622	8		CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y6V100R104Z
A3C21	0180-0229	7	2	CAPACITOR-FXD 33UF±10% 10VDC TA	56289	150D336X9010B2
A3C22	0180-0229	7		CAPACITOR-FXD 33UF±10% 10VDC TA	56289	150D336X9010B2
A3C23	0180-2255	3		CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180-2255
A3C24	0160-3470	4	4	CAPACITOR-FXD 01UF +80-20% 50VDC CER	28480	0160 3470
A3C25	0180-2255	3		CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180-2255
A3C27	0180-2255	3		CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180 2255
A3C28	0180-2255	3		CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180 2255
A3C29	0180-2255	3		CAPACITOR-FXD 2 2UF±20% 20VDC TA	28480	0180 2255
A3C30	0160-3470	4		CAPACITOR-FXD 01UF +80-20% 50VDC CER	28480	0160 3470
A3C31	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160 3508
A3C32	0160-0166	9		CAPACITOR-FXD 066UF ±10% 200VDC POLYE	28480	0160 0166
A3C33	0180 0141	2	1	CAPACITOR-FXD 60UF+75-10% 50VDC AL	56289	300506G050CD2
A3C34	0160-0166	8		CAPACITOR-FXD 066UF ±10% 200VDC POLYE	28480	0160 0166
A3C35	0160-3452	2	1	CAPACITOR-FXD 02UF ±20% 100VDC CER	28480	0160 3452
A3C36	0160-3622	8		CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y6V100R104Z
A3C37	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C38	0160-3622	8		CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y6V100R104Z
A3C39	0160-3470	4		CAPACITOR-FXD 01UF +80-20% 50VDC CER	28480	0160-3470
A3C40	0160-3470	4		CAPACITOR-FXD 01UF +80-20% 50VDC CER	28480	0160-3470
A3CR1	1901 0040	1	8	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901 0040
A3CR2	1901-0026	3	6	DIODE-PWR RECT 200V 750MA DO-29	28480	1901 0026
A3CR3	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901 0026
A3CR6	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR7	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR8	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901 0040
A3CR9	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A3CR10	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A3CR11	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A3CR12	1901 0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901 0026
A3CR13	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR14	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901 0040
A3CR15	1901 0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901-0026
A3CR16	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901 0026
A3CR17	1901-0026	3		DIODE-PWR RECT 200V 750MA DO-29	28480	1901 0026
A3E1	2110-0269	0	2	FUSEHOLDER-CLIP TYPE 250-FUSE	28480	2110 0269
A3E2	2110-0269	0		FUSEHOLDER-CLIP TYPE 250-FUSE	28480	2110 0269
A3E3	9170 0759	6	3	CORE-SHIELDING BEAD	28480	9170 0759
A3E4	9170-0759	6		CORE-SHIELDING BEAD	28480	9170 0759
A3E5	9170-0759	6		CORE-SHIELDING BEAD	28480	9170 0759
A3E6	9170-0029	3	1	CORE-SHIELDING BEAD	28480	9170 0029
A3F1	2110-0007	4	1	FUSE 1A 250V TD 1 25X 25 UL	75915	313001
A3J1	1251-6572	7	1	CONNECTOR	28480	1251 6572
A3J2	1251-6573	8	1	CONNECTOR	28480	1251-6573
A3J3	1251-6322	6	1	CONNECTOR 10-PIN M METRIC POST TYPE	28480	1251-6322
A3J4	1251-6568	3	1	CONNECTOR 9-PIN M METRIC POST TYPE	28480	1251 6568
A3J5	1251-6000	6	2	CONNECTOR 6-PIN M METRIC POST TYPE	28480	1251 6000
A3J6	1251-4836	2	2	CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251 4836
A3J7	1251-5971	8	1	CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A3J8	1251-4836	2		CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251-4836
A3J9	1251-6000	6		CONNECTOR 6-PIN M METRIC POST TYPE	28480	1251 6000

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3L1	9140-0171	3	1	INDUCTOR RF-CH-MLD 40UH 10% 296DX.866LG	28480	9140-0171
A3L2	9100-1641	0	1	INDUCTOR RF-CH-MLD 240UH 5% 166DX.385LG	28480	9100-1641
A3MP1	1206-0065	0	4	HEAT SINK SGL TO-5/TO-39-CS	30161	32255
A3MP6	1200-0185	8	4	INSULATOR-XSTR NYLON	28480	1200-0185
A3MP9	5041-3062	3	1	SUPPORT POST-CABLE	28480	5041-3062
A3P1	1251-5942	3		CONNECTOR-PC EDGE 20-CONT/ROW 2-ROWS	28480	1251-5942
A3Q1	1854-0215	1	21	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q2	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q3	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q4	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q5	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q6	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q7	1853-0036	2	4	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A3Q8	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q9	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q10	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q12	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q13	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q14	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q15	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q16	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q17	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q18	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q19	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q20	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q21	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A3Q22	1853-0232	0	2	TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0232
A3Q23	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q24	1854-0419	7	2	TRANSISTOR NPN SI TO-39 PD=1W FT=200MHZ	28480	1854-0419
A3Q25	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A3Q26	1853-0232	0		TRANSISTOR PNP SI TO-39 PD=1W FT=200MHZ	28480	1853-0232
A3Q27	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A3Q28	1854-0419	7		TRANSISTOR NPN SI TO-39 PD=1W FT=200MHZ	28480	1854-0419
A3Q30	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A3R1	0757-0401	0	10	RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R2	0757-0429	2	1	RESISTOR 1.82K 1% .125W F TC=0±100	24546	C4-1/8-T0-1021-F
A3R3	0757-0283	6	8	RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R4	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R5	0757-0435	0	1	RESISTOR 3.92K 1% .125W F TC=0±100	24546	C4-1/8-T0-3921-F
A3R6	0757-0479	2	2	RESISTOR 392K 1% .125W F TC=0±100	19701	MF4C1/8-T0-3923-F
A3R7	0757-0472	5	1	RESISTOR 200K 1% .125W F TC=0±100	24546	C4-1/8-T0-2003-F
A3R8	0757-0465	6	7	RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A3R9	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R10	0757-0449	6	2	RESISTOR 20K 1% .125W F TC=0±100	24546	C4-1/8-T0-2002-F
A3R11	0757-0431	6	1	RESISTOR 2.43K 1% .125W F TC=0±100	24546	C4-1/8-T0-2431-F
A3R12	0757-0416	7	3	RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A3R13	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R14	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R15	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R16	2100-2497	9	1	RESISTOR-TRMR 2K 10% C TOP-ADJ 1-TRN	73138	82PR2K
A3R17	0757-0346	2	6	RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R18	0757-0427	0	2	RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A3R19	0757-0442	9	11	RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R21	0698-3160	8	1	RESISTOR 31.6K 1% .125W F TC=0±100	24546	C4-1/8-T0-3162-F
A3R22	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0±100	24546	C4-1/8-T0-681R-F
A3R23	2100-3211	7	2	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A3R24	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A3R25	0761-0006	0	7	RESISTOR 10K 5% 1W MO TC=0±200	28480	0761-0006
A3R26	0757-0280	3	8	RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R27	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R28	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A3R29	0761-0028	6	2	RESISTOR 12K 5% 1W MO TC=0±200	28480	0761-0028
A3R30	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R31	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R32	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R34	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R35	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R36	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R37	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0±100	24546	C4-1/8-T0-6811-F
A3R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R39	0757-0427	0	1	RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A3R42	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R43	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R44	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R45	0757-0442	8		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R46	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R47	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R48	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R49	0757-0442	8		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R50	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R51	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R52	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R53	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R54	0757-0278	9	1	RESISTOR 1.78K 1% .125W F TC=0±100	24546	C4-1/8-T0-1781-F
A3R55	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R56	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R57	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R58	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A3R59	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0±100	24546	C4-1/8-T0-51R1-F
A3R60	2100-2061	3	1	RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	73138	82PR200
A3R61	0757-0466	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A3R62	0757-0200	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R63	2100-3211	7		RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A3R64	0761-0006	0		RESISTOR 10K 5% 1W MO TC=0±200	28480	0761-0006
A3R65	0757-0442	8		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R66	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A3R67	0761-0028	6		RESISTOR 12K 5% 1W MO TC=0±200	28480	0761-0028
A3R68	0757-0[illegible]4	[illegible]		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R69	0698-3445	2	1	RESISTOR 348 1% .125W F TC=0±100	24546	C4-1/8-T0-348R-F
A3R70	0757-040[illegible]	3	1	RESISTOR 130 1% .125W F TC=0±100	24546	C4-1/8-T0-131-F
A3R71	0757-0449	6		RESISTOR 20K 1% .125W F TC=0±100	24546	C4-1/8-T0-2002-F
A3R72	0757-0124	4	1	RESISTOR 39.2K 1% .125W F TC=0±100	28480	0757-0124
A3R[illegible]	0757-0463	4	1	RESISTOR 82.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-8252-F
A3R[illegible]4	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A3R75	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R76	0698-3159	5	1	RESISTOR 26.1K 1% .125W F TC=0±100	24546	C4-1/8-T0-2612-F
A3R77	0757-0442	8		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R78	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R79	0757-0440	7	2	RESISTOR 7.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-7501-F
A3R80	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-7501-F
A3R81	0757-0478	1	1	RESISTOR 365K 1% .125W F TC=0±100	19701	MF4C1/8-T0-3653-F
A3R82	0757-0484	8	1	RESISTOR 619K 1% .125W F TC=0±100	28480	0757-0484
A3R83	2100-3213	0	1	RESISTOR-TRMR 200K 10% C TOP-ADJ 1-TRN	28480	2100-3213
A3R84	0757-0466	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A3R85	0684-1011	5	1	RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011
A3R86	0683-2265	1	1	RESISTOR 22M 5% .25W FC TC=-900/+1200	01121	CB2265
A3R87	0684-1211	7	1	RESISTOR 1[illegible] 10% .25W FC TC=-400/+600	01121	CB1211
A3R88	0757-0466	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A3R89	0757-0479	2		RESISTOR 392K 1% .125W F TC=0±100	19701	MF4C1/8-T0-3923-F
A3R90	0687-3911	4	1	RESISTOR 390 10% 5W CC TC=0±529	01121	EB3911
A3R91	0684-4711	8	1	RESISTOR 470 10% .25W FC TC=-400/+600	01121	CB4711
A3R92	2100-3253	7	1	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	2100-3253
A3R93	2100-0658	9	1	RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	28480	2100-0658
A3R94	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A3R95	0757-0442	8		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R96	0757-0442	8		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A3R97	0757-0465	6		RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A3R98	2100-3214	0	1	RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	28480	2100-3214
A3R99	0757-0346	2		RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A3R100	0684-1021	7	2	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A3R101	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A3R106	0698-5422	9	1	RESISTOR 5.6K 10% .125W CC TC=-250/+857	01121	BB5621
A3S1	3101-0973	5	1	SWITCH-SL DPDT MINTR 5A 125VAC/DC PC	28480	3101-0973
A3U1	1826-0167	3	1	IC OP AMP PRGMBL TO-99 PKG	01928	CA3094AT
A3U2	1826-0271	0	2	IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A3U3	1820-1682	3	1	IC SHF-RGTR CMOS SERIAL-IN PRL-[illegible] 8-BIT	01928	CD4004BE
A3U4	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U5	1820-1196	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A3U6	1826-0271	0		IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A3U7	1820-1934	2	1	IC CONV 8-B D/A 16-DIP-C PKG	06665	DAC-08EQ
A3U8	1820-1858	9	1	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A3U13	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U14	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3VR2	1902-3323	1	1	DIODE ZNR 42.2V 5% DO-35 PD=.4W TC=+.06%	28480	1902-3323

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3XA21	1251-6941	2	1	CONNECTOR PC EDGE 35-CONT/ROW 2-ROWS	28480	1251-6941
A3XA22	1251-6942	3	1	CONNECTOR PC EDGE 20-CONT/ROW 2-ROWS	28480	1251-6942
A3XU2	1200-0796	8	2	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A3XU3	1200-0607	0	3	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU4	1200-0638	7	3	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A3XU5	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A3XU6	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A3XU7	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU8	1200-0639	8	1	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU9	1200-0830	1	4	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0830
A3XU10	1200-0830	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0830
A3XU11	1200-0830	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0830
A3XU12	1200-0830	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0830
A3XU13	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A3XU14	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	01980-66547	1	1	PROCESSOR BOARD ASSEMBLY	28480	01980-66547
A4C5	0160-3470	4	44	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C6	0180-0374	3	2	CAPACITOR-FXD 10UF±10% 20VDC TA	56289	1500106X902082
A4C7	0180-0374	3		CAPACITOR-FXD 10UF±10% 20VDC TA	56289	1500106X902082
A4C8	0180-0197	8	2	CAPACITOR-FXD 2.2UF±10% 20VDC TA	56289	1500225X9020A2
A4C9	0180-0197	8		CAPACITOR-FXD 2.2UF±10% 20VDC TA	56289	1500225X9020A2
A4C10	0180-0230	0	2	CAPACITOR-FXD 1UF±20% 50VDC TA	56289	1500106X0050A2
A4C11	0180-0230	0		CAPACITOR-FXD 1UF±20% 50VDC TA	56289	1500106X0050A2
A4C13	0180-0228	6	9	CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C14	0180-1746	5	2	CAPACITOR-FXD 15UF±10% 20VDC TA	56289	1500156X902082
A4C15	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C16	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C17	0180-1746	5		CAPACITOR-FXD 15UF±10% 20VDC TA	56289	1500156X902082
A4C18	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C19	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C20	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C21	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C28	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C29	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C30	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C31	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C32	0160-3443	1	5	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C40	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V PC-MTG	52763	304322 5.5-18PF NPO
A4C41	0160-3587	0	1	CAPACITOR-FXD 10PF ±5% 100VDC CER 0.30	28480	0160-3587
A4C42	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C43	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C45	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C46	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C47	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C49	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C50	0180-0068	0	1	CAPACITOR-FXD 50UF+75-10% 25VDC AL	56289	300506G025CC2
A4C51	0160-3443	1		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3443
A4C90	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C91	0180-0228	6		CAPACITOR-FXD 22UF±10% 15VDC TA	56289	1500226X9015B2
A4C100	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C101	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C102	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C103	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C104	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C105	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C106	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C107	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C108	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C109	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C110	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C111	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C112	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C113	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C114	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C115	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C116	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C117	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C118	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C119	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C120	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C121	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C122	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C123	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C124	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C125	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C126	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C127	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C128	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C129	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C130	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C131	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C132	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C133	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C134	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4C135	0160-3470	4		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A4CR1	1901-0040	1	13	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040

See introduction to this section for ordering information

Table 6-2, Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4CR10	1901-0535	8	1	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A4CR13	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR14	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR15	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR16	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR17	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR18	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR19	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR20	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4E1	9170-0759	6	10	CORE-SHIELDING BEAD	28480	9170-0759
A4E2	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E3	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E4	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E5	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E7	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E8	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E9	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E10	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E11	9170-0759	6		CORE-SHIELDING BEAD	28480	9170-0759
A4E12	1251-6094	8	1	CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6094
A4H1	2200-0170	3	4	SCREW-MACH 4-40 .[illegible] IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A4J2	1251-6571	6	1	CONNECTOR 34-PIN M POST TYPE	28480	1251-6571
A4J4	1251-6574	9	1	CONNECTOR 14-PIN M POST TYPE	28480	1251-6574
A4J5	1251-6572	7	2	CONNECTOR 26-PIN M POST TYPE	28480	1251-6572
A4J6	1251-6578	3	2	CONNECTOR 34-PIN M POST TYPE	28480	1251-6578
A4J7	1251-6578	3		CONNECTOR 34-PIN M POST TYPE	28480	1251-6578
A4J8	1251-4837	3	1	CONNECTOR 4-PIN M METRIC POST TYPE	28480	1251-4837
A4J9	1200-0607	0	11	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4J10	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4J11	1251-6573	8	1	CONNECTOR 20-PIN M POST TYPE	28480	1251-6573
A4J12	1251-6572	7		CONNECTOR 26-PIN M POST TYPE	28480	1251-6572
A4L1	9140-0029	0	2	INDUCTOR RF-CH-MLD 100UH 10% .250X.313LG	28480	9140-0029
A4L3	9140-0105	3	1	INDUCTOR RF-CH-MLD 8.2UH 10%	28480	9140-0105
A4L4	9140-0029	0		INDUCTOR RF-CH-MLD 100UH 10% .250X.313LG	28480	9140-0029
A4MP1	5041-1550	0	1	HOUSING-SUBSTRAIT	28480	5041-1550
A4MP2	01980-04106	8	1	COVER-HYBRID	28480	01980-04106
A4MP3	5041-3062	3	1	SUPPORT POST-CABLE	28480	5041-3062
A4MP4	1200-0185	[illegible]	1	INSULATOR-TRANSISTOR	28480	1200-0185
A4P1	1251-6901	8	1	CONNECTOR-PC EDGE 40-CONT/ROW 2-ROWS	28480	1251-6903
A4Q1	1854-0471	2	6	TRANSISTOR NPN SI DARL PD=600MW	04713	MPS-A14
A4Q2	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A4Q3	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A4Q4	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A4Q5	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A4Q6	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A4Q7	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A4Q8	1854-0472	2		TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A4Q9	1854-0215	1	7	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q10	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q11	1853-0036	2	4	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q12	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q15	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q16	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4Q18	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q19	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q20	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q21	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4Q22	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A4R1	0757-0280	3	6	RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-TO-1001-F
A4R3	0757-1094	9	8	RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-TO-1471-F
A4R6	0757-0434	9	2	RESISTOR 3.65K 1% .125W F TC=0±100	24546	C4-1/8-TO-3651-F
A4R7	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-TO-1471-F
A4R8	0698-3153	9	1	RESISTOR 3.83K 1% .125W F TC=0±100	24546	C4-1/8-TO-3831-F
A4R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-TO-1001-F
A4R10	0757-0438	3	3	RESISTOR 5.11K 1% .125W F TC=0±100	24546	C4-1/8-TO-5111-F
A4R11	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	C4-1/8-TO-5111-F
A4R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-TO-1001-F
A4R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-TO-1001-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R17	0757-0283	6	7	RESISTOR 2K 1% 125W F TC=0±100	24546	C4-1/8-T0 2001-F
A4R18	0698-3085	0	1	RESISTOR 2.61K 1% .125W F TC=0±100	24546	C4-1/8-T0-2611-F
A4R21	0698-3160	8	1	RESISTOR 31.6K 1% .125W F TC=0±100	24546	C4-1/8-T0-3162-F
A4R22	0698-3157	3	1	RESISTOR 19.6K 1% .125W F TC=0±100	24546	C4-1/8-T0-1962-F
A4R24	0757-0273	4	10	RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R25	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-T0-1471-F
A4R26	0757-0434	9		RESISTOR 3.65K 1% .125W F TC=0±100	24546	C4-1/8-T0-3651-F
A4R27	0757-0317	7	1	RESISTOR 1.33K 1% .125W F TC=0±100	24546	C4-1/8-T0-1331-F
A4R30	0698-3430	5	8	RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R31	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R32	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R33	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R34	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R35	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R36	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R37	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0±100	03888	PME55-1/8-T0-21R5-F
A4R40	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R41	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R42	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R43	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R44	0757-0433	8	4	RESISTOR 3.32K 1% .125W F TC=0±100	24546	C4-1/8-T0-3321-F
A4R45	0757-0433	8		RESISTOR 3.32K 1% .125W F TC=0±100	24546	C4-1/8-T0-3321-F
A4R46	0757-0433	8		RESISTOR 3.32K 1% .125W F TC=0±100	24546	C4-1/8-T0-3321-F
A4R47	0757-0433	8		RESISTOR 3.32K 1% .125W F TC=0±100	24546	C4-1/8-T0-3321-F
A4R48	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R49	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R50	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R51	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R52	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0±100	24546	C4-1/8-T0-3011-F
A4R59	0757-0442	9	6	RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A4R60	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0±100	24546	C4-1/8-T0-1211-F
A4R61	0757-0462	3	3	RESISTOR 75K 1% .125W F TC=0±100	24546	C4-1/8-T0-7502-F
A4R62	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A4R63	0757-0462	3		RESISTOR 75K 1% .125W F TC=0±100	24546	C4-1/8-T0-7502-F
A4R64	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A4R65	0757-0282	5	1	RESISTOR 221 1% .125W F TC=0±100	24546	C4-1/8-T0-221R-F
A4R71	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A4R73	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-T0-1471-F
A4R77	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A4R78	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A4R79	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A4R82	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A4R83	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A4R85	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-5111-F
A4R90	0757-0417	8	2	RESISTOR 562 1% .125W F TC=0±100	24546	C4-1/8-T0-562R-F
A4R91	0757-0411	2	3	RESISTOR 332 1% .125W F TC=0±100	24546	C4-1/8-T0-332R-F
A4R92	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-T0-1471-F
A4R93	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A4R94	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-T0-1471-F
A4R95	0757-0411	2		RESISTOR 332 1% .125W F TC=0±100	24546	C4-1/8-T0-332R-F
A4R96	0757-0411	2		RESISTOR 332 1% .125W F TC=0±100	24546	C4-1/8-T0-332R-F
A4R97	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-T0-1471-F
A4R98	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A4R99	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0±100	24546	C4-1/8-T0-1471-F
A4R100	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A4R104	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A4R107	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A4R108	0757-0473	6	2	RESISTOR 221K 1% .125W F TC=0±100	24546	C4-1/8-T0-2213-F
A4R109	0757-0473	6		RESISTOR 221K 1% .125W F TC=0±100	24546	C4-1/8-T0-2213-F
A4R110	0757-0417	8		RESISTOR 562 1% .125W F TC=0±100	24546	C4-1/8-T0-562R-F
A4R111	0757-0424	7	1	RESISTOR 1.1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1101-F
A4R112	0757-0465	6	1	RESISTOR 100K 1% .125W F TC=0±100	24546	C4-1/8-T0-1003-F
A4R113	0757-0470	3	1	RESISTOR 162K 1% .125W F TC=0±100	24546	C4-1/8-T0-1623-F
A4R114	0757-0407	6	1	RESISTOR 200 1% .125W F TC=0±100	24546	C4-1/8-T0-201-F
A4R120	0684-2221	1	34	RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R121	0757-0462	3		RESISTOR 75K 1% .125W F TC=0±100	24546	C4-1/8-T0-7502-F
A4R200	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R201	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R202	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R203	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R204	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R205	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R206	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R207	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R208	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R209	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R210	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R211	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R212	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R213	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R214	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R215	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R216	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R217	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R218	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R219	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R220	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R221	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R222	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R223	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R224	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R225	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R226	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R227	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R228	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R229	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R230	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R231	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R232	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
A4R233	0698-7096	7	2	RESISTOR 10 10% .125W CC TC=-120/+400	01121	BB1001
A4R234	0698-7096	7		RESISTOR 10 10% .125W CC TC=-120/+400	01121	BB1001
A4S1	3101-2063	8	1	SWITCH ROCKER	28480	3101-2063
A4TP1	0360-0535	0	6	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4U1	1820-1226	5	1	SHF-RGTR TTL ASYNCHRO SERIAL-IN	28480	1820-1226
A4U2	1826-0138	8	3	COMPARATOR GP QUAD 14-DIP P PKG	01295	LM339N
A4U3	1820-2024	3	5	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A4U4	1820-1216	3	1	IC DCDR TTL LS 3-TO 8-LINE 3-INP	01295	SN74LS138N
A4U5	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A4U6	1820-1430	3	3	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A4U7	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A4U8	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A4U9	1820-1669	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A4U10	1820-1427	8	2	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS156N
A4U11	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A4U12	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP P PKG	01295	LM339N
A4U13	1KB1-5010	1	2	LAMP DRIVER	28480	1KB1-5010
A4U14	1820-0806	6	1	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A4U15	1KB1-5010	1		LAMP DRIVER	28480	1KB1-5010
A4U16	1818-0735	4	1	IC 2K RAM 400 NS	34649	P8155
A4U17	1820-2370	2	1	IC	28480	1820-2370
A4U18	1820-2367	7	1	IC	28480	1820-2367
A4U19	1820-2181	6	1	IC MICPROC ACCESS NMOS 8 BIT	34649	P8276
A4U20	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A4U21	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A4U22	1820-2368	8	1	IC MISC TTL S	18324	82S100N PROGRAMMED
A4U23	1818-0614	7	1	IC NMOS ROM CHAR GEN	04713	MCM6670P MASKED
A4U24	1820-1975	1	1	IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
A4U25	1820-1427	8		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS156N
A4U26	1818-1654	0	1	IC NMOS (32K) ROM	28480	1818-1654
A4U27	1818-1655	9	1	IC NMOS (32K) ROM	28480	1818-1655
A4U28	1818-1337	4	1	IC NMOS (32K) ROM	28480	1818-1337
A4U29	1818-1690	2	1	IC NMOS (32K) ROM	28480	1818-1690
A4U30	1818-1073	6	1	IC NMOS 32768 (32K) ROM 450 NS 3 S	18324	N263_N MASKED
A4U31	1820-2143	7	1	IC MICPROC ACCESS NMOS	34649	P8257
A4U32	1818-1153	2	2	IC NMOS 4096 (4K) RAM STAT 450 NS 3 S	34649	P2142L
A4U33	1818-1153	2		IC NMOS 4096 (4K) RAM STAT 450 NS 3 S	34649	P2142L
A4U34	1P15-1346	6	4	IC CMOS 4096 (4K) RAM STAT 450 NS	0003J	UPD444/6514
A4U35	1818-1346	5		IC CMOS 4096 (4K) RAM STAT 450 NS	0003J	UPD444/6514
A4U36	1818-1346	5		IC CMOS 4096 (4K) RAM STAT 450 NS	0003J	UPD444/6514
A4U37	1818-1346	5		IC CMOS 4096 (4K) RAM STAT 450 NS	0003J	UPD444/6514
A4U38	1820-1918	2	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A4U39	1820-2074	3	1	IC MICPROC NMOS 8 BIT	34649	P8085
A4U40	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A4U41	1KB4-5011	8	1	DAC REFRESHER	28480	1KB4-5011
A4U42	1818-0708	1	2	IC CMOS 1024 (1K) RAM STAT 650 NS 3 S	0003J	UPD5101LC

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U43	1818-0708	1		IC CMOS 1024 (1K) RAM STAT 650-NS 3-S	0003J	UPD5101LC
A4U44	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP P PKG	01295	LM339N
A4U45	1820-0881	7	1	IC SWITCH ANLG QUAD 14 DIP P PKG	01928	CD4016AE
A4U46	1820-2102	8		IC LCH TTL LS D-TYPE OCT	01295	SN74LS373N
A4U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A4U48	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A4U49	1820-1433	6	3	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A4U50	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A4U51	1820-0078	2	1	IC GATE CMOS DUAL	01928	CD4007AE
A4U52	1820-1112	8		IC FF TTL LS D-TYPE POS EDGE-TRIG	01295	SN74LS74AN
A4U53	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-IN	01295	SN74LS00N
A4U54	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A4U55	1820-1433	6		IC SHF-RGTR TTL LS R-S SERIAL IN PRL-OUT	01295	SN74LS164N
A4U56	1820-2344	0	1	IC SHF-RGTR CMOS NEG EDGE-TRIG SERIAL-IN	04713	MC14557BCP
A4U57	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
A4U58	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A4U59	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A4U60	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A4U61	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A4U62	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A4U63	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A4U64	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A4U65	1826-0092	3	1	IC OP AMP GP DUAL TO-99 PKG	28480	1826-0092
A4U66	1NA1-8001	1	1	DAC HYBRID	28480	1NA1-8001
A4U67	1810-0212	6	1	NETWORK-RES 16-DIP22 2K OHM X 8	01121	3168223
A4U68	1810-0376	3	1	NETWORK-RES 9-SIP2 2K OHM X 8	28480	1810-0376
A4U69	1810-0281	6	1	NETWORK-RES 10-SIP100 0K OHM X 8	01121	210A104
A4U70	1810-0206	7	1	NETWORK-RES 8-SIP4 7K OHM X 7	01121	208A472
A4U71	1810-0155	6	2	NETWORK-RES 6-SIP4 0K OHM X 5	91637	CTP06C07-402K
A4U72	1810-0155	6		NETWORK-RES 5-SIP4 0K OHM X 5	91637	CSP06C07-402K
A4U73	1810-0269	3	1	NETWORK-RES 9-SIP10 0K OHM X 8	28480	1810-0269
A4U74	1810-0176	1	1	NETWORK-RES 5-SIP4 7K OHM X 4	28480	1810-0176
A4VR1	1902-3105	7	1	DIODE-ZNR 5.62V 2% DO-35 PD=.4W	28480	1902-3105
A4VR2	1902-3066	9	1	DIODE-ZNR 4.02V 2% DO-35 PD=.4W	28480	1902-3066
A4XU1	1200-0639	8	13	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU2	1200-0638	7	10	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU3	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU4	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU5	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU6	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU7	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU8	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU9	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU10	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU11	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU12	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU13	1200-0641	1	7	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0641
A4XU15	1200-0641	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0641
A4XU16	1200-0654	7	7	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A4XU17	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A4XU18	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A4XU19	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A4XU20	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU21	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU22	1200-0667	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0667
A4XU23	1200-0639	7	5	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0639
A4XU24	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU25	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU26	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A4XU27	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A4XU28	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A4XU29	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A4XU30	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A4XU31	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A4XU32	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU33	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU34	1200-0639	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0639
A4XU35	1200-0639	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0639
A4XU36	1200-0639	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0639
A4XU37	1200-0639	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0639
A4XU38	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU39	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A4XU40	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU41	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654

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Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4XU42	1200-0612	7	2	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A4XU43	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A4XU44	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU45	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU46	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU47	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU48	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU49	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU50	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU51	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU52	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU53	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU54	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU55	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU56	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A4XU57	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU58	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU59	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU60	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A4XU61	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU62	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU63	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4XU64	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A4Y1	0410-0423	2	1	CRYSTAL-QUARTZ 10.000 MHZ	28480	0410-0423

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Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	01980-66506	1	1	SCOPE BOARD ASSEMBLY	28480	01980-66506
A5C1	0160-3443	1	65	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C2	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C3	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C4	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C5	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C6	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C7	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C8	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C9	0160-3848	0	1	CAPACITOR-FXD 3.3PF ±.5PF 100VDC CER	28480	0160-3848
A5C10	0160-0694	8	2	CAPACITOR-FXD 1.5PF ±.1PF 100VDC CER	28480	0160-0694
A5C11	0160-0694	8		CAPACITOR-FXD 1.5PF ±.1PF 100VDC CER	28480	0160-0694
A5C12	0160-3802	6	2	CAPACITOR-FXD 150PF ±10% 100VDC CER	28480	0160-3802
A5C13	0160-3802	6		CAPACITOR-FXD 150PF ±10% 100VDC CER	28480	0160-3802
A5C14	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C15	0160-3569	2	1	CAPACITOR-FXD 27PF ±5% 100VDC CER 0±30	28480	0160-3569
A5C16	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C17	0160-2055	9	27	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C18	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C19	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C20	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C21	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C23	0121-0060	0	2	CAPACITOR-V TRMR-CER 2-8PF 350V PC-MTG	52763	304322 2/8PF NPO
A5C24	0160-2205	1	1	CAPACITOR-FXD 120PF ±5% 300VDC MICA	28480	0160-2205
A5C25	0180-0491	3	2	CAPACITOR-FXD 100UF ±10% 20VDC TA	56289	1090107X9030T2
A5C26	0160-3324	7	2	CAPACITOR-FXD 1UF ±5% 100VDC MET-POLYC	28480	0160-3324
A5C27	0180-0491	3		CAPACITOR-FXD 100UF±10% 20VDC TA	56289	1090107X9030T2
A5C28	0160-3324	7		CAPACITOR-FXD 1UF ±5% 100VDC MET-POLYC	28480	0160-3324
A5C29	0160-2202	8	2	CAPACITOR-FXD 75PF ±5% 300VDC MICA	28480	0160-2202
A5C31	0140-0204	4	1	CAPACITOR-FXD 47PF ±5% 500VDC MICA	72136	DM15E470J0500WV1CR
A5C32	0160-0115	7	1	CAPACITOR-FXD 27PF ±10% 500VDC CER	28480	0160-0115
A5C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C35	0160-2306	5	2	CAPACITOR-FXD 36PF ±5% 300VDC MICA	28480	0160-2306
A5C36	0160-2264	2	1	CAPACITOR-FXD 20PF ±5% 500VDC CER 0±30	28480	0160-2264
A5C37	0140-0190	7	1	CAPACITOR-FXD 39PF ±5% 300VDC MICA	72136	DM15E390J0300WV1CR
A5C39	0160-2202	8		CAPACITOR-FXD 75PF ±5% 300VDC MICA	28480	0160-2202
A5C40	0160-3652	4	2	CAPACITOR-FXD 4.7PF ±.5PF 200VDC CER	28480	0160-3652
A5C41	0160-2306	5		CAPACITOR-FXD 36PF ±5% 300VDC MICA	28480	0160-2306
A5C43	0160-3638	8	1	CAPACITOR-FXD 0.22UF ±20% 200VDC CER	28480	0160-3638
A5C44	0180-0106	9	3	CAPACITOR-FXD 60UF±20% 6VDC TA	56289	1500606X0006B2
A5C45	0160-3508	9	3	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C46	0180-0106	9		CAPACITOR-FXD 60UF±20% 6VDC TA	56289	1500606X0006B2
A5C47	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C48	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C49	0160-3567	0	1	CAPACITOR-FXD 10PF ±5% 100VDC CER 0±30	28480	0160-3567
A5C51	0180-1731	8	1	CAPACITOR-FXD 4.7UF±10% 50VDC TA	56289	1500475X9050B2
A5C52	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C53	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C54	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C55	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C56	0180-0155	8	2	CAPACITOR-FXD 2.2UF±20% 20VDC TA	56289	150D225X0020A2
A5C57	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C58	0180-1746	5	2	CAPACITOR-FXD 15UF±10% 20VDC TA	56289	150D156X9020B2
A5C59	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C60	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C61	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C62	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C63	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C64	0180-0155	8		CAPACITOR-FXD 2.2UF±20% 20VDC TA	56289	150D225X0020A2
A5C65	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C66	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C67	0160-2255	3	4	CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0160-2255
A5C68	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C69	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C70	0180-1714	7	1	CAPACITOR-FXD 330UF±10% 6VDC TA	56289	1500337X9006S2
A5C71	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C72	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C73	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C74	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C75	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

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Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5C76	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C77	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C78	0160-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0160-2255
A5C79	0160-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0160-2255
A5C81	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C82	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C83	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C84	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C85	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C86	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C87	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C88	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C89	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C90	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C91	0180-0374	3	1	CAPACITOR-FXD 10UF±10% 20VDC TA	56289	150D106X9020B2
A5C92	0180-1701	2	3	CAPACITOR-FXD 6.8UF±20% 6VDC TA	56289	150D685X0006A2
A5C93	0180-2255	3		CAPACITOR-FXD 2.2UF±20% 20VDC TA	28480	0180-2255
A5C94	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C95	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C96	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C97	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C98	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C99	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C100	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C101	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C102	0180-0106	9		CAPACITOR-FXD 60UF±20% 6VDC TA	56289	150D606X0006B2
A5C103	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C104	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C105	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C106	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C107	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C108	0180-0229	7	1	CAPACITOR-FXD 33UF±10% 10VDC TA	56289	150D336X9010B2
A5C109	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C110	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C111	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C112	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C113	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C114	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C115	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C116	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C117	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C118	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C119	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C120	0180-1746	5		CAPACITOR-FXD 15UF±10% 20VDC TA	56289	150D156X9020B2
A5C121	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C122	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C123	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C124	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C125	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C126	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C127	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C128	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C129	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C130	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C131	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C132	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C133	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C134	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C138	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C139	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C140	0160-0300	4	2	CAPACITOR-FXD 4.7UF±20% 10VDC TA	56289	150D475X0010A2
A5C141	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C142	0160-0300	4		CAPACITOR-FXD 4.7UF±20% 10VDC TA	56289	150D475X0010A2
A5C144	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C145	0180-1701	2		CAPACITOR-FXD 6.8UF±20% 6VDC TA	56289	150D685X0006A2
A5C146	0180-1701	2		CAPACITOR-FXD 6.8UF±20% 6VDC TA	56289	150D685X0006A2
A5C147	0140-0199	6	1	CAPACITOR-FXD 240PF ±5% 300VDC MICA	72136	DM15F241J0300WV1CR
A5C148	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C149	0180-0098	8	1	CAPACITOR-FXD 100UF±20% 20VDC TA	56289	150D107X0020S2
A5C150	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C151	0160-3652	4		CAPACITOR-FXD 4.7PF ± .5PF 200VDC CER	28480	0160-3652
A5C152	0121-0467	1	1	CAPACITOR-V TRMR-CER 2.5-9PF 350VDC	52736	304322 2.5-9PF NPO

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5CR1	1901-0943	3	4	DIODE-SM SIG SCHOTTKY	28480	1901-0943
A5CR2	1901-0047	8	7	DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR3	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR4	1901-0943	3		DIODE-SM SIG SCHOTTKY	28480	1901-0943
A5CR5	0122-0077	1	2	DIODE-VVC C1/C10-MIN=1.9 BVR=25V	04713	MV2201
A5CR6	0122-0077	1		DIODE-VVC C1/C10-MIN=1.9 BVR=25V	04713	MV2201
A5CR7	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR8	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR9	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR10	1901-0635	9	6	DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR11	1901-0635	9		DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR12	1901-0635	9		DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR13	1901-0635	9		DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR14	1901-0635	9		DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR15	1901-0635	9		DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR16	1901-0635	9		DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR17	1901-0635	9		DIODE-SM SIG SCHOTTKY	28480	1901-0635
A5CR18	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR19	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A5CR20	1901-0943	3		DIODE-SM SIG SCHOTTKY	28480	1901-0943
A5CR21	1901-0943	3		DIODE-SM SIG SCHOTTKY	28480	1901-0943
A5E1	9170-0029	3	10	CORE-SHIELDING BEAD	28480	9170-0029
A5E2	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E3	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E4	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E5	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E6	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E7	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E8	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E9	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E10	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A5E11	9170-0769	6	1	CORE-SHIELDING BEAD	28480	9170-0769
A5E12	1251-6084	8	12	CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6084
A5H1	2200-0113	4	12	SCREW-MACH 4-40 .625 IN LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A5J1	1251-5971	8	5	CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A5J2	1251-6571	6	1	CONNECTOR	28480	1251-6571
A5J3	1251-6607	9	2	CONNECTOR	28480	1251-6607
A5J4	1251-4836	2	2	CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251-4836
A5J5	1251-5971	8		CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A5J6	1251-4837	3	1	CONNECTOR 4-PIN M METRIC POST TYPE	28480	1251-4837
A5J7	1251-5971	8		CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A5J8	1251-5971	8		CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A5J9	1251-6607	9		CONNECTOR	28480	1251-6607
A5J10	1251-5971	8		CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A5J11	1251-4836	2		CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251-4836
A5J12	01980-67601	0	1	CONNECTOR ASSEMBLY-H F SCOPE	28480	01980-67601
A5L1	9100-2250	9	1	INDUCTOR RF-CH-MLD 180NH 10% .105DX.26LG	28480	9100-2250
A5L2	9140-0096	1	7	INDUCTOR RF-CH-MLD 1UH 10% .166DX.385LG	28480	9140-0096
A5L3	9140-0096	1		INDUCTOR RF-CH-MLD 1UH 10% .166DX.385LG	28480	9140-0096
A5L4	9140-0096	1		INDUCTOR RF-CH-MLD 1UH 10% .166DX.385LG	28480	9140-0096
A5L5	9140-0114	4	3	INDUCTOR RF-CH-MLD 10UH 10% .166DX.385LG	28480	9140-0114
A5L7	9140-0096	1		INDUCTOR RF-CH-MLD 1UH 10% .166DX.385LG	28480	9140-0096
A5L8	9140-0114	4		INDUCTOR RF-CH-MLD 10UH 10% .166DX.385LG	28480	9140-0114
A5L9	9140-0114	4		INDUCTOR RF-CH-MLD 10UH 10% .166DX.385LG	28480	9140-0114
A5L11	9140-0096	1		INDUCTOR RF-CH-MLD 1UH 10% .166DX.385LG	28480	9140-0096
A5L12	9140-0096	1		INDUCTOR RF-CH-MLD 1UH 10% .166DX.385LG	28480	9140-0096
A5L13	9140-0096	1		INDUCTOR RF-CH-MLD 1UH 10% .166DX.385LG	28480	9140-0096
A5MP1	5041-1550	0	3	HOUSING-SUBSTRATE	28480	5041-1550
A5MP2	01950-04101	7	3	COVER-HYBRID	28480	01950-04101
A5MP3	5041-3062	3	6	SUPPORT POST-CABLE	28480	5041-3062
A5P1	1251-1887	7	1	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1887
A5Q1	1854-0628	0	8	TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q2	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q3	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q4	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q5	1853-0075	9	1	TRANSISTOR-DUAL PNP PD=400MW	28480	1853-0075
A5Q6	1853-0354	7	8	TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A5Q7	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A5Q8	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A5Q9	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A5Q10	1854-0092	2	1	TRANSISTOR NPN SI PD=200MW FT=600MHZ	28480	1854-0092

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5Q11	1854-0215	1	3	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A5Q12	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q13	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q14	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q15	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-H17
A5Q16	1853-0034	0	2	TRANSISTOR PNP SI TO-18 PD=360MW	28480	1853-0034
A5Q17	1853-0034	0		TRANSISTOR PNP SI TO-18 PD=360MW	28480	1853-0034
A5Q18	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A5Q19	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A5Q20	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=360MW	28480	1853-0354
A5Q21	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=360MW	28480	1853-0354
A5Q22	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=360MW	28480	1853-0354
A5Q23	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=360MW	28480	1853-0354
A5R1	0684-1031	9	9	RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A5R2	0684-1021	7	6	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A5R3	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A5R4	0757-0449	6	5	RESISTOR 20K 1% .125W F TC=0±100	24546	C4-1/8-T0-2002-F
A5R5	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A5R6	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A5R7	0757-0449	6		RESISTOR 20K 1% .125W F TC=0±100	24546	C4-1/8-T0-2002-F
A5R8	0684-1041	1	6	RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A5R9	0684-1041	1		RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A5R10	0757-0460	1	2	RESISTOR 61.9K 1% .125W F TC=0±100	24546	C4-1/8-T0-6192-F
A5R11	0757-0460	1		RESISTOR 61.9K 1% .125W F TC=0±100	24546	C4-1/8-T0-6192-F
A5R12	0757-0282	5	4	RESISTOR 221 1% .125W F TC=0±100	24546	C4-1/8-T0-221R-F
A5R13	0757-0448	5	2	RESISTOR 18.2K 1% .125W F TC=0±100	24546	C4-1/8-T0-1822-F
A5R14	0757-0448	5		RESISTOR 18.2K 1% .125W F TC=0±100	24546	C4-1/8-T0-1822-F
A5R15	0757-0280	3	8	RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R16	0757-0282	5		RESISTOR 221 1% .125W F TC=0±100	24546	C4-1/8-T0-221R-F
A5R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R18	0698-7212	9	2	RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-T0-100R-G
A5R20	0757-0452	1	12	RESISTOR 27.4K 1% .125W F TC=0±100	24546	C4-1/8-T0-2742-F
A5R21	0698-7226	5	1	RESISTOR 383 1% .05W F TC=0±100	24546	C3-1/8-T0-383R-G
A5R22	0698-7212	9		RESISTOR 100 1% .05W F TC=0±100	24546	C3-1/8-T0-100R-G
A5R23	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0±100	24546	C4-1/8-T0-750R-F
A5R24	0757-0413	4	5	RESISTOR 392 1% .125W F TC=0±100	24546	C4-1/8-T0-392R-F
A5R25	0757-0452	1		RESISTOR 27.4K 1% .125W F TC=0±100	24546	C4-1/8-T0-2742-F
A5R27	0757-0282	5		RESISTOR 221 1% .125W F TC=0±100	24546	C4-1/8-T0-221R-F
A5R28	0757-0430	5	1	RESISTOR 3.21K 1% .125W F TC=0±100	24546	C4-1/8-T0-3211-F
A5R29	0698-4130	4	1	RESISTOR 39.6% .125W CC TC=-270/+640	01121	BB3905
A5R30	0757-0402	1	2	RESISTOR 110 1% .125W F TC=0±100	24546	C4-1/8-T0-111-F
A5R31	0757-0402	1		RESISTOR 110 1% .125W F TC=0±100	24546	C4-1/8-T0-111-F
A5R32	0757-0442	9	5	RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A5R33	2100-2216	0	3	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	73138	82PR5K
A5R34	0757-0442	9		RESISTOR 10K 1% .125W F TC=0±100	24546	C4-1/8-T0-1002-F
A5R35	2100-1964	7	1	RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	73138	82PR100
A5R36	0757-0401	0	17	RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R37	2100-1966	9	2	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	73138	82PR1K
A5R38	0757-0419	0	2	RESISTOR 681 1% .125W F TC=0±100	24546	C4-1/8-T0-681R-F
A5R39	0757-0419	0		RESISTOR 681 1% .125W F TC=0±100	24546	C4-1/8-T0-681R-F
A5R40	0757-0420	3	5	RESISTOR 750 1% .125W F TC=0±100	24546	C4-1/8-T0-751-F
A5R41	0757-0420	3		RESISTOR 750 1% .125W F TC=0±100	24546	C4-1/8-T0-751-F
A5R42	0698-7222	1	1	RESISTOR 261 1% .05W F TC=0±100	24546	C3-1/8-T0-261R-G
A5R43	0698-3446	2	1	RESISTOR 348 1% .125W F TC=0±100	24546	C4-1/8-T0-348R-F
A5R44	0698-7204	9	2	RESISTOR 46.4 1% .05W F TC=0±100	24546	C3-1/8-T00-46R4-G
A5R45	0698-7204	9		RESISTOR 46.4 1% .05W F TC=0±100	24546	C3-1/8-T00-46R4-G
A5R46	0698-7203	8	2	RESISTOR 42.2 1% .05W F TC=0±100	24546	C3-1/8-T00-42R2-G
A5R47	0684-1031	9		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A5R48	0698-7203	8		RESISTOR 42.2 1% .05W F TC=0±100	24546	C3-1/8-T00-42R2-G
A5R49	0698-7255	0	1	RESISTOR 6.19K 1% .05W F TC=0±100	24546	C3-1/8-T0-6191-G
A5R50	0698-7284	5	1	RESISTOR 100K 1% .05W F TC=0±100	24546	C3-1/8-T0-1003-G
A5R51	0698-7262	7	2	RESISTOR 4.64K 1% .05W F TC=0±100	24546	C3-1/8-T0-4641-G
A5R52	0698-7279	8	1	RESISTOR 61.9K 1% .05W F TC=0±100	24546	C3-1/8-T0-6192-G
A5R53	0684-1011	5	2	RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011
A5R54	0757-0422	5	1	RESISTOR 909 1% .125W F TC=0±100	24546	C4-1/8-T0-909R-F
A5R55	0757-0420	3		RESISTOR 750 1% .125W F TC=0±100	24546	C4-1/8-T0-751-F
A5R56	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R57	0757-0437	2	5	RESISTOR 4.75K 1% .125W F TC=0±100	24546	C4-1/8-T0-4751-F
A5R58	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A5R59	0698-6435	6	1	RESISTOR 2.61K 5% .05W F TC=0±100	28480	0698-6435
A5R60	0698-7216	3	1	RESISTOR 147 1% .05W F TC=0±100	24546	C3-1/8-T0-147R-G
A5R61	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0±100	24546	C4-1/8-T0-4751-F
A5R62	0757-0420	3		RESISTOR 750 1% .125W F TC=0±100	24546	C4-1/8-T0-751-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R63	0757-0420	3		RESISTOR 750 1% .125W F TC=0±100	24546	C4-1/8-T0-751-F
A5R64	0757-0438	3	7	RESISTOR 6.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-6111-F
A5R65	0757-0438	3		RESISTOR 6.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-6111-F
A5R66	0757-0438	3		RESISTOR 6.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-6111-F
A5R67	0757-0438	3		RESISTOR 6.11K 1% .125W F TC=0±100	24546	C4-1/8-T0-6111-F
A5R68	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0±100	24546	C4-1/8-T0-10R0-F
A5R69	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0±100	24546	C4-1/8-T0-51R1-F
A5R70	0698-3437	2	2	RESISTOR 133 1% .125W F TC=0±100	24546	C4-1/8-T0-133R-F
A5R71	0757-0772	4	2	RESISTOR 619 1% .125W F TC=0±100	24546	C4-1/8-T0-619R-F
A5R72	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R73	0699-0774	6	8	RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R74	0699-0773	5	2	RESISTOR 4.75K 1% .125W F TC=0±100	28480	0699-07[illegible]
A5R75	0757-0247	2	2	RESISTOR 750 1% .5W F TC=0±100	28480	0757-0247
A5R76	0698-8184	6	4	RESISTOR 7.5K 1% .125W F TC=0±100	28480	0698-8184
A5R77	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0±100	24546	C4-1/8-T0-4751-F
A5R78	0698-8184	6		RESISTOR 7.5K 1% .125W F TC=0±100	28480	0698-8184
A5R79	0698-7634	8	2	RESISTOR 42.2K 1% .125W F TC=0±100	28480	0698-7634
A5R80	0699-0774	6		RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R81	0699-0774	6		RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R82	0698-3460	9	3	RESISTOR 42.2K 1% .125W F TC=0±100	24546	C4-1/8-T0-4[illegible]
A5R83	0699-0774	6		RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R84	0698-3437	2		RESISTOR 133 1% .125W F TC=0±100	24546	C4-1/8-T0-133R-F
A5R85	0699-0772	4		RESISTOR 619 1% .125W F TC=0±100	28480	0699-0772
A5R86	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R87	0699-0774	6		RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R88	0699-0773	5		RESISTOR 4.75K 1% .125W F TC=0±100	28480	0699-0773
A5R89	0757-0247	2		RESISTOR 750 1% .5W F TC=0±100	28480	0757-0247
A5R90	0698-8184	6		RESISTOR 7.5K 1% .125W F TC=0±100	28480	0698-8184
A5R91	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0±100	24546	C4-1/8-T0-4751-F
A5R92	0698-8184	6		RESISTOR 7.5K 1% .125W F TC=0±100	28480	0698-8184
A5R93	0698-7634	8		RESISTOR 42.2K 1% .125W F TC=0±100	28480	0698-7634
A5R94	0699-0774	6		RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R95	0699-0774	6		RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R96	0698-3460	9		RESISTOR 42.2K 1% .125W F TC=0±100	24546	C4-1/8-T0-4222-F
A5R97	0699-0774	6		RESISTOR 6.65K 1% .125W F TC=0±100	28480	0699-0774
A5R98	0757-0416	7	6	RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A5R99	0698-3460	9		RESISTOR 42.2K 1% .125W F TC=0±100	24546	C4-1/8-T0-4222-F
A5R100	2100-2216	0		RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	73138	82PR5K
A5R101	0757-0434	9	5	RESISTOR 3.65K 1% .125W F TC=0±100	24546	C4-1/8-T0-3651-F
A5R102	0757-1102	0	3	RESISTOR 180 1% .125W F TC=0±100	24546	C4-1/8-T0-181-F
A5R103	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A5R104	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R105	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R106	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R107	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R108	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R109	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A5R110	0757-0418	9		RESISTOR 619 1% .125W F TC=0±100	24546	C4-1/8-T0-619R-F
A5R111	2100-2216	0		RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	73138	82PR5K
A5R112	0757-0434	9		RESISTOR 3.65K 1% .125W F TC=0±100	24546	C4-1/8-T0-3651-F
A5R113	0757-0440	7	3	RESISTOR 7.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-7501-F
A5R114	0757-0418	9		RESISTOR 619 1% .125W F TC=0±100	24546	C4-1/8-T0-619R-F
A5R115	0757-0427	0	2	RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A5R116	0757-0449	6		RESISTOR 20K 1% .125W F TC=0±100	24546	C4-1/8-T0-2002-F
A5R117	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-7501-F
A5R118	0684-1031	9		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A5R119	0757-1102	0		RESISTOR 180 1% .125W F TC=0±100	24546	C4-1/8-T0-181-F
A5R120	0757-0283	6		RESISTOR 2K 1% .125W F TC=0±100	24546	C4-1/8-T0-2001-F
A5R121	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R122	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R123	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R124	0757-0394	0	5	RESISTOR 51.1 1% .125W F TC=0±100	24546	C4-1/8-T0-51R1-F
A5R125	0757-0274	5	2	RESISTOR 1.21K 1% .125W F TC=0±100	24546	C4-1/8-T0-1211-F
A5R126	0757-0449	6		RESISTOR 20K 1% .125W F TC=0±100	24546	C4-1/8-T0-2002-F
A5R128	0684-1031	9		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A5R129	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A5R130	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-7501-F
A5R131	0757-0401	0		RESISTOR 100 1% .125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R132	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0±100	24546	C4-1/8-T0-1501-F
A5R133	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R134	2100-2031	7	1	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	73138	82PR50K
A5R135	0757-0416	7		RESISTOR 511 1% .125W F TC=0±100	24546	C4-1/8-T0-511R-F
A5R136	0757-0444	1	1	RESISTOR 12.1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1212-F
A5R137	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0±100	24546	C4-1/8-T0-51R1-F
A5R138	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0±100	24546	C4-1/8-T0-1211-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R139	0757-0401	0		RESISTOR 100 1% 125W F TC=0+100	24546	C4-1/8-T0-101-F
A5R140	0757-0394	0		RESISTOR 51.1 1% 125W F TC=0+100	24546	C4-1/8-T0-51R1-F
A5R141	0757-0434	9		RESISTOR 3.65K 1% 125W F TC=0+100	24546	C4-1/8-T0-3651-F
A5R142	0757-0436	3		RESISTOR 5.11K 1% 125W F TC=0+100	24546	C4-1/8-T0-5111-F
A5R143	0757-0434	9		RESISTOR 3.65K 1% 125W F TC=0+100	24546	C4-1/8-T0-3651-F
A5R144	0757-0436	3		RESISTOR 5.11K 1% 125W F TC=0+100	24546	C4-1/8-T0-5111-F
A5R145	0757-0449	6		RESISTOR 20K 1% 125W F TC=0+100	24546	C4-1/8-T0-2002-F
A5R146	0757-0434	9		RESISTOR 3.65K 1% 125W F TC=0+100	24546	C4-1/8-T0-3651-F
A5R147	0757-0436	3		RESISTOR 5.11K 1% 125W F TC=0+100	24546	C4-1/8-T0-5111-F
A5R148	0698-4157	5	3	RESISTOR 10K 1% 125W F TC=0+50	28480	0698-4157
A5R149	0698-8607	8	1	RESISTOR [illegible] 1% 125W F TC=0+25	28480	0698-8607
A5R150	0698-6355	9	1	RESISTOR 400 1% 125W F TC=0+25	28480	0698-6355
A5R151	0698-6364	0	1	RESISTOR 50 1% 125W F TC=0+25	28480	0698-6364
A5R152	0698-6354	8	1	RESISTOR 40 1% 125W F TC=0+25	28480	0698-6354
A5R153	0698-5462	5	1	RESISTOR 10 1% 125W F TC=0+50	28480	0698-5462
A5R154	0684-1031	9		RESISTOR 10K 10% 25W FC TC=+400/+700	01121	CB1031
A5R155	0757-0442	9		RESISTOR 10K 1% 125W F TC=0+100	24546	C4-1/8-T0-1002-F
A5R156	0757-0436	1	1	RESISTOR 5.32K 1% 125W F TC=0+100	24546	C4-1/8-T0-4321-F
A5R157	0698-4157	5		RESISTOR 10K 1% 125W F TC=0+50	28480	0698-4157
A5R158	0698-4157	5		RESISTOR 10K 1% 125W F TC=0+50	28480	0698-4157
A5R160	0757-0416	7		RESISTOR 511 1% 125W F TC=0+100	24546	C4-1/8-T0-511R-F
A5R161	0757-0401	0		RESISTOR 100 1% 125W F TC=0+100	24546	C4-1/8-T0-101-F
A5R162	0757-0401	0		RESISTOR 100 1% 125W F TC=0+100	24546	C4-1/8-T0-101-F
A5R163	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R164	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R165	0698-3443	0	4	RESISTOR 287 1% 125W F TC=0+100	24546	C4-1/8-T0-287R-F
A5R166	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R167	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R168	0698-3443	0		RESISTOR 287 1% 125W F TC=0+100	24546	C4-1/8-T0-287R-F
A5R169	0757-0281	4	2	RESISTOR 2.74K 1% 125W F TC=0+100	24546	C4-1/8-T0-2741-F
A5R170	0757-0426	9	2	RESISTOR 1.3K 1% 125W F TC=0+100	24546	C4-1/8-T0-1301-F
A5R171	2100-3212	8	2	RESISTOR-TRMR 200 10% C TOP ADJ 1-TRN	28480	2100-3212
A5R173	0684-1031	9		RESISTOR 10K 10% 25W FC TC=+400/+700	01121	CB1031
A5R174	0684-1031	9		RESISTOR 10K 10% 25W FC TC=+400/+700	01121	CB1031
A5R175	0684-1031	9		RESISTOR 10K 10% 25W FC TC=+400/+700	01121	CB1031
A5R176	0757-0437	2		RESISTOR 4.75K 1% 125W F TC=0+100	24546	C4-1/8-T0-4751-F
A5R177	0757-0428	1	1	RESISTOR 1.62K 1% 125W F TC=0+100	24546	C4-1/8-T0-1621-F
A5R178	0757-0431	6	1	RESISTOR 2.43K 1% 125W F TC=0+100	24546	C4-1/8-T0-2431-F
A5R179	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R180	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R181	0698-3443	0		RESISTOR 287 1% 125W F TC=0+100	24546	C4-1/8-T0-287R-F
A5R182	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R183	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R184	0698-3443	0		RESISTOR 287 1% 125W F TC=0+100	24546	C4-1/8-T0-287R-F
A5R185	0757-0426	9		RESISTOR 1.3K 1% 125W F TC=0+100	24546	C4-1/8-T0-1301-F
A5R186	0757-0281	4		RESISTOR 2.74K 1% 125W F TC=0+100	24546	C4-1/8-T0-2741-F
A5R187	2100-3212	8		RESISTOR-TRMR 200 10% C TOP ADJ 1-TRN	28480	2100-3212
A5R188	0675-1011	6	9	RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R190	0698-7931	9	7	RESISTOR 1.5K 10% 125W CC TC=-350/+857	01121	BB1521
A5R191	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R192	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R193	0698-7931	9		RESISTOR 1.5K 10% 125W CC TC=-350/+857	01121	BB1521
A5R194	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R195	0698-7931	9		RESISTOR 1.5K 10% 125W CC TC=-350/+857	01121	BB1521
A5R196	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R197	0698-7931	9		RESISTOR 1.5K 10% 125W CC TC=-350/+857	01121	BB1521
A5R198	0698-7252	7		RESISTOR 4.64K 1% 05W F TC=0+100	24546	C3-1/8-T0-4641-G
A5R199	0698-7248	1	1	RESISTOR 3.16K 1% 05W F TC=0+100	24546	C3-1/8-T0-3161-G
A5R189	0698-7931	9		RESISTOR 1.5K 10% 125W CC TC=-350/+857	01121	BB1521
A5R200	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R201	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R202	0698-7931	9		RESISTOR 1.5K 10% 125W CC TC=-350/+857	01121	BB1521
A5R203	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R204	0698-7931	9		RESISTOR 1.5K 10% 125W CC TC=-350/+857	01121	BB1521
A5R205	0698-7235	6	2	RESISTOR 909 1% 05W F TC=0+100	24546	C3-1/8-T0-909R-G
A5R206	0698-7235	6		RESISTOR 909 1% 05W F TC=0+100	24546	C3-1/8-T0-909R-G
A5R207	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R208	0757-0462	1		RESISTOR 27.4K 1% 125W F TC=0+100	24546	C4-1/8-T0-2742-F
A5R210	0757-0416	7		RESISTOR 511 1% 125W F TC=0+100	24546	C4-1/8-T0-511R-F
A5R211	0684-1011	5		RESISTOR 100 10% 25W FC TC=+400/+500	01121	CB1011
A5R212	0757-0394	0		RESISTOR 51.1 1% 125W F TC=0+100	24546	C4-1/8-T0-51R1-F
A5R213	0757-0282	5		RESISTOR 221 1% 125W F TC=0+100	24546	C4-1/8-T0-221R-F
A5R214	0675-1011	6		RESISTOR 100 10% 125W CC TC=-270/+640	01121	BB1011
A5R215	0684-1021	7		RESISTOR 1K 10% 25W FC TC=+400/+600	01121	CB1021
A5R216	0684-1021	7		RESISTOR 1K 10% 25W FC TC=+400/+600	01121	CB1021

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R217	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R218	0699-0001	2	2	RESISTOR 2.7 10% 5W CC TC=0+412	01121	EB27G1
A5R220	0698-3132	4	1	RESISTOR 261 1% 125W F TC=0±100	24546	C4-1/8-T0-2610-F
A5R221	0757-0281	4		RESISTOR 2.74K 1% 125W F TC=0±100	24546	C4-1/8-T0-2741-F
A5R222	0757-0394	0		RESISTOR 51.1 1% 125W F TC=0±100	24546	C4-1/8-T0-51R1-F
A5R223	0757-0439	4	2	RESISTOR 6.81K 1% 125W F TC=0±100	24546	C4-1/8-T0-6811-F
A5R224	0757-0439	4		RESISTOR 6.81K 1% 125W F TC=0±100	24546	C4-1/8-T0-6811-F
A5R225	0757-0283	6		RESISTOR 2K 1% 125W F TC=0±100	24546	C4-1/8-T0-2001-F
A5R226	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R227	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R228	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A5R229	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A5R230	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A5R231	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A5R232	0698-3155	1	3	RESISTOR 4.64K 1% 125W F TC=0±100	24546	C4-1/8-T0-4641-F
A5R233	0698-3155	1		RESISTOR 4.64K 1% 125W F TC=0±100	24546	C4-1/8-T0-4641-F
A5R234	0698-3155	1		RESISTOR 4.64K 1% 125W F TC=0±100	24546	C4-1/8-T0-4641-F
A5R235	0683-0275	9	8	RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R236	0683-0275	9		RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R237	0683-0275	9		RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R238	0683-0275	9		RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R239	0683-0275	9		RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R240	0683-0275	9		RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R241	0683-0275	9		RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R242	0683-0275	9		RESISTOR 2.7 5% 25W FC TC=-400/+800	01121	CB27G5
A5R243	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R244	0757-0401	0		RESISTOR 100 1% 125W F TC=0±100	24546	C4-1/8-T0-101-F
A5R245	0757-0178	8	1	RESISTOR 100 1% .25W F TC=0±100	24546	C8-1/4-T0-101-F
A5R246	0684-5611	9	4	RESISTOR 560 10% 25W FC TC=-400/+600	01121	CB5611
A5R247	0684-5611	9		RESISTOR 560 10% 25W FC TC=-400/+600	01121	CB5611
A5R248	0684-5611	9		RESISTOR 560 10% 25W FC TC=-400/+600	01121	CB5611
A5R249	0757-0280	3		RESISTOR 1K 1% .125W F TC=0±100	24546	C4-1/8-T0-1001-F
A5R250	0684-5611	9		RESISTOR 560 10% 25W FC TC=-400/+600	01121	CB5611
A5R251	0684-1031	9		RESISTOR 10K 10% 25W FC TC=-400/+700	01121	CB1031
A5R252	0757-0480	5	1	RESISTOR 432K 1% 125W F TC=0±100	28480	0757-0480
A5R255	0699-0001	2		RESISTOR 2.7 10% 5W CC TC=0+412	01121	EB27G1
A5R256	2100-1985	9		RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	73138	82PR1K
A5RT1	0837-0113	1	1	THERMISTOR DISC 100K OHM TC=-5%/C-DEG	50157	4D101
A5TP1	0360-0535	0	2	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5U1	1NA3-8003	7	1	TRIG HYBRID	28480	1NA3-8003
A5U2	1820-1882	9	1	IC GATE ECL EXCL-OR QUAD	04713	MC10113L
A5U3	1820-1662	3	3	IC SHF-RGTR CMOS SERIAL-IN PRL-OUT 8-BIT	01928	CD4094BE
A5U4	1820-0809	8	1	IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A5U5	1820-1662	3		IC SHF-RGTR CMOS SERIAL-IN PRL-OUT 8-BIT	01928	CD4094BE
A5U6	1820-1662	3		IC SHF-RGTR CMOS SERIAL-IN PRL-OUT 8-BIT	01928	CD4094BE
A5U7	1NA2-8002	4	1	PREAMP HYBRID	28480	1NA2-8002
A5U8	1820-1400	7	2	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A5U9	1NA5-8005	3	1	HORIZ HYBRID	28480	1NA5-8005
A5U10	1820-0668	7	1	IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
A5U11	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A5U12	1820-1173	1	1	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A5U13	1826-0312	0	1	IC OP AMP GP QUAD 14-DIP-P PKG	04713	MC3403P
A5U14	1816-1389	2	1	IC TTL S 4096 (4K) PROM 70-NS 3-S	01295	TBP18S42N PROGRAMMED
A5U15	1820-2313	3	1	IC SHF-RGTR TTL LS SERIAL-IN SERIAL-OUT	01295	SN74LS673N
A5U16	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A5U17	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A5U18	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A5U19	1820-1246	9	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS09N
A5U20	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A5U21	1826-0628	0	1	IC OP AMP LOW-BIAS H-IMPD TO-99 PKG	27014	LF356BH
A5U22	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A5U23	1820-1441	0	1	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A5U24	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A5U25	1820-1315	3	1	IC MULTIPLXR 8-CHAN ANLG 16-DIP-P PKG	04713	MC14051BCP
A5U26	1820-1966	0	1	IC SWITCH ANLG QUAD 14-DIP-P PKG	01928	CD4016BE
A5VR1	1902-3086	3	2	DIODE-ZNR 4.75V 2% DO-35 PD=.4W	28480	1902-3086
A5VR2	1902-3086	3		DIODE-ZNR 4.75V 2% DO-35 PD=.4W	28480	1902-3086
A5VR3	1902-0959	3	1	DIODE-ZNR 11V 5% DO-35 PD=.4W TC=+.062%	28480	1902-0959
A5XU2	1200-0607	0	11	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU3	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU4	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU5	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU6	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5XU8	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU10	1200-0638	7	9	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU11	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU12	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU13	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU14	1200-0639	8	1	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A5XU15	1200-0641	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0641
A5XU16	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU17	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU18	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU19	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU20	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU22	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU23	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU24	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5XU25	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A5XU26	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A5A1	01980-66002	3	1	INDUCTOR ASSEMBLY	28480	01980-66002
A5A1C1	NSR	4		CAPACITOR-FXD NSR-NOT SEPARATELY REPLACEABLE ORDER 01980-66002	28480	NSR
A5A1L1	NSR	4		INDUCTOR NSR-NOT SEPARATELY REPLACEABLE ORDER 01980-66002	28480	NSR
A6	01980-66538	0	1	INTERCONNECT BOARD ASSEMBLY	28480	01980-66538
A6J1	1251-4837	3	1	CONNECTOR 4-PIN M METRIC POST TYPE	28480	1251-4837
A6X1	1251-1626	2	3	CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251-1626
A6X2	1251-1626	2		CONNECTOR-PC EDGE 12-CONT/ROW 2-ROWS	28480	1251-1626
A6X3	1251-1626	2		CONNECTOR-PC EDGE 12 CONT/ROW 2-ROWS	28480	1251-1626
A7	01980-66506	4	1	CAPACITOR BOARD ASSEMBLY	28480	01980-66506
A7C1	0180-2954	9	1	CAPACITOR-FXD 8800UF+75-10% 40VDC AL	55289	36D882G040BM2A
A7C2	0180-0482	4	2	CAPACITOR-FXD 250UF+50-10% 200VDC AL	00853	500251T200AA2B
A7C3	0180-0482	4		CAPACITOR-FXD 250UF+50-10% 200VDC AL	00853	500251T200AA2B
A7C4	0180-3069	9	2	CAPACITOR-FXD 012F+75-10% 20VDC AL	28480	0180-3069
A7C5	0180-3069	9		CAPACITOR-FXD 012F+75-10% 20VDC AL	28480	0180-3069
A7C6	0180-0574	0	1	CAPACITOR-FXD 4000UF+75-10% 30VDC AL	28480	0180-0574
A7C7	0180-2181	4	2	CAPACITOR-FXD 1300UF+75-10% 50VDC AL	00853	539-7471-02
A7C8	0180-2181	4		CAPACITOR-FXD 1300UF+75-10% 50VDC AL	00853	539-7471-02
A7H1	2680-0129	0	16	SCREW-MACH 10-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A7H2	2190-0011	8	15	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
A7P1	1251-5888	6	1	CONNECTOR 20-PIN F POST TYPE	28480	1251-5888
A7R1	0684-1041	1	7	RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A7R2	0687-1041	7	1	RESISTOR 100K 10% 5W CC TC=0+882	01121	EB1041
A7R3	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A7R4	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A7R5	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A7R6	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A7R7	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A7R8	0684-1041	1		RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A8	01980-66514	2	1	LINE SELECT BOARD	28480	01980-66514
A8J1	1251-5121	0	1	CONNECTOR 11-PIN M POST TYPE	28480	1251-5121
A8S1	3101-0433	2	2	SWITCH-SL DPDT STD 2A 250VAC PC	28480	3101-0433
A8S2	3101-0433	2		SWITCH-SL DPDT STD 2A 250VAC PC	28480	3101-0433

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	01980-60604	9	1	HEAT SINK ASSEMBLY	28480	01980-60604
A8B1W1	01980-61626	7	1	CABLE-FAN MOTOR DRIVE	28480	01980-61626
A8B1	3160-0266	3	1	FAN-TBAX 30-CFM 6-16VDC	28480	3160-0266
A8H1	2200-0139	4	12	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A8H2	0380-0063	5	4	SPACER-RND .688-IN-LG .114-IN-ID	28480	0380-0063
A8H3	0620-0127	6	4	SCREW-MACH 2-56 .188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A8H4	2190-0045	8	4	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0045
A8H5	3050-0106	6	4	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0106
A8H6	2190-0019	6	4	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
A8H7	2200-0121	4	4	SCREW-MACH 4-40 1.125-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A8H8	2190-0376	8	12	WASHER-FL MTLC NO. 4 .115-IN-ID	28480	2190-0376
A8H9	2190-0030	1	12	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0030
A8H10	3050-0791	6	12	INSULATOR-XSTR NYLON	28480	3050-0791
A8H11	3050-0457	3	12	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0457
A8MP1	01980-20601	1	1	HEAT SINK PANEL	28480	01980-20601
A8MP2	0340-0956	7	4	INSULATOR-MICA	28480	0340-0956
A8Q1	1854-0663	3	3	TRANSISTOR	28480	1854-0663
A8Q2	1854-0803	3	2	TRANSISTOR NPN SI TO-220AB P[illegible]2W	01295	TIP75B
A8Q3	1854-0663	3		TRANSISTOR	28480	1854-0663
A8Q4	1854-0828	2	2	TRANSISTOR NPN SI TO-220AB PD=65W	01295	TIP-122
A8Q5	1854-0663	3		TRANSISTOR	28480	1854-0663
A8Q6	1854-0[illegible]	2		TRANSISTOR NPN SI TO-220AB PD=65W	01295	TIP-122
A8Q7	1854-0803	3		TRANSISTOR NPN SI TO-220AB PD=2W	01295	TIP75B
A8Q8	1853-0498	0	1	TRANSISTOR	01295	TIP145
A8U1	1826-0620	3	1	IC	28480	1826-0620
A8U2	1826-0294	7	2	IC V RGLTR TO-220	04713	MC7905CT
A8U3	1826-0106	0	1	IC 7815 V RGLTR TO-220	04713	MC7815CP
A8U4	1826-0294	7		IC V RGLTR TO-220	04713	MC7905CT
A9A1	01980-66537	9	1	HEAT SINK BOARD ASSEMBLY	28480	01980-66537
A9A1C1	0160-3508	9	2	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A9A1E1	1200-0462	5	12	SOCKET-IC 1-CONT STRIP DIP-SLDR	28480	1200-0462
A9A1J1	1251-6546	6	4	SOCKET	28480	1251-6546
A9A1J2	1200-0661	0	8	SOCKET-XSTR 3-CONT PLST PWR DIP-SLDR	28480	1200-0661
A9A2	01980-66536	8	1	HEAT SINK BOARD ASSEMBLY	28480	01980-66536
A9A2C1	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A9A2E1	1200-0462	5		SOCKET-IC 1-CONT STRIP DIP-SLDR	28480	1200-0462
A9A2J1	1251-6610	4	1	SOCKET	28480	1251-6610
A9A2J2	1200-0661	6		SOCKET-XSTR 3-CONT PLST PWR DIP-SLDR	28480	1200-0661
A9A2U1	1826-0760	2	1	IC	27014	LM335AZ

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12	01980-60209	0	1	BNC PANEL ASSEMBLY	28480	01980-60209
A12BT1	1420-0273	2	1	BATTERY 3V 1.2A-HR LI/S DIOX FLAT	28480	1420-0273
A12H1	2200-0147	4	4	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A12H2	2190-0019	6	4	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
A12H3	2950-0043	8	7	NUT-HEX-DBL CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A12H4	3050-0106	6	4	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0106
A12H5	0360-1632	0	7	TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	28480	0360-1632
A12J1	1250-0118	3	7	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
A12J2	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
A12J3	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
A12J6	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
A12J7	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
A12J10	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
A12J11	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
A12MP1	5041-3068	7	1	BATTERY HOLDER	28480	5041-3068
A12A1	01980-00203	8	1	PANEL-BNC	28480	01980-00203
A12A2	01980-66526	6	1	BNC PANEL BOARD ASSEMBLY	28480	01980-66526
A12A2F1	2110-0077	8	1	FUSE 1.25A 125V .281X.093	28480	2110-0077
A12A2J4	1251-4836	2	1	CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251-4836
A12A2J5	1251-5000	0	1	CONNECTOR 5-PIN M METRIC POST TYPE	28480	1251-5000
A12A2J8	1251-4837	1	1	CONNECTOR 4-PIN M METRIC POST TYPE	28480	1251-4837
A12A2J9	1251-5971	8	1	CONNECTOR 3-PIN M METRIC POST TYPE	28480	1251-5971
A12A2S1	3101-0433	2	1	SWITCH-SL DPDT STD 2A 250VAC PC	28480	3101-0433

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13	01980-63401	0	1	VERTICAL ATTENUATOR ASSEMBLY	28480	01980-63401
A13C1	0160-3443	1	2	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A13C2	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A13E1	NSR	4	4	PROBE TAG, NSR (ORDER 01980-24301)	28480	NSR
A13E2	NSR	4		PROBE TAG, NSR (ORDER 01980-24301)	28480	NSR
A13E3	1251-6116	6	2	CONNECTOR-ELASTOMERIC	28480	1251-6116
A13E4	1251-6116	6		CONNECTOR-ELASTOMERIC	28480	1251-6116
A13E5	0360-0037	7	2	TERMINAL-SLDR LUG PL MTG FOR #8 SCR	28480	0360-0037
A13H1	2950-0043	8	1	NUT-HEX-DBL CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A13H2	2200-0757	2	10	SCREW-MACH 4-40 1.25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A13H3	2190-0016	3	1	WASHER-LK INTL 7.3/8 IN .377-IN ID	28480	2190-0016
A13H4	2190-0019	4	1	WASHER-LK HLCL NO. 4 .115-IN ID	28480	2190-0019
A13H5	2200-0115	6	7	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A13H6	01980-09105	7	1	WASHER, GROUNDING CLIP	28480	01980-09105
A13J1	1250-1669	1	2	CONNECTOR-RF BNC FEM SGL-HOLE-FR	28480	1250-1669
A13J2	1250-1669	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR	28480	1250-1669
A13MP1	01980-06202	7	2	RELAY-HOUSING	28480	01980-06202
A13MP2	01980-20603	4	1	SHIELD-LOWER	28480	01980-20603
A13MP3	0060-2004	5	1	SHIELD-UPPER	28480	0060-2004
A13MP4	01980-45001	8	16	ARMATURE	28480	01980-45001
A13MP5	01980-00603	2	1	SHIELD-DECOUPLE-RIGHT	28480	01980-00603
A13MP6	01980-00605	4	1	SHIELD-DECOUPLE-CENTER	28480	01980-00605
A13MP7	01980-00604	3	1	SHIELD-DECOUPLE-LEFT	28480	01980-00604
A13MP8	01980-40203	6	1	PANEL-TRIM-TIME-VT	28480	01980-40203
A13MP9	7121-0626	9	1	LABEL-VERT ATTEN	28480	7121-0626
A13MP10	01980-24301	7	1	PANEL-BNC VOLTAGE	28480	01980-24301
A13MP11	4040-1452	8	2	ELASTOMERIC RETAINER	28480	4040-1452
A13MP12	1400-0065	6		PIN-DWL ANSI-HDND/GND .0930-IN-DIA	28480	1400-0065
A13MP13	01980-09106	8	1	GROUND CLIP	28480	01980-09106
A13MP14	01980-23702	9	4	CLAMPING BAR	28480	01980-23702
A13A1	01980-63502	4	1	BOARD ASSEMBLY VERTICAL ATTENUATOR KIT	28480	01980-63502
A13A1C1	NSR	4			28480	NSR
A13A1C2	NSR	4			28480	NSR
A13A1C3	NSR	4			28480	NSR
A13A1C4	NSR	4			28480	NSR
A13A1C5	NSR	4			28480	NSR
A13A1C6	NSR	4			28480	NSR
A13A1C7	NSR	4			28480	NSR
A13A1C8	NSR	4			28480	NSR
A13A1C9	NSR	4			28480	NSR
A13A1C10	NSR	4			28480	NSR
A13A1C11	NSR	4			28480	NSR
A13A1C12	NSR	4			28480	NSR
A13A1C13	NSR	4			28480	NSR
A13A1C14	NSR	4			28480	NSR
A13A1C15	NSR	4			28480	NSR
A13A1C16	NSR	4			28480	NSR
A13A1C17	NSR	4			28480	NSR
A13A1C18	NSR	4			28480	NSR
A13A1C19	NSR	4			28480	NSR
A13A1C20	NSR	4			28480	NSR
A13A1C21	NSR	4			28480	NSR
A13A1C22	NSR	4			28480	NSR
A13A1C23	NSR	4			28480	NSR
A13A1C24	NSR	4			28480	NSR
A13A1CR1	NSR	4			28480	NSR
A13A1CR2	NSR	4			28480	NSR
A13A1Q1	1855-0426	8	2	TRANSISTOR-JFET DUAL N-CHAN D-MODE	28480	1855-0426
A13A1Q2	1855-0426	8		TRANSISTOR-JFET DUAL N-CHAN D-MODE	28480	1855-0426
A13A1R1	0698-8648	7	2	RESISTOR 50 2% 5W MO	28480	0698-8648
A13A1R2	NSR	4			28480	NSR
A13A1R3	NSR	4			28480	NSR
A13A1R4	NSR	4			28480	NSR
A13A1R5	NSR	4			28480	NSR
A13A1R6	NSR	4			28480	NSR
A13A1R7	NSR	4			28480	NSR
A13A1R8	NSR	4			28480	NSR
A13A1R9	NSR	4			28480	NSR
A13A1R10	NSR	4			28480	NSR

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13A1R11	NSR	4			28480	NSR
A13A1R12	NSR	4			28480	NSR
A13A1R13	NSR	4			28480	NSR
A13A1R14	NSR	4			28480	NSR
A13A1R15	NSR	4			28480	NSR
A13A1R16	0698-6648	7		RESISTOR 50 2% 5W MO	28480	0698-6648
A13A1R17	NSR	4			28480	NSR
A13A1R18	NSR	4			28480	NSR
A13A1R19	NSR	4			28480	NSR
A13A1R20	NSR	4			28480	NSR
A13A1R21	NSR	4			28480	NSR
A13A1R22	NSR	4			28480	NSR
A13A1R23	NSR	4			28480	NSR
A13A1R24	NSR	4			28480	NSR
A13A1R26	NSR	4			28480	NSR
A13A1R26	NSR	4			28480	NSR
A13A1R27	NSR	4			28480	NSR
A13A1R28	NSR	4			28480	NSR
A13A1R29	NSR	4			28480	NSR
A13A1R30	NSR	4			28480	NSR
A13A1S1-A13A1S16	NSR	4			28480	NSR
A13A1A1	NSR	4		CAP BRACKET ASSEMBLY-CH 1	28480	NSR
A13A1A1C1	NSR	4			28480	NSR
A13A1A1C2	NSR	4			28480	NSR
A13A1A1L1	NSR	4			28480	NSR
A13A1A1R1	NSR	4			28480	NSR
A13A1A2	NSR	4		CAP BRACKET ASSEMBLY CH 2 NSR-NOT SEPARATELY REPLACEABLE- ORDER 01980-66515	28480	NSR
A13A1A2C1	NSR	4			28480	NSR
A13A1A2C2	NSR	4			28480	NSR
A13A1A2L1	NSR	4			28480	NSR
A13A1A2R1	NSR	4			28480	NSR
A13A2	01980-66516	4	1	VERICAL SOLENOID BOARD ASSEMBLY	28480	01980-66516
A13A2C1	0160-0309	4	1	CAPACITOR-FXD 4.7UF±20% 10VDC TA	56289	1500475X0010A2
A13A2CR1	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13A2J1	1251-6607	9	1	CONNECTOR	28480	1251-6607
A13A2L1-A13A2L16	0491-0103	5	16	SOLENOID-COIL 15V	28480	0491-0103
A13A2R1	0684-1041	1	1	RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
A13A2U1	1820-1662	3	2	IC SHF-RGTR CMOS SERIAL-IN PRL-OUT 8-BIT	01928	CD4094BE
A13A2U2	1820-1662	3		IC SHF-RGTR CMOS SERIAL-IN PRL-OUT 8-BIT	01928	CD4094BE
A13A2U3	1858-0061	3	2	TRANSISTOR ARRAY 16-PIN PLSTC DIP	13606	ULN-2004A
A13A2U4	1858-0061	3		TRANSISTOR ARRAY 16-PIN PLSTC DIP	13606	ULN-2004A
A13A2XU1	1200-0607	0	4	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A13A2XU2	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A13A2XU3	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A13A2XU4	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A14	01980-63402	1	1	TRIGGER ATTENUATOR ASSEMBLY	28480	01980-63402
A14C1	0160-3443	1	2	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A14C2	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A14E1	NSR	4	2		28480	NSR
A14E2	NSR	4			28480	NSR
A14E3	1251-6116	6	2	CONNECTOR-ELASTOMERIC	28480	1251-6116
A14E4	1251-6116	6		CONNECTOR-ELASTOMERIC	28480	1251-6116
A14E6	0360-0037	7		TERMINAL-SLDR LUG PL-MTG FOR #6 SCR	28480	0360-0037
A14H1	2950-0043	8	2	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A14H2	2200-0757	2	8	SCREW-MACH 4-40 1.25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A14H3	2190-0016	3	2	WASHER-LK HTL T 3/8 IN .377-IN-ID	28480	2190-0016
A14H4	2190-0019	6	8	WASHER-LK HTL NO. 4 .115-IN-ID	28480	2190-0019
A14H5	2200-0115	6	7	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A14H6	2200-0103	2	2	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A14J1	1250-1669	1	2	CONNECTOR-RF BNC FEM SGL-HOLE-FR	28480	1250-1669
A14J2	1250-1669	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR	28480	1250-1669
A14MP1	01980-05202	7	2	RELAY HOUSING	28480	01980-05202
A14MP2	01980-20603	4	1	SHIELD-LOWER	28480	01980-20603
A14MP3	0050-2004	5	1	SHIELD-UPPER	28480	0050-2004
A14MP4	01980-45001	8	11	ARMATURE	28480	01980-45001
A14MP5	01980-00603	2	1	SHIELD-DECOUPLE-RIGHT	28480	01980-00603
A14MP6	01980-00604	3	1	SHIELD-DECOUPLE-LEFT	28480	01980-00604
A14MP7	01980-00605	4	1	SHIELD-DECOUPLE-CENTER	28480	01980-00605
A14MP8	01980-40203	6	1	PANEL-TRIM-TIME/VT	28480	01980-40203
A14MP9	7121-0627	1	1	LABEL-TRIGGER ATTENUATOR	28480	7121-0627
A14MP10	01980-24302	8	1	PANEL-BNC TIME	28480	01980-24302
A14MP11	4040-1452	8	2	ELASTOMERIC RETAINER	28480	4040-1452
A14MP12	1480-0065	6	2	PIN-DWL ANSI-HDND/GND .0930-IN-DIA	28480	1480-0065
A14MP13	01980-09106	8	1	GROUND CUP	28480	01980-09106
A14MP14	01980-23702	9	4	CLAMPING B-R	28480	01980-23702
A14A1	01980-69503	5	1	BOARD ASSY-TRIGGER ATTENUATOR KIT	28480	01980-69503
A14A1C1	NSR	4			28480	NSR
A14A1C2	NSR	4			28480	NSR
A14A1C3	NSR	4			28480	NSR
A14A1C4	NSR	4			28480	NSR
A14A1C5	NSR	4			28480	NSR
A14A1C6	NSR	4			28480	NSR
A14A1C7	NSR	4			28480	NSR
A14A1C8	NSR	4			28480	NSR
A14A1C9	NSR	4			28480	NSR
A14A1C10	NSR	4			28480	NSR
A14A1C11	NSR	4			28480	NSR
A14A1C12	NSR	4			28480	NSR
A14A1C13	NSR	4			28480	NSR
A14A1C14	NSR	4			28480	NSR
A14A1C15	NSR	4			28480	NSR
A14A1C16	NSR	4			28480	NSR
A14A1C17	NSR	4			28480	NSR
A14A1C18	NSR	4			28480	NSR
A14A1C19	NSR	4			28480	NSR
A14A1C20	NSR	4			28480	NSR
A14A1CR1	NSR	4			28480	NSR
A14A1CR2	NSR	4			28480	NSR
A14A1L1	NSR	4			28480	NSR
A14A1L2	NSR	4			28480	NSR
A14A1Q1	1855-0262	0	2	TRANSISTOR-JFET DUAL N-CHAN D-MODE SI	28480	1855-0262
A14A1Q2	1855-0262	0		TRANSISTOR-JFET DUAL N-CHAN D-MODE SI	28480	1855-0262
A14A1R1	0698-6648	7	2	RESISTOR 50 2% .5W MO TC 0+150	28480	0698-6648
A14A1R2	NSR	4			28480	NSR
A14A1R3	NSR	4			28480	NSR
A14A1R4	NSR	4			28480	NSR
A14A1R5	NSR	4			28480	NSR
A14A1R6	NSR	4			28480	NSR
A14A1R7	NSR	4			28480	NSR
A14A1R8	NSR	4			28480	NSR
A14A1R9	NSR	4			28480	NSR
A14A1R10	NSR	4			28480	NSR

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A14A1R11	0698-8648	7		RESISTOR 60 2% 6W MO TC-0±150	28480	0698 8648
A14A1R12	NSR	4			28480	NSR
A14A1R13	NSR	4			28480	NSR
A14A1R14	NSR	4			28480	NSR
A14A1R15	NSR	4			28480	NSR
A14A1R16	NSR	4			28480	NSR
A14A1R17	NSR	4			28480	NSR
A14A1R18	NSR	4			28480	NSR
A14A1R19	NSR	4			28480	NSR
A14A1R20	NSR	4			28480	NSR
A14A1S1-A14A1S11	NSR	4			28480	NSR
A14A2	01980-66518	6	1	BOARD ASSEMBLY-TRIGGER SOLENOID	28480	01980 66518
A14A2C1	0180 0309	4	1	CAPACITOR-FXD 7UF±20% 10VDC TA	56289	150D475X0010A2
A14A2CR1	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A14A2J1	1251-6607	9	1	CONNECTOR	28480	1251 6607
A14A2L1-A14A2L11	0490-0103	3	11	SOLENOID-COIL, 15V	28480	0490 0103
A14A2R1	0684-1041	1	1	RESISTOR 100K 10% 25W FC TC=-400/+800	01121	CB1041
A14A2U1	1820-1602	3	1	IC SHF-RGTR CMOS SERIAL IN PRL-OUT 8-BIT	01928	CD4094BE
A14A2U2	1858 0061	3	2	TRANSISTOR ARRAY 16 PIN PLSTC DIP	13606	ULN 2004A
A14A2U3	1858-0061	3		TRANSISTOR ARRAY 16 PIN PLSTC DIP	13606	ULN 2004A
A14A2XU1	1200-0607	0	3	SOCKET-IC 16-CONT DIP DIP SLDR	28480	1200 0607
A14A2XU2	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200 0607
A14A2XU3	1200 0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200 0607

See Introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A15	01980-60203	4	1	CONTROL PANEL ASSEMBLY	28480	01980-60203
A15E1	1251-6168	7	2	CONNECTOR-ELASTAMERIC	28480	1251-6168
A15E2	1251-6168	7		CONNECTOR-ELASTAMERIC	28480	1251-6168
A15H1	01980-26301	1	2	BAYONET LATCH	28480	01980-26301
A15H2	2200-0106	4	1	SCREW-MACH 4-40 .312-IN-LG PAN HD-POZI	00000	ORDER BY DESCRIPTION
A15H3	3030-0007	5	4	SCREW-SET 4-40 .125-IN-LG SMALL CUP-PT	00000	ORDER BY DESCRIPTION
A15H4	3030-0005	3	1	SCREW-SET 8-32 .125-IN-LG SMALL CUP-PT	00000	ORDER BY DESCRIPTION
A15H6	2950-0043	8	1	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A15MP1	01980-44701	3	1	SUPPORT-SHAFT	28480	01980-44701
A15MP2	01980-67401	8	1	KNOB-FOCUS	28480	01980-67401
A15MP3	01980-67402	9	1	KNOB-SCALE	28480	01980-67402
A15MP4	01980-61001	2	1	SHAFT ASSEMBLY-RPG	28480	01980-61001
A15MP5	0370-3025	0	1	KNOB ASSEMBLY	28480	0370-3025
A15R1	2100-3804	4	1	RESISTOR-VAR DUAL 2.5M-10%-C 100-10%-C	28480	2100-3804
A15A1	01980-66512	0	1	LAMP BOARD-CONTROL	28480	01980-66512
A15A1C1	0160-3638	6	1	CAPACITOR-FXD 0.22UF ±20% 200VDC CER	28480	0160-3638
A15A1CR1	1901-0050	3	1	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A15A1DS1	1990-0735	8	2	DISPLAY-NUM-SEG 4 CHAR .11-H RED	28480	1990-0735
A15A1DS2	1990-0735	8		DISPLAY-NUM-SEG 4 CHAR .11-H RED	28480	1990-0735
A15A1DS3	2140-0508	3	1	LAMP-INCAND	28480	2140-0508
A15A1E1	0360-1646	6	1	TERMINAL-STUD SPCL-FDTHRU PRESS-MTG	28480	0360-1646
A15A1J1	1251-6570	5	1	CONNECTOR	28480	1251-6570
A15A1J2	1251-6545	4	1	CONNECTOR	28480	1251-6545
A15A1R1	2100-3252	6	1	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
A15A1R2	2100-3214	0	1	RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	28480	2100-3214
A15A2	01980-60211	4	1	FRONT PANEL CONTROL	28480	01980-60211

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Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				PARTS LIST FOR STANDARD DISPLAY PANEL		
A16	01980-60204	5	1	DISPLAY PANEL ASSEMBLY	28480	01980-60204
A16E1	1251-6119	8	1	CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6119
A16H1	01980-26301	1	2	BAYONET LATCH	28480	01980-26301
A16H2	2200-0105	4	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A16A1	01980-66533	5	1	PC BOARD ASSEMBLY-DISPLAY	28480	01980-66533
A16A1DS1	2140-0427	5	4	LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1DS2	2140-0427	5		LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1DS3	2140-0427	5		LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1DS4	2140-0427	5		LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1J1	1251-6606	8	1	CONNECTOR	28480	1251-6606
A16A2	01980-60210	3	1	FRONT PANEL ASSEMBLY	28480	01980-60210
				PARTS LIST FOR OPTION 860 DISPLAY PANEL		
A16	01980-60214	7	1	DISPLAY PANEL ASSEMBLY (OPT 860)	28480	01980-60214
A16E1	1251-6119	8	1	CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6119
A16H1	01980-26301	1	2	BAYONET-LATCH	28480	01980-26301
A16H2	2200-0105	4	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A16A1	01980-66533	5	1	PC BOARD ASSEMBLY-DISPLAY	28480	01980-66533
A16A1DS1	2140-0427	5	4	LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1DS2	2140-0427	5		LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1DS3	2140-0427	5		LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1DS4	2140-0427	5		LAMP-INCAND 5VDC 60MA T-1-BULB	28480	2140-0427
A16A1J1	1251-6606	8	1	CONNECTOR	28480	1251-6606
A16A2	01980-60215	8	1	FRONT PANEL ASSEMBLY (OPT 860)	28480	01980-60215

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Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A17	01980-60202	3	1	VOLT PANEL ASSEMBLY	28480	01980-60202
A17E1	1251-6118	8	2	CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6119
A17E2	1251-6110	8		CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6119
A17H1	01980-26302		2	BAYONET-LATCH	28480	01980-26302
A17H2	2200-0105		5	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A17H3	01980-26303	3	2	NUT, ADJUSTABLE LATCH	28480	01980-26303
A17A1	01980-66531	3	2	PC BOARD ASSEMBLY-VOLT	28480	01980-66531
A17A1U1	1KB1-5010	1	1	LAMP DRIVER	28480	1KB1-5010
A17A2	01980-60212	6	2	FRONT PANEL ASSEMBLY	28480	01980-60212
				DOES NOT INCLUDE U1		
A17A2C1	0160-3508	9	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A17A2C2	0160-3470	4	1	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A17A2CR1	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A17A2CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A17A2CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A17A2DS1-A17A2DS25	2140-0427	5	25	LAMP-INCAND 6VDC 60MA T-1-BULB	28480	2140-0427
A17A2J1	1251-6578	3	1	CONNECTOR	28480	1251-6578
A17A2XU1	1200-0641	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0641
A18	01980-60201	2	1	TIME PANEL ASSEMBLY	28480	01980-60201
A18E1	1251-6119	8	2	CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6119
A18E2	1251-6119	8		CONNECTOR-ELASTOMERIC COMPRESSION RANGE	28480	1251-6119
A18H1	01980-26302	2	2	BAYONET-LATCH	28480	01980-26302
A18H2	2200-0105	4	5	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A18H3	01980-26303	3	2	NUT, ADJUSTABLE LATCH	28480	01980-26303
A18A1	01980-66530	2	1	PC BOARD ASSEMBLY-TIME	28480	01980-66530
A18A1C1	0160-3508	9	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A18A1C2	0160-3470	4	1	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A18A1CR1	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A18A1CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A18A1CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A18A1DS1-A18A1DS41	2140-0427	5	41	LAMP-INCAND 6VDC 60MA T-1-BULB	28480	2140-0427
A18A1J1	1251-6578	3	1	CONNECTOR 34 PIN M POST TYPE	28480	1251-6578
A18A1U1	1KB1-5010	1	2	LAMP DRIVER	28480	1KB1-5010
A18A1U2	1KB1-5010	1		LAMP DRIVER	28480	1KB1-5010
A18A1XU1	1200-0641	1	2	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0641
A18A1XU2	1200-0641	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0641
A18A2	01980-60213	6	1	FRONT PANEL ASSEMBLY	28480	01980-60213

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A20	01980-60602	7	1	CRT DISPLAY ASSEMBLY	28480	01980-60602
A20A1	01980-20601	6	1	SHIELD ASSEMBLY-CRT	28480	01980-20601
A20A2	01701-66001	5	1	COIL ASSEMBLY-ALIGN, SMALL	28480	01701-66001
A20A3	01980-65501	6	1	COIL ASSEMBLY-LARGE	28480	01980-65601
A20H1	2200-0101	0	2	SCREW-MACH 4-40 188-IN-LG PAN HD-POZI	00000	ORDER BY DESCRIPTION
A20H2	2190-0019	6	2	WASHER-LK HLCL NO .4 .115-IN-ID	28480	2190-0019
A20H3	2360-0117	0	4	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A20H4	2200-0139	4	2	SCREW-MACH 4-40 .25 IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A20H5	3050-0010	2	2	WASHER-FL MTLC NO .6 .147-IN-ID	28480	3050-0010
A20H6	2360-0113	2	2	SCREW MACH 6-32 .25-IN-LG	00000	ORDER BY DESCRIPTION
A20H7	2360-0209	0	4	SCREW-MACH 6-32 .812-IN-LG	00000	ORDER BY DESCRIPTION
A20H8	3050-0071	5	4	WASHER-FL MTLC NO .8	00000	ORDER BY DESCRIPTION
A20H9	2190-0006	1	3	WASHER-LK HLCL NO .6 .141-IN-ID	28480	2190-0006
A20MP1	01980-24701	1	1	CRT/CAMERA MOUNT	28480	01980-24701
A20MP2	7121-0333	7	1	LABEL-IDENT	28480	7121-0333
A20MP3	0400-0001	1	1	GROMMET-RND .562-IN-ID .75-IN-GRV-OD	28480	0400-0001
A20MP4	0400-0002	2	2	GROMMET-RND .188-IN-ID .312-IN-GRV-OD	28480	0400-0002
A20MP5	5041-2617	5	1	SHOCK MOUNT	28480	5041-2617
A20MP6	5041-3042	9	1	SHOCK MOUNT-CRT	28480	5041-3042
A20MP7	01980-20601	2	1	CRT SAFETY SHIELD	28480	01980-20601
A20MP8	01980-20602	3	1	MASK-CRT	28480	01980-20602
A20MP9	0905-0673	2	1	GASKET RND NPRN-FM 1-THK 2.9-OD 2.15-ID	28480	0905-0673
A20MP10	0400-0010	2	2	GROMMET-RND .25-IN-ID	28480	0400-0010
A20MP11	0400-0226	2	1	GROMMET-CHAN	06987	C5G 06-NATURAL
A20MP12	01980-01227	8	1	CLAMP, RING-CRT MOUNT	28480	01980-01227
A20MP13	01980-01228	9	1	BRACKET-CRT MOUNT	28480	01980-01228
A20MP14	5041-3145	3	1	SUPPORT COLLAR-CRT	28480	5041-3145
A20MP15	1400-1163	9	1	HOSE CLAMP	28480	1400-1163
A20V1	5083-5652	9	1	CRT-P31 ALIGNMENT	28480	5083-5652
A20W1	01980-61608	5	1	CABLE-CRT BIAS ASSEMBLY	28480	01980-61608
A23	19842-66503	3	1	BUS INTERFACE BOARD ASSEMBLY	28480	19842-66503
A23C1	0160-2055	9	2	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A23C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A23C3	0160-3622	8	2	CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A23C4	0160-3622	8		CAPACITOR-FXD 1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
A23C5	0180-0226	6	1	CAPACITOR-FXD 22UF±10% 15VDC TA	56289	150D226X9015B2
A23J1	1200-0607	0	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A23J2	1200-0607	0		SOCKET-IC 16-CONT DIP DIP SLDR	28480	1200-0607
A23P1	1251-6661	5	1	CONNECTOR 16-PIN F POST TYPE	28480	1251-6661
A23U1	1818-1639	9	1	IC NMOS (32K) ROM	24840	1818-1639
A23U2	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS06N
A23U3	1820-2549	7	1	HP-IB TALKER/LISTENER CHIP	28480	1820-2549
A23U4	1820-2461	2	2	IC MISC TTL OCTL	04713	MC3447P3
A23U5	1820-2461	2		IC MISC TTL OCTL	04713	MC3447P3
A23W19	8120-3209	1	2	CABLE ASSY 26AWG 16-CNDCT	28480	8120-3209
A23W20	8120-3209	1		CABLE ASSY 26AWG 16-CNDCT	28480	8120-3209
A23XU1	1200-0641	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0641
A23XU3	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A24	19842-66502	8	1	HP-IB CONNECTOR BOARD	28480	19842-66502
A24J1	1251-6667	1	1	CONNECTOR 18-PIN M POST TYPE	28480	1251-6667
A24J2	1251-4040	0	1	CONNECTOR 24-PIN F MICRO RIBBON	28480	1251-4040

See Introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
0027	SCHURTER A G H	LUZERN	SW	
0000	ANY SATISFACTORY SUPPLIER			
003J	NIPPON ELECTRIC CO			
046G	NORELCO NORTH AMER PHILIPS LTG COR	LOS ANGELES	CA	90021
0853	SANGAMO ELEC CO S CAROLINA DIV	PICKENS	SC	29671
0909	KEMET			
1121	ALLEN BRADLEY CO	MILWAUKEE	WI	53204
1295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
1928	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	08876
2111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91746
3868	KDI PYROFILM CORP	WHIPPANY	NJ	07981
4713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
6665	PRECISION MONOLITHICS INC	SANTA CLARA	CA	95050
7263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
3866	SPRAGUE ELECT CO SEMICONDUCTOR DIV	CONCORD	NH	03301
8324	SIGNETICS CORP	SUNNYVALE	CA	94086
9701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
4046	TRANSITRON ELECTRONIC C[illegible] P	WAKEFIELD	MA	01880
4546	CORNING GLASS WORKS [illegible]DFORD)	BRADFORD	PA	16701
6654	VARADYNE INC	SANTA MONICA	CA	90404
7014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
8480	HEWLETT PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
0161	AAVID ENGINEERING INC	LACONIA	NH	03246
2997	BOURNS INC TRIMPOT PROD DIV	RIVERSIDE	CA	92507
4849	INTEL CORP	MOUNTAIN VIEW	CA	95051
0167	MIDWEST COMPONENTS	MUSKEGON	MI	49443
1042	CENTRE E[illegible]GINEERING INC	STATE COLLEGE	PA	16801
2763	STETTNER-TRUSH INC	CAZENOVIA	NY	13035
6289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
0730	THOMAS & BETTS CO THE	ELIZABETH	NJ	07207
2136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226
3138	BECKMAN INSTRUMENTS INC HELIPOT DI	FULLERTON	CA	92634
6042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108
5916	LITTELFUSE INC	DES PLAINES	IL	60016
6385	MINOR RUBBER CO INC	BLOOMFIELD	NJ	07003
8553	TINNERMAN PRODUCTS INC	CLEVELAND	OH	44101
1637	DALE ELECTRONICS INC	COLUMBUS	NE	68601
5987	WECKESSER CO INC	CHICAGO	IL	60641

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

This section normally contains information for adapting this manual to instruments for which the content does not apply directly. Since this manual does apply directly to instruments having serial numbers listed on the title page, no change information is given here. Refer to INSTRUMENTS COVERED BY MANUAL in Section I for additional important information about serial number coverage.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

This section contains schematics, repair and replacement information, component locators, waveforms and test conditions.

8-2. SAFETY CONSIDERATIONS.

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

WARNING

Maintenance described in this section is performed with power supplied to the instrument and with protective covers removed. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed. Read the Safety Summary on back of "Service Manual" tab before attempting repair on this instrument.

CAUTION

Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

CAUTION

This instrument contains multilayer printed circuit boards. Extreme caution should be exercised when soldering or unsoldering components to prevent damage to the circuit boards.

CAUTION

The semiconductor components used in this instrument can be susceptible to damage by electrostatic discharge. These components include CMOS, PMOS, NMOS, ECL, TTL, and linear devices and diodes and transistors. To protect these devices from electrostatic discharge, the following protective items are recommended when repairing the instrument:

1. *A portable field service kit, which includes table top, ground cord, and wrist strap, such as 3M Model 8005 Portable Field Service Kit.*
2. *Grounded soldering iron.*
3. *Antistatic solder sucker.*
4. *Conductive foam for holding and storing unmounted components.*
5. *Antistatic bags for holding and storing printed circuit board assemblies.*

8-3. SERVICE SHEETS.

The service sheet is a unit of information for a circuit which includes a schematic diagram, component locators, testing information, and a list of mnemonics used on the schematic. The service sheet number is a large bold number printed on the lower right-hand corner of each schematic.

8-4. Schematics.

Schematics are printed on foldout pages for easy reference to the text and figures in other sections. The schematics are drawn to show the electronic function of the circuits. Any one schematic may include all or part of several different physical assemblies. Graphic symbols (figure 8-1) used in this manual are based on ANSI Y32.2-1975, Graphic Symbols for Electrical and Electronics Diagrams.

The schematics are numbered in sequence with a bold number at the lower right-hand corner of each page. These numbers are used to cross reference signal connections between the schematics. At circuit breaking points, a number in a circle is shown, followed by another number in bold type. The circled number indicates the signal and the bold number indicates the associated schematic that contains the source or destination of the signal. To find the source or destination of the signal, turn to the indicated schematic and find the circled number.

A table on each schematic lists all components shown on the schematic by reference designation. Component reference designators that have been deleted from the schematic are listed below the table.

All components within the bordered areas of the schematic are physically located on circuit board assemblies. Components not physically located on a circuit board assembly are shown in the unbordered areas of the schematic.

REFER TO ANSI Y 32.2 FOR GRAPHIC SYMBOLS NOT LISTED IN THIS TABLE

CIRCUIT ASSEMBLY BORDERLINE

FRONT-PANEL MARKING

REAR-PANEL MARKING

MAIN SIGNAL PATH

PRIMARY FEEDBACK PATH

SINGLE-PIN CONNECTOR ON BOARD

PIN OF PLUG-IN BOARD OR CABLE

COAXIAL CABLE CONNECTED TO SNAP-ON JACK

COAXIAL CONNECTOR CONNECTED DIRECTLY TO BOARD

BREAKDOWN DIODE (ZENER)

SCHOTTKY (HOT-CARRIER) DIODE

STEP-RECOVERY DIODE

VARACTOR DIODE (VARICAP)

TRIAC

TEMPERATURE SENSOR

DUAL TRANSISTOR

DUAL FIELD-EFFECT TRANSISTOR (N-TYPE BASE)

FERRITE BEAD

THERMISTOR

SOLENOID-ACTUATED SWITCH

GLOW LAMP

TOROIDAL TRANSFORMER

SLIDE SWITCH

RESISTOR JUMPER

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED

CHASSIS GROUND

SOLDER OR MECHANICAL CONNECTION

ELASTOMERIC CONNECTOR

TOOL-AIDED ADJUSTMENT

TP1 NUMBERED TEST POINT. MEASUREMENT AID PROVIDED

LETTERED TEST POINT. NO MEASUREMENT AID PROVIDED

146 SIGNAL REFERENCE

15 SCHEMATIC REFERENCE

INDICATES MULTIPLE PATHS REPRESENTED BY ONE LINE. LETTERS OR NAMES IDENTIFY INDIVIDUAL PATHS. NUMBERS INDICATE NUMBER OF PATHS REPRESENTED BY THE LINE.

923 WIRE COLORS ARE GIVEN BY ENCLOSED NUMBERS USING THE RESISTOR COLOR CODE.

923 IS WHT-RED-GRN

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

Figure 8-1. Graphic Symbols

8-5. Component Locations.

Locations of components on assemblies and subasssemblies are illustrated on line drawings adjacent to the schematics. Since the schematics are drawn to show function, portions of a particular assembly may appear on several different schematics.

8-6. Mnemonics.

Signals on the schematics have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H or L) indicates the active state of the signal. The remainder of the signal name indicates function of the signal. An H prefix indicates the function is active in the high state; an L prefix indicates the function is active in the low state. The mnemonics shown on a schematic (if applicable) are listed on the component locator adjacent to that schematic.

8-7. REFERENCE DESIGNATIONS.

Reference designations used in this manual are based on ANSI Y32.16-1975, Reference Designations for Electrical and Electronics Parts and Equipments. Minor variations from the standard, due to design and manufacturing practices, may be noted.

Each electrical component is assigned a class letter and a number. This letter-number combination is the basic reference designation. Components which are part of an assembly have, in addition to the basic designation, a prefix designation indicating the assembly of which the component is a part. For instance, resistor R23 on assembly A1 is called A1R23.

8-8. LOGIC SYMBOLOGY.

The logic symbols used in this manual are based on ANSI Y32.14-1973, Graphic Symbols for Logic Diagrams (Two-State Devices). Basic logic symbols are shown in figure 8-2. The function labels associated with these symbols are shown in figure 8-3.

8-9. Logic Conventions.

Positive logic convention is used in this manual, unless otherwise noted on the schematics. Positive logic convention defines a logic "1" as the more positive voltage (high) and a logic "0" as the more negative voltage (low).

8-10. Qualifier Symbols.

Qualifier symbols (figure 8-4) indicate the relationship between internal logic states and external logic states.

8-11. Dependency Notation.

Dependency notation is a technique for obtaining simplified symbols for complex elements by defining input/output and input/input relationships, without showing all the elements and interconnections involved. Dependency notation information supplements qualifying symbol information for the function of an element. Logic relationships are shown between inputs and outputs by using the following notation:

A ADDRESS DEPENDENCY — When A-labeled inputs are active, address is selected for A-dependent inputs or outputs.

C CONTROL DEPENDENCY — When C-labeled input is active, C-dependent inputs or outputs have their normally defined effect on the function of the logic element.

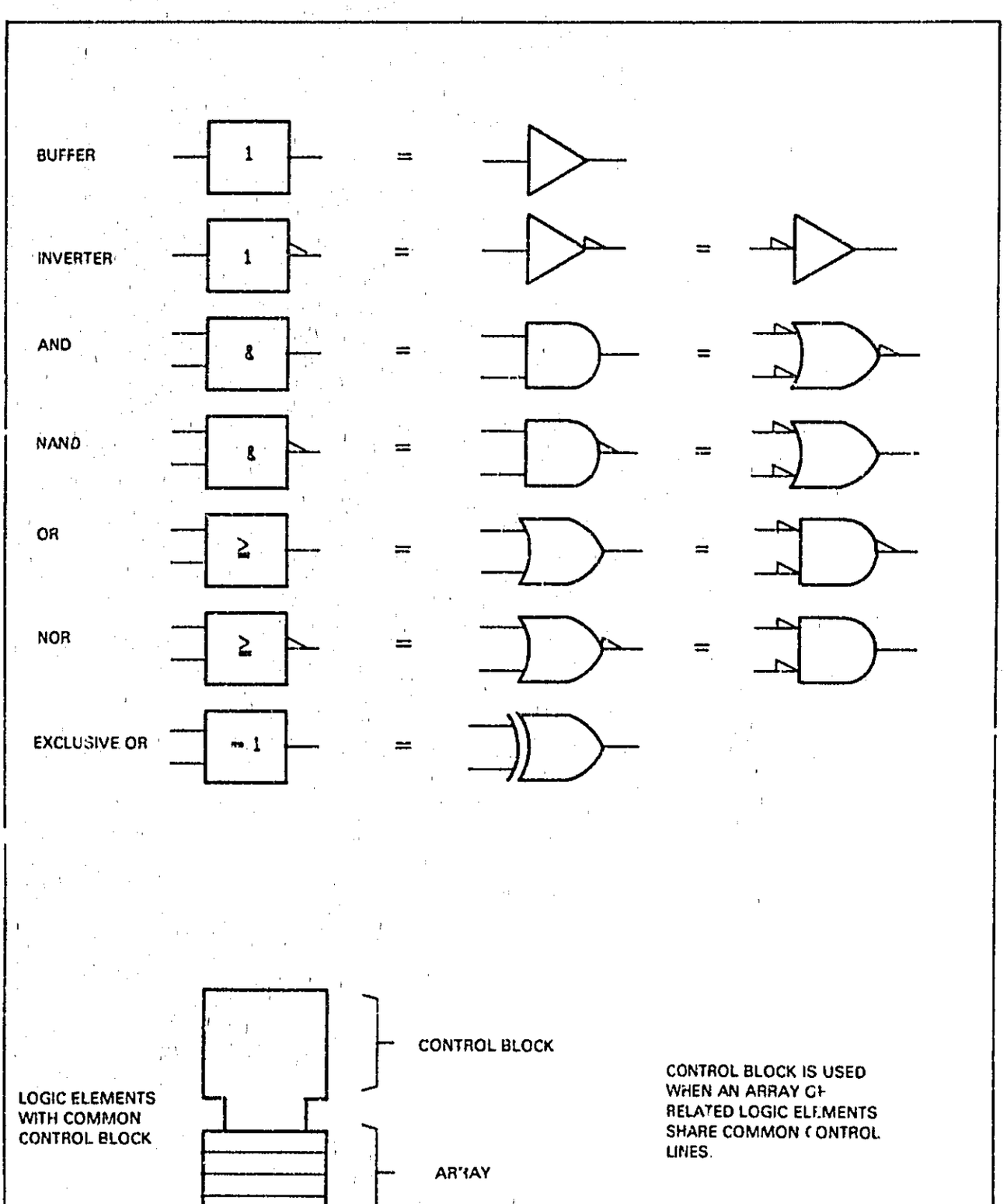


Figure 8-2. Basic Logic Symbols

	AMPLIFIER/BUFFER
1 	MONOSTABLE MULTIVIBRATOR (ONE-SHOT)
&	AND GATE
≥1	OR GATE
=1	EXCLUSIVE OR GATE
X→Y	ENCODER, DECODER
XMAX→Y	PRIORITY ENCODER
CNTR	COUNTER
DEMUX	DEMULTIPLEXER
FF	FLIP-FLOP
RAM	RANDOM-ACCESS MEMORY
REG	REGISTER
ROM	READ-ONLY MEMORY
SAR	SUCCESSIVE APPROXIMATION REGISTER
SEL	SELECTOR
SREG	SHIFT REGISTER
TX/RX	TRANSMITTER/RECEIVER

Figure 8-3. Function Labels

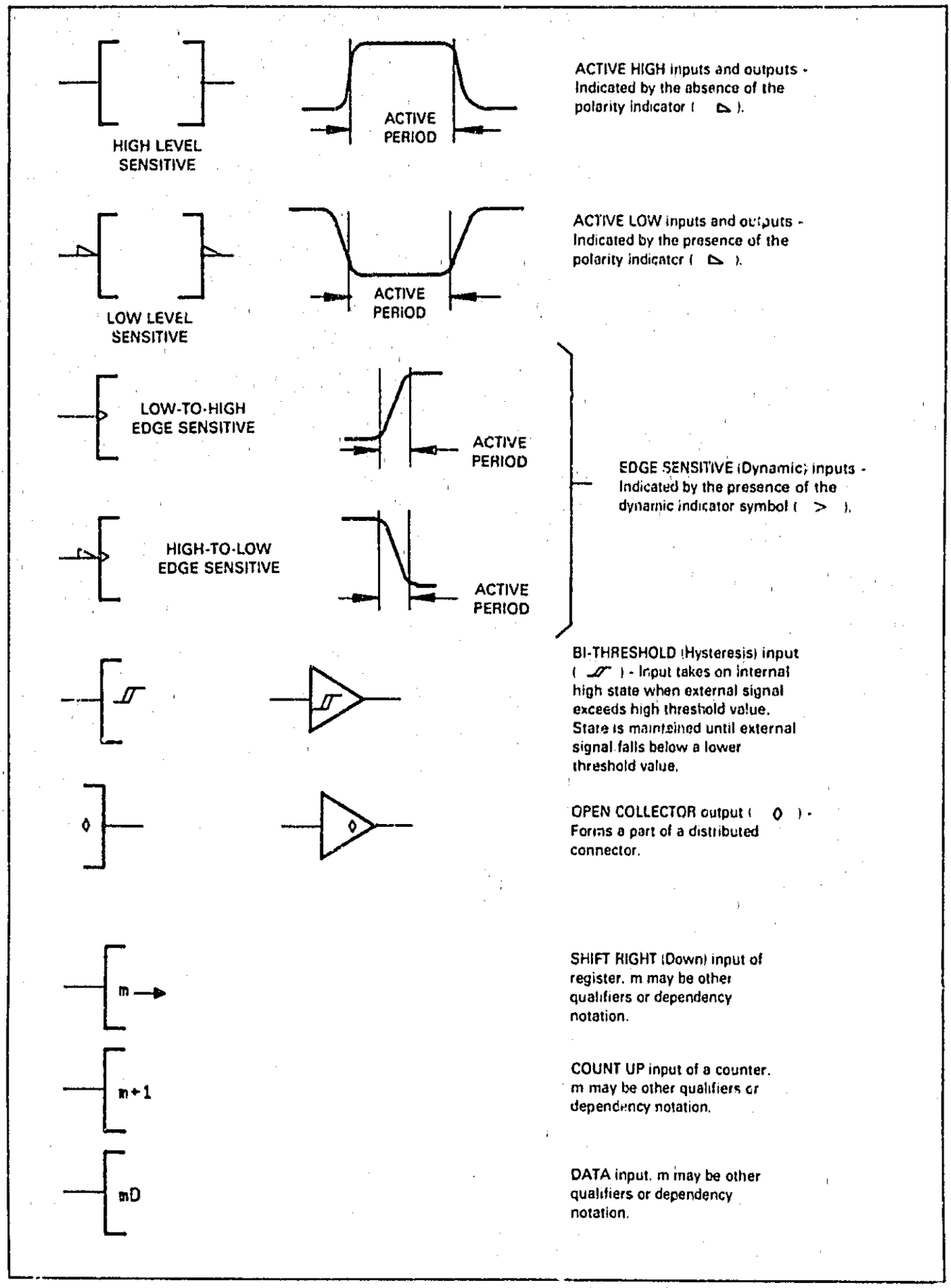


Figure 8-4. Qualifying Symbols

F FREE DEPENDENCY — When F-labeled input is active, F-dependent inputs or outputs function normally. When F-labeled input is inactive, F-dependent inputs or outputs are in high-impedance state (3-state).

G GATE (AND) DEPENDENCY — The G-labeled input gates G-dependent inputs or outputs, and form an AND relationship.

R RESET DEPENDENCY — When R-labeled input is active, a low state is imposed on normally active-high outputs, and a high state is imposed on normally active-low outputs.

S SET DEPENDENCY — When S-labeled input is active, a high state is imposed on normally active-high outputs, and a low state is imposed on normally active-low outputs.

8-12. Complex Devices.

Figure 8-5 illustrates examples of complex logic devices. The examples denote applications of common control blocks, function labels, qualifying symbols, and dependency notation.

8-13. TROUBLESHOOTING.

The troubleshooting flow charts are located on the pages just before the Block Diagrams. These flowcharts are a guideline to locating a problem area, and are not intended to locate the bad component.

Once the problem area or faulty circuit has been located, using the troubleshooting flow charts, signature analysis and conventional troubleshooting methods can be used to find the faulty component.

8-14. SIGNATURE ANALYSIS USING THE HP MODEL 5004A SIGNATURE ANALYZER.

The A4 Processor Board incorporates signature analysis as a troubleshooting aid. Troubleshooting the processor board using signature analysis requires the use of service tool HP Model 5004A Signature Analyzer. The Signature Analyzer receives signals from the circuit under test, compresses them, and displays the result in the form of digital signatures associated with data nodes in the circuit under test.

8-15. Signature Analyzer Features.

Front Panel. The Signature Analyzer has four seven-segment displays on the front panel. A light to the left of the display indicates the presence of an unstable signature. Six pushbutton switches control power on/off, start, stop, and clock edge polarities, a hold mode for single cycle events or freezing the signature, and a self-test mode. Stop, start, clock, and data test sockets on the right-hand side of the front panel are for a self-test diagnostic setup for the Signature Analyzer.

Data Probe. The active Data Probe (commonly referred to as probe) is a hand-held probe that accepts signature information and may also be used as a logic probe. The lamp at the probe tip glows bright for a logic high, turns off for a logic low, blinks when digital activity is present, and glows dimly for a bad logic level, open circuit, or open state of a 3-state device.

Active Test Pod. The Active Test Pod (commonly referred to as pod) houses three identical channels for start, stop, and clock control inputs. The input wires can be plugged directly into a 0.03-inch round socket or connected to a "grabber" which can be connected to a test point, component lead, or IC pin. It may be necessary to extend the length of the input wires of the pod. This can be accomplished by connecting wires of the desired length, with "grabbers" at each end, to the "grabbers" already present at the pod.

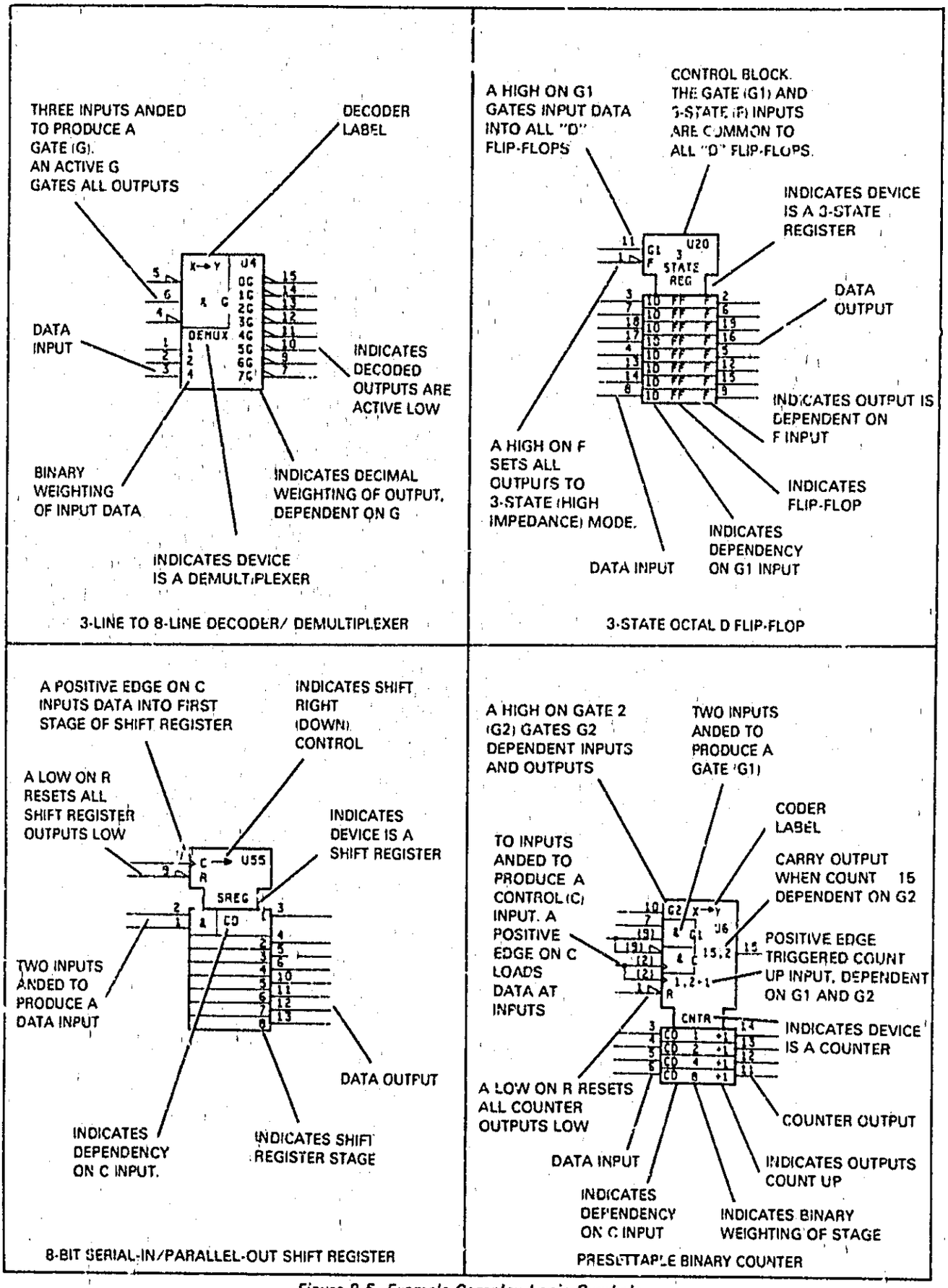


Figure 8-5. Example Complex Logic Symbols

8-16. Signature Analyzer Operation.

Signature Display. The Signature Analyzer uses a compression technique that reduces any long, complex data stream on a logic node into a four-digit signature. The digits used for this signature display are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, C, F, P, and U. The last six digits (letters) were chosen rather than the hexadecimal A, B, C, D, E, and F because the Signature Analyzer uses seven-segment displays. Letters were chosen which could not be confused with similar numerals. For example, an "8" and a "B" would appear exactly the same on a seven-segment display.

Logic data is input to the Signature Analyzer through the probe for each circuit clock cycle that occurs within a circuit controlled time window. Within the Signature Analyzer is a 16-bit shift register. There are 65,536 possible states to which the shift register can become set during a measurement window. These states are encoded and displayed as a signature. This signature is a unique number representing time dependent logic activity during a specified measurement interval for the node being monitored. Because the 1980 A4 Processor Board is put into a software loop by opening or closing switches during signature analysis, the signature taken at a node during the specified setup will always be the same for that node, providing the circuit is functioning properly. Any change in the behavior of the node will produce a different signature indicating a circuit malfunction. The signal that causes the node to produce a signature is the stimulus. The stimulus is provided by the instrument under test in the form of start, stop, and clock signals. Location of these signals to be used for troubleshooting is located in the signature analysis troubleshooting procedures.

When the probe is connected to a logic node whose correct signature is known, a comparison is made, with the circuit functioning at normal operating speed, between the signature displayed on the Signature Analyzer and the correct signature provided in the signature analysis troubleshooting procedures. The comparison of these signatures is the means by which a defective component is located on a printed circuit board.

Unstable Signature. Signature analysis can detect intermittent faults if they occur within a measurement window. However, the Signature Analyzer may not indicate an unstable signature if the measurement cycle time is too short. The UNSTABLE SIGNATURE indicator lamp on the Signature Analyzer will blink indicating an unstable signature if there is a difference between successive signatures input to the analyzer.

Hold Mode. The hold mode of the Signature Analyzer holds the signature present on the display, preventing the gate control from starting another cycle. This mode is useful in testing single-shot events such as start-up sequences. Hold mode is initiated by pushing in the HOLD switch on the front panel of the Signature Analyzer and begins at the end of the current measurement window.

Self-Test. The HP 5004A Signature Analyzer has a built-in self-test function which tests the entire Signature Analyzer except the clock edge select circuit and the ground wire at the pod input. Refer to the Operation section of the HP 5004A Signature Analyzer Operating and Service Manual for detailed self-test procedures.

8-17. Using Signature Analysis Tests.

Signature analysis tests (where applicable) are located adjacent to the affected service sheet.

WARNING

Read the Safety Summary at the front of this manual before performing signature analysis tests.

CAUTION

Always set the 1980 instrument power to off before starting a test setup to ensure that no pins are shorted together while making START, STOP, and CLOCK connections to the processor board.

1. Connect Signature Analyzer START, STOP, and CLOCK leads from the pod to the points listed in the test being performed. Connect the pod GND lead to a convenient chassis ground point on the processor board.

2. Set Signature Analyzer START, STOP, and CLOCK edge polarities to the position listed in the test being performed.

3. Set up the test configuration as indicated in the test being performed, such as connecting or removing jumpers or setting switches.

4. Verify the +5 volt signature in the test being performed. This signature can be verified by either probing the +5 Vdc supply or by pressing and releasing the RESET button on the probe tip while the probe tip is not connected to any signal. A correct +5 volt signature verifies that the START, STOP, and CLOCK signal inputs from the processor board to the Signature Analyzer are functioning properly. If the +5 volt signature is incorrect, check equipment setup configuration and pod connections.

5. Probe the A4 processor board at the test points shown in the signature table in the test being performed. The TEST POINT column lists the test point (colored on the service sheet) and component pin number. The last column lists the service sheet number and the service sheet grid location where the test point is located. For physical location of the test point, refer to the component location diagram of the applicable service sheet.

8-18. PREVENTIVE MAINTENANCE.

8-19. Cleaning.

Painted surfaces can be cleaned with a commercial glass cleaner or with a mild soap and water solution.

CAUTION

Do not use chemical cleaning agents or abrasive cleaners which might damage the plastics used in this instrument. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), or a solution of 1% mild detergent and 99% water.

8-20. CORRECTIVE MAINTENANCE.

8-21. Attenuator Maintenance.

If a problem in the attenuator is suspected, cleaning of the attenuators may solve the problem. The attenuators may be cleaned using the following procedures.

8-22. Vertical Attenuator (A13) Cleaning Procedure.

1. Remove Vertical Attenuator Assembly (A13) as outlined in Vertical Attenuator Assembly (A13) Removal and Replacement Procedure.

Note

Refer to figure 8-14 when performing steps 2 through 12.

2. Remove Vertical Attenuator Housing (MP52) from Vertical Attenuator Assembly (A13) by removing 4 screws (H22).

3. Unsolder probe sense wires (0 and 2 wires) from rear of Vertical Attenuator Solenoid Board Assembly (A13A2) and pull them from between the Relay Housings (A13MP1).

4. Remove 8 screws (A13H2) mounting Relay Housings (A13MP1) to Upper Shield (A13MP3).

Note

When the Relay Housings (A13MP1) and Solenoid Board Assembly (A13A2) are removed from the Upper Shield (A13MP3) the Relay Armatures (A13MP4) will be loose. To avoid "spilling" Relay Armatures (A13MP4) set Attenuator Assembly (A13) on work surface in upright position.

5. With Vertical Attenuator Assembly (A13) on work surface in upright position, lift Relay Housings (A13MP1) and Solenoid Board Assembly (A13A2) straight up until clear of Upper Shield (A13MP3).

6. Carefully remove the Relay Armatures (A13MP4) by turning Attenuator Assembly (A13) over in the palm of hand to catch Relay Armatures (A13MP4).

CAUTION

Clean only with isopropyl alcohol. Do not use any type degreaser or lubricant on this assembly.

7. Place Relay Armatures (A13MP4) in container of isopropyl alcohol and allow to soak for a few minutes.

8. Using a clean cotton swab dipped in isopropyl alcohol, clean the Upper Shield (A13MP3). Insure all areas which will come into contact with Relay Armatures are clean.

CAUTION

Do not allow cotton swab to come into contact with switches on the Attenuator Board (A13A1) as they are easily bent.

9. Remove excess alcohol, lint, and dirt from Upper Shield by blowing clean with a low pressure (less than 30 psi) air gun.

10. Using tweezers remove the Relay Armatures, one at a time, from the container of alcohol and clean with a lint-free cloth.

11. Using tweezers, place Relay Armatures in Upper Shield (A13MP3).

CAUTION

Do not put any pressure on Relay Armatures once they are installed in the Upper Shield. Pressure on the Relay Armatures may distort the switches on the Attenuator Board Assembly (A13A1).

12. Reassemble the Vertical Attenuator Assembly (A13), install Vertical Attenuator Housing (MP52), and reinstall assembly in instrument.

Note

Tighten the 8 screws (A13H2) to 0.565 newton-metre (5 in-lb) torque maximum.

8-23. Trigger Attenuator (A14) Cleaning Procedure.

1. Remove Trigger Attenuator Assembly (A14) as outlined in Trigger Attenuator Assembly (A14) Removal and Replacement Procedure.

Note

Refer to figure 8-15 when performing steps 2 through 12.

2. Remove Trigger Attenuator Housing (MP52) from Trigger Attenuator Assembly (A14) by removing 4 screws (H22).

3. Unsolder probe sense wires (0 and 2 wires) from rear of Trigger Attenuator Solenoid Board Assembly (A14A2) and pull them from between the Relay Housings (A14MP1).

4. Remove 8 screws (A14H2) mounting Relay Housings (A14MP1) to Upper Shield (A14MP3).

Note

When the Relay Housings (A14MP1) and Solenoid Board Assembly (A14A2) are removed from the Upper Shield (A14MP3) the Relay Armatures (A14MP4) will be loose. To avoid "spilling" Relay Armatures (A14MP4) set Attenuator Assembly (A14) on work surface in upright position.

5. With Trigger Attenuator Assembly (A14) on work surface in upright position, lift Relay Housings (A14MP1) and Solenoid Board Assembly (A14A2) straight up until clear of Upper Shield (A14MP3).

6. Carefully remove the Relay Armatures (A14MP4) by turning Attenuator Assembly (A14) over in the palm of hand to catch Relay Armatures (A14MP4). Note position of Relay Armatures (A14MP4) for reinstallation.

CAUTION

Clean only with isopropyl alcohol. Do not use any type degreaser or lubricant on this assembly.

7. Place Relay Armatures (A14MP4) in container of isopropyl alcohol and allow to soak for a few minutes.

CAUTION

Do not allow cotton swab to come into contact with switches on the Attenuator Board (A14A1) as they are easily bent.

8. Using a clean cotton swab dipped in isopropyl alcohol, clean the Upper Shield (A14MP3). Ensure all areas which will come into contact with Relay Armatures are clean.

9. Remove excess alcohol, lint, and dirt from Upper Shield by blowing clean with a low pressure (less than 30 psi) air gun

10. Using tweezers, remove the Relay Armatures, one at a time, from the container of alcohol and clean with a lint-free cloth or tissue.

11. Using tweezers, place Relay Armatures in Upper Shield (A14MP3).

CAUTION

Do not put any pressure on Relay Armatures once they are installed in the Upper Shield. Pressure on the Relay Armatures may distort the switches on the Attenuator Board Assembly (A14A1).

12. Reassemble the Trigger Attenuator Assembly (A14), install Trigger Attenuator Housing (MP52), and reinstall assembly in instrument.

Note

Tighten the 8 screws (A14H2) to 0.565 newton-metre (5 in-lb) torque maximum.

8-24. Elastomeric Connectors.

Many right angle connections within the 1980 are made with elastomeric connectors. These devices are fragile and easily contaminated. They should be handled with extreme care. There is evidence the elastomeric connectors can become contaminated by body oils, therefore, cotton gloves or finger cots should be worn when elastomeric connectors are handled. The elastomeric connectors are also susceptible to corrosion from contaminates leaking through the gold plating on the printed circuit board pads.

The above problems are common to all elastomeric connectors, however, of most concern in the 1980 are the four long connectors used by each of the four major hybrids, (A4U66, A5U1, A5U7, and A5U9). If a problem with hybrid connections (or hybrid failure) is suspected or when replacing a hybrid the following procedure should be followed.

1. Remove the hybrid cover, hybrid, and hybrid carrier.
2. Thoroughly clean the printed circuit board area with isopropyl alcohol.
3. Thoroughly dry the printed circuit board.
4. Apply a very thin film of Cramolin, HP Part Number 6010-0491. This may be accomplished by applying Cramolin with a cotton swab, then remove the excess with a clean dry swab, leaving only the faintest trace of Cramolin film.
5. If the elastomerics exhibit excessive green color or very deep indentations from the printed circuit board pads, replace them with new connectors.

Note

The green color is an indication that the Cramolin encountered corrosion. It is red when applied. Use only the recommended type of Cramolin, HP Part Number 6010-0491, and ensure the directions are followed.

8-25. REMOVAL AND REPLACEMENT.

Instructions for removing and replacing assemblies are shown on pages 8-17 through 8-41. Refer to figures 8-6 through 8-14 for location of parts. The replaceable parts list is provided in section VI.

8-26. COVER REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-9 for part location.

A) Top (MP37) or Bottom (MP38) Cover Removal and Replacement.

1) Remove rear standoffs (MP45) as required.

2) Remove the screw (H34) mounting the handle strap retainer (MP35).

3) Loosen captive screw on rear of top or bottom cover.

Note

Make sure screwdriver (posidrive) remains properly seated during removal and replacement of captive screw. Screws are easily damaged.

4) Slide cover toward rear of instrument until free.

5) Replace cover by reversing steps 1 through 3.

B) Side Covers (MP33 and MP77) Removal and Replacement.

1) Remove top and bottom covers.

2) Remove rear standoff (MP45) as required.

3) Loosen captive screw on rear of side cover.

4) Slide cover toward rear of instrument until free.

5) Replace Side Covers (MP33 and MP77) by reversing steps 1 to 4.

8-27. GATE BOARD ASSEMBLY (A3) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Remove top cover as outlined in Cover Removal Procedure.

2) Remove cable connectors at J1 thru J7 by pulling connectors straight away from pins.

3) Remove connector at transistor (Q1) by pulling connector housing away from transistor. Make note of the wire color orientation so that it can be reinstalled correctly.

4) Remove two leads (93 and 95) from square pin connectors at rear of the board using long nose pliers.

5) Remove 6 retaining screws (H8) (3 each side).

6) Remove board by lifting vertically and allowing the cable connectors to move through the rectangular holes in board.

Note

If the Digital Waveform Storage Option is installed, its vertical leads "straddle" the vertical leads to the CRT. Care must be taken not to remove the Digital Waveform Storage Option board's hook tabs from the deck. The Digital Waveform Storage Boards must remain in place and the Gate board must be lifted off them. When reinstalling the Gate board the Digital Waveform Storage Option boards must be in place and the Gate board set down on them and connected.

7) Reinstall Gate Board Assembly (A3) by reversing the removal procedure. Be sure the P1 connector on the lower side of board is mating with XA3 on the interconnect board before tightening screws.

8-28. CRT ASSEMBLY (A20) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Remove top and bottom covers as outlined in Cover Removal Procedure.

2) Remove Gate board as outlined in Gate Board Removal and Replacement Procedure.

3) Remove Trim Strip (MP21) from top of front casting by inserting a soldering aid in slot close to one end and pulling up. Continue lifting trim strip until it is completely removed.

4) Remove trim strips (MP10) from both sides of front casting by lifting one corner and pulling away from casting.

Note

This trim strip is self-adhesive and care should be exercised to keep the adhesive side clean for reinstallation. If strip cannot be re-used order a new strip.

WARNING

Voltages capable of causing injury or death are present on the Post Accelerator connector even though the instrument is off and power cord is disconnected.

5) Disconnect PA connector by prying male connector from female connector with a large blade screwdriver.

6) Immediately discharge the PA lead to the chassis.

7) Loosen set screw (A15H4) in RPG Shaft Assy (A15MP4).

8) Release Control Panel (A15) from snap mounts by prying upper and lower left corner with a soldering aid.

9) Pull Control Panel out far enough to disconnect connectors at J1 and J2.

10) Continue to pull control panel until the RPG shaft is clear of front panel.

11) Release Display Panel (A16) from snap mounts by prying upper and lower right corners with a soldering aid.

Note

It is not necessary to remove Line Switch Extender or Switch Pushbutton, however, care should be taken not to break Switch Extender.

12) Pull Display Panel (A16) out far enough to disconnect connector at J1.

13) Disconnect CRT socket by alternately prying connector away from CRT on left and right side.

14) Disconnect Vertical and Horizontal plate cables (W10 and W13) from CRT neck pins. Exercise care not to bend CRT neck pins or lead clips. If CRT neck pins are broken, CRT replacement is required.

15) Remove screws (H41) which attach CRT/Camera Mount (A20MP1) to Front Casting (MP20).

16) Disconnect CRT Shock Mount Bracket (A20 MP13) from Deck.

17) Slide CRT Assembly (A20) (includes CRT, shield and CRT/Camera Mount) forward until assembly clears the front panel. During removal make sure all cables are free of obstruction.

18) CRT is installed into instrument by reversing the removal procedure.

Note

Attention must be given to aligning slot at the bottom rear of CRT shield and shoulder rivet on lower sheet metal deck.

8-29. CRT (A20V1) REMOVAL PROCEDURE.

Refer to figure 8-11 for part location.

1) Remove CRT Assembly (A20) as outlined in CRT Assembly (A20) Removal and Replacement Procedure.

2) Remove cable A20W1 from CRT neck pins. Exercise care not to bend CRT neck pins or lead clips. If CRT neck pins are broken, CRT replacement is required.

3) Loosen Hose Clamp (A20MP14) and remove CRT Support Collar (A20MP15) and Hose Clamp by sliding off back of CRT.

4) Remove CRT/Camera Mount (A20MP1) by removing 4 screws (A20H3) from the rear. Bezel is the only thing holding the CRT inside shield, therefore when screws are removed do not allow the CRT to slide forward.

5) Slide the CRT forward until the CRT is clear of the shield. PA lead connector fits through shield grommet snuggly, care should be exercised not to pull hard on CRT if PA connector is impeded by grommet.

8-30. CRT (A20V1) REPLACEMENT PROCEDURE.

Refer to figure 8-11 for part location.

1) Place shock mount belt (A20MP6) over front of CRT, centering top, bottom, and side center creases in belt over center graticule lines. Thicker edge of belt is to front of CRT, cog chamfers are to rear.

2) Align front edge of Shock Mount Belt (A20MP6) flush with front edge of CRT face.

3) Start CRT into shield until PA connector can be inserted through grommet (A20MP3). Continue sliding CRT into shield keeping Shock Mount Belt (A20MP6) in place. Slide CRT into shield as far as it will go.

4) Push rear shock mount (A20MP9) into rear of shield around CRT until rear edge of mount is 1 inch in from rear edge of shield.

5) Insert CRT Mask (A20MP8) into CRT/Camera Mount (A20MP1).

6) Place CRT/Camera Mount (A20MP1) face down on work surface with the larger cast area to the right. Provide protective surface for CRT/Camera Mount to rest on.

7) While holding CRT (A20V1) inside shield (A20A1) insert CRT and shield into CRT/Camera Mount (A20MP1). The PA lead of CRT must be on the right when CRT/Camera Mount is oriented according to step 6. Top and bottom edges of shield must be inside CRT/Camera Mount.

8) Insert four screws (A20H3) through CRT shield flange and into CRT/Camera Mount (A20MP1). Tighten screws alternately until snug.

9) Check alignment between the CRT graticule and top inside edge of CRT/Camera Mount. If they are not parallel proceed to the following steps.

10) Remove four screws (A20H3) just installed.

11) Remove CRT (A20V1) and CRT Shield Assembly (A20A1) from CRT Bezel (A20MP1).

12) Push CRT (A20V1) out of CRT Shield Assembly (A20A1) far enough to reposition Shock Mount Belt (A20MP6).

13) Rotate Shock Mount Belt (A20MP6) in the opposite direction that CRT must rotate for proper alignment. Belt must be lifted slightly when rotated to prevent it from rotating back.

14) To check alignment, repeat steps 7 and 8. If alignment is correct, proceed to step 15. If not, repeat steps 10 through 13.

15) Reinstall Hose Clamp and CRT Support Collar.

16) Reinstall CRT assembly into instrument.

8-31. DISPLAY PANEL ASSEMBLY (A16) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Release Display Panel (A16) from snap mounts by prying upper and lower right corners with a soldering aid

Note

It is not necessary to remove Line Switch Extender or Switch Pushbutton, however, care should be taken not to break Switch Extender.

2) Pull Display Panel out far enough to disconnect connector at J1.

3) Replace Display Panel Assembly (A16) by reversing steps 1 and 2.

8-32. DISPLAY PANEL LAMP (A16DS1-DS4) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-12 for part location.

1) Remove Display Panel as outlined in Display Panel (A16) Removal and Replacement Procedure.

2) Unscrew snap mount studs (A16H1) and screw (A16H2) from rear of Display panel.

3) With Display Panel Assembly (A16) face down, remove Lamp Board Assembly (A16A1) by lifting board vertically. In order to prevent damage to Elastomeric Connector (A16E1) do not allow Lamp Board Assembly to slide.

4) Replace defective bulb.

5) Install Lamp Board Assembly (A16A1) by reversing steps 2 and 3.

6) Reinstall Display Panel Assembly (A16) as outlined in Display Panel Assembly (A16) Removal and Replacement Procedure.

8-33. CONTROL PANEL ASSEMBLY (A15) REMOVAL AND REPLACEMENT PROCEDURE.

F Refer to figure 8-10 for part location.

1) Loosen set screw (A15H4) in RPG Shaft Assembly (A15MP4).

2) Release Control Panel Assembly (A15) by prying upper and lower corners with a soldering aid.

3) Pull Control Panel Assembly (A15) out far enough to disconnect connectors at J1 and J2.

4) Continue to pull Control Panel Assembly (A15) until RPG Shaft Assembly (A15MP4) is clear of front panel.

5) Replace Control Panel Assembly (A15) by reversing steps 1 through 4.

8-34. CONTROL PANEL LAMP (A15A1DS3) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-12 for part location.

1) Remove Control Panel Assembly (A15) as outlined in Control Panel Removal and Replacement Procedure.

1 2) With Control Panel Assembly (A15) face down on work surface, unsolder lamp (A15A1DS3) and remove.

3) Install new lamp.

4) Reinstall Control Panel Assembly (A15).

8-35. ENHANCEMENT MODULE FILLER PANEL (MP39) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-13 for part location.

1) Insert straight bladed screwdriver into slot and pry against lower edge of front casing until Enhancement Module Filler Panel (MP39) is released from snap mount.

2) Replace Enhancement Module Filler Panel (MP39) by aligning snap mount clips to studs on Vertical and Trigger Attenuator Housings and pushing panel into place.

8-36. VOLTAGE PANEL ASSEMBLY (A17) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-13 for part location.

1) Remove Enhancement Module Filler Panel (MP39) as outlined in Enhancement Module Filler Panel Removal and Replacement Procedure, or optional Enhancement Module.

2) Using long nose pliers or soldering aid, pull Slidebar Latch (MP53) on Vertical Attenuator Housing (MP52) toward the Trigger Attenuator until it stops.

3) Pull top of Voltage Panel Assembly (A17) away from Fill Strip (MP49) until it is clear of the Fill Strip.

4) Lift Voltage Panel Assembly (A17) slightly while continuing to pull panel out far enough to disconnect cable.

5) Disconnect connector at J1.

6) Replace Voltage Panel by reversing steps 1 through 5.

CAUTION

Push inward on panel while attempting to push slidebar latch into latched position. Ensure Slidebar Latch (MP53) is fully seated. If not seated properly, it may interfere with removal and replacement of Enhancement Module.

8-37. VOLTAGE PANEL LAMP (A17DS1-DS25) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-12 for part location.

1) Remove Voltage Panel Assembly (A17) as outlined in Voltage Panel Assembly (A17) Removal and Replacement Procedure.

2) Remove Bayonet Latches (A17H1) and screws (A17H2).

3) With Voltage Panel Assembly (A17) face down, remove Lamp Board Assembly (A17A1) by lifting board vertically. To avoid damage to Elastomeric Connectors (A17E1 and A17E2) do not allow Lamp Board Assembly (A17A1) to slide.

Note

To remove and replace bulbs DS2,9, and 12, U1 must be removed from socket to provide access to bulb leads.

4) Replace Lamp Board Assembly (A17A1) by reversing steps 2 and 3.

5) Reinstall Voltage Panel Assembly (A17) as outlined in Voltage Panel Assembly (A17) Removal and Replacement Procedure.

8-38. TIME PANEL ASSEMBLY (A18) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-13 for part location.

1) Remove Enhancement Module Filler Panel (MP39) as outlined in Enhancement Module Filler Panel (MP39) Removal and Replacement Procedure, or Optional Enhancement Module.

2) Using long nose pliers or soldering aid, pull Slidebar Latch (MP53) on Trigger Attenuator Housing (MP54) toward the Voltage Attenuato Assembly until it stops.

3) Pull top of Time Panel Assembly (A18) away from Fill Strip (MP49) until it clears Fill Strip.

4) Lift panel slightly while continuing to pull panel out far enough to disconnect cable.

5) Disconnect connector at J1.

6) Replace Time Panel Assembly (A18) by reversing steps 2 through 5.

CAUTION

Push inward on panel while attempting to push slidebar latch into latched position. Ensure Slidebar Latch (MP53) is fully seated. If not seated properly, it may interfere with removal and replacement of option Enhancement Module.

8-39. TIME PANEL LAMP (A18DS1-DS41) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-12 for part location.

1) Remove Time Panel Assembly (A18) as outlined in Time Panel Assembly (A18) Removal and Replacement Procedure.

2) Remove Bayonet Latches (A18H1) and screws (A18H2).

3) With Time Panel Assembly (A18) face down, remove Lamp Board Assembly (A18A1) by lifting board vertically. To prevent damage to Elastomeric Connectors (A18E1 and A18E2) do not allow Lamp Board Assembly (A18A1) to slide.

Note

To remove and replace bulbs DS9,13,15,16,18, or 24, ICU1 or U2 must be removed from socket to provide access to bulb leads.

4) Replace Lamp Board Assembly (A18A1) by reversing steps 2 and 3.

5) Reinstall Time Panel Assembly (A18) as outlined in Time Panel Assembly Removal and Replacement Procedure.

8-40. RPG ASSEMBLY (A19) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Remove top cover as outlined in Cover Removal and Replacement Procedure.

2) Remove Gate Board Assembly (A3) as outlined in Gate Board Assembly (A3) Removal and Replacement Procedure.

3) Loosen set screw (A15H4) in RPG Shaft Assembly (A15MP4). Remove RPG Shaft Assembly (A15MP4) from RPG Assembly (A19).

4) Disconnect RPG cable (A19W1) from J8 of Processor Board Assembly (A4).

5) Remove nut (H21) from RPG Assembly (A19).

6) Move RPG Assembly (A19) to the rear until the control shaft is clear of mount and remove.

7) Replace RPG Assembly (A19) by reversing steps 1 through 6.

8-41. VERTICAL ATTENUATOR ASSEMBLY (A13) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-13 for part location.

1) Remove bottom cover as outlined in Cover Removal and Replacement Procedure.

2) Remove Enhancement Module Filler Panel (MP39) as outlined in Enhancement Module Filler Panel (MP39) Removal and Replacement Procedure, or optional Enhancement Module.

3) Remove Voltage Panel Assembly (A17) as outlined in Voltage Panel Assembly (A17) Removal and Replacement Procedure.

4) Remove 4 screws (3-H35 and 1-H33) attaching Scope Board Assembly (A5) to Vertical Attenuator Assembly (A13).

5) Remove 2 screws (H36) attaching Vertical Attenuator Assembly (A13) to lower edge of front casting.

6) While gently lifting the right front corner of Scope Board Assembly (A5) slightly, pull Vertical Attenuator Assembly (A13) and Vertical Attenuator Housing (MP52) out until cable connector at rear of Solenoid Board Assembly (A13A2) is accessible.

7) Rotate Vertical Attenuator Assembly (A13) counter-clockwise 90 degrees and remove cable connector. Vertical Attenuator Assembly (A13) is now free to be removed.

8) Install Vertical Attenuator Assembly (A13) by reversing steps 1 through 7 making sure right front corner of Scope Board Assembly (A5) is lifted slightly to prevent damage to Elastomeric connectors on Vertical Attenuator Assembly (A13).

9) Make sure slot in Vertical Attenuator Housing (MP52) is properly aligned and seated under shoulder rivet on Upper Deck (MP39).

8-42. VERTICAL ATTENUATOR DISASSEMBLY.

Refer to figure 8-14 for part location.

A) General.

1) Remove Vertical Attenuator Assembly (A13) as outlined in Vertical Attenuator Assembly (A13) Removal and Replacement Procedure.

2) Remove 9 screws (A13H5) mounting Lower Shield (A13MP2) to Upper Shield (A13MP3).

Note

Three Decoupling Shields (MP5,6, and 7) will be loose when screws are removed and care should be taken not to damage or lose them.

3) Remove Lower Shield (A13MP2) by lifting vertically.

Note

Dowel Pins (A13MP12) may be loose and care should be taken not to lose them.

B) Attenuator Board Assembly (A13A1) Replacement.

1) Unsolder signal leads at BNC connector.

2) Lift Vertical Attenuator Board Assembly (A13A1) up far enough to clear Dowel Pins (A13MP12).

3) Slide Vertical Attenuator Board Assembly (A13A1) rearward until probe sense leads clear the slot in the front of the board.

CAUTION

Do not allow Vertical Attenuator Board Assembly (A13A1) to come any closer to the casting than the Dowel Pins (A13MP12) allow.

Note

The Vertical Attenuator Board Assembly (A13A1) is field serviceable only to the extent of replacing plug-in components. Replacing any other components is not recommended.

4) Install new Vertical Attenuator Board Assembly (A13A1) by reversing steps 2 through 6.

5) Reinstall Vertical Attenuator Assembly (A13).

C) Input FET or 50 ohm Resistor Replacement.

1) Reinstall 2 screws (A13H5) through loops in gold shield plates and tighten until snug.

2) Remove Input FET or 50 ohm resistor as required.

   a) Each FET in Vertical Attenuator Assembly (A13) has one lead soldered into a teflon stand-off. Heat solder until FET can be pulled out of board. Note orientation for installation of new FET.

   b) Resistors can be pulled from socket.

3) Install new FET or 50 ohm resistor.

   a) Insert FET by heating solder and inserting 1 lead into teflon stand-off and the other 5 leads into PC sockets.

   b) Install resistor by pluggir , properly formed leads into sockets.

4) Remove 2 screws (A13H5) from gold shield plates.

5) Reinstall Lower Shield (A13MP2) making sure probe sense wires are not pinched.

6) Reinstall Vertical Attenuator Assembly (A13) into instrument.

8-43. VERTICAL ATTENUATOR SOLENOID BOARD ASSEMBLY (A13A2) OR SOLENOID (A13A2L1-L16) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-14 for part location.

A) General.

CAUTION

Do not attempt to replace attenuator solenoid board or solenoids without a torque indicating screwdriver, such as Snap-on Tools, Co., Torque Driver part no. TQSI.055.

1) Remove Vertical Attenuator Assembly (A13) as outlined in Vertical Attenuator Assembly (A13) Removal and Replacement Procedure.

2) Remove Vertical Attenuator Housing (MP52) from Vertical Attenuator Assembly (A13) by removing 4 screws (H22).

3) Unsolder probe sense wires (0 and 2 wires) from rear of Vertical Attenuator Solenoid Board Assembly (A13A2) and pull them from between the Relay Housings (A13MP1).

4) Remove 8 screws (A13H2) mounting Relay Housings (A13MP1) to Upper Shield (A13MP3).

Note

When the Relay Housings (A13MP1) and Solenoid Board Assembly (A13A2) are removed from the Upper Shield (A13MP3) the Relay Armatures (A13MP4) will be loose. To avoid "spilling" Relay Armatures (A13MP4) set Attenuator Assembly (A13) on work surface in upright position.

5) With Vertical Attenuator Assembly (A13) on work surface in upright position, lift Relay Housings (A13MP1) and Solenoid Board Assembly (A13A2) vertically until clear of Upper Shield (A13MP3).

6) Remove Relay Housings (A13MP1) from Vertical Attenuator Solenoid Board Assembly (A13A2) by gently rocking and pulling apart.

B) Solenoid Board Assembly Replacement.

1) Place Relay Housings (A13MP1) on new Vertical Attenuator Solenoid Board Assembly (A13A2).

Note

Row of 4 pins must be to outside of Solenoid Board Assembly.

2) Carefully set Vertical Attenuator Solenoid Board Assembly (A13A2) with Relay Housings (A13MP1) installed, on Upper Shield (A13MP3).

3) Reinstall 8 screws (A13H2) in Relay Housing (A13MP1).

CAUTION

Tighten the 8 screws (A13H2) to 0.565 newton-metre (5 in/lb) torque maximum.

4) Place Probe Sense wires (0 and 2 wires) between Relay Housings (A13MP1) and solder to new Vertical Attenuator Solenoid Board Assembly (A13A2).

5) Reinstall Vertical Attenuator Housing (MP52) on Vertical Attenuator Assembly (A13).

6) Reinstall Vertical Attenuator Assembly (A13) in instrument.

C) Solenoid (A13A1L1-L16) Replacement.

1) Remove bad solenoid (A13A2L1-L16) by unsoldering leads.

2) Replace solenoid (A13A2L1-L16) making certain the base of coil form is flush against Vertical Attenuator Solenoid Board Assembly (A13A2).

3) Replace Relay Housings (A13MP1) on Vertical Attenuator Solenoid Board Assembly (A13A2).

Note

Row of 4 pins must be to outside of Solenoid Board Assembly.

4) Carefully set Vertical Attenuator Solenoid Board Assembly (A13A2) with Relay Housings (A13MP1) installed, on Upper Shield (A13MP3).

5) Reinstall 8 screws (A13H2) in Relay Housing (A13MP1).

CAUTION

Tighten the 8 screws (A13H2) to 0.565 newton-metre (5 in/lb) torque maximum.

6) Place Probe Sense wires (0 and 2 wires) between Relay Housings (A13MP1) and solder to new Vertical Attenuator Solenoid Board Assembly (A13A2).

7) Reinstall Vertical Attenuator Housing (MP52) on Vertical Attenuator Assembly (A13).

8) Reinstall Vertical Attenuator Assembly (A13) in instrument.

8-44. TRIGGER ATTENUATOR ASSEMBLY (A14) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-13 for part location.

1) Remove bottom cover as outlined in Cover Removal and Replacement Procedure.

2) Remove Enhancement Module Filler Panel (MP39) as outlined in Enhancement Module Filler Panel Removal and Replacement Procedure, or optional Enhancement Module.

3) Remove Time Panel Assembly (A18) as outlined in Time Panel Assembly (A18) Removal and Replacement Procedure.

4) Remove 4 screws (3-H35 and 1-H33) attaching Scope Board Assembly to Trigger Attenuator Assembly (A14).

5) Remove 2 screws (H38) attaching Trigger Attenuator Assembly (A14) to lower edge of front casting.

6) While gently lifting the left front corner of Scope Board Assembly (A5) slightly, pull Trigger Attenuator Assembly (A14) and Trigger Attenuator Housing (MP54) out until cable connector at rear of Solenoid Board Assembly (A14A2) is accessible.

7) Rotate Trigger Attenuator Assembly (A14) clockwise 90 degrees and remove cable connector. Trigger Attenuator Assembly (A14) is now free to be removed.

8) Install Trigger Attenuator Assembly (A14) by reversing steps 1 through 7 making sure left front corner of Scope Board Assembly (A5) is lifted slightly to prevent damage to Elastomeric connectors on Trigger Attenuator Assembly (A14).

9) Make sure slot in Trigger Attenuator Housing (MP54) is properly aligned and seated under shoulder rivet on Upper Deck (MP23).

8-45. TRIGGER ATTENUATOR DISASSEMBLY.

Refer to figure 8-15 for part location.

A) General.

1) Remove Trigger Attenuator Assembly (A14) as outlined in Trigger Attenuator Assembly (A14) Removal and Replacement Procedure.

2) Remove 7 screws (A14H5) mounting Lower Shield (A14MP2) to Upper Shield (A14MP3).

Note

Three Decoupling Shields (MP5,6, and 7) will be loose when screws are removed and care should be taken not to damage or lose them.

3) Remove Lower Shield (A14MP2) by lifting vertically.

Note

Dowel Pins (A14MP12) may be loose and care should be taken not to lose them.

B) Attenuator Board Assembly (A14A1) Replacement.

1) Unsolder signal leads at BNC connector.

2) Lift Trigger Attenuator Board Assembly (A14A1) up far enough to clear Dowel Pins (A14MP12).

3) Slide Trigger Attenuator Board Assembly (A14A1) rearward until probe sense leads clear the slot in the front of the board.

CAUTION

Do not allow Trigger Attenuator Board Assembly (A14A1) to come any closer to the casting than the Dowel Pins (A14MP12) allow.

Note

The Trigger Attenuator Board Assembly (A14A1) is field serviceable only to the extent of replacing plug-in components. Replacing any other components is not recommended.

4) Reinstall Trigger Attenuator Board Assembly (A14A1) by reversing steps 2 through 6.

5) Reinstall Trigger Attenuator Assembly (A14).

C) Input FET or 50 Ohm Resistor Replacement.

1) Remove Input FET or 50 ohm resistor as required.

a) Each FET in Trigger Attenuator Assembly (A14) has one lead soldered into a teflon stand-off. Heat solder until FET can be pulled out of board. Note orientation for installation of new FET.

b) Resistors can be pulled from socket.

2) Install new FET or 50 ohm resistor.

a) Insert FET by heating solder and inserting 1 lead into teflon stand-off and the other 5 leads into PC sockets.

b) Install resistor by plugging properly formed leads into sockets.

3) Reinstall Lower Shield (A14MP2) making sure probe sense wires are not pinched.

4) Reinstall Trigger Attenuator Assembly (A14) into instrument.

8-46. TRIGGER ATTENUATOR SOLENOID BOARD ASSEMBLY (A14A2) OR SOLENOID (A14A2L1-L11) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-15 for part location.

A) General.

CAUTION

Do not attempt to replace solenoid board without a torque indicating screwdriver, such as Snap-on Tools Co., Torque Driver part no. TQSI.055.

1) Remove Trigger Attenuator Assembly (A14) as outlined in Trigger Attenuator Assembly (A14) Removal and Replacement Procedure.

2) Remove Trigger Attenuator Housing (MP52) from Trigger Attenuator Assembly (A14) by removing 4 screws (H22).

3) Unsolder probe sense wires (0 and 2 wires) from rear of Trigger Attenuator Solenoid Board Assembly (A14A2) and pull them from between the Relay Housings (A14MP1).

4) Remove 8 screws (A14H2) mounting Relay Housings (A14MP1) to Upper Shield (A14MP3).

Note

When Relay Housings (A14MP1) and Solenoid Board Assembly (A14A2) are removed from Upper Shield (A14MP3) the Relay Armatures (A14MP4) will be loose. To avoid "spilling" Relay Armatures (A14MP4) set Attenuator Assembly (A14) on work surface in upright position.

5) With Trigger Attenuator Assembly (A14) on work surface in upright position, lift Relay Housings (A14MP1) and Solenoid Board Assembly (A14A2) vertically until clear of Upper Shield (A14MP3).

6) Remove Relay Housings (A14MP1) from Trigger Attenuator Solenoid Board Assembly (A14A2) by gently rocking and pulling apart.

B) Solenoid Board Assembly Replacement.

1) Place Relay Housings (A14MP1) on new Trigger Attenuator Solenoid Board Assembly (A14A2).

Note

Row of 4 pins must be to outside of Solenoid Board Assembly.

2) Carefully set Trigger Attenuator Solenoid Board Assembly (A14A2) with Relay Housings (A14MP1) installed, on Upper Shield (A14MP3).

3) Reinstall 8 screws (A14H20) in Relay Housing (A14MP1).

CAUTION

Tighten the 8 screws (A14H2) to 0.565 newton-metre (5 in-lb) torque maximum.

4) Place Probe Sense wires (0 and 2 wires) between Relay Housings (A14MP1) and solder to new Trigger Attenuator Solenoid Board Assembly (A14A2).

5) Reinstall Trigger Attenuator Housing (MP52) on Trigger Attenuator Assembly (A14).

6) Reinstall Trigger Attenuator Assembly (A14) in instrument.

C) Solenoid (A14A2L1-L11) Replacement.

1) Remove bad solenoid (A14A2L1-L11) by unsoldering leads.

2) Replace solenoid (A14A2L1-L11) making certain the base of coil form is flush against Trigger Attenuator Solenoid Board Assembly (A14A2).

3) Replace Relay Housings (A14MP1) on Trigger Attenuator Solenoid Board Assembly (A14A2).

Note

Row of 4 pins must be to outside of Solenoid Board Assembly.

4) Carefully set Trigger Attenuator Solenoid Board Assembly (A14A2) with Relay Housings (A14MP1) installed, on Upper Shield (A14MP3).

5) Reinstall 8 screws (A14H2) in Relay Housing (A14MP1).

CAUTION

Tighten the 8 screws (A14H2) to 0.565 newton-metre (5 in-lb) torque maximum.

6) Place Probe Sense wires (0 and 2 wires) between Relay Housings (A14MP1) and solder to new Trigger Attenuator Solenoid Board Assembly (A14A2).

7) Reinstall Trigger Attenuator Housing (MP52) on Trigger Attenuator Assembly (A14).

8) Reinstall Trigger Attenuator Assembly (A14) in instrument.

8-47. HP-IB BOARD ASSEMBLY (A23) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Remove right side cover as outlined in Cover Removal and Replacement Procedure.

2) Remove 4 screws (H8) mounting HP-IB Board Assembly (A23) to HVPS Cover (MP6).

3) Disconnect cables at J9 and J10 of Processor Board Assembly (A4).

4) Remove HP-IB Board Assembly (A23) from instrument.

Note

The rear of HP-IB Board Assembly (A23) is connected to pin connectors and if not removed by pulling straight out, connector damage may result.

5) Replace HP-IB Board Assembly (A23) by reversing steps 2 through 4.

8-48. HIGH VOLTAGE POWER SUPPLY BOARD ASSEMBLY (A2) OR HIGH VOLTAGE MULTIPLIER (A11) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Remove top cover as outlined in Cover Removal and Replacement Procedure.

2) Remove Gate Board as outlined in Gate Board Assembly (A3) Removal and Replacement Procedure.

3) Remove HP-IB Board Assembly (A23) as outlined in HP-IB Board Assembly (A23) Removal and Replacement Procedure.

WARNING

Voltages capable of causing injury or death are present in the High Voltage Power Supply. Exercise caution if troubleshooting is necessary with power applied.

4) Remove High Voltage Power Supply Cover (MP6) by removing 4 screws (H8) and lifting cover. Lift front of cover slightly and move forward, under processor board. Then lift rear of cover and remove.

5) Disconnect Multiplier Assembly (A11) ground wire from connector pin located at the front-right corner of HV Power Supply Board Assembly (A2).

6) Disconnect PA connector by prying male connector from female connector with a large blade screwdriver. Immediately discharge PA connector to chassis.

7) Disconnect CRT Socket and lift it up and out of instrument.

8) Remove screw (H8) from bottom of HV Powar Supply Board Assembly (A2).

9) Lift HV Box, HV Board and HV Multiplier, up and out of instrument.

10) Disconnect J1 from HV Power Supply Board Assembly (A2).

11) Remove and Replace HV Power Supply Board Assembly (A2) or High Voltage Multiplier Assembly (A11).

8-49. HV TRANSFORMER ASSEMBLY (A2A1) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Remove Top Cover as outlined in Cover Removal and Replacement Procedure.

2) Remove HP-IB Board Assembly (A23) as outlined in HP-IB Board Assembly Removal and Replacement Procedure.

3) Remove Gate Board Assembly (A3) as outlined in Gate Board Assembly (A3) Removal and Replacement Procedure.

4) Remove HV Power Supply Board Assembly (A2) as outlined in HV Power Supply Assembly (A2) or HV Multiplier (A11) Removal and Replacement Procedure.

5) Unsolder filament leads (2-yellow wires) from bottom side of HV Power Supply Board Assembly (A2).

6) Unsolder HV Rectifier (A2CR1) from HV Transformer Assembly (A2A1).

7) Unsolder 7 bus wires from HV Transformer Assembly (A2A1).

Note

Care must be exercised when unsoldering bus wires since they will be used when installing new Transformer (T1).

8) Remove 2 nylon screws (A2H1) holding HV Transformer Assembly (A2A1) to ceramic stand-offs (A2MP1).

9) Place new Transformer Assembly (A2A1) in slot in HV Power Supply Board Assembly (A2), making sure each bus wire is properly aligned with the corresponding hole.

10) Insert nylon screws (A2MP1) and tighten until snug. Do not over tighten screws.

11) Solder bus wires and reconnect HV Rectifier (A2CR1).

12) Install HV Power Supply Board Assembly (A2) by reversing steps 1 to 9.

8-50. BATTERY (A12BT1) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-17 for part location.

1) Remove 4 screws (H8) mounting BNC Panel Assembly (A12) to Rear Panel (MP8).

2) Pull BNC Panel Assembly (A12) out and rotate bottom of BNC Panel Assembly (A12) away from Rear Panel.

CAUTION

To prevent excessive current flow from the battery during the replacement process, make sure power cord and all cables are disconnected from the instrument.

3) Remove screws (A12H1) attaching Battery Holder (A12MP1) to BNC Panel Board Assembly (A12A1).

4) Unsolder battery wires from battery terminals.

5) Solder battery wires to terminals of new battery.

6) Place new battery into Battery Holder making sure battery leads are properly routed in slots of battery holder.

7) Replace BNC Panel Assembly (A12) by reversing steps 1 and 2.

8) Perform a Normal Calibration, Section 5, Paragraph 5-7.

8-51. FAN (A9B1) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-16 for part location.

1) Turn instrument off and remove power cord.

2) Remove 4 screws (H33) mounting Heat Sink Assembly (A9) to Rear Panel (MP8).

3) Pull Heat Sink Assembly (A9) away from Rear Panel far enough to unplug cables.

4) Remove 4 screws (A9H7) and spacers (A9H2) mounting Fan (A9B1) to Heat Sink Assembly (A9).

5) Lift fan (A9B1) clear of Heat Sink Assembly (A9).

Note

Note position of wires and fan orientation for installation of new fan.

6) Unsolder wires from terminals.

7) Solder wires to terminals of new fan as removed in step 6

8) Position new fan into Heat Sink Assembly (A9). Ensure the new fan is orientated the same as the one that was removed.

CAUTION

Make sure wires are not pinched between Fan (A9B1) and Heat Sink Assembly (A9).

9) Replace 4 screws (A9H7) and spacers (A9H2) removed in step 2.

10) Reconnect cables that were removed in step 3.

11) Replace Heat Sink Assembly (A9) on Rear Panel.

12) Replace power cord and energize instrument to check fan operation.

Note

Fan should start as soon as power is applied. If fan does not start, remove power from instrument and check for binding, faulty electrical connections or pinched wires.

8-52. LVPS BOARD ASSEMBLY (A1) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-13 for part location.

1) Remove left side cover as outlined in Cover Removal Procedure.

2) Remove cable connectors at J2, J3, J4, J5, J6, J7, J8, J11, J12, and J17 of LVPS Board Assembly (A1) by pulling connectors straight away from pins.

3) Remove 2 and 9 wires from pin connectors.

4) Remove Connector Holders (E1 and E2) from J1 and XA7 of LVPS Board Assembly (A1)

5) Remove 9 retaining screws (H8)

6) Lift LVPS Board Assembly (A1) vertically far enough to disconnect cables.

7) Disconnect 3 and 9 wires from pin connectors on bottom of board.

8) Remove LVPS Board Assembly (A1).

9) Reinstall LVPS Board Assembly (A1) by reversing the removal procedure. Be sure the P1 connector on the lower side of board is mating with XA1 on the Interconnect Board Assembly (A6) before tightening screws.

8-53. PROCESSOR BOARD ASSEMBLY (A4) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-10 for part location.

1) Remove right side cover as outlined in Cover Removal Procedure.

2) Remove cable connectors at J2, J4, J5, J8, J9, J10, J11, and J12, of Processor Board Assembly (A4) by pulling connectors straight away from pins.

3) Unsolder BATT wires (0 and 2 wires) from Processor Board Assembly (A4).

4) Remove 7 retaining screws (H8).

5) Lift Processor Board Assembly (A4) vertically approx. 2 inches.

6) Disconnect cables at J6 and J7 of Processor Board Assembly (A4).

7) Remove Processor Board Assembly (A4).

8) Reinstall Processor Board Assembly (A4) by reversing the removal procedure. Be sure the P1 connector on the lower side of board is mating with XA4 on the Interconnect Board Assembly (A6) before tightening screws.

9) Perform a Normal Calibration. Refer to Calibration Procedure Section 4.

8-54. SCOPE BOARD ASSEMBLY (A5) REMOVAL AND REPLACEMENT PROCEDURE.

Refer to figure 8-13 for part location.

1) Remove Enhancement Module if installed.

2) Remove bottom cover as outlined in Cover Removal Procedure.

3) Remove cable connectors at J1, J2, J4, J5, J6, J7, J10, and J11 of Scope Board Assembly (A5) by pulling connectors straight away from pins.

4) Remove 2 screws (H19) mounting horizontal hybrid heat sink (MP46) to horizontal heat sink bracket (MP47).

5) Remove 14 retaining screws (6-H35, 6-H8, and 2-H33).

6) Lift Scope Board Assembly (A5) vertically far enough to disconnect cables.

7) Disconnect cables at J3 and J9 of Scope Board Assembly (A5).

8) Remove Scope Board Assembly (A5).

9) Reinstall Scope Board Assembly (A5) by reversing the removal procedure. Be sure the P1 connector on the circuit side of board is mating with XA5 on the Interconnect Board Assembly (A6) before tightening screws.

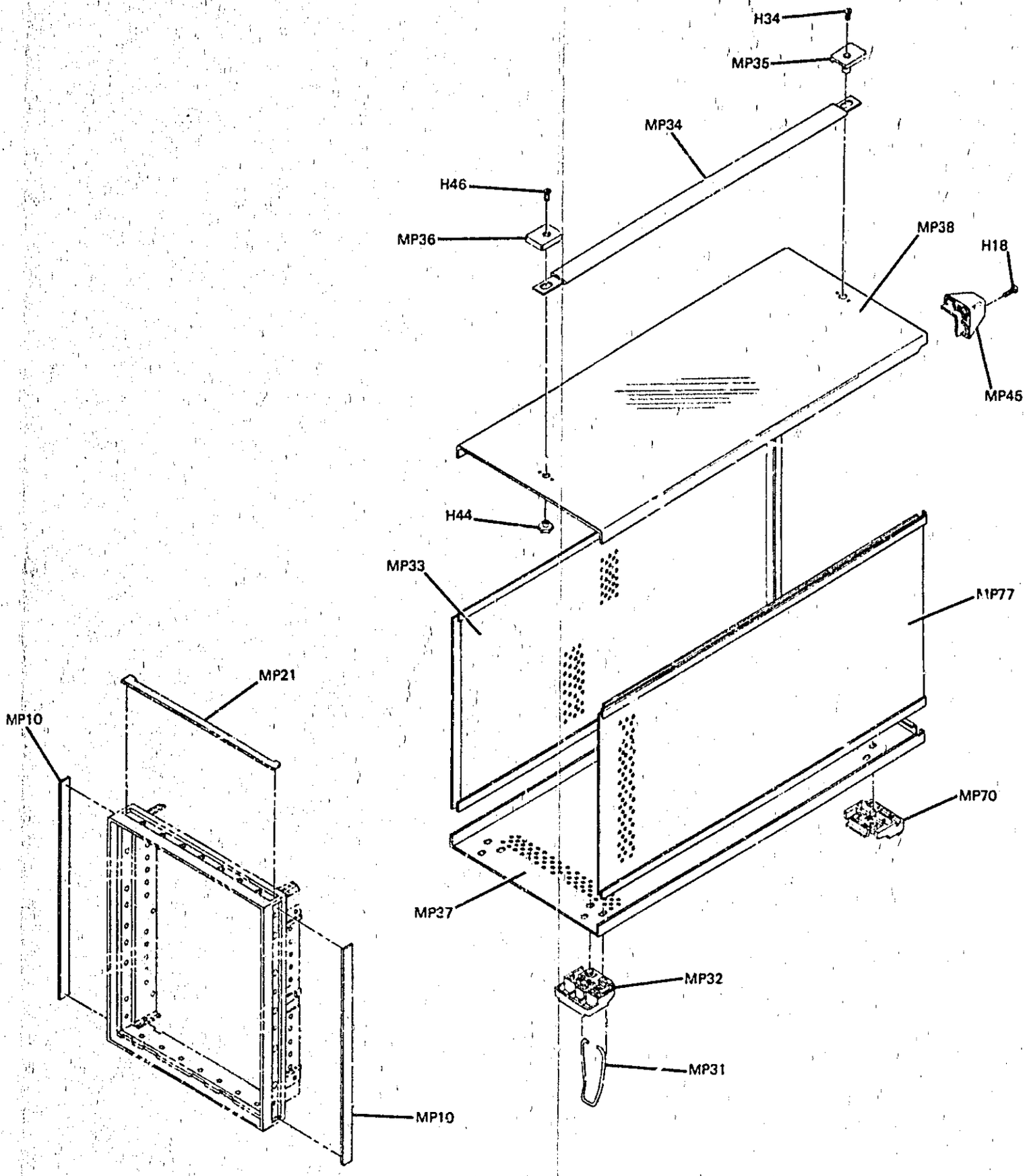


Figure 8-66.
Covers and Trim Part Locations

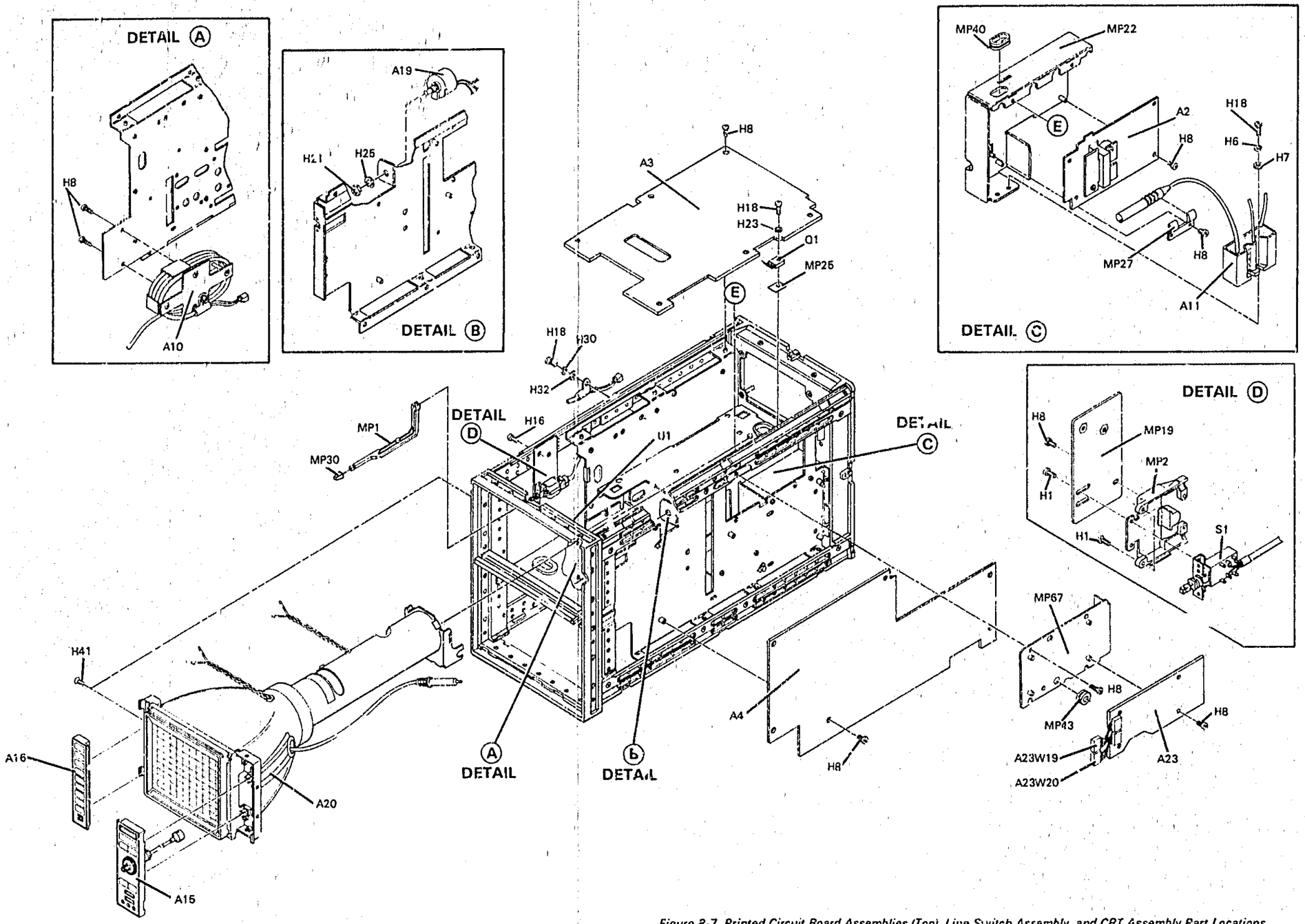


Figure 8-7. Printed Circuit Board Assemblies (Top), Line Switch Assembly, and CRT Assembly Part Locations

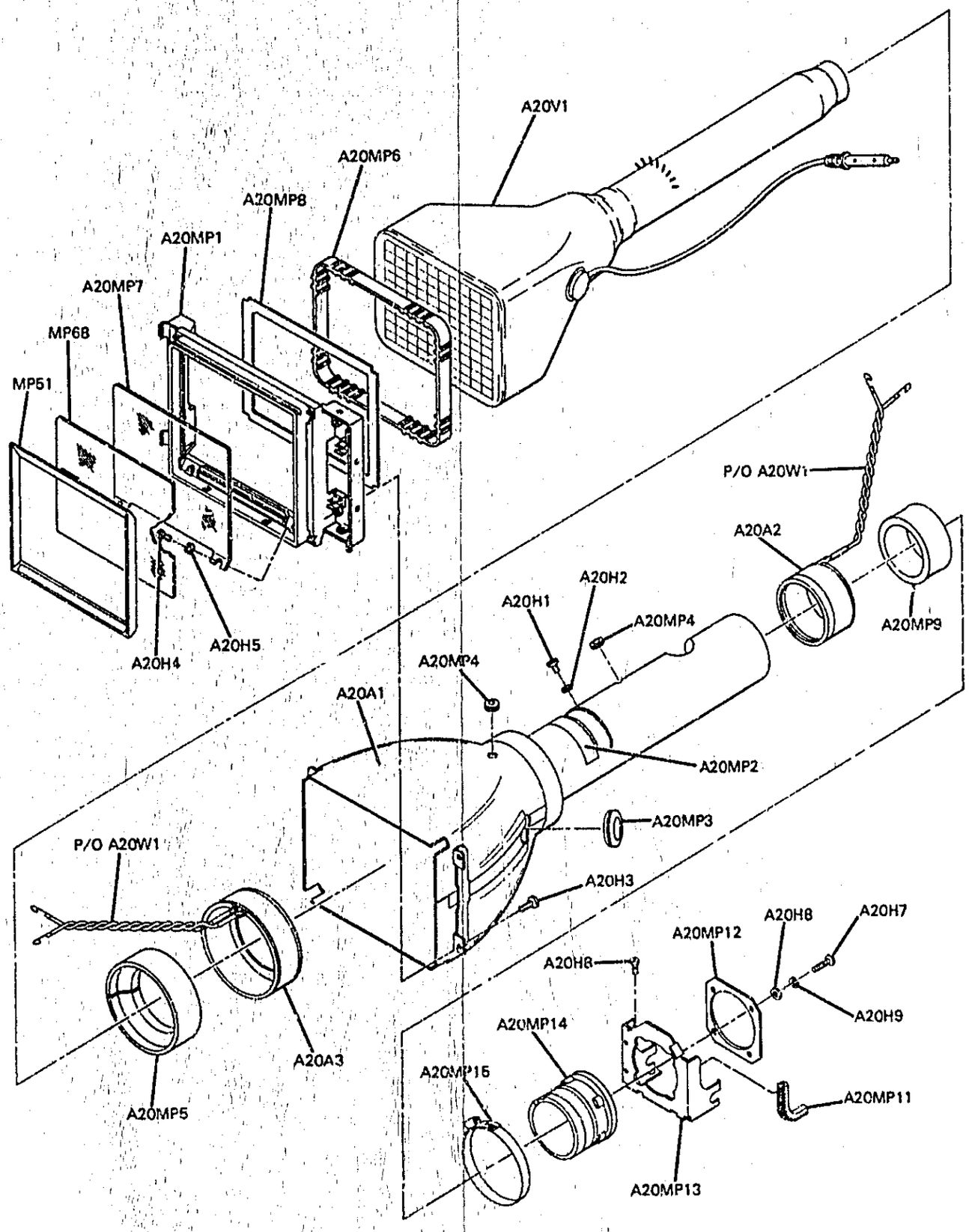
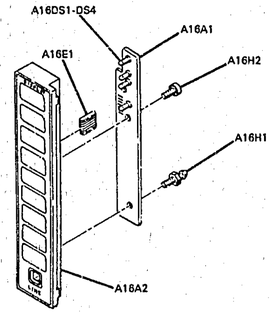
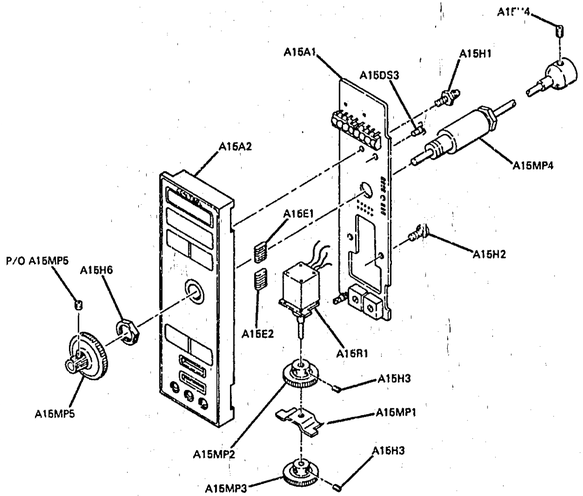


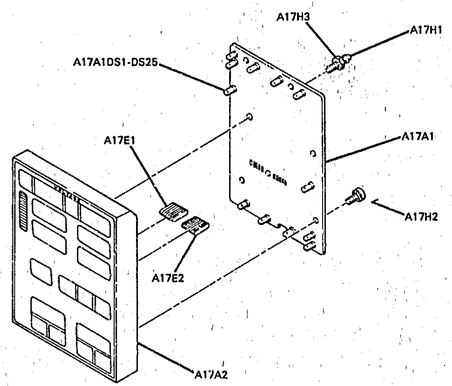
Figure 8-8.
CRT Assembly Part Locations



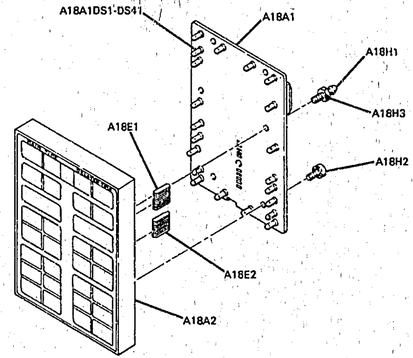
DISPLAY PANEL



CONTROL PANEL



VOLTAGE PANEL



TIME PANEL

Figure 8-9.
Display Panel, Control Panel, Voltage Panel, and Time Panel Part Locations

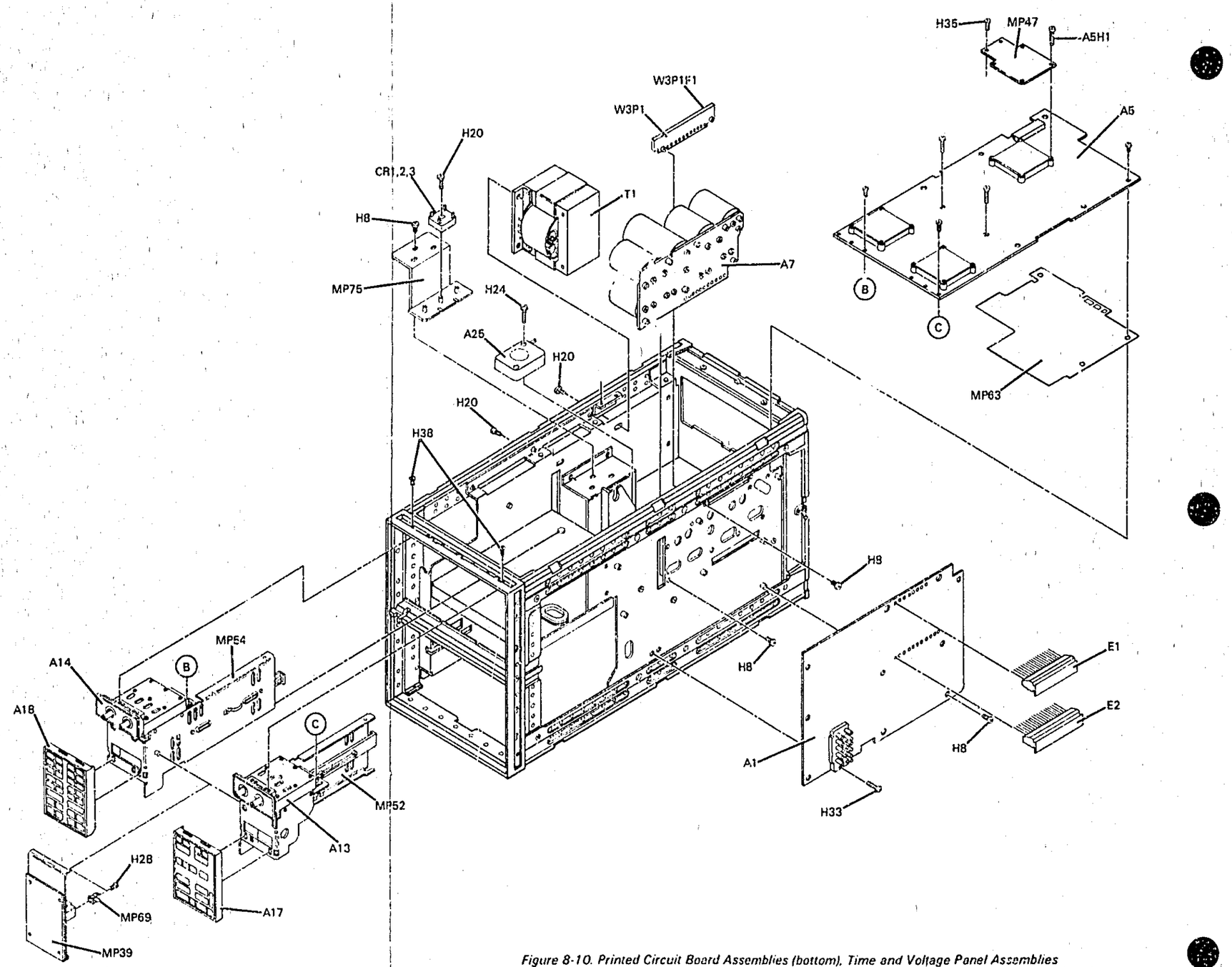


Figure 8-10. Printed Circuit Board Assemblies (bottom), Time and Voltage Panel Assemblies and Attenuator Assemblies Part Locations

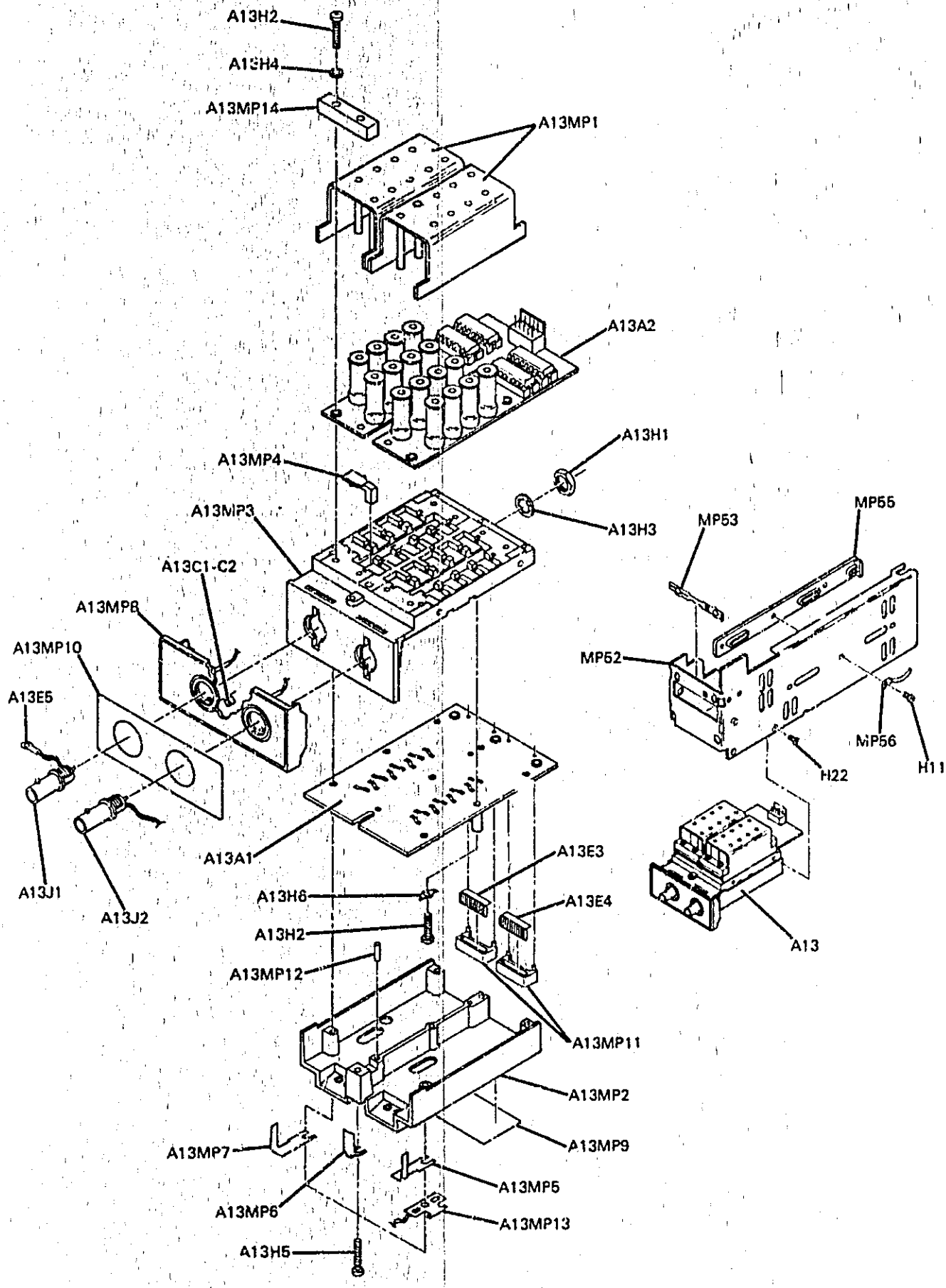


Figure 8-11.
Vertical Attenuator Assembly (A13) Part Locations

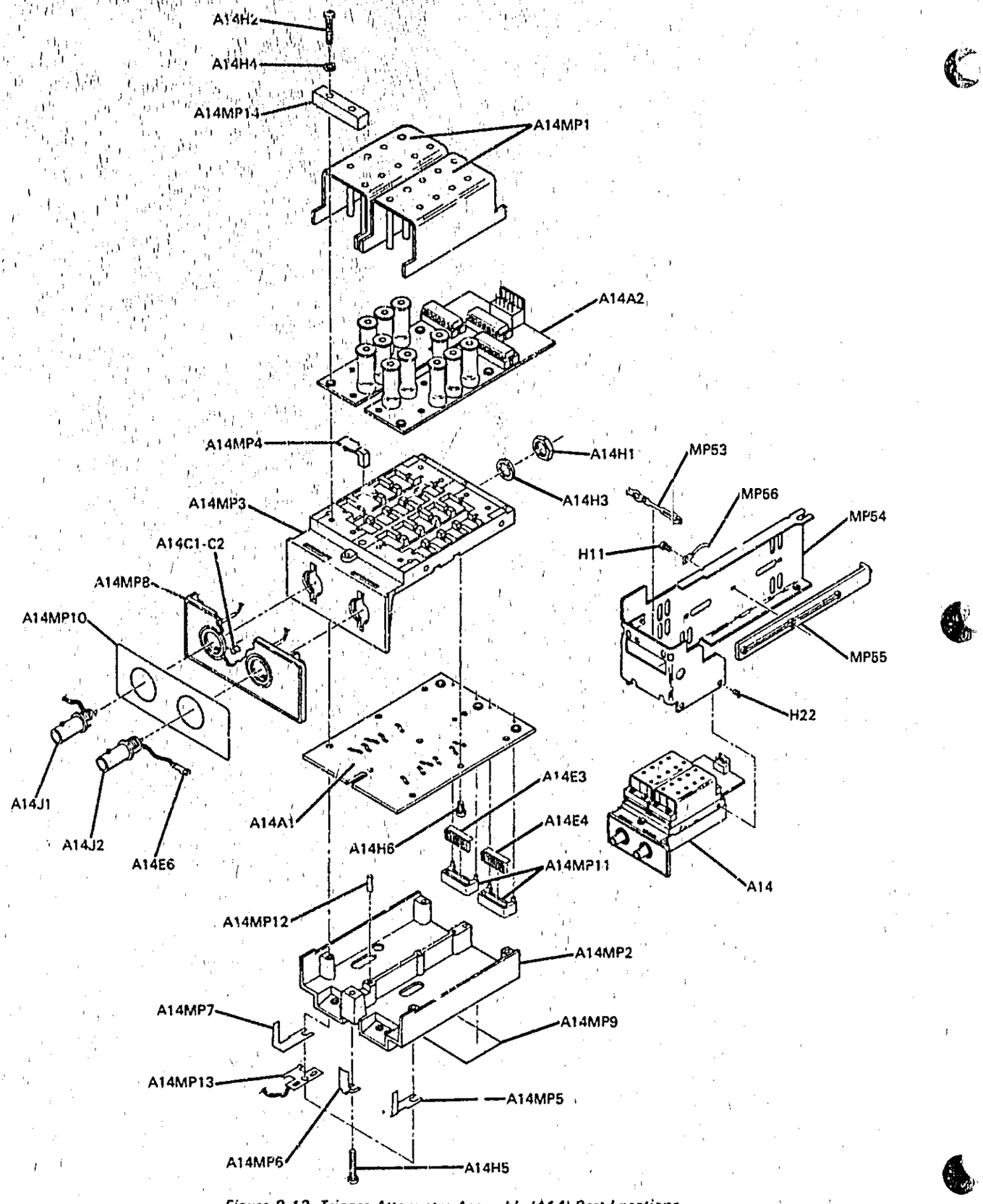
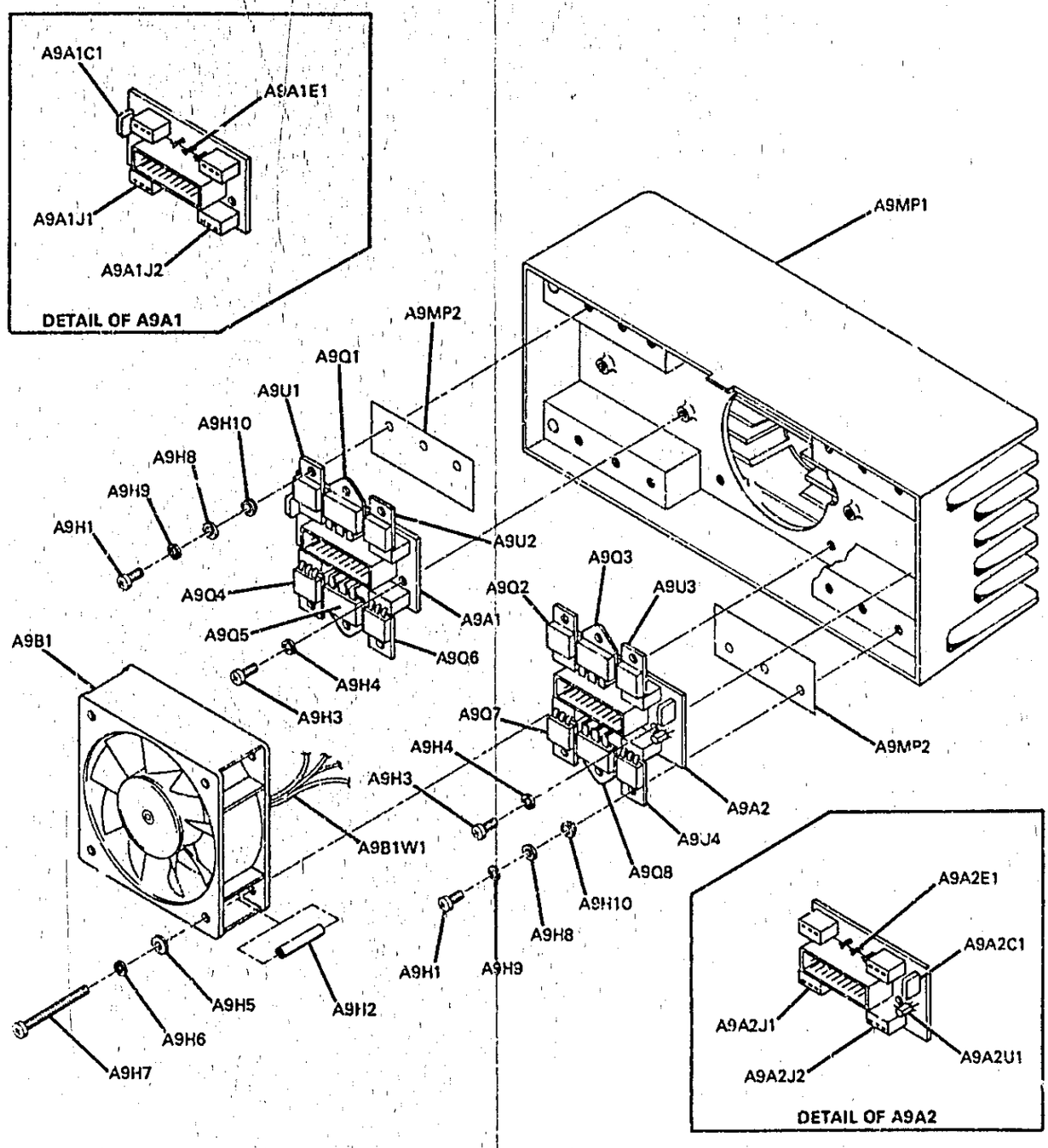
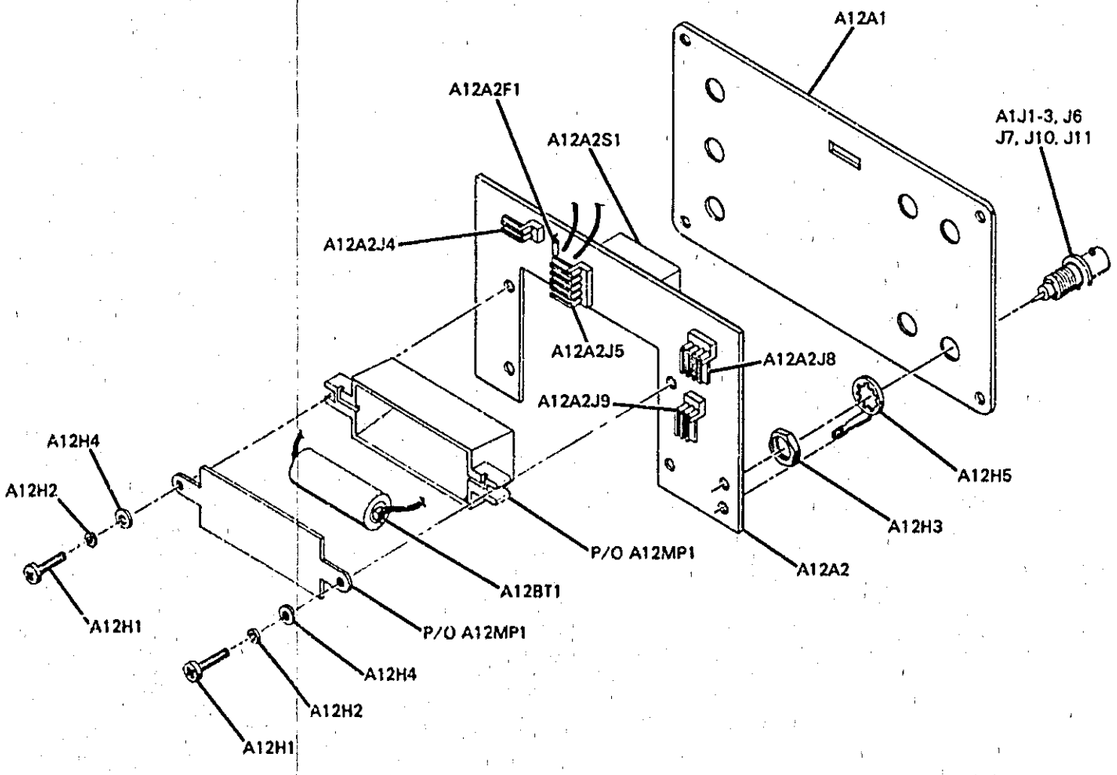


Figure 8-12. Trigger Attenuator Assembly (A14) Part Locations



HEAT SINK

Figure 8-13.
Heat Sink (A9) Part Locations
8-51/(8-52 blank)



BNC PANEL

Figure 8-14.
BNC Panel (A12) Part Locations

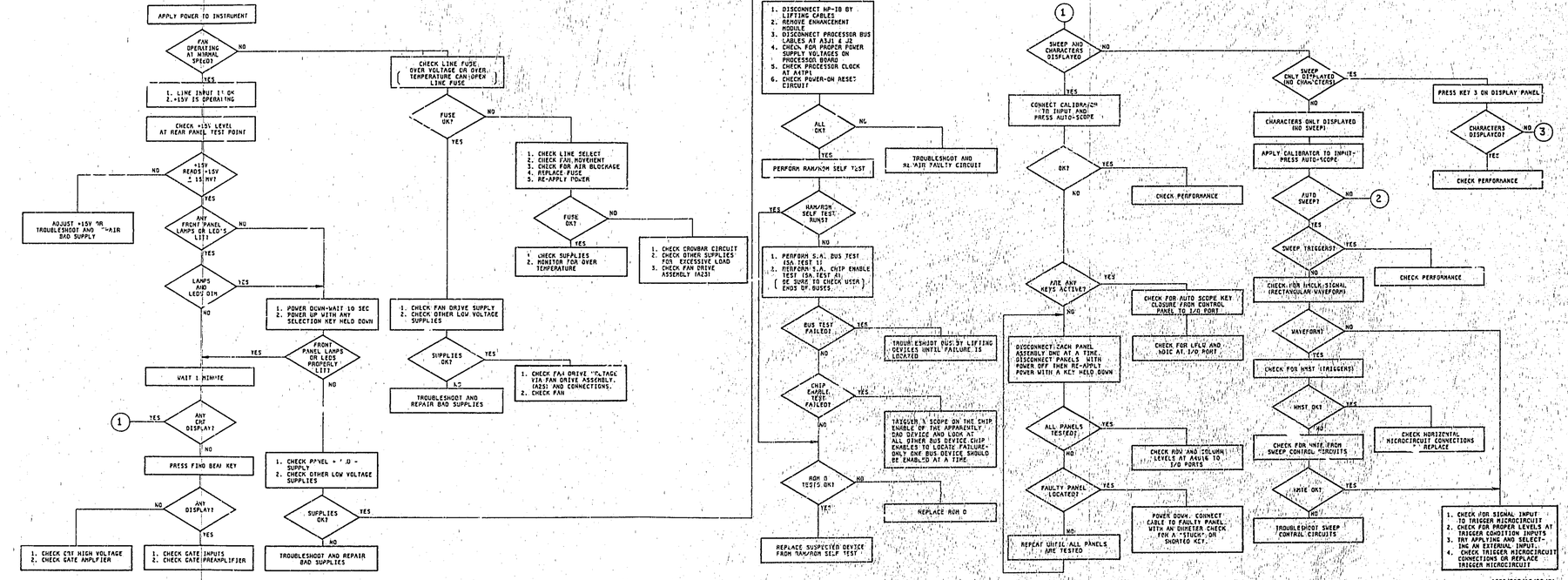
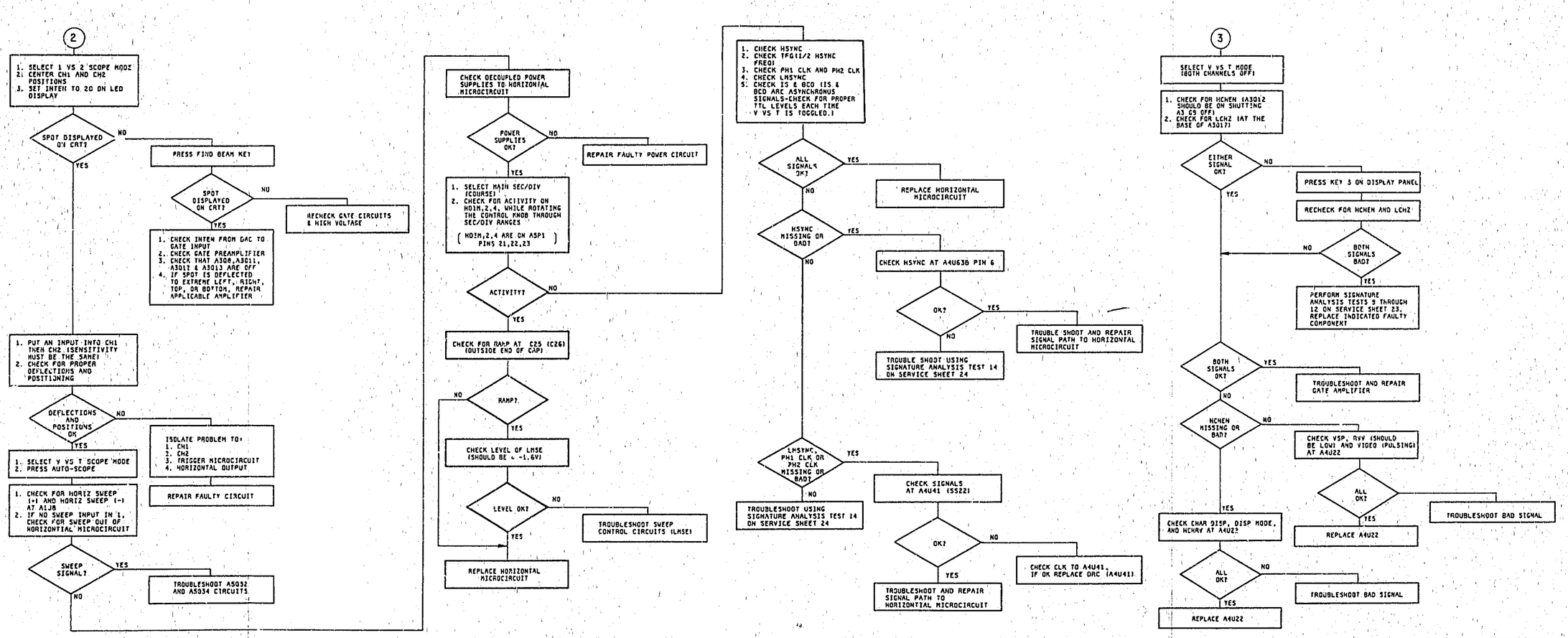


Figure 8-15. Troubleshooting Flow Chart (Sheet 1 of 2)



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Figure 8-15.
Troubleshooting Flow Chart (Sheet 2 of 2)

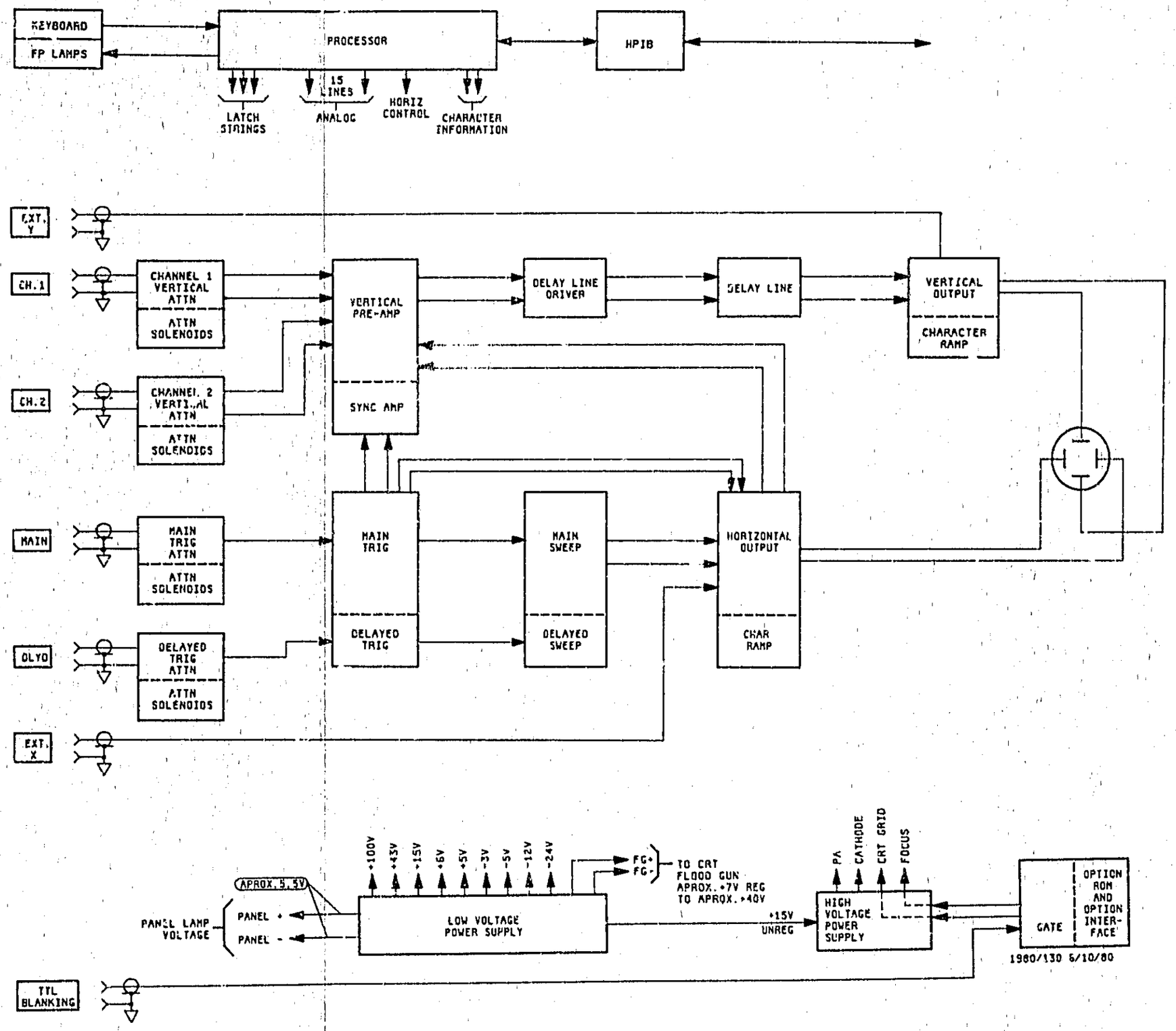


Figure 8-16. 1980 Simplified Block Diagram

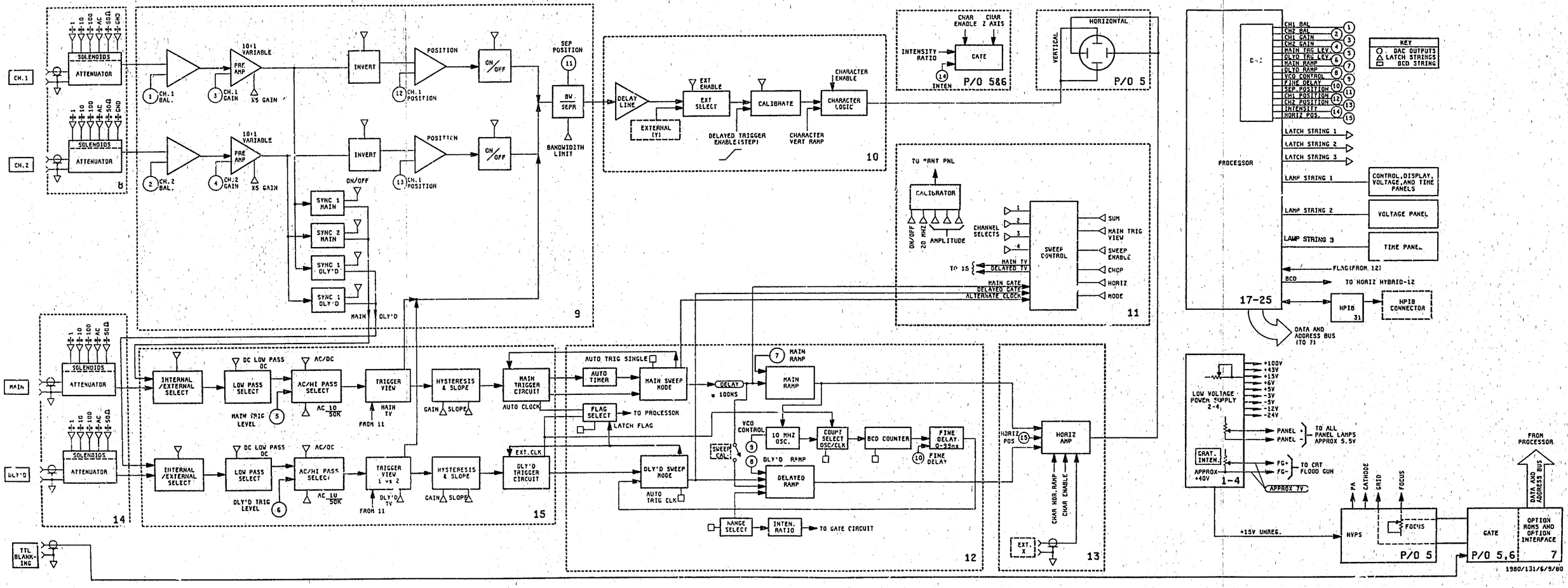
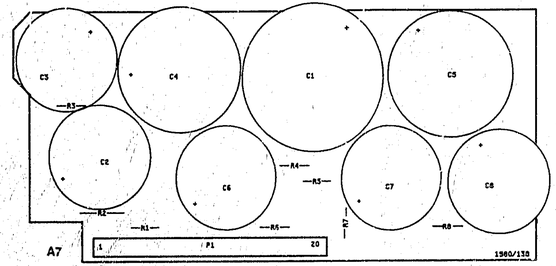
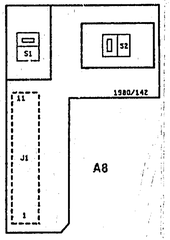


Figure 8-17.
1980 Overall Block Diagram
8-57

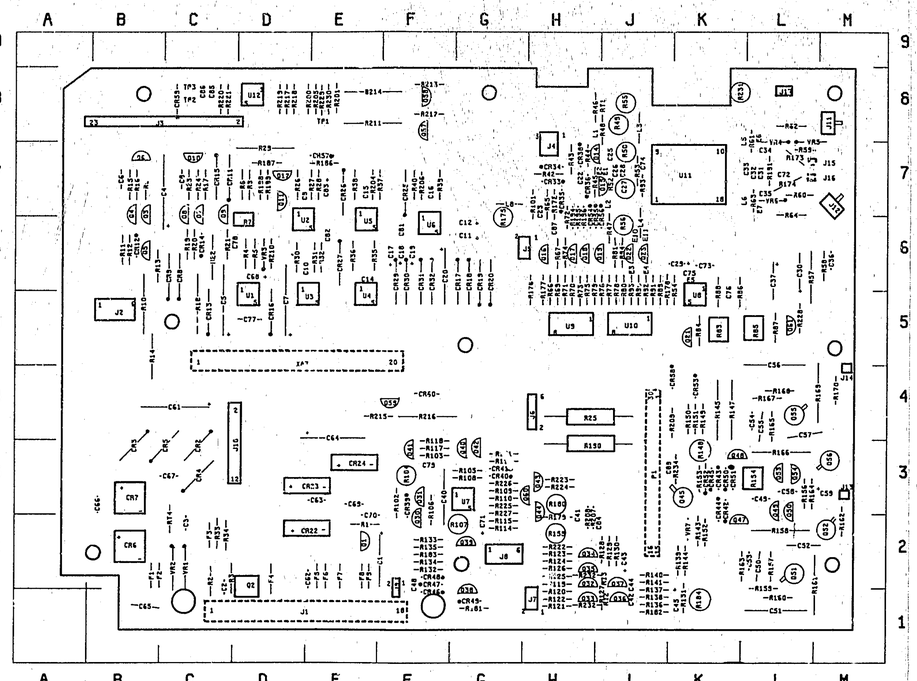




A1 LVPS BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C51	L-1	CR8	C-6	CR55	H-6	L3	J-8	Q47	K-2	R29	D-7	R75	H-5	R128	J-2	R172	H-7	R221	C-8
C2	C-2	C52	L-2	CR9	C-6	CR56	H-6	L4	J-6	Q48	K-3	R30	D-6	R76	H-5	R129	J-2	R173	L-7	R222	H-2
C3	C-3	C53	L-2	CR11	C-7	CR57	E-7	L5	K-7	Q49	L-3	R31	E-6	R77	J-5	R130	J-2	R174	L-7	R223	H-3
C4	B-7	C54	L-4	CR12	B-6	CR58	J-4	L6	K-7	Q50	L-3	R32	E-6	R78	J-5	R131	K-1	R175	G-6	R224	H-3
C5	C-8	C55	L-4	CR13	C-5	CR59	C-8	L8	G-7	Q51	L-2	R33	C-2	R79	H-5	R132	F-2	R176	H-5	R225	G-3
C6	B-7	C56	L-5	CR14	C-6	CR60	F-4	P1	J-3	Q52	M-2	R34	C-2	R80	J-5	R133	F-2	R177	H-5	R226	G-3
C7	D-5	C57	L-4	CR15	C-7	E1	J-7	Q1	E-2	Q53	L-3	R35	E-6	R81	J-6	R134	F-2	R178	J-5	R227	G-3
C8	C-7	C58	L-3	CR16	C-7	E2	J-7	Q2	D-2	Q54	L-3	R36	E-6	R82	K-5	R135	J-1	R179	H-2	R228	L-5
C9	E-7	C59	M-3	CR17	G-6	E3	J-6	Q3	B-7	Q55	L-4	R37	E-7	R84	K-5	R136	J-1	R180	H-3	R229	E-8
C10	D-8	C61	C-4	CR18	G-6	E4	J-6	Q4	B-7	Q56	M-3	R38	E-7	R85	L-5	R137	J-1	R181	C-1	R230	E-8
C11	G-8	C62	D-2	CR19	G-6	E5	K-6	Q5	B-6	Q57	F-8	R39	F-7	R86	K-5	R138	J-1	R182	J-1	R231	K-8
C12	G-8	C63	E-3	CR20	G-6	E6	L-7	Q6	B-7	Q58	F-8	R40	F-7	R87	L-5	R139	K-2	R183	F-2	R232	H-1
C14	E-5	C64	E-4	CR22	D-2	E7	L-7	Q7	C-7	Q59	F-4	R42	H-7	R88	K-5	R140	J-2	R184	K-1	R233	H-2
C15	E-7	C65	B-1	CR23	D-3	E10	J-6	Q8	C-7	Q60	G-3	R43	H-7	R89	J-5	R141	J-2	R185	E-7	R234	K-3
C16	F-7	C66	E-3	CR24	E-3	E11	J-6	Q9	C-7	Q61	L-5	R44	H-7	R90	J-5	R142	K-2	R186	E-7	R71	H-8
C17	F-8	C67	C-3	CR25	F-7	F1	B-2	Q10	C-7	R1	E-2	R45	H-7	R91	J-5	R144	K-2	R187	E-7	R72	J-1
C18	F-8	C68	D-6	CR26	E-7	F2	C-2	Q11	D-7	R2	D-2	R46	H-8	R92	J-5	R145	K-4	R190	L-7	R73	J-2
C19	F-8	C69	E-3	CR27	E-6	F3	C-2	Q12	D-7	R3	D-2	R47	J-6	R93	J-1	R147	K-4	R191	L-7	R74	C-2
C20	F-6	C70	E-2	CR28	F-6	F4	D-2	Q14	H-7	R4	D-6	R48	H-8	R94	J-1	R148	K-3	R194	H-6	TP1	E-8
C22	H-7	C71	G-2	CR30	F-6	F5	E-2	Q15	H-7	R5	D-6	R49	J-8	R101	H-2	R149	K-4	R195	H-6	TP2	C-8
C23	H-7	C72	L-7	CR31	F-6	F6	E-2	Q16	H-6	R6	D-7	R50	J-7	R102	F-3	R150	K-4	R196	H-6	TP3	C-8
C25	J-7	C73	K-6	CR32	F-6	F7	E-2	Q17	H-6	R7	D-6	R52	J-7	R103	F-3	R151	L-4	R198	D-7	U1	D-5
C26	J-7	C74	J-7	CR33	H-7	F8	E-2	Q18	H-6	R8	D-7	R53	J-7	R104	F-3	R152	K-2	R199	D-7	U2	D-6
C27	J-7	C75	K-6	CR34	H-7	F9	E-2	Q19	H-6	R9	B-7	R54	J-6	R106	G-3	R153	K-3	R200	D-8	U3	D-5
C28	J-7	C76	L-5	CR35	H-7	J1	D-1	Q21	K-5	R10	B-6	R55	J-8	R108	F-3	R154	L-3	R201	E-8	U4	E-5
C29	K-6	C77	D-5	CR36	H-7	J2	B-5	Q22	J-6	R11	B-6	R56	J-6	R107	G-2	R155	H-2	R204	E-7	U5	E-6
C30	L-5	C78	C-8	CR38	H-7	J3	B-8	Q23	J-6	R12	B-6	R57	L-6	R109	G-3	R156	H-2	R205	E-7	U6	F-6
C31	L-7	C79	F-3	CR39	F-3	J4	H-7	Q30	F-2	R13	B-6	R58	M-6	R110	G-3	R157	L-2	R206	F-7	U7	G-3
C32	L-7	C81	F-6	CR40	F-3	J5	H-5	Q31	F-3	R14	B-6	R60	L-7	R111	G-2	R158	L-4	R207	H-2	U8	K-5
C33	K-7	C82	E-6	CR41	G-3	J6	G-1	Q32	H-2	R15	B-7	R60	L-7	R114	G-2	R159	L-2	R208	J-4	U9	H-5
C34	L-7	C83	E-7	CR42	K-3	J7	H-1	Q33	H-1	R16	B-7	R61	L-7	R115	G-2	R160	L-1	R209	J-4	U10	J-5
C35	L-7	C84	H-2	CR43	K-3	J8	G-2	Q34	H-2	R17	C-7	R62	L-8	R116	G-3	R161	M-2	R210	D-6	U11	K-7
C36	M-6	C85	C-8	CR44	K-3	J9	F-2	Q35	H-2	R18	C-6	R63	L-7	R117	F-3	R162	M-2	R211	E-8	U12	D-8
C37	K-6	C86	C-6	CR45	K-3	J10	L-3	Q36	J-1	R19	C-6	R64	L-7	R118	F-3	R163	K-2	R212	F-8	V61	C-2
C40	F-3	C87	H-8	CR46	F-1	J11	V-8	Q37	J-2	R20	C-6	R65	H-7	R119	H-2	R164	L-3	R213	F-8	VR2	C-2
C41	H-2	C88	G-7	CR47	F-2	J12	M-7	Q38	G-1	R21	C-6	R66	H-5	R120	H-1	R165	L-4	R214	E-8	VR3	D-6
C42	J-1	C89	J-3	CR48	F-2	J13	M-3	Q39	G-2	R22	C-6	R67	H-5	R121	H-1	R166	L-3	R215	E-7	VR4	L-7
C43	J-2	CR2	C-3	CR49	G-1	J14	M-4	Q40	G-3	R23	C-7	R68	H-5	R122	H-1	R167	L-4	R216	F-4	VR5	L-7
C44	J-2	CR3	B-3	CR50	K-3	J15	M-7	Q41	F-3	R24	C-7	R70	H-5	R123	H-2	R168	L-4	R217	D-8	VR6	L-7
C45	K-1	CR4	C-3	CR51	K-3	J16	M-7	Q42	G-3	R25	H-4	R71	H-5	R124	H-2	R169	L-4	R218	D-8	VR7	K-2
C48	J-2	CR5	B-3	CR52	K-3	J17	L-8	Q43	H-3	R26	D-7	R72	H-6	R125	H-2	R170	M-4	R219	D-8	VR8	K-3
C49	L-3	CR6	B-2	CR53	K-4	L1	H-8	Q44	H-3	R27	D-7	R73	H-5	R126	H-2	R171	G-3	R220	C-8	X47	D-6
C50	L-2	CR7	B-3	CR54	H-6	L2	J-7	Q45	K-3	R28	E-7	R74	H-6	R127	J-1						

A1



Note

Refer to Section VI for location of chassis mounted components and A9 Heat Sink Assembly components.

Service Sheet 1. Component Locator
P/O Low Voltage Power Supply Board, +100 V and +43 V Outputs

SERVICE SHEET 1 — THEORY OF OPERATION

Input Circuit. The low voltage power supply operates from an ac power source. The ac line is applied to the input power circuit where 100/120/220/240 Vac operation is selectable. The input power circuit contains the ac line protection fuse. The ac input is applied to a stepdown power transformer with multiple secondaries.

+100 V Supply Operation. Approximately 103 V rms from T1 pins 1 and 2 is fused by A1F1, rectified by A1CR6 and filtered by A7C2 (located on the Capacitor Board Assembly, A7). A9Q2 (located on the rear panel Heat Sink Assembly, A9) is the series regulator transistor. The current through the regulator transistor is controlled by the circuits of A1Q3, A1Q4, and A1Q6.

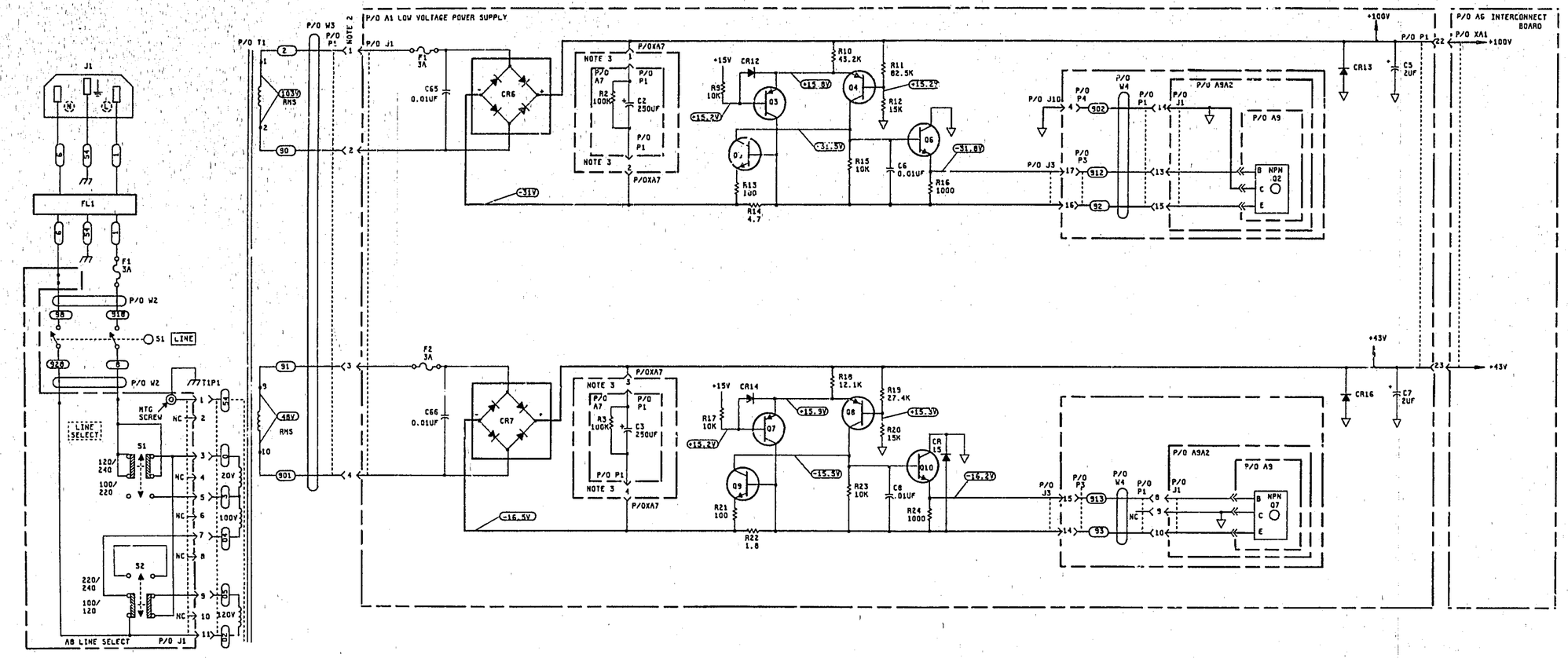
A1Q3 sets a reference potential from the +15 V supply. With a fixed voltage on the emitter of Q4 any change in the +100 V output is felt on the base of A1Q4, and will change the biasing of A1Q6. When the current of A1Q6 is changed the voltage at the base of the regulator transistor, A9Q2, is also changed. The changing current in the regulator transistor, A1Q2, causes the current of the +100 V load and the +100 V output to change.

The transistor, A1Q5, is a current limit device. When an excessive amount of current is drawn by the +100 V circuit a large enough voltage is developed across A1R14 to bias A1Q5 into conduction. When A1Q5 conducts, the decreased base voltage of A1Q6 will cause the conduction of A1Q6 to be greatly decreased and limit the current flow through the series regulator transistor.

+43 V Supply Operation. Approximately 48 V rms from T1 pins 9 and 10 is fused by A1F2, rectified by A1CR7 and filtered by A7C3 (located on the Capacitor Board Assembly, A7). A9Q7 (located on the rear panel Heat Sink Assembly, A9) is the series regulator transistor. The current through the regulator transistor is controlled by the circuits of A1Q7, A1Q8, and A1Q10.

A1Q7 sets a reference potential from the +15 V supply. With a fixed voltage on the emitter of A1Q8 any change in the +43 V output is felt on the base of A1Q8, and will change the biasing of A1Q10. When the current of A1Q10 is changed the voltage at the base of the regulator transistor, A1Q7, is also changed. The changing current in the regulator transistor, A1Q7, causes the current of the +43 V load and the +43 V output to change.

A1Q9 is a current limit device. When an excessive amount of current is drawn by the +43 V circuit a large enough voltage is developed across A1R22 to bias A1Q9 into conduction. When A1Q9 conducts, the decreased base voltage of A1Q10 will cause the conduction of A1Q10 to be greatly decreased and limit the current flow through the series regulator transistor.



NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES

2. CONNECTIONS BETWEEN W3P1 AND A1J1 ARE MADE USING CONNECTOR HOLDER E1.

3. CONNECTIONS BETWEEN XA7 AND A7P1 ARE MADE USING CONNECTOR HOLDER E2.

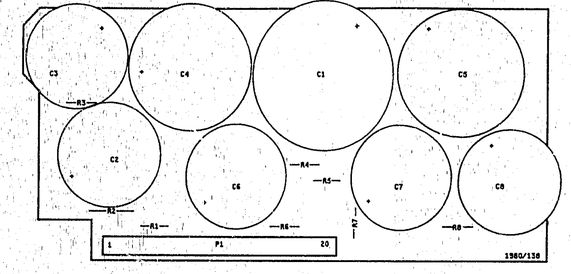
PARTS ON THIS SCHEMATIC

P/O A1	CHASSIS	P/O A6
C5-8,65,66 CR6,7,12-16 F1,2 P/O J1,J3,J10 P/O P1 Q3-10 R9-24 P/O XA7	P/O E1,2 F1 FL1 J1 S1 P/O T1 P/O W2,3,4	P/O XA1
	P/O A9	P/O A7
	P/O A2 P/O A2J1 Q2,Q7	C2-3 P/O P1 R1,2
		P/O A8
		J1 S1,2

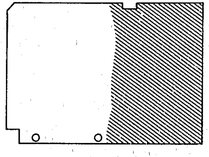
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Service Sheet 1. Schematic Diagram
P/O Low Voltage Power Supply Board, +100 V and +43 V Outputs



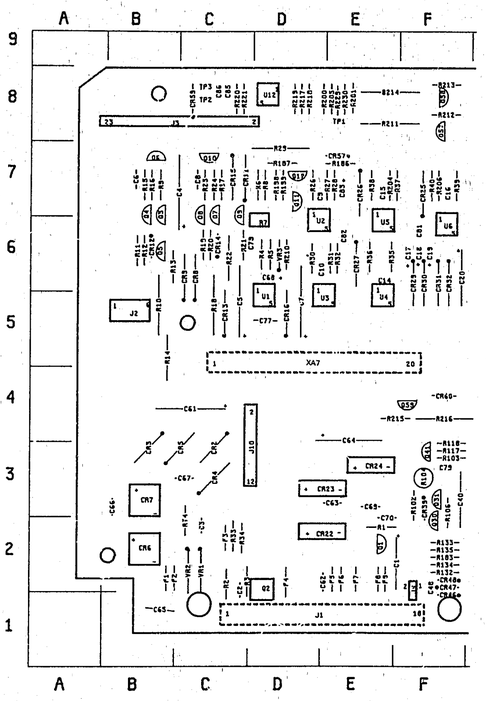
A7



A1 LVPS BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C51	L-1	CR8	C-6	CR55	H-6	L3	J-8	Q47	K-2	R28	D-7	R75	H-5	R128	J-2	R172	H-7	R221	C-8
C2	C-2	C52	L-2	CR9	C-6	CR56	H-6	L4	J-6	Q48	K-3	R30	D-6	R76	H-5	R129	J-2	R173	L-7	R222	H-2
C3	C-3	C53	L-3	CR11	C-7	CR57	E-7	L5	K-7	Q49	L-3	R31	E-6	R77	J-5	R130	J-1	R174	L-7	R223	H-3
C4	B-7	C54	L-4	CR12	B-6	CR58	J-6	L6	K-7	Q50	L-3	R32	E-6	R78	J-5	R131	K-1	R175	G-6	R224	H-3
C5	C-6	C55	L-4	CR13	C-5	CR59	C-8	L8	G-7	Q51	L-2	R33	C-2	R79	H-5	R132	F-2	R176	H-5	R225	G-3
C6	B-7	C56	L-5	CR14	C-6	CR60	F-6	P1	J-3	Q52	M-2	R34	C-2	R80	J-5	R133	F-2	R177	H-5	R226	G-3
C7	D-5	C57	L-4	CR15	C-7	E1	J-7	Q1	E-2	Q53	L-3	R35	E-6	R81	J-6	R134	F-2	R178	J-5	R227	G-3
C8	C-7	C58	L-3	CR16	D-5	E2	J-7	Q2	D-2	Q54	L-3	R36	E-7	R83	K-5	R135	F-2	R179	H-2	R228	L-3
C9	E-7	C59	M-3	CR17	G-6	E3	J-6	Q3	B-7	Q55	L-4	R37	E-7	R84	K-5	R136	J-1	R180	H-3	R229	E-8
C10	D-6	C61	C-4	CR18	G-6	E4	J-6	Q4	B-7	Q56	M-3	R38	F-7	R85	L-5	R137	J-1	R181	G-1	R230	E-8
C11	G-6	C62	D-2	CR19	G-6	E5	K-6	Q5	B-6	Q57	F-8	R39	F-7	R86	K-5	R138	J-1	R182	J-1	R231	K-8
C12	G-6	C63	E-3	CR20	G-6	E6	L-7	Q6	B-7	Q58	F-8	R40	F-7	R87	L-5	R139	K-2	R183	F-2	R232	H-1
C14	E-6	C64	E-4	CR22	D-2	E7	L-7	Q7	C-7	Q59	F-4	R42	H-7	R88	K-5	R140	J-2	R184	K-1	R233	H-2
C15	E-7	C65	B-1	CR23	D-3	E10	J-6	Q8	C-7	Q60	G-3	R43	H-7	R89	J-5	R141	J-2	R186	E-7	R234	K-3
C16	F-7	C66	B-3	CR24	E-3	E11	J-6	Q9	C-7	Q61	L-5	R44	H-7	R90	J-5	R143	K-2	R187	D-7	RT1	H-8
C17	F-6	C67	C-3	CR25	F-7	F1	B-2	Q10	C-7	R1	E-2	R45	H-7	R91	J-5	R144	K-2	R190	H-3	RT2	J-1
C18	F-6	C68	D-5	CR26	E-7	F2	C-2	Q11	D-7	R2	D-2	R46	H-8	R92	J-5	R145	K-4	R191	L-7	RT3	J-2
C19	F-6	C69	E-3	CR27	E-6	F3	C-2	Q12	D-7	R3	D-2	R47	J-6	R93	J-5	R147	K-4	R193	J-7	RT4	C-2
C20	F-6	C70	E-2	CR29	F-6	F4	D-2	Q14	H-7	R4	D-6	R48	H-8	R94	J-6	R148	K-3	R194	H-6	TP1	E-8
C22	H-7	C71	G-2	CR30	F-6	F5	E-2	Q15	H-7	R5	D-6	R49	J-8	R101	H-7	R149	K-4	R195	H-6	TP2	C-8
C23	H-7	C72	L-7	CR31	F-6	F6	E-2	Q16	H-6	R6	D-7	R50	J-7	R102	F-3	R150	K-4	R196	H-6	TP3	C-8
C25	J-7	C73	K-8	CR32	F-6	F7	E-2	Q17	H-6	R7	D-6	R52	J-7	R103	F-3	R151	K-4	R198	D-7	U1	D-5
C26	J-7	C74	J-7	CR33	H-7	F8	E-2	Q18	H-6	R8	D-7	R53	J-7	R104	F-3	R152	K-2	R199	D-7	U2	D-6
C27	J-7	C75	K-6	CR34	H-7	F9	E-2	Q19	H-6	R9	B-7	R54	J-6	R105	G-3	R153	K-3	R200	D-8	U3	D-5
C28	J-7	C76	L-6	CR35	H-7	J1	D-1	Q21	K-5	R10	B-6	R55	J-8	R106	F-3	R154	L-3	R201	E-8	U4	E-5
C29	K-6	C77	D-6	CR36	H-7	J2	B-5	Q22	J-6	R11	B-6	R56	J-6	R107	G-2	R155	H-2	R204	E-7	U5	E-6
C30	L-6	C78	C-5	CR37	H-7	J3	B-8	Q23	J-6	R12	B-6	R57	L-6	R108	G-3	R156	L-3	R206	E-8	U6	F-6
C31	L-7	C79	F-3	CR38	F-3	J4	H-7	C10	F-2	R13	B-6	R58	M-6	R109	G-3	R157	L-2	R206	F-7	U7	G-3
C32	L-7	C81	F-6	CR40	G-3	J5	H-6	Q31	F-3	R14	B-6	R59	L-7	R110	G-3	R158	L-2	R207	H-2	U8	K-5
C33	K-7	C82	E-6	CR41	G-3	J6	G-4	Q32	H-2	R15	B-7	R60	L-7	R114	G-2	R159	L-2	R208	H-2	U9	H-5
C34	L-7	C83	E-7	CR42	K-3	J7	H-1	Q33	H-1	R16	B-7	R61	L-7	R115	G-2	R160	L-1	R209	J-4	U10	J-5
C35	L-7	C84	H-3	CR43	K-3	J8	G-2	Q34	H-2	R17	C-7	R62	L-8	R116	G-3	R161	M-2	R210	D-6	U11	K-7
C36	M-6	C85	C-8	CR44	K-3	J9	F-2	Q35	H-2	R18	C-6	R63	L-7	R117	F-3	R162	M-2	R211	E-8	U12	D-8
C37	K-8	C86	C-8	CR45	K-3	J10	C-3	Q36	J-1	R19	C-6	F-24	L-7	R118	F-3	R163	K-2	R212	F-8	VR1	C-2
C40	F-3	C87	H-5	*R46	F-1	J11	M-8	Q37	J-2	R20	C-6	R65	H-7	R119	H-2	R164	L-3	R213	F-8	VR2	C-2
C41	H-2	C88	G-7	*R47	F-1	J12	M-7	Q38	G-1	R21	C-7	R66	H-5	R120	H-1	R165	L-4	R214	E-8	VR3	D-5
C42	J-1	C89	J-3	*R48	F-2	J13	M-3	Q39	G-2	R22	C-6	R67	H-6	R121	H-1	R166	L-3	R215	E-4	VR4	L-7
C43	J-2	CR2	C-3	CR49	G-1	J14	M-4	Q40	G-3	R23	C-7	R69	H-5	R122	H-1	R167	L-4	R216	F-4	VR5	L-7
C44	J-2	CR3	B-3	CR50	K-3	J15	M-7	Q41	F-3	R24	C-7	R70	H-5	R123	H-2	R168	L-4	R217	D-8	VR6	L-7
C45	K-1	CR4	C-3	CR51	K-3	J16	M-7	Q42	G-3	R25	H-4	R71	H-5	R124	H-2	R169	L-4	R218	D-8	VR7	K-2
C48	F-2	CR5	B-3	CR52	K-3	J17	L-8	Q43	H-3	R26	D-7	R72	H-6	R125	H-2	R170	M-4	R219	D-8	VR8	K-3
C49	L-3	CR6	B-2	CR53	K-4	L1	L-8	Q44	H-3	R27	D-7	R73	H-6	R126	H-2	R171	G-3	R220	C-8	XA7	D-6
C50	L-2	CR7	B-3	CR54	H-6	L2	J-7	Q45	K-3	R28	E-7	R74	H-6	R127	J-1						

A1



Note

Refer to Section VI for location of chassis mounted components and A9 Heat Sink Assembly components.

Service Sheet 2. Component Locator
P/O Low Voltage Power Supply Board, +15 V Output and Fan Control

SERVICE SHEET 2 — THEORY OF OPERATION

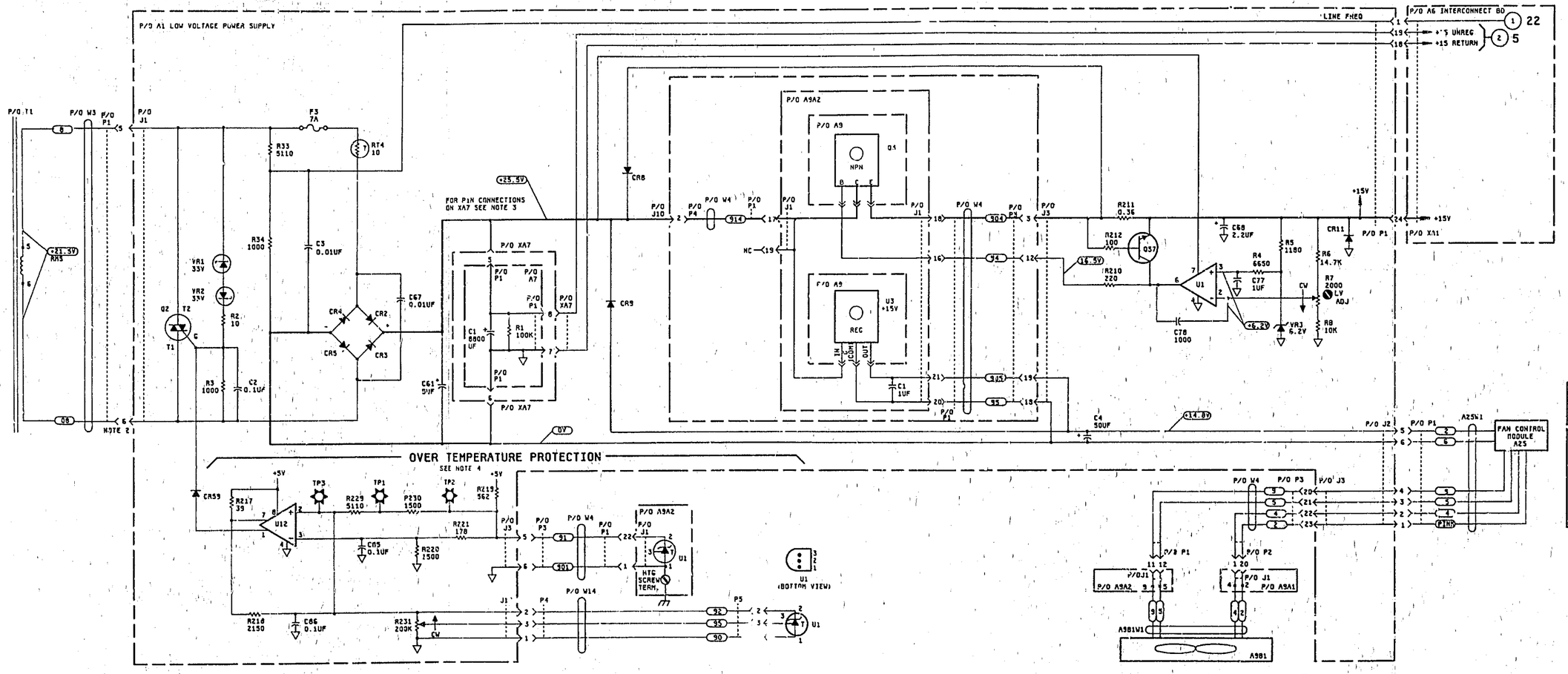
+15 V Unregulated. Approximately +21.5 V rms on T1 pins 5 and 6 is across the Triac, A1Q2, and two voltage regulators VR1 and VR2. The secondary voltage is fused by A1F3, rectified by A1CR2 through A1CR5, then filtered by A7C1 (on the Capacitor Board Assembly, A7). The unregulated +15 V is picked off across A7C1 (XA7 pins 7 and 8) for use in the High Voltage Power Supply Assembly.

+15 V Regulated Power Supply. The voltage across A7C1 is regulated by the series regulator A9Q3 (on the rear panel Heat Sink Assembly, A9) to become the regulated +15 V output. The current through A9Q3 is controlled by the Operational Amplifier, A1U1. The Op Amp, A1U1, has a fixed reference voltage applied to its positive input on pin 3. The fixed reference voltage is set by the zener diode, VR3, which maintians the positive input of the Op Amp at +6.2 V. The negative input to the Op Amp is adjustable by A1R7, The Low Voltage Adjust, A1R7, should be adjusted for +15 V measured at the '+15 V REF' output on the rear panel. The transistor, A1Q57, is a current limit device. When an excessive amount of current is drawn by the +15 V circuit a large enough voltage is developed across A1R211 to bias A1Q57 into conduction. When A1Q57 conducts, the decreased base voltage of A9Q3 will cause the conduction of A9Q3 to be greatly decreased and limit the current flow through the +15 V circuit.

Fan Control Module Supply. Another regulated +15 V is available for use of the Fan Control Module, A25. The unregulated voltage across A7C1 is connected to the input and common terminals of the +15 V Regulator I.C. The +15 V Regulator I.C. produces an output of approximately +14.8 V to the Fan Control Module.

Over Voltage Protection. If the input voltage is excessive, from an extreamly high line or the line select switchs are not properly set, the line fuse F1 will be opened by the input circuit in the +15 V supply. If the voltage across T1 pins 5 and 6 exceeds approximately 33 V p-p one of the voltage regulators A1VR1 or A1VR2 will breakdown causing current to flow through the other voltage regulator and A1R3. The voltage drop across A1R3 will be sufficient to gate the triac into conduction. The triac A1Q2 can be gated on with either a positive or negative voltage on the gate. With the triac conducting, the current flow in the secondary winding will cause enough primary current flow to oper. F1.

Over Temperature Protection Circuit. The Over Temperature Protection circuit is to open the Line Fuse, F1, if the temperature of the rear panel Heat Sink Assembly, A9, exceeds the ambient temperature inside the instrument near the Control Panel Assembly. A temperature sensing device, U1, is mounted near the Control Panel Assembly at the front and inside the 1980. This device is adjusted by A1R231 for a specific operating temperature. Another temperature sensing device, A9A2U1, is mounted on the Heat Sink Assembly. If the temperature of the Heat Sink Assembly riser faster than the temperature of U1 a voltage unbalance will occur on the inputs of the voltage comparator A1U12. The output of the voltage comparator, A1U12 pin 1, will go positive gating the triac, A1Q2 on. With the triac conducting the current flow in the secondary winding, T1 pins 5 and 6, will cause enough primary current to open F1.



NOTES:

1. UNLESS OTHERWISE NOTED: RESISTANCE IS IN OHMS CAPACITANCE IS IN PICOFARADS INDUCTANCE IS IN MICRO-HENRIES
2. CONNECTS BETWEEN W3P1 AND A1J1 ARE MADE USING CONNECTOR HOLDER E1
3. CONNECTIONS BETWEEN XA7 AND A7P1 ARE MADE USING CONNECTOR HOLDER E2
4. THE OVER TEMPERATURE PROTECTION CIRCUIT WILL BLOW F1(INPUT FUSE) IF THE HEAT SINK GETS TOO WARM. OPERATION OF THE FAN SHOULD BE CHECKED AFTER FUSE IS REPLACED.

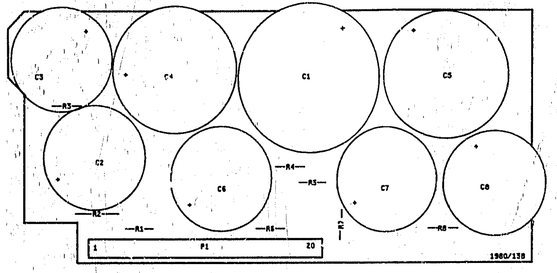
PARTS ON THIS SCHEMATIC

P/O A1	CHASSIS	P/O A9
C2-4,61,67,68, 77,78,85,86 CR2-3,8,9,11,59 F3 J17 P/O J1,2,3,10 P/O P1 Q2,37 R2,33,34 R210-212,217-221, 229-231 RT4 TP1-3 U1,12,13 VR1-3 XA7	A25 P/O T1 P/O W3,4 P/O W14 U1	P/O A1,2 A2U1 B1 Q3 U3
	P/O A6	
	P/O XA1	
	P/O A7	
	C1,R3 P/O P1	

1980/202/7/16/81

2

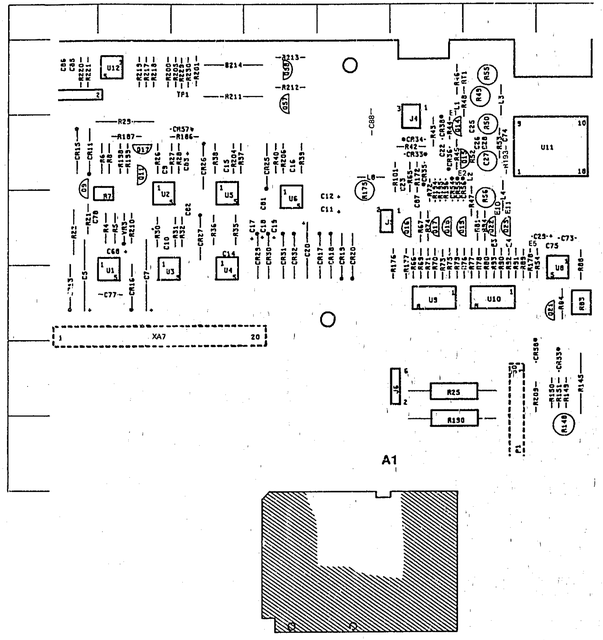
Service Sheet 2. Schematic Diagram
P/O Low Voltage Power Supply Board, +15 V Output and Fan Control



A7

A1 LVPS BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C51	L-1	CR8	C-6	CR65	H-6	L3	J-3	Q47	K-2	R29	D-7	R76	H-5	R128	J-2	R172	H-7	R221	C-8
C2	C-2	C52	L-2	CR9	C-6	CR66	H-6	L4	J-1	Q48	K-3	R30	D-6	R78	H-5	R129	J-2	R173	L-7	R222	H-2
C3	C-3	C53	L-2	CR11	C-7	CR67	E-7	L5	K-7	Q49	L-3	R31	E-6	R79	J-5	R130	J-2	R174	L-7	R223	H-3
C4	B-7	C54	L-4	CR12	B-6	CR68	J-4	L6	K-7	Q50	L-3	R32	E-6	R80	J-5	R131	K-1	R175	G-6	R224	H-3
C5	C-5	C55	L-4	CR13	C-5	CR69	C-8	L8	G-7	Q51	L-2	R33	C-2	R79	H-5	R132	F-2	R176	H-5	R225	G-3
C6	B-7	C56	L-4	CR14	C-6	CR70	F-4	P1	J-3	Q52	M-2	R34	C-2	R80	J-5	R133	F-2	R177	H-5	R226	G-3
C7	D-5	C57	L-4	CR15	C-7	E1	J-7	Q1	E-2	Q53	L-3	R35	E-6	R81	J-6	R134	F-2	R178	J-5	R227	G-3
C8	C-7	C58	L-3	CR16	D-5	E2	J-7	Q2	D-2	Q54	L-3	R36	E-6	R83	K-5	R135	F-2	R179	H-2	R228	L-5
C9	E-7	C59	M-3	CR17	G-6	E3	J-6	Q3	B-7	Q55	L-4	R37	E-7	R84	K-5	R136	J-1	R180	H-3	R229	E-8
C10	E-7	C61	C-4	CR18	G-6	E4	J-6	Q4	B-7	Q56	M-3	R38	E-7	R85	L-5	R137	J-1	R181	G-1	R230	E-8
C11	G-6	C62	D-2	CR19	G-6	E5	K-6	Q5	B-6	Q57	F-8	R39	F-7	R86	K-5	R138	J-1	R182	J-1	R231	K-8
C12	G-6	C63	E-3	CR20	G-6	E6	L-7	Q6	B-7	Q58	F-8	R40	F-7	R87	L-5	R139	K-2	R183	F-2	R232	H-1
C14	E-6	C64	E-4	CR22	D-2	E7	J-7	Q7	C-7	Q59	F-4	R42	H-7	R88	K-5	R140	J-2	R184	K-1	R233	H-2
C15	E-7	C65	B-1	CR23	D-3	E10	J-6	Q8	C-7	Q60	G-3	R43	H-7	R89	J-5	R141	J-2	R185	E-7	R234	K-3
C16	F-7	C66	B-3	CR24	E-3	E11	J-6	Q9	C-7	Q61	L-5	R44	H-7	R90	J-5	R143	K-2	R187	D-7	RT1	H-8
C17	F-6	C67	C-3	CR25	F-7	F1	D-2	Q10	C-7	R1	E-2	R45	H-7	R91	J-5	R144	K-2	R190	H-3	RT2	J-1
C18	F-6	C68	D-6	CR26	E-7	F2	C-2	Q11	D-7	R2	D-2	R46	H-8	R92	J-5	R145	K-4	R191	L-7	RT3	J-2
C19	F-6	C69	E-3	CR27	E-6	F3	C-2	Q12	D-7	R3	D-2	R47	J-6	R93	J-5	R147	K-4	R193	J-7	RT4	C-2
C20	F-6	C70	E-2	CR29	F-6	F4	D-2	Q14	H-7	R4	D-6	R48	H-8	R94	J-6	R148	K-3	R194	H-6	TP1	E-8
C22	H-7	C71	G-2	CR30	J-6	F5	E-2	Q15	H-7	R5	D-6	R49	J-8	R101	H-7	R149	K-4	R195	H-6	TP2	C-8
C23	H-7	C72	L-7	CR31	F-6	F6	E-2	Q16	H-6	R6	D-7	R50	J-7	R102	F-3	R150	K-4	R196	H-6	TP3	C-8
C25	J-7	C73	K-6	CR32	F-6	F7	E-2	Q17	H-6	R7	D-6	R52	J-7	R103	F-3	R151	K-4	R198	D-7	U1	D-5
C26	J-7	C74	J-7	CR33	H-7	F8	E-2	Q18	H-6	R8	D-7	R53	J-7	R104	F-3	R152	K-2	R199	D-7	U2	D-6
C27	J-7	C75	K-6	CR34	H-7	F9	E-2	Q19	H-6	R9	B-7	R54	J-5	R105	G-3	R153	K-3	R200	D-8	U3	D-5
C28	J-6	C76	L-5	CR35	H-7	J1	D-7	Q21	K-6	R10	B-6	R55	J-8	R106	F-3	R154	L-3	R201	E-8	U4	E-5
C29	K-6	C77	D-5	CR36	H-7	J2	B-6	Q22	J-6	R11	B-8	R56	J-6	R107	G-2	R155	H-2	R204	E-7	U5	E-6
C30	L-6	C78	C-5	CR38	H-7	J3	B-8	Q23	J-6	R12	B-6	R57	L-6	R108	G-3	R156	L-3	R205	E-8	U6	F-6
C31	L-7	C79	F-3	CR39	F-3	J4	H-7	Q30	F-2	R13	B-6	R58	M-6	R109	G-3	R157	L-2	R206	F-7	U7	G-3
C32	L-7	C81	F-6	CR40	G-3	J5	H-6	Q31	F-3	R14	B-5	R59	L-7	R110	G-3	R158	L-2	R207	H-2	U8	K-5
C33	K-7	C82	E-6	CR41	C-3	J6	G-4	Q32	H-2	R15	B-7	R60	L-7	R114	G-2	R159	L-2	R208	L-3	U9	H-5
C34	L-7	C83	E-7	CR42	K-3	J7	H-1	Q33	H-1	R16	B-7	R61	L-7	R115	G-2	R160	L-1	R209	J-4	U10	J-5
C35	L-7	C84	H-2	CR43	K-3	J8	G-2	Q34	H-7	R17	C-7	R62	L-8	R116	G-3	R161	M-2	R210	D-8	U11	K-7
C36	M-6	C85	C-8	CR44	K-3	J9	F-2	Q35	H-7	R18	C-5	R63	L-7	R117	F-3	R162	M-2	R211	E-8	U12	D-8
C37	K-5	C86	C-8	CR45	K-3	J10	C-3	Q36	J-1	R19	C-6	R64	L-7	R118	F-3	R163	K-2	R212	F-8	VR1	C-2
C40	F-3	C87	H-6	CR46	F-1	J11	M-8	Q37	J-2	R20	C-6	R65	H-7	R119	H-2	R164	L-3	R213	F-8	VR2	C-2
C41	H-2	C88	G-7	CR47	F-2	J12	M-7	Q38	G-1	R21	C-6	R66	H-5	R120	H-1	R165	L-4	R214	E-8	VR3	D-6
C42	J-1	C89	J-3	CR48	F-2	J13	M-3	Q39	G-2	R22	C-6	R67	H-6	R121	H-1	R166	L-3	R215	E-4	VR4	L-7
C43	J-2	CR2	C-3	CR49	G-1	J14	M-4	Q40	G-3	R23	C-7	R69	H-5	R122	H-1	R167	L-4	R216	F-4	VR5	L-7
C44	J-2	CR3	B-3	CR50	K-3	J15	M-7	Q41	F-3	R24	C-7	R70	H-5	R123	H-2	R160	L-4	R217	D-8	VR6	L-7
C45	K-1	CR4	C-3	CR51	K-3	J16	M-7	Q42	G-3	R25	H-4	R71	H-5	R124	H-2	R169	L-4	R218	D-8	VR7	K-2
C46	F-2	CR5	B-3	CR52	K-3	J17	L-8	Q43	H-3	R26	D-7	R72	H-6	R125	H-2	R170	M-4	R219	D-8	VR8	K-3
C48	L-3	CR6	B-2	CR53	K-4	L1	H-8	Q44	H-3	R27	D-7	R73	H-6	R126	H-2	R171	G-3	R220	C-8	XA7	D-5
C50	L-2	CR7	B-3	CR54	H-6	L2	J-7	Q45	K-3	R28	E-7	R74	H-6	R127	J-1						



Note

Refer to Section VI for location of chassis mounted components and A9 Heat Sink Assembly components.

Service Sheet 3. Component Locator
P/O Low Voltage Power Supply Board, +6 V, +5 V, -5 V, and -5 V Outputs

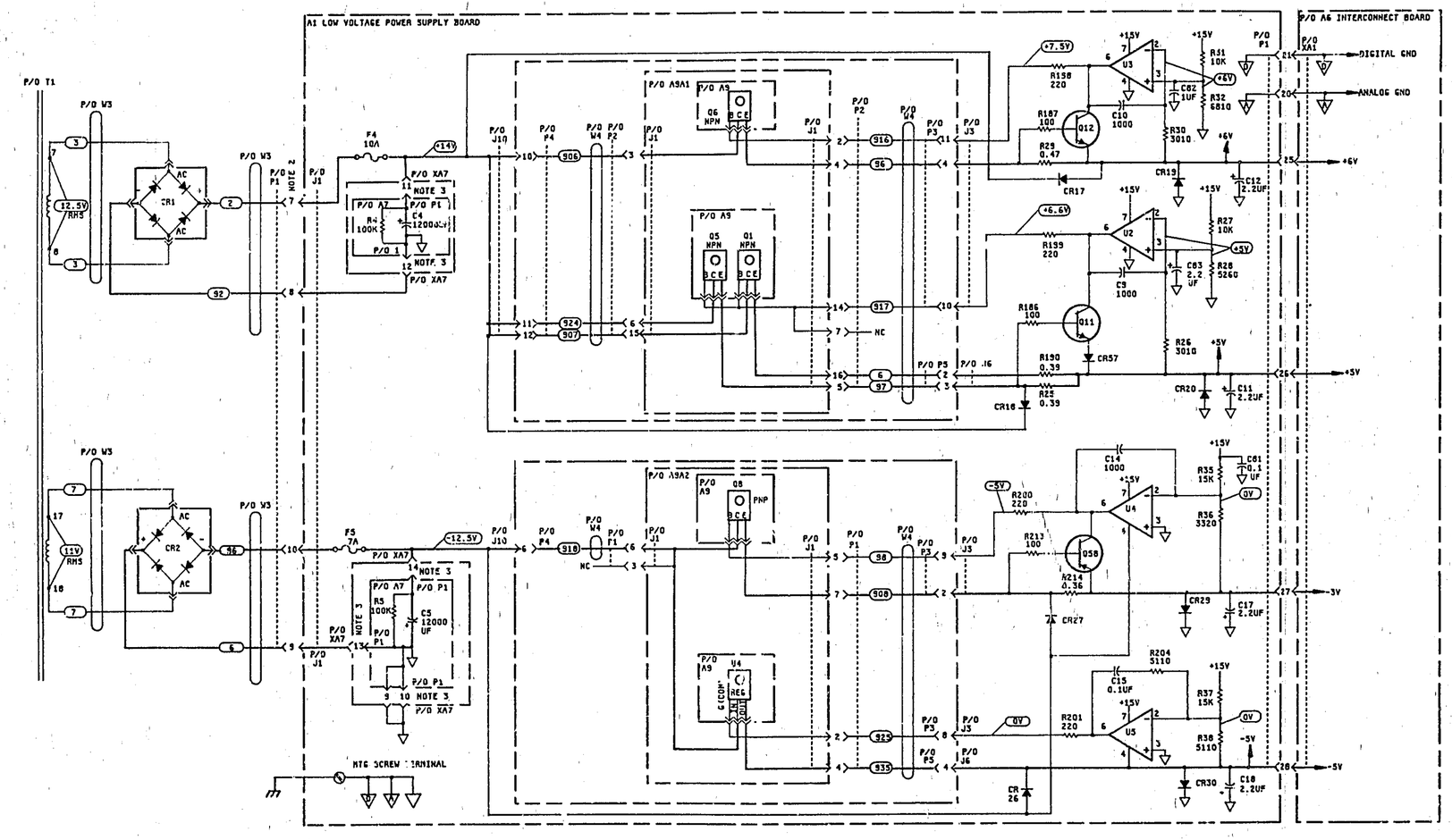
SERVICE SHEET 3 — THEORY OF OPERATION

+6 V Regulator. Approximately 12.5 V rms on T1 pins 7 and 8 is rectified by CR1 (mounted on the 1980 chassis), fused by A1F4, and filtered by A7C4. A9Q6 is a series regulator which is controlled by Op Amp A1U3. A reference for the positive input of the Op Amp is developed from the +15 V. The negative input side is tied to the regulated +6 V output. If the +6 V output changes the voltage at A1U3 pin 6 will change controlling the current flow through A9Q6. A1Q12 is the current limit transistor.

+5 V Regulator. The same input circuit is used for the +5 V regulator as for the +6 V regulator. The voltage for the series regulators A9Q1 and A9Q5 is picked off across A7C4. The series regulators are controlled by Op Amp A1U2. A reference input for the positive input of the Op Amp is developed from the +15 V. The negative input side is tied to the regulated +5 V output. If the +5 V output changes the voltage at A1U2 pin 6 will change controlling the current flow through A9Q1 and A9Q5. A1Q11 is the current limit transistor.

-3 V Regulator. Approximately 11 V rms on T1 pins 17 and 18 is rectified by CR2 (mounted on the 1980 chassis), fused by A1F5, and filtered by A7C5. A9Q8 is a series regulator which is controlled by Op Amp A1U4. A reference input for the negative input of the Op Amp is developed from the +15 V and the -3 V output. The positive input side is tied to ground. Any change in the -3 V output will cause a change in the voltage at A1U4 pin 2 which will result in a change of voltage at A1U4 pin 6 controlling the current flow through A9Q8. A1Q58 is the current limit transistor.

-5 V Regulator. The same input circuit is used for the -5 V regulator as for the -3 V regulator. The voltage for the series regulator A9U4 is picked off across A7C5. The series regulator is controlled by Op Amp A1U5. A reference for the negative input of the Op Amp is developed from the +15 V and the -5 V output. The positive input side is tied to ground. If the -5 V output changes the voltage at A1U5 pin 2 will change which changes the reference for the voltage regulator A9U4. When the potential at the common input of the regulator changes, the regulator changes the -5 V output in an attempt to maintain -5 V from the common input. The regulator I.C. has an internal current limit circuit.



NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES

2. CONNECTIONS BETWEEN W3P1 AND A1J1 ARE MADE USING CONNECTOR HOLDER E1.

3. CONNECTIONS BETWEEN XA7 AND A7P1 ARE MADE USING CONNECTOR HOLDER E2

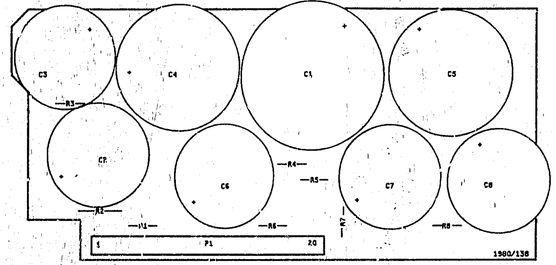
PARTS ON THIS SCHEMATIC

CHASSIS	P/O A1	P/O A6
CR1,2 P/O T1 P/O W3,W4 P/O E1,2	C9-12,14,15,17,18,81-83 CR17-20,26,27,29,30,57 F4,5 Q11,12,58 R25-32,35-38,146,187 190,198-201,204,213,214 U2-5 P/O J1,J3,J6,J10 P/O P1 P/O XA7	P/O XA1
P/O A9		P/O A7
A1,2 Q1,5,6,8 U4		C4,5 R4,5 P/O P1

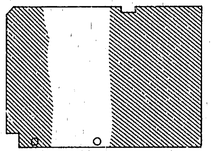
DELETED: R188,189,203 CR28 1360/204/4/23/81

3

Service Sheet 3. Schematic Diagram
P/O Low Voltage Power Supply Board, +6 V, +5 V, -3 V, and -5 V Outputs

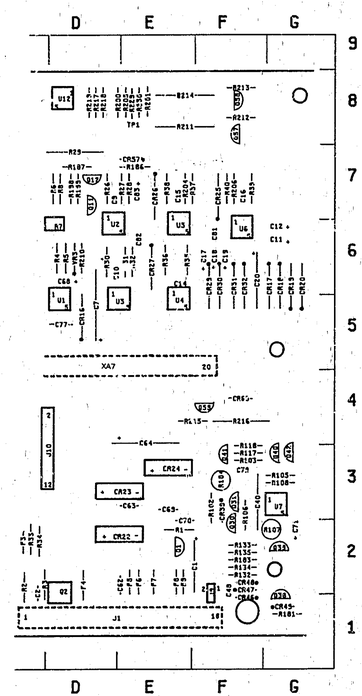


A7



A1 LVPS BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	CR1	L-1	CR8	C-6	CR55	H-6	L3	J-8	Q47	K-2	R29	D-7	R75	H-5	R128	J-2	R172	H-7	R221	C-8
C2	C-2	CR2	L-2	CR9	C-6	CR56	H-6	L4	J-6	Q49	K-3	R30	D-6	R76	H-5	R129	J-2	R173	L-7	R222	H-2
C3	C-3	CR3	L-2	CR11	C-7	CR57	E-7	L5	K-7	Q50	L-3	R31	E-6	R77	J-5	R130	J-2	R174	L-7	R223	H-3
C4	B-7	CR4	L-4	CR12	B-6	CR58	J-4	L6	K-7	Q50	L-3	R32	E-6	R78	J-5	R131	K-1	R175	G-6	R224	H-3
C5	C-5	CR5	L-4	CR13	C-5	CR59	C-8	L8	G-7	Q51	L-3	R33	C-2	R79	H-5	R132	F-2	R176	H-5	R225	G-3
C6	B-7	CR6	L-5	CR14	C-6	CR60	F-4	P1	J-3	Q52	M-2	R34	C-2	R80	J-5	R133	F-2	R177	H-5	R226	G-2
C7	D-5	CR7	L-4	CR15	C-7	E1	J-7	Q1	C-2	Q53	L-3	R35	E-6	R81	J-5	R134	F-2	R178	J-5	R227	G-3
C8	C-7	CR8	L-3	CR16	D-5	E2	J-7	Q2	D-2	Q54	L-3	R36	E-6	R83	K-5	R135	F-2	R179	H-2	R228	L-5
C9	E-7	CR9	M-3	CR17	G-6	E3	J-6	Q3	B-7	Q55	L-4	R37	E-7	R84	K-5	R136	J-1	R180	H-3	R229	E-8
C10	D-6	CR1	C-4	CR18	G-6	E4	J-6	Q4	B-7	Q56	M-3	R38	E-7	R85	L-5	R137	J-1	R181	G-1	R230	E-8
C11	G-6	CR2	D-2	CR19	G-6	E5	K-6	Q5	B-6	Q57	F-8	R39	F-7	R86	K-5	R138	J-1	R182	J-1	R231	K-8
C12	G-6	CR3	E-3	CR20	G-6	E6	L-7	Q6	B-7	Q58	F-8	R40	F-7	R87	L-5	R139	K-2	R183	F-2	R232	H-1
C14	E-6	CR4	E-4	CR22	G-7	E7	L-7	Q7	C-7	Q59	F-4	R42	H-7	R88	K-5	R140	J-2	R184	K-1	R233	H-2
C15	E-7	CR5	B-1	CR23	D-3	E10	J-6	Q8	C-7	Q60	G-3	R43	H-7	R89	J-5	R141	J-2	R185	E-7	R234	K-3
C16	F-7	CR6	B-3	CR24	E-3	E11	J-6	Q9	C-7	Q61	L-5	R44	H-7	R90	J-5	R143	K-2	R187	D-7	RT1	H-8
C17	F-6	CR7	C-3	CR25	F-7	F1	B-2	Q10	C-7	R1	E-2	R45	H-7	R91	J-5	R144	K-2	R190	H-3	RT2	J-1
C18	F-6	CR8	D-6	CR26	E-7	F2	C-2	Q11	D-7	R2	D-2	R46	H-8	R92	J-5	R145	K-4	R191	L-7	RT3	J-2
C19	F-6	CR9	E-3	CR27	E-6	F3	C-2	Q12	D-7	R3	D-2	R47	J-6	R93	J-5	R147	K-4	R193	J-7	RT4	C-2
C20	F-6	CR10	E-2	CR29	F-6	F4	D-2	Q14	H-7	R4	E-6	R48	H-8	R94	J-6	R148	K-3	R194	H-6	TP1	E-8
C22	H-7	CR11	G-2	CR30	F-6	F5	E-2	Q15	H-7	R5	D-5	R49	J-8	R101	H-7	R149	K-4	R195	H-6	TP2	C-8
C23	H-7	CR12	L-7	CR31	F-6	F6	E-2	Q16	H-6	R6	D-7	R50	J-7	R102	F-3	R150	K-4	R196	H-6	TP3	C-8
C25	J-7	CR13	K-6	CR32	F-6	F7	E-2	Q17	H-6	R7	D-5	R52	J-7	R103	F-3	R151	K-4	R198	D-7	U1	D-5
C26	J-7	CR14	J-7	CR33	H-7	F8	E-2	Q18	H-6	R8	D-7	R53	J-7	R104	F-3	R152	K-2	R199	D-7	U2	D-6
C27	J-7	CR15	K-6	CR34	H-7	F9	E-2	Q19	H-6	R9	B-7	R54	J-5	R105	G-3	R153	K-3	R200	D-8	U3	D-5
C28	J-7	CR16	L-5	CR35	H-7	J1	D-1	Q21	K-5	R10	B-5	R55	J-8	R106	F-3	R154	L-3	R201	E-8	U4	E-5
C29	C-6	CR17	D-5	CR36	H-7	J2	B-5	Q22	J-6	R11	B-6	R56	J-6	R107	G-2	R155	H-2	R204	E-7	U5	E-6
C30	L-6	CR18	C-6	CR38	H-7	J3	B-8	Q23	J-6	R12	B-6	R57	L-6	R108	G-3	R156	L-3	R205	E-8	U6	F-6
C31	L-7	CR19	F-3	CR39	F-3	J4	H-7	Q30	F-2	R13	B-6	R58	M-6	R109	G-3	R157	L-2	R206	F-7	U7	G-3
C32	L-7	CR21	F-6	CR40	K-3	J5	H-6	Q31	F-2	R14	B-5	R59	L-7	R110	G-3	R158	L-2	R207	H-2	U8	K-5
C33	K-7	CR22	E-6	CR41	G-3	J6	G-4	Q32	H-2	R15	B-7	R60	L-7	R114	G-2	R159	L-2	R208	H-2	U9	H-5
C34	L-7	CR23	E-7	CR42	K-3	J7	H-1	Q33	H-1	R16	B-7	R61	L-7	R115	G-2	R160	L-1	R209	J-4	U10	J-5
C35	L-7	CR24	M-2	CR43	K-3	J8	H-2	Q34	H-2	R17	C-7	R62	L-7	R116	G-3	R161	M-2	R210	D-6	U11	K-7
C36	M-6	CR25	C-8	CR44	K-3	J9	F-2	Q35	H-2	R18	C-5	R63	L-7	R117	F-3	R162	M-2	R211	E-8	U12	D-8
C37	K-5	CR26	C-8	CR45	K-3	J10	C-3	U2E	J-1	R19	C-8	R64	L-7	R118	F-3	R163	K-2	R212	F-8	VR1	C-2
C40	F-3	CR27	H-6	CR46	F-1	J11	M-8	Q37	J-2	R20	C-6	R65	H-7	R119	H-2	R164	L-3	R213	F-8	VR2	C-2
C41	H-2	CR28	D-7	CR47	F-2	J12	M-7	Q38	G-1	R21	C-6	R66	H-5	R120	H-1	R165	L-4	R214	E-8	VR3	D-6
C42	J-1	CR29	J-3	CR48	F-2	J13	M-3	Q39	G-2	R22	C-6	R67	H-6	R121	H-1	R166	L-3	R215	E-8	VR4	L-7
C43	J-2	CR2	G-3	CR49	G-1	J14	M-4	Q40	G-3	R23	C-7	R69	H-5	R122	H-1	R167	L-4	R216	F-8	VR5	L-7
C44	J-2	CR3	B-3	CR50	K-3	J15	M-7	Q41	F-3	R24	C-7	R70	H-5	R123	H-2	R168	L-4	R217	D-8	VR6	L-7
C45	K-1	CR4	C-3	CR51	K-3	J16	M-7	Q42	G-3	R25	H-6	R71	H-5	R124	H-2	R169	L-4	R218	D-8	VR7	K-2
C46	F-2	CR5	B-3	CR52	K-3	J17	L-8	Q43	H-3	R26	D-7	R72	H-6	R125	H-2	R170	M-4	R219	D-8	VR8	K-3
C48	L-3	CR6	B-2	CR53	K-4	L1	H-8	Q44	H-3	R27	D-7	R73	H-5	R126	H-2	R171	G-3	R220	C-8	XA7	D-5
C50	L-2	CR7	B-3	CR54	H-6	L2	J-7	Q45	K-3	R28	E-7	R74	H-6	R127	J-1						



SERVICE SHEET 4, MNEMONICS

FG+	**Floodgun Positive** — voltage to CRT Floodgun — (Elevated)
FG–	**Floodgun Return**
FP INT	**Front Panel (Lamp) Intensity** — From gate shift register to vary Front Panel lamps in 7 discrete steps (LED reads 0-99).
PANEL+	**Panel Positive** — Panel lamp supply voltage.
PANEL–	**Panel Negative** — Panel lamp supply voltage return.

Note

Refer to Section VI for location of chassis mounted components and A9 Heat Sink Assembly components.

Service Sheet 4, Component Locator
P/O Low Voltage Power Supply Board, –12 V, –24 V, Floodgun, and Panel Outputs

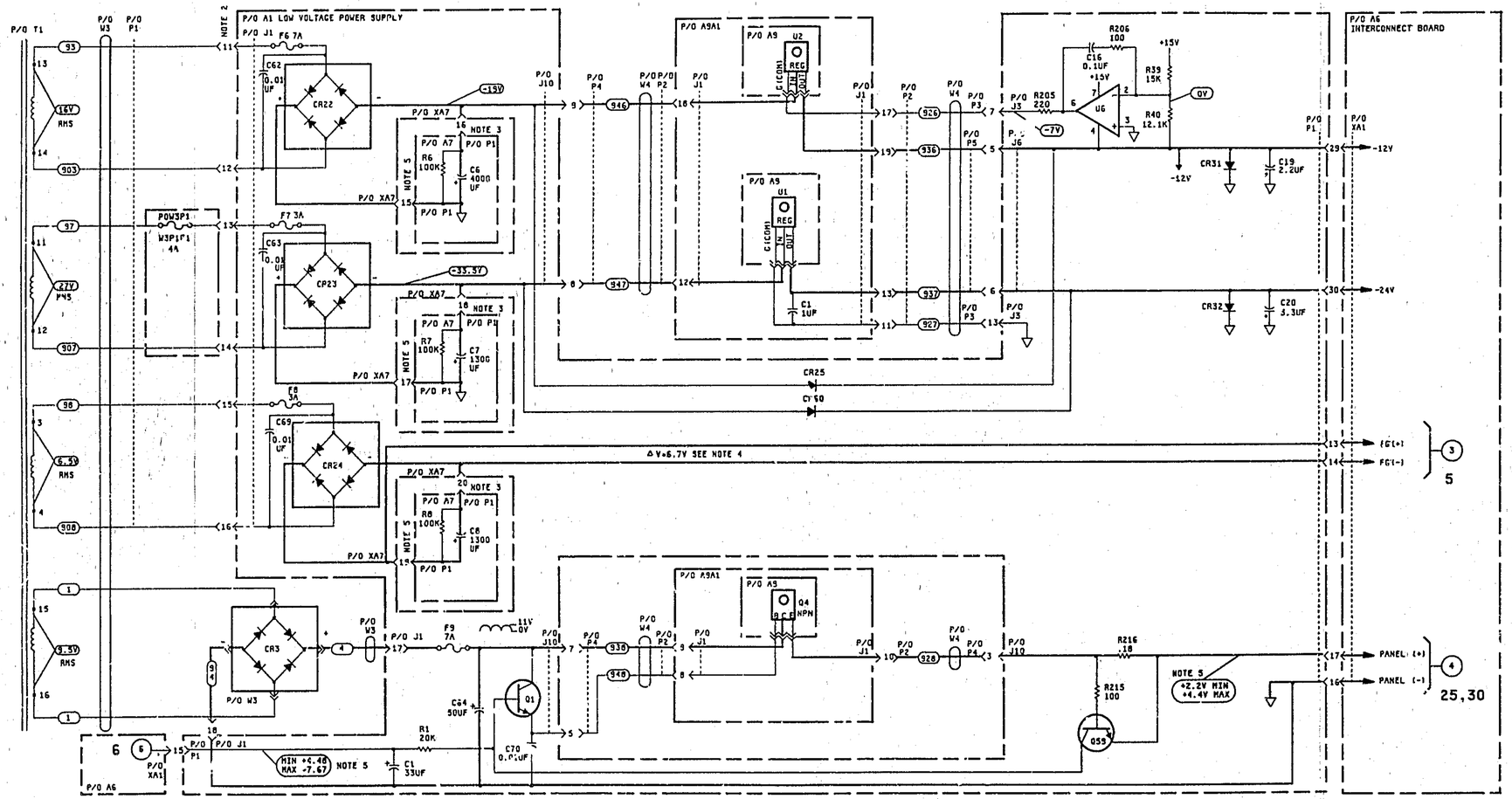
SERVICE SHEET 4 — THEORY OF OPERATION

−12 V Regulator. Approximately 16 V rms on T1 pins 13 and 14 is fused by A1F6, rectified by A1CR22, and filtered by A7C6. The filtered voltage is applied to the IN terminal of the regulator IC A9U2. The series regulator is controlled by Op Amp A1U6. A reference for the negative input of the Op Amp is developed from the +15 V and the −12 V output. The positive input side is tied to ground. If the −12 V output changes, the voltage at A1U6 pin 2 will change which changes the reference for the voltage regulator A9U2. When the potential at the common input of the regulator changes, the regulator changes the −12 V output in an attempt to maintain −12 V from the common input. The regulator I.C. has an internal current limit circuit.

−24 V Regulator. Approximately 27 V rms on T1 pins 11 and 12 is fused by A1F7, rectified by A1CR23, and filtered by A7C7. The filtered voltage is applied to the IN terminal of the regulator IC A9U1. The series regulator is referenced to ground at its common input. If the −24 V output changes, the series regulator changes the output to maintain −24 volts from its common input. The regulator I.C. has an internal current limit circuit.

Flood Gun Power Supply. Approximately 6.6 V rms on T1 pins 3 and 4 is fused by A1F8, rectified by A1CR24, and filtered by A7C8. The voltage across A7C8 is available to Service Sheet 5 as the Flood Gun voltage. This supply is not referenced to ground, therefore, all readings must be taken using FG(−) as the reference.

Panel Lamps Supply. Approximately 9.5 V rms on T1 pins 15 and 16 is rectified by CR3 (mounted on the 1980 chassis), fused by A1F9, and filtered by A1C64. A9Q4 is a series regulator which is controlled by transistor A1Q1. The input to the base of A1Q1 is a voltage which is proportional to the setting of the control knob when assigned to panel intensity. If the input voltage to A1Q1 is changed, the current through A9Q4 will also change and change panel lamp intensity. A1Q59 is the current limit transistor.



NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
2. CONNECTIONS BETWEEN W3P1 AND A1J1 ARE MADE USING CONNECTOR HOLDER E1
3. CONNECTIONS BETWEEN XA7 AND A7P1 ARE MADE USING CONNECTOR HOLDER E2
4. Δ V TAKEN WITH "CRAT INTEN" FULL ON LEVEL ABOVE GND CHANGES WITH FG PATT ADJUSTMENT.
5. VOLTAGE READINGS WILL CHANGE IN STEPS BETWEEN MIN AND MAX READINGS AS PANEL INTENSITY IS CHANGED.

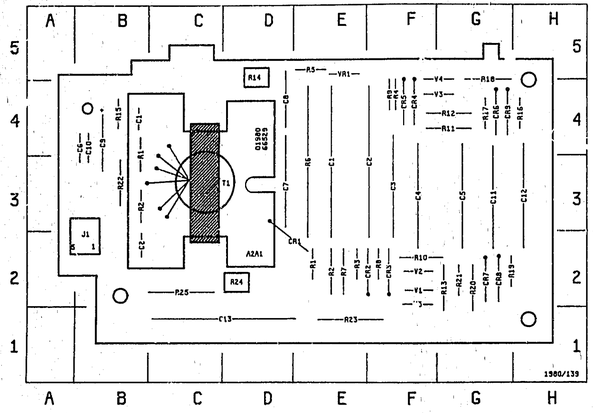
PARTS ON THIS SCHEMATIC

P/O A1	P/O A9	P/O A6
C1,16,19,20, 62-64,69,70 CR22-25,31,32 F6-9 P/O J1,3,6,10 P/O P1 Q1,59 R1,39,40,205, 206,215,216 U6 P/O XA7	P/O A9A1 Q4 U1,2 A1C1	P/O XA1
	CHASSIS	P/O A7
	CR2,3 P/O T1 P/O W3,4 P/O E1,2 W3P1F1	C6-8 P/O P1 R6-8

1980/206/10/7/81

4

Service Sheet 4. Schematic Diagram
P/O Low Voltage Power Supply Board, -12 V, -24 V, Floodgun, and Panel Outputs



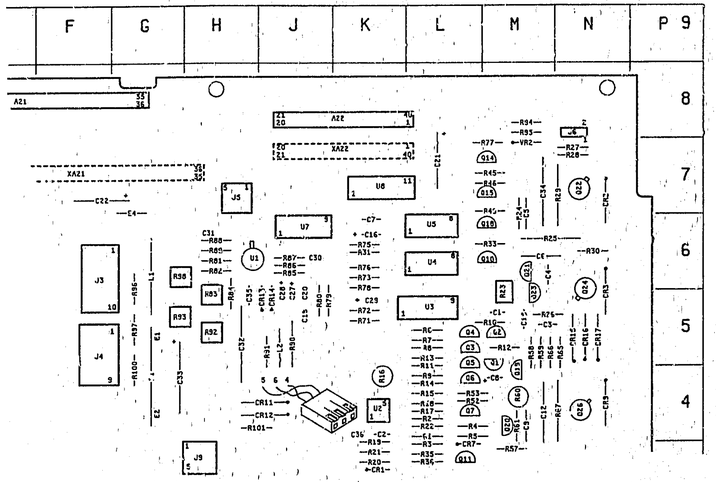
A2

A2 HVPS BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1C1	B-4	CR4	F-4	R14	D-4
A1C2	B-2	CR5	F-4	R15	B-4
A1R1	B-4	CR6	G-4	R16	H-4
A1R2	B-3	CR7	G-2	R17	G-4
A1T1	D-3	CR8	G-2	R18	G-4
C1	E-3	CR9	G-4	R19	G-2
C2	F-3	J1	B-2	R20	G-2
C3	F-3	R1	E-2	R21	E-4
C4	F-3	R2	E-2	R22	B-3
C5	G-3	R3	E-2	R23	E-7
C6	B-4	R4	F-4	R24	D-2
C7	D-3	R5	E-5	R25	C-2
C8	B-4	R6	E-3	TP1	E-2
C9	B-4	R7	E-2	TP2	F-4
C10	B-4	R8	F-2	TP3	G-2
C11	G-3	R9	F-4	V1	F-2
C12	H-3	R10	F-2	V2	F-2
C13	D-1	R11	G-4	V3	G-4
CR1	D-2	R12	G-4	V4	G-4
CR2	F-2	R13	F-2	VR1	E-4
CR3	F-2				

A3 GATE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A21	E-8	C32	H-5	J2	C-2	Q21	M-6	R24	M-6	R58	M-6	R89	H-6
A22	K-8	C33	G-4	J3	F-6	Q22	N-7	R25	M-6	R59	M-5	R90	J-5
C1	M-6	C35	M-7	J4	F-5	Q23	M-5	R26	M-5	R60	M-4	R91	J-5
C2	K-4	C36	H-5	J5	H-7	Q24	N-5	R27	N-7	R61	M-4	R92	H-5
C3	M-6	C38	K-4	J6	N-8	Q25	M-3	R28	N-7	R62	M-2	R93	G-5
C4	M-6	C37	K-3	J7	K-7	Q26	N-4	R29	N-7	R63	M-3	R94	M-8
C5	M-6	C38	K-3	J8	M-2	C27	M-2	R30	M-6	R64	M-3	R95	M-8
C6	M-6	C39	C-5	J9	H-5	Q28	N-3	R31	K-6	R65	N-6	R96	G-6
C7	K-6	C40	C-4	L1	G-6	R1	L-4	R33	M-6	R66	M-5	R97	G-5
C8	M-4	CR1	K-3	L2	J-5	R2	L-4	R34	J-3	R67	N-4	R98	G-6
C9	M-4	CR2	N-7	P1	F-3	R3	L-3	R35	L-3	R68	N-3	R99	L-2
C10	M-3	CR3	N-5	Q1	M-5	R4	L-4	R36	L-3	R69	L-2	R100	G-5
C11	M-3	CR6	M-3	Q2	M-5	R5	L-4	R37	K-3	R70	L-2	R101	H-4
C12	M-4	CR7	L-3	Q3	L-6	R6	L-5	R38	K-3	R71	K-5	S1	B-2
C13	M-3	CR8	M-3	Q4	L-5	R7	L-5	R39	L-2	R72	K-5	U1	H-4
C14	M-2	C9	M-4	Q5	L-5	R8	L-5	R42	L-3	R73	K-6	U2	K-4
C15	M-5	CR10	N-3	Q6	L-4	R9	L-4	R43	L-3	R74	M-2	U3	L-5
C16	K-6	CR11	J-4	Q7	L-4	R10	M-5	R44	L-3	R75	K-6	U4	L-6
C17	M-2	CR12	J-4	Q8	L-3	R11	L-5	R45	M-7	R76	K-6	U5	L-6
C18	L-2	CR13	J-5	Q9	L-2	R12	M-5	R46	M-7	R77	M-7	U6	K-3
C19	J-5	CR14	J-5	Q10	M-6	R13	L-5	R47	L-3	R78	K-6	U7	J-6
C20	J-5	CR15	N-5	Q11	L-2	R14	L-4	R48	L-3	R79	J-5	U8	K-7
C21	L-7	CR16	N-5	Q12	L-3	R15	L-4	R49	M-7	R80	J-5	U9	C-4
C22	F-7	CR17	N-5	Q13	L-3	R16	K-4	R50	L-2	R81	H-6	U10	C-4
C23	C-7	E1	G-5	Q14	M-7	R17	L-4	R51	L-2	R82	H-6	U11	C-5
C24	B-7	E2	G-4	Q15	M-7	R18	L-3	R52	L-4	R83	H-5	U12	C-6
C25	C-3	E3	A-3	Q16	L-2	R19	K-3	R53	L-4	R84	H-5	U13	B-3
C27	J-6	E4	G-7	Q17	L-2	R20	K-3	R54	L-3	R85	J-6	U14	B-3
C28	J-6	E5	D-3	Q18	M-6	R21	K-3	R55	L-2	R86	J-6	VR2	M-7
C29	K-5	FI	G-4	Q19	M-4	R22	L-4	R56	L-2	R87	J-6	XA21	F-7
C30	J-6	J1	E-2	Q20	M-3	R23	M-6	R57	M-3	R88	H-6	XA22	J-7
C31	H-5												



SERVICE SHEET 5 MNEMONICS

FG+	Floodgun Positive — voltage to CRT Floodgun. - (Elevated)
FG-	Floodgun Return

Service Sheet 5. Component Locator
High Voltage Power Supply and CRT

SERVICE SHEET 5 — THEORY OF OPERATION

High-voltage Oscillator. The high-voltage power supply consists of an oscillator and a rectifing circuit. Transistor Q1 is made to oscillate because of feedback between transformer A2A1T1's primary winding in combination with feedback from the secondary windings through A3U1. With varying conduction through Q1, the circuit oscillates at a rate determined by the inherent distributed inductance and capacitance of the oscillator circuit, consequently the output of the power supply is controlled by the voltage at the output of differential amplifier A3U1.

High-voltage Regulator. Operational Amplifier A3U1 compares the voltage at the junction of A2R6 and A3R83 with ground, then drives HV Oscillator Q1 to compensate for any differences. The voltage level is determined by the divider action of A3R81, A3R82, and A3R83. For example, an increase in the cathode current of the CRT (V1) will tend to change the cathode voltage resulting in the (+) input of A3U1 going positive. The output of A3U1 follows the input, forcing Q1 to conduct harder. When the oscillator conducts harder, the HV from A2CR1 goes more negative returning the input of A3U1 to 0 V (equal to the reference level applied to the (−) input (pin 2).

High-Voltage Rectifier. The CRT cathode and grid voltages are developed in the secondary of the high-voltage transformer A2A1T1. The cathode voltage is rectified and filtered before application to the cathode of the CRT. It is also used as a feedback control to the high-voltage oscillator, as reference for the CRT filament winding, as a reference for the grid bias supply, and for the focus voltage divider network. The cathode voltage is set to −2750 volts by A3R83.

The CRT grid voltage is partly derived from the secondary winding of transformer A2A1T1 at TP2. This voltage is applied through an RC network (A2A1C1, A2A1R1) to diodes that clamp the voltage swing upper level with the intensity limit control circuit and lower level with the gate output voltage waveform. Consequently the waveform at TP2 is an ac carrier with an upper level clamped at a dc level and a lower level envelope which is modulated by the gate's output waveform.

The gate output is usually a squarewave which has a high and low level timed to turn the beam on during a trace and off during retrace. The grid is referenced to the cathode by A2R3 and A2R7. The result is a rectified grid voltage which has a dc level that follows the cathode voltage but differs from it by an amount proportional to the gate output waveform. This difference between grid and cathode voltage determines the beam intensity.

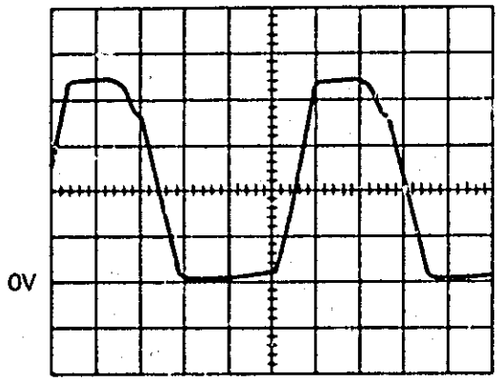
The Intensity Limit adjustment, A2R14, is to compensate for the difference in cutoff values of CRTs. The Intensity Limit should only require adjustment when the CRT has been changed. The Focus Limit, A2R24, is to adjust for optimum focus over the entire display area of the CRT.

The HV Multiplier voltage is picked off the secondary winding of transformer A2A1T1 at the cathode of A2CR1. The voltage is applied to assembly A11 where it is multiplied by 6, rectified, filtered, and then applied to the post accelerator of the CRT. The post accelerator voltage is approximately 16.5 kV.

TP 2

Monitor Oscilloscope Setup

20 Volts/Div
5 μSec/Div

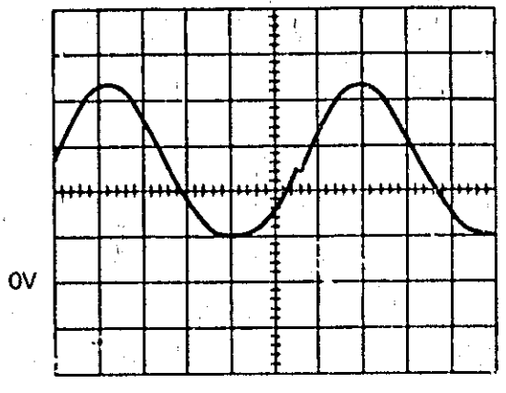


1980 Setup

Intensity Level 0

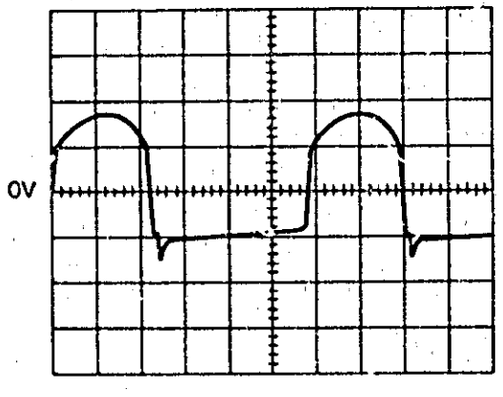
Monitor Oscilloscope Setup

10 Volts/Div
5 μSec/Div



Monitor Oscilloscope Setup

0.5 Volts/Div
5 μSec/Div

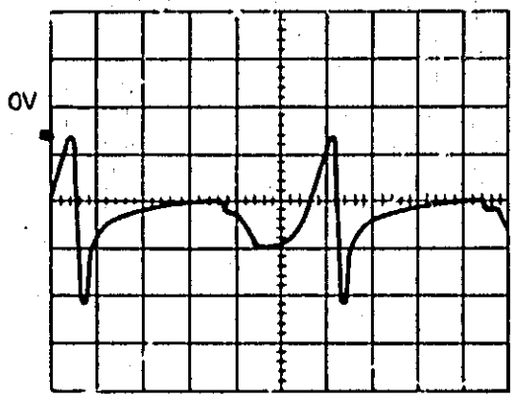


Service Sheet 5. Test Information
High Voltage Power Supply and CRT

C

Monitor
Oscilloscope
Setup

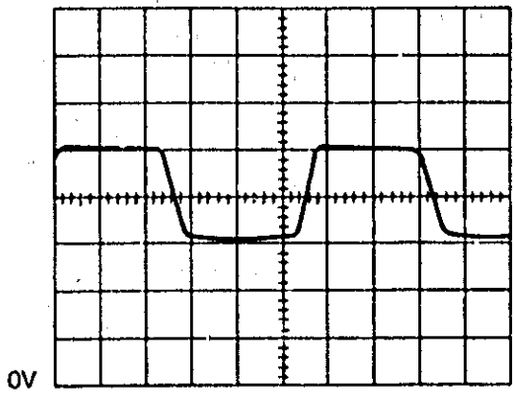
2 Volts/Div
5 μSec/Div



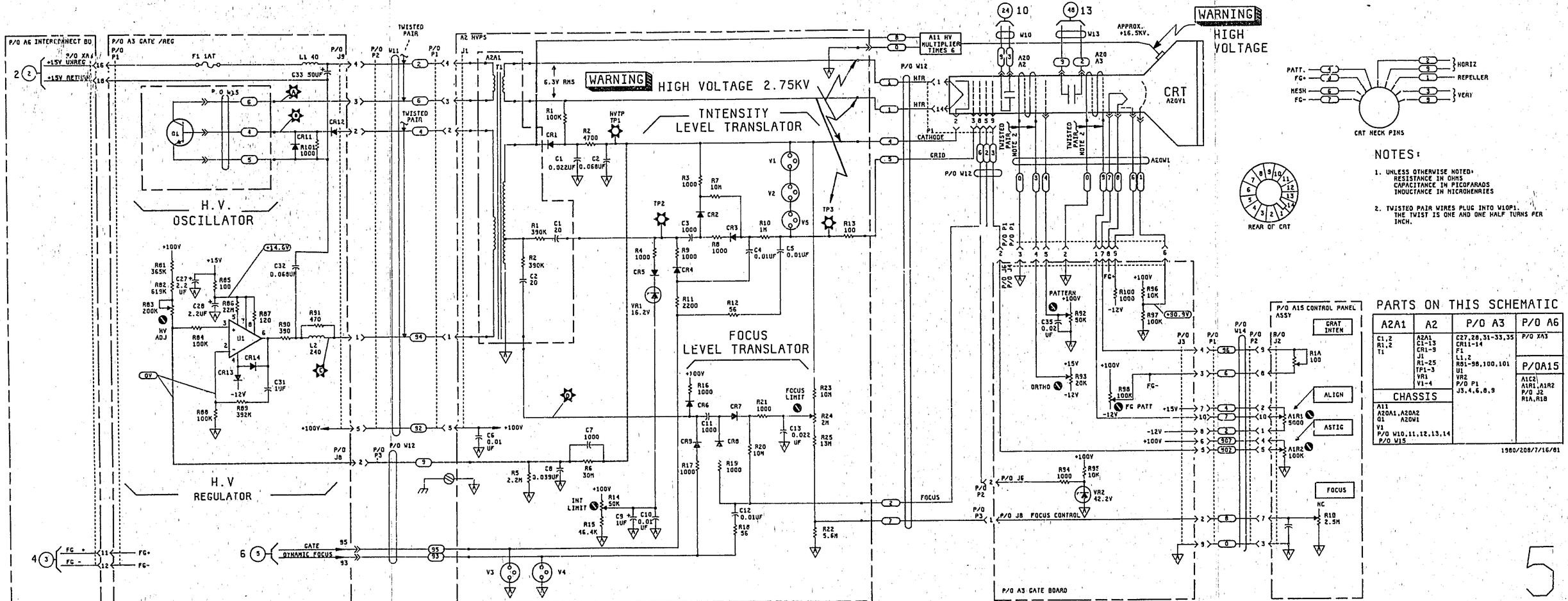
D

Monitor
Oscilloscope
Setup

20 Volts/Div
5 μSec/Div



1980
Setup
Intensity Level 0



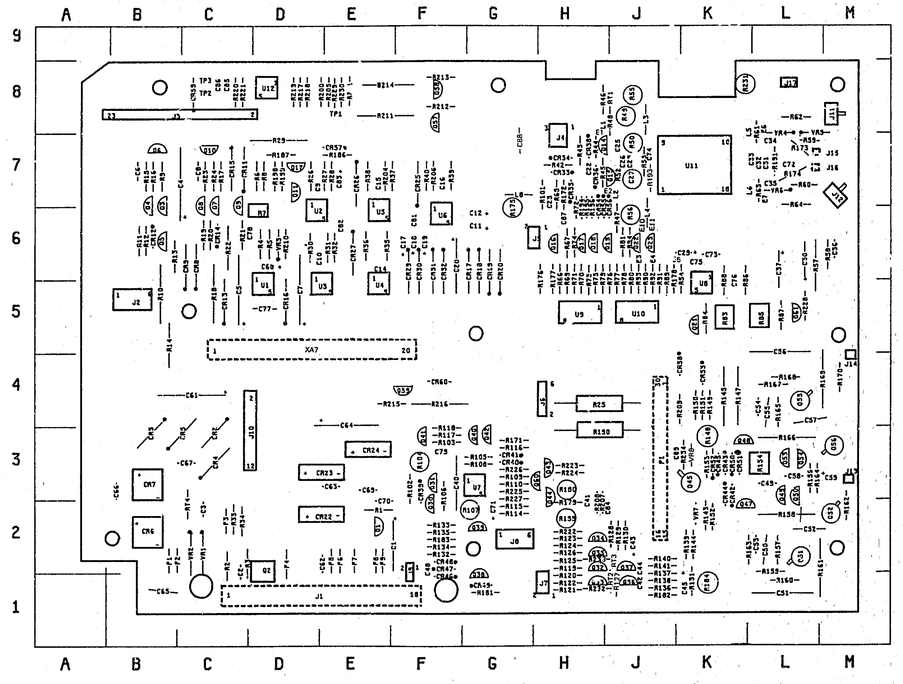
PARTS ON THIS SCHEMATIC

A2A1	A2	P/O A3	P/O A6
C1,2 R1,2 T1	A2A1 C1-13 CR1-9 J1 R1-25 TP1-3 VR1 V1-4	C27,28,31-33,35 CR11-14 F1 L1,2 R81-98,100,101 U1 VR2 P/O P1 J3,4,6,8,9	P/O XA3
CHASSIS			P/OA15
A11 A20A1,A20A2 Q1 A20W1 V1 P/O W10,11,12,13,14 P/O W15			A1C2 A1R1,A1R2 P/O J2 R1A,R1B

1980/208/7/16/81

A3 GATE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A21	E-8	C32	H-5	J2	C-7	Q21	M-6	R24	M-6	R58	M-5	R89	H-6
A22	K-8	C33	G-4	J3	F-6	Q22	N-7	R25	M-6	R59	M-5	R90	J-5
C1	M-5	C34	M-7	J4	F-5	Q23	M-5	R26	M-6	R60	M-4	R91	J-5
C2	K-4	C35	H-5	J5	H-7	Q24	N-5	R27	N-7	R61	M-4	R92	H-5
C3	M-5	C36	K-4	J6	N-8	Q25	M-3	R28	N-7	R62	M-2	R93	G-5
C4	M-6	C37	K-3	J7	K-2	Q26	N-4	R29	N-7	R63	M-3	R94	M-8
C5	M-6	C38	K-3	J8	M-2	Q27	M-2	R30	N-6	R64	M-3	R95	M-8
C6	J-6	C39	C-5	J9	H-3	Q28	N-3	R31	K-6	R65	M-5	R96	G-6
C7	K-6	C40	C-4	L1	G-8	R1	L-4	R32	M-6	R66	M-5	R97	G-5
C8	M-4	C41	K-3	L2	J-5	R2	L-4	R34	J-3	R67	N-4	R98	G-6
C9	M-4	CR2	N-7	P1	F-3	R3	L-3	R35	L-3	R68	N-3	R99	L-2
C10	M-3	CR3	N-5	Q1	M-5	R4	L-4	R36	L-3	R69	L-2	R100	G-5
C11	M-3	CR6	M-3	Q2	M-5	R5	L-4	R37	K-3	R70	L-2	R101	H-4
C12	M-4	CR7	L-3	Q3	L-5	R6	L-5	R38	K-3	R71	K-5	S1	B-2
C13	M-3	CR8	M-3	Q4	L-5	R7	L-5	R39	L-2	R72	K-5	U1	H-6
C14	M-2	CR9	N-4	Q5	L-5	R8	L-5	R42	L-3	R73	K-6	U2	K-4
C15	M-5	CR10	N-3	Q6	L-4	R9	L-4	R43	L-3	R74	M-2	U3	L-6
C16	K-6	CR11	J-4	Q7	L-4	R10	M-6	R44	L-3	R75	K-6	U4	L-6
C17	M-2	CR12	J-4	Q8	L-3	R11	L-5	R45	M-7	R76	K-6	U5	L-6
C18	L-2	CR13	J-5	Q9	L-3	R12	M-5	R46	M-7	R77	M-7	U6	L-3
C19	J-5	CR14	J-5	Q10	M-6	R13	L-5	R47	L-3	R78	K-6	U7	J-6
C20	J-5	CR15	N-5	Q11	L-3	R14	L-4	R48	L-3	R79	J-5	U8	K-7
C21	L-7	CR16	N-5	Q12	L-3	R15	L-4	R49	M-7	R80	J-5	U9	C-4
C22	F-7	CR17	N-5	Q13	L-3	R16	K-4	R50	L-2	R81	H-6	U10	C-4
C23	C-7	E1	G-5	Q14	M-7	R17	L-4	R51	L-2	R82	H-6	U11	C-5
C24	B-3	E2	G-4	Q16	M-7	R18	L-4	R52	L-4	R83	H-5	U12	C-6
C25	C-3	E3	A-2	Q16	L-2	R19	K-3	R53	L-4	R84	H-5	U13	B-3
C27	J-5	E4	G-7	Q17	L-2	R20	K-3	R54	L-3	R85	J-6	U14	B-3
C28	J-5	E5	D-3	Q18	M-6	R21	K-3	R55	L-2	R86	J-6	VR2	M-7
C29	K-5	F1	G-4	Q19	M-4	R22	L-4	R56	L-2	R87	J-6	XA21	F-7
C30	J-6	J1	E-2	Q20	M-4	R23	M-5	R57	M-3	R88	H-6	XA22	J-7
C31	H-6												



SERVICE SHEET 6 MNEMONICS

CHAR INTEN — **Character Intensity** — Analog voltage level from DAC (A3U7) to set character intensity.

CSG — **Clock, Serial Gated Data** — Clock from IO port to unblanking gate shift register.

FP INT — **Front Panel (Lamp) Intensity** — From gate shift register to vary Front Panel lamps in 7 discrete steps (LED reads 0-99).

HBG (PI) — **High, Blanking Gate (Plug-In)** — not presently used but is available for plug in use to blank beam as necessary.

HBLNK — **High, Blank** — Unblanks CRT for trace and blanks during retrace and holdoff.

HCHEN — **High, Character Enable** — Signal which activates character ramps in vertical and horizontal outputs while also enabling gate circuit to receive Z-axis unblanking

HDIM1, HDIM2, HDIM4 — **High, Delayed Intensity Modifier Bits** — Output from horizontal microcircuit to gate circuit where they are used during delayed and dual to modify delayed sweep intensity levels comparative to main sweep speeds in an attempt to maintain relatively even intensity regardless of sweep speeds.

HEXEN — **High, External Enable** — Exerted high when external X, Y, and Z inputs are to be used for deflection and blanking of beam.

HTDC — **High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.

INTEN — **Intensity** — Analog voltage level from the DAC to gate circuit to set beam intensity level.

LBFD — **Low, Beam Find** — When front panel "FIND BEAM" key is pressed, line is grounded to override intensity to obtain a viewable trace while decreasing vertical and horizontal gain to bring presentation on screen.

LCHZ — **Low, Character Z Blanking** — Shared by character generator and Digital Waveform Storage Option to form characters or digitized waveform - all unwanted "spaces" are blanked after beam is unblanked by HCHEN and intensity level set by CHAR INTEN.

LDSE — **Low, Delayed Sweep Enable** — After all necessary conditions have been met in the sweep control circuit the delayed sweep is enabled — it will then ramp (if in auto) or await HJST (if in TRGD).

LIN7 — **Low, Intensified** — Complement of HINT sent to the Gate amplifier to intensity main gate during delayed ramp time.

OPT INT — **Option Intensity** — Not connected.

SDTA — **Serial Data** — Data string from IO to various shift registers, when clocked into the shift register strings initiates various functions, lamps, etc.

SWP CAL — **Sweep Calibrate** — Output of gate shift register during front panel calibration sweep timing routine that enables HDTE signal to be inserted into vertical amplifier as a step to perform sweep time calibration.

Service Sheet 6. Component Locator
Gate and Dynamic Focus Circuits

SERVICE SHEET 6 — THEORY OF OPERATION

Main Sweep Gate. The main sweep gate is produced when A3Q9 is conducting. A3Q9 is biased to be normally conducting and is not conducting when any one of the current switch transistors (A3Q8,Q10,Q11,Q12,Q13) is gated on. Each of the current switch transistors is controlled by a different blanking signal. Current switch, A3Q12, is on when HCHEN (High, Character Enable) is high. HCHEN is high when characters are being written on the CRT. Current switch, A3Q8, is on when HBLNK (High, Blank) is high. HBLNK is high during the main sweep retrace. Current switch, A3Q13, is on when HBG(PI) (High, Blanking Gate (Plug In) is high. HBG(PI) may be used for some future expansion module and will always be low with the Enhancement Module removed. Current switch, A3Q11, is on when HEXEN (High, External Enable) and H=EXT BLANK are both high. HEXEN is high only in X-Y-Z Scope mode and H=EXT BLANK is from the Z Blanking input on the rear panel.

The amount of current flow through A3Q9 will determine the amplitude of the Gate signal to the CRT, and therefore the intensity of the beam. A3Q9's current is determined by the voltage level at the collector of A3Q7. When only a main sweep is displayed its intensity is determined by the signal INTEN which is an output from the DAC on the Processor Board. INTEN is an analog value that is proporational to the sweep intensity number set from the front panel Control Knob. When an intensified portion of the main sweep is displayed the signal LINT (Low, Intensified) is used to enable the Intensified Gate (A3Q5,Q6) to supply more current to A3Q9 during the intensified portion of the sweep. The INT RATIO (A3R16) adjustment adjusts the brightness of the intensified portion of the sweep. When a Delayed Sweep is present, its intensity is controlled by the DLYD INTENSITY MODIFIER (A3Q1 through A3Q4) circuit. The signal LDSE (Low, Delayed Sweep Enable) enables the circuit operation and HDIM1, HDIM2, and HDIM4 (High, Delayed Intensity Modifier) from the horizontal microcircuit are digital bits controlled by the main and delayed sweep speed. As the ratio of main to delayed sweep speed is increased, a more intense sweep is required to be visiable and more delayed intensity modifier bits will be active (high).

Character Sweep Gate. The character Sweep Gate is produced when A3Q16 is conducting. A3Q16 is biased to be normally conducting and is cutoff when A3Q17 is conducting. A3Q17 will cutoff when HCHEN (High, Character Enable) is high and LCHZ (Low, Character Z Axis) is low. The Character Sweep Gate is only produced when a dot of the character is to be displayed on the CRT. Character intensity is controlled by the front panel Control Knob through the digital to analog converter, A3U7, shown on Service Sheet 7.

Gate Output Amplifier. The Gate Output Amplifier is a shunt feedback stage consisting of transistors A3Q25 through A3Q28. A3Q25 and A3Q27 are emitter followers with A3Q25 providing the ac signal path. Resistor A3R64 provides the dc feedback path. Variable capacitor, A3C11 and potentiometer A3R63 control the fast corner response. The Dynamic Focus adjustment, A3R60, is to compensate for varations in the capacitive load of the CRT. The Dynamic Focus should only require adjustment after the CRT has been changed.

The output signal of the Gate circuits is a composite gate signal to the High Voltage Board Assembly. The composite signal is made up of Main Sweep level, Delayed Sweep level, Intensified level, and Character level.

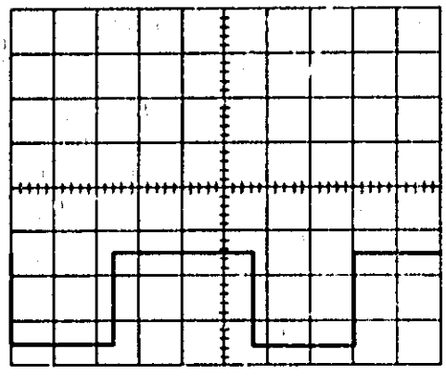
Dynamic Focus Circuit. The Dynamic Focus circuit is to maintain focus on the CRT while the display intensity is varied from one level to another. Dynamic Focus operates from the Gate Pulse levels.

Transistors A3Q19 and A3Q20 set up a reference level for the Dynamic Focus Amplifier. The reference bias level is adjustable with the potentiometer A3R60. The Dynamic Focus Output Amplifier is a shunt feedback stage consisting of transistors A3Q21 through A3Q24. A3Q21 and A3Q23 are emitter followers with A3Q21 providing the ac signal path. A3R25 provides the dc feedback path. Variable capacitor A3C6 controls fast corner response and A3R23 controls slightly slower corner response.

(A)

Monitor Oscilloscope Setup

0.5 Volts/Div
50 µSec/Div
Trig = Neg Slope



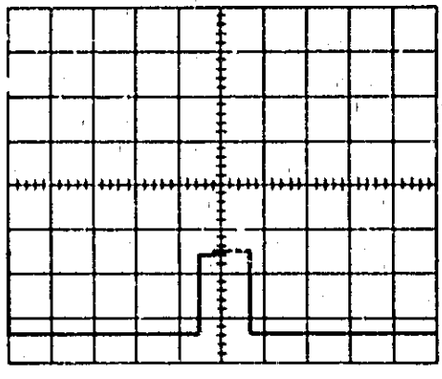
1980 Setup

Intensified Mode
Main Sec/Div = 20 µSec/Div
DLY'D Sec/Div = 10 µSec/Div
CHAR = OFF

(B)

Monitor Oscilloscope Setup

0.5 Volts/Div
50 µSec/Div
Trig = Neg Slope



1980 Setup

Intensified Mode
Main Sec/Div = 20µs
DLY'D Sec/Div = 10 µs
CHAR = OFF

Intensity Level 0
0 V DC

(C)

Intensity Level 99
+4 VDC

Intensity Level 0
+3.8 VDC

(D)

Intensity Level 99
-0.1 VDC

Intensity Level 0
+3.8 VDC

(E)

Intensity Level 99
+3.3 VDC

Service Sheet 6. Test Information
Gate and Dynamic Focus Circuits

Intensity Level 0
0 V

(F)

Intensity Level 99
-3.8 VDC

Intensity Level 0
0 V

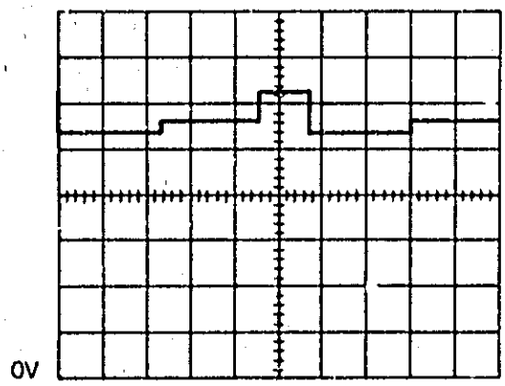
(G)

Intensity Level 99
-9.4 VDC

(H)

Monitor Oscilloscope Setup

10 Volts/Div
50 μSec/Div
Trig = Neg Slope



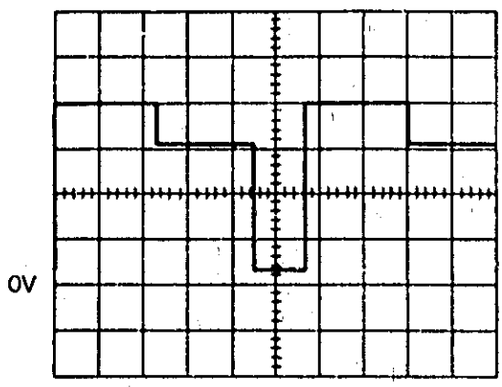
1980 Setup

Intensified Mode
Main Sec/Div = 20 μSec/Div
DLY/D Sec/Div = 10 μSec/Div
CHAR = OFF

(I)

Monitor Oscilloscope Setup

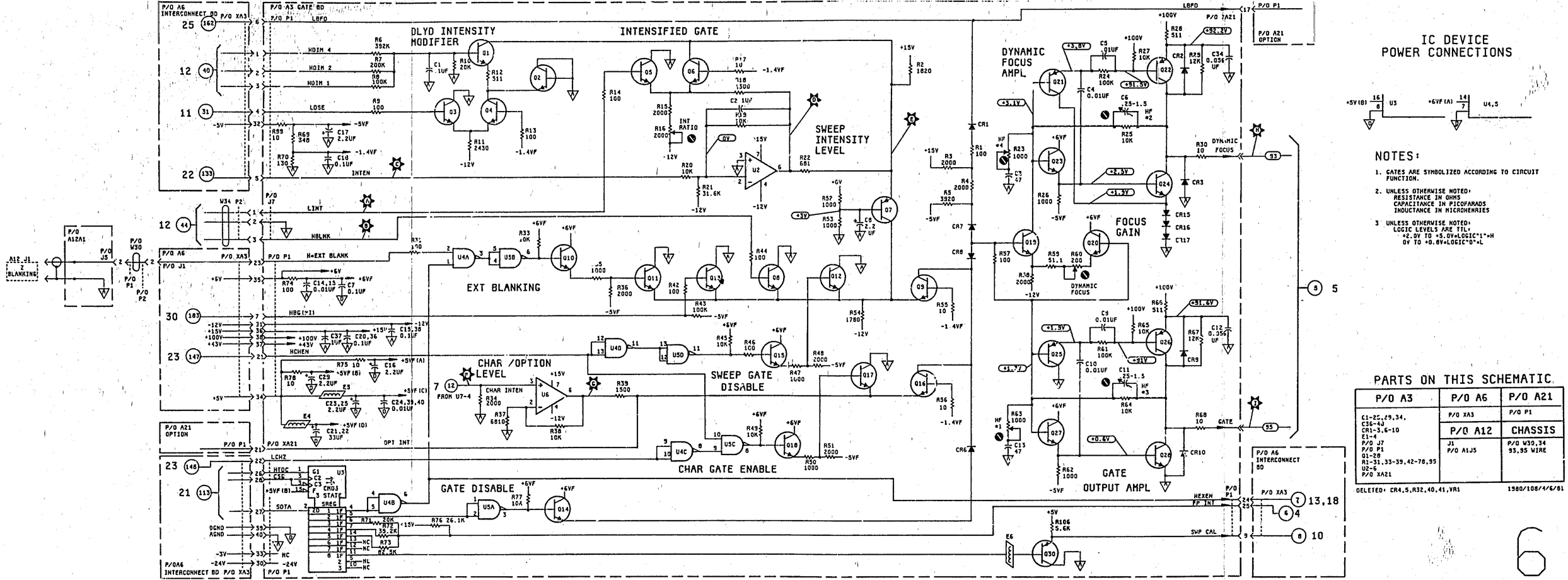
5 Volts/Div
50 μSec/Div
Trig = Pos Slope



1980 Setup

Intensified Mode
Main Sec/Div = 20 μSec/Div
DLY/D Sec/Div = 10 μSec/Div
CHAR = OFF

Service Sheet 6. Test Information
Gate and Dynamic Focus Circuits



IC DEVICE POWER CONNECTIONS

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A3	P/O A6	P/O A21
C1-25,29,34, C36-40 CR1-5,6-10 E1-4 P/O J7 P/O P1 Q1-28 R1-31,33-39,42-78,95 U2-6 P/O XA21	P/O XA3	P/O P1
	P/O A12	CHASSIS
	J1 P/O A1J5	P/O W30,34 93,95 WIRE

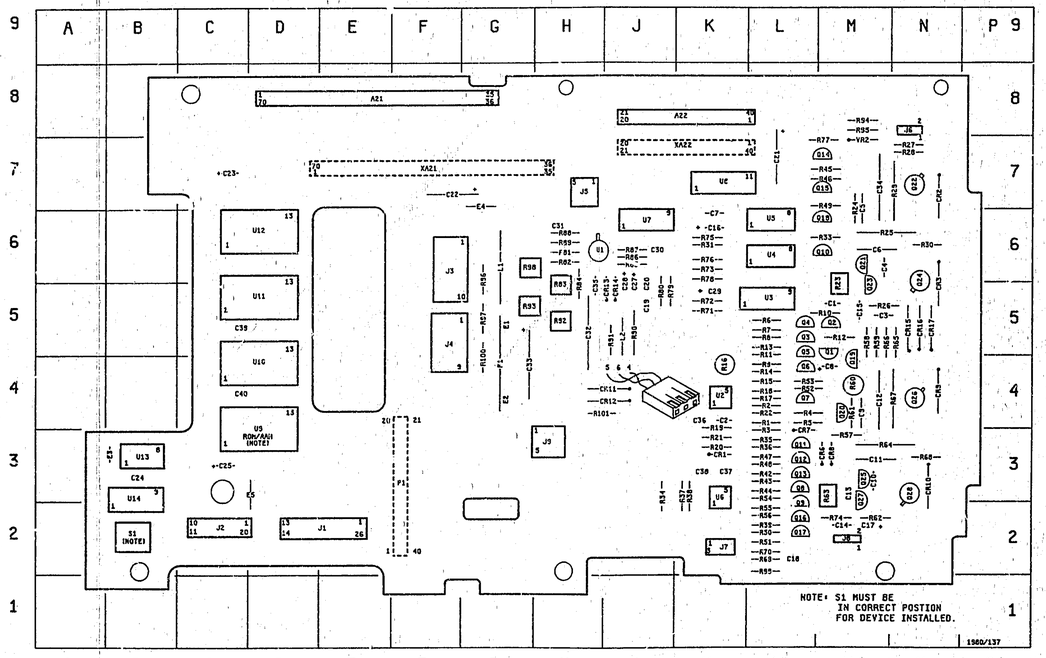
DELETED: CR4,5,R32,40,41,VR1

1980/108/4/6/81

A3 GATE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A21	E-8	C32	H-5	J2	C-2	Q21	M-6	R24	M-6	R58	M-5	R89	H-6
A22	K-8	C33	G-4	J3	F-6	Q22	N-7	R25	M-6	R59	J-5	R90	J-5
C1	M-5	C34	M-7	J4	F-5	Q23	M-5	R26	M-6	R60	M-4	R91	J-5
C2	K-4	C35	H-6	J5	N-7	Q24	N-6	R27	N-7	R61	M-4	R92	H-5
C3	M-5	C36	K-4	J6	N-8	Q25	M-3	R28	N-7	R62	M-2	R93	G-5
C4	M-6	C37	K-3	J7	K-2	Q26	N-4	R29	N-7	R63	M-3	R94	M-8
C5	M-6	C38	K-3	J8	M-2	Q27	M-2	R30	N-6	R64	M-3	R95	M-8
C6	M-6	C39	C-5	J9	N-3	Q28	N-3	R31	K-6	R65	N-5	R96	G-6
C7	K-6	C40	C-4	L1	G-6	R1	L-4	R33	M-6	R66	M-5	R97	G-5
C8	M-4	C11	K-3	L2	J-5	R2	L-4	R34	J-3	R67	N-4	R98	G-5
C9	M-4	C12	N-7	P1	F-3	R3	L-3	R35	L-3	R68	N-3	R99	L-2
C10	M-3	C13	N-5	Q1	M-5	R4	L-4	R36	L-3	R69	L-2	R100	G-5
C11	M-	C16	M-3	Q2	M-5	R5	L-4	R37	K-3	R70	L-2	R101	[illegible]
C12	M-	C17	L-3	Q3	L-5	R6	L-5	R38	K-3	R71	K-5	S1	K-2
C13	M-2	C18	M-3	Q4	L-5	R7	L-5	R39	L-2	R72	K-6	U1	H-6
C14	M-2	C19	N-1	Q5	L-5	R8	L-5	R42	L-3	R73	K-6	U2	K-4
C15	M-5	C110	N-3	Q6	L-4	R9	L-4	R43	L-3	R74	M-2	U3	L-5
C16	K-6	C111	J-4	Q7	L-4	R10	M-5	R44	L-3	R75	K-6	U4	L-6
C17	M-2	C112	J-4	Q8	L-3	R11	J-5	R45	M-7	R76	K-6	U5	L-5
C18	L-2	C113	J-5	Q9	L-2	R12	M-5	R46	M-7	R77	M-7	U6	K-3
C19	J-5	C114	J-5	Q10	M-6	R13	L-5	R47	L-3	R78	K-6	U7	J-5
C20	J-5	C115	N-5	Q11	L-3	R14	L-4	R48	L-3	R79	J-5	U8	K-7
C21	L-7	C116	N-5	Q12	L-3	R15	L-4	R49	M-7	R80	J-5	U9	C-4
C22	F-7	C117	N-5	Q13	L-4	R16	K-4	R50	L-2	R81	H-6	U10	C-4
C23	C-7	E1	G-5	Q14	M-7	R17	L-4	R51	L-2	R82	H-6	U11	C-5
C24	B-3	E2	G-4	Q15	M-7	R18	L-4	R52	L-4	R83	H-5	U12	C-6
C25	C-3	E3	A-3	Q16	L-2	R19	K-3	R53	L-4	R84	H-5	U13	B-3
C27	J-5	E4	G-7	Q17	L-2	R20	K-3	R54	L-3	R85	J-5	U14	B-3
C28	J-5	E5	D-3	Q18	M-6	R21	K-3	R55	L-2	R86	J-5	VR2	M-7
C29	K-5	F1	G-4	Q19	M-4	R22	L-4	R56	L-2	R87	J-5	XA21	F-7
C30	J-6	J1	E-2	Q20	M-4	R23	M-5	R57	M-2	R88	H-6	XA22	J-7
C31	H-6												

A3



SERVICE SHEET 7 MNEMONICS

A0-A15	**Address Lines 0-15** — A0-A7 are developed from the AD0-AD7 bus. A8 through A15 are most significant 8 bits of address.
AD0-AD7	**Address/Data bus** — microprocessor bidirectional bus. Data on this bus can be the least significant 8 bits of address.
ALE	**Address Latch Enable** — microprocessor output — falling edge is used to latch data on the AD0-AD7 bus into the address latch.
ARMT	**Arm Trigger** (Option signal).
B8, B9	**Bit 8, Bit 9** (Option signals).
CHAR INTEN	**Character Intensity** — Analog voltage level from DAC (A3U7) to set character intensity.
CLK	**Clock** — From microprocessor — 3.333333 MHz processor clock input divided by two.
CNT0	**Count Equals 0** ( )ption signal)
FIL	**Filter** — Option signal.
GET	**Group Execute Trigger** — from HP-IB — allows bus simulation of a FIND BEAM key closure.
HDB	**High, Display Blanking** — Option signal.
HDRQ2	**High, DMA Request 2** — DMA request from option —requests the DMA controller to interrupt processor and take control of the address and data buses to transfer data to the option.
HSTB	**High, Strobe** — Option signal.
HTC	**High, Terminal Count** — from DMA controller indicating the number of DMA cycles programmed have been completed. No more DMA requests will be honored until the DMA controller has been reprogrammed by the microprocessor.
IO/LM	**High, IO/Low, Memory** — selects either IO or Memory devices.
LDACK2	**Low, DMA Acknowledge 2** — From DMA controller to option acknowledging that processor has accepted interrupt and DMA data transfer has begun.
LCC	**Low, Conversion Complete** — Option signal.
LF	**Low, Function Enable** — Option signal.
LIOR	**Low, IO Read** — tells the selected IO device to output a byte of data on the AD0-AD7 lines - usually controlled by the DMA Controller.
LIOW	**Low, IO Write** — indicates to the selected IO device that a data byte is available on the AD0-AD7 lines - the IO device will then latch the data - usually controlled by the DMA controller.
LMEMR	**Low, Memory Read** — causes the addressed memory location to be read - usually controlled by the DMA controller.
LMEMW	**Low, Memory Write** — causes the memory device to write the data byte on the AD0-AD7 lines to the addressed memory location.
LOC	**Low, Output Control** — Option signal.
LOPT RDY	**Low, Option Ready** — When low option puts processor into a wait state until it completes the bus operation.
LRD	**Low, Read** — Asserted by the microprocessor to read data from an addressed memory location.

Service Sheet 7. Component Locator
P/O Gate Board, Option Memory and Option Interface

SERVICE SHEET 7 MNEMONICS (CONT'D)

LWR	**Low, Write** — Asserted by the microprocessor to allow writing into an addressed memory location.
PB0-PB7	**Port B IO Lines 0-7** — Option signals.
RESET	Reset pulse from microprocessor to initalize peripherals to proper states at power up or power down.
X	**X Input** — Horizontal information transfer board to board in option.
XCOM	**X Input Common** — Ground on X input from option.
XDISP	**X Display Input** — Output of option to horizontal output for display.
Y	**Y Input** — Vertical information transfer board to board in option.
YCOM	**Y Input Common** — Ground on Y input from option.
YDISP	**Y Display Input** — Output of option to vertical output for display.

SERVICE SHEET 7 — THEORY OF OPERATION

Service Sheet 7 contains a character intensity digital to analog converter, a chip select encoder, and four locations for option memory.

Option Memory Select Encoder. When the address line A15 from the processor board is brought high the Chip Select Encoder, A3U14, is enabled. When enabled A3U14 encodes the address lines A12, A13, and A14 into eight possible low active outputs (G0 through G7). Three of the outputs are not used and five become chip select signals for option memory.

Character Intensity Digital to Analog Converter. Data on the Address/Data bus is clocked into the register A3U8 when LIOW (Low, I/O Write) is low. The AD0 through AD7 data is gated out of the register A3U8 when G4 from the Option Memory Select Encoder goes low. Digital data (AD0-AD7) into the D/A Converter A3U7 is changed to a voltage level of approximately 0 to −4 V. The intensity level out is to the Op Amp A3U6 (on Service Sheet 6) which controls the intensity level of characters or Digital Waveform Storage Option display if installed.

Option Memory. The socket A3U9 is able to accept either a ROM or a RAM. The switch A3S1 must be in the proper position for the device being operated. The sockets A3U10, A3U11, and A3U12 are wired for ROM operation only. See individual Option Instructions for installation and operation of these devices.

SERVICE SHEET 7 SIGNATURE ANALYSIS

Note
Remove Expansion Module before performing tests.

TEST 4. Chip Enable Test
(Service Sheets 18 and 19)

ε Set instrument power to off.

b. Signature Analyzer connections:
START ⅂ to TP6 (A15)
STOP ⅂ to TP6 (A15)
CLOCK ⎍ to TP5 (LRD)

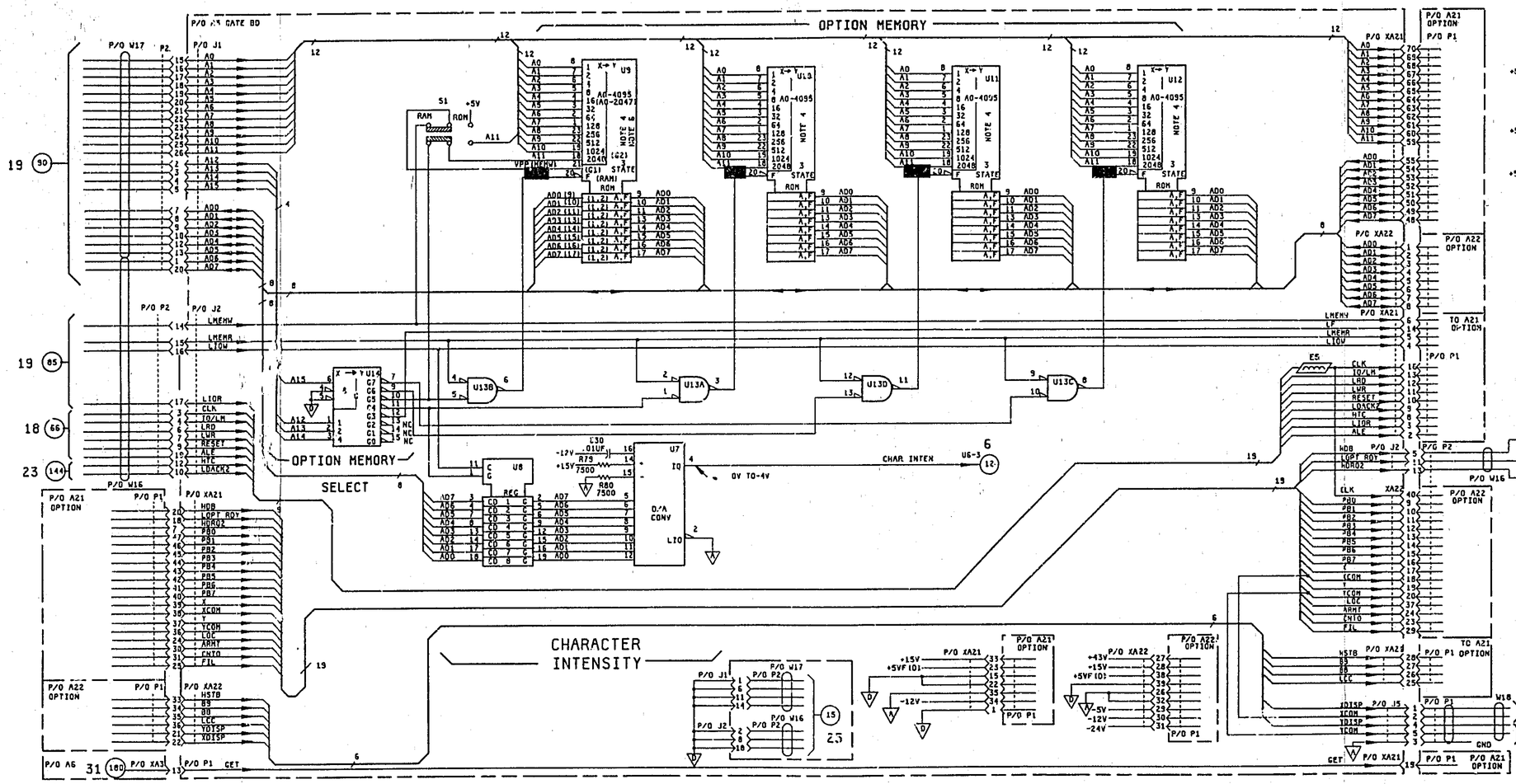
c. Set S1-B and S1-C to closed.

d. Set instrument power to on.

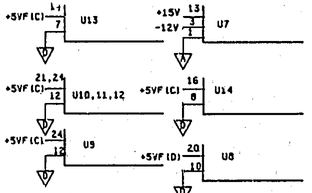
e.

TEST POINT		SIGNATURE	SS/GRID LOC
Probe to +5V		0001	
4-A	(U57-2)	0001	18/B5
4-B	(U57-3)	0001	
4-C	(U57-4)	0001	
4-D	(U57-5)	0001	
4-E	(U57-6)	0001	
4-F	(U57-7)	0001	
4-G	(U57-8)	0001	
4-H	(U57-9)	0000	
4-J	(U3-18)	383A	19/B3
4-K	(U3-3)	7631	
4-L	(U3-16)	160U	
4-M	(U3-5)	04UH	
4-N	(U3-14)	CFHH	
4-P	(U3-7)	546U	
4-Q	(U3-9)	A640	
4-R	(U3-12)	C55F	
4-S	(A3U9-20)	54F5	7
4-T	(A3U10-20)	A711	7
4-U	(A3U11-20)	603C	7
4-V	(A3U12-20)	826U	7

f Set S1-B and S1-C to open



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L
4. U9,10,11,12 ARE FOR OPTIONS AND NOT NORMALLY INSTALLED ON PC ASSEMBLY
5. CONNECTORS A21 AND A22 (NOT SHOWN) ARE FOR OPTION SERVICE AND ARE WIRED IN PARALLEL WITH XA21 AND XA22
6. U9 MAY BE ROM OR RAM DEPENDING ON OPTION INSTALLED. SEE OPTION DOCUMENTATION.

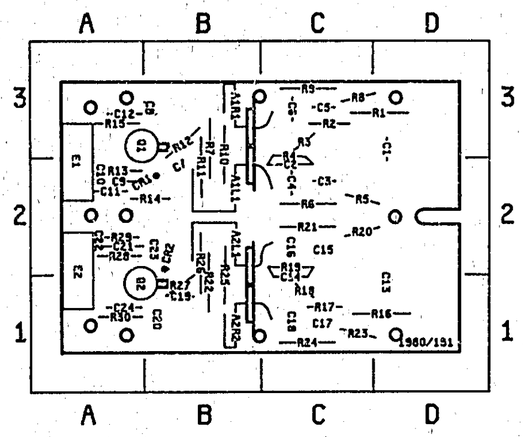
PARTS ON THIS SCHEMATIC

P/O A3	A21	A22
A21,22(NOTE 5) C30 F5 J1,2,5 R79,80 S1 P/O P1 U7-U14 XA21,22	P1	P1
	P/O A6	CHASSIS
	P/O XA3	P/O W16 P/O W17

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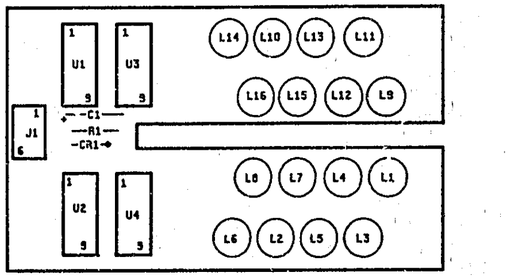
Service Sheet 7. Schematic Diagram
P/O Gate Board, Option Memory and Option Interface



A13A1

A13A1 VERTICAL ATTENUATOR BOARD, COMPONENT LOCATION

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1L1	B-2	C13	D-1	Q1	A-3	R15	A-3
A1R1	B-3	C14	C-1	Q2	A-1	R16	D-1
A2L1	B-2	C15	C-2	R1	D-3	R17	C-1
A2R1	B-1	C16	C-2	R2	C-3	R18	C-1
C1	D-3	C17	C-1	R3	C-3	R19	C-2
C2	C-2	C18	C-1	R4	C-3	R20	C-2
C3	C-2	C19	B-1	R5	C-2	R21	C-2
C4	C-2	C20	B-1	R6	C-2	R22	B-1
C5	C-3	C21	A-2	R7	B-3	R23	C-1
C6	C-3	C22	A-2	R8	C-3	R24	C-1
C7	B-2	C23	B-2	R9	C-3	R25	B-1
C8	B-3	C24	A-1	R10	D-3	R26	B-2
C9	A-2	CR1	B-2	R11	B-2	R27	B-1
C10	A-2	CR2	B-2	R12	B-3	R28	A-2
C11	A-2	E1	A-2	R13	A-2	R29	A-2
C12	A-3	E2	A-2	R14	B-2	T30	A-1



A13A2

SERVICE SHEET 8 MNEMONICS

CH1 BAL	**Channel 1 Balance** — From balance half of channel 1 FET to vertical preamplifier input.
CH2 BAL	**Channel 2 Balance** — From balance half of channel 2 FET to vertical preamplifier input.
CH1 SIG	**Channel 1 Signal** — From signal half of channel 1 FET to vertical preamplifier input.
CH2 SIG	**Channel 2 Signal** — From signal half of channel 2 FET to vertical preamplifier input.
CH1 VERT TAG	**Channel 1 Probe Tag** — Input to processor to denote probe division ratio and thereby alter channel gain accordingly.
CH2 VERT TAG	**Channel 2 Probe Tag** — Input to processor to denote probe division ratio and thereby alter channel gain accordingly.
CVT	**Clock, Vertical and Trigger** — Clock for vertical and trigger shift register string, to shift data through the string.
HTDC	**High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.
LB16	**Latch Bit 16** — 16th bit of a 56 bit serial data string.

Service Sheet 8. Component Locator
Vertical Attenuator

SERVICE SHEET 8 — THEORY OF OPERATION

The Vertical Attenuator is a series of switches to select attenuator ranges and input couplings. The attenuators also contain an input impedance matching device for each channel.

Attenuator Switching. All attenuator switching is controlled by the processor control system through the use of relay switching. Switching command data is from a serial data string, LB16 (Latch Bit 16), and is shifted into the proper storage register by the signal CVT (Clock, Vertical and Trigger). After LB16 is properly shifted into A13U2 and A13U1 the signal HTDC (High, Transfer Data Command) enables parallel output of the shift registers, A13U2,U1. Any high output from A13U2 or A13U1 through the inverter/drivers, A13U3 or A13U4, will cause a relay solenoid to be energized

The 16 relays in the Vertical Attenuator are made up of three pieces. The 16 relay solenoids are located on the solenoid board. Mounted on the frame below each solenoid is a moveable armature. When a solenoid is energized it creates a magnetic field which attracts the back of the armature. When the rear of the armature is pulled up, the front is forced down and will close a switch contact located on the attenuator board.

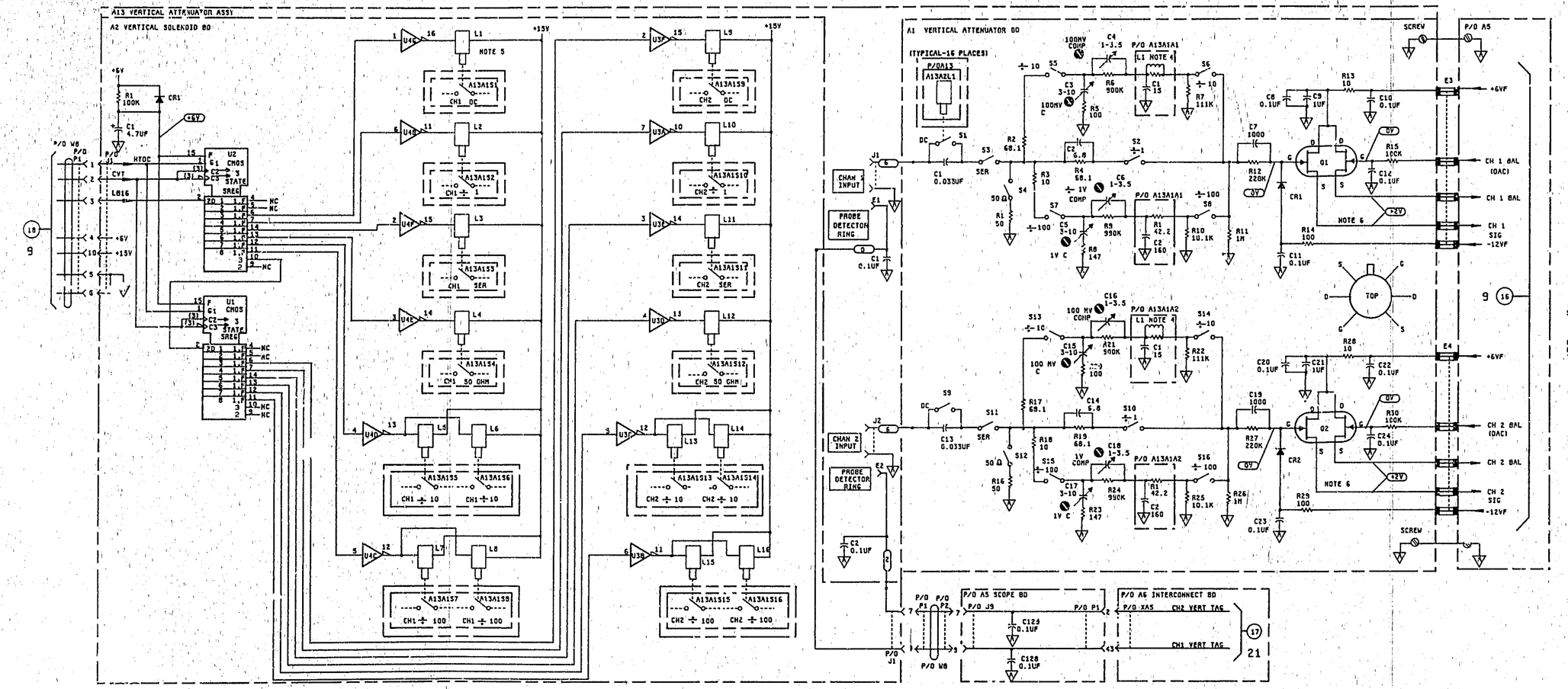
Attenuator Input Circuit. Each input is located on the 1980 front panel and contains a BNC connector with a conductive ring around the connector. When a 1008X series probe is connected to the BNC connector a probe key button makes contact with the conductive ring to identify the divider ratio of the attached probe. The probe detector rings are wired to the Processor Board as Vertical Tag signals.

Attenuator Board Assembly. The Attenuator Board Assembly contains two identical attenuator circuits, one for channel 1 input and the other for channel 2 input. The channel one and channel two attenuators are identical, therefore, only the channel one circuit will be discussed.

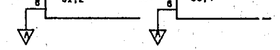
Input Coupling. When GND coupling is selected, S3 (Series Switch) is opened and ground is connected to the attenuator through S4 (50 ohm switch) and A13R1. All coupling modes except GND require S3 to be closed. If AC coupling is selected, the signal path is through C1. If DC coupling is selected, S1 (DC switch) will be closed shunting around A13C1. If 50 OHM DC is selected, S1 and S4 will both be closed causing a series DC signal path with 50 ohms to ground.

Attenuator Selection. When divide by one attenuation is selected S2 (÷1 switch) will be closed. If divide by ten is selected both 5 and S6 (÷10 switches) will be closed and if divide by 100 is selected S7 and S8 (÷100 switches) must be closed. The signal is attenuated and applied to the gate of a JFET, Q1. The JFET is connected in a source follower configuration. The other half of the JFET recieves a dc level from the DAC to set the operating level for the JFET. The operating level of the JFET is set so that 0 V is at the center of the CRT. Output of the Attenuator Board Assembly is CH1 SIG and CH1 BAL which go to the vertical preamp microcircuit shown on Service Sheet 9.

It is not recommended that repairs other than replacement of R1, R16, Q1, and Q2, be attempted on the Attenuator Board Assembly.



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. A13A1A1L1,A13A1A2L1 ARE 56 OHM 10% 1/4W RESISTORS WITH 10 TURNS AWG 32 WIRE WRAPPED AROUND THE BODY.
5. TYPICAL RESISTANCE OF EACH COIL L1-L16 IS APPX. 560 OHMS.
6. VOLTAGE DEPENDS ON GATE-TO-SOURCE VOLTAGE OF THE FET. TYPICAL VALUES RANGE BETWEEN +1V AND +3V THE VOLTAGE LEVEL AT THE SOURCES OF Q1A AND Q1B (Q2A AND Q2B) MUST BE EQUAL WITH NO INPUT TO J1(J2).

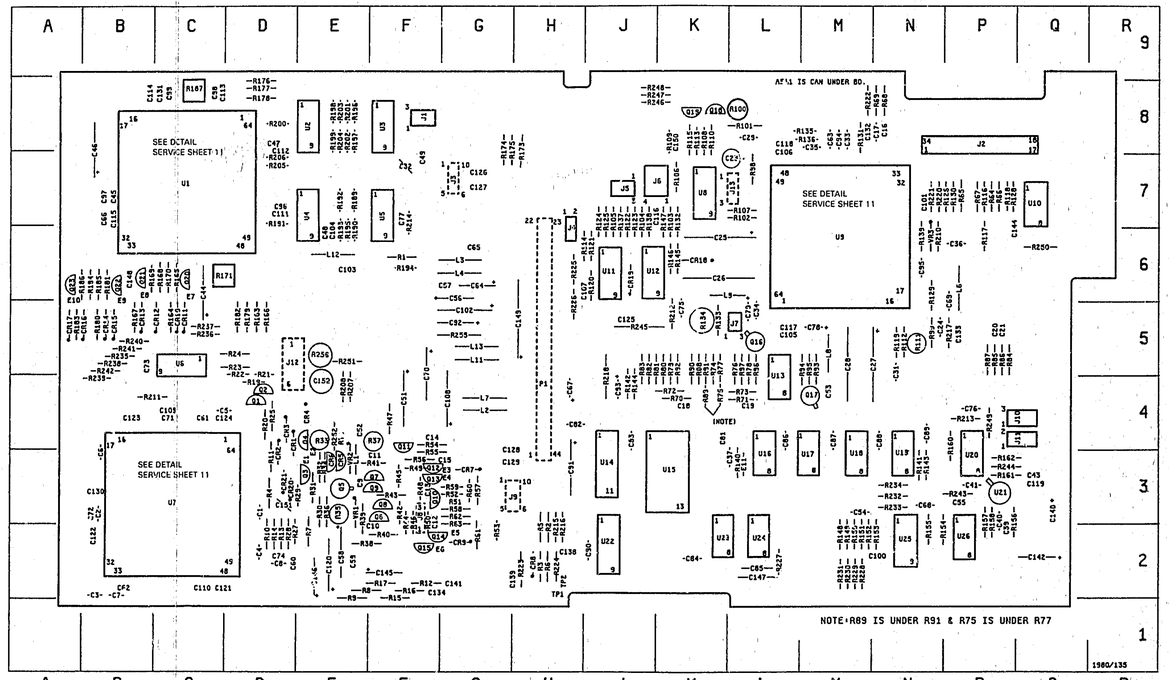
PARTS ON THIS SCHEMATIC

A13	A13A1	A13A1A1
A1,2 C1,2 E1,2 J1,2	A1,2 C1-24 CR1,2 E3,4 Q1,2 R1-30 S1-16	C1,2 R1 L1
A13A1A2	**A13A2**	**P/O A4**
C1,2 R1 L1	C1 CR1 U1-4 J1 L1-16 R1	P/O P1
P/O A5	**P/O A6**	**CHASSIS**
C128,129 P/O J9 P/O P1	P/O XA1, P/O XJ5	W8

1980/101/4/6/81

AS SCOPE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	L-9	C61	C-4	C118	L-8	E6	F-2	R2	H-2	R60	G-3	R116	P-7	R174	G-8	R232	N-3
C1	D-3	C62	D-3	C120	D-3	E7	C-6	R4	D-3	R62	G-3	R117	P-6	R175	G-8	R233	N-3
C2	B-3	C63	M-8	C120	E-3	E7	C-6	R4	D-3	R62	G-3	R118	P-7	R176	D-8	R234	N-3
C3	B-2	C64	G-6	C121	C-2	E8	B-6	R5	H-2	R63	G-3	R119	N-5	R177	D-8	R235	B-5
C4	D-2	C65	B-7	C122	B-2	E9	B-6	R6	E-2	R64	P-7	R120	J-6	R178	D-8	R236	C-5
C5	C-4	C66	B-7	C123	B-4	E10	A-6	R7	E-2	R65	P-7	R121	J-6	R179	D-8	R237	G-5
C6	B-3	C67	H-4	C124	C-4	E11	L-3	R8	E-2	R66	P-7	R122	J-7	R180	B-5	R238	B-5
C7	B-2	C68	N-3	C125	J-5	J1	F-8	R9	E-2	R67	P-7	R123	J-7	R181	B-6	R239	B-4
C8	D-2	C69	N-6	C126	G-7	J2	P-8	R10	D-2	R68	M-8	R124	J-7	R182	D-5	R240	B-5
C9	E-3	C70	F-6	C127	G-7	J3	G-7	R11	D-3	R69	M-8	R125	J-7	R183	A-5	R241	B-5
C10	F-2	C71	C-4	C128	G-3	J4	H-7	R12	F-2	R70	K-4	R126	N-7	R184	B-6	R242	B-5
C11	F-3	C72	B-3	C129	G-3	J5	J-7	R13	D-2	R71	L-4	R127	P-7	R185	E-6	R243	P-3
C12	F-2	C73	B-5	C130	B-3	J6	J-7	R14	D-2	R72	K-4	R128	N-6	R186	A-6	R244	P-3
C13	F-3	C74	D-2	C131	C-8	J7	L-5	R15	F-2	R73	L-4	R130	P-7	R187	C-8	R245	J-5
C14	F-4	C75	K-5	C132	M-8	J8	F-3	R16	F-2	R74	K-5	R131	M-8	R188	E-7	R246	J-8
C15	G-3	C76	P-4	C133	P-5	J9	G-3	R17	F-2	R75	K-4	R132	K-7	R190	E-6	R247	J-8
C16	N-8	C77	F-7	C134	F-3	J10	P-4	R18	D-4	R76	L-5	R133	K-6	R191	D-7	R248	J-8
C17	M-8	C78	M-5	C135	H-2	J11	P-4	R20	D-4	R77	K-5	R134	K-5	R192	E-7	R249	P-4
C18	K-4	C79	L-5	C139	H-2	J12	P-5	R21	D-5	R78	L-5	R135	M-8	R193	E-6	R250	G-6
C19	L-4	C81	K-4	C140	G-3	J13	L-7	R22	D-5	R79	K-5	R136	M-8	R194	F-6	R251	E-5
C20	P-5	C82	H-4	C141	G-3	L1	E-3	R23	D-5	R80	K-5	R137	J-7	R195	E-8	R252	E-4
C21	P-5	C83	J-4	C142	G-2	L2	G-4	R24	D-5	R81	J-5	R138	J-7	R196	E-8	R255	G-5
C23	L-6	C84	K-2	C144	P-8	L3	G-8	R25	D-4	R82	J-5	R139	N-6	R197	E-8	R256	E-5
C24	N-5	C85	L-2	C145	F-2	L4	G-6	R27	D-2	R83	J-5	R140	L-3	R198	E-8	R11	E-4
C25	K-6	C86	L-4	C146	E-2	L6	P-6	R28	D-2	R84	P-5	R141	N-3	R199	E-8	TP1	H-2
C26	K-6	C87	M-4	C147	L-2	L7	G-4	R29	E-3	R85	P-5	R142	J-4	R200	D-8	TP2	H-2
C27	M-5	C88	N-4	C148	B-6	L8	M-5	R30	E-3	R86	P-5	R143	N-3	R201	E-8	U1	C-7
C28	M-5	C89	M-4	C149	N-5	L9	K-6	R31	E-3	R87	P-5	R144	J-4	R202	E-8	U3	F-8
C29	L-8	C90	J-2	C150	K-8	L11	G-5	R32	E-3	R88	K-5	R145	K-6	R203	E-8	U4	F-8
C31	N-5	C91	H-3	C151	D-3	L12	E-6	R33	E-4	R89	K-4	R146	K-6	R204	E-8	U5	E-7
C32	F-8	C92	G-5	C152	E-4	L13	G-5	R34	E-3	R90	K-5	R147	K-7	R206	D-7	U6	F-7
C33	M-8	C93	J-4	CR1	D-4	P1	H-4	R35	E-3	R91	K-5	R148	M-2	R206	D-7	U6	C-5
C34	L-5	C94	M-8	CR2	D-3	Q1	D-4	R36	E-3	R92	K-6	R149	M-2	R207	E-4	U7	C-3
C35	M-8	C95	N-8	CR3	D-4	Q2	D-4	R37	F-4	R93	M-5	R150	M-2	R208	E-4	U8	K-7
C36	P-5	C96	D-7	CR4	E-4	Q3	E-3	R38	F-2	R94	M-5	R151	M-2	R210	N-4	U9	M-6
C37	K-3	C97	D-7	CR5	E-3	Q4	E-4	R39	E-3	R95	M-5	R152	M-2	R211	D-4	U10	Q7
C39	P-2	C98	C-8	CR6	E-3	Q5	E-3	R40	F-2	R96	L-5	R153	N-2	R212	K-5	U11	J-6
C40	P-2	C99	L-8	CR7	G-3	Q6	F-3	R41	F-3	R97	L-5	R154	N-2	R213	P-4	U12	J-6
C41	P-3	C100	N-2	CR8	H-2	Q7	F-3	R42	F-3	R98	L-7	R155	N-2	R214	F-7	U13	L-5
C43	G-3	C101	N-7	CR9	G-2	Q8	F-3	R43	F-3	R99	L-5	R156	P-2	R215	H-2	U14	L-3
C44	C-6	C102	G-5	CR10	C-5	Q9	F-3	R44	F-3	R100	L-8	R157	P-2	R216	H-2	U15	K-3
C45	B-7	C103	E-5	CR11	C-5	Q10	F-3	R45	F-3	R101	L-8	R158	P-2	R217	N-5	U16	L-3
C46	B-6	C104	E-5	CR12	B-5	Q11	F-4	R46	F-3	R102	L-7	R160	P-4	R218	J-4	U17	M-3
C47	D-8	C105	L-5	CR13	B-5	Q12	F-3	R47	F-4	R103	K-7	R161	P-3	R220	N-7	U18	N-3
C48	E-6	C106	L-5	CR14	L-5	Q13	F-3	R48	F-3	R104	K-7	R162	P-3	R221	N-7	U19	P-3
C49	F-7	C107	H-6	CR15	K-5	Q14	F-2	R49	F-3	R105	J-7	R163	D-5	R222	M-8	U20	P-3
C51	F-4	C108	G-7	CR16	A-5	Q15	F-2	R50	G-3	C106	K-7	R164	C-5	R223	H-2	U21	P-3
C52	E-4	C109	C-4	CR17	A-5	Q16	L-5	R51	G-3	R107	L-7	R165	C-5	R224	H-2	U22	J-2
C53	M-4	C110	C-2	CR18	K-6	Q17	M-4	R52	G-3	R108	K-8	R166	D-5	R225	H-5	U23	K-2
C54	M-3	C111	D-7	CR19	J-6	Q18	K-8	R53	G-2	R109	K-8	R167	B-5	R226	H-5	U24	L-2
C55	P-3	C112	D-8	CR20	D-3	R1	K-8	R54	F-4	R110	K-8	R168	C-5	R227	L-2	U25	N-2
C56	G-6	C113	C-8	CR21	D-3	R2	C-6	R55	F-3	R111	N-5	R169	B-6	728	M-2	U26	P-2
C57	G-6	C114	B-8	E1	E-3	R21	B-6	R56	F-3	R112	N-5	R170	C-6	R228	M-2	VR1	E-3
C58	E-2	C115	B-7	E2	E-3	R22	B-6	R57	G-3	R113	K-8	R171	C-6	R230	M-2	VR2	E-3
C59	E-2	C116	J-7	E3	G-3	R23	A-6	R59	G-3	R114	M-6	R173	H-5	R231	M-2	VR3	N-5
C60	D-2	C117	L-5	E4	G-3	R1	F-6	R59	G-2	R115	K-8						



SERVICE SHEET 9 MNEMONICS

CH1 BAL	**Channel 1 Balance** — From balance half of channel 1 FET to vertical preamplifier input.
CH2 BAL	**Channel 2 Balance** — From balance half of channel 2 FET to vertical preamplifier input.
CH1 BAL (DAC)	**Channel 1 Balance Voltage** — Analog voltage output of DAC to set channel 1 balance.
CH1 BAL (DAC)	**Channel 1 Balance Voltage** — Analog voltage output of DAC to set channel 2 balance.
CH1 GAIN	**Channel 1 Gain Voltage** — Analog voltage from DAC to set channel 1 gain (volts/division).
CH2 GAIN	**Channel 2 Gain Voltage** — Analog voltage from DAC to set channel 2 gain (volts/division).
CH1 SIG	**Channel 1 Signal** — From signal half of channel 1 FET to vertical preamplifier input.
CH2 SIG	**Channel 2 Signal** — From signal half of channel 2 FET to vertical preamplifier input.
CH1 POS	**Channel 1 Position Voltage** — Analog output of DAC to set vertical position of channel 1 trace.
CH2 POS	**Channel 2 Position Voltage** — Analog output of DAC to set vertical position of channel 2 trace.
CVT	**Clock, Vertical and Trigger** — Clock for vertical and trigger shift register string, to shift data through the string.
HBL	**High, Bandwidth Limit** — When high, limits vertical bandwidth to approximately 20 MHz.
HCH1	**High, Channel 1** — Bit to turn channel 1 on when desired.
HCH2	**High, Channel 2** — Bit to turn channel 2 on when desired.
HTDC	**High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.
LB16	**Latch Bit 16** — 16th bit of a 56 bit serial data string.
LB24	**Latch bit 24** — 24th bit of a 56 bit serial data string.
LSEN	**Low, Separate Enable** — From horizontal control circuit during dual sweep mode to separate main intensified and DLY'D traces.
SEP POS	**Separate Position Voltage** — Analog output of DAC to position the separation of traces in DUAL.

Service Sheet 9. Component Locator
P/O Scope Board, Vertical Preamp

SERVICE SHEET 9 — THEORY OF OPERATION

Service Sheet 9 contains the Vertical Preamplifier and the Delay Line Driver circuits. This Service Sheet also contains the Vertical Interface for the Enhancement modules, the Bandwidth Limit circuit, and the Dual Separation circuit.

Processor Control. Processor Control of the Vertical Preamp is through the serial data string LB24 (Latch Bit 24) and an eight bit shift register, A5U6. The serial data string contains data for the Trigger Preamplifier, Trigger Attenuator, Vertical Preamplifier, and Vertical Attenuator. This serial data string contains 48 useable data bits which are shifted through a series of shift registers. The shift register A5U6 is clocked by the signal CVT (Clock, Vertical and Trigger). A string of at least 48 CVT pulses must occur during the vertical and trigger load in order for the data to be latched into the correct shift register location. After completion of the CVT pulse string a HTDC (High, Transfer Data Command) will gate the data to the output of all the shift registers in the string.

Vertical Preamplifier. The Vertical Preamp is contained on a single hybrid intregrated circuit. Inputs to the Vertical Preamp are channel 1 and channel 2 vertical signals from the Vertical Attenuator Assembly, channel 1 and channel 2 Balance signals from the Vertical Attenuator Assembly, control data from the shift register A5U6, channel 1 and channel 2 Position signals from the microprocessor DAC, and HCH1 and HCH2 (High, Channel 1 and 2) select signals from the sweep control circuits.

Channel 1 and Channel 2 Position signals are dc levels from the DAC. The data for the DAC is stored when the Control Knob is assigned to channel 1 or channel 2 position. Channel 1 and Channel 2 Gain are dc levels and thier data is stored when the Control Knob is assigned to channel 1 or channel 2 volts/division. The control signals, stored in the shift registers, control the channel select (CH1 or CH2), the Preamp Gain Ch1(X5) or Ch2(X5), and trigger source for internal trigger (MAIN TRIG CH1, MAIN TRIG CH2, DLYD TRIG CH1, DLYD TRIG CH2).

Vertical Preamplifier Output. The vertical output signal from the vertical preamp intregrated circuit is on A5U7 pins 56 and 57. This is a differential signal which has been switched to select channel 1 or channel 2 operation or the channel 1 and channel 2 signals have been combined for 1+2 operation. The signal path for the differential vertical signal is through diodes A5CR20 and A5CR21 to the amplifiers A5Q3 and A5Q4. The vertical signal is then applied to the common emitter transistors A5Q5A and A5Q5B to be amplified further. The common emitter circuits of A5Q5A and A5Q5B contain a Gain adjustment (A5R35), a Balance adjustment (A5R33), two varactors (A5CR5,A5CR6), and a thermistor (A5RT1). The Gain and Balance adjustments center the operation of the circuits to the CRT. The thermistors resistance will change with temperature and change the biasing on the varactors. When the bias on the varactors is changed the capacitance of the devices changes. The changing capacitance in the emitters of A5Q5A and A5Q5B will change the high frequency gain of the transistors. The signal is again amplified by the preamplifier output stage. The output stage consists of two amplifiers (A5Q6 and A5Q8, A5Q7 and A5Q9) with feedback. Across the input of the feedback amplifiers is a pulse shaping network (A5C9,A5L1,A5R37) which is adjusted for best pulse response with HF1.

Enhancement Module Vertical Input. The vertical input from the enhancement module is a differential vertical signal which comes into the A5 board on J12 pins 5 and 6. The signal is added to the main vertical signal path through A5CR1 and A5CR4. Two enhancement vertical peaking adjustments (A5C152 and A5R256) are across the input and are adjusted for best pulse shape of the enhancement modules vertical signal.

Trigger View Vertical Input. The trigger view input from the horizontal microcircuit is a twisted pair of wires connected to the emitter resistors of A5Q1 and A5Q2. A5Q1 and A5Q2 are non-inverting amplifiers and isolate the horizontal microcircuit output from the vertical signal path.

Bandwidth Limit. Across the vertical output lines is a bandwidth limit circuit. When HBL (High, Bandwidth Limit) is high A5Q11 and A5Q10 will conduct placing A5C12 and A5C13 across the output to decrease bandwidth.

Dual Separation. If the 1980 is operating in the DUAL horizontal mode, the dual separation function may be activated from the Dual Separation key on the front panel. When Dual Separation is selected the signal LSEN (Low, Separate Enable) will go low allowing the separation circuit to operate by placing a ground on the bases of A5Q13 and A5Q14. LSEN is only low during the delayed sweep portion of the dual horizontal mode. SEP POS (Separate Position) is a dc potential from the microprocessor DAC which controls the amount of the separation of the delayed sweep from the main sweep. The separation circuit produces a dc offset on the output of the vertical signal lines which is proporational to the DAC number setup by the Control Knob when assigned to DUAL SEP.

Main and Delayed Sync. The sync outputs are a pickoff of the vertical signals which are conditioned for use by the Trigger Preamp.

TP 1



Range -0 VDC To +4 VDC

TYPICAL READING — +.12VDC To +3.0 VDC

Reading changes as Volts/Div (CH 1) is changed. Readings repeat on each range. Readings are end points measured as function (CH 1 Gain) is varied. Reading is calibration factor dependent.

TP 2



Range -0 VDC To +4 VDC

TYPICAL READING — +.12VDC To 3.0 VDC

Reading changes as Volts/Div (CH 2) is changed. Readings repeat on each range. Readings are end points measured as function (Ch2 Gain) is varied. Reading is calibration factor dependent.



Range -0VDC To +8 VDC

TYPICAL READING — +4.4 VDC To +6.9 VDC

Reading is calibration factor dependent. Readings are end points measured as function (CH 1 or CH2 POS) is varied.

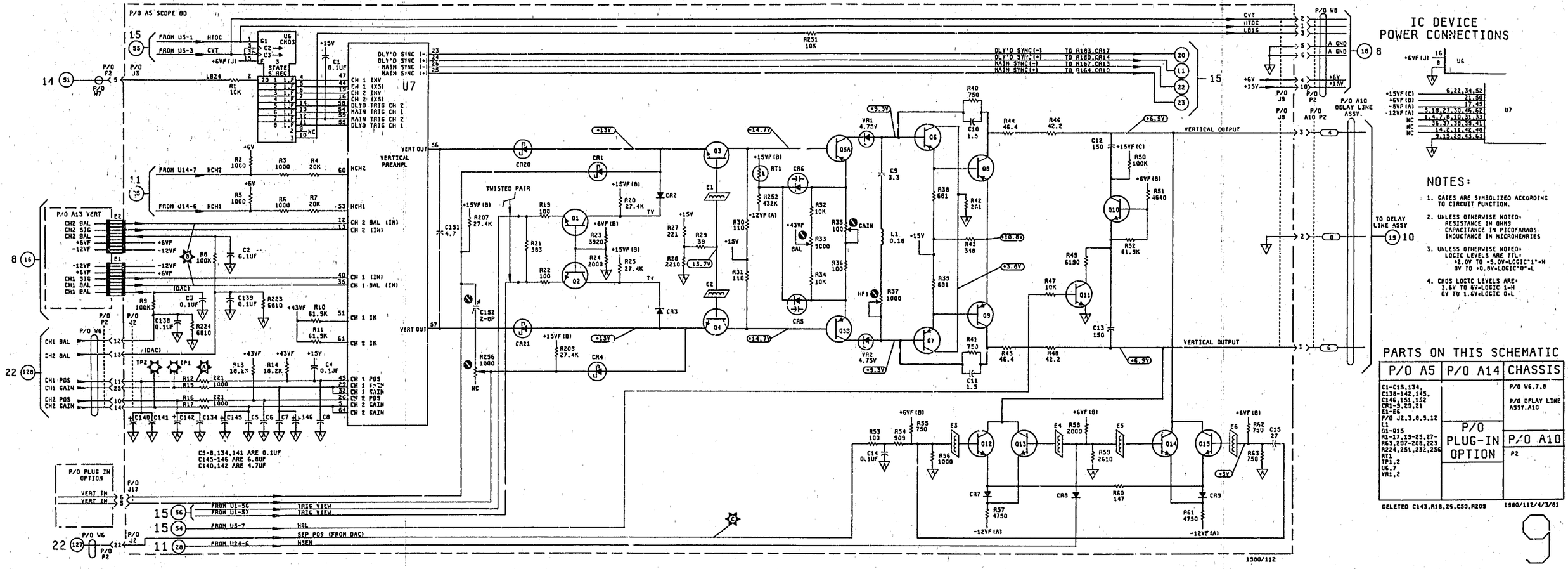


≅ 0 VDC

Each channel to Ground. Reading Valid if channel is balanced.
Reading is calibration factor dependent.



Range -0VDC to +4 VDC
Reading is calibration factor dependent.



IC DEVICE POWER CONNECTIONS

+6VF (J)	16	U6
	8	
+15VF (C)	6,22,34,52	U7
+6VF (B)	21,50	
-5VF (A)	17,45	
-12VF (A)	9,18,27,30,49,62	
NC	1,4,7,8,10,31,33	
NC	35,37,38,39,41	
NC	14,2,11,42,48	
	9,15,28,43,63	

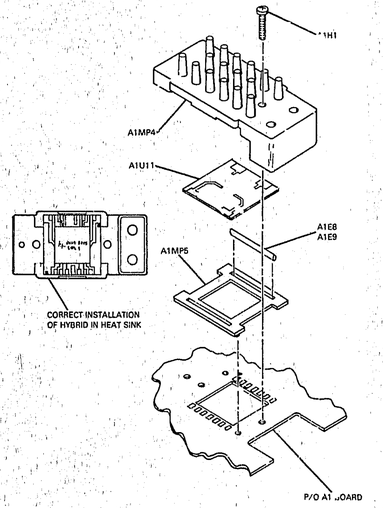
NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED: RESISTANCE IN OHMS, CAPACITANCE IN PICOFARADS, INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED: LOGIC LEVELS ARE TTL: +2.0V TO +5.0V=LOGIC "1"=H; 0V TO +0.8V=LOGIC "0"=L
4. CMOS LOGIC LEVELS ARE: 3.6V TO 6V=LOGIC 1=H; 0V TO 1.6V=LOGIC 0=L

PARTS ON THIS SCHEMATIC

P/O A5	P/O A14	CHASSIS
C1-C15,134, C138-142,145, C146,151,152 CR1-5,20,21 E1-E6 P/O J2,3,8,9,12 L1 Q1-Q15 R1-17,19-25,27-R63,207-208,223 R224,251,252,256 RT1 TP1,2 U6,7 VR1,2	P/O PLUG-IN OPTION	P/O W6,7,8 P/O DELAY LINE ASSY.A10 P/O A10 P2

DELETED C143,R18,25,C50,R209 — 1980/112/4/3/81

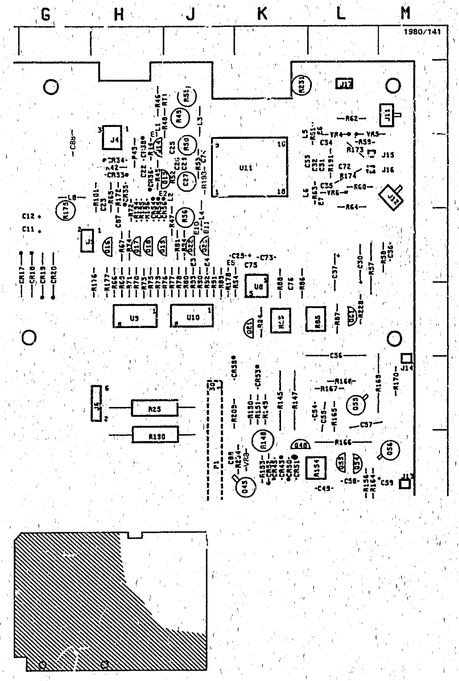


DETAIL OF VERTICAL OUTPUT AMPLIFIER ASSEMBLY

A1 LVPS BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C51	L-1	CR8	F-6	CR55	H-6	L3	J-6	Q47	K-2	R29	D-7	R76	H-6	R128	J-2	R172	H-7	R221	C-8
C2	C-2	C52	L-2	CR9	C-6	CR56	H-6	L4	J-6	Q48	K-3	R30	D-6	R76	H-6	R129	J-2	R173	L-7	R222	H-2
C3	C-3	C53	L-2	CR11	C-7	CR57	E-7	L5	K-7	Q49	L-3	R31	E-6	R77	H-5	R130	J-2	R174	L-7	R223	H-3
C4	B-7	C54	L-4	CR12	B-6	CR58	J-4	L6	K-7	Q50	L-3	R3-	E-6	R78	J-5	R131	K-1	R175	G-6	R224	H-3
C5	C-6	C55	L-4	CR13	C-6	CR59	C-8	L8	F-7	Q51	L-3	R3-	C-2	R79	H-5	R132	F-2	R176	H-6	R225	G-3
C6	B-7	C56	L-5	CR14	C-7	CR60	F-4	P1	J-3	Q52	M-2	R34	C-2	R80	-	R133	F-2	R177	H-5	R226	G-3
C7	D-5	C57	L-4	CR16	C-7	E1	J-7	Q1	E-2	Q53	L-3	R35	E-6	R81	J-6	R134	F-2	R178	J-5	R227	G-3
C8	C-7	C58	L-3	CR17	D-6	E2	J-7	Q2	D-2	Q54	L-3	R36	E-6	R83	K-6	R135	F-2	R179	H-2	R228	L-5
C9	E-7	C59	M-3	CR17	L-3	E3	J-6	Q3	B-7	Q55	L-4	R37	E-7	R84	K-5	R136	J-1	R180	H-3	R229	E-8
C10	D-6	C61	C-4	CR18	G-6	E4	J-6	Q4	B-7	Q56	M-3	R38	E-7	R85	L-5	R137	J-1	R181	G-1	R230	E-7
C11	G-6	C62	D-2	CR18	G-6	E5	K-6	Q5	B-6	Q57	F-8	R39	E-7	R86	K-6	R138	J-1	R182	J-1	R231	K-8
C12	G-6	C63	E-3	CR20	G-6	E6	L-7	Q6	E-7	Q58	F-8	R40	F-7	R87	L-5	R139	K-2	R183	F-2	R232	H-2
C13	E-4	C64	E-4	CR22	D-3	E7	L-7	Q7	C-7	Q59	F-8	R42	H-7	R88	K-5	R140	J-2	R184	K-1	R233	H-2
C15	E-7	C65	B-1	CR23	D-3	E10	J-6	Q8	C-7	Q60	G-3	R41	H-7	R89	J-6	R141	J-2	R186	E-7	R234	K-3
C16	F-7	C66	B-3	CR24	E-3	E11	J-6	Q9	C-7	Q61	L-7	R44	H-7	R90	J-6	R143	K-2	R187	D-7	RT1	H-8
C17	F-6	C67	C-3	CR26	F-7	F1	B-2	Q10	C-7	R1	E-2	R45	H-7	R91	J-6	R144	K-2	R190	H-3	*T2	J-1
C18	F-6	C68	D-6	CR28	E-7	F2	C-2	Q11	D-7	R2	D-2	R46	H-8	R92	J-6	R145	K-4	R191	L-7	H1	J-2
C19	F-6	C69	E-3	CR27	E-7	F3	C-2	Q12	D-7	R3	D-2	R47	J-6	R93	J-5	R147	K-4	R193	J-7	RT4	C-2
C20	F-6	C70	E-2	CR29	F-6	F4	D-2	Q14	H-7	R4	D-6	R48	H-8	R94	J-6	R148	K-3	R194	H-6	TP1	E-8
C22	H-7	C71	G-2	CR30	F-6	F5	E-2	Q15	H-7	R5	D-6	R49	J-7	R101	J-7	R149	K-4	R195	H-6	TP2	C-8
C23	H-7	C72	L-7	CR31	F-6	F6	E-2	Q16	H-6	R6	D-7	R50	J-7	R102	F-3	R150	K-4	R196	H-6	TP3	C-8
C25	J-7	C73	K-6	CR33	F-6	F7	E-2	Q17	H-6	R7	D-6	R52	J-7	R103	F-3	R151	I-1	R198	D-7	U1	D-6
C26	J-7	C74	J-7	CR33	H-7	F8	E-2	Q18	H-6	R8	D-7	R53	J-7	R104	F-3	R152	K-3	R199	D-7	U2	D-6
C27	J-7	C75	K-6	CR34	H-7	F9	E-2	Q19	H-6	R9	B-7	R54	J-5	R105	G-2	R153	K-2	R200	D-8	U3	D-5
C28	J-7	C76	L-5	CR35	H-7	J1	D-1	Q21	K-8	R10	B-6	R55	J-8	R106	F-3	R154	L-3	R201	E-8	U5	E-5
C29	K-6	C77	D-5	CR36	H-7	J2	B-6	Q22	J-6	R11	B-6	R56	J-6	R107	G-2	R155	H-2	R204	E-7	U6	E-5
C30	L-6	C78	C-6	CR38	H-7	J3	B-6	Q23	J-6	R12	B-6	R57	L-6	R108	G-3	R156	L-3	R205	E-8	U7	F-5
C31	L-7	C79	F-3	CR39	F-3	J4	H-7	Q30	F-2	R13	B-6	R58	M-6	R109	G-3	R157	L-2	R206	F-7	U8	G-3
C32	L-7	C81	F-6	CR40	G-3	J5	H-6	Q31	F-3	R14	B-7	R59	L-7	R110	G-3	R158	L-2	R207	H-2	U9	K-5
C33	K-7	C82	E-6	CR41	G-3	J6	G-4	Q32	H-2	R15	B-7	R60	L-7	R114	G-2	R160	L-2	R209	H-2	U6	H-5
C34	L-7	C83	E-7	CR42	K-3	J7	H-1	Q33	H-1	R16	B-7	R61	L-7	R115	G-2	R160	L-1	R208	J-4	U10	J-5
C35	L-7	C84	H-2	CR43	K-3	J8	G-2	Q34	H-2	R17	C-7	R62	I-1	R116	G-3	R161	M-7	R210	D-6	U11	K-7
C36	M-6	C85	C-8	CR44	K-3	J9	F-2	Q35	H-2	R18	C-6	R63	L-1	R117	F-3	R162	M-6	R211	E-8	U12	D-8
C37	K-6	C86	C-8	CR45	K-3	J10	C-6	Q36	J-1	R19	C-6	R64	J-5	R118	F-3	R163	K-2	R212	F-8	VR1	C-2
C40	F-3	C87	H-6	CR46	F-1	J11	M-8	Q37	J-2	R20	C-6	R65	H-7	R119	H-2	R164	L-3	R213	F-8	VR2	C-2
C41	H-2	C88	G-7	CR47	F-2	J12	M-7	Q38	G-1	R21	C-6	R66	H-5	R120	H-1	R165	L-4	R214	E-8	VR3	D-6
C42	J-1	C89	J-3	CR48	F-2	J13	M-3	Q39	G-1	R22	C-6	R67	H-6	R121	H-1	R166	L-3	R215	E-4	VR4	L-7
C43	J-2	CR2	C-3	CR49	G-1	J14	M-4	Q40	G-2	R23	C-7	R68	H-5	R122	H-1	R167	L-4	R216	F-4	VR5	L-7
C44	J-2	CR3	B-3	CR50	K-3	J15	M-7	Q41	F-3	R24	C-7	R70	H-5	R123	H-2	R168	L-4	R217	D-6	VR6	L-7
C45	K-1	CR4	C-3	CR51	K-3	J16	M-7	Q42	G-1	R25	H-4	R71	H-5	R124	H-2	R169	L-4	R218	D-8	VR7	K-2
C48	F-2	CR5	B-3	CR52	K-3	J17	L-8	Q43	H-1	R26	D-7	R72	H-6	J26	H-2	R170	M-4	R219	D-8	U10	K-3
C49	L-3	CR6	B-2	CR53	K-4	L1	H-8	Q44	H-2	R27	D-7	R73	H-5	R126	H-2	R171	G-3	R220	C-8	XA7	D-5
C50	L-2	CR7	B-3	*R54	H-6	L2	J-7	Q45	K-3	R28	E-7	R74	H-6	R127	J-1						

A1



SERVICE SHEET 10 MNEMONICS

HCHEN	**High, Character Enable** — Signal which activates character ramps in vertical and horizontal outputs while also enabling gate circuit to receive Z-axis unblanking.
HCHRV	**High, Character Reset Vertical** — Signal from video controller that synchronizes and activates character ramp vertically.
HDTE	**High, Delayed Trigger Enable** — Generated at end of main sweep and applied to trigger circuit to allow HDST to be generated when desired.
HEXEN	**High, External Enable** — Exerted high when external X, Y, and Z inputs are to be used for deflection and blanking of beam.
LBFD	**Low, Beam Find** — When front panel "FIND BEAM" key is pressed, line is grounded to override intensity to viewable trace while decreasing vertical and horizontal gain to bring viewable presentation on screen.
SWP CAL	**Sweep Calibrate** — Output of gate shift register during front panel sweep timing routine that enables HDTE signal to be inserted into vertical amplifier as a step used to perform sweep time calibration.
Y AXIS	**Y-Axis Input** — Vertical input from rear panel to be used for digital display (outputs from HP Model 1607 or similar).
YCOM	**Y Input Common** — Ground on Y input from option.
YDISP	**Y Display Input** — Output of option to vertical output for display.

Service Sheet 10. Component Locator
P/O Low Voltage Power Supply Board, Vertical Output

SERVICE SHEET 10 — THEORY OF OPERATION

Service Sheet 10 contains the Delay Line Assembly, A10, Vertical Output Amplifier and the interface circuits for all other vertical deflection sources. The other vertical deflection sources are character ramps, external Y Axis, sweep calibration, and internal options.

Delay Line Assembly, A10. The Delay Line Assembly has a differential impedance of approximately 125 ohms and provides a time delay of approximately 100 nanoseconds. This delay is sufficient to allow the internal sync signal to trigger the time base to start the horizontal sweep. Without this time delay in the signal path, the sweep would start after the signal reached the vertical deflection plates of the CRT and the leading edge of fast rise time signals would not be displayed.

Vertical Output Amplifier. The vertical signal from the delay line is input to the Vertical Output Amplifier, A1U11. Across the output of the delay line is a diode coupled LBFD (Low, Beam Find) signal. When the FIND BEAM key is pressed LBFD is low and will greatly decrease the Vertical signal amplitude to bring the signal on screen. Transistors A1Q14 and A1Q15 in the vertical signal path are switching devices. If the signal at the cathodes of A1CR35 and A1CR36 is low, transistors A1Q14 and A1Q15 will be cutoff and another signal source will be selected. The adjustments HF1, HF2, HF3, HF4, and HF5 are adjusted for best pulse shape. The vertical signal selected for display is amplified by A1U11 and goes to the vertical CRT deflection plates and to connectors for internal options.

External Vertical Signals and Interface. There are three other sources of vertical signals. The first of these is is Y Axis input from the rear panel. When a Y Axis input is desired, X-Y-Z scope mode must be selected. When external inputs are selected the signal HEXEN (High, External Enable) will be high from the processor control. When HEXEN is high a low is present at the junction of A1CR35 and A1CR36 disabling the channel 1 and 2 vertical input. HEXEN, through A1U10C will also enable A1Q16 and A1Q17 to gate the Y Axis input signal to the vertical output amplifier. The X-Y-Z. Mode is a special operating mode and the 1980 specifications should be checked for X, Y, and Z input requirements.

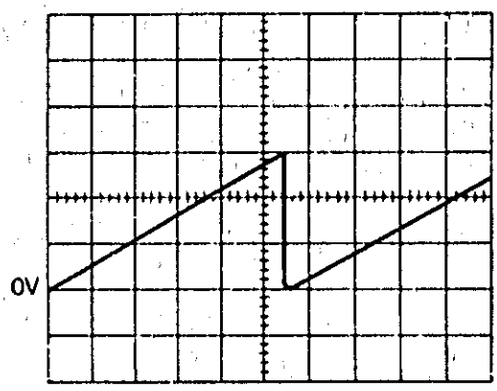
The second of the three signals is HDTE (High, Delayed Trigger Enable) which is gated to the vertical output amplifier by SWP CAL (Sweep Calibration). SWP CAL is used during the Front Panel Calibration routine.

The third of the gate circuits is A1Q22 and A1Q23 which is gated on by HCHEN (High, Character Enable). Two signals are gated through A1Q22 and A1Q23. The first of these signals is Y DISP from the Waveform Storage Option. The other signal is the vertical character ramp which is generated by A1Q21, A1U8, and A1Q61. When the signal HCHRV (High, Character Retrace Vertical) is high, A1Q61 will conduct placing a ground potential on the collector of A1Q21. After a character retrace interval, HCHRV goes low, which removes the ground from the collector of A1Q21 and will allow the capacitor A1C37 (at A1U8 pin 3) to charge through A1Q21, A1R83, and A1R84. At the output of A1U8 (pin 6) a positive going ramp voltage is produced until the HCHRV signal again goes high. The vertical character gain (ramp amplitude) is adjusted with A1R82 and the vertical character position is adjusted with A1R85.

(A)

Monitor Oscilloscope Setup

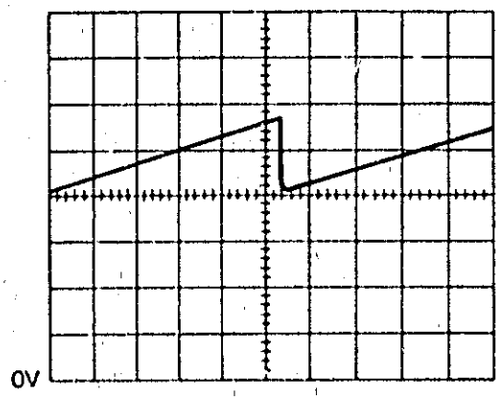
0.5 Volts/Div
2 mSec/Div



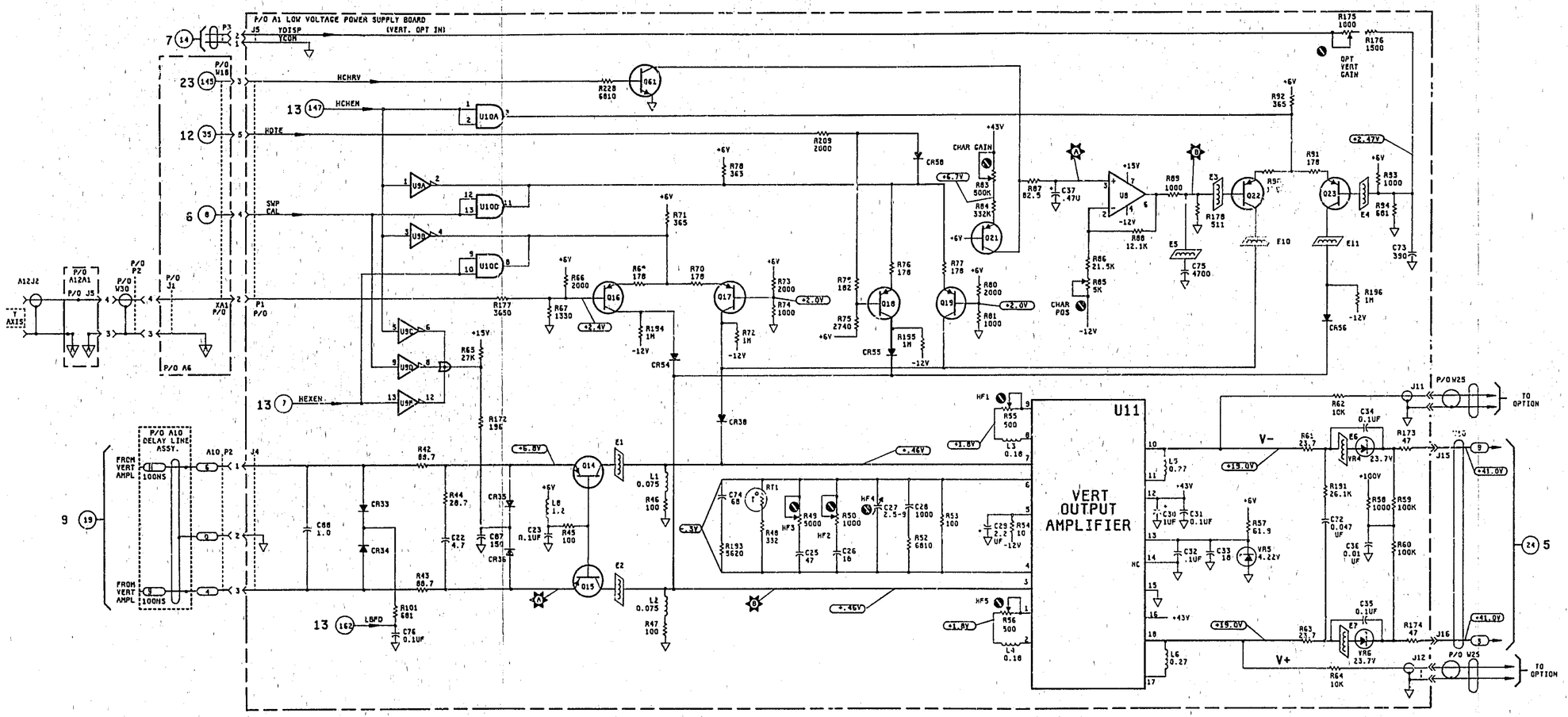
(B)

Monitor Oscilloscope Setup

0.5 Volts/Div
2 mSec/Div



Service Sheet 10. Test Information
P/O Low Voltage Power Supply Board, Vertical Output



IC DEVICE POWER CONNECTIONS

+5V — U9,10

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L

PARTS ON THIS SCHEMATIC

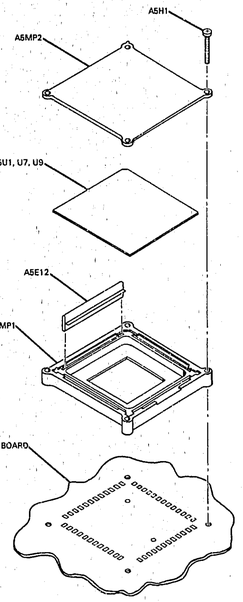
CHASSIS	P/O A1	P/O A6
P/O A10 P/O W18,25,26 P/O W10,30	C22,23,25-37 C72-76,87,88 CR33-36,38,54-56 CR58 E1-7 L1-6,8 P/O J4,5,11,12,15,16 Q14-19,21-23,61 R42-50,52-67,69-71,83-94,101 R172-176,191,193-196,209,228 RT1 U8-11 VR4-6 P/O P1	P/O XA1 J1 **P/O A12** J2 P/O A1J5

DELETED R82,55,020,C24,L7,CR37 R51,R68

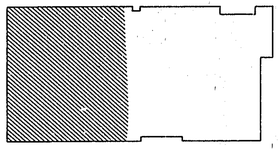
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10

Service Sheet 10. Schematic Diagram
P/O Low Voltage Power Supply Board, Vertical Output
8-105



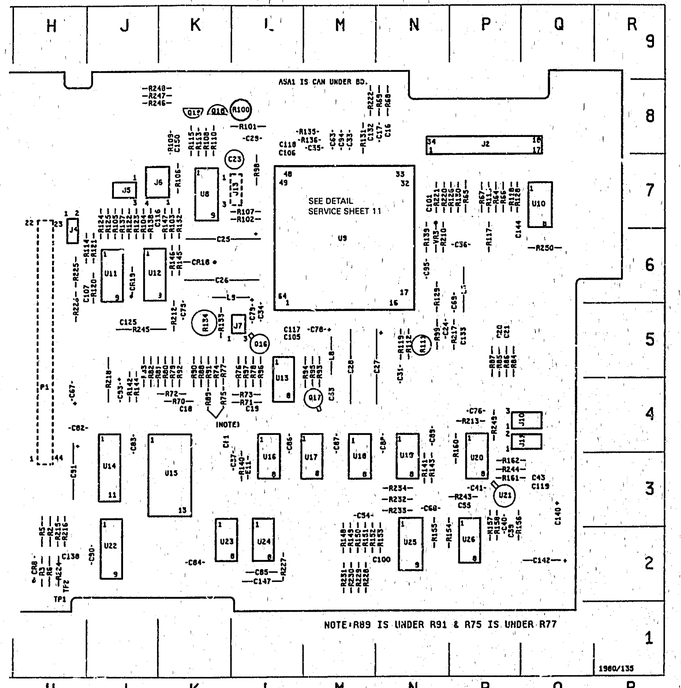
DETAIL OF HYBRID ASSEMBLY



A5 SCOPE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	L-9	C61	C-4	C118	L-8	E5	F-2	R2	H-2	R60	G-3	R116	P-7	R174	G-8	R232	N-3
C1	D-3	C62	M-2	C119	Q-3	E6	F-2	R3	H-2	R61	G-2	R117	P-6	R175	G-8	R233	N-3
C2	B-3	C63	M-8	C120	E-2	E7	C-6	R4	D-3	R62	G-3	R118	P-7	R176	D-8	R234	N-3
C3	B-2	C64	G-6	C121	C-2	E8	B-6	R5	H-2	R63	C-3	R119	N-5	R177	D-8	R235	B-5
C4	D-2	C65	G-6	C122	B-2	E9	B-6	R6	H-2	R64	P-7	R120	J-6	R178	D-8	R236	B-5
C5	C-4	C66	B-7	C123	C-1	E10	A-6	R7	E-2	R65	P-7	R121	J-6	R179	D-5	R237	C-5
C6	D-3	C67	H-4	C124	C-4	E11	L-3	R8	E-2	R66	P-7	R122	J-7	R180	B-5	R238	B-5
C7	B-3	C68	N-3	C125	J-5	J1	F-8	R9	E-2	R67	P-7	R123	J-7	R181	B-6	R239	B-4
C8	D-2	C69	N-6	C126	G-7	J2	P-8	R10	D-2	R68	N-9	R124	J-7	R182	D-5	R240	B-5
C9	E-3	C70	F-8	C127	G-7	J3	G-7	R11	D-3	R69	V-3	R125	J-7	R183	A-6	R241	B-5
C10	F-2	C71	C-4	C128	G-3	J4	H-7	R12	F-2	R70	K-4	R126	N-7	R184	B-6	R242	B-5
C11	F-3	C72	B-3	C129	G-3	J5	J-7	R13	D-2	R71	L-4	R128	P-7	R185	A-6	R243	P-3
C12	F-2	C73	B-5	C130	B-3	J6	J-7	R14	D-2	R72	K-4	R129	N-6	R186	A-6	R244	P-3
C13	F-3	C74	D-2	C131	M-8	J7	L-5	R15	F-2	R73	L-4	R130	P-7	R187	C-8	R245	J-5
C14	F-4	C75	K-5	C132	M-8	J8	F-3	R16	F-2	R74	K-5	R131	M-8	R189	E-7	R246	J-8
C15	G-3	C76	P-4	C133	P-5	J9	G-3	R17	F-2	R75	K-4	R132	K-7	R190	E-6	R247	J-8
C16	N-5	C77	F-7	C134	F-2	J10	P-4	R19	D-4	R76	L-5	R133	K-6	R191	D-7	R248	J-8
C17	M-8	C78	M-5	C138	H-2	J11	P-4	R20	D-4	R77	K-5	R134	K-5	R192	E-7	R249	P-4
C18	K-4	C79	L-5	C139	H-2	J12	P-5	R21	D-5	R78	L-5	R135	M-8	R193	E-6	R250	G-5
C19	L-4	C81	K-4	C140	Q-3	J13	L-7	R22	D-5	R79	K-5	R136	M-8	R194	F-6	R251	E-5
C20	P-5	C82	H-4	C141	G-2	L1	E-3	R23	D-5	R80	K-6	R137	J-7	R195	E-6	R252	E-4
C21	P-5	C83	J-4	C142	Q-3	L2	J-5	R24	D-5	R81	J-5	R138	J-7	R196	E-8	R255	G-5
C23	L-8	C84	K-2	C144	P-6	L3	G-6	R25	D-4	R82	J-5	R139	N-9	R197	E-8	R256	E-5
C24	N-5	C85	L-2	C145	F-2	L4	G-6	R27	D-2	R83	J-5	R140	L-3	R198	F-8	R7	E-4
C25	K-6	C86	L-4	C146	E-2	L6	P-6	R28	D-2	R84	P-5	R141	N-3	R199	E-8	TP1	H-2
C26	K-6	C87	M-4	C147	L-7	L7	G-4	R29	E-3	R85	P-5	R142	J-4	R200	D-8	TP2	H-2
C27	M-6	C88	N-4	C148	B-6	L8	M-5	R30	E-3	R86	P-5	R143	N-3	R201	E-8	U1	C-7
C28	M-5	C89	N-4	C149	H-5	L9	K-6	R31	E-3	R87	P-5	R144	J-4	R202	E-8	U2	E-8
C29	L-8	C90	J-2	C150	K-8	L10	E-6	R32	E-3	R88	K-5	R145	K-6	R203	E-8	U3	F-8
C31	N-5	C91	H-3	C151	D-3	L12	E-6	R33	E-4	R89	K-4	R146	K-6	H204	E-8	U4	E-7
C32	C-2	C92	J-3	C152	E-4	L13	G-5	R34	E-4	R90	K-5	R147	K-7	R205	D-7	U5	F-7
C33	M-8	C93	J-4	CR1	D-4	P1	H-4	R35	E-3	R91	K-5	R148	M-2	R206	D-7	U6	C-5
C34	L-5	C94	M-8	CR2	D-3	Q1	D-4	R36	E-3	R92	K-5	R149	M-2	R207	E-4	U7	C-3
C35	M-8	C95	D-4	CR3	D-4	Q2	D-4	R37	F-4	R93	M-5	R150	M-2	R208	E-4	U8	K-7
C36	P-6	C96	D-7	CR4	E-4	Q3	E-3	R38	F-2	R94	M-5	R151	M-2	R210	N-6	U9	M-6
C37	K-3	C97	B-7	CR5	E-3	Q4	E-4	R39	E-3	R95	M-5	R152	M-2	R211	B-4	U10	G-7
C39	P-2	C98	C-8	CR6	E-3	Q5	E-3	R40	F-2	R96	L-5	R153	N-2	R212	K-5	U11	J-6
C40	P-2	C99	C-8	CR7	G-3	Q6	F-3	R41	F-3	R97	L-5	R154	N-2	R213	K-5	U12	J-6
C41	P-3	C100	N-2	CR8	H-2	Q7	F-3	R42	F-3	R98	L-7	R155	N-2	R214	F-7	U13	L-5
C43	Q-3	C101	N-7	CR9	G-2	Q8	F-3	R43	F-3	R99	N-5	R156	P-2	R215	N-2	U14	J-3
C44	C-6	C102	C-5	CR10	C-5	Q9	F-3	R44	F-3	R100	L-8	R157	P-2	R216	J-4	U17	M-3
C45	B-7	C103	E-6	CR11	C-5	Q10	F-3	R45	F-3	R101	L-8	R158	P-2	R217	N-5	U16	L-3
C46	B-8	C104	E-6	CR12	B-5	Q11	F-4	R46	F-3	R102	L-7	R160	P-4	R218	J-4	U17	M-3
C47	L-8	C105	L-5	CR13	B-5	Q12	F-3	R47	F-4	R103	K-7	R161	P-3	R220	N-7	U18	M-3
C48	E-6	C106	L-8	CR14	B-5	Q13	F-3	R48	F-3	R104	J-7	R162	P-3	R221	N-7	U19	N-3
C49	F-7	C107	H-5	CR15	B-5	Q14	F-2	R49	F-3	R105	J-7	R163	D-5	R222	M-2	U20	P-3
C51	F-4	C108	G-4	CR16	A-5	Q15	F-2	R50	G-3	R106	K-7	R164	C-5	R223	H-2	U21	P-3
C52	E-4	C109	C-4	CR17	A-5	Q16	L-5	R51	G-3	R107	L-7	R165	C-6	R224	H-2	U22	J-2
C53	M-4	C110	C-2	CR18	K-6	Q17	M-4	R52	G-3	R108	K-8	R166	D-5	R225	H-5	U23	K-2
C54	M-3	C111	D-7	CR19	J-6	Q18	K-8	R53	G-2	R109	K-8	R167	B-5	R226	H-5	U24	L-2
C55	P-3	C112	D-8	CR20	D-3	Q19	K-8	R54	F-4	R110	K-8	R168	C-5	R227	L-2	U25	N-2
C56	G-6	C113	C-8	CR21	D-3	Q20	C-6	R55	F-3	R111	N-5	R169	B-6	R228	M-2	U26	P-2
C57	G-6	C114	B-8	E1	E-3	Q21	B-6	R56	F-3	R112	N-5	R170	C-6	R229	M-2	VR1	E-3
C58	E-2	C115	B-7	E2	E-3	Q22	B-6	R57	G-3	R113	K-8	R171	C-6	R230	M-2	VR2	E-3
C59	E-2	C116	J-7	E3	G-3	Q23	A-6	R58	G-3	R114	H-6	R173	H-8	R231	M-2	VR3	N-5
C60	D-2	C117	L-5	E4	G-3	R1	F-6	R59	G-3	R115	K-8						

A5



SERVICE SHEET 11 MNEMONICS

A	**Calibrator Bit Code A** — In conjunction with Bit Codes B and C determines calibrator amplitude.
ALT	**Alternate** — Used to alternate sweep between CH1 and CH2, CH1, CH2, CH3 and CH4, Main and Delayed in dual.
ALT CLK	**Alternate Clock** — Output of the horizontal microcircuit occuring at the end of each sweep.
B	**Calibrator Bit Code B** — In conjunction with Bit Codes A and C determines calibrator amplitude.
C	**Calibrator Bit Code C** — In conjunction with Bit Codes A and B determines calibrator amplitude.
CH1-CH4	**Channel Select Bits** — "Converted" to HCH1 through HCH4 in A5U14 - used to turn channels on via preamplifier.
CHOP CLK	**Chop Clock** — Derived from processor clock via DAC Refresh Controller — used to "sample" traces in chopped mode.
CH SUM	**Channel Sum** — Used to turn on multiple channels for algebraic summation.
GET	**Group Execute Trigger** — From HP-IB. Allows bus simulation of a FIND BEAM key closure.
H BLANK CLK	**High, Blanking Clock** — Wire-ored with HBLNK from the horizontal microcircuit — provides chopped blanking when trace is normally unblanked.
H CAL OFF	**High, Calibrator off** — Used to turn calibrator off when oscillator (CAL) is on.
HCH1	**High, Channel 1** — Bit to turn channel 1 on when desired.
HCH2	**High, Channel 2** — Bit to turn channel 2 on when desired.
HCH3	**High, Channel 3** — Bit to turn channel 3 on when desired.
HCH4	**High, Channel 4** — Bit to turn channel 4 on when desired.
HCRS	**Horizontal Counter Reset** — Signal from IO to sweep control circuit to reset counter when a sweep interrupt is requested.
HDTV	**High, Delayed Trigger View** — When activated allows delayed trigger signal to be applied to the vertical for viewing.
HINT	**High, Intensified** — Inverted and used to intensify main gate during delayed sweep period.
HMTV	**High, Main Trigger View** — When activated allows main trigger signal to be applied to vertical for viewing.
H OSC OFF	**High, Oscillator Off** — Low only during "Delay Time Cal" function in Front Panel calibration rountine.
HTDC	**High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.
L1 vs L2	**Low, 1 vs 2** — Derived in the sweep control circuits during 1 vs 2 mode to unblank beam and inhibit blanking by or generation of sweeps. Separate signal(s) activates proper amplifier paths.
LDSE	**Low, Delayed Sweep Enable** — Signal to horizontal microcircuit to output delayed sweep.
LMSE	**Low, Main Sweep Enable** — Signal to horizontal microcircuit to output main sweep.

Service Sheet 11, Component Locator
P/O Scope Board, Sweep Control Circuits

SERVICE SHEET 11 MNEMONICS (CONT'D)

LSEN	**Low, Separate Enable** — From horizontal control circuit during dual sweep mode to separate MAIN INTENSIFIED and DLY'D traces.
LTV	**Low, Trigger View** — Via the sweep control circuit when all channels are off, LTV allows trigger view — if MTV is high main trigger view results — if MTV is low delayed trigger view results.
MTV	**Main Trigger View** — When high main TV is selected — if low delayed TV is selected.
PCHC	**Pulse Clock Horizontel and Calibrator** — From IO port to sweep control to gate data for channel, sweep, or calibrator functions.
SB0	**Sweep Bit 0** — With SB1 determines the sweep mode in the sweep control circuits.
SB1	**Sweep Bit 1** — With SB0 determines the sweep mode in the sweep control circuits.
SDTA	**Serial Data** — Data string from IO to various shift registers that when clocked into the shift register strings initiates various functions, lamps, etc.
TFQ	**Timing Frequency** — LMSYNC signal divided by 2 to activate the calibrator switch and form calibrator square wave (~1.86 kHz).

SERVICE SHEET 11 — THEORY OF OPERATION

Service Sheet 11 contains the Horizontal Sweep Control circuits which select the correct sweep mode and produce the signals to gate the vertical signals and the calibrator circuits.

Processor Control. Processor control data is received by the shift register A5U15 on the SDTA (Serial Data) line. The serial data is shifted into A5U15 by PHCH (Pulse Clock Calibrator and Horizontal) and gated to the latched output by HTDC (High, Transfer Data Command). The processor control bits stored in locations 1 through 11 of the shift register are for control of the sweep functions and the data in locations 12 through 16 control the calibrator functions.

State Machine Operation. The programmed ROM, A5U14, the Adder, A5U23, and the Counter, A5U23, are connected as a state machine to control the displayed sweeps. The state machine receives major scope setups (horizontal mode, number of channels displayed, trigger views displayed, etc.) from the processor, through the serial to parallel interface A5U15. Once a setup has been made, the state machine repeats a sequence until another setup takes place.

The setup data addresses a region (high order address bits) of the ROMs memory. Programmed within the selected memory region is a number (7 – # of sweeps + 1) which represents the number of sweeps required for the selected operating mode. For example, if the one sweep is required, the memory contains 7; if four sweeps are required, the memory contains 4, and if eight sweeps are required, the memory contains 0. This number is availeble on the DO5, DO6, and DO7 outputs of the ROM, and get added (in A5U23) with LTV (low, Trigger View). If Trigger View is not selected (high), the result from the adder is the same as the input from the ROM. If Trigger View is selected (low), the result from the adder is the input number minus one.

The output of the adder is loaded into the counter, A5U22, with HCRS (Horizontal Counter Reset) at the time of the setup and when the counter is incremented to its terminal count. The clock input to the counter pin 2 will increment the output by one count with each input clock. As the counter is incremented, successive ROM addresses are selected to enable the next displayed trace. If operating in the DUAL mode, DO4 will be high during each main sweep and low during each delayed sweep and any holdoff time.

When the Counter reaches terminal count A5U22 pin 15 will go high to enable a parallel load of itself by placing a low at pin 9. When the next clock is input to the counter the parallel load will occor, removing rhe terminal count, and the counter will again begin incrementing. This sequence will repeat until another major setup takes place.

Following is a list of the signal conditions which are required tc develop the sweep control outputs.

HDTV — channels 1 - 4 must be off (HCH1 - HCH4, low), and
— Delayed trigger view must be selected (LTV, low; MTV, Low)

LSEN — any channel on or trigger view selected (HCH1, HCH2, HCH3, HCH4, or LTV, high), and
— sweep bit 0 must be low (INTEN or DUAL selected), and
— main sweep is not sweeping (LMSE is high)

HMTV — channels 1 - 4 must be off (HCH1 - HCH4, low), and
— main trigger view must be selected (LTV, low; MTV, high)

LMSE — SB1 high (MAIN or INTEN mode selected), or
— DO4 high (in DUAL and not sweeping Delayed or in holdoff), or
— SB0 and SB1 low and MTV high (in DUAL and MTV selected)

LDSE — not in 1 vs 2 mode (L1 vs 2 high), and
— SB1 low (in DUAL or Delayed mode), and
— DO4 low (not sweeping Main), and
— SB0 and SB1 low or MTV low (not in dual with Main trigger view enabled)

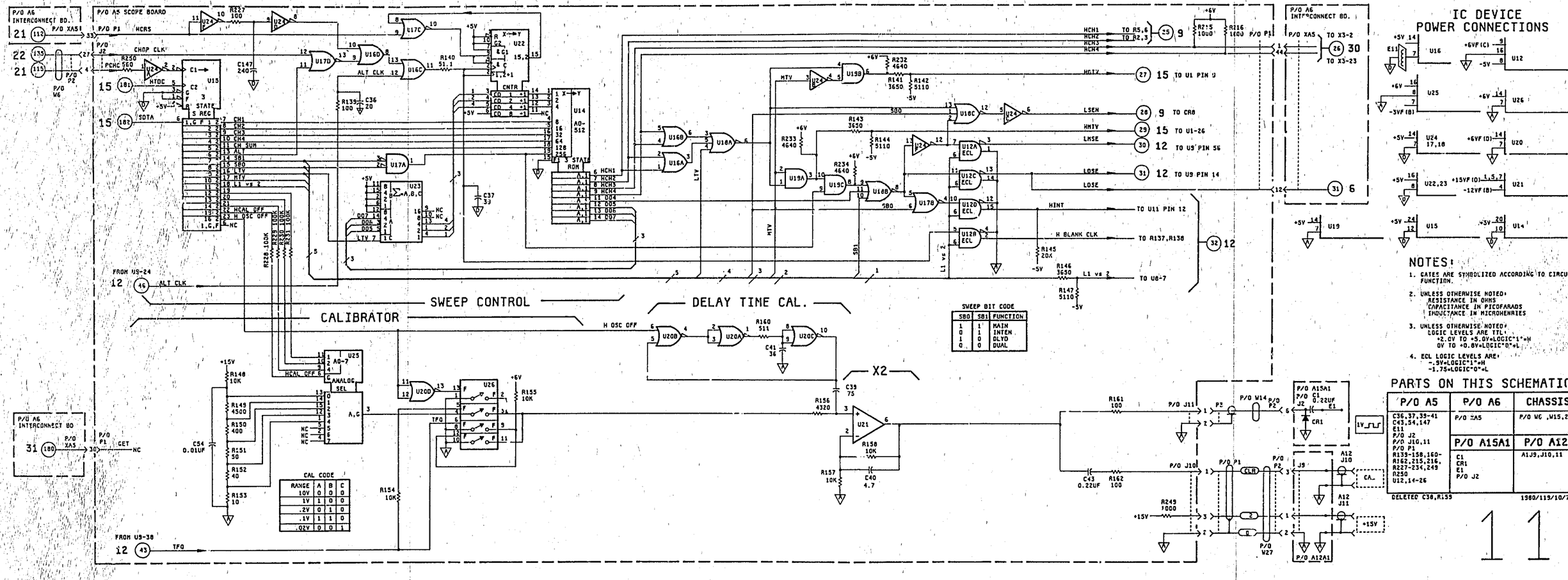
H BLANK CLK — not in 1 vs 2 mode (L1 vs 2 high), and
— ALT CLK or HCRS high, or
— ALT low and CHOP CLK low (not in alternate and chop clock is low)
HINT — not in 1 vs 2 mode (L1 vs 2 is high), and
— SBO low (in INTEN or DUAL), and
— LDSE high (not sweeping delayed sweep)

Calibrator Circuits. The calibrator contains a Selector, A5U25, a switching circuit, A5U26, and a Delay Time Calibrator Oscillator, A5U20A,B,C.

The selector, A5U25, is addressed from processor data by bits 12, 13, and 14 from the shift register, A5U15. The address bits into the analog selector will select one of the five inputs to be gated to the output. When HCAL OFF is high the output of the analog selector is available to the bilateral switch, A5U26. Each of the four switchs has its own control input and the switch is closed when the control input is high. The signal TFQ (Timing Frequency) is a symmetrical square wave which controls two sections of A5U26. When TFQ is high, A5U26 pin 4 is connected to pin 3 placing the selected analog level on the input of the X2 amplifier A5U21. With TFQ high pin 8 is connected to pin 9 placing a ground on the control input pin 12 to ensure pin 10 is not connected to pin 11. With TFQ low, pin 10 will be connected to pin 11 placing a ground on the input of the X2 amplifier, A5U21. In this manner a symmetrical square wave is produced. The amplitude of the calibrator output will be between the selected calibrator level and ground. The output of the X2 amplifier, A5U21, is ac coupled to both outputs.

Five calibrator levels are available from the Analog Selector A5U25. During normal operation, the selected output is a 1 V peak to peak calibrator signal. In the Front Panel Calibration routine 10 V, 1 V, 100 mV, and 20 mV are selected to aid in adjusting the Vertical Sensitivity. The four voltages above and 200 mV calibrator levels are available through the use of HP-IB commands.

The Delay Time Calibrator Oscillator will oscillate when HOSC OFF is low. The oscillating frequency is determined by A5C41 and A5R160. The frequency of this oscillator is relatively unimportant, it is only a convenient signal source for the Fine Delay Calibration. The Delay Time Oscillator is on only when in the Fine Delay Calibration routine.



IC DEVICE POWER CONNECTIONS

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. ECL LOGIC LEVELS ARE:
   -.9V=LOGIC"1"=H
   -1.75=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A5	P/O A6	CHASSIS
C36,37,39-41 C43,54,147 E11 P/O J2 P/O J10,11 P/O P1 R139-158,160- R162,215,216, R227-234,249 R250 U12,14-26	P/O XA5	P/O W6 ,W15,27
	P/O A15A1	P/O A12
	C1 CR1 E1 P/O J2	A1J9,J10,11

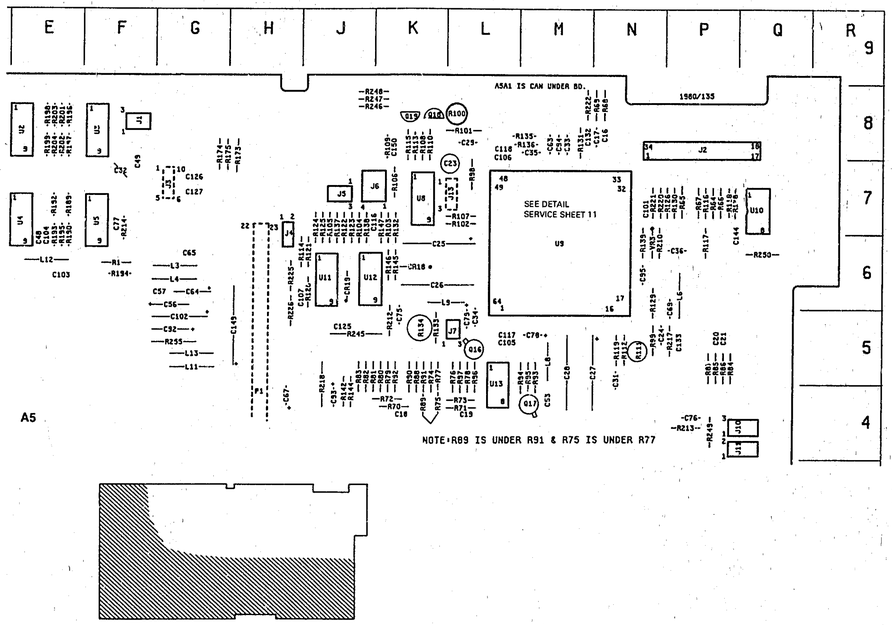
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A5 SCOPE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	L-9	C61	C-4	C118	L-6	E5	F-2	R2	H-2	R60	G-3	R116	P-7	R174	G-8	R232	N-3
C1	D-3	C62	B-3	C119	G-3	E6	F-2	R3	H-2	R61	G-3	R117	P-6	R175	G-8	R233	N-3
C2	B-3	C63	M-8	C120	E-2	E7	C-6	R4	D-3	R62	G-3	R118	P-7	R176	D-8	R234	N-3
C3	B-2	C64	G-6	C121	C-2	E8	B-6	R5	H-2	R63	G-3	R119	N-6	R177	D-8	R235	B-5
C4	D-2	C65	G-6	C122	B-2	E9	B-6	R6	H-2	R64	P-7	R120	J-6	R178	D-8	R236	C-5
C5	C-4	C66	B-7	C123	B-4	E10	A-6	R7	E-2	R65	P-7	R121	J-6	R179	D-5	R237	C-5
C6	D-3	C67	H-4	C124	C-4	E11	L-3	R8	E-2	R66	P-7	R122	J-7	R180	B-5	R238	B-5
C7	B-2	C68	N-3	C125	J-5	J1	F-8	R9	E-2	R67	P-7	R123	J-7	R181	B-6	R239	B-4
C8	D-2	C69	N-6	C126	G-7	J2	P-8	R10	D-2	R68	N-8	R124	J-7	R182	D-5	R240	B-5
C9	E-3	C70	F-5	C127	G-7	J3	G-7	R11	D-3	R69	M-8	R125	J-7	R183	A-5	R241	B-5
C10	F-2	C71	C-4	C128	G-3	J4	H-7	R12	F-2	R70	K-4	R126	N-7	R181	B-6	R242	B-5
C11	F-3	C72	B-3	C129	G-3	J5	J-7	R13	D-2	R71	L-4	R128	P-7	R184	B-6	R243	P-3
C12	F-2	C73	B-5	C130	B-3	J6	J-7	R14	D-2	R72	K-4	R129	N-6	R186	A-6	R244	P-3
C13	F-3	C74	D-2	C131	C-8	J7	L-5	R15	F-2	R73	L-4	R130	P-7	R187	C-8	R245	J-6
C14	F-4	C75	K-5	C132	M-8	J8	F-3	R16	F-2	R74	K-5	R131	M-8	R189	E-7	R246	J-8
C15	G-3	C76	P-4	C133	P-5	J9	G-3	R17	F-2	R75	K-4	R132	K-7	R190	E-6	R247	J-8
C16	N-8	C77	F-7	C134	C-2	J10	P-4	R18	D-4	R76	L-5	R133	K-5	R191	D-7	R248	J-8
C17	M-8	C78	M-6	C138	H-2	J11	P-4	R20	D-4	R77	K-5	R134	K-5	R192	E-7	R249	P-4
C18	K-4	C79	L-5	C140	H-3	J12	D-6	R21	D-5	R78	L-5	R135	M-8	R193	E-6	R250	Q-6
C19	L-4	C81	K-4	C140	G-3	J13	L-7	R22	D-5	R79	K-5	R136	M-8	R194	F-6	R251	E-6
C20	P-5	C82	H-4	C141	G-2	L1	E-3	R23	D-6	R80	K-5	R137	J-7	R195	E-6	R252	E-4
C21	P-5	C83	J-4	C142	D-2	L2	G-4	R24	D-6	R81	J-5	R138	J-7	R196	E-6	R255	G-5
C22	L-8	C84	-2	C144	P-6	L3	G-6	R25	D-4	R82	J-5	R139	N-8	R197	E-8	R256	E-5
C24	K-5	C85	L-2	C145	F-2	L4	G-6	R27	D-2	R83	J-5	R140	L-3	R198	E-8	RT1	E-4
C26	K-6	C86	L-4	C146	E-2	L6	P-6	R28	D-2	R84	P-5	R141	N-3	R199	E-8	TP1	H-2
C2E	K-6	C87	M-4	C147	L-2	L7	G-4	R29	E-3	R85	P-5	R142	J-4	R200	D-8	TP2	H-2
C27	M-5	C88	N-4	C148	B-6	L8	M-6	R30	E-3	R86	P-5	R143	N-3	R201	E-8	U1	C-7
C28	M-5	C89	N-4	C149	H-5	L9	K-6	R31	E-3	R87	P-5	R144	J-4	R202	E-8	U2	E-8
C29	L-8	C90	J-2	C150	K-8	L11	G-5	R32	E-3	R84	K-5	R145	K-6	R203	E-8	U3	F-8
C31	N-6	C91	H-3	C151	D-3	L12	E-6	R33	E-4	R89	K-4	R146	K-6	*204	E-8	U4	E-7
C32	F-8	C92	G-6	C152	E-4	L13	G-5	R34	E-3	R90	K-5	R147	K-7	A205	D-7	U5	F-7
C33	M-8	C93	J-4	CR1	D-4	P1	H-4	R35	E-3	R91	K-5	R148	M-2	R206	D-7	U6	C-6
C34	L-5	C94	M-8	CR2	D-3	Q1	D-4	R36	E-3	R92	K-5	R149	M-2	R207	E-4	U7	C-3
C35	M-8	C95	N-6	CR3	D-4	Q2	D-4	R37	E-4	R93	M-5	R150	M-2	R208	E-4	U8	K-7
C36	P-6	C96	D-7	CR4	E-4	Q3	E-3	R38	F-2	R94	M-5	R151	M-2	R210	N-6	U9	M-6
C37	K-3	C97	B-7	CR5	E-3	Q4	E-4	R39	E-3	R95	M-5	R152	M-2	R211	B-4	U10	O7
C39	P-2	C98	C-8	CR6	E-3	Q5	E-3	R40	F-2	R96	L-5	R153	N-2	R212	K-5	U11	J-6
C40	P-2	C99	C-8	CR7	G-3	Q6	F-3	R41	F-3	R97	L-5	R154	N-2	R213	P-4	U12	J-6
C41	P-2	C100	N-2	CR8	H-2	Q7	F-3	R42	F-3	R98	L-7	R155	N-2	R214	F-6	U13	L-5
C43	Q-3	C101	N-7	CR9	G-2	Q8	F-3	R43	F-3	R99	N-5	R156	P-2	R215	H-2	U14	J-3
C44	C-6	C102	Q-5	CR10	C-5	Q9	F-3	R44	F-3	R100	L-8	R157	P-2	R216	H-2	U15	K-3
C45	B-7	C103	E-6	CR11	C-5	Q10	F-3	R45	F-3	R101	L-8	R158	P-2	R217	N-5	U16	L-3
C46	B-8	C104	E-6	CR12	B-5	Q11	F-4	R46	F-3	R102	L-7	R160	P-4	R218	J-4	U17	M-3
C47	D-8	C105	L-5	CR13	B-6	Q12	F-3	R47	F-4	R103	K-7	R161	P-3	R220	N-7	U18	M-3
C48	E-6	C106	L-8	CR14	B-6	Q13	F-3	R48	F-3	R104	J-7	R162	P-3	R221	N-7	U19	N-3
C49	F-7	C107	H-6	CR15	B-5	Q14	F-2	R49	F-3	R106	J-7	R163	D-5	R222	M-8	U20	P-3
C51	F-4	C108	G-4	CR16	A-5	Q15	F-2	R50	G-3	R106	K-7	R164	C-5	R223	H-2	U21	P-3
C52	E-4	C109	C-4	CR17	A-5	Q16	L-6	R51	G-3	R107	L-7	R165	C-6	R224	H-2	U22	J-2
C53	M-4	C110	C-2	CR18	K-6	Q17	M-4	R52	G-3	R108	K-8	R166	D-5	R226	H-5	U23	K-2
C54	M-3	C111	D-7	CR19	J-6	Q18	K-8	R53	G-2	R109	K-8	R167	B-5	R226	H-5	U24	L-2
C55	P-3	C112	D-8	CR20	D-3	Q19	K-8	R54	F-4	R110	K-8	R168	C-6	R227	L-2	U25	N-2
C56	G-6	C113	C-8	CR21	D-3	Q20	C-8	R55	F-3	R111	N-5	R169	B-6	R228	M-2	U26	P-2
C57	G-6	C114	B-8	E1	E-3	Q21	B-5	R56	F-3	R112	N-5	R170	C-4	R229	M-2	VR1	E-3
C58	E-2	C115	B-7	E2	E-3	Q22	B-6	R57	G-3	R113	K-8	R171	C-6	R230	M-2	VR2	E-3
C59	E-2	C116	J-7	E3	G-3	Q23	A-6	R58	G-3	R114	H-6	R173	H-8	R231	M-2	VR3	N-6
C60	D-2	C117	L-6	E4	G-3	R1	F-6	R59	G-3	R115	K-8						



SERVICE SHEET 12 MNEMONICS

ALT CLK	**Alternate Clock** — Output of the horizontal microcircuit occuring at the end of each sweep.
BCD1	56-bit serial data from microprocessor to horizontal microcircuit with sweep instructions.
BCD2	56-bit serial data from horizontal microcircuit to microprocessor used to effect VCO frequency control.
BCD IN/OUT	Bidirectional line to and from horizontal microcircuit.
HBLNX	**High, Blank** — Unblanks CRT for trace and blanks during retrace and holdoff.
H BLNK CLK	**High, Blanking Clock** — Wire-ored with HBLNK from horizontal microcircuit - provides chopped blanking when trace is normally unblanked.
HDCLK	**High, Delayed Clock** — Signal from delayed trigger output used by the horizontal microcircuit to count events to digitally delay delayed sweep.
HDIC	**High, Display Inhibit Control** — Signal to processor IO signifying single sweep is complete, horizontal awaits reset.
HDIM1, HDIM2, HDIM4	**High, Delayed Intensity Modifier Bits** — Output from horizontal microcircuit to gate circuit where they are used during delayed and dual to modify delayed sweep intensity levels comparative to main sweep speeds in an attempt to maintain relatively even intensity regardless of sweep speeds.
HDNT	**High, Delayed Not Triggered** — Signal to light "NOT TRGD" lamp denoting delayed sweep is not triggered. Not active when delayed is in auto.
HDSG	**High, Delayed Sweep Gate** — From horizontal microcircuit during delayed ramp time — available for option enhancement module, and rear panel output.
HDST	**High, Delayed Sweep Trigger** — Generated by trigger circuit to start delayed sweep in the triggered mode.
HDTE	**High, Delayed Trigger Enable** — Generated at end of main sweep and applied to trigger circuit to allow HDST to be generated when desired.
HINT	**High, Intensified** — Inverted and used to intensify main gate during delayed sweep period.
HMCLK	**High, Main Clock** — Trigger signal output of main trigger microcircuit — used by horizontal microcircuit to RESET the auto sweep timer.
HMNT	**High, Main Not Triggered** — Derived from horizontal when main sweep is not triggered (both normal and auto) - used to light main "NOT TRGD" lamp.
HMSG	**High, Main Sweep Gate** — From horizontal microcircuit during main sweep ramp time — available for option, enhancement module, and rear panel output.
HMST	**High, Main Sweep Trigger** — Generated by trigger microcircuit to start main sweep in triggered mode.
HMTE	**High, Main Trigger Enable** — From horizontal microcircuit to main trigger circuit signifying main sweep is ready to accept a trigger - after holdoff.
HSYNC	**Horizontal Sync** — From processor horizontal interface to horizontal microcircuit to synchronize processor/horizontal state changes.
IS	**Instruction String** — A 10 bit serial data string sent to the horizontal microcircuit to denote that a state change instruction is to follow.

Service Sheet 12, Component Locator
P/O Scope Board, Horizontal Sweep Circuits

SERVICE SHEET 12 MNEMONICS (CONT'D)

L1 vs L2	**Low, 1 vs 2** — Derived in the sweep control circuits during 1 vs 2 mode to unblank beam and inhibit blanking by or generation of sweeps. Separate signal(s) activates proper amplifier paths.
LDSE	**Low, Delayed Sweep Enable** — Signal to horizontal microcircuit to output delayed sweep.
LFLG	**Low, Flag** — Output from horizontal microcircuit to an IO port signifying to the processor that a main sweep trigger was initiated during the delayed sweep ramp — used in the auto scope routine and available to HP-IB.
LINT	**Low, Intensified** — Complement of HINT sent to the Gate amplifier to intensity main gate during delayed ramp time.
LMSE	**Low, Main Sweep Enable** — Signal to horizontal microcircuit to output main sweep.
LMSYNC	**Low, Master Sync** — Derived from processor clock by the DRC to synchronize data transfer to the DAC, and used by the horizontal microcircuit to synchronize its operation.
PH1 CLK	**Phase 1 Clock** — Processor clock divided by eight — from the DRC to the DAC and horizontal microcircuit.
PH2 CLK	**Phase 2 Clock** — Processor clock divided by eight from the DRC to the DAC and horizontal microcircuit — displaced from PH1 CLK by two processor clock periods.
TFQ	**Timing Frequency** — LMSYNC signal divided by 2 to activate the calibrator switch and form calibrator square wave (~1.86 kHz).

SERVICE SHEET 12 — THEORY OF OPERATION

Service Sheet 12 contains the horizontal sweep circuits. Most of the circuitry for the horizontal sweep and interface is contained within the horizontal microcircuit, A5U9. The horizontal microcircuit contains three separate chips inside the single package. The horizontal microcircuit produces the sweep ramps, receives command data from the microprocessor, produces the sweep gate, and timing signals for use by other circuits.

Horizontal Instructions. The horizontal microcircuit, A5U9, receives processor control data on a bidirectional serial data line, BCD IN/OUT, and sends data to the processor circuits on the same line. BCD1 is serial data from the processor to the horizontal microcircuit and BCD2 is data from the horizontal microcircuit to the processor horizontal interface circuits shown on service sheet 24. The BCD data string to or from the horizontal microcircuit is a 56 bit string.

The IS (Instruction String) signal is a serial data string 10 bits in length with the first two bits of the string being 0s. The instruction string contains the commands for the horizontal microcircuit. The instructon string data commands the horizontal microcircuit to read new data, output data, and how to use the data input. LMSYNC (Low, Master Sync), PH1 CLK (Phase 1 Clock), and PH2 CLK (Phase 2 Clock) are timing signals from the DAC Refresh Controller. LMSYNC occors after the IS string and before the BCD string and is to syncronize the horizontal microcircuit with the processor horizontal interface for proper data communication. The PH1 CLK and PH2 CLK are used for data transmission and data shift clocks.

Main Sweep. In order for the horizontal microcircuit to output a main sweep, LMSE (Low, Main Sweep Enable) must be low from the sweep control circuits on service sheet 11. The horizontal microcircuit also produces the signal HMTE (High, Main Trigger Enable) on A5U9 pin 18. At this time the main trigger circuits will be armed and waiting for a vertical, external, or auto trigger to produce the trigger pulse. When the trigger pulse is produced, the signal HMST (High, Main Sweep Trigger) is produced by the trigger microcircuit and is input to the horizontal microcircuit on pin 16. HMST is required by the horizontal microcircuit to produce a HMSG (High, Main Sweep Gate) output to the rear panel and enhancement module. HMSG will also start the main sweep ramp generator. The MSG output is adjusted by A5R100. The Main Sweep Gate is adjusted for enough width to see the entire sweep and not the retrace. At the end of the main sweep ramp a delayed sweep will be produced and another main sweep cannot be generated until the delayed cycle has been completed.

Delayed Sweep. In order for the horizontal microcircuit to output a delayed sweep, LDSE (Low, Delayed Sweep Enable) must be low from the sweep control circuits on service sheet 11. The horizontal microcircuit also produces the signal HDTE (High, Delayed Trigger Enable) on A5U9 pin 52. At this time the delayed trigger circuits will be armed and waiting for a vertical, external or auto trigger to produce the trigger pulse. When the trigger pulse is produced, the signal HDST (High, Delayed Sweep Trigger) is produced by the trigger microcircuit and is input to the horizontal microcircuit on pin 53. HDST is required by the horizontal microcircuit to produce a HDSG (High, Delayed Sweep Gate) output to the rear panel and enhancement module. HDSG will also start the delayed sweep ramp generator. The DSG output is adjusted by A5R111. The Delayed Sweep Gate is adjusted for enough width to see the delayed sweep ramp and not the retrace.

Sweep Ramp Generators. Each of the sweep ramp generators (main and delayed) contain four ramp capacitors which are selected for different ranges. One of the capacitors is switched across the current source inputs by the sweep range select bits contained in the BCD data string. The sweep capacitors for the two slowest sweep ranges (A5C25,A5C26 for main and A5C27, A5C28 for delayed) are external to the horizontal microcircuit and the other two are internal to the horizontal microcircuit. The selected ramp capacitor is charged by the ramp current source to produce a main or delayed horizontal ramp voltage at pins 63 and 64. The ramp voltage is amplified (service sheet 13) and applied to the CRT horizontal deflecton plates. SWP ST (Sweep Start), A5R133, is adjusted for Main and Delayed sweeps to start at the same time

Each of the ramp current sources is controlled by an input voltage from the microprocessor DAC The DAC voltage is determined by the sweep calibration factors and the setting of the sweep time from the front panel Control Knob.

VCO Control. The VCO is a startable (with MSG) 10 MHz oscillator inside the horizontal microcircuit used for delay time measurements. The frequency determining components for the VCO are A5A1L1 and A5A1C1 which are mounted on a small Printed circuit board inside the shield on the back of the A5 board. The VCO frequency is manually adjusted with A5C23 and adjusted by the microprocessor with the VCO Control input on A5U9 pin 46. VCO control is a processor DAC voltage. When in VCO Calibration mode the frequency of the VCO is compared to the processor crystal clock frequency and the VCO is adjusted by the microprocessor until the frequencies are the same.

Miscellaneous Outputs. HDIM 1, HDIM 2, HDIM 4 (High, Delayed Intensity Modifier) bits adjust the displayed intensity level of the delayed sweep. Intensity is varied to create a visable display at all main and delayed sweep speeds. Activity on these lines is an indication that most of the horizontal microcircuit is functioning.

HMNT (High, Main Not Triggered) is the signal that illuminates the "NOT" lamp in Main Not Triggered display. Lamp is on if HMNT is high.

HDNT (High Delayed Not Triggered) is the signal that illuminates the "NOT" lamp in the Delayed Not Triggered display. Lamp is on if HDNT signal is high. HDNT is high when HDTE is high and HDSG(3) has not gone high indicating trigger circuit is armed but a trigger has not been produced.

LFLG (Low, Flag) is a signal which indicates if a triggered occurred during the delayed sweep gate. Used in Autoscope mode and available to HP-IB.

HDIC (High, Display Inhibit Control) is active at the end of the sweep in single sweep mode.

ALT CLK (Alternate Clock) is active at the end of each sweep and is used to clock the sweep control counter after each sweep has been completed.

TFQ (Timing Frequency) is a symmerical square wave of approximately 1.86kHz, used to produce the calibrator output square wave. TFQ is LMSYNC divided by two.

HBLNK (High, Blank) is used by the gate circuits to blank the sweep during horizontal retrace. HBLNK is "wire-ored" with H BLANK CLK to blank the chop switching transient.

LINT (Low Intensified) is used in the gate circuits to enable the intensified portion of the sweep.

Ⓐ

Range -0 VDC To -16VDC

TYPICAL READING — -3 VDC To -9 VDC

Reading is calibration factor dependent. Readings are end points measured as function (Main Ramp) is varied.

Ⓑ

Range -0 VDC To -9VDC

TYPICAL READING — -3 VDC To -9 VDC

Reading is calibration factor dependent. Readings are end points measured as function (Delayed Ramp) is varied.

Ⓒ

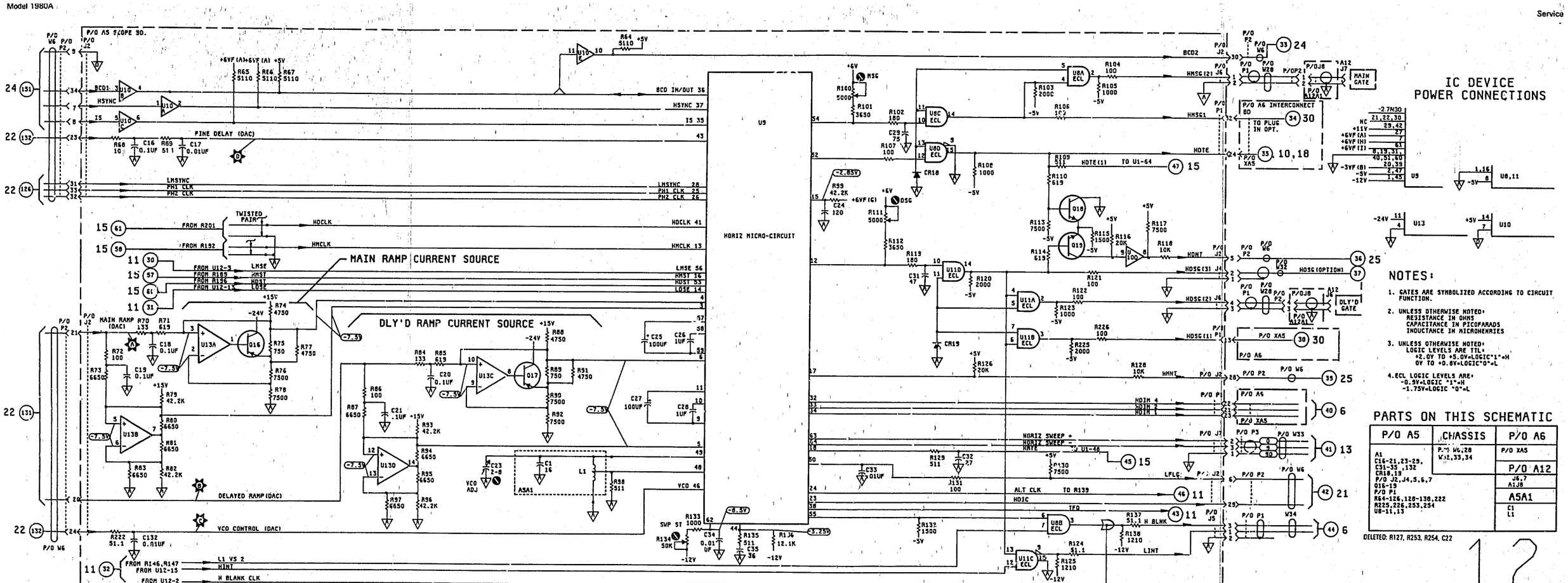
0 VDC To +4 VDC (typically +1.6 VDC)

Ⓓ

Range -0 VDC To +4 VDC

TYPICAL READING — +0.22 VDC To +3 VDC

Reading is calibration factor dependent. Readings are end points measured as function (Fine Delay) is varied.

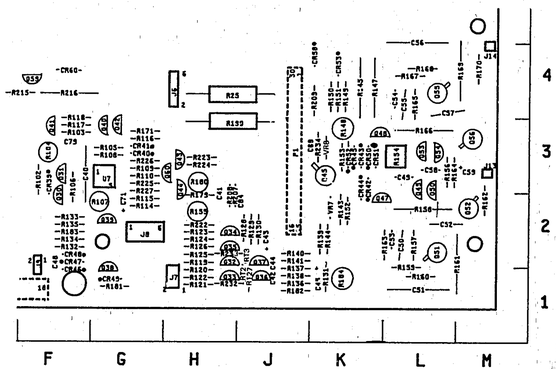


12

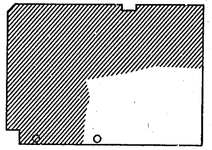
Service Sheet 12. Schematic Diagram
P/O Scope Board, Horizontal Sweep Circuits

A1 LVPS BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	E-2	C51	L-1	CR8	C-6	CR55	H-6	L3	J-8	Q47	K-2	R29	D-7	R76	H-5	R128	J-2	R172	H-7	R221	C-8
C2	D-2	C52	L-2	CR9	C-7	CR56	H-5	L4	J-6	Q48	K-3	R30	D-6	R78	H-5	R129	J-2	R173	L-7	R222	H-2
C3	D-3	C53	L-2	CR11	C-7	CR57	E-7	L5	K-7	Q49	L-3	R31	E-6	R77	J-5	R130	J-2	R174	L-7	R223	H-3
C4	B-7	C54	L-4	CR12	B-6	CR58	J-4	L6	K-7	Q50	L-3	R32	E-6	R76	J-5	R131	K-1	R175	G-6	R224	H-3
C5	C-6	C55	L-4	CR13	C-6	CR59	C-8	L8	G-7	Q51	L-2	R33	C-2	R79	H-5	R132	F-2	R176	H-5	R225	G-3
C6	B-5	C56	L-5	CR14	C-6	CR60	F-4	P1	J-3	Q52	M-2	R34	C-2	R80	J-6	R133	F-2	R177	H-5	R226	G-3
C7	D-5	C57	L-4	CR16	C-7	E1	J-7	Q1	E-3	Q53	L-3	R35	E-6	R81	J-6	R134	F-2	R178	J-6	R227	G-3
C8	C-7	C58	L-3	CR16	G-6	E2	J-7	Q2	D-2	Q54	L-3	R36	E-6	R83	K-5	R135	F-2	R179	H-2	R228	L-5
C9	E-3	C59	M-3	CR17	G-6	E3	J-6	Q3	B-7	Q55	L-4	R37	E-7	R84	K-5	R136	J-1	R180	H-3	R229	E-8
C10	D-6	C61	C-4	CR18	G-6	E4	J-6	Q4	B-7	Q56	M-3	R38	E-7	R85	L-5	R137	J-1	R181	G-1	R230	E-8
C11	G-5	C62	D-2	CR19	G-6	E5	K-5	Q5	B-6	Q57	F-8	R39	F-7	R86	K-5	R138	J-1	R182	J-1	R231	K-8
C12	G-5	C63	E-3	CR20	G-6	E6	L-7	Q6	B-7	Q58	F-8	R40	F-7	R87	L-5	R139	K-2	R183	F-7	R232	H-1
C14	E-6	C64	E-4	CR22	D-2	E7	L-7	Q7	C-7	Q59	F-4	R42	H-7	R88	K-5	R140	J-2	R184	K-1	R233	H-2
C15	H-7	C65	B-3	CR23	D-3	E10	J-6	Q8	C-7	Q60	G-3	R43	H-7	R89	J-5	R141	J-2	R188	E-7	R234	K-3
C16	F-7	C66	B-3	CR24	E-3	E11	J-6	Q9	C-7	Q61	L-5	R44	H-7	R90	J-5	R142	K-2	R187	D-7	RT1	H-8
C17	F-6	C67	C-3	CR25	F-7	F1	B-2	Q10	C-7	R1	E-2	R45	H-7	R91	J-5	R144	K-2	R190	H-3	RT2	J-1
C18	F-5	C68	D-8	CR26	E-7	F2	C-2	Q11	D-7	R2	D-2	R46	H-8	R92	J-5	R145	K-4	R191	L-7	RT3	J-2
C19	F-6	C69	B-3	CR27	E-6	F3	C-2	Q12	D-7	R3	D-2	R47	J-6	R93	J-5	R147	K-4	R193	L-7	RT4	C-2
C20	F-5	C70	E-2	CR29	F-6	F4	D-2	Q14	H-7	R4	D-6	R48	H-8	R94	J-5	R148	K-3	R194	H-6	TP1	E-8
C22	H-7	C71	G-2	CR30	F-6	F5	E-2	Q15	H-7	R6	D-6	R50	J-8	R101	H-7	R149	K-4	R195	H-6	TP2	C-8
C23	H-7	C72	L-7	CR31	F-6	F6	E-2	Q16	H-6	R6	D-7	R50	J-7	R102	F-3	R150	K-4	R196	H-6	TP3	C-8
C25	J-7	C73	K-6	CR32	F-6	F7	E-2	Q17	H-6	R7	D-6	R52	J-7	R103	F-3	R151	K-4	R198	D-7	U1	D-5
C26	J-7	C74	J-7	CR33	H-7	F8	E-2	Q18	H-6	R8	D-7	R53	J-7	R104	F-3	R152	K-2	R199	D-7	U2	D-6
C27	J-7	C75	K-6	CR34	H-7	F9	E-2	Q19	H-6	R9	D-7	R54	J-6	R105	G-3	R153	K-3	R200	D-8	U3	D-5
C28	J-7	C76	L-6	CR35	H-7	J1	D-1	Q21	K-5	R10	B-5	R55	J-8	R106	F-3	R154	L-3	R201	E-8	U4	E-5
C29	K-6	C77	D-5	CR36	H-7	J2	B-5	Q22	J-6	R11	B-6	R56	J-6	R107	G-2	R155	H-2	R204	E-7	U5	E-6
C30	L-6	C78	C-8	CR38	H-7	J3	B-8	Q23	J-6	R12	B-6	R57	L-6	R108	G-3	R156	L-3	R205	E-8	U6	F-6
C31	L-7	C79	F-3	CR39	F-3	J4	H-7	Q30	F-2	R13	B-6	R58	M-6	R109	G-3	R157	L-2	R206	F-7	U7	G-3
C32	L-7	C81	F-8	CR40	G-3	J5	H-8	Q31	F-3	R14	B-5	R59	L-7	R110	G-3	R158	L-2	R207	H-2	U8	K-5
C33	K-7	C82	E-8	CR41	G-3	J6	G-4	Q32	H-2	R15	B-7	R60	L-7	R114	G-2	R159	L-1	R208	H-2	U9	H-8
C34	L-7	C83	E-7	CR42	K-3	J7	H-1	Q33	H-1	R16	B-7	R61	L-7	R115	G-2	R160	L-1	R209	J-4	U10	J-5
C35	L-7	C84	H-2	CR43	K-3	J8	G-2	Q34	H-2	R17	C-7	R62	L-8	R116	G-3	R161	M-2	R210	D-8	U11	K-7
C36	M-6	C85	C-8	CR44	K-3	J9	F-2	Q35	H-2	R18	C-6	R63	L-7	R117	F-3	R162	M-2	R211	E-8	U12	D-8
C37	K-6	C86	C-8	CR45	K-3	J10	C-3	Q36	J-1	R19	C-6	R64	L-7	R118	F-3	R163	K-2	R212	F-8	VR1	C-2
C40	F-3	C87	H-6	CR46	F-1	J11	M-8	Q37	J-2	R20	C-6	R65	H-7	R119	H-2	R164	L-3	R213	F-8	VR2	C-2
C41	H-2	C88	G-7	CR47	F-2	J12	M-7	Q38	G-1	R21	C-6	R66	H-5	R120	H-1	R165	L-4	R214	E-8	VR3	D-6
C42	J-1	C89	J-3	CR48	F-2	J13	M-3	Q39	G-2	R22	C-6	R67	H-6	R121	H-1	R166	L-3	R215	E-4	VR4	L-7
C43	J-2	C92	C-3	CR49	G-1	J14	M-4	Q41	G-3	R23	C-7	R69	H-5	R122	H-1	R167	L-4	R216	F-4	VR5	L-7
C44	J-2	CR3	B-3	CR50	K-3	J15	M-7	Q41	F-3	R24	C-7	R70	H-5	R123	H-2	R168	L-4	R217	D-8	VR6	L-7
C45	K-1	CR4	C-3	CR51	K-3	J16	M-7	Q42	G-3	R25	H-4	R71	H-5	R124	H-2	R169	L-4	R218	D-8	VR7	K-2
C46	F-2	CR5	B-2	CR52	K-3	J17	L-8	Q43	H-3	R26	D-7	R72	H-6	R125	H-2	R170	M-4	R219	D-8	VR8	K-3
C49	L-3	CR6	B-2	CR53	K-4	L1	H-8	Q44	H-3	R27	D-7	R73	H-5	R126	H-2	R171	G-3	R220	C-8	XA7	D-5
C50	L-2	CR7	B-3	CR54	H-6	L2	J-7	Q45	K-3	R28	E-7	R74	H-6	R127	J-1						



A1



SERVICE SHEET 13 MNEMONICS

HCHEN — **High, Character Enable** — Signal which activates character ramps in vertical and horizontal outputs while also enabling gate circuit to receive Z-axis unblanking.

HCHRH — **High, Character Reset Horizontal** — Signal from video controller that activates and synchronizes the horizontal character ramp.

HEXEN — **High, External Enable** — Exerted high when external X, Y, and Z inputs are to be usad for deflection and blanking of beam.

HORIZ POS — **Horizontal Position** — Analog voltage from DAC to position traces horizontally - does not control spot in 1vs2 mode.

LBFD — **Low, Beam Find** — When front panel "FIND BEAM" key is pressed, line is grounded to override intensity to obtain a viewable trace while decreasing vertical and horizontal gain to bring presentation on screen.

XCOM — **X Input Common** — Ground on X input from option.

XDISP — **X Display Input** — Output of option to horizontal output for display.

Service Sheet 13. Component Locator
P/O Low Voltage Power Supply Board, Horizontal Output Circuits

SERVICE SHEET 13 — THEORY OF OPERATION

Service Sheet 13 contains the horizontal sweep gating and output drivers circuits. Several horizontal signals cause horizontal deflection on the CRT. In normal operation the horizontal sweep is time shared with a character horizontal sweep. In X·Y·Z scope mode the horizontal deflection signal is the external X AXIS input. In 1 vs 2 mode the channel 2 signal becomes the horizontal deflection signal. The internal options can also produce a horizontal deflection signal.

Horizontal Sweep Signal Path. The horizontal sweep inputs are on J8 pins 5 and 6 to A1Q32 and A1Q34. The 1 vs 2 mode horizontal signal inputs are in parallel with the horizontal sweep inputs to A1Q33 and A1Q35. Only the horizontal sweep inputs or the 1 vs 2 horizontal signal inputs are available depending on the selected mode of operation. A1R135 is to adjust the horizontal deflection of the 1 vs 2 horizontal signal input.

The horizontal sweep signal is applied to the bases of A1Q36 and A1Q37. At the base of A1Q37 a HORIZ POS (Horizontal Position) signal is added to the signal. The horizontal position is a dc DAC voltage which is proporitional to the setting of the Control Knob when assigned to Horizontal Position. The signal is amplified in these transistors and applied to the bases of A1Q45A and A1Q45B. The emitters of A1Q45A and A1Q45B contain the Sweep Length adjustment, A1R148, and the LBFD (Low, Beam Find) signal input. When the front panel FIND BEAM key is pressed, LBFD is low and will greatly decrease the gain of A1Q45A and A1Q45B. With the gain of these amplifiers decreased the horizontal deflection displayed on the CRT is greatly decreased. The collectors of A1Q45A and A1Q45B have a Plate Average adjustment (A1R184) connected between them. The adjustment is to balance the dc potential on the horizontal deflection plates of the CRT.

The horizontal sweep signal will be gated through the switches A1Q47 and A1Q48 and become the inputs for the Output Driver stages.

Horizontal Output Drivers. The Horizontal Output Drivers are shunt feedback stages. In the upper Output Driver stage, A1Q49 and A1Q50 are emitter followers with A1Q49 providing the ac signal path. Resistor A1R158 provides the dc feedback path. Variable capacitors, A1C52 and A1C57 adjust the sweep linearity at high sweep rates (less than 50 ns). In the lower Output Driver stage, A1Q53 and A1Q54 are emitter followers with A1Q53 providing the ac signal path. Resistor A1R166 provides the dc feedback path.

X AXIS Input. The X AXIS input, from the rear panel, is enabled when the signal HEXEN is high. HEXEN will be high when X·Y·Z Scope mode is selected. With HEXEN high, the transistors A1Q38 and A1Q39 are enabled and the external input becomes a differential signal to the bases of A1Q36 and A1Q37. The X·Y·Z. Mode is a special operating mode and the 1980 specifications should be checked for X, Y, and Z input requirements.

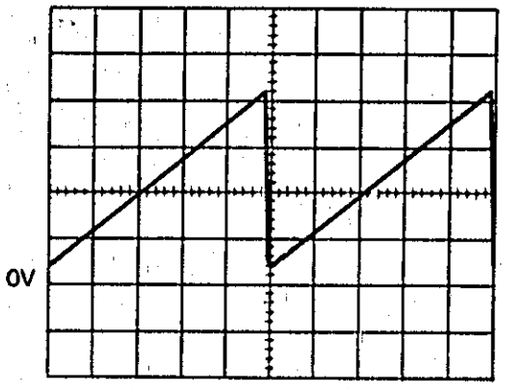
Horizontal Character Ramp. The signal HCHRH (High Character Reset Horizontal) controls the horizontal ramp. With HCHRH high transistor A1Q30 will conduct placing a ground at the top of A1R106 and discharging the ramp capacitor A1C40. When HCHRH goes low A1C40 will charge through A1Q31, A1R104, and A1R105. Resistor, A1R104, adjusts the ramp amplitude to set the horizontal character gain. The voltage across A1C40 is applied to the input of the Op Amp A1U7 to produce a positive going ramp voltage at the output. The other input of the Op Amp contains the horizontal character position adjustment, A1R107, which sets the dc operating point for the ramp voltage. The ramp voltage is applied to the base of A1Q43 where it is amplified and the output of A1Q43 is applied to the main signal path if gated on by HCHEN. When HCHEN (High, Character Enable) is high, causing A1Q41 to conduct and turn A1Q47 and A1Q48 off to block the main sweep signal. HCHEN, when high, also turns A1Q40 on and A1Q42 off to allow the character ramp signal through A1CR44 and A1CR45 to produce the horizontal deflection signal.

Horizontal Option In. The DISPX (Display X) signal from the Waveform Storage Option on A1J7 pin 1 is applied to the base of A1Q44. The DISPX signal is available to the output drivers through A1Q44 and A1Q43 if the signal HCHEN is high. While the DISPX signal is being displayed, the horizontal character ramp is disabled by holding the signal HCHRH high.

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Monitor Oscilloscope Setup

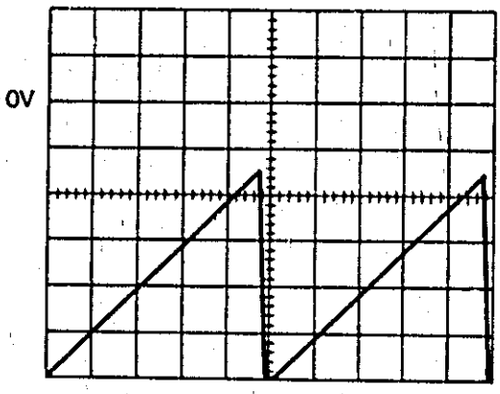
0.5 Volts/Div
10μSec/Div

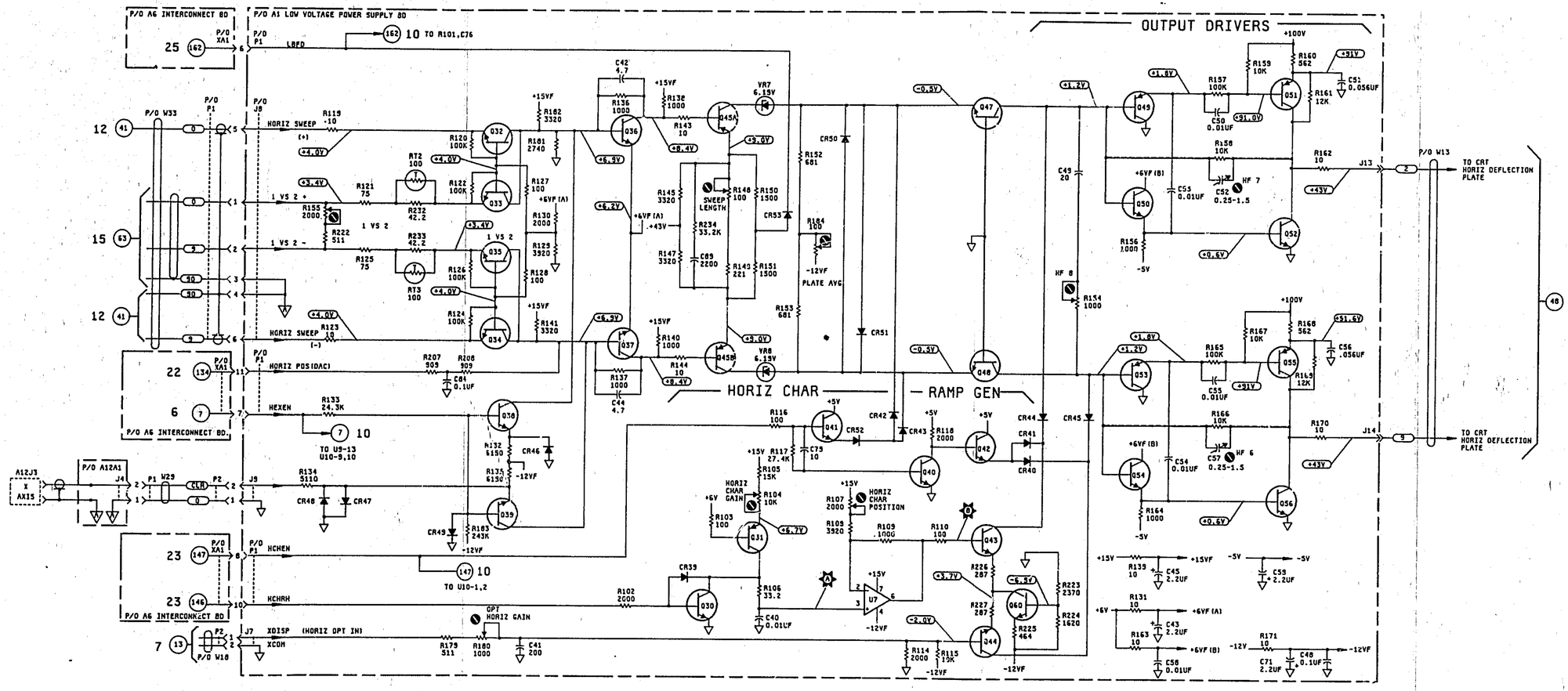


Ⓑ

Monitor Oscilloscope Setup

0.5 Volts/Div
10μSec/Div





NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES

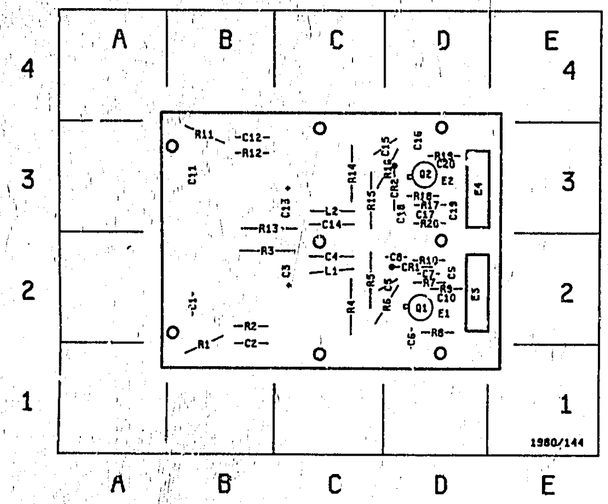
PARTS ON THIS SCHEMATIC

P/O A1	P/O A6
C40,41,43-45,48-59,71, 79,84,89 CR39-53 J7-9,13,14 P/O P1 Q30-45,47-56 R102-110,114-141,143-145 147-171,179-184,207,208 R222-227,R232-234 RT2,3 U7 VR7,8	P/O XA1
	CHASSIS
	P/O W13 P/O W29 P/O W33 P/O W16
	P/O A12
	J3 A1J4

DELETED R142,R146,C42,C46,C47,C49 1980/218/7/16/81

13

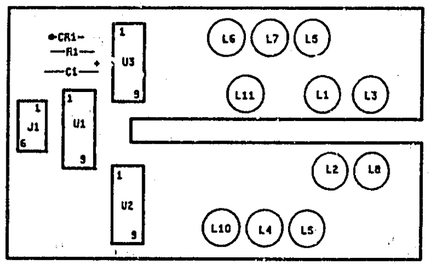
Service Sheet 13. Schematic Diagram
P/O Low Voltage Power Supply Board, Horizontal Output Circuits



A14A1

A14A1 TRIGGER ATTENUATOR BOARD, COMPONENT LOCATIONS

REF DESIG.	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-2	C14	C-3	L1	C-2	R9	D-2
C2	B-1	C15	D-3	L2	C-3	R10	D-2
C3	C-2	C16	D-3	Q1	D-2	R11	B-3
C4	C-2	C17	D-3	Q2	D-3	R12	B-3
C5	D-2	C18	D-3	R1	B-1	R13	B-3
C6	D-2	C19	D-3	R2	B-2	R14	C-3
C7	D-2	C20	D-3	R3	B-2	R15	C-3
C8	D-2	CR1	D-2	R4	C-2	R16	D-3
C9	D-2	CR2	D-3	R5	C-2	R17	D-3
C10	D-2	E1	D-2	R6	D-2	R18	D-3
C11	B-3	E2	D-3	R7	D-2	R19	D-3
C12	B-3	E3	D-2	R8	D-2	R20	D-3
C13	C-3	E4	D-3				



A14A2

SERVICE SHEET 14 MNEMONICS

CVT	**Clock, Vertical and Trigger** — Clock for vertical and trigger shift register string, to shift data through the string.
DEXT	**Delayed External Trigger** — Front panel input.
DLY'D TRIG TAG	**Delayed Trigger Probe Tag** — Signal to indicate division ratio of probe attached to delayed ext. trigger input.
HTDC	**High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.
LB32	**Latch bit 32** — 32nd bit of a 56 bit serial data string.
MAIN TRIG TAG	**Main Trigger Probe Tag** — Signal to indicate division ratio of probe attached to main ext. trigger input.
MEXT	**Main External Trigger** — Input from Front Panel.

Service Sheet 14. Component Locator
Trigger Attenuator

SERVICE SHEET 14 — THEORY OF OPERATION

The Trigger Attenuator is a series of switches to select the attenuator ranges and input couplings. The attenuators also contain a input impedance matching device.

Attenuator Switching. All attenuator switching is controlled by the processor control system through the use of relay switching. Switching command data is from a serial data string, LB32 (Latch Bit 32), and is shifted into the proper storage register by the signal CVT (Clock, Vertical and Trigger). After LB32 is properly shifted into A14U1 the signal HTDC (High, Transfer Data Command) enables parallel output of the shift register, A14U1. Any high output from A14U1 through the inverter drivers, A14U2 or A14U3, will cause a relay solenoid to be energized.

The 11 relays in the Trigger Attenuator are made up of three pieces. The 11 relay solenoids are located on the solenoid board. Mounted on the frame below each solenoid is a moveable armature. When a solenoid is energized it creates a magnetic field which attracts the back of the armature. When the rear of the armature is pulled up, the front is forced down and will close a switch contact located on the attenuator board.

Attenuator Input Circuit. Each input is located on the 1980 front panel and contains a BNC connector with a conductive ring around the connector. When a 1008X series probe is connected to the BNC connector a probe key button makes contact with the conductive ring to identify the divider ratio of the attached probe. The probe detector rings are wired to the Processor Board as Trigger Tag signals.

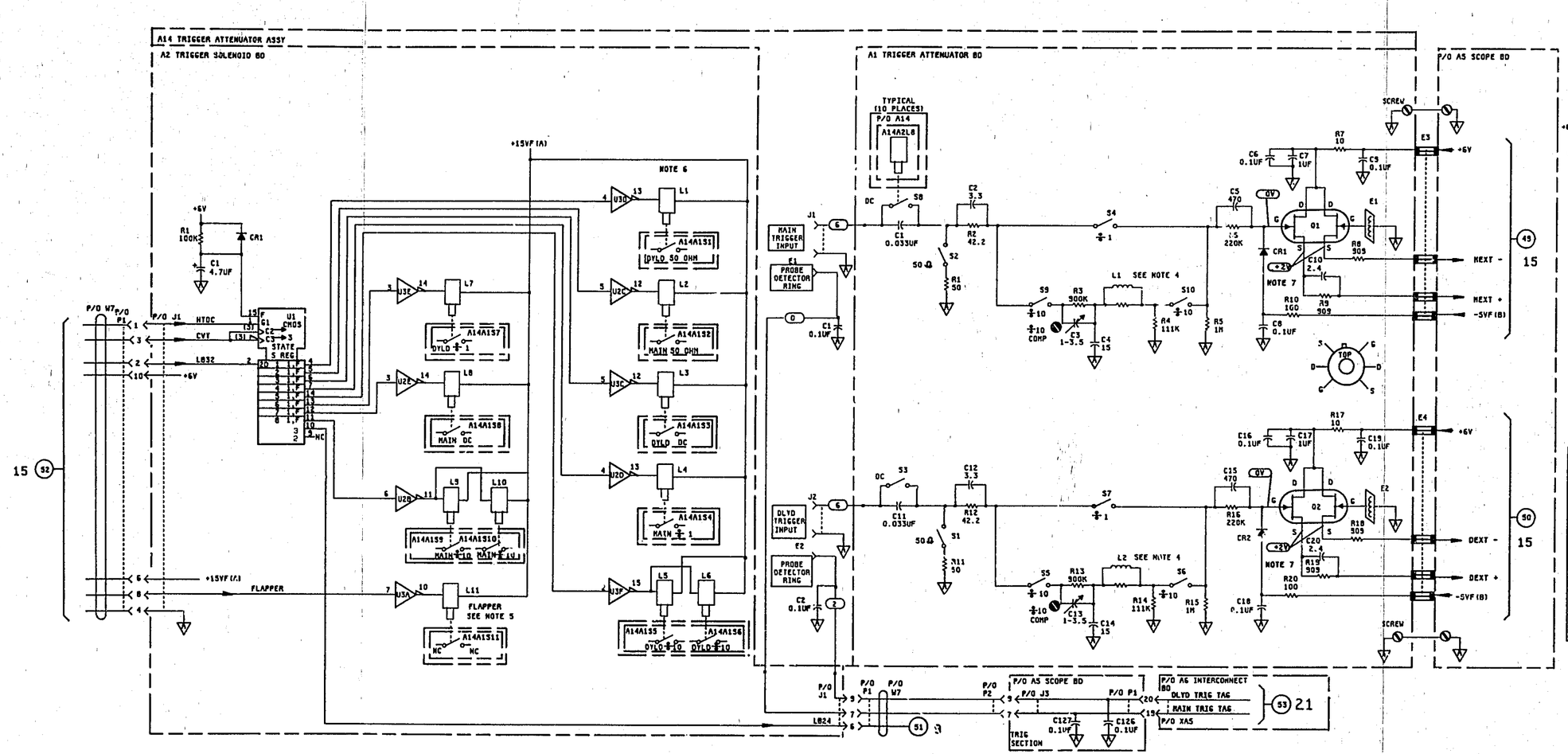
Attenuator Board Assembly. The Attenuator Board Assembly contains two identical attenuator circuits, one for Main Trigger input and the other for Delayed Trigger input. The Main Trigger and Delayed Trigger attenuaters are identical, therefore, only the Main Trigger circuit will be discussed.

Input Coupling. When GND coupling is selected, S3 (Series Switch) is opened and ground is connected to the attenuator through S4 (50 ohm switch) and A13R1. All coupling modes except GND require S3 to be closed. If AC coupling is selected, the signal path is through C1. If DC coupling is selected, S1 (DC switch) will be closed shunting around A13C1. If 50 OHM DC is selected, S1 and S4 will both be closed causing a series DC signal path with 50 ohms to ground.

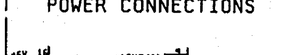
Input Coupling. If AC coupling is selected, the signal path is through C1. If DC coupling is selected, S8 (DC switch) will be closed shunting around A14C1. If 50 OHM DC is selected, S8 and S2 will both be closed causing a series DC path with 50 ohms to ground.

Attenuator Selection. When divide by one attenuation is selected S4 (÷1 switch) will be closed. If divide by ten is selected both S9 and S10 (÷10 switches) will be closed. The signal is attenuated and applied to the gate of a JFET, Q1. The JFET is connected in a source follower configuration. Output of the Attenuator Board Assembly is MEXT + and MEXT − which go to the trigger preamp microcircuit shown on Service Sheet 15.

It is not recommended that repairs, other than replacement of R1, R11, Q1, and Q2, be attempted on the Attenuator Board Assembly.



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENARIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L
4. A14A1L1 AND A14A1L2 ARE 56 OHM, 10I,0.25W RESISTORS WITH 8 TURNS AWG 32 WIRE WRAPPED AROUND THE RESISTOR BODY.
5. FLAPPER IS MECH. DEVICE FOR MAKING CLICK SOUND.
6. TYPICAL RESISTANCE OF EACH COIL L1-L11 IS APPX 580 OHMS
7. VOLTAGE DEPENDS ON GATE -TO- SOURCE VOLTAGE OF THE FET. TYPICAL VALUES RANGE BETWEEN +1V AND +3V. THE VOLTAGE LEVEL AT THE SOURCES OF Q1A AND Q1B (Q2A AND Q2B) MUST BE EQUAL WITH NO INPUT TO J1(J2).

PARTS ON THIS SCHEMATIC

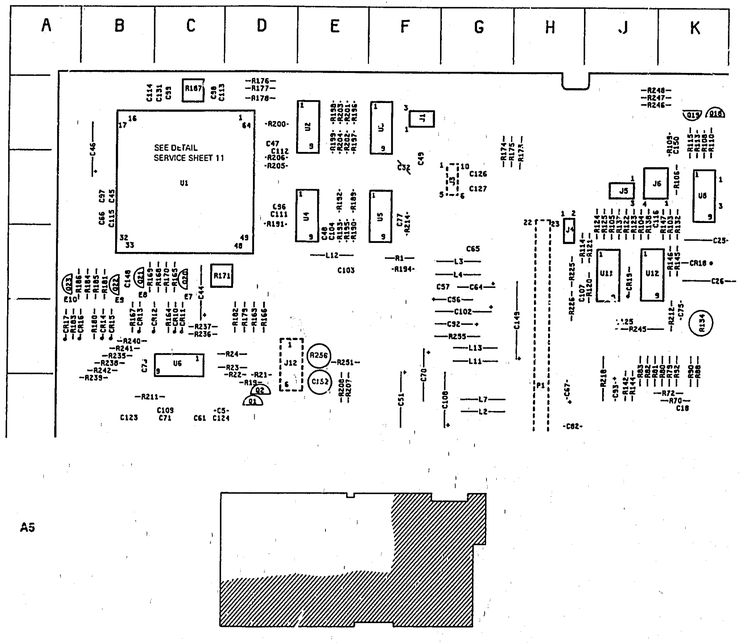
A14	A14A1	A14A2
A1,2 C1,2 E1,2 J1,2	C1-20 CR1,2 E1-4 L1,2 R1,2 R1-20 S1-11	C1 CR1 J1 L1-11 R1 U1,2B,C,D,E U3A,C,D,E,F
P/O A4	P/O A5	P/O A6
P/O P1	C126,127 P/O J3 P/O P1	P/O XA5, P/O XA4
CHASSIS		
W7		

1980/100/4/6/81

14

A5 SCOPE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	L-9	C61	C-4	C118	L-8	E6	F-2	R2	H-2	R60	G-3	R116	P-7	R174	G-8	R232	N-3
C1	D-3	C62	B-2	C119	Q-3	E6	F-2	R3	J-2	R61	G-2	R117	P-6	R175	G-8	R233	N-3
C2	B-3	C63	M-8	C120	E-1	E7	C-6	R4	G-7	R62	G-3	R118	P-7	R176	D-8	R234	N-3
C3	B-2	C64	G-6	C121	C-2	E8	B-6	R5	H-2	R63	G-3	R119	N-5	R177	D-8	R235	B-5
C4	D-2	C65	G-8	C122	B-2	E9	B-6	R6	H-2	R64	P-7	R120	J-6	R178	D-8	R236	C-5
C5	C-4	C66	B-7	U23	B-4	E10	A-6	R7	E-2	R65	P-7	R121	J-6	R179	D-5	R237	C-5
C6	B-3	C67	H-4	U124	C-4	E11	L-3	R8	E-2	R66	P-7	R122	J-7	R180	G-5	R238	B-5
C7	B-2	C68	N-3	C125	J-5	J1	F-8	R9	E-2	R67	P-7	R123	J-7	R181	D-6	R239	B-4
C8	D-2	C69	N-6	C126	G-7	J2	F-8	R10	D-2	R68	N-8	R124	J-7	R182	D-5	R240	B-5
C9	E-3	C70	F-5	C127	G-7	J3	G-7	R11	D-3	R69	M-8	R125	J-7	R183	A-5	R241	B-5
C10	F-2	C71	C-4	C128	G-3	J4	H-7	R12	F-2	R70	K-4	R126	N-7	R184	E-6	R242	B-5
C11	F-3	C72	B-3	C129	G-3	J5	J-7	R13	D-2	R71	L-4	R128	P-7	R185	B-6	R243	P-3
C12	F-2	C73	B-5	C130	B-3	J6	J-7	R14	D-2	R72	K-4	R129	N-6	R186	A-6	R244	P-3
C13	F-3	C74	D-2	C131	C-8	J7	L-5	R15	F-2	R73	L-4	R130	P-7	R187	C-8	R245	J-5
C14	F-4	C75	K-6	C132	M-8	J8	F-3	R16	F-2	R74	K-5	R131	M-8	R189	E-7	R246	J-8
C16	G-3	C76	P-6	C133	P-5	J9	A-7	R17	F-2	R75	K-4	R132	K-7	R190	E-6	R247	J-8
C18	N-8	C77	F-7	C134	F-2	J10	P-4	R19	D-4	R76	L-5	R133	K-5	R191	D-7	R248	J-8
C17	M-8	C78	M-5	C135	H-2	J11	P-4	R20	D-4	R77	K-5	R134	K-5	R192	E-7	R249	P-4
C18	K-4	C79	L-5	C139	H-2	J12	D-5	R21	D-5	R78	L-5	R135	M-8	R193	E-6	R250	G-6
C19	L-4	C81	K-4	C140	Q-3	J13	L-7	R22	D-5	R79	K-6	R136	M-8	R194	F-6	R251	E-5
C20	F-5	C82	H-4	C141	G-2	L1	E-3	R23	D-5	R80	K-5	R137	J-7	R195	E-6	R252	E-4
C21	P-5	C83	J-4	C142	G-2	L2	G-4	R24	D-5	R81	J-5	R138	J-7	R196	E-8	R255	G-5
C22	L-8	C84	K-2	C144	F-6	L3	G-6	R25	D-4	R82	J-5	R139	N-8	R197	E-8	R256	E-5
C24	N-5	C85	L-2	C145	F-2	L4	G-6	R27	D-2	R83	J-5	R140	L-3	R198	E-8	RT1	E-4
C25	K-6	C86	L-4	C146	E-2	L6	P-6	R28	D-2	R84	P-5	R141	N-3	R199	E-8	TP1	H-2
C26	K-6	C87	M-4	C147	L-2	L7	G-4	R29	E-3	R85	P-5	R142	J-4	R200	D-8	TP2	H-2
C27	M-5	C89	N-4	C148	B-6	L8	M-8	R30	E-3	R86	P-5	R143	N-3	R201	E-8	U1	C-7
C28	M-5	C90	N-4	C149	H-6	L9	K-6	R31	E-3	R87	P-5	R144	J-4	R202	E-8	U2	E-8
C29	L-8	C90	J-2	C150	K-8	L11	G-5	R32	E-3	R88	K-5	R145	K-6	R203	E-8	U3	F-8
C31	N-5	C91	H-3	C161	D-3	L12	K-6	R33	E-4	R89	K-4	R146	K-6	R204	E-8	U4	E-7
C32	F-8	C92	G-5	C162	E-4	L13	G-5	R34	E-3	R90	K-5	R147	K-7	R205	D-7	U5	F-7
C33	M-8	C93	J-4	CR1	D-4	P1	H-4	R35	E-3	R91	K-5	R148	M-2	R206	D-7	U6	C-5
C34	L-5	C94	M-8	CR2	D-3	Q1	D-4	R36	E-3	R92	K-5	R149	M-2	R207	E-4	U7	C-3
C35	M-8	C95	N-5	CR3	D-4	Q2	D-4	R37	F-4	R93	M-5	R150	M-2	R208	E-4	U8	K-7
C36	P-6	C96	D-7	CR4	F-4	Q3	E-3	R38	F-2	R94	M-5	R151	M-2	R210	N-6	U9	M-5
C37	K-3	C97	B-7	CR5	E-3	Q4	E-4	R39	E-3	R95	M-5	R152	M-2	R211	B-4	U10	Q7
C38	P-5	C98	C-8	CR6	E-3	Q5	E-3	R40	F-2	R96	L-5	R153	N-2	R212	K-5	U11	J-6
C40	P-2	C99	C-8	CR7	G-3	Q6	F-3	R41	F-3	R97	L-5	R154	N-2	R213	P-4	U12	J-6
C41	P-3	C100	N-2	CR8	H-2	Q7	F-3	R42	F-3	R98	L-7	R155	N-2	R214	F-7	U13	L-5
C43	Q-3	C101	H-7	CR9	G-2	Q8	F-3	R43	F-3	R99	N-5	R156	P-2	R215	P-2	U14	Q-3
C44	C-6	C102	G-5	CR10	C-5	Q9	F-3	R44	F-3	R100	L-8	R157	P-2	R216	H-2	U15	K-3
C45	B-7	C103	E-6	CR11	C-5	Q10	F-3	R45	F-3	R101	L-8	R158	P-2	R217	K-5	U16	J-3
C46	B-8	C104	E-8	CR12	B-5	Q11	F-4	R46	F-3	R102	L-7	R160	P-4	R218	J-4	U17	M-3
C47	D-8	C105	L-5	CR13	B-5	Q12	F-4	R103	K-7	R103	K-7	R161	P-3	R220	D-5	U18	M-3
C48	E-6	C106	L-8	CR14	B-5	Q13	F-3	R48	F-3	R104	J-7	R161	P-3	R221	N-7	U19	N-3
C49	F-7	C107	H-6	CR15	B-5	Q14	F-2	R49	F-3	R106	J-7	R163	D-5	R222	M-8	U20	P-3
C51	F-4	C108	G-4	CR16	A-5	Q15	F-2	R50	G-3	R106	K-7	R164	C-6	R223	H-2	U21	P-3
C52	E-4	C109	C-4	CR17	A-5	Q16	L-5	R51	G-3	R107	L-7	R165	C-6	R224	H-2	U22	J-2
C53	M-4	C110	C-2	CR18	K-6	Q17	M-4	R52	G-3	R108	K-8	R166	D-5	R225	H-6	U23	J-2
C54	M-3	C111	D-7	CR19	J-6	Q18	K-8	R53	G-2	R109	K-8	R167	B-5	R226	N-5	U24	L-2
C55	P-3	C112	D-8	CR20	J-3	Q19	K-8	R54	F-4	R110	K-8	R168	C-5	R227	L-2	U25	N-2
C56	G-6	C113	C-8	CR21	D-3	Q20	C-6	R55	F-3	R111	N-5	R169	B-6	R228	M-2	U26	P-2
C57	G-6	C114	B-8	E1	E-3	Q21	B-6	R56	F-3	R112	N-5	R170	C-6	R229	M-2	VR1	E-3
C58	E-2	C115	B-7	E2	E-3	Q22	B-6	R57	G-3	R113	K-8	R171	C-6	R230	M-2	VR2	E-3
C59	E-2	C116	J-7	E3	G-3	Q23	A-6	R58	G-3	R114	H-8	R173	H-8	R231	M-2	VR3	N-6
C60	D-2	C117	L-5	E4	G-3	R1	F-8	R59	G-3	R115	K-8						



SERVICE SHEET 15 MNEMONICS

CVT — Clock, Vertical and Trigger — Clock for vertical and trigger shift register string, to shift data through the string.

DEXT — Delayed External Trigger — Front panel input.

DT10HZ — Delayed Trigger Low Frequency Reject — Control signal from processor to trigger microcircuit — high = AC coupled 10 Hz cutoff; low = DC coupled.

DTAC — Delayed Trigger AC Coupling — Contol signal from processor to trigger microcircuit — high = AC coupling —coupling is in the trigger microcircut and independent of attenuator coupling.

DTHYST — Delayed Trigger Hysteresis — Control signal from processor to trigger microcircuit — sets trigger sensitivity lower on 2-9.99 mV range. High = low gain; low = high gain.

DTINT — Delayed Trigger Internal — Control signal from processor to trigger microcircuit to select internal or external trigger source — high = internal; low = external.

DTLP — Delayed Trigger Low Pass — Control signal from processor to trigger microcircuit — High frequency reject —high = HF REJ; low = DC coupled.

DTSLP — Delayed Trigger Slope — Control signal from processor to trigger microcircuit — selects trigger slope —high = positive slope; low = negative slope.

DT VU ADJ — Delayed Trigger View Adjust.

HBL — High, Bandwidth Limit — When high limits vertical bandwidth to approximately 20 MHz.

HDCLK — High, Delayed Clock — Signal from delayed trigger output used by the horizontal microcircuit to count events to digitally delay delayed sweep.

HDCLKP — High, Delayed Clock Plug In — Signal from delayed trigger output available to the enhancement module.

HDST — High, Delayed Sweep Trigger — Generated by trigger circuit to start delayed sweep in the triggered mode.

HDTE — High, Delayed Trigger Enable — Generated at end of main sweep and applied to trigger circuit to allow HDST to be generated when desired.

HDTV — High, Delayed Trigger View — When activated allows delayed trigger signal to be applied to the vertical for viewing.

HMCLK — High, Main Clock — Out at from main trigger microcircuit of trigger signal — used by horizontal microcircuit to RESET the auto sweep timer.

HMCLKP — High, Main Clock Plug In — Output from main trigger microcircuit of the trigger signal available to the enhancement module.

HMST — High, Main Sweep Trigger — Generated by trigger microcircuit to start main sweep in triggered mode.

HMTE — High, Main Trigger Enable — From horizontal microcircuit to main trigger circuit signifying main sweep is ready to accept a trigger — after holdoff.

HMTV — High, Main Trigger View — When activated allows main trigger signal to be applied to vertical for viewing.

Service Sheet 15, Component Locator
P/O Scope Board, Trigger Preamp

SERVICE SHEET 15 MNEMONICS (CONT'D)

HTDC	**High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.
LB32	**Latch bit 32** — 32nd bit of a 56 bit serial data string.
LEVENTS	**Low, Events** — When low the delay time is oependent on the number of events before a delayed ramp is enabled.
MEXT	**Main External Trigger** — Input from Front Panel.
MT10HZ	**Main Trigger Low Frequency Reject** — Control signal from processor to trigger microcircuit - high = AC coupled 10 Hz cutoff; low = DC coupled.
MTAC	**Main Trigger AC Coupling** — Contol signal from processor to trigger microcircuit — high = AC coupling —coupling is in the trigger microcircut and independent of attenuator coupling.
MTHYST	**Main Trigger Hysterisis** — Control signal from processor to trigger microcircuit — sets trigger sensitivity lower on 2-9.99 mV range. High = low gain; low = high gain.
MTINT	**Main Trigger Internal** — Control signal from processor to trigger microcircuit to select internal or external trigger source — high = internal; low = external.
MTLP	**Main Trigger Low Pass** — Control signal from processor to trigger microcircuit — High frequency reject —high = HF REJ; low = DC coupled.
MTSLP	**Main Trigger Slope** — Control signal from processor to trigger microcircuit - selects trigger slope high = positive slope; low = negative slope.
MT VU ADJ	Main Trigger View Adjust
PIDSYNC	**Plug-in Delayed Sync** — Signal from enhancement module to internally trigger delayed sweep if selected.
PIMSYNC	**Plug-in Main Sync** — Signal from enhancement module to internally trigger main sweep if selected.
SDTA	**Serial Data** — Data string from IO to various shift registers wher, clocked into shift register strings initiates various functions, lamps, etc.
TV	**Trigger View** — Outputs of trigger amplifier to vertical for viewing trigger signal.

SERVICE SHEET 15 — THEORY OF OPERATION

Service sheet 15 contains the Trigger Preamplifier and associated circuits. Most of the trigger circuitry is contained within a single hybrid intregrated circuit. Trigger functions are selected and controlled by the processor control circuits.

Processor Control. Control data from the Processor Board Assembly is the signal SDTA (Serial Data). SDTA input on A5J2 pin 3 is the input to two shift registers A5U5 and A5U3. The two shift registers are clocked by CVT (Clock, Vertical and Trigger) and the serial data output of A5U5 is the input for A5U3. After the proper number of clocks to shift the SDTA into the correct shift register location a HTDC (High, Transfer Data Command) is produced. The HTDC makes the data available to the parallel outputs of all the shift registers in the string.

The processor control signals set many of the conditions for the trigger microcircuit. The processor control signals and descriptions are as follows:

MTHYST (DTHYST) — Main Trigger Hysteresis (Delayed Trigger Hysteresis) — Selects the trigger sensitivity to be used. This signal is controlled by the volts/division setting of the selected trigger source channel. If the volts/division of the selected channel is 9.99 mv or less the MTHYST signal is high to decrease the gain of the trigger signal. DTHYST is the same as main for control of the delayed trigger.

MTINT (DTINT) — Main Trigger Internal (Delayed Trigger Internal) — Selects Main internal or external trigger source. This signal is controlled from the front panel INT key. The DTINT serves the same function for the delayed trigger.

MTSLP (DTSLP) — Main Trigger Slope (Delayed Trigger Slope) — Selects either the positive going or negative going edge of the trigger signal as the trigger slope. A high selects the positive going edge. DTSLP serves the same function for the delayed trigger. These signals are controlled from the front panel Main and Delayed Slope keys.

MTLP (DTLP) — Main Trigger Low Pass (Delayed Trigger Low Pass) — Selects a high frequency reject circuit and passes only the low frequency portion of the selected trigger signal or selects a dc coupled trigger signal. With MTLP high, High Frequency Reject is selected and low MTLP selects the dc coupled signal. Controlled from the front panal HF REJ key. DTLP serves the same function for the delayed trigger.

MT10HZ (DT10HZ) — Main Trigger 10 Hz (Delayed Trigger 10 Hz) — Selects a low frequency reject circuit and passes only the high frequency portion of the selected trigger signal or selectes an ac coupled trigger signal. When the ac coupled trigger signal is selected it has a cutoff of approximately 10 Hz. With MT10HZ high AC Coupled with 10 Hz cutoff is selected and when low, Low Frequency Reject is selected. MT10HZ is controlled by the front panel LF REJ key. DT10HZ serves the same function for the delayed trigger.

MTAC (DTAC) — Main Trigger AC Coupled (Delayed Trigger AC Coupled) — Selects ac coupling within the Trigger microcircuit when high. MTAC is controlled by the front panel AC key.

HBL — High Bandwidth Limit — Not used by the Trigger circuits. Used by the vertical output circuits to decrease the bandwidth of the vertical output when high.

FLAPPER — Used to produce an audible indication that a key closure has been made. Energizes a relay soleniod in the trigger attenuator.

LB32 — Latch Bit 32 — Serial data output of the trigger preamp to the trigger attenuator.

LEVENTS — Low, Events — Selects the events delay mode. With this signal low a number of trigger events must occur before the delayed sweep ramp can be produced. The number of events of delay is set when the front panel Control Knob is assigned to DGTL DLY.

1 vs 2 — Enables the 1 vs 2 mode within the trigger microcircuit. The channel 1 input is the vertical signal via the standard vertical amplifiers, and channel 2 input becomes the horizontal signal via the sync output of the vertical preamp to the horizontal amplifiers.

The other inputs to the trigger microcircuit are MAIN SYNC ± which is the main sync outputs from the vertical microcircuit. PIMSYNC ± are the main sync outputs from the vertical microcircuit contained in the enhancement module. Only one of the main sync will be available depending on the selected main trigger channel.

DLYD SYNC ± and PIDSYNC ± are the delayed trigger signals from the vertical microcircuit and vertical microcircuit in the enhancement module.

The signal HMTE (High, Main Trigger Enable) is from the horizontal microcircuit indicating the sweep is armed an a trigger can be produced. HDTE (High, Delayed Trigger Enable) is from the horizontal microcircuit and enables the delayed trigger circuits.

Main Trigger Level and Delayed Trigger Level are from the processor DAC and determine the trigger point on the signal. The DAC voltage is set when the Control Knob is assigned to main or delayed trigger level functions.

The adjustments, MT VU ADJ (Main Trigger View Adjust) and DT VU ADJ (Delayed Trigger View Adjust) set the trigger point of the sweep on the trigger view signal. The adjustment is made so that 0 volts s at center screen.

The TV (Trigger View) outputs on A5U1 pins 56 and 57 are the trigger view signal to the vertical deflection circuits on service sheet 9.

HMST (High, Main Sweep Start) is the signal that triggers the horizontal microcircuit to start the main sweep. The trigger must recieve a HMTE before it will produce the HMST. HDST (High, Delayed Sweep Start) is the signal that triggers the horizontal microcircuit to start the delayed sweep. The trigger microcircuit must receive a HDTE before it will produce the HDST. The HDTE signal is only produced after a main sweep has been completed.

HMCLK (High, Main Clock) and HMCLKP (High, Main Clock Plug-in) are produced by the trigger microcircuit from the trigger signal. HMCLK is used by the horizontal microcircuit to reset the Auto Sweep Timer. HMCLKP is available to the enhancement module connector.

HDCLK (High, Delayed Clock) and HDCLKP (High, Delayed Clock Plug-in) are produced by the trigger microcircuit and used by the horizontal microcircuit to count events in the digital delay mode and to start the triggered delayed sweep. HDCLKP is available to the enhancement module connector.



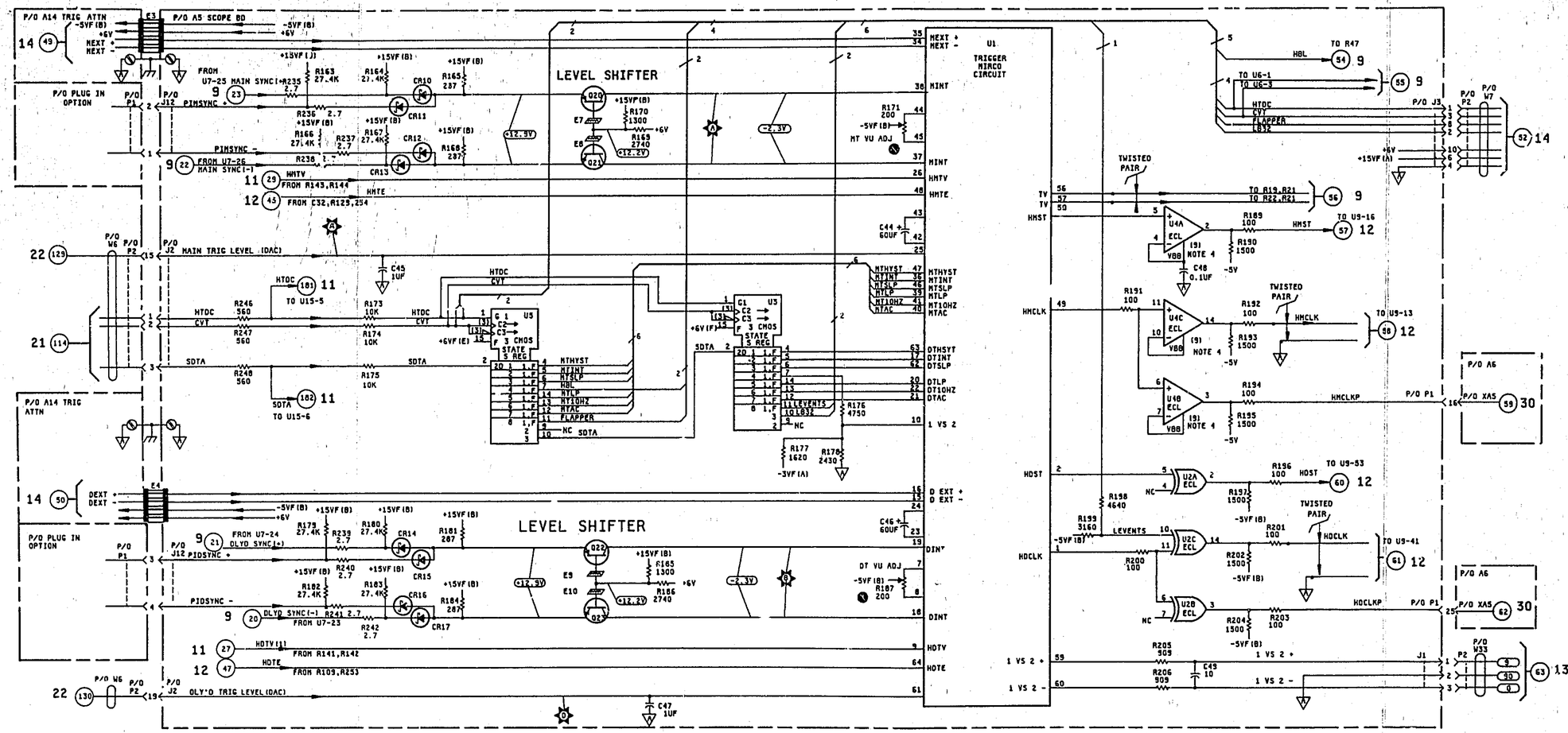
−4 VDC To +4 VDC

Reading is calibration factor dependent. Readings are end points measured as function (MAIN TRIG LEVEL) is varied.

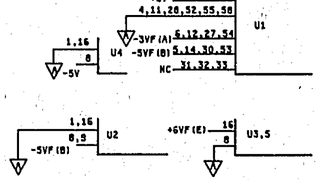


−4 VDC To +4 VDC

Reading is calibration factor dependent. Readings are end points measured as function (DLY'D TRIG LEVEL) is varied.



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. U4 PIN 9 IS AN INTERNALLY GENERATED BASE BIAS SUPPLY = -1.3V
5. ECL LOGIC LEVELS ARE :
   -0.9V =LOGIC"1"=H
   -1.75V =LOGIC"0"=L

PARTS ON THIS SCHEMATIC

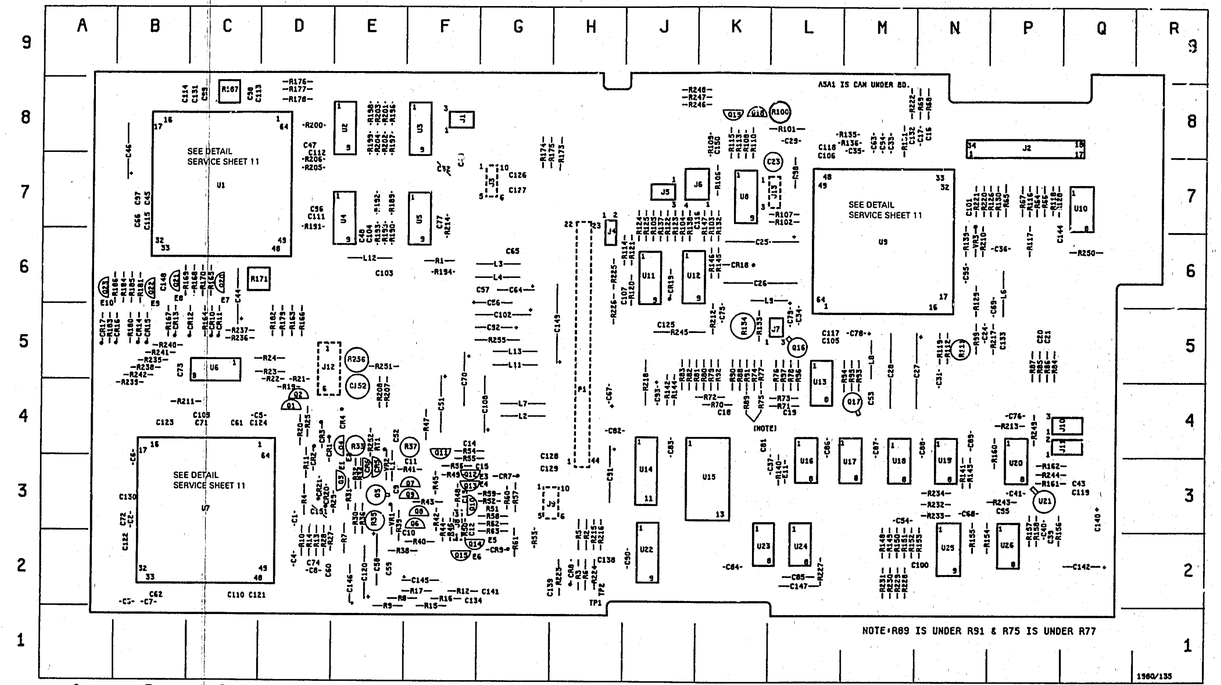
P/O A5	P/O A6	P/OA14
C44-49 CR10-17 E7-10 J1 P/O J2,3,12 P/O P1 Q20-23 R163-171,173-187,189-R206,235-242,246-248 U1,2,3,4	P/O XA5	E3,4
	CHASSIS	P/O PLUG IN
	P/O W6,7,33	

DELETE R172,R188,U20,U40

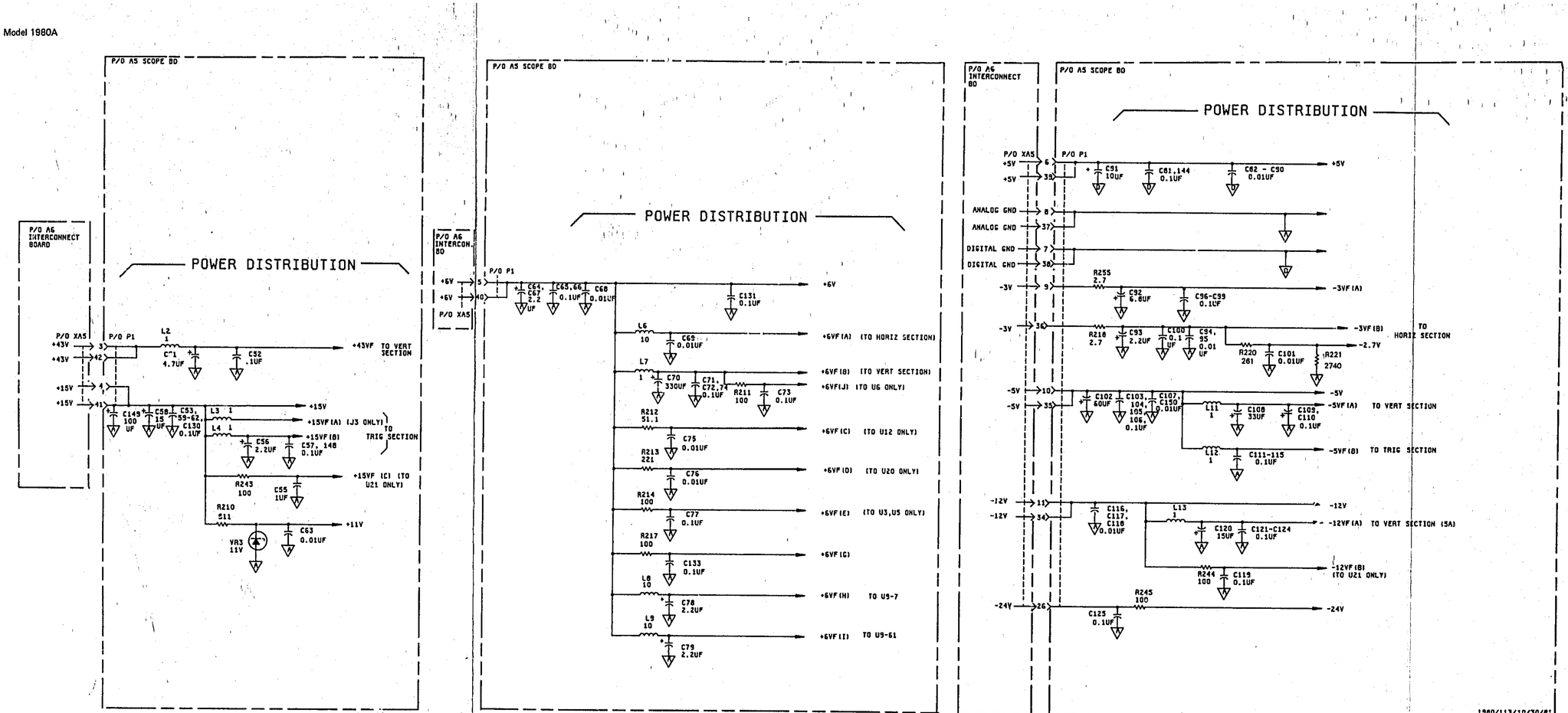
1980/109/10/30/61

A5 SCOPE BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
A1	L-3	C61	C-4	C118	L-6	E5	F-2	R2	H-2	R60	G-3	R116	P-7	R174	G-8	R232	N-3
C1	D-3	C62	B-2	C119	D-3	E6	F-2	R3	H-2	R61	G-3	R117	P-6	R175	G-8	R233	N-3
C2	B-3	C63	M-8	C120	E-2	E7	C-6	R4	D-3	R62	G-3	R118	P-7	R176	D-8	R234	N-3
C3	B-2	C64	G-6	C121	J-2	E8	B-6	R5	H-2	R63	G-3	R119	N-5	R177	D-8	R235	B-5
C4	D-2	C65	G-6	C122	J-1	E9	B-6	R6	H-2	R64	P-7	R120	J-6	R178	D-8	R236	C-5
C5	C-4	C66	B-7	C123	J-4	E10	A-6	R7	E-2	R65	P-7	R121	J-6	R179	D-5	R237	C-5
C6	B-3	C67	H-4	C124	C-4	E11	L-3	R8	E-2	R66	P-7	R122	J-7	R180	B-5	R238	G-5
C7	B-2	C68	N-3	C125	J-5	J1	F-8	R9	E-2	R67	P-7	R123	J-7	R181	B-6	R239	B-4
C8	D-2	C69	N-6	C126	G-7	J2	P-8	R10	D-2	R68	M-8	R124	J-7	R182	D-5	R240	B-5
C9	E-3	C70	F-5	C127	G-7	J3	G-7	R11	D-3	R69	M-8	R125	J-7	R183	A-5	R241	B-5
C10	F-2	C71	C-4	C128	G-3	J4	H-7	R12	F-2	R70	K-4	R126	N-7	R184	E-6	R242	B-5
C11	F-3	C72	B-3	C129	G-3	J5	J-7	R13	D-2	R71	L-4	R128	P-7	R185	B-6	R243	P-3
C12	F-2	C73	B-5	C130	B-3	J6	J-7	R14	D-2	R72	K-4	R129	N-6	R186	A-6	R244	P-3
C13	F-3	C74	D-2	C131	C-8	J7	L-5	R15	F-2	R73	K-4	R130	P-7	R187	C-7	R245	J-5
C14	F-4	C75	K-6	C132	M-8	J8	F-3	R16	F-2	R74	K-5	R131	M-8	R189	E-7	R246	J-8
C15	G-3	C76	F-4	C133	P-6	J9	G-3	R17	F-2	R75	K-4	R132	K-7	R190	E-6	R247	J-8
C16	N-8	C77	F-7	C134	F-2	J10	P-4	R19	D-4	R76	L-5	R133	K-5	R191	D-7	R248	J-8
C17	M-8	C78	M-5	C138	H-2	J11	P-4	R20	D-4	R77	K-5	R134	K-5	R192	E-7	R249	P-4
C18	K-4	C79	L-5	C139	H-2	J12	D-5	R21	D-5	R78	L-5	R135	M-8	R193	E-6	R250	Q-6
C19	L-4	C81	K-4	C140	G-3	J13	F-7	R22	D-5	R79	K-5	R136	M-8	R194	F-6	R251	E-6
C20	P-5	C82	H-4	C141	G-2	L1	E-3	R23	D-5	R80	K-5	R137	J-7	R195	E-6	R252	E-4
C21	P-5	C83	J-4	C142	Q-2	L2	G-4	R24	D-5	R81	J-5	R138	J-7	R196	E-8	R255	G-5
C23	L-8	C84	K-2	C144	P-6	L3	G-6	R25	D-4	R82	J-5	R139	N-6	R197	E-8	R256	E-6
C24	N-5	C85	L-2	C145	F-2	L4	G-8	R27	D-2	R83	J-5	R140	L-3	R198	E-8	R11	E-4
C25	K-6	C86	L-4	C146	E-2	L6	P-6	R28	D-2	R84	P-5	R141	N-3	R199	E-8	TP1	H-2
C26	K-6	C87	M-4	C147	L-2	L7	G-4	R29	E-3	R85	P-5	R142	J-4	R200	D-8	TP2	H-2
C27	M-5	C88	N-4	C148	B-6	L8	M-6	R30	E-3	R86	P-5	R143	N-3	R201	E-8	U1	C-7
C28	M-5	C89	N-4	C149	H-6	L9	K-8	R31	E-3	R87	P-5	R144	J-4	R202	E-8	U2	E-8
C29	L-8	C90	J-2	C150	K-8	L11	G-6	R32	E-3	R88	K-5	1145	K-6	R203	E-8	U3	F-8
C31	M-8	C91	N-3	C151	D-3	L12	G-6	R33	E-4	R89	K-4	R146	K-6	R204	E-8	U4	E-7
C32	F-8	C92	G-5	C152	E-4	L13	G-5	R34	E-3	R90	J-5	R147	K-7	R206	D-7	U5	F-7
C33	M-8	C93	J-4	CR1	D-4	P1	H-4	R35	E-3	R91	K-5	R148	M-2	R206	D-7	U6	C-5
C34	L-5	C94	M-8	CR2	D-3	Q1	D-4	R36	E-3	R92	K-5	R149	M-2	R207	E-4	U7	C-3
C35	M-8	C95	N-8	CR3	D-4	Q2	D-4	R37	F-4	R93	M-5	R150	M-2	R208	E-4	U8	K-7
C36	P-8	C96	D-7	CR4	E-4	Q3	E-3	R38	F-2	R94	M-5	R151	M-2	R210	N-8	U9	M-6
C37	K-3	C97	B-7	CR5	E-3	Q4	E-4	R39	E-3	R95	M-5	R152	N-2	R211	E-4	U10	G-7
C39	P-2	C98	C-8	CR6	E-3	Q5	E-3	R40	F-2	R96	L-5	R153	N-2	R212	K-5	U11	J-6
C40	P-2	C99	C-8	CR7	G-3	Q6	F-3	R41	F-3	R97	L-5	R154	N-2	R213	P-4	U12	J-6
C41	P-3	C100	N-2	CR8	H-2	Q7	F-3	R42	F-3	R98	L-7	R155	N-2	R214	F-7	U13	L-5
C43	D-3	C101	N-7	CR9	G-2	Q8	F-3	R43	F-3	R99	N-5	R156	P-2	R215	H-2	U14	L-3
C44	C-6	C102	G-5	CR10	C-5	Q9	F-3	R44	F-3	R100	L-8	R157	P-2	R216	H-2	U15	K-3
C45	B-7	C103	E-6	CR11	C-5	Q10	F-3	R45	F-3	R101	L-8	R158	P-2	R217	N-5	U16	L-3
C46	B-8	C104	E-6	CR12	B-5	Q11	F-4	R46	F-3	R102	L-7	R160	P-4	R218	J-4	U17	M-3
C47	D-8	C105	L-8	CR13	B-5	Q12	F-3	R47	F-4	R103	K-7	R161	P-3	R220	N-7	U18	M-3
C48	E-8	C106	L-8	CR14	B-5	Q13	F-3	R48	F-3	R104	J-7	R162	P-3	R221	N-7	U19	N-3
C49	F-7	C107	H-1	CR15	B-5	Q14	F-2	R49	F-3	R105	J-7	R163	D-5	R222	M-8	U20	P-3
C51	F-4	C108	L-2	CR16	A-5	Q15	F-2	R50	G-3	R106	K-7	R164	C-5	R223	H-2	U21	P-3
C52	E-4	C109	C-4	CR17	A-5	Q16	L-5	R51	G-3	R107	K-7	R165	C-6	R224	H-2	U23	J-2
C53	M-4	C110	C-2	CR18	K-6	Q17	M-4	R52	G-3	R108	K-8	R166	D-5	R226	H-6	U23	K-2
C54	M-3	C111	D-7	CR19	J-6	Q18	K-8	R53	G-2	R109	K-8	R167	B-5	R226	H-5	U24	L-2
C55	P-3	C112	D-8	CR20	D-3	Q19	K-8	R54	F-4	R110	K-8	R168	C-6	R227	L-2	U25	N-2
C56	G-3	C113	C-8	CR21	D-3	Q20	C-6	R55	F-3	R111	K-5	R169	B-6	R228	M-2	U26	P-2
C57	G-6	C114	B-8	E1	E-3	Q21	B-6	R56	F-3	R112	N-5	R170	C-6	R229	M-2	VR1	E-3
C58	E-2	C115	B-7	E2	E-3	Q22	B-6	R57	G-3	R113	K-8	R171	C-6	R230	M-2	VR2	E-3
C59	E-2	C116	J-7	E3	G-3	Q23	A-6	R58	G-3	R114	H-6	R173	H-8	R231	M-2	VR3	N-6
C60	D-2	C117	L-5	E4	G-3	R1	F-6	R59	G-3	R115	K-8						



Service Sheet 16. Component Locator
P/O Scope Board, Power Distribution



NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES

PARTS ON THIS SCHEMATIC

P/O A5	P/O A6
C51-53,55-79,81-125, C130,131,133,144,146-150 L2-4,6-9,11-13 R210-214,217,218,220, RZ21,243-245,255 P/O P1 VR3	P/O XA5

DELETED: C80,C135,C136,L5,L10,R219

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Service Sheet 16. Schematic Diagram P/O Scope Board, Power Distribution

SERVICE SHEET 17 — THEORY OF OPERATION

INTRODUCTION.

The 1980 Processor System is a micro processor system which includes 24K bytes of read-only memory (ROM) 3 1/2K bytes of random access memory (RAM), a 4 channel DMA controller, programmable timer, 64 bits of software controlled IO, and a variety of special interface subsystems. In addition, bus interfaces are provided to the HP-IB, enhancement module, Digital Waveform Storage Option and feature ROM options.

In order to fully describe the various functions of the processor, it is necessary to consider the system as a collection of five subsystems, which are: (1) the processor bus, (2) the parallel I/O subsystem, (3) the DAC subsystem, (4) the horizontal interface, and (5) the DMA/character generator subsystem. Each of these subsystems will be examined from both a functional and operational point of view. In addition to a fundamental hardware description, there will also be included various notes on the software interaction required to control each subsystem.

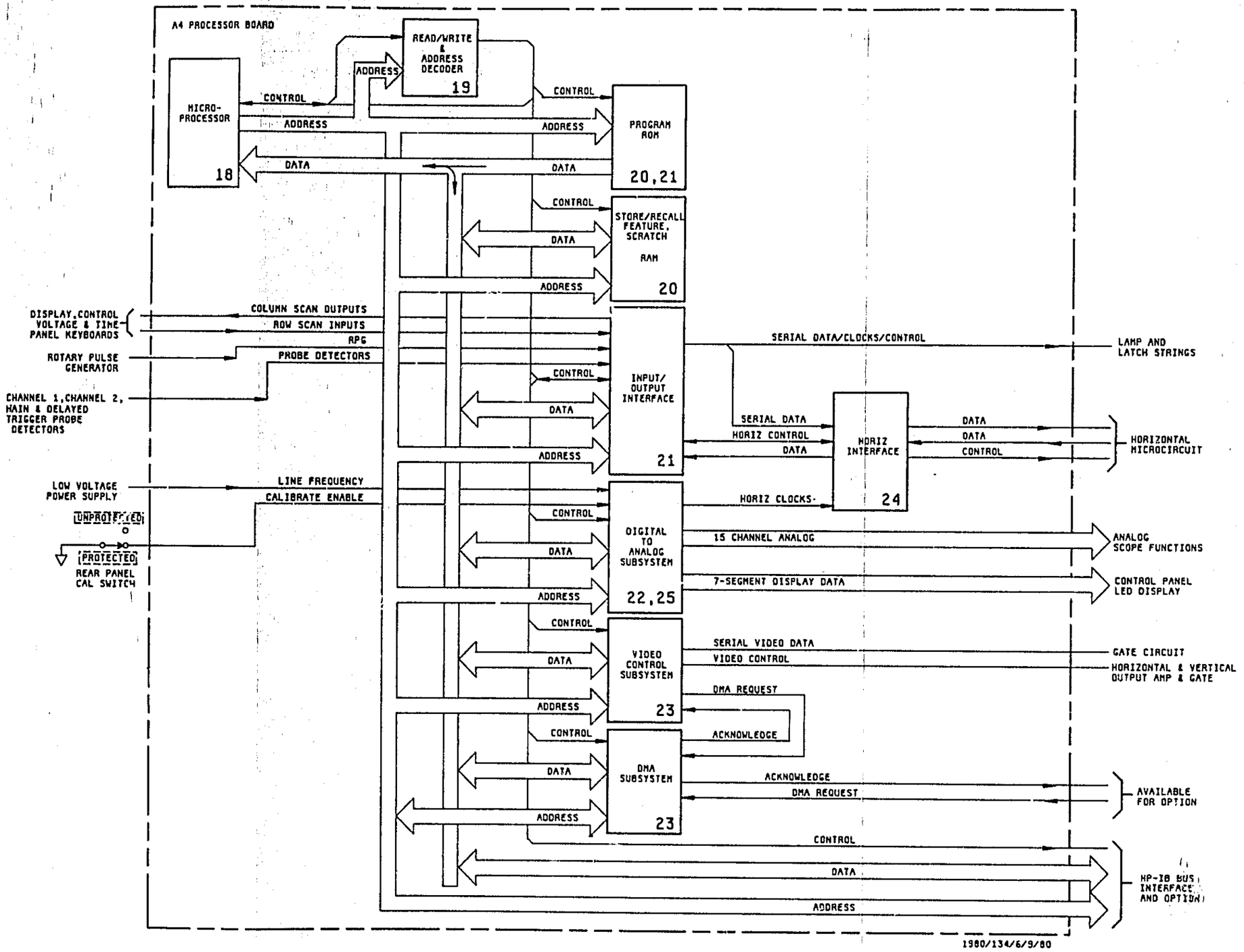
Processor Bus. The processor bus consists of the following elements:

1. 8085A microprocessor
2. Crystal-controlled clock oscillator
3. Bus buffers and bus transceivers
4. Address and control bus decoding logic
5. ROM memory
6. RAM memory

Together these elements form the basic components necessary for program execution. All other subsystems of the processor board provide the means of input and output of processed and unprocessed information. The basic function of the processor bus is to monitor the I/O subsystems and act upon external events (such as a front panel key closure or an HP-IB transaction). The software stored within the ROM memories contains all of the required logic to interpret these events and perform the necessary response.

ROM Memory. There are 24K bytes of read-only memory on the 1980 mainframe. Five of these devices are 4K × 8 mask ROM's (A4U26-A4U30 on Service Sheet 20), and two devices are ROM/IO ports (A4U17-A4U18 on Service Sheet 21), each of which store 2K bytes of mask ROM and contain 16 bits of direction programmable IO. All of the ROM memory is addressed

RAM Memory. There are 3 1/2 K bytes of random access storage in the mainframe system which consists of one RAM/IO (A4U16) port with 256 bytes of static RAM (on Service Sheet 21), two 256×4 CMOS static RAMs (A4U42-A4U43 on Service Sheet 22), four 1K×4 CMOS static RAMs (A4U34,A4U37 on Service Sheet 20), and two 1K×4 NMOS static RAMS (A4U32-A4U33 on Service Sheet 23).

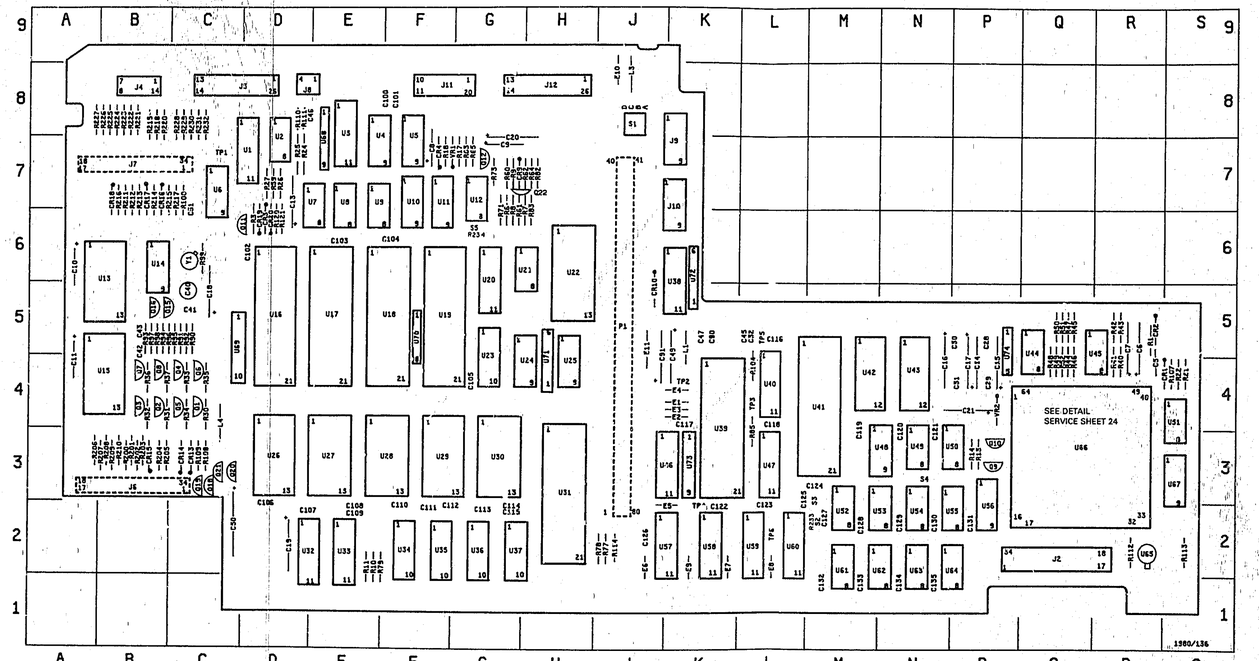


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Service Sheet 17.
Processor Board Simplified Block Diagram

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	R-4	C114	G-2	J2	Q-2	R24	D-7	R97	B-5	R231	C-8	U32	D-2		
C6	R-5	C115	G-2	J4	B-8	R25	D-7	R98	B-5	R232	C-8	U33	E-2		
C7	R-5	C116	L-5	J5	C-8	R26	D-7	R99	C-5	R233	M-2	U34	F-2		
C8	F-7	C117	K-4	J6	B-3	R27	D-7	R100	C-7	R234	G-8	U35	F-2		
C9	G-7	C118	L-4	J7	B-7	R30	C-4	R104	L-4	S1	J-8	U36	G-7		
C10	A-6	C119	M-3	J8	D-8	R31	B-4	R107	S-4	S2	M-2	U37	G-2		
C11	A-4	C120	N-3	J9	K-7	R32	B-4	R109	C-3	S3	M-2	U38	K-6		
C13	D-7	C121	N-3	J10	K-7	R33	C-4	R109	C-3	S4	N-3	U39	K-4		
C14	P-4	C122	K-2	J11	F-8	R34	C-4	R110	D-8	S5	G-8	U40	L-4		
C15	P-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	C-7	U41	M-4		
C16	N-4	C124	M-3	L1	K-5	R36	B-4	R112	R-2	TP2	K-4	U42	M-4		
C17	P-4	C125	L-3	L3	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	N-4		
C18	C-5	C126	J-2	L4	C-4	R40	B-4	R114	J-2	TP4	K-3	U44	O-5		
C19	D-2	C127	M-2	P1	J-5	R41	B-4	R120	D-6	TP5	L-5	U45	R-5		
C20	G-7	C128	M-2	Q1	C-4	R42	B-5	R121	D-6	TP6	L-2	U46	K-3		
C21	P-4	C129	N-2	Q2	B-4	R43	R-6	R200	B-3	U1	D-7	U47	L-3		
C28	P-5	C130	N-2	Q7	B-4	R44	Q-4	R201	B-3	U2	D-7	U48	N-3		
C29	P-4	C131	P-2	Q8	C-4	R45	Q-5	R202	B-3	U3	E-7	U49	N-3		
C30	P-5	C132	M-1	Q9	C-4	R46	Q-4	R203	B-3	U4	E-7	U50	N-3		
C31	P-4	C133	M-1	Q10	C-4	R47	Q-5	R204	B-3	U5	F-7	U51	S-4		
C32	L-5	C134	N-1	Q7	B-4	R48	Q-4	R205	B-3	U6	C-7	U52	M-2		
C40	C-5	C135	N-1	Q8	B-4	R49	Q-4	R206	A-3	U7	E-7	U53	N-2		
C41	C-5	CR1	S-4	Q9	P-3	R50	Q-5	R207	B-3	U8	E-7	U54	N-2		
C42	B-5	CR2	R-5	Q10	P-3	R51	Q-5	R208	B-3	U9	E-7	U55	N-2		
C43	B-5	CR3	D-5	Q11	D-5	R52	Q-4	R209	B-3	U10	F-7	U56	P-5		
C45	L-5	CR4	F-7	Q12	G-7	R53	D-7	R210	B-3	U11	F-7	U57	K-2		
C46	D-8	CR5	G-7	Q15	B-5	R60	D-7	R211	B-7	U12	G-7	U58	K-2		
C47	K-5	CR10	J-5	Q16	B-5	R61	G-5	R212	B-7	U13	B-5	U59	L-2		
C48	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	B-5	U60	L-2		
C50	C-2	CR14	C-3	Q19	C-3	R63	G-7	R214	B-7	U15	B-4	U61	M-2		
C51	C-5	CR15	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2		
C90	K-5	CR16	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-5	U63	N-2		
C91	J-4	CR17	B-7	Q22	G-7	R71	G-5	R217	C-7	U18	F-5	U64	P-2		
C100	F-8	CR18	B-7	R1	R-5	R72	G-7	R218	C-8	U19	F-5	U65	R-2		
C101	F-8	CR19	D-6	R2	G-6	R77	J-2	R219	B-8	U20	G-5	U66	Q-3		
C102	D-5	CR20	D-6	R6	G-6	R78	H-2	R220	B-8	U21	H-5	U67	S-3		
C103	E-5	E1	K-4	R7	H-6	R79	E-2	R221	B-8	U22	H-5	U68	E-7		
C104	F-5	E2	K-4	R8	G-6	R82	H-7	R222	B-8	U23	G-4	U69	C-5		
C105	G-4	E3	K-4	R9	G-7	R83	H-6	R223	B-8	U24	H-4	U70	F-5		
C106	D-2	E4	K-4	R10	E-2	R85	L-3	R224	B-8	U25	H-4	U71	H-4		
C107	E-1	E5	K-2	R11	E-2	R90	C-5	R225	B-8	U26	D-3	U72	K-5		
C108	E-2	E6	J-2	R12	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3		
C109	E-2	E7	K-2	R14	P-3	R92	C-5	R227	A-8	U28	F-3	U74	P-5		
C110	F-2	E8	L-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	F-7		
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4		
C112	F-2	E10	J-8	R21	S-4	R95	C-5	R230	C-8	U31	N-3	Y1	C-8		
C113	G-2	E11	J-5	R22	S-4	R96	B-5								



SERVICE SHEET 18 MNEMONICS

A0-A15 — **Address Lines 0-15** — A0-A7 are developed from the AD0-AD7 bus. A8 through A15 are most significant 8 bits of address.

AD0-AD7 — **Address/Data bus** — Microprocessor bidirectional bus. Data on this bus can be the least significant 8 bits of address.

ALE — **Address Latch Enable** — Microprocessor output. Falling edge is used to latch data on the AD0-AD7 bus into the address latch.

CLK — **Clock** — From microprocessor — 3.333333 MHz processor clock input divided by two.

HDTE — **High, Delayed Trigger Enable** — Generated at end of main sweep and applied to trigger circuit to allow HDST to be generated when desired.

HEXEN — **High, External Enable** — Exerted high when external X, Y, and Z inputs are to be used for deflection and blanking of beam.

HLDA — **Hold Acknowledge** — Acknowledges a DMA Controller hold request when control of the address and data buses are available for control by the DMA Controller — also places proper levels to various devices during DMA cycles.

HOLD — Request from the DMA Controller to the microprocessor to interrupt its cycle so the DMA controller can take control of the address and data buses for DMA data transfer.

IO/LM — **High, IO/Low, Memory** — selects either IO or Memory devices.

LDRC RDY — **Low, DAC Refresh Controller Ready** — Output from DRC which puts the processor in wait states until the DRC is ready to complete its bus cycle.

LINTRQ — **Low, Interrupt Request** — From HP-IB, wire ored with LINTRQ(PI) and inverted to become RST 5.5 to the processor. When low the processor is placed into an interrupt service routine.

LINTRQ(PI) — **Low, Interrupt Request (Plug In)** — From enhancement module, wired-ored with LINTRQ and inverted to become RST 5.5 to the processor. When low the processor is placed into an interrupt service routine.

L OPT RDY — **Low, Option Ready** — When low option puts processor into a wait state until it completes the bus operation.

L PI RDY — **Low, Plug In Ready** — When low enhancement module puts processor into a wait state until it completes the bus operation.

LRD — **Low, Read** — Asserted by the microprocessor to read data from an addressed memory location.

LWR — **Low, Write** — Asserted by the microprocessor to allow writing into an addressed memory location.

PWR DET — **Power Detector** — Input to processor at power on and power off which generates reset pulses for the processor and peripherals.

RDY — **Ready** — Input to microprocessor — when low wait states are inserted into the microprocessor cycle to give peripheral device time to complete its function.

RESET — Reset pulse from microprocessor to initialize peripherals to proper states at power up or power down.

RST 5.5 — **Restart 5.5** — Prioritized Interrupt Input to the Microprocessor — When pulled high by peripheral device normal microprocessor routine is interrupted and the microprocessor is placed in an interrupt service routine. RST 5.5 is the lowest priority restart interrupt.

RST 6.5 — **Restart 6.5** — Prioritized Interrupt Input to the Microprocessor - When pulled high by peripheral device normal microprocessor routine is interrupted and the microprocessor is placed in an interrupt service routine.

Service Sheet 18. Component Locator
P/O Processor Board, Microprocessor Circuits

SERVICE SHEET 18 MNEMONICS (CONT'D)

RST 7.5	**Restart 7.5** — Prioritized Interrupt Input to the Microprocessor - When pulled high by peripherial device normal microprocessor routine is interrupted and the microprocessor is placed in an interrupt service routine. RST 7.5 is the highest priority restart interrupt.
SID	**Serial Input Data** — Normally tied high — Pulled low during signature analysis rountine.
SOD	**Serial Output Data** — Test signal used only during signature analysis routine.
S0-S1	**Status Bits 0 and 1** — Output of microprocessor -S1 is used in signature analysis. S0 is not used.

SERVICE SHEET 18 — THEORY OF OPERATION

8085 Microprocessor. The microprocessor (A4U39) intergrated circuit is the primary logic element required for software execution. This device is sequenced through the software instructions in a synchronous fashion at an execution speed which is determined by the frequency of the clock oscillator.

The microprocessor continuously executes programs stored in ROM memory, and is continuously exercising the bus. As each instruction of the program is executed, the address of the instruction is placed on the address bus (A0 - A15) and is decoded by the address decoding logic to select one of the ROM memory devices. The selected ROM then places the instruction onto the data bus (AD0 - AD7) where the data is read and internally latched into the microprocessor. The instruction is interpreted, and the processing procedes. Some instructions may require additional bytes of information to be read into the microprocessor from either ROM, RAM, or an I/O port. In this case additional read cycles would be performed by the microprocessor by again placing an address byte on the A0-A15 lines. The addressed device would then place the data on the Address/Data bus, AD0-AD7.

Other instructions fetched during the first (or op code fetch) cycle will cause one or more bytes of data to be output from an internal register of the microprocessor to either a RAM or IO location (data cannot be output to a ROM location). This type of operation is called a WRITE CYCLE, whereas the first two operations are called FETCH or READ CYCLES. Again the microprocessor outputs to A0 - A15 the location in RAM or IO to be accessed. However, during a write cycle the microprocessor drives the lines AD0 - AD7. The selected device then latches or stores the data on AD0-7 into the proper RAM or IO register.

The OP code FETCH, READ and WRITE cycles are the essence of the operation of the microprocessor. These three transactions are controlled by the address bus A0 - A15, the data bus AD0 AD7, and the control bus, which includes ALE, LRD, LWR, IO/LM, RESET, and CLK. These last six signals are asserted by the mic.oprocessor during each bus cycle to control the direction and timing of the data flow on the bus. ALE (Address Latch Enable) is pulsed at the beginning of each cycle and is used to latch the lower eight bits of the address. These bits are presented by the microprocessor onto the data bus AD0-AD7 during this portion of the cycle, and on the trailing edge of ALE, are latched onto the address bus with an external latch (A4U46). Then for the rest of the bus cycle, AD0-AD7 will contain data to or from the processor. The IO/LM line will also go high or low at the beginning of the cycle. This line is used by the address select logic, and by certain IO devices, to qualify the data on A0-A15 as either an IO or memory address. Thus, should a ROM location and an IO port both be selected for a given pattern on A0 - A15, the IO/LM line will determine which device is the object of the bus transaction. The signals LRD and LWR are used to strobe the data contained on AD0-AD7 into either the microprocessor (LRD) or into a RAM or IO location (LWR). In both cases, the trailing edges of the pulses are used to sample the state of the data bus. The CLK signal is used to determine when ALE, LRD, LWR, and IO/LM occur, and is a divide by two derivative of the X1 clock input to the microprocessor. This signal is also used as a master timing reference for digital to analog conversion and for synchronous communication to the horizontal system of the scope. RESET occurs only during power-up and power-down sequences and is used to initialize all devices external to the microprocessor. RESET occurs whenever the PWRDET input to the microprocessor goes low.

In addition to these three buses, a set of additional control signals are used by the microprocessor. These are HOLD, HLDA, RDY, RST5.5, 6.5, and 7.5. The HOLD signal is an input used to request the microprocessor to release control of the bus (A0-A15, AD0-AD7, LRD, LWR) so that the bus can be controlled by the DMA (Direct Memory Access) controller (A4U31). The DMA controller raises HOLD high and, when the microprocessor recognizes the request and raises HLDA (hold acknowledge) high, executes a read or write operation to/from memory and I/O. When the DMA is complete, HOLD is dropped low, and HLDA goes low, thus indicating the processor is now back in control. It is important to note that during a HOLD cycle all address and data outputs from the microprocessor and its associated buffers and latches are three-stated so that the DMA controller can assert those lines.

The RDY input is another input to the microprocessor to control the operation of the bus in a significantly different way from HOLD. If RDY is pulled low by an external device during a READ or WRITE CYCLE, this indicates to the microprocessor that the device being accessed requires additional time in order to complete the data transaction. Therefore, when RDY goes low (indicating not ready), the processor maintains the state of the address bus A0 A15, and continues to assert either LRD or LWR until the accessed device restores RDY high (indicating now ready). The READ or WRITE cycle then continues normally. During the time that RDY is low, the processor executes WAIT states, which differs from a HOLD state in that a HOLD state causes the address and data bus to be three-stated, whereas a WAIT state simply causes the address and data bus to maintain their present state until the RDY line goes high. Another important difference is that the RDY input is a wire-ored type signal, so that more than one open-collector device can exercise the line, whereas HOLD is an active high signal that is exercised only by the DMA controller. Within the 1980 mainframe, the only device which control RDY is the DAC Refresh Controller (DRC), which controls memory accesses to the NV RAM. However, RDY is also available from the enhancement module and the Digital Waveform Storage Option.

There are three other inputs to the microprocessor which can modify normal operation. These are RST 5.5, 6.5, and 7.5. The lines are vectored interrupt request inputs. When one of these lines is asserted high, normal program execution in the microprocessor is "interrupted" at the completion of the current instruction. If the interrupt is internally "enabled" by the software the processor will jump to one of three fixed locations in ROM (depending on which RST input occurs) and begin program execution there. As part of the interrupt cycle, the address of the next instruction that would have been executed had the interrupt not occurred is "saved" automatically within a designated area of RAM called the stack (A4U32,A4U33 on Service Sheet 23). The address of the stack is defined internally within the microprocessor with a 16 bit register called the stack pointer. Thus, as part of the interrupt cycle, the address stored in the stack pointer is output to the address bus and two memory write cycles are executed, sequentially storing the upper and lower bytes of the address of the next instruction in the interrupted program. As each byte is stored, the microprocessor automatically decrements the value of the stack pointer so that the bytes are stored in adjacent locations within the RAM, and so that the stack pointer is always pointing to the last RAM location in which a stack storage operation occurred.

Each of the three RST interrupts are caused by different hardware events. The programs which start at the three vector locations perform special tasks. Once these tasks are completed, the program will execute a return instruction. This instruction performs an inverse of the stack operation which was automatically executed during the interrupt sequence. The contents of the stack pointer again appear on the address bus and two memory read cycles are performed to retrieve the address of the next instruction of the interrupted program. As each byte is read the stack pointer is incremented by the microprocessor. The two retrieved bytes are internally loaded into the program counter within the microprocessor. This is a register which always contains the address of the next instruction to be fetched. The interrupted program then resumes execution, and the stack pointer is automatically reset to point to the next available stack location in RAM.

The three RST inputs are generated by the following hardware events: RST 7.5 is the output of the 8155 programmable timer circuit (A4U16 on Service Sheet 21). This timer can be preset to divide the processor clock by a 14 bit binary value. When this timer counts down to 0, a RST 7.5 interrupt will occur. This timer is used by the software to make accurate timing measurements during calibration, and for other time-related routines. RST 6.5 is an output from the video controller (A4U19 on Service Sheet 23), used to flag the processor that a video frame is nearing completion, and that the DMA controller (A4U31 on Service Sheet 23), which is used to transfer data into the video controller, must be re-initialized by the software. RST 5.5 is a general purpose interrupt which may originate from the HP-IB or enhancement modules and is configured as a wire-ored signal via an external inverter.

Crystal-Controlled Clock. The clock oscillator provides three functions within the 1980. The primary function is to provide a single phase TTL level clock source to the microprocessor X1 input. Secondly, the oscillator provides the time-base reference for all time dependent measurements within the 1980. Thirdly, a clock source is provided which determines the dot and frame rates for the character generator.

The oscillator is actually three separate circuits, which are: (1) the oscillator amplifier with a quartz crystal feedback element, (2) an output amplifier to convert the oscillator amplifier's low-level output to a TTL compatible signal, and (3) a counter to divide the 10 MHz oscillator frequency to a 3.333333 MHz, 33% duty cycle TTL signal for use on the microprocessor (A4U39).

The oscillator amplifier consists of a dual ECL gate (A4U14). One gate is used for the actual oscillator feedback loop, the other as an output buffer to drive the TTL converter section (A4U6). Two complimentary outputs are available from each gate. The noninverting output of the oscillator is used to drive the positive feedback loop, with the 10 MHz crystal operating in a series resonant mode (0 phase shift through a feedback element).

The inverting output of the oscillator gate provides a signal take-off from the oscillator loop, thus isolating signal load from the oscillator loop. This ECL level signal drives the input to the second ECL gate. The two outputs of this gate are then used to drive the base inputs of two transistors (A4Q16, A4Q15) connected as a differential pair. This differential configuration is to minimize the current switching through the +5 volt supply, and to provide two TTL level 10 MHz signals for use by the microprocessor and video controller.

One 10 MHz TTL output is then applied to a counter (A4U6), which performs a divide by 3 operation on its input clock. The QB output controls the load operation to the counter, and when QB goes low, the counter outputs are set to the state 0010 with the next leading edge of the clock.

The 10 MHz TTL output from A4Q16 is used to toggle a D flip flop (A4U8B), providing a 5 MHz 50% duty cycle clock used to define the dot rate for the character generator.

Bus Buffers. There are four bus buffer devices employed to enhance the bus drive capability of the microprocessor (A4U39). Two drivers are required to drive the 16 bit address bus, one bidirectional transceiver is used to drive the data bus, and an additional driver is employed to drive the control bus.

One of the address bus buffers is A4U59 and is used to buffer the A8-A15 outputs of the microprocessor. The other address bus buffer is A4U46 and is used to capture the lower eight address bits from the AD0-AD7 outputs of the microprocessor at the beginning of each bus cycle. The ALE output of the microprocessor is used to gate this device. The outputs of this device drive the signals A0-A7, the lower half of the 16 bit address bus.

A4U57 a bi-directional bus transceiver is used to buffer the AD bus. The LRD input is used to control the buffer direction. When high, the transmission path is from left to right. The control bus is buffered by A4U40. The control lines include ALE, IO/M, RD, WR, RESET, CLK, and HLDA.

During a DMA cycle, the address and data bus buffers are three stated so that the DMA controller (A4U31) may exercise these lines. The HLDA signal is used to control the output enables of all of these devices, and when HLDA goes high, all of these devices are three-stated. However, on the control bus buffer, only the IO/LM, LRD, and LWR lines are three-stated during DMA, while the CLK, RESET, HLDA, and ALE outputs of the buffer remain active.

It should be noted that the bi-directional transceiver buffering the AD bus from the microprocessor performs an additional function. This device isolates the system data bus from the microprocessor data bus during signature analysis.

PROCESSOR BOARD SIGNATURE ANALYSIS

Note
Remove Expansion Module before performing tests.

ROM/RAM Self Test

a. Set instrument power to off.

b. Signature Analyzer connections:

START ⎍ to TP2 (SOD)
STOP ⎍ to TP2 (SOD)
CLOCK ⎾ to TP4 (ALE)

c. Set rear panel CAL switch to the Unprotected position.

d. Set S1-A to closed.

e. Set instrument power to on.

f. +5V signature is 60UF if test has passed. If test has failed, compare +5V signature displayed to signatures listed in step g.

g.

SIGNATURE	TEST FAILED AT
2A2C	U32 and U33 (stack)
454H	U26 (ROM 0)
0F60	U27 (ROM 2)
P204	U28 (ROM 4)
8U93	U29 (ROM 6)
AF62	U30 (ROM 8)
1069	U17 (I/O ROM)
H05C	U18 (I/O ROM)
FC35	U16 (Scratchpad RAM-I/O)
H2U9	U32 and U33 (Character RAM)
H80P	U34 and U36 (Feature RAM)
P2H5	U35 and U37 (Store/Recall RAM)
A307	U42 and U43 (Non-volatile RAM)

h. Set S1-A to open.

i. Set rear panel CAL switch to the Protected position.

j. If the test failed at a device, perform Test 5 on Service Sheet 20 and Tests 1 through 4 on Service Sheets 18 and 19 to isolate the problem. The most common failures will be shorted address or data bus or a bus conflict (more than one device being chip-enabled at a time). If a bus conflict is indicated, trigger a scope on the chip select of the apparently bad device and look at all other bus device chip selects to locate the failure. If the bus appears to be shorted, lift bus devices one at a time until the short is located.

SERVICE SHEET 18 SIGNATURE ANALYSIS

Note

Remove Expansion Module before performing tests.

TEST 1. Bus Test (Service Sheets 18 and 19)

a. Set instrument power to off.
b. Signature Analyzer connections:
START ⅂ to TP6 (A15)
STOP ⅂ to TP6 (A15)
CLOCK ⅂ to TP4 (ALE)
c. Set S1-B and S1-C to closed.
d. Set instrument power to on.
e.

TEST POINT		SIGNATURE	SS/GRID LOC
Probe to +5V		0001	
1-A	(U39-12)	UUUU	18/B4
1-B	(U39-13)	5555	
1-C	(U39-14)	CCCC	
1-D	(U39-15)	7F7F	
1-E	(U39-16)	5H21	
1-F	(U39-17)	0AFA	
1-G	(U39-18)	UPFH	
1-H	(U39-13)	52F8	
1-J	(U39-21)	HC89	
1-K	(U39-22)	2H70	
1-L	(U39-23)	HPP0	
1-M	(U39-24)	1293	
1-N	(U39-25)	HAP7	
1-P	(U39-26)	3C96	
1-Q	(U39-27)	3827	
1-R	(U39-28)	755U	
1-S	(U57-18)	UUUU	18/B6
1-T	(U57-17)	5555	
1-U	(U57-16)	CCCC	
1-V	(U57-15)	7F7F	
1-W	(U57-14)	5H21	
1-X	(U57-13)	0AFA	
1-Y	(U57-12)	UPFH	
1-Z	(U57-11)	52F8	
1-AA	(U46-2)	UUUU	18/C6
1-AB	(U46-5)	5555	
1-AC	(U46-6)	CCCC	
1-AD	(U46-9)	7F7F	
1-AE	(U46-12)	5H21	
1-AF	(U46-15)	0AFA	
1-AG	(U46-16)	UPFH	
1-AH	(U46-19)	52F8	
1-AJ	(U59-18)	HC89	
1-AK	(U59-16)	2H70	
1-AL	(U59-14)	HPP0	
1-AM	(U59-12)	1293	
1-AN	(U59-9)	HAP7	
1-AP	(U59-7)	3C96	
1-AQ	(U59-5)	3827	
1-AR	(U59-3)	755U	
1-AS	(U4-15)	383A	19/B2
1-AT	(U4-14)	7631	
1-AU	(U4-13)	160U	
1-AV	(U4-12)	04UH	
1-AW	(U4-11)	CFHH	
1-AX	(U4-10)	57HH	
1-AY	(U4-9)	96F8	
1-AZ	(U4-7)	546U	
1-BA	(U5-9)	A640	19/B2
1-BB	(U5-10)	C55F	
1-BC	(U5-11)	2718	
1-BD	(U5-12)	A2FH	
1-BE	(U5-6)	0PC5	19/C2
1-BF	(U5-7)	5969	
1-BG	(U10-15)	logic 0	19/C3
1-BH	(U10-9)	1U61	
1-BJ	(U10-10)	CHAH	

f. Set S1-B and S1-C to open.

TEST 2. Control Buffer Test (Service Sheet 18)

a. Set instrument power to off.
b. Signature Analyzer connections:
START ⅃ to TP3 (S1)
STOP ⅃ to TP3 (S1)
CLOCK ⅃ to TP1 (3.333333 MHz)
c. Set S1-B to closed.
d. Set instrument power to on.
e.

TEST POINT		SIGNATURE	SS/GRID LOC
Probe to +5		7339	
2-A	(U39-37)	H117	18/B4
2-B	(U39-3)	logic 0	
2-C	(U39-31)	70C1	
2-D	(U39-32)	1F6P	
2-E	(U39-30)	4291	
2-F	(U39-34)	logic 0	
2-G	(U39-38)	logic 0	
2-H	(U40-7)	H117	18/A5
2-J	(U40-5)	logic 0	
2-K	(U40-14)	70C1	
2-L	(U40-16)	1F6P	
2-M	(U40-3)	4291	
2-N	(U40-18)	logic 0	
2-P	(U40-9)	logic 0	

f. Set S1-B to open.

TEST 4. Chip Enable Test (Service Sheets 18 and 19)

a. Set instrument power to off.
b. Signature Analyzer connections:
START ⅂ to TP6 (A15)
STOP ⅂ to TP6 (A15)
CLOCK ⅃ to TP5 (LRD)
c. Set S1-B and S1-C to closed.
d. Set instrument power to on.
e.

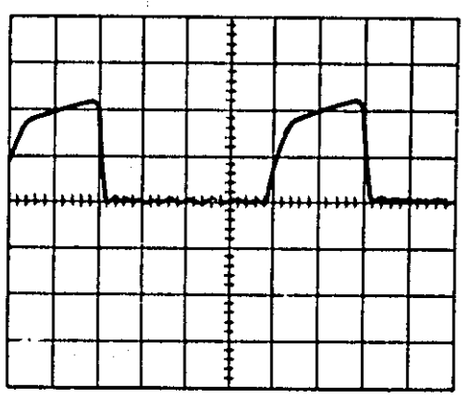
TEST POINT		SIGNATURE	SS/GRID LOC
Probe to +5V		0001	
4-A	(U57-2)	0001	18/B5
4-B	(U57-3)	0001	
4-C	(U57-4)	0001	
4-D	(U57-5)	0001	
4-E	(U57-6)	0001	
4-F	(U57-7)	0001	
4-G	(U57-8)	0001	
4-H	(U57-9)	0000	
4-J	(U3-18)	383A	19/B3
4-K	(U3-3)	7631	
4-L	(U3-16)	160U	
4-M	(U3-5)	04UH	
4-N	(U3-14)	CFHH	
4-P	(U3-7)	546U	
4-Q	(U3-9)	A640	
4-R	(U3-12)	C55F	
4-S	(A3U9-20)	54F5	7
4-T	(A3U10-20)	A711	7
4-U	(A3U11-20)	603C	7
4-V	(A3U12-20)	826U	7

f. Set S1-B and S1-C to open.

TP 1

Monitor
Oscilloscope
Setup

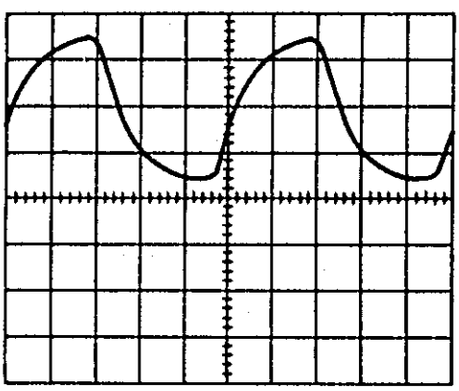
2 Volts/Div
.05 μSec/Div



Ⓐ

Monitor
Oscilloscope
Setup

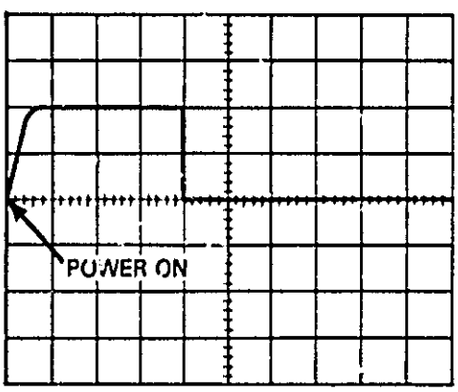
1 Volt/Div
.02 μSec/Div



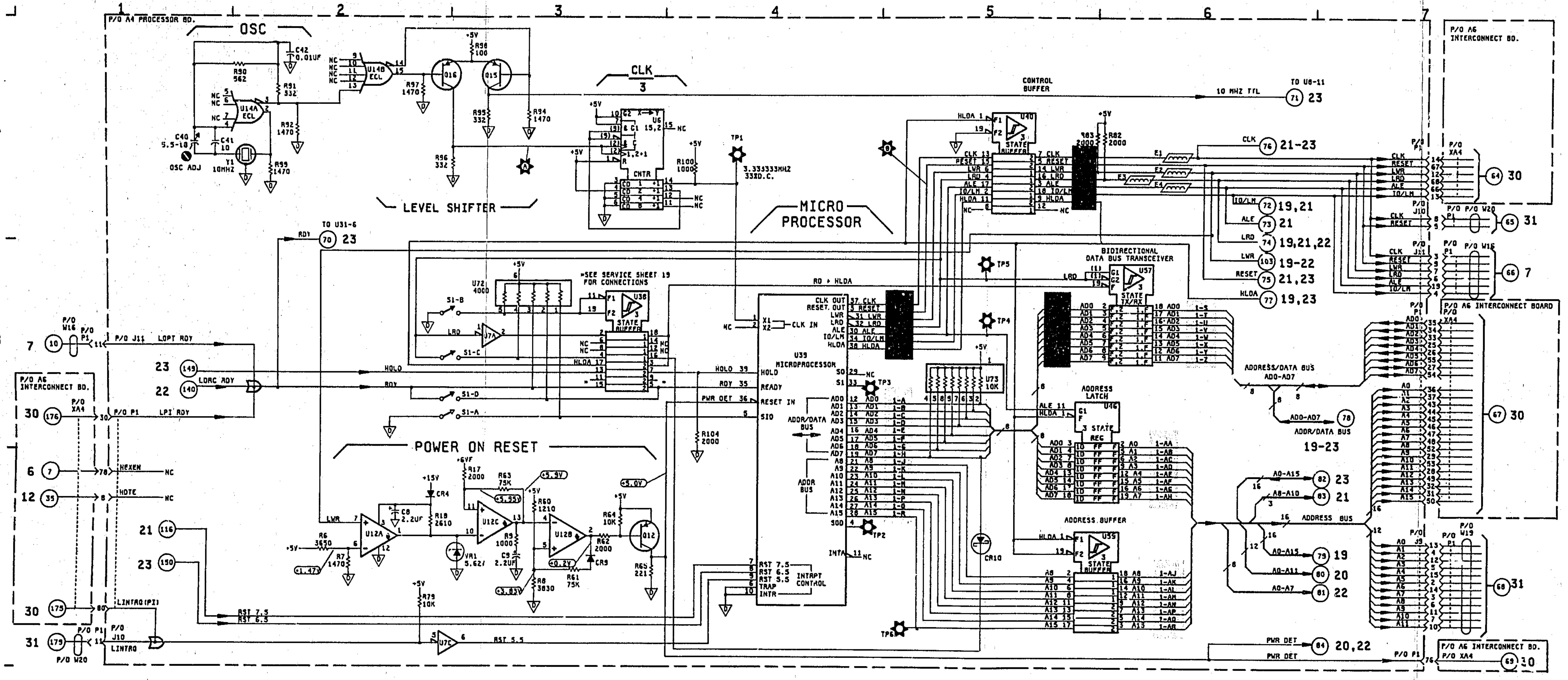
Ⓑ

Monitor
Oscilloscope
Setup

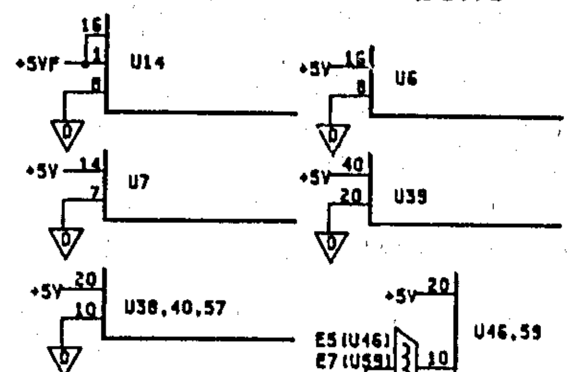
2 Volts/Div
50 mSec/Div



Service Sheet 18. Test Information
P/O Processor Board, Microprocessor Circuits



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. ECL LOGIC LEVELS ARE:
   -0.9V=LOGIC "1"=H
   -1.75V= LOGIC "0"=L

SWITCH NO.	FUNCTION
S1-A	START DSA EXERCISER ROUTINE
S1-B	FREE RUN MICROPROCESSOR
S1-C	FREE RUN OP CODE SELECT
S1-D	FREE RUN READY ENABLE

ALL SWITCHES OPEN FOR NORMAL SYSTEM OPERATION

PARTS ON THIS SCHEMATIC

P/O A4	P/O A6
C8,9,40-42,44 CR4,9,10 E1-5,7 P/O J9,10,11 L6 P/O P1 Q12,15,16 R6-9,17,18,60-65,79,82,83,90-92, 94-100,104 S1 TP1-6 U6,7A,7C,12A,12B,12C,14,38-40,46 57,59,72,73 VR1 Y1	P/O XA4 **CHASSIS** P/O W16,P/O W19 P/O W20

DELETED: C44,L6,E6

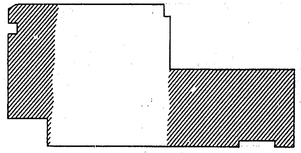
1980/114/4/7/81

18

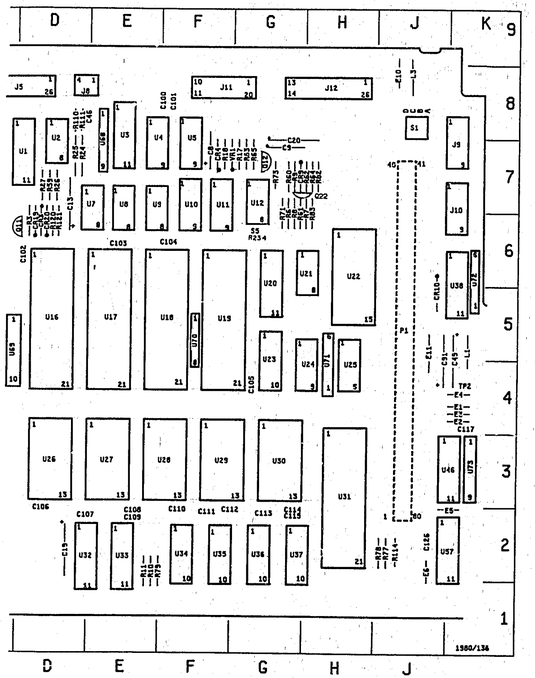
Service Sheet 18. Schematic Diagram
P/O Processor Board, Microprocessor Circuits

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	R-4	C114	G-2	J2	O-2	R24	D-7	R97	B-5	R231	C-8	U32	D-2		
C6	R-5	C115	G-2	J4	B-8	R25	D-7	R98	B-5	R232	C-9	U33	E-2		
C7	R-5	C116	L-6	J6	C-8	R26	D-7	R99	C-6	R233	M-2	U34	F-2		
C8	F-7	C117	K-4	J8	B-3	R27	C-7	R100	C-7	R234	G-8	U35	F-2		
C9	G-7	C118	L-4	J7	B-2	R30	C-4	R104	L-4	S1	J-8	U36	G-2		
C10	A-6	C119	M-3	J8	D-8	R31	B-4	R107	S-4	S2	M-2	U37	G-2		
C11	L-4	C120	N-3	J9	K-7	R32	B-4	R108	C-3	S3	M-2	U38	K-6		
C13	P-4	C121	N-3	J10	K-7	R33	C-4	R109	C-3	S4	N-3	U39	K-4		
C14	P-4	C122	K-2	J11	F-8	R34	C-4	R110	D-8	S5	G-8	U40	L-4		
C15	P-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	C-7	U41	M-4		
C16	N-4	C124	M-3	L1	K-6	R36	B-4	R112	R-2	TP2	K-4	U42	M-4		
C17	P-4	C125	L-3	L3	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	N-4		
C18	C-5	C126	J-2	L4	C-4	R40	R-4	R114	J-2	TP4	K-2	U44	O-5		
C19	D-2	C127	M-2	P1	J-5	R41	R-4	R120	D-6	TP5	L-5	U45	R-5		
C20	G-7	C128	M-2	Q1	C-4	R42	R-5	R121	D-6	TP6	L-2	U46	K-3		
C21	P-4	C129	N-2	Q2	B-4	R43	R-5	R200	B-3	U1	D-7	U47	L-3		
C28	P-5	C130	N-2	Q3	B-4	R44	O-4	R201	B-3	U2	D-7	U48	N-3		
C29	P-4	C131	P-2	Q4	C-4	R45	O-5	R202	B-3	U3	E-7	U49	N-3		
C30	P-4	C132	M-1	Q5	C-4	R46	O-4	R203	B-3	U4	E-7	U50	N-3		
C31	P-4	C133	M-1	Q6	C-4	R47	O-5	R204	B-3	U5	F-7	U51	L-4		
C32	L-6	C134	N-1	Q7	B-4	R48	O-4	R205	B-3	U6	C-7	U57	M-2		
C40	C-6	C135	N-1	Q8	B-4	R49	O-4	R206	A-3	U7	E-7	U63	N-2		
C41	C-5	CR1	S-4	Q9	P-3	R50	O-5	R207	B-3	U8	E-7	U64	N-2		
C42	B-5	CR2	R-5	Q11	D-9	R51	O-5	R208	B-3	U9	E-7	U65	P-2		
C43	B-5	CR3	D-8	Q11	D-9	R52	O-4	R209	B-3	U10	F-7	U66	P-5		
C45	L-5	CR4	F-7	Q12	G-7	R59	D-7	R210	B-3	U11	F-7	U67	K-2		
C46	D-8	CR9	G-7	Q15	B-5	R60	G-7	R211	B-7	U12	G-7	U68	K-2		
C47	K-5	CR10	J-5	Q16	B-5	R61	G-6	R212	B-7	U13	B-5	U69	L-2		
C49	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	B-6	U60	L-2		
C50	C-2	CR14	C-3	Q19	C-3	R63	G-7	R214	B-7	U15	B-4	U61	M-2		
C51	C-6	CR15	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2		
C52	K-5	CR16	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-5	U63	N-2		
C91	J-4	CR17	B-7	Q22	G-7	R71	G-6	R217	C-7	U18	F-5	U64	P-2		
C100	F-8	CR18	B-7	R1	R-5	R73	G-7	R218	B-8	U19	F-5	U65	R-2		
C101	F-8	CR19	D-8	R3	D-5	R77	J-2	R219	B-8	U20	G-5	U66	Q-3		
C102	D-6	CR20	D-8	R6	G-8	R78	J-2	R220	B-8	U21	H-5	U67	S-3		
C103	E-6	E1	K-4	R7	H-6	R79	E-2	R221	J-8	U22	H-6	U68	E-7		
C104	F-6	E2	K-4	R8	G-8	R82	H-7	R222	B-8	U23	G-4	U69	C-5		
C105	G-4	E3	K-4	R9	G-7	R83	H-6	R227	B-8	U24	H-4	U70	F-5		
C106	D-2	E4	K-4	R10	E-2	R85	L-3	R224	B-8	U25	H-4	U71	N-4		
C107	E-2	E5	K-2	R11	E-2	R90	C-5	R225	B-8	U26	D-3	U72	K-5		
C108	E-2	E6	J-2	R13	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3		
C109	E-2	E7	K-2	R14	P-3	R92	C-5	R227	A-8	U28	F-3	U74	P-5		
C110	F-2	E8	L-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	F-7		
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4		
C112	F-2	E10	J-5	R21	S-4	R95	C-5	R230	C-8	U31	H-3	Y1	C-6		
C113	G-2	E11	J-5	R22	S-4	R96	B-5								



A4



SERVICE SHEET 19 MNEMONICS

A0-A15 — Address Lines 0-15 — A0-A7 are developed from the AD0-AD7 bus. A8 through A15 are most significant 8 bits of address.

AD0-AD7 — Address/Data bus — Microprocessor bidirectional bus. Data on this bus can be the least significant 8 bits of address.

CHAR RAM — Character RAM — Chip select decoded from address to select character RAMs, A4U32 and A4U33.

CSM0 — Chip Select Memory 0 — Chip select decoded from address to select ROM0, A4U26.

CSM1 — Chip Select Memory 1 — Chip select decoded from address to select ROM1, A4U27.

CSM2 — Chip Select Memory 2 — Chip select decoded from address to select ROM2, A4U28.

CSM3 — Chip Select Memory 3 — Chip select decoded from address to select ROM3, A4U29.

CSM4 — Chip Select Memory 4 — Chip select decoded from address to select ROM4, A4U30.

CSIO0 — Chip Select IO 0 — Chip select decoded from address to select IO device 0, A4U19 (Video Controller).

CSIO1 — Chip select IO 1 — Chip select decoded from address to select IO device 1, A4U31 (DMA Controller).

FRAM — Feature RAM — Chip select decoded from address to select feature RAMs, A4U34 and A4U36.

HLDA — Hold Acknowledge — Acknowledges a DMA Controller hold request when control of the address and data buses are available for control by the DMA Controller — also places proper levels to various devices during DMA cycles.

IBIO — Interface Bus IO — Chip select decoded from address to select HP-IB IO, A23U3.

IBROM — Interface Bus ROM — Chip select decoded from address to select HP-IB ROM, A23U1.

IO/LM — High, IO/Low, Memory — selects either IO or Memory devices.

IO/RAM — IO/RAM Chip Select — Chip select decoded from address to select IO/RAM, A4U16.

IO/ROM 5 — IO/ROM 5 Chip Select — Chip select decoded from address to select IO/ROM 5, A4U17.

IO/ROM 6 — IO/ROM 6 Chip Select — Chip select decoded from address to select IO/ROM 6, A4U18.

LIOR — Low, IO Read — tells the selected IO device to output a byte of data on the AD0-AD7 lines. Usually controlled by the DMA Controller.

LIOW — Low, IO Write — indicates to the selected IO device that a data byte is available on the AD0-AD7 lines. The IO device will then latch the data. Usually controlled by the DMA Controller.

LMEMR — Low, Memory Read — causes the addressed memory location to be read. Usually controlled by the DMA Controller.

LMEMW — Low, Memory Write — causes the memory device to write the data byte on the AD0-AD7 lines to the addressed memory location.

LRD — Low, Read — Asserted by the microprocessor to read data from an addressed memory location.

LWR — Low, Write — Asserted by the microprocessor to direct writing into an addressed memory location.

NVRAM — Nonvolatile RAM — Chip select decoded from address to the DRC — allows the DRC to read or write to the memory it controls, A4U42 and A4U43.

SRRAM — Store/Recall RAM Chip Select — Chip select decoded from address to the Store/Recall RAM, A4U35 and A4U37.

Service Sheet 19. Component Locator
P/O Processor Board, Read/Write and Address Decoder

SERVICE SHEET 19 — THEORY OF OPERATION

Address and Control Bus Decoding logic. The function of the address decoding logic is to decode the high order bits of the address bus into a set of unique enable signals (chip enables) which then select a unique memory or IO device to decode the remaining lower order address lines and respond to the bus control lines (LRD, LWR, IO/LM, etc). For each IO and memory device there exists a unique chip enable signal. A given device can respond to a read or write request if and only if its chip enable is true (usually low) when LRD or LWR occurs.

The LRD, LWR, IO/LM and HLDA signals from the microprocessor are used to form four additional signals; two memory access strobes, and two IO access strobes. These lines LMEMR, LMEMW, LIOR, and LIOW, form a secondary set of LRD and LWR pulses, each qualified by the state of IO/LM. This decoding is implemented with A4U25 a 3 to 8 line decoder. An important point to note is that during DMA bus transactions, LMEMR, LMEMW, LIOR, and LIOW are controlled by the DMA controller (A4U31 on Service Sheet 23). Note that the lines LRD and LWR are three-stated by A4U40 (on Service Sheet 18) during DMA. These various read and write strobes are employed throughout the system, including the address decoding logic.

The address decoding logic is implemented with three different decoding devices, each of which has a unique characteristic.

The highest level of decoding is implemented with A4U4 a 3 to 8 line decoder. This device is enabled whenever the most significant address bit, A15, is low. The next three MSB's A14, A13, and A12 are then decoded into 8 possible combinations. Each output of the decoder decodes 4K bytes of address space. The first five outputs (0G-4G) are used as the chip enables for the five 4K×8 ROMs. The next output, 5G, is used to enable a 4K address space for the two 8355 IO/ROMs. In order to provide two unique chip selects for these devices further decoding using the A11 address signal is implemented with A4U5A a dual 2 to 4 line decoder. The signal 5G from A4U4 is used to enable a 2 to 4 line decoder, and the state of A11 determines whether the 2G or the 3G output of this decoder goes true. The other input to this 2 to 4 line decoder is tied high.

The 6G output of A4U4 selects the 4K address region containing all of the mainframe RAM. This signal enables the other half of the 2 to 4 line decoder (A4U5B), with the next two lower order address lines, A11 and A10, driving the 2 and 1 inputs to this decoder. The 1st 1K section controlled by the 0G output enables either the 8155 IO/RAM (A4U16), or the 256 byte CMOS NVRAM (A4U42 and A4U43), which is used to refresh the DAC. This 0G output enables one half of A4U10 a dual 2 to 4 line decoder. The next lower order address bit, A9, then selects either the IO/RAM, or the NVRAM. Note that in order for this side of A4U10 to be active, the IO/LM line must be low, designating the bus transaction as a memory cycle. During IO, neither of the chip selects are activated, however the other half of A4U10 is enabled. The two outputs, 0G and 1G, of A4U10 are then enabled whenever the 6G output of A4U4 goes true to drive the IO/RAM chip enable. This is necessary since IO addresses are only 8 bits, a larger address space is required in order to access all of A4U16's IO registers than is required to access the 256 bytes of RAM in A4U16. The two outputs 0G and 1G are wire-ored so that A4U16 is enabled during IO accesses regardless of the states of A11, A10, or A9, and are also tied to the memory access chip enable to form a single chip enable to A4U16.

The other three 1K chip enables derived from A4U5B are used to enable the character RAM (A4U32 and A4U33), the feature RAM (A4U34 and A4U36), and the store/recall RAM (A4U35 and A4U37), all of which are 1K in length.

The last 4K chip enable from A4U4 is used as a ROM chip select for the HP-IB card, which has a 4K X 8 ROM for HP-IB software.

A number of chip enables derived from this set of decoders require additional gating with either the LRD or LWR pulses in order to guarantee that no bus conflict will exist during the first state of a bus cycle, when AD0-AD7 are being driven by microprocessor (A4U39). These devices have no independent output enable pin, and therefore must not be enabled to drive the bus until the lower 8 address bits are latched at the end of ALE. To implement this, an octal three-state buffer (A4U3) is used. The outputs of this buffer are always three-stated and externally pulled high except during LMEMR and LMEMW, when the outputs are allowed to follow the inputs. When one of the chip enables is low, during LMEMR or LMEMW the output of A4U3 will drive low.

As stated previously, IO accesses differ from memory accesses in that IO port addresses are only eight bits wide. Therefore, when an I/O read or write cycle occurs, both the upper and lower bytes of the address bus will hold the same 8 bit IO port address. Since the high order address lines are used for both IO port and memory address decoding, certain distinctions are made concerning devices which contain both memory and IO, since the amount of memory address space to be decoded differs from the amount of IO address space required to be decoded. Three such IO/memory devices are used in the processor system; one 8155 IO/RAM (A4U16) (256 bytes) and two 8355 IO/ROM's (A4U17,18) (2K bytes each). As noted earlier, the RAM portion of the 8155 (A4U16) is enabled within a 512 byte space of the 16 bit memory address, but during IO, the lower four bits of the 8 bit IO address are left undefined so that 16 possible IO port addresses are available to A4U16. The two IO/ROM (A4U17 and A4U18) chip enables each decode 2K bytes of memory address space, and 8 possible IO port address locations.

Three other IO port chip enables are also provided, each of which decodes 16 port locations within the 8 bit IO address. The chip enables CSIO0, CSIO1, and IBIO are the same decoder outputs which are used for ROM chip enables. This is allowable since the ROM chip enables are gated by LMEMR, which will not occur during IO cycles. Conversely, when these ROM's are accessed during memory read cycles (and LMEMR goes true) the IO devices which are also selected (the video controller (A4U19), the DMA controller (A4U31), and the HP-IB interface) all respond to LIOR or LIOW, which will never occur during memory access cycles. Thus, no conflict exists between IO devices and memory devices which use the same address space.

SERVICE SHEET 19 SIGNATURE ANALYSIS

Note

Remove Expansion Module before performing tests.

TEST 1. Bus Test (Service Sheets 18 and 19)

a. Set Instrument power to off.
b. Signature Analyzer connections:
START ⌝ to TP6 (A15)
STOP ⌝ to TP6 (A15)
CLOCK ⌝ to TP4 (ALE)
c. Set S1-B and S1-C to closed.
d. Set Instrument power to on.
e.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		0001		
1-A	(U39-12)	UUUU	18/B4	
1-B	(U39-13)	5555		
1-C	(U39-14)	CCCC		
1-D	(U39-15)	7F7F		
1-E	(U39-16)	5H21		
1-F	(U39-17)	0AFA		
1-G	(U39-18)	UPFH		
1-H	(U39-19)	52F8		
1-J	(U39-21)	HC89		
1-K	(U39-22)	2H70		
1-L	(U39-23)	HPP0		
1-M	(U39-24)	1293		
1-N	(U39-25)	HAP7		
1-P	(U39-26)	3C96		
1-Q	(U39-27)	3827		
1-R	(U39-28)	755U		
1-S	(U57-18)	UUUU	18/B6	
1-T	(U57-17)	5555		
1-U	(U57-16)	CCCC		
1-V	(U57-15)	7F7F		
1-W	(U57-14)	5H21		
1-X	(U57-13)	0AFA		
1-Y	(U57-12)	UPFH		
1-Z	(U57-11)	52F8		
1-AA	(U46-2)	UUUU	18/C6	
1-AB	(U46-5)	5555		
1-AC	(U46-6)	CCCC		
1-AD	(U46-9)	7F7F		
1-AE	(U46-12)	5H21		
1-AF	(U46-15)	0AFA		
1-AG	(U46-16)	UPFH		
1-AH	(U46-19)	52F8		
1-AJ	(U59-18)	HC89		
1-AK	(U59-16)	2H70		
1-AL	(U59-14)	HPP0		
1-AM	(U59-12)	1293		
1-AN	(U59-9)	HAP7		
1-AP	(U59-7)	3C96		
1-AQ	(U59-5)	3827		
1-AR	(U59-3)	755U		
1-AS	(U4-15)	383A	19/B2	
1-AT	(U4-14)	7631		
1-AU	(U4-13)	160U		
1-AV	(U4-12)	04UH		
1-AW	(U4-11)	CFHH		
1-AX	(U4-10)	57HH		
1-AY	(U4-9)	96F8		
1-AZ	(U4-7)	546U		
1-BA	(U5-9)	A640	19/B2	
1-BB	(U5-10)	C55F		
1-BC	(U5-11)	2718		
1-BD	(U5-12)	A2FH		
1-BE	(U5-6)	0PC5	19/C2	
1-BF	(U5-7)	5969		
1-BG	(U10-15)	logic 0	19/C3	
1-BH	(U10-9)	1U61		
1-BJ	(U10-10)	CHAH		

f. Set S1-B and S1-C to open.

TEST 3. Read/Write Decoder Test (Service Sheet 19)

a. Set Instrument power to off.
b. Signature Analyzer connections:
START ⌐ to TP3 (S1)
STOP ⌐ to TP3 (S1)
CLOCK ⌐ to U39-37 (CLK)
c. Set S1-B to closed.
d. Set Instrument power to on.
e.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		0UP7		
3-A	(U25-2)	logic 0	19/A1	
3-B	(U25-13)	09P8		
3-C	(U25-3)	0UUF		
3-D	(U25-1)	logic 0		
3-E	(U25-5)	logic 1	19/A2	
3-F	(U25-6)	logic 1		
3-G	(U25-11)	09P8		
3-H	(U25-10)	0UUF		
3-J	(U7-8)	001C	19/B2	
3-K	(U7-10)	060U		
3-L	(U21-13)	09U3		

f. Set S1-B to open.

TEST 4. Chip Enable Test (Service Sheets 18 and 19)

a. Set Instrument power to off.

b. Signature Analyzer connections:
START to TP6 (A15)
STOP to TP6 (A15)
CLOCK to TP5 (LRD)

c. Set S1-B and S1-C to closed.

d. Set Instrument power to on.

e.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		0001		
4-A	(U57-2)	0001	18/B5	
4-B	(U57-3)	0001		
4-C	(U57-4)	0001		
4-D	(U57-5)	0001		
4-E	(U57-6)	0001		
4-F	(U57-7)	0001		
4-G	(U57-8)	0001		
4-H	(U57-9)	0000		
4-J	(U3-18)	383A	19/B3	
4-K	(U3-3)	7631		
4-L	(U3-16)	160U		
4-M	(U3-5)	04UH		
4-N	(U3-14)	CFHH		
4-P	(U3-7)	546U		
4-Q	(U3-9)	A640		
4-R	(U3-12)	C55F		
4-S	(A3U9-20)	54F5	7	
4-T	(A3U10-20)	A711	7	
4-U	(A3U11-20)	603C	7	
4-V	(A3U312-20)	826U	7	

f. Set S1-B and S1-C to open.

P/O A4 PROCESSOR BOARD

READ/WRITE DECODER

"SEE SERVICE SHEET 18 FOR ALL OTHER CONNECTIONS"

HLDA (77)
LRD (74)
LWR (103)
IO/LM (72)
18

U25 DEMUX
U71 4000 +5V
U36 3 STATE BUFFER
U70, U7F, U21D
U3 3 STATE BUFFER
P/O U68 2200
CS0 CS1 CS2 CS3 CS4
SRAM FRAM (98) 20
(97) 20

LMEMW LMEMR LIOW LIOR
P/O J11 P/O P1 P/O W16 (85) 7
LIOW LIOR
P/O J10 P/O P1 P/O W20 (86) 31
P/O XA4 (87) 30
P/O A6 INTERCONNECT BD
LIOR (92) 23
LIOW (93) 23
LMEMR LMEMW (94)
CSIO0 (95)
CSIO1 (96) 23
IBIO
IBROM
P/O J10 P/O P1 P/O W20 (88)
(89) 31

U4 DEMUX
A15 A12 A13 A14 A9
1-A5 1-A7 1-AU 1-AV 1-AW 1-AX 1-AY 1-AZ

A10
U58 DEMUX 1-BA 1-BB 1-BC 1-BD
U10 60-3
IO/LM 1-BG
1-BH 1-BJ
P/O U68 2200
IO/RAM NVRAM (99) 21
(100) 22
CHAR RAM (101) 23

A11
USA DEMUX 1-BE 1-BF
IO/ROM 5 IO/ROM 6 (102) 21

ADDRESS DECODER

ADDRESS BUS A0-A15 (79) 16
ADDRESS/DATA BUS A00-A07 (78) 18

A00 A01 A02 A03 A04 A05 A06 A07
P/O J12 P/O P1 P/O W17 (90) 7
P/O J11 P/O P1 P/O W16
P/O J10 P/O P1 P/O W20 (91) 31

IC DEVICE POWER CONNECTIONS

+5V U7,21
+5V U4,5,10,25
+5V U3

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A4	P/O A6	CHASSIS
P/O J10,11,12 P/O P1 U3-5, 7D,7E,10, U21D,25 U60,71	P/O XA4	P/O W16-17, P/O W20

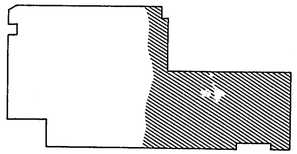
1980/117/10/30/81

19

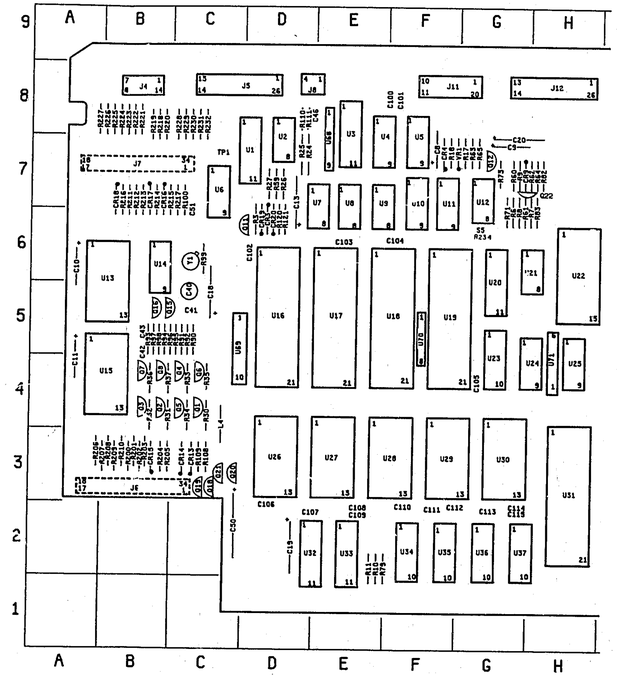
Service Sheet 19. Schematic Diagram
P/O Processor Board, Read/Write and Address Decoder
8-151

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	B-4	C114	G-2	J2	G-2	R24	D-7	R97	B-5	R231	C-8	U32	D-2		
C6	B-5	C115	G-2	J4	B-8	R25	D-7	R98	B-5	R232	C-8	U33	E-2		
C7	B-5	C116	L-6	J5	C-8	R26	D-7	R99	C-6	R233	M-2	U34	F-2		
C8	F-7	C117	K-4	J6	B-3	R27	D-7	R100	C-7	R234	G-8	U35	F-2		
C9	G-7	C118	L-4	J7	B-7	R30	C-4	R104	L-4	S1	J-8	U36	G-2		
C10	A-6	C119	M-3	J8	D-8	R31	B-4	R107	B-4	S2	M-2	U37	G-2		
C11	A-4	C120	N-3	J9	K-7	R32	B-4	R108	C-3	S3	M-2	U38	K-6		
C13	D-7	C121	N-3	J10	K-7	R33	C-4	R109	C-3	S4	N-3	U39	K-4		
C14	F-4	C122	K-2	J11	F-8	R34	C-4	R110	D-8	S5	G-8	U40	L-4		
C15	F-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	C-7	U41	M-4		
C16	K-4	C124	M-3	L1	K-8	R36	C-4	R112	F-2	TP2	K-4	U42	M-4		
C17	F-4	C125	L-3	L3	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	N-4		
C18	C-5	C126	J-2	L4	C-4	R40	R-4	R114	J-2	TP4	K-2	U44	G-8		
C19	D-2	C127	M-2	P1	J-5	R41	R-4	R120	D-6	TP5	L-5	U45	R-5		
C20	G-7	C128	M-2	Q1	C-4	R42	R-5	R121	D-6	TP6	L-3	U46	K-3		
C21	F-4	C129	N-2	Q2	B-4	R43	R-5	R200	B-3	U1	D-7	U47	L-3		
C28	F-5	C130	N-2	Q3	B-4	R44	Q-4	R201	B-3	U2	D-7	U48	N-3		
C29	F-4	C131	P-2	Q4	C-4	R45	Q-5	R202	B-3	U3	E-7	U49	N-3		
C30	F-5	C132	M-1	Q5	C-4	R46	Q-4	R203	B-3	U4	E-7	U50	N-3		
C31	F-4	C133	M-1	Q6	C-4	R47	Q-5	R204	B-3	U5	F-7	U51	S-4		
C32	L-5	C134	N-1	Q7	B-4	R48	Q-4	R205	B-3	U6	C-7	U52	M-2		
C40	C-5	C135	N-1	Q8	B-4	R49	Q-4	R206	A-3	U7	E-7	U53	N-2		
C41	C-5	CR1	B-4	Q9	P-3	R50	Q-5	R207	B-3	U8	E-7	U54	N-2		
C42	B-5	CR2	R-5	Q10	P-3	R51	Q-5	R208	B-3	U9	E-7	U55	P-2		
C43	B-5	CR3	D-8	Q11	D-8	R52	Q-4	R209	B-3	U10	F-7	U56	P-6		
C45	L-5	CR4	F-7	Q12	G-7	R59	D-7	R210	B-3	U11	F-7	U57	K-2		
C46	D-8	CR9	G-7	Q15	B-5	R60	G-7	R211	B-7	U12	G-7	U58	K-2		
C47	K-6	CR10	J-5	Q16	B-5	R61	G-8	R212	B-7	U13	B-5	U59	L-2		
C49	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	E-6	U60	L-2		
C50	C-2	CR14	C-3	Q18	C-3	R63	G-7	R214	B-7	U15	B-4	U61	M-2		
C51	C-6	CR15	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2		
C60	K-6	CR16	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-6	U63	N-2		
C61	J-4	CR17	B-7	Q22	G-7	R71	G-8	R217	C-7	U18	F-5	U64	P-2		
C100	F-8	CR18	B-7	R1	R-5	R73	G-7	R218	B-8	U19	F-5	U65	R-2		
C101	F-8	CR19	D-8	R3	D-5	R77	J-2	R219	B-8	U20	G-5	U66	Q-3		
C102	D-6	CR20	D-8	R6	G-8	R78	J-2	R220	B-8	U21	H-6	U67	S-3		
C103	E-6	E1	K-4	R7	H-6	R79	E-2	R221	B-8	U22	H-6	U68	E-7		
C104	F-6	E2	K-4	R8	G-6	R82	H-7	R222	B-8	U23	G-4	U69	C-5		
C105	G-4	E3	K-4	R9	G-7	R83	H-8	R223	B-8	U24	H-4	U70	F-6		
C106	D-2	E4	K-4	R10	E-2	R85	L-3	n224	B-8	U25	H-4	U71	H-4		
C107	E-2	E5	K-2	R11	E-2	R90	C-5	R225	B-8	U26	D-3	U72	K-5		
C108	E-2	E6	J-2	R13	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3		
C109	E-2	E7	K-2	R14	P-3	R92	C-6	R227	A-8	U28	F-3	U74	P-5		
C110	F-2	E8	L-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	F-7		
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4		
C112	F-2	E10	J-8	R21	S-4	R95	C-5	R230	C-8	U31	H-3	Y1	C-6		
C113	G-2	E11	J-5	R22	S-4	R96	B-5								



A4



SERVICE SHEET 20 MNEMONICS

A0-A11 — **Address Lines 0-11** — A0-A7 are developed from the AD0-AD7 bus. A8 through A11 are most significant 4 bits of address.

AD0-AD7 — **Address/Data bus** — Microprocessor bidirectional bus. Data on this bus can be the least significant 8 bits of address.

CSM0 — **Chip Select Memory 0** — Chip select decoded from address to select ROM0, A4U26.

CSM1 — **Chip Select Memory 1** — Chip select decoded from address to select ROM1, A4U27.

CSM2 — **Chip Select Memory 2** — Chip select decoded from address to select ROM2, A4U28.

CSM3 — **Chip Select Memory 3** — Chip select decoded from address to select ROM3, A4U29.

CSM4 — **Chip Select Memory 4** — Chip select decoded from address to select ROM4, A4U30.

FRAM — **Feature RAM** — Chip select decoded from address to select feature RAMs, A4U34 and A4U36.

LCMOSWR — **Low, CMOS RAM Write** — Write enable signal to the CMOS RAMs, A4U34 through A4U37. LWR is gated with PWR DET so that writing to these RAMs is only possible after power comes up to the proper level.

LWR — **Low, Write** — Asserted by the microprocessor to allow writing into an addressed memory location.

PWR DET — **Power Detector** — Input to processor at power on and power off which generates reset pulses for the processor and peripherals.

SRRAM — **Store/Recall RAM Chip Select** — Chip select decoded from address to the Store/Recall RAM, A4U35 and A4U37.

VBATT — **Battery Voltage** — Voltage that sustains NVRAM when instrument has been powered down.

Service Sheet 20. Component Locator
P/O Processor Board, Store/Recall RAM, Feature RAM, and Program ROM

SERVICE SHEET 20 — THEORY OF OPERATION

The mask RO.M' '44U26-A4U30) receive no control bus lines and have no independent output enable control. Therefore, in order to ensure ',at the- 4 devices respond only when a memory access to their address region occurs, the chip enables are gated with the LMEMR strobe. This gating of the chip enable also prevents these devices from prematurely driving the data bus during the time that the AD lines contain address infor-mat'on, which would occur had the chip enable been connected directly to the address decoder without gating by LMEMR.

Four CMOS RAMs are configured as two 1K×8 RAMs one of which is the feature RAM, the other being the store/recall RAM. The feature RAMs (A4U34,A4U36) is a 1K scratch pad RAM made available as buffer space for use by special feature software which is stored in one or more option ROMs on the gate board. The store/recall RAMs (A4U35,A4U37) are used by the mainframe software for storage of up to 8 different scope set-ups. Since these devices do not have an independent output enable, the chip enables are gated with LMEMR and LMEMW in the address decoding logic.

All four of these devices, as well as the two CMOS NVRAM's (A4U42 a J A4U43 on service sheet 22), have a continuous battery back-up power source so that the data is retained during power down periods. A special switching circuit is provided, as system power comes up, the load is shifted from the battery to the +5V powe supply. A voltage comparator controls this switch, as the +5 volt supply exceeds the battery supply, the comparator switches the output which turns on a PNP switch, which then saturates and provides a current path from +5V to the CMOS RAM and a full +5V VCC to the RAM. This is necessary for normal read and write operation.

As power goes down, the comparator switches off, and the battery begins suppling standby current. All of the CMOS RAM's (A4U34-A4U37) have a minimum VCC of 2.0V for data rentention. The battery, which consists of a single 3V lithium cell mounted on the rear panel, is interfaced to /BATT supply through a blocking diode to prevent current leakage back into the battery when power comes on. The diode, CR3, in series with the battery, will only have a voltage drop across it of approximately 160 mV due to the low cur-ent drain when operating from the battery supply.

SERVICE SHEET 20 SIGNATURE ANALYSIS

Note

Remove Expansion Module before performing tests.

TEST 5. ROM C Test
(Service Sheet 20)

a. Set instrument power to off.

b. Signature Analyzer connections:
START ⎣ to U26-20 (CSM0)
STOP ⎍ to U3-18 (CSM0)
CLOCK ⎍ to TP5 (LRD)

c. Set S1-B and S1-C to closed.

d. Set instrument power to on.

e.

TEST POINT		SIGNATURE	SS/GRID LOC
Probe to +5			
5-A	(U26-9)	P872	20/A2
5-B	(U26-10)	3H9A	
5-C	(U26-11)	CAU9	
5-D	(U26-13)	3A3U	
5-E	(U26-14)	214H	
5-F	(U26-15)	1FA3	
5-G	(U26-16)	H951	
5-H	(U26-17)	P0P6	

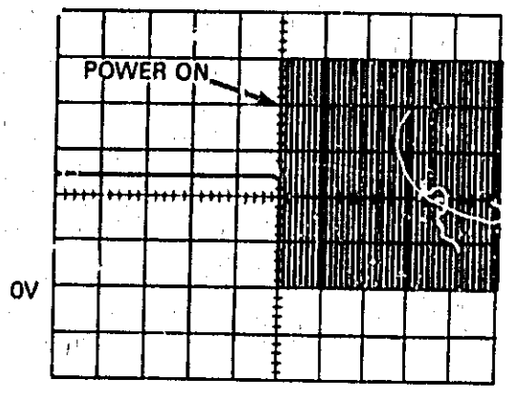
f. Set S1-B and S1-C to open.

Ⓐ

POWER ON

Monitor Oscilloscope Setup

1 Volt/Div
0.2 Sec/Div

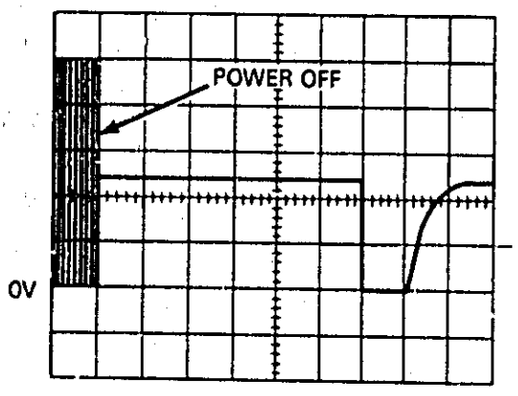


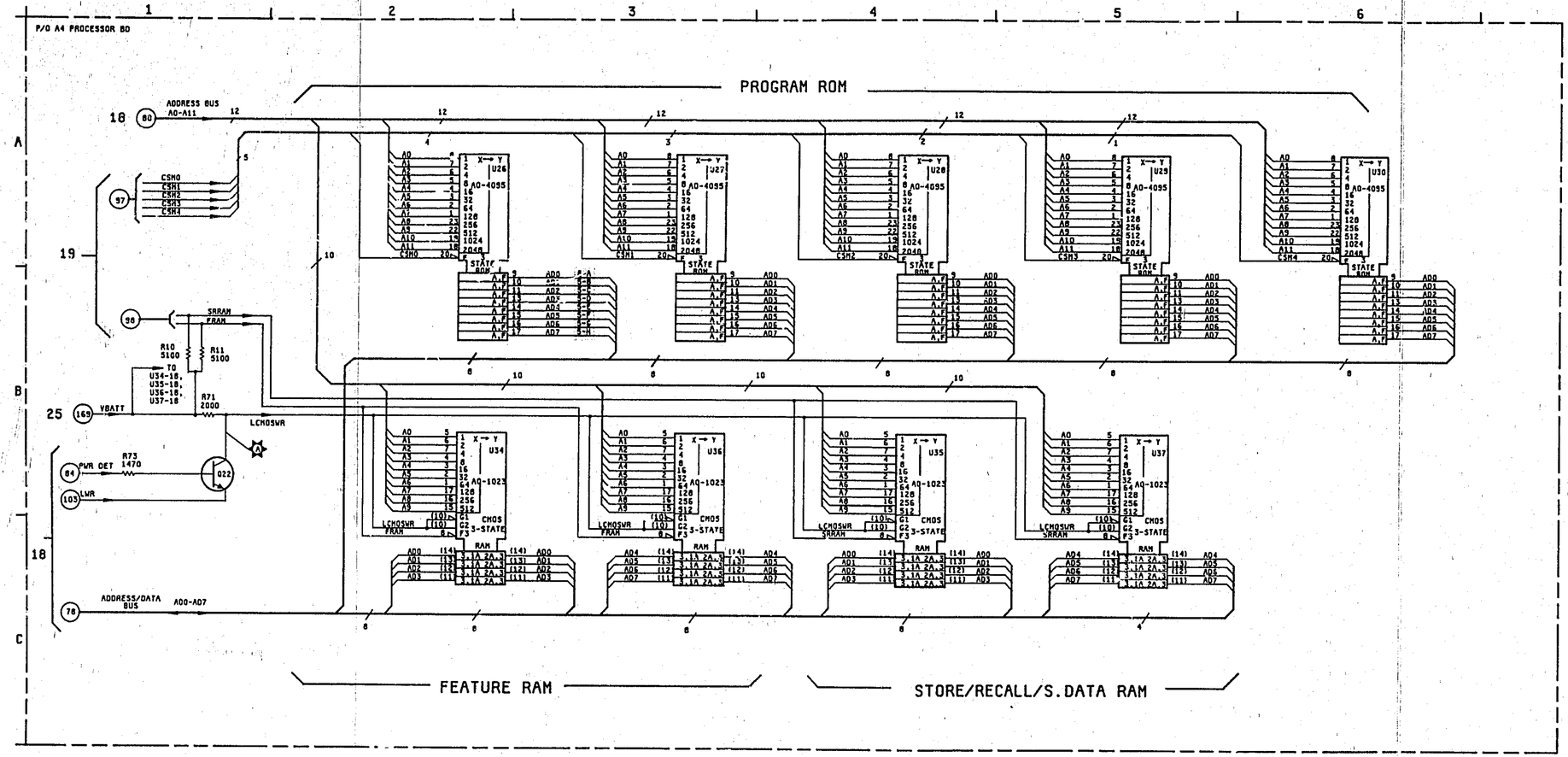
Ⓐ

POWER OFF

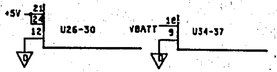
Monitor Oscilloscope Setup

1 Volt/Div
0.2 Sec/Div





IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A4
R10,11,71,73 Q22 U26-30,34-37

DELETE:C48,R70,R72,U120

1980/115/10/22/81

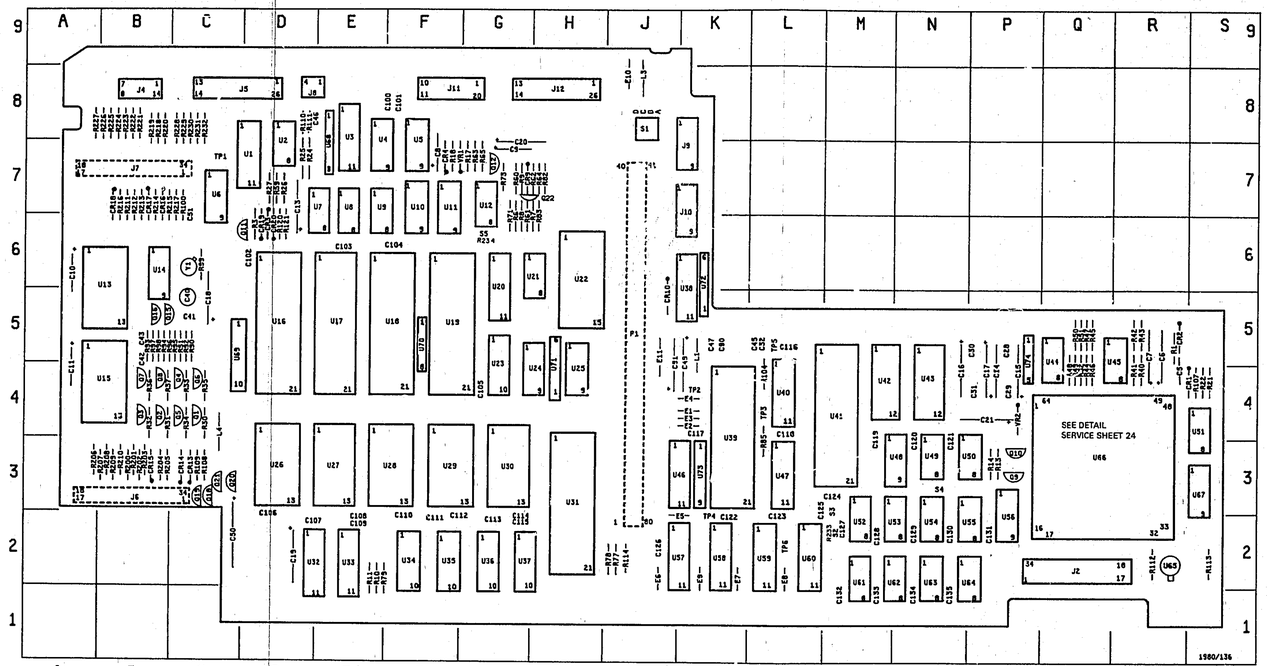
20

Service Sheet 20. Schematic Diagram
P/O Processor Board, Store/Recall RAM, Feature RAM, and Program ROM

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	R-4	C114	G-2	J2	Q-2	R24	D-7	R97	B-5	R231	C-8	U32	D-2		
C6	R-5	C115	G-3	J4	B-8	R25	D-7	R98	1-5	R232	C-8	U33	E-2		
C7	R-5	C116	L-5	J6	C-8	R26	D-7	R99	C-6	R233	M-2	U34	F-2		
C8	F-7	C117	L-4	J8	B-3	R27	D-7	R100	C-7	R234	G-6	U35	F-2		
C9	G-7	C118	L-4	J7	B-7	R30	C-4	R104	L-4	S1	J-8	U36	G-2		
C10	A-6	C119	M-3	J9	D-8	R31	B-4	R107	S-4	S2	M-2	U37	G-2		
C11	A-4	C120	N-3	J9	K-7	R32	B-4	R108	C-3	S3	M-2	U38	K-6		
C13	D-7	C121	M-3	J10	K-7	R33	C-4	R109	C-3	S4	N-3	U39	K-4		
C14	P-4	C122	K-2	J10	F-8	R34	C-4	R110	D-8	S5	G-6	U40	L-4		
C15	P-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	C-7	U41	M-4		
C16	N-4	C124	M-3	L1	K-8	R36	B-4	R112	R-2	TP2	K-4	U42	M-4		
C17	P-4	C125	L-3	L3	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	N-4		
C18	C-6	C126	J-2	L4	C-4	R40	R-4	R114	J-2	TP4	K-2	U44	O-5		
C19	D-2	C127	M-2	P1	J-5	R41	R-4	R120	D-6	TP5	L-5	U45	R-5		
C20	G-7	C128	M-2	Q1	C-4	R42	R-5	R121	D-6	TP6	L-2	U46	K-3		
C21	P-4	C129	N-2	Q2	B-4	R43	R-5	R200	B-3	U1	D-7	U47	L-3		
C28	P-5	C130	N-2	Q3	B-4	R44	Q-4	R201	B-3	U2	D-7	U48	N-3		
C29	P-4	C131	P-2	Q4	C-4	R45	Q-5	R202	B-3	U3	E-7	U49	N-3		
C30	P-5	C132	M-1	Q5	C-4	R46	Q-4	R203	B-3	U4	E-7	U50	N-3		
C31	P-4	C133	M-1	Q6	C-4	R47	Q-4	R204	B-3	U5	E-7	U51	S-4		
C32	L-5	C134	N-1	Q7	B-4	R48	Q-4	R205	B-3	U6	E-7	U52	M-2		
C40	C-5	C135	N-1	Q8	B-4	R49	Q-4	R206	A-3	U7	E-7	U53	N-2		
C41	C-5	CR1	S-4	Q9	P-3	R50	Q-5	R207	B-3	U8	E-7	U54	N-2		
C42	B-5	CR2	R-5	Q10	P-3	R51	Q-5	R208	B-3	U9	E-7	U55	P-2		
C43	B-5	CR3	D-6	Q11	D-6	R52	Q-4	R209	B-3	U10	F-7	U56	P-4		
C45	L-5	CR4	F-7	Q12	G-7	R59	D-7	R210	B-3	U11	F-7	U57	K-2		
C46	D-8	CR9	G-7	Q15	B-5	R60	G-7	R211	B-7	U12	G-7	U58	K-2		
C47	K-5	CR10	J-5	Q16	B-5	R61	G-6	R212	B-7	U13	B-5	U59	L-2		
C48	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	B-6	U60	L-2		
C50	C-2	CR14	C-3	Q19	C-3	R63	H-7	R214	B-7	U15	D-5	U61	M-2		
C51	C-6	CR16	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2		
C90	C-5	CR18	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-5	U63	N-2		
C91	J-4	CR17	B-7	Q22	G-7	R71	G-6	R217	C-7	U18	F-5	U64	P-2		
C100	F-8	CR18	B-7	R1	R-5	R73	G-7	R218	B-8	U19	F-5	U65	B-2		
C101	F-8	CR19	D-6	R3	D-8	R77	J-2	R219	B-8	U20	G-5	U66	G-3		
C102	D-6	CR20	D-5	R6	G-6	R78	J-2	R220	B-8	U21	H-6	U67	S-3		
C103	E-6	E1	K-4	R7	H-6	R79	E-2	R221	B-8	U22	H-5	U68	E-7		
C104	F-6	E2	K-4	R8	G-6	R82	H-7	R222	B-8	U23	G-4	U69	C-5		
C105	G-4	E3	K-4	R9	G-7	R83	H-6	R223	B-8	U24	H-4	U70	F-5		
C106	D-2	E4	K-4	R10	E-2	R85	L-3	R224	B-8	U25	H-4	U71	H-4		
C107	E-2	E5	K-2	R11	E-2	R90	C-5	R225	B-8	U26	D-3	U72	K-5		
C108	E-2	E6	J-2	R13	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3		
C109	E-2	E7	K-2	R14	P-3	R92	C-5	R227	A-8	U28	F-3	U74	P-5		
C110	F-2	E8	K-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	K-7		
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4		
C112	F-2	E10	J-8	R21	S-4	R95	C-5	R230	C-8	U31	H-3	Y1	C-6		
C113	G-2	E11	J-5	R22	S-4	R96	B-5								

A4



SERVICE SHEET 21 MNEMONICS

A8-A10	Address Bus lines 8 through 10.
AD0-AD7	**Address/Data bus** — Microprocessor bidirectional bus, Data on this bus can be the least significant 8 bits of address.
ALE	**Address Latch Enable** — Microprocessor output. Falling edge is used to latch data on the AD0-AD7 bus into the address latch.
BCD SHIFT	**BCD Shift Clock** — Used to shift the 56 bit serial data (DATA IN) through the shift register from horizontal interface to IO port.
BUSY	Goes high at the beginning of CYCLE ST and remains high until the end of the BCD frame — to processor via IO port.
CH1 VERT TAG	**Channel 1 Probe Tag** — Input to processor to denote probe division ratio and thereby alter channel 1 gain accordingly.
CH2 VERT TAG	**Channel 2 Probe Tag** — Input to processor to denote probe division ratio and thereby alter channel 2 gain accordingly.
CHAN 1	**Phase 1 Output of RPG** — Pulse string out of RPG — counted by processor to detect rate of change.
CHAN 2	**Phase 2 Output of RPG** — Pulse string out of RPG — phase difference of CHAN 1 and CHAN 2 denotes direction of rotation.
CHAR DISP	**Character Display** — Bit determining character mode — if high characters are on — if low characters are off and option display is allowed.
CLK	**Clock** — From microprocessor — 3.333333 MHz processor clock input divided by two.
COL0-COL7	**Column 0-7** — Outputs from IO to keyboard — along with ROW inputs determine if a key has been closed, and which key has been closed.
CSG	**Clock, Serial Gated Data** — Clock from IO port to unblanking gate shift register.
CVT	**Clock, Vertical and Trigger** — Clock for vertical and trigger shift register string, to shift data through the string.
CYCLE ST	**Cycle Start** — Output by processor via IO port to sync horizontal interface communications.
DATA IN	56 bit data string from horizontal microcircuit to (BCD2 via horizontal interface) to calibrate VCO frequency.
DISP MODE	**Display Mode** — From IO to Programmable Logic Array (PLA) -allows character or option display.
DLY'D TRIG TAG	**Delayed Trigger Probe Tag** — Signal to indicate division ratio of probe attached to delayed ext. trigger input.
HCRS	**Horizontal Counter Reset** — Signal from IO to sweep control circuit to reset counter when a sweep interrupt is requested.
HDIC	**High, Display Inhibit Control** — Signal to processor IO signifying single sweep is complete, horizontal awaits reset.
HTDC	**High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.

Service Sheet 21. Component Locator
P/O Processor Board, Input/Output Interface

SERVICE SHEET 21 MNEMONICS (CONT'D)

IO/LM	**High, IO/Low, Memory** — selects either IO or Memory devices.
IO/RAM	**IO/RAM Chip Select** — Chip select decoded from address to select IO/RAM, A4U16.
IO/ROM 5	**IO/ROM 5 Chip Select** — Chip select decoded from address to select IO/ROM 5, A4U17.
IO/ROM 6	**IO/ROM 6 Chip Select** — Chip select decoded from address to select IO/ROM 6, A4U18.
IS SHIFT	**Instruction String Shift** — Signal to shift SDTA through the Instruction shift register to produce the 10 bit instruction string (IS).
LCL 1,2,3	**Lamp Clock 1,2,3** — Clocks generated by software to shift SDTA through the lamp driver strings to light applicable panel lamps.
LFLG	**Low, Flag** — Output from horizontal microcircuit to an IO port signifying to the processor that a main sweep trigger was initiated during the delayed sweep trigger ramp — used in the auto scope routine and available to HP-IB.
LIN/OUT	**Low, Input/High, Output** — Controls direction of BCD data into or out of the horizontal microcircuit.
LIOW	**Low, IO Write** — indicates to the selected IO device that a data byte is available on the AD0-AD7 lines. The IO device will then latch the data. Usually controlled by the DMA Controller.
LRD	**Low, Read** — Asserted by the microprocessor to read data from an addressed memory location.
LWR	**Low, Write** — Asserted by the microprocessor to allow writing into an addressed memory location.
MAIN TRIG TAG	**Main Trigger Probe Tag** — Signal to indicate division ratio of probe attached to main ext. trigger input.
MLT	**Main Line Trigger** — Output from IO port to DAC activating line trigger of main sweep.
PCHC	**Pulse Clock Horizontal and Calibrator** — From IO port to sweep control to gate data for channel, sweep, or calibrator functions.
RESET	Reset pulse from microprocessor to initalize peripherals to proper states at power up or power down.
ROW0-ROW7	**Row inputs from front panel to IO ports** — when a key is pressed a signal from a column output will be present on a row input.
RPG0-RPG6	RPG counter data lines to IO ports.
RRPG	**Reset RPG Counter** — Output of IO port to reset RPG counter.
SDTA	**Serial Data** — Data string from IO to various shift registers that when clocked through initiates various functions, lamps, etc.
TAG IN 0 TAG IN 3	Probe tag information to IO port to set sensitivity as recognized for attached probes.
TAG SEL0 TAG SEL3	**Tag Selection 0-3** — Input to probe recognition circuit from IO port which selects probe information.
URPG	**RPG Counter Counting Up** — Direction of rotation information from RPG counter to IO port.

SERVICE SHEET 21 — THEORY OF OPERATION

The Parallel IO Subsystem. The microprocessor has two basic methods of controlling the analog instrumentation circuitry of the 1980. The DAC sub-system is used to provide 16 analog voltages to the various sweep, gain, position, and intensity circuits within the analog system. However, in addition to this control a number of state related controls must be manipulated such as the state of the attenuator solenoids, range selections for sweep and vertical gain, display mode data (1 vs 2, X·Y·Z, trigger view, etc), and various other miscellaneous control functions. These functions are asserted by the processor through the use of several parallel IO ports, and a series of serial shift register/latches.

These IO ports provide other control outputs and status sensory inputs required to interface the processor to the following functional circuitry:

(1) Shift Register strings. (2) Lamp driver strings. (3) The front panel keyboard contacts. (4) Probe tags. (5) RPG rotational detection circuitry (6) Character display control. (7) Horizontal interface control. (8) Main line triggering.

Three parallel IO devices are interfaced to the microprocessor bus to provide these IO functions; one IO/RAM/Timer (A4U16), and two ROM/IO ports (A4U17,A4U18).

IO/RAM/Timer. The IO/RAM/Timer serves both as a random access memory, and as a 22 bit IO port. In addition, it contains a programmable timer, which is configured to generate a RST 7.5 interrupt when the 14 bit divide factor reaches terminal count, dividing the 1.67 MHz processor clock into 16,384 possible interval periods. This timer is used by the software for all time related control sequences such as horizontal VCO calibration, and during the RPG slewing routine.

Port A and Port B are used by the processor as a front panel keyboard interface. The front panel keyboard is organized into an 8 row 8 column crossbar matrix, with the eight row lines serving as sensory inputs to Port A and the eight column lines serving as scanning outputs from Port B. In order to detect a keyboard contact closure, the processor is required to sequentially strobe each column output low and read the row inputs on Port A. A particular row input on Port A is normally pulled high and is driven low by a given column output on Port B only when a contact closure occurs. When a row input goes low as a result of a specific column output being driven low, the location of the contact closure is identified. Each keyboard contact on the front panel is assigned a unique Row/Column combination.

During normal operation, the software periodically executes a "quick key" test to detect activity on the front panel. During this test, the ROW inputs on Port A are read with all of the column outputs on Port B held low. Should any bit on Port A be found low, a sequential column scan is executed to determine exactly which key was pressed. A good indication that the system is operating properly is to verify that all eight outputs on Port B are being held low.

The remaining port on the IO/RAM/Timer is Port C. This port is used to provide 6 additional output ports to the system. The lines PC0 - PC3 are the signals TAG SEL0 - TAG SEL3 and are used to control the operation of the probe tag interface. The bits PC4 and PC5 are the signals CHAR DISP and DISP MODE and are used to control the external operation of the character generator.

The IO/RAM (A4U16) is used as scratch pad storage for various logical and arithmetic operations by the software. Like the ROM/IOs (A4U17,A4U18), this device is microprocessor bus compatible, with an internal address latch to capture the address present on AD0-AD7 during ALE. Therefore the chip enable for this device goes active at the beginning of the bus cycle, and is not gated with LMEMR or LMEMW.

IO/ROMs. Two IO/ROMs are employed to provide additional ROM memory for program storage, and to provide additional IO. Each IO/ROM supports 2K bytes of ROM and 16 bits of IO, organized into two eight bit ports. Each bit can be independently programmed as an input or output. The function of the various control signals on these ports will be described as they pertain to various circuitry.

The IO/ROMs (A4U17-A4U18) are bus compatible with the microprocessor bus system. These devices directly use the control signal ALE to internally latch the lower eight address bits during each bus cycle. Therefore, the chip enable to these devices goes low true at the beginning of the bus cycle, before ALE is pulsed, rather than going true during the LRD strobe. The IO/LM line is also directly used by the IO/ROMs (A4U17-A4U18) to interpret the LRD and LWR strobes as either IO or memory. Special Purpose Interface Circuity. As was mentioned previously, a number of special purpose interface circuits are controlled by the parallel IO subsystem. The function and operation of these circuits are individually described below.

Shift Register Strings. As stated previously, a considerable number of state-related control information must be passed from the processor to various analog subsystems throughout the instrument. Since it would be impractical to provide direct parallel access to these functions via bus interfaced IO ports, a means of serial communication is required. A series of shift registers are used, each containing an internal serial shift register and a parallel output latch to transfer data from the shift register to the outputs. Each of these shift registers require a serial data input, a shift clock, and a strobe to transfer the shift register data to the latch outputs.

These shift registers are organized into strings, with the serial data input to each subsequent shift register being provided by the serial data output of the previous shift register in the string. Each shift register in the string is then provided with a common shift clock which is unique to the string. Three such strings of shift registers are implemented to convey the required information throughout the scope, with each string having an individual shift clock which is under software control from three IO port outputs. These clocks, CSC, PCHC, and CVT are toggled by the processor whenever new data is to be output to either the gate/power supply, horizontal, or vertical/trigger strings. The serial data input to each shift register string is provided from a single IO port output SDTA. This signal is set and cleared under software control before a given shift clock is pulsed. Although SDTA is present on the serial input of each latch string, the state of SDTA is only shifted into one string at a time, since only one shift clock is pulsed by the software after SDTA is set.

Data is transferred to all shift register outputs simultaneously with a single IO port output called HTDC. HTDC (High, Transfer Data Command) is pulsed by the software each time a shift operation is complete.

Lamp Drivers. In addition to controlling the shift register strings, the parallel I/O subsystem is also interfaced to five lamp driver ICs, used to drive the incandescent lamps on the front panel. These devices are specially designed shift registers containing a 16 bit serial shift register, and 16 buffered, latched outputs. Each output is capable of sinking the required current to drive a lamp.

The lamp drivers are organized into three strings, with two devices being located on the TIME panel, one on the VOLTS panel, and two on the processor board. Communication to these lamp driver strings is done in the same method as described for shift register strings. Three lamp string shift clocks, LCL1, LCL2, and LCL3 are provided from output ports on A4U17. The common serial data line SDTA is used to input serial data to each string, and the common HTDC strobe is used to transfer the data to the lamp driver buffered outputs. However, it should be noted that HTDC is inverted to form LTDC (on Service Sheet 25 by A4U2C) since the transfer data input on the lamp drivers is low-true.

Probe Tag Interface. A special feature on the BNC inputs of the vertical and trigger attenuators allows the divide ratio of the probe to be monitored by the processor. This input, known as the probe tag, will have a fixed resistance within the probe from the tag input to analog ground, the value of which is determined depending upon whether a 1:1, 10:1, 100:1, or 1000:1 probe is connected to the BNC. Based on this divide ratio, the vertical sensitivity readout is appropriately corrected by the processor. In addition, if a short is detected, this is interpreted by the processor to mean that the programmable "smart probe" key has been pressed.

There are four probe tag inputs to the processor board, corresponding to the Channel 1, Channel 2, main and delayed trigger probes. Each of these inputs are pulled high to +6V on the processor board. Therefore, for a given tag resistance to ground, a discrete voltage is established on the TAG input lines, which can be evaluated as the resistive divide ratio of the tag resistance.

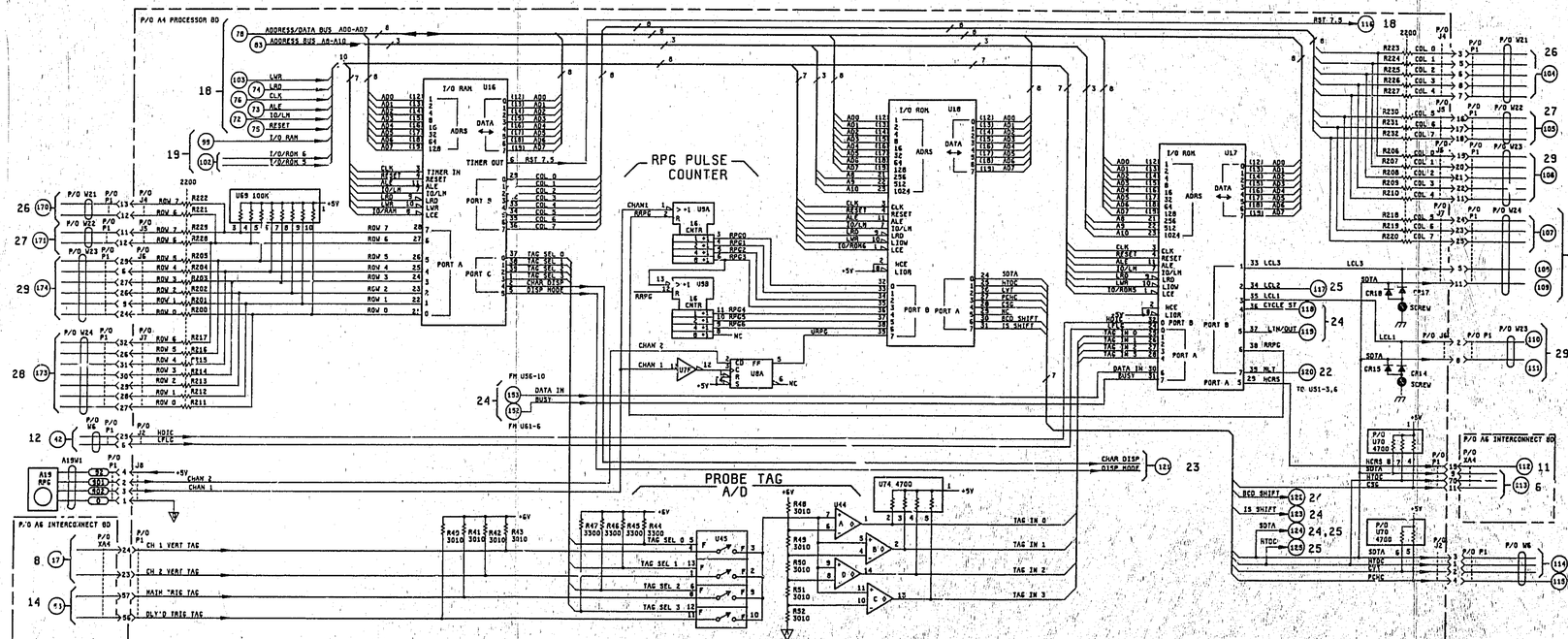
Periodically the processor scans these TAG levels by sequentially measuring the voltage present on each tag. This is accomplished by driving each of the TAG SEL signals, which originate from an output port from A4U16, to a high state. Each TAG SEL output controls a CMOS analog switch (A4U45), and thus causes the DC level on the selected tag to be transmitted to the input of a simple analog to digital converter (A4U44). This converter consists of four voltage comparators, with one input of each comparator tied together, and connected to the output of the analog switches. The other input of each comparator is then tied to +6 V, thus creating five possible ranges for the probe tag measurement. The outputs of these four comparators, TAGIN0 -TAGIN3, are then connected to four port inputs on A4U17, where they can be read by the processor after the processor has selected a given tag with one of the TAG SEL lines from A4U16.

When all four TAG IN lines are high during a tag measurement this indicates a TAG impedance greater than 12K and is considered an open or a 1:1 probe. When all four TAG IN lines are low, this indicates a tag impedance of less than 750 ohms and is interpreted as a smart probe contact closure. The following is a truth table of conditions where the TAG IN signals occur versus maximum resistance values on the probe tags.

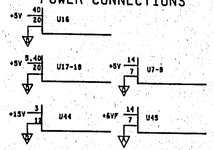
PROBE TYPE	TAG RESISTANCE	TAG IN 0	TAG IN 1	TAG IN 2	TAG IN 3
1:1	greater than 12K	1	1	1	1
10:1	4.5K to 12K	0	1	1	1
100:1	2K to 4.5K	0	0	1	1
1000:1	750 to 2K	0	0	0	1
key closure	less than 750	0	0	0	0

RPG Interface. All numerical adjustments are relayed to the processor system via a single rotary pulse generator. This device generates two pulse trains whenever it is rotated. The pulse frequency is a function of the speed of rotation. The relative phase of the two pulse trains is a function of the direction of rotation. The phase angle between channel 1 and channel 2 will be positive in one direction, and negative in the other.

The rate of change of the RPG is measured by the processor through the use of a 7 bit binary counter (A4U9), which is incremented by the channel 1 pulse train of the RPG, and cleared under software control. Access to the seven counter outputs is available to the processor through 7 input ports (RPG0-6) to A4U18. The RPG counter is cleared by an output port RRPG from A4U17. An edge-triggered flip flop (A4U8A) is used to detect the phase of channel 1 versus channel 2. The trailing edge of the pulses on channel 1 is used to clock the level on channel 2 to the output of the flip flop (A4U8). If channel 2 lags channel 1, the flip-flop will be set. If channel 2 leads channel 1, the flip-flop is cleared. The trailing edge of channel 1 is used in order to guarantee that at least one pulse time occurs before the direction is determined.



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

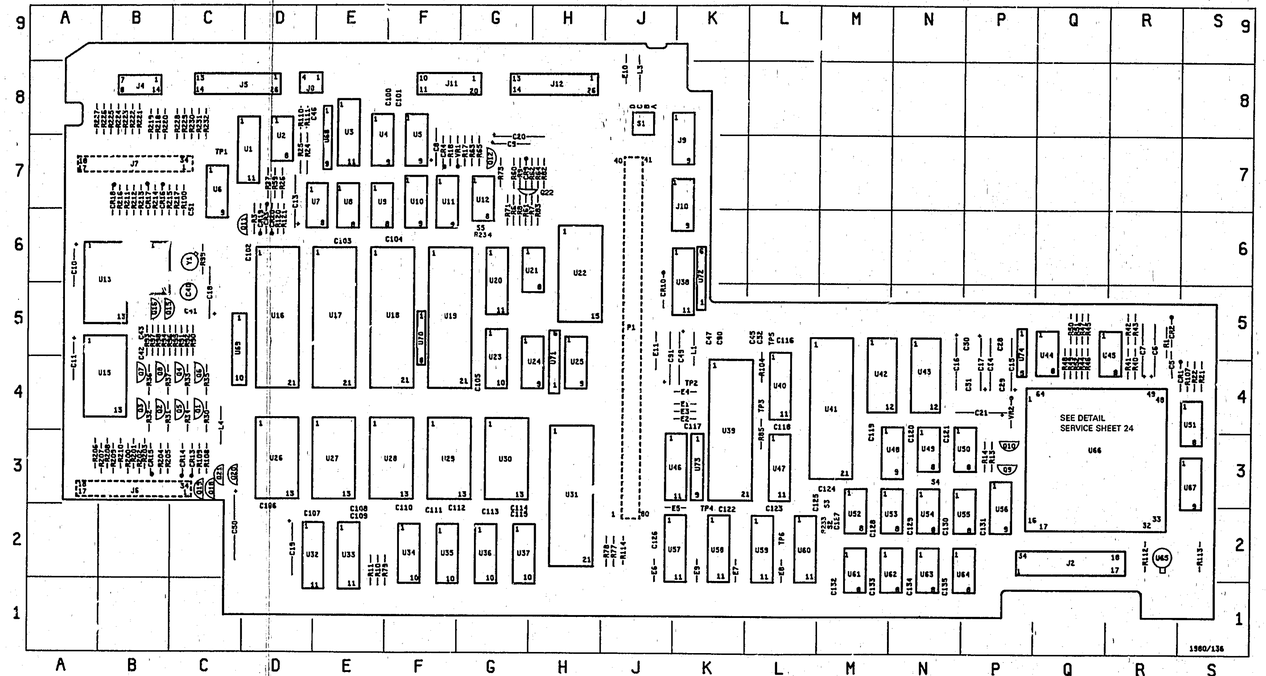
PARTS ON THIS SCHEMATIC

P/O A4	P/O A6	CHASSIS
CR14,15,17,18 R40-52,200-232 J8,P/O J2, P/O J4-7 P/O P1 U7,44,5,16-18, U44,45,69 70,74	P/O XA4 A19 V1	A19 P/O V6 P/O Z1-24

1980/11E/10/7/81

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	R-4	C114	G-2	J2	O-2	R24	D-7	R97	P-5	R231	C-8	U32	D-2
C6	R-5	C115	G-2	J4	B-8	R25	D-7	R98	C-6	R232	C-8	U33	E-2
C7	R-5	C116	L-5	J5	C-8	R26	D-7	R99	C-6	R233	M-2	U34	F-2
C8	F-7	C117	K-4	J6	B-3	R27	D-7	R100	C-7	R234	G-6	U35	F-2
C9	G-7	C118	L-4	J7	B-7	R30	C-4	R104	L-4	S1	J-8	U36	G-2
C10	A-4	C119	M-3	J8	D-8	R31	B-4	R107	S-4	S2	M-2	U37	G-2
C11	A-4	C120	N-3	J9	K-7	R32	B-4	R108	C-3	S3	M-2	U38	K-6
C13	D-7	C121	N-3	J10	K-7	R33	C-4	R109	C-3	S4	N-3	U39	K-4
C14	P-4	C122	K-2	J11	F-8	R34	C-4	R110	D-8	S5	G-6	U40	L-4
C15	P-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	C-7	U41	M-4
C16	N-4	C124	M-3	L1	K-6	R36	B-4	R112	R-2	TP2	K-4	U42	M-4
C17	P-4	C125	L-3	L3	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	N-4
C18	C-5	C126	J-2	L4	C-4	R40	B-4	R114	J-2	TP4	K-2	U44	G-5
C19	D-2	C127	M-2	P1	J-5	R41	R-4	R120	D-6	TP5	L-5	U45	R-5
C20	G-7	C128	M-2	Q1	C-4	R42	R-5	R121	D-6	TP6	L-6	U46	K-3
C21	P-4	C129	N-2	Q2	B-4	R43	R-5	R200	B-3	U1	D-7	U47	L-3
C28	P-5	C130	N-2	Q3	B-4	R44	Q-4	R201	B-3	U2	D-7	U48	N-3
C29	P-4	C131	P-2	Q4	C-4	R45	Q-5	R202	B-3	U3	E-7	U49	N-3
C30	P-5	C132	M-1	Q5	C-4	R46	Q-4	R203	B-3	U4	E-7	U50	N-3
C31	P-4	C133	M-1	Q6	C-4	R47	Q-5	R204	B-3	U5	F-7	U51	S-4
C32	L-5	C134	N-1	Q7	B-4	R48	Q-4	R205	B-3	U6	C-7	U52	M-2
C40	C-5	C135	N-1	Q8	B-4	R49	Q-4	R206	A-3	U7	E-7	U53	N-2
C41	C-5	CR1	E-4	Q9	P-3	R50	Q-5	R207	C-3	U8	E-7	U54	N-2
C42	B-5	CR2	R-5	Q10	P-3	R51	Q-5	R208	B-3	U9	E-7	U55	P-2
C43	B-5	CR3	D-6	Q11	D-6	R52	Q-4	R209	B-3	U10	F-7	U56	P-2
C45	L-5	CR4	F-7	Q12	G-7	R59	D-7	R210	B-3	U11	F-7	U57	K-2
C46	D-8	CR9	G-7	Q15	B-5	R60	G-7	R211	B-7	U12	G-7	U58	K-2
C47	K-5	CR10	J-5	Q16	B-5	R61	G-6	R212	B-7	U13	B-5	U59	L-2
C48	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	B-6	U60	L-2
C50	K-2	CR14	C-3	Q19	C-3	R63	G-7	R214	B-7	U15	B-4	U61	M-2
C51	C-6	CR15	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2
C80	K-5	CR16	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-3	U63	N-2
C91	J-4	CR17	B-7	Q22	G-7	R71	G-6	R217	C-7	U18	F-5	U64	P-2
C100	F-8	CR18	B-7	R1	R-5	R73	G-7	R218	B-8	U19	F-5	U65	R-2
C101	F-8	CR19	D-6	R3	D-5	R77	J-2	R219	B-8	U20	G-5	U66	G-3
C102	D-6	CR20	D-6	R6	G-5	R78	J-2	R220	B-8	U21	H-6	U67	S-3
C103	E-6	E1	K-4	R7	H-5	R79	E-2	R221	B-8	U22	H-6	U68	E-7
C104	F-6	E2	K-4	R8	G-6	R82	H-7	R222	B-8	U23	G-4	U69	C-5
C105	K-4	E3	K-4	R9	G-7	R83	H-6	R223	B-8	U24	H-4	U70	F-5
C106	D-1	E4	K-4	R10	E-2	R85	L-3	R224	B-8	U25	H-4	U71	H-4
C107	E-6	E5	J-2	R11	E-2	R90	C-6	R225	B-8	U26	D-3	U72	K-5
C108	E-2	E6	J-2	R13	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3
C109	E-2	E7	K-2	R14	P-3	R92	C-5	R227	A-8	U28	F-3	U74	P-5
C110	F-2	E8	J-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	F-7
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4
C112	F-2	E10	J-8	R21	E-4	R95	C-5	R230	C-8	U31	H-3	Y1	C-6
C113	G-2	E11	J-5	R22	S-4	R96	B-5						



A4

SERVICE SHEET 22 MNEMONICS

A0-A7	Address Bus Lines 0-7.
AD0-AD7	**Address/Data bus** — Microprocessor bidirectional bus Data on this bus can be the least significant 8 bits of address.
CAL EN	**Calibrate Enable** — Input to DRC to allow the cal factors to be written into memory — from rear panel "Protected-Not Protected" switch.
CHOP CLK	**Chop Clock** — Derived from processor clock via DAC Refresh Controller — used to "sample" traces in chopped mode.
CH2 BAL	**Channel 2 Balance** — From balance half of channel 2 FET to vertical preamplifier input.
CH1 GAIN	**Channel 1 Gain Voltage** — Analog voltage from DAC to set channel 1 gain (volts/division).
CH1 POS	**Channel 1 Position Voltage** — Analog output of DAC to set vertical position of channel 1 trace.
CLK	**Clock** — From microprocessor — 3.333333 MHz processor clock input divided by two.
D0-D7	**Data 0-7** — DAC Refresh Controller data input/output lines.
DA1	**Data 1** — 256 bit data stream from DRC to DAC containing 7-segment (LED) display information.
DA2	**Data 2** — 256 bit data stream from DRC to DAC containing 16 channel DAC information.
DLY'D RAMP	**Delayed Ramp Voltage** — Analog output of DAC to set delay ramp charge current.
DLY'D TRIG LEVEL	**Delayed Trigger Level Voltage** — Analog output of DAC to set delayed trigger level.
DS	**Descriptor** — 256 bit data stream from DRC to DAC to decode DA1 for LED display.
DTRIG BIAS	**Delayed Trigger Bias** — Bias voltage input to the DAC.
FINE DELAY	**Fine Delay Ramp Voltage** — Analog output of DAC to control the Fine Delay ramp.
HORIZ CLK	**Horizontal Clock** — Derivative of processor clock from the DAC Refresh Controller to horizontal interface to develop synchronous communications.
INTEN	**Intensity** — Analog voltage level from the DAC to gate circuit to set beam intensity level.
LDRC RDY	**Low, DAC Refresh Controller Ready** — Output from DRC which puts the processor in wait states until the DRC is ready to complete its bus cycle.
LINE FREQ	**Line Frequency** — From line transformer secondary — when main line trigger is selected LINE FREQ via DAC modulates the main trigger level DAC output.
LMSYNC	**Low, Master Sync** — Derived from processor clock by the DRC to synchronize data transfer to the DAC and used by the horizontal microcircuit to synchronize its operation.
LRD	**Low, Read** — Asserted by the microprocessor to read data from an addressed memory location.
LWR	**Low, Write** — Asserted by the microprocessor to allow writing into an addressed memory location.
MAIN RAMP	**Main Ramp Voltage** — Analog output of DAC to set main ramp charge current.
MAIN TRIG LEVEL	**Main Trigger Level Voltage** — Analog output from DAC to set main trigger level.

Service Sheet 22. Component Locator
P/O Processor Board, Digital to Analog Subsystem

SERVICE SHEET 22 MNEMONICS (CONT'D)

MLT	**Main Line Trigger** — Output from IO port to DAC activating line trigger of main sweep.
NVRAM	**Nonvolatile RAM** — Chip select decoded from address to the DRC — allows the DRC to read or write to the memory it controls, A4U42 and A4U43.
PBS	**Protected Block Select** — Tied low to protect Cal Factor Memory in conjunction with CAL EN.
PH1 CLK	**Phase 1 Clock** — Processor clock divided by eight from the DRC to the DAC and horizontal microcircuit.
PH2 CLK	**Phase 2 Clock** — Processor clock divided by eight from the DRC to the DAC and horizontal microcircuit —displaced from PH1 CLK by two processor clock periods
PWR DET	**Power Detector** — Input to processor at power on and power off which generates reset pulses for the processor and peripherals.
RCD	**Reset Cathode Driver** — Derivative of processor clock via DRC used to reset the shift registers to synchronize the LED displays.
SA-SG	**Segments A-G** — Outputs from DAC to LED displays to light selected segments of each LED.
SCAN	**Digit Strobe** — Output of DAC to LED digit shift register to enable selected LED digits.
SDP	**Segment, Decimal Point** — Output of DAC to LED displays to light selected decimal point.
SEP POS	**Separate Position Voltage** — Analog output of DAC to position the separation of traces in DUAL.
VBATT	**Battery Voltage** — Voltage that sustains NVRAM when instrument has been powered down.
VCO CONTROL	**VCO Control Voltage** — Analog output of DAC to control frequency of VCO.

SERVICE SHEET 22 — THEORY OF OPERATION

DAC Subsystem. In order to provide discrete analog control over certain instrumentation circuitry, a 16 channel Digital-to-Analog Converter (A4U66) is used. This is a hybrid device which contains a single DAC and 16 sample and hold capacitors, providing 16 analog voltages to control beam intensity, horizontal and vertical position, vertical gain and horizontal sweep speeds within digitally selected ranges, main and delayed trigger levels, and two fine adjustment controls for the VCO and fine delay. In addition, this device performs the auxiliary function of controlling the front panel LED display scanning.

The DAC receives data input for the D to A converter and the LED's via three serial data streams. Two of these data streams, DA1 and DS, are used to carry information for the 7 segment LED displays. The third data path, DA2, carries data for the 16 channel D/A converter. There are 256 bits of information in each frame, where the frame is defined by the signal LMSYNC. In addition to the LMSYNC input, two phase clocks, PH1 CLK and PH2 CLK are provided to the DAC (A4U66). The PH1 CLK pulse leads PH2 CLK by two processor clock periods, 1.2 us, and is used by the DAC to sample data on DA1, DS, and DA2. PH2 CLK determines when the data transition is used by the DAC as a shift clock. These clocks are also utilized internally by the DAC, by various synchronous logic circuitry, and by the D/A integrator.

The serial data streams and the three input clocks are generated by a special purpose device called the DAC Refresh Controller (A4U41).

DAC Refresh Controller. The DAC Refresh Controller is a special purpose hybrid intregrated circuit which provides a means to interface a byte oriented microprocessor memory with the serial oriented DAC intregrated circuit.

The DRC can address the RAM memory (A4U42 and A4U43) and controls the read and write functions of these RAMs with the signal LWE (Low, Write Enable). The DRC also produces the signal AOE (Address Output Enable) to control the three state buffer (A4U47).

The three state buffer (A4U47) is used to isolate the microprocessor's address bus from the RAMs (A4U42, A4U43). Both the microprocessor and the DRC read data from and write data to these RAMs. The DRC signal AOE determines which device can address the RAMs. When AOE is low the F1 and F2 inputs of A4U47 are active and the output of the buffer follows the input microprocessor address bus. With AOE high, the RAMs will be addressed by the DRC and the microprocessor address bus is isolated by A4U47.

The microprocessor keeps the data in the RAMs (A4U42,A4U43) updated as required by changes in the front panel settings and correct data for the LED displays. The microprocessor can only write to the RAMs when allowed by the DRC. If the microprocessor and the DRC both attempt a memory access at the same time the DRC will set LDRC RDY low to place the microprocessor in a wait state until the DRC memory access is complete.

The DRC contains three internal 8 bit shift registers to convert parallel input data to the three serial data strings DA1, DS, and DA2. The DRC reads a memory byte of data for DA1 and parallel loads the first shift register, changes the memory address and reads a byte of data for DS and parallel loads the second shift register, changes the memory address and reads a byte of data for DA2 and parallel loads the third shift register then releases the address bus to the microprocessor. The three data strings, DA1, DS, and DA2 are shifted out to the DAC at the same time. The data load and shift sequence is repeated until 256 data bits have been shifted out for each data string. The three shift registers are loaded during the PH1 CLK (Phase 1 Clock) and shifted by PH2 CLK (Phase 2 Clock). A MSYNC (Master Sync) pulse is produced at the same time as the 256th shift clock and is synchronized to the PH2 CLK. A RCD (Reset Cathode Driver) signal is produced when the 128th bit and the 256th bit is shifted out.

DA1 (Data 1) is a 256 bit data string that contains the 7-segment LED display information. DS (Descriptor) is a 256 bit data string that describes how the DA1 data is to be decoded for display. DA2 (Data 2) is a 256 bit data string that contains the 16 channels of Digital to Analog converter data for the DAC.

The DRC also produces the HORIZ CLK (Horizontal Clock) and the CHOP CLK for use of the horizontal sweep and sweep control circuits. The HORIZ CLK output frequency is CLK÷64 and the CHOP CLK output frequency is CLK÷4.

Main Line Triggering. In order to implement line frequency triggering for the main trigger, a line frequency sine wave is summed into the DAC analog output for the main trigger level. This causes the main trigger level to modulate with the power line frequency, causing the threshold to be detected at a line frequency rate. The LINE FREQ input to the processor is generated from a low voltage secondary of the power supply transformer. This signal is voltage limited by two diode clamps (A4CR1 and A4CR2) and, when the processor asserts MLT high, LINE FREQ is switched by an analog switch (A4U51) into a special input to the DAC (A4U51).

SERVICE SHEET 22 SIGNATURE ANALYSIS

Note
Remove Expansion Module before performing tests

TEST 6. Write Protected Logic Test (Service Sheet 22)

a. Set instrument power to off.

b. Signature Analyzer Connections:
START ⅂ to U41-27 (NVRAM)
STOP ⎍ to U10-10 (NVRAM)
CLOCK ⎍ to U21-8 (LWR)

c. Ensure rear panel CAL switch is in the Protected position.

d. Set S1-B and S1-D to closed.

e. Set instrument power to on.

f.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		4596		
6-A	(U64-3)	logic 0	22/B3	
6-B	(U63-2)	9971		
6-C	(U64-4)	4596		
6-D	(U21-8)	4596 or 0000	22/B4	
6-E	(U63-3)	9971		
6-F	(U21-10)	HFP7		
6-G	(U7-4)	9971		

g. Set S1-B and S1-D to open.

g. (Cont'd)

TEST POINT		SIGNATURE	SS/GRID	LOC
7-N	(U47-9)	8C36		
7-P	(U47-7)	FA11		
7-Q	(U47-5)	41F7		
7-R	(U47-3)	HFP7		
7-S	(U60-17)	3F8H or 791C	22/C5	
7-T	(U60-15)	0000		
7-U	(U60-13)	0000		
7-V	(U60-11)	3F8H or 791C		
7-W	(U60-8)	3F8H or 791C		
7-X	(U60-6)	3F8H or 791C		
7-Y	(U60-4)	0000		
7-Z	(U60-2)	0000		
7-AA	(U41-26)	0000		
7-AB	(U60-3)	3F8H or 791C		
7-AC	(U60-5)	0000		
7-AD	(U60-7)	0000		
7-AE	(U60-9)	3F8H or 791C		
7-AF	(U60-12)	3F8H or 791C		
7-AG	(U60-14)	3F8H or 791C		
7-AH	(U60-16)	0000		
7-AJ	(U60-18)	0000		

h. Set S1-B, S1-C, and S1-D to open.

TEST 7. DRC/RAM Test (Service Sheet 22)

NOTE
Calibration factors will be lost when this test is performed.

a. Set instrument power to off.

b. Signature Analyzer connections:

START ⅂ to U41-27 (NVRAM)
STOP ⎍ to U10-10 (NVRAM)
CLOCK ⎍ to TP5 (LRD)

c. Set rear panel CAL switch to the Unprotected position.

d. Set S1-B and S1-D to closed.

e. Set instrument power to on.

f. Set S1-C to closed.

g.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		4596		
7-A	(U47-2)	3F8H	22/B2	
7-B	(U47-4)	PC84		
7-C	(U47-6)	627P		
7-D	(U47-8)	CHU8		
7-E	(U47-11)	8C36		
7-F	(U47-13)	FA11		
7-G	(U47-15)	41F7		
7-H	(U47-17)	HFP7		
7-J	(U47-18)	3F8H		
7-K	(U47-16)	PC84		
7-L	(U47-14)	627P		
7-M	(U47-12)	CHU8		

TEST 8. DRC Test (Service Sheet 22)

NOTE
Calibration factors will be lost when this test is performed.

a. Set instrument power to off.

b. Signature Analyzer connections:
START ⎍ to U41-37 (LMSYNC)
STOP ⎍ to U41-37 (LMSYNC)
CLOCK ⎍ to U41-9 (CLK)

c. Set rear panel CAL switch to the Unprotected position.

d. Set S1-B and S1-D to closed.

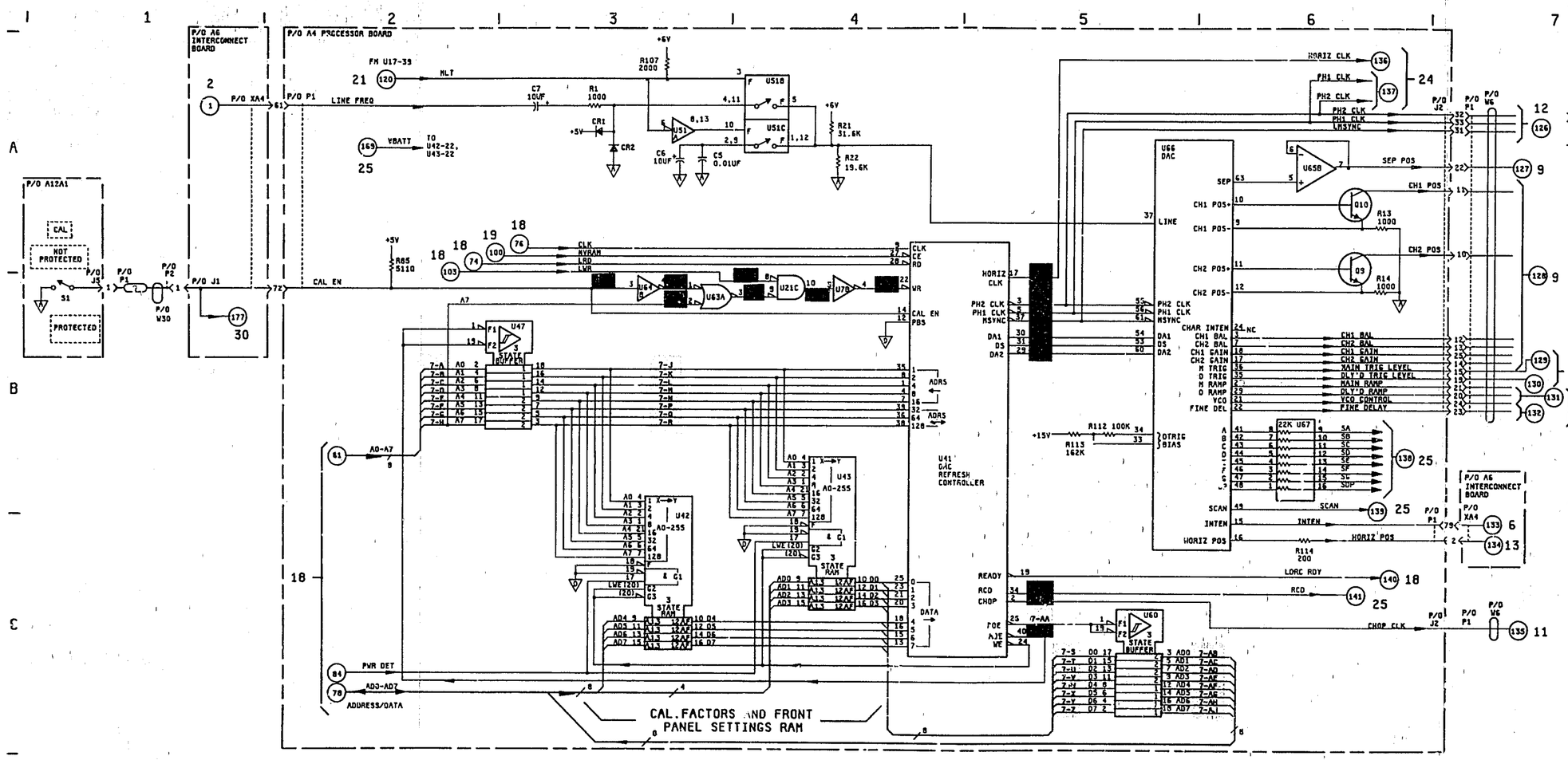
e. Set instrument power to on.

f. Set S1-C to closed.

g.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		7A70		
8-A	(U41-17)	A20F	22/B5	
8-B	(U41-3)	85F7		
8-C	(U41-5)	998P		
8-D	(U41-37)	7A8P		
8-E	(U41-30)	5P77 or UHUP		
8-F	(U41-31)	0439 or HUCF		
8-G	(U41-29)	92AA or 972F	22/C5	
8-H	(U41-34)	6AU1		
8-J	(U41-2)	A663		
8-K	(U41-40)	2H8P		

h. Set S1-B, S1-C, and S1-D to open.



IC DEVICE POWER CONNECTIONS

NC	1,2,4,57,58,59
+15V	14,19,26,30,40
+11V	51
+6V	52
-5V	4,6,38,50
-12V	13,20,31,64
	3,8,23,25,27,32, 39,62

U66

+6VF 6 10,32 -3VF (A) 11,33 U41

+5V 14 7 U7,21,63,64

YBATT 22 8 U42,43

+6 14 7 U51

+15V 8 -12V 4 U65

+5V 20 10 E8 U60

+5V 20 10 U47

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A4	P/O A6
C5-7 CR1,2 E8 P/O J2 P/O P1 Q9,10 R1,13,14,21,22,85,107, 112-114 U7B,21C,41-43,47,51,60, 63A,64B,65B,66,67	P/O XA4 P/O J1
	P/O A12A1
	S1 P/O J5
	CHASSIS
	P/O W6, P/O W30

1980/122/4/7/81

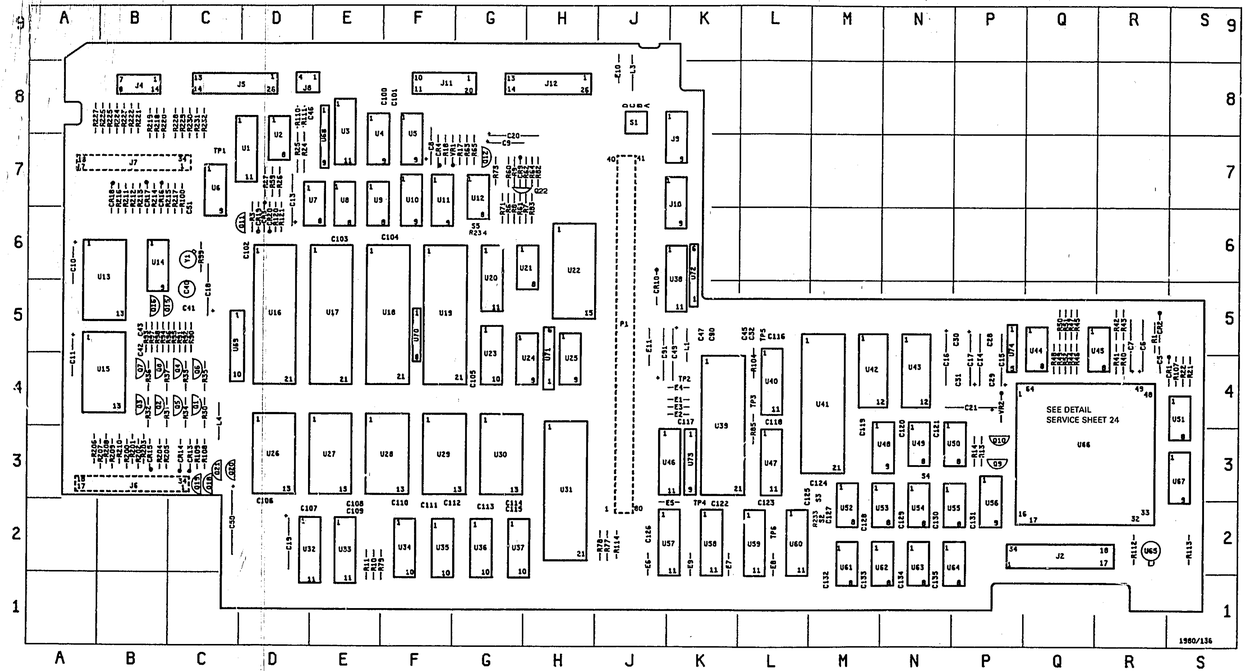
22

Service Sheet 22. Schematic Diagram
P/O Processor Board, Digital to Analog Subsystem

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	R-4	C114	G-2	J2	G-2	R24	D-7	R97	B-5	R231	C-8	U32	D-2
C6	R-5	C115	G-2	J4	B-8	R25	D-7	R98	B-5	R232	C-8	U33	E-2
C7	R-5	C116	L-5	J5	J-2	R26	D-7	R99	C-6	R233	M-2	U34	F-2
C8	F-7	C117	K-4	J6	B-3	R27	D-7	R100	C-7	R234	G-6	U35	F-2
C9	G-7	C118	L-4	J7	B-7	R30	C-4	R104	L-4	S1	J-8	U36	G-2
C10	A-6	C119	M-3	J8	D-8	R31	B-4	R107	S-4	S2	M-2	U37	G-2
C11	A-4	C120	N-3	J9	K-7	R32	B-4	R108	C-3	S3	M-2	U38	K-6
C13	D-7	C121	N-3	J10	K-7	R33	C-4	R109	C-3	S4	M-3	U39	K-4
C14	P-4	C122	K-2	J11	F-8	R34	C-4	R110	D-8	S5	G-6	U40	L-4
C15	P-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	D-7	U41	M-4
C16	N-4	C124	M-3	L1	K-5	R36	B-4	R112	R-2	TP2	K-4	U42	M-4
C17	P-4	C125	L-3	L2	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	M-4
C18	C-5	C126	J-2	L4	C-4	R40	R-4	R114	J-2	TP4	K-2	U44	G-5
C19	D-2	C127	M-2	P1	J-5	R41	R-4	R120	D-6	TP5	L-5	U45	R-5
C20	G-7	C128	M-2	Q1	C-4	R42	R-5	R121	D-6	TP6	L-2	U46	K-3
C21	P-4	C129	N-2	Q2	B-4	R43	R-5	R200	B-3	U1	D-7	U47	L-3
C28	P-5	C130	N-2	Q3	B-4	R44	Q-4	R201	B-3	U2	D-7	U48	N-3
C29	P-4	C131	P-2	Q4	C-4	R45	Q-5	R202	B-3	U3	E-7	U49	N-3
C30	P-5	C132	M-1	Q5	C-4	R46	Q-4	R203	B-3	U4	E-7	U50	N-3
C31	P-4	C133	M-1	Q6	C-4	R47	Q-5	R204	B-3	U5	F-7	U51	S-4
C32	L-5	C134	N-1	Q7	B-4	R48	Q-4	R205	B-3	U6	C-7	U52	M-2
C40	C-5	C135	N-1	Q8	B-4	R49	Q-4	R206	A-3	U7	E-7	U53	N-2
C41	C-5	CR1	S-4	Q9	P-3	R50	Q-5	R207	B-3	U8	E-7	U54	N-2
C42	B-5	CR2	R-5	Q10	P-3	R51	Q-5	R208	B-3	U9	E-7	U55	P-2
C43	B-5	CR3	D-5	Q11	D-5	R52	Q-4	R209	B-3	U10	F-7	U56	P-5
C45	L-5	CR4	F-7	Q12	G-7	R59	D-7	R210	B-3	U11	F-7	U57	K-2
C46	D-8	CR9	G-7	Q15	B-5	R60	G-7	R211	B-7	U12	G-7	U58	K-2
C47	K-5	CR10	J-5	Q16	B-5	R61	G-6	R212	B-7	U13	B-5	U59	L-2
C48	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	B-6	U60	L-2
C50	C-2	CR14	C-3	Q19	C-3	R63	G-7	R214	B-7	U15	B-4	U61	M-2
C51	C-8	CR15	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2
C90	K-5	CR16	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-5	U63	N-2
C91	J-4	CR17	B-7	Q22	G-7	R71	G-7	R217	B-8	U18	E-5	U64	N-2
C100	F-8	CR18	B-7	R1	R-5	R73	G-7	R218	B-8	U19	F-5	U65	R-2
C101	F-8	CR19	D-8	R3	D-6	R77	J-2	R219	B-8	U20	G-5	U66	G-3
C102	F-8	CR20	D-6	R4	G-6	R78	J-2	R220	B-8	U21	H-6	U67	S-3
C103	E-6	E1	K-4	R7	H-6	R79	E-2	R221	B-8	U22	H-6	U68	E-7
C104	F-6	E2	K-4	R8	G-6	R82	H-7	R222	B-8	U23	G-4	U69	C-6
C105	G-4	E3	K-4	R9	G-7	R83	H-6	R223	B-8	U24	H-4	U70	F-5
C106	D-2	E4	K-4	R10	E-2	R85	L-3	R224	B-8	U25	H-4	U71	H-4
C107	E-2	E5	K-2	R11	E-2	R90	C-5	R225	B-8	U26	D-3	U72	K-6
C108	E-2	E6	J-2	R13	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3
C109	E-2	E7	K-2	R14	P-3	R92	C-5	R227	A-8	U28	F-3	U74	P-5
C110	F-2	E8	L-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	F-7
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4
C112	F-2	E10	J-8	R21	S-4	R95	C-5	R230	C-8	U31	H-3	Y1	C-6
C113	G-2	E11	J-5	R22	S-4	R96	B-5						

A4



SERVICE SHEET 23 MNEMONICS

10 MHz TTL	**10 MHz oscillator output** — TTL levels.
A0-A15	**Address Lines 0 - 15** — A0-A7 are developed from the AD0-AD7 bus. A8 through A15 are most significant 8 bits of address.
AD0-AD7	**Address/Data bus** — Microprocessor bidirectional bus. Data on this bus can be the least significant 8 bits of address.
CCLK	**Character Clock** — Dot clock divided by seven — used by video controller.
CHAR DISP	**Character Display** — Bit determining character mode — if high characters are on — if low characters are off and option display is allowed.
CHAR RAM	**Character RAM** — Chip select decoded from address to select characters RAMs, A4U32 and A4U33.
CLK	**Clock** — From microprocessor — 3.333333 MHz processor clock input divided by two.
CSIO0	**Chip Select IO 0** — Chip select decoded from address to select IO device 0, A4U19 (Video Controller).
CSIO1	**Chip select IO 1** — Chip select decoded from address to select IO device 1, A4U31 (DMA Controller).
DCLK	**Dot Clock** — 10 MHz oscillator clock divided by two — used to generate timing for character display.
DISP	**Display** — Used to enable or disable display of characters - from RS flip-flop controlled by general purpose attributes.
DISP MODE	**Display Mode** — From IO to Programmable Logic Array (PLA) — allows character or Digital Waveform Storage Option display.
HCHEN	**High, Character Enable** — Signal which activates character ramps in vertical and horizontal outputs while also enabling gate circuit to receive Z-axis unblanking.
HCHRH	**High, Character Reset Horizontal** — Signal from video controller that activates and synchronizes the horizontal character ramp.
HCHRV	**High, Character Reset Vertical** — Signal from video controller that synchronizes and activates character ramp vertically.
HDB	**High, Display Blanking** — Option signal.
HDRQ0	**High, DMA Request 0** — From enhancement module requesting the DMA Controller to interrupt the microprocessor and take control of the address and data buses to service the enhancement module.
HDRQ1	**High, DMA Request 1** — From video controller requesting the DMA Controller to interrupt the microprocessor and take control of the address and data buses to service the video controller.
HDRQ2	**High, DMA Request 2** — From option requesting the DMA Controller to interrupt the microprocessor and take control of the address and data buses to service the option.
HDRQ3	**High, DMA Request 3** — Not used — tied low.
HLDA	**Hold Acknowledge** — Acknowledges a DMA Controller hold request when control of the address and data buses are available for control by the DMA Controller — also places proper levels to various devices during DMA cycles.
HOLD	**Hold** — Request from the DMA Controller to the microprocessor to interrupt its cycle so the DMA controller can take control of the address and data buses for DMA data transfer.
HTC	**High, Terminal Count** — From DMA Controller indicating the number of DMA cycles programmed have been completed. No more DMA requests will be honored until the DMA Controller has been reprogrammed by the microprocessor.

Service Sheet 23. Component Locator
P/O Processor Board, DMA and Video Control Subsystems

SERVICE SHEET 23 MNEMONICS (CONT'D)

LATCH EN	**Latch Enable** — Output of PLA to delay attributes while characters are shifted through shift register so that characters and attributes are in synchronization.
LCHZ	**Low, Character Z Blanking** — Shared by character generator and option to form characters or digitized waveform — all unwanted "spaces" are blanked after beam is unblanked by HCHEN and intensity level set by CHAR INTEN.
LCLD	**Low, Load Counter Dot** — Signal generated by PLA logic to reset dot clock counter during character vertical retrace.
LDACK0	**Low, DMA Acknowledge 0** — From DMA Controller to enhancement module acknowledging that processor has accepted interrupt and DMA data transfer has begun.
LDACK1	**Low, DMA Acknowledge 1** — From DMA Controller to video controller acknowledging that processor has accepted interrupt and DMA data transfer has begun.
LDACK2	**Low, DMA Acknowledge 2** — From DMA Controller to option acknowledging that processor has accepted interrupt and DMA data transfer has begun.
LDACK3	**Low, DMA Acknowledge 3** — Not Used.
LIOR	**Low, IO Read** — tells the selected IO device to output a byte of data on the AD0-AD7 lines. Usually controlled by the DMA Controller.
LIOW	**Low, IO Write** — indicates to the selected IO device that a data byte is available on the AD0-AD7 lines. The IO device will then latch the data. Usually controlled by the DMA Controller.
LMEMR	**Low, Memory Read** — causes the addressed memory location to be read. Usually controlled by the DMA Controller.
LMEMW	**Low, Memory Write** — causes the memory device to write the data byte on the AD0-AD7 lines to the addressed memory location.
LSR LOAD	**Low, Character Shift Load** — Allows data from character ROM to be loaded into shift register.
LTEN	**Light Enable** — Output of video controller caused by an underline character being decoded — causes an underline until another control character is encountered.
QA,QB,QC	Outputs of the dot clock divider.
RDY	**Ready** — Input to microprocessor — when low wait states are inserted into the microprocessor cycle to give peripherial device time to complete its function.
RESET	Reset pulse from microprocessor to initalize peripherals to proper states at power up or power down.
RST 6.5	**Restart 6.5** — Prioritized Interrupt Input to the Microprocessor — When pulled high by peripherial device normal microprocessor routine is interrupted and the microprocessor is placed in an interrupt service routine.
RVV	**Reverse Video** — Produced in the video controller by a control character being decoded to cause an inverse video display until another control character is decoded.
SR CLK	**Shift Register Clock** — Inverted DCLK to shift video data through the shift register.
VIDEO	**Video Serial Data** — From character ROM to PLA to form characters.
VSP	**Video Suppression** — Produced in the video controller by a control character being decoded to cause video to be blanked until another control character is encountered.

SERVICE SHEET 23 — THEORY OF OPERATION

Character Generator Subsystem. In order to facilitate the display of both scope settings and user-interactive information, an alphanumeric character generation system is used. This subsystem consists of a video controller (A4U19), 1K of volatile static RAM (A4U32,A4U33) for storing ASCII information to be displayed, a DMA controller (A4U31) to control high speed data transfers from the 1K character RAM to the video controller, a dot pattern character generator ROM (A4U23), and support circuitry to control and synchronize the video output.

Video Controller. The Video Controller (A4U19) is a special IO port for controlling raster scan type video monitors. Its basic function is to acquire data from a RAM via a DMA channel, to buffer this data internally on a row by row basis, and synchronously output this information to a character generator ROM in a repetitive fashion so that the desired dot pattern is output at the correct time to the Z axis amplifier. In addition, the Video Controller generates the required horizontal and vertical reset pulses at the proper time to ensure that the vertical and horizontal ramps are synchronized to the Z axis video information.

As an additional function, the Video Controller provides control character decoding of buffer characters and outputs appropriate control signals to manipulate such features as reverse video, blanking, underline, etc. The Video Controller also generates an interrupt near the end of each video frame which is used to flag the processor that the DMA controller must be reinitialized for the next frame of data transfers.

Data Acquisition. One of the principle functions of the Video Controller (A4U19) is to initiate data transfers via DMA channel from the character RAM into its internal buffers. In order to accomplish this, a handshake must exist between the Video Controller and the DMA controller. Two signals are required. The first, which orginates from the Video Controller, is the HDRQ1 (High, DMA Request 1) output. When HDRQ1 is high, this is sensed by the DMA controller. The DMA Controller then asserts a HOLD request to the microprocessor. When the processor completes its current bus cycle, it three states the address and data bus, then issues a HLDA (Hold Acknowledge) to the DMA Controller to acknowledge the HOLD request. The DMA controller then initiates a data transfer from the character RAM (A4U32, A4U33) to the Video Controller and generates a second pulse, LDACK1, to the Video Controller (A4U19).

This data transfer assumes the form of a simultaneous memory read/IO write bus cycles. The DMA controller (A4U31) outputs a 16 bit address onto the address bus. A0-A7 are driven directly by the DMA Controller (A4U31) while A8-A15 are driven by an 8 bit register (A4U58). This register (A4U58) is loaded by the DMA Controller in a manner similar to the way the microprocessor (A4U39) outputs its lower address lines, via the data bus. During the initial portion of the DMA cycle, the data bus AD0-AD7 will be driven by the DMA Controller (A4U31), and will contain the address bits A8-A15 for the DMA transfer. The DMA Controller (A4U31) activates the ADSTB line, which strobes this information into the register (A4U58). The address bus A0-A15 will then contain address information which will be decoded, causing the RAM's (A4U32,A4U33) to be chip enabled.

At this point the DMA Controller (A4U31) ceases to drive the data bus and acknowledges the Video Controller (A4U19) with the LDACK1 signal. This signal, which is connected to the DACK input of the Video Controller, tells the Video Controller (A4U19) that its DMA request has been acknowledged and that a memory read/IO write cycle is underway.

The DMA Controller (A4U31), in addition to having control over A0-A15, also has control over LMEMR, LMEMW, LIOR, and LIOW. The LMEMR and LIOW strobes are then driven low by the DMA Controller (A4U31). LMEMR will cause the RAMS (A4U32, A4U33) to output a byte of character data onto the data bus AD0-AD7. LIOW then signals the Video Controller (A4U19) to latch the information on AD0-AD7 and store the transferred byte into its internal storage buffer. At this point a single byte transfer has been completed and the LDACK1 strobe is brought back high by the DMA Controller (A4U31).

The two 1K X 4 NMOS RAM's (A4U32,A4U33) are used as a buffer for the character generator, and as the processor stack. These devices are accessed by both the microprocessor (A4U39) and the DMA Controller (A4U31) and have independent output enables which are connected to the LMEMR line. Therefore, the chip enable for these devices goes low true at the beginning of the bus cycle, and are not gated with LMEMR or LMEMW.

The Video Controller (A4U19) has several DMA request formats which are programmable. In the format which is currently used, DMA requests are in bursts of 38, so that one entire row of characters is acquired each time the microprocessor is placed into a hold state. Therefore, 38 of the previously described cycles are executed sequentially. Each cycle is identical to the one described above, with the exception that with each cycle the address presented by the DMA Controller (A4U31) is incremented by 1. Once an entire row is acquired by the Video Controller (A4U19), DMA requests cease and the processor is allowed to regain bus control and continue executing until the Video Controller (A4U19) requires more data for the next row.

A total of 20 such bursts of DMA is required during each video frame, each burst being a 38 byte transfer. Once the last burst is complete, the internal terminal count register in the DMA Controller (A4U31) will have been decremented to zero and reached the "terminal count" state. Further DMA requests made by the Video Controller (A4U19) cannot be acknowledged until this terminal count register within the DMA Controller (A4U31) has been re-initialized. This re-initialization must be done by the processor via IO instructions to the DMA Controller (A4U31).

The processor is signaled that a frame is nearing completion by the Video Controller. When the Video Controller begins outputting the final row of characters it drives the RST 6.5 output high. The microprocessor is then vectored to an interrupt service routine which procedes to re-initilize the DMA controller. This procedure will be complete before the Video Controller begins requesting DMA for the next frame. This request comes near the end of the vertical retrace interval, several hundred microseconds after the RST 6.5 microprocessor interrupt.

Video Output. A primary function of the Video Controller (A4U19) is to provide the basic timing and synchronization functions required for video output. The Video Controller is directly responsible for generating the vertical and horizontal retrace pulses which are used to reset the vertical and horizontal ramp generators on the low voltage power supply board. A third function of the Video Controller is to sequentially present each of the characters in each row to an external character generator ROM (A4U23), along with the line count code, so that a 5 bit dot pattern can be accessed, loaded, and shifted out as Z-axis video data.

During the display of each row of characters, 9 horizontal lines must be drawn on the screen. The entire row of character data must be output to the character generator ROM 9 times. During the first line, the Video Controller line counter outputs, LC0-LC2, are held at all 0s. Each character in the row will appear on the Video Controller outputs, CC0-CC6, and will be held stable for one character clock period. This period is determined in the Video Controller by the frequency of the Video Controller input CCLK which is driven at 714.286 KHz or 1.4 us. During this 1.4 us period the character generator ROM must access the proper 5 bit pattern for the given ASCII character and line count. The five outputs of this device are then loaded into an external shift register (A4U24) in parallel. The Video Controller then presents the next character in the row to the character ROM, while the first character dot pattern is shifted out to the Z-axis.

The Video Controller contains two memory arrays which are used as temporary storage of characters. Each array has enough memory to store a single row of characters. When the Video Controller does DMA, it will store the transferred data into one of its two row buffers. While this is occurring, the other row buffer is being used for video output. When the video output for one row is complete, the other row buffer is used and the Video Controller begins the video output for the next row using the newly loaded buffer. The first buffer, which now contains old data, is used as storage for the next burst of DMA. These two buffers are therefore interleaved back and forth. While one buffer is being used for video output, the other is being used as data storage during DMA.

Control Character Decoding. As mentioned previously, the Video Controller (A4U19) is programmed to support 38 characters per row, with 20 rows per frame, for a total of 760 characters. Not all of these characters are actual displayed ASCII data. In fact, only 33 of the 38 characters in each row are displayable characters. Five are reserved for control.

The Video Controller has the internal capability of recognizing and responding to the presence of control characters placed within a row. These characters are placed in context with other ASCII data in order to modify the display of the data. Such functions as reverse video, blinking, and underline are implemented with these control codes. Whenever the Video Controller encounters a control character during the output of a line the appropriate external signal is activated. For example, when a reverse video character is encountered, the Video Controller output RVV is brought high, and will remain high until either the end of the line or until another control character appears which will shut off the reverse video field. This RVV line is gated into external logic and essentially causes the video Z-axis output to be inverted.

Other Video Controller outputs which are effected by control characters are VSP (video suppress), LTEN, GPA0 and GPA1. VSP is brought high whenever the video output is to be turned off, and will periodically go high and low during horizontal and vertical retrace periods. However, if a blink control character is placed ahead of a character string, VSP will be activated at a very slow rate during these character periods such that the field will blink on and off. Another control character is required at the end of the field to be blinked.

The LTEN output is activated by the underline control character in a similar manner to reverse video. The LTEN signal is gated via external logic into the Z-axis output. The Video Controller is responsible for timing the occurrence of LTEN so that it appears on the proper line of the row, and at the proper character period. The actual line of dots is caused by the LTEN signal going high and being gated into the Z-axis.

The two outputs GPA0 and GPA1 are general purpose attribute signals and are generated by a general purpose control character. These two signals will be activated for one character period only and are used in the 1980 to perform a very special function. GPA0 and GPA1 are the set and reset inputs to a cross-coupled NOR latch (A4U21). The output of this latch is a signal called DISP. DISP is latched high whenever a control character appears in a row which activates GPA0, and is reset low whenever a GPA1 control character appears. The DISP signal is then gated within the PLA (Programmable Logic Array) (A4U22) with vertical retrace and becomes the signal HCHEN (High, Character Enable). Whenever HCHEN is high, the sweep will be chopped so that characters can be displayed on the CRT. Whenever HCHEN is low, the sweep is allowed to continue on the CRT even though the character x, y, and z axis are still operating. What this affects is size of the "hole" which appears in the sweep at lower sweep rates.

During a normal display only two rows of characters appear on the top of the frame, and two rows at the bottom. Only 4 of the 20 rows are actually displaying meaningful data, with 16 blank rows. Each blank row requires just as much output time as the active rows. A GPA1 control character can be placed in the beginning of the unused row, causing DISP to latch low for the entire row, and allowing the sweep to continue uninterrupted until the next GPA0 control character is encountered. This would normally be the beginning of the next row which contains meaningful data and would cause DISP to latch high. This in turn activates HCHEN and causes the sweep to be chopped until the next GPA1 character is encountered.

External Timing and Syncronization. The basic input to this circuitry is a 10 MHz TTL clock which originates from the master clock oscillator. This clock drives a flip flop (A4U8B) connected in a "toggle" configuration so that a 5 MHz output is produced. This output is referred to as the signal DCLK (Dot Clock) and establishes the dot period for raster scan. The character format provides for a 7 × 9 dot matrix for each character, with an actual 5 × 7 character construction surrounded by a perimeter of blank dots. The vertical dimension of 9 dots is programmed into the Video Controller as the number of lines per row. The horizontal dimension of 7 is built into the timing circuitry through the use of a counter (A4U11). This counter is clocked by the DCLK and is programmed to divide the dot clock by 7. The three outputs of the counter, QA, QB, and QC are decoded within the PLA (Programmable Logic Array) (A4U22) such that when the counter reaches state 6 a LCLD (Low, Counter Load) is output by

the PLA and, on the next clock edge, resets the counter state to zero. The most significant output of this counter QC, is buffered in the PLA and is used to generate the Video Controller input CCLK (Character Clock). Thus CCLK is the DCLK divided by 7. The QA, QB, and QC inputs to the PLA are also decoded at counter state 5 and gated with the low portion of DCLK to generate a low true 100 ns shift register load pulse (LSR LOAD) used to parallel load the 5 dot output of the character ROM into the shift register (A4U24). The PLA also inverts DCLK to generate the shift register clock required to shift the video data out of the shift register.

All of the various control signals generated by the Video Controller (A4U19) (VRTC, HRTC, GPA0, GP01, LTEN, RVV and VSP) assume a valid state coincident to the falling edge of the Video Controller input CCLK, which is the same edge where the character code and line count outputs change state. Since actual video output of this character does not occur until several dot clock periods later, when the shift register is parallel-loaded, the control lines associated with the current character must be delayed or shifted in time such that the timing of these signals is coincident with the actual video output of the character. This time shift is implemented with a register (A4U20). The gate (clock) input to this register is the positive true version of the shift register (LATCH EN) load pulse and is generated by the PLA using the QA, QB, QC and DCLK PLA inputs. The attributes and controls generated for a given character are actually gated and latched five DCLK periods later, when the video shift operation begins.

Programmable Logic Array. A PLA (Programmable Logic Array) (A4U22) has been used to implement various combinational logic functions required by the external synchronization logic. The PLA consists of 16 inputs and 8 outputs. The 16 inputs and and their complements are internally connected to 48 AND gates inside the PLA. The 48 outputs from these gates then internally connect to the inputs of 8 OR gates. The output and the complementary output of each OR gate is connected to an output pin of the PLA. Each of the internal gate inputs contains a ni-chrome fuse that, when blown, causes that input to be a "don't care". In addition, a fuse exists on the 8 OR gate outputs that, when blown, causes the complimentary, or NOR output to connect to the output pin.

Using this device, a boolean function of AND/OR combinations has been programmed into the PLA such that the outputs F0 - F7 each contain a unique logic function. The logical function of the outputs CCLK, HCHEN, SR CLK, LATCH EN, LSR LOAD, LCHZ, and LCLD are shown on Service Sheet 23.

DMA Controller. Although a basic description of how the DMA Controller interacts with the Video Controller was given in a previous section, it is perhaps necessary to fully describe the features of this device, and the extent of its capabilities within the 1980.

The DMA Controller (A4U31) is a programmable bus cycle controller which contains four separate DMA channels, one of which is used by the Video Controller. The DMA Controller is used to facilitate high speed data transfers between memory and IO. Associated with each DMA channel are two distinct 16 bit registers within the DMA Controller and an individual pair of DMA request/acknowledge control signals DRQ0-3 and DACK0-3). One of the two registers associated with each channel is called the DMA address register. This register contains a memory address and is used as an address for the memory accesses associated with that channel. The other register is called the terminal count register, and is used to determine the number of DMA accesses that will occur on a given DMA channel before DMA on that channel is stopped. These registers must be preprogrammed, into the DMA controller before a DMA transaction can occur, through the use of IO instructions from the microprocessor. The DMA controller IC itself has a unique IO address space where these registers are accessed.

Once a DMA channel has been initialized by the processor, DMA requests received on that channel will be acknowledged by the DMA Controller and DMA transactions can occur. The type of transaction (memory to IO vs IO to memory) must also be programmed into a control register within the DMA Controller to determine how the four bus controls LMEMR, LMEMW, LIOR, and LIOW will be manipulated by the DMA Controller.

On the first DMA following initialization of the channel, the memory address that will appear on the address bus will be the initialized value of the DMA address register. At the completion of the first, and each subsequent DMA cycle, the value of the DMA address register is automatically incremented by 1, while the internal terminal count register is decremented by 1. When the terminal count register reaches zero, this indicates that the desired number of transfers has occurred and further DMA requests are not acknowledged. The TC output (HTC) of the DMA Controller will go high when terminal count is reached.

An important principle to note about the DMA Controller is that during DMA byte transfers the DMA Controller provides only the memory address. The other part to the transfer, the IO port, is enabled via the DACK output, and not via an address decoder. This is known as one cycle DMA. The power of the device lies in the fact that in four clock periods (the time required to fetch an instruction by the microprocessor) a memory read/IO write or IO read/memory write operation can occur.

SERVICE SHEET 23 SIGNATURE ANALYSIS

Note
Remove Expansion Module before performing tests

TEST 9. DMA Address Latch Test (Service Sheet 23)

a. Set instrument power to off.

b. Signal Analyzer connections:
START ⎍ to U19-8 (VRTC)
STOP ⎍ to U20-3 (VRTC)
CLOCK ⎏ to U31-24 (LDACK1)

c. Set instrument power to on.

d. Press front panel OPTION MENU key; then press soft key 1.

e.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		U2H7		
9-A	(U31-30)	5UUP	23/B2	
9-B	(U31-29)	HCCC		
9-C	(U31-28)	U2H7		
9-D	(U31-27)	0000		
9-E	(U31-26)	0000		
9-F	(U31-23)	U2H7		
9-G	(U31-22)	U2H7		
9-H	(U31-21)	0000		

TEST 10. DMA Transfer Test (Service Sheet 23)

a. Set instrument power to off.

b. Logic Analyzer connections:
START ⎍ to U19-8 (VRTC)
STOP ⎍ to U20-3 (VRTC)
CLOCK ⎍ to U31-24 (LDACK1)

c. Set instrument power to on.

d. Press front panel OPTION MENU key; then press soft key 1.

e.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5		U2H7		
10-A	(U31-32)	51C2	23/A2	
10-B	(U31-33)	FU6P		
10-C	(U31-34)	3FP3		
10-D	(U31-35)	UFOP		
10-E	(U31-37)	C34U		
10-F	(U31-36)	F968		
10-G	(U31-39)	PCH4		
10-H	(U31-40)	AU8A		
10-J	(U58-2)	5UUP	23/B3	
10-K	(U58-5)	HCCC		
10-L	(U58-6)	U2H7		
10-M	(U53-9)	0000		
10-N	(U58-12)	0000		
10-P	(U58-15)	U2H7		
10-Q	(U58-16)	U2H7		
10-R	(U58-19)	0000		
10-S	(U19-12)	92C7	23/B4	
10-T	(U19-13)	AP34		
10-U	(U19-14)	3HHH		
10-V	(U19-15)	6FU8		
10-W	(U19-16)	A2P7		
10-X	(U19-17)	9A84		
10-Y	(U19-18)	F3F2		
10-Z	(U19-19)	445U		

TEST 11. Video Controller Test (Service Sheet 23)

a. Set instrument power to off.

b. Signal Analyzer connections:
START ⎏ to U19-8 (VRTC)
STOP ⎏ to U20-3 (VRTC)
CLOCK ⎏ to U19-30 (CCLK)

c. Set instrument power to on.

d. Press front panel OPTION MENU key; then press soft key 1.

e.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		H953		
11-A	(U19-23)	*	23/A5	
11-B	(U19-24)	*		
11-C	(U19-25)	*		
11-D	(U19-26)	*		
11-E	(U19-27)	*		
11-F	(U19-28)	*		
11-G	(U19-29)	*		
11-H	(U19-4)	U40P		
11-J	(U19-3)	A91F		
11-K	(U19-2)	PC89		
11-L	(U23-12)	*		
11-M	(U23-13)	*		
11-N	(U23-14)	*		
11-P	(U23-15)	*		
11-Q	(U23-16)	*		
11-R	(U24-9)	*	23/A6	
11-S	(U19-6)	12HA	23/B5	
11-T	(U19-7)	5C4H		
11-U	(U19-33)	F2U1		
11-V	(U19-34)	9P1P		
11-W	(U19-37)	logic 0		
11-X	(U19-36)	logic 0		
11-Y	(U19-35)	UAH3		
11-Z	(U20-2)	12HA	23/B5	
11-AA	(U20-6)	5C4H		
11-AB	(U20-19)	F2U1		
11-AC	(U20-16)	9P1P		
11-AD	(U20-5)	logic 0		
11-AE	(U20-12)	logic 0		
11-AF	(U20-15)	UAH3		
11-AG	(U21-4)	178F	23/B6	
11-AH	(U21-1)	FPHU		
11-AJ	(U22-26)	logic 1	23/B6	
11-AK	(U22-8)	logic 0		
11-AL	(U22-10)	0000	23/B7	
11-AM	(U22-18)	H953		
11-AN	(U22-17)	0000		
11-AP	(U22-13)	0556		
11-AQ	(U22-16)	C4F4	23/C7	

*Random data which is later blanked causes nonvalid signatures to be obtained on these test points.

SERVICE SHEET 23 SIGNATURE ANALYSIS (Cont'd)

Note
Remove Expansion Module before performing tests

TEST 12. Video Sync Logic Test (Service Sheet 23)

a. Set instrument power to off.

b. Remove resistor R234 jumper from S5.

c. Signal Analyzer connections:
START ⌝ to U11-11
STOP ⌝ to U11-11
CLOCK ⌐ to U8-9 (DCLK)

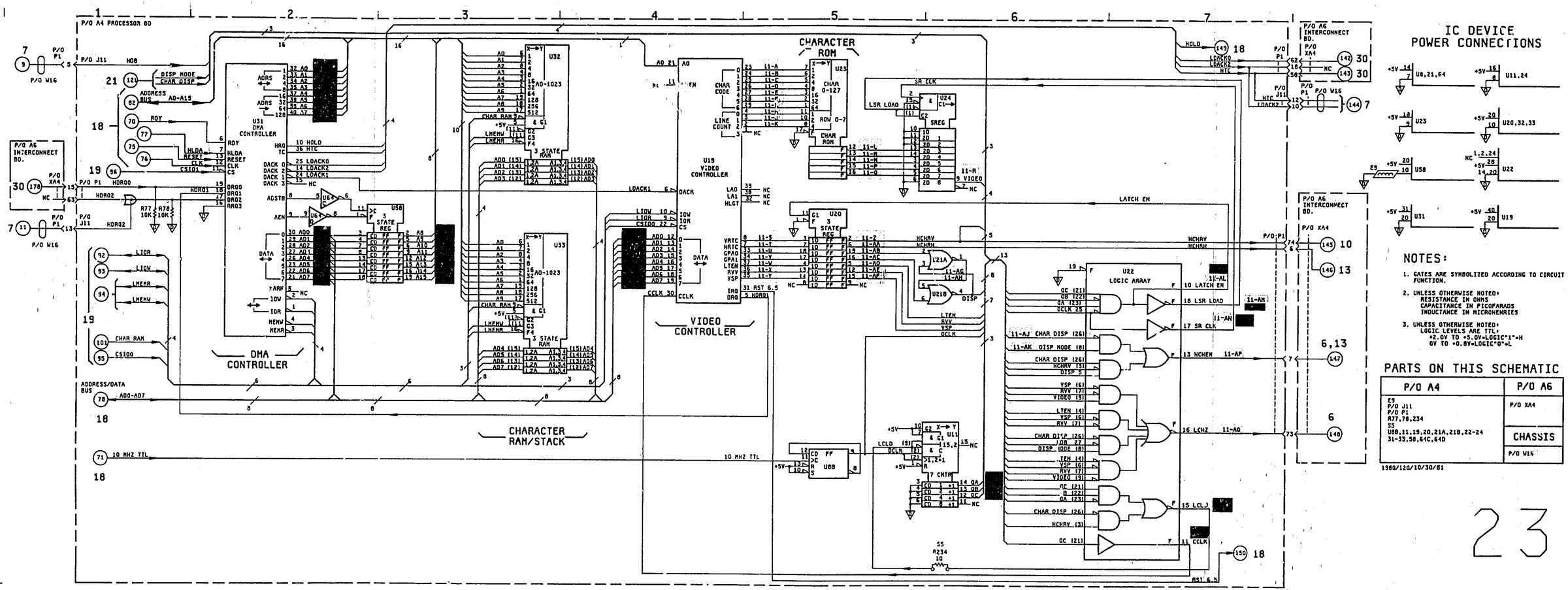
d. Set instrument power to on.

e.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5		UP73		
12-A	(U11-14)	55H1	23/C6	
12-B	(U11-13)	334U		
12-C	(U11-12)	0U16		
12-D	(U22-10)	040P	23/B7	
12-E	(U22-18)	UA7H		
12-F	(U22-17)	UP73		
12-G	(U22-15)	UF74	23/C7	
12-H	(U22-11)	0U16		

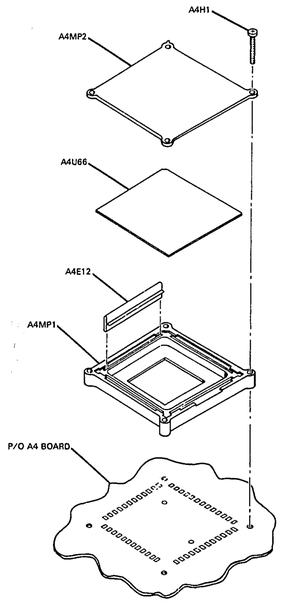
f. Set instrument power to off.

g. Reinsert R234 into S5.



23

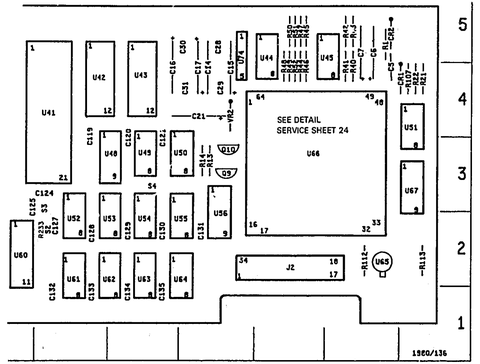
Service Sheet 23. Schematic Diagram
P/O Processor Board, DMA and Video Control Subsystems
8-179



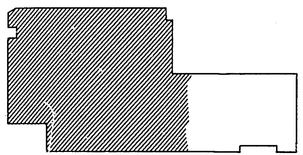
DETAIL OF HYBRID ASSEMBLY

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	R-4	C114	G-2	J2	Q-2	R24	D-7	R97	B-5	R231	C-8	U32	D-2		
C6	R-5	C115	G-3	J4	B-8	R26	D-7	R98	B-5	R232	C-8	U33	E-2		
C7	R-5	C116	G-2	J5	C-8	R26	D-7	R99	G-6	R23[illegible]	M-2	U34	F-2		
C8	F-7	C117	K-4	J6	B-3	R27	D-7	R100	C-7	R2[illegible]	G-6	U35	F-2		
C9	G-7	C118	L-4	J7	B-7	R30	C-4	R104	L-4	S1	J-8	U36	G-2		
C10	A-6	C119	M-3	J8	D-8	R31	B-4	R107	S-4	S2	M-2	U37	G-2		
C11	A-4	C120	N-3	J9	K-7	R32	B-4	R108	C-3	S3	M-2	U38	K-6		
C13	D-7	C121	N-3	J10	K-7	R33	C-4	R109	C-3	S4	N-3	U39	K-4		
C14	P-4	C122	K-2	J11	F-8	R34	C-4	R110	D-8	S5	G-6	U40	L-4		
C15	P-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	C-7	U41	M-4		
C16	N-4	C124	M-3	L1	K-5	R36	B-4	R112	R-2	TP2	K-4	U42	M-4		
C17	P-4	C125	L-3	L3	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	N-4		
C18	C-5	C126	J-2	L4	C-4	R40	R-4	R114	J-2	TP4	K-2	U44	Q-5		
C19	D-2	C127	M-2	P1	J-5	R41	R-4	R120	D-6	TP5	L-5	U45	R-5		
C20	G-7	C128	M-2	Q1	C-4	R42	R-5	R121	D-6	TP6	L-2	U46	K-3		
C21	P-4	C129	N-2	Q2	B-4	R43	R-5	R200	B-3	U1	D-7	U47	L-3		
C28	P-5	C130	N-2	Q3	B-4	R44	Q-4	R201	B-3	U2	D-7	U48	N-3		
C29	P-4	C131	P-2	Q4	C-4	R45	Q-5	R202	B-3	U3	E-7	U49	N-3		
C30	P-5	C132	M-1	Q5	C-4	R46	Q-4	R203	B-3	U4	E-7	U50	N-3		
C31	P-4	C133	M-1	Q6	C-4	R47	Q-5	R204	B-3	U5	F-7	U51	S-4		
C32	L-5	C134	N-1	Q7	B-4	R48	Q-4	R205	B-3	U6	C-7	U52	M-2		
C40	C-5	C135	N-1	Q8	B-4	R49	Q-4	R206	A-3	U7	E-7	U53	N-2		
C41	C-5	CR1	S-4	Q9	P-3	R50	Q-5	R207	B-3	U8	E-7	U54	N-2		
C42	B-5	CR2	R-5	Q10	P-3	R51	Q-5	R208	B-3	U9	F-7	U55	P-2		
C43	B-5	CR3	D-6	Q11	D-5	R52	Q-4	R209	B-3	U10	F-7	U56	P-5		
C45	L-5	CR4	F-7	Q12	G-7	R59	D-7	R210	B-3	U11	F-7	U57	K-2		
C46	D-8	CR9	G-7	Q15	B-5	R60	G-7	R211	B-7	U12	G-7	U58	K-2		
C47	K-5	CR10	J-5	Q16	B-5	R61	G-6	R212	B-7	U13	B-6	U59	L-2		
C49	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	B-6	U60	L-2		
C50	C-2	CR14	C-3	Q19	C-3	R63	G-7	R214	B-7	U15	B-4	U61	M-2		
C51	C-6	CR15	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2		
C52	K-6	CR16	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-5	U63	N-2		
C91	J-4	CR17	B-7	Q22	G-7	R71	G-6	R217	C-7	U18	F-5	U64	P-2		
C100	F-8	CR18	B-7	R1	R-5	R73	G-7	R218	B-8	U19	F-5	U65	R-2		
C101	F-8	CR19	D-6	R3	D-6	R77	J-2	R219	B-8	U20	G-5	U66	Q-3		
C102	D-6	CR20	D-6	R6	G-6	R78	J-2	R220	B-8	U21	H-6	U67	S-3		
C103	E-6	E1	K-4	R7	H-6	R79	E-2	R221	B-8	U22	H-6	U68	E-7		
C104	F-6	E2	K-4	R8	G-6	R82	H-7	R222	B-8	U23	G-4	U69	C-5		
C105	G-4	E3	K-4	R9	G-7	R83	H-6	R223	B-8	U24	H-4	U70	F-5		
C106	D-2	E4	K-4	R10	E-2	R85	L-3	R224	B-8	U25	h-4	U71	H-4		
C107	E-2	E5	K-2	R11	E-2	R90	C-5	R225	B-8	U26	D-3	U72	K-5		
C108	E-2	E6	J-2	R13	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3		
C109	E-2	E7	K-2	R14	P-3	R92	C-5	R227	A-8	U28	F-3	U74	P-5		
C110	F-2	E8	L-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	F-7		
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4		
C112	F-2	E10	J-8	R21	S-4	R95	C-5	R230	C-8	U31	H-3	Y1	C-6		
C113	G-2	E11	J-5	R22	S-4	R96	B-5								



A4



SERVICE SHEET 24 MNEMONICS ,

BCD SHIFT — BCD Shift Clock — Used to shift the 56 bit serial data (DATA IN) through the shift register from horizontal interface to IO port.

BCD1 — 56-bit serial data from microprocessor to horizontal microcircuit with sweep instructions.

BCD2 — 56-bit serial data from horizontal microcircuit to microprocessor used to effect VCO frequency control.

BUSY — Goes high at the beginning of CYCLE ST and remains high until the end of the BCD frame - to processor via IO port.

CYCLE ST — Cycle Start — Output by processor via IO port to sync horizontal interface communications.

DATA IN — 56 bit data string from horizontal microcircuit to :BCD2 via horizontal interface) to calibrate VCO frequency.

HORIZ CLK — Horizontal Clock — Derivative of processor clock from the DAC Refresh Controller to horizontal interface to develop synchronous communications.

HSYNC — Horizontal Sync — From processor horizontal interface to horizontal microcircuit to synchronize processor/horizontal state changes.

IS — Instruction String — A 10 bit serial data string sent to the horizontal microcircuit to denote that a state change instruction is to follow.

IS SHIFT — Instruction String Shift — Signal to shift SDTA through the Instruction shift register to produce the 10 bit instruction string (IS).

LIN/OUT — Low, Input/High, Output — Controls direction of BCD data into or out of the horizontal microcircuit.

PH1 CLK — Phase 1 Clock — Processor clock divided by eight from the DRC to the DAC and horizontal microcircuit

PH2 CLK — Phase 2 Clock — Processor clock divided by eight from the DRC to the DAC and horizontal microcircuit — displaced from PH1 CLK by two processor clock periods.

SDTA — Serial Data — Data string from IO to various shift registers that when clocked into the shift register strings initiates various functions, lamps, etc.

Service Sheet 24. Component Locator
P/O Processor Board, Horizontal Interface

SERVICE SHEET 24 — THEORY OF OPERATION

Horizontal Interface. Communication between the microprocessor and the horizontal microcircuit is required whenever the status of the horizontal system is modified, or whenever the voltage controlled delay time oscillator is calibrated. The horizontal microcircuit, located on the scope board (A5), is interfaced to the processor system via a bi-directional, serial synchronous data link. The horizontal microcircuit receives two data inputs from the microprocessor. The IS (Instruction String) line, which contains instruction data, and the BCD1 line, which is used by the processor to transmit data pertinent to the instruction. The horizontal microcircuit returns to the processor the BCD2 signal, over which data is transmitted back to the processor whenever a read command appears in the IS field. The IS field is 10 bits long with the first two least significant bits defined as 0s. The BCD field (both BCD2 and BCD1) is 56 bits in length. In addition to these data lines, the processor board generates two phase clocks, PH1 CLK and PH2 CLK, and a HSYNC output, which is used to define the boundaries of the transmission frame.

In order to initiate a data transmission to the horizontal microcircuit the processor will serially load two shift registers. Data for those registers is output by the processor over the SDTA line, in a method similar to that used in loading data out to shift register strings. Two shift clocks, IS SHIFT and BCD SHIFT are provided via output ports from I/O ROM (A4U18) and are toggled under software control to load the contents on SDTA into either the 8 bit IS register (A4U55), or the 56 bit BCD register (A4U56).

Once these two registers are loaded, the processor initiates a synchronous communication cycle by pulsing the output port of I/O ROM (A4U17) CYCLE ST high. This pulse will set a flip flop within the synchronization logic of the horizontal interface. Then, at the beginning of the next HSYNC period, the data in the IS and BCD registers is shifted out to the horizontal. The data outputs are shifted coincident with the leading edge of PH2 CLK and are sampled by the horizontal during the next PH1 CLK pulse period.

The IS word is the first field to be transmitted. Although the transmission is begun on the leading edge of HSYNC, the actual shifting of the IS register does not begin until the 3rd PH2 CLK pulse, since during the 1st and 2nd bit times the IS data is held to 0. On the third bit period, the LSB of the IS register will appear on the IS line. The IS register is then continually shifted through the rest of the frame. However, only the first 10 bits are sampled and decoded by the horizontal microcircuit, with the trailing edge of HSYNC designating the end of the IS field.

Two bit times after the IS frame completes the BCD frame begins. The 56 bit BCD register (A4U56) is then shifted in sync with PH1 CLK. If the cycle is a transmit from the processor to the horizontal, the data that was pre-loaded into the BCD register (A4U56) will appear on the output (A4U56 pin 10) during the leading edge of each PH1 CLK of the BCD frame. This data is then resynchronized to PH2 CLK by a flip flop (A4U62A) so that the BCD1 line will be stable during the next PH1 CLK, when it is sampled by the horizontal hybrid. The BCD register is clocked by 56 PH1 CLKs during this operation.

If the cycle is to be a receive operation from the horizontal to the processor, the BCD1 line must be held to a high state in order to avoid internal hardware conflicts within the horizontal hybrid. Before the cycle is started, the processor asserts the output port LIN/OUT low. This forces the BCD1 line high by holding the PH2 CLK synchronization flip flop (A4U62A) preset.

When CYCLE ST is pulsed, the IS field will have been loaded with a READ command. The IS field is then transmitted normally, ending with the trailing edge of HSYNC. During the two bit period between the end of the IS field and the beginning of the BCD field, the horizontal microcircuit decodes the READ command. During the first PH2 CLK period of the BCD field the horizontal microcircuit will begin placing data onto the BCD2 line. Since the 56 bit BCD register is shifted coincidental with PH1 CLK, the data on BCD2 will be sampled during its stable state. The BCD shift register (A4U56) has two selectable inputs. The SDTA input is normally selected, but during the BCD frame, the BCD2 input is selected by the synchronization logic.

The BCD shift register is sequentially clocked for 56 bit times, and is loaded with the data on the BCD2 line. When the cycle is complete, the processor then begins pulsing BCD SHIFT and reads the contents of the BCD register on the input IO port DATA IN.

It can be noted that the only hardware state change which differentiates a transmit from a receive cycle is the preset of the BCD1 line by LIN/OUT. The significance of this is that, during both transmit and receive cycles, the contents of the BCD2 line are shifted into the BCD registers as the contents of the BCD register are shifted out to the BCD1 line. During transmit cycles, the BCD2 line is the 'echo' of what is present on BCD1 which effectively causes the contents of the BCD register to be recirculated. However, this does not occur in the 8 bit IS register. Once its information is transmitted, it continues to be clocked and the state of the SDTA port will be shifted into the IS register (either all 0s or all 1s).

During each transmit or receive cycle, a status input to the processor is activated. This signal, BUSY, is asserted high at the leading edge of the CYCLE ST pulse and remains high until the end of the BCD frame.

SERVICE SHEET 24 SIGNATURE ANALYSIS

Note
Remove Expansion Module before performing tests

TEST 13. Horizontal IF Timing and Control Test (Service Sheet 24)

a. Set instrument power to off.

b. Signature Analyzer connections:
START ⎍ to U48-12
STOP ⎍ to U49-1
CLOCK ⎍ to U41-9 (CLK)

c. Set S1-B, S1-C, and S1-D to closed.

d. Set instrument power to on.

e. Connect signature analyzer to test point U63-6 (13-P). Verify signature displayed is A276. If signature is correct, go to next test. If signature is incorrect perform tests in step f.

f.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5V		991H		
13-A	(U64-11)	UA1A	24/A3	
13-B	(U64-10)	6307		
13-C	(U64-13)	1502		
13-D	(U64-12)	6F1U		
13-E	(U48-2)	AP86	24/B1	
13-F	(U48-11)	49H6	24/C2	
13-G	(U48-12)	2768		
13-H	(U49-3)	F8HA	24/B2	
13-J	(U49-5)	P8C1		
13-K	(U49-13)	U4H5	24/C2	
13-L	(U50-5)	AA8P	24/C3	
13-M	(U50-10)	1HF4		
13-N	(U64-2)	3393	24/C3	
13-P	(U63-6)	A276	24/C4	

g. Set S1-B, S1-C, and S1-D to open.

TEST 14. Horizontal Sync Logic Test (Service Sheet 24)

a. Set instrument power to off.

b. Remove U17 and U18 (IO/ROMs on Service Sheet 21).

c. Remove R233 jumper from S2.

d. Remove ribbon cable from J2.

e. Connect jumper wire from J2-30 to chassis ground.

f. Insert jumper wire in S3 and in S4.

g. Set S1-B, S1-C, and S1-D to closed.

h. Signature Analyzer connections:
START ⎍ to U52-5
STOP ⎍ to U54-2
CLOCK ⎍ to U41-9 (CLK)

i. Set instrument power to on.

j.

TEST POINT		SIGNATURE	SS/GRID	LOC
Probe to +5		9C86		
14-N	(U61-6)	728P	24/B4	
14-U	(U63-8)	990A	24/B6	
14-Z	(U56-10)	A99A	24/C5	
14-AA	(U62-5)	H4FH	24/B6	

k. If signatures in step j. are correct go to next test; if any signatures in step j. are incorrect perform the tests in step l.

l.

TEST POINT		SIGNATURE	SS/GRID	LOC
14-A	(U52-11)	973C	24/A2	
14-B	(U52-9)	U9FF		
14-C	(U52-8)	624A		
14-D	(U52-3)	AUP6		
14-E	(U52-5)	029C	24/A3	
14-F	(U52-6)	991H		
14-G	(U62-11)	66AC	24/B3	
14-H	(U62-8)	A546		
14-J	(U62-9)	3PF0		
14-K	(U54-3)	174P	24/A4	
14-L	(U54-6)	278F		
14-M	(U54-5)	CF0A		
14-P	(U53-4)	H396		
14-Q	(U53-3)	CF0A	24/A5	
14-R	(U53-6)	47H9		
14-S	(U61-12)	UCH3		
14-T	(U55-13)	990A	24/B6	
14-V	(U53-8)	3PF0	24/B4	
14-W	(U53-11)	U863		
14-X	(U61-8)	F6A3		
14-Y	(U56-7)	0000	24/C5	

m. Set instrument power to off.

n. Remove jumper wire from J2-30.

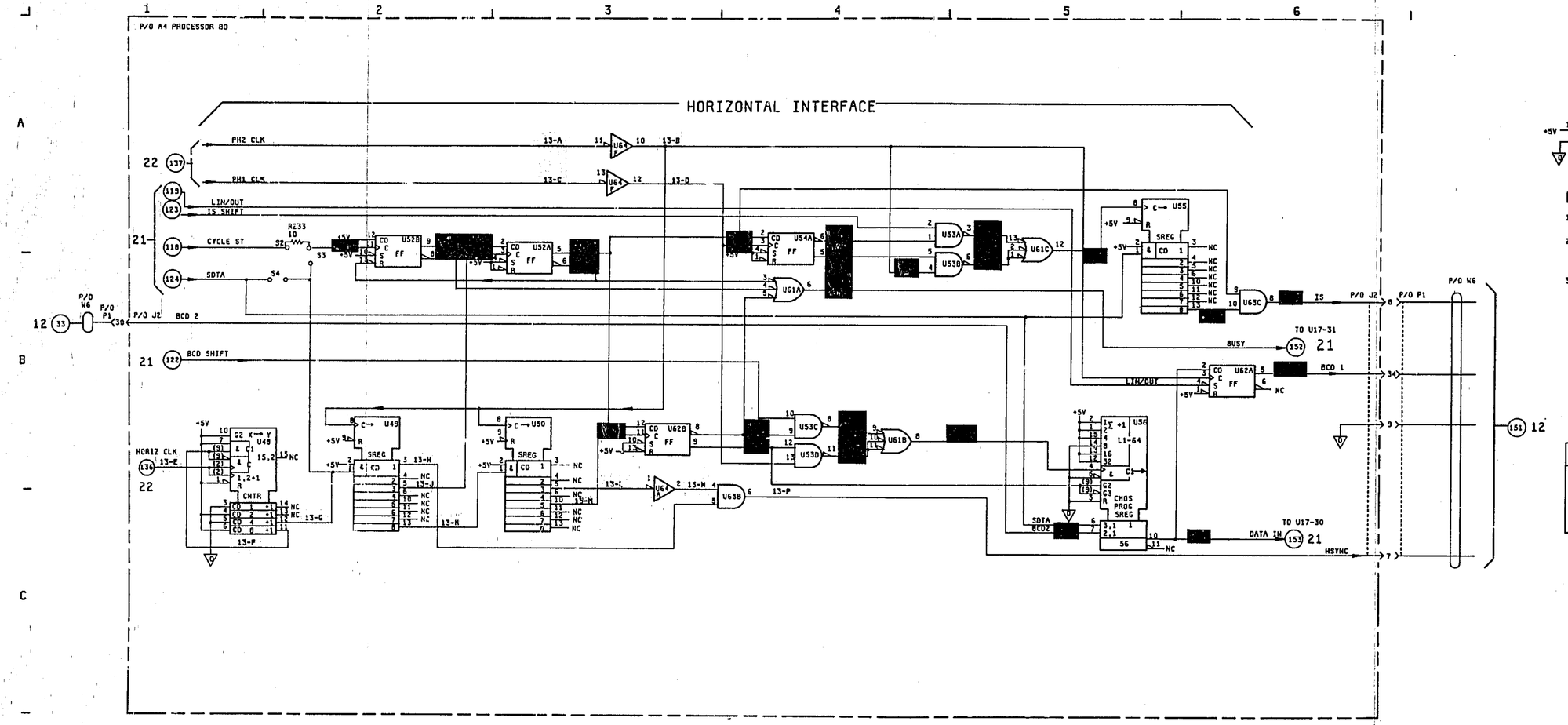
o. Reconnect ribbon cable to J2.

p. Reinsert R233 into S2.

q. Remove jumper wires from S3 and S4.

r. Reinsert U17 and U18.

s. Set S1-B, S1-C, and S1-D to open.



IC DEVICE POWER CONNECTIONS

+5V (14) U49,50,52,53, 54,55,61,62,63, 64 (7) GND

+5V (16) U48,56 (8) GND

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENARIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

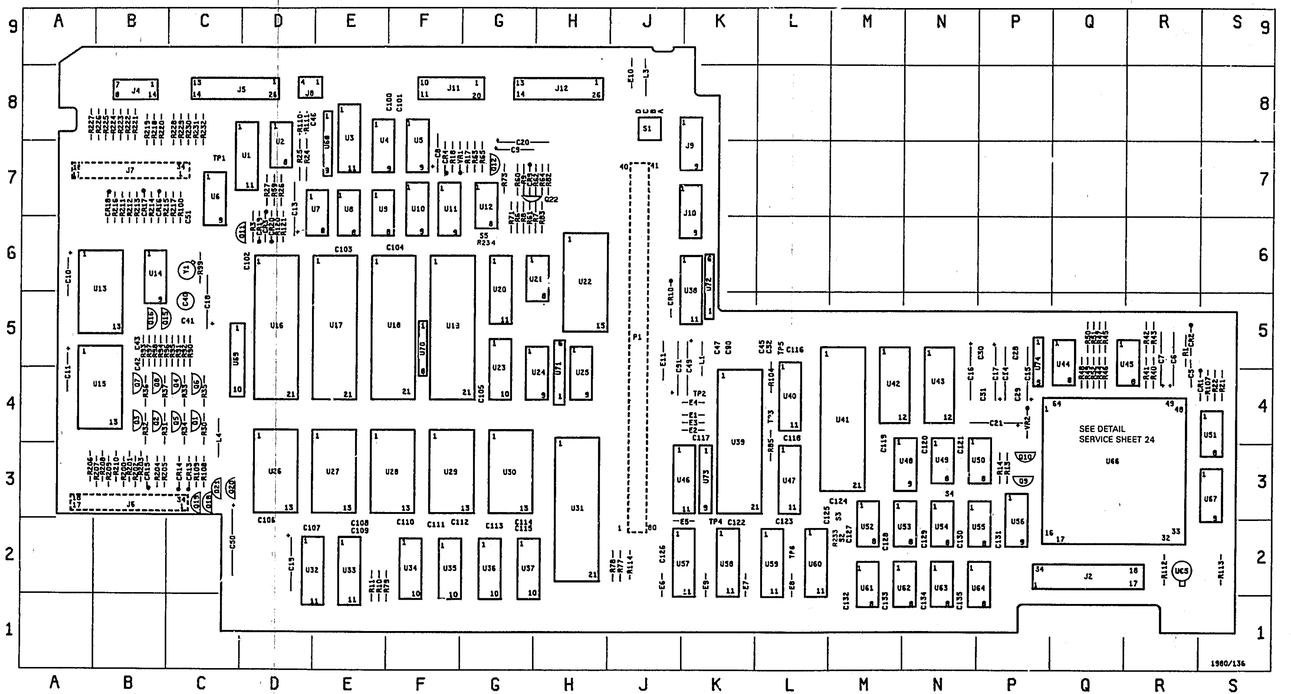
PARTS ON THIS SCHEMATIC

P/O A4	CHASSIS
P/O J2 R233 S2-4 U48=50,52,53,54A,55,56 61,62,63B,63C,64A,64E, 64F	P/O W6

1980/121/10/7/81

A4 PROCESSOR BOARD, COMPONENT LOCATIONS

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C5	R-4	C114	G-2	J2	Q-2	R24	D-7	R97	B-5	R231	C-8	U32	D-2
C6	R-5	C115	G-2	J4	D-8	R25	D-7	R98	B-5	R232	C-8	U33	E-2
C7	R-5	C116	L-5	J5	C-8	R26	D-7	R99	C-6	R233	M-2	U34	F-2
C8	F-7	C117	K-4	J6	B-3	R27	D-7	R100	C-7	R234	G-6	U35	F-2
C9	G-7	C118	L-4	J7	B-7	R30	C-4	R104	L-4	S1	J-8	U36	G-2
C10	A-6	C119	M-3	J8	D-8	R31	B-4	R107	S-4	S2	M-2	U37	G-2
C11	A-4	C120	N-3	J9	K-7	R32	B-4	R108	C-3	S3	M-2	U38	K-6
C12	D-7	C121	N-3	J10	K-7	R33	C-4	R109	C-3	S4	N-3	U39	K-4
C14	P-4	C122	K-2	J11	F-8	R34	C-4	R110	D-8	S5	G-6	U40	L-4
C15	P-4	C123	L-2	J12	H-8	R35	C-4	R111	D-8	TP1	C-7	U41	M-4
C16	N-4	C124	M-3	L1	K-5	R36	C-4	R112	P-2	TP2	K-4	U42	M-4
C17	P-4	C125	L-3	L3	J-8	R37	B-4	R113	S-2	TP3	L-4	U43	N-4
C18	C-5	C126	J-2	L4	C-4	R40	R-4	R114	J-2	TP4	K-2	U44	Q-5
C19	D-2	C127	M-2	P1	J-5	R41	R-4	R120	D-6	TP5	L-5	U45	R-5
C20	G-7	C128	M-2	Q1	C-4	R42	R-5	R121	D-6	TP6	L-2	U46	K-3
C21	P-4	C129	N-2	Q2	B-4	R43	R-5	R200	B-3	U1	D-7	U47	L-3
C28	P-5	C130	N-2	Q3	B-4	R44	Q-4	R201	B-3	U2	D-7	U48	N-3
C29	P-4	C131	P-2	Q4	C-4	R45	Q-5	R202	B-3	U3	E-7	U49	N-3
C30	P-5	C132	M-1	Q5	C-4	R46	Q-4	R203	B-3	U4	E-7	U50	N-3
C31	P-4	C133	M-1	Q6	C-4	R47	Q-5	R204	B-3	U5	F-7	U51	S-4
C32	L-5	C134	N-1	Q7	B-4	R48	Q-4	R205	B-3	U6	C-7	U52	M-2
C40	C-5	C135	N-1	Q8	B-4	R49	Q-4	R206	A-3	U7	E-7	U53	J-2
C41	C-5	CR1	E-4	Q9	P-3	R50	Q-5	R207	B-3	U8	E-7	U54	N-3
C42	B-5	CR2	R-5	Q10	P-3	R51	Q-5	R208	B-3	U9	E-7	U55	P-2
C43	B-5	CR3	D-6	Q11	D-6	R52	Q-4	R209	B-3	U10	F-7	U56	P-6
C45	L-5	CR4	F-7	Q12	G-7	R59	D-7	R210	B-3	U11	F-7	U57	K-2
C46	D-8	CR9	G-7	Q15	B-5	R60	G-7	R211	B-7	U12	G-7	U58	K-1
C47	K-5	CR10	J-5	Q16	B-5	R61	J-5	R212	B-7	U13	B-5	U59	L-2
C48	K-4	CR13	C-3	Q18	C-3	R62	H-7	R213	B-7	U14	B-6	U60	L-2
C50	C-2	CR14	C-3	Q19	C-3	R63	G-7	R214	B-7	U15	B-4	U61	M-2
C51	C-5	CR15	B-3	Q20	C-3	R64	H-7	R215	B-7	U16	D-5	U62	N-2
C52	K-5	CR16	B-7	Q21	C-3	R65	G-7	R216	B-7	U17	E-5	U63	N-2
C61	J-4	CR17	B-7	Q22	G-7	R71	G-6	R217	C-7	U18	F-5	U64	P-2
C100	F-8	CR18	B-7	R1	R-5	R73	G-7	R218	B-8	U19	F-5	U65	R-2
C101	F-8	CR19	D-8	R3	D-6	R77	J-2	R219	B-8	U20	G-5	U66	Q-3
C102	D-8	CR20	D-6	R6	G-5	R78	J-2	R220	B-8	U21	H-5	U67	S-3
C103	E-5	E1	K-4	R7	H-5	R70	E-2	R221	B-8	U22	H-5	U68	E-7
C104	F-5	E2	K-4	R8	G-5	R82	H-7	R222	B-8	U23	G-4	U69	C-5
C105	G-4	E3	K-4	R9	G-7	R83	H-6	R223	B-8	U24	H-4	U70	F-5
C106	D-2	E4	K-4	R10	E-2	R85	L-5	R224	B-8	U25	H-4	U71	H-4
C107	E-1	E5	K-2	R11	E-2	R90	C-5	R225	B-7	U26	D-3	U72	K-5
C108	E-2	E6	J-2	R13	P-3	R91	C-5	R226	B-8	U27	E-3	U73	K-3
C109	E-2	E7	K-2	R14	P-3	R92	C-5	R227	A-8	U28	F-3	U74	P-5
C110	F-2	E8	L-2	R17	G-7	R93	B-5	R228	C-8	U29	F-3	VR1	F-7
C111	F-2	E9	K-2	R18	F-7	R94	B-5	R229	C-8	U30	G-3	VR2	P-4
C112	F-2	E10	J-8	R21	S-4	R95	C-5	R230	C-8	U31	H-3	Y1	C-6
C113	G-2	E11	J-5	R22	S-4	R96	B-5						



SERVICE SHEET 25 MNEMONICS

DLY'D NOT TRGD **Delayed Not Triggered Lamp Enable** — Signal to light "NOT TRGD" lamp denoting delayed sweep is not triggered. Not active when delayed is in auto.

HDNT **High, Delayed Not Triggered** — Signal to light "NOT TRGD" lamp denoting delayed sweep is not triggered. Not active when delayed is in auto.

HMNT **High, Main Not Triggered** — Derived from horizontal when main sweep is not triggered (both normal and auto) — used to light main "NOT TRGD" lamp.

HTDC **High, Transfer Data Command** — Signal generated by software via IO port to transfer data to parallel outputs of shift register strings.

LBFD **Low, Beam Find** — When front panel "FIND BEAM" key is pressed, line is grounded to override intensity to viewable trace while decreasing vertical and horizontal gain to bring viewable presentation on screen.

LCL2 **Lamp Clock 2** — Clock generated by software to shift SDTA through the lamp driver string to light applicable panel lamps.

LTDC **Low, Transfer Data Command** — Inverted HTDC — loads SDTA into lamp driver strings.

MAIN NOT TRGD **Main Not Triggered Lamp Enable** — Signal to light "NOT TRGD" lamp denoting main sweep is not triggered. Not active when main is in auto.

PANEL+ **Panel Positive** — Panel lamp supply voltage.

PANEL– **Panel Negative** — Panel lamp supply voltage return.

RCD **Reset Cathode Driver** — Derivative of processor clock via DRC used to reset the shift registers to synchronize the LED displays.

SA-SG **Segments A-G** — Outputs from DAC to LED displays to light selected segments of each LED.

SCAN **Digit Strobe** — Output of DAC to LED digit shift register to enable selected LED digits.

SDP **Segment, Decimal Point** — Output of DAC to LED displays to light selected decimal point.

SDTA **Serial Data** — Data string from IO to various shift registers that when clocked into the shift register strings initiates various functions, lamps, etc.

SEG A-SEG G **Segment A-G** — Enable voltages for LED displays.

SEG DP **Segment Decimal Point** — Enable voltage for LED decimal display.

VBATT **Battery Voltage** — Voltage that sustains NVRAM when instrument has been powered down.

Service Sheet 25. Component Locator
P/O Processor Board, Front Panel Interface and Power Distribution



Power OFF ≅ 2.4 VDC (Battery Dependent)
Power ON ≅ 5.2 VDC

NOTE

Under normal conditions the battery (A12BT1) will last approximately three years. However, if battery leads are shorted together for any period of time the battery life will drastically be reduced. The battery should be replaced when voltage at VBATT (Test point A, instrument power off) drops below 2 VDC.



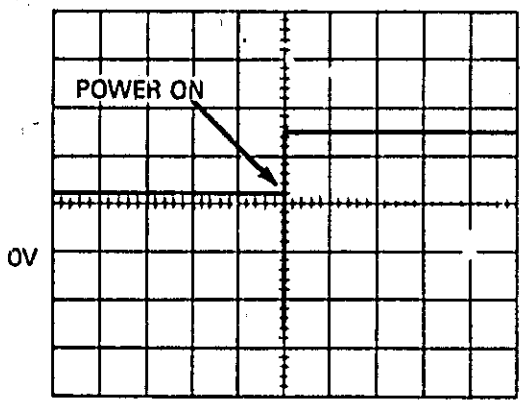
Power OFF ≅ 2.4 VDC (Battery Dependent)
Power on ≅ 5.0 VDC

Ⓒ

POWER ON

Monitor Oscilloscope Setup

2 Volts/Div
0.5 Sec/Div

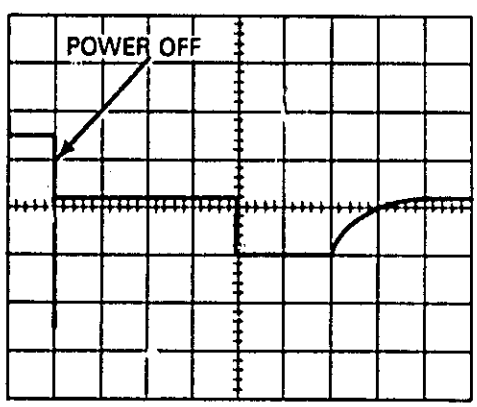


Ⓒ

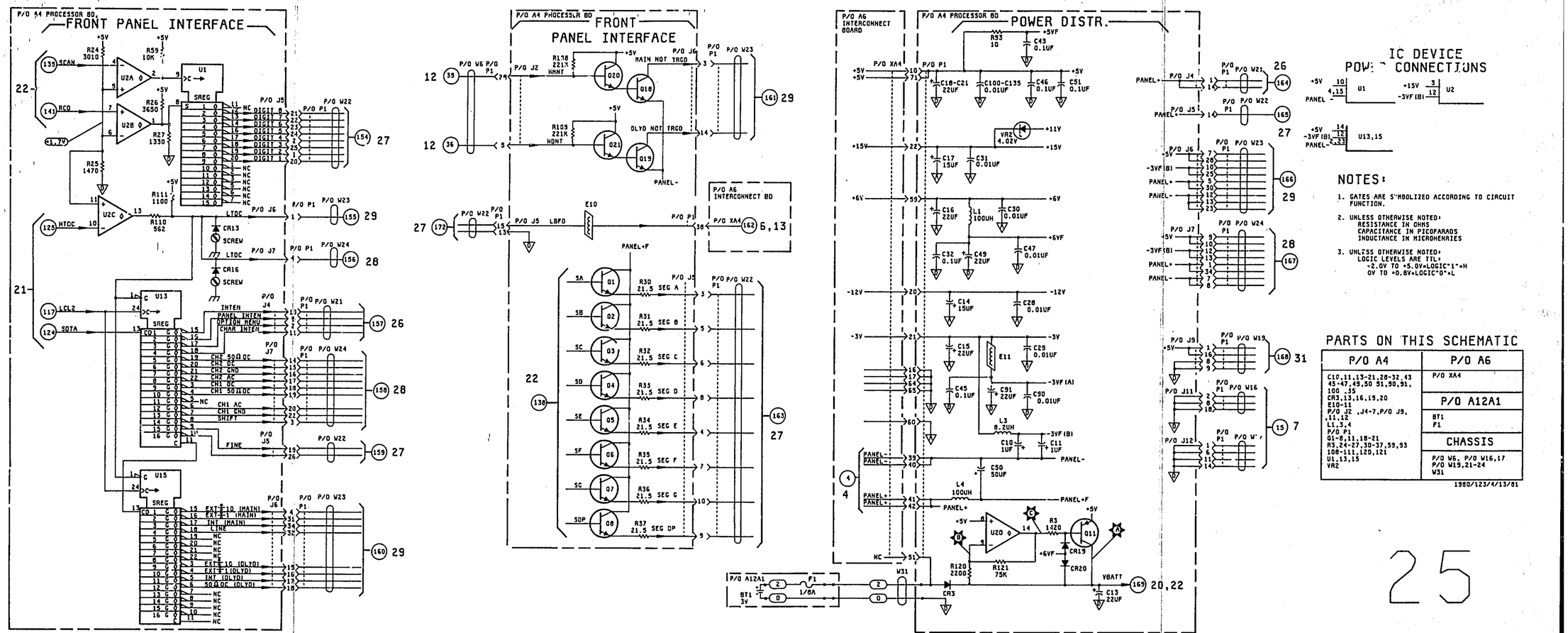
POWER OFF

Monitor Oscilloscope Setup

2 Volts/Div
0.5 Sec/Div



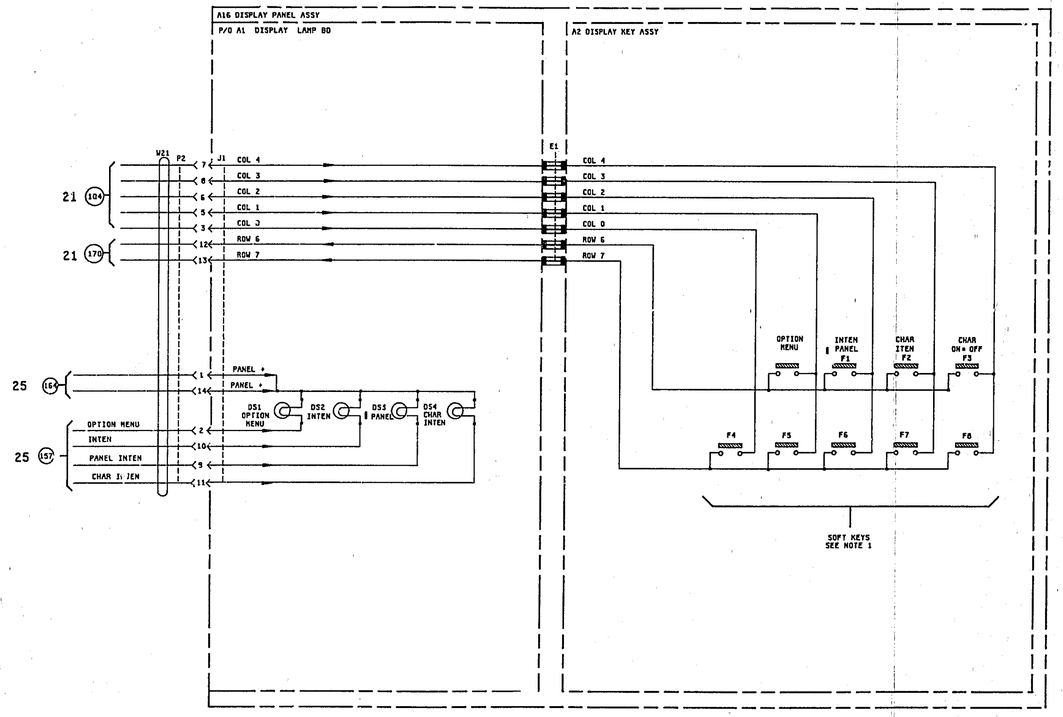
Service Sheet 25. Test Information
P/O Processor Board, Front Panel Interface and Power Distribution



Service Sheet 25. Schematic Diagram
P/O Processor Board, Front Panel Interface and Power Distribution
8-189/(8-190 blank)

SERVICE SHEET 26 MNEMONICS

COL 0-COL 4	Column 0 through 4 inputs from processor board
PANEL +	Panel Positive Lamp Voltage
ROW 6-ROW 7	Row 6 and 7 outputs to processe board



NOTES:

1. F1-F8 ARE SOFT KEYS. THE FUNCTION OF THESE SOFT KEYS IS DEFINED IN THE OPERATION PORTION OF THIS MANUAL.

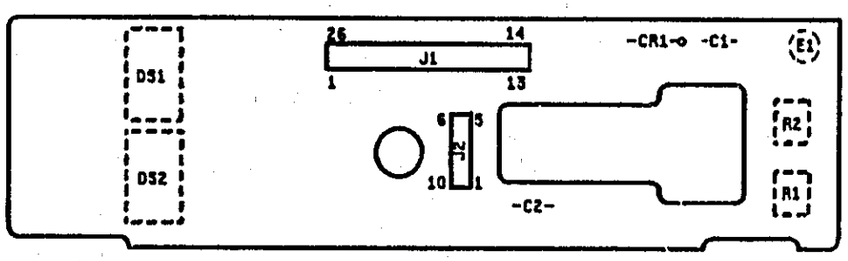
PARTS ON THIS SCHEMATIC

A16	A16A1	CHASSIS
A16A1 A16A2 E1	DS1-4 J1	W21

1980/128/5/30/80

26

Service Sheet 26. Schematic Diagram
Display Panel Assembly



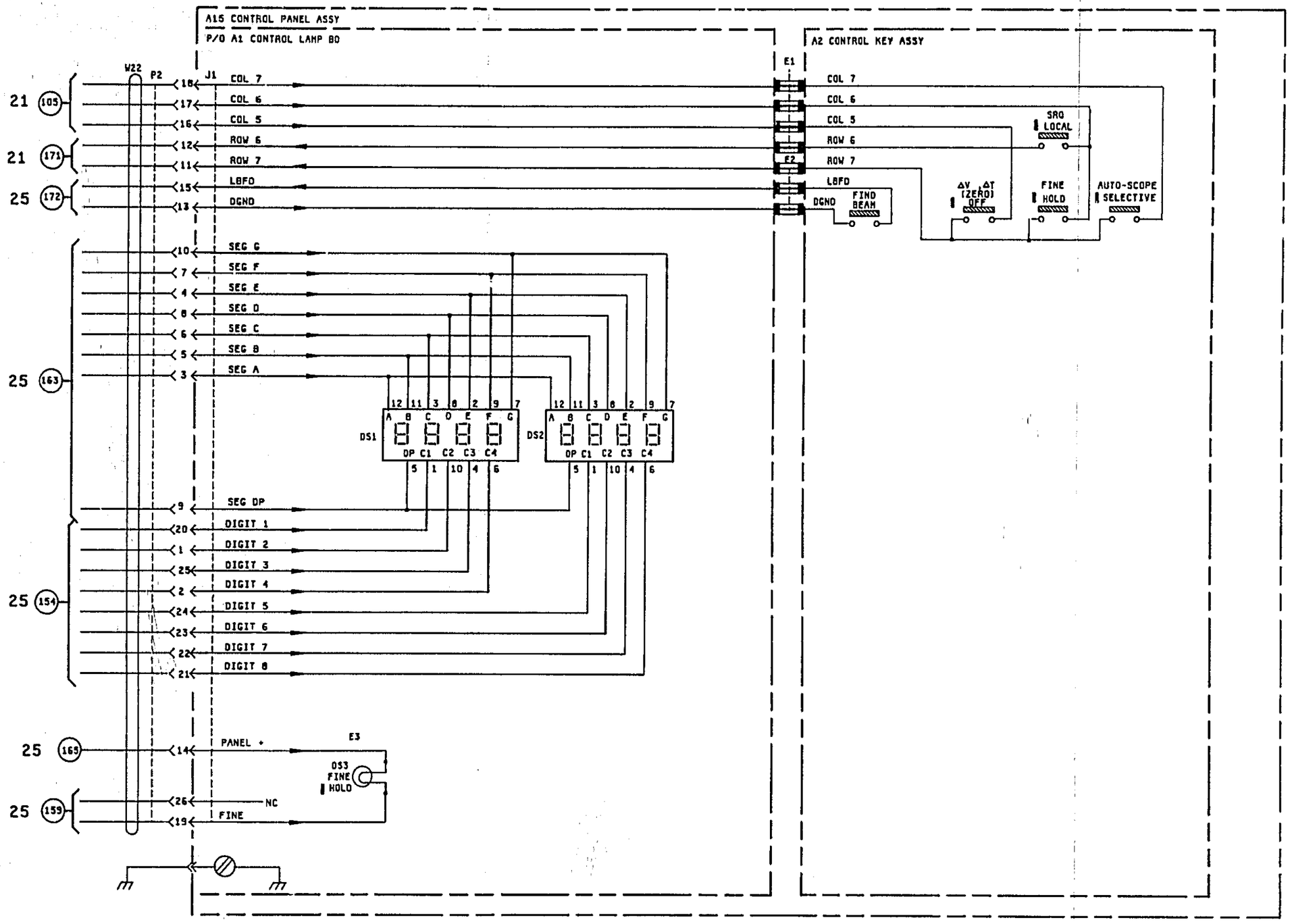
1980/150

A15A1

SERVICE SHEET 27 MNEMONICS

COL 5-COL 7	**Column 5-7** — Outputs from IO to keyboard to check for key closure.
PANEL+	**Panel Positive** — Panel lamp supply voltage.
ROW6-ROW7	Row inputs from keyboard to IO ports.
SEG A-SEG G	**Segment A-G** — Enable voltages for LED displays.
SEG DP	**Segment Decimal Point** — Enalble voltage for LED decimal display.

Service Sheet 27. Component Locator
Control Panel Assembly



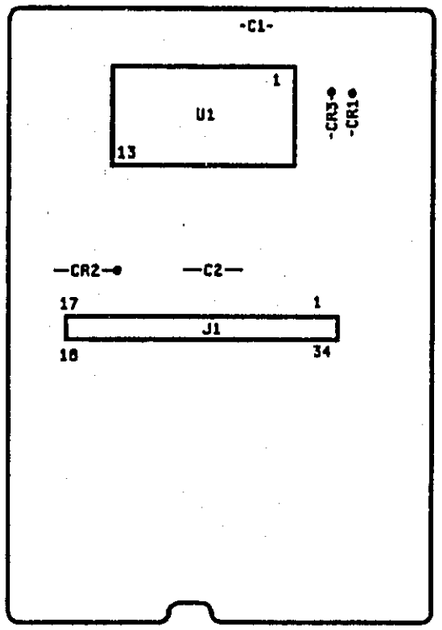
PARTS ON THIS SCHEMATIC

P/O A15	P/OA15A1	CHASSIS
A1 A2 E1,2	DS1-3 J1	W22

1980/127/10/30/01

27

Service Sheet 27. Schematic Diagram
Control Panel Assembly



1900/148

A17A1

SERVICE SHEET 28 MNEMONICS

COL 5-COL 7 — **Column 5-7** — Outputs from IO to keyboard to check for key closure.

LCL3 — **Lamp Clock 3** — Clock generated by software to shift SDTA through the lamp driver string to light applicable panel lamps.

LTDC — **Low, Transfer Data Command** — Inverted HTDC — loads SDTA into lamp driver strings.

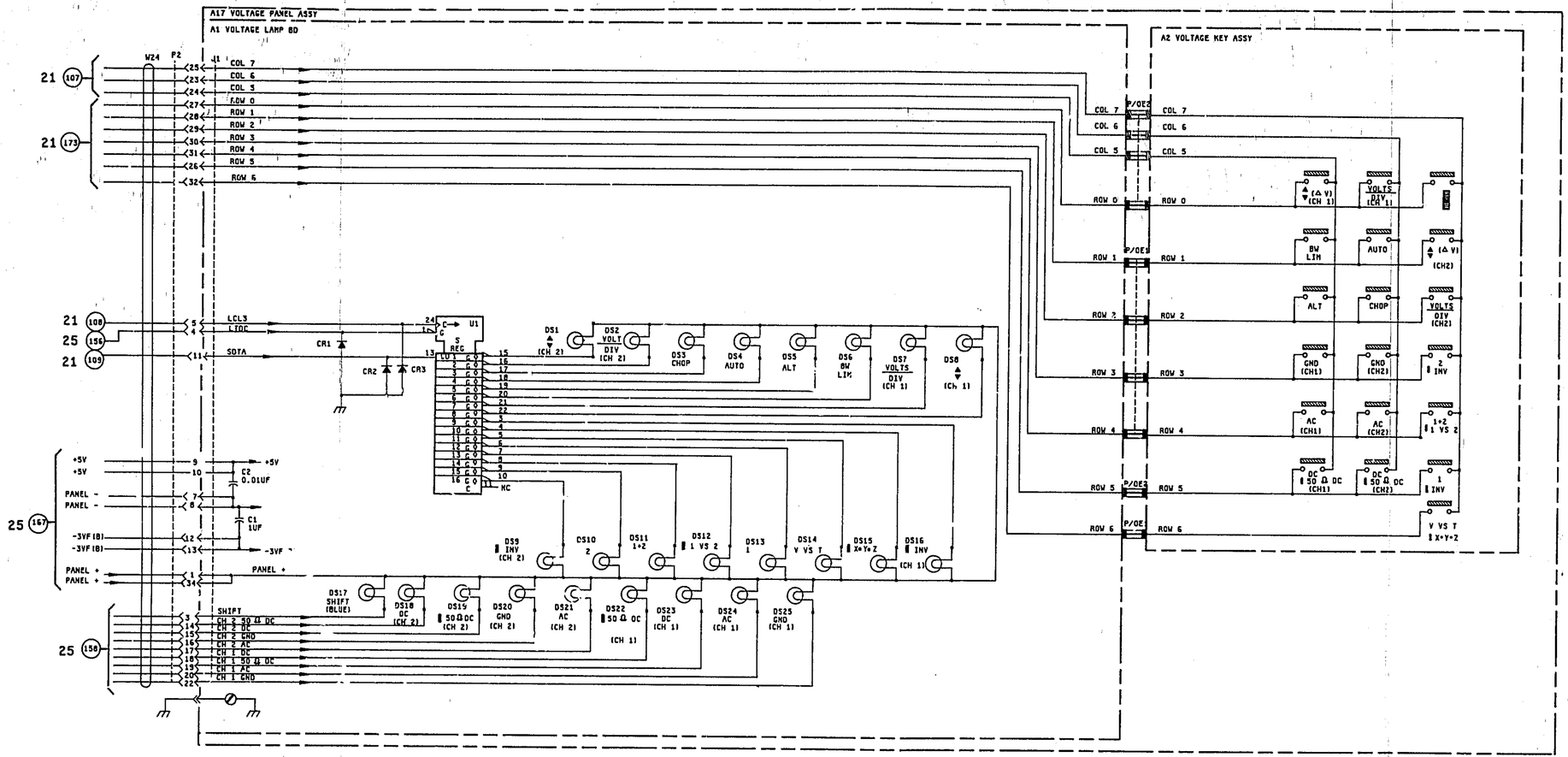
PANEL+ — **Panel Positive** — Panel lamp supply voltage.

PANEL– — **Panel Negative** — Panel lamp supply voltage return.

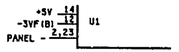
ROW0-ROW6 — **Row inputs from front panel to IO ports** — when a key is pressed a signal from a column output will be present on a row input.

SDTA — **Serial Data** — Data string from IO to various shift registers that when clocked into the shift register strings initiates various functions, lamps, etc.

Service Sheet 28. Component Locator
Voltage Panel Assembly



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

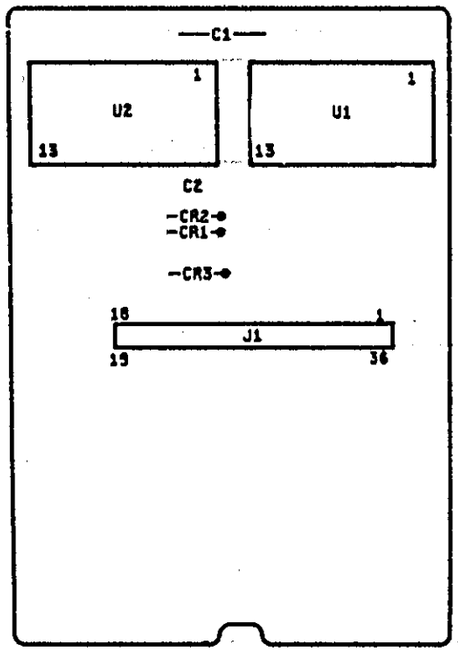
PARTS ON THIS SCHEMATIC

A17	A17A1	CHASSIS
A1 A2 E1,2	C1,2 CR1,2,3 DS1-25 J1 U1	W24

1980/126 5/30/80

28

Service Sheet 28. Schematic Diagram
Voltage Panel Assembly



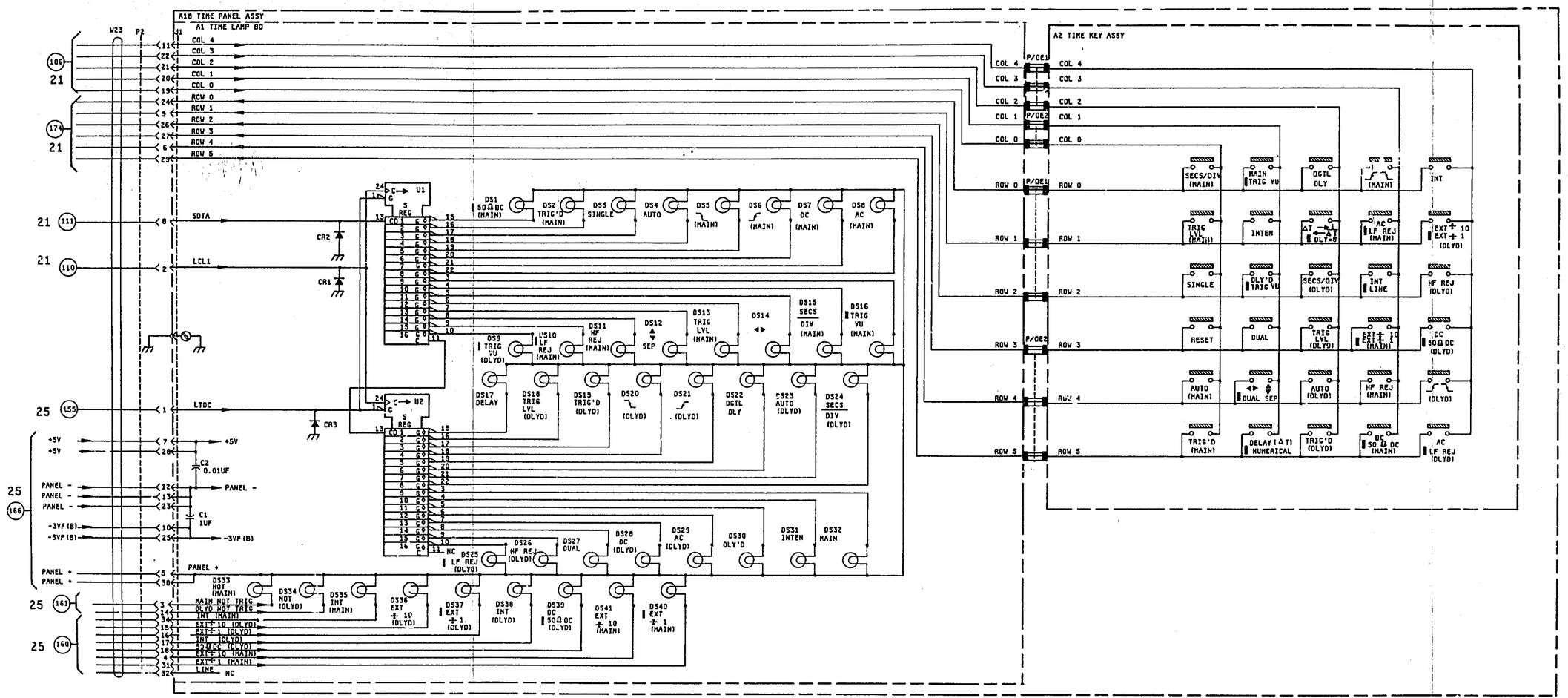
1980/149

A18A1

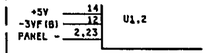
SERVICE SHEET 29 MNEMONICS

COL0-COL4	**Column 0-4** — Outputs from IO to keyboard — along with ROW inputs determine if a key has been closed, and which key has been closed.
LCL1	**Lamp Clock 1** — Clock generated by software to shift SDTA into the lamp driver string to light applicable panel lamps.
LTDC	**Low, Transfer Data Command** — Inverted HTDC — loads SDTA into lamp driver strings.
PANEL+	**Panel Positive** — Panel lamp supply voltage.
PANEL-	**Panel Negative** — Panel lamp supply voltage return.
ROW0-ROW5	Row inputs from front panel to IO ports —when a key is pressed a signal from a column output will be present on a row input.
SDTA	**Serial Data** — Data string from IO to various shift registers that when clocked into the shift register strings initiates various functions, lamps, etc.

Service Sheet 29. Component Locator
Time Panel Assembly



IC DEVICE POWER CONNECTIONS



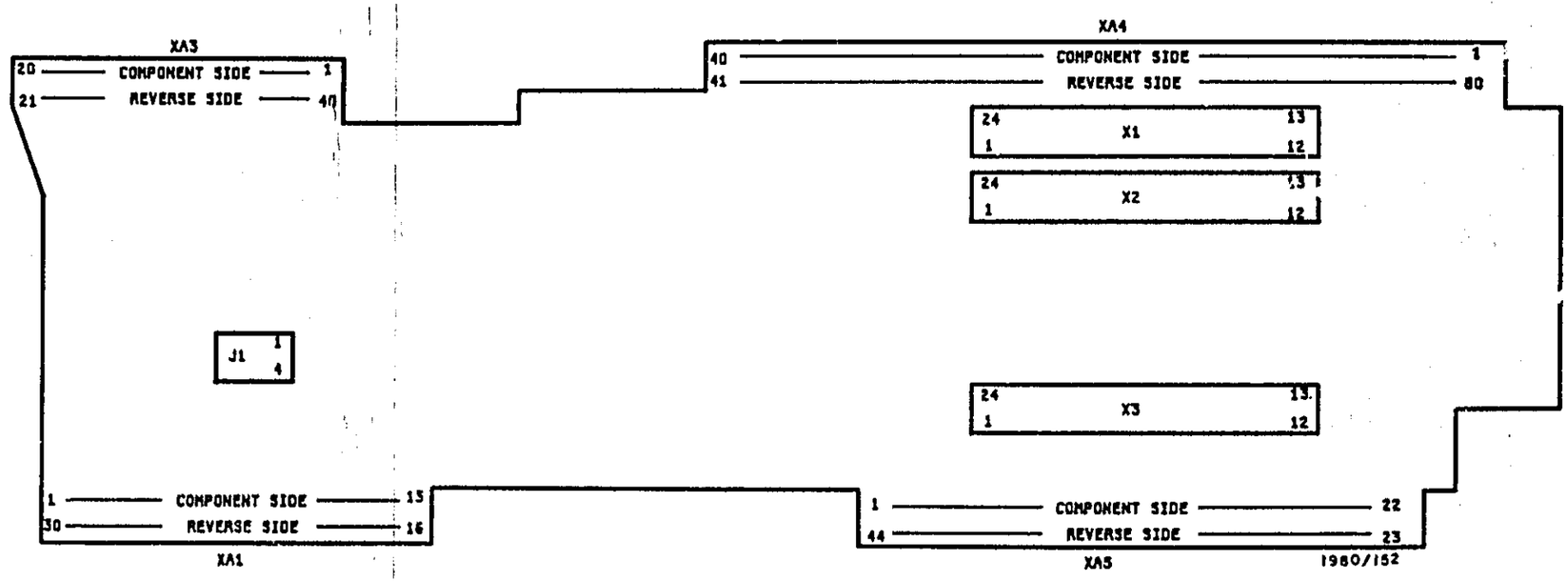
NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +4.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

A18	A18A1	CHASSIS
A1 A2 E1,2	C1,2 CR1-3 U31-41 J1 U1,2	W23

1980/124/5/31/80



A6

Service Sheet 30. Component Locator Interconnect Board

A6 INTERCONNECT BOARD

The following is a listing for the A6 interconnect board of the signal mnemonics, connector pin(s) where the signals appear, and the service sheets where the signals are shown. The last column in the list gives the interconnect number (bubble on service sheet) and the service sheet number where the signal originates.

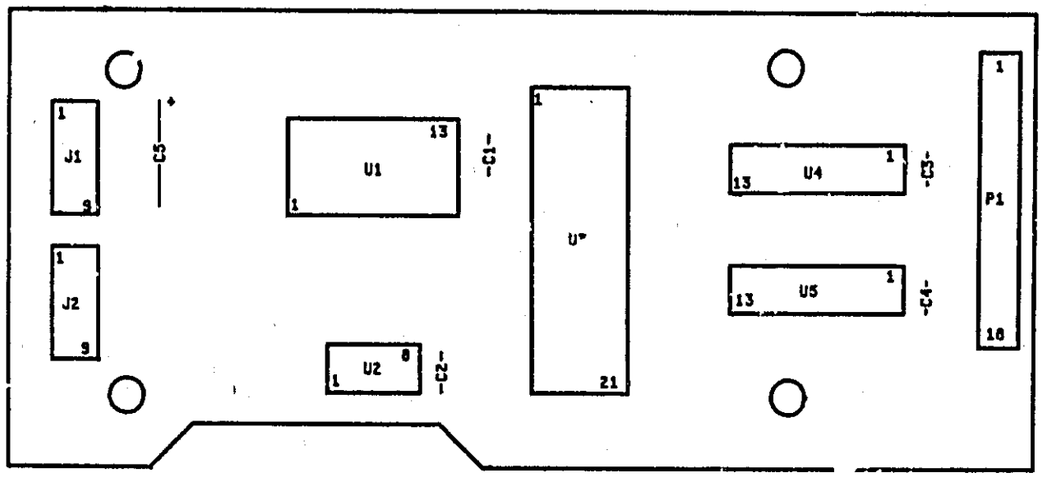
The abbreviations used on this service sheet:

LVPS —	Low Voltage Power Supply Board (A1)
GATE —	Gate Board (A3)
PROC —	Processor Board (A4)
SCOPE —	Scope Board (A5)
PI —	Plug in (not in standard instrument)
IN —	Interconnect number

SIGNAL MNEMONIC	LVPS XA1	GATE XA3	PROC XA4	SCOPE XA5	PLUG-IN X1	PLUG-IN X2	PLUG-IN X3	J1	IN/ORIGIN
A0			36/(18)		2/(—)				67/(18)
A1			37/(18)		3/(—)				67/(18)
A2			43/(18)		4/(—)				67/(18)
A3			44/(18)		5/(—)				67/(18)
A4			45/(18)		6/(—)				67/(18)
A5			46/(18)		7/(—)				67/(18)
A6			47/(18)		8/(—)				67/(18)
A7			48/(18)		9/(—)				67/(18)
A8			52/(18)			15/(—)			67/(18)
A9			29/(18)			16/(—)			67/(18)
A10			53/(18)			17/(—)			67/(18)
A11			28/(18)			18/(—)			67/(18)
A12			49/(18)			19/(—)			67/(18)
A13			32/(18)			20/(—)			67/(18)
A14			31/(18)			21/(—)			67/(18)
A15			50/(18)			22/(—)			67/(18)
AD0			35/(18)		18/(—)				67/(18)
AD1			34/(18)		19/(—)				67/(18)
AD2			33/(18)		20/(—)				67/(18)
AD3			25/(18)		17/(—)				67/(18)
AD4			26/(18)		13/(—)				67/(18)
AD5			55/(18)		14/(—)				67/(18)
AD6			27/(18)		15/(—)				67/(18)
AD7			54/(18)		16/(—)				67/(18)
AGND	20/(3)	40/(6)	60/(25)	8/(16) 37/(16)	12/(—)		10/(—) 15/(—)	3/(10)	—/(3)
ALE			66/(18)			4/(—)			64/(18)
CAL EN			72/(22)		11/(—)			1/(22)	177/(22)
CH1 VERT TAG			24/(21)	43/(8)					17/(8)
CH2 VERT TAG			23/(21)	2/(8)					17/(8)
CLK			14/(18)			9/(—)			64/(18)
CSG		28/(6)	11/(21)						113/(21)
DGND	21/(3)	39/(6)	16/(25) 17/(25) 64/(25) 65/(25)	7/(16) 38/(16)	10/(—)	2/(—)	9/(—) 16/(—)		—/(3)
DLY'D TRIG TAG			57/(21)	19/(14)					53/(14)
FP INT	15/(4)	25/(6)							6/(6)
FG+	13/(4)	11/(6)							3/(4)
FG–	14/(4)	12/(6)							3/(4)
GET		13/(7)	1/(31)	30/(11)	21/(—)				180/(31)
HBG(PI)		7/(6)					14/(—)		183/(PI)
HCHEN	8/(13)	21/(6)	7/(23)						147/(23)
HCHRH	10/(13)	6/(23)							146/(23)
HCHRV	3/(10)		74/(23)						145/(23)
HCH3				1/(11)			2/(—)		26/(11)
HCH4				44/(11)			23/(—)		26/(11)
HCRS			19/(21)	33/(11)					112/(21)
HDCLKP				25/(15)			12/(—)		62/(15)
HDRQ0			15/(23)			11/(—)			178/(PI)
HDSG(1)				13/(12)			13/(—)		38/(12)
HDTE	5/(10)		8/(18)	24/(12)					35/(12)
HEXEN	7/(13)	24/(6)	78/(18)						7/(6)
HMCLKP				16/(15)			2/(—)		59/(15)
HMSG(1)				32/(12)			8/(—)		34/(12)
HORIZ POS	11/(13)		2/(22)						134/(22)

SIGNAL MNEMONIC	LVPS XA1	GATE XA3	PROC XA4	SCOPE XA5	PLUG-IN X1	PLUG-IN X2	PLUG-IN X3	J1	IN/ORIGIN
HTC			58/(23)			10/(—)			143/(23)
HTDC		26/(6)	70/(21)						113/(21)
HDIM4		1/(6)		22/(12)					40/(12)
HDIM2		2/(6)		21/(12)					40/(12)
HDIM1		3/(6)		23/(12)					40/(12)
INTEN		5/(6)	79/(22)						133/(22)
IO/LM			13/(18)			7/(—)			64/(18)
LBFD	6/(13)	6/(6)	38/(25)						162/(25)
LCHZ		22/(6)	73/(23)						148/(23)
LDACK0			62/(23)			12/(—)			142/(23)
LDSE		4/(6)		12/(11)					31/(11)
LINE FREQ	1/(2)		61/(22)						1/(2)
LINTRQ(PI)			80/(18)			1/(—)			175/(PI)
LIOR			3/(19)			24/(—)			87/(19)
LIOW			77/(19)			3/(—)			87/(19)
LMEMR			5/(19)			14/(—)			87/(19)
LMEMW			75/(19)			13/(—)			87/(19)
LPIRDY			30/(18)			23/(—)			176/(PI)
LRD			68/(18)			6/(—)			64/(18)
LWR			12/(18)			5/(—)			64/(18)
MAIN TRIG TAG			56/(21)	20/(14)					53/(14)
PANEL+	17/(4)		41/(25) 42/(25)				21/(—)		—/(4)
PANEL–	16/(4)		39/(25) 40/(25)				22/(—)		—/(4)
PWRDET			76/(18)		1/(—)				69/(18)
RESET			67/(18)			8/(—)			64/(18)
SDTA		27/(6)	9/(21)						113/(21)
SWP CAL	4/(10)	9/(6)							8/(6)
Y AXIS	2/(10)							4/(10)	—/(10)
Z BLANKING		26/(6)						2/(6)	—/(6)
+100V	22/(2)	38/(6)					18/(—)		—/(2)
+43V	23/(2)	37/(6)		3/(16) 42/(16)			3/(—)		—/(2)
+15V	24/(2)	36/(6)	22/(25)	4/(16) 41/(16)			4/(—)		—/(2)
+15V UNREG	19/(2)	16/(5)							—/(2)
+15V RETURN	18/(2)	18/(5)							—/(2)
+6V	25/(3)	35/(6)	59/(25)	5/(16) 40/(16)	23/(—)		20/(—)		—/(3)
+5V	26/(3)	34/(6)	10/(25) 71/(25)	5/(16) 39/(16)	22/(—)		5/(—)		—/(3)
–3V	27/(3)	33/(6)	21/(25)	9/(16) 36/(16)	24/(—)		19/(—)		—/(3)
–5V	28/(3)	32/(6)		10/(16) 35/(16)			6/(—)		—/(3)
–12V	29/(4)	31/(6)	20/(25)	11/(16) 34/(16)			7/(—)		—/(4)
–24V	30/(4)	30/(6)		26/(16)			17/(—)		—/(4)

30



1980/145

A23

SERVICE SHEET 31 MNEMONICS

A0-A11	**Address Lines 0-11** — A0-A7 are developed from the AD0-AD7 bus. A8 through A11 are most significant bits.
AD0-AD7	**Address/Data Bus** — Microprocessor bidirectional Bus. Data on this bus can be the least significant 8 bits of address.
ATN	**Attention** — HP-IB command. Refer to HP-IB operation and programming.
CLK	**Clock** — From microprocessor - 3.333333 MHz processor clock input divided by two.
DAV	**Data Available** — HP-IB signal. Refer to HP-IB operation and programming.
DIO1-DIO8	**Data Input/Output** — HP-IB data IO lines. Refer to HP-IB operation and programming.
EIO	**End Or Identify** — HP-IB signal. Refer to HP-IB operation and programming.
GET	**Group Execute Trigger** — HP-IB Signal. Allows bus simulation of a FIND BEAM key closure. Refer to HP-IB operation and programming.
IBIO	**Interface Bus IO** — Chip select decoded from address to select HP-IB IO, A23U3.
IBROM	**Interface Bus ROM** — Chip select decoded from address to select HP-IB ROM, A23U1.
IFC	**Interface Clear** — HP-IB command. Refer to HP-IB operation and programming.
LINTRQ	**Low, Interrupt Request** — From HP-IB, wire-ored with LINTRQ(PI) and inverted to become RST5.5 to the processor. When low the processor is placed into an interrupt service routine.
LIOR	**Low, IO Read** — tells the selected IO device to output a byte of data on the AD0-AD7 lines. Usually controlled by the DMA Controller.
LIOW	**Low, IO Write** — indicates to the selected IO device that a data byte is available on the AD0-AD7 lines. The IO device will then latch the data. Usually controlled by the DMA Controller.
NDAC	**Not Data Accepted** — HP-IB Signal. Refer to HP-IB operation and programming.
NRFD	**Not Ready For Data** — HP-IB signal. Refer to HP-IB operation and programming.
REN	**Remote Enable** — HP-IB signal. Refer to HP-IB operation and programming.
SRQ	**Service Request** — HP-IB signal. Refer to HP-IB operation and programming.
T/R1-T/R2	**Transmit/Receive 1-2** — Produced by the HP-IB Interface Control (A23U3) to control the direction of data through the bus receiver/transmitter ICs (A23U4 and A23U5).

Service Sheet 31. Component Locator
HP-IB Interface

SERVICE SHEET 31 SIGNATURE ANALYSIS

Note

Remove Expansion Module before performing tests.

TEST 16. HP-IB ROM Test

Note

This test checks the ability of the processor to access the HP-IB COM. Ensure an external controller is not connected to the 1980 when this test is being performed.

a. Set instrument power to off.

b. Signature Analyzer Connections:

START ⅂ to A23U1-20 (IBROM)
STOP ⎍ to A4U3-7 (BROM)
CLOCK ⎍ to A4TP5 (LRD)

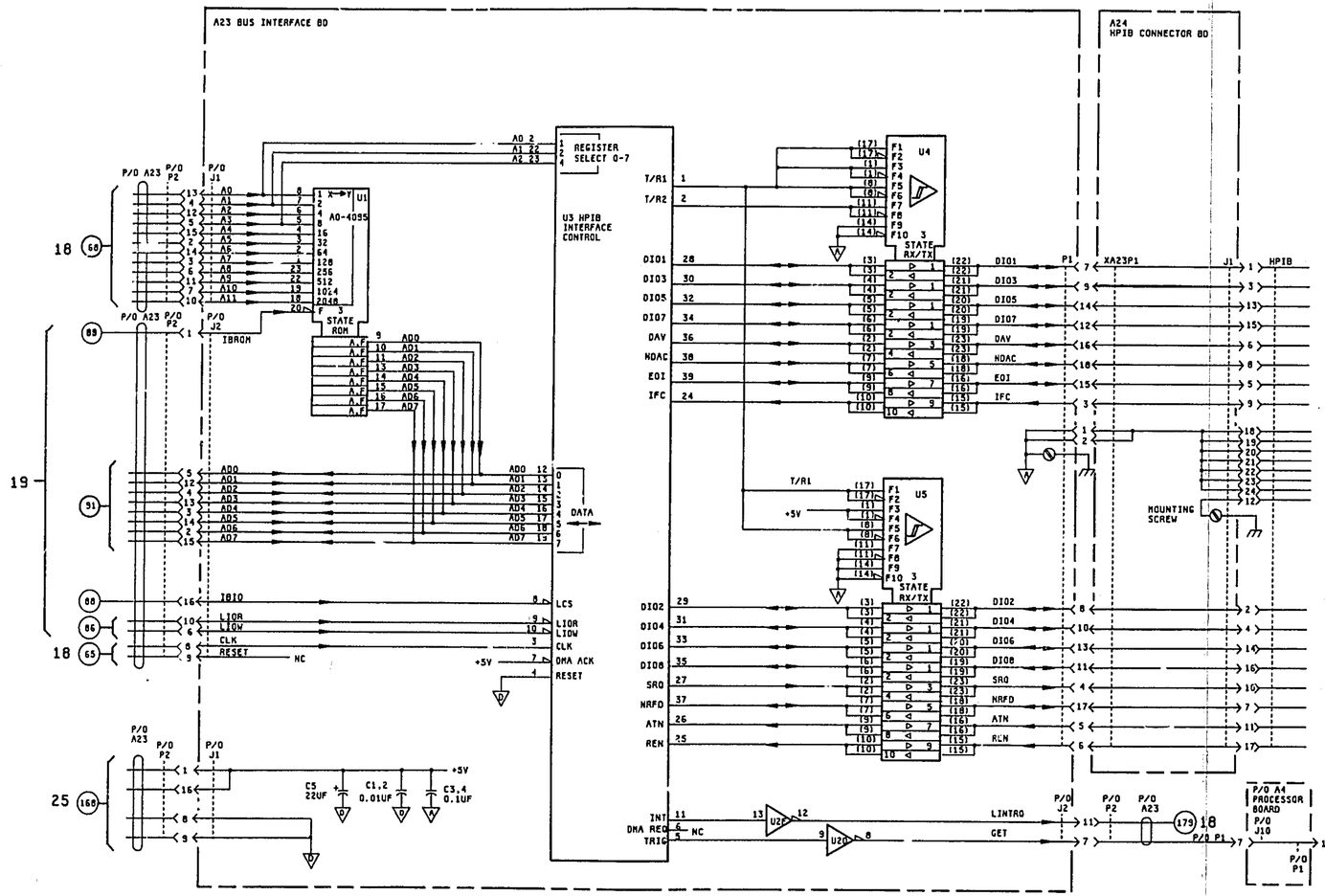
c. Set A4S1-B and A4S1-C to closed.

d. Set instrument power to on.

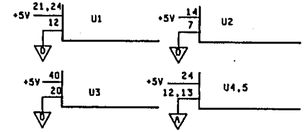
e.

TEST POINT	SIGNATURE
Probe to +5 V	826P
A0 (U1-8)	7P25
A1 (U1-7)	2A1F
A2 (U1-6)	A206
A3 (U1-5)	C133
A4 (U1-4)	8P3U
A5 (U1-3)	3319
A6 (U1-2)	7C47
A7 (U1-1)	C25F
A8 (U1-23)	5H21
A9 (U1-22)	19H6
A10 (U1-19)	HP66
A11 (U1-18)	7A70
AD0 (A4U57-18)	8U80
AD1 (A4U57-17)	7ACA
AD2 (A4U57-16)	24C2
AD3 (A4U57-15)	CAPF
AD4 (A4U57-14)	0922
AD5 (A4U57-13)	CA40
AD6 (A4U57-12)	1C71
AD7 (A4U57-11)	H967

f. Set A4S1-B and A4S1-C to open.



IC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

A23	A24	CHASSIS
C1-5 J1-2 P1 U1-5	J1 XA23P1	W19,20
P/O A4		P/O A6
P/O J10 P/O P1		P/O XA4

1980/129/4/13/81

MANUAL CHANGES

MANUAL IDENTIFICATION

Model Number: 1980A
Date Printed: February 1982
Part Number: 01980-90907

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement:
Make all ERRATA corrections.
Make all appropriate serial number related changes indicated in the tables below.

Serial Prefix or Number	Make Manual Changes
2209A	1
2240A	1, 2
2309A	1, 2, 3
2339	1, 2, 3, 4
2403A	1, 2, 3, 4, 5,
2429A	1, 2, 3, 4, 5, 6

Serial Prefix or Number	Make Manual Changes
2507A	1, 2, 3, 4, 5, 6, 7

▲ NEW ITEM

ERRATA

Section 1. General Information.

Page 1-6. Table 1-1. Specifications,
Change: EXTERNAL TRIGGER INPUTS to read: Input RC: AC or DC, 1 M ohm ±2% shunted by approx. 11 pF. . .

Page 1-7. Table 1-1. Specifications,
Change: Operating Characteristics to read: Autoscope: seeks, scales, and displays input signals >35 mV and >50 Hz.

Page 1-8.
Add: Page 1-8a "Table 1-1a. Trigger Flag Specifications" in this change sheet.

Section 3. Operation.

Page 3-3.
Change: "Maximum Input Voltage at Frequency ≥1 KHz" as shown in Figure 6.

NOTE

Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies quote the manual identification information from your supplement, or the model number and print date from the title page of the manual.

HEWLETT PACKARD

Printed in U.S.A.

ERRATA (Cont'd)

Page 3-3. Paragraph 3-7. Operators Maintenance.
Change as follows:
Painted Surfaced and panel facias can be cleaned using a soft cloth and either a commercial glass cleaner, or a mild soap and water solution.

CAUTION

Do not use chemical cleaning agents or abrasive cleaners that might damage the plastics or facia adhesives used in this instrument. Recommended cleaning procedure is to lightly dampen a cloth with the cleaning agent and wipe surfaces clean. DO NOT spray cleaning agents on facia or use cloths heavily soaked with cleaning agents.

Page 3-38.
Change: The last two lines of paragraph 3-47 to read
"HP-IB status advisory should read: HP-IB: R"
"Controller display should read 128.00 (HP9825) or 128 (HP9835/45)."

Add: Paragraph 3-47a "Trigger Flag Operation Checks" with page 3-38a in this change sheet.

Page 3-46.
Change: Description to
frequency ..... >50Hz
amplitude ..... >35 mV to maximum input

Page 3-65.
Replace: Page 3-65 "Table 3-11. Hardware Error Codes" with replacement page 3-65 in this change sheet.

Page 3-108.
Change: "Maximum Input Voltage at Frequency ≥1 KHz" as shown in Figure 6.

Page 3-117.
Replace: Page 3-117 through 3-119 "Trigger Flag" with the replacement pages 3-117 - 3-119 in this change sheet.

Add: Page A3, "Appendix II" to the back of the Operating and Programming Manual.

Section 4. Performance Tests.

Page 4-2.
Add: Pages 4-2a through 4-2g, "Operational Verification" for the 1965, 1950, and 19860.

Page 4-24.
Add: Pages 4-24a through 4-24c, "Operational Verification Test Record" for the 1965, 1950, and 19860.

Section 5. Adjustments.

Page 5-3.
Replace: Page 5-3, "Table 5-2. Required Adjustment after repair" with the revised page in this change sheet.

Section 6. Replaceable Parts.

Page 6-14. Table 6-2. Replaceable Parts.
Change: A1 to HP Part Number and Mfr Part Number 01980-66554, CD0.
Change: A7 to HP Part Number and Mfr Part Number 01980-66553, CD9.
Change: A10 to HP Part Number and Mfr Part Number 01980-61651.
Add: C1, HP Part Number 0160-4835, CD7, Qty 3, CAPACITOR-FXD 0.1UF 50V. Mfr Code 02010, Mfr Part Number MA305C104KAA.
Add: C2, HP Part Number 0160-4835, CD7, CAPACITOR-FXD 0.1UF 50V. Mfr Code 02010, Mfr Part Number MA305C104KAA.
Add: C3, HP Part Number 0160-4835, CD7, CAPACITOR-FXD 0.1UF 50V. Mfr Code 02010, Mfr Part Number M305C104KAA.
Change: H24 to HP Part Number and Mfr Part Number 2360-0235, CD7, .688 IN-LG.

ERRATA (Cont'd)

Page 6-15. Table 6-2. Replaceable Parts.
Add: H49, HP Part Number and Mfr Part Number 2360-0111, CD0, Qty 2, SCREW-MACH 6-32 .188 IN-LG, Mfr Code 28480.
Add: H50, HP Part Number and Mfr Part Number 0520-0127, CD6, Qty 1, SCREW-MACH 2-56 .188 IN-LG, Mfr Code 28480.

Page 6-16. Table 6-2. Replaceable Parts.
Change: W10 to HP Part Number and Mfr Part Number 01980-61649, CD4.
Change: W13 to HP Part Number and Mfr Part Number 01980-61650, CD7.
Change: W30 to HP Part number and Mfr Part Number 01980-61645, CD0.

Page 6-17. Table 6-2. Replaceable Parts.
Change: A1 to HP Part Number and Mfr Part Number 01980-66554, CD0.
Change: A1C22 to HP Part Number and Mfr Part Number 0160-3799, 18PF 100V.

Page 6-20. Table 6-2. Replaceable Parts.
Change: A1R36 to HP Part Number 0699-1011, CD6, Qty 1, RESISTOR 3.32K 0.1%, Mfr Code 28480, Mfr Part Number 0699-1011.

Page 6-25. Table 6-2. Replaceable Parts.
Delete: A3C8.
▲ Change: A3C32 to HP Part Number and Mfr. Part Number to 0160-3719.
Change: A3C35 to HP Part Number and Mfr Part Number 0160-3459, CD9.
Change: A3J1 to HP Part Number and Mfr Part Number 1251-7229, CD3.
Change: A3J2 to HP Part Number and Mfr Part Number 1251-8273, CD9.

Page 6-27. Table 6-2. Replaceable Parts.
Change: A3R82 to HP Part Number and Mfr Part Number 0698-8959, CD4.

Page 6-29. Table 6-2. Replaceable Parts.
Delete: A4C6.
Change: A4C7 Qty to 1.

Page 6-30. Table 6-2. Replaceable Parts.
Change: A4E1 Qty to 11.
Add: A4E13, HP Part Number and Mfr Part Number 9170-0759, CD6, CORE-BEAD SHIELDING, Mfr Code 28480.
Change: A4J2 to HP Part Number and Mfr Part Number 1251-8276, CD1.
Change: A4J4 to HP Part Number and Mfr Part Number 1251-8274, CD0.
Change: A4J6 to HP Part Number and Mfr Part Number 1251-8277, CD3.
Change: A4J7 to HP Part Number and Mfr Part Number 1251-8277, CD3.
Change: A4J11 to HP Part Number and Mfr Part Number 1251-8273, CD9.
Change: A4J12 to HP Part Number and Mfr Part Number 1251-7229, CD3.
Delete: A4L?
Change: A4MP1 to HP Part Number and Mfr Part Number 0050-2109, CD1.

▲ Page 6-31. Table 6-2. Replaceable Parts.
Change: A4R30 through A4R37 to HP Part Number 0698-6364 and Mfr. Part Number PME55-1/8-T0-50R0-F.

Page 6-33. Table 6-2. Replaceable Parts.
Change: A4U45 to HP Part Number and Mfr Part Number 1820-1958, CD0.
Change: A4U51 to HP Part Number and Mfr Part Number 1820-1503, CD1.

Page 6-36. Table 6-2. Replaceable Parts.
Add: *A5C153, HP Part Number and Mfr Part Number 0160-4380, CD7, Qty 1, CAPACITOR-FXD 1.0PF, Mfr Code 28480.
Add: *A5C153, HP Part Number and Mfr Part Number 0160-4381, CD8, Qty 1, CAPACITOR-FXD 1.5PF, Mfr Code 28480.
Add: *A5C153, HP Part Number and Mfr Part Number 0160-3872, CD0, Qty 1, CAPACITOR-FXD 2.2PF, Mfr Code 28480.
Add: *A5C154, HP Part Number and Mfr Part Number 0160-4380, CD7, Qty 1, CAPACITOR-FXD 1.0PF, Mfr Code 28480.
Add: *A5C154, HP Part Number and Mfr Part Number 0160-4381, CD8, Qty 1, CAPACITOR-FXD 1.5PF, Mfr Code 28480.

ERRATA (Cont'd)

Add: *A5C154, HP Part Number and Mfr Part Number 0160-3872, CD0, Qty 1, CAPACITOR-FXD 2.2PF, Mfr Code 28480.
Add: "*Selected By Test" on bottom margin of page.

Page 6-37. Table 6-2. Replaceable Parts.
Change: A5E1 Qty to 12.
Add: A5E13, HP Part Number and Mfr Part Number 9170-0029, CD3, CORE-SHIELDING BEAD, Mfr Code No. 28480.
Add: A5E14, HP Part Number and Mfr Part Number 9170-0029, CD3, CORE-SHIELDING BEAD, Mfr Code No. 28480.
Change: A5H1 to HP Part Number 2200-0170, CD3, Qty 12, SCREW-MACH 4-40 .625 IN-LG CSK, Mfr Code 00000, Mfr Part Number ORDER BY DESCRIPTION.
Change: A5J2 to HP Part Number and Mfr Part Number 1251-8275, CD1.
Change: A5J3 to HP Part Number and Mfr Part Number 1251-8276, CD2.
Change: A5MP1 to HP Part Number and Mfr Part Number 0050-2109, CD1.
▲ Change: A5Q5 to HP Part Number and Mfr. Part Number 1853-0589.

Page 6-40. Table 6-2. Replaceable Parts.
Change: A5R171 to HP Part Number and Mfr Part Number 2100-0554, CD5, 500 ohms.
Change: A5R187 to HP Part Number and Mfr Part Number 2100-1788, CD9, 500 ohms.

Page 6-41. Table 6-2. Replaceable Parts.
Change: A5U9 to HP Part Number and Mfr Part Number 1NA4-8005.

Page 6-46. Table 6-2. Replaceable Parts.
Change: A13A2J1 to HP Part Number and Mfr Part Number 1251-8276, CD2.

Page 6-47. Table 6-2. Replaceable Parts.
Delete: A14MP13.

Page 6-48. Table 6-2. Replaceable Parts.
Change: A14A2L1 to HP Part Number and Mfr Part Number 0491-0103, CD5.
Change: A14A2J1 to HP Part Number and Mfr Part Number 1251-8276, CD9.

Page 6-49. Table 6-2. Replaceable Parts.
▲ Change: A15A1CR1 to HP Part Number and Mfr Part Number 1901-1164.
Change: A15A1J1 to HP Part Number and Mfr Part Number 1251-7743, CD6.
Change: A15A1R1 to HP Part Number and Mfr Part Number 2100-4043, CD5.
Change: A15A1R2 to HP Part Number and Mfr Part Number 2100-4044, CD6.

Page 6-50. Table 6-2. Replaceable Parts.
Change: A16A1J1 to HP Part Number and Mfr Part Number 1251-8139, CD6.

Page 6-51. Table 6-2. Replaceable Parts.
▲ Change: A17A2CR1 through A17A2CR3 to HP Part Number and Mfr Part Number 1901-1164.
Change: A17A2J1 to HP Part Number and Mfr Part Number 1251-8277, CD3.
Change: A18A1C2 Qty to 2.
Add: A18A1C3, HP Part Number and Mfr Part Number 0160-3470, CD4, CAPACITOR-FXD 0.01UF +80 50VDC CER, Mfr Code 28480.
▲ Change: A18A2CR1 through A18A2CR3 to HP Part Number and Mfr Part Number 1901-1164.
Change: A18A1J1 to HP Part Number and Mfr Part Number 1251-8277, CD3.

Page 6-52. Table 6-2. Replaceable Parts.
Change: A23W19 to HP Part Number and Mfr Part Number 8120-3467, CD3.
Change: A23W20 to HP Part Number and Mfr Part Number 8120-3467, CD3.

Section 8. Service.

Page 8-12. Paragraph 8-19. Cleaning.
Change as follows:
Painted Surfaces and panel facias can be leaned using a soft cloth and either a commercial glass cleaner, or a mild soap and water solution.

ERRATA (Cont'd)

CAUTION

Do not use chemical cleaning agents or abrasive cleaners that might damage the plastics or facia adhesives used in this instrument. Recommended cleaning procedure is to lightly dampen a cloth with the cleaning agent and wipe surfaces clean. DO NOT spray cleaning agents on facia or use cloths heavily soaked with cleaning agents.

Page 8-61. Service Sheet 1, Schematic Diagram.
Change: C65 value to 0.1UF.
Change: C66 value to 0.1UF.

Page 8-69. Service Sheet 3. Schematic Diagram.
Add: C1 from T1 pin 7 to T1 pin 8. Value is 0.1UF.
Add: C2 from T1 pin 17 to T1 pin 18. Value is 0.1UF.

Page 8-73. Service Sheet 4. Schematic Diagram.
Add: C3 from T1 pin 15 to T1 pin 16. Value is 0.1UF.

Page 8-78.
Delete: Component Locator (A3 Board Component Locator is located on page 8-84).

Page 8-101. Service Sheet 9. Schematic Diagram.
Change: A5C152 value to 2.5-9.
Add: *A5C153, between U7 pin 12 and U7 pin 13.
Add: *A5C154, between U7 pin 35 and U7 pin 40.
Reverse: CR5.
Reverse: CR6.
Change: A5R23 value to 7E0.
Change: A5R24 value to 39.1.
Add: "*Selected by Test" in the bottom margin of page.

Page 8-131. Service Sheet 15, Schematic Diagram.
Change: R171 and R187 value to 500.
Add: E13 between Q22 collector and U1 pin 19.
Add: E14 between Q23 collector and U1 pin 18.

Page 8-145. Service Sheet 18, Schematic Diagram.
Delete: Short across R90.

Page 8-169. Service Sheet 22, Schematic Diagram.
Delete: C6.

▲ Page 8-187. Service Sheet 25. Schematic Diagram.
Change: Value of R30 through R37 to 50.

Page 8-189. Service Sheet 25, Schematic Diagram.
Change: L3 to E13.

Page 8-197. Service Sheet 29, Schematic Diagram.
Add: C3 between Panel + and Panel –. Value is 0.01UF.

Page 8-201. Service Sheet 31 / Signature Analysis.
Replace: Page 8-201 with the revised page in this change sheet.

CHANGE 1

Section 6. Replaceable Parts,

Page 6-14,
Delete: FL1
Add: A26 HP Part Number 01980-66552, CD8, Qty 1, LINE FILTER BOARD ASSEMBLY, Mfr Code Number 28480, Mfr Part Number 01980-66552.

Page 6-15,
Change: MP13 to HP Part Number and Mfr Part Number 01980-01233, CD6.

Page 6-53,
Add: A26 HP Part Number 01980-66552, CD8, Qty 1, LINE FILTER BOARD ASSEMBLY, Mfr Code Number 28480, Mfr Part Number 01980-66552.
Add: A26C1 HP Part Number 0160-4323, CD8, Qty 1, CAPACITOR-FXD.
Add: A26C2 HP Part Number 0160-4281, CD7, Qty 2, CAPACITOR-FXD 2200PF ±20%, Mfr Code Number 28480, Mfr Part Number 0160-4281.
Add: A26C3 HP Part Number 0160-4281, CD7, CAPACITOR-FXD 2200PF ±20%, Mfr Code Number 28480, Mfr Part 0160-4281.

Page 8-43, Service Sheet 1B, Schematic Diagram
Delete: Short across R90.

Page 8-59,
Change: Service Sheet 1 Schematic as shown in Figure 1.

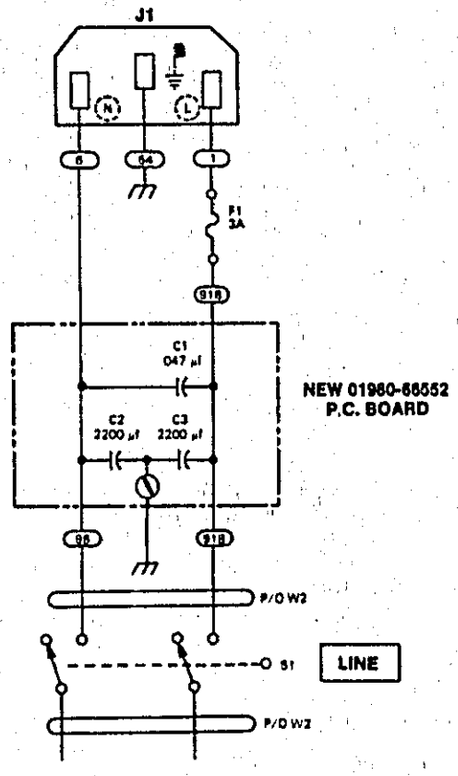


Figure 1

CHANGE 2

Page 6-14. Table 6-2, Replaceable Parts,
Change: A3 to HP Part Number and Mfr Part Number 01980-66544, CD8.

Page 6-25. Table 6-2, Replaceable Parts,
Change: A3 to HP Part Number and Mfr Part Number 01980-66544, CD8.
Change: A3C12 Qty to 3.
Add: A3C41, HP Part Number 0160-0168, CD1, Qty 1, CAPACITOR-FXD 0.1UF ±10% 200WVDC POLYE, Mfr Code 28480, Mfr Part Number 0160-0168.
Add: A3C42, HP Part Number 0160-0165, CD8, Qty 1, CAPACITOR-FXD 0.056UF ±10% 200WVDC, Mfr Code 28480, Mfr Part Number 0160-0165.
Change: A3CR1 Qty to 6.
Delete: A3CR6.
Add: A3CR18, HP Part Number 1901-0040, CD1, DIODE-SWITCHING 30V 50MA 2NS DO-35, Mfr Code 28480, Mfr Part Number 1901-0040.

Page 6-26. Table 6-2, Replaceable Parts,
Delete: A3Q14.
Add: A3Q29, HP Part Number 1854-0215, CD1, TRANSISTOR NPN SI PD=350MW FT=300MHZ, Mfr Code 04713, Mfr Part Number 2N3904.
Change: A3R19 Qty to 10.

Page 6-27. Table 6-2, Replaceable Parts,
Delete: A3R77.
Change: A3S1 to HP Part Number 3101-1618, CD6, Qty 1, SWITCH-SL DPDT MINTR .5A 125VAC/DC PC, Mfr Code 28480, Mfr Part Number 3101-1618.
Add: A3VR3, HP Part Number 1902-3059, CD0, Qty 1, DIODE-ZNR 3.83V 5% DO35 PD=.4W, Mfr Code 28480, Mfr Part Number 1902-3059.

Section 8.

Page 8-77. Service Sheet 5, Schematic Diagram,
Add: A3C42, .056μf between A3J3 pin 5 and "A" ground.

Page 8-83. Service Sheet 6, Schematic Diagram,
Add: CR18, R108, Q29, R107, and VR3 to schematic diagram as shown in Figure 4.
Add: C41, 0.1μf between +100V (at P1 pin 38) and "A" ground.
Change: .6VF at collectors of Q20, Q23, and Q27 to +15V. Reverse: Position of R89 and C31.

Page 8-84. Service Sheet 6, Component Locator,
Add: CR18, Q29, R107, R108, VR3, C41, and C42 to component locator as shown in Figure 5.

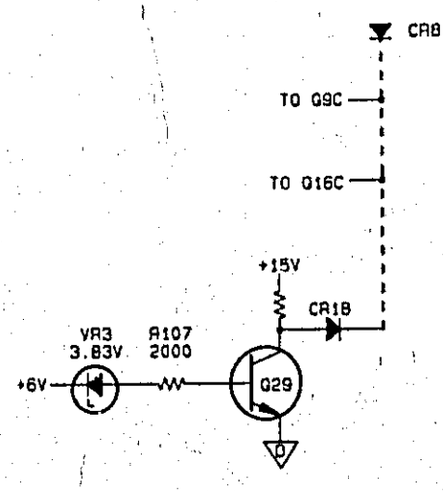


Figure 4

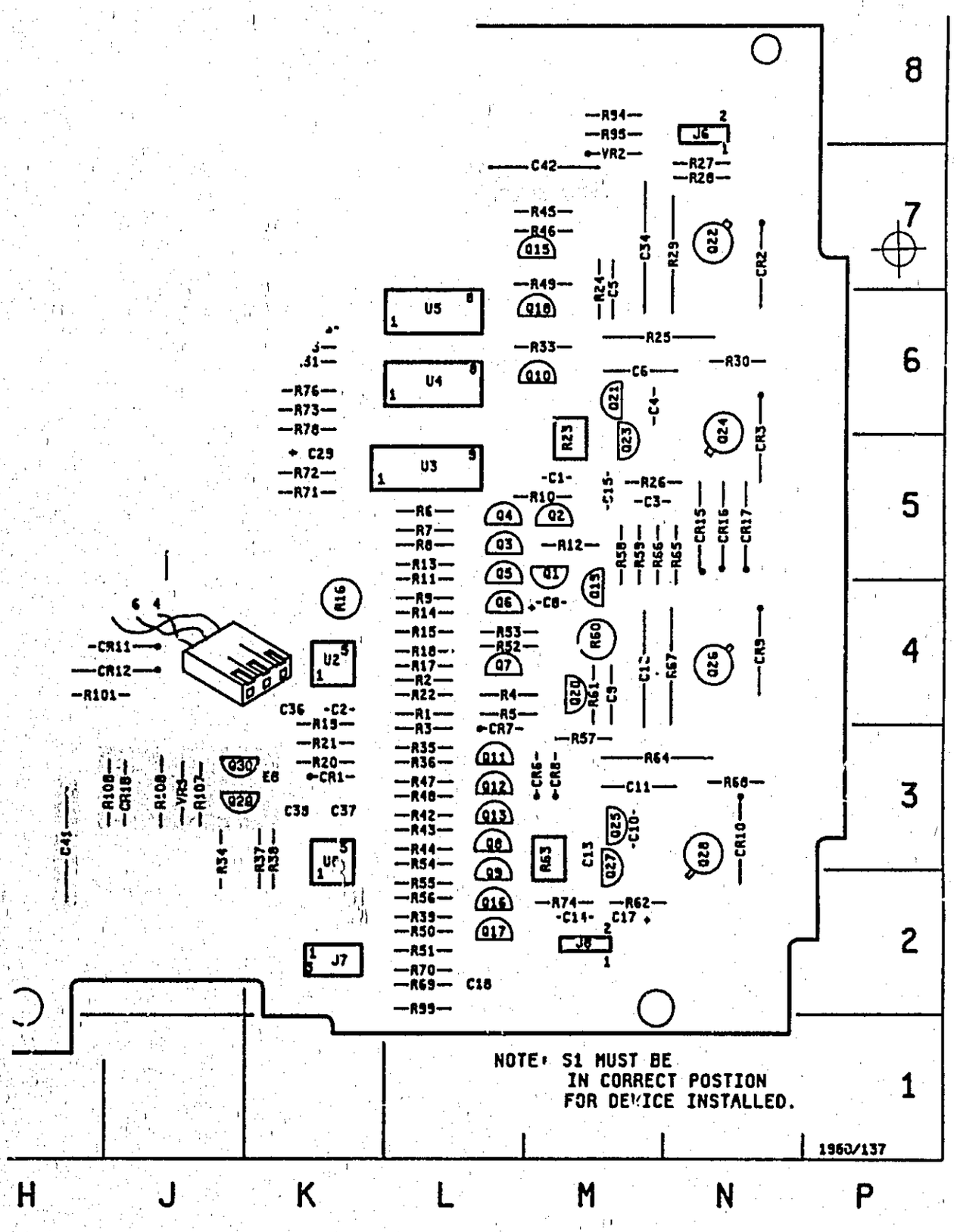

NOTE: S1 MUST BE
IN CORRECT POSTION
FOR DEVICE INSTALLED.
1960/137
H J K L M N P
8 7 6 5 4 3 2 1
U5
U4
U3
U2
U1
J7
J6
J6

Figure 5

Table 1-1a. Trigger Flag Specifications

VERTICAL

SOURCES: Selectable from Channel 1, Channel 2, External Trigger inputs, or Enhancement Module. Main and Delayed sources are independently selectable.

TRIGGER THRESHOLD: Main or Delayed Trigger Level; expressed in divisions for internal sources, volts for external trigger inputs.

Dynamic range: ±20.00 div for internal sources; ±12 V for ext ÷ 10; ±1.2 V for ext ÷ 1.

Resolution: 0.01 div for internal sources; 0.01 V for ext ÷ 10; 0.001 V for ext ÷ 1.

Accuracy (%): dc to 10 MHz; 10 ns pulse width minimum; internal sources only.

$$\text{Gain Error} + 100 \times \frac{\text{Offset} \times \text{Deflection} + \text{Hysteresis Voltage Error}^*}{\text{V input}}$$

*Refer to definitions

Gain Error: Measured at frequency of calibration; ±4%.

DC Offset: Internal sources only: ±0.5 div.

Hysteresis: Internal sources only, measured at dc, high frequency reject off: for deflection factors <10 mV/div, typically 0.4 div; for deflection factors ≥10 mV/div, typically 0.2 div.

Repeatability: Within 20° to 30°C and 8 hours; internal sources only; 0 or 1 trace displayed:

Deflection Factor	Repeatability (div)
<10 mV/div	±0.20
≥10 mV/div	±0.15

Slope: Either positive or negative slope can be selected.

COUPLING:

ac: attenuates signals <10 Hz.

dc: direct coupled.

HF Rej: attenuates signals > approx 35 kHz.

LF Rej: attenuates signals < approx 35 kHz.

HORIZONTAL

GATE START TIME: Gate starts at end of delay.

Delayed Trigger Latched Mode

Delay: 1980A/B Time Delay

Range: 0 to 9.9999999999 s

Resolution: 100 ps

Accuracy: ±(Delay Time Accuracy + Delay Jitter) − Comparator Setup Time + Hysteresis Time Error

Delay Time Accuracy:

Delay or Time Interval	
<200 μs	≥200μs
±(2 ns + 0.1% of reading)	±(2 ns + 0.05% of reading)

Delay Jitter: 0.002% of delay time; at 10 MHz ±10 kHz, .01% of delay time.

Main Trigger Latched Mode

Delay: 1980A/B Events Delay

Range: 0 to 99999999 events

Resolution: 1 event

Maximum rep rate: 15 MHz

COMPARATOR SETUP TIME: Minimum time after main trigger until a delayed trigger event can be detected: ≤45 ns.

GATE WIDTH: Approximately (1.1 × delayed sweep speed) + 20 ns min gate width (at 5e−9 s/div) ≤75 ns.

OPERATING CHARACTERISTICS

FREQUENCY RESPONSE: Typical gain error as a function of frequency; internal sources only; when calibrated at 1.8 kHz using the front panel calibration.

Frequency	dc	100 Hz	1.8 kHz	1 MHz	10 MHz
% Gain Error V/div≤10 mV	4.5	1.7	0±4%	−4.7	−8
V/div≥10 mV	4.5	1.7	0±4%	−2.9	−5.6

LOCAL OPERATION: Not available from 1980A/B's front panel.

REMOTE OPERATION

Dynamic flag: may be used only in V vs T scope mode, and in any horizontal mode.

Latched flag: may be used only in V vs T scope mode and only in intensified, delayed, and dual horizontal modes.

Sweep Wait Timer: Provides programmable time-out for sweep completion. For proper Trigger Flag operation, sweep wait time must be set ≥ the maximum sweep cycle time. Sweep cycle time is given by the expression:

MAX[MS speed or (DS speed + delay)] + trigger period + sweep holdoff

Sweep holdoff time is a function of sweep speed (the maximum, either main or delayed sweep).

Sweep Speed	Holdoff Time (typ)
10 ms - 1 s	200 ms
100 μs - 9.99 ms	2 ms
1 μs - 99.9 μs	11.2 μs
5 ns - 999 ns	1.2 μs

GENERAL

OPERATING ENVIRONMENT

Temperature: 0° to +55°C.

Humidity: to 95% relative at +40°C.

Altitude: to 4600 m (15 000 ft).

Vibration: vibrated in three planes for 15 mm each with 0.38 mm (0.015 in.) excursion, 10 to 55 Hz.

HYSTERESIS VOLTAGE ERROR:

Flag Mode	Signal Type	Hysteresis Voltage Error
Latched	+ peak	−Hysteresis × Deflection/2
Latched	− peak	+Hysteresis × Deflection/2
Dynamic*	dc	±Hysteresis × Deflection/2

*algorithm dependent, hysteresis error is zero if the mean of arm and fire point is taken.

HYSTERESIS TIME ERROR:

$$\frac{\text{Hysteresis} \times \text{Deflection}/2}{\text{input signal slew rate at trigger point}}$$

3-47a. Trigger Flag Operation Checks

Description The following procedures can be executed from the Oscilloscope Measurement Systems front panel to check the internal Trigger Flag Operation. These procedures check that the Oscilloscope Measurement system can determine signal amplitude and pulse width using the trigger flag. It is assumed the trigger flag bit will be available at the HP-IB if the bit is operating internally and "HP-IB I/O Checks" operate properly.

Procedure To check Trigger Flag internal operation a Balance Self-Cal then a Confidence test is ran.

To execute the Balance Self-Cal press the following key sequence:

OPTION MENU

CHAR INTEN CALIBRATE SELF CAL

CHAR INTEN BALANCE SELF CAL

NOTE

Do not apply any signals to channel 1 or 2 inputs while executing the Balance Self-Cal procedure.

When the Banance Self-Cal rountine is complete, execute a Confidence Test by pressing the following key sequence.

OPTION MENU

CHAR INTEN CONFIDENCE TEST 1980A/B

Then connect the calibrator signal to the vertical channel to be tested. To execute the test, press any key except [illegible] or FIND MEAS .

Indication While Balance Self-Cal is executing, advisory message Balance Self-Cal CH1 (or CH2) is displayed on the CRT. The Balance Self-Cal finishes without an error condition. While Confidence test is executing signals are auto ranged and upon completion the advisory passed test is displayed on the CRT.

Error Messages (Cont'd)

HP-IB

Table 3-11. Hardware Error Codes

LED code	HP-IB Code	Error Description
Err -0	26	ROM 0 Failed checksum
Err -2	28	ROM 2 Failed checksum
Err -4	30	ROM 4 Failed checksum
Err 6	32	ROM 6 Failed checksum
Err -8	34	ROM 8 Failed checksum
Err 10	36	ROM 10 Failed checksum
Err -12	38	ROM 12 Failed checksum
Err -14	40	ROM 14 Failed checksum
Err -16	42	ROM 16 Failed checksum
Err -18	44	ROM 18 Failed checksum
Err -20	46	ROM 20 Failed checksum
Err -22	48	ROM 22 Failed checksum
Err -24	50	ROM 24 Failed checksum
Err -26	52	ROM 26 Failed checksum
Err -28	54	ROM 28 Failed checksum
Err -30	56	ROM 30 Failed checksum
Err -31	57	Confidence-test vertical channel error
Err -32	58	Confidence-test horizontal range error
Err -33	59	Confidence-test 10 V signal not found
Err -34	60	Confidence-test 1 V signal not found
Err -35	61	Confidence-test 0.1 V signal not found
Err -36	62	Confidence-test 0.02 V signal not found
Err 40	66	1980A/B cal factor checksum error
Err 51	77	Channel 1 failed autobalance
Err 52	78	Channel 2 failed autobalance
Err -60	86	Scratch RAM (U16) failed
Err -61	87	Nonvolatile RAM (U42, 43) failed
Err -62	88	Character RAM (U32, 33) failed
Err -64	90	Feature RAM (U34, 36) failed
Err -66	92	Save/Recall RAM (U35, 37) failed
Err 72	98	Horizontal Word output failed

Trigger Flag

HP-IB

Description The trigger flag is a trigger circuit output that can be monitored via the HP-IB. It is used in remote operation to detect trigger events and to make voltage and timing measurements.

Trigger flag detects whether a valid trigger event occurred. Either the main or delayed trigger can be selected to set the flag. The four modes of trigger flag are described below.

Delayed Source Latched (TF1) - Flag is set to one if a delayed trigger occurs during gate time. Delay to start of gate is in units of time. Gate starts at the end of delay time, stops at end of delayed sweep. Figure 3-23 contains examples of latched mode trigger flag state as delayed time is changed.

Delayed Source Dynamic (TF2) - Flag follows delayed trigger source:
If positive slope trigger is selected flag is one while trigger source is greater than trigger level.

If negative slope trigger is selected flag is one while trigger source is less than trigger level.

Figure 3-24 contains examples of trigger flag state in dynamic mode.

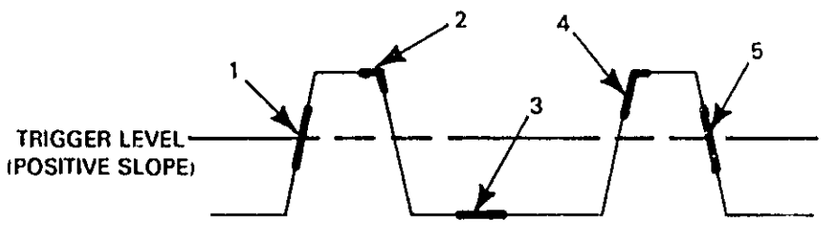
Main Source Latched (TF3) - Flag is set to 1 if a main trigger occurs during gate time. Delay to start of gate is in units of events (Digital Delay). Gate starts at end of count of delay trigger events, stops at end of delayed sweep.

Figure 3-23 contains examples of latched mode trigger flag state as delay time is changed.

Main Source Dynamic (TF4) - Flag follows main trigger source:
If positive slope trigger is selected flag is one while trigger source is greater than trigger level.

If negative slope trigger is selected flag is one while trigger source is less than trigger level.

Figure 3-24 contains an example of trigger flag state in dynamic mode.



1) FLAG = 1
2) FLAG = 0
3) FLAG = 0
4) FLAG = 0
5) FLAG = 0

Figure 3-23. Latched Mode Trigger Flag State Examples

HP-IB

Trigger Flag (Cont'd)

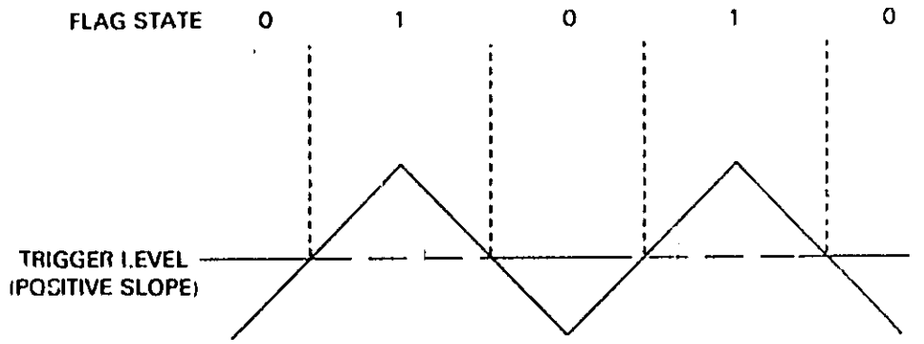


Figure 3-24.Dynamic Mode Trigger Flag State Example

A special horizontal mode must be selected to use the trigger flag. This mode is enabled with the program code "SG". This command puts main sweep in single mode, resets the sweeps, and initializes the trigger flag.

The "SG" command does not affect any of the variable function parameters.

The 1980A/B can be programmed to issue the Require Service message at the completion of "SG" enabled sweeps. Also, a timer can be set to cause Require Service after a maximum sweep wait time has expired. The procedure for enabling Require Service after "SG" enabled sweeps or timeout is described in the "Service Request Condition" Detailed Operating Instruction.

Procedure Follow this general procedure when making trigger flag measurements:

Preset horizontal and vertical functions for the measurement procedure.

Set the trigger flag mode and enter the sweep wait time.

Enter RQS mask value for end of sweep if SRQ interrupt is desired.

Start search with "SG" command and wait for end of sweep or timeout interrupt (or test status byte for these conditions).

Test trigger flag state.

HP-IB **Program Codes**

Set trigger flag mode:

TF <mode>

mode::= **1** delayed trigger source, latched
2 delayed trigger source, dynamic
3 main trigger source, latched
4 main trigger source, dynamic

Trigger Flag (Cont'd)

HP-IB

Initialize trigger flag and enable sweep:

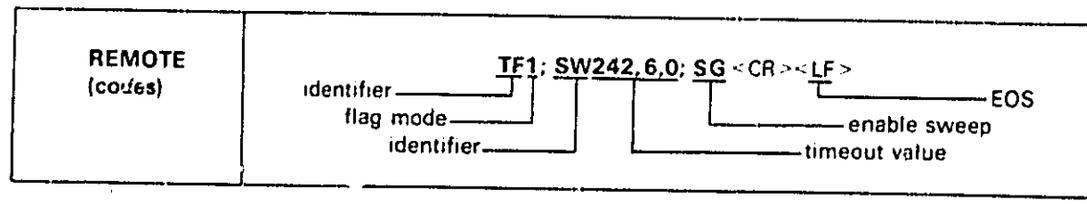
SG

Enter maximum sweep wait time:

SW <factor1>,<factor 2>,<factor 3>

factor 1 ::=	integer ddd 0 to 255 units of 23 μsec
factor 2 ::=	integer ddd 0 to 255 units of 5.84 msec
factor 3 ::=	integer ddd 0 to 255 units of 1.5 sec

Example Program the trigger flag to detect a trigger from the delayed trigger source during delayed sweep. Set maximum wait time =40.6 msec and enable sweep.



Comments After the program code "SG" is sent to the 1980A/B, it is in a special state that is not indicated on the front Panel. After executing a routine using "SG", proper instrument state can be restored by sending the program code "SM1" (selecting V vs T mode.)

When using trigger flag in the latched mode (TF1 or TF3) the trigger flag state should be checked with the "OQ" command immediately after the program code "SG" has been sent. This should be done because many program codes cause the trigger flag status bit to be reset. The program codes shown in the table below should not be sent in the same data message as "SG" or prior to reading the trigger flag status bit.

HP-IB

Trigger Flag (Cont'd)

Program Code	Function
AC	Vertical Mode
AS	Autoscope
BW	Bandwidth Limit
CG	Charactor Generator
CH	Text Display
DM	Sweep Mode, Delayed
DS	Sweep Speed, Delayed
DT	Trigger, Delayed Sweep
DV	Delta Volts
DZ	Delta Time
FP	Intensity, Readout
HM	Horizontal Mode
IN	Intensity Limit
KY	Key
MM	Sweep Mode, Main
MS	Sweep Speed, Main
MT	Trigger, Main Sweep
RC	Control Knob
SA	Autoscope (selective)
SG	Trigger Flag
SK	Soft Key
SM	Scope Mode
TV	Trigger View
VC	Vertical Coupling
VM	Vertical Mode
VS	Vertical Deflection Factor

If the main trigger source-latched mode is selected The delay to start of gate is in units of events (digital delay). In latched mode, the duration of delayed sweep must be considered. Sweep length is not calibrated and can increase from the nominal 11 divisions to more than 40 divisions at fast sweep speeds.

Sweep Wait Timer - Provides programmable time-out for sweep completion. For proper Trigger Flag operation, sweep wait time must be set => the maximum sweep cycle time. Sweep cycle time is given by the expression:

MAX [MS speed or (DS speed + delay)] + trigger period + sweep holdoff

Related Sections

Delay
Instrument Status
Horizontal Mode
Reading Values Via HP-IB
Service Request Conditions
Sweep Mode, Delayed
Sweep Mode, Main
Trigger, Delayed Sweep
Trigger, Main Sweep

OPERATIONAL VERIFICATION.

4-4A. 1980A/B Operation Verification Test.

Description:

During this operational verification test, the Autoscope capability will be repeatedly checked; Confidence test will be used to check all attenuator ranges ability to pass various signal levels and the ability to trigger on these signals; two ranges of the attenuator will be checked for amplitude accuracy; Delay accuracy, Calibrator frequency, and limited sweep accuracy will be checked.

Equipment:

BNC Cable

Procedure:

a. Apply power to the 1980 Oscilloscope Measurement System.

NOTE

Insure the fan is running (audible) and that "Err 40" is not displayed in the LED display. If either of these conditions occur, abort this test and repair or calibrate as necessary.

b. Press AUTO-SCOPE SELECTIVE. Insure that no signal is attached to the 1980s inputs.

1. Observe that the Autoscope "Routine" runs.

2. Check the characters displayed on the CRT are as follows:

CH1 = 2.000 DC
MT = CH1
MAIN = 50.0µs DC

c. Connect the back panel Calibrator output to channel 1 with a BNC cable.

d. Press AUTO-SCOPE SELECTIVE.

1. Observe that approximately two cycles of the calibrator waveform is displayed and that the waveform is properly triggered.

2. Observe that the characters displayed on the CRT are as follows:

CH1 = (approximately) 250-500 mV DC
MT = CH1
MAIN = 100 .us DC (Typical)

e. Rotate the Control Knob and note that the sweep speed changes as the knob is rotated.

PERFORMANCE TEST

NOTE

The sweep start point should be at the left graticule but may "pull" right at 100.μS/Div. There is no specification on this phenomenon and some instruments may exhibit about one minor division of "offset".

f. Press OPTION MENU.

g. Press CHAR ON-OFF CONFIDENCE TEST (OPTION 8).

h. Press any key except Find Beam or SK8 OPTION MENU OFF and observe that the confidence test is executed without errors and PASSED TEST is displayed on the CRT at the end of the routine.

i. Press VOLTS/DIV (Channel 1).

j. Rotate the Control Knob for a reading of CH1=100.mV/Div. on the CRT.

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

k. Rotate the Control Knob for a reading of CH1=99.9mV/Div.

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

l. Connect the Calibrator Output signal to the Channel 2 input.

m. Press OPTION MENU.

n. Press CHAR ON-OFF CONFIDENCE TEST (OPTION 8).

o. Press any key except Find Beam or SK8 OPTION MENU OFF and observe that the confidence test is executed without errors and PASSED TEST is displayed on the CRT at the end of the routine

p. Press VOLTS/DIV (Channel 2).

q. Rotate the Control Knob for a reading of CH2=100.mV/Div. on the CRT.

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

r. Rotate the Control Knob for a reading of CH2=99.9mV/Div.

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

s. Press AUTO-SCOPE (SELECTIVE).

t. Press INTEN (OFF SKP'S).

PERFORMANCE TEST

u. Press DELAY.

v. Rotate the Control Knob to place the intensified portion on the first falling edge of the waveform.

w. Press DUAL then press FINE.

x. Rotate the Control Knob to put the first falling edge on the center graticule.

y. Press Δ AT.

z. Rotate the Control Knob to put the second falling edge on the center graticule.

1. The CRT display should read Δ T= [illegible] ±3.7us and the LED display should read 537.60-(±3.7 μs.)

aa. Press AUTO-SCOPE.

ab. Press FINE.

ac. Rotate the Control Knob to set Sec/Div (Main) for one complete cycle displayed over the 10 division graticule.

1. Observe that the CRT and the LED display indicates 53.8 μs/Div (±1.6 μs.)

PERFORMANCE TEST

4-4B. 19860A Operation Verification.

DESCRIPTION:

The following procedure checks that the digitizer is operational and is not beyond automatic calibration; proper vertical dot placement checks for right HP-IB data output; amplitude and offset are checked.

PROCEDURE:

a. Connect the Calibrator Output signal to Channel 1 input.

b. Press AUTO-SCOPE SELECTIVE.

c. Press OPTION MENU.

d. If 19860A is installed it should be noted at SK6. Press CHAR INTEN CALIBRATE & UTILITIES.

e. Press 5 WAVEFORM STORAGE TEST & CAL.

f. Press 6 INTERNAL ADJ. PATTERN-NORMAL.

g. After "update" occurs.:

1. Observe the data in the upper right corner is as follows:

024	524	(±23 for both)
[illegible]	15 to 240	(typically 150-200)

2. Observe two short straight lines, one near the top graticule and one near the center graticule with 5 division separation.

3. Observe dots at top and bottom of vertical center graticule ±1 minor division.

4. Observe dots at left and right ends of the horizontal center graticule ±1 minor division.

Note

Ignore the dots at the upper left corner and the center of the graticule.

h. Press any key to exit the test pattern.

i. Press 8 OPTION MENU.

j. If the serial prefix of the 1980 is 2142A or above or if the operating ROM and Display panel have been updated, press 8 OPTION MENU OFF to exit the option menu. If the serial prefix is below 2142 and the ROMs and Display panel have not been updated, go to step l.

PERFORMANCE TEST

k. Press [illegible] to store displayed signal into memory one.

1. Observe that no error messages are reported after the store.

2. Observe that the stored waveform represents the real time waveform.

3. Observe that the stored waveform is positioned vertically within one minor division of the real time waveform.

4. Observe that the stored waveforms amplitude is within one minor division of the real time waveform.

Note

The stored waveform may be offset horizontally due to sweep pull at 100 µs/div and any horizontal offset noted with the horizontal dots in the pattern test.

l. If the serial prefix of the 1980A/B is below 2142 and the ROMs and display panel have not been updated, press [illegible]

m. Press [illegible]

1. Observe that no error messages are reported after the store.

2. Observe that the stored waveform represents the real time waveform.

3. Observe that the stored waveform is positioned vertically within one minor division of the real time waveform.

4. Observe that the stored waveforms amplitude is within one minor division of the real time waveform.

Note

The stored waveform may be offset horizontally due to sweep pull at 100 us/div and any horizontal offset noted with the horizontal dots in the pattern test.

PERFORMANCE TEST

4-4C. 1950A Operation Verification.

DESCRIPTION:

The following procedure insures all attenuator ranges can pass various level signals and internal sync paths are O.K.; two attenuator ranges will be checked for amplitude accuracy.

PROCEDURE:

a. Press OPTION MENU .

1. If the 1950A is installed, it should be noted at SK7.

b. Connect Calibrator Output signal to Channel 3 input.

c. Press RECALL 1950A, then press CHAR ON-OFF then press any key except Find Beam or SK8.

1. Observe that the confidence test is executed without errors and PASSED TEST is displayed on the CRT at the end of the routine.

d. Press VOLTS DIV (Channel 3).

e. Rotate the Control Knob for a reading of on the CRT.

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

f. Rotate the Control Knob for a reading of

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

g. Press OPTION MENU .

h. Connect Calibrator Output signal to Channel 4 input.

i. Press RECALL 1950A, then press CHAR ON-OFF then press any key except Find Beam or SK8.

1. Observe that the confidence test is executed without errors and PASSED TEST is displayed on the CRT at the end of the routine.

j. Press VOLTS DIV (Channel 4).

k. Rotate the Control Knob for a reading of on the CRT.

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

l. Rotate the Control Knob for a reading of

1. Observe that the displayed signal is 10 Divisions ±.3 Div.

PERFORMANCE TEST

4-4D. 1965A OPERATION VERIFICATION TEST.

Description:

This test uses the 1980 calibrator signal to verify that the 1965A is operational. This procedure will not test the 1965A against it's performance specifications.

Equipment:

BNC Cable

Procedure:

a. Press OPTION MENU .

1. If the 1965A is installed it should be noted at SK7.

b. Connect the 1980 Rear Panel Cal output to the channel 1 or channel 2 input to the 1980.

c. Press AUTO-SCOPE .

Note

After the Autoscope is completed, the 1965A may or may not have FREQ A lighted. Press FREQ A if it is not lighted.

d. Check for a frequency readout of approximately with all except the least significant digit being stable.

e. Press PERIOD A on the 1965A. Check for a Period readout of approximately with all except the least significant digit being stable.

f. Press INTEN on the 1980 and ensure the Delayed Trigger Slope is set to ⎍ (+) slope. (If the slope key is pressed, ignore the advisory message that is displayed on the CRT.)

g. Press T INTVL A→B , GATED A THRU B , and MAIN TRIG (B Source)

h. Press ARM DELAY and adjust the Control Knob to place intensified portion of the trace on the second positive waveform edge.

i. The time interval readout in the upper left corner of the CRT should read the same as the value read in step e ± .002 μs.

1980A/B OPERATION VERIFICATION RECORD
HP MODEL 1980A/B OSCILLOSCOPE MEASUREMENT SYSTEM

Paragraph Number	Test	Result	
		YES	NO
4-4A-b	1. Autoscope Operates		
	2. Characters displayed are correct		
4-4A-d	1. Approximately 2 cycles displayed		
	2. Characters displayed are correct		
4-4A-e	Sweep Speed Changes		
4-4A-h	Confidence Test is executed and PASSED TEST is displayed		
4-4A-j	1. Signal is 10 divisions ± .3		
4-4A-k	1. Signal is 10 divisions ± .3		
4-4A-o	Confidence Test is executed and PASSED TEST is displayed		
4-4A-q	1. Signal is 10 divisions ± .3		
4-4A-r	1. Signal is 10 divisions ± .3		
4-4A-z	1. Reading is 537.60 μs ± 3.7 μs		
4-4A-ac	1. Reading is 53.8 μS/Div ± 1.6 μs		

19860A OPERATION VERIFICATION RECORD
HP MODEL 19860A DIGITAL WAVEFORM STORAGE OPTION

Paragraph Number	Test	Result YES	Result NO
4-4B-g	1. Data is correct	____	____
	2. Lines are 5 divisions apart	____	____
	3. Dots at top and bottom of center vertical graticule ±1 minor division	____	____
	4. Dots at left and right of center horizontal graticule ±1 minor division	____	____
4-4B-k	1. No error messages after store	____	____
	2. Stored waveform is same as real time waveform	____	____
	3. Stored waveform is within 1 minor division vertically of real time waveform	____	____
	4. Stored waveforms amplitude is within 1 minor division of real time waveform	____	____
4-4B-m	1. No error messages after store	____	____
	2. Stored waveform is same as real time waveform	____	____
	3. Stored waveform is within 1 minor division vertically of real time waveform	____	____
	4. Stored waveforms amplitude is within 1 minor division of real time waveform	____	____

1950A OPERATION VERIFICATION RECORD
HP MODEL 1950A 2 CHANNEL EXPANSION MODULE

Paragraph Number	Test	Result	
		YES	NO
4-4C-c	1. Confidence Test is executed and PASSED TEST is displayed	_____	_____
4-4C-e	1. Signal is 10 divisions ± .3 divisions	_____	_____
4-4C-f	1. Signal is 10 divisions ± .3 divisions	_____	_____
4-4C-i	1. Confidence Test is executed and PASSED TEST is displayed	_____	_____
4-4C-k	1. Signal is 10 divisions ± .3 divisions	_____	_____
4-4C-l	1. Signal is 10 divisions ± .3 divisions	_____	_____

1965A OPERATION VERIFICATION RECORD
HP MODEL 1965A GATED UNIVERSAL COUNTER

Paragraph Number	Test	Result	
		YES	NO
4-4D-d	Frequency ≅ 1.8601xxxxkHz Only the last digit is changing	_____	_____
4-4D-g	Period ≅ 537.6xxxx us Only the last digit is changing	_____	_____
4-4D-i	Reads the same as step e ±.002 μs	_____	_____

Table 5-2. Required Adjustments After Repair

	5-8	5-9	5-10	5-11	5-12	5-13	5-14	5-15	5-16	5-17	5-18	5-19	5-20	5-21	5-22	5-23	5-24	5-25	5-26	5-27	5-28	5-29	5-30	5-31	5-32	5-33
A1 Board (LVPS)	X	X	X						X					X		X	X					X	X			X
A1 LVPS components (IC's and pass devices)	X	X																			X					
Vertical Output Hybrid																	X			X	X		X			X
Horizontal Output components														X		X						X				
A2;HV xfmr;multiplier;osc			X	X		X	X				X	X									X		X			
A3 GATE board			X	X		X	X	X		X	X	X									X		X			
A4 PROCESSOR board																		X	X		X					
NV RAM's																					X					
A5 SCOPE board													X	X	X		X		X	X	X		X			X
Vertical Hybrid																	X			X	X		X			X
Trigger Hybrid																				X	X		X			
Horizontal Hybrid													X	X	X						X					
A10 Delay Line Assy																					X					X
A12 Battery (Low Voltage or Inst. off)																					X					
A13 Vertical Attenuator board																					X			* X	* X	
A14 Trigger Attenuator board																					X			X		
A19 RPG Assy																										
A20 CRT Assy	X		X	X	X	X	X	X	X	X	X	X		X		X	X					X	X			X

* These adjustments should be made for the A13 sections only and should be made before a Front Panel Calibration is attempted.

APPENDIX II

The information in appendix is for updating of operational changes. When the HP-IB ROM is installed, the operation listed under "NEW DEVICE (1818-3148)" is in effect.

Operating Changes

Area	Old Device (1818-1639)	New Device (1818-3148)
OPTION MENU	SK5 Text was "HP-IB ADDRESS MODE	SK5 Text is "HP-IB ADDRESS
HP-IB ADDRESS (Sub Menu)	SK3 was "INCREMENT" SK4 was "DECREMENT" SK6 was "CHANGE ADDRESS MODE"	SK3 is " ↑ " SK4 is " ↓ " SK6 is "MODE"
TEST COMMAND	"TX1,;" would wipe out ENTIRE TEXT Display	Now clears only line 1 of display
HP-IB allowed characters per line	28 characters	35 characters
Blank Spaces	Blank spaces not allowed in instructions	Blank spaces allowed
Spurious Syntax Errors and Bus Lock ups	Could occasionally occur, (e.g. if an instruction took longer to parse than the time between instruction inputs).	Program corrections made to overcome these spurious occurrences.

SERVICE SHEET 31 SIGNATURE ANALYSIS

Note

Remove Expansion Module before performing tests.

TEST 15. HP-IB ROM Test, HP Part No. 1818-3148

Note

This test checks the ability of the processor to access the HP-IB ROM. Ensure an external controller is not connected to the 1980 when this test is being performed.

a. Set instrument power to off.

b. Signature Analyzer Connections:

START ⅂ to A23U1-20 (IBROM)
STOP ⌋ to A4U3-7 (IBROM)
CLOCK ⌋⌈ to A4TP5 (LRD)

c. Set A4S1-B and A4S1-C to closed.

d. Set instrument power to on.

e.

TEST POINT	SIGNATURE
Probe open	826P
A0 (U1-8)	7P25
A1 (U1-7)	2A1F
A2 (U1-6)	A206
A3 (U1-5	C133
A4 (U1-4)	8P3U
A5 (U1-3	3319
A6 (U1-2)	7C47
A7 (U1-1	C25F
A8 (U1-23)	5H21
A9 (U1-22)	19H6
A10 (U1-19)	HP66
A11 (U1-18)	7A70
AD0 (A4U57-18)	P7U1
AD1 (A4U57-17)	CH7H
AD2 (A4U57-16)	09P4
AD3 (A4U57-15)	A747
AD4 (A4U57-14)	8A9H
AD5 (A4U57-13)	2HFC
AD6 (A4U57-12	1P25
AD7 (A4U57-11)	CA9A

f. Set A4S1-B and A4S1-C to open.