8350A
SWEEP OSCILLATOR
(Including Options 001 and 400)

SERIAL NUMBERS

This manual applies directly to HP Model 8350A Sweep Oscillator having serial number prefix 2024A.

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed 2007A and 2019A.

For additional information about serial numbers, refer to INSTRUMENTS COVERED BY MANUAL in Section I.

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MANUAL PART NO. 08350-90001

Printed: OCTOBER 1980

HEWLETT PACKARD

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3) Schematic diagram pages are typically scanned in black and white at 600 dpi unless the original manual had colored high lighting (as is the case for some 70's vintage Tektronix manuals).

Thanks

Dave & Lynn Henderson

Dave & Lynn Henderson
Artek Media

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been designed and tested in accordance with international standards.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND

This is a Safety Class I product (provided with a protective earthing terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer make sure the common terminal is connected to the neutral (grounded side of mains supply).

SERVICING

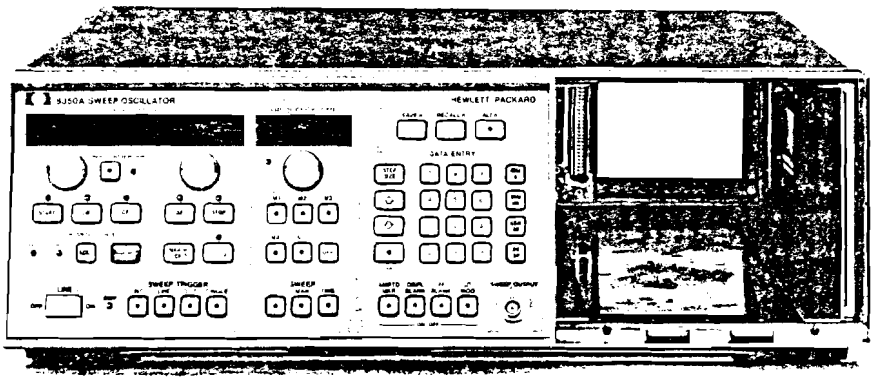
WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

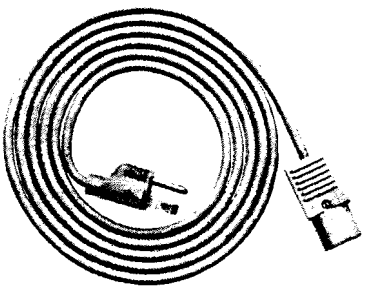
Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

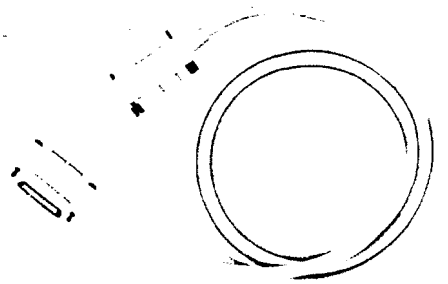


HP 8350A SWEEP OSCILLATOR

POWER CABLE*

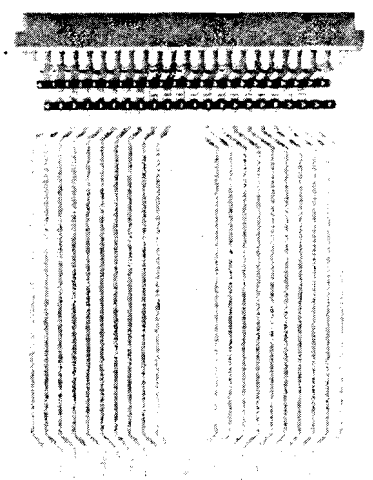


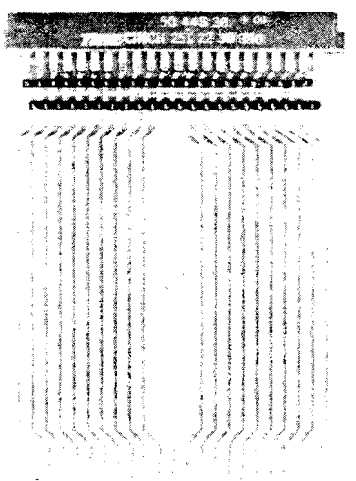
HP-IB INTERCONNECT CABLE
HP 10631B

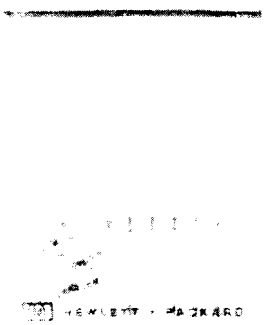


*POWER CABLE/PLUG SUPPLIED DEPENDS ON COUNTRY OF DESTINATION. REFER TO SECTION II FOR PART NUMBER INFORMATION.

ACCESSORY KIT SUPPLIED
08350-60020







FUSE KIT

44-PIN EXTENDER BOARDS
08350-60031 (EACH)

Figure 1-1. Model 8350A Sweep Oscillator With Accessories Supplied

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This Operating and Service Manual contains information required to install, operate, test, adjust, and service the Hewlett-Packard Model 8350A Sweep Oscillator. Figure 1-1 shows the Model 8350A and the accessories supplied with the instrument.

1-3. This manual is divided into eight major sections which provide the following information:

a. SECTION I, GENERAL INFORMATION, includes a brief description of the instrument, safety considerations, specifications, supplemental characteristics, instrument identification, options available, accessories available, and a list of recommended test equipment.

b. SECTION II, INSTALLATION, provides information for initial inspection, preparation for use, battery information, rack mounting, storage, and shipment.

c. SECTION III, OPERATION, consists of three subsections which contain general operating information, local operation information (non-HP-IB), and remote operation information (Programming Notes which provide information on HP-IB use of the Model 8350A).

d. SECTION IV, PERFORMANCE TESTS, presents procedures required to verify that performance of the instrument is in accordance with published specifications. Performance Tests which are general to most RF plug-in units are given in the section. Performance Test limits and other special tests related to specific RF plug-ins are supplied in each RF plug-in Operating and Service Manual. Included is a Local and Remote Operation Verification procedure.

e. SECTION V, ADJUSTMENTS, presents procedures required to properly adjust and align the Model 8350A Sweep Oscillator mainframe after repair. Refer to the Operating and Service Manual of the specific RF plug-in used for adjustments related to the RF plug-in.

f. SECTION VI, REPLACEABLE PARTS, provides information required to order all parts and assemblies.

g. SECTION VII, MANUAL BACKDATING CHANGES, provides backdating information required to make this manual compatible with earlier shipment configurations.

h. SECTION VIII, SERVICE, provides an overall instrument block diagram with troubleshooting and repair procedures. Each assembly within the instrument is covered on a separate Service Sheet which contains a circuit description, schematic diagram, component location diagram, and troubleshooting information to aid the proper maintenance of the instrument.

1-4. Supplied with this manual is an Operating Information Supplement. This is simply a copy of the first three sections of the manual which should be kept with the instrument for use by the instrument operator.

1-5. On the front cover of this manual is a "Microfiche" part number. This number may be used to order 4- by 6-inch microfilm transparencies of the Manual. Each 4- by 6-inch microfiche contains up to 60 photo duplicates of the manual pages. The microfiche package also includes the latest Manual Changes sheet as well as all pertinent Service Notes.

1-6. Refer any questions regarding this manual, the Manual Changes sheet, or the instrument to the nearest HP Sales/Service Office. Always identify the instrument by model number, complete name, and complete serial number in all correspondence. Refer to the inside rear cover of this manual for a worldwide listing of HP Sales/Service Offices.

Table 1-1. Model 8350A Specifications (1 of 2)

SPECIFICATIONS
8350A SWEEP OSCILLATOR
(with RF Plug-in installed)

FREQUENCY CONTROL FUNCTIONS

Range: Determined by RF plug-in unit used.

Linearity: Refer to RF plug-in unit specifications.

START/STOP Sweeps: Sweeps up from the START frequency to the STOP frequency.

Range: START and STOP parameters are independent, fully calibrated, and continuously adjustable over the entire frequency range. STOP frequency must be greater than or equal to START frequency.

CF/ΔF Sweep: Sweeps symmetrically upward in frequency, centered on the CF (Center Frequency) setting.

ΔF: Frequency width of sweep. Continuously adjustable from zero to 100% of frequency range. START/STOP and CF/ΔF modes can be interchanged without affecting RF output.

ΔF Accuracy: Refer to RF plug-in unit specifications.

CF Accuracy: Refer to RF plug-in unit specifications.

CF Resolution: 0.024% (4096 points across band).

ΔF Resolution: 0.1% of full band (1024 points across band); 0.012% of full band for 1/8 band or less (8192 points across band); 0.0015% of full band for 1/64 band or less (16,384 points across band).

Display Resolution: 5 digits.

CW Operation: Single frequency RF output. When changing between CF/ΔF and CW mode, the CW frequency and the Center Frequency (CF) are equivalent.

CW Accuracy: Refer to RF plug-in unit specifications.

CW Resolution: Same as CF.

Vernier: Adjusts CW frequency of swept range up to ± 0.05% of RF plug-in band being swept. The vernier adds its value to the appropriate frequency parameter and then resets to zero when the adjustment exceeds ± 0.05% for continuous adjustment. The "≠0" LED is on whenever a vernier adjustment value is present.

Vernier Resolution: 4 ppm (64 points between each CW point; 262,144 points across band).

Offset: Allows the CW frequency or center frequency of swept range to be offset by any amount up to the full range of the RF plug-in. After entering an offset and returning the displays to the previous mode, the "≠0" LED will be on indicating that an offset is present; however, the display will remain unchanged.

Resolution: Same as CF.

Accuracy: Refer to RF plug-in unit specifications.

Frequency Markers: Five frequency markers are independently adjustable and fully calibrated over the entire sweep range. Front panel key provides for the selection of either amplitude or intensity markers.

Resolution: 0.4% of selected sweep width (256 points/sweep).

Accuracy: Refer to RF plug-in unit specifications.

Marker Output: Negative rectangular pulse available from the POS Z BLANK connector on the rear panel. Refer to Table 1-2.

Table 1-1. Model 8350A Specifications (2 of 2)

Marker Sweep: RF output is swept between Marker 1 and Marker 2 frequency values. The Marker 1 and Marker 2 frequency values can be entered as permanent sweep values with the SHIFT key. Pressing Marker SWP again returns the instrument to the last START/STOP values.

Marker→CF: Marker-to-Center Frequency function causes the CW or Center Frequency (CF) of the sweep output to equal the frequency of the active marker.

SWEEP AND TRIGGER MODES

Internal: Sweep recurs automatically.

Line: Sweep triggered by ac power line frequency.

External Trigger: Sweep is actuated by an external trigger signal applied to pin 9 of the rear panel Programming Connector on the rear panel. Trigger signal must be > +2 Vdc, wider than 0.5 us, and not greater than 1 MHz in frequency.

Single: Selects mode and triggers/aborts a single sweep.

Sweep Time: Continuously adjustable from 10 ms to 100 seconds. Minimum sweep time may be more than 10 ms depending upon the specific RF plug-in used and the bandwidth swept.

Manual Sweep: Front panel controls (knobs, keyboard, and step keys) provide continuous manual adjustment of frequency between end frequencies set in any of the sweep functions. Resolution is 0.1% of selected sweep width (980 points across sweep).

External Sweep: Sweep is controlled by a zero to +10 volt sweep ramp external signal applied to the front or rear panel SWP OUTPUT/SWP INPUT connectors. Resulting RF Output frequency accuracy will be a function of input sweep ramp accuracy and linearity.

Sweep Output: Positive-going, direct-coupled sawtooth at front and rear panel SWP OUTPUT/SWP INPUT connectors, concurrent with swept RF output. In CW mode, dc output is proportional to the RF plug-in unit full-band frequency. Refer to Table 1-2.

MODULATION CHARACTERISTICS

External AM: Refer to RF plug-in unit specifications. Rear panel BNC connector.

Internal AM: Square wave modulation available at all sweep speeds through front panel control. Refer to RF plug-in for On/Off ratio specifications. Refer to Table 1-2 for frequency characteristics.

External FM: Refer to RF plug-in unit specifications. Rear panel BNC connector.

GENERAL SPECIFICATIONS

Blanking

RF Blanking: When enabled, RF automatically is turned off during retrace and remains off until the start of next sweep.

Display Blanking: POS Z BLANK; direct-coupled, positive rectangular pulse during retrace and bandswitch points of sweep. Negative intensity marker signals are also output through this connector. NEG Z BLANK; direct-coupled, negative rectangular pulse during retrace and bandswitch points of sweep. Both are rear panel BNC outputs. Refer to Table 1-2.

Pen Lift: Output to control the pen lift function of an X-Y recorder. Refer to Table 1-2 for maximum sink current rating.

Counter Trigger (CNTR TRIG): Output for controlling the external trigger input of the HP 5343A Microwave Frequency Counter. Rear panel BNC connector.

Stop Sweep: Input for stopping the progress of a forward sweep. Rear panel BNC connector.

Table 1-2. Model 8350A Supplemental Characteristics (1 of 2)

SUPPLEMENTAL CHARACTERISTICS
8350A SWEEP OSCILLATOR
(with RF Plug-in installed)

INPUT/OUTPUT SIGNAL CHARACTERISTICS

Frequency Marker Output: Rectangular pulse, typically −5 volts peak, available from the POS Z BLANK connector on the rear panel. Source impedance is approximately 1000 ohms.

External Sweep: Sweep is controlled by an External Sweep Input signal applied to the front or rear panel SWP OUTPUT/SWP INPUT connectors. The External Sweep Input must be zero volts at start of sweep, increasing linearly to +10 volts at the end of sweep.

Sweep Output: Direct-coupled sawtooth, zero to approximately +10 volts, at front and rear panel SWP OUTPUT/SWP INPUT connectors concurrent with swept RF output. Zero volts at start of sweep, approximately +10 volts at end of sweep, regardless of sweep width. In CW mode, dc output is proportional to the RF plug-in unit full-band frequency. In SHIFT CW mode, a 0 to +10 volt ramp is output, regardless of CW frequency.

MODULATION CHARACTERISTICS

Internal AM: Square wave modulation available at all sweep speeds. Factory preset to 27.8 kHz although selectable (via internal jumper) to 1000 Hz or 27.8 kHz. Refer to RF plug-in for On/Off ratio specifications.

INSTRUMENT CONTROL

Control Knobs, Step Keys, and Data Entry Keyboard: All instrument parameters, whether time, frequency, or power, may be set in three ways. The control knobs allow for continuous adjustment of any parameter. An exact function value can be entered through the Data Entry Keyboard. For incrementing or decrementing power or frequency values, the Step Keys (Step Up/Step Down) can be used. The step size can be entered by the user or the pre-programmed default values may be used. The SHIFT key is used to effect the function written in blue on the front panel.

INSTRUMENT STATE STORAGE

SAVE n/RECALL n: Up to 9 different front panel settings can be stored in the 8350A via the SAVE n (n=1 through 9) function. Instrument settings are stored in memory locations 1 through 9 and can be recalled randomly or in sequence (1,. . . ,9,1,. . .) with Step Up/Step Down keys or by contact closure to ground of the Step Up Advance (pin 22 on the rear panel Programming Connector).

ALT n: The ALT n function causes the RF output to alternate on successive sweeps between the current front panel setting and the setting stored in memory location n (n=1 through 9).

INSTRUMENT STATE

Instrument Preset: The Instrument Preset (INSTR PRESET) key sets the 8350A into the following predetermined state: the RF output is swept over the full frequency range of the RF plug-in at the maximum or minimum (specified by a presetable configuration switch located within the RF plug-in) specified output power level, the internal square wave AM modulation is off, and the frequency markers are off. Instrument Preset also causes an internal analog and digital self-test to occur. If certain internal errors or failures are detected during the self-test or during normal operation of the 8350A, they are indicated via error code messages in the form of "Ennn" (where n=0 through 9) read from the left FREQUENCY display.

Local Operation: The Local (LCL) key is used to return the 8350A to local control from the remotely controlled state. The REM LED indicates when the 8350A is being controlled remotely. The ADRS'D LED indicates when data is being transmitted or received over the HP-IB.

Table 1-2. Model 8350A Supplemental Characteristics (2 of 2)

REMOTE PROGRAMMING (HP-IB)

Instrument Control: All front panel controls except the line power switch may be controlled or programmed remotely. The 8350A is fully compatible with the HP-IB. The 8350A has both input and output capability, providing complete control of the instrument state. The HP-IB address can be displayed on the front panel and is selectable by the user from 0 to 30. Refer to Table 2-3 for a listing of HP-IB address codes.

HP-IB Functions

Input Mode Functions: All front panel controls except the ac power line switch are programmable. Functions that require numerical values typically have greater entry resolution than is displayed. Several special HP-IB functions are provided that are not available from the front panel.

Frequency Resolution: Same as CF/ΔF plus vernier.

Power Resolution: Refer to RF plug-in unit specifications.

Output Mode Functions: The 8350A can output to a controller an instrument state message that completely describes the present instrument status (sweep mode, trigger mode, etc.) and can supply the present numerical value of any function (sweep time, marker frequencies, power levels, start/stop frequencies, etc.).

GENERAL SPECIFICATIONS

Nonvolatile Memory

Option 001: Continuous memory that retains the contents of all instrument state storage registers and the HP-IB address along with the current instrument state when the ac power is turned off for approximately 20 days.

Display Blanking Outputs

POS Z BLANK: Direct-coupled rectangular pulse approximately +5 volts during retrace and bandswitch points of sweep. Intensity marker signals are also output through this rear panel BNC connector. Marker signals are −4 volt pulses with the exception of the active marker which is −8 volts.

NEG Z BLANK: Direct-coupled rectangular pulse approximately −5 volts during retrace and bandswitch points of sweep. No markers are output from this rear panel BNC connector.

Pen Lift Output: Output to control the pen lift function of an X-Y recorder. Maximum sink current is approximately 600ma.

Rear Panel Programming Connector: Additional control of and information on the 8350A instrument state is provided via a 25-pin rear panel connector. Output signals such as display and RF blanking, X-Y recorder pen lift, HP 8410B and HP 5343A interface signals. Input signals affect the sweep status, display and RF blanking, pen lift outputs, etc. Refer to Figure 2-7 for a complete listing of signals and voltages on the rear panel Programming Connector.

8410B Interface Cable: Permits multi-octave operation of HP 8410B Network Analyzer with the 8350A (order HP Part Number 08410-60146). Connects between 8410B rear panel SOURCE CONTROL and 8350A rear panel PROGRAMMING CONNECTOR.

Furnished: 2.29m (7.5 foot) power cable with NEMA plug; spare fuses; two extender boards for servicing; 1.0m (3.3 foot) HP-IB cable.

Operating Temperature Range: 0°C to +55°C.

Power: 100, 120, 220, or 240 volts, +5% −10%, 50 to 60 Hz (Option 400; 60 to 400 Hz). Approximately 270 volt-amps including RF plug-in unit (depends upon specific RF plug-in unit used).

Weight (not including RF plug-in unit): Net 16.5 kg (36.4 lb) Shipping 22.7 kg (50 lb).

Dimensions: 425 W, 133.3 H, 422 mm D (16.75 x 5.25 x 16.6 in).

1-7. SPECIFICATIONS

1-8. Listed in Table 1-1 are the specifications for the Model 8350A Sweep Oscillator. These specifications are the performance standards, or limits, against which the instrument may be tested. Only the specifications for the Model 8350A Sweep Oscillator mainframe are given in this manual. Refer to the Operating and Service Manual for the specific RF plug-in used for complete specifications relating to the RF plug-in. Table 1-2 lists the sweep oscillator supplemental characteristics. Supplemental characteristics are not specifications but are typical characteristics included as additional information for the user.

1-9. SAFETY CONSIDERATIONS

1-10. General

1-11. This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been manufactured and tested in accordance with international safety standards.

1-12. Safety Symbols

1-13. A complete listing of the safety symbols used in this manual is given on the page preceding Figure 1-1. Included are descriptions of symbols which refer the operator to the manual from the instrument, Protective Earth Ground, Frame or Chassis Terminals, Warning, and Caution symbols.

1-14. INSTRUMENTS COVERED BY MANUAL

1-15. Attached to the rear panel of the instrument is a serial number plate. A typical serial number plate is shown in Figure 1-2. The serial number is in two parts. The first four digits followed by a letter comprise the serial number prefix. The last five digits form the sequential suffix that is unique to each instrument. The content of this manual applies directly to instruments having the same serial number prefix as those listed on the title page of this manual under SERIAL NUMBER.

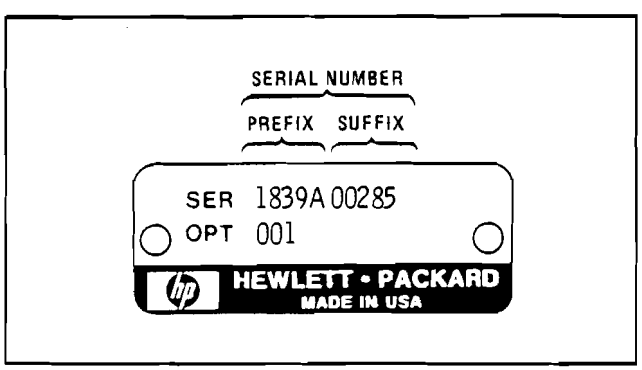


Figure 1-2. Typical Serial Number Plate

1-16. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. An unlisted serial prefix indicates that the instrument is different from those documented in this manual. The manual for the instrument is then supplied with a Manual Changes supplement that contains information that documents the differences.

1-17. In addition to change information, the Manual Changes supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is keyed to the manual's print date and part number, both of which appear on the title page. Complimentary copies of the Manual Changes supplement are available on request from Hewlett-Packard.

1-18. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes Supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-19. DESCRIPTION

1-20. The Hewlett-Packard Model 8350A Sweep Oscillator, together with an RF plug-in unit, forms a complete, solid-state, swept signal source. The Model 8350A can be used with network analyzer systems such as the HP Model 8410B Network Analyzer, the HP Model 8755 Frequency Response Test Set, and the HP Microwave Link Analyzers to provide a complete measurement system.

1-21. The front panel of the Model 8350A has been conveniently laid out to optimize the use of instrument operation function blocks. Frequency modes, sweep modes, marker operation, storage register control, and data entry controls are individually grouped for ease of operation and full control versatility on the Model 8350A Sweep Oscillator.

1-22. Upon initial turn on, or after the INSTRument PRESET pushbutton is selected, the instrument automatically goes through an internal self check routine to verify proper instrument operation. If certain errors or failures are detected during the self test or in normal operation, they are indicated via error codes displayed on the far left digital display. An INSTRument PRESET condition is then set which automatically presets the sweep oscillator to full RF plug-in band sweep operation.

1-23. Accurate High Resolution Data Entry

1-24. Accurate, high resolution digital displays indicate all major function values. Function values may be set by activating the appropriate pushbutton and using the corresponding knob, step keys, or data entry keyboard to enter the desired values.

1-25. Sweep and Trigger Modes

1-26. The sweep may be triggered INTernally, through ac power LINE frequency, EXTernally, or in SINGLE sweep operation. SWEEP TIME is continuously variable from 10 ms to 100 seconds. (Minimum sweep time may be greater than 10 ms depending upon the specific RF plug-in used and the bandwidth being swept). A MANual SWEEP function allows the data entry controls to provide continuous manual adjustment of frequency between the end frequencies set in any of the sweep functions. A direct coupled sawtooth sweep ramp, zero to approximately 10 volts, is available through both front and rear panel SWEEP OUTPUT/SWEEP INPUT BNC connectors.

1-27. START/STOP Mode

1-28. The START/STOP frequency sweep mode, selected upon Instrument Preset, is indicated by yellow LEDs located above the selected operation pushbuttons. In this mode the Model 8350A sweeps up from the START frequency to the STOP frequency. START and STOP frequencies are indicated on the FREQUENCY LED displays. START frequency or STOP frequency may then be changed through the use of the data entry controls.

1-29. CW Mode

1-30. When CW (Continuous Wave) mode is selected, the instrument is tuned to a single frequency RF Output, indicated on the FREQUENCY LED display. CW mode operation is indicated by the yellow LED located above the CW pushbutton. CW frequency, when enabled, may be varied through the use of the data entry controls. When the SHIFT CW mode is selected, a 0 to 10 volt sweep ramp will be output at the front and rear panel SWEEP OUTPUT/SWEEP INPUT BNC connectors, even though the RF frequency is fixed in the CW mode.

1-31. CF/ΔF Mode

1-32. The CF/ΔF frequency sweep mode allows the instrument to sweep upward in frequency, symmetrically centered about a CF (Center Frequency) setting. CF/ΔF sweep mode operation is indicated by the yellow LEDs centered above the CF and ΔF pushbuttons. CF and ΔF frequencies may be individually varied through use of the data entry controls. START/STOP and CF/ΔF sweep modes may be interchanged without affecting the RF Output. When changing between CF/ΔF sweep mode and CW mode, the CW frequency and the Center Frequency (CF) are equivalent.

1-33. Frequency Marker Operation

1-34. Five independent, continuously variable, amplitude or intensity markers are available to note significant points on the frequency sweep. Marker selection is indicated by a yellow LED located within each Marker pushbutton. Marker frequency is indicated on the FREQUENCY/TIME LED display. The frequency difference between any two markers can be displayed by the MKRΔ function. A MARKER SWEEP function allows a frequency sweep using Marker 1 and Marker 2 as the START/STOP frequency limits while maintaining the original START/STOP values. For greater accuracy, marker frequencies can also be counted directly using the HP Model 5343A Microwave Frequency Counter. The sweep is momentarily stopped allowing the counter to measure the START, STOP, or activated marker frequency.

1-35. Instrument State Storage

1-36. Up to 9 different front panel settings can be stored and recalled in the Model 8350A via the SAVE n (n=1 through 9) function. The ALT n function causes the RF Output to alternate on successive sweeps between the current front panel setting and the setting stored in the recalled memory location (n=1 through 9). This allows the

Model 8350A to work in conjunction with the HP Model 8755 Frequency Response Test Set to allow two different measurements to be made simultaneously by utilizing two different sweep widths and/or power levels.

1-37. Modulation Characteristics

1-38. The Model 8350A is capable of internally square wave modulating the RF Output at a 27.8 kHz or 1 kHz (selected by an internal jumper) modulation frequency, as controlled by the front panel Square Wave Modulation pushbutton. The RF Output may also be AM or FM modulated by an external source via the Model 8350A Sweep Oscillator rear panel inputs.

1-39. Remote Programming (HP-IB)

1-40. All front panel controls, except the line power switch, may be controlled or programmed remotely via the rear panel HP-IB interface connector. The Model 8350A can also output to a controller an instrument state message that completely describes the current instrument status (sweep mode, trigger mode, etc.) and can supply the present numerical value of any function (sweep time, marker frequencies, power levels, START/STOP frequencies, etc.).

1-41. Other Features

1-42. The Model 8350A also provides RF output blanking during sweep retrace and rear panel positive and negative polarity display blanking outputs for retrace and bandswitching points of sweep. A rear panel PEN LIFT output generates a pulse which is coincident in time with the endpoints of the sweep. A COUNTER TRIGGER output and STOP SWEEP input are also available on the rear panel to interface with the HP Model 5343A Microwave Frequency Counter. A 25-pin rear panel Programming Connector provides additional control of and information on the Model 8350A instrument state. A listing of pin configuration and signals on the Programming Connector is given in Figure 2-7. Output signals on the Programming Connector supplement other rear panel output signals such as display and RF blanking, X-Y recorder penlift, and HP Model 8410B and HP Model 5343A interface signals. Input signals on the Programming Connector affect the sweep status, display and RF blanking, penlift outputs, etc.

1-43. To have a complete operating unit, the Model 8350A Sweep Oscillator must be used in conjunction with an RF plug-in unit which operates in the desired frequency range. The HP Model 83500 Series RF Plug-in units have been specifically designed for use with the Model 8350A. With the addition of the Model 11869A RF Plug-in Adapter, the HP Model 86200 Series RF Plug-ins may also be used with the Model 8350A.

1-44. OPTIONS

1-45. Option 001, Nonvolatile Memory

1-46. Option 001 instruments contain a battery pack (inserted in the battery holder with a battery hold down clamp) and a special A3 Microprocessor board. With Option 001 installed, the Model 8350A has a nonvolatile memory which retains the contents of all instrument state storage registers, the current instrument state, and the HP-IB address. When fully charged, the batteries will retain a sufficient charge to hold the memory contents for approximately 20 days. The batteries are charged within the instrument and a full charge is maintained when the instrument LINE switch is ON.

1-47. An Option 001 Battery Kit may be ordered for standard Model 8350A Sweep Oscillators to upgrade them to Option 001 capability by ordering HP Part Number 08350-60013. This kit contains a battery pack, a battery pack hold down clamp, and a special A3 Microprocessor board. All other necessary wiring and hardware connections have been made at the factory on all standard instruments.

1-48. Option 400, 400 Hz AC Power Operation

1-49. The standard Model 8350A requires that the ac power line frequency be 50 to 60 Hz. Option 400 allows the instrument to operate with a 400 Hz ac power line frequency.

1-50. Option 907, Front Handles Kit

1-51. Option 907, HP Part Number 5061-0089, contains a pair of front handles and the necessary hardware for mounting the handles to the Model 8350A. Refer to Section II of this Operating and Service Manual for a detailed description of this kit and instructions for installation.

1-52. Option 908, Rack Mount Kit

1-53. Option 908, HP Part Number 5061-0077, contains a pair of flanges and the necessary hardware to mount the Model 8350A in an equipment rack with 482.6 mm (19 inches) horizontal spacing. Refer to Section II of this Operating and Service Manual for a detatiled description of this kit and instructions for installation.

1-54. Option 909, Rack Mount/Front Handles Kit

1-55. Option 909, HP Part Number 5061-0083, contains one Option 907 Front Handles Kit and one Option 908 Rack Mount Kit (see descriptions in preceding paragraphs). Refer to Section II of this Operating and Service Manual for a detailed description of this kit and instructions for installation.

1-56. Option 910, Extra Operating and Service Manual

1-57. The standard instrument is supplied with one Operating and Service Manual. Each Option 910 provides one additional Operating and Service Manual. To obtain additional Operating and Service Manuals after initial shipment, order by manual part number, listed on the title page and rear cover of this manual.

1-58. ACCESSORIES SUPPLIED

1-59. Figure 1-1 shows the Model 8350A and the accessories supplied. The accessories include:

- One power cable. The power cable supplied depends upon the country of destination. Refer to Section II of this manual for HP Part Number information.
- Two 44-pin printed circuit board extenders. The HP Part Number for each extender is 08350-60031. These boards have keyed slots which allow them to be used in troubleshooting various Model 83500 Series RF Plug-ins as well.
- One Model 10631B HP-IB Cable. Length: 2m (6.6 ft).
- One fuse kit, containing two of each type of fuse used in the Model 8350A. Refer to Section VI of this manual for HP Part Number information regarding individual fuses.

1-60. Additional Accessory Kits (including the 2 extender boards and the fuse pack) can be ordered as HP Part Number 08350-60020.

1-61. EQUIPMENT REQUIRED BUT NOT SUPPLIED

1-62. To have a complete operating sweep oscillator, The Model 8350A Sweep Oscillator must have an RF plug-in unit installed. The HP 83500 Series RF Plug-ins have been specifically designed for use with the Model 8350A. They provide calibrated output power levels, calibrated power sweeps, internal leveling and slope control, and full HP-IB programmability. Economical use of the HP Model 86200 Series RF Pug-ins may be utilized with the Model 8350A with the addition of the HP Model 11869A RF Plug-in Adapter. The Model 11869A mounts at the rear of the Model 86200 Series RF Plug-in and provides the interface for signals and voltages from the Model 8350A to the RF plug-in. All of the Model 8350A standard operating features including HP-IB remote programming are available, however, specific RF plug-in functions (output power level, RF on/off, etc.) cannot be controlled or remotely programmed by the Model 8350A mainframe.

1-63. To use the HP-IB capabilities of the Model 8350A, a computing controller such as the HP 9825 Desktop Computer or the HP 85 Personal Computer is needed.

1-63. EQUIPMENT AVAILABLE

1-64. Service Accessories

1-66. An Accessory Kit is supplied with the Model 8350A, as shown in Figure 1-1. Additional Accessory Kits containing two 44-pin extender boards (HP Part Number 08350-60031, each) and a fuse package (containing two of each fuse used in the Model 8350A) may be obtained by ordering HP Part Number 08350-60020.

1-67. In order to fully service all sections of the RF plug-in, it must be removed from the sweep oscillator mainframe. All electrical connections can be maintained through the use of an RF plug-in extender cable set. The RF Plug-in Interface Connection (J2) is extended by one cable (HP Part

Number 08350-60034) and the Power Supply Interface Connection (J3) is extended by another cable (HP Part Number 08350-60035)

1-68. A Hex Balldriver (HP Part Number 8710-0523) is available to aid in removing the hold down plate hex screws from the front panel when repair is necessary.

1-69. Model 8410B/8411A Network Analyzer

1-70. The Model 8350A Sweep Oscillator is compatible with the HP Model 8410B Network Analyzer system. The combination of the Model 8410B Network Analyzer, the Model 8411A Frequency Convertor, and an appropriate display plug-in forms a phasemeter and a ratiometer for direct phase and amplitude ratio measurement on RF voltages. These measurements can be made on single frequencies and on swept frequencies from 110 MHz to 18 GHz. Several RF plug-in units for the Model 8350A are capable of multi-octive sweeps in this range. The Model 8410B has an Auto-Frequency range mode which gives it the capability of automatically tracking the Model 8350A Sweep Oscillator over octave and multi-octave frequency bands. Two interconnections to the Model 8350A are necessary to ensure that the Model 8410B will phase lock properly. The Model 8410B Source Control Cable (HP 08410-60146) connects the Model 8410B rear panel SOURCE CONTROL connector to the Model 8350A rear panel PROGRAMMING CONNECTOR. Additionally, the sweep oscillator RF plug-in 1V/GHz output connects to the Model 8410B rear panel FREQ REF INPUT. The Model 8410B Source Control Cable connector pins and signals are illustrated in Table 1-3.

1-71. Model 8755 Frequency Response Test Set

1-72. The Model 8350A Sweep Oscillator is compatible with the Model 8755 Frequency Response Test Set for broadband swept scalar measurements. The Model 8350A provides internal 27.8 kHz square wave modulation of the RF output eliminating unnecessary cable connections to the Model 8755 or the use of an external modulator. The Model 8350A can also produce alternate sweeps through use of the ALT n function which works in conjuction with the channel switching circuits in the Model 8755C. This permits Channel 1 on the Model 8755C to respond only to the Model 8350A current state and Channel 2 to the alternate state. A single cable (HP Part Number 8120-3174) connects between the Model 8350A rear panel ALT SWP INTERFACE connector and the Model 8755C front panel ALT SWP INTERFACE connector.

1-73. Power Meters and Crystal Detectors

1-74. Depending upon the RF plug-in unit used, the RF output can be externally leveled using the HP Model 432 Power Meter or negative polarity output crystal detectors. Refer to the Operating and Service Manual of the specific RF plug-in used for detailed information on leveling systems that may be used with the Model 8350A/RF Plug-in combination.

NOTE

The Model 435A and 436A Power Meters should not be used in Model 8350A external leveling systems.

Table 1-3. Model 8410B Source Control Cable

8410B Source Control Cable - HP Part Number 08410-60146				
Mnemonic	**Description**	**8350A Connector Pin (25-pin D Type Male HP Part No. 1251-0063)**	**8410B Connector Pin (14-pin Micro Ribbon Male HP Part No. 1251-0142)**	**Wire Color Code**
L SSRQ	Low = Stop Sweep Request	18	7	905
SYNC TRG	High = Synchronizing Trigger	24	1	901
GND DIG	Digital Ground	19	11	90

Table 1-4. Recommended Test Equipment[1] (1 of 4)

Instrument	Critical Specifications	Recommended Model	Use[2]
Spectrum Analyzer	Frequency Range: 0.01 to 22 GHz Residual FM: ≤100 Hz Must have auxiliary IF output when used with the HP 8901A Modulation Analyzer.	HP 8565A	P,T
Oscilloscope	Dual channel X vs. Y display mode Sensitivity: ≤0.1 μS/DIV Horizontal Sweep Rate: ≤0.1 μS/DIV	HP 1740A	P
Display Mainframe	Compatible with HP 8755C Swept Amplitude Analyzer and HP 8750A Storage-Normalizer	HP 182T, 180TR	P
Swept Amplitude Analyzer	Capable of transmission measurements Power Resolution: ≤0.25 dB/DIV	HP 8755C	P
Detector	Compatible with Swept Amplitude Analyzer Frequency Range: 0.01 to 12.4 GHz Power Range: −20 to +10 dBm	HP 11664A	P
Power Splitter	Frequency Range: 0.01 to 12.4 GHz Output Port Tracking: ≤0.25 dB Maximum Input Power: ≥+20 dBm	HP 11667A	P
Storage-Normalizer	Compatible with Display Mainframe and Swept Amplitude Analyzer	HP 8750A	P
Digital Voltmeter	Accuracy: ≤0.005% Input Impedance: ≥10 MΩ	HP 3455A	A,T
Universal Counter	Frequency Mode Frequency Range: ≥30 kHz Frequency Resolution: ≤10 Hz Time Period Mode Frequency Range: ≥20 kHz Resolution: ≤50 μS	HP 5328A	A
Oscilloscope Probe	1 : 1 General Purpose Probe	HP 10008B	A
Modulation Analyzer	(May be used in addition to Spectrum Analyzer) Frequency Range: Must cover auxiliary IF Output frequency of Spectrum Analyzer used Residual FM: ≤10 Hz	HP 8901A	P
Power Meter	Power Range: −20 to +10 dBm (No substitution when used for external power meter leveling).	HP 432A	P

Table 1-4. Recommended Test Equipment[1] (2 of 4)

Instrument	Critical Specifications	Recommended Model	Use[2]
Thermistor Sensor	Frequency Range: 0.01 to 12.4 GHz Maximum SWR: ≤1.75	HP 8478B	P
Frequency Counter	Frequency Range: 0.01 to 12.4 GHz Sensitivity: ≤−20 dBm Maximum Input Power: ≥0 dBm Frequency Accuracy: ≤1 kHz	HP 5343A	P
Directional Coupler	Frequency Range: 0.1 to 2.0 GHz Nominal Coupling: ≥20 dB Maximum Coupling Variation: ≤±1 dB Minimum Directivity: ≥32 db	HP 778D	P
Directional Coupler	Frequency Range: 2 to 12.4 GHz Mean Output Coupling: ≥20 dB Output Coupling Variation: ≤±1 dB Minimum Directivity: ≥26 dB	HP 779D	P
RMS Voltmeter	dB Range: −20 to −70 dBm (0 dBm = 1 mW into 600 Ohms) Frequency Range: 10 Hz to 10 MHz Accuracy: ±5% of full scale	HP 3400A	P
Function Generator	Frequency Range: 0.1 Hz to 10 MHz Output Level: 10V p-p into 50 Ohms Output Level Flatness: ≤±3% from 10 Hz to 100 kHz ≤±10% from 100 kHz to 10 MHz	HP 3312A	P,T
Crystal Detector	Frequency Response: 0.01 to 12.4 GHz Maximum Input Power: ≥100 mW	HP 423B	P
Air Line Extension (2 required)	Impedance: 50 Ohms Frequency Range: dc to 12.4 GHz Reflection Coefficient: 0.018 + 0.001 (times the frequency in GHz)	HP 11567A	P
RF Cable	Refer to Table 4-3	HP 11770B	P
Step Attenuator	Frequency Range: dc to 12.4 GHz Incremental Attenuation: 0 to 70 dB in 10 dB steps Calibration Accuracy: ≤±0.1 dB at all steps	HP 8495A Option 890	P

Table 1-4. Recommended Test Equipment[1] (3 of 4)

Instrument	Critical Specifications	Recommended Model	Use[2]
Attenuator	Attenuation: 3 dB ± 0.5 dB Frequency Range: 0.01 to 12.4 GHz Maximum Input Power: ≥+20 dBm	HP 8491B Option 003	P
Attenuator	Attenuation: 6 dB ± 0.5 dB Frequency Range: 0.01 to 12.4 GHz Maximum Input Power: ≥+20 dBm	HP 8491B Option 006	P
Attenuator	Attenuation: 10 ± 0.5 dB Frequency Range: 0.01 to 12.4 GHz Maximum Input Power: ≥+20 dBm	HP 8491B Option 010	P
Attenuator	Attenuation: 20 ± 0.5 dB Frequency Range: 0.01 to 12.4 GHz Maximum Input Power: ≥+20 dBm	HP 8491B Option 020	P
Adjustable Short	Frequency Range: 1.8 to 12.4 GHz Impedance: 50 ± 1.5 Ohms	Maury Microwave[3] 1953-2	P
Adjustable AC Line Transformer	Select to cover line voltage used 100—120 volt	General Radio[4] W5MTB	P
	220—240 volt	General Radio W10HM73	P
Line Voltage Monitor	To be used with above Adjustable AC Line Transformers		
	120 volt Monitor	RCA[5]120B	P
	240 volt Monitor	RCA WV 503A	P
Frequency Meters	Frequency Accuracy: ≤0.17% Calibration Increments: ≤2 MHz Select to cover Frequency range of RF plug-in		
	0.96 to 4.2 GHz	HP 536A	P
	3.7 to 12.4 GHz	HP 537A	P
Adapter	APC-7 to Type N(m)	HP 11525A	P
Adapter	APC-3.5(f) to Type N(m)	Amphenol[6] 131-7018	P
Delay Line Discriminator	Refer to Figure 1-3		P

Table 1-4. Recommended Test Equipment[1] (4 of 4)

Instrument	Critical Specifications	Recommended Model	Use[2]
PC Board Extender[7]	44-pin, extends printed circuit boards	HP Part Number 08350-60031 (each)	T
RF Plug-in Extender Cable	Extends RF Plug-in Interface Connector (J2)	HP Part Number 08350-60034	T
RF Plug-in Extender Cable	Extends RF Plug-in Power Supply Interface Connector (J3)	HP Part Number 08350-60035	T

[1]Refer to the Recommended Test Equipment list in the Operating and Service Manual of the RF plug-in used for a listing of equipment specifically relating to the RF plug-in used. Not all equipment included in this list is necessary for all RF plug-ins.

[2]P=Performance Test; A=Adjustments; T=Troubleshooting

[3]Mauray Microwave Corp., 8610 Helms Ave., Cucamonga, CA 91730

[4]General Radio, 300 Baker Avenue., Concord, MA 01742

[5]RCA Distribution & Special Products Div., Dept. EM, New Holland Ave., Lancaster, PA 17604

[6]Amphenol North America, Bunker-Ramo Corp., RF Operations, 33 E. Franklin St., Danbury, CT 06810

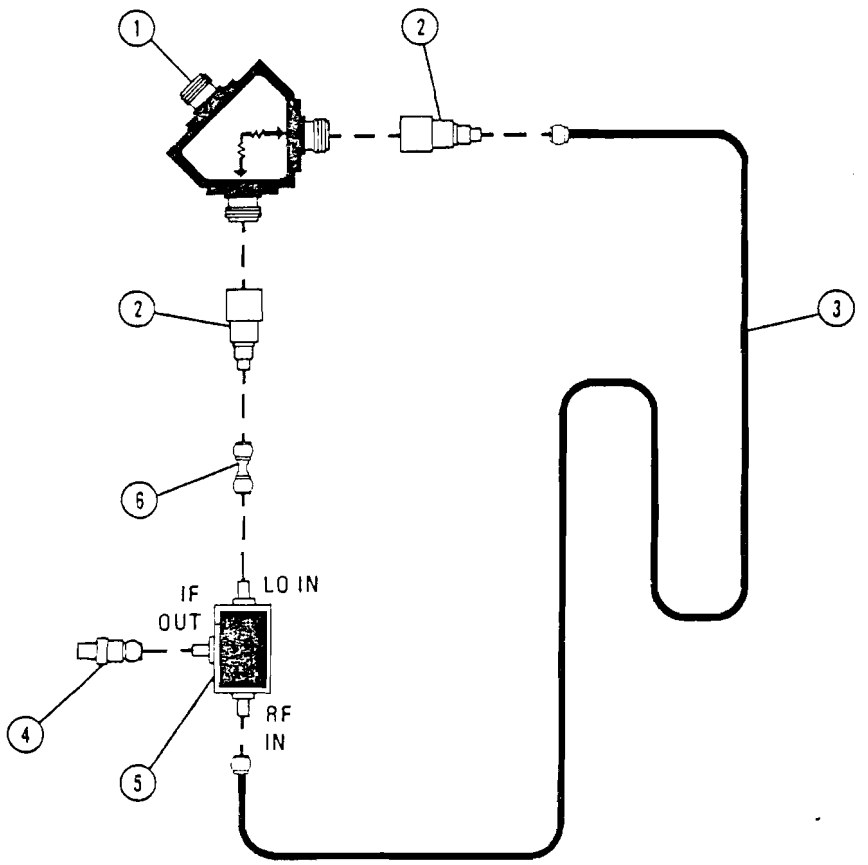
[7]Two 44-pin printed circuit board extenders and a fuse kit are included with the Model 8350A Accessory Kit Supplied (HP Part Number 08350-60020). Refer to Figure 1-1 in this manual.

1-75. RECOMMENDED TEST EQUIPMENT

1-76. Equipment required for testing and adjustment of the instrument is listed in Table 1-4. Other equipment may be substituted if it meets or exceeds the critical specifications indicated in the table.

1-77. HEWLETT-PACKARD INTERFACE BUS. (HP-IB)

1-78. The Model 8350A is factory equipped with a remote programming interface using the Hewlett-Packard Interface Bus (HP-IB). This provides a remote operator with the same control of the instrument available to a manual (local) operator. Remote control is maintained by a system controller (desktop computor, computor, etc.) that sends commands or instructions to and receives data from the Model 8350A using the HP-IB. The HP-IB is Hewlett-Packards implementation of the IEEE Standard 488-1978. A complete general description of the HP-IB is provided in the manual entitled "Condensed Description of the Hewlett-Packard Interface Bus" (HP Part Number 59401-90030.



Item	Description	HP Part Number
1	Power Splitter	HP 11667A
2	Adapter: Type N Male to SMA Female (2 required)	1250-1250
3	Delay Line: >3 feet in length, SMA male connectors	08503-20038
4	Adapter: BNC Female to Male SMA	1250-1200
5	Mixer: Double Balanced 1 to 12 GHz: RHG Electronics Part No. DM 1-12 1 to 18 GHz: RHG Electronics Part No. DM 1-18 RHG Electronics Laboratories, Inc. Deer Park, NY 11729	 0960-0451 None
6	Adapter: SMA Male to SMA Male	1250-1159

Figure 1-3. Delay Line Discriminator

SECTION II
INSTALLATION

2-1. INTRODUCTION

2-2. This section provides installation instructions for the Model 8350A Sweep Oscillator and its acccessories. This section also includes information about initial inspection and damage claims, preparation for use, and packaging, storage, and shipment.

2-3. INITIAL INSPECTION

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as shown in Figure 1-1. Procedures for checking electrical performance are given in Section IV, Performance Tests, of this manual. If the instrument combination does not pass the electrical Performance Tests, refer to Section V, Adjustments, of this manual. If, after the adjustments have been made, the instrument combination still fails to meet specifications, refer to Section V, Adjustments, of the Operating and Service Manual for the RF plug-in being used. If a circuit malfunction is suspected, refer to troubleshooting procedures in Section VIII, Service, of this or the RF plug-in manual. If the instrument does not pass the above electrical tests, if the shipment contents are incomplete, or if there is mechanical damage or defect, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement without waiting for claim settlement.

2-5. PREPARATION FOR USE

2-6. Power Requirements

2-7. The Model 8350A Sweep Oscillator requires a power source of 100, 120, 220, or 240 Vac, +5% to −10%, 50 to 60 Hz, single-phase (50 to 400 Hz, single-phase for Option 400 instruments). Power consumption is approximately 270 volt-amps, depending upon the specific RF plug-in unit used.

2-8. Line Voltage and Fuse Selection

2-9. Figure 2-1 illustrates the line voltage selection card and fuse location in the Power Line Module on the rear panel of the Model 8350A. Select the line voltage and fuse as follows:

a. Measure the ac line voltage.

b. Refer to Figure 2-1. At the instrument rear panel power line module, select the line voltage (100, 120, 200, or 220 volts) closest to the voltage you measured in step a. Note the available line voltage must be within +5% or −10% of the line voltage selection as shown in Table 2-1. If it is not, you must use an autotransformer between the power source and the Model 8350A.

Table 2-1. Line Voltage/Fuse Selection

Measured ac Line Voltage	PC Selector Board Position	Fuse/ HP Part Number
90 to 105 volts	100	4.0A 2110-0055
108 to 126 volts	120	4.0A 2110-0055
198 to 231 volts	220	2.0A 2110-0002
216 to 252 volts	240	2.0A 2110-0002

c. Make sure the correct fuse is installed in the fuse holder. The required fuse rating for each line voltage is indicated in Table 2-1 and below the power line module on the rear panel of the Model 8350A.

CAUTION

To prevent damage to the instrument, make the correct line voltage and fuse selection before connecting line power to the instrument.

2-10. Power Cable

2-11. In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate power line outlet, this cable grounds the instrument cabinet. Table 2-2 shows the styles of plugs available on power cables supplied with HP instruments. The HP Part Numbers for the plugs are part numbers for the complete power cables. The type of power cable/plug shipped with the instrument depends upon the country of destination.

WARNING

Before switching on this instrument, be sure that only the specified power cable is used. The instrument is provided with a three-wire power cord which grounds the instrument cabinet. This power cord should only be inserted in a socket outlet provided with a protective earth contact. This protective action should not be negated by the use of an extension cord (power cable) without a protective conductor (ground). Grounding one conductor of a two-conductor outlet is not sufficient protection.

2-12. The offset pin of the three-prong connector is the grounding pin. When operating the Model 8350A from a two-contact outlet, the protective grounding feature may be preserved by using a three-prong to two-prong adapter (USA connectors only, HP Part Number 1251-0048) and connecting the green wire of the adapter to ground.

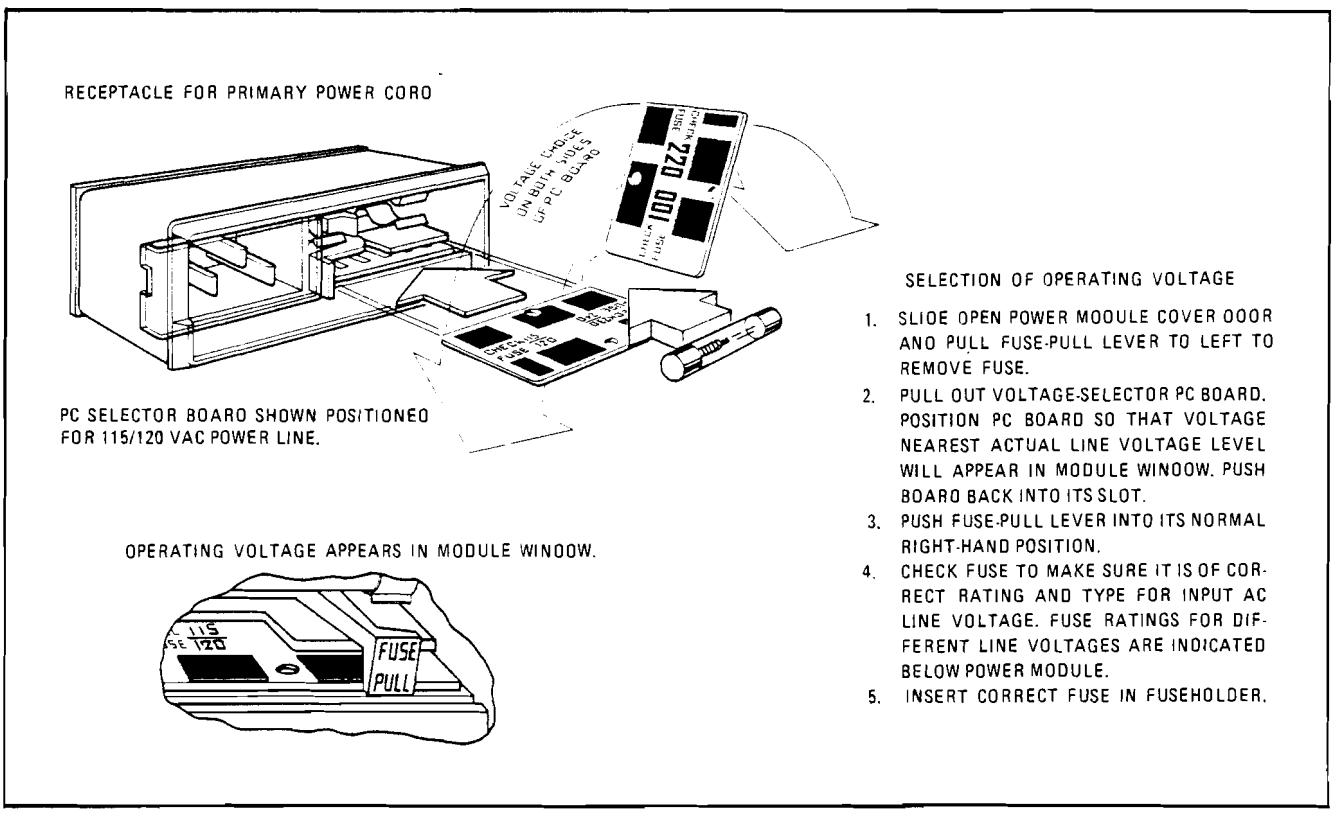
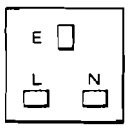
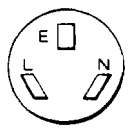
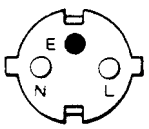
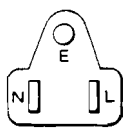
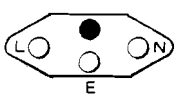
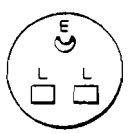
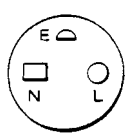
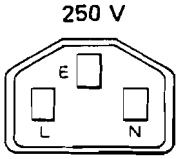


Figure 2-1. Power Line Module

Table 2-2. AC Power Cables Available

Plug Type	Cable HP Part Number	C D	Plug Description	Cable Length (inches)	Cable Color	For Use In Country
250V 	8120-1351 8120-1703	0 6	Straight*BS1363A 90°	90 90	Mint Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Rhodesia, Singapore
250V 	8120-1369 8120-0696	0 4	Straight*NZSS198/ASC112 90°	79 87	Gray Gray	Austrailia, New Zealand
250V 	8120-1689 8120-1692	7 2	Straight*CEE7-Y11 90°	79 79	Mint Gray Mint Gray	East and West Europe, Saudi Arabia, Egypt So. Africa, India (unpolarized in many nations)
125V 	8120-1348 8120-1398 8120-1754 8120-1378 8120-1521 8120-1676	5 5 7 1 6 2	Straight*NEMA5-15P 90° Straight*NEMA5-15P Straight*NEMA5-15P 90° Straight*NEMA5-15P	80 80 36 80 80 36	Black Black Black Jade Gray Jade Gray Jade Gray	United States, Canada, Japan (100V or 200V), Mexico, Philippines, Taiwan
250V 	8120-2104	3	Straight*SEV1011 1959-24507 Type 12	79	Gray	Switzerland
250V 	8120-0698	6	Straight*NEMA6-15P			United States, Canada
220V 	8120-1957 8120-2956	2 3	Straight*DHCK 107 90°	79 79	Gray Gray	Denmark
250 V 	8120-1860	6	Straight*CEE22-VI (Systems Cabinet use)			

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug.
E = Earth Ground; L = Line; N = Neutral

2-13. HP-IB Address Selection

WARNING

The HP-IB address switch is set with the top cover removed from the Model 8350A. Prior to setting the HP-IB address switch, the LINE switch should be set to OFF and the power cord should be disconnected from the ac power source for maximum safety. Capacitors inside the instrument may still be charged even when the instrument is disconnected from its ac power source. Use caution when setting the HP-IB address switch to avoid touching assemblies or components within the instrument other than the HP-IB address switch.

2-14. When the Model 8350A is used under remote control with the HP-IB, the controller on the bus refers to the Model 8350A by an HP-IB "address". The Model 8350A is differentiated from any other instrument on the bus by its own unique address. This HP-IB address is initially preset in the Model 8350A by a 5-segment address switch A8S1, located on the A8 HP-IB Interface assembly, as shown in Figure 2-2. A diagram of A8S1 is given in Figure 2-3. Each of the 5 switches corresponds to one of the digits of the 5-digit binary equivalent of the address, as shown in Table 2-3. A8S1 switch A1 corresponds to the Least Significant Bit (LSB) of the binary address and switch A5 corresponds to the Most Significant Bit. The HP-IB address can be modified by a front panel SHIFT function.

2-15. Thirty-one different address codes are available (decimal 0 to 30). The Model 8350A is shipped from the factory preset to binary address "10011" (decimal 19), as shown in Figure 2-3. In all standard Model 8350A instruments, the HP-IB address will be read by the processor from the HP-IB address switch A8S1 upon initial power on only. This HP-IB address will remain in effect until the address is changed by modifying the A8S1 switch pattern (and turning the LINE switch OFF and ON) or by resetting the address through the front panel SHIFT LOCAL function. The HP-IB address can be read directly from the front panel by pressing SHIFT LCL. The current HP-IB address is then displayed in decimal form on the FREQUENCY/TIME display. If the HP-IB

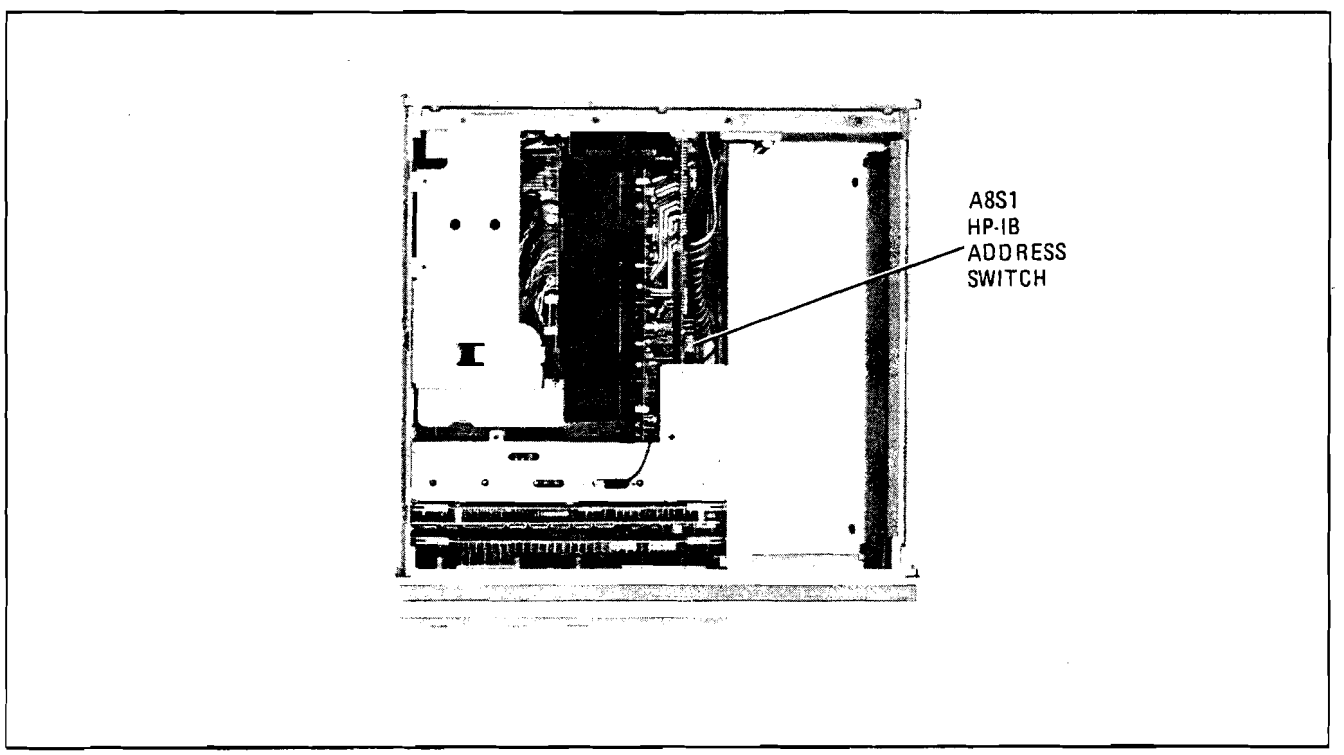


Figure 2-2. Location of A8S1 HP-IB Address Switch

address must be changed from that which is displayed, enter the new decimal equivalent of the desired HP-IB address and press GHz to terminate the entry. The FREQUENCY/TIME display should now display the new HP-IB address. This address will remain in effect until the Model 8350A LINE switch is turned OFF. When the instrument LINE switch is set to ON once again, the HP-IB address will revert back to the A8S1 address switch setting. An INSTRUMENT PRESET command will not modify the current HP-IB address setting.

2-16. Option 001 Model 8350A instruments contain a battery supported memory and a special A3 Microprocessor board. The battery option allows the instrument memory to retain the assigned HP-IB address when the instrument is turned off, regardless of the A8S1 address switch setting. Upon initial power on, the HP-IB address will need to be set to the desired code through the front panel SHIFT LOCAL function. The address will be retained as long as the battery is charged to a sufficient level. Refer to the Battery Operation (Option 001) paragraph in this section of the manual further information on Option 001 instruments.

2-17. HP-IB address labels are available by ordering HP Part Number 7120-6835 (each). (See Figure 2-4). These labels allow easy reference to the HP-IB address of each system component.

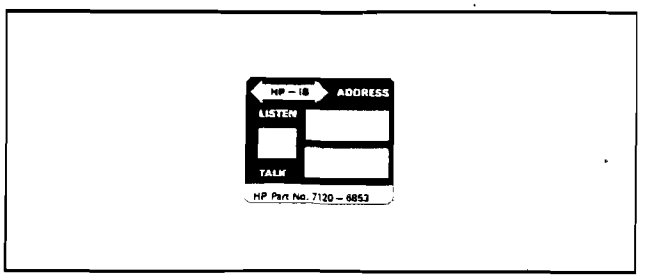


Figure 2-4. HP-IB Address Label

2-18. 11869A Switch Settings for HP 86200 Series RF Plug-ins

2-19. The identification switch on the Model

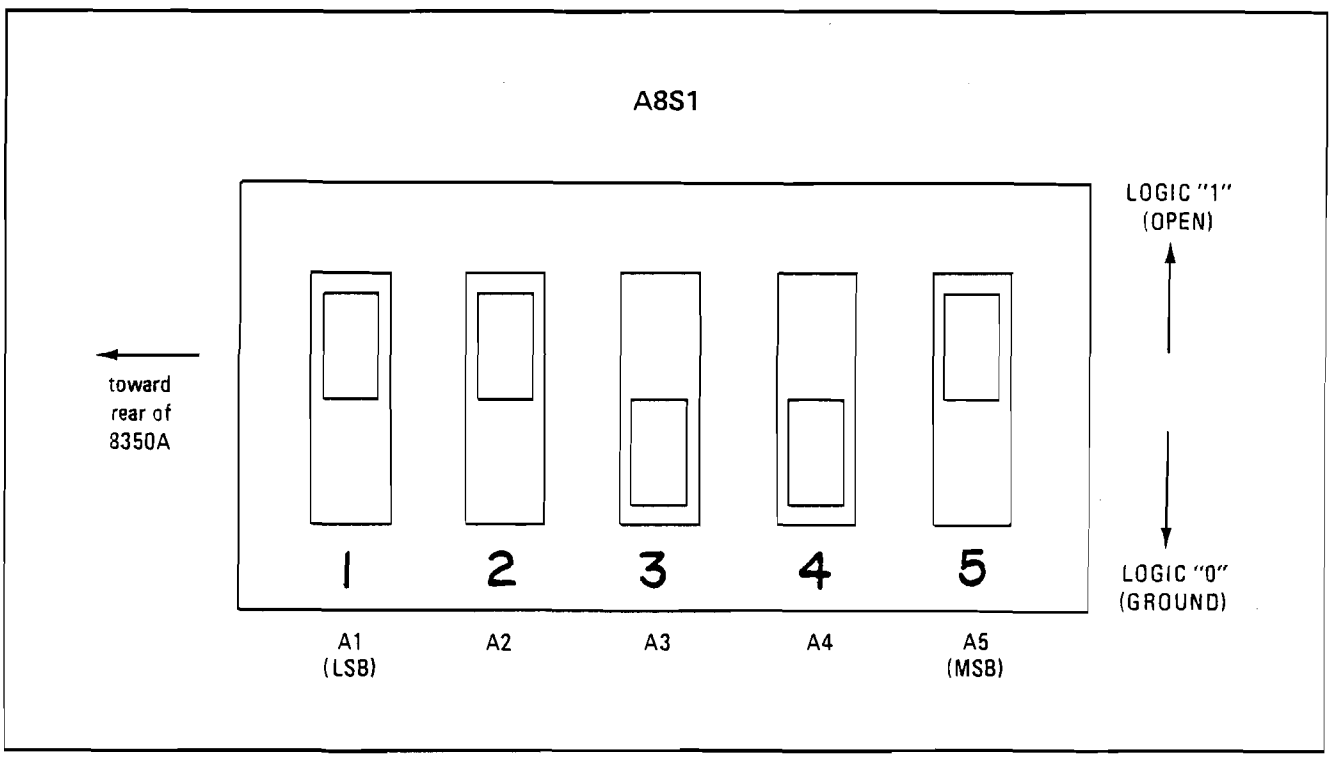


Figure 2-3. A8S1 HP-IB Address Switch

Table 2-3. HP-IB Address Codes

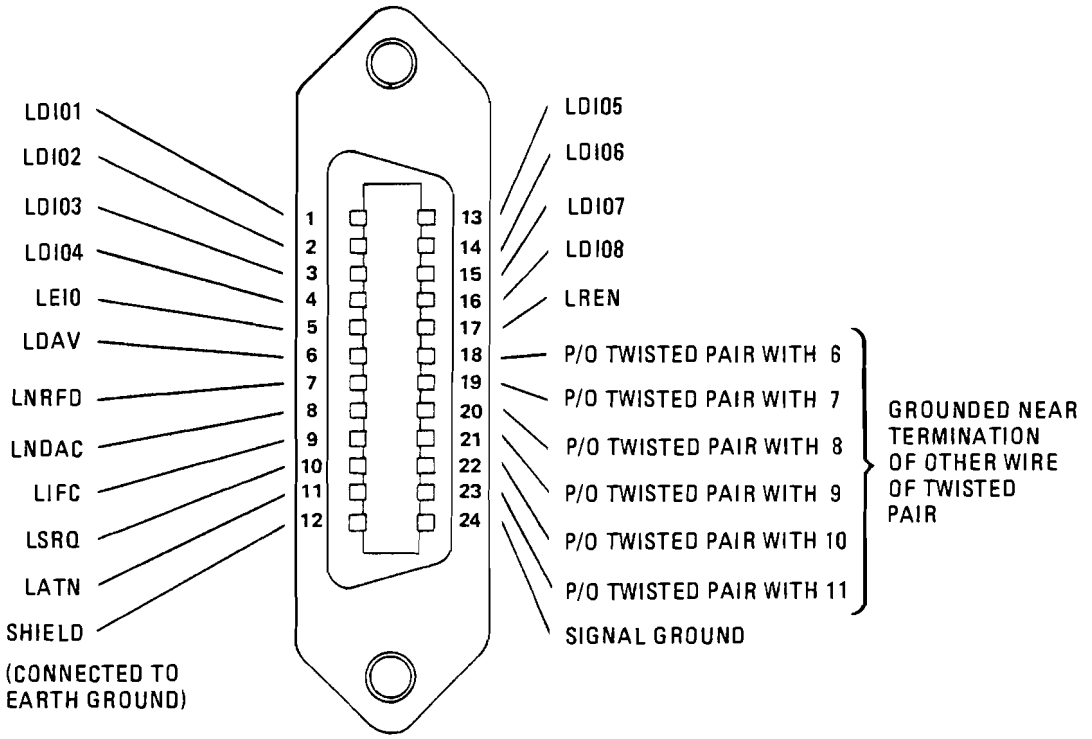
Address Characters		A8S1 Address Switch Settings					Address
Listen	Talk	(MSB) A5	A4	A3	A2	(LSB) A1	Decimal Equivalent
SP	@	0	0	0	0	0	0
!	A	0	0	0	0	1	1
"	B	0	0	0	1	0	1
#	C	0	0	0	1	1	3
$	D	0	0	1	0	0	4
%	E	0	0	1	0	1	5
&	F	0	0	1	1	0	6
'	G	0	0	1	1	1	7
(	H	0	1	0	0	0	8
)	I	0	1	0	0	1	9
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
-	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	2	0	0	0	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	1	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

11869 RF Plug-in Adapter must be preset when using the adapter with HP 86200 Series RF Plug-ins in the Model 8350A. The setting of the identification switch is interrogated at power on, when the 8350A INSTR PRESET button is pressed, or when an HP-IB Instrument Preset ("IP") command is received. If the identification switch is set incorrectly, the START/STOP frequencies will be in error. Refer to Section II, Installation, of the Model 11869A Operating and Service Manual for instructions to properly set the identification switch.

2-20. Internal Square Wave Modulation Frequency Selection

2-21. Internal square wave modulation is available at all sweep speeds on the Model 8350A. Internal square wave modulation is selected by the front panel ⊔⊓ MOD pushbutton. Modulation frequency is selectable by an internal jumper to be either 27.8 kHz (preset at the factory for use with Model 8755 Swept Amplitude Analyzer systems) or 1 kHz. Refer to Section V Adjustments in this manual for detailed infor-

HP-IB CONNECTOR J4
(as viewed from rear of instrument)



HP-IB Logic Levels:
True (low) State ≤0.8 Vdc; False (high) State ≥+2.4 Vdc.

MNEMONICS TABLE

Mnemonic	Description
L ATN	LOW = Attention control line
L DAV	LOW = Data Valid Control line
L DIO1 thru 8	LOW = Data Input/Output lines
L EOI	LOW = End Or Identify control line
L IFC	LOW = Interface Clear control line
L NDAC	LOW = Data Not Accepted control line
L NRFD	LOW = Not Ready For Data control line
L REN	LOW = Remote Enable control line
L SRQ	LOW = Service Request control line

Figure 2-5. HP-IB Connector Signals and Pin Configuration

mation on how to select and adjust the internal square wave modulation frequency.

2-22. RF Plug-in Configuration Switch

2-23. Each RF plug-in may have a configuration switch which must be preset prior to operation in the Model 8350A. This is a multiple switch with individual switches that correspond to various RF plug-in functions such as FM sensitivity selection, FM modulation input coupling selection (direct coupled or cross-over), RF power level at instrument power on, and Option 002 Step Attenuator operation. Refer to the Operating and Service Manual of the specific RF plug-in used for detailed information on the configuration switch.

2-24. Interconnections

2-25. There are two RF plug-in interconnections on the Model 8350A Sweep Oscillator mainframe. These are the RF Plug-in Interface Connector (J2) and the Power Supply Interface Connector (J3). J2 and J3 are visible at the rear of the RF plug-in channel. A complete listing of pins and the associated signals and voltages for these connectors are listed on the overall instrument Wiring List in Section VIII, Service, of this manual.

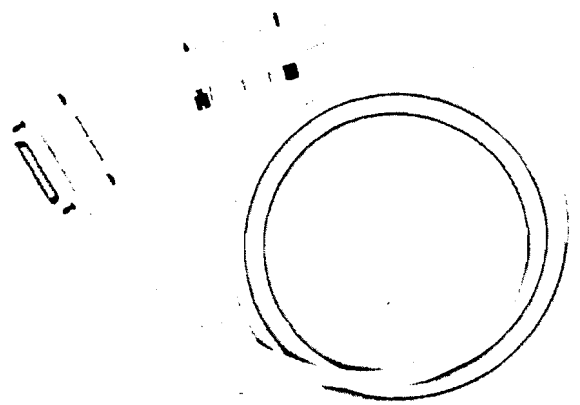
2-26. Mating Connectors

2-27. All of the externally mounted connectors on the Model 8350A are listed in Table 2-4. Opposite each mainframe connector is an industry identification, the HP part number of a mating connector, and the part number of an alternate source for the mating connector. For HP part numbers of the externally mounted connectors themselves, refer to Section VI, Replaceable Parts, of this manual.

2-28. HP-IB Interface Connector and Cables

2-29. The HP-IB Interface Connector J4, located on the rear panel of the Model 8350A, allows the sweep oscillator to be connected to any other device on the HP-IB Interface Bus. A complete illustration of pin configuration and signals on the HP-IB Interface connector is given in Figure 2-5.

2-30. All instruments on the HP-IB Interface Bus are interconnected by HP-IB Interface Cables. One Model 10631B HP-IB Interface Cable is supplied with the Model 8350A. A list of the available HP-IB Interface Cables and their part numbers is given in Figure 2-6. As many as 15 instruments can be connected in parallel on the HP-IB Interface Bus. To achieve design performance on the bus, proper voltage levels and timing relationships must be maintained. If the system cable is too long or if the accumulated cable length between instruments is too long, the data and control lines cannot be driven properly and the system may fail to perform. Therefore, the following restrictions must be observed:



HP-IB Cable Part Numbers	Lengths
HP 10631A	1 m (3.3 ft.)
HP 10631B	2 m (6.6 ft.)
HP 10631C	4 m (13.2ft.)
HP 10631D	0.5 m (1.6 ft.)

Figure 2-6. HP-IB Interface Cables Available

Table 2-4. Model 8350A Mating Connectors

8350A Connector		Mating Connector	
Connector Name	**Industry Identification**	**HP Part Number**	**Alternate Source**
J1 SWEEP OUTPUT/ SWEEP INPUT (front panel)	BNC	1251-0256	Specialty Connector 25-P118-1
J4 HP-IB INTERFACE BUS*	24-Pin Micro Ribbon	1251-0293	Amphenol 57-30240
J5 POS Z BLANK	BNC	1250-0256	Specialty Connector 25-P118-1
J6 NEG Z BLANK	BNC	1250-0256	Specialty Connector 25-P118-1
J7 PEN LIFT	BNC	1250-0256	Specialty Connector 25-P118-1
J8 SWEEP OUT/IN (rear panel)	BNC	1250-0256	Speciality Connector 25-P118-1
J9 CNTR TRIG	BNC	1250-0256	Specialty Connector 25-P118-1
J10 STOP SWEEP	BNC	1250-0256	Specialty Connector 25-P118-1
J11 FM INPUT	BNC	1250-0256	Specialty Connector 25-P118-1
J12 AM INPUT	BNC	1250-0256	Specialty Connector 25-P118-1
J13 PROGRAMMING CONNECTOR	25-Pin D Series	1251-0063	ITT Cannon DBM-25P
J14 ALT SWP INTERFACE**	Audio 3-Pin Connector	no HP Part Number	Switchcraft TA-3F

*Refer to Figure 2-6 for HP-IB Interface Cable information. HP-IB Interface connector J4 signals and pin configuration are given in Figure 2-5.

** A 1219 mm (48") cable assembly with a Switchcraft TA-3F Audio 3-Pin connector on each end is supplied with the Model 8755C Swept Amplitude Analyzer as the Alternate Sweep Interface Cable. The complete cable may be ordered separately as HP Part Number 8120-3174.

a. With two instruments in a system, the cable length must not exceed 4 meters (12 feet).

b. When more than two instruments are connected on the bus, the cable length to each instrument must not exceed 2 meters (6 feet) per unit.

c. The total cable length between all units cannot exceed 20 meters (65 feet).

2-31. Programming Connector

2-32. The Programming Connector J13 on the rear panel of the Model 8350A provides digital control of display functions and sweep oscillator Step Up control. Figure 2-7 gives a description of all pins and signals available on the Programming Connector. When the Model 8410B/8411A Network Analyzer is used with the Model 8350A, the Model 8410B Source Control Cable (HP Part Number 08410–60146) connects the Model 8410B rear panel SOURCE CONTROL and the Model 8350A rear panel PROGRAMMING CONNECTOR. Additionally, the sweep oscillator RF plug-in 1V/GHz output connects to the Model 8410B rear panel FREQ REF INPUT to insure that the Model 8410B phase locks with the sweep oscillator properly when sweeping octave or multi-octave bands. The Model 8410B Source Control Cable connector pins and signals are illustrated in Table 1-3 of this manual.

2-33. Operating Environment

2-34. Temperature. The instrument may be operated in temperatures from 0°C to +55°C.

2-35. Humidity. The instrument may be operated in environments with humidity from 5% to 80% relative at +25°C to +40°C. However, the instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-36. Altitude. The instrument may be operated at altitudes up to 4572 meters (approximately 15,000 feet).

2-37. Cooling. Clearances for ventilation should be at least 10 cm (4 inches) at the rear of the cabinet and 7.6 cm (3 inches) at the sides. The clearances provided by the plastic feet in bench stacking and the filler strips in rack mounting are adequate for the top and bottom cabinet surfaces. A diagram illustrating the path for cooling airflow generated by the rear panel fan is given in Figure 2-8. Insure that the air intake and exhaust venting holes are not obstructed within the limits shown in Figure 2-8.

2-38. Installation Instructions

2-39. To operate as a completely functional sweep oscillator, the Model 8350A Sweep Oscillator must have an RF plug-in unit installed. To install an HP 86200 Series RF plug-in (coupled to a Model 11869A RF Plug-in Adapter) in the Model 8350A, refer to Section II, Installation, in the Model 11869A Operating and Service Manual. To install an HP 83500 Series RF plug-in unit into the Model 8350A mainframe:

a. Set the Model 8350A mainframe LINE switch to OFF.

b. Remove all connectors and accessories from the front and rear panel connectors to prevent them from being damaged.

c. Position the RF plug-in unit latching handle in the fully raised position. The latching handle should spring easily into the raised position and be held by spring tension.

d. Insure that the mainframe RF plug-in channel is clear, align the RF unit in the channel and slide it carefully into place towards the rear of the channel. It should slide easily without binding.

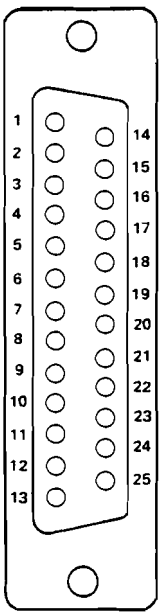
e. The drawer latch handle slot will engage with the locking pin just before the RF plug-in is fully seated in position.

f. Press the latch handle downward, while still pushing in on the RF plug-in, until the drawer latch is fully closed and the front panel of the RF plug-in is aligned with the mainframe front panel.

2-40. Bench Operation

2-41. The instrument cabinet has plastic feet and a foldaway tilt stand for convenience in bench operation. The tilt stand inclines the instrument for ease of operating the front panel controls and to allow the RF plug-in to be removed easier. The plastic feet provide clearance for air circulation and make the instrument self-aligning when stacked on other Hewlett Packard full rack-width modular instruments.

PROGRAMMING CONNECTOR J13
(as seen from rear panel)



Logic Levels:*

Low ≤ 0.8 Vdc
High ≥ 2.4 Vdc

Control of input lines can be accomplished by contact closure to ground for a logic low level and open circuit for a logic high level.

Pin	Mnemonic	Description	In/Out
1		NO CONNECTION	
2	L MP	LOW = MARKER PULSE	OUTPUT
3	L PLRQ	LOW = PENLIFT REQUEST	INPUT
4	ALT1	ALTERNATE SWEEP 1	OUTPUT
5	L SFSRQ	LOW = STOP FORWARD SWEEP REQUEST	INPUT
6	+5VA	+5 VOLTS (100 ma MAX)	OUTPUT
7	L RFB	LOW = RF BLANK	OUTPUT
8	L RF BRQ	LOW = RF BLANK REQUEST	INPUT
9	EXT TRG	HIGH = EXTERNAL TRIGGER SWEEP	INPUT
10	PL	HIGH = PENLIFT	OUTPUT*
11	L MUTE	LOW = PEN MUTE FOR X-Y RECORDER	OUTPUT
12		NO CONNECTION	
13		NO CONNECTION	
14	L BP1	LOW = BLANKING PULSE 1	OUTPUT
15	L MRKQ	LOW = MARKER REQUEST	INPUT
16	L RTS	LOW = RETRACE STROBE	OUTPUT
17	L ALTE	LOW = ALTERNATE SWEEP ENABLE	OUTPUT
18	L SSRQ	LOW = STOP SWEEP REQUEST	INPUT
19	GND DIG	DIGITAL GROUND	
20	L BPRQ	LOW = BLANKING PULSE REQUEST	INPUT
21	L CNTR	LOW = COUNTER TRIGGER	OUTPUT
22	L STPADV	LOW = STEP ADVANCE	INPUT
23	L PL	LOW = PENLIFT	OUTPUT
24	SYNC TRG	HIGH = SYNCHRONIZING TRIGGER	OUTPUT
25		NO CONNECTION	

* OPEN COLLECTOR OUTPUT

Figure 2-7. Programming Connector Signals and Pin Configuration

2-42. Front Handles (Option 907)

CAUTION

When installing front handles and rack mount kits, insure that the correct screws, specified in the installation figures in this section of the manual, are used. Use of a screw which is longer than the specified length may result in damage to internal components located behind the screw mounting holes in the instrument.

2-43. Instruments with Option 907 contain a Front Handle Kit. This kit supplies the necessary hardware and installation instructions for mounting two front handles on the instrument. Installation instructions are also given in Figure 2-9. Additional Option 907 Kits may be ordered as HP Part Number 5061-0089.

2-44. Rack Mounting (Option 908)

2-45. Instruments with Option 908 contain a Rack Mount Kit. This kit supplies the necessary hardware and installation instructions for preparing the instrument to mount on an equipment rack with 482.6 mm (19 inches) support spacing. Installation instructions are also given in Figure 2-10. Additional Option 908 Kits may be ordered as HP Part Number 5061-0077.

2-46. Rack Mounting with Front Handles (Option 909)

2-47. Instruments with Option 909 contain a

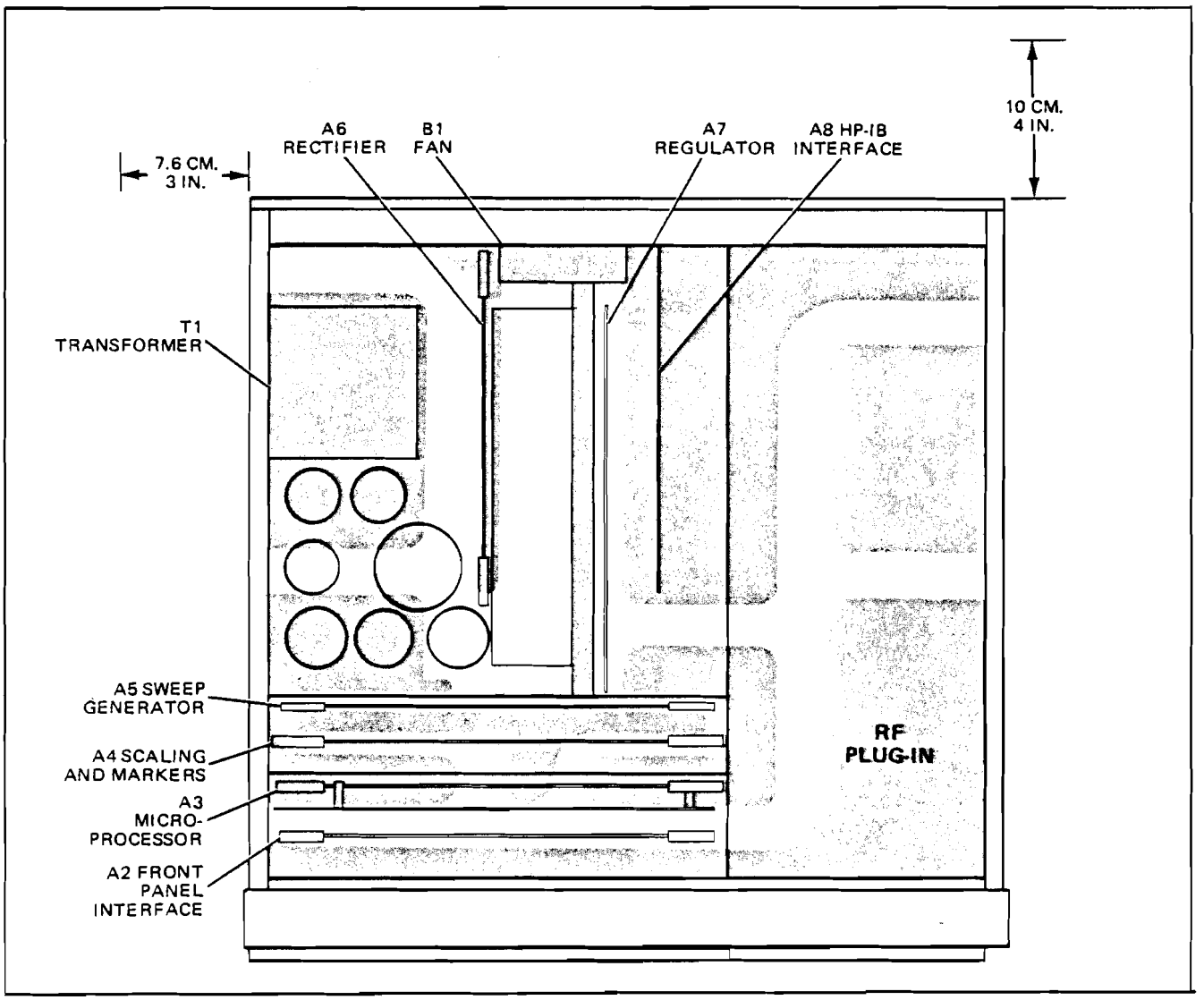
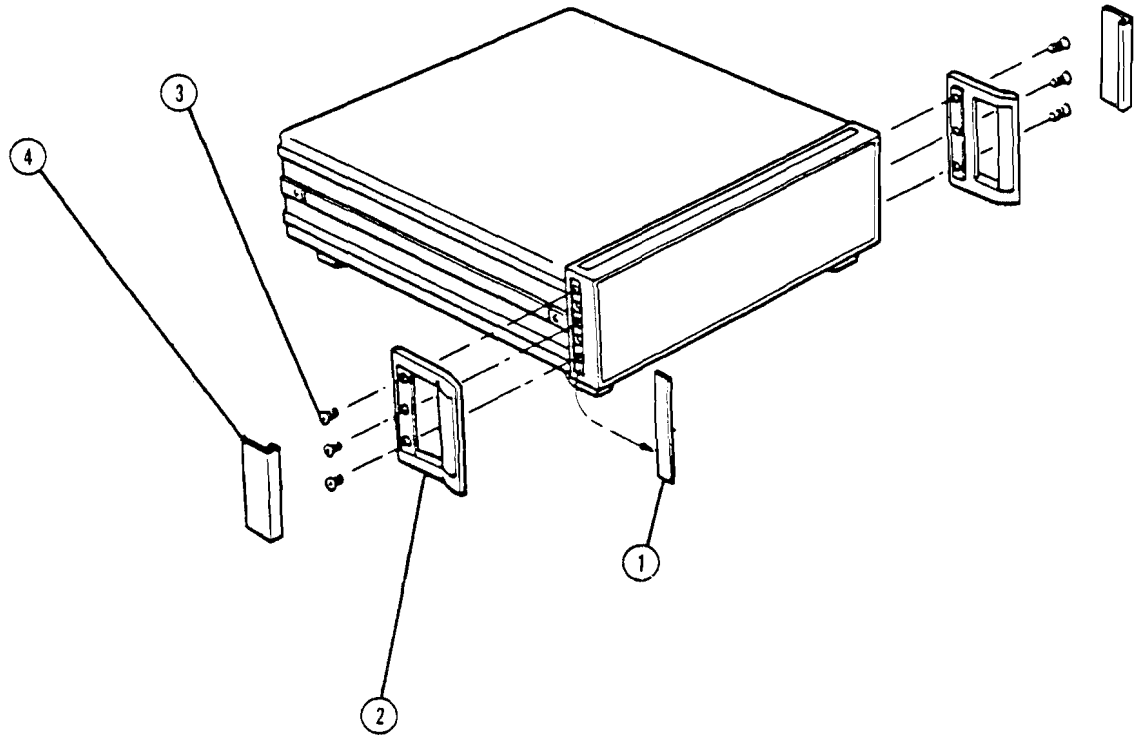


Figure 2-8. Model 8350A Ventilation Clearances and Airflow



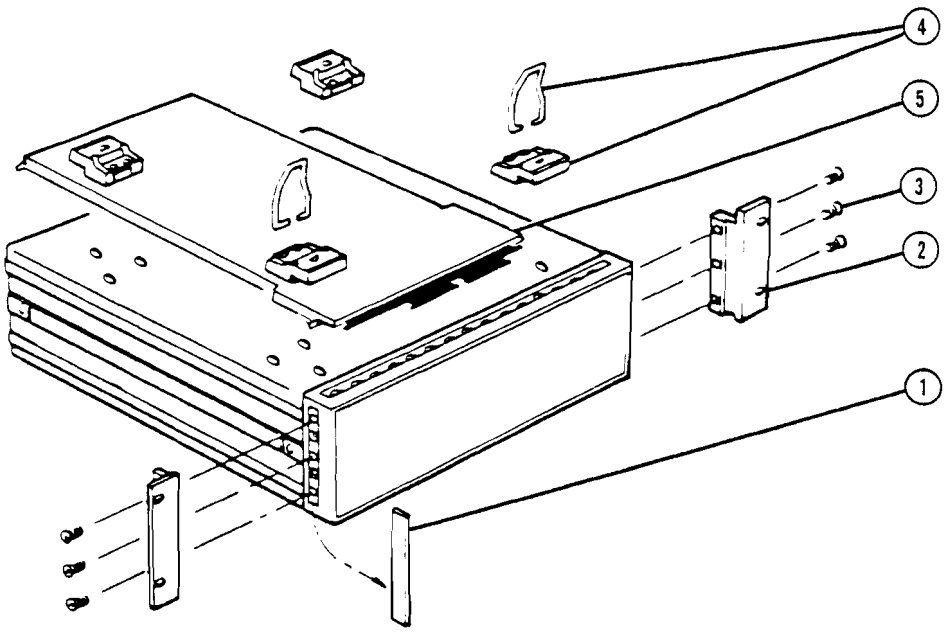
INSTALLATION INSTRUCTIONS:

1. REMOVE SIDE TRIM STRIPS (1).
2. ATTACH FRONT HANDLE ASSEMBLY (2) WITH THREE 8-32 x 3/8 SCREWS (3) PER SIDE.
3. PRESS FRONT HANDLE TRIM (4) IN PLACE.

OPTION 907 (HP Part No. 5060-0089) CONTENTS

Item	Qty.	HP Part No.	C D	Description
2	2	5060-9899	6	Front Handle Assembly
3	6	2510-0195	9	#8-32 x 3/8 Screw
4	2	5020-8896	7	Front Handle Trim

Figure 2-9. Option 907 Front Handles Kit



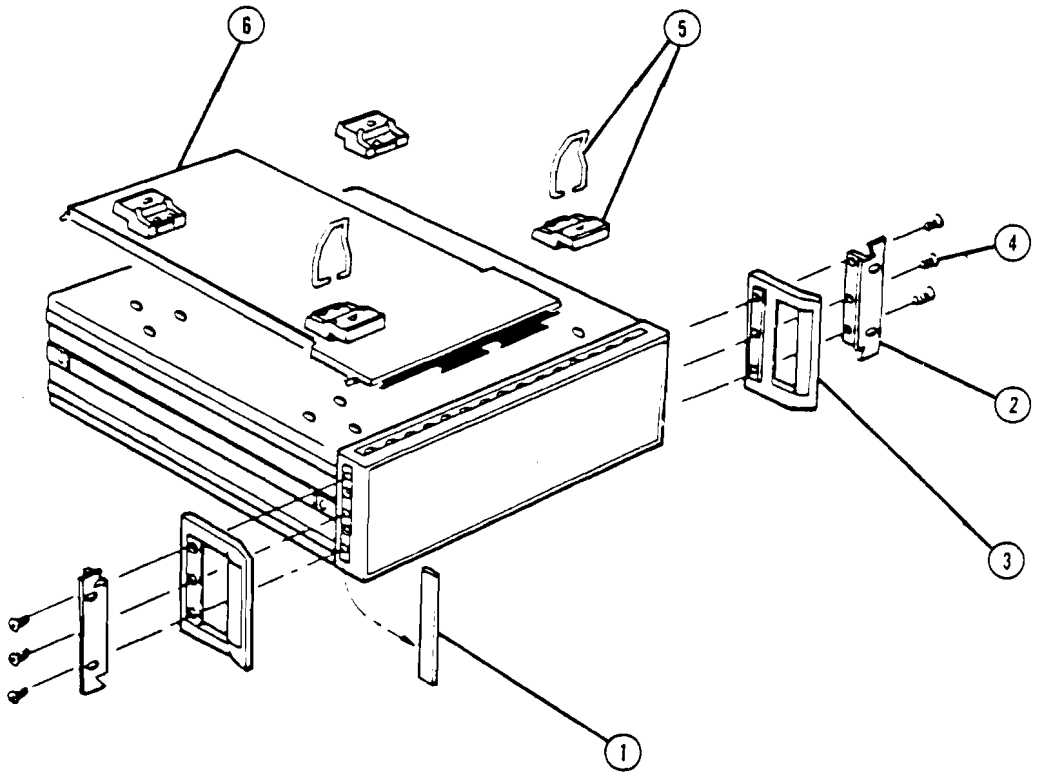
INSTALLATION INSTRUCTIONS:

1. REMOVE SIDE TRIM STRIPS (1).
2. ATTACH RACK MOUNT FLANGE (2) WITH 8-32 x 3/8 SCREWS (3).
3. REMOVE FEET AND TILT STANDS (4) BEFORE RACK MOUNTING. THIS ALSO REMOVES INFORMATION CARD TRAY (5). TO RETAIN USE OF INFORMATION CARDS, DO NOT REMOVE FEET, AND WHEN RACK MOUNTING, ALLOW APPROXIMATELY 2CM (3/4 INCH) BELOW INSTRUMENT TO ACCOMODATE THE TRAY. (NO FILLER STRIP IS PROVIDED.)

OPTION 908 (HP Part No. 5061-0077) CONTENTS

Item	Qty.	HP Part No.	C O	Description
2	2	5020-8862	7	Rack Mount Flange
3	6	2510-0913	9	#8-32 x 3/8 Screw

Figure 2-10. Option 908 Rack Mount Kit



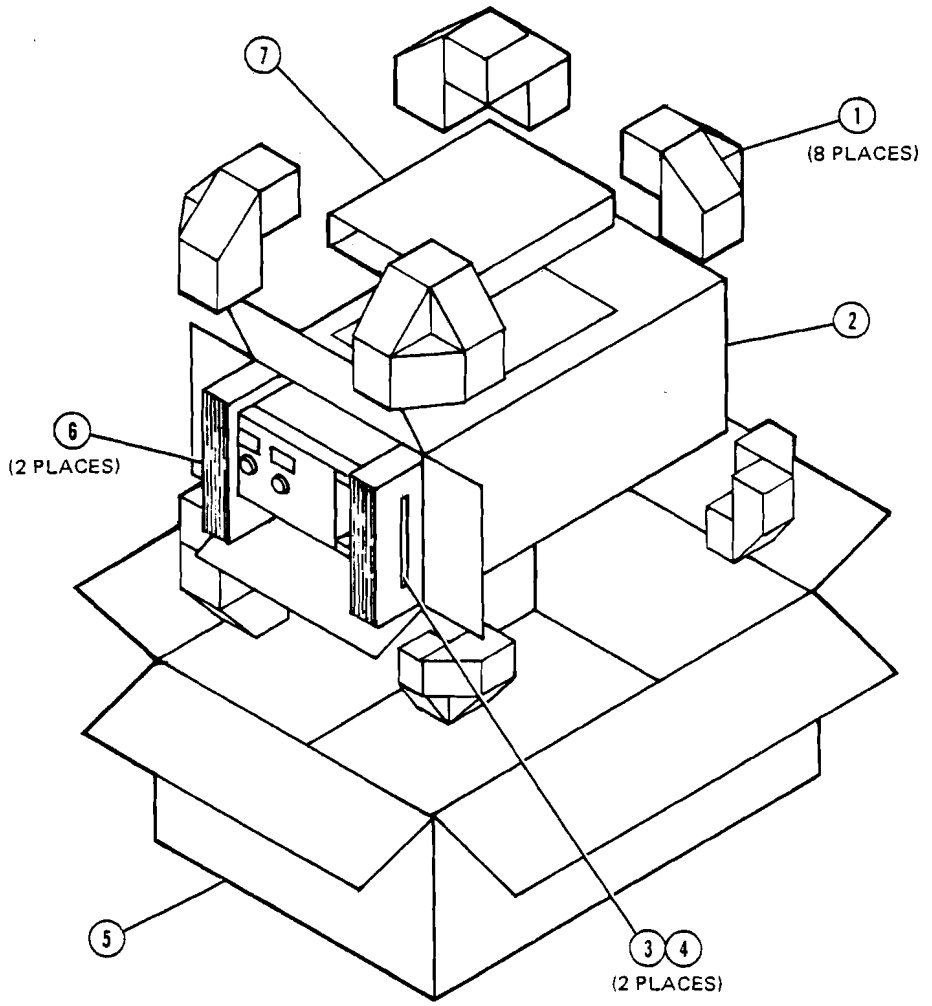
INSTALLATION INSTRUCTIONS:

1. REMOVE SIDE TRIM STRIPS (1).
2. ATTACH RACK MOUNT FLANGE (2) AND FRONT HANDLE ASSEMBLY (3) WITH THREE 8-32 x 5/8 SCREWS (4) PER SIDE.
3. REMOVE FEET AND TILT STANDS (5) BEFORE RACK MOUNTING. THIS ALSO REMOVES INFORMATION CARD TRAY (6). TO RETAIN USE OF INFORMATION CARDS, DO NOT REMOVE FEET, AND WHEN RACK MOUNTING, ALLOW APPROXIMATELY 2CM (3/4 INCH) BELOW INSTRUMENT TO ACCOMODATE THE TRAY. (NO FILLER STRIP IS PROVIDED.)

OPTION 909 (HP Part No. 5061-0083) CONTENTS

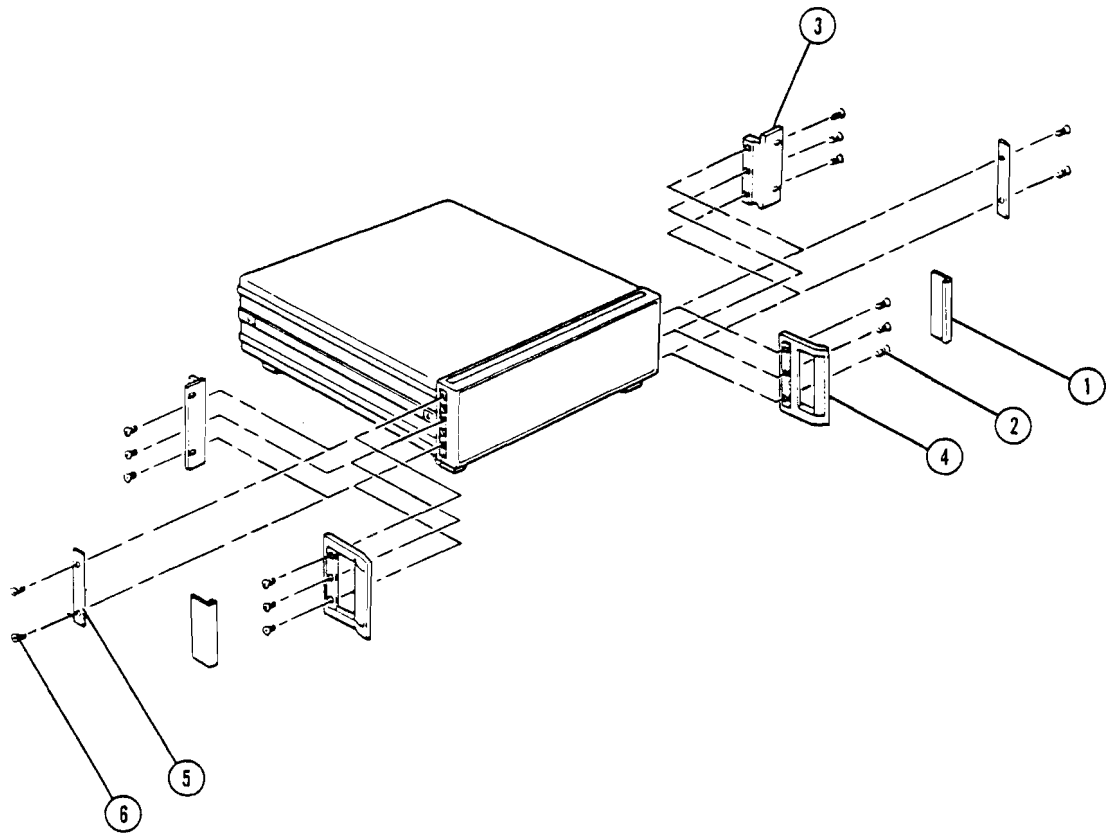
Item	Qty.	HP Part No.	C D	Description
2	2	5020-8874	1	Rack Mount Flange
3	2	5060-9899	6	Front Handle Assembly
4	6	2510-0194	8	#8-32 x 5/8 Screw

Figure 2-11. Option 909 Rack Mount Kit with Handles



Item	Qty	HP Part No.	C D	Description
1	8	9220-2733	7	FOAM PADS - TOP CORNERS; BOTTOM CORNERS
2	1	9211-3462	2	CARTON - INNER
3	2	4040-1738	3	BARS - SHIPPING, NYLON
4	4	2510-0103	9	SCREW - FOR ATTACHING SHIPPING BARS
5	1	9211-3463	3	CARTON - OUTER
6	2	9220-3365	3	SIDE PADS - CORRUGATED CARDBOARD
7	1	9220-2950	0	SLEEVE - FOR MANUAL PROTECTION
8	1	9222-0484	5	POLY BAG - TO COVER INSTRUMENT (NOT SHOWN)

Figure 2-12. Packaging for Shipment using Factory Packaging Materials



*Refer to Figure 2–5 for Part Numbers of Shipping Bars and Screws.

Figure 2-13. Preparation of Instrument for Shipment

Rack Mount Kit with Front Handles, a combination of the Option 907 Kit and the Option 908 Kit. This kit supplies the necessary hardware and installation instructions for preparing the instrument to mount on equipment rack with 482.6 mm (19 inches) support spacing, with the addition of front handles. Installation instructions are also given in Figure 2-11. Additional Option 909 Kits may be ordered as HP Part Number 5061-0083.

2-48. Battery Operation (Option 001)

2-49. Instruments with Option 001 contain a battery pack (inserted in the battery holder with a battery hold down clamp) and a modified A3 Microprocessor board. With Option 001 installed, the instrument has a nonvolatile memory which retains the contents of all instrument state storage registers, the current instrument state, and the HP-IB address. When shipped from the factory, the batteries are fully charged. The batteries will retain a sufficient charge to hold the memory contents for approximately 20 days from the date at which they were fully charged. The batteries are charged within the instrument, and a full charge is maintained at all times when the instrument LINE switch remains ON. The batteries do not charge when the instrument LINE switch is OFF. When fully discharged, the batteries will typically take approximately 33 hours to obtain a full charge. Allow the instrument to be on for at least 24 hours when new or when the instrument has been turned off for a sufficiently long enough period of time that the batteries might have become discharged to a level where memory contents may have been lost. Additional Option 001 Battery Kits may be ordered for the Model 8350A to upgrade a standard instrument to an Option 001 instrument by ordering HP Part Number 08350-60013. This Option 001 Battery Kit contains a battery pack, a battery pack hold down clamp, and a special A3 Microprocessor board. All other necessary wiring and hardware connections have been made at the factory on all standard instruments. Refer to Section VI Replaceable Parts in this manual for information and part numbers required to order individual battery packs.

2-56. Other Packaging. The following general instructions should be used for repackaging with commercially available packaging materials:

a. Wrap the instrument in heavy paper or plastic. If shipping to a Hewlett-Packard Office or Service Center, attach a tag indicating the type of service required, return address, model number, and full serial number.

b. Use a strong shipping container.

c. Use enough shock-absorbing material around all sides of the instrument to provide a firm cushion and to prevent movement inside the container. Protect the control panel with cardboard.

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to assure careful handling.

f. In any correspondence, refer to the instrument by model number and full serial number.

2-50. STORAGE AND SHIPMENT

2-51. Environment

2-52. The instrument may be stored or shipped in environments within the following limits:

Temperature	−40°C to +75°C
Humidity	5% to 95% relative at 0° to +40°C
Altitude	Up to 15240 meters (approximately 50,000 feet)

2-53. The instrument should also be protected from temperature extremes which may cause condensation in the instrument.

2-54. Packaging

2-55. Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. A complete diagram and listing of packaging materials used for the Model 8350A is shown in Figure 2-12. Prior to shipping in the factory packaging materials, the shipping bars should replace the front handles or rack mount flanges, as shown in Figure 2-13, to hold the instrument securely in the packaging material. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number (located on rear panel serial plate). Mark the container FRAGILE to assure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

SECTION III
OPERATION

The Operation section of this manual consists of the following three subsections:

1. **OPERATING INFORMATION:** This subsection contains indexed functional blocks which provide complete (local and remote) information on the use of the 8350A Sweep Oscillator by function. Also contained in this subsection is Operator's Maintenance, Local, and Remote Operator's checks.

2. **LOCAL OPERATION:** This subsection provides Local (non-HP-IB) operating information arranged by function. This subsection also contains information on locally interfacing with the following test equipment:

   - HP 8755S Frequency Response Test Set
   - HP 8410B Network Analyzer
   - HP 7010B and other X-Y Recorders
   - HP 5343A Frequency Counter

3. **PROGRAMMING NOTES:** Programming Notes are individual publications documenting the HP-IB use of the sweep oscillator. The following programming notes are included in this section:

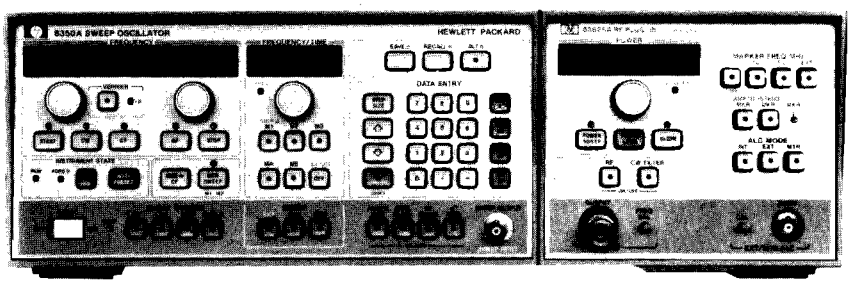
   - Introductory Operating Guide for use with the HP 9825A/B.
   - Introductory Operating Guide for use with the HP 9835A.
   - Introductory Operating Guide for use with the HP 9545A.
   - Introductory Operating Guide for use with the HP 85.
   - Quick Reference Guide.

Contact your local sales office for copies of other Programming Notes as they become available.

This section also includes a blue service tag page. If sweep oscillator service is required, remove one of the tags and fill in as much information as possible. Attach this tag to the sweep oscillator to aid in servicing and reduce turn-around time.

OPERATING INFORMATION

8350A SWEEP OSCILLATOR



HEWLETT PACKARD

8350A
SWEEP OSCILLATOR

MANUAL PART NO. 08350-90001
Microfiche Part No. 08350-90002

Printed: AUGUST 1980

HEWLETT PACKARD

SECTION III
OPERATING INFORMATION

3-1. INTRODUCTION

3-2. This subsection contains a index of keys and functions which refer to the figured functional blocks at the end of this subsection. Included in this section are descriptions of all front panel controls connectors and indicators, operator's checks, operating instructions, and operator's maintenance.

3-3. SAFETY

3-4. Before appplying power, refer to SAFETY CONSIDERATIONS in Section I of this manual.

3-5. The information, cautions, and warnings in this manual must be followed to ensure safe operation and to keep the insturment safe.

WARNING

Before the instrument is switched on, all protective earth terminals, extension cords, auto-transformers and devices connected to it should be connected to a protective earth grounded socket. Any interruption of the protective earth grounding will cause a potential shock hazard that could result in personal injury.

Only fuses with the required rated current and specified type should be used. Do not use repaired fuses or short circuited fuseholder. To do so could cause a shock or fire hazard.

CAUTION

Before the instrument is switched on, it must be set to the voltage of the power source, or damage to the instrument may result.

3-6. OPERATING CHARACTERISTICS

3-7. Table 3-1 briefly summarizes the major operating characteristics of the Sweep Oscillator. The table is not intended to be an in-depth listing of all operations and ranges. For more information on Sweep Oscillator capabilities, refer to Specifications Table 1-1, and Supplemental Information Table 1-2.

3-8. Panel Features

3-9. Figure 3-1 Front Panel features provides a reference to a functional block figure number which provides a complete description of each control within the function block.

3-10. Rear Panel features are described in Figure 3-2.

3-11. OPERATOR'S CHECKS

3-12. The local operator's check (Figure 3-3) allows the operator to make a quick check of the main instrument functions prior to use. This check assumes that an RF plug-in is installed in the Sweep Oscillator and that a 10 dB attenuator, oscilloscope, and appropriate crystal detector are available. If these items are not available the preliminary self test may still be performed.

3-13. The remote operator's check (Figure 3-4) allows the operator to make a quick check to the main remote functions prior to use. This test is shown in program statements for HPL and BASIC and a general flow chart.

3-14. OPERATING INSTRUCTIONS

3-15. Located underneath the Sweep Oscillator is a pullout information card which contains information on general operating instructions, some remote programming information, and some plug-in usage information.

3-16. For a complete reference of each function refer to the function group index (Table 3-2).

3-17. LOCAL OPERATION

3-18. The operation of the 8350A Sweep oscillator in the Local mode is described in the Local Operation handbook and by functional block figures indexed in the table of contents and Table 3-2.

FRONT PANEL FEATURES

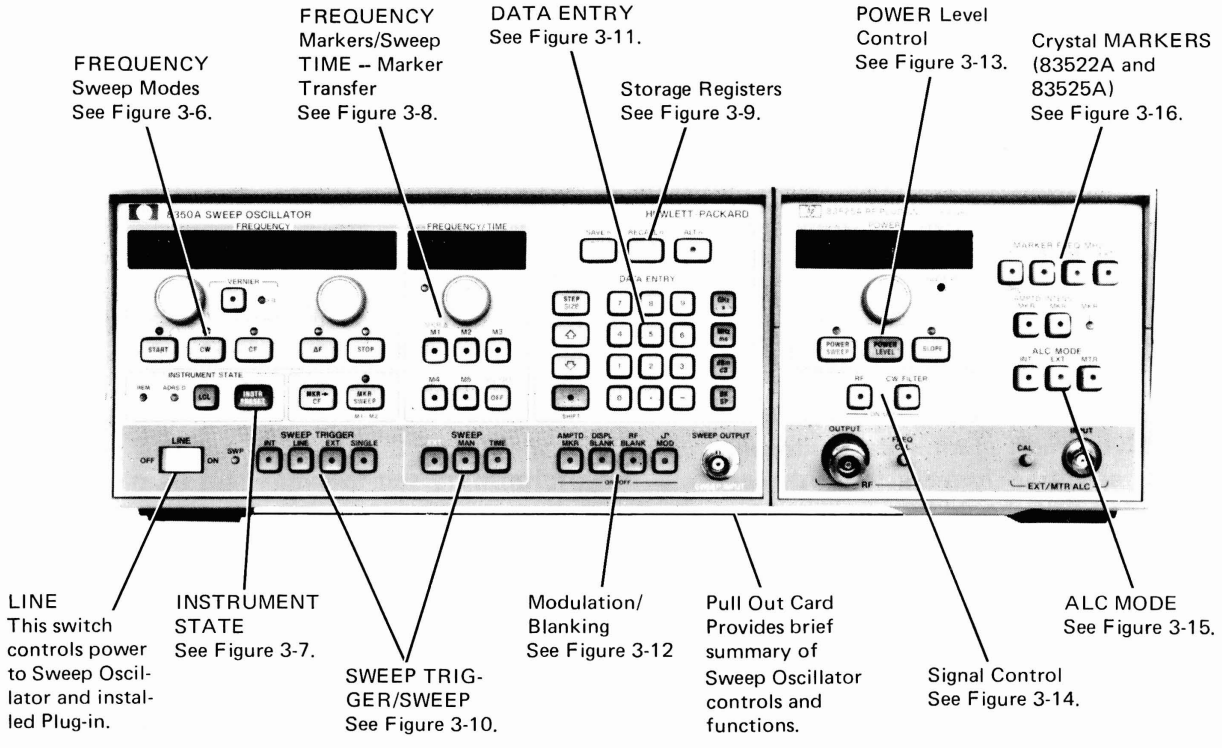
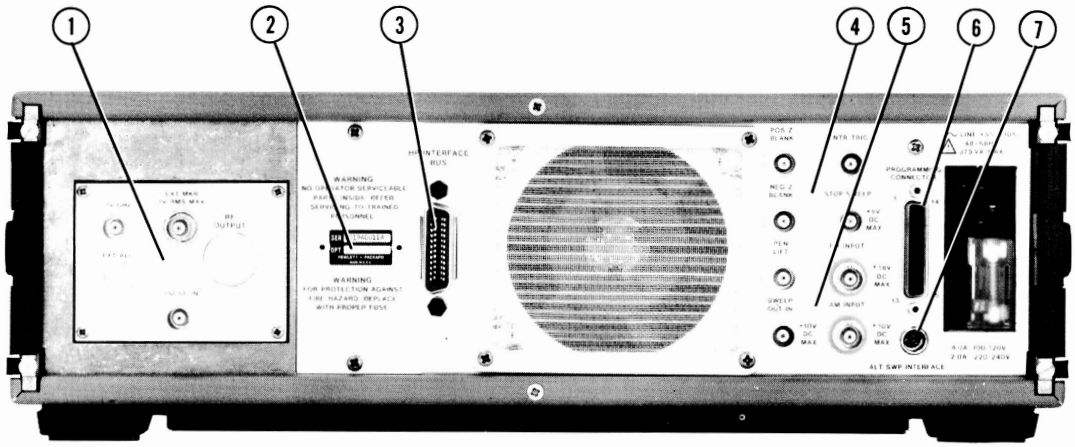


Figure 3-1. Front Panel Features

REAR PANEL FEATURES



Plug-in connectors (as apply)

1 1V/GHz Frequency Reference output connector provides approximately 1V (DC) per GHz of sweep signal output.

EXT MKR (1V RMS MAX) (on 83522A and 83525A only) input connector allows use of external markers when plug-in front panel EXT MARKER FREQ button is engaged.

SQUAREWAVE INPUT connector provides input connector for external pulse or squarewave modulation (8755 compatability).

EXT ALC and RF OUTPUT. These connectors replace the corresponding front panel connectors in Option 004 plug-ins.

2 SERIAL PLATE and Option label.

3 HP INTERFACE BUS input/output connector allows interface with other HP-IB instrument or controllers.

4 POS Z BLANK output connector provides positive (+5V) retrace and bandswitch blanking and negative intensity Marker Z-axis Modulation signals for external display.

CNTR TRIG. Counter trigger output connector when used with STOP SWEEP with appropriate frequency counter (SWP INTFC B) to stop the forward sweep long enough to take a frequency count.

NEG Z BLANK output connector provides retrace (−5V) and bandswitch blanking Z-axis modulation signals for external displays.

5 PEN LIFT output connector provides an open collector output to the remote penlift coil of an X-Y recorder.

SWEEP OUT/IN connector parallels front panel SWEEP OUT/IN connector. Provides and accepts sweep signal.

FM INPUT connector passes signal thru to plug-in for frequency modulation or phase-lock error signal inputs.

6 PROGRAMMING CONNECTOR provides digital control of external display functions and sweeper ◆ control.

Pin	Description	in/out	Logic
1	———		
2	Marker Pulses	output	TTL –
3	Pen Lift Request	input	TTL –
4	Sweep Alternate	output	TTL –
5	Stop Fwd Swp Req.	input	TTL –
6	+5 volts (100 ma Max)	output	TTL –
7	RF Blanking	output	TTL –
8	RF Blank Request	input	TTL –
9	Ext Trig Input	input	TTL +
10	Pen Lift	output	*
11	Recorder Mute	output	TTL –
12	———		
13	———		
14	Blanking Pulse	output	TTL –
15	Marker Request	input	TTL –
16	Retrace	output	TTL –
17	Alternate Swp En	output	TTL –
18	Stop Swp Request	input	TTL –
19	Digital Ground	in/out	
20	Blk Pulse Request	input	TTL –
21	Counter trigger	output	TTL –
22	Step Up Advance	input	TTL –
23	Inverse Penlift	output	TTL –
24	8410 Ext Trigger	output	TTL +
25	———		

7 ALT SWP INTERFACE connector may be connected to the 8755C ALT SWP INTERFACE connector via cable HP Part No. 8120-3174 to provide Alternate Sweep Function.

*Open collector (+4 volts dc 40 ma)

Figure 3-2. Rear Panel Features

Table 3-1. Sweep Oscillator Operating Characteristics

FREQUENCY RANGE	Set automatically when plug-in installed
SWEEP MODES	START-STOP CENTER FREQUENCY-ΔF Marker→Center frequency Marker Sweep CW Frequency
MARKERS	5 settable frequency markers amplitude and intensity
SWEEP TIME	Range .01–100 seconds
POWER	Control power level with 83500 Series Plug-ins

Table 3-2. Functional Block Index (1 of 2)

Table 3-2. Functional Block Index (2 of 2)

Function	Function Block Index	Page
Intensity Markers 8350A	Frequency Markers	26
Internal ALC	ALC Mode	41
Internal Sweep Trigger	Sweep/Sweep Trigger	32
Learn String	HP-IB Only Functions	45
Level Power	Power Control	38
Line Sweep Trigger	Sweep/Sweep Trigger	32
Local key	Instrument State	24
Manual Sweep	Sweep/Sweep Trigger	32
M1 to M5	Frequency Markers	26
Markers Crystal	Crystal Markers	43
Marker Delta	Frequency Markers	26
Marker Sweep	Frequency Markers	26
Marker→Center Frequency	Frequency Markers	26
Meter ALC	ALC Mode	41
Millisecond	Data Entry	34
MHz	Data Entry	34
Network Analyzer Trigger	HP-IB Only functions	45
Offset	Frequency Sweep Mode	21
Output Active Parameter	HP-IB Only Functions	45
Power Level	Power Control	38
Power Sweep	Power Control	38
Recall n	Storage Registers	30
RF	Power Control	38
Save n	Storage Registers	30
Shift	Data Entry	34
Single Sweep Trigger	Sweep/Sweep Trigger	32
Slope	Power Control	38
Slope Cal	Power Control	38
Square Wave ⊔⊓ Modulation	Blanking/Modulation	36
Start Sweep	Frequency Sweep Mode	21
Step Size	Data Entry	34
Stop Sweep	Frequency Sweep Mode	21
Time Sweep	Frequency Markers	26
UP ◆ Step key	Data Entry	34
Vernier	Frequency Sweep Mode	21

LOCAL OPERATOR'S CHECKS

DESCRIPTION

The Preliminary check provides assurance that most of the internal functions of the Sweep Oscillator are working. The main check provides a general check of the overall functions of the Sweep Oscillator.

PRELIMINARY CHECK

(Self test) Each time the Sweep Oscillator is turned on or INSTR PRESET button is engaged the instrument performs a series of self tests taking about one second to complete. When the self test is complete the instrument will be in the preset mode if a plug-in is installed or the left-most frequency display will have an E001 error code indicating no plug-in is installed. If error code E016 is observed refer to paragraph 3-103. If another error code is noted the Sweep Oscillator requires service refer to paragraph 3-107. Plug-in related error information (E050 to E059) is in the plug-in manual.

1. Set LINE switch to ON. Observe display in START/STOP mode with display frequency equaling plug-in range or E001 if no plug-in is installed.

MAIN CHECK

Equipment:

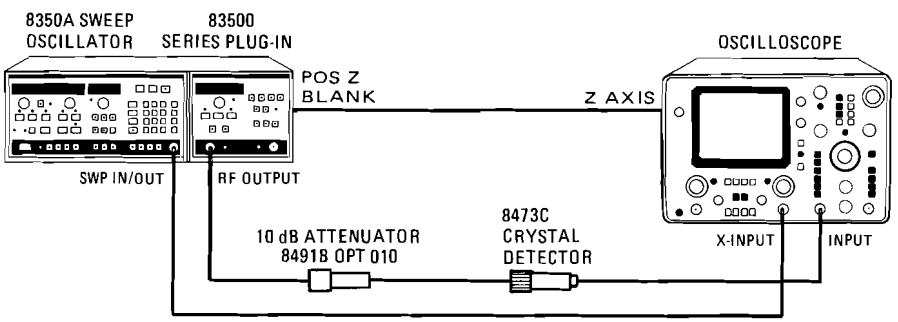
RF Plug-in ..... HP 83500 series or HP 86200 series with adapter HP 11869A (18 GHz or less)
Oscilloscope..... HP 1220A or HP 1740A

Crystal Detector ..... HP 8473C or a crystal detector that will cover frequency range of interest.

Attenuator 10 dB ..... 8491B Option 010

Cables BNC to BNC (3)..... 10503A (123 cm)

Setup:



Connect the equipment listed above as shown in above diagram.

Figure 3-3. Local Operator's Check (1 of 2)

LOCAL OPERATOR'S CHECKS (Cont'd)

CAUTION

BEFORE CONNECTING LINE POWER, ensure that all devices connected to this instrument are connected to the protective (earth) ground.

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that the line power plug is connected to a three-conductor line power outlet that has a protective (earth) ground. (Grounding one conductor of a two-conductor outlet is not sufficient.)

NOTE

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and the safety precautions are taken. See Power Requirements, Line Voltage Selection, Power Cables, and associated warnings and cautions in Section II.

Procedure:

1. Set LINE switch to ON position. Observe that LEDs above START and STOP buttons are on with the frequency range of installed plug-in displayed above them. Oscilloscope trace should show detected RF signal output below zero–volt reference with no discontinuities in swept trace across band.

2. Press CW button. Observe LED above CW on and trace is reduced to dot at center of CRT with display at center of plug-in frequency range.

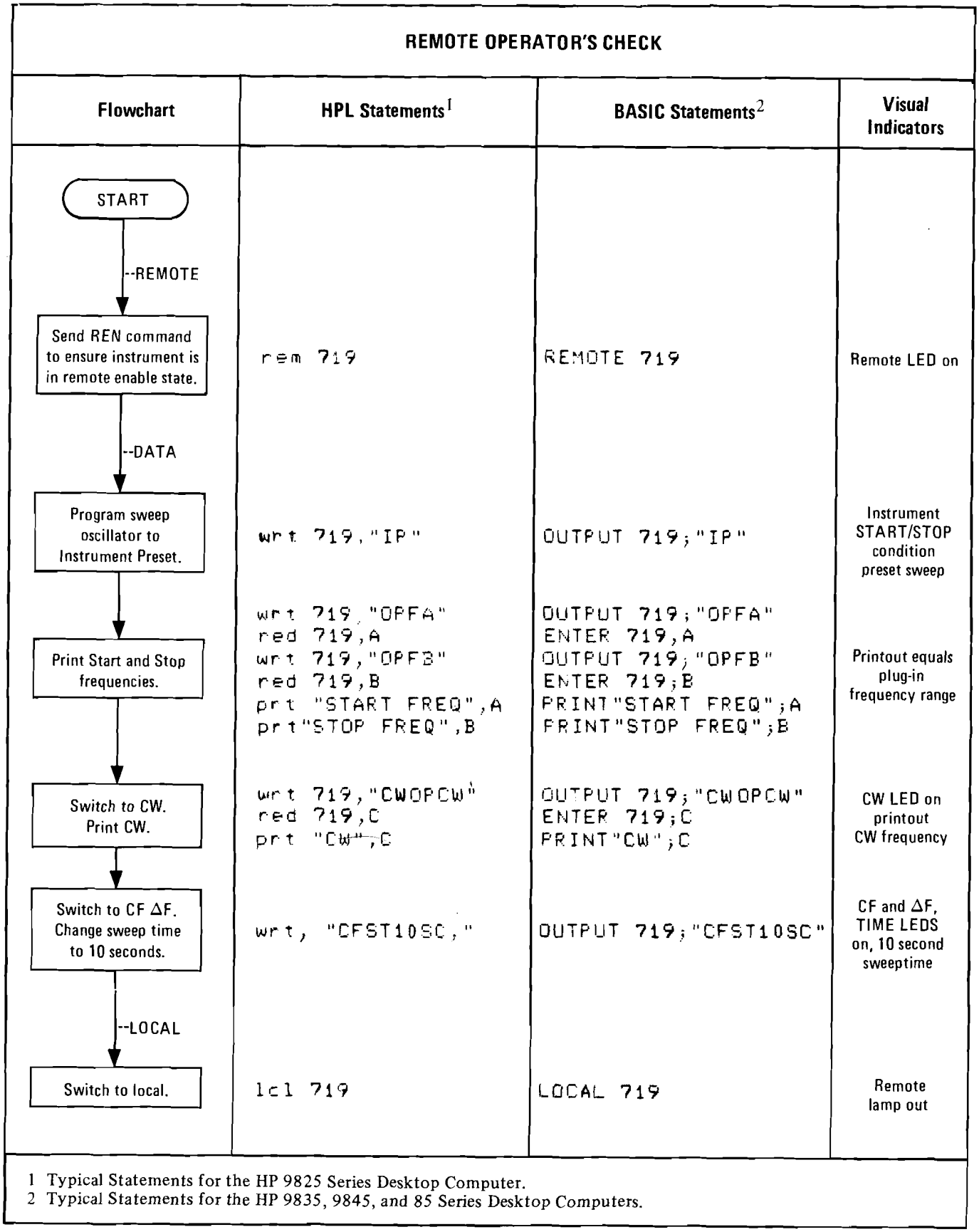
3. Press CF button. Observe LED above CF and ΔF buttons on, that displayed center frequency is at center of plug-in frequency range and ΔF display is equal to frequency span.

4. Press M1 button. Observe button LED on an blinking and a intensity dot at approximately the center of the trace.

5. Press SWEEP TIME button then press DATA ENTRY ◄ button a few times and observe sweep getting slower. Press DATA ENTRY ► button a few times and observe sweep getting faster.

6. Press DATA ENTRY . 1 GHz/s and observe FREQUENCY/TIME display is 0.100 sec.

Figure 3-3. Local Operator's Check (2 of 2)



1 Typical Statements for the HP 9825 Series Desktop Computer.
2 Typical Statements for the HP 9835, 9845, and 85 Series Desktop Computers.

Figure 3-4. Remote Operator's Check

3-19. REMOTE OPERATION: HEWLETT-PACKARD INTERFACE BUS

3-20. The 8350A Sweep Oscillator can be operated remotely via the Hewlett-Packard Interface Bus (HP-IB). Bus compatibility, programming capability, and data formats are described in the following paragraphs. For complete information on specific program code syntax, functions, limits, etc., please see Functional Block Index Table 3-2.

3-21. All front panel functions except for the LINE switch and Set HP-IB Address are programmable through the HP-IB. Also provided are special HP-IB only functions to aid the programmer. Complete descriptions of all HP-IB programmable functions are contained within the functional blocks.

3-22. To verify that the Sweep Oscillator's HP-IB interface is functional, a quick check is provided in Figure 3-4 Remote Operators' Check. This tests that the 8350A can respond and send to the controller the fundamental HP-IB bus messages. The following information gives a general description of the HP-IB and defines the terms, concepts, and messages used in an HP-IB system.

3-23. For more information about the HP-IB, refer to any of the following documents:

IEEE Interface Standard 488-1975

ANSI Interface Standard MC1.1

"Improving Measurements in Engineering and Manufacturing" (HP Part No. 5952–0058)

"Condensed Description of the Hewlett-Packard Interface Bus" (HP Part No. 59401–90030)

3-24. General HP-IB Description

3-25. The HP-IB is a parallel bus of 16 active signal lines grouped into three sets according to function, to interconnect up to 15 instruments. Figure 3-5 is a diagram of the interface connections and bus structure. Table 3-3 defines the function of each signal line.

Table 3-3. The Bus Signals

Name	Nmemonic	Description
Data Input/Output	DIO1-8	The eight data lines for the byte of data.
Data Valid	DAV	Indicates the data lines have a valid byte of data.
Not Ready for Data	NRFD	Indicates that the listening devices are not ready to accept further data.
Not Data Accepted	NDAC	Indicates that the listening devices have not completely accepted the present byte of data.
Attention	ATN	Enables a device to interpret data on the bus as a controller command (command mode) or data transfer (data mode).
Interface Clear	IFC	Initializes the HP-IB system to an idle state (no activity on the bus).
Service Request	SRQ	Alerts the controller to a need for communication.
Remote Enable	REN	Places instruments under remote program control
End Or Identify	EOI	Indicates last data transmission during a data transfer sequence; used with ATN to poll devices for their status.

3-26. Eight signal lines form the first set and are termed "data" lines. The data lines carry coded messages which reperesent addresses, program data, measurements, and status bytes. The same data lines are used for input and output messages in bit-parallel, byte-serial form. Normally, a seven-bit ASCII code represents each piece (byte) of data, leaving the eighth bit available for parity checking.

3-27. Data transfer is controlled by means of an interlocked "handshake" technique which permits data transfer (asynchronously) at the rate of the slowest device participating in that particular conversation. The three data byte transfer control lines which implement the handshake (DAV, NRFD, NDAC) form the second set of lines.

3-28. The remaining five general interface management lines form the third set and are used in such ways as activating all the connected devices at once, clearing the interface, allowing a device to request service, etc.

3-29. Definition of HP-IB Terms and Concepts

3-30. The following list defines the terms and concepts that describe HP-IB system operations.

Byte: A unit of information consisting of 8 binary digits (bits).

Device: Any unit that is compatible with the IEEE Standard 488-1975.

Device Dependent: An action a device performs in response to information sent on the HP-IB. The action is characteristic of an individual devices' design and may vary from device to device.

Addressing: The set of characters sent by a controller to specify which device will send information on the bus and which device(s) will receive that information. A device may also have its address fixed so that it may receive information (listen only) or send information (talk only).

Polling: The process by which a controller can identify a device that needs interaction with it. The controller may poll devices for their operational condition one at a time, which is termed a serial poll, or as groups of devices simultaneously, which is termed a parallel poll.

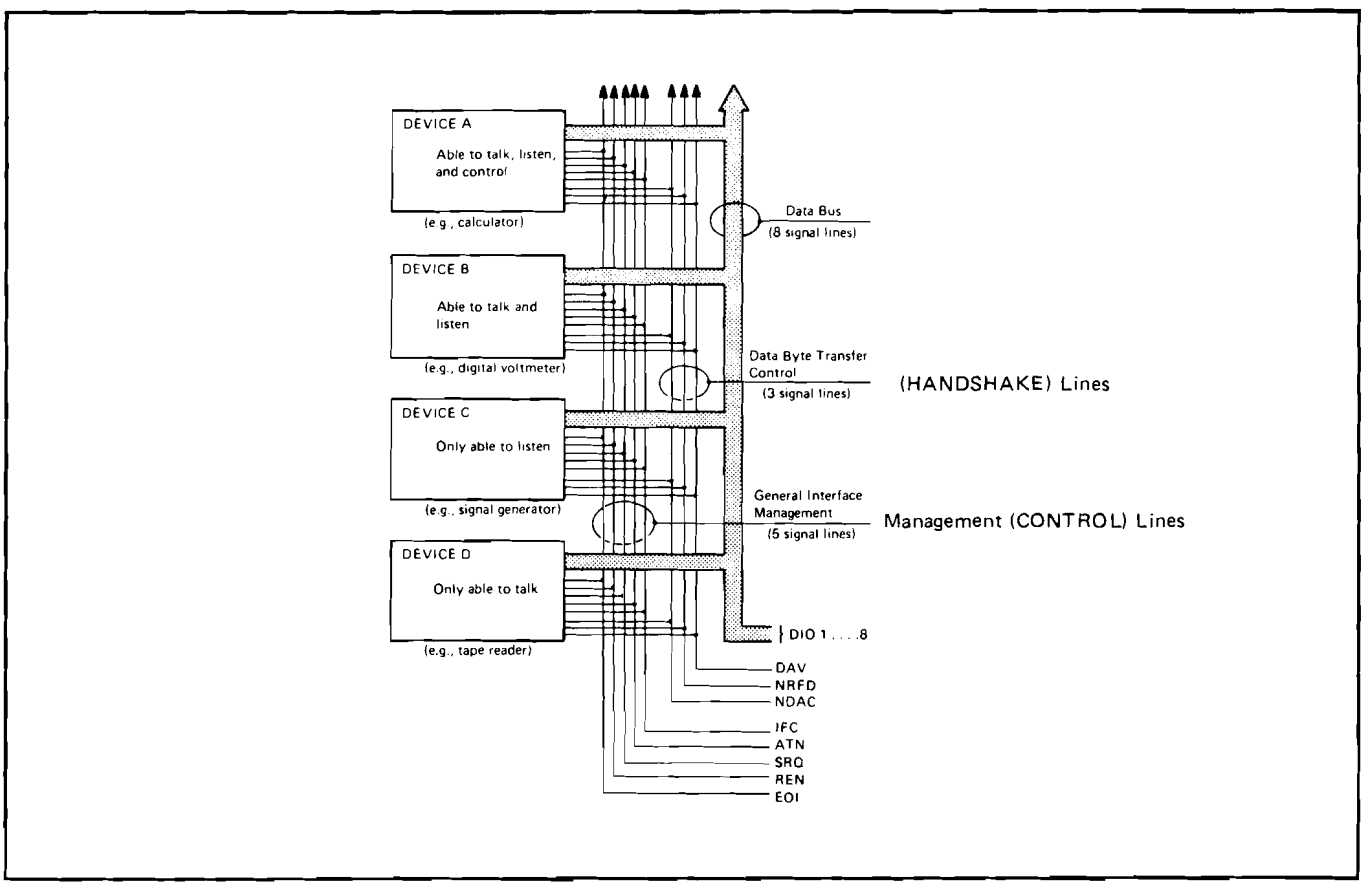


Figure 3-5. Interface Connections and Bus Structure

3-31. Basic Device Communication Capability

3-32. Devices which communicate along the interface bus fall into three basic categories.

Talkers: Devices which send information on the bus when they have been addressed.

Listeners: Devices which receive information sent on the bus when they have been addressed.

Controllers: Devices that can specify the talker and listener(s) for an information transfer. The controller can be an active controller or a system controller. The active controller is defined as the current controlling device on the bus. The system controller can take control of the bus even if it is not the active controller. Each system can have only one system controller, even if several controllers have system control capability.

3-33. HP-IB System Messages

3-34. The transfer of information via the HP-IB occurs from one device to one or more devices, thus consider the information to be a message. There are twelve types of messages on the HP-IB. The following describes each of the HP-IB System Messages.

a. **The Data Message:** The actual information which is sent from the talker to one or more listeners on the HP-IB. The information or data can be numeric or a string of characters.

b. **The Trigger Message:** This causes the listening device(s) to perform a device-dependent action when addressed.

c. **The Clear Message:** This causes either the listening device(s) or all of the devices on the bus to return to a predefined device-dependent state.

d. **The Remote Message:** This causes the listening device(s) to switch from local front panel control to remote program control when addressed to listen. This message remains in effect so that devices subsequently addressed to listen will go into remote operation.

e. **The Local Message:** This clears the remote message from listening device(s) and returns the device(s) to local front panel control.

f. **The Local Lockout Message:** This prevents the user of a device from manually inhibiting remote program control.

g. **The Clear Lockout/Set Local Message:** This causes all devices on the bus to be removed from local lockout and revert to local. This message also clears the remote message for all devices on the bus.

h. **The Require Service Message:** A device can send this message at any time to signify that the device needs some type of interaction with a controller. The message is cleared by sending the device's Status Byte message if the device no longer needs service.

i. **The Status Byte Message:** A byte that represents the status of a single device on the bus. Within this byte, the seventh most significant bit (bit 6 of bits 0 through 7) indicates whether the device has sent a Require Service message. The remaining bits indicate the present operational conditions defined by the device. This byte is sent from a talking device in response to a serial poll operation performed by a controller.

j. **The Status Bit Message:** A byte that represents the operational conditions of a group of devices on the bus. Each device responds on a particular bit of the byte thus identifying a device-dependent condition. This bit is typically sent by devices in response to a parallel poll operation by a controller.

k. **The Pass Control Message:** This transfers the bus management responsibilities from the active controller to another controller.

l. **The Abort Message:** The system controller sends this message to unconditionally assume control of the bus. This message terminates all bus communications but does not implement the Clear message.

This message can also be used by a controller to specify the particular bit and logic level that a device will respond with when a parallel poll operation is performed. Thus more than one device can respond on the same bit.

A summary of the twelve bus messages, their related commands and mnemonics are provided in Table 3-4.

Table 3-4. The Twelve Bus Messages (1 of 2)

HP-IB Message	Appli-cable	8350A Response	Related Comments	Interface Function	Message Type	Sample Statements	
						HPL (9825)	BASIC (9835,9845,85)
Data	Yes	Input data controls all front panel functions (except the Line switch) plus special HP-IB only functions. Output data includes information as to present instrument state, values of selected functions, and the instrument status.		T6 L4 AH1 SH1	Input Data	wrt 719,"..."	OUTPUT 719;"..."
					Output Data	red 719,A;...	ENTER 719;A,...
Trigger	Yes	Responds by triggering a sweep if and only if in the single sweep trigger mode.	GET	DT1	System Trigger	trg 7	TRIGGER 7
					Device Trigger	trg 719	TRIGGER 719
Clear	Yes	Clears the instrument status byte and the extended status byte.	DCL SDC	DC1	System Clear	clr 7	RESET 7
					Device Clear	clr 719	CLEAR 719
Remote	Yes	Removes the 8350A from local front panel control to remote HP-IB control. All functions remain the same as in local and the keyboard is non-responsive except the LOCAL key.	REN	RL1	System Remote	rem 7	REMOTE 7
					Device Remote	rem 719	REMOTE 719
Local	Yes	Removes the 8350A from remote HP-IB control to local front panel control. All functions remain the same as in the remote state.	GTL	RL1	System Local	lcl 7	LOCAL 7
					Device Local	lcl 719	LOCAL 719
Local Lockout	Yes	Functions the same as the remote message except that the entire front panel is disabled including the LOCAL key.	LLO	RL1		llo 7	LOCAL LOCKOUT 7
Clear Lockout/ Set Local	Yes	Removes the 8350A from local lockout and remote HP-IB control to local front panel control. All functions remain the same as in the remote state.	$\overline{\text{REN}}$	RL1		lcl 7	LOCAL 7
Require Service	Yes	The 8350A can set the HP-IB SRQ (Service Request) line if one of the following instrument conditions exists and has been enabled by the Request Mask value. Testable conditions include: parameter value altered, syntax error, end of sweep, power failure, and RF unleveled.	SRQ	SR1		rds(719)→A if bit (6,A) =1; gto "SRQ"	STATUS 719; A IF BIT (A,6)=1 THEN Srq

Table 3-4. The Twelve Bus Messages (2 of 2)

HP-IB Message	Appli-cable	8350A Response	Related Comments	Interface Function	Message Type	Sample Statements	
						HPL (9825)	BASIC (9835,9845,85)
Status Byte	Yes	Responds to a Serial Poll with one 8-bit byte with the seventh most significant bit (bit 6 of bits 0 through 7) set if the 8350A is Requesting Service. Bit 2 indicates a status change has occurred that can be detected only by analyzing the extended status byte which is accessible with the Output Status function only.	SPE SPD	T6		rds(719)→A	STATUS 719; A or A=S POLL (719)
Status Bit	No	The 8350A does not respond to a Paralell Poll.	PPØ				
Pass Control	No	The 8350A does not have the ability to take or pass control of the HP-IB.	CØ				
Abort	Yes	Responds by terminating all Listener or Talker functions.	IFC	T6 L4		cli 7	ABORT TO 7

3-35. HP-IB Addressing

3-36. Certain messages require that a specific talker and listener be designated. Each instrument on the bus has its own distinctive listen and/or talk address which distinguishes it from other devices. Devices can be listen only, talk only, and both talker and listener.

3-37. Addressing usually takes the form of "universal unlisten command, device talk address, device(s) listen address(es)". The universal unlisten command removes all listeners from the bus, thereby allowing only the listener(s) designated by the device(s) listen address(es) to receive information. The information is sent by the talker designated by the talk address. The system controller may designate itself as either talker or listener.

3-38. Table 3-5 lists all the possible talk and listen addresses on the bus. The device address is typically set via five binary bits which are the same for both listen and talk addresses, with the sixth and seventh bits used to determine when the address is listen (bits are 0,1) or talk (bits are 1,0). Some controllers distinguish between listen and talk automatically, requiring only the 5-bit code equivalent to designate a device.

3-39. 8350A HP-IB MESSAGE RESPONSES

3-40. The 8350A responds to the twelve bus messages as shown in Table 3-4.

3-41. 8350A HP-IB Compatibility.

3-42. Table 3-6 lists the 8350A Sweep Oscillators' HP-IB capability, which are compatible with IEEE Standard 488-1975.

Table 3-5. Possible HP-IP Addresses

ASCII Listen Address	Characters Talk Address	Address Code (Binary) 5 4 3 2 1	Equivalent Decimal Value
SP	@	0 0 0 0 0	00
!	A	0 0 0 0 1	01
"	B	0 0 0 1 0	02
#	C	0 0 0 1 1	03
$	D	0 0 1 0 0	04
%	E	0 0 1 0 1	05
&	F	0 0 1 1 0	06
'	G	0 0 1 1 1	07
(	H	0 1 0 0 0	08
)	I	0 1 0 0 1	09
*	J	0 1 0 1 0	10
+	K	0 1 0 1 1	11
,	L	0 1 1 0 0	12
-	M	0 1 1 0 1	13
.	N	0 1 1 1 0	14
/	O	0 1 1 1 1	15
0	P	1 0 0 0 0	16
1	Q	1 0 0 0 1	17
2	R	1 0 0 1 0	18
3	S	1 0 0 1 1	19
4	T	1 0 1 0 0	20
5	U	1 0 1 0 1	21
6	V	1 0 1 1 0	22
7	W	1 0 1 1 1	23
8	X	1 1 0 0 0	24
9	Y	1 1 0 0 1	25
:	Z	1 1 0 1 0	26
;	[	1 1 0 1 1	27
<	\	1 1 1 0 0	28
=	]	1 1 1 0 1	29
>	↑	1 1 1 1 0	30

Table 3-6. 8350A Interface Functions

Code	Function
SH1	Source handshake capability
AH1	Acceptor handshake capability
T6	Basic talker; Serial Poll; Unaddress to talk if addressed to listen
L4	Basic listener; Unaddressed to listen if addressed to talk
SR1	Service Request capability
RL1	Remote; Local capability
PP0	No Parallel Poll capability
DC1	Device clear capability
DT1	Device trigger capability
C0	No controller capability
E1	Open collector bus drivers

3-43. Compatible Universal and Addressed HP-IB Commands.

3-44. The 8350A will respond to the following universal and addressed commands, which are sent in the command modes (ATN true).

Mnemonic	Command	ASCII Code
Universal:		
DCL	Device Clear	DC4
LLO	Local Lockout	DC1
MLA	My Listen Address	(selectable)
MTA	My Talk Address	(selectable)
SPD	Serial Poll Disable	EM
SPE	Serial Poll Enable	CAN
UNL	Unlisten	?
UNT	Untalk	–
Addressed:		
GET	Group Execute Trigger	BS
GTL	Go to Local	SOH
SDC	Selected Device Clear	EOT

3-45. Remote Mode.

3-46. Remote Capability. The 8350A communicates on the bus in both remote and local modes. In remote, its front panel controls are disabled except the LINE switch and LCL key. The 8350A can be addressed to listen or talk. When addressed to listen, the 8350A will automatically stop talking and respond to the following bus messages: Data, Trigger, Clear, Remote, Local, Local Lockout, Clear Lockout/Set Local, and Abort. When addressed to talk, the 8350A will automatically stop listening and send one of the following messages: Data, Require Service, or Status Byte.

3-47. Displays. The REM light is on when the 8350A is in the remote mode. The ADRS'D light is on when the 8350A is currently addressed to talk or listen. All other displays function the same as in local front panel control.

3-48. Local-to-Remote Change. The 8350A switches to remote upon receipt of the two part Remote message. The two parts of the Remote message are:

Remote Enable (REN)
Addressed to Listen (MLA)

3-49. The Sweep Oscillator's output signal and all control settings remain unchanged with the local-to-remote transition.

3-50. Local Mode.

3-51. Local Capability. In local, the 8350A can send a Require Service message, send a Status Byte, and respond to the Remote message.

NOTE

The 8350A can respond to all HP-IB messages except the Data Message while in local. However, most of these messages would not normally be used in the local mode.

3-52. Remote-to-Local Change. The 8350A returns to local control upon receipt of the Local or Clear Lockout/ Set Local message. It can also be set to local by pressing the front panel LCL key (assuming that local lockout is not in effect). The Sweep Oscillator's output signal and all control settings remain unchanged with the remote-to-local transition.

3-53. Local Lockout. When a data transmission is interrupted, which can happen by returning the 8350A to local with the front panel LCL key, the data could be lost. This would leave the 8350A in an unknown state. To prevent this, a local lockout is recommended to disable the LCL key. Local lockout remains in effect until the 8350A is returned to the local state by either turning the LINE switch off/on or by programming the Local Message.

3-54. 8350A Address Assignment Information.

3-55. The 8350A has a primary address that is determined by an internal storage register. The register is initialized upon power turn on by reading the address bits A5 through A1 from switches located on the 8350A A8 HP-IB Assembly. Note that these switches are factory preset to decimal 19 (Listen address of "3", Talk address of "S"). The 8350A HP-IB address can be dynamically changed from the front panel in local mode by executing the "Set HP-IB Address" function (Shift Local).

The present 8350A HP-IB address can be found by pressing the SHIFT followed by the LCL key.

3-56. The decimal equivalent of the talk/listen address will be displayed in the FREQUENCY/ TIME display. Refer to Table 3-5 for interpretation of the equivalent decimal value into separate talk and listen address characters. To change the address refer to Figure 3-7 "Instrument State" for further information.

3-57. Receiving The Data Message

3-58. The 8350A accepts program codes that contain information for programming all of the front panel and special HP-IB only functions (except the LINE switch). The 8350A will respond to the Data message when in remote and addressed to listen.

3-59. Input Syntax. The 8350A responds to program codes in a Data message in the order in which they are received. Each function is programmed with a string of ASCII coded characters that follow one of the following sequences:

[Function Code] [Numeric Value] [Units Terminator] [EOS]
[Function Code] [Numeric Value] [EOS]
[Function Code] [EOS]

3-60. Function Codes. Function codes are typically 2 to 4 character mnemonics. For functions that have a numeric value associated with it, passing the function code only will enable and activate the function for further data entry.

3-61. Numeric Value. These are either a single decimal digit, a set of 14 characters or less representing a number, or a string of binary bytes. If the numeric value is a single digit (0 through 9), it represents a storage register. A string of 14 characters maximum can be expressed in exponential, decimal, or integer form. Acceptible numeric formats are referenced in further sections by the following format syntax:

Exponential	±d***d.d***E±dd
Decimal	±d***d.d***d
Integer	±d***d
Single Digit	d
Binary String	b***b
Binary Byte	b

Where the character 'd' indicates a leading or trailing zero, a space, or a numeric digit (0 through 9). The Characters '***' indicate a variable number of the previous characters. The character 'b' indicates an 8-bit binary byte. Numeric values that are not binary in nature are scaled by the appropriate units terminator.

3-62. Units Terminator. These are 2 character codes that terminate and scale the associated numeric value. Frequency values can be entered in GHz, MHz, kHz, or Hz. Sweep time values can be entered in Seconds or milliseconds. Power values can be entered in dBm or dB. If a units terminator is not passed, the 8350A assumes the numeric value is in the fundamental units of Hz or Seconds.

3-63. End Of String Message (EOS). This can be the ASCII character Line Feed (LF, decimal 10), the bus END command (EOI and ATN true), or another function code string.

NOTE

The HP-IB program code syntax typically mirrors that of the local front panel keystroke sequence.

3-64. Valid Characters. The alpha program codes can be either upper or lower case since the 8350A can accept either type. Spaces, unnecessary signs (+,−), leading zeroes, and carriage returns (CR) are ignored.

3-65. Program Codes. See Table 3-7 for the summary of input programming codes that are acceptible via the Data message.

3-66. Sending The Data Message.

3-67. The 8350A can send Data messages when in remote and addressed to talk. The available output modes are:

Learn String
Micro Learn String
Mode String
Interrogate Function
Active Function
Status

3-68. Each function is activated by the 8350A receiving a Data message with the appropriate function code (refer to Table 3-7). The Learn String, Micro Learn String, Mode String, and Status functions send a Data message consisting of a string of 8-bit binary bytes terminated using the bus END command (EOI and ATN true) with the last byte. The Interrogate and Active functions send a Data message consisting of a 14 character ASCII string representing the numeric value and terminated with a Carriage Return/Line Feed (CR/LF).

3-69. Binary Syntax. [b***b] [EOI]

3-70. Numeric Syntax. [±d.dddddE±dd][CR][LF]

3-71. The character 'b' indicates an 8-bit binary byte and 'd' indicates a decimal digit (0 through 9). The Characters '***' indicate a variable number of the previous characters. Note that the binary output format could have bytes that could be misinterpreted as Carriage Returns and/or Line Feeds so the user should defeat the ASCII CR/LF as a valid character string terminator.

3-72. Receiving The Trigger Message.

3-73. The 8350A responds to the Group Execute Trigger (GET) command to the HP-IB bus select code and a Selective Device Trigger to the 8350A HP-IB address. The effect of the GET command is to trigger the sweep if presently in the External Sweep Trigger mode only, otherwise no action is taken. The response is as if a Data message consisting of the Single Sweep Trigger (T4) program code were transmitted.

3-74. Receiving The Clear Message

3-75. The 8350A responds to both Device Clear (DCL) and Selective Device Clear (SDC) by resetting all HP-IB handshake lines to the inactive state. The effect is to remove the 8350A from any Talker or Listener control functions. The 8350A responds by clearing the Status Byte and the Extended Status Byte.

3-76. Receiving The Remote Message.

3-77. The Remote message causes the 8350A to switch to remote mode. It has two parts: 1) remote enable and 2) address-to-listen. The Sweep Oscillator's output and all other controls do not change with the local-to-remote transition.

3-78. The REM light turns on only when the 8350A is in remote mode and after receiving its first Data Message. The ADRS'D light turns on when the 8350A is addressed to talk or listen.

3-79. Receiving The Local Message.

3-80. The 8350A returns to front panel control when it receives the Local message. Its output and all other controls do not change with the remote-to-local transition.

3-81. When the 8350A goes to local mode, the front panel REM indicator turns off. However, the ADRS'D indicator would still illuminate if the 8350A were addressed.

3-82. The local message is the means by which the controller sends the Go To Local (GTL) bus command. The front panel LCL key can also return the 8350A to local mode. However, pressing the LCL key might interrupt a Data message to the 8350A and this would leave the 8350A in a state unkown to the controller. This situation could be avoided by sending the Local Lockout message which disables the LCL key.

3-83. Receiving The Local Lockout Message.

3-84. After receiving the Local Lockout message, the 8350A front panel LCL key is disabled in addition to all the other front panel keys. With local lockout in effect, the 8350A can be returned to local only by the controller or by turning the 8350A front panel LINE switch off/on.

3-85. Receiving The Clear Lockout/Set Local Message.

3-86. The 8350A responds to the Clear Lockout/ Set Local message in the same way as to the Local message. Hence it returns to local front panel control. The 8350A need not be addressed to listen to receive this message.

3-87. Sending The Request Service Message.

3-88. The 8350A sends a Request Service message (RQS) whenever one of the following conditions exist and if it has been preprogrammed

Table 3-7. HP-IB Program Codes

Code	Description	Code	Description
AKm	Amplitude Marker On/Off	MPm	Marker 1-2 Sweep On/Off
ALmn	Alternate Sweep On/Off	MS	Milliseconds
A1	Internal Leveling	MZ	MHz
A2	External Crystal Leveling	M0	Marker Off
A3	External Power Meter Leveling	M1	Marker #1
BK	Backspace	M2	Marker #2
CAm	Amplitude Crystal Marker On/Off (83522/83525 Only)	M3	Marker #3
CF	Center Frequency	M4	Marker #4
CIm	Intensity Crystal Marker On/Off (83522/83525 Only)	M5	Marker #5
CW	CW Frequency	NT	Network Analyzer Trigger (8410B)
C1	1 MHz Crystal Marker Frequency (83522/83525 Only)	OA	Output Active Parameter
C2	10 MHz Crystal Marker Frequency (83522/83525 Only)	OL	Output Learn String
C3	50 MHz Crystal Marker Frequency (83522/83525 Only)	OM	Output Mode String
C4	External Crystal Marker Frequency (83522/83525 Only)	OP	Output Interrogated Parameter
DF	Delta F Frequency Span	OS	Output Status bytes
DM	dBm	OX	Output Micro Learn String
DN	Step Down/Decrement	PL	Power Level
DPm	Display Blanking On/Off	PSm	Power Sweep On/Off
DUm	Display Update On/Off	RCn	Recall Register
E	Exponent Power Of 10	RFm	RF Power On/Off
FA	Start Frequency	RM	Service Request Mask
FB	Stop Frequency	RPm	RF Blanking On/Off
FIm	CW Filter In/Out	RS	Reset Sweep
F1	−20 MHz/V FM	SC	Seconds
F2	−6 MHz/V FM	SF	Frequency Step Size
GZ	GHz	SH	Shift Function
HZ	Hz	SLm	Slope On/Off
IL	Input Learn String	SM	Manual Sweep
IP	Instrument Preset	SP	Power Step Size
IX	Input Micro Learn String	SS	Step Size
KZ	KHz	ST	Sweep Time
MC	Marker To Center Frequency	SVn	Save Register
MDm	Square Wave Amplitude Modulation On/Off	SX	external Sweep
MO	Marker Off	TS	Take Sweep
		T1	Internal Sweep Trigger
		T2	Line Sweep Trigger
		T3	External Sweep Trigger
		T4	Single Sweep
		UP	Step Up/Increment
		VR	CW Vernier
		0–9 + −	Acceptable Numeric Data

NOTES

1. **Program codes of the form "XXm" use "m" to turn the function On or Off (1 or 0). For the storage register functions the "n" is 1 through 9.**
2. **The 8350A ignores spaces, plus signs, negative signs (except when valid) and any unexpected characters. Program codes can be upper or lower case alpha characters.**

to send the message by the Service Request Mask (RM) function:

Error in syntax
Parameter value modified to default value
Hardware failure
End of sweep

3-89. The 8350A can send a Require Service message in either the local or remote mode. Further information pertaining to the instrument state can be obtained by conducting a Serial Poll or by executing the Output Status function, both of which access Status Byte information. The RQS state and the bus SRQ line are cleared only by executing a Serial Poll.

3-90. Sending The Status Byte Message.

3-91. After receiving a Serial Poll Enable command (SPE) and when addressed to talk, the 8350A responds by sending its Status Byte message as indicated in Table 3-8. A second status byte is available but must be accessed via the Output Status function. When the seventh most significant bit (bit 6, Request Service) of the Status Byte is true (one), an SRQ has occurred. See Service Request for the conditions causing a Service Request. Bit 4 indicates whether a change has occurred in the Extended Status Byte. If Bit 4 is true, then the second status byte should be accessed via the Output Status function to determine the cause of the status change. All other bits indicate the present status of the noted function. The bits are true (one) if and only if the associated function/condition is true. To select an SRQ for a particular set of circumstances, both Status Bytes can be masked with the Service Request Mask function. The mask for each byte is determined by summing the decimal values of each selected function/condition that is desired. The default Service Request Mask Value is '00000000', or decimal 0. See Table 3-8 for decimal values of each Status Byte bit.

3-92. Sending The Status Bit Message.

3-93. The 8350A does not respond to the Parallel Poll Enable (PPE) bus command and thus cannot send a Status Bit message.

3-94. Receiving The Pass Control Message.

3-95. The 8350A does not have the ability to take or pass control thus it cannot respond to the Pass Control message.

3-96. Receiving The Abort Message.

3-97. The 8350A responds to the Abort message (IFC true) by stopping all Talker or Listener functions.

Table 3-8. Status Byte Information

STATUS BYTE (#1)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	N/A	REQUEST SERVICE (RQS)	SRQ on Syntax Error	SRQ on End of Sweep	N/A	SRQ on Change in Extended Status Byte	N/A	SRQ on Numeric Parameter Altered to Default Value

EXTENDED STATUS BYTE (#2)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	Airflow Failure	*RF Unleveled	Power Failure/on	N/A	N/A	N/A	N/A	Self Test Failed

*Bit/Functions not usable with 86200 Series Plug-ins and 11869A Adapter.

3-98. OPERATOR'S MAINTENANCE

3-99. Operator's maintenance consists of replacing defective fuses, cleaning the air filter, and cleaning the plug-in interface connectors. These items are discused in the following paragraphs.

3-100. Fuses

3-101. There are twelve fuses in the 8350A. Only the ac line fuse located at the back of the instrument may be replaced by the Operator. The value for the ac fuse is printed on the rear panel of the instrument below the power module. The value and HP part number for the ac fuse may be found in Sections II (Installation) and IV (Replaceable Parts).

WARNING

For continued protection against fire hazard, replace only with 250 V fuses of the same current rating and type (normal blow).

3-102. To replace the ac fuse the Line switch should be switched off then the ac line cord removed from the power source and instrument. With the line cord removed, access may be gained to the fuse compartment. The fuse may be removed by pulling the lever inside the fuse compartment. The internal fuses should only be replaced by a qualified service technician.

WARNING

It is important that the following maintenance procedures be executed to retain the safety features which have been designed into the instrument.

3-103. Air Filter

3-104. The cooling fan located on the rear panel has a metal filter attached which will require periodic cleaning. Due to the variety of environmental conditions the interval between cleanings cannot be estimated. Error signal E016 indicates reduced air flow through an increase in temperature in the cooling system. When this error is noted on display a clogged filter may be the reason. To clean the filter refer to Section 8 of the manual.

3-105. Plug-in Interconnect

3-106. If plug-ins are changed frequently and/or the interconnectors are dirty the 8350A plug-in interconnect connector may require cleaning to avoid voltage losses (tune voltage).

3-107. Service Tag Information

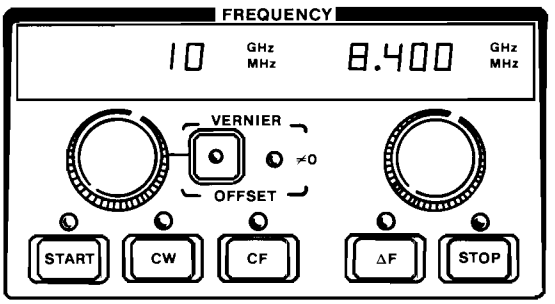
3-108. If the Sweep Oscillator requires service and the operators maintenance is not sufficient the instrument may be sent as per Section 2 to your local HP service organization. Before sending the instrument back, fill out and attach one of the blue service tags. If a sweep oscillator error code is noticed when a failure occurs, note that error code in the failure symptoms/special control settings section of the tag.

FREQUENCY Sweep Mode

DESCRIPTION

This function block contains the keys to select one of the three desired modes (START/STOP, CW, CF/ΔF) or a modification of the mode (VERNIER, OFFSET). The two displays provide a visual display of the frequencies in the mode selected. The rotary control knobs provide a variable control to change the frequency of the function selected.

PANEL LAYOUT



FUNCTIONS/INDICATORS

START: Enables START/STOP mode and allows selection of the lower frequency limit of sweep.

STOP: Enables START/STOP mode and allows selection of the upper frequency limit of sweep.

CW: Enables single frequency (CW) mode and allows selection of the frequency.

Swept CW: Enables CW mode with full SWEEP OUTPUT voltage (0-10 volts).

CF: Enables center frequency/delta frequency mode and allows selection of the center frequency.

ΔF: Enables center frequency/delta frequency mode and allows selection of the total frequency span.

VERNIER: Provides high resolution adjustments to values of the effective sweep center and CW frequencies. Range is 0.1 percent of plug-in frequency band.

OFFSET: Offset RF frequency by entered value. START/STOP, CF/ΔF, and CW displays do not indicate the change. Light indicates non-zero OFFSET value.

≠0: This lamp indicates when a non−zero frequency vernier or offset value is in effect. To zero the vernier or offset, enter 0 MHz.

Figure 3-6. Frequency Sweep Mode (1 of 3)

LIMITATIONS/CONCERNS

1. The range of frequencies input to mainframe is determined by the plug-in (will accept values to ±2% out of range).

2. CW resolution equals 4096 points per band (includes ± 2% overange) except in VERNIER. Example; using a 2 to 8.4 GHz plug-in, 1.6 MHz is the resolution. The display range is 1 MHz to 99.99 GHz.

3. The order in which START/STOP or CFΔF are entered is not important.

4. START frequency must be lower than STOP frequency. Entering a START frequency greater than the STOP frequency causes the STOP frequency to equal the START frequency. If the START frequency is greater than the STOP, then START equals the new STOP frequency.

5. Lights except as noted indicate active values/function.

6. Frequency values entered do not change when mode is changed.

7. Sweep Out provides a 0 to 10 volt ramp for all sweeps with 0 volts corresponding to the effective start frequency and 10 volts to the stop frequency. In CW mode the voltage out is equal to the percent of band (except swept CW).

8. Vernier value can "roll over" if knob or step causes the vernier value to exceed the maximum value then the CW/CF value is changed and the vernier value reset to 0 MHz (or appropriate value).

Figure 3-6. Frequency Sweep Mode (2 of 3)

LOCAL FUNCTION PROCEDURES:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard[1]	
Start Frequency	START		X	X	X	Range: See plug-in Resolution: ±0.24% of band
Stop Frequency	STOP		X	X	X	
Continuous Wave	CW		X	X	X	
Swept CW	SHIFT ΔF		X	X	X	
Center Frequency	CF		X	X	X	
Delta Frequency	ΔF		X	X	X	
Offset	SHIFT VERNIER		X	X	X	
Vernier	VERNIER		X	X	X	Range: ±.05% of plug-in Resolution: ±.0008% of band

[1] Values must end with terminator (GHz or MHz).

REMOTE FUNCTION PROCEDURES:

Mode	Function	Program Code				
		Suffix	Scale	Resolution	Range	Resolution
START/STOP	Start	FA	Plug-in	±0.24%	GZ MZ KZ HZ	$X10^9$ $X10^6$ $X10^3$ X1
	Stop	FB				
CW	CW	CW				
	Swept CW	SH CW				
CF/ΔF	Center Frequency	CF				
	Delta Frequency	DF				
OFFSET	Frequency Offset	SH VR				
VERNIER	Frequency Vernier	VR	±0.05% of band	±.0008%		

[1] Depends on plug-in used: 1KHz if <2 GHz in 83525 or 83522.

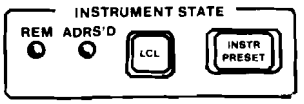
Figure 3-6. Frequency Sweep Mode (3 of 3)

INSTRUMENT STATE

DESCRIPTION

This function block contains two LEDs one that indicates whether Sweep Oscillator is in the remote mode, and another indictates when it is addressed to talk or listen. The local key when not in local lockout will switch the Sweep Oscillator from remote to local (front panel) control. The Instrument Preset key when engaged will first run the Sweep Oscillator self test then set the controls to the preset condition.

PANEL LAYOUT



FUNCTIONS/INDICATORS

LCL: Returns Sweep Oscillator control to front panel from remote operation unless a Local Lockout has been executed. The 8350A retains the same control settings when switched from remote to local.

Select HP-IB Address: Provides a way to see and change the current HP-IP address code (0 to 30). The code is displayed in the FREQUENCY/TIME display.

INSTR PRESET: The following two steps take place when instrument preset is engaged or the sweep oscillator is switched on. Plug-in related error (E050 to E059) information is found in the plug-in manual.

1. A self test of the entire instrument is begun that takes approximately 1½ seconds to complete. If an error is found the test stops and an error code is displayed. Section 8 has a list of error codes and failures.

2. After self test the sweep oscillator presets the controls as follows:

   SWEEP MODE: START/STOP, over the full frequency range of the plug-in
   SWEEP TIME: fastest allowable for plug-in
   Markers/Modulation: off, Marker frequency values reset to center of band
   Vernier/Offset: 0 MHz
   SAVE/RECALL: all registers set to INSTR PRESET value (if Opt. 001 Non-volatile memory, values unchanged)

   When using 83500 series plug-ins:

   POWER LEVEL: maximum leveled value
   RF, CW Filter: on
   ALC MODE: INT
   CRYSTAL MARKERS: off (50MHz lamp on)

Figure 3-7. Instrument State (1 of 2)

REMOTE: Sets Sweep Oscillator into remote HP-IB operation.

LIMITATIONS/CONCERNS

1. Local key will not function if a Local Lockout has been implemented.
2. Allowable HP-IB addresses are from 0 thru 30. However the value 21 is typically reserved for the controller and should be avoided.
3. The HP-IB address set remains in effect until line power is turned off. At power turn on the internal HP-IB address switches are read and used as the address unless 8350A Option 001 is used. If Option 001 is used, the HP-IB address will remain unchanged.
4. If an instrument problem occurs Section 8 of the manual contains some operator initiated tests. These tests may isolate problems to enable service (via blue tag) to repair them faster.

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard	
Local Key	LCL	X				
Select HP-IB Address	SHIFT LCL				X[1]	Integers from 0 to 30
Instrument Preset	INSTR PRESET	X				
Remote	Not Available					

[1] Address entered only after pressing the GHz, MHz, or dBm keys.

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix				Resolution
Local	Use HP - IB Command					
Select HP-IB Address	Not Available					
Instrument Preset	Instrument Preset	I P				
Remote	Use HP - IB Command					

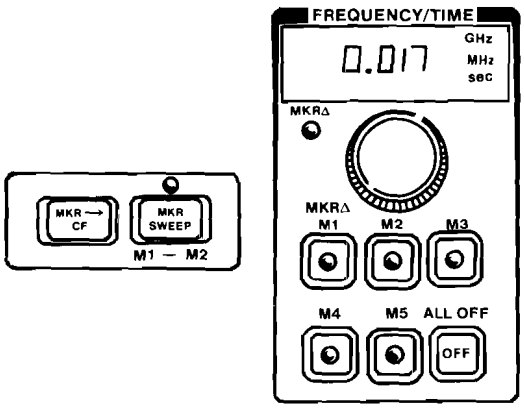
Figure 3-7. Instrument State (2 of 2)

FREQUENCY Markers/Sweep TIME-Marker Transfer

DESCRIPTION

The frequency marker functions consist of up to five independent and contiuously variable frequency markers. The Marker Δ function displays the difference frequency between any two markers. MKR→CF sets the effective sweep center frequency (CF) equal to the active marker frequency. MARKER SWEEP initiates/exits sweep between Marker 1 and Marker 2. After exit, sweep returns to original sweep limits. The FREQUENCY/TIME display will display active marker frequency, Marker Δ frequency, Sweep Time, or frequency in manual sweep mode.

PANEL LAYOUT



FUNCTIONS/INDICATORS

Markers 1 to 5: Each marker (M1 through M5) can be enabled and a frequency value defined. The last marker engaged is the active marker and it is the one modifiable by the control, step keys, keyboard, or remote control. Lamp off indicates marker off, lamp on, indicates marker on and lamp flickering indicates marker is active.

Active marker off: Turns off the active frequency marker and saves previous previous value. The value is recalled when marker is turned on later.

All Markers Off: Turns off all frequency markers saving the values of each to be recalled later when markers are turned on.

Marker Delta: Selects the MKR Δ mode where the FREQUENCY/TIME display indicates the frequency difference between the active frequency marker and the previously active frequency marker. The active marker is still active and modifiable via the FREQUENCY/TIME knob, step keys, keyboard or remotely. If in intensity marker mode the display trace is intensified between the two selected frequency markers.

Marker to Center Frequency: This function takes the value of the presently active frequency marker and reassigns it to the CW frequency, Center Frequency, or effective center frequency of the Start/Stop sweep. The frequency marker value is unchanged, the previous center frequency value is lost.

Figure 3-8. Frequency Markers/Sweep Time – Marker Transfer (1 of 4)

Marker Sweep: This function temporarily uses the values of Markers 1 and 2 and reassigns them to the Start and Stop frequencies respectively. The previous values of the Start and Stop frequencies are saved and reassigned when exiting Marker Sweep mode. If Marker 1 is greater than Marker 2 (or M2 less than M1) the lower frequency is used for the Start frequency, and the higher value for the Stop frequency. Note that the values of Markers 1 and 2 and hence the temporary Start and Stop frequency values can be modified in marker sweep mode by using either the start or the stop controls or M1 or M2 controls. The new values of M1 and M2 are retained upon exiting Marker Sweep mode.

Marker 1 to Start, Marker 2 to Stop: This functions the same as marker sweep except that the Start and Stop frequencies are permanently reassigned and not restorable to their previous values.

Counter Interface Enable and Disable: When Sweep Oscillator is used in swept mode this function enables the use of the 5343A Microwave Frequency Counter to count Start, Stop, or Marker frequencies.

LIMITATIONS/CONCERNS

1. All frequency markers are initialized to the value of the center frequency of the frequency range of the plug-in at power on.

2. Frequency markers if active and the present value is out of the present sweep frequency range, will be reassigned the value of the present effective center frequency when the FREQUENCY/ TIME knob is first turned.

3. If no markers are presently active when entering MKR Δ, Markers 1 and 2 are assumed the active and previously active markers respectively.

4. If Marker 1 frequency is higher than Marker 2 frequency then these values are permanently interchanged in Marker Sweep mode.

5. Start and Stop values are modified to correspond to the new center frequency and old sweep width in MKR→CF. Likewise the Δ Frequency Span and Start/Stop may be modified so that the new frequency sweep is within the frequency range of the plug-in.

6. If no marker is presently active the previously active marker is assumed. At power on Marker 1 is assumed to be the active marker.

7. If Marker 1 and/or Marker 2 are not on when entering Marker Sweep mode, they are turned on and their previous values used. At power on, all markers are assigned the value of the effective center frequency of the plug-in frequency range.

8. If sweep width is out of range when MKR→CF is engaged it will automatically scale down the Δ Frequency to be within plug-in frequency range.

9. The plug-in and markers have the capability of 2 percent frequency overrange, if this occurs a flickering of the GHz or MHz indicators will occur.

Figure 3-8. Frequency Markers/Sweep Time – Marker Transfer (2 of 4)

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard[1]	
Markers	M1 to M5		X	X	X	
Marker Δ	SHIFT M1		X	X	X	
Marker to Center Frequency	MKR→CF		X	X	X	Range See plug-in Resolution: .024% of band
Marker Sweep	MKR SWEEP	X	X	X	X	
Permanent Marker Sweep	SHIFT MKR SWEEP		X	X	X	
Turn Off Active Marker	OFF	X				
Turn Off All Markers	SHIFT OFF	X				
Counter Interface Enable	[function] SHIFT M2	X				
Counter Interface Disable	SHIFT M3	X				

[1] Values must end with terminator (GHz or MHz).

Figure 3-8. Frequency Markers/Sweep Time - Marker Transfer (3 of 4)

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
Markers	Select and Position Markers	M1 to M5	Plug-in	.024%		
Δ Marker	Displays Difference Frequency	SH M1			GZ MZ KZ HZ	$X10^9$ $X10^6$ $X10^3$ X^1
MKR → CF	Active Marker To	MC				
MARKER SWEEP	Sweep ON M1 and M2 OFF	MP1 MP0				
MARKER SWEEP	Permanent Marker Sweep	SH MP				
OFF	Active Marker Off	M1 to M5			MO MO	
ALL OFF	All Markers Off	SH			MO MO	
Counter Interface Enable	Counting End Points or Marker On Swept Frequency	FA, FB, or M1 to M5 SH M2				
Counter Interface Disable	Disables Swept Counting	SH M3				

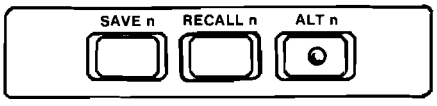
Figure 3-8. Frequency Markers/Sweep Time – Marker Transfer (4 of 4)

Storage Registers

DESCRIPTION

The Save n function allows all the control settings to be stored in one of the nine internal registers. The Recall n function will implement the previously stored settings. Alternate n function alternates between current state and register selected on successive sweeps.

PANEL LAYOUT



FUNCTIONS/INDICATORS

SAVE : Enables current settings (modes, frequencies etc.) to be stored in a register. Nine registers are available for storage (1 through 9).

RECALL: Enables a resetting of one of the nine stored register modes. When enabled the registers may be incremented with the UP control or decremented with the down control. Registers not previously stored will contain the instrument preset settings.

Alternate: Alternates between current state and selected stored register on successive sweeps. If used with appropriate HP 8755C, current state response is on channel 1 and selected state response is on channel 2.

LIMITATIONS/CONCERNS

1. Unused registers have instrument preset values stored until new new values are stored.
2. The instrument preset function sets all registers to instrument preset settings except in Option 001 instruments which retain stored settings even with AC power off.
3. Remote Step Up Advance (Programming Connector) or Auto Step allows cycling of storage registers.

Figure 3-9. Storage Registers (1 of 2)

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard	
Store Settings	SAVEn				X	Integers 1 to 9
Recall Settings	RECALLn			X[1]	X	Integers 1 to 9
Alternate Sweep Settings	ALTn			X[1]	X	Integers 1 to 9
Alternate Sweep Off	ALTn	X			X	

[1] Step keys activated only after a number has been entered.

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
SAVE	Store Current Settings	SV	Register 1 to 9			
RECALL	Resets Stored Settings	RC	Register 1 to 9			
ALTERNATE	Successive Sweep Selected and Current	AL1	Register 1 to 9			
	Alternate Off	AL0				

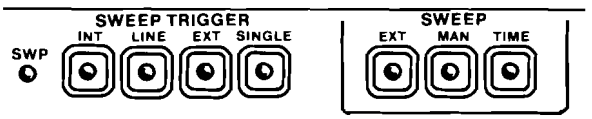
Figure 3-9. Storage Registers (2 of 2)

SWEEP/SWEEP TRIGGER

DESCRIPTION

This function Block contains seven keys for control of sweep source and time. This block also has a SWP LED to indicate sweep in progress. The SWEEP type keys enable selection of EXT, MAN or TIME sweep controls. The SWEEP TRIGGER keys enable selection of INTernal, LINE, EXTernal and SINGLE sources of sweep triggering. Lights on keys indicate active function.

PANEL LAYOUT



FUNCTIONS/INDICATORS

SWEEP EXTERNAL: Enables sweep input via front or rear panel SWP input BNC (SWP INPUT 0 to 10 volts) to externally tune plug-in oscillator.

SWEEP MANUAL: Enable manual control of sweep voltage via frequency inputs. Manual frequency is displayed on FREQUENCY/TIME display.

SWEEP TIME: Enables internally timed sweep. The triggering for TIME may be one of the following sweep trigger modes.

INT: Enables internal sweep triggering (free run, auto).

LINE: Enables triggering by power line frequency.

SWEEP TRIGGER EXT: Enables external triggering of sweep via rear panel auxiliary connector pin 9. A two volt trigger (20 volts max) must be supplied to auxiliary connector.

SINGLE: Selects and/or triggers or aborts single sweep.

LIMITATIONS/CONCERNS

1. SWEEP TRIGGER controls work only in TIME sweep mode.
2. Using the step keys with sweep time forces specific values in a 1,2,5 sequence such as 10ms, 20ms, 50ms, 100ms, etc. No step value can be set for sweep time.
3. When first engaged, single sweep is selected if in a different sweep trigger mode. If presently in single sweep, this triggers a new sweep.

Figure 3-10. Sweep/Sweep Trigger (1 of 2)

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off[3]	Knob	Step	Keyboard[1]	
SWEEP TYPE External	EXT	X				
Manual	MAN		X	X	X	Range: Present Sweep Width Resolution: 0.01% of present sweep
Time	TIME		X	X[2]	X	Range: 0.01 to 100 sec.[4]. Resolution: 0.001 sec.
SWEEP TRIGGER Internal	INT	X				
Line	LINE	X				
External Volts	EXT	X				2 to 5 Volts Input
Single Activates	SINGLE					Key and Triggers

[1] Values must end with terminator (GHz, MHz, S, or mS).
[2] The step size may not be set for time.
[3] Each mode (except TIME) disables other modes.
[4] The limit for broad band sweeps is higher than 0.01 second.

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
Sweep Type	External	SX				
	Manual	SM	Frequency		GZ MZ KZ HZ	$X10^9$ $X10^6$ $X10^3$ X1
	Time	ST	0.01–100 second	0.001 second	SC MS	X1 second $X10^{-3}$ seconds
Sweep Trigger	Internal	T1				
	Line	T2				
	External	T3				
	Single	T4				

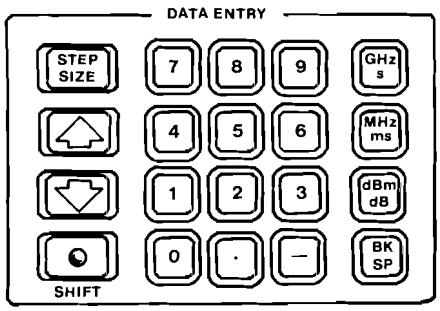
Figure 3-10. Sweep/Sweep Trigger (2 of 2)

DATA ENTRY-Step Keys/Keyboard

DESCRIPTION

This function block contains the step key function, numeric entry keyboard and terminators which allow modification of many of the values of functions. This function block has a back key which works like a erase or rubout of the last entry. Also in this function block is a shift key (blue) which enables shift key functions.

PANEL LAYOUT



FUNCTIONS/INDICATORS

STEP SIZE: This function allows the setting of the frequency or power level step size.

▲ (step up): This function increments the presently active parameter value by the appropriate step size.

▼ (step down): This function decrements the presently active parameter value by the appropriate step size.

0-9,—,.: Numeric digits, sign, and decimal point useable to input data for active function.

BACK SPACE: This function performs a character back space, or rubout, to erase the last digit entered on the present numeric entry. Function enabled only when entering a number and units terminator have not been entered.

GHz/s: Units terminator for Gigahertz frequency data or seconds time data.

MHz/ms: Units terminator for Megahertz frequency data or millisecond time data.

dBm/dB: Units terminator for dbm or dB power data.

SHIFT (blue key): This function enables the "shift" functions that are labeled in blue on the front panel or required key code in remote HP-IB.

LIMITATIONS/CONCERNS

1. Step size not settable for sweep time. It is a 1,2,5 data progression like 10 msec, 20 msec, 50 msec, 100msec, etc.
2. No visable data display for step size values.
3. Step size entry is differentiated via units terminator (ie. frequency or power step).
4. All numeric entries are not input/entered until the appropriate units terminator is entered.
5. Auto Step via depressing up or down key causes the active parameter to be stepped as long as the key is depressed.
6. The dBm/dB key will be a default value of Hz or sec.

Figure 3-11. Data Entry- Step Keys/Keyboard (1 of 2)

7. Negative numeric data must be entered with negative sign first.
8. Blank and unnecessary negative signs are ignored by the sweep oscillator.
9. Some shift functions are not labeled on the front panel, References Shift Function section.
10. Shift key indicator on until a correct shift function key stroke is entered.
11. The default Step Size values are 0.1% of the present ΔF for frequency parameters, 1 dB for power parameters.

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard	
STEP SIZE Frequency	(Frequency Parameter) STEP SIZE		X	X	X	Range: See plug-in frequency limits. Resolution: 1 MHz
STEP SIZE Power	(Power Parameter) STEP SIZE		X X	X X	X X	Range: See plug-in power limits Resolution: 0.01 dB
Reset to default STEP SIZE	SHIFT STEP SIZE	X				

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
STEP SIZE	Frequency Step Size	SF	See Plug-in Frequency Limits	1 MHz	GZ MZ KZ HZ	$X10^9$ $X10^6$ $X10^3$ X1
	Power Step Size	SP	See Plug-in	0.1 dB	DM	
STEP INCREMENT	Step Up (▲)	UP				
STEP DECREMENT	Step Down (▼)	DN				
BACK SPACE	Back Space	BK				
Default STEP SIZE	Reset to default STEP SIZE	SH SS				

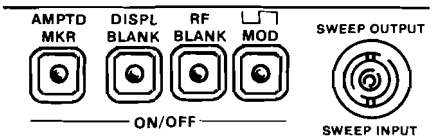
Figure 3-11. Data Entry – Step Keys/Keyboard (2 of 2)

Modulation/Blanking

DESCRIPTION

This function block controls the frequency marker display mode, RF power and external CRT control. Mainframe frequency markers can be RF amplitude dips or CRT intensity dots (via Z-axis control). The RF power can be turned off during the retrace sweep. The CRT display retrace sweep can be blanked. The internal squarewave amplitude modulation can be enabled. The squarewave frequency is 27.8 KHz standard for proper operation with the HP 8755 Frequency Response Test Set or internally selectable (see Section IV) for 1 KHz for proper operation with the HP 415 SWR Meter and other instruments. The sweep input/output connector is also in this block.

PANEL LAYOUT



FUNCTIONS/INDICATORS

AMPLITUDE MARKER: This function when engaged (light on) sets the mainframe frequency markers into RF amplitude dips instead of CRT intensity dots (via Z-axis control).

DISPLAY BLANKING: This function when engaged (light on) blanks the retrace sweep on CRT displays via Z−axis control.

RF BLANKING: This function when engaged (light on) blanks (turns off) the RF power during the retrace sweep.

⊔⊓ **SQUAREWAVE MODULATION:** This function when engaged (light on) enables the internal amplitude modulation squarewave. The standard squarewave frequency is 27.8 KHz, internally selectable to 1 KHz.

SWEEP OUTPUT/INPUT: When Sweep Oscillator is in manual or time sweep mode this connector provides a linear ramp voltage from 0 to 10 volts that is synchronous with RF sweep. In external sweep mode connector is input for a sweep ramp from 1 to 10 volts.

LIMITATIONS/CONCERNS

1. Changing frequency of modulation (1 or 27.8 KHz) requires removal of a jumper (see Adjustment section).

2. Plug-in frequency markers are controlled from plug-in for CRT intensity dots or RF amplitude dips.

Figure 3-12. Modulation/Blanking (1 of 2)

3. Internal squarewave modulation and a External AM signal can be used simultaneously.

4. CRT Z-axis control is provided with both positive and negative polarity control for blanking (via rear panel POS Z-BLANK or NEG Z-BLANK). Mainframe frequency markers, when used in the CRT intensity dot mode are useable with positive polarity Z-axis control only.

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard	
Amplitude Markers	AMPTD MKR	X				
Display Blanking	DSPL BLANK	X				
RF Blanking	RF BLANK	X				
Squarewave Modulation	⌐¬ MOD	X				

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
Amplitude Markers	Amplitude Marker On Amplitude Marker Off	AK1 AK0				
Blanking	Display Blanking On Display Blanking Off	DP1 DP0				
	RF Blanking On RF Blanking Off	RP1 RP0				
Modulation	⌐¬ Modulation On ⌐¬ Modulation Off	MD1 MD0				

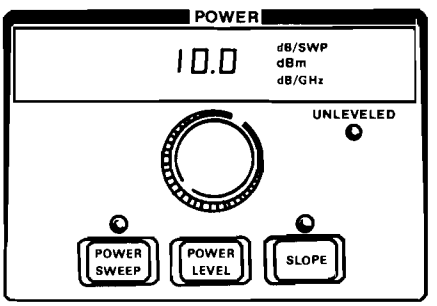
Figure 3-12. Modulation/Blanking (2 of 2)

POWER Control

DESCRIPTION

This function block contains all functions relating to the RF output power level. The desired power level can be set. To compensate for a linear lose through a device (like a cable) on the output of the plug-in, a slope compensation can be set to level the output. To provide a ramp of output power, a power sweep width can be set and the Power Sweep function enabled. Power Sweep starts the RF output power at the Power Level setting then ramps up the specific Power Sweep width.

PANEL LAYOUT



FUNCTIONS/INDICATORS

POWER LEVEL: This function when enabled (light on) allows setting of the output power level for all ALC modes. Calibrated power level in internal leveling mode only.

POWER SWEEP: This function when enabled (light on) allows setting of the power sweep width (in dB) for the power sweep function. Power Sweeps from Power Level to Power level plus Power Sweep width.

SLOPE: This function when engaged (light on) allows setting of the frequency slope compensation in dB/GHz. Allows compensation for lossy devices to achieve a flat, leveled output power at output of device/cable by increasing the output power at higher frequencies.

UNLEVELED Light: Light is on when all or portion of sweep is unleveled.

POWER Display: Provides digital display of Power Level and Power Sweep to a tenth of a dB and Slope to 0.01 dB. The units for power level are dBm, for power sweep dB, and for slope it is dB/GHz.

Figure 3-13. Power Control (83500 series Plug-ins) (1 of 2)

LIMITATIONS/CONCERNS

1. Power level control is calibrated over a 10 dB range, typically 15 dB. Power Level range up to 80 dB with plug-in Option 001 (70 dB Step Attenuator).
2. The total combined Slope and Power Sweep range is 15 dB.
3. Power Sweep will not cross a Step Attenuator boundary.
4. Power Sweep and Slope values may not be negative.

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard[1]	
Power Level	POWER LEVEL		X	X	X	Range: See plug-in Resolution: 0.024 dB
Power Sweep	POWER SWEEP		X	X	X	
Slope	SLOPE		X	X	X	

[1] Values must end with terminator (dBm or dB).

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
Power	Level	PL	10-15 dB	0.01dBm	DM	X1 dBm X1 dB
Power	Sweep On	PS1	25.5 dB			
	Sweep Off	PS0				
	Slope On	SL1	5 dB/GHz			
	Slope Off	SL0				

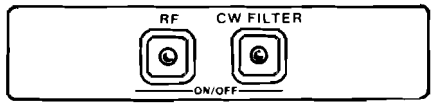
Figure 3-13. Power Control (83500 series Plug-ins) (2 of 2)

Signal Control

DESCRIPTION

This function block controls the signal purity and switches the signal RF off or on. The CW Filter, when enabled, reduces the oscillator tuning voltage noise and hence Residual FM. The CW Filter is inactive in sweep modes.

PANEL LAYOUT



FUNCTIONS/INDICATORS

RF ON/OFF: This function switches RF power on (light on) or off (≥30dB attenuation).

CW FILTER ON/OFF: This function enables (light on) or disables the oscillator tune voltage filter when in CW or manual sweep modes only.

LIMITATIONS/CONCERNS

1. CW filter not enabled during sweeps.

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard	
RF Power	RF	X				
CW Filter	CW FILTER	X				

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
RF	Power On Power Off	RF1 RF0				
CW Filter	Filter On Filter Off	FI1 FI0				

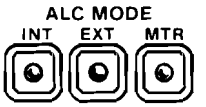
Figure 3-14. Signal Control (83500 series plug-ins)

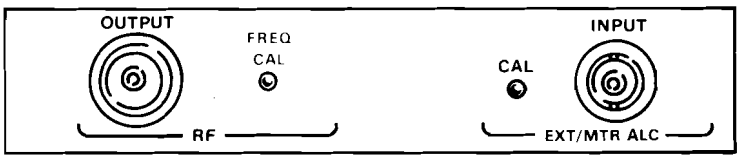
ALC MODE

DESCRIPTION

This functional block controls all Automatic Leveling Control (ALC) functions of the output power. Several modes of ALC can be selected, these are Internal, External via a Crystal/Detector, or external via a Power Meter.

PANEL LAYOUT





FUNCTIONS/INDICATORS

INTERNAL ALC: This selects the internal crystal detector/coupler for leveling the output power at the front panel output connector.

EXTERNAL ALC: This selects the external crystal detector for leveling with the detector output applied to the front panel External ALC BNC input connector.

METER ALC: This selects the external power meter for leveling with the power meter output applied to the front panel External ALC input connector.

EXT/MTR/ALC INPUT: Input connector for External crystal detector and power meter outputs.

ALC CAL: Used to adjust external leveling gain when using EXTERNAL leveling. Clockwise rotation increases gain.

FREQUENCY CAL: Adjustment that allows calibrating the RF plug-in frequency using the crystal markers, frequency marker indicator, and a CW or Start Frequency value.

LIMITATIONS/ CONCERNS

1. Only crystal detectors of negative polarity (−10 to −150 millivolts) can be used.

2. Only power meter outputs of 0 to 1 volts can be used. The HP 431 and 432 series are compatible, the HP 435 and 436 are not.

Figure 3-15. ALC Mode (83500 series plug-ins) (1 of 2)

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off[1]	Knob	Step	Keyboard	
Internal Leveling	INT	X				
External Leveling	EXT	X				
Power Meter Leveling	MTR	X				

[1] Each mode disables all other appropriate modes.

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix[1]	Range	Resolution	Suffix	Scale
ALC Leveling	INTERNAL	A1				
	External Crystal	A2				
	External Power Meter	A3				

[1] Mode disables all other possible modes.

FREQUENCY MARKER INDICATOR: Lamp lites when RF output frequency is coincident with the selected crystal marker frequency.

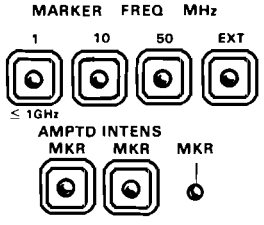
Figure 3-15. ALC Mode (83500 series plug-ins) (2 of 2)

Crystal MARKER FREQUENCY

DESCRIPTION

This functional block controls the crystal frequency markers by selection of the marker crystal frequency and the marker display mode (intensity or amplitude). Crystal frequency combs of 1 MHz (usable below 1 GHz), 10 MHz, 50 MHz, or an external frequency may be input to the rear panel External Marker input. The crystal frequency markers can be displayed independent of the mainframe frequency markers in their CRT intensity dot (via Z-axis control) and/or RF amplitude dips.

PANEL LAYOUT



FUNCTIONS/INDICATORS

1 MHz CRYSTAL: Selects (light on) a crystal frequency comb of markers at harmonics of 1 MHz.

10 MHz CRYSTAL: Selects (light on) a crystal frequency comb of markers at harmonics of 10 MHz.

50 MHz CRYSTAL: Selects (light on) a crystal frequency comb of markers at harmonics of 50 MHz.

EXTERNAL FREQUENCY: Selects frequency markers at the RF frequencies that are input to the rear panel External Marker input to the rear panel External Marker input. Allowable RF power range at input is −10 dBm minimum to +10 dBm maximum.

INTENSITY MARKER: Sets the marker display mode to CRT intensity dots via Z-axis control.

AMPLITUDE MARKER: Sets the marker display mode to RF amplitude dips.

EXTERNAL MARKER INPUT: Rear panel input for external frequency marker. Maximum drive range −10 to +10 dBm.

Figure 3-16. Crystal Marker Frequency (83500 series plug-ins) (1 of 2)

LIMITATIONS/CONCERNS

1. Plug-in markers display modes are independent of the 8350A mainframe markers. Hence any combination of intensity or amplitude markers will work.
2. Intensity markers obtainable using the positive polarity Z-axis output only.
3. Maximum drive level of External Marker Input is +10 dBm.
4. Plug-in markers can be intensity and amplitude variety simultaneously.

LOCAL FUNCTION PROCEDURE:

Function	Activate	Data Forms				Range and Resolution
		On/Off	Knob	Step	Keyboard	
1 MHz Marker	1	X				
10 MHz Marker	10	X				
50 MHz Marker	50	X				
External	EXT	X				
Amplitude Markers	AMPTD MKR	X				
Intensity Markers	INTENS MKR	X				

REMOTE FUNCTION PROCEDURE:

Mode	Function	Program Code				
		Prefix	Range	Resolution	Suffix	Scale
Crystal Marker Frequency	1 MHz [1]	C1				
	10 MHz [1]	C2				
	50 MHz [1]	C3				
	External Input [1]	C4				
Crystal Marker	Amplitude MKR On Amplitude MKR Off	CA1 CA0				
	Intensity MKR On Intensity MKR Off	CI1 CI0				

[1] Mode disables the previous mode.

Figure 3-16. Crystal Marker Frequency (83500 series plug-ins) (2 of 2)

HP-IB ONLY FUNCTIONS

DESCRIPTION

This section describes functions which are only accessible via the HP-IB. These functions allow the HP-IB user to learn about the present instrument state, setup the instrument state, and enable some special functions to improve HP-IB operation.

FUNCTIONS

INPUT/OUTPUT LEARN STRING: A string of 90 bytes of binary data that completely describes the present instrument state (does not include the storage registers) of the 8350A and 83500 Series Plug-in. This information is packed and encoded for minimal storage requirements thereby making data analysis difficult. If data analysis is necessary, use the Output Mode String and Output Interrogated Parameter functions instead. When output from the 8350A and stored in an ASCII character data string, the Learn String can later be input to the 8350A to restore that instrument state. The length of the Learn String is fixed, independent of the functions selected and the plug-in used.

The Output Learn String function learns the present sweeper settings only. To learn the storage register settings, sequentially recall each storage register then learn the present sweeper settings. Likewise to restore the storage registers, input the learn string for the appropriate storage register then save the present sweeper settings in the proper register.

INPUT/OUTPUT MICRO LEARN STRING: A string of 8 bytes of binary data that completely describes the present CW Frequency, Vernier, Sweep Output voltage, and Power Level of the 8350A and 83500 Series Plug-in. This information is packed and encoded for minimal storage requirements thereby making data analysis difficult. When output from the 8350A and stored in an ASCII character data string, the Micro Learn String can later be input to the 8350A to restore the instrument state for rapid CW frequency programming. The length of the Micro Learn String is fixed, independent of the functions selected and the plug-in used.

In this mode the 8350A numeric displays are blanked and the Micro Learn String bytes are used to pre-load the appropriate internal DAC's. For proper operation the 8350A must be in the CW mode and the plug-in CW Filter capacitor should be off. Since the Micro Learn String overrides the present values of the 8350A when it is input, do not program any functions while in this mode. If a function is programmed one of two things may occur: 1) the 8350A may exit the Input Micro Learn String mode with the previous sweeper settings restored, or 2) the 8350A may interpret the program codes as another Micro Learn String and cause the instrument to enter a non-predicatable state. The only function that is valid for execution while the Micro Learn String is in effect is the Network Analyzer Trigger function.

To output the Micro Learn String: 1) program the desired CW frequency, 2) program the "OX" code, then 3) read the 8 byte string.

To input the Micro Learn String: program the "IX" code and the 8 byte string. When the user desires to exit the Input Micro Learn String mode and return to the normal mode of operation, the user must exit properly. When in the Input Micro Learn String mode the 8350A accepts the input program code/bytes in a special binary entry mode. The mode is exited by programming

Figure 3-17. HP-IB Only Functions (1 of 7)

the 8350A with a function code that does not start with a number (0—9) or the letters A through F since these are interpreted as possible Micro Learn String data characters. It is suggested that the user exit this mode by using the "M0" code as the mode terminator then restore the numeric displays via the "CW", "ST", and "PL" function codes.

OUTPUT MODE STRING: A string of 25 bytes of binary data that describes all of the presently active functions of the 8350A and 83500 Series Plug-in. This information is not packed thus allowing simple data analysis. The information passed indicates only which functions are presently active functions with no numeric values included. By determining the decimal value of each byte the user can determine which function is active. To determine the actual numeric value of some functions use the Output Interrogated Parameter function. The length of the Mode String is fixed, independent of the functions selected and the plug-in used.

OUTPUT INTERROGATED PARAMETER: The 8350A outputs the present numeric value of the instructed parameter that is to be interrogated. Any parameter that has a numeric value associated with it such as Start Frequency, Sweep Time, etc., can be interrrogated. The units of the output data are Hz, dBm, dB, or sec., implied with the function selected.

OUTPUT ACTIVE PARAMETER: The 8350A outputs the numeric value of the parameter that is presently active, ie. enabled for value modification from the step keys or data entry. The units of the output data are Hz, dBm, dB, or sec., implied with the function selected.

OUTPUT STATUS: The 8350A outputs 2 sequential bytes, 8 bits wide, that indicate the present instrument status. The first status byte is equivalent to the Status Byte of the Serial Poll (the Status Byte Message), the second status byte is the Extended Status Byte which provides additional information. See the Status Byte Information table for a description of each Status Byte. Status Byte values are cleared upon execution of a Serial Poll (the Status Byte Message), Device Clear (the Clear Message), and/or Instrument Preset function command.

Status Byte Information Table

STATUS BYTE (#1)								
BIT #	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1
FUNCTION	N/A	REQUEST SERVICE (RQS)	SRQ on Syntax Error	SRQ on End of Sweep	N/A	SRQ on Change in Extended Status Byte	N/A	SRQ on Numeric Parameter Altered to Default Value

EXTENDED STATUS BYTE (#2)								
BIT #	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1
FUNCTION	Airflow Failure	*RF Unleveled	Power Failure/on	N/A	N/A	N/A	N/A	Self Test Failed

*Bit/Functions not usable with 86200 Series Plug-ins and 11869A Adapter.

Figure 3-17. HP-IB Only Functions (2 of 7)

SERVICE REQUEST MASK: This determines which bits within the 8350A Status Byte (byte #1) can cause the 8350A to send a Request Service (RQS) Message to the HP-IB controller. The Request Mask is a one 8-bit byte value where with each bit position corresponds to the same bit position as in the 8350A Status Byte. If in the Request Mask byte a bit is set (logical '1') then this condition is enabled for RQS generation. If the bit value is cleared (logical '0') then the bit is ignored. The Request Mask value ranges from decimal 0 to 255 where the decimal value can be determined by summing the decimal values of each Status Byte bit to be enabled (the user need not select the RQS bit). The default at power on is a Request Mask byte of '00000000' or decimal 0. The Request Mask is reset to the default value at power on only and is not affected by an Instrument Preset.

NETWORK ANALYZER TRIGGER (8410B): This causes an external trigger pulse to be generated for the HP 8410B Microwave Network Analyzer to re-phase lock on the present RF signal. This is used to insure proper HP-IB operation in stepped CW frequency sweeps to guarantee that the 8410B is phase-locked at the proper RF frequency after CW settling.

RESET SWEEP: This aborts the present single sweep that is in progress and resets the sweep so that it can be triggered again. This function is enabled only if the 8350A is in the Single Sweep Trigger mode and has the same effect as programming a single sweep trigger ("T4").

TAKE SWEEP: This triggers a single sweep. This function is enabled only if the 8350A is in the Single Sweep Trigger mode and has the same effect as programming a single sweep trigger ("T4").

DISPLAY UPDATE ON/OFF: This selects whether or not the 8350A updates its numeric displays upon further programming of any parameter with a numeric value. The function reduces the amount of time involved in programming the 8350A numerically related parameters (ie. CW Frequency) and aids in producing faster stepped CW frequency sweeps. The default at power on and Instrument Preset is the Display Update On state. When in the Display Update Off state, the 8350A numeric displays will be blanked.

FM SENSITIVITY (83500 Series Plug-ins Only): This selects the External FM Input sensitivity of −20 MHz per volt or −6 MHz per volt. This function is normally selected with an internal plug-in switch but can be overriden via the HP-IB. Note that the FM sensitivity is reset to the switch position after an Instrument Preset is executed. Thus the user should select the desired sensitivity after every Instrument Preset.

LIMITATIONS/CONCERNS

1. When using the Micro Learn String (both Input and Output), the 8350A must be in the CW mode and the plug-in CW Filter capacitor should be off.

2. You must exit the Input Micro Learn String mode with the "M0" code only. The numeric displays will still be blanked until the appropriate functions are re-activated.

Figure 3-17. HP-IB Only Functions (3 of 7)

3. All Learn String and Micro Learn String characters must be retained and re-input to the 8350A. If the 8350A does not receive the expected number of characters it will undergo an Instrument Preset.

4. The valid functions for the Output Interrogated Parameter are: FA, CW, CF, DF, FB, VR, SHVR, M1, M2, M3, M4, M5, SHM1, SF, SM, ST, PL, PS, SL, and SP.

5. The Request Mask byte value is reset only when another value is programmed. It is unaffected by Instrument Preset.

6. The plug-in FM Sensitivity range is reset after an Instrument Preset to the value selected by the internal switch.

7. The Output Learn String, Output Micro Learn String, Output Mode String, and Output Status functions send a Data message consisting of a string of 8-bit binary bytes terminated using the bus END command (EOI and ATN true) with the last byte. The Output Interrogated Parameter and Output Active functions send a Data message consisting of a 14 character ASCII string representing the numeric value in exponential form terminated with a Carriage Return/Line Feed (CR/LF).

   Binary Syntax: [b***b] [EOI]

   Numeric Syntax: [+d.dddddE+dd] [CR] [LF]

   Where the character 'b' indicates an 8-bit binary byte and 'd' indicates a decimal digit (0 through 9). Note that the binary output format could have bytes that may be misinterpreted as Carriage Returns and/or Line Feeds so the user should defeat the ASCII CR/LF as valid character string terminators and rely on the byte count.

REMOTE FUNCTION PROCEDURE:

Mode	Function	Input		8350A Output Response To Input	Notes
		Prefix	Data		
Display Update On/Off	DISPLAY UPDATE ON	DU1			
	DISPLAY UPDATE OFF	DUØ			
FM Sensitivity	−20 MHz/V	F1			
	−6 MHz/V	F2			

Figure 3-17. HP-IB Only Functions (4 of 7)

REMOTE FUNCTION PROCEDURE:

Mode	Function	Input		8350A Output Response To Input	Notes
		Prefix	Data		
Learn String	OUTPUT LEARN STRING	OL		90 bytes [EOI]	
	INPUT LEARN STRING	IL	90 bytes		
Micro Learn String	OUTPUT MICRO LEARN STRING	OX		8 bytes [EOI]	
	INPUT MICRO LEARN STRING	IX	8 bytes		
Mode String	OUTPUT MODE STRING	OM		25 bytes [EOI]	
Output Interrogated Parameter	OUTPUT INTERROGATE	OP	(Function Prefix)	±d.dddddE±dd [CR/LF]	Valid Functions: FA, CW, CF, DF, FB, M1, M2, M3, M4, M5, VR, SHVR, SHM1, SS, ST, SM, PL, PS, SL, SP
Output Active Parameter	OUTPUT ACTIVE	OA		±d.dddddE±dd [CR/LF]	
Output Status Bytes	OUTPUT STATUS	OS		2 bytes [EOI]	
Request Mask	REQUEST MASK	RM	1 byte		
Reset Sweep	RESET SWEEP	RS			
Take Sweep	TAKE SWEEP	TS			

Figure 3-17. HP-IB Only Functions (5 of 7)

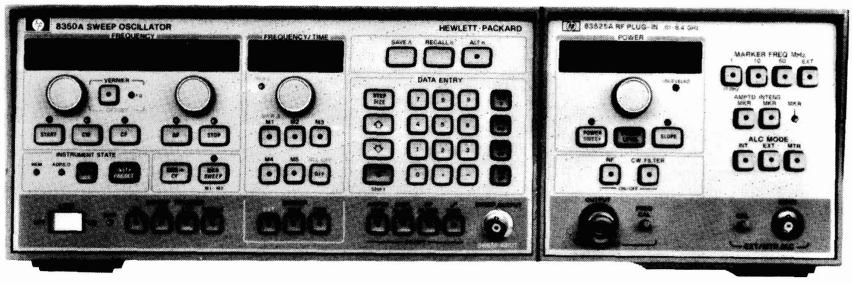
MODE STRING (1 of 2)			
Byte #	**Bit Usage 76543210**	**Example**	**Description**
1	00000000	0	SWEEP MODE: Start/Stop
	00000001	1	CW
	00000010	2	CF/ΔF
2	00000000	0	SWEEP TRIGGER: Int
	00000001	1	Line
	00000010	2	Ext
	00000011	3	Single
3	00000000	0	SWEEP SOURCE: Time
	00000001	1	Man
	00000010	2	Ext
4			MODULATION/BLANKING:
	0000---1	On	Amplitude Mkr On/Off (On=1, Off=0)
	0000--1-	On	Display Blanking On/Off
	0000-1--	On	RF Blanking On/Off
	00001---	On	Sq. Wave Modulation On/Off
5	00000000	0	ACTIVE MARKER #: M1
	00000001	1	M2
	00000010	2	M3
	00000011	3	M4
	00000100	4	M5
6	00000000	0	REFERENCE MAKRER #: M1
	00000001	1	M2
	00000010	2	M3
	00000011	3	M4
	00000100	4	M5
7	000----1	On	MARKERS ON/OFF: M1 (On=1, Off=0)
	000---1-	On	M2
	000--1--	On	M3
	000-1---	On	M4
	0001----	On	M5
8			COUNTER TRIGGER PARAMETER:
	00000000	0	Start Freq.
	00000001	1	Stop Freq.
	00000010	2	Marker Freq.
9			SPECIAL CONDITIONS:
	-------1	On	Non-Swept CW On/Off (On=1, Off=0)
	------1-	On	Default Step Size On/Off
	-----1--	Yes	Vernier Negative Yes/No (Yes=1, No=0)
	----1---	Yes	Offset Negative Yes/No
	---1----	On	Mkr Δ Mode On/Off
	--1-----	On	Mkr Sweep Mode On/Off
	-1------	On	Counter Trigger On/Off
	1-------	On	Alt. Sweep On/Off
10			KEYBOARD ASSIGNMENT:
	00000000	0	Start
	00000001	1	Stop
	00000010	2	CW/CF
	00000011	3	ΔF
	00000100	4	Vernier
	00000101	5	Offset
	00000110	6	Markers

Figure 3-17. HP-IB Only Functions (6 of 7)

MODE STRING (2 of 2)			
Byte #	**Bit Usage 76543210**	**Example**	**Description**
10 (Cont'd)	00000111	7	Step Size
	00001000	8	Sweep Time
	00001001	9	Manual Sweep
	00001010	10	Save/Recall/Alt
	00001011	11	Hex Entry Address
	00001100	12	Hex Entry Data
	00001101	13	Key Test
	00001110	14	HP-IB Address
	01111111	127	None
	01000000	128	Power Level
	01000001	129	Power Sweep
	01000010	130	Slope
11	00000000	0	ALTERNATE REGISTER #: 0
	00000001	1	1
	00000010	2	2
	00000011	3	3
	00000100	4	4
	00000101	5	5
	00000110	6	6
	00000111	7	7
	00001000	8	8
	00001001	9	9
12	00000000	0	NOT DEFINED
13	00000000	0	ALC Mode: Int
	00000001	1	Ext
	00000010	2	Mtr
14	000000-1	On	POWER CONTROL:
	0000001-	On	CW Filter On/Off (On=1, Off=0)
			Power Sweep On/Off
15	000000-1	On	POWER FUNCTIONS:
	0000001-	On	Slope On/Off (On=1, Off=0)
			Power Sweep On6Off
16	000000-1	On	CRYSTAL MARKER MODES:
	0000001-	On	Amplitude Mkr On/Off (On=1, Off=0)
			Intensity Mkr On/Off
17	00000000	0	CRYSTAL MARKER FREQUENCY:
	00000001	1	1 MHz
	00000010	2	10 MHz
	00000011	3	50 MHz
			Ext Freq
18	00000000	0	FM INPUT SENSITIVITY:
	00000001	1	−20 MHz/V
			−6 MHz/V
19	00000000	0	NOT DEFINED
20	00000000	0	
21	00000000	0	
22	00000000	0	
23	00000000	0	
24	00000000	0	
25	00000000	0	
END OF MODE STRING			

Figure 3-17. HP-IB Only Functions (7 of 7)

8350A SWEEP OSCILLATOR



HEWLETT PACKARD

8350A
SWEEP OSCILLATOR

MANUAL PART NO. 08350-90001
Microfiche Part No. 08350-90002

Printed: AUGUST 1980

HEWLETT PACKARD

LOCAL OPERATION

INTRODUCTION

This Local Operation handbook provides information on the local use (non HP-IB) of the 8350A Sweep Oscillator with 83500 series Plug-ins. Throughout this handbook are blocks of example procedures on implementing some of the information. The front panel controls are divided into function groups. These groups and and other information topics are arranged in the following sequence:

- GETTING STARTED – Brief example of control usage.
- INSTRUMENT PRESET – Error codes and preset conditions.
- DATA ENTRY – Numeric, step, units, and shift keys.
- FREQUENCY – Mode selection, vernier and offset.
- FREQUENCY/TIME – Markers and sweep control.
- SAVEn/RECALLn/ALTn – Storage Registers, Step Up Advance.
- DISPLAY FUNCTIONS — Blanking, Modulation, and Sweep Out/In.
- 83500 SERIES PLUG-INS – Power, signal, and crystal markers.
- USE WITH SPECIFIC MEASUREMENT EQUIPMENT:
  HP 8755S Frequency Response Test Set
  HP 8410B Network Analyzer
  HP 7010B and other X-Y Recorders
  HP 5343A Frequency Counter
- APPENDIX 1 – Rear panel connector information.
- APPENDIX 2 – Use of 86200 series Plug-Ins with 11869A Adapter.
- APPENDIX 3 – Summary of Sweep Oscillator front panel controls with fold-out front panel drawing.

GETTING STARTED

NOTE

If a 86200 series RF Plug-in and 11869A Adapter are used, the plug-in coding on the adapter must be set properly to get the correct frequency display.

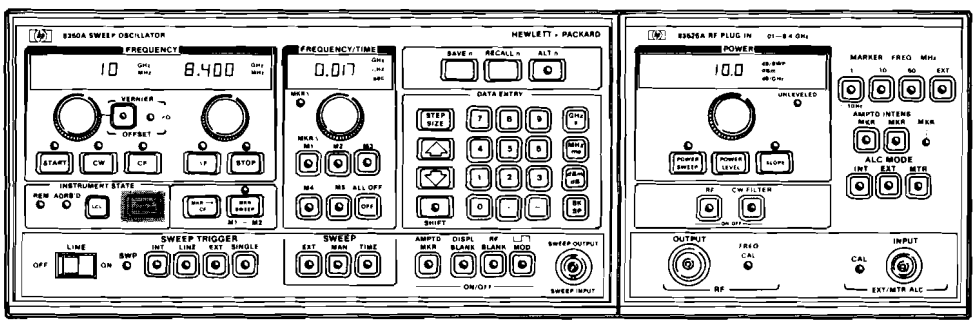
When the 8350A is turned on or when the INSTR PRESET key is pressed the front panel of the 8350A is set to the following pre-determined state: The RF output is swept over the full frequency range of the plug-in at the maximum specified leveled output power, minimum sweep time for the RF Plug-in installed, and the internal square wave amplitude modulation is off.

Example:

8350A with 83525A 0.01-8.4 GHz Plug-in

To change from the INSTR PRESET state to 4.2 to 6.2 GHz sweep (in START/STOP mode), 0.20 second sweep time, +4.5 dBm output power, 27.8 KHz square wave modulation on RF output:

1. Press the **START** key and then rotate the START control clockwise to increase the start frequency until the display above the START key reads 4.200 GHz
2. Rotate the STOP control counterclockwise to decrease the STOP frequency to 6.500 GHz.
3. Press the **TIME** key, then turn the FREQUENCY/TIME control clockwise to increase the sweep time to 0.2 second (displayed on the FREQUENCY/TIME display).
4. Press **MOD** key to activate the internal 27.8 KHz square wave modulation. The lamp in the center of the key will be on.
5. Press the **POWER LEVEL** key, then turn the plug-in POWER control until the display reads +4.5 dBm.



INSTRUMENT PRESET

This condition occurs when the power is turned on or when the INSTR PRESET key is pressed.

INSTR PRESET causes an internal self test to occur after which the instrument will be set to the preset condition. If certain internal errors or failures are detected during the self test or during normal operation of the 8350A they are indicated via error codes in the form "Ennn" (where n= 0, . . . , 9) read from the left FREQUENCY display. For a complete description of the error code listing see the Operating and Service Manual Section 8. The error codes are:

E001 Plug-in interface failure. Check plug-in.

E002 Sweep voltage DAC/Marker voltage DAC failure

E003 Tuning voltage DAC/Marker voltage DAC failure

Figure 1. Instrument Preset Key (1 of 2)

E004 Power supply failure

E005 Instrument interface bus failure

E006 Front panel bus failure

E007 ROM failure
E008
E009
E010

E011 RAM failure
E012
E013
E014

E015 Microprocessor failure

E016 Insufficient cooling. Check fan.

If the self test completes without errors the instrument presets to:

SWEEP MODE: START/STOP, over full frequency range of plug-in

SWEEP TIME: fastest allowable for plug-in

MARKERS: off

MODULATION: off

SWEEP TRIGGER/SWEEP: INT, TIME

VERNIER/OFFSET: 0 MHz

DISPLAY BLANKING: on

SAVE/RECALL: Initial power on sets all memory locations to INSTR PRESET state, if using 8350A Option 001 (Non−Volatile Memory) or if instrument is already on, the memory values remain unchanged when INSTR PRESET is pressed.

ALL OTHER FUNCTIONS: off

When using 83500 series Plug-ins:

POWER LEVEL: maximum specified leveled value

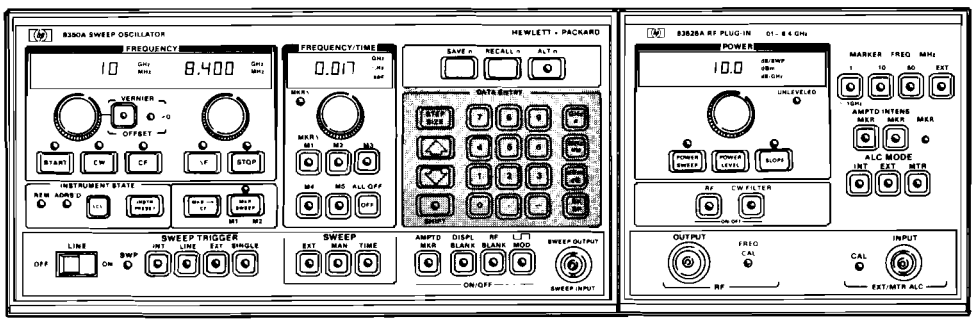
RF and CW FILTER: on

ALC MODE: INT

CRYSTAL MARKERS: off (83522A, 83525A only)

ALL OTHER FUNCTIONS: off

Figure 1. Instrument Preset Key (2 of 2)



DATA ENTRY

This section contains the numeric keyboard, terminators (i.e., GHz, seconds, dBm), step size/up/down, backspace and shift keys. In addition to using the appropriate control, a function value can be set to an exact value or incremented by a specific amount via the keyboard.

Number/unit keys

These keys are used to enter values of frequency, time or power. Holding a number key down causes it to repeat.

Example:

To enter a START frequency of 1.870 GHz:

Press **START** 1 . 8 7 **GHz/sec**

or

START 1 8 7 0 **MHz/ms**

to enter the equivalent frequency in MHz.

Backspace Key BK SP. Prior to pressing a units key the value entered from the keyboard may be changed via the BK SP key without effecting the current instrument state. The backspace key allows the user to alter digits already entered.

Step UP and Step DOWN keys

These keys increment or decrement the active parameter (including memory registers) by the STEP SIZE or preset amount. By holding either key down the 8350A will continue to step

Figure 2. Data Entry (1 of 2)

therefore eliminating the need for the user to repeatedly press the step keys. The STEP UP function may be engaged via the remote STEP UP ADVANCE on the rear panel Programming Connector. The STEP UP ADVANCE is incremented by supplying contact closure to ground or logical 0 to pin 22.

STEP SIZE

This key is used to enter a frequency or power increment to be used with the UP or DOWN key. The STEP SIZE key is pressed before the quantity is entered. A frequency step that is entered is common for START, STOP, CF, CW, ΔF, VERNIER, OFFSET, MARKER and MANUAL SWEEP parameters. A power step is used for varying POWER LEVEL, POWER SWEEP and SLOPE. Default values are assigned at power on and instrument preset for step sizes until new values are entered. Note that a step size cannot be set for sweep time. The keyboard and step keys affect the last active function. The entered Step Size is not displayed.

Example:

To set a 250 MHz step size:

Press **STEP SIZE** **2** **5** **0** **MHz/ms**

After this, each time the UP or DN key is pressed the active frequency parameter will change by 250 MHz.

SHIFT key (BLUE)

This key is used to activate the functions coded in blue and some special functions. The lamp in the center of this key is on when the key is active.

Example:

Press **M1** **M2** **M3** **M4** **M5**

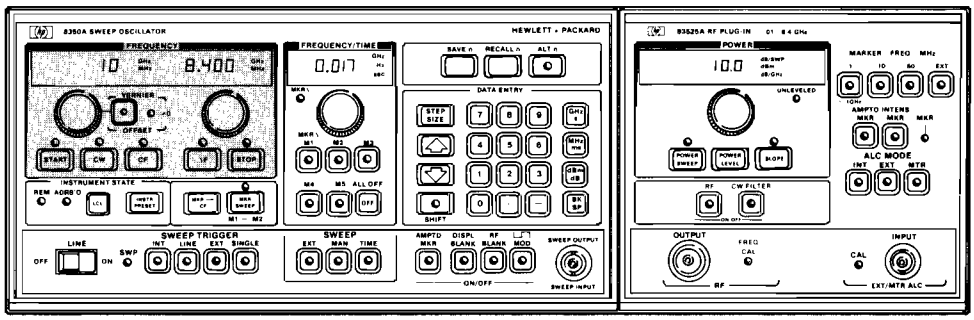
(MARKERS) ALL OFF. Pressing SHIFT, OFF turns off all markers.

The SHIFT key is also used to set the HP-IB address. Press SHIFT LCL ; the FREQUENCY/ TIME display will indicate the present HP-IB address number. The address may be changed to any value between 0 and 30 by using the keyboard to enter a number and the GHz, MHz or dBm key as a terminator. The 8350A is factory preset for an HP-IB address of 19.

NOTE

Address number 21 is normally reserved for calculator addressing and HP-IB interface functions and should not be used.

Figure 2. Data Entry (2 of 2)



FREQUENCY

This section controls the sweep mode and frequency limits.

START/STOP

When either the START or STOP key is pressed the sweep oscillator is put in START/STOP mode. Swept RF output begins at START frequency and ends at STOP frequency. The START frequency must be less than or equal to the STOP frequency. The vernier and offset can be used to change the effective center frequency of the sweep. Left FREQUENCY display is start frequency of sweep; right FREQUENCY display is stop frequency. Frequencies may be changed in three ways.

- Frequency controls – Provides continuous adjustment. Clockwise rotation increases frequency.
- Data entry – Can enter specific frequency values from the number/units keyboard.
- Step up/down – enter step size (in GHz or MHz) using DATA ENTRY keyboard section. By first pressing the appropriate key (START or STOP) and then the UP or DOWN key can now increment or decrement the appropriate frequency sweep limit. If a step size has not been entered the function will change by the default value when UP or DOWN is pressed.

CF (CF/ΔF)

Puts display in mode where swept output is read as a center frequency and frequency sweep width. Output is swept from CF−ΔF/2 (start frequency) to CF+ΔF/2 (stop frequency). When changing between CF/ΔF and START/STOP modes only the method of display changes, the swept RF output remains the same.

When either CF or ΔF is activated the left display is center frequency (CF), the right display is delta frequency (ΔF). Both the CF and ΔF can be changed via the appropriate control, number/units keyboard and step size keys.

CW

When activated causes the 8350A to output a constant frequency. The value of the CW frequency is displayed on left FREQUENCY display. The CW frequency is the same as the center frequency (CF) of the previous swept range. The CW frequency value can be changed using the

Figure 3. Frequency Controls (1 of 2)

control, data entry keyboard or step keys. In CW mode, the SWEEP OUT voltage is equal to percent of full band. Pressing SHIFT, CW enters a "swept" CW mode with the SWEEP OUT being a 0 to 10 volt ramp that results in the display trace being a flat horizontal line. This is often useful when reading values (e.g., dB of attenuation) from a CRT screen when at a CW frequency.

FREQUENCY VERNIER

The effective center frequency of any mode (CW or swept) may be adjusted with high resolution up to ±0.05% of the frequency band being used with the vernier. Pressing the VERNIER key activates the function and sets the left FREQUENCY display to read the vernier value in MHz.

1. "≠0" light is on whenever a frequency vernier or frequency offset is present in any mode. After setting vernier, to return to the previous mode, press the appropriate key (e.g., START, CF, etc.) and the display will return to reading the appropriate frequencies and the "≠ 0" lamp will be lit.

2. Frequency vernier can be set by the control, data entry keyboard or step keys.

3. The displayed vernier adjustment can be up to ±0.05% of the frequency band being swept. When in a sub-band of a multiband plug-in (for example, the 0.01-2 GHz band of the 83525A .01-8.4 GHz plug-in) the adjustment range will be ±0.05% of the sub-band. This feature allows for better frequency resolution than would otherwise be possible with the vernier when using a multiband plug-in.

4. The vernier adds its value to the appropriate frequency parameter and then resets to zero when the adjustment exceeds ±0.05% for continuous adjustment.

5. ZEROING VERNIER. To set the vernier to zero, press VERNIER 0 MHZ/ms and the"≠0" lamp will turn off.

FREQUENCY OFFSET

The frequency offset feature allows the CW frequency and/or the effective center frequency of the swept range to be shifted by any amount up to the full range of the plug-in.

1. To enter an offset press SHIFT VERNIER and enter the offset by either the left FREQUENCY control or data entry keyboard. The amount of offset (in GHz or MHz) will be shown in the left FREQUENCY display and the "≠0" lamp will be lit.

2. To exit the displayed offset mode press the appropriate mode key (i.e., START, CW, etc.). The sweep limits displayed will appear to be unchanged, however the "≠ 0" lamp will be on indicating the offset is present and the actual RF output frequency will be shifted.

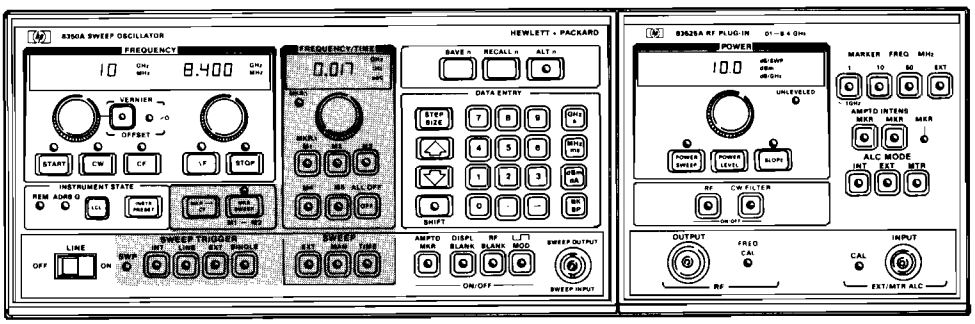
3. To return display or adjustment the frequency offset press SHIFT VERNIER. To zero the offset press SHIFT VERNIER 0 MHz.

OVERRANGE

The 8350A will permit frequency sweeps beyond the specified range of the plug-in by ±2.0% of the plug-in bandwidth. However, plug-in performance in the overrange condition is unspecified.

As a warning of the frequency overrange condition the GHz or MHz annunicator will flicker in the appropriate function display.

Figure 3. Frequency Controls (2 of 2)



FREQUENCY/TIME

This display will read either GHz, MHz or sec depending upon the presently active function and range. This section controls five mainframe markers, manual sweep, and the sweep time. The five independent frequency markers can be displayed simultaneously as intensified dots on a CRT using the Z-axis or amplitude dips on the RF output.

SWEEP

Controls the rate at which the RF output is swept.

TIME. When the TIME key is pressed the output is swept at the user-specified or default rate. If time key is lit but display reads GHz/MHz or is blank, press TIME key again and display will read seconds. The mainframe can allow sweep times from 100 seconds to 0.01 second although the minimum sweep time is dependent on the plug-in being used and bandwidth being swept.

When display reads seconds, sweep time can be adjusted with the control knob or data entry keyboard. The step keys can be used to adjust the sweep time in a 1-2-5 sequency.

MANUAL SWEEP(MAN). FREQUENCY/TIME display will read GHz/MHz. By using the FREQUENCY/TIME control, step keys or data entry keyboard, it is possible to manually sweep the frequency range with the display indicating the present output frequency.

EXTERNAL SWEEP(EXT). The 8350A can be swept via an external voltage. Apply 0 to 10 volts into sweep output/input (can use BNC connector on front or rear panel) with 0V input corresponding to the lower frequency limit of the sweep range and 10V corresponding to the upper limit. DC sweep input voltages will cause CW frequency outputs. Markers and blanking outputs are disabled when in external sweep mode.

SWEEP TRIGGER

Controls when the sweep will begin in the timed sweep mode. The sweep light, SWP, is lit when the sweep is occurring.

INT. Sweep triggered internally, free running.

LINE. Sweep triggered by power line frequency.

Figure 4. Frequency/Time Controls (1 of 3)

EXT. The sweep can be triggered externally by applying a positive going signal from 0 to 2 volts minimum, +20 volts maximum to Programming Connector pin 9. The trigger signal must be wider than 0.5 microsecond at less than a 1 MHz repetition rate.

SINGLE. This key selects single sweep mode and aborts present sweep when first pressed. Subsequent keying will trigger or abort single sweeps at current sweep time.

MARKERS

Any or all of the five markers (M1 through M5) may be enabled by pressing the marker key corresponding to the marker desired. When a marker is activated it is set to its last active frequency unless INSTRUMENT PRESET has been activated in which case the marker will be set to the center of the fullband sweep. A marker can be in one of three states:

- ACTIVE – Lamp in center of key flashing.
- ON – Lamp on.
- OFF – Lamp off.

Only one marker at a time (the "active" marker) can have its value altered. The five mainframe markers are normally supplied through the positive Z-axis blanking pulses connector on the rear panel. By pressing the AMPTD MKR key the markers may be displayed as amplitude dips on the RF output.

- When a marker is active the keyboard, FREQUENCY/TIME control and step keys can be used to modify its value. The value of the active marker in GHz/MHz is displayed.
- By pressing OFF, the active marker only will be turned off. If multiple markers are on, the remaining lamps will remain lit although the display will go blank.
- A marker may be initially activated or returned to active state by pressing the corresponding marker key.
- All markers may be turned off simultaneously by pressing SHIFT, OFF.

Example:

Press M3 (Note M3 lamp flashing other lamps off.)

Press M5 (Note M5 lamp flashing, M3 lamp on and other lamps off.)

MKR (Marker) SWEEP. In this mode the RF output is swept between markers M1 and M2. The lamp over the key will be on. Marker 1 must be less than or equal to Marker 2 in frequency (if M1 is greater than M2 the values of M1 and M2 are permanently interchanged). By varying the active marker (1 or 2) or by turning the START/STOP controls the sweep limits can be altered. When both M1 and M2 are not on, the sweep occurs between the most recent values of M1 and M2. To exit this mode press MKR SWEEP and the lamp over the key will go out. Pressing SHIFT, MKR SWEEP causes the values of M1 and M2 to become the START/STOP frequency values permanently.

Figure 4. Frequency/Time Controls (2 of 3)

MARKER-TO-CENTER FREQUENCY (MKR→CF). When this key is pressed the frequency of the active marker becomes the center frequency of the swept output. The frequency span remains unchanged if within the frequency limits of the plug-in. If original frequency span exceeds plug-in limits, the frequency span will be reduced to retain symmetry.

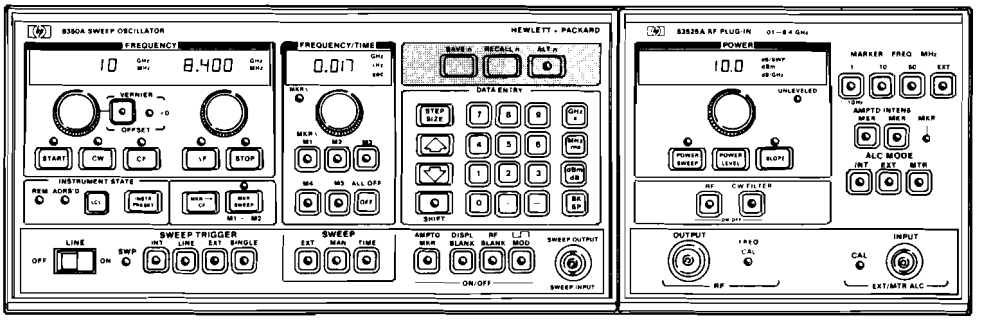
MKR Δ. This function allows the frequency difference between any two markers to be displayed and the trace between them intensified (if intensity markers are selected).

1. Press SHIFT M1 the display shows the frequency difference between the currently active marker and the one that was previously active.
2. The FREQUENCY/TIME control, keyboard and step keys can change the active marker value.
3. To exit MKR Δ mode press OFF.

Example:

1. Press M4 and set frequency via DATA ENTRY keyboard or Control to 2 GHz.
2. Press M2 and set frequency via DATA ENTRY keyboard or Control to 2.4 GHz.
3. Press SHIFT MKR Δ (Note Frequency/Time display reads difference between Marker 4 and Marker 2, 400 MHz).

Figure 4. Frequency/Time Controls (3 of 3)



SAVEn/RECALLn/ALTn

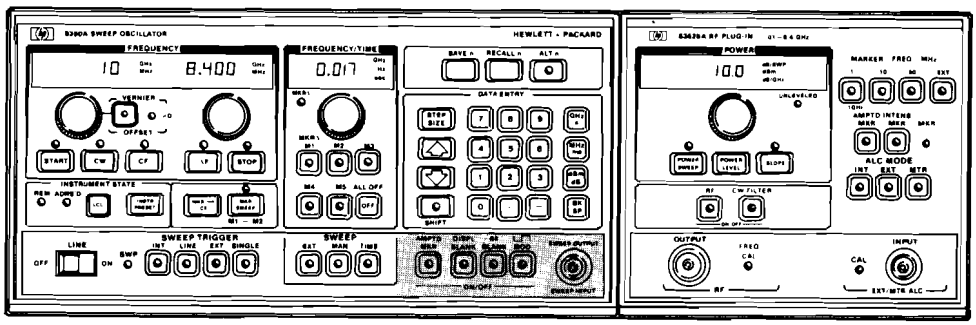
SAVEn/RECALLn

The 8350A is equipped with memory registers which allow up to nine complete front panel settings (frequency range, markers, power level, etc.) to be stored and later recalled. Instrument settings are stored in memory locations 1 through 9 by pressing SAVEn and 1, . . . , or 9. To recall a stored instrument setting press RECALLn and 1, . . . , or 9. The STEP keys may be used to step through the stored registers. The instrument settings stored in memory may be recalled remotely in sequence by using the Step Up Advance on pin 22 of the Programming Connector on the rear panel of the 8350A. A contact closure to ground or logic 0 is used to implement this function.

ALTn

ALTn causes the 8350A to alternate between the current instrument state and the setting stored in memory location n (where n=1, . . . ,9) on successive sweeps. When the 8350A is in this mode the lamp will be on and the SAVEn and RECALLn keys disabled. To exit from the ALTn mode press the key again, the lamp wil turn off and the SAVEn/RECALLn keys will become operational. When using the 8350A with an HP 8755C Swept Amplitude Analyzer, channel 1 displays the current instrument state and channel 2 displays the stored setting (provided the 8350A/8755C ALT SWP INTERFACE cable is connected).

Figure 5. Save n, Recall n, and ALT n Keys



DISPLAY FUNCTIONS

AMPTD MKR, DISPL BLANK, RF BLANK. (Function in effect when lamp in center of key is lit)

DISPL BLANK ON/OFF. Blanks the display during the retrace via the POS Z BLANK or NEG Z BLANK outputs.

RF BLANK ON/OFF. Blanks (turns off) the RF power during the retrace.

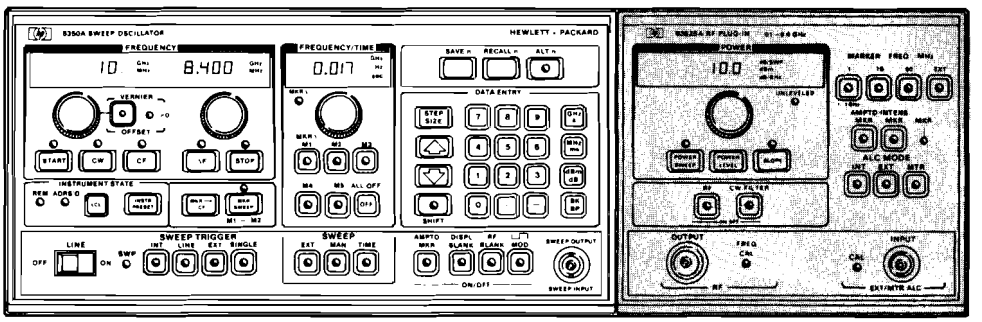
⊔⊓MOD ON/OFF. Activates the internal 27.8 KHz square wave amplitude modulation of the RF output. This feature makes the 8350A directly compatible with the HP 8755 Frequency Response Test Set. The 8350A may be modified via an internal jumper to provide 1000 Hz square wave amplitude modulation for instruments like the HP 415E SWR Meter (refer to the Operating and Service Manual, Section 5).

SWP (Sweep) OUTPUT/SWP (Sweep) INPUT (BNC connection).

SWP (Sweep) OUTPUT. Supplies a 0 to 10 Volt signal when 8350A is in MAN or TIME sweep mode. 0V output is at the start frequency of sweep, 10V output is at the stop frequency of sweep. In CW mode the output is a dc voltage proportional to the percent of full band. Can be used to drive the X-axis on a CRT or X-Y recorder.

SWP (Sweep) INPUT. Used when in EXT SWEEP mode. Supplying a dc voltage will tune RF where 0 volts tunes to the lower frequency of the set sweep and 10 volts tunes to the upper frequency. The input can be a ramp for a swept output or DC for a CW frequency. The display and RF blanking must be off when externally sweeping.

Figure 6. Display Function Keys



83500 SERIES PLUG-IN

Power Control

POWER LEVEL. When pressed, the plug-in display indicates the RF output power. The output power may be varied using the POWER control, keyboard or step size keys. Note that the internal leveling must be on and the unleveled light out for calibrated output power. The power is typically calibrated over a 15 dB range (80 dB with plug-in Option 002, Step Attenuator).

SLOPE. Compensates for high frequency power losses in external RF cables by increasing the power at higher frequencies. This compensation provides a flat RF signal output at the end of a cable or test set. Press SLOPE and the display will indicate the dB per GHz of the present sweep of compensation desired. Use the POWER control, keyboard or step keys to enter the amount of slope. Press SLOPE again to remove all compensation.

POWER SWEEP. This function enables the output power to be swept up. The maximum calibrated power sweep range is typically 10 dB. Note that when using plug-ins with Option 002 Step Attenuator, the power cannot be swept across the internal attenuator switch points. The procedure for performing a power sweep is:

1. After selecting the output frequency (sweep range or "swept" CW mode) use the power level to set the starting value for the power sweep.

2. Press the POWER SWEEP key, the display will now read the dB/SWP. By using the POWER control, data entry keyboard or step keys set the desired sweep range. Press the POWER SWEEP key again to turn the power sweep off.

Figure 7. Plug-in Controls (1 of 2)

Signal Control

RF ON/OFF. Turns the RF power on and off.

CW FILTER ON/OFF. When on, this filters the internal oscillator's tuning voltage to provide a more stable CW or MANUAL SWEEP frequency output. During swept operation this filter is always disabled.

ALC (Automatic Level Control) Mode: INT, EXT, MTR

INT. Provides internal leveling of output power at the output connector. The 83500 series Plug-in must be on INT leveling for calibrated output power.

EXT. This setting is used when leveling with an external crystal/diode detector. The front panel EXT ALC input accepts negative voltages in the −25 to −250 millivolt range (typically).

MTR. Used when leveling output power with an HP 432A/B/C Power Meter.

CAL. Adjusts the ALC gain so the display can be calibrated by an external power meter or detector.

CRYSTAL MARKERS (83522A, 83525A Plug-ins only)

50, 10, and 1 MHz crystal frequency marker combs are available. The 50 and 10 MHz are available at frequencies less than 2 GHz while the 1 MHz markers are available under 1 GHz.

AMPTD/INTENS. The markers can be set to be amplitude dips (on the RF output) and/or intensified spots (on the Z-axis of the CRT) or both. They are independent of the mainframe markers.

EXT (External Marker). An external frequency marker can be input through the rear panel of the plug-in. The marker appears when the RF output frequency equals the marker frequency. The external marker input power should be between −10 dBm and +10 dBm.

MKR Lamp. When the 8350A is in CW or manual/external sweep mode the MKR Lamp will light when the CW frequency is at a marker frequency. Useful when an accurate CW frequency reference is desired and to calibrate plug-ins.

RF OUTPUT CONNECTOR

Type N female. The 83570A 18 to 26.5 GHz Plug-in is equipped with a WR-42 waveguide output connector.

Figure 7. Plug-in Controls (2 of 2)

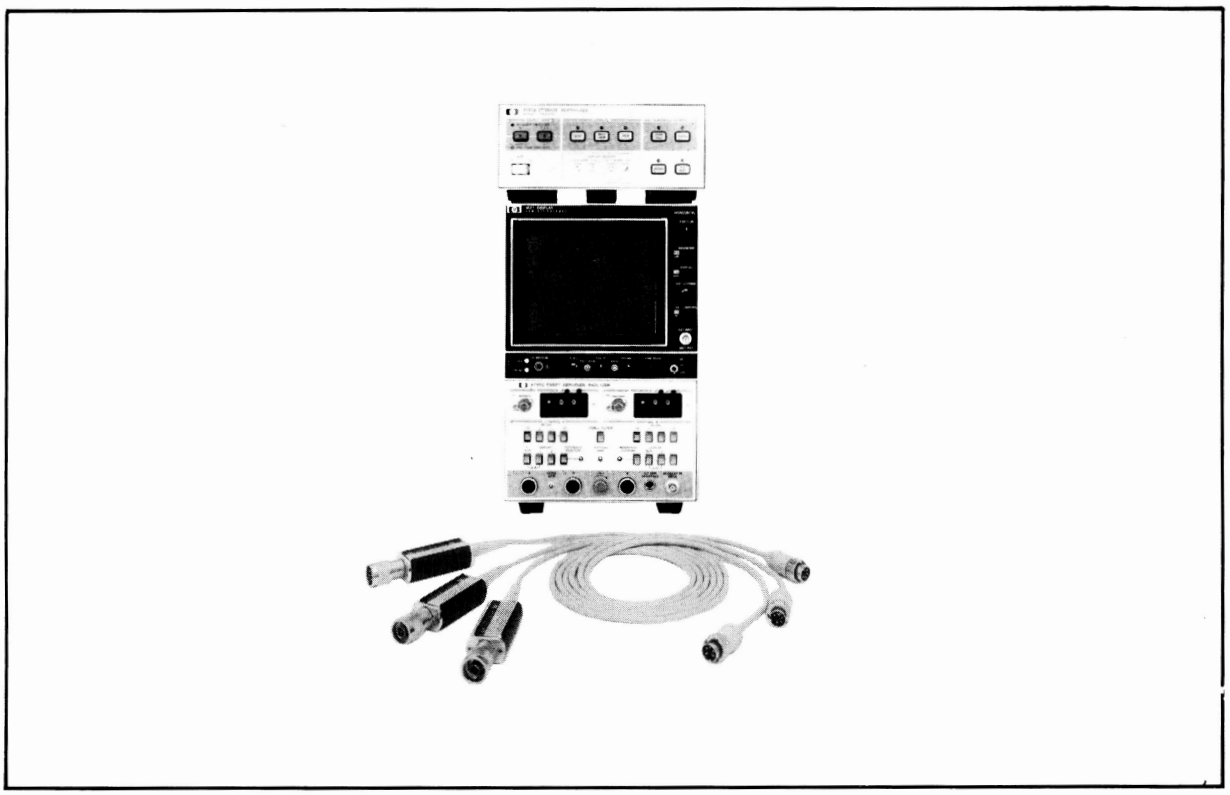


Figure 8. Frequency Response Test Set

INTERFACING THE 8350A WITH SPECIFIC MEASUREMENT EQUIPMENT

8755S FREQUENCY RESPONSE TEST SET

The 8755S consist of:

- 8755C Swept Amplitude Analyzer
- 182T Oscilloscope
- 11664A Detectors (3 each)
- 8750A Storage-Normalizer

The 8755S is used for scalar transmission and reflection measurements requiring up to 60 dB of dynamic range and for absolute power measurement from −50 dBm to +10 dBm.

The 8350A has the following features designed specifically for use with the 8755S Frequency Response Test Set:

RF Square-wave Modulation. By engaging the ⊔⊓MOD key an internally generated squarewave modulation of the RF output is available thus eliminating the need for external modulating equipment. A jumper internal to the 8350A enables the square wave modulation frequency to be changed to 1 KHz (see section 5 of the Operating and Service manual for details).

Alternate Sweep Function. The ALTn function of the 8350A allows two different frequency and power settings to be swept on successive sweeps. The front panel setting and the setting stored in a memory register location n (n=1, . . . ,9) can be selected for alternate sweeps. The Alternate Sweep Function will not work properly with the 8755A or 8755B. See Figure 9 for a sweep display of the ALTn function when used to view a bandpass response at different resolutions and offsets.

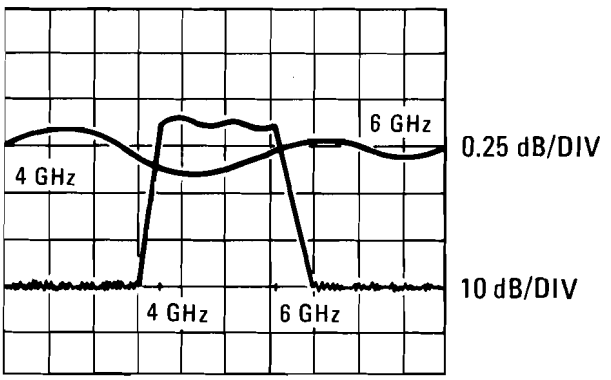


Figure 9. Alternate Sweep Function Display

Some other features enhancing the convenience and versatility of the 8755S are:

Marker Δ. The MKR Δ function is useful when using alternate sweep in overlapping different sweep widths. The overlapping portion of one of the sweeps can have an increased intensity. The 8750A Storage-Normalizer will need to be in BYPASS mode to view Z-axis modulation on the oscilloscope.

Power Sweep. The RF output power may be ramped up when the sweeper is in the swept or "swept" CW mode by using the POWER SWEEP function. See Figure 10 for a gain compression display using power sweep.

Save and Recall. This function allows the storage and recall of nine complete instrument settings.

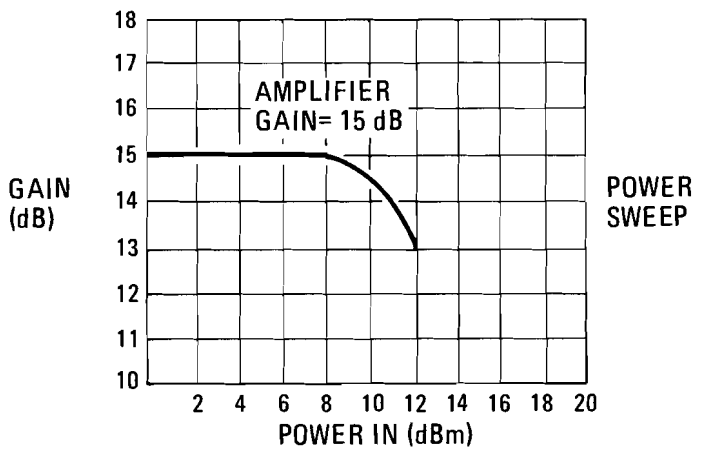


Figure 10. Gain Compression Display

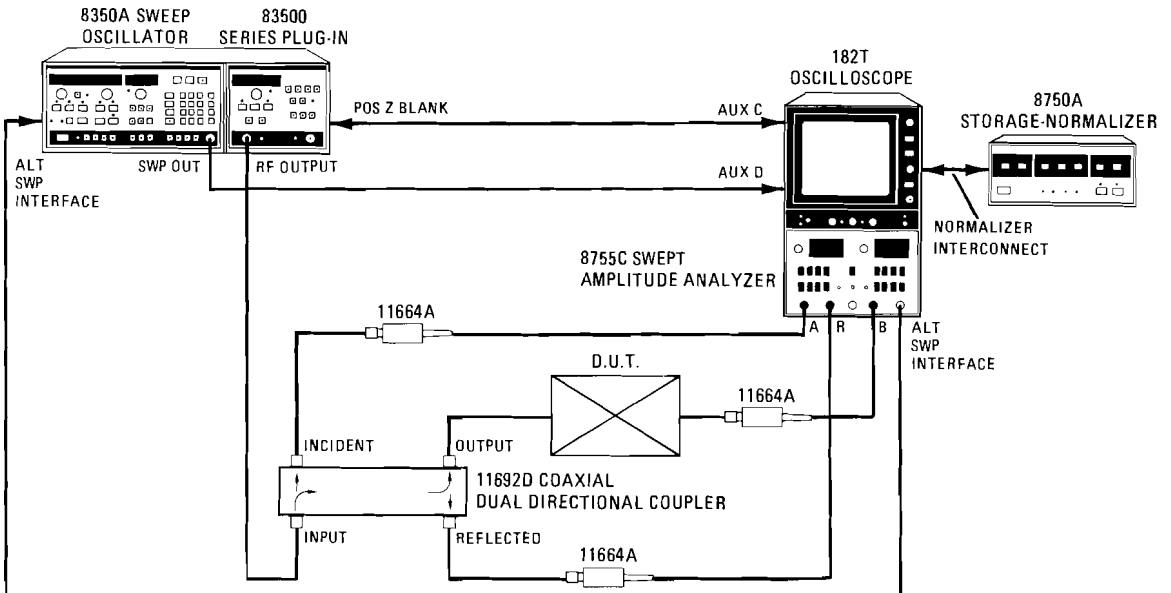
Figure 11 outlines the general procedure used in making a scalar transmission and reflection measurement. The 11692D Dual-Directional Coupler is used in the example but if a 11666A Reflectometer Bridge is available it may be used instead of the Coupler and two detectors (8755S Option 002).

To keep the following procedure brief the 8750A will not be used (switched to BYPASS) in the procedure. The following anomalies exist when using the 8750A with the 8350A Sweep Oscillator:

- The 8350A DISPL BLANK must be engaged to ensure triggering 8750A updating.
- Intensity markers are changed to amplitude markers. In MKR Δ mode they appear as a level shift over the MKR Δ range.
- If an 8755 channel is switched off the trace goes to the reference line (bottom of CRT).

Example:

1. Connect the equipment as shown in Figure 11. Initially, the 8350A should be set by pressing **INSTR PRESET** and **⊓ MOD** (Set to 27.8 KHz) which will set the front panel instrument state and activate the internal square wave modulation.



Notes on connections:

- Either the front or rear panel SWEEP OUT/IN may be used.
- When in ALTn mode both channels 1 and 2 (on 8755) must be on and receiving inputs.

2. Turn off channel 1 on the 8755C by releasing the display pushbutton. Set the 8350A controls as desired . On channel 2 set the function, dB/DIV and Offset desired for viewing the current sweep setting.

3. Set the 8350A controls as desired then store the current 8350A sweep setting in any available memory location. Then turn off channel 2 by releasing its display pushbuttons.

4. Turn on Channel 1 of the 8755C and set the function, dB/DIV and Offset as desired. Set 8350A controls as desired.

5. Turn on channel 2. Press **ALTn** , n and the 8350A will alternate between the two settings on successive sweeps.

Channel 1 now displays the response due to the current front panel setting while channel 2 displays the response to the setting stored in memory location n. The front panel controls of the 8350A are enabled and the current sweep setting may be altered if necessary.

Figure 11. Typical Test Setup Using 8755S

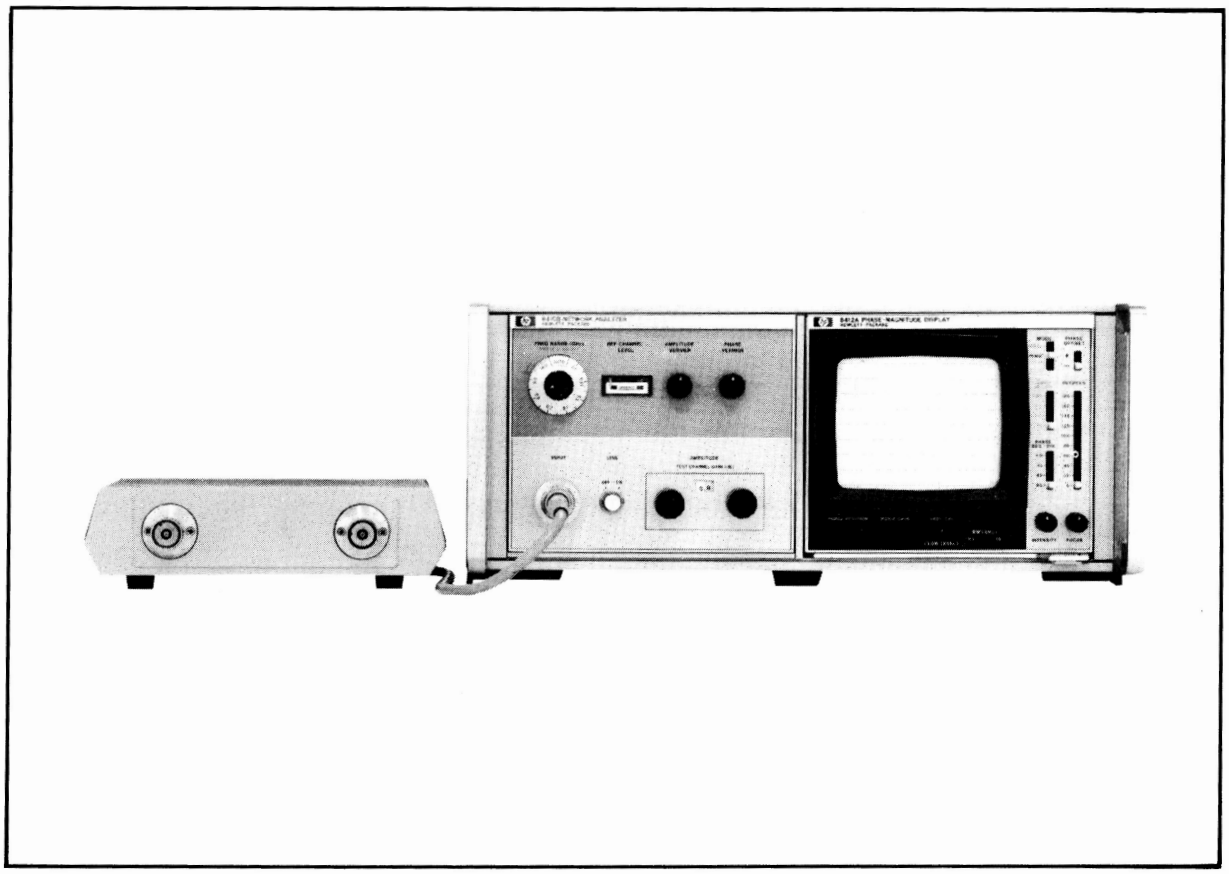


Figure 12. 8410B Network Analyzer

8410B NETWORK ANALYZER

The 8350A is compatible with the 8410B Network Analyzer systems and accessories. The Source Control Cable (HP P/N 08410-60146) synchronizes the two instruments to provide continuous multi-octave coaxial magnitude and phase measurement capability from 110 MHz to 18 GHz with 65 dB dynamic range. The frequency markers can be displayed in polar format as intensity dots (Z-axis). Frequency markers derived from crystal oscillators allow frequency measurements to be made with an accuracy of five parts per million.

Waveguide measurements between 18 and 26.5 GHz can be made with the K8747A Reflection/Transmission Test Unit which is designed for use with the 8410B. This test system utilizes two 8350A Sweep Oscillators and 83570A 18 to 26.5 GHz RF Plug-ins. One sweeper is used as a local oscillator while the second is used to sweep the desired frequency range.

See Figure 13 for an example measurement set up using the 8410B with a single 8350A and 83500 series Plug-in.

The 8410B FREQ RANGE should be set to AUTO. In addition, the sweep time on the 8350A should be slow enough and/or sweep range narrow enough to insure phase locking over entire sweep range.

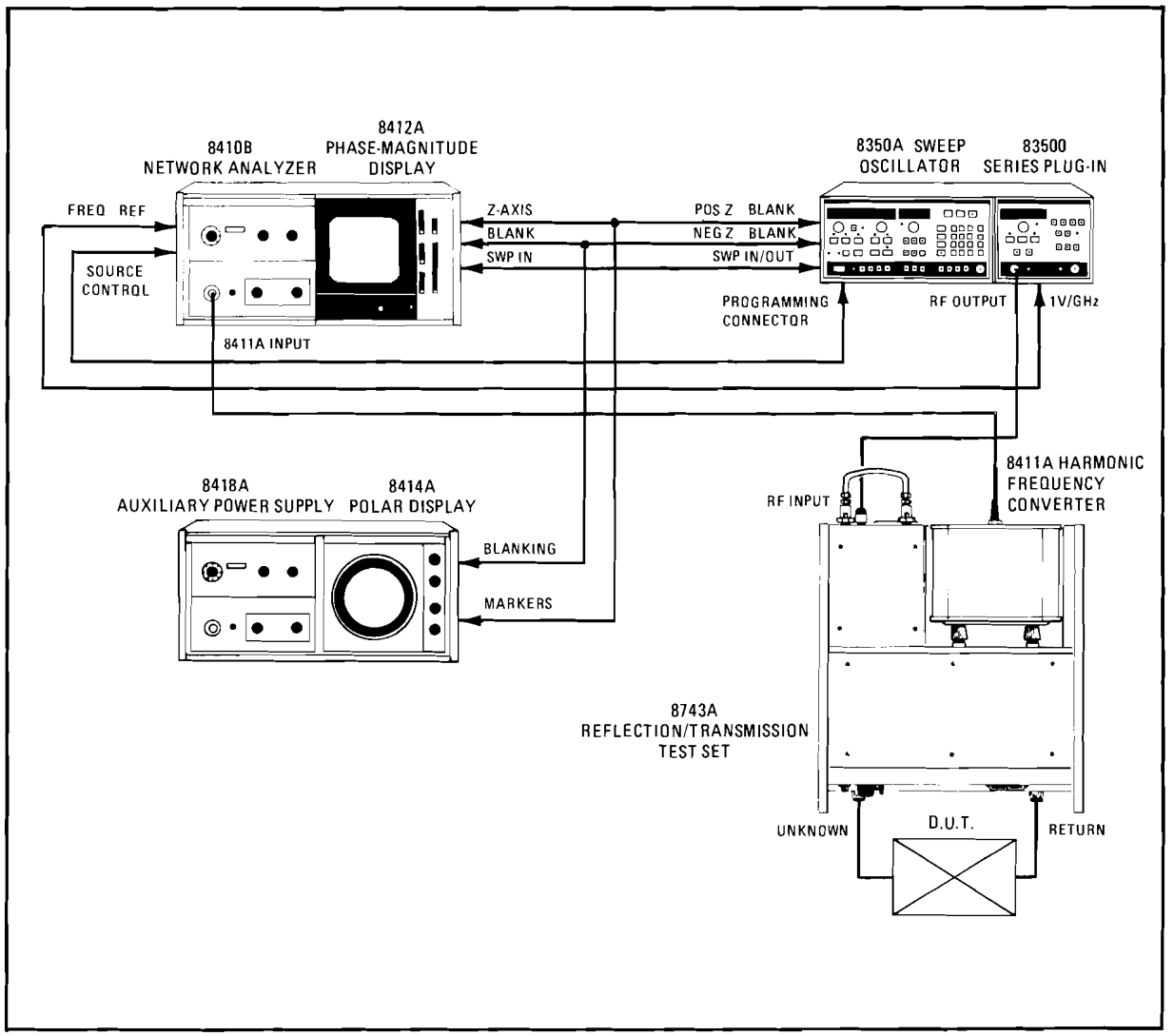


Figure 13. 8350A Connections to 8410

Notes on connections:

- FREQ REF output of the 83500 or 86200 series Plug-ins provides a 1-volt-per-GHz output so that the 8410B may synchronize with the sweep.
- The 8410B display units (8412A, 8414A) require that the NEG Z BLANK from the 8350A be used as the blanking signal.
- POS Z BLANK (from the 8350A line contains the Z-axis markers. This line connects to the MARKERS input on the 8414A Polar Display and to the Z AXIS input on the 8412A Phase-Magnitude Display.
- SWEEP OUT/IN outputs a 0 to +10 volt signal in proportion to the swept or CW frequency output. 0V corresponds to the lower frequency sweep limit; +10V to the upper. Swept RF output causes a ramp voltage out; CW output causes a dc voltage out.This connection is necessary only when using 8412A Phase-Magnitude Display.
- 8350A/8410B SOURCE CONTROL CABLE. Provides "handshake" lines for synchronization between 8350A and 8410B (HP Part No. 08410-60146).

X-Y RECORDERS

The 8350A is equipped with outputs for controlling X-Y analog recorders.

Some of the HP X-Y recorders that may be used with the 8350A are:

7010B/7015B
7035B
7004B/7034A
7044/7045/7046/7047

The available/required signals for proper operation with an X-Y recorder are:

X INPUT – Typically SWEEP IN/OUT. Supplied by BNC connector on front or rear panel.

Y INPUT– Y axis voltage. On 8755S Frequency Response Test Set this would be AUX A for channel 1 or AUX B for channel 2. For 8410B systems, the 8412A display provides amplitude and phase outputs.

PEN LIFT – Signal line for controlling remote pen up/down. Pen up is open contact or +5 volts. Pen down (current sink) is contact closure to ground or 0 volt. Supplied by BNC connector on rear panel or pin #10 on 8350A Programming Connector.

RECORDER (SERVO) MUTE – 7044/7045/7047 only. Control line that mutes the power to the recorder servos for 100 ms at bandswitch (when using multi-band plug-ins) or designated points. Pin #1 on the 8350A Programming Connector.

PEN LIFT REQUEST – Allows a pen lift to be initiated by remote control independent of the present pen lift status. Pin #3 on the 8350A Programming Connector.

INVERSE PEN LIFT – Inverse function of Pen Lift, pin #23 on 8350A Programming Connector.

The pen lift control line is assigned to a pin on the Remote Control connector of the X-Y recorder. For a complete pin assignment listing refer to the Operating Manual for the particular X-Y recorder being used.

Pen lift pin location on X-Y recorders:

Recorder	Pen Lift Pin No.
7010B/7015B	3
7035B	18
7004B/7034A	18
7044A/45A/47A	1
7046A	34

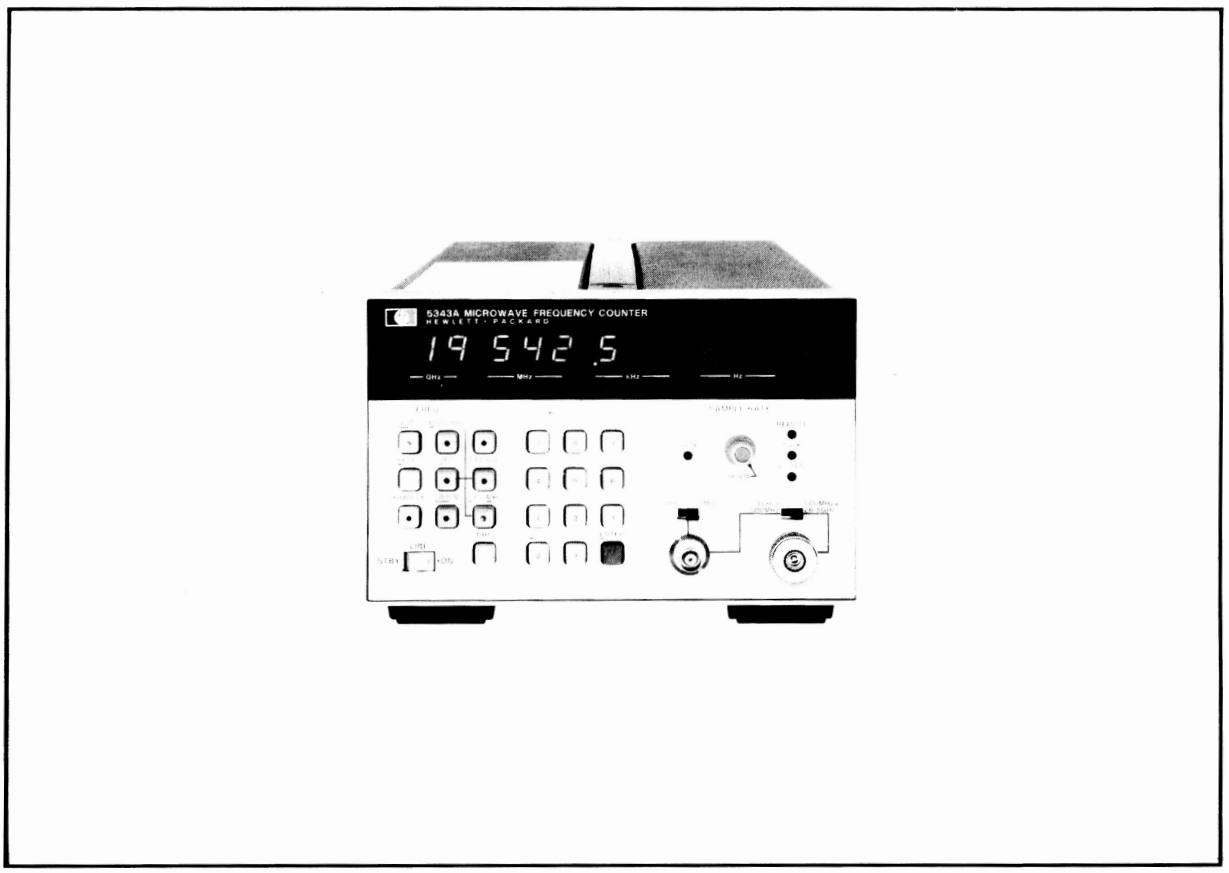


Figure 14.. 5343A Microwave Frequency Counter

5343A FREQUENCY COUNTER

The 5343A Microwave Frequency Counter can be used with the 8350A to measure frequencies in swept mode in addition to normal CW frequency measurements.

During swept operation the 5343A will stop the 8350A sweep and count a selected frequency parameter such as the START frequency, STOP frequency or any frequency markers in the sweep range. To accomplish this, the 8350A and 5343A communicate via two signal lines (Counter Trigger, Stop Sweep on the 8350A and Sweep Interface A and B on the 5343A) that enable the 8350A to externally trigger the 5343A and then allow the 5343A to stop the sweep long enough to gate and count the selected frequency parameter.

See Figure 15 for the test set up.

Measuring CW frequencies

When measuring CW frequencies the CNTR TRIG and STOP SWEEP connections are not necessary. The 5343A should be in the AUTO mode and the internal square wave modulation on the 8350A must be off.

Auxiliary Output

The auxiliary output of an RF Plug-in (if available) may be used with the 5343A. When using the auxiliary output of a multi-band plug-in such as the 83592A (0.01-20 GHz) the frequency multiplier feature of the 5343A may be used so that the proper RF frequency is displayed.

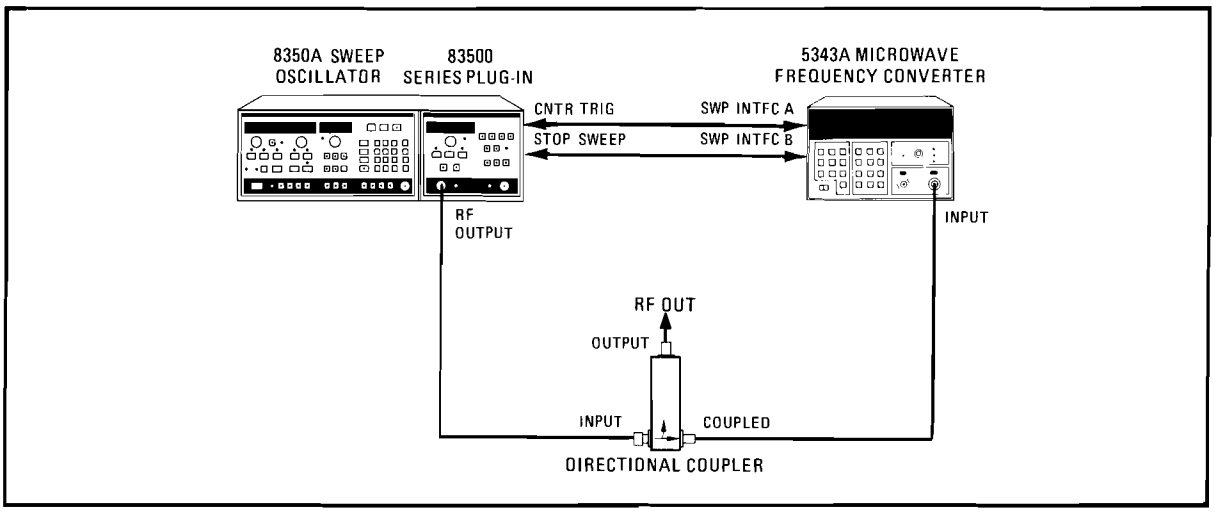


Figure 15. 5343A Test Setup

Notes on connections:

- A power splitter or directional coupler may be used as long as the input to the 5343A does not exceed +7 dBm or go below the minimum sensitivity.
- CNTR TRIG (Counter Trigger): Output for controlling the HP 5343A Microwave Frequency Counter. This allows a frequency count of the selected marker, START or STOP frequency of the present sweep. Connects to the SWP INTFC A (sweep interface, on the rear panel of the 5343A) to externally trigger the counter.
- STOP SWEEP: Input for stopping the progress of the forward sweep. When connected to the SWP INTFC B (sweep interface, on the rear panel of the 5343A) the 5343A stops the sweep long enough for the counter to gate and measure the selected frequency marker, START or STOP frequency. If the internal modulation on the 8350A is on, it is momentarily disabled so that the counter may measure the frequency.

To measure a START, STOP, or marker frequency during a sweep:

5343A: Set to AUTO, SWP M and set desired frequency resolution. Set the rear panel ACQ TIME switch to MED or FAST.

8350A: Select the frequency parameter to be measured by pressing the appropriate key, START, STOP, or any marker Mn (where n=1, . . . ,5) and then press SHIFT M2

If the sweep setting is changed or it is desired to exit this mode, disable the 5343A by pressing SHIFT M3 on the 8350A front panel.

Example:

To measure the START frequency.

1. Connect equipment as shown in Figure 15. Set the 5343A to AUTO, SWP M and set desired frequency resolution.
2. Press the 8350A INSTR PRESET START SHIFT and M2 keys. The 5343A will temporarily stop the sweep, measure the frequency and display it at the desired resolution.

APPENDIX 1
REAR PANEL CONNECTIONS.

For a diagram of the rear panel see Figure 16.

POS Z BLANK. Positive Z axis blanking signal. Supplies a rectangular pulse of approximately +5V into 2500 ohms during the retrace and bandswitch points of the RF output. Also supplies a −5V (−8 volts for active marker) pulse when the RF is coincident with a marker frequency if intensity markers are selected.

NEG Z BLANK. Negative Z-axis blanking signal. Supplies a negative rectangular pulse (−5V into 2500 ohms) during the retrace and bandswitch points of the RF output.

PEN LIFT. Output to control the pen lift function of an X-Y recorder. Maximum pen-up level is +40V and maximum pen-down sink current is 500 mA (at +0.7V).

SWEEP OUT/IN. Wired in parallel with sweep out/in BNC connector on front panel. See Display Functions Control group for a description.

CNTR TRIG. Counter Trigger (HP 5343A Frequency Counter only). Output for controlling the external trigger input of the HP 5343A frequency counter.

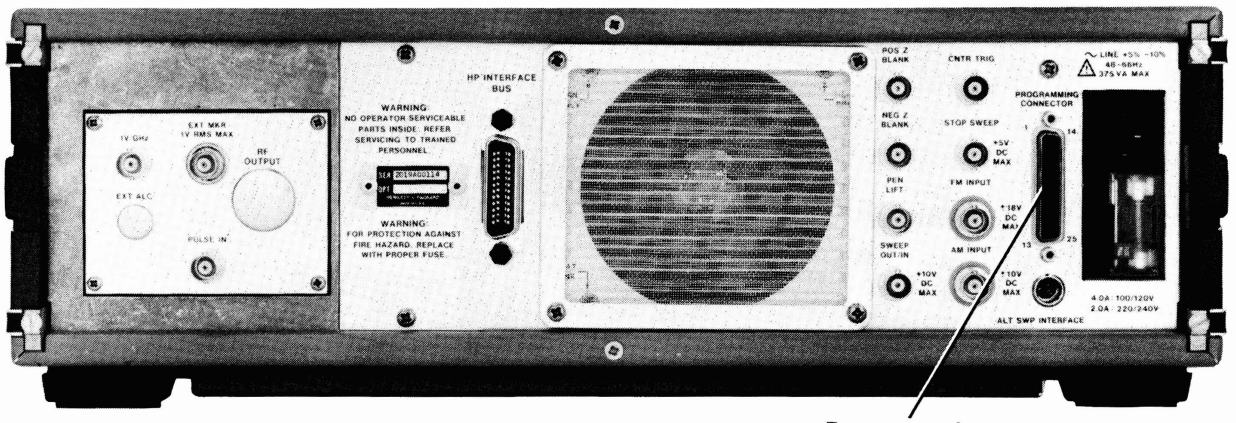
STOP SWEEP. Input for stopping the progress of a forward sweep. When input is 0 to 0.8 volt, sweep is stopped − RF output is a constant CW frequency. Sweep continues when input voltage returns to greater than 2 volts or open circuit. Usable with the HP 5343A Frequency Counter and CNTR TRIG to select and measure frequency points along the sweep.

FM INPUT. Input for frequency modulation or phase lock error signal for the plug-in. This input is passed through to the plug-in and processed by the plug-in only. See plug-in specifications for frequency deviation and sensitivity.

AM INPUT. Input for external amplitude modulation of the plug-in. This input is passed through to the plug-in. See plug-in specifications for amplitude input range.

ALT SWP INTERFACE. Connects via cable HP Part No. 8120-3174 to 8755C to provide Alternate Sweep function.

PROGRAMMING CONNECTOR. See Figure 16 for pin designation.



PROGRAMMING CONNECTOR

Pin No.	Description		Pin No.	Description	
1			15 −	Marker Pulse Request	(I)
2 −	Marker Pulse	(O)			
3 −	Pen Lift Request	(I)	16 −	Retrace	(O)
4 −	Sweep Alternate	(O)	17 −	Alternate Sweep Enable	(O)
5 −	Stop Fwd. Sweep Request	(I)	18 −	Stop Sweep Request	(I)
6	+5 Volt (100 ma MAX)	(O)			
7 −	RF Blanking	(O)	19	Digital Ground	(I/O)
8 −	RF Blank Request	(I)	20 −	Blanking Pulse Request	(I)
9 −	Ext. Trigger Input	(I)	21 −	Counter Trigger	(O)
10 +	Pen Lift	(O)	22 −	Step Up	(I)
11 −	Recorder Mute	(O)	22 −	Advance	
12	—	(O)	23 −	Inverse Pen Lift	(O)
13	—		24 +	8410 Ext. Trigger	(O)
14 −	Blanking	(O)	25	—	

− Negative Logic (True is logical "Ø")
+ Positive Logic

(I) Input
(O) Output

Figure 16. Rear Panel Connections

APPENDIX 2:

86200 SERIES PLUG-INS WITH 11869A ADAPTER

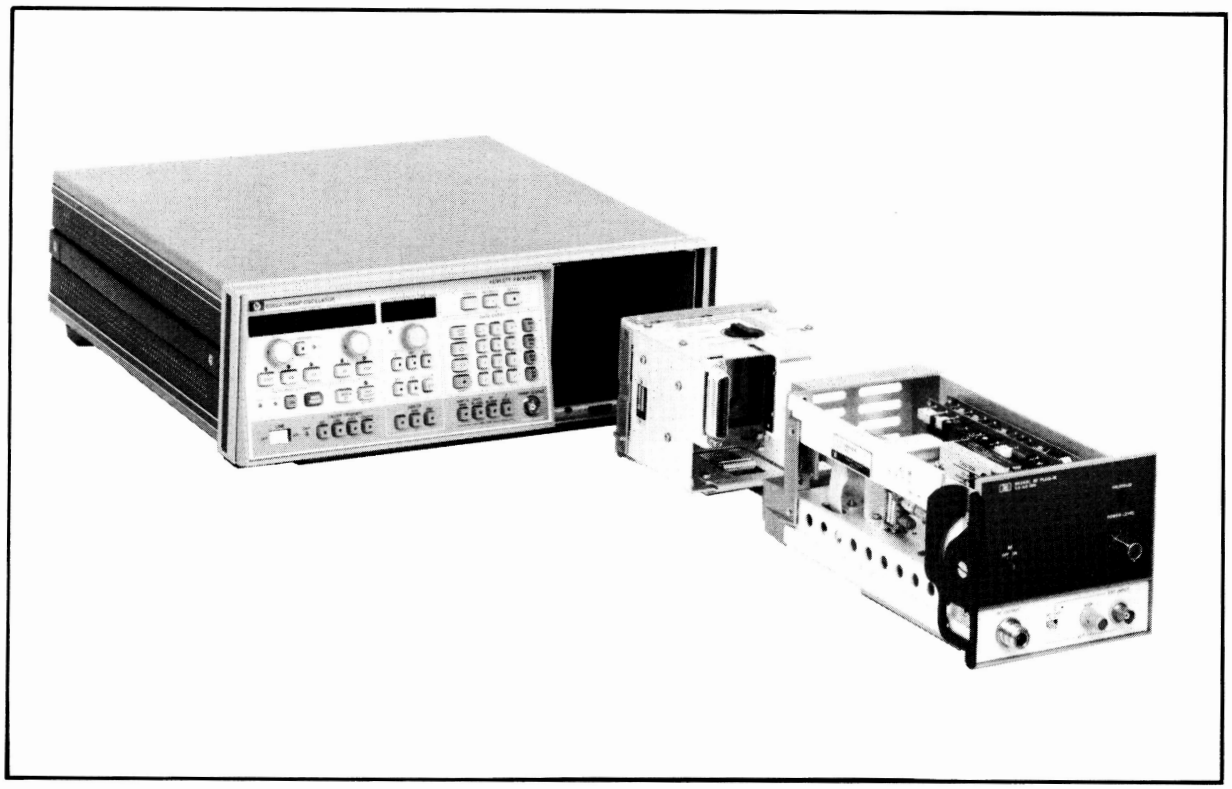


Figure 17. Connecting 11869A Adapter to 86200 series Plug-in

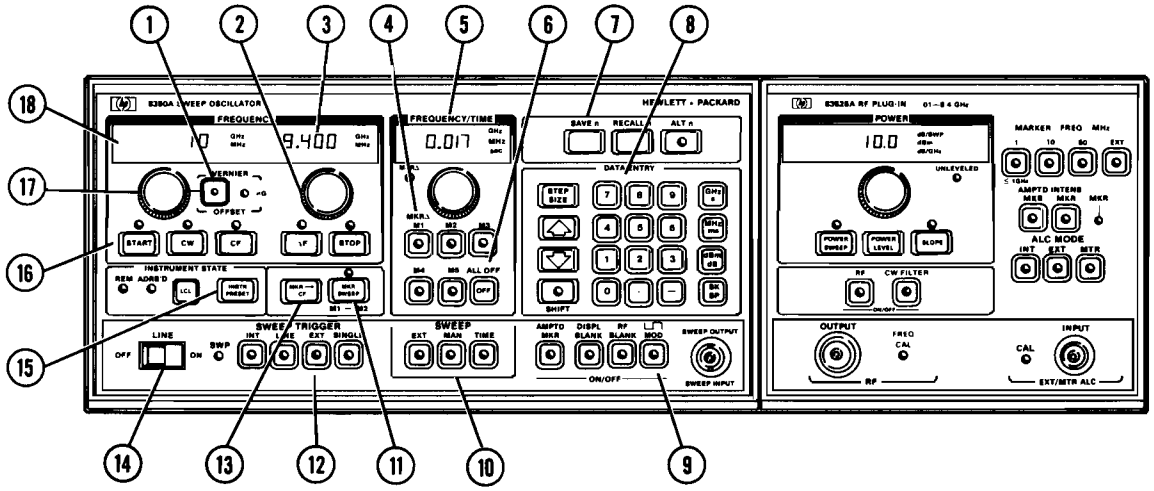
Although designed for the 8620 Sweep Oscillator, the 86200 series RF Plug-ins can be used in the 8350A Sweep Oscillator with the addition of the 11869A Adapter.

The 11869A Adapter provides the electrical and mechanical interface between the 8350A and an 86200 series Plug-in. A switch on the 11869A allows the user to select the appropriate interface code (from the code listing on the adapter) so that an 86200 series Plug-in can be used in the 8350A.

All of the standard performance and control of the 8350A is available when using an 86200 Plug-in with the 11869A Adapter. However, plug-in functions (e.g. output power, RF on/off, plug-in markers) will not be programmable and will not respond to keyboard and step keys. On the rear panel of the 11869A Adapter are several hole plugs that allow connections to be made to the back panel of the plug-in. 11869A Option 004 provides two semi-rigid cables to allow connection of 86200 series rear panel RF output to 11869A rear panel.

Special Plug-ins: (Plug-ins with Option HXX)

When using 86200 series Plug-ins that have been factory modified for a non-standard frequency range, a PROM obtained from the factory must be used in the 11869A Adapter. The PROM is inserted in the 16-pin socket on the PC board of the adapter and is needed for proper interfacing and controlling of a non-standard plug-in.



APPENDIX 3
FRONT PANEL CONTROLS SUMMARY

1. **Vernier/Offset.** Vernier function offsets sweep ranges, CW or CF frequencies. ≠0 lamp lit when non-zero offset or vernier present.

2. **Right Frequency Control.** Adjusts ΔF or STOP frequency.

3. **Right Frequency Display.** Displays STOP or ΔF frequency in GHz or MHz.

4. **MKR-Δ.** Allows user to display frequency difference between any two markers and intensifies the appropriate portion of the display.

5. **Frequency/Time Display.** Display Marker or manual sweep frequency in GHz or MHz. Sweep Time in seconds and HP-IB address.

6. **Markers.** Controls the five independent, mainframe supplied frequency markers.

7. **Save n/Recall n/Alt n.** Can save and recall up to nine different settings.

8. **Data Entry Keyboard.** Can enter exact values or step sizes for most sweep parameters via the keyboard.

9. **Output Controls.** Can control marker display mode, RF and display blanking and internal square wave modulation (of the RF output).

10. **Sweep Mode.** Selects External, Manual, or Timed sweep mode.

11. **MARKER SWEEP.** Causes Marker 1 frequency to temporarily become start of sweep, Marker 2 frequency to become stop of sweep.

12. **Sweep Trigger.** Determines how sweep will trigger.

13. **MKR→CF.** Causes center frequency of sweep to be shifted to the frequency of the currently active marker.

14. **Line switch.** Turns on/off 8350A mainframe and plug-in.

15. **Instrument Preset.** Selects a pre-determined instrument state.

16. **START/CF/CW/ΔF/STOP Sweep mode keys.** Selects mode of output and display.

17. **Left frequency Control.** Adjusts START, CW, CF, VERNIER or OFFSET.

18. **Left Frequency Display.** Displays START, CW, CF, VERNIER or OFFSET frequency in GHz or MHz, depending on mode selected, plus self test error codes.

Figure 18. Front Panel Controls

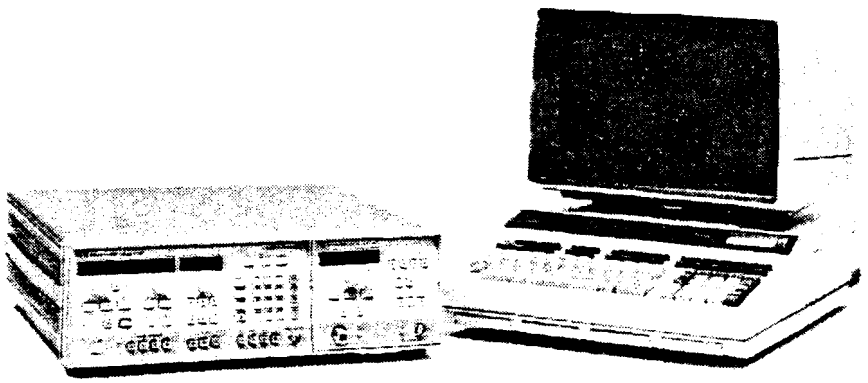
DESIGNED FOR HP-IB SYSTEMS

Programming Note

8350A/9835A-1
Supersedes: None

OCTOBER 1980

Introductory Operating Guide for the HP 8350A Sweep Oscillator with the HP 9835A Desktop Computer



INTRODUCTION

This programming note is a guide to the remote operation of the HP 8350A Sweep Oscillator and appropriate HP 83500 Series Plug-in using the HP 9835A Desktop Computer. Included in this guide are the system connections for remote operation and several example programs with descriptions of each step.

The 8350A is fully compatibile with the Hewlett-Packard Interface Bus (HP-IB). When used with a controller such as the 9835A, complete control of the sweep mode, frequency limits, frequency markers, power level, and all other front panel controls can be achieved.

REFERENCE INFORMATION

For further information on the HP Interface Bus, the following reference should prove helpful:

- Condensed Description of the Hewlett-Packard Interface Bus (HP Literature No. 59401-90030).

Complete reference information on the 8350A can be found in the 8350A Sweep Oscillator Operating and Service Manual (HP Part No. 08350-90001). For information on operating the 9835A the following references are available:

- 9835A Operating and Programming Manual (HP Part No. 09835-90000).
- 9835A I/O ROM Programming Manual (HP Part No. 09835-90060).

EQUIPMENT REQUIRED

To perform all the example programs described in this programming note, you will need the following equipment and accessories:

1. HP 8350A Sweep Oscillator with any HP 83500 Series Plug-in. Note that an HP 86200 Series Plug-in with the HP 11869A Adapter can be used but all references to power level and power control are not applicable.
2. HP 9835A Desktop Computer with:
   a. HP 98332A I/O ROM (actually 4 ROM's)
   b. HP 98034A Revised HP-IB Interface Card/ Cable

HEWLETT PACKARD

NOTE

The following equipment is not required for the programs to function but rather for a visual display of the 8350A functions.

3. HP 8755S Frequency Response Test Set with:
   a. HP 8755C Swept Amplitude Analyzer
   b. HP 180TR or 182T Display Unit
   c. HP 11664A or 11664B Detector
   d. Two 120 cm.(4 ft.) cables (HP 11170C type).

   or any appropriate Oscilloscope with Crystal/ Schottky Detector, Attenuator, and BNC Cabling.

4. Any test device over the frequency range of the 83500 Series Plug-in.

SET-UP

Figure 1 shows the system connection and switch settings for the 98034A Interface and the 9835A Desktop Computer. The following procedure completes the setup:

1. Turn off the power to the 9835A.

2. Verify that the ROM's are installed in the 9835A. If not, then install the ROM's in an unused ROM drawer then insert the drawer in one of the front panel slots of the 9835A.

3. Install the 98034A Interface Card into one of the rear panel slots of the 9835A.

4. Verify that the rotary switch on top of the 98034A is set to "7". If not then set it to "7" since this is the select code for the interface card for all programs found within this guide.

5. Connect the 24-pin HP-IB connector of the 98034A to the rear panel HP-IB connector of the 8350A. This connector is tapered to insure proper connection.

CAUTION

Do not attempt to mate black metric threaded screws on one connector with silver English threaded nuts on another connector, or vice-versa, as damage may result. A metric conversion kit which will convert one cable and one or two instruments to metric hardware is available by ordering HP Part No. 5060-0138.

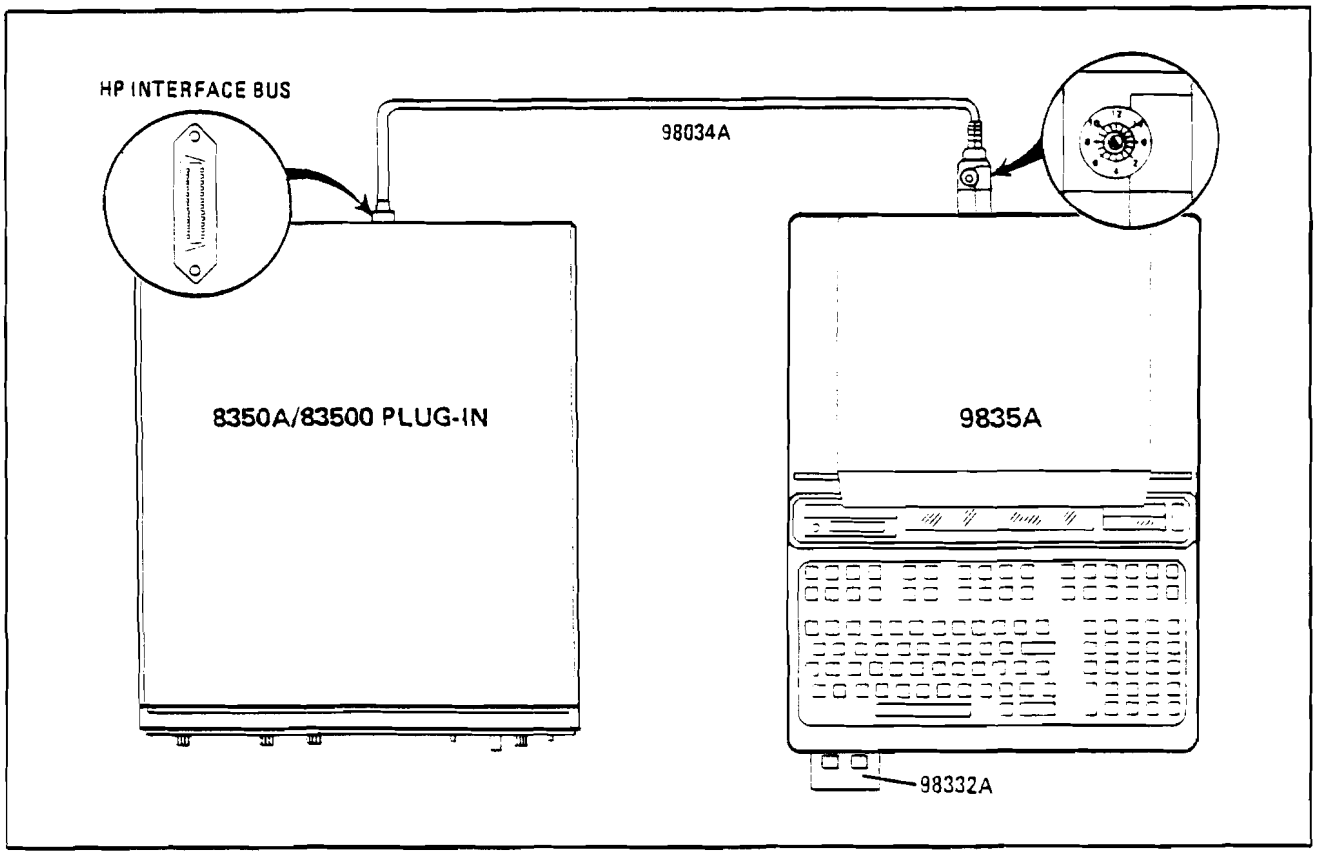


Figure 1. System Connection

6. All programs within this guide expect the 8350A HP-IB address to be decimal 19. The 8350A HP-IB address switches are located inside the instrument and are factory preset to decimal 19. To execute a front panel 'Set HP-IB Address' which will display the present HP-IB address:

   Press SHIFT LCL

   The FREQUENCY/TIME display will indicate the present decimal address. To reset the number if 19 is not displayed:

   Press 1 9 GHz

   This HP-IB address will remain in effect until the instrument is powered off since the internal address switches are read at power on (unless 8350A Option 001 Non-volatile Memory is used). Since Example 4 requires the 8350A to be powered off then on, the internal address switches should be reset to 19 if necessary.

CHECK-OUT

Turn on the 9835A and the 8350A. The 9835A should undergo an internal memory test then display "9835A READY FOR USE" on the CRT display. The 8350A should also undergo a turn-on self test consisting of the red LED numeric displays being blanked and all yellow indicator LED's on, then the 8350A sweep controls are set to the instrument preset state: Start/Stop Sweep over the entire plug-in frequency range, fastest sweep time for plug-in used (typically 10 milliseconds), and maximum leveled output power for the plug-in. If the 8350A fails the power-up self test an error message will be displayed in the far left LED display. Check section 8 of the 8350A Operating and Service Manual for error message decoding and diagnostics.

To verify that the HP-IB connections and interface are functional perform the following on the 9835A:

1. Press CONTROL STOP (or RESET)
2. Type 'REMOTE 719'
3. Press EXECUTE

Verify that the REM light on the 8350A is lit. If this fails, verify that the 98034A select code switch is set to "7", the 8350A address switches are set to "19", and the interface cable is properly connected.

If the 9835A display indicates an error message, it is possible that the above remote message was typed in incorrectly or the ROM's are not properly installed. If the 9835A accepts the remote statement and the display is clear but the 8350A REM light does not turn on, you could have a defective 98034A or 8350A. Perform the operational checks as outlined in the respective Operating and Service Manuals to find the defective device.

PROGRAMMING EXAMPLES

The following sample programs show the various ways of controlling the 8350A. In remote control situations the 8350A Sweep Oscillator can interact with the system HP-IB controller in two basic ways:

1. "Listen Mode": The 8350A listens to the control commands as to modifying the present instrument state. This effectively commands the 8350A to do a specific event much like setting a front panel function.

2. "Talk Mode": The 8350A informs the controller of the present instrument state with a numeric value or a string of characters. This effectively allows the user to interrogate or learn any 8350A function.

Each programming example is structured using the following format:

1. A general description of the functions exercised.
2. The program listing.
3. An explanation of each program line.
4. Detailed instructions for operating the program.

EXAMPLE PROGRAM 1: Remote, Local, Local Lockout, and Instrument Preset

Before programming the 8350A for different sweep functions, the user should be aware of the extent of remote control that can be used. The Remote Enable ('REMOTE') command sets the 8350A into remote control from the local (manual) mode. In remote the 8350A will perform only as its functions are programmed. However if the LCL button is pressed, the 8350A will return from the remote state to local control. To prevent this from occurring the Local Lockout ('LOCAL LOCKOUT') command disables all front panel controls, specifically the "Local" key. The Go To Local ('LOCAL') command will return the 8350A to front panel control thereby removing it from the remote and local lockout modes. Note that the above remote and local commands are different from the general HP-IB bus

local and remote commands ('LOCAL 7' and 'REMOTE 7'). Finally, in remote control it is periodically desirable to reset the 8350A to a predefined state, this is achievable with the Instrument Preset function.

PROGRAM 1

```
10   REMOTE 719
20   DISP "Remote"
30   PAUSE
40   REMOTE 719
50   LOCAL LOCKOUT 7
60   DISP "Local Lockout"
70   PAUSE
80   LOCAL 719
90   DISP "Local"
100  PAUSE
110  OUTPUT 719;"IP"
120  END
```

PROGRAM 1 EXPLANATION:

Line 10: Sets 8350A to remote.

Line 20: The 9835A displays "Remote".

Line 30: Temporarily stops program execution.

Line 40: Sets 8350A to remote.

Line 50: Sets local lockout mode.

Line 60: The 9835A displays "Local Lockout".

Line 70: Temporarily stops program execution.

Line 80: Sets 8350A to local.

Line 90: The 9835A displays "Local".

Line 100: Temporarily stops program execution.

Line 110: Sets 8350A to remote and performs an Instrument Preset.

Line 120: Stops program execution.

To verify and investigate the different remote modes do the following:

1. Press CONTROL STOP, SCRATCH, A, EXECUTE on the 9835A. This scratches the program memory.
2. Press INSTR PRESET on the 8350A.
3. Type in the above program.
4. Press RUN on the 9835A.
5. With the 9835A displaying "Remote", verify that the 8350A REM light is lit. From the front panel, verify that the start frequency cannot be changed. Verify that the INSTR PRESET key and all other keys except LCL are disabled. Now press the LCL key and verify that the 8350A REM light is off and that you can modify any of the sweep functions.
6. Press CONTINUE on the 9835A. With the 9835A displaying "Local Lockout" verify that the 8350A REM light is again lit. Again attempt to change the start frequency and perform an instrument preset. Verify that this is impossible. Now press the LCL key and verify that still no action is taken.
7. Press CONTINUE on the 9835A. With the 9835A displaying "Local" verify that the 8350A REM light is off. Also verify that all sweep functions can now be modified via the front panel controls.
8. Press CONTINUE on the 9835A. Verify that the 8350A has undergone an Instrument Preset and the REM light is on. The Output ('OUTPUT 719') statement does two things, one it performs a 'REMOTE 719', and second it passes data to the 8350A.

Note that the 8350A LCL key produces the same result as programming 'LOCAL 719' or 'LOCAL 7'. Be careful as the latter command places all instruments on the HP-IB in local state as opposed to the 8350A alone.

EXAMPLE PROGRAM 2: Programming Functions

To program any function on the 8350A the controller must pass specific program codes and data to the sweeper. The statement that allows this is the Output ('OUTPUT') statement. The alphanumeric data string of the output statement can be a concatenation of character strings and/or variables. The data can be specific codes, free field formatted data, or reference a specific image ('IMAGE') statement. For example, to program the CW Frequency (CW), one program code sequence is "CW", the frequency in GHz, "GZ". If the frequency is to be 7.555 GHz, then the string "CW7.555GZ" will suffice. However if the frequency were to change then a variable 'F' could indicate the frequency in GHz and the program string could be "CW",F,"GZ". Using an image statement also allows a specific number of digits to be passed, thereby avoiding any unexpected round off errors.

NOTE

This program expects an 83500 Series Plug-in that covers the frequency 7.555 GHz. If using a plug-in that does not cover this frequency range then the value in lines 30 and 40 should be changed to an appropriate value.

PROGRAM 2

```
10   OUTPUT 719;"IP"
20   FIXED 2
30   OUTPUT 719;"CW7.555GZ"
40   DISP "CW = 7.555 GHz"
50   PAUSE
60   INPUT "CW (in GHz) = ?",F
70   PRINT "CW = ";F;" GHz"
80   OUTPUT 719;"CW";F;"GZ"
90   GOTO 60
100  IMAGE "CW",DD.DDD,"GZ"
110  OUTPUT 719 USING 100;F
120  GOTO 60
```

PROGRAM 2 EXPLANATION:

Line 10: Puts the 8350A into a predefined state via instrument preset.

Line 20: Fixes numeric data output to 2 decimal places.

Line 30: Puts the 8350A in CW mode and programs a CW frequency of 7.555 GHz.

Line 40: The 9835A displays "CW = 7.555 GHz".

Line 50: Temporarily stops program execution.

Line 60: The 9835A displays "CW (in GHz) =?". The user is prompted to input a new CW frequency value which is stored in the variable 'F'.

Line 70: Print on the CRT display the programmed CW frequency.

Line 80: Program the CW frequency using the default data format.

Line 90: Go to line 60.

Line 100: Image statement is set up for programming the CW frequency with a 1 MHz resolution.

Line 110: Program the CW frequency via image statement in line 100.

Line 112: Go to line 60.

The equipment setup is the same as the previous example. Reset the 9835A, scratch the 9835A memory, then type in the above program. Then do the following:

1. Run the program. The 9835A displays "CW = 7.555 GHz". The 8350A changes from the instrument preset state of Start/Stop sweep to a CW frequency of 7.555 GHz.
2. Press CONTINUE on the 9835A. The 9835A now displays "CW (in GHz) =?". Type in a new CW frequency (value in GHz), then press CONTINUE.
3. The 8350A will be programmed to the new CW frequency with the new value printed on the CRT display. The program jumps back to step (2) above.

When inputting the CW frequency try several values, each with a different number of digits after the decimal point. Notice that the 8350A displays the frequency to 3 decimal places (1 MHz frequency resolution). Values with better than 1 MHz frequency resolution are rounded to the nearest MHz by the 8350A. However when the 9835A is reset all numeric output data defaults to the 'FIXED 2' or fixed 2 decimal places format. Thus the 9835A rounds the desired frequency to the nearest 10 MHz. To change this free-field format to more decimal places modify the fixed format statement in line 20 to 'FIXED 5' then re-run the program. Another approach is to utilize the image statement to set the desired number of decimal places. To use the image statement in the program, do the following on the 9835A:

Press STOP
Type 'DEL 80, 90'
Press EXECUTE.

This should delete lines 80 and 90 from program #2 and allow the use of lines 100, 110, and 120 instead. Run the modified program again and use the same steps for operation as before. Now if the value inputted has a frequency resolution greater than 1 MHz the 9835A does the rounding instead of the 8350A. This is the preferred programming approach. Change the image statement for 10 MHz frequency resolution and verify the results from the 8350A frequency display.

Since a device select code address can be a variable, verify that this can be used in the modified or original program #2 by doing the following:

1. Insert before Line 10 a new line with the variable 'Swp' by:

   Press STOP
   Type '5 Swp=719'
   Press STORE.

2. Modify the output statement(s) by editing the necessary lines and changing the 'OUTPUT 719' to 'OUTPUT Swp' and 'OUTPUT 719 USING 100' to 'OUTPUT Swp USING 100'.

3. Re-run the modified program using the same operation steps as above.

EXAMPLE PROGRAM 3: Setting Up A Typical Sweep

Typically the sweeper is programmed for the proper sweep frequency range, sweep time, power level, and marker frequencies for a test measurement. This program sets up the sweeper for a general purpose situation using several dedicated image statements. Note that not all parameters need to be reprogrammed every time.

NOTE

This program expects an 83500 Series Plug-in that covers the frequency range of at least 3 to 7 GHz. If using a plug-in with a different frequency range, change the values in lines 60, 90, and 100, to the appropriate values. If using an 86200 Series Plug-in then do not enter line 70.

PROGRAM 3

```
10   IMAGE "FA",DD.DDD,"GZFB",DD.DDD,"GZ"
20   IMAGE "ST",DDDDD,"MS"
30   IMAGE "M",D,DD.DDD,"GZ"
40   IMAGE "PL",DDD.D,"DM"
50   OUTPUT 719;"IPMD1"
60   OUTPUT 719 USING 10;3,7
70   OUTPUT 719 USING 40;10
80   OUTPUT 719 USING 20;50
90   OUTPUT 719 USING 30;1,4
100  OUTPUT 719 USING 30;2,6
110  END
```

PROGRAM 3 EXPLANATION:

Line 10: Image statement for setting the Start and Stop Sweep frequencies in GHz.

Line 20: Image statement for setting the Sweep Time in milliseconds.

Line 30: Image statement for setting a Frequency Marker by marker number and frequency in GHz.

Line 40: Image statement for setting the Output Power Level in dBm.

Line 50: Preset the sweeper to a known state via instrument preset and enable the internal 27.8 kHz Square Wave Amplitude Modulation.

Line 60: Set a Start/Stop Sweep of 3.0 to 7.0 GHz.

Line 70: Set the Output Power Level to +10 dBm.

Line 80: Set the Sweep Time to 50 milliseconds.

Line 90: Set Marker#1 to 4 GHz.

Line 100: Set Marker#2 to 6 GHz.

Line 110: Stop program execution.

Set up the equipment as shown in Figure 2 by adding the 8755C, the 180TR or 182T, the 11664, and a test device like a 4 to 6 GHz Bandpass Filter. It is important that the two rear panel connections from the 8350A to the 8755C/182T are made for a proper CRT display. For the example measurement set the following front panel controls:

On the 8755C:

Channel 1:

Display..... OFF (press all the display push buttons so that they are all out)

Channel 2:

Display..... 8
dB/DIV..... 10 dB
Reference Level..... −10 dB
Reference Level Vernier..... OFF

On the 182T or 180TR:

Magnifier..... X1
Display..... INT

After connecting the equipment: reset the 9835A, scratch the 9835A memory, then type in the above program. Then run the program. The 8350A will initially undergo an instrument preset which will set the proper power leveling mode and sweep blanking signals. Since the 8755C requires the RF signal to be modulated at a 27.8 kHz rate, the internal amplitude modulation is enabled. If using a 4 to 6 GHz Bandpass Filter as the test device, the CRT display should reflect the filter transmission response over the 3 to 7 GHz range. Two frequency markers of the Z-Axis Intensity dot variety are set to 4 and 6 GHz, hopefully within the passband or near the 3 dB points. The setup can be modified by changing the values in lines 60, 70, 80, 90, and/or 100, then re-run the program.

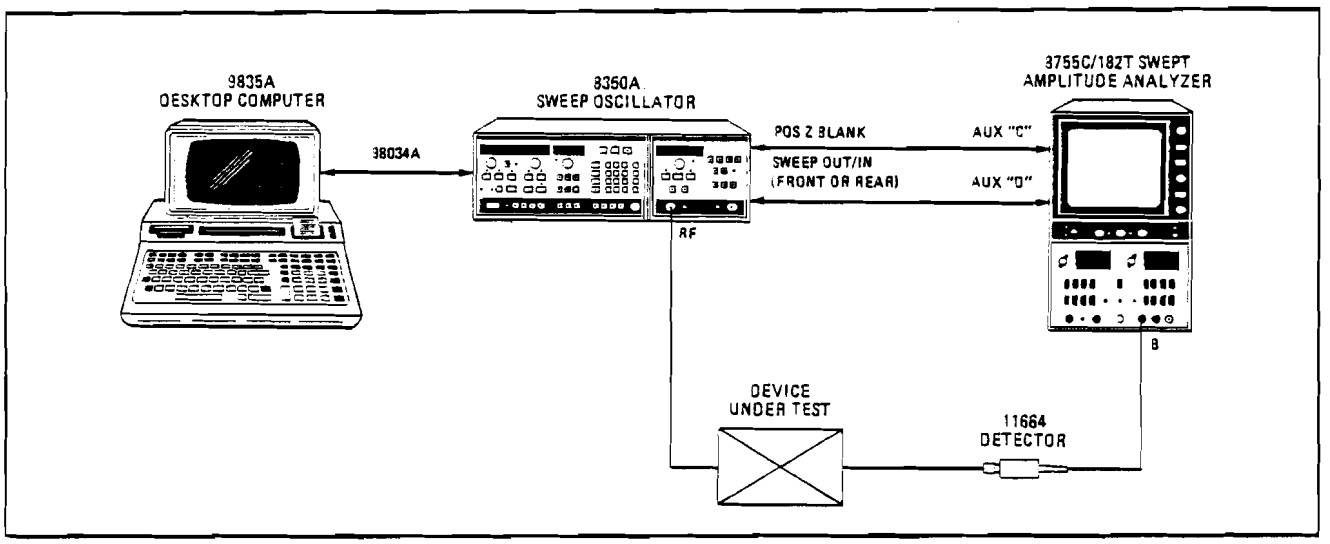


Figure 2. Equipment Setup For Program 3

EXAMPLE PROGRAM 4: Learning An Instrument State

Being able to save a specific instrument state is helpful when it is needed several times in a test or measurement procedure. The user could save the instrument state by manually logging the important sweep parameters such as frequency range, power level, ALC modes, etc., then re-inputting them at the appropriate time. A somewhat simpler approach is to save the instrument state in one of the 8350A internal storage registers, then recall it when needed. However, this is not a permanent solution unless the 8350A Non-volatile Memory option (Option 001) is used. A more permanent solution is to use the Output Learn String function of the 8350A so that the 9835A can learn then store a data string that describes the present instrument state on a tape cartridge or in its' internal memory. Once an instrument state is stored or learned, the 8350A can then be restored to that state using the Input Learn String function. The power of these instrument Learn/Teach functions are demonstrated by the following program using the 9835A fast data transfer function.

PROGRAM 4

```
10   OPTION BASE 1
20   DIM A$[100]
30   OUTPUT 719;"IPMD1"
40   LOCAL 719
50   PAUSE
60   OUTPUT 719;"OL"
70   ENTER 719 BFHS 90 USING "#,90A";A$
80   PAUSE
90   OUTPUT 719;"IL"&A$
100  END
```

PROGRAM 4 EXPLANATION:

Line 10: Define the first element in any array to be at index number 1.

Line 20: Set the length of the A$ string to 100 characters.

Line 30: Set the 8350A to a predefined state via instrument preset and enable the square wave modulation.

Line 40: Return the 8350A to local control.

Line 50: Temporarily stops program execution.

Line 60: Program the 8350A to output the Learn String.

Line 70: Read the Learn String into the 9835A using a byte fast handshake transfer of 90 string characters ignoring the line feed as the string terminator. Store the 90 character Learn String in A$.

Line 80: Temporarily stops program execution.

Line 90: Program the 8350A to accept a Learn String, then send the new Learn String to the 8350A.

Line 100: Stop program execution.

Setup the equipment as in example 3 using the CRT display to verify the sweep settings. Note that the original equipment setup can also be used with the 8350A front panel indicators used for verification. Reset the 9835A, scratch the 9835A memory, then

type in the above program. Run the program. The 8350A will undergo an instrument preset, enable the square wave modulation, then return to local front panel control. Then perform the following:

1. Adjust the 8350A to a preferred instrument state, then press CONTINUE on the 9835A.
2. Turn the 8350A line power off. Wait five seconds then turn the 8350A power back on. Press INSTR PRESET on the 8350A.
3. Press CONTINUE on the 9835A. Verify on the CRT display and/or the 8350A that the original instrument state has been restored.

EXAMPLE PROGRAM 5: Interrogating The Present Value Of A Function

While the 8350A Learn String enables the user to completely save a string of characters that define the present instrument state, the information is densely packed and encoded to save memory space. If the user wishes to determine the actual value of a specific parameter, say the Start Frequency, it would require a tedious process to extract a numeric value from several characters within the Learn String. An easier approach is to use the Output Interrogated Parameter function of the 8350A. With this function the 9835A instructs the 8350A to output the present numeric value of a specified function. Any function that has a numeric value associated with it can be interrogated. Note that if the parameter is not presently active, the 8350A uses a computed value or its previous value. The following program demonstrates the capability of the interrogate function.

PROGRAM 5

```
10   OUTPUT 719;"IPMD1"
20   LOCAL 719
30   PAUSE
40   OUTPUT 719;"OPFA"
50   ENTER 719;A
60   PRINT "Start Freq = ";A/1E6;" MHz"
70   OUTPUT 719;"OPFB"
80   ENTER 719;B
90   PRINT "Stop Freq  = ";B/1E6;" MHz"
100  OUTPUT 719;"OPST"
110  ENTER 719;T
120  PRINT "Sweep Time = ";1000*T;" msec"
130  END
```

PROGRAM 5 EXPLANATION:

Line 10: Set the 8350A to a predefined instrument state via instrument preset and enable the square wave modulation.

Line 20: Return the 8350A to local control.

Line 30: Temporarily stops program execution.

Line 40: Program the 8350A to output the present value of the Start Frequency.

Line 50: Read the value into the 9835A and store it in the variable 'A'.

Line 60: Print on the CRT display the present value of the Start Frequency in MHz.

Line 70: Program the 8350A to output the present value of the Stop Frequency.

Line 80: Read the value into the 9835A and store it in the variable 'B'.

Line 90: Print on the CRT display the present value of the Stop Frequency in MHz.

Line 100: Program the 8350A to output the present value of the Sweep Time.

Line 110: Read the value into the 9835A and store it in the variable 'T'.

Line 120: Print on the CRT display the present value of the Sweep Time in milliseconds.

Line 130: Stops program execution.

Setup the equipment as in example 3 using the analyzers' CRT display to verify the sweep settings. Note that the original equipment setup can also be used with the 8350A front panel indicators used for verification. Reset the 9835A, scratch the 9835A memory, then type in the above program. Run the program. The 8350A will undergo an instrument preset, enable the square wave modulation, then return to local front panel control. Then perform the following:

1. Adjust the 8350A to a preferred instrument state using the Start Frequency, Stop Frequency, and Sweep Time controls.
2. Press CONTINUE on the 9835A.
3. The present values of the Start Frequency, Stop Frequency, and Sweep Time are sequentially interrogated and then printed on the CRT of the 9835A.

EXAMPLE PROGRAM 6: A Stepped CW Sweep

Present automatic measurement systems typically make measurements at a sequence of CW test frequencies instead of analog sweeping the frequency range of interest. If swept, the measurement data taking machine would need to sample the RF signal at a very fast rate to maintain accurate frequency information, too. This is typically not accomplished. Stepped CW sweeps can be accomplished in several ways with the 8350A:

1. Program sequential CW test frequencies.

2. Program the frequency sweep range then enable the manual sweep mode. Perform a stepped manual sweep by repetitively programming the step up/increment function.

3. Program the CW frequency to the start frequency, the Step Size to an appropriate value, then repetitively program the step up/increment function.

Considering the speed of programming the above approaches, the third is the most efficient. This program illustrates a stepped sweep using this approach.

PROGRAM 6

```
10   OUTPUT 719;"IPMD1FI0"
20   INPUT "Start Freq (GHz) = ?",A
30   INPUT "Stop Freq (GHz) = ?",B
40   INPUT "Step Size (GHz) = ?",C
50   D=(B-A)/C
60   OUTPUT 719;"CWSS";C;"GZ"
70   OUTPUT 719;"CW";A;"GZ"
80   FOR I=1 TO D
90   OUTPUT 719;"UP"
100  WAIT 20
110  NEXT I
120  GOTO 70
```

PROGRAM 6 EXPLANATION:

Line 10: Set the 8350A to the predefined instrument state, enable the square wave modulation, and disable CW Filter.

Line 20: The 9835A displays "Start Freq (GHz) = ?", input prompts for Start frequency of the sweep. Store it in the variable 'A'.

Line 30: The 9835A displays "Stop Freq (GHz) = ?", input prompts for the stop frequency of the sweep. Store it in 'B'.

Line 40: The 9835A displays "Step Size (GHz) = ?", input prompts for the step size of the sweep. Store it in 'C'.

Line 50: Determine the number of frequency steps in sweep, store in 'D'.

Line 60: Set the CW Step Size.

Line 70: Set the CW frequency to the start frequency value.

Line 80: Iterate the CW step 'D' times.

Line 90: Program the Step Increment/Up function.

Line 100: Wait 20 milliseconds for settling.

Line 110: Continue step iteration.

Line 120: Go to line 70.

The equipment setup is the same as in the previous example. Reset the 9835A, scratch the 9835A memory, then type in the above program. Run the program. The 8350A will undergo an instrument preset and enable the square wave modulation. Then perform the following:

1. The 9835A will display "Start Freq (GHz) = ?". Answer this prompt by inputting the desired Start frequency (value in GHz) of the sweep, then press CONTINUE.

2. The 9835A will display "Stop Freq (GHz) = ?". Answer this prompt with the desired Stop frequency (in GHz) of the sweep, then press CONTINUE.

3. The 9835A will display "Step Size (GHz) = ?". Answer this prompt with the desired Step size (in GHz) of the sweep, then press CONTINUE.

4. The 8350A CW frequency will be programmed to the Start frequency of the sweep selected. Then the CW frequency is repetitively incremented by the step size value. The sweep is then restarted after reaching the stop frequency.

To stop the program press STOP.

Since part of the time involved in changing CW frequencies is in updating the numeric LED display if this could be defeated the CW frequency time can be optimized. Note that one drawback is that the numeric display will not indicate the present frequency. The 8350A provides a Display Update On/Off function and it can be implemented by modifying line 10 to be:

```
OUTPUT 719;"IPMD1FI0DU0"
```

Then re-run the modified program using the same operation steps as above.

EXAMPLE PROGRAM 7: Using Service Requests, Status Bytes, and Request Mask

Certain error conditions of the 8350A can be detected by the 9835A so that corrective action can be taken. Examples of some detectable error conditions are RF power unleveled, numeric data entry out of range, and line power failure. If an error condition exists, the user can instruct the 8350A to request service from the 9835A by initiating a Service Request (SRQ). The 9835A can detect whether an SRQ has taken place on the bus by analyzing bit 7 (see note below) of the Status Byte of the 98034A HP-IB Interface. Two modes are available for analyzing the 98034A Status Byte: (1) periodically read the Status Byte, or (2) enable bit 7 to interrupt the program when it is set. In either case, once it is determined that the 8350A has requested service, the specific error condition(s) can then be determined by reading and analyzing the Status Bytes of the 8350A. The 8350A has two Status Bytes, each consisting of 8 bits with each bit indicating the present status of a particular function or condition. See Table 1 for a complete description of the conditions associated with each Status Byte bit. The user can analyze these Status Bytes for every SRQ, or more simply, instruct the 8350A to issue an SRQ only if a specific set of error conditions exists. The set of conditions is determined by a numeric value passed by the Request Mask function. This numeric value is generated by summing the decimal values of each Status Byte bit to be checked. This program demonstrates the capability of the SRQ and Status Bytes to detect an error condition.

PROGRAM 7

```
10   ABORTIO 7
20   CLEAR 719
30   OUTPUT 719;"IPMD1RM"&CHR$(97)
40   ON INT #7 GOSUB Srq
50   CONTROL MASK 7;128
60   CARD ENABLE 7
70   INPUT "CW Freq (GHz) = ?",F
80   OUTPUT 719;"CW";F;"GZ"
90   WAIT 100
100  GOTO 70
110 Srq: STATUS 719;A
120  IF BIT(A,6)<>1 THEN GOTO 160
130  IF BIT(A,0)=1 THEN PRINT
     "Parameter Altered"
140  IF BIT(A,5)=1 THEN PRINT "Syntax Error"
150  CLEAR 719
160  CONTROL MASK 7;128
170  CARD ENABLE 7
180  RETURN
```

NOTE

This assumes that the status bits are numbered 0 thru 7 with the least-significant bit being number 0. Other references may assume that the bits are numbered 1 thru 8 with the least-significant bit being number 1.

If using an 86200 Series Plug-in, the Status Bytes can provide only limited information. Table 1 indicates which Status Byte functions/bits are usable.

PROGRAM 7 EXPLANATION:

Line 10: Clear the status of the HP-IB.

Line 20: Clear the status of the 8350A.

Line 30: Preset the 8350A to a predefined instrument state and enable the square wave modulation, and set the Request Mask to enable Parameter Altered and Syntax Error SRQ's.

Line 40: Indicate that if an interrupt from the 98034A HP-IB Interface is received that program execution will branch to the interrupt service routine located at the line labelled 'Srq'.

Line 50: Specify an interrupt from the 98034A if bit 7 (decimal value 128) is set.

Line 60: Enable the controller to accept an interrupt from the 98034A.

Line 70: The 9835A displays "CW Freq (GHz) = ?", input prompts for the desired CW frequency value in GHz. Store it in the variable 'F'.

Line 80: Set the CW frequency as determined by 'F'.

Line 90: Wait 100 milliseconds to allow the 8350A to interrupt.

Line 100: Go to line 70.

Line 110: Location of the interrupt service routine. Read the Status Byte of the 8350A and store it in 'A'.

Line 120: Check bit 0 of the 8350A Status Byte for an Altered Parameter error. Print on the CRT display "Parameter Altered" if one exists.

Line 130: Check bit 5 of the 8350A Status Byte for a Syntax error. Print on the CRT display "Syntax Error" if one exists.

Line 140: Clear the 8350A Status Byte to enable another SRQ.

Line 150: Re-specify bit 7 of the 98034A to cause an interrupt.

Line 160: Re-enable interrupts from the 98034A.

Line 170: Return from the interrupt service routine to the main program.

The equipment setup is the same as the previous example. Reset the 9835A, scratch the 9835A memory, then type in the above program. Run the program. The 8350A will undergo an instrument preset and enable the square wave modulation. The 9835A then displays "CW Freq (GHz) =?". Answer this prompt by inputting the desired CW frequency in GHz, then press CONTINUE. Verify that the 8350A CW frequency has been properly programmed. Try several values that are out of range of the plug-in's frequency limits and verify that an error message was printed on the CRT display. The program repeats the above input prompt. To stop the program press STOP.

Table 1. 8350A Status Byte Descriptions

STATUS BYTE (#1)								
BIT #	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1
FUNCTION	N/A	REQUEST SERVICE (RQS)	SRQ on Syntax Error	SRQ on End of Sweep	N/A	SRQ on Change in Extended Status Byte	N/A	SRQ on Numeric Parameter Altered to Default Value

EXTENDED STATUS BYTE (#2)								
BIT #	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1
FUNCTION	Airflow Failure	*RF Unleveled	Power Failure/on	N/A	N/A	N/A	N/A	Self Test Failed

*Bit/Functions not usable with 86200 Series Plug-ins and 11869A Adapter.

HP-IB PROGRAMMING CODES

Code	Description
AKm	Amplitude Marker On/Off
ALmn	Alternate Sweep On/Off
A1	Internal Leveling
A2	External Crystal Leveling
A3	External Power Meter Leveling
BK	Backspace
CAm	Amplitude Crystal Marker On/Off (83522/83525 Only)
CF	Center Frequency
CIm	Intensity Crystal Marker On/Off (83522/83525 Only)
CW	CW Frequency
C1	1 MHz Crystal Marker Frequency (83522/83525 Only)
C2	10 MHz Crystal Marker Frequency (83522/83525 Only)
C3	50 MHz Crystal Marker Frequency (83522/83525 Only)
C4	External Crystal Marker Frequency (83522/83525 Only)
DF	Delta F Frequency Span
DM	dBm
DN	Step Down/Decrement
DPm	Display Blanking On/Off
DUm	Display Update On/Off
E	Exponent Power Of 10
FA	Start Frequency
FB	Stop Frequency
FIm	CW Filter In/Out
F1	−20 MHz/V FM
F2	−6 MHz/V FM
GZ	GHz
HZ	Hz
IL	Input Learn String
IP	Instrument Preset
IX	Input Micro Learn String
KZ	KHz
MC	Marker To Center Frequency
MDm	Square Wave Amplitude Modulation On/Off
MO	Marker Off
MPm	Marker 1-2 Sweep On/Off
MS	Milliseconds
MZ	MHz
M0	Marker Off
M1	Marker #1
M2	Marker #2
M3	Marker #3
M4	Marker #4
M5	Marker #5
NT	Network Analyzer Trigger (84108)
OA	Output Active Parameter
OL	Output Learn String
OM	Output Mode String
OP	Output Interrogated Parameter
OS	Output Status bytes
OX	Output Micro Learn String
PL	Power Level
PSm	Power Sweep On/Off
RCn	Recall Register
RFm	RF Power On/Off
RM	Service Request Mask
RPm	RF Blanking On/Off
RS	Reset Sweep
SC	Seconds
SF	Frequency Step Size
SH	Shift Function
SLm	Slope On/Off
SM	Manual Sweep
SP	Power Step Size
SS	Step Size
ST	Sweep Time
SVn	Save Register
SX	external Sweep
TS	Take Sweep
T1	Internal Sweep Trigger
T2	Line Sweep Trigger
T3	External Sweep Trigger
T4	Single Sweep
UP	Step Up/Increment
VR	CW Vernier
0–9 + −	Acceptable Numeric Data

NOTES

1. **Program codes of the form "XXm" use "m" to turn the function On or Off (1 or 0). For the storage register functions the "n" is 1 through 9.**
2. **The 8350A ignores spaces, plus signs, negative signs (except when valid) and any unexpected characters. Program codes can be upper or lower case alpha characters.**

For more information, call your local HP Sales Office or nearest Regional Office: **Eastern** (201) 265-5000; **Midwestern** (312) 255-9800; **Southern** (404) 955-1500; **Western** (213) 970-7500; **Canadian** (416) 678-9430. Ask the operator for instrument sales. Or write Hewlett-Packard, 1501 Page Mill Road, Palo Alto, CA 94304. In **Europe**: Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box, CH 1217 Meyrin 2, Geneva, Switzerland. In **Japan**: Yokogawa-Hewlett-Packard Ltd., 29-21, Takaido-Higashi 3-chome, Suginami-ku, Tokyo 168.

5952-9306

Printed in U.S.A.

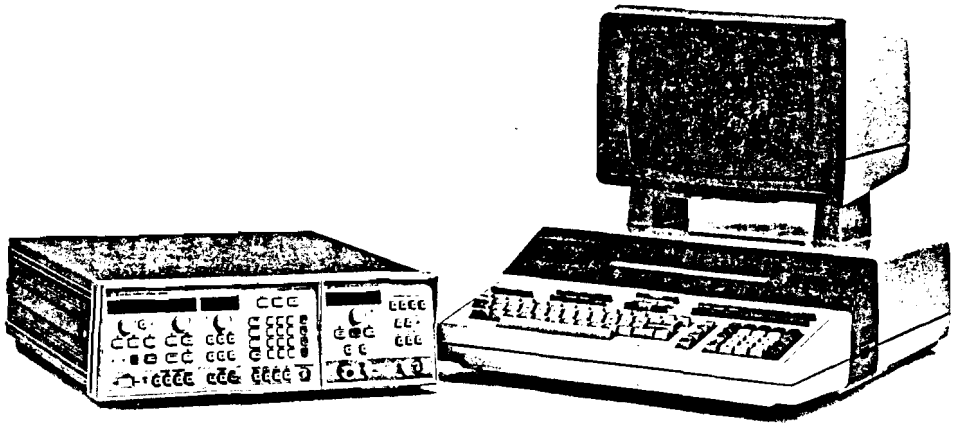
DESIGNED FOR HP-IB SYSTEMS

Programming Note

8350A/9845B-1
Supersedes: None

OCTOBER 1980

Introductory Operating Guide for the HP 8350A Sweep Oscillator with the HP 9845B Desktop Computer



INTRODUCTION

This programming note is a guide to the remote operation of the HP 8350A Sweep Oscillator and appropriate HP 83500 Series Plug-in using the HP 9845B Desktop Computer. Included in this guide are the system connections for remote operation and several example programs with descriptions of each step.

The 8350A is fully compatible with the Hewlett-Packard Interface Bus (HP-IB). When used with a controller such as the 9845B, complete control of the sweep mode, frequency limits, frequency markers, power level, and all other front panel controls can be achieved.

REFERENCE INFORMATION

For further information on the HP Interface Bus, the following reference should prove helpful:

- Condensed Description of the Hewlett-Packard Interface Bus (HP Literature No. 59401-90030).

Complete reference information on the 8350A can be found in the 8350A Sweep Oscillator Operating and Service Manual (HP Part No. 08350-90001). For information on operating the 9845B the following references are available:

- 9845B Operating and Programming Manual (HP Part No. 09845-91000).
- 9845B I/O ROM Programming Manual (HP Part No. 09845-91060).

EQUIPMENT REQUIRED

To perform all the example programs described in this programming note, you will need the following equipment and accessories:

1. HP 8350A Sweep Oscillator with any HP 83500 Series Plug-in. Note that an HP 86200 Series Plug-in with the HP 11869A Adapter can be used but all references to power level and power control are not applicable.

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2. HP 9845B Desktop Computer with:
   a. HP 98412A I/O ROM (actually 2 ROM's)
   b. HP 98034A Revised HP-IB Interface Card/ Cable

NOTE

The following equipment is not required for the programs to function but rather for a visual display of the 8350A functions.

3. HP 8755S Frequency Response Test Set with:
   a. HP 8755C Swept Amplitude Analyzer
   b. HP 180TR or 182T Display Unit
   c. HP 11664A or 11664B Detector
   d. Two 120 cm. (4 ft.) BNC cables (HP 11170C variety)

   or any appropriate Oscilloscope with Crystal/ Schottky Detector, Attenuator, and BNC Cabling.
4. Any test device over the frequency range of the 83500 Series Plug-in.

SET-UP

Figure 1 shows the system connection and switch settings for the 98034A Interface and the 9845B Desktop Computer. The following procedure completes the setup:

1. Turn off the power to the 9845B.
2. Verify that the ROM's are installed in the 9845B. If not, then install the ROM's in the appropriate side panel drawers of the 9845B.
3. Install the 98034A Interface Card into one of the rear panel slots of the 9845B.
4. Verify that the rotary switch on top of the 98034A is set to "7". If not then set it to "7" since this is the select code for the interface card for all programs found within this guide.
5. Connect the 24-pin HP-IB connector of the 98034A to the rear panel HP-IB connector of the 8350A. This connector is tapered to insure proper connection.

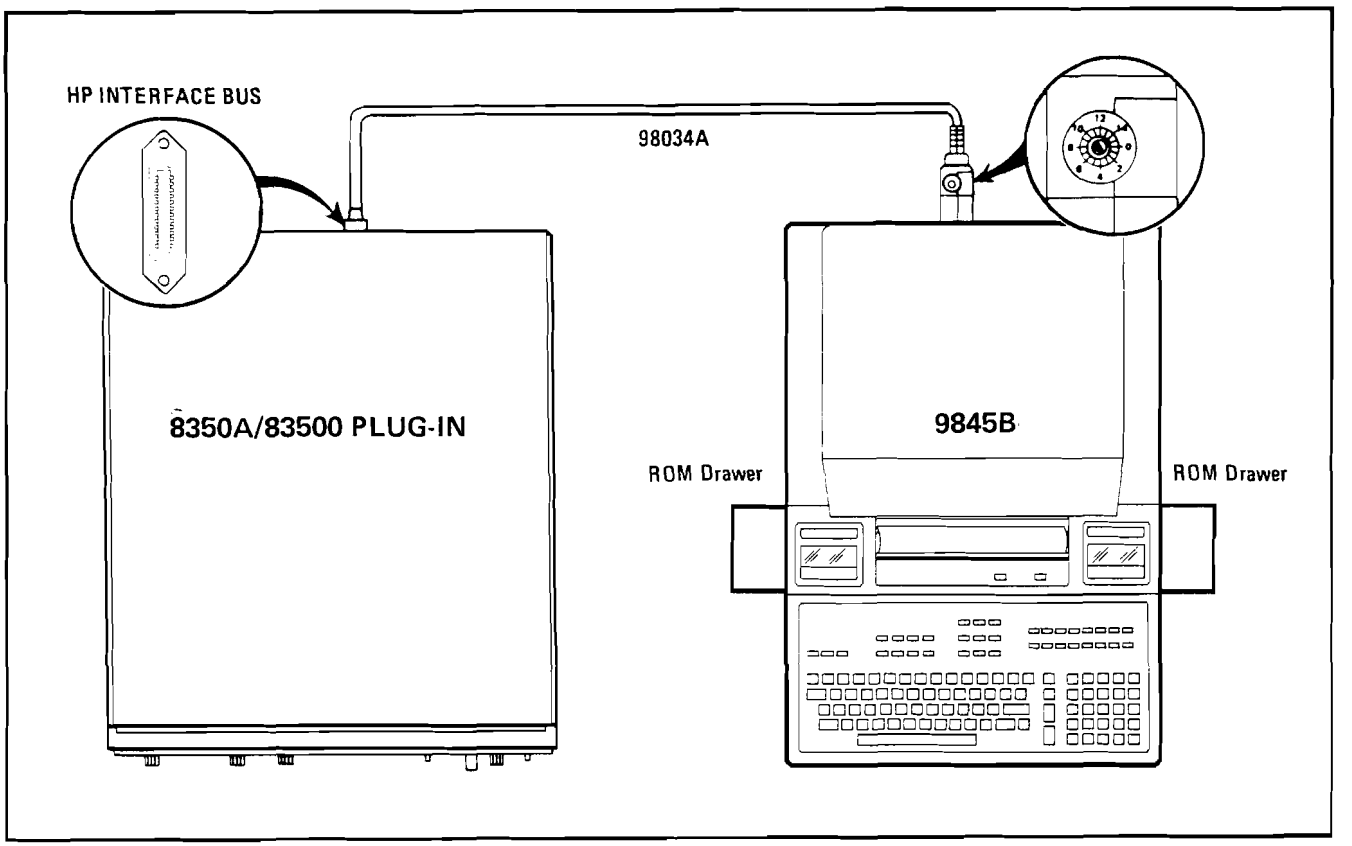


Figure 1. System Connection

CAUTION

Do not attempt to mate black metric threaded screws on one connector with silver English threaded nuts on another connector, or vice-versa, as damage may result. A metric conversion kit which will convert one cable and one or two instruments to metric hardware is available by ordering HP Part No. 5060-0138.

6. All programs within this guide expect the 8350A HP-IB address to be decimal 19. The 8350A HP-IB address switches are located inside the instrument and are factory preset to decimal 19. To execute a front panel 'Set HP-IB address' which will display the present HP-IB address:

   Press SHIFT LCL

   The FREQUENCY/TIME display will indicate the present decimal address. To reset the number if 19 is not displayed:

   Press 1 9 GHz

   This HP-IB address will remain in effect until the instrument is powered off since the internal address switches are read at power on (unless 8350A Option 001 Non-volatile Memory is used). Since Example 4 requires the 8350A to be powered off then on, the internal address switches should be reset to 19 if necessary.

CHECK-OUT

Turn on the 9845B and the 8350A. The 9845B should undergo an internal memory test then display "9845B READY FOR USE" on the CRT display. The 8350A should also undergo a turn-on self test consisting of the red LED numeric displays being blanked and all yellow indicator LED's on, then the 8350A sweep controls are set to the instrument preset state: Start/Stop Sweep over the entire plug-in frequency range, fastest sweep time for plug-in (typically 10 milliseconds), and maximum leveled output power for the plug-in. If the 8350A fails the power-up self test an error message will be displayed in the far left LED display. Check section 8 of the 8350A Operating and Service Manual for error message decoding and diagnostics.

To verify that the HP-IB connections and interface are functional perform the following on the 9845B:

1. Press CONTROL STOP (or RESET)
2. Type 'REMOTE 719'
3. Press EXECUTE

Verify that the REM light on the 8350A is lit. If this fails, verify that the 98034A select code switch is set to "7", the 8350A address switches are set to "19", and the interface cable is properly connected.

If the 9845B display indicates an error message, it is possible that the above remote message was typed in incorrectly or the ROM's are not properly installed. If the 9845B accepts the remote statement and the display is clear but the 8350A REM light does not turn on, you could have a defective 98034A or 8350A. Perform the operational checks as outlined in the respective Operating and Service Manuals to find the defective device.

PROGRAMMING EXAMPLES

The following sample programs show the various ways of controlling the 8350A. In remote control situations the 8350A Sweep Oscillator can interact with the system HP-IB controller in two basic ways:

1. "Listen Mode": Here the 8350A listens to the control commands as to modifying the present instrument state. This effectively commands the 8350A to do a specific event much like setting a front panel function.

2. "Talk Mode": Here the 8350A informs the controller of the present instrument state with a numeric value or a string of characters. This effectively allows the user to interrogate or learn any 8350A function.

Each programming example is structured using the following format:

1. A general description of the functions exercised
2. The program listing
3. An explanation of each program line
4. Detailed instructions for operating the program.

EXAMPLE PROGRAM 1: Remote, Local, Local Lockout, and Instrument Preset

Before programming the 8350A for different sweep functions, the user should be aware of the extent of remote control that can be used. The Remote Enable ('REMOTE') command sets the 8350A into

remote control from the local (manual) mode. In remote the 8350A will perform only as its functions are programmed. However if the LCL button is pressed, the 8350A will return from the remote state to local control. To prevent this from occurring the Local Lockout ('LOCAL LOCKOUT') command disables all front panel controls, specifically the "Local" key. The Go To Local ('LOCAL') command will return the 8350A to front panel control thereby removing it from the remote and local lockout modes. Note that the above remote and local commands are different from the general HP-IB bus local and remote commands ('LOCAL 7' and 'REMOTE 7'). Finally, in remote control it is periodically desirable to reset the 8350A to a predefined state, this is achievable with the Instrument Preset function.

PROGRAM 1

```
10   REMOTE 719
20   DISP "Remote"
30   PAUSE
40   REMOTE 719
50   LOCAL LOCKOUT 7
60   DISP "Local Lockout"
70   PAUSE
80   LOCAL 719
90   DISP "Local"
100  PAUSE
110  OUTPUT 719;"IP"
120  END
```

PROGRAM 1 EXPLANATION:

Line 10: Sets 8350A to remote.

Line 20: The 9845B displays "Remote".

Line 30: Temporarily stops program execution.

Line 40: Sets 8350A to remote.

Line 50: Sets local lockout mode.

Line 60: The 9845B displays "Local Lockout".

Line 70: Temporarily stops program execution.

Line 80: Sets 8350A to local.

Line 90: The 9845B displays "Local".

Line 100: Temporarily stops program execution.

Line 110: Sets 8350A to remote and performs an Instrument Preset.

Line 120: Stops program execution.

To verify and investigate the different remote modes do the following:

1. Press CONTROL STOP SCRATCH A EXECUTE on the 9845B. This scratches the program memory.
2. Press INSTR PRESET on the 8350A.
3. Type in the above program.
4. Press RUN on the 9845B.
5. With the 9845B displaying "Remote", verify that the 8350A REM light is lit. From the front panel, attempt to change the start frequency and verify that this is impossible. Verify that the Instrument Preset key and all other keys except LCL are disabled. Now press the LCL key and verify that the 8350A REM light is off and that you can modify any of the sweep functions.
6. Press CONT on the 9845B. With the 9845B displaying "Local Lockout" verify that the 8350A REM light is again lit. Again attempt to change the start frequency and perform an instrument preset. Verify that this is impossible. Now press the LCL key and verify that still no action is taken.
7. Press CONT on the 9845B. With the 9845B displaying "Local" verify that the 8350A REM light is off. Also verify that all sweep functions can now be modified via the front panel controls.
8. Press CONT on the 9845B. Verify that the 8350A has undergone an Instrument Preset and the REM light is on. The Output ('OUTPUT 719') statement does two things, one it performs a 'REMOTE 719', and second it passes data to the 8350A.

Note that the 8350A LCL key produces the same result as programming 'LOCAL 719' or 'LOCAL 7'. Be careful as the latter command places all instruments on the HP-IB in local state as opposed to the 8350A alone.

EXAMPLE PROGRAM 2: Programming Functions

To program any function on the 8350A the controller must pass specific program codes and data to the sweeper. The statement that allows this is the Output ('OUTPUT') statement. The alphanumeric data string of the output statement can be a concatenation of character strings and/or variables. The data can be specific codes, free field formatted data, or reference a specific image ('IMAGE') statement. For example, to program the CW Frequency (CW), one program code sequence is "CW",

followed by the frequency in GHz, then "GZ". If the frequency is to be 7.555 GHz, then the string "CW7.555GZ" will suffice. However if the frequency were to change then a variable 'F' could indicate the frequency in GHz and the program string could be "CW",F,"GZ". Using an image statement also allows a specific number of digits to be passed, thereby avoiding any unexpected round off errors.

NOTE

This program expects an 83500 Series Plug-in that covers the frequency 7.555 GHz. If using a plug-in that does not cover this frequency range then the value in lines 30 and 40 should be changed to an appropriate value.

PROGRAM 2

```
10   OUTPUT 719;"IP"
20   FIXED 2
30   OUTPUT 719;"CW7.555GZ"
40   DISP "CW = 7.555 GHz"
50   PAUSE
60   INPUT "CW (in GHz) = ?",F
70   PRINT "CW = ";F;" GHz"
80   OUTPUT 719;"CW";F;"GZ"
90   GOTO 60
100  IMAGE "CW",DD.DDD,"GZ"
110  OUTPUT 719 USING 100;F
120  GOTO 60
```

PROGRAM 2 EXPLANATION:

Line 10: Puts the 8350A into a predefined state via instrument preset.

Line 20: Fixes numeric data output to 2 decimal places.

Line 30: Puts the 8350A in CW mode and programs a CW frequency of 7.555 GHz.

Line 40: The 9845B displays "CW = 7.555 GHz".

Line 50: Temporarily stops program execution.

Line 60: The 9845B displays "CW (in GHz) =?". The user is prompted to input a new CW frequency value which is stored in the variable 'F'.

Line 70: Print on the CRT display the programmed CW frequency.

Line 80: Program the CW frequency using the default data format.

Line 90: Go to line 60.

Line 100: Image statement is set up for programming the CW frequency with a 1 MHz resolution.

Line 110: Program the CW frequency via image statement in line 100.

Line 120: Go to line 60.

The equipment setup is the same as the previous example. Reset the 9845B, scratch the 9845B memory, then type in the above program. Then do the following:

1. Run the program. The 9845B displays "CW = 7.555 GHz". The 8350A changes from the instrument preset state of Start/Stop sweep to a CW frequency of 7.555 GHz.

2. Press CONT on the 9845B. The 9845B now displays "CW (in GHz) =?". Type in a new CW frequency (value in GHz), then press CONT.

3. The 8350A will be programmed to the new CW frequency with the new value printed on the CRT display. The program jumps back to step (2) above.

When inputting the CW frequency try several values, each with a different number of digits after the decimal point. Notice that the 8350A displays the frequency to 3 decimal places (1 MHz frequency resolution). Values with better than 1 MHz frequency resolution are rounded to the nearest MHz by the 8350A. However when the 9845B is reset all numeric output data defaults to the 'FIXED 2' or fixed 2 decimal places format. Thus the 9845B rounds the desired frequency to the nearest 10 MHz. To change this free-field format to more decimal places modify the fixed format statement in line 20 to 'FIXED 5' from the keyboard then re-run the program. Another approach is to utilize the image statement to set the desired number of decimal places. To use the image statement in the program, do the following on the 9845B:

Press STOP
Type 'DEL 80, 90'
Press EXECUTE

This should delete lines 80 and 90 from program #2 and allow the use of lines 100, 110, and 120 instead. Run the modified program again and use the same steps for operation as before. Now if the value

inputted has a frequency resolution greater than 1 MHz the 9845B does the rounding instead of the 8350A. This is the preferred programming approach. Change the image statement for 10 MHz frequency resolution and verify the results from the 8350A frequency display.

Since a device select code address can be a variable, verify that this can be used in the modified or original program #2 by doing the following:

1. Insert before Line 10 a new line with the variable 'Swp' by:

   Press STOP
   Type '5 Swp=719'
   Press STORE

2. Modify the output statement(s) by editing the necessary lines and changing the 'OUTPUT 719' to 'OUTPUT Swp' and 'OUTPUT 719 USING 100' to 'OUTPUT Swp USING 100'.

3. Re-run the modified program using the same operation steps as above.

EXAMPLE PROGRAM 3: Setting Up A Typical Sweep

Typically the sweeper is programmed for the proper sweep frequency range, sweep time, power level, and marker frequencies for a test measurement. This program sets up the sweeper for a general purpose situation using several dedicated image statements. Note that not all parameters need to be reprogrammed every time.

NOTE

This program expects an 83500 Series Plug-in that covers the frequency range of at least 3 to 7 GHz. If using a plug-in with a different frequency range, change the values in lines 60, 90, and 100, to the appropriate values. If using an 86200 Series Plug-in then do not enter line 70.

PROGRAM 3

```
10   IMAGE "FR",DD.DDD,"GZFB",DD.DDD,"GZ"
20   IMAGE "ST",DDDDD,"MS"
30   IMAGE "M",D,DD.DDD,"GZ"
40   IMAGE "PL",DDD.D,"DM"
50   OUTPUT 719;"IPMD1"
60   OUTPUT 719 USING 10;3,7
70   OUTPUT 719 USING 40;10
80   OUTPUT 719 USING 20;50
90   OUTPUT 719 USING 30;1,4
100  OUTPUT 719 USING 30;2,6
110  END
```

PROGRAM 3 EXPLANATION:

Line 10: Image statement for setting the Start and Stop Sweep frequencies in GHz.

Line 20: Image statement for setting the Sweep Time in milliseconds.

Line 30: Image statement for setting a Frequency Marker by marker number and frequency in GHz.

Line 40: Image statement for setting the Output Power Level in dBm.

Line 50: Preset the sweeper to a known state via instrument preset and enable the internal 27.8 kHz Square Wave Amplitude Modulation.

Line 60: Set a Start/Stop Sweep of 3.0 to 7.0 GHz.

Line 70: Set the Output Power Level to +10 dBm.

Line 80: Set the Sweep Time to 50 milliseconds.

Line 90: Set Marker#1 to 4 GHz.

Line 100: Set Marker#2 to 6 GHz.

Line 110: Stops program execution.

Set up the equipment as shown in Figure 2 by adding the 8755C, the 180TR or 182T, the 11664, and a test device like a 4 to 6 GHz Bandpass Filter. It is important that the two rear panel connections from the 8350A to the 8755C/182T are made for a proper CRT display. For the example measurement set the following front panel controls:

On the 8755C:
- Channel 1:
  - Display ..... OFF (press all the display push buttons so that they are all out)
- Channel 2:
  - Display ..... B
  - dB/DIV ..... 10 dB
  - Reference Level ..... −10 dB
  - Reference Level Vernier ..... OFF

On the 182T or 180TR:
- Magnifier X1
- Display ..... INT

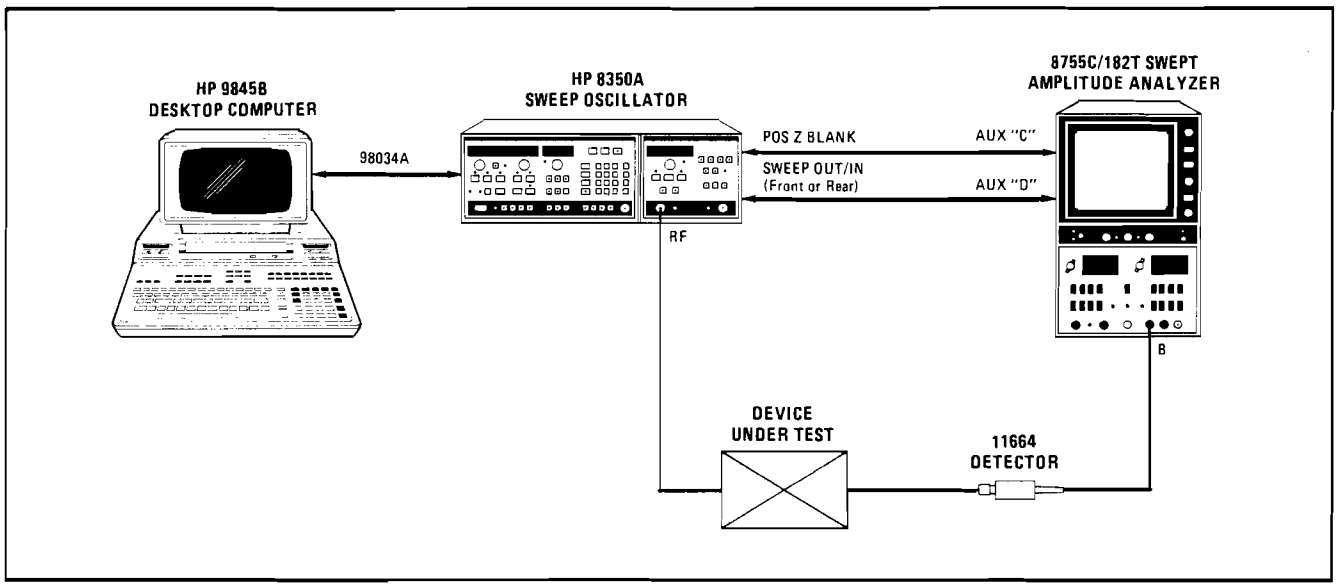


Figure 2. Equipment Setup For Program 3

After connecting the equipment: reset the 9845B, scratch the 9845B memory, then type in the above program. Then run the program. The 8350A will initially undergo an instrument preset which will set the proper power leveling mode and sweep blanking signals. Since the 8755C requires the RF signal to be modulated at a 27.8 kHz rate, the internal amplitude modulation is enabled. If using a 4 to 6 GHz Bandpass Filter as the test device, the CRT display should reflect the filter transmission response over the 3 to 7 GHz range. Two frequency markers of the Z-Axis Intensity dot variety are set to 4 and 6 GHz, hopefully within the passband or near the 3 dB points. The setup can be modified by changing the values in lines 60, 70, 80, 90, and/or 100, then re-run the program.

EXAMPLE PROGRAM 4: Learning An Instrument State

Being able to save a specific instrument state is helpful when it is needed several times in a test or measurement procedure. The user could save the instrument state by manually logging the important sweep parameters such as frequency range, power level, ALC modes, etc., then re-inputting them at the appropriate time. A somewhat simpler approach is to save the instrument state in one of the 8350A internal storage registers, then recall it when needed. However, this is not a permanent solution unless the 8350A Non-volatile Memory option (Option 001) is used. A more permanent solution is to use the Output Learn String function of the 8350A so that the 9845B can learn then store a data string that describes the present instrument state on a tape cartridge or in its' internal memory. Once an instrument state is stored or learned, the 8350A can then be restored to that state using the Input Learn String function. The power of these instrument Learn/Teach functions are demonstrated by the following program using the 9845B fast data transfer function.

PROGRAM 4

```
10   OPTION BASE 1
20   DIM A$[100]
30   OUTPUT 719;"IPMD1"
40   LOCAL 719
50   PAUSE
60   OUTPUT 719;"OL"
70   ENTER 719 BFHS 90 USING "#,90A";A$
80   PAUSE
90   OUTPUT 719;"IL"&A$
100  END
```

PROGRAM 4 EXPLANATION:

Line 10: Define the first element in any array to be at index number 1.

Line 20: Set the length of the A$ string to 100 characters.

Line 30: Set the 8350A to a predefined state via instrument preset and enable the square wave modulation.

Line 40: Return the 8350A to local control.

Line 50: Temporarily stops program execution.

Line 60: Program the 8350A to output the Learn String.

Line 70: Read the Learn String into the 9845B using a byte fast handshake transfer of 90 string characters ignoring the line feed as the string terminator. Store the 90 character Learn String in A$.

Line 80: Temporarily stops program execution.

Line 90: Program the 8350A to accept a Learn String, then send the new Learn String to the 8350A.

Line 100: Stops program execution.

Setup the equipment as in example 3 using the CRT display to verify the sweep settings. Note that the original equipment setup can also be used with the 8350A front panel indicators used for verification. Reset the 9845B, scratch the 9845B memory, then type in the above program. Run the program. The 8350A will undergo an instrument preset, enable the square wave modulation, then return to local front panel control. Then perform the following:

1. Adjust the 8350A to a preferred instrument state, then press CONT on the 9845B.
2. Turn the 8350A line power off. Wait five seconds then turn the 8350A power back on. Press INSTR PRESET on the 8350A.
3. Press CONT on the 9845B. Verify on the CRT display and/or the 8350A that the original instrument state has been restored.

EXAMPLE PROGRAM 5: Interrogating The Present Value Of A Function

While the 8350A Learn String enables the user to completely save a string of characters that define the present instrument state, the information is densely packed and encoded to save memory space. If the user wishes to determine the actual value of a specific parameter, say the Start Frequency, it would require a tedious process to extract a numeric value from several characters within the Learn String. An easier approach is to use the Output Interrogated Parameter function of the 8350A. With this function the 9845B instructs the 8350A to output the present numeric value of a specified function. Any function that has a numeric value associated with it can be interrogated. Note that if the parameter is not presently active, the 8350A uses a computed value or its previous value. The following program demonstrates the capability of the interrogate function.

PROGRAM 5

```
10   OUTPUT 719;"IPMD1"
20   LOCAL 719
30   PAUSE
40   OUTPUT 719;"OPFA"
50   ENTER 719;A
60   PRINT "Start Freq = ";A/1E6;" MHz"
70   OUTPUT 719;"OPFB"
80   ENTER 719;B
90   PRINT "Stop Freq  = ";B/1E6;" MHz"
100  OUTPUT 719;"OPST"
110  ENTER 719;T
120  PRINT "Sweep Time = ";1000*T;" msec"
130  END
```

PROGRAM 5 EXPLANATION:

Line 10: Set the 8350A to a predefined instrument state via instrument preset and enable the square wave modulation.

Line 20: Return the 8350A to local control.

Line 30: Temporarily stops program execution.

Line 40: Program the 8350A to output the present value of the Start Frequency.

Line 50: Read the value into the 9845B and store it in the variable 'A'.

Line 60: Print on the CRT display the present value of the Start Frequency in MHz.

Line 70: Program the 8350A to output the present value of the Stop Frequency.

Line 80: Read the value into the 9845B and store it in the variable 'B'.

Line 90: Print on the CRT display the present value of the Stop Frequency in MHz.

Line 100: Program the 8350A to output the present value of the Sweep Time.

Line 110: Read the value into the 9845B and store it in the variable 'T'.

Line 120: Print on the CRT display the present value of the Sweep Time in milliseconds.

Line 130: Stops program execution.

Setup the equipment as in example 3 using the analyzers' CRT display to verify the sweep settings. Note that the original equipment setup can also be used with the 8350A front panel indicators used for verification. Reset the 9845B, scratch the 9845B memory, then type in the above program. Run the program. The 8350A will undergo an instrument preset, enable the square wave modulation, then return to local front panel control. Then perform the following:

1. Adjust the 8350A to a preferred instrument state using the Start Frequency, Stop Frequency, and Sweep Time controls.
2. Press CONT on the 9845B.
3. The present values of the Start Frequency, Stop Frequency, and Sweep Time are sequentially interrogated and then printed on the CRT of the 9845B.

EXAMPLE PROGRAM 6: A Stepped CW Sweep

Present automatic measurement systems typically make measurements at a sequence of CW test frequencies instead of analog sweeping the frequency range of interest. If swept, the measurement data taking machine would need to sample the RF signal at a very fast rate to maintain accurate frequency information, too. This is typically not accomplished. Stepped CW sweeps can be accomplished in several ways with the 8350A:

1. Program sequential CW test frequencies.
2. Program the frequency sweep range then enable the manual sweep mode. Perform a stepped manual sweep by repetitively programming the step up/increment function.
3. Program the CW frequency to the start frequency, the Step Size to an appropriate value, then repetitively program the step up/increment function.

Considering the speed of programming the above approaches, the third is the most efficient time wise. This program illustrates a stepped sweep using this approach.

PROGRAM 6

```
10   OUTPUT 719;"IPMD1FI0"
20   INPUT "Start Freq (GHz) = ?",A
30   INPUT "Stop Freq (GHz) = ?",B
40   INPUT "Step Size (GHz) = ?",C
50   D=(B-A)/C
60   OUTPUT 719;"CWSS";C;"GZ"
70   OUTPUT 719;"CW";A;"GZ"
80   FOR I=1 TO D
90   OUTPUT 719;"UP"
100  WAIT 20
110  NEXT I
120  GOTO 70
```

PROGRAM 6 EXPLANATION:

Line 10: Set the 8350A to a predefined instrument state, enable the square wave modulation, and disable CW Filter.

Line 20: The 9845B displays "Start Freq (GHz) = ?", input prompts for Start frequency of the sweep. Store it in the variable 'A'.

Line 30: The 9845B displays "Stop Freq (GHz) = ?", input prompts for the stop frequency of the sweep. Store it in 'B'.

Line 40: The 9845B displays "Step Size (GHz) = ?", input prompts for the step size of the sweep. Store it in 'C'.

Line 50: Determine the number of frequency steps in sweep, store in 'D'.

Line 60: Set the CW Step Size.

Line 70: Set the CW frequency to the start frequency value.

Line 80: Iterate the CW step 'D' times.

Line 90: Program the Step Increment/Up function.

Line 100: Wait 20 milliseconds for settling.

Line 110: Continue step iteration.

Line 120: Go to line 70.

The equipment setup is the same as in the previous example. Reset the 9845B, scratch the 9845B memory, then type in the above program. Run the program. The 8350A will undergo an instrument preset and enable the square wave modulation. Then perform the following:

1. The 9845B will display "Start Freq (GHz) = ?". Answer this prompt by inputting the desired Start frequency (value in GHz) of the sweep, then press CONT.
2. The 9845B will display "Stop Freq (GHz) = ?". Answer this prompt with the desired Stop frequency (in GHz) of the sweep, then press CONT.

3. The 9845B will display "Step Size (GHz) = ?". Answer this prompt with the desired Step size (in GHz) of the sweep, then press CONT.
4. The 8350A CW frequency will be programmed to the Start frequency of the sweep selected. Then the CW frequency is repetitively incremented by the step size value. The sweep is then restarted after reaching the stop frequency.

To stop the program press STOP.

Since part of the time involved in changing CW frequencies is in updating the numeric LED display if this could be defeated the CW frequency time can be optimized. Note that one drawback is that the numeric display will not indicate the present frequency. The 8350A provides a Display Update On/Off function and it can be implemented by modifying line 10 to be:

OUTPUT 719;"IPMD1FI0DU0"

Then re-run the modified program using the same operation steps as above.

EXAMPLE PROGRAM 7: Using Service Requests, Status Bytes, and Request Mask

Certain error conditions of the 8350A can be detected by the 9845B so that corrective action can be taken. Examples of some detectable error conditions are RF power unleveled, numeric data entry out of range, and line power failure. If an error condition exists, the user can instruct the 8350A to request service from the 9845B by initiating a Service Request (SRQ). The 9845B can detect whether an SRQ has taken place on the bus by analyzing bit 7 (see note below) of the Status Byte of the 98034A HP-IB Interface. Two modes are available for analyzing the 98034A Status Byte: (1) periodically read the Status Byte, or (2) enable bit 7 to interrupt the program when it is set. In either case, once it is determined that the 8350A has requested service, the specific error condition(s) can then be determined by reading and analyzing the Status Bytes of the 8350A. The 8350A has two Status Bytes, each consisting of 8 bits with each bit indicating the present status of a particular function or condition. See Table 1 for a complete description of the conditions associated with each Status Byte bit. The user can analyze these Status Bytes for every SRQ, or more simply, instruct the 8350A to issue an SRQ only if a specific set of error conditions exists. The set of conditions is determined by a numeric value passed by the Request Mask function. This numeric value is generated by summing the decimal values of each Status Byte bit to be checked. This program demonstrates the capability of the SRQ and Status Bytes to detect an error condition.

NOTE

This assumes that the status bits are numbered 0 thru 7 with the least-significant bit being number 0. Other references may assume that the bits are numbered 1 thru 8 with the least-significant bit being number 1.

If using an 86200 Series Plug-in, the Status Bytes can provide only limited information. Table 1 indicates which Status Byte functions/bits are usable.

PROGRAM 7

```
10   ABORTIO 7
20   CLEAR 719
30   OUTPUT 719;"IPMD1RM"&CHR$(97)
40   ON INT #7 GOSUB Srq
50   CONTROL MASK 7;128
60   CARD ENABLE 7
70   INPUT "CW Freq (GHz) = ?",F
80   OUTPUT 719;"CW";F;"GZ"
90   WAIT 100
100  GOTO 70
110 Srq: STATUS 719;A
120  IF BIT(A,6)<>1 THEN GOTO 160
130  IF BIT(A,0)=1 THEN PRINT
     "Parameter Altered"
140  IF BIT(A,5)=1 THEN PRINT "Syntax Error"
150  CLEAR 719
160  CONTROL MASK 7;128
170  CARD ENABLE 7
180  RETURN
```

PROGRAM 7 EXPLANATION:

Line 10: Clear the status of the HP-IB.

Line 20: Clear the status of the 8350A.

Line 30: Preset the 8350A to a predefined instrument state enable the square wave modulation, and set the Request Mask to enable Parameter Altered and Syntax Error SRQ's.

Line 40: Indicate that if an interrupt from the 98034A HP-IB Interface is received that program execution will branch to the interrupt service routine located at the line labelled 'Srq'.

Line 50: Specify an interrupt from the 98034A if bit 7 (decimal value 128) is set.

Table 1. 8350A Status Byte Descriptions

STATUS BYTE (#1)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	N/A	REQUEST SERVICE (RQS)	SRQ on Syntax Error	SRQ on End of Sweep	N/A	SRQ on Change in Extended Status Byte	N/A	SRQ on Numeric Parameter Altered to Default Value

EXTENDED STATUS BYTE (#2)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	Airflow Failure	*RF Unleveled	Power Failure/on	N/A	N/A	N/A	N/A	Self Test Failed

*Bit/Functions not usable with 86200 Series Plug-ins and 11869A Adapter.

Line 60: Enable the controller to accept an interrupt from the 98034A.

Line 70: The 9845B displays "CW Freq (GHz) = ?", input prompts for the desired CW frequency value in GHz. Store it in the variable 'F'.

Line 80: Set the CW frequency as determined by 'F'.

Line 90: Wait 100 milliseconds to allow the 8350A to interrupt.

Line 100: Go to line 70.

Line 110: Location of the interrupt service routine. Read the Status Byte of the 8350A and store it in 'A'.

Line 120: Check bit 6 of the 8350A Status Byte to see if it generated the SRQ, go to line 160 if not.

Line 130: Check bit 0 of the 8350A Status Byte for an Altered Parameter error. Print on the CRT display "Parameter Altered" if one exists.

Line 140: Check bit 5 of the 8350A Status Byte for a Syntax error. Print on the CRT display "Syntax Error" if one exists.

Line 150: Clear the 8350A Status Byte to enable another SRQ.

Line 160: Re-specify bit 7 of the 98034A to cause an interrupt.

Line 170: Re-enable interrupts from the 98034A.

Line 180: Return from the interrupt service routine to the main program.

The equipment setup is the same as the previous example. Reset the 9845B, scratch the 9845B memory, then type in the above program. Run the program. The 8350A will undergo an instrument preset and enable the square wave modulation. The 9845B then displays "CW Freq (GHz) = ?". Answer this prompt by inputting the desired CW frequency in GHz, then press CONT. Verify that the 8350A CW frequency has been properly programmed. Try several values that are out of range of the plug-in's frequency limits and verify that an error message was printed on the CRT display. The program repeats the above input prompt. To stop the program press STOP.

HP-IB PROGRAM CODES

Code	Description
AKm	Amplitude Marker On/Off
ALmn	Alternate Sweep On/Off
A1	Internal Leveling
A2	External Crystal Leveling
A3	External Power Meter Leveling
BK	Backspace
CAm	Amplitude Crystal Marker On/Off (83522/83525 Only)
CF	Center Frequency
CIm	Intensity Crystal Marker On/Off (83522/83525 Only)
CW	CW Frequency
C1	1 MHz Crystal Marker Frequency (83522/83525 Only)
C2	10 MHz Crystal Marker Frequency (83522/83525 Only)
C3	50 MHz Crystal Marker Frequency (83522/83525 Only)
C4	External Crystal Marker Frequency (83522/83525 Only)
DF	Delta F Frequency Span
DM	dBm
DN	Step Down/Decrement
DPm	Display Blanking On/Off
DUm	Display Update On/Off
E	Exponent Power Of 10
FA	Start Frequency
FB	Stop Frequency
FIm	CW Filter In/Out
F1	−20 MHz/V FM
F2	−6 MHz/V FM
GZ	GHz
HZ	Hz
IL	Input Learn String
IP	Instrument Preset
IX	Input Micro Learn String
KZ	KHz
MC	Marker To Center Frequency
MDm	Square Wave Amplitude Modulation On/Off
MO	Marker Off
MPm	Marker 1-2 Sweep On/Off
MS	Milliseconds
MZ	MHz
M0	Marker Off
M1	Marker #1
M2	Marker #2
M3	Marker #3
M4	Marker #4
M5	Marker #5
NT	Network Analyzer Trigger (8410B)
OA	Output Active Parameter
OL	Output Learn String
OM	Output Mode String
OP	Output Interrogated Parameter
OS	Output Status Bytes
OX	Output Micro Learn String
PL	Power Level
PSm	Power Sweep On/Off
RCn	Recall Register
RFm	RF Power On/Off
RM	Service Request Mask
RPm	RF Blanking On/Off
RS	Reset Sweep
SC	Seconds
SF	Frequency Step Size
SH	Shift Function
SLm	Slope On/Off
SM	Manual Sweep
SP	Power Step Size
SS	Step Size
ST	Sweep Time
SVn	Save Register
SX	external Sweep
TS	Take Sweep
T1	Internal Sweep Trigger
T2	Line Sweep Trigger
T3	External Sweep Trigger
T4	Single Sweep
UP	Step Up/Increment
VR	CW Vernier
0–9 + −	Acceptable Numeric Data

NOTES

1. **Program codes of the form "XXm" use "m" to turn the function On or Off (1 or 0). For the storage register functions the "n" is 1 through 9.**
2. **The 8350A ignores spaces, plus signs, negative signs (except when valid) and any unexpected characters. Program codes can be upper or lower case alpha characters.**

For more information, call your local HP Sales Office or nearest Regional Office: **Eastern** (201) 265-5000; **Midwestern** (312) 255-9800; **Southern** (404) 955-1500; **Western** (213) 970-7500; **Canadian** (416) 678-9430. Ask the operator for instrument sales. Or write Hewlett-Packard, 1501 Page Mill Road, Palo Alto, CA 94304. **In Europe:** Hewlett-Packard S.A., 7, rue du Bois-du-Lan, P.O. Box, CH 1217 Meyrin 2, Geneva, Switzerland. **In Japan:** Yokogawa-Hewlett-Packard Ltd., 29-21, Takaido-Higashi 3-chome, Suginami-ku, Tokyo 168.

5952-9307

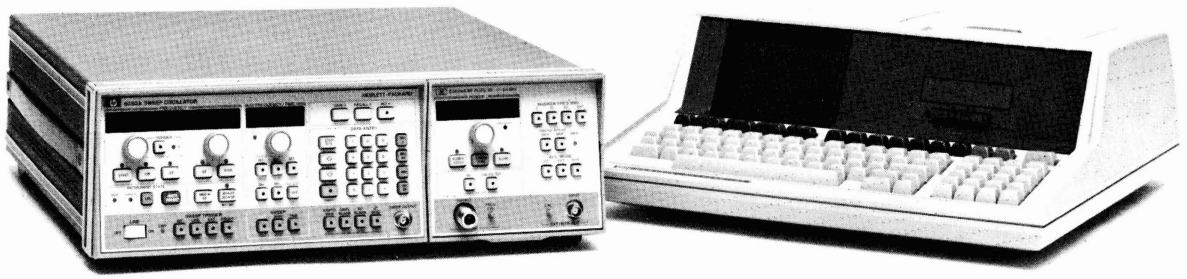
Printed in U.S.A.

DESIGNED FOR HP-IB SYSTEMS

Programming Note

8350A/85-1
Supersedes: None

Introductory Operating Guide for the HP 8350A Sweep Oscillator with the HP 85A Personal Computer



INTRODUCTION

This programming note is a guide to the remote operation of the HP 8350A Sweep Oscillator and appropriate HP 83500 Series Plug-in using the HP 85A Personal Computer. Included in this guide are the system connections for remote operation and several example programs with descriptions of each step.

The 8350A is fully compatible with the Hewlett-Packard Interface Bus (HP-IB). When used with a controller such as the 85A, complete control of the sweep mode, frequency limits, frequency markers, power level, and all other front panel controls can be achieved.

REFERENCE INFORMATION

For further information on the HP Interface Bus, the following references should prove helpful:

- Condensed Description of the Hewlett-Packard Interface Bus (HP Literature No. 59401-90030).

Complete reference information on the 8350A can be found in the 8350A Sweep Oscillator Operating and Service Manual (HP Part No. 08350-90001). For information on operating the 85A the following references are available:

- 85A Owner's Manual and Programming Guide (HP Part No. 00085-90002).
- 85A I/O Programming Guide (HP Part No. 00085-90142).

HEWLETT PACKARD

EQUIPMENT REQUIRED

To perform all the example programs as described in this programming note, you will need the following equipment and accessories:

1. HP 8350A Sweep Oscillator with any HP 83500 Series Plug-in. Note that an HP 86200 Series Plug-in with the HP 11869A Adapter can be used but all references to power level and power control are not applicable.

2. HP 85A Personal Computer with:

   a. HP Part No. 00085-15003 I/O ROM

   b. HP 82936A ROM Drawer

   c. HP 82937A HP-IB Interface Card/Cable

NOTE

The following equipment is not required for the programs to function but rather for a visual display of the 8350A functions.

3. HP 8755S Frequency Response Test Set with:

   a. HP 8755C Swept Amplitude Analyzer

   b. HP 180TR or 182T Display Unit

   c. HP 11664A or 11664B Detector

   d. Two 120 centimetre BNC cables (HP 11170C variety)

   or any appropriate Oscilloscope with Crystal/ Schottky Detector, Attenuator, and BNC Cabling.

4. Any test device over the frequency range of the 83500 Series Plug-in.

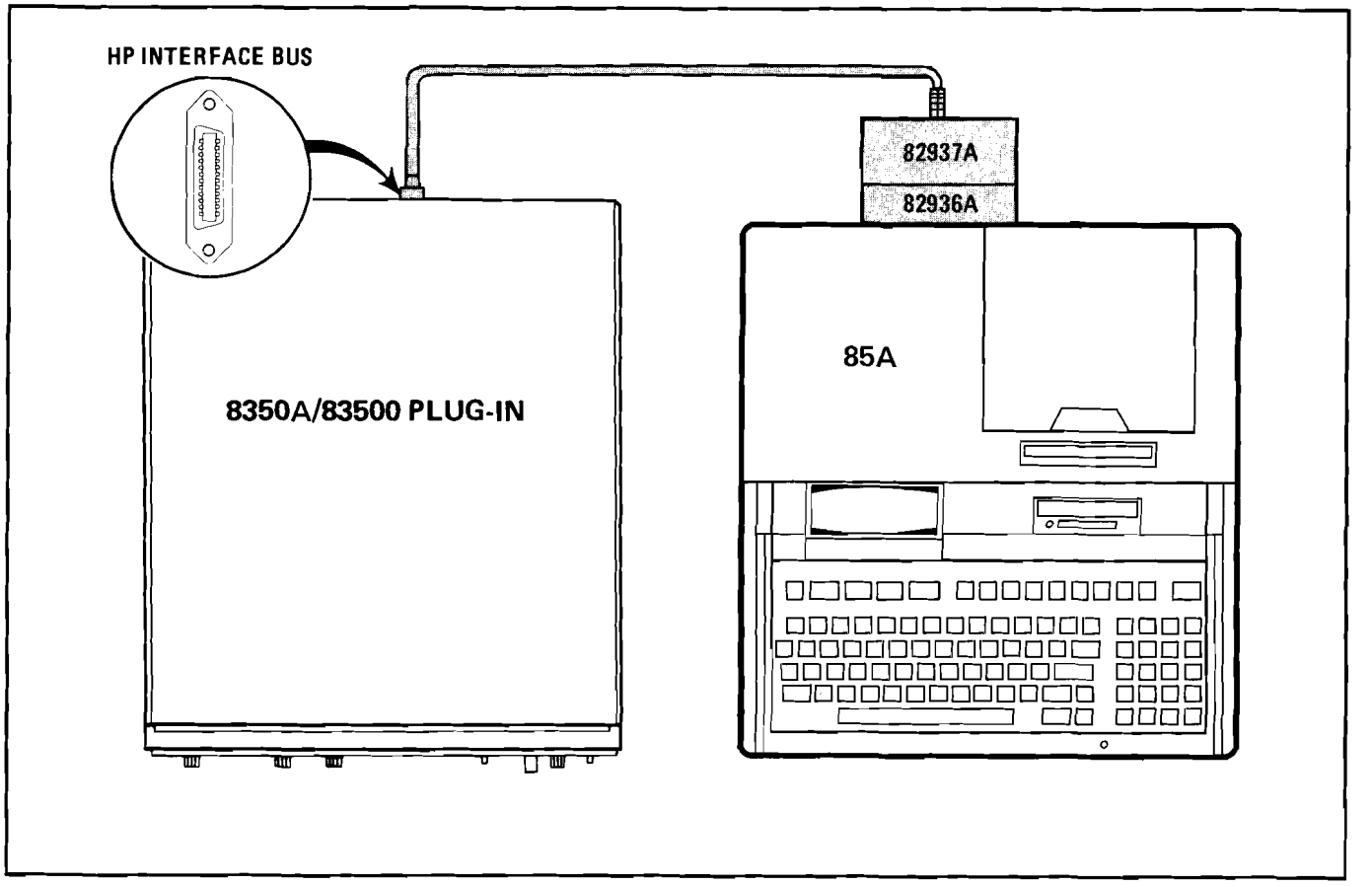


FIGURE 1: System Connection

SET-UP

Figure 1 shows the system connection and switch settings for the 82937A HP–IB Interface and the 85A Personal Computer. The following procedure completes the setup:

1. Turn off the power to the 85A.
2. Verify that the ROM is installed in the 85A. If not, then install the ROM in the 82936A ROM Drawer then insert the drawer in one of the rear panel slots of the 85A.
3. Install the 82937A HP–IB Interface Card into one of the rear panel slots of the 85A.
4. Connect the 24-pin HP-IB connector of the 82937A to the rear panel HP-IB connector of the 8350A. This connector is tapered to insure proper connection.

   CAUTION

   Do not attempt to mate black metric threaded screws on one connector with silver English threaded nuts on another connector, or vice-versa, as damage may result. A metric conversion kit which will convert one cable and one or two instruments to metric hardware is available by ordering HP Part No. 5060-0138.

5. All programs within this guide expect the 8350A HP-IB address to be decimal 19. The 8350A HP-IB address switches are located inside the instrument and are factory preset to decimal 19. To find the present HP-IB address use the front panel "Set HP-IB Address" by executing:

   Press **SHIFT** **LCL**

   The FREQUENCY/TIME display will indicate the present decimal address. To reset the number displayed if not 19:

   Press **1** **9** **GHz**

   This HP-IB address will remain in effect until the instrument is powered off since the internal address switches are read at power on (unless 8350A Option 001 Non-volatile Memory is used). Since Example 4 requires the 8350A to be powered off and then on, the internal address switches should be reset to 19 if necessary.

CHECK-OUT

Turn on the 85A and the 8350A. The 85A should display the cursor ("–") in the upper left corner of the CRT display. The 8350A should undergo a turn-on self test consisting of the red LED numeric displays being blanked and all yellow indicator LED's on, then the 8350A sweep controls are set to the instrument preset state: Start/Stop Sweep over the entire plug-in frequency range, fastest sweep time for plug-in (typically 10 milliseconds), and maximum leveled output power for the plug-in. If the 8350A fails the power-on self test an error message will be displayed in the far left LED display. Check section 8 of the 8350A Operating and Service Manual for error message decoding and diagnostics.

To verify that the HP-IB connections and interface are functional perform the following on the 85A:

1. Press **SHIFT** **RESET**
2. Type 'REMOTE 719'
3. Press **END LINE**

Verify that the REMote light on the 8350A is lit. If this fails, verify that the 82937A select code switch is set to "7" (this switch is located inside the 82937A so refer to its Installation Manual), the 8350A address switches are set to "19", and the interface cable is properly connected.

If the 85A display indicates an error message, it is possible that the above remote message was typed in incorrectly or the ROM's are not properly installed. If the 85A accepts the remote statement and the display is clear but the 8350A REMote light does not turn on, you could have a defective 82937A or 8350A. Perform the operational checks as outlined in the respective Operating and Service Manuals to find the defective device.

PROGRAMMING EXAMPLES

The following sample programs show the various ways of controlling the 8350A. In remote control situations the 8350A Sweep Oscillator can interact with the system HP-IB controller in two basic ways:

1. "Listen Mode": The 8350A listens to the control commands as to modifying the present instrument state. This effectively commands the 8350A to do a specific event much like setting a front panel function.
2. "Talk Mode": The 8350A informs the controller of the present instrument state with a numeric value or a string of characters. This effectively allows the user to interrogate or learn any 8350A function.

Each programming example is structured using the following format:

1. A general description of the functions exercised.
2. The program listing.
3. An explanation of each program line.
4. Detailed instructions for operating the system.

EXAMPLE PROGRAM 1: Remote, Local, Local Lockout, and Instrument Preset

Before programming the 8350A for different sweep functions, the user should be aware of the extent of remote control that can be used. The Remote Enable ('REMOTE') command sets the 8350A into remote control from the local (manual) mode. In remote the 8350A will perform only as its functions are programmed. However if the LOCAL button is pressed, the 8350A will return from the remote state to local control. To prevent this from occurring the Local Lockout ('LOCAL LOCKOUT') command disables all front panel controls, specifically the "Local" key. The Go To Local ('LOCAL') command will return the 8350A to front panel control thereby removing it from the remote and local lockout modes. Note that the above remote and local commands are different from the general HP-IB bus local and remote commands ('LOCAL 7' and 'REMOTE 7'). Finally, in remote control it is periodically desirable to reset the 8350A to a predefined state, this is achievable with the Instrument Preset function.

PROGRAM 1

```
 10 REMOTE 719
 20 DISP "Remote"
 30 PAUSE
 40 REMOTE 719
 50 LOCAL LOCKOUT 7
 60 DISP "Local Lockout"
 70 PAUSE
 80 LOCAL 719
 90 DISP "Local"
100 PAUSE
110 OUTPUT 719 ;"IP"
120 END
```

PROGRAM 1 EXPLANATION:

Line 10: Sets 8350A to remote.
Line 20: The 85A displays "Remote'.
Line 30: Temporarily stops program execution.
Line 40: Sets 8350A to remote.
Line 50: Sets local lockout mode.
Line 60: The 85A displays "Local Lockout".
Line 70: Temporarily stops program execution.
Line 80: Sets 8350A to local.
Line 90: The 85A displays "Local".
Line 100: Temporarily stops program execution.
Line 110: Sets 8350A to remote and performs an Instrument Preset.
Line 120: Stops program execution.

To verify and investigate the different remote modes do the following:

1. Press CONTROL RESET SCRATCH END LINE on the 85A. This scratches the program memory.
2. Press INSTR PRESET on the 8350A.
3. Type in the above program.
4. Press SHIFT CLEAR RUN on the 85A.
5. With the 85A displaying "Remote", verify that the 8350A REMote light is lit. From the front panel, attempt to change the start frequency and verify that this is impossible. Verify that the Instrument Preset key and all other keys except LCL are disabled. Now press the LCL key and verify that the 8350A REMote light is off and that you can modify any of the sweep functions.
6. Press CONT on the 85A. With the 85A displaying "Local Lockout" verify that the 8350A REMote light is again lit. Again attempt to change the start frequency and perform an instrument preset. Verify that this is impossible. Now press the 8350A LCL key and verify that still no action is taken.
7. Press CONT on the 85A. With the 85A displaying "Local" verify that the 8350A REMote light is off. Also verify that all sweep functions now can be modified via the front panel controls.
8. Press CONT on the 85A. Verify that the 8350A has undergone an Instrument Preset and the REMote light is on. The Output ('OUTPUT 719') statement does two things, one it performs a 'REMOTE 719', and second it passes data to the 8350A.

Note that the 8350A LCL key produces the same result as programming 'LOCAL 719' or 'LOCAL 7'. Be careful as the latter command places all instruments on the HP-IB in local state as opposed to the 8350A alone.

EXAMPLE PROGRAM 2: Programming Functions

To program any function on the 8350A the controller must pass specific program codes and data to the sweeper. The statement that allows this is the Output ('OUTPUT') statement. The alphanumeric data string of the output statement can be a concatenation of character strings and/or variables. The data can be specific codes, free field formatted data, or reference a specific image ('IMAGE') statement. For example, to program the CW Frequency (CW), one program code sequence is "CW", followed by the frequency in GHz, then "GZ". If the frequency is to be 7.555 GHz, then the string "CW7.555GZ" will suffice. However if the frequency were to change then a variable 'F' could indicate the frequency in GHz and the program string could be "CW",F,"GZ". Using an image statement also allows a specific number of digits to be passed, thereby avoiding any unexpected round off errors.

NOTE

This program expects an 83500 Series Plug-in that covers the frequency 7.555 GHz. If using a plug-in that does not cover this frequency then the value in lines 20 and 30 should be changed to an appropriate value.

PROGRAM 2

```
10 OUTPUT 719 ;"IP"
20 OUTPUT 719 ;"CW7.555GZ"
30 DISP "CW=7.555 GHz"
40 PAUSE
50 DISP "CW=(in GHz)=";
60 INPUT F
70 PRINT "CW=";F;"GHz"
80 OUTPUT 719 ;"CW";F;"GZ"
90 GOTO 50
100 IMAGE "CW",DD.DDD,"GZ"
110 OUTPUT 719 USING 100 ; F
120 GOTO 50
```

PROGRAM 2 EXPLANATION:

Line 10: Puts the 8350A into a predefined state via instrument preset.
Line 20: Puts the 8350A in CW mode and programs a CW frequency of 7.555 GHz.
Line 30: The 85A displays "CW = 7.555 GHz".
Line 40: Temporarily stops program execution.
Line 50: The 85A displays "CW (in GHz) =?".
Line 60: The user is prompted to input a new CW frequency value which is stored in the variable 'F'.
Line 70: Print on the CRT display the programmed CW frequency.
Line 80: Program the CW frequency using the default data format.
Line 90: Go to line 50.
Line 100: Image statement is set up for programming the CW frequency with a 1 MHz resolution.
Line 110: Program the CW frequency via image statement in line 100.
Line 120: Go to line 50.

The equipment setup is the same as the previous example. Reset the 85A, scratch the 85A memory, then type in the above program. Then perform the following:

1. Clear the 85A CRT display then run the program. The 85A displays "CW = 7.555 GHz". The 8350A changes from the instrument preset state of Start/Stop sweep to a CW frequency of 7.555 GHz.

2. Press CONT on the 85A. The 85A now displays "CW (in GHz) =?". Type in a new CW frequency (value in GHz), then press END LINE

3. The 8350A will be programmed to the new CW frequency with the new value printed on the internal printer. The program jumps back to step (2) above.

When inputting the CW frequency try several values, each with a different number of digits after the decimal point. Notice that the 8350A displays the frequency to 3 decimal places (1 MHz frequency resolution). Values with better than 1 MHz frequency resolution are rounded to the nearest MHz by the 8350A. However the 85A outputs data in a free-field format that outputs a number with all appropriate significant digits. Another approach is to utilize the image statement to set the desired number of decimal places. To use the image statement in the program, perform the following on the 85A:

Press PAUSE SHIFT CLEAR
Type 'DELETE 80, 90'
Press END LINE

This should delete lines 80 and 90 from program #2 and allow the use of lines 100, 110, and 120 instead. Run the modified program again and use the same steps for operation as before. Now if the value inputted has a frequency resolution greater than 1 MHz the 85A does the rounding instead of the 8350A. This is the preferred programming approach. Change the image statement for 10 MHz frequency

resolution and verify the results from the 8350A frequency display.

Since a device select code address can be a variable, verify that this can be used in the modified or original program #2 by doing the following:

1. Insert before line 10 a new line with the variable 'S' by:

   Press PAUSE SHIFT CLEAR
   Type '5 S=719'
   Press END LINE

2. Modify the output statement(s) by editing the necessary lines and changing the 'OUTPUT 719' to 'OUTPUT S' and 'OUTPUT 719 USING 100' to 'OUTPUT S USING 100'.

3. Re-run the modified program using the same operation steps as above.

EXAMPLE PROGRAM 3: Setting Up A Typical Sweep

Typically the sweeper is programmed for the proper sweep frequency range, sweep time, power level, and marker frequencies for a test measurement. This program sets up the sweeper for a general purpose situation using several dedicated image statements. Note that not all parameters need to be reprogrammed every time.

NOTE

This program expects an 83500 Series Plug-in that covers the frequency range of at least 3 to 7 GHz. If using a plug-in with a different frequency range, change the values in lines 60, 90, and 100, to the appropriate values. If using an 86200 Series Plug-in then do not enter line 70.

PROGRAM 3

```
 10 IMAGE "FA",DD.DDD,"GZFB",DD.
    DDD,"GZ"
 20 IMAGE "ST",DDDDD,"MS"
 30 IMAGE "M",D,DD.DDD,"GZ"
 40 IMAGE "PL",DDD.DD,"DM"
 50 OUTPUT 719 "IPMD1"
 60 OUTPUT 719 USING 10 ; 3,7
 70 OUTPUT 719 USING 40 ; 10
 80 OUTPUT 719 USING 20 ; 50
 90 OUTPUT 719 USING 30 ; 1,4
100 OUTPUT 719 USING 30 ; 2,6
110 END
```

PROGRAM 3 EXPLANATION:

Line 10: Image statement for setting the Start and Stop Sweep frequencies in GHz.
Line 20: Image statement for setting the Sweep Time in milliseconds.
Line 30: Image statement for setting a Frequency Marker by marker number and frequency in GHz.
Line 40: Image statement for setting the Output Power Level in dBm.
Line 50: Preset the sweeper to a known state via instrument preset and enable the internal 27.8 kHz Square Wave Amplitude Modulation.
Line 60: Set a Start/Stop Sweep of 3.0 to 7.0 GHz.
Line 70: Set the Output Power Level to +10 dBm.
Line 80: Set the Sweep Time to 50 milliseconds.
Line 90: Set Marker #1 to 4 GHz.
Line 100: Set Marker #2 to 6 GHz.
Line 110: Stop program execution.

Setup the equipment as shown in figure 2 by adding the 8755C, the 180TR or 182T, the 11664, and a test device like a 4 to 6 GHz Bandpass Filter. It is important that the two rear panel connections from the 8350A to the 8755C/182T are made for a proper CRT display. For the example measurement set the following front panel controls:

On the 8755C:
  Channel 1:
    Display ..... OFF (press all the display push buttons so that they are all out)
  Channel 2:
    Display ..... B
    dB/DIV ..... 10 dB
    Reference Level ..... −10 dB
    Reference Level Vernier ..... OFF
On the 182T or 180TR:
  Magnifier X1
  Display ..... INT

After connecting the equipment: reset the 85A, scratch the 85A memory, then type in the above program. Clear the 85A CRT display then run the program. The 8350A will initially undergo an instrument preset which will set the proper power leveling mode and sweep blanking signals. Since the 8755C requires the RF signal to be modulated at a 27.8 kHz rate, the internal amplitude modulation is

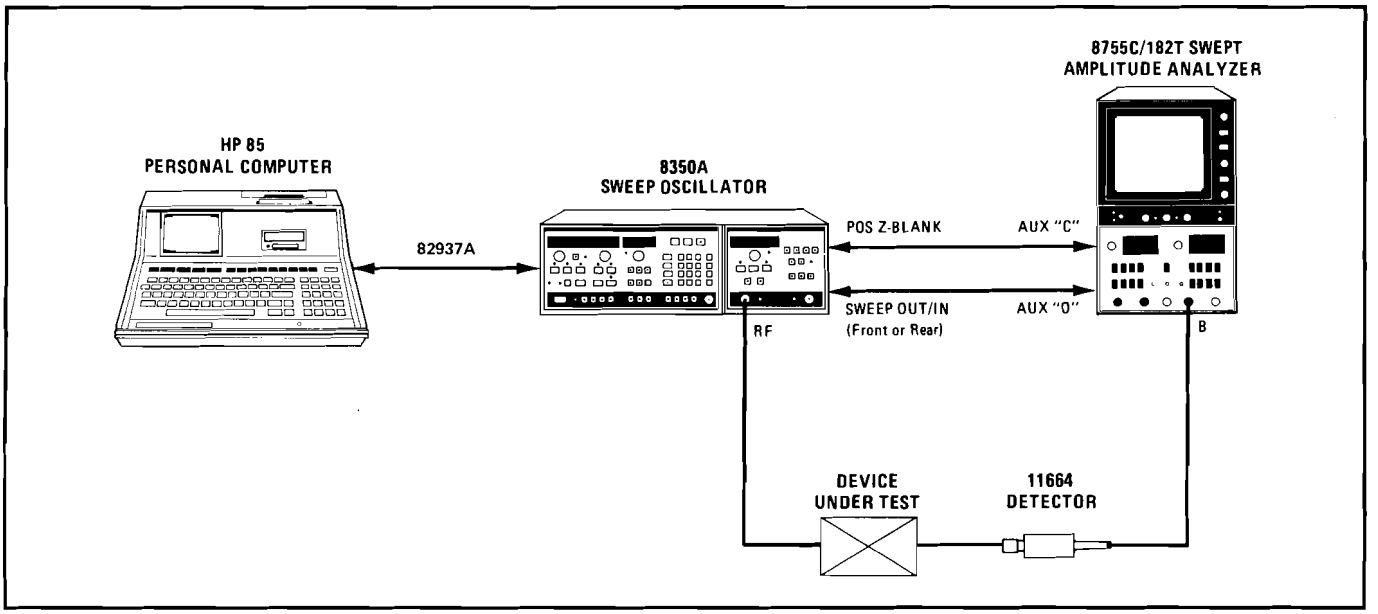


FIGURE 2: Equipment Setup For Program #3

enabled. If using a 4 to 6 GHz Bandpass Filter as the test device, the CRT display should reflect the filter transmission response over the 3 to 7 GHz range. Two frequency markers of the Z-Axis Intensity dot variety are set to 4 and 6 GHz, hopefully within the passband or near the 3 dB points. The setup can be modified by changing the values in lines 60, 70, 80, 90, and/or 100, then re-run the program.

EXAMPLE PROGRAM 4: Learning An Instrument State

Being able to save a specific instrument state is helpful when it is needed several times in a test or measurement procedure. The user could save the instrument state by manually logging the important sweep parameters such as frequency range, power level, ALC modes, etc., then re-inputting them at the appropriate time. A somewhat simpler approach is to save the instrument state in one of the 8350A internal storage registers, then recall it when needed. However, this is not a permanent solution unless the 8350A Non-volatile Memory option (Option 001) is used. A more permanent solution is to use the Output Learn String function of the 8350A so that the 85A can learn then store a data string that describes the present instrument state on a tape cartridge or in its' internal memory. Once an instrument state is stored or learned, the 8350A can then be restored to that state using the Input Learn String function. The power of these instrument Learn/Teach functions are demonstrated by the following program using the 85A fast data transfer function.

PROGRAM 4

```
 10 OPTION BASE 1
 20 DIM A$[100]
 30 IOBUFFER A$
 40 OUTPUT 719 ;"IPMD1"
 50 LOCAL 719
 60 PAUSE
 70 OUTPUT 719 ;"OL"
 80 TRANSFER 719 TO A$ FHS ; EOI
 90 A$=A$[1,90]
100 PAUSE
110 OUTPUT 719 ;"IL"&A$
120 END
```

PROGRAM 4 EXPLANATION:

Line 10: Define the first element of any array to be at index number 1.

Line 20: Set the length of the A$ string to 100 characters.

Line 30: Set up the string A$ as an I/O Buffer for data storage in fast read/write data transfer operations.

Line 40: Set the 8350A to a predefined state via instrument preset and enable the square wave modulation.

Line 50: Return the 8350A to local control.

Line 60: Temporarily stop program execution.

Line 70: Program the 8350A to output the Learn String.

Line 80: Read the Learn String into the 85A via the fast data transfer function using the HP-IB EOI (End or Identify) signal to terminate the transfer. Store the Learn String in A$.
Line 90: Extract the Learn String information from the I/O Buffer by removing the buffer pointers. Re-save the Learn String only in A$.
Line 100: Temporarily stop program execution.
Line 110: Program the 8350A to accept a Learn String, then send the new Learn String to the 8350A.
Line 120: Stop program execution.

Setup the equipment as in example 3 using the analyzers' CRT display to verify the sweep settings. Note that the original equipment setup can also be used with the 8350A front panel indicators used for verification. Reset the 85A, scratch the 85A memory, then type in the above program. Clear the 85A CRT display then run the program. The 8350A will undergo an instrument preset, enable the square wave modulation, then return to local front panel control. Then perform the following:

1. Adjust the 8350A to a preferred instrument state, then press **CONT** on the 85A.

2. Turn the 8350A line power off. Wait five seconds then turn the 8350A power back on. Press **INSTR PRESET** on the 8350A.

3. Press **CONT** on the 85A. Verify on the analyzers' CRT display and/or the 8350A that the original instrument state has been restored.

EXAMPLE PROGRAM 5: Interrogating The Present Value Of A Function

While the 8350A Learn String enables the user to completely save a string of characters that define the present instrument state, the information is densely packed and encoded to save memory space. If the user wishes to determine the actual value of a specific parameter, say the Start Frequency, it would require a tedious process to extract a numeric value from several characters within the Learn String. An easier approach is to use the Output Interrogated Parameter function of the 8350A. With this function the 85A instructs the 8350A to output the present numeric value of a specified function. Any function that has a numeric value associated with it (except Step Size) can be interrogated. Note that if the parameter is not presently active, the 8350A uses a computed value or its previous value. The following program demonstrates the capability of the interrogate function.

PROGRAM 5

```
10 OUTPUT 719 ;"IPMD1"
20 LOCAL 719
30 PAUSE
40 OUTPUT 719 ;"OPFA"
50 ENTER 719 ; A
60 PRINT "Start Freq=";A/100000
   0;"MHz"
70 OUTPUT 719 ;"OPFB"
80 ENTER 719 ; B
90 PRINT "Stop Freq=";B/1000000
   ;"MHz"
100 OUTPUT 719 ;"OPST"
110 ENTER 719 ; T
120 PRINT "Sweep Time=";1000*T;"
   msec"
130 END
```

PROGRAM 5 EXPLANATION:

Line 10: Set the 8350A to a predefined instrument state via instrument preset and enable the square wave modulation.
Line 20: Return the 8350A to local control.
Line 30: Temporarily stops program execution.
Line 40: Program the 8350A to output the present value of the Start Frequency.
Line 50: Read the value into the 85A and store it in the variable 'A'.
Line 60: Print on the internal printer the present value of the Start Frequency in MHz.
Line 70: Program the 8350A to output the present value of the Stop Frequency.
Line 80: Read the value into the 85A and store it in the variable 'B'.
Line 90: Print on the internal printer the present value of the Stop Frequency in MHz.
Line 100: Program the 8350A to output the present value of the Sweep Time.
Line 110: Read the value into the 85A and store it in the variable 'T'.
Line 120: Print on the internal printer the present value of the Sweep Time in milliseconds.
Line 130: Stops program execution.

Setup the equipment as in example 3 using the analyzers' CRT display to verify the sweep settings. Note that the original equipment setup can also be used with the 8350A front panel indicators used for verification. Reset the 85A, scratch the 85A memory, then type in the above program. Clear the 85A CRT display then run the program. The 8350A will

undergo an instrument preset, enable the square wave modulation, then return to local front panel control. Then perform the following:

1. Adjust the 8350A to a preferred instrument state using the Start Frequency, Stop Frequency, and Sweep Time controls.
2. Press CONT on the 85A.
3. The present values of the Start Frequency, Stop Frequency, and Sweep Time are sequentially interrogated and then printed on the internal printer of the 85A.

EXAMPLE PROGRAM 6: A Stepped CW Sweep

Present automatic measurement systems typically make measurements at a sequence of CW test frequencies instead of analog sweeping the frequency range of interest. If swept, the measurement data taking machine would need to sample the RF signal at a very fast rate to maintain accurate frequency information, too. This is typically not accomplished. Stepped CW sweeps can be accomplished in several ways with the 8350A:

1. Program sequential CW test frequencies.
2. Program the frequency sweep range then enable the manual sweep mode. Perform a stepped manual sweep by repetitively programming the step up/increment function.
3. Program the CW frequency to the start frequency, the Step Size to an appropriate value, then repetitively program the step up/increment function.

Considering the speed of programming the above approaches, the third is the most efficient time wise. This program illustrates a stepped sweep using this approach.

PROGRAM 6

```
10 OUTPUT 719 ;"IPMD1"
20 DISP "Start Freq (GHz)="
30 INPUT A
40 DISP "Stop Freq (GHz)=";
50 INPUT B
60 DISP "Step Size (GHz)=";
70 INPUT C
80 D=(B-A)/C
90 OUTPUT 719 ;"CWSS";C;"GZ"
100 OUTPUT 719 ;"CW";A;"GZ"
110 FOR I=1 TO D
120 OUTPUT 719 ;"UP"
130 WAIT 20
140 NEXT I
150 GOTO 100
```

PROGRAM 6 EXPLANATION:

Line 10: Set the 8350A to a predefined instrument state and enable the square wave modulation.
Line 20: The 85A displays "Start Freq (GHz) = ?".
Line 30: Input prompts for start frequency of the sweep. Store it in the variable 'A'.
Line 40: The 85A displays "Stop Freq (GHz) = ?".
Line 50: Input prompts for the stop frequency of the sweep. Store it in 'B'.
Line 60: The 85A displays "Step Size (GHz) = ?".
Line 70: Input prompts for the step size of the sweep. Store it in 'C'.
Line 80: Determine the number of frequency steps in sweep, store in 'D'.
Line 90: Set the CW Step Size.
Line 100: Set the CW frequency to the start frequency value.
Line 110: Iterate the CW step 'D' times.
Line 120: Program the Step Increment/Up function.
Line 130: Wait 20 milliseconds for settling.
Line 140: Continue step iteration.
Line 150: Go to line 100.

The equipment setup is the same as in the previous example. Reset the 85A, scratch the 85A memory, then type in the above program. Clear the 85A CRT display then run the program. The 8350A will undergo an instrument preset and enable the square wave modulation. Then perform the following:

1. The 85A will display "Start Freq (GHz) = ?". Answer this prompt by inputting the desired Start frequency (value in GHz) of the sweep, then press END LINE
2. The 85A will display "Stop Freq (GHz) = ?". Answer this prompt with the desired Stop frequency (in GHz) of the sweep, then press END LINE
3. The 85A will display "Step Size (GHz) = ?". Answer this prompt with the desired Step size (in GHz) of the sweep, then press END LINE
4. The 8350A CW frequency will be programmed to the Start frequency of the sweep selected. Then the CW frequency is repetitively incremented by the step size value. The sweep is then restarted after reaching the stop frequency.

To stop the program press STOP .

Since part of the time involved in changing CW frequencies is in updating the numeric LED display if this could be defeated the CW frequency time can be optimized. Note that one drawback is that the numeric display will not indicate the present frequency. The 8350A provides a Display Update On/Off function and it can be implemented by modifying line 10 to be:

OUTPUT 719 ;"IPMD1DU0"

Then re-run the modified program using the same operation steps as above.

EXAMPLE PROGRAM 7: Using Service Requests, Status Bytes, and Request Mask

Certain error conditions of the 8350A can be detected by the 85A so that corrective action can be taken. Examples of some detectable error conditions are RF power unleveled, numeric data entry out of range, and line power failure. If an error condition exists, the user can instruct the 8350A to request service from the 85A by initiating a Service Request (SRQ). The 85A can detect whether an SRQ has taken place on the bus by analyzing bit 7 (see note below) of the Status Byte of the 82937A HP-IB Interface. Two modes are available for analyzing the 82937A Status Byte: 1) periodically read the Status Byte, or 2) enable bit 7 to interrupt the program when it is set. In either case, once it is determined that the 8350A has requested service, the specific error condition(s) can then be determined by reading and analyzing the Status Bytes of the 8350A. The 8350A has two Status Bytes, each consisting of 8 bits with each bit indicating the present status of a particular function or condition. See Figure 3 for a complete description of the conditions associated with each Status Byte bit. The user can analyze these Status Bytes for every SRQ, or more simply, instruct the 8350A to issue an SRQ only if a specific set of error conditions exists. The set of conditions is determined by a numeric value passed by the Request Mask function. This numeric value is generated by summing the decimal values of each Status Byte bit to be checked. This program demonstrates the capability of the SRQ and Status Bytes to detect an error condition.

TABLE 1: 8350A Status Byte Descriptions

STATUS BYTE (#1)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	Front Panel SRQ REQUEST	REQUEST SERVICE (RQS)	SRQ on Syntax Error	SRQ on End of Sweep	*SRQ on RF Settled	SRQ on Change in Extended Status Byte	SRQ on Front Panel Entry Complete	SRQ on Numeric Parameter Altered to Default Value

EXTENDED STATUS BYTE (#2)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	N/A	*RF Unleveled	Power Failure	*RF Unlocked	*External Freq. Ref. Selected	*Oven Cold	*Over Modulation	Self Test Failed

*Bit/Functions not usable with 86200 Series Plug-ins and 11869A Adapter.

NOTE

This assumes that the status bits are numbered 0 thru 7 with the least-significant bit being number 0. Other references may assume that the bits are numbered 1 thru 8 with the least-significant bit being number 1.

If using an 86200 Series Plug-in, the Status Bytes can provide only limited information. Table 1 indicates which Status Byte functions/bits are usable.

PROGRAM 7 †

```
 10 ABORTIO 7
 20 CLEAR 719
 30 OUTPUT 719 ;"IPMD1"
 40 ON INTR 7 GOSUB 110
 50 ENABLE INTR 7;8
 60 DISP "CW Freq (GHz)=";
 70 INPUT F
 80 OUTPUT 719 ;"CW";F;"GZ"
 90 WAIT 100
100 GOTO 60
110 STATUS 7,1 ; X
120 A=SPOLL(719)
130 IF BIT(A,0)=1 THEN PRINT "Pa
    rameter Altered"
140 IF BIT(A,5)=1 THEN PRINT "Sy
    ntax Error"
150 CLEAR 719
160 ENABLE INTR 7;8
170 RETURN
```

PROGRAM 7 EXPLANATION:

Line 10: Clear the status of the HP-IB.
Line 20: Clear the status of the 8350A.
Line 30: Preset the 8350A to a predefined instrument state and enable the square wave modulation.
Line 40: Indicate that if an interrupt from the 82937A HP-IB Interface is received that program execution will branch to the interrupt service routine located at the line 110.
Line 50: Specify and enable the controller to accept an interrupt from the 82937A if bit 3 (decimal value 8) is set.
Line 60: The 85A displays "CW Freq (GHz) = ?".
Line 70: Input prompts for the desired CW frequency value in GHz. Store it in the variable 'F'.
Line 80: Set the CW frequency as determined by 'F'.
Line 90: Wait 100 milliseconds to allow the 8350A to interrupt.
Line 100: Go to line 60.
Line 110: Read the 82937A interrupt cause register to enable another interrupt.
Line 120: Location of the interrupt service routine. Read the Status Byte of the 8350A and store it in 'A'.
Line 130: Check bit 0 of the 8350A Status Byte for an Altered Parameter error. Print on the internal printer "Parameter Altered" if one exists.
Line 140: Check bit 5 of the 8350A Status Byte for a Syntax Error. Print on the internal printer "Syntax Error" if one exists.
Line 150: Clear the status of the 8350A.
Line 160: Re-specify and re-enable bit 3 of the 82937A to cause an interrupt.
Line 170: Return from the interrupt service routine to the main program.

The equipment setup is the same as the previous example. Reset the 85A, scratch the 85A memory, then type in the above program. Clear the 85A CRT display then run the program. The 8350A will undergo an instrument preset and enable the square wave modulation. The 85A then displays "CW Freq (GHz) = ?". Answer this prompt by inputting the desired CW frequency in GHz, then press END LINE. Verify that the 8350A CW frequency has been properly programmed. Try several values that are out of range of the plug-in's frequency limits and verify that an error message was printed on the internal printer. The program repeats the above input prompt. To stop the program press PAUSE

† NOTE

For Program 7 to function properly change line 30 to: 30 OUTPUT 719; "IPMD1RM" & CHR$(97). This change enables bit 5 (SRQ on Syntax Error) and bit 0 (SRQ on Numeric Parameter to Default Value).

HP-IB PROGRAM CODES

CODE	DESCRIPTION
AKm	Amplitude Marker On/Off
ALmn	Alternate Sweep On/Off
A1	Internal Leveling
A2	External Crystal Leveling
A3	External Power Meter Leveling
BK	Backspace
CAm	Amplitude Crystal Marker On/Off (83522/83525 Only)
CF	Center Frequency
CIm	Intensity Crystal Marker On/Off (83522/83525 Only)
CW	CW Frequency
C1	1 MHz Crystal Marker Frequency (83522/83525 Only)
C2	10 MHz Crystal Marker Frequency (83522/83525 Only)
C3	50 MHz Crystal Marker Frequency (83522/83525 Only)
C4	External Crystal Marker Frequency (83522/83525 Only)
DF	Delta F Frequency Span
DM	dBm
DN	Step Down/Decrement
DPm	Display Blanking On/Off
DUm	Display Update On/Off
E	Exponent Power Of 10
FA	Start Frequency
FB	Stop Frequency
FIm	CW Filter In/Out
GZ	GHz
HZ	Hz
IL	Input Learn String
IP	Instrument Preset
IX	Input Micro Learn String
KZ	KHz
MC	Marker To Center Frequency
MDm	Square Wave Amplitude Modulation On/Off
MO	Marker Off
MPm	Marker 1-2 Sweep On/Off
MS	Milliseconds
MZ	MHz
M0	Marker Off
M1	Marker #1
M2	Marker #2
M3	Marker #3
M4	Marker #4
M5	Marker #5
NT	Network Analyzer Trigger (8410B)
OA	Output Active Parameter
OL	Output Learn String
OM	Output Mode String
OP	Output Interrogated Parameter
OS	Output Status Bytes
OX	Output Micro Learn String
PL	Power Level
PSm	Power Sweep On/Off
RCn	Recall Register
RFm	RF Power On/Off
RM	Service Request Mask
RS	Reset Sweep
SC	Seconds
SH	Shift Function
SLm	Slope On/Off
SM	Manual Sweep
SS	Step Size
ST	Sweep Time
SVn	Save Register
SX	External Sweep
TS	Take Sweep
T1	Internal Sweep Trigger
T2	Line Sweep Trigger
T3	External Sweep Trigger
T4	Single Sweep
UP	Step Up/Increment
VR	CW Vernier
0–9 + –	Acceptable Numeric Data

NOTES

1. **Program codes of the form "XXm" use "m" to turn the function On or Off (1 or 0). For the storage register functions the "n" is 1 through 9.**
2. **The 8350A ignores spaces, plus signs, negative signs (except for vernier, offset, and power values), and any unexpected characters. Program codes can be upper or lower case alpha characters.**

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5952-9308

Printed in U.S.A.

DESIGNED FOR HP-IB SYSTEMS

Programming Note

8350A/0000-2
Supersedes: None

SEPTEMBER 1980

Quick Reference Guide
for the HP 8350A Sweep Oscillator

INTRODUCTION

This programming note is a reference guide for the remote operation of the HP 8350A Sweep Oscillator and HP 85300 Series Plug-ins. This note is intended for use by those familiar with HP-IB programming and the basic functions of the HP 8350A Sweep Oscillator. For complete programming information refer to the HP 8350A Operating and Service manual.

INPUT DATA

The 8350A Sweep Oscillator and 83500 Series Plug-ins accept programming codes that contain information for programming all of the front panel and special HP-IB only functions except the Line switch and Set HP-IB Address. The programming data string consists of a string of ASCII coded characters composed of one or more the following control fields:

- Sweep Mode/Limits
- Frequency Markers
- Sweep Trigger
- Modulation/Blanking
- Step Size
- Instrument State/Registers
- Power Level
- Power Control
- ALC Modes
- Crystal Markers (83522/83525 Plug-ins only)
- Special HP-IB Only Functions

Input Syntax. The 8350A responds to program codes in the order in which they are received. Each function is programmed with a string of ASCII coded characters that follow one of the following sequences.

- [Function Code] [Numeric Value] [Units terminator] [EOS]
- [Function Code] [Numeric Value] [EOS]
- [Function Code] [EOS]

NOTE

The HP-IB program code sequence typically mirrors that of the local front panel keystroke sequence.

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Function Codes (Prefix Activate). Function codes are typically 2 to 4 character mnemonics. For functions that have a numeric value associated with it, passing the function code only will enable and activate the function for further data entry.

Numeric Value (Numeric Format). These are either a single decimal digit, a set of 14 characters or less representing a number, or a string of binary bytes. A string of 14 characters maximum can be expressed in exponential, decimal, or integer form. Acceptible numeric formats are referenced in further sections by the following format syntax:

Format #1: Exponential	±d***d.d***dE±dd
Format #2: Decimal	±d***d.d***d
Format #3: Integer	±d***d
Format #4: Single Digit	d
Format #5: Binary String	b***b
Format #6: Binary Byte	b

Where the character 'd' indicates a leading or trailing zero, a space, or a numeric digit (0 through 9). The character 'b' indicates an 8-bit binary byte. The characters "***" indicate a variable number of the previous character. Numeric values that are not binary in nature are scaled by the appropriate units terminator.

Units Terminator (Suffix). These are 2 character codes that terminate and scale the associated numeric value. Frequency values can be entered in GHz, MHz, kHz, or Hz. Sweep time values can be entered in seconds or milliseconds. Power values can be entered in dBm or dB. If a units terminator is not passed and a Line Feed (LF), semicolon (;) or comma (,) is encountered, the 8350A assumes the numeric value is in the fundamental units of Hz, seconds, or dB.

End Of String Message (EOS). This can be the ASCII characters Line Feed (LF, decimal 10), semicolon (";",decimal 59),comma(",",decimal 44) the bus EOI line true, or another function code string.

Valid Characters. The alpha program codes can be either upper or lower case since the 8350A will accept either type (they can be interchanged). Spaces, unnecessary signs (+,−), leading zeroes, and carriage returns (CR) are ignored.

Programming Data. See Table 1 for Input Programming Codes.

NOTE

If using an 83500 Series Plug-in that has Option 002 (70 dB Step Attenuator), the lifetime of the Step Attenuator will be reduced if using the Alternate Sweep function that alternates between two power levels using different Step Attenuator settings. Likewise rapid power level programming between step attenuator settings can cause a similar problem.

Instrument Preset. Instrument Preset turns off all functions then sets the following:

Sweep Mode: Start/Stop
  Start = minimum specified frequency
  Stop = maximum specified frequency
Sweep Type: Timed, minimum sweep time
Sweep Trigger: Internal
Vernier/Offset: set to 0 MHz
Markers: all values set to center of frequency span, all off
Modulation/Blanking: Display Blanking on
Frequency Step Size: set to default value (10% of span)
Status Bytes: cleared

83500 Series Plug-ins:
Power Level: maximum specified power (switch selectable to minimum power)
Power Sweep/Slope: set to 0 dB
RF/CW Filter: on/enabled
FM Sensitivity: determined by internal switch
Power Step Size: set to default value (1 dB)
Crystal Markers: 50 MHz, off

Instrument Preset does not affect Storage Registers, HP-IB address, or Service Request Mask value.

OUTPUT DATA

The 8350A has several output modes that allow the user to learn and interrogate the present instrument state. The following output modes are available:

- Learn String
- Micro Learn String
- Mode String
- Interrogated Function
- Active Function
- Status

The program codes and syntax to enable each function are described in the Input Data section. The Learn String, Micro Learn String, Mode String, and Status functions send a Data message consisting

Table 1. Input Programming Codes (1 of 4)

MODE	FUNCTION	PROGRAM CODE			NUMERIC VALUE		
		PREFIX ACTIVATE	NUMERIC FORMAT	SUFFIX	SCALE FACTOR	RANGE	RESOLUTION
SWEEP LIMITS/MODE							
Start/Stop Sweep	START	FA	1,2,3,4	GZ	$\times 10^9$Hz	Plug-in Frequency Limits	Approximately 0.03% of Plug-in Bandwidth
	STOP	FB					
Center Frequency /ΔF Sweep	CF	CF		MZ	$\times 10^6$Hz		
	ΔF	DF					
CW Frequency	CW	CW		KZ	$\times 10^3$Hz		
	SWEPT CW	SHCW					
Frequency Offset	OFFSET	SHVR					
Frequency Vernier	VERNIER	VR		HZ	×1 Hz	±0.05% of BW	0.0004% of BW
FREQUENCY MARKERS							
Turn On and Set Marker Frequency	MARKER 1	M1	1,2,3,4	GZ	$\times 10^9$Hz	Plug-in Frequency Limits	Approximately 0.4% of present ΔF
	MARKER 2	M2		MZ	$\times 10^6$Hz		
	MARKER 3	M3		KZ	$\times 10^3$Hz		
	MARKER 4	M4					
	MARKER 5	M5		HZ	×1 Hz		
Turn Off A Frequency Marker	M1 OFF	M1		MØ			
	M2 OFF	M2					
	M3 OFF	M3					
	M4 OFF	M4					
	M5 OFF	M5					
Turn Off All Markers	ALL OFF	SHMØ					
Turn On and Set Mkr Δ	MKRΔ, Marker "m", Marker "n"	SHM1	Mm Mn			where: m, n:1–5	
Turn Off Mkr Δ	MKRΔ OFF	MØ					
Active Marker to Center Frequency	MKR→ CF	MC					
Marker 1–2 Sweep	MARKER SWEEP ON	MP1					
	MARKER SWEEP OFF	MPØ					
Marker 1 to Start Marker 2 to Stop	M1→ST M2→SP	SHMP					
SWEEP TRIGGER TYPE							
Sweep Trigger Mode	INTERNAL	T1					
	LINE	T2					
	EXTERNAL	T3					
	SINGLE	T4					

Table 1. Input Programming Codes (2 of 4)

MODE	FUNCTION	PROGRAM CODE			NUMERIC VALUE		
		PREFIX ACTIVATE	NUMERIC FORMAT	SUFFIX	SCALE FACTOR	RANGE	RESOLUTION
SWEEP TRIGGER TYPE (Cont'd)							
Sweep Type	EXTERNAL SWEEP	SX					
	MANUAL SWEEP FREQUENCY	SM	1,2,3,4	GZ	$\times 10^9$Hz	Present Start/ Stop Frequency	0.1% of Present ΔF
				MZ	$\times 10^6$Hz		
				KZ	$\times 10^3$Hz		
				HZ	×1 Hz		
	SWEEP TIME	ST	1,2,3,4	SC	×1 sec.	See Plug-in Typically .01 to 100 sec.	0.001 sec.
				MS	$\times 10^{-3}$ sec.		
MODULATION/BLANKING							
Amplitude Frequency Markers	AMPTD MKR ON	AK1					
	AMPTD MKR OFF	AKØ					
Display Blanking	DISP BLANK ON	DP1					
	DISP BLANK OFF	DPØ					
RF Blanking	RF BLANK ON	RP1					
	RF BLANK OFF	RPØ					
Square Wave Modulation	⊓ MOD ON	MD1					
	⊓ MOD OFF	MDØ					
STEP FUNCTIONS							
Setting Frequency Step Size	FREQUENCY STEP SIZE	SF	1,2,3,4	GZ	$\times 10^9$Hz	Ø to 100% of Plug-in BW	Approximately 0.03% of Plug-in Bandwidth
				MZ	$\times 10^6$Hz		
				KZ	$\times 10^3$Hz		
				HZ	×1 Hz		
Setting Power Step Size*	POWER STEP SIZE	SP	1,2,3,4	DM	×1 dB	Ø to 15 dB	0.02 dB
Resetting Step Sizes To Default Values**	DEFAULT STEP SIZES	SHSS					
Increment Active Parameter	STEP UP ◆	UP					
Decrement Active Parameter	STEP DOWN ◆	DN					
INSTRUMENT STATE							
Instrument Preset	INSTR. PRESET	IP					
Saving An Instrument State	SAVE n	SV	4		×1	Registers 1 through 9	
Recalling An Instrument State	RECALL n	RC					
Alternate Sweep Mode	ALT n ON	AL1	4		×1	Registers 1 through 9	
	ALT n OFF	ALØ					
Undergo Self Test	SELF TEST #nn	SH	3		×1	00–99	

*These codes/functions do not apply to 86200 Series Plug-ins. **Both frequency and power step size.

Table 1. Input Programming Codes (3 of 4)

MODE	FUNCTION	PROGRAM CODE			NUMERIC VALUE		
		PREFIX ACTIVATE	NUMERIC FORMAT	SUFFIX	SCALE FACTOR	RANGE	RESOLUTION
SPECIAL HP-IB FUNCTIONS							
Status Bytes and Service Requests	OUTPUT STATUS	OS					
	SERVICE REQUEST MASK	RM	6			1 byte	
Full Learn String	OUTPUT LEARN STRING	OL					
	INPUT LEARN STRING	IL	5			90 bytes	
Micro Learn String***	OUTPUT MICRO LEARN STRING	OX					
	INPUT MICRO LEARN STRING†	IX	5			8 bytes	
Active Mode String	OUTPUT MODE STRING	OM	5			25 bytes	
Output Active Parameter Value	OUTPUT ACTIVE VALUE	OA					
Output Interrogated Parameter Value	OUTPUT INTERROGATED VALUE	OP	Interrogated Parameter Code				
Numeric Display Update	DISPLAY UPDATE ON	DU1					
	DISPLAY UPDATE OFF	DUØ					
Single Sweep Start/Stop	RESET SWEEP	RS					
	TAKE SWEEP	TS					
Network Analyzer Trigger (8410B)	NETWORK TRIGGER	NT					
PLUG-IN POWER LEVEL*							
Set Output Power Level	POWER LEVEL	PL	1,2,3,4	DM	×1 dBm	Plug-in Power Limits	0.02 dBm
Power Sweep Mode	POWER SWEEP ON	PS1	1,2,3,4	DM	×1 dB/Swp	Ø to 25.5 dB	0.02 dB
	POWER SWEEP OFF	PSØ					
Power Slope Mode	SLOPE ON	SL1	1,2,3,4	DM	× dB/GHz	Ø to 5 dB	0.01 dB
	SLOPE OFF	SLØ					
PLUG-IN ALC/SIGNAL CONTROL*							
ALC Leveling Modes	INTERNAL	A1					
	EXTERNAL (CRYSTAL)	A2					
	EXTERNAL POWER METER	A3					
RF Power	RF ON	RF 1					
	RF OFF	RF Ø					
CW Filter	FILTER ON	FI 1					
	FILTER OFF	FI Ø					

*These codes/functions do not apply to 86200 Series Plug-ins. ***Must be in CW mode, CW Filter off. †Exit this mode via "MØ " code.

Table 1. Input Programming Codes (4 of 4)

MODE	FUNCTION	PROGRAM CODE			NUMERIC VALUE		
		PREFIX ACTIVATE	NUMERIC FORMAT	SUFFIX	SCALE FACTOR	RANGE	RESOLUTION
PLUG-IN CRYSTAL MARKERS*							
Crystal Marker Frequency	1 MHz	C1					
	10 MHz	C2					
	50 MHz	C3					
	EXTERNAL INPUT	C4					
Amplitude Markers	AMPL MKR ON	CA 1					
	AMPL MKR OFF	CA Ø					
Intensity Markers	INTEN MKR ON	CI 1					
	INTEN MKR OFF	CI Ø					
PLUG-IN SPECIAL FUNCTIONS*							
FM Input Sensitivity	−20 MHz/V	F1					
	−6 MHz/V	F2					
Peak Output Power ‡	PEAK	SHPL					

*These codes/functions do not apply to 86200 Series Plug-ins. ‡83590 Series Plug-in Only.

of a string of 8-bit binary bytes terminated using the bus EOI line true with the last byte. The Interrogate and Active functions send a Data message consisting of a 14 character ASCII string representing the numeric value in exponential form terminated with a Carriage Return/Line Feed (CR/LF).

Binary Syntax: [b***b] [EOI]

Numeric Syntax: [±d.dddddE±dd] [CR] [LF]

Where the character 'b' indicates an 8-bit binary byte and 'd' indicates a decimal digit (0 through 9). Note that the binary output format could have bytes that may be misinterpreted as Carriage Returns and/or Line Feeds so the user should defeat the ASCII CR/LF as valid character string terminators and rely on the byte count.

Learn String:

Selected with the "OL" program code, the 8350A outputs a Learn String of 90 bytes in length. This binary data string completely describes the present instrument state (does not include the Storage Registers) of the 8350A and 83500 Series Plug-in. The information is packed and encoded for minimal storage requirements thereby making data analysis difficult. When stored in an ASCII character data string, the Learn String can later be input to the 8350A to restore that instrument state (See Input Data for Input Learn String information). The length of the Learn String is fixed, independent of the functions selected and the plug-in used.

Format: 90 [8 bit bytes] [EOI]

Micro Learn String:

Selected with the "OX" program code, the 8350A outputs a Micro Learn String of 8 bytes in length. This binary data string completely describes the present CW frequency, Vernier, Sweep Output voltage, and Power Level of the 8350A and 83500 Series Plug-in. The information is packed and encoded for minimal storage requirements thereby making data analysis difficult. When stored in an ASCII character data string, the Micro Learn String can later be input to the 8350A to restore that instrument state for rapid frequency programming (See Input Data for Input Micro Learn String information). Note the 8350A must be in CW mode and the CW Filter should be off when using this function. The length of the Micro Learn String is fixed, independent of the functions selected and the plug-in used.

Format: 8 [8 bit bytes] [EOI]

Mode String:

Selected with the "OM" program code, the 8350A outputs a Mode String of 25 bytes in length. This binary data string describes all presently active functions of the 8350A and 83500 Series Plug-in. The information is not packed thereby making data analysis simpler. The information passed includes only the active functions with no numeric values included. Use the Active or Interrogate Function if numeric values are desired. The length of the Mode String is fixed, independent of the functions selected and the plug-in used.

Format: 25 [8 bit bytes] [EOI]

Interrogate Function:

Selected with the "OP" program code and the program code for the function to be interrogated, the 8350A will output the present numeric value of the selected function. The units of the output data are Hz, dBm, dB, or sec., implied with the function selected.

Format: [±d.dddddE±dd] [CR] [LF]

Active Function:

Selected with the "OA" program code, the 8350A will output the present numeric value of the presently active function (ie. enabled for modification from the keyboard or step keys). The units of the output data are Hz, dBm, dB, or sec., implied with the function selected.

Format: [±d.dddddE±dd] [CR] [LF]

Status:

Selected with the "OS" program code, the 8350A will output 2 sequential bytes, 8 bits wide, giving the present instrument status. The first status byte is equivalent to the Status Byte of the Serial Poll, the second status byte is the Extended Status Byte which provides additional information. See Table 2 for a description of each Status Byte. Status Byte values are cleared upon execution of a Serial Poll (Status Byte message), Device Clear message, and/or the Instrument Preset function.

TRIGGER

The 8350A responds to the Group Execute Trigger (GET) command to the HP-IB bus select code and a Selective Device Trigger to the 8350A HP-IB address. The effect of the GET command is to trigger the sweep if presently in the Single Sweep Trigger mode only, otherwise no action is taken. The response is as if a Data message consisting of the Single Sweep Trigger (T4) program code were transmitted.

CLEAR

The 8350A responds to both Device Clear (DCL) and Selective Device Clear (SDC) messages by clearing the Status Byte and the Extended Status Byte.

REMOTE/LOCAL CHANGES

The Local to Remote change is programmed by the Selective Device Remote Enable message (REN and 8350A address). The 8350A instrument state is unchanged with all future changes affected by program codes only. Note that all front panel functions are disabled in Remote except the LCL key.

The Remote to Local change is programmed by the Go To Local (GTL) command or by setting the REN line false (high). The 8350A instrument state is unchanged with all future changes affected by the front panel controls. The 8350A can also be set to Local by pressing the LCL key. Note that the 8350A does not respond to the LCL key if the Local Lockout command has been executed. This command disables all front panel functions including the LCL key.

SERVICE REQUEST

The 8350A can initiate a Service Request (SRQ) whenever one of the following conditions exist:

- Error in syntax
- Parameter value modified to default value
- Hardware failure
- End of sweep

Further information can be obtained by conducting a Serial Poll or by executing the Output Status command, both of which access Status Byte information. The SRQ is cleared only by executing a Serial Poll. To select an SRQ for a particular set of circumstances, the Request Mask function can be used to select which of the bits in the first Status Byte can cause an SRQ. The mask value is determined by summing the decimal values of each selected function/condition that is desired. The default Request Mask at power on is '00000000' or decimal 0. This mask value is reset to the default value only at power on.

STATUS BYTE

The 8350A responds to a Serial Poll by sending its status byte as indicated in Table 2. A second status byte is available but must be accessed via the Output Status command. When Bit 6 (Request Service) of the Status Byte is true (one), an SRQ has occurred. See Service Request for the conditions causing a Service Request. Bit 4 indicates whether a change has occurred in the Extended Status Byte. If Bit 4 is true, then the second status byte should be accessed via the Output Status function to determine the cause of the status change. All other bits indicate the present status of the noted function. The bits are true (one) if and only if the associated function/condition is true.

STATUS BIT

The 8350A does not respond to a Parallel Poll.

PASS CONTROL

The 8350A does not have the ability to take or pass control.

ABORT

The 8350A responds to the Abort message (Interface Clear — IFC true) by stopping all Listener or Talker functions.

ADDRESS ASSIGNMENT INFORMATION

The 8350A has a primary address that is determined by an internal storage register. The register is initialized upon power turn on by reading the address bits A5 thru A1 from switches located on the 8350A A8 HP-IB Assembly. Note that these switches are factory preset to decimal 19. The 8350A HP-IB address can be dynamically changed from the front panel in local mode by executing the "Set HP-IB Address" command (Shift Local). See the 8350A Operating and Service Manual for further information.

Table 2. 8350A Status Byte Descriptions

STATUS BYTE (#1)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	N/A	REQUEST SERVICE (RQS)	SRQ on Syntax Error	SRQ on End of Sweep	N/A	SRQ on Change in Extended Status Byte	N/A	SRQ on Numeric Parameter Altered to Default Value

EXTENDED STATUS BYTE (#2)								
BIT #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DECIMAL VALUE	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
FUNCTION	Airflow Failure	*RF Unleveled	Power Failure/on	N/A	N/A	N/A	N/A	Self Test Failed

*Bit/Functions not usable with 86200 Series Plug-ins and 11869A Adapter.

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5952-9309

Printed in U.S.A.

SECTION IV
PERFORMANCE TESTS

4-1. INTRODUCTION

4-2. The procedures in this section test the electrical performance of the 8350A Sweep Oscillator/83500 series RF Plug-in combination with the specifications of the Plug-in used as the performance standards. These specifications may be found in Section I of the manual for the Plug-in being tested. None of the tests require access to the interior of the 8350A Sweep Oscillator.

4-3. EQUIPMENT REQUIRED

4-4. Equipment required to test any Plug-in with an output frequency up to 12.4 GHz is listed in the Recommended Test Equipment table in Section I of this manual. The RF Plug-in manual Recommended Test Equipment table lists only the test equipment for that particular plug-in. Any equipment that satisfies the critical specifications given in the tables may be substituted for the recommended model.

4-5. OPERATION VERIFICATION

4-6. Operation Verification consists of performing the tests listed on paragraph 4-13 steps 1 to 13 and paragraph 4-14 steps 1 to 15. Operation Verification of the HP-IB functions may be done by executing the program listed on Table 4-1 HP-IB Operation Verification Program using the 9825A/B Desktop Computer. These tests provide reasonable assurance that the sweep oscillator and plug-in are functioning properly and should meet the needs of an incoming inspection (80% verification).

4-7. TEST RECORD

4-8. Results of the performance test may be tabulated on the Test Record Card at the end of Section IV in the Plug-in manual. The Test Record Card lists all of the tested specifications and their acceptable limits.

4-9. TEST SEQUENCE

4-10. Table 4-2 lists the sequence of the performance tests and the major test equipment required for each test. The performance tests should be performed in the order listed. The performance test for crystal markers and other unique plug-in functions are in the plug-in manual.

4-11. CALIBRATION CYCLE

4-12. The performance tests in this section should be performed in intervals of one year or less for the 8350A. For plug-in calibration cycle see respective plug-in manual.

NOTE

Plug-ins with output frequencies greater than 12.4 GHz will require use of the Performance Test in the plug-in manual.

```
0: "HP-IB Operation Verification Test. 18 Sept 80.":
1: "Change Address in Line 3 If Needed.":
2: dim A$[3],B$[3]
3: dev "8350",719
4: "Check REM Line.":
5: rem "8350"
6: dsp "Check REM Light. [CONT] If ON.";stp
7: "Check Handshake Line":
8: on err "HP-IB"
9: time 3000
10: wrt "8350","IP OPST"
11: red "8350",A
12: jmp 1
13: "HP-IB":dsp "Handshake or ATN Line Error.";stp
14: "Check Programmability and Read Output":
15: wrt "8350","ST 100 MS"
16: wrt "8350","OPST";red "8350",A
17: if A=.1;jmp 1
18: "READ":dsp "Programmability or Read Error";stp
19: "Check Data Lines.":
20: on err "DATA"
21: wrt "8350","RM"&char(170)
22: wrt "8350","SH 00 M1 0114 M3"
23: red "8350",A$;wait 20
24: wrt "8350","M0 RM"&char(85)
25: wrt "8350","SH 00 M1 0114 M3"
26: red "8350",B$;wait 20
27: if A$[1,2]="AA" and B$[1,2]="55";jmp 2
28: dsp "Data Bus Error.";stp
29: "DATA":ern→A;erl→B;rom→C;dsp A,B,C
30: "Check Interrupt Request Capability.":
31: wrt "8350","M0 RM"&char(96)
32: oni 7,"SYN"
33: eir 7
34: wrt "8350","XYZ"
35: wait 500
36: dsp "SRQ Line Error.";stp
37: "SYN":jmp 0
38: wrt "8350","IP"
39: lcl "8350"
40: dsp "End of Test. HP-IB is Verified.";stp
41: end
*30275
```

Table 4-2. Performance Test

Paragraph	Title	Major Equipment
4-13	Frequency Range and CW Accuracy Frequency Range CW accuracy Swept Frequency Accuracy Marker accuracy	Frequency Counter
4-14	Output Amplitude Power Meter Leveling Maximum Leveled Power Power variations Power level accuracy Power Sweep Slope Compensation	Power Meter Frequency Response Test Set
4-15	Frequency Stability With Line Voltage WithPower Level With Time (10 minutes) With Load Impedance	Frequency Counter Directional Coupler Adjustable Short Adjustable AC Line Transformer
4-16	Residual FM At 10 kHz bandwidth	Spectrum Analyzer
4-17	Spurious Signals Harmonic Non-Harmonic	Spectrum Analyzer
4-18	Output VSWR	Directional Coupler Detector Oscillator Air Line
4-19	Residual AM	RMS Voltmeter
4-20	External FM Deviation	Spectrum Analyzer Function Generator Frequency Counter Oscilloscope Delay Line Discriminator Power Splitter
4-21	FM Response	Oscillascope Function Generator Delay Line Discriminator
4-22	AM ON/OFF Ratio and Square Wave Symmetry	Spectrum Analyzer
4-23	Attenuator Accuracy (Option 002)	Spectrum Analyzer Step Attenuator

NOTE

Allow 1 hour warmup time

4-13. FREQUENCY RANGE AND ACCURACY TEST

SPECIFICATION:

See Performance Test Record Card in section IV of the plug-in manual for frequency range and accuracy specifications.

DESCRIPTION:

A frequency counter is used to check frequency range and accuracy in the CW mode. The frequency counter is also used to check swept frequency accuracy and markers in the START/STOP mode.

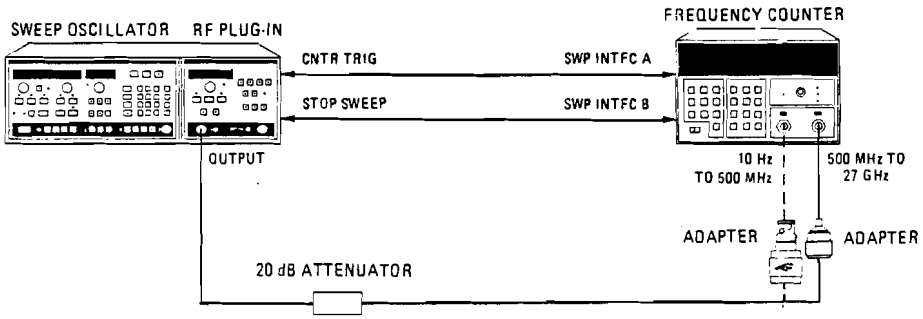


Figure 4-1. Frequency Range and CW Accuracy Test Setup

EQUIPMENT:

Plug-in	HP 83500 series
Frequency Counter	HP 5343A*
20-dB Attenuator	HP 8491B, Option 020
Adapter	Type-N, male to APC 3.5, female
Adapter	Type-N, male to BNC male

*If another counter is used the swept frequency measurements will require the use of additional test equipment. This equipment is listed in the Alternate Swept Frequency Test at the end of this paragraph.

PROCEDURE:

NOTE

Plug-ins having a FREQ CAL adjustment on the front panel require performing the FREQ CAL procedure in section 3 of the plug-in manual prior to performance of this test.

1. Connect equipment as shown in Figure 4-1.

4-13. FREQUENCY RANGE AND ACCURACY TEST (Cont'd)

2. Set controls as follows:

   Frequency Counter

   LINE ..... ON
   SAMPLE RATE ..... minimum (full CCW)
   Range connector ..... 500 MHz to 27 GHz except as noted
   Impedance Switch 50Ω
   ACQ TIME (rear panel) ..... FAST

3. Press 8350A INSTR PRESET key. Note sweep oscillator display of START and STOP frequencies equals the frequency range on the test card.

Frequency Range

4. Press 8350A CW key and enter the previously noted start frequency (If start frequency is below 500 MHz use the 10 Hz to 500 MHz counter input connector). If the frequency observed on frequency counter is greater than the start frequency rotate 8350A CW control counterclockwise until frequency on counter is at or below the specified start frequency. Enter the frequency counter reading on the test card step 4.

5. Enter the previously noted stop frequency. If frequency observed on frequency counter is lower than the specified high frequency rotate the 8350A CW control clockwise until the frequency counter reading is higher or equals the specified high frequency. Enter the frequency counter reading on the test card step 5.

Frequency Accuracy

6. Check frequency accuracy by setting the CW frequency on the 8350A and recording the frequency observed on the frequency counter at the three points on each band as shown on the test card step 6. Follow the sequence of frequencies on the test card to avoid band crossover problems.

Swept Frequency Accuracy

7. Press frequency counter RESET, SWP M (Light on), Blue Key, 1KHz. Press 8350A INSTR PRESET and set sweep time to 105 msec.

8. Press 8350A START, SHIFT, then M2. Check and record the frequency counter reading on the test card step 8.

9. Press 8350A STOP, SHIFT, then M2. Check and record the frequency counter reading on the test card step 9.

10. For multiband plug-ins repeat steps 8, and 9 using the start and stop frequencies on test card step 10.

4-13. FREQUENCY RANGE AND ACCURACY TEST (Cont'd)

Frequency Marker Accuracy

11. Press 8350A INSTR PRESET and set sweep time to 105 msec.

12. Set the markers to the frequencies listed and record the frequency counter readings on the test card step 12.

13. For multiband plug-ins set the start and stop frequencies on the test card step 13 and repeat the previous step with the markers set as shown on the test card step 13.

Alternate Swept Frequency and Marker Accuracy Test

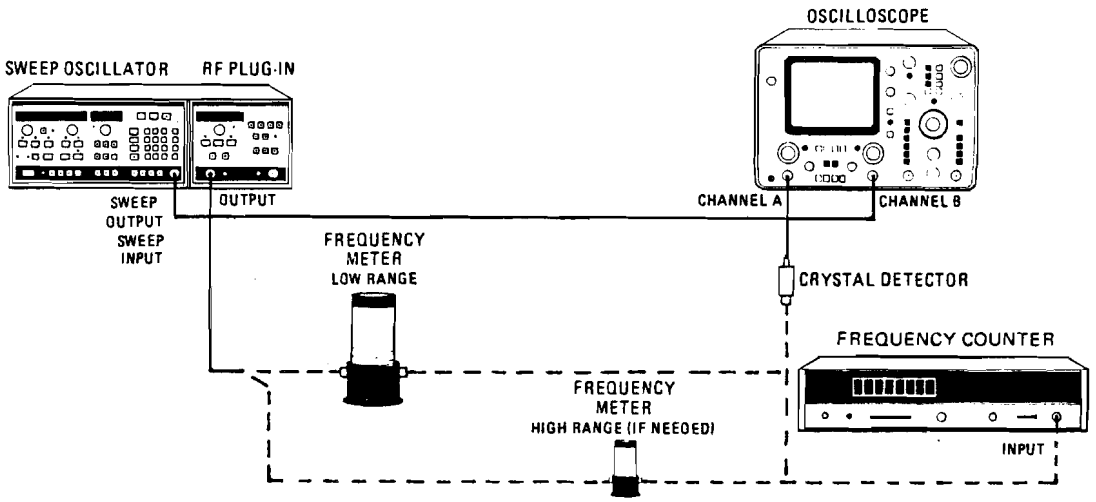


Figure 4-2. Alternate Swept Frequency Accuracy Test Setup

EQUIPMENT:

Plug-in	HP83500 series
Crystal Detector	HP 8470B
Frequency Counter	HP 5340A
Oscilloscope	Any general purpose oscilloscope such as HP 1222A or 1740A
Frequency Meters as needed to cover frequency range of plug-in)	
0.96 to 4.2 GHz	HP 536A
3.7 to 12.4 GHz	HP537A

NOTE

The low frequency limit of the Frequency Meters is 0.96 GHz which limits the RF Plug-ins with output frequencies lower than 1 GHz to a swept frequency check of 1.00 GHz or using the 5343A.

4-13. FREQUENCY RANGE AND ACCURACY TEST (Cont'd)

7A. Connect equipment as shown in Figure 4-2. Use Frequency Meter/s necessary to cover the high and low frequency range of the installed plug-in. Press 8350A INSTR PRESET key then set sweep time to 105 msec. If start frequency displayed is lower than 1 GHz the start frequency must be changed to 1 GHZ. Set oscilloscope to A vs. B and MAG X10 mode.

NOTE

To use the frequency meters for swept and marker frequency accuracy first calibrate the frequency meters. Calibrate meters by using the frequency counter to set the 8350A swept CW frequency to each frequency listed on the test card steps 8, 9, 10, 12, and 13 then connect the oscilloscope and adjust the frequency meter to dip trace. Record difference between actual and frequency meter reading.

8A. Adjust frequency meter to move notch on oscilloscope to start frequency. Check and record corrected Frequency Meter reading on test card step 8A.

9A. Adjust frequency meter to move notch on oscilloscope to Stop Frequency. Check and record corrected Frequency Meter reading on test card Step 9.

10A. For multiband plug-ins repeat steps 8 and 9 using the start and stop frequencies on test card step 10A.

11A. Press 8350A INSTR PRESET and set sweep time to 105 msec.

12A. Set the markers to the frequencies listed on the test card. Adjust the frequency meter notch over each marker and record the corrected frequency meter reading on the test card step 12.

13A. For multiband plug-ins set the start and stop frequencies on the test card step 13 and repeat the previous step with the markers set as shown on the test card step 13.

4-14. OUTPUT AMPLITUDE TEST

SPECIFICATION:

See Performance Test Record Card in section IV of the appropriate plug-in manual for output amplitude specifications.

DESCRIPTION:

A Power Meter is used to check maximum power and power variations in power meter leveling. A Swept Amplitude Analyzer is used to check power variations at maximum leveled power internally leveled, power level accuracy, and power sweep.

4-14. OUTPUT AMPLITUDE TEST (Cont'd)

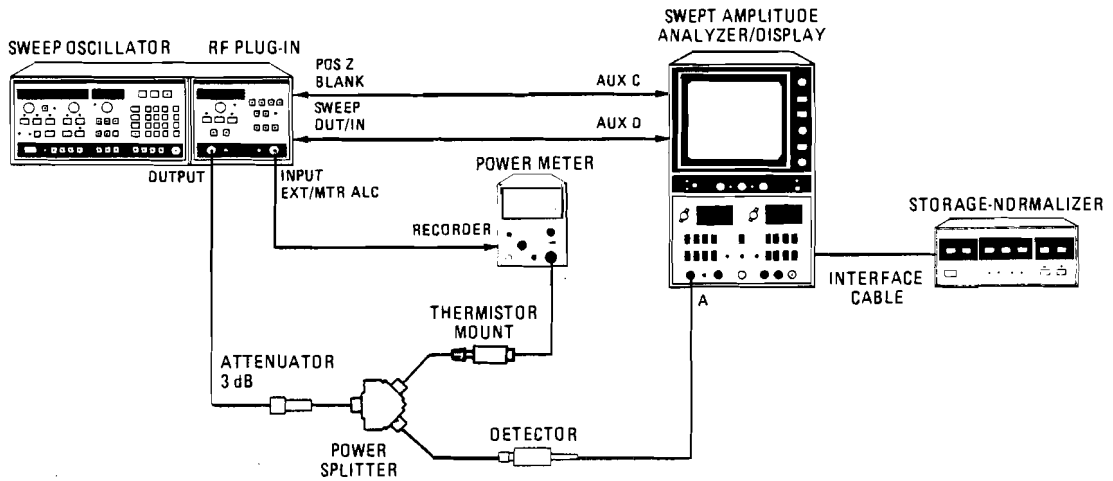


Figure 4-3. Output Amplitude Test Setup

EQUIPMENT:

NOTE

If a Storage-Normalizer 8750A is not available use a grease pencil to record the detector response on the CRT.

Plug-in	HP 83500 series
Power Meter	HP 432A
Thermistor Mount	HP 8478B
Oscilloscope	HP 182T
Swept Amplitude Analyzer	HP 8755C
Detector	HP 11664A
Power Splitter	HP 11667A
3 dB Attenuator	HP 8491B Opt 003
Storage-Normalizer	HP 8750A

PROCEDURE:

NOTE

If oscilloscope will not synchronize on CRT it may be due to the ⌐¬ MOD frequency being set to 1 kHz. To change the frequency to 27.8 kHz refer to section VIII of this manual.

4-14. OUTPUT AMPLITUDE TEST (Cont'd)

1. Connect equipment as shown in Figure 4-3. Turn on Storage-Normalizer and Swept Amplitude Analyzer. Adjust GAIN and REFERENCE POSITION controls as per the Amplitude Analyzer manual. Adjust Storage-Normalizer per its operation section to match the Swept Amplitude Analyzer using the Network Analyzer card.

2. Press INSTR PRESET and SHIFT CW then engage ⎍ MOD on the 8350A. Set plug-in POWER LEVEL display to specified maximum leveled power and ALC mode to MTR.

3. Adjust power meter CALIBRATION FACTOR to the value on the thermistor mount corresponding to the frequency displayed on the 8350A. Set power meter RANGE switch and adjust plug-in EXT/MTR ALC CAL for a power meter reading 12 dB below plug-in displayed power. The 12 dB is due to the following losses: Power Splitter=6 dB, Attenuator=3 dB, and ⎍ MOD=3 dB.

4. Press SELECT CH 1, and BYPASS on storage-normalizer.

5. Set amplitude analyzer controls as follows:

VIDEO FILTER ..... OFF

CHANNEL 1
- DISPLAY ..... A
- dB/DIV 10
- VERNIER ..... ON
- OFFSET ..... −00

CHANNEL 2
- DISPLAY ..... All buttons out

6. Adjust CH 1 REFERENCE LEVEL VERNIER to center trace. Change dB/DIV to 0.25 and center trace again using REFERENCE VERNIER.

7. Set 8350A controls to:

SWEEP TIME ..... 100 sec
SWEEP TRIGGER ..... SINGLE
Sweep Mode ..... START/STOP(full plug-in range)

8. Engage INPUT and STORE INPUT keys on storage-normalizer.

Power Meter Leveling

NOTE

If plug-in is multiband allow a small discontinuity (typically <0.25 dB) at the band switching point/s listed on the test card step 9.

9. Press 8350A SWEEP TRIGGER SINGLE key to start sweep while observing that the SWP light goes on. Observe and record power meter peak-to-peak meter fluctuations on test record card step 9.

4-14. OUTPUT AMPLITUDE TEST (Cont'd)

10. To store the observed trace in the 8750A (STORE light off) a trigger signal may be needed. To get a trigger signal press the 8350A SINGLE key once and wait until the 8750A store light goes off. Then press the SINGLE key again to stop the sweep.

NOTE

System irregularties can be checked by exchanging the thermistor and detector and sweeping again with the storage-normalizer in INPUT-MEM.

11. Set the following controls:

Plug-in
ALC MODE ..... INT

8350A
SWEEP TIME ..... 10 msec
SWEEP TRIGGER ..... INT
SWEEP MODE ..... SHIFT CW

Storage-Normalizer
DISPLAY ..... INPUT-MEM

Plug-in
Connect power meter to plug-in OUTPUT, turn off LFTMOD. Adjust POWER LEVEL control until power meter reads the specified maximum leveled power. Reconnect attenuator and power splitter to plug-in and turn on LFTMOD.

Amplitude Analyzer
Adjust VERNIER until trace (mid-point in frequency sweep) lies on the center line. This calibrates center line of Amplitude Analyzer for specified maximum leveled absolute power.

Power Level Accuracy

12. Press the POWER LEVEL key on the plug-in then via the 8350A Data Entry keys enter the specified maximum leveled output power. Press the START key on the 8350A. Check and record that the amplitude analyzer peak-to-peak power variations are within the limits shown on the test record card step 12.

Calibrated Range

13. Press the POWER LEVEL key on the plug-in then press the 8350A ◂ key to reduce plug-in power by 1 dB. Reduce amplitude analyzer REFERENCE LEVEL switch setting by 1 dB. Check and record that peak-to-peak power variations are within the limits shown on test record card step 13. Repeat this step for the power levels on the test card to verify power level accuracy over the entire range.

4-14. OUTPUT AMPLITUDE TEST (Cont'd)

14. Press the POWER LEVEL key on the plug-in then via the 8350A Data Entry keyboard enter the maximum specified output power. Switch the REFERENCE LEVEL switch to −00 dBm.

Maximum Internally Leveled Output Power and Variation

15. Use Power Level control to adjust power level such that the minimum power point across the sweep lies exactly on the center line (See example on Figure 4-4). The minimum power on the full sweep is then at the specified maximum power. Check and record the peak power across the whole band on the test record card step 15.

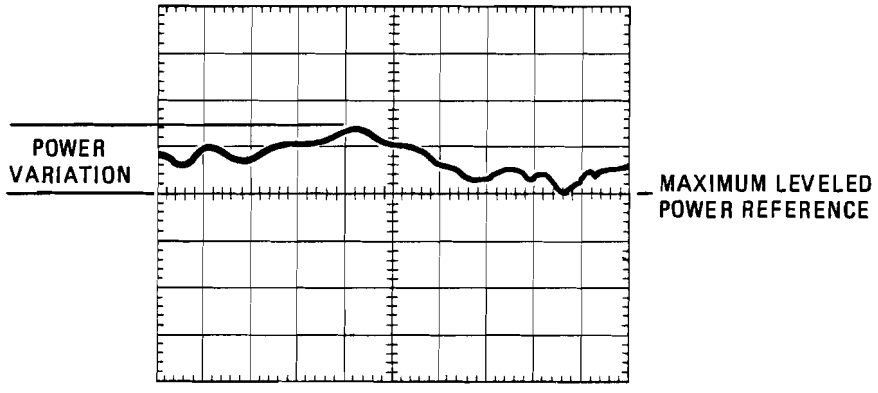


Figure 4-4. Typical Maximum Leveled Power and Variation

16. Press BYPASS on the storage-normalizer. Engage the 10 dB/DIV button on the amplitude analyzer.

Power Sweep Check

17. Press START on 8350A. Press POWER LEVEL on plug-in and adjust power control to the value shown on the performance test card step 17. Engage POWER SWEEP and adjust POWER control clockwise until the UNLEVELED light turns on. Turn POWER control counterclockwise until the unleveled light remains off. Check the POWER SWEEP display and amplitude analyzer display to verify the amplitude change from beginning to end of sweep is at least the level specified on the test card step 17.

4-15. FREQUENCY STABILITY TEST

SPECIFICATION:

See Performance Test Record Card in section IV of the plug-in manual used for Frequency Stability specifications.

DESCRIPTION:

A frequency counter is used to check frequency change due to line voltage changes, time (10 minutes), output power level changes, and load impedence changes.

4-15. FREQUENCY STABILITY TEST (Cont'd)

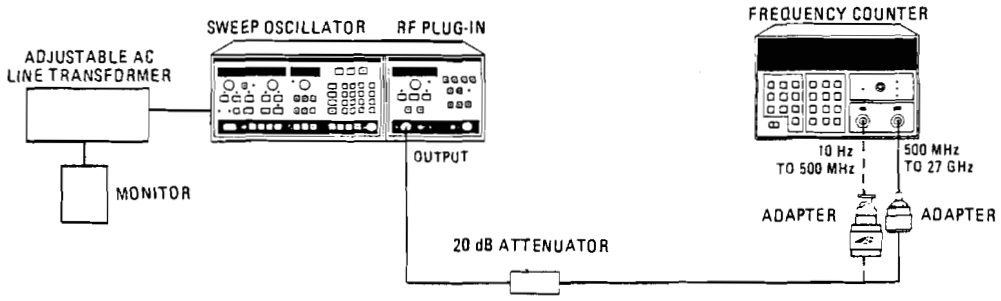


Figure 4-5. Frequency Change with Line Voltage Change

EQUIPMENT:

NOTE

More than one model number is listed for some test equipment. Use only the equipment needed to cover the line voltage used.

RF Plug-in ..... HP 83500 series
Frequency Counter ..... HP 5343A
20 dB Attenuator ..... HP 8491B Option 020
Adapter ..... Type-N, male to APC 3.5, female

Directional Coupler ..... HP 778D

Adjustable AC Line Transformer and monitor (Select for line voltage needed)
- 100-120 volt ..... General Radio W5MTB
- 120 V Monitor ..... RCA WV 120B
- 220-240 volt ..... General Radio W10HM73
- 240V Monitor ..... RCA WV 503A

3 dB Attenuator ..... HP 8491B Opt. 003
Adjustable Short ..... Maury Microwave 1953–2

PROCEDURE:

Frequency Change with Line Voltage Change

1. Connect equipment as shown in Figure 4-5 and set 8350A LINE switch to ON.

4-15. FREQUENCY STABILITY TEST (Cont'd)

2. Set adjustable line transformer using suitable monitor to the line voltage set on the 8350A power module. Press the 8350A INSTR PRESET and CW key and enter the 8350A frequency shown on the test card (Frequency Stability Step 2).Rotate frequency counter SAMPLE RATE knob to HOLD, press SET, OFS MHZ, Blue Key, then rotate the Frequency Counter SAMPLE RATE knob counter-clockwise back to the normal position.

Table 4-3. High and Low Line Voltage Selection Table

Nominal Line Voltage	100V	115/120V	220V	240V
Low Line Voltage	90V	108V	198V	216V
High Line Voltage	105V	126V	231V	252V

3. Set adjustable line transformer to the low line voltage using suitable monitor which corresponds to the selected nominal voltage in Table 4-3. Check and record on the test record card step 3 the difference frequency displayed on counter.

4. Set adjustable line transformer using suitable monitor to the high line voltage using suitable monitor which corresponds to the selected nominal voltage. Check and record on the test record card step 4 the difference frequency displayed on counter.

Frequency Change with Time (10 minutes)

5. Set adjustable line transformer voltage to nominal. Set Plug-In RF power and CW frequency to that shown on test card step 5 (wait one minute for frequency counter and oscillator to settle).

6. Rotate the frequency counter SAMPLE RATE knob to HOLD, press SET, OFS MHZ, Blue Key, then rotate the Frequency Counter SAMPLE RATE knob counter-clockwise back to the normal position. The counter is now indicating frequency change with time.

7. Wait 10 minutes while observing frequency count for maximum frequency change and record this maximum change on the performance test record card step 7.

8. If the Plug-in is a multiband unit repeat steps 6 and 7 for the other frequencies shown on the test card.

Frequency Change With 10 dB Power Level Change

9. Set output power and CW frequency as indicated on test record card step 9.

4-15. FREQUENCY STABILITY TEST (Cont'd)

10. Rotate the frequency counter SAMPLE RATE knob to HOLD, press SET, OFFSET, Blue Key, then rotate the frequency counter SAMPLE RATE knob counter-clockwise back to the normal position. Reduce the output power to the level shown on the test card (−10 dB) and record the frequency change on the test card step 10.

11. If the Plug-in is a multiband unit repeat step 10 for the other frequencies shown on the test card step 11.

Frequency Change With 3:1 Load SWR

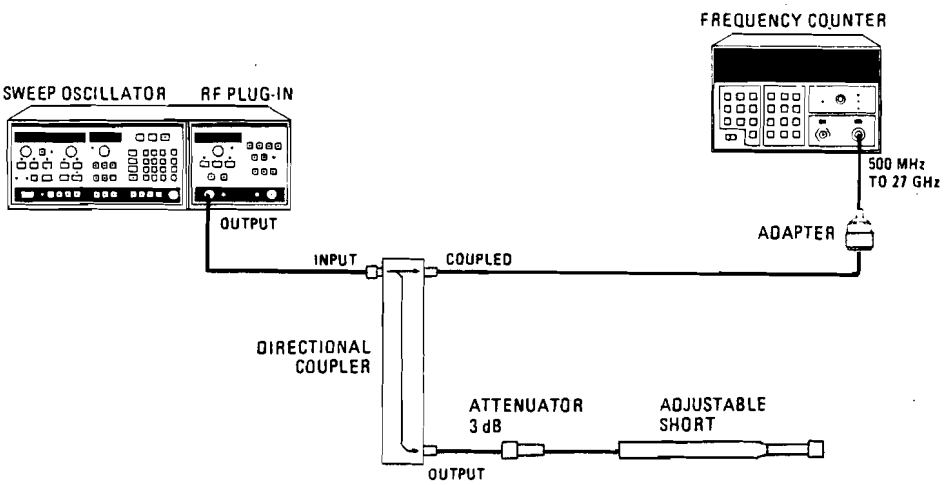


Figure 4-6. Frequency Change with 3:1 Load SWR Test Setup

12. Connect equipment as shown in Figure 4-6. Press the 8350A INSTR PRESET key then the CW key.

13. Enter the 8350A display frequency and power noted on the test card (step 13). On counter rotate the SAMPLE RATE knob clockwise to HOLD, press SET. OFS MHZ. Blue Key, then rotate the SAMPLE RATE knob counter-clockwise to the normal position on the Frequency Counter.

14. Adjust the adjustable short through its range while observing the frequency counter for the greatest plus and minus frequency change. Check and record the sum of the maximum plus and minus frequency change on the test card step 14.

15. If the Plug-in is a multiband unit the test should be repeated for the other band/s by repeating steps 13 and 14. for the other frequency/ies on the Plug-in test card. Record on test card step 15.

4-16. RESIDUAL FM TEST

SPECIFICATION:

See Performance Test Record Card in section IV of plug-in manual for residual FM specification.

DESCRIPTION:

RF output signal is displayed on a spectrum analyzer with the option of direct readings using the modulation analyzer. Without the modulation analyzer the residual FM is observed on the storage display by displaying five superimposed traces.

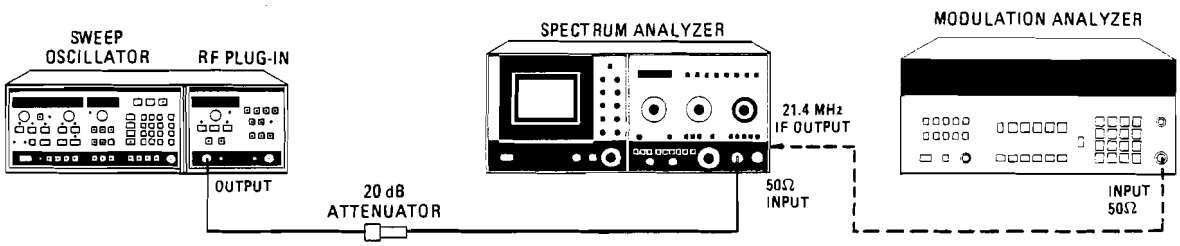


Figure 4-7. Residual FM Test Setup

EQUIPMENT:

NOTE

The modulation analyzer listed below is not required for the test. It is included to make the test convenient.

Sweep Oscillator	HP 8350A
Spectrum Analyzer	HP 8565A
Modulation Analyzer	HP 8901A
20 dB Attenuator	HP 8491B, Option 020

PROCEDURE:

1. Connect equipment as shown in Figure 4-7.
2. Press 8350A INSTR PRESET, CW. Enter frequency shown on test card step 2.

NOTE

To minimize drift allow 5 minutes before continuing with test.

4-16. RESIDUAL FM TEST (Cont'd)

3. Tune spectrum analyzer to CW frequency set for plug-in. Set spectrum analyzer resolution bandwidth to 10 kHz and frequency span per division to 10 kHz while keeping signal centered on CRT display. Auto stabilizer should be on.

4. Select spectrum analyzer linear (LIN) amplitude scale and adjust reference level controls for a full eight division vertical display. Set scan time per division to 20 msec.

5. Set spectrum analyzer sweep trigger to single sweep. Set persistance control fully clockwise and erase the trace. Push spectrum analyzer start/reset pushbutton five times within a two second interval and store resultant traces on CRT screen. Display should be similar to that shown in Figure 4-8. Note the peak-to-peak residual FM across the top of the trace and divide it by two to get the peak. Record the peak residual FM on the test card step 5.

6. If plug-in is a multiband unit repeat steps 3, 4, and 5 at the frequency/ies on the test card step 6.

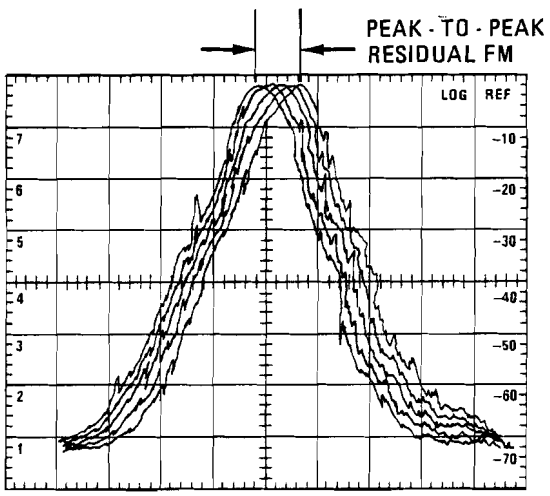


Figure 4-8. Residual FM Display on Spectrum Analyzer

With optional Modulation Analyzer

5A. Set spectrum analyzer to 1 MHz bandwidth, and 0 spanwidth. Adjust the spectrum analyzer fine frequency control for maximum amplitude. The spectrum analyzer is now being used as a down converter only. Set 8901A high pass filter to 50 Hz and low pass filter to 15 kHz. Press 8901A FM, AUTOMATIC OPERATION, PEAK +, and PEAK HOLD keys on Modulation Analyzer. Check and record the displayed Residual FM on the test card step 5.

6A. If plug-in is a multiband unit, repeat steps 3, 4, and 5A using the frequency/ies on the test card step 6.

4-17. SPURIOUS SIGNALS TEST

SPECIFICATION:

See Performance Test Record Card in section IV of plug-in manual for harmonic and non-harmonic spurious signals specifications.

DESCRIPTION:

RF output signal from sweep oscillator is displayed on a spectrum analyzer to verify that harmonic and non−harmonic spurious signals are at or below the specified level.

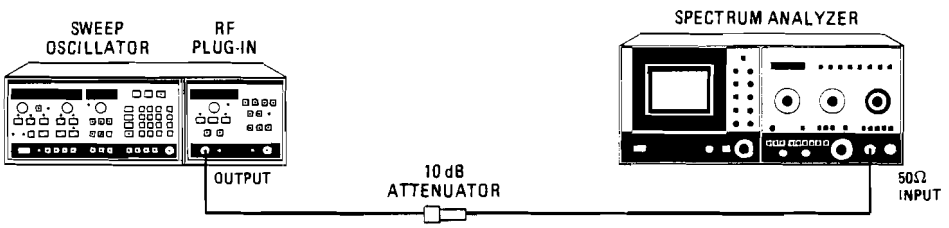


Figure 4-9. Spurious Signals Test Setup

EQUIPMENT:

RF Plug-in	HP 83500 series
Spectrum Analyzer	HP 8565A
10 dB Attenuator	HP 8491B, Option 010

PROCEDURE:

1. Connect equipment as shown in Figure 4-9.

2. Set controls as follows:

8565A:
Set all Normal Settings (controls marked with green)
FREQUENCY BAND GHz ..... .01−1.8
INPUT ATTEN ..... 10 dB
REF LEVEL dBm .... Set for same level as plug-in maximum leveled power
FREQUENCY SPAN MODE ..... FULL BAND

8350A
Press **INSTR PRESET**, **CW**, and enter the low frequency limit of the plug-in used.

Plug-in
POWER ..... maximum specified
CW FILTER ..... ON

4-17. SPURIOUS SIGNALS TEST (Cont'd)

NOTE

The spectrum analyzer originates some mixing products that may appear on the display. If a signal is in question, increase the spectrum analyzer input attenuation by 10 dB, note if signal decreases in amplitude by 10 dB, then return the attenuator to the original position. If the signal in question comes from an external source, it will change by 10 dB. If the signal in question originates in the spectrum analyzer, the level will either change by greater or less than 10 dB or may not change at all.

The 8350A CW control when being rotated may generate some noise spikes.

If a spurious signal is found that appears out of specifications check the fundamental signal amplitude to ensure it is at maximum specified power. Then check spurious level by subsituting a known amplitude signal on the spectrum analyzer.

3. Adjust the 8350A CW control through the entire range of the RF plug-in and check for harmonic and non-harmonic spurious signals. The specifications for harmonic and non-harmonic signals are on the performance test record card step 3.

4. Change the spectrum analyzer to each of the next higher frequency bands and repeat the previous step.

4-18. OUTPUT VSWR TEST

SPECIFICATION:

See Performance Test Record Card in section IV of plug-in manual for output VSWR specifications.

DESCRIPTION:

The RF Output signal is measured using a directional coupler, crystal detector, and oscilloscope. The signal at the oscilloscope contains (1) the incident signal from the oscillator, and (2) the reflected signal. The reflected signal is developed as follows: The incident signal travels down the 20 cm air lines (2 to 18 GHz) or 3 to 6 metres of coaxial cable (.01 to 2 GHz), encounters the open end, and is reflected back to the source. If the reflected signal at the RF OUTPUT connector encounters a perfect 50-ohm source match, no signal is reflected back. However, the greater the mismatch, the greater the reflected signal. This reflected signal either adds to or subtracts from the incident signal. This variation is displayed on the oscilloscope.

4-18. OUTPUT VSWR TEST (Cont'd)

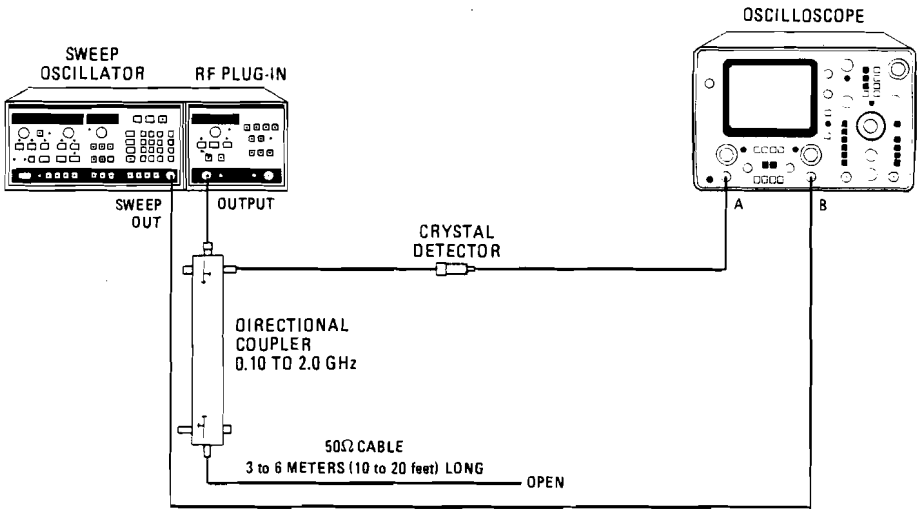


Figure 4-10. Low Frequency Output VSWR Test Setup

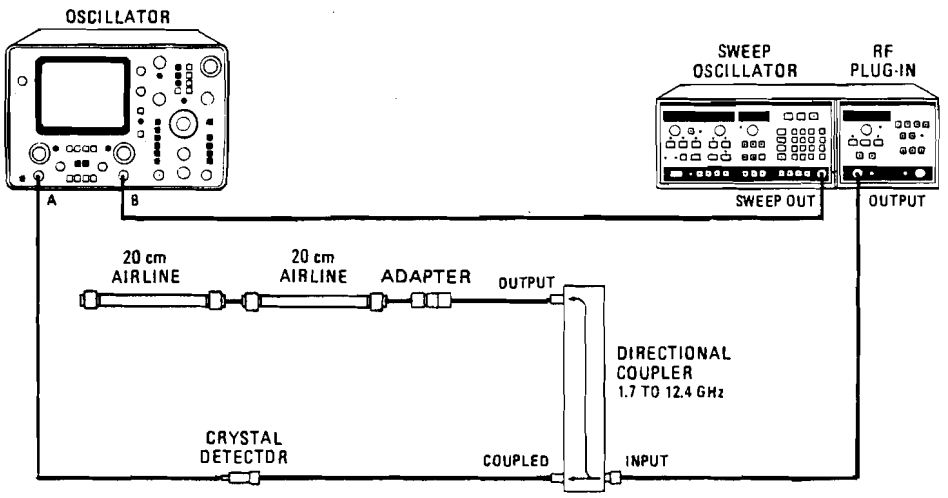


Figure 4-11. High Frequency Output VSWR Test Setup

4-18. OUTPUT VSWR TEST (Cont'd)

EQUIPMENT:

RF Plug-in	HP 83500 series
Oscilloscope	Any general purpose oscilloscope such as HP 1222A or 1740A
Crystal Detector	423B
Directional couplers	
0.10 to 2 GHz	HP 778D
1.7 to 12.4 GHz	HP 779D
Cable	
0.01 to 2 GHz	3 to 6 metres(10 to 20 feet) see Table 4-3
2 to 18	HP 11567A 20-cm Air Lines (2 required)
Adapter APC-7 to Type-N male	HP 11525AC

PROCEDURE:

Low Frequency Output VSWR Test

NOTE

A single section of 3 to 6 metre (10 to 20 feet) 50-ohm cable is required to avoid mismatch of connector when performing the low frequency VSWR test.

1. If the specified output frequency range of the plug-in under test is lower than 2 GHz connect equipment as shown in Figure 4-10 if not go to step 7.

2. Press INSTR PRESET, STOP, 2, GHZ/s on 8350A. Set DISPL BLANK off and RF BLANK on.

3. Adjust POWER level control on plug-in for an maximum output power of −25 millvolts peak trace on oscilloscope display in order to keep crystal in square law output range.

4. Select several points on trace and calculate V MAX/V MIN (see Figure 4-12).

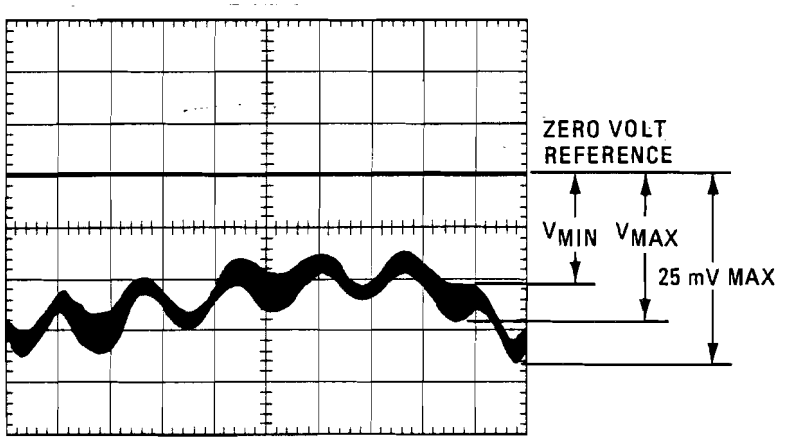


Figure 4-12. Typical Low Frequency Swept VSWR Measurement

4-18. OUTPUT VSWR TEST (Cont'd)

5. Determine the loss at selected frequency of the length of coaxial cable (between coupler end and cable open end), using manufacturer's specifications for loss/foot. (Refer to Table 4-4.)

6. Convert V MAX/V MIN ratio noted in step 5 into sourch match SWR, using Figure 4-13 and the cable loss calculated in step 5. The SWR should be less than noted on the performance test card step 6.

High Frequency Output VSWR Test

7. Connect equipment as shown in Figure 4-11.

8. Press INSTR PRESET, START, 2, GHz/s on 8350A. Set DISPL BLANK off and RF BLANK on.

9. Adjust POWER control on plug-in for a maximum output power of −25 millivolts peak trace on oscilloscope display in order to keep crystal in square law output range.

10. Select points on trace where V MAX/V MIN appear to have greatest separation and calculate V MAX/V MIN for each point.

11. Convert greatest V MAX/V MIN ratio noted in step 10 into source match SWR using Figure 4-13 on the 0 dB loss line. The SWR should be less than noted on the performance test record card step 11.

Table 4-4. Loss in Coaxial Cable

RG Cable Type	Attenuation (dB/100 ft.) at Selected Frequency					
	0.1 GHz	0.2 GHz	0.4 GHz	0.6 GHz	1 GHz	3 GHz
58/U	2.4	3.6	5.2	6.6	8.8	16.7
98/U	2.3	3.4	5.2	6.5	9.0	17.0
55A/U	4.8	7.0	10.5	13.0	17.0	32.0
58A/U	6.2	9.2	14.0	17.5	23.5	45.0
58C/U	6.2	9.2	14.0	17.5	23.5	45.0
177/U	0.95	1.5	2.4	3.2	4.5	9.5
212/U	2.4	3.6	5.2	6.6	8.8	16.7
213/U	2.1	3.1	5.0	6.5	8.8	17.5
214/U	2.3	3.4	5.2	6.5	9.0	17.0
215/U	2.1	3.1	5.0	6.5	8.8	16.7
217/U	1.5	2.3	3.5	4.4	6.0	11.7
218/U	0.95	1.5	2.4	3.2	4.5	9.5
219/U	0.95	1.5	2.4	3.2	4.5	9.5
220/U	0.69	1.12	1.85	—	3.6	7.7
221/U	0.69	1.12	1.85	—	3.6	7.7
223/U	4.8	7.0	10.5	13.0	17.0	32.0
224/U	1.5	2.3	3.5	4.4	6.0	11.7

PERFORMANCE TESTS

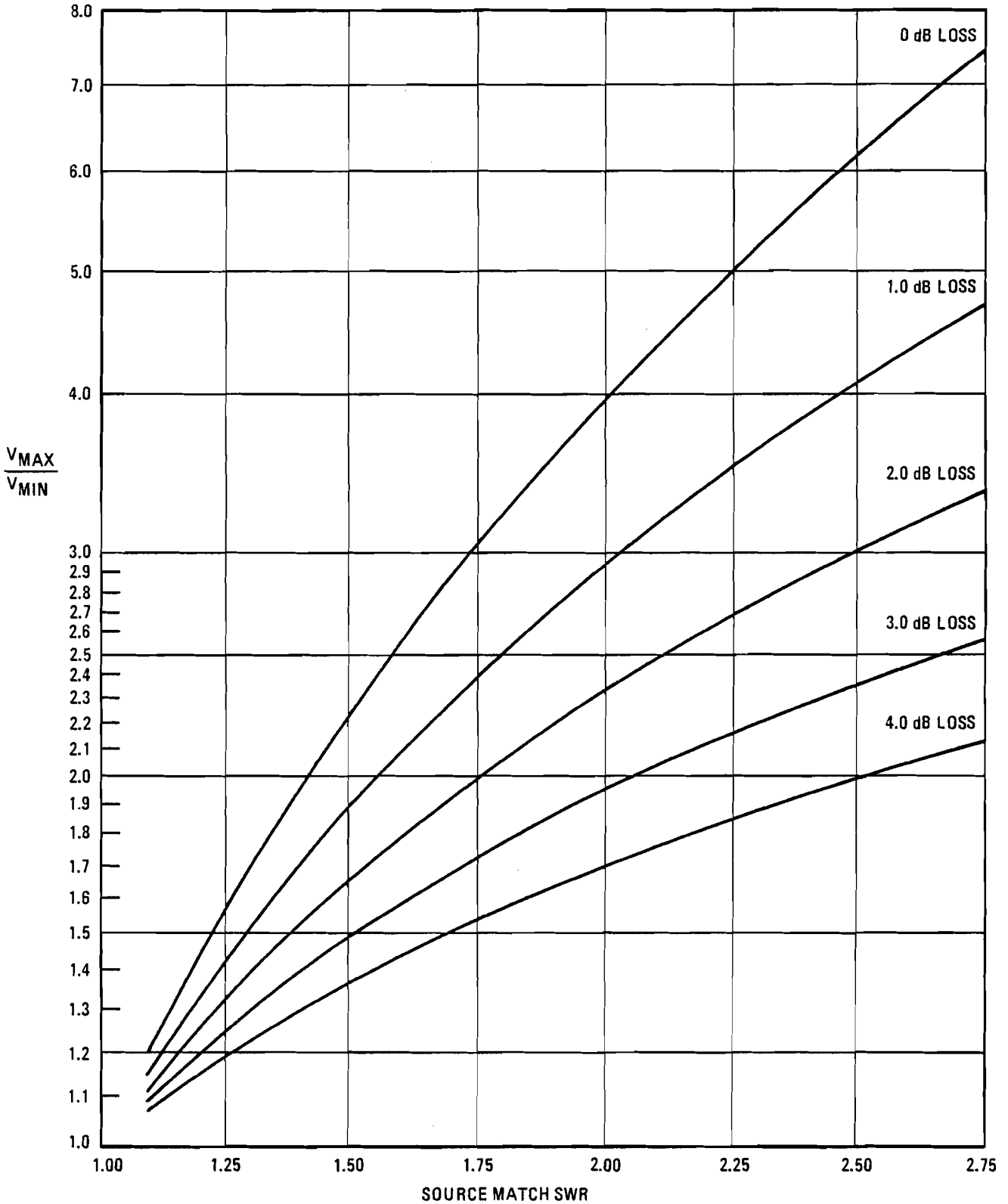


Figure 4-13. Conversion of Oscilloscope Trace to Source Match SWR

4-19. RESIDUAL AM

SPECIFICATION:

See Performance Test Record Card in section IV of plug-in manual for Residual AM specification.

DESCRIPTION:

The RF Output signal from RF Plug-in is amplitude modulated with square wave from the 8350A. This modulated signal is used to establish a reference on the RMS voltmeter that is 9 dB below actual carrier signal. The 9 dB reduction occurs because of voltmeter response to square wave and square-law response of crystal detector. Modulation is then removed and magnitude of Residual AM component is measured with respect to established reference.

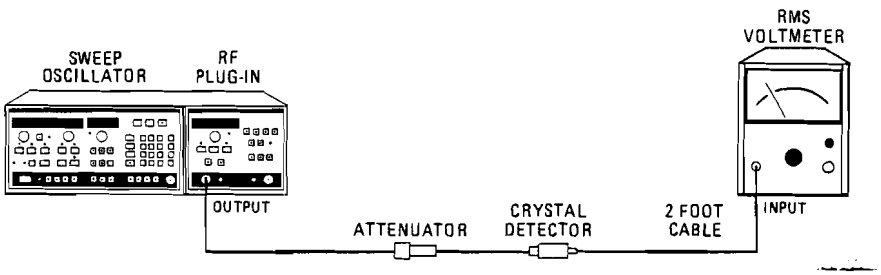


Figure 4-14. Residual AM Test Setup

EQUIPMENT:

RF Plug-in	HP 83500 series
RMS Voltmeter	HP 3400A
Crystal Detector	HP 423B
Attenuator	Refer to PROCEDURE
60 cm (24 in) cable (Limits bandwidth to approximately 100 kHz)	HP11170B

PROCEDURE:

1. Connect equipment as shown in Figure 4-14 using a 20 dB attenuator.
2. Press INSTR PRESET, CW, engage ⎍ MOD (1 kHz or 27.8 kHz), disengage DISPL BLANK.

NOTE

A 41 dB decrease in the RMS voltmeter indication corresponds to a 50-dB reduction in signal level. A correction factor of 9 dB is added because of the RMS voltmeter response to a square wave and the square-law response of the crystal detector.

4-19. RESIDUAL AM (Cont'd)

3. Enter frequency and power shown on test card step 3.

4. Vary attenuation using 3 dB, 6 dB, and 10 dB attenuators until reading on RMS voltmeter is −28 dB ±3 dB. Note voltmeter reading.

5. Disengage RF MOD. Change RMS voltmeter range switch to obtain an on-scale indication. Calculate the difference between this reading and the indication noted in step 4. Add 9 dB to compensate for square-law inequities, and record this number on the test record card step 5.

6. Engage RF MOD. If plug-in is a multiband unit repeat steps 4 and 5 for frequency/ies shown on test card step 6.

4-20. EXTERNAL FREQUENCY MODULATION TEST

SPECIFICATION:

See Performance Test Record Card in section IV of plug-in manual for External FM deviation specifications.

DESCRIPTION:

The RF Output is modulated with an external signal at 100 Hz, 1 MHz, 2 MHz and 10 MHz. The 100 Hz deviation is measured directly on a spectrum analyzer. The deviation at the higher frequencies is found by using a delay line discriminator to observe an increase in the modulation on an oscilloscope until distortion is observed. This frequency change is measured on a frequency counter.

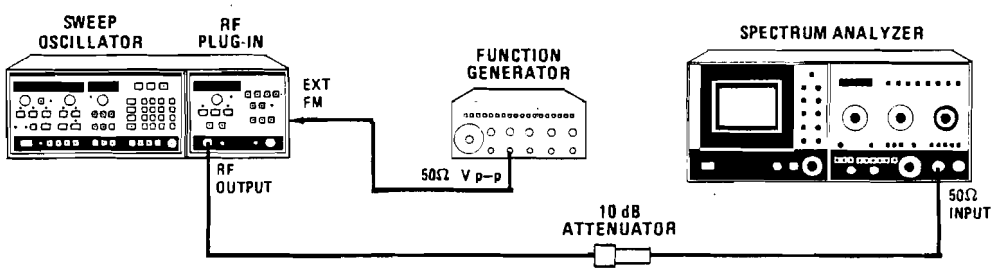


Figure 4-15. 100 Hz External Frequency Modulation Test Setup

4-20. EXTERNAL FREQUENCY MODULATION TEST (Cont'd)

EQUIPMENT:

RF Plug-in	HP 83500 series
Spectrum Analyzer	HP 8565A
Frequency Counter	HP 5343A
Function Generator	HP 3312A
Oscilloscope	Any general purpose oscilloscope such as HP 1222A* or 1740A
10 dB Attenuator	HP 8491B, Opt. 010
Power Splitter	HP 11667A
Delay Line Discriminator	(See Figure 1-3)

*Add a 50Ω load and BNC Tee to each oscilloscope input.

PROCEDURE:

100 Hz Modulation

1. Ensure that modulation sensitivity is set to −20 MHz/volt and modulation coupling to DC. Refer to section III of the plug-in manual for information on FM switch position. Connect equipment as shown in Figure 4-15.

2. Press 8350A INSTR PRESET, CW and disengage the DISPL BLANK key. Disengage RF plug-in CW FILTER key. Center fundamental signal on spectrum analyzer CRT display. Set function generator frequency to 100 Hz sinewave and amplitude to full counterclockwise. Adjust function generator amplitude control slowly clockwise while monitoring display on spectrum analyzer. Deviation from center line should be symmetrical at first then become non-symmetrical as deviation increases.

3. Note point at which deviation becomes non-symmetrical. Record the highest symmetrical observed deviation frequency on the test card step 3.

4. Turn 8350A LINE switch to off. Remove RF plug-in and switch modulation coupling to cross-over (refer to plug-in manual section III). Install the RF plug-in and turn the 8350A LINE switch to on. Then repeat steps 2 and 3 and record the deviation on test card step 4.

>100 Hz FM Modulation

4-20. EXTERNAL FREQUENCY MODULATION TEST (Cont'd)

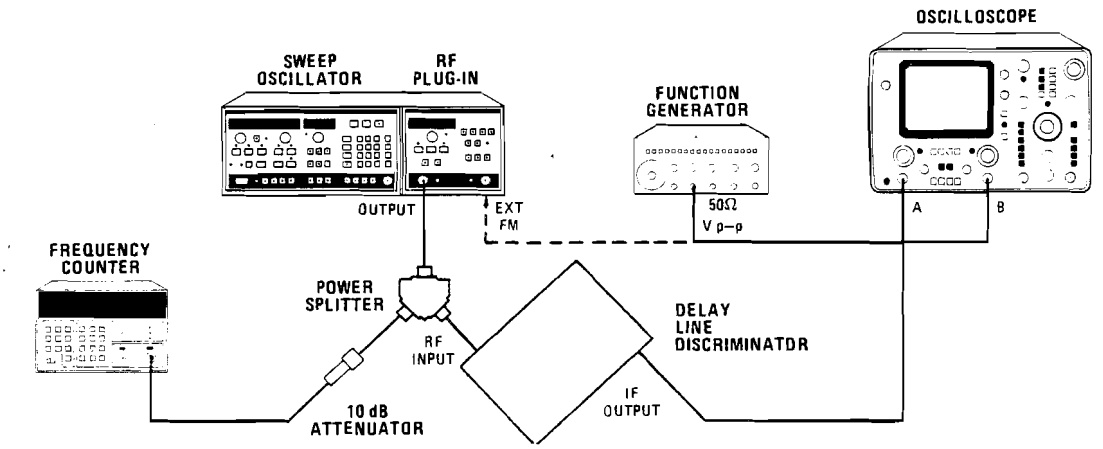


Figure 4-16. >100Hz Frequency Modulation Test Setup

5. Set function generator frequency to 1 MHz. Set both oscilloscope inputs to 50Ω.

6. Set function generator output amplitude to 0.1 volt p-p output. Connect equipment as shown in Figure 4-16 with function generator output not connected. Adjust CW and CW VERNIER for a delay line discriminator output of '0' volts as observed on oscilloscope. Note frequency counter reading on test card step 6.

7. Connect function generator output to 8350A FM INPUT (rear panel) and adjust oscilloscope for a clear display of the function generator sinewave.

8. Increase the function generator output amplitude until the deviation becomes non-symmetrical or distorted. Use oscilloscope B input to monitor function generator output. If the output is offset the test is invalid.

9. Mark peak of sinewave on oscilloscope with grease pencil. Remove function generator output from FM INPUT and adjust CW/CW VERNIER to the grease pencil mark. Calculate the difference between the present frequency counter reading and the previous reading (step 6). Record on the test card step 9.

10. Set the function generator to 2 MHz then 10 MHz repeating steps 6 through 9 for each frequency and record the results on the test card step 10.

11. Change mode of plug-in modulation coupling and repeat steps 6 through 10. Record the results on the test card step 11.

4-21. FM FREQUENCY RESPONSE TEST

SPECIFICATION:

See Performance Test Record Card in section IV of plug-in manual for FM Response specifications.

DESCRIPTION:

FM deviation of the RF Plug-in is compared to a known voltage reference using a delay line discriminator, and the difference is measured with an oscilloscope. Since the oscilloscope is calibrated so that four major divisions are equal to 100 percent, each minor division is equal to 5 percent. A difference of +41, −29 percent is approximately equal to ±3 dB, and a difference of +18, −16 percent is approximately equal to ±1.5 dB.

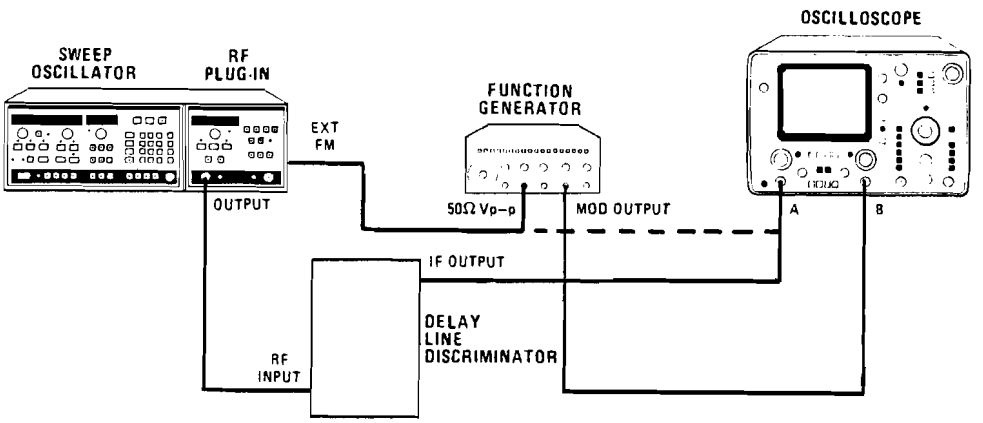


Figure 4−17. FM Frequency Response Test Setup

EQUIPMENT:

RF Plug-in	HP 83500 series
Oscilloscope	Any general purpose oscilloscope such as HP 1222A* or 1740A
Function Generator	HP 3312A
Delay Line Discriminator	(See Figure 1-3)

*Add a 50Ω load and BNC Tee to oscilloscope Channel A input.

PROCEDURE:

1. Connect equipment as shown in Figure 4-17. Press 8350A INSTR PRESET, CW and disengage DISPL BLANK, and plug-in CW FILTER.

4-21. FM FREQUENCY RESPONSE TEST (Cont'd)

2. Set controls as follows:

Oscilloscope
CHAN A
VOLTS/DIV ..... 0.02(CAL)
Input..... 50Ω

Mode..... A vs. B
CHAN B volts/DIV 1

Function Generator:
RANGE Hz 100
FREQUENCY..... 10
FUNCTION ..... ~
OFFSET..... CAL
SYM ..... CAL
MODULATION ..... SWP
SWP START ..... Fully counterclockwise
RANGE Hz VERNIER..... Best display

3. Adjust the oscilloscope with GND reference switched in for a trace on center line then reset oscilloscope to 50Ω input. Connect the function generator output to Channel A and adjust output for 100 mv peak-to-peak on CRT. Reconnect the equipment as shown in Figure 4-17. Check GND reference on oscilloscope. Return oscilloscope to 50Ω input. Adjust CW and CW Vernier control to center trace on CRT.

4. Set Oscilloscope Channel A Volts/DIV to .005 (CAL). Adjust the oscilloscope CAL control for a four-division discriminator output display on the oscilloscope.

5. Vary function generator frequency from 0.1 Hz to 2 MHz. Record maximum amplitude deviations of trace on the performance test record card step 5.

4-22. AM ON/OFF RATIO AND SQUARE WAVE SYMMETRY TEST

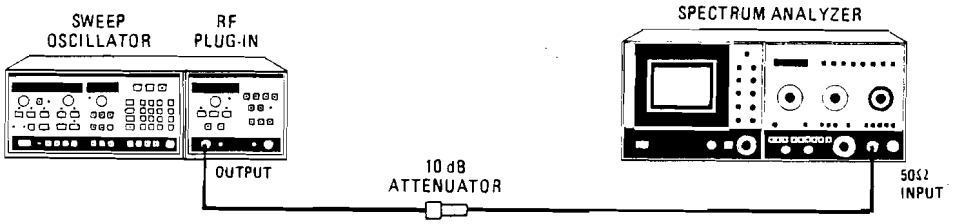
SPECIFICATION:

See Performance Test Record Card in section IV of plug-in manual for AM on/off ratio and square wave symmetry specifications.

DESCRIPTION:

The AM ON/OFF ratio is checked on the amplitude axis of a video triggered spectrum analyzer display. The symmetry is checked by calculating the on/off time ratio on the frequency axis.

4-22. AM ON/OFF RATIO AND SQUARE WAVE SYMMETRY TEST (Cont'd)



4-18. AM ON/OFF Ratio and Square Wave Symmetry Test Setup

EQUIPMENT:

RF Plug-in	HP 83500 series
10 dB Attenuator	HP 8491B, Opt. 010
Spectrum Analyzer	HP 8565A

PROCEDURE:

1. Connect equipment as shown in Figure 4-18. Press 8350A INSTR PRESET, CW and engage ⊓ MOD. Set 8350A frequency as shown on test card step 1. Set plug-in to maximum rated output power.

2. Set controls as follows:

   8565A:
   Set all Normal Settings (controls marked with green)

FREQUENCY BAND GHz	To cover CW set
INPUT ATTENUATION	10 dB
REFERENCE LEVEL	10 dBm
FREQUENCY SPAN MODE	ZERO SPAN
SWEEP TRIGGER	VIDEO
RESOLUTION BW	3 MHz
AUTO STABILIZER	OFF
SWEEP TIME/DIV	.1 msec for 1 kHz 5 μsec for 27.8 kHz

3. Adjust spectrum analyzer TUNING control to observe signal on CRT. Adjust REFERENCE LEVEL to set signal on top trace. Record AM ON/OFF ratio on test card step 3.

4. Record the symmetry of the observed signal on the test card step 4.

5. Set CW frequency as indicated on test record card step 5. Repeat steps 3 and 4 and record results on test record card steps 5.

4-23. STEP ATTENUATOR ACCURACY TEST (OPTION 002)

SPECIFICATION:

If plug-in is Option 002 see Performance Test Record Card in section IV of plug-in manual for Attenuator Accuracy specifications.

DESCRIPTION:

The plug-in RF output is compared to a specially calibrated attenuator and displayed on a spectrum analyzer.

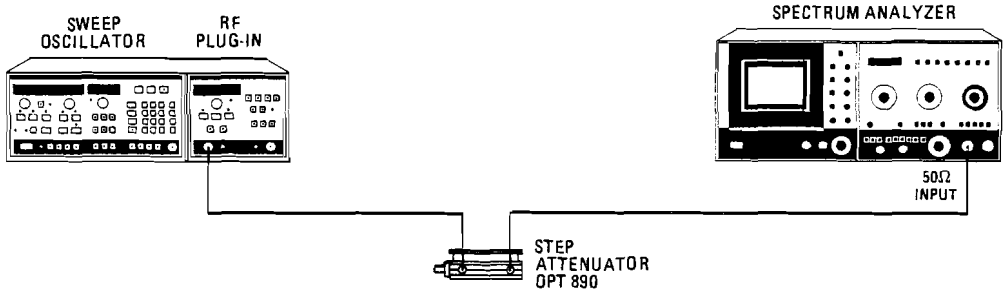


Figure 4-19. Attenuator Accuracy Test Setup

EQUIPMENT:

RF Plug-in	HP 83500 series
Step Attenuator	HP 8495A Opt. 890
Spectrum Analyzer	HP 8565A

PROCEDURE:

NOTE

Frequency may be set to any value listed on Calibration Report within Plug-in frequency. Use Calibration Report data for frequency of plug-in output.

1. Connect equipment as shown in Figure 4-19. Press 8350A INSTR PRESET, CW. Enter the frequency and power level shown on the test card step 1.

2. Set controls as follows:

Step Attenuator	
ATTENUATION	As shown on test card step 4

4-23. STEP ATTENUATOR ACCURACY TEST (OPTION 002) (Cont'd)

Spectrum Analyzer
Set all normal settings (controls marked with green)

INPUT ATTEN	10 dB
REFERENCE LEVEL	−50 dBm
RESOLUTION BANDWIDTH	1 MHz
FREQUENCY SPAN/DIV	5 MHz
FREQUENCY SPAN MODE	FULL BAND
VIDEO FILTER	Adjust as necessary
FREQUENCY BAND	Select to cover frequency in step 1

3. Press 8350A POWER LEVEL, STEP SIZE, 1, 0, and dBm/dB.

4. Record the actual Attenuation values listed on the calibration report (Option 890) at the frequency and the seven attenuation steps used. Calculate the variation from 10 dB between adjacent attenuator settings (example: Calibration report lists 30.15 for the 30 dB attenuator setting and 39.95 for the 40 dB attenuator setting. The variation from the set 10 dB change is 0.2 dB.) Enter the values in the appropriate places on the test card.

5. Adjust spectrum analyzer TUNING control to center notch on sweep oscillator output signal. Reduce spectrum analyzer FREQUENCY SPAN/DIV to .2 MHz and recenter TUNING control. Press FREQUENCY SPAN MODE ZERO SPAN key and adjust FINE TUNING to peak signal on spectrum analyzer display. Adjust spectrum analyzer REFERENCE LEVEL VERNIER for a trace at the center gradicule line. Press 1 dB/DIV and recenter trace.

6. Press the 8350A ◄ key and decrease the reference attenuation by 10 dB.

7. Record the power level change observed on the spectrum analyzer display (be sure to designate the direction of the change: +−) and add it to the variation value recorded in step 4.

8. Record this sum on the test record card then repeat steps 6 and 7 for the other attenuation values.

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

5-2. This section provides adjustment procedures for the Model 8350A Sweep Oscillator. These procedures should not be performed as routine maintenance but should be used (1) after replacement of a part or component, or (2) when performance tests show that the specifications of Table 1-1 cannot be met. Table 5-1 lists all of the adjustments by reference designation, adjustment name, adjustment paragraph, performance test paragraph, and description. Each procedure includes a test setup illustration and one or more adjustment location illustrations.

NOTE

Allow the 8350A Sweep Oscillator to warm up for 30 minutes prior to making any adjustments.

5-3. SAFETY CONSIDERATIONS

5-4. Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by a skilled person who is aware of the hazard involved.

WARNING

Adjustments in this section are performed with power supplied to the instrument while protective covers are removed. There are voltages at points in the instrument which can, if contacted, cause personal injury. Be extremely careful. Adjustments should be performed only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged, even if the instrument has been disconnected from its power supply source.

Use a non-metallic adjustment tool whenever possible.

5-5. EQUIPMENT REQUIRED

5-6. Table 1-4 lists the equipment required for the adjustment procedures. If the test equipment recommended is not available, other equipment may be used if its performance meets the Critical Specifications listed in Table 1-4. The specific equipment required for each adjustment is referenced in each procedure.

5-7. FACTORY-SELECT COMPONENTS

5-8. Table 5-2 contains a list of factory-selected components that include the reference designation, the related performance test, the allowable range of values, and the basis of selection. Nominal values are given for the factory-selected components, designated by an asterisk (*), on the schematic diagram and in the replaceable parts list. HP Part Numbers for selected values are given in Table 5-3. Check Digit information is given as an ordering convenience.

5-9. RELATED ADJUSTMENTS

5-10. Interactive adjustments are noted in the adjustment procedures. Table 5-4 indicates, by paragraph numbers, the adjustments that must be performed if an assembly has been repaired or replaced or if an adjustment has been made on an assembly. Table 5-5 lists the adjustment procedures included in this section.

Table 5-1. Adjustable Components

Reference Designation	Adjustment Name	Adjustment Paragraph	Description
A4R2	ΔF OFFSET	5-19	Sets low end of band frequency accuracy (OFFSET) in ΔF sweep mode.
A4R15	ΔF2	5-19	Sets frequency accuracy (GAIN) in ΔF sweep mode for ΔF settings <1/8 and ≥1/64 of RF plug-in band.
A4R18	ΔF3	5-19	Sets frequency accuracy (GAIN) in ΔF sweep mode for ΔF settings <1/64 of RF plug-in band.
A4R22	VERNIER	5-19	Sets symmetry (GAIN) of VERNIER control at low end of VERNIER range.
A4R25	ΔF1	5-19	Sets high end of band frequency accuracy (GAIN) in ΔF sweep mode for ΔF settings ≥1/8 of RF plug-in band.
A4R27	CW	5-19	Sets frequency accuracy (GAIN) in CW sweep mode.
A4R28	MKR	5-20	Sets marker frequency accuracy (GAIN).
A4R44	CW OFFSET	5-19	Sets symmetry (OFFSET) of VERNIER at high end of VERNIER range.
A4R59	+10V REF	5-14	Adjusts +10V REF DAC power supply.
A5R2	10 mSEC	5-15	Sets sweep time accuracy for sweep times <1 second.
A5R25	1 SEC	5-15	Sets sweep time accuracy for sweep times from 1 second to 100 seconds.
A5R43	MANUAL	5-16	Sets sweep ramp accuracy in MANual sweep mode.
A5R51	SQUARE WAVE	5-18	Sets internal AM 27.8/1 kHz oscillator frequency accuracy.
A7R10	+20V	5-11	Adjusts +20V REG power supply
A7R21	−10V	5-11	Adjusts −10V REG power supply
A7R39	−40V	5-11	Adjusts −40V REG power supply
A7R58	AIRFLOW BAL	5-12	Adjusts airflow detection circuit temperature threshold.

Table 5-2. Factory Select Components

Reference Designator	Adjustment Paragraph	Allowable Range of Values	Basis of Selection
A5R70	5-17	not critical	Selected to set the retrace time for a 10 ms sweep to insure repetitive sweeps on LINE SWEEP TRIGGER.
A7R76	5-13	not critical	Selected to set the output voltage level of the +5VB power supply under a no load condition.

Table 5-3. HP Part Numbers of Standard Value Replacement Components

RESISTORS

RANGE: 10 to 1.47M Ohms
TYPE: Fixed-Film
WATTAGE: 0.5 at 125°C
TOLERANCE: ±1%

Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D	Value (Ω)	HP Part Number	C D
10.0	0757-0984	4	215	0698-3401	0	4.64K	0698-3348	4	110K	0757-0859	2
11.0	0575-0985	5	237	0698-3102	8	5.11K	0757-0833	2	121K	0757-0860	5
12.1	0757-0986	6	261	0757-1090	5	5.62K	0757-0834	3	133K	0757-0310	0
13.3	0757-0001	6	287	0757-1092	7	6.19K	0757-0196	0	147K	0698-3175	5
14.7	0698-3388	2	316	0698-3402	1	6.81K	0757-0835	4	162K	0757-0130	2
16.2	0757-0989	9	348	0698-3403	2	7.50K	0757-0836	5	178K	0757-0129	9
17.8	0698-3389	3	383	0698-3404	3	8.25K	0757-0837	6	196K	0757-0063	0
19.6	0698-3390	6	422	0698-3405	4	9.09K	0757-0838	7	215K	0757-0127	7
21.5	0698-3391	7	464	0698-0090	7	10.0K	0757-0839	8	237K	0698-3424	7
23.7	0698-3392	8	511	0757-0814	9	12.1K	0757-0841	2	261K	0757-0064	1
26.1	0757-0003	8	562	0757-0815	0	13.3K	0698-3413	4	287K	0757-0154	0
28.7	0698-3393	9	619	0757-0158	4	14.7K	0698-3414	5	316K	0698-3425	8
31.6	0698-3394	0	681	0757-0816	1	16.2K	0757-0844	5	348K	0757-0195	9
34.8	0698-3395	1	750	0757-0817	2	17.8K	0698-0025	8	383K	0757-0133	5
38.3	0698-3396	2	825	0757-0818	3	19.6K	0698-3415	6	422K	0757-0134	6
42.2	0698-3397	3	909	0757-0819	4	21.5K	0698-3416	7	464K	0698-3426	9
46.4	0698-3398	4	1.00K	0757-0159	5	23.7K	0698-3417	8	511K	0757-0135	7
51.1	0757-1000	7	1.10K	0757-0820	7	26.1K	0698-3418	9	562K	0757-0868	3
56.2	0757-1001	8	1.21K	0757-0821	8	28.7K	0698-3103	9	619K	0757-0136	8
61.9	0757-1002	9	1.33K	0698-3406	5	31.6K	0698-3419	0	681K	0757-0869	4
68.1	0757-0794	4	1.47K	0757-1078	9	34.8K	0698-3420	3	750K	0757-0137	9
75.0	0757-0795	5	1.62K	0757-0873	0	38.3K	0698-3421	4	825K	0757-0870	7
82.5	0757-0796	6	1.78K	0698-0089	4	42.2K	0698-3422	5	909K	0757-0138	0
90.0	0757-0797	7	1.96K	0698-3407	6	46.4K	0698-3423	6	1M	0757-0059	4
100	0757-0198	2	2.15K	0698-3408	7	51.1K	0757-0853	6	1.1M	0757-0139	1
110	0757-0798	8	2.37K	0698-3409	8	56.2K	0757-0854	7	1.21M	0757-0871	8
121	0757-0799	9	2.61K	0698-0024	7	61.9K	0757-0309	7	1.33M	0757-0194	8
133	0698-3399	5	2.87K	0698-3101	7	68.1K	0757-0855	8	1.47M	0698-3464	5
147	0698-3400	9	3.16K	0698-3410	1	75.0K	0757-0856	9			
162	0757-0802	5	3.48K	0698-3411	2	82.5K	0757-0857	0			
178	0698-3334	8	3.83K	0698-3412	3	90.9K	0757-0858	1			
196	0757-1060	9	4.22K	0698-3346	2	100K	0757-0367	7			

Table 5-4. Related Adjustments

Assembly Changed or Repaired		Related Assemblies	Perform the Following Paragraph Number
A1	Front Panel	A1	None
A2	Front Panel Interface	A2	None
A3	Microprocessor	A3	None
A3A1	PROM	A3A1	None
A4	Scaling and Marker	A4, A5	5-14, 5-16, 5-19, 5-20
A5	Sweep Generator	A6, A7	5-14, 5-15, 5-16, 5-17, 5-18
A6	Rectifier	A6, A7	5-11, 5-12, 5-13
A7	Regulator	A7	5-11, 5-12, 5-13
A8	HP-IB Interface	A8	None

Table 5-5. Adjustments

Paragraph	Adjustment
5-11	+20V, −40V, AND −10V POWER SUPPLY ADJUSTMENTS
5-12	AIRFLOW DETECTOR ADJUSTMENT
5-13	+5VB POWER SUPPLY ADJUSTMENT
5-14	+10V REF DAC POWER SUPPLY ADJUSTMENT
5-15	SWEEP TIME ADJUSTMENTS
5-16	MANUAL SWEEP ADJUSTMENT
5-17	SWEEP RETRACE TIME ADJUSTMENTS
5-18	28.8/1 kHz OSCILLATOR ADJUSTMENT
5-19	FREQUENCY CONTROL ADJUSTMENTS
5-20	MARKER DAC ADJUSTMENT

ADJUSTMENTS

5-11. +20V, −40V, AND −10V POWER SUPPLY ADJUSTMENTS

REFERENCE:

A7 Regulator

DESCRIPTION:

The +20V, −40V, and −10V power supplies are adjusted under load for the proper voltage levels with an HP 83500 Series RF plug-in or HP 11869A RF Plug-in Adapter installed.

5-11. +20V, −40V, and −10V POWER SUPPLY ADJUSTMENTS (Cont'd)

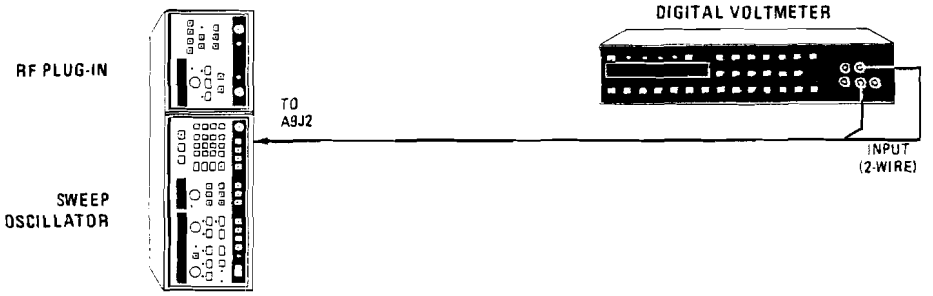


Figure 5-1. +20V, −40V, and −10V Power Supply Adjustments Setup.

EQUIPMENT:

Sweep Oscillator	HP 8350A
RF Plug-in	any HP 83500 Series RF Plug-in or HP 11869A RF Plug-in Adapter
Digital Voltmeter (DVM)	HP 3455A

PROCEDURE:

1. Install an HP 83500 Series RF plug-in (or the HP 11869A RF Plug-in Adapter) in the HP 8350A mainframe.

2. Set LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.

3. Position the sweep oscillator on its side as shown in Figure 5-1 and remove the top and bottom covers.

4. Connect the DVM to the bottom of the A9 Motherboard connector A9J2 pin 7 (+20V RETURN SENSE) and A9J2 pin 6 (+20V SENSE). A7DS2 (green LED) should be lit. Refer to Figure 5-2 for A7 Regulator component locations.

5. Adjust A7R10 +20V ADJ for a DVM reading of 20.000 ± 0.001 Vdc. Refer to Figure 5-2 for adjustment location.

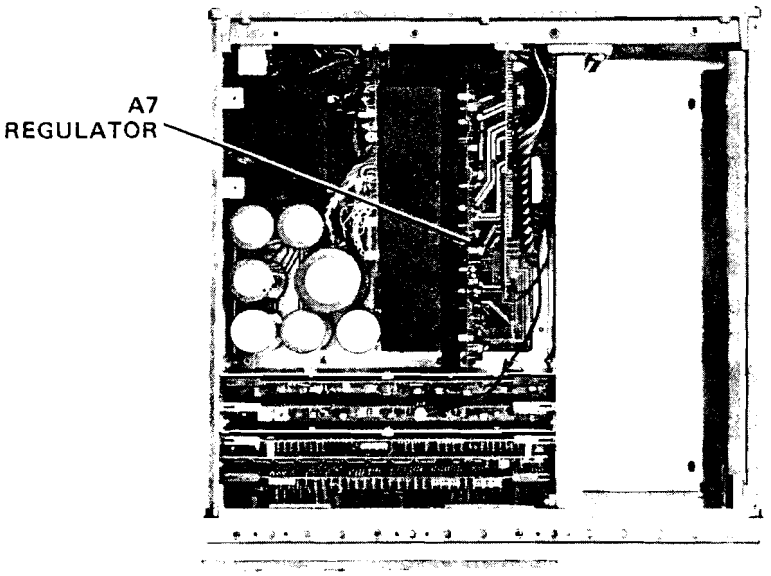
6. Connect the DVM to the bottom of the A9 Motherboard connector A9J2 pin 16 (−40V RETURN SENSE) and A9J2 pin 15 (−40V SENSE). A7DS4 should be lit. Refer to Figure 5-2 for A7 Regulator component locations.

7. Adjust A7R39 −40V ADJ for a DVM reading of −40.000 ± 0.002 Vdc. Refer to Figure 5-2 for adjustment location.

8. Connect the DVM to the bottom of the A9 Motherboard connector A9J2 pin 12 (−10V RETURN SENSE) and A9J2 pin 11 (−10V SENSE). A7DS3 should be lit. Refer to Figure 5-2 for A7 Regulator component locations.

9. Adjust A7R21 −10V ADJ for a DVM reading of −10.000 ± 0.001 Vdc. Refer to Figure 5-2 for adjustment location.

5-11. +20V,−40V, and −10V POWER SUPPLY ADJUSTMENTS (Cont'd)



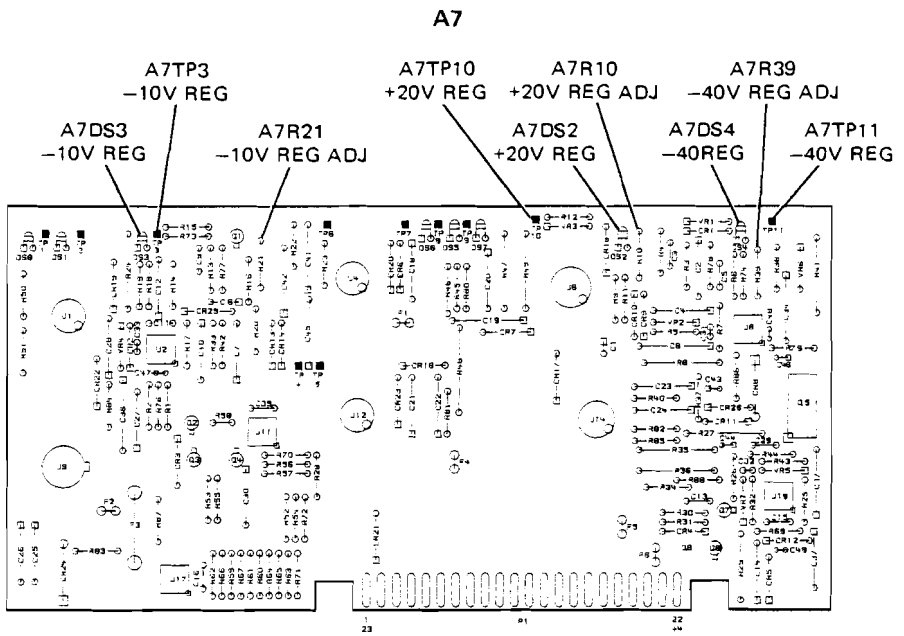


Figure 5-2. Location of +20V, −40V, and −10V Power Supply Adjustments.

5-12. AIRFLOW DETECTOR ADJUSTMENT

REFERENCE:

A7 Regulator

DESCRIPTION:

The Airflow Detection circuit senses the internal air flow generated by fan B1 and flags the A3 Microprocessor if the airflow is restricted. The instrument is allowed to warm up to operating temperature and A7R53 is jumpered by a short to remove the hysteresis from comparator A7U11. A7R58 is then adjusted until the inputs are balanced which will then cause A7U11 output LPST (LOW POWER SUPPLY TEMPERATURE) to oscillate. LPST is monitored by the A3 Microprocessor and the state of the Airflow Detection circuit is sent to the Status Buffer at hexadecimal location 1000H. A Hexadecimal Data Read command (M3) is entered which then displays the current Status Buffer state on the FREQUENCY/TIME LEDs. When the display LEDs oscillate between 00H and 02H, indicating LPST is oscillating, A7R58 is adjusted correctly.

PROCEDURE:

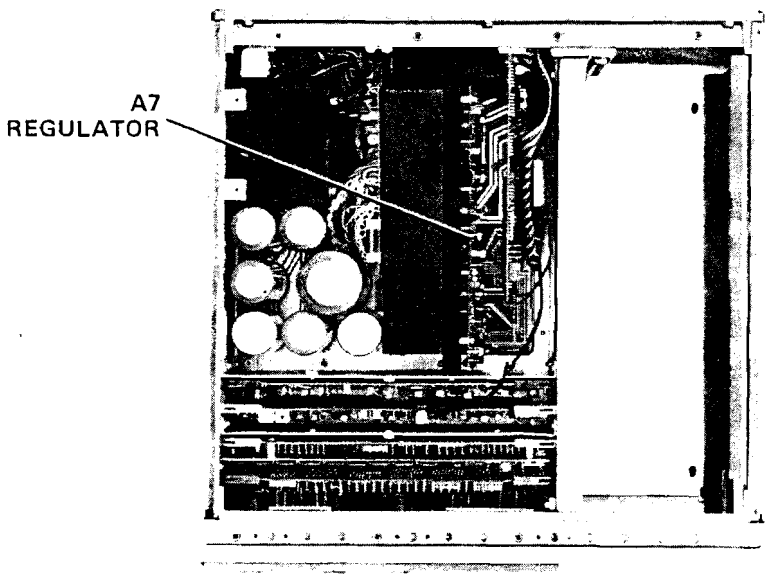
1. Remove the RF plug-in from the sweep oscillator mainframe.
2. Set the LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.
3. Position the sweep oscillator upright and remove the top cover.
4. Short A7TP4 and A7TP5 together. This removes the hysteresis from comparator A7U11. Refer to Figure 5-3 for the location of A7TP4 and A7TP5.
5. Replace the top cover and allow the instrument to operate with top cover in place for 5 minutes.
6. Press INSTR PRESET SHIFT 0 0 M1 1 0 0 0 M3 . This enables the hexadecimal data in the Status Buffer (at address location 1000H) to be displayed on the front panel FREQUENCY/TIME LEDs. The LED display should now read 1000 00 or 1000 02.
7. Adjust A7R58 AIRFLOW BAL until the LED display oscillates between 1000 00 and 1000 02. Refer to Figure 5-3 for A7R58 adjustment location.

NOTE

A7R58 AIRFLOW BAL adjust pot is accessable through the hole in the left support of the RF plug-in opening. This adjustment MUST be made with the 8350A at normal operating temperature and all covers in place.

8. Wait 1 minute after adjustment to insure that the display still oscillates. If it does not and has settled at 1000 00 or 1000 02, repeat steps 6 and 7.
9. Remove jumper from A7TP4 and A7TP5.
10. Verify that the display indicates 1000 00.

5-12. AIRFLOW DETECTOR ADJUSTMENT (Cont'd)



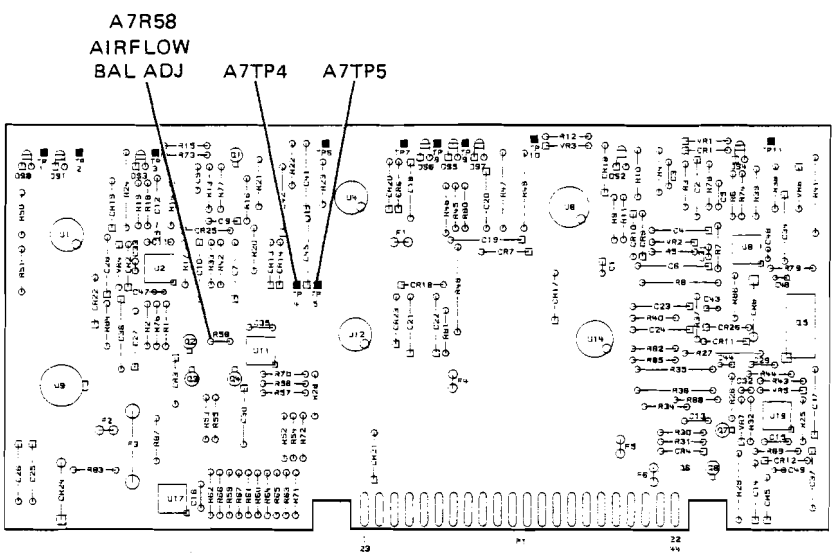


Figure 5-3. Location of AIRFLOW BALance Adjustment.

5-13. +5VB POWER SUPPLY ADJUSTMENT

REFERENCE:

A7 Regulator Assembly

DESCRIPTION:

A7R76* is selected to set the output of A7U10 (+5VB REG) to 5.33 ± 0.03 Vdc in a no load condition (without an RF plug-in installed).

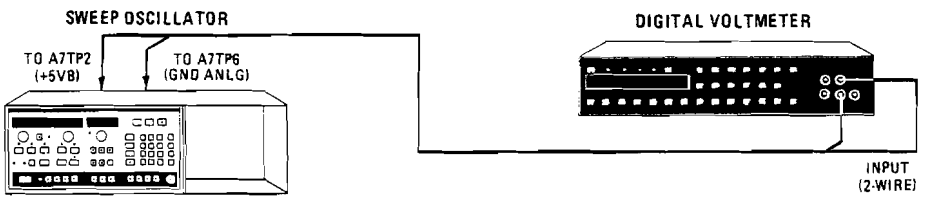


Figure 5-4. +5VB Power Supply Adjustment Setup.

EQUIPMENT:

Sweep Oscillator	HP 8350A
Digital Voltmeter (DVM)	HP 3455A

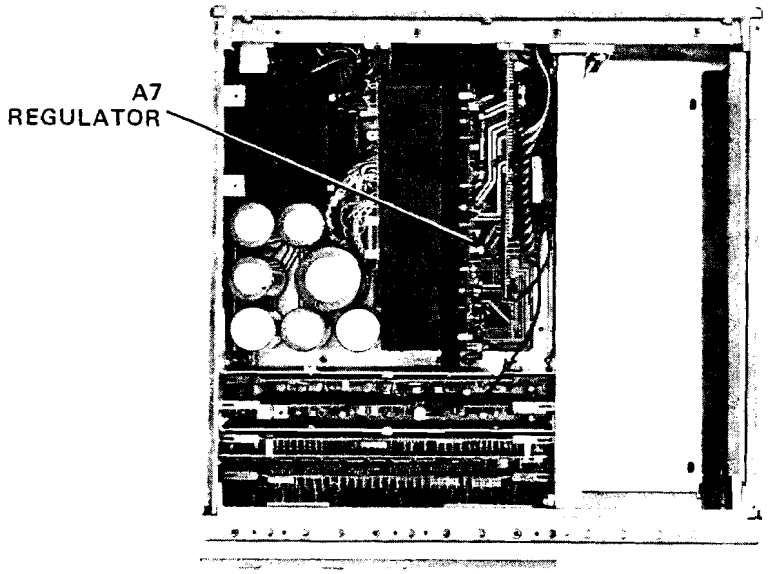
PROCEDURE:

1. Remove the RF plug-in from the sweep oscillator mainframe.
2. Set the LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.
3. Position the sweep oscillator upright as shown in Figure 5-4 and remove the top cover.
4. Connect a shorting jumper from the anode of A7CR22 (+5VB GND REF) to A7TP6 (GND ANLG).
5. Connect the DVM to A7TP2 (+5VB REG) and A7TP6 (GND ANLG). A7DS1 (green LED) should be lit.
6. The DVM should indicate 5.33 ± 0.03 Vdc. If it does not, A7R76* must be changed as necessary to achieve the proper level. Refer to Table 5-2 for the range of values allowable for A7R76*. Refer to Figure 5-5 for A7R76* component location.

NOTE

Decreasing A7R76* to the next lower recommended value shown in Table 5-3 will decrease the level of the +5VB power supply. Inversely, increasing the value of A7R76* to the next higher recommended value will increase the level of the +5VB power supply.

5-13. +5VB POWER SUPPLY ADJUSTMENT (Cont'd)



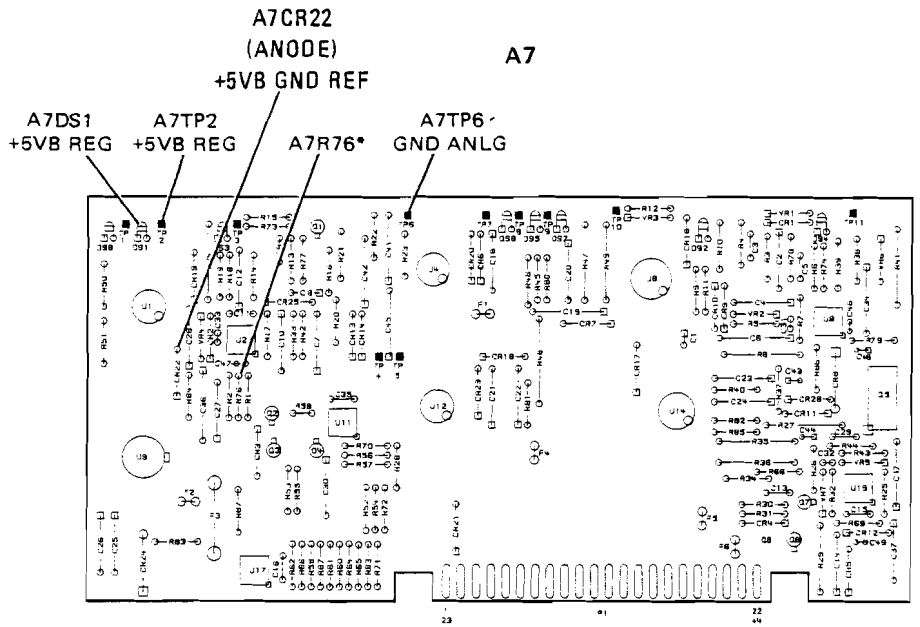


Figure 5-5. Location of +5VB Power Supply Adjustment.

5-14. +10V REF DAC POWER SUPPLY ADJUSTMENT

REFERENCE:

A4 Scaling and Marker Assembly

DESCRIPTION:

A4R59 +10V REF ADJ is adjusted for the proper voltage level to provide an accurate reference voltage for all Digital-to-Analog Converters (DACS) in the 8350A mainframe.

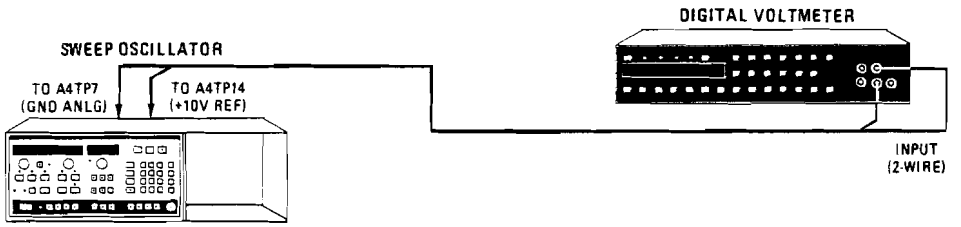


Figure 5-6. +10V REF DAC Power Supply Adjustment Setup.

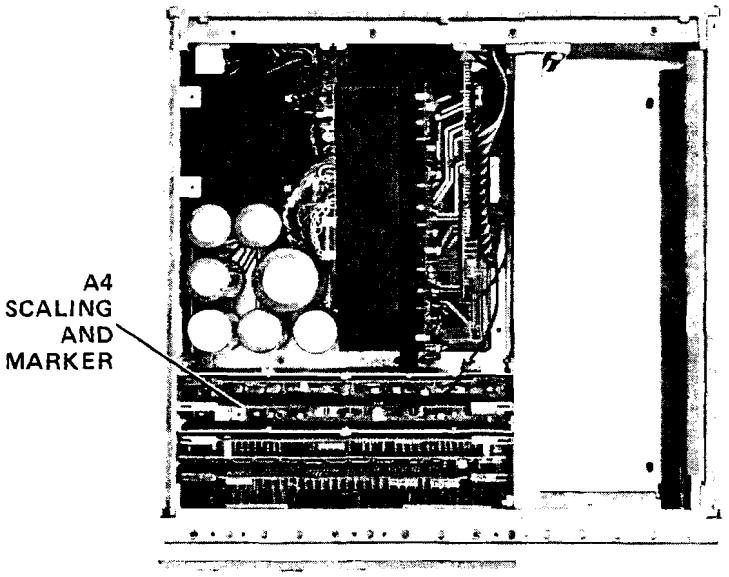
EQUIPMENT:

Sweep Oscillator	HP 8350A
Digital Voltmeter (DVM)	HP 3455A

PROCEDURE:

1. Remove the RF plug-in from the sweep oscillator mainframe.
2. Set the LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.
3. Position the sweep oscillator upright as shown in Figure 5-6 and remove the top cover and the A4/A5 shield cover.
4. Connect the DVM to A4TP14 (+10V REF) and A4TP7 (GND ANLG) as shown in Figure 5-6.
5. Adjust A4R59 +10V REF ADJ for a DVM reading of 10.0000 ± 0.0001 Vdc. Refer to Figure 5-7 for location of adjustment.

5-14. +10V REF DAC POWER SUPPLY ADJUSTMENT (Cont'd)



A4

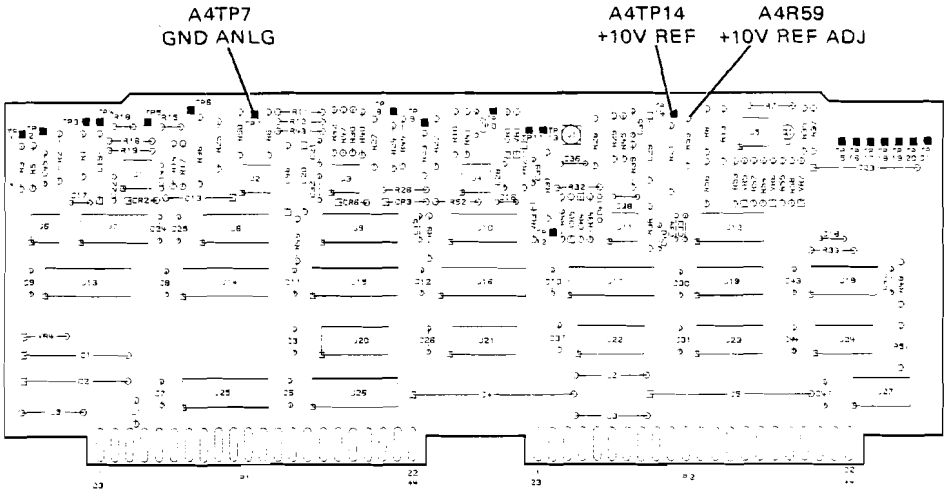


Figure 5-7. Location of +10V REF DAC Power Supply Adjustment.

5-15. SWEEP TIME ADJUSTMENTS

REFERENCE:

A5 Sweep Generator

DESCRIPTION:

Programmable current source A5U2 is a 10-bit Digital-to-Analog Converter (DAC) whose output current determines the sweep time (slope) of the sweep ramp. Input reference current is supplied by the +10V REF power supply through A5R4 and 10 mSEC ADJ pot A5R2 for sweep times < 1 second, and additionally, through A5R28 and 1 SEC ADJ pot A5R25 for sweep times from 1 second to 100 seconds. 8350A rear panel POS Z BLANK BNC output goes low during the forward sweep time and is monitored by a time interval counter (returns high during sweep retrace). A5R2 is adjusted during a 10 ms sweep and A5R25 is adjusted during a 1 second sweep to give the proper forward sweep times for a fast and slow sweep.

Figure 5-8. Sweep Time Adjustments Setup.

EQUIPMENT:

Sweep Oscillator	HP 8350A
Universal Counter	HP 5328A

PROCEDURE:

1. Remove the RF plug-in from the sweep oscillator mainframe.
2. Set the 8350A LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.

NOTE

The validity of this adjustment procedure is based in part on the accuracy of the +10V REF DAC power supply. Proper adjustment of the +10V REF DAC power supply is necessary before proceeding with this adjustment procedure.

5-15. SWEEP TIME ADJUSTMENTS (Cont'd)

3. Connect the POS Z BLANK BNC output connector on the rear panel of the 8350A to the INPUT A connector on the 5328A Universal Counter and set the 5328A controls as follows:

FUNCTION	TI A→B
SAMPLE RATE	CCW
OSC (rear panel)	INT
ARM ON/OFF (rear panel)	OFF
STORAGE ON/OFF (rear panel)	ON
POWER	ON
Input Amplifier Control Switch	COM A
Channel A SLOPE	−
Channel A Coupling	DC
Channel A ATTEN	X10
Channel A Trigger LEVEL A	CW
Channel B SLOPE	+
Channel B Coupling	DC
Channel B ATTEN	X10
Channel B Trigger LEVEL B	CW

4. Position the sweep oscillator upright as shown in Figure 5-8 and remove the top cover.

5. Press INSTR PRESET SWEEP TIME 1 0 ms .

6. Set the 5328A FREQUENCY RESOLUTION, N control to 10 KHz 10^2. From the CW position, adjust Channel A and B trigger LEVELS CCW until just past the point where both triggering LEDs blink.

NOTE

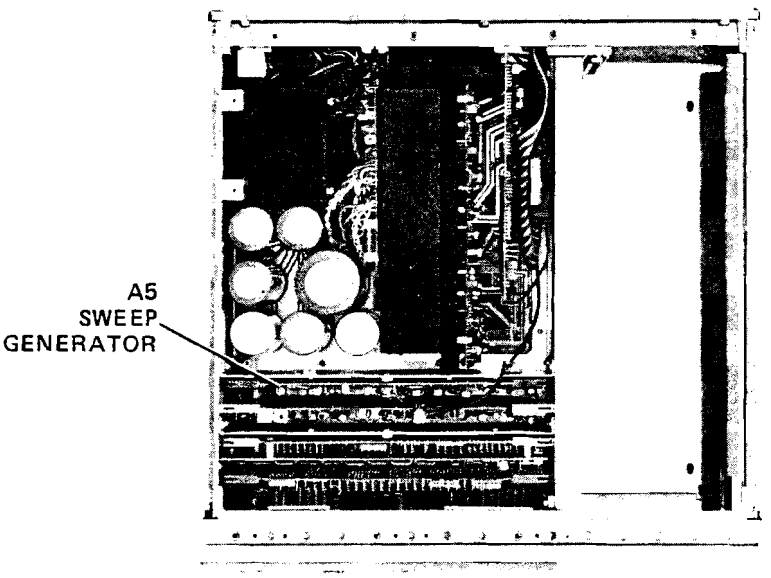
The setting of the 5328A triggering controls is critical for an accurate time interval measurement.

7. Adjust A5R2 10 mSEC ADJ for a counter reading of 10.000 ± 0.020 ms. Refer to Figure 5-9 for location of adjustment.

8. Press INSTR PRESET SWEEP TIME 1 s .

9. Adjust A5R25 1 SEC ADJ for a counter reading of 1000 ± 5 ms. Refer to Figure 5-9 for location of adjustment.

5-15. SWEEP TIME ADJUSTMENTS (Cont'd)



A5

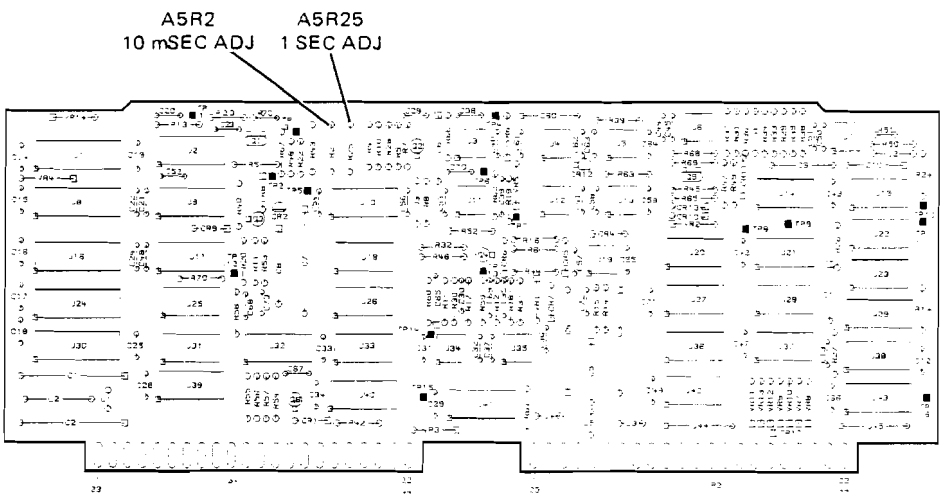


Figure 5-9. Location of Sweep Time Adjustments.

5-16. MANUAL SWEEP ADJUSTMENT

REFERENCE:

A4 Scaling and Marker
A5 Sweep Generator

DESCRIPTION:

A5R43 MANUAL sweep adjust sets the gain of sweep ramp generator output amplifier A5U3 (when operating in a linear mode during MANUAL SWEEP). The adjustment is made with the A5 Sweep Generator sweep ramp DAC A5U2 at the high end of its range so that the upper limit of the manual sweep voltage is the same as the +10V clamped level which limits normal sweeps. The output is monitored at A4TP11 (VTUNE) which is the point at which the reference sweep voltage is sent to the RF plug-in.

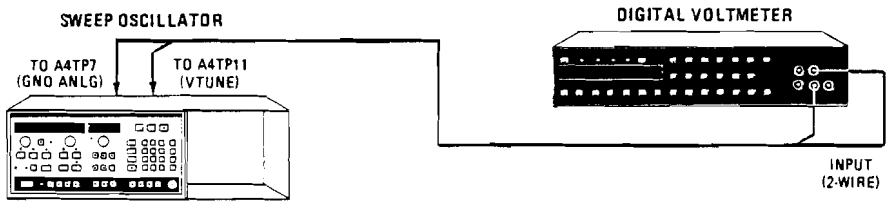


Figure 5-10. Manual Sweep Adjustment Setup.

EQUIPMENT:

Sweep Oscillator	HP 8350A
Digital Voltmeter (DVM)	HP 3455A

PROCEDURE:

1. Remove the RF plug-in from the sweep oscillator mainframe.
2. Set the LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.
3. Position the sweep oscillator upright as shown in Figure 5-10 and remove the top cover.

NOTE

The validity of this adjustment procedure is based in part on the accuracy of the sweep time adjustments. Proper adjustment of the forward sweep times is necessary before proceeding with this adjustment procedure.

4. Connect the DVM to A4TP11 (VTUNE) and A4TP7 (GND ANLG).
5. Press INSTR PRESET.
6. Press SHIFT 0 0 M1 2 0 1 6 M2 GHz 9. The FREQUENCY/TIME display should indicate C9. This sets the control line outputs from A5U8 to the A5 Sweep Generator circuits for a manual sweep condition.

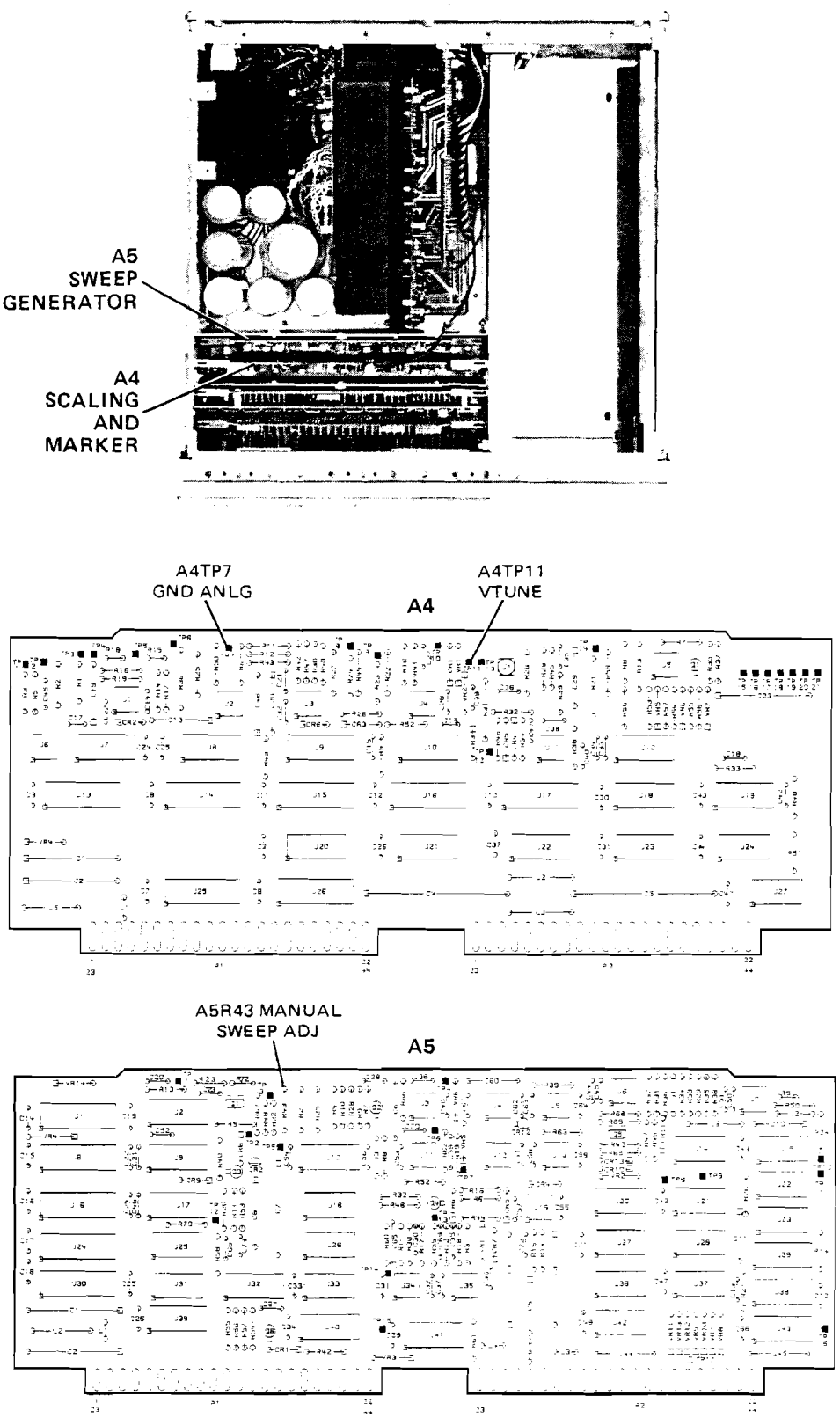


Figure 5-11. Location of Manual Sweep Adjustment.

5-16. MANUAL SWEEP ADJUSTMENT (Cont'd)

7. Press M1 2 0 1 7 M2 BK SP dBm. The FREQUENCY/TIME display should indicate FE. This sets the sweep ramp generator DAC A5U2 to 4 bits below its maximum level.

8. Adjust A5R43 MANUAL adjust until the voltage clamps at the upper limit. The adjustment is correctly set at the point just when the voltage clamps at the maximum level (typically about +10 Vdc). Refer to Figure 5-11 for location of manual sweep adjustment.

5-17. SWEEP RETRACE TIME ADJUSTMENTS

REFERENCE:

A5 Sweep Generator

DESCRIPTION:

The integrating capacators, which are used to generate the sweep ramp on the A5 Sweep Generator, discharge through A5R70* and A5R20 during sweep retrace. By monitoring forward sweep time plus retrace time at the rear panel POS Z BLANK BNC output (high=sweep retrace, low=forward sweep) with a time interval counter, A5R70* is selected during a 10 ms sweep to give a total sweep plus retrace time of 15.85 ±0.20 ms. This insures that the sweep oscillator will trigger on the line frequency repetitively.

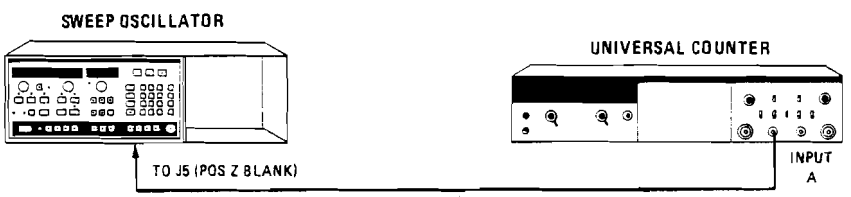


Figure 5-12. Sweep Retrace Time Adjustments Setup.

EQUIPMENT:

Sweep Oscillator	HP 8350A
Universal Counter	HP 5328A

PROCEDURE:

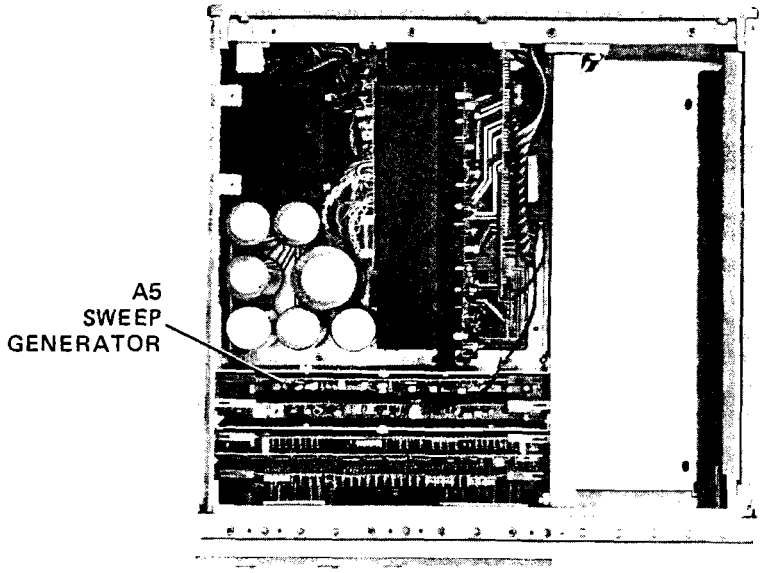
1. Remove the RF plug-in from the sweep oscillator mainframe.

2. Set the 8350A LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.

NOTE

The validity of this adjustment procedure is based in part on the accuracy of the sweep time adjustments. Proper adjustment of the forward sweep times is necessary before proceeding with this adjustment procedure.

5-17. SWEEP RETRACE TIME ADJUSTMENTS (Cont'd)



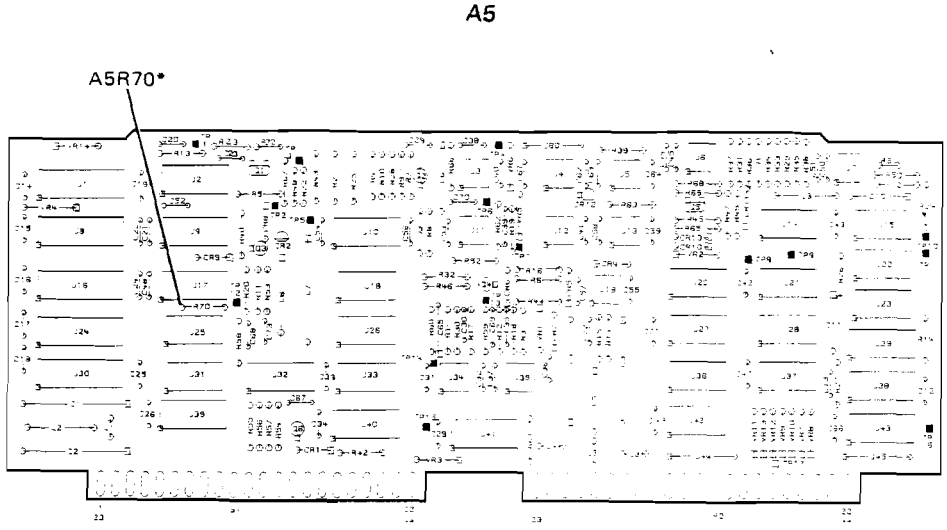


Figure 5-13. Location of Sweep Retrace Time Adjustments.

5-17. SWEEP RETRACE TIME ADJUSTMENTS (Cont'd)

3. Connect the POS Z BLANK BNC output connector on the rear panel of the 8350A to the INPUT A connector on the 5328A Universal Counter and set the 5328A controls as follows:

FUNCTION	PER A
SAMPLE RATE	CCW
OSC (rear panel)	INT
ARM ON/OFF (rear panel)	OFF
STORAGE ON/OFF (rear panel)	ON
POWER	ON
Input Amplifier Control Switch	SEP
Channel A SLOPE	−
Channel A Coupling	DC
Channel A ATTEN	X10
Channel A Trigger LEVEL A	CW

4. Position the sweep oscillator upright as shown in Figure 5-12.

5. Press INSTR PRESET SWEEP TRIGGER INT SWEEP TIME 1 0 ms.

6. Set the 5328A FREQUENCY RESOLUTION, N control to 10 KHz 10^2. Adjust Channel A trigger LEVEL until the Channel A triggering LED blinks.

7. A5R70* is selected to give a counter reading of 15.85 ±0.20 ms. Refer to Table 5-2 for the range of values allowable for A5R70*. Refer to Figure 5-13 for A5R70* component location.

NOTE

Decreasing A5R70* to the next lower recommended value shown in Table 5-3 will decrease the sweep retrace time by approximately 0.15 ms. Inversely, increasing A5R70* to the next higher recommended value will increase the sweep retrace time by approximately 0.15 ms.

5-18. 27.8/1 kHz OSCILLATOR ADJUSTMENT

REFERENCE:

A5 Sweep Generator Assembly

DESCRIPTION:

The internal AM 27.8/1 kHz oscillator frequency is adjusted for optimum center frequency at either 27.8 kHz or 1 kHz. A jumper on the A5 Sweep Generator Assembly selects the oscillator frequency which will then be used to modulate the RF Output frequency when SQUARE WAVE MODulation is selected by the front panel ⊓⊔ key.

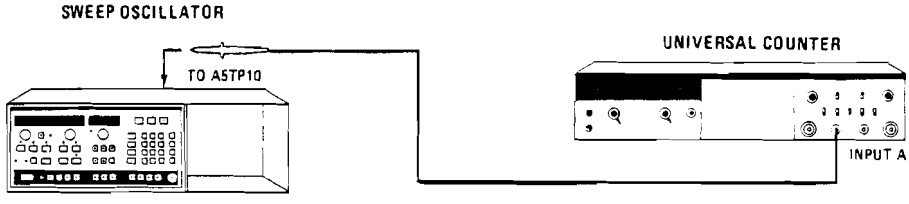


Figure 5-14. 27.8/1 kHz Oscillator Adjustment Setup.

EQUIPMENT:

Sweep Oscillator	HP 8350A
Universal Counter	HP 5328A
1:1 Probe	HP 10008B

PROCEDURE:

1. Remove the RF plug-in from the sweep oscillator mainframe.
2. Position the sweep oscillator upright as shown in Figure 5-14 and remove the top cover and the A4/A5 shield cover.
3. Set the 5328A controls as follows:

FUNCTION	FREQ A
SAMPLE RATE	CCW
OSC (rear panel)	INT
ARM ON/OFF (rear panel)	OFF
STORAGE ON/OFF	ON
POWER	ON
Input Amplifier Control Switch	SEP
Channel A SLOPE	+
Channel A Coupling	AC
Channel A ATTEN	X10
Channel A Trigger LEVEL A	CW

5-18. 27.8/1 kHz OSCILLATOR ADJUSTMENT (Cont'd)

NOTE

When SQUARE WAVE MODULATION is selected, the internal AM 27.8/1 kHz oscillator frequency will be determined by the position of the A5J2 frequency select jumper. If the oscillator has been initially calibrated for one frequency and the jumper is moved to the alternate frequency position, the oscillator must be recalibrated for the new frequency setting. Calibration for each frequency is thus independent for each jumper setting. Steps 4 through 8 adjust the oscillator for 1 kHz modulation. Steps 9 through 13 adjust the oscillator for 27.8 kHz modulation.

1kHz Oscillator Adjustment

4. Set the 8350A LINE switch to OFF, remove the A5 Sweep Generator assembly and set the frequency select jumper A5J2 to the 1kHz position. Refer to Figure 5-15 for A5J2 jumper location. Replace the A5 Sweep Generator assembly in the 8350A mainframe.

5. Connect the equipment as shown in Figure 5−15.

6. Set the 8350A LINE switch to ON and press INSTR PRESET ⌐L MOD.

7. Set the 5328A FREQUENCY RESOLUTION,N control to 1 Hz 10^6. Adjust Channel A Trigger LEVEL until the Channel A triggering LED blinks.

8. Adjust A5R51 SQUARE WAVE MODULATION FREQUENCY adjust for a counter reading of 1000 ± 10 Hz.

27.8 kHz Oscillator Adjustment

9. Set the 8350A LINE switch to OFF, remove the A5 Sweep Generator assembly and set the frequency select jumper A5J2 to the 27.8 kHz position. Refer to Figure 5-15 for A5J2 jumper location. Replace the A5 Sweep Generator in the 8350A mainframe.

10. Connect the equipment as shown in Figure 5-14.

11. Set the 8350A LINE switch to ON and press INSTR PRESET ⌐L MOD.

12. Adjust the 5328A Channel A Trigger LEVEL until the Channel A triggering LED blinks.

13. Adjust A5R51 SQUARE WAVE MODULATION FREQUENCY adjust for a counter reading of 27800 ± 100 Hz.

5-18. 27.8/1 kHz OSCILLATOR ADJUSTMENT (Cont'd)

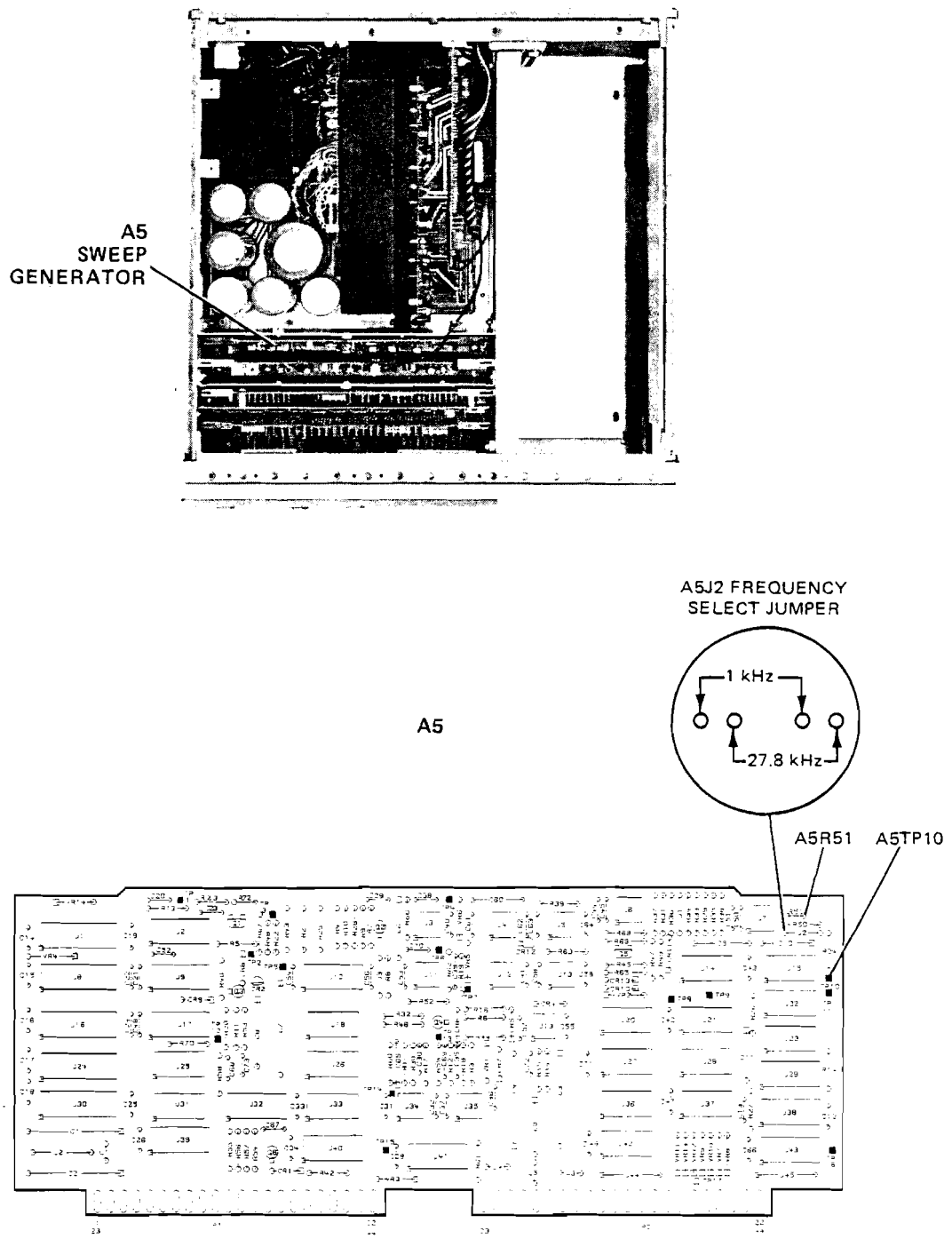


Figure 5-15. Location of 27.8/1 kHz Oscillator Adjustment.

5-19. FREQUENCY CONTROL ADJUSTMENTS

REFERENCE:

A4 Scaling and Marker Assembly

DESCRIPTION

The A4U10 VERNIER DAC is first calibrated for symmetrical frequency operation with no RF plug-in installed. With the 8350A set to −200 MHz in CW mode, A4R44 CW OFFSET is set to adjust the accuracy of the low end of the VERNIER frequency range. A4R22 VERNIER is then adjusted to set the accuracy of the high end of the VERNIER frequency range. The 8350A is then tuned to a CW frequency of 10.2 GHz and A4R27 CW is adjusted to set the CW frequency accuracy at the high end of the frequency band. The A4 ΔF Generation circuits are then adjusted for frequency accuracy on each of three ΔF frequency ranges (full-band range, 1/8-band range, and 1/64-band range in ΔF sweeps). The high and low end accuracy of the full RF plug-in band ΔF range is adjusted by A4R2 ΔF OFFSET and A4R25 ΔF1. The VERNIER then adjusts the center frequency to the exact center of the band in a 0 GHz ΔF sweep mode. At this point, the ΔF sweep range is narrowed to 1.299 GHz, just below the switch point at 1.3 GHz where the resolution scaling of the A4 ΔF Generation circuits change from full-band to < 1/8-band range. A4R15 ΔF2 is then adjusted to calibrate the resolution accuracy for ΔF sweeps in this range. The ΔF sweep range is narrowed again to 162.4 MHz, just below the switch point at 162.5 MHz where the resolution scaling of the A4 ΔF Generation circuits changes to < 1/64-band range. A4R18 ΔF3 is then adjusted to calibrate the resolution accuracy in the narrowest ΔF sweep range.

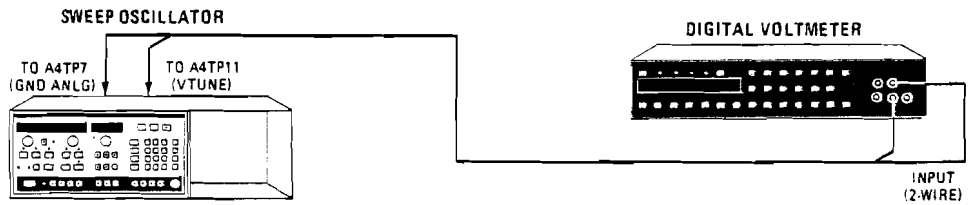


Figure 5-16. Frequency Control Adjustments Setup.

EQUIPMENT:

Sweep Oscillator	HP 8350A
Digital Voltmeter (DVM)	HP 3455A

PROCEDURE:

1. Remove the RF plug-in fron the sweep oscillator mainframe.
2. Position the sweep oscillator upright as shown in Figure 5-16 and remove the top cover.
3. Set the LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.

5-19. FREQUENCY CONTROL ADJUSTMENTS (Cont'd)

VERNIER Calibration

NOTE

The validity of this adjustment procedure is based in part on the accuracy of the +10V REF DAC power supply. Proper adjustment of the +10V REF DAC power supply is necessary before proceeding with this adjustment procedure.

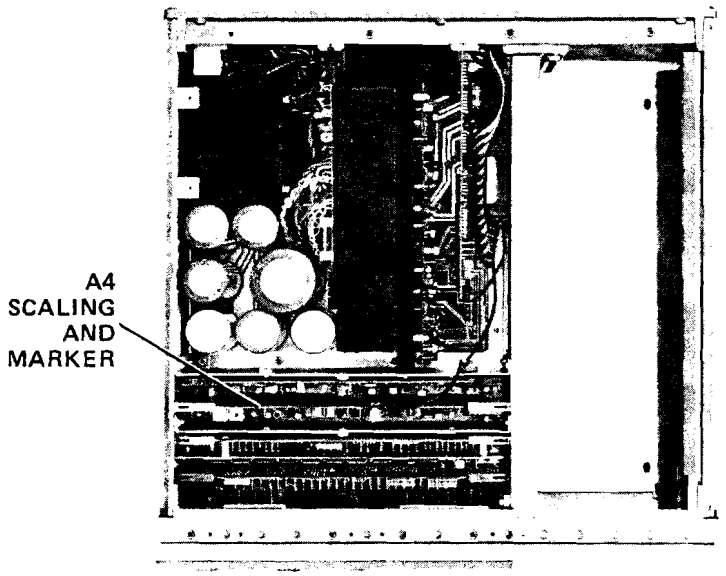
4. Connect the DVM to A4TP11 (VTUNE) and A4TP7 (GND ANLG).
5. Press INSTR PRESET CW — 2 0 0 MHz. This sets the sweep ramp circuits at the start of sweep.
6. Press SHIFT 0 0 M1 3 0 0 0 M2 0 1. The FREQUENCY/TIME display should indicate 01. This sets Digital-to-Analog Converter (DAC) A4U10 to 01H.
7. Adjust A4R44 CW OFFSET for a DVM reading of −0.20508 ± 0.00002 Vdc. Refer to Figure 5-17 for adjustment location.
8. Press BK SP BK SP. The FREQUENCY/TIME display should indicate FF. This sets A4U10 DAC to its maximum level.
9. Adjust A4R22 VERNIER for a DVM reading of −0.19492 ± 0.00002 Vdc. Refer to Figure 5-17 for adjustment location.
10. Press 8 0. The FREQUENCY/TIME display should indicate 80. This sets A4U10 DAC to midrange.
11. Check to insure that the DVM reading is −0.20000 ± 0.00002 Vdc.
12. Press INSTR PRESET CW 1 0 . 2 GHz.
13. Remove A4/A5 shield cover and adjust A4R27 CW for a DVM reading of 10.2000 ± 0.0001 Vdc. Refer to Figure 5-17 for adjustment location.

ΔF GENERATION Adjustments

NOTE

The validity of this adjustment is based in part on the accuracy of the VSW1 input from the A5 Sweep Generator assembly. Proper adjustment of the A5 Sweep Generator circuits is necessary before proceeding with this adjustment procedure.

5-19. FREQUENCY CONTROL ADJUSTMENTS (Cont'd)



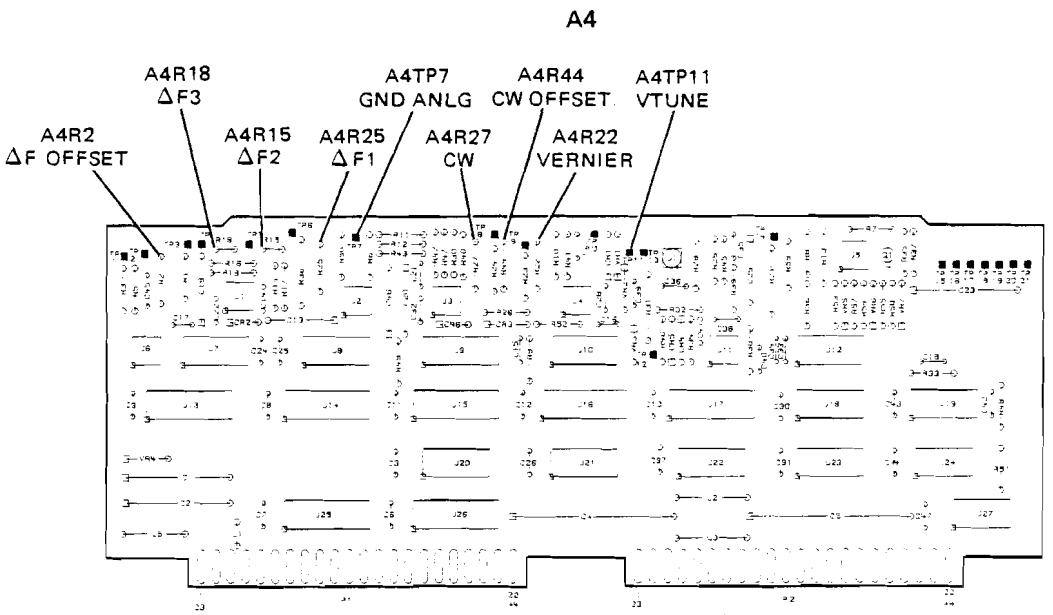


Figure 5-17. Location of Frequency Control Adjustments.

5-19. FREQUENCY CONTROL ADJUSTMENTS (Cont'd)

14. Press INSTR PRESET ΔF 1 0 . 4 GHz SWEEP MAN 1 0 . 2 GHz.

15. Adjust A4R25 ΔF1 for a DVM reading of 10.2000 ± 0.0001 Vdc. Refer to Figure 5-17 for adjustment location.

16. Press — 2 0 0 MHz.

17. Adjust A4R2 ΔF OFFSET for a DVM reading of −0.2000 ± 0.0001 Vdc. Refer to Figure 5-17 for adjustment location.

18. Press ΔF 0 GHz.

19. Check to insure the DVM reading is 5.00000 ± 0.00005 Vdc. If it is not, press VERNIER, rotate CW VERNIER until the DVM reading is 5.00000 ± 0.00005 Vdc.

20. Press ΔF 1 . 2 9 9 GHz.

21. Adjust A4R15 ΔF2 for a DVM reading of 4.35064 ± 0.00005 Vdc. Refer to Figure 5-17 for adjustment location.

22. Press ΔF 1 6 2 . 4 MHz.

23. Adjust A4R18 ΔF3 for a DVM reading of 4.91883 ± 0.00005 Vdc. Refer to Figure 5-17 for adjustment location.

5-20. MARKER DAC ADJUSTMENT

REFERENCE:

A4 Scaling and Marker Assembly

DESCRIPTION:

The 8350A is set, without an RF plug-in installed, for a stop frequency of 10 GHz with a single marker set to 10 GHz also. The rear panel POS Z BLANK BNC output (high=sweep retrace, low=forward sweep) is monitored by a time interval counter and A4R28 MKR is adjusted to set the reference voltage for marker DAC A4U12 so that the marker DAC output is calibrated to match the end of the sweep ramp.

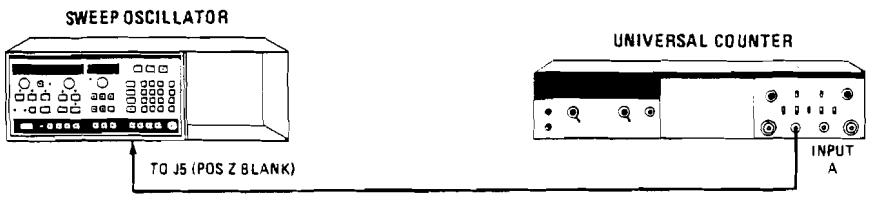


Figure 5-18. Marker DAC Adjustment Setup

EQUIPMENT:

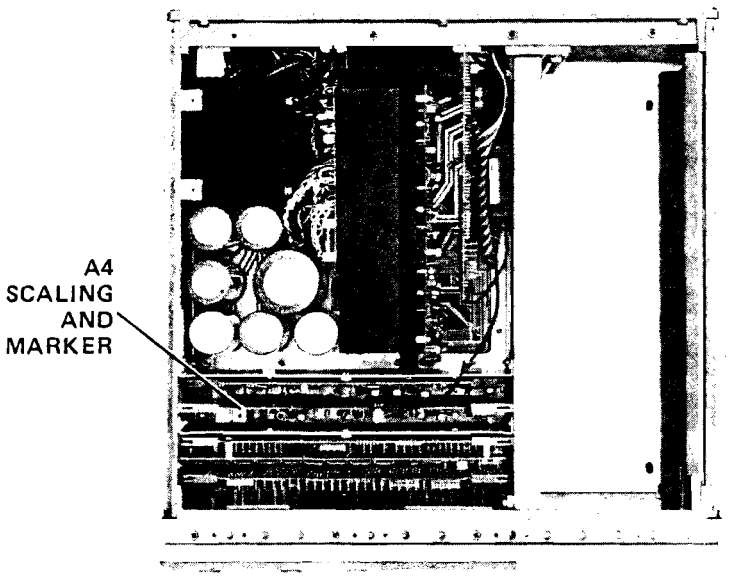
Sweep Oscillator	HP 8350A
Universal Counter	HP 5328A

PROCEDURE:

1. Remove the RF plug-in from the sweep oscillator mainframe.
2. Set the 8350A LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.
3. Connect the POS Z BLANK BNC output connector on the rear panel of the 8350A to the INPUT A connector on the 5328A Universal Counter and set the 5328A controls as follows:

FUNCTION	TI A→B
SAMPLE RATE	CCW
OSC (rear panel)	INT
ARM ON/OFF (rear panel)	OFF
STORAGE ON/OFF (rear panel)	ON
POWER	ON
Input Amplifier Control Switch	COM A
Channel A SLOPE	−
Channel A Coupling	DC
Channel A ATTEN	X10
Channel A Trigger LEVEL A	CCW
Channel B SLOPE	+

5-20. MARKER DAC ADJUSTMENT (Cont'd)



A4

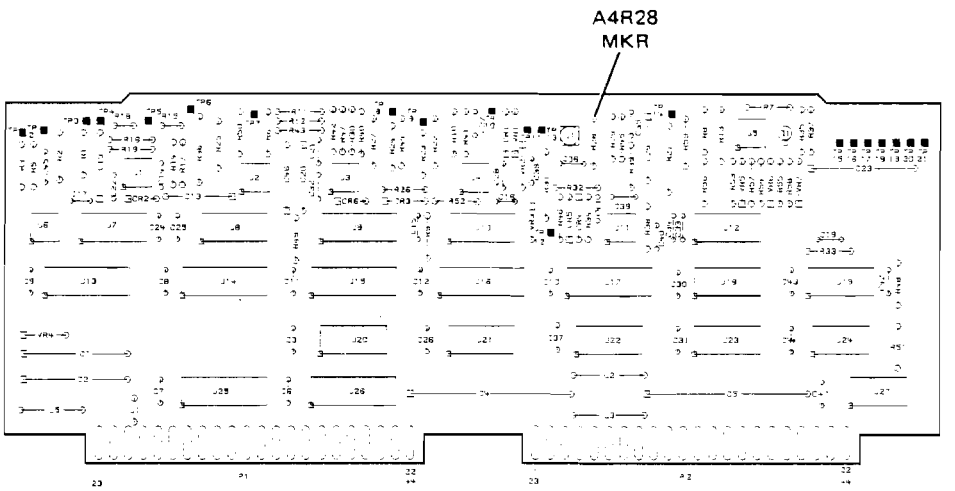


Figure 5-19. Location of Marker DAC Adjustment

5-20. MARKER DAC ADJUSTMENT (Cont'd)

Channel B Coupling ..... DC
Channel B ATTEN X10
Channel B Trigger LEVEL B ..... CCW

4. Position the sweep oscillator upright as shown in Figure 5-18 and remove the top cover.

5. Press INSTR PRESET STOP 1 0 GHz MI 1 0 GHz SWEEP TIME 1 s. This sets marker M1 at the STOP frequency of 10 GHz.

6. Preset A4R28 MKR fully clockwise to insure that a marker will occur before the end of the sweep ramp is reached.

7. Set the 5328A FREQUENCY RESOLUTION, N control to 0.1 MHz 10. From the CCW position, adjust Channel A and B trigger LEVELS CW until just past the point where both triggering LEDs blink. This should typically occur at the 10 o'clock position on both trigger LEVEL controls. The counter should now read approximately 4000 us.

NOTE

The setting of the 5328A triggering controls is critical for an accurate time interval measurement.

8. Adjust A4R28 MKR counterclockwise for a counter reading of 500 ± 100 us. This sets the width of the −8 volt marker pulse as shown in Figure 5-20. Refer to Figure 5-19 for adjustment location.

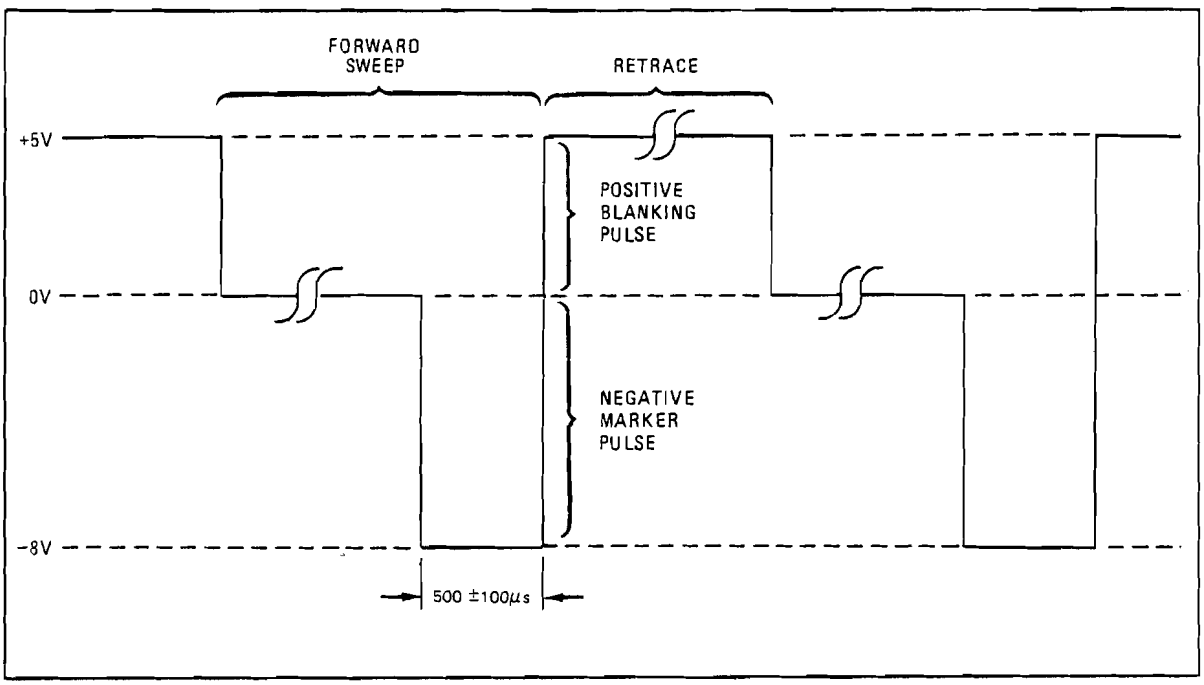


Figure 5-20. Marker DAC Adjustment Waveform

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list, reference designator definitions, and the manufacturer's code list. Table 6-2 lists replaceable parts in reference designator order.

6-3. REPLACEABLE PARTS LIST

6-4. Table 6-2 is the list of replaceable parts and is organized as follows:

1. Electrical assemblies and their components in alpha-numerical order by reference designation.
2. Miscellaneous parts, at the end of the list for each major assembly.
3. Chassis-mounted parts, in alphanumerical order by reference designation, at the end of the parts list.
4. Illustrated parts locations.

6-5. The information given for each part consists of the following:

1. The Hewlett-Packard part number.
2. Part number check digit (CD).
3. The total quantity (Qty) in the instrument. This quantity is given only once, at the first appearance of the part in the list.
4. The description of the part.
5. A typical manufacturer of the part in a five-digit code.
6. The manufacturer part number.

6-9. ORDERING INFORMATION

6-10. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

6-11. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

Table 6-1. Reference Designations, Abbreviations, and Code List of Manufacturers (1 of 3)

REFERENCE DESIGNATIONS

A . . . . . assembly
AT . . attenuator; isolator; termination
B . . . . . fan; motor
BT . . . . . battery
C . . . . . capacitor
CP . . . . . coupler
CR . . . . . diode; diode thyristor; varactor
DC . . . directional coupler
DL . . . . . delay line
DS . . . . . annunciator; signaling device (audible or visual); lamp; LED
E . . . . . miscellaneous electrical part
F . . . . . fuse
FL . . . . . filter
H . . . . . hardware
HY . . . . . circulator
J . . . electrical connector (stationary portion); jack
K . . . . . relay
L . . . . . coil; inductor
M . . . . . meter
MP . . . . . miscellaneous mechanical part
P . . . electrical connector (movable portion); plug
Q . . . . . transistor; SCR; triode thyristor
R . . . . . resistor
RT . . . . . thermistor
S . . . . . switch
T . . . . . transformer
TB . . . . . terminal board
TC . . . . . thermocouple
TP . . . . . test point
U . . . . . integrated circuit; microcircuit
V . . . . . electron tube
VR . . . . voltage regulator; breakdown diode
W . . . . cable; transmission path; wire
X . . . . . socket
Y . . . . crystal unit (piezoelectric or quartz)
Z . . . . tuned cavity; tuned circuit

ABBREVIATIONS

A

A. . . . . Across Flats, Acrylic, Air (Dry Method), Ampere
AC. . . . . Actinium, Alternating Current, Alumina-Ceramic
ADJ. . . . . Adjust, Adjustment
AG . . . . . Silver
AL. . . . . Aluminum
AMP . . . . . Amperage
ANLG. . . . . Analog
ASSY . . . . . Assembly
AWG. . . . . American Wire Gage

B

BD . . . . . Board, Bundle
BE-CU. . . . . Beryllium Copper
BFR. . . . . Before, Buffer
BIN. . . . . Bin Box (Container), Binary
BNC. . . . . Type of Connector
BSC . . . . . Basic

C

C . . . . . Capacitance, Capacitor, Center Tapped, Centistoke, Ceramic, Cermet, Circular Mil Foot, Closed Cup, Cold, Compression
CAP . . . . . Capacitor, Capacity
CER . . . . . Ceramic
CFM. . . . . Cubic Feet Per Minute
CH . . . . . Center Hole
CNTR. . . . . Container, Counter
COM . . . . . Commercial, Common
COMPTR. . . . . Comparator
CONN . . . . . Connect, Connection, Connector
CONT. . . . . Contact, Continuous, Control, Controller
CONV . . . . . Converter

D

D. . . . . Deep, Depletion, Depth, Diameter, Direct Current
D/A. . . . . Digital–to–Analog
DC. . . . . Direct Current, Double Contact
DCDR . . . . . Decoder
DEG . . . . . Degree
DIA. . . . . Diameter
DIEL . . . . . Dielectric
DIFF. . . . . Differential
DIP. . . . . Dual In-Line Package
DO . . . . . Package Type Designation
DPDT . . . . . Double Pole Double Throw
DRVR . . . . . Driver

E

EPROM. . . . . Eraseable Programmable Read Only Memory
EXCL. . . . . Excluding, Exclusive
EXTR . . . . . Extractor

F

F. . . . . Fahrenheit, Farad, Female, Film (Resistor), Fixed, Flange, Flint, Fluorine, Frequency
FF. . . . . Flange, Female Connection; Flip Flop
FIG. . . . . Figure
FL. . . . . Flash, Flat, Fluid
FM . . . . . Flange, Male Connection; Foam, Frequency Modulation
FT. . . . . Current Gain Bandwidth Product (Transition Frequency); Feet, Foot
FXD. . . . . Fixed

G

GEN. . . . . General, Generator
GRN. . . . . Green

H

H . . . . . Henry, Hermaphrodite, High, Hole Diameter, Hot, Hub Inside Diameter, Hydrogen
HD. . . . . Hand, Hard, Head, Heavy Duty
HEX. . . . . Hexadecimal, Hexagon, Hexagonal
HLCL. . . . . Helical
HP-IB. . . . . Hewlett-Packard Interface Bus
HZ . . . . . Hertz

I

IC. . . . . Collector Current, Integrated Circuit
ID. . . . . Identification, Inside Diameter
IF . . . . . Forward Current, Intermediate Frequency
IMPD . . . . . Impedance
IN. . . . . Inch, Indium
INFO. . . . . Information
INP. . . . . Input
INT. . . . . Integral, Intensity, Internal
INV. . . . . Invert, Inverter

J

J-FET. . . . . Junction Field Effect Transistor

K

K. . . . . Kelvin, Key, Kilo, Potassium

L

LCH. . . . . Latch
LED . . . . . Light Emitting Diode
LG . . . . . Length, Long
LK. . . . . Link, Lock
LS. . . . . Loudspeaker, Low Power Schottky, Series Inductance
LUM . . . . . Luminous

M

M . . . . . Male, Maximum, Mega, Mil, Milli, Mode, Momentary, Mounting Hole Centers, Mounting Hole Diameter
MA. . . . . Milliampere
MACH . . . . . Machined
MAGTD . . . . . Magnitude

Table 6-1. Reference Designations, Abbreviations, and Code List of Manufacturers (2 of 3)

MAX ..... Maximum
MCD ..... Millicandela
MET ..... Metal, Metallic, Metallized, Metallurgical
MH ..... Medium High
MISC ..... Miscellaneous
MLD ..... Mold, Molded
MNT ..... Minute (Angle)
MONO/ASTBL ..... Monostable / Astable
MONOSTBL ..... Monostable
MTLC ..... Metallic
MUXR ..... Multiplexer
MV ..... Millivolt, Multivibrator
MW ..... Milliwatt

N

N ..... Fan Out, Intrinsic Stand Off Ratio, Nano, Nanosecond, Nitrogen, None
NAND ..... Logic Not-AND
NEG ..... Negative
NM ..... Nanometer, Nonmetallic
NMOS ..... N-Channel Metal Oxide Semiconductor
NO ..... Normally Open, Number
NPN ..... Negative Positive Negative (Transistor)
NS ..... Nanosecond, Non-Shorting, Nose

O

OCTL ..... Octal
OP ..... Operational
OPN ..... Open, Operation
OPT ..... Optical, Option, Optional
OR ..... Logic OR, Output Register
ORN ..... Orange

P

P ..... Peak, Phosphorus, Pico, Picosecond, Pitch, Plastic, Plug, Pole, Polyester, Power, Probe, Pure
PC ..... Picocoulomb, Piece, Printed Circuit
PCB ..... Printed Circuit Board
PD ..... Pad, Palladium, Pitch Diameter, Power Dissipation
PF ..... Picofarad; Pipe, Female Connection; Power Factor
PNP ..... Positive Negative Positive (Transistor)
P/O ..... Part Of
POLYC ..... Polycarbonate
POLYE ..... Polyester
POS ..... Position, Positive
PRCN ..... Precision
PROM ..... Programmable Read Only Memory
PRP ..... Purple, Purpose
PVC ..... Polyvinyl Chloride
PWR ..... Power
PWW ..... Precision Wirewound

Q

QUAD ..... Set of Four

R

R ..... Range, Red, Resistance, Resistor, Right, Ring, Rosin, Rubber-Resin, Run Torque
RAM ..... Random Access Memory
RCPT ..... Receptacle
RCVR ..... Receiver
RECT ..... Rectangle, Rectangular, Rectifier
REG ..... Register, Regular, Regulated, Regulation, Regulator
RES ..... Research, Resistance, Resistor, Resolution
RETRIG ..... Retriggerable
RF ..... Radio Frequency
RGLTR ..... Regulator
RKR ..... Rocker
RMS ..... Root Mean Square
RND ..... Round
RPG ..... Rotary Pulse Generator

S

S ..... Saybolt Seconds Universal, Scattering Parameter, Schottky, Screw Size, Second, Shorting, Side, Siemens, Silicone, Silk (Insulation), Soft, Solid, Square Mil Foot, Standard Threaded, Start Torque, Stearine, Steel, Strut Center Spacing, Stud Size, Sulfur
SCR ..... Screw, Scrub, Silicon Controlled Rectifier
SEL ..... Select, Selected
SGL ..... Single
SHLDR ..... Shoulder
SI ..... Silicon, Square Inch
SIP ..... Single In-Line Package
SKT ..... Skirt, Socket
SLDR ..... Solder
SM ..... Samarium, Seam, Small, Square Meter, Sub Modular, Sub-miniature
SNP ..... Snap
SPCL ..... Special
SPST ..... Single Pole Single Throw
SQ ..... Square
STAT ..... Status
STRP ..... Strapped, Strip
SUBMIN ..... Subminiature
SYNCHRO ..... Synchronous
SZ ..... Size

T

T ..... Tab Width, Taper, Teeth, Temperature, Tera, Tesla, Thermoplastic (Insulation), Thickness, Time, Timed, Tooth, Turns Ratio, Typical
TA ..... Ambient Temperature, Tantalum
TBAX ..... Tube Axial
TC ..... Thermoplastic
THD ..... Thread, Threaded
THERM ..... Thermometer
THK ..... Thick
THKNS ..... Thickness
THRD ..... Thread
TNG ..... Tongue, Training
TO ..... Package Type Designation, Troy Ounce
TPG ..... Tapping
TRIG ..... Trigger, Triggerable, Triggering, Trigonometry
TRMR ..... Trimmer
TRN ..... Turn, Turns
TTL ..... Tan Translucent, Transistor Transistor Logic

U

UCD ..... Microcandela
UF ..... Microfarad
UL ..... Microliter, Underwriters' Laboratories, Inc.

V

V ..... Vanadium, Variable, Violet, Volt, Voltage
VREG ..... Voltage Regulator
VRRM ..... Repetitive Peak Inverse Voltage

W

W ..... Watt, Wattage, White, Wide, Width, Wire

X

X ..... By (Used With Dimensions), Reactance

Y

YEL ..... Yellow

Z

Z ..... Impedance
ZNR ..... Zener

Table 6-1. Reference Designations, Abbreviations, and Code List of Manufacturers (3 of 3)

CODE LIST OF MANUFACTURERS

Mfr. No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
00853	SANGAMO ELEC CO S CAROLINA DIV	PICKENS	SC	29671
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
02768	ILLINOIS TOOL WORKS INC FASTEX DIV	DES PLAINES	IL	60016
03296	NYLON MOLDING CORP	SPRINGFIELD	NJ	07081
03888	KDI PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
05245	CORCOM INC	CHICAGO	IL	60657
06001	MEPCO ELECTRA CORP	IRMO	SC	29063
06540	AMATOM ELEK HARDWARE DIV OF MITE	NEW ROCHELLE	NY	06515
06665	PRECISION MONOLITHICS INC	SANTA CLARA	CA	95050
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
09353	C AND K COMPONENTS INC	WATERTOWN	MA	02172
0G791	THOMPSON BREMER DIV VARE	CHICAGO	IL	60622
11236	CTS OF BERNE INC	BERNE	IN	46711
12697	CLAROSTAT MFG CO INC	DOVER	NH	03820
17856	SILICONIX INC	SANTA CLARA	CA	95054
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
20932	EMCON DIV ITW	SAN DIEGO	CA	92129
20940	MICRO-OHM CORP	EL MONTE	CA	91731
22526	BERG ELECTRONIC INC	CUMBERLAND	PA	17070
24046	TRANSITRON ELECTRONIC CORP	WAFEFIELD	MA	01880
24355	ANALOG DEVICES INC	NORWOOD	MA	02062
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
24931	SPECIALTY CONNECTOR CO INC	GREENWOOD	IN	46227
25088	SIEMENS CORP	ISELIN	NJ	08830
27014	NATIONAL SEMICONDUCCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
4N833	ETRI INC	MONROE	NC	60521
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
71400	BUSSMAN MFG DIV OF MCGRAW-EDISON CO	ST LOUIS	MO	63107
71785	TRW ELEK COMPONENTS CINCH DIV	ELK GROVE VLGE	IL	60007
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIAMANTIC	CT	06226
72962	ELASTIC STOP NUT DIV OF AMPERACE	UNION	NJ	07083
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108
75915	LITTELFUSE INC	DES PLAINES	IL	60016
76530	TRW ELEK CMPNT CINCH-MONADNOCK DIV	CITY OF IND	CA	91747
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF	ELGIN	IL	60126
79963	ZIERICK MFG CO	MT KISCO	NY	10549
80103	LAMBDA ELECCTRONICS CORP	MELVILLE	NY	11746
82647	TEXAS INST DEPT CONTROL PROD DIV	ATTLEBORO	MA	02703
84411	TRW CAPACITOR DIV	OGALLALA	NE	69153
91506	AUGAT INC	ATTLEBORO	MA	02703
92702	IMC MAGNETICS CORP EASTERN DIV	LONG ISLAND	NJ	11591
92895	AMERICAN OIL & SUPPLY CO	NEWARK	NJ	07105
95987	WECKESSER CO INC	CHICAGO	IL	60641
C0633	RIFA	BROMMA	SE	

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	08350-60021	6	1	BOARD ASSEMBLY-FRONT PANEL NOTE: FRONT PANEL KEY CAPS ARE INCLUDED IN HP PART NO. 08350-60021. FOR THE INDIVIDUAL PART NUMBERS SEE FIG. 6-1, FRONT PANEL, PARTS LOCATION.	28480	08350-60021
A1C1	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A1C2	0180-2207	5	11	CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A1C3	0160-2055	9	153	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1D81	1990-0582	3	7	LED-VISIBLE LUM-INT=3MCD IF=60MA-MAX	28480	5082-4160
A1D82	1990-0582	3		LED-VISIBLE LUM-INT=3MCD IF=60MA-MAX	28480	5082-4160
A1D83	1990-0582	3		LED-VISIBLE LUM-INT=3MCD IF=60MA-MAX	28480	5082-4160
A1D84	1990-0582	3		LED-VISIBLE LUM-INT=3MCD IF=60MA-MAX	28480	5082-4160
A1D85	1990-0582	3		LED-VISIBLE LUM-INT=3MCD IF=60MA-MAX	28480	5082-4160
A1D86	1990-0582	3		LED-VISIBLE LUM-INT=3MCD IF=60MA-MAX	28480	5082-4160
A1D87	1990-0582	3		LED-VISIBLE LUM-INT=3MCD IF=60MA-MAX	28480	5082-4160
A1D88	1990-0487	7	30	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D89	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D810	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D811	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D812	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D813	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D814	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D815	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D816	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D817	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D818	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D819	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D820	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D821	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D822	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D823	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D824	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D825	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D826	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D827	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D828	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D829	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D830	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D831	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D832	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D833	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D834	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D835	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D836	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1D837	1990-0487	7		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4584
A1J1	1251-4053	5	2	CONNECTOR 34-PIN M POST TYPE	28480	1251-4053
A1J2	1251-4827	1	2	CONNECTOR 50-PIN M POST TYPE	28480	1251-4827
A1L1	08503-80001	9	12	COIL-TOROID	28480	08503-80001
A1L2	08503-80001	9		COIL-TOROID	28480	08503-80001
A1Q1	1853-0281	9	13	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1Q2	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1Q3	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1Q4	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1Q5	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1Q6	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1Q7	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1Q8	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A1R1	0757-0180	2	9	RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1R2	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1R3	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1R4	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1R5	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1R6	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1R7	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1R8	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A1S1	5060-9436	7	50	PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S2	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S3	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S4	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S5	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1S6	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S7	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S8	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S9	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S10	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S11	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S12	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S13	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S14	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S15	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S16	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S17	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S18	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S19	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S20	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S21	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S22	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S23	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S24	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S25	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S26	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S27	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S28	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S29	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S30	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S31	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S32	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S33	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S34	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S35	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S36	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S37	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S38	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S39	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S40	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S41	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S42	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S43	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S44	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S45	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S46	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S47	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S48	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S49	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1S50	5060-9436	7		PUSHBUTTON SWITCH P.C. MOUNT	28480	5060-9436
A1U1	1820-2266	5	2	IC DRVR TTL	18324	NE590F
A1U2	1820-2266	5		IC DRVR TTL	18324	NE590F
A1VR1	1902-0551	1	6	DIODE-ZNR 6.19V 5% DO-15 PD=1W TC=+.022%	28480	1902-0551
A1XA1	1200-0846	9	3	SOCKET-STRP 15-CONT DIP-SLDR	28480	1200-0846
A1XA2	1200-0846	9		SOCKET-STRP 15-CONT DIP-SLDR	28480	1200-0846
A1XA3	1200-0846	9		SOCKET-STRP 15-CONT DIP-SLDR	28480	1200-0846
A1XU1	1200-0507	9	2	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
A1XU2	1200-0507	9		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0507
				A1 MISCELLANEOUS PARTS		
	0380-1233	9	11	LED-SPACER	00000	ORDER BY DESCRIPTION
	1450-0588	5	3	LIGHT-HOUSING	28480	1450-0588
	0360-0031	1	2	TERMINAL-CRIMP R-TNG #6 22-16-AWG RED	28480	0360-0031
	5060-9444	7	3	ROTARY-PULSE GENERATOR	28480	5060-9444
				*NOTE: RPGS AND ASSOCIATED HARDWARE MUST BE ORDERED SEPARATELY. NOT INCLUDED WITH THE A1 BOARD. FOR PART NUMBERS AND ASSEMBLY DRAWING SEE FIG. 6-3, RPG PARTS LOCATION.		
A2	08350-60022	7	1	BOARD ASSEMBLY - FRONT PANEL INTERFACE	28480	08350-60022
A2C1	0160-3456	6	11	CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A2C2	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A2C3	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A2C4-A2C13	0160-2055	9		CAPACITOR-FXD .01UF+80-20% 100VDC CER	28480	0160-2055
A2C14	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A2C15	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2C16	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	1500107X9010R2
A2C17	0160-4084	8	7	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A2C18	0160-3879	7	6	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C20	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C21	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C22	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C23	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2J1				NOT ASSIGNED		
A2J2				NOT ASSIGNED		
A2J3	1251-4053	5		CONNECTOR 34-PIN M POST TYPE	28480	1251-4053
A2J4	1251-4827	1		CONNECTOR 50-PIN M POST TYPE	28480	1251-4827
A2L1	08503-80001	9		COIL-TOROID	28480	08503-80001
A2L2	08503-80001	9		COIL-TOROID	28480	08503-80001
A2Q1	1854-0477	7	14	TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A2Q2	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A2Q3	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A2Q4	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A2Q5	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A2Q6	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A2R1	0757-0442	9	34	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R2	0757-0200	7	2	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A2R3	0698-4037	0	3	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A2R4	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A2R5	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
A2S1	3101-2243	6	3	SWITCH-DIP	28480	3101-2243
A2S2	3101-2243	6		SWITCH-DIP	28480	3101-2243
A2TP1	0360-0535	0	119	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP13	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP14	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP15	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP16	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP17	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP18	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP19	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP20	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP21	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP22	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP23	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP24	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP25	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP26	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2U1	1810-0206	8	3	NETWORK-RES 8-SIP10.0K OHM X 7	01121	208A103
A2U2	1820-1416	5	9	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A2U3	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U4	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U5	1820-1989	7	6	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A2U6	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A2U7	1820-1759	9	4	IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A2U8	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A2U9	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A2U10	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A2U11	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A2U12	1820-1759	9		IC BFR TTL LS NON-INV OCTL	27014	DM81LS97N
A2U13	1820-1730	6	18	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U14	1810-0280	8	5	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A2U15	1820-1873	8	1	IC BFR TTL LS INV OCTL 2-INP	27014	DM81LS96N
A2U16	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U17	1820-1197	9	9	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A2U18	1810-0332	1	1	NETWORK-RES 8-SIP680.0 OHM X 7	01121	208A681
A2U19	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A2U20	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2U21	1906-0092	3	1	DIODE-ARRAY 25V 400MA	28480	1906-0092
A2U22	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U23	1820-1216	3	7	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A2U24	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U25	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U26	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U27	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U28	1820-1417	6	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS26N
A2U29	1810-0247	7	1	NETWORK-RES 16-DIP220.0 OHM X 8	01121	3168221
A2U30	1810-0265	9	1	NETWORK-RES 16-DIP680.0 OHM X 8	01121	3168681
A2U31	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A2U32	1810-0283	1	4	NETWORK-RES 16-DIP270.0 OHM X 8	28480	1810-0283
A2U33	1810-0283	1		NETWORK-RES 16-DIP270.0 OHM X 8	28480	1810-0283
A2U34	1810-0283	1		NETWORK-RES 16-DIP270.0 OHM X 8	28480	1810-0283
A2U35	1810-0283	1		NETWORK-RES 16-DIP270.0 OHM X 8	28480	1810-0283
A2U36	1810-0204	6	1	NETWORK-RES 8-SIP1.0K OHM X 7	01121	208A102
A2VR1	1902-0041	4	10	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A2VR2	1902-0551	1		DIODE-ZNR 6.19V 5% DO-15 PD=1W TC=+.022%	28480	1902-0551
				A2 MISCELLANEOUS PARTS		
	4040-0750	7	2	EXTR-PC BD RED POLYC .062-BD-THKNS	28480	4040-0750
	1480-0073	6	10	PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU	28480	1480-0073
A3	08350-60038	5	1	BOARD ASSEMBLY-MICROPROCESSOR	28480	08350-60038
A3	08350-60036	3	1	BOARD ASSEMBLY-MICROPROCESSOR(OPT 001)	28480	08350-60036
A3C1	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A3C2	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A3C3	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C5	0160-2308	5	2	CAPACITOR-FXD 36PF +-5% 300VDC MICA	28480	0160-2308
A3C6	0160-2308	5		CAPACITOR-FXD 36PF +-5% 300VDC MICA	28480	0160-2308
A3C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C10	0140-0192	9	4	CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A3C11	0140-0192	9		CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A3C12	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A3C13	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A3C14	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A3C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C30	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A3C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C37	0140-0192	9		CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A3C38	0140-0192	9		CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A3CR1	1901-0050	3	12	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A3D81	1990-0486	6	4	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A3D82	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A3D83	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A3D84	1990-0486	6		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
A3J1	1251-6135	8	1	CONNECTOR 11-PIN M POST TYPE	28480	1251-6135
A3J2				NOT ASSIGNED		
A3J3	1251-5618	0	1	CONNECTOR 8-PIN M POST TYPE	28480	1251-5618
A3J4	1251-5041	3	1	CONNECTOR 5-PIN M POST TYPE	22526	65500-105
A3J5	1200-0893	6	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0893

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3L1	08503-60001	9		COIL-TOROID	28480	08503-60001
A3Q1	1853-0405	9	2	TRANSISTOR PNP SI TO-18 PD=300MW	04713	2N4209
A3Q2	1853-0405	9		TRANSISTOR PNP SI TO-18 PD=300MW	04713	2N4209
A3Q3	1854-0019	3	2	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
A3Q4	1854-0019	3		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
A3Q5	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A3Q6	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
A3Q7	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A3R1	0757-0416	7	9	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3R2	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3R3	0698-3155	1	4	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R4	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A3R5	0757-0280	3	13	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R6	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R7	0698-3430	5	4	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A3R8	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A3R9	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A3R10	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A3R11	0757-0401	0	11	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R12	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R15	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3R16	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R17	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A3R18	0698-3437	2	2	RESISTOR 133 1% .125W F TC=0+-100	24546	C4-1/8-T0-133R-F
A3R19	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A3R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R21	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R24-A3R53				NOT ASSIGNED		
A3R54	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R55	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3S1	3101-2243	6		SWITCH-RKR DIP-RKR-4S8Y 8-1A .05A 30VDC	28480	3101-2243
A3TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP13	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP14	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP15	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP16	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP17	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP18	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP19	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP20	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP21	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP22	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP23	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP24	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP25	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP26	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP27	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP28	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP29	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP30	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP31	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP32	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3U1	1810-0203	5	1	NETWORK-RES 8-SIP470.0 OHM X 7	01121	208A471
A3U2	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A3U3	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U4	1820-1425	6	2	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A3U5	1820-2358	6	1		28480	1820-2358
A3U6	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3U7	1818-0562	5	4	IC NMOS 4K RAM STAT 300-NS 3-S	34649	P2114A-5
A3U8	1818-0562	5		IC NMOS 4K RAM STAT 300-NS 3-S	34649	P2114A-5
A3U9				NOT ASSIGNED		
A3U10				NOT ASSIGNED		

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U11				NOT ASSIGNED		
A3U12	08350-60002	5	1	PROM-CLOCK GENERATOR	28480	08350-60002
A3U13	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3U14	1818-0562	5		IC NMOS 4K RAM STAT 300-NS 3-S	34649	P2114A-5
A3U15	1818-0562	5		IC NMOS 4K RAM STAT 300-NS 3-S	34649	P2114A-5
A3U16	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U17	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U18	1820-1199	1	5	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U19	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A3U20	1820-1917	1	6	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U21	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U22	1820-2075	4	4	IC MISC TTL LS	01295	SN74LS245N
A3U23	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U24	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U25	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A3U26	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U27	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U28	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3U29	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U30	1810-0338	7	6	NETWORK-RES 16-DIP100.0 OHM X 8	11236	761-3-R100
A3U31	1810-0338	7		NETWORK-RES 16-DIP100.0 OHM X 8	11236	761-3-R100
A3U32	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U33	1810-0338	7		NETWORK-RES 16-DIP100.0 OHM X 8	11236	761-3-R100
A3U34	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A3U35				NOT ASSIGNED		
A3VR1	1902-0551	1		DIODE-ZNR 6.19V 5% DO-15 PD=1W TC=+.022%	28480	1902-0551
A3W1	1460-1489	8	1	WIREFORM SE CU AG (OPTION 001 ONLY)	28480	1460-1489
A3XU11	1200-0892	5	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0892
A3Y1	0410-0787	1	1	CRYSTAL-QUARTZ	28480	0410-0787
				A3 MISCELLANEOUS PARTS		
	4040-0751	8	2	EXTR-PC SO ORN POLYC .062-SQ-THKNS	28480	4040-0751
	1480-0073	6		PIN-ROLL .062-IN-DIA .25-IN-LG SE-CU	28480	1480-0073
A3A1	08350-60030	7	1	BOARD ASSEMBLY-PROM	28480	08350-60030
A3A1C1	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3A1C2	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A3A1C3	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A3A1C4	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A3A1C5	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A3A1C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3A1CR1	1901-0200	5	1	DIODE-PWR RECT 100V 1.5A	28480	1901-0200
A3A1E1	8159-0005	0	3	WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
A3A1L1	08503-80001	9		COIL-TOROID	28480	08503-80001
A3A1R1	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3A1R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3A1R3	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3A1R4	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3A1R5	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A3A1TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3A1TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3A1TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3A1TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3A1TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3A1TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3A1TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3A1U1	1818-0498	6	18	IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U2	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U3	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U4	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U5	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U6	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U7	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U8	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U9	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U10	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U11	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U12	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U13	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U14	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U15	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U16	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U17	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U18	1818-0498	6		IC NMOS 16384-BIT EPROM 450-NS 3-S	01295	TMS2516JL
A3A1U19	1820-2024	3	6	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3A1U20	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3A1U21	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A3A1U22	1810-0338	7		NETWORK-RES 16-DIP100,0 OHM X 8	11236	761-3-R100
A3A1U23	1820-1211	8	5	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A3A1U24	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A3A1U25	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A3A1U26	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A3A1U27	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A3A1U28	1820-1281	2	3	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3A1U29	1820-1281	2		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3A1U30	1820-1281	2		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3A1U31	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74L800N
A3A1U32	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74L330N
A3A1W1	08350-60012	5	1	CABLE ASSEMBLY-26C	28480	08350-60012
A3A1W2	08350-60011	4	1	CABLE ASSEMBLY-14C	28480	08350-60011
A4	08350-60024	9	1	BOARD ASSEMBLY-SCALING & MARKER	28480	08350-60024
A4C1	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A4C2	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A4C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C4	0180-2144	9	2	CAPACITOR-FXD 200UF+75-10% 25VDC AL	56289	30D207G025DH9
A4C5	0180-2144	9		CAPACITOR-FXD 200UF+75-10% 25VDC AL	56289	30D207G025DH9
A4C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C13	0180-0100	3	3	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X903582
A4C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C15	0160-3454	4	5	CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3454
A4C16	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A4C17	0160-4084	8		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-4084
A4C18	0160-3455	5	2	CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3455
A4C19	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X903582
A4C20	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X903582
A4C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C22	0160-3454	4		CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3454
A4C23	0180-2208	6	1	CAPACITOR-FXD 220UF+-10% 10VDC TA	56289	150D227X901082
A4C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C27	0160-3455	5		CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3455
A4C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C29	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
A4C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C36	0160-4299	7	8	CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M822-CDH
A4C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4C41	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A4C42	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A4C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C45	0160-3454	4		CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3454
A4C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A4C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4CR1	1901-0033	2	15	DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A4CR2	1901-0535	9	2	DIODE-SCHOTTKY	28480	1901-0535
A4CR3	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A4CR4	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A4CR5	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A4CR6	1901-0535	9		DIODE-SCHOTTKY	28480	1901-0535
A4J1	1250-0543	8	1	CONNECTOR-RF SM-BNP M PC 50-OHM	28480	1250-0543
A4L1	08503-80001	9		COIL-TOROID	28480	08503-80001
A4L2	9100-1654	5	2	INDUCTORRF-CH-MLD 1.1MH 5% .23DX.57LG	28480	9100-1654
A4L3	9100-1654	5		INDUCTORRF-CH-MLD 1.1MH 5% .23DX.57LG	28480	9100-1654
A4L4				NOT ASSIGNED		
A4L5	9100-1642	1	1	INDUCTORRF-CH-MLD 270UH 5% .2DX.45LG	28480	9100-1642
A4Q1	1854-0557	4	1	TRANSISTOR NPN 2N2432A SI TO-18 PD=300MW	01295	2N2432A
A4R1	0811-3312	4	2	RESISTOR 10K .25% .05W PWW TC=0+-5	28480	0811-3312
A4R2	2100-3052	4	2	RESISTOR-TRMR 50 10% C SIDE-ADJ 17-TRN	02111	43P500
A4R3	0757-0438	3	8	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A4R4		4		NOT ASSIGNED		
A4R5	0811-3312	4		RESISTOR 10K .25% .05W PWW TC=0+-5	28480	0811-3312
A4R6	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A4R7	0757-0395	1	2	RESISTOR 56.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-56R2-F
A4R8	0811-3362	4	1	RESISTOR 825 .1% .05W PWW TC=0+-10	28480	0811-3362
A4R9	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R10	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R11	0698-6619	8	8	RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A4R12	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A4R13	0811-3315	7	1	RESISTOR 3.94K .25% .125W PWW TC=0+-2	28480	0811-3315
A4R14	0698-8167	5	1	RESISTOR 18K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1802-B
A4R15	2100-3350	5	1	RESISTOR-TRMR 200 10% C SIDE-ADJ 1-TRN	28480	2100-3350
A4R16	0698-6631	4	1	RESISTOR 2.5K .1% .125W F TC=0+-25	28480	0698-6631
A4R17	0698-6630	3	4	RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A4R18	2100-0552	3	1	RESISTOR-TRMR 50 10% C SIDE-ADJ 1-TRN	28480	2100-0552
A4R19	0698-6346	8	1	RESISTOR 300 .1% .125W F TC=0+-25	28480	0698-6346
A4R20				NOT ASSIGNED		
A4R21	0811-1641	3	1	RESISTOR 6.71K .1% .25W PWW TC=0+-5	20940	43-1/8-C-6711-B
A4R22	2100-3164	9	1	RESISTOR-TRMR 10 20% C SIDE-ADJ 17-TRN	02111	43P100
A4R23	0757-0395	1		RESISTOR 56.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-56R2-F
A4R24	0698-6977	1	1	RESISTOR 30K .1% .125W F TC=0+-25	28480	0698-6977
A4R25	2100-3095	5	2	RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN	02111	43P201
A4R26	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A4R27	2100-3109	2	1	RESISTOR-TRMR 2K 10% C SIDE-ADJ 17-TRN	02111	43P202
A4R28	2100-3095	5		RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN	02111	43P201
A4R29	0698-3440	7	1	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A4R30	0698-3152	8	1	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
A4R31	0811-2037	8	1	RESISTOR 2.4K 1% .25W PWW TC=0+-10	20940	143-D-2401-F
A4R32	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R33	0757-0279	0	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A4R34	0757-1094	9	2	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A4R35	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R36	0811-1642	9	1	RESISTOR 8.825K .1% .25W PWW TC=0+-5	20940	143-1/8-C-8825R-B
A4R37	0757-0180	2		RESISTOR 31.6 1% .125W F TC=0+-100	28480	0757-0180
A4R38	0698-0083	8	1	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R39	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A4R40	0811-3366	8	2	RESISTOR 5K .1% .05W PWW TC=0+-2	28480	0811-3366
A4R41	0811-3366	8		RESISTOR 5K .1% .05W PWW TC=0+-2	28480	0811-3366
A4R42	0698-3157	3	3	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A4R43	0698-6362	8	4	RESISTOR 1K .1% .125W F TC=0+-25	28480	0698-6362
A4R44	2100-3122	9	2	RESISTOR-TRMR 100 10% C SIDE-ADJ 17-TRN	02111	43P101
A4R45	0699-0079	4	1	RESISTOR 4.667K .1% .1W F TC=0+-10	28480	0699-0079
A4R46	0698-3437	2		RESISTOR 133 1% .125W F TC=0+-100	24546	C4-1/8-T0-133R-F
A4R47	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A4R48	0757-0444	1	1	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A4R49	0757-0465	6	3	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A4R50	0757-0419	0	2	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A4R51	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R52	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R53	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A4R54	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A4R55	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A4R56	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R57	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R58	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R59	2100-3103	6	1	RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN	02111	43P103
A4TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP13	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP14	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP15	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP16	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP17	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP18	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP19	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP20	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4TP21	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4U1	1826-0471	2	10	IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A4U2	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A4U3	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A4U4	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A4U5	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A4U6	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A4U7	1826-0264	1	1	IC CONV 10-B-D/A 16-DIP-P	24355	AD7520LN
A4U8	1826-0796	4	4	IC SWITCH ANLG LINEAR	27014	LF13202D
A4U9	1826-0797	5	1	IC D/A LINEAR CMOS CONV	24355	AD7541BD
A4U10	1826-0188	8	1	IC CONV 8-B-D/A 16-DIP-C	04713	MC1408L-8
A4U11	1826-0026	3	5	IC COMPARATOR PRCN TO-99	01295	LM311L
A4U12	1826-0462	1	1	IC CONV 10-B-D/A 16-DIP-C	04713	MC3410CL
A4U13	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A4U14	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A4U15	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A4U16	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A4U17	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A4U18	1816-1089	9	2	IC TTL LS 64-BIT RAM STAT 80-NS 3-S	27014	DM74LS189N
A4U19	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
A4U20	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A4U21	1820-1194	6	1	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
A4U22	1820-1419	8	1	IC COMPTR TTL LS MAGTD 4-BIT	01295	SN74LS85N
A4U23	1816-1089	9		IC TTL LS 64-BIT RAM STAT 80-NS 3-S	27014	DM74LS189N
A4U24	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A4U25	1820-1918	2	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A4U26	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A4U27	1820-1201	6	4	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A4VR1	1902-3171	7	3	DIODE-ZNR 11V 5% DO-35 PD=.4W TC=+.062%	28480	1902-3171
A4VR2	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A4VR3	1902-3149	9	1	DIODE-ZNR 9.09V 5% DO-35 PD=.4W	28480	1902-3149
A4VR4	1902-0551	1		DIODE-ZNR 6.19V 5% DO-15 PD=1W TC=+.022%	28480	1902-0551
A4VR5	1902-0625	0	3	DIODE-ZNR 1N829 6.2V 5% DO-7 PD=.25W	04713	1N829
A4VR6	1902-0625	0		DIODE-ZNR 1N829 6.2V 5% DO-7 PD=.25W	04713	1N829
A4VR7	1902-0625	0		DIODE-ZNR 1N829 6.2V 5% DO-7 PD=.25W	04713	1N829
				A4 MISCELLANEOUS PARTS		
	4040-0752	9	2	EXTR-PC BD YEL POLYC .062-BD-THKNS	28480	4040-0752
	1480-0073	6		PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU	28480	1480-0073
A5	08350-60025	0	1	BOARD ASSEMBLY-SWEEP GENERATOR	28480	08350-60025
A5C1	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	1500107X9010R2
A5C2	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	1500107X9010R2
A5C3	0180-0097	7	2	CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	1500476X9035B2
A5C4	0180-0097	7		CAPACITOR-FXD 47UF+-10% 35VDC TA	56289	1500476X9035B2
A5C5	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A5C6	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A5C7	0160-3742	3	1	CAPACITOR-FXD 1UF +-5% 50VDC MET-POLYC	84411	X483-1055R5M2
A5C8	0180-3020	2	1	CAPACITOR-FXD 120UF+-10% 50VDC TA	28480	0180-3020
A5C9	0160-0297	7	1	CAPACITOR-FXD 1200PF +-10% 200VDC POLYE	28480	0160-0297
A5C10	0180-2073	3	1	CAPACITOR-FXD .033UF+-10% 35VDC TA	28480	0180-2073

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5C11	0180-1743	2	1	CAPACITOR-FXD .1UF+-10% 35VDC TA	56289	150D104X9035A2
A5C12	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M822-CDH
A5C13	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M822-CDH
A5C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C23	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M822-CDH
A5C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C27				NOT ASSIGNED		
A5C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C39	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M822-CDH
A5C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C46				NOT ASSIGNED		
A5C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C48	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C49	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C50	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C52	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C53	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C54	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C55	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C56	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C57	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C58	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C59	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C60	0180-2071	1	1	CAPACITOR-FXD .022UF+-10% 35VDC TA	28480	0180-2071
A5C61	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C62	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C63	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C64	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C65	0160-3454	4		CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3454
A5C66	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C67	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M822-CDH
A5C68	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M822-CDH
A5C69	0160-3454	4		CAPACITOR-FXD 220PF +-10% 1KVDC CER	28480	0160-3454
A5C70	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C71	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C72	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A5C73	0160-3821	9	1	CAPACITOR-FXD .33UF +-20% 50VDC CER	28480	0160-3821
A5CR1	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR2	1901-0358	4	1	DIODE-DUAL 50V VF DIFF=3MV	04713	MSD6101
A5CR3				NOT ASSIGNED		
A5CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR6	1901-0376	6	2	DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A5CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR8	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	28480	1901-0376
A5CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A5CR12	1901-0538	2	1	DIODE-DUAL 70V	28480	1901-0538
A5CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5J1	8159-0005	0		WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
A5J2	1258-0124	7	1	PIN-PROGRAMING JUMPER .30 CONTACT	91506	8136-475G1
A5J3	8159-0005	0		WIRE 22AWG W PVC 1X22 80C	28480	8159-0005
A5L1	08503-80001	9		COIL-TOROID	28480	08503-80001
A5L2	9100-1655	6	1	INDUCTORRF-CH-MLD 1.2MH 5% .230X.57LG	28480	9100-1655
A5L3	08503-80001	9		COIL-TOROID	28480	08503-80001
A5L4	08503-80001	9		COIL-TOROID	28480	08503-80001
A5L5	08503-80001	9		COIL-TOROID	28480	08503-80001
A5Q1	1854-0475	5	1	TRANSISTOR-DUAL NPN PD=750MW	28480	1854-0475
A5Q2	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A5Q3	1853-0451	5	1	TRANSISTOR PNP 2N3799 SI TO-18 PD=360MW	01295	2N3799
A5Q4	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A5Q5	1853-0316	1	1	TRANSISTOR-DUAL PNP PD=500MW	28480	1853-0316
A5Q6	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A5R1	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R2	2100-3056	8	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 17-TRN	02111	43P502
A5R3	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A5R4	0698-3046	9	1	RESISTOR 16K .1% .125W F TC=0+-25	19701	MF4C1/8-T9-1602-B
A5R5	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A5R6	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A5R7	0698-3154	0	3	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A5R8	0698-8822	9	1	RESISTOR 6.81 1% .125W F TC=0+-100	28480	0698-8822
A5R9	0698-7929	5	1	RESISTOR 9.09K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-9091-B
A5R10	0699-0273	0	2	RESISTOR 2.15K .1% .125W F TC=0+-25	28480	0699-0273
A5R11	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A5R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R13	0757-0199	3	2	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A5R14	0698-3443	0	1	RESISTOR 287 1% .125W F TC=0+-100	24546	C4-1/8-T0-287R-F
A5R15	0698-3444	1	8	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A5R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R17	0757-0441	8	1	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A5R18	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A5R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R20	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A5R22	0698-7277	6	2	RESISTOR 51.1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-5112-G
A5R23	0698-7263	0	1	RESISTOR 13.3K 1% .05W F TC=0+-100	24546	C3-1/8-T0-1332-G
A5R24	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A5R25	2100-3163	8	1	RESISTOR-TRMR 1M 20% C SIDE-ADJ 17-TRN	02111	43P105
A5R26	0698-3450	9	4	RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A5R27	0698-3450	9		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A5R28	0698-3162	0	1	RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
A5R29	0698-3160	8	3	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A5R30	0757-0424	7	1	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
A5R31	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A5R32	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A5R33	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A5R34	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A5R35	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A5R36	0757-0123	3	3	RESISTOR 34.8K 1% .125W F TC=0+-100	28480	0757-0123
A5R37	0757-0123	3		RESISTOR 34.8K 1% .125W F TC=0+-100	28480	0757-0123
A5R38	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A5R39	0698-8958	2	1	RESISTOR 511K 1% .125W F TC=0+-100	28480	0698-8958
A5R40	0698-3158	5	2	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A5R41	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A5R42	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R43	2100-3161	6	1	RESISTOR-TRMR 20K 10% C SIDE-ADJ 17-TRN	02111	43P203
A5R44	0757-0123	3		RESISTOR 34.8K 1% .125W F TC=0+-100	28480	0757-0123
A5R45	0757-0440	7	2	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A5R46	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A5R47	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R48	0698-7277	6		RESISTOR 51.1K 1% .05W F TC=0+-100	24546	C3-1/8-T0-5112-G
A5R49	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R50	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A5R51	2100-3207	1	1	RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN	28480	2100-3207
A5R52	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R53	0698-3150	5		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A5R54	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R55	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R56	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R57	0698-3450	9		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A5R58	0698-3450	9		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A5R59	0698-3243	8	2	RESISTOR 178K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1783-F
A5R60	0698-3243	8		RESISTOR 178K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1783-F
A5R61	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R62	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A5R63	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A5R64				NOT ASSIGNED		
A5R65	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A5R66	0699-0273	0		RESISTOR 2.15K .1% .125W F TC=0+-25	28480	0699-0273
A5R67	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A5R68	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A5R69	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
*A5R70	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A5R72	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A5TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP13	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP14	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP15	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP16	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP17	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5U1	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A5U2	1826-0827	2	1	IC CONV 10-B-D/A 16-DIP-C	28480	1826-0827
A5U3	1826-0371	1	2	IC OP AMP LOW-BIAS-M-IMPD TO-99	27014	LF256M
A5U4	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A5U5	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A5U6	1826-0741	9	2	IC OP AMP LOW-BIAS-M-IMPD DUAL TO-99	04713	MC34002AG
A5U7	1826-0180	0	1	IC TIMER TTL MONO/ASTBL	04713	MC1455P1
A5U8	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A5U9	1826-0796	4		IC D/A LINEAR CMOS CONV	24355	AD7541BD
A5U10	1826-0796	4		IC D/A LINEAR CMOS CONV	24355	AD7541BD
A5U11	1826-0371	1		IC OP AMP LOW-BIAS-M-IMPD TO-99	27014	LF256M
A5U12	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A5U13	1826-0471	2		IC OP AMP LOW-DRIFT TO-99	28480	1826-0471
A5U14	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A5U15	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A5U16	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A5U17	1826-0796	4		IC D/A LINEAR CMOS CONV	24355	AD7541BD
A5U18	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A5U19	1826-0741	9		IC OP AMP LOW-BIAS-M-IMPD DUAL TO-99	04713	MC34002AG
A5U20	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A5U21	1820-1202	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A5U22	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A5U23	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U24	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A5U25	1820-1200	5	2	IC INV TTL LS HEX	01295	SN74LS05N
A5U26	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U27	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U28	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A5U29	1820-1423	4	3	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A5U30	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A5U31	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U32	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A5U33	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A5U34	1826-0026	3		IC COMPARATOR PRCN TO-99	01295	LM311L
A5U35	1826-0026	3		IC COMPARATOR PRCN TO-99	01295	LM311L
A5U36	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A5U37	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A5U38	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A5U39	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A5U40	1820-1244	7	2	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
A5U41	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
A5U42	1820-1200	5		IC INV TTL LS HEX	01295	SN74LS05N
A5U43	1820-1244	7		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
A5U44	1810-0206	8		NETWORK-RES 8-SIP10.0K OHM X 7	01121	208A103
A5U45	1810-0206	8		NETWORK-RES 8-SIP10.0K OHM X 7	01121	208A103
A5VR1	1902-0579	3	1	DIODE-ZNR 5.11V 5% DO-15 PO=1W TC=-.009%	28480	1902-0579
A5VR2	1902-3171	7		DIODE-ZNR 11V 5% DO-35 PO=.4W TC=+.062%	28480	1902-3171
A5VR3	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PO=.4W	28480	1902-0041
A5VR4	1902-0551	1		DIODE-ZNR 6.19V 5% DO-15 PO=1W TC=+.022%	28480	1902-0551
A5VR5	1902-3203	6	3	DIODE-ZNR 14.7V 5% DO-35 PO=.4W	28480	1902-3203

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5VR6	1902-3203	6		DIODE-ZNR 14.7V 5% DO-35 PD=.4W	28480	1902-3203
A5VR7	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A5VR8	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A5VR9	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A5VR10	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A5VR11	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A5VR12	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A5VR13	1902-0041	4		DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A5VR14	1902-1260	1	1	DIODE-ZNR 1N5525C 6.2V 2% DO-7 PD=.4W	04713	1N5525C
				A5 MISCELLANEOUS PARTS		
	1251-4932	9	4	CONNECTOR-SGL CONT SKT .021-IN-BSC-SZ	91506	L8G-1AG14-1
	1480-0073	6		PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU	28480	1480-0073
	4040-0753	0	2	EXTR-PC 80 GRN POLYC .062-BD-THKNS	28480	4040-0753
A6	08350-60026	1	1	BOARD ASSEMBLY-RECTIFIER	28480	08350-60026
A6C1	0160-0970	3	8	CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C2	0160-0970	3		CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C3	0160-0970	3		CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C4	0160-0970	3		CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C5	0160-0970	3		CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C6	0160-0970	3		CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C7	0160-0970	3		CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C8	0160-0168	1	2	CAPACITOR-FXD .1UF +-10% 200VDC POLYE	28480	0160-0168
A6C10	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
A6C11	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
A6C12	0160-0970	3		CAPACITOR-FXD .47UF +-10% 80VDC POLYE	28480	0160-0970
A6C13	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X902082
A6C14	0160-0168	1		CAPACITOR-FXD .1UF +-10% 200VDC POLYE	28480	0160-0168
A6CR1	1901-0662	3	16	DIODE-PWR RECT 100V 6A	04713	MR751
A6CR2	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR3	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR4	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR5	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR6	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR7	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR8	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR9	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR10	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR11	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR12	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR13	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR14	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A6CR15	1901-0767	9	4	DIODE-PWR RECT 400V 6A	04713	MR754
A6CR16	1901-0767	9		DIODE-PWR RECT 400V 6A	04713	MR754
A6CR17	1901-0767	9		DIODE-PWR RECT 400V 6A	04713	MR754
A6CR18	1901-0767	9		DIODE-PWR RECT 400V 6A	04713	MR754
A6CR19	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A6CR20	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A6CR21	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A6CR22	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A6CR23	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A6CR24	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A6F1	2110-0002	9	2	FUSE 2A 250V NTD 1.25X.25 UL	75915	312002
A6F2	2110-0002	9		FUSE 2A 250V NTD 1.25X.25 UL	75915	312002
A6Q1	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A6Q2	1854-0361	8	1	TRANSISTOR NPN 2N4239 SI TO-5 PD=6W	04713	2N4239
A6Q3	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A6Q4	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A6R1	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A6R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R3	0698-3438	3	1	RESISTOR 147 1% .125W F TC=0+-100	24546	C4-1/8-T0-147R-F
A6R4	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R5	0698-0084	9	5	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A6R6	0698-3260	9	1	RESISTOR 464K 1% .125W F TC=0+-100	28480	0698-3260
A6R7	0757-1000	7	3	RESISTOR 51.1 1% .5W F TC=0+-100	28480	0757-1000
A6R8	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R9	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R10	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R11	0757-1000	7		RESISTOR 51.1 1% .5W F TC=0+-100	28480	0757-1000
A6R12	0757-0814	9	1	RESISTOR 511 1% .5W F TC=0+-100	28480	0757-0814
A6U1	1826-0026	3		IC COMPARATOR PRCN TO-99	01295	LM311L

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6VR1	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
A6VR2	1902-3333	3	1	DIODE-ZNR 46.4V 5% DO-35 PD=.4W	28480	1902-3333
				A6 MISCELLANEOUS PARTS		
	1480-0073	6		PIN-ROLL .062-IN-DIA .25-IN-LG BE-CU	28480	1480-0073
	2110-0269	0	6	FUSEHOLDER-CLIP TYPE 5A .250-FUSE	28480	2110-0269
	4040-0754	1		EXTR-PC BD BLUE POLYC .062-BD-THKNS	28480	4040-0754
A7	08350-60027	2	1	BOARD ASSEMBLY-REGULATOR	28480	08350-60027
A7C1	0180-2661	5	2	CAPACITOR-FXD 1UF+-10% 50VDC TA	25088	D1R0G81A50K
A7C2	0180-0291	3	18	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C3	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A7C4	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C5	0160-2202	8	3	CAPACITOR-FXD 75PF +-5% 300VDC MICA	28480	0160-2202
A7C6	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A7C7	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C8	0180-2661	5		CAPACITOR-FXD 1UF+-10% 50VDC TA	25088	D1R0G81A50K
A7C9	0160-4299	7		CAPACITOR-FXD 2200PF +-20% 250VDC CER	56289	C067F251F222M522-CDM
A7C10	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C11	0160-2202	8		CAPACITOR-FXD 75PF +-5% 300VDC MICA	28480	0160-2202
A7C12	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C13	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A7C14	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C15	0160-2202	8		CAPACITOR-FXD 75PF +-5% 300VDC MICA	28480	0160-2202
A7C16	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A7C17	0180-3087	7	2	CAPACITOR-FXD 1.5UF 50VDC TA	28480	0180-3087
A7C18	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C19	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A7C20	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C21	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C22	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C23	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C24	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C25	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C26	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C27	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C28	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A7C30	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C31	0160-3875	3	3	CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A7C32	0160-3875	3		CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A7C33	0160-3875	3		CAPACITOR-FXD 22PF +-5% 200VDC CER 0+-30	28480	0160-3875
A7C34	0180-3087	7		CAPACITOR-FXD 1.5UF 50VDC TA	28480	0180-3087
A7C35	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
A7C36	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A7C37	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A7C41	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A7C42	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A7C43	0180-2697	7	2	CAPACITOR-FXD 10UF+-10% 25VDC TA	28480	0180-2697
A7C44	0180-2697	7		CAPACITOR-FXD 10UF+-10% 25VDC TA	28480	0180-2697
A7C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A7C46	0180-2617	1	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	25088	D6R8G81835X
A7C47	0160-0570	9	3	CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A7C48	0160-0570	9		CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A7C49	0160-0570	9		CAPACITOR-FXD 220PF +-20% 100VDC CER	20932	5024EM100RD221M
A7CR1	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A7CR2	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A7CR3	1901-0028	5	12	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR4	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A7CR5	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A7CR6	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR7	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR8	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A7CR9	1901-0743	1	6	DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A7CR10	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A7CR11	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A7CR12	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A7CR13	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A7CR14	1901-0743	1		DIODE-PWR RECT 1N4004 400V 1A DO-41	01295	1N4004
A7CR16	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
A7CR17	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR18	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR19	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR20	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR21	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7CR22	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR23	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR24	1901-0662	3		DIODE-PWR RECT 100V 6A	04713	MR751
A7CR25	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7CR26	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A7DS1	1990-0485	5	12	LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7DS2	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7DS3	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7DS4	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7DS5	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7DS6	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7DS7	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7DS8	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A7F1	2110-0332	8	4	FUSE 3A 125V .25X.27	28480	2110-0332
A7F2	2110-0818	3	1	FUSE 5A 125V NTD .25X.27	28480	2110-0818
A7F3	2110-0036	9	1	FUSE 8A 125V NTD 1.25X.25 UL	75915	312008
A7F4	2110-0332	8		FUSE 3A 125V .25X.27	28480	2110-0332
A7F5	2110-0332	8		FUSE 3A 125V .25X.27	28480	2110-0332
A7F6	2110-0425	0	1	FUSE 2A 125V .25X.27	28480	2110-0425
A7M*1	0380-0059	5	6	SPACER-RVT-ON .25-IN-LG .152-IN-ID	00000	ORDER BY DESCRIPTION
A7Q1	1855-0421	3	1	TRANSISTOR J-FET 2N5114 P-CHAN D-MODE	17856	2N5114
A7Q2	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A7Q3	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A7Q4	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A7Q5	1884-0261	0	1	THYRISTOR-SCR TO-220AB VRRM=100	28480	1884-0261
A7Q6*	1854-0743	0	1	TRANSISTOR NPN 2N5878 SI TO-3 PD=150W	01295	2N5878
A7Q7	1854-0477	7		TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
A7Q8	1854-0271	9	1	TRANSISTOR NPN SI TO-39 PD=1W FT=150MHZ	28480	1854-0271
A7R1	0698-3442	9	1	RESISTOR 237 1% .125W F TC=0+-100	24546	C4-1/8-T0-237R-F
A7R2	0757-0422	5	2	RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A7R3	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A7R4	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R5	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R6	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A7R7	0757-0422	5		RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A7R8	0698-0089	4	1	RESISTOR 1.78K 1% .5W F TC=0+-100	28480	0698-0089
A7R9	0698-8805	8	1	RESISTOR 10.35K .1% .125W F TC=0+-25	28480	0698-8805
A7R10	2100-3123	0	1	RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A7R11	0698-8808	9	1	RESISTOR 4.525K .1% .125W F TC=0+-25	28480	0698-8808
A7R12	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A7R13	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A7R14	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A7R15	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A7R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R17	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R18	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A7R19	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R20	0698-6322	0	3	RESISTOR 4K .1% .125W F TC=0+-25	28480	0698-6322
A7R21	2100-3052	4		RESISTOR-TRMR 50 10% C SIDE-ADJ 17-TRN	02111	43P500
A7R22	0698-6322	0		RESISTOR 4K .1% .125W F TC=0+-25	28480	0698-6322
A7R23	0698-6322	0		RESISTOR 4K .1% .125W F TC=0+-25	28480	0698-6322
A7R24	0757-0818	3	3	RESISTOR 825 1% .5W F TC=0+-100	28480	0757-0818
A7R25	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R26	0698-3136	8	1	RESISTOR 17.8K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1782-F
A7R27	0757-1000	7		RESISTOR 51.1 1% .5W F TC=0+-100	28480	0757-1000
A7R28	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A7R29	0811-1553	1	1	RESISTOR .68 5% 2W PW TC=0+-300	75042	BWH2-11/1B-J
A7R30	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R31	0698-3160	8		RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A7R32	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R33	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A7R34	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R35	0698-3410	1	2	RESISTOR 3.16K 1% .5W F TC=0+-100	28480	0698-3410
A7R36	0698-3410	1		RESISTOR 3.16K 1% .5W F TC=0+-100	28480	0698-3410
A7R37	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A7R38	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A7R39	2100-3122	9		RESISTOR-TRMR 100 10% C SIDE-ADJ 17-TRN	02111	43P101
A7R40	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A7R41	0757-0818	3		RESISTOR 825 1% .5W F TC=0+-100	28480	0757-0818
A7R42	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R43	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A7R44	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A7R45	0698-6782	6	1	RESISTOR 250 .1% .125W F TC=0+-25	28480	0698-6782

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7R46	0699-0407	2	1	RESISTOR 1,749K .1% .25W F TC=0+-25	28480	0699-0407
A7R47	0757-0818	3		RESISTOR 825 1% .5W F TC=0+-100	28480	0757-0818
A7R48	0698-3406	5	2	RESISTOR 1.33K 1% .5W F TC=0+-100	28480	0698-3406
A7R49	0698-3406	5		RESISTOR 1.33K 1% .5W F TC=0+-100	28480	0698-3406
A7R50	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A7R51	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A7R52	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A7R53	0698-3431	6	1	RESISTOR 23.7 1% .125W F TC=0+-100	03888	PME55-1/8-T0-23R7-F
A7R54	0698-6362	8		RESISTOR 1K .1% .125W F TC=0+-25	28480	0698-6362
A7R55	0698-6362	8		RESISTOR 1K .1% .125W F TC=0+-25	28480	0698-6362
A7R56	0698-3158	4	1	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A7R57	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A7R58	2100-3534	5	1	RESISTOR-TRMR 100 10% C SIDE-ADJ 17-TRN	28480	2100-3534
A7R59	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A7R60	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A7R61	0698-6360	6	2	RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A7R62	0698-6362	8		RESISTOR 1K .1% .125W F TC=0+-25	28480	0698-6362
A7R63	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A7R64	0698-6630	3		RESISTOR 20K .1% .125W F TC=0+-25	28480	0698-6630
A7R65	0698-6619	8		RESISTOR 15K .1% .125W F TC=0+-25	28480	0698-6619
A7R66	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A7R67	0699-0083	0	1	RESISTOR 681 .1% .1W F TC=0+-10	28480	0699-0083
A7R68	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A7R69	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A7R70	0698-3444	1		RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A7R71	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R72	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A7R73	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A7R74	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
*A7R75	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
A7R77	0698-8812	7	8	RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R78	0698-8812	7		RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R79	0698-8812	7		RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R80	0698-8812	7		RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R81	0698-8812	7		RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R82	0698-8812	7		RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R83	0698-8812	7		RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R84	0698-8812	7		RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812
A7R85	0698-7576	8	1	RESISTOR 217 .1% .125W F TC=0+-25	19701	MF4C1/8-T9-217R-B
A7R86	0698-3940	2	1	RESISTOR 2.39K .1% .125W F TC=0+-25	28480	0698-3940
A7R87	0698-6320	8	1	RESISTOR 5K .1% .125W F TC=0+-25	03888	PME55-1/8-T9-5001-B
A7TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7U1	1826-0693	0	2	IC V RGLTR-FXD-POS 12V TO-66 PKG	28480	1826-0693
A7U2	1826-0569	9	3	IC OP AMP LOW-NOISE TO-99	18324	NE5534AT
A7U3	1826-0690	7	2	IC V RGLTR-ADJ-NEG 1.2/37V TO-3 PKG	28480	1826-0690
A7U4	1826-0693	0		IC V RGLTR-FXD-POS 12V TO-66 PKG	28480	1826-0693
A7U5	1826-0722	6	2	IC V RGLTR-ADJ-POS 1.2/37V TO-3 PKG	28480	1826-0722
A7U6	1826-0691	8	1	IC V RGLTR-FXD-POS 20V TO-66 PKG	28480	1826-0691
A7U7	1826-0722	6		IC V RGLTR-ADJ-POS 1.2/37V TO-3 PKG	28480	1826-0722
A7U8	1826-0569	9		IC OP AMP LOW-NOISE TO-99	18324	NE5534AT
A7U9	1826-0732	8		IC V RGLTR-FXD-POS 5V TO-3 PKG	28480	1826-0732
A7U10	1826-0724	8	1	IC V RGLTR-ADJ-POS 1.2/33V TO-3 PKG	28480	1826-0724
A7U11	1826-0098	9	1	IC COMPARATOR PRCN TO-99	27014	LM211H
A7U12	1826-0692	9	2	IC V RGLTR-FXD-POS 15V TO-66 PKG	28480	1826-0692
A7U13	1826-0725	9	1	IC V RGLTR-FXD-POS 14.4/15.6V TO-3 PKG	28480	1826-0725
A7U14	1826-0692	9		IC V RGLTR-FXD-POS 15V TO-66 PKG	28480	1826-0692
A7U15	1826-0690	7		IC V RGLTR-ADJ-NEG 1.2/37V TO-3 PKG	28480	1826-0690
A7U16	1826-0513	3	1	IC V RGLTR TO-3	80103	LAS-1905
A7U17	1826-0026	3		IC COMPARATOR PRCN TO-99	01295	LM311L
A7U18	1826-0732	8	2	IC V RGLTR-FXD-POS 5V TO-3 PKG	28480	1826-0732
A7U19	1826-0569	9		IC OP AMP LOW-NOISE TO-99	18324	NE5534AT
A7VR1	1902-0025	4	2	DIODE-ZNR 10V 5% DO-35 PD=.4W TC=+.06%	28480	1902-0025
A7VR2	1902-0680	7	1	DIODE-ZNR 1N827 6.2V 5% DO-7 PD=.4W	24046	1N827
A7VR3	1902-3203	6		DIODE-ZNR 14.7V 5% DO-35 PD=.4W	28480	1902-3203
A7VR4	1902-0025	4		DIODE-ZNR 10V 5% DO-35 PD=.4W TC=+.06%	28480	1902-0025
A7VR5	1902-3330	0	1	DIODE-ZNR 44.2V 2% DO-35 PD=.4W	28480	1902-3330

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7VR6	1902-0244	9	1	DIODE-ZNR 30.1V 5% DO-15 PD=1W TC=+.075%	28480	1902-0244
A7VR7	1902-3171	7		DIODE-ZNR 11V 5% DO-35 PD=.4W TC=+.062%	28480	1902-3171
				A7 MISCELLANEOUS PARTS		
	1205-0202	1	1	THERMAL LINK DUAL TO-18-CS	28480	1205-0202
	2110-0269	0		FUSEHOLDER-CLIP TYPE 5A .250-FUSE	28480	2110-0269
	2360-0115	4	13	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	1251-2313	6	43	CONNECTOR-SGL CONT SKT .04-IN-BSC-SZ RND	28480	1251-2313
	1251-3172	7	7	CONNECTOR-SGL CONT SKT .03-IN-BSC-SZ RND	28480	1251-3172
	08350-20002	9	7	FRAME-HEAT SINK	28480	08350-20002
	08350-20003	0	7	FINS-HEAT SINK	28480	08350-20003
				*NOTE: HEAT SINK, ASSOCIATED DEVICES AND HARDWARE ARE NOT INCLUDED IN A7, HP PART NUMBER 08350-60027. FOR REGULATOR HEAT SINK PARTS LOCATION SEE FIGURE 6-8, REGULATOR HEAT SINK, PARTS LOCATION.		
A8	08350-60029	4	1	BOARD ASSEMBLY-HP-IB	28480	08350-60029
A8C1	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C15	0180-2207	5		CAPACITOR-FXD 100UF+-10% 10VDC TA	56289	150D107X9010R2
A8C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A8DS1	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A8DS2	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A8DS3	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A8DS4	1990-0485	5		LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
A8J1	1200-0565	9	1	SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0565
A8L1	08503-80001	9		COIL-TOROID	28480	08503-80001
A8S1	3101-2340	4	1	SWITCH-DIP SPST 5-POSITION	28480	3101-2340
A8TP1	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A8U1	1810-0338	7		NETWORK-RES 16-DIP100.0 OHM X 8	11236	761-3-R100
A8U2	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A8U3	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A8U4	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A8U5	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A8U6	1820-2357	5	1		28480	1820-2357
A8U7	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A8U8	1820-2483	8	1	IC RCVR TTL LS BUS OCTL	01295	SN75161N
A8U9	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A8U10	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A8U11	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A8U12	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A8U13	1820-2485	0	1	IC RCVR TTL LS BUS OCTL	01295	SN75160N
A8U14	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A8U15	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A8U16	1820-1130	0	2	IC GATE TTL S NAND 13-INP	01295	SN74S133N
A8U17	1820-1130	0		IC GATE TTL S NAND 13-INP	01295	SN74S133N
A8U18	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A8U19	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A8U20	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

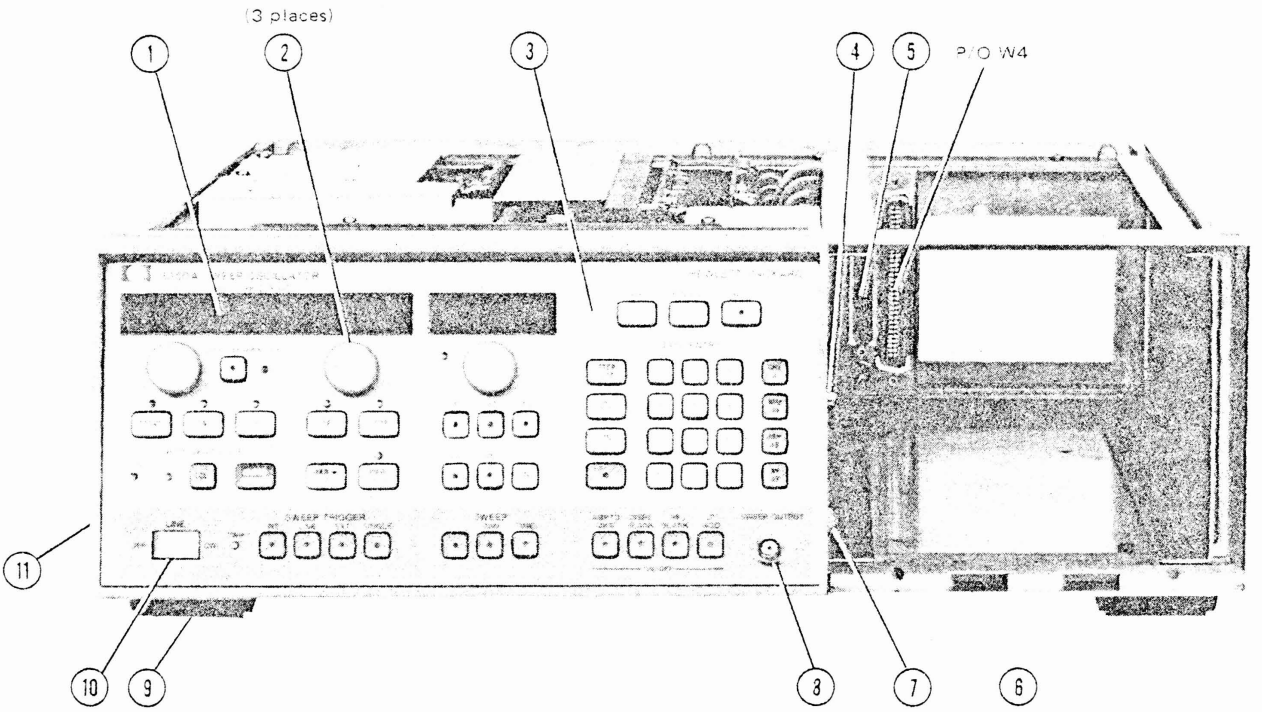
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8U21	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A8U22	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A8U23	1810-0338	7		NETWORK-RES 16-DIP100,0 OHM X 8	11236	761-3-R100
A8U24	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A8U25	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A8VR1	1902-0551	1		DIODE-ZNR 6.19V 5% DO-15 PD=1W TC=+.022%	28480	1902-0551
A9	08350-60028	3	1	BOARD ASSEMBLY-MOTHER	28480	08350-60028
A9E1-A9E7	1251-0600	0	7	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SO	28480	1251-0600
A9F1	2110-0333	9	1	FUSE 1.5A 125V .25X.27	28480	2110-0333
A9F2	2110-0332	8		FUSE 3A 125V .25X.27	28480	2110-0332
A9F3	2110-0218	9	1	FUSE .1A 250V .25X.27	28480	2110-0218
A9J1	1251-5902	5	2	CONNECTOR 32-PIN M POST TYPE	28480	1251-5902
A9J2	1251-4715	5	1	CONNECTOR 17-PIN M POST TYPE	28480	1251-4715
A9J3	1251-4542	7	1	CONNECTOR 26-PIN M POST TYPE	28480	1251-4542
A9XA2	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA3A	1251-1365	6	10	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA3B	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA4A	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA4B	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA5A	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA5B	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA6	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA7	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
A9XA8	1251-1365	6		CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	28480	1251-1365
				A9 MISCELLANEOUS PARTS		
	1251-2313	6		CONNECTOR-SGL CONT SKT .04-IN-BSC-SZ RND	28480	1251-2313
				CHASSIS PARTS		
B1	08350-60015	3	1	FAN/SHIELD ASSY	28480	08350-60015
B1 (OPT 400)	08350-60032	9	1	400 HZ FAN ASSY	28480	08350-60032
BT1 (OPT 001)	08672-60092	0	1	BATTERY PACK	28480	08672-60092
C1	0180-2317	3	3	CAPACITOR-FXD 3600UF +75-10% 40VDC	00853	339-7448-02
C2	0180-2317	3		CAPACITOR-FXD 3600UF +75-10% 40VDC	00853	339-7448-02
C3	0180-2317	3		CAPACITOR-FXD 3600UF +75-10% 40VDC	00853	339-7448-02
C4	0180-2495	3	1	CAPACITOR-FXD 8700 UF +75-10% 40VDC	00853	500872G040AC2A
C5	0180-3017	7	1	CAPACITOR-FXD 45000UF +75-10% 25VDC	56001	36F5112M1
C6	0180-2603	5	1	CAPACITOR-FXD 7200 UF +75-10% 50VDC	00853	500722G050AC2A
C7	0180-2922	1	1	CAPACITOR-FXD 2600 UF +75-10% 100VDC	56289	36DX262G100AC2A
CR1-4	1901-0033	2	4	DIODE-GEN 180V 200MA DO-7	07263	FDH5369
E1	08350-60014	7	1	FAN CABLE ASSY	28480	08350-60014
E1 (OPT 400)	08350-60033	0	1	400 HZ FAN CABLE ASSY	28480	08350-60033
F1	2110-0002	9	1	FUSE 2A 250V NTD 1.25X.25 UL	71400	AGC-2
F2	2110-0055	2	1	FUSE 4A 250V NTD 1.25X.25 UL	71400	MTH-4
FL1	0960-0448	6	1	LINE MODULAR FILTER	05245	FL927
J1	1250-0083	1	7	CONNECTOR-RF BNC F, SWP OUT	24931	28JR130-1
J2				P/O W4, PLUG-IN INTERFACE		
J3				P/O W6, PLUG-IN PWR SUPPLY INTERFACE		
J4				P/O W5, HP-IB INTERFACE		
J5	1250-0083	1		CONNECTOR-RF BNC F, POS Z BLANK	24931	28JR130-1
J6	1250-0083	1		CONNECTOR-RF BNC F, NEG Z BLANKING	24931	28JR130-1
J7	1250-0083	1		CONNECTOR-RF BNC F, PEN LIFT	24931	28JR130-1
J8	1250-0083	1		CONNECTOR-RF BNC F, SWP OUT/IN	24931	28JR130-1
J9	1250-0083	1		CONNECTOR-RF BNC F, CNTR FRIG	24931	28JR130-1
J10	1250-0083	1		CONNECTOR-RF BNC F, STOP SWEEP	24931	28JR130-1
J11	1250-0118	3	2	CONNECTOR-RF BNC F, FM INPUT	24931	0140-7
J12	1250-0118	3		CONNECTOR-RF BNC F, AM INPUT	24931	0140-7
J13				P/O W7, AUX. PROGRAMMING		
J14	1251-6731	0	1	CONNECTOR-8755 INTERFACE	28480	1251-6731
S1	3101-2269	6	1	SWITCH-TOGGLE DPDT 3A 250VAC	09353	8201-P3-H-Z-Q
S2	3103-0009	2	1	SWITCH-THRM +150F 5A OPN-ON-RISE	32647	20700L10-205
T1	5081-9885	4	1	TRANSFORMER, POWER	28480	5081-9885
W1	08350-60003	4	1	CABLE ASSY, RIBBON 34C	28480	08350-60003
				A1/A2 INTERCONNECT		
W2	08350-60004	5	1	CABLE ASSY, RIBBON 50C	28480	08350-60004
				A1/A2 INTERCONNECT		
*W3	08350-60006	7	1	CABLE ASSY, COAX/BROWN	28480	08350-60006
				/ TUNE		
W4	08350-60005	6	1	CABLE ASSY, RIBBON 64C, PLUG-IN INTERFACE	28480	08350-60005
W5	08350-60013	5	1	CABLE ASSY, RIBBON 26C	28480	08350-60013
				HP-IB INTERFACE		
*W6	08350-60010	3	1	CABLE ASSY 17 PIN, PLUG IN POWER SUPPLY	28480	08350-60010
				INTERFACE		
W7	08350-60002	3	1	CABLE ASSY RIBBON 26C PROGRAMMING/8755	28480	08350-60002
				INTERFACE		
*W8	08350-60007	3	1	CABLE ASSY COAX/ORANGE FM IN	28480	08350-60007
*W9	08350-60008	9	1	CABLE ASSY COAX/YELLOW	28480	08350-60008
W10	08350-60019	1	1	CABLE ASSY REAR PANEL	28480	08350-60019
				*W3, W6, W8 AND W9 ARE COMMON TO J3 (PART OF PLUG-IN INTERFACE)		

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts

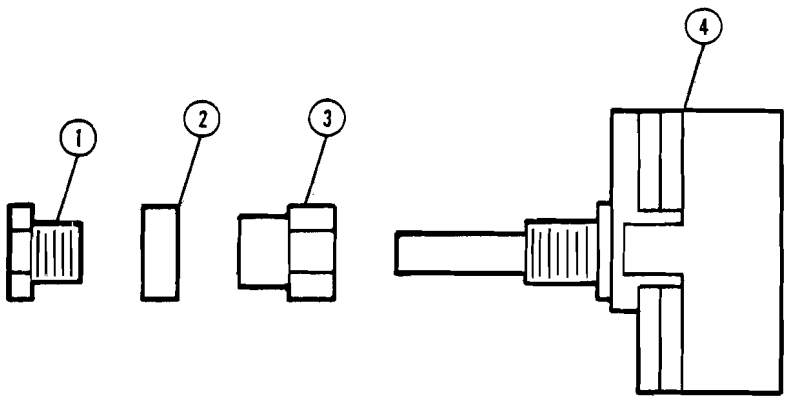
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				MISCELLANEOUS		
	2360-0130	5	5	TERMINAL, SLDR LUG	79963	720-.330H
	3390-0106	8	4	NUT HEX PLASTIC 2-56-THD .1-3-IN-THK	72962	22NM-26
	2190-0009	4	1	WASHER-LK NO. 3 .168-IN-ID	0G791	900-3C
	2190-0016	3	9	WASHER-LK 3/8IN. .377-IN-ID	28480	2190-0016
	2360-0055	1	4	SCREW-MACH 6-32 .188-IN-LG	93907	N-632-3/16
	2360-0132	5	5	SCREW-MACH 4-40 .312-IN-LG	28480	2360-0132
	2360-0138	3	2	SCREW-MACH 6-32 .438-IN-LG	28480	2360-0138
	2360-0353	8	3	SCREW-MACH 6-32 .25-IN-LG 100DEG	28480	2360-0353
	2420-0001	5	6	NUT-HEX 6-32THD .113-IN-THK	78189	511-0611200-00-3280-2580
	2680-0172	1	4	SCREW-MACH 10-32 .375-IN-LG 100DEG	28480	2680-0172
	2950-0001	3	2	NUT-HEX 3/8-32-THD .094-IN-THK	12697	2074-13

See introduction to this section for ordering information
*Indicates factory selected value



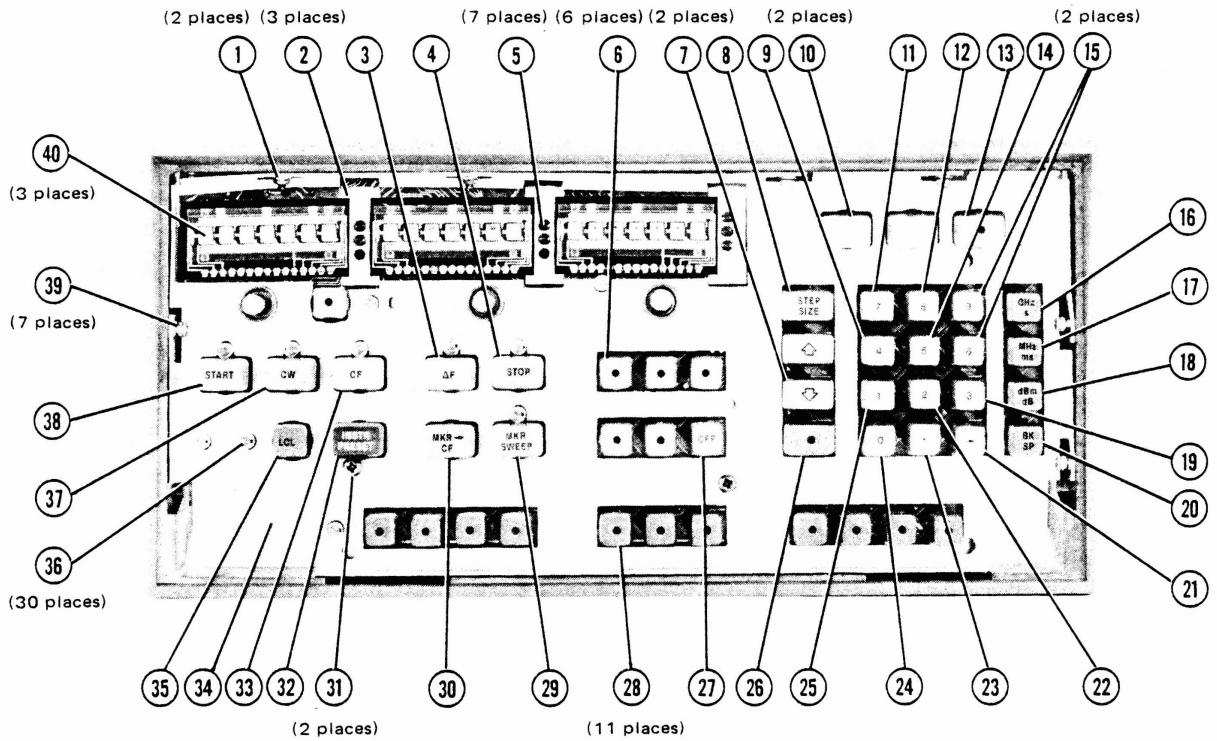
Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	1000-0532	6	1	Display Window	28480	1000-0532
2	0370-3023	8	3	Knob-Round	28480	0370-3023
3	08350-00001	6	1	Panel, Front Dress	28480	08350-00001
4	08620-20062	8	1	Screw-Latch Bearing	28480	08620-20062
5	1251-5903	6	1	Conn-21 Pin F Submin	71785	DCM F21 WA45
	1251-2942	7	2	Conn-R&P Lock	71785	D20418-2
6	08350-20015	4	2	Guide Pin	28480	08350-20015
	2360-0115	4	2	Screw Mach 6-32	28480	2360-0115
7	0361-1088	2	1	Rivet-Push In .275-in-lg	02768	254-090401-00-0101
8	1250-0083	1	1	Conn-RF BNC F	24931	28JR 130-1
9	5040-7201	8	4	Foot - Bottom	28480	5040-7201
10	3131-0435	7	1	Switch - Front Panel On/Off	28480	3131-0435
	1480-0080	5	1	Pin Roller - Switch	72962	59-022-094-0750
	08350-00012	9	1	Clip Wire - Switch	28480	08350-00012
	4040-1657	5	1	Bracket - Switch Holder	28480	4040-1657
11	08350-20001	8	1	Front Panel Frame	28480	08350-20001

Figure 6-1. Front Panel, Parts Identification



Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	08350-20013	2	3	Nut - Hex	28480	08350-20013
2	08350-20015	4	3	Spacer - Panel	28480	08350-20015
3	08350-20012	1	3	Bushing Panel	28480	08350-20012
4	5060-9444	7	3	Rotary Pulse Generator	28480	5060-9444

Figure 6-2. Rotary Pulse Generator (RPG), Parts Identification

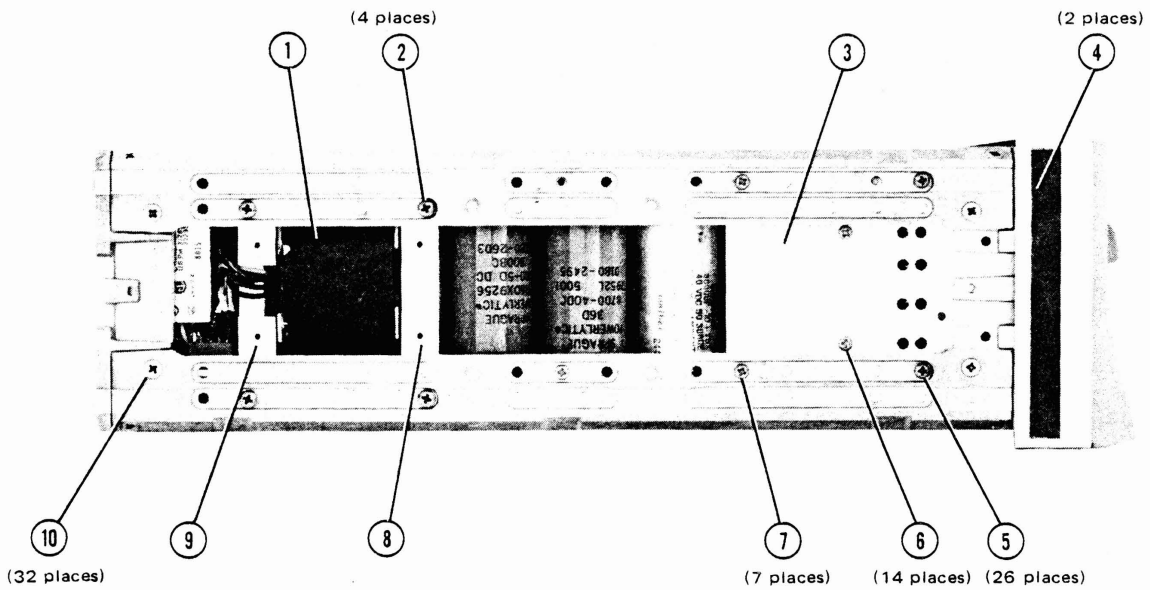


Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	2260-0002 2190-0019	6 6	2 2	Nut-Hex 4-40THD Washer-Lk HLCL .115-in.-ID	28480 28480	2260-0002 2190-0019
2	1450-0588	5	3	Lamp Housing, Polycarbonate	28480	1450-0588
3	5041-1773	9	1	Key ΔF	28480	5041-1773
4	5041-1777	3	1	Key STOP	28480	5041-1777
5	1990-0582	3	7	LED-Visible IF=60mA max	28480	1990-0582
6	5041-0285	6	6	Key	28480	5041-0285
7	5041-0855	6	2	Key	28480	5041-0855
8	5041-1771	7	1	Key STEP SIZE	28480	5041-1771
9	5041-1760	4	1	Key 4	28480	5041-1760
10	5041-0277	6	2	Key	28480	5041-0277
11	5041-1763	7	1	Key 7	28480	5041-1763

Figure 6-3. Sub Panel, Parts Identification (1 of 2)

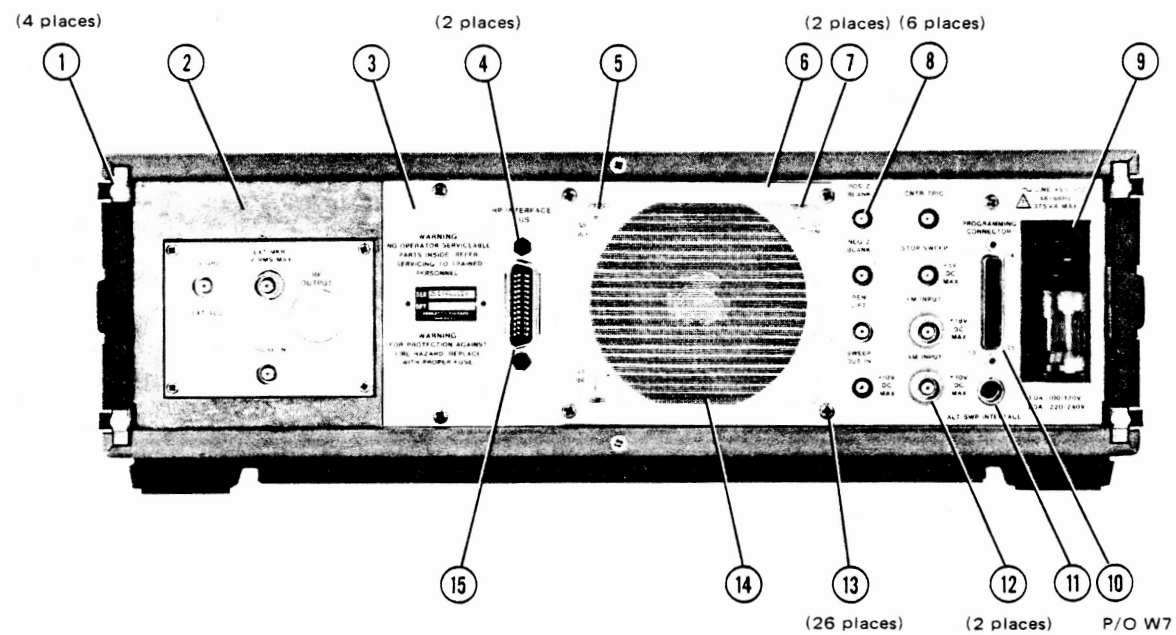
Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
12	5041-1764	8	1	Key	28480	5041-1764
13	5041-0286	7	1	Key	28480	5041-0286
14	5041-1761	5	1	Key	28480	5041-1761
15	5041-1762	6	2	Key	28480	5041-1762
16	5041-1766	0	1	Key	28480	5041-1766
17	5041-1767	1	1	Key	28480	5041-1767
18	5041-1940	2	1	Key	28480	5041-1940
19	5041-1759	1	1	Key	28480	5041-1759
20	5041-1769	3	1	Key	28480	5041-1769
21	5041-1770	6	1	Key	28480	5041-1770
22	5041-1758	0	1	Key	28480	5041-1758
23	5041-1755	7	1	Key	28480	5041-1755
24	5041-1756	8	1	Key	28480	5041-1756
25	5041-1757	9	1	Key	28480	5041-1757
26	5041-0451	8	1	Key (blue)	28480	5041-0451
27	5041-1765	9	1	Key	28480	5041-1765
28	5041-0318	6	11	Key (dark gray)	28480	5041-0318
29	5041-1951	5	1	Key	28480	5041-1951
30	5041-2088	1	1	Key	28480	5041-2088
31	2200-0091	7	2	Screw - Mach 4-40 .562-in.-lg	28480	2200-0091
32	5041-0720	4	1	Key (green)	28480	5041-0720
33	5041-1772	8	1	Key	28480	5041-1772
34	08350-00002	7	1	Sub Panel, Front	28480	08350-00002
35	5041-0726	Ø	1	Key	28480	5041-0726
36	1990-0487	7	30	LED-Visible IF=20mA max	28480	5082-4584
37	5041-1774	Ø	1	Key	28480	5041-1774
38	5041-1776	2	1	Key	28480	5041-1776
39	3030-0189	4	7	Screw-Skt Hd Cap 4-40 .25-in.-lg	28480	3030-0189
40	08350-60009	Ø	3	Digital Display	28480	08350-60009

Figure 6-3. Sub Panel, Parts Identification (2 of 2)



Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	08350-00020	9	1	Shield, Transformer	28480	08350-00020
2	2510-0051	6	4	Screw-Mach 8-32 .625-in.-lg	28480	2510-0051
3	08350-00005	Ø	1	Gusset, Left	28480	08350-00005
4	5001-0439	8	2	Trim Strip	28480	5001-0439
5	2360-0115	4	26	Screw-Mach 6-32 .312-in.-lg	28480	2360-0115
6	2360-0113	2	14	Screw-Mach 6-32 .25-in.-lg	28480	2360-0113
7	2360-0117	6	7	Screw-Mach 6-32 .375-in.-lg	28480	2360-0117
8	08350-20016	5	1	Support, Transformer Forward	28480	08350-20016
9	08350-20005	2	1	Support, Transformer Rear	28480	08350-20005
10	2510-0192	6	32	Screw-Mach 8-32 .25-in.-lg 100 deg	28480	2510-0192

Figure 6-4. Left Side View, Parts Identification



Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	0570-1170	6	4	Screw-SPCL 10-32 .388-in.-lg	28480	0570-1170
2	08350-20011	Ø	1	Frame, Rear	28480	08350-20011
3	08350-00004	9	1	Panel, Rear Sheet	28480	08350-00004
4	0380-0643	3	2	Standoff - Hex .255-in.-lg 6-32 thd	28480	0380-0643
5	2360-0184	7	1	Screw-Mach 6-32 .438-in.-lg 82 deg	28480	2360-0184
6	3150-0054	6	1	Filter-Air	28480	3150-0054
7	2360-0218	8	2	Screw-Mach 6-32 2-in.-lg 82 deg	28480	2360-0218
8	1250-0083	1	6	Conn-RF BNC F	24931	28JR130-1
9	0960-0048	6	1	Line Modular Filter	05245	F1927
10				P/O W7 (see Chassis Parts)		
11	1251-6781	Ø	1	Connector RCPT 3 M	28480	1251-6781
12	1250-0118	3	2	Conn-RF BNC F	24931	C140-7
	5040-0345	7	4	Insulator-Conn	28480	5040-0345
13	2360-0115	4	26	Screw-Mach 6-32 .312-in.-lg	28480	2360-0115
14	3160-0288	Ø	1	Fan TBAX 60 CFM 115V 50/60 Hz	4N833	113XN-182
	3160-0317 (Opt 400)	5	1	Fan TBAX 40 CFM 115V 440 Hz	92702	MBCZ206 F-6-5
	08350-00019	6	1	Gasket, Rubber	28480	08350-00019
15				P/O W/5 (see Chassis Parts)		

Figure 6-5. Rear Panel, Parts Identification

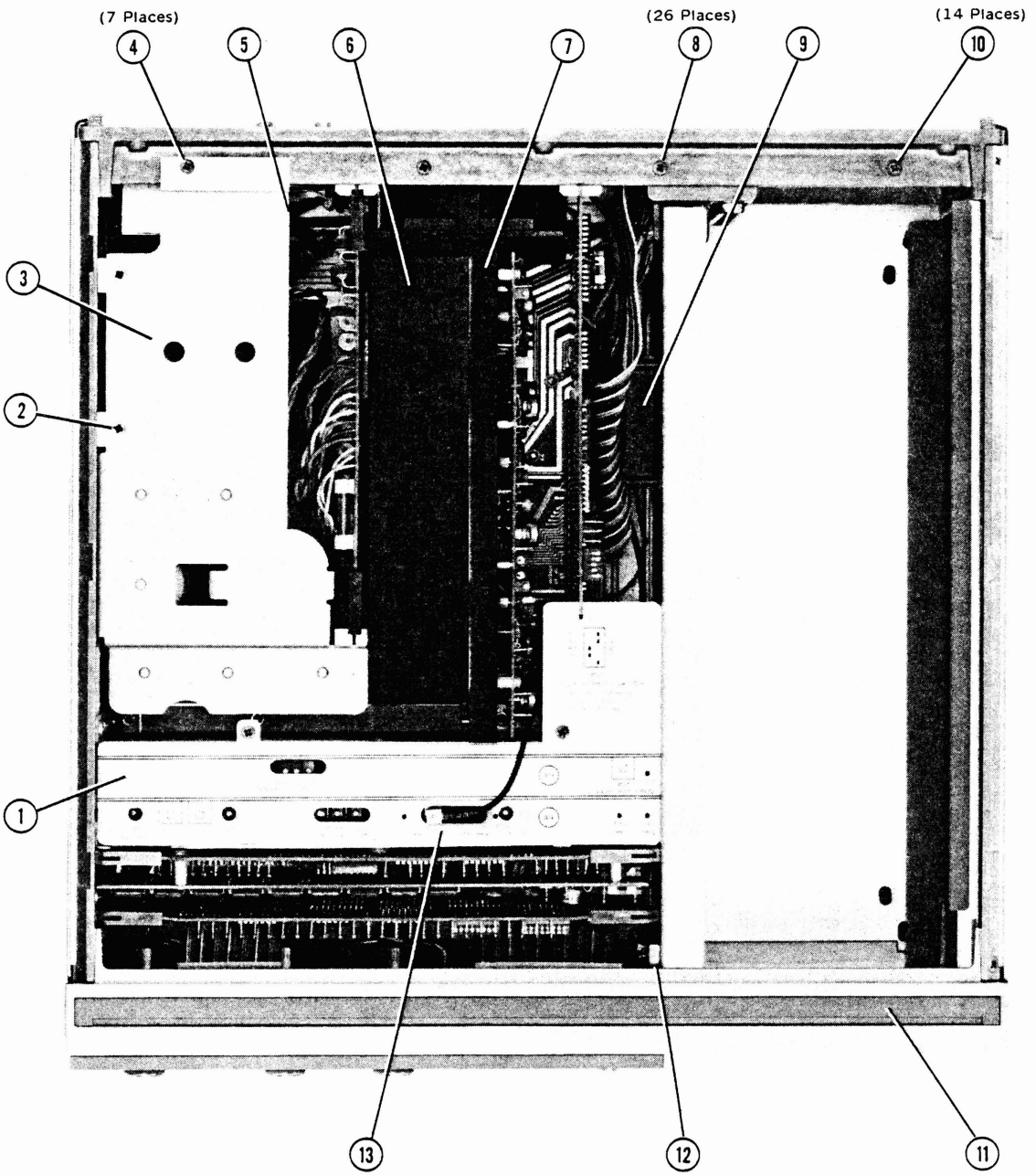


Figure 6-6. Top View With Covers, Parts Identification (1 of 2)

Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	08350-00011	8	1	Cover, Shield	28480	08350-00011
2	2360-0322	5	2	Screw-Mach 6-32 .375-in.-lg 100 deg	28480	08350-00022
3	08350-00015	2	1	Capacitor Cover	28480	08350-00015
4	2360-0117	6	7	Screw-Mach 6-32 .375-in.-lg	28480	2360-0117
5	0400-0018	Ø	.50 ft.	Grommet, Cap Cover	03296	G-51H-A
6	08350-20003	Ø	1	Fins, Heatsink	28480	08350-20003
7	08350-20002	9	1	Frame, Heatsink	28480	08350-20002
8	2360-0115	4	26	Screw-Mach, 6-32 .312-in.-lg	28480	2360-0115
9	08672-60092 (Opt 001)	Ø	1	Battery Pack	28480	08672-60092
	85660-20138	9	1	Battery Holder	28480	85660-20138
	85660-00054 (Opt 001)	6	1	Battery Clamp	28480	85660-00054
	0363-0160	3	2	Contacts-Electric	28480	0363-0160
	0624-0289	1	4	Screw-Tpg 2-28 .312-in.-lg	28480	0624-0289
10	2360-0113	2	14	Screw-Mach 6-32 .25-in.-lg	28480	2360-0113
11	5040-7202	9	1	Trim Strip, Top	28480	5040-7202
12	08620-20061	7	1	Bearing Latch	28480	08620-20061
	8350-20006	3	1	Bracket, Plug Latch	28480	08350-20006
	2420-0003	7	1	Nut-Hex, 6-32-Thd .094-in.-thk	28480	2420-0003
13	0400-0233	1	1	Grommet - Ellipse	28480	0400-0233

Figure 6-6. Top View With Covers, Parts Identification (2 of 2)

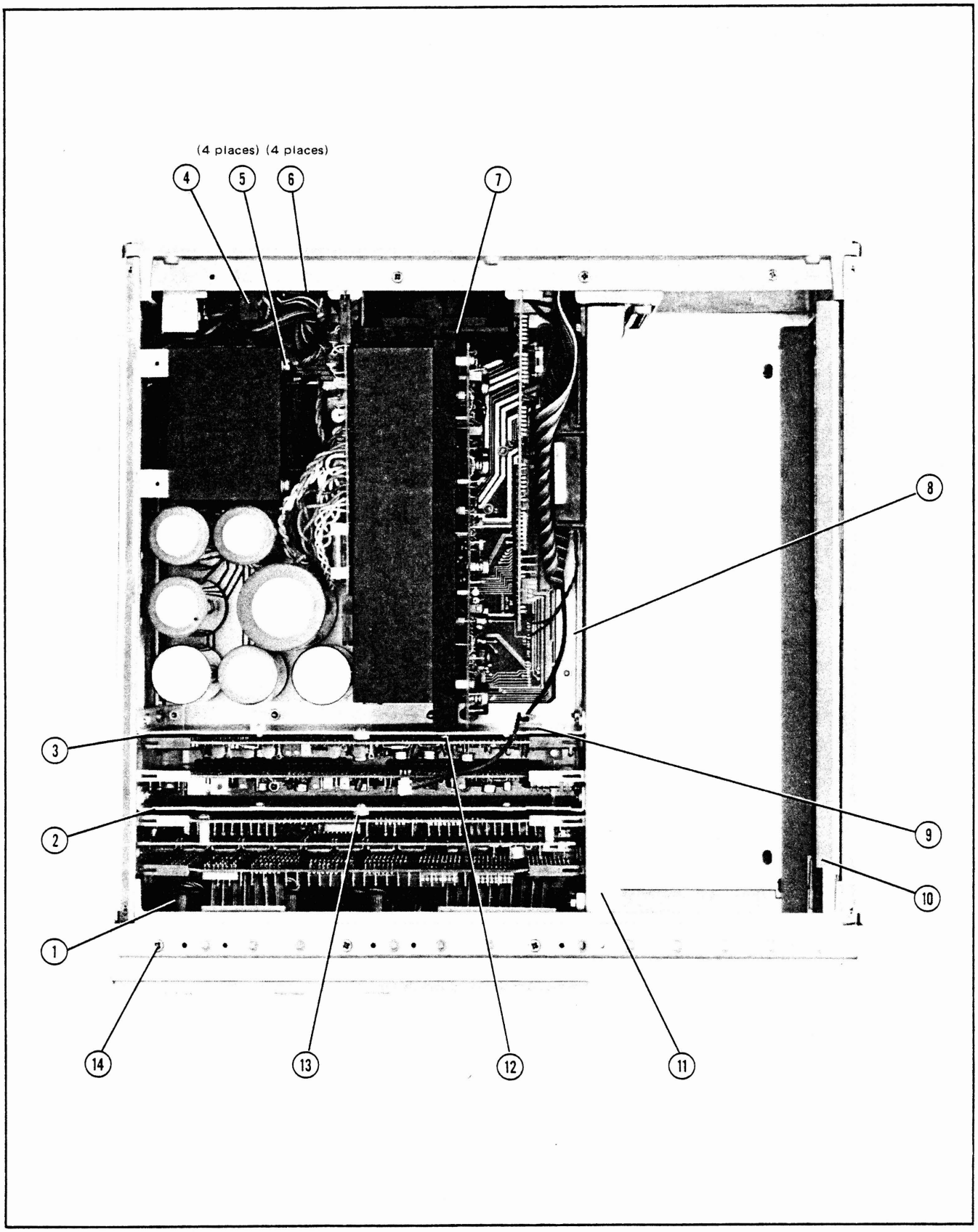


Figure 6-7. Top View Without Covers, Parts Identification (1 of 2)

Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	5060-9444	7	3	Rotary Pulse Generator	28480	5060-9444
2	08350-00024	9	1	Gusset Shield, Front	28480	08350-60024
3	08350-00003	4	1	Gusset Shield, Rear	28480	08350-60003
4	08350-60014	7	1	Fan Cable Assembly	28480	08350-60014
	08350-60033	0	1	400 Hz Fan Cable Assy (Opt 400 only)	28480	08350-60033
5	2680-0253	9	4	Screw Mach 10-32	28480	2680-0253
	3050-0021	5	4	Washer-FL NM No. 8 .188-in.-id	28480	3050-0021
	2190-0034	5	4	Washer - LK No. 10 .193-in.-id	28480	2190-0034
6	1901-0033	2	4	Diode - Gen 180V 200ma DO-7	07263	FDH3369
7	08350-60015	8	1	Fan/Shield Assy	28480	08350-60015
	08350-60032	9	1	400 Hz Fan Assy (Opt 400 only)	28480	03350-60032
8	08350-00006	1	1	Bracket - PC Support	28480	08350-00006
9	1400-0510	8	1	Cable Clamp	02768	8511-01-00-9909
10	08350-00008	3	1	Support, Right	28480	08350-00008
11	08350-00007	2	1	Support, Left	28480	08350-00007
12	2360-0115	4	26	Screw-Mach 6-32 .312-in.-lg	28480	2360-0115
13	0403-0026	6	2	Glide Nylon - fits 0.192 hole	02768	207-120241-03-0101
14	2360-0118	7	5	Screw - Mach 6-32 .375-in.-lg 82 deg	28480	2360-0118

Figure 6-7. Top View Without Covers, Parts Identification (2 of 2)

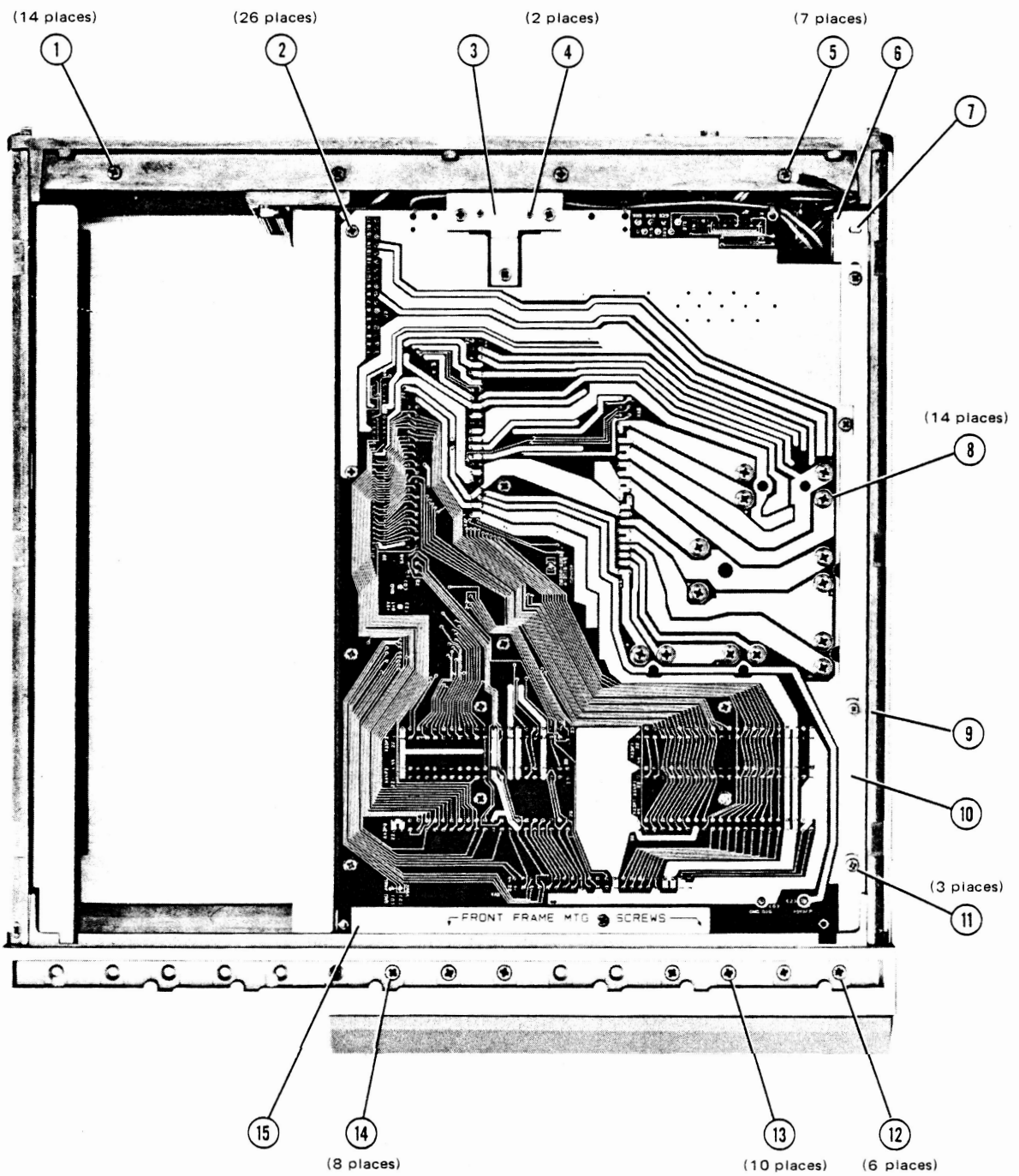
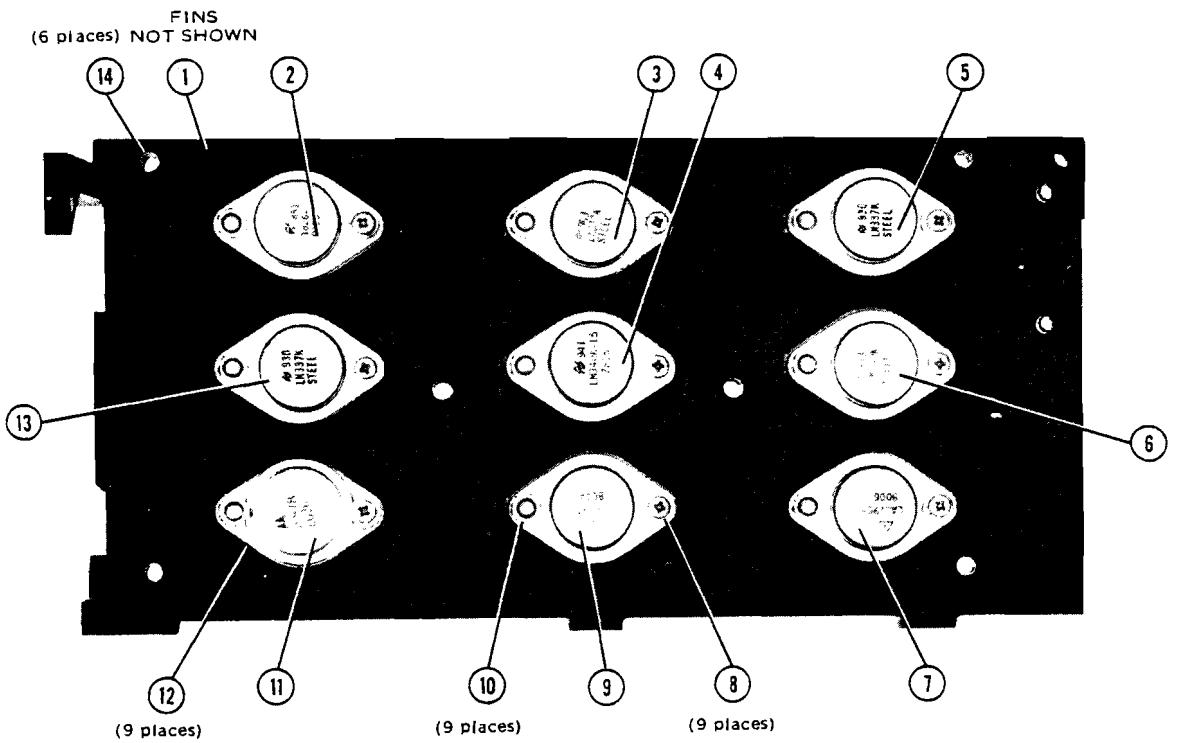


Figure 6-8. Bottom View, Parts Identification (1 of 2)

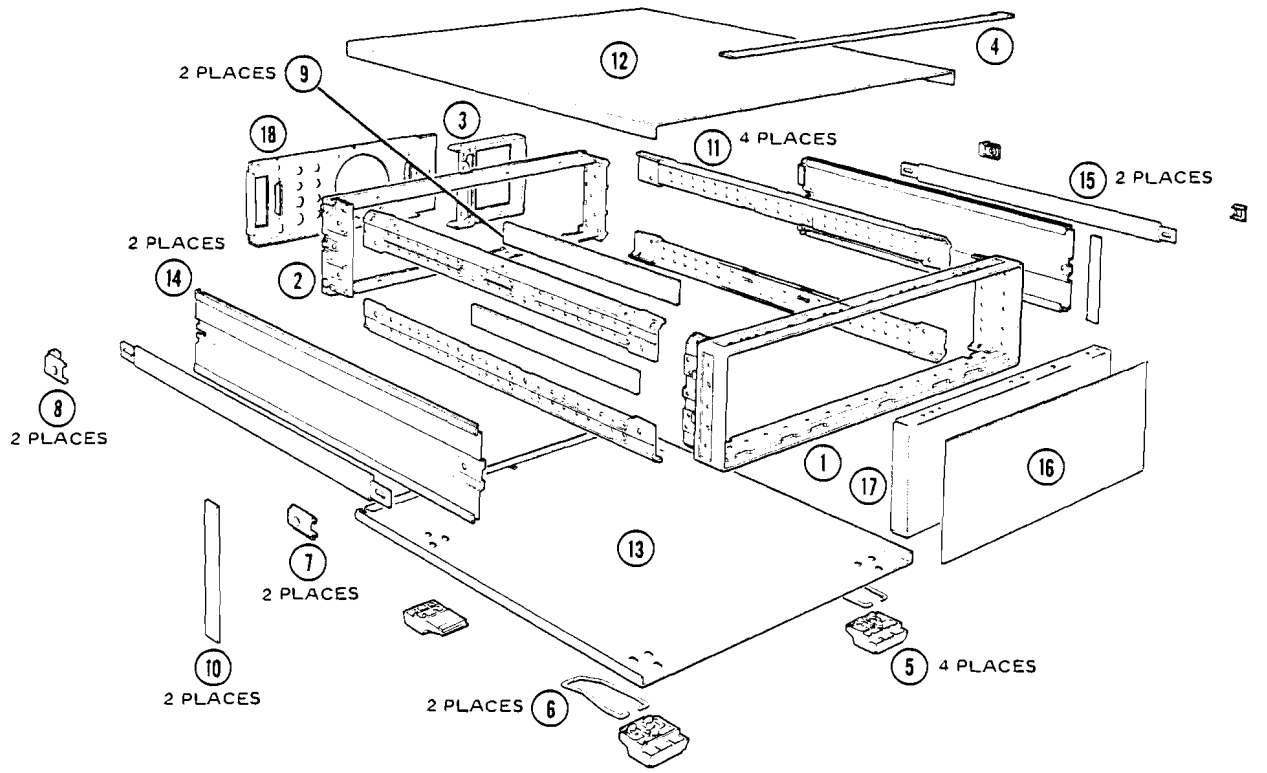
Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	2360-0113	2	14	Screw-Mach 6-32 .25-in.-lg	28480	2360-0113
2	2360-0115	4	26	Screw-Mach 6-32 .312-in.-lg	28480	2360-0115
3	08350-00018	5	1	Bracket, Therm Switch Mnt	28480	08350-00018
	3103-0009	2	1	Switch - Thrm Fxd +150F 5A Opn-On-Rise	82647	20700L 10-205
	4040-1770	3	1	Switch Cap	28480	4040-1770
4	0520-0127	6	2	Screw - Mach 2-56 .188-in.-lg	28480	0520-0127
5	2360-0117	6	7	Screw - Mach 6-32 .375-in.-lg	28480	2360-0117
6	08350-00009	4	1	Bracket - Toggle Switch Mnt	28480	08350-00009
7	3101-2269	6	1	Switch - Toggle DPDT 3A 250 VAC	09353	9201-P3-H-Z-Q
	08350-20009	6	1	Bushing, Thrd	28480	08350-20009
8	2680-0129	8	14	Screw-Mach 10-32 .312-in.-lg	28480	2680-0129
	2190-0011	8	14	Washer - Lk No. 10 .195-in.-id	OG791	1022
9	2200-0143	Ø	1	Screw - Mach 4-40 .375-in.-lg	28480	2200-0143
10	08350-00010	7	1	Lever, Switch Actuator	28480	08350-00010
11	2360-0199	4	3	Screw - Mach 6-32 .438-in.-lg	28480	2360-0199
	2190-0006	1	4	Washer - Lk No. 6 .141-in.-id	28480	2190-0006
	3050-0227	3	3	Washer - Fl Mtlc No. 6 .149-in.-id	28480	3050-0227
	3050-0647	1	3	Washer - Shldr No. 6 .14-in.-id	06540	2638-24850-N140
12	2360-0196	1	6	Screw-Mach 6-32 .375 100 deg	28480	2360-0196
13	2360-0182	5	10	Screw - Mach 6-32 .312-in.-lg 100 deg	28480	2360-0182
14	2360-0192	7	8	Screw - Mach 8-32 .25-in.-lg 100 deg	28480	2360-0192
15	08350-00013	Ø	1	Bracket - Conn Mount	28480	08350-00013

Figure 6-8. Bottom View, Parts Identification (2 of 2)



Ref Desig	HP Part Number	C D	Qty	Description	Mfr. Code	Manufacturer's Part Number
1	08350-20002	9	1	Frame, Heat Sink	28480	08350-20002
	08350-20003	Ø	1	Fins, Heat Sink (not pictured)	28480	08350-20003
2	1826-0722	6	2	(U7), IC Reg-Adj-Pos 1.2/37V TO-3	28480	1826-0722
3	1826-0722	6		(U5), IC Reg-Adj-Pos 1.2/37V TO-3	28480	1826-0722
3	1826-0725	9	1	(U13), IC Fixed Reg 14.4/15.6V TO-3	28480	1826-0725
5	1826-0690	7	2	(U3), IC Reg-Adj-Neg 1.2/37V TO-3	28480	1826-0690
6	1826-0724	8	1	(U10), IC Reg-Adj-Pos 1.2/33V TO-3	28480	1826-0724
7	1826-0513	3	1	(U16), IC Reg-Fxd-Pos 4.9/5.25V TO-3	80103	LAS-1905-001
8	2200-0143	Ø	9	Screw-Mach 4-40 .375-in.-lg	28480	2200-0143
	2190-0003	8	9	Washer-Lk HLCL No. 4 .115-in.-id	28480	3050-0105
	3050-0105	6	9	Washer-Fl Mtlc No. 4 .125-in.-id	28480	3050-0105
	1200-0081	4	9	Insulator bushing .115 D	28480	1200-0081
9	1826-0732	8	1	(U18), IC Reg-Fxd-Pos 5V TO-3	80103	L6-OV-5
10	08350-20004	1	9	Connector Pin, Threaded	28480	08350-20004
	1200-0147	3	9	Insulator Bushing .115 D	28480	1200-0147
	2260-0009	3	9	Nut, Hex 4-40 Thd .094-in.-thk	28480	2260-0009
11	184-0743	Ø	1	(Q6), Transistor-NPN S1 TO-3 PD=150W	01295	2N5878
12*	1200-0043	8	9	Insulator-Transistor, Aluminum	76530	322047
	6040-0454	0	—	Thermal compound; 4-oz. tube	92895	530 1977
13	1826-0690	7		(U15), IC Reg-Adj-Neg 1.2/37V TO-3	28480	1826-0690
14	2360-0209	7	6	Screw-Mach 6-32 1-in.-lg	78480	2360-0209
	2190-0007	2	6	Washer - Lk No. 6 141-in.-id	78189	1906-00

Figure 6-9. Regulator Heatsink, Parts Identification



Reference Designation	HP Part Number	C D	Qty	Description
1	08350-20008	5	1	Front Frame
2	5020-8804	7	1	Rear Frame
3	08350-20011	0	1	Frame, Plug-in Interface
4	5040-7202	9	1	Top Trim, Front Frame
5	5040-7201	8	4	Foot
6	1460-1345	5	2	Tilt Stand
7	5040-7219	8	2	Front Cap, Strap Handle
8	5040-7220	1	2	Rear Cap, Strap Handle
9	08350-00014	1	2	Side Rail Bracket
10	5001-0439	8	2	Side Trim, Front Frame
11	5020-8836	5	4	Corner Strut
12	5060-9834	9	1	Top Cover
13	5060-9836	3	1	Bottom Cover
14	5060-9936	2	2	Side Cover
15	5060-9803	2	2	Strap Handle
16	08350-00001	6	1	Front Dress Panel
17	08350-00002	7	1	Front Sub Panel
18	08350-00004	9	1	Rear Panel
*	5061-2032	7	1	Info Tray
*	08350-90005	9	1	Info Card
* (Not Pictured)				

Figure 6-10. Chassis Parts Identification

SECTION VII
MANUAL BACKDATING CHANGES

7-1. INTRODUCTION

7-2. This manual has been written for and applies directly to instruments with serial numbers prefixed as indicated on the title page. Earlier versions of the instrument (serial numbers prefixed lower than the ones indicated on the title page) may be slightly different in design or appearance. The purpose of this section of the manual is to document these differences.

7-3. With the information provided in this section, this manual can be corrected so that it applies to any earlier version or configuration of the instrument. Later versions of the instrument (serial numbers prefixed higher than the ones indicated on the title page) are documented in a yellow Manual Changes supplement.

7-4. To adapt this manual to an earlier instrument, refer to Table 7-1 and make all of the manual backdating changes listed opposite your instrument serial number or serial number prefix. Perform these changes in the alphabetical sequence listed.

7-5. For additional important information about serial number coverage, refer to INSTRUMENTS COVERED BY THE MANUAL in Section I.

Table 7-1. Manual Backdating Changes by Serial Number Prefix

Serial Prefix	Make Manual Changes
2019A	A
2007A	A and B

7-6. MANUAL CHANGE INSTRUCTIONS

CHANGE A

Page 5-7, Paragraph 5-12:
Replace Paragraph 5-12 with the following procedure:

5-12. AIRFLOW DETECTOR ADJUSTMENT

REFERENCE:

A7 Regulator

DESCRIPTION:

The Airflow Detection circuit senses the internal air flow generated by fan B1 and flags the A3 Microprocessor if the airflow is restricted. The instrument is allowed to warm up to operating temperature and A7R53 is jumpered by a short to remove the hysteresis from

comparator A7U11. A7R58 is then adjusted until the inputs are balanced which will then cause A7U11 output LPST (LOW=POWER SUPPLY TEMPERATURE) to oscillate. LPST is monitored by the A3 Microprocessor and the state of the Airflow Detection circuit is stored in the Status Buffer at hexadecimal location 1000H. A Hex Data Read command (M3) is entered which then displays the current Status Buffer state on the FREQUENCY/ TIME LEDs. When the display LEDs oscillate between 00H and 02H, A7R58 is adjusted correctly.

PROCEDURE:

1. Remove the RF plug-in from the sweep oscillator mainframe.

2. Position the sweep oscillator upright and remove top cover.

3. Set the LINE switch to ON and allow the sweep oscillator to warm up for 30 minutes.

4. Connect a shorting jumper across A7R53. This removes the hysteresis from comparator A7U11. Refer to Figure 5-3 for the location of A7R53.

5. Replace the top cover and allow the instrument to operate with all covers in place for 5 minutes.

6. Press SHIFT 0 0 M1 1 0 0 0 M3. This enables the hexadecimal data in the Status Buffer (at address location 1000H) to be displayed on the front panel FREQUENCY/TIME LEDs. The LED display should now read 1000 00 or 1000 02.

7. Remove the top cover and quickly adjust A7R58 AIRFLOW BAL until the LED display oscillates between 1000 00 and 1000 02. Refer to Figure 5-3 for A7R58 adjustment location.

NOTE

The A7R58 AIRFLOW BAL adjustment MUST be made with the 8350A at normal operating temperature. The top cover should only be removed for a short period of time to make the actual adjustment.

8. Replace the top cover and wait 1 minute after adjustment to insure that the display still oscillates. If it does not, and has settled at 1000 00 or 1000 02, repeat steps 6 and 7.

9. Remove jumper from A7R53.

10. Verify that the display indicates 1000 00.

CHANGE A (Cont'd)

Page 5-8, Figure 5-3:
Replace Figure 5-3 with the following figure:

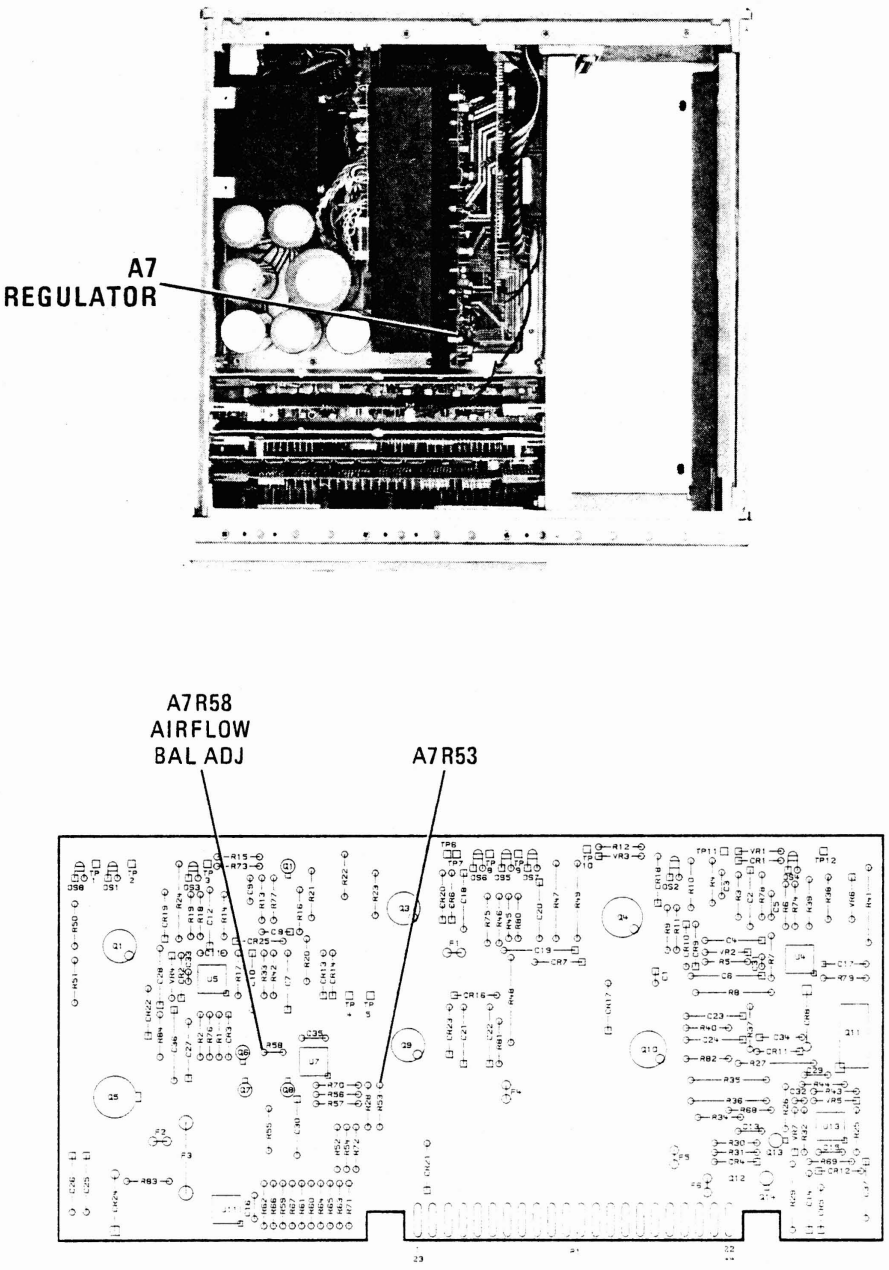


Figure 5-3. Location of AIRFLOW BALance Adjustment

CHANGE A (Cont'd)

Page 8-83, Figure 8-54:
In Function Block (B), move TP4 to the inverting input of U11, and TP5 to the noninverting input of U11.

CHANGE B

Page 6-18, Table 6-2:
Change A7C3, A7C9, A7C13, A7C16, and A7C35 to HP Part No. 0160-0945, CD 2, CAPACITOR-FXD 910PF ±5% 100VDC MICA.
Change A7C17 and A7C34 to HP Part No. 0180-2620, CD 6, CAPACITOR-FXD 2.2UF ±10% 50VDC TA.
Delete A7C41 through A7C49.

Page 6-19, Table 6-2:
Delete A7CR26.
Change Reference Designator DS1 to DS9.

Page 6-19 and 6-20, Table 6-2:
Make the following Reference Designator changes:

Table 7-2. A7 Reference Designator Conversion

From	To	From	To	From	To
Q1	Q2	U1	Q1	U11	U7
Q2	Q6	U2	U5	U12	Q9
Q3	Q7	U3*	U1*	U13*	U8*
Q4	Q8	U4	Q3	U14	Q10
Q5	Q11	U5*	U2*	U15*	U9*
Q6*	Q12*	U6	Q4	U16	U10
Q7	Q13	U7*	U3*	U17	U11
Q8	Q14	U8	U4	U18*	U12*
		U9	Q5	U19	U13
		U10	U6		

*Indicates heat sink loaded components.

Page 6-19, Table 6-2:
Change A7R26 to HP Part No. 0698-3154, CD 0, RESISTOR 4.22K 1% .125W F TC = 0±100, MFR PART NO. C4-1/8-TO-4221−F.
Change A7R45 to HP Part No. 0698-3442, CD 9, RESISTOR 237 1% .125W F TC = 0±100, MFR CODE 24546, MFR PART NO. C4-1/8-TO-237R-F.

Page 6-20, Table 6-2:
Change A7R46 to HP Part No. 0757-0278, CD 9, RESISTOR 1.78K 1% .125W F TC=0±100, MFR PART NO. 0757-0278.

CHANGE B (Cont'd)

Change A7R59, A7R63, and A7R64 to HP Part No. 0698-3157, CD 3, RESISTOR 19.6K 1% .125W F TC=0±100, MFR CODE 24546, MFR PART NO. C4-1/8-TO-1962-F.
Change A7R60 and A7R65 to HP Part No. 0698-3156, CD 2, RESISTOR 14.7K 1% .125W F TC=0±100, MFR CODE 24546, MFR PART NO. C4-1/8-TO−1472-F.
Add A7R75, HP Part No. 0698-3136, CD 8, RESISTOR 17.8K 1% .125W F TC=0±100, MFR CODE 24546, MFR PART NO. C4-1/8-TO-1782-F.
Delete A7R85 through A7R87.
Add A7TP12, HP Part No. 0360-0535, CD 0, TERMINAL TEST POINT PCB.

Page 8-78 through Page 8-80:
Change all A7 reference designators as per Table 7-2, above.

Page 8-78:
Under the subheading **−15V Regulator**, delete two sentences:
"The regulator output voltage..... shorted to ground."

Under the subheading **+10V Regulator**, after "..... and current through A7R46," add the following: ... and parallel resistor A7R75.

Page 8-83, Figure 8-51:
Change TP11 to TP12. (TP11 will not appear on the block diagram.)

Page 8-83, Figure 8-52:
Replace Figure 8-52 with the Component Locations Diagram in this section.
Change the reference designators on each of the nine heatsink-loaded regulators as per Table 7-2.

Page 8-83, Figure 8-54:
Make the following changes to the A7 Regulator schematic:

1. Change reference designations as indicated by Table 7-2 above.

2. Value Changes.

Reference Designator	Value
C3, C9, C13, C16, and C35	910 pF
C34	2.2 μF
R26	4220Ω
R45	237 Ω
R59, R63, R64	19.6 kΩ
R60, R65	14.7 kΩ

3. In Function Block ①: Change TP11 to TP12.

CHANGE B (Cont'd)

4. Add:

   In Function Block Ⓒ: TP11 between R74 and the wiper of R10.
   In Function Block Ⓔ: R75, 17.8K, in parallel with R46.

5. Delete:

   In Function Block Ⓐ: R87 and the +5VB line.
   In Function Block Ⓒ: C48.
   In Function Block Ⓕ: C41, C42, C45, and C47.
   In Function Block Ⓗ: C46, CR26, R85, and R86. (U9, pin 1 is shorted to ground.)
   In Function Block Ⓘ: C43, C44, and C49.

6. Change NOTE 4 to read: "Heat Sink Mounted Components are: U1, U2, U3, U6, U8, U9, U10, U12, and Q12."

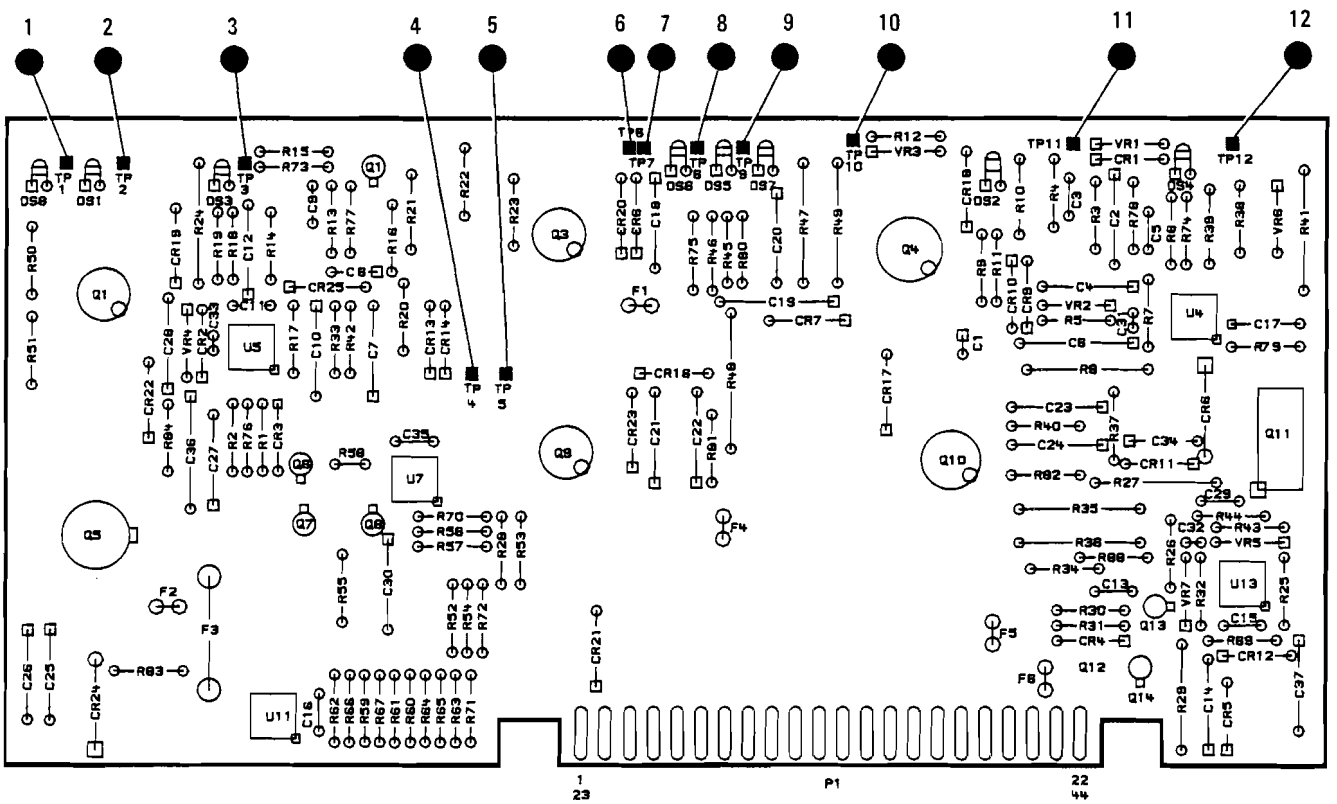


Figure 8-52. A7 Component Locations Diagram (CHANGE B)

SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section provides instructions for troubleshooting and repairing the Model 8350A Sweep Oscillator. Information includes circuit descriptions, troubleshooting procedures, block diagrams, schematics, and component location maps for each PC board assembly.

8-3. SERVICE SHEETS

8-4. Each service sheet pertains to a specific assembly and contains the information listed above. Service sheets are arranged in assembly number order from A1 to A9. Table 8-1 provides a Service Sheet Index.

Table 8-1. Service Sheet Index

Information	Figure Number
A1 Front Panel Assembly	
Circuit Description (Includes A1 and A2)	—
Troubleshooting (Includes A1 and A2)	—
A1 Component Locations	8-13
Block Diagram (Includes A1 and A2)	8-17
A1 Schematic	8-14
A2 Front Panel Interface Assembly	
Circuit Description (Includes A1 and A2)	—
Troubleshooting (Includes A1 and A2)	—
Block Diagram (Includes A1 and A2)	8-17
A2 Component Locations	8-18
A2 Schematic	8-23
A3 Microprocessor Assembly	
Circuit Description	—
Troubleshooting	—
Block Diagram	8-25
Component Locations	8-26
Schematic	8-29
A3A1 PROM Assembly	
Circuit Description	—
Troubleshooting	—
Component Locations	8-30
Schematic	8-30A
A4 Scaling and Marker Assembly	
Circuit Description	—
Troubleshooting	—
Block Diagram	8-34
Component Locations	8-35
Schematic	8-38

Information	Figure Number
A5 Sweep Generator	
Circuit Description	—
Troubleshooting	—
Block Diagram	8-39/44
Component Locations	8-40/45
Schematic (2 fold-outs)	8-43
A6 Rectifier Assembly	
Circuit Description (Includes A6 and A7)	—
Troubleshooting (Includes A6 and A7)	—
A6 Component Locations	8-49
A6 Schematic	8-50
A7 Regulator Assembly	
Block Diagram (Includes A6 and A7)	8-51
A7 Component Locations	8-52
A7 Schematic	8-54
A8 HP-IB Interface Assembly	
Circuit Description	—
Troubleshooting	—
Block Diagram	8-56
Self-Test Block Diagram	8-57
Component Locations	8-58
Schematic	8-60
A9 Motherboard	
Component Locations	8-61
Wiring List	8-62
Major Assemblies Locations	8-63
Cable List (*Table)	*8-35

8-5. Service Sheets fold out and up to facilitate access to reference material. Block diagrams appear on the fold-down apron. Component location maps, PC board pin-edge connections, and pertinent circuit information (e.g., waveforms) are found on the fold-up apron of the service sheet, with the schematic directly below. Circuit description and assembly level troubleshooting are located on pages immediately preceding the service sheet.

8-6. SCHEMATIC DIAGRAM NOTES

8-7. Figure 8-1, Schematic Diagram Notes, provides definitions to schematic symbols.

8-8. INTERCONNECT CABLES AND MNEMONICS

8-9. All interconnect cables and their associated connectors are listed in Table 8-35, located within the A9 Service Sheet.

8-10. Table 8-62 alphabetically lists and defines all 8350A signal mnemonics, references the point-to-point distribution of each signal to and from the PC board sockets and the cable connectors on the A9 Motherboard assembly, and identifies the signal source. This table is located on the A9 Service Sheet.

8-11. TROUBLESHOOTING

WARNING

With the ac power cable connected, the ac line voltage is present at the terminals of power line module FL1 (mounted on rear panel) and at the LINE switch, whether the LINE switch is on or off. With the covers removed, these terminals are exposed. Care must be taken to avoid contact with these terminals.

With the covers removed, terminals are exposed that have voltages capable of causing death. Any maintenance or repair of the opened instrument under voltage should be carried out only by a skilled person who is aware of the hazard involved.

After disconnecting ac line power cord, allow a minimum of 30 seconds for the power supplies to discharge before removing the protective cover. However, be aware that the −40V supply has no path for dissipation. This supply must be manually discharged before any repairs are attempted.

CAUTION

Improper methods of discharging the −40V supply will result in damage to the instrument. See Figure 8-6 for procedure.

8-12. Troubleshooting is generally divided into two maintenance levels in this manual. The first level isolates the problem to a circuit or assembly. Self-Test (described in paragraph 8-14), together with the Overall Block Diagram and Troubleshooting hints, helps to isolate the problem source to a particular assembly.

8-13. The second maintenance level isolates the trouble to the component. Operator-initiated tests (paragraph 8-18), schematic diagrams, and circuit descriptions for each assembly aid in troubleshooting to the component level.

8-14. Self-Test

8-15. 8350A software provides microprocessor and operator-initiated checks. These checks verify the proper functioning of the majority of the 8350A's digital circuitry and a portion of the analog devices.

BASIC COMPONENT SYMBOLOGY

R, L, C — Resistance is in ohms, inductance is in microhenries, capacitance is in microfarads, unless otherwise noted.

P/O — Part of.

✳ — Indicates a factory selected component.

Panel Control.

Screwdriver adjustment.

Encloses front panel designation.

Encloses rear panel designation.

Circuit assembly borderline.

Other assembly borderline.

Heavy line with arrows indicates path and direction of main signal.

Indicates path and direction of main feedback.

Earth ground symbol.

Assembly ground. May be accompanied by a number or letter to specify a particular ground.

Chassis ground.

n — Represents n number of transmission paths.

Test Point: Terminal provided for test probe.

Pin Edge Connector output of PC board.

Indicates wire or cable color code. Color code same as resistor color code. First number indicates base color, second and third numbers indicate colored stripes.

Indicates shielding conductor for cables.

Indicates a plug-in connection.

Indicates a soldered or mechanical connection.

Connection symbol indicating a male connection.

Connection symbol indicating a female connection.

Resistor.

Variable Resistor.

General purpose diode.

Breakdown Diode: Zener

Light-Emitting Diode.

SCR (Silicon Controlled Rectifier).

FET: Field Effect Transistor (N-channel).

FET: Field Effect Transistor-Guarded gate- (N channel).

Dual Transistor.

Transistor NPN

Transistor PNP

Electrolytic Capacitor.

Toroid: Magnetic core inductor.

Operational Amplifier.

Fuse

Pushbutton Switch.

Toggle Switch.

Thermal Switch.

Summing Point.

Oscillator; RPG (Rotary Pulse Generator).

B1 — Fan, Motor.

Toroidal Transformer

LOGIC SYMBOLOGY

& — AND Gate

≥1 — OR Gate

& — NAND Gate

≥1 — NOR Gate

=1 — Exclusive OR Gate

Buffer/Amplifier

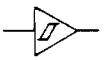
Inverter

Negation symbol. Line is active low.

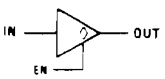
Indicated edge-sensitive input.

Figure 8-1. Schematic Diagram Notes (1 of 3)

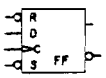
INTEGRATED CIRCUIT SYMBOLOGY



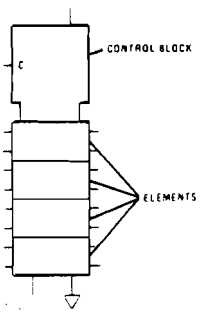
Schmitt Trigger: The gate of the Schmitt Trigger switches at different points for positive - and negative-going signals. The difference between the positive and negative thresholds is defined as hysteresis voltage.



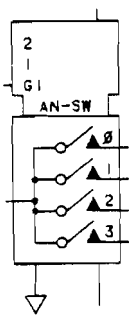
3-State Buffer: Three States:
Enable (EN) Input low: High impedence output.
Enable input high: Output = 0 or
Output = 1



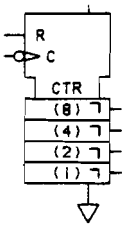
Data Flip-Flop: Set (S) and Reset (R) are asynchronous controls. Active S sets the noninverting output high and the inverting output (○—) low; active R resets both outputs. When S and R are both inactive, the outputs remain latched in the last state. An active clock (—▷) enables the D input, at which time the noninverting output = D, and the inverting output = $\bar{D}$.



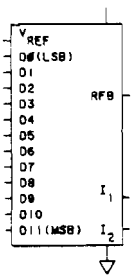
Control Block: All controlling inputs (gates, clocks, inhibits, etc.) connect to the control block.
Elements: Can be one or more of any logic function (flip-flop, counter, gate, RAM, etc.). Data inputs are on the left side of element, data outputs on the right.



Analog Switch: Control lines 1 and 2 decode to select one of four inputs. G1, high=enable.



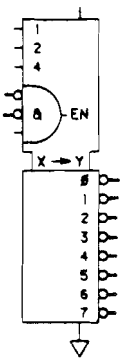
Counter: Binary-weighted registers count on the falling edge of each clock pulse. Active (high) R clears all registers.



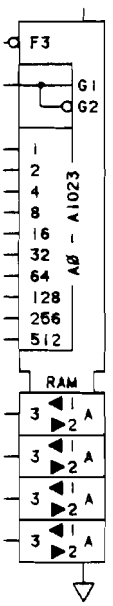
Digital to Analog Converter (DAC): Provides a scaled current output (I_1), the product of V_{REF} and the fractional binary input:

$D_{11}2^{-1} + D_{10}2^{-2} + D_9 2^{-3} + \ldots D_0 2^{-12}$

The product of V_{REF} and complement of the binary input appears at I_2.



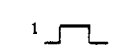
Decoder: The logic states of the three select lines A, B, and C, and the three enable inputs (EN), determine which one of the eight outputs will be decoded. The selected output will be low, while all others are high.



Random-Access Memory (RAM): Binary addresses (A0 to A9) access one of 1024 registers in RAM. When G1 is high, bits appearing at D0 to D3 will be written to the addressed location (A0 to A9). When G2 is low, bits appearing at D0 to D3 have been accessed from the addressed location.

Figure 8-1. Schematic Diagram Notes (2 of 3)

FUNCTION LABEL ABBREVIATIONS

Σ	Adder	◇	Open Collector	LED	Light-Emitting Diode
	Amplifier/Buffer		Monostable Multivibrator	MUX	Multiplexer
	Schmitt Trigger	BCD	Binary Coded Decimal	RAM	Random-Access Memory
&	AND	CTR	Counter	REG	Register
≥1	OR	DAC	Digital-to-Analog Converter	ROM	Read Only Memory
=1	Exclusive OR	FF	Flip-Flop	RPG	Rotary Pulse Generator
X→Y	Encoder, Decoder	I/O	Input/Output		

LINE LABEL ABBREVIATIONS

CK, C	Clock Input	MSB	Most Significant Bit	T	Trigger Input (Monostable)
D	Data or Delay Input (Flip-Flop)	Q	Output	WR	Write
EN	Enable	$\overline{Q}$	Not Q Complement of Q	+1	Count Up
F	3-State Enable Input	R	Reset or Clear Input	−1	Count Down
G	Gating Input	RD	Read	3-ST	3-State (placed by function)
LSB	Least Significant Bit	S	Set Input		

Figure 8-1. Schematic Diagram Notes (3 of 3)

*Table 8-2. *Self-Test Index*

Functions Tested	Error Code	** Local Operator Initiation
A3 Microprocessor	*** E015	none
RAM	*** E014 to E011	SHIFT 07
ROM	*** E010 to E007	SHIFT 06
Front Panel Bus	*** E006	SHIFT 08
Instrument Bus	E005	SHIFT 09
Power Supply	E004	none
VTUNE vs. Marker	E003	SHIFT 10
Sweep vs. Marker	E002	SHIFT 11
Plug-in Bus	E001	SHIFT 12

* SELF-TEST is initiated by "power-on", or by pressing INSTR PRESET.

** To access a particular check, make the appropriate keyboard entry. The test will recycle continuously until locally interrupted. (i.e., INSTR PRESET).

*** May only be displayed on A3 Microprocessor LEDs. However, if repeated initialization of SELF-TEST results in different error codes, suspect a ROM failure.

8-16. Whenever the 8350A is powered-on, or the front panel INSTR PRESET pushbutton is pressed, instrument Self-Test is initiated. Instrument Self-Test checks the A3 Microprocessor assembly, I/O busses and several analog signals. If a failure is detected during Self-Test, the appropriate error code will be displayed in one or all of the following locations: front panel Digital Display, front panel Sweep Trigger annunciators, and the four LEDs atop the A3 Microprocessor assembly. (The A3 LEDs are the most reliable source of error codes). Sweep Trigger and A3 LEDs display the error code in binary form; ON=1. For example, error code E006 would be displayed as 0110, or OFF-ON-ON-OFF. Table 8-2 cross references each functional area exercised by Self-Test with its local operator-initiated key signals and error code.

8-17. If the front panel display, Sweep Trigger annunciators, or A3 LEDs indicate an error code, refer to the Overall Block Diagram and Troubleshooting section, located in front of the A1 Service Sheet. This section will help the operator to define the troubled area.

8-18. OPERATOR-INITIATED TESTS

8-19. The microprocessor services several operator-initiated tests to check functions which are not exercised during Self-Test. Initiate the test by making the appropriate key entry indexed in Table 8-3. For further description of these tests, refer to the Overall Block Diagram.

Table 8-3. Operator-Initiated Tests

Test	Key Entry	Reference
Key Codes	SHIFT 04	A1/A2 Service Sheet
Display Exercise Routine	SHIFT 05	A1/A2 Service Sheet
CW DAC	SHIFT 13	A4 Service Sheet
ΔF DAC	SHIFT 14	A4 Service Sheet
Sweep vs. ΔF DAC	SHIFT 15	A4 Service Sheet
Marker DAC	SHIFT 16	A4 Service Sheet
RPG Circuit	SHIFT 17	A1/A2 Service Sheet
Front Panel Lamps	SHIFT 18	A1/A2 Service Sheet
Vernier DAC	SHIFT 19	A4 Service Sheet

8-20. Access to most of the 8350A digital circuitry can be achieved through local programming.

Function	Key Entry
Hex Address Entry	SHIFT 0 0 M1 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*To address a different location, press M1 and enter the new address, or use the increment keys ◂ ▸ to step to the new address.

By entering the Hex address location of a specific device, that device can be exercised. (Addresses are supplied next to the mnemonic on each schematic. Also, circuit descriptions usually include Address Decoder Tables to define the addresses used on that particular assembly.) Hex Address Entry must be made prior to any of the following:

NOTE

Before addressing an 8350A component, determine whether or not the Microprocessor can READ or WRITE to that particular device. The majority of 8350A digital chips do NOT have both READ and WRITE capabilities.

- HEX DATA WRITE, M2, allows the operator to write any combination of hex data bytes to the addressed device. The outputs can then be checked to see if the device is functioning properly.
- HEX DATA READ, M3, allows the operator to read the outputs of an addressed device.
- HEX DATA ROTATION WRITE, M4, strobes a '1' (high state) through a column of zeroes (low states) to the addressed device. In effect, Hex Data Rotation Write is a rapid WRITE mode, exercising the addressed device in real time. The microprocessor inputs the data continuously, without servicing interrupts from the rest of the instrument. Latch enable lines, inputs, and outputs can be checked in this mode. Figure 8-2 illustrates the appropriate waveforms.

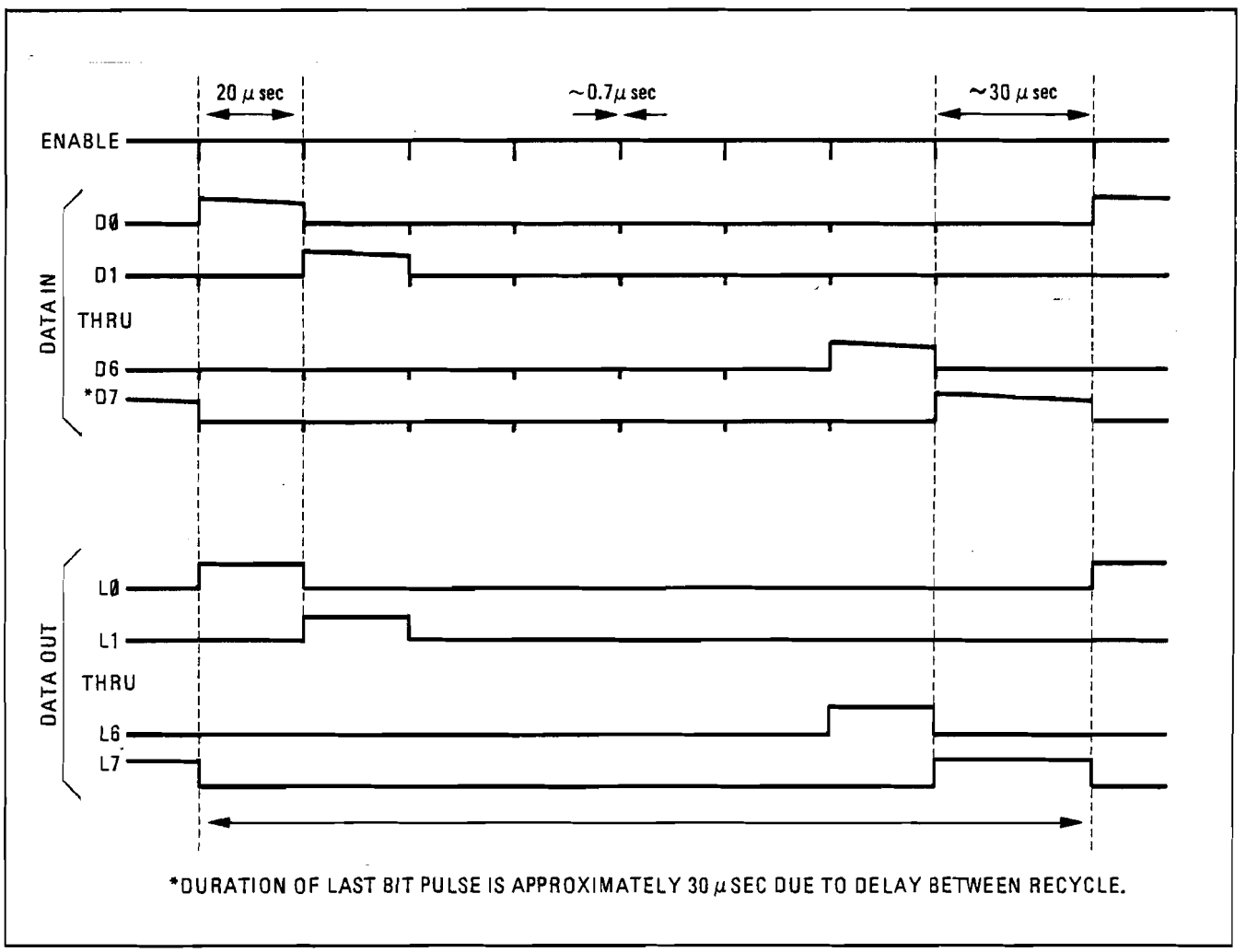


Figure 8-2. Hex Data Rotation Write – Bit Pattern

- HEX ADDRESSED FAST READ, M5, provides an operator-initiated check for verification of the data bus, in which the addressed device is clocked in real time. Latch outputs can be traced from the on-board location back through the data bus to the microprocessor. At each buffer, verify TTL level response to the enable pulse. Enable line waveforms are shown in Figure 8-3.

8-21. HEXADECIMAL

8-22. Hexadecimal is the number system used to locally address 8350A logic components. Available programmed checks were indexed in Table 8-3.

8-23. The hexadecimal system uses 16 digits: 0 through 9 and A through F. Since 16 is the fourth power of 2, 4-bit binary numbers can be expressed with one hexadecimal digit, making local programming easier. Table 8-4 provides hexadecimal conversion.

8-24. When the 8350A is in the Hex Data WRITE mode (see paragraph 8-20), several front panel keyboard pushbuttons function as hexadecimal digits. See Figure 8-4.

8-25. RECOMMENDED TEST EQUIPMENT

8-26. Test equipment required to maintain the Model 8350A is listed in Section I. If the equipment listed is not available, equipment that meets the minimum specifications shown may be substituted.

Table 8-4. Hexadecimal Equivalents

Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
b	1011	11
C	1100	12
d	1101	13
E	1110	14
F	1111	15

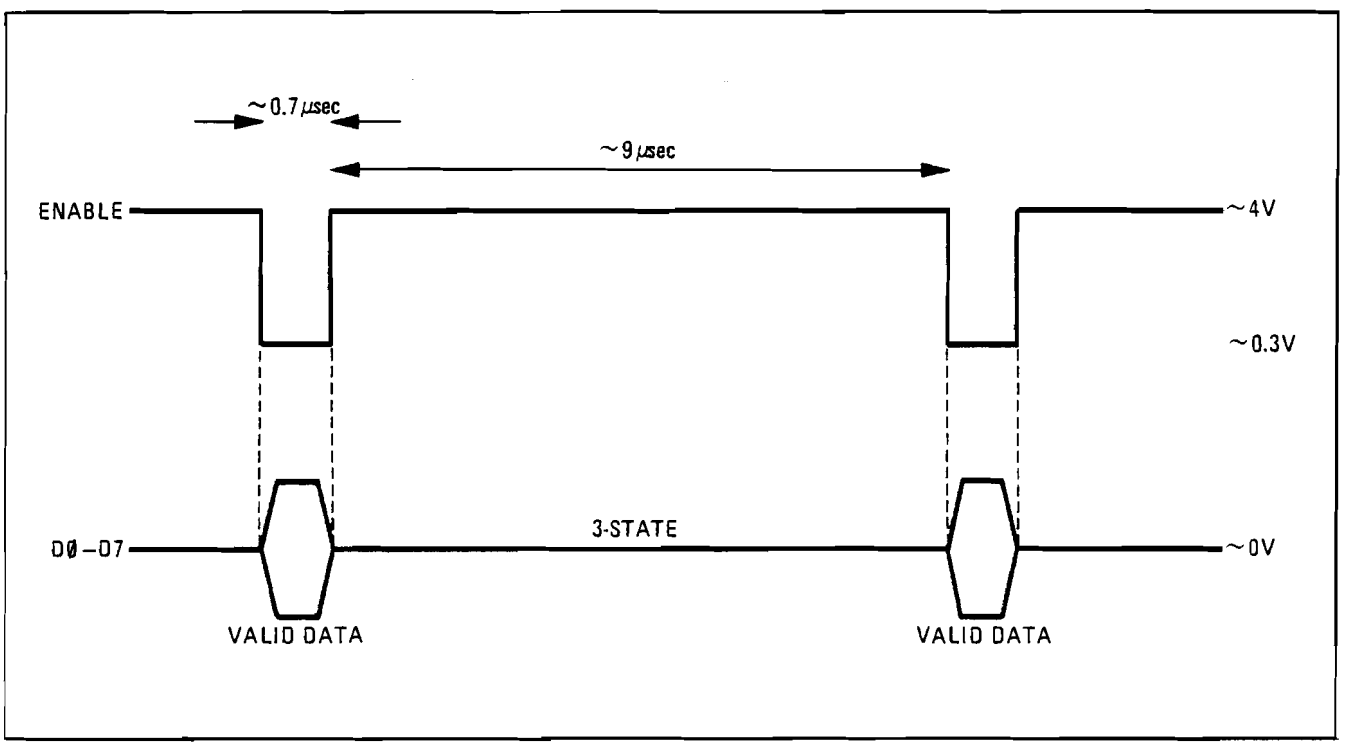


Figure 8-3. Hex Addressed Fast Read – Timing Diagram

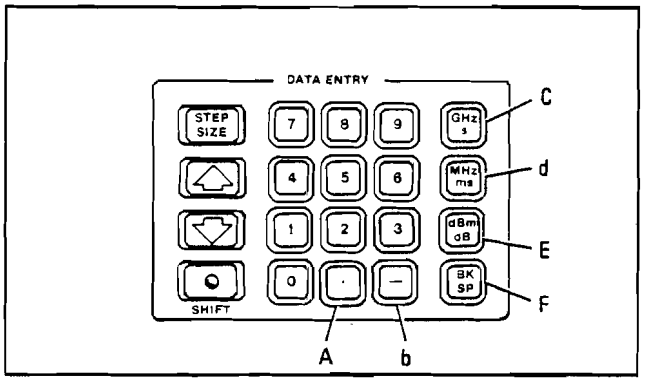


Figure 8-4. Hex Entry Keys

8-27. AFTER-SERVICE PRODUCT SAFETY CHECKS

8-28. Visually inspect interior of instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy cause of any such condition.

8-29. Using a suitable ohmmeter, check resistance from instrument enclosure to ground pin on power cord plug. The reading must be less than one ohm. Flex the power cord while making this measurement to determine whether intermittent discontinuities exist.

8-30. Check resistance from instrument enclosure to line and neutral (tied together) with the line switch ON and the power source disconnected. The minimum acceptable resistance is 2 megohms. Replace any component which results in failure to meet this minimum.

8-31. Check line fuse to verify that a correctly rated fuse is installed.

8-32. REPAIR

8-33. Paragraph 8-34 and the following figures provide written instructions and/or illustrations to aid in servicing the instrument.

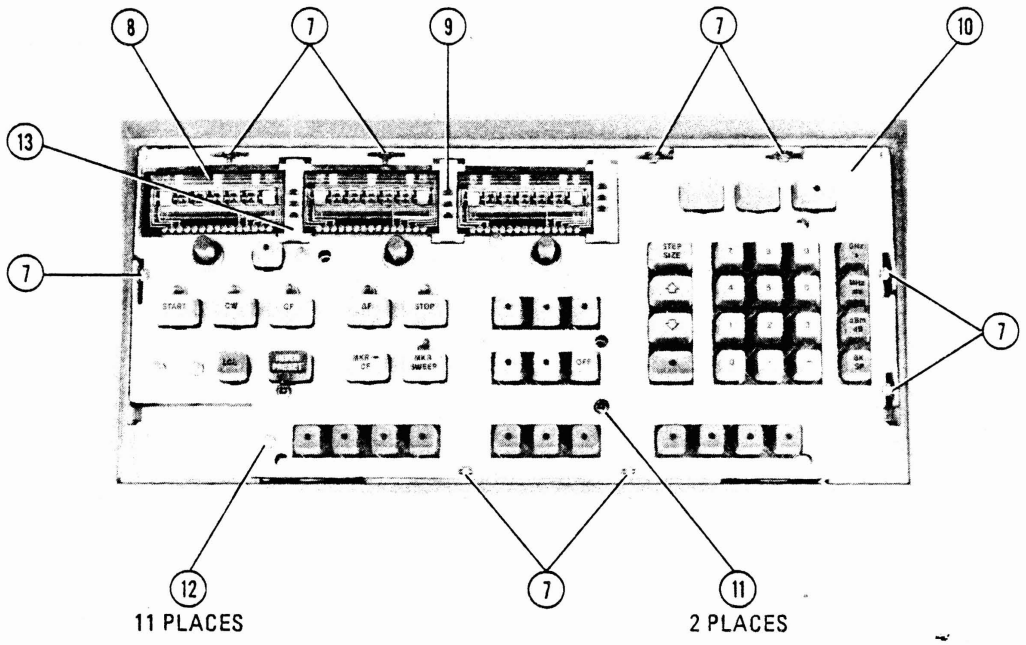
8-34. Air Filter Cleaning

WARNING

The following procedure must be performed periodically to retain the safety features which have been designed into the instrument.

8-35. The metal filter, attached to the cooling fan (rear panel), will require periodic cleaning. Due to the variety of environmental conditions, the interval between cleanings cannot be estimated. Error signal E016 indicates increased temperatures in the cooling system caused by reduced air flow. When this error is displayed, a clogged filter may be the reason. Clean as follows:

1. Disconnect line power cord.
2. Remove four screws holding air filter to rear panel.
3. Brush dust off screen. Blow compressed air in the opposite direction of normal air flow; or wash with mild soap and water, then dry.



1. Turn LINE switch to OFF and remove AC power cord from rear panel.

2. Remove top and bottom covers, trim strip, and RF plug-in.

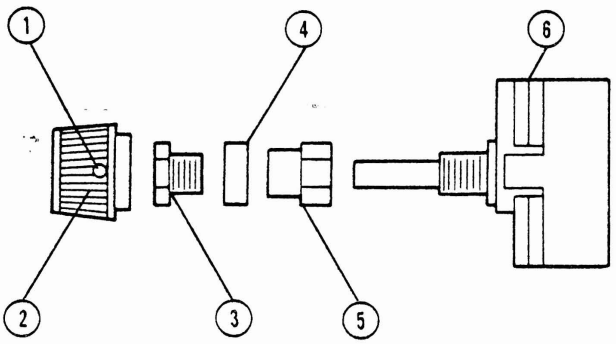
3. Remove seven flat-head screws from front frame: three under top trim; two from bottom of frame (note arrows on bracket); and two from left support, inside plug-in opening.

4. Remove A2 board and disconnect ribbon cables.

5. Remove two pan-head screws (located under A2) connecting Front Panel +5V (red) and ground (black) wires to the mother board.

6. The front panel assembly is now free from the cabinet. From inside the box, gently push the front panel assembly through the frame.

7. Remove retaining clips from the five dress panel studs (backside of A1 board).



8. Loosen two set screws ① to remove each of the round front panel knobs ②. Remove the exposed hex nuts ③ with a 7/16" socket.

9. Ease dress panel from assembly by pushing gently on the dress panel studs protruding from A1.

10. Remove spacer ring ④ from each RPG shaft.

NOTE

In the following step, removal of hex screws is facilitated by using a hex balldriver, HP Part Number 8710-0523, CD7.

Figure 8-5. Front Panel Disassembly (1 of 2)

11. Remove nine screws ⑦ from hold down plate ⑩. Remove two screws from back of A1 board. Remove hold-down plate ⑩ and A1 assembly from frame. Remove two screws ⑪ from middle of hold down plate and separate hold down plate from A1 board assembly.

RPG Replacement

12. Desolder four wires from the back of A1, corresponding to the defective RPG.

13. Remove 7/16" hex nut ⑤ and lock washer. Remove RPG ⑥.

14. To install new RPG, reverse the procedure.

15. To reassemble front panel, reverse steps 1 through 11. When replacing the hold-down plate and dress panel, carefully position the yellow LEDs ⑫ before applying pressure to the plates.

Numeric Display Replacement

The numeric display consists of three interlocking chips. To replace the center chip one of the outer chips must first be removed.

16. Gently lift up and out on the outermost display chip ⑧. To free the chip, lift up slightly on the white plastic light housing ⑬.

17. To install new display chips, reverse the procedure. Take care when replacing light housings to avoid bending fragile LED leads ⑫.

NOTE

Display assemblies may crack if flexed. Do not bend. Also, to prevent display assembly from see-sawing, always apply pressure across two points.

18. Apply pressure on the chip until it is firmly seated in the jack.

19. Replace hold-down plate and dress panel. Carefully align yellow LEDs ⑫ before seating either plate.

    The following procedure checks display continuity before reassembling front panel.

    a. Connect +5V (red) and ground (black) wires to motherboard.

    b. Replace A2 and reconnect ribbon cables.

    c. Apply AC line power to 8350A.

    d. Press SHIFT 0 5 to initiate Display Exercise Routine (see A1/A2 Service Sheet). This routine should reveal any connection problems.

20. Remove AC power cord. Reverse steps 1 through 8 to reassemble Front Panel.

Keyboard Switch Replacement

21. Remove button from defective switch.

22. Cut off plastic feedthrough "nubs" from backside of A1 assembly. Remove switch.

23. Replace new switch. Melt plastic pins with soldering iron to hold switch to pc board. Replace key.

24. To reassemble Front Panel reverse steps 1 through 11. Carefully align dress panel and hold down plate ⑩ before applying pressure to avoid bending the yellow LEDs ⑫.

25. Verify proper functioning of new switch by performing the Key Code test. Press SHIFT 0 4. Then press the key corresponding to the new switch. The proper key code, listed in Table 8-9 of the A1/A2 Service Sheet, should appear in the front panel FREQUENCY/TIME display window.

Figure 8-5. Front Panel Disassembly (2 of 2)

1. Remove AC power cord.

WARNING

Before attempting this procedure, manually discharge the −40V supply as described in step 2 below.

CAUTION

Do not attempt to discharge the −40V supply capacitor through chassis ground. Use only the method prescribed below, or damage to the instrument will result.

2. Set instrument on its top side. Remote 8350A bottom cover. Provide a discharge path for the −40V supply capacitor by applying a 0.5 watt, 100 ohm resistor (via shielded clip leads) between the two motherboard-capacitor screws ③ for a period no less than 1 second. This method painlessly discharges the −40V supply.
3. Remove three aligned screws: one connecting thermal switch bracket to heat sink②; two connecting heat'sink to mother board①.
4. Remove top cover. Disconnect W3 (brown coaxial cable) from A4 board. Remove PC board cover and A5 board.
5. Remove screw holding heat sink to gusset shield (behind A5).
6. Remove air filter screen (rear panel) to reveal two screws marked HEAT SINK. Remove these two screws and lift heat sink and A7 assembly from mainframe box.
7. Remove six screws from the A7 board. Heat sink frame, fins and A7 will pull apart.
8. Be sure both sides of insulator shields are coated with a thin layer of thermal compound, HP Part Number 6040-0454. Before installing new regulators, straighten IC leads in the holes provided on the heat sink frame.
9. Check isolation between regulator casing and heat sink frame. Reading should be greater than 2 megohms.
10. To replace Regulator heatsink, reverse above procedure.

Figure 8-6. Regulator/Heat Sink Replacement (1 of 2)

If the front panel ON/OFF LINE button does not effect an audible switching sound, or cycle the line power to the 8350A, the switch actuator lever may need adjustment.

1. Remove AC power cord from rear panel.

WARNING

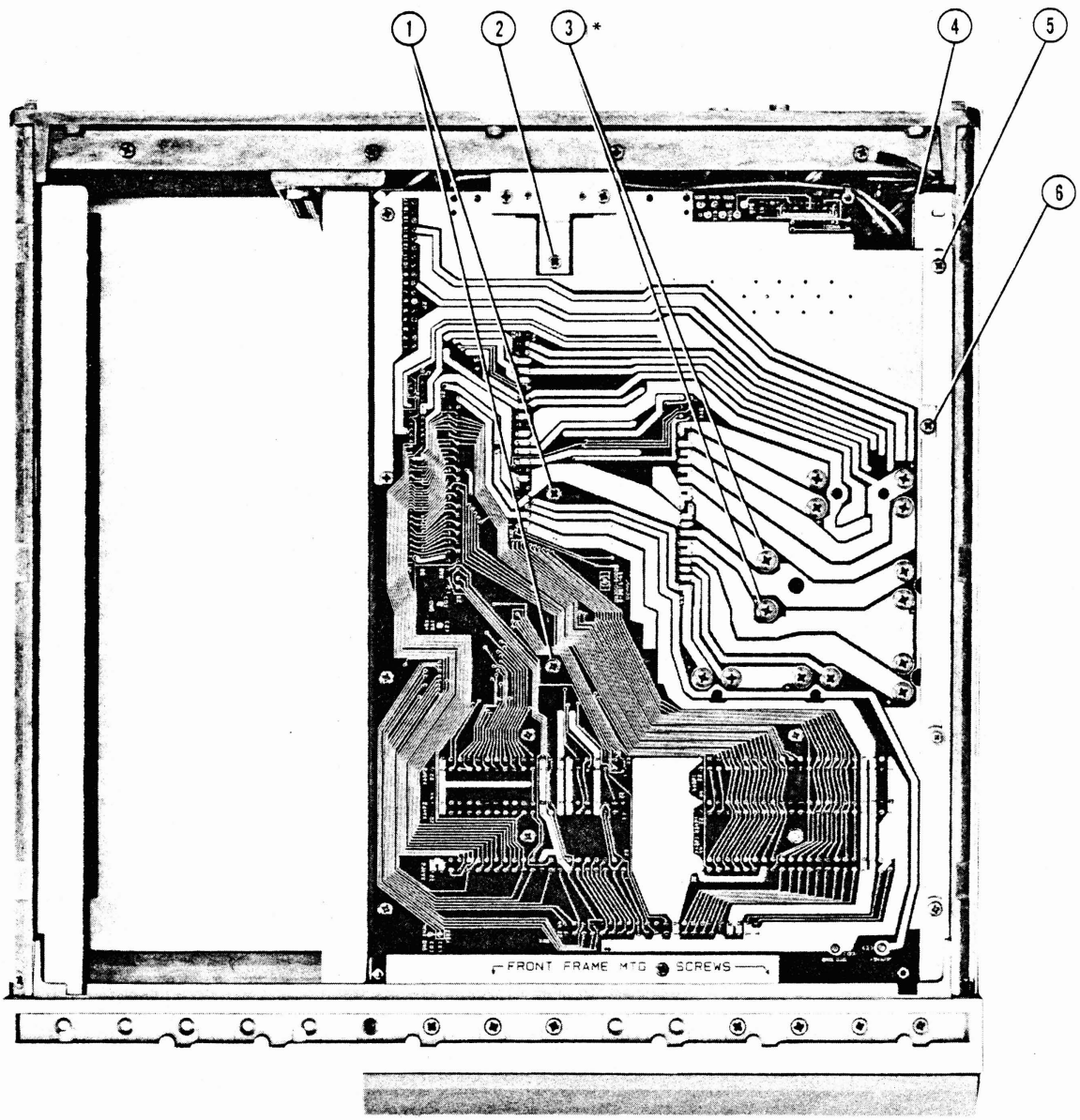
Before attempting this procedure, manually discharge the −40V supply as described in step 2 below.

CAUTION

Do not attempt to discharge the −40V supply capacitor through chassis ground. Use only the method prescribed below, or damage to the instrument will result.

2. Set instrument on its top side. Remove bottom cover. Provide a discharge path for the −40V supply capacitor by applying a 0.5 watt, 100 ohm resistor (via shielded clip leads) between the two motherboard-capacitor screws ③ for a period no less than one second. This method painlessly discharges the −40V supply.
3. Loosen two adjustment screws⑤ ⑥. .
4. Slide toggle switch ④ in either direction along the lever until ON/OFF button activates the switch. Tighten screws. NOTE: The adjustment screw ⑤ nearest the toggle switch must be reasonably loose to allow for lever movement.

Figure 8-7. ON/OFF Switch Lever Actuator Adjustment (1 of 2)



* See WARNING within procedures Figure 8-6/Figure 8-7.

Figure 8-6. Regulator/Heat Sink Replacement (2 of 2)/
Figure 8-7. ON/OFF Switch Lever Actuator Adjustment (2 of 2)

OVERALL BLOCK DIAGRAM, CIRCUIT DESCRIPTION

The 8350A is a microprocessor-based Sweep Oscillator that provides the necessary controls and power supplies for the RF Plug-in. The flexibility of a microprocessor-based instrument allows the 8350A to learn what plug-in is installed, and adapt its outputs accordingly.

The A3 Microprocessor uses two buffered digital busses to control all functions of the 8350A. All communication between the microprocessor and the front panel is on the Front Panel bus. The A3 Microprocessor communicates with the rest of the 8350A and the RF Plug-in via the Instrument Bus. Each bus contains its buffered address, data, and control lines.

The A5 Sweep Generator provides a 0 to +10V sweep ramp which is scaled for frequency tuning the RF Plug-in by the A4 Scaling and Marker assembly. The sweep ramp is also used to synchronize sweep related events (i.e. blanking, and markers).

The A8 HP-IB Interface provides the communication interface with an external controller, and provides the capability of externally programming both the 8350A and RF Plug-in operation.

Power supplies are provided for the RF Plug-in. Due to voltage accuracy requirements for some supplies in the RF Plug-in, these supplies are accurately regulated by sensing the voltage level in the RF Plug-in.

A3 Microprocessor

All data processing in the 8350A is performed by the A3 Microprocessor. This assembly consists of the microprocessor, ROM (Read Only Memory), RAM (Random Access Memory), and the necessary devices for clock generation, address decoding, buffering, and handling of interrupts.

The microprocessor is controlled by a software program stored in ROM. With this software, the microprocessor is capable of performing data transfers (read or write) and internally processes data it has accessed. All data transfers must go through the microprocessor.

The A3 Microprocessor communicates with the rest of the 8350A and the RF Plug-in through two buffered digital busses (Front Panel and Instrument). Each bus uses a separate block of address space.

The Front Panel bus provides the interface to the front panel. This bi-directional interface updates the microprocessor whenever any new data is entered from the front panel. All front panel annunciators and displays are updated through the front panel bus. Since all the interface circuits for the front panel are located on A2, the Front Panel bus only connects between A2 and the A3 Microprocessor.

The Instrument Bus provides the interface between the microprocessor and the rest of the 8350A and the RF Plug-in. This bus is used for bi-directional data transfers between the microprocessor the A8 HP-IB Interface or the RF Plug-in. This bus structure allows the microprocessor to interface with an external controller over the HP-IB bus, and both write and read data to/from the RF Plug-in. Only the outputting of data is necessary for the control of the A5 Sweep Generator and A4 Marker and Scaling assembly.

At initial power on, or whenever INSTR PRESET is pressed, the microprocessor jumps to an Instrument Preset self test routine stored in ROM. Refer to the Overall Block Diagram Troubleshooting information for a description of the test. Upon completion of the Instrument Preset self test, the microprocessor goes into an idle loop, and waits for an interrupt request from one of the assemblies or the RF Plug-in. The microprocessor then reads the Status Buffer to determine the reason for the interrupt, and then performs the appropriate service which is stored in ROM. Upon completion of the service routine, the microprocessor again enters an idle loop, and waits for another interrupt.

A1 Front Panel/A2 Front Panel Interface

The A2 Front Panel Interface contains all the latching, decoding, timing, and driver circuitry necessary for interfacing the front panel keyboard, controls, annunciators, and digital displays to the A3 Microprocessor. The front panel keyboard is connected in a matrix of rows and columns. The A2 Front Panel Interface strobes the columns and senses each row to determine what key, if any, is closed. The A2 Front Panel Interface then notifies the A3 Microprocessor of any keyboard entries. Direction and amount of rotation of the three front panel RPGs (Rotary Pulse Generators) is decoded by the RPG Interface circuit on the A2 assembly. This information is also read by the microprocessor, and is used to update the 8350A. While the data for the digital displays is latched on the A2 Front Panel Interface, the digital displays must be continuously strobed by the microprocessor to maintain a display. Both the annunciators and digital displays are updated by the microprocessor if the state of the instrument changes. The Front Panel Interrupt circuit requests an interrupt when the front panel needs service or when the A5 Sweep Generator is doing a sweep retrace (when a complete update of the instrument is initiated).

A5 Sweep Generator

The A5 Sweep generator produces a 0V to +10V sweep voltage that (after scaling) is used for sweeping the RF plug-in frequency. The sweep voltage is also routed to the front and rear panels (sweep out) for driving the X-axis of monitoring instruments. The sweep voltage is generated by supplying a constant, but programmable, current to the integrator. The integrator converts this current to a sweep voltage. The sweep voltage is limited by two comparators in the sweep trigger circuit. The Sweep Ramp Generator actually produces a ramp that sweeps from −0.95V to +10.8V in amplitude. This voltage is clamped by the Clamping circuit at 0V and +10V. The unclamped ramp is buffered and used by the Sweep Ramp Status and Sweep Trigger circuits. The 0V to +10V clamped ramp is buffered and forms four outputs.

A number of real-time digital lines interface the 8350A and the RF Plug-in. These lines provide the proper sequencing of events during bandswitch points (i.e., stop sweep, blanking). The Output Control circuit provides the necessary blanking and penlift pulses. The Counter Interface circuit provides the necessary timing and sequencing of events for interfacing the 8350A with an external counter such as the HP 5343A. This interface allows the counting of the Start, Stop, or Marker frequencies while the 8350A is in a swept operation.

A4 Scaling and Marker

The A4 Scaling and Marker assembly provides a scaled tuning voltage to the RF Plug-in, and generates marker pulses for the five 8350A frequency markers (M1 through M5).

The VTUNE output is the sum of three scaling DACs (Digital-to-Analog Converters). These DACs are programmed by the microprocessor and updated each sweep retrace. The ΔF Generation DAC scales the sweep voltage (VSW1) to provide an output which is symmetrical around 0V, and is proportional to the frequency range swept. This swept output is summed with the CW,CF and Vernier DAC outputs, which set the center frequency, to provide a scaled tuning voltage for the RF Plug-in installed.

The Marker circuits generate markers in respect to the sweep voltage (VRAMP). Marker data is loaded by the microprocessor during every sweep retrace. This data is used to control the Marker DAC. The Marker Comparator monitors both the Marker DAC output and VRAMP. When both inputs are equal, a marker output pulse is generated.

A8 HP-IB Interface

The A8 HP-IB Interface provides the interface between the external HP-IB bus and the internal Instrument bus. The interface consists mainly of a Large Scale Intergrated (LSI) circuit and associated buffers. The LSI circuit handles the specified handshake with the HP-IB controller and stores information in internal registers until it is processed by either the 8350A microprocessor or the external HP-IB controller. Status indicators are provided to indicate the present status of an HP-IB operation (Listen, Talk, Service Request, or Remote). An address switch is provided to select the HP-IB address of the 8350A.

Self test circuitry is also on the A8 assembly, and is used to verify operation of the Instrument bus during the Instrument Bus self test. This test is performed during the Instrument Preset self test.

A6 Rectifier and A7 Regulator

The A6 Rectifier and A7 Regulator not only supply power for the 8350A, but also provide power for the RF Plug-in. All supplies are overvoltage protected and current limited.

The +20V, −10V, and −40V supplies are used only in the RF Plug-in. They provide power for the RF microcircuits, and are also used for reference voltages to control frequency and power. Therefore, these supplies must be well regulated (independent of voltage drops through connectors and traces). For these supplies, their respective voltages are sensed in the RF Plug-in, and regulated at that point. The remainder of the supplies are regulated by conventional three-terminal regulators.

The Power On circuit resets the microprocessor at initial power on. The Supply Failure circuit flags the microprocessor if a power supply output goes low, and the microprocessor responds by displaying error code E004. The Air Flow circuit detects if the air flow from the fan is too low and flags the microprocessor to display error code E016.

Self Tests

Self tests are available to aid in troubleshooting the 8350A. These tests fall into two catagories, Instrument Preset and Operated Initiated self tests.

- Instrument Preset − A series of self tests is performed when initial power is turned on or when the front panel INSTR PRESET key is pressed. If all tests are satisfactory, the front panel FREQUENCY displays should indicate the

full frequency range of the RF plug-in installed. If the 8350A fails one of the self tests, an error code is displayed (see explanation of error codes). Figure 8-8 is a flow diagram showing the tests performed during Instrument Preset. Note that the A3 Microprocessor circuits are checked initially, then the digital busses are checked. Once the digital circuits are verified, the Instrument Preset test checks the power supplies and functional operation of the Tuning Voltage, Marker, and Sweep Ramp circuits. Finally the digital interface with the RF Plug-in is checked.

- Operator Initiated – Operator initiated self tests are provided to aid in troubleshooting once a problem is isolated to a particular area. Most tests performed during Instrument Preset can also be initiated from the front panel. No error codes are generated by Operator Initiated self tests. Most of these tests are repetitive, and provide known conditions for exercising and checking specific circuits. Table 8-3 gives a brief explanation of each Operator Initiated self test.

Error Codes

The A3 Microprocessor generates an error code if one of the self tests performed during Instrument Preset fails. An error code may be displayed at each of the following locations (See Figure 8-9).

- A3 Microprocessor Error Code LEDs. Primary error code indicator and is used for all error codes. If different error code indication occurs between different displays, the error code indicated by the A3 Microprocessor is correct.

- SWEEP TRIGGER Annunciators. Used only for error codes E015 through E006. Provides front panel indication if part of front panel is operational. Error code display is identical to display on the A3 Microprocessor. If error code is displayed, verify the same error code is displayed on the A3 Microprocessor.

- FREQUENCY Display. Used for error codes E016 and E005 through E001. Requires that the front panel is operational. If error code is displayed, verify the same error code is displayed on the A3 Microprocessor.

Troublehooting with Self Tests

Initial troubleshooting should begin by initiating an Instrument Preset self test and checking for error codes. This self test is automatically initiated at power on, or can be selected by pressing the INSTR PRESET key. Depending on the results of the Instrument Preset self test, proceed to the troubleshooting hints for either passing or failing this test.

Front Panel Display Failure

It is possible to have a front panel failure without generating an error code. Initiate the Instrument Preset self test and check for any activity from the A3 Microprocessor LEDs. If the LEDs do not cycle on then off, the Instrument Preset was not initiated. Check the +5V power supply, then refer to the A3 Microprocessor service sheet. If the LEDs cycle on then off, this indicates that the 8350A has passed the Instrument Preset self test. The front panel display problem could be caused by the A1 Front Panel, A2 Front Panel Interface, or the RF Plug-in. Front Panel operation is verified if the front panel displays are operational without the RF Plug-in

installed. Check front panel operation as follows.

1. Remove RF plug-in.
2. Initiate Instrument Preset (Error code E001 should be displayed).
3. Press START key. The 8350A front panel displays should indicate a start/stop frequency sweep of 0 MHz to 10,000 GHz.

Fail Instrument Preset

Refer to Table 8-5 for a list of error codes and troubleshooting hints.

Table 8-5. 8350A Error Codes

Error Code	Function Tested	Operator Initiated Test	Troubleshooting Hints
E016	Airflow	None	Check fan filter is clean and clear of obstructions.
E015	Microprocessor	None	Refer to A3 Microprocessor and A3A1 PROM board service sheets. Troubleshoot using the Free Run test.
E011-014	RAM	SHIFT 07	Refer to A3 Microrpocessor service sheet. Check RAM power supply and address decoding.
E007-010	ROM	SHIFT 06	Refer to A3A1 PROM board service sheet. Check A3A1 interconnections with A3 Microprocessor. Check address decoding and power supply. Troubleshoot using the Free Run test.
E006	Front Panel Bus	SHIFT 08	Trouble may be either the A2 Front Panel Interface or the A3 Microprocessor. Refer to the A2 Front Panel Interface service sheet for troubleshooting information.
E005	Instrument Bus	SHIFT 09	Shorted or open Instrument bus lines. Isolate to assembly by removing RF Plug-in, A4 Marker and Scaling, A5 Sweep Generator, and disconnecting RF Plug-in interface cable W4 from the 8350A Motherboard. If E005 still occurs, refer to the A8 HP-IB service sheet for further troubleshooting.
E004	Power Supplies	None	Check power supply LEDs on the A7 Regulator to determine faulty power supply. Cycle power on and off with the RF plug-in removed to determine if the problem is caused by the 8350A or the RF Plug-in. Check appropriate fuses.
E003	TV/Marker	SHIFT 10	Trouble is probably with thy A4 Scaling and Marker assembly. Refer to the A4 service sheet for further troubleshooting.
E002	Sweep/Marker	SHIFT 11	Marker circuit was verified in previous test. Check VRAMP output from A5 Sweep Generator. Ramp should go from 0V to about +4.2V in 3 steps. If VRAMP is verified, refer to A4 Scaling and Marker service sheet. If VRAMP is not verified, refer to A5 Sweep Generator service sheet.
E001	Rf Plug-in Bus	SHIFT 12	Open Instrument Bus between 8350A and RF Plug-in Digital Interface assembly. Ensure RF Plug-in is installed and making good contact. Check RF Plug-in interface cables. Check RF Plug-in cables are making good contact. Refer to RF Plug-in Digital Interface service sheet for further troubleshooting. If 11869A Adapter is installed, refer to Adapter A1 Logic service sheet for further troubleshooting.

Pass Instrument Preset

If the 8350A passes the Instrument Preset self test, the instrument is functionally operating, but the analog voltages are not verified for accuracy. Table 8-6 references each assembly and describes what functions are verified by the Instrument Preset self test. Also listed are some major functions that are not verified and may require further testing.

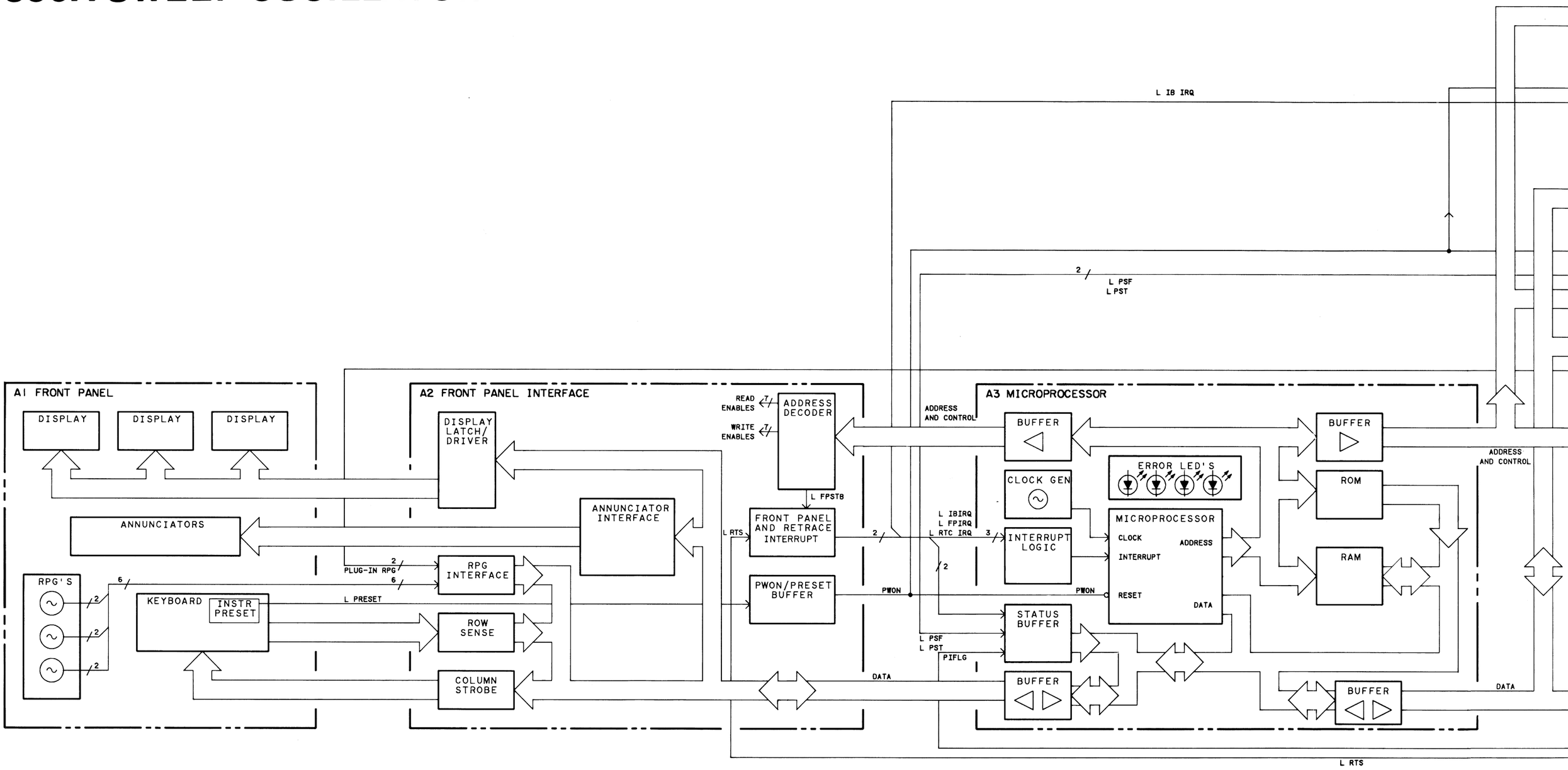
Table 8-6. Assembly Functions Verified by Instrument Preset Self Test (1 of 2)

Assembly	Instrument Preset Self Test	Operator Initiated Self Tests		Troubleshooting Hints
A1	None	Key Codes	SHIFT 04	Check cable connections to A2 Front Panel Interface. Check +5V and return wire connections to the A9 Motherboard. Refer to A1 Service Sheet for explanation of the Operator Initiated Self Tests
A2	Front Panel Bus	Key Codes Display Exercise Front Panel Bus RPG Circuit Front Panel Lamps	SHIFT 04 SHIFT 05 SHIFT 08 SHIFT 17 SHIFT 18	Front Panel Bus Test verifies that data can be written to and read from A2, and that none of the data lines are shorted. Interface circuits to A1 can be checked by using Operator Initiated Self Tests. Refer to A2 Service Sheet for further troubleshooting.
A3	Microprocessor	ROM RAM Front Panel Bus Instrument Bus Free Run (See A3 Service Sheet)	SHIFT 06 SHIFT 07 SHIFT 08 SHIFT 09	Instrument Preset Self Tests verify basic operation of all functions. Operation of the Interrupt Logic and Status Buffer circuit is not completely verified. A component failure on A3 usually disables operation of the 8350A. Refer to the A3 Service Sheet for further troubleshooting.
A4	Tuning Voltage vs. Marker Sweep vs. Marker	Tuning Voltage vs. Marker Sweep vs. Marker CW DAC ΔF DAC Sweep vs. ΔF DAC Marker DAC Vernier DAC	SHIFT 10 SHIFT 11 SHIFT 13 SHIFT 14 SHIFT 15 SHIFT 16 SHIFT 19	The CW, CF DAC and ΔF DAC can be controlled by the A3 Microprocessor, but scaling accuracy is not verified. Marker circuits are functional, but actual marker outputs are disabled during Instrument Preset. Scaling Problem – Check VTUNE Cable to RF Plug-in is connected at A4J1. Check +10V REF accuracy. Check VSW1 input from Sweep Generator. Check Scaling DACs with Operator Initiated Self Tests. Refer to A4 Service Sheet for further troubleshooting. Marker Problem – Refer to A4 Service Sheet for further troubleshooting.

Table 8-6. Assembly Functions Verified by Instrument Preset Self Test (2 of 2)

Assembly	Instrument Preset Self Test	Operator Initiated Self Tests		Troubleshooting Hints
A5	Sweep vs. Marker	Sweep vs. Marker Sweep vs. ΔF DAC	SHIFT 11 SHIFT 15	Sweep Generator can be programmed in manual sweep operation. Integrator and Sweep Trigger circuits are not checked. VRAMP output to A4 is operational but not necessarily accurate. Refer to A5 Service Sheet for further troubleshooting.
A6	Power Supply	None		Power On circuit is operational. Voltage outputs are supplied to A7. Penlift and Line Trigger circuits are not checked. Refer to A6 Service Sheet for further troubleshooting.
A7	Power Supply	None		Power Supplies are operational, but not necessarily accurate. Air Flow Detection circuit is not checked. Refer to A7 Service Sheet for further troubleshooting.
A8	INSTRUMENT BUS	INSTRUMENT BUS	SHIFT 09	The Self Tests verify that data can be written to and read from Self Test circuits. Address lines are operational. HP-IB Interface circuits are not checked. Refer to A8 Service Sheet for further troubleshooting.

8350A SWEEP OSCILLATOR



A8 HP-IB INTERFAC

ADDRESS DECODER

HP-IB INTERFACE
ADDR.
DATA IN
DATA OUT
RESET
INTERRUPT REQUEST

HP-IB BUS DRIVER

J4

HP INTERFACE BUS

DATA BUFFER

ADDRESS SWITCH

STATUS INDICATOR
LSN TALK SRQ RMT

A6 RECTIFIER
A7 REGULATOR

POWER ON

SUPPLY FAILURE DETECTION

AIR FLOW

PWON

L PSF

L PST

RF PLUG-IN

J2
±15V → 28, 29 → ±15V
+5VB → 18, 50, 51 → +5VB
J3
+20V → 7 → +20V
-10V → 13 → -10V
-40V → 11 → -40V
+10V → 8 → +10V

ADDRESS BUS

DATA BUS

J3
7,8 11-13 40-44 → 13
J2
32 → LSSRQ
5-8 27-30 → 8
60 61 → 2 → PIRPG1A PIRPG1B → RPG
64 → VSW

SWEEP GENERATOR

ADDRESS DECODER

SOFTWARE CONTROL

SWEEP RAMP GEN

CLAMP +10

SWEEP VOLTAGES BUFFERS
V SW
V RAMP
V SW1
V SW2

SWEEP TRIGGER
+10.8
-0.95
PL1

SWEEP STATUS
START/STOP SWEEP
L PL1

COUNTER INTERFACE
LAMK

OUTPUT CONTROL

SQUARE WAVE OSCILLATOR
OSC EN

DATA BUFFER

A4 SCALING AND MARKER

ADDRESS DECODER

MARKER DATA AND RAM

DAC

MARKER COMPARATOR
L AMK

V RAMP

MKR CNTR ADV

VERNIER

+10V REF

+10V REF

CW, CF GEN

VSW1

△F GEN

DATA BUFFER

SUMMING AMP

VTUNE

J2
20 → PI FLG
J3
A1 → V TUNE
J2
26 → SQ MOD

J12
AM IN → J3 A4 → AM

J11
FM IN → J3 A3 → FM

J1 SWEEP OUTPUT
SWEEP INPUT
J8 SWEEP OUT/IN
J6 NEG Z BLANK
J5 POS Z BLANK
J7 PEN LIFT
J4 CNTR TRIG
J10 STOP SWEEP

Figure 8-10. 8350A Overall Block Diagram

A1 FRONT PANEL and A2 FRONT PANEL INTERFACE, CIRCUIT DESCRIPTION

NOTE

Because of the electrical and physical structure of the A1/A2 interface, the two boards are discussed simultaneously. Therefore, block diagrams, circuit description, and trouble-shooting procedures have been combined and completely reprinted in both the Al and A2 Service Sheets.

The A2 Front Panel Interface Assembly contains all the necessary circuitry to allow bidirectional communication between the A3 Microprocessor Assembly and the A1 Front Panel functions. Table 8-7 indexes the rate of data transfer between the Microprocessor and the various Front Panel registers. The A1/A2 Block Diagram is shown in Figure 8-17. The following circuit description is broken down by front panel function: Address Decoder, Keyboard, RPGs, Digital Display, Annunciators, and Interrupt circuitry.

Table 8-7. A2 Activity Rate

ACTIVITY	RATE (approximate)
Refresh Display	1.6 kHz (Each display has an individual refresh rate of 100 Hz. (1.6 kHz÷16 digits))
Scan Keyboard	200 Hz (Debounce at a 30 Hz rate if active.)
Read RPGs	60 Hz
Blink Annunciators: GHz, MHz (for out-of-range indication and blink active marker annunciator).	150 Hz

NOTE

All reference designations refer to A2 components unless otherwise noted.

Address Decoder A2: (B)

Three-to-eight decoders, U23 and U31 interpret the Front Panel Bus address lines, LFPA0 through LFPA2. Decoder outputs enable the particular devices to be addressed by the Microprocessor during data transfer. Decoding activity is determined by three enable lines: FPE (Front Panel Enable) and LFPSTB (Low=Front Panel Strobe) allow access to the front panel; LFPRD (Low=Front Panel Read) determines the direction of data flow (read or write) at the addressed device. Note that all A2 latches are unidirectional. U23 decodes all READ enables while U31 decodes all WRITE enables, allowing the overlap of 1800-series addresses. Only fourteen of the sixteen possible enable lines from U23 and U31 are used: LRE1–4, LRE6–8, LWE1–6, and LWE8. Table 8-8 provides decoding information.

Table 8-8. Address Decoding

Mnemonic	Address	Location	Read/Write	Test Point	Description
LRE1	1800H	U15	Read	23	Read Keyboard Row Sense
LRE2	1801H	U10	Read	9	Read RPG Sign/Digit and Digital Counter
LRE3	1802H	U11	Read	11	Read RPG1/RPG2 Counts
LRE4	1803H	U12	Read	16	Read RPG3/PIRPG Counts
LRE5					Not Used
LRE6	1805H	U8B	Read	4	Clear Retrace Interrupt
LRE7	1806H	U5A/B U6A/B	Read	8	Reset RPG Counters
LRE8	1807H	U7	Read	26	Read Column Data (Self-Test)
LWE1	1800H	U16	Write	25	Latch Keyboard Column Data
LWE2	1801H	U13	Write	22	Latch Annunciator Data
LWE3	1802H	U25	Write	21	Latch Annunciator Data
LWE4	1803H	U27	Write	17	Latch Annunciator Data
LWE5	1804H	U26	Write	20	Latch Annunciator Data
LWE6	1805H	U24	Write	18	Latch Annunciator Data
LWE7					Not Used
LWE8	1807H	U8A	Write	10	Enables Display/Clears Front Panel Interrupt

Keyboard A1: (F) A2: (A) (H)

The Microprocessor periodically uses the Keyboard Interface circuits for scanning the Keyboard state. Coded data is loaded into the Column Strobing Latch U16 by the Microprocessor. The resulting row data from the keyboard matrix (F) is read back when U15 is enabled. The Microprocessor scans the Keyboard Interface at a rate of 200 Hz to determine whether a keyboard pushbutton has been pressed.

Two additional signals are scanned through the keyboard interface:

LPRESET. When the line power is cycled or INSTR PRESET is pressed, the microprocessor resets and initiates Self-Test. In either case PWON (A) is driven low to reset latches and flip-flops. However, the Microprocessor must determine which action caused the reset in order to execute the appropriate RAM initialization routine. If the instrument ON/OFF switch is toggled, the Microprocessor will clear all RAM registers (not true for 8350A Opt. 001). If INSTR PRESET has been pressed, LPRESET signal will be detected at U15, bit 7. In this case, the SAVE/RECALL registers are not cleared.

LSTPADV. Low Step Up Advance, from the rear J13, increments the Step Up function for the act registers).

RPGs (Rotary Pulse Generation) A2: (G)

RPG Interface circuitry senses the direction of output of four RPGs: three on the 8350A Front Pa RF plug-in. There are two pulse train outputs from relationship of the pulse train pair is sensed by a f translates the RPG direction (+, −) of rotation processor reads the flip-flop outputs and increme display accordingly.

One pulse train output from each RPG clocks a fo When LRE3 and LRE4 go low, the counter outpu and read by the Microprocessor. Data is then writ (U22) and eventually used to update the display se after each READ enable.

Front Panel Interrupt Routine A2: (C) (E)

The following signals, used to interrupt the Micro

LDE: Low=Display Enable, TP6.
LRTS: Low=Retrace Strobe, P1-42
LRE6: Low=Read Enable 6, TP4.
LWE8: Low=Write Enable 8, TP10.
LFPIRQ: Low=Front Panel Interrupt Requ
DSPCLK: Display Clock, TP3.
LDCINCR: Low=Digit Counter Increment,
LRTCIRQ: Low=Retrace Interrupt Request

A series of three digital counters (U20A, U20B, an functions. LFPSTB is being used as an 823 kHz processor I/O Strobe data transfer timing signal. counters during each machine cycle of the micro

DSPCLK pulses at approximately 1.6 kHz (823 resets LDCINCR low, to increment the digit co request (LFPIRQ) to the Microprocessor. At this displays while the Microprocessor services the inte holds the FP Interrupt Timer. LWE8 sets LDE simultaneously latches the new data into U22 (F clear the interrupt request.

LRTS, from the A5 Sweep Generator assembly, o retrace and sets LFPIRQ and LRTCIRQ low. The interrupt is a function of the retrace (LRTCIRQ) a the instrument. LRE6 clears the retrace interrupt

Digital Display Control A1: (A) A2: (F)

Each time LFPIRQ is set low, LDCINCR increme Microprocessor executes the Front Panel Interru routine, the Microprocessor refreshes one displa A1U2 decode the outputs of Digit Counter U19B updated. The refresh rate per digit is approxi maintain a flicker-free display.

ddress Decoding

e	Test Point	Description
	23	Read Keyboard Row Sense
	9	Read RPG Sign/Digit and Digital Counter
	11	Read RPG1/RPG2 Counts
	16	Read RPG3/PIRPG Counts
		Not Used
	4	Clear Retrace Interrupt
	8	Reset RPG Counters
	26	Read Column Data (Self-Test)
	25	Latch Keyboard Column Data
	22	Latch Annunciator Data
	21	Latch Annunciator Data
	17	Latch Annunciator Data
	20	Latch Annunciator Data
	18	Latch Annunciator Data
		Not Used
	10	Enables Display/Clears Front Panel Interrupt

Keyboard Interface circuits for scanning into the Column Strobing Latch U16 by ata from the keyboard matrix (F) is read ocessor scans the Keyboard Interface at a eyboard pushbutton has been pressed.

ugh the keyboard interface:

led or INSTR PRESET is pressed, the est. In either case PWON (A) is driven low ne Microprocessor must determine which ute the appropriate RAM initialization n is toggled, the Microprocessor will clear pt. 001). If INSTR PRESET has been ected at U15, bit 7. In this case, the d.

LSTPADV. Low Step Up Advance, from the rear panel Programming Connector J13, increments the Step Up function for the active mode (i.e., SAVE/RECALL registers).

RPGs (Rotary Pulse Generation) A2: (G)

RPG Interface circuitry senses the direction of rotation and counts the pulsed output of four RPGs: three on the 8350A Front Panel and one on the 83500 series RF plug-in. There are two pulse train outputs from each RPG. The Lead/Lag phase relationship of the pulse train pair is sensed by a flip-flop (U3A/B, U4A/B) which translates the RPG direction (+, −) of rotation. See Figure 8-21. The Microprocessor reads the flip-flop outputs and increments or decrements the numeric display accordingly.

One pulse train output from each RPG clocks a four-bit counter (U5A/B, U6A/B). When LRE3 and LRE4 go low, the counter outputs are enabled onto the data bus and read by the Microprocessor. Data is then written to the Display Control Latch (U22) and eventually used to update the display segments. RE7 resets the counters after each READ enable.

Front Panel Interrupt Routine A2: (C) (E)

The following signals, used to interrupt the Microprocessor, are discussed below:

LDE: Low=Display Enable, TP6.
LRTS: Low=Retrace Strobe, P1-42
LRE6: Low=Read Enable 6, TP4.
LWE8: Low=Write Enable 8, TP10.
LFPIRQ: Low=Front Panel Interrupt Request, P1-23.
DSPCLK: Display Clock, TP3.
LDCINCR: Low=Digit Counter Increment, TP7.
LRTCIRQ: Low=Retrace Interrupt Request, TP5.

A series of three digital counters (U20A, U20B, and U19A) perform divide-by-two functions. LFPSTB is being used as an 823 kHz time base, tracking the Microprocessor I/O Strobe data transfer timing signal. Therefore, LFPSTB clocks the counters during each machine cycle of the microprocessor.

DSPCLK pulses at approximately 1.6 kHz (823 kHz ÷ 512). Each rising pulse resets LDCINCR low, to increment the digit counter (F), and sets the interrupt request (LFPIRQ) to the Microprocessor. At this time LDE is high to disable the displays while the Microprocessor services the interrupt. High LDE also resets and holds the FP Interrupt Timer. LWE8 sets LDE low to enable the displays, and simultaneously latches the new data into U22 (F). LWE8 also resets LFPIRQ to clear the interrupt request.

LRTS, from the A5 Sweep Generator assembly, occurs coincident with the sweep retrace and sets LFPIRQ and LRTCIRQ low. The Microprocessor senses that the interrupt is a function of the retrace (LRTCIRQ) and initiates a complete update of the instrument. LRE6 clears the retrace interrupt request.

Digital Display Control A1: (A) A2: (F)

Each time LFPIRQ is set low, LDCINCR increments Digit Counter U19B and the Microprocessor executes the Front Panel Interrupt Service Routine. During the routine, the Microprocessor refreshes one display digit. Digit Drivers, A1U1 and A1U2 decode the outputs of Digit Counter U19B to determine which digit will be updated. The refresh rate per digit is approximately 100 Hz, fast enough to maintain a flicker-free display.

With each low-to-high transition of LWE8, U22 latches data which determines the segment states for the active digit. Resistor and diode networks (U30, U29, and U21) bias Segment Drivers A1Q1 through A1Q8. A low data bit to U22 activates the corresponding segment driver, producing a 30 mA current source. A high data bit input (greater than or equal to 2V) turns off the segment driver. Figure 8-11 shows the simplified schematic.

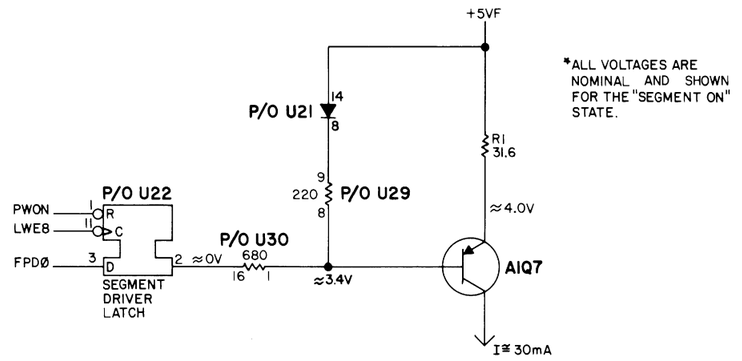


Figure 8-11. Typical Segment Driver Schematic

Annunciators A1: (E) A2: (D)

Five latches (U13, U24−U27) with current limiting resistors, latch and buffer data to drive the Front Panel annunciators (with the exception of SWP). Q1 through Q6 provide three constant current sources to ensure uniform intensity in the unit Annunciators (i.e., GHz, MHz, sec). LPRESETE signal is stored in the Annunciator function block.

A1/A2 TROUBLESHOOTING PROCEDURE

NOTE

Because of the electrical and physical structure of the A1/A2 interface, the two boards are discussed simultaneously. Therefore, block diagrams, circuit descriptions, and troubleshooting procedures have been combined and completely reprinted in both Al and A2 Service Sheets.

Since the 8350A Instrument Self-Test, does not detect all possible Front Panel failures, A1/A2 troubleshooting information is divided into two major sections: A. Front Panel Self-Test FAIL; B. Front Panel Self-Test PASS. Each section outlines suspect areas and component level troubleshooting.

PRELIMINARY CHECKS

Perform a brief visual inspection of the A2 board for physical or heat damage. Check the following: +5V supply at TP 15; that LPRESET (TP 1) and PWON (TP 2) are both high during normal instrument operation; that all S1 switches are closed and all S2 switches open for NORMAL operation; that A1/A2 ribbon cable connections are firmly seated over the correct pins.

NOTE

All reference designations refer to A2 components unless otherwise noted.

NOTE

Timing diagrams referenced for A1/A2 Troubleshooting are located on the A2 Service Sheet.

A. FRONT PANEL SELF-TEST FAIL

The A2 Front Panel Interface board is exercised and checked as part of the Self-Test routine performed at each "turn-on" or Instrument Preset. (Refer to Table 8-8, Self-Test Flowchart, in the Overall Troubleshooting section for details.)

If the microprocessor detects a Front Panel failure, the instrument Self-Test sequence will be aborted and the Front Panel Self-Test will be cycled continuously. In this mode, all Front Panel annunciators will be lit, and a single numeral '8' with its decimal point will flicker sequentially from right to left across the digit display. The Error Code E006 will not appear in the Front Panel Digital Display, however, the Error Code LEDs on the A3 Microprocessor Board and the Sweep Trigger annunciators will display the code in its binary form: 0110 ('1' turns the LED on).

The Front Panel error code indicates a possible failure in the Address Decoder, Data Bus, Column Latch, or the Self-Test Buffer. To troubleshoot these areas place A2 on an extender board. Push **INSTR PRESET** to allow the failure to begin the repetitive test. Troubleshoot as described below.

Address Decoder

During the Front Panel Self-Test, each of the Read Enables (U23) is addressed to enable in sequence, followed by each Write Enable (U31). The Write Enable sequence starts with LWE2 enabled first and LWE1 enabled last. (Note: additional pulses appear on the LWE1, LWE2, LWE5, and LWE8 lines slightly later and throughout the cycle).

Set the oscilloscope at a sweep speed of 50 microseconds/division and externally trigger from LRE1 (TP23). Verify proper pulse location and duration of each Address Decoder line. Refer to Figure 8-19. If any lines cannot be verified, check the LFPRD, LFPSTB, FPE, and address lines for activity. If any of these signals are missing, trace the lines back to the A3 Microprocessor board and the Front Panel buffers, A3U22 and A3U32. If the Microprocessor busses and control lines appear dead, perform the Free Run Test described in the A3 Troubleshooting Section.

Data Bus, Column Latch, and Self-Test Buffer

To verify proper functioning of Keyboard Column Latch U16, a binary '1' is stepped through each column (C0—C7) while a '0' is written to the other seven. After a delay, LRE8 is pulsed low. The latched data is read back to the microprocessor through the Self-Test buffer (U7) and verified. The next LWE1 pulse clears the bit and shifts the '1' to the next column.

Check the inputs and outputs of U7 against Figure 8-19. This exercise thoroughly checks the Data Bus and partially verifies the Address Bus, Address Decoder Block, and FPE and LFPRD lines.

B. FRONT PANEL SELF-TEST PASS

If an Error Code E005 or lower, or no Error Code, occurs during power-up or INSTR PRESET, the Front Panel Self-Test routine has been successfully performed. This verifies that the Front Panel Data Bus, Address Bus, Keyboard Column buffer, Self Test buffer, and part of the Address Decoder block are functioning correctly.

If symptoms apparent at the Front Panel indicate a failure in the Keyboard, RPGs, Annunciators, or Digital Display, refer to the apropriate section below for further troubleshooting. If the entire Front Panel does not respond, but the A3 Microprocessor board has been verified, refer to the Interrupt Control section below and Address Decoder troubleshooting outlined earlier.

The following troubleshooting procedures utilize the repetitive mode of the Front Panel Self-Test. The routine can be initiated as follows:

1. If the 8350A responds to front panel commands, simply enter SHIFT 0 8 .

2. If the 8350A does not respond to Front Panel commands, connect a jumper between LTEST (A3 TP20) and GND (A3 TP14). Press INSTR PRESET or cycle the line power.

Keyboard Failure

Since the instrument passed the Front Panel Self-Test, the Keyboard Column latches and Data Bus are functioning properly. If the Keyboard is not working, suspect the LRE1 line, the Keyboard Row sense driver (U15), or the Keyboard matrix:

1. Initiate the Front Panel Self-Test and check the LRE1 line against Figure 8-19. If it is faulty, go back and troubleshoot the Address Decoder block.

2. Initiate the Front Panel Self-Test. While pressing a key, check that the appropriate Row line (input to U15) follows the corresponding Column line. See Figure 8-19. If these are normal, suspect U15. If this test fails, the problem lies in the keyboard matrix or interconnecting lines. Initiate the Key Code Test. (If the instrument will not execute the Key Code Test, troubleshoot the keyboard matrix.

3. Enter SHIFT 0 4 to initiate Key Code Test. Press any key and the appropriate code, indexed in Table 8-9, should appear in the digital display. If a depressed key is not being detected, the code will not light up. If two keys are shorted together, both will produce the same code. The Key Code Test should detect most keyboard failures. Further matrix troubleshooting should be performed with a continuity checker.

Table 8-9. Key Codes (1 of 2)

Pushbutton	Keycode	Column (U16)	Row (U15)
START	20	7	0
CW	24	4	2
CF	22	2	2
Delta F	23	1	2
STOP	21	0	2
VERNIER/OFFSET	25	3	2
LCL	1b	7	2
INSTR PRESET	*		
MKR→ CF	26	6	2
MKR SWEEP	27	5	2

Table 8-9. Key Codes (2 of 2)

Pushbutton	Keycode	Column (U16)	Row (U15)
M1	10	2	5
M2	11	0	5
M3	12	1	5
M4	13	2	4
M5	14	0	4
OFF	15	1	4
SAVEn	18	0	6
RECALLn	19	1	6
ALTn	1A	2	6
STEP SIZE	1C	3	6
Up Arrow	1d	3	5
Down Arrow	1E	3	4
0	0	4	3
1	1	4	4
2	2	5	4
3	3	6	4
4	4	4	5
5	5	5	5
6	6	6	5
7	7	4	6
8	8	5	6
9	9	6	6
.	A	5	3
-	b	6	3
GHz/s	C	7	6
MHz/ms	d	7	5
dB/dBm	E	7	4
BKSP	F	7	3
SHIFT	1F	3	3
INT (Sweep Trig)	28	3	1
LINE (Sweep Trig)	29	2	1
EXT (Sweep Trig)	2A	1	1
SINGLE (Sweep Trig)	2B	0	1
EXT (Sweep)	2C	2	3
MAN (Sweep)	2d	0	3
TIME (Sweep)	2E	1	3
AMPL MKR	30	4	1
DSPL BLANK	31	5	1
RF BLANK	32	6	1
⊔⊓ MOD	33	7	1

*Note: INSTR PRESET is not scanned through the Keyboard Matrix. It is enabled through Addr 1805, Data Bit 7 (Low to Enable).

Rotary Pulse Generator (RPG) Failure

If an RPG effects no Front Panel changes, check its +5VR supply and inspect wires for damage. Place A2 on an extender board. The RPG outputs are accessible at the inputs of U9. Carefully probe the two pin connections corresponding to the suspected RPG. Slowly rotate the RPG in each direction while observing the waveforms on a scope, and compare them to those in Figure 8-21. If no activity is seen, check continuity of RPG leads and A1/A2 interconnect ribbon cables. Before replacing the RPG, perform the RPG self-test described below.

During the RPG Self-Test, the actual RPG outputs are switched out of the circuit (S1 open). Data written to the Keyboard Column Latch (U16) by the Microprocessor is switched in (S2 closed) to pulse the RPG sign latches (U3/4) and counters (U5/6) repetitively.

CAUTION

The following steps must be performed in the order given or the instrument will lock up.

The RPG Self-Test is initiated by performing the following steps:

1. Turn off the line power.
2. Place A2 on an extender board.
3. Open all S1 switches.
4. Turn the line power on.
5. Enter SHIFT 1 7 (The digit display will go blank).
6. Close all S2 switches to place the Front Panel Interface in the TEST mode.

To examine the waveforms in the RPG Interface, externally trigger the oscilloscope from the non-inverting output of the RPG sign latch (U4, pin 5). Set the oscilloscope at a sweep speed of 100 to 200 microseconds/division. (TP11 or TP8 will sometimes provide adequate triggering.)

CAUTION

Use IC TEST CLIP, HP Part Number 1400-0734 when probing IC pins.

Read/Write Enables. The four Read Enable lines associated with the RPG circuitry (LRE2, LRE3, LRE4, and LRE7) are each pulsed low. Since the Keyboard Column latches are used to pulse the RPG circuitry, the LWE1 line is pulsed rapidly, and should be checked for activity. See Figure 8-22 for typical waveforms.

If the Enable lines cannot be verified, troubleshoot the Address Decoder block as described earlier.

RPG Counters. In the TEST mode, U5 and U6 count the number of pulses produced by Keyboard Column latch U16. Each 4-bit binary counter begins at 0 (Binary: 0000). They are clocked sixteen times, counting to 15 (Binary: 1111) and then overflow back to 0. Waveforms for each of the four counters are identical. See Figure 8-22. If the Enable lines have been verified but the counters fail, replace the defective counter.

Table 8-16. RPG Counter Test Points

Function	Left RPG	Middle RPG	Right RPG	Plug-In RPG
Clock	U5, p1	U5, p13	U6, p1	U6, p13
Counter (1) (LSB)	U5, p3	U5, p11	U6, p3	U6, p11
Counter (2)	U5, p4	U5, p10	U6, p4	U6, p10
Counter (4)	U5, p5	U5, p9	U6, p5	U6, p9
Counter (8) (MSB)	U5, p6	U5, p8	U6, p6	U6, p8

RPG Sign Latches. U3 and U4 are D Flip-Flops whose outputs depend on whether the RPG is being rotated clockwise or counterclockwise. Refer to Figure 8-21. During the RPG exercise, data is written to the Keyboard Column latches to test both states of the latches. First, a low is written to all four latches, and the counters run through their range. A high is then written to the latches, the counters run their range again, and the cycle repeats. Verify the waveforms in Figure 8-22. The four RPG Sign Latches all have identical waveforms. If the Enable lines have been verified but the latches fail, replace the defective latch.

Table 8-17. RPG Sign Latch Test Points

Function	Left RPG	Middle RPG	Right RPG	Plug-In RPG
Clock	U4, p11	U4, p3	U3, p11	U3, p3
D Input	U4, p12	U4, p2	U3, p12	U3, p2
Sign Output	U4, p9	U4, p5	U3, p9	U3, p5

Exit the RPG Self-Test as follows:

1. Turn off the line power.
2. Close all S1 switches and open all S2 switches to return the Front Panel to NORMAL operation.
3. Turn line power on.

Digital Display Failure

The Digit Exercise Routine checks each digit and each segment of the digital display. Enter SHIFT 0 5 to initiate the test. Observe the sequence of the Front Panel digital displays as illustrated in Figure 8-12.

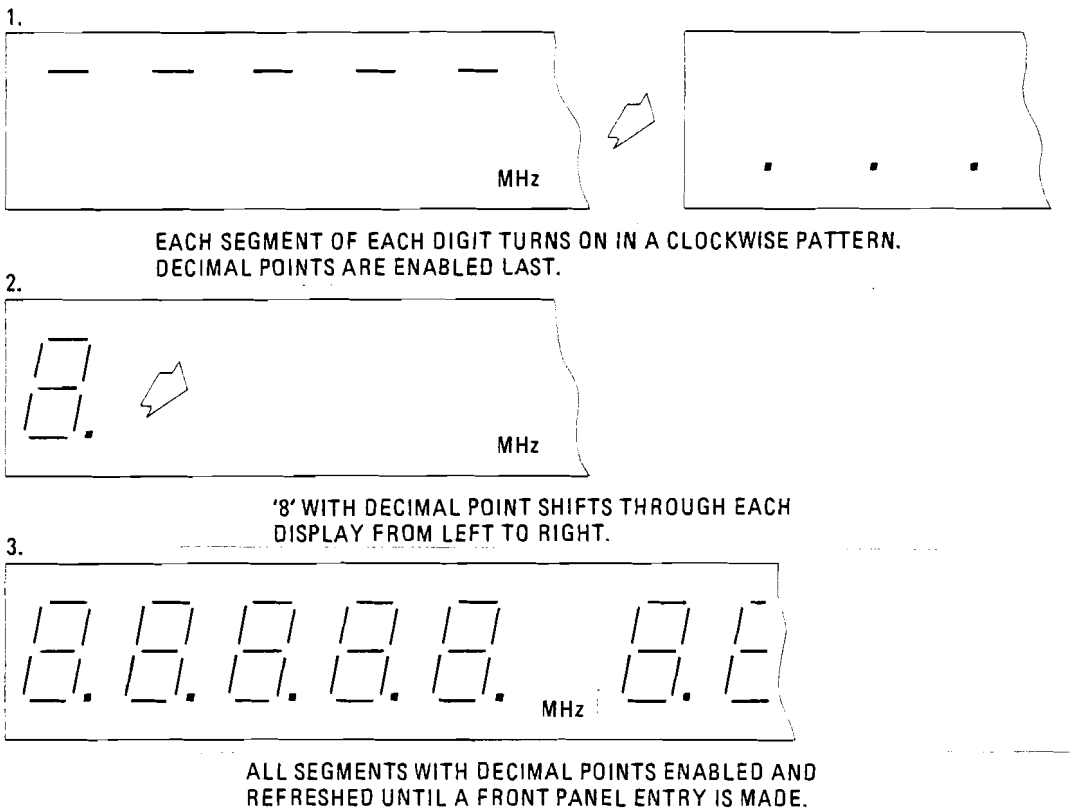


Figure 8-12. Digit Exercise Routine

Digit drivers (A1U1 and A1U2) and Segment latch (U22) can be verified while the Front Panel is in the last enabled state of the Digit Exercise Routine (all segments with decimal points enabled and continuously refreshed). In this mode, U22 outputs should all read low. The outputs of A1U1 and A1U2 should go low sequentially, at a 100 Hz rate.

A missing segment indicates a faulty data line, U22 failure, problems in the A1 Segment Drivers, or bad LEDs. A missing digit indicates a faulty Digit Counter, Digit Driver, or problems in the LED display.

The data written to each digit is stored in RAM on the A3 Microprocessor while the test data is taken from ROM. Therefore, if the Digit Exercise Routine test appears normal, yet indecipherable or random characters appear in the Digital Display during normal operation, suspect a RAM failure on the A3 Microprocessor.

Annunciator Failure

Several Self-Tests are available to test the annunciators:

1. Press **INSTR PRESET** and hold. All LEDs should turn on. This is the easiest way to test for burned out LEDs.

2. Annunciator Self-Test is initiated by entering **SHIFT** **1** **8** . During this test, all front panel annunciators (except SWP) are turned on and off together at a 1 Hz rate. LEDs which are locked on or off, or groups of annunciators addressed by a faulty enable line are easily identified. Table 8-12, Annunciator Address Decoding, cross references annunciators with the appropriate address.

3. Hex Address Write/Read: By entering the address of a group of Annunciators, data can be written to light any combination of LEDs. To initiate the test enter SHIFT 0 0. Then enter an address between 1801 and 1805. Refer to Table 8-12. Press M2, and enter the two hex digits of data to be written to that address:

   - Enter 0 0 (0000 0000) to light all LEDs in the addressed group.
   - Press BK SP, BK SP, which enters FF, (1111 1111) and turns off all LEDs in the addressed group.
   - By alternating between 5 5 (0101 0101) and , , which enters AA, (1010 1010), adjacent shorts can be found.

   To enter a new address, press M1 and the new address; or use the ▲ ▼ keys to step to the new address.

Front Panel Interrupt Timer and Interrupt Control

Failures in the Front Panel Interrupt Timer or Control blocks, generally, will either prevent Front Panel interrupts or cause them continuously, resulting in various front panel displays. Usually the front panel will not respond to RPG or keyboard entry.

1. Remove the A5 board to prevent retrace interrupts.
2. Press INSTR PRESET.
3. Check the LFPSTB line (TP13) for pulses at approximately 823 kHz.
4. Check Interrupt Timer counters (U20A, U20B, and U19A) for divide-by-two sequence. (NOTE: The pulse at TP3 is immediately reset and of extremely short duration).
5. Check LDE (TP6) and LDCINCR (TP7) for the waveforms shown in Figure 8-20. These lines should be set regularly at 720 microsecond intervals, but their active states are of various durations.
6. Finally, check A3TP7 for the waveform in Figure 8-20, to make sure the interrupt requests are being transmitted to the microprocessor.

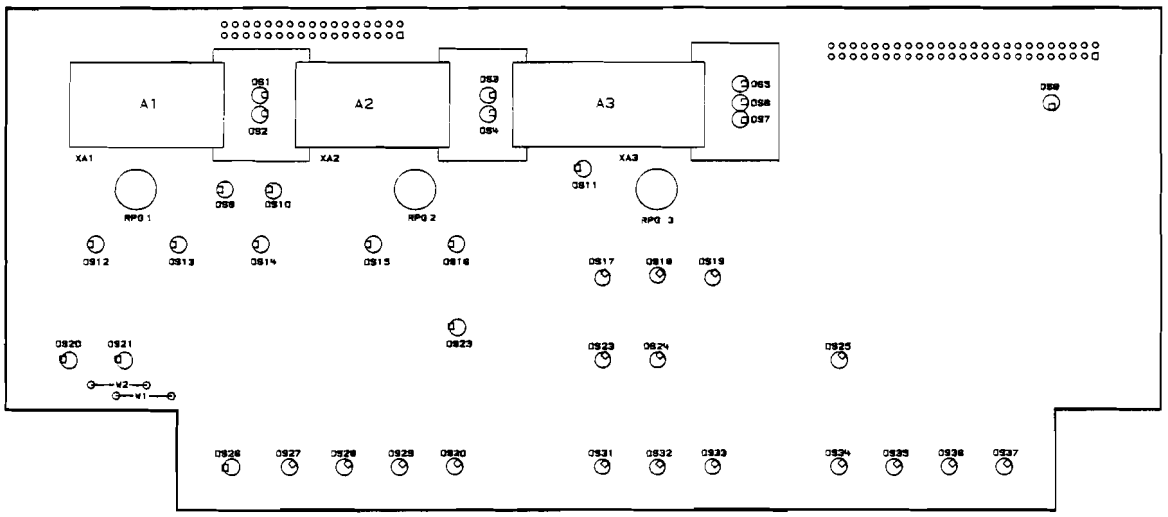
If A3TP7 remains low, the Microprocessor is being continuously interrupted. Connect a jumper between IRQE (A3 TP21) and GND (A3 TP14) to disable the interrupts, and then examine the circuits above to determine why the interrupts cannot be cleared. Ensure that the plug-in (TP 31) and HP-IB (TP 29) are not requesting service. If necessary, remove the plug-in from the mainframe and A8 from its Motherboard socket to make troubleshooting easier.

Table 8-12. Annunciator Address Decoding

Mnemonic	Address	Data Bit	Description/Explanation
LDS1	1801	2	GHz (Frequency Left)
LDS2	1801	6	MHz
LDS3	1801	4	GHz (Frequency Right)
LDS4	1801	3	MHz
LDS5	1801	5	GHz (Frequency/Time)
LDS6	1801	0	MHz
LDS7	1801	1	sec
(NC)	1801	7	
LDS8	1803	0	ALTn
LDS9	1801	7	VERNIER/OFFSET
LDS10	1805	3	VERNIER/OFFSET # 0
LDS11	1802	2	MKR Delta
LDS12	1803	5	START
LDS13	1803	3	CW
LDS14	1803	6	CF
LDS15	1803	2	Delta F
LDS16	1804	4	STOP
LDS17	1802	1	M1
LDS18	1802	0	M2
LDS19	1802	6	M3
LDS20	1802	4	REM
LDS21	1803	1	ADRS'D
LDS22	1805	4	MARKER SWEEP
LDS23	1804	6	M4
LDS24	1804	5	M5
LDS25	1803	4	Shift
LDS26	**	#	SWP
LDS27	1804	3	INT (Sweep Trig)
LDS28	1804	2	LINE (Sweep Trig)
LDS29	1804	1	EXT (Sweep Trig)
LDS30	1804	0	SINGLE (Sweep Trig)
LDS31	1804	7	EXT (Sweep)
LDS32	1802	3	MAN (Sweep)
LDS33	1802	5	TIME (Sweep)
LDS34	1805	2	AMPTD MKR
LDS35	1803	7	DISPL BLANK
LDS36	1805	0	RF BLANK
LDS37	1805	1	Square-Wave MOD

A1

FRONT



REAR

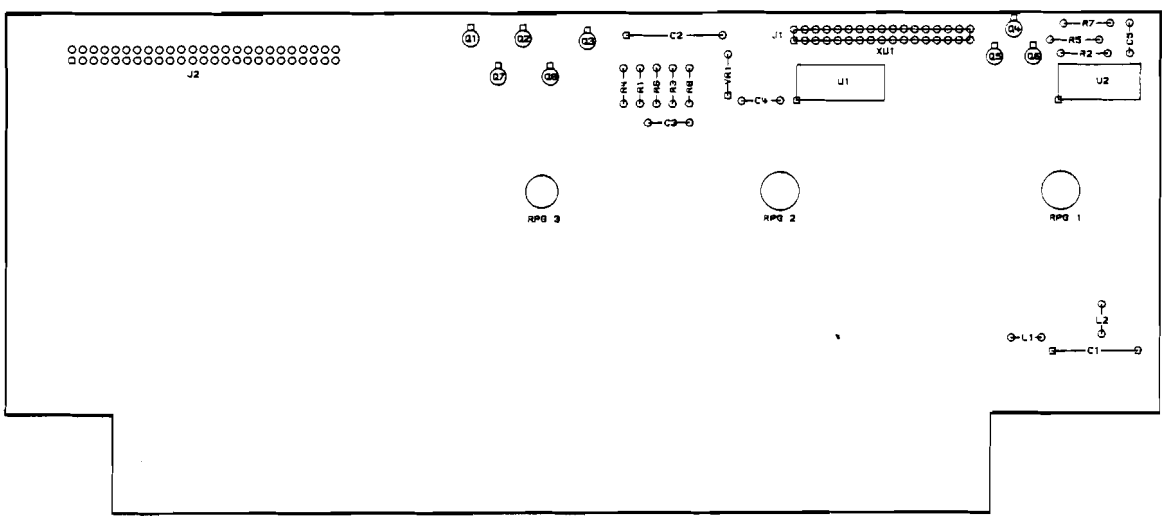


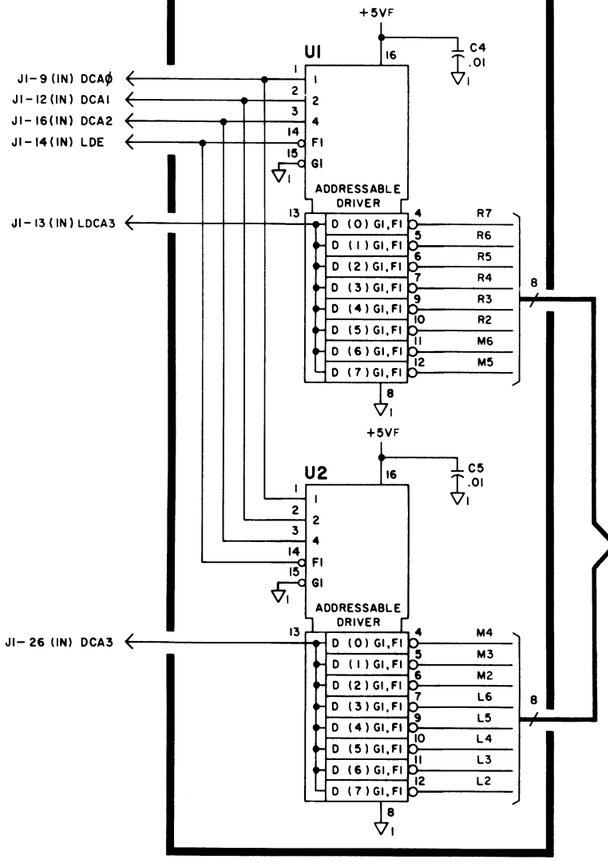
Figure 8-13. A1 Front Panel, Component Locations

A2J3	A2J3/A1J1 INTERCONNECT				A1J1
PIN	FUNCTION	SIGNAL	TO/FROM	FUNCTION	PIN
1	D	IC2	→	E	1
2	D	IC3	→	E	2
3	D	IC1	→	E	3
4	G	RPG3A	←	C	4
5	F	Ca	→	B	5
6	G	RPG3B	←	C	6
7	F	Cd	→	B	7
8	F	Cf	→	B	8
9	F	DCA0	→	A	9
10	F	Cc	→	B	10
11		NOT USED			11
12	F	DCA1	→	A	12
13	F	LDCA3	→	A	13
14	E	LDE	→	A	14
15	D	LDS10	→	E	15
16	F	DCA2	→	A	16
17	J	+5VR	→	G	17
18	J	+5VR	→	G	18
19	G	RPG2B	←	C	19
20	D	LDS22	→	E	20
21	G	RPG2A	←	C	21
22	J	GND R		G	22
23	J	GND R		G	23
24	J	GND R		G	24
25	A	LPRESET	←	F	25
26	F	DCA3	→	A	26
27	D	LPRESET	→	F	27
28	F	Cdp	→	B	28
29	G	RPG1B	←	C	29
30	F	Cc	→	B	30
31	G	RPG1A	←	C	31
32	F	Cb	→	B	32
33	F	+5VF SENSE	←	B	33
34	F	Cg	→	B	34

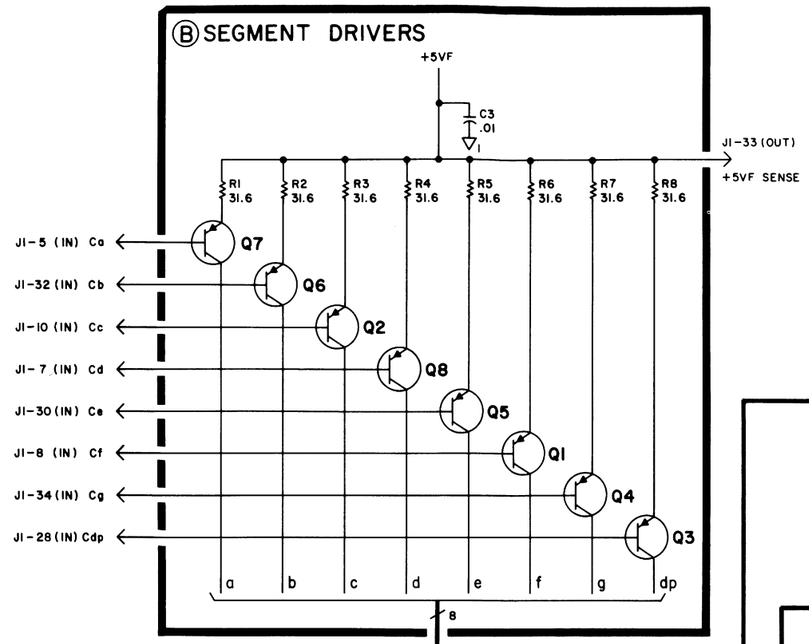
A2J4	A2J4/A1J2 INTERCONNECT				A1J2
PIN	FUNCTION	SIGNAL	TO/FROM	FUNCTION	PIN
1	H	R4	←	F	1
2	D	LDS34	→	E	2
3	H	R5	←	F	3
4	H	R1	←	F	4
5	H	C2	→	F	5
6	D	LDS37	→	E	6
7	D	LDS8	→	E	7
8	D	LDS36	→	E	8
9	H	C6	→	F	9
10	D	LDS35	→	E	10
11	H	C1	→	F	11
12	H	C7	→	F	12
13	H	C5	→	F	13
14	H	R3	→	F	14
15	H	C4	→	F	15
16	H	C0	→	F	16
17	D	LDS21	→	E	17
18	D	LDS14	→	E	18
19	D	LDS25	→	E	19
20	D	LDS12	→	E	20
21	D	LDS26	→	E	21
22	D	LDS13	→	E	22
23	D	LDS27	→	E	23
24	D	LDS15	→	E	24
25	D	LDS28	→	E	25
26	D	LDS16	→	E	26
27	D	LDS29	→	E	27
28	H	R6	←	F	28
29	D	LDS30	→	E	29
30	H	C3	→	F	30
31	D	LDS31	→	E	31
32	D	LDS23	→	E	32
33	D	LDS32	→	E	33
34	D	LDS24	→	E	34
35	D	LDS33	→	E	35
36	D	LDS20	→	E	36
37	D	LDS17	→	E	37
38	D	LDS11	→	E	38
39	H	R0	←	F	39
40	H	R2	←	F	40
41	D	LDS9	→	E	41
42	D	LDS19	→	E	42
43	D	LDS4	→	E	43
44	D	LDS18	→	E	44
45	D	LDS5	→	E	45
46	D	LDS3	→	E	46
47	D	LDS7	→	E	47
48	D	LDS1	→	E	48
49	D	LDS6	→	E	49
50	D	LDS2	→	E	50

A1 FRONT PANEL
08350-60021

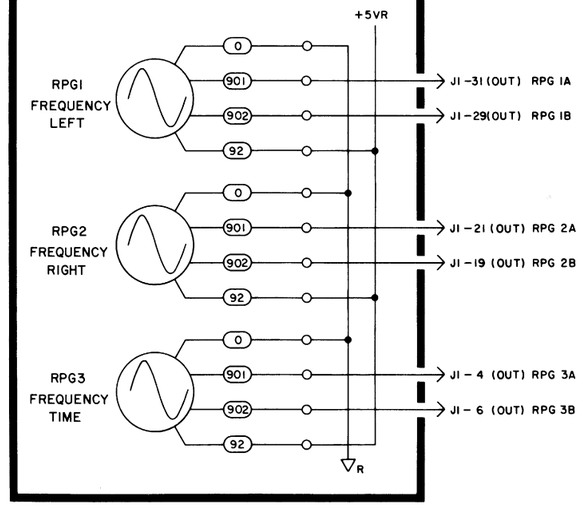
Ⓐ DIGIT DRIVERS



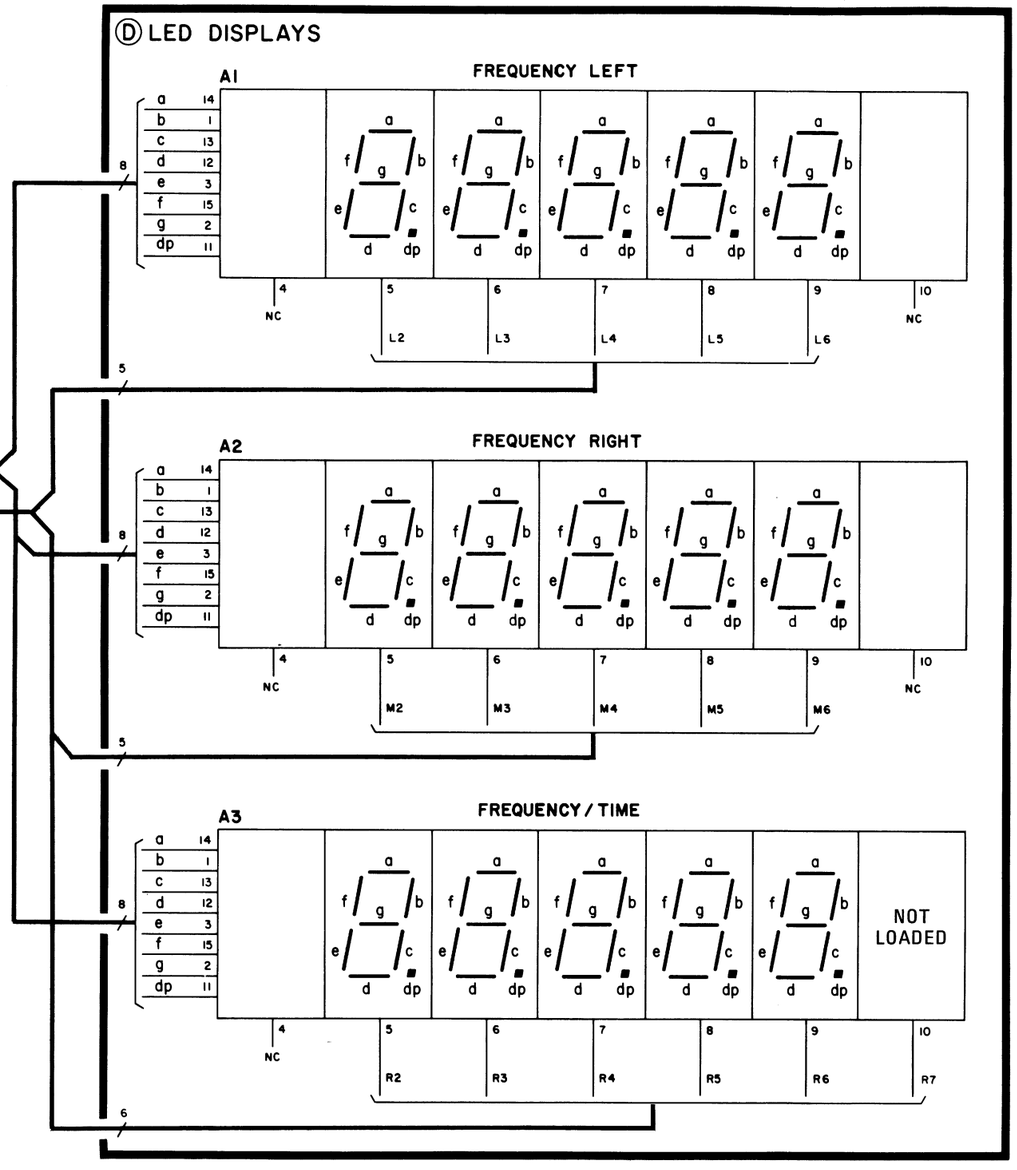
Ⓑ SEGMENT DRIVERS



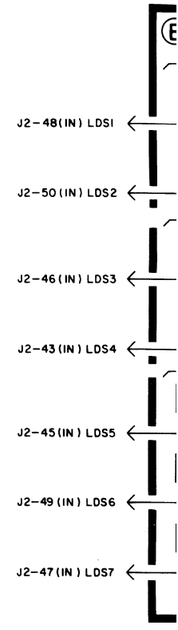
Ⓒ RPG's



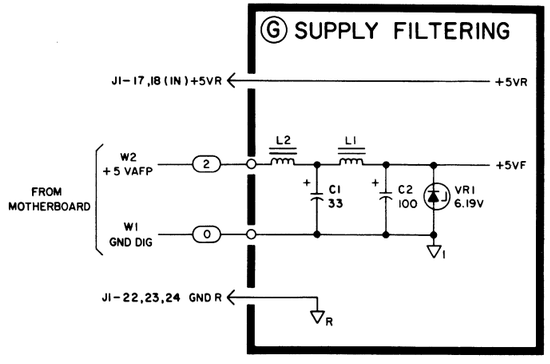
Ⓓ LED DISPLAYS



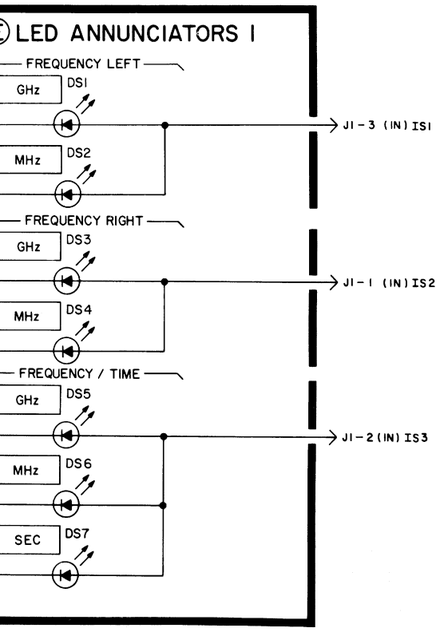
Ⓔ

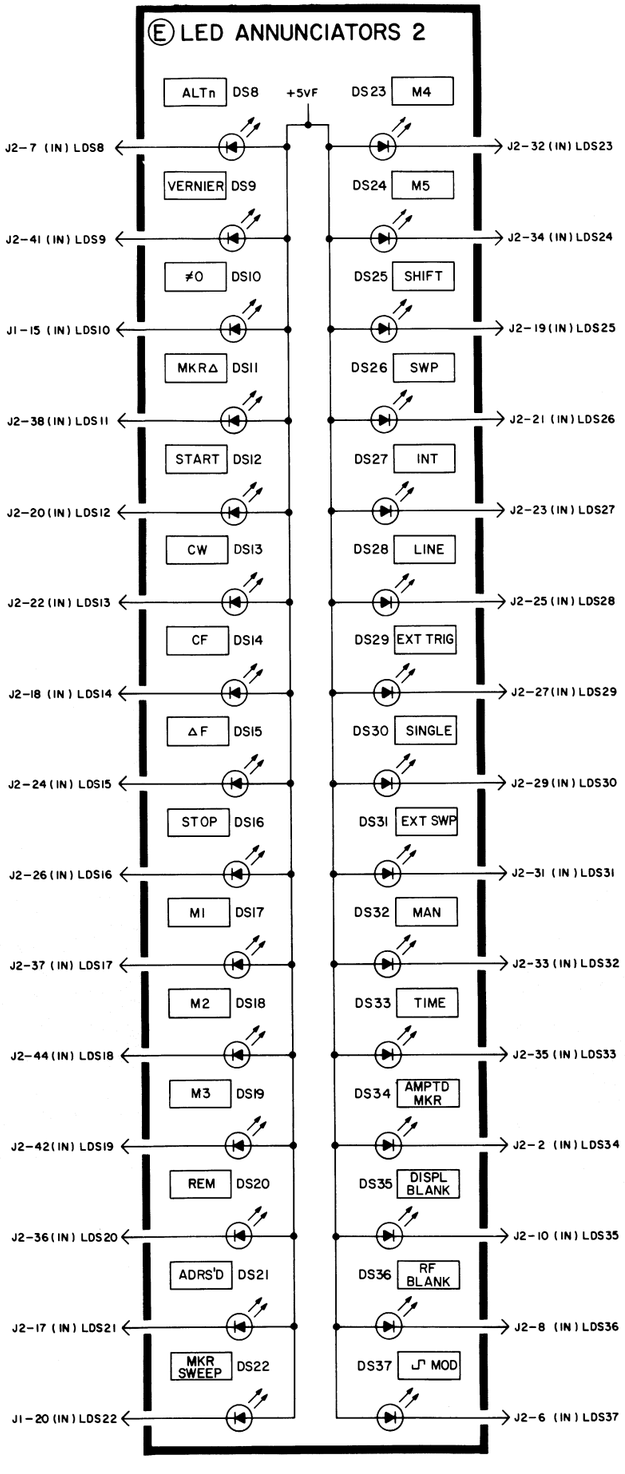


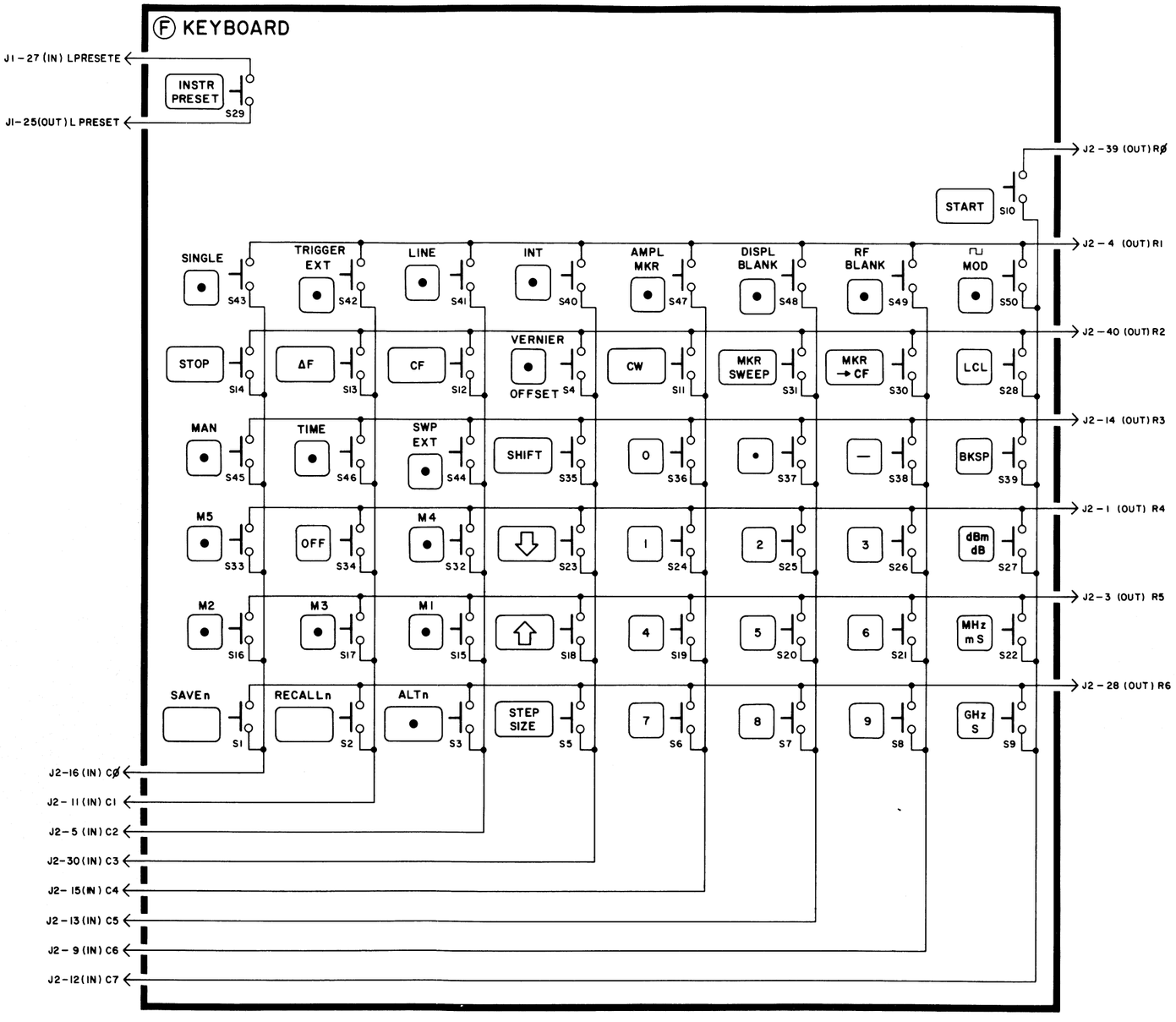
Ⓖ SUPPLY FILTERING



SERIAL PREFIX: 2024A







NOTE

MPLIFIED BLOCK DIAGRAM
R A1 FRONT PANEL IS
MBINED WITH A2 FRONT
NEL INTERFACE, AND IS
CATED ON THE FOLDED A2
RVICE SHEET.

A1

Figure 8-14. A1 Front Panel, Schematic Diagram

A1 FRONT PANEL and A2 FRONT PANEL INTERFACE, CIRCUIT DESCRIPTION

NOTE

Because of the electrical and physical structure of the A1/A2 interface, the two boards are discussed simultaneously. Therefore, block diagrams, circuit description, and trouble-shooting procedures have been combined and completely reprinted in both the Al and A2 Service Sheets.

The A2 Front Panel Interface Assembly contains all the necessary circuitry to allow bidirectional communication between the A3 Microprocessor Assembly and the A1 Front Panel functions. Table 8-13 indexes the rate of data transfer between the Microprocessor and the various Front Panel registers. The A1/A2 Block Diagram is shown in Figure 8-17. The following circuit description is broken down by front panel function: Address Decoder, Keyboard, RPGs, Digital Display, Annunciators, and Interrupt circuitry.

Table 8-13. A2 Activity Rate

ACTIVITY	RATE (approximate)
Refresh Display	1.6 kHz (Each display has an individual refresh rate of 100 Hz. (1.6 kHz÷16 digits))
Scan Keyboard	200 Hz (Debounce at a 30 Hz rate if active.)
Read RPGs	60 Hz
Blink Annunciators: GHz, MHz (for out-of-range indication and blink active marker annunciator).	150 Hz

NOTE

All reference designations refer to A2 components unless otherwise noted.

Address Decoder A2: (B)

Three-to-eight decoders, U23 and U31 interpret the Front Panel Bus address lines, LFPA0 through LFPA2. Decoder outputs enable the particular devices to be addressed by the Microprocessor during data transfer. Decoding activity is determined by three enable lines: FPE (Front Panel Enable) and LFPSTB (Low=Front Panel Strobe) allow access to the front panel; LFPRD (Low=Front Panel Read) determines the direction of data flow (read or write) at the addressed device. Note that all A2 latches are unidirectional. U23 decodes all READ enables while U31 decodes all WRITE enables, allowing the overlap of 1800-series addresses. Only fourteen of the sixteen possible enable lines from U23 and U31 are used: LRE1–4, LRE6–8, LWE1–6, and LWE8. Table 8-14 provides decoding information.

Table 8-14. Address Decoding

Mnemonic	Address	Location	Read/Write	Test Point	Description
LRE1	1800H	U15	Read	23	Read Keyboard Row Sense
LRE2	1801H	U10	Read	9	Read RPG Sign/Digit and Digital Counter
LRE3	1802H	U11	Read	11	Read RPG1/RPG2 Counts
LRE4	1803H	U12	Read	16	Read RPG3/PIRPG Counts
LRE5					Not Used
LRE6	1805H	U8B	Read	4	Clear Retrace Interrupt
LRE7	1806H	U5A/B U6A/B	Read	8	Reset RPG Counters
LRE8	1807H	U7	Read	26	Read Column Data (Self-Test)
LWE1	1800H	U16	Write	25	Latch Keyboard Column Data
LWE2	1801H	U13	Write	22	Latch Annunciator Data
LWE3	1802H	U25	Write	21	Latch Annunciator Data
LWE4	1803H	U27	Write	17	Latch Annunciator Data
LWE5	1804H	U26	Write	20	Lateh Annunciator Data
LWE6	1805H	U24	Write	18	Latch Annunciator Data
LWE7					Not Used
LWE8	1807H	U8A	Write	10	Enables Display/Clears Front Panel Interrupt

Keyboard A1: (F) A2: (A) (H)

The Microprocessor periodically uses the Keyboard Interface circuits for scanning the Keyboard state. Coded data is loaded into the Column Strobing Latch U16 by the Microprocessor. The resulting row data from the keyboard matrix (F) is read back when U15 is enabled. The Microprocessor scans the Keyboard Interface at a rate of 200 Hz to determine whether a keyboard pushbutton has been pressed.

Two additional signals are scanned through the keyboard interface:

LPRESET. When the line power is cycled or INSTR PRESET is pressed, the microprocessor resets and initiates Self-Test. In either case PWON (A) is driven low to reset latches and flip-flops. However, the Microprocessor must determine which action caused the reset in order to execute the appropriate RAM initialization routine. If the instrument ON/OFF switch is toggled, the Microprocessor will clear all RAM registers (not true for 8350A Opt. 001). If INSTR PRESET has been pressed, LPRESET signal will be detected at U15, bit 7. In this case, the SAVE/RECALL registers are not cleared.

LSTPADV. Low Step Up Advance, from the rea
J13, increments the Step Up function for the a
registers).

RPGs (Rotary Pulse Generation) A2: (G

RPG Interface circuitry senses the direction o
output of four RPGs: three on the 8350A Front P
RF plug-in. There are two pulse train outputs fro
relationship of the pulse train pair is sensed by a
translates the RPG direction (+, −) of rotatio
processor reads the flip-flop outputs and increm
display accordingly.

One pulse train output from each RPG clocks a
When LRE3 and LRE4 go low, the counter outp
and read by the Microprocessor. Data is then wr
(U22) and eventually used to update the display
after each READ enable.

Front Panel Interrupt Routine A2: (C) (

The following signals, used to interrupt the Mic

LDE: Low=Display Enable, TP6.
LRTS: Low=Retrace Strobe, P1-42
LRE6: Low=Read Enable 6, TP4.
LWE8: Low=Write Enable 8, TP10.
LFPIRQ: Low=Front Panel Interrupt Req
DSPCLK: Display Clock, TP3.
LDCINCR: Low=Digit Counter Incremen
LRTCIRQ: Low=Retrace Interrupt Reque

A series of three digital counters (U20A, U20B, a
functions. LFPSTB is being used as an 823 kH
processor I/O Strobe data transfer timing signa
counters during each machine cycle of the mic

DSPCLK pulses at approximately 1.6 kHz (82
resets LDCINCR low, to increment the digit c
request (LFPIRQ) to the Microprocessor. At thi
displays while the Microprocessor services the in
holds the FP Interrupt Timer. LWE8 sets LDE
simultaneously latches the new data into U22 (
clear the interrupt request.

LRTS, from the A5 Sweep Generator assembly,
retrace and sets LFPIRQ and LRTCIRQ low. Th
interrupt is a function of the retrace (LRTCIRQ) a
the instrument. LRE6 clears the retrace interru

Digital Display Control A1: (A) A2: (F)

Each time LFPIRQ is set low, LDCINCR increm
Microprocessor executes the Front Panel Interr
routine, the Microprocessor refreshes one displa
A1U2 decode the outputs of Digit Counter U19B
updated. The refresh rate per digit is approxi
maintain a flicker-free display.

A2 FRONT PANEL INTERFACE, CIRCUIT

NOTE

trical and physical structure of the A1/A2 boards are discussed simultaneously. agrams, circuit description, and trouble- s have been combined and completely he AI and A2 Service Sheets.

ssembly contains all the necessary circuitry to allow between the A3 Microprocessor Assembly and the e 8-13 indexes the rate of data transfer between the s Front Panel registers. The A1/A2 Block Diagram llowing circuit description is broken down by front der, Keyboard, RPGs, Digital Display, Annunci-

ble 8-13. A2 Activity Rate

RATE (approximate)
1.6 kHz Each display has an individual refresh rate of 100 Hz. (1.6 kHz÷16 digits))
200 Hz (Debounce at a 30 Hz rate if active.)
60 Hz
150 Hz

NOTE

nations refer to A2 components unless

nd U31 interpret the Front Panel Bus address lines, oder outputs enable the particular devices to be ssor during data transfer. Decoding activity is lines: FPE (Front Panel Enable) and LFPSTB w access to the front panel; LFPRD (Low=Front ection of data flow (read or write) at the addressed are unidirectional. U23 decodes all READ enables E enables, allowing the overlap of 1800-series sixteen possible enable lines from U23 and U31 are 1–6, and LWE8. Table 8-14 provides decoding

Table 8-14. Address Decoding

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LRE4	1803H	U12	Read	16	Read RPG3/PIRPG Counts
LRE5					Not Used
LRE6	1805H	U8B	Read	4	Clear Retrace Interrupt
LRE7	1806H	U5A/B U6A/B	Read	8	Reset RPG Counters
LRE8	1807H	U7	Read	26	Read Column Data (Self-Test)
LWE1	1800H	U16	Write	25	Latch Keyboard Column Data
LWE2	1801H	U13	Write	22	Latch Annunciator Data
LWE3	1802H	U25	Write	21	Latch Annunciator Data
LWE4	1803H	U27	Write	17	Latch Annunciator Data
LWE5	1804H	U26	Write	20	Latch Annunciator Data
LWE6	1805H	U24	Write	18	Latch Annunciator Data
LWE7					Not Used
LWE8	1807H	U8A	Write	10	Enables Display/Clears Front Panel Interrupt

Keyboard A1: (F) A2: (A) (H)

The Microprocessor periodically uses the Keyboard Interface circuits for scanning the Keyboard state. Coded data is loaded into the Column Strobing Latch U16 by the Microprocessor. The resulting row data from the keyboard matrix (F) is read back when U15 is enabled. The Microprocessor scans the Keyboard Interface at a rate of 200 Hz to determine whether a keyboard pushbutton has been pressed.

Two additional signals are scanned through the keyboard interface:

LPRESET. When the line power is cycled or INSTR PRESET is pressed, the microprocessor resets and initiates Self-Test. In either case PWON (A) is driven low to reset latches and flip-flops. However, the Microprocessor must determine which action caused the reset in order to execute the appropriate RAM initialization routine. If the instrument ON/OFF switch is toggled, the Microprocessor will clear all RAM registers (not true for 8350A Opt. 001). If INSTR PRESET has been pressed, LPRESET signal will be detected at U15, bit 7. In this case, the SAVE/RECALL registers are not cleared.

LSTPADV. Low Step Up Advance, from the rear panel Programming Connector J13, increments the Step Up function for the active mode (i.e., SAVE/RECALL registers).

RPGs (Rotary Pulse Generation) A2: (G)

RPG Interface circuitry senses the direction of rotation and counts the pulsed output of four RPGs: three on the 8350A Front Panel and one on the 83500 series RF plug-in. There are two pulse train outputs from each RPG. The Lead/Lag phase relationship of the pulse train pair is sensed by a flip-flop (U3A/B, U4A/B) which translates the RPG direction (+, −) of rotation. See Figure 8-21. The Microprocessor reads the flip-flop outputs and increments or decrements the numeric display accordingly.

One pulse train output from each RPG clocks a four-bit counter (U5A/B, U6A/B). When LRE3 and LRE4 go low, the counter outputs are enabled onto the data bus and read by the Microprocessor. Data is then written to the Display Control Latch (U22) and eventually used to update the display segments. RE7 resets the counters after each READ enable.

Front Panel Interrupt Routine A2: (C) (E)

The following signals, used to interrupt the Microprocessor, are discussed below:

LDE: Low=Display Enable, TP6.
LRTS: Low=Retrace Strobe, P1-42
LRE6: Low=Read Enable 6, TP4.
LWE8: Low=Write Enable 8, TP10.
LFPIRQ: Low=Front Panel Interrupt Request, P1-23.
DSPCLK: Display Clock, TP3.
LDCINCR: Low=Digit Counter Increment, TP7.
LRTCIRQ: Low=Retrace Interrupt Request, TP5.

A series of three digital counters (U20A, U20B, and U19A) perform divide-by-two functions. LFPSTB is being used as an 823 kHz time base, tracking the Microprocessor I/O Strobe data transfer timing signal. Therefore, LFPSTB clocks the counters during each machine cycle of the microprocessor.

DSPCLK pulses at approximately 1.6 kHz (823 kHz ÷ 512). Each rising pulse resets LDCINCR low, to increment the digit counter (F), and sets the interrupt request (LFPIRQ) to the Microprocessor. At this time LDE is high to disable the displays while the Microprocessor services the interrupt. High LDE also resets and holds the FP Interrupt Timer. LWE8 sets LDE low to enable the displays, and simultaneously latches the new data into U22 (F). LWE8 also resets LFPIRQ to clear the interrupt request.

LRTS, from the A5 Sweep Generator assembly, occurs coincident with the sweep retrace and sets LFPIRQ and LRTCIRQ low. The Microprocessor senses that the interrupt is a function of the retrace (LRTCIRQ) and initiates a complete update of the instrument. LRE6 clears the retrace interrupt request.

Digital Display Control A1: (A) A2: (F)

Each time LFPIRQ is set low, LDCINCR increments Digit Counter U19B and the Microprocessor executes the Front Panel Interrupt Service Routine. During the routine, the Microprocessor refreshes one display digit. Digit Drivers, A1U1 and A1U2 decode the outputs of Digit Counter U19B to determine which digit will be updated. The refresh rate per digit is approximately 100 Hz, fast enough to maintain a flicker-free display.

With each low-to-high transition of LWE8, U22 latches data which determines the segment states for the active digit. Resistor and diode networks (U30, U29, and U21) bias Segment Drivers A1Q1 through A1Q8. A low data bit to U22 activates the corresponding segment driver, producing a 30 mA current source. A high data bit input (greater than or equal to 2V) turns off the segment driver. Figure 8-15 shows the simplified schematic.

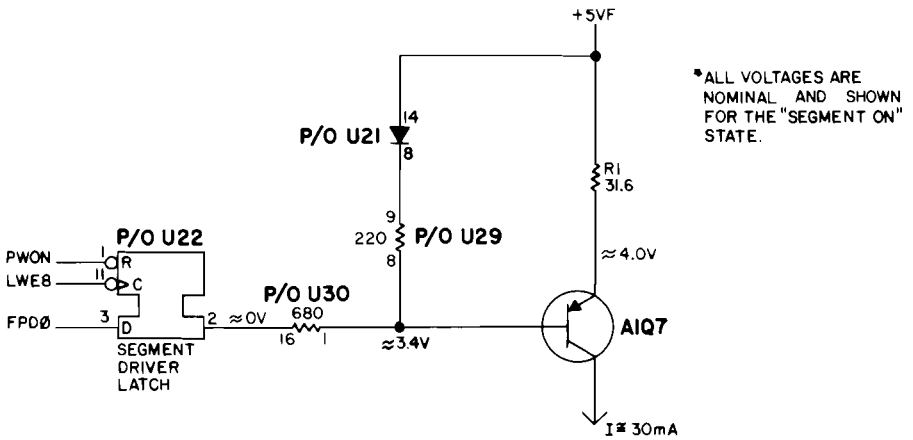


Figure 8-15. Typical Segment Driver Schematic

Annunciators A1: Ⓔ A2: Ⓓ

Five latches (U13, U24–U27) with current limiting resistors, latch and buffer data to drive the Front Panel annunciators (with the exception of SWP). Q1 through Q6 provide three constant current sources to ensure uniform intensity in the unit Annunciators (i.e., GHz, MHz, sec). LPRESETE signal is stored in the Annunciator function block.

A1/A2 TROUBLESHOOTING PROCEDURE

NOTE

Because of the electrical and physical structure of the A1/A2 interface, the two boards are discussed simultaneously. Therefore, block diagrams, circuit descriptions, and troubleshooting procedures have been combined and completely reprinted in both Al and A2 Service Sheets.

Since the 8350A Instrument Self-Test, does not detect all possible Front Panel failures, A1/A2 troubleshooting information is divided into two major sections: A. Front Panel Self-Test FAIL; B. Front Panel Self-Test PASS. Each section outlines suspect areas and component level troubleshooting.

PRELIMINARY CHECKS

Perform a brief visual inspection of the A2 board for physical or heat damage. Check the following: +5V supply at TP 15; that LPRESET (TP 1) and PWON (TP 2) are both high during normal instrument operation; that all S1 switches are closed and all S2 switches open for NORMAL operation; that A1/A2 ribbon cable connections are firmly seated over the correct pins.

NOTE

All reference designations refer to A2 components unless otherwise noted.

NOTE

Timing diagrams referenced for A1/A2 Troubleshooting are located on the A2 Service Sheet.

A. FRONT PANEL SELF-TEST FAIL

The A2 Front Panel Interface board is exercised and checked as part of the Self-Test routine performed at each "turn-on" or Instrument Preset. (Refer to Table 8-8, Self-Test Flowchart, in the Overall Troubleshooting section for details.)

If the microprocessor detects a Front Panel failure, the instrument Self-Test sequence will be aborted and the Front Panel Self-Test will be cycled continuously. In this mode, all Front Panel annunciators will be lit, and a single numeral '8' with its decimal point will flicker sequentially from right to left across the digit display. The Error Code E006 will not appear in the Front Panel Digital Display, however, the Error Code LEDs on the A3 Microprocessor Board and the Sweep Trigger annunciators will display the code in its binary form: 0110 ('1' turns the LED on).

The Front Panel error code indicates a possible failure in the Address Decoder, Data Bus, Column Latch, or the Self-Test Buffer. To troubleshoot these areas place A2 on an extender board. Push INSTR PRESET to allow the failure to begin the repetitive test. Troubleshoot as described below.

Address Decoder

During the Front Panel Self-Test, each of the Read Enables (U23) is addressed to enable in sequence, followed by each Write Enable (U31). The Write Enable sequence starts with LWE2 enabled first and LWE1 enabled last. (Note: additional pulses appear on the LWE1, LWE2, LWE5, and LWE8 lines slightly later and throughout the cycle).

Set the oscilloscope at a sweep speed of 50 microseconds/division and externally trigger from LRE1 (TP23). Verify proper pulse location and duration of each Address Decoder line. Refer to Figure 8-19. If any lines cannot be verified, check the LFPRD, LFPSTB, FPE, and address lines for activity. If any of these signals are missing, trace the lines back to the A3 Microprocessor board and the Front Panel buffers, A3U22 and A3U32. If the Microprocessor busses and control lines appear dead, perform the Free Run Test described in the A3 Troubleshooting Section.

Data Bus, Column Latch, and Self-Test Buffer

To verify proper functioning of Keyboard Column Latch U16, a binary '1' is stepped through each column (C0—C7) while a '0' is written to the other seven. After a delay, LRE8 is pulsed low. The latched data is read back to the microprocessor through the Self-Test buffer (U7) and verified. The next LWE1 pulse clears the bit and shifts the '1' to the next column.

Check the inputs and outputs of U7 against Figure 8-19. This exercise thoroughly checks the Data Bus and partially verifies the Address Bus, Address Decoder Block, and FPE and LFPRD lines.

B. FRONT PANEL SELF-TEST PASS

If an Error Code E005 or lower, or no Error Code, occurs during power-up or INSTR PRESET, the Front Panel Self-Test routine has been successfully performed. This verifies that the Front Panel Data Bus, Address Bus, Keyboard Column buffer, Self Test buffer, and part of the Address Decoder block are functioning correctly.

If symptoms apparent at the Front Panel indicate a failure in the Keyboard, RPGs, Annunciators, or Digital Display, refer to the apropriate section below for further troubleshooting. If the entire Front Panel does not respond, but the A3 Microprocessor board has been verified, refer to the Interrupt Control section below and Address Decoder troubleshooting outlined earlier.

The following troubleshooting procedures utilize the repetitive mode of the Front Panel Self-Test. The routine can be initiated as follows:

1. If the 8350A responds to front panel commands, simply enter SHIFT 0 8.

2. If the 8350A does not respond to Front Panel commands, connect a jumper between LTEST (A3 TP20) and GND (A3 TP14). Press INSTR PRESET or cycle the line power.

Keyboard Failure

Since the instrument passed the Front Panel Self-Test, the Keyboard Column latches and Data Bus are functioning properly. If the Keyboard is not working, suspect the LRE1 line, the Keyboard Row sense driver (U15), or the Keyboard matrix:

1. Initiate the Front Panel Self-Test and check the LRE1 line against Figure 8-19. If it is faulty, go back and troubleshoot the Address Decoder block.

2. Initiate the Front Panel Self-Test. While pressing a key, check that the appropriate Row line (input to U15) follows the corresponding Column line. See Figure 8-19. If these are normal, suspect U15. If this test fails, the problem lies in the keyboard matrix or interconnecting lines. Initiate the Key Code Test. (If the instrument will not execute the Key Code Test, troubleshoot the keyboard matrix.

3. Enter SHIFT 0 4 to initiate Key Code Test. Press any key and the appropriate code, indexed in Table 8-15, should appear in the digital display. If a depressed key is not being detected, the code will not light up. If two keys are shorted together, both will produce the same code. The Key Code Test should detect most keyboard failures. Further matrix troubleshooting should be performed with a continuity checker.

Table 8-15. Key Codes (1 of 2)

Pushbutton	Keycode	Column (U16)	Row (U15)
START	20	7	0
CW	24	4	2
CF	22	2	2
Delta F	23	1	2
STOP	21	0	2
VERNIER/OFFSET	25	3	2
LCL	1b	7	2
INSTR PRESET	*		
MKR→ CF	26	6	2
MKR SWEEP	27	5	2

Table 8-15. Key Codes (2 of 2)

Pushbutton	Keycode	Column (U16)	Row (U15)
M1	10	2	5
M2	11	0	5
M3	12	1	5
M4	13	2	4
M5	14	0	4
OFF	15	1	4
SAVEn	18	0	6
RECALLn	19	1	6
ALTn	1A	2	6
STEP SIZE	1C	3	6
Up Arrow	1d	3	5
Down Arrow	1E	3	4
0	0	4	3
1	1	4	4
2	2	5	4
3	3	6	4
4	4	4	5
5	5	5	5
6	6	6	5
7	7	4	6
8	8	5	6
9	9	6	6
.	A	5	3
-	b	6	3
GHz/s	C	7	6
MHz/ms	d	7	5
dB/dBm	E	7	4
BKSP	F	7	3
SHIFT	1F	3	3
INT (Sweep Trig)	28	3	1
LINE (Sweep Trig)	29	2	1
EXT (Sweep Trig)	2A	1	1
SINGLE (Sweep Trig)	2B	0	1
EXT (Sweep)	2C	2	3
MAN (Sweep)	2d	0	3
TIME (Sweep)	2E	1	3
AMPL MKR	30	4	1
DSPL BLANK	31	5	1
RF BLANK	32	6	1
⊔⊓ MOD	33	7	1

*Note: INSTR PRESET is not scanned through the Keyboard Matrix. It is enabled through Addr 1805, Data Bit 7 (Low to Enable).

Rotary Pulse Generator (RPG) Failure

If an RPG effects no Front Panel changes, check its +5VR supply and inspect wires for damage. Place A2 on an extender board. The RPG outputs are accessible at the inputs of U9. Carefully probe the two pin connections corresponding to the suspected RPG. Slowly rotate the RPG in each direction while observing the waveforms on a scope, and compare them to those in Figure 8-21. If no activity is seen, check continuity of RPG leads and A1/A2 interconnect ribbon cables. Before replacing the RPG, perform the RPG self-test described below.

During the RPG Self-Test, the actual RPG outputs are switched out of the circuit (S1 open). Data written to the Keyboard Column Latch (U16) by the Microprocessor is switched in (S2 closed) to pulse the RPG sign latches (U3/4) and counters (U5/6) repetitively.

CAUTION

The following steps must be performed in the order given or the instrument will lock up.

The RPG Self-Test is initiated by performing the following steps:

1. Turn off the line power.
2. Place A2 on an extender board.
3. Open all S1 switches.
4. Turn the line power on.
5. Enter SHIFT 1 7 (The digit display will go blank).
6. Close all S2 switches to place the Front Panel Interface in the TEST mode.

To examine the waveforms in the RPG Interface, externally trigger the oscilloscope from the non-inverting output of the RPG sign latch (U4, pin 5). Set the oscilloscope at a sweep speed of 100 to 200 microseconds/division. (TP11 or TP8 will sometimes provide adequate triggering.)

CAUTION

Use IC TEST CLIP, HP Part Number 1400-0734 when probing IC pins.

Read/Write Enables. The four Read Enable lines associated with the RPG circuitry (LRE2, LRE3, LRE4, and LRE7) are each pulsed low. Since the Keyboard Column latches are used to pulse the RPG circuitry, the LWE1 line is pulsed rapidly, and should be checked for activity. See Figure 8-22 for typical waveforms.

If the Enable lines cannot be verified, troubleshoot the Address Decoder block as described earlier.

RPG Counters. In the TEST mode, U5 and U6 count the number of pulses produced by Keyboard Column latch U16. Each 4-bit binary counter begins at 0 (Binary: 0000). They are clocked sixteen times, counting to 15 (Binary: 1111) and then overflow back to 0. Waveforms for each of the four counters are identical. See Figure 8-22. If the Enable lines have been verified but the counters fail, replace the defective counter.

Table 8-16. RPG Counter Test Points

Function	Left RPG	Middle RPG	Right RPG	Plug-In RPG
Clock	U5, p1	U5, p13	U6, p1	U6, p13
Counter (1) (LSB)	U5, p3	U5, p11	U6, p3	U6, p11
Counter (2)	U5, p4	U5, p10	U6, p4	U6, p10
Counter (4)	U5, p5	U5, p9	U6, p5	U6, p9
Counter (8) (MSB)	U5, p6	U5, p8	U6, p6	U6, p8

RPG Sign Latches. U3 and U4 are D Flip-Flops whose outputs depend on whether the RPG is being rotated clockwise or counterclockwise. Refer to Figure 8-21. During the RPG exercise, data is written to the Keyboard Column latches to test both states of the latches. First, a low is written to all four latches, and the counters run through their range. A high is then written to the latches, the counters run their range again, and the cycle repeats. Verify the waveforms in Figure 8-22. The four RPG Sign Latches all have identical waveforms. If the Enable lines have been verified but the latches fail, replace the defective latch.

Table 8-17. RPG Sign Latch Test Points

Function	Left RPG	Middle RPG	Right RPG	Plug-In RPG
Clock	U4, p11	U4, p3	U3, p11	U3, p3
D Input	U4, p12	U4, p2	U3, p12	U3, p2
Sign Output	U4, p9	U4, p5	U3, p9	U3, p5

Exit the RPG Self-Test as follows:

1. Turn off the line power.
2. Close all S1 switches and open all S2 switches to return the Front Panel to NORMAL operation.
3. Turn line power on.

Digital Display Failure

The Digit Exercise Routine checks each digit and each segment of the digital display. Enter SHIFT 0 5 to initiate the test. Observe the sequence of the Front Panel digital displays as illustrated in Figure 8-16.

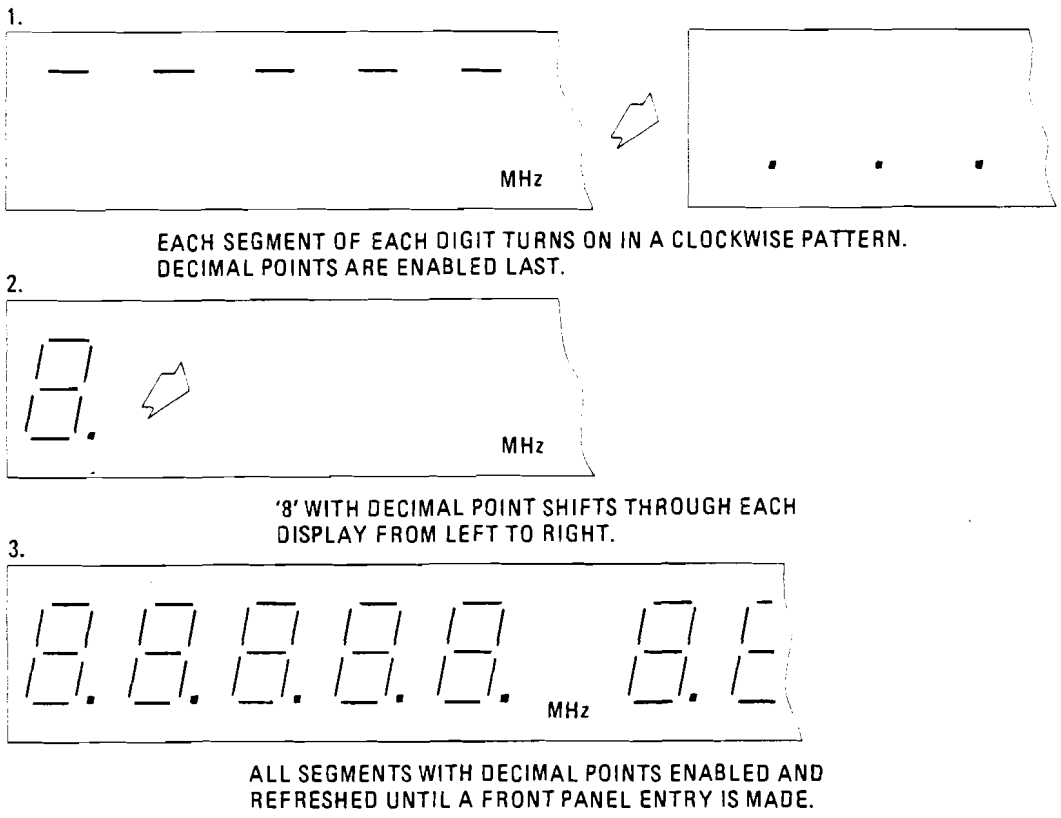


Figure 8-16. Digit Exercise Routine

Digit drivers (A1U1 and A1U2) and Segment latch (U22) can be verified while the Front Panel is in the last enabled state of the Digit Exercise Routine (all segments with decimal points enabled and continuously refreshed). In this mode, U22 outputs should all read low. The outputs of A1U1 and A1U2 should go low sequentially, at a 100 Hz rate.

A missing segment indicates a faulty data line, U22 failure, problems in the A1 Segment Drivers, or bad LEDs. A missing digit indicates a faulty Digit Counter, Digit Driver, or problems in the LED display.

The data written to each digit is stored in RAM on the A3 Microprocessor while the test data is taken from ROM. Therefore, if the Digit Exercise Routine test appears normal, yet indecipherable or random characters appear in the Digital Display during normal operation, suspect a RAM failure on the A3 Microprocessor.

Annunciator Failure

Several Self-Tests are available to test the annunciators:

1. Press INSTR PRESET and hold. All LEDs should turn on. This is the easiest way to test for burned out LEDs.

2. Annunciator Self-Test is initiated by entering SHIFT 1 8. During this test, all front panel annunciators (except SWP) are turned on and off together at a 1 Hz rate. LEDs which are locked on or off, or groups of annunciators addressed by a faulty enable line are easily identified. Table 8-18, Annunciator Address Decoding, cross references annunciators with the appropriate address.

3. Hex Address Write/Read: By entering the address of a group of Annunciators, data can be written to light any combination of LEDs. To initiate the test enter SHIFT 0 0 . Then enter an address between 1801 and 1805. Refer to Table 8-18. Press M2 , and enter the two hex digits of data to be written to that address:

   - Enter 0 0 (0000 0000) to light all LEDs in the addressed group.
   - Press BK SP, BK SP, which enters FF, (1111 1111) and turns off all LEDs in the addressed group.
   - By alternating between 5 5 (0101 0101) and . ., which enters AA, (1010 1010), adjacent shorts can be found.

   To enter a new address, press M1 and the new address; or use the ▲ ▼ keys to step to the new address.

Front Panel Interrupt Timer and Interrupt Control

Failures in the Front Panel Interrupt Timer or Control blocks, generally, will either prevent Front Panel interrupts or cause them continuously, resulting in various front panel displays. Usually the front panel will not respond to RPG or keyboard entry.

1. Remove the A5 board to prevent retrace interrupts.
2. Press INSTR PRESET.
3. Check the LFPSTB line (TP13) for pulses at approximately 823 kHz.
4. Check Interrupt Timer counters (U20A, U20B, and U19A) for divide-by-two sequence. (NOTE: The pulse at TP3 is immediately reset and of extremely short duration).
5. Check LDE (TP6) and LDCINCR (TP7) for the waveforms shown in Figure 8-20. These lines should be set regularly at 720 microsecond intervals, but their active states are of various durations.
6. Finally, check A3TP7 for the waveform in Figure 8-20, to make sure the interrupt requests are being transmitted to the microprocessor.

If A3TP7 remains low, the Microprocessor is being continuously interrupted. Connect a jumper between IRQE (A3 TP21) and GND (A3 TP14) to disable the interrupts, and then examine the circuits above to determine why the interrupts cannot be cleared. Ensure that the plug-in (TP 31) and HP-IB (TP 29) are not requesting service. If necessary, remove the plug-in from the mainframe and A8 from its Motherboard socket to make troubleshooting easier.

Table 8-18. Annunciator Address Decoding

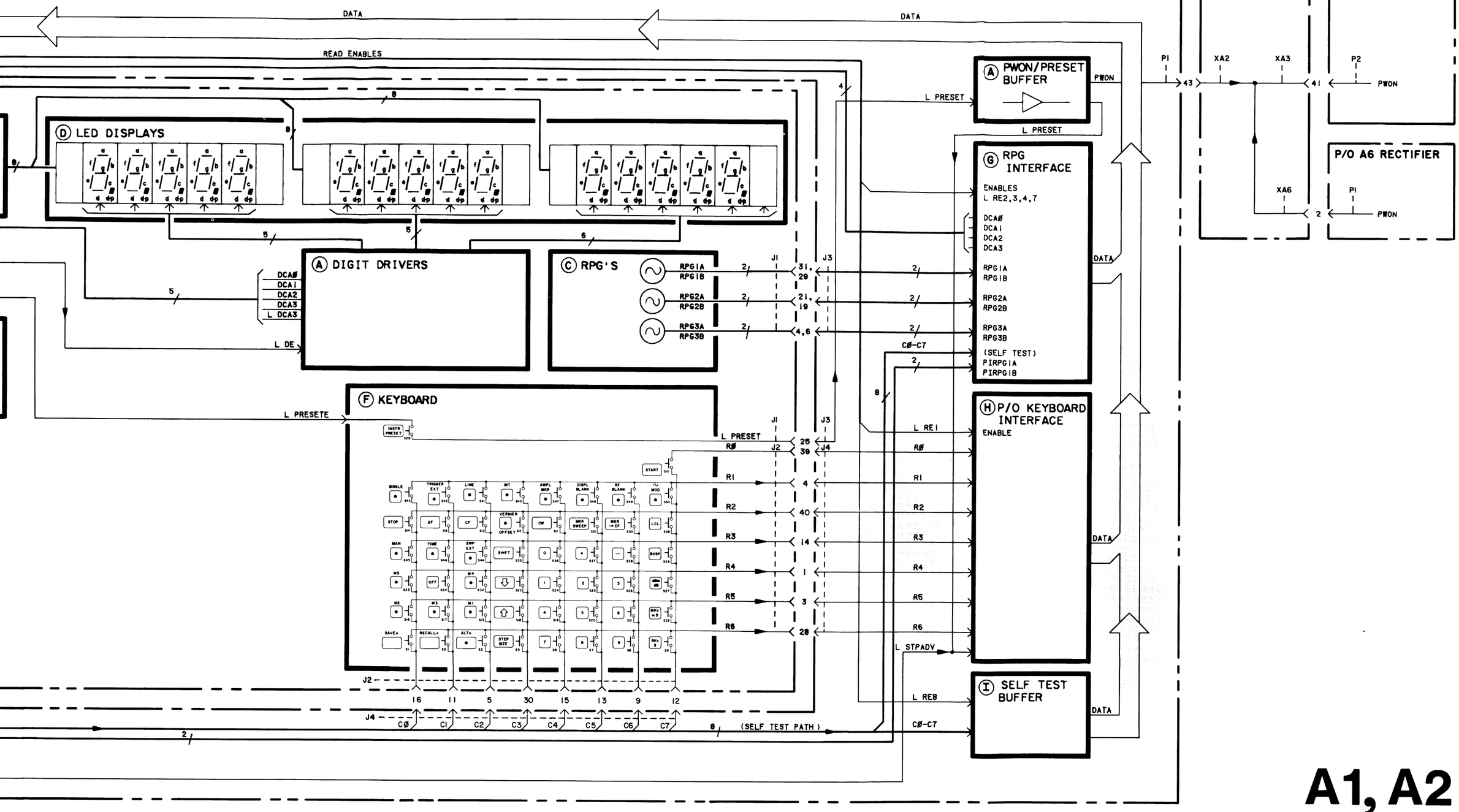
Mnemonic	Address	Data Bit	Description/Explanation
LDS1	1801	2	GHz (Frequency Left)
LDS2	1801	6	MHz
LDS3	1801	4	GHz (Frequency Right)
LDS4	1801	3	MHz
LDS5	1801	5	GHz (Frequency/Time)
LDS6	1801	0	MHz
LDS7	1801	1	sec
(NC)	1801	7	
LDS8	1803	0	ALTn
LDS9	1801	7	VERNIER/OFFSET
LDS10	1805	3	VERNIER/OFFSET #0
LDS11	1802	2	MKR Delta
LDS12	1803	5	START
LDS13	1803	3	CW
LDS14	1803	6	CF
LDS15	1803	2	Delta F
LDS16	1804	4	STOP
LDS17	1802	1	M1
LDS18	1802	0	M2
LDS19	1802	6	M3
LDS20	1802	4	REM
LDS21	1803	1	ADRS'D
LDS22	1805	4	MARKER SWEEP
LDS23	1804	6	M4
LDS24	1804	5	M5
LDS25	1803	4	Shift
LDS26	**	#	SWP
LDS27	1804	3	INT (Sweep Trig)
LDS28	1804	2	LINE (Sweep Trig)
LDS29	1804	1	EXT (Sweep Trig)
LDS30	1804	0	SINGLE (Sweep Trig)
LDS31	1804	7	EXT (Sweep)
LDS32	1802	3	MAN (Sweep)
LDS33	1802	5	TIME (Sweep)
LDS34	1805	2	AMPTD MKR
LDS35	1803	7	DISPL BLANK
LDS36	1805	0	RF BLANK
LDS37	1805	1	Square-Wave MOD

A2 FRONT PANEL INTERFACE

P/O A5 SWEEP GENERATOR

P/O H KEYBOARD INTERFACE

A1 FRONT PANEL



A1, A2

Figure 8-17. A1 Front Panel/A2 Front Panel Interface, Block Diagram

Figure 8-23. A2 Front Panel Interface, Schematic Diagram

A2 FRONT PANEL INTERFACE
08350-60022

PI- 6 (I/O) FPDØ
PI-28 (I/O) FPD1
PI- 7 (I/O) FPD2
PI-29 (I/O) FPD3
PI- 8 (I/O) FPD4
PI-30 (I/O) FPD5
PI- 9 (I/O) FPD6
PI-31 (I/O) FPD7

8 8

DATA BUS

Ⓐ PWON/PRESET BUFFERING

J3-25(IN) LPRESET
PI-43(IN) PWON
TP1 TP2
+5VF +5VF
C3 10
U1B 10K
U2E
+5VF U28C
R1 10K
U28D
L PRESET
LPWON
PWON

Ⓑ ADDRESS DECODING

PI-16(IN) L FPAØ
PI-38(IN) L FPA1
PI-17(IN) L FPA2
PI-13(IN) L FPSTB
PI-37(IN) L FPRD
PI-15(IN) FPE
TP4 TP2 TP3
+5VF
U23
C11 .01
L FPSTB
L FPRD
FPE
X→Y
1800H L RE1
1801H L RE2
1802H L RE3
1803H L RE4
1804H NC
1805H L RE6
1806H L RE7
1807H L RE8
U31
U2F
L FPSTB
L FPRD
L WRITE
FPE
X→Y
1800H L WE1
1801H L WE2
1802H L WE3
1803H L WE4
1804H L WE5
1805H L WE6
1806H NC
1807H L WE8

Ⓓ ANNUNCIATOR INTERFACE

PI-44(IN) LSW
CONTROL AND DRIVE

TP17 PWON 1803H L WE4
U27 C13 .01
U35 (270)
TP21 PWON 1802H L WE3
U25 C12 .01
U33 (270)
TP22 PWON 1801H L WE2
U13
FPDØ FPD1 FPD2 FPD3 FPD4 FPD5 FPD6 FPD7
L DS8 L DS21 L DS15 L DS13 L DS25 L DS12 L DS14 L DS35
L DS18 L DS17 L DS11 L DS32 L DS20 L DS33 L DS19 L DS9
L DS6 L DS7 L DS1 L DS4 L DS3 L DS5 L DS2 NC

TP18 PWON 1805H L WE6
U24
U32 (270)
TP20 PWON 1804H L WE5
U26
U34 (270)
FPDØ FPD1 FPD2 FPD3 FPD4 FPD5 FPD6 FPD7
L DS26 L DS36 L DS37 L DS34 L DS10 L DS22 NC NC
L DS30 L DS29 L DS28 L DS16 L DS24 L DS23 L DS31

J3-27(OUT) L PRESETE

J4-48(OUT) L DS1
J4-50(OUT) L DS2
J4-46(OUT) L DS3
J4-43(OUT) L DS4
J4-45(OUT) L DS5
J4-49(OUT) L DS6
J4-47(OUT) L DS7
J4-7 (OUT) L DS8
J4-41 (OUT) L DS9
J3-15(OUT) L DS10
J4-38(OUT) L DS11
J4-20(OUT) L DS12
J4-22(OUT) L DS13
J4-18 (OUT) L DS14
J4-24(OUT) L DS15
J4-26(OUT) L DS16
J4-37 (OUT) L DS17
J4-44(OUT) L DS18
J4-42 (OUT) L DS19
J4-36(OUT) L DS20
J4-17 (OUT) L DS21
J3-20(OUT) L DS22
J4-32(OUT) L DS23
J4-34(OUT) L DS24
J4-19 (OUT) L DS25
J4-21 (OUT) L DS26
J4-23(OUT) L DS27
J4-25(OUT) L DS28
J4-27(OUT) L DS29
J4-29(OUT) L DS30
J4-31 (OUT) L DS31
J4-33(OUT) L DS32
J4-35(OUT) L DS33
J4-2 (OUT) L DS34
J4-10 (OUT) L DS35
J4-8 (OUT) L DS36
J4-6 (OUT) L DS37

FREQUENCY LEFT
FREQUENCY RIGHT
FREQUENCY/TIME
+5VF
R2 5620
U36B 1000
Q3 Q6
R3 46.4
U36F 1000
Q2 Q5
R5 46.4
U36C 1000
Q1 Q4
R4 46.4
U36A 1000

J3-2(OUT) IS3
J3-1(OUT) IS2
J3-3(OUT) IS1

Ⓕ DISPLAY CONTROL

U21
NC NC NC NC NC
U22
PWON 1807H L WE8
U29 (220)
U30 (680)
FPDØ FPD1 FPD2 FPD3 FPD4 FPD5 FPD6 FPD7

DIGIT COUNTER
LPWON
L DCINCR
U19B
CTR
DCAØ DCA1 DCA2 DCA3
LDCA3
U17C

Ⓔ FRONT PANEL AND RETRACE INTERRUPT CONTROL

PWON
1807H L WE8
1805H L RE6
DSPCLK
C4 .01
U8A
TP7 TP6 TP10
L DCINCR
J3-14(OUT) LDE
U17B U17A
PI-23(OUT) LFPIRQ
U8B TP5 TP4
PI-42(IN) LRTS
U1D 10K
U2A
PI-21(OUT) LRTCIRQ

Ⓒ FP INTERRUPT TIMER

L FPSTB
U20A U20B U19A
CTR
TP3
L DE

CONTROL BUS

Ⓙ SUPPLY FILTERING

L1 L2
+5VA
J3-17,18 +5VR
C14 33
TP15 +5V
C15 100
C16 100
VR2 6.19V
PI-3,4,25,26(IN) +5VA
PI-1,2,5,10,12,14,19, 22,24,27,32,35,36,40 GND DIG
TP19 GND
J3-22,23,24 GND R

SERIAL PREFIX: 2024A

CONTROL BUS

DATA BUS

SEGMENT CONTROL

J3-33(IN) +5VF SENSE

J3-5 (OUT) Ca
J3-32 (OUT) Cb
J3-10 (OUT) Cc
J3-7 (OUT) Cd
J3-30 (OUT) Ce
J3-8 (OUT) Cf
J3-34 (OUT) Cg
J3-28 (OUT) Cdp

J3-9(OUT) DCAØ
J3-12(OUT) DCA1
J3-16(OUT) DCA2
J3-26(OUT) DCA3
J3-13(OUT) LDCA3

RF PLUG-IN RPG

PI-41(IN) PIRPGA
PI-20(IN) PIRPGB

Ⓖ RPG INTERFACE

BUFFERING

U18 680 +5VF

C23 .01 C22 .01 C20 .01 C21 .01 C18 .01 C19 .01

TEST SWITCHES

J3-31(IN) RPG1A
J3-29(IN) RPG1B
J3-21(IN) RPG2A
J3-19(IN) RPG2B
J3-4 (IN) RPG3A
J3-6 (IN) RPG3B

U9 S1

U1C 10K U1A 10K U2B,C

C2 1000pF C1 1000pF

S2 CØ C1 C2 C3 C4 C5 C6 C7

TP8 1806H L RE7 U17D RE7

U5A U5B U6A U6B

LRE3 1802H LRE4

TP11 U11 TP16 U12

FPDØ FPD1 FPD2 FPD3 FPD4 FPD5 FPD6 FPD7

COUNT ACCUMULATION AND SENSING
SIGN SENSING

U4B U4A U3B U3A

TP9 L RE2 1801H U10

DCAØ DCA1 DCA2 DCA3

Ⓗ KEYBOARD INTERFACE

TP23 1806H L RE1

L PRESET TP24 U14 (10K)

PI-33(IN) L STPADV VR1 5.11V

U15 C17 .1 C7 .01

J4-39 (IN) RØ
J4-4 (IN) R1
J4-40 (IN) R2
J4-14 (IN) R3
J4-1 (IN) R4
J4-3 (IN) R5
J4-28 (IN) R6

ROW SENSING

TP25 1800H L WE1 PWON U16

FF

J4-16 (OUT) CØ
J4-11 (OUT) C1
J4-5 (OUT) C2
J4-30 (OUT) C3
J4-15 (OUT) C4
J4-13 (OUT) C5
J4-9 (OUT) C6
J4-12 (OUT) C7

COLUMN STROBING

Ⓘ SELF-TEST BUFFER

TP26 U7 1807H L RE8

RPG INTERFACE TESTING ONLY

SELF TEST ONLY

Figure 8-23. A2 Front Panel Interface, Schematic Diagram

A3 MICROPROCESSOR, CIRCUIT DESCRIPTION

The circuits on the A3 Microprocessor assembly form a microprocessor-based machine that controls the internal operation of the 8350A and RF plug-in installed. A block diagram of A3 is shown in Figure 8-29. Control of the 8350A is implemented over two separate bus systems — the Front Panel Bus and Instrument Bus. Each bus consists of the following logic lines.

- Control Lines – Control direction and timing of data transfer and provide status information.
- Address Lines – Designates device or memory location of data transfer to/from microprocessor.
- Data Lines – Bi-directional logic lines used for communicating between the microprocessor and memory or input/output devices.

The Microprocessor uses the Front Panel Bus to read information from the front panel keyboard and Rotary Pulse Generators (RPGs), and write information to the front panel displays and annunciators. The Instrument Bus is used for communicating with the A4 Scaling and Marker, A5 Sweep Generator, A8 HP-IB Interface, and the RF Plug-in.

The Clock Generation circuit provides the two-phase clock for the microprocessor and other timing signals for the remaining circuits on the A3 assembly.

The microprocessor executes a 32K byte program stored in ROM (Read Only Memory). Three types of instructions are implemented.

- Read Data – Transfer data from ROM, RAM, or input device to internal registers in microprocessor.
- Write Data – Transfer data from internal registers to a specific location in RAM or an output device.
- Process Data – Perform arithmetic or logic operations on data loaded in internal registers.

The microprocessor address lines determine the source/destination of microprocessor data. The Address Decoder circuit decodes the high level bits of the address lines into control lines used to enable data transfers between the microprocessor and specific blocks of memory or other sections of the instrument.

The Front Panel Bus Buffer circuit provides the interface between the microprocessor and the A2 Front Panel Interface. The Instrument Bus Buffer circuit provides the interface between the microprocessor and the rest of the instrument.

Figure 8-24 is a flow chart of the program executed by the microprocessor. When the 8350A is "powered on", or the INSTR PRESET key is pressed, the self test routine is executed. After completing this routine, the microprocessor enters an "idle" loop. The microprocessor continues in the idle loop until there is an interrupt or a status change in the front panel. The cause of an interrupt request can be the HP-IB Interface, RF Plug-in, sweep retrace, or Front Panel timed interrupt. When the microprocessor is interrupted, it completes the present instruction before jumping to the interrupt service routine. During this routine, the microprocessor reads the Status Buffer to determine the source of the interrupt. The microprocessor

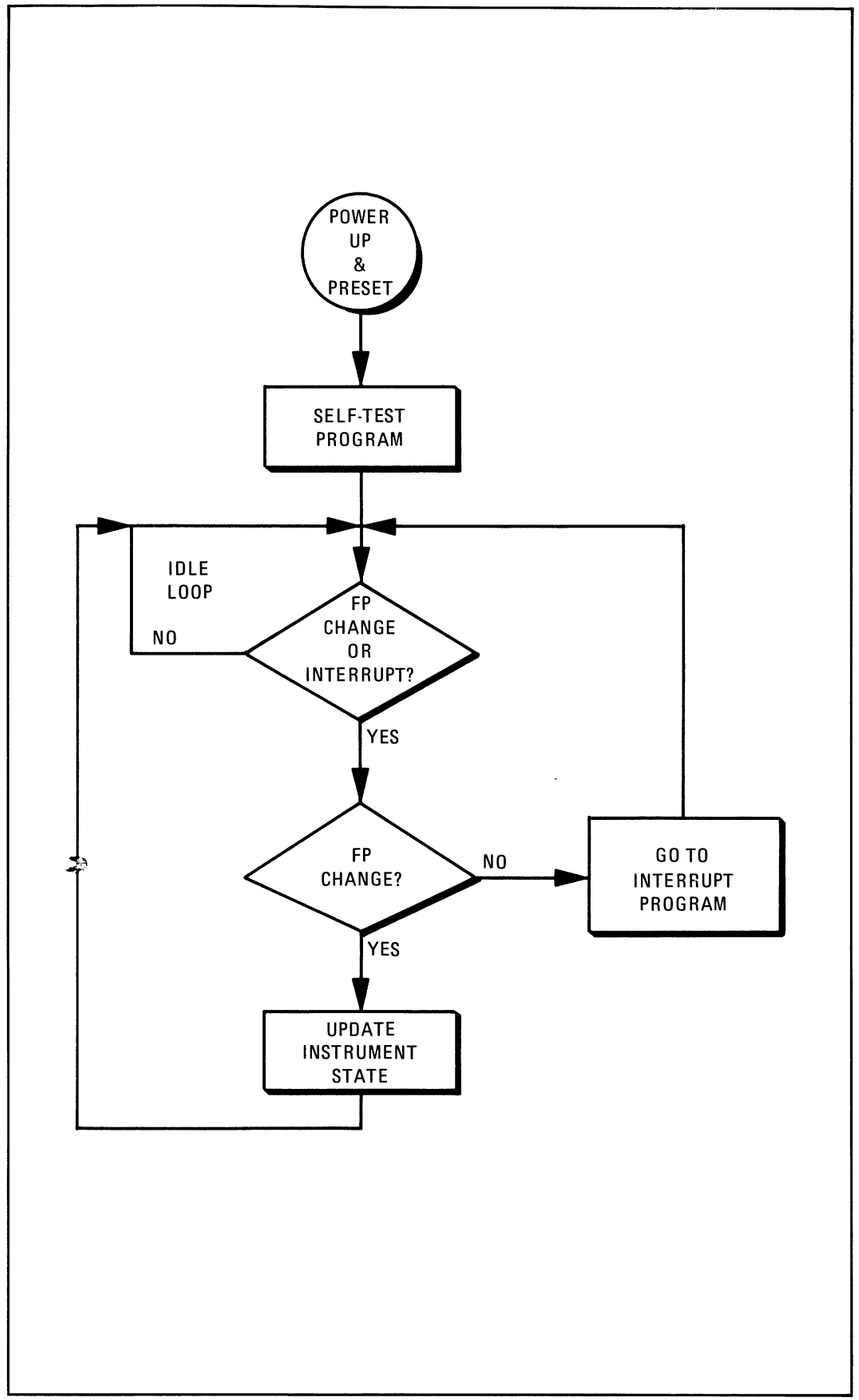


Figure 8-24. 8350A Simplified Program Routine (1 of 2)

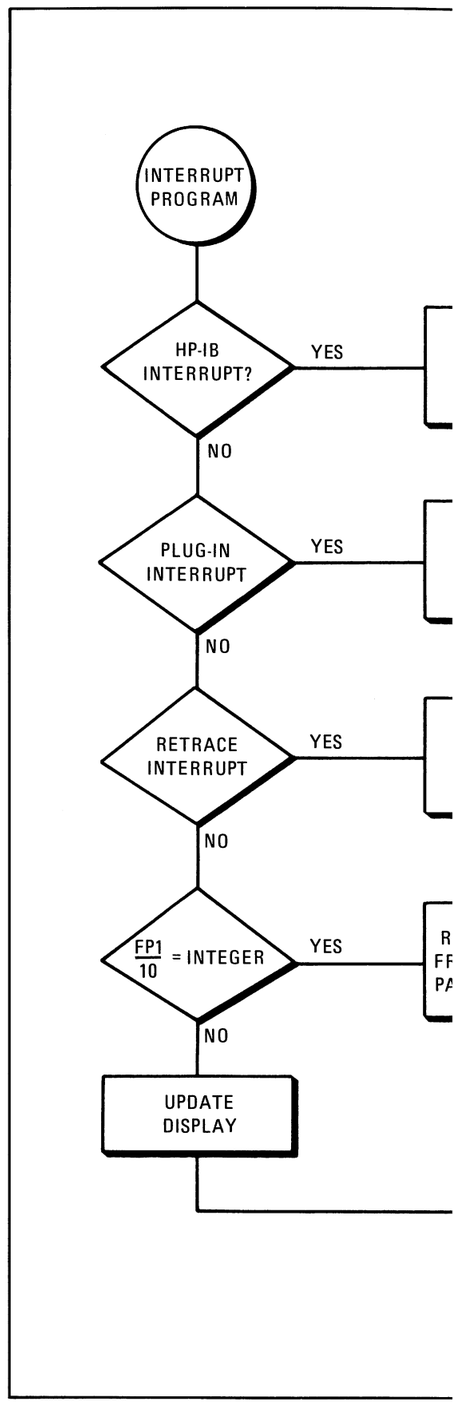


Figure 8-24. 8350A Simplified

RCUIT DESCRIPTION

cessor assembly form a microprocessor-based operation of the 8350A and RF plug-in installed. wn in Figure 8-29. Control of the 8350A is s systems — the Front Panel Bus and Instrument owing logic lines.

ection and timing of data transfer and provide

s device or memory location of data transfer

logic lines used for communicating between the or input/output devices.

nt Panel Bus to read information from the front Generators (RPGs), and write information to the ators. The Instrument Bus is used for communi- arker, A5 Sweep Generator, A8 HP-IB Interface,

vides the two-phase clock for the microprocessor remaining circuits on the A3 assembly.

2K byte program stored in ROM (Read Only ions are implemented.

from ROM, RAM, or input device to internal

from internal registers to a specific location in

thmetic or logic operations on data loaded in

es determine the source/destination of micro- coder circuit decodes the high level bits of the used to enable data transfers between the s of memory or other sections of the instrument.

cuit provides the interface between the micro- el Interface. The Instrument Bus Buffer circuit e microprocessor and the rest of the instrument.

program executed by the microprocessor. When e INSTR PRESET key is pressed, the self test ting this routine, the microprocessor enters an ntinues in the idle loop until there is an interrupt nel. The cause of an interrupt request can be the ep retrace, or Front Panel timed interrupt. When d, it completes the present instruction before outine. During this routine, the microprocessor e the source of the interrupt. The microprocessor

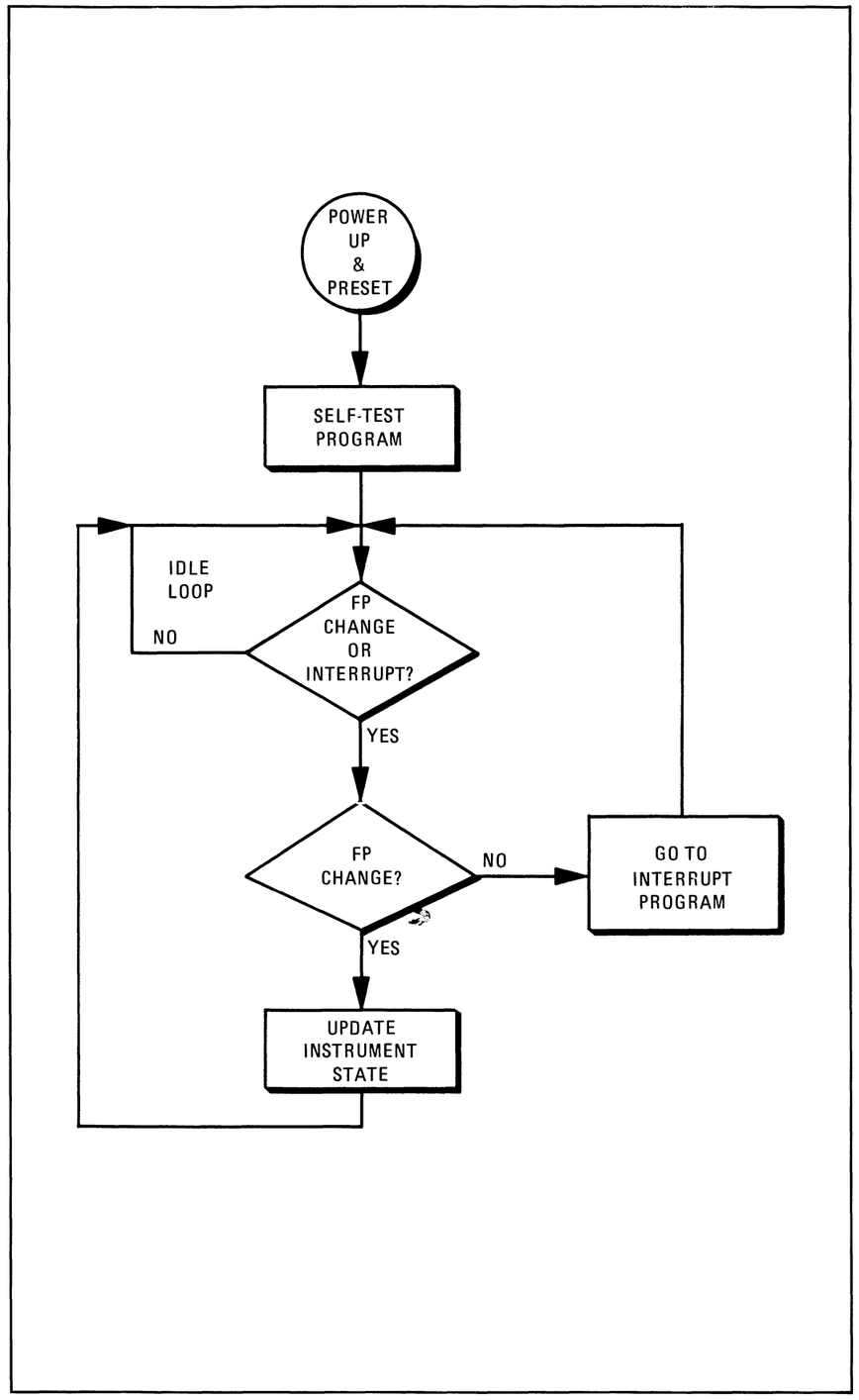


Figure 8-24. 8350A Simplified Program Routine (1 of 2)

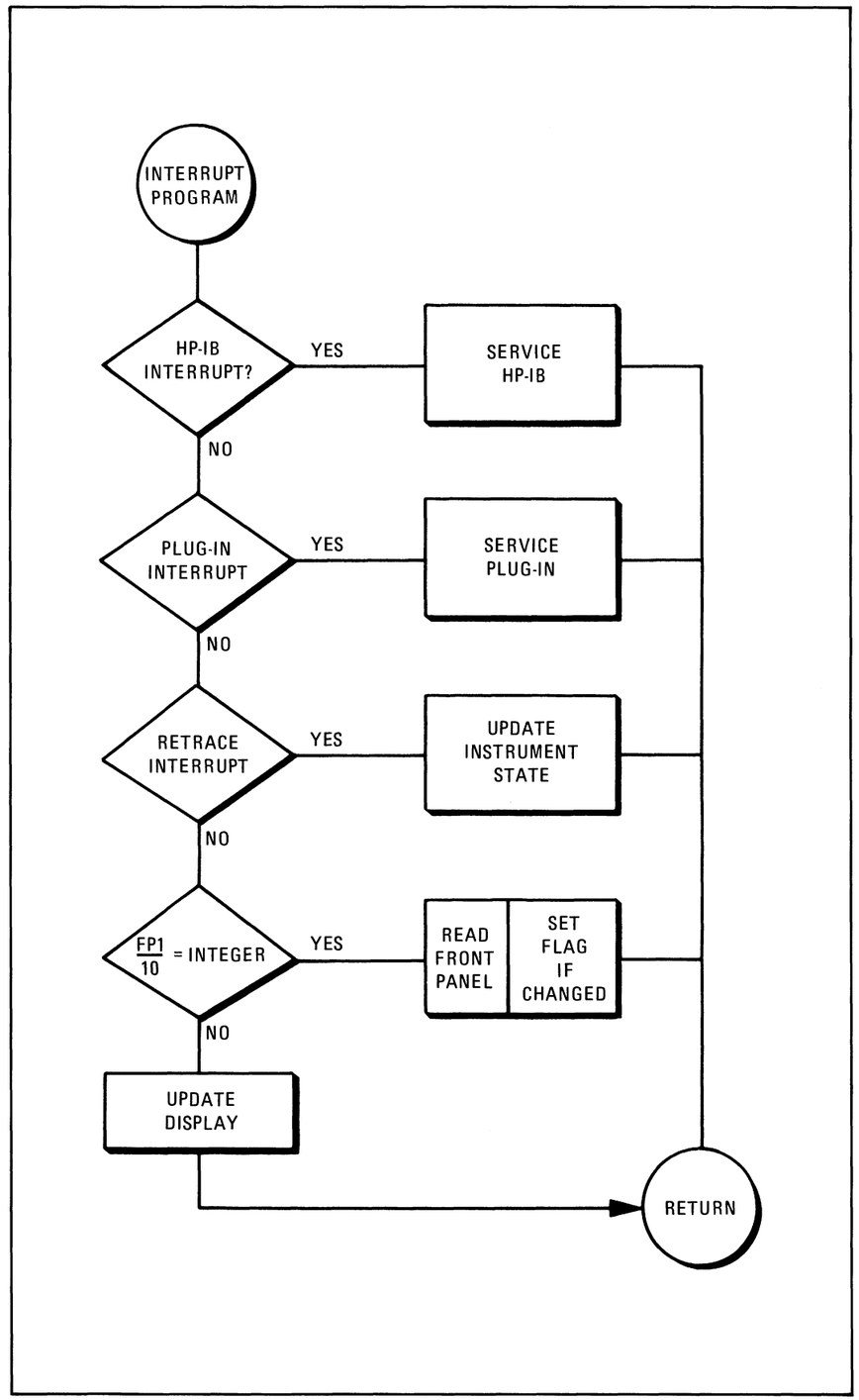


Figure 8-24. 8350A Simplified Program Routine (2 of 2)

then jumps to a service routine to communicate with the interrupting device.

Clock Generation Ⓐ

The Clock Generation circuit produces four timing signals for use on the A3 Microprocessor assembly. Phase 1 (Ø1) and Phase 2 (Ø2)outputs are a two-phase clock signal for microprocessor U5. The I/O Strobe (IOS) output is used for timing of most I/O (Input/Output) operations. The Address Valid Strobe (AVS) indicates when the microprocessor address lines are valid for decoding. Figure 8-27 (see A3 schematic) shows the timing relationship of these signals and their relationship to activity on the microprocessor address and data lines (data bus activity is shown for both a read and write operation).

Clock Oscillator. Crystal Y1 and logic gates U21A, U21C, and U21D form a crystal oscillator with two feedback loops. The basic oscillator is comprised of U21C, Y1, and RC phase shifters R1/C5 and R2/C6. This circuit oscillates at approximately the crystal resonant frequency of 10.7 MHz. At the oscillation frequency, the two RC phase shifters provide enough phase shift to ensure a total loop phase shift of about 360 degrees. Logic gates U21A and U21D provide bias, and stabilization. Logic gate U21B inverts and buffers the oscillator output to the Clock Generator circuit.

Clock Generator. Latch U16 and 32-by-8 PROM U12 form a small state machine that generates the four main timing signals. The clock oscillator output provides the time base for the state machine operation. Thirteen consecutive address locations of U12 contain data that define the state of the four timing signals over thirteen clock oscillator cycles. For each address, the lower four bits of data are the logic state of the PROM Ø1, PROM Ø2, IOS, and AVS signals. The four higher data bits address the PROM for the next clock oscillator cycle. U16 latches and buffers the U12 outputs during each clock oscillator cycle.

Clock Drivers. Clock drivers Q1/Q3 and Q2/Q4 invert and buffer the PROM Ø1 and PROM Ø2 to provide the microprocessor U5 with its two-phase clock signals (Ø1 and Ø2).The drivers are identical, so only the circuit for Ø1 is explained. If the PROM Ø1 input is a logic low, Q1 is on and Q3 is turned off; this causes a high Ø1 output (nominally +5V). When PROM Ø1 changes state to a logic high, Q1 is turned off and Q3 is turned on; this causes Ø1 to go low (nominally 0.2V). RC combinations R3/C10 and R54/C37 at the base of Q1 and Q3 ensure fast desaturation of the transistor base-emitter junction when the transistor is turned off. Without this RC combination, the switching speed of each transistor would be much slower.

Microprocessor Ⓓ

The Microprocessor circuit executes the program stored in ROM to control the 8350A and RF Plug-in. Microprocessor U5 is the main element in this circuit, which utilizes the following signals to execute the program stored in ROM.

- Address Lines (A0—A15) — The microprocessor outputs sixteen address lines that specify an address location, between hexidecimal 0000 and FFFF, for the source or destination of any data transfer. Unless instructed to do otherwise, the microprocessor automatically increments the address location after each read or write operation.

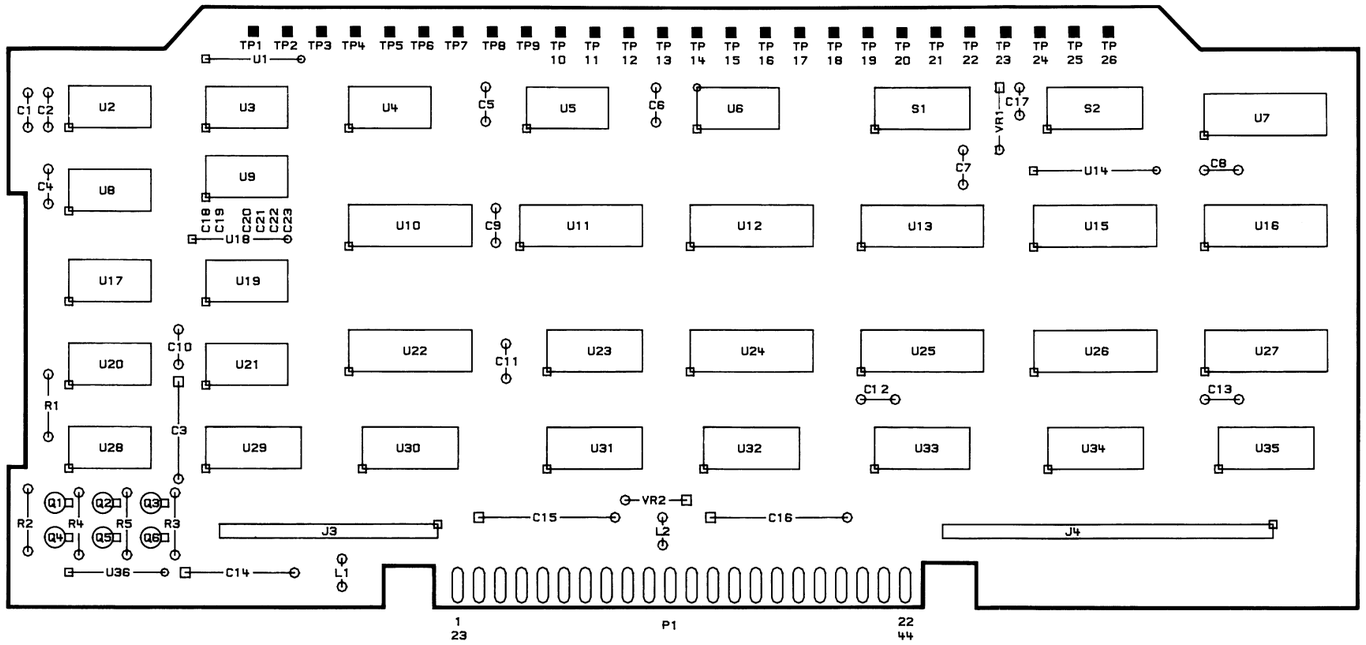


Figure 8-18. A2 Front Panel Interface, Component Locations

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

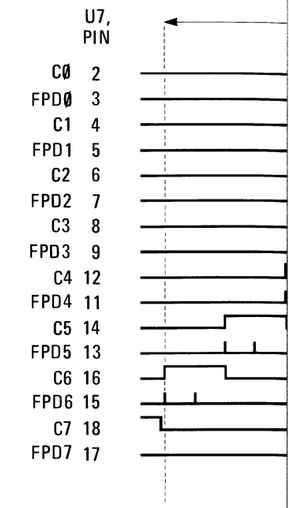
*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◄ ► TO STEP TO THE NEW ADDRESS.

2. ALL WAVEFORM LEVELS ARE TTL: HIGH = 4.5V; LOW = 0V.

3. DURING SHIFT 0 8 , FRONT PANEL SELF-TEST, CONTROL LINES LRE1–8 & LWEI–8 ARE RAPIDLY PULSED WITHIN THE TIME FRAME INDICATED BY THE SHADED PATTERN IN FIGURE 8-19 . NOTE THE DIFFERENCE IN TIME SCALES BETWEEN ACTIVE CONTROL LINES AND COLUMN STROBING. CONTROL LINE PULSE DURATION IS APPROXIMATELY .07 μSEC.

A2P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1	GND DIG	IN		J
23	LFPIRQ	OUT	A3P1-1	E
2	GND DIG	IN		J
24	GND DIG	IN		J
3	+5VA	IN	A7P1-2, 24	J
25	+5VA	IN	A7P1-2, 24	J
4	+5VA	IN	A7P1-2, 24	J
26	+5VA	IN	A7P1-2, 24	J
5	GND DIG	IN		J
27	GND DIG	IN		J
6	FPD0	I/O	A3P1-6	
28	FPD1	I/O	A3P1-7	
7	FPD2	I/O	A3P1-8	
29	FPD3	I/O	A3P1-9	
8	FPD4	I/O	A3P1-10	
30	FPD5	I/O	A3P1-11	
9	FPD6	I/O	A3P1-12	
31	FPD7	I/O	A3P1-13	
10	GND DIG	IN		J
30	DNG DIG	IN		J
11				
33	LSTPADV	IN	J13-22	H
12	GND DIG	IN		J
34				
13	LFPSTB	IN	A3P2-1	B
35	GND DIG	IN		J
14	GND DIG	IN		J
36	GND DIG	IN		J
15	FPE	IN	A3P2-3	B
37	LFPRD	IN	A3P2-25	B
16	LFPA0	IN	A3P2-4	B
38	LFPA1	IN	A3P2-26	B
17	LFPA2	IN	A3P2-5	B
39	LFPA3			NOT USED
18	LFPA4			NOT USED
40	GND DIG	IN		J
19	GND DIG	IN		J
41	PIRPGA	IN	J2-60	G
20	PIRPGB	IN	J2-61	G
42	LRTS	IN	A5P2-18, 19	E
21	LRTCIRQ	OUT	A3P2-8	E
43	PWON	IN	A6P1-2	A
22	GND DIG	IN		J
44	LSW	IN	A5P2-28	D



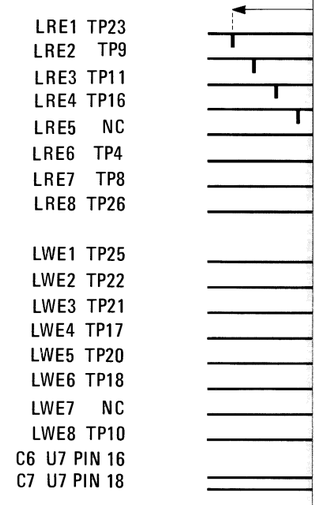
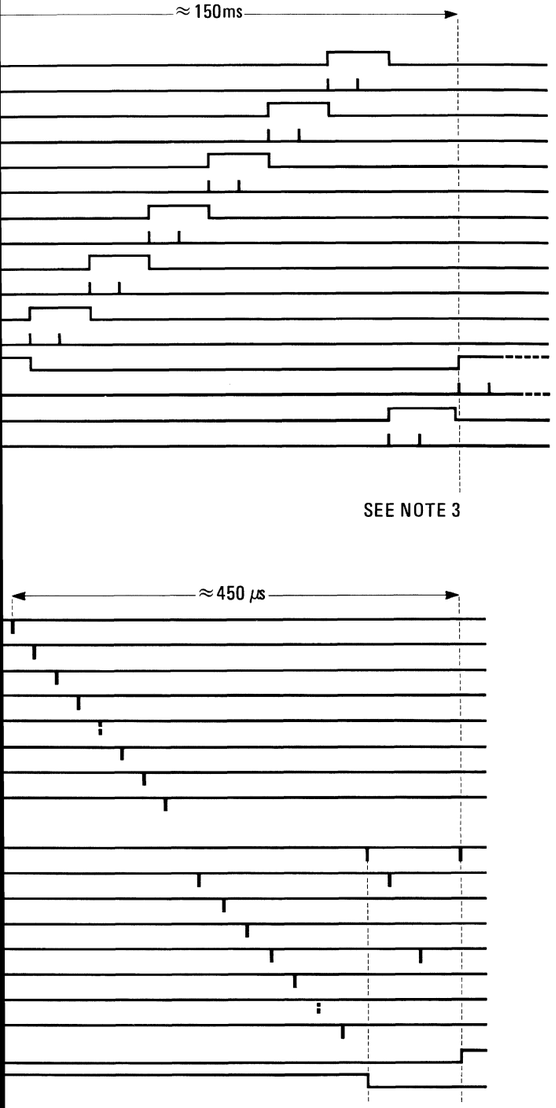


Figure 8-1

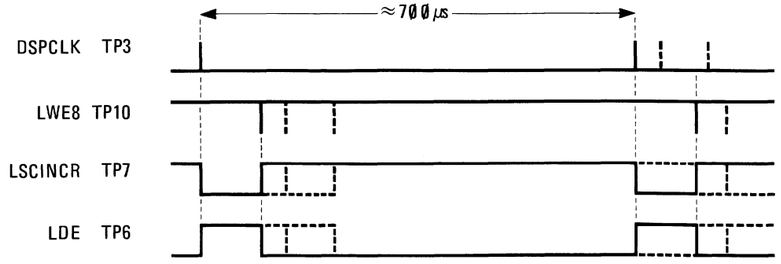
COLUMN STROBING TIM.



TO ACCESS TEST PATTERN:

1. ENTER SHIFT 0 8
2. EXTERNAL TRIGGER AT TP23

Figure 8-19. Front Panel Self Test Timing Diagrams



LENGTH OF INTERRUPT VARIES FROM 100µs TO 220µs.

—— INDICATES MOST PREVALENT TRACE.

---- INDICATES UNSTABLE TRACE PATTERN.

Figure 8-20. Front Panel Interrupt Timing Diagram

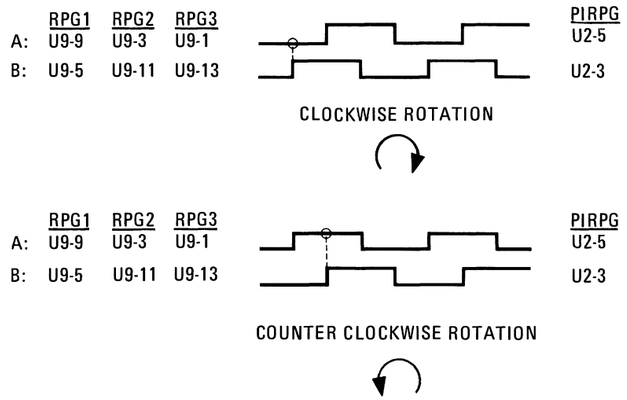
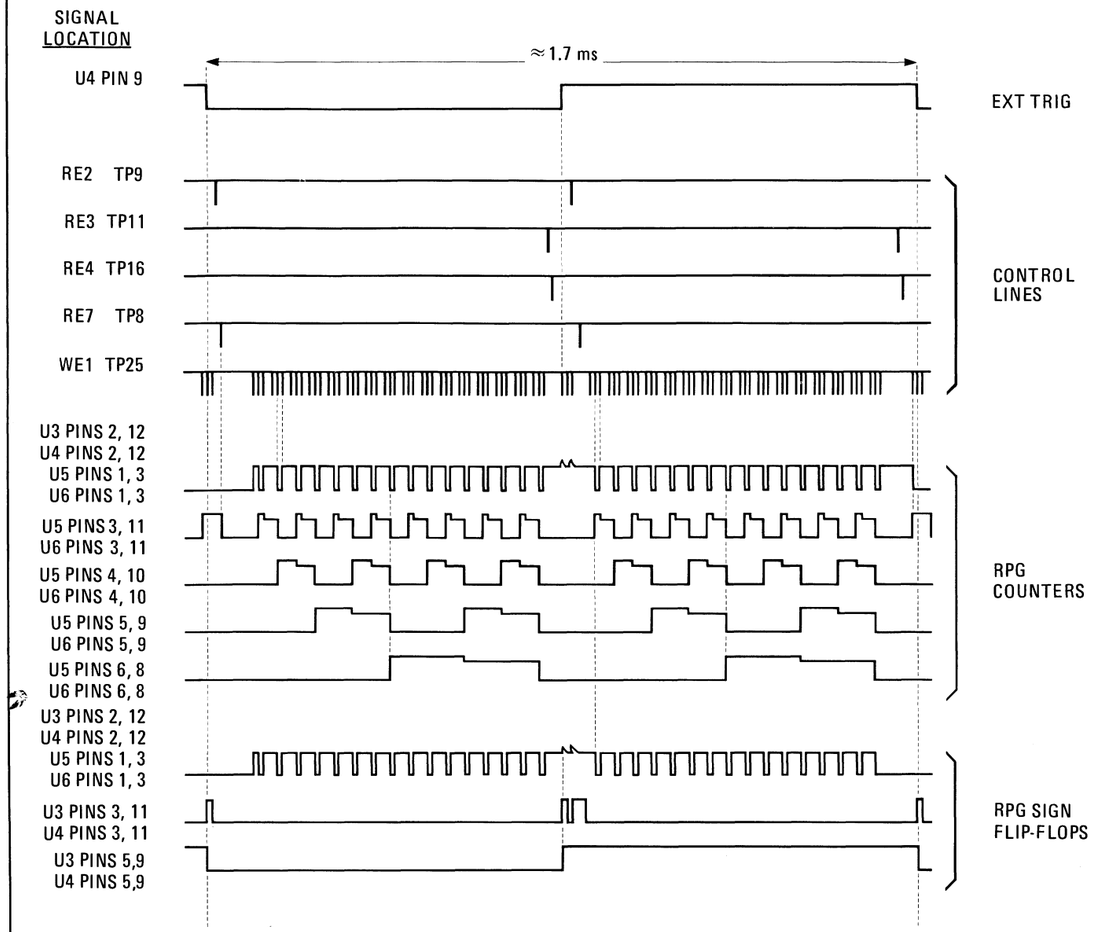


Figure 8-21. RPG Pulse Train



(REFER TO A1/A2 TROUBLESHOOTING FOR RPG SELF-TEST DESCRIPTION.)

Figure 8-22. RPG Interface Timing Diagram

- Data Lines (D0–D7) – The eight data lines are bi-directional and are used by the microprocessor to communicate with the address location specified by the address bus.

- L WRITE Line – The microprocessor L WRITE (Low=Write) output controls the direction of the data transfer on the data bus. A logic high, read, indicates a data transfer from the addressed device to the microprocessor. A logic low, write, indicates a data transfer from the microprocessor to the addressed device.

- VMA – The VMA (Valid Memory Address) output indicates when the Address Bus has a stable and valid address for a data transfer.

Address lines A0–A9, all data lines, and the L WRITE line all use pull-up resistors (U6, U13, and R21) to limit their high logic levels to +3.6Vdc. This ensures that when the nonvolatile memory option (Option 001) is installed, the logic levels on these lines do not exceed the supply voltage of the CMOS RAM.

A low PWON input at TP23 resets microprocessor U5 at initial "power on" or whenever the front panel INSTR PRESET key is pressed. An active low L RES (Low=Reset) input to microprocessor U5, resets the microprocessor, which initializes program execution at address FFFE. (The address of the first program instruction is stored at addresses FFFE and FFFF.) The PWON (Power On) input from the A6 Rectifier is shaped and buffered by Schmitt trigger logic gates U4B and U4A to provide fast rise and fall time of the L RES microprocessor input. RC combination R14/C30 causes a delay in transition of PWON of approximately 3 clock cycles. This keeps the microprocessor reset until all the digital circuits have sufficient power.

The AVS (Address Valid Strobe) from the Clock Generation circuit functions as a Data Bus Enable (DBE) input to microprocessor U5. This line must be a logic high to enable the microprocessor to read or write data. The microprocessor has two interrupt inputs, LNMI (Low=Non-Maskable Interrupt) and LIRQ (Low=Interrupt Request). The difference between the two signals is that LIRQ is ignored (masked) by the microprocessor if an internal flag is cleared, but an active low LNMI always requires a response. When either interrupt input is active low, the microprocessor completes the instruction it is executing then immediately jumps to the Interrupt Service Routine stored in ROM.

A "Free Run Test" of the microprocessor can be performed by setting all eight sections of S1 open and grounding TP9, LDSA (Low= Digital Signature Analysis). This "Free Run Test" isolates the microprocessor from the data bus and forces a CLR B (Clear B Accumulator) instruction into the microprocessor. The result is that the microprocessor increments through its entire address field, generating signatures at various nodes of the A3 Assembly. Refer to Microprocessor Troubleshooting for more detailed information on the "Free Run Test".

Address Decoder (E)

The Address Decoder decodes the high level address bits (A10–A15) into control lines that enable data transfers between the microprocessor and specific blocks of memory or other sections of the instrument. Each section that communicates with the microprocessor is given a specific block of address space. Table 8-19 lists the address space allocation for the system.

Table 8-19. Microprocessor Address Space Allocation

Address Space (Hex)	Amount of Space	Device	Control Line
0000-03FF	1K	RAM	L RAME1 (Low = RAM Enable 1)
0400-07FF	1K	RAM	L RAME2 (Low = RAM Enable 2)
0800-0FFF		Self Test Counter	L EAC (Low = Error Accum. Clock)
1000-17FF	2K	Status Buffer	L SBE (Low = Status Buffer Enable)
1800-IFFF	2K	Front Panel Interface	L FPE (Low = Front Panel Enable)
2000-27FF*	2K	A5 Sweep Gen/ A8 HP-IB	L I/OE1 (Low = I/O Enable 1)
2800-2FFF*	2K	RF Plug-in	L I/OE2 (Low = I/O Enable 2)
3000-37FF*	2K	A4 Scaling and Marker	L I/OE3 (Low = I/O Enable 3)
3800-3FFF	2K	Self Test Counter	L EAR (Low = Error Accum. Reset)
4000-5FFF*	8K	RF Plug-in ROM	L PIROME (Low = Plug-in ROM Enable
6000-7FFF**	8K	ROM	L ROM5 (Low = ROM 5)
8000-9FFF**	8K	ROM	L ROM4 (Low = ROM 4)
A000-BFFF**	8K	ROM	L ROM3 (Low = ROM3)
C000-FFFF**	16K	ROM	L ROM1,2 (Low = ROM 1,2)

* In each of these cases the L IBE (Low = Instrument Buffer Enable) control line is also true, enabling the address and data buffers of the instrument bus buffer to be active.

** Of the 40K of address space reserved here only 32K is used.

Most of the control line outputs listed in Table 8-19 are generated directly by 3-to-8 decoders U23 and U24. However, additional decoding is provided to generate the following control lines.

- L RAME1 and L RAME2 are both developed from the L RAM output of U23 pin 15, and further decoding of the A10 address line (L A10 is used to generate L RAME2). Both signals are gated with IOS (Input Output Strobe) and PWON (Power On) control lines through NAND gates U19A and U19B. Because both RAM enable lines are gated with IOS, they are only allowed to be active during a data transfer. Gating with the PWON control line prevents random data from being written into RAM when the line power is turned off on Option 001 instruments (Nonvolatile memory).

- L ROM1,2 is developed through decoding of L ROM2 (U24 pin 9) and L ROM 1 (U24 pin 7) control lines with NAND gate U3C and inverter U18B. If either of these lines is active low, L ROM1,2 goes active low. The L ROM1 and L ROM2 control lines are used for addressing EPROM on the A3A1 PROM board. If A3A1 is not installed (replaced with masked ROMs U9–11 and U35) the L ROM1 and L ROM2 lines are not used.

When AVS (Address Valid Strobe) and VMA (Valid Memory Address) are active high, U24 is enabled to decode address lines A13 through A15 and enable address space in 8K blocks. U23 is is enabled when AVS and VMA are active high and both A14 and A15 are low (first 16K of address space). U23 decodes address lines A11 through A13 to enable address space in 2K blocks.

Two other control lines generated by the Address decoder are L IBE (Low=Instrument Buffer Enable) and II/OS (Instrument Input/Output Strobe). L IBE is active low whenever the microprocessor communicates on the Instrument Bus (Addresses 2000H through 5FFFH), and enables the address and data buffers in the Instrument Bus Buffer. The II/OS control line is a gated I/OS signal that is used to strobe data onto the Instrument Bus.

When the microprocessor Free Run test is run, TP12 is grounded to disable the Address Decoder circuit (see A3 Troubleshooting at the end of this circuit description). The L A10 address line at TP11 is also useful for troubleshooting, and can be used to provide a pulsed source for checking shorted data or control lines.

ROMS (F)

If the A3A1 PROM assembly is not installed, ROMs U9, U10, U11, and U35 store the 32K by 8 bits of program data that is executed by the microprocessor to control the rest of the 8350A and the RF Plug-in installed. Each ROM stores 8K bytes of program,and has a unique ROM enable line that enables the ROM over an 8K block address space.

L ROM1,2 – Enables ROM U9 for address locations C000 through FFFF.

L ROM3 – Enables ROM U11 for address locations A000 through BFFF.

L ROM4 – Enables ROM U35 for address locations 8000 through 9FFF.

L ROM5 – Enables ROM U10 for address locations 6000 through 7FFF.

RAMs (H)

Data that is generated and/or processed during program execution is stored in RAM (Random Access Memory) (U14, U15, U7, and U8). Examples of the types of data stored in RAM are the present state of the front panel, the data associated with the nine SAVEn/RECALLn front panel settings, the data used to control the rest of the 8350A, the HP-IB address, the RF Plug-in code, etc.

The total RAM storage capacity is 2K by 8 bits. Since each RAM can store 1K by 4 bits, two RAMs are combined to form a 1K by 8 bit memory space. The two pair of RAMs combine to form a 2K by 8 bit memory space. One RAM in each pair (U7 and U14) store the low order four bits (D0–D3) of the data bus, and the high order bits (D4–D7) are stored by the other RAM in each pair (U8 and U15). U14 and U15 store the first 1K of data, and are enabled when control line L RAME1 (Low= RAM Enable 1) is active low. L RAME1 is active low for address locations 0000 to 03FF.

U7 and U8 store the second 1K bytes of data and are enabled when control line L RAME2 is active low. L RAME2 is active low for address locations 0400 to 07FF.

The logic level of the L WRITE signal for each RAM determines if data is written to the RAM or the data stored is read by the microprocessor. When L WRITE is active low, the microprocessor writes data into the addressed RAM location. When L WRITE is active high, the microprocessor reads data from the addressed RAM location.

All four RAM power supply connections are to V_{CCP} which is the battery backup supply for option 001 instruments.

Front Panel Bus Buffer (J)

The Front Panel Bus Buffer circuit provides the interface for the address, data, and control lines between the microprocessor and the Front Panel Bus. The Front Panel Bus is used to transfer data between Front Panel circuits and the A3 Microprocessor Assembly. Bi-directional buffer U22 is a 3-state device that provides the interface for the eight front panel data lines (FPD0—FPD7). Transfer of data through U22 is enabled when control line L FPE (Low=Front Panel Enable) is active low. L FPE is active low for microprocessor addresses 1800 through 1FFF. Direction of data flow is determined by the logic state of the microprocessor L WRITE signal. This signal is high when reading data from the front panel and is low when writing data to the front panel. 3-state buffer U32 drives the five address lines (FPA0—FPA4), and three control lines (FPE, L FPRD, and L FPSTB) associated with the Front Panel Bus. U32 is always enabled. The front panel uses the address lines to select the source/destination of information on the data lines. The control lines manage the data flow. A more detailed functional description of these lines is provided in the A2 Front Panel Interface circuit description.

Interrupt Logic and Status Buffer (B)

The Interrupt Logic and Status Buffer circuit performs the following functions:

- Multiplex the following interrupt request signals onto the microprocessor maskable interrupt request control input, L IRQ (Low = Interrupt Request).
  - L PIIRQ (Low = Plug-in Interrupt Request)
  - L IBIRQ (Low = HP-IB Interrupt Request)
  - L FPIRQ (Low = Front Panel Interrupt Request) L FPIRQ also goes active low when there is a L RTCIRQ (Low = Retrace Interrupt Request). So, there is no need to multiplex L RTCIRQ to develop a L IRQ input to the microprocessor.
- Buffer the L PINMI (Low = Plug-in Nonmaskable Interrupt) signal onto the microprocessor nonmaskable interrupt control input, L NMI (Low = Non-maskable Interrupt).
- When addressed by the microprocessor, interface the following control lines onto the microprocessor data bus.

- Interrupt Requests: L RTCIRQ (Low=Retrace Interrupt Request), L PIIRQ (Low=Plug–in Interrupt Request), and L IBIRQ (Low=HP-IB Interrupt Request)
- Flags: L PIFLG (Low=Plug-in Flag), and L MFLG (Low=Marker Flag)
- Power Supply Status: L PSF (Low=Power Supply Failure), and L PST (Low=Power Supply Overtemperature)
- L TEST (Low=Test): When active (TP20 jumpered to ground), initiates Front Panel Bus self test. Used if keyboard is not operational.

Interrupt Logic. Quad Schmitt Trigger NAND gate U34 multiplexes several interrupt requests onto the microprocessor interrupt request control input (L IRQ). An active low microprocessor interrupt request (L IRQ) is generated any time one of the interrupt request inputs to U34 is active low. If the microprocessor is enabled to accept interrupts, the microprocessor completes the instruction it is executing, then jumps to the Interrupt Service Routine stored in ROM. The interrupt requests may be disabled by grounding TP21, IRQE (High=Interrupt Request Enable). This forces the U34C output (L IRQ) high (not active) regardless of the state of the interrupt requests.

Schmitt trigger NAND gates U4C and U4D shape and buffer the L PINMI (Low=Plug-in Nonmaskable Interrupt) control line onto the microprocessor nonmaskable interrupt control input, L NMI. When L PINMI is active low, L NMI is active low, causing the microprocessor (after the current instruction is executed) to jump to the Interrupt Service Routine stored in ROM. This interrupt can not be masked, so the microprocessor always responds to an active L PINMI. L PINMI can be disabled by grounding TP16, NMIE (Nonmaskable Interrupt Enable). This forces U4D pin 13 low, causing U4D pin 11 high (not active) regardless of the state of L PINMI.

Status Buffer. 3-state buffer U20 buffers and inverts the plug-in and marker flags, power supply status lines, the L TEST control line, and all but one of the interrupt requests onto the microprocessor data bus. The combination of these lines is called the status byte. When active low, the L SBE (Low=Status Buffer Enable) control line from the Address Decoder enables the status byte onto the data bus. L SBE is active low for address locations 1000 through 17FF. The microprocessor periodically reads the status byte during program execution to check the status of the two power supply status control lines, as well as the plug-in and marker flags. If either of the power supply status lines is active low for a certain period, the microprocessor briefly writes an error message to the front panel displays. The marker flag is monitored during the Instrument Preset and operator initiated self tests. The marker flag is active low when the marker circuits on the A4 Marker and Scaling assembly have passed the test routine. The plug-in flag is monitored during the program idle loop, and, when active low, indicates the plug-in requires a low priority of service (i.e. front panel update).

The microprocessor also reads the status byte following an interrupt request. The microprocessor uses the status byte to determine the source of the interrupt request. Note that L FPIRQ is not included in the status byte. If all other interrupt requests are not active, the microprocessor assumes L FPIRQ caused the interrupt request.

The L TEST input is used for front panel troubleshooting and is active low when TP20 is grounded. If L TEST is active low when the microprocessor reads the status byte, the microprocessor jumps to the Front Panel Bus self test. For more details of this test refer to the troubleshooting section for the A2 Front Panel Interface.

Self Test Error Code Indicator Ⓒ

The Self Test Error Code Indicator circuit provides a pass/fail indication for the tests in the Self Test Routine (STR). The STR is initiated by any of the following actions:

- Cycling the ac line power
- Pressing the front panel INSTR PRESET key.
- Programming the Instrument Preset function via HP-IB.

Either of the first two actions cause the PWON (Power On) control line input to go low, which resets microprocessor U5 through U4A and U4B. This results in the microprocessor jumping to and executing the Self Test Routine. The L RES output of U4A is also buffered through NAND gate U3A, and resets the Self Test counter U2A. With all of the U2A outputs low, LEDs DS1 through DS4 are turned on. The indicator LEDs are binary weighted (8−4−2−1) with DS1 being the Most Significant Bit (MSB). An LED that is turned on indicates a logical one (1).

At the beginning of the Self Test Routine, the microprocessor ensures that the Self Test Counter is reset by setting L EAR (Low = Error Accumulator Reset) active low. The Self Test Counter remains reset until either a Self Test fails or all tests pass. If a test fails, the microprocessor executes a set of instructions to increment the Self Test Counter with L EAC (Low = Error Accumulator Clock). The microprocessor then continues execution of the test routine for the failed test. The number of L EAC clock pulses generated is equal to 15 minus the test number. For example, if the Front Panel Bus test (Test number 6) fails, the number of L EAC transitions generated is nine (15 − 6). As a result, the Self Test Counter outputs represent the binary equivalent of nine and the LEDs indicate:

DS1(MSB) = OFF DS2 = ON DS3 = ON DS4(LSB) = OFF

This indication is interpreted as a six (E006). If all tests pass, the Self Test Routine generates fifteen transitions of L EAC, resulting in all of the indicator LEDs being turned off.

The Self Test Routine may also be initiated by programming the Instrument Preset function through HP-IB. Operation of the Self Test circuit is the same with the following exceptions. The microprocessor is "programmed" to reset instead of using the PWON control line, and Self Test Counter U2A is reset only by the L EAR control line.

PROM Board Connector Ⓖ

The PROM Board connector supplies five ROM enable lines (L ROM1 through L ROM5) to the A3A1 PROM board. This connector is not used if masked ROMs are installed on the A3 Microprocessor (U9−U11 and U35).

Supply Filtering Ⓚ

The Supply Filtering circuit filters the supply voltages used by the A3 Microprocessor, and provides a protected +5V supply (V_{CCP}) for RAM. For standard instruments, jumper W1 is connected across the collector-emitter of transistor Q6, and V_{CCP} always tracks the level of the +5VF supply. For Option 001 (Nonvolatile

memory) instruments, jumper W1 is removed, and the circuit operates in one of two states.

- When ac line power is applied to the 8350A (LINE switch in ON position), transistors Q5 through Q7 are all biased on. Thus, V_{CCP} approximately equals +5VF and the Option 001 battery, BT1 (which connects to the circuit at P1−21, +5V BAT), charges through R18.

- When the 8350A ON/OFF switch is in the OFF position, transistors Q5 through Q7 are all turned off, and the source for the V_{CCP} supply is the Option 001 battery, BT1. Thus the RAM is kept active when line power is disconnected.

During the transition between battery-backup and internal power for the RAM, Q5 through Q7 ensure that V_{CCP} does not drop below the battery voltage.

Instrument Bus Buffer (I)

The Instrument Bus Buffer circuit interfaces the microprocessor address, data, and control lines onto the Instrument Bus, which is the main communication bus for the rest of the 8350A (except for the front panel circuits). U25 is a 3-state bi-directional buffer that provides the interface for the eight instrument data lines (ID0−ID7). Transfer of data through U25 is enabled when L IBE (Low=Instrument Bus Enable) is active low (Addresses 2000 through 5FFF). Direction of data flow is determined by the logic state of the microprocessor L WRITE control output (Low=Write, High=Read).

3-state buffers U27 and U29 drive the thirteen address lines (L IA0 through L IA12) and the L IRD (Low=Instrument Bus Read) control line associated with the Instrument Bus. The logic state of the address lines determine the source/destination of the data transfer and the logic state of L IRD determines direction of data flow at the addressed device. U27 and U29 are enabled by the L IBE control line.

3-state buffer U26 drives the remaining control lines associated with the Instrument bus, and is always enabled. Table 8-20 lists these control lines, with definition and function description. All lines associated with the Instrument Bus (except I/OE3) are reverse-terminated by 100 ohm resistors to reduce ringing.

Table 8-20. Instrument Bus Control Signals

Control Line	Definition	Function
L I/OCLK	Low = I/O Clock	Timing Clock for the A8 HP-IB Interface
L I/OSTB	Low = I/O Strobe	Master Data enable pulse for Instrument Bus
I/OE1	I/O Enable 1	Enable line for A5 Sweep Generator and A8 HP-IB Interface
I/OE2	I/O Enable 2	Enable line for RF Plug-in
I/OE3	I/O Enable 3	Enable line for A4 Scaling and Marker
PIROME	Plug-in ROM Enable	Enable line for RF Plug-in ROM

TROUBLESHOOTING

Since the A3 Microprocessor controls all functions in the 8350A, a component failure on this board assembly generally disables the entire instrument. The most likely indications of an A3 Microprocessor component failure are as follows:

- Instrument Preset self test failure (Error codes E015 through E006)
- Front Panel Lock-up (Some or all the front panel lights are on; pushbuttons produce no response.)
- Flashing Lights (Front panel lights flash in a random or periodic fashion; pushbuttons will not function properly, but may have an effect.)
- Partial Failure (The instrument works most of the time, but certain front–panel functions do not work.)

Instrument Preset Self Test

Begin troubleshooting by initiating the Instrument Preset self test, and checking the four LEDs mounted on top of the A3 Microprocessor for an error code. When INSTR PRESET is pressed, or when ac line power is initially turned on, the four LEDs should momentarily turn on; then, either an error code should be displayed, or the four LEDs should turn off (indicating the self test is complete). In addition to indicating which Self-Test failed, the error code provides additional information about the tests that passed. Any section of circuitry exercised by a test before the indicated failure code is very probably functioning properly and can be eliminated from further troubleshooting procedures. Refer to the description of the Self-Tests in the General Troubleshooting section for details.

A list of the error codes for the A3 Microprocessor follows below.

NOTE

In the event of a Front Panel failure, the four Front Panel SWEEP TRIGGER annunciators used to indicate errors, may display an incorrect error code, or none at all. Check the four LEDs on the A3 Microprocessor to be certain of the error code. Press and hold down the Instrument Preset button to light ALL the LEDs and insure that none are burned out. Press Instrument Preset several times to make sure the same error code appears each time.

No LEDs turn on. Self Test not initiated; LEDs do not turn on when INSTR PRESET key is pressed.

Check that the Power Supplies are functioning. Check that TP17 is at +5 Vdc and free of excessive digital noise. Power for the RAMs is supplied by a special circuit (Q5, Q6, and Q7). In instruments with Option 001 (nonvolatile memory), this circuit recharges the battery, and prevents it from discharging through the power supply when the power is off. Check pin 18 of the RAMs (U14, U15, U7, and U8) for slightly under 5 Vdc. Also make sure that pin 1 of U13 or U6 is at approximately 3.6 Vdc.

Next, the Clock Generation block should be checked. The Clock Oscillator output (TP27) should be a 10.7 MHz square wave. The AVS (TP4) and IOS (TP10) lines are driven directly by U16, while the Phase 1 (TP2) and Phase 2 (TP1) lines are buffered by Clock Drivers Q1, Q3, Q2, and Q4. These four clock signals run at approximately 823 kHz, completing one cycle for every thirteen cycles of the 10.7 MHz clock. Typical waveforms can be found on the A3 schematic.

Check the other control lines to the microprocessor. In normal operation, L RES (pin 40), L HALT (pin 2), L NMI (pin 6 or TP8), and VCC (pin 8) should all be at 5.0 Vdc. If L NMI is low, it can be forced back high by grounding TP16. If the microprocessor then functions properly, troubleshoot the interrupt circuitry. In normal operation, L IRQ will show periodic interrupts from the Front Panel at roughly 1370 Hz, plus occasional End-of-Sweep interrupts.

E015 Microprocessor. All of the Error Code LEDs turn on if the microprocessor cannot execute the first (RAM) Self-Test. This can be caused by one or more of several different failures. These include malfunctioning of the microprocessor itself, a failure in ROM1,2 (Addresses C000 to FFFF) containing the Self-Test software or its enable line, or a failure in the Address or Data Busses. In most cases, the Free Run Test must be performed to isolate the failure.

E014, E013, E012, E011 RAM. These codes indicate a failure in RAM according to Table 8-21.

Table 8-21. RAM Error Codes

Error Code	Enable Line	Address (Hexidecimal)	Data Lines	RAM
E014	L RAME1	0400-07FF	D4–D7	U15
E013	L RAME1	0400-07FF	D0–D3	U14
E012	L RAME2	0000-03FF	D4–D7	U8
E011	L RAME2	0000-03FF	D0–D3	U7

The RAM Test checks every bit of every RAM address location for both read and write capability. The microprocessor steps through each location, reads its contents, writes the complement, and reads it back. These two words are then checked to assure that the complement was indeed written into RAM and read back. Finally, the original contents of the locations are restored. If an error occurs, the microprocessor determines if the most significant bits (D4–D7) or least significant bits (D0–D3) caused the error, and displays the appropriate error code. When a RAM failure is detected, the microprocessor jumps immediately to the beginning of the RAM test and starts over.

Error codes E014 through E011 occur if a RAM cell is locked high or low, or if the RAM's write capability is lost. However, this error also occurs if the RAM Control section or L WRITE line are malfunctioning. It is especially important that L RAME1, L RAME2, and the L WRITE be checked for activity, since a failure in the Address Decoder could cause a RAM error code. For example, if the error code indicates a failure in U7 or U8, there should at least be a short pulse in L RAME2 to check the first cell. If there is not, the problem is probably not in the RAM at all, but in the Address Decoder. The Free Run Test can be employed to check the Address Decoder outputs appropriate to RAM.

Also bear in mind that RAM has a power supply distinct from the 5.0 V supplies.

E010, E009, E008, E007 ROM. These codes indicate ROM failures as follows:

E010 – ROM 5 (6000–7FFF) – U10
E009 – ROM 4 (8000–9FFF) – U35
E008 – ROM 3 (A000–BFFF) – U11
E007 – ROM 1,2 (C000–FFFF) – U9

The ROM Test adds together all 8K bytes in each ROM, ignores the overflow, and compares the result against a check sum stored in a single location. If the check sum for any ROM doesn't agree, the program jumps immediately back to test the first ROM again, and does not test the remaining ROM.

The error code isolates the problem down to the individual ROM. However, a failure in the 8K Select section of the Address Decoder could also cause the error, so the enabling lines (L ROME1,2 through L ROME5) should also be checked using the Free Run Test.

E006 Front Panel Bus. This error code usually indicates a failure in the A2 Front Panel Interface or A1 Front Panel assemblies. A description of the test can be found in the service section for those assemblies. However, it is possible that a failure in one of the Front Panel Bus Buffers (U22 or U32) can cause this error code. U32 is an inverting buffer that is always enabled; therefore, the output of each buffer should be the complement of its input.

U22 is a 3-state bi-directional buffer. Check the L WRITE (TP5) and L FPE (TP6) lines for activity, and ensure that identical data appears on both the input and output sides of the buffer when the L FPE is active low.

The Free Run Test can be used to check Front Panel Bus problems related to the A3 Microprocessor. Refer to the Address Decoder and Front Panel Bus sections of the Free Run Test description.

E005 Instrument Bus. This error code indicates a problem in the Instrument Bus, using the Self-Test hardware located on the A8 HP-IB Interface assembly. A full description of the test is contained in the service section for that assembly. However, the error code could also be produced by faulty Instrument Bus buffers on the A3 Microprocessor.

U26 is an inverting buffer that is always enabled; hence, inputs and outputs should be complements of each other.

U27 and U28 are inverting 3-state buffers. When enabled by L IBE, outputs should be complements of the inputs.

U25 is a bi-directional 3-state buffer enabled by L IBE and controlled by L WRITE. When enabled, inputs and outputs should be identical.

The Free Run Test can again be employed to isolate Instrument Bus errors traced back to the A3 Board. Refer to the Address Decoder and Instrument Bus sections of the Free Run Test description.

Free Run Test

The "Free Run Test" verifies the microprocessor U5 itself, provided the power supplies, power-on circuits, and clock circuits are functioning properly. This mode

of testing is also useful for checking the Address Decoder, the Address and Data Busses, and ROM.

The "Free Run Test" is initiated by setting the eight sections of S1 open, and connecting a jumper from L DSA (TP9) to GND (TP14). This isolates the microprocessor from the Data Bus, so that the program codes from ROM during normal operation have no effect. Instead, the command "Clear Register B" is continuously delivered to ,and executed by, the microprocessor. In this free-run mode, the microprocessor repetitively cycles through every address location (0000 to FFFF) in sequence.

Address Bus. Since the microprocessor increments through all the address locations in binary sequence, the fifteen address lines should show a "divide by two" relationship. The A0 line (least significant bit) toggles at half the rate of the Phase 1 and Phase 2 clocks. A1 toggles at half the rate of A0, A2 at half that, and so on to A15 (the most significant bit) which has a period of approximately 160 ms. Check each line for activity. Any line locked high or low could be caused by a faulty microprocessor output, shorted or opened bus lines, or a faulty input at an address line termination. If the "divide by two" relationship between two adjacent lines is not observed, these lines may be shorted together.

Address Decoding. As the address lines are sequenced through their range, the various I/O Ports, RAMs, and ROMs are selected in turn by the Address Decoder circuitry. The proper location and duration of these pulses in relation to the A15 line is shown in the Free Run Test Timing Diagram. These can be checked on a dual-trace oscilloscope by using a 20 ms/div sweep speed while triggering off the falling edge of the A15 line. TP12 has been provided to disable the VMA line controlling the Address Decoder. When TP12 is connected to Ground (TP14), all the enabling outputs from the Address Decoder should go high.

Data Bus. Since every possible I/O port and memory location is addressed while the microprocessor is in the free run mode, each of the data lines (D0 through D7) should show some activity. TP12 can be connected to GND to disable all ROM, RAM, and I/O outputs. In this condition, none of the 3-state drivers are enabled, and the Data Bus can be driven by an outside source. L A10 (TP11) is a convenient square-wave source while the microprocessor is in the Free Run Test. Connect TP12 to TP14 (DIG GND), and drive each of the data lines (D0 through D7) in turn at J3 with a jumper from TP11. Check each line at one of the Data Bus terminations (e.g. U22 or U25) for the L A10 signal. Also check all other data lines for adjacent shorts.

Front Panel Bus. The Front Panel bus is controlled by two buffers on the A3 Board. U32 is a uni-directional inverting buffer that is always enabled to pass five address lines and three control signals. In the Free Run Mode, the addresses cycle in binary sequence, so the "divide-by-two" sequence should be observed continuously on L FPA0 through L FPA4. FPE should show occasional bursts of activity, being an inverted version of L FPE shown in the Address Decoder Timing Diagram. L FPRD should remain in the low (read) state, and L FPSTB should strobe at roughly 823 kHz.

U22 is a bi-directional 3-state buffer passing 8 bits of data. In the Free Run Mode, this buffer is periodically enabled by L FPE to read in data. (Refer to the Free Run Test Timing Diagram.) Data is never written, since L WRITE stays high. The buffers can be easily tested by using L A10 (TP11) as an artificial source of data during Free Run. Pull the A2 Board out of the Motherboard to disconnect its data drivers. Connect TP11 to one of the Front Panel data lines (FPD0–FPD7); the extender board pins are convenient. Trigger the oscilloscope off L FPE, and

observe the corresponding data line on the microprocessor side using the Data Bus test pins. The L A10 signal should pass through the buffer only when L FPE goes low and at no other times. Check all data lines for adjacent shorts.

Instrument Bus. The Instrument Bus terminations on the A3 Board include four buffers: one for data, two for addressing, and one for control.

U26 is always enabled and passes six inverted control signals. In the Free Run Mode, L I/OCLK should run at 823 kHz. L I/OSTB should run at the same rate, but in bursts corresponding L IBE going low. The others — I/OE1, I/OE2, I/OE3, and PIROME — are inverted versions of the signals shown by the Free Run Test Timing Diagram.

U27 and U29 pass thirteen inverted address lines, plus L WRITE, to the Instrument Bus when L IBE is low. In the Free Run Mode, the address lines should show the usual "divide-by-two" relationship, but only when L IBE is active low. L IRD should remain low, since the microprocessor only reads during Free Run.

U25 is a bi-directional 3-state buffer also enabled by L IBE. The buffer is easily checked during Free Run. Remove the A4, A5, and A8 Assemblies from the Motherboard and remove the RF Plug-in. Connect L A10 (TP11) to the data line in question on the Instrument Bus side. By triggering off the L IBE line, the L A10 signal should be observed on the corresponding test point of the Data Bus when U25 is enabled. (Note that data is only read in.) Check all lines to eliminate the possibility of adjacent shorts.

A3 MICROPROCESSOR

MOTHERBOARD

P/O A8 HP-IB IN
P1
XA8
L IBIRQ → 2

P/O A6 RECTIFIER
P1
XA6
PWON → 6

P/O A2 FRONT PANEL INTERFACE
P1
XA2
INSTR PRESET
PWON → 43
L FPIRQ → 23
L RTCIRQ → 21

J2
RF PLUG-IN CONNECTOR
L PINMI 19
L PIIRQ 52
PIFLG 20

P/O A4 SCALING AND MARKER
P2
XA4B
L MFLG → 11

P/O A7 REGULATOR
P1
XA7
L PST → 4
L PSF → 27

XA3B
P2
41 ← PWON
XA3A
33 ← L IBIRQ
1 ← L FPIRQ
XA3B
40 ← L PINMI
20 ← L PIIRQ
19 ← L PIFLG
8 ← L RTCIRQ
3 ← L MFLG
XA3A
9 ← L PST
11 ← L PSF
XA3B
21 ← +5V BAT
OPTION 001 ONLY

Ⓐ CLOCK GENERATOR
CLOCK GENERATOR
CLOCK
TP27
10.7MHZ
IOS
AVS
DRIVER
Ø1,Ø2

Ⓑ INTERRUPT LOGIC AND STATUS BUFFER
INTERRUPT LOGIC
L NMI, L IRQ
2
ENABLE
L SBE
STATUS BUFFER
TP20
L TEST

Ⓒ SELF TEST ERROR CODE INDICATOR
2
L EAC
L EAR
8 4 2 1

Ⓓ MICROPROCESSOR SECTION
2 PHASE CLOCK
RESET
R/W
L WRITE
VMA
ADDRESS BUS (AØ-A15)
INTERRUPTS
TP9
LDSA
DATA BUS (DØ-D7)

CONTROL BUS
2
AVS, IOS

Ⓔ ADDRESS DECODER
L ROM 1,2-
L ROM5
II/OS
L IBE
L PIROME
L RAME1
L RAME2
L EAC
L SBE
L FPE
L I/OE1
L I/OE2
L I/OE3
L EAR
12
TP12
TP11

ADDRESS BU

Ⓚ SUPPLY FILTERING
VCCP

SERIAL PREFIX: 2024A

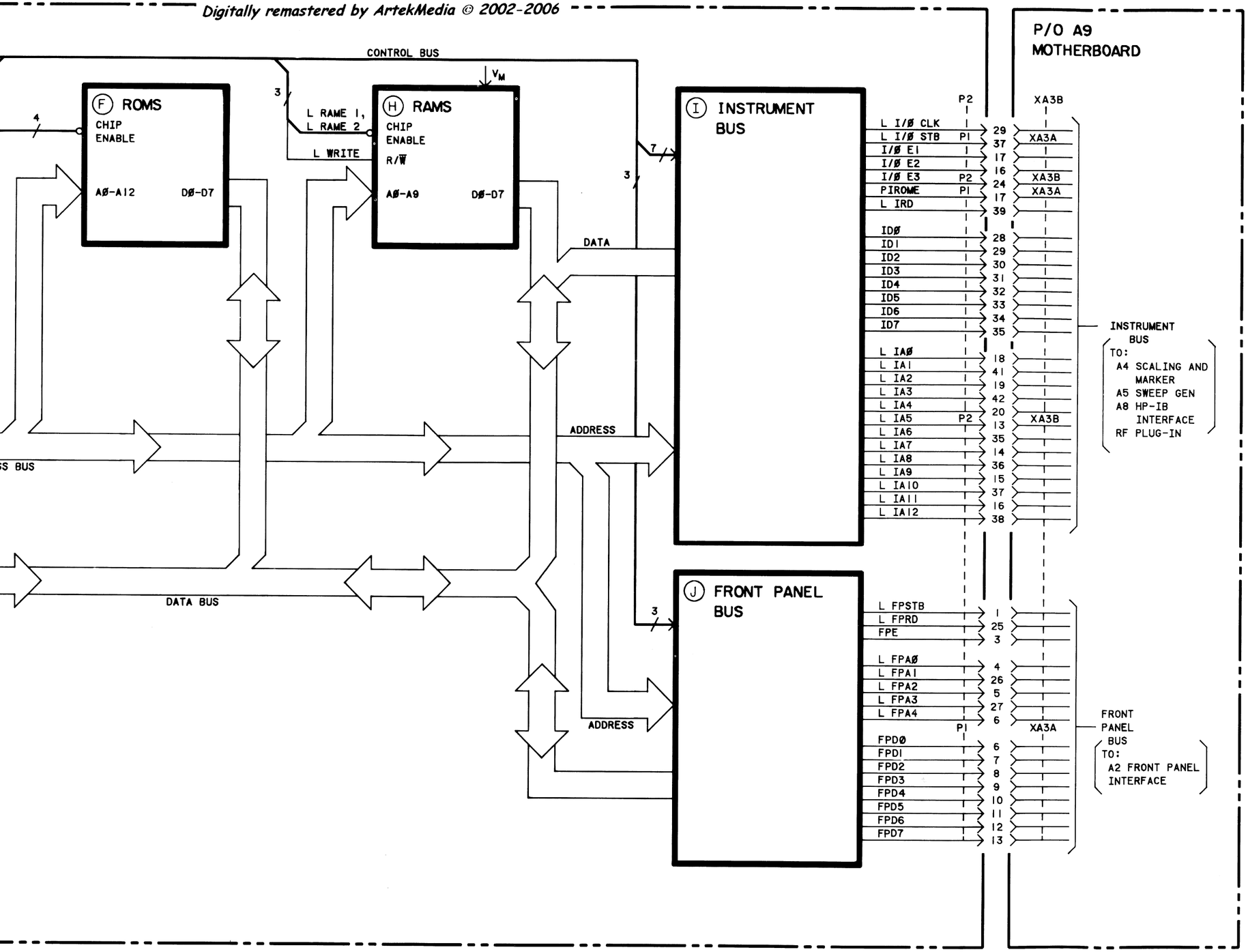


Figure 8-25. A3 Microprocessor, Block Diagram

Table 8-22. Instrument Preset Error Codes

Self Test	Error Code	DS1 (8)	DS2 (4)	DS3 (2)	DS4 (1)
Microprocessor	E015	ON	ON	ON	ON
RAM	E014	ON	ON	ON	OFF
	E013	ON	ON	OFF	ON
	E012	ON	ON	OFF	OFF
	E011	ON	OFF	ON	ON
ROM	E010	ON	OFF	ON	OFF
	E009	ON	OFF	OFF	ON
	E008	ON	OFF	OFF	OFF
	E007	OFF	ON	ON	ON
Front Panel Bus	E006	OFF	ON	ON	OFF
Instrument Bus	E005	OFF	ON	OFF	ON
Power Supplies	E004	OFF	ON	OFF	OFF
Tune Volt./Marker	E003	OFF	OFF	ON	ON
Sweep Marker	E002	OFF	OFF	ON	OFF
RF Plug-in	E001	OFF	OFF	OFF	ON
Pass Instr. Preset		OFF	OFF	OFF	OFF

Figure 8-29. A3 Microprocessor, Schematic Diagram

A3 MICROPROCESSOR
08350-60038 (08350-60036 FOR OPTION 001)

CONTROL BUS

Ⓐ CLOCK GENERATION

CLOCK OSCILLATOR

Y1 10.7MHz

U21D U21C U21A U21B

R1 511 R2 511 C5 36PF C6 36PF C7 .01

10.7MHz TP27

U12 2-31

PROM A0 PROM A1 PROM A2 PROM A3

ROM FF

U16 C8 .01 C9 .01

TP4 AVS TP10 IOS

PROM Ø1 PROM Ø2 I/OS AVS PROM A0 PROM A1 PROM A2 PROM A3

CLOCK GENERATOR

C10 68PF R3 4640 R5 1000 Q1 R8 21.5 TP2 Ø1

R54 10K C37 68PF Q3 R7 21.5

C11 68PF R4 4640 R6 1000 Q2 R10 21.5 C14 0.1

R55 10K C38 68PF Q4 R9 21.5 Ø2 TP1

CLOCK DRIVERS

Ⓒ SELF-TEST ERROR CODE INDICATOR

U3A L RES L EAR L EAC

U2A R C CTR (8) (4) (2) (1) C31 .01

U1 470 DS1 DS2 DS3 DS4

Ⓓ MICROPROCESSOR SECTION

P2-41 (IN) PWON TP23 R14 10K C30 1000PF U4B U4A C15 .01 L RES

U5 LRES Ø1 Ø2 DBE BA VCC L HALT L IRQ L NMI TSC NC NC VSS

+3.6V TP5 R21 10K L WRITE VMA

U6 10K

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 J1 J4

AVS

TP7 L IRQ TP8 L NMI C16 .01 R13 10K

U13 10K S1 D0 D1 D2 D3 D4 D5 D6 D7 J3

CR3 CR4 TP9 L DSA

Ⓔ ADDRESS DECODER

U24 A13 A14 A15 X

U1G 470 TP12 U3D VMA AVS I/OS PWON

U23 A10 A11 A12 A13

U18F U3B U18E A14 A15

Ⓑ INTERRUPT LOGIC AND STATUS BUFFER

STATUS BUFFER

U28 10K U20 3-ST TP19 LSBE

P2-11(IN)L PSF P2-9 (IN)L PST P2-19(IN)PIFLG L TEST P2-31(IN)L MFLG P2-8(IN)L RTCIRQ P2-20(IN)L PIIRQ P2-33(IN)L IBIRQ

D0 D1 D2 D3 D4 D5 D6 D7

TP 20 TP 30 TP 28 TP 31 TP 29

U34B U34A U34D U34C C12 1000PF C4 .01 TP21 IRQE R12 10K

P1-1(IN)L FPIRQ

TP16 NMIE R22 10K R23 10K U4C U4D C13 1000PF

P2-40(IN)L PINMI

INTERRUPT LOGIC

DATA BUS

Ⓚ SUPPLY FILTERING

P1-3,4,25,26 (IN) +5VA GND DIG P1-2,5,14,15,22,23, 24,27,36,38,40,44 P2-2,7,10,12,18,21,22,23 28,30,32,34,39,43,44 P1-21 (IN) +5V BAT

L1 C1 100 C2 100 VR1 6.19V SEE NOTE 2 W1 Q6 Q5 Q7 R18 133 C3 33 R20 10K R19 511 TP32 BAT TP18 TP17 TP14 CR1 CR2 R15 511 +5VA +5VF +5VCCP SEE NOTE 3 +3.6V

DATA BUS 8

13

SERIAL PREFIX: 2024A

CONTROL BUS

CONTROL BUS

ADDRESS BUS 13

DATA BUS 8

ADDRESS BUS 13

DATA BUS 8

ADDRESS BUS 13

DATA BUS 8

ADDRESS BUS 10

DATA BUS 8

ADDRESS BUS 8

DATA BUS 8

Ⓖ PROM BOARD CONNECTOR

J5 +5VA

L ROM1
L ROM2
L ROM3
L ROM4
L ROM5

Ⓕ ROMS

U9 U11 U35 U10 +5VF C27 C33 C29 C32 .01

A0-A8191

TP22 L ROM1,2
TP25 L ROM 3
TP26 L ROM4
TP24 L ROM5

ROM A0-A12 D0-D7

Ⓗ RAMS

U14 U15 U7 U8 +5VCCP C24 C23 C26 C34 .01

TP15 TP13

LRAM1 LRAM2 L WRITE

A0-A9 A0-A1023

RAM D0-D3

U23 U24 +5VF C20 C18 .01

X-Y

0 15 0000H
1 14 2000H
2 13 4000H
3 12 6000H
4 11 8000H
5 10 A000H
6 9 C000H
7 7 E000H

U17C U17A U17B U17D U3C U8C U8A U9B U9A U8B

I/OS PWON L IBE L PIROME L ROM5 L ROM4 L ROM3 L ROM1,2 L ROM2 L ROM1 L RAME2 L RAME1 L EAC L SBE L FPE L IOE1 L IOE2 L IOE3 L EAR II/OS

TP11 +5VCCP C36 .01

L RAM L LA10

0 0800H
1 1000H
2 1800H
3 2000H
4 2800H
5 3000H
6 3800H
7 3800H

Ⓘ INSTRUMENT BUS

U26 U31 U31F U27 U31G U31H U33 U29 U33 U31B U25 U30 +5VF C25 C17 C22 .01

3-ST

I/OS II/OS L I/O E1 L I/O E2 L I/O E3 L PIROME L IBE L WRITE

P2-29(I/O)L I/O CLK
P1-37(OUT)L I/O STB
P1-17(OUT)I/O E1
P1-16(OUT)I/O E2
P2-24(OUT)I/O E3
P2-17(OUT) PIROME
P1-18(OUT)L IA0
P1-41(OUT)L IA1
P1-19(OUT)L IA2
P1-42(OUT)L IA3
P1-20(OUT)L IA4
P2-13(OUT)L IA5
P2-35(OUT)L IA6
P2-14(OUT)L IA7
P2-36(OUT)L IA8
P2-15(OUT)L IA9
P2-37(OUT)L IA10
P2-16(OUT)L IA11
P2-38(OUT)L IA12
P1-39(OUT)L IRD
P1-28(I/O)ID0
P1-29(I/O)ID1
P1-30(I/O)ID2
P1-31(I/O)ID3
P1-32(I/O)ID4
P1-33(I/O)ID5
P1-34(I/O)ID6
P1-35(I/O)ID7

TP3 LIBE

R11 100 R16 100 R17 100

Ⓙ FRONT PANEL BUS

TP6 LFPE

U22 U32 +5VF C21 C28 .01

L WRITE L FPE I/OS A0 A1 A2 A3 A4

P1-6 (I/O) FPD0
P1-7 (I/O) FPD1
P1-8 (I/O) FPD2
P1-9 (I/O) FPD3
P1-10 (I/O) FPD4
P1-11 (I/O) FPD5
P1-12 (I/O) FPD6
P1-13 (I/O) FPD7
P2-1 (OUT) L FPSTB
P2-25 (OUT) L FPRD
P2-3 (OUT) FPE
P2-4 (OUT) L FPA0
P2-26 (OUT) L FPA1
P2-5 (OUT) L FPA2
P2-27 (OUT) L FPA3
P2-6 (OUT) L FPA4

Figure 8-29. A3 Microprocessor, Schematic Diagram

A3A1 PROM BOARD CIRCUIT DESCRIPTION

The A3A1 PROM Board stores the program software and constants used by the A3 Microprocessor. The board is mounted on the A3 Microprocessor Board, and directly substitutes for the ROM on the A3 Microprocessor. Connections for the address inputs (A0 through A12) and data outputs (D0 through D7) are made through A3A1W1, which connects to the A3U11 ROM socket on the A3 Microprocessor. The control line connections are made through A3A1W2 to A3J5.

Address Bus Buffers Ⓐ

Thirteen address lines (A0 through A12) are provided by the A3 Microprocessor Board to the A3A1 PROM Board through A3A1W1. These are buffered by a pair of 3-state buffers, U19 and U20. These buffers are always enabled, and continuously provide the PROM address signals (PA0 through PA12) to the Chip Select Decoding and PROM circuits.

Chip Select Decoder Ⓑ

The Chip Select circuits decode the five ROM Enable lines (LROM1 through LROM5) with address lines PA11 and PA12 to provide the eighteen PROM Enable lines (LEN1 through LEN18). These lines select the appropriate PROM for suppling data to the data bus. U28, U29, and U30 are two-to-four decoders with inverted outputs. Each decoder is enabled by one of the ROM Enable lines. In effect, the 8k blocks of address decoded by the A3 Address Decoding circuit is further broken down into 2k blocks for the PROMs. (See Table 8-23.) The memory space decoding is straightforward with the exception of the 8k block corresponding to LROM1. Out of 8k of memory space, only addresses F800 through FFFF (U30A, pin 7) are utilized. These addresses, plus addresses D800 through DFFF (U29B, pin 9), are ORed together through jumper E1 at U31B and enable the same PROM (U18). LEN16 and LEN17 are decoded and buffered, but are not used in the PROM circuit.

Chip Select Buffers Ⓒ

The Chip Select Buffers consist of dual-input Exclusive-OR gates, U23, U24, U25, U26, and U27. Each PROM Enable line is exclusive ORed with the L NORM control line from W2P1. This line is normally low, passing the PROM Enable signals from the Chip Select Decoding circuit through the Chip Select Buffers to the PROMs.

PROMs Ⓓ

The PROM circuit consists of sixteen 2k x 8 PROM packages. (The spaces for U16 and U17 are not loaded.) All sixteen are connected with parallel address inputs and data outputs. The PROM Enable lines (LENx) select only one PROM to be active at a time. The MEM EN (Memory Enable) control line is always high, allowing the PROM Enable lines to determine which PROM is being read while the others are inactive.

Data Bus Buffer Ⓔ

The eight data lines (PD0 through PD7) are buffered by bi-directional tri-state buffer (U21) before being fed to the Microprocessor Data Bus via W1P1. Combinational logic (U32 and U31C) ensures that the buffer is active only when at least one of the ROM Enable lines (LROMx) is low. The READ line controls the direction of the buffer, and is always high to read data out of PROM.

TROUBLESHOOTING

The program stored in PROM is tested with a "checksum" routine at initial power on or whenever the INSTR PRESET key is pressed. Error codes E007 through E010 indicate a problem in a specific section of memory. See Table 8-23 for memory locations of each error code. Since the "check sum" test is repeated if an error code is generated, the PROM board can be checked without initiating any further self test. Error code E015 may be generated if the PROM board can not be accessed to initiate the Self Test routine. Determine error code from the four LEDs on the A3 Microprocessor and troubleshoot as follows.

NOTE

If the problem is isolated to a faulty PROM, order a set of four masked ROMs (A3U9-11 and U35) and install them on the A3 Microprocessor. Contact your nearest Hewlett-Packard sales or service office, or check the lates yellow Manual Changes Supplement for the HP Part Number of the masked ROM set.

E015. The A3 Microprocessor is not able to access program stored in PROM. Problem could be on A3 or A3A1. Check the +5V power supplies at TP2 and TP7. Initiate the "Free Run" test described in the A3 Troubleshooting section (Open data lines with switch A3S1 and jumper A3TP9 to ground). Check that L MEMEN (A3A1TP6) and L NORM (A3A1TP4) are low, and that READ (A3A1TP3) is high. Check address and data lines on A3A1 for activity. Check each of the following control lines for activity:

- L ROM 1 (U32-1)
- L ROM 2 (U32-2)
- L ROM 3 (U32-3)
- L ROM 4 (U32-4)
- L ROM 5 (U32-5)
- L DBE (TP5)

Check PROM data lines as follows:

1. Initiate Free Run test (See A3 Microprocessor troubleshooting information.)
2. Jumper A3A1TP8 to ground.
3. Jumper A3TP11 to one of the PROM data lines (i.e. PD0 at A3A1U1 pin 9).
4. Externally trigger oscilloscope on the low transition of L DBE (A3A1TP5).
5. Check respective data line at A3J3 for activity coincident with active low L DBE.
6. Check all other data lines at A3J3 for shorts.

E007 through E010. Problem is with a specif Table 8-23 to determine control lines and PRO Check for activity on these control lines. If an LE problem towards the A3 Microprocessor. If all th problem is most likely the PROM.

If the problem is isolated to a PROM, the A3A1 PR with a set of masked ROMs on the A3 Microproce

Table 8-23. A3A1 PROM Addres

Error Code	ROM 8k Block	ROM Control	PROM 2k Block
10	6000-7FFF	LROM5	6000-67FF 6800-6FFF 7000-77FF 7800-7FFF
9	8000-9FFF	LROM4	8000-87FF 8800-8FFF 9000-97FF 9800-9FFF
8	A000-BFFF	LROM3	A000-A7FF A800-AFFF B000-B7FF B800-BFFF
7	C000-DFFF	LROM2	C000-C7FF C800-CFFF D000-D7FF D800-DFFF
7	E000-EFFF	LROM1	E000-E7FF E800-EFFF F000-F7FF F800-FFFF

*U16 and U17 are not loaded. U18 is enabled by addr the F800-FFF blocks. Refer to the text under "Chip description.

ad data out of PROM.

necksum" routine at initial power essed. Error codes E007 through of memory. See Table 8-23 for "check sum" test is repeated if an e checked without initiating any ed if the PROM board can not be ne error code from the four LEDs follows.

OM, order a set of four nd install them on the rest Hewlett-Packard lates yellow Manual Number of the masked

access program stored in PROM. V power supplies at TP2 and TP7. roubleshooting section (Open data ground). Check that L MEMEN nd that READ (A3A1TP3) is high. vity. Check each of the following

sor troubleshooting information.)

lines (i.e. PD0 at A3A1U1 pin 9).

transition of L DBE (A3A1TP5).

vity coincident with active low L

rts.

E007 through E010. Problem is with a specific block of memory. Refer to Table 8-23 to determine control lines and PROM associated with error code. Check for activity on these control lines. If an LENx line is inactive, trace the problem towards the A3 Microprocessor. If all the LENx lines are active, the problem is most likely the PROM.

If the problem is isolated to a PROM, the A3A1 PROM board should be replaced with a set of masked ROMs on the A3 Microprocessor.

Table 8-23. A3A1 PROM Address Decoding

Error Code	ROM 8k Block	ROM Control	PROM 2k Block	PROM Control	Ref Desig
10	6000-7FFF	LROM5	6000-67FF	LEN1	U1
			6800-6FFF	LEN2	U2
			7000-77FF	LEN3	U3
			7800-7FFF	LEN4	U4
9	8000-9FFF	LROM4	8000-87FF	LEN5	U5
			8800-8FFF	LEN6	U6
			9000-97FF	LEN7	U7
			9800-9FFF	LEN8	U8
8	A000-BFFF	LROM3	A000-A7FF	LEN9	U9
			A800-AFFF	LEN10	U10
			B000-B7FF	LEN11	U11
			B800-BFFF	LEN12	U12
7	C000-DFFF	LROM2	C000-C7FF	LEN13	U13
			C800-CFFF	LEN14	U14
			D000-D7FF	LEN15	U15
			D800-DFFF	LEN16/LEN18	U18*
7	E000-EFFF	LROM1	E000-E7FF	LEN17	Not Used
			E800-EFFF	Not Used	Not Used
			F000-F7FF	Not Used	Not Used
			F800-FFFF	LEN15/LEN18	U18*

*U16 and U17 are not loaded. U18 is enabled by addresses in either the D800-DFFF or the F800-FFF blocks. Refer to the text under "Chip Select Decoding" for a detailed description.

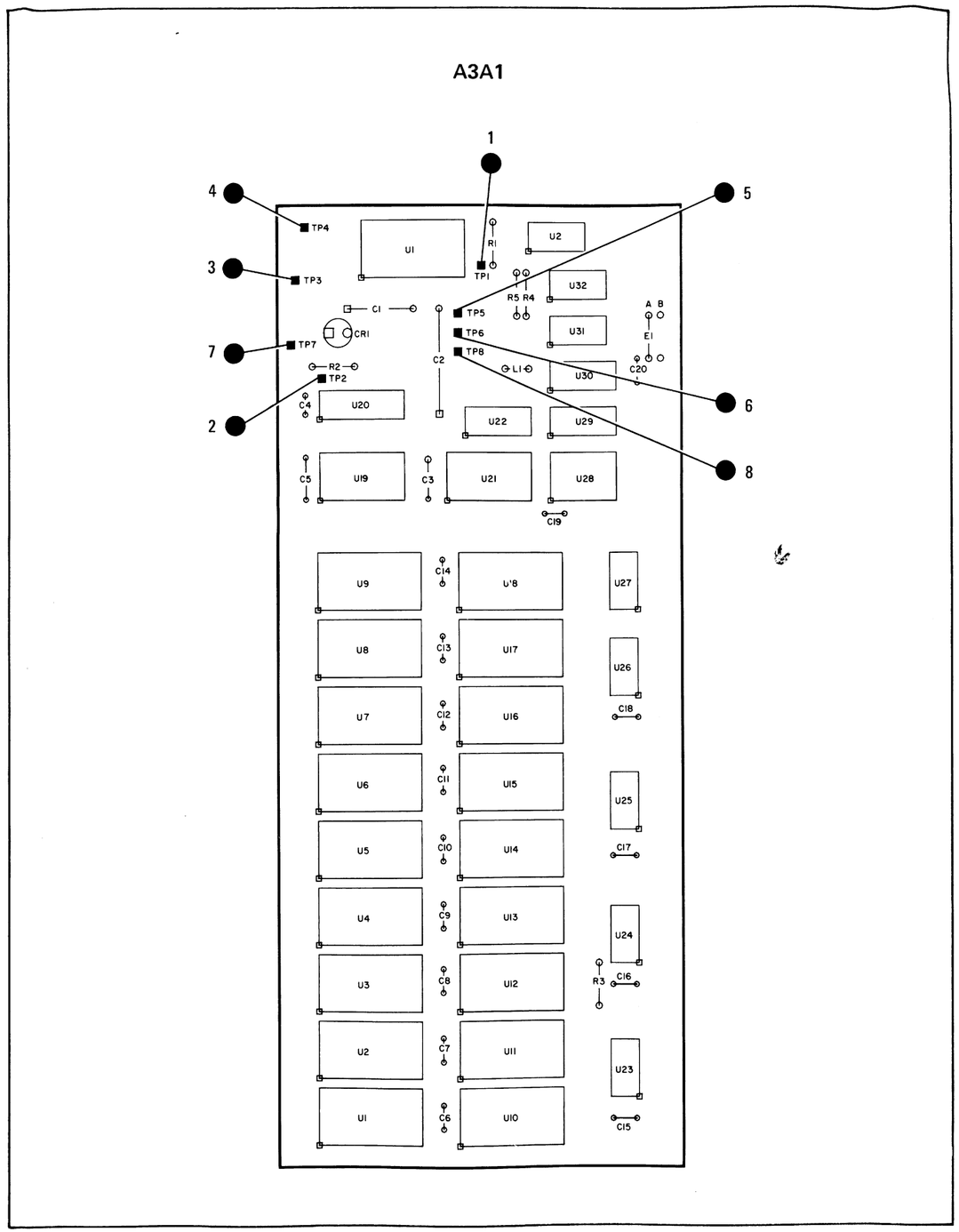


Figure 8-30. A3A1 PROM Assembly, Component Locations

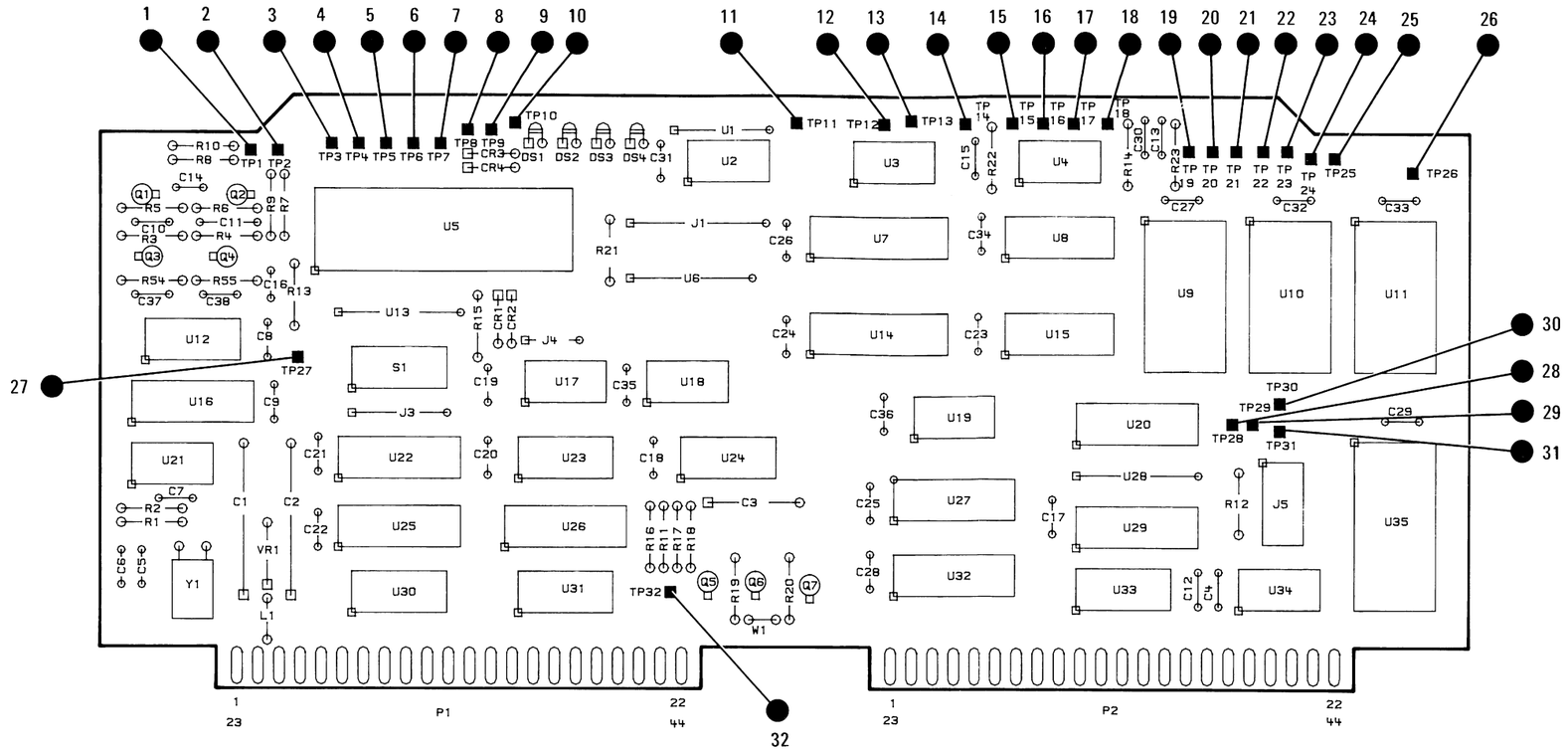


Figure 8-26. A3 Microprocessor, Component Locations

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

2. A3W1 IS NOT INSTALLED FOR OPTION 001 NONVOLATILE MEMORY.

3. +5VCCP IS THE RAM POWER SUPPLY. FOR OPTION 001, THIS VOLTAGE IS MAINTAINED BY +5V BAT WHEN THE MAIN POWER IS TURNED OFF.

4. IF A3A1 PROM BOARD IS MOUNTED ON A3, THE A3 ROMS ARE NOT INSTALLED AND THE PROM BOARD CONNECTIONS ARE THROUGH A3J5 AND THE SOCKET FOR A3U11.

*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◄ ► TO STEP TO THE NEW ADDRESS.

A3P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1	L FPIRQ	IN	A2P1-23	B
23	GND DIG			K
2	GND DIG			K
24	GND DIG			K
3	+5VA	IN	A7P1-2, 24	K
25	+5VA	IN	A7P1-2, 24	K
4	+5VA	IN	A7P1-2, 24	K
26	+5VA	IN	A7P1-2, 24	K
5	GND DIG			K
27	GND DIG			K
6	FPD0	I/O	A2P1-28	J
28	ID0	I/O	INST. BUS	I
7	FPD1	I/O	A2P1-28	J
29	ID1	I/O	INST. BUS	I
8	FPD2	I/O	A2P1-7	J
30	ID2	I/O	INST. BUS	I
9	FPD3	I/O	A2P1-29	J
31	ID3	I/O	INST. BUS	I
10	FPD4	I/O	A2P1-8	J
32	ID4	I/O	INST. BUS	I
11	FPD5	I/O	A2P1-30	J
33	ID5	I/O	INST. BUS	I
12	FPD6	I/O	A2P1-9	J
34	ID6	I/O	INST. BUS	I
13	FPD7	I/O	A2P1-31	J
35	ID7		INST. BUS	I
14	GND DIG			K
36	GND DIG			K
15	GND DIG			K
37	L I/OSTB	OUT	INST. BUS	I
16	I/OE2	OUT	INST. BUS	I
38	GND DIG			K
17	I/OE1	OUT	INST. BUS	I
39	L IRD	OUT	INST. BUS	I
18	L IA0	OUT	INST. BUS	I
40	GND DIG			K
19	L IA2	OUT	INST. BUS	I
41	L IA1	OUT	INST. BUS	I
20	L IA4	OUT	INST. BUS	I
42	L IA3	OUT	INST. BUS	I
21	+5V BAT	IN	BT1	K
43	GND DIG			K
22	GND DIG			K
44	GND DIG			K

A3P2

PIN	SIGNAL	I/O
1	L FPSTB	OUT
23	GND DIG	
2	GND DIG	
24	I/OE3	OUT
3	FPE	OUT
25	L FPRD	OUT
4	L FPA0	OUT
26	L FPA1	OUT
5	L FPA2	OUT
27	L FPA3	OUT
6	L FPA4	OUT
28	GND DIG	
7	GND DIG	
29	L I/OCLK	OUT
8	L RTCIRQ	IN
30	GND DIG	
9	L PST	IN
31	L MFLG	IN
10	GND DIG	
32	GND DIG	
11	L PSF	IN
33	L IBIRQ	IN
12	GND DIG	
34	GND DIG	
13	L IA5	OUT
35	LIA6	OUT
14	L IA7	OUT
36	LIA8	OUT
15	L IA9	OUT
37	L IA10	OUT
16	L IA11	OUT
38	L IA12	OUT
17	PIROME	OUT
39	GND DIG	
18	GND DIG	
40	L PINMI	IN
19	L PIFLG	IN
41	PWON	IN
20	L PIIRQ	IN
42	N. C.	
21	GND DIG	
43	GND DIG	
22	GND DIG	
44	GND DIG	

	I/O	TO/FROM	FUNCTION
	OUT	A2P1-13	J K
	OUT	INST. BUS	K I
	OUT OUT	A2P1-15 A2P1-37	J J
	OUT OUT	A2P1-16 A2P1-38	J J
	OUT OUT	A1P1-17 A2P1-39	J J
	OUT	A2P1-18	J K
	OUT	INST. BUS	K I
	IN	A2P1-21	B K
	IN IN	A7P1-4 A4P2-11	B B
			K K
	IN IN	A7P1-27 A8P1-2	B B
			K K
	OUT OUT	INST. BUS INST. BUS	I I
	OUT OUT	INST. BUS INST. BUS	I I
	OUT OUT	INST. BUS INST. BUS	I I
	OUT OUT	INST. BUS INST. BUS	I I
	OUT	J2-45	I K
	IN	J2-19	K B
	IN IN	J2-20 A6P1-6	B D
	IN	J2-52	B
			K K
			K K

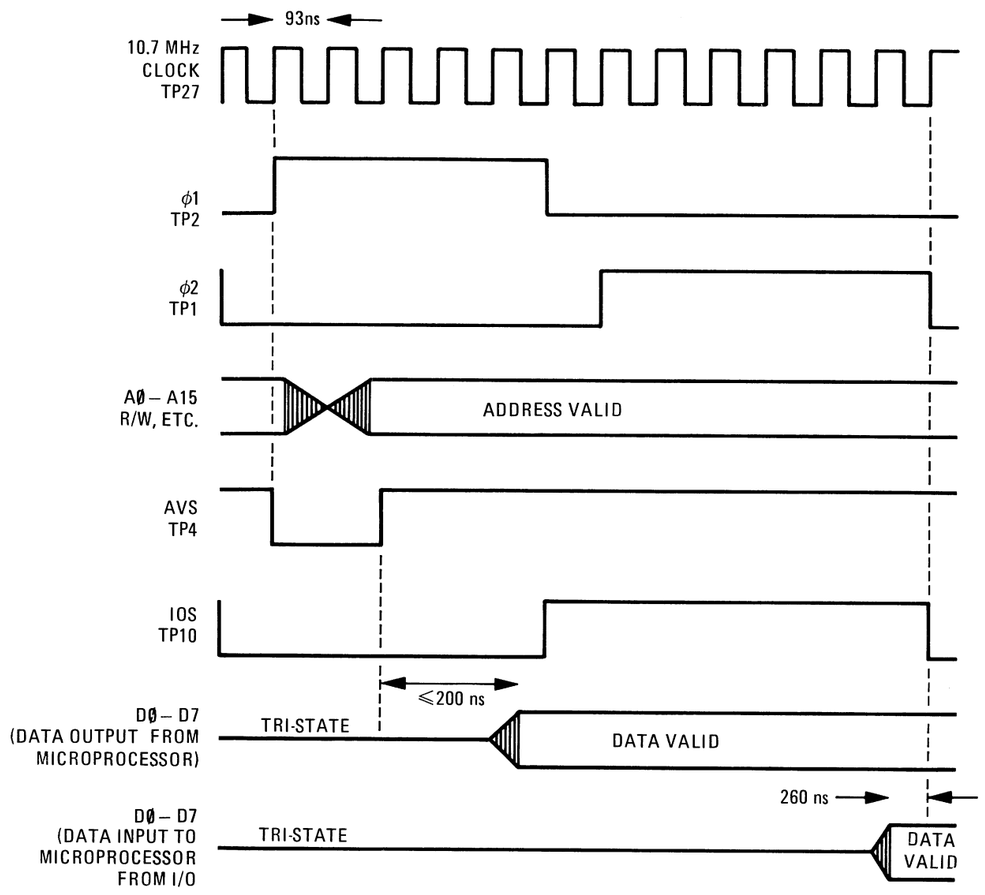


Figure 8-27. A3 Microprocessor Read/Write Timing Diagram

FREE RUN TEST:

SET 8 SECTIONS OF A3S1 OPEN

JUMPER A3TP9 TO GROUND (A3TP14)

TRIGGER OSCILLOSCOPE ON NEGATIVE EDGE OF A15 (A3J4-1)

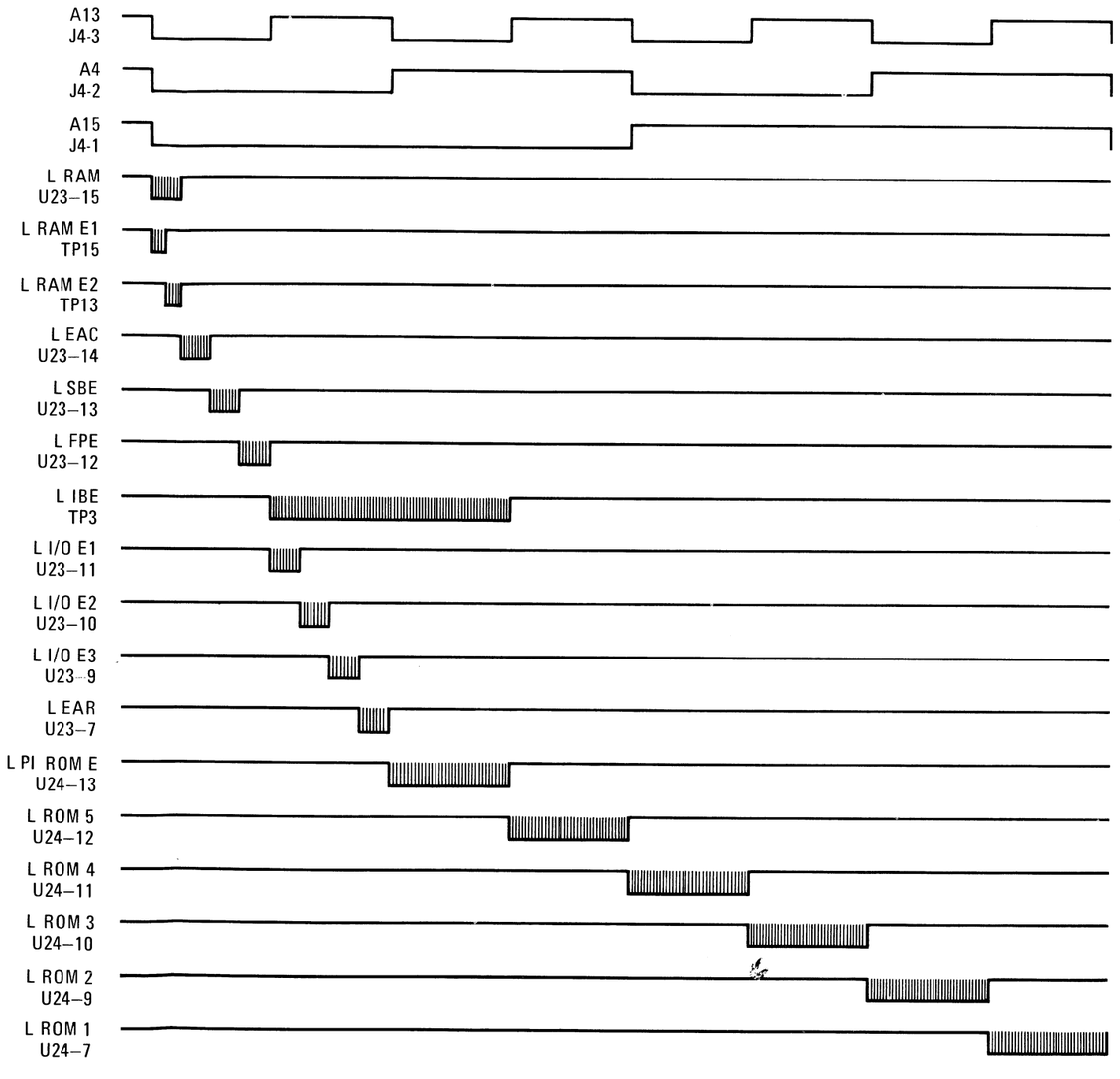


Figure 8-28. Free Run Test, Timing Diagram

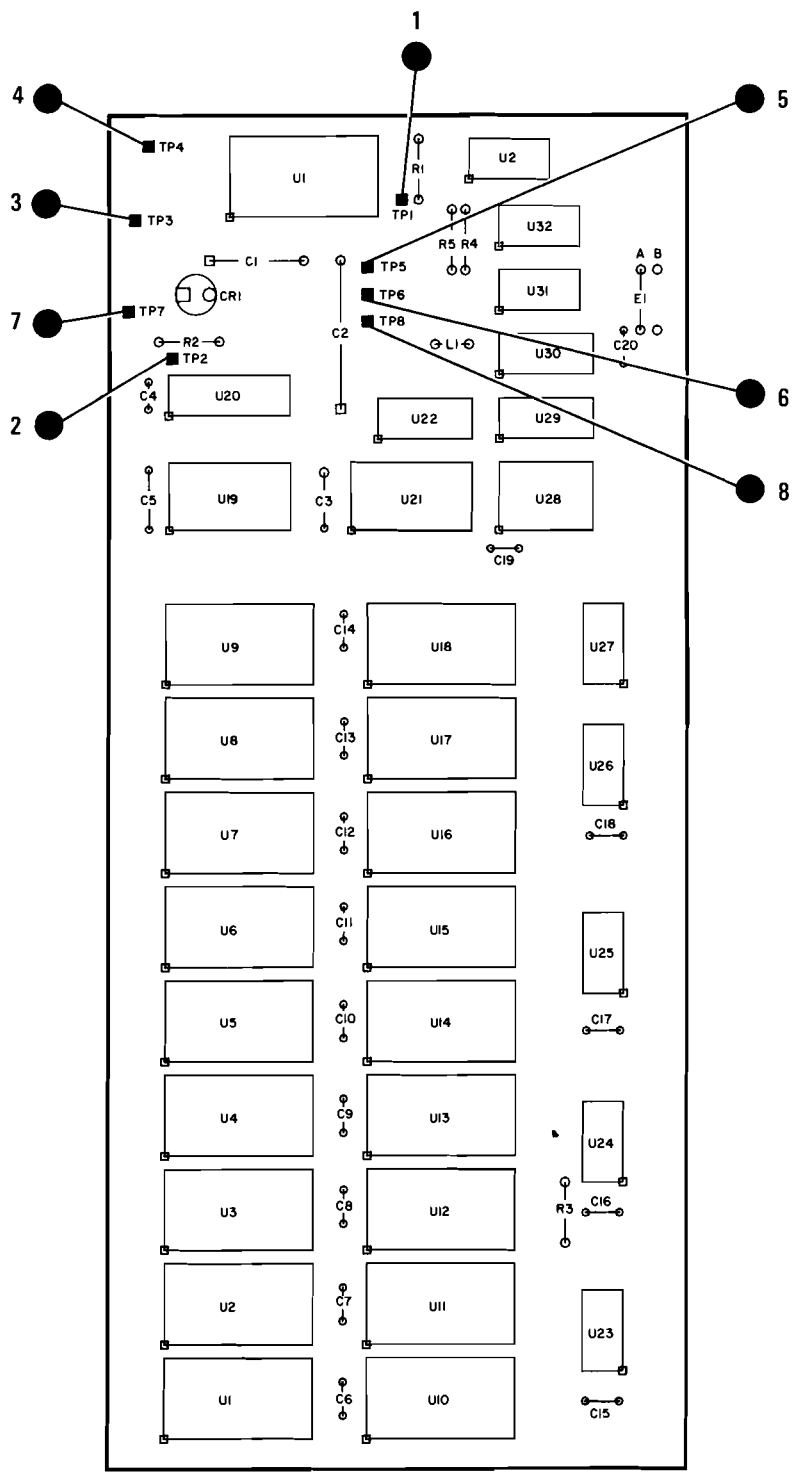


Figure 8-30. A3A1 PROM Assembly, Component Locations

A3A1 PROM
08350-60030

FROM A3J5
FROM A3U11 SOCKET

W2P1 W2 W1 W1P1

L ROM1(IN) 1
L ROM2(IN) 2
L ROM3(IN) 3
L ROM4(IN) 4
L ROM5(IN) 5
DBE(+5VA)(IN) 9
L NORM(IN) 10
MEM EN(+5VA)(IN) 11
READ(+5VF)(IN) 24

9 CONTROL BUS

Ⓐ ADDRESS BUS BUFFERS

U19 U20 — 3-ST — +5VF — C5 0.1 — C4 0.1 — F1 F2

AØ	11	9	PAØ
A1	8	12	PA1
A2	13	7	PA2
A3	15	5	PA3
A4	4	16	PA4
A5	17	3	PA5
A9	2	18	PA9
A10	6	14	PA10
A6	6	14	PA6
A7	4	16	PA7
A8	15	5	PA8
A11	2	18	PA11
A12	17	3	PA12
NC	8	12	NC
NC	11	9	NC
NC	13	7	NC

W1P1 W1

AØ(IN) 8
A1(IN) 7
A2(IN) 6
A3(IN) 5
A4(IN) 4
A5(IN) 3
A6(IN) 2
A7(IN) 1
A8(IN) 23
A9(IN) 22
A10(IN) 19
A11(IN) 18
A12(IN) 21

8 13 5 5 8

Ⓑ CHIP SELECT DECODER

U30A U31A U31B U29B U29A U28B U28A — +5VF — C20 .01 — E1

L ROM1 L ROM2 L ROM3 L ROM4 L ROM5

PA11 PA12 EN X→Y NC

5 13 2 11

Ⓒ CHIP SELECT BUFFERS

TP4 R3 10K +5VF L NORM

U27B 6 L EN 18 F800H
U26B 6 L EN 17 E000H
U26A 3 L EN 16 D800H
U25B 6 L EN 15 D000H
U25A 3 L EN 14 C800H
U24B 6 L EN 13 C000H
U24A 3 L EN 12 B800H
U23B 6 L EN 11 B000H
U23A 3 L EN 10 A800H
U27C 8 L EN 9 A000H
U26C 8 L EN 8 9800H
U26D 11 L EN 7 9000H
U25C 8 L EN 6 8800H
U25D 11 L EN 5 8000H
U24C 8 L EN 4 7800H
U24D 11 L EN 3 7000H
U23C 8 L EN 2 6800H
U23D 11 L EN 1 6000H
U27A NC
U27D NC

18

Ⓕ SUPPLY FILTERING

W2P1 W2

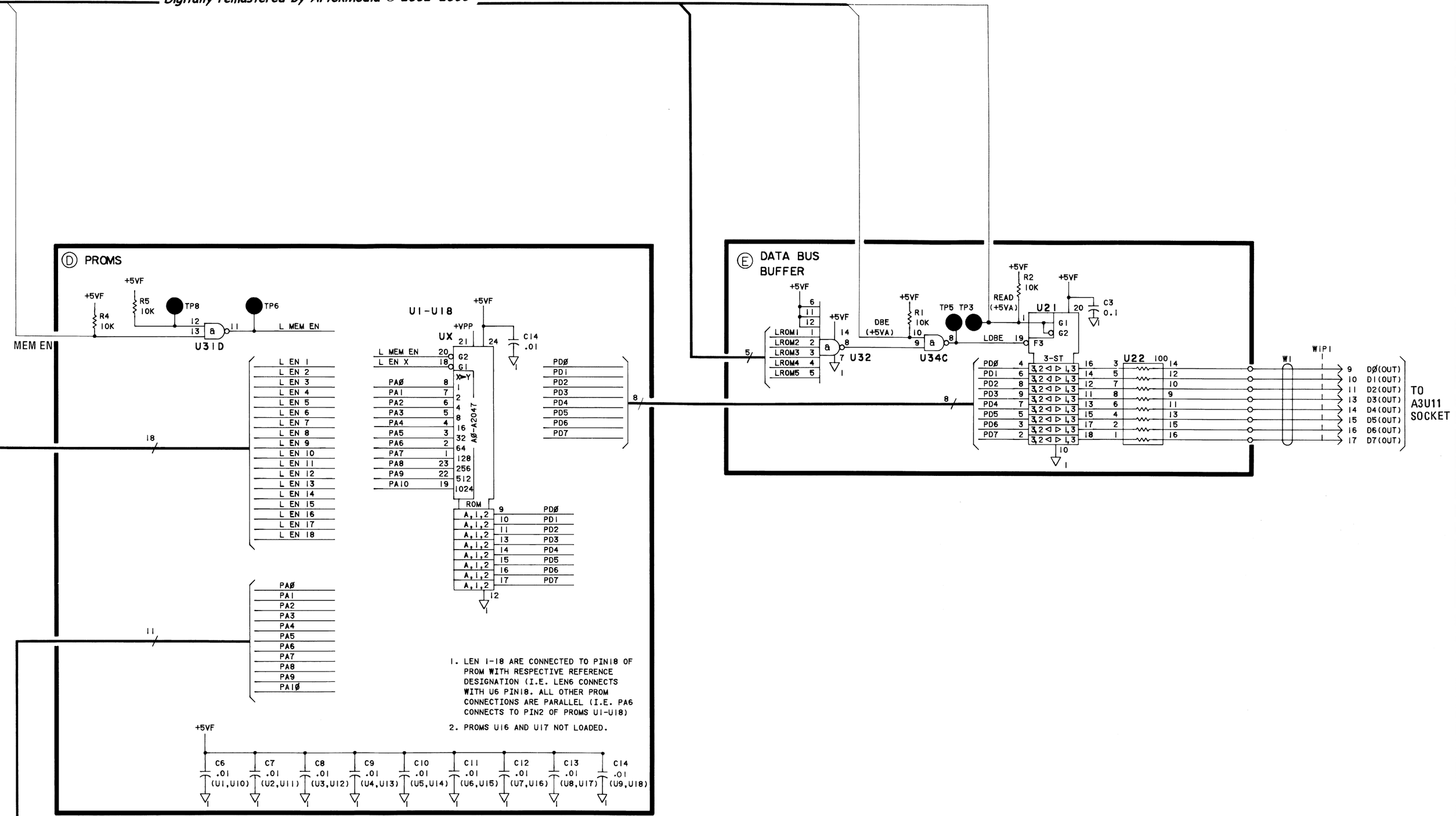
+5VA(IN) 13
+5VA(IN) 14
VPP(IN) 12
GND DIG(IN) 6
GND DIG(IN) 7
GND DIG(IN) 8

FROM A3J5

L1 C1 33 C2 100 CR1 TP1 TP2 TP7 +5VF VPP

ADDRESS BUS 11

SERIAL PREFIX: 2024A



A3A1

Figure 8-30A. A3A1 PROM Assembly, Schematic Diagram

A4 SCALING AND MARKER ASSEMBLY, CIRCUIT DESCRIPTION

The A4 Scaling and Marker assembly provides a scaled tuning voltage (VTUNE) to the RF Plug-in, and generates marker pulses for the five 8350A markers (M1 through M5). A +10V Reference supply provides an accurate reference voltage for all Digital-to-Analog Converters (DACs) in the 8350A. The Address Decoder and Data Buffer provide the interface with the A3 Microprocessor.

Scaling Circuits. The VTUNE output is the sum of the three following scaling DAC outputs.

- CW, CF Generation – The voltage at TP8 is proportional to CW frequency or the Center Frequency (CF) during swept operation. This output voltage is determined by data written into DAC U9 through data latches U15 and U17A.
- Vernier – The output current at TP9 is proportional to front panel VERNIER control. This control provides fine adjustment of CW, CF frequency. Data is written to DAC U10 through data latch U16.
- ΔF Generation – The output voltage at TP6 is proportional to the frequency range swept (i.e. For a 2 GHz to 3 GHz sweep, ΔF is 1 GHz.) The 0 to +10V sweep ramp (VSW1) at TP1 is scaled by DAC U7 according to data written into data latches U13 and U14. Analog switch U8A/B/C provides further scaling according to the ratio of ΔF sweep to full band sweep.

Marker Circuits. The Marker circuits generate a pulse corresponding to each selected marker frequency. A pulse is also generated corresponding to the active marker, that is, the marker whose key annunciator is blinking.

For each marker, two data bytes are neccessary from the A3 Microprocessor to generate one marker pulse; one byte corresponding to the beginning of marker, and one byte corresponding to end of marker. Therefore, to generate five separate markers, a total of ten bytes are required. One additional byte, the marker terminator byte, is required to ensure that no more than five marker pulses are generated.

The marker counter in the Marker Counter and Active Marker Comparator is used to select the address locations of Marker RAM. The ten marker bytes plus the marker terminator byte are stored in the Marker RAM. The marker bytes are stored in frequency order, not the number order as they are designated on the front panel. The leading edge marker byte for the lowest frequency marker is stored in the lowest RAM address location (hexadecimal 0), followed by the trailing edge byte in the next higher RAM address location (hexadecimal 1). The marker terminator byte is stored in RAM address location hexadecimal A (following the trailing edge of the fifth marker). Refer to Table 8-24 for the RAM address mapping.

The marker bytes are the digital inputs which program the Marker DAC. During the sweep, the output from the Marker DAC is compared to a current developed from VRAMP in the Comparator and Marker Pulse Generator. From two bytes of information, one marker pulse (L MK) is developed at TP18. Feedback from the Comparator and Marker Pulse Generator is provided to increment the marker counter in the Marker Counter and Active Marker Comparator.

To determine the active marker, the microprocessor compares the output of the Marker Counter to the known RAM address of the active marker stored in data latch U17B. The LAMK, low active marker pulse is generated when the marker counter output equals the active marker address.

Table 8-24. Marker RAM Memory Map

Address Location (Hexadecimal)	Data Information
0	Leading edge of first marker (Lowest Frequency Marker)
1	Trailing edge of first marker (Lowest Frequency Marker)
2	Leading edge of second marker
3	Trailing edge of second marker
4	Leading edge of third marker
5	Trailing edge of third marker
6	Leading edge of fourth marker
7	Trailing edge of fourth marker
8	Leading edge of fifth marker (Highest Frequency Marker)
9	Trailing edge of fifth marker (Highest Frequency Marker)
A	Marker Terminator (FF)

Data Buffer Ⓐ

Data buffer U25 is a 3state buffer that is always enabled and buffers the Instrument data bus lines D0–D7 on the A4 Scaling and Marker Assembly. Since data is only written to (not read from) the A4 assembly, U25 only passes data in one direction.

Address Decoder Ⓑ

The A4 assembly uses address locations 3000H through 3007H. When the instrument bus contains a valid address for this assembly, 3-to-8 decoder U20 decodes the address to determine which device on the A4 assembly is addressed by the A3 Microprocessor.

3-state buffer U26 buffers the I/OE3, L IRD, I/OSTB, and instrument address bus lines L IA0 through L IA2. Three-to-eight decoder U20 is enabled by L I/OE3, L WRITE, and L I/OSTB. U20 decodes address lines L IA0 through L IA2 and generates the low active chip select signals (LEN1–LEN7) for the A4 assembly. See Table 8-25 for an index of the address decoding.

Table 8-25. Scaling and Marke

Address (Hexadecimal)	Address Decoder Components	Components Addressed
3000	U20, U26	U16
3001	U20, U26	U15
3002	U20, U26	U17A, U17B
3003	U20, U26	U13
3004	U20, U26	U14
3005	U20, U26	U21
3006	U20, U26	U21, U18, U23
3007	U20, U26	Not Used

CW, CF Generation Ⓒ

The CW, CF Generation circuit generates a
selected CW frequency or the center frequency

The A3 Microprocessor writes on the Instrume
the CW or CF frequency. Since U9 is a 12-b
required to load the DAC. Data flip-flops U15
instrument data bus when clocked by LEN2 a
applied to the inputs of digital to analog con
programmable current source, with the maxim
the +10V V_{REF} input. Operational amplifi
conversion with its feedback resistor internal t
therefore the voltage at TP8, is directly propor
loaded. The output is applied through resistor R
2. CW adjustment R27 sets the gain for the C

RKER ASSEMBLY, CIRCUIT DESCRIPTION

r assembly provides a scaled tuning voltage (VTUNE) to erates marker pulses for the five 8350A markers (M1 erence supply provides an accurate reference voltage for verters (DACs) in the 8350A. The Address Decoder and nterface with the A3 Microprocessor.

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current at TP9 is proportional to front panel VERNIER provides fine adjustment of CW, CF frequency. Data is through data latch U16.

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Marker circuits generate a pulse corresponding to each . A pulse is also generated corresponding to the active r whose key annunciator is blinking.

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5	Trailing edge of third marker
6	Leading edge of fourth marker
7	Trailing edge of fourth marker
8	Leading edge of fifth marker (Highest Frequency Marker)
9	Trailing edge of fifth marker (Highest Frequency Marker)
A	Marker Terminator (FF)

Data Buffer Ⓐ

Data buffer U25 is a 3state buffer that is always enabled and buffers the Instrument data bus lines D0–D7 on the A4 Scaling and Marker Assembly. Since data is only written to (not read from) the A4 assembly, U25 only passes data in one direction.

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The A4 assembly uses address locations 3000H through 3007H. When the instrument bus contains a valid address for this assembly, 3-to-8 decoder U20 decodes the address to determine which device on the A4 assembly is addressed by the A3 Microprocessor.

3-state buffer U26 buffers the I/OE3, L IRD, I/OSTB, and instrument address bus lines L IA0 through L IA2. Three-to-eight decoder U20 is enabled by L I/OE3, L WRITE, and L I/OSTB. U20 decodes address lines L IA0 through L IA2 and generates the low active chip select signals (LEN1–LEN7) for the A4 assembly. See Table 8-25 for an index of the address decoding.

Table 8-25. Scaling and Marker Address Decoding

Address (Hexadecimal)	Address Decoder Components	Components Addressed	Read or Write	Description
3000	U20, U26	U16	WRITE	Address data latch for Vernier DAC U10.
3001	U20, U26	U15	WRITE	Address data latch for lower 8 bits of CW, CF DAC U9.
3002	U20, U26	U17A, U17B	WRITE	Address data latch for upper 4 bits of CW, CF DAC U9, and Active Marker Comparator U22.
3003	U20, U26	U13	WRITE	Address data latch for lower 8 bits of ΔF DAC U7.
3004	U20, U26	U14	WRITE	Address data latch for upper 2 bits of ΔF DAC U7, Scaling Switch U8A, B, C, Self Test Switch U8D, and MARKER DISABLE Gate U27C
3005	U20, U26	U21	WRITE	Preset Marker Counter U21 to data input value.
3006	U20, U26	U21, U18, U23	WRITE	Decrement Marker Counter by one count. Address Marker RAM U18, U23.
3007	U20, U26	Not Used		

CW, CF Generation Ⓒ

The CW, CF Generation circuit generates a voltage at TP8 proportional to the selected CW frequency or the center frequency (CF) of a swept frequency setting.

The A3 Microprocessor writes on the Instrument data bus the digital equivalent of the CW or CF frequency. Since U9 is a 12-bit DAC, two write operations are required to load the DAC. Data flip-flops U15 and U17A latch the data from the instrument data bus when clocked by LEN2 and LEN3 respectively. This data is applied to the inputs of digital to analog converter (DAC) U9. U9 is basically a programmable current source, with the maximum current available determined by the +10V V_{REF} input. Operational amplifier U3 provides current-to-voltage conversion with its feedback resistor internal to U9. The DAC current output, and therefore the voltage at TP8, is directly proportional to V_{REF} and the digital value loaded. The output is applied through resistor R40 to the summing junction, U4 pin 2. CW adjustment R27 sets the gain for the CW signal.

ΔF Generation Ⓓ

The ΔF Generation circuit generates the scaled ramp portion of the tuning voltage for all swept frequency modes. The A3 Microprocessor sends out on the instrument data bus the digital equivalent of the swept frequency setting. Data flip-flops U13 and U14 latch the data when clocked by LEN4 and LEN5 respectively.

VSW1, is a 0V to +10V ramp from the A5 Sweep Generator Assembly. Operational amplifier U6 offsets and amplifies the VSW1 input to provide a −10V to +10V ramp output. Potentiometer R2 provides an offset adjustment for the ramp output. This −10V to +10V ramp is applied to DAC U7 as the reference voltage (V_{REF}). Since V_{REF} is proportional to the sweep ramp, the digital data loaded scales the ramp output at TP3 to provide a ramp proportional to the swept frequency range.

Over wide sweep widths the inverted scaled output of U1 is selected by switch U8A and applied to the noninverting input of U2. For narrower sweep widths the output of U1 is applied through divider network R14, R15, R16 (divide by eight) or R17, R18, R19 (divide by 64) to provide greater resolution. The switching occurs when the swept frequency range is 1/8 or 1/64 of the RF Plug-in band. U8 selects the appropriate scaled ΔF signal. Data lines D2 through D4 (DA210 through DA212) are latched by U14 and control the switch settings of U8.

The selected ΔF signal is applied to buffer U2 and is sent to the summing junction via R36, R50, and R25. ΔF1 potentiometer R25 sets the ΔF gain, R15 (ΔF2) and R18 (ΔF3) adjust the divide ratio for the higher resolution settings (narrow sweeps).

Vernier Ⓔ

The Vernier DAC provides a symmetrical output corresponding to a vernier range of ± 0.05% of the frequency range of the RF Plug-in.

The A3 Microprocessor writes on the Instrument data bus the digital equivalent of the CW vernier setting on the front panel of the 8350A. This data is latched into U16 when clocked by LEN1. The data is applied to the digital inputs of DAC U10.

+10 V_{REF} is applied through R10 to pin 14 of DAC U10. This voltage is converted into a current internal to U10 and is scaled according to the digital inputs. The resultant current is then applied through a current divider comprised of R24, R23, and R22 to the summing junction, U4 pin 2. R22 (VERNIER) adjusts the vernier gain, and R44 adjusts the CW offset. The DAC is set to midrange when the Vernier setting is zero.

Summing Amplifier Ⓕ

The outputs from the three scaling DACs are summed together at the summing junction, U4 pin 2. This combined signal is inverted through U4 and becomes VTUNE. CR1 and VR1 are utilized as protection diodes to prevent VTUNE from going beyond +11.0 volts or lower than −0.6 volts. VTUNE exits the assembly via J1 and is sent to the plug-in connector J3 via cable W3. VTUNE is also supplied to the Comparator and marker Pulse Generator through the Self Test switch (U8D) during the Tuning Voltage versus Marker self-test.

Self Test (I)

The Tuning Voltage versus Marker DAC self test is initiated at initial power on, during instrument preset, or when SHIFT 1 0 is entered. During this test, SELF TEST ENABLE from the ΔF Generation circuit goes high engaging switch U8D. The output from the summimg amplifier U4 is compared to the output from the Marker DAC at pin 3 of U11. When the value of the combined outputs crosses zero volts, U11 pin 7 goes low. This signal is buffered through U27B and is sent to the A3 Microprocessor as LMFLG (Low=Marker Flag). If the microprocessor does not receive the LMFLG signal during power on or instrument preset, error message E003 is displayed on the front panel.

+10V Reference (G)

$+10V_{REF}$ is applied through R35 to three parallel resistor zener diode networks, R56 VR5, R57 VR6 R58 VR7. This reduces the noise on the +6.2 volt signal applied to the noninverting input of operational amplifier U5. Feedback is provided through Q1, R13 and R59. R59 sets the gain for U5, and is adjusted for +10 volts at TP14. Q1 provides current drive capability for the +10 volt supply. +15VF through R7 and R35 provides initial start-up bias.

Marker Circuits (H) (J) (K) (L)

The Marker circuits produce a Low Marker pulse (L MK) and Marker Flag (L MFLG) output for each marker. LMFLG is used only for Self tests. During sweep retrace, the A3 Microprocessor loads the Marker RAM with two data bytes for each marker position. The Marker RAM addressing is controlled by Marker Counter U21. At the beginning of each forward sweep, Marker Counter U21 is preset to zero to access the data for the leading edge of the lowest frequency marker. This data byte is used to program Marker DAC U12. Marker Comparator U11 compares the DAC output with the sweep ramp voltage (VRAMP), and generates a low output when they are equal. The Marker counter is incremented, and the Marker DAC output is increased to correspond with the marker trailing edge position. This results in Marker Comparator output being reset high, and enable the detection of the marker trailing edge.

Marker Load Cycle. Two enable lines are used during the load cycle. LEN6 which presets Marker Counter U21, and LEN7 which enables the writing of data to the Marker RAM, and decrements the marker counter. The following sequence occurs during every sweep retrace.

NOTE

The Marker RAM data output is the complement of its data input. For example, to obtain all high outputs (hexadecimal FF), all data inputs must be low (hexadecimal Ø Ø).

The A3 Microprocessor writes on Instrument Bus data lines D0 through D3 the hexadecimal value A. LEN6 is set low and this value is loaded into Marker Counter U21. This value appears at the counter output and addresses Marker RAM location A (hexadecimal). The A3 Microprocessor then writes on the Instrument Bus data lines D0 through D7 the marker terminator byte. LEN7 is set low, and the terminator byte is written to the Marker RAM (hexadecmical Ø Ø is loaded so that the RAM data output will be hexadecimal FF). LEN7 simultaneously decrements the Marker Counter U21 to address the next lower RAM address (9). The A3

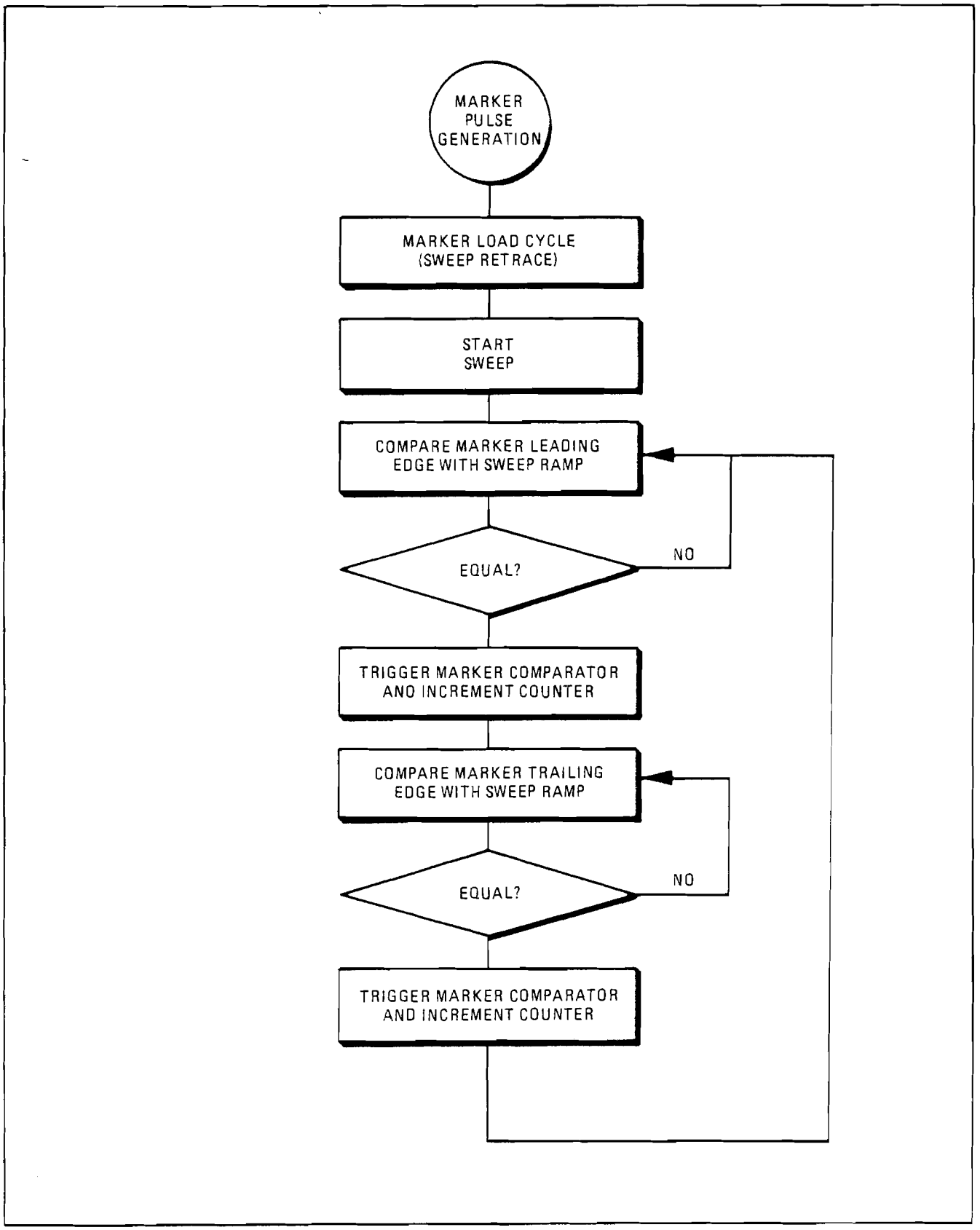


Figure 8-31. Marker Pulse Generation, Flow Diagram

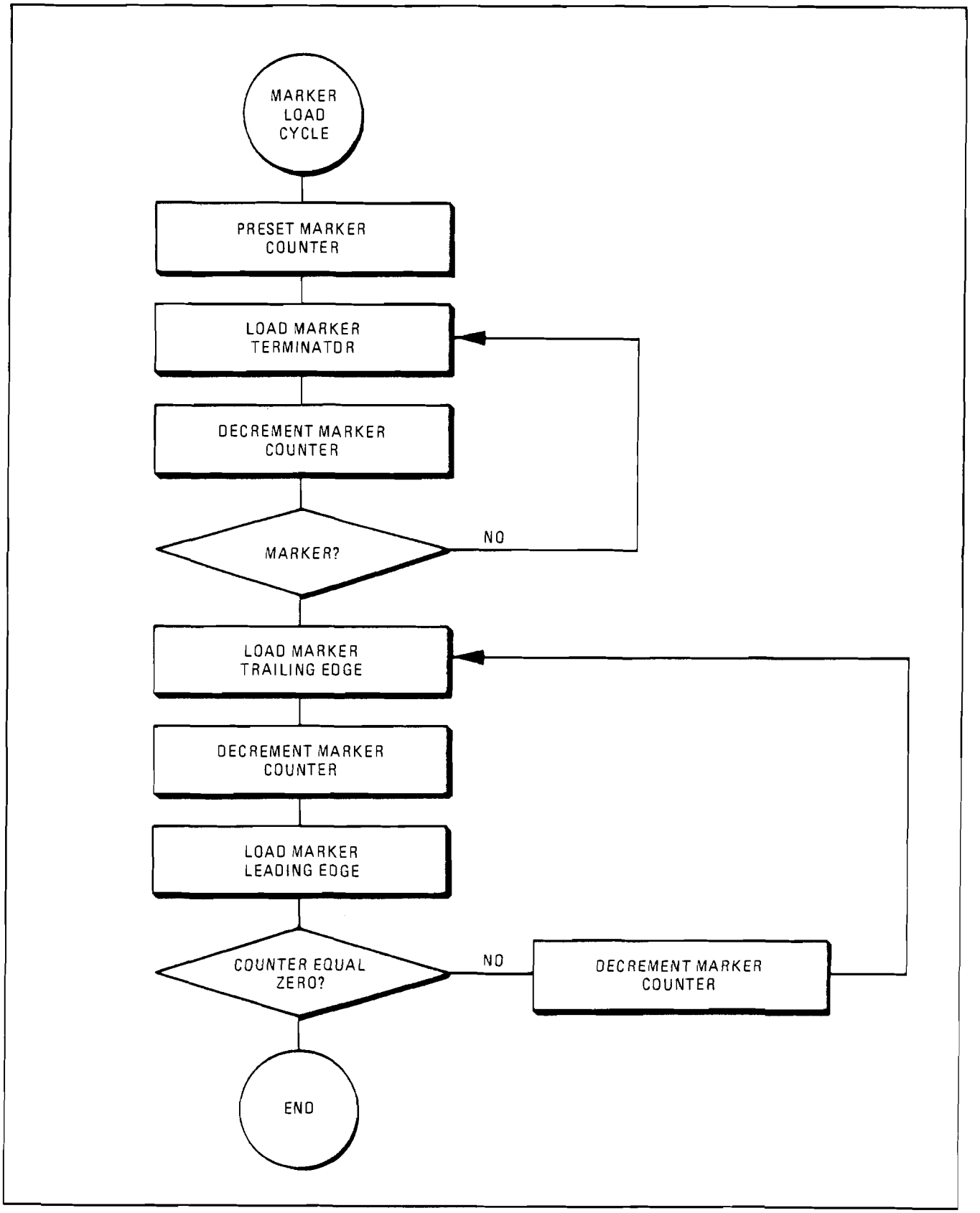


Figure 8-32. Marker Load Cycle, Flow Diagram

Microprocessor writes on the Instrument Bus data lines D0 through D7 the value of marker trailing edge for the highest frequency marker. LEN7 is set low and this value is stored in RAM location nine. The Marker Counter output is decremented by one, and the microprocessor writes the leading edge of the highest frequency marker into RAM location eight. The cycle continues until the trailing and leading edges for all five markers are loaded into RAM. The microprocessor then presets the Marker Counter to zero for the start of sweep. Refer to Table 8-24 for the RAM loading diagram.

Marker Pulse Generation. Marker DAC U12 operates as a current sink with the maximum current limit determined by the +10V V_{REF} input. The output current is scaled by the data loaded. $+10V_{REF}$ is connected through R45, R27, and R28 to the $+V_{REF}$ input of U12. Since the Marker Counter is preset to zero, the resultant current at the DAC output is equivalent to the leading edge of the lowest frequency marker.

This signal is compared to the current developed by VRAMP across R31 and R46 at the inverting input of comparator U11. When the value at U11 pin 3 crosses zero, U11 pin 7 switches low. C36 delays VRAMP to equalize the delay of the sweep ramp generated in the ΔF Generation circuit. CR5 and CR4 are protection diodes for U11. C41 and R32 provide ac hysteresis to ensure a clean rapid transition from comparator U11.

A negative transition at U11 pin 7 triggers monostable multivibrator U19B. It's output (a ten microsecond pulse determined by R48 and C42) appears at TP17 and clocks U24A pin 6 low. This is the beginning of the marker pulse L MK. The inverted output of U19B is used to trigger U19A. The output from U19A (a one microsecond pulse determined by R33 and C18) is buffered through U27A and fed back to increment the marker counter U21.

With the counter output incremented by one, the RAM address is incremented, and the data byte corresponding to the marker trailing edge for the lowest frequency marker is output by the Marker RAM. The DAC is programmed to the new value, which is greater in value than the marker leading edge value, resulting in comparator U11 being reset. The output of the DAC is compared to the current developed by VRAMP at the inverting input of comparator U11. When the value at U11 pin 3 again crosses zero, U11 output switches low. This causes U19B to trigger again, and its output at TP17 clocks U24A. The L MK output of U24A goes high ending the marker pulse. The inverted output of U19B triggers U19A again and its output is fed back to increment the Marker Counter again, which increments the Marker RAM address. This address contains the data byte corresponding to the leading edge of the next marker.

This cycle continues through all five markers. After the fifth marker pulse is generated, the marker counter is set to the hexadecimal value A. The RAM is set to hexadecimal address A which contains the marker terminator byte. This terminator byte programs the Marker DAC to sink more current than can be provided from VRAMP. The input to comparator U11 can not cross zero. This ensures that no more marker pulses are generated.

The marker RAM is loaded with values for five markers during every sweep retrace. If fewer than five markers are selected on the front panel, the values loaded into RAM for the unused markers is the same value as the marker terminator byte. Therefore marker pulses are only generated for each selected marker. The Marker Counter is reset to zero at the start of each sweep.

During retrace, LBP2 (Low=Blanking Pulse 2) is buffered through U27D and disables the marker pulse components U19A and B, U24A and B. During CW operation L MKR DISABLE is buffered through U27D and disables the marker pulse circuit. This ensures that no marker pulses are generated during retrace, CW operation or manual sweep.

Active Marker. The active marker is determined as follows. During retrace, LEN3 clocks the active marker leading edge Marker RAM address into data latch U17B. During the sweep, comparator U22 compares the Marker Counter output with the active marker address latched in U17B. When the two values are equal, the U22 output goes high. When U24B is clocked for the marker leading edge the Low Active Marker (L AMK) output goes low. When the Marker Counter is incremented, the U22 output goes low. Therefore, when U24B is clocked for the marker trailing edge, the L AMK output returns high. Refer to Figure 8-37 for timing relationship.

MarkerΔMode. When Marker Δ is selected on the front panel, one intensity or amplitude marker is extended between the last two markers entered. The Marker Δ mode is strictly a function of data loaded in Marker Ram, and operation of the Marker circuits is identical to normal marker operation.

Troubleshooting

Component failures on the A4 Scaling and Marker Assembly may be classified as either an Instrument Bus failure, a Scaling failure, a Marker failure, or a Power Supply failure. If upon instrument preset, error codes E005, E003, or E002 occur, a failed component may exist on this assembly. There are a total of seven self-tests available specifically for troubleshooting the A4 Scaling and Marker assembly. Two of these tests (Tuning Voltage versus Marker, and Sweep versus Marker) are functional checks that are performed at initial power on or whenever INSTR PRESET is pressed. Since these checks only check basic operation (not accuracy), the A4 Scaling and Marker assembly may have a component failure without generating an error code. Five operator initiated tests are available for checking the operation of each DAC circuit. By using the the Hex Data Write feature of the 8350A, each DAC may also be individually addressed and loaded from the front panel, and monitored with an oscilloscope. The following troubleshooting information is organized by symptoms (error code or type of failure), with an explanation of applicable self tests and waveforms.

Error Code E005

Instrument Bus Test. Correct Instrument Bus operation is checked during the Instrument Preset self tests. If the front panel INSTR PRESET is pressed and error code E004 or lower occurs, Instrument Bus operation is verified. If E005 occurs, perform an Instrument Preset self test with the A4 Scaling and Marker assembly removed. (This removes the possibility of A4 causing an Instrument Bus error code.) If E005 still occurs, refer to the General Troubleshooting section with the Overall Troubleshooting Block diagram to isolate the problem to the assembly level.

If, upon removal of A4, E003 occurs after Instrument Preset, reinstall the A4 Scaling and Marker Assembly. Press INSTR PRESET. If E005 reoccurs, the trouble is with A4U25 or A4U26. Set the 8350A into the repetitive Instrument Bus Self Test by pressing SHIFT 0 9, and checking the data, address and control inputs for activity, adjacent shorts and excessive loading.

Error Code E003

Tuning Voltage vs. Marker Test. This test is performed upon Instrument Preset, and compares the output of the summing amplifier against the output of the Marker DAC; when both outputs are equal, a Marker Flag (L MFLG) is generated and sent to the A3 Microprocessor.

The CW DAC is programmed so that its output at TP8 is −5 volts. The ΔF DAC is programmed so that its output at TP6 is a 0 to +5V rectangular waveform. The two signals are summed by Summing Amplifier U4 with the resultant +2.5V to +5V square wave at TP11. Self Test switch U8D is closed to supply the VTUNE signal to the inverting input of marker comparator U11.

Marker counter U21 is sequentially decremented via LEN7 thereby addressing different Marker RAM locations. The RAM is loaded with different values by the A3 Microprocessor. The RAM output programs Marker DAC U12. The Marker DAC output is summed with VTUNE at the inverting input of Marker Comparator U11. When the combined values of VTUNE and Marker DAC output cross zero, the U11 output at TP15 switches low. The pulse is buffered through U27B and sent to the A3 Microprocessor as LMFLG (Low=Marker Flag). Note that the marker outputs LMK and LAMK are disabled by L MARKER DISABLE at the U27D pin 13 input.

If error code E003 occurs, a problem exists on either the A5 Sweep Generator Assembly, or in the CW,CF Generation, ΔF Generation, Summing Amplifier, Self Test, Marker, or +10 Volt Reference circuits. Set the 8350A into the Tuning Voltage vs Marker repetitive self test by keying SHIFT 1 0. Verify the +10 Volt Reference supply at TP14. Verify that TP1 is at 0V. If TP1 is in error, a problem exists on the A5 Sweep Generator Assembly. Refer to the troubleshooting procedure for the A5 assembly. Check waveforms at TP11, TP12 and TP15 according to Figure 8-36. If a waveform is incorrect, proceed as follows:

- TP11: Perform ΔF DAC and CW, CF DAC self tests.
- TP12: Verify switch U8D is closed, then proceed to Marker circuit troubleshooting.
- TP15: Trouble is with Marker Comparator.

Error Code E002

Sweep versus Marker Test. This test is performed upon Instrument Preset, and compares the Sweep voltage (VRAMP) from the A5 Sweep Generator Assembly against the output of the Marker DAC; when both signals are equal, a Marker Flag is generated and sent to the A3 Microprocessor.

The Sweep DAC on the A5 Sweep Generator is programmed for a delayed stepped output, which can be monitored at A4TP13 (VRAMP). This signal is applied through R31 and R46 to the inverting input of Marker Comparator U11.

Marker circuit operation is identical with the operation in the Tuning Voltage versus Marker self test, and, if it functions properly in this previous test, should not cause an error code.

If error code E002 occurs, a failure exists either in the A5 Sweep Generator or Self Test switch U8D on this assembly. Check Self Test switch U8D is open, and verify waveform at A4TP13. If waveform at A4TP13 is incorrect, refer to the trouble-shooting procedure for the A5 Sweep Generator.

Scaling Failure

Provided the Instrument Bus is operational, a scaling failure is limited to one of the following circuits:

- CW, CF Generation Ⓒ
- Vernier Ⓕ
- ΔF Generation Ⓘ
- Summing Amplifier Ⓜ

Basic operation of the CW, CF generation, ΔF, and Summing Amplifier circuits is checked during Instrument Preset, but not all failures in these circuits may be detected. Separate Self Tests exist for each of the scaling DACs. A description of each self test follows.

CW, CF Generation.

CW DAC SHIFT 1 3. Correct operation of the CW, CF Generation circuit is verified by implementing the CW DAC repetitive self test SHIFT 1 3. This self test writes a rotating "one" to CW DAC U9. This rotating "one" is a single high bit that is rotated from the least significant to the most significant bit with the remaining bits loaded as zeros. Check for missing bits in the stepped waveform at TP8. (See Figure 8-36.)

Vernier.

VERNIER DAC SHIFT 1 9. This self test writes a rotating one to Vernier DAC U10, and results in a stepped waveform at TP11. (See Figure 8-36.) Increased amplitude is obtained by shorting TP9 to TP10.

ΔF Generation.

Sweep versus ΔF DAC SHIFT 1 5. This self test writes a rotating one from the least significant to most significant bit of the ΔF DAC U7. VSW1 is applied as a 0 to +10V square wave. This results in the symmetrical stepped waveform at TP3.

The Sweep vs ΔF DAC self test can be utilized to verify performance of operational amplifier U6, data latches U13 and U14, DAC U7, and operational amplifier U1 in the ΔF circuitry. To implement the self test press SHIFT 1 5 and check for waveforms indicated in Figure 8-36.

ΔF DAC SHIFT 1 4. This self test writes a rotating one from the least significant to most significant bit of ΔF DAC U7. VSW1 (TP1) is held to a constant +10 volts. This results in the stepped waveform at TP3 (See Figure 8-36).

Once proper data latch operation has been confirmed, switches U8A, B, and C, and operational amplifier U2 can be tested. Each switch is enabled separately and the output of U2 is monitored. To test these components, perform the following key strokes:

NOTE

All data entries are in hexadecimal. For hexadecimal values A through F, the key entry shown is the actual key label (i.e. BKSP equals hexadecimal F).

SHIFT 0 0	Access to HEX Address Entry Self Test
MI 3 0 0 3	Addresses data latch U13
M2 BKSP BKSP	Enters hex FF into data latch U13
MI 3 0 0 4	Addresses data latch U14
M2 0 7	Writes ones into the two most significant digits of U7 and enables switch U8A. The output of U2 at TP6 will be a +10V to −10V clamped ramp.
M2 0 —	Writes ones into the two most significant digits of U7 and enables switch U8C. The output of U2 at TP6 will be a +1.2V to −1.2V clamped ramp.
M2 1 3	Writes ones into the two most significant digits of U7 and enables switch U8B. The output of U2 at TP6 will be a +0.15V to −0.15V clamped ramp.

Summing Amplifier

Provided the three scaling DACs are operational, the Summing Amplifier can be checked as follows:

- Remove RF plug-in from 8350A
- Set line switch ON (8350A should cycle through self tests and indicate E001, RF Plug-in error code)
- Monitor A4TP11. Verify the output of operational amplifier U4 is a 0V to +10V clamped ramp.

Self Test

Provided the three scaling DACs and summing amplifier are operational, Self test switch U8D can be verified.U8D is enabled when U14 pin 15 is high. To test U8D perform the following key strokes:

NOTE

All data entries are in hexadecimal. For hexadecimal values A through F, the key entry shown is the actual key label (i.e. BKSP equals hexadecimal F).

SHIFT 0 0	Access to HEX Address Entry Self Test
M1 3 0 0 1	Addresses data latch U15
M2 BKSP BKSP	Enters hex ØF into data latch U17A
M1 3 0 0 2	Addresses data latch U17A
M2 0 BKSP	Enters hex F into data latch U17A
M1 3 0 0 3	Addresses data latch U13
M2 BKSP BKSP	Enters hex FF into data latch U13
M1 3 0 0 4	Addresses data latch U14
M2 2 7	Writes ones into the two most significant digits of U7, enables switch U8A, and enables switch U8D. Monitor TP12 to obtain waveform located in Figure 8-33.

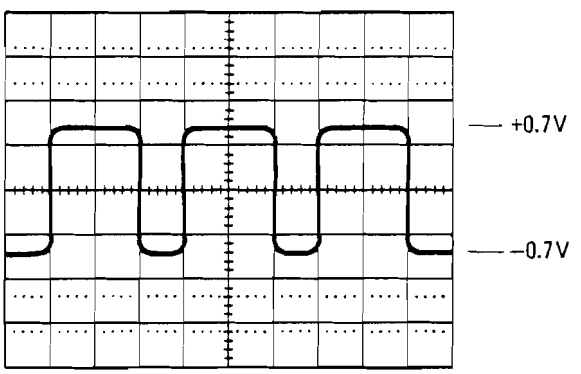


Figure 8-33. Self-Test Waveform

Marker Circuits

NOTE

TP13 must be grounded to obtain valid waveforms for Marker DAC self test SHIFT 1 6.

Marker DAC SHIFT 1 6. This test verifies the operation of Marker Counter U21, Marker RAMs U18 and U23, and the Marker DAC U12. The Marker Counter U21 is incremented sequentially, therefore addressing the different marker RAM locations of U18 and U23. A rotating one is loaded into the RAM locations. Therefore the Marker DAC output at TP12 is a stepped response.

Tuning Voltage versus Marker SHIFT 1 0. Operation of the Marker circuits can be verified by initiating the Tuning Voltage vs Marker DAC repetitive self test, SHIFT 1 0. This test checks the performance of Marker Counter U21, Marker RAMs U18 and U23, Marker DAC U12, Marker Comparator U11, and Marker Flag buffer U27B. To initiate the test, press SHIFT 1 0 and check for waveforms in Figure 8-36.

The Marker Pulse Generator and Active Marker Comparator circuit can be verified using specific front panel settings. Provided that U21, U18, U23, U12, U11, the front panel, the front panel bus and instrument bus are operational, the following instrument set up will test the Marker Pulse Generator and Active Marker Comparator circuits.

INSTR PRESET

M1 1 GHz	Initiates marker M1
M2 2 GHz	Initiates Marker M2
M3 3 GHz	Initiates Marker M3
M4 4 GHz	Initiates Marker M4
M5 5 GHz	Initiates Marker M5 (Must be entered last to be the active marker)

NOTE

In Figure 8-37, marker M5 is the active marker (last marker entered).

Verify the waveforms located in Figure 8-37.

P/O MICROPROCESSOR

P1 — XA3A

ID0 → 28
ID1 → 29
ID2 → 30
ID3 → 31
ID4 → 32
ID5 → 33
ID6 → 34
ID7 → 35

P2 — XA3B

I/OE3 → 24
L IRD → 39
L I/O STB → 37
L IA0 → 18
L IA1 → 41
L IA2 → 19
L IA3 → 42
L IA4 → 20

P/O INSTRUMENT BUS

XA4A — P1

6 → ID0
28 → ID1
7 → ID2
29 → ID3
8 → ID4
30 → ID5
9 → ID6
31 → ID7

XA4B — P2

3 → I/OE3
XA4A 37 → P1 L IRD
13 → L I/O STB
16 → L IA0
39 → L IA1
47 → L IA2
40 → L IA3
18 → L IA4

A4 SCALING AND MARKER ASSEMBLY

Ⓐ DATA BUFFER

ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7

Ⓑ ADDRESS DECODER

I/OE3 L IRD L I/O STB L IA0 L IA1 L IA2 L IA3 L IA4

SCALING

Ⓒ CW, CF GENERATION

LATCH — DAC (DATA, OUT, REF) — TP8 CW

L EN2 3001H, L EN3 3002H, +10V REF

Ⓔ VERNIER

LATCH — DAC (DATA, OUT, REF) — TP9 VERN

L EN1 3000H, +10V REF

Ⓓ △F GENERATION

LATCH — DAC (DATA, OUT, REF) — TP3, TP6 △F

L EN4 3003H, L EN5 3004H, VSW1

SELF TEST ENABLE

Ⓕ SUMMING AMPLIFIER

Σ, −, + — TP11 — VTUNE

Ⓘ S

MARKER

Ⓗ MARKER COUNTER AND ACTIVE MARKER COMPARATOR

COUNTER — COMPARATOR — ACTIVE MKR

L EN6 3005H, L EN7 3006H, +1, L EN3 3002H

Ⓚ MARKER RAM

RAM — EN1 (3000H), L EN7 3006H, DATA IN, DATA OUT, ADDRESS

Ⓛ MARK

DATA

AC

L

VR

P/O A5 SWEEP GENERATOR

A5P1 — XA5A — XA4A — P1

VSW1 → 21 → 21 → V SW1

A5P2 — XA5B — XA4B — P2

L BP2 → 11 → 33 → L BP2
V RAMP → A5P1 20 → XA5A 20 → XA4A 20 → P1 V RAMP

SCALING

TP8 CW

TP9 VERN

TP3

TP6 ΔF

F SUMMING AMPLIFIER

TP11

VTUNE

SELF TEST ENABLE

I SELF TEST

TEST

G +10V REFERENCE

TP14

+10V REF

+10V REF

P2

P/O A9 MOTHERBOARD

XA4B

XA5B

7, 29

A5 SWEEP GENERATOR

A5P2

+10V REF

J1

V TUNE

W3

J2

A1

RF PLUG-IN INTERCONNECT

MARKER

8

RATOR

COMPARATOR

ACTIVE MKR

L EN3 3002H

4

K MARKER RAM

RAM

3000H

EN1

L EN7 3006H

DATA IN

DATA OUT

ADDRESS

8

L MARKER DAC

DATA

OUT

ACTIVE MARKER

L BP2

VRAMP

J COMPARATOR AND MARKER PULSE GENERATOR

MARKER COMPARATOR

VTUNE

V RAMP

ACTIVE MARKER

L BP2

MARKER PULSE GENERATOR

TRIGGER

DISABLE

&

TP15

TP18

TP19

L MFLG

L MK

L AMK

P2

L MFLG

L MK

L AMK

11

6

27

P/O A9 MOTHERBOARD

XA4B

XA3

XA5

L MFLG

L MK

L AMK

31

6

27

P/O A3 MICROPROCESSOR

P2

L MFLG

P/O A5 SWEEP GENERATOR

P2

L MK

L AMK

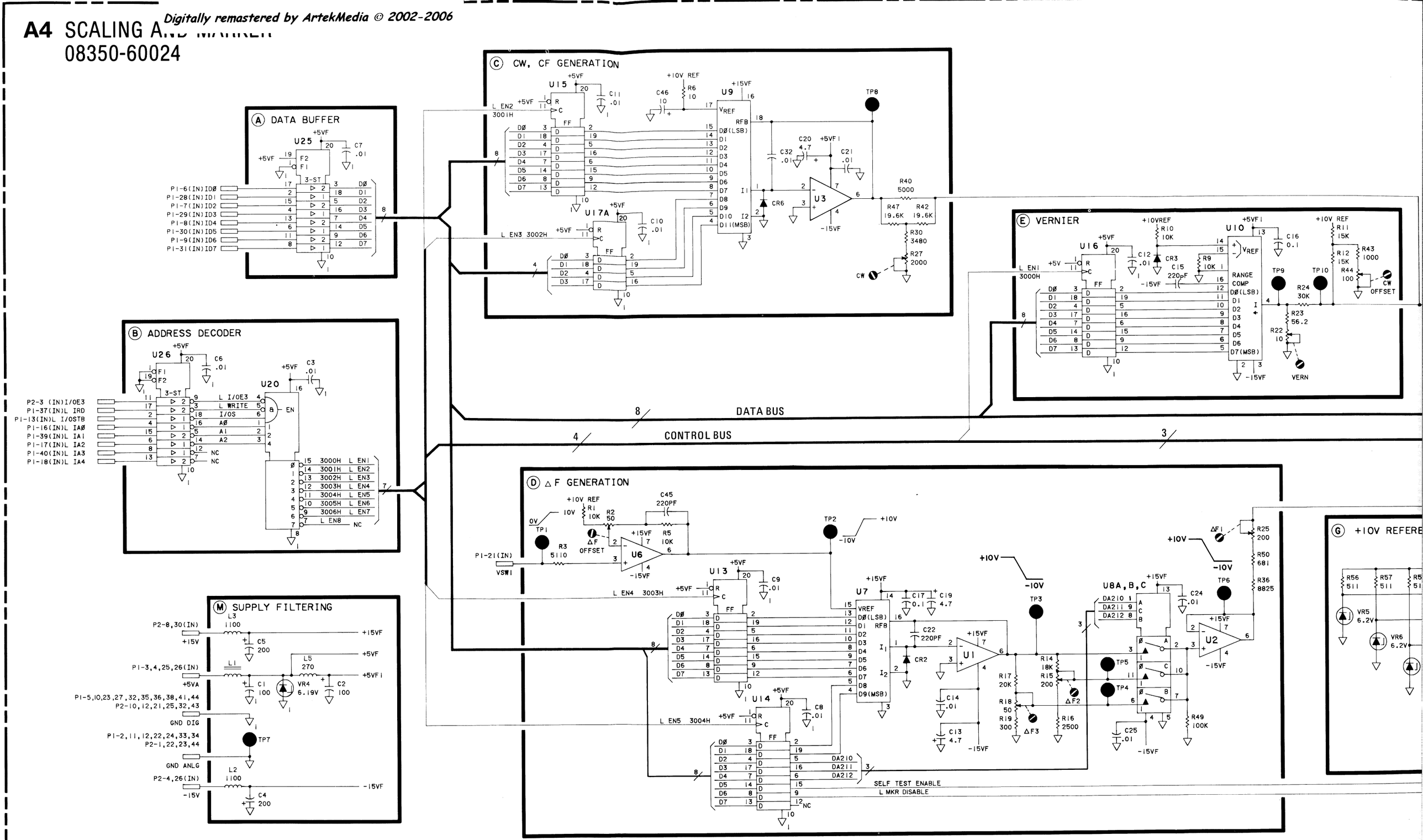
MARKER COUNTER ADVANCE

A4

Figure 8-34. A4 Scaling and Marker Assembly, Block Diagram

Figure 8-38. A4 Scaling and Marker Assembly, Schematic Diagram

A4 SCALING AND MARKER
08350-60024



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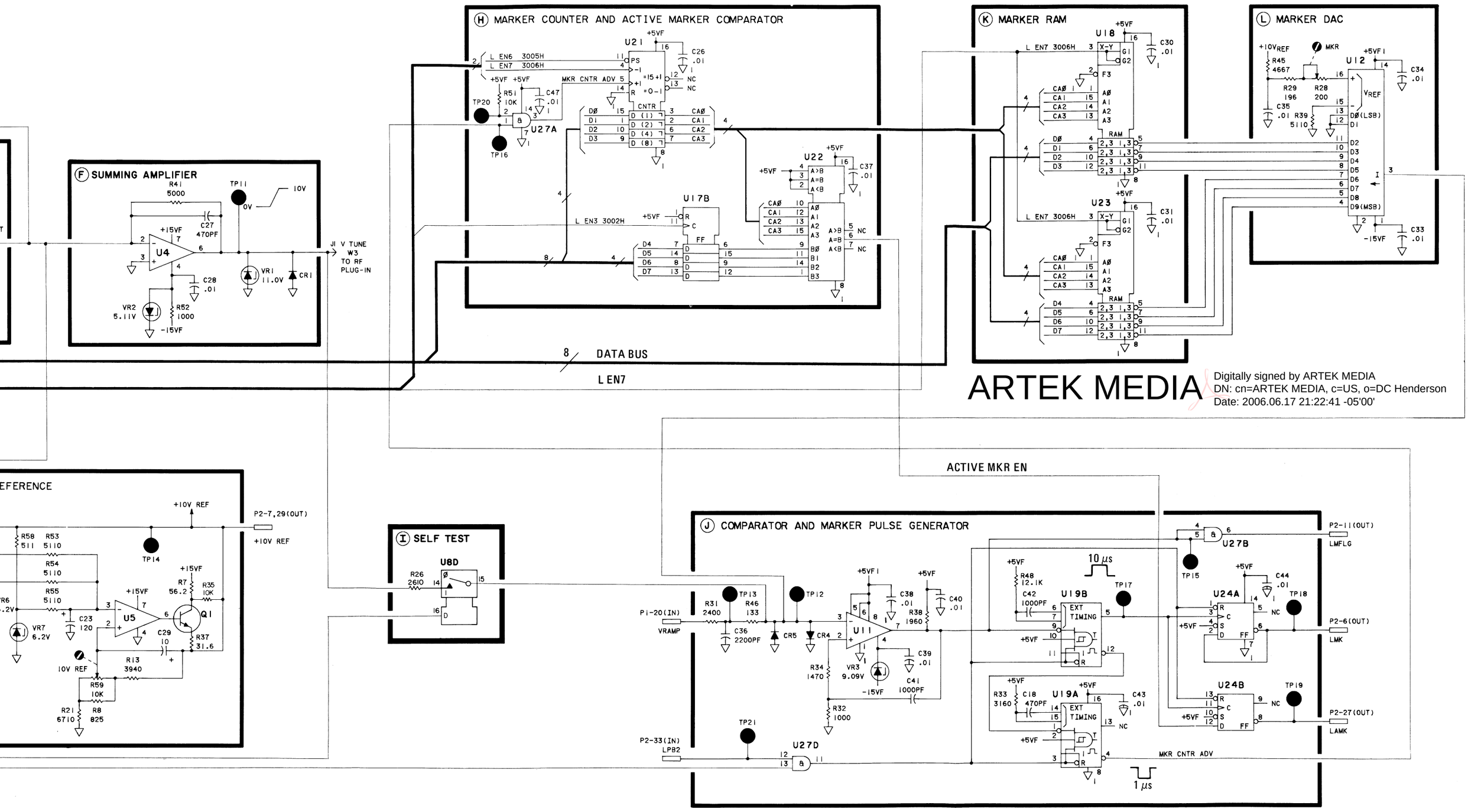

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Figure 8-38. A4 Scaling and Marker Assembly, Schematic Diagram

A5 SWEEP GENERATOR, CIRCUIT DESCRIPTION

The A5 Sweep Generator produces a 0V to +10V sweep ramp that is used primarily to tune the frequency of the RF Plug-in. The sweep ramp is also routed to the front and rear panels (sweep out) for driving the X axis of monitoring instruments. Another function of the Sweep Generator is to provide timing signals to external instruments. The timing signals are in respect to the start and end of the sweep ramp.

The sweep ramp is generated by supplying a constant but programmable current to the integrator. The integrator converts the constant current to a sweep ramp. The sweep ramp is limited by two comparators in the Sweep Trigger circuit. The reference voltages at the comparators are set for the upper ramp limit and the lower ramp limit. When the ramp voltage crosses these limits a retrace current source (Q3) is turned on or off. With this current source off, the ramp is a positive going ramp, and with it on, the ramp is a negative going ramp.

In the internal sweep trigger mode, the start of the sweep is triggered from the low ramp comparator. The start of the sweep can also be triggered from the ac line frequency, from an external signal or by the single trigger function.

The Ramp Generator actually produces a ramp that sweeps from −.95V to +10.8V in amplitude. This voltage is clamped by the Clamping circuit at 0 and +10V. The unclamped ramp is buffered and used by the sweep timing circuit. The 0 to +10V ramp is buffered and forms four outputs: VRAMP, VSW, VSW1, and VSW2.

Address Decoder Ⓐ

The A5 Sweep Generator uses address locations 2014H through 2017H. When the Instrument Bus contains an address for this assembly, 3-to-8 decoder U39 decodes the address to determine which device on the A5 assembly is being addressed by the A3 Microprocessor. Table 8-26 provides an index of the address decoding.

Data Bus Buffer Ⓑ

Data Bus Buffer U30 buffers the eight Instrument Bus data lines (ID0−ID7) going to the data latches in the Software Control circuit, and is always enabled. Data can only be written to the Software Control circuit.

Software Control Ⓒ

The Software Control circuit consists of four eight-bit latches (U1, U8, U16, and U24) that store control information generated by the A3 Microprocessor. Each latch is individually clocked by an enable line from the Address Decoder. Table 8-27 lists the control lines stored by the Software Control circuit. Note that some of these lines are wire ORed in the Sweep Ramp Generator with hardware generated control lines.

Table 8-26. A5 Sweep Generator Address Decoding

Address (Hexidecimal)	Address Decoder Components	Components Addressed	Read or Write	Description
2014	U31B, U33A, U39	U24	WRITE	Software Control
2015	U31B, U33A, U39	U16	WRITE	Software Control
2016	U31B, U33A, U39	U8	WRITE	Data Latch for lower 2 bits of U2 DAC and Software Control.
2017	U31B, U33A, U39	U1	WRITE	Data Latch for upper 8 bits of U2 DAC.

Table 8-27. Software Control Outputs

Mnemonic	Definition	Remarks	Destination
L ABORT	Low = Abort	Resets sweep ramp	E
L ALTE	Low = Alternate Sweep enable	Enable alternate sweep function	J13/J14
ALT1	Alternate Sweep 1	High indicates alternate sweep one is being generated.	J13/J14
L CLAMP DISABLE	Low = Clamp Disable	Disable sweep voltage ramp upper clamp.	F
CT1	Counter Trigger 1	Coded control line for determining counter trigger source.	I
CT2	Counter Trigger 2	Coded control line for determining counter trigger source.	I
DBPE	Display Blanking Pulse Enable	Enables BP1 onto LP1 control line.	K
L DISABLE TRIG	Low = Disable Trigger	Disable Sweep trigger circuit.	E
L EX SW	Low = External Sweep	1. Disables integrator (Holds at high level) 2. Switches External Sweep input into VSW Buffer (Disabling VSW thru buffer)	D F
L HPIB/TRIG	LOW=HP-IB Trigger	Trigger SYNC TRG control line.	K
INT/L AMP MK	Intensity/Low= Amplitude Marker	Level determines if Output Logic circuit produces Intensity or RF Marker trigger.	K
MANUAL	Manual Sweep	Changes integrator to a current-to-voltage buffer. Sets buffer gain.	D
L MANUAL	Low=Manual	Complement of MANUAL 1. Changes integrator buffer offset value. 2. Disables Sweep	D E
L RESET	Low=Reset	Disable 27 kHz/1kHz Oscillator	J
RFBE	RF Blanking Enable	Enable PL1 to control RF blanking	K
L SNGL	Low=Single Sweep	Single sweep trigger	E
L SSRQ	Low=Stop Sweep Request	Stops and holds sweep ramp voltage.	D
TM1	Trigger Mode 1	Coded control line for determining trigger source.	E
TM2	Trigger Mode 2	Coded control line for determining trigger source.	E
1ms–999ms		Selects 1 ms through 999ms sweep time range of integrator.	D
1s–100s		Selects 1s through 100s sweep time range of integrator.	

Sweep Ramp Generator Ⓓ

The Sweep Ramp Generator has four major sectio
source, the integrator, the stop sweep, and the ret

Programmable Current Source. The program
bit DAC (Digital-to-Analog Converter). The amou
the sweep time (slope) of the ramp. The maximum
the reference voltage input (V_{REF}) which is scaled b
from the Software Control circuit. The data is gene
and written to latches U1 and U8. Reference current
from the +10V reference supply through R4 and
second to 100 seconds) analog switch (U10D) close
to pin 16 of the DAC, and resulting in more current f
analog switch U9 selects C8 as the integrating capa
circuit. The amount of current, or sweep time, can be
and R25.

Integrator. The DAC current is applied to the in
operational amplifier U3, and charges either in
depending on the sweep time. For faster sweep tim
switched in through analog switch U9B (analog swi
the sweep ramp). The capacitor selected and the c
used to set the sweep time. Voltage divider R9, R
reference at U3 pin 3.

If the Sweep Ramp Generator is waiting for a star
single sweep or external sweep trigger), the retrace ci
output negative. Since the retrace circuit contin
integrator inverting input until the next sweep is trig
ensure the integrator never reverse biases the integ
tion is provided by CR2 and R8. As long as the int
than about −1.6V, CR2B is biased on, keeping CR2
the integrator output approaches −1.6V), CR2A
current from the integrator inverting input. CR2B
cathode bias. This results in both anode voltages tra
is flowing through R8, the integrator output is n
positive level than the integrator input.

Manual Sweep. For manual sweep, the integrat
and analog switch U17A connects R11, R43, and R
Analog switch U17D provides the output for the n
acts as a linear amplifier and the dc voltage out is a f
by the DAC.

Retrace. For retrace, the emitter of Q3 and paral
+5VF1 by analog switch U17B. This switch is ac
External Sweep), or PL1 (Pen Lift 1), and is disabled
Request). For internal sweep trigger mode the PL1
ramp reaches 10.8V and goes low when the ramp sw
voltage of Q3 is determined by the collector voltage
connected as a differential amplifier. Q1 senses t
Higher current through R5 results in a more nega
turning it on harder. The current through Q3 and
capacitor and also supplies current to the DAC; t
ramp or sweep down (retrace). The slope of the

8-27. Software Control Outputs

nition	Remarks	Destination
Abort	Resets sweep ramp	E
Alternate enable	Enable alternate sweep function	J13/J14
e Sweep 1	High indicates alternate sweep one is being generated.	J13/J14
Clamp	Disable sweep voltage ramp upper clamp.	F
Trigger 1	Coded control line for determining counter trigger source.	I
Trigger 2	Coded control line for determining counter trigger source.	I
Blanking Enable	Enables BP1 onto LP1 control line.	K
Disable	Disable Sweep trigger circuit.	E
External	1. Disables integrator (Holds at high level) 2. Switches External Sweep input into VSW Buffer (Disabling VSW thru buffer)	D F
P-IB Trigger	Trigger SYNC TRG control line.	K
y/Low= tude Marker	Level determines if Output Logic circuit produces Intensity or RF Marker trigger.	K
Sweep	Changes integrator to a current-to-voltage buffer. Sets buffer gain.	D
anual	Complement of MANUAL 1. Changes integrator buffer offset value. 2. Disables Sweep	D E
eset	Disable 27 kHz/1kHz Oscillator	J
nking Enable	Enable PL1 to control RF blanking	K
ngle Sweep	Single sweep trigger	E
op Sweep st	Stops and holds sweep ramp voltage.	D
Mode 1	Coded control line for determining trigger source.	E
Mode 2	Coded control line for determining trigger source.	E
	Selects 1 ms through 999ms sweep time range of integrator.	D
	Selects 1s through 100s sweep time range of integrator.	

Sweep Ramp Generator (D)

The Sweep Ramp Generator has four major sections. The programmable current source, the integrator, the stop sweep, and the retrace circuits.

Programmable Current Source. The programmable current source U2 is a 10-bit DAC (Digital-to-Analog Converter). The amount of DAC current determines the sweep time (slope) of the ramp. The maximum DAC current is determined by the reference voltage input (V_{REF}) which is scaled by the data lines D0 through D9 from the Software Control circuit. The data is generated by the A3 Microprocessor and written to latches U1 and U8. Reference current to the DAC is applied to pin 16 from the +10V reference supply through R4 and R2. For longer sweep times (1 second to 100 seconds) analog switch (U10D) closes, supplying additional current to pin 16 of the DAC, and resulting in more current from the DAC. At the same time, analog switch U9 selects C8 as the integrating capacitor and switches C7 out of the circuit. The amount of current, or sweep time, can be adjusted by potentiometers R2 and R25.

Integrator. The DAC current is applied to the inverting input of the integrating operational amplifier U3, and charges either integrating capacitor C7 or C8, depending on the sweep time. For faster sweep times (10 msec to 999 msec), C7 is switched in through analog switch U9B (analog switch U9C provides the output for the sweep ramp). The capacitor selected and the current from the DAC are both used to set the sweep time. Voltage divider R9, R10, and R66 provides a −1.6V reference at U3 pin 3.

If the Sweep Ramp Generator is waiting for a start sweep trigger (i.e. 8350A is in single sweep or external sweep trigger), the retrace circuit tries to drive the integrator output negative. Since the retrace circuit continues to supply current to the integrator inverting input until the next sweep is triggered, protection is required to ensure the integrator never reverse biases the integrating capacitors. This protection is provided by CR2 and R8. As long as the integrator output is more positive than about −1.6V, CR2B is biased on, keeping CR2A biased off. During retrace (as the integrator output approaches −1.6V), CR2A becomes biased on, shunting current from the integrator inverting input. CR2B remains biased on due to the cathode bias. This results in both anode voltages tracking each other. Since current is flowing through R8, the integrator output is maintained at a slightly more positive level than the integrator input.

Manual Sweep. For manual sweep, the integrating capacitors are switched out and analog switch U17A connects R11, R43, and R53 as feedback resistors for U3. Analog switch U17D provides the output for the manual sweep voltage. U3 now acts as a linear amplifier and the dc voltage out is a function of the current supplied by the DAC.

Retrace. For retrace, the emitter of Q3 and parallel resistor R40 are switched to +5VF1 by analog switch U17B. This switch is activated by L EX SW (Low = External Sweep), or PL1 (Pen Lift 1), and is disabled by L SSRQ (Low = Stop Sweep Request). For internal sweep trigger mode the PL1 line goes high when the sweep ramp reaches 10.8V and goes low when the ramp sweeps down to −0.95V. The base voltage of Q3 is determined by the collector voltage of Q1B. Q1 is a dual transistor connected as a differential amplifier. Q1 senses the DAC current through R5. Higher current through R5 results in a more negative voltage at the base of Q3 turning it on harder. The current through Q3 and R40 discharges the integrating capacitor and also supplies current to the DAC; this results in a negative going ramp or sweep down (retrace). The slope of the ramp, or sweep down time, is determined by the current through Q3 and the parallel resistor R40. Factory select resistor R70 compensates for differences in the gains or betas of Q1 and Q3, and the differences in the voltages produced by zener diode VR14. VR14 and R72 provide a constant voltage source at the emitters of Q1 independent of voltage variations in the −15V supply. For small DAC currents, the voltage drop across R5 decreases and both bases of Q1 become close to equal. The collector voltage of Q1B approaches the emitter voltage of Q3, turning it off, and current is supplied only through parallel resistor R40. Therefore, the retrace slope is a direct function of the forward sweep slope.

Stop Sweep. The sweep can be stopped by L SSRQ (Low = Stop Sweep Request) or L SFSR (Low = Stop Forward Sweep Request). These signals close analog switch U17C, reverse biasing diode CR8. Since the DAC current cannot flow through reverse biased CR8 to discharge the integrating capacitor, the sweep voltage is held constant and the sweep stopped. CR9 provides a path to ground for the DAC current. The L SSRQ and L SFSRQ functions are disabled for manual sweep by the L MANUAL line to U18D.

Sweep Trigger (E)

The Sweep Trigger PL1 output (Pen Lift 1) triggers the start of each sweep, and also triggers the sweep retrace when the sweep voltage reaches +10.8V. Two ramp limit comparators monitor the sweep voltage at TP13. The Low Ramp Limit comparator (U35) enables a sweep trigger when the sweep retrace reaches −0.95V. The High Ramp Limit comparator (U34) triggers a sweep retrace when the sweep voltage reaches +10.8V. One of four sweep trigger modes is selected by the TM1, TM2 control inputs to multiplexer U40 (see Table 8-28). The PL1 logic level is controlled by R-S flip-flop U41D when the internal trigger mode is selected, and by R-S flip-flop U41A for all other trigger modes.

High Ramp Limit. High Ramp Limit comparator U34 produces a logic low at TP14 whenever the sweep voltage at TP13 exceeds +10.8V. This logic low output sets R-S flip-flops U41A and U41D to latch the PL1 output high and initiate a sweep retrace. The +10.8V reference voltage for U34 is supplied by voltage divider R17, R30.

Low Ramp Limit. Low Ramp Limit comparator U35 produces a logic high whenever the sweep voltage at TP13 is more negative than −0.95V. This output resets R-S flip-flop U41D, and enables the sweep trigger selected by U40 to reset R-S flip-flop U41A resulting in a logic low on the PL1 output).

Internal Trigger. For internal trigger mode, the sweep up voltage is initiated immediately after the sweep retrace is completed. Multiplexer U40 disables timer U32B by selecting +5V as its trigger input (U32−9). U40B selects the U41D output to provide the PL1 control output to the Sweep Ramp Generator. When the sweep retrace voltage reaches −0.95V, Low Ramp Limit comparator U35 resets U41D, and produces a low PL1 output (initiating the sweep up ramp). A sweep retrace is initiated when the High Ramp Limit comparator senses the sweep voltage crossing +10.8V and sets U41D (resulting in a logic high on the PL1 output).

Line, EXT, Single, and Remote Sweep Trigger Modes. Multiplexer U40A selects one of three trigger inputs according to the status of its TM1, TM2 control inputs (see Table 8-28). A low on the selected trigger line sets the U32B timer output high for 40 microseconds. This output is gated through U26 by the Low Ramp Limit comparator so that R-S flip-flop U41A is reset by the trigger only when the Sweep Ramp Generator is waiting to start a new sweep. The High Ramp Limit comparator

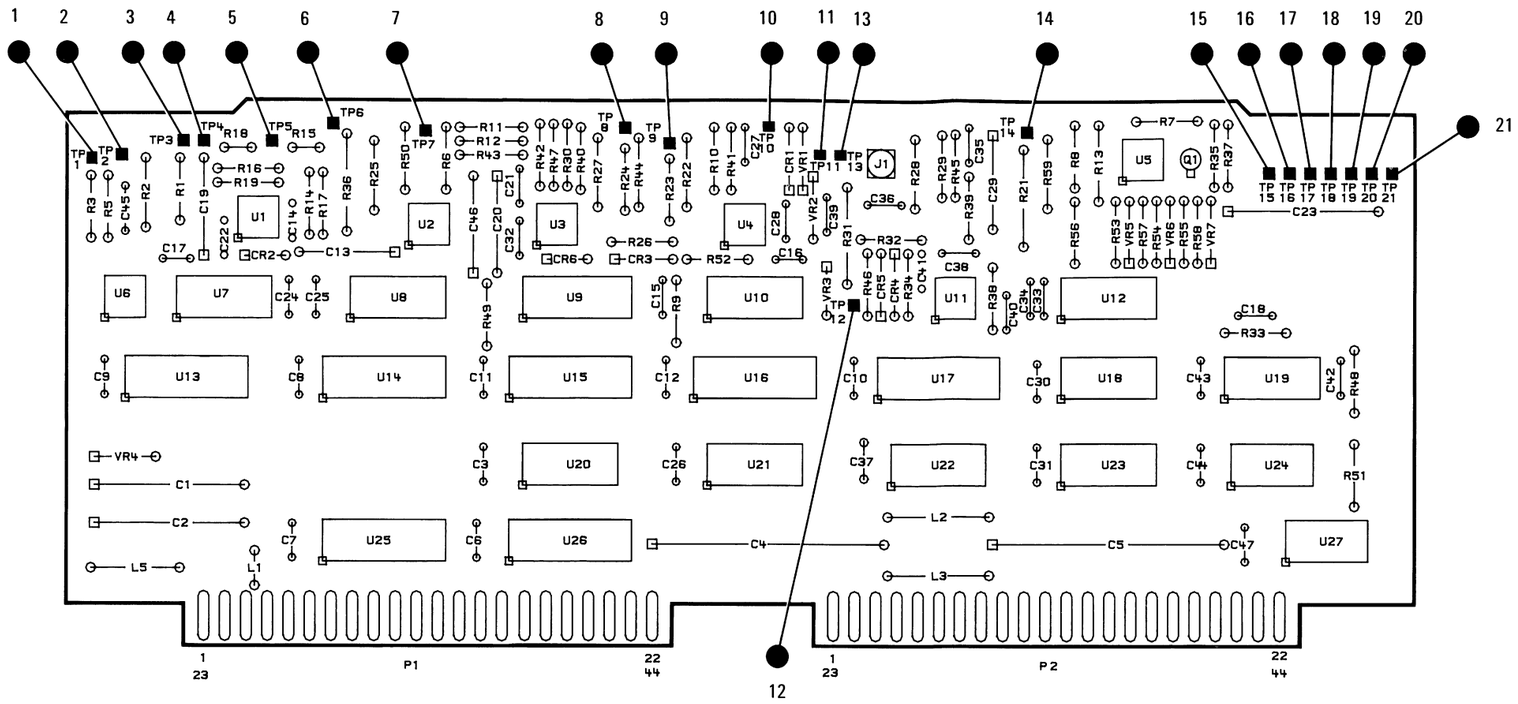


Figure 8-35. A4 Scaling and Marker Assembly, Component Locations

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◂▸ TO STEP TO THE NEW ADDRESS.

2. WAVEFORMS SHOWN ON THE SCHEMATIC ARE FOR INSTRUMENT PRESET CONDITIONS AND NO RF PLUG-IN INSTALLED.

A4P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	GND DIG GND DIG			M M
2 24	GND ANLG GND ANLG			M M
3 25	+5VA +5VA	IN IN	A7P1-2, 24 A7P1-2, 24	M M
4 26	+5VA +5VA	IN IN	A7P1-2, 24 A7P1-2, 24	M M
5 27	GND DIG GND DIG			M M
6 28	ID0 ID1	IN IN	A3P1-28 A3P1-29	A A
7 29	ID2 ID3	IN IN	A3P1-30 A3P1-31	A A
8 30	ID4 ID5	IN IN	A3P1-32 A3P1-33	A A
9 31	ID6 ID7	IN IN	A3P1-34 A3P1-35	A A
10 32	GND DIG GND DIG			M M
11 33	GND ANLG GND ANLG			M M
12 34	GND ANLG GND ANLG			M M
13 35	L I/OSTB GND DIG	IN	A3P1-37	B M
14 36	I/OE2 GND DIG	IN	A3P1-16	NOT USED M
15 37	I/OE1 L IRD	IN IN	A3P1-17 A3P1-39	NOT USED B
16 38	L IA0 GND DIG	IN	A3P1-18	B M
17 39	L IA2 L IA1	IN IN	A3P1-19 A3P1-41	B B
18 40	L IA4 L IA3	IN IN	A3P1-20 A3P1-42	B B
19 41	N.C. GND DIG			 M
20 42	VRAMP N.C.	IN	A5P1-20	J
21 43	VSW1 N.C.	IN	A5P1-20	D
22 44	GND ANLG GND DIG			M M

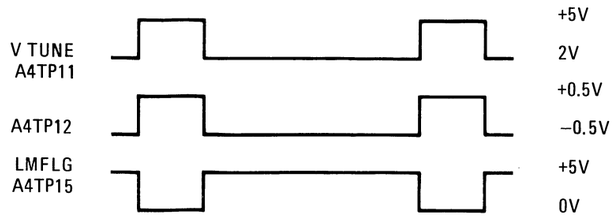
A4P2

PIN	SIGNAL
1 23	GND ANLG GND ANLG
2 24	N.C. N.C.
3 25	I/OE3 GND DIG
4 26	−15V −15V
5 27	N.C. L AMK
6 28	L MK N.C.
7 29	+10V REF +10V REF
8 30	+15V +15V
9 31	L I/OCLK GND DIG
10 32	GND DIG GND DIG
11 33	L MFLG L BP2
12 34	GND DIG N.C.
13 35	N.C. N.C.
14 36	N.C. N.C.
15 37	N.C. N.C.
16 38	N.C. N.C.
17 39	N.C. N.C.
18 40	N.C. N.C.
19 41	N.C. N.C.
20 42	N.C. N.C.
21 43	GND DIG GND DIG
22 44	GND ANLG GND ANLG

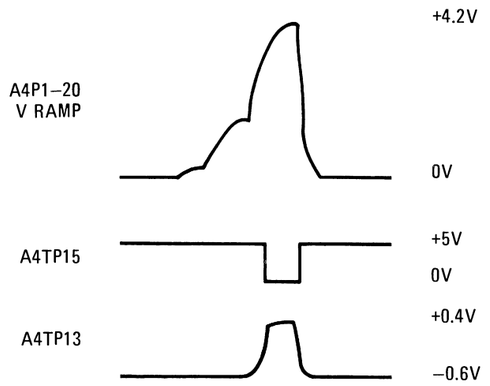
GNAL	I/O	TO/FROM	FUNCTION
ANLG			M
ANLG			M
I.C.			
I.C.			
OE3	IN	A3P2-24	B
D DIG			M
15V	IN	A7P1-14, 36	M
15V	IN	A7P1-14, 36	M
I.C.			
AMK	OUT	A5P2-27	J
MK	OUT	A5P2-6	J
I.C.			
V REF	OUT	A5P2-7, 29	G
V REF	OUT	A5P2-7, 29	G
15V	IN	A7P1-8, 30	M
15V	IN	A7P1-8, 30	M
OCLK	IN	A3P2-29	NOT USED
D DIG			M
D DIG			M
D DIG			M
IFLG	OUT	A3P2-31	J
BP2	IN	A5P2-11	J
D DIG			M
.C.			
.C.			
.C.			
.C.			
.C.			
.C.			
.C.			
.C.			
.C.			
D DIG			M
D DIG			M
ANLG			M
ANLG			M

TESTS

TUNING VOLTAGE VS. MARKER SHIFT 10

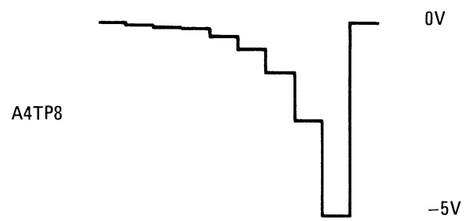


SWEEP VS. MARKER SHIFT 11

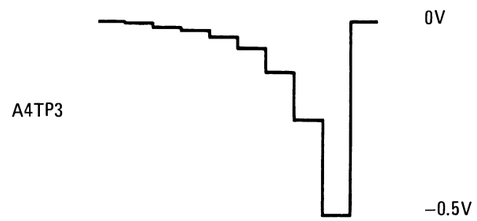


SCALING DAC SELF TESTS

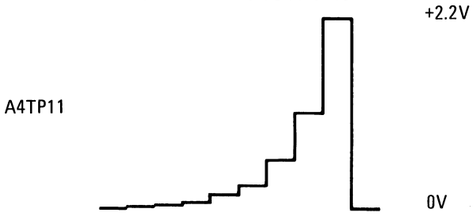
CW DAC SHIFT 13



△F DAC SHIFT 14



VERNIER DAC SHIFT 19
JUMPER A4TP9 TO A4TP10



SWEEP VS. △F DAC SHIFT 15

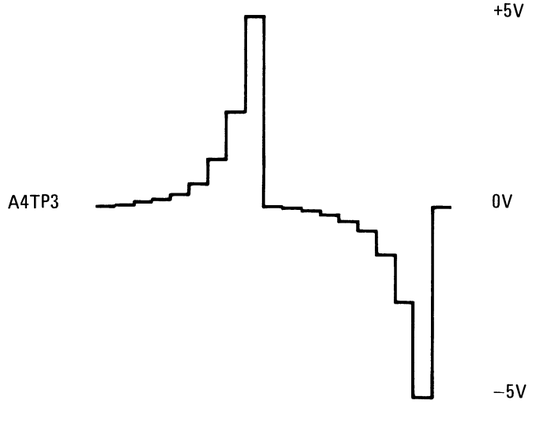
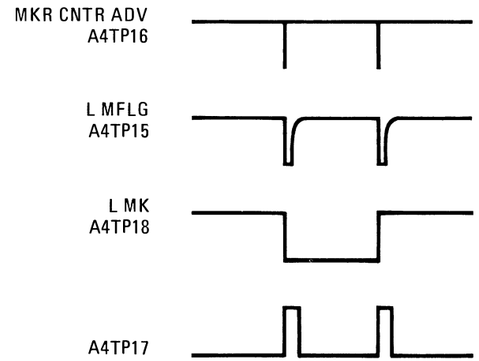


Figure 8-36. Operator Initiated Self Tests

MARKER PULSE GENERATION



MARKER TIMING DIAGRAM
(NO RF PLUG-IN INSTALLED)

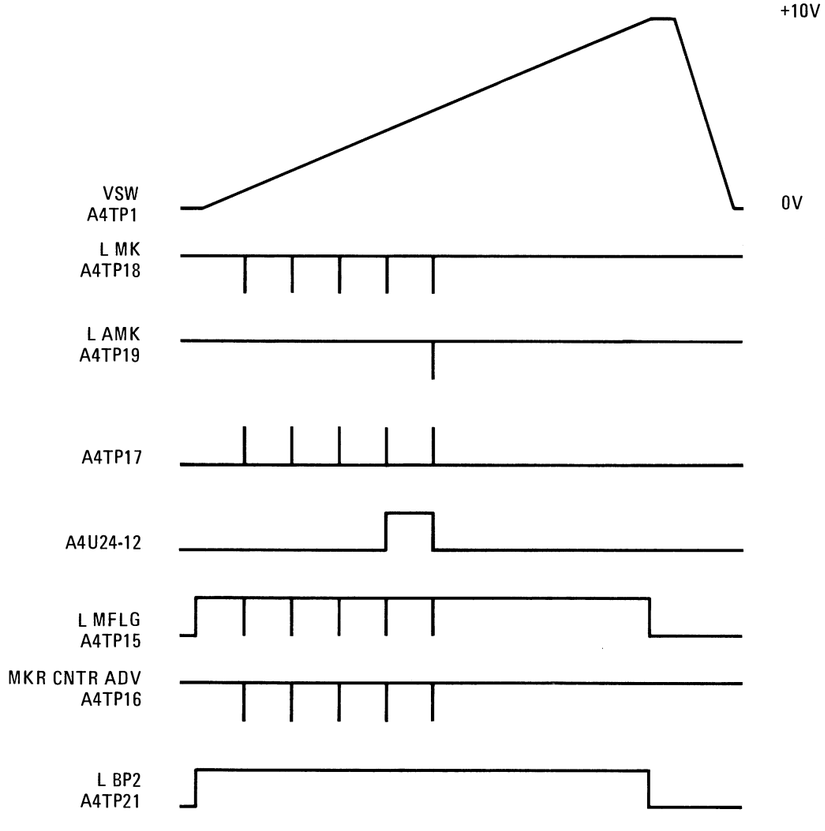


Figure 8-37. Marker Timing Diagrams

sets the U41A output low when the sweep voltage reaches +10.8V. U41A is also set by L ABORT (U26B−6) if the front panel SINGLE key is pressed during a sweep.

Clamping (F)

The Clamping circuit limits the sweep voltage at 0V and +10V. The sweep voltage (−0.95V to +10.8V) from the integrator is buffered through voltage follower U12, and applied through the clamp diodes (CR12A/B) to the inverting input of U19A.

Low Ramp Clamp. With the sweep voltage at the low end (−0.95V), CR12A is forward biased by current from Q5B. Both CR12 anodes are at −.35V, which reverse biases CR12B. No current flows through R65 or R63, therefore the voltage at that junction is 0V. It remains 0V until CR12B is forward biased, allowing current to flow through R65. CR12B becomes forward biased when the sweep voltage reaches 0V. After CR12B starts to conduct, the voltage at its cathode follows the sweep voltage from U12 pin 6.

High Ramp Clamp. CR4 clamps the sweep voltage at +10V. A +10V reference voltage is applied to the noninverting input of U19A. When the sweep voltage applied to U19A pin 2 passes through +10V, U19A (which has been saturated positive) changes states, and tries to saturate negative. However, diode CR4 (which is feedback for U19A) starts to conduct, holding the sweep voltage at pin 2 equal to the +10V reference voltage at pin 3.

The high ramp clamp can be disabled,by an active low L CLAMP DISABLE input to the base of Q4. With Q4 off, CR6 is forward biased through R46 to the +15V supply. R46 and R14 now form a voltage divider to set U19A pin 3 at 10.9V. The sweep voltage never exceeds 10.8V. Therefore U19A is always saturated positive and CR4 is never forward biased.

Sweep Voltage Buffers (G)

The clamped 0V to 10V sweep voltage from the Clamping circuit is buffered by voltage followers U11, U13, U4, and U5. The output of U11 is VRAMP, which is used in the marker circuit on the A4 Scaling and Marker assembly.

When analog switches U10A and U10C are closed by a logic high on the L EXT SW line (Low = External Sweep), the front and rear panel sweep output voltage (VSW2) is provided by U13. The output of U13 also goes to U4 and U5. The U4 output (VSW1) is used by the ΔF DAC on the A4 assembly. The U5 output (VSW) is used in the RF Plug-in.

When the L EX SW line is low, analog switches U10A and U10C are open to allow the sweep out/in from the front and rear panels to become the inputs to U4 and U5. VR5 and VR6 are protection diodes.

NOTE

The A5 Circuit Description and Troubleshooting information pertaining to the circuits on sheet 2 of the schematic are located on the back of sheet 1.

TROUBLESHOOTING

Component failures on the A5 Sweep Generator may affect the sweep voltage outputs (VSW, VSW1, VSW2, and VRAMP), blanking, sweep related timing, the counter interface, or the squarewave modulation. Since the RF Plug-in can control operation of the A5 Sweep Generator, initial troubleshooting should be without the RF Plug-in installed. Once the A5 operation is verified without the RF Plug-in, troubleshooting can be limited to the interfacing circuits between the RF Plug-in and the A5 Sweep Generator. If upon instrument preset, error codes E005, E003, or E002 occur, a failed component may exist on this assembly. Operation of the A5 Sweep generator can be checked through the use of the Instrument Preset self tests, available operator initiated self tests, and troubleshooting procedures provided. The following troubleshooting information is organized by symptom (error code or type of failure) with an explanation of applicable self tests, and waveforms.

Error Code 005

Instrument Bus Test. Correct Instrument Bus operation is checked during the Instrument Preset self tests. If the front panel INSTR PRESET key is pressed and error code E004 or lower occurs, Instrument Bus operation is verified. If E005 occurs, perform an Instrument Preset self test with the A5 Sweep Generator removed. This removes the possibility of A5 causing an Instrument Bus error code. If E005 still occurs, refer to the General Troubleshooting section with the Overall Block diagram to isolate the problem to the assembly level.

If upon removal of A5, E002 occurs after Instrument preset, reinstall the A5 Sweep Generator. Press INSTR PRESET. If E005 reoccurs, the trouble is in the Data Buffer or Address decoder circuits. Set the 8350A into the repetitive Instrument Bus self test by pressing SHIFT 0 9, and checking the data, address, and control inputs for activity, adjacent shorts, and excessive loading.

Error Code E002

Sweep versus Marker Test. This test is performed upon Instrument Preset, and generates a 0V to +4.2V 3-stepped VRAMP output which is compared with the marker position on the A4 Scaling and Marker assembly. When the marker position and VRAMP are equal, the A4 assembly outputs a marker flag to the microprocessor. If the microprocessor does not receive the flag, error code E002 is generated.

Correct operation of A5 for this self test is verified by initiating a repetitive Sweep versus Marker self test (SHIFT 1 1) and checking for a 0V to +4.2V 3-stepped ramp at A5TP6 (See Figure 8−42.). If the waveform at A5TP6 is correct, refer to the A4 Scaling and Marker assembly service sheet for further troubleshooting.

The sweep voltage at TP6 generated for this test is the result of the Sweep Ramp Generator being controlled by the A3 Microprocessor through the Software control circuit. The Sweep Ramp Generator is set to manual sweep mode, the Stop Sweep and Retrace functions are off (A5TP3 and A5TP12 are 0V), and the integrator programmable current source (DAC U2) is programmed sequentially through its three most significant bits. Check sweep voltage waveforms (A5TP5 and A5TP6) for this test in Figure 8−42. If the waveform at A5TP5 is correct, but the waveform at A5TP6 is incorrect, the trouble is in the Clamping or Sweep Voltage Buffers circuit.

Error Code E003

Tuning Voltage versus Marker Test. This test is performed on Instrument Preset or by pressing SHIFT 10. While this test checks operation of the A4 Scaling and Marker assembly, the VSW1 Sweep Generator outputis used on A4 as a DAC reference voltage. For this test the VSW1 output should be 0V.

No Sweep Ramp

If an RF plug-in is not installed, a no sweep ramp condition is usually caused by the Sweep Ramp Generator circuit, or the Sweep Trigger circuit. Check the sweep voltage at A5TP5 to determine if the ramp is stopped at the beginning (−1V) or end (+11V) of the sweep. If the voltage at A5TP5 is approximately +11V, check that a retrace sweep is enabled by +5V at A5TP12. If A5TP5 is approximately −1V, check that the retrace circuit is disabled by 0V at A5TP12. Check operation of Sweep Ramp Generator and Sweep Trigger circuits as follows:

Sweep Ramp Generator Check. Check each of the following test points:

- A5TP2 − Should be approximately −1.2V.
- A5TP3 − Should be approximately 0V (Stop Sweep circuit is off).

Sweep Trigger Check. The Ramp Limit comparators can be checked by forcing A5TP13 high (+15V) and low (−10V). Check the High Ramp Limit comparator (U34) by jumpering +15VF (U34 pin 8) to A5 TP13. The U34 output at A5TP14 should be low (0V). Check the Low Ramp Limit comparator (U35) by jumpering −10V (U34 pin 4) to A5TP13. The voltage level at A5TP15 should be about 0V.

Clamping

The lower clamp (0V) requires that Q5 is conducting to forward bias CR12A. The higher clamp (+10V) requires that Q4 be turned on, and that U19A is operational. CR4 is forward biased when the sweep voltage is greater than +10V, and clamps the ramp at +10V.

Sweep Voltage Buffers

Voltage follower U11 provides the VRAMP output at TP6. U13 is a voltage follower for all sweep modes except external sweep. U13 provides the sweep out voltage at TP7 as well as the drive for voltage followers U4 and U5. The inputs for these voltage followers is the sweep voltage from the clamp circuit.

Address Decoder, Data Buffer, and Software Control

Troubleshooting the Address Decoder, Data Buffer, and Software control circuits involves using the Hexadecimal Data Write feature of the 8350A (See Note 1 in the A5 schematic diagram notes). Each data flip-flop in the Software Control circuit should be addressed and data written into it. Check the data flip-flop outputs respond correctly to the data written.

.P GENERATOR

PROGRAMMING CONNECTOR 18 — 18 — 39

RF PLUG-IN INTERFACE 32 — J2 L SSRQ — P/O W4 — 32 — J1

P/O A3 MICROPROCESSOR

PI — XA3A — XA5A — PI

I/O EI	17	I/O EI	15
L I/O STB	37	L I/O STB	13
L IAØ	18	LIAØ	16
L IA1	41	LIA1	39
L IA2	19	LIA2	17
L IA3	42	LIA3	40
L IA4	20	LIA4	18
IDØ	28	IDØ	6
ID1	29	ID1	28
ID2	30	ID2	7
ID3	31	ID3	29
ID4	32	ID4	8
ID5	33	ID5	30
ID6	34	ID6	9
ID7	35	ID7	31

Ⓐ ADDRESS DECODER — 2014H TO 2017H — 4

Ⓑ DATA BUS BUFFER — DATA — 8

Ⓒ SOFTWARE CONTROL — 10

SWP RAMP CONTROL

PROGRAMMABLECURRENT SOURCE INPUTS

L SSRQ

SWEEP RAMP CONTROL

SWEEP TRIGGER CONTROL

CNTR CONTROL

OUTPUT LOGIC CONTROL — 13

Ⓓ SWEEP RAMP GENERATOR

DAC — TP1 — STOP SWEEP — TP2 — TP5 — +10.8V -0.95V — SWEEP VOLTAGE

L SSRQ — L SFSRQ — L MAN — ≥1 — TP3

L EXT SW — PL1 — ≥1 — TP12 — RETRACE

P/O A8 HP-IB INTERFACE

PI — XA8 — XA5B — P2

L REM TRG — 3 — 25

P/O A6 RECTIFIER ASSY

PI — XA6 — XA5A — PI

L LINE TRG — 24 — 16

STOP SWEEP — J10 — 925 — E3 — XA5B — P2 — 41

PROGRAMMING CONNECTOR — J13 — P/O W7 — J3

5	L SFSRQ	5	5	
9	EXT TRG	9	9	
3	L PLRQ	3	3	
15	L MKRQ	15	15	
8	L RFBRQ	8	8	
20	L BPRQ	20	20	

RF PLUG-IN INTERFACE — J2 — P/O W4 — J1

54	L RFBRQ	54	
55	L BPRQ	55	
23	L ZMRQ	23	

XA5B — P2 — 19

16 L PLRQ
38 L MKRQ
17 L RFBRQ
40 L BPRQ
33 L ZMRQ
27 L AMK
6 L MK

P/O A4 SCALING AND MARKER

P2 — XA4B

L AMK — 27
L MK — 6

Ⓔ SWEEP TRIGGER

TP13 — LOW RAMP LIMIT — TP15 — -0.3V

+10.8V — -0.95V — SWEEP VOLTAGE

HIGH RAMP LIMIT — TP19 — +10.8V

TM1 — TM2 — SNGL — INT

TP9 — PL1

L REM TRG
L LINE TRG
EXT TRG

Ⓗ SWEEP RAMP STATUS

UPPER CLAMP — UPPER CLAMP SENSE — ≥1 — BP

SWEEP VOLTAGE — -0.3V — START OF SWEEP UP SENSE — L PL1

Ⓙ 27KHZ/1KHZ OSCILLATOR

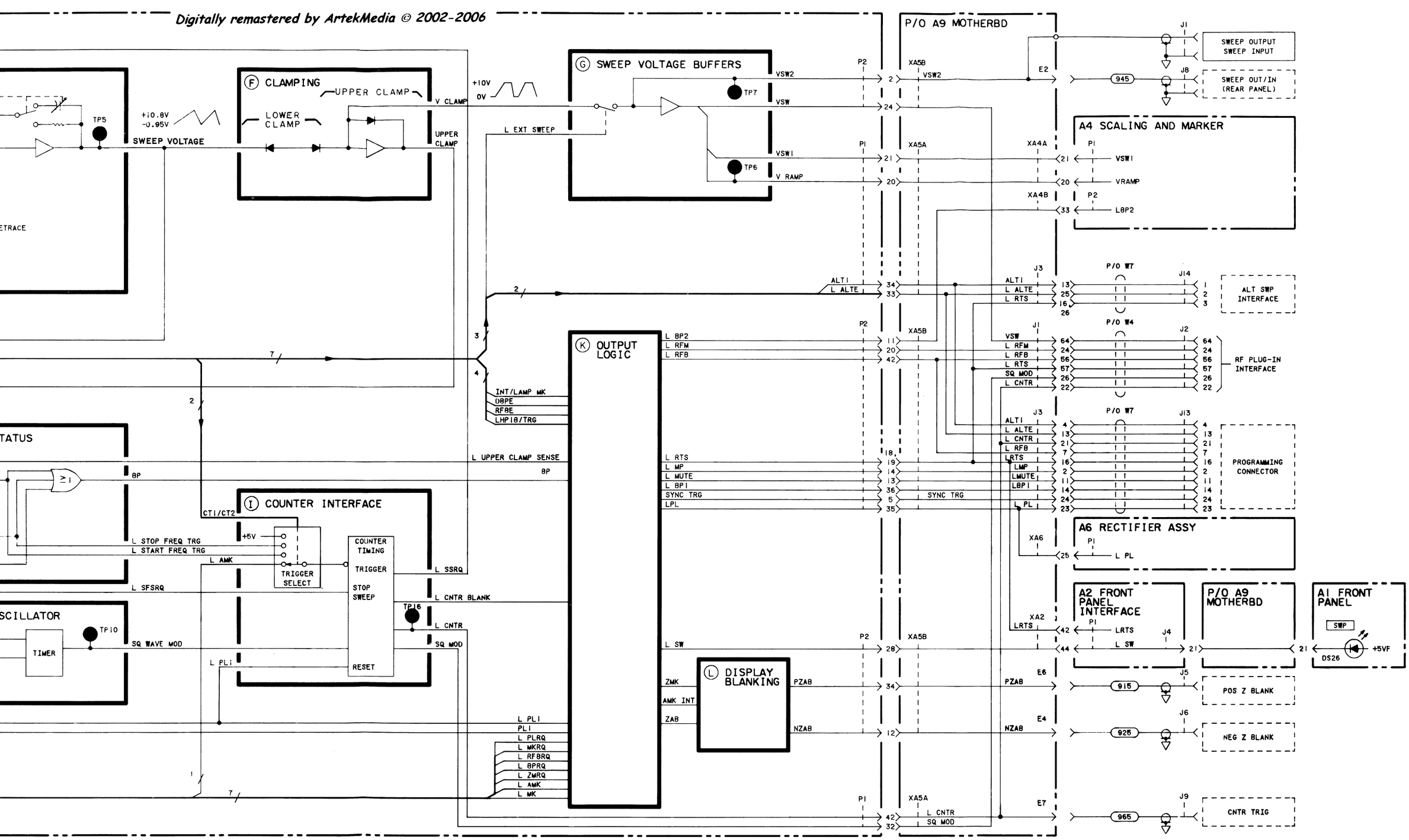
L RESET — J2 27KHZ 1KHZ — TIMER — TP10 — SQ WAVE MOD

L PLI

L STOP FREQ TRG
L START FREQ TRG
L AMK
L SFSRQ

CT1/CT2 — +5V

Ⓕ CLA — LOW CLA

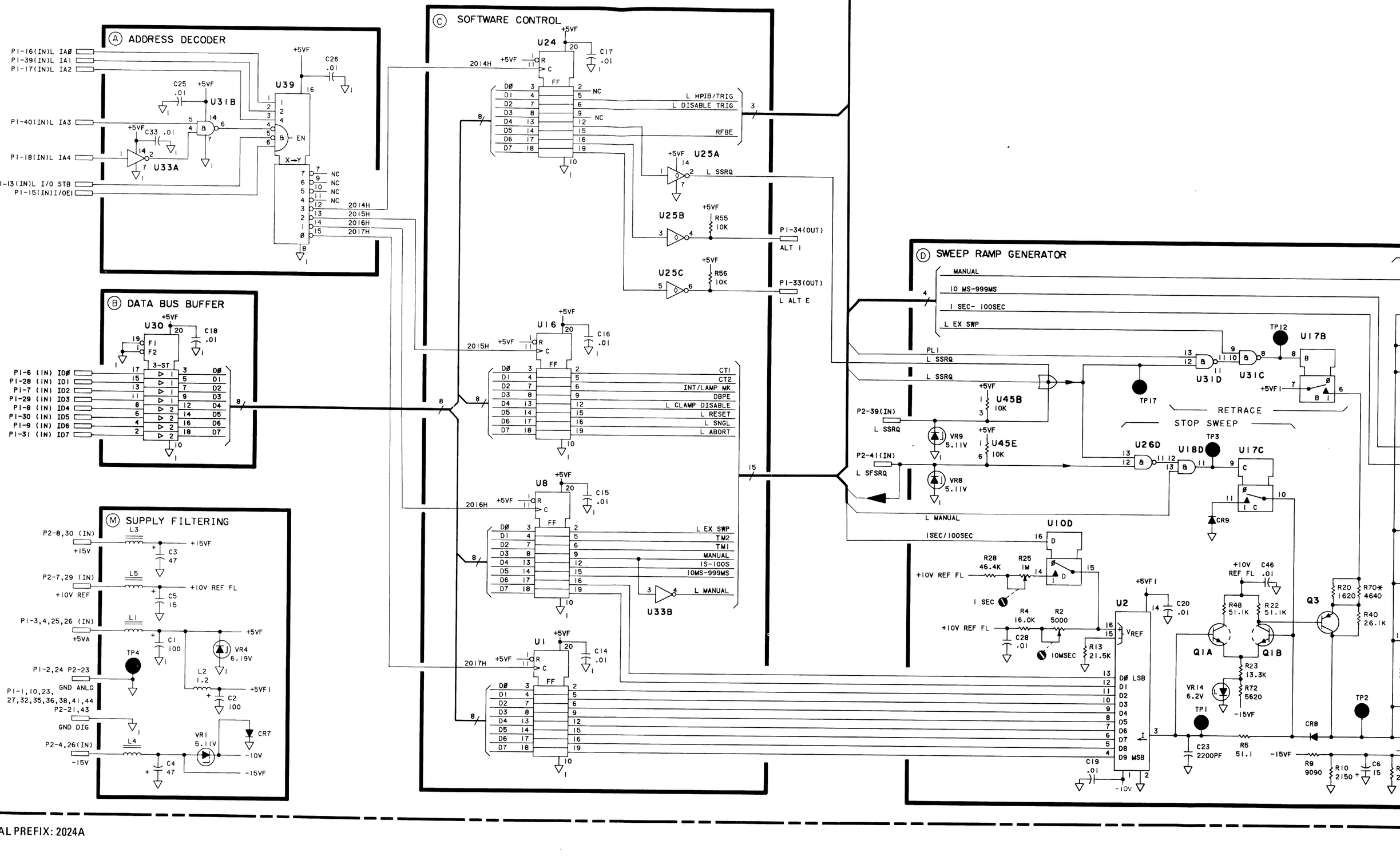


A5

Figure 8-39. A5 Sweep Generator Block Diagram

Figure 8-43. A5 Sweep Generator, Schematic Diagram (1 of 2)

A5 SWEEP GENERATOR (TYPE 2)
08350-60025



SERIAL PREFIX: 2024A

17

CONTROL BUS

11

TO SHEET 2

Figure 8-43. A5 Sweep Generator, Schematic Diagram (1 of 2)

A5 SWEEP GENERATOR, CIRCUIT DESCRIPTION (Cont'd)

Sweep Ramp Status Ⓗ

The Sweep Ramp Status circuit generates digital signals that indicate the present status of the sweep voltage. The signals generated are as follows:

- L UPPER CLAMP SENSE – Active low when the sweep voltage is in the upper clamp (+10V).
- L START FREQ TRG – High-to-low transition used to trigger Counter interface circuit when externally counting the start sweep frequency.
- L STOP FREQ TRG – High-to-low transition used to trigger Counter interface circuit when externally counting the stop sweep frequency.
- BP – Blanking Pulse. Active high from start of upper clamp until start of sweep up voltage.

Start of Sweep Up Sense. Operational amplifier U19B acts as a comparator with its noninverting input referenced to −0.3V. The unclamped sweep voltage (−0.95V to +10.8V) is the inverting input to U19B. While the unclamped sweep voltage is more positive than −0.3V, the U19B output is saturated negative (feedback is removed because CR5 is reverse biased). CR10 is also reverse biased, producing a logic low at the input to schmitt trigger inverter U14B.

When the unclamped sweep voltage goes more negative than −0.3V, the U19B output goes positive, and CR5 is forward biased to connect feedback resistor R44. CR10 is also forward biased and, when the U19B output reaches a valid logic high, the schmitt trigger inverter U14B output switches low. This low output is produced prior to the unclamped sweep voltage reaching its negative peak, and lasts until the sweep voltage approaches −0.3V on the sweep up ramp.The Start of Sweep Up Sense output sets R-S flip-flop U41B at the end of each sweep retrace, and maintains an active blanking pulse (BP) until just prior to the clamped sweep voltage comes out of its lower clamp.

Upper Clamp Sense. When the sweep voltage is less than +10V, the U19A output from the Clamping circuit biases on zener diode VR2. This results in a high logic state for the U20D output (L UPPER CLAMP SENSE). When the sweep voltage exceeds +10V, the U19A output drops to +9.4V, and VR2 is biased off; resulting in an active low L UPPER CLAMP SENSE output.

Start Frequency Trigger. R-S flip-flop U41C is reset at the start of each sweep when blanking pulse BP goes low. The leading edge of the U41C low output is used to trigger the Counter Interface circuit. U41C is set by L PL1 when the sweep voltage voltage reaches its peak (+10.8V); this allows L START FREQ TRG to be generated again on the next sweep.

Stop Frequency Trigger. R-S flip-flop U41B is reset by L UPPER CLAMP SENSE when the sweep voltage reaches +10V; the leading edge of the U41B low output is used to trigger the Counter interface circuit. U41B is set at the start of the next sweep by the U14B output, which allows another L STOP FREQ TRG to be generated at the end of the sweep.

Blanking Pulse. The BP (Blanking Pulse) signal is generated by the 3-input NAND gate U21A. It is active high at all times except when the sweep up voltage is between −0.3V and +10V. The Upper Clamp Sense output initiates the blanking pulse when the sweep up voltage reaches +10V. The L PL1 (Low = Pen Lift 1) to U21A maintains the active blanking output for the sweep retrace (+10.8V to −0.95V).The U14B output from the Start of Sweep Up Sense circuit keeps BP active high until the sweep up voltage reaches about −0.3V.

Counter Interface Ⓘ

The counter interface circuit provides digital signals to allow a microwave frequency counter to measure either the Start frequency, the Stop frequency, or the Active Marker frequency, while in the sweep mode, independent of sweep time. While the counter is measuring the frequency, the sweep is stopped. The length of time the sweep is stopped is determined by the gate time of the counter. While the counter is counting, the internal 27.8/1 KHz squarewave AM modulation is disabled and a blanking signal is generated to avoid a bright spot on a display. A muting signal is also generated to disable a recorder.

The counter function is initiated by a SHIFT M2. The counter measures whichever function was last active (ie., START, STOP, or ACTIVE MARKER). SHIFT M3 shuts off the counter function. Multiplexer U43 selects either the L START FREQ TRG, the L STOP FREQ TRG or the LAMK (Low = Active Marker) line. Control lines CT1 and CT2 set the condition of the multiplexer. When the counter function is not selected, the counter circuit is disabled by +5V at the input of the multiplexer.

A high-to-low transition on the selected input line initiates the counter interface by triggering the 40 microsecond timer U38A. When the timer is triggered, the L SSRQ (Low = Stop Sweep Request) line stops the sweep and the L CNTR (Low = Counter) line triggers the counter. The counter responds to the L CNTR trigger pulse by setting L SFSRQ (Low = Stop Forward Sweep Request) low within 40 microseconds.

When the inverted LSFSR is applied to D flip-flop U15B, it clocks through the high from U38A. This sets the U15B flip-flop outputs pin 8 low, and pin 9 high. The high-to-low transition at pin 8 triggers 20 microsecond timer U29B. After the timer has timed out, pin 12 goes high to disable the squarewave modulation with a low at TP11. The low at pin 8 of flip-flop U15B also puts a low on the L CNTR BLANK line and on L SSRQ, pin 12 U42F. This L SSRQ is wire ORed with the L SSRQ from U42E pin 10. This continues to stop the sweep after 40 microsecond timer U38A has timed out. When the counter has finished counting, it puts a high on the L SFSRQ line resetting flip-flop U15B through U23B. The low at flip-flop U15B pin 9 puts a high at TP11 enabling the squarewave. The high at pin 8 of the flip-flop triggers the 1.5 millisecond timer U29A. After the timer has timed out, the L SSRQ line goes high allowing the sweep to start and the L CNTR line goes high unblanking the display and enabling the recorder.

The interface circuit is disabled during retrace by a low on the LPL1 line.

27 kHz/1 kHz Oscillator Ⓙ

Timer U7 is connected as a free running oscillator and provides a stable output frequency to clock data flip-flop U15A. The timer oscillation frequency is determined by the RC network consisting of R24, R50, R51, C9, and C10 (C10 is connected by jumper J2 for a 1 kHz output at TP10). Data flip-flop U15A acts as a divide-by-two circuit. Since it is only clocked on
output, the squarewave output maintains a 50 perce
timer output duty cycle.The L RESET input is set a
MOD key is not selected. This turns off the oscill
output at TP10 is low (not affecting the RF powe

Output Logic Ⓚ

The Output Logic circuit provides several dig
synchronizing events with the sweep ramp. An ind
Table 8-29.

Display Blanking Ⓛ

The Display Blanking circuit provides signals to th
NEG Z BLANK BNC connectors. This informa
external CRT display during retrace, or while t
switching, or frequency counting. The POS Z BLA
CRT trace for markers and the ΔMarker funct
blanking outputs accommodate the use of differe

U6A drives the Negative Z-axis Blanking (NZAB)
Z-axis Blanking (ZAB) input to a −3.5V output

U6B drives the Positive Z-axis Blanking (PZAB) o
to +5V during sweep retrace and to −3.5V for in

Intensity markers are generated by the ZMK (Z
higher intensity marker is generated for the active
the AMK (Active Marker) input. This results in a
marker or the ΔMarker function.

TROUBLESHOOTING (Cont'd)

Sweep Ramp Status

The Sweep Ramp Status circuit produces a blanki
at all times except when the sweep ramp is positve
The L UPPER CLAMP SENSE line is high during
then high again when the sweep goes below +10
FREQ TRG and L STOP FREQ TRG lines are
circuit. Refer to Figure 8−46 for a timing diagr
waveforms.

Counter Interface

To troubleshoot the Counter Interface circuit with
a cable between rear panel CNTR TRIG and S
INSTR PRESET . Select Marker 3 (press M3). Th
should indicate a Marker 3 frequency in the cent
activate the counter interface by pressing SHI
shown in Figure 8−47.

CIRCUIT DESCRIPTION (Cont'd)

t generates digital signals that indicate the present
e signals generated are as follows:

SE – Active low when the sweep voltage is in the

– High-to-low transition used to trigger Counter
ernally counting the start sweep frequency.

High-to-low transition used to trigger Counter
ernally counting the stop sweep frequency.

ctive high from start of upper clamp until start of

Operational amplifier U19B acts as a comparator
ferenced to −0.3V. The unclamped sweep voltage
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n −0.3V, the U19B output is saturated negative
CR5 is reverse biased). CR10 is also reverse biased,
nput to schmitt trigger inverter U14B.

voltage goes more negative than −0.3V, the U19B
is forward biased to connect feedback resistor R44.
d, when the U19B output reaches a valid logic high,
B output switches low. This low output is produced
oltage reaching its negative peak, and lasts until the
3V on the sweep up ramp.The Start of Sweep Up
op U41B at the end of each sweep retrace, and
pulse (BP) until just prior to the clamped sweep
clamp.

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ut (L UPPER CLAMP SENSE). When the sweep
9A output drops to +9.4V, and VR2 is biased off;
PPER CLAMP SENSE output.

R-S flip-flop U41C is reset at the start of each sweep
ow. The leading edge of the U41C low output is used
circuit. U41C is set by L PL1 when the sweep voltage
'); this allows L START FREQ TRG to be generated

R-S flip-flop U41B is reset by L UPPER CLAMP
e reaches +10V; the leading edge of the U41B low
unter interface circuit. U41B is set at the start of the
, which allows another L STOP FREQ TRG to be
eep.

Blanking Pulse. The BP (Blanking Pulse) signal is generated by the 3-input NAND gate U21A. It is active high at all times except when the sweep up voltage is between −0.3V and +10V. The Upper Clamp Sense output initiates the blanking pulse when the sweep up voltage reaches +10V. The L PL1 (Low = Pen Lift 1) to U21A maintains the active blanking output for the sweep retrace (+10.8V to −0.95V).The U14B output from the Start of Sweep Up Sense circuit keeps BP active high until the sweep up voltage reaches about −0.3V.

Counter Interface (I)

The counter interface circuit provides digital signals to allow a microwave frequency counter to measure either the Start frequency, the Stop frequency, or the Active Marker frequency, while in the sweep mode, independent of sweep time. While the counter is measuring the frequency, the sweep is stopped. The length of time the sweep is stopped is determined by the gate time of the counter. While the counter is counting, the internal 27.8/1 KHz squarewave AM modulation is disabled and a blanking signal is generated to avoid a bright spot on a display. A muting signal is also generated to disable a recorder.

The counter function is initiated by a SHIFT M2. The counter measures whichever function was last active (ie., START, STOP, or ACTIVE MARKER). SHIFT M3 shuts off the counter function. Multiplexer U43 selects either the L START FREQ TRG, the L STOP FREQ TRG or the LAMK (Low = Active Marker) line. Control lines CT1 and CT2 set the condition of the multiplexer. When the counter function is not selected, the counter circuit is disabled by +5V at the input of the multiplexer.

A high-to-low transition on the selected input line initiates the counter interface by triggering the 40 microsecond timer U38A. When the timer is triggered, the L SSRQ (Low = Stop Sweep Request) line stops the sweep and the L CNTR (Low = Counter) line triggers the counter. The counter responds to the L CNTR trigger pulse by setting L SFSRQ (Low = Stop Forward Sweep Request) low within 40 microseconds.

When the inverted LSFSR is applied to D flip-flop U15B, it clocks through the high from U38A. This sets the U15B flip-flop outputs pin 8 low, and pin 9 high. The high-to-low transition at pin 8 triggers 20 microsecond timer U29B. After the timer has timed out, pin 12 goes high to disable the squarewave modulation with a low at TP11. The low at pin 8 of flip-flop U15B also puts a low on the L CNTR BLANK line and on L SSRQ, pin 12 U42F. This L SSRQ is wire ORed with the L SSRQ from U42E pin 10. This continues to stop the sweep after 40 microsecond timer U38A has timed out. When the counter has finished counting, it puts a high on the L SFSRQ line resetting flip-flop U15B through U23B. The low at flip-flop U15B pin 9 puts a high at TP11 enabling the squarewave. The high at pin 8 of the flip-flop triggers the 1.5 millisecond timer U29A. After the timer has timed out, the L SSRQ line goes high allowing the sweep to start and the L CNTR line goes high unblanking the display and enabling the recorder.

The interface circuit is disabled during retrace by a low on the LPL1 line.

27 kHz/1 kHz Oscillator (J)

Timer U7 is connected as a free running oscillator and provides a stable output frequency to clock data flip-flop U15A. The timer oscillation frequency is determined by the RC network consisting of R24, R50, R51, C9, and C10 (C10 is connected by jumper J2 for a 1 kHz output at TP10). Data flip-flop U15A acts as a divide-by-two circuit. Since it is only clocked on the positive edge of the timer output, the squarewave output maintains a 50 percent duty cycle independent of the timer output duty cycle. The L RESET input is set active low when the front panel ⊔⊓ MOD key is not selected. This turns off the oscillator and ensures the SQ WAVE output at TP10 is low (not affecting the RF power level).

Output Logic (K)

The Output Logic circuit provides several digital outputs that are used for synchronizing events with the sweep ramp. An index of these outputs is provided in Table 8-29.

Display Blanking (L)

The Display Blanking circuit provides signals to the rear panel POS Z BLANK and NEG Z BLANK BNC connectors. This information is used for blanking of an external CRT display during retrace, or while the sweep is stopped for band-switching, or frequency counting. The POS Z BLANK output can also intensify the CRT trace for markers and the ΔMarker function. The positive and negative blanking outputs accommodate the use of different external displays.

U6A drives the Negative Z-axis Blanking (NZAB) output. It converts the 0V to +5V Z-axis Blanking (ZAB) input to a −3.5V output during sweep retrace.

U6B drives the Positive Z-axis Blanking (PZAB) output. It converts the ZAB input to +5V during sweep retrace and to −3.5V for intensity markers.

Intensity markers are generated by the ZMK (Z-axis Marker) input to U6B. A higher intensity marker is generated for the active marker by summing ZMK with the AMK (Active Marker) input. This results in a −7V PZAB output for the active marker or the ΔMarker function.

TROUBLESHOOTING (Cont'd)

Sweep Ramp Status

The Sweep Ramp Status circuit produces a blanking pulse (BP) that is active high at all times except when the sweep ramp is positve going and between 0 and +10V. The L UPPER CLAMP SENSE line is high during sweep up and goes low at +10V then high again when the sweep goes below +10V during retrace. The L START FREQ TRG and L STOP FREQ TRG lines are used by the Counter Interface circuit. Refer to Figure 8−46 for a timing diagram of the Sweep Ramp Status waveforms.

Counter Interface

To troubleshoot the Counter Interface circuit without an external counter, connect a cable between rear panel CNTR TRIG and STOP SWEEP connectors. Press INSTR PRESET. Select Marker 3 (press M3). The FREQUENCY/TIME display should indicate a Marker 3 frequency in the center of the frequency band. Then activate the counter interface by pressing SHIFT M2. Check for waveforms shown in Figure 8−47.

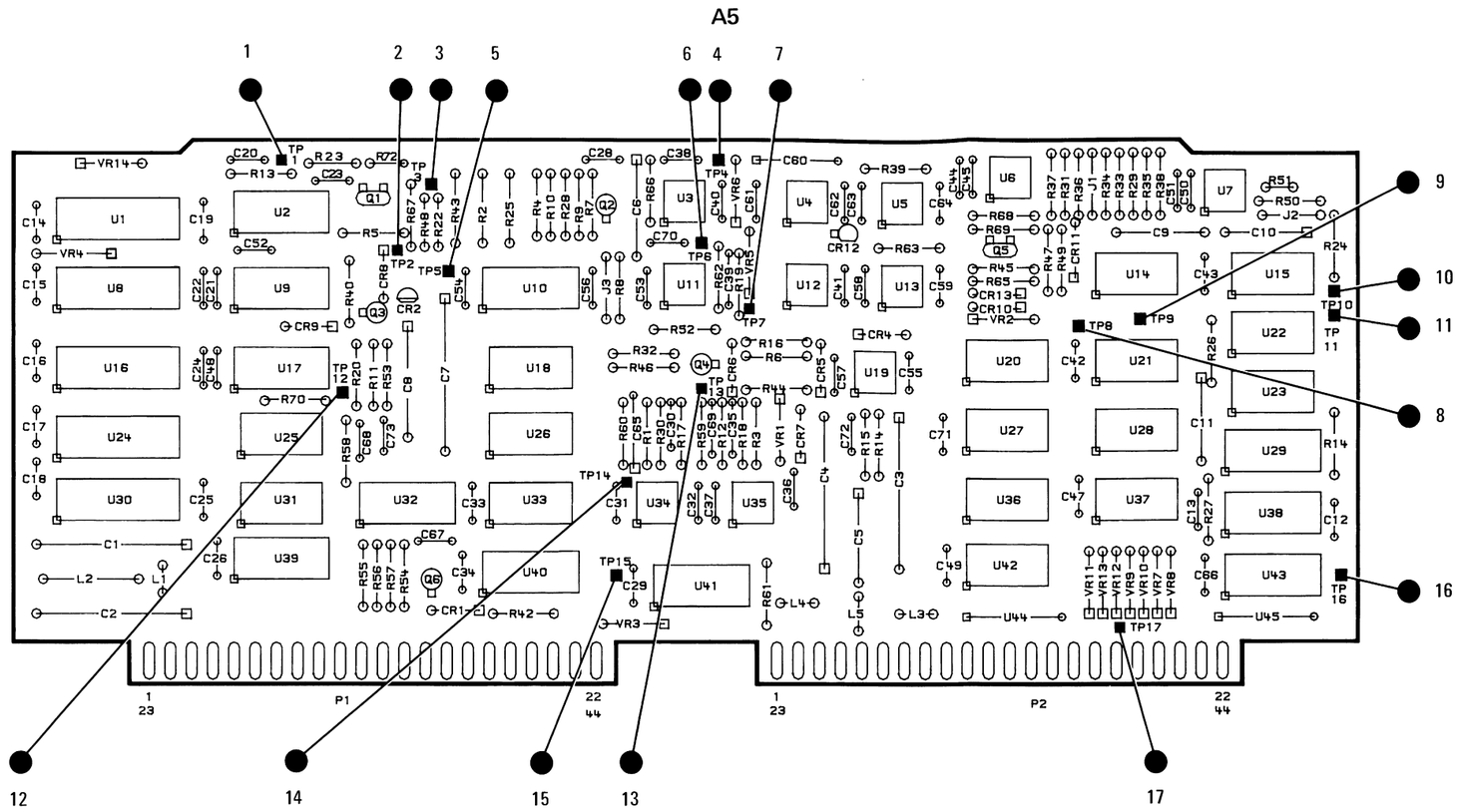


Figure 8-40. A5 Sweep Generator, Component Locations

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◄ ► TO STEP TO THE NEW ADDRESS.

A5P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1	GND DIG			M
23	GND DIG			M
2	GND ANLG			M
24	GND ANLG			M
3	+5VA	IN	A7P1-2, 24	M
25	+5VA	IN	A7P1-2, 24	M
4	+5VA	IN	A7P1-2, 24	M
26	+5VA	IN	A7P1-2, 24	M
5	GND DIG			M
27	GND DIG			M
6	ID0	IN	A3P1-28	B
28	ID1	IN	A3P1-29	B
7	ID2	IN	A3P1-30	B
29	ID3	IN	A3P1-31	B
8	ID4	IN	A3P1-32	B
30	ID5	IN	A3P1-33	B
9	ID6	IN	A3P1-34	B
31	ID7	IN	A3P1-35	B
10	GND DIG			M
32	GND DIG			M
11	GND ANLG			M
33	L ALTE	OUT	J13-17, J14-2	C
12	GND ANLG			M
34	ALT1	OUT	J13-4, J14-1	C
13	L I/OSTB	IN	A3P1-37	A
35	GND DIG			M
14	I/OE2	IN	A3P1-16	NOT USED
36	GND DIG			M
15	I/OE1	IN	A3P1-17	A
37	L IRD	IN	A3P1-39	NOT USED
16	L IA0	IN	A3P1-18	A
38	GND DIG			M
17	L IA2	IN	A3P1-19	A
39	L IA1	IN	A3P1-41	A
18	L IA4	IN	A3P1-20	A
40	L IA3	IN	A3P1-42	A
19	EXT TRG	IN	J13-9	E
41	GND DIG			M
20	VRAMP	OUT	A4P1-20	G
42	L CNTR	OUT	J2-22, J9	I
21	VSW1	OUT	A4P1-20	G
43	N.C.			
22	GND ANLG			M
44	GND DIG			M

A5P2

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	GND ANLG GND ANLG			M M
2 24	VSW2 VSW	I/O OUT	J1, J8 J2-64	G G
3 25	N.C. L REMTRG	 IN	 A8P1-3	 E
4 26	−15V −15V	IN IN	A7P1-14, 36 A7P1-14, 36	M M
5 27	SYNC TRG L AMK	OUT IN	J13-24 A4P2-27	K I
6 28	L MK L SW	IN OUT	A4P2-6 A2P1-44	K K
7 29	+10V REF +10V REF	IN IN	A4P2-7, 29 A4P2-7, 29	M M
8 30	+15V +15V	IN IN	A7P1-8, 30 A7P1-8, 30	M M
9 31	GND DIG GND DIG			M M
10 32	GND DIG GND DIG			M M
11 33	L BP2 L ZMRQ	OUT IN	A4P2-33, J2-53 J2-23	K K
12 34	NZAB PZAB	OUT OUT	J6 J5	L L
13 35	L MUTE L PL	OUT OUT	J13-11 A6P1-25	K K
14 36	L MP L BP1	OUT OUT	J13-2 J13-14	K K
15 37	L LINETRG SQ MOD	IN OUT	A6P1-24 J2-26	E I
16 38	L PLRQ L MKRQ	IN IN	J13-3 J13-15	K K
17 39	L RFBRQ L SSRQ	IN IN	J2-54, J13-8 J2-32, J13-18	K D
18 40	L RTS L BPRQ	OUT IN	A2P1-42, J2, J13, J14 J2-55, J13-20	K K
19 41	L RTS L SFSRQ	OUT IN	A2P1-42, J2, J13, J14 J13-5, J10	K D, I
20 42	L RFM L RFB	OUT OUT	J2-24 J2-56, J13-7	K K
21 43	GND DIG GND DIG			M M
22 44	GND ANLG GND ANLG			M M

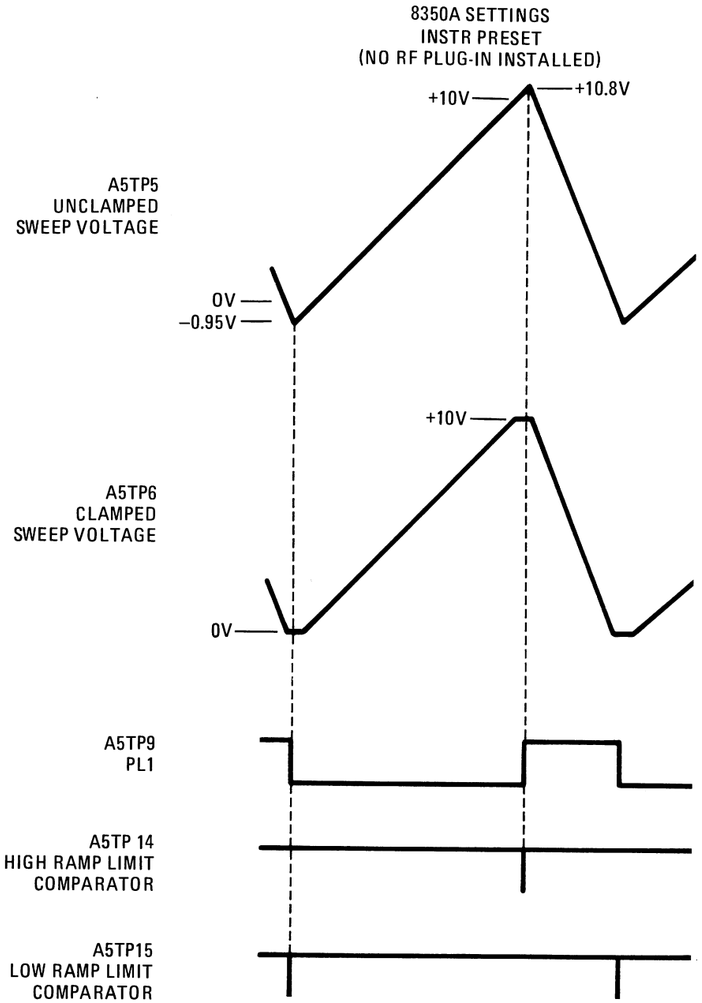
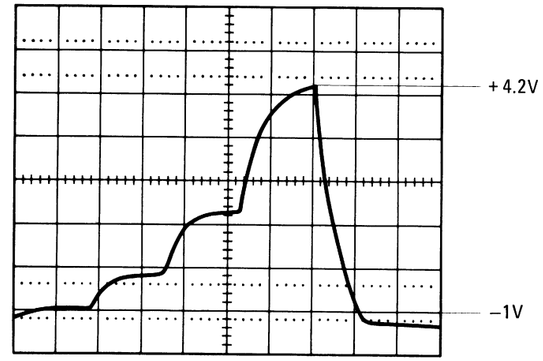


Figure 8-41. Sweep Trigger Timing Diagram

Table 8-28. Sweep Trigger Mode Select

TM1	TM2	Sweep Trigger Mode
0	0	INTERNAL
0	1	LINE
1	0	EXTERNAL
1	1	SINGLE/REMOTE

A5TP5 SHIFT II



A5TP6 SHIFT II

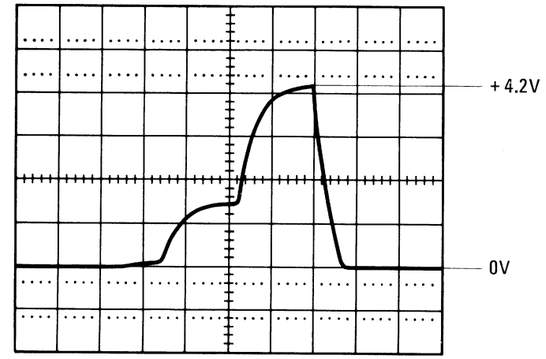


Figure 8-42. Sweep Voltage Waveforms for Sweep versus Marker Self Test

Table 8-29. Output Logic Outputs

Signal	Description
AMK	1. L AMK and ZAB and L MP are low.
L BP1	1. L BPRQ is low. or 2. DBPE and BP1 are high.
L BP2	1. BP1 is high.
L MP	1. L ZMRQ is low. or 2. INT/L AMP MK is high and L MKR is low. or 3. INT/L AMP MK is high and L MK is low.
L MUTE	1. L CNTR BLANK or L BPRQ is low.
L PL	1. LP1 is low. or 2. L UPPER CLAMP SENSE is low. or 3. L PLRQ is low.
L RFB	1. L RFBRQ is low. or 2. PL1 and RFBE are high.
L RFM	1. INT/L AMP MK is low AND: a. a. L MK is low. a. or b. L MKRQ is low
L RTS	1. PL1 is high.
L SW	1. L PL1 is high.
SYNC TRG	1. U32A pin 4 is low (40 μs pulse triggered by L HPIB TRG) or 2. L RFBRQ is low or 3. L PL1 is low.
ZAB	1. DBPE and BP1 are high. or 2. L CNTR BLANK is low. or 3. L BPRQ is low.
ZMK	1. L MP and ZAB are low.

A5 SWEEP GENERATOR (2 OF 2)
08350-60025

FROM SHEET 1 — 11 — CONTROL BUS — 11 — 10

(H) SWEEP RAMP STATUS

PL1

UPPER CLAMP SENSE

UPPER CLAMP — VR2 11V — U14A — CR11 — R49 1000 — U20D — U21B — NC — C42 .01 — TP8 — BP — U21A

FROM SHEET 1 — L PL1

SWEEP VOLTAGE — R6 5110 — -0.3V — U19B — R44 34.8K — CR5 — CR10 — U14B — R47 1000

U41B — L STOP FREQ TRG

U41C — L START FREQ TRIG

START OF SWEEP UP SENSE

L UPPER CLAMP SENSE

8

(I) COUNTER INTERFACE

U43 — CT1 — CT2 — FA — FB — MUX — +5VF — C66 .01

U38A — R27 42.2K — C13 2200PF — 40µs — TP16

L STOP FREQ TRG — L START FREQ TRG — U42E

P2-27(IN) — L AMK — U44A 10K — NC

U29A — R26 42.2K — C11 0.1

U29B — R41 21.5K — C12 2200PF

L PL1 — L SFSRQ — U22C — U23B — U20E — U15B — FF

3

(J) 27KHZ/1KHZ OSCILLATOR

LRESET — MOD FREQ — R51 5000 — R50 7500 — R24 1210 — C50 .01

U7 — EXT TMG — 1KHZ — J2 — 27KHZ — C10 .033 — C9 .0012 — C51 .01

U15A — C43 .01 — TP10 — SQ WAVE

SERIAL PREFIX: 2024A

CONTROL BUS

OUNTER INTERFACE

U43 C66 .01 U38A R27 42.2K C13 2200PF TP16 40µs P1-42(OUT) L CNTR VR3 5.11V U42E L SSRQ LSSRQ U44A 10K L STOP FREQ TRG L START FREQ TRG MUX NC U29A R26 42.2K C11 0.1 U23A U42F L SSRQ U14D L CNTR BLANK U29B R41 21.5K C12 2200PF U15B U22C U23B U20E L PLI L SFSRQ FF U23D 20µs U23C TP11 P2-37(OUT) SQ MOD SQ WAVE

7KHZ/1KHZ OSCILLATOR

RESET MOD FREQ R51 5000 R50 7500 R24 1210 C50 .01 U7 EXT TMG LRESET 1KHZ J2 27KHZ C9 .0012 C51 .01 C10 .033 U15A C43 .01 TP10 SQ WAVE

K OUTPUT LOGIC

P2-33(IN)L ZMRQ U44D 10K VR11 5.11V U44B 10K U45A 10K U37B U37D U27B U36C P2-14(OUT)

P2-6(IN) L MK P2-38(IN)L MKRQ VR12 5.11V U37C U36D INT/LAMP MK P2-20(OUT)

U20B U28B ZMK L AMK U14C U22A AMK P2-13(OUT)

L CNTR BLANK U28D U45D 10K P2-40(IN)L BPRQ VR7 5.11V C71 .01 U28C U27A DBPE U21C ZAB U45F 10K P2-36(OUT)

BP U20F P2-11(OUT)

U42C P2-18,19(OUT)

PL1 RFBE U27D U22D P2-42(OUT)

U45C 10K P2-17(IN)L RFBRQ VR10 5.11V U18A U26A P2-5(OUT) S

R58 42.2K C68 2200PF U32A 40µs C49 .01 U44C 10K P2-28(OUT)

L HPIB/ TRIG NC U42B

L PLI U28A U37A C47 .01 U42D U44E 10K P2-35(OUT)

L UPPER CLAMP SENSE U44F 10K P2-16(IN)L PLRQ VR13 5.11V

CONTROL BUS

P1-42(OUT) L CNTR

L SSRQ

LSSRQ

U42F

L SSRQ

U14D L CNTR BLANK

TP11

U23C

P2-37(OUT) SQ MOD

SQ WAVE

K OUTPUT LOGIC

P2-33(IN)L ZMRQ

P2-6(IN) L MK

P2-38(IN)L MKRQ

INT/LAMP MK

P2-14(OUT) L MP

P2-20(OUT) L RFM

L AMK

L CNTR BLANK

P2-40(IN)L BPRQ

DBPE

BP

PL1

RFBE

P2-13(OUT) L MUTE

ZAB

P2-36(OUT) L BP1

P2-11(OUT) L BP2

P2-18,19(OUT) L RTS

P2-42(OUT) L RFB

P2-17(IN)L RFBRQ

P2-5(OUT) SYNC TRG

L HPIB/ TRIG

NC

L PL1

L UPPER CLAMP SENSE

P2-16(IN)L PLRQ

P2-28(OUT) L SW

P2-35(OUT) L PL

L DISPLAY BLANKING

ZMK

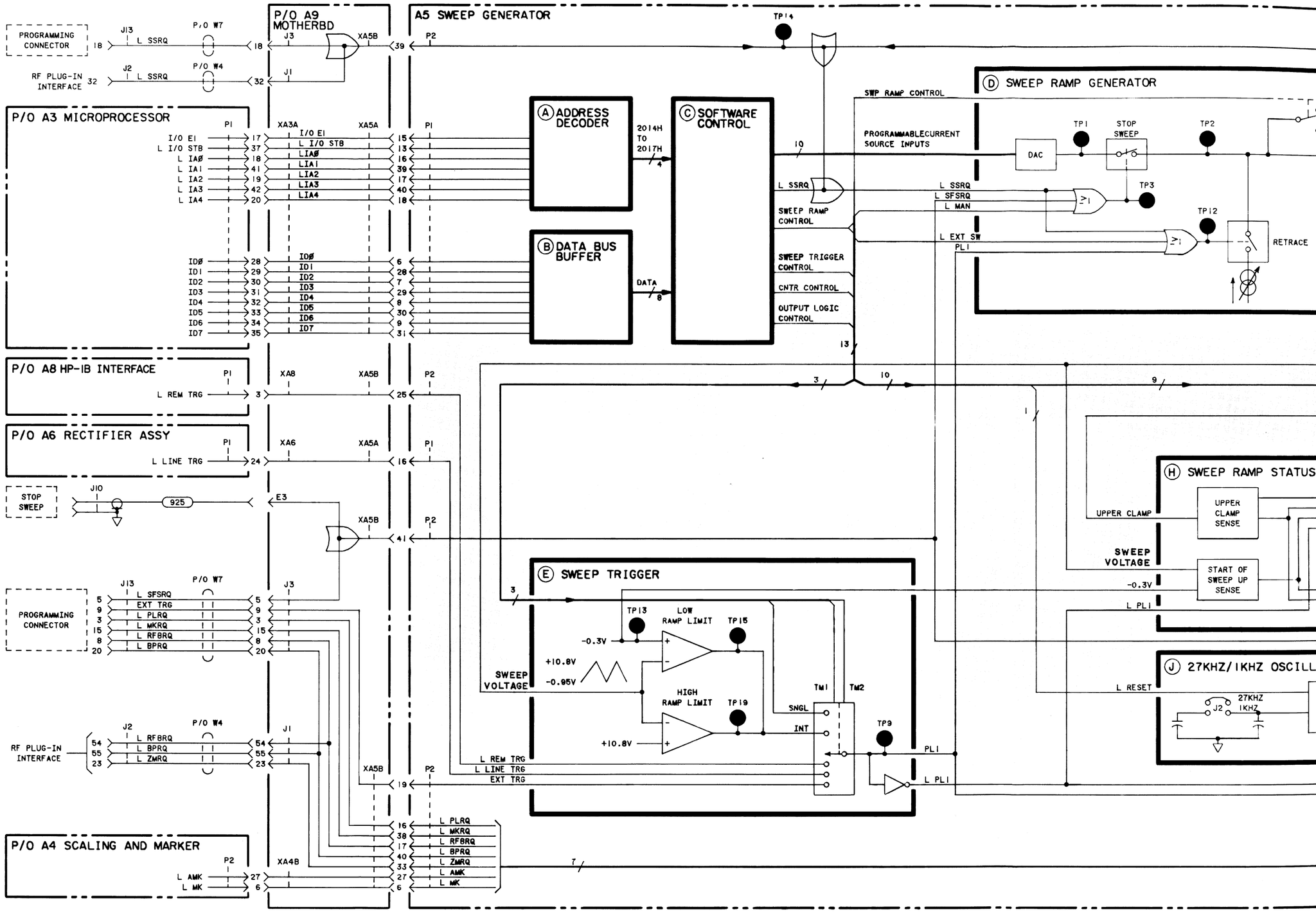
AMK

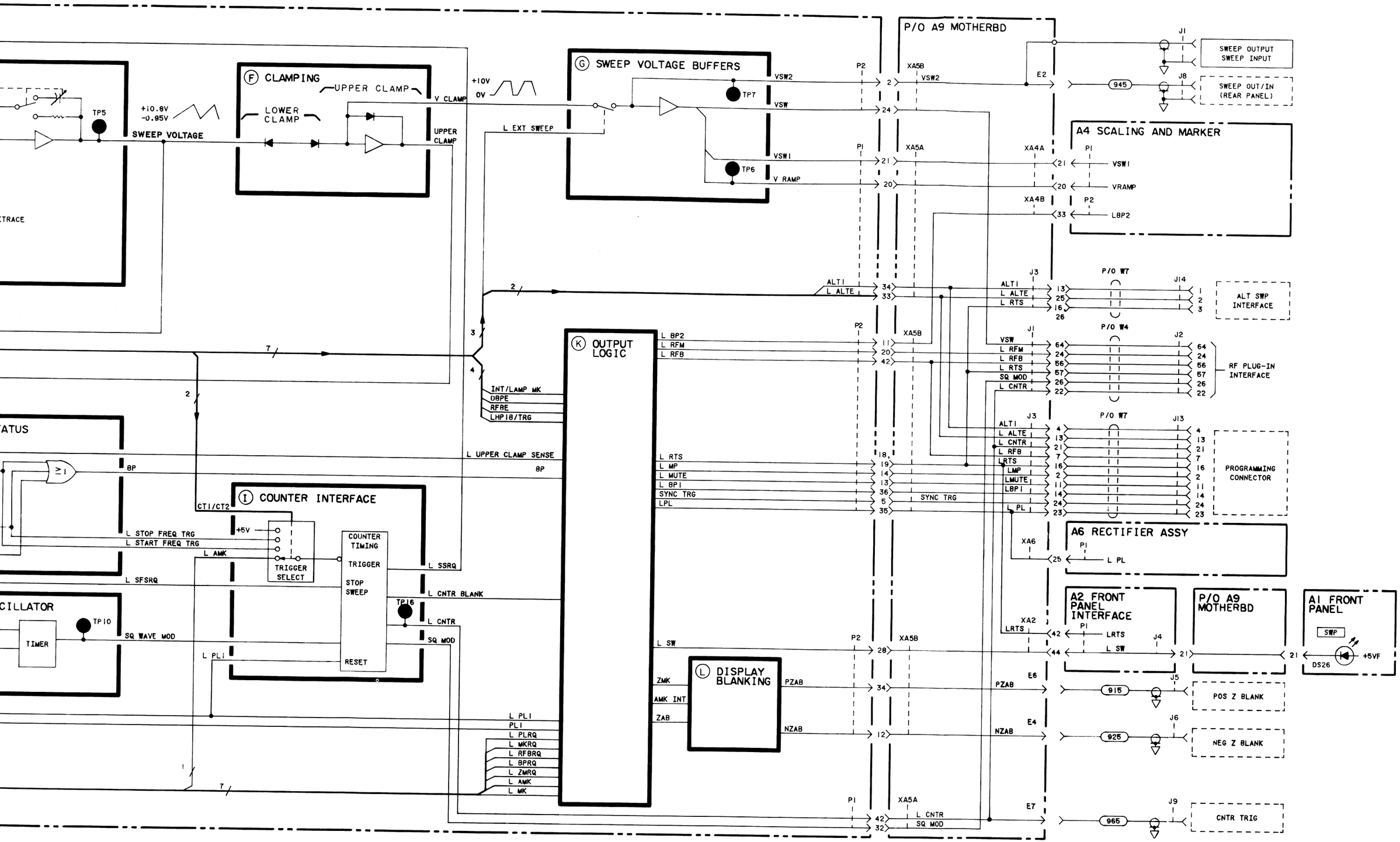
ZAB

P2-34(OUT) PZAB

P2-12(OUT) NZAB

Figure 8-43. A5 Sweep Generator, Schematic Diagram (2 of 2)





A5

Figure 8-44. A5 Sweep Generator, Block Diagram

A6 RECTIFIER and A7 REGULATOR, CIRCUIT DESCRIPTION

The main function of the A6 Rectifier and A7 Regulator is to provide regulated power supply voltages for the 8350A and RF Plug-in installed. Table 8-30 lists the regulated power supply outputs and describes where they are used. Overvoltage protection and "power on" LED indicators for all regulated supplies are on the A7 Regulator.

The +20V, −10V, and −40V power supplies are used only in the RF plug-in. They provide power for the RF microcircuits, and are also used for reference voltages to control frequency and power. Therefore, these supplies must be very well regulated. To ensure high stability (independent of voltage drops through the various connectors, motherboard traces, and cables) post regulation is used. For these supplies, their respective voltages and returns are sensed in the RF Plug-in, and regulated at that point. (See simplified diagram in Figure 8-48.)

Additional functions provided are as follows:

- Penlift Driver
- Power-up − Resets microprocessor when power is turned on.
- Line Trigger
- Power Supply Failure Detection
- Air Flow Detection

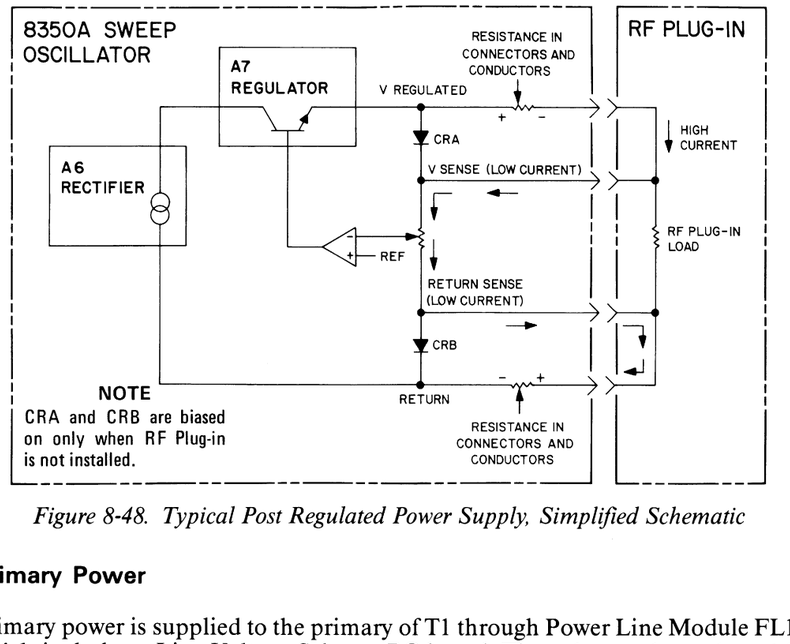


Figure 8-48. Typical Post Regulated Power Supply, Simplified Schematic

Primary Power

Primary power is supplied to the primary of T1 through Power Line Module FL1, which includes a Line Voltage Selector PC board. The voltage selector board is positioned to provide correct power connections to T1 for operation with line voltages of 100 Vac, 120 Vac, 220 Vac, or 240 Vac. (See Figure 2-1 for correct installation of the Line Voltage Selection PC board.)

Thermal switch S2 senses the internal temperature and opens to turn off primary power if the temperature exceeds 65°C. Suppression of radio frequency interference (RFI) is provided by the LC filter in FL1. The front panel LINE switch S1 turns the line power on or off.

Transformer T1 supplies 120 Vac through the Power Line Module to fan B1. Assembly E1 contains a spark gap which fires to short across the primary of T1 and blow the Power Line Module fuse if the line voltage applied is excessive (i.e. Line Voltage PC board positioned for 100 Vac, and 240 Vac line power is applied). Assembly E1 also contains a capacitor for filtering audio noise.

NOTE

All power supply circuit descriptions include the unregulated (A6 Rectifier) and regulated (A7 Regulator) sections of the supply.

Table 8-30. Power Supply Distribution

Power Supply	Distribution
+20V	RF Plug-in
+15V	A4, A5, RF Plug-in
+10V	RF Plug-in
+5VA	A2, A3, A4, A5, A6, A8, J13
+5VAFP	A1
+5VB	RF Plug-in
−10V	RF Plug-in
−15V	A4, A5, RF Plug-in
−40V	RF Plug-in

+20V Power Supply

+20V Unregulated. The approximately 26 Vac T1 output is rectified by full-wave bridge rectifer A6CR1−4. A6C1 and A6C12 filter switching transients, and A9C6 filters ac line ripple.

+20V Regulator. Regulation is provided by 3-terminal regulator A7U7. Error amplifier A7U8 improves regulation by controlling the reference voltage to the regulator A7U7 pin 1. Under normal operating conditions, the voltage difference between the regulator output and its reference input is about 1.25V. Zener diode VR2 provides a stable reference voltage to the noninverting input of A7U8. The +20V output is scaled by the voltage divider consisting of A7R9, A7R10 (+20V ADJ potentiometer), and A7R11, and
amplifier U8 drives the regulato
a direct function of the referenc
the voltage divider is connected
(+20V Return Sense) inputs
regulated supply or current re
generates an error signal to A7
Plug-in is not installed, diodes
REG and +20V RET lines acr
drops being added to the volta
power supply output voltage. If
−40V supplies are automatical

Voltage regulator A7U7 has o
ground, A7U7 will go into a cu
Fuse A7F5 protects the +20V l
protection is provided by crov
greater than approximately +2
ground and causing regulator
fuse A7F5 provides overcurre
regulator A7U7 from positive tr
a power on indication when
Diode A7CR18 provides revers

±15V Power Supplies

±15V Unregulated. The t
(approximately 20Vac) are ap
rectifier provides both a +15V a
tap (system ground). Fuses A6
and A6C3 filter switching tran

+15V Regulator. Three-te
current limiting. The actual vol
reference input of the regulat
protection. If the power supply
on, shorting the +15V supply t
limit. LED A7DS6 provides a p
approximately +12V. Diode A

−15V Regulator. Regulati
The regulator output voltage is
through A7R86. Diode A7CR2
shorted to ground. Overvoltage
the power supply output excee
the −15V supply to ground, an
provides a power on indicatio
−12V. Diode A7CR17 provide

±10V Power Supplies

±10V Unregulated. The t
(approximately 16 Vac) are ap
rectifier provides both a +10V
the T1 center-tap (which is isc

EGULATOR, CIRCUIT DESCRIPTION

Rectifier and A7 Regulator is to provide regulated
8350A and RF Plug-in installed. Table 8-30 lists the
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implified diagram in Figure 8-48.)

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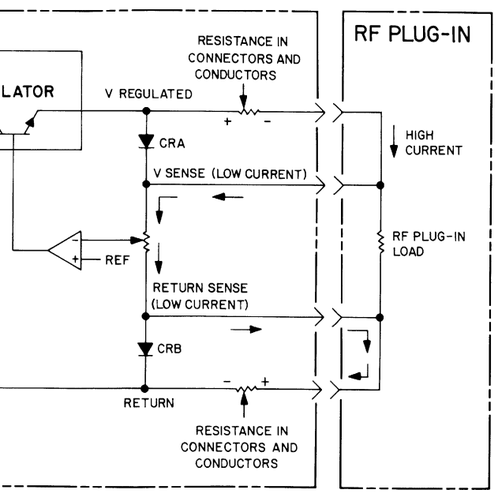

t Regulated Power Supply, Simplified Schematic

the primary of T1 through Power Line Module FL1,
ge Selector PC board. The voltage selector board is positioned to provide correct power connections to T1 for operation with line voltages of 100 Vac, 120 Vac, 220 Vac, or 240 Vac. (See Figure 2-1 for correct installation of the Line Voltage Selection PC board.)

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NOTE

All power supply circuit descriptions include the unregulated (A6 Rectifier) and regulated (A7 Regulator) sections of the supply.

Table 8-30. Power Supply Distribution

Power Supply	Distribution
+20V	RF Plug-in
+15V	A4, A5, RF Plug-in
+10V	RF Plug-in
+5VA	A2, A3, A4, A5, A6, A8, J13
+5VAFP	A1
+5VB	RF Plug-in
−10V	RF Plug-in
−15V	A4, A5, RF Plug-in
−40V	RF Plug-in

+20V Power Supply

+20V Unregulated. The approximately 26 Vac T1 output is rectified by full-wave bridge rectifer A6CR1−4. A6C1 and A6C12 filter switching transients, and A9C6 filters ac line ripple.

+20V Regulator. Regulation is provided by 3-terminal regulator A7U7. Error amplifier A7U8 improves regulation by controlling the reference voltage to the regulator A7U7 pin 1. Under normal operating conditions, the voltage difference between the regulator output and its reference input is about 1.25V. Zener diode VR2 provides a stable reference voltage to the noninverting input of A7U8. The +20V output is scaled by the voltage divider consisting of A7R9, A7R10 (+20V ADJ potentiometer), and A7R11, and is applied to the inverting input of U8. Since error amplifier U8 drives the regulator to balance its inputs, the power supply stability is a direct function of the reference voltage stability. When an RF plug-in is installed, the voltage divider is connected across the +20V SENSE and +20V RET SENSE (+20V Return Sense) inputs from the RF Plug-in. Any change in the +20V regulated supply or current return in the RF plug-in is sensed by A7U8, which generates an error signal to A7U7 to maintain the voltage constant. When the RF Plug-in is not installed, diodes A7CR9 and A7CR10 conduct to connect the +20V REG and +20V RET lines across the voltage divider. This results in two diode-drops being added to the voltage divider, with a corresponding increase in the power supply output voltage. If the +20V supply turns off, then +10V, −10V, and −40V supplies are automatically turned off.

Voltage regulator A7U7 has overcurrent protection. If the supply is shorted to ground, A7U7 will go into a current limit foldback condition, limiting the current. Fuse A7F5 protects the +20V loads in case the +20V regulator fails. Overvoltage protection is provided by crowbar circuit A7U6. If the power supply output is greater than approximately +23V, A7U6 turns on, shorting the +20V supply to ground and causing regulator A7U7 to current limit. If the regulator is defective, fuse A7F5 provides overcurrent protection. A7CR1, A7VR1, and A7R6 protect regulator A7U7 from positive transients on the +20V output. LED A7DS2 provides a power on indication when the output voltage exceeds approximately +18V. Diode A7CR18 provides reverse voltage protection.

±15V Power Supplies

±15V Unregulated. The two ac outputs of the T1 center-tapped secondary (approximately 20Vac) are applied to full-wave bridge rectifier A6CR5−8. The rectifier provides both a +15V and −15V output that is referenced to the T1 center-tap (system ground). Fuses A6F1 and A6F2 provide overcurrent protection. A6C2 and A6C3 filter switching transients, and A9C2 and A9C3 filter ac line ripple.

+15V Regulator. Three-terminal regulator A7U13 provides regulation and current limiting. The actual voltage output is greater than +15V due to CR16 on the reference input of the regulator. Crowbar circuit A7U12 provides overvoltage protection. If the power supply output exceeds approximately +17V, A7U12 turns on, shorting the +15V supply to ground, and causing regulator A7U13 to current limit. LED A7DS6 provides a power on indication when the output voltage exceeds approximately +12V. Diode A7CR23 provides reverse voltage protection.

−15V Regulator. Regulation is provided by three-terminal regulator A7U15. The regulator output voltage is determined by the voltage across A7R85 and current through A7R86. Diode A7CR26 protects the regulator if the −15V UNREG input is shorted to ground. Overvoltage protection is provided by crowbar circuit A7U14. If the power supply output exceeds approximately −17V, A7U14 turns on, shorting the −15V supply to ground, and causing the regulator to current limit. LED A7DS7 provides a power on indication when the power supply exceeds approximately −12V. Diode A7CR17 provides reverse voltage protection.

±10V Power Supplies

±10V Unregulated. The two ac outputs of the T1 center-tapped secondary (approximately 16 Vac) are applied to full-wave bridge rectifier A6CR9−12. The rectifier provides both a +10V and −10V unregulated output that is referenced to the T1 center-tap (which is isolated from system ground by A6R11). A6C4 and

A5

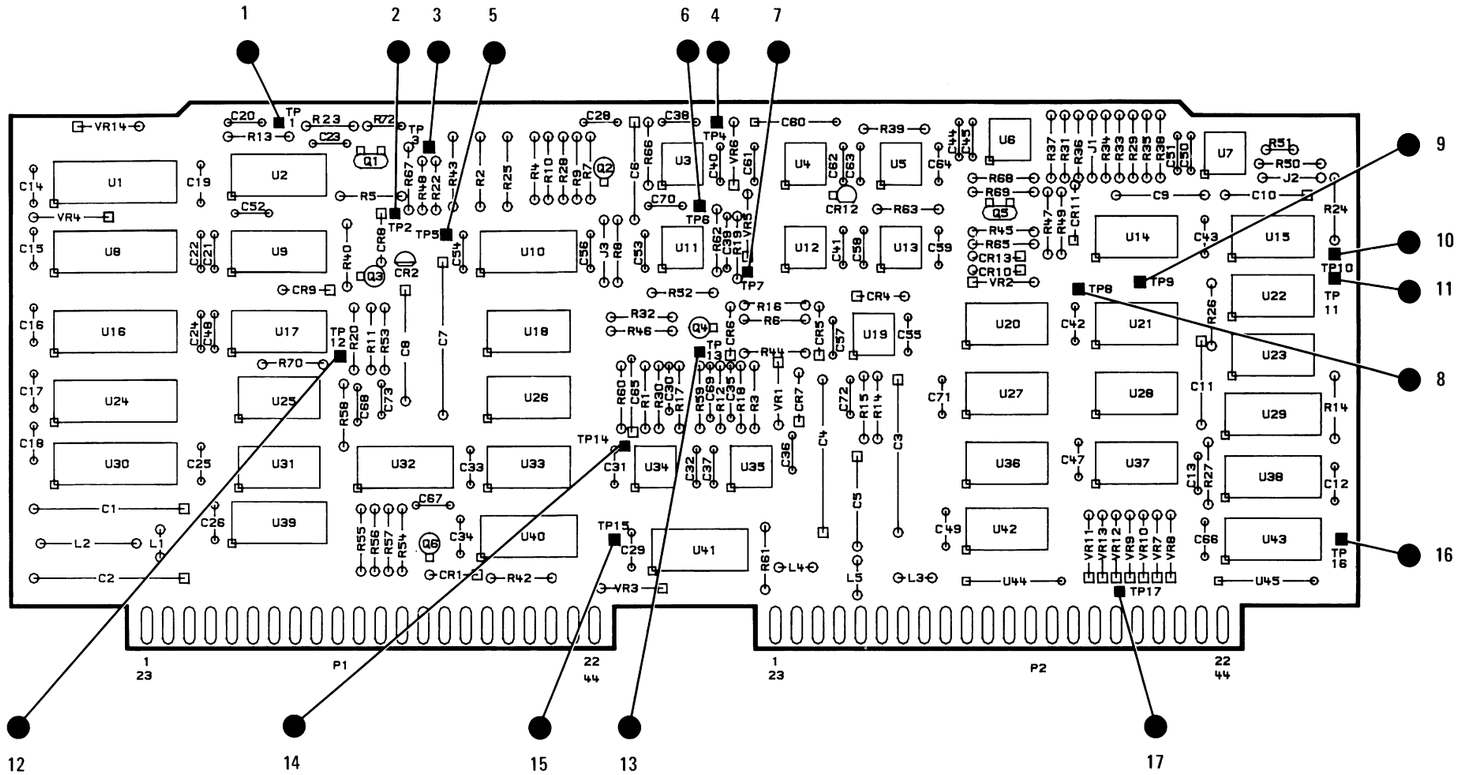


Figure 8-45. A5 Sweep Generator, Component Locations

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◄ ► TO STEP TO THE NEW ADDRESS.

2. IF THE POSITION OF JUMPER A5J1 IS CHANGED, A5R51 MOD FREQ POTENTIOMETER MUST BE READJUSTED. SEE SECTION V FOR THE ADJUSTMENT PROCEDURE.

A5P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1	GND DIG			M
23	GND DIG			M
2	GND ANLG			M
24	GND ANLG			M
3	+5VA	IN	A7P1-2, 24	M
25	+5VA	IN	A7P1-2, 24	M
4	+5VA	IN	A7P1-2, 24	M
26	+5VA	IN	A7P1-2, 24	M
5	GND DIG			M
27	GND DIG			M
6	ID0	IN	A3P1-28	B
28	ID1	IN	A3P1-29	B
7	ID2	IN	A3P1-30	B
29	ID3	IN	A3P1-31	B
8	ID4	IN	A3P1-32	B
30	ID5	IN	A3P1-33	B
9	ID6	IN	A3P1-34	B
31	ID7	IN	A3P1-35	B
10	GND DIG			M
32	GND DIG			M
11	GND ANLG			M
33	L ALTE	OUT	J13-17, J14-2	C
12	GND ANLG			M
34	ALT1	OUT	J13-4, J14-1	C
13	L I/OSTB	IN	A3P1-37	A
35	GND DIG			M
14	I/OE2	IN	A3P1-16	NOT USED
36	GND DIG			M
15	I/OE1	IN	A3P1-17	A
37	L IRD	IN	A3P1-39	NOT USED
16	L IA0	IN	A3P1-18	A
38	GND DIG			M
17	L IA2	IN	A3P1-19	A
39	L IA1	IN	A3P1-41	A
18	L IA4	IN	A3P1-20	A
40	L IA3	IN	A3P1-42	A
19	EXT TRG	IN	J13-9	E
41	GND DIG			M
20	VRAMP	OUT	A4P1-20	G
42	L CNTR	OUT	J2-22, J9	I
21	VSW1	OUT	A4P1-20	G
43	N.C.			
22	GND ANLG			M
44	GND DIG			M

A5P2

PIN	SIGNAL	I/O
1	GND ANLG	
23	GND ANLG	
2	VSW2	I/O
24	VSW	OUT
3	N.C.	
25	L REMTRG	IN
4	−15V	IN
26	−15V	IN
5	SYNC TRG	OUT
27	L AMK	IN
6	L MK	IN
28	L SW	OUT
7	+10V REF	IN
29	+10V REF	IN
8	+15V	IN
30	+15V	IN
9	GND DIG	
31	GND DIG	
10	GND DIG	
32	GND DIG	
11	L BP2	OUT
33	L ZMRQ	IN
12	NZAB	OUT
34	PZAB	OUT
13	L MUTE	OUT
35	L PL	OUT
14	L MP	OUT
36	L BP1	OUT
15	L LINETRG	IN
37	SQ MOD	OUT
16	L PLRQ	IN
38	L MKRQ	IN
17	L RFBRQ	IN
39	L SSRQ	IN
18	L RTS	OUT
40	L BPRQ	IN
19	L RTS	OUT
41	L SFSRQ	IN
20	L RFM	OUT
42	L RFB	OUT
21	GND DIG	
43	GND DIG	
22	GND ANLG	
44	GND ANLG	

	I/O	TO/FROM	FUNCTION
			M M
	I/O OUT	J1, J8 J2-64	G G
	IN	A8P1-3	E
	IN IN	A7P1-14, 36 A7P1-14, 36	M M
	OUT IN	J13-24 A4P2-27	K I
	IN OUT	A4P2-6 A2P1-44	K K
	IN IN	A4P2-7, 29 A4P2-7, 29	M M
	IN IN	A7P1-8, 30 A7P1-8, 30	M M
			M M
			M M
	OUT IN	A4P2-33, J2-53 J2-23	K K
	OUT OUT	J6 J5	L L
	OUT OUT	J13-11 A6P1-25	K K
	OUT OUT	J13-2 J13-14	K K
	IN OUT	A6P1-24 J2-26	E I
	IN IN	J13-3 J13-15	K K
	IN IN	J2-54, J13-8 J2-32, J13-18	K D
	OUT IN	A2P1-42, J2, J13, J14 J2-55, J13-20	K K
	OUT IN	A2P1-42, J2, J13, J14 J13-5, J10	K D, I
	OUT OUT	J2-24 J2-56, J13-7	K K
			M M
			M M

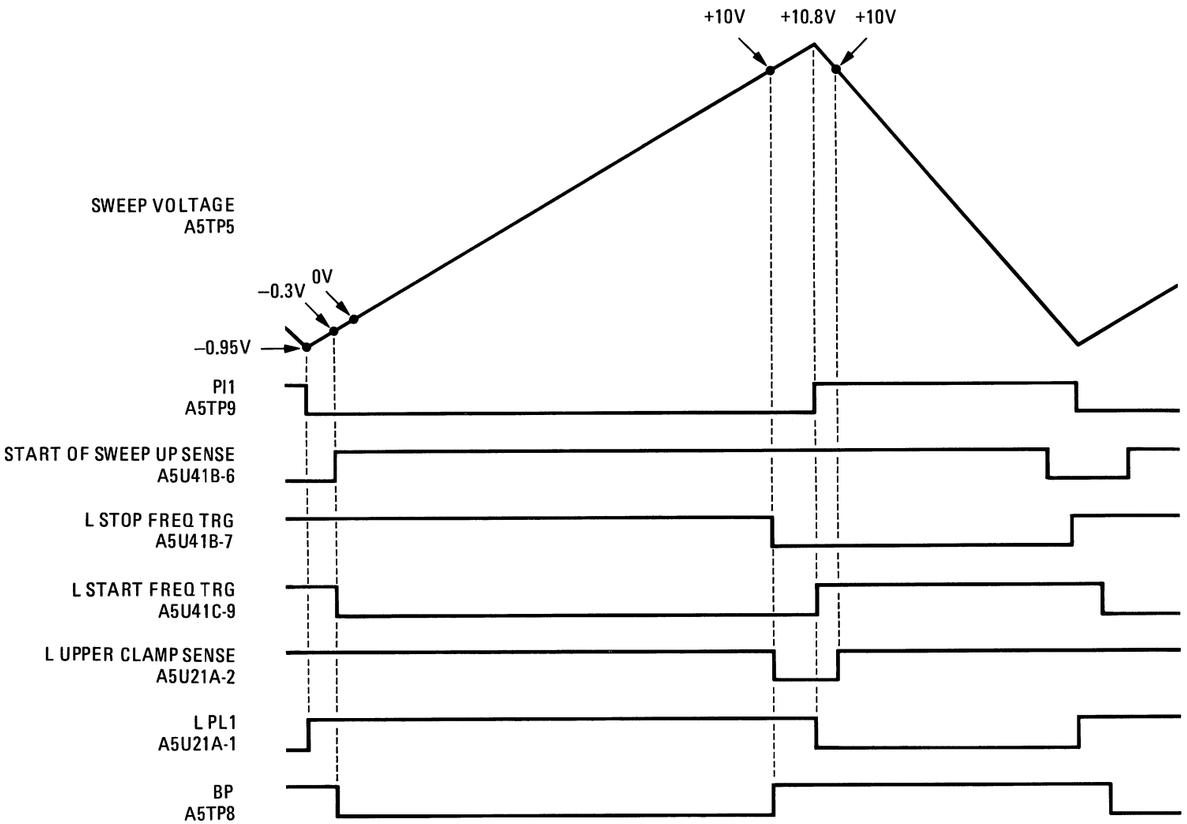


Figure 8-46. Sweep Ramp Status Timing Diagram

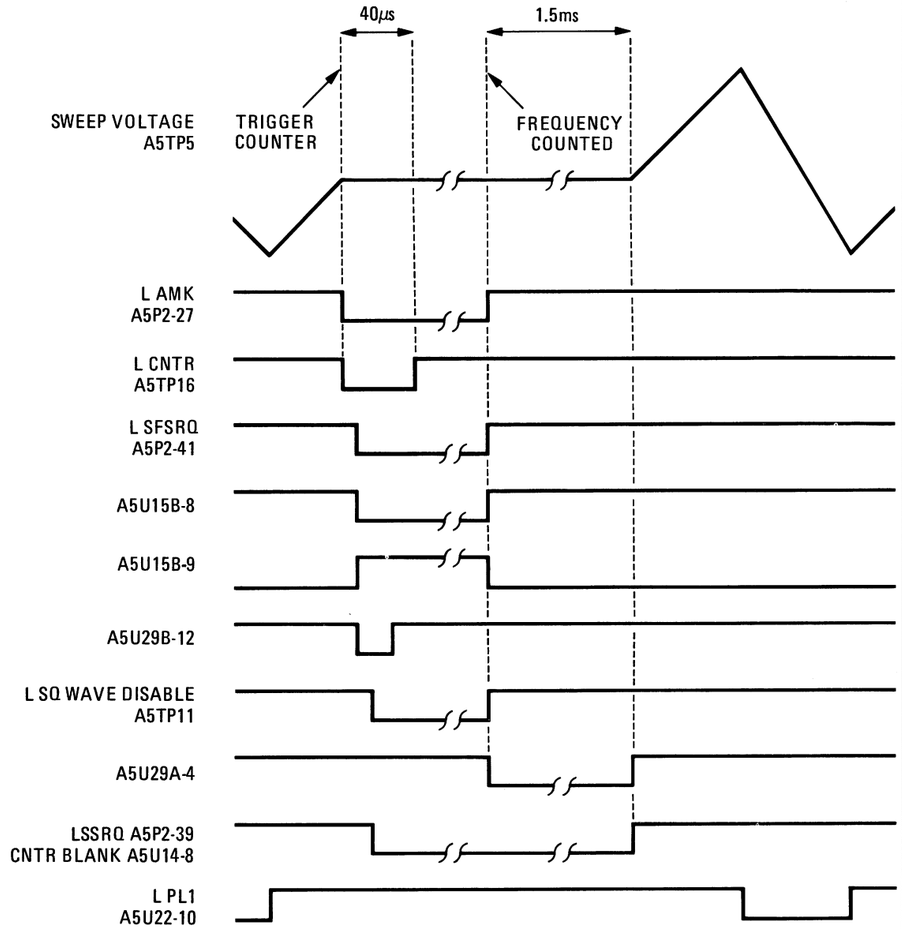


Figure 8-47. Counter Interface Timing Diagram

A6C5 filter switching transients, and A9C1 and A9C4 filter ac line ripple.

+10V Regulator. Regulation is provided by three-terminal regulator A7U5. The regulator output voltage is determined by the voltage drop across A7R45 and current through A7R46. Diode A7CR6 protects the A7U5 regulator if the +10V UNREG input is shorted to ground. Overvoltage protection is provided by crowbar circuit A7U4. If the power supply output exceeds approximately +13.7V, A7U4 turns on, shorting the +10V supply to ground, and causing regulator A7U5 to current limit. LED A7DS5 provides a power on indication when the power supply exceeds approximately +8V. Diode A7CR20 provides reverse voltage protection. If the +20V power supply is off, A7CR7 biases on to turn off the +10V supply.

−10V Regulator. Operation of the −10V Regulator is similar to the +20V Regulator. Adjustable three-terminal regulator A7U3 and error amplifier A7U2 provide the voltage regulation. Voltage divider A7R23, A7R22, A7R21 (−10V ADJ potentiometer), and A7R20 uses the +20V SENSE line as the reference voltage. The −10V supply is automatically turned off by Q1 if the +20V supply is missing.

−40V Power Supply

−40V Unregulated. The approximately 47 Vac T1 output is rectified by full-wave bridge rectifier A6CR15−18. A6C8 and A6C14 filter switching transients, and A9C7 filters ac line ripple.

−40V Regulator. The −40V Regulator operation is similar to the +20V regulator except that the regulator consists of discrete components (A7Q6−8) and, for improved reliability, the return side of the unregulated supply is regulated. The −40V output is common with −40V output of the Unregulated supply.

A7Q6 is a series pass regulator with A7R29 functioning as the current sense resistor for foldback current limit transistor A7Q7. Error amplifier U19 controls the series pass base drive through A7Q8 to maintain a regulated −40V. The positive error amplifier input is scaled by the voltage divider consisting of A7R37−40. A7R39 is adjusted for −40V in the RF Plug-in. The voltage divider is normally connected across the +20V SENSE and −40V SENSE inputs from the RF Plug-in. However, if the RF Plug-in is not installed, diodes A7CR11 and A7CR12 (in the +20V Regulator) conduct to connect the voltage divider across the −40V regulator output and +20V regulator output. Overvoltage protection is provided by a crowbar circuit (A7Q5, A7VR5). If the power supply output exceeds approximately −43V, zener diode VR5 turns on and switches SCR Q5 on, shorting the −40V supply to ground, and causing the −40V supply to current limit. Diode A7CR8 provides reverse voltage protection.

+5V Power Supply

+5V Unregulated. The two ac outputs of the T1 center-tapped secondary are half-wave rectified by diodes A6CR13 and A6CR14. A6C6 and A6C7 filter switching transients, and A9C5 filters ac line ripple.

+5V Regulators. The +5V UNREG from the A6 Rectifier is applied to two regulators. The A7U16 regulator output at A7TP1 is used only in the 8350A. The A7U10 regulator output at A7TP2 is used only by the RF plug-in. Each power supply output is provided overvoltage protection by crowbar circuits A7U9 and A7U18. Diodes A7CR21 and A7CR22 provide reverse voltage protection. Power on indication for each supply is provided by A7DS1 and A7DS8.

Three-terminal regulator A7U16 provides regulation and current limiting for the +5VA and +5VAFP supply outputs. Regulation for the +5VB output is provided by three-terminal regulator A7U10. The regulator output voltage is determined by the voltage drop across A7R1 and current through parallel resistors A7R2 and A7R76. A7R76 is factory selected for a +5.3V output at A7TP2. The extra 0.3V ensures sufficient voltage level at the RF plug-in. A7CR24 provides noise isolation between +5VB GND REF and GND DIG.

Penlift A6: (F)

The Penlift circuit controls the Penlift solenoid in the X-Y Recorder to raise or lower the pen. When L PL (Low=Penlift) from the A5 Sweep Generator goes active low, A6Q1 and A6Q2 turn off, deactiviting the penlift solenoid in the plotter or recorder. When L PL goes high, A6Q1 and A6Q2 are turned on, grounding the penlift solenoid, and causing the pen to set down. The Q2 collector voltage of about +40V is supplied through the Penlift solenoid by the plotter or recorder. A6VR2 provides overvoltage protection.

Power-up Circuit A6: (G)

The Power-up circuit provides the PWON output (Power On) that goes high after the +5VA supply reaches +5VA at initial power on. PWON goes low when power is removed, but before the +5VA supply begins to drop. When low, the PWON output resets the microprocessor and initializes the 8350A. Diodes CR19 through CR24 rectify the T1 secondary output. At initial power on, A6Q4 is biased on by A6R4 and A6R5. A6C10 charges to about +8V and biases A6CR21 and A6CR24 off. The voltage at the noninverting input of comparator A6U1 rises immediately to about +2.4V. The voltage rise at the inverting input of comparator U1 is much slower, since A6C11 must charge through A6R1, A6R2, and CR23. Therefore, the U1 output is initially high which keeps A6Q4 biased on. After the +5VA supply reaches +5V, and A6C11 is fully charged, the voltage level at the A6U1 inverting input is about +2.6V. The U1 output goes low and turns off A6Q4 to switch the PWON output high.

When power is removed, A6C10 discharges quickly through A6R12. A6CR21 turns on and the voltage level at the U1 inverting input decreases. This results in a high A6U1 output that turns on A6Q4 and switches the PWON output low before the +5VA supply starts to decrease. This disables all activity on the A3 Microprocessor before the +5VA supply is able to turn off. This is important for option 001 (nonvolatile memory) instruments to ensure that none of the data stored in RAM is altered or lost when power is turned off.

When power is turned off, A6CR24 provides a discharge path for A6C11. A6R6 provides some hysteresis when the comparator output changes states.

Line Trigger A6: (H)

The Q3 base is connected through R8 to the 5V secondary winding of T1. CR22 clips the negative half of the 60 Hz sine wave, and Q3 amplifies and inverts the clipped sine wave to provide a square wave output to the A5 Sweep Generator. The Q3 collector is connected to +5V through a resistor on the A5 Sweep Generator.

Power Supply Failure Detection A7: (A)

The Power Supply Failure Detection circuit provides an active low L PSF

(Low=Power Supply Failure) output if any of the regulated power supplies fail (except +5VA, which is monitored by the Power-up circuit). The positive regulated power supply outputs are connected through a voltage divider to the noninverting input of comparator A7U17. The negative regulated supplies are connected through a voltage divider with the +5VA regulated supply to the inverting input of A7U17. Under normal operating conditions, the noninverting comparator input is more positive. If a power supply fails, the inverting comparator input goes more positive, and the comparator output, L PSF (Low = Power Supply Fail) goes active low.

Air Flow Detection A7 (B)

The Air Flow Detection circuit senses the internal air flow generated by fan B1, and flags the A3 Microprocessor if the air flow is restricted. This results in error message E016 being displayed on the front panel FREQUENCY display, but does not disable the instrument.

AIR FLOW BAL potentiometer A7R58 is adjusted to balance the voltage levels of the two A7U11 comparator inputs under conditions of normal airflow. Transistor A7Q4 is always biased on, and, through a heatsink, acts as a heater for A7Q3. The efficiency of Q4 as a heater is directly dependent on airflow across the heatsink. If the airflow is restricted, A7Q3 is heated by A7Q4, and the A7Q3 base-emitter voltage drop decreases. This unbalances the bridge network, and the inputs to A7U11 are unbalanced, causing the A7U11 output (L PST) to go active low and flag the A3 Microprocessor. Since the microprocessor reads the flag only once every 10 minutes, the Air Flow error code (E016) is not immediately displayed.

A7C35 prevents the comparator from triggering for transients. Resistor A7R28 provides some hysteresis once the comparator is triggered.

Troubleshooting

The regulators for the +20V, +10V, +5VB, −10V, and −15V power supplies are operating properly if the voltage difference between the regulated output and error voltage input pins is about 1.25 Vdc. If the output voltage is low, and the above voltage difference exists, the problem is either the crowbar circuit or the load, which is causing the regulator to current limit.

Table 8-31 lists each regulated supply with its voltage limits. Test points for the voltage and return connections are provided for either an 83500 series RF plug-in or an 11869A Adapter/86200 series RF plug-in installed. The +20V, −10V, −40V, and +5VB supplies are adjustable. If these supplies are not within the limits, refer to Section V, before further troubleshooting.

The logic state of the Airflow Detection circuit output (L PST) is monitored by the A3 Microprocessor, and stored in the Status Buffer at hexadecimal address location 1000. The Status Buffer data is displayed on the front panel FREQUENCY/ TIME display when the following key sequence is entered.

SHIFT 0 0 MI 1 0 0 0 M3

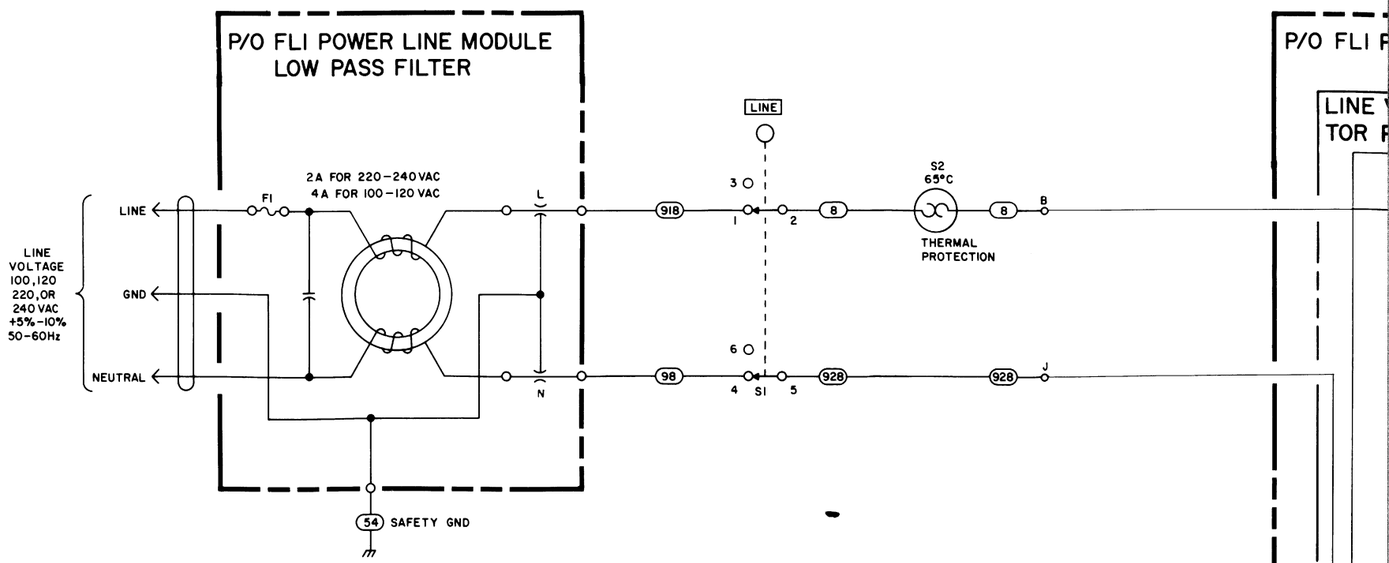
The FREQUENCY/TIME display should indicate 02 if L PST is active low, and 00 if L PST is high. Jumper A7TP4 to A7TP5; the FREQUENCY/TIME display should cycle between 00 and 02. If the display does not cycle, refer to the Airflow adjustment procedure in Section V.

A6P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1	GND DIG			I
23	+5VA	IN	A7P1-2, 24	I
2	PWON	OUT	DIST.	G
24	L LINETRG	OUT	A5P2-15	H
3	PL	OUT	J7, J13-10	F
25	L PL	IN	A5P2-35	F
4	–40V	OUT	A7P1-20	E
26	–40V	OUT	A7P1-20	E
5	–40V UNREG RET		A7P1-43	E
27	–40V	OUT	A7P1-20	E
6	–40V UNREG RET		A7P1-43	E
28	–40V UNREG RET		A7P1-43	E
7	+20V UNREG	OUT	A7P1-18, 40	A
29	+20V UNREG	OUT	A7P1-18, 40	A
8	+20V UNREG	OUT	A7P1-18, 40	A
30	+20V UNREG	OUT	A7P1-18, 40	A
9	+20V RET		A7P1-15	A
31	+20V RET		A7P1-15	A
10	+20V RET		A7P1-15	A
32	+20V RET		A7P1-15	A
11	+5V RET			D
33	+5V RET			D
12	+5V RET			D
34	+5V RET			D
13	+5V UNREG	OUT	A7P1-3, 26	D
35	+5V RET			D
14	+5V UNREG	OUT	A7P1-3, 26	D
36	+5V UNREG	OUT	A7P1-3, 26	D
15	+5V UNREG	OUT	A7P1-3, 26	D
37	+5V UNREG	OUT	A7P1-3, 26	D
16	–10V UNREG	OUT	A7P1-42	C
38	–10V UNREG	OUT	A7P1-10, 32	C
17	±10V RET		A7P1-13, 35	C
39	±10V RET		A7P1-13, 35	C
18	±10V RET		A7P1-13, 35	C
40	±10V RET		A7P1-13, 35	C
19	+10V UNREG	OUT	A7P1-42	C
41	+10V UNREG	OUT	A7P1-42	C
20	–15V UNREG	OUT	A7P1-37	B
42	–15V UNREG	OUT	A7P1-37	B
21	±15V RET			B
43	±15V RET			B
22	+15V UNREG	OUT	A7P1-29	B
44	+15V UNREG	OUT	A7P1-29	B

NOTES

1. SWITCH CONNECTIONS SHOWN ARE ACTUALLY CONNECTIONS THAT ARE DETERMINED BY LINE VOLTAGE SELECTOR PC BOARD POSITIONING. BOARD POSITION SHOWN IS FOR 120 VAC LINE VOLTAGE. INSTRUCTIONS FOR LINE VOLTAGE SELECTION ARE PROVIDED IN SECTION II, INSTALLATION.
2. SEE A7 REGULATOR SERVICE SHEET FOR A6/A7 BLOCK DIAGRAM.



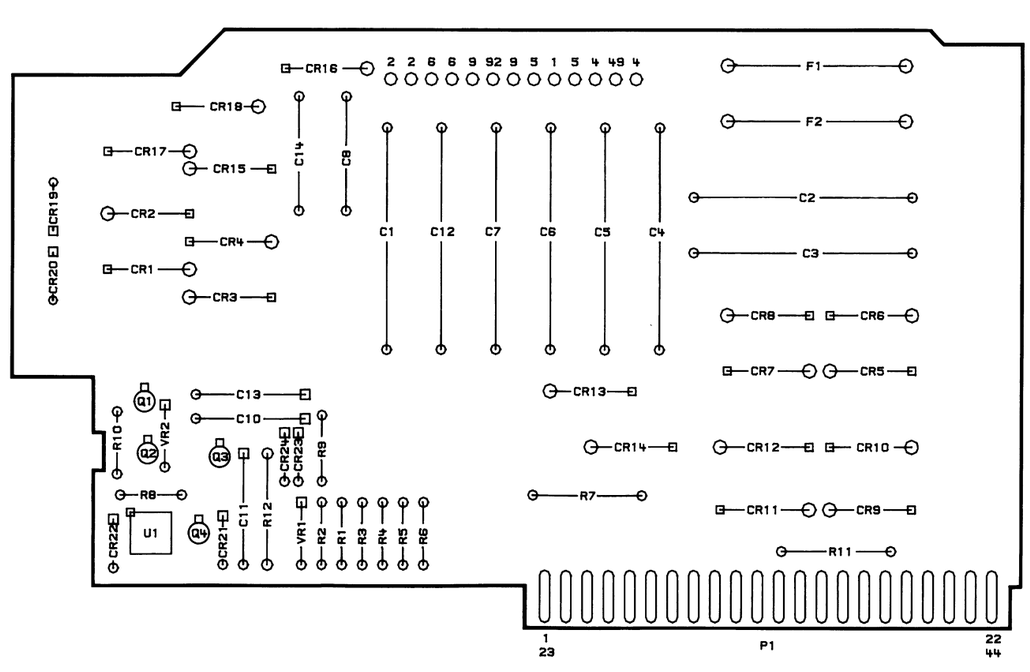


Figure 8-49. A6 Rectifier, Component Locations

SERIAL PREFI

NE MODULE
LTER

VAC
VAC

TY GND

LINE

L

N

3

1

2

6

4

S1

5

S2
65°C

THERMAL
PROTECTION

918

8

8

B

98

928

928

J

P/O FLI POWER LINE MODULE

LINE VOLTAGE SELEC-
TOR PC BOARD

120/240

100/220
NOTE 1

100/120

220/240
NOTE 1

100/120

220/240
NOTE 1

C

A

E

D

F

T1

0

3

958

E1

958

B1

948

948

04

05

02

F1

F2

C2

C3

CR8

CR6

CR7

CR5

CR12

CR10

CR11

CR9

R11

P1

22
44

A6 RECTIFIER
08350-60026

Ⓐ +20V UNREG

6

6

C1
.47

C12
.47

CR1

CR2

CR3

CR4

R7
51.1

6

Ⓑ ± 15V UNREG

4

94

4

F1
2A

F2
2A

C2
.47

C3
.47

CR5

CR6

CR7

CR8

Ⓒ ± 10V UNREG

5

1

5

C4
.47

C5
.47

CR9

CR10

CR11

CR12

R11
51.1

6

Ⓔ −40V UNREG

2

2

C8
0.1

C19
0.1

CR14

CR16

CR17

CR18

Ⓓ +5V UNREG

9

92

9

C6
.47

C7
.47

CR13

CR14

6

P/O A9 MOTHERBOARD

7,8,
29,
30

9,10,
31,
32

+20V UNREG
TO
A7 REGULATOR
P1-18,40

C6
7200

+20V RET
TO
A7 REGULATOR
P1-15

21,
43

22,
44

20,
42

±15V RET
TO
SYSTEM
GROUND

C3
3600

+15V UNREG
TO
A7 REGULATOR
P1-29

C2
3600

−15V UNREG
TO
A7 REGULATOR
P1-37

17,18,
39,
40

19,
41

16,
38

±10V RET
TO
A7 REGULATOR
P1-13,35

C1
3600

+10V UNREG
TO
A7 REGULATOR
P1-42

C4
8700

−10V UNREG
TO
A7 REGULATOR
P1-10,32

5,6,
28

4,26,
27

−40V UNREG RET
TO
A7 REGULATOR
P1-43

C7
2600

−40V REG
TO
A7 REGULATOR
P1-20

13,
14,
15,
36,
37

11,12,
33,
34,
35,

+5V UNREG
TO
A7 REGULATOR
P1-3,26
+5V RET

C5
45000

SYSTEM
GROUND

1

6

P1-2

G

P1-

ocations

SERIAL PREFIX: 2024A

R LINE MODULE

AGE SELEC-
OARD

240
220
E 1

/120
/240
E 1

/120
/240
E 1

24A

A8 RECTIFIER
08350-60026

T1

Ⓐ +20V UNREG

C1 .47
C12 .47
CR1 CR2 CR3 CR4
R7 51.1

Ⓑ ± 15V UNREG

F1 2A
F2 2A
C2 .47
C3 .47
CR5 CR6 CR7 CR8

Ⓒ ± 10V UNREG

C4 .47
C5 .47
CR9 CR10 CR11 CR12
R11 51.1

Ⓔ −40V UNREG

C8 0.1
C19 0.1
CR14 CR16 CR17 CR18

Ⓓ +5V UNREG

CR13
C6 .47
C7 .47
CR14

P/O A9 MOTHERBOARD

+20V UNREG TO A7 REGULATOR PI-18,40
C6 7200
+20V RET TO A7 REGULATOR PI-15

±15V RET TO SYSTEM GROUND
C3 3600
+15V UNREG TO A7 REGULATOR PI-29
C2 3600
−15V UNREG TO A7 REGULATOR PI-37

±10V RET TO A7 REGULATOR PI-13,35
C1 3600
+10V UNREG TO A7 REGULATOR PI-42
C4 8700
−10V UNREG TO A7 REGULATOR PI-10,32

−40V UNREG RET TO A7 REGULATOR PI-43
C7 2600
−40V REG TO A7 REGULATOR PI-20

+5V UNREG TO A7 REGULATOR PI-3,26 +5V RET
C5 45000
SYSTEM GROUND

Ⓘ POWER SUPPLY

PI-23 (IN) +5VA
C13 10
PI-1 GND DIG

Ⓕ PENLIFT CIRCUIT

PI-25(IN) LPL
R9 10K
+5VA
Q1
Q2
R10 100K
VR2 46.4V
PI-3(OUT) PL

Ⓗ LINE TRIGGER CIRCUIT

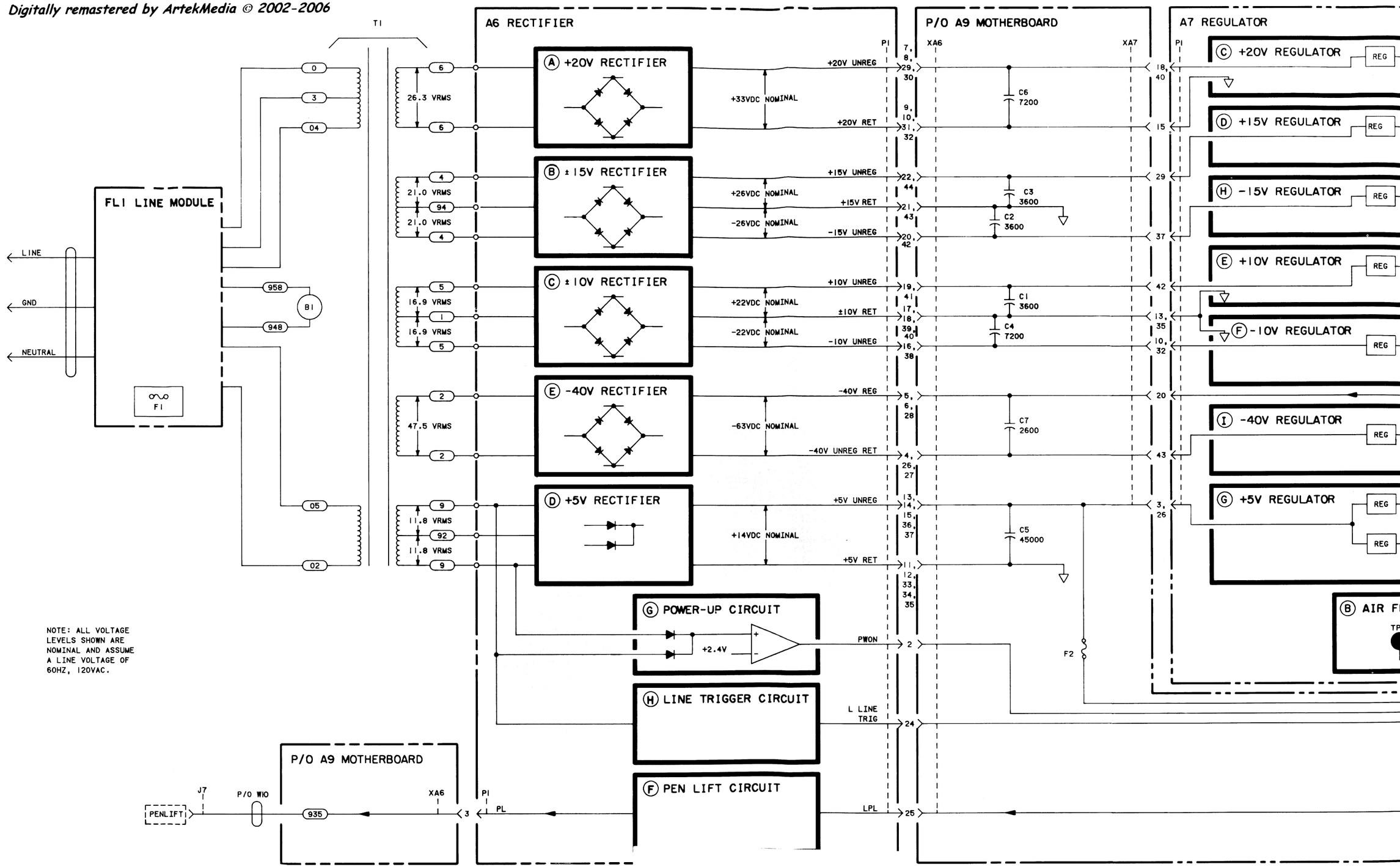
R8 10K
Q3
CR22
PI-24(OUT) L LINE TRIG

Ⓖ POWER-UP CIRCUIT

CR20
CR19
C10 10
CR21
CR24
R12 511
CR23
C11 10
+5VA
R1 9090
R3 147
R2 10K
VR1 2.37V
U1
R6 464K
R4 10K
R5 2150
Q4
PI-2(OUT) PWON

A6

Figure 8-50. A6 Rectifier, Schematic Diagram



NOTE: ALL VOLTAGE LEVELS SHOWN ARE NOMINAL AND ASSUME A LINE VOLTAGE OF 60HZ, 120VAC.

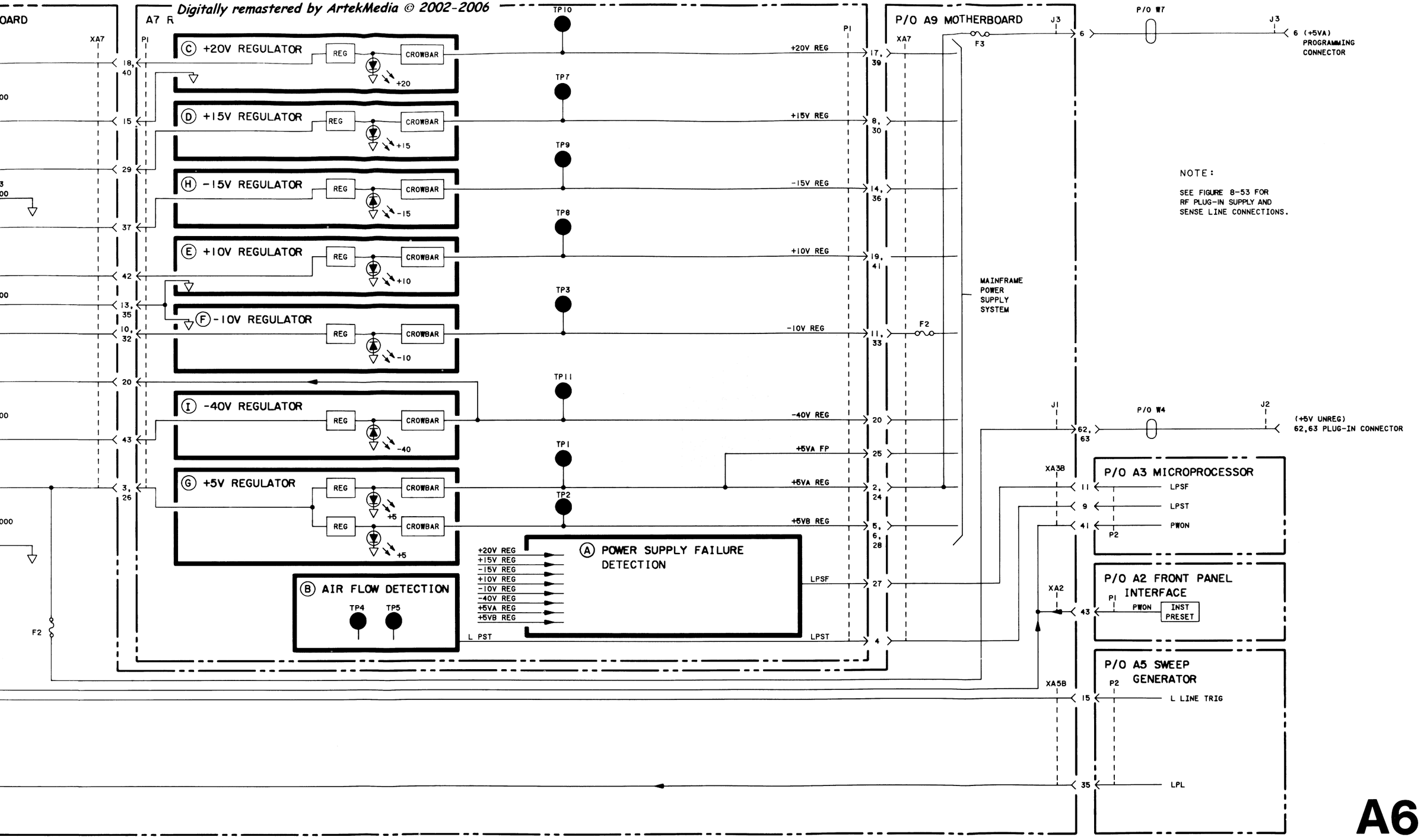
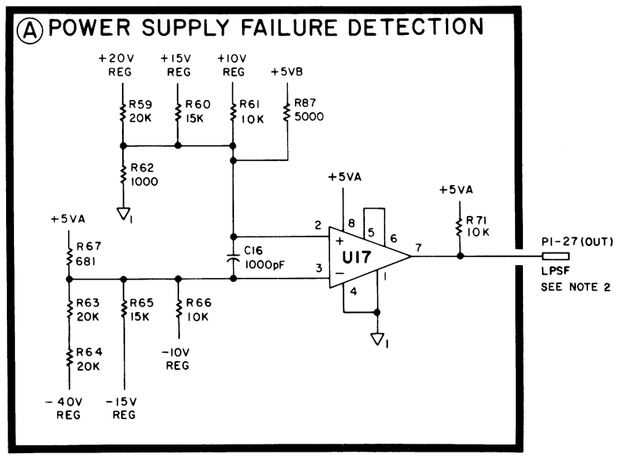
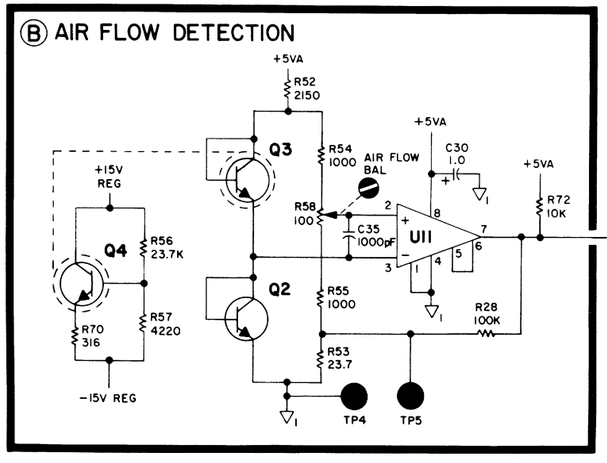


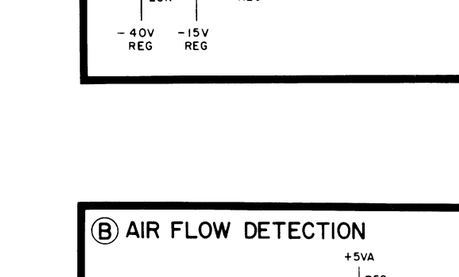
Figure 8-51. A6 Rectifier/A7 Regulator, Block Diagram

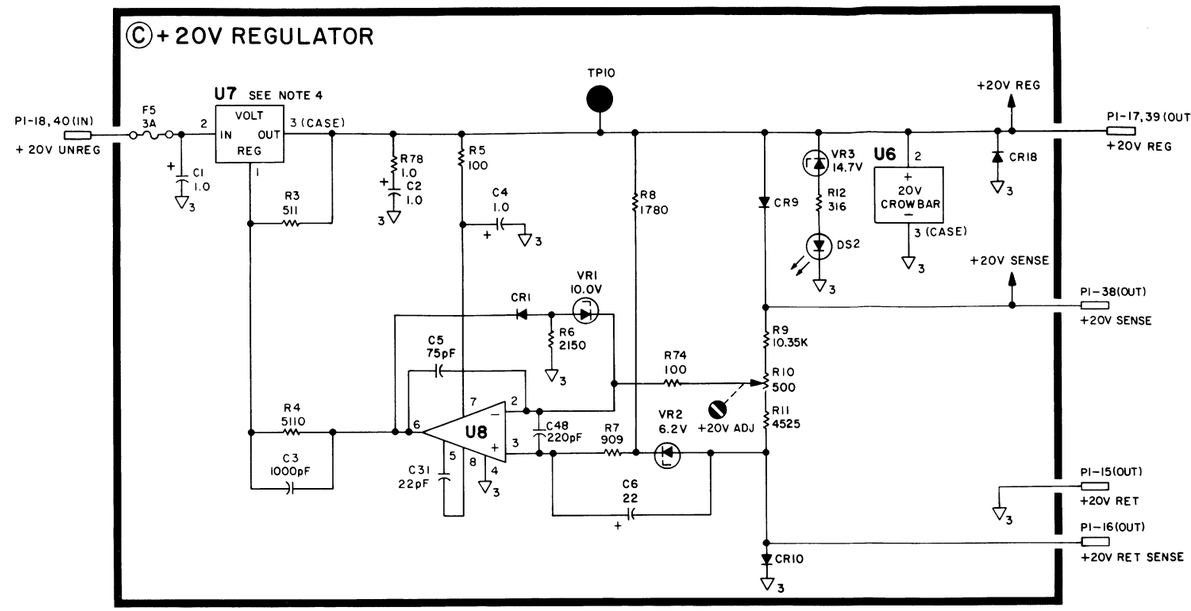
Figure 8-54. A7 Regulator, Schematic Diagram

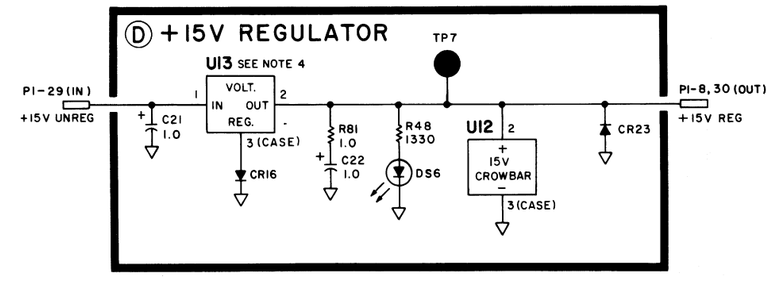
A7 REGULATOR
08350-60027

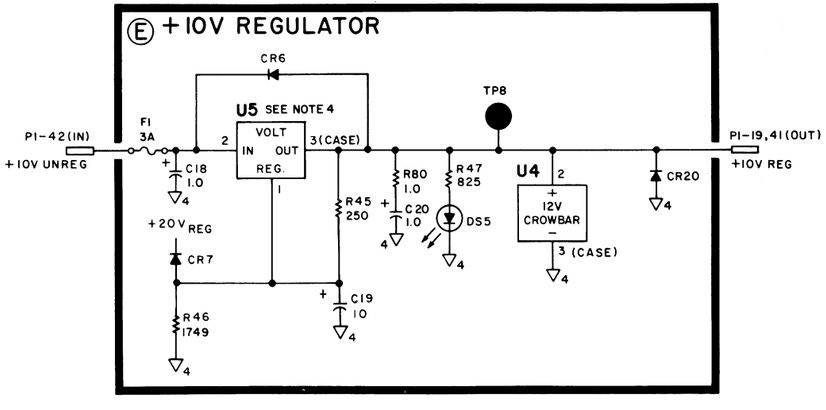












SERIAL PREFIX: 2024A

LATOR

TE 4

(CASE)

R78 1.0 C2 1.0

R5 100

C4 1.0

TP10

R8 1780

VR1 10.0V

CR1

C5 75pF

R6 2150

R74 100

VR2 6.2V +20V ADJ

U8

C48 220pF

R7 909

C31 22pF

C6 22

CR9

VR3 14.7V

R12 316

DS2

U6 20V CROWBAR

+20V REG

CR18

PI-17,39 (OUT) +20V REG

+20V SENSE

PI-38(OUT) +20V SENSE

R9 10.35K

R10 500

R11 4525

PI-15(OUT) +20V RET

PI-16(OUT) +20V RET SENSE

CR10

ULATOR

TP7

R81 1.0 C22 1.0

R48 1330

DS6

U12 15V CROWBAR

3(CASE)

CR23

PI-8,30 (OUT) +15V REG

LATOR

OTE 4

3(CASE)

TP8

R45 250

R80 1.0 C20 1.0

R47 825

DS5

U4 12V CROWBAR

3 (CASE)

CR20

PI-19,41(OUT) +10V REG

C19 10

Ⓖ +5V REGULATORS

PI-3,26(IN) +5V UNREG

F3 8A

C25 1.0

U16 SEE NOTE 4 VOLT IN OUT REG.

3 (CASE)

TP1

R83 1.0 C26 1.0

R50 316

DS8

U18 SEE NOTE 4 5V CROWBAR

CR21

PI-25 (OUT) +5VA FP

PI-2,24 (OUT) +5VA REG SEE NOTE 1

CR3

U10 SEE NOTE 4 VOLT IN OUT REG.

F2 5A

C27 1.0

TP2

R1 237

R84 1.0 C28 1.0

R51 316

DS1

U9 5V CROWBAR

CR22

PI-5,6,28 (OUT) +5VB REG

PI-7 (IN) +5VB GND REF

CR24

R76 * 4640

R2 909

C36 10

Ⓕ −10V REGULATOR

+20V REG

R15 19.6K

R16 10K

Q1

C9 2200pF

R14 5110

R19 100 C12 1.0

U2

C33 22pF

C47 220pF

C11 75pF

R33 2150

CR14

C42 1.0

PI-12(OUT) −10V RET SENSE

PI-13,35(OUT) ± 10V RET

+20V SENSE

R23 4000

R22 4000

R21 50

R20 4000

R42 10K

C45 10

VR4 10.0V

CR2

R73 100

R18 2150

−10V ADJ

R13 511

C10 1.0

R17 100

CR25

U3 VOLT IN OUT REG

SEE NOTE 4

PI-34(OUT) −10V SENSE

CR13

C41 10

PI-10,32 (IN) −10V UNREG

F4 3A

C7 1.0

C8 1.0 R77 1.0

DS3

R24 825

CR19

U1 12V CROWBAR

PI-11,33(OUT) −10V REG SEE NOTE 1

TP3

Ⓘ −40V REGULATO

PI-43(IN) −40V UNREG RET

F6 2A

Q8

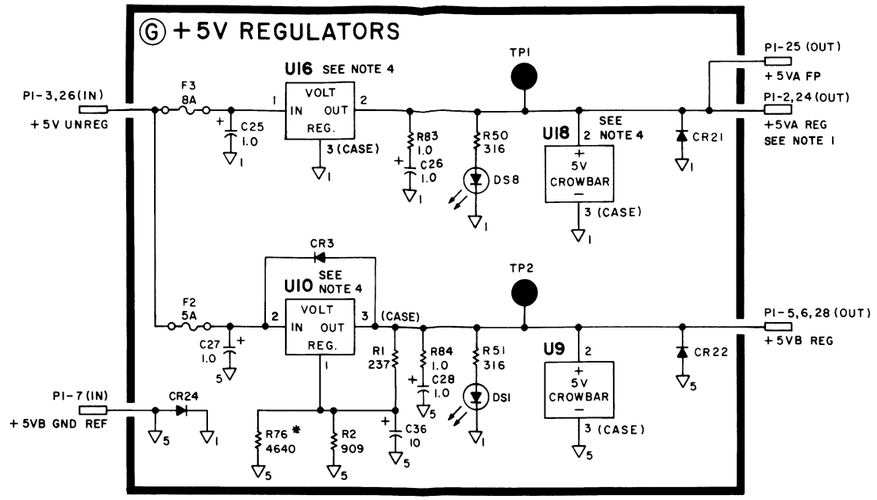
Q6

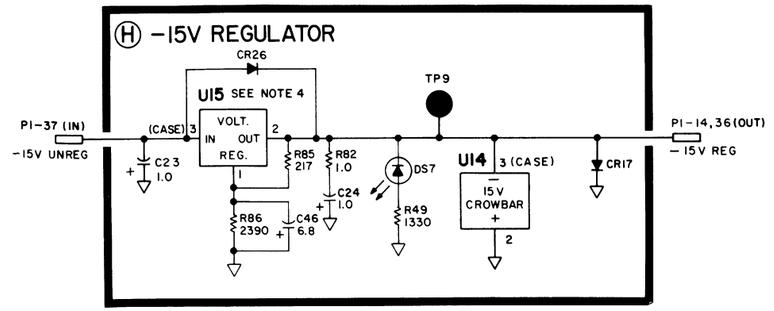
(CASE)

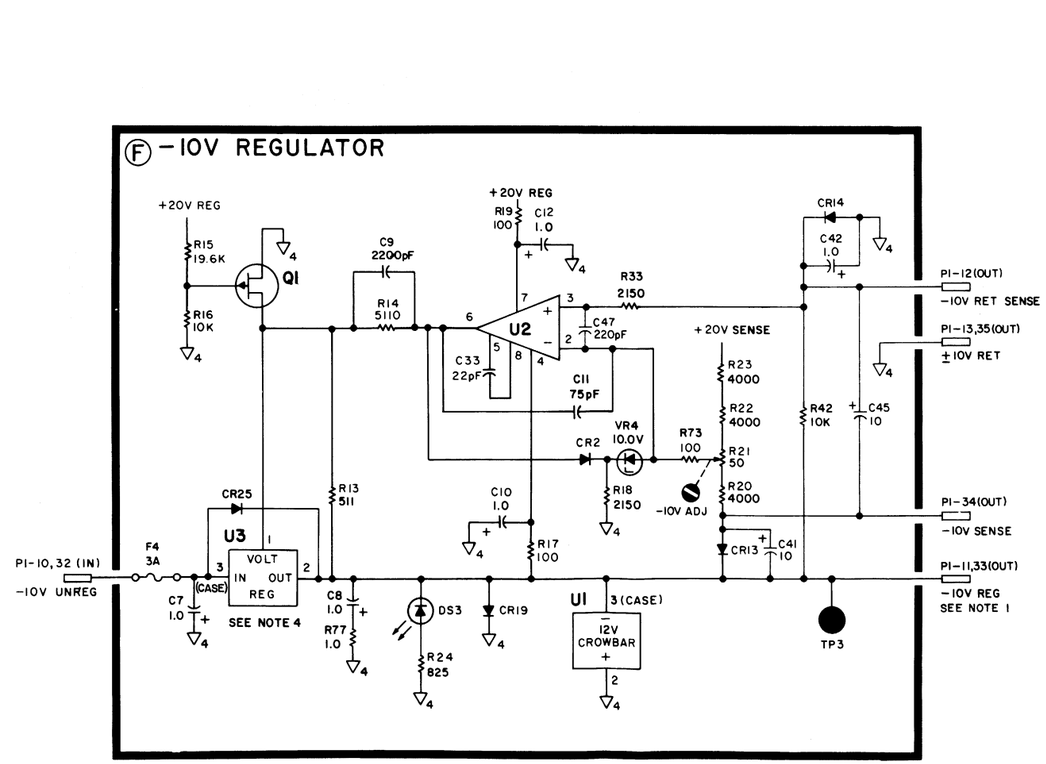
SEE NOTE 4

R30 1000

R29 0.68







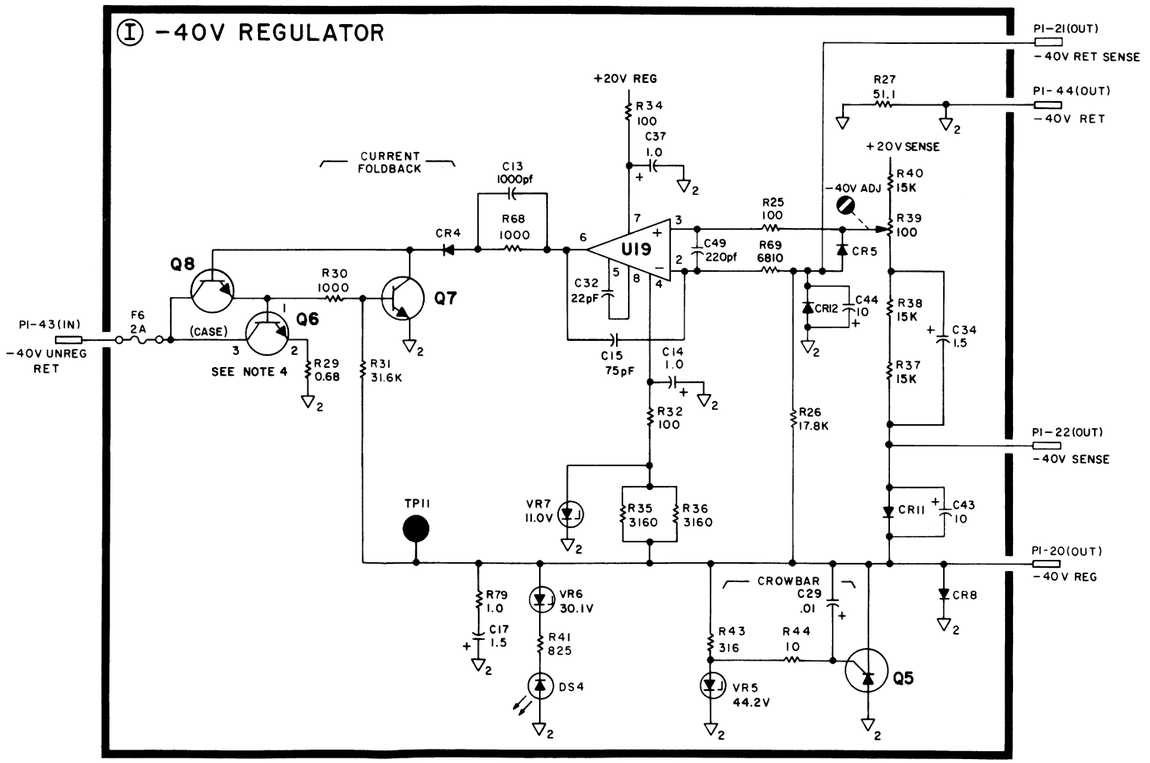


Figure 8-54. A7 Regulator, Schematic Diagram

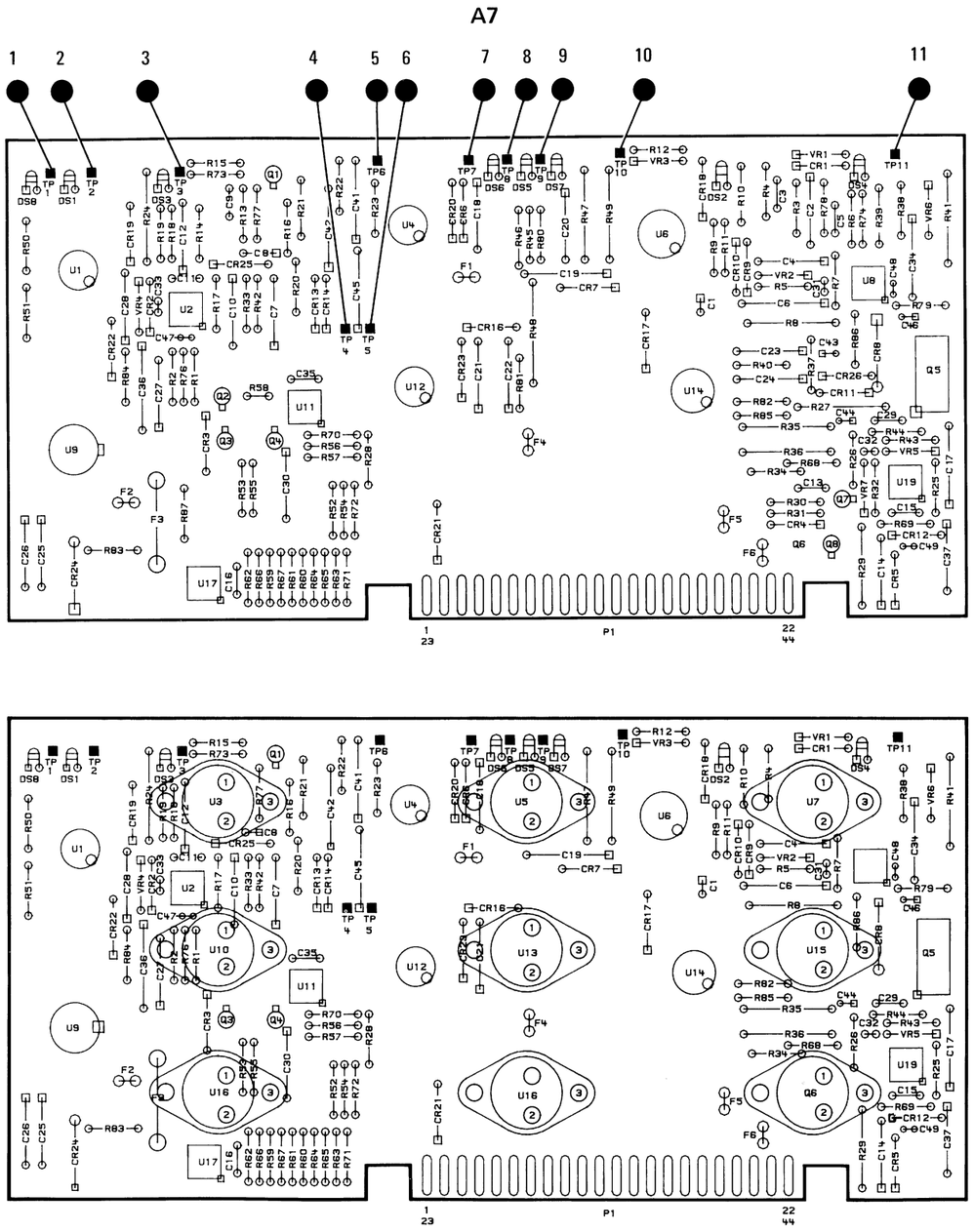


Figure 8-52. A7 Regulator, Component Locations

NOTES

1. SEE BLOCK DIAGRAM FOR FUSES MOUNTED ON MOTHERBOARD.

2. THE STATE OF POWER SUPPLY FAILURE AND AIRFLOW FLAGS LPSF AND LPST ARE READ BY THE A3 MICROPROCESSOR AND STORED WITH THE STATUS BYTE AT HEX ADDRESS 1000. PERFORMING A HEX DATA READ FROM THE FRONT PANEL WILL GIVE 01 IF LPSF IS TRUE (LOW), 02 IF LPST IS TRUE (LOW), AND 03 IF BOTH ARE TRUE.

3. THE RETURN FOR EACH SUPPLY IS SHOWN IN THE FUNCTION BLOCKS.

4. THESE COMPONENTS ARE NOT VISIBLE ON THE COMPONENT SIDE OF THE PC BOARD BUT THE CONNECTIONS TO THESE COMPONENTS ARE SHOWN ON THE LOWER COMPONENT LOCATION FIGURE.

A7P1

PIN	SIGNAL	I/O	TO/FROM	FUNCTION
1 23	GND DIG GND DIG			J J
2 24	+5VA +5VA	OUT OUT	DIST. DIST.	G G
3 25	+5V UNREG +5VAFP	IN OUT	A6P1-13, 14 A9E8	G G
4 26	L PST +5V UNREG	OUT IN	A3P2-9 A6P1-13, 14	B G
5 27	+5VB L PSF	OUT OUT	J2-18, 50 A3P2-11	G A
6 28	+5VB +5VB	OUT OUT	J2-18, 50 J2-18, 50	G G
7 29	+5VB GNDREF +15V UNREG	IN	J2-21 A6P1-22, 44	G D
8 30	+15V +15V	OUT OUT	DIST. DIST.	D D
9 31	GND ANLG GND ANLG			J J
10 32	−10V UNREG −10V UNREG	IN IN	A6P1-16, 38 A6P1-16, 38	F F
11 33	−10V −10V	OUT OUT	J3-13 J3-13	F F
12 34	−10V RET SENSE −10V SENSE		J3-12 J3-4	F F
13 35	±10V RET ±10V RET		A6P1-17, 18 A6P1-17. 18	E, F E, F
14 36	−15V −15V	OUT OUT	DIST. DIST.	H H
15 37	+20V RET −15V UNREG	IN	A6P1-9, 10 A6P1-20, 42	C H
16 38	+20V RET SENSE +20V SENSE		J3-6 J3-15	C C
17 39	+20V +20V	OUT OUT	J3-7 J3-7	C C
18 40	+20V UNREG +20V UNREG	IN IN	A6P1-7, 8 A6P1-7, 8	C C
19 41	+10V +10V	OUT OUT	J3-8 J3-8	E E
20 42	−40V +10V UNREG	OUT IN	J3-11 A6P1-19, 41	I E
21 43	−40V RET SENSE −40V UNREG RET		J3-10 A6P1-5, 6	I I
22 44	−40V SENSE −40V RET		J3-2 J3-1	I I

Supply	With DVM Pro
+20V	A9J2-pin
−10V	A9J2-pin
−40V	A9J2-pin
+5VA	A7TP1
+5VB	A7TP2
+10V	A7TP8
+15V	A7TP7
−15V	A7TP9

*Voltage limits give

**The −40 volts su
power is remove
unplugged 8350A**

Table 8-31. Regulated Supply Limits

With 83500-Series		With 11869A Adapter		Limits
VM Probe	Ground	DVM Probe	Ground	
A9J2-pin 7	A9J2-pin 6	A7TP10*	A7P1-38	19.990V to 20.010V
9J2-pin 16	A9J2-pin 15	A7TP3*	A7P-1-22*	−10.005V to −9.995V
9J2-pin 16	A9J2-pin 4	A7TP11*	A7P1-34*	−40.02V to−39.980V
A7TP1	A7TP6	A7TP1	A7TP6	4.750V to 5.250V
A7TP2	A7TP6	A7TP2	A7TP6	5.000V to 5.450V
A7TP8	A7TP6	A7TP8	A7TP6	9.50V to 10.50V
A7TP7	A7TP6	A7TP7	A7TP6	15.00V to 16.40V
A7TP9	A7TP6	A7TP9	A7TP6	−15.50V to−14.10V

nits given are for 11869A Adapter without the 86200-series RF Plug-in connected.

WARNING

olts supply has no bleeder resistor thus the voltage remains long after removed. To reduce the risk of electrical shock when working with an l 8350A, discharge the −40 volts.

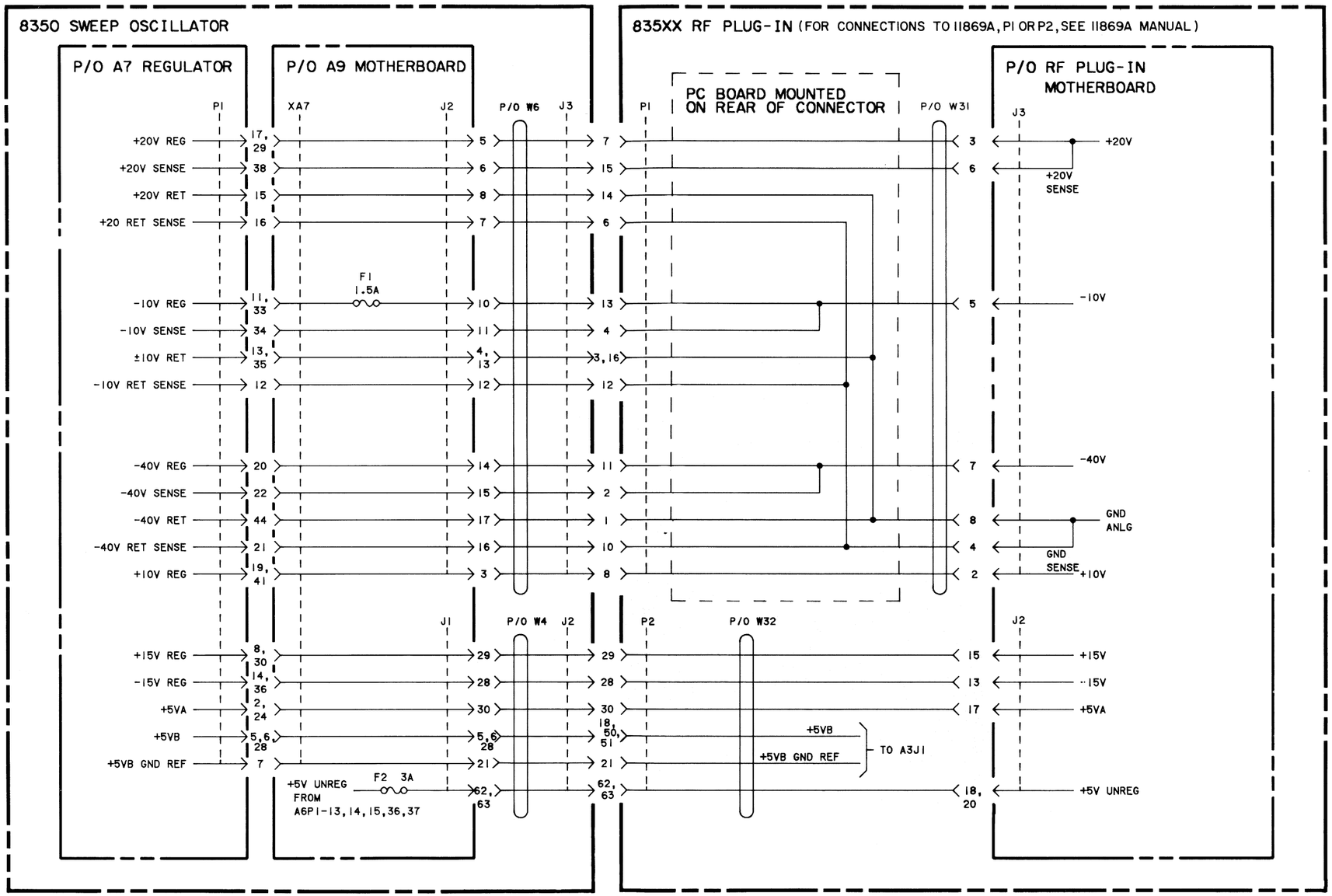


Figure 8-53. 8350A/RF Plug-in Power Supply Interface, Schematic Diagram

A8 HP-IB INTERFACE, CIRCUIT DESCRIPTION

The A8 HP-IB Interface functions as a Talker/Listener for interfacing the 8350A to the Hewlett Packard Interface Bus (HP-IB). For an explanation of bus operation, refer to "Condensed Description of the Hewlett Packard Interface Bus" (HP Part No. 59401-90030). The A8 HP-IB Interface assembly interfaces with the external HP-IB through rear panel connector J4. The sixteen bus lines are buffered by the HP-IB Bus Driver, and connect to the HP-IB Interface circuit. Communication with the A3 Microprocessor is through the Instrument Bus (Data, Address, and Control).

The Address Decoder decodes the instrument address bus lines L IA0 through L IA4 and I/OE1 to generate chip select signals for specific components on the A8 HP-IB assembly.

Upon power-on, the A3 Microprocessor reads the setting of the HP-IB Address Switch. The HP-IB address is stored in RAM on the A3 Microprocessor and in an internal register of the HP-IB Interface circuit. (For Option 001, the A3 Microprocessor does not read the Address Switch, and a new address must be entered from the front panel.)

The HP-IB Interface circuit handles the data transfer, handshake timing, device clearing and triggering, service requests, and serial and parallel polling. When a remote command is received, the HP-IB Interface circuit transmits a L IBIRQ (Low=HP-IB Interrupt Request) to the A3 Microprocessor. The microprocessor responds by polling the HP-IB Interface circuit to determine the status of the interrupt. When addressed to listen, the HP-IB Interface circuit outputs the received instruction onto the Instrument Bus data lines. The data is buffered through the Bi-directional Data Buffer U19 and sent to the A3 Microprocessor. The microprocessor decodes the HP-IB information and implements the remote instruction.

Since the 8350A is both a talker and a listener, data transfer is bi-directional between the 8350A and the HP-IB bus. Instrument Bus control line L IRD (Low=Instrument Bus Read) controls the direction of data flow through the Bi-directional Data Buffer. L IRD is inverted to L WRITE and controls the data flow direction into and out of the HP-IB Interface circuit. The direction of data flow through HP-IB Bus Driver is determined by T/LR (Talk/Low Receive) and L ATN (Low=Attention) signals.

The A3 Microprocessor communicates with the Self Test circuit to verify operation of the Instrument Bus. This Instrument Bus self test is part of the series of self tests performed at initial "power on" or when front panel INSTR PRESET key is pressed. The Instrument Bus self test is also initiated by pressing front panel keys SHIFT 0 9 . This self test checks only operation of the Instrument Bus, and does not check the HP-IB Interface circuit. To check the Instrument Data Bus, the A3 Microprocessor writes a specific bit pattern to the HP-IB Status Indicator where the data is latched. This data is then read by the Microprocessor and compared to the original bit pattern. If the data received does not equal the data sent, error code E005 is displayed on the Front Panel.

If data bus operation is verified, the Microprocessor then places a specific bit pattern on the Instrument Address Bus. This bit pattern is repeated fifteen times. The address lines are decoded and used to increment a counter. The counter output is applied to the data bus and this information is then read by the Microprocessor. The Microprocessor reads the counter output when the counter is cleared and when it has counted to its maximum state. If the data received is not correct, error code E005 is displayed on the front panel.

NOTE

All address locations are given in hexadecimal.

Address Decoder Ⓐ

The HP-IB Interface assembly uses address locations 2000 to 200F. When the Instrument Address Bus contains an address within this range, the Address Decoder decodes the address to determine which device on the A8 HP-IB Interface assembly is addressed by the A3 Microprocessor. The address decoding for the HP-IB Interface circuitry is provided by NAND gate U11B and its associated circuitry. Three-to-Eight decoder U15 provides the decoding for the remaining circuits. Table 8-32 shows the address decoding for each device.

Address lines L IA0−L IA2 are inverted and buffered through U24A, U24F and U24B. These three lines are multiplexed into eight lines by U15. Address lines L IA3, L IA4, control signals I/OE1 (Input/Output Enable 1) and L I/OSTB (Low Input/Output Strobe) are used to enable U15. The outputs of U15 are active low and are used as enable signals for U5, U9, U10 and U14.

The address lines L IA0−L IA4 are inverted and buffered by U24A−F and are sent to the Self Test and HP-IB Interface circuits. The output from U11B, LCS (Low=Chip Select), is the enable signal for the HP-IB Interface circuit U6.

Bi-directional Data Buffer Ⓑ

Transceiver U19 buffers the data on the Instrument Data Bus and the data on the HP-IB Interface. U19 is enabled for address locations 2000 to 200F. Control line L IRD determines the direction of flow of the data through U19. When L IRD is low, the data transfers from the A8 HP-IB Interface Assembly to the Instrument Data Bus. When L IRD is high, the data transfers from the Instrument Data Bus to the A8 HP-IB Interface Assembly. Resistor array U23 provides series resistors for each data line to reduce ringing and crosstalk.

HP-IB Address Ⓒ

Switch S1 is used to set the HP-IB address for the 8350A. When buffer U14 is enabled (LEN7 is low), the S1 switch settings are read by A3 Microprocessor where they are compared to the address being sent on the HP-IB bus. U18 provides pull up resistors for the S1 switch lines. The HP-IB address is read at power on, and stored in RAM. If Option 001 (nonvolatile memory) is installed the HP-IB address is not read at power on, and any changes must be entered from the front panel (SHIFT LCL nn GHz, where nn is between 0 and 30).

HP-IB Interface Ⓔ

Integrated circuit U6 is an HP-IB Talker/Listener device that provides the communications between the 8350A and the HP-IB bus. U6 handles the data transfer, handshake timing, device clearing and triggering, service requests, and serial and parallel polling. Figure 8-55 is a flow diagram showing the logic involved upon receipt of a command from the HP-IB bus.

Table 8-32. HP-IB Interface Add

Address	Address Decoder Components	Components Addressed	Re
2000	U11A, U15, U24, U25	U5	
2001		U10	
2002		U9	
2003		Not used	
2004		Not Used	
2005		Not Used	
2006		U14	
2007		Not Used	
2008	U11B, U24, U25A, F	U6	
2009			
200A			
200B			
200C			
200D			
200E			
200F			

When the 8350A is addressed by the HP-IB bus to
U6 interrupts the A3 Microprocessor by sending
The Microprocessor responds to the interrupt re
the status of the interrupt. Communication then c
Data Bus between U6 and the Microprocessor.
what remote command to implement and perfo

on is then read by the Microprocessor.
t when the counter is cleared and when
data received is not correct, error code

E

given in hexadecimal.

ss locations 2000 to 200F. When the
dress within this range, the Address
hich device on the A8 HP-IB Interface
ssor. The address decoding for the HP-
gate U11B and its associated circuitry.
decoding for the remaining circuits.
each device.

d buffered through U24A, U24F and
to eight lines by U15. Address lines L
utput Enable 1) and L I/OSTB (Low
. The outputs of U15 are active low and
and U14.

and buffered by U24A–F and are sent
rcuits. The output from U11B, LCS
the HP-IB Interface circuit U6.

trument Data Bus and the data on the
locations 2000 to 200F. Control line L
data through U19. When L IRD is low,
face Assembly to the Instrument Data
rom the Instrument Data Bus to the A8
U23 provides series resistors for each

s for the 8350A. When buffer U14 is
are read by A3 Microprocessor where
n the HP-IB bus. U18 provides pull up
ddress is read at power on, and stored
) is installed the HP-IB address is not
entered from the front panel (SHIFT
30).

r/Listener device that provides the
he HP-IB bus. U6 handles the data
and triggering, service requests, and
w diagram showing the logic involved
B bus.

Table 8-32. HP-IB Interface Address Decoding

Address	Address Decoder Components	Components Addressed	Read or Write	Description
2000	U11A, U15, U24, U25	U5	Write	Write HP-IB Status
2001		U10	Read	Read Self Test
2002		U9	Read	Read HP-IB Status
2003		Not used		
2004		Not Used		
2005		Not Used		
2006		U14	Read	Read HP-IB Address switch
2007		Not Used		
2008	U11B, U24, U25A, F	U6	Read Write	Read Data in Write Data out
2009			Read Write	Interrupt Status 1 Interrupt Mask 1
200A			Read	Interrupt Status 2 Interrupt Mask 2
200B			Read Write	Serial Poll Status Serial Poll Mode
200C			Read Write	Address Status Address Mode
200D			Read Write	Command Pass Through Aux Mode
200E			Read Write	Address 0 Address 0/1
200F			Read Write	Address 1 EOS

When the 8350A is addressed by the HP-IB bus to implement a remote command, U6 interrupts the A3 Microprocessor by sending an interrupt request (L IBIRQ). The Microprocessor responds to the interrupt request and polls U6 to determine the status of the interrupt. Communication then continues through the Instrument Data Bus between U6 and the Microprocessor. The Microprocessor determines what remote command to implement and performs the instruction.

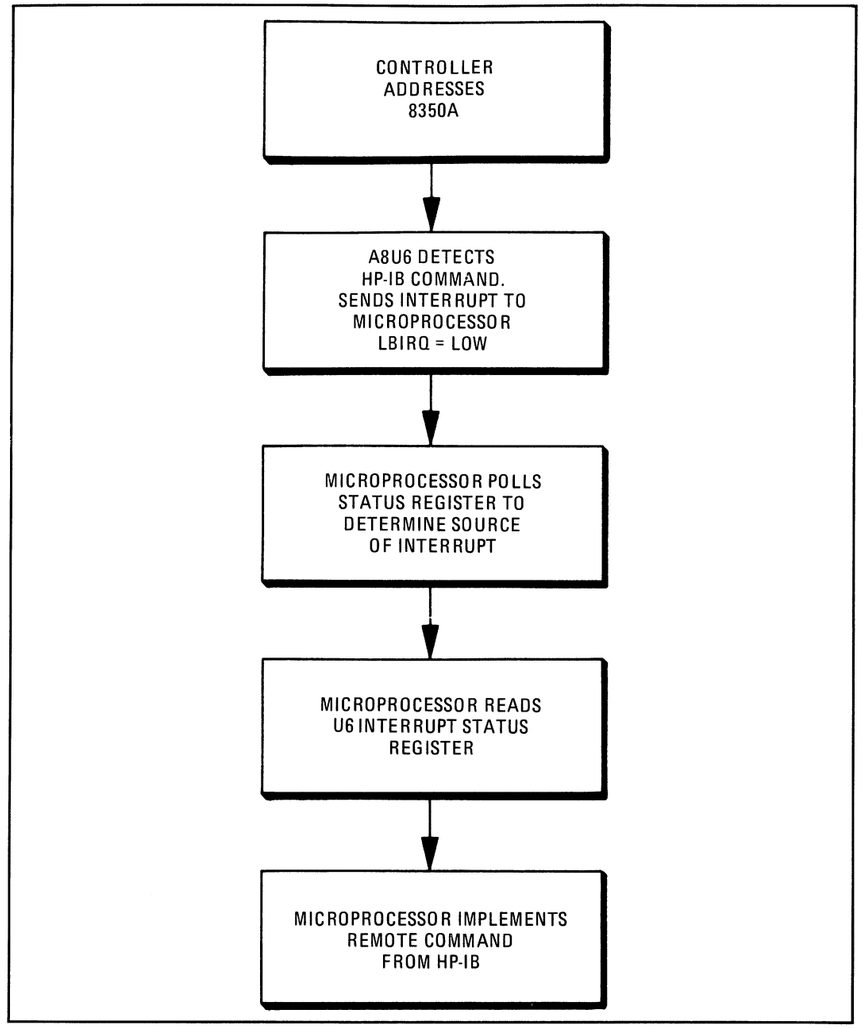


Figure 8-55. HP-IB Interrupt Flow Diagram

NOTE

HP-IB signals L REN, and L IFC are always inputs to the 8350A. Signal L SRQ is always an output to HP-IB.

Table 8-33. A8U8 Directional Control

Controls		Direction of Data			
T/LR	L ATN	L EOI	L NRFD	L NDAC	L DAV
H	H	OUT	IN	IN	OUT
H	L	IN	IN	IN	IN
L	X	IN	OUT	OUT	IN

HP-IB Bus Driver Ⓕ

The HP-IB Bus Driver provides a link between the HP-IB Interface and the HP-IB bus. The sixteen HP-IB signal lines are interfaced through transceivers U8 and U16. U8 handles the data transfer and bus management signals and U13 handles the eight line data bus. For U8, the direction of signal flow is determined by T/LR (Talk/Low Receive), and L ATN (Low=Attention) inputs. Directional control for U8 is shown in Table 8-33.

The direction of signal flow for transceiver U13 is also determined by T/LR. When T/LR is high, data is transferred from U6 to the HP-IB bus. When T/LR is low, data transfers from the HP-IB bus to U6. The sixteen signal lines travel from U8 and U13 through J1 and ribbon cable W5 to the rear panel HP INTERFACE BUS connector J4.

HP-IB Status Indicator Ⓖ

Latch U5 has two functions. It is utilized for the self-test routines as well as for HP-IB status indication. Refer to the Self Test circuit description for operation in the self-test routine.

U5 latches in the data from the Instrument Data Bus which turns on LEDs DS1−DS3 to indicate the HP-IB status of the 8350A. U5 is clocked by LEN1 from the Address Decoder. L SRQ (Low Service Request) is taken directly from the output of U6 and inverted twice through U2B and U2F. The HP-IB state for this signal is indicated by LED DS4. LEDs DS1−DS4 indicate an active state when illuminated (i.e. when the 8350A is in the talk mode DS3 and DS2 are on).

Self Test Ⓓ

The A3 Microprocessor writes a data pattern into latch U5, then reads U9 and compares this data with the original data written into U5. Since U9 is the three-state buffer used to read the latched U5 output, the two data patterns should be identical. The data pattern written is a single high data bit (all other bits are low). This data bit is rotated from the least significant to the most significant bit over a sequence of eight write/read/compare cycles.

The Instrument Bus address lines are then checked. The A3 Microprocessor outputs a series of addresses that are decoded by the Self test circuit, and used to control counter U7. The counter is reset at the beginning of the test by an address bit pattern that results in all highs at the input of 13-input NAND gate U17. This results in a counter reset pulse that is gated with L I/O STB in NOR gate U3D. The A3 Microprocessor then complements the address bit pattern, which results in all highs on the input to 13-input NAND gate U16. The U16 output is gated with I/O STB by U11C, and is used to increment counter U7. This address bit pattern is repeated 15 times to increment the counter so all its outputs are high (a count of 15). The A3 Microprocessor then reads 3-state buffer U10 to determine the counter output. If the counter outputs are all high, the Instrument Bus address lines are operational.

Troubleshooting

Component failures on the A8 HP-IB Interface may be classified as either an Instrument Bus self test failure or HP-IB Interface failure. Instrument Bus operation should be verified before troubleshooting a HP-IB Interface failure.

Instrument Bus Failure Correct Instrument Bus operation is checked during the power on or Instrument Preset self tests. If the front panel INSTR PRESET key is pressed and error code E004 or lower occurs, Instrument Bus operation is verified. If E005 occurs, perform an Instrument Preset self test with A4 Marker and Scaling, A5 Sweep Generator and the RF Plug-in removed. (This removes the possibility of these board assemblies causing an Instrument Bus error code.) If E005 still occurs, set the 8350A into the repetitive Instrument Bus Self Test by pressing SHIFT 0 9 , and checking waveforms shown in Figure 8-59.

HP-IB Interface Failure Provided the Instrument Bus is operational, a HP-IB failure is limited to one of the following circuits:

- Address Decoder (U11B and U15 pin 6)
- HP-IB Address
- HP-IB Interface
- HP-IB Bus Driver
- HP-IB Status Indicator

Basic remote programming operation is verified by performing the Remote Operator's Check in Section III. Depending on the outcome of the Remote Operator's Check, troubleshoot the HP-IB interface as follows:

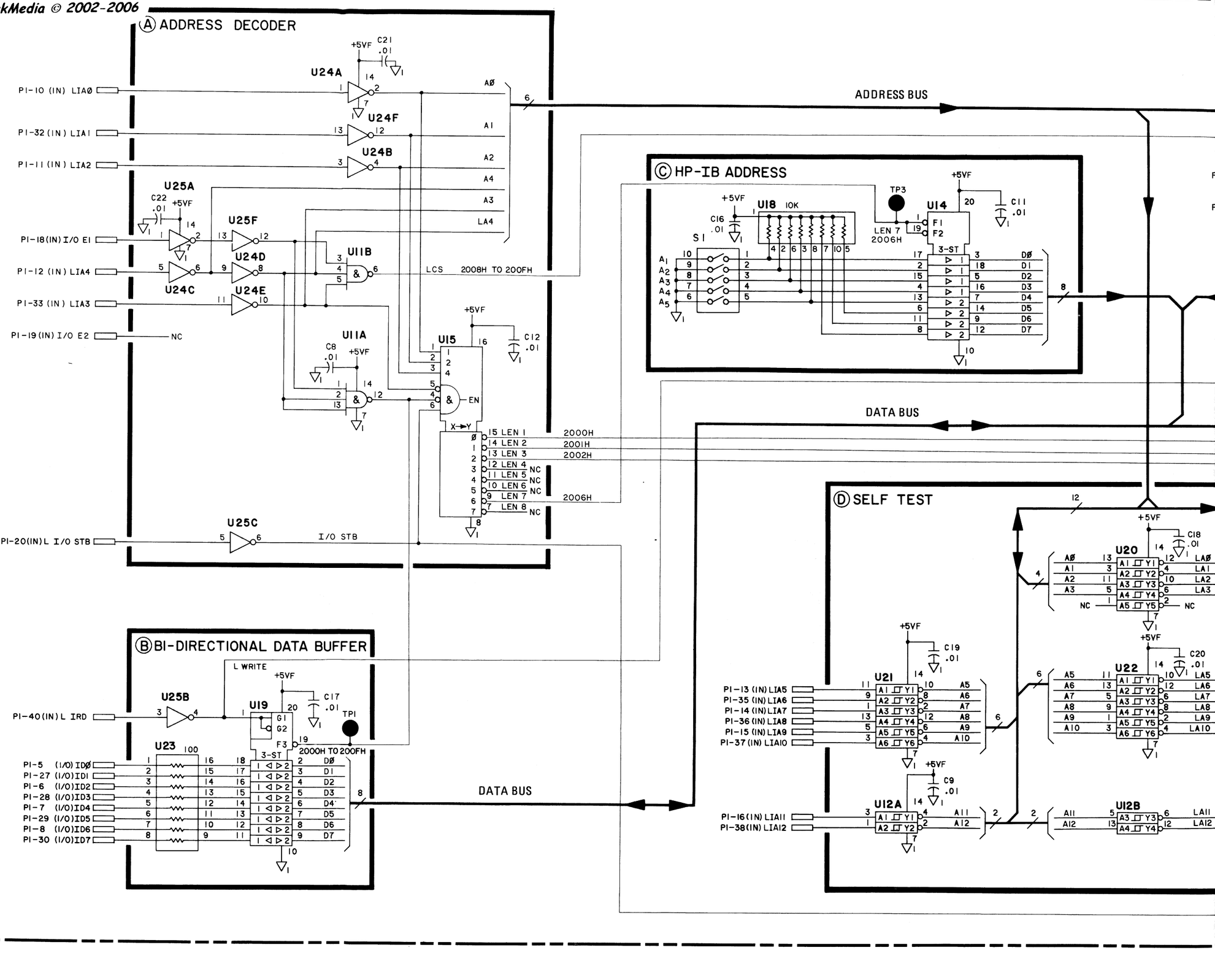
Not able to complete Remote Operator's Check

1. Check Address Switch for correct HP-IB Address. Press Shift LCL (Local) keys to read the HP-IB address and compare it with the actual switch setting.
2. Check interrupt operation. Run Remote Check program in Table 8-34 (See A8 schematic). Check that U6 generates an active low L IBIRQ signal and that U6 receives an active low L CS input. Generation of the interrupt request indicates that U6 has received an HP-IB command. An active L CS pulse indicates that the A3 Microprocessor responds to the interrupt request.
3. Run Remote Check program in Table 8-34. Check for activity on handshake lines (L ATN, L NDAC, L NRFD, and L DAV) and the L REN bus management line.
4. Run Talk/Listen program in Table 8-34. Check HP-IB status indicators switch between TALK and LISTEN indications.

Remote Operator's Check is Verified

1. Check operation of Bus management lines (L SRQ, L IFC, and L EOI). Run programs listed in Table 8-34 to exercise each bus management line and check for activity on that line.
2. Run L REMTRG Check program in Table 8-34, and check L REMTRG line for activity.
3. Problem may be software related. Check that software conforms to guidelines in Section III.

A8 HP-IB INTERFACE
08350-60029



SERIAL PREFIX: 2024A

ADDRESS BUS

DATA BUS

DATA BUS

Ⓒ HP-IB ADDRESS

+5VF
C16 .01
S1
U18 10K
TP3
LEN 7
2006H
U14
C11 .01
3-ST
A1 A2 A3 A4 A5
DØ D1 D2 D3 D4 D5 D6 D7

Ⓔ HP-IB INTERFACE

+5VF C23 .01
U6
AØ A1 A2
RSØ RS1 RS2
2008H TO 200FH
LCS
NC
LEØI LSRQ LREN LIFC LATN LNDAC LNRFD LDAV
LBØ LB1 LB2 LB3 LB4 LB5 LB2 LB7
T/LR
L IBIRQ
REMTRG
NC
PI-2(OUT) L IBIRQ
PI-3(OUT) L REMTRG
PI-24 (IN) L I/O CLK
PI-22 (IN) PWON
U25E
U25D
I/O CLK
RESET
DØ D1 D2 D3 D4 D5 D6 D7
RD
WR
C2 .01
L WRITE
U4C
U4D
U2D
U2C

Ⓕ HP-IB

Ⓓ SELF TEST

U20
U21
U22
U12A
U12B
C18 .01
C19 .01
C20 .01
C9 .01
PI-13 (IN) LIA5
PI-35 (IN) LIA6
PI-14 (IN) LIA7
PI-36 (IN) LIA8
PI-15 (IN) LIA9
PI-37 (IN) LIA10
PI-16 (IN) LIA11
PI-38 (IN) LIA12
U16
U17
U12D
U11C
U12C
C13 .01
C14 .01
C1 .01
TP4
U3D
I/O STB

LEN 3
2002H
U9
C6 .01
LEN 2
2001H
U10
C4 .01
C7 .01
U7
CNTR
(1) (2) (4) (8)

Ⓖ HP-IB STATUS IN

TP2
LEN 1
2000H
U5
FF
LSRQ

Figure 8-60. A8 HP-IB Interface, Schematic Diagram

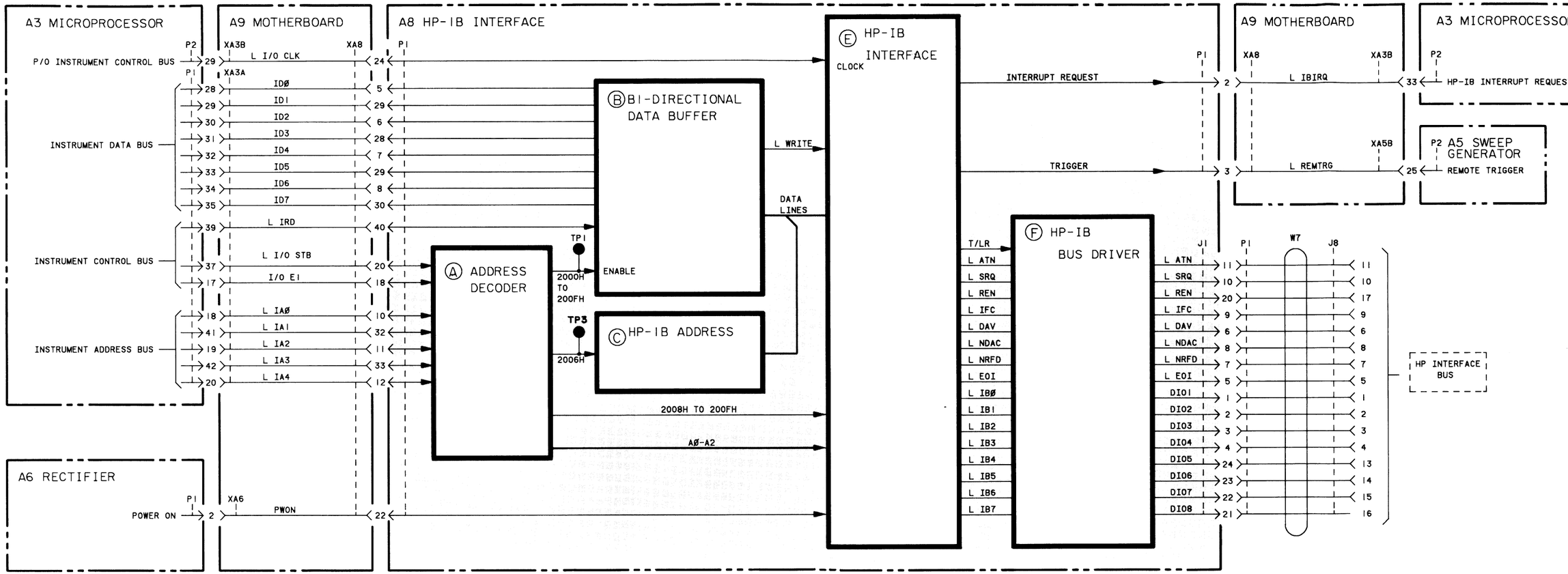
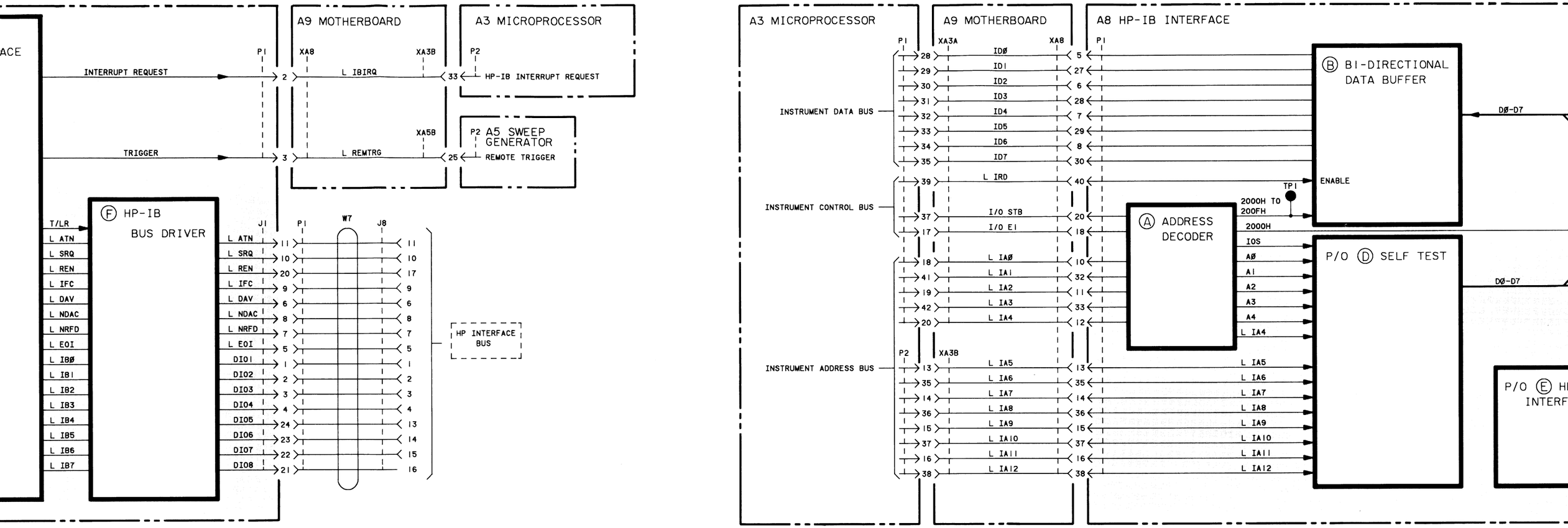
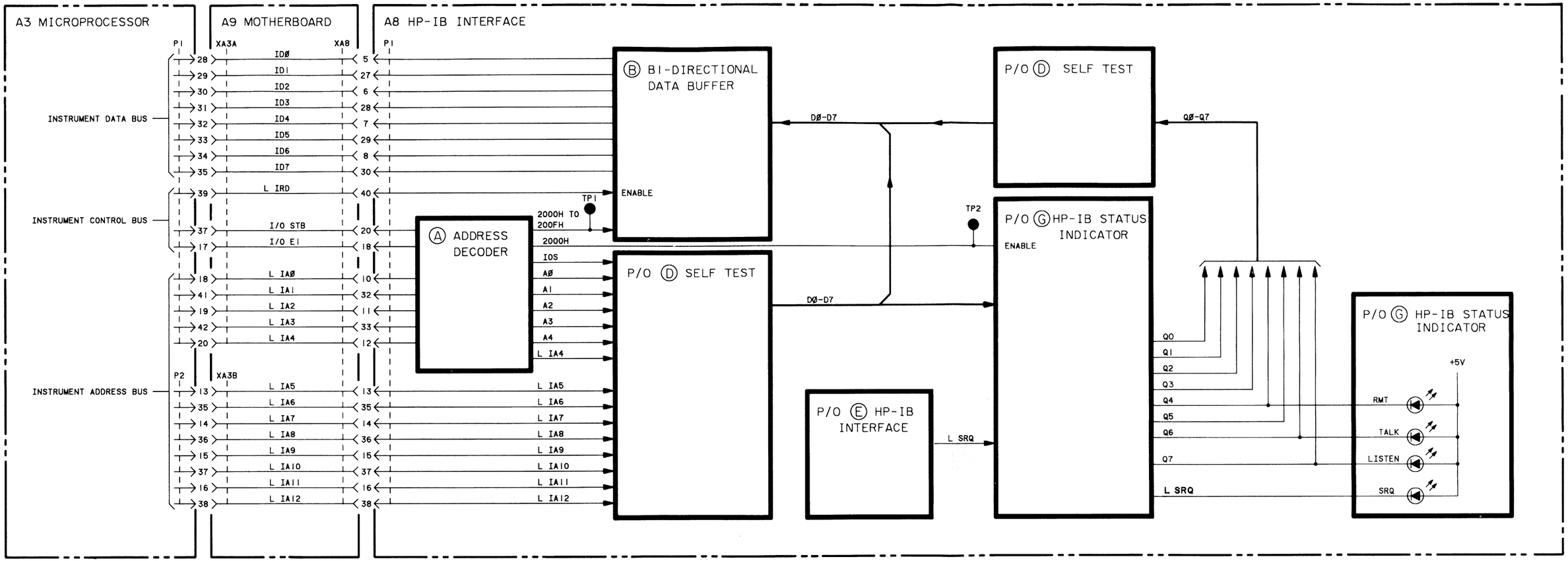


Figure 8-56. A8 HP-IB Interface, Block Diagram



gure 8-56. A8 HP-IB Interface, Block Diagram



A8

Figure 8-57. A8 HP-IB Interface Self Test, Block Diagram

Figure 8-60. A8 HP-IB Interface, Schematic Diagram

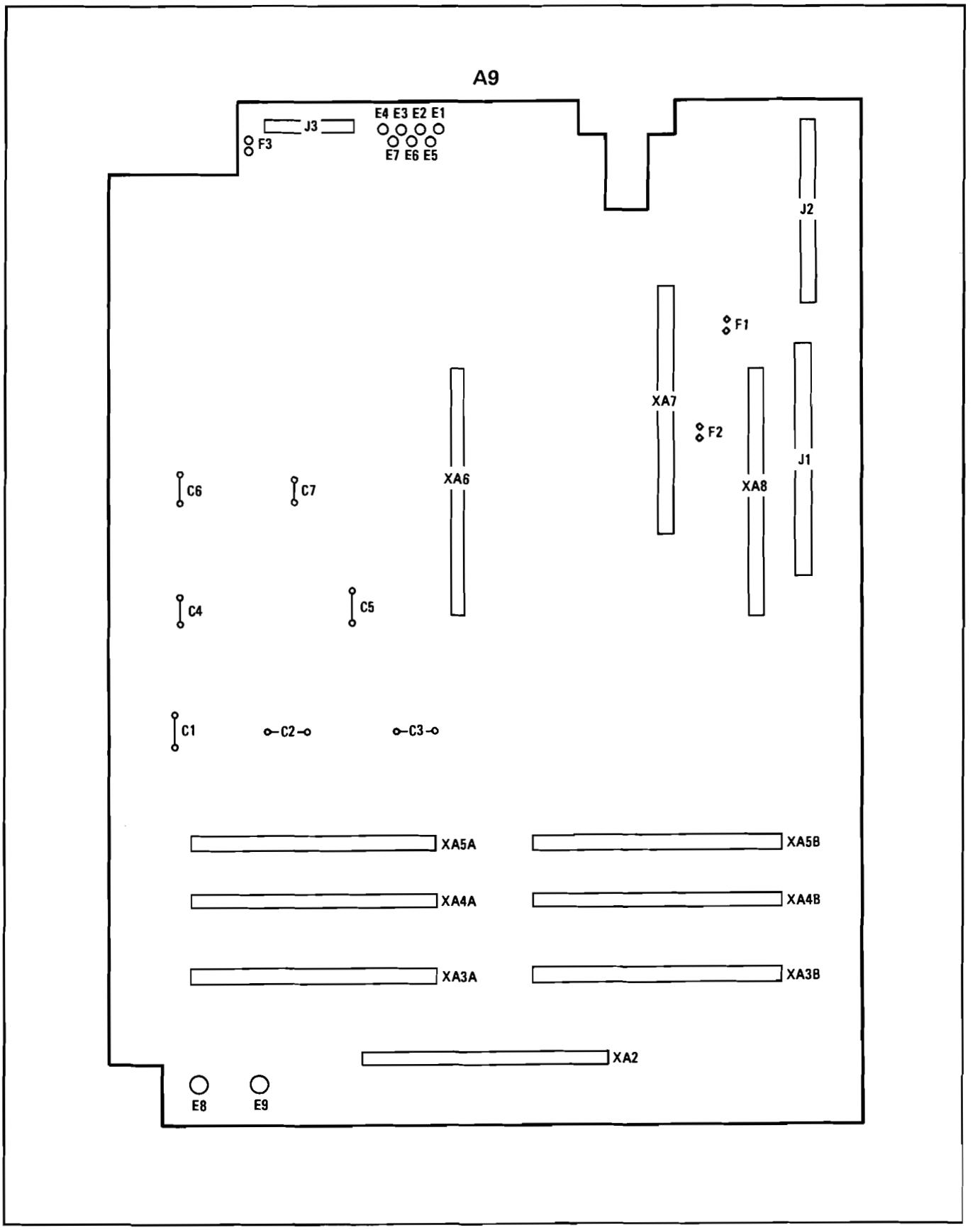


Figure 8-61. A9 Motherboard, Component Locations

MNEMONIC	SOURCE	DESCRIPTION	A1J1 (W1)	A1J2 (W2)	A2J3 (W1)	A2J4 (W2)	A2P1	A3P1	A3P2	A4P1	A4P2	A5P1	A5P2	A6P1	A7P1	A8J1 (W5)	A8P1	A9J1 (W4)	A9J2 (W6)	A9J3 (W7)	MISC.	CHASSIS
ALT1	A5P1-34	Alternate Sweep 1									–	34	–			–				4,13	–	J13-4, J14-1
L ALTE	A5P1-33	Low = Alternate Sweep Enable									–	33	–			–				17,25	–	J13-17, J14-2
AM	J12	Amplitude Modulation Input									–	–	–			–				–	W9	J3-A4, J12
L AMK	A4P2-27	Low = Active Marker									27	–	27			–				–	–	–
L ATN	J4-11	Low = Attention (HP-IB)									–	–	–			11				–	–	J4-11
L BP1	A5P2-36	Low = Blanking Pulse 1		–		–					–		36					–		14		J13-14
L BP2	A5P2-11	Low = Blanking Pulse 2		–		–					33		11					53		–		J2-53
L BPRQ	J2-55,J13-20	Low = Blanking Pulse Request		–		–					–		40					55		20		J2-55, J13-20
CO	A2J4-16	Keyboard Column 0		16		16					–		–					–		–		–
C1	A2J4-11	Keyboard Column 1		11		11					–		–					–		–		–
C2	A2J4-5	Keyboard Column 2		5		5																
C3	A2J4-30	Keyboard Column 3		30		30																
C4	A2J4-15	Keyboard Column 4		15		15																
C5	A2J4-13	Keyboard Column 5		13		13																
C6	A2J4-9	Keyboard Column 6		9		9																
C7	A2J4-12	Keyboard Column 7	–	12	–	12																
Ca	A2J3-5	Digital Display Segment a	5	–	5	–																
Cb	A2J3-32	Digital Display Segment b	32	–	32	–																
Cc	A2J3-10	Digital Display Segment c	10	–	10	–																
Cd	A2J3-7	Digital Display Segment d	7	–	7	–																
Cdp	A2J3-28	Digital Display Decimal Point	28		28							–						–		–	–	–
Ce	A2J3-30	Digital Display Segment e	30		30							–						–		–	–	–
Cf	A2J3-8	Digital Display Segment f	8		8							–						–		–	–	–
Cg	A2J3-34	Digital Display Segment g	34		34							–						–		–	–	–
L CNTR	A5P1-42	Low = Counter Trigger	–		–							42						22		21	W10,A9E7	J2-22,J9,J13-21
L DAV	J4-6	Low = Data Valid (HP-IB)	–		–											6						J4-6
DCA0	A2J3-9	Digit Counter Address 0 (LSB)	9		9											–						–
DCA1	A2J3-12	Digit Counter Address 1	12		12											–						–
DCA2	A2J3-16	Digit Counter Address 2	16		16											–						–
DCA3	A2J3-26	Digit Counter Address 3 (MSB)	26		26											–						–
L DCA3	A2J3-13	Low = Digit Counter Address 3 (MSB)	13		13											–						–
L DE	A2J3-14	Low = Display Enable, Front Panel	14		14											–						–
DIO1	J4-1	HP-IB Data Input/Output (LSB)	–		–											1						J4-1
DIO2	J4-2	HP-IB Data Input/Output	–		–											2						J4-2
DIO3	J4-3	HP-IB Data Input/Output	–		–											3						J4-3
DIO4	J4-4	HP-IB Data Input/Output														4						J4-4
DIO5	J4-13	HP-IB Data Input/Output														24						J4-13
DIO6	J4-14	HP-IB Data Input/Output														23						J4-14
DIO7	J4-15	HP-IB Data Input/Output														22						J4-15
DIO8	J4-16	HP-IB Data Input/Output														21						J4-16
L DS1	A2J4-48	Low = Left Frequency GHz Annunciator On		48		48																
L DS2	A2J4-50	Low = Left Frequency MHz Annunciator On		50		50																
L DS3	A2J4-46	Low = Right Frequency GHz Annunciator On		46		46																
L DS4	A2J4-43	Low = Right Frequency MHz Annunciator On		43		43																
L DS5	A2J4-45	Low = Frequency/Time GHz Annunciator On		45		45																
L DS6	A2J4-49	Low = Frequency/Time MHz Annunciator On	–	49	–	49																
L DS7	A2J4-47	Low = Frequency/Time Sec Annunciator On	–	47	–	47																
L DS8	A2J4-7	Low = ALTn Annunciator On	–	7	–	7																
L DS9	A2J4-41	Low = Vernier Annunciator On	–	41	–	41																
L DS10	A2J3-15	Low = ≠0 Annunciator On	15	–	15	–																

Figure 8-62. Motherboard Wiring List (1 of 5)

MNEMONIC	SOURCE	DESCRIPTION	A1J1 (W1)	A1J2 (W2)	A2J3 (W1)	A2J4 (W2)	A2P1	A3P1	A3P2	A4P1	A4P2	A5P1	A5P2	A6P1	A7P1	A8J1 (W5)	A8P1	A9J1 (W4)	A9J2 (W6)	A9J3 (W7)	MISC.	CHASSIS
L DS11	A2J4-38	Low = MKRΔ Annunciator On		38		38																
L DS12	A2J4-20	Low = Start Annunciator On		20		20																
L DS13	A2J4-22	Low = CW Annunciator On		22		22																
L DS14	A2J4-18	Low = CF Annunciator On		18		18																
L DS15	A2J4-24	Low = ΔF Annunciator On		24		24																
L DS16	A2J4-26	Low = Stop Annunciator On		26		26																
L DS17	A2J4-37	Low = M1 Annunciator On		37		37																
L DS18	A2J4-44	Low = M2 Annunciator On		44		44																
L DS19	A2J4-42	Low = M3 Annunciator On		42		42																
L DS20	A2J4-36	Low = REM Annunciator On		36		36																
L DS21	A2J4-17	Low = ADRS'D Annunciator On	–	17	–	17																
L DS22	A2J3-20	Low = Marker Sweep Annunciator On	20	–	20	–																
L DS23	A2J4-32	Low = M4 Annunciator	–	32	–	32																
L DS24	A2J4-34	Low = M5 Annunciator On	–	34	–	34																
L DS25	A2J4-19	Low = Shift Annunciator On (Blue Key)	–	19	–	19																
L DS26	A2J4-21	Low = Swp Annunciator On		21		21																
L DS27	A2J4-23	Low = Int Annunciator On		23		23																
L DS28	A2J4-25	Low = Line Annunciator On		25		25																
L DS29	A2J4-27	Low = Ext Trig Annunciator On		27		27																
L DS30	A2J4-29	Low = Single Annunciator On		29		29																
L DS31	A2J4-31	Low = Ext Swp Annunciator On		31		31																
L DS32	A2J4-33	Low = Man Annunciator On		33		33																
L DS33	A2J4-35	Low = Time Annunciator On		35		35																
L DS34	A2J4-2	Low = Amptd Mkr Annunciator On		2		2																
L DS35	A2J4-10	Low = Displ Blank Annunciator On		10		10																
L DS36	A2J4-8	Low = RF Blank Annunciator On		8		8						–				–				–	–	–
L DS37	A2J4-6	Low = ⎍MOD Annunciator On		6		6						–				–				–	–	–
L EO1	J4-5	Low = End or Identify (HP-IB)		–		–						–				5				–	–	J4-5
EXT TRG	J13-9	High = External Trigger Sweep		–		–						19				–				9	–	J13-9
FM INPUT	J11	Frequency Modulation Input		–		–						–				–				–	W8	J3-A3,J11
L FPA0	A3P2-4	Low = Front Panel Address Line 0 (LSB)					16		4													
L FPA1	A3P2-26	Low = Front Panel Address Line 1					38		26													
L FPA2	A3P2-5	Low = Front Panel Address Line 2					17		5													
L FPA3	A3P2-27	Low = Front Panel Address Line 3 (Not Used)					39*		27*													
L FPA4	A3P2-6	Low = Front Panel Address Line 4 (MSB) (Not Used)					18*		6*													
FPD0	A3P1-6	Front Panel Data Line 0 (LSB)					6	6														
FPD1	A3P1-7	Front Panel Data Line 1					28	7														
FPD2	A3P1-8	Front Panel Data Line 2					7	8														
FPD3	A3P1-9	Front Panel Data Line 3					29	9														
FPD4	A3P1-10	Front Panel Data Line 4					8	10														
FPD5	A3P1-11	Front Panel Data Line 5					30	11	–													
FPD6	A3P1-12	Front Panel Data Line 6					9	12	–													
FPD7	A3P1-13	Front Panel Data Line 7 (MSB)					31	13	–													
FPE	A3P2-3	Front Panel Enable					15	–	3													
L FPIRQ	A2P1-23	Low = Front Panel Interrupt Request					23	1	–													
L FPRD	A3P2-25	Low = Front Panel Read (High = Write)					37	–	25	–		–					–	–				–
L FPSTB	A3P2-1	Low = Front Panel Strobe					13	–	1	–		–					–	–				–
L IA0	A3P1-18	Low = Instrument Address Line 0 (LSB)					–	18	–	16		16					10	38				J2-38
L IA1	A3P1-41	Low = Instrument Address Line 1					–	41	–	39		39					32	7				J2-7
L IA2	A3P1-19	Low = Instrument Address Line 2					–	19	–	17		17					11	39				J2-39

*Not used on this assembly.

Figure 8-62. Motherboard Wiring List (2 of 5)

MNEMONIC	SOURCE	DESCRIPTION	A1J1 (W1)	A1J2 (W2)	A2J3 (W1)	A2J4 (W2)	A2P1	A3P1	A3P2	A4P1	A4P2	A5P1	A5P2	A6P1	A7P1	A8J1 (W5)	A8P1	A9J1 (W4)	A9J2 (W6)	A9J3 (W7)	MISC.	CHASSIS
L IA3	A3P1-42	Low = Instrument Address Line 3						42	–	40		40					33	8				J2-8
L IA4	A3P1-20	Low = Instrument Address Line 4						20	–	18		18					12	40				J2-40
L IA5	A3P2-13	Low = Instrument Address Line 5						–	13	–		–					13	41				J2-41
L IA6	A3P2-35	Low = Instrument Address Line 6						–	35	–		–					35	10				J2-10
L IA7	A3P2-14	Low = Instrument Address Line 7						–	14	–		–					14	42				J2-42
L IA8	A3P2-36	Low = Instrument Address Line 8							36								36	11				J2-11
L IA9	A3P2-15	Low = Instrument Address Line 9							15								15	43				J2-43
L IA10	A3P2-37	Low = Instrument Address Line 10							37								37	12				J2-12
L IA11	A3P2-16	Low = Instrument Address Line 11							16								16	44				J2-44
L IA12	A3P2-38	Low = Instrument Address Line 12 (MSB)							38								38	13				J2-13
L IBIRQ	A8P1-2	Low = HP-IB Interrupt Request						–	33	–		–					2	–				–
ID0	A3P1-28	Instrument Data Line 0 (LSB)						28	–	6		6					5	33				J2-33
ID1	A3P1-29	Instrument Data Line 1						29	–	28		28					27	2				J2-2
ID2	A3P1-30	Instrument Data Line 2						30	–	7		7					6	34				J2-34
ID3	A3P1-31	Instrument Data Line 3						31	–	29		29					28	3				J2-3
ID4	A3P1-32	Instrument Data Line 4						32		8		8				–	7	35				J2-35
ID5	A3P1-33	Instrument Data Line 5						33		30		30				–	29	4				J2-4
ID6	A3P1-34	Instrument Data Line 6						34		9		9				–	8	36				J2-36
ID7	A3P1-35	Instrument Data Line 7 (MSB)						35		31		31				–	30	5				J2-5
L IFC	J4-9	Low = Interface Clear (HP-IB)						–		–		–				9	–	–				J4-9
L I/O CLK	A3P2-29	Low = Input/Output Clock						–	29	–	9*	–					24	–				–
I/OE1	A3P1-17	High = I/O Enable for Sweep Gen. and HP-IB Interface						17	–	15*	–	15					18	–				–
I/OE2	A3P1-16	High = I/O Enable for RF Plug-in						16	–	14*	–	14*					19	47				J2-47
I/OE3	A3P2-24	High = I/O Enable for Scaling and Marker						–	24	–	3	–					–	–				–
L I/OSTB	A3P1-37	Low = Input/Output Strobe						37	–	13	–	13					20	17				J2-17
L IRD	A3P1-39	Low = Instrument Bus Read (High = Write)	–		–			39		37		37	–	–			40	15				J2-15
IS1	A2J3-3	Annunciator Current Source (Left Freq Display)	3		3			–		–		–	–	–			–	–				–
IS2	A2J3-1	Annunciator Current Source (Right Freq Display)	1		1			–		–		–	–	–			–	–				–
IS3	A2J3-2	Annunciator Current Source (Freq/Time Display)	2		2			–		–		–	–	–			–	–				–
L LINETRG	A6P1-24	Low = Line Trigger	–		–			–		–		–	15	24			–	–				–
L MFLG	A4P2-11	Low = Marker Flag							31		11		–							–		–
L MK	A4P2-6	Low = Marker							–		6		6							–		–
L MKRQ	J13-15	Low = Marker Request							–		–		38							15		J13-15
L MP	A5P2-14	Low = Marker Pulse							–		–		14							2		J13-2
L MUTE	A5P2-13	Low = Pen Mute for X-Y Recorder							–		–		13							11		J13-11
L NDAC	J4-8	Low = Not Data Accepted (HP-IB)							–				–			8		–			–	J4-8
L NRFD	J4-7	Low = Not Ready for Data (HP-IB)							–				–			7		–			–	J4-7
NZAB	A5P2-12	Negative Z Axis Blanking							–				12			–		–			W10,A9E4	J6
L PIFLG	J2-20	Low = Plug-in Flag							19				–			–		20			–	J2-20
L PIIRQ	J2-52	Low = Plug-in Interrupt Request							20				–			–		52			–	J2-52
L PINMI	J2-19	Low = Plug-in Nonmaskable Interrupt					–		40					–				19		–	–	J2-19
PIROME	A3P2-17	Plug-in ROM Enable					–		17					–				45		–	–	J2-45
PIRPG1A	J2-60	Plug-in RPG Output					41		–					–				60		–	–	J2-60
PIRPG1B	J2-61	Plug-in RPG Output					20		–					–				61		–	–	J2-61
PL	A6P1-3	High = Penlift					–		–					3				–		10	W10,A9E1	J7,J13-10
L PL	A5P2-35	Low = Penlift	–		–				–				35	25	–					23		J13-23
L PLRQ	J13-3	Low = Penlift Request	–		–				–				16	–	–					3		J13-3
L PRESET	A1J1-25	Low = Instrument Preset	25		25				–				–	–	–					–		–
L PRESETE	A2J3-27	Low = Instrument Preset Enable	27		27				–				–	–	–					–		–
L PSF	A7P1-27	Low = Power Supply Failure	–		–				11				–	–	27					–		–

*Not used on this assembly.

Figure 8-62. Motherboard Wiring List (3 of 5)

MNEMONIC	SOURCE	DESCRIPTION	A1J1 (W1)	A1J2 (W2)	A2J3 (W1)	A2J4 (W2)	A2P1	A3P1	A3P2	A4P1	A4P2	A5P1	A5P2	A6P1	A7P1	A8J1 (W5)	A8P1	A9J1 (W4)	A9J2 (W6)	A9J3 (W7)	MISC.	CHASSIS
L PST	A7P1-4	Low = Power Supply Overtemp. (Airflow)		–		–	–		9				–	–	4		–	–			–	–
PWON	A6P1-2	High = Power On		–		–	43		41				–	2	–		22	25			–	J2-55
PZAB	A5P2-34	Positive Z Axis Blanking		–		–	–		–				34	–	–		–	--			W10,A9E6	J5
R0	A1J2-39	Keyboard Row 0 Sense		39		39	–		–				–	–	–		–	–			–	–
R1	A1J2-4	Keyboard Row 1 Sense		4		4	–		–				–	–	–		–	–			–	–
R2	A1J2-40	Keyboard Row 2 Sense		40		40																
R3	A1J2-14	Keyboard Row 3 Sense		14		14																
R4	A1J2-1	Keyboard Row 4 Sense		1		1																
R5	A1J2-3	Keyboard Row 5 Sense		3		3																
R6	A1J2-28	Keyboard Row 6 Sense		28		28																
L REM TRG	A8P1-3	Low = Remote Trigger (Group Execute)											25			–	3	–		–		–
L REN	J4-17	Low = Remote Enable (HP-IB)											–			20	–	–		–		J4-17
L RFB	A5P2-42	Low = RF Blank											42			–	–	56		7		J13-7,J2-56
L RFBRQ	J2-54,J13-8	Low = RF Blank Request											17			–	–	54		8		J13-8,J2-54
L RFM	A5P2-20	Low = RF Marker (Amplitude)											20			–	–	24		–		J2-24
RPG1A	A1J1-31	Left Frequency RPG Output	31		31																	
RPG1B	A1J1-29	Left Frequency RPG Output	29		29																	
RPG2A	A1J1-21	Right Frequency RPG Output	21		21																	
RPG2B	A1J1-19	Right Frequency RPG Output	19		19																	
RPG3A	A1J1-4	Frequency/Time RPG Output	4		4																	
RPG3B	A1J1-6	Frequency/Time RPG Output	6		6		–		–				–					–		–	–	–
L RTCIRQ	A2P1-21	Low = Retrace Interrupt Request	–		–		21		8				–					–		–	–	–
L RTS	A5P2-18,19	Low = Retrace Strobe	–		–		42		–				18,19					57		16,26	–	J2-57, J13-16, J14-3
L SFSRQ	J13-5,J10	Low = Stop Forward Sweep Request	–		–		–		–				41					–		5	W10,A9E3	J13-5, J10
SQ MOD	A5P2-37	Squarewave Modulation (1 kHz or 27.8 kHz)	–		–		–		–				37					26		–	–	J2-26
L SRQ	A8J1-10	Low = Service Request (HP-IB)					–						–			10		–		–		J4-10
L SSRQ	J2-32,J13-18	Low = Stop Sweep Request					–						39			–		32		18		J13-18, J2-32
L STPADV	J13-22	Low = Step Advance					33						–			–		–		22		J13-22
L SW	A5P2-28	Low = Forward Sweep					44						28			–		–		–		–
SYNC TRG	A5P2-5	High = Synchronizing Trigger					–						5			–		–		24		J13-24
VRAMP	A5P1-20	Voltage Ramp								20	–	20	–					–			–	–
VSW	A5P2-24	Sweep Voltage to Plug-in								–	–	–	24					64			–	J2-64
VSW1	A5P1-21	Sweep Voltage to A4 Scaling and Marker								21	–	21	–					–			–	–
VSW2	A5P2-2	Swp Voltage to/from Swp Out/In Connectors								–	–	–	2					–			W10,A9E2	J1, J8
VTUNE	A4J1	Voltage Tuning								–	–	–	–					–			A4J1, W3	J3-A1
L ZMRQ	J2-23	Low = Intensity Marker Request									–		33					23				J2-23
+10V REF	A4P2-7, 29	+10V Reference									7, 29		7, 29					–				–

Figure 8-62. Motherboard Wiring List (4 of 5)

MNEMONIC	SOURCE	DESCRIPTION	A1J1 (W1)	A1J2 (W2)	A2J3 (W1)	A2J4 (W2)	A2P1	A3P1	A3P2	A4P1	A4P2	A5P1	A5P2	A6P1	A7P1	A8J1 (W5)	A8P1	A9J1 (W4)	A9J2 (W6)	A9J3 (W7)	MISC.	CHASSIS
+20V	A7P1-17, 39	+20V Regulated Power Supply												–	17,39				5		–	J3-7
+20V RET	A6P1-9,10 31,32	+20V Return												9,10, 31,32	15				8		A9C6(–)	J3-14
+20V RET SENSE	J3-6	+20V Return Sense												–	16				7		–	J3-6
+20V SENSE	J3-15	+20V Sense												–	38				6		–	J3-15
+20V UNREG	A6P1-7,8, 29,30	+20V Unregulated												7, 8, 29,30	18,40						A9C6(+)	–
+15V	A7P1-8,30	+15V Regulated									8,30		8,30	–	8,30			29			–	J2-29
+15V UNREG	A6P1-22,44	+15V Unregulated									–		–	22,44	29			–			A9C3(+)	–
±15V RET	A6P1-21,43	±15V Return									–		–	21,43	–			–			A9C2(+),A9C3(–)	–
+10V	A7P1-19,41	+10V Regulated												–	19,41				3		–	J3-8
+10V UNREG	A6P1-19,41	+10V Unregulated												19,41	42				–		A9C1(+)	–
±10V RET	A6P1-17,18, 39,40	±10V Return												17,18, 39,40	13,35				4,13		A9C1(–),A9C4(+)	J3-3,16
+5VA	A7P1-2,24	+5V Regulated for 8350A	–	–	–		3,4, 25,26	3,4, 25,26		3,4, 25,26		3,4, 25,26		23	2,24		44	30		6	A9F3	J2-30,J13-6
+5VAFP	A7P1-25	+5V Regulated for Front Panel	–	–	–		–	–		–		–		–	25		–	–		–	A9E8	–
+5VB	A7P1-5,6, 28	+5V Regulated for RF Plug-in	–	–	–		–	–		–		–		–	5,6, 28		–	18,50, 51		–	–	J2-18,50,51
+5V BAT	BT1	+5V Battery (Option 001 only)	–	–	–		–	21		–		–		–	–		–	–		–	–	BT1
+5VB GND REF	A7P1-7	+5VB Ground Reference	–	–	–		–	–		–		–		–	7		–	21		–	–	J2-21
+5VF SENSE	A2J3-33	+5VAFP Sense	33	–	33		–	–		–		–		–	–		–	–		–	–	–
+5VR	A2J3-17,18	+5V Rotary Pulse Generator	17,18	–	17,18		–	–		–		–		–	–		–	–		–	–	–
+5V RET	A6P1-11,12, 33,34, 35	+5V Return	–		–		–	–		–		–		11,12, 33,34, 35	–		–	–		–	A9C5(–)	–
+5V UNREG	A6P1-13,14, 15,36, 37	+5V Unregulated	–	–	–		–	–		–		–		13,14, 15,36, 37	3,26		–	62,63		–	A9F2,A9C5(+)	J2-62,63
–10V	A7P1-11,33	–10V Regulated												–	11,33				10		A9F1	J3-13
–10V RET SENSE	J3-12	–10V Return Sense												–	12				12		–	J3-12
–10V SENSE	J3-4	–10V Sense												–	34				11		–	J3-4
–10V UNREG	A6P1-16,38	–10V Unregulated												16,38	10,32				9		A9C4(–)	J3-5
–15V	A7P1-14,36	–15V Regulated									4,26		4,26	–	14,36			28			–	J2-28
–15V UNREG	A6P1-20,42	–15V Unregulated									–		–	20,42	37			–			A9C2(–)	–
–40V	A6P1-4,26, 27	–40V Regulated												4,26, 27	20				14		A9C7(–)	J3-11
–40V RET	A7P1-44	–40V Return												–	44				17		–	J3-1
–40V RET SENSE	J3-10	–40V Return Sense												–	21				16		–	J3-10
–40V SENSE	J3-2	–40V Sense												–	22				15		–	J3-2
–40V UNREG RET	A6P1-5,6, 28	–40V Unregulated Return												5, 6, 28	43				–		A9C7(+)	–
GND ANLG	SYSTEM GROUND	Ground Analog								2,11, 12,22, 24,33, 34	1,22, 23,24	2,11, 12,22, 24	1,22, 23,44		9,31			27,58, 59			W10,A9E5	J2-27,58,59, J1,J8
GND DIG	SYSTEM GROUND	Ground Digital					1,2,5, 10,12, 14,19, 22,24, 27,32, 35,36, 40	2,5,14, 15,22, 23,24, 27,36, 38,40, 43,44	2,7,10, 12,18, 21,22, 23,28, 30,32, 34,39, 43,44	1,5,10, 23,27, 32,35, 36,38, 41,44	10,12, 21,25, 31,32, 43	1,5,10, 23,27, 32,35, 36,38, 41,44	9,10, 21,31, 32,43	1	1,23		4,9,17, 23,25, 26,31, 34,39, 41,42	1,6,9, 14,16, 31,37, 46,48, 49		19	A9E9	J2-1,6,9, 14,16,31, 37,46,48, 49,J13-19, BT1
GND HP-IB	J4-18 to 23	HP-IB Ground Returns	–		–								13-19								–	J4-18-23
GND R	A2J3-22, 23,24	Ground Rotary Pulse Gen.	22,23, 24		22,23, 24								–								–	–
SHIELD HP-IB	J4-12	HP-IB Cable Shield	–		–								–								CHASSIS	J4-12

Figure 8-62. Motherboard Wiring List (5 of 5)

Table 8-55. 8350A Cable List

Cable	Description	Connections
W1	Cable Assy, Ribbon 34C, A1/A2 Interconnect	A2J3 – Front Panel Interface A1J1 – Front Panel
W2	Cable Assy, Ribbon 50C, A1/A2 Interconnect	A2J4 – Front Panel Interface A1J2 – Front Panel
W3	Cable Assy, Coax, Brown, VTUNE	A4J1 – Scaling and Marker Assy J3 – Plug-in Pwr Supply Interface
W4	Cable Assy, Ribbon 64C, Plug-in Interface	A9J1 – Motherboard J2 – Plug-in Interface
W5	Cable Assy, Ribbon 26C, HP-IB	A8J1 – HP-IB Interface Assy J4 – HP-IB Interface (rear panel)
W6	Cable Assy, 17 pin, Plug-in Pwr Supply Interface	A9J2 – Motherboard J3 – Plug-in Pwr Supply Interface
W7	Cable Assy, Ribbon 25C, Programming/ALT SWP Interface	A9J3 – Motherboard J13 – PROGRAMMING CONNECTOR (rear panel) J14 – ALT SWP INTERFACE (rear panel)
W8	Cable Assy, Coax-Orange, FM	J11 – FM INPUT (rear panel) J3 – Plug-in Pwr Supply Interface
W9	Cable Assy, Coax-Yellow, AM	J12 – AM INPUT (rear panel) J3 – Plug-in Pwr Supply Interface
W10	Cable Assy, Rear Panel	J7 – PEN LIFT (rear panel)/ A9E1 Motherboard J8 – SWEEP OUT/IN (rear panel)/A9E2 Motherboard J10 – STOP SWEEP (rear panel)/ A9E3 Motherboard J6 – NEG Z BLANK (rear panel)/ A9E4 Motherboard Chassis ground/ A9E5 Motherboard J5 – POS Z BLANK (rear panel)/ A9E6 Motherboard J9 – CNTR TRIG (rear panel)/ A9E7 Motherboard

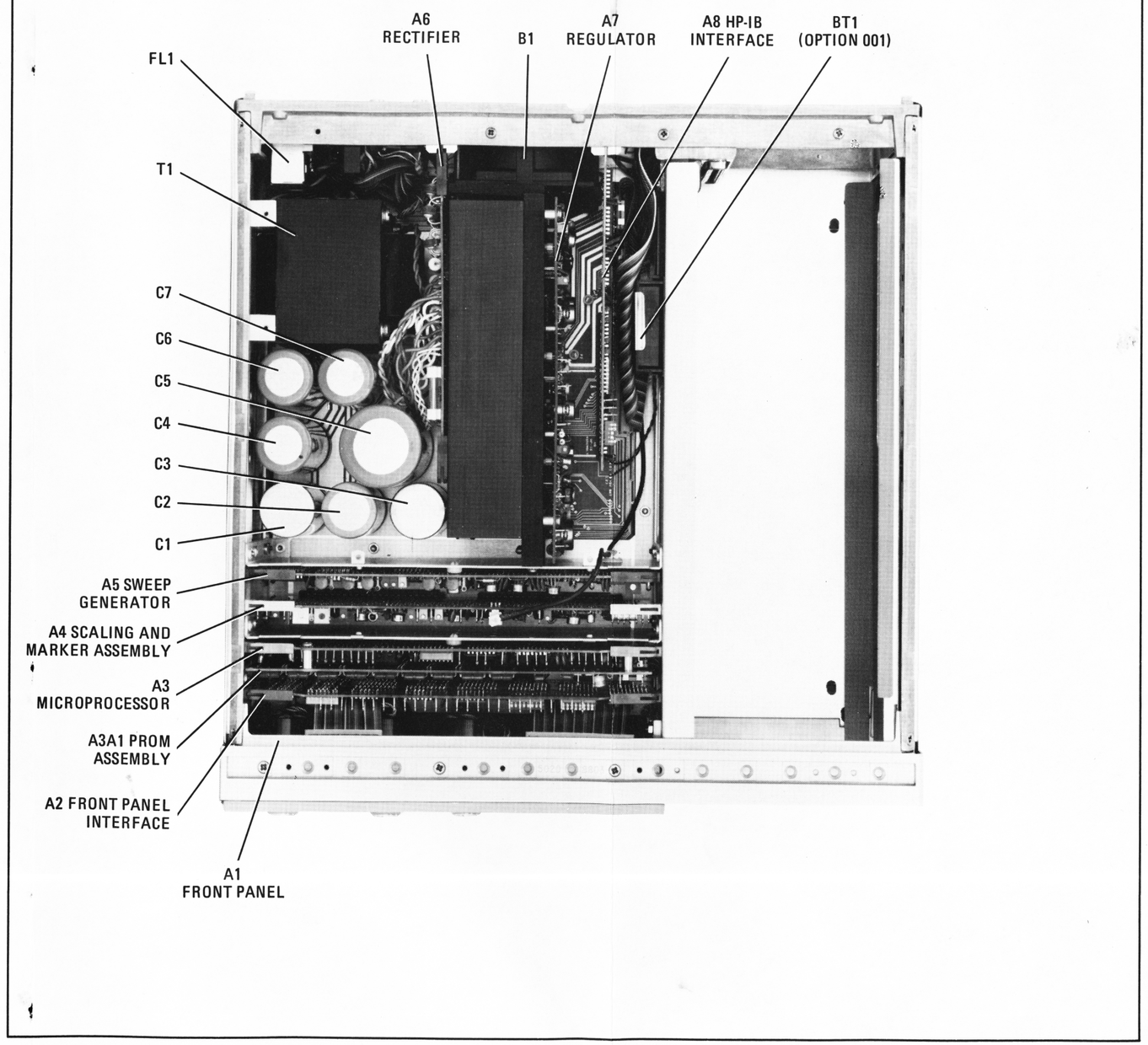


Figure 8-63. Major Assemblies Locations