# SYNTHESIZED SIGNAL GENERATOR 8660C 

Including Options 001, 002,003, 004, 005 and 100

## SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed 1416A.

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

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Thanks


Dave \& Lynn Henderson
Artek Media

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## NOTE

Although this is a Class 1 instrument, all warning, grounding, safety and voltage information is repeated here to ensure that all users of the instrument are aware of the safety and other precautions required to assure that the instrument is operated properly. The information is repeated at appropriate intervals throughout the manual.

## WARNINGS

## SAFETY

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on:
a. If this instrument is to be energized via an autotransformer for voltage reduction, make sure that the common terminal is connected to the earthed pole of the power source.
b. The power cable plug shall only be inserted into a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord without a protective conductor (grounding).
c. Before switching on the instrument, the protective earth terminal of the instrument must be connected to a protective conductor of the power cord. This is accomplished by ensuring that the instrument's internal earth terminal is correctly connected to the instrument's chassis and that the power cord is wired correctly.

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation. Such equipment should be suitably tagged explaining the cause of malfunction, and include a warning that the equipment is not to be used until the malfunction is corrected.

Any interruption of the protective (grounding) conductor inside or outside the instrument or disconnection of the protective earth terminal is likely to make the instrument dangerous. Intentional interruption is prohibited.

## HIGH VOLTAGE

Any adjustment, maintenance, and repair of the opened instrument under voltage should be
avoided as much as possible and, if inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

## FUSES

Make sure that only fuses with the required rated current and of the specified type (normal blow time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.


## GROUNDING

Any interruption of the protective (grounding) conductor inside or outside the instrument is likely to cause damage, this instrument and all line powered devices connected to it must be connected to the same earth ground (see Section II).

## LINE VOLTAGE

Be sure to select the correct fuse rating for the selected line voltage (see LINE VOLTAGE SELECTION in Section II); fuse ratings are listed on the fuse compartment.

To prevent damage to the instrument, make the line voltage selection BEFORE connecting line power. Also ensure that the line power cord is connected to a line power socket that is provided with a protective earth contact.

## SAFETY

To avoid the possibility of damage to test equipment, read completely through each test before starting it. Make any preliminary control settings necessary for correct test equipment operation.


RACK MOUNTING KIT

Figure 1-1. Model 8660C and Accessories Supplied

# SECTION I <br> GENERAL INFORMATION 

## 1-1. INTRODUCTION

1-2. This manual contains all information required to install, operate, test, adjust and service the Hewlett-Packard Model 8660C Synthesized Signal Generator mainframe. This section covers instrument identification, specifications and other basic information. Figure 1-1 shows a front view of the instrument and accessories supplied.

1-3. The other various sections of this manual provide information as follows:
a. SECTION II, INS'TALLATION, provides information relative to incoming inspection, power requirements, mounting, packing for shipment, etc.
b. SECTION III, OPERATION, provides information relative to operating the instrument.
c. SECTION IV, PERFORMANCE TESTS, provides information required to ascertain that the instrument is performing in accordance with published specifications.
d. SECTION V, ADJUSTMENTS, provides information required to properly adjust and align the instrument after repairs are made.
e. SECTION VI, REPLACEABLE PARTS, provides ordering information for all replaceable parts and assemblies.
f. SECTION VII, MANUAL CHANGES, normally will contain no relevant changes in the original issue of a manual. This section is reserved to provide backdated and up-dated information in manual revision or reprints.
g. SECTION VIII, SERVICE, includes all information required to service the instrument when a malfunction occurs.

1-4. Packaged with this instrument is an Operating Information Supplement. This is simply a copy of the first three sections of this manual (less Table 1-2). This supplement should stay with the instrument for use by the operator. Additional copies of the Operating Information Supplement may be ordered separately through your nearest Hewlett-

Packard office. The part number is listed on the inside title page of this manual below the Manual Part Number.

1-5. Also listed on the inside title page of this manual, below the manual part number, is a "Microfiche" part number. This number may be used to order $4 \times 6$ inch microfilm transparancies of the manual. Each microfiche contains up to 60 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes Supplement as well as all pertinent Service Notes.

## 1-6. SPECIFICATIONS

1-7. Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument may be tested.

## 1-8. INSTRUMENTS COVERED BY MANUAL

1-9. This instrument has a two-part serial number. The first four digits and the letter comprise the serial number prefix. The last five digits form the sequential suffix that is unique to each instrument. The contents of this manual apply directly to instruments having the same serial number prefix(es) as listed under SERIAL NUMBERS on the inside title page.

1-10. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the inside title page. This unlisted serial prefix indicates that the instrument is different from those documented in this manual. The manual for this instrument is supplied with a yellow Manual Changes supplement that contains "change information" that documents the differences.

1-11. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement for this manual. The supplement for this manual is keyed to this manual's print date and part number, both of

## SPECIFICATIONS

## Frequency Selection:

Keyboard control panel allows selection of CW (or center frequency) by entry keys or synthesized tuning dial. Least significant digit either 1 Hz (standard) or 100 Hz (Option 004).*

## Reference Oscillator:

Internal: 10 MHz quartz oscillator. Aging rate less than $\pm 3$ parts in $10^{8}$ per 24 hours after 72 hour warmup ( $\pm 3$ parts in $10^{9}$ per 24 hours after 30 day warmup, Option 001).
External: Rear panel switch allows operation from any 5 MHz or 10 MHz signal at a level between 0.2 V and 2.0 V rms into 170 ohms. Stability and spectral purity will be partially determined by characteristics of external reference oscillator.

## Reference Output:

Rear panel BNC connector provides output of signal selected (INT. or EXT.) at the following levels into 170 ohms:
Internal Reference: 0.5 V to 1 V rms.
External Reference: Nominally equal to external input.

## Display:

Ten-digit numerical LED display of CW frequency is active in either local or remote mode. Springloaded pushbuttons provide display of sweep width, selected step size, or characters being entered on the keyboard.

## Synthesized Search:

Synthesized search dial changes the synthesized output frequency 180 steps per revolution (with the 86601A, the COARSE and STEP tuning are desensitized to 36 steps/revolution). Step sizes are 1 Hz , $1 \mathrm{kHz}, 1 \mathrm{MHz}$, or any step size entered through the keyboard.

## Digital Sweep:

Type: Symmetrical about CW/center frequency. Sweep width is divided into 100 synthesized steps for fastest sweep speed or 100 steps for slower speeds or Manual Sweep.
Sweep Width: Continuously adjustable over range of RF section installed. Smallest step size is equal to frequency resolution of mainframe.
Sweep End Point Accuracy: Same as reference oscillator accuracy.

Sweep Speed: Selectable $0.1 \mathrm{sec}, 1 \mathrm{sec}$, or 50 sec per sweep (Auto or Single).
Sweep Output: 0 to +8 V stepped ramp, 100 or 1000 equal steps depending on sweep speed.
Manual Sweep: Synthesized search dial allows manual sweep over width selected in 1000 steps (LED display follows output frequency during manual sweep).
Single Sweep: Initiated by momentary contact pushbutton.

## Frequency Stepping:

After a step size has been entered on the keyboard, depressing STEP $\uparrow$ or STEP $\downarrow$ button will increment frequency up or down by the desired step size.
Step Accuracy: Same as reference oscillator accuracy.

## REMOTE PROGRAMMING

CW frequency, frequency stepping (STEP $\uparrow$ or STEP $\downarrow$ ) and output level, and most modulation functions are programmable. Note: digital sweep is NOT programmable.

## Frequency:

CW frequency is programmable over entire range with same resolution obtained in manual operation.

## Frequency Step:

STEP $\uparrow$ or STEP $\downarrow$ may also be programmed to change output frequency by a previously selected step size.

## Output Level:

Programmable in 1 dB steps over the output range of the RF section installed (for output level accuracy see RF section specifications).

Modulation: See specifications for modulation and RF section installed.

## Programming Input:

Connector Type: 36 pin Cinch type (mating connector supplied). (Optional HP-IB interface; 24 pin Cinch type 57 (mating connector NOT supplied)).
Logic: TTL compatible (negative true) " 0 " logic state corresponds to +2 V or higher. " 1 " logic state corresponds to +0.8 V or lower.
Internal Fan-in from Programming Connector:
10; (required current approximately 15 mA per line in the " 1 " state).

[^0]Table 1-1. Model 8660C Specifications (2 of 2)

| GENERAL |  |
| :---: | :---: |
| Operating Temperature Range: $0^{\circ}$ to $+55^{\circ} \mathrm{C}$. | Options: |
| Leakage: Meets radiated and conducted limits of MIL I-6181D. | Option 001: $\pm 3 \times 10^{-9} /$ day internal reference oscillator. <br> Option 002: No internal reference oscillator. |
| er: 100, 120, 200 | Option 003: Operation from 50 to 400 Hz line. |
| $48-66 \mathrm{~Hz} .400 \mathrm{VA}$ maximum. | Option 004: 100 Hz frequency resolution $(200 \mathrm{~Hz}$ above 1300 MHz center frequency.) |
| Weight: (Mainframe only): Net, $23.2 \mathrm{~kg}(51 \mathrm{lb})$, Shipping $28.6 \mathrm{~kg}(63 \mathrm{lb})$. | Option 005: HP-IB programming interface. Option 100: 11661B factory installed. |

which appear on the inside title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-12. For information concerning a serial number prefix not listed on the inside title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

## 1-13. DESCRIPTION

1-14. The Model 8660C Synthesized Signal Generator Mainframe requires two plug-in sections to provide a useable RF output. The plug-ins required are an RF Section and a Modulation (or Auxiliary) Section. These plug-in sections are inserted into the front of the Model 8660 C ; all operating controls are on the front panels of the plug-in sections or on the mainframe panel.

1-15. An internal plug-in unit, the Frequency Extension Module (HP accessory number 11661) is required when any RF Section other than the HP Model 86601 is in use.

## 1-16. GENERAL OPERATING PRINCIPLES

1-17. All of the signals generated in the Model 8660 C are phase locked, directly or indirectly, to a 100 MHz master oscillator in the reference section. The 100 MHz master oscillator is phase locked to an internal temperature controlled oscillator or to an external standard. Provisions are made for the internal oscillator to be used as a reference signal for other equipment.

1-18. The Model 8660C uses synthesizer techniques to provide digitally controlled, precise RF signals which are used in the RF Section output plug-ins to produce the selected output frequency. The output frequencies are exactly those selected
in 1 Hz or 2 Hz increments in the standard instruments, or in 100 Hz or 200 Hz increments in Option 004 instruments.

1-19. Six phase locked loops, (four in Option 004 instruments), all phase locked to the 100 MHz master oscillator, are used to generate the RF signals used in the RF Section plug-ins to produce the final output signal.

1 -20. The Model 8660 C output frequency may be selected by front panel controls or by a remote programming device.

1-21. Operating of the plug-in sections may also be remotely programmed through the mainframe circuits.

1-22. Descriptions, operating instructions and service information for the various plug-in sections is provided in separate manuals.

## NOTE

The 8660 family, and plug-ins available are described briefly on the first foldout Sheet.

## 1-23. OPTIONS

1-24. Option 001: Reference Oscillator with $\pm 3$ $\times 10^{-9} /$ per day stability.

1-25. Option 002: No internal standard reference oscillator.

1-26. Option 003: 50 to 400 Hz ac operation.
1-27. Option 004: 100 Hz resolution below $1300 \mathrm{MHz}, 200 \mathrm{~Hz}$ resolution above 1300 MHz .

1-28. Option 005: Hewlett-Packard Interface Bus installed instead of BCD interface. HP-IB utilizes some ASCII interface codes (also previously referred to as General Purpose Interface Bus).

1-29. Option 100: Adds an internal plug-in, the 11661 (for use with an 86602 or 86603 RF Section) before the instrument is shipped from the factory.

## 1-30. EQUIPMENT REQUIRED BUT NOT SUPPLIED

1-31. An RF Section and a Modulation or Auxildiary Section must be installed in the Model 8660C mainframe. In addition when an RF Section such as the 86602 or 86603 , is used, the internal Frequency Extension Module (Model 11661) must be used.

## 1-32. EQUIPMENT AVAILABLE

1-33. A service kit, Hewlett-Packard accessory number 11672 A , is recommended for servicing and adjusting the mainframe and the plug-in sections. Contents of the service kit are listed in Table 1-2. Individual items in the kit may be ordered searately if desired.

## 1-34. ACCESSORIES SUPPLIED

$1-35$. The following accessories are provided with the Model 8660C:
a. A detachable three-wire power cable. The type of power cord will be determined by the shipment destination.
b. A rack mounting kit part number 08660-60070, consisting of the following:

| 1 | CONNECTOR: RF STRAIGHT ADAPTER | $1250-0780$ |
| :--- | :--- | :--- |
| 3 | SCREW, MACHINE $6-32$ | $2360-0180$ |
| 8 | SCREW, MACHINE $8-32 \times 0.31$ | $2510-0043$ |
| 1 | BRACKET TH LEFT HAND RACK MOUNT | $5020-7623$ |
| 1 | BRACKET TH RIGHT HAND RACK MOUNT | $5020-7624$ |
| 1 | EXTENSION BOARD ASSY 20 CONTACT | $5060-0256$ |
| 1 | EXTENSION BOARD ASSY 24 CONTACT | $5060-0258$ |
| 2 | EXTENDER BOARD ASSY 15 PIN | $5060-0276$ |
| 1 | EXTENDER BOARD ASSY 18 PIN | $5060-0277$ |
| 1 | STRIP, FILLER "02" | $5580-2042$ |
| 1 | PLUG, 36 CONTACT MALE W/HOOD AND |  |
|  | CLAMP | $1251-0084$ |

## 1-36. WARRANTY

1-37. Certification and warranty information for the Model 8660 C appears on the inside front cover of this manual.

## 1-38. TEST EQUIPMENT AND ACCESSORIES

1-39. Table 1-2 lists the test equipment and accessories recommended to test, adjust and service the Model 8660C.

## 1-40. ELECTRICAL PROTECTION

1-41. The safety classification of this instrument is Safety Class I.

1-42. This apparatus has been designed and tested to operate in a safe manner. The Operating and Service Manual contains information, warnings and cautions which must be followed by the user to ensure safe operation and to retain safe operating conditions.

Table 1-2. Test Equipment and Accessories List (1 of 2)

| Item | Minimum Specifications | Suggested Model | Use* |
| :---: | :---: | :---: | :---: |
| Digital Voltmeter | $\begin{aligned} & \text { Voltage Accuracy } \pm 0.01 \% \\ & 0.000 \mathrm{~V} \text { to } 8.0 \mathrm{~V} \end{aligned}$ | HP Model 3480 with 3482 plug-in | P, A, S |
| AC Microvoltmeter | $3 \mu \mathrm{~V}$ to 3 V Tuneable to 120 Hz | HP 3410A | A, S |
| Variable Voltage Transformer | Range 103 to 127 Vac <br> Meter Range 103-127 Vac $\pm 1 \mathrm{~V}$ | General Radio W4MT3A | A |
| VLF Comparator | Sensitivity $1 \mu \mathrm{~V}$ into 50 ohms; Compares 100 kHz input to NBS station WWVB | HP 117A | P, A |
| Oscilloscope | Frequency dc to 50 MHz Time base 10 ns to 1 s Time base accuracy $3 \%$ | HP 180A with HP 1801A and HP 1821A plug-ins | P, A, S |
| 10:1 Divider Probes | 10:1 Divider 10 Megohm 10 pF | HP 10004A (2) |  |
| Spectrum Analyzer | Frequency Range 10 to 600 MHz , <br> Response $\pm 1 \mathrm{~dB}$, <br> Measurement Accuracy $\pm 2.0 \mathrm{~dB}$ | HP 140/HP 8554B/ HP 8552 | A, S |
| Frequency Counter | Range $0-50 \mathrm{MHz}, 0-500 \mathrm{MHz}$ with plug-in accuracy $\pm 1$ count $\pm$ time base accuracy. <br> External time base 10 MHz | HP 5245 M with HP 5253 plug-in | P, A, S |
| Pulse Generator | Pulse rate 100 kHz <br> Pulse width $0.035 \mu \mathrm{sec}$ <br> Amplitude 0.5 V <br> Polarity - Selectable | HP 222A | A |
| Signal Generator/ Sweeper | Frequency $-1-110 \mathrm{MHz}$ <br> Output Range +20 to -20 dBm <br> Output CW or swept | HP 8601A | P, A, S |
| RF Voltmeter | Range 0.1 to 2 V <br> Frequency Range 1 to 10 MHz | HP 411A | P |
| Test Oscillator | Freq. Range 10 Hz to 1 kHz Output Level +10 to -20 dBm | HP 651B | A, S |
| Frequency Synthesizer | Freq. Accuracy $0.001 \%$ Freq. Stability $\pm 10$ parts in $10^{6}$ per year | HP 3320B | P |
| Marked Card Programmer | Capable of programming either BCD or HP-IB bus data | HP 3260A | S |
| Logic Analyzer | Sequential display of 16 12-bit binary words | HP 1601 with HP 180 Oscilloscope | P, S |

Table 1-2. Test Equipment and Accessories List (2 of 2)


# SECTION II <br> INSTALLATION 

## 2-1. INTRODUCTION

2-2. This section provides information on incoming inspection, selecting the input line voltage, operating environment, and information applicable to bench and rack mounted operation of the Model 8660C.

## 2-3. INITIAL INSPECTION

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged it should be kept until the contents of the shipment have been checked mechanically and electrically. The contents of the shipment are shown in Figure 1-1, and the procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defects, or if the instrument does not pass the electrical performance test, notify the nearest Hewlett-Packard office. If the shipping container is damaged or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection. The HP office will arrange for repair or replacement without waiting for claim settlements.
$2-5$. The warranty statement for the instrument is on the inside front cover of this manual. Contact the nearest Sales/Service Office for information relative to warranty claims.

## 2-6. PREPARATION FOR USE

## 2-7. Power Requirements

$2-8$. The Model 8660C Synthesized Signal Generator requires a power source of $100,120,220$ or 240 Vac $+5 \%,-10 \%, 48$ to 66 Hz signal phase. Power consumption is 400 VA maximum.

## 2-9. Line Voltage Selection

## CAUTION

To prevent damage to the instrument make the line voltage selection BEFORE connecting the line power. Also ensure the line power cord is connected to a line power circuit that is provided with a protective earth contact.

2-10. A rear panel line power module, (A7), permits operation from $100,120,220$, or 240 Vac. The number visible in the window (located on the module) indicates the nominal line voltage to which the instrument must be connected.

2-11. To prepare the instrument for operation, slide the fuse compartment cover to the left (the line power cable must be disconnected). Pull the handle marked FUSE PULL and remove the fuse; rotate the handle to the left. Gently pull the printed circuit voltage selector card from its slot and orient it so that the desired operating voltage appears on the top-left side (see Figure 2-1). Firmly push the voltage selector card back into its slot. Rotate the FUSE PULL handle to the right, install a fuse of the correct rating, and slide the fuse compartment cover to the right.

## WARNING

To avoid the possibility of injury or death, the following precautions must be followed before the instrument is switched on:
a. Note that the protection provided by grounding the instrument cabinet may be lost if any power cable other than the three-pronged type supplied is used to couple the ac line voltage to the instrument.
b. If this instrument is to be energized via an autotransformer to reduce or increase the line voltage, make sure that the common terminal is connected to the earthed pole of the power source.
c. The power cable plug shall only be inserted into a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord without a protective conductor (grounding).
d. Before switching on the instrument, the protective earth terminal of the instrument must be connected to a protective conductor of the power cord. This is accomplished by ensuring that the instrument's internal earth terminal is correctly connected to the instrument's chassis and that the power cord is wired correctly.


Figure 2-1. Line Voltage Selection

## NOTE

The correct fuse rating for the line voltage selected is listed on the line power module. More information about fuses is given in the table of replaceable parts in Section VI (reference designation is A7F1).

## 2-12. Power Cable

2-13. In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate power line outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Refer to Figure 2-2 for the part numbers of the power cable plugs available.

## 2-14. Mating Connectors

$2-15$. Internal mating connectors between the Model 8660 C and the plug-in sections are in fixed positions. Refer to Figure 8-118 for plug-in con-
nector information. Refer to Figure 8-106 for information relative to the remote control connector, J3.

## 2-16. Operating Environment

$2-17$. The operating environment should be within the following limitations:

| Temperature |  | . | . | . | . | . | 0 to $55^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | ---: |
| Humidity | . | . | . | . | . | . | . |
| Altitude | . | . | . | . | . | . | . |

2-18. A forced air cooling system is used to maintain the operating temperature required by the instrument. The air exhaust fan is located on the rear panel of the instrument; the air intake is through the side panels of the instrument. When operating the instrument, choose a location that provides at least three inches of clearance at the rear and at least an inch of clearance for each side. The clearances provided by the plastic feet in bench stacking and the filler strip in rack mounting are adequate for the top and bottom cabinet surfaces.


Figure 2-2. Power Cable HP Part Numbers

## 2-19. Bench Operation

2-20. The instrument has plastic feet and a foldaway tilt stand for convenience in bench operation. The tilt stand raises the front of the instrument for easier viewing of the control panel and the plastic feet are shaped to make full width modular instruments self aligning when stacked.

## 2-21. Rack Mounting

$2-22$. This instrument is supplied with a rack mounting kit. This kit contains all the necessary hardware and installation instructions for mounting the instrument in a rack with 19 inch spacing (see Figure 2-3).

## 2-23. STORAGE AND SHIPMENT

## 2-24. Environment

$2-25$. The instrument should be stored in a clean, dry environment. The following environmental limitations apply to both storage and shipment:
$\begin{array}{llllllll}\text { Temperature } & & . & . & . & . & -40^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C} \\ \text { Humidity } & . & . & . & . & . & <95 \% \text { relative } \\ \text { Altitude } & . & . & . & . & . & <20,000 \text { feet }\end{array}$

## 2-26. Packaging

2-27. Original Packaging. Containers and materials identical to those used in factory packaging are


Figure 2-3. Preparation for Rack Mounting
available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also, mark the container FRAGILE to assure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-28. Other Packaging. The following general instructions should be used for re-packaging with commercially available materials:
a. Wrap the instrument in heavy paper or plastic. (If shipping to a Hewlett-Packard office or service center, attach a tag indicating the type of service required, return address, model number, and full serial number.)
b. Use a strong shipping container. A doublewall carton made of 250 -pound test material is adequate.
c. Use enough shock-absorbing material (3 to 4 -inch layer) around all sides of the instrument to provide firm cushion and prevent movement inside the container. Protect the control panel with cardboard.
d. Seal the shipping container securely.
e. Mark the shipping container FRAGILE to assure careful handling.

## SECTION III OPERATION

## 3-1. INTRODUCTION

3-2. This section provides operating instructions for the Hewlett-Packard Model 8660C Synthesized Signal Generator mainframe for both the local and remote modes.

3-3. The Model 8660 C is designed to provide precise digitally controlled signals for use in plug-in sections which provide the selected output frequency with the chosen modulation parameters. It will be necessary to have the operating manuals for the plug-in sections being used in order to efficiently operate the instrument.

## NOTE

If a Modulation plug-in Section is not used it will be necessary to have an Auxiliary Section in place of the Modulation Section. The Auxiliary Section completes a signal path from the mainframe to the RF Section plug-in and also provides a means of modulating the $R F$ Section from an external source.

## 3-4. PANEL FEATURES

$3-5$. Front and rear panel controls, indicators and connectors of the 8660 C are shown, and their functions described, in Figure 3-1.

## 3-6. OPERATOR'S MAINTENANCE

3-7. Operator's maintenance of the Model 8660C Synthesized Signal Generator mainframe is limited to fuse replacement.

## 3-8. OPERATING PRINCIPLES

3-9. The Model 8660 C may be operated by front panel controls in the local mode or externally programmed in the remote mode.

## WARNING

The power requirements and safety precautions listed throughout this Manual must be observed to preserve the built-in safety features of the Model 8660C.

## 3-10. LOCAL OPERATION

3-11. In the local mode of operation, all functions of the mainframe are controlled by front panel controls, except when an external reference oscillator is used. When an external reference oscillator is used, the rear panel SELECTOR switch must be in the EXT position.

## 3-12. The 20 -key keyboard may be used to:

a. Select any frequency within the range of the RF Section plug-in in 1 Hz increments (above $1300 \mathrm{MHz}, 2 \mathrm{~Hz}$ increments) for standard instruments. Option 004 instruments are selectable in 100 Hz increments (above $1300 \mathrm{MHz}, 200 \mathrm{~Hz}$ increments).

## NOTE

> Frequencies which are above the output frequency range of the RF Section, if selected, will be stored in the keyboard register, but the information will not be transferred to the center frequency register. The center frequency register and the readout will retain the last valid input. Frequencies below the output frequency range of the RF Section will be transferred to the center frequency register and the output register; the output frequency will be accurate but the output amplitude will be degraded. As an example, the Model 86601A RF Section has a specified lower frequency limit of 10 kHz , but typically will produce a useable RF output down to 3 kHz or lower.
b. When frequencies below the RF Section frequency range are selected, the OUT OF RNG lamp lights and remains lit.
c. Select any desired sweep width within the frequency range of the RF Section in use. See paragraph 3-14 for further details of sweep operation.
d. Select any incremental step within the frequency range of the RF Section in use. See


Figure 3-1. Front and Rear Panel Controls, Indicators and Connectors (1 of 2)
(1) KYBD pushbutton. When pressed, causes the information stored in the keyboard storage register to be displayed on the CENTER FREQUENCY readout.
(2) STEP pushbutton. When pressed, causes the information stored in the step storage register to be displayed on the CENTER FREQUENCY readout.

3 SWP WIDTH pushbutton. When pressed, causes the information stored in the sweep width storage register to be displayed on the CENTER FREQUENCY readout.
4) LINE STBY - ON switch. In the STBY position, with the instrument connected to the ac line source, the reference oscillator oven temperature is maintained at the operating temperature to avoid the necessity of allowing for a warm up period each time the instrument is used.
(5) CENTER FREQUENCY readout. Normally displays the output center frequency of the RF Section.
(6) ANNUNCIATIR. Provides visual display of mode of operation, crystal oven temperature and out of range frequency selection.
(1) MANUAL MODE RESOLUTION. Works in conjunction with the TUNING control to step the rf output in steps of 1 Hz (FINE), 1 kHz (MED) and 1 MHz (COARSE). In the STEP position the TUNING control steps the rf output frequency by the step stored in the step register.
(8) TUNING - MANUAL SWEEP. Works as specified in the MANUAL MODE RESOLUTION description. May also be used to set the rf output to any point within the limits stored in the sweep register when the SWEEP MODE switch is set to MAN.
(9) Keyboard. Contains 20 keys which are used to enter data or instructions as follows:

Numerals 0 through 9
Decimal Point (.)
CLEAR KYBD. Clears keyboard register (does NOT clear other registers).
$\mathrm{GHz}, \mathrm{MHz}, \mathrm{kHz}$ and Hz select frequency in conjunction with numeric keys.

CF. Transfers keyboard storage register data to the center frequency register.

STEP. $\uparrow$ Transfers keyboard storage register data to the step register and steps the center frequency up. May also be used to step the frequency up by the step stored in the step register without a new keyboard entry.
STEP. $\downarrow$ Same as STEP $\uparrow$ except that frequency is stepped down.
SWP WIDTH. Transfers the data in the keyboard storage register to the sweep register.
(10)

SINGLE pushbutton. In the SINGLE mode, when pressed, causes the rf output to be swept, one time only, across the range stored in the sweep register, at a speed determined by the RATE switch.

11 OUTPUT ( 0 to +8 V ). Provides a sweep ramp for use in external equipment (oscilloscopes, X-Y recorders, etc.) when operating in the swept mode.
(12) RATE switch. The rate switch selects sweep rates as follows: FAST - 100 steps at 1 millisecond per step, MED - 1000 steps at 1 millisecond per step, and SLO -1000 steps at 50 milliseconds per step.
(13) SWEEP MODE switch. With the sweep mode switch in the AUTO position sweep operation is automatic; the output rf is swept about the center frequency by the data stored in the sweep register at the rate selected by the RATE switch. In the SINGLE mode the rf output is swept once each time the SINGLE pushbutton is pressed. In the MAN mode the sweep is controlled by the MANUAL TUNE control and the data stored in the sweep register.
14 LINE MODULE. Contains a means of switching input line voltage to $100 / 120 / 220 / 240 \mathrm{Vac}+5 \%-10 \%$, fuse, line cable connector and filtering. NOTE: the cabinet (earth) ground is also applied through the line module.
(15) REFERENCE INPUT. Used when an external standard of 5 or 10 MHz is used.

16 REFERENCE OUTPUT. Provides the capability of using the internal reference as a time base in external equipment.

SELECTOR. Selects INT or EXT reference.
(18) REMOTE INPUTS. When the instrument is operated in the remote mode (pin 5 of this connector is grounded by the programming device), all functions of the instrument are controiled by the remote programming device. Front panel controls (except for LINE STBY-ON) have no effect on operation of the instrument.
paragraph 3-18 for further details of incremental step operation.

## 3-13. Operating Modes

3-14. Sweep. In the sweep mode the sweep width is selected by the keyboard. The sweep width may be displayed on the CENTER FREQUENCY readout by pressing the SWP WIDTH pushbutton to the left of the readout. Only the center frequency is shown in the AUTO or SINGLE SWEEP modes. In the MAN sweep mode the actual RF output frequency of the RF Section will be displayed.

3-15. When the SWEEP MODE switch is placed in the AUTO position the output signal of the RF Section is swept about the selected center frequency by the selected sweep width. (Example: center frequency 50 MHz , sweep width 20 MHz , the RF output is swept from 40 to 60 MHz .) The sweep rate, selected by the RATE switch is as follows: FAST -100 steps at 1 millisecond per step, MED - 1000 steps at 1 millisecond per step and SLO -1000 steps at 50 milliseconds per step.
$3-16$. When the SWEEP MODE switch is placed in the SINGLE position, pressing the SINGLE pushbutton causes the output of the RF Section to be swept one time. When the single sweep is completed, the output of the RF Section returns to the selected center frequency. The sweep width and sweep rate are selected in the same manner as they are in the AUTO mode.

3-17. When the SWEEP MODE switch is placed in the MAN position the step rate of the output frequency of the RF Section may be manually controlled by the MANUAL SWEEP control. In this mode the sweep width is still controlled by the information in the sweep register. The selected sweep width, in this mode, is divided by 1000 and the output of the RF Section may be controlled in frequency steps that are $1 / 1000$ of the sweep width. (Example: center frequency 50 MHz , sweep width 20 MHz , output may be swept manually from 40 to 60 MHz in 20 kHz steps.)

3-18. Step. The center frequency may be stepped up or down, in any increment within the frequency range of the RF Section in use. The increnent selected, including units, must be entered in the keyboard before the STEP $\uparrow$ or STEP $\downarrow$ key is pressed. The step entered into the step register remains in the register until changed (or the instrument is place; in the standby mode) and may
be displayed on the readout by pressing a STEP pushbutton.

3-19. When the MANUAL SWEEP control, a Rotary Pulse Generator, is used to control the STEP mode, the size of the step is determined by the information stored in the STEP register.

3-20. Manual. Manual mode operation is essentially the same as the step mode except that increments selected by the MANUAL MODE switch are 1 Hz (FINE), 1 kHz (MED) and 1 MHz (COARSE). These increments are controlled only by the TUNING control when the MANUAL MODE switch is placed in the selected position.

3-21. Combined. The sweep mode, step mode and manual mode may all be used simultaneously except for Manual Sweep which locks out the Manual Tuning Mode. This feature allows the user to quickly determine the frequency parameters of any device being tested.

## 3-22. Operator's Checks

3-23. During final checkout at the factory the Model 8660C Synthesized Signal Generator mainframe is adjusted for proper operation. No adjustments should be required when the instrument is received. The operator's checks listed in Table 3-1 are based on the assumption that properly operating RF Sections and Modulation Sections are in place during the tests. Refer to the manuals for the specific plug-ins for operating parameters.

3-24. The steps listed in Table 3-1 need not be followed in the sequence listed. Their purpose is to aid the operator in familiarizing himself with the instrument, and to provide assurance that all functions of the instrument are operating properly.

## NOTES

1. Numbers shown in the "Result" column of Table 3-1 are those which should be displayed on the CENTER FREQUENCY readout.
2. Any operator's checks specified in the plug-in Manuals should also be performed.

## 3-25. Modulator Units

$3-26$. Since the modulator plug-ins are not affected by the mainframe except for digital control

Table 3-1. Operator's Checks (Local Operation) (1 of 4)

\begin{tabular}{|c|c|c|}
\hline Step \& Operation \& Result <br>
\hline 1
$1-\mathrm{a}$
$1-\mathrm{b}$

$1-\mathrm{c}$ \& | Initial Turn-on, all Models |
| :--- |
| Set the rear panel line select in the power line Module to be compatible with the available line power. |
| Connect the instrument to the power outlet; use ground pin adapter for electrical systems having no ground line. |
| NOTE |
| The instrument should remain connected to the power source in the STBY (standby) mode when not in use. This will maintain constant temperature in the crystal oven and eliminate the need for a long warm-up period. |
| Place the LINE STBY/ON switch in the ON position. | \& Cooling fan starts. CF is 1.000000 MHz . <br>

\hline 2
$2-\mathrm{a}$
2-b

2-c
$2-\mathrm{d}$

$2-\mathrm{e}$ \& | Keyboard Register and Readout Checks all Models |
| :--- |
| Hold in KYBD pushbutton adjacent to CF readout and enter 1.23456789. Note that readout input steps from right to left. |
| With KYBD pushbutton held in : Press MHz key |
| Press kHz key |
| Press Hz key |
| Release KYBD pushbutton |
| Press KYBD pushbutton |
| With KYBD pushbutton held in: Press kHz key |
| Press MHz key |
| Press GHz key |
| Press CLEAR KYBD key | \& | Unit lights ( $\mathrm{GHz}, \mathrm{MHz}, \mathrm{kHz}$, Hz ) are off. 1.234567890 |
| :--- |
| 1.234567 MHz |
| 1.234 kHz |
| 1 Hz |
| 1.000000 MHz |
| 1 Hz |
| 1.000 kHz |
| 1.000000 MHz |
| 1.000000000 GHz |
| Readout all zeroes | <br>

\hline 3
$3-\mathrm{a}$
3 3-b
3-c
3-d

3-e \& \begin{tabular}{l}
Step $\uparrow$ and step $\downarrow$ register and OUT OF RNG annunciator check (86601A). <br>
Enter 109.000000 MHz CF on the KYBD <br>
Enter 111111 Hz STEP $\uparrow$ on the keyboard <br>
Press the KYBD pushbutton <br>
Release the KYBD pushbutton <br>
Press the STEP $\uparrow$ key until the readout shows. <br>
Note that the readout has increased in steps of <br>
Press the STEP $\uparrow$ key one more time. <br>
Place the MANUAL MODE switch in the STEP position and turn the TUNING control counterclockwise.

 \& 

109.000000 MHz <br>
109.111111 MHz <br>
111111 kHz <br>
109.111111 MHz <br>
109.999999 MHz <br>
111111 Hz <br>
110.111110 MHz OUT OF <br>
RNG light flashes once. <br>
Readout decreases in 111111 Hz steps.
\end{tabular} <br>

\hline
\end{tabular}

Table 3-1. Operator's Checks (Local Operation) (2 of 4)

\begin{tabular}{|c|c|c|}
\hline Step \& Operation \& Result <br>
\hline $3-\mathrm{f}$

$3-\mathrm{g}$ \& | Enter 10 kHz CF on the keyboard |
| :--- |
| Enter 1 Hz STEP $\uparrow$ on keyboard |
| Press STEP pushbutton adjacent to CF readout |
| Press STEP $\downarrow$ key twice |
| NOTE: With the Model 86601A RF Section the specified lower frequency limit is 10 kHz . |
| NOTE |
| The Model 86601 A RF Section lower frequency limit is specified at 10 kHz . However, the output frequency is accurate down to |
| 1 Hz . The output power level is typically accurate down to 3 kHz or less. |
| Enter 3 kHz CF on the keyboard |
| Enter 100 Hz STEP $\downarrow$ |
| Repeatedly press the STEP $\downarrow$ key. Note that the frequency readout decreases in 100 Hz steps. The rf frequency level will typically start to drop below 2 kHz . | \& \[

$$
\begin{aligned}
& 10.000 \mathrm{kHz} \\
& 10.001 \mathrm{kHz} \\
& 1 \mathrm{~Hz} \\
& 9.999 \mathrm{kHz}
\end{aligned}
$$
\]

$$
\begin{aligned}
& 3.000 \mathrm{kHz} \\
& 2.900 \mathrm{kHz}
\end{aligned}
$$ <br>

\hline 4 \& MANUAL MODE - MANUAL TUNING Check (86601A) \& <br>
\hline 4-a \& Set the SWEEP MODE switch to OFF and enter 0 MHz CF \& . 000000 MHz <br>

\hline 4-b \& | Set the MANUAL MODE switch to COARSE and rotate the TUNING CONTROL clockwise until the readout indicates : |
| :--- |
| Note that the readout steps in 1 MHz increments. | \& \[

109.000000 \mathrm{MHz}
\] <br>

\hline 4-c \& | Set the MANUAL MODE switch to MED and rotate the TUNING control clockwise until the readout indicates : |
| :--- |
| Note that the readout steps in 1 kHz increments. | \& \[

109.999000 \mathrm{MHz}
\] <br>

\hline 4-d \& | Set the MANUAL MODE switch to FINE and rotate the TUNING control clockwise until the readout indicates: |
| :--- |
| Note that the readout steps in 1 Hz increments. | \& 109.999999 MHz <br>

\hline \& The OUT OF RNG light flashes on when the RF Section upper frequency limit is passed. The system rejects overrange frequencies and the center frequency register retains the last valid entry. \& <br>

\hline 5 \& | Sweep Mode Checks with the 86601A RF Section |
| :--- |
| NOTE |
| Proper operation of the instrument in the sweep mode is best verified with a spectrum analyzer as described in step 5-c. However, operation of the sweep function can be verified by front panel indications as described in steps $5-a$ and 5-b. | \& <br>

\hline
\end{tabular}

Table 3-1. Operator's Checks (Local Operation) (3 of 4)

| Step | Operation | Result |
| :---: | :---: | :---: |
| 5-a <br> 5-b <br>  <br> 5- <br> 5-c | Set CF to 5 kHz and SWP WIDTH to 10 kHz . Place the SWEEP MODE switch in the AUTO position and the RATE switch in the SLO position. <br> Set CF to 10 kHz . Other functions as in step 5 -a. <br> Connect the rf output to the RF INPUT of the spectrum analyzer. Enter 10 MHz CF and 10 MHz SWP WIDTH and SWEEP MODE to AUTO. Position the RATE switch to MED and adjust the spectrum analyzer for a clear display. Enter 5 MHz STEP and step the frequency across the rf range. | SWEEP and OUT OF RNG lights on. RF output level drops every ten seconds. <br> SWEEP LIGHT remains lit. OUT OF RNG light alternates, 25 seconds on, 25 seconds off. <br> Readout increases in 5 MHz steps. Sweep continues to be 5 MHz on each side of the center frequency. |
| 6 $6-a$ | Sweep Mode checks with the higher frequency RF Sections. <br> Set the CF to 5 MHz , set SW WIDTH to 10 MHz . <br> Set the SWEEP MODE switch to AUTO and RATE switch to SLO. | 5.000000 MHz 5.000000 MHz <br> OUT OF RNG light <br> flashes ever 50 seconds. <br> RF OUTPUT Meter <br> also dips. SWEEP light |
| $6-b$ $6-c$ | Set CF to 1 MHz <br> Set CF to 5 MHz on keyboard. <br> Set SWEEP RATE to MED. | 1.000000 MHz Sweep light on, OUT OF RNG light on 25 seconds; off 25 seconds. <br> 5.000000 MHz <br> 5.000000 MHz <br> OUT OF RNG light flashes on at a 1 second rate. |
| 7 <br> 7-a | MANUAL SWEEP Check <br> Enter 50 MHz CF and 10 MHz SWP WIDTH. Place the SWEEP MODE switch in the MAN position. Rotate the MANUAL SWEEP control through its range. | Center frequency is tuneable from 45 to 55 MHz . |

Table 3-1. Operator's Checks (Local Operation) (4 of 4)

| Step | Operation | Results |
| :---: | :---: | :---: |
| 8 $8-\mathrm{a}$ | SINGLE SWEEP Check <br> Enter 50 MHz CF and 20 MHz SWP WIDTH and place the SWEEP MODE switch in the SINGLE position. Press SWP WIDTH pushbutton. Connect the rf output to the RF INPUT of the spectrum analyzer and tune the analyzer to display the 50 MHz signal. Press the SINGLE pushbutton. | 50.000000 MHz 20.000000 MHz Spectrum analyzer displays is swept once from 40 to 60 MHz . |
| 9 $9-\mathrm{a}$ 9-b 9-b 9-c 9-d 9 | Model 86602 <br> STEP $\uparrow$ and STEP $\downarrow$ register and OUT OF RNG annunciator check with the higher frequency RF Sections. <br> Enter 1200.000000 MHz (86602) on the keyboard. <br> Enter 11.111111 MHz STEP $\uparrow$ on the keyboard. <br> Press KYBD pushbutton <br> Release KYBD pushbutton <br> Continue pressing STEP $\uparrow$ key until readout displays: <br> Press the STEP $\uparrow$ key one more time <br> Set the MANUAL MODE switch to the STEP position and turn the TUNING control counterclockwise <br> Enter 1 MHz CF on the keyboard <br> Enter 1 Hz STEP $\uparrow$ on the keyboard <br> Press STEP pushbutton <br> Press STEP $\downarrow$ on the keyboard twice | 1200.000000 MHz <br> 1211.111111 MHz <br> 11.111111 MHz <br> 1211.111111 MHz <br> 1299.999999 MHz <br> 1299.999999 MHz OUT OR RNG light flashes once <br> Readout decreases in 11.111111 MHz steps <br> 1.000000 MHz <br> 1.000001 MHz <br> 1 Hz <br> .999999 MHz OUT OF RNG light stays on. |
|  | NOTE <br> These checks will work with any of the RF Sections. It is only necessary to be aware of the frequency parameters and adjust the control settings accordingly. |  |

voltages, operator's checks for the modulators are not included in Table 3-1. Refer to the individual manuals for the modulator plug-in in use for applicable operator's checks.

## 3-27. RF Units

$3-28$. Many of the tests specified in Table 3-1 do not apply specifically to an RF Section. Those checks which are not referred to a specific RF Section apply equally to the Model 86601,86602 , and the 86603 . When procedures apply to specific RF Sections only, this information is conveyed following the procedure.

## NOTE

Most of the programming tables in this section apply equally to local and remote modes.

## 3-29. REMOTE OPERATION

3-30. There are currently two means of remotely programming the Model 8660 C . They are BCD (Binary Coded Decimal) and HP-IB (HewlettPackard Interface Bus). In the text which follows, programming and other requirements which are common to both means will be discussed first, then BCD requirements, and finally HP-IB requirements.

## 3-31. General Programming Requirements

$3-32$. There are several conventions which must be observed when remotely controlling the Model 8660C. Besides providing data with the least significant digit first, these conventions include:
a. All output levels are referenced to +13 dBm . This reference operation involves subtracting 13 from the desired output level.
b. There are three separate modulation parameters which may be programmed; source, type and \%. Source and type are combined into one number (source is the least significant digit).
c. When in the remote mode, all front panel controls except the LINE STBY/ON and FM CAL controls are inhibited.
d. Digital sweep may not be operated in the remote mode of operation.
e. When changing from the local to the remote mode of operation the temporary storage
register should be cleared before a remote entry is made.
f. The data level inputs to the Model 8660 C are as follows: approximately 0 volts (TTL LOW $)=1$ and approximately 2.8 V (TTL HIGH) $=$ 0 (sometimes referred to as negative or ground true logic).

## 3-33. BCD Remote Operation

$3-34$. The following information pertaining to BCD programming, does not apply to HP-IB programming.

3-35. In BCD remote operation two four-bit parallel codes are applied to the instrument circuits through a rear panel connector (J3). These inputs, if numeric data, are converted to BCD digit serial information and clocked into a temporary storage register. If the inputs are address information they are clocked into a temporary storage register. If the inputs are address information they are used to direct a clock to strobe the data from the temporary storage register into the desired final storage register.

3-36. When all of the significant data entries have been stored in the temporary storage registers, the least significant digit is stored in a position to allow it to be the first digit strobed out, then the next least significant digit, etc, so that the information will be stored in the appropriate register in the same sequence in which it was received.
$3-37$. Operation of the storage registers not located in the Model 8660C mainframe is detailed in the manuals for the plug-in sections. Table 3-3 provides examples of programming the registers which may be programmed when the Model 8660C mainframe is used.

3-38. Refer to Figures 3-2 and 3-3 for timing information and to Table $3-5$ for interconnection information.

## NOTE

> Although it is not necessary to program frequency first, then modulation (if any), then attenuation, this sequence minimizes the time required for entering data.

3-39. Data Inputs. Data inputs (logic $1=0$ ) must be referenced to the command pulse as shown in


Figure 3-2. Model 8660C Data Input Timing


Figure 3-3. Model 8660C Error Output Timing

Figure 3-2. The data inputs may be terminated after the command pulse trailing edge.
$3-40$. The command pulse causes the input data to be stored in the temporary storage register or, if the data input is an address, to be stored in one of the final.storage registers. These pulses are logic 1 (0V) pulses of 100 nanoseconds minimum width, maximum frequency of 500 kHz . Pulses for low transfer frequencies may be wider if consistent with the duty cycle. The leading edge must have a fall time of 100 nanoseconds or less. Transfer occurs on the leading edge of the pulse. Note that data must be held until the command pulse terminates. The flag signal is also initiated by the falling (leading) edge of the command pulse.

3-41. Flag Signal. The flag signal indicates receipt and execution of the command pulse from the remote programming device. The flag signal will be logic $1(0 \mathrm{~V})$. Duration of the signal will depend on the function programmed.

3-42. Error Signal. Indicates frequency out of range or crystal oven temperature is not stabilized. The error signal will be at a logic $1(0 \mathrm{~V})$ for the period of the function error (see Figure 3-3).

3-43. Reset. Controls the DCU circuits in the same manner as the DCU power detect circuit does when the instrument is first turned on. It also initializes circuitry and resets the data registers. Requires a logic 1 ( 0 V ) level which may be as short as 5 microseconds.

## NOTE

When switching from remote to local operation clear the keyboard before making an entry.

## 3-44. HP-IB Remote Operation

3-45. HP-IB (Hewlett-Packard Interface Bus) is a general purpose interface system. Although the

Table 3-2. Storage Register Addresses

| Name of Register | Address $0=\text { High, } 1=\text { Low }$ | Location | Function |
| :---: | :---: | :---: | :---: |
| Center Frequency | 0000 (0) | Mainframe | To set Center Frequency |
| Step $\uparrow$ | 0001 (1) |  | To step center frequency up in any increment |
| Step $\downarrow$ | 0010 (2) | Mainframe DCU | To step center frequency down in any increment |
| Attenuator | 0011 (3) | RF Section plug-in | Controls level of RF OUTPUT |
| AM-FM Function | 0100 (4) | Modulation Section plug-in | Selects Modulation Function |
| AM-FM\% | 0101 (5) | Modulation Section plug-in | *Selects AM \% of Modulation or FM Deviation |
| FM CAL 86635 or 86632 only | 0110 (6) | Modulation Section plug-in | Phase locks 20 MHz FM oscillator to the reference loop 20 MHz |
| *The 86632B and the 86635A require jnputs of one half of the desired deviation in remote mode. |  |  |  |

Table 3-3. Model 8660C Programming Examples (1 of 3)

| EXAMPLE 1. Set 100.000000 MHz Center Frequency (CF) |  |  |
| :---: | :---: | :---: |
| $0=\text { High } \begin{array}{ll}  & \text { Input } \\ & 1=\text { Low } \end{array}$ | Temporary Register | CF Register |
| Data: $\quad D_{1} 0001$ (1) $\mathrm{D}_{2} 0000$ (0) <br> Temporary Command <br> Address: $\mathrm{D}_{1} 1111$ (15) $\mathrm{D}_{2} 0000$ (0) <br> Transfer Command | $\begin{aligned} & 0000000000 \\ & 0100000000 \\ & 0100000000 \\ & 0000000000 \end{aligned}$ | Last Input <br> Last Input <br> Last Input <br> 0100000000 |
| EXAMPLE 2. Set 107.654321 MHz Center Frequency (CF) |  |  |
| $\begin{array}{lll} \hline & \text { Input } & \\ 0=\text { High } & 1=\text { Low } \end{array}$ | Temporary Register | CF Register |
| Data: $\quad D_{1} 0001(1) D_{2} 0010(2)$ <br> Temporary Command <br> Data: $\quad \mathrm{D}_{1} 0011$ (3) $\mathrm{D}_{2} 0100$ (4) <br> Temporary Command <br> Data: $\quad D_{1} 0101$ (5) $\mathrm{D}_{2} 0110$ (6) <br> Temporary Command <br> Data: $\quad D_{1} 0111$ (7) $\mathrm{D}_{2} 0000(0)$ <br> Temporary Command <br> Address: $\mathrm{D}_{1} 1111$ (15) $\mathrm{D}_{2} 0000$ (0) <br> Transfer Command | 0000000000 2100000000 2100000000 4321000000 4321000000 6543210000 6543210000 0765432100 0107654321 0000000000 | Last Input <br> Last Input <br> Last Input <br> Last Input <br> Last Input <br> Last Input <br> Last Input <br> Last Input <br> Last Input <br> 0107654321 |
| EXAMPLE 3. Set 120 dB Attenuation (RF SECTION) Below +13 dBm (1 volt) |  |  |
| $\begin{array}{lll} \hline & \text { Input } & \\ 0=\text { High } & 1-\text { Low } \end{array}$ | Temporary Register | Atten Register |
| Data: $\quad \mathrm{D}_{1} 0010$ (2) $\mathrm{D}_{2} 0001$ (1) <br> Temporary Command <br> Address: $\mathrm{D}_{1} 1111$ (15) $\mathrm{D}_{2} 0011$ (3) <br> Transfer Command | $\begin{aligned} & 0000000000 \\ & 1200000000 \\ & 1200000000 \\ & 0000000000 \end{aligned}$ | Last Input Last Input Last Input 120 |
| NOTE <br> The attenuator is a three-digit register; only the three most significant digits are retained. |  |  |

Table 3-3. Model 8660C Programming Examples (2 of 3)

| EXAMPLE 4. Set 7 dB Attenuation (RF SECTION) Below +13 dBm (1 volt) |  |  |
| :---: | :---: | :---: |
| $0=\text { High } \quad \text { Input } \quad 1=\text { Low }$ | Temporary Register | Atten Register |
| Data: $\quad D_{1} 0000(0) D_{2} 0111$ (7) Temporary Command <br> Data: $\quad D_{1} 0000(0) D_{2} 0000(0)$ <br> Temporary Command <br> Address: $\mathrm{D}_{1} 1111$ (15) $\mathrm{D}_{2} 0011$ (3) <br> Transfer Command | $\begin{aligned} & 0000000000 \\ & 7000000000 \\ & 7000000000 \\ & 0070000000 \\ & 0070000000 \\ & 0000000000 \end{aligned}$ | Last Input <br> Last Input <br> Last Input <br> Last Input <br> Last Input <br> 007 |
| See note for Example 3 |  |  |
| EXAMPLE 5. Shut off Modulation (MODULATION SECTION) |  |  |
| $0=\text { High }{ }^{\text {Input }} 1=\text { Low }$ | Temporary Register | Function Register |
| Address: $\mathrm{D}_{1} 1111$ (15) $\mathrm{D}_{2} 0100$ (4) <br> Transfer Command | 0000000000 0000000000 | Last Input 00 |
| NOTE: All digits are zero - no modulation |  |  |
| EXAMPLE 6. Set 3\% AM Modulation, Internal 1 kHz (MODULATION SECTION) |  |  |
| $0=\text { High } \quad \text { Input } \quad \text { 1=Low }$ | Temporary Register | AM-FM \% Register |
| Data: $\quad D_{1} 0011$ (3) $D_{2} 0000(0)$ <br> Temporary Command <br> Address: $\mathrm{D}_{1} 1111$ (15) $\mathrm{D}_{2} 0101$ (5) <br> Transfer Command <br> Data $\quad D_{1} 0001(1) D_{2} 1000(8)$ <br> Temporary Command <br> Address: $\mathrm{D}_{1} 1111$ (15) $\mathrm{D}_{2} 0100$ (4) <br> Transfer Command | 0000000000 0300000000 0300000000 0000000000 0000000000 8100000000 8100000000 0000000000 | Last Input <br> Last Input <br> Last Input <br> 03 into \% Storage <br> 81 into AM-FM <br> Function Register <br> Sets AM and 1 kHz |
| NOTE: See Table 3-4. for AM-FM Function Register Codes |  |  |

Table 3-3. Model 8660C Programming Examples (3 of 3)
EXAIMPLE 7. Set 10 MHz STEP $\uparrow$

| 0=High Input $\quad 1=$ Low | Temporary Register | INCR Register |
| :--- | :--- | :--- |
| Data: $\mathrm{D}_{1} 0000(0) \quad \mathrm{D}_{2} 0001(1)$ | 0000000000 | Last Input |
| Temporary Command | 1000000000 | Last Input |
| Data: $\mathrm{D}_{1} 0000(0) \quad \mathrm{D}_{2} 0000(0)$ | 1000000000 | Last Input |
| Temporary Command | 0010000000 | Last Input |
| Address: $\quad \mathrm{D}_{1} 1111(15) \quad \mathrm{D}_{2} 0001(1)$ | 0010000000 | Last Input |
| Transfer Command | 0000000000 | 0010000000 |

Table 3-4. AM - FM Function Register Coding

| 0=High | 1=Low | $0=\mathrm{High} \quad \text { DIGIT } 1\left(D_{1}\right)$ | 1=Low |
| :---: | :---: | :---: | :---: |
| 0 M | 1100 (12) | EXT. AC (UNLEVELED | $\begin{aligned} & 1001(9) \\ & 86633 \text { only } \end{aligned}$ |
| FM X . 1 | 0100 (4) | EXT. DC | 0100 (4) |
| FM X 1 | 0010 (2) | INT. 400 Hz | 0010 (2) |
| FM X 10 | 0001 (1) | INT. 1 kHz | 0001 (1) |
| OFF | 0000 (0) |  |  |

Table 3-5. Programming Connections to J3

| J3 Pin No. | To A3XA5 Pin No. | Signal | Other |
| :---: | :---: | :--- | :--- |
| 1 |  |  | To J3 pin 18 |
| 3 | 2 | Error |  |
| 5 | 5 | LCL-RMT |  |
| 9 | 11 | Command |  |
| 13 | 15 | Digit 1-8 |  |
| 14 | 16 | Digit 1-4 |  |
| 15 | 17 | Digit 1-2 |  |
| 16 | 18 | Digit 1-1 |  |
| 17 | A | Flag (Busy) |  |
| 24 | J | Reset |  |
| 28 | S | Digit 2-8 |  |
| 29 | T | Digit 2-4 |  |
| 30 | U | Digit 2-2 |  |
| 31 | Vigit 2-1 | Ground |  |
|  |  |  |  |
| J3 pins not listed are also wired to A3XA5. See the rear interface board schematic |  |  |  |
| diagram for wiring information. |  |  |  |

HP-IB uses many of the operational parameters (coding, handshake, etc.), the terms HP-IB and ASCII should not be used interchangeably because they are not completely compatible.
$3-46$. The HP-IB interface systems use seventeen lines to effect the transfer of data between the instruments connected to the bus. Eight of these lines are used for the actual transfer of data, one line is ground and the remaining eight lines are used for control.

3-47. Table 3-6 illustrates the HP-IB bus interface line designations. The ground line, being selfexplanatory, is not shown.
$3-48$. The structure and operation of the bus is analogous to an old-fashioned party line, and many of the conventions which apply to a party line apply to the HP-IB interface as well. For instance, at any given time only one person may talk on the party line, while many people may listen, and most will not be using the party line at all.

3-49. Similarly, on the HP-IB interface, only one instrument may talk (send data) at any given time, although many instruments may listen (receive data), and most instruments will not interact with the bus at all.

3-50. In order to determine which instruments are to "talk", which are to "listen", and which are to remain inactive, some sort of a controller is required. This controller, which might be a calculator, assigns functions to the various instruments by sending data over the eight lines to all instruments. Any instrument becomes a listener when its listen address is placed on the bus and remains a listener until the "unlisten" command is transmitted. Talkers, on the other hand, stop functioning as talkers whenever another talk address is put on the data lines. This prevents more than one device from talking at any given time.

3-51. In order for the instrument to distinguish between data and addresses, both of which are sent over the eight data lines, an "address mode/data mode" selector called the Multiple Response Enable (MRE) line is driven by the controller. When this line is low, all instruments listen to the eight data lines and interpret the information being transmitted by the controller as addresses. When the MRE line is high, information on the eight data lines is interpreted as data and the instruments talk, listen or remain inactive as determined during the time they were addressed when MRE was low.

3-52. Three-Wire Handshake. Information, whether addresses, measurement results, or other data is transferred on the data lines under control of a technique called the three-wire handshake. The handshake involves the use of three control lines, and operates as follows:
a. A listener indicates that it is ready to accept data by letting the Ready for Data (RFD) line go high. Listeners are connected to the RFD line in a logical AND configuration so the RFD line does not go high until all active listeners are ready for data.
b. After RFD has gone high, the talker indicates that it has placed a data byte on the eight data lines by setting the Data Valid (DAV) line low.
c. After DAV has gone low, each listener pulls RFD low, accepts the data, and then lets the data accepted (DAC) line go high. Again, all listeners are logically ANDed and DAC does not go high until all listeners have accepted the data.
d. After the DAC line has gone high, the talker can let DAV go high again and take the data off the lines. When DAV goes high, the listeners set DAC back to low and the sequence is ready to repeat with step 1 of Figure 3-4.

3-53. As can be seen from the description, data transfer is asynchronous, proceeding only as fast as the slowest active (addressed to talk or listen) device on the line.

## NOTE

Figure 3-4 illustrates a flow chart of the three-wire handshake operation.

3-54. The four remaining control lines operate as follows:
a. The Remote Enable (REN) line allows the controller to put all instrument on the bus in the remote mode. When this line is low, all instruments will go into remote as soon as they are addressed, and remain in remote until the line goes high again.
b. The End Output (EOP) line, when pulled low by the system controller, will halt all activity on the bus and cause all instruments to unaddress themselves.

Table 3-6. HP-IB Interface Lines

c. The Service Request (SRQ) line allows instruments to get the attention of the controller. The Model 8660C does not use this line, so its function will not be described here.
d. The End OR Identify (EOI) line is used to identify which instrument pulled the SRQ line low. The Model 8660C does not use this line.
$3-55$. When a standard Model 8660 C is modified to accept the HP-IB interface the instructions contained in the modification kit must be followed to install the two new circuit boards.

3-56. In addition to following the modification instructions, special care should be taken to observe jumper positions on the HP-IB boards.

3-57. Before installing the HP-IB circuit boards check the address jumpers, and change if required. It should be noted that if more than one Model

8660 C is used in a system, it is not likely that operational parameters will be the same for each, so different addresses will probably be required for each instrument.

3-58. When used in the Model 8660C, jumper J2 must not be connected.

3-59. Jumper J1 is installed at the operator's choice. With it in place the internally generated BUSY signal is used to delay the RFD response. Without it, the operator must make allowances in programming for the necessary settling time of the Model 8660C.

3-60. The information contained in this section of this manual applies only to Model 8660C Option 005 HP-IB instruments. Refer to Table 3-7 for HP-IB codes. Information contained in this section for other types of remote control does not apply to Option 005 instruments.

3-61. Local control operation of Option 005 instruments is the same as that described for the Model 8660 C in other parts of this section.

3 -62. Basically, the Model 8660C Option 005 instruments are the same as the standard Model 8660C instruments except that the capability of remote operation using the HP-IB interface is added and BCD interface is deleted. Basic information about HP-IB is included in the General Information Section of this manual.
$3-63$. Option 005 allows remote programming via the HP-IB interface of all 8660C front panel controls except LINE, (POWER), SWEEP MODE, and MANUAL MODE. All front panel controls except LINE AND FM CAL are locked out when the Model 8660C is in remote.

3-64. The Model 8660C HP-IB interface will recognize an internally preset "listen" address and accept bit-parallel, word serial HP-IB information. When addressed to listen, the Model 8660 C shifts incoming data into a temporary storage register. This data must be presented to the interface least significant digit first to satisfy the internal logic
requirements of the Model 8660 C . When a programming code is detected in the input data, the contents of the temporary storage register are shifted into the register selected by the internal address character. The temporary register is then cleared to make way for more data.

3-65. There are three separate modulation parameters which may be programmed; source, type and \%. Source and type are combined into one number (source is the least significant digit) and this number is followed by the address " $\$$ ". To turn off the modulation section, code $\emptyset$ for modulation type. When programming AM, \% modulation refers to percentage of full scale. Thus the FM X 10 range is 1000 kHz full scale, and $20 \%$ would mean 200 kHz deviation. With this setup the deviation of the 86632B or the 86635A would be 400 kHz .

3-66. One last convention is that after the Model 8660 C is placed in remote, the first output of the HP-IB interface should be a false address which serves to clear the temporary storage register. This can be accomplished by first addressing the Model 8660C to listen, then placing " $p$ " on the HP-IB line.


Figure 3-4. Handshake Flow Chart

Table 3-7. HP-IB Code Allocations


# SECTION IV PERFORMANCE TESTS 

## 4-1. INTRODUCTION

$4-2$. The procedures in this section test the instruments electrical performance using the specifications of Table 1-1 as the performance standards. A simpler operations test is included in Section III under Operator's Checks.

## 4-3. EQUIPMENT REOUIRED

4-4. Equipment required for the performance tests is listed in the Recommended Test Equipment table in Section I. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

## 4-5. TEST RECORD

$4-6$. Results of the performance tests may be tabulated on the Test Record at the end of the
procedures. The Test Record lists all of the tested specifications and their acceptable limits. Test results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

## WARNING

Performance test 4-7 requires removal of the top instrument cover. This exposes the input line voltage and the dc voltage outputs of the power supply. Care should be exercised to avoid physical contact with these voltage points. In addition, the power source should be disconnected during cover removal. All required tests must be performed only by qualified service personnel.

## PERFORMANCE TESTS

## 4-7. INTERINAL CRYSTAL OSCILLATOR AGING RATE

## SPECIFICATION:

Reference Oscillator Internal: 10 MHz quartz oscillator. Aging rate less than $\pm 3$ parts in $10^{8}$ per 24 hours after 72 hour warmup. ( $\pm 3$ parts in $10^{9}$ per 24 hours after 30 day warmup, Option 001.)

## DESCRIPTION:

This test verifies the reference oscillator aging rate by comparing it to the National Bureau of Standards signal from WWVB.


Figure 4-1. Crystal Oscillator Aging Rate Test Setup
EQUIPMENT:
VLF Comparator HP 117A

## 4-7. INTERNAL CRYSTAL OSCILLATOR AGING RATE (Cont'd)

## PROCEDURE:

1. Remove ac power and the Model 8660 C top cover after the instrument has been connected to the ac line for 72 hours.
2. Connect a cable from the 100 kHz output of the A4A1 reference divider assembly to the VLF Comparator 100 kHz input. Reconnect ac power and switch power to ON.
3. Refer to the operating Section of the VLF Comparator Operating and Service Manual for Comparator operating instructions.
4. Aging rate is checked by noting the average offset between the two signals at two times several hours apart and dividing the offset difference by the hours between observations. The hourly offset is then converted to aging rate per day.

Example:
First reading +3 parts in $10^{10}$ at 10:00 AM
Second reading +6 parts in $10^{11}$ at 4:00 PM
The difference is 2.4 parts in $10^{10}$ in 6 hours
$\frac{2.4}{6} \times 10^{10}=0.4$ parts in $10^{10}$ per hour
Frequency change is 0.96 parts in $10^{9}$ per day.

## 4-8. REFERENCE TEST

## SPECIFICATION:

About 1 Vrms, 10 MHz into 170 ohms.
DESCRIPTION:
This test verifies proper operation of the reference amplifier and relay switching circuits.

## 4-8. REFERENCE TEST (Cont'd)



Figure 4-2. Internal Reference Test Setup
TEST EQUIPMENT:
RMS Voltmeter (with high impedance probe) . . . . . . . . HP 411A

## PROCEDURE:

1. Connect the RMS Voltmeter to the REFERENCE OUTPUT (rear panel) jack and set the SELECTOR switch (rear panel) to the INT position.
2. The RMS Voltmeter should display a signal about 1 volt in amplitude.

Table 4-1. Performance Test Record

Hewlett-Packard Model 8660C
Synthesized Signal Generator
Serial No. $\qquad$

Tests performed by

Date $\qquad$
Crystal Oscillator Aging Rate OPT 001

Output Reference Level
Actual $\qquad$ Actual $\qquad$

## SECTION V ADJUSTMENTS

## 5-1. INTRODUCTION

$5-2$. This section describes adjustments and checks required to return the Model 8660C to peak operating capability when repairs have been made. Included in this section are test setups and procedures.

5-3. Except for the power supply adjustment procedures, which should be performed before repairs are made to any part of the instrument, the adjustment procedures are arranged in the same sequence as the service sheets to which they refer.

## 5-4. EQUIPMENT REOUIRED

$5-5$. Each adjustment procedure in this section contains a list of test equipment and accessories required to perform the procedure. Each test setup identifies test equipment and accessories by callouts.

5-6. Minimum specifications for test equipment used in the adjustment procedures are detailed in Table 1-2. Because the Model 8660C is an extremely accurate instrument, minimum specifications in Table 1-2 are particularly important in perfoming these adjustment procedures.

## 5-7. ADJUSTMENT AIDS

$5-8$. The HP 11672A Service Kit is an accessory item available from Hewlett-Packard for use in maintaining the Model 8660C Synthesized Signal Generator. Table $1-2$ contains a detailed description of the Service Kit. Any item in the kit may be ordered separately.

## 5-9. FACTORY SELECTED COMPONENTS

$5-10$. Some component values are selected at the time of final checkout at the factory. Usually these values are not extremely critical; they are selected to provide optimum compatibility with associated components.
$5-11$. Factory selected components and suggested range of values are listed in Table 5-1.

5-12. The recommended procedure for replacing a factory selected component is as follows:
a. Try the original value, then perform the test specified in Section V of this manual for the circuit being repaired.
b. If the specified test capnot be satisfactorily performed, try the typical value shown in the parts list and repeat the test.
c. If the test results are still not satisfactory, substitute various values within the tolerances specified in Table 5-1 until the desired result is achieved.

## 5-13. RELATED ADJUSTMENTS

$5-14$. Most of the adjustments within any given phase lock loop are interrelated. This is especially true in digital-to-analog converters. Adjustments should be made in the order in which they appear for any given loop.

5-15. Generally, it will not be necessary to adjust any of the phase lock loops except the one in which the component failure occurred. An exception to this will be when adjustment to any phase lock loop has been attempted while the reference section is not functioning properly.

## 5-16. ADJUSTMENT LOCATIONS

5-17. Adjustment locations are identified pictorially on Section VIII foldout service sheets referred to in the individual procedures and in Figures listed in the individual procedures.

## 5-18. CHECKS AND ADJUSTMENTS

5-19. Data taken while following the adjustment procedures should be recorded in spaces provided. This information may then be used as reference in later tests.

Table 5-1. Factory Selected Components

| Designation | Location | Purpose | Range of Values |
| :---: | :---: | :---: | :---: |
| A4A2C11 | Reference Loop | To control 3 dB bandwidth of 40 to 70 kHz | 38 to 72 pF |
| A4A4L12 | Reference Loop | To control output level of 100 MHz | 0.34 to $1.0 \mu \mathrm{H}$ |
| A4A6R18 | HF Loop | To center range of associated potentiometer | 100 to 200 ohms |
| A4A6R26 | HF Loop |  | 60 to 250 ohms |
| A4A6R33 | HF Loop |  | 100 to 300 ohms |
| A4A6R38 | HF Loop |  | 100 to 500 ohms |
| A4A6R43 | HF Loop |  | 200 to 700 ohms |
| A4A6R47 | HF Loop |  | 200 to 900 ohms |
| A4A6R51 | HF Loop |  | 500 to 1500 ohms |
| A4A6R55 | HF Loop |  | 1.2 K to 3.1 K |
| A4A6R59 | HF Loop |  | 2K to 7 K |
| A4A4Q7 | Reference Loop | To optimize performance of 500 MHz tuned amplifier |  |
| A4A4Q8 | Reference Loop | To optimize performance of 100 MHz tuned amplifier. |  |
| A8R18 | N3 Oscillator | To aid in balancing Summing loop for Varactor tuning. | 19.6 K to 25 K |
| A8R25 | N3 Oscillator |  | 4 K to 6K |
| A19R55 | SL1 Oscillator | To prevent oscillation in Q1 | 1 K to 2 K |

## NOTES

a. In the following tests it is assumed that at the start of the test the output frequency is set to 0 .
b. An RF Section output plug-in section must be in place during the tests.
c. A Modulator Section or an Auxiliary Section must be in place in the modulator compartment.
d. All tests in which a counter is used should be made with the Model 8660C and the counter referenced to the same source. If the Hewlett-Packard Model 5245M Frequency Counter is used, the Model 8660C internal reference may be used as the source.

## 5-20. SAFETY CONSIDERATIONS

5-21. Although this instrument has been designed in accordance with international safety standards, this manual contains information and warnings
which must be followed to ensure safe operation and to retain the instrument in a safe condition (see Section II). Service and adjustments should be performed only by qualified service personnel.

## WARNING

Any interruption of the protective (grounding) conductor inside or outside the instrument or disconnection of the protective earth terminal is likely to make the apparatus dangerous. Intentional interruption is prohibited.
$5-22$. Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazards involved. The opening of covers or removal of parts may expose live parts, and also accessible terminals may be live.
$5-23$. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

5-24. Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.
$5-25$. Whenever it is likely that the protection has been impaired, the instrument must be made
inoperative and be secured against any unintended operation.

## NOTE

When repairs or adjustments to the instrument are required, such work should not be performed, even by a skilled technician, unless another person is in the same general area. This is not to be interpreted to mean that two persons are required to perform the necessary work, but only that another person should be available, should the need for assistance arise.

## ADJUSTMENTS

## 5-26. POWER SUPPLY

REFERENCE:
Service Sheet 41

## DESCRIPTION:

The power supplies in the Model 8660 C provide regulated outputs of $+20 \mathrm{~V},+5.25 \mathrm{~V},-10 \mathrm{~V}$ and -40 V . Unregulated supplies provide $+30 \mathrm{~V},+19 \mathrm{~V},+4 \mathrm{~V}$ and -19 V . These checks verify proper operation of the power supply.

## ADJUSTMENTS

## 5-26. POWER SUPPLY (Cont'd)



Figure 5-1. Power Supply Test Setup

## TEST EQUIPMENT:

> Digital Voltmeter . . . . . . . . . . . . . . . . . . . . . . . . HP 3480/3482 AC Microvoltmeter . . . . . . . . . . . . . . . . . . . . . . . HP 3410A Variable Voltage Transformer . . . . . . . . . . . . General Radio W5MT3A

## PROCEDURE:

1. Remove the top and bottom covers of the Model 8660C and connect the instrument to the ac line through the variable voltage transformer.
2. Use the digital voltmeter and the ac microvoltmeter to check voltages, tolerances and ripple at A20 test points specified in Table 5-2. Adjust the variable voltage transformer to check tolerance of the power supplies at $\pm 10 \%$ line voltage variations.
3. Use the digital voltmeter and the ac microvoltmeter to check for voltages, tolerances and 120 Hz ripple at A5 test points specified in Table 5-3. Adjust the dc levels shown in Table $5 \cdot 3$ with controls specified in Table 5-3, then adjust the variable voltage transformer to check tolerance of the power supplies at $\pm 10 \%$ of the normal line voltage.

## ADJUSTMENTS

5-26. POWER SUPPLY (Cont'd)

Table 5-2. Unregulated Power Supplies

| Test Location | Voltage <br> at normal line | Tolerance <br> high to low line <br> (from normal line) | 120 Hz Ripple <br> (at normal line) |
| :--- | :--- | :--- | :--- |
| + side of A20C7 | Typical +3.67 V | Specified $\pm 0.6 \mathrm{~V}$ | Typical .31 Vrms |
|  | Actual | Actual | Actual - |
| + side of A20C4 | Typical +19.8V | Specified $\pm 2.4 \mathrm{~V}$ | Typical 1.1 Vrms |
|  | Actual | Actual | Actual - |
| - side of A20C5 | Typical +19.8 V | Specified $\pm 2.4 \mathrm{~V}$ | Typical 1.15 Vrms |
|  | Actual | Actual | Actual |
| + side of A20C1 | Typical +33 V | Specified $\pm 4 \mathrm{~V}$ | Typical .46 Vrms |
|  | Actual | Actual | Actual |

Table 5-3. Regulated Power Supplies

| Test Point | Adjust <br> Control | Voltage <br> at Normal Line <br> Specified | Tolerance <br> High to Low Line <br> Specified | RMS Ripple <br> 120 Hz <br> (Normal Line) |
| :---: | :--- | :--- | :--- | :--- |
| A5TP4 | A5R24 | +5.25 V | $\pm 20 \mathrm{mV}$ | $125 \mu \mathrm{~V}$ |
|  | +5.25 ADJ | Actual | Actual | Actual - |
| A5TP2 | A5R26 | -10.0 V | $\pm 5 \mathrm{mV}$ | $50 \mu \mathrm{~V}$ |
| A5TP3 | -10 ADJ | Actual | Actual | Actual - |
| A5R21 | +20.0 V | $\pm 10 \mathrm{mV}$ | $50 \mu \mathrm{~V}$ |  |
|  | +20 ADJ | Actual | Actual | Actual |
|  | A5R28 | -40.0 V | $\pm 20 \mathrm{mV}$ | $50 \mu \mathrm{~V}$ |
|  | -40 ADJ | Actual | Actual | Actual - |

## ADJUSTMENTS

## 5-27. REFERENCE SECTION

## REFERENCE:

Service Sheets 2 and 3 and Figure 8-119.

## DESCRIPTION:

The reference section contains a voltage controlled master oscillator from which all RF signals generated in the Model 8660C mainframe are derived. The master oscillator is phase locked to an internal temperature controlled crystal oscillator or to an external standard. The reference section provides outputs of 500 MHz , $100 \mathrm{MHz}, 20 \mathrm{MHz}, 10 \mathrm{MHz}, 2 \mathrm{MHz}, 400 \mathrm{kHz}$ and 100 kHz . These checks verify proper operation of the circuits within the reference section.


Figure 5-2. Reference Accuracy Adjustment Test Setup

## EQUIPMENT:

| VLF Comparator | . . . . . . . . . . . . . . . . . . . . . . . . HP 117A |
| :--- | :--- |
| Oscilloscope (with $10: 1$ divider probes) | . . . . . . HP 180A/1801A/1820A |
| Spectrum Analyzer | . . . . . . . . . . . . . . . . . . HP 140/8554L/8552 |
| Frequency Counter | . . . . . . . . . . . . . . . . . . . HP 5245M/5253B |

## PROCEDURE:

1. Internal Reference Accuracy Adjustment (see Figure 5-2). (Allow adequate warmup time.)
a. Remove the Model 8660 C top cover and connect the 100 kHz output from the A4A1 assembly to the 100 kHz input of the VLF Comparator.
b. Remove the left side panel from the Model 8660C.
c. Remove the cap screw to provide access to the adjustment point of the A21 Crystal oscillator assembly.
d. Refer to Section III of the VLF Comparator Operating and Service Manual for operating instructions and align the Model 8660C A21 assembly.

## ADJUSTMENTS

## 5-27. REFERENCE SECTION (Cont'd)

## NOTE

If the VLF Comparator is not available, and an accurate signal source is, the reference oscillator may be adjusted by using an oscilloscope for comparison of the two signals.
2. Alternate Reference Accuracy Adjustment (see Figure 5-3)
a. Use the signal source to trigger the oscilloscope at the SYNC INPUT and connect the reference output from the Model 8660C rear panel reference output to the oscilloscope vertical input.
b. Observe the 10 MHz sine wave on the oscilloscope and adjust the A21 oscillator until the oscilloscope display stops drifting.
c. Set the oscilloscope to sweep at $0.1 \mu \mathrm{Sec} /$ Division and the sweep magnifier to X 10 . If drift is observed readjust the A21 oscillator.

## NOTE

When the oscilloscope display drift is less than 1 division in 10 seconds the Model 8660 reference oscillator is set within 1 part in $10^{9}$ of the signal source.


Figure 5-3. Alternate Reference Accuracy Adjustment Test Setup
3. 100 MHz Output Adjustment.
a. Connect the frequency counter to the 100 MHz output on the A4A4 assembly (see Figure 5-4).
b. If the internal reference is being used, place the rear panel INT/EXT switch in the EXT position to open to 100 MHz phase lock loop. (If an external reference is being used, disconnect the source.)
c. Allow at least 15 minutes warmup time for the oscillator to stabilize and adjust A4A4C2 for a counter readout of $100.000 \mathrm{MHz} \pm 20 \mathrm{kHz}$. Disconnect the frequency counter.

## ADJUSTMENTS

## 5-27. REFERENCE SECTION (Cont'd)



Figure 5-4. 100 MHz Adjustment Test Setup
d. Connect the Spectrum Analyzer RF INPUT to the 100 MHz output of the A4A4 assembly and tune the Spectrum Analyzer CENTER FREQUENCY to 100 MHz . The 100 MHz signal should be $>+10 \mathrm{dBm}$ (see Figure 5-5).


Figure 5-5. RF Level Checks Test Setup
e. Disconnect the Spectrum Analyzer and enable the 100 MHz phase lock loop by returning the INT/EXT switch to INT or by reconnecting the external standard.
4. 500 MHz Output Adjustment
a. Connect the Spectrum Analyzer RF INPUT to the 500 MHz output connector on the A4A4 assembly and tune the analyzer to 500 MHz . Set the analyzer scan width to 50 MHz per division and other analyzer controls for a clear display (see Figure 5-5).
b. Adjust A4A4C17, A4A4C23 and A4A4C31 for a peak amplitude of the 500 MHz signal. The 500 MHz signal amplitude should be $>+3 \mathrm{dBm}$. The 400 MHz signal observed at the 500 MHz output is typically $<-10 \mathrm{dBm}$. The 600 MHz signal observed at the 500 MHz output is typically $<-20 \mathrm{dBm}$. Disconnect the analyzer.
$\qquad$

## 5-27. REFERENCE SECTION (Cont'd)

5. 20 MHz Output Check
a. Connect the Spectrum Analyzer RF INPUT to the 20 MHz output on the A4A4 assembly and tune the analyzer to 20 MHz . The 20 MHz signal should be $>-6 \mathrm{dBm}$ and $<-2 \mathrm{dBm}$. Disconnect the analyzer.

20 MHz dBm
6. Reference Section Outputs Not Previously Checked
a. Check the outputs listed in Table 5-3 for the levels shown (see Figure 5-6).


Figure 5-6. Oscilloscope Level Checks Test Setup

Table 5-4. Reference Section Output Levels

| Test Point | Frequency | Specified Level | Actual Level |
| :---: | :---: | :--- | :--- |
| A4J6 | 10 MHz | $>1 \mathrm{Vp}-\mathrm{p}$ | - |
| A4J1 | 2 MHz | $>2.2 \mathrm{Vp}-\mathrm{p}$ | - |
| A4J3 | 400 kHz | $>2.2 \mathrm{Vp}-\mathrm{p}<5.0 \mathrm{~V}$ | - |
| A4J2 | 100 kHz | $>2.2 \mathrm{Vp-p}<5.0 \mathrm{~V}$ | - |
| A4J4 | 100 kHz | $>2.2 \mathrm{Vp}-\mathrm{p}<5.0 \mathrm{~V}$ | - |

## ADJUSTMENTS

## 5-28. HIGH FREQUENCY SECTION

## REFERENCE:

Service Sheets 4, 5, and 6, and Figure 8-117.

## DESCRIPTION:

The High Frequency Section contains a voltage controlled oscillator which provides eleven discrete output frequencies from 350 to 450 MHz in 10 MHz steps. The output of the voltage controlled oscillator is phase locked to a 10 MHz reference derived from the master oscillator in the reference section. The output from the HF section is used in the RF Section plug-in or in the internal frequency extension plug-in module. These checks verify proper operation of the High Frequency Section circuits.


Figure 5-7. Phase Detector Response Adjustment Test Setup

## TEST EQUIPMENT:

$$
\begin{array}{lcl}
\text { Frequency Counter } & \text {. . . . . . . . . . . . . . . . . . . . . HP 5245M/5253B } \\
\text { Digital Voltmeter } & \text {. . . . . . . . . . . . . . . . . . . . . HP 3480/3482 } \\
\text { Pulse Generator . . . . . . . . . . . . . . . . . . . . . . HP 222A } \\
\text { Spectrum Analyzer } & \text { HP . . . . . . . . . . . . . HP 140/8554L/8552/8553 } \\
\text { Oscilloscope (with 10:1 divider probes) . . . . . . . HP 180A/1801A/1821A } \\
\text { Signal Generator/Sweeper . . . . . . . . . . . . . . . . . . . . . . HP 8601A }
\end{array}
$$

## ADJUSTMENTS

## 5-28. HIGH FREQUENCY SECTION (Cont'd)

## PROCEDURE:

1. Phase Detector Response Adjustments (see Figure 5-7)
a. Disconnect the coaxial cable from VCO INPUT A4J11. Connect the PULSE OUTPUT of the Pulse Generator to A4J11. Set the Pulse Generator for 100 kHz pulse rate, $0.035 \mu$ Sec pulse width, 0.5 volt amplitude and + polarity.
b. Connect the Spectrum Analyzer RF INPUT to the "phase error" signal at A4TP1 outside A4A6. Set the analyzer controls as follows:

$$
\begin{aligned}
& \text { CENTER FREQUENCY } \\
& \text { SCAN WIDTH PER DIVISION . . . . . . . . . . . . . . . . . . . . . . } 5 \mathrm{MHz} \\
& \text { SCAN TIME PER DIVISION } \\
& \text { Gain and Attenuation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . } \mathrm{m} \text { required }
\end{aligned}
$$

c. Adjust EFFiciency control A4A7R18 for a flat response to approximately 5 MHz with very slight peaking ( $1 \mathrm{~dB} \pm 1 \mathrm{~dB}$ ). See the waveform in Figure 5-7 for typical response.
d. Disconnect the Pulse Generator and the Spectrum Analyzer.
2. Balance Adjustment
a. Connect the digital voltmeter to "phase error" TP.
b. Adjust the BALance control (A4A7R22) for a reading of 0 volts $\pm .05$ volt. Disconnect the digital voltmeter.
3. Voltage Controlled Oscillator Adjustment (see Figure 5-8)
a. Remove the A4A6 cover. With the output cable of the A4A5 assembly disconnected from the VCO OUTPUT (A4J10), connect the Digital Voltmeter to the A4A6 FREQuency control output (white lead).
b. Adjust the A4A6 " 0 " control (A4A6R13) for a Digital Voltmeter reading of -34 volts (voltage should be adjustable from about -33 to -35 volts).
c. Connect the Frequency Counter to the A4A5 voltage controlled oscillator output, A4J12. Replace the A4A6 assembly cover.

## ADJUSTMENTS

## 5-28. HIGH FREQUENCY SECTION (Cont'd)



Figure 5-8. Voltage Controlled Oscillator Adjustments Test Setup
d. The Counter should display $450 \mathrm{MHz} \pm 1 \mathrm{MHz}$. If the correct reading is obtained proceed to step f . If the frequency reading is not correct, proceed to step e.
e. Remove the A4A5 cover and adjust A5A5C3 for a $450 \mathrm{MHz} \pm 1 \mathrm{MHz}$ reading.
f. Disconnect the frequency counter and reconnect the voltage controlled oscillator output to the phase detector.
g. Connect the digital voltmeter to the "phase error" TP. Connect the frequency counter to A4A5J2 ( $350-450 \mathrm{MHz}$ OUTPUT).
h. Set the center frequencies as shown in Table 5-4 and set the digital to analog controls on the A4A6 assembly for $0 \pm 0.1$ volt for each frequency listed. Note that the counter displays the output frequency listed for each center frequency setting.

## NOTE

When the 86602 or 86603 is installed in the mainframe the 350 MHz output of the High Frequency Section is not used. When this situation exists, the adjustment procedure for A4A6R15 " 10 " is not calid and the following procedure should be substituted:

1. Ground the collector for A4A6Q1.
2. Adjust A4A6R15 " 10 " for 350 MHz .
3. Remove the ground from the collector of A4A6Q1.

## 5-28. HIGH FREQUENCY SECTION (Cont'd)

Table 5-5. Pretune Adjustments

| Center Frequency | Adjust Control | Counter Readout |
| :---: | :--- | :--- |
| 0 MHz | A4A6R13 "0" | 450.000000 MHz |
| 10 MHz | A4A6R60 "1" | 440.000000 MHz |
| 20 MHz | A4A6R56 "'2" | 430.000000 MHz |
| 30 MHz | A4A6R52 "3" | 420.000000 MHz |
| 40 MHz | A4A6R48'"4" | 410.000000 MHz |
| 50 MHz | A4A6R44 " $5 "$ | 400.000000 MHz |
| 60 MHz | A4A6R40 "6" | 390.000000 MHz |
| 70 MHz | A4A6R35 "7" | 380.000000 MHz |
| 80 MHz | A4A6R28 "8" | 370.000000 MHz |
| 90 MHz | A4A6R22 "9", | 360.000000 MHz |
| 100 MHz | A4A6R15 "10" | 350.000000 MHz |
| NOTE |  |  |

The adjustments shown in Table 5-5 should be made with the counter time base connected to the synthesizer REFERENCE OUTPUT.
i. If any of the controls listed in Table 5-4 cannot be adjusted to 0 volts, adjust A4A6R20 "profile" to obtain additional range. Repeat all pretune adjustments until satisfactory results are obtained. Disconnect the digital voltmeter and the frequency counter.
4. Loop Gain Adjustment (see Figure 5-9).
a. With the center frequency set to 0 MHz connect the Spectrum Analyzer RF INPUT to A4A5J2 (350-450 MHz OUTPUT) and set the analyzer controls as follows:

```CENTER FREQUENCY450 MHzBANDWIDTH30 kHz
```

SCAN WIDTH PER DIVISION ..... 5 MHz
SCAN TIME PER DIVISION ..... 5 ms
b. Disconnect the reference input to A 4 A 7 J 2 and reconnect it together with the RF output of the Signal Generator/Sweeper.
c. Set the Signal Generator/Sweeper to 11.5 MHz CW at -35 dBm and symmetrical sweep width to 3 MHz . The analyzer display should be approximately as shown in the typical waveform shown in Figure 5-9. Adjust the A4A6 GAIN control (A4A6R2) for the response shown.
d. Disconnect the Analyzer and the Generator/Sweeper. Reconnect the reference signal to A4A7J2.

## ADJUSTMENTS

## 5-28. HIGH FREQUENCY SECTION (Cont'd)



Figure 5-9. Loop Gain Adjustment Test Setup
5. 10 MHz Trap Adjustment (see Figure $5-10$ ).

## NOTE

This adjustment is necessary only if the A4A6 10 MHz trap has been repaired.
a. Disconnect the coaxial cable from A4J10 ( $350 / 450 \mathrm{MHz}$ to $\emptyset$ detector).
b. Disconnect the 10 MHz reference signal from A4J13 and reconnect it using a TEE connector. Connect the 10 MHz reference signal from the other TEE port to the $\emptyset$ input of the A4A6 assembly (white wire from the A4A7 assembly).
c. Connect the Spectrum Analyzer RF INPUT to the A4A6 FREQuency control output (white-black-violet wire). Set the analyzer controls as follows:

| CENTER FREQUENCY | 10 MHz |
| :---: | :---: |
| BANDWIDTH | 30 kHz |
| SCAN WIDTH PER DIVISION | 200 kHz |
| VIDEO FILTER | OFF |
| INPUT ATTENUATION | 0 dB |
| SCAN TIME PER DIVISION | 1 Msec |
| REF LEVEL | 30 dB |

d. Adjust A4A6C5 trap for minimum 10 MHz amplitude.

## ADJUSTMENTS

## 5-28. HIGH FREQUENCY SECTION (Cont'd)

e. Reconnect $\emptyset_{\text {input to }}$ A4A6.
f. Replace all High Frequency Section Covers.


Figure 5-10. 10 MHz Trap Adjustment Test Setup
6. Output Frequency and Amplitude Check (see Figure 5-11).
a. Set the 8660 C CF to 6 MHz .
b. Connect the Spectrum Analyzer RF INPUT to A4A5J2. Set the analyzer controls as required to view the 450 MHz signal. The output should be +13 dBm to +15 dBm .
$\qquad$ dBm
c. Switch digits 9 and 8 from 00 through 10 . The frequency should decrease in 10 MHz steps (amplitude at +13 dBm minimum).

| 440 MHz __ ${ }^{\text {dBm }}$ | 430 MHz | 420 MHz ___ dBm |
| :---: | :---: | :---: |
| 410 MHz | 400 MHz | 390 MHz ___ dBm |
| 380 MHz ___ dBm | 370 MHz _ ${ }^{\text {dBm }}$ | 360 MHz |
| 350 MHz |  |  |

## ADJUSTMENTS

## 5-28. HIGH FREQUENCY SECTION (Cont'd)



Figure 5-11. Output Amplitude Check Test Setup

## 5-29. N1 PHASE LOCK LOOP

## REFERENCE:

Service Sheets 7 and 8 and Figure 8-120.

## DESCRIPTION:

The N1 phase lock loop produces digitally controlled RF signals from 19.8 to 29.7 MHz in 100 kHz steps. The output frequency is selected by digits 6 and 7 . These checks verify proper operation of the loop circuits.


Figure 5-12. N1 Loop Test Setup

## ADJUSTMENTS

## 5-29. N1 PHASE LOCK LOOP (Cont'd)

## TEST EQUIPMENT:

$$
\begin{array}{ll}
\text { Digital Voltmeter . . . . . . . . . . . . . . . . . . . . . . . . HP 3480/3482 } \\
\text { Frequency Counter } & \text {. . . . . . . . . . . . . . . . . . . . . HP 5245M/5253B }
\end{array}
$$

PROCEDURE: (see Figure 5-12)

1. Enter 0 MHz center frequency and ground motherboard test point A2TP16 with one of the jumper plugs provided. Connect the digital voltmeter to A2TP18.
2. Adjust A17R31 or A17R28 for a voltmeter reading of -30 volts and disconnect the digital voltmeter.
3. Connect the frequency counter to the N 1 oscillator output on the A 2 mother board and adjust A17C17 for a counter reading as close as possible to 29.7 MHz (must be within $\pm 200 \mathrm{kHz}$ ).
4. Enter 500 kHz center frequency and adjust A17R28 or A17R31 for a counter reading of 29.2 MHz .
5. Enter 9.5 MHz center frequency and record the counter readout.

MHz $\qquad$
6. Determine the frequency difference between the readout for step 5 and 20.2 MHz and record.

MHz $\qquad$
7. Enter 500 kHz center frequency.
a. If the reading in step 5 was higher than 20.2 MHz adjust A17R28 for a counter readout of 29.2 MHz plus the difference frequency recorded in step 6 .
b. If the reading in step 5 was lower than 20.2 MHz adjust A17R28 for a counter readout of 29.2 MHz minus the difference frequency recorded in step 6.
8. Adjust A17R31 for an output frequency readout of 29.2 MHz .
9. Repeat steps 5 through 8 until the counter readout is $29.2 \mathrm{MHz} \pm 20 \mathrm{MHz}$ for a 500 kHz center frequency and $20.2 \mathrm{MHz} \pm 20 \mathrm{kHz}$ for a 9.5 MHz center frequency.
10. Remove the ground jumper from A2TP16.
11. Disconnect the 400 kHz reference signal by disconnecting the cable from A4A1J3 and connect the digital voltmeter to A2TP17. Adjust A16R38 for a digital voltmeter readout of $0 \mathrm{~V} \pm 10 \mathrm{mV}$. Reconnect the 400 kHz reference signal.
12. Enter center frequencies shown in Table 5-5. The counter readings should be as shown in the table.

## ADJUSTMENTS

## 5-29. N1 PHASE LOCK LOOP (Cont'd)

Table 5-6. N1 Loop Output Frequency Checks

| Center Frequency | Counter Readout |
| :---: | :---: |
| 0 | 29.700000 MHz |
| 1.1 MHz | 28.600000 MHz |
| 2.2 MHz | 27.500000 MHz |
| 3.3 MHz | 26.400000 MHz |
| 4.4 MHz | 25.300000 MHz |
| 5.5 MHz | 24.200000 MHz |
| 6.6 MHz | 23.100000 MHz |
| 7.7 MHz | 22.000000 MHz |
| 8.8 MHz | 20.900000 MHz |
| 9.9 MHz | 19.800000 MHz |
| NOTE |  |

The adjustments shown in Table 5-6 should be made with the counter time base connected to the synthesizer REFERENCE OUTPUT.

## 5-30. N2 PHASE LOCK LOOP

## NOTE

Option 004 instruments use a different N2 programmable divider designated as $N 2 a$. In the following procedure the frequencies shown in parenthesis apply to N2a.

REFERENCE:
Service Sheets 9 and 10.
DESCRIPTION:
The N2 phase lock loop produces controlled RF signals from 19.80 to 29.79 MHz in 10 kHz increments. The output frequency selected by the $100 \mathrm{~Hz}, 1 \mathrm{kHz}$ and 10 kHz steps. These checks verify proper operation of the loop circuits.

## ADJUSTMENTS

## 5-30. N2 PHASE LOCK LOOP (Cont'd)



Figure 5-13. N2 Loop Test Setup

## TEST EQUIPMENT:

$$
\begin{array}{ll}
\text { Digital Voltmeter . . . . . . . . . . . . . . . . . . . . . . . . . HP 3480/3482 } \\
\text { Frequency Counter } & \text {. . . . . . . . . . . . . . . . . . . . . HP 5245M/5253B }
\end{array}
$$

PROCEDURE: (see Figure 5-13)

1. Set the center frequency to 0 MHz and ground A2TP12 on the mother board with one of the jumper plugs provided.
2. Connect the digital voltmeter to A2TP9 and adjust A13R37 or A13R39 to -30 volts. Disconnect the digital voltmeter.
3. Connect the frequency counter to the N2 oscillator output at XA13-1-4. Adjust A13C19 for a counter reading as close as possible to 29.79 MHz ( N 2 a 30.00 MHz ) must be within $\pm 200 \mathrm{kHz}$.
4. Set the center frequency to 5.5 kHz . Adjust A13R37 or A13R39 for an output frequency reading of 29.250 MHz . (N2a 29.450 MHz .)
5. Set the center freuqency to 95.5 kHz and record the counter readout.
$\qquad$
6. Determine the frequency difference between step 5 and 20.25 MHz ( N 2 a 20.450 MHz ) and record:

MHz $\qquad$
7. Set the center frequency to 5.5 kHz .
a. If the reading in step 5 was more than 20.25 MHz ( N 2 a 20.45 MHz ) adjust A13R39 to 29.25 MHz ( N 2 a 29.45 MHz ) plus the difference frequency recorded in step 6.

## ADJUSTMENTS

## 5-30. N2 PHASE LOCK LOOP (Cont'd)

b. If the reading in step 5 was less than 20.25 MHz ( N 2 a 20.45 MHz ) adjust A13R39 to 29.25 MHz ( N 2 a 29.45 MHz ) minus the difference frequency recorded in step 6.
8. Adjust A13R 37 for an output frequency of 29.25 MHz ( N 2 a 29.45 MHz ).
9. Repeat steps 4 through 7 until the counter readout is $29.25 \mathrm{MHz}(\mathrm{N} 2 \mathrm{a} 29.45 \mathrm{MHz}) \pm 20 \mathrm{kHz}$ for a center frequency of 20.25 MHz ( N 2 a 20.45 MHz ) $\pm 20 \mathrm{kHz}$ for a center frequency of 95.5 kHz .
10. Remove the ground from A2TP12.
11. Set center frequency as shown in Table 5-6. The counter readings should be as shown in the table.

Table 5-7. N2 Oscillator Output Frequency Checks

| Center Frequency | Counter Readout N2 | Counter Readout N2a |
| :--- | :---: | :---: |
| 0 | 29.790000 MHz | 30.000000 MHz |
| 11.1 kHz | 28.680000 MHz | 28.890000 MHz |
| 22.2 kHz | 27.570000 MHz | 27.780000 MHz |
| 33.3 kHz | 26.460000 MHz | 26.670000 MHz |
| 44.4 kHz | 25.350000 MHz | 25.560000 MHz |
| 55.5 kHz | 24.240000 MHz | 24.450000 MHz |
| 66.6 kHz | 23.130000 MHz | 23.340000 MHz |
| 77.7 kHz | 22.020000 MHz | 22.230000 MHz |
| 88.8 kHz | 20.910000 MHz | 21.120000 MHz |
| 99.9 kHz | 19.800000 MHz | 20.010000 MHz |

## 5-31. N3 PHASE LOCK LOOP

NOTE
Option 004 instruments do not include the N3 loop.

## ADJUSTMENTS

## 5-31. N3 PHASE LOCK LOOP (Cont'd)

## REFERENCE:

Service Sheets 11 and 12 and Figure 8-120.

## DESCRIPTION:

The N3 phase lock loop produces digitally controlled RF signals from 2.001 to 2.100 MHz in 1 kHz increments. The output frequency is selected by 1 Hz and 10 Hz steps. These checks verify proper operation of the loop circuits.


Figure 5-14. N3 Loop Test Setup

## TEST EQUIPMENT:

> Digital Voltmeter . . . . . . . . . . . . . . . . . . . . . . . . HP 3480/3482 Frequency Counter

PROCEDURE: (see Figure 5-14)

1. Set center frequency to 0 MHz and ground A2TP4 on the mother board with one of the jumper plugs provided.
2. Connect the counter to the N3 oscillator output at XA8-1-4 on the mother board. Adjust A8R26 or A8R24 for a counter readout of 2.100 MHz .
3. Set the center frequency to 5 Hz . Adjust A8R24 for a counter reading of 2.095 MHz . (must be within $\pm 20 \mathrm{kHz}$.)
4. Set the center frequency to 95 Hz , and record the frequency displayed on the counter.

MHz $\qquad$
5. Determine the frequency difference between that recorded in step 4 and 2.005 MHz and record.
$\qquad$

## ADJUSTMENTS

## 5-31. N3 PHASE LOCK LOOP (Cont'd)

6. Set the center frequency to 5 Hz .
a. If the reading in step 4 was less than 2.005 MHz adjust A8R24 to 2.095 MHz minus the frequency difference recorded in step 5.
b. If the reading in step 4 was more than 2.005 MHz adjust A8R24 to 2.095 MHz plus the frequency difference recorded in step 5.
7. Adjust A8R26 for an output frequency of 2.095 MHz .
8. Repeat steps 3 through 6 until the counter readout is $2.095 \mathrm{MHz} \pm 20 \mathrm{kHz}$ for a 5 Hz center frequency, and $2.005 \mathrm{MHz} \pm 20 \mathrm{kHz}$ for a 95 Hz center frequency.
9. Remove the ground from A2TP4.
10. Set center frequencies as shown in Table 5-8. The counter readings should be as shown in the table.

Table 5-8. N3 Oscillator Output Frequency Checks

| Center Frequency | Counter Readout |
| :---: | :---: |
| 0 Hz | 2.1000000 MHz |
| 11 Hz | 2.0890000 MHz |
| 22 Hz | 2.0780000 MHz |
| 33 Hz | 2.0670000 MHz |
| 44 Hz | 2.0560000 MHz |
| 55 Hz | 2.0450000 MHz |
| 66 Hz | 2.0340000 MHz |
| 77 Hz | 2.0230000 MHz |
| 88 Hz | 2.0120000 MHz |
| 99 Hz | 2.0010000 MHz |

## 5-32. SUMMING LOOP 2 (SL2)

## NOTE

Option 004 instruments do not include SL2.

## ADJUSTMENTS

## 5-32. SUMMING LOOP 2 (SL2) (Cont'd)

REFERENCE:
Service Sheets 13 and 14 and Figure 8-120.

## DESCRIPTION:

SL2 is a phase lock loop that provides a digitally controlled RF output to Summing Loop 1. This output, which is from 20.0001 to 30.000 MHz in 100 Hz steps, is controlled by $100 \mathrm{~Hz}, 1 \mathrm{kHz}$ and 10 kHz steps, it is also indirectly controlled by 1 Hz and 10 Hz steps. These checks verify proper operation of the loop circuits.


Figure 5-15. SL1 and SL2 Test Setup

## TEST EQUIPMENT:

> Digital Voltmeter . . . . . . . . . . . . . . . . . . . . . . . . HP 3480/3482 Frequency Counter Oscilloscope (with $10: 1$ divider probes) . . . . . . . . . . HP HP $180 \mathrm{H} / 1801 \mathrm{~A} / 1820 \mathrm{~A} / \mathrm{H}^{2}$

## PROCEDURE: (see Figure 5-15)

1. Set center frequency to 55.5 kHz .
a. With the digital voltmeter connected to A2TP8, adjust A11R15 or A11R19 to $0.00 \pm$ 10 millivolts.
b. With the oscilloscope connected to A1TP7 adjust A12R37 for $50 / 50$ symmetry.
c. Disconnect the digital voltmeter and the oscilloscope.
2. Connect the digital voltmeter to varactor test point A2TP5, ground mother board test point A2TP8 with a clip lead, and set center frequency to 0 MHz .

## ADJUSTMENTS

## 5-32. SUMMING LOOP 2 (SL2) (Cont'd)

a. Adjust A11R15 or A11R19 to read -30 volts on the digital voltmeter and then disconnect the digital voltmeter.
b. Connect the counter to test point A2TP6 and adjust A11C17 for a counter readout as close to 30 MHz as possible (must be within $\pm 300 \mathrm{kHz}$ ).
3. Set center frequency to 4.5 kHz . Adjust A11R15 or A11R19 for a counter reading of 29.550 MHz .
4. Set center frequency to 94.5 kHz . Record the output at A2TP6 as read on the counter.

MHz $\qquad$
5. Determine the difference frequency between that recorded in step 4 and 20.5500 MHz and record.
$\qquad$
a. Set center frequency to 4.5 kHz .
b. If the frequency readout in step 4 was higher than 20.5500 MHz adjust A11R15 to 29.550 MHz plus the difference frequency determined in step 5 .
c. If the frequency readout in step 4 was lower than 20.5500 MHz adjust A11R15 to 29.550 MHz minus the difference frequency determined in step 5.
6. Reset the frequency to 29.550 MHz with A11R19.
7. Repeat steps $3,4,5$ and 6 until the counter indicates $20.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ for a center frequency of 94.5 kHz and $29.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ for a center frequency of 4.5 kHz .
8. Set center frequency as shown in Table 5-9. Adjust the controls listed for counter readouts shown.

Table 5-9. SL2 Oscillator Output Frequency Adjustments

| Center Frequency | Adjust | Counter Readout |
| :---: | :---: | :---: |
| 84.5 kHz | A11R39 " 8 " | $21.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 74.5 kHz | A11R54 " 7 " | $22.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 64.5 kHz | A11R60 " 6 " | $23.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 54.5 kHz | A11R67 " $5 "$ | $24.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 44.5 kHz | A11R73 " $4 "$ | $25.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 34.5 kHz | A11R77 " 3 " | $26.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 24.5 kHz | A11R83 " 2 " | $27.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 14.5 kHz | A11R90 " $1 "$ " | $28.55 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |

## ADJUSTMENTS

## 5-32. SUMMING LOOP 2 (SL2) (Cont'd)

9. Disconnect the counter, remove the ground from A2TP8 and connect the oscilloscope to A2TP7.
10. Set center frequencies as shown in Table 5-9 and adjust the associated potentiometers for 50/50 symmetry as seen on the oscilloscope (all must be within 40/60).

## 5-33. SUMMING LOOP 1 (SL1)

## REFERENCE:

Service Sheets 15, 16 and 17 and Figure 8-130.

## DESCRIPTION:

SL1 is a phase lock loop that provides a digitally controlled RF output to the RF Section plug-in. This output, which is from 20.000001 to 30.000000 MHz in 1 Hz steps is pretuned by $1 \mathrm{MHz}, 100 \mathrm{kHz}$ and 10 kHz steps and is also indirectly controlled by 1 kHz to 1 Hz steps. These checks verify proper operation of the loop circuits.

## NOTE

In Option 004 instruments the SL1 output is 100 Hz steps.


Figure 5-16. SL1 Test Setup

## TEST EQUIPMENT:

## ADJUSTMENTS

## 5-33. SUMMING LOOP 1 (SL1) (Cont'd)

PROCEDURE: (see Figure 5-16)

1. Set center frequency to 5.55 MHz .
a. With the digital voltmeter connected to A2TP14, adjust A19R3 or A19R9 to 0.00 volt $\pm$ 10 millivolts.
b. With the oscilloscope connected to A2TP13, adjust A15R14 for 50/50 symmetry.
c. Disconnect the digital voltmeter and the oscilloscope.
2. Connect the digital voltmeter to varactor test point A2TP21, ground mother board test point A2TP14 with the jumper provided, and set center frequency to 0 .
a. Adjust A19R3 or A19R9 to -30 volts and disconnect the digital voltmeter.
b. Connect the counter to SL1 OSC at XA19-1-2 and adjust A19C18 for a counter readout as close as possible to 30 MHz (must be within $\pm 300 \mathrm{kHz}$ ).
3. Set center frequency to 450 kHz . Adjust A19R3 or A19R9 for a counter reading of 29.550 MHz .
4. Set center frequency to 9.45 MHz . Record frequency of output at SL1 OSC at XA19-1-2.

MHz $\qquad$
5. Determine the difference frequency between that recorded in step 4 and 20.550 MHz and record:

$$
\mathrm{MHz} .
$$

$\qquad$
a. Set center frequency to 450 kHz .
b. If the frequency readout in step 4 was higher than 20.550 MHz adjust A19R3 to 29.550 MHz plus the difference frequency recorded in step 5 .
c. If the frequency readout in step 4 was lower than 20.550 MHz adjust A19R3 to 29.550 MHz minus the difference recorded in step 5.
6. Reset the frequency to 29.550 MHz with A19R9.
7. Repeat steps 3 through 6 until the counter indicates $20.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ for a center frequency of 9.45 MHz and $29.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ for a center frequency setting of 450 kHz .
8. Set center frequency as shown in Table 5-9. Adjust controls listed for counter readouts shown.
9. Disconnect the counter, remove the ground from A2TP14 and connect the oscilloscope to A2TP13.
10. Set center frequencies as shown in Table $5-9$ and adjust the controls listed for $50 / 50$ symmetry as seen on the oscilloscope. Disconnect the oscilloscope. (All settings must be within 40/60 symmetry.)

## ADJUSTMENTS

5-33. SUMMING LOOP 1 (SL.1) (Cont'd)

Table 5-10. SL1 Oscillator Output Frequency Adjustments

| Center Frequency | Adjust | Counter Readout |
| :---: | :---: | :---: |
| 8.45 MHz | A18R35 " 8 " | $21.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 7.45 MHz | A18R40 " 7 " | $22.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 6.45 MHz | A18R44 " 6 " | $23.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 5.45 MHz | A18R51 " 5 " | $24.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 4.45 MHz | A18R55 " $4 "$ | $25.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 3.45 MHz | A18R62 " $3 "$ | $26.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 2.45 MHz | A18R67 " 2 " | $27.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |
| 1.45 MHz | A18R74 " 1 " | $28.550 \mathrm{MHz} \pm 20 \mathrm{kHz}$ |

## 5-34. DCU SWEEP OUTPUT

## REFERENCE:

Service Sheet

## DESCRIPTION:

The Model 8660C sweep output may be used to drive the horizontal sweep of an oscilloscope while the RF output is used to determine the characteristics of a device being tested. This procedure provides information required to properly adjust the sweep ramp.

TEST EQUIPMENT:
Digital Voltmeter . . . . . . . . . . . . . . . . . . . . . . . HP 3480B/3482

1. Remove the top and bottom covers from the 8660 B . Remove the four DCU retaining screws (one at each corner inside).
2. With the 8660 C inverted, gently slide the DCU out of the mainframe to the extent of connecting cables and connect the DVM to the 0 to +8 V output.
3. Enter 1.000500 MHz center frequency and 1 kHz sweep width.
4. Set to manual sweep.
5. Using the MANUAL SWEEP control set frequencies shown in Table 5-11 and make the indicated adjustments. Adjustment locations are shown in Figure 5-17. All adjustments must be $\pm 1$ millivolt.

## ADJUSTMENTS

## 5-34. DCU SWEEP OUTPUT (Cont'd)

NOTE
Refer to Figure 8-50 for adjustment locations.

Table 5-11. Adjustments

| Step | Frequency | Adjust |
| :---: | :---: | :--- |
| 1 | 1.000799 | Note DVM output reading typical 6.392V <br> R29 for an output 8 mV greater than above <br> reading is typically 6.4 V |
| 2 | 1.000800 | R11 for an output of 7.992V <br> 3 |
| 4 | 1.000999 | R28 for an output of 0.000 V |
|  | 1.00000 | Repeat steps 1 through 4 |
| 5 | 1.001000 | R30 for an output of 8.000 V |

Table 5-12. Frequency Versus Exact Output Levels

| Frequency | Output Level |
| :---: | :---: |
| 1.000000 MHz | 0.000 V |
| 1.000799 MHz | 6.392 V |
| 1.000800 MHz | 6.400 V |
| 1.000999 MHz | 7.992 V |
| 1.001000 MHz | 8.000 V |
| Nominal step size $-8 \mathrm{mV} / \mathrm{Hz}$ |  |

## 5-35. REMOTE PROGRAMMING

## SPECIFICATIONS:

Specifications applying to operational tests in the LOCAL mode also apply to operational tests performed by remote programming (HP-IB or BCD interface).

## DESCRIPTION:

All front panel frequency, output level, and modulation functions are programmable and can be tested using an HP 3260A Marked Card Programmer.

The standard remote cable for the 3260A is used with the HP-IB programming (OPT 005). The 3260A OPT 001 cable is used for standard BCD programming.

The Marked Card Programmer does not check the HP-IB Handshake Cycle.

## TEST EQUIPMENT:

| Frequency Counter | . | . | . | . | . | . | . | . | HP 5340A |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Spectrum Analyzer | . | . | . | . | . | . | . | . | HP 140T/8555A/8552A |  |
| Marked Card Programmer | . | . | . | . | . | . | . | . | HP 3260A OPT 001 |  |
| Marked Card Programmer | . | . | . | . | . | . | . | . | . | HP 3260A |

## PROCEDURE:

Center Frequency Test

1. Connect the Synthesizer 10 MHz Reference output to the Frequency Counter external reference input.
2. Program the RF Section for 0 dB attenuation and connect the RF output of the Synthesizer to the Frequency Counter input.
3. Program the mainframe for a center frequency within the RF Section frequency limits. The Frequency Counter should display a frequency reading of $\pm 1$ digit of the progranmed frequency.

## Attenuation Test

4. Disconnect the Frequency Counter and connect the Spectrum Analyzer in its place.
5. Program the mainframe for a center frequency of 100 MHz .
6. Program the RF Section for 0 dB attenuation. The RF Section should be at maximum power output.

## AM Test

7. Program mainframe for a center frequency of 50 MHz and RF Section for 10 dB of attenuation.
8. Program AM, 1 kHz Source, and $50 \%$ Modulation. Amplitude of sidebands should be $-12 \pm 0.5 \mathrm{~dB}$ with respect to carrier.
9. Program AM, Source, and $25 \%$ Modulation. Depth of sidebands should be $-18.1 \pm 0.5 \mathrm{~dB}$ with respect to carrier.

## ADJUSTMENTS

## 5-35. REMOTE PROGRAMMING (cont'd)

## FM Test

10. Program the mainframe for a center frequency of 100 MHz and RF Section for 0 dBm output.
11. Program in 1 kHz , FM Source, and 200 kHz peak deviation.
12. Set Spectrum Analyzer Controls for:


Display rising and falling edges should be 400 kHz pk-pk wide at top ( 200 kHz pk ).


Figure 5-17. Typical Remote Programming Test Setup

# SECTION VI REPLACEABLE PARTS 

## 6-1. INTRODUCTION

6-2. This section contains information for ordering parts. Table 6-2 lists abbreviations used in the parts list and throughout the manual. Table 6-3 lists all replaceable parts in reference designator order. Table 6-4 contains the names and addresses that correspond to the manufacturer's code numbers.

## 6-3. EXCHANGE ASSEMBLIES

6-4. Table 6-1 lists assemblies within the instrument that may be replaced on an exchange basis, thus affording a considerable cost saving. Exchange, factory-repaired and tested assemblies are available only on a trade-in basis; therefore, the defective assemblies must be returned for credit. For this reason, assemblies required for spare parts stock must be ordered by the new assembly part number.

## 6-5. ABBREVIATIONS

6-6. Table 6-2 lists abbreviations used in the parts list, schematics and throughout the manual. In some cases, two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lower case and upper case letters.

## 6-7. REPLACEABLE PARTS LIST

6-8. Table $6-3$ is the list of replaceable parts and is organized as follows:
a. Electrical assemblies and their components in alpha-numerical order by reference designation.
b. Chassis-mounted parts in alpha-numerical order by reference designation.
c. Miscellaneous parts.

6-9. The information given for each part consists of the following:
a. The Hewlett-Packard part number.
b. The total quantity (Qty) in the instrument.
c. The description of the part.
d. A typical manufacturer of the part in a five-digit code.
e. The manufacturer's number for the part.
$6-10$. The total quantity for each part is given only once - at the first appearance of the part number in the list.

## NOTE

Total quantities for optional assemblies are totaled by assembly and not integrated into the standard list.

## 6-11. ORDERING INFORMATION

6-12. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-13. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

## 6-14. SPARE PARTS KIT

6-15. Stocking spare parts for an instrument is often done to insure quick return to service after a malfunction occurs. Hewlett-Packard has a "Spare Parts Kit" available for this purpose. The kit consists of selected replaceable assemblies and components for this instrument. The contents of the kit and the "Recommended Spares" list are
based on failure reports and repair data, and parts support for one year. A complimentary "Recommended Spares" list for this instrument may be obtained on request and the "Spare Parts Kit" may be ordered through your nearest Hewlett-Packard office.

## 6-16. ILLUSTRATED PARTS BREAKDOWNS

6-17. Figure $6-1$ provides a breakdown of Cabinet Parts. The parts are not identified by part
numbers or descriptions. These parts are identified by MP (miscellaneous part) numbers which are further identified in Table 6-3 of this section.

6-18. Figure $6-2$ provides a breakdown of DCU front panel parts. The parts are identified by MP numbers or assembly numbers which are further identified in Table 6-3 of this section.

Table 6-1. Part Numbers for Assembly Exchange Orders

|  | Assembly | New Part No. | Exchange No. |
| :--- | :--- | :---: | :---: |
| A1A1 | Sw. Control | $08660-60200$ | $08660-60271$ |
| A1A2 | Key Control | $08660-60176$ | $08660-60177$ |
| A1A3 | Readout Control | $08660-60191$ | $08660-60265$ |
| A1A4 | Rom Input | $08660-60197$ | $08660-60266$ |
| A1A6 | Register Assy | $08660-60198$ | $08660-60267$ |
| A1A12 | Numeric R/O | $08660-60190$ | $08660-60264$ |
| A1A17 | Man. Mode Turner | $08660-60123$ | $08660-60251$ |

Table 6-2. Reference Designations and Abbreviations (1 of 2)

| REFERENCE DESIGNATIONS |  |  |  |
| :---: | :---: | :---: | :---: |
| AT . . . . . . . . . . . astenuator; isomblator; | .... miscellaneous electrical part fuse | . electrical connector (movable portion); plug | U ...... integrated circuit; |
| B . . . . . . . . fan motor | FL . . . . . . . . . filter | Q . . . . . transistor: SCR: | VR .... voltage regulator; |
| ${ }^{\text {BT }}$. $\ldots \ldots \ldots \ldots$ battery | ${ }_{\mathrm{HY}} \mathrm{H}$. $\ldots \ldots \ldots$ hardware | triode thyristor | breakdown diode |
| $\underset{\mathbf{C P}}{\mathbf{C}} \ldots \ldots \ldots \ldots \ldots$. ${ }_{\text {capacitor }}^{\text {coupler }}$ |  |  | cable; transmission path; wire |
| CR ...... diode; diode | (stationary portion); | switch | socket |
| DC ... $\begin{gathered}\text { thyristor: } \\ \text { directional } \\ \text { varactor } \\ \text { coupler }\end{gathered}$ | ${ }_{\text {jack }}$ | $\begin{aligned} & \text { T. . . . . . . . terminal boarmer } \\ & \text { TB } \end{aligned}$ | crystal unit (piezo- |
| DL .......... delay line | K............ relay | тС ...... thermocouple | tuned cavity ; tuned |
| DS ....... annunciator; | L . . . . . . . . coili inductor | TP ......... test point | circuit |
| signaling device <br> (audible or visual) | $\begin{aligned} & \text { M. . . . . . . . . . . . . . meter } \\ & \text { MP } \end{aligned}$ |  |  |
| lamp; LED | mechanical part |  |  |
| ABBREVIATIONS |  |  |  |
| A ............ ampere | COEF ....... coefficient | EDP . . . . electronic data | Int ........... internal |
| ac .... alternating current | сом......... common | processing | kg ............ killoeram |
| ACCESS ..... ${ }^{\text {accessory }}$ | COMP $\ldots . .$. composition | ${ }_{\text {ELECT }} \ldots \ldots$ electrolytic |  |
| ADJ $\ldots \ldots \ldots$ adjustment | COMPL . . . . . . complete | ENCAP .... encapsulated |  |
| A/D $\ldots .$. analog-to-digital | CONN . . . . . . connector | ${ }_{\text {EXT }} \ldots \ldots \ldots$ external | $\mathrm{kV}^{\mathrm{kV}} \ldots . . . . . . .$. . killovolt |
| ${ }_{\text {AFC }} \mathrm{AF} \ldots .$. audio frequency | ${ }_{\text {CPT }}^{\text {CP }} \ldots \ldots$ cathode-ray pabe | $\underset{\mathrm{FET}}{\mathrm{F}} \ldots \ldots \ldots \ldots$. ${ }_{\text {dieldeffect }}^{\text {farad }}$ |  |
| AFC. $\underset{\text { frequency }}{\text { antomatic }}$ control | ${ }_{\text {CTL }} \ldots \ldots$ cathode-ray tube | FET . . ${ }_{\text {cransistor }}$ field-effect | LC . . . capacitance inuctance- |
| AGC . . . . . automatic gain | cw $\ldots . . \begin{gathered}\text { transistor } \text { logic } \\ \text { continuous wave }\end{gathered}$ |  |  |
|  | cw ......... clockwise | FIL H . . . . f fillister head | LG . . . . . . . . . . . ${ }^{\text {dong }}$ |
|  | cm ......... centimeter | FM. .frequency modulation | LH . . . . . . . . . left hand |
|  | D/A . . . digital-to-analog | FP . . . . . . front panel | LIM . . . . . . . . . . Hmit |
|  | $\mathrm{dB}^{\text {d }} \ldots \ldots \ldots \ldots$ decibel | FREQ ....... frequency | LIN .... Hnear taper (used |
|  | $\mathrm{dBm} \ldots$. decibel referred |  |  |
| AMPL $\ldots \ldots$ amplifierAPC $\ldots$ automatic phasecontrol | to 1 mW | $\mathrm{g}_{\mathrm{gE}} \ldots \ldots \ldots \ldots$ gram | $\underline{\operatorname{lin}} \ldots \ldots \ldots \ldots$ unear |
|  | dc $\ldots \ldots$. $\begin{aligned} & \text { direct current } \\ & \text { deg } \ldots\end{aligned}$ degree $_{\text {(temperature }}$ | $\begin{aligned} & \text { GE . . . . . . . . germanium } \\ & \text { GHz . . . . . . gigahertz } \end{aligned}$ | LK WASH . . . lock washer LO . . low; local oscillator |
| ASSYAUX $\ldots \ldots \ldots \ldots$ assemblyavg $\ldots \ldots \ldots .$. aviliaryaverage | interval or differ- | GL. . . . . . . . . . glass | LOG . . . lograrithmic taper |
|  | ence) degree (plane | $\mathrm{GRD}^{\text {Gra }} \ldots \ldots$. grounded) | (uved in parts list) |
| $\underset{\text { AWG }}{\text { avg }} \underset{\text { gauge }}{\text { American wire }}$ | angle) | henry | $\mathrm{LPF}_{\text {LF }} \ldots \ldots, \ldots$ ow pam filter |
|  | ${ }^{\circ} \mathrm{C}$...... degree Celsius | HET . . . . . . heterodyne | LV . . . . . . . . low voltage |
| $\underset{\text { BCD }}{\text { BAL }} \ldots \ldots \ldots$ binary | - (centigrade) | HEX $\ldots . . .$. . hexagonal | $\mathrm{m} . . . . .$. meter (distance) |
|  | ${ }_{0} \mathbf{F}$. . . degree Fahrenheit |  | $\mathrm{mA} \ldots . . . .$. milliampere |
| CD decimal | ${ }^{\text {K }}$. . . . . . degree Kelvin | HDw ........ hardware | MAX . . . . . . maximum |
| BE CU $\underset{\text { copper }}{\ldots}$. ${ }^{\text {a }}$ beryllium | ${ }_{\text {DET }}^{\text {DEPC }}$. ${ }^{\text {deposited carbon }}$ | ${ }_{\text {HG }}^{\text {HF }}$. $\ldots .$. high frequency |  |
|  | diam $\ldots \ldots \ldots \ldots$ diameter |  | MEG $\ldots \underset{\text { in parts }}{\text { mitt }}$ ) ) (used |
| BFO .... beat frequency | DIA . . . diameter (used in | HP . . . . Hewlett-Packard | MET FLM . . . . metal flum |
|  | list) | HPF ..... high pass filter | MET OX . . metallic oxide |
| ${ }_{\text {BKDN }}^{\text {BH }} \ldots \ldots$.binder head <br> breakdown | DIFF AMPL $\underset{\text { amplifier }}{\text { differential }}$ | HR $\ldots \underset{\text { parts }}{ }$ list) hour (used in | MF $\ldots$ medium frequency; |
| BP ......... bandpass | div $\ldots \ldots \ldots \ldots$ division | HV . . . . . . . high voltage | parts list) |
| BPF $\ldots \ldots$ bandpass filter | DPDT ..... d double-pole, | Hz ............ Hertz | MFR . . . . . manufacturer |
| BWO . . . . . . backward-wave | double-throw | IC .... integrated circuit | mg ......... miligram |
|  | DR........... drive | ID . . . . . . inside diameter | MHz . . . . . . . megahertz |
|  | DSB . . . . double sideband | IF ....... intermediate | mH. . . . . . . . millihenry |
| CAL . . . . . .... calibrate | DTL $\ldots$ logic $_{\text {diode transistor }}$ | IMPG $\begin{gathered}\text { frequency } \\ \text { impregnated }\end{gathered}$ | ${ }_{\text {min }}^{\text {mho }} \ldots \ldots \ldots \ldots . . \mathrm{min}^{\text {mho }}$ minimum |
|  | dvm . . . digital voltmeter | in. . . . . . . . . . . . inch | $\min$. . . . . minute (time) |
|  | ECL . . . emitter coupled | INCD ..... incandescent | minute (plane |
|  | ${ }^{\text {logic }}$ | INCL $\ldots . .$. . include(s) | angle) |
|  | EMF . . electromotive force | INP . . . . . . . . . input |  |
| $\underset{\text { CMO }}{\text { COAX }}$. .abinet mount only ${ }^{\text {a }}$ coaxial | EMF . . electromotive force | Ins ......... insulation | mm . . . . . . . millimeter |
| NOTE |  |  |  |
| All abbreviations in the parts list will be in upper-case. |  |  |  |

Table 6-2. Reference Designations and Abbreviations (2 of 2)

| MOD . . . . . modulator |  |
| :---: | :---: |
| MOM | momentary |
| MOS . . . . . metalor mexide |  |
| ms | millisecond |
| MTG . . . . . . . mounting |  |
| MTR . . . meter (indicating |  |
| mV . . . . . . . . . millivolt |  |
| mVac . . . . . millivolt, ac |  |
| mVdc . . . . . millivolt, dc |  |
| mVpk . . . . millivolt, peak |  |
| mVp-p $\underset{\text { to-peak }}{\underset{\text { millivolt, peak- }}{\text {. }} \text {. }}$ |  |
| mVrms . . . millivolt, rms |  |
| mW . . . . . . . . milliwatt |  |
| MUX . . . . . multiplex |  |
| MY . . . . . . . . . . . mylar |  |
| $\mu \mathrm{A}$. . . . . . microampere |  |
| $\mu \mathrm{F}$. . . . . . microfarad |  |
| $\mu \mathrm{H}$. . . . . . . microhenry |  |
| $\mu \mathrm{mho} \mathrm{}. \mathrm{}. \mathrm{}. \mathrm{}. \mathrm{}. \mathrm{}$. |  |
| $\mu_{\text {s }} . . . . . . . . ~ m i c r o s e c o n d ~$ |  |
| $\mu \mathrm{V}$. . . . . . . . microvolt |  |
| $\mu$ Vac . . . . . microvolt, ac |  |
| $\mu \mathrm{Vdc}$. . . . microvolt, dc |  |
| $\mu \mathrm{Vpk}$. . . microvolt, peak |  |
| $\mu \mathrm{Vp}-\mathrm{p} . .$. microvolt, peak-to-peak |  |
| $\mu \mathrm{Hrms} . . . . \quad$ microvolt, rms |  |
| $\mu \mathrm{W} . . . . . . . . . ~ m i c r o w a t t ~$ |  |
| nA . . . . . . . nanoampere |  |
| NC . . . . . no connection |  |
| N/C . . . normally closed |  |
| NE . . . . . . . . . . neon |  |
| NEG . . . . . . . ${ }^{\text {a }}$ negative |  |
| nF . . . . . . . . nanofarad |  |
| NI PL . . . . . . nickel plate |  |
| N/O . . . . . normally open |  |
| NOM . . . . . . . nominal |  |
| NORM . . . . . . . normal |  |
| NPN . . ${ }_{\text {negative }}^{\text {negative-positive- }}$ |  |
| NPO |  |
|  | zero (zero temperature coefficient) |
| NRFR | . . not recommended for field replacement |
| NSR | . . . . not separately replaceable |
| ns | nanosecond |
| nW | . nanowatt |
| OBD | order by descrip- |
|  | tion |


| OD . . . . outside diameter PWV . . . . . peak working |  |
| :---: | :---: |
| OH . . . . . . . . oval head | voltage |
| OP AMPL . . . operational amplifier | RC . . . . . . . . resistancecapacitance |
| OPT . . . . . . . . option | RECT . . . . . . . rectifier |
| OSC . . . . . . . . oscillator | REF . . . . . . . . reference |
| OX . . . . . . . . . . . oxide | REG . . . . . . . . regulated |
| oz . . . . . . . . . . . ounce | REPL . . . . . replaceable |
| ת . . . . . . . . . . . . ohm | RF . . . . radio frequency |
| P . . . peak (used in pa | RFI . . . . radio frequency |
|  | interference |
| PAM . . . . pulse-amplitude | RH . . . . round head; right |
| PC . . . . . . printed circuit | RLC . . . . . . . resistance- |
| PCM .. pulse-code modula-tion; pulse-countinductance- <br> capacitance |  |
| PDM . . . . . pulse-duration | rms . . . . root-mean-square |
| modulation | RND . . . . . . . . . . round |
| pF . . . . . . . picofarad | ROM . . read-only memory |
| PH BRZ phosphor bronze | R\&P . . . . . rack and panel |
| PHL . . . . . . . . . Phillips | RWV . . . reverse working |
| PIN . . . positive-intrinsic- | voltage <br> S <br> scattering parameter |
| PIV . . . . . . peak inverse | . . . . . second (time) |
|  | ." . second (plane angle) |
| pk . . . . . . . . . . . peak | S-B . . . . slow-blow (fuse) |
| PL . . . . . . . . phase lock | (used in parts list) |
| PLO . . . . . . . phase lock | SCR . . . silicon controlled |
| PM . . . . phase | SE . . . . . . . scrifer selenium |
| PNP . . . positive-negative- | SECT . . . . . . sections |
| positive | SEMICON . . . . . semicon- |
| P/O . . . . . . . . . part of | ductor |
| POLY . . . . . polystyrene | SHF . . . . . superhigh fre- |
| PORC . . . . . . . porcelain | quency |
| POS . . positive; position(s) | SI . . . . . . . . . . silicon |
|  | SIL . . . . . . . . . . . silver |
| POSN . . . . . . . position | SL . . . . . . . . . . . . slide |
| POT . . . . potentiometer | SNR . . signal-to-noise ratio |
| p-p . . . . . . peak-to-peak | SPDT . . . . . single-pole, |
| PP ... peak-to-pea | double-throw |
|  | SPG . . . . . . . . . spring |
| PPM . . . . pulse-position | SR . . . . . . . . . split ring |
| modulation | SPST . . . . . single-pole, |
| PREAMPL . . . preamplifier | single-throw |
| PRF . . . pulse-repetition | SSB . . . . . single sideband |
| frequency | SST . . . . . . stainless steel |
| PRR . . . pulse repetition | STL . . . . . . . . . . steel |
| rate | SQ . . . . . . . . . square |
| ps . . . . . . . . picosecond | SWR . . standing-wave ratio |
| PT . . . . . . . . . . point | SYNC . . . . . synchronize |
| PTM . . . . . . . . pulse-time | T . . timed (slow-blow fuse) |
| modulation | TA . . . . . . . . tantalum |
| PWM . . . . . . pulse-width | TC . . . . . . . temperature |
| modulation | compensating |

TD . . . . . . . . . time delay TERM . . . . . . . terminal TFT . . thin-film transistor
TGL . . . . . . . . . . . toggle
THD . . . . . . . . . . thread
THRU . . . . . . . through
TI . . . . . . . . . titaniumTOL . . . . . . . . . tolerance
TRIM . . . .... trimmer

TTL . . transistor-transistor logic
TV . . . . . . . . television TVI television interference TWT . . traveling wave tube
U . . . . micro $\left(10^{-6}\right.$ ) (used in parts list)
UF . . . microfarad (used in parts list)
UHF . . ultrahigh frequency UNREG . . . . unregulated
V . . . . . . . . . . . . . . volt
VA . . . . . . . . voltampere
Vac . . . . . . . . . volts, ac
VAR . . . . . . . . . . variable
VCO ... voltage-controlled oscillator
Vdc . . . . . . . . volts, dc
VDCW. . volts, dc, working (used in parts list)
V(F) . . . . . . volts, filtered
VFO .. variable-frequency oscillator
VHF . . . . . . very-high frequency
Vpk . . . . . . . volts, peak
Vp-p . . volts, peak-to-peak
Vrms . . . . . . . volts, rms
VSWR . . . voltage standing wave ratio
VTO . . . . . . voltage-tuned oscillator
VTVM .... vacuum-tube voltmeter
V(X) . . . . . volts, switched
W . . . . . . . . . . . . . . watt
W/ . . . . . . . . . . . . with

WIV . . . . working inverse voltage
ww ....... wirewound
W/O . . . . . . . . . without
YIG .. yttrium-iron-garnet
$\mathrm{Z}_{\mathrm{o}} \ldots \ldots$.... characteristic

## NOTE

All abbreviations in the parts list will be in upper-case.

## MULTIPLIERS

| Abbreviation | Prefix | Multiple |
| :---: | :--- | :---: |
| T | tera | $10^{12}$ |
| G | giga | $10^{9}$ |
| M | mega | $10^{6}$ |
| k | kilo | $10^{3}$ |
| da | deka | 10 |
| d | deci | $10^{-1}$ |
| c | centi | $10^{-2}$ |
| m | milli | $10^{-3}$ |
| $\mu$ | micro | $10^{-6}$ |
| n | nano | $10^{-9}$ |
| p | pico | $10^{-12}$ |
| f | femto | $10^{-15}$ |
| a | atto | $10^{-18}$ |

Table 6-3. Replaceable Parts



Figure 6-1. Cabinet Parts

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\left\lvert\, \begin{aligned} & 1 \\ & 2 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & 0370-1131 \\ & 0370-2193 \end{aligned}\right.$ | 1 | KNOB; CONC: BAR AND PTR; . 5 IN; JGK KNOB:MANUAL MODE SWITCH | $\left\lvert\, \begin{aligned} & 28480 \\ & 28480 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & 0370-1131 \\ & 0370-2193 \end{aligned}\right.$ |
| $\left\lvert\, \begin{aligned} & 3 \\ & 4 \end{aligned}\right.$ | $\begin{aligned} & 2950-0043 \\ & 1250-0118 \end{aligned}$ | 4 | NUT-HEX-DBL CHAM 3/8-32-THD .094-THK CONNECTOR-RF BNC FEM SGL HOLE FR | $\begin{aligned} & 73743 \\ & 90949 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 2 x 28200 \\ & 31-2221-1022 \end{aligned}\right.$ |
| 5 | 12370-2194 | 1 | KNOB: SWEFP SWITCH | 28480 | 0370-2194 |
| 6 | 0370-1303 | 1 | KNOB; BASF; RND; 1.125 IN; JGK; SGI | 28480 | 0370-1303 |
| 7 | 08660-20101 | 1 | FRONT PANEL frame | 28480 | 08660-20101 |
| $\begin{aligned} & 8 \\ & 9 \end{aligned}$ | $2190-0016$ $08660-60115$ | 2 | WASHER-LK INTL T . 377 IN 10.507 IN OD SWITCH ASSY, MANUAL MODE (A16) | $\begin{aligned} & 78189 \\ & 28480 \end{aligned}$ | 1920-02 080115 |
| 10 | 08660-60123 | 1 | TUNER ASSY, MANUAL MODF (A17) | 28480 | 08660-60123 |
| 11 | 08660-20154 | 1 | RETAINER | 28480 | 08660-20154 |
| 12 | 0520-0129 | 3 | SCREW-MACH 2-56 Pan Ho Pozi rec sst-300 | 28480 | 0520-0129 |
| 13 | 08660-60113 | 1 | SWITCH ASSY, KEYBOARD (A1AL5) | 29480 | 08660-60113 |
| 14 | 08660-20153 | 1 | RETA INER, BRACKET | 28480 | 08660-20153 |
| 15 | 9100-3354 | 1 | COIL: FXD: AUNIO CHOKE; 4UH | 28480 | 9100-3354 |
| 176 | $2200-0105$ $2200-0141$ | 2 | SCREW-MACH $4-40$ PAN HD POZI REC SST-300 SCREW-MACH 4-40 PAN HD POZI PEC | 28480 28490 | 2200-0105 |
| 17 | 2200-0141 |  | SCREW-MACH 4-40 PAN HD POZI REC SST-300 | 28480 | 2200-0141 |
| 18 | 2190-0019 | 4 | WASHER-LK HLCL NO. 4.115 IN ID. 226 IN | 28480 | 2190-0019 |
| 19 | 3050-0023 | , | WASHER-FL NM NO. 6.144 IN ID . 25 IN OD | 28480 | 3050-0023 |
| 20 | 3050-0016 | 3 | WA SHER-FL MTLC NO. 6.147 IN 10.281 IN | 28480 28480 | $3050-0016$ |
| $\begin{array}{\|l} 21 \\ 22 \end{array}$ | $\left\lvert\, \begin{aligned} & 08660-60111 \\ & 0520-0174 \end{aligned}\right.$ | 1 | BOARD ASSY, NUMERAL READOUT (A1A12) <br> SCREW-MACH 2-56 PAN HD POZI REC SST-300 | $\begin{array}{l\|l\|l\|l\|} 28480 \\ 284800 \end{array}$ | $\left\lvert\, \begin{aligned} & 08660-60111 \\ & 0520-0174 \end{aligned}\right.$ |
| 23 | 3101-1655 | 1 | SWITCH-TGL SUBMIN SPDT 5A 115VAC/OC | 09353 | 7101-J1CX |
| 24 | 08660-60114 | 1 | SWITCH ASSY, SWEEP YODE (AL5) | 23480 | 08660-60114 |
| 25 | 08660-40107 | 1 | SINGLE SWEFP PUSHBUTTON | 28480 | 08660-40107 |
| 26 27 | 0360-1190 | 1 | TERMINAL, SLDR LUG, 3/8 SCR, . $38 / .078$ FRONT PANEL, LEFT SIDE | 28480 28480 | 0360-1190 $08660-00106$ |
| 28 | 08660-20177 |  | WINDOW, FRDNT | 28480 | 08660-20177 |
| 29 | 08660-00102 | 1 | FPONT PANEL, RIGHT SIDE | 28480 | 08660-00102 |
| 30 | 08660-40004 | 1 | ANNUNCIATOR BLOCK | 28480 | 08560-40004 |
| 31 | 08660-60159 | 1 | anNunciator circuit board | $28480$ | 08660-60159 |
| 32 | $0510-1149$ | 1 | RETAINER ${ }^{\text {P PUSH ON; }} \mathbf{1 2 5}$ DIA; PHS STL | 28480 | 0510-1149 |
| $\left\lvert\, \begin{aligned} & 33 \\ & 34 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & 2140-0356 \\ & 08660-40108 \end{aligned}\right.$ | $1$ | LAMP; INCAND: BULB T1; 5V PUSHBUTTON, READDUT | $\begin{array}{\|l\|l\|} \hline 71744 \\ 28480 \end{array}$ | $\begin{aligned} & \text { CM7-7683 } \\ & 08660-40108 \end{aligned}$ |



Figure 6-2. DCU Front Panel Parts

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | 08660-60272 | 1 | DIGITAL CONTROL ASSY | 28480 | 08660-60272 |
| A1C1 | 0160-3448 | 1 | CAPACITOR-FXD 1000 PF +-10\% 1000NVDC CER | 28480 | 0160-3448 |
| Ald 1 | 1250-0118 | 1 | CONNECTOR-RF BNC FEM SGL HOLE FR | 90949 | 31-2221-1022 |
| All 1 | 9100-3354 | 1 | COIL: FXD: AUDIO CHOKE; 4 UH | 28480 | 9100-3354 |
| A1H1 A1H2 | 08660-60116 | 1 | CABLE ASSY, SWITCH CABLE ASSY. KEYBDARD | $\left\lvert\, \begin{aligned} & 28480 \\ & 28480 \end{aligned}\right.$ | 08660-601 16 08660-60117 |
| A1H3 | 08660-60117 | 2 | CABLE ASSY, READOUT | 28480 28480 | 08660-60117 |
| A1H4 | 08660-60118 |  | CABLE ASSY, REACOUT | 28480 | 08660-60118 |
| AlW 5 | 08680-60124 | 1 | CABLE, d/A OUTPUT | 28480 | 08660-60124 |
| A1W6 <br> A1H7 | $\left\lvert\, \begin{aligned} & 08660-60126 \\ & 08660-60129 \end{aligned}\right.$ | 1 | WIRING HARNESS CABLE ASSY, 4V FILTER | $\begin{array}{\|l\|l} 28480 \\ 28480 \end{array}$ | $\begin{aligned} & 08660-60126 \\ & 08660-60129 \end{aligned}$ |
|  |  |  | miscellaneous al |  |  |
|  | 0900-0023 | 1 | "RING" 0.250" ID | 07322 | MR 8010 |
|  | 08660-00069 | 1 | SHIELD, R.F.I. | 28480 | 08660-00069 |
|  | 08660-00101 | 1 | SUPPORT, DIGITAL TOP | 28480 | 08660-091 01 |
|  | 08660-00103 | 1 | SUPPDRT, DIGITAL BOTTOM INSULATOR, INTER CONNECT | 28480 28480 | $\left\lvert\, \begin{aligned} & 08680-00103 \\ & 08660-00110 \end{aligned}\right.$ |
|  | $\left\lvert\, \begin{aligned} & 08660-20121 \\ & 08660-20152 \end{aligned}\right.$ | 1 | SUB-PANEL. FRONT FRONT PANEL, KEYBOARD | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-20121 \\ & 08660-20152 \end{aligned}$ |
|  | 08660-20160 | 1 | RETAINER, P.C. BJAPD | 28480 | 08660-20160 |
|  | 08660-20161 | 1 | SPACER, ROD | 28480 | 08660-20161 |
|  | 08660-40105 | 1 | FREQUENCY RANGE INDICATOR | 28480 | 08660-40105 |
|  | 08660-40108 | 1 | PUSHBUTTON, READOUT | 28480 | 08660-40108 |
| A141 | 08660-60200 | 1 | BIARD ASSY, SHITCH CONTROL | 28480 | 08660-60200 |
| A IA 1C1 | 0 180-2206 | $4$ | CAPACITOR-FXD; 6OUF+-10\% GVDC TA-SOLID | 56289 | $1500606 \times 900682$ |
| A 1A1C2 | 0160-3536 | $1$ | CAPACITOR-FXD 62OPF +-5\% 100WVDC MICA | 28480 | $0160-3536$ |
| A1AIC3 | 0130-1714 |  | CAPACITOR-FXD; 330UF+-10\% 6VOC, TA-SOLIO | 56289 | $1500337 \times 900652$ |
| AlAIC4 AIAIC5 | $0180-0197$ $0180-0197$ | 62 | CAPACI TOR-FXD; $2.2 \mathrm{UF}+-10 \%$ 20VDC TA CAPACITOR-FXD; $2.2 \mathrm{UF}+-10 \% 20 \mathrm{VDC} \mathrm{TA}$ | 56289 56289 | $\begin{aligned} & 1500225 \times 9020 A 2 \\ & 1500225 \times 9020 A 2 \end{aligned}$ |
| Alalcs | 0180-0197 |  | CAPACITOR-FXD: 2.2UF + -10\% 20VDC TA | 56289 | $1500225 \times 902022$ |
| A1A1C6 | $0180-0197$ |  | CAPACITOR-FXD: $2.2 U^{C+-10 \% ~ 20 V D C ~ T A ~}$ | 56289 | $1500225 \times 902042$ |
| A1A1C7 | 0 180-0197 |  | CAPACITOR-FXD: 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 9020 \mathrm{~A} 2$ |
| AIAIC8 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA | 56289 56289 | 150D225 X9020A2 |
| AlAICO | 0180-0197 |  | CAPACITOR-FXD; 2.2UF + - 10\% 20VDC TA | 56289 | $1500225 \times 902042$ |
| AlAlCrl | 1901-0040 | 70. | DIDDE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A 1A1R1 | 0698-7228 | $4$ | RESISTOR 464 OHM 2\% .05W F TUBLLAR | 24546 | C3-1/8-T0-464R-G |
| AIA1R2 | $0698-7272$ | $1$ | RESISTOR 31.6K 2\% .05W F TUBULAR | 24546 | $\text { C } 3-1 / 8-T 0-3162-G$ |
| AIA1R3 | 0698-7253 | 16 | RESISTOR 5.11K 2\% .O5W F TUBULAR | 24546 | $\text { C } 3-1 / 8-10-5111-6$ |
| A IA1R4 | $0698-7253$ |  | RESISTIR 5.11 K 2\% .05W F TUBILIAR | 24546 | C3-1/8-70-5111-G |
| AlAR 5 | $0698-7253$ |  | RESISTOR 5.11 K 2\% .05W F TUBULAR | 24546 | C3-1/8-T0-5111-G |
| AlAIR 6 A1A1R A | $\begin{aligned} & 0698-7253 \\ & 0698-7253 \end{aligned}$ |  |  |  | $C 3-1 / 8-T O-5111-G$ |
| AIA1R7 | 0698-7253 |  | RESISTOR 5.11K 2\% .O5W F TUBULAR | $\begin{aligned} & 24546 \\ & 74546 \end{aligned}$ | $\operatorname{c3-1/8-T0-5111-6}$ |
| AIAIR8 | 0698-7253 |  | RESISTOR 5.11K $2 \pi .05 \mathrm{~W}$ F TUBULAR | 24546 | $\mid C 3-1 / 8-T 0-5111-6$ |
| AIA1R9 AIA1R10 | $\begin{aligned} & 0698-7253 \\ & 0698-7253 \end{aligned}$ |  | RESISTOR 5.11K 2\% .05N F TUBULAR RESISTOR 5.11 K 2 F .05 W F TUBULAR | 24546 24546 | $\left\lvert\, \begin{aligned} & C 3-1 / 8-T 0-5111-G \\ & C 3-1 / 8-T 0-5111-G \end{aligned}\right.$ |
| AIAIR 10 | 0698-7253 |  | RESISTOR 5.11K 2\% .05W F TUBULAR | $24546$ | C3-1/8-T0-5111-G |
| A 1A1R11 |  |  | RESISTOR 5.11K 2\% .05W F TUBULAR |  | C3-1/8-T0-5111-G |
| AIA1R12 | $0698-7253$ |  | RESISTOR $5.11 \mathrm{~K} 2 \% .05 \mathrm{~W}$ F TURULAR | $24546$ | $\text { C } 3-1 / 8-\text { T0-5111-6 }$ |
|  | $\begin{aligned} & 0698-7253 \\ & 0698-7222 \end{aligned}$ |  | RESISTOR 5.11K 2\% .05W F TUBILLAR RESISTOR 261 OHM $2 \% .05 \mathrm{H}$ F TUBULAR | 24546 24546 | C3-1/8-T0-5111-6 <br> C3-1/B-T0-261R-G |
| A IA 1 R14 A IA 1215 | $\text { \| } 0698-7222$ | 3 | RESISTOR 261 DHM $2 \% .05 \mathrm{~W}$ F TUBULAR RESISTOR 454 OHM 2\%.05W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 3-1 / 8-T 0-261 R-G \\ & C 3-1 / g-T 0-464 R-G \end{aligned}\right.$ |
| AIA1R 15 | 0698-7228 |  | RESISTOR 454 OHM 2\% .05W F TUBULAR | $24546$ | C3-1/8-T0-464R-G |
| A AAR16 A1A1R17 $A$ |  |  | RESISTOR 5.11K 2\% .05W F TUBULAP RESISTOR 5.11K 2\%.05W F TUBULAR |  |  |
| A $141 R 17$ A A A P18 $A$ | 0698-7253 |  | RESISTOR $5.11 \mathrm{~K} 2 \%$.05W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 3-1 / 8-T 0-5111-G \\ & C 3-1 / 8-T 0-5111-G \end{aligned}\right.$ |
| AIAR19 | 0698-7253 |  | RESISTOR 5.11K 2\% .05W F TUBULAR. | 24546 | C3-1/8-T0-5111-6 |
| A 1A1R 20 | 0698-7253 |  | RESISTOR 5.11K 2\%.05N F TUBULAR | 24546 | C3-1/8-10-5111-G |
|  | $\begin{aligned} & 0698-7212 \\ & 0698-7212 \\ & 0698-7228 \\ & 0698-7228 \end{aligned}$ | 3 | RESISTOR 100 OHM 2\% .O5W F TUBULAR RESISTOR 100 กHM 2\%.05W F TUBULAR RESISTOR 464 OHM 2\%.05W F TURULAR RESISTIR 464 THM 2\%.05W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 3-1 / 8-T O-100 R-G \\ & C 3-1 / 8-T O-100 R-G \\ & C 3-1 / 8-T 0-464 R-G \\ & \mathrm{C} 3-1 / 8-T 0-464 R-G \end{aligned}$ |
| A1A1TPI <br> AIA1TP2 | $\left\lvert\, \begin{aligned} & 0360-1514 \\ & 0360-1514 \end{aligned}\right.$ | 15 | TERMINAL: SLDR STIO TERMINAL: SLDR STUD | $\begin{array}{\|l\|l} 28480 \\ 28480 \end{array}$ | $\left\lvert\, \begin{aligned} & 0360-1514 \\ & 0360-1514 \end{aligned}\right.$ |
| A 141111 | 1820-0913 | 3 | IC DGTL SN74L 122 n MIJLTIVIBRATOR | 01295 | SN74L122N |
| alaluz | 1820-0174 | 17 | IC DGTL SN74 04 N INVERTER | 01295 | SN7404N |
| A 14103 | 1820-0256 | 3 | IC DGTL MC 858 BP BUFFER | 04713 | MC859p |
| A 141114 A 14115 | $1820-0600$ $1820-0600$ | 6 | IC DGTL DM85L 90N COUNTER IC DGTL DMB5L $90 N$ COUNTER | $\begin{aligned} & 27014 \\ & 27014 \end{aligned}$ | $\text { DM74L } 90 \mathrm{~N}$ <br> DMF4L90N |

Table 6-3. Replaceable Parts

\begin{tabular}{|c|c|c|c|c|c|}
\hline \begin{tabular}{l}
Reference \\
Designation
\end{tabular} \& HP Part Number \& Oty \& Description \& Mfr Code \& Mfr Part Number \\
\hline A1A1U6 \& 1820-0600 \& \& IC DGTL DM85L 90N COUNTER \& 27014 \& DM74L90N \\
\hline Alalu7 \& 1820-0600 \& \& IC JGTL OMP5L 90N COUNTER \& 27014 \& DM74L90N \\
\hline A1A1U8 \& 1820-0600 \& \& IC OGTL DM85L 90N COUNTER \& 27014 \& DM74L90N \\
\hline A 1 A1U9
A 1 A 1410 \& 1820-0600 \& \& \& 27014
01295 \& DM74L90N
SN7400N \\
\hline A LA 1010 \& 1820-0054 \& 63 \& IC DGTL SN74 00 NGATE \& 01295 \& SN7400N \\
\hline A 141011 \& 1820-0595 \& 5 \& IC DGTL DM74L 73N FLIP-FLOP \& \[
27014
\] \& DM74L 73N \\
\hline A 141012 \& 1820-0174 \& \& IC DGTL SN74 04 N INVERTER \& 01295 \& N7404N \\
\hline A 1 A 11113 \& 1820-0372 \& 8 \& IC DGTL SN74H 11 N GATE \& 01295 \& SN74H11N \\
\hline A1A1U14
A1A1U15 \& \(1820-0587\)
\(1820-0596\) \& 5 \& IC OGTL DM74L 10 N GATE \& 27014
27014 \& DM \(74 L 10 \mathrm{~N}\)
DM74L74N \\
\hline AlAlU16 \& 1820-0595 \& 1 \& IC DGTL FLIP FLOP \& 27014 \& DM74L73N \\
\hline A 141017 \& 1820-0174 \& \& IC DGTL SN74 04 N INVERTER \& 01295 \& SN7404N \\
\hline A1A1H18 \& 1820-0054 \& \& IC DGTL SN74 00 N GATE \& 01295 \& SN7400N \\
\hline A 1 A1U19 \& 1820-0374 \& 1 \& IC DGTL SN74H 21 N GATE \& 01295 \& SN74H21N \\
\hline A1A 1 U (
A1A 1 U 21 \& \(1820-0511\)
\(1820-0077\) \& 14 \& \[
\begin{array}{llll}
\text { IC OGTL SN74 } \& \text { O8 } \& \text { N GATE } \\
\text { IC DGTL SN74 } \& 74 \& \text { N FLIP-FLOP }
\end{array}
\] \& \[
\text { |ll } \begin{aligned}
\& 01295 \\
\& 01295
\end{aligned}
\] \& \[
\begin{array}{|l}
\text { SN7408N } \\
\text { SN7474N }
\end{array}
\] \\
\hline a 141022 \& 1820-0587 \& \& IC DGTL DM74L 10N GATE \& 27014 \& DM74L10N \\
\hline A1A1U23 \& 1820-0595 \& \& IC DGTL DM74L 73N FLIP-FLOP \& 27014 \& DM74LT3N \\
\hline A 141024 \& 1820-0328 \& 10 \& IC DGTL SN74 02 N GATE \& 01295 \& SN7402N \\
\hline A 141025 \& 1820-0054 \& \& IC OGTL SN74 00 N GATE \& 01295 \& SN7400V \\
\hline A1A1U26 \& 1820-0495 \& 4 \& IC DGTL DECDDER \& 07263 \& 93110 C \\
\hline A 1A1U27 \& 1820-0054 \& \& IC DGTL SN74 00 N GATE \& 01295
27014 \& \begin{tabular}{l}
SN1400N \\
DM74174N
\end{tabular} \\
\hline A1A1U28 \& 1820-0596 \& \& IC DGTL DM74L 74 N FLIP-FLOP IC DGTL SN74 74 N FLIP-FLOP \& 27014
01295 \& \[
\begin{aligned}
\& \text { DM741 74N } \\
\& \text { SN7474N }
\end{aligned}
\] \\
\hline  \& \(1820-0077\)
\(1820-0661\) \& 11 \& IC
IC
IC
OGTL
OGTL
SN74
SN74 \& 01295
01295 \& SN7474N \\
\hline A A 1u31 \& 1820-0054 \& \& IC DGTL SN74 00 N GATE \& 01295 \& SN7400N \\
\hline A 1A \(1 \cup 32\) \& 1820-0596 \& \& IC DGTL OM74L 74 N FLIP-FLOP \& 27014 \& \[
\text { DM74L } 74 \mathrm{~N}
\] \\
\hline A1A1U33 \& 1820-0511 \& \& IC DGTL SN74 08 N GATE \& 01295 \& SN7408V \\
\hline A1A1XA1 \& 1200-0507 \& 10 \& SOCKET: ELEC; IC 16-CONT DIP SLDR TERM \& 06776 \& ICN-163-S3W \\
\hline A 142 \& 08660-60176 \& 1 \& BOARD ASSY,KEY CONTROL \& 28480 \& 08660-60176 \\
\hline A1A 2C1 \& 0160-0945 \& 3 \& CAPACITOR-FXD 910PF +-5\% 100WVDC MICA \& 28480 \& 0160-0045 \\
\hline A1A2C2 \& 0160-2204 \& 13 \& CAPACITOR-FXD 100PF +-59 300WVDC MICA \& 28480 \& 0160-2204 \\
\hline A1A 2C5 \& 0180-0197 \& \& CAPACITOR-FXD; \(2.2 \mathrm{UF}+-10 \%\) 20VDC TA \& 56289 \& \(1500225 \times 902042\) \\
\hline A1A2C6 \& 0180-0197 \& \& CAPACITOR-FXD; 2.2UF+-10\% 20VOC TA \& 56289 \& \(1500225 \times 902\) OA2 \\
\hline A1A 2C7 \& 0180-0197 \& \& CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA \& 56289 \& \(1500225 \times 902042\) \\
\hline A1A2C8 \& 0180-0197 \& \& CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA \& 56289 \& \(1500225 \times 902042\) \\
\hline A1A 2C9 \& 0180-0197 \& \& CAPACITOR-FXD; 2.2UF+-10\% 2OVNC TA \& 56289 \& \(1500225 \times 902042\) \\
\hline A1A2C10 \& 0180-0197 \& \& CAPACITDR-FXD; 2.2UF+-10\% 2OVDC TA \& 56289 \& 1500225 9002042 \\
\hline \[
\begin{aligned}
\& A 1 A 2 C 11 \\
\& A 1 A 2 C 12
\end{aligned}
\] \& \[
\left\lvert\, \begin{array}{lll}
0 \& 180-0197 \\
0 \& 140-0199
\end{array}\right.
\] \& \& CAPACITOR-FXD: 2.2UF+-10\% 20VDC TA CAPACITOR-FXD 240PF +-5\% 300WVDC MICA \& \[
\begin{aligned}
\& 56289 \\
\& 72136
\end{aligned}
\] \& \[
\begin{aligned}
\& 1500225 \times 902042 \\
\& \text { DM15F241J0300WV1CR }
\end{aligned}
\] \\
\hline A1A2C13 \& 0 160-3533 \& 1 \& CAPACITOR-FXD 470PF +-5\% 100WVDC MICA (JPT 004 ONLY) \& 28480 \& 0160-3533 \\
\hline A 142C14 \& 0160-0161 \& 6 \& CAPACITOR-FXD . \(01 U F+\)-10\% 200WVOC POLYE \& 56289 \& 292P10392 \\
\hline \[
\begin{aligned}
\& A 1 A 2 C 15 \\
\& A 1 A 2 C 16
\end{aligned}
\] \& \(\begin{aligned} \& 0160-0161 \\ \& 0 \\ \& 0\end{aligned} 160-0161\) \& \& CAPACITOR-FXD .OIUF +-10\% 200WVDC POLYE CAPACITOR-FXD \(01 \mathrm{UF}+-10 \%\) 200WVDC POLYE \& \[
\begin{aligned}
\& 56289 \\
\& 56289
\end{aligned}
\] \& \[
\begin{aligned}
\& 292 P 10392 \\
\& 292 P 10392
\end{aligned}
\] \\
\hline A1A 2C17 \& -180-0197 \& \& CAPACITOR-FXD; \(2.2 \mathrm{UF}+-10 \%\) 20VDC TO. \& 55689 \& 1508225×902042 \\
\hline A1A201 \& 1853-0020 \& 4 \& TRANSISTOR PNP SI CHIP PD=300MH \& 28480 \& 1853-0020 \\
\hline A 1A 2R 1 \& 0757-0419 \& 2 \& RESISTOR 681 DHM 1\%.125W F TUBULAR \& 24548 \& C.4-1/8-T0-581R-F \\
\hline \(A 1 A 2 R 2\) \& 0757-0428 \& 24 \& RESISTDR 1.62 K 19.125 W F TUBULAR \& 24546 \& C4-1/8-T0-1621-F \\
\hline A1A2R 3 \& 0698-0082 \& 36 \& RESISTIR 464 OHM 19.125 W F TUBULAR \& 16299 \& C4-1/8-T0-4640-F \\
\hline A1A2R 4 \& 0757-0280 \& 46 \& RESI STOR 1K 1\% -125W F TUBULAR \& 24546 \& C4-1/8-T0-1001-F \\
\hline A1: 2R 5 \& 0698-3430 \& 9 \& RESISTOR 21.5 OHM 1\%.125W F TURULAR \& 03888 \& PME 55-1/9-T0-21R5-F \\
\hline \[
\begin{aligned}
\& A 1 A 2 R 6 \\
\& A 1 A 2 R 7
\end{aligned}
\] \& \[
\begin{aligned}
\& 0698-3430 \\
\& 0757-0280
\end{aligned}
\] \& \& RESISTOR 21.5 OHM 1\% . 125 W F TUBULAR RESISTOR 1K 1\% • 125 W F TURULAR \& \[
\begin{aligned}
\& 03888 \\
\& 24546
\end{aligned}
\] \& \[
\begin{aligned}
\& \text { PME 55-1/8-T0-21R5-F } \\
\& \text { C4-1/8-T0-1001-F }
\end{aligned}
\] \\
\hline \(\triangle 142 \mathrm{R} 8\) \& 0698-3430 \& \& RESISTDR 21.5 gHM 18.125 W F TUBULAP. \& 03888 \& PME 55-1/8-T0-21R5-F \\
\hline A1A2R9 \& 0698-3430 \& \& RESISTOR 21.50 OHM 12.125 W F TUBULAR \& 03888 \& PME 55-1/8-T0-21R5-F \\
\hline A 1A2R 10 \& 0757-0280 \& \& RESISTOR 1 K 12. 125 W F TUBULAR \& 24546 \& C4-1/8-T0-1001-F \\
\hline A \(1822^{\circ} 11\) \& 0757-0438 \& 12 \& RESISTOR 5.11K 1\% 125 H F TUBULAR \& 24546 \& \\
\hline A1A 2 P 12
A 1 A 2 O 13 \& \(0757-0395\)
\(0698-3430\) \& 2 \& RESISTOR 56.2 OHM \(1 \% .125 \mathrm{~W}\) F TUBULAR \& 24546
03888 \& \begin{tabular}{l}
\[
\mathrm{C} 4-1 / 8-\mathrm{TO}-56 \mathrm{R} 2-\mathrm{F}
\] \\
PMF 55-1/8-T 0-21R5-F
\end{tabular} \\
\hline A 142013
\(A 142 R 14\) \& \(0698-3430\)
\(0698-3160\) \& \& RESISTOR
RESISTOR
21.5 OHM

RES \& 03888
16299 \& PME 55-1/8-T 0-21R5-F C4-1/8-TO-3162-F <br>
\hline A 142214

A 142 P 15 \& 0698-3160 \& 2 \& | RESISTOR |
| :--- |
| RESISTOR |
| 31.6 K |
| $1 \%$ |
| $1 \%$ | \& 16299

16299 \& C4-1/8-T0-3162-F
C4-1/8-T0-3162-F <br>
\hline A 1A 2816 \& 0698-3430 \& \& RESISTOR 21.5 OHM 1\% . 125W F TUBULAR \& 03888 \& PME 55-1/8-T 0-21 R5-F <br>
\hline A 142817 \& 0698-3159 \& 3 \& RESISTOR . 26.1 K 1\% .125W F TUBULAR \& 16299 \& C4-1/8-T0-2612-F <br>
\hline A1A2R18 \& 0698-3159 \& \& RESISTOR 26.1K 1\% .125W F TUBULAR \& 16299 \& C4-1/8-T0-2612-F <br>
\hline 4142 P 19 \& 0757-0438 \& \& RESISTOR 5.11K 1 \% .125W F TUBULAR \& 24546 \& C4-1/8-T0-5111-F <br>
\hline A142F 20 \& 0898-3132 \& 16 \& RESISTOR 261 OHM 1\%.125W F TUBULAR \& 16299 \& C4-1/8-T0-2610-F <br>
\hline A 142221 \& 0757-0433 \& \& RESISTOR 5.11K 19 . 125 W F TUBULAR \& 24546 \& C4-1/8-T0-5111-F <br>
\hline A 142 R 22 \& 0757-0298 \& 7 \& RESISTOR 0.09 K 1\% \& 19701 \& MF4C1/8-T0-9091-F <br>
\hline A1ATR 23 \& 0757-0280 \& \& RESISTOR 1K 1 T , 125 W F TUBULAR \& 24546 \& C4-1/8-T0-1 001-F <br>
\hline A1428 24 \& 0698-3132 \& \& RESISTOR 261 IHM 18.125 W F TUBULAR \& 16299 \& C4-1/8-T0-2610-F <br>
\hline A14 2P 25 \& 0698-3132 \& \& RESISTOR 261 DHM $1 \% .125 \mathrm{~W}$ F TUBULAR \& 16299 \& C4-1/8-T0-2610-F <br>
\hline
\end{tabular}

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number 0 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & A 1 A 2 T P 1 \\ & A 1 A 2 T P 2 \end{aligned}$ | $\begin{aligned} & 0360-1514 \\ & 0360-1514 \end{aligned}$ |  | TERMINAL: SLDR STUD TERMINAL; SLDR STUD | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0360-1514 \\ & 0360-1514 \end{aligned}$ |
| A 1A 2U1 | 1820-0174 |  | IC DGTL SN74 04 N INVERTER | 01295 | SN7404N |
| A 14202 | 1820-0661 |  | IC DGTL SN74 32 NGATF | 01295 | SN7432V |
| Ala 203 | 1820-0054 |  | IC DGTL SN74 00 NGATE | 01295 | SN7400Y |
| A 14214 | 1820-0709 | 10 | IC DGTL REGISTER | 07263 | 93L 280C |
| alazus | 1820-0659 | 17 | If dgil register. | 07263 | 931000: |
| A 14206 | 1820-0709 |  | IC DGTL REGISTER | 07263 | $931280 \%$ |
| A 1a 207 | 1820-0281 | 1 | IC OGTL SN74 107 N FLIP-FLOP | 01295 | SN74107N |
| A1A2U8 | 1820-0511 |  | IC OGTL SN74 O8 N GATE | 01205 | SN7408V |
| A1A2U9 | 1820-0054 |  | IC OGTL SN74 00 N GATE | 01295 | SN7400N |
| A1A2U10 * | 1820-0511 |  | IC DGTL SN74 08 N GATE | 01295 | SN7408V |
| A 142011 | 1820-0710 | 6 | IC OGTL MULTIPLEXER | 07263 | 931220 C |
| A $142 \mathrm{Ul2}$ | 1820-0710 |  | IC DGTL MULTIPLEXER | 07263 | 9322205 |
| A1A 2U13 | 1820-0659 |  | IC DGTL REGISTER | 07263 | 9310005 |
| A 1 A 2014 | 1820-0659 |  | IC OGTL REGISTER | 07263 | 93 LOODC |
| A 142015 | 1820-0710 |  | IC gGtl multiplexer | 07263 | 93L 22DC |
| A 142016 | 1820-0054 |  | IC DGTL SN74 00 N GATE | 01295 | SN7400N |
| A1A2U17 | 1820-0596 |  | IC OGTL OM74L 74N FLIP-ELOD | 27014 | DM74L74N |
| A 142418 | 1820-0174 |  | IC DGTL SN74 04 N INVERTER | 01295 | SN7404N |
| A 142 Cl A 142 U 20 | 1820-0913 |  |  | 01295 07263 | SN74L12 2N <br> 7110 C |
| A 1A 2 U 20 | 1826-0055 | 1 |  | 07263 | 7110 C |
| A 1 A 2021 | 1820-0069 | 5 | IC DGTL SN74 20 N GATE | 01295 | SN7420N |
| A 1 A 2 U 22 | 1820-0174 |  | IC DGTL SN74 04 N INVERTER | 01295 | SN7404N |
| A 142 S 23 A 1 A $2 U 24$ | 1820-0214 | 7 | $\begin{array}{llll}\text { IC } & \text { OGTL } \\ \text { IC } & \text { SN74 } & 42 & \mathrm{~N} \text { DECODER } \\ \text { SNT4 } & 32 & \mathrm{~N} \text { GATE }\end{array}$ | 01295 01295 | SN7442N |
| A142U25 | 1820-0055 | 4 | IC DGTL SN74 90 N COUNTER | 01295 | SN7400N |
| A 1A 2026 | 1820-0491 | 1 | IC DGTL SN74 145 N DFCODER | 01295 | SN74145N |
| A1A3 | 08660-60191 | 1 | BOARD ASSY, READOUT CONTRCL | 28480 | 08660-50191 |
| A1A3Ct | 0180-0197 |  | CAPACITOR-FXI; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 902042$ 泪 |
| A 1a3C2 | 0180-0197 |  | CAPACITAR-FXD; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 902042$ |
| A 1A 3C3 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 902012$ \% |
| A 1A 3C4 | 0180-0197 |  | CAPACITDR-FXD: 2.2UF+-108 20VDC TA | 56289 | $1500225 \times 902042$, 帾 |
| A1A3C5 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 902042$, |
| A1A3C6 | 0180-0197 |  | CAPACITOR-FXO; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 902042$ |
| A1A3C7 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 902042$ |
| A 1A 3C8 | 0180-0197 |  | CAPACITOR-FXD; $2.2 \mathrm{UF}+-10 \%$ 20VDC TA | 56289 | $1500225 \times 902042$ |
| A1A3C9 | 0160-3534 | 2 | CAPACITOR-FXD 510PF +-5\% 100HVDC MICA | 28480 | 0160-3534 |
| A1A3C10 | 0160-0161 |  | CAPACITOR-FXD . $01 U F+-10 \%$ 200HVDC POLYE | 56289 | 292P10392 |
| A1A3C11 | 0160-2208 | 2 | CAPACITDR-FXO $330 P F+-5 \% ~ 300 W V D C ~ M I C A ~$ | 28480 72136 | 0160-2208 |
| A1A3C 12 | 0140-0196 | 2 | CAPACITOR-FXD 150PF +-5\% 300NVDC MICA | 72136 | OM15F151J0300WV1CR |
| A 14 A 3R 1 A 1A 3 2 A | 0698-3447 | 22 | RESISTOR 422 GHM 1\%. 125 W F TUBULAR | 16299 | C4-1/8-T0-422R-F |
| A 1A 3R2 | 0698-3447 |  | RESISTOR 422 OHM 1\%.125W F TUBULAR | 16299 | C4-1/8-T0-422R-F |
| A1A3R 3 | 0698-3447 |  | RESISTOR 422 OHM 1\%.125 F F TUBULAR | 16299 | C4-1/8-T0-422R-F |
| A1A3R4 | 0698-3447 |  | RESISTOR 422 OHM 18.125 W F TUBULAR | 16299 | C4-1/8-T0-422R-F |
| A 1A 3R 5 | 0698-3447 |  | RESISTOR 422 OHM 1\% .125W F TUBULAR | 16299 | C4-1/8- 0 - $422 \mathrm{R}-\mathrm{F}$ |
| A 14 <br> A 143 P | 0698-3447 |  | RESISTOR 422 OHM 18.125 W F TUBULAR |  | C4-1/8-T0-422R-F ${ }^{\text {c }}$. |
| A1A 1 3R 7 AlA 3 P 8 | 0698-3447 |  | RESISTOR 422 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 16299 | $(4-1 / 8-T 0-422 R-F$ |
|  | 0698-3447 |  | RESISTDR 422 OHM 1\% . 125 W F TUBULAR | 18299 | C4-1/8-T0-422R-F |
| A1A 389 A 1 A 3 P 10 | 0698-3447 |  | RESISTOR 422 OHM 1\%.125W F TUBULAR | 16299 | $C 4-1 / 8-T 0-422 n-F$ |
| A 1A 3R 10 | 0698-3447 |  | RESISTOR 422 OHM 18.125 W F TUBULAR | 16299 | C4-1/8-T0-422R-F |
| A 143 SR 11 A 1 A 3 R 12 | 0698-3159 | 30 | RESISTOR 26.1 K 1 1\% 125 W F TUBULAR RESISTOR 100 OHM 1 m . 125 W F TUBULAR | 16299 24545 | $C 4-1 / 8-\mathrm{TO}-2612-F$ $\mathrm{C} 4-1 / 8-\mathrm{TO}$ C |
| A1A3R 12 A 1A 3R13 | $0757-0401$ $0698-3447$ | 30 | RESISTIR RESISTOR 422 OHM | 24548 16299 | $\left\{\begin{array}{l} C 4-1 / 8-T 0-101-F \\ C 4-1 / 8-T 0-422 R-F \end{array}\right.$ |
| A1A3R 14 | 0757-0346 | 16 | RESISTOP. 10 OHM 1\%.125W F TUBULAR | 24546 | C4-1/8-T0-10RO-F |
| A 143 R 15 | 0757-0346 |  | RESISTOR 10 OHM 18.125W F TUBULAR | 24546 | C4-1/8-TO-I OR O-F |
| Ala 301 A1A 302 | 1820-0661 |  | IC OGTL SN74 NOT ASSI GNED | 01295 | SN7432N |
| A1A3U3 | 1820-0725 | 1 | If. DGTL SN74 170 J MEMORY | 01295 | SN74170J |
| A 14304 | 1820-0054 |  | IC DGTL SN74 00 N GATE | 01295 | SN7400N |
| A1A3U5 | 1820-0054 |  | IC DGTL SN74 00 N GATE. | 01295 | SNT400N |
| A1A3U6 | 1820-0174 |  | If DGTL SN74 04 N INVFRTFR | 01205 | SN7404V |
| A 14307 | 1820-0214 |  | If DGTL SN74 42 N DECCDER | 01295 | SN7442V |
| -1A3U8 | 1820-0659 |  | IT DGTL RFGISTER | 07263 | 93L000: |
| A143U9 | 1820-0054 |  | IC OGTL SNT4 00 N GATE | 01295 | SN7400V |
| A1A3U10 | 1820-0913 |  | IC DGTL SN74L 122 N MULTIVIBRATOR | 01295 | SN74L122N |
| $\begin{aligned} & \text { AlA } 3 U 11 \\ & \text { A1A } 3 U 12 \end{aligned}$ | 1820-0904 | 1 | IC TGTL CNMPARATOR NOT ASSIGNED | 07263 | 9312400 |
| A 143013 | 1820-0328 |  | if. DGTL SN74 02 N GATE | 01295 | SN7402N |
| A1A3U14 | 1820-0596 |  | IC JGTL DM74L 74N FLIP-FLOP | 27014 | DM74L74N |
| A1431115 | 18.20-0054 |  | IC JGTL SN74 00 N GATE | 01295 | SN7400N |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A $143 U 16$ A $1 A 3 U 17$ A $1 A 3 U 18$ $A 1 A 3 U 19$ $A 1 A 3 U 20 ~$ | $\begin{array}{\|l} \hline 1820-0054 \\ 1820-0710 \\ 1820-0372 \\ 1820-0328 \\ 1820-0055 \end{array}$ |  | IC DGTL SN74 00 N GATE  <br> IC OGTL MULTIPLEXER   <br> IC OGTL SN74H 11 N GATE <br> IC OGTL SN74 02 N GATE <br> IC DGTL SN74 90 N COUNTER | $\begin{aligned} & 01295 \\ & 07263 \\ & 01295 \\ & 01295 \\ & 01295 \end{aligned}$ | SN7400N 93L22DC SN74H11N SN7402N SN7490N |
| $\begin{aligned} & A 1 A 3 U 21 \\ & A 1 A 3 U 22 \\ & A 1 A 3 U 23 \\ & A 1 A B U 24 \\ & A 1 A 3 U \\ & A 1 A 3 U 25 \end{aligned}$ | $\begin{array}{\|l} 1820-0661 \\ 1820-0372 \\ 1820-0661 \\ 1820-0174 \\ 1820-0511 \end{array}$ |  | IC DGTL SN74 32 N GATE  <br> IC DGTL SN74H 11 N GATE  <br> IC OGTL SN74 32 N GATE  <br> IC DGTL SN74 04 N INVERTER <br> IC OGTL SN74 08 N GATE  | $\left\lvert\, \begin{array}{ll} 01295 \\ 01 & 295 \\ 01 & 295 \\ 01 & 295 \\ 01 & 295 \end{array}\right.$ | SN7432N <br> SN74H11N <br> SN7432N <br> SN7404N <br> SN7408V |
| $\begin{aligned} & \text { A } 1 A 3 U 26 \\ & \text { A } 1 A 3 U 27 \\ & \text { A } 1 A 3 U 28 \\ & \text { A } 1 A 3 U 29 \\ & A 1 A 3 U 30 \end{aligned}$ | $\begin{aligned} & 1820-0258 \\ & 1820-0659 \\ & 1820-0903 \\ & 1820-0065 \\ & 1820-0054 \end{aligned}$ | 8 | IC DGTL MC 858P BUFFER <br> IC DGTL REGISTER <br> IC DGTL SN74L 164 N REGISTER <br> IC DGTL SN74 70 N FLIP-FLOP <br> IC DGTL SN74 00 N GATE | $\begin{aligned} & 04713 \\ & 07263 \\ & 01295 \\ & 01295 \\ & 01295 \end{aligned}$ | MC858P <br> 93L OODC <br> SN74L164N <br> SN7470V <br> SN7400N |
| A1A3031 <br> A1A3U32 <br> A1A3U33 <br> A1A3U34 <br> A1A3U35 | $\begin{aligned} & 1820-0174 \\ & 1820-0511 \\ & 1820-0069 \\ & 1820-0054 \\ & 1820-0068 \end{aligned}$ | 12 | IC OGTL SN74 04 N INVERTER <br> IC OGTL SN74 OB N GATE <br> IC DGTL SN74 20 N GATE <br> IC DGTL SN74 00 N GATE <br> IC DGTL SN74 10 N GATF | 01295 01295 01295 01295 01295 | SN7404N <br> SN7408N <br> SN7420N <br> SN7400V <br> SN7410N |
| $\begin{aligned} & A 1 A 3 U 36 \\ & A 1 A 3 U 37 \\ & A 1 A 3 U 38 \\ & A 1 A 3 U 39 \end{aligned}$ | $\begin{aligned} & 1820-0903 \\ & 1820-0903 \\ & 1820-0903 \\ & 1820-0659 \end{aligned}$ |  | IC DGTL SNT4L 164 N REGISTER IC DGTL SN74L 164 N REGISTER IC DGTL SN74L 164 N PEGISTER IC DGTL REGISTER | $\begin{aligned} & 01295 \\ & 01295 \\ & 01295 \\ & 07263 \end{aligned}$ | SN74L154N SN74L164N SN74L $164 N$ 93L ODD: |
| A1A4 | 08660-60197 | 1 | BOARD ASSY, ROM INPUT | 28480 | 08660-60197 |
| A1A4C1 <br> A1A4C2 <br> A1A 4C 3 <br> A1A4C4 <br> A1A 4C5 | $\left\lvert\, \begin{aligned} & 0180-0197 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 180-0180-0197 \\ & 0 \end{aligned} 180-0197\right.$ |  | CAPACITMR-FXD; 2.2UF+-10\% 20VDC TA CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA CAPACITOR-FXD: 2.2UF+-10\% 2OVDC TA CAPACITDR-FXD; 2.2UF+-10\% 20VDC TA | $\begin{aligned} & 56289 \\ & 56289 \\ & 56289 \\ & 56289 \\ & 56289 \end{aligned}$ | $1500225 \times 902042$ $1500225 \times 902042$ $1500225 \times 902042$ $1500225 \times 902042$ $1500225 \times 902042$ |
| A1A4CR1 | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A1A4DS1 <br> A1A4DS2 <br> A1A40S3 <br> A1A40S4 <br> A1A4DS5 | $\begin{aligned} & 1990-0326 \\ & 1990-0326 \\ & 1990-0326 \\ & 1990-0326 \\ & 1990-0326 \end{aligned}$ | 7 | PHOTO-DEVICE; SW PNP-SI $3 V$ $.05 M W$ PD <br> PHOTO-DEVICE; SW PNP-SI $3 V$ $.05 M W$ PD <br> PHOTO-DEVICE; SH PNP-SI $3 V$ $.05 M H$ PD <br> PHOTO-DEVICE; SW PNP-SI $3 V$ $.05 M W$ PD <br> PHOTO-DEVICE; SW PNP-SI $3 V$ $.05 M W$ PD | $\begin{array}{\|l} 28480 \\ 28480 \\ 28480 \\ 28480 \\ 28480 \end{array}$ | $\begin{aligned} & 1990-0326 \\ & 1990-0326 \\ & 1990-0326 \\ & 1990-0326 \\ & 1990-0326 \end{aligned}$ |
| $\begin{aligned} & A 1 A 4 D S 6 \\ & \text { A1A40S7 } \end{aligned}$ | $\begin{aligned} & 1990-0326 \\ & 1990-0326 \end{aligned}$ |  | PHOTO-DEVICE; SW PNP-SI 3V .O5MW PD PHOTO-DEVICE; SW PNP-SI 3V .O5MW PD | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 1990-0326 \\ & 1990-0326 \end{aligned}\right.$ |
| $\begin{aligned} & A 1 A 4 R 1 \\ & A 1 A 4 R 2 \\ & A 1 A 4 R 3 \\ & A 1 A 4 R 4 \\ & A 1 A 4 R 5 \end{aligned}$ | $\begin{aligned} & 0698-3153 \\ & 0698-3445 \\ & 0698-3153 \\ & 0698-3153 \\ & 0698-3153 \end{aligned}$ | $\begin{aligned} & 17 \\ & 34 \end{aligned}$ | RESISTOR 3.83K 1\% . 125 W F TUBULAR RESISTOR 348 OHM $1 \%$. 125 W F TUBULAR RESISTOR 3.83K 1\% . 125 W F TUBULAR RESISTOR 3.83K 1\% .125W F TUBULAR RESISTOR 3.83K 1\% . 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / B-T 0-3831-F \\ & C 4-1 / 8-T 0-348 R-F \\ & C 4-1 / 8-T 0-3831-F \\ & C 4-1 / 8-T 0-3831-F \\ & C 4-1 / 8-T 0-3831-F \end{aligned}$ |
| A1A4R 6 <br> A1A4R7 <br> A1A4R 8 <br> A1A4R9 <br> A 1 A4R10 | $\begin{aligned} & 0698-3445 \\ & 0698-3153 \\ & 0698-3445 \\ & 0698-3153 \\ & 0698-3445 \end{aligned}$ |  | RESISTOR 348 OHM 1 \% . 125 W F TUBULAR RESISTOR 3.83K 1\% . 125 W F TUBIJLAR RESISTOR 342 DHM 1\%. 125 W F TUBULAR RESISTOR 3.83K 1\% . 125 W F TUQULAR RESISTOR 348 OHM 1 . 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 18209 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T O-348 R-F \\ & C 4-1 / 8-T O-3831-F \\ & C 4-1 / 8-T 0-348 R-F \\ & C 4-1 / 8-T 0-3831-F \\ & C 4-1 / 8-T 0-348 R-F \end{aligned}$ |
| A1A4P11 <br> $\triangle 1 A 4 R 12$ <br> A1A4R13 <br> A 144 R 14 <br> A1A4P15 | $\begin{aligned} & 0698-3153 \\ & 0698-3445 \\ & 0698-3153 \\ & 0698-3445 \\ & 0698-3153 \end{aligned}$ |  | RESISTOR 3.83K 1\% . 125 W F TUBULAR RESISTOR 348 OHM 18 . 125 W F TUBULAR RESISTOR 3.83K 1\% . 125 W F TUBULAR RFSISTOR 348 OHM $1 \%$. 125 W F TUBULAR RESISTOR 3.83K 1\% . 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-3831-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-348 \mathrm{~F}-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-3831-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-348 \mathrm{R}-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-3831-\mathrm{F} \end{aligned}$ |
| $\begin{aligned} & \triangle 1 A 4 R 16 \\ & A 1 A K R 17 \\ & A 1 A 4 Q 18 \end{aligned}$ | $\begin{aligned} & 0698-3445 \\ & 0698-3153 \\ & 0698-3445 \end{aligned}$ |  | RESISTOR 348 OHM 1 : . 125W F TUBULAR RESTSTOR 3.83K 1\% . 125 W F TUBULAR RFSISTOR 348 OHM 1\%.125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 16209 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-348 R-F \\ & C .4-1 / 8-T 0-3831-F \\ & C 4-1 / 8-T 0-349 R-F \end{aligned}\right.$ |
| A144S 1 | 3101-0137 | 4 | SWITCH-SENS SPDT SURMIN . 5 A 28 VDCC | 91929 | 1581-T |
| $\begin{aligned} & \triangle 1 A 4^{T} P 1 \\ & A 1 A T_{1} P 2 \\ & \triangle 1 A T T P 3 \\ & A 1 A 4 T P 4 \\ & A 1 A 4 T P 5 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0 & 360-1514 \\ 0 & 360-1514 \\ 0 & 360-1514 \\ 0 & 360-1514 \\ 0 & 360-1514 \end{array}\right.$ |  | TERMINAL: SLDR STUD <br> TERMINAL; SLDR STUD <br> TERMINAL: SLDR STUD <br> TERMINAL: SLDR STUD <br> TERMINAL; SLOR STUD | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0360-1514 \\ & 0360-1514 \\ & 0360-1514 \\ & 0360-1514 \\ & 0360-1514 \end{aligned}$ |
| $\begin{aligned} & A 1 A 4 T P 6 \\ & A 1 A 4 T P 7 \\ & A 1 A 4 T P B \\ & \triangle 1 A 4 T P Q \\ & A 1 A 4 T P 10 \end{aligned}$ | $\begin{aligned} & 0360-1514 \\ & 0360-1514 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 360-1514 \\ & 0 \\ & 0 \end{aligned} 360-1514$ |  | TERMINAL; SLDR STUD <br> TERMINAL: SLDR STUD <br> TERMINAL: SLDR STUD <br> TERMINAL; SLDR STUD <br> TERMINAL; SLDR STUO | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0360-1514 \\ & 0360-1514 \\ & 0360-1514 \\ & 0360-1514 \\ & 0360-1514 \end{aligned}$ |
| $\begin{aligned} & A 1 A 4111 \\ & A 1 \Delta 4 U 2 \\ & A 1 A 4113 \\ & A 1 A 4114 \\ & A 1 \Delta 4115 \end{aligned}$ | $\begin{aligned} & 1820-0070 \\ & 1820-0511 \\ & 1820-0174 \\ & 1820-0076 \\ & 1820-0076 \end{aligned}$ | 5 4 | IC DGTL SN74 30 N GATE <br> IC OGTL SN74 08 N GATE <br> IC OGTL SN74 04 N INVERTER <br> IC DGTL SN74 76 N FLIP-FLDO <br> IC DGTL SN74 76 N FLIP-FLOD | 01295 <br> 01295 <br> 01275 <br> 01295 <br> 01295 | SN7430N <br> SN7408V <br> SN7404N <br> SN7476N <br> SN7476V |

Table 6-3. Replaceable Parts


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| Reference <br> Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1ABR6 A1ABR A1A BR 8 $A$ $A 1 A B R 9$ $A 1 A B R 10$ | $0757-0472$ $0698-6248$ $0698-6248$ $0757-0439$ $0698-7090$ | 6 3 12 1 | RESISTOR 200 K 18 $\cdot 125 \mathrm{~W}$ F TUBULAR <br> RESISTOR 400 K 18 $\cdot 125 \mathrm{~W}$ TUBULAR <br> RESISTOR 400 K 18 $\cdot 125 \mathrm{~F}$ FUBULAR <br> RESISTOR 6.81 K 18 .125 W F TUBULAR <br> RESISTOR 4.5 K 18 .125 F TUBULAR | $\begin{aligned} & 24546 \\ & 19701 \\ & 19701 \\ & 24546 \\ & 19701 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-T0-2003-F } \\ & \text { MF4C1/8-T0-4003-F } \\ & \text { MF4C1/8-T0-4003-F } \\ & \text { C4-1/8-T0-8811-F } \\ & \text { MF4C1/8-T0-4502-F } \end{aligned}$ |
| A 1A BR II <br> A1ABR12 <br> A 1A BR 13 <br> A1A BR 14 <br> A IA BR 15 | $\begin{aligned} & 2100-3122 \\ & 0698-6248 \\ & 0757-0420 \\ & 0757-0274 \\ & 0757-0442 \end{aligned}$ | 4 9 8 105 | RESISTOR; VAR; TRMR; 100 DHM 10\% C RESISTOR 400K 1\% - 125W F TUBIULAR RESISTOR 750 OHM 1\% . 125W F TUBULAR RESISTOR 1.21K 1\% .125W F TUBULAR RESISTOR 10K 1\% . 125 W F TUBULAR | $\begin{aligned} & 32997 \\ & 19701 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & 3006 Y-1-101 \\ & \text { MF4C1/8-TO-4003-F } \\ & C 4-1 / 8-T 0-751-F \\ & C 4-1 / 8-T 0-1213-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |
| A 1A BR 16 <br> A AABR17 <br> A A A BR 18 <br> A 1A BR 19 <br> A1A8R 20 | $\begin{aligned} & 0757-0449 \\ & 0698-4008 \\ & 0698-3201 \\ & 0757-0280 \\ & 0698-3154 \end{aligned}$ | 3 1 1 | RESISTOR 20K 18 . 125 F F TUBULAR RESISTOR 40K 1\% . 125 F F TUBULAR RESISTOR 80K 18 . 125 W F TUBULAR RESISTOR 1K 1\% . 125W F TUBULAR RESISTOR 4.22K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 16299 \\ & 24548 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-2002-F \\ & C 4-1 / 8-T 0-4002-F \\ & C 4-1 / 8-T 0-8002-F \\ & C 4-1 / 8-T 0-1001-F \\ & C 4-1 / 8-T 0-4221-F \end{aligned}$ |
| A 1A8R 21 <br> A1A8R 22 <br> A 1A 8R 23 <br> A1A8R 24 <br> A1A 8R 25 | $\begin{aligned} & 0757-0422 \\ & 0757-0283 \\ & 0698-5808 \\ & 0698-3200 \\ & 0757-0420 \end{aligned}$ | 2 1 1 1 | RESI STOR 909 DHM 1\% . $125 W$ F TUBULAR RESISTOR 2K 1\% •125M F TUBULAR RESISTOR 4K 1\% . 125W F TUBULAR RESISTIR 8K 1\% . 125W F TUBULAR RESI STOR 750 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-909 R-F \\ & C 4-1 / 8-T 0-2001-F \\ & C 4-1 / 8-T 0-4001-F \\ & C 4-1 / 8-T 0-8001-F \\ & C 4-1 / 8-T 0-751-F \end{aligned}$ |
| A 1A 8R 26 A1A8R27 A1A8R28 A1A8R29 A1A8R 30 | $\left\lvert\, \begin{aligned} & 0698-3154 \\ & 0698-3154 \\ & 2100-3122 \\ & 2100-3122 \\ & 2100-3122 \end{aligned}\right.$ |  | RESI STOR 4.22K 18.125 W F TUBULAR RESISTOR 4.22K $1 \% .125 \mathrm{H}$ F TUBULAR RESISTOR; VAR; TRMR: 100 CHM $10 \%$ C RESISTOR: VAR; TRMR: 100 DHM 10\% C RESISTOR: VAR; TRMR; 100 DHM $10 \%$ C | $\begin{aligned} & 16299 \\ & 16299 \\ & 32997 \\ & 32997 \\ & 32997 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-4221-F \\ & C 4-1 / 8-T 0-4221-F \\ & 3008 Y-1-101 \\ & 300 \mathrm{BY}-1-101 \\ & 3006 Y-1-101 \end{aligned}$ |
| A AABU1 <br> A IABU2 <br> A 14 BU3 <br> A1ABU4 <br> A1A8U5 | $\begin{aligned} & 1826-0013 \\ & 1820-0583 \\ & 1820-0583 \\ & 1820-0070 \\ & 1820-0546 \end{aligned}$ | 1 3 | IC LIN AMPLIFIER <br> IC DGTL DM74L OON GATE <br> IC DGTL DM74L OON GATE <br> IC DGTL SN74 30 N GATE <br> IC DGTL SN74 192 N COUNTER | $\begin{aligned} & 28480 \\ & 27014 \\ & 27014 \\ & 01295 \\ & 01295 \end{aligned}$ | $\begin{aligned} & 1826-0013 \\ & \text { DM74LOON } \\ & \text { OM74LCON } \\ & \text { SN743ON } \\ & \text { SN74192N } \end{aligned}$ |
| A1A8U6 <br> A 1 A $8 U 7$ <br> AlA BUB <br> AlA 8 U 9 <br> A1A8U10 | $\begin{aligned} & 1820-0068 \\ & 1820-0577 \\ & 1820-0546 \\ & 1820-0328 \\ & 1820-0546 \end{aligned}$ | 3 | IC OGTL SN74 10 N GATE <br> IC OGTL SN74 16 N <br> INVERTER     <br> IC OGTL SN74 192 N COUNTER <br> IC DGTL SN74 02 N GATE <br> IC DGTL SN74 192 N COUNTER | $\begin{aligned} & 01295 \\ & 01295 \\ & 01295 \\ & 01295 \\ & 01295 \end{aligned}$ | SNT410N <br> SN7416N <br> SN74192N <br> SN7402N <br> SN74192N |
| A148U11 <br> Alabul2 <br> A1A8U13 | $\begin{aligned} & 1820-0577 \\ & 1820-0328 \\ & 1820-0577 \end{aligned}$ |  | IC DGTL SN74 16 N INVERTER <br> IC DGTL SN74 02 N GATE  <br> IC DGTL SN74 16 N INVERTER | $\begin{aligned} & 01295 \\ & 01295 \\ & 01205 \end{aligned}$ | $\begin{aligned} & \text { SN7416N } \\ & \text { SN7402N } \\ & \text { SN7416 } \end{aligned}$ |
| A1A9 | 08660-60199 | 1 | BOARD ASSY, REGISTER "A" | 28480 | 08660-60199 |
| $\begin{aligned} & A 1 A 9 C 1 \\ & A 1 A S C 2 \\ & A 1 A G C 3 \\ & A 1 A C C 4 \end{aligned}$ | $\begin{array}{lll} 0 & 180-0197 \\ 0 & 180-0197 \\ 0 & 180-0197 \\ 0 & 180-0197 \end{array}$ |  | CAPACITOR-FXD; 2.2UF+=10\% 2OVDC TA CAPACITOR-FXD; 2.2UF+-10\% 2OVDC TA CAPACITOR-FXD; 2.2UF+-10\% 2OVDC TA CAPACITOR-FXD; 2.2UF+-10\% 2OVDC TA | $\begin{aligned} & 56289 \\ & 56289 \\ & 56289 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 1500225 \times 902042 \\ & 1500225 \times 902042 \\ & 1500225 \times 902042 \\ & 1500225 \times 902042 \end{aligned}$ |
|  | $\begin{aligned} & 1820-0709 \\ & 1820-0709 \\ & 1820-0659 \\ & 1820-0659 \\ & 1820-0659 \end{aligned}$ |  | IC DGTL REGISTER <br> IC OGTL REGISTER <br> IC OGTL REGISTER <br> IC DGTL REGISTER <br> IC DGTL REGISTER | $\begin{aligned} & 07263 \\ & 07263 \\ & 07263 \\ & 07263 \\ & 07263 \end{aligned}$ | $\begin{aligned} & 93 L 28 D C \\ & 93 L 2 B D E \\ & 93 L 000 C \\ & 93 L 000 C \\ & 93 L 000 \end{aligned}$ |
| $\begin{aligned} & \text { A } 1 \text { A } 9 U 6 \\ & \text { A } 1 \text { A } 9 U 7 \\ & \text { A } 1 \text { A } 9 \cup 8 \\ & \text { A } 1 \text { A } 9 U 9 \\ & \text { A } 149 U 10 \end{aligned}$ | $\begin{aligned} & 1820-0659 \\ & 1820-0659 \\ & 1820-0710 \\ & 1820-0305 \\ & 1820-0054 \end{aligned}$ |  |  | $\begin{aligned} & 07263 \\ & 07263 \\ & 07263 \\ & 01295 \\ & 01295 \end{aligned}$ | $\begin{aligned} & 93 L 000: \\ & 93 L 000 \\ & 93 L 220= \\ & \text { SN7483N } \\ & \text { SN7400V } \end{aligned}$ |
|  | $\begin{aligned} & 1820-0372 \\ & 1820-0372 \\ & 1820-0054 \\ & 1820-0054 \\ & 1820-0054 \end{aligned}$ |  | IC DGTL SN74H 11 N GATE IC DGTL SN74H 11 N GATE IC OGTL SNT4 00 N GATF IC DGTL SN74 00 N GATE IC DGTL SN74 00 N GATE | $\begin{array}{ll} 01295 \\ 01295 \\ 01295 \\ 01295 \\ 01295 \end{array}$ | $\begin{aligned} & \text { SN74H11N } \\ & \text { SN74H1IN } \\ & \text { SN7400N } \\ & \text { SN7400V } \\ & \text { SN7400V } \end{aligned}$ |
| A 1 a 9016 | 1820-0174 |  | IC OGTL SNT4 04 N INVFRTER | 01295 | SN7404V |
| A 1 A 10 | 08660-60128 | 1 | BOARD ASSY, OUTPUT REGISTER | 28480 | 08660-60128 |
| A1A10C1 A1A10C2 A1A10C3 | $\left\lvert\, \begin{array}{lll} 0 & 180-0197 \\ 0 & 140-0196 \\ 0 & 180-0197 \end{array}\right.$ |  | CAPACITIR-FXD; 2.2UF+-10\% 20VOC TA CAPACITOP-FXD 150PF +-5\% 300WVDC MICA CAPARITOR-FXD; 2.2UF+-10\% 20VDC TA | 56289 72136 56289 | $1501225 \times 902042$ DM15F151J0300WV1CR $1500225 \times 902042$ |
| $\begin{aligned} & \text { A IA IOR } 1 \\ & \text { A IA IOR } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-0082 \\ & 0698-0082 \end{aligned}\right.$ |  | RESISTOR 464 OHM 1\% . 125 W F TUBULAR RESISTIR 464 OHM 1\% . 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-4640-F \\ & C 4-1 / 8-50-4640-F \end{aligned}\right.$ |
| $\begin{aligned} & \text { A } 1 \text { A } 10 U 1 \\ & \text { A } 1 A 10 U 2 \\ & \text { A } 1 A 10 U 3 \\ & A 1 A 10 U 4 \\ & A 1 A 1 O U 5 \end{aligned}$ | $\begin{aligned} & 1820-0627 \\ & 1820-0535 \\ & 1820-0054 \\ & 1820-0614 \\ & 1820-0614 \end{aligned}$ | 1 1 5 | IC DGTL DFCODER <br> IC DGTL SN75 451BP DRIVER <br> IC DGTL SN74 00 N GATE <br> IC DGTL LATCH <br> IC OGTL LATCH | $\begin{aligned} & 07263 \\ & 01295 \\ & 01295 \\ & 07263 \\ & 07263 \end{aligned}$ | 93LOID: <br> SN75451 BP <br> SN7400N <br> 931080 <br> 93L 03D |
| $\begin{aligned} & \text { A } 1 \text { A } 10 U 6 \\ & \text { A A } 10 U 7 \\ & \text { A } 1 \text { A } 10 U B \end{aligned}$ | $\begin{aligned} & 1820-0614 \\ & 1820-0614 \\ & 1820-0614 \end{aligned}$ |  | IC DGTL LATCH IC OGTL LATCH IC DGTL LATCH | $\begin{aligned} & 07263 \\ & 07263 \\ & 07263 \end{aligned}$ | $\begin{aligned} & 93 \mathrm{~L} 0805 \\ & 93 \mathrm{~L} 0805 \\ & 93 \mathrm{~L} 080 \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Alall | 08660-60257 | 1 | BOARD ASSY, INTERCONNECT | 28480 | 08660-60257 |
| $\left\lvert\, \begin{array}{ll} A & 1 A 11 C 1 \\ \text { A } 1 A 11 C 2 \end{array}\right.$ | $\left\lvert\, \begin{aligned} & 0160-3452 \\ & 0 \\ & 0 \end{aligned} 160-3879\right.$ | 1 | CAPAC.ITOR-FXD . O2UF +-20\% 100WVDC CER CAPACITDR-FXD .OIUF +-20\% 100WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0160-3452 \\ & 0160-3879 \end{aligned}\right.$ |
| Alallc3 | 0 160-3879 |  | CAPACITOR-FXD . 01 LUF +-20\% 100WVDC CER | 28480 | 0160-3879 |
| Alalljl | 1200-0507 |  | SOCKET; ELEC; IC 16 -CONT DIP SLDR TERM | 06776 | ICN-163-53W |
| A1A11J2 | 1200-0507 |  | SOCKET; ELEC; It 16-CONT DIP SLDR TERM | 06776 | ICN-163-53H |
| Alall J3 | 12000-0507 |  | SOCKET; ELEC; IC 16-CONT DIP SLDR TERM | 06776 | $1 \mathrm{ICN-163-53W}$ |
| A1A11 J4 | 1250-1255 | 7 | CONNECTOR-RF SMB M PC | 98291 24995 | 51-051-0000 |
| A1A11J5 | 1251-2361 | 3 | CONTACT, CONN, U/W POST TYPE SER, MALE | 24995 | 86091-2 |
| A1A11J6 | 1251-2361 |  | CONTACT, CONN, U/h Post type ser, male | 24995 | 86091-2 |
| A1A11TP1 | 0360-1514 |  | TERMINAL; SLDR STUD' | 28480 | 0360-1514 |
| $\text { A } 1 A 11 X A 1-1$ <br> A1A11XA1-2 | $1251-2035$ $1251-2026$ | 33 10 | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER CONNECTOR; PC EDGE; 18-CONT; DIP SOLDER | $\begin{aligned} & 71785 \\ & 71785 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 252-15-30-300 \\ & 252-18-30-300 \end{aligned}\right.$ |
| A1A11XA2-1 | $1251-2035$ |  | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 | 25-15-30-300 |
| A1A11XA2-2 | 1251-2026 |  | CONNECTOR; PC EDGE; 18-CONT; DIP SOLDER | 71785 | 252-18-30-300 |
| A1A11XA3-1 | 1251-2035 |  | CONNECTOR: PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A 1 A $11 \times$ X 3-2 | 1251-2026 |  | CONNFCTOR: PC EDGE; 18-CONT; DIP SOLDER CONNECTDR; PC EDGE; $15-C O N T ; ~ D I P ~ S O L D R R ~$ | 71785 71785 | $\begin{aligned} & 252-18-30-300 \\ & 252-15-30-300 \end{aligned}$ |
| A1A11XA $4-1$ | $1251-2035$ $1251-2026$ |  | CONNECTDR; PC EDGE; $15-C O N T ; ~ D I P ~ S O L D E R ~$ CONNECTOR; PC EDGE; 18-CONT; DIP SOLDER | 71785 71785 77785 | $\begin{aligned} & 252-15-30-300 \\ & 252-18-30-300 \\ & 2520 \end{aligned}$ |
| A1A11 XA5-1 | 1251-2035 |  | CONNFCTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| Alallxas-2 | 1251-2026 |  | CONNECTOR; PC EDGE; 18-CONT; DIP SOLDER | 71785 | 252-1 8-30-300 |
| A1A11XA6-1 | 1251-2035 |  | CONNECTOR: PC EDGE ; 15-CONT; DIP SOLDER | 71785 71785 | 252-15-30-300 |
|  | $1251-2026$ $1251-2035$ |  | CONNECTOR; PC EDGE; 18-CONT; DIP SOLDER CONNECTIR: PC EDGE; 15-CDNT; DIP SOLDER | 71785 71785 | $\left\lvert\, \begin{aligned} & 252-18-30-300 \\ & 252-15-30-300 \end{aligned}\right.$ |
| A 1 A11 $\times 47-2$ | 1251-2026 |  | CONNECTOR; PC EDGE; 13-CONT; DIP SOLDER | 71785 | 252-18-30-300 |
|  | 1251-2035 |  | CONNECTOR: PC EDGE; 15-CONT; OIP SOLDER | 71785 | 252-15-30-300 |
| A 1 Al1 1 PA $8-2$ | 1251-2026 |  | CONNECTOR: PC EDGE: 1B-CONT; OIP SOLDER | 71785 | 252-18-30-300 |
| A1A11XA9-1 | 1251-2035 |  | CONNECTOR; PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| AlAll A $1411 \times A 9-2$ | $1251-2026$ $1251-2035$ |  | CONNECTOR; PC EDGE; $18-C O N T ; ~ D I P ~ S O L D E R ~$ CONNECTOR: PC EDGE: $15-C O N T ;$ DIP SOLDER | 71785 71785 7775 | 252-18-30-300 |
| A 1 A11 Xal0 | 1251-2026 |  | CONNECTOR; PC EDGE; 18-CONT; DIP SOLDER | 71785 | 252-18-30-300 |
| A 1412 | 08660-60190 | 1 | biard assy, numeric readdut | 28480 | 08660-60190 |
| A1A12Cl A1A12C2 | $\begin{aligned} & 0180-0228 \\ & 0180-1714 \end{aligned}$ | 16 | CAPACITDR-FXD; 22UF+-10\% 15VDC TA-SOLID CAPACITOR-FXD; 330UF + -10\% GVDC TA-SOLID | $\left\lvert\, \begin{aligned} & 56289 \\ & 56289 \end{aligned}\right.$ | $\begin{aligned} & 1500226 \times 901582 \\ & 1500337 \times 900652 \end{aligned}$ |
| A1A12C3 | 0160-2055 | 152 | CAPACITOR-FXD . $014 \mathrm{~F}+80-20 \%$ 100WVOC CER | 28480 | 0160-2055 |
| A1A12C4 | -160-2055 |  | CAPACITOR-EXD . $01 \mathrm{UF}+80-20 \% 100 \mathrm{WVDC}$ CER | 28480 | 0160-2055 |
| AlAl20S 1 A1A12ns | $2140-0356$ | 4 | LAMP; INCAND BULB TI; 5 V LAMP; INCAND BULB TI; | 71744 71744 | $\begin{aligned} & \text { CM7-76B3 } \\ & \text { CM7-76B3 } \end{aligned}$ |
| A1412ns2 A1A120S | 2140-0356 |  | LAMP ; INCAND BULB TI; 5V | 71744 | CM7-76B3 |
| AlA120S 4 | 2140-0356 |  | LAMP; INCAND BULB TI; 5V | 71744 | CM7-76B3 |
| A1412J1 | 1200-0507 |  | SOCKET: ELEC: IC 16-CONT DIP SLOR TERM | 06776 | ICN-163-S3W |
| A1A12J2 | 1200-0507 |  | SOCKET; FLEC; IC 16-CONT DIP SLDR TERM | 06776 | ICN-163-S3H |
| 4141201 | 1854-0492 | 20 | TRANSISTIDR NPN SI PD $=350 \mathrm{MH}$ FT $=2504 \mathrm{HZ}$ | 28480 | 1854-0492 |
| A141202 | 1854-0492 |  | TPANSISTER NPN SI PD=350MH FT $=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| Alall 1203 | 1854-0492 |  | TRANSISTOR NDN SI PD $=350 \mathrm{MW}$ FT $=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A1A1204 | 1854-0492 |  | TRANSTSTOR NPN SI PD $=350 \mathrm{MH} \quad \mathrm{FT}=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A141205 | 1854-0492 |  | TRANSISTOR NPN SI PD $=350 \mathrm{MH} \mathrm{FT}=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A14 1206 A1A 1207 | $\begin{aligned} & 1854-0492 \\ & 1854-0492 \end{aligned}$ |  | TRANSISTOR NPN SI PD $=350 \mathrm{MW} \quad \mathrm{FT}=250 \mathrm{MHZ}$ TRANSISTOR NPN SI PD $=350 \mathrm{MW} \quad \mathrm{FT}=250 \mathrm{MHZ}$ | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0492 \\ & 1854-0492 \end{aligned}$ |
| A1A1208 | 1854 -0492 |  | TRANSISTOR NPN SI Pn=350MH FT $=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A 141209 | 1854-0492 |  | TRANSISTDR NPN SI PD=350MH FT $=250 \mathrm{MHZ}$ | 28430 | 1854-049? |
| A1A12010 | 1854-0492 |  | TRANSISTOR NPN SI PD $=350 \mathrm{MH}$ FT $=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| $\text { A } 1412011$ $\text { A1A } 12012$ | $\begin{aligned} & 1854-0492 \\ & 1854-0492 \end{aligned}$ |  | TRANSISTOR NPN SI PD=350MI FT $=250 \mathrm{MHZ}$ TRANSISTIR NPN SI PD $=350 \mathrm{MH} \quad \mathrm{FT}=250 \mathrm{MHZ}$ | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0492 \\ & 1854-0492 \end{aligned}$ |
| A1A 12013 | 1854-0492 |  | TRANSISTOR NPN SI PD $=350 \mathrm{MH} \quad \mathrm{FT}=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A 1412014 | 1854-0492 |  | TRANSISTTR NPN $S$ I PD $=350 \mathrm{MH} \mathrm{FT}^{\top}=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A1A12015 | 1854-0492 |  | TQANSTSTIP NPN SI PD=350MH FT $=250 \mathrm{MHZ}$ | 28480 | 1954-0492 |
| $\begin{aligned} & A 1412016 \\ & A 1 A 12017 \end{aligned}$ | $\begin{aligned} & 1854-0492 \\ & 1854-0492 \end{aligned}$ |  | TRANSISTOR NPN SI PD $=350 \mathrm{MH} \quad \mathrm{FT}=250 \mathrm{MHZ}$ <br> TRANSISTOR NPN SI PD $=350 \mathrm{MW} \quad \mathrm{FT}=250 \mathrm{MHZ}$ | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0492 \\ & 1854-0492 \end{aligned}$ |
| A 1 A12018 | 1854-0492 |  | TRANSISTOR NPN SI PJ $=350 \mathrm{MW} \quad \mathrm{FT}=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A1412019 | 1854-0492 |  | TRANSISTOR NDN SI PD $=350 \mathrm{MH} \quad \mathrm{FT}=250 \mathrm{MHZ}$ | 29490 | 1854-0492 |
| A 1412020 | 1854-0492 |  | TRANSISTOR NPN SI Pn=350MH FT $=250 \mathrm{MHZ}$ | 28480 | 1854-0492 |
| A1A12R1 AIA12R2 | $\begin{aligned} & 0698-7208 \\ & 0698-7208 \end{aligned}$ | 4 | RESISTOR 63.1 OHM 2\%.05W F TUBILLAR RESISTOR 68.1 OHM 2\% .05W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 3-1 / 8-T 00-68 R 1-G \\ & \mathrm{C} 3-1 / 8-T 00-68 R 1-\mathrm{T} \end{aligned}$ |
| alalirs | 0698-7208 |  | RESISTIR 68.1 $1 \mathrm{HHM} 2 \% .05 \mathrm{~W}$ F TUBULAR | 24546 | C3-1/8-T00-6821-G |
| A1A12R4 | 0698-7208 |  | RESISTOR 68.1 OHM 2\%.05W F TUBULAP | 24546 | C3-1/8-T00-69R1-G |
| $\begin{aligned} & A 1 A 12 S 1 \\ & A 1 A 12 S 2 \end{aligned}$ | $\begin{array}{llll} 3 & 101-0137 \\ 3 & 101-0137 \end{array}$ |  | SWITCH-SENS SPDT SUBMIN .5A 28 VDC SWITCH-SENS SPDT SURMIN .5A $28 V D C$ | 91929 | $15 \times 1-T$ $15 \times 1-T$ |
| alal2s3 | 3101-0137 |  | SWITCH-SENS SPDT SUBMIN .5A 28VDr. | 91929 | 15x1-T |
| $\begin{array}{\|l} A 1 A 12 U 1 \\ \text { A1A12U? } \end{array}$ | $\left\lvert\, \begin{aligned} & 1820-0571 \\ & 1820-0571 \end{aligned}\right.$ | 2 | IC DGTL GENERATOR IC DGTL GENERATOR | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 1820-0571 \\ & 1820-0571 \end{aligned}\right.$ |
| A1A12U3 | 1990-0311 | 2 | DISPLAY NUM DOT MAT 6 CHAR . 273 IN HIGH | 28480 | 1990-0311 |
| 4181214 | 1990-0311 |  | DISPLAY NUM DOT MAT 6 CHAR . 273 IN HIGH | 28480 | 1990-0311 |
| A1A12U5 | 1820-1060 | 1 | IC DGTL SCANNER | 28480 | 1820-1060 |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1A12XU3 A1A12 XU4 | $\begin{aligned} & 1200-0481 \\ & 1200-0481 \\ & 1251-1556 \end{aligned}$ | 2 6 | SOCKET, ELEC, IC $36-C O N T$ DIP SLDR TERM SOCKET: ELEC, IC $36-C O N T ~ D I P ~ S L D R ~ T E R M ~$ CONNECTDR:1-CONT SKT. 04 DIA | $\begin{aligned} & 28480 \\ & 28480 \\ & 28490 \end{aligned}$ | $\begin{aligned} & 1200-0481 \\ & 1200-0481 \\ & 1251-1556 \end{aligned}$ |
| A1A13 | 08660-60159 | 1 | BOARD ASSY, ANNUNCIATOR BLOCK | 28480 | 08560-60159 |
| $\begin{aligned} & A 1 A 13 D S 1 \\ & A 1 A 130 S 2 \end{aligned}$ | 2140-0356 |  | LAMP ; INCAND: BULB $\mathrm{T} 1 ; 5 \mathrm{VV}$ LAMP; INCAND; BULB $\mathrm{T} 1 ; 5 \mathrm{~V}$ | 71744 71744 | $\begin{aligned} & \text { CM7-7593 } \\ & \text { CMT-7683 } \end{aligned}$ |
| A1A130S 3 | 2140-0356 |  | LAMP ; INCAND; BULB T1; 5V | 71744 | CM7-7693 |
| A1A130S 4 | 2140-0356 |  | LAMP ; INCAND; BULB T1; 5 V | 71744 | CM7-7683 |
| A1A13055 | 2140-0356 |  | LAMP: INCAND: BULB T1; 5V | 71744 | CM7-7683 |
| $\begin{aligned} & A 1 A 13 T P 1 \\ & A 1 A 13 T P 2 \end{aligned}$ | 0362-0063 | 6 |  | 91886 91886 | 122-0192-019 |
| A1A13TP3 | 0362-0063 |  | TERMINAL, CRP, QDISC FEM, 0.046 TAB, | 91886 | 122-0192-019 |
| A1A13TP4 | 0362-0063 |  | TERMINAL, CRP, ODISC FEM, 0.046 TAB, | 91886 | 122-0192-019 |
| A1A13TP5 | 0362-0063 |  | TERMINAL, CRP, QDISC FFM, 0.046 TAB, | 91886 | 122-0192-019 |
| AlAl3tP6 | 0362-0063 |  | TERMINAL, CRP, QDISC FEM, 0.046 TAB, | 91886 | 122-0192-019 |
| A1A13XA1 | 1251-1556 |  | CONNECTOR;1-CONT SKT . 04 OIA | 28480 | $1251-1558$ |
| AlA $13 \times A 2$ A1A13XA | 1251-1556 |  | CONNECTOR:1-CDNT SKT CONNECTOR: 04 STONT SKT | 28480 28480 | $\text { \| } \left\lvert\, \begin{aligned} & 1251-1556 \\ & 1251-1556 \end{aligned}\right.$ |
| A1A13xA4 | 1251-1556 |  | CONNECTOR;1-CONT SKT . 04 DIA | 28480 | 1251-1556 |
| A1A13XA5 | 1251-1556 |  | CONNECTOR;1-CONT SKT . 04 DIA | 28480 | 1251-1556 |
| A1A 14 | 08660-60114 | 1 | SWITCH ASSY, SWFEP | 28480 | 08660-60114 |
| A1A14.Jl | 1200-0507 |  | SOCKET: ELEC: IC 16-CONT DIP SLDR TERM | 06776 | ICN-163-53W |
| A1A15 | 08660-60113 | 1 | SWITCH ASSY, KEYBOARD | 28480 | 08660-60113 |
| A1A15J1 | 1200-0507 |  | SOCKET; ELEC; IC 16-CONT DIP SLOR TERM | 06776 | ICN-163-S3W |
|  |  |  | MISCELLANEOUS AlAL5. |  |  |
|  | 0570-0031 | 1 | SCREW-MACH 4-40 RD HD SLT REC NYL-BLK | 95987 | N-440-1/2 |
|  | 5040-0364 | , | UPPER CECK | 28480 | 5040-0364 |
|  | 5001-0109 | 1 | SPRING | 28480 | 5001-0109 |
|  | 5040-0365 | 1 | LDWER DECK FLIPPER | 28480 28480 | $\begin{aligned} & 5040-0365 \\ & 5040-0366 \end{aligned}$ |
|  | 5040-0367 | 1 | ACTUATDR | 28480 | 5040-0367 |
|  | 5040-6901 | 1 | KEY: DEC POINT | 28480 | 5040-6901 |
|  | 5040-6902 | 1 | KEY: NUMBER 1 | 28480 | 5040-6902 |
|  | 5040-6903 | 1 | KEY NUMBER 2 | 28480 |  |
|  | 5040-6904 | 1 | KEY NUMBER 3 | 28480 | $5040-6904$ |
|  | 5040-6905 | 1 | KEY NUMBER 4 | 28480 | 5040-6905 |
|  | 5040-6906 | 1 | KFY NUMRER 5 | 28480 | 5040-6906 |
|  | 5040-6907 | 1 | KEY NUMPER 6 | 28480 | 5040-6907 |
|  | 5040-6908 | 1 | KEY NUMBER 7 | 28480 | 5040-6908 |
|  | 5040-6909 | 1 | KEY NUMBER 8 | 28480 | 5040-6909 |
|  | 5040-6910 | 1 | KEY NUMBFR 9 | 28480 | 5040-6910 |
|  | 5040-6911 | 1 | KEY NUMBER 0 | 28480 | 5040-6911 |
|  | 5040-6912 | 1 | KEY: CLEAR KEYBDARD | 28480 | 5040-6912 |
|  | 5040-6913 | 1 | KEY: STFP UP | 28480 | 5040-6913 |
|  | 5040-6914 | 1 | KEY: STEP DOWN | 28480 | 5040-6914 |
|  | 5040-6915 | 1 | KFY: SHEEP WI DTH | 28480 | 5040-6015 |
|  | 5040-6916 | 1 | KEY: CONTRAL FREQUENCY | 28480 | 5040-6915 |
|  | 5040-6917 | 1 | KEY: HZ KEY: $M H Z$ | 28480 28480 | 5040-6917 |
|  | 5040-6919 | 1 | KEY: KHZ | 28480 | 5040-6919 |
|  | 5040-6920 | 1 | KEY: GHZ | 28480 | 5040-6920 |
| A1A16 | 08660-60115 | 1 | Shirch assy, manual mmde | 28480 | 08660-60115 |
| A1A16J1 | $\begin{aligned} & 1200-0507 \\ & 0330-0187 \end{aligned}$ | 1 | SOCKET: ELEC; IC 16-CONT DIP SLDR TERM INSULATOP, MYLAR $3^{\prime \prime} \mathrm{N} \times 4^{\text {n }}$ LG | $\begin{aligned} & 06776 \\ & 008^{\circ} M \end{aligned}$ | $\begin{aligned} & \text { ICN-163-S3W } \\ & \text { QRD } \end{aligned}$ |
| A1417 | 08860-60123 | 1 | TUNER ASSY, MANUAL MODE | 28480 | 08660-60123 |
| A 2 | 08660-60020 | 1 | BIARD ASSY, INTERCONNFCTITON | 28480 | 08660-50020 |
|  | $0160-3456$ | 30 | CAPACITOR-FXD $1000 \mathrm{PF}+-10 \% 1000 \mathrm{HVOC}$ CER |  |  |
| A 2 C. 2 <br> A 2 C <br> 1 | 0160-3456 |  | CAPACITAR-FXD 1000 PF +-10\% 1000 WVDC CER CAPACITOR-FXD $1000 \mathrm{PF}+-10 \% 1000 \mathrm{VDC}$ CER | 28480 28480 | $0150-3456$ $0160-3456$ |
| ${ }^{\text {A 2 C }} 4$ | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000 WVOC CER | 28480 | 0160-3456 |
| A 2 C 5 | 0160-3456 |  | CAPACITCR-FXD 1000 PF +-10\% 1000WVOC CER | 28480 | 0160-3455 |
| A2C6 | 0160-3456 |  | CAPACITOR-FXC 1000 PF +-109 1000WVDC CER | 28480 | 0160-3456 |
| A2C7 | 0160-3456 |  | CAPACITOR-FXD 1000PF +-10\% 1000WVIC CER | 28480 | 0160-3456 |
| A 2 C 8 | 0160-3458 |  | CAPACITOR-FXO 1000 PF +-10\% 1000 VVOC CER | 28480 | 0160-3456 |
| A 2 C 9 A 2 Cl 10 | -160-2055 |  | CAPACITDR-FXD .O1UF +B0-20\% 100WVDC CER CAPACITOR-FXD. . $1 \mathrm{LUF}+80-20 \%$ 100WVDC CFR | 28480 28480 | $\begin{aligned} & 0160-2055 \\ & 0160-2055 \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A2C11 | 0160-2055 |  | CAPACITOR-EXD .01UF +80-209 100WVDC CER | 28480 | 0160-2055 |
| A 2 C 12 | 0160-2055 |  | CAPACITDR-FXD .01UF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A 2 C .13 | 0160-3456 |  | CAPACITOR-FXD $1000 \mathrm{PFF}+-10 \% 100$ OWVDC CER | 28480 | 0160-3456 |
| A 2C 14 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 100 OWVDC CER | 28480 | 0160-3456 |
| A 2C 15 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000WVDC CER | 28480 | 0160-3456 |
| ${ }^{\text {A 2 } 2 C 16}$ | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000WVDC CER | 28480 | 10160-3456 |
| A 2 Cl 17 A 2 C 18 | -160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 100 OHVDC CER CAPACITOR-FXD 1000PF +-10\% CAPA | 28480 28480 | $\begin{aligned} & 0160-3456 \\ & 0160-3456 \end{aligned}$ |
| A 2C. 18 A 2 C .19 | O160-3456 |  |  | 28480 28480 | 0160-3456 $0160-3456$ |
| $\triangle 2 \mathrm{C} 20$ | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000HVDC CER | 28480 | 0160-34 56 |
| A 2 C 21 | 0160-2055 |  | CAPACITOR-FXD .01UF +80-208 10 OHVOC CER | 28480 | 0160-2055 |
| A C C 22 $A 2 C$ $A$ | 0160-2055 |  | CAPACITOR-FXO .O1UF +80-20\% 100WVDC CER | 28480 28480 | 0160-2055 |
| A 2 C 23 A 2 C 24 | 0160-2055 |  |  | 28480 28480 | 0160-2055 |
| A2C 25 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-108 1000 WVDC CER | 28480 | 0180-3456 |
| A 2 C 26 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000wVOC CER | 28480 | 0160-3456 |
| A 2 C 27 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 100 OWVDC CER | 28480 | 0160-3456 |
| A 2 C 28 | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| ${ }^{\text {A } 2 C 29}$ | 0160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A2C 30 | 0160-2055 |  | CAPACITOR-FXD .O1UF +80-20\% 100WVDC GER | 28480 | 0160-2055 |
| A 2 C 31 | 0160-2055 |  | CAPACITOR-FXO .O1UF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| ${ }^{\text {A } 2 C 32}$ | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000WVDC CER | 28480 | 0160-3456 |
| A $2 C 33$ A 2 C 34 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 100 OHVDC CER CAPACITOR-FXD 1000PF +-10\% 1000 HVDC CER | 28480 28480 | 10160-3456 |
| A2C 34 A $2 C 35$ | 0160-3456 $0160-3456$ |  | CAPACITOR-FXD 1000 PF +-10\% 1000 WVDC CER CAPACITOR-FXD 1000PF +-10\% 100 OWVOC CER | 28480 28480 | 10160-3456 |
| A 25. 36 | 0160-3456 |  | CAPACITOR-FXO 1000 PF +-10\% 1000WVDC CER | 28480 | 0160-3456 |
| A 2 C 37 | 0 160-3456 |  | CAPACITOR-FXD 1000PF +-10\% 100 OWVDC CER | 28480 | 0180-3456 |
| A 2C 38 | 0 160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000 WVDC CER | 28480 | 0160-3456 |
| 4.2C39 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000WVDC CER | 28480 | 0160-3456 |
| A2C40 | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 1000WVDC CER | 28480 | 0160-3456 |
| ${ }_{-} \mathrm{A} 2 \mathrm{C} 41$ | 0160-2055 |  | CAPACITOR-FXD . $01 U F+80-20 \%$ 100YVDC CER | 28480 | 0160-2055 |
| ${ }^{\text {A } 2 C 42}$ | 0160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A2C43 A2C44 | -160-2055 |  | CAPACITOR-FXD .O1UF +80-20\% 100WVDC CER CAPACITOR-FXD .OIUF +80-20\% 10OWVDC CER | 28480 28480 | $\left\lvert\, \begin{aligned} & 0160-2055 \\ & 0160-2055 \end{aligned}\right.$ |
| A 231 | 1250-1255 |  | CONNECTOR-RF SMB M PC | 98291 | 51-051-0000 |
| A 2.12 | 1250-1255 |  | CONNECTOR-RF SMB M PC | 98291 | 51-051-0000 |
| A 2.13 A 254 | 1250-1255 |  | CONNECTOR-RF SMB M PC CONNECTOR-RF SMB M PC | 98291 98291 | 51-051-0000 |
| A2W2 | 08660-60080 |  | CABLE ASSY, GRAY | 28480 | 08660-60080 |
| A2×A8-1 | 1251-2035 |  | CONNECTOR: PC EDGE; 15-EONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 888$ - 2 | 1251-2035 |  | CONNECTOR; PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A2XA9-1 | 1251-2035 |  | CONNECTOR: PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 410-1$ | 1251-2035 |  | CONNECTOR: PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 410-2$ | 1251-2035 |  | CONNECTOR; PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times A 11-1$ | 1251-2035 |  | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 71785 | $\left\lvert\, \begin{aligned} & 252-15-30-300 \\ & 252-15-30-300 \end{aligned}\right.$ |
| A $2 \times A 11-2$ $A 2 X A 12-1$ | $1251-2035$ $1251-2035$ |  | CONNECTOR; PC EDGE: $15-C O N T ; ~ D I P ~ S O L D E R ~$ CONNECTOR: PC EDGE; $15-C O N T ;$ DIP SOLDER | 71785 71785 | 252-15-30-300 |
| A $2 \times \Delta 12-2$ | $1251-2035$ |  | CONNECTOR; PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 413-1$ | 1251-2035 |  | CONNECTOR; PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times A 13-2$ | 1251-2035 |  | CONNECTOR: PC EDGE; 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 414-1$ | 1251-2035 |  | CONNECTOR: PC EDGE: 15-CDNT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 414-2$ | 1251-2035 |  | CONNECTOR; PC EOGE: 15-CONT: DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 415-1$ | 1251-2035 |  | CONNECTOR: PC EDGE; 15-CONT: DIP SOLDER | 71785 | 252-15-30-300 |
| A 2xal 5-2 | 1251-2035 |  | CONNECTOR; PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-300 |
| A $2 \times 416-1$ | 1251-2035 |  | CONNECTOP: PC FOGF: 15-CONT; DIP SOLDER | 71785 | $252-15-30-300$ |
| A $2 \times 416-2$ | 1251-2035 |  | CONNECTRR: PC EDGE; 15-CONT; DIP SOLDER | 71785 | $\left\lvert\, \begin{aligned} & 252-15-30-300 \\ & 252-15-30-300 \end{aligned}\right.$ |
| A $2 \times A 17-1$ A $2 \times A 17-2$ | $1251-2035$ $1251-2035$ |  | CONNFCTOR; PC EDGE; $15-C O N T ; ~ D I P ~ S O L D E R ~$ CONNECTOR: PC EDGE; $15-C O N T$; OIP SOLDER | 71785 | $252-15-30-300$ $252-15-30-300$ |
| A $2 \times A 17-2$ $A 2 \times A 18-1$ | $1251-2035$ $1251-2035$ |  | CONNECTOR: PC EDGE; $15-C O N T ; ~ O I P ~ S O L D E R ~$ CONNECTIR ${ }^{\text {P }}$ PC EDGE; 15-CONT; DIP SOLDER | 71785 71785 | 252-15-30-300 |
| A $2 \times 418-2$ | 1251-2035 |  | CINNECTOR: PC EDGE: 15-CONT: DIP SOLDER | 71785 | 252-15-30-300 |
| $\triangle 2 \times A 19-1$ | 1251-2035 |  | CONNECTOR: PC EDGF: 15-CONT: DIP SOLDER CONNECTOR: PC EDGE: 15-CONT: DID SOLDER | 71785 71785 | $\begin{aligned} & 252-15-30-300 \\ & 252-15-30-300 \end{aligned}$ |
| A 2xal 9-2 | 1251-2035 |  | CONNECTOR: PC EDGE: $15-C O N T$; DIP SOLDER | 71785 | $252-15-30-300$ |
| A3A 1 | 08660-60028 | 1 | BIARD ASSY, DIGITAL INTERFACE(FRONT) | 28480 | 08660-60028 |
| $\begin{aligned} & A 3 A 1 C l \\ & A 3 A 1 C ? \end{aligned}$ | $\begin{aligned} & 0160-0154 \\ & 0180-0197 \end{aligned}$ | 3 | CAPACITOR-FXD $2200 \mathrm{PF}+-10 \%$ 200WVOC POLYE CAPACITOR-FXD; 2.2UC+-10\% 20VDC TA | $\begin{aligned} & 56289 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 292 \mathrm{P} 22292 \\ & 1500225 \times 902042 \end{aligned}$ |
| A 3 A 1C. 3 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 902042$ |
| $4381 \mathrm{IC}_{4}$ | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 20VDC TA | 56289 | $1500225 \times 90204$ ? |
| A3A1C5 | 0180-1746 | 3 | CAPACITOR-FXD; 15UF+-10\% 20VOC TA-SOLID | 55289 | $1500156 \times 902082$ |
| A3A1C6 | 0180-0373 | 1 | CAPACITOR-FXD: .68UF+-10\% 35VDC TA | 56289 | $1500684 \times 903542$ |
| $\begin{aligned} & A 3 A 1 C R 1 \\ & A 3 A I C R 2 \end{aligned}$ | $\begin{aligned} & 1902-3059 \\ & 1901-0040 \end{aligned}$ | 1 | DIDDE-ZNR 3.83V 5\% DO=7 PD=.4W TC= DIDDF-SWITCHING 2NS 3OV 5OMA | $\begin{aligned} & 04713 \\ & 28480 \end{aligned}$ | $\begin{array}{ll} S Z & 10939-62 \\ 1901-0040 \end{array}$ |

Table 6-3. Replaceable Parts


Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A3A1 | 08660-60188 | 1 | BOARD ASSY, HD IB OUTPUT | 23480 | 08660-50188 |
| A3A1C1 | 0180-0373 | 1 | CAPACITOR-FXO; 6 68UF+-10\% 35VDC TA | 56289 | $1500634 \times 903542$ |
| A 3A 1C2 A 3A1C3 | 0180-1746 | 1 | CAPACITOR-FXD; $15 U \mathrm{~F}+-10 \%$ 20VDC TA-SOL ID CAPACITOR-FXD; $2.2 U \mathrm{~F}+-10 \%$ 20VDC TA | 55289 56289 | $1500156 \times 902082$ $1500225 \times 902042$ |
| A 3A1C3 A 3 1 1 C a | 0180-0197 | 6 | CAPACITOR-FXD; CAPACITOR-FXD; 2.2UF + - 2 -10\% 2OVDC | 56289 56239 | $1500225 \times 902042$ $1500225 \times 902042$ |
| A 3A1C5 | 0130-0197 |  | CAPACITOR-FXO; 2.2UF+-10\% 2OVDC TA | 56289 | $1500225 \times 902042$ |
| A3A1C6 | 0160-0301 | 1 | CAPACITOR-FXD . $012 \mathrm{UC}^{\text {+ }}$ - $10 \% 200 \mathrm{WVDC} \mathrm{POLYF}$ | 56289 | 292P12392 |
| A3A ICR1 | 1901-0040 | 1 | OIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A3A1CR2 | 1902-3059 | 1 | DIDDE-ZNR 3.83V 5\% no-7 PD=.4W TC= | 04713 | $\text { S2 } 10939-62$ |
| A 3 A1J1 A 3 1 1 J 2 | 1251-2194 | 2 | CONNECTOR:1-CONT SKT . 021 DIS <br> CONNECTRP;1-CONT SKT . 021 DIA | $\begin{aligned} & 00779 \\ & 00779 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 3-331272-0 \\ & 3-331272-0 \end{aligned}\right.$ |
| A 3A 101 | 1853-0020 | 1 | TRANSISTIR PNP SI CHIP PD=300MH | 28480 | 1853-0020 |
| A3A 102 | 1854-0071 | 1 | TRANSISTOR NPN SI PD $=300 \mathrm{MW}$ FT $=200 \mathrm{MHZ}$ | 28480 | 1854-0071 |
| A 3A1R1 $A 3 A 1 R 2$ | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0757-0442 \end{aligned}\right.$ | 4 |  | 24546 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / B-T O-1002-F \\ & C 4-1 / 8-T O-1002-F \end{aligned}\right.$ |
| A 3A 1R 3 | 0757-0442 |  | RESISTOR 10K 1\% -125W F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| A 3AIR 4 | 0757-0442 |  | RESISTOR 10K 1\% 1 -125W F TUBULAR | 24548 | C4-1/8-T0-1 002-F |
| A 3AIR 5 | 0757-0279 | 1 | RESISTOR $3.16 \mathrm{~K} 1 \%$.125 F F TUBULAR | 24546 | C4-1/8-T0-3161-F |
| A3AIRG | 0757-0394 | 1 | RESISTOR 51.1 DHM 1 19, 125 W F TUBULAR | 24546 24546 | $\mathrm{C} 4-1 / 8-\mathrm{TO}-5121-\mathrm{F}$ |
| A 3A1R 7 A 3 A1R 8 | 0698-7210 | 9 | RESISTOR RESISTOR 82.5 R | 24546 24546 | $\left\lvert\, \begin{aligned} & C 3-1 / 8-T 00-82 R 5-G \\ & C 3-1 / 8-T 00-82 R 5-G \end{aligned}\right.$ |
| A 3A1R9 | 0898-7210 |  | RESISTOR 82.5 OHM 2\% .05 F F TUBULAR | 24546 | C3-1/8-TOO-82R5-G |
| A 3A1R10 | 0698-7210 |  | RESISTOR 82.5 OHM 2\%.05W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A 3 A 1211 | 0698-7210 |  | RESISTOR 82.5 OHM 29.05 W F TJBBULAR | 24546 | C 3-1/8-T0 0-82R5-G |
| A 3 A1R12 $A 3 A 1 R 13$ | 0757-0278 | 1 | RESISTOR RESISTOR R | 24546 16299 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-1781-F \\ & C 4-1 / 8-T 0-33 R 3-F \end{aligned}\right.$ |
| $\begin{aligned} & A 3 A 1 R 13 \\ & \text { A } 3 A 1 R 14 \end{aligned}$ | $0698-3435$ $0898-7210$ | 1 | RESISTOR RESISTOR 88.3 R | 16299 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-33 R 3-F \\ & \text { C 3-1/8-T00-82R5-G } \end{aligned}\right.$ |
| A3A1R15 | 0698-7210 |  | RESISTOR 82.5 OHM 2\%.05W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A3A1R16 | 0698-7210 |  | RESISTOR 82.5 OHM 2\%.05W F TUBULAR | 24546 | C3-1/8-T00-8295-G |
| A3A1R17 | 0698-7210 |  | RESISTOR 82.5 OHM $2 \% .05 \mathrm{~W}$ F TUBULAR RESISTOR $31.5 K$ | 24546 16299 | $\left\lvert\, \begin{aligned} & C 3-1 / 8-\text { TOO-82R5-G } \\ & C 4-1 / 8-T 0-3152-F \end{aligned}\right.$ |
| A3A1218 | 0698-3160 | 1 | RFSISTOR 31.8K 1\% . 125 W F TUBULAR | 16299 | C4-1/8-70-3152-F |
| A3A1U1 | 1820-0511 | 3 | IC DGTL SN74 OB N GATE | 01295 | SN7408N |
| A 3 A 142 | 1820-0134 | 1 | IC OGTL REGISTER | 07263 | 93000 C SN7400 |
| A 3 A 163 A 3 A 104 | 1820-0054 | 1 |  | 01295 01295 | SN7400V SN7442N |
| A 3A 104 A 3 L 105 | $1820-0214$ $1820-0328$ | 1 |  | 01295 01295 | $\begin{aligned} & \text { SN7442N } \\ & \text { SN7402N } \end{aligned}$ |
| A 3 A 106 $A 3 A 1 U 7$ | $1820-0579$ $1820-0076$ | 1 | $\begin{array}{lllrl}\text { IC } & \text { OGTL } & \text { SN74 } & 123 & \text { N MULTIVIBPATOR } \\ \text { IC } & \text { OGTL } & \text { SN74 } & 76 & \mathrm{~N} \\ \text { FLIP-FLDP }\end{array}$ | 01295 01295 | SN74123N SN7476N SN4 |
| A 34107 $43 A 108$ | $1820-0076$ $1820-0372$ | 1 | IC. | 01295 01295 | SN74H11N |
| A3Alug | 1820-0054 |  | IC DGTL SN74 DO N GATE | 01295 | SNT 400 N |
| A3A1U10 | 1820-0174 | 3 | IC DGTL SN74 34 N INVERTEF | 01295 | SN7404V |
| A 3 A 2 | 08660-60192 | 1 | BOARD ASSY, HP IB INPUT | 28480 | 08660-50192 |
| A3A 2C1 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 20VNO TA | 56289 | $1500225 \times 902042$ |
| A3A2C2 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-10\% 2OVDC TA | 56289 | $1500225 \times 902042$ |
| A 3A 2C3 | 0180-0197 |  | CAPACITOR-FXD; 2.2UF+-109 20VDC TA | 562.89 | $1507225 \times 902042$ |
| A 3A 2C4 | $0160-0157$ <br> 0 <br> $160-0157$ | 3 | CAPACITOR-FXD 4700 PF +-10\% 200WVDC PDLYE CAPACITOR-FXD 4700PF +-10\% 200WVDC PDLYE | 56289 56289 | 292047292 292947297 |
| A 3A 2C5 | 0160-0157 |  | CAPACITOR-FXD 4700PF +-10\% 200WVDC POLYE | 56289 | 292P4729? |
| $A 3 A^{2} \mathrm{C} 6$ | 0160-0157 |  | CAPACITOR-FXD 4700PF +-10\% 200WVDC POL.YE | 55289 | 292P47292 |
| A3A 2R1 | 0757-0403 | 3 | RESISTOR 121 THM 1\% . 125 W F TUBULAR | 24546 | $\mathrm{r} .4-1 / 8=T 0-1212-F$ |
| $A 3 A 2 R 2$ | 0757-0403 |  | RESISTOR 121 OHM 19.125 W F TUBULAR | 24546 | $C 4-1 / 8-T 0-121 R-F$ |
| A 3A 2R 3 | 0757-0403 |  | RESISTIR 121 OHM 19.125W F TUBULAR | 24546 | C4-1/8-T0-121R-F |
| A 3 a 201 | 1820-0054 |  |  | 01295 | SN7400N SN7438N |
| A 342012 A 34203 | $18200-0621$ $1820-0511$ | 1 | $\begin{array}{llll}\text { IC } \\ \text { IC } & \text { DGTL } & \text { SN74 } \\ \text { ONT } & 38 \\ \text { SN }\end{array}$ | 01295 01295 | SN7438N SN7408V |
| A 3 A 204 | 1820-0070 | 3 | IC DGTL SN74 30 N GATE | 01295 | SN7430V |
| A 30205 | 1820-0070 |  | IC DGTL SNT4 30 N GATE | 01295 | SN7430V |
| A3A2U6 | 1320-0174 |  | IC DGTL SN74 04 N INVERTER | 01295 | SN7404V |
| -342U7 | 1820-1053 | 2 | IC DGTL SN74 14 N SCHMITT TRIGGFR | 01295 | SN7414V |
| A34218 | 1810-0136 | 2 | NETWORK-OFS 10-PIN SIP. 1-PIN-SPCG | 28480 | 1810-0136 |
| A 342119 A 302110 | $1820-0077$ $1820-0511$ | 1 | IC <br> IC <br> IC OGTL <br> OGTL <br> SNT <br> St | 01295 01295 | SN7474N SN7408N |
| A3A 2011 | 1820-0174 |  | IC DGTL SN74 $04 \wedge$ INVERTSR | 01295 | SN7404N |
| A3A2U12 | 1820-0070 |  | IC OGTL SN74 30 N GATE | 01295 | SN7430V |
| A 342013 | 1820-1053 |  | IC OGTL SN74 14 N SCHMITT TRIGGER | 01295 | SN7414V |
| A 342014 | 1810-0136 |  | NETWOPK-RFS 10-PIN SIP. - PIN-SPCG | 28480 | 1810-0135 |
| J3A1 | 08660-60187 | 1 | CABLE, ADAPTER, HP IB (INCLUDES MP1 THRU MP6 | 28490 | 08660-60187 |
| $\begin{aligned} & \text { J } 3 A 1 M P 1 \\ & \text { J } 3 A 1 M P 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0380-1036 \\ & 1251-0483 \end{aligned}\right.$ | $2$ | STANDJFF-HEX M/FEM .255-LG 6-32-THD CONVECTMR, 36-CONT, MALE, MICPC RIBBDN | $\begin{aligned} & 28480 \\ & 71785 \end{aligned}$ | $\begin{aligned} & 0380-1038 \\ & 57-10360-375 \end{aligned}$ |
| J3A1MP3 | 1251-3283 | 2 | CONNCCTRR: 24-CONT: FFM; MICRIRIBRON | 28480 | 1251-3293 |
| J3A MMP4 | 08660-00060 | 2 | MCUNT, HPIP CMANECTTR | 23430 | 08660-00060 |
| J3A1MP5 | 08660-20165 | 2 | COVER, HPIB ADAPTER | 28430 | 08660-20165 |
| J3A 1MP6 | 03660-20166 | 2 | SPACFR, CINNETTIR | 29490 | 08560-20166 |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A3A2 | 08660-60029 | 1 | BOARD ASSY, DIGITAL INTERFACE(REARI | 28480 | 08660-60029 |
| $A 3 A 2 C 1$ | $0180-0197$ $0180-0197$ |  | CAPACII TOR-FXD; CAPACI 2. $2 \mathrm{UF}+-10 \%$ 20V | 56289 | $1500225 \times 902042$ |
| A 3 A 2C 28 $A 3 A 2 C 3$ | 0180-0197 |  | CAPACIITOR-FXD; $2.2 \mathrm{UF}+-10 \%$ 20VDC TA CAPACITOR-FXD; $2.2 \mathrm{UF}+-10 \%$ 20VOC TA | 56289 56289 | $\begin{aligned} & 1505225 \times 902042 \\ & 1500225 \times 902082 \end{aligned}$ |
| A 3A 2 C 4 | 0 160-2219 | 1 | CAPACITOR-FXD $1100 \mathrm{PF}+-5 \% 300 \mathrm{VVDC} \mathrm{MICA}$ | 28430 | 10160-2210 |
| A 3 A 201 | 1854-0071 |  | TRANSISTOR NPN SI PD $=300 \mathrm{MH} \quad \mathrm{FT}=200 \mathrm{MHZ}$ | 28480 | 1854-0071 |
| A3A 202 | 1854-0071 |  | TRANSISTOR NPN SI PD $=300 \mathrm{MW} \quad \mathrm{FT}=200 \mathrm{MHZ}$ | 28480 | 1854-0071 |
| $\begin{aligned} & A 3 A 2 R 1 \\ & A 3 A 2 R 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0421 \\ & 0698-3445 \end{aligned}\right.$ | 26 | RESISTOR 825 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 348 OHM R | 24546 16299 | $\begin{aligned} & C 4-1 / 8-T 0-825 R-F \\ & C 4-1 / 8-T 0-348 R-F \end{aligned}$ |
| A 3A 2R 3 | 0757-0279 |  | RESISTOR 3.16K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-3161-F |
| A 3A 2R 4 | 0698-3445 |  | RESISTOR 348 OHM 1\% | 15299 | C4-1/8-T0-348R-F |
| A 3A 2R 5 | 0698-3445 |  | RESISTOR 348 OHM 1\%.125W F TUBULAR | 16299 | C4-1/8-T0-348R-F |
| A 3A 2R 6 | 0698-3445 |  | RESISTOR 348 OHM 1\% -125W F TUBULAR | 16299 | C4-1/8-T0-348R-F |
| A 3A 2R7 | 0698-3445 |  | RESISTOR 348 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 16299 | C4-1/8-T0-348R-F |
| A 3A2R 8 | 0757-0279 |  | RESISTOR 3.16K 15 . 125 W F TUBULAR | 24546 | C4-1/8-T0-3161-F |
| A 3A 2R9 | 0757-0421 |  | RESISTOR 825 OHM 18.125 W F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A3A 2R 10 | 0757-0421 |  | RESISTOR 825 OHM 12.125 W F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A 3A 2R 111 | 0757-0421 |  | RESISTOR 825 OHM 1 I . 125 W F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A3A $2 R 12$ | 0757-0421 |  | RESISTOR 825 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | $C 4-1 / 8-T 0-825 R-F$ |
| A 3 A $2 R 13$ A 3 2R14 $A$ | 0698-3445 |  |  | $1 \begin{aligned} & 16299 \\ & 15299\end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-348 R-F \\ & C 4-1 / 8-T O-348 R-F \end{aligned}\right.$ |
| A 3A 2R 15 | 0698-3445 |  | RESISTOR 348 OHM 18.125 W F TUBULAR | 15299 | C4-1/8-T0-348R-F |
| A3A $2 R 16$ A 3 A $2 R 17$ | 0698-3445 |  |  | 16299 24546 | C4-1/8-TO-348R-F $\mathrm{C} 4-1 / 8-\mathrm{TO}-825 \mathrm{R}-\mathrm{F}$ |
| A 3 A 2 R 177 A 3 2R 18 | 0757-0421 |  | RESISTOR RESISTOR 825 R | 24546 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-825 R-F \\ & C 4-1 / 8-T O-825 R-F \end{aligned}\right.$ |
| A 3A 2R 19 | 0757-0421 |  | RESISTOR 825 OHM 18.125 W F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A 3A 2R 20 | 0757-0421 |  | RESISTOR 825 OHM 1\%.125W F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| $\begin{aligned} & A 3 A 2 R 21 \\ & A 3 A 2 R 22 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0416 \\ & 0757-0279 \end{aligned}\right.$ | 29 | RESI STOR 511 OHM 1\% -125W F TUBULAR RESISTOR 3.16K 1\%.125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-5112-F \\ & C_{4}-1 / 8-T 0-3161-F \end{aligned}\right.$ |
| A3A2R23 | 0757-0279 |  | RESISTOR 3.16K 1\% .125N F TUBULAR | 24546 | C4-1/8-T0-3161-F |
| A 3A 2R 24 | 0757-0279 |  | RESISTOR 3.16K 18. 125 W F TUBULAR | 24546 | C4-1/8-T0-3161-F |
| A 3A 2R 25 | 0757-0421 |  | RESISTOR 825 OHM 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-825R-F. |
| $\begin{aligned} & \text { A } 3 A 2 R 26 \\ & \text { A } 3 A 2 R 27 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0421 \\ & 0757-0279 \end{aligned}\right.$ |  | RESISTJR 825 OHM $1 \% .125 \mathrm{H}$ F TUBULAR RESISTOR 3.16K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-825 R-F \\ & C 4-1 / 8-T 0-3151-F \end{aligned}\right.$ |
| A 3A2R28 | 0757-0279 |  | RESISTOR $3.16 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-3161-F |
| A 3A 2R 29 | 0698-3445 |  | RESISTOR 348 OHM 1\%.125W F TUBULAR | 15299 | C4-1/8-T0-348R-F |
| A 3A 2R 30 | 0698-3445 |  | RESISTOR 348 OHM 1\% .125W F TUBULAR | 16299 | C4-1/8-50-348P-F |
| $\begin{aligned} & \text { A } 3 A 2 U 1 \\ & \text { A } 3 A 2 U 2 \end{aligned}$ | $1820-0054$ $1820-0301$ | 2 | $\begin{array}{llllll}\text { IC } & \text { DGTL } & \text { SN74 } & 00 & \text { N GATE } \\ \text { IC } & \text { DGTL } & \text { SN74 } & 75 & \mathrm{~N} \text { LATCH }\end{array}$ | 01295 01295 | SN7400N |
| a 3 a 2 U 3 | 1920-0256 |  | IC DGTL MC 858P BUFFER | 04713 | MC 358 P |
| A 3A 204 | 1820-0301 |  | IC DGTL SN74 75 N LATCH | 01295 | SN7475N |
| A3A 3 | 08660-60025 | 1 | BOARD ASSY, DIGITAL INTERCONNECT | 28480 | OB66)-50025 |
| $\begin{aligned} & A 3 A 3 \mathrm{~J} 1 \\ & A 3 A 3 \mathrm{~J} 2 \end{aligned}$ | $\begin{aligned} & 1250-1255 \\ & 1250-1255 \end{aligned}$ |  | CONNFC TOR-RF SMB M PC CONNECTOR-RF SMB M PC | $\begin{aligned} & 98291 \\ & 98291 \end{aligned}$ | 51-051-0000 |
| A4 | 08660-60042 | 1 | LODP ASSY, H.F. | 28480 | 08650-60042 |
| $\triangle 4 \mathrm{Cl} 1$ | 0160-2437 | 23 | CAPACITOR-FXD 5000PF +80-20\% 200WVDC CER <br> CAPACITOR-EXD $5000 \mathrm{PF}+80-20 \%$ 200WVDC CER | $\begin{aligned} & 28480 \\ & 78480 \end{aligned}$ | $\begin{aligned} & 0160-2437 \\ & 0160-2437 \end{aligned}$ |
| A4C 3 | O 160-2437 |  | CAPACITTR-FXD 5000PF + 80-20\% 200WVDC CER | 28480 | 0160-2437 |
| A 4 C 4 | 0 160-2437 |  | CAPACITOR-FXD 5000PF +80-20\% 200WVD: C.ER | 28430 | 0150-2437 |
| A4C5 | 0 160-2437 |  | CAPACITOR-FXO 5000PF +80-20\% 200WVDC CER | 28480 | 0150-2437 |
| $\triangle 4 C 6$ |  |  |  |  |  |
| A4C $A 4$ 4.8 | $\begin{aligned} & 0160-2437 \\ & 0 \\ & 0\end{aligned} 160-2437$ |  | CAPACITOR-FXD 5000PF +80-20\% 200WVDC CER CAPACITOR-FXD 5000PF +80-20\% 200WVDC CFR | 28480 28480 | $0160-2437$ $0160-2437$ |
| A4C9 | O 160-3744 | 6 | CAPACITOR-FXD 1000PF +30-20\% 200WVDC CER | 28480 | 0160-3744 |
| A4C 10 | 0160-2437 |  | CAPACITDR-FXD 5000PF +80-20\% 200WVDC CER | 28480 | 0180-243? |
| A4C11 |  |  | CAPACITOR-FXD 1000 PF +80-20\% 200WVDC CER |  |  |
| $\triangle 4 C 12$ $A 4 C 13$ | O 160-2437 0 0 $160-3744$ |  | CAPACITDR-FXD $5000 \mathrm{PF}+80-20 \%$ CAPACITOR-FXD 200 1000 | 28480 28480 | 0160-2437 |
| A4C14 | 0 160-2437 |  | CAPACITDR-FXD 5000PF + $30-20 \%$ 200WVOC CER | 28480 | 0150-2'37 |
| A4C15 | 0 160-3744 |  | CAPACITOP-FXD 1000PF +80-20\% 200WVOC CER | 23480 | 0160-3744 |
| $\begin{aligned} & \triangle 4 C 16 \\ & A 4 C 17 \end{aligned}$ | $\left\lvert\, \begin{array}{ll} 0 & 160-2437 \\ 0 & 160-3744 \end{array}\right.$ |  | CAPACITOR-FXD 5000 PF +80-20\% 200WVOC CER CAPACTTOR-FXD 1000PF +80-20\% 200WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $0180-2437$ \|0160-3744 |
| A4C18 | 0160-2437 |  | CAPACITOR-FXO 5000 PF + 80-20\% 200WVDC CEP | 28480 | 0160-2437 |
| A4C19 | 0 160-3744 |  | CAPACITOR-FXT $1000 \mathrm{PF}+80-20 \%$ 200WVDC CFP | 28480 | 0160-3744 |
| A $4 C 20$ | 0160-2437 |  |  | 28480 | 0160-2437 |
| $\begin{aligned} & A 4 C 21 \\ & A 4 C 22 \\ & A 4 C 23 \end{aligned}$ | $\begin{array}{lll} 0 & 160-2437 \\ 0 & 160-2437 \\ 0 & 160-2437 \end{array}$ |  | CAPACITOR-FXD $5000 \mathrm{PF}+80-20 \%$ $200 W V D C$ CER <br> CAPACITOR-FXD $5000 \mathrm{PF}+80-20 \%$ $200 W V D C$ CER <br> C $\triangle P A C I T O R-F X D ~$ $5000 P F$   <br>   $80-20 \%$ $200 W V D C$ | 28480 28480 28480 | $\begin{aligned} & 0160-2437 \\ & 0160-2437 \\ & 0160-2437 \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $1250-0901$ $1250-0901$ $1250-0901$ $1250-0901$ $1250-0901$ | 18 | CONNECTOR-RF SMB M SGL HOLE FR <br> CONNECTOR-RF SMB $M$ $S G L$ HOLE FR <br> CONNECTOR-RF SMB $M$ $S G L$ HOLE FR <br> CONNECTOR-RF SMB $M$ $S G L$ HOLE FR <br> CONNFCTOR-PF SMB $M$ $S G L$ HOLE FR | $\begin{aligned} & \text { 2K } 497 \\ & 2 K 497 \\ & 2 K 497 \\ & 2 K 497 \\ & 2 K 497 \end{aligned}$ | $\begin{aligned} & 700166 \\ & 700166 \\ & 700166 \\ & 700166 \\ & 700166 \end{aligned}$ |
|  | $1250-0901$ $1250-0901$ $1250-0901$ $1250-0901$ $1250-0901$ |  | CONNECTOR-RF SMB M SGL HOLE FR CONNFCTOR-RF SMB M SGL HOLE FR CONNECTOR-RF SMB M SGL HOLE FR CONNECTOR-RF SMB M SGL HOLE FR CONNECTOR-RF SMB M SGL HOLE FR | $\begin{aligned} & \text { 2K } 497 \\ & \text { 2K } 497 \\ & \text { 2K } 497 \\ & \text { 2K } 497 \\ & \text { 2K } 497 \end{aligned}$ | $\begin{aligned} & 700166 \\ & 700166 \\ & 700166 \\ & 700166 \\ & 700166 \end{aligned}$ |
|  | $1250-0901$ $1250-0901$ $1250-0901$ $1250-0901$ |  | CONNECTOR-RF SMB M SGL HOLE FR CONNECTOR-RF SMB M SGL HOLE FR CONNECTOR-RF SMB M SGL HOLE FR CONNECTOR-RF SMB M SGL HOLE FR | $\begin{aligned} & \text { 2K } 497 \\ & 2 K 497 \\ & 2 K 497 \\ & 2 K 497 \end{aligned}$ | $\begin{aligned} & 700166 \\ & 700166 \\ & 700166 \\ & 700166 \end{aligned}$ |
| A4L 1 | 9140-0144 | 4 | COIL: FXD; MOLDED RF CHOKE; 4.7UH $10 \%$ | 24226 | 10/471 |
| $\begin{aligned} & A 4 W 1 \\ & A 4 W 2 \\ & A 4 W 3 \\ & A 4 W \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-60080 \\ & 08660-60050 \\ & 08660-60063 \\ & 08660-60055 \end{aligned}\right.$ | 1 1 1 | CABLE ASSY, GRAY CABLE ASSY, GRAY CABLE ASSY, GRAY CABLE ASSY, GRAY | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-60080 \\ & 08660-60050 \\ & 08660-60063 \\ & 08660-60055 \end{aligned}$ |
|  |  |  | miscellanedus a 4. |  |  |
|  | $\begin{array}{\|l} 08660-00014 \\ 08660-00015 \\ 08660-00016 \\ 08660-00017 \\ 08660-00018 \end{array}$ | 1 1 1 1 1 | ```COVER, REF. OSC. COVER, REF. DIVIDER COVER, REF. PHASE DETECTOR COVER, DIVIDE BY THO. COVER, PRETUNE``` | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-00014 \\ & 08660-00015 \\ & 08660-00016 \\ & 08660-00017 \\ & 08660-00018 \end{aligned}$ |
|  | 08660-00019 08660-00020 08660-20063 | 1 1 1 | COVER, VCO COVER, PHASE DFTECTDR HOUSING, H.F. LP | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-90019 \\ & 08660-00020 \\ & 08660-20063 \end{aligned}$ |
| $\triangle 4 A_{1}$ | 08660-60003 | 1 | BOARD ASSY, REF. DIVIDER | 28480 | 08660-60003 |
| $\begin{aligned} & A 4 A 1 C 1 \\ & A 4 A 1 C 2 \end{aligned}$ | 0160-2201 | 1 | CAPACITOR-FXD 51PF +-5\% 300WVOC MICA CAPACITGR-FXD; 6.8UF+-10\% 35VDC TA | 28480 56289 | $\begin{aligned} & 0160-2201 \\ & 1500685 \times 903582 \end{aligned}$ |
| A4A1C3 | 0180-0229 | 11 | CAPACITOR-FXD; $330 \mathrm{~F}+-10 \%$ IOVDC TA-SOLID | 56289 | $1500336 \times 901082$ |
| A 4A 1C4 | 0160-2199 | 1 | CAPACITOR-FXD 30PF +-5\% 300WVDC MICA | 28480 | 0160-2199 |
| A 4A 1C5 | 0160-0154 |  | CAPACITOR-FXD 2200PF +-10\% 200wVOC POLYE | 56289 | 292 P22292 |
| $\begin{aligned} & A 4 A 1 C 6 \\ & \text { A } 4 \text { A } 1 C 7 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0 & 160-0154 \\ 0 & 160-0297 \end{array}\right.$ | 2 | CAPACITOR-FXD 2200PF +-10\% 200WVDC POLYE CAPACITOR-FXD 1200PF +-10\% 200WVDC POLYE | $\begin{aligned} & 56289 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 292 P 22292 \\ & 292 P 12292 \end{aligned}$ |
| A4A1CR1 | 1902-0048 | 1 | DICDE-ZNR 6.81V 5\% DO-7 PD=.4W | 28480 | 1902-0048 |
| A4A1L1 $A 4 A 1 L 2$ | 9 9 $9100-1642$ 9 | 2 | COIL: FXD; MOLDED RF CHOKE; 270UH 5\% COIL; FXD; MOLDED RF CHOKE; 270UH 5\% | $\begin{aligned} & 24226 \\ & 24226 \end{aligned}$ | $\begin{aligned} & 19 / 273 \\ & 19 / 273 \end{aligned}$ |
| $\begin{aligned} & A 4 A 1 L 2 \\ & A 4 A 1 L 3 \end{aligned}$ | 9100-1642 |  | COIL: FXD; MOLDED RF CHOKE; 270UH 5\% COIL; FXD; MOLDED RF CHOKE; 4.7UH 10\% | \|l4226 | $\begin{aligned} & 19 / 273 \\ & 10 / 471 \end{aligned}$ |
| A4A101 A4A102 | $1854-0019$ $1854-0019$ | 15 | TRANSISTOP NPN SI TO-18 PD=360MW TRANSISTOR NPN SI TR-18 PD=360MH | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 1854-0010 \\ & 1854-0019 \end{aligned}\right.$ |
| A4A103 | 1854-0045 | 4 | TRANSISTOR NPN SI TO-18 PD=500MW | 28480 | 1854-0045 |
| $\begin{aligned} & \triangle 4 A 1 R 1 \\ & A 4 A 1 R 2 \end{aligned}$ | $\left\lvert\, \begin{gathered} 0757-0444 \\ 0698-3622 \end{gathered}\right.$ | 13 1 | RESISTOR $12.1 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 120 OHM 5\% 2W MO TUBIJLAR | 24546 24546 | $\begin{aligned} & C 4-1 / 8-\text { T0-1 } 212-F \\ & \text { FP42-2-TOO-120R-J } \end{aligned}$ |
| A4AIR 3 | 0698-0083 | 40 | RESISTIR 1.96 K 1\% 1 . 125 W F TUBULAR | 16299 | C4-1/8-T?-1 961-F |
| A4A1R4 | 0757-0280 |  | RESISTOR 1K 1\%.125W F TUBULAR | 24546 | C4-1/8-T0-1 001-F |
| A4A1R 5 | 0757-0394 |  | RESISTOR 51.1 OHM 19.125W F TUBULAR | 24546 | C4-1/8-T0-51R1-F |
| $\begin{aligned} & A 4 A 1 R 6 \\ & A 4 A 1 R 7 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0280 \\ & 0698-0083 \end{aligned}\right.$ |  | RESISTOR 1K 1\% . 125W F TUBULAR RESISTOR 1.96K 1\%.125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1001-F \\ & C 4-1 / 8-T D-1961-F \end{aligned}$ |
| A4AIR 8 | 0757-0280 |  | RESISTOR 1K 1\%.125W F TUBULAR | 24546 | C4-1/8-T0-1001-F |
| A4AIR9 | 0757-0394 |  | RESISTOR 51.1 DHM 1\%.125w F TUBULAR | 24546 | C4-1/8-T0-51R1-F |
| A4A1R 10 | 0757-0280 |  | RESISTOR 1K 1\%. 125 W F TUBULAR | 24546 | C4-1/8-T0-1001-F |
| $\begin{aligned} & A 4 A 1 R 11 \\ & A 4 A 1 R 12 \end{aligned}$ | $\begin{aligned} & 0698-3441 \\ & 0698-3441 \end{aligned}$ | 17 | RESI STOR RESI STOR 215 215 OHM OHM R | $\left\lvert\, \begin{aligned} & 16299 \\ & 16299 \end{aligned}\right.$ | $\begin{aligned} & C 4-1 / B-T O-215 R-F \\ & C 4-1 / 8-T 0-215 R-F \end{aligned}$ |
| A4A1R13 | 0698-3441 |  | RESISTOR 215 OHM 1\%.125W F TUBULAR | $16299$ | $\mathrm{C} 4-1 / 8-\mathrm{TO}-215 \mathrm{R}-\mathrm{F}$ |
| A4A1R14 | 0757-0401 |  | RESISTOR 100 OHM 1\%.125W F TUBULAR | $24546$ | C4-1/8-T0-101-F |
| A4A1U1 | 1820-0054 |  | IC DGTL SN74 00 N GATE |  |  |
| A4A1U2 A 41103 | $1820-0055$ $1820-0055$ |  | IC OGTL SN74 90 N COUNTER <br> IC DGTL SN74 90 N COUNTER | $\left\lvert\, \begin{array}{ll} 01295 \\ 01295 \end{array}\right.$ | $\begin{aligned} & \text { SN7490N } \\ & \text { SN7490V } \end{aligned}$ |
| A44103 | 1820-0055 |  | IC DGTL SNT4 90 N GOUNTER | 01295 | SN7490 |
| A4A2 | 08660-60002 | 1 | bIARD ASSY,REF. PHASE DETCCTTIR | 28480 | 08660-60002 |
| A4A $2 C 1$ $\triangle 4 A 2 C 2$ | $0180-0100$ $0180-0116$ | 1 | CAPACITOR-FXD; 4.7UF+-10\% 35VDC TA CAPACITOR-EXD; 6.8UFt-10\% 35VOC TA | 58299 58289 | $\begin{aligned} & 1500475 \times 9035 \mathrm{B2} \\ & 1500685 \times 9035 \mathrm{B2} \end{aligned}$ |
| A4a2C3 | 0180-0228 |  | CAPACITOR-EXD; $22 \mathrm{UF} \mathrm{F}+10 \mathrm{O}$ 15VDC TA-SOL IO | 56289 | $1500225 \times 901582$ |
| A 4A 2C.4 | 0180-2055 |  | CAPACITOR-FXD.01UF +80-20\% 100WVDC CED | $\left\lvert\, \begin{aligned} & 28480 \\ & 56390 \end{aligned}\right.$ | $160-2055$ |
| A4A 2C5 | 0180-1746 |  | CAPACITOR-FXD; $15 \mathrm{JJF}+-10 \%$ 2OVDR TA-SNLID | $56289$ | $1500155 \times 902082$ |
| $\begin{aligned} & A 4 A 2 C 6 \\ & A 4 A 2 C 7 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0160-2055 \\ & 0160-2055 \end{aligned}\right.$ |  | CAPACITOR-FXD .OLUF +80-20\% 100WVDC GER CAPACITOR-FXD .OIUF + 80-20\% 10OWVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0150-2055 \\ & 0150-2055 \end{aligned}\right.$ |
| A4A2C8 | -160-2055 |  |  | 29480 | 0150-2055 |
| $\begin{aligned} & A 4 \Delta \geqslant C 9 \\ & A 4 A 2 C 10 \end{aligned}$ | $\begin{aligned} & 0190-0229 \\ & 0 \\ & 0 \end{aligned} 160-2055$ |  | CAPACITOR-FXD; $33 U F+=10 \%$ 1OVIC TA-SDLID CAPACITDR-FXO .DIUF +80-20\% 10OWVDC CER | $\left\lvert\, \begin{aligned} & 56289 \\ & 28490 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & 1500336 \times 9010 B 2 \\ & 0150-2055 \end{aligned}\right.$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A4A2C11* | 0140-0191 | 1 | CAPACITOR-FXD 56PF +-5\% 300WVDC MICA <br> * FACTORY SELECTED PaRT | 72136 | DM15E550J0300WVICR |
| A4A 2C12 | 0160-2308 | 1 | CAPACITJR-FXD 36PF +-5\% 300WVIC MIICA | 28480 | $\begin{aligned} & 0160-2308 \\ & 0160-2095 \end{aligned}$ |
| A4A 2C13 A4A 2C14 | \|r160-2055 |  |  | 28480 28480 | 0160-2055 |
| A 4A 2C15 | 0160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A4A 2C 16 | 0160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A4A2C17 | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-20\% 100HVOC CER | 28480 | 0160-2055 |
| A4A 2C18 | 0160-2055 |  | CAPACITIR-FXD .01UF +80-20\% 100WVOC CER | 28480 | 0160-2055 |
| A442C19 | 0160-2055 |  | CAPACITOR-FXD . $01.1 \mathrm{FF}+80-20 \%$ 100WVDC CER | 28480 | 0160-2055 |
| $\begin{aligned} & \text { A4A 2C } 20 \\ & \text { A4A } 2 C 21 \end{aligned}$ | $\begin{aligned} & 10160-2204 \\ & 10160-2055 \end{aligned}$ |  | CAPACITOR-FXD 100PF +-5\% 300WVDC MICA CAPACITIR -FXD. $01 \mathrm{LUF}+80-20 \%$ 100WVOC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | \|0160-2204 |
| A4A2C22 | 0180-1743 | 1 | CAPACITOR-FXD; . 1 UF+-10\% 35VOC TA-SOLID | 285289 | 1500104 X9035A2 |
| A4A 2C 23 | 0 160-3537 | 2 | CAPACITMR-FXD 680PF +-5\% 100WVDC MICA | 28480 | 16160-3537 |
| A4A 2C. 24 | 0160-2205 | 3 | CAPACITOR-FXD 120PF +-5\% 300HVDC MICA | 28480 | 0160-2205 |
| $\begin{aligned} & A 4 A 2 C 25 \\ & A 4 A 2 C 26 \end{aligned}$ | 0160-2218 | 3 1 | CAPACITCR-FXD 1000PF +-5\% 300WVDC MICA CAPACITOR-FXD; . 33UF $+-10 \%$ 35VOC TA | $\begin{aligned} & 28480 \\ & 56380 \end{aligned}$ | $\begin{aligned} & 0160-2218 \\ & 1500334 \times 903542 \end{aligned}$ |
| A4A2C27 | 0160-2055 |  | CAPACITOR-FXD. 01 l | 28480 | $0160-2055$ |
| $\begin{aligned} & \text { A4A } 2 C R 1 \\ & \text { A4A CCR2 } \end{aligned}$ | 1902-0041 | 7 | DIODE-2NP 5.11V 5\% DO-7 $\mathrm{PD}=.4 \mathrm{~W}$ TC= DIODE-SWITCHING 2NS 30V 50MA | $\begin{aligned} & 04713 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{array}{ll} 52 & 10939-98 \\ 1901-0040 \end{array}\right.$ |
| A4A 2CR3 | 1901-0040 |  | DI ODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A4A2CR4 | 1901-0179 | 6 | DIDDE-SWITCHING 75OPS 15V 50MA | 28480 | 1901-0179 |
| A4A2CR5 | 1901-0179 |  | DIODE-SWITCHING 750PS 15V 50MA | 28480 | 1901-0179 |
| $A 4 A^{2} 21$ | 9100-1629 | 28 | COIL : FXD; MOLDED RF CHOKF; 47UH 5\% | 24226 | $15 / 472$ |
| A4A 2 LL 2 $A 4 A 2 L 3$ | 9100-1629 |  | COIL : FXD: MOLDFD RF CHOKE: 47UH 5\% | 24226 76493 | $\begin{aligned} & 15 / 472 \\ & 9230-26 \end{aligned}$ |
| A4A 2 L 3 $A 4$ 4 4 | 9100-2260 | 2 | COIL COIL FXD: MOD FXD; MOLDED | 76493 24226 | $\begin{aligned} & 9230-26 \\ & 15 / 223 \end{aligned}$ |
| A4A 2L 5 | 9140-0237 | 1 | COIL ; FXD: MOLDED RF CHOKE; 200UH 5\% | 24226 | 15/203 |
| A4A 201 A4A202 | 1854-0019 |  | TPANSISTOR NPN SI TO-18 PD=360MW | $28480$ |  |
| A4A202 A4A203 | $1854-0019$ $1854-0019$ |  | $\begin{array}{llllll}\text { TRANSISTOR } & \text { NPN SI } & \text { TO-18 } & P D=360 \mathrm{MH} \\ \text { TRANSISTOR } & \\ \text { NPN SI } & \text { SO-18 } & P D=360 \mathrm{MW}\end{array}$ | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0019 \\ & 1854-0019 \end{aligned}$ |
| A 4A 203 | 1854-0019 |  | TRANSISTOR NPN SI TO-18 PD=360MW | 28480 | 1854-0019 |
| A4A205 | 1853-0015 | 6 | TRAVSISTOR PNP SI CHIP PD=200MW | 28480 | 1853-0015 |
| $\begin{aligned} & A 4 A 206 \\ & A 4 A 207 \end{aligned}$ | $\begin{aligned} & 1854-0019 \\ & 1853-0020 \end{aligned}$ |  | TRANSISTOR NPN SI TO-18 PD=360MW TPANSISTOR PNP SI CHIP PD=30OMW | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0019 \\ & 1853-0020 \end{aligned}$ |
| A 4A 208 | 1854-0071 |  | TRANSISTOR NPN SI PD $=300 \mathrm{MH} \mathrm{FT}=200 \mathrm{MHZ}$ | 28480 | 1854-0071 |
| A4A209 | 1854-0071 |  | TRANSISTOR NPN SI PD $=300 \mathrm{MH}$ FT $=200 \mathrm{MHZ}$ | 28480 | 1854-0071 |
| A4A2010 | 1854-0071 |  | TRANSISTOR NPN SI PD= $=300 \mathrm{MW} \mathrm{FT}=200 \mathrm{MHZ}$ | 28480 | 1854-0071 |
| A4A2011 | 1854-0019 |  | TRANSISTOR NPN SI TO-18 PD=360MH | 28480 | 1854-0019 |
| A4A 2R 1 | 0698-3440 | 24 | RFSISTOR 196 OHM $1 \%$. 125W F TUBULAR | 16299 | C4-1/8-T0-196R-F |
| A4A 2R 2 $A 4 A 2 R 3$ | 0757-0401 |  | RESISTOR 100 OHM 1 \$ . $125 W$ F TUBULAR RESISTOR 10K 1\% . 125W F TUBULAR | 16299 24546 | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-100 \mathrm{R}-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-T 0-1002-F \end{aligned}\right.$ |
| A4A2R 3 A 4ARR | 0757-0442 | 17 | RESISTOR $10 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 8.25 K 19.125 W F TUBULAR | 24546 24546 | C4-1/8-T0-1 002-F |
| A 4A2R 5 | 0757-0416 |  | RESISTOR 511 OHM 18.125 W F TUBULAR | 24546 | C4-1/8-T0-511R-F |
| $\begin{aligned} & A 4 A 2 R 6 \\ & A 4 A 2 R 7 \end{aligned}$ | $\begin{aligned} & 0757-0280 \\ & 0757-0401 \end{aligned}$ |  | RESISTOR 1 K 1\% . 125 W F TUBULAR RESISTOR 100 ЭHM 1 \% . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-1001-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-101-\mathrm{F} \end{aligned}$ |
| A4A2R 8 | 0698-0083 |  | RESISTOP 1.96 K 18.125 WF TUBULAR | 15299 | C4-1/8-T0-1961-F |
| A4A2R 9 | 0757-0438 |  | RESISTOR 5.11K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-5111-F |
| A4A 2R 10 | 0698-3156 | 8 | RESISTOR 14.7K 1\%, 125 W F TUBULAR | 16209 | C4-1/8-T0-1472-F |
| $\begin{aligned} & A 4 A 2 R 11 \\ & \text { A4A 2R } 12 \end{aligned}$ | $\begin{array}{\|l} 0757-1090 \\ 0757-0401 \end{array}$ | 1 | RESISTOR 261 OHM 1\%.5W F TUBULAR RESISTOR 100 OHM $1 \% .125 \mathrm{~W}$ F TUBIJLAR | $\begin{aligned} & 19701 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \text { MF7C1/2-T0-261R-F } \\ & C 4-1 / 8-50-101-F \end{aligned}$ |
| A4A2R13 | 0698-0083 |  | RFSISTOR 1.96 K 18.125 W F TUBULAR | 16299 | C4-1/8-70-1961-F |
| A 4A2R 14 | 0757-0280 |  | RESISTOR 1K 1\% . 125 W F TUBULAP. | 2454.6 | C4-1/8-T0-1001-F |
| A4A2R15 | 0757-0401 |  | RESISTOR 100 OHM 18.125 W F TUBULAR | 24546 | C4-1/8-T0-101-F |
| $\begin{aligned} & \text { A 4A 2R } 16 \\ & \text { A 4A 2R } 17 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-0082 \\ & 0698-3441 \end{aligned}\right.$ |  | RESISTOR 464 OHM 1\% . 125 W F TUBULAR RESISTOP 215 DHM 1 \% . 125W F TUBULAR | $\begin{aligned} & 16209 \\ & 16209 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-4640-F \\ & C 4-1 / 8-T 0-215 R-F \end{aligned}\right.$ |
| A4A2R18 | 0698-0084 | 12 | RESISTOR 2.15k 1\%.125W F TURULAR | 16299 | C4-1/8-T0-2151-F |
| A4A2R19 | 0757-0280 |  | RESISTOR $1 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-1001-F |
| A4A2R 20 | 0698-3132 |  | RESISTOP 261 OHM $1 \% \cdot 125 \mathrm{~W}$ F TUBULAR | 16299 | C4-1/8-T0-2610-F |
| $\begin{aligned} & A 4 A 2 R 21 \\ & \text { A } 4 A 2 R 22 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0441 \\ & 0757-0441 \end{aligned}\right.$ |  | RESISTOR 8.25K 1\% . 125 H F TUBULAR RESISTOR 8.25K 1\% -125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-8251-F \\ & C 4-1 / 8-T 0-8251-F \end{aligned}\right.$ |
| A4A2R 23 | 0698-3438 | 9 | RESISTOR 147 OHM 1\% 125 W F TUBULAR | 16209 | C4-1/8-T0-147R-F |
| A4A2R 24 | 0757-0346 |  | RFSISTOR 10 OHM 18.125W F TUBULAR | 24546 | C4-1/8-T0-1 0R O-F |
| A4A 2R 25 | 0757-0346 |  | RESISTOP. 10 OHM 1\%.125W F TURULAR | 24546 | ( $4-1 / 8$-T0-1 OR 0-F |
| $\begin{aligned} & A 4 A 2 R 26 \\ & A 4 A 2 R 27 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3438 \\ & 0757-0418 \end{aligned}\right.$ | 6 | RESISTOR 147 OHM 1\%. 125 W F TURULAR RESISTOF 610 THM $1 \% .125 \mathrm{~W}$ F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-147 R-F \\ & C 4-1 / 8-T 0-61 ? R-F \end{aligned}$ |
| A4A2P28 | 0698-3158 | 3 | PESISTOR 23.7K 1\% .125W F TUBULAR | 16299 | C4-1/8-T0-2372-F |
| A4A2R 29 | 0698-3154 |  | RFSISTOR 4.22 K 1\% $\%$.125W F TUBULAR | 16299 | C4-1/8-T0-4221-F |
| A4A 2R 30 | 0698-3154 |  | RFSISTOR 4.22K 1\% . 125 W F TUBIILAR | 16299 | C4-1/8-T0-4221-F |
| $\begin{aligned} & A 4 A \text { PR } 31 \\ & A 4 A \text { 2R } 32 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0757-0346 \end{aligned}\right.$ |  | RESISTOR 10K 1\% . 125 W F TUBULAR PESISTIR 10 OHM 12. 125W F TURULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / B-T O-1 \text { OR O-F } \end{aligned}$ |
| A 4A2R 33 | 0757-0346 |  | RESISTIR 10 OHM 17.125 W F TUBULAR | 24546 | C4-1/8-T0-1 0R 0-F |
| A4A 2R 34 A 4 2 2 l | $0698-3453$ $0698-3260$ | 1 | RESISTCR RESISTOR | $\begin{aligned} & 16299 \\ & 19701 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-1963-F \\ & \text { MF } 4 C 1 / 8-\text { TO-4643-F } \end{aligned}\right.$ |

Table 6-3. Replaceable Parts


Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A4A3U1 | 1820-0469 | 3 | IC DGTL SN74H 102 N FLIP-FLOP | 01205 | SN74H102N |
| A4A4 | 08660-60001 | 1 | BOARD ASSY,REF. VCO | 28480 | 08660-60001 |
| $\begin{aligned} & A 4 A 4 C 1 \\ & A 4 A 4 C 2 \end{aligned}$ | $\begin{aligned} & 0160-3456 \\ & 0121-0451 \end{aligned}$ | 3 | CAPACITOR-FXD 1000 PF +-10\% 1000WVDC CER CAPACITOR; VAR; TRMR; AIR: 1.7/11PF | 28489 74970 | $\begin{aligned} & 0160-3456 \\ & 187-0106-005 \end{aligned}$ |
| A4A4C3 | 0180-0116 |  | CAPACITOR-FXD; $6.8 \mathrm{UF}+-10 \% 35 \mathrm{VDC} \mathrm{TA}$ | 56289 | $1500685 \times 903582$ |
| A 4A 4C4 | 0180-0228 |  | CAPACITOR-FXD; $22 \mathrm{UVF+-10} \mathrm{\%} \mathrm{15VDC} \mathrm{TA-SOLID}$ | 55289 | $150 \mathrm{D} 225 \times 9015 \mathrm{B2}$ |
| $A 4 A 4 C 5$ | $0160-0214$ | 1 | CAPAP.ITRR-FXD 10PF +-5\% 500WVDC CER | 28480 | $0160-0214$ |
| $\begin{aligned} & A 4 A 4 C 6 \\ & A 4 A 4 C 7 \end{aligned}$ | $\begin{aligned} & 0160-2266 \\ & 0180-0116 \end{aligned}$ | 10 | CAPACITOR-FXD 24 PF +-59 500WVDC CER 0+ CAPACITOR-FXD; 6.8UF+-10\% 35VDC TA | $\begin{aligned} & 28480 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 0160-2266 \\ & 1500685 \times 9035 R 2 \end{aligned}$ |
| A4A4C8 | 0160-2055 |  | CAPACITOR-FXD . $01 \mathrm{UFF}+80-20 \%$ 100WVDC CER | 28480 | 150160-2055 |
| A4A4C9 | 0160-2055 |  | CAPACITOR-FXD . $01 U F+80-20 \% 100 \mathrm{WVDC}$ CER | 28480 | 0160-2055 |
| A4A4C10 | 0160-2306 | 1 | CAPACITMR-FXD 27PF +-5\% 300WVDC MICA | 28480 | 0160-2305 |
| $\begin{aligned} & A 4 A 4 C 11 \\ & A 4 A 4 C 12 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0140-0190 \\ & 0180-0228 \end{aligned}\right.$ | 4 | CAPACITOR-FXD 39PF + $-5 \%$ 30OHVOC MICA CAPACITDR-FXD: $22 \mathrm{UF}+-10 \% 15 \mathrm{VDC}$ TA-SOLID | $\begin{aligned} & 72136 \\ & 56289 \end{aligned}$ | DM15E39 OJ0300WVICR 150ח226×9015R2 |
| A 4 A 4 Cl 13 | 0160-2055 |  | CAPACITOR-FXD .O1UF +80-20\% 100WVOC CER | 28480 | 16160-2055 |
| A4A4C14 | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER | 28430 | 0160-2055 |
| A4A4C15 | 0160-2055 |  | CAPACITOR-FXD. .OIUF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| $\begin{aligned} & A 4 A 4 C 16 \\ & A 4 A 4 C 17 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0160-2055 \\ & 0121-0046 \end{aligned}\right.$ | 1 | CAPACITOR-FXD .OLUF +80-20\% 100WVOC CER CAPACITDR; VAR; TRMR; CER; 9/35PF | $\begin{aligned} & 28480 \\ & 73899 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & \text { DV11PS357 } \end{aligned}$ |
| A 4A 4C18 | O160-3879 |  | CAPACITOR-FXD . $014 \mathrm{~F}+-208100 \mathrm{WVDC}$ CER | 28480 | 0160-3879 |
| A4A4C19 | 0160-2327 | 4 | CAPACITOR-FXD 1000 PF +-20\% 100 WVDC CER | 28480 | 0160-2327 |
| A4A4C20 | 0140-0190 |  | CAPACITOR-FXO 39PF +-5\% 300WVDC MICA | 72136 | DM15E300J0300WV1CR |
| $\begin{aligned} & A 4 A 4 C 21 \\ & A 4 A 4 C 22 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0140-0190 \\ & 0160-2055 \end{aligned}\right.$ |  | CAPACITOR-FXD 39PF +-5\% 300WVIC MICA CAPACITOR-FXD .O1UF + 80-20\% 100WVDC CER | $\begin{aligned} & 72136 \\ & 28480 \end{aligned}$ | OM15F $390 J 03$ OOWV1CR $0160-2055$ |
| A4A4C23 | 0 121-0451 |  | CAPACITOR; VAR; TRMR : AIR; $1.7 / 11 \mathrm{PF}$. | 74970 | 187-0106-005 |
| $\triangle 444 C 24$ | 0160-2327 |  | CAPACITOR-FXD 1000PF +-20\% 100 WVOC CER | 284880 | 10160-2327 |
| A4A4C25 | 0160-2055 |  | CAPACITOR-FXD . $01 U F+80-20 \%$ 100WVOC CER | 28480 | 0160-2055 |
| A4A 4C26 $A 4 A 4 C 27$ | O160-2055 |  | CAPACITOR-FXD . O1UF +80-20\% 100WVDC CER CAPACITOR-FXD .O1UF +80-20\% 100WVDC CER | 28480 28420 | $\text { \|lol } 0160-2055$ |
| $\triangle 4 A 4 C 28$ | - 160-2055 |  | CAPACITOR-FXD .01UF + 30-20\% 100 WVOC CER | 29480 | 0160-2055 |
| A4A4C29 | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-20\% 100 WVOC CER | 28480 | 0160-2055 |
| A4A4C 30 | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-203 100WVDC CER | 28490 | 0160-2055 |
| $\begin{aligned} & A 4 A 4 C 31 \\ & A 4 A 4 C 32 \end{aligned}$ | 0121-0451 |  | CAPACITOR; VAR; TRMR; AIR: 1.7/11PF CAPACITOR-FXD 1000 PF +-20\% 100 WVDC CER | $\begin{aligned} & 74970 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 187-0106-005 \\ & 0150-2327 \end{aligned}$ |
| A4A4C33 | 0160-2055 |  | CAPACI TOR-FXO .OIUF +80-20\% 100 WVOC CER | 28480 | 0160-2055 |
| A4A4C 34 | 0160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100WVC CFR | 28480 | 0160-2055 |
| A4A4C35 | 0140-0190 |  | CAPACITOR-FXD 39PF +-59 300WVDC MICA | 72136 | DM1 5¢ 390J0300NVICR |
| $\begin{aligned} & A 4 A 4 C 36 \\ & A 4 A 4 C 37 \end{aligned}$ | $\left\lvert\, \begin{array}{ll} 0 & 160-2307 \\ 0 & 160-2055 \end{array}\right.$ | 1 | CAPACITOR-FXD 47PF +-5\% 300WVDC MICA CAPACITOR-FXD .OIUF +80-20\% 10OWVOC CER | 28480 28480 | $\left\lvert\, \begin{aligned} & 0160-2307 \\ & 0160-2055 \end{aligned}\right.$ |
| A4A4C38 | 0160-2205 |  | CAPACITOR-FXC 120PF +-5\% 300WVDC MICA | 29480 | 0160-2205 |
| A4A4C39 | 0160-2205 |  | CAPACITOR-FXD 120PF +-5\% 300WVDC MICA | 28480 | 0160-2205 |
| A4A4C40 | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-20\% 100WVOC CER | 28480 | 0160-2055 |
| A4A4C41 | 0121-0448 | 1 | CAPACITMR; VAR; TRMR; CER: 2.5/5PF | 0086S | 5S-TRIKn-03, 2.5 - |
| $\begin{aligned} & A 4 A 4 C R 1 \\ & A 4 A 4 C R 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0122-0287 \\ & 1902-0041 \end{aligned}\right.$ | 1 | DIO-VVC 10PF 5\% C.2/C 20=2000000 MIN DIODE-ZNR 5.11V 5\% DO-7 PD=.4W TC= | $\begin{aligned} & 04713 \\ & 04713 \end{aligned}$ | SMV389-287 <br> S2 1093 O-98 |
| $\begin{aligned} & A 4 A 4 L 1 \\ & A 4 A 4 L 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 9 \text { 100-1623 } \\ & 9100-1629 \end{aligned}\right.$ | 1 | COIL: FXD: MOLDED PF CHOKE; 27UH 5\% <br> COIL: FXD; MDLDFD RF CHOKE; 47UH 5\% | $\begin{aligned} & 24226 \\ & 24226 \end{aligned}$ | $\begin{aligned} & 15 / 272 \\ & 15 / 472 \end{aligned}$ |
| A4A4L 3 | $9100-1629$ |  | COIL F FXD; MOLDED RF CHOKE; 47 UH 5\% | 24226 | $15 / 472$ |
| A4A4L 4 | 08660-80002 | 1 | INDUCTOR | 28480 | 08660-80002 |
| A4A4L 5 | 08660-80009 | 3 | INDUCTDR | 28480 | 08660-80009 |
| A4A4L 6 | 9100-2247 | 3 | COIL : FXD; MOLDEC RF CHEKE; . 1 UH 108 | 24.226 |  |
|  | 9100-2247 |  | COIL ; FXD; MOLDED RF CHOKF; . 1 UH $10 \%$ PART OF PPINTED CIRCUIT BOARD | 24226 | $10 / 100$ |
| A4AALC |  |  | PART OF PRINTED CIRCUIT BOARD |  |  |
| A4A4L 10 | 9100-2247 |  | COIL: FXO; MOLDED RF CHOKE; . IUH $10 \%$ | 24226 | 10/100 |
| $\begin{aligned} & A 4 A 4 L 11 \\ & A 4 A 4 L 12 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 9140-0158 \\ & 9100-2254 \end{aligned}\right.$ | 1 | COIL, FXD, MOLDED RF CHEKE, 1UH 10\% <br> COIL; FXD; MOLDFD RF CHOKE; . 39 UH 10\% | $\begin{aligned} & 24226 \\ & 24226 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 10 / 101 \\ & 10 / 300 \end{aligned}\right.$ |
| A4A401 | 1854-0019 |  | TRANSISTOR NPN SI TO-18 PD $=360 \mathrm{MW}$ | 28480 | 1854-0019 |
| A44402 | 1854-0345 |  | TRANSISTOR NPN 2 N5 $177^{\circ} \mathrm{SI} \quad \mathrm{PD}=200 \mathrm{MW}$ | 04713 | 2N5179 |
| A44403 | 1854-0345 |  | TRAVSISTOR NPN 2 N5 179 SI PR=200M | 04713 | 2N5179 |
| A4A404 A4A405 | $1854-0431$ $1854-0540$ | 9 3 | TRANSISTOR NPN $2 N 5179$ SI TO-72 PD $=200 \mathrm{MH}$ TRANSISTOR NPN SI TO-72 PD=200MW | 02735 28480 | $\left\lvert\, \begin{aligned} & 2 N 5179 \\ & 1854-0540 \end{aligned}\right.$ |
|  | 1854-0540 |  |  |  |  |
| $\begin{aligned} & A 4 A 406 \\ & 44 A 407 \end{aligned}$ | $\begin{aligned} & 1854-0540 \\ & 1854-0540 \end{aligned}$ |  | TRANSTSTOR NPN SI TO-72 PD=200MW TRANSISTOP NPN SI TO-72 PD $=200 \mathrm{MW}$ | $\left\lvert\, \begin{aligned} & 28480 \\ & 28480 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & 1854-0540 \\ & 1854-0540 \end{aligned}\right.$ |
| 444408 444409 | $\begin{aligned} & 1854-0431 \\ & 1854-0404 \end{aligned}$ |  | TRAVSISTOR NPN $2 N 5179$ SI TO-72 PR $=200 \mathrm{MH}$ TRANSISTOF NPN SI TO-18 PI $=360 \mathrm{MW}$ | $\begin{aligned} & 02735 \\ & 28480 \end{aligned}$ | $\begin{aligned} & \text { 2N5179 } \\ & 1854-0404 \end{aligned}$ |
| A44409 | 1854-0404 | 1 | TRANSISTOF NPN SI TO-18 P? $=360 \mathrm{MW}$ | $28480$ | 1854-0404 |
| A4A4R1 <br> A4A4R2 <br> A4A4R 3 <br> A4 4 4R 4 <br> A4A4R 5 | $\begin{aligned} & 0757-0442 \\ & 0757-0401 \\ & 0757-0418 \\ & 0757-0394 \\ & 0757-0416 \end{aligned}$ |  | RESISTOP 1OK 1\% . 125 W F TUBULAR RESISTOR 100 OHM 1\% . 125 W F TUBULAR RESISTOR 619 OHM 19.125 H F TUBULAR RESISTOR 51.1 OHM 1\%. 125W F TUBULAR RESISTOR 511 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-1002-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-101-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-610 \mathrm{R}-\mathrm{F} \\ & \mathrm{C} 4-1 / \mathrm{R}-\mathrm{TO}-51 \mathrm{P} 1-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-511 \mathrm{P}-\mathrm{F} \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { A4A 4R6 } \\ & A 4 A 4 R 7 \\ & A 4 A 4 R 8 \\ & A 4 A 4 R 9 \\ & A 4 A 4 R 10 \end{aligned}$ | $0757-0394$ $0698-0082$ $0757-0278$ $0757-0441$ $0698-3153$ |  | RESISTOR 51.1 OHM $1 \%$ .125 W F TUBULAR <br> RESISTOR 464 OHM $1 \%$ 125 W F TUBULAR  <br> RESISTOR 1.78 K $1 \%$ .125 W FUBULAR  <br> RESISTOR $8.25 K$ $1 \%$ .125 F F TUBULAR  <br> RESISTOR 3.83 K $1 \%$ .125 W F TUBULAR  | $\begin{aligned} & 24546 \\ & 16299 \\ & 24546 \\ & 24546 \\ & 16299 \end{aligned}$ | $C 4-1 / 8-T 0-51 R 1-F$ $C 4-1 / 8-T 0-4640-F$ $C 4-1 / 8-T 0-1781-F$ $C 4-1 / 8-T 0-8251-F$ $C 4-1 / 8-T 0-3831-F$ |
|  | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0757-0442 \\ & 0698-3440 \\ & 0698-0083 \\ & 0757-0422 \end{aligned}\right.$ |  | RESISTOR 1OK 1\% . 125W F TUBULAR RESISTOR 1OK 1\% . 125 W F TUBULAR RESISTOR 196 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 1.96K 1\% .125W F TUBULAR RESISTOR 909 OHM $1 \%$. 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16299 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-196 R-F \\ & C 4-1 / 8-T 0-1961-F \\ & C 4-1 / 8-T 0-909 R-F \end{aligned}$ |
|  | $\left\lvert\, \begin{aligned} & 0757-0401 \\ & 0757-1094 \\ & 0698-3434 \\ & 0757-0398 \\ & 0764-0033 \end{aligned}\right.$ | 8 3 1 | RESI STOR 100 OHM $1 \%$. $125 W$ F TUBULAR RESISTOR 1.47K 1\% .125W F TUBULAR RESISTOR 34.8 OHM 1\% . 125 H F TUBULAR RESISTOR 75 OHM 1\% . 125W F TUBULAR RESISTIR 33 OHM 5\% 2W MO TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-101-F \\ & C 4-1 / 8-T 0-1471-F \\ & C 4-1 / 8-T 0-34 R 8-F \\ & C 4-1 / 8-T 0-75 R 0-F \\ & \text { FP42-2-T00-3302-J } \end{aligned}$ |
| $\begin{aligned} & A \text { AA 4R } 21 \\ & A 4 A \text { 4R } 22 \\ & A 4 A 4 R 23 \\ & A 4 A 4 R 24 \\ & A 4 A 4 R 25 \end{aligned}$ | $\begin{aligned} & 0757-0441 \\ & 0698-3153 \\ & 0698-3440 \\ & 0757-0441 \\ & 0698-3153 \end{aligned}$ |  | RESISTOR 8.25K 1\% .125W F TUBULAR RESISTOR 3.83K 1\% .125W F TUBULAR RESISTOR 196 OHM 1 \% . 125 W F TUBULAR RESISTOR 8.25K 1\% .125W F TUBULAR RESISTOR 3.83K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 15299 \\ & 16299 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-8251-F \\ & C 4-1 / 8-T 0-3831-F \\ & C 4-1 / 8-T O-I 96 R-F \\ & C 4-1 / 8-T 0-8251-F \\ & C 4-1 / 8-T 0-3831-F \end{aligned}$ |
| $\begin{aligned} & A 4 A 4 R 26 \\ & A 4 A 4 R 27 \\ & A 4 A 4 R 2 B \\ & A 4 A 4 R 29 \\ & A 4 A 4 R 30 \end{aligned}$ | $\left\lvert\, \begin{array}{r} 0757-0394 \\ 0698-3155 \\ 0698-3155 \\ 0698-3440 \\ 0757-0401 \end{array}\right.$ | 15 | RESISTOR 51.1 OHM 1\% . 125 F F TUBULAR RESISTOR $4.64 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR PESISTOR 4.64K 1\% .125W F TUBULAR RESISTOR 196 OHM 1\% . 125 W F TUBULAR RESISTOR 100 OHM $1 \%$. 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 16299 \\ & 15299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-T 0-4641-F \\ & C 4-1 / 8-T 0-4641-F \\ & C 4-1 / 8-T 0-196 R-F \\ & C 4-1 / 8-T 0-100 R-F \end{aligned}$ |
| $\begin{aligned} & A 4 A \text { 4R } 31 \\ & \text { A4A 4R } 32 \end{aligned}$ | $\left\lvert\, \begin{array}{r} 0757-0422 \\ 0698-7195 \end{array}\right.$ | 1 | RESISTOR 909 OHM 1\% . 125W F TUBULAR RFSISTOR 19.6 OHM 2\% .05W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-909 R-F \\ & C 3-1 / 8-T 00-19 R 6-G \end{aligned}\right.$ |
| A4A4U1 | 1820-0714 | 1 | IC DGTL PRESCALER | 28480 | 1820-0714 |
| A4A 5 | 08660-60005 | 1 | BOARD ASSY, VCO \& AMPLIFIFRS | 28480 | 08660-60005 |
| $A 4 A 5 C 1$ | $0160-3878$ | 21 | CAPACITOR-FXO 1000PF +-20\% 100WVDC CER CAPACITDR-FXD 1000 PF +-20\% 100WVOC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-3878 \\ & 0160-3878 \end{aligned}$ |
| A4A 5C 3 | 0121-0452 | 2 | CAPACITOR; VAR; TRMR; AIR; $1.3 / 5.4 P \mathrm{~F}$ | 74970 | 187-0103-005 |
| A 4 A 5C4 | 0160-3878 |  | CAPACITDR-FXD 1000 PF +-20\% 100 WVDC CER | 28480 | 0160-3878 |
| A4A5C5 | 0160-3878 |  | CAPACITOR-EXD 1000PF +-20\% 100WVDC CER | 28480 | 0150-3878 |
| A4A 5C 6 <br> A4A 5C. 7 <br> $A 4 \Delta 5 C 8$ <br> A4A 5C 9 <br> A4A5C10 | $\left\lvert\, \begin{array}{lll} 0 & 160-2250 \\ 0 & 160-2266 \\ 0 & 160-2266 \\ 0 & 160-3878 \\ 0 & 160-3878 \end{array}\right.$ | 2 | CAPACITOR-FXD 5.1PF +-.25PF 500WVOC CER CAPACITOR-FXD 24PF +-5\% 500WVDC CER 0+ CAPACITOR-FXD 24PF +-5\% 500WVDC CER 0+ CAPACITOR-FXD 1000PF +-20\% 100WVDC CER CAPACITOR-FXD 1000 PF +-20\% 100 WVOC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2250 \\ & 0160-2266 \\ & 0160-2266 \\ & 0160-3878 \\ & 0160-3878 \end{aligned}$ |
| A4A 5C11 | 0160-3878 |  | CAPACITOR-FXD 1000PF +-20\% 100WVDC CER | 28480 | 0160-3878 |
| A4A 5C, 12 | 0160-3978 |  | CAPACITOR-FXD 1000 PF +-20\% 100WVDC CER | 28480 | 0160-3878 |
| A4A5C13 | 0160-2266 |  | CAPACITOR-FXD 24PF +-5\% 500WVDC CER $0+$ | 28480 | 0160-2266 |
| A4A 5C14 | 0 160-2266 |  | CAPACITMR-FXD 24PF +-5\% 500WVIC CER 0+ | 23480 | 0160-2266 |
| A4A 5C. 15 | 0160-3878 |  | CAPACITOR-FXD 1000PF +-20\% 100WVDC CER | 28480 | 0160-3878 |
| $\begin{aligned} & A 4 A 5 C 16 \\ & A 4 A 5 C 17 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0160-3878 \\ & 0160-3878 \end{aligned}\right.$ |  | CAPACITIR-FXD 1000PF +-20\% 100WVDC CER CAPACITOR-FXD 1000PF +-20\% 100WVDC CER | 28480 28480 | $\begin{aligned} & 0160-3878 \\ & 0160-3879 \end{aligned}$ |
| A4A5C.18 | 0160-3878 |  | CAPACITDR-FXD 1000PF +-20\% 100WVDC CER | 28480 | 0160-3878 |
| A 4A 5C. 19 | 0 160-2266 |  | CAPACITOR-FXD 24PF +-5\% 500WVOC CER O+ | 28490 | 0160-2265 |
| A4A5C20 | 0160-2266 |  | CAPACITOR-FXD 24PF +-5\% 500WVOC CER 0+ | 28480 | 0160-2266 |
| $\begin{aligned} & A 4 A 5 C 21 \\ & A 4 A 5 C 22 \\ & A 4 A 5 C 23 \\ & A 4 A 5 C 24 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0 & 160-3878 \\ 0 & 160-3878 \\ 0 & 160-3879 \\ 0 & 160-3878 \end{array}\right.$ |  | CAPACITOR-FXD 1000PF +-20\% 100WVDC CER CAPACITOR-FXD 1000PF +-20\% 100WVDC CER CAPACITOR-FXD 1000PF +-20\% 100WVDC CER CAPACITOR-FXD 1000PF +-20\% 100WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-3878 \\ & 0160-3878 \\ & 0160-3878 \\ & 0160-3879 \end{aligned}$ |
| $\begin{aligned} & A 4 A 5 C R 1 \\ & A 4 A 5 C R 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0122-0248 \\ & 1901-1034 \end{aligned}\right.$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | DIO-VVC 1N5140A 10 PF 5\% C. $4 / \mathrm{C} 60=2800000$ DIDDE-STABISTOR 9OV | $\begin{aligned} & 04713 \\ & 03508 \end{aligned}$ | $\begin{aligned} & \text { 1N5140n } \\ & \text { MPO400 } \end{aligned}$ |
| A4A5FLI | 08660-20038 | 1 | FILTFR, L.P. 500 MHz | 28480 | 08660-20038 |
| $\text { A4A 5L } 1$ |  |  | PART OF PRINTFD CIRRCUIT RTARD |  |  |
| $A 4 A 5 L 12$ $A 4 A 5 L 3$ | $9100-2250$ $09650-80006$ | $\begin{aligned} & 7 \\ & 4 \end{aligned}$ | CCIL: FXD: MOLDE INDUCTOR INS CHOKF; - $18 U H$ 10\% | 24226 | $\left\lvert\, \begin{aligned} & 10 / 180 \\ & 08660-80006 \end{aligned}\right.$ |
| A4A5L4 | 08660-80006 |  | INDUCTOR | 28430 | 08660-80006 |
| A 4A5L5 | 9100-2250 |  | COIL: FXC; MOLDED RF CHOKE; . 18 8JH $10 \%$ | 24226 | $10 / 180$ |
| $\begin{aligned} & A 4 A 5 L 6 \\ & A 4 A 5 L 7 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 9100-2250 \\ & 08660-80006 \end{aligned}\right.$ |  | COIL: EXD; MOLDED RF CHOKE; . 18 BUH 10\% INDUCTOR | $\begin{aligned} & 24226 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 10 / 180 \\ & 08650-80006 \end{aligned}$ |
| A4A5LA | 0 8660-80006 |  | INDUCTOR | 28480 | 08660-80006 |
| A4A5L9 A 4 A 5 LCL | $9100-2250$ $9100-2250$ |  | COIL ; FXD; MCLDED RF CHCKE: . $18 \mathrm{UHH} 10 \%$ COIL ; FXD; MOLDED RE CHOKE; 18 (UH $10 \%$ | 24226 24226 | $10 / 180$ $10 / 180$ |
| A4A5L10 | $9100-2250$ |  | COIL: FXD; MOLDED RE CHOKE: . 18 UUH $10 \%$ | 24226 | 10/180 |
| $\begin{aligned} & \text { A } 4 A 5 L 11 \\ & \text { A } 4 A 5 L .12 \end{aligned}$ | $\left\lvert\, \begin{array}{\|c} 08650-80009 \\ 08660-80009 \end{array}\right.$ |  | INDUCTITR <br> INDUCTRR | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-80009 \\ & 08660-80009 \end{aligned}\right.$ |
| A405L13 | 9100-2250 |  | COIL ; FXD; MOLDED RF CHOKE: . 18 UH (10\% | 24226 | $\begin{aligned} & 08060-8 \\ & 10 / 180 \end{aligned}$ |
| A4A5L 14 | $9100-2250$ |  |  | 24226 | 101180 |
| A44501 | 1854-0431 |  | TRANSISTOF NPN $2 N 5179$ SI TD-72 DD $=200 \mathrm{MW}$ | 02735 | 2N5179 |
| A44502 | 1854-0431 |  | TRANSISTOR NPN 2 N5 179 SI TO-72 On= 200 MW | 02735 | 2N5179 |
| 444503 | 1854-0431 |  | TRANSISTRE NPN 2 N5 179 SI TO-72 PD $=200 \mathrm{MW}$ | 02735 | 2N5179 |
| A44504 | 1854-0540 |  | TRANSISTOP NPN SI TT-72 PD $=200 \mathrm{MW}$ | 28480 | 1854-0540 |
| A4A505 | 1354-0431 |  | TRANSISTOR NPN 2 N5 179 SI TO-72 DO $=200 \mathrm{MW}$ | 02.735 | 2N5179 |

Table 6-3. Replaceable Parts


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Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & A 4 A 7 C 6 \\ & A 4 A 7 C 7 \\ & A 4 A 7 C 8 \\ & A 4 A 7 C 9 \\ & A 4 A 7 C 10 \end{aligned}$ | $\begin{aligned} & 0180-2214 \\ & 0180-0049 \\ & 0160-3878 \\ & 0160-0839 \\ & 0160-3064 \end{aligned}$ | 1 |  | $\begin{aligned} & 56289 \\ & 56289 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $300906 G 016 \mathrm{CC2}$ 300206 G 050 C 2 $0160-3878$ $0160-0839$ $0160-3064$ |
| $\begin{aligned} & A 4 A 7 C 11 \\ & A 4 A 7 C 12 \\ & A 4 A 7 C 13 \\ & A 4 A 7 C 14 \\ & A 4 A 7 C 15 \end{aligned}$ |  | 2 1 | CAPACITOR-FXD 47PF +-58 300WVDC MICA CAPACITOR-FXD 47PF +-5\% 300WVDC MICA CADACITOR-FXD 5.1PF +-.25PF 500WVDC CER CAPACITDR-FXD 24 PF $+-5 \%$ 500WVOC CER O+ CAPACITOR-FXD; 1.5UF+-10\% 20VDC TA | $\begin{aligned} & 28430 \\ & 28490 \\ & 28480 \\ & 28480 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 0160-0182 \\ & 0160-0182 \\ & 0160-2250 \\ & 0160-2266 \\ & 1500155 \times 9020 A 2 \end{aligned}$ |
| $\begin{aligned} & A 4 A 7 C 16 \\ & A 4 A 7 C 17 \\ & A 4 A 7 C 18 \\ & A 4 A 7 C 19 \\ & A 4 A 7 C 20 \end{aligned}$ | $\begin{aligned} & 0180-2266 \\ & 0 \\ & 0 \\ & 0 \\ & 160-2264 \\ & 0180-0291 \\ & 0 \\ & 0 \end{aligned} 180-02910 \text {-0291 }$ | 16 | CAPACITOR-FXD 24 PF +-5\% 500WVDC CER 0+ CAPACITMR-FXD 2OPF t-5\% 500WVDC CER 0+ CAPACITDR-FXD; $1 U F+10 \%$ 35VDC TA-SOLID CAPACITOR-FXD; 1UF+-10\% 35VOC TA-SOLID CAPACITOR-FXD; $1 U F+=10 \%$ 35VDC TA-SOLID | $\begin{aligned} & 28480 \\ & 29480 \\ & 56289 \\ & 56299 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 0160-2766 \\ & 0160-2264 \\ & 1500105 \times 9035 A 2 \\ & 150105 \times 9035 A 2 \\ & 1500105 \times 9035 A 2 \end{aligned}$ |
| $\begin{aligned} & A 4 A 7 C 21 \\ & A 4 A 7 C 22 \\ & A 4 A 7 C 23 \\ & A 4 A 7 C 24 \\ & A 4 A 7 C 25 \end{aligned}$ | $\begin{aligned} & 0180-0197 \\ & 0180-0291 \\ & 0180-0197 \\ & 0180-0291 \\ & 0180-0183 \end{aligned}$ |  | CAPACITOR-FXD; 2.2UF+-10\% 20VOC TA CAPACITOR-FXD; 1UF +-10\% 35VDC TA-SOLID CAPACITOR-FXD; 2.2UF+-10\% 20VOC TA CAPACITOR-FXD; 1UF $+10 \%$ 35VDC TA-SOLID CAPA .ITOR-FXD; 10UF+75-10\% 50VDC AL | 56289 56289 56289 56289 56289 | $\begin{aligned} & 1500225 \times 902042 \\ & 1500105 \times 9035 \mathrm{~A} 2 \\ & 1500225 \times 9020 \mathrm{~A} 2 \\ & 1500105 \times 9035 \mathrm{~A} 2 \\ & 3001065050 \mathrm{CB} \end{aligned}$ |
| A4A7C26 | 0160-2266 |  | CAPACITDR-FXD $24 \mathrm{PF}+\boldsymbol{+ 5 8} 500 \mathrm{WVOC}$ CER $0^{+}$ | 28480 | 0160-2266 |
| $\begin{aligned} & \text { A4A 7CR1 } \\ & \text { A4A 7CR2 } \\ & \text { A4A 7CR } \\ & \text { A4A 7CR } \\ & \text { A4A7CR5 } \end{aligned}$ | $\begin{aligned} & 1901-0189 \\ & 5080-0271 \\ & 5080-0271 \\ & 5080-0271 \\ & 5080-0271 \end{aligned}$ | $\begin{aligned} & 1 \\ & 4 \end{aligned}$ | DIODE-STEP RCVY 20 V <br> DIODE: SILICON MATCHED QUAD <br> DI ODE:SILICON MATCHEO QUAD <br> DIODE:SILICON MATCHED QUAD <br> DIODE:SILICDN MATCHED QUAD | 28480 <br> 28480 <br> 28480 <br> 28490 <br> 28480 | $\begin{aligned} & 1901-0189 \\ & 5080-0271 \\ & 5080-0271 \\ & 5080-0271 \\ & 5080-0271 \end{aligned}$ |
| A4A 7CR6 <br> A4A 7CR 7 <br> A4A7CR8 <br> A4A 7CR 9 <br> A4ATCR10 | $\begin{array}{r} 1902-0041 \\ 1902-0041 \\ 1902-0041 \\ 1902-0041 \\ 1901-0033 \end{array}$ |  | OIODE-2NR 5.11V 5\% DO-7 PD=.4W TC= DIODE-ZNR 5.11V 5\% DO-7 PD=.4W TC= DIODE-ZNR 5.1IV 5\% DD-7 PD=.4W TC= DIODE-ZNR 5.11V 5\% DD-7 PD=.4W TC= DIDDE-GEN PRP 180 V 200MA | $\begin{aligned} & 04713 \\ & 04713 \\ & 04713 \\ & 04713 \\ & 28480 \end{aligned}$ | $\begin{array}{ll} S Z & 10939-98 \\ S Z & 10939-98 \\ S Z & 10939-98 \\ S Z & 10939-98 \\ 1901-0033 \end{array}$ |
| A4A7J1 | 1250-0836 | 1 | CONNECTIR-RF SMC M PC | 2K497 | CD-700141 |
| A4ATLI <br> A4A7L2 <br> A4ATl 3 <br> A4ATL4 <br> A4ATL5 | $\begin{aligned} & 9140-0144 \\ & 9140-0210 \\ & 9140-0210 \\ & 9100-2260 \\ & 9100-2254 \end{aligned}$ | 2 | COIL: EXD; MOLDED RF CHOKF; 4.7IIH 10 名 <br> COIL: FXD; MOLDED RF CHOKE; 100UH 5\% <br> COIL: FXD: MOLOED RF CHOKE: 100 IJH 5\% <br> COIL: FXD; MOLDED RF CHCKE; 1.8UH 10\% <br> COIL: FXD: MOLDED RF CHOKE; . 39 UH 10\% | $\begin{aligned} & 24226 \\ & 24226 \\ & 24226 \\ & 76493 \\ & 24226 \end{aligned}$ | $\begin{aligned} & 10 / 471 \\ & 15 / 103 \\ & 15 / 103 \\ & 9230-26 \\ & 10 / 390 \end{aligned}$ |
| $\begin{aligned} & A 4 A 7 L 6 \\ & A 4 A 7 L T \end{aligned}$ | 08660-80005 | 2 | INDUCTOR I NDUCTOR | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-80005 \\ & 08660-80005 \end{aligned}$ |
| $\begin{aligned} & A 4 A 701 \\ & A 4 A 702 \\ & A 4 A 703 \\ & A 4 A 704 \\ & A 4 A 705 \end{aligned}$ | $\begin{aligned} & 1854-0019 \\ & 1854-0019 \\ & 1853-0034 \\ & 1855-0049 \\ & 1853-0007 \end{aligned}$ | 9 3 | TRANSISTOR NPN SI TO-18 PR=360MH TRANSISTOR NPN SI TO-18 PD=360MW TRANSISTOR PNP SI CHIP TO-18 PD=360MW TRANSISTOR; JFET;DUAL; N-CHAN D-MODE SI TRANSISTGR PNP $2 N 3251$ SI CHIP | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 04713 \end{aligned}$ | $\begin{aligned} & 1854-0019 \\ & 1854-0019 \\ & 1853-0034 \\ & 1855-0049 \\ & 2 \text { N3251 } \end{aligned}$ |
| A44706 | 1854-0023 | 1 | TRAYSISTOR NPN SI TO-18 PD=360MN | 28480 | 1854-0723 |
| A4A 7R 1 <br> A4A 7R 2 <br> A4A 7R 3 <br> A4A7R4 <br> A4A 7R 5 | $\begin{aligned} & 0757-0398 \\ & 0698-0084 \\ & 0757-0280 \\ & 0698-3440 \\ & 0757-0346 \end{aligned}$ |  | RESISTOR 75 OHM 1\% . 125W F TURULAR RESISTOR 2.15K 1\% . 125 W F TIJBULAR RESISTOR 1K 1\% . 125 W F TUBULAR RESISTOR 196 OHM $1 \%$. 125W F TUBULAR RESISTOR 10 OHM 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 24546 \\ & 16290 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-75 R 0-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} 2151-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-1001-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-106 R-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-10 R 0-F \end{aligned}$ |
| A4A 7R 6 <br> A4ATR7 <br> A4ATR 8 <br> A4A 7R 9 <br> A4A 7R 10 | $\begin{aligned} & 0698-3437 \\ & 0698-3443 \\ & 0757-0346 \\ & 0698-0034 \\ & 0757-0280 \end{aligned}$ | 5 | RESISTOR 133 DHM 1\% •125W F TUBULAR RFSISTOR 287 OHM 1\% . 125W F TUBULAR RESISTOR 10 OHM 1\% . 125W F TUBULAR RESISTOR 2.15K 1\%.125W F TUBULAR RESISTOR 1K 1\% . 125 F F TUBULAR | $\begin{aligned} & 16299 \\ & 16290 \\ & 24546 \\ & 15259 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-133 R-F \\ & C 4-1 / 8-T 0-287 R-F \\ & C 4-1 / 8-T 0-10 R 0-F \\ & C 4-1 / 8-T 0-2151-F \\ & C 4-1 / 8-T 0-1001-F \end{aligned}$ |
| A4A7R11 <br> A4A7R12 <br> A4A7R 13 <br> A4A 7R 14 <br> A4A7R15 | $\begin{aligned} & 0757-0276 \\ & 0898-3438 \\ & 0757-0394 \\ & 0757-0394 \\ & 0757-0394 \end{aligned}$ | 1 | RESISTOR 61.9 OHM 1\% . 125W F TUBULAR RESISTOR 147 OHM 1\%. 125 W F TUBULAR RESISTOR 51.1 OHM 1\% . 125W F TUBULAR RESISTCR 51.1 OHM 1\% . 125 W F TUBULAR RESISTOR 51.1 OHM 1\% . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 18299 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C .4-1 / 8-T 0-6192-F \\ & C 4-1 / 8-T 0-147 R-F \\ & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-T 0-51 R 1-F \end{aligned}$ |
| A 4 A 7816 <br> A4A7P 17 <br> A4ATR 18 <br> A4ATR 19 <br> A4A7R20 | $\begin{aligned} & 0757-0280 \\ & 0757-0280 \\ & 2100-1986 \\ & 0757-0394 \\ & 0757-0394 \end{aligned}$ |  | RESISTOR 1K 1男 . 125W F TUBULAR RESISTOR 1K 1\% . 125W F TUBULAR RESISTOR: VAR; TRMR; IKCHM 10\% C RESISTOR 51.1 nHM 1\%. 125W F TUBULAR RESISTOR 51.1 OHM 1\%. 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 30983 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1001-F \\ & C 4-1 / 8-T 0-1001-F \\ & \text { FT50W102 } \\ & \text { C4-1/8-TO-51R1-F } \\ & C 4-1 / 8-T 0-51 R 1-F \end{aligned}$ |
| A4A7R 21 <br> A4A7R 22 <br> A4A7R 23 <br> A4A7R24 <br> A4A 7R 25 | $\begin{aligned} & 0757-0442 \\ & 2100-1986 \\ & 0757-0442 \\ & 0757-0401 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 10K 1\% . 125W F TUBULAR RFSISTOR: VAR; TRMR: IKOHM 1O\% C RESISTOR 10K 1\% . 125 W F TURULAR RESISTOR 100 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RFSISTDR 10K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 30983 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-TO- } 1002-F \\ & \text { ET50W102 } \\ & \text { C4-1/8-T0-1 002-F } \\ & \text { C4-1/8-T0-1 01-F } \\ & \text { C4-1/B-T0-1002-F } \end{aligned}$ |
| A4A 7R 26 <br> A4A7R 27 <br> A4A7R28 <br> $\triangle 4 A 7 P 29$ <br> A4A7R 30 | $\begin{aligned} & 0757-1094 \\ & 0757-0394 \\ & 0757-0401 \\ & 0898-3445 \\ & 0757-0394 \end{aligned}$ |  | RESISTOR 1.47K 17. 125 W F TUBULAR RESISTOR 51.1 OHM 1\%. 125W F TUBULAR RESISTOR 100 OHM 1\%.125W F TUBULAR RFSISTOP 348 OHM 19.125 W F TUPULAR RESISTOR 51.1 OHM 1\%. 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / B-T 0-1471-F \\ & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-T 0-101-F \\ & C 4-1 / 8-T 0-34 R R-F \\ & C 4-1 / 8-T 0-51 R 1-F \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & A 4 A 7 R 31 \\ & A 4 A 7 R 32 \\ & A 4 A 7 R 33 \\ & A 4 A 7 R 34 \end{aligned}$ | $\begin{aligned} & 0898-3445 \\ & 0698-3101 \\ & 0757-0416 \\ & 0757-0394 \end{aligned}$ | 1 |  | $\begin{aligned} & 16299 \\ & 03888 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-T0-348R-F } \\ & \text { PME 65-1/2-T0-2871-F } \\ & \text { C4-1/8-T0-511R-F } \\ & \text { C4-1/8-T0-51R1-F } \end{aligned}$ |
| $\begin{aligned} & A 4 A 7 T 1 \\ & A 4 A T T 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-80011 \\ & 08660-80010 \end{aligned}\right.$ | $1$ | TR ANSF ORMER, TRIFI LAR TRANSFORMER B BIFILAR | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-80011 \\ & 08660-80910 \end{aligned}$ |
| A5 | 08660-60023 | 1 | BOARD ASSY, REGULATOR | 28480 | 08660-60023 |
| $\triangle 5 C 1$ $\triangle 5 C 2$ | $\begin{aligned} & 0180-0291 \\ & 0180-0291 \end{aligned}$ |  | CAPACITOR-FXD; 1UF +-10\% 35VDC TA-SOLID CAPACITOR-FXD; 1UF +-10\% 35VDC TA-SOLID | $\begin{aligned} & 56289 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 1500105 \times 9035 A 2 \\ & 1500105 \times 9035 A 2 \end{aligned}$ |
| $\triangle 5 \mathrm{C} 3$ | 0180-0291 |  | CAPACITOR-FXD; 1UF+10\% 35VDC TA-SOLID | 56289 | $1500105 \times 9035 \mathrm{~A} 2$ |
| ${ }^{\text {A } 5 C 4}$ | 0180-0291 |  | CAPACITOR-FXD; 1UF +-10\% 35VDC TA-SOLID | 56289 | $1500105 \times 9035 \mathrm{~A} 2$ |
| A5C5 | 0160-2207 | 1 | CAPACITOR-FXD 300PF +-5\% 300WVDC MICA | 28480 | 0160-2207 |
| $\triangle 5 C 6$ | 0180-1704 | 7 | CAPACITOR-FXD; 47UF+-10\% 6VDC TA-SOLID | 56289 | $1500476 \times 900682$ |
| $\triangle 5 C 7$ $A 5 C 8$ | 0 180-0374 | 5 | CAPACITOR-FXD; 10UF+-10\% 2OVDC TA-SOLID | 55289 | $1500106 \times 902082$ |
| A 5C A $5 C 9$ | 0180-0291 |  | CAPACITOR-FXD: 1UF+-10\% 35VDC TA-SOLID CAPACITOR-FXD 330PF +-5\% 300WVDC MICA | 58289 28480 | $\begin{aligned} & 1500105 \times 9035 A 2 \\ & 0160-2208 \end{aligned}$ |
| A5C 10 | 0180-1704 |  | CAPACITOR-FXD; $47 \mathrm{UF+-10} \mathrm{\%}$ GVOC TA-SOLID | 56289 | $1500475 \times 900682$ |
| A5C11 |  |  | NOT ASSIGNED |  |  |
| $\triangle 5 C 12$ | 0160-2218 |  | CAPACITOR-FXD 1000 PF +-5\% 300WVDC MICA | 28480 | 0160-2218 |
| A5C13 A5C14 | 0180-0291 |  | CAPACITOR-FXD; CAF | 56289 56289 | $1500105 \times 903542$ $1500476 \times 900682$ |
| A5C15 | 0180-0269 | 2 | CAPACITOR-FXD; 1UF+75-108 150VDC AL. | 56289 | 3001056150842 |
| A $5 C 16$ $A 5 C 17$ |  |  | NOT ASSIGNED |  |  |
| A 5 Cl 18 | 0160-2218 |  | CAPACITOR-FXD; 1UF+75-10\% 150VDC AL | 284889 | 0160-2218 3051508 C |
| A5C19 | 0180-0058 | 14 | CAPACITOR-FXD; 50UF+75-10\% 25VDC AL | 55289 | 3005065025ct2 |
| A 5CR1 | 1902-3104 | 2 | DIODE-ZNR 5.62V 5\% DO-7 PD=.4W | 04713 | SZ 10939-110 |
| A 501 | 1853-0037 | 5 | TRANSISTOR PNP SI CHIP TO-39 PD= 14 | 28480 | $\begin{aligned} & 1853-0037 \\ & 1853-0050 \end{aligned}$ |
| A 502 A 503 | $1853-0050$ $1853-0037$ | 17 | TRANSISTOP PNP SI CHIP TO-18 TRANSIS $=360 \mathrm{MW}$ TRANS | 28480 28480 | $1853-0059$ $1853-0037$ |
| A 504 | 1853-0050 |  | TRANSISTOD PNP SI CHIP TO-18 PD=360MW | 28480 | 1853-0050 |
| A 505 | 1853-0037 |  | TRANSISTOR PNP SI CHIP TO-39 PD=1W | 28480 | 1853-0037 |
| A 506 | 1853-0326 | 1 | TRANSISTOP PNP SI CHIP PD=1H FT $=50 \mathrm{MHZ}$ | 28480 | 1853-0326 |
| A 5R1 A 5 2 2 | \|0757-0397 |  | RESISTOR 68.1 OHM 1\% . 125N F TUBULAR RESISTOR 10 DHM 17.125 W F TUBULAR | 24546 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-68 R 1-F \\ & C 4-1 / 8-T 0-10 R 0-F \end{aligned}\right.$ |
| A 5R 3 | 0698-3132 |  | RESISTOR 261 JHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 16299 | C4-1/8-T0-2610-F |
| A 5R. 4 | 0757-0397 |  | RESISTOR 68.1 OHM 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-68R1-F |
| A5R 5 | 0757-0397 |  | RESISTOR 68.1 OHM 1\% . 125 NF F TUBULAR | 24546 | C4-1/8-T0-58R1-F |
| $\triangle 5 R 6$ $A 5 R 7$ | 0757-0398 |  | RESISTOR 75 OHM 1\% . 125W F TUBULAR | 24546 24546 |  |
| A SR 7 A 588 | 0757-0280 $0757-0401$ |  | $\begin{array}{lll}\text { RESISTOR } & 1 K & 1 \% \\ \text { RESISTOR } & 100 \text { OHM } 125 \mathrm{~W} & \text { F TUBULAR } \\ \text { RESISTOR } & 125 \mathrm{~W} & \mathrm{~F} \text { TUBIJLAR }\end{array}$ | 24546 24546 | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / \mathrm{S}-\mathrm{T} 0-1001-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-101-\mathrm{F} \end{aligned}\right.$ |
| A5R9 | 0757-0397 |  | RESISTOR 68.1 OHM 17.125 W F TUBULAR | 24546 | C4-1/8-T0-68R1-F |
| A5R 10 | 0698-0082 |  | RESISTOR 464 OHM 1\%.125W F TUBULAR | 15299 | C4-1/8-T0-4640-F |
| A $5 R 11$ $A 5 R 12$ | 0757-0442 |  | RESISTOR 10K 1\%. 125 W F TUBULAR | 24546 |  |
|  | $0757-0280$ $0757-0394$ |  |  | 24546 24545 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-1001-F \\ & C 4-1 / 8-T 0-51 R 1-F \end{aligned}\right.$ |
| A 5R 14 | 0698-3161 | 1 | RESISTOR 38.3K 18. 125 WF F TUBULAR | 16299 | C4-1/8-T0-3832-F |
| A5R15 | 0757-0424 | 15 | RESISTOR 1.1K 1 \% . 125 W F TUBULAR | 24546 | C4-1/8-T0-1101-F |
| A SR 16 A 517 | $\left\lvert\, \begin{aligned} & 0757-0394 \\ & 0698-3150 \end{aligned}\right.$ |  | RESISTOR 51.1 OHM 1\% . 125W F TUBULAR RESISTIR 2.37K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-T 0-2371-R \end{aligned}\right.$ |
| A 5R 18 | 0698-3150 |  | RESISTOR 2.37K 1\% .125W F TUBULAR | 15299 | C4-1/8-T0-2371-F |
| A 5R 19 | 0698-3136 | 4 | RESISTOR 17.8K 18.125 W F TUBULAR | 16299 | C4-1/8-T0-1782-F |
| A 5R 20 | 0757-1094 |  | RESISTOR 1.47K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-1471-F |
| $\begin{aligned} & A 5 P 21 \\ & A 5 P 22 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 2100-1973 \\ & 0757-0278 \end{aligned}\right.$ | 1 | RESI STOR; VAR; TRMR; 200 OHM 10\% WW RESISTOR 1.78K 1\% .125W F TUBULAR | $\begin{aligned} & 32997 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 30059-1-201 \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-1781-F \end{aligned}\right.$ |
| A 5R 23 | 0698-3152 |  | RESISTOR $3.48 \mathrm{~K} 1 \%$. 125 W F TUBULAR | 16299 | C4-1/8-T0-3481-F |
| A5R 24 | 2100-1799 | 1 | RESI STOR-VAR TRMR 500 DHM 10\% WH SIDE | 32997 | $3005 P-1-501$ |
| D 5R 25 | 0757-0428 |  | RESISTDR 1.62 K 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-1 621-F |
| $\begin{aligned} & \text { A 5R } 26 \\ & \text { A SR } 27 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 2100-2852 \\ & 0698-3155 \end{aligned}\right.$ | 1 | RESISTOR-VAR TRMR IKOHM 10\% WW SIDE ADJ RESISTOR 4.64K 1\% . 1 ?5W F TUBIILAR | $\begin{aligned} & 32997 \\ & 16299 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 3005 \mathrm{P}-1-102 \\ & \mathrm{C} 4-1 / 8-\mathrm{TO-4641-F} \end{aligned}\right.$ |
| 45R28 | 2100-1739 | 1 | RESISTOP-VAR TRMR 5 KDHM 10\% WW SIDE ADJ | 32097 | 3005D-1-502 |
| - 5P 29 | 0693-3136 |  | RESISTOR 17.8K 1\% .125W F TUBIJLAR | 16299 | C 4-1/8-T0-1782-F |
| A 501 $A 502$ | $1826-0016$ $1825-0004$ | 1 | IC LIN LM2O4H REGULATOR IC L IN LM304,H REGULATOR | 27014 27014 | $L M \geq 04 H$ lLM304H |
| A5U3 | 1820-0247 | 2 | IC LIN LM305 PFGULATOR | 27014 | LM305 |
| 4504 | 1820-0247 |  | IC LIN LM305 RFGULATOP | 27014 | LM305 |
| $\begin{aligned} & A 6 \\ & A 6 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-60276 \\ & 08660-60275 \end{aligned}\right.$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | FAN ASSY, 400 HZ (OPTION 003 ONLY) FAN ASSY, $60 H Z$ (STANDARD INSTRUMENT) | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-60276 \\ & 08650-60275 \end{aligned}\right.$ |
| A6A 1 | 08660-60024 | 1 | BIARD ASSY, PRE-REGULATIR | 28480 | 05550-60024 |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A6EIC1 | 0180-0141 |  | CAPACITOR-FXD: 50UF+75-10\% 50VDC AL | 56289 | $\begin{aligned} & 300506 G 0500 \mathrm{D2} \\ & 300506 \mathrm{G} 0500 \mathrm{n} \end{aligned}$ |
| $\triangle 6 A 1 C 2$ $A 6 A 1 C 3$ | $0180-0141$ $0180-0080$ | 1 |  | 56289 56289 | 3005066050002 $300106 F 150002$ |
| AGA1C4 | 0150-0121 | 48 | CAPACITOR-FXD .1UF +80-20\% 50WVDC CER | 28480 | 0150-0121 |
| ASAIC5 | 0150-0121 |  | CAPACITOR-FXD . $1 \mathrm{UF}+80-20850 \mathrm{WVDC}$ CER | 28480 | 0150-0121 |
| A 6A 1C6 | 0150-0121 |  | CAPACITOR-FXD .1UF +80-20\% 50WVDC CER | 28480 | 0150-0121 |
| A6A1C7 | 0 150-0121 |  | CAPACITCR-FXD -1UF +80-20\% 50WVDC CER | 28480 | 0150-0121 |
| A6A1C 8 | 0150-0121 |  | CAPACITOR-FXD .1UF +80-20\% 50WVDC CER | 28480 | 0150-0121 |
| AGA1C9 AGA $1 C 10$ | ( $\begin{aligned} & 150-0121 \\ & 0160-3679\end{aligned}$ | 2 | CAPACITOR-FXO -1UF +80-20\% 50WVIC CER CAPACITJR-FXD 1UF $+10 \% ~ 220 W V A C ~ M E T ~$ | $\begin{aligned} & 28480 \\ & 56289 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0150-0121 \\ & 439 \mathrm{P} 1059220 \end{aligned}\right.$ |
|  |  | 2 | (JPT 003 ONLY) |  |  |
| AGA1CR1 | 1902-3262 | 1 | DIODE-ZNR 24.9 V 5\% OO-7 $\mathrm{PD}=.4 \mathrm{~W}$ | 04713 | S2 $10939-296$ |
| ASAICR2 AGAICR3 | 1902-3203 | 1 | $\begin{array}{llllll}\text { DIODE-ZNR } & 14.7 \mathrm{~V} & 58 & 70-7 & \mathrm{PD}=.4 \mathrm{4} \\ \text { DIODE-ZNR } & 46.4 \mathrm{~V} & 58 & 00-7 & \mathrm{PO}=.4 \mathrm{~W}\end{array}$ | 04713 04713 | $\begin{array}{ll} \text { SZ } & 10939-230 \\ \text { SZ } & 10939-374 \end{array}$ |
| 464101 | 1854-0072 | 1 | TRANSISTOR NPN 2N3054 SI PD=25H | 02735 | 2N3054 |
| A6A 102 | 1853-0052 | 1 | TRANSISTOR PNP 2 N3740 SI CHIP PD $=25 \mathrm{~W}$ | 04713 | 2N3740 |
| AGA 103 | 1853-0037 |  | TRANSISTOR PNP SI CHIP TO-39 PD=1W | 28480 | 1853-0037 |
| A6A104 | 1854-0063 | 3 | TRANSISTOP NPN 2N3055 SI PD=115W | 28480 | 1854-0063 |
| A6A 105 | 1853-0059 | 1 | TRANSISTOR PNP 2 N3791 SI CHIP PD $=150 \mathrm{~W}$ | 04713 | 2N3791 |
| $\begin{aligned} & A G A 106 \\ & A G A 107 \end{aligned}$ | $\begin{aligned} & 1853-0037 \\ & 1854-0063 \end{aligned}$ |  | TRANSISTOR PNP SI CHIP TO-39 PDEIW TRANSISTOR NPN $2 N 3055$ SI $P D=115 \mathrm{~W}$ | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1853-0037 \\ & 1854-0063 \end{aligned}$ |
| A6A 108 | 1854-0063 |  | TRANSISTOR NPN 2N3055 SI PD=115W | 28480 | 1854-0083 |
| A6A109 | 1854-0003 | 1 | TRANSISTOR NPN SI TO-39 PD=800MW | 28480 | 1854-0003 |
| A6A 1010 | 1854-0313 | 1 | TRANSISTOR NPN 2N3771 SI PD=150W | 02735 | 2N3771 |
| $\begin{aligned} & A G A 1 R 1 \\ & A G A 1 R 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3447 \\ & 0698-3132 \end{aligned}\right.$ |  | $\begin{array}{lllllll}\text { RESISTOR } & 422 \text { OHM } & 1 \% & .125 \mathrm{~W} & \text { F TUBULAR } \\ \text { PESI STOR } & 261 & \text { OHM } & 1 \% & .125 \mathrm{~W} & \text { TUBULAR }\end{array}$ | $\begin{aligned} & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T O-422 R-F \\ & C 4-1 / 8-T O-2610-F \end{aligned}$ |
| AGAIR 3 | 0757-0274 |  | RESISTOR $1.21 \mathrm{~K} 1 \%$.125W F TUBULAR | 24546 | C4-1/8-T0-1213-F |
| A6A1R4 | 0698-3447 |  | RESISTOR 422 OHM 1\%.125W F TUBULAR | 15299 | C4-1/8-T0-422R-F |
| AGA1R 5 | 0698-3132 |  | RESISTOR 261 OHM 1\%.125W F TUBULAR | 16299 | C4-1/8-T0-2610-F |
| A SAIR 6 AGAIR | 0757-0274 |  | $\begin{array}{llllllll}\text { RESISTOR } & 1.21 \mathrm{~K} & 12 & .125 \mathrm{H} & \text { F TUBULAR }\end{array}$ | 24546 28480 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-1213-F \\ & 0812-0014 \end{aligned}\right.$ |
| AGAIR ${ }^{\text {A }}$ | 0812-0019 | 2 | RESISTOR . 33 OHM 5 5 3 WW PW TUBULAR | 28480 | CW2B-1 |
| AGA 1 R9 | 0812-0019 |  | RESISTAR -33 OHM $593 \mathrm{3H} \mathrm{PW}$ TUBULAR | 91637 | $\mathrm{CW} 2 \mathrm{~B}-1$ |
| ASAIR 10 | 0812-0020 | 1 | RESISTOR - 30 OHM 5\% 3W PW TUBULAR | 91637 | CW2B1-3-「2-39/100-J |
| A6A 1R11 | 0811-1670 | 1 | RESISTOR 2.2 OHM 5\% 2W PW TUBULAR | 75042 | BWH2-22 2-J |
| A6A1×A20-1 | 1251-1388 | 1 | CONNECTOR: PC EDGE: 15-CONT; DIP SOLDER | 71785 | 252-15-30-008 |
|  | $\left\lvert\, \begin{aligned} & 1200-0043 \\ & 0340-0162 \\ & 08660-20173 \end{aligned}\right.$ | 1 1 1 | INSULATOR; XSTR; TO- 3; . 02 THK INSULATOR; XSTR; TO- 66; . 02 THK HEAT SINK | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 1200-0043 \\ & 0340-0162 \\ & 08660-20173 \end{aligned}\right.$ |
| A6A 2 | 3160-0056 | 1 | FAN-TBAX 115-CFM 115V 50/60-HZ 1.5-THK (EXCEPT DPT 003) | 28490 | 3160-0056 |
| 4642 | 3160-0087 | 1 | FAN-TBAX 95-CFM 115 V 50/60/400-HZ 1.5 (OPT DO3 ONLY) | 28480 | 3160-0087 |
| A $6 A_{2} \mathbf{C 1}$ | 0160-3679 |  | CAPACITOR-FXD 1UF +-10\% 220WVAC MET (OPT 003 ONLY) | 56289 | 43981059220 |
|  |  |  | miscellaneous agaz. |  |  |
|  | $\left\lvert\, \begin{aligned} & 08660-00063 \\ & 08660-00064 \\ & 0403-0026 \end{aligned}\right.$ | 1 1 2 | FAN, SHIELD HEAT SINK COVER GLIDE: NYLON | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-00063 \\ & 08660-00064 \\ & 0403-0026 \end{aligned}$ |
| A 7 | 5060-9409 | 1 | POWER LINF MODULE/FILTER | 28480 | 5060-9409 |
| ATCI | 0160-4065 | 1 | CAPACITOR, FXO 0.1UF+-20\% 250WVAC PAPER | 0057R | PME 271 M 610 |
| ATF 1 ATF | $\text { 2 } 2110-0029$ | 1 | FUSE, 3A SLO-BLD (FOR 100/120 VAC) FUSE, 1.5A SLD-BLO (FOR 220/240 VACI | $\left\lvert\, \begin{aligned} & 71400 \\ & 71400 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & \operatorname{mox}-3 \\ & \operatorname{MDX}-1-1 / 2 A \end{aligned}\right.$ |
| A 7R 1 | 0839-0006 | 1 | THERMISTOR, NFG TC, 10 THM DISC | 83186 | 118212 |
| A 8 | 08660-60014 | 1 | BOARD ASSY, N3 OSCILLATOR (EXCEPT OPT 004) | 28480 | 08660-60014 |
| $\begin{aligned} & \triangle B C 1 \\ & A R C 2 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0180-0058 \\ & 0180-1704 \end{aligned}\right.$ |  | CAPACITCR-FXD; 50UF+75-10\% 25VDC AL CAPACITDR-FXD; 47UFt-10\% SVDC TA-SOLID | $\left\lvert\, \begin{aligned} & 56289 \\ & 56289 \end{aligned}\right.$ | $\begin{aligned} & 3095065025 C \mathrm{C2} \\ & 1500476 \times 9006 \mathrm{E} 2 \end{aligned}$ |
| $\triangle 8 C 3$ | 0180-0228 |  | CAPACITOR-FXD; 22UF+-10\% 15VDC TA-SJLIO | 56289 | $1500226 \times 901582$ |
| A 8C\% $\triangle 8 C 5$ | $0180-0049$ $0150-0121$ |  | CAPACITCR-FXD; $20 U F+75-10 \%$ 50VDC AL CAPACITIR-FXO - 1UF + 80-20\% 5OWYDC CER | 56289 28480 | $3002065050 C \mathrm{C} 2$ |
|  |  |  |  |  |  |
| $\begin{aligned} & A B C 6 \\ & \triangle B C 7 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0 & 160-3459 \\ 0 & 150-0121 \end{array}\right.$ | 6 | CAPACITOR-FXD .02UF +-20\% 100WVDC CER CAPACITDR-FXD . 1UF + 80-20 5 OWVDC CER | $\left\lvert\, \begin{aligned} & 28480 \\ & 23480 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & 0160-3459 \\ & 0150-0121 \end{aligned}\right.$ |
| $\triangle 8 C 8$ | 0 150-0121 |  | CAPACITOR-FXD .1UF +80-20\% 50WVOC CER | 28480 | 0150-0121 |
| $A 8 C 9$ | 0 160-3459 |  | CAPACITOR-FXD .02UF $+20 \% 100 W$ VDC CER | 23480 | 0160-3459 |
| A8C 10 | 0160-0174 |  | CAPACITOR-FXD .47UF +80-20\% 25 HVDC CER | 28480 | 0160-0174 |

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ABC11 ABC 12 A BC 13 ABC 14 A BC 15 | $\begin{aligned} & 0160-2055 \\ & 0160-0386 \\ & 0160-2204 \\ & 0170-0082 \end{aligned}$ | 15 | CAPACITOR-FXD . OIUF +80-208 10OHVIC. CER CAPACITOR-FXD 3.3PF +-.25PF 500WVOC CER CAPACITOR-FXD 100PF +-5\$ 300WVDC MICA CAPACITOR-EXD .O1UF +-208 5OWVDC POLYF not assignen | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 84411 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0160-0336 \\ & 0160-2204 \\ & 601 \text { PE1030R5W1 } \end{aligned}$ |
| ABC 16 A8C 17 A8C 18 A8C 19 A8C. 20 | $\begin{aligned} & 0160-0386 \\ & 0160-0386 \\ & 0 \\ & 0 \\ & 0 \end{aligned} 160-2055$ |  | CAPAC.ITOR-FXD 3.3PF +-.25PF 500WVDC CER CAPACITOR-FXD 3.3DF +-.25PF 500WVDC CER CAPACITOR-FXD .OIUF +80-20\% 100 WVOC CER CAPACITOR-FXD . $01 U \mathrm{~F}$ +80-20\% 100 WVDC CER CAPACITOR-FXD .OLUF +80-20\% 100 WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-0385 \\ & 0150-0385 \\ & 0150-2055 \\ & 0180-2055 \\ & 0160-2055 \end{aligned}$ |
|  | $\begin{aligned} & 0160-2055 \\ & 0160-2055 \end{aligned}$ |  | CAPACITOR-FXD. .O1UF +90-20\% 100WVDC CER CAPACITOR-FXD .OIUF +80-20\% 100 WVDC CER | $\begin{aligned} & 23480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0180-2055 \end{aligned}$ |
| A BCR1 A BCR2 A ACR | $\left\lvert\, \begin{aligned} & 1901-0040 \\ & 1901-0040 \end{aligned}\right.$ |  | DIODE-SHITCHING 2NS 30V 50MA <br> DIODE-SWITCHING 2NS 30V 50MA <br> DIO-VVC 82PF $5 \%$ C2/C $20=2000000$ MIN | $\begin{aligned} & 28480 \\ & 28490 \\ & 04713 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 1901-0040 \\ & 1901-0040 \\ & \text { SMV } 389-299 \end{aligned}\right.$ |
| A 8CR3 | 0122-0299 | 1 | D10-VVC 82PF 5\% C2/C $20=2000000$ MIN | 04713 | SMV 389-299 |
| ${ }_{\text {A BLI }}$ | 9100-1629 |  | COIL ; FXD; MOLDED RF CHOKE; 47UH 5\% | 24226 | 15/472 |
| ${ }^{\text {A BL }} 2$ | 9140-0114 | 10 | COIL: FXD; MOLDED RF CHOKE; IOUH 108 | 24226 | $15 / 102$ |
|  | $9100-1629$ $9100-1629$ |  | COIL ; FXD; COIL FXD; | 24226 24226 | $15 / 472$ $15 / 472$ |
| A 8L 5 | 9100-2815 | 5 | COIL ; FXD; NON-MOLDED RF CHOKE; .7UH 5\% | 28480 | 9100-2915 |
| $\left\lvert\, \begin{aligned} & A B L 6 \\ & A B L \end{aligned}\right.$ | $\begin{aligned} & 9140-0179 \\ & 9140-0179 \end{aligned}$ | 25 | COIL: FXD; MOLDED RF CHDKE; 22UH 108 COIL; FXD; MOLDFD RF CHOKE; 22UH 108 | $\begin{aligned} & 24226 \\ & 24226 \end{aligned}$ | $\begin{aligned} & 15 / 222 \\ & 15 / 222 \end{aligned}$ |
| $\begin{aligned} & A 801 \\ & A B O 2 \\ & A 803 \\ & A 803 \\ & A 804 \\ & A 805 \end{aligned}$ | $\begin{aligned} & 1854-0092 \\ & 18540345 \\ & 1853-0050 \\ & 1853-0050 \\ & 1853-0050 \end{aligned}$ | 32 | TRANSISTOR NPN SI PD $=200 \mathrm{MN}$ FT $=600 \mathrm{MHZ}$ TRANSISTOR NPN 2N5 179 SI $P D=200 \mathrm{MW}$ TRANSISTOR PNP SI CHIP TO-18 PD=360MW TRANSISTOR PNP SI CHIP TO-18 PD=360MH TRANSISTOR PNP SI CHIP TO-18 PD=36DMW | $\begin{aligned} & 28480 \\ & 04713 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0092 \\ & 2 N 5179 \\ & 1853-0050 \\ & 18530050 \\ & 1853-0050 \end{aligned}$ |
| A 806 A 807 A808 A809 A8010 | $\begin{aligned} & 1854-0087 \\ & 1855-0081 \\ & 1853-0007 \\ & 1853-0007 \\ & 1853-0007 \end{aligned}$ | $\begin{aligned} & 8 \\ & 5 \end{aligned}$ | TRANSISTOR NPN SI PD $=360 \mathrm{MW} \quad \mathrm{FT}=75 \mathrm{MHZ}$ TRANSISTOR: J-FET N-CHAN, D-MODE SI TRANSISTOR PNP 2N3251 SI CHIP TRANSISTOR PNP $2 N 3251$ SI CHIP TRANSISTOR PNP $2 N 3251$ SI CHIP | $\begin{aligned} & 28480 \\ & 01295 \\ & 04713 \\ & 04713 \\ & 04713 \end{aligned}$ | $\begin{aligned} & 1854-0087 \\ & \text { 2N5245 } \\ & \text { 2N3251 } \\ & \text { 2N3251 } \\ & \text { 2N3251 } \end{aligned}$ |
| $\left\lvert\, \begin{aligned} & A 8011 \\ & A 8012 \end{aligned}\right.$ | $\begin{aligned} & 1853-0007 \\ & 1854-0087 \end{aligned}$ |  | TRANSISTOR PNP 2N3251 SI CHIP <br> TRANSISTOR NPN SI PD=360MW FT $=75 \mathrm{MHZ}$ | $\begin{aligned} & 04713 \\ & 28480 \end{aligned}$ | $\begin{aligned} & \text { 2N3251 } \\ & 1854-0087 \end{aligned}$ |
| $\begin{aligned} & A 8 R 1 \\ & A B R 2 \\ & A B R 3 \\ & A B R 4 \\ & A B R 5 \end{aligned}$ | $\begin{aligned} & 0757-0428 \\ & 0757-0428 \\ & 0757-028 \\ & 0757-0428 \\ & 0757-048 \end{aligned}$ |  | NOT ASSIGNED <br> RESISTOR 1.62K 1\% . 125 W F TUBULAR <br> RESISTOR 1.62K 1\% . 125 W F TUBULAR <br> RESISTOR 1.62K 1\% . 125 W F TUBULAR <br> RESISTOR 1.62K 1\% . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-1621-F \\ & \mathrm{C} 4-1 / 8-T 0-1621-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-T 0-1621-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO-1} 621-\mathrm{F} \end{aligned}\right.$ |
| $\begin{aligned} & \text { ABR } 6 \\ & \text { A } 8 R 7 \\ & \text { A } 8 R 8 \\ & \text { A } 8 R 9 \\ & \text { A } 9 R 10 \end{aligned}$ | $\begin{aligned} & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \\ & 0757-0479 \end{aligned}$ | 5 | RESISTOR 10K 18.125W F TUBULAR RESISTOR 1OK 1\% . 125 W F TUBULAR RESISTOR 1OK 1\% .125W F TUBULAR RESISTOR 10K $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 392K 15 . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24545 \\ & 19701 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-T0-1002-F } \\ & \text { C4-1/8-T0-1002-F } \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \\ & M F 4 C 1 / B-T 0-3023-F \end{aligned}$ |
|  | $\begin{aligned} & 0757-0472 \\ & 0757-0465 \\ & 0698-3228 \\ & 0698-3155 \end{aligned}$ | 5 | RESISTOR 200K 1\%.125 F TUBULAR RESISTOR 100K 18 . 125W F TUBULAR RESISTOR 49.9K 1\% .125W F TUBULAR NDT ASSIGNED RESISTOR 4.64 K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 07716 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \text { C C - } 1 / 8-T 0-2003-F \\ & \text { C4-1/8-TO-1003-F } \\ & \text { CEA } 1 / 8-T 0-4091-F \\ & C 4-1 / 8-T 0-4641-F \end{aligned}$ |
| $\begin{array}{\|l\|l} A 8 R 16 \\ A B R 17 \\ A 8 R 18 \\ A 818 \\ A 8 R 19 \\ A R R 20 \end{array}$ | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0698-3151 \\ & 0757-0199 \\ & 0757-0200 \\ & 0757-0199 \end{aligned}\right.$ | 7 | RESISTOR 10K 1\% . 125 W F TUBULAR RESISTOR 2.87K 1\% . 125W F TUBULAR RESISTOR 21.5K 17 . 125 W F TUBULAR RESISTOR 5.62K 1\% .125W F TUBULAR RESISTOR 21.5K 1\% . 125 H F TURULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-2871-F \\ & C .4-1 / 8-T 0-2152-F \\ & C .4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-2152-F \end{aligned}$ |
| $\begin{aligned} & A B R 21 \\ & A B R 22 \\ & A 8 R 23 \\ & A B R 24 \\ & A 8 R 25 \end{aligned}$ | $\begin{aligned} & 0698-0085 \\ & 0757-0421 \\ & 0698-4037 \\ & 2100-1760 \\ & 0698-4002 \end{aligned}$ | $\begin{aligned} & 3 \\ & 6 \\ & 3 \end{aligned}$ | RESISTOR $2.61 \mathrm{~K} 1 \%$. 125 W F TUBULAR RESISTOR 825 OHM 18.125 H F TUBULAR RESISTOR 46.4 OHM 12.125 H F TUBULAR RESISTOR; VAR; TRMR; 5 KOHM 5\% WH RESISTOR 5K 18. 125W F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \\ & 16299 \\ & \text { GB027 } \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-2611-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-825 \mathrm{~F}-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-46 \mathrm{R} 4-\mathrm{F} \\ & \mathrm{CT}-106-4 \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-5001-\mathrm{F} \end{aligned}$ |
| $\begin{aligned} & \text { A BR } 26 \\ & \text { A BR } 27 \\ & \text { A 8R } 28 \\ & \text { A } 8 R 29 \\ & \text { A BR } 30 \end{aligned}$ | $\begin{aligned} & 2100-1759 \\ & 0698-3157 \\ & 0698-3158 \\ & 0698-3156 \end{aligned}$ | 5 | RESISTOR; VAR; TRMR; 2KOHM 5\% WW RESISTOR 19.6K 1\% . 125 W F TUBULAR RESISTOR 23.7K 1\% . 125 W F TUBULAR NOT ASSIGNED <br> RESISTOR 14.7K 1\% . 125 F F TUBULAR | $\begin{aligned} & G 8027 \\ & 16299 \\ & 15299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{Cr}-106-4 \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-1962-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} 2372-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} \end{aligned}$ |
| $\begin{aligned} & A 8 R 31 \\ & A 8 R 32 \\ & A 8 R 33 \\ & A 8 R 3 \\ & A 8 R 34 \\ & A 8 R 35 \end{aligned}$ | $\begin{aligned} & 0757-0441 \\ & 0757-0279 \\ & 0698-0082 \\ & 0757-0443 \\ & 0757-0199 \end{aligned}$ | 2 | RESISTOR 8.25K 1\% .125W F TUBILAR RFSISTOR 3.16K 1\% .125W F TUBULAR RESISTOR $4640 \mathrm{HH}^{1 \%}$. 125 W F TUBULAR RESISTDR 11K 18 . 125 W F TUBULAR RESISTOR 21.5K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24446 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-8251-F \\ & C 4-1 / 8-T 0-3161-F \\ & C 4-1 / 8-T 0-4640-F \\ & \mathrm{C} 4-1 / 8-T 0-1102-F \\ & \mathrm{C} 4-1 / 8-T 0-2152-F \end{aligned}$ |
| $\begin{aligned} & \text { ABR } 36 \\ & \text { A BR } 37 \\ & \text { A BR } 38 \\ & \text { A BR } 39 \\ & \text { A BR } 40 \end{aligned}$ | $0757-0442$ $0757-0401$ $0683-8245$ $0698-3243$ | $\begin{array}{r} 5 \\ 13 \end{array}$ | RESISTOR 10K 18.125 H F TUBULAR <br> NOT ASSI GNED <br> RFSISTOR 100 OHM 18.125 W F TUBIJLAR <br> RESISTOR 820K 5\% . 25W CC TUBULAR <br> RESISTOR 178K 1\%.125K F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 041121 \\ & 18299 \end{aligned}$ | $\left\{\begin{array}{l} \text { C } 4-1 / 8-\mathrm{TO} \text {-1 002-F } \\ \text { C4-1/8-T0-1 01-F } \\ \text { CB8245 } \\ \text { C } 4-1 / 8-\text { T0-1 783-F } \end{array}\right.$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A8R 41 $A 8 R 42$ $A 8 R 43$ A PR 44 $A 8 R 45$ | $0757-0442$ $0698-3440$ $0698-0082$ $0757-0200$ $0698-3154$ |  |  | $\begin{aligned} & 24546 \\ & 16299 \\ & 16299 \\ & 24546 \\ & 16299 \end{aligned}$ | $C 4-1 / 8-T 0-1002-F$ $C .4-1 / 8-T 0-196 R-F$ $C 4-1 / 8-T 0-4640-F$ $C 4-1 / 8-T 0-5621-F$ $C 4-1 / 8-T 0-4221-F$ |
| A PR 46 | 0698-3445 |  |  | $\begin{aligned} & 18209 \\ & 24546 \end{aligned}$ | C 4-1/8-T0-348R-F C $4-1 / 8-\mathrm{TO}-121 \mathrm{~F}$ |
| A BR 47 $A 8848$ A 48 | 0757-0403 | 4 |  | $\begin{aligned} & 24546 \\ & 15209 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-121 R-F \\ & C 4-1 / 8-T 0-316 R-F \end{aligned}$ |
| A88. 49 | 0698-3445 |  | RESISTOR 348 OHM 18.125 W F TUBULAR | 16209 | C4-1/8-70-348R-F |
| A 8250 | 0698-3438 |  | RESISTOR 147 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 16290 | C4-1/8-T0-147R-F |
| A 8191 A $8 \cup 2$ $A 84$ | $\begin{aligned} & 1820-0054 \\ & 1820-0054 \end{aligned}$ |  | $\begin{array}{lllll}\text { IC } & \text { OGTL } & \text { SN74 } & 00 & \text { N GATE } \\ \text { IC } & \text { DGTL } & \text { SN74 } & \text { OO } \\ \text { IC } & \text { GATE }\end{array}$ | 01295 | $\begin{aligned} & \text { SN7400N } \\ & \text { SN740ON } \end{aligned}$ |
| 4803 | 1820-0450 | 12 | IC DGTL N8290A COUNTER | 18324 | N82904 |
| $\triangle 9$ | 08660-60045 | 1 | CABLE ASSY, LOOP ROX | 28480 | 08660-60045 |
| A9W 1 | 8120-1614 | 1 | CABLE, UNSHLD 28-COND 28 AWG | 75037 | 3401 |
| A9A 1 | 08660-60037 | 1 | BDARD ASSY, OIGITAL PROGRAM | 28480 | 08650-60037 |
| A9A1F1 | 0360-1636 | 1 | TERMINAL | 76381 | 3402 |
| A9AIR1 A9A1R2 | $\left\lvert\, \begin{aligned} & 0698-7210 \\ & 0698-7210 \end{aligned}\right.$ | 28 | RESISTOR 82.5 OHM $2 \%$ .05 W F TUBULAR <br> RFSISTOR 82.5 OHM $2 \%$ .05 F F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C \text { C 3-1/8-TO 0-82R5-G } \\ & \text { C 3-1/8-T00-82R5-G } \end{aligned}\right.$ |
| A9A1R3 | 0698-7210 |  | RESISTOR 82.50 OHM 28.05 W F TUBULAR | 24546 | C3-1/8-900-8205-G |
| A9A124 | 0698-7210 |  | RESISTOR 82.5 OHM 2\%.05W F TUBULAR | 24.546 | C3-1/8-T00-82R5-G |
| A9A1R 5 | 0698-7210 |  | RESISTOR 82.5 OHM $2 \% .05 \mathrm{~W}$ F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A9A106 | 0698-7210 |  | RESISTOR 82.5 OHM 2\% . 05 W F TUBIJLAR | 24546 | $\text { C } 3-1 / 8-\text { T00- 82R.5-G }$ |
| A $941 R 7$ $A 9 A 1 R 8$ | 0698-7210 |  | RESISTOR RESISTOR 82.5 R2.5 OHM R | 24546 24546 | $\left\lvert\, \begin{aligned} & C 3-1 / 8-T 00-82 R 5-G \\ & C 3-1 / 8-T 00-82 R 5-G \end{aligned}\right.$ |
| A9A1R9 | 0698-7210 |  | RESISTOR $82.50 \mathrm{OHM} 2 \% .05 \mathrm{~W}$ F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| AgAlR10 | 0698-7210 |  | RESISTOR 82.5 OHM 2\%.05W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A9A1R11 | 0698-7210 |  | RESISTOR 82.5 OHM 2\% . 05 W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| AGA1R12 | 0698-7210 |  | RESISTOR 82.5 OHM 2\% .05W F TUBULAR | 24546 24546 | $\begin{aligned} & \text { C 3-1/8-T00-82R5-G } \\ & \text { C } 3-1 / 8-T 00-82 R 5-G \end{aligned}$ |
| A9A1R13 AGAlR14 | $0698-7210$ $0698-7210$ |  | RESISTOR 82.50 HM RESISTIR R2.5 OHM | 24546 24546 | $\left\lvert\, \begin{aligned} & \text { C 3-1/8-T00-82R5-G } \\ & \text { C 3-1/8-TOO-82R5-G } \end{aligned}\right.$ |
| A9A1R15 | 0698-7210 |  | RESISTOR 82.5 OHM 2\%.05W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| 4941216 | 0698-7210 |  | RESISTOR 92.5 OHM 2\% .05W F TUBULAR | $24546$ | $\text { C } 3-1 / 8-T 00-82 R 5-G$ |
| A 9 A 1217 ASA 18 | $0698-7210$ $0698-7210$ |  | RESISTOR RESISTOR 82.5 R | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & \text { C } 3-1 / 8-T 00-82 R 5-G \\ & \text { C } 3-1 / 8-T 00-82 R 5-G \end{aligned}\right.$ |
| A9A1R19 | 0698-7210 |  | RESISTOR 82.5 OHM 2\% .05W F TUBULAR | 24546 | C 3-1/8-T00-82R5-G |
| A9A1R20 | 0698-7210 |  | RESISTOR 82.5 OHM 2\%.05W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A9A1R21 | 0698-7210 |  | RESISTOR 82.5 DHM 2\% .05W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A9A1R22 A A A 23 | 0698-7210 |  | PESISTOR RESISTOR 82.5 R2, OHM OHM 2\% | 24546 | $\left\lvert\, \begin{aligned} & \text { C 3-1/8-T00-82R5-G } \\ & \text { C 3-1/8-TO0-82R5-G } \end{aligned}\right.$ |
| A9A1P24 | 0698-7210 |  | RESISTIR 82.5 OHM 2\% .05W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A9A1R25 | 0698-7210 |  | RESISTIR 82.50 HM 28.05 W F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| $\begin{array}{\|l\|} \hline A 9 A 1 R 26 \\ A 9 A 1 R 27 \end{array}$ | $\begin{aligned} & 0698-7210 \\ & 0698-7210 \end{aligned}$ |  | RESISTHR 82.5 OHM 2\% .05W F TUBULAR RFSISTOR 82.5 OHM 2\% .05W F TUBULAR | 24546 24546 | $C 3-1 / 8-\mathrm{TOO-82R5-G}$ $\mathrm{C} 3-1 / 8 \mathrm{~T} 00-82 R 5-\mathrm{G}$ |
| A 9 A1228 | 0698-7210 |  | RESISTOR $82.50 \mathrm{HM} 2 \% .05 \mathrm{~W}$ F TUBULAR | 24546 | C3-1/8-T00-82R5-G |
| A10 | 08660-60013 | 1 | BIAARD ASSY, N3 PHASE DETECTOR (EXCEPT OPT 004) | 28480 | 08660-60013 |
| A10Cl A10C2 | $\begin{aligned} & 0160-2055 \\ & 0 \\ & 0 \end{aligned} 160-2055$ |  | CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER CAPACITOR-FXD . OLUF +80-20\% 100WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | \|0160-2055 |
| A10C3 | $0180-0058$ |  | CAPACITOR-FXD; $50 \cup \mathrm{~F}+75-10 \% 25 \mathrm{VOC}$ AL | 56289 | 300506 O 025 C 2 |
| A 10C4 | 0180-2206 |  | CAPACITOR-FXD; 60UF+-10\% 6 VDC TA-SOLID | 56289 | $1500606 \times 900682$ |
| A10C5 | 0180-0228 |  | CAPACITJR-FXD; $22 \mathrm{UVF+-10} \mathrm{\%} \mathrm{15VDC} \mathrm{TA-SOLTD}$ | 56289 | $1500226 \times 901582$ |
| $\begin{aligned} & \text { A } 10 C 6 \\ & \text { A } 10 \mathrm{C} 7 \end{aligned}$ | $\begin{array}{llll} 0 & 1 & 50-01 & 21 \\ 0 & 150-01 & 1 \end{array}$ |  | CAPACITMR-FXD - IUF +80-20\% 50WVDC CER CAPACITOR-FXD . 1UF +80-20\% 50WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0150-0121 \\ & 0150-0121 \end{aligned}$ |
| A10c. 8 | 0160-0157 |  | CAPACITOR-FXD 4700 PF +-10\% 200WVDC POLYE | 56289 | 292P47292 |
| A10C9 | 0 160-2055 |  | CAPACITOR-FXD . OIUF +80-20\% 100 WVDC CER | 28480 | 0160-2055 |
| A10C10 | 0150-0121 |  | CAPACITOR-FXD . $1 U F+80-20 \% 50 W V D C ~ C E R ~$ | 28480 | 0150-0121 |
| $\begin{aligned} & A 10 C 11 \\ & A 10 C 12 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0 & 150-0121 \\ 0 & 160-2055 \end{array}\right.$ |  | CAPACITOR-FXD - IUF +80-20\% 50WVDC CER CAPACTTDR-FXD .O1UF +80-20\% 100WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | \|l|50-0121 |
| A 10 Cl 3 | 0140-0172 | 2 | CAPACITIR-FXD 3000 PF + -1\% 100 WVDC MICA | 72136 | DM1 9F $302 \mathrm{2FO1} 00 \mathrm{WVICR}$ |
| A 10 C.14 | 0180-0229 |  | CAPACITOR-FXD; 33UF+-10\% 10VOC TA-SOLID | 56289 | $1500336 \times 901082$ |
| A 10 Cl 5 | 0160-2055 |  | CAPACITOR-FXD . 01 l ( ${ }^{\text {+80-20\% } 100 W V D C ~ C E R ~}$ | 28480 | 0160-2055 |
| $\begin{aligned} & A 10 C 16 \\ & A 10 C 17 \end{aligned}$ | $\left\lvert\, \begin{array}{llll} 0 & 150-0 & 1 & 21 \\ 0 & 150-0 & 1 & 21 \end{array}\right.$ |  | CAPACITMQ-FXD . IUF +80-20\% 50WVOC CER CAPACITOR-FXD . 1UF + 80-20\% 50WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0150-0121 \\ 0150-0121 \end{array}\right.$ |
| A 10 Cl 18 | 0150-0121 |  | CAPACITOR-FXD . 1UF +80-20\% 50WVDC CER | 28480 | 0150-0121 |
| A10C19 | 0 160-2055 |  | CAPACITSR-FXD . $014 \mathrm{~F}+80-208100 \mathrm{WVDC} \mathrm{CER}$ | 28480 | 0160-2055 |
| A10C20 | 0160-2055 |  | CAPACITSR-FXD .OIUF +80-202 100WVDC CER | 28480 | 0160-2055 |
| $\begin{aligned} & A 10 C 21 \\ & \text { A } 10 C 22 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0 & 160-2055 \\ 0 & 160-3539 \end{array}\right.$ | 3 | CAPACITITR-FXD .OIUF +80-20\% 10OWVDC CER CAPACITOR-EXD 820PF +-5\% 100WVDC MICA | 28480 28480 | \|0160-2055 |
| A $10 C 23$ A $10 C 24$ | $0160-2453$ $0170-0040$ | $\begin{aligned} & 2 \\ & 2 \end{aligned}$ | CAPACITDR-FXD .22UF +-10\% 80WVDC POLYE CAPACITAR-FXD 047UF +-10\% 200UVDC POLYE | $\begin{aligned} & 84411 \\ & 58289 \end{aligned}$ | $\begin{aligned} & \text { HEN-238T } \\ & 292 \text { P47392 } \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A 10CR 1 | 1901-0040 |  | DIDDE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A 10 CR2 | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 504A | 28480 | 1901-0040 |
| A IOCR 3 | 1901-0179 |  | DIODE-SWITCHING 750PS 15V 50MA | 28480 | 1901-0179 |
| A LOCR 4 | 1901-0179 |  | DICDE-SWITCHING 750PS 15V 50MA | 28480 | 1901-0179 |
| A10L1 | 9100-1629 |  | COIL ; FXD: MOLDED RF CHOKE; 47UH 5\% | 24226 | $15 / 472$ |
| A101. 2 | 9140-0114 |  | COIL ; EXD; MnLOED RF CHOKE; 10UH 10\% | 24.226 | $15 / 102$ |
| A1013 | 9100-1629 |  | COIL ; FXD; MOLDED RF CHCKE; 47UH 5\% | 24226 | $15 / 472$ |
| A1014 | 9140-0179 |  | COIL ; FXD: MOLDED RF CHOKF; 22UH 10\% | 24226 | 151222 |
| A1015 | 9100-1650 | 2 | COIL ; FXD; MOLDED RF CHJKE; 68OUH 5\% | 24226 | $19 / 683$ |
| A1016 | 9140-0114 |  | COIL ; FXD; MOLDED RF CHDKE; 10UH 10\% | 24226 | $15 / 102$ |
| A1017 | 9100-1652 | 3 | COIL: FXD; MOLDED RF CHOKE; 82OUH 5\% | 24226 | $19 / 823$ |
| A 1001 | 1853-0034 |  | TRANSISTOR PNP SI CHIP TO-18 PD=36OMW | $\begin{aligned} & 28490 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1853-0034 \\ & 1853-0034 \end{aligned}$ |
| A1002 A 1003 | $1853-0034$ $1853-0034$ |  | TRANSISTOR PNO SI CHIP TO-13 PD $=360 \mathrm{MW}$ | 28480 | 1853-0034 |
| A 1004 | 1855-0049 |  | TRANSISTOR: JFET;DUAL; N-CHAN D-MODE. SI | 28480 | 1855-0049 |
| A1005 | 1854-0045 |  | TRANSISTOR NPN SI TS-18 PD=500MW | 28480 | 1854-0045 |
| A1006 | 1853-0015 |  | TRAVSISTOR PNP SI CHIP PD=200M | 28480 | $1853-0015$ |
| A 1007 | 1854-0092 |  | TRANSISTOR NPN SI P9 $=200 \mathrm{MH}$ FT $=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A10R1 | 0698-0082 |  | RESISTOR 464 OHM 1\% . 125 W F TUBULAR | 16299 | $C 4-1 / 8-T 0-4.540-F$ MF4 |
| Al0R2 | $0757-0289$ | 5 | RESISTIR 13.3K 1\% . 125 W F TUBULAR | 19701 | MF4C1/8-T0-1332-F |
| A 10 R3 | 0757-0439 |  | RESISTOR 6.81K 1\% -125N F TUBULAR | 24546 | $\mathrm{C} 4-1 / 8-\mathrm{TO-6811-F}$ |
| A10R4 | 0698-0085 |  | RESISTOR $2.61 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 16299 24546 | $\begin{aligned} & C 4-1 / 8-T 0-2611-F \\ & C 4-1 / 8-T 0-511 R-F \end{aligned}$ |
| A10R5 | 0757-0416 |  | RESISTOR 511 OHM 1\% - 125 W F TUBULAR | 24546 | C4-1/8-T0-511R-F |
| A10R6 | 0698-3446 |  | RESISTOR 383 OHM 1\%.125W F T'JBULAR | $16299$ | $C 4-1 / 8-T 0-383 R=F$ |
| Al0R7 | 0757-0424 |  | RESISTOR 1.1K 1\% . 125 W F TUBULAR | $24546$ | r:4-1/8-TO-1101-F |
| Al0R8 | 0757-0416 |  | RESISTOR 511 OHM 1\% 125 W F TUBULAR | 24546 | C4-1/8-T0-5118-F |
| Al0R9 | 0757-0442 |  | RESISTOR 10K 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-1 002-F |
| Al0R10 | 0757-0442 |  | RESISTOR 10K 18.125 W F TUBULAR | 24546 | C4-1/8-T0-1 002-F |
| A 10 Rl 11 | 0698-3450 | 4 | RESISTOR 42.2K 1\% . 125 W F TUBULAR | 16299 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-4222-F \\ & C 4-1 / 8-T 0-1622-F \end{aligned}\right.$ |
| A 10 R 12 A 10 R 13 | 0757-0447 |  | RESISTOR 16.2K 1\% .125W F TUBULAR RESISTOR 1.1K 1\% . 125W F TUBULAR | 24546 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-1622-F \\ & \mathrm{C} 4-1 / 8-T 0-1101-F \end{aligned}\right.$ |
| A 10R14 | 0757-0424 |  | RESISTOR 511 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-511R-E |
| A 10 R1 5 | 0757-0421 |  | RESISTOR 825 OHM 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-825Q-F |
| A 10 R 16 | 0757-0424 |  | RESISTOR 1.1 KK 18. 125 W F TUBULAR | 24546 03888 | $\begin{aligned} & \text { C4-1/B-TO-1101-F } \\ & \text { PMC55-1/8-T0-21R5-F } \end{aligned}$ |
| Al0R17 A 10 R 18 | 0698-3430 |  | RESISTOR 21.50 OHM 18.125 W F TUBULAR RESISTOR 422 OHM 18.125 W TUBULAR | (03888 | ( ${ }^{\text {PM }}$ (55-1/8-T0-21R5-F |
| AlOR19 | 0757-0279 |  | RESISTOR 3.16 K 18.125 W F TUBULAR | 24546 | C.4-1/8-T0-3161-F |
| A 10R20 | 0757-0421 |  | RESISTOR 825 OHM 1\%.125 F F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A 10 R 21 | 0757-0442 |  | RESISTOR $10 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| A 10 R 22 | 0757-0279 |  | RESISTOR 3.16 K 19.125 W F TUBULAR | 24546 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-3151-F \\ & C .4-1 / 8-T 0-3161-F \end{aligned}\right.$ |
| A 10 R23 | 0757-0279 |  | RESISTOR 3.16 K 1\% | 24546 16299 | $\begin{aligned} & C .4-1 / 8-T 0-3161-F \\ & C, 4-1 / 8-T 0-3831-F \end{aligned}$ |
| A 10R24 AlOR25 | -0698-3153 |  |  | 16299 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-3831-F \\ & C 4-1 / 8-T 0-51 R 1-F \end{aligned}\right.$ |
| A10R26 | 0757-0394 |  | RESISTOR 51.1 OHM 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-51R1-F |
| A10R27 | 0757-0416 |  | RESISTOR 511 DHM 18.125 W F TUBULAR | 24546 | $C 4-1 / 8-T 0-511 R=F$ |
| Al0R28 | 0757-0416 |  | RESISTOR 511 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-511R-F |
| A 10 R29 | 0757-0442 |  | RESISTOR 10K 18.125 W F TUBULAR | 24546 | C4-1/8-T0-1 002-F |
| A 10R30 | 0757-0200 |  | RESISTOR 5.62K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-5621-F |
| A 10R31 | 0757-0424 |  |  | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\{\begin{array}{l} r_{4}-1 / 8-T 0-11101-F \\ r 4-1 / 8-T 0-5111-F \end{array}\right.$ |
| A 10832 A $10 R 33$ | $\left\lvert\, \begin{aligned} & 0757-0438 \\ & 0757-0444 \end{aligned}\right.$ |  | RESISTOR 5.11K 1\% . 125W F TUBULAR RESISTOR 12.1K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-5111-F \\ & C 4-1 / B-T 0-1212-F \end{aligned}\right.$ |
| A $10 R 33$ A 10834 | 0757-0424 |  | RESISTOR 1.1K $1 \% .125 \mathrm{FF}$ TUBULAR | 24546 | C4-1/8-T0-1101-F |
| A 10 R 35 | 0757-0444 |  | RESISTOR 12.1K 1\% .125 F TUBULAR | 24546 | C4-1/8-T0-1212-F |
| Al0R36 | 0757-0280 |  | RESISTOR 1K 1\%. 125 W F TUBULAR | 24546 | C4-1/8-T0-1 001-F |
| A 10 TL | 08660-80001 | 3 | TRANSFORMER, SAMPLER | 28480 | 08660-80001 |
| A10U1 A10U2 | $1820-0451$ $1820-0451$ | 6 | IC DGTL MC 3062P FLIP-FLOP IC DGTL MC 3062P FLIP-FLO ${ }^{\circ}$ | $\begin{aligned} & 04713 \\ & 04713 \end{aligned}$ | $\begin{aligned} & \text { MC } 3062^{P} \\ & \text { MC } 3062 P \end{aligned}$ |
| A 1003 | 1820-0204 | 3 | IC DGTL MC 3006P GATE | 04713 | MC 3006P |
| A 1004 | 1820-0751 | 11 | IC DGTL SN74196N COUNTER | $01295$ | SN74196N |
| A10U5 | 1820-0751 |  | IC DGTL SN74196N COUNTER | $01295$ | SN74196N |
| A10U6 A10U7 | $\left\lvert\, \begin{aligned} & 1820-0751 \\ & 1820-0054 \end{aligned}\right.$ |  | IC DGTL SN74196N COUNTER IC DGTL SN74 00 N GATE | $\begin{aligned} & 01295 \\ & 01295 \end{aligned}$ | SN74196N <br> SN7400N |
| A11 | 08660-60019 | 1 | BOARD ASSY, SL2 OSCILLATOR (EXCEPT OPT 004) | 28480 | 08660-60019 |
| A 11 | 08660-20040 |  | BOARD ASSY, N2 LOOP-SLI LOOP COUPLER (OPT 004 ONLY) | 28480 | 03660-20040 |
| A11C1 <br> AllC2 <br> AllC3 <br> AllC4 <br> A11C5 | $\left\lvert\, \begin{array}{lll} 0 & 150-0121 \\ 0 & 180-0058 \\ 0 & 180-1704 \\ 0 & 180-2214 \\ 0 & 150-0121 \end{array}\right.$ |  | CAPACITOR-FXO . 1UF + 80-20\% 50WVOC CER CAPACITOR-FXD; 50UF+75-10\% 25VDC AL CAPACITOR-FXD: $47 \mathrm{UF}+-10 \%$ 6VDC TA-SOLID CAPACITOR-FXD; $90 U F+75-10 \%$ 16VDC AL CAPACITOR-FXD . 1 UF +80-20\% 50WVDC CER | $\begin{aligned} & 28480 \\ & 56289 \\ & 56289 \\ & 56289 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0150-0121 \\ & 3005065025 \mathrm{CC} 2 \\ & 1500476 \times 9006 \mathrm{B2} \\ & 300906 \mathrm{G} 016 \mathrm{CC} \\ & 0150-0121 \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A11C6 | 0160-0174 |  | CAPACITMR-FXD .47UF +80-208 25 WVDC. CSD | 28490 | 0160-017 |
| AllCt | 0180-0049 |  | CAPACITOR-FXD; 20UF+75-10\% $50 \mathrm{~V} D \mathrm{C}$ AL | 56289 | 300206;050cc2 |
| $\triangle 11 \mathrm{CB}$ | 0160-0174 |  | CAPACITCR-FXD -47UF +80-209 25 WVDC CER | 28480 | 0160-0174 |
| Al1co | 0180-0116 |  | CAPACITOR-FXD; $6.8 U F+-10 \%$ 35VDC TA | 56289 | $1500385 \times 9035 \mathrm{R} 2$ |
| Allcio | 0180-2210 | 2 | CAPACITIR-FXD; 2UF+50-10\% 150VDC AL | 56299 | $300205{ }^{\circ} 1508 \mathrm{B2}$ |
| A $11 \mathrm{Cl1}$ | 0150-0121 |  | CAPACITOR-FXD. .1UF + 80-20\% 50WVDC CER | 28480 | 0150-0121 |
| Allciz | 0180-0374 |  | CAPACITOR-FXD; 10UF+-10\% 20VDC TA-SOLID | 55289 | $1500106 \times 90208 ?$ |
| A11C13 | 0160-2055 |  | CAPACITOR-FXD . 01 UF +80-20\% 100 WVDC CER | 28490 | 0150-2055 |
| A11C14 | 0160-0386 |  | CAPACITOR-FXO 3.3PF +-.25PF 500WVDC CER | 28480 | 0160-0386 |
| AllCls | 0170-0082 |  | CAPACITOR-FXD . O1UF +-20\% 50WVDC POLYE | 84411 | S01PE1030R5 W1 |
| Al1C16 | 0170-0082 |  | CAPACITOR-FXD . O IUF +-20\% 5OWVDC POLYE | 84411 | 601 PE1030R5 Wi |
| AllC17 | 0121-0059 | 4 | CAPACITOR; VAR; TRMR; CER; 2/8PF | 73899 | DV11PR8A |
| A11C18 | 0160-2204 |  | CAPACI TOR-FXD 100PF +-5\% 300WVOC MICA | 29480 28480 | 0160-2204 |
| A11C19 A11 d | O160-0386 $0160-0386$ |  | CAPACITOR-FXO 3.3PF +-. 25 SF $500 W V D C$ CER CAPACITMR-FXD 3.3PF +-.25PF 500 VVOC CER | 28480 28480 | $0160-0386$ $0160-0385$ |
| AllC21 | 0160-2055 |  | CAPACITIR-FXD . DIUF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A11C22 | 0160-2055 |  | CAPACITOR-FXD . $014 \mathrm{~F}+80-20 \%$ 100WVOC CER | 28480 | 0160-2055 |
| A11C23 | 0160-2055 |  | CAPACITOR-FXD . O1UF +80-20\% 100WVOC CER | 28480 | 0160-2055 |
| A11C24 | 0160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A11C25 | 0180-0228 |  | CAPAC!TOR-FXO; 22UF+-10\% 15VDC TA-SOLID | 56289 | $1500226 \times 901592$ |
| A11C26 | 0180-2207 | 4 | CAPACITOR-FXD; 100UF+-10\% 10VDC TA | 56289 | $1509107 \times 901$ OR 2 |
| A11C27 | 0180-0116 |  | CAPACITOR-FXD: $6.8 \mathrm{BFF}+10 \%$ 35VDC TA | 55289 | $1500685 \times 9035 \mathrm{R} 2$ |
| A11C28 | 0160-2228 | 1 | CAPACITOR-FXD 2700PF +-5\% 300WVDC MICA | 28480 | 0160-22-29 |
| A11CR1 A11CR2 | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1001-0040 |
| AllCR2 $A 11 C R 3$ | 1901-0040 |  | DIDDE-SWITCHING 2NS 30V 50 MA | 28480 28480 | 1901-0040 |
| A11CR 3 All 11 | 1901-0040 |  | DIDDE-SWITCHING 2NS 30 V 50MA | 28480 28480 | $1901-0040$ $1901-0040$ |
| A11CR4 | 1901-0040 |  | DIDDE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| AllCr6 | 1901-0040 |  | DIDOE-SWITCHING 2NS 30V 50MA | 29480 | 1901-0040 |
| A11CR 7 | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| Al1CR 8 | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A11CR9 | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 50Ma | 28480 | 1901-0040 |
| A11CR10 | 1901-0040 |  | OIDOE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A11CR11 | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A11CR12 | 1901-0040 |  | DIODF-SHITCHING 2NS 30V 50MA | 28430 | $1901-0040$ |
| A11CR 13 Al1 Al 14 | 0122-0264 | 4 | DIO-VVC 1N5148A 47PF 5\% C4/C60 $=3200000$ | 04713 | $1 N 51484$ |
| A 11 CR 14 A11 CR 15 | $\left\lvert\, \begin{aligned} & 0122-0262 \\ & 1901-0040 \end{aligned}\right.$ | 4 | DIOLVVC IN5147A 39PF 5\% C4/C60=3200000 DIODE-SHITCHING 2NS 30V 5OMA | 04713 28480 | $\begin{aligned} & 1 N 51474 \\ & 1901-0040 \end{aligned}$ |
| A11CR 15 | $1901-0040$ |  | DIODE-SHITCHING 2NS 30V 5OMA | 28480 | 1901-0040 |
| A11CR 16 | 1901-0518 | 2 | didoe-schottik | 28480 | 1901-0518 |
| Alll | 9100-1629 |  | COIL ; FXD: MOLOED RF CHOKE: 47UH 5\% | 24226 | $15 / 472$ |
| A1112 | 9 140-0114 |  | COIL: FXD; MOLDED RF CHOKE; 10UH $10 \%$ | 24226 | $15 / 102$ |
| A1113 | 9100-1629 |  | COIL ; FXD; MOLDED RF CHOKE; 47UH 5\% | 24226 | $15 / 472$ |
| A1114 | 9100-1629 |  | COIL F EXD; MDLDED RF CHOKE; 47UH 5\% | 24226 | $15 / 472$ |
| A11L5 | 9140-0179 |  | COIL: FXD; MOLDED RF CHOKE: 22UH 10\% | 24226 | $15 / 222$ |
| A1116 | 9140-0170 |  | COIL: FXD: MOLDED RF CHOKE; 22 UH 10\% | 24226 | $15 / 222$ |
| A1117 | 9100-1629 |  | CTIL ; FXD; MOLDFO RF CHOKE; 47UH 5\% | 24226 | $15 / 472$ |
| A11L8 | 9 100-2815 |  | COIL: FXD; NON-MOLDED RF CHOKE; -7UH 5\% | 28480 | 9100-2915 |
| A111.9 Allio | $9140-0179$ $9140-0179$ |  | COIL: FXD: MOLDED RF CHOKE: 22UH $10 \%$ COIL: FXD: MOLDED RF CHOKE; 22UH $10 \%$ | 24226 24226 | $15 / 222$ $15 / 222$ |
| A11L10 |  |  | COIL: FXD; MOLDED RF CHOKE; 22UH 10\% | 24226 | $15 / 222$ |
| A11111 | $9140-0129$ $9100-0368$ |  | COIL: FXD: MOLDED RF CHOKE; 220UH 5\% COIL: FXD: MOLDED RF CHOKE: 33UH 10\% | 24226 24226 | $\begin{aligned} & 15 / 223 \\ & 10 / 330 \end{aligned}$ |
| A11L12 | 9100-0368 | 1 | COIL: FXD; MOLDED RF CHOKE; . 33 UH 10\% | 24226 | $\text { \| } 10 / 330$ |
| A 1101 | 1854-0092 |  | TRANSISTOR NPN SI PD=200MH FT $=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A1102 | 1855-0081 |  | TRANSISTMR: J-FET N-CHAN, D-MODE SI | 01295 | 2N5245 |
| A 1103 | 1854-0345 |  | TRANSISTOR NPN 2 N5 179 SI POL ${ }^{\text {P }}$ 200MW | 04713 | 2N5179 |
| A1104 | 1853-0050 |  | TRANSISTOR PNP SI CHIP TO-18 PD=360MH | 28430 | 1853-005] |
| A1105 | 1853-0050 |  | TRANSISTOR PNP SI CHIP TO-18 PD=360MW | 28480 | 1853-0050 |
| A 1106 | 1854-0087 |  | TRANSISTOR NPN SI PD=360MW FT $=75 \mathrm{MHZ}$ | 28480 | 1854-0087 |
| A1107 | 1853-0007 |  | TRANSISTOR PNP $2 N 3251$ SI CHIP | 04713 | 2N3251 |
| A1108 | 1853-0007 |  | TRANSISTOR PNP 2N3251 SI CHIP | 04713 | 2N3251 |
| A 11109 A 11010 | 1853-0007 |  | TRANSISTOR PNP $2 N 3251$ SI CHIP TRANSISTIR PNP $2 N 3251$ SI CHIP | 04713 04713 | 2N3251 2N3251 |
| A11010 | 1853-0007 |  | TRANSISTIR PNP $2 N 3251$ SI CHIP | 04713 | 2N3251 |
| A 11011 | 1853-0007 |  | TRANSISTOR PNP $2 N 3251$ SI CHIP | 04713 | 2N3251 |
| A11012 | 1853-0007 |  | TRANSISTOR PNP 2 N3251 SI CHIP | 04713 | 2N3251 |
| A 11013 | 1853-0007 |  | TRANSISTOR PNP 2N3251 ST CHIP | 04713 | 2N3251 |
| A 11014 | 1853-0007 |  | TPANSISTOR PNP 2N3251 SI CHIP | 04713 | 2N3251 |
| A11015 | 1853-0050 |  | TRANSISTOR PNP SI CHIP TO-18 PD=360MW | 28480 | 1853-0059 |
| A11016 | 1853-0007 |  | TRAVSISTOO PNP $2 N 3251$ SI CHIP | 04713 | 2N3251 |
| A 11017 | 1853-0007 |  | TRANSISTRR PNP 2N3251 SI CHIP | 04713 | 2N3251 |
| A11018 | 1853-0007 |  | TRANSISTOR PNP 2N3251 SI CHIP | 04713 | 2N3251 |
| A11019 | 1853-0007 |  | TRANSISTOR PNP 2 N3 251 SI CHIP | 04713 | 2N3251 |
| A11020 | 1853-0007 |  | TRANSISTOR PNP 2N3251 SI CHIP | 04713 | 2N3251 |
| Al1R1 | 0698-0093 |  | RESISTOR 1.96K 1\% .125W F TUBULAR | 16299 | C4-1/8-T0-1 961-F |
| Al1R2 | 0698-0083 |  | RESISTOR 1.96K 1\% .125W F TUBULAR | 16299 | C4-1/8-Tก-1961-F |
| A11R3 | 0698-0083 |  | RESISTOR 1.96K 1\% .125 F F TUSULAR | 16299 | C4-1/8-T3-1961-F |
| Al1R4 | 0698-0083 |  | RESISTOR $1.96 \mathrm{~K} 1 \%$-125 F F TUBULAR | 16299 | C4-1/8-77-1961-F |
| AllR5 | 0757-0442 |  | RESISTOP 10K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-1002-F |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AllR6 A11R7 Al1R8 A11R9 $A 11 R 10$ | $\begin{aligned} & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \\ & 0757-0479 \\ & 0757-0472 \end{aligned}$ |  | PESISTOR $10 K$ $1 \%$ $.125 W$ $F$ TUBULAR <br> RFSISTGR $10 K$ 12 $.125 W$ $F$ TUBULAR <br> RESISTOR $10 K$ $1 \%$ $.125 W$ $F$ TUBULAR <br> RESISTOR $392 K$ 18 $.125 W$ $F$ TUBUI. AR <br> RESISTOR $200 K$ 18 $.125 W$ $F$ TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 19771 \\ & 24545 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \\ & M F 4 C 1 / 8-T 0-3923-F \\ & C 4-1 / 8-T 0-2003-F \end{aligned}$ |
| $\begin{aligned} & \text { AllR11 } \\ & \text { A11R12 } \\ & \text { A11R13 } \\ & \text { A11R14 } \\ & \text { A11R15 } \end{aligned}$ | $\begin{aligned} & 0757-0465 \\ & 0698-3228 \\ & 0757-0274 \\ & 0757-0460 \\ & 2100-1760 \end{aligned}$ | 2 | RESISTOR 100K 1\% . 125W F TUBULAR RESISTOR 49.9K 1\% . 125 H F TUBULAR RESISTOR 1.21K 1\% . 125W F TUBULAR RESISTOR 61.9K 1\% . 125W F TUBULAR RESISTOR: VAR: TRMR; 5KOHM 5\% WH | $\begin{aligned} & 24546 \\ & 07716 \\ & 24546 \\ & 24546 \\ & G 8027 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1003-F \\ & C E A 1 / 8-T O-4991-F \\ & C 4-1 / 8-T 0-1213-F \\ & C 4-1 / 8-T 0-6192-F \\ & C T-106-4 \end{aligned}$ |
| A11R16 <br> AllR17 <br> Al1R18 <br> Al1R19 <br> A11R20 | $\begin{aligned} & 0698-3156 \\ & 0698-0083 \\ & 0757-0442 \\ & 2100-1759 \\ & 0757-0439 \end{aligned}$ |  | RESISTOR 14.7K 1\% .125W F TUBULAR RESISTOR 1.96K $1 \%$.125W F TUBULAR RESISTOR 10K 1\% . 125 W F TUBULAR RESISTOR: VAR; TRMR; 2KOHM 5\% WW RESISTOR 6.81K 1\% . 125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 24546 \\ & \text { G8 } 027 \\ & 24546 \end{aligned}$ | $\left(\begin{array}{l} C 4-1 / 8-T 0-1472-F \\ C 4-1 / 8-T V-1061-F \\ C .4-1 / 8-T 0-1002-F \\ C T-106-4 \\ C 4-1 / 8-T 0-6811-F \end{array}\right.$ |
| $\begin{aligned} & A 11 R 21 \\ & A 11 R 22 \\ & A 11 R 23 \\ & A 11 R 24 \\ & A 11 R 25 \end{aligned}$ | $\begin{array}{\|} 0757-0200 \\ 0757-0442 \\ 0698-3440 \\ 0698-3154 \\ 0698-0083 \end{array}$ |  | RESTSTER 5.62K $1 \% .125 W$ F TIJBULAR RESISTOR 10K 18.125 W F TUBULAR RESISTOR 196 OHM 1\%.125W F TUBULAR RESISTOR 4.22K 1\% . 125W F TUBIJLAR RESISTOR 1.96K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16209 \\ & 16209 \\ & 15299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-196 R-F \\ & C 4-1 / 9-T 0-4221-F \\ & C .4-1 / B-T 7-1951-F \end{aligned}$ |
| A11R26 <br> A11R27 <br> A11228 <br> A11R29 <br> Al1R30 | $\begin{aligned} & 0757-0442 \\ & 0757-0453 \\ & 0757-0461 \\ & 0757-0464 \\ & 0757-0467 \end{aligned}$ | 4 4 4 4 | RESISTOR 10K 1\% . 125W F TUBULAR RESISTOR 51.1K 1\% .125W F TUSULAR RESISTDR 68.1K 1\% . 125W F TUBULAR RESISTOR 90.9K 1\% .125W F TUBULAR RESISTDR 121K 1\% . 125W F TUBULAP | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C .4-1 / R-T 0-1002-F \\ & C .4-1 / B-T 0-5112-F \\ & C 4-1 / 8-T O-6812-F \\ & C 4-1 / 8-T 0-9092-F \\ & C 4-1 / 8-T 0-1213-F \end{aligned}$ |
| A11R31 <br> A11R32 <br> A11R33 <br> A11R34 <br> A11R35 | $\begin{aligned} & 0757-0466 \\ & 0698-3243 \\ & 0698-3243 \\ & 0698-3266 \\ & 0698-3266 \end{aligned}$ | 4 8 | RESISTOR 110K 1\% . 125H F TUBULAR <br> RFSISTOR 178K 1\% . 125W F TUBULAR <br> RESISTOR 178K 1\% . 125W F TUBULAR <br> RESISTOR 237K 1\% . 125W F TUBULAR <br> RESISTOR 237K 18 • 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-1103-F \\ & C 4-1 / 8-T 0-1783-F \\ & C 4-1 / 8-T 0-1783-F \\ & C 4-1 / 8-T 0-2373-F \\ & C 4-1 / 8-T 0-2373-F \end{aligned}\right.$ |
| A11R36 <br> A11R37 <br> A11R38 <br> A11R39 <br> A11R40 | $\left\lvert\, \begin{aligned} & 0698-3459 \\ & 0698-3162 \\ & 0698-3155 \\ & 2100-2574 \\ & 0698-3155 \end{aligned}\right.$ | 4 5 4 | RESISTOR 383K 1\% . 125W F TUBULAR RESISTOR 46.4K 1\% .125W F TUBULAR RESISTOR 4.64K 1\% .125W F TUBULAR RESISTDR: VAR; TRMR: 500 OHM 10\% C RESISTOR 4.64K 1\% . 125W F TUBULAR | $\begin{aligned} & 19701 \\ & 16299 \\ & 16299 \\ & 19701 \\ & 16279 \end{aligned}$ | $\begin{aligned} & \text { MF4C1/B-T0-3833-F } \\ & \text { C } 4-1 / 8-T 0-4642-F \\ & \text { C4-1/R-TO-4641-F } \\ & \text { ET50 } \\ & \text { C } 4-1 / 801 \\ & \hline \end{aligned}$ |
| $\begin{array}{\|l\|l} \text { A } 11 \text { R41 } \\ \text { All R42 } \\ \text { All R43 } \\ \text { All R44 } \\ \text { A11R45 } \end{array}$ | $\begin{aligned} & 0698-0083 \\ & 0757-0442 \\ & 0698-3442 \\ & 0698-3437 \\ & 0757-0405 \end{aligned}$ |  | RESISTOR 1.96K 1\%.125W F TUBULAR RESISTOR 10K 1\% . 125 W F TUBULAR RESISTOR 237 DHM 17.125 W F TUBULAR RESISTOR 133 OHM 1\% . 125W F TUBULAR RESISTOR 162 OHM 1\%. 125 W F TUBULAR | $\begin{aligned} & 16209 \\ & 24546 \\ & 15279 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T O-1961-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T O-237 R-F \\ & C 4-1 / 8-T 0-133 R-F \\ & C 4-1 / 8-T 0-162 R-F \end{aligned}$ |
| A11R46 <br> A11R47 <br> A11R48 <br> A11R49 <br> AllR50 | $\left\lvert\, \begin{aligned} & 0698-3439 \\ & 0698-3440 \\ & 0698-3132 \\ & 0698-3443 \\ & 0698-3445 \end{aligned}\right.$ |  | RESISTOR 178 OHM 1\% . 125 W F TUBULAR RESISTOR 196 JHM $1 \% .125$ W F TUBULAR RESISTOR 261 DHM 1\% .125N F TUBULAR RESISTOR 287 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 348 DHM 1\%.125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-178 R-F \\ & C 4-1 / 8-T 0-1 O 6 R-F \\ & C 4-1 / 8-T 0-2610-F \\ & C 4-1 / 8-T 0-287 R-F \\ & C 4-1 / 8-T 0-348 P-F \end{aligned}$ |
| A11R51 <br> A11R52 <br> Al1R53 <br> A11R54 <br> Al1R55 | $\begin{array}{r} 0698-3447 \\ 0698-0082 \\ 0757-0317 \\ 2100-2574 \\ 0698-3258 \end{array}$ | 4 2 | RESI STOR 422 OHM 17 . 125W F TUBULAR RESISTOR 464 OHM 1 . .125W F TUBILLAR RESISTOR 1.33K 1\% .125W F TUBULAR RESISTOR: VAR; TRMR; 500 OHM 10\% C RESISTOR 5.36K 1\%.125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 24546 \\ & 19791 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-422 R-F \\ & C 4-1 / 8-T 0-4640-F \\ & C 4-1 / 8-T 0-1331-F \\ & E T 50 \times 501 \\ & C 4-1 / 8-T 0-5361-F \end{aligned}$ |
| $\begin{aligned} & A 11 R 56 \\ & A \\ & A \\ & A \end{aligned} 11 R 578$ | $\begin{aligned} & 0698-3132 \\ & 0757-0834 \\ & 0698-0083 \\ & 0757-0442 \\ & 2100-2633 \end{aligned}$ | 4 6 | RESISTOR 261 OHM 1\% . 125 W F TUBULAR RESISTOR 5.62K 1\% .5W F TUBULAR RESISTOR 1.96K $1 \%$. 125 W F TUBULAR RESISTOR 1OK 18.125 W F TUBULAR RESISTOR: VAR; TRMR; 1KOHM 10\% C | $\begin{aligned} & 15290 \\ & 19701 \\ & 16299 \\ & 24546 \\ & 19701 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-2610-F \\ & \text { MF7C1/2-TO-5621-F } \\ & C 4-1 / 8-T J-1961-F \\ & C 4-1 / 8-T 0-1002-F \\ & \text { ET50×102 } \end{aligned}$ |
| AllR61 <br> A11R62 <br> Al1R63 <br> Al1R64 <br> A11R65 | $\begin{aligned} & 0757-0290 \\ & 0757-0441 \\ & 0698-0083 \\ & 0757-0442 \\ & 0757-0279 \end{aligned}$ |  | RESISTOR 6.19K 1\% . 125 W F TUBULAR RESISTOR 8.25K 1\% . 125 W F TUBULAR RESISTOR 1.96 K 1\% . 125 W F TUBULAR RESISTOR 10K 1\% •125W F TUBULAR RESISTOR $3.16 \mathrm{~K} \quad 18.125 \mathrm{~W}$ F TUBULAR | $\begin{aligned} & 19701 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \text { MF4C1/8-TO-6191-F } \\ & \text { C4-1/8-TO-8251-F } \\ & \text { C4-1/8-TO-1 961-F } \\ & \text { C4-1/8-TO-1002-F } \\ & \text { C4-1/8-T0-3161-F } \end{aligned}$ |
| A11R66 <br> AllR67 <br> AllR68 <br> A11R69 <br> AllR70 | $\begin{aligned} & 0757-0442 \\ & 2100-2633 \\ & 0757-0440 \\ & 0757-0444 \\ & 0698-0083 \end{aligned}$ |  | RESISTOR IOK 1\% . 125 W F TUBULAR RESISTOR; VAR; TRMR; IKOHM 10\% C RESISTOR 7.5K 1\% - 125W F TUBULAR RESISTOR 12.1K 18 . 125W F TUBULAR RESISTOR 1.96K 18.125 K F TUBULAR | $\begin{aligned} & 24546 \\ & 19701 \\ & 24546 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-T0-1 002-F } \\ & \text { ET50×102 } \\ & \text { C4-1/8-T0-7501-F } \\ & \text { C4-1/8-T0-1 } 212-F \\ & \text { C4-1/8-TJ-1 } 961-F \end{aligned}$ |
| $\begin{array}{\|l\|l} A 11 R 71 \\ A 11 R 72 \\ A 11 R 73 \\ A & 11 R 74 \\ A 11 R 75 \end{array}$ | $\begin{aligned} & 0757-0442 \\ & 0698-3157 \\ & 2100-2521 \\ & 0757-0288 \\ & 0698-0083 \end{aligned}$ | 4 | RESISTOR 10K 1\% . 125 W F TUBULAR RESISTOR 19.6K 1* . 125 W F TUBULAR RESISTOR; VAR; TRMR; 2KOHM 10\% C RESISTOR 9.09K $1 \%$. 125 W F TUBULAR RESISTOR 1.96K 18 .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 19701 \\ & 19701 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \text { C 4-1/8-T0-1 002-F } \\ & \text { C4-1/8-T0-1 962-F } \\ & \text { ET50X202 } \\ & \text { MF4C1/8-T 0-9091-F } \\ & \text { C4-1/8-TR-1961-F } \end{aligned}$ |
| AllR76 A11R77 A11R78 A11R79 A11R80 | $\begin{aligned} & 0757-0442 \\ & 2100-2521 \\ & 0757-0444 \\ & 0698-0083 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 1OK 1\% . 125 W F TUBULAR RESISTOR: VAR; TRMR; 2KIHM 10\% © RESISTOR 12.1K 18 . 125 W F TUBULAR RESISTOR 1.96K $1 \%$.125W F TUBULAR RESISTOR 10K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 10701 \\ & 24546 \\ & 18299 \\ & 24546 \end{aligned}$ |  |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A11R81 | 0683-8245 |  | RESISTOR 320K 5\% . 25N CC TIJRJLAP | 01121 | CB8245 |
| AllRs2 | 0698-3243 |  | RESISTOR 178K 1\% . 125 H F TUBULAR | 16299 | C4-1/8-T0-1783-F |
| -11893 | 2100-2439 | 2 | RESISTOR: VAR; TRMP; 5KOHM 10\% C | 19701 | FT50×502 |
| A11084 | 0698-3136 |  | RFSISTTOR 17.8K 19, 125 W F TUBULAR | 18299 | C4-1/8-T0-1782-F |
| C11 RR5 | 0698-3440 |  | RESISTOR 196 OHM $1 \%$.125W F TUBULAR | 16299 | C4-1/8-T0-196R-F |
| Al1R86 | 0698-0092 |  | RESISTOR 464 万HM 1\% .125W F TUBULAR | 16299 | 「4-1/8-T0-4640-F |
| Al1R97 | 0698-0083 |  | RESISTOR $1.96 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 16200 | C4-1/8-T0-1961-F |
| Al1R98 | 0757-0442 |  | RESISTOR 10K 1\% 12 I25 F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| $\triangle 11$ RS9 | 0757-0200 |  | RESISTOR 5.62 K 19.125 W F TUBULAR | 24546 | C4-1/8-T0-5621-F |
| A 11 Roo | 2100-2522 | 2 | RESISTOR: VAR; TRMR; 10 KOHM 10\% C | 19701 | ET50x103 |
| A1189 1 | 0757-0123 | 2 | RESISTOP 34.8K 1\% .125W F TUBULAR | 24546 | C5-1/4-T0-3482-F |
| AllR92 | 0757-0403 |  | RESISTOR 121 OHM 1\%.125W F TUBULAR | 24546 | C $4-1 / 8-\mathrm{TO}$-121R-F |
| A11R93 | 0698-3154 |  | RESISTOR $4.22 \mathrm{~K} 1 \mathrm{1} \mathrm{\%} .125 \mathrm{~W}$ F TUBULAR | 16299 | C4-1/8-T0-4221-F |
| A11R94 | 0698-3444 |  | RESISTOR 316 OHM 17.125 H F TUBULAR | 16299 | C4-1/8-T0-3168-F |
| A11R95 | 0698-0085 |  | RESISTOR $2.61 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 16299 | C4-1/8-T0-2611-F |
| A 11 RO6 | 0757-0402 | 1 | RESISTOR 110 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-111-F |
| Al1r97 | 0757-0288 |  | RESISTOR 0.09 K 19.125 W F TUBULAR | 10701 | MF4C1/8-T0-9091-F |
| Al1R98 | 0698-0085 |  | RESISTOR $2.61 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 16299 | $C 4-1 / 8-70-2511-F$ |
| $\begin{aligned} & A 11 R 99 \\ & A 11 R 100 \end{aligned}$ | $\begin{aligned} & 0757-0421 \\ & 0757-0395 \end{aligned}$ |  | RESISTOR 825 OHM $1 \%$. 125 W F TUBULAR RFSISTOR 56.2 OHM 18 . 125W F TUBULAR | 24546 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-825 R-F \\ & C 4-1 / 8-T 0-56 R 2-F \end{aligned}\right.$ |
|  |  |  |  |  |  |
| A11R101 | 0698-3439 |  | RESISTSR 178 OHM 18.125W F TUBIJLAR | 16299 |  |
| A11P102 | 0698-3444 |  | RESISTOR 316 OHM 1 \% 125 W F TUBULAR | 16299 | $\left\{\begin{array}{l} C 4-1 / 8-T 0-316 R-F \\ C 4-1 / 8-T 0-147 R-F \end{array}\right.$ |
| Al1R103 Al1R104 | 0698-3438 |  |  | 16209 16299 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-147 R-F \\ & C 4-1 / 8-T 0-4640-F \end{aligned}\right.$ |
| AllR105 | 0757-0442 |  | RESISTOR 10K 1\% .125\% F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| A11R106 A11R107 | \|0698-3441 |  | RESISTOR 215 OHM 1\% . 125 W F TUBULAR RESISTOR 1K 19. .125 F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T O-215 R-F \\ & C 4-1 / 8-T O-1001-F \end{aligned}$ |
| Allul | 1820-0054 |  | IC DGTL SN74 00 NGATE | 01295 | SN7400V |
| Allue | 1820-0214 |  | IC DGTL SN74 42 N DECDOER | 01295 | SN7442N |
| A1113 | 1820-0054 |  | IC DGTL SN74 00 NGATE | 01295 | SN7400V |
| A 12 | 08660-60018 | 1 | BOARD ASSY, SL2 DETECTOR (EXCEPT OPT 004) | 28480 | 08660-60018 |
| A 12 | 08650-20040 |  | BOARD ASSY, N2 LOOP-SLI LOOP COUPLER (DPT 004 ONLY) | 28480 | 08660-20040 |
| ${ }^{\text {A } 12 C 1}$ | 0160-0174 |  | CAPACITOR-FXD .47UF +80-202 25WVOC CER | 28480 | 0150-0174 |
| A12C. | 0190-2207 |  | CAPACITOR-FXD: $100 \mathrm{UF}+-102$ 10VDC TA | 56289 28480 | $1509107 \times 901022$ |
| A12C3 A12C4 | - $160-0174$ |  |  | 28480 29480 | $\left\lvert\, \begin{aligned} & 0160-0174 \\ & 0160-0174 \end{aligned}\right.$ |
| A12C4 A 12 C 5 | O160-0174 |  | CAPACITMR-FXO CAPACITOR-FXD .47UF +80-20\% 25WVDC +80-20\% 25WVOC CER | 28480 28490 | $\begin{aligned} & 0160-0174 \\ & 0150-0174 \end{aligned}$ |
|  | 0180-0058 |  | CAPACITOR-FXD; 50UF+75-108 25VOC AL | 56239 | $30 \cap 5066025 \mathrm{CC} 2$ |
| A12C, 7 | 0160-2055 |  | CAPACITOR-FXD . $01 U \mathrm{~F}+80-20 \%$ 10OHVOC CER | 28480 | \|0160-2055 |
| A12C8 | 0150-0121 |  | CAPACITOR-FXD . $1 \mathrm{UF}+80-20 \mathrm{~S} 50 \mathrm{WVOC}$ CER | 28480 | 0150-0121 |
| A12C9 | - 160-0301 | 5 | CAPACITOR-FXD .0 12UF +-10 E 200WVDC POLYE | 56289 | 292012392 |
| A12C10 | 0180-2055 |  | CAPACITOR-FXD .OIUF +80-208 100WVOC CER | 28480 | 0160-2055 |
| A 12C11 | 0160-0301 |  | CAPACITOR-FXD .012UF +-10\% 200WVDC POLYE | 56289 | 292P12392 |
| A 12 Cl 12 | 0160-2261 | 4 | CAPACITIR-FXD 15PF +-5\% 500HVDC CER O+ | 23480 | 0160-2261 |
| A12C13 | 0160-2261 |  | CAPAC.ITOR-FXD 15PF +-5\% 500HVDC CER O+ | 23480 | 0160-2261 |
| ${ }^{\text {A } 12 C 14}$ | 0160-0174 |  | CAPACITOR-FXD - 47UF +80-209 25WVIC CER | 28480 | Q160-0174 |
| A12C15 | 0180-2141 | 1 | CAPACITOR-FXD: 3.3UF+-10\% 50VDC TA | 55289 | $1505335 \times 905082$ |
| A 12 Cl 6 | 0160-2055 |  | CAPAEITOR-FXD .O1UF +80-20\% 100WVDC CER | 23480 |  |
| A $12 \mathrm{Cl17}$ | 0 180-0058 |  | CAPACITOR-FXD: 50UF+75-10\% 25VDC AL | 56289 | $300506 G 025 C C 2$ |
| A12C18 | 0160-0299 | $2$ | CAPACITOR-FXD 1800PF +-10\% 200WVDC POLYE | 58289 | $292 \text { P1 } 8292$ |
| A12C19 A 12 C 20 | 0160-0939 | $1$ | CAPACITOR-FXD 430PF +-5\% 300WVOC MICA | 28480 28480 | $\left\lvert\, \begin{aligned} & 0160-0939 \\ & 0160-0174 \end{aligned}\right.$ |
|  |  |  | CAPACITDR-FXD 1800PF +-10\% 200WVDC POLYE | 56289 |  |
| A 12 C 22 | $0180-0291$ |  | CAPACITDR-EXD; 1UF+-10\% 35VDC TA-SOLID | 56299 | $1500105 \times 903542$ |
| A12C23 | 0160-2055 |  | CAPAC ITOR-FXD . $01 \mathrm{IUF}+80-208100 \mathrm{HVDC}$ CER | 28480 | 0160-2055 |
| A 12 C 24 | 0 160-3534 |  | CAPACITOR-FXD 510PF +-5\% 100WVDC MICA | 28490 | 10160-3534 |
| A12C25 | 0180-0291 |  | CAPACITOR-FXD; 1UF +-10\% 35VDC TA-SOLID | 55289 | $1507105 \times 903542$ |
| A 12 Fl | 10534 C | 2 | MIXER: 200 MHz | 28480 | 10534 C |
| A12L1 | 9140-0179 |  | COIL: FXD; MOLDED RF CHOKE; 22UH 10\% | 24276 | $15 / 222$ |
| A12L2 | 9140-0114 |  | COIL: FXD; MOLDED RF CHOKE: 10UH 10\% | 24226 | $15 / 102$ |
| A12L3 | 9140-0179 |  | COIL: FXO; MOLDED RF CHOKE: 22UH 10\% | 24228 | $15 / 222$ |
| A12L4 | 9100-1621 | 2 | CDIL : FXD; MOLDED RF CHOKE; 18UH $10 \%$ | 24226 | $15 / 182$ |
| A12L5 | 9140-0179 |  | COIL : FXD: MOLDED RF CHOKE; 22UH 108 | 24226 | 15/222 |
| A 1226 | 9140-0179 |  | COIL: FXD; MOLDED RF CHOKE; 22UH 10\% | 24226 | $15 / 222$ |
| A12L7 | 9100-1658 | 1 | COIL: FXD; MOLOFD RF CHOKE; 1.6MH 5\% | 24226 | $22 / 164$ |
| A 1201 | 1853-0015 |  | TRANSISTOR PNP SI CHIP PD=200MW | 28480 | 1853-0015 |
| A 1202 | 1854-0092 |  | TRANSISTIR NPN SI PD=200M FT $=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A 1203 | 1854-0092 |  | TRANSISTOR NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A1204 | 1854-0092 |  | TRANSISTO ${ }^{\circ}$ NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A 1205 | 1854-0092 |  | TPANSISTOR NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Nun:ber |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 41206 | 1854-0092 |  | TRANS!STIP NPN SI P $=200 \mathrm{MW}$ FT $=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A 1207 | 1854-0092 |  | TPANSISTIR NPN SI PD $=200 \mathrm{MW} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | 28480 | 1854-0292 |
| A 1208 | 1853-0007 |  | TRANSISTOP PNP 2 N3251 SI CHID | 04713 | 2N3251 |
| A 1209 | 1853-0007 |  | TRANSISTOR PNP 2 N3251 SI CHIP | Cヶ713 | 2N3251 |
| A 12010 | 1853-0007 |  | TRANSISTIJR PNP 2 N3251 SI CHIP | 04713 | 2N3251 |
| A 12011 | 1853-0007 |  | TRANSISTOR PNP 2 N3 251 SI CHIP | 04713 | 1325] |
| A 12012 | 1854-0092 |  | TRANSISTOR NON SI PD= $200 \mathrm{MW} \quad \mathrm{FT}^{\text {¢ }}=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| ${ }^{\text {A }} 1281$ | 0757-0399 |  | RESI STOR 82.5 OHM 19.125 W F TUBULAP | 24546 | $C 4-1 / 8-70-82 P 5-E$ |
| A12R2 A12R3 | $0757-0400$ $0757-0399$ | 3 | RESISTOR 90.9 OHM 18.125 W F TUBULAR | 24546 24546 | $\left\lvert\, \begin{gathered} C 4-1 / 8-T 0-9020-F \\ C 4-1 / 8-T 0-8225-F \end{gathered}\right.$ |
| A12R4 | 0698-3151 |  | RESISTOR 2.87K 1\% .125W F TUBIULAR | 16299 | C4-1/8-T0-2871-F |
| A 12R5 | 0698-3151 |  | RESISTOP 2.87K 1\% .125H F TUBULAR | 16209 | C4-1/8-T0-2971-F |
| A $12 R 6$ A12R7 | 0698-3445 |  |  | 16299 24546 | C4-1/9-T0-34RR-F |
| Al2R7 A12R8 | 0757-0416 |  | RESISTOR 511 OHM 18.125 W F TUBULAR RESISTOR 8.25 K 18.125 W R | 24548 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-511 R-F \\ & C 4-1 / 8-T O-8251-F \end{aligned}\right.$ |
| A12R9 | 0757-0279 |  | RESISTOR 3.16 K 18.125 W F TUBULAR | 24546 | C4-1/8-T0-3161-F |
| A12910 | 0757-0420 |  | RESISTOP 750 OHM 12.125 W F TUBULAR | ? 2546 | C4-1/8-T0-751-F |
| A 12R11 | 0698-3442 |  | RESISTOR 237 OHM $1 \%-125 \mathrm{~W}$ F TUBULAR | 16299 | C4-1/8-T0-237R-F |
| A $12 \mathrm{R12}$ | 0757-0440 |  | RESISTOR 7.5 K 18, 125 H F TUBULAR | 24546 | C4-1/8-T0-7501-F |
| A $12 R 13$ A12R14 | 0757-0394 |  | RESISTOR 51.1 OHM 1\% . 125W F TUBULAR NOT ASSIGNED | 24546 | C4-1/8-T0-51R1-F |
| A12R15 | 0757-0294 | 2 | RESISTOR 17.8 OHM 15.125 F FUBULAR | 19701 | MF4C1/8-T0-17R8-F |
| A12R16 | 0757-0280 |  | RESISTOR 1 K 1\% 125 W F TUBULAR | 24546 | C.4-1/8-T0-1001-F |
| A12R17 | 0757-0230 |  | RESISTIR 1 K 12. 125 W F TUAULAR | 24546 | C4-1/8-T0-1001-F |
| A12R18 | 0757-0421 $0757-0280$ |  | RESI STOR 825 OHM 18.125 W F TUBULAR | 24546 24548 | C4-1/8-T0-825R-F |
| A12R20 | 0757-0421 |  | RESI STOR 825 OHM 18.125W F TUBULAR | 24546 | C4-1/8-T0-825P-F |
| A 12R21 | 0698-0082 |  | RESISTOR 464 OHM 1\% . 125 W F TUBULAR | 16299 | C4-1/8-T0-4540-F |
| A $12 \mathrm{R22}$ | 069 8-0083 |  | RESISTOR 1.96 K 1\% 18.125 W F TUBULAR | 16299 | C4-1/8-T7-1961-F |
| A12R23 | $0698-0083$ |  | RESISTOR 1.96 K 1\% 18.125 H F TUBULAR | 15299 | C4-1/8-70-1961-F |
| $\begin{aligned} & \text { A12R24 } \\ & \text { A12R25 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-0083 \\ & 0698-0083 \end{aligned}\right.$ |  | $\begin{array}{lllll}\text { RESI STOR } & 1.96 \mathrm{~K} & 18 & .125 \mathrm{~K} & \text { F TUBULAR } \\ \text { RESISTOR } & 1.98 \mathrm{~K} & 18 & .125 \mathrm{~W} & \text { F TUBULAR }\end{array}$ | 16299 16299 | $\left\{\begin{array}{l} \mathrm{C} 4-1 / 8-\mathrm{T}]-1961-F \\ \mathrm{C} 4-1 / 8-\mathrm{T}]-1961-F \end{array}\right.$ |
| A12R26 | 0698-0082 |  | RESISTOR 464 OHM 18.125H F TUBULAR | 16299 | C4-1/8-T0-4640-F |
| A12R27 | 0757-0442 |  | RESISTOR 10K 18.125w F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| A12R28 | 0757-0442 |  | RESISTOR 10K 18.125 W F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| A12R29 | 0757-0442 |  | RESISTOR 10K 1\% .125w F TUBULAR | 24546 | C4-1/8-T0-1 002-F |
| A12R30 | 0757-0442 |  | RESISTOR 10K 1\% -125H F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| A12R31 <br> A12R32 | $\begin{aligned} & 0683-3955 \\ & 0683-2055 \\ & 068 \end{aligned}$ | 2 | RESISTOR $3.9 \mathrm{M} 5 \%$. 25 W CC TUBULAR RESISTOR $2 M 5 \% .25 \mathrm{H}$ CC TUBULAR | $\left\lvert\, \begin{array}{lll} 01 & 121 \\ 0 & 1 & 12 \end{array}\right.$ | $\begin{aligned} & C B 3955 \\ & C B 2055 \end{aligned}$ |
| A12R33 | 0683-1055 | 2 | RESISTOP 1M 5\%.25 CC TUBULAR | 01121 | CB1055 |
| A 12 R 34 | 0698-3263 | 2 | RESISTOR 500K 1\% . 125 W F TUBULAR | 19701 | MF5.1/8-T0-5003-F |
| A12R35 | 0757-0200 |  | RESISTOR 5.62 K 18.125 W F TUBULAR | 24546 | C4-1/8-70-5621-F |
| $\begin{aligned} & \text { A12R36 } \\ & \text { A12R37 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3441 \\ & 2100-2633 \end{aligned}\right.$ |  | RESISTOR 215 OHM 18 . 125 W F TUBIJLAR RESISTOR; VAR; TRMR; 1 KOHM 10\% C | $\begin{aligned} & 15299 \\ & 19701 \end{aligned}$ | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / 8-T 0-2152-F \\ & \mathrm{ET} 50 \times 102 \end{aligned}\right.$ |
| A12R38 | O757-0200 |  | RESISTOR 5.62 K 18 .125W F TUBULAR | 24546 | C4-1/8-T0-5621-F |
| A12R39 | 0699-3150 |  | RESISTITR 2.37 K 18.125 W F TUBULAR | 15299 | C4-1/8-T0-2371-F |
| A12R40 | 0757-0418 |  | RESI STOR 619 DHM 1\%.125W F TUBULAR | 24546 | C4-1/8-70-6192-F |
| $\begin{aligned} & A 12 R 41 \\ & A 12 R 42 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0893-3155 \\ & 0757-0280 \end{aligned}\right.$ |  | RESISTOR 4.64K 1\% . 125W F TUBULAR RESISTOR 1K 18 . 125 F F TUBULAR | $\begin{aligned} & 15299 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / 8-T 0-4841-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO-1001-F} \end{aligned}\right.$ |
| A12R43 | 0757-0421 |  | RESISTIR 825 OHM 18 .125W F TUBULAR | 24546 | C $4-1 / 8-\mathrm{TO}-825 \mathrm{R}$ - |
| A12R44 | 0698-3443 |  | RESISTOR 287 OHM 1\% -125W F TUBILAR | 15299 | C4-1/8-T0-287R-F |
| A12R45 | 0698-3151 |  | RESISTIR 2.87K 1\% .125W F TUBULAR | 16299 | C4-1/8-70-2871-F |
| A12R46 A12R47 | $\begin{aligned} & 0698-0084 \\ & 0757-0280 \\ & 075 \end{aligned}$ |  | RESISTOR 2.15K 1\% . 125 H F TUBULAR RESISTOR 1K 1\%.125W F TUBULAR | $\begin{aligned} & 15299 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-2151-F \\ & C 4-1 / 8-T 0-1001-E \end{aligned}\right.$ |
| A12R48 | 0757-0280 |  | RESISTOR $1 \mathrm{LK} 1 \% .125 \mathrm{~F}$ F TUBULAR | 24546 | C4-1/8-T0-1001-F |
| A12R49 | 0698-0082 |  | RESISTOR 464 OHM 1\%.125W F TUBULAR | 15290 | C4-1/8-T0-4640-F |
| A12R50 | 0757-0401 |  | RESISTOR 100 OHM 18.125 W F TUBULAR | 24546 | C4-1/8-T0-101-F |
| A12R51 | 0757-0280 |  | RESISTOR 1K 1\%.125w F TUBULAR | 24546 | C4-1/8-T0-1 001-F |
| Al2U1 $\text { A } 12 \mathrm{U} 2$ | $\begin{aligned} & 1820-0054 \\ & 1820-0077 \end{aligned}$ |  | It DGTL SN74 00 N GATE  <br> IC OGTL SN74 74 N FLIP-FLOP | $\begin{aligned} & 01295 \\ & 01295 \end{aligned}$ | $\begin{aligned} & \text { SN7400V } \\ & \text { SN7474N } \end{aligned}$ |
| Al2U3 | $1820-0054$ |  | IC DGTL SN74 00 N GATE | 01295 | SN7400V |
| A12U3 | 1820-0054 |  | IC OGTL SN74 00 N GATE | 01295 | SN7400N |
| A12U5 | 1820-0068 |  | IC DGTL SN74 10 NGATE | 01295 | SN7410N |
| Al2U6 A12 | 1820-0054 |  |  |  |  |
| A 1207 Al2 A | 1820-0054 |  | IC DGTL SNT4 00 N GATE | $\left(\begin{array}{l} 01295 \\ 01295 \end{array}\right.$ | $\begin{aligned} & \text { SN7400N } \\ & \text { SN7400N } \end{aligned}$ |
| Al2U9 | 1820-0751 |  | IC DGTL SN74196N COUNTER | -1295 | $\begin{aligned} & \text { SN7400N } \\ & \text { SN74196N } \end{aligned}$ |
| A13 | 08660-60012 | 1 | BOARD ASSY, NZ OSCILLATOR | 28480 | 08660-60012 |
| A13C1 <br> A13C2 <br> A13C3 <br> A13C4 <br> A13C5 | $\begin{aligned} & 0180-0058 \\ & 0180-0228 \\ & 0180-0049 \\ & 0180-2207 \\ & 0150-0121 \end{aligned}$ |  | $\begin{aligned} & \text { CAPACITOR-FXD; } 50 \cup F+75-10825 V D C \text { AL } \\ & \text { CAPACITOR-FXD; } 22 U F+10815 \mathrm{VDC} \text { TA-SOLIO } \\ & \text { CAPACITOR-FXD; } 20 U F+75-10850 \mathrm{VOC} \text { AL } \\ & \text { CAPACITOR-FXD; 100UF+108 } 10 \mathrm{VDC} \text { TA } \\ & \text { CAPACITOR-FXD } 10 \mathrm{HF}+80-20850 \mathrm{WVOC} \text { CER } \end{aligned}$ | $\begin{aligned} & 56289 \\ & 56289 \\ & 56289 \\ & 56289 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 3005065025 \mathrm{CC2} \\ & 1500226 \times 9015 R 2 \\ & 3002066050 \mathrm{CC} 2 \\ & 1500107 \times 0010 R 2 \\ & 0150-0121 \end{aligned}$ |

Table 6-3. Replaceable Parts


Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & A 13 R 11 \\ & A 13 R 12 \\ & A 13 R 13 \\ & A 13 F 14 \\ & A 13 R 15 \end{aligned}$ |  |  |  | [ 24546 | $C 4-1 / 8-T O-1002-F$ $C 4-1 / 8-T 0-1002-F$ $C 4-1 / 8-T O-1002-F$ $C 4-1 / 8-T 0-1002-F$ $C 4-1 / 8-T 0-1002-F$ |
| $\begin{aligned} & A 13 R 16 \\ & A 13 R 17 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0757-0479 \end{aligned}\right.$ |  | RESISTER 10K 1\% . 125 W F TUBULAR RESISTDR 302K 1\% • 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 19701 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-\text { TO-1 002-F } \\ & \text { MF4C1/8-T 0-3023-F } \end{aligned}\right.$ |
| A13R18 | 0757-0472 |  | RESISTOP 200K 19.125H F TUBULAR. | 24546 | C4-1/8- ${ }^{\text {c }}$-2003-F |
| 413919 | 0757-0465 |  | RESISTOR 100K 18.125W F TUPILLAR | 24546 | C4-1/8-T0-1 003-F |
| A13R20 | 0698-3228 |  | RESISTER 49.9K 12. .125W F TURULAR | 07716 | CEA 1/9-T0-4 991-F |
| $\begin{aligned} & A 13 R 21 \\ & A 13 R 22 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0124 \\ & 0757-0449 \end{aligned}\right.$ | 2 | RFSISTOR 30.2K 1\% . 125W F TUBULAR RESISTOR 2OK 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C .5-1 / 4-T 0-3922-F \\ & \mathrm{C} \\ & \hline \text { - } 1 / 8-\mathrm{T} 0-2002-\mathrm{F} \end{aligned}\right.$ |
| A13R23 | 0757-0442 |  | RFSISTOR 10K 18.125 W F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| A 13 R 24 | 0698-4002 |  | RESISTOR $5 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 16299 | (C4-1/8-T0-5001-F |
| A13R25 | 0757-0442 |  | RESISTOR 10K 1\% . 125 W F TUBULAR | 24546 | (C4-1/8-T0-1 002-F |
| A13R26 | 0698-0085 |  | RESISTOR 2.61 K 1 t ( 125 H F TUPULAR | 16299 | C4-1/8-T0-2611-F |
| A13R27 | 0757-0274 |  | RESISTOR $1.21 \mathrm{~K} 1 \% .125 \mathrm{HF}$ FUBULAR | 24546 | C4-1/8-T0-1213-F |
| A13P30 | 0757-0290 |  | RESISTOR 6.19 K 1\% 125 W F TUBULAR | 24546 19701 | MF4C1/8-T0-6191-F |
| $\begin{aligned} & A 13 R 31 \\ & A 13 R 32 \end{aligned}$ | \|o698-3162 |  | RFSISTOR 46.4K 1\% . 125 W F TUBULAR RESISTOR 4.64K 1\% .125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-4642-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-4641-\mathrm{F} \end{aligned}$ |
| A13R33 | 0698-0085 |  | RFSISTOR 2.61 K 18.125 HF TUBULAR | 16299 | C4-1/8-T0-2611-F |
| A13R34 | 0757-0421 |  | RESISTOR 825 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A13R35 | 0698-4037 |  | RESISTOR 46.4 OHM 12.125W F TUBULAR | 16299 | C4-1/8-T0-46R4-F |
| $\begin{aligned} & E 13 R 36 \\ & A 13237 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3156 \\ & 2100-1759 \end{aligned}\right.$ |  | RESISTOP 14.7K 1\% . 125W F TUBULAR RESISTOR; VAR; TRMR; 2KOHM $5 \$$ WH | $\begin{aligned} & 16299 \\ & \text { GB } 027 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-1472-\mathrm{F} \\ & \mathrm{CT} \text {-106-4 } \end{aligned}$ |
| A13R38 |  |  |  |  |  |
| A13R39 | 2100-1760 |  | RFSISTOR; VAR; TRMR; 5KOHM 5\% WH | G8 027 | $C T-106-4$ |
| A13240 | 0757-0441 |  | RESISTOR 8.25K 1\% .125W F TUSULAR | 24546 | C4-1/8-T0-8251-F |
| A 13841 A $13 R 42$ A | 0757-0279 |  | RESISTOR RESISTOR R | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\mid C 4-1 / 8-T 0-3161-F$ |
| A13043 | 0757-0199 |  | $\begin{array}{ll}\text { RFSTSTOR } & 21.5 \mathrm{~K} \\ \text { 1\% }\end{array}$ | 24546 | C4-1/8-T0-2152-F |
| A 13844 | 0757-0442 |  | RESISTIR $10 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C4-1/8-T0-1 002-F |
| A13R45 | 0757-0834 |  | RESISTOR 5.62 K 18.5 W F TUBULAR | 19701 | MF7C1/2-T0-5621-F |
| A 13 R 46 A 13247 | $\left\lvert\, \begin{gathered} 0698-3459 \\ 0698-0082 \end{gathered}\right.$ |  | RESI STOR 383 K 1\% . 125 W F TUBULAR RESISTOR 464 OHM 1\%.125W F TUBULAR | $\begin{array}{\|l} 19701 \\ 16299 \end{array}$ | $\left\lvert\, \begin{aligned} & \text { MF4C1/8-T0-3833-F } \\ & C 4-1 / 8-T 0-4640-F \end{aligned}\right.$ |
| A13R48 | 0698-3441 |  | RESISTOR 215 OHM 1\%.125W F TUBULAR | 16299 | C4-1/g-ro-215R-F |
| A 13 R 49 | 0698-3266 |  | RESISTOR 237K 18.125W F TUBULAR | 16299 | C4-1/8-T0-2373-E |
| A 13 R 50 | 0698-3447 |  | RESISTOR 422 OHM 1\%.125 F TUBULAR | 16299 . | C4-1/8-T0-422R-F |
| $\begin{aligned} & A 13 R 51 \\ & A 13 R 52 \end{aligned}$ | 0757-0443 |  | NOT ASSIGNED RESISTOP 11K 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-1 102- |
| A13R53 | 0698-3266 |  | RESISTOR 237 K 18. 125 W F TUBULAR | 16299 | C4-1/8-T0-2373-F |
| A13R54 | 0698-3445 |  | RESISTOR 348 OHM $1 \% .125 W$ F TUBULAR | 16299 | C4-1/8-TO-348R-F |
| A13255 | 0698-3243 |  | RESISTOR 178K 1\% . 125W F TUBULAR | 16299 | C4-1/8-T0-1783-F |
| $\begin{aligned} & \text { A13R56 } \\ & \text { A13R57 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3443 \\ & 0757-0401 \end{aligned}\right.$ |  | RESI STOR 287 OHM 1\%.125W F TUBULAR RESISTOR 100 OHM $1 \%$. 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \end{aligned}$ | $\mathrm{C} 4-1 / 8-\mathrm{TO-2} 87 \mathrm{R}-\mathrm{F}$ $\mathrm{C} 4-1 / 8-\mathrm{TO-101-F}$ |
| A13R58 | 0693-3243 |  | $\begin{array}{ll}\text { RESISTDR } & 178 \mathrm{~K} \\ \text { 18 }\end{array}$ | 16299 | C4-1/8-T0-1783-F |
| A 13259 | 0698-3132 |  | RESISTOR 261 OHM 12.125 W F TUBULAR | 16299 | C4-1/8-T0-2610-F |
| A 13860 | 0757-0466 |  | RESISTOR 110K 18.125 W F TUBULAR | 24546 | C4-1/8-T0-1103-F |
| $\begin{aligned} & A 13 R 61 \\ & \text { A } 13 \text { R62 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3440 \\ & 0683-3245 \end{aligned}\right.$ |  | RESISTOR 196 DHM $1 \% .125 \mathrm{~W}$ F TUBIJLAR RESISTOR 820K 5\% . 25W CC TUBULAR | $\left\lvert\, \begin{aligned} & 16299 \\ & 01121 \end{aligned}\right.$ | $\begin{aligned} & \text { C4-1/8-TO-196R-F } \\ & \text { CRR245 } \end{aligned}$ |
| A 13 R63 | 0698-3243 |  | RESISTIR 178K 1\% - 125 W F TUBULAR | 16299 | C4-1/8-TO-1783-F |
| A 13 R 64 | 0757-0442 |  | RESISTOR 10K 1 \% . 125 W F TUBULAR | $24546$ | $\mathrm{C} 4-1 / 8-\mathrm{TO}-1002-\mathrm{F}$ |
| A13R65 | 0757-0467 |  | RESISTOR 121K 1\% . 125 W F TUBULAR | $24546$ | C4-1/8-T0-1213-F |
| A13R66 A $13 R 67$ |  |  | RESISTOR 178 DHM 1\% . 125 W F TUBULAR RESISTOR 196 DHM $1 \% .125 \mathrm{~W}$ F TUBULAR |  |  |
| A 13 R667 A 13 P 68 A | $\left\lvert\, \begin{aligned} & 0698-3440 \\ & 0698-0082 \end{aligned}\right.$ |  | RESISTOR 196 DHM $1 \%$. 125 W F TUBULAR RESISTOR 464 OHM $1 \% .125 W$ F TUBULAR | $\begin{aligned} & 15290 \\ & 16299 \end{aligned}$ | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-196 \mathrm{R}-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-4640-\mathrm{F} \end{aligned}\right.$ |
| A13R68 A13R69 | 0698-0082 |  | RESISTOR 464 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 90.9 K 18.125 FF TUBULAR | 16299 24546 | C4-1/8-T0-4640-F $\mathrm{C} 4-1 / 8-70-9092-\mathrm{F}$ |
| $\Delta 13 \mathrm{R} 70$ | 0757-0405 |  | RESISTOR 162 DHM 18.125 W F TUBULAR | 24546 | C4-1/8-TO-162R-F |
| $\begin{aligned} & A 13 R 71 \\ & A 13 R 72 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0461 \\ & 0698-3437 \end{aligned}\right.$ |  | RESISTOR 68.1K $1 \%$. 125 W F TUBULAR RESISTOR 133 OHM $1 \%$. 125W F TUBULAR | $\left\lvert\, \begin{aligned} & 24546 \\ & 16299 \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / \mathrm{B}-\mathrm{TO}-6812-F \\ & \mathrm{C} 4-1 / \mathrm{R}-\mathrm{T} 0-133 \mathrm{R}-\mathrm{F} \end{aligned}\right.$ |
| A13R73 | 0757-0200 |  | RESISTOR 5.62 K 1\% $\mathrm{S}^{\text {P }}$.125W F TUBULAR | 24546 | C4-1/8-T0-5621-F |
| A13R74 | 0698-3154 |  | RESISTOR 4.22K 1\% .125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16900 \end{aligned}$ | $\mathrm{C} 4-1 / 8-T 0-4221-F$ |
| A13R75 | 0698-3445 |  | RESISTOP 348 OHM $1 \%$. 125 W F TUBULAR | $16299$ | C.4-1/8-TO-348R-F |
| A13R76 A13R77 | $\left\lvert\, \begin{aligned} & 0757-0403 \\ & 0698-3444 \end{aligned}\right.$ |  | RESISTOR 121 OHM 17 . 125W F TURULAR RESISTOR 316 OHM 18 . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-121 R-F \\ & C 4-1 / 8-T O-316 R-F \end{aligned}\right.$ |
| A13R78 | -0698-3444 |  |  | 16299 24546 | C4-1/8-T0-316R-F |
| A13R79 | 0698-3442 |  | RESISTIR 237 OHM 1 \% 0.125 W F TUBULAR | 16299 | C4-1/8-T0-237R-F |
| A13R80 | 0698-3132 |  | RESISTOR 261 DHM 1\%.125W F TUBULAR | 16290 | C4-1/8-T0-2610-F |
| $\begin{aligned} & A 13 R 81 \\ & A 13 R B 2 \\ & A 13 R 83 \\ & A 13 R 84 \\ & A 13 R 85 \end{aligned}$ | $\begin{aligned} & 0698-3442 \\ & 0757-0400 \\ & 0698-3438 \\ & 0698-3441 \\ & 0698-3441 \end{aligned}$ |  | RESISTOR 237 OHM 1\% . 125W F TUBULAR RESISTOQ 90.9 OHM 1\%.125W F TUBULAR RESISTOR 147 OHM 1\% . 125W F TUBULAR RESISTOR 215 OHM $1 \%$. 125W F TUBULAR RESISTOR $215 \mathrm{OHM} 1 \% .125 \mathrm{~N}$ F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-237 R-F \\ & \mathrm{C} 4-1 / 8-T 0-90 R 9-F \\ & \mathrm{C} 4-1 / 8-T 0-147 R-F \\ & \mathrm{C} 4-1 / 8-T 0-215 R-F \\ & \mathrm{C} 4-1 / 8-T 0-215 R-F \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & A 13 U 1 \\ & A 13 U 2 \\ & A 13 U 3 \end{aligned}$ | $\begin{aligned} & 1820-0054 \\ & 1820-0054 \\ & 1820-0054 \end{aligned}$ |  | IC DGTL SN74 00 N GATE <br> IC GGTL SN74 00 N GATF <br> IC DGTL SN74 00 N GATE | $\begin{aligned} & 01205 \\ & 01295 \\ & 01295 \end{aligned}$ | $\begin{aligned} & \text { SN740NN } \\ & \text { SN7400Y } \\ & \text { SN74300N } \end{aligned}$ |
| A 14 | 08660-60011 | 1 | BOARD ASSY, N2 PHASF DETECTOR (EXCEPT OPT 004) | 29480 | 08660-50311 |
| A 14 | 08660-60039 | 1 | BOARD ASSY. N2 PHASE DETECTOR (OPT 004 ONLY) | 28490 | 08650-60039 |
| A14C1 <br> A14C2 <br> A14C3 <br> $\triangle 14 \mathrm{C} 4$ <br> A14C5 | $\begin{aligned} & 0160-2055 \\ & 0180-0058 \\ & 0180-2206 \\ & 0180-0228 \end{aligned}$ |  | CAPACITOR-FXD .OLUF +80-202 10OWVDC CER NOT ASSIGNED <br> CAPACITOR-FXI; 50UF+75-10\% 25VDR AL <br> CAPAC.ITOR-FXD; 6OUF+-10\% 6VDC TA-SOLID <br> CAPACITOR-FXD; 22UF+-10\% 15VDC TA-SOLID | $\begin{aligned} & 28490 \\ & 56289 \\ & 58289 \\ & 56299 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 30050650255 C 2 \\ & 1500606 \times 9006 R 2 \\ & 1500225 \times 901582 \end{aligned}$ |
| $\begin{aligned} & A 14 C 6 \\ & A 14 C 7 \\ & A 14 C 8 \\ & A 14 C D \\ & A 14 C 10 \end{aligned}$ | $\begin{array}{lll} 0 & 150-0121 \\ 0 & 180-0229 \\ 0 & 150-0121 \\ 0 & 160-0157 \\ 0 & 160-20 & 55 \end{array}$ |  | CAPACITOR-FXD . 1UF +80-20\% 50WVDC CER CAPACITOR-FXD; 33UFt-10\% 1OVOC TA-SOLID CAPACITOR-FXD •1UF +80-20\% 50WVDC CER CAPACITOR-FXD 4700PF +-10\% 200WVOC DOLYE CAPACITCR-FXD. $014 F+80-20 \%$ 100WVDC CER | $\begin{aligned} & 28480 \\ & 55289 \\ & 28480 \\ & 56289 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0150-0121 \\ & 1500336 \times 01092 \\ & 0150-0121 \\ & 202947292 \\ & 0150-2055 \end{aligned}\right.$ |
| A14C11 <br> A14Cl 2 <br> A14Cl 3 <br> A14C14 <br> A14C15 | $\begin{array}{lll} 0 & 150-0121 \\ 0 & 150-0121 \\ 0 & 160-2055 \\ 0 & 140-0172 \\ 0 & 160-2055 \end{array}$ |  | CAPACITCR-FXD . 1 UF +80-20\% 50WVDC CER CAPACITOR-FXD -1UF +80-20\% 50WVDC CER CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER CAPACITCR-FXD 3000 PF +-1\% 100WVDC MICA CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER | $\begin{aligned} & 28490 \\ & 28480 \\ & 28480 \\ & 72136 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0150-0121 \\ & 0150-0121 \\ & 0160-2055 \\ & 0 M 19 F 302501 \text { OOWV1CR } \\ & 0160-2055 \end{aligned}$ |
| A14C16 <br> A14C17 <br> A14Cl 8 <br> A14C19 <br> A14C20 | $\left\lvert\, \begin{array}{cccc} 0 & 150-0 & 1 & 21 \\ 0 & 150 & 50-0 & 1 \\ 0 & 150 & 21 \\ 0 & 160-20 & 161 \\ 0 & 160-20 & 55 \\ \hline \end{array}\right.$ |  | CAPACITOR-FXD .IUF +80-20\% 50WVDC CER CAPACITOR-FXD . 1UF +80-208 50WVDC CER CAPACITOR-FXC . IUF + BO-208 50WVDC CER CAPACITDR-FXD .OLUF +80-20\% 100WVDC CER CAPACITOR-FXD .O1UF +80-20\% 100HVDC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0150-0121 \\ & 0150-0121 \\ & 0150-0121 \\ & 0160-2055 \\ & 0160-2055 \end{aligned}\right.$ |
| $\begin{aligned} & A 14 C 21 \\ & A 14 C 22 \\ & A 14 C 23 \\ & A 14 C 24 \\ & A 14 C 25 \end{aligned}$ | $\begin{array}{ll} 0 & 160-2055 \\ 0 & 160-3539 \\ 0 & 160-2453 \\ 0 & 170-0040 \\ 0 & 180-0229 \end{array}$ |  | CAPACITOR-FXD .O1UF +80-205 100WVDC CER CAPACITOR-FXD 820PF +-5\% 100WVDC MICA CAPACITOR-FXD . $22 U F+-10 \%$ 8OWVDC POLYE CAPACITCR-FXD .047UF +-10\% 200WVDC POLYE CAPACITOR-FXD; 33UF+-10\% 10VDC TA-SILIO | $\begin{aligned} & 28480 \\ & 28480 \\ & 84411 \\ & 56289 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0160-3539 \\ & H E W-238 T \\ & 292 P 47392 \\ & 1500336 \times 01082 \end{aligned}$ |
| A14C26 | 0180-0374 |  | CAPACITOR-FXD; 10UF+-102 2OVOC TA-SOLIO | 58289 | $1500106 \times 02082$ |
| A 14 CR 1 <br> A 14 CR 2 <br> A14CR 3 <br> A14CR4 | $\begin{aligned} & 1901-0040 \\ & 1901-0040 \\ & 1901-1086 \\ & 1901-1066 \end{aligned}$ | 2 | DIODE-SWITCHING 2NS 30V 5OMA DIOOE-SWITCHING 2NS 30V 50MA DIODE-SWITCHING $750 P S$ 15V 50MA DIODE-SHITCHING 75 OPS $15 V$ 50MA | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1901-0040 \\ & 1901-0040 \\ & 1901-1066 \\ & 1901-1066 \end{aligned}$ |
| $\begin{aligned} & \text { A 14L1 } \\ & \text { A14L2 } \end{aligned}$ | $\begin{aligned} & 9100-1629 \\ & 9140-0114 \end{aligned}$ |  | COIL ; FXD; MOLDED RF CHOKE: 47UH 5\% <br> COIL: FXD: MOLDED RF CHOKE; 10UH 10\% | $\begin{aligned} & 24226 \\ & 24226 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 15 / 472 \\ & 15 / 102 \end{aligned}\right.$ |
| A1413 | 9100-1629 |  | COIL F FXD; MOLDED RF CHOKE; 47UH 5\% | 242226 | 15/472 |
| A1414 | $9140-0179$ $9140-0114$ |  | COIL ; FXD; MOLDED RF CHOKE; 22UH 10\% COIL ; FXD; MOLDED RF CHOKE; 10UH 102 | 24226 24226 | $\begin{aligned} & 15 / 222 \\ & 15 / 102 \end{aligned}$ |
| A14L6 <br> A14L7 <br> A14L8 | $\begin{aligned} & 9100-1614 \\ & 9100-1650 \\ & 9100-1652 \end{aligned}$ | 2 | ```COIL: FXD; MOLDED RF CHOKE; .82UH 10% COIL: FXD; MOLDED RF CHOKE; 68OUH 5% COIL: FXD; MOLDED RF CHOKE; 82OUH 5%``` | $\begin{aligned} & 24226 \\ & 24226 \\ & 24226 \end{aligned}$ | $\begin{aligned} & 15 / 820 \\ & 19 / 683 \\ & 19 / 823 \end{aligned}$ |
| 41401 <br> A 1402 <br> A 1403 <br> A 1404 <br> A 1405 | $\begin{aligned} & 1853-0034 \\ & 1853-0034 \\ & 1853-0034 \\ & 1855-0049 \\ & 1854-0045 \end{aligned}$ |  | TRANSISTOR PNP SI CHIP TO-18 PD=360MW <br> TRANSISTOR PNP SI CHIP TO-18 PD $=360^{\mathrm{MW}}$ <br> TRANSISTOF PNP SI CHIP TO-18 PD=360MH <br> TRANSISTOR; JFET;DUAL; N-CHAN D-MODE SI TRANSISTOR NPN SI TO-18 PD=500MW | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1853-0034 \\ & 1853-0034 \\ & 1853-0034 \\ & 1855-0049 \\ & 1854-0045 \end{aligned}$ |
| $\text { A } 1406$ $\text { A } 1407$ | $\left\lvert\, \begin{aligned} & 1853-0015 \\ & 1854-0092 \end{aligned}\right.$ |  | TRANSISTOR PNP SI CHIP PD=200MH <br> TRANSISTOR NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1853-0015 \\ & 1854-0092 \end{aligned}$ |
| A14R1 <br> A14R2 <br> A14R3 <br> A14R4 <br> A14R5 | $\begin{aligned} & 0757-0289 \\ & 0698-0082 \\ & 0757-0439 \\ & 0698-0085 \\ & 0757-0416 \end{aligned}$ |  | RESISTOR 13.3K 1\% . 125 W F TUBULAR RESISTOR 464 OHM 1 \% -125W F TUBULAR RESISTOR 6.81K 1\% . 125 W F TUBULAR RESISTOR 2.61K $1 \%$.125W F TUBULAR RESISTOR 511 DHM $1 \% .125 \mathrm{~W}$ F TUBULAR | $\begin{aligned} & 19701 \\ & 16299 \\ & 24546 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \text { MF4C1/8-TO-1332-F } \\ & \text { C4-1/8-T0-4S40-F } \\ & \text { C. } 4-1 / 8-T 0-6811-F \\ & \text { C4-1/B-T0-2611-F } \\ & \text { C4-1/8-T0-511R-F } \end{aligned}$ |
| A14R6 <br> A14R7 <br> A14R8 <br> A14R9 <br> A14R10 | $\begin{aligned} & 0757-0416 \\ & 0757-0442 \\ & 0698-3446 \\ & 0757-0424 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 511 OHM $1 \%$. $125 W^{\prime} F$ TUBULAR RESISTOR 1OK 1\% . 125W F TUBULAR RESISTOR 383 OHM 1\% . 125 W F TUBULAR RESISTOR 1.1K 1\% . 125W F TUBULAR RESISTOR 10K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-5112-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / R-T O-383 R-F \\ & C 4-1 / 8-T 0-1101-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}\right.$ |
| A14R11 <br> A 14 R1 2 <br> A14R13 <br> A14R14 <br> A14R15 | $\begin{aligned} & 0757-0424 \\ & 0757-0416 \\ & 0698-3450 \\ & 0757-0447 \\ & 0698-3430 \end{aligned}$ |  | RESISTOR 1.1K 1\% . 125W F TUBULAR RESISTOR 511 OHM 1 . . 125N F TUBULAR RESISTOR 42.2K 1\% .125W F TUBULAR RESTSTOR 16.2K $1 \%$.125W F TUBULAR RESISTOR 21.5 OHM 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 03888 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1101-F \\ & C 4-1 / 8-T 0-511 R-F \\ & C 4-1 / 8-T 0-4222-F \\ & C 4-1 / 8-T 0-1622-F \\ & \text { PME } 55-1 / 8-T O-21 R 5-F \end{aligned}$ |
| A14R16 <br> A14R17 <br> A14R18 <br> A14R19 <br> A14R20 | $\begin{aligned} & 0757-0424 \\ & 0757-0421 \\ & 0698-3447 \\ & 0757-0279 \\ & 0757-0279 \end{aligned}$ |  | RESISTOR 1.1K 1\% . 125 W = TUBULAR RESISTOR 825 OHM 1 \% . 125W F TUBULAR RESISTOR 422 OHM 1\% . 125 W F TUBULAR RESISTOR 3.16K 1\% . 125 W F TUBULAR RESISTOR 3.16K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 15290 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1101-F \\ & C 4-1 / 8-T 0-825 R-F \\ & C 4-1 / 8-T 0-422 R-F \\ & C 4-1 / 8-T 0-3161-F \\ & C 4-1 / 8-T 0-3181-F \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $A 14 R 21$ $A 14 F 22$ $A 14 R 23$ $A 14 R 24$ $A 14 P 25$ | $0757-0279$ $0698-3155$ $0757-0290$ $0698-3150$ $0757-0394$ |  |  | 24546 16299 19701 16299 24546 | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-3181-F \\ & \mathrm{C} 4-1 / 8-T 0-4641-\mathrm{F} \\ & \text { MF4C1/8-T0-6191-F } \\ & \mathrm{C} 4-1 / 8-\mathrm{TO-2371-F} \\ & \mathrm{C} 4-1 / 8-T 0-51 P 1-F \end{aligned}$ |
| $\begin{aligned} & A 14 R 26 \\ & A 14 R 27 \\ & A 14 R 2 B \\ & A 14 R 29 \\ & A 14 P 30 \end{aligned}$ | $\begin{aligned} & 0757-0394 \\ & 0757-0416 \\ & 0757-0442 \\ & 0757-0200 \\ & 0757-0424 \end{aligned}$ |  | RFSISTOR 51.1 OHM 1\%.125W F TUBULAR RESISTOR 511 OHM 19.125 W F TUBULAR RESISTOR $10 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 5.62K 18.125H F TUBULAR RESISTOR 1.1 K 1\% . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24446 \\ & 24546 \\ & 24456 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-T 0-511 R-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-1101-F \end{aligned}$ |
| $\begin{aligned} & A 14 R 31 \\ & A 14 P 32 \\ & A 14 R 33 \\ & A 14 R 34 \\ & A 14 \mathrm{~F} 35 \end{aligned}$ | 0757-0438 <br> 0757-0444 <br> 0757-0444 <br> 0757-0424 <br> 0757-1094 |  | RESISTOR 5.11K 1\%. 125 W F TUBULAR RESISTOR 12.1K 1\% . 125 W F TUBULAR RFSISTOR 12.1 K 1\% .125W F TU3ULAR RESISTOR 1.1 K 12. 125 W F TUBIMAP. RESISTOQ 1.47 K 1\% . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24446 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ |  |
| A14R36 | 0757-0416 |  | RESISTOR 511 OHM 1\% . 125 H F TUBULAR | 24546 | C4-1/8-TO-511R-F |
| A 14 T1 | 08660-80001 |  | TRANSFORMER, SAMPLER | 28480 | 08660-80001 |
| $\begin{aligned} & A 14 U 1 \\ & A 114112 \\ & A \\ & A 14 U 3 \\ & A 14144 \\ & A \\ & A 1415 \end{aligned}$ | $\begin{aligned} & 1820-0451 \\ & 1820-0204 \\ & 1820-0469 \\ & 1820-0451 \\ & 1820-0751 \end{aligned}$ |  | IC DGTL MC 3062P FLIP-FLOP IC DGTL MC 3006D GATE If DGTL SN74H 102 N FLIP-FLOP IC DGTL MC 3062P FLIP-FLOP IC DGTL SN74196N COUNTER | $\begin{aligned} & 04713 \\ & 04713 \\ & 01295 \\ & 04713 \\ & 01295 \end{aligned}$ | MC3052 ${ }^{\circ}$ MC 3006P SN74H 102 N MC3062P SN74196N |
| $\begin{aligned} & A 14 U 6 \\ & A 14 U 7 \\ & A 14 U 8 \end{aligned}$ | $\begin{aligned} & 1820-0751 \\ & 1820-0751 \\ & 1820-0054 \end{aligned}$ |  | IC OGTL SN74196N COUNTER <br> IC DGTL SN74196N COUNTER <br> IC DGTL SN74 00 N GATE | $\begin{aligned} & 01295 \\ & 01295 \\ & 01295 \end{aligned}$ | $\begin{aligned} & \text { SN74196N } \\ & \text { SN74196N } \\ & \text { SN7400V } \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A 14 | 08660-60039 | 1 | BCARD ASSY, N2A PHASE DETFCTOR (OPT 004 ONLY) | 23480 | 08660-50039 |
| A14Cl | 0160-2055 | 8 | CAPACITTR-FXD . 010 F +80-20\% 100 WVDC CER | 23480 | 0160-2055 |
| A 14 Cl 2 | 0180-0053 | 1 | CAPACITOR-FXD; $50 \cup \mathrm{~F}+75-10 \% 25 \mathrm{VDC} \mathrm{AL}$ | 56299 | $3005065025 \mathrm{CC2}$ |
| A 14.4 | 0180-2206 | 1 | CAPACITOR-FXD; 6OUF+-10\% GVDC TA-SOLID | 56299 | $1500605 \times 900682$ |
| A 14 CL | 0180-0228 | 1 | CAPACITTRR-FXD: $22 U \mathrm{Ft-10} \mathrm{\%} 15 \mathrm{VDC} \mathrm{TA-SOLID}$ | 55289 | $150 \mathrm{C} 25 \times 9015 \mathrm{B2}$ |
| A14C5 | 0150-0121 | 7 | CAPACITAR-FXD . $1 \mathrm{CF}+80-20 \% 50 W \mathrm{VDC} \mathrm{CER}$ | 28480 | 0150-0121 |
| $\begin{aligned} & A 14 C 6 \\ & A 14 C 7 \end{aligned}$ | $\left\lvert\, \begin{array}{lll} 0 & 160-2055 \\ 0 & 150-0121 \end{array}\right.$ |  | CAPACITOR-FXD .O1UF +80-20\% 100WVDC CER CAPACITOR-FXD . 1 UF $+80-20 \%$ 50WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0150-2055 \\ & 0150-0121 \end{aligned}\right.$ |
| A 14 CB | 0150-0121 |  | CAPACITOR-FXD .1UF +80-20\% 50 WVOC CER | 23480 | 0150-0121 |
| A14C9 | 0160-0157 | 1 | CAPACITOR-FXD 4700 PF +-10\% 200WVDC POLYE | 56289 | 292 P 47292 |
| A14C10 | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER | 23480 | 0160-2055 |
| A 14C11 | 0150-0121 |  | CAPACITCR-FXD .1UF +80-20\% 50WVDC CER | 28480 | 0150-0121 |
| A 14C12 | 0150-0121 |  | CAPACITOR-FXD . IUF +80-20\% 50WVDC CER | 28480 | 0150-0121 |
| A 14 Cl 3 | 0150-0121 |  | CAPACITOR-FXD . $1 \mathrm{UF}+80-20 \% 50 \mathrm{VVDC}$ CER | 28480 | 0150-0121 |
| A 14 Cl 14 | 0160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100WVDC CER | 28480 | 0180-2055 |
| A14C15 | 0140-0172 | 1 | CAPACITAP-FXD 3000PF +-18 100WVDC MICA | 72136 | CM1 OF 302F01 00WVICR |
| ${ }^{\text {A } 14 C 18 ~}{ }^{\text {A14C17 }}$ | 0180-0229 | 2 | CAPACITOR-FXD; 33UF+-10\% 10VDC TA-SOLID CAPACITIR-FXD 0 IUF +80-20\% 100 WVDC CER | $56289$ $28480$ | $\begin{aligned} & 1500336 \times 901032 \\ & 0160-2055 \end{aligned}$ |
| ${ }^{\text {A } 14 C 17}$ | - $\begin{aligned} & 0180-2055 \\ & 0150-0121\end{aligned}$ |  |  | 28480 28480 | (0180-2055 |
| A14C19 | 0180-0374 | 1 | CAPACITTR-FXD; 10UF+-10\% 20VDC TA-SOLID | 56289 | $1500105 \times 902082$ |
| A14C20 | 0160-2055 |  | C.APACITOR-FXD .OIUF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A 14 C 21 A 14 C 22 | $0160-2055$ $0180-0229$ |  | CAPACITOR-FXD . O1UF +80-20\% 100WVDC CER CAPACITOR-FXD; $334 \mathrm{~F}+10 \% 10 \mathrm{VDC} \mathrm{TA-SOLID}$ | 28480 56299 | $\begin{aligned} & 0150-2055 \\ & 1500335 \times 901082 \end{aligned}$ |
| A 14 C 22 A14C23 | $0180-0229$ $0160-3539$ | 1 | CAPACITDR-FXD 820PF +-5\% 100WVDC MICA | 28480 | 150033 0160 -35 ${ }^{\text {1 }}$ |
| A14C24 | 0 160-2453 | 1 | CAPACITOR-FXD .? 2UF +-10\% 80WVDC PDLYE | 84411 | HEW-238T |
| A 14C25 | 0170-0040 | 1 | CAPACITOR-FXD .047UF +-10\% 200WVDC PDLYE | 56289 | 292P47392 |
| A14C26 | 0160-2055 |  | CAPACITMR-FXD .OLUF +80-20\% 100WVDC CER | 28480 | 0160-2055 |
| A 14CR 1 A $14 C R 2$ | $\text { \|l\|l\|l\|} \left\lvert\, \begin{aligned} & 1901-0040 \\ & 1901-1066 \end{aligned}\right.$ | $\begin{aligned} & 2 \\ & 2 \end{aligned}$ | DIODE-SWITCHING 2NS 3OV 5OMA DIODE-SWITCHING 75 OPS 15V 50MA | 28480 28480 | $\left\lvert\, \begin{aligned} & 1901-0040 \\ & 1901-1066 \end{aligned}\right.$ |
| A14CR 3 | 1901-1066 |  | DIODE-SWITCHING 75OPS 15V 50MA | 28480 | 1901-1066 |
| ${ }^{\text {A } 1421}$ | 9100-1629 | 2 | COIL : FXD: MOLDED RF CHOKE: 47UH 5\% | 24226 |  |
| A14L2 A14L3 | $9140-0114$ $9100-1629$ | 2 | COIL ; FXD; MOLDED RF CHOKE; 10UH 10\% COIL: FXD; MDLDED RF CHDKE; $47 \mathrm{UH} 5 \%$ | 24226 24226 | $\left\lvert\, \begin{aligned} & 15 / 102 \\ & 15 / 472 \end{aligned}\right.$ |
| A14L3 A 1424 | $9100-1629$ $9100-1650$ | 1 | COIL : FXD; MDLDED RF CHDKE; $47 \mathrm{UH} 5 \%$ COIL FXD; | 24226 24226 | $15 / 472$ $19 / 683$ |
| A14L5 | 9100-1652 | 1 | COIL ; FXD; MOLDED RF CHOKE; 82OUH 5\% | 24226 | $19 / 823$ |
| A14L6 | 9140-0114 |  | COIL ; FXD; MDLDED RF CHDKE; 10UH 10\% | 24226 | $15 / 102$ |
| A 1401 | 1853-0034 | 3 | TRANSISTOR PNP SI CHIP TO-18 PD=360MW | 28480 | 1853-0034 |
| A1402 A1403 | $1854-0210$ $1853-0034$ | 2 | TRANSISTOR NPN 2 N2 222 SI $P D=500 \mathrm{MW}$ | 04713 28480 | $\begin{aligned} & 2 N 2222 \\ & 1853-0034 \end{aligned}$ |
| A 1403 A1404 | $1853-0034$ $1853-0015$ | 1 | TRANSISTOR PNP SI TRANSISTOR TR | 28480 29480 | 1853-0034 |
| A1405 | 1854-0210 |  | TRANSISTOR NPN 2N2222 SI PD=500MW | 04713 | 2N2222 |
| A1406 A 1407 | $\left\lvert\, \begin{array}{l\|l} 1853-0034 \\ 1855-0049 \end{array}\right.$ | 1 | TRANSISTOR PNP SI CHIP TO-18 PD=360MW TRANSISTOR: JFET;DUAL: N-CHAN D-MODE SI | $\begin{aligned} & 23480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1853-0034 \\ & 1855-0049 \end{aligned}$ |
| A14R1 | 0757-0440 | 1 | RESISTOR 7.5K 1\% . 125W F TUBULAR | 24546 | C4-1/8-T0-7501-F |
| A14R2 | 0757-0421 | 2 | RESISTOR 825 DHM 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A14R3 | 0757-0280 | 3 | RESISTOR 1K 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-1 001-F |
| A14R4 | 0757-0280 |  | RESISTOR 1K 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-1 001-F |
| A14R5 | 0757-0442 | 3 | RESISTOR 10K 1\% . 125 W F TUBULAR | 24546 | C4-1/8-T0-1 002-F |
| A14R6 | 0698-3446 | 1 | RESISTOP 383 OHM 1\% . 125W F TUBULAR | 16299 | $\mathrm{C} 4-1 / 8-T 0-383 \mathrm{P}-\mathrm{F}$ |
| A14R7 A $14 R 8$ | 0698-0082 | 1 | RESISTOR 464 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR <br> RESISTOR <br> 13.3 K <br> $1 \% .125 \mathrm{~W}$ <br> F TUBULAR | 16299 | C4-1/8-T0-4640-F MF4C1/8-T0-1332-F |
| A14R9 | 0757-0439 | 1 | RESISTOR 6.81K 1\% .125W F TUBULAR | 24546 | C 4-1/8-T0-6811-F |
| A14R10 | 0757-0280 |  | RESISTOR 1K 1\%.125W F TUBULAR | 24546 | C4-1/8-T0-1001-F |
| $\begin{aligned} & \text { A } 14 \text { R1 } 1 \\ & \text { A } 14 R 12 \end{aligned}$ | $\begin{aligned} & 0757-0442 \\ & 0757-0424 \end{aligned}$ | 4 | RESISTOR 10K 1\% . 125W F TUBULAR RESISTOR 1.1K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1101-F \end{aligned}$ |
| A14R13 | 0757-0416 | 4 | RESISTOR 511 OHM 1 \% $\% 125 \mathrm{H}$ F TUBULAR | 24546 | C4-1/8-T0-511R-F |
| A14R14 | 0757-0424 |  | RESISTOR 1.1K 1\%.125W F TURULAR | 24546 | C4-1/8-T0-1101-F |
| A14R15 | 0698-3430 | 1 | RESISTOR 21.5 OHM 18.125W F TUBULAR | 03888 | PME 55-1/8-T0-21R5-F |
| $\begin{aligned} & A 14 R 16 \\ & A 14 R 17 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0424 \\ & 0698-3450 \end{aligned}\right.$ | 1 | RESISTOR 1.1K 1\% . 125 W F TUBULAR RESISTOR 42.2 K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1101-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-4222-F \end{aligned}$ |
| A14R18 | 0757-0447 | 1 | RESISTOR 16.2K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-1622-F |
| A14R19 | 0757-0421 |  | RESISTOR 825 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR | 24546 | C $4-1 / 8-T 0-825 R-F$ |
| A14R20 | 0698-3447 | 1 | RESISTOR 422 OHM 1\% .125W F TUBULAR | 16299 | C4-1/8-T0-422R-F |
| $\begin{aligned} & \text { A } 14 R 21 \\ & \text { A } 14 R 22 \end{aligned}$ | $\left\lvert\, \begin{gathered} 0757-0279 \\ 0698-3155 \end{gathered}\right.$ | $\begin{aligned} & 3 \\ & 2 \end{aligned}$ | RESISTOR 3.16K 1\%.125W F TUBULAR RESISTOR 4.64K 1\% . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-\mathrm{T} 0-3161-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-4641-F \end{aligned}$ |
| A14R23 | 0757-0290 | 1 | RESISTIR $6.19 \mathrm{~K} 1 \%$ 1\% 125 W F TUBULAR | 19701 | C4-1/8-10-4641-F MF4C1/8-T0-6191-F |
| A14R24 | 0757-0279 |  | RESISTOR 3.16 K 18.125 W F TUBULAQ | 24546 | C4-1/8-T0-3161-F |
| A14R25 | 0757-0279 |  | RESISTOR 3.16K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-3161-F |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{\|l\|} \hline A 14 R 26 \\ A 14 R 27 \\ A 14 R 28 \\ A 14 R 29 \\ A 14 R 30 \end{array}$ | $0698-3150$ $0757-1094$ $0757-0394$ $0757-0304$ $0757-0416$ | $\begin{aligned} & 1 \\ & 1 \\ & 2 \end{aligned}$ |  | $\begin{aligned} & 16299 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-2371-F \\ & C 4-1 / 8=T 0-1471-F \\ & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-r 0-51 R 1-F \\ & C 4-1 / 8=T 0-511 R-F \end{aligned}$ |
| A14R31 <br> A14R32 <br> A14R33 <br> A14R34 <br> A14R35 | $\begin{aligned} & 0757-0416 \\ & 0757-0438 \\ & 0757-0200 \\ & 0757-0278 \\ & 0757-0442 \end{aligned}$ | 1 1 1 | RESISTOR 511 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOF $5.11 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 5.62 K 18 . 125 W F TUBULAR RESISTOR 1.78 K 1\% .125W F TUBULAR RESISTOR 10K $1 \%$. 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-511 R-F \\ & C 4-1 / 8-T 0-5111-F \\ & C 4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-1781-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |
| $\begin{aligned} & A 14 R 36 \\ & A 14 R 37 \\ & A 14 R 38 \\ & A 14 R 39 \\ & A 14 R 40 \end{aligned}$ | $\begin{aligned} & 0757-0444 \\ & 0757-0424 \\ & 0757-0444 \\ & 0698-0085 \\ & 0757-0416 \end{aligned}$ | 2 1 | RESISTOR 12.1K 1\% .125W F TUBULAR RESISTOR $1.1 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR RFSISTOR 12.1K 1\% .125W F TUBULAR RESISTOR $2.61 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TUBULAR RFSISTOR 511 OHM $1 \%$. 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 16299 \\ & 24546 \end{aligned}$ |  |
| A 14 R 41 | 0698-3155 |  | RESISTIT 4.64 K 18.125 W F TUBULAR | 16299 | C4-1/8-T0-4641-F |
| A14T1 | 08660-80001 | 1 | TRANSFORMER, SAMPLER | 28480 | 08660-80001 |
| $\begin{aligned} & A 14 U 1 \\ & \text { A } 1442 \\ & A 14 U 3 \\ & A 1444 \\ & A 14 U 5 \end{aligned}$ | $\begin{aligned} & 1820-0451 \\ & 1820-0451 \\ & 1820-0204 \\ & 1820-0450 \\ & 1820-0450 \end{aligned}$ | 2 1 3 | IC DGTL MC 3062P FLIP-FLOP IC DGTL MC 3062P FLIP-FLOP IC DGTL MC 3006P GATE IC DGTL N8290A COUNTER IC DGTL N82904 COUNTER | $\begin{aligned} & 04713 \\ & 04713 \\ & 04713 \\ & 18324 \\ & 18324 \end{aligned}$ | $\begin{aligned} & M C 3062^{P} \\ & M C 3062^{\circ} \\ & M C 3006{ }^{\circ} \\ & N 8290 A \\ & N 8290 A \end{aligned}$ |
| $\begin{aligned} & A 14 U 6 \\ & A 14 U 7 \end{aligned}$ | $\begin{aligned} & 1820-0450 \\ & 1820-0374 \end{aligned}$ | 1 | IC DGTL N8290A COUNTER IC DGTL SN74H 21 N GATE | $\begin{aligned} & 18324 \\ & 01295 \end{aligned}$ | $\begin{aligned} & \text { N8290A } \\ & \text { SN74H21N } \end{aligned}$ |

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{4} 15$ | 08660-60016 | 1 | BIARD ASSY, SLI DETECTOR | 23480 | 08660-60016 |
|  | 0160-2055 |  | CAPACITOR-FXD .OIUF +80-208 100WVDC CFR CAPACITIR-FXD IUF +80-20\% 50UVOC CER | 28480 28430 | $0160-2055$ |
| A15C3 | O150-0174 |  | CAPACITMR-FXD. $47 \mathrm{TUF}+80-20 \mathrm{z}$ 25WVDC CER | 28480 | 0150-0174 |
| A15C4 | 0150-0121 |  | CAPACITOR-FXD .1UF +80-208 50WVDC CER | 28480 | 0150-0121 |
| A15C5 | 0160-2055 |  | CAPACITOR-FXD .OLUF +80-20\% 100 WVDC CER | 28480 | 0160-2055 |
| ${ }^{\text {A } 15 C 6}$ | 0160-3456 |  | CAPACITOR-FXD 1000 PF +-10\% 100 OWVDC CER | $\begin{aligned} & 28480 \\ & 56289 \end{aligned}$ |  |
| A $15 C 7$ A $15 C 8$ | O180-0058 |  | CAPACITOR-FXD; 50UF+75-10\% 25VDC AL CAPACITOR-FXD; 100UF+-10\% 10VDC TA | $\begin{aligned} & 56289 \\ & 56289 \end{aligned}$ | $\begin{aligned} & 300506 G 025 C C 2 \\ & 1500107 \times 901 \text { OR2 } \end{aligned}$ |
| A 15 C 9 | 0180-0058 |  | CAPACITOR-FXD; 50UF+75-108 25VDC AL | 56289 | $3005065925 C C 2$ |
| A 15C10 | 0160-2261 |  | CAPACITAR-FXD 15PF +-5\% 500wVOC CER $0+$ | 28480 | 0160-2261 |
| A $15 \mathrm{Cl11}$ | 0160-2261 |  | CAPACITOR-FXD 15PF +-5\% 500WVDC CER 0+ CAPACITOR-FXD . O1UF +80-20\% 10OMVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ |  |
| A $15 C 12$ A 15 Cl 3 | O160-2055 0 0 $160-2204$ |  | CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER CAPACITOR-FXD 100PF t-5\% 300WVDC MICA | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\text { \| } \begin{aligned} & 0160-2055 \\ & 0150-2204 \end{aligned}$ |
| A15C14 | 0160-2055 |  | CAPACITOR-FXD .01UF +80-208 100 WVDC CER | 28480 | 0160-2055 |
| A15C15 | 0160-0298 | 2 | CAPACITOR-FXD 1500 PF +-108 200WVDC POLYE | 55289 | 292P15292 |
| $\left\lvert\, \begin{array}{lll} A 15 C 16 \\ A 15 C 17 \end{array}\right.$ | $\begin{array}{ll} 0 & 150-0121 \\ 0 & 160-0298 \end{array}$ |  | CAPACITOR-FXD .1UF +80-20\% 50WVDC CER CAPACITOR-FXD 1500 PF +-10\% 200WVDC PDLYE | $\begin{aligned} & 28480 \\ & 56289 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0150-0121 \\ & 292 P 15292 \end{aligned}\right.$ |
| A 15 Cl 18 | 0150-0121 |  | CAPACITOR-FXD .1UF +80-208 50WVDC CER | 28480 | 0150-0121 |
| A $15 \mathrm{Cl} \mathrm{C}^{\circ}$ | 0180-0291 |  | CAPACITOR-FXD: 1UF +108 35VOC TA-SOL ID | 55289 | $1500105 \times 903512$ |
| A15C20 | 0160-2055 |  | CAPACITOR-FXD. . DIUF +80-205 100WVDC CER | 28480 | 0160-2055 |
| $\left\lvert\, \begin{array}{ll} A 15 C 21 \\ A 15 C 22 \end{array}\right.$ | $\begin{array}{lll} 0 & 160-2208 \\ 0 & 160-0174 \end{array}$ |  | CAPACITOR-FXD 330PF +-5\% 300WVDC MICA CAPACITOR-FXD •47UF +80-20\% 25WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0160-2208 \\ & 0160-0174 \end{aligned}\right.$ |
| A15L1 | 9140-0179 |  | COIL: FXD; MOLDED RF CHOKE; 22UH 10\% | 24226 | 15/22? |
| A 1512 | 9140-0179 |  | COIL: FXD: MOLDED RF CHORE: 22UH $10 \%$ | 24226 | $15 / 222$ |
| A15L3 A 15 L A | 9140-0114 914 |  | COIL; FXD; MOLDED RF CHOKE; 10UH 108 COIL: FXD; MOLDED RF CHOKE; 22UH 108 | 24226 | 15/102 |
| $\begin{array}{\|l\|l\|} \text { A15L4 } \\ \text { A15L5 } \end{array}$ | 9140-0179 |  | COIL; FXD; MOLDED RF CHOKE; 22UH 108 NOT ASSIGNED | 24226 | 15/222 |
| A 1516 A 1517 | $9140-0179$ $9100-1659$ | 1 |  | 24226 28480 | $\left\lvert\, \begin{aligned} & 151222 \\ & 9100-1659 \end{aligned}\right.$ |
| A15L8 | 9140-0179 | 1 | COIL ; FXD: MOLDED RF CHOKE; $22 \mathrm{UH} 10 \%$ | 24226 | $151222$ |
| $\left\lvert\, \begin{array}{ll} A 1501 \\ \text { A } 1502 \end{array}\right.$ | $\begin{aligned} & 1854-0092 \\ & 1853-0015 \end{aligned}$ |  | TRANSISTOR NPN SI PD=200MH FT=600MHZ TRANSISTDQ PNP SI CHIP PD=200MM | 28480 28480 | $\left\lvert\, \begin{aligned} & 1854-0092 \\ & 1853-0015 \end{aligned}\right.$ |
| A 1503 | 1854-0092 |  | TRANSISTOP NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A1504 | 1854-0092 |  | TRANSI STOR NPN SI PD $=200 \mathrm{MH}$ FT $=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A1505 | 1854-0092 |  | TRANSISTOR. NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A 1506 | 1854-0092 |  | TRANSISTOR NPN SI PD=200MH FT $=600 \mathrm{MHZ}$ | 28480 | 1854-0092 |
| A15R1 A15R2 | 0698-3156 |  |  | $\begin{aligned} & 16299 \\ & 16299 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-1472-F \\ & C 4-1 / 8-T 0-4640-F \end{aligned}\right.$ |
| A15R3 | 0757-0379 | 1 | RESISTOR 12.1 OHM 1\% .125M F TUBULAR | 16299 19701 | MF4C1/8-T0-12R1-F |
| A15R4 |  |  | NOT ASSI GNED |  |  |
| A15R5 | 0757-0280 |  | RESISTOR 1K 12.125M F TUBULAR | 24546 | C4-1/8-T0-1 001-F |
| A15R6 A15R7 | $\text { \| } 0757-0280$ |  | RESISTOR 1 K 1\% . 125w F TUBULAR RESISTOR 825 OHM $1 \% .125 W$ F TUBULAR | $\begin{aligned} & 24546 \\ & 24548 \end{aligned}$ | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-1001-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-825 \mathrm{R}-\mathrm{F} \end{aligned}\right.$ |
| A15R8 | 0757-0421 |  | RESISTOR 825 OHM 1\% 18.125 W F TUBULAR | 24546 | C4-1/8-T0-825R-F |
| A15R9 | 0698-0082 |  | RESISTOR 464 OHM 1\% .125W F TUBULAR | 16290 | C4-1/8-T0-4640-F |
| A15R10 | 0698-0082 |  | RESISTOR 464 OHM 12.125W F TUBULAR | 16299 | C4-1/8-T0-4640-F |
| $\begin{aligned} & A 15 R 11 \\ & \text { A } 15 R 12 \end{aligned}$ | $\text { \| } 0757-0280$ |  | RESISTOR 1K 1\% •125H F TUBULAR RESISTOR 5.62K 18.125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-1001-F \\ & C 4-1 / 8-T 0-5621-F \end{aligned}\right.$ |
| A15R13 | 0698-3441 |  | RESISTOR $2150 H M 1 \%$.125W F TUBULAR | 16299 | C4-1/8-T0-215R-F |
| A15R14 | 2100-2633 |  | RESISTOR: VAR; TRMR; 1 KOHM 108 C | 19701 | ET50x102 |
| A15R15 | 0757-0200 |  | RESISTOR 5.62K 1\% .125W F TUBULAR | 24546 | C4-1/8-T0-5621-F |
| $\begin{aligned} & \text { A15R16 } \\ & \text { A } 15 R 17 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3150 \\ & 0757-0280 \end{aligned}\right.$ |  | RESISTOR 2.37K $1 \%$. 125W F TUBULAR RESISTOR 1K $1 \%$. 125 F F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-2371-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} 0-1001-\mathrm{F} \end{aligned}\right.$ |
| A15R18 | 0698-3155 |  | RESISTOR 4.64K 1\%.125W F TUBULAR | 16299 | C4-1/8-T0-4641-F |
| A15R19 | $0757-0280$ |  | RESISTOR 1K 18.125 W F TUBULAR | $24546$ | C.4-1/8-T0-1001-F |
| A15R20 | $0757-0424$ |  | RESISTOR 1.1K 1\% .125N F TUBULAR | $24546$ | C4-1/8-T0-1101-F |
| $\begin{aligned} & A 15 R 21 \\ & \text { A } 15 R 22 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0417 \\ & 0698-3151 \end{aligned}\right.$ |  | RESISTOR 562 OHM 1\%.125w F TUBULAR RESISTOR 2.87K $1 \% .125 \mathrm{~W}$ F TUBULAR | $\begin{array}{\|l} 24546 \\ 15299 \end{array}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-562 R-F \\ & C 4-1 / 8-T 0-2871-F \end{aligned}\right.$ |
| A15R23 | 0757-0280 |  | RESISTOR 1K 1\% .125w F TUBULAR | 24546 | C4-1/8-T0-1001-F |
| $\begin{aligned} & \text { A } 15 R 24 \\ & \text { A } 15 R 25 \end{aligned}$ | 0698-0084 |  | RESISTOR 2.15K 18.125 W F TUBULAR RESISTOR 100 OHM 1\%.125W F TUBULAR | $\begin{aligned} & 16209 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-2151-F \\ & C 4-1 / 8-T 0-101-F \end{aligned}\right.$ |
| $\begin{aligned} & A 15 R 26 \\ & \text { A } 15 R 27 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-7236 \\ & 0757-0416 \end{aligned}\right.$ |  | RESISTOR 1K 2\% .O5W F TUBULAR RESISTOR 511 OHM 17.125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \text { C } 3-1 / 8-T 0-1001-G \\ & C 4-1 / 8-T 0-511 R-F \end{aligned}$ |
| A15U1 <br> A15U2 <br> Al5U3 <br> A15U4 <br> A15U5 | $\begin{aligned} & 1820-0054 \\ & 1820-0077 \\ & 1820-0054 \\ & 1820-0054 \\ & 1820-0751 \end{aligned}$ |  | IC DGTL SN74 00 N GATE <br> IC DGTL SN74 74 N FLIP-FLOP <br> IC DGTL SN74 00 N GATE <br> IC OGTL SN74 00 N GATE <br> IC DGTL SN74196N COUNTER  | 01295 01295 01295 01295 01295 | SN7400N <br> SN7474V <br> SN7400N <br> SN7400N <br> SN74196N |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A 15136 A 1507 $A 1508$ $A 15 U 9$ $A 15110$ | $\begin{aligned} & 1820-0751 \\ & 1820-0068 \\ & 1820-0054 \\ & 1820-0054 \\ & 1820-0054 \end{aligned}$ |  | IC DGTL SN74196N COUNTER   <br> IC DGTL SN74 10 N GATE <br> IC DGTL SN74 DO N GATE  <br> IC DGTL SN74 00 N GATE <br> IC DGTL SN74 00 N GATE | 01295 01295 01295 01295 0 0 295 | SN74196N SN7410N SN7400N SN7400N SN7400N |
| A16 | 08660-60009 | 1 | BoARD ASSY, N1 PHASE DETECTOR | 28480 | 08660-60009 |
| A16C1 <br> A1AC2 <br> A16C3 <br> A16C4 <br> AleC5 | $\begin{aligned} & 0160-2055 \\ & 0180-0058 \\ & 0180-2206 \\ & 0180-0228 \\ & 0150-0121 \end{aligned}$ |  | CAPACITOR-FXD . $01 U \mathrm{~F}+80-20 \% 100 \mathrm{NVDC}$ CFR CAPACITOR-FXD: 50UF+75-10\% 25VOC AL CAPACITOR-FXD: 60UF+-10\% GVDC TA-SOLIO CAPACITOR-FXD: 22UF+-10\% 15VDC TA-SOLID CAPACITOR-FXO. 1 UF + 80-20\% 5OWVDC CER | $\begin{aligned} & 28480 \\ & 56289 \\ & 56289 \\ & 56289 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0180-2055 \\ & 300506 \mathrm{G} 025 \mathrm{CC2} \\ & 1500606 \times 9006 \mathrm{B2} \\ & 1500228 \times 9015 \mathrm{B2} \\ & 0150-0121 \end{aligned}$ |
| A 16 C6 <br> A16C7 <br> A16C8 <br> A16C9 <br> A16C10 | $\begin{array}{lll} 0 & 160-2055 \\ 0 & 150-0121 \\ 0 & 160-0297 \\ 0 & 160-2055 \\ 0 & 150-0121 \end{array}$ |  | CAPACITOR-FXD .OIUF +90-20\% 100WVDC CER CAPACITBR-FXD . IUF +80-20\% 5OWVDC CER CAPACITIR-FXD 1200PF +-10\% 200WVDC POLYE CAPACITTR-FXD .O1UF + 80-20\% 100WVCC CER CAPACITOR-FXD . 1 UF +80-20\% 5OWVOC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 56289 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0150-0121 \\ & 292 P 12292 \\ & 0160-2055 \\ & 0150-0121 \end{aligned}$ |
| A16Cl1 <br> A16C12 <br> A16Cl 3 <br> A16C14 <br> A16C15 | $\left(\begin{array}{lll} 0 & 150-01 & 21 \\ 0 & 160-2055 \\ 0 & 160-0937 \\ 0 & 160-3450 \\ 0 & 150-0121 \end{array}\right.$ | 1 | CAPACITOR-FXO - 1 UF +80-20\% 5OWVDC CER CAPACITOR-EXO .O1UF +80-20\% 100WVDC CER CAPACITOR-FXD 1000 PF $+-2 \% 300 \mathrm{HVDC}$ MICA CAPACITOR-EXD .O2UF +-20\% 100WVDC CER CAPACITJR-FXD . $1 U F+80-20 \%$ 5OWVDC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 29480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0150-0121 \\ & 0160-2055 \\ & 0160-0937 \\ & 0160-3459 \\ & 0150-0121 \end{aligned}\right.$ |
| A16C16 <br> A16C17 <br> A16C18 <br> A16C19 <br> A16C20 | $\left(\begin{array}{lll} 0 & 180-0197 \\ 0 & 160-2055 \\ 0 & 150-0121 \\ 0 & 180-0228 \\ 0 & 160-2055 \end{array}\right.$ |  | CAPACITDR-FXD; 2.2UF+-10\% 2OVDC TA CAPACITOR-FXD.01UF +80-20\% 100 WVDC CER CAPACITOR-FXD. 1UF + BO-20\% 50WVDC CER CAPACITOR-FXO; $22 \mathrm{UF}+-10 \%$ 15VDC TA-SOLID CAPACITOR-FXD .OLUF +80-20\% 100WVDC CER | $\begin{aligned} & 56289 \\ & 28480 \\ & 28430 \\ & 56289 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1500225 \times 702042 \\ & 0150-2055 \\ & 0150-0121 \\ & 1500226 \times 9015 B 2 \\ & 0160-2055 \end{aligned}$ |
| A16C21 <br> A 16 C22 <br> A16C23 <br> A16C24 <br> A16C25 | $\begin{array}{ll} 0 & 160-2055 \\ 0 & 160-3539 \\ 0 & 180-1746 \\ 0 & 180-0229 \\ 0 & 160-3459 \end{array}$ |  | CAPACITOR-FXD .O1UF +80-20\% 10OWVDC CER CAPACITOR-FXD 82OPF +-5\% 100WVDC MICA CAPACITOR-FXD: $15 U F+\mathbf{- 1 0 \%}$ 2OVDC TA-SOLID CAPACITMR-FXD; 33UF+-10\% 10VDC TA-SOLID CAPACITOR-FXD .O2UF $+-20 \%$ 100HVDC CER | $\begin{aligned} & 28480 \\ & 29480 \\ & 56289 \\ & 56289 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0160-3539 \\ & 1500156 \times 902082 \\ & 1500336 \times 901082 \\ & 0160-3459 \end{aligned}$ |
| A16C26 <br> A16C27 <br> A16C28 <br> A16C29 <br> A16C30 | $\begin{array}{lll} 0 & 180-0229 \\ 0 & 160-0134 \\ 0 & 160-0134 \\ 0 & 160-0302 \\ 0 & 160-0945 \end{array}$ | 2 | CAPACITOR-FXD: 33UF+-10\% 10VDC TA-SDLID CAPACITOR-FXD 220PF +-5\% 300WVDC. MICA CAPACITOR-FXD 220PF +-5\% 300WVDC MICA CAPARITOR-FXD .018UF +-10\% 200WVDC POLYE CAPACITOR-FXD $910 P F+-5 \%$ 100WVDC MICA | $\begin{aligned} & 56289 \\ & 28480 \\ & 28480 \\ & 56289 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1500336 \times 901 O B 2 \\ & 0160-0134 \\ & 0160-0134 \\ & 292 \mathrm{P} 18392 \\ & 0160-0945 \end{aligned}$ |
| A16C31 | 0140-0200 | 1 | CAPACITTR-FXO 390PF +-5\% 300WVDC MICA | 72136 | DM15F391J0300WVICR |
| A16CR1 <br> A 16CR 2 <br> A16CR 3 <br> A16CR4 <br> A16CR 5 | $\begin{array}{\|l} 1902-3104 \\ 1901-0040 \\ 1901-0040 \\ 1901-0179 \\ 1901-0179 \end{array}$ |  | DIODE-ZNR 5.62V 5\% DO-7 PD=.4W <br> DIODE-SWITCHING $2 N S$ 30V 50MA <br> DI ODE-SWITCHING 2NS 3OV 5OMA <br> DIODE-SWITCHING 750PS 15V 50MA <br> DI ODE-SWITCHING $750 P \mathrm{~S}$ 15V 50MA | $\begin{aligned} & 04713 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{array}{ll} S Z & 10939-110 \\ 1901-0040 \\ 1901-0040 \\ 1901-0179 \\ 1901-0179 \end{array}\right.$ |
| A 16CR6 | 1902-0025 | 1 | DIODE-ZNR LOV 5\% DO-7 PD $=.4 \mathrm{~K}$ TC= +.06\% | 04713 | SZ 10939-182 |
| A16L1 <br> A16L2 <br> A16L3 <br> A16L4 <br> A16L5 | $\begin{aligned} & 9100-1629 \\ & 9140-0114 \\ & 9100-1629 \\ & 9100-1614 \\ & 9100-2564 \end{aligned}$ | 2 | COIL; FXD: MOLDED RF CHOKE; 47UH 5\% <br> COIL; FXD; MOLDED RF CHOKE; 10UH 10\% <br> CDIL: FXD; MOLDED RF CHOKE; 47UH 5\% <br> COIL; FXD; MOLDED RF CHOKF; . 82 UH 10\% <br> CDIL: FXO: MOLDED RF CHJKE; 150UH 10\% | $\begin{aligned} & 24226 \\ & 24226 \\ & 24226 \\ & 24226 \\ & 06560 \end{aligned}$ | $\begin{aligned} & 15 / 472 \\ & 15 / 102 \\ & 15 / 472 \\ & 15 / 820 \\ & 15 S-151 K \end{aligned}$ |
| A16L6 | 9100-2564 |  | COIL : FXD; MOLDED RF CHOKE; 150UH $10 \%$ | 06560 | 15S-151K |
| A1601 <br> A 1602 <br> A 1603 <br> A 1604 <br> A1605 | $\begin{aligned} & 1853-0034 \\ & 1853-0034 \\ & 1855-0082 \\ & 1854-0092 \\ & 1853-0015 \end{aligned}$ | 1 | TPANSISTOR PNP SI CHIP TO-18 PD=360MH TRANSISTOF PNP SI CHIP TO-18 PD $=360 \mathrm{MW}$ TRANSI STDR: J-FET P-CHAN, D-MDDE SI TRANSISTIR NPN SI PD $=200 \mathrm{MW} \quad \mathrm{FT}=600 \mathrm{MHZ}$ TRANSISTDR PNP SI CHIP PD=200MW | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1853-0036 \\ & 1853-0034 \\ & 1855-0082 \\ & 1854-0092 \\ & 1853-0015 \end{aligned}$ |
| A1606 | 1854-0045 |  | TRANSISTOR NPN SI TD-18 PD $=500 \mathrm{MH}$ | 28480 | 1854-0045 |
| A16R1 <br> A16R2 <br> A16R3 <br> A16R4 <br> Al6R5 | $\begin{aligned} & 0698-3155 \\ & 0757-0421 \\ & 0898-3155 \\ & 0698-0082 \\ & 0757-1092 \end{aligned}$ | 1 | RESISTOR 4.64K 1\% . 125 W F TUBULAR RESISTIR 825 THM 1 IT . 125 W F TUBULAR RESISTITR 4.64K 1\% . 125 W F TUBULAR RESISTOR 464 OHM $1 \%$. 125 W F TUBIILAR RESISTOR 287 OHM $1 \% .5 \mathrm{~W}$ F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \\ & 18299 \\ & 16209 \\ & 19701 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-4641-F \\ & C 4-1 / 8-T 0-825 R-F \\ & C 4-1 / 8-T 0-4641-F \\ & C 4-1 / 8-T 0-4640-F \\ & \text { MF7C1/2-TO-287R-F } \end{aligned}$ |
| A16R6 <br> A16R7 <br> A16R8 <br> A16R9 <br> A16R10 | $\begin{aligned} & 0757-0289 \\ & 0757-0439 \\ & 0757-0418 \\ & 0757-0420 \\ & 0698-0085 \end{aligned}$ |  | RESI STOR 13.3K 1\% . 125 W F TUBULAR RESISTIR 6.R1K 1\% . 125W F TUBULAR RESI STHR 511 OHM 1\% . 125W F TUBULAR RESISTOR 750 OHM 1 \% . 125 W F TUBULAR RESISTOR 2.61K 1\% . 125 H F TUBULAR | $\begin{aligned} & 19701 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \text { MF } 4 C 1 / 8-T 0-1332-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-6811-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} 511 \mathrm{R}-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-751-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} 0-2611-F \end{aligned}$ |
| A 16R11 <br> A16R12 <br> A16R13 <br> A16R14 <br> A16R15 | $\begin{aligned} & 0757-0416 \\ & 0757-0442 \\ & 0698-3446 \\ & 0757-0424 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 511 DHM 1\% . 125 H F TUBULAR RESISTDR 10K 1\% . 125W F TUBULAR RESISTIR 383 OHM 1\% . 125 H F TUBULAR RESISTOR 1.1K 1\% . 125W F TUBULAR RESISTOR 10K 1\% . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 15299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-511 R-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-393 R-F \\ & C 4-1 / 8-T 0-1101-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A $16 R 16$ A16R17 A16R18 A16R19 A16R20 | $0757-0424$ $0757-0416$ $0698-3450$ $0757-0447$ $0698-3430$ |  |  | 24546 24546 16299 24546 03998 | $\begin{aligned} & C 4-1 / 8-T 0-1101-F \\ & C 4-1 / 8-T 0-511 R-F \\ & T 4-1 / 8-T 0-4222-F \\ & C, 4-1 / 8-T 0-1622-F \\ & \text { PME 55-1/9-T0-21R5-F } \end{aligned}$ |
| $\begin{aligned} & A 16 R 21 \\ & A 16 R 22 \\ & A 16 R 23 \\ & A 16 R 24 \\ & A 16 R 25 \end{aligned}$ | $\begin{aligned} & 0757-0424 \\ & 0757-0421 \\ & 0698-3447 \\ & 0757-0279 \\ & 0698-3153 \end{aligned}$ |  | RESISTOR 1.1K 1\% . 125W F TUBULAR RESISTOR 825 DHM $1 \% .125 W$ F TUBULAR RESISTOR 422 OHM 1 \% . 125W F TUBULAR RESISTITR 3.16K 1\% . 125 W F TUBULAR RESISTOR 3.83K $1 \% .125 \mathrm{~W}$ F TUBULAR | $\begin{aligned} & 24546 \\ & 24548 \\ & 16299 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1101-F \\ & C 4-1 / 9-T 0-825 R-F \\ & C 4-1 / 8-T 0-422 R-F \\ & C 4-1 / 8-T 0-3161-F \\ & C 4-1 / 8-T 0-3831-F \end{aligned}$ |
| $\begin{aligned} & A 16 R 26 \\ & A 16 R 27 \\ & A 16 R 28 \\ & A 16 R 29 \\ & A 16 R 30 \end{aligned}$ | $\begin{aligned} & 0757-0279 \\ & 0757-0279 \\ & 0698-0084 \\ & 0757-0200 \\ & 0757-0394 \end{aligned}$ |  | RFSISTOR 3.16K 1\% . 125 W F TUBULAR RESISTOR 3.16K 1\% .125W F TUBULAR RESISTOR 2.15K 18.125 W F TUBULAR RESISTOR 5.62K $1 \%$. 125 W F TUBULAR RESISTOR 51.1 OHM 1\% . 125 F FUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-3161-F \\ & C 4-1 / 8-T 0-3161-F \\ & C 4-1 / 8-T 0-2151-F \\ & C 4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-51 R 1-F \end{aligned}$ |
| $\begin{aligned} & A 16 R 31 \\ & A 16 R 32 \\ & A 16 R 33 \\ & A 16 R 34 \\ & A 16 R 35 \end{aligned}$ | $\begin{aligned} & 0757-0394 \\ & 0757-0280 \\ & 0698-3162 \\ & 0698-3450 \\ & 0757-0420 \end{aligned}$ |  | RESISTOR 51.1 OHM 1\%. 125H F TUBULAR RESISTOR 1K 1\% . 125 F F TUBULAR RESISTDR 46.4K 1\% . 125 W F TUBIGLAR RESISTOR 42.2K $1 \%$. 125 W F TUBULAR RESISTOR 750 OHM $1 \%$. 125 W F TUBILLAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16299 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8=T 0-1001-F \\ & \mathrm{C} 4-1 / 8-T 0-4642-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-4222-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-751-F \end{aligned}$ |
| $\begin{aligned} & \text { A16R36 } \\ & \text { A16R37 } \\ & \text { A16R38 } \\ & \text { A16R39 } \\ & \text { A16R40 } \end{aligned}$ | $\begin{aligned} & 0698-3156 \\ & 0757-0289 \\ & 2100-1760 \\ & 0757-0280 \\ & 0757-0274 \end{aligned}$ |  | RESISTOR 14.7K 1\% .125W F TUBIJLAR RESISTOR 13.3K 1\% . 125 W F TUBULAR RESISTOR: VAR; TRMR; 5KOHM 5\% WH RESISTOR 1K 1\% . 125 W F TUBULAR RESISTIR 1.21 K 1\% . 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 19701 \\ & \text { GB 027 } \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1472-F \\ & \text { MF4C1/8-TO-1332-F } \\ & \mathrm{CT} \text { T-106-4 } \\ & \mathrm{C} 4-1 / 8-T 0-1001-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1213-F \end{aligned}$ |
| $\begin{aligned} & A 16 R 41 \\ & \text { A } 16 R 42 \\ & \text { A } 16 R 43 \\ & \text { A } 16 R 44 \\ & \text { A16R45 } \end{aligned}$ | $\begin{aligned} & 0698-3156 \\ & 0757-1094 \\ & 0699-3158 \\ & 0757-0394 \\ & 0757-0420 \end{aligned}$ |  | RESISTOR 14.7K 1\% .125W F TUBULAR RESISTOR $1.47 \mathrm{~K} \quad 1 \%$.125W F TUBULAR RESISTOR 23.7K 18 .125W F TUBULAR RESISTOR 51.1 OHM 1\% .125W F TUBULAR RESISTOR 750 OHM 1\%. 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1472-F \\ & C 4-1 / 8-T 0-1471-F \\ & C 4-1 / 8-T 0-2372-F \\ & C 4-1 / 8-T 0-51 R 1-F \\ & C 4-1 / 8-T 0-751-F \end{aligned}$ |
| $\begin{aligned} & A 16 R 46 \\ & A 16 R 47 \end{aligned}$ | $\begin{aligned} & 0757-0440 \\ & 0757-0441 \end{aligned}$ |  | RESISTOR 7.5K 1\% . 125W F TUBULAR RESISTOR 8.25K $1 \%$. 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T 0-7501-F \\ & C 4-1 / 8-T 0-8251-F \end{aligned}\right.$ |
| A16T1 | 08660-80001 |  | TRANS ORMER, SAMPLER | 28480 | 08660-80001 |
| $\begin{aligned} & A 16 \text { TP } 1 \\ & \text { A } 16 \text { TP } 2 \\ & \text { A } 16 \text { TP } 3 \\ & \text { A } 16 \text { TP } 4 \\ & \text { A } 16 \text { TP } 5 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0360-0124 \\ & 0360-0124 \\ & 0360-0124 \\ & 0360-0124 \\ & 0 \\ & 0 \end{aligned} 360-0124\right.$ | 8 | $\begin{array}{llll} \text { TERMINAL } & \text { STUD } & .040^{\prime \prime} \\ \text { TERMINAL } & \text { STUD } & .040^{\prime \prime} \\ \text { TERMINAL } & \text { STUD } & .040^{\prime \prime} \\ \text { TERMINAL } & \text { STUD } & .040^{\prime \prime} \\ \text { TERMINAL } & \text { STUD } & .040^{\prime \prime} \end{array}$ | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28490 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0360-0124 \\ & 0360-0124 \\ & 0360-0124 \\ & 0360-0124 \\ & 0360-0124 \end{aligned}\right.$ |
| A 16 TP 6 A16TP7 A16TP 8 | $\left\lvert\, \begin{aligned} & 0360-0124 \\ & 0360-0124 \\ & 0360-0124 \end{aligned}\right.$ |  | $\begin{aligned} & \text { TERMINAL STUD .040" } \\ & \text { TERMINAL STUD .040" } \\ & \text { TERMINAL STUD .040" } \end{aligned}$ | $\begin{aligned} & 29480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0360-0124 \\ & 0360-0124 \\ & 0360-0124 \end{aligned}\right.$ |
| A16U1 <br> A16U2 <br> A16U3 <br> A16U4 <br> A16U5 | $\begin{aligned} & 1820-0058 \\ & 1820-0451 \\ & 1820-0451 \\ & 1820-0469 \\ & 1820-0751 \end{aligned}$ | 1 | ```IC LIN AMPLIEIER IC DGTL MC 3062P FLIP-FLOP IC DGTL MC 3062P FLIP-FLOP IC DGTL SN74H 102 N FLIP-FLOP IC DGTL SN74196N COUNTER``` | $\begin{aligned} & 07263 \\ & 04713 \\ & 04713 \\ & 01295 \\ & 01295 \end{aligned}$ | 709HC <br> MC $3062 P$ <br> MC 3062P <br> SN74H102N <br> SN74196N |
| A 16 U6 <br> A 16 U7 | $\left\lvert\, \begin{aligned} & 1820-0751 \\ & 1820-0204 \end{aligned}\right.$ |  | IC DGTL SN74196N COUNTER <br> IC DGTL MC 3006D GATE <br> MISCELLANEOUS A16. | $\begin{aligned} & 01295 \\ & 04713 \end{aligned}$ | $\begin{aligned} & \text { SN74196N } \\ & \text { MC3006P } \end{aligned}$ |
|  | $\left\lvert\, \begin{gathered} 08660-20155 \\ 08660-20155 \end{gathered}\right.$ | 2 | SHIELD, INDUCTOR <br> SHIELD, INDUCTOR | $\begin{array}{l\|} 28480 \\ 28480 \end{array}$ | $\begin{aligned} & 08660-20155 \\ & 08660-20155 \end{aligned}$ |
| 417 | 08660-60010 | 1 | BOARD ASSY, NI OSC ILLATOR | 28480 | 08660-60010 |
| A17C1 <br> A17C2 <br> A17C3 <br> A17C4 <br> A17C5 | $\begin{array}{lll} 0 & 180-0058 \\ 0 & 180-2215 \\ 0 & 180-0049 \\ 0 & 180-1704 \\ 0 & 150-0121 \end{array}$ | 1 | CAPACITOR-FXO: 50UF+75-10\% 25VDC AL CAPACITOR-FXD: $170 U F+75-10 \%$ 15VDC AL CAPACITOR-FXD; 20UF+75-10\% 50VDC AL CAPACITOR-FXD; 47UF+-102 6VDC TA-SOLID CAPACITOR-FXD . IUF +80-20\% 50WVOC CER | 56289 <br> 56289 <br> 56289 <br> 56239 <br> 29480 | $3005065025 C 2$ 300177G015DD2 305206 G 050 C 5 $1500476 \times 900632$ 0150-0121 |
| $\begin{aligned} & \text { A17C6 } \\ & \text { A17C7 } \\ & \text { A17C8 } \\ & \text { A17C } \\ & \text { A17C10 } \end{aligned}$ | $\begin{array}{lll} 0 & 150-0121 \\ 0 & 160-2055 \\ 0 & 180-0229 \\ 0 & 180-0228 \\ 0 & 180-0229 \end{array}$ |  | CAPACI TOR-FXD . 1 UF +80-20\% 50WVDC CER CAPACITOR-FXD .OIUF $+80-20 \%$ 100WVDC CER CAPACITOR-FXD; 33UF+-10\% 10VDC TA-SDLID CAPACITOR-FXD; 22UF+-10\% 15VDC TA-SOLID CAPACITOR-FXD; 33UF+-10\% 10VOC TA-SOLID | $\begin{array}{\|l} 28480 \\ 28480 \\ 56289 \\ 56289 \\ 56289 \end{array}$ | $\begin{aligned} & 0150-0121 \\ & 0160-2055 \\ & 1500336 \times 901082 \\ & 1500226 \times 901582 \\ & 1500336 \times 901082 \end{aligned}$ |
| $\begin{aligned} & A 17 C 11 \\ & \text { A } 17 C 12 \\ & \text { A } 17 C 13 \\ & \text { A } 17 C_{14} \\ & \text { A } 17 C 15 \end{aligned}$ | $\left\lvert\, \begin{array}{ccc} 0 & 180-0183 \\ 0 & 180-0374 \\ 0 & 160-2055 \\ 0 & 160-3047 \\ 0 & 160-0386 \end{array}\right.$ | 1 | CAPACITOR-FXD: $10 U F+75-10 \% 50 V D C$ AL CAPACITOR-FXD; 10UF+-10\% 20VDC TA-SOLID CAPACITOR-FXD .01UF +80-20\% 100WVDC CER CAPACITOR-FXD 3280 PF +-18 100WVDC MICA CAPACITOR-FXD 3.3PF +-. 25PF 500WVDC GER | $\begin{aligned} & 56289 \\ & 56289 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 3001066050 C B 2 \\ & 1500106 \times 9020 R 2 \\ & 0160-2055 \\ & 0160-3047 \\ & 0160-0385 \end{aligned}$ |
| $\begin{aligned} & A 17 C 16 \\ & A 17 C 17 \\ & A 17 C 18 \\ & A 17 C 19 \\ & A 17 C 20 \end{aligned}$ | $\begin{array}{lll} 0 & 170-0082 \\ 0 & 121-0059 \\ 0 & 160-2204 \\ 0 & 160-2055 \\ 0 & 160-0301 \end{array}$ |  | CAPACITOR-FXD .OULU +-20\% 50WVDC PDLYE CAPACITOR; VAR; TRMR: CER; 2/8PF CAPACITOR-FXD 100PF +-5\% 300WVDC MICA CAPACITOR-FXD . OLUF +80-20\% 100WVDC CER CAPACITOR $-F X D$. $012 U F+-10 \%$ 200WVDC POLYE | $\begin{aligned} & 84411 \\ & 73899 \\ & 28480 \\ & 28480 \\ & 56289 \end{aligned}$ | 601 PE 10 30R5W1 <br> DVIIPR8A <br> 0160-2204 <br> 0160-2055 <br> 292P1 2392 |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A $17 C 21$ $A 17 C 22$ $A 17 C 23$ $A 17 C 24$ $A 17 C 25$ | $\begin{aligned} & 0160-3092 \\ & 0 \\ & 0 \\ & 0 \end{aligned} 160-0386$ | 1 |  | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-3092 \\ & 0150-0386 \\ & 0160-0386 \\ & 0160-2055 \end{aligned}$ |
| $\begin{aligned} & A 17 C 26 \\ & \text { A17C27 } \\ & \text { A17C28 } \\ & \text { A17C29 } \\ & \text { A17C30 } \end{aligned}$ | $\begin{array}{lll} 0 & 160-2055 \\ 0 & 160-2055 \\ 0 & 160-2055 \\ 0 & 160-2055 \\ 0 & 160-2055 \end{array}$ |  | CAPACITOR-FXD .DIUF +80-20\% 100WVDC CER CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER CAPACITOR-FXD .OLUF +80-20\% 100WVOC CER CAPACITOR-FXO .OLUF +80-20\% 100WVDC CER CAPACITOR-FXD .OIUF +80-20\% 10OWVDC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0160-2055 \\ & 0160-2055 \\ & 0160-2055 \\ & 0160-2055 \end{aligned}$ |
| A17C31 <br> A17C32 <br> A17C33 <br> A17C34 <br> A17C35 | $\begin{array}{ll} 0 & 160-2055 \\ 0 & 150-0121 \\ 0 & 160-2055 \\ 0 & 160-2055 \\ 0 & 160-2055 \end{array}$ |  | CAPACITOR-FXN . DIUF +80-20\% 100WVDC CER CAPACITOP-FXD . $1 \mathrm{UF}+80-20 \%$ 5OWVOC CER CAPACITOR-FXD .O1UF +80-20\% 10OWVDC CER CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER CAPACITRR-FXD .OLUF +80-20\% 100WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0150-0121 \\ & 0160-2055 \\ & 0160-2055 \\ & 0160-2055 \end{aligned}$ |
| $\begin{aligned} & A 17 C 36 \\ & A 17 C 37 \\ & A 17 C 38 \\ & \text { A17C39 } \end{aligned}$ | $\begin{array}{lll} 0 & 160-2055 \\ 0 & 160-0162 \\ 0 & 140-0210 \\ 0 & 160-20 & 55 \end{array}$ | 1 | CAPACITOR-FXD .O1UF +80-20\% 100WVDC CER CAPACITOR-FXD . O22UF +-10\% 200WVDC POLYE CAPACITCR-FXD 27OPF +-5\% 300WVDC MICA CAPAC.ITOR-FXD .O1UF +80-20\% 100WVDC CER | $\begin{aligned} & 28480 \\ & 56289 \\ & 72136 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 292 P 22392 \\ & \text { DM15F } 271 \mathrm{~J} 0300 \text { WV1CR } \\ & 0160-2055 \end{aligned}$ |
| $\begin{aligned} & A 17 C R 1 \\ & A 17 C R 2 \\ & A 17 C R 3 \\ & A 17 C R 4 \\ & A 17 C R 5 \end{aligned}$ | $\begin{aligned} & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \end{aligned}$ |  | DIODE-SWITCHING 2NS 30V 5OMA DI ODE-SWITCHING 2NS 30V 50MA DIDDF-SWITCHING 2NS 30V 5OMA DI ODE-SWITCHING 2NS 30V 50MA DIODE-SWITCHING 2NS 30V 50MA | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \end{aligned}$ |
| A17CRG <br> A17CR 7 <br> A17CR 8 <br> A17CR 9 <br> A17CR 10 | $\begin{array}{\|cccc} 0 & 1 & 22-0264 \\ 0 & 1 & 22 & 2-0262 \\ 1 & 90 & 1-0040 \\ 1 & 90 & 1-0040 \\ 1 & 90 & 1-0040 \end{array}$ |  | ```DIO-VVC 1N5148A 47PF 5% C4/C50=3200000 DID-VVC IN5147A 39PF 5% C4/C60=3200000 DIODE-SWITC.HING 2NS 30V 5OMA DIODE-SWITCHING 2NS 30V 50MA DIDJE-SWITCHING 2NS 30V 5OMA``` | $\begin{aligned} & 04713 \\ & 04713 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1 N 5148 A \\ & 1 N 5147 A \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \end{aligned}$ |
| A17CR11 <br> A17CR12 <br> A17CR13 <br> A 17 CR 14 <br> A17CR15 | $\begin{aligned} & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \end{aligned}$ |  | DIODE-SWITCHING 2 2NS 30 V 50MA | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \\ & 1901-0040 \end{aligned}$ |
| $\begin{aligned} & \text { A } 17 \text { CR } 16 \\ & \text { A } 17 \text { CR } 17 \end{aligned}$ | 1901-0040 |  | DIODE-SWITCHING 2NS 30V 5OMA DI DDE-SWITCHING 2NS 30V 50MA | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | 1901-0040 |
| $\begin{array}{\|l} A 17 L 1 \\ A 17 L 2 \\ A 17 L 3 \\ A 17 L 4 \\ A 17 L 5 \end{array}$ | $\begin{aligned} & 9100-1629 \\ & 9100-2562 \\ & 9100-1629 \\ & 9100-1629 \\ & 9140-0179 \end{aligned}$ | 2 | COIL; FXD; MOLDED RF CHOKE; 47UH 5\% <br> COIL: FXD: MOLDED RF CHOKE: 100UH 10\% <br> COIL: FXD: MOLDED RF CHOKE; $47 \mathrm{UH} 5 \%$ <br> COIL: FXD: MOLDED RF CHOKE; 47UH 5\% <br> COIL: EXD; MOLDED RF CHOKE: 22UH 10\% | $\begin{aligned} & 24226 \\ & 06560 \\ & 24226 \\ & 24226 \\ & 24226 \end{aligned}$ | $\begin{aligned} & 15 / 472 \\ & 155-101 K \\ & 15 / 472 \\ & 15 / 472 \\ & 15 / 222 \end{aligned}$ |
| A17L6 <br> A17L7 <br> A17L8 <br> A17L9 | $\begin{aligned} & 9100-2815 \\ & 9100-1652 \\ & 9100-2566 \\ & 9100-2568 \end{aligned}$ | 1 | COIL: FXD; NON-MOLDED RF CHOKF: . 7 UH 58 <br> COIL: FXD: MOLDED RF CHOKE; 820UH 5\% <br> COIL: FXD: MOLDED RF CHOKE; 270UH 10\% <br> COIL: FXD; MOLDED RF CHOKE; 390UH 108 | $\begin{aligned} & 28480 \\ & 24226 \\ & 06560 \\ & 06560 \end{aligned}$ | $\begin{aligned} & 9100-2815 \\ & 19 / 823 \\ & 15 S-271 K \\ & 15 S-391 K \end{aligned}$ |
| $\begin{aligned} & \text { A } 1701 \\ & \text { A } 1702 \\ & \text { A } 1703 \\ & \text { A } 1704 \\ & \text { A } 1705 \end{aligned}$ | $\begin{aligned} & 1854-0092 \\ & 1853-0050 \\ & 1854-0345 \\ & 1853-0050 \\ & 1855-0081 \end{aligned}$ |  | TRANSISTOR NPN SI PD $=200 \mathrm{MH} F T=600 \mathrm{MHZ}$ TRANSISTOR PNP SI CHIP TO-18 PD=360MW TRANSISTOR NPN 2N5 179 SI $P D=200 \mathrm{MW}$ TRANSISTOR PNP SI CHIP TO-18 PD=360MW TRANSISTDR: J-FET N-CHAN, D-MNDE SI | $\begin{aligned} & 28480 \\ & 28480 \\ & 04713 \\ & 28480 \\ & 01295 \end{aligned}$ | $\begin{aligned} & 1854-0092 \\ & 1853-0050 \\ & 2 N 5179 \\ & 1853-0050 \\ & 2 N 5245 \end{aligned}$ |
| $\begin{aligned} & A 1706 \\ & A 1707 \\ & A 1708 \\ & A 1709 \\ & A 17010 \end{aligned}$ | $\begin{aligned} & 1854-0087 \\ & 1853-0050 \\ & 1854-0092 \\ & 1854-0087 \\ & 1854-0092 \end{aligned}$ |  | TRANSISTOR NPN SI $P \Pi=360 \mathrm{MW} \quad \mathrm{F} T=75 \mathrm{MHZ}$ <br> TRANSISTOR PNP SI CHIP TO-18 PD=360MM <br> TRANSISTOP NPN SI PD=200MH FT $=600 \mathrm{MHZ}$ <br> TRANSISTOR NPN SI PD $=360 \mathrm{MH} \quad \mathrm{FT}=75 \mathrm{MHZ}$ <br> TRAVSISTOR NPN SI $P D=200 \mathrm{MW} \quad \mathrm{F}^{\top}=600 \mathrm{MHZ}$ | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0087 \\ & 1853-0050 \\ & 1854-0092 \\ & 1854-0087 \\ & 1854-0092 \end{aligned}$ |
| A 17011 <br> A 17012 <br> A 17013 <br> A 17014 <br> A17015 | $\begin{aligned} & 1853-0007 \\ & 1853-0007 \\ & 1853-0007 \\ & 1853-0007 \\ & 1854-0092 \end{aligned}$ |  | TRANSISTOR PNP 2N3251 SI CHIP <br> TRANSISTDR PNP 2N3251 SI CHIP <br> TRANSISTOR PNP 2N3251 SI CHIP <br> TRANSISTOR PNP 2N3251 SI CHIP <br> TRANSISTOR NPN SI PD $=200 \mathrm{MW} \quad \mathrm{FT}=600 \mathrm{MHZ}$ | $\begin{aligned} & 04713 \\ & 04713 \\ & 04713 \\ & 04713 \\ & 28480 \end{aligned}$ | $\begin{aligned} & \text { 2N3251 } \\ & \text { 2N3251 } \\ & \text { 2N3251 } \\ & \text { 2N3251 } \\ & 1854-0092 \end{aligned}$ |
| $\begin{aligned} & A 17016 \\ & A 17017 \\ & A 17018 \\ & A 17019 \end{aligned}$ | $\begin{aligned} & 1853-0007 \\ & 1853-0007 \\ & 1853-0007 \\ & 1853-0007 \end{aligned}$ |  | TRANSISTOR PNP $2 N 3251$ SI CHID <br> TRANSISTOR PNP $2 N 3251$ SI CHIP <br> TRANSISTOR PNP 2N3251 SI CHIP <br> TRANSISTOP PNP 2N3251 SI CHIP | $\begin{aligned} & 04713 \\ & 04713 \\ & 04713 \\ & 04713 \end{aligned}$ | $\begin{array}{\|l} \text { 2N3 } 251 \\ \text { 2N3251 } \\ \text { 2N3251 } \\ \text { 2N3 } 251 \end{array}$ |
| $\begin{array}{\|l\|l} A 17 R 1 \\ A 17 R 2 \\ A 17 R 3 \\ A 17 R 4 \\ A 17 R 5 \end{array}$ | $\begin{aligned} & 0757-0428 \\ & 0757-0428 \\ & 0757-0428 \\ & 0757-0428 \\ & 0757-0428 \end{aligned}$ |  | RESISTOR 1.62 K 1\% .125W F TUBULAR RESISTOR 1.62K 1\% .125W F TUBULAR RESISTOR 1.62K 1\% .125W F TUBULAR RESISTOR 1.62K 1\% . 125 W F TUBULAR RESISTOR 1.62K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1621-F \\ & C 4-1 / 8-T 0-1621-F \\ & C 4-1 / 8-T 0-1621-F \\ & C 4-1 / 8-T 0-1621-F \\ & C 4-1 / 8-T 0-1621-F \end{aligned}$ |
| $\begin{aligned} & A 17 R 6 \\ & A 17 R 7 \\ & A 17 R B \\ & A 17 R 9 \\ & A 17 R 10 \end{aligned}$ | $\begin{aligned} & 0757-0428 \\ & 0757-0428 \\ & 0757-0428 \\ & 0757-0442 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 1.62K 18 . 125W F TUBULAP <br> RESISTDR 1.62K 1\% .125W F TUBULAR <br> RESISTOR 1.62K 18 .125W F TUBULAR <br> RESISTOR 10K 1\% . 125W F TUBULAR <br> RESISTOR 10K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1621-F \\ & C 4-1 / 8-T 0-1621-F \\ & C 4-1 / 8-T 0-1621-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{\|l} A \text { A 17R11 } \\ \text { A } 17 R 12 \\ \text { A } 17 R 13 \\ \text { A } 17 R 14 \\ A 17 R 15 \end{array}$ | $\begin{aligned} & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \end{aligned}$ |  | RFSISTOR $10 K$ $1 \%$ .125 W F TUBULAR <br> RESISTOR $10 K$ $1 \%$ .125 W F TUBULAR <br> RESISTOR 10 K $1 \%$ .125 W F TUBULAR <br> RESISTOR 10 K $1 \%$ .125 W F TUBULAR <br> RESISTOR 10 K $1 \%$ .125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-1002-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1002-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1002-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1002-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1002-F \end{aligned}$ |
| $\begin{aligned} & A 17 R 16 \\ & A 17 R 17 \\ & A 17 R 18 \\ & \text { A17R19 } \\ & \text { A17R20 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0757-0479 \\ & 0757-0472 \\ & 0757-0465 \\ & 0698-3228 \end{aligned}\right.$ |  | RESISTOP 10K 1\% . 125W F TUBULAR RESISTDR 392K 1\% . 125W F TUBULAR RESISTDR 200K 1\% . 125W F TUBULAR RESISTOR 100K 18 . 125W F TUBULAR RESISTOP 49.9K 15 . 125 F F TUBULAR | $\begin{aligned} & 24546 \\ & 19701 \\ & 24546 \\ & 24546 \\ & 07716 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & \text { MF4C1/R-T0-3923-F } \\ & C 4-1 / 8-T 0-2003-F \\ & \text { C4-1/8-T0-1003-F } \\ & \text { CEA1/8-T0-4991-F } \end{aligned}$ |
| $\begin{aligned} & \text { A } 17 R 21 \\ & \text { A } 17 R 22 \\ & \text { A17R23 } \\ & \text { A17R24 } \\ & \text { A17R25 } \end{aligned}$ | $\begin{aligned} & 0757-0124 \\ & 0757-0449 \\ & 0757-0442 \\ & 0698-4002 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 39.2K 1\% .125W F TUBULAR RESISTIR 20K 18.125W F TUBULAR RESISTOR 1OK 1\% . 125W F TUBULAR RESISTOR 5 K 1\% . 125 F F TUBULAR RESISTOR 1OK 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 15299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 5-1 / 4-T 0-3922-F \\ & C 4-1 / 8-T 0-2002-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-5001-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |
| $\begin{aligned} & \text { A17R26 } \\ & \text { A17R27 } \\ & \text { A17R28 } \\ & \text { A17R29 } \\ & \text { A17R30 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-3441 \\ & 0698-0085 \\ & 2100-1760 \\ & 0698-3156 \\ & 0757-0274 \end{aligned}\right.$ |  | RESISTOR 215 OHM $1 \%$. 125W F TUBULAR RESISTOR 2.61K 17 . 125W F TUBULAR RESISTOR: VAR; TRMR; 5KOHM 5\% WH RESISTOR 14.7K 1\% . 125 W F TUBULAR RESISTOR 1.21K 1\% .125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & G B 027 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-215 R-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-2611-F \\ & \mathrm{CT}-106-4 \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1472-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1213-F \end{aligned}$ |
| A17R31 <br> A17R32 <br> A17R33 <br> A17R34 <br> A17R35 | $\begin{aligned} & 2100-1759 \\ & 0757-0290 \\ & 0757-0200 \\ & 0757-0199 \\ & 0698-0085 \end{aligned}$ |  | RESISTOR; VAR; TRMR; 2KOHM 5\% WW RESISTOR 6.19K 1\% .125W F TUBULAR RESISTOR 5.62K $1 \%$. 125 W F TUBULAR RESISTOR 21.5K 1\% .125W F TUBULAR RESISTOR 2.61K 1\% .125W F TUBULAR | $\begin{aligned} & \text { GB } 027 \\ & 19701 \\ & 24546 \\ & 24546 \\ & 16209 \end{aligned}$ | $\begin{aligned} & C T-106-4 \\ & \text { MF4C1/8-T0-6191-F } \\ & C 4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-2152-F \\ & C 4-1 / 8-T 0-2611-F \end{aligned}$ |
| $\begin{aligned} & \text { A17R36 } \\ & \text { A17R37 } \\ & \text { A17R38 } \\ & \text { A17R39 } \\ & \text { A17R40 } \end{aligned}$ | $\begin{aligned} & 0757-0421 \\ & 0698-4037 \\ & 0698-3162 \\ & 0698-3155 \\ & 0757-0441 \end{aligned}$ |  | RESI STOR 825 DHM $18.125 W$ F TUBILLAR RESISTOR 46.4 OHM $18 \cdot 125 \mathrm{~W}$ F TUBULAR RESISTOR 46.4K 1\% .125W F TUBULAR RESISTOR 4.64K $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 8.25K $1 \%$.125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 16299 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-825 R-F \\ & C 4-1 / 8-T 0-46 R 4-F \\ & C 4-1 / 8-T 0-4642-F \\ & C 4-1 / 8-T 0-4641-F \\ & C .4-1 / 8-T 0-9251-F \end{aligned}$ |
| $\begin{aligned} & A 17 R 41 \\ & A 17 R 42 \\ & A 17 R 43 \\ & A 17 R 44 \\ & A 17 R 45 \end{aligned}$ | $\begin{aligned} & 0757-0279 \\ & 0757-0834 \\ & 0757-0317 \\ & 0757-0199 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 3.16K $1 \%$.125W F TUBULAR RESISTOR 5.62K 1\% .5W F TUBULAR RESISTOR 1.33K 1\% .125W F TUBULAR RESISTOR 21.5K 1\% .125W F TUBULAR RESISTOR 10K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 19701 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-3161-F \\ & \text { MF7C1/2-TO-5621-F } \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-1331-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} 2152-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-1002-\mathrm{F} \end{aligned}$ |
| $\begin{aligned} & A 17 R 46 \\ & A 17 R 47 \\ & A 17 R 48 \\ & A 17 R 49 \\ & A 17 R 50 \end{aligned}$ | $\begin{aligned} & 0698-3441 \\ & 0698-3459 \\ & 0698-0082 \\ & 0757-0835 \\ & 0698-3266 \end{aligned}$ | 1 | RESISTOR 215 DHM $1 \% .125 W$ F TUBULAR RESISTOR 383K 18 - 125W F TUBULAR RFSISTOR 464 OHM $1 \%$. 125 F F TUBULAR RESISTOR 6.81K 1\% .5W F TUBULAR RESISTOR 237K 1\% •125W F TUBULAR | $\begin{aligned} & 16299 \\ & 19701 \\ & 16299 \\ & 19701 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-215 R-F \\ & \text { MF4C1/9-TO-3833-F } \\ & \text { C4-1/8-TO-4640-F } \\ & \text { MF7C1/2-T0-6811-F } \\ & C 4-1 / 8-T 0-2373-F \end{aligned}$ |
| A17R51 <br> A 17 R5 2 <br> A17R53 <br> A17R54 <br> A17R55 | $\begin{aligned} & 0698-3440 \\ & 0698-3447 \\ & 0698-3266 \\ & 0698-3445 \\ & 0698-3243 \end{aligned}$ |  | RESISTOR 196 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 422 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 237K 1\% . 125W F TUBULAR RESISTOR 348 OHM 1\% . 125 W F TUBULAR RESISTOR 178K 18 . 125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / B-T 0-196 R-F \\ & C 4-1 / R-T 0-422 R-F \\ & C 4-1 / 8-T 0-2373-F \\ & C 4-1 / 8-T 0-348 R-F \\ & C 4-1 / 8-T 0-1783-F \end{aligned}$ |
| A17R56 <br> A17R57 <br> A17R58 <br> A17R59 <br> A17R60 | $\begin{aligned} & 0698-3443 \\ & 0698-3243 \\ & 0698-3132 \\ & 0757-0466 \\ & 0683-8245 \end{aligned}$ |  | RESISTOR 287 OHM 1\%. 125W F TUBULAR RESISTOR 178K 1\% - 125W F TUBULAR RESISTOR 261 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 110K 1\% . 125W F TUBULAR RESISTOR 820K 5\% . 25W CC TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 16209 \\ & 24546 \\ & 01121 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-287 R-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-1783-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-2610-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-1103-\mathrm{F} \\ & \mathrm{CB} 8245 \end{aligned}$ |
| A17R61 <br> A 17 R62 <br> A17R63 <br> A17R64 <br> A17R65 | $\begin{aligned} & 0698-3243 \\ & 0698-3440 \\ & 0698-3440 \\ & 0698-0082 \\ & 0757-0467 \end{aligned}$ |  | RESISTOR 178K 1\% . 125W F TUBULAR RESISTOR 196 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTDR 196 OHM $1 \% .125 W$ F TUBULAR RESISTOR 464 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 121K 1\% - 125W F TUBULAR | $\begin{aligned} & 16290 \\ & 16209 \\ & 16299 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T O-1783-F \\ & C 4-1 / 8-T O-196 R-F \\ & C 4-1 / 8-T 0-196 R-F \\ & C 4-1 / 8-T 0-4640-F \\ & C 4-1 / 8-T 0-1213-F \end{aligned}$ |
| A17R66 <br> A17R67 <br> A17R68 <br> A17R69 <br> A17R70 | $\begin{aligned} & 0698-3439 \\ & 0757-0200 \\ & 0698-3154 \\ & 0757-0464 \\ & 0698-3445 \end{aligned}$ |  | RESI STOR 178 OHM $1 \%$. 125W F TUBULAR RESISTOR 5.62K $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 4.22K $1 \%$.125W F TUBULAR RESISTOR 90.9K $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 348 OHM 18.125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-178 R-F \\ & \mathrm{C} 4-1 / 8-T 0-5621-F \\ & \mathrm{C} 4-1 / 8-T 0-4221-F \\ & \mathrm{C} 4-1 / 8-T 0-9092-F \\ & \mathrm{C} 4-1 / 8-T 0-348 R-F \end{aligned}$ |
| $\begin{aligned} & A 17 R 71 \\ & A 17 R 72 \\ & A 17 R 73 \\ & A 17 R 74 \\ & A 17 R 75 \end{aligned}$ | $\begin{aligned} & 0757-0405 \\ & 0757-0461 \\ & 0757-0403 \\ & 0698-3444 \\ & 0698-3437 \end{aligned}$ |  | RESI STOP 162 OHM $1 \%$. 125W F TUBULAR RESISTOR 68.1K 1\% . 125W F TU8ULAR RESISTOR 121 OHM $1 \% .125 W$ F TUBULAR RESISTOR 316 OHM 1 . 125 W F TUBULAR RESISTOR 133 OHM $1 \%$. 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T O-162 R-F \\ & C 4-1 / 8-T 0-6812-F \\ & C 4-1 / 8-T 0-121 R-F \\ & C 4-1 / 8-T O-316 R-F \\ & C 4-1 / 8-T 0-133 R-F \end{aligned}$ |
| $\begin{aligned} & A 17 R 76 \\ & \text { A17R77 } \\ & \text { A17R78 } \\ & \text { A17R79 } \\ & \text { A17R80 } \end{aligned}$ | $\begin{aligned} & 0757-0458 \\ & 0698-3442 \\ & 0757-0401 \\ & 0757-0200 \\ & 0757-0280 \end{aligned}$ |  | RESI STOR 51.1K 18 . 125 W F TUBULAR RESISTOR 237 OHM 1\%.125W F TUBULAR RESISTOR 100 OHM $1 \%$-125W F TUBULAR RESISTOR 5.62K 1\%. .125W F TUBULAR RESISTOR 1K 1\% . 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 18290 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-5112-F \\ & C 4-1 / 8-T 0-237 R-F \\ & C 4-1 / 8-T 0-101-F \\ & C 4-1 / B-T 0-5621-F \\ & C 4-1 / 8-T 0-1001-F \end{aligned}$ |
| A 17 R8 1 <br> A17R82 <br> A17R83 <br> A17R84 <br> A17R85 | $\begin{aligned} & 0698-3154 \\ & 0757-0401 \\ & 0698-3132 \\ & 0698-3444 \\ & 0698-3444 \end{aligned}$ |  | RESI STOR 4.22K 18.125 W F TUBULAR RESISTOR 100 OHM 17.125 W F TUBULAR RESISTOR 261 OHM $1 \%$. 125W F TUBULAR RESISTOR 316 OHM 1\% .125W F TUBULAR RESISTOR 316 OHM 18.125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-4221-F \\ & C 4-1 / 8-T 0-101-F \\ & C 4-1 / 8-T 0-2610-F \\ & C 4-1 / 8-T 0-316 R-F \\ & C 4-1 / 8-T 0-316 R-F \end{aligned}$ |

Table 6-3. Replaceable Parts


Table 6-3. Replaceable Parts

| Reference Designation | HP Part <br> Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A18R1 A18R2 A18R3 A18R4 A18R5 | $0698-0083$ $0698-0083$ $0698-0083$ $0698-0083$ $0698-0083$ |  | RESISTOR $1.96 K$ $1 \%$ $.125 W$ $F$ TUBULAR <br> RESISTOR $1.96 K$ $1 \%$ $.125 W$ $F$ TUBULAR <br> RESISTOR $1.96 K$ $1 \%$ $.125 W$ $F$ TURULAR <br> RESISTOR $1.98 K$ $1 \%$ $.125 W$ $F$ TUBULAR <br> RESISTOR $1.96 K$ $1 \%$ $.125 W$ $F$ TURULAR | $\begin{aligned} & 15209 \\ & 15299 \\ & 15299 \\ & 16299 \\ & 15299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T Y-1961-F \\ & C .4-1 / 8-T 3-1961-F \\ & C 4-1 / 8-T ?-1961-F \\ & C 4-1 / 8-T 0-1961-F \\ & C 4-1 / 8-T ?-1961-F \end{aligned}$ |
| $\begin{aligned} & \text { A18R6 } \\ & \text { A18R7 } \\ & \text { A1BRB } \\ & \text { A18RO } \\ & \text { A18R10 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0698-0083 \\ & 0698-0083 \\ & 0698-0083 \\ & 0757-0442 \\ & 0757-0442 \end{aligned}\right.$ |  | RESISTOR 1.96 K 1\% .125W F TUBULAR RESISTOR 1.96 K 1\% . 125 W F TUBULAR RESISTOR 1.96K 1\% .125W F TUBULAR RESISTOR 10K 1\% . 125 W F TUBILAR RESISTOR 1OK 1\% . 125 W F TUBULAR | $\begin{aligned} & 16290 \\ & 15299 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T)-1061-F \\ & C 4-1 / 8-T 0-1961-F \\ & C 4-1 / 8-T)-1961-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |
| $\begin{aligned} & \text { A 18R11 } \\ & \text { A 18R12 } \\ & \text { A 18R13 } \\ & \text { A 18R14 } \\ & \text { A 18R15 } \end{aligned}$ | $\begin{aligned} & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 1OK 18.125 W F TUBULAR <br> RESISTOR 10K 1\% . 125 W F TUBULAR <br> RESISTOR IOK 1\% . 125 W F TUBULAR <br> RESISTOR 1OK 1\% . 125 W F TUBULAR <br> RESISTOR 10K $1 \%$. 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |
| A18R16 <br> A18R17 <br> A18R18 <br> Al8R19 <br> A18R20 | $\begin{aligned} & 0757-0442 \\ & 0757-0479 \\ & 0757-0472 \\ & 0757-0465 \\ & 0798-3228 \end{aligned}$ |  | RESISTOR 10K 1\% . 125 F F TUBULAR RESISTOR 392K 1\% •125W F TUBULAR RESISTOR 200K 1\% - 125W F TUBULAR RESISTOR 100 K 1\% . 125W F TUBULAR RESISTOR 49.9K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 19701 \\ & 24546 \\ & 24546 \\ & 07716 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-TO-1 002-F } \\ & \text { MF4C1/8-T0-3923-F } \\ & \text { C4-1/8-TO-2003-F } \\ & \text { C4-1/8-T0-1003-F } \\ & \text { CEA1/B-TO-4991-F } \end{aligned}$ |
| A18R21 <br> A18R22 <br> A18R23 <br> A18R24 <br> A18R25 | $\begin{aligned} & 0683-3955 \\ & 0683-2055 \\ & 0683-1055 \\ & 0698-3263 \\ & 0698-0083 \end{aligned}$ |  | RESISTOR 3.9M 5\% . 25W CC TUBULAR RESISTOR 2M 5\% . 25W CC TUBULAR RESISTOR 1M 5\%.25W CC TUBULAR RESI STOR 500K 1\% . 125W F TUBULAR RESISTOR 1.96K $1 \%$. 125 W F TUBULAR | $\left\lvert\, \begin{array}{llll} 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 \\ 01 & 1 & 1 \\ 1 & 9 & 7 & 1 \\ 16 & 29 \end{array}\right.$ | $\begin{aligned} & \text { CB3955 } \\ & \text { CB2055 } \\ & \text { CB1055 } \\ & \text { MF } 5 C 1 / 8-\text { TO- } 5003-F \\ & \text { C4-1/8-TB-1 961-F } \end{aligned}$ |
| A18R26 <br> A18R27 <br> A18R28 <br> A18R29 <br> A18R30 | $\begin{aligned} & 0757-0442 \\ & 0757-0200 \\ & 0698-3154 \\ & 0698-3440 \\ & 0698-3154 \end{aligned}$ |  | RESISTOR 10K 1\% . 125 W F TUBULAR RESISTOR 5.62 K 1\% .125W F TUBULAR RESISTOR 4.22K 1\% .125W F TUBULAR RESISTOR 196 OHM $1 \% .125 W$ F TUBULAR RESISTOR 4.22K 15 -125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 16299 \\ & 16299 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-4221-F \\ & C 4-1 / 8-T 0-196 R-F \\ & C 4-1 / 8-T 0-4221-F \end{aligned}$ |
| A18R31 <br> A18R32 <br> A18R33 <br> A18R34 <br> A18R35 | $\begin{aligned} & 0698-3444 \\ & 0698-3444 \\ & 0698-0083 \\ & 0757-0442 \\ & 2100-2574 \end{aligned}$ |  | RESISTOR 316 OHM 1\% . 125N F TUBULAR RESISTOR 316 OHM 1\% .125W F TUBULAR RESISTOR 1.96 K 1\% .125W F TUBULAR RESISTOR 1OK 1\% .125H F TUBULAR RESISTOR: VAR; TRMR; 500 OHM 10\% C | $\begin{aligned} & 16299 \\ & 16209 \\ & 16299 \\ & 24546 \\ & 19701 \end{aligned}$ |  |
| A18R36 <br> A18R37 <br> Al8R38 <br> A18R39 <br> A18R40 | $\begin{aligned} & 0698-3155 \\ & 0698-0082 \\ & 0698-0083 \\ & 0757-0442 \\ & 2100-2574 \end{aligned}$ |  | RESISTOR 4.64K 1\% .125W F TUBULAR RESISTOR 464 OHM 1:.125W F TUBULAR RESISTOR 1.96K $1 \%$ •125W F TUBULAR RESISTOR 1OK 1\% . 125 W F TUBULAR RESISTOR: VAR; TRMR; 500 DHM 10\% C | $\begin{aligned} & 16299 \\ & 16299 \\ & 16299 \\ & 24546 \\ & 19701 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-4641-F \\ & C 4-1 / 8-T 0-4640-F \\ & C 4-1 / 8-T 3-1961-F \\ & \text { C4-1/8-T0-1002-F } \\ & \text { ET50×501 } \end{aligned}$ |
| A18R41 <br> A18R42 <br> A18R43 <br> A18R44 <br> A18R45 | $\begin{aligned} & 0698-3258 \\ & 0698-0083 \\ & 0757-0442 \\ & 2100-2633 \\ & 0757-0290 \end{aligned}$ |  | RESISTOR 5.36K 1\% . 125 W F TUBULAR RESISTOR 1.96K 18.125 W F TUBULAR RESISTOR 10K 1\% .125N F TUBULAR RESISTOR: VAR; TRMR: 1KOHM 10\% C RESISTOR 6.19K 1\% .125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 24546 \\ & 19701 \\ & 19701 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-T0-5361-F } \\ & \text { C4-1/8-TJ-1 } 961-F \\ & \text { C4-1/8-T0-1002-F } \\ & \text { ET50X102 } \\ & \text { MF4C1/8-T 0-6191-F } \end{aligned}$ |
| A18R46 <br> A18R47 <br> A1BR48 <br> A18R49 <br> A18R50 | $\begin{aligned} & 0757-0399 \\ & 0757-0400 \\ & 0757-0399 \\ & 0698-0083 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 82.5 OHM 1\% .125W F TUBULAR RESISTOR 90.9 OHM 1\%. 125W F TUBULAR RESISTOR 82.5 OHM 18.125W F TUBULAR RESISTOR $1.96 \mathrm{~K} 1 \%$. 125 W F TUBULAR RESISTOR 10K 1\% . 125 H F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 16209 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-92 R 5-F \\ & C 4-1 / 8-T 0-90 R 9-F \\ & C_{4}-1 / 8-T 0-82 R 5-F \\ & C 4-1 / 8-T 3-1961-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |
| A18R51 <br> A 18R52 <br> A18R53 <br> A18R54 <br> A18R55 | $\begin{aligned} & 2100-2633 \\ & 0757-0440 \\ & 0698-0083 \\ & 0757-0442 \\ & 2100-2521 \end{aligned}$ |  | RESISTOR ; VAR: TRMR: 1KOHM 10\% C RESISTOR 7.5K 1\% . 125 H F TUBULAR RESISTOR 1.96 K 1\% .125W F TUBULAR RESISTOR 1OK 1\% . 125 W F TUBULAR RESISTOR: VAR; TRMR; 2KOHM $10 \% \mathrm{C}$ | $\begin{aligned} & 19701 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 19701 \end{aligned}$ | $\begin{aligned} & \text { ET50×102 } \\ & C 4-1 / 8-T 0-7501-F \\ & C 4-1 / 8-T J-1961-E \\ & C 4-1 / 8-T 0-1002-F \\ & \text { ET50×202 } \end{aligned}$ |
| A18R56 <br> A18R57 <br> A18R58 <br> A18R59 <br> A18R60 | $\begin{aligned} & 0757-0288 \\ & 0757-0394 \\ & 0698-3151 \\ & 0698-3151 \\ & 0698-0083 \end{aligned}$ |  | RESISTOR 9.09K $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 51.1 OHM 15.125W F TUBULAR RESISTOR 2.87K 1\% .125W F TUBULAR RESISTOR 2.87K 1\% .125W F TUBULAR RESISTOR 1.96K 1\% . 125 W F TUBULAR | $\begin{aligned} & 19701 \\ & 24546 \\ & 16209 \\ & 16299 \\ & 16290 \end{aligned}$ | $\begin{aligned} & \text { MF4C1/8-T0-9091-F } \\ & \text { C4-1/8-T0-51R1-F } \\ & \text { C4-1/8-TO-2871-F } \\ & C 4-1 / 8-T 0-2871-F \\ & C 4-1 / 8-T J-1961-F \end{aligned}$ |
| A18R61 <br> A18R62 <br> A18R63 <br> A18R64 <br> A18R65 | $\begin{aligned} & 0757-0442 \\ & 2100-2521 \\ & 0757-0444 \\ & 0698-3445 \\ & 0757-0416 \end{aligned}$ |  | RESISTOR 10K 1\% . 125 W F TUBULAR RESISTOR; VAR; TRMR: 2KOHM 10\% C RESISTOR 12.1K 1\% . 125W F TUBULAR RESISTOR 348 OHM 1\% . 125W F TUBULAR RESIS'OR 511 OHM 18.135 W F TUBULAR | $\begin{aligned} & 24546 \\ & 19701 \\ & 24546 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \text { C4-1/8-T0-1 002-F } \\ & \text { ET50×202 } \\ & \text { C4-1/8-T0-1212-F } \\ & \text { C4-1/8-T0-348R-F } \\ & \text { C4-1/8-T0-511R-F } \end{aligned}$ |
| A18R66 <br> A18R67 <br> A18R68 <br> A18R69 <br> A18R70 | $\begin{aligned} & 0698-0083 \\ & 0757-0442 \\ & 2100-2489 \\ & 0698-3136 \\ & 0757-0441 \end{aligned}$ |  | RESISTOR 1.96K $1 \%$-I25W F TUBULAR RESISTOR 10K 1\% . 125 F F TUBULAR RESISTOR: VAR; TRMR: 5KOHM 10\% C RESISTOR 17.8K 18 .125W F TUBULAR RESISTOR 8.25K 1\% .125W F TUBULAR | $\begin{aligned} & 16209 \\ & 24546 \\ & 19701 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T D-1961-F \\ & C 4-1 / 8-T 0-1002-F \\ & \text { CT50 } 502 \\ & C 4-1 / 8-T 0-1782-F \\ & C 4-1 / 8-T 0-8251-F \end{aligned}$ |
| A18R71 <br> A18R72 <br> A18R73 <br> A18R74 <br> A18R75 | $\begin{aligned} & 0757-0279 \\ & 0698-0083 \\ & 0757-0442 \\ & 2100-2522 \\ & 0757-0123 \end{aligned}$ |  | RESISTOR 3.16K 1\% .125W F TUBULAR RESISTOR 1.96K 1\% . 125W F TUBULAR RESISTOR 1OK 1\% . 125W F TUBULAR RESISTOR; VAR; TRMR; 1OKOHM 10\% C RESISTOR 34.8K 1\% .125W F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 24546 \\ & 19701 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-3161-E \\ & C 4-1 / 8-T J-1961-F \\ & C 4-1 / 8-T 0-1002-F \\ & E T 50 \times 103 \\ & C 5-1 / 4-T 0-3482-F \end{aligned}$ |

Table 6-3. Replaceable Parts


Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{\|l\|} \hline A 19 L 1 \\ A 19 L 2 \\ A 19 L 3 \\ A 19 L 4 \\ A 19 L 5 \end{array}$ | $9100-1629$ $9100-2562$ $9100-1629$ $9100-1629$ $9100-2572$ | 1 | COIL; EXD; MOLDED RF CHOKF; 47UH 5\% COIL; FXD; MOLDED RF CHOKE; 100JH 10\% COIL; FXD; MOLDED RF CHOKE; 47UH 5\% COIL; FXD; MOLDED RF CHOKE; 47UH 5\% COIL; FXD; MOLDED RF CHOKE; 820UH 10\% | $\begin{aligned} & 24226 \\ & 06560 \\ & 24226 \\ & 24226 \\ & 06560 \end{aligned}$ | $\begin{aligned} & 15 / 472 \\ & 15 S-101 K \\ & 15 / 472 \\ & 15 / 472 \\ & 15 S-821 K \end{aligned}$ |
| A1916 <br> A1917 <br> A19L8 <br> A19L9 <br> A19L10 | $\begin{aligned} & 9100-2815 \\ & 9140-0179 \\ & 9140-0179 \\ & 9100-1611 \\ & 9100-1611 \end{aligned}$ | 2 | COIL: FXD; NON-MOLDED RF CHOKE; . TUH 5\% COIL; FXD; MDLDED RF CHOKE; 22UH 108 COIL: FXD; MDLDED RF CHOKE; 22UH 10\% COIL; FXD; MCLDED RE CHOKE; .22UH 20\% COIL; FXD; MOLDED RF CHOKE; .22UH 20\% $\text { COIL; FXD; MCLDED RF CHOKE; . } 22 U H 20 \$$ $\text { COIL; FXD; MOLDED RF CHOKE; . } 22 \mathrm{UH} 208$ | $\begin{aligned} & 28480 \\ & 24226 \\ & 24226 \\ & 24226 \\ & 24226 \end{aligned}$ | $\begin{aligned} & 9100-2815 \\ & 15 / 222 \\ & 15 / 222 \\ & 15 / 220 \\ & 15 / 220 \end{aligned}$ |
| $\begin{aligned} & A 1901 \\ & A 1902 \\ & A 1903 \\ & A 1904 \\ & A 1905 \end{aligned}$ | $\begin{aligned} & 1854-0092 \\ & 1854-0092 \\ & 1854-0092 \\ & 1855-0081 \\ & 1854-0345 \end{aligned}$ |  | TRANSISTOR NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ TRANSISTOR NPN SI PD $=200 \mathrm{MH} \quad \mathrm{FT}=600 \mathrm{MHZ}$ TRANSISTOR NPN SI PD $=200 \mathrm{MH} \quad \mathrm{F}^{\top}=600 \mathrm{MHZ}$ TRANSISTOR: J-FET N-CHAN, D-MODE SI TRANSISTOR NPN $2 N 5179$ SI PD $=200 \mathrm{MW}$ | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 01295 \\ & 04713 \end{aligned}$ | $\begin{aligned} & 1854-0092 \\ & 1854-0092 \\ & 1854-0092 \\ & 2 N 5245 \\ & 2 N 5179 \end{aligned}$ |
| 41906 <br> A1907 <br> A 1908 <br> A1909 <br> A 19010 | $\begin{aligned} & 1853-0050 \\ & 1853-0050 \\ & 1854-0092 \\ & 1854-0092 \\ & 1854-0022 \end{aligned}$ | 1 | TRAVSISTOR PNP SI CHIP TD-18 PD=360MW TRANSISTOR PNP SI CHIP TO-18 PD=360MW TRANSISTOR NPN SI PD=200MM $F T=600 \mathrm{MHZ}$ TRANSI STOR NPN SI PO=200MM FT $=600 \mathrm{MHZ}$ TRANSISTOR NPN SI TT-39 PD=700MW | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 07263 \end{aligned}$ | $\begin{aligned} & 1853-0050 \\ & 1853-0050 \\ & 1854-0092 \\ & 1854-0092 \\ & 517843 \end{aligned}$ |
| A19R1 <br> A19R2 <br> A19R3 <br> A19R4 <br> A19R5 | $\begin{aligned} & 0698-3132 \\ & 0698-3442 \\ & 2100-1760 \\ & 0757-0458 \\ & 0698-3437 \end{aligned}$ |  | RESISTDR 261 OHM 18.125H F TUBULAR RESISTOR 237 OHM 18.125 W F TUBULAR RESISTOR: VAR; TRMR: 5 KOHM 58 WW RESISTOR 51.1K 1\% .125 F F TUBULAR RFSISTOR 133 OHM 1\% .125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 68027 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-2610-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-237 \mathrm{R}-\mathrm{F} \\ & \mathrm{CT} \text {-106-4 } \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-5112-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-133 \mathrm{R}-\mathrm{F} \end{aligned}$ |
| A19R6 <br> A19R7 <br> A19R8 <br> A19R9 <br> A19R10 | $\begin{aligned} & 0757-0460 \\ & 0757-0461 \\ & 210001759 \\ & 0757-0439 \end{aligned}$ |  | RESISTOR 61.9K 18 . 125 W F TUBULAR NOT ASSIGNED <br> RESISTOR 68.1K 18 . 125 H F TUBULAR RFSISTOR: VAR; TRMR; 2 KOHM $5 \%$ WW RESISTOR 6.81K 18 . 125 W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & \text { GB } 027 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / \mathrm{R}-\mathrm{T} 0-6192-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-6812-\mathrm{F} \\ & \mathrm{C} T-106-4 \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-6811-F \end{aligned}$ |
| A 19R11 <br> A 19R1 2 <br> A19R13 <br> A 19R14 <br> A19R15 | $\begin{aligned} & 0757-0200 \\ & 0757-0405 \\ & 0757-0464 \\ & 0757-0442 \\ & 0898-3439 \end{aligned}$ |  | RESISTOR $5.62 \mathrm{~K} \quad 1 \%$. 125W F TUBULAR RESISTIR 162 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 90.9K 1\% .125W F TUBULAR RESISTOR 10K $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOR 178 DHM $1 \%$. 125W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \\ & 24546 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-5621-F \\ & C 4-1 / 8-T 0-162 R-F \\ & C 4-1 / 8-T 0-9092-F \\ & C 4-1 / 8-T 0-1002-F \\ & C 4-1 / 8-T 0-178 R-F \end{aligned}$ |
| A19R16 <br> A19R17 <br> A19R18 <br> A19R19 <br> A19R20 | $\begin{aligned} & 0757-0467 \\ & 0698-3440 \\ & 0757-0466 \\ & 0757-0834 \\ & 0698-3132 \end{aligned}$ |  | RESISTOR 121 K 18. 125W F TUBULAR RESISTOR 196 OHM 1\% .125W F TUBULAR RESISTOR 110K 18 . 125W F TUBULAR RCSISTOR 5.62K 18 .5W F TUBULAR RESISTOR 261 OHM 18 . 125 H F TUBULAR | $\begin{aligned} & 24546 \\ & 16299 \\ & 24546 \\ & 19701 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-1213-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-196 R-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1103-\mathrm{F} \\ & \mathrm{MF} 7 \mathrm{C} 1 / 2-\mathrm{TO} 0-5621-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-2610-\mathrm{F} \end{aligned}$ |
| A19R21 <br> A 19R22 <br> A 19R23 <br> A 19R24 <br> A19R25 | $\begin{aligned} & 0698-3243 \\ & 0698-3443 \\ & 0757-0441 \\ & 0698-3440 \\ & 0698-3243 \end{aligned}$ |  | RESISTOR 178 K 18 . 125W F TUBULAR RESISTOR 287 OHM 18. 125 F F TUBULAR RESISTOR B.25K 1\% -125W F TUBULAR RESISTDR 196 DHM 1\% . 125 W F TUBULAR RESISTOR 178K 1\%. 125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 24546 \\ & 1629 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-1783-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO-287R-F} \\ & \mathrm{C} 4-1 / 8-\mathrm{TO}-8251-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-196 R-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-T 0-1783-\mathrm{F} \end{aligned}$ |
| $\begin{aligned} & \text { A 19R26 } \\ & \text { A19R27 } \\ & \text { A19R28 } \\ & \text { A19R29 } \\ & \text { A19R30 } \end{aligned}$ | $\begin{aligned} & 0698-3445 \\ & 0757-0279 \\ & 0698-3266 \\ & 0757-0442 \\ & 0698-3447 \end{aligned}$ |  | RESISTOR 348 OHM 18.125 W F TUBULAR RESISTOR 3.16K 18 . 125 W F TUBULAR RESISTOR 237K 1\% . 125W F TUBULAR RESISTOR 10K 18.125 H F TUBULAR RESISTIR 422 OHM $1 \%$. 125 W F TUBULAR | $\begin{aligned} & 16299 \\ & 24546 \\ & 16299 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-349 R-F \\ & \mathrm{C} 4-1 / 8-T 0-3161-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-2373-F \\ & \mathrm{C} 4-1 / 8-T 0-1002-F \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-422 R-F \end{aligned}$ |
| A 19R31 <br> A 19R32 <br> A19R33 <br> A19R34 <br> A19R35 | $\begin{aligned} & 0699-3266 \\ & 0698-0082 \\ & 0757-0444 \\ & 0698-3459 \\ & 0698-3162 \end{aligned}$ |  | RESISTOR 237K 18. .125W F TUBULAR RESISTOR 464 OHM 18.125 W F TUBULAR RESISTOR 12.1 K 12.125 W F TUBULAR RESISTIR 383 K 18.125 W F TUBULAR RESISTIR 46.4 K 15 .125W F TUBULAR | $\begin{aligned} & 16299 \\ & 16299 \\ & 24546 \\ & 19701 \\ & 16299 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-T 0-2373-F \\ & \mathrm{C} 4-1 / 8-\mathrm{TO-4640-F} \\ & \mathrm{C} 4-1 / 8-T 0-1212-F \\ & \text { MF4C1/B-TO-3833-F } \\ & \mathrm{C} 4-1 / 8-\mathrm{TO} 0-4642-\mathrm{F} \end{aligned}$ |
| A19R36 <br> A19R37 <br> A19R38 <br> A19R39 <br> A 19 R40 | $\begin{aligned} & 0698-3157 \\ & 0757-0288 \\ & 0698-3155 \\ & 0757-0317 \\ & 0757-0442 \end{aligned}$ |  | RESISTOR 19.6 K 18 . 125 W F TUBULAR RESISTOR 9.09 K 18.125 W F TUBULAR RESISTOR 4.64K 18 .125W F TUBULAR RESISTOR 1.33K 18 .125W F TUBULAR RESISTOR 10K 18 .125W F TUBULAR | $\begin{aligned} & 16299 \\ & 19701 \\ & 16299 \\ & 24546 \\ & 24546 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-1962-F \\ & M F 4 C 1 / 8-T 0-9091-F \\ & C, 4-1 / 8-T 0-4841-F \\ & C 4-1 / 8-T 0-1331-F \\ & C 4-1 / 8-T 0-1002-F \end{aligned}$ |
| A19R41 <br> A19R42 <br> A19R43 <br> A19R44 <br> A19R45 | $\begin{aligned} & 0683-8245 \\ & 0698-3243 \\ & 0698-3446 \\ & 0698-0082 \\ & 0757-0200 \end{aligned}$ |  | RESISTOR 820K 58 . 25H CC TUBULAR RESISTOR 178K 18. 125W F TUBULAR RESISTOR 383 OHM 18.125 W F TUBULAR RESISTOR 464 DHM 18.125 W F TUBULAR RESISTOR 5.62K 18 . 125 W F TUBULAR | $\left\lvert\, \begin{aligned} & 01121 \\ & 15299 \\ & 16299 \\ & 16299 \\ & 24546 \end{aligned}\right.$ | $\begin{aligned} & C B 9245 \\ & C 4-1 / 8-T 0-1783-F \\ & C 4-1 / 8-T 0-383 R-E \\ & C 4-1 / 8-T 0-4640-E \\ & C 4-1 / 8-T 0-5621-F \end{aligned}$ |
| A19R46 <br> A $19 R 47$ <br> A19R48 <br> A19R49 <br> A19R50 | $\begin{aligned} & 0698-3154 \\ & 0698-3441 \\ & 0698-3444 \\ & 0757-0401 \\ & 0698-3440 \end{aligned}$ |  | RESISTOR 4.22K 1\% .125W F TUBULAR RESISTOR 215 OHM 1\%. 125W F TUBULAR RESISTOR 316 OHM $1 \%$. 125W F TUBULAR RESISTOR 100 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RFSISTOR 196 OHM 1\% . 125W F TUBULAR | $\begin{aligned} & 16299 \\ & 15299 \\ & 16299 \\ & 24546 \\ & 16299 \end{aligned}$ | $\begin{aligned} & C 4-1 / 8-T 0-4221-F \\ & C 4-1 / 8-T 0-215 R-F \\ & C 4-1 / 8-T 0-316 R-F \\ & C 4-1 / 8-T 0-101-F \\ & C 4-1 / 8-T 0-196 R-F \end{aligned}$ |
| A19R51 <br> A19R52 <br> A19R53 <br> A19R54 <br> A19R55 | $\begin{aligned} & 0757-0200 \\ & 0698-3154 \\ & 0757-0200 \\ & 0698-3154 \\ & 0757-0280 \end{aligned}$ |  | RESISTOR 5.62K 1\% .125W F TUBULAR RESISTOR 4.22K 1\% .125W F TUBULAR RESISTOR 5.62K 1\% .125W F TUBULAR RESISTOR 4.22K 18 . 125 W F TUBULAR RESISTOR 1K 1\% . 125 F F TUBULAR | $\begin{aligned} & 24546 \\ & 15299 \\ & 24546 \\ & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{T} 0-5621-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-4221-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-5621-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-4221-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-1001-\mathrm{F} \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference <br> Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A19R56 | 0698-3447 |  | RESISTOR 422 DHM 1\%.125W F TUBULAR | 16299 | C4-1/8-T0-422R-F |
| A19R57 | 0698-3447 |  | RESISTIRR 422 DHM 18. 125 W F TUBULAR | 16200 | C4-1/8-T0-422R-F |
| A19R58 | 0698-0082 |  | RESISTOR 464 OHM 1\% . 125 W F TUBULAR | 16209 | C4-1/8-T0-4640-F |
| A 19859 | 0698-3444 |  | RESISTOR 316 DHM 1 \% 125 W F TUBULAR | 16299 | C4-1/8-T0-316R-F |
| A 19R60 | 0698-0082 |  | RESISTOR 464 OHM 1\% .125W F TUBULAR | 16299 | C4-1/8-T0-4640-F |
| A19R61 | 0698-0082 |  | RESISTIR 464 OHM 19.125W F TUBULAR | 16299 | C4-1/8-70-4640-F |
| A19R62 | 0698-0092 |  | RESISTDR 464 OHM 1\%. 125 W F TUBULAR | 16299 | C4-1/8-T0-4640-F |
| A19R63 | 0757-0130 | 1 | RESISTMR 31.6 OHM 17.125 W F TUBULAR | 24546 | C5-1/4-T0-3126-F |
| A19R64 | 0757-0401 |  | RESISTOR 100 OHM 1\%. 125 W F TUBULAR | 2454.6 | C4-1/8-T0-1 01-F |
| A 19 R 65 | 0698-3443 |  | RFSISTER 287 IHM 1\%.125w F TUBULAR | 16299 | C4-1/8-50-287R-F |
| A19R66 | 0757-0294 |  | RESISTOR 17.8 OHM 18 . 125 W F TUBULAR | 19701 | MF4C1/8-T0-17R8-F |
| A19R67 A19RS8 | 0698-3443 |  | RESISTOR 287 OHM $1 \% .125 \mathrm{~W}$ F TUBULAR RESISTOP 13.3K 1\% .125W F TURULAR | 16299 19701 | $\begin{aligned} & \text { C4-1/8-TO-2 87R-F } \\ & \text { MF4C } 1 / 8-\text { TO-1332-F } \end{aligned}$ |
| A19R58 A19R69 | 0757-0289 |  | RESISTOP RESISTOR 1. RES | 10701 24546 24546 | $\left\lvert\, \begin{aligned} & \text { MF 4C } 1 / 8-\text { TO-1332-F } \\ & \text { C } 4-1 / 8-\text { TO-1 } 213-F \end{aligned}\right.$ |
| A19R70 | 0757-0401 |  | RESISTOR 100 OHM 1\% 1225 W F TUBULAR | 24546 | C4-1/8-T0-101-F |
|  | \|0698-3153 |  | RESISTOR 3.83K 18. 125 W F TUBULAR RESISTOR 100 DHM $1 \% .125 \mathrm{~W}$ F TUBILIAR | $\begin{aligned} & 16299 \\ & 24546 \end{aligned}$ | $\begin{aligned} & \mathrm{C} 4-1 / 8-\mathrm{TO}-3831-\mathrm{F} \\ & \mathrm{C} 4-1 / 8-\mathrm{T} 0-101-\mathrm{F} \end{aligned}$ |
| A 20 | 08660-60021 | 1 | BOARD ASSY, RECTIFIFR | 28490 | 08660-60021 |
| A 20 Cl A 20 C 2 | O180-2369 | 2 | CAPACITOR-FXI: $3600 U F+75-10 \% ~ 40 V D C ~ A L$ CAPACITOR-FXD: $18000 \mathrm{UF}+75-10 \%$ 15VDC AL | $\left\lvert\, \begin{aligned} & 56289 \\ & 28480 \end{aligned}\right.$ | $\begin{aligned} & 360362 G 040 A B 2 B \\ & 0180-1968 \end{aligned}$ |
| A20C3 | 0180-2369 |  | CAPACITOR-FXD; $3600 \mathrm{UF}+75-10 \% 40 \mathrm{VDC} \mathrm{AL}$ | 56289 | $3603625040482 B$ |
| A $20 C^{4}$ | 0180-0094 | 2 | CAPACITOP-FXD; $100 \mathrm{UF}+75-10 \% 25 \mathrm{VDC} \mathrm{AL}$ | 56289 | $30010760250 D 2$ |
| A20C5 | 0180-0094 |  | CAPACITOR-FXD: 100UF+75-10\% 25VOC AL | 56289 | 300107F025002 |
| A 2066 | 0180-2334 | 1 | CAPACITRP-FXD; $39000 \mathrm{JF}+75-10 \% 75 \mathrm{VDC} \mathrm{AL}$ | 56289 | $360392 F 0758828$ |
| A 20067 | 0180-2154 | 1 | CAPACITOR-FXD; $19000 \mathrm{~F}+75-10 \% 15 \mathrm{VDC}$ AL | 56289 | $39019850156 L 4$ |
| A20C8 A 20 C 9 | O180-0058 |  | CAPACITOR-FXD; 50UF+75-10\% 25VDC AL CAPACITRR-FXD; 33UF+-10\% 10VDC TA-SOLID | 56289 56289 | $\left\lvert\, \begin{aligned} & 3005065025 C C 2 \\ & 1500336 \times 01082 \end{aligned}\right.$ |
| A20C10 | 0180-0228 |  | CAPACITOR-FXD; 22UF+-10\% 15VOC TA-SOLID | 56289 | $1500226 \times 901582$ |
| A 20C11 | 0180-0049 |  | CAPACITOR-FXO; 20UF+75-10\% 50VDC AL | 56289 | 30D206r.050CC2 |
| $\begin{aligned} & A 20 C R 1 \\ & \text { A } 20 C R 2 \end{aligned}$ | 1901-0638 | 4 | DIODE: MULT: FULL WAVF BRIDGE RECTIFIER NOT ASSIGNED | 28480 | 1901-0638 |
| A $20 C \mathrm{Cr} 3$ | 1901-0638 |  | DIDDE; MULT; ${ }^{\text {CULL }}$ WAVE BRIDGE RECTIFIER | 28480 | 1901-0638 |
| A 20CR 4 | 1901-0638 |  | DIDDF; MULT: FULL WAVE BRIDGE RECTIFIER | 28480 | 1901-0638 |
| A 20CR 5 | 1901-0364 | 1 | DIDDE-MULT FULL HAVE BRIDGE RECTIFIER | 04713 | SDA $10185-4$ |
| $\begin{aligned} & A 20 C R 6 \\ & A 20 C R 7 \end{aligned}$ | $\begin{aligned} & 1901-0638 \\ & 1884-0024 \end{aligned}$ | 1. | DIODE: MULT; FULL WAVE BRIDGE RECTIFIER THYRISTOR: SCR | $\begin{array}{\|l\|l} 28480 \\ 28480 \end{array}$ | $\left\lvert\, \begin{aligned} & 1901-0639 \\ & 1884-0024 \end{aligned}\right.$ |
| A20F1 | 2110-0051 | 1 | FUSE 104 250V | 28480 | 2110-0051 |
| A 20 F 2 | 2110-0332 | 1 | FUSE 3A 125V | 71400 | GMW 3 |
| $\triangle 20 \mathrm{~F} 3$ | 2110-0047 | 3 | FUSE 1A 125V | 71400 | TYPE GMH-1/2 |
| A20F4 | 2110-0047 |  | FUSF 1A 125V | 71400 | TYPF GMH-1/2 |
| A20F5 | 2110-0047 |  | FUSE 1A 125V | 71400 | TYDE G4W-1/2 |
| A20K1 A 20 K 2 | $0490-0908$ $0490-0908$ | 2 | RELAY, 24VDC, CONT 5A $115 V A C$ FORM 4C RELAY, $24 \mathrm{VDC}, \mathrm{CONT} 5 \mathrm{~A}$ 115VAC FORM 4 C | $\begin{aligned} & 77342 \\ & 77342 \end{aligned}$ | R 40-F $1-\mathrm{X4}$-V800 R 40-E1-X4-V800 |
| A20k2 | 0490-0908 |  |  |  | R40-E1-X4-V800 |
| A 20 MP 1 A $20 \mathrm{MP2}$ | 0490-0861 | 2 | SPRING SPRING RLY RTNR RTM | 77342 77342 | P40-P 33 R 40-P 33 |
| A 20 MP 3 | 4040-0554 | 1 | COVER, CAPACITOP | 28480 | 4040-0554 |
| A20R1 | 0757-0442 |  | RESISTOR 10K 1\% . 125 W F TUBULAR | 24546 | $\mathrm{C} 4-1 / 8-\mathrm{TO}-1002-\mathrm{F}$ |
| A 20R2 A 20R3 | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0757-0442 \end{aligned}\right.$ |  | RFSISTOR RESISTOR lok R | 24546 24546 | $\left\lvert\, \begin{aligned} & C 4-1 / 8-T O-1002-F \\ & C 4-1 / 8-T O-1002-F \end{aligned}\right.$ |
| A 2083 A $20 R 4$ | 0757-0442 |  |  | 24546 24546 | C4-1/8-T0-1 002-F C4-1/8-T0-1 002-F |
| A20R5 | 0757-0442 |  | RESISTOR 10 K 12.125 W F TUBULAR | 24546 | C4-1/8-T0-1002-F |
| $\begin{aligned} & A 20 R 6 \\ & \text { A } 20 R 7 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0757-0442 \\ & 0757-0198 \end{aligned}\right.$ | 1 | RESISTOR 10K 1: . 125W F TUBULAR RESISTOR 100 OHM $1 \% .5 \mathrm{H}$ F TUBULAR | $\begin{array}{\|l} 24546 \\ 19701 \end{array}$ | $\begin{aligned} & \text { C4-1/8-TO-1 002-F } \\ & \text { MF7C1/2-TO-101-F } \end{aligned}$ |
| A $20 \times 11$ | 1251-2313 | 6 | CONNECTOR:1-CONT SKT . 04 DIA | 00770 | 3-332070-5 |
| A $20 \times 45$ | 1251-1626 |  | CONNECTOR; PC EDGE: 12-CONT; DIP SOLDER | 71785 | 252-12-30-300 |
| A $20 \times \mathrm{XAK1}$ A20 | $0400-0907$ $0490-0907$ | 2 | SOCKET; ELFC; RELAY 15-CONT DIP SLDR SOCKFT; EIEC; RELAY 15-CONT DIP SLDR | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0490-0907 \\ & 0400-0907 \end{aligned}$ |
| A 21 | 0960-0151 | 1 | CRYSTAL OSCILLATOR: 10 MHZ <br> (EXCEPT OPT'S 001 AND 002) | 28480 | 0960-0151 |
| A 21 | 0960-0150 | 1 | CRYSTAL OSCILLATOR: 10 MHZ (OPT 001 ONLY) (OMIT A21 ASSY FOR OPT 002) | 28480 | 0960-0150 |
| A 22 | $\left\lvert\, \begin{aligned} & 08660-60043 \\ & 08660-20051 \end{aligned}\right.$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | SWITCH ASSY, REFFRENCE HOUSING, PEF. SWITCH | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-50043 \\ & 08560-20051 \end{aligned}\right.$ |
| $\begin{aligned} & \mathrm{A} 22 \mathrm{Cl} \\ & \mathrm{~A} 22 \mathrm{C} 2 \end{aligned}$ | $\left\lvert\, \begin{array}{ll} 0 & 160-2437 \\ 0 & 160-2437 \end{array}\right.$ |  | CAPACITOR-FXD 5000PF +80-20\% 200WVDC CER CAPACITOR-FXD 5000PF +80-20\% 200WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0160-2437 \\ & 0160-2437 \end{aligned}\right.$ |
| A22C3 | O 160-2437 |  | CAPACITOR-FXO 5000PF +80-20\% 200 WVDC CER | 28480 | 0160-2437 |
| A $22 \mathrm{C4}$ | 0 160-2437 |  | CAPACITOR-FXD 5000 PF +80-20\% 200WVDC CER | 28480 | 0160-2437 |
| A22C5 | 0160-2437 |  | CAPACITOR-FXD 5000PF +80-20\% 200WVDC CER | 28480 | 0160-2437 |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A22C6 | 0160-2437 |  | CAPAC.ITAR-FXD 5000PF +80-20\% 200WVDC CFR | 28480 | 0160-2437 |
| A $22 . \mathrm{Jl}$ | 1250-0901 |  | CONNEC TOR-RF SMB M SGL HOLE FR CONNFCTOR-RF SMB M SGL HOLE FR | $2 K 407$ $2 \times 407$ | $\begin{aligned} & 700168 \\ & 700166 \end{aligned}$ |
| A 22 J 3 | 1250-0901 |  | CONNECTIR-RF SMR M SGL HoLE FR | 2<497 | 700166 |
| A22 14 | 1250-0901 |  | CONNFCTOR-RF SMB M SGL HOLE FR | 2K497 | 700166 |
| A22L1 | 9100-1648 | 1 | COIL ; FXD; MOLDED PF CHOKE: 56OUH 5\% | 24226 | $19 / 563$ |
| A22Al | 08660-60027 | 1 | BOARD ASSY, REFERENCE SHITCH | 28480 | 08660-6002? |
| $\begin{aligned} & A 22 A 1 C 1 \\ & A 22 A 1 C 2 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0160-2055 \end{aligned}$ |  | CAPACITOR-FXD . O1UF +80-20\% 100WVDC CER CAPACITOR-FXD .OIUF +80-20\% 100WVDC CER | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 0160-2055 \\ & 0160-2055 \end{aligned}$ |
| A22A1C3 | 0160-2055 |  | CAPACITOP-FXD .OLUF +80-20\% 100WVDC CER | 28430 | 0160-2055 |
| A22A1C4 | 0160-2055 |  | CAPACITIR-FXD .OLUF +80-20\% 100 WVOC CER | 28480 | 0160-2355 |
| A 22 A1k1 | 0490-0916 | 6 | RELAY: REEC: 1A .5A 50V CONT; 5V COIL | $284 \circ 0$ | 0490-0916 |
| A22A1K2 A22A1K3 | 0490-0916 |  | RELAY: PEED; 1A .5A 50V CONT: 5V COIL RELAY; REFD; 1A $.5 A$ 5OV CONT: 5V COIL | $\begin{array}{\|l\|} 28480 \\ 28480 \end{array}$ | $\left\lvert\, \begin{aligned} & 0490-0916 \\ & 0490-0916 \end{aligned}\right.$ |
| A22A2 | 08660-60026 | 1 | BIARD ASSY, REFERENCE AMPLIFIER SWITCH | 28480 | 08660-60026 |
| A22A2Cl | 0160-2055 |  | CAPACITTRR-FXD. 014 L +80-20\% 100 WVDC CER | 28480 | 0160-2055 |
| A22A2C.2 | 0160-2055 |  | CAPACITOR-FXD .OLUF +80-20\% 100HVDC CER | 28480 | 0150-2055 |
| A22ALC3 | 0160-2055 |  | CAPACITOR-FXD . O1UF +80-20\% 100 NVDC CER | 28430 | 0160-2055 |
| A22A2C4 A22A2C5 | -1160-2055 |  | CAPACITOR-FXD .01UF +80-20\% 100 NVDC CER CAPACITOR-FXD .O1UF +80-208 100WVDC CER | 28480 28480 | 0160-2055 $0150-2055$ |
| A $22 \mathrm{~A} 2 \mathrm{C6}$ | 0180-0291 |  | CAPACITMR-FXD; 1UF+-10\% 35VPC TA-SOLID | 56299 | $1500105 \times 9035 \pm 2$ |
| A22A2C7 | 0180-0291 |  | CAPACITOR-FXD; 1UF+-10\% 35VDC TA-SOLID | 56299 | $1500105 \times 903502$ |
| A22 A2C8 | 0160-2055 |  | CAPACITOR-FXO .01UF +80-20\% 100WVOC CER | 28490 | 0160-2055 |
| A22A2C9 | 0160-2055 |  | CAPACITOR-FXD .OLUF +80-20\% 100WVDC CFR | 28480 | 0160-2055 |
| A 22 A2CR 1 | 1901-0040 |  | OIDDE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| A 22A2CR 2 | 1901-0040 |  | DIDOE-SWITCHING 2NS 30V 50MA | 28480 | 1901-0040 |
| $\begin{aligned} & \text { A22A2K1 } \\ & \text { A22A2K2 } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 0490-0916 \\ & 0490-0916 \end{aligned}\right.$ |  | RELAY; REED; 1A .5A 50V CONT; 5V COIL RELAY: RFED: $1 A .5 A$ 50V CONT: 5V COIL | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $0490-0916$ $0490-0915$ |
| A22A2K3 | 0490-0916 |  | RELAY; REED; 1A .5A 50V CONT; 5V COIL | 28480 | 0490-0918 |
| $\begin{aligned} & \text { A } 22 \text { A2L } 1 \\ & \text { A22A2L } \end{aligned}$ | $\left\lvert\, \begin{aligned} & 9140-0118 \\ & 9140-0144 \end{aligned}\right.$ | 1 | COIL: FXD; MOLDED RF CHOKE; 500UH 5\% <br> COIL; FXD: MOLDED RF CHOKE; 4.7UH 10\% | $\begin{aligned} & 24226 \\ & 24226 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 19 / 503 \\ & 10 / 471 \end{aligned}\right.$ |
| A 224201 | 1854-0071 |  | TRANSISTOR NPN SI PD $=300 \mathrm{MH} \mathrm{FT}=200 \mathrm{MHZ}$ | 28480 | 1854-0071 |
| A224202 | 1854-0071 |  | TRANSISTOR NPN SI PD $=300 \mathrm{MW}$ FT $=200 \mathrm{MHZ}$ | 28490 | 1854-0071 |
| A22A203 | 1853-0020 |  | TRANSISTOR PNP SI CHIP PD $=300 \mathrm{MW}$ | 28480 | 1853-0020 |
| A 22 A2R1 | 0698-7227 | 1 | RESISTOR 422 OHM 2\% .05W F TUBULAR | $\begin{aligned} & 24546 \\ & 24546 \end{aligned}$ | C3-1/8-TO-422R-G |
| A22A2R2 | $0698-722$ $0698-7240$ | 1 | RESISTOR RESISTOR 1.47 K | 24546 24546 | C3-1/8-Y0-2b1R-G |
| A22A2R4 | 0698-7248 | 1 | RESISTOR 3.16K 28 . 05 W F TUBULAR | 24546 | C.3-1/8-T0-3161-G |
| A22A2R 5 | 0698-7222 |  | RESISTOR 261 OHM 2\% .05W F TUBLLAR | 24546 | C3-1/8-T0-2618-G |
| A22A2R6 | 0698-7212 |  | RESISTOR 100 OHM 2\%.05W F TUBULAR | 24546 24546 |  |
| A22A2R7 A22 A2RB | $0698-7229$ $0698-7188$ | 1 | RESISTOR 511 OHM 2\% .05W F TUBULAR RFSISTCR 10 OHM 2\% .05W F TUBULAR | 24546 | $\left\lvert\, \begin{aligned} & C 3-1 / B-T O-511 R-G \\ & C 3-1 / 8-T O O-10 R=G \end{aligned}\right.$ |
| A22A2R9 | 0698-7188 |  | RESISTOR 10 OHM 2\%.05W F TUBULAR | 24546 | C3-1/8-T00-10R-G |
| A23 | 08660-60044 | 1 | WIRING HARNESS, MAIN | 28480 | 08860-60044 |
| A 23.13 A 23.3 | 1251-0085 |  |  | 71785 |  |
| A23J3 A 23 J 3 | $1251-1908$ $1251-0545$ | 1 | CONTACT, CONN, U/W RECTANGULAR SER, CONTACT, R \& P CONNECTOR | 81312 81312 | $\left\lvert\, \begin{aligned} & 100-1022^{\circ} \\ & \text { III }-17054 \text { P } \end{aligned}\right.$ |
| A23 J3 | $1251-1910$ | 1 | CONTACT, CONN, U/W RECTANGULAR SER, | 81312 | 100-1016P |
| A23, ${ }^{2} 4$ | 1251-2663 |  | CONNECTOR: PC EDGE: 18-CONT: SOLDER EYE | 05574 | 3VH18/13N5 |
| A23J4 | 1251-0544 | 2 | BOOY, R \& P CONNECTOR,42-MALE CONTACTS | 81312 | MPAC42PG-4192 |
| A 2335 A 23 J 6 | $1251-0544$ $1251-0547$ |  | BODY, $R \& P$ CONNECTOR,42-MALE CONTACTS | $\begin{array}{llll} 8 & 3 & 31 & 2 \\ 8 & 1 & 31 & 2 \end{array}$ | $\text { MRAC } 42 P G-4192$ |
| A23J7 | 1251-1017 | 2 | CONVECTOR, 4-CONT, WINCH JF | 81312 81312 | $J F 2 S=2 P-5 B$ |
| $\begin{aligned} & \text { A } 23 W 1 \\ & \text { A } 23 W 2 \end{aligned}$ |  |  | "UNDER CHASSIS PARTS" <br> "UNDER CHASSIS PARTS" |  |  |
| A 233 W 3 A 23 W 4 A 23 | 08660-60054 | 1 | CABLE ASSY, WHITE <br> mUNDER CHASSIS PARTS" | 28480 | 08660-60054 |
| A 23 W5 |  |  | "UNDER CHASSIS PARTS* |  |  |
| A23W6 | 08660-60056 | 1 | CABLE ASSY, ORANGE | 28480 | 08660-60056 |
| A23W7 | 08660-60058 | 1 | CABLE ASSY, WHITE/RED | 28480 | 08660-60058 |
| A23 W8 | 08660-60057 | 1 | CABLE ASSY, WHITE/GRESN | 28480 | 08660-60057 |
| ${ }^{1} 23 \mathrm{W9}$ | 08660-60071 | 1 | CABLE ASSY, HHITE/BROWN | 28480 | 08660-60071 |
| A 23 WlO | 08660-60052 | 1 | CABLE ASSY, RED | 28480 | 08660-60052 |
| A 23 W 11 | 08660-60053 | 1 | CABLE ASSY, BROWN | 28480 | 08660-60053 |
| A 23W12 | 08660-60075 | 1 | CABLE ASSY, GREEN | 28480 | 08660-60075 |
| A $23 \mathrm{Wl3}$ | 08660-60067 | 1 | CABLE ASSY, WHITE/RED | 23480 | 08680-60067 |
| $\begin{aligned} & A 23 W 14 \\ & A 23 W 15 \end{aligned}$ | 08660-60066 | 1 | CABLE ASSY, WHITF/BLUE CABLE ASSY, WHITE/YELLOW | 28480 28480 | $\begin{aligned} & 08660-60066 \\ & 08660-60059 \end{aligned}$ |

Table 6-3. Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A $23 W 16$ $A$ $A$ $A$ $A$ $23 W 178$ | $\begin{aligned} & 08650-60081 \\ & 08660-60074 \\ & 08560-60072 \\ & 08660-60073 \\ & 08660-60076 \end{aligned}$ | 1 1 1 1 1 | CABLE NSSY, WHITE/RED CABLE ASSY, WHITE/RNOWN CARLE ASSY, WHITE/ ORANGE CABLE ASSY, WHITE/YELLDW CABLF ASSY, WHITF/BLACK | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-60081 \\ & 08660-50074 \\ & 08660-60072 \\ & 08660-60073 \\ & 08660-50076 \end{aligned}$ |
| $\left\lvert\, \begin{array}{lll} A & 2 & 3 W \\ A & 23 W & 1 \end{array}\right.$ | $\left\lvert\, \begin{aligned} & 08660-60077 \\ & 08660-60062 \end{aligned}\right.$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | CABLE ASSY, WHITC/GRAY CABLE ASSY, WHITE (EXCEPT APT 004 ) | $\begin{array}{\|l\|l} 28480 \\ 28480 \end{array}$ | $\left\lvert\, \begin{aligned} & 08660-60077 \\ & 08660-60062 \end{aligned}\right.$ |
| $\begin{aligned} & A 23 W 23 \\ & A 23 W 24 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-60060 \\ & 08660-60093 \end{aligned}\right.$ | 1 | CABLE ASSY, WHITR/ORANGE CABLF ASSY | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $08660-60060$ $08680-60093$ |
| $\begin{aligned} & A 23 W 25 \\ & A 23 W 2 G \\ & A 23 W 27 \end{aligned}$ | 08660-60004 08660-60095 08660-60175 | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | ```CABLE ASSY CABLE ASSY CABLE, VIOLFT MISCFLLANEOUS A23.``` | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-50094 \\ & 08660-60095 \\ & 08660-60175 \end{aligned}$ |
|  | 08660-20052 | 3 | Pin, fuide | 28480 | 08560-20052 |
| A 24 | 08660-60064 |  | WIRING harness | 28480 | 08660-60064 |
| A24P7 | 1251-1017 |  | CONNECTOR, 4-CONT, WINCH JF | 81312 | JF2S-2P-AB |
| A 24 S1 | 3101-1536 | 1 | SHITCH-TGL DPDT 34125 VA C | 28480 | 3101-1536 |
|  |  |  | CHASSIS DARTS |  |  |
| $\begin{aligned} & F_{1} \\ & F_{1} \end{aligned}$ |  |  | PART OF AT (PRIMARY FUSE) PART DF A2O |  |  |
| $\begin{aligned} & \text { F2 } \\ & \text { F3 } \\ & \text { F4 } \\ & \text { F5 } \end{aligned}$ |  |  | PART DF A20. <br> PART DF A2O. <br> PART DF A20. <br> PART DF AZO. |  |  |
| \$1 | 3101-1235 | 1 | SWITCH-SL DPDT-NS 3A $125 V A C$ (INT/EXT RFFERENCE SWITCH) | 22753 | SH 322 |
| T1 | 9100-3543 | 1 | COIL, FXO | 28480 | 9100-3542 |
| T1CR1 | 1901-1001 | 1 | DIDOE, MULT, SILICON, DUAL | 28480 | 1901-1001 |
| $\begin{aligned} & W 1 \\ & W 2 \\ & W 3 \\ & W 4 \\ & W 5 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-60061 \\ & 08660-60061 \end{aligned}\right.$ | 2 | CABLE ASSY, GRAY CABLE ASSY, GRAY PART DF 423. | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\left\lvert\, \begin{aligned} & 08660-60061 \\ & 08660-60051 \end{aligned}\right.$ |
|  | $\left\lvert\, \begin{aligned} & 08660-60046 \\ & 08660-60065 \end{aligned}\right.$ | $\begin{aligned} & 1 \\ & 1 \end{aligned}$ | CABLE ASSY, INTERFACE CABLF ASSY, ORANGE | $\left\lvert\, \begin{array}{l\|l} 28480 \\ 28480 \end{array}\right.$ | $\left\lvert\, \begin{aligned} & 08660-60046 \\ & 08660-50065 \end{aligned}\right.$ |
|  |  |  | miscellanfous parts |  |  |
|  | $\begin{aligned} & 8120-1348 \\ & 5040-1485 \\ & 8150-008272 \\ & 08660-00003 \\ & 08660-00004 \end{aligned}$ | $\begin{aligned} & 1 \\ & 3 \\ & 6 \\ & 1 \\ & 1 \end{aligned}$ | CABLE: UNSHLD 3-COND $18 A W G$ <br> CONDUCTOR ASSEMBLY:PLUG-IN JUMPER <br> WIRE, RED \#18. <br> SUPPORT, 66-PIN CONNECTOR <br> SUPPORT, 42-PIN CONNECTIR | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 8120-1348 \\ & 5040-1485 \\ & 8150-008272 \\ & 08660-00003 \\ & 08660-00004 \end{aligned}$ |
|  | $\begin{array}{\|} 03680-00005 \\ 08660-20167 \\ 08660-00007 \\ 08660-00027 \\ 08660-00028 \end{array}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | BRACKET, LEFT INTERFACE BPACKET, RIGHT INTEPFACE SUPPDRT, REFERENCE OSCILLATOR SUPPORT, LOOD BOX, REAR CLAMP, REF. OSC. (OPT JO2) | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | 08660-00005 08660-20167 08660-00007 08660-00027 08660-00028 |
|  | 08660-00029 <br> 08660-00030 <br> 08660-00031 <br> 08660-00058 <br> 08660-00032 | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | BRACKET, L.P. BOX, LT SD COVER, SLI OSCILLATOR <br> COVER, SLI PHASE DETECTOR GASKET, SL1-N1 <br> COVER, NI | $\begin{aligned} & 28480 \\ & 23480 \\ & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | 08660-00029 08660-00030 08660-00031 08660-00058 08660-00032 |
|  | $\left\lvert\, \begin{aligned} & 08660-00033 \\ & 08660-00034 \\ & 08660-00035 \end{aligned}\right.$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | ```COVER, N2 (OPT 004) COVER, N3 (OPT 004) COVER, SLZ (OPT OO4)``` | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-00033 \\ & 08660-00034 \\ & 08660-00035 \end{aligned}$ |
|  | $\begin{aligned} & 03660-00036 \\ & 08660-00037 \\ & 08660-00038 \\ & 08660-00041 \\ & 08660-00042 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | SUPPORT, H.F. LIW PASS BOX COVER, BOTTOM 1. 3GHZ MOD. LATCH, H.F. LOW PASS BOX COVER, WIRING HARNESS COVER, N2A (OPT 0041 | $\begin{aligned} & 28480 \\ & 28480 \\ & 23480 \\ & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 08660-00036 \\ & 08660-00037 \\ & 08660-50038 \\ & 08660-00041 \\ & 08660-00042 \end{aligned}$ |
|  | $\begin{aligned} & 08660-00043 \\ & 08660-00044 \\ & 08660-00061 \\ & 08660-20040 \\ & 08660-20050 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 3 \\ & 1 \end{aligned}$ | COVER, COUPLING BOARD (OPT O34) COVER, BLANK (OPT 004) BRACKET, CONMECT OP BOARD, P.C. (OPT OO4) HEAT SINK | $\begin{aligned} & 28480 \\ & 28480 \\ & 28480 \\ & 29480 \\ & 28490 \end{aligned}$ | $\begin{aligned} & 08650-00043 \\ & 08650-00044 \\ & 08660-00061 \\ & 08660-20040 \\ & 08560-20050 \end{aligned}$ |

See introduction to this section for ordering information

Table 6-3. Replaceable Parts


Table 6-4. Code List of Manufacturers

| Mfr Code | Manufacturer Name | Address | Zip Code |
| :---: | :---: | :---: | :---: |
| 66627 | neobm | england |  |
| cusim | ${ }_{\text {RIMPA }}^{\text {RINC }}$ | harrisburg pa | 17105 |
| 00605 | STETTNER-TRUSH inc | cazenovia ny | 13035 |
| \%U84M | MABI CO HEE GLLEN GRADLEY CO | milwauke wi | 53212 |
| 01245 | texas instr inc semicono cmpnt liv | dallas ix | 75231 |
| - 02114 | FERROXCUBE Carp RCA COR SOLID State div | SAUGERTIES NY | ${ }_{08876} 12476$ |
| cis | ge cor semiconnuctor prio dept | SYRacuse NY | 138201 <br> 1 |
| 938.48 | PYROHILM CORP | WHIPPANY NJ | 07981 |
| ¢4713 | MOTRRELA SFMICONDUCTLK VIKINS INOUSTKIES INC | PHOENIX AZ CHATSLORTH CA | ${ }_{91311}^{85008}$ |
| C0500 | Airco sper elek civ air ricn co | nogales az | 85621 |
| 00770 07263 | ROBINSON NUGENT INC FAIRCHILT SEMICONGICIOR oiv | NEW ALEANY IN | 47150 94040 |
| 07263 | FAIRCHILD SEMICONGUCTOR OIV MINNESOTA KUELER CO | MINNEAPOLIS MN | 55416 |
| 07716 | TRW INC BURLINGTJN Div | BURLI NGTON IA | 52601 |
| 04353 10299 | C AND K CEMPJNENTS INC CoRNING GL WK ELEC CMPNT div | HATERTOUN MA | 02172 27604 |
| 18324 | SIGNETICS Crikp | Sunnyvale ca | 94086 |
| 19701 | MEPCO/ELECTRA CORP | ${ }^{\text {MINFRAL HELLS }}$ TX | 76067 |
| $2 \times 447$ 22753 | Cablewave syste ys inc | NORTH HAVEN CT | 06473 |
| 22753 $242<6$ |  | HOLL GWOOD FL | 33021 14070 |
| 245+6 | CORNING GLASS WORSS | BRADFORDPA | 16701 |
| 24995 | ENVIRUNMENTAL CONTAINER SY STEMS INC | PALO ALTO CA | 94304 |
| 27014 | NAIIONAL SEMICONDUCTOR CORP | SALO ALTORA Ca | 95051 94304 |
| 30983 | MEPCO/ELECTRA CURP | SAN DIEGOCA | 922121 |
| 32947 | GJURNS INE TRIMPOY PRGU DIV SPRAGUF ELECTKIC CO | RIVERS NORTH ACAMS cha | 92507 01247 |
| 7140 | bussman mpg div of mcgrah-edison co | St louis mo | 63017 |
| 71744 | CHICAGG MINIATURE LAMP WORKS TRW HLEK COMPDNENTS CINCH DIV | ${ }_{\text {CHICAGO IL }}^{\text {elt }}$ grove village il | 60840 60007 |
| 11785 72130 7 | TRW ELEK COMPONENTS CINCH DIV ELECTRG MUTIVE MFG CO INC | ELK Grove village il | 60007 06226 |
| 73743 | Fischer speital mfg co | CINCINNATI OH | 45206 |
| 73894 74976 | J F D electronics corp Johnson ef momen | BASECA MN ${ }^{\text {BRROKLN }}$ NY | 11219 56093 |
| 75042 | TRW inc Philajelphia div 3 m company | Philadelphia Pa St Paul mn | 19108 55101 |
| 70493 | gell industries inc miller jw div | COMPTON CA | 90224 |
| 77342 | potter e brumfielo oiv amp inc | princeton in | 47570 |
| 78159 81312 | ILLINGIS TOOL HORKS INC SHAKEPROOF WINCHESTER ELEK OIV LITON IND INC | ELGIN LL CT | 60126 06779 |
| ${ }_{83166}$ | WICTORY ENGINERING CORP | SPRINGFIELD NJ | -0779 |
| 84411 <br> 9044 <br> 0 | TRW CAPaCitor oiv AMPHENOL SALES Div of bunx er-ramo | OgALL ALA NE | 69153 63042 |
| 91637 | AMPLENOL SALES Dics jaf bunker-ramo | Columbus ne | 68642 |
| 91880 91425 | Malco meg Coin inc | CHICAGO IL | 60650 |
| 91924 | HONEYHELL | FREEPORT IL | 61032 |
| 98291 | WECKESSER ${ }_{\text {SEALECTRU }}^{\text {CJTP }}$ | MAMARONECK NY | ${ }_{10544}$ |

## SECTION VII MANUAL CHANGES

## 7-1. INTRODUCTION

$7-2$. This section will be used in future issues or revisions of this manual to provide back-dating information.

7-3. In the interim, any necessary changes to the information contained in this manual will be documented in Manual Change Sheets shipped with the manual.

# SECTION VIII <br> SERVICE 

## 8-1. INTRODUCTION

8 -2. This section of the manual is designed to aid the technician in returning the instrument to proper operating condition in the shortest time possible should a malfunction occur in any of the operating circuits.

## 8-3. PRINCIPLES OF OPERATION

8-4. Operation of the various circuits within the 8660C mainframe are explained beginning with paragraph 8-87. Each of the phase locked loops, the interface circuits and the Digital Control Unit are briefly explained. These circuits are also graphically shown in the System Block Diagram and Service Sheet 1.

## 8-5. TROUBLESHOOTING

8-6. In general, this section is designed to aid in isolating the assembly, circuit or Plug-in Section which is causing faulty operation, by a series of tables identified in Table 8-1. The tables listed in Table 8-1 identify the source of trouble and also provide information relative to the location of the schematic (Service Sheet, abbreviated SS) of the defective circuit. These Service Sheets provide the schematic, a pictorial display of component locations and technical data about the circuits in the assembly.

8-7. Due to the digital design of the Model 8660 C , two major troubleshooting aids in this manual are an ASM diagram (Algorithmic State Machine, sometimes called a flow chart) located on the last foldout page of this manual and a system of mnemonics (basically a system of abbreviated terms) which serve to reduce clutter in the ASM diagram and in the circuits of the Digital Control Unit (DCU) and interface units. The basic principles of ASM diagrams and an example of ASM diagram use appears beginning in paragraph 8-36. Figure 8-5 illustrates a basic ASM diagram (actually a part of the Model 8660C ASM diagram) and describes the use of an ASM diagram in isolating the cause of a malfunction. Mnemonics are described beginning with paragraph 8-71 and listed in Table 8-4. An explanation of the use of

Table 8-1. 8660C Troubleshooting Tables

| No. | Title |
| :---: | :---: |
| 8-6 | Power Supply Troubleshooting |
| 8.7 | Troubleshooting DCU by Assembly Replacement |
| 8-8 | DCU and Interface Troubleshooting Guide |
| 8.9 | Incorrect Initial Readout |
| 8-10 | Center Frequency Readout Faulty |
| 11 | BCD Data to Mainframe Incorrect |
| 8-12 | Readout is Partially Displayed or Incorrect |
| 8-13 | Only 1 or 2 Half-Digits Displayed |
| 8-14 | Center Frequency Readout Does Not Justify Correctly |
| $8-15$ | Readout Does Not Justify with only One Units Key |
| 8-16 | Either STEP $\uparrow$ or STEP $\downarrow$ Operation Defective |
| 8-17 | Both STEP $\uparrow$ and STEP $\downarrow$ Defective at the RF Output |
| 8.18 | Manual STEP Defective |
| 8.19 | Manual Tune Mode Inoperative |
| 8-20 | Manual Tune Defective on One Range, Fine, Medium, or Coarse |
| 8-21 | Either Up or Down Manual Tune Defective |
| 8-22 | Auto Sweep Defective at all Sweep Rates |
| $8-23$ | Auto Sweep Defective at One Rate |
| 8-24 | Single Sweep Defective |
| 8-25 | Manual Sweep Defective |
| 8-26 | Out-of-Range Indicator Inoperative |
| 8-27 | KYBD Pushbutton Readout Defective |
| 8-28 | STEP Pushbutton Readout Defective |
| 8-29 | Sweep Width Pushbutton Readout Defective |
| 8-30 | Remote Control Problems |
| 8-31 | Harmonics Excessive Below 1.3 GHz |
| 8-32 | Output Frequency is Half Indicated Frequency Above 1.3 GHz |
| 8-33 | Troubleshooting Option 005 Interface Problems |
| 8-34 | Troubleshooting the Reference Section |
| 8-35 | High Frequency Loop Troubleshooting |
| 8-36 | Summing Loop 1 Troubleshooting |
| 8-37 | Summing Loop 2 Troubleshooting |
| 8-38 | N3 Loop Troubleshooting |
| 8-39 | N2 Loop Troubleshooting |
| 8-40 | N1 Loop Troubleshooting |
| 8-41 | Low Frequency Loops Notes |

8-6 Power Supply Troubleshooting
8-7 Troubleshooting DCU by Assembly Replacement
8-8 DCU and Interface Troubleshooting Guide
8-9 Incorrect Initial Readout
8-10 Center Frequency Readout Faulty
8-11 BCD Data to Mainframe Incorrect
8-12 Readout is Partially Displayed or Incorrect
8-13 Only 1 or 2 Half-Digits Displayed
8-14 Center Frequency Readout Does Not Justify Correctly
8-15 Readout Does Not Justify with only One Units Key
8-16 Either STEP $\uparrow$ or STEP $\downarrow$ Operation Defective
8-17 Both STEP $\uparrow$ and STEP $\downarrow$ Defective at the RF Output
8-18 Manual STEP Defective
8-19 Manual Tune Mode Inoperative
8-20 Manual Tune Defective on One Range, Fine, Medium, or Coarse
8-21 Either Up or Down Manual Tune Defective
8-22 Auto Sweep Defective at all Sweep Rates
8-23 Auto Sweep Defective at One Rate
8-24 Single Sweep Defective
8-25 Manual Sweep Defective
8-26 Out-of-Range Indicator Inoperative
8-27 KYBD Pushbutton Readout Defective
8-28 STEP Pushbutton Readout Defective
8-29 Sweep Width Pushbutton Readout Defective
8-30 Remote Control Problems
8-31 Harmonics Excessive Below 1.3 GHz
8-32 Output Frequency is Half Indicated Frequency Above 1.3 GHz
8-33 Troubleshooting Option 005 Interface Problems
8-34 Troubleshooting the Reference Section
8-35 High Frequency Loop Troubleshooting
8-36 Summing Loop 1 Troubleshooting
8-37 Summing Loop 2 Troubleshooting
8-38 N3 Loop Troubleshooting
8-39 N2 Loop Troubleshooting

8-41 Low Frequency Loops Notes
mnemonics is included in the first part of Table 8-4.

## 8-8. RECOMMENDED TEST EOUIPMENT

8-9. Test equipment and accessories required to maintain the Model 8660C are listed in Table 1-2. If the equipment listed is not available, equipment that meets the minimum specifications shown may be substituted.

8-10. Also listed in Table 1-2 is Service Kit HP Model 11672A. This kit consists of extension cables, cable adapters and an alignment tool. The items within the kit are listed individually in Table 1-2. The entire kit, or any part within the kit may be ordered separately.

## 8-11. REPAIR

## 8-12. Factory Selected Components

8-13. Some component values are selected at the time of final checkout at the factory (see Table $5-1$ ). Usually these values are not extremely critical, they are selected to provide optimum compatibility with associated components. These components are identified on individual schematics by an asterisk (*). The recommended procedure for replacing a factory-selected component is shown in Section V of this manual.

## 8-14. Board Repair.

8-15. Etched Circuits. The etched circuit boards in the Synthesized Signal Generator are of the platedthrough type consisting of metallic conductors bonded to both sides of insulating material. The metallic conductors are extended through the component mounting holes by a plating process. Soldering can be done from either side of the board with equally good results. Table 8-2 lists recommendations and precautions pertinent to etched circuit repair work.
a. Avoid unnecessary component substitution; it can result in damage to the circuit board and/or adjacent components.
b. Do not use a high-power soldering iron on etched boards. Excessive heat may lift a conductor or damage the board.
c. Use a suction device (Table 8-2) or wooden toothpick to remove solder from component mounting holes. DO NOT USE A SHARP METAL OBJECT SUCH AS AN AWL OR TWIST

DRILL FOR THIS PURPOSE. SHARP OBJECTS MAY DAMAGE THE PLATED-THROUGH CONDUCTOR.
d. After soldering, remove excess flux from the soldered areas and apply a protective coating to prevent contamination and corrosion. (Avoid getting flux remover on the printed circuit board extractors.) See Table 8-2 for recommendations.

8-16. Etched Conductor Repair. A broken or burned section of conductor can be repaired by bridging the damaged section with a length of tinned copper wire. Allow adequate overlay and remove any varnish from etched conductor before soldering wire into place.

8-17. Component Replacement. Remove defective component from board.

## NOTE

> Although not recommended on boards with high-frequency signals or where both sides of a board are accessible, axial lead components, such as resistors and tubular capacitors, can be replaced without unsoldering. Clip leads neare body of defective component, remove component and straighten leads left in board. Wrap leads of replacement component one turn around original leads. Solder wrap connection and clip off excess lead.

8-18. If component was unsoldered, remove solder from mounting holes, and position component as original was positioned. DO NOT FORCE LEADS INTO MOUNTING HOLES: sharp lead ends may damage plated-through conductor.

8-19. Transistor Replacement. Transistors are packaged in many physical forms. This sometimes results in confusion as to which lead is the collector, which is the emitter, and which is the base. Figure 8-1 shows typical epoxy and metal case transistors and the means of identifying the leads.

8-20. To replace a transistor, proceed as follows:
a. Do not apply excessive heat; see Table 8-2 for recommended soldering tools.
b. If possible, use long-nose pliers between transistor and hot soldering tools.
c. When installing replacement transistors, ensure sufficient lead length to dissipate soldering heat by using about the same length of exposed lead as used for the original transistor.
d. Integrated circuit replacement instructions are the same as for transistors.

8-21. Some transistors are mounted on heat sinks for good heat dissipation. This requires good thermal contact with mounting surfaces. To assure good thermal contact for a replacement transistor, coat both sides with Dow Corning No. 5 silicone compound or equivalent before fastening the transistor to the chassis. Dow Corning No. 5 compound is available in 8 oz . tubes from HP; order HP Part No. 9500-0059.

8-22. Diode Replacement. Solid state diodes have many different physical forms. This sometimes results in confusion as to which lead is the anode (positive), since all diodes are not marked with the standard symbols. Figure $8-1$ shows examples of some diode marking methods. If doubt exists as to polarity, an ohmmeter may be used to determine the proper connection. It is necessary to know the polarity of the ohms lead for the ohmmeter used. (For the HP Model 410B Vacuum Tube Voltmeter, the ohms lead is negative with respect to the common; for the HP Model 412A DC Vacuum Tube Voltmeter, the ohms lead is positive with respect to the common.) When the ohmmeter indicates the least diode resistance, the cathode of the diode is connected to the ohmmeter lead which is negative with respect to the other lead.

## NOTE

Replacement instructions for diodes are the same as those listed for transistors.

8-23. Illustrated Parts Breakdown (IPB's). Figure 6-1 and Figure 6-2 show IPB's for the Cabinet Parts and the inside of the DCU front panel.

## 8-24. MODULE EXCHANGE

$8-25$. Some of the assemblies within the Mainframe Digital Control Unit are available on an exchange-for-credit basis. These assemblies and the special exchange numbers are listed in Table 6-1. When ordering an exchange module be sure to use the special exchange module numbers shown in Table 6-1 and refer to Figure 8-2 for the procedure to be followed.

## 8-26. SAFETY REQUIREMENTS

8-27. Safety requirements are listed on page vii (directly preceding Section I). They are also called out where required in the Manual.

## 8-28. SERVICE AIDS

8-29. Posidriv Screwdrivers. Many of the screws in the instrument appear to be Phillips, but are not. To avoid damage to the screw slots, Pozidriv screwdrivers should be used.

8-30. Extender Boards. Extender boards are furnished with the rack mounting kit (accessory part number 08660-60070). These boards and other furnished assemblies are listed in Section I of this Manual. The extender boards may be used to extend any plug-in board free of the chassis for maintenance except the A3 Interface boards. Figure 8-3 shows a typical use of the extender board for maintenance purposes.

8-31. Part Locator Aids. The locations of chassis mounted parts and assemblies are shown in Figure $8-113$. The locations of individual components mounted on printed circuit boards or other assemblies are shown on the appropriate schematic page or the page opposing it. The part reference designator is the assembly number followed by the schematic reference designator (for example, A6R9 is R9 on the A6 assembly). For specific component description and ordering information refer to the parts list in Section VI.

8-32. Assembly Adjustment Locations. Near the rear cover of this Manual is a series of Figures which locate the adjustments for all assemblies. These Figures are referred to in each of the adjustment procedures in Section V.

8-33. Servicing Aids on Printed Circuit Boards. The servicing aids include test points, transistor and integrated circuit designations, adjustment callouts and assembly stock numbers.

8-34. Table 8-3 (two sheets) Schematic Diagram Notes, provides information relative to symbols and values shown on the schematic diagrams.

8 -35. Figure $8-4$ illustrates the method used to number the connectors used on the printed circuit boards.

## 8-36. ALGORITHMIC STATE MACHINES (ASM's)

8-37. ASM diagrams, sometimes called flow graphs, are the most practical approach to under-


Figure 8-1. Examples of Diode and Transistor Marking Methods
Table 8-2. Etched Circuit Soldering Equipment

| Item | Use | Specification | Item Recommended |
| :---: | :---: | :---: | :---: |
| Soldering Tool | Soldering, unsoldering | Wattage range: $37-50$; Tip Temp: 750-800 ${ }^{\circ}$ | Unger \#766 handle w/*Ungar \#1237 heating unit |
| Soldering Tip | Soldering, unsoldering | *Shape: pointed | *Unger \#PL111 |
| De-soldering Aid | To remove molten solder from connection | Suction device | Soldapult by Edsyn Co., Arleta, California |
| Resin (flux) Solvent | Remove excess flux from from soldered area before application of protective coating | Must not dissolve etched circuit base board | Freon; Acetone; Lacquer Thinner |
| Solder | Component replace ment. Circuit board repair. Wiring. | Resin (flux) core, high tin content (60/40 tin/lead), 18 gauge (AWG) preferred |  |
| Protective | Contamination, corrosion protection | Good electrical insulation; corrosionprevention properties | Silicone Resin such as GE DRI-FILM**88 |
| * For working on circuit boards; for general purpose work, use Ungar No. 4037 Heating Unit ( $471 / 2-561 / 2 \mathrm{~W}$ ) tip temperature of 850-900 degrees and Ungar No. PL113 1/8" chisel tip. <br> General Electric Co., Silicone Products Dept. Waterford, New York, U.S.A. |  |  |  |

## Module Exchange Repair Program

The module exchange program described here is a method of keeping your Hewlett-Packard instrument in service without repairing the instrument to the component level.


* HP pays postage on boxes mailed in U.S.A.
A.


Rebuilt-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:

Module repair report
Return address label
Tape for resealing box
B.


Open box carefully - it will be used to return defective module to HP. Complete repair report. Place it and defective module in box. Be sure to remove enclosed return address label.
C.


Seal box with tape provided. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label: instead, address box to the nearest HP office.

Figure 8-2. Modular Exchange Procedure


Figure 8-3. Model 8660C With Circuit Board Extended for Maintenance

Table 8-3. Schematic Diagram Notes (1 of 2)

## SCHEMATIC DIAGRAM NOTES

Inductance is in microhenries, Resistance is in ohms and Capacitance is in microfarads unless otherwise noted.

## P/0 part of

- Screwdriver Adjustment

Encloses Front Panel designations

| O | Panel Control |
| :---: | :--- |
| $-\beth$ | Encloses Rear Panel <br> designations |

Circuit assembly borderline

-     -         -             -                 - Other assembly borderline


## $\xi<\omega$



Numbers in stars on circuit assemblies show locations of test points.

Encloses wire color code. Code used (MIL-STD-681) is the same as the resistor color code. First number identifies the base color, second number the wider stripe, and the third number the narrower stripe. Example: (947 denotes white base, yellow wide stripe, violet narrow stripe.

A 2 Indicates an output from a schematic that goes to an input identified as $\boldsymbol{A}$ on Service Sheet 2.

6 (K) Indicates an input to a schematic that comes from an output identified as $\mathbb{K}$ on Service Sheet 6.

## NOTE

When the above two symbols appear within the borderline of a schematic, they indicate a connection within the borderline of the referenced schematic.
$\xlongequal{\perp} \quad$ Indicates circuit ground.

Table 8-3. Schematic Diagram Notes (2 of 2)



Figure 8-4. Printed Circuit Board Connector Identification
standing circuitry as complex as that in the Model 8660 C DCU.

## DEFINITIONS:

Algorithm: A fixed step-by-step procedure for finding the solution to a problem.

State: A condition, or a set of conditions which exist at a given point in time.

8-38. ASM diagrams are particularly valuable in servicing the Model 8660 C because built-in test features permit the technician to set the DCU to any state. Seven LED's verify or deny that the DCU is in the state selected. The DCU may be held in the selected state, manually stepped to succeeding states or reset to any other state. This is accomplished by temporarily grounding selected Test Points or operating the MAN SW in the self-test facilities.

8-39. Figure 8-5 represents a portion of the overall DCU ASM which is shown in its entirety in Figure 8-122. The following description of the information shown in Figure 8-5 is equally applicable to the overall ASM diagram.

8-40. The mnemonics (Table 8-4) in the state (rectangular) boxes and the qualifier (diamond shaped) boxes are not truly representative of specific electrical points in the circuit; the function represented by the mnemonic may appear at many points in the DCU. Table 8-4, mnemonics information, will enable the technician to quickly locate the points in the DCU where the function appears. The $-\mathrm{H}(>+2.8 \mathrm{~V})$ or the $-\mathrm{L}(<+0.8 \mathrm{~V})$ following the mnemonics indicates that the function is High or Low in the assertive (active) state.

8-41. The lines connecting the qualifiers and the states are not representative of electrical connections. Their purpose is to provide information as to what the next state will be. Usually the qualifier determines which of two states is next. In some cases however, the qualifier holds the present machine state for a predetermined period of time.

8 -42. In the Model 8660 C there are about 112 machine states. Some of these states are used in many operations (see Table 8-4 and the overall ASM diagram). Seven "state" flip-flops determine present machine state by their logic conditions. The outputs of these flip-flops are designated as $\mathrm{A}_{p}$ through $\mathrm{A}_{6}$ and their binary weighting determines
the state number. Take, for instance, the state of $5 / 11 ; A_{6}$ and $A_{4}$, with weighting of 4 and 1 provides the binary number 5 , or $\operatorname{BCD} 101$ for the first part of the number and $\mathrm{A}_{3} \mathrm{~A}_{1}$ and $\mathrm{A}_{p}$ with weighting of 8,2 and 1 provide the binary number of 11 or BCD 1011 for the second part of the number. Breaking the number into two parts is for convenience only - it is shown in both numerals and BCD format for each state in the box (in the example it would be 5-11-101 1011).

8 -43. Refer to Figure $8-5$. The starting point for this ASM diagram is in the upper left hand corner.
$8-44$. State $7 / 15$ is an invalid state. It is representative of ROM addresses which are not normally addressable. There is a remote possibility that one of these addresses might be randomly selected at initial turn on, in which case state $7 / 15$ would force the machine state to $0 / 0$, the normal starting point.

8-45. Figure $8-5$ illustrates the state path for an entry of a number or a decimal point. It also illustrates the start of the state path for justification (decimal point placement) when a decimal point is entered.

## NOTE

The seven "state" LED's, test points and the stepping microswitch (MAN SW) are shown in Figure 8-118 to the left of the ASM. This foldout sheet may be folded out for ready reference while going through the state sequences.

8-46. Numeral Entry State Path (heavy line). When the first entry is made with the keyboard (JF10)-L (J input to flip-flop 10 goes low) is active. Qualifier F10 goes high and the next state is $4 / 10$. (JSW1)-L is a sweep function and has no effect on entries other than sweep functions.

8-47. To follow the state path through the DCU for a numerical entry, remove the cabinet bottom cover and temporarily ground the MAN. TP. All of the LED's should be extinguished, indicating state $0 / 0$ (if they are not, temporarily ground the STATE 0/0 TP).

8-48. Press and hold in a numeric keyboard key until state $4 / 10$ is reached. Note that pressing a numeric key does not (by itself) cause a change in state. The MAN. TP. must be pressed each time the state is changed for any operation.

8-49. In order to reach state $4 / 0$ or any other succeeding state, it is necessary to press the MAN. TP. microswitch. (It is suggested that the MAN. TP. be pressed with the eraser end of a pencil. This switch is very sensitive and the least amount of nervousness may cause a progression through more than one state.)

8-50. Qualifier F7-H is active only in sweep functions so pressing the MAN. TP. when the instrument is in state $4 / 40$ should cause the next state to be $5 / 0$.

8-51. Qualifier DP-L is active only when a decimal point has been entered, so pressing the MAN. TP. one time when in state $5 / 0$ should cause the next state to be $6 / 0$.

8-52. Qualifier NUM-H is active when a numeric entry is made. Pressing the MAN. TP. one time when the state is at $6 / 0$ should cause the next state to be $6 / 1$.

8-53. Qualifier F2-H is active for only the first key entry of any new keyboard entry. In this case the first entry is a numeral, so pressing the MAN. TP. one time should cause the next machine state to be $1 / 5$. State $1 / 5$ includes instructions (RF2, RJCT)-L.

8-54. Qualifier NUM-H following state $1 / 5$ is active, so pressing the MAN. TP. one time should cause the next state to be $0 / 2$ which contains instruction ETKO-L. This instruction causes the number BCD (format) to be stored in a 1 digit shift register KO.
$8-55$. Pressing the MAN. TP. one time now causes the next state to be $0 / 3$ which contains instructions KDTK-L and CK10. Qualifier CKB-H is low and the state remains at $0 / 3$ until the BCD data from the K 0 register is clocked into the least significant digit of the keyboard shift register ( 10 clock pulses).

8-56. When CKB-H again goes high the path is directly through states $6 / 14,1 / 1,4 / 1,1 / 9$ and $4 / 9$ to state $4 / 10$. (Once again, the MAN TP must be pressed one time for each state progression.)

8-57. Qualifier KDN-H is active only when a keyboard key is pressed. Since it takes only a few microseconds to reach state $4 / 0, \mathrm{KDN}-\mathrm{H}$ is active and the high output holds the machine state in state $4 / 10$ until the key is released and KDN-H goes low.
$8-58$. When KDN-H goes low (and the MAN. TP. is pressed), the next state is $5 / 10$. Since this is a local operation, RMT-H is low and the next state, when the MAN. TP. is pressed, is $0 / 0$. The instrument is now ready for the next keyboard entry.

## 8-59. Decimal Entry State Path

8-60. Note that for a decimal entry in the manual step mode the decimal point key must remain pressed in and the MAN. TP. must be pressed one time for each state change.

8-61. When a decimal point is entered on the keyboard, the path is the same as the numeral path until state $5 / 0$ is reached. Since DP-L is now active, the next state is $5 / 1$.

8-62. If the decimal point is the first keyboard entry, qualifier $\mathrm{F} 2-\mathrm{H}$ following state $5 / 1$ is active and the next state is $1 / 5$.

8-63. State $1 / 5$, which contains instructions RF2-L, RKB-L and RJCT-L is followed by NUM-H. Since the entry was not a number, the next state is $3 / 5$ which contains instruction SJCT-L. The state path from this point back to state $0 / 0$ is the same as it was for a numeric entry.

8-64. If the decimal point was not the first entry, qualifier F 2 -H following state $5 / 1$ is low and state $1 / 5$ is bypassed.

## 8-65. Units Entry State Path.

$8-66$. As with a numeric or decimal entry, the keyboard key for the unit selected ( $\mathrm{Hz}, \mathrm{kHz}, \mathrm{MHz}$, or GHz ) must remain pressed in and the MAN. TP. must be pressed one time for each state change.
$8-67$. When a units key ( $\mathrm{Hz}, \mathrm{kHz}, \mathrm{MHz}$, or GHz ) is pressed the state path is the same as it is for a numeral until state $6 / 0$ is reached. When state $6 / 0$ is reached, qualifier NUM-H is low and the next state is $0 / 4$.

8-68. State $0 / 4$ which contains instruction RKO-L is followed by qualifier QU1-H. Since a units entry has been made, QU1-H is active and the next state is $1 / 5$.

8-69. State $1 / 6$ which contains instructions JUS-L, JF2-L, KF3-L and a clock, CK10J, is followed by qualifier QJO-H. QJO-H is active until the keyboard entry is justified (decimal point is positioned properly for the units selected).


Figure 8-5. Part of the Algorithmic State Machine for Model 8660C DCU

8-70. When QJO-H goes low the remaining state path is the same as it was for a numeric or decimal point entry until state $0 / 0$ is again reached.

## 8-71. MNEMONICS

8-72. Many of the terms used to describe functions of the DCU, ASM and interface circuits would take up entirely too much room if they were spelled out each time they were used. Most of these terms are abbreviated by the use of mnemonics and shown in Table 8-4. Also shown in the mnemonics table is a definition of such terms, locations where the terms are used, the point of origination of the terms, and information as to whether the mnemonics are high or low in the assertive (active) state (illustrated by an H or an L that follows the mnemonics).

8-73. Note that the mnemonics do not follow normal dictionary type identifications, but are identified by function.

## 8-74. LOGIC SYMBOLS AND DESCRIPTIONS

$8-75$. Table $8-5$ shows some of the "basic building blocks" of logic symbols with the equivalent electronics circuits.

8-76. Figure 8-6 illustrates gates and inverters which are used throughout the instrument. These integrated circuits are shown to avoid repeating details on each schematic.

8-77. Other, more complex, integrated circuits are explained in the supporting text for the schematic on which they appear.

## 8-78. TROUBLESHOOTING

8-79. Mnemonics. Before proceeding with troubleshooting this instrument the technician should become familiar with the use and meaning of mnemonic terms. These terms appear throughout the Algorithmic State Machine (flow graph) and the schematics. The terms are defined in Table 8-2.

8-80. Algorithmic State Machine (ASM). The ASM which appears on a foldout page (Figure 8-119) covers all of the functions of the DCU within the instrument. A partial ASM for the DCU appears in Figure 8-5. The paragraphs directly preceding Figure $8-5$ provide information relative to the basic use of the ASM in troubleshooting the instrument.

8-81. Troubleshooting Procedures. Basically there are three troubleshooting methods defined in this manual. They are:
a. A logical procedure for replacement of circuit boards in the Digital Control Unit for those who have a spare set of assemblies on hand. This procedure is to be followed in the sequence shown when a malfunction has been traced to the DCU. Some of these assemblies are available on an exchange basis (see Section VI for more information regarding this procedure.
b. Repair to the assembly level. With this procedure, assemblies are ordered to replace the known defective assembly. This procedure eliminates the requirement to repair to the component level. Information is provided in tabular format to assist the technician in locating the cause of the malfunction.
c. Repair to the component level. In this procedure, the cause of a malfunction is localized to an assembly and reference is then made to the applicable Service Sheet to provide additional information required to repair to the component level.

8-82. The troubleshooting tables which follow serve a dual purpose. These tables identify the circuit board or assembly which is the cause of the malfunction; if it is not desired to make repairs to the component level, a replacement assembly may be ordered from the part numbers which appear in Section VI of this manual. If repairs are to be made to the component level, the tables also refer to the appropriate schematic diagram and additional technical data to aid the technician in making such repairs.

## NOTE

If symptoms of the cause of the malfunction indicate that the trouble is in a given assembly or circuit, the technician may proceed directly to the applicable table, and perform the specified tests without going through the preceding tests. Each table refers to the assembly and the Service Sheet for the assembly which is most likely to be causing the malfunction.

8-83. The troubleshooting tables are arranged in the most likely cause of the malfunction order. This order is as follows:
a. Table 8-6, Power Supply Troubleshooting.
b. Table 8-7, DCU Repair by Replacement. (To be used only if DCU trouble is suspected and a spare set of compatible assemblies are on hand.
c. Table $8-8$ is a guide designed to lead the technician to the defective assembly within the DCU.
d. Table 8-9 through Table 8-30, DCU and interface troubleshooting tables.
e. Table 8-31 through 8-40, Mainframe RF loops troubleshooting.

## NOTE

When a malfunction has been found and corrected in any circuit containing adjustable components, the adjustment procedures specified in Section $V$ of this manual for the repaired circuit should be performed.

8-84. Each of the troubleshooting tables list the test equipment required to perform the tests in the

Table and refer the technician to the appropriate Service Sheet which contains additional information about the circuit.

8-85. In Table 8-8, , the steps referred to in the prior steps column must have been observed and found to be operating properly before proceeding to the next function of any step.

8-86. The following notes apply to all of the troubleshooting Tables:
a. Always check qualifiers or instructions in the machine state with which they are listed.
b. Refer to Table 8-4 for descriptions of mnemonics and "where used" information.
c. When an instruction or qualifier which should be high is found to be low, the source is listed as the faulty assembly. However, it is possible that the load may be shorted to a low level. Circuit trace and isolate before ordering a replacement assembly.

Table 8-4. Mnemonics Information (1 of 13)
How to use this table:
When the mnemonic has been found and identified, the remaining three columns provide the following information:
The Assy No. column identifies the assembly where the mnemonics appear. The * indicates the assembly where the mnemonic originates.

The "Where Used SS No." column identifies the Service Sheet(s) on which the mnemonic appears.
The * identifies the Service Sheet on which the mnemonic originates.
Prefix all assembly numbers with A1 except those which are prefixed in the assembly number column as $\mathrm{A} 3 \mathrm{~A}(\mathrm{x})$.

The ASM State column indicates the state(s) in which the mnemonics appear. When followed by a " $Q$ " the mnemonic is a qualifier following the state shown.

The mnemonics are also used on all DCU Service Sheets (SS), the Interface Service Sheets and the ASM, Figure 8-122.

| Mnemonic | Description | Assy No. | Where Used SS. No. | ASM State |
| :---: | :---: | :---: | :---: | :---: |
| $+20 \mathrm{~V}$ | +20 V regulated | A8, A11, A2 | 33, 21 |  |
| +4V | +4V unregulated | A12 | 36 |  |
| $+5 \mathrm{~V}$ | +5 V regulated | A1, A2, A3, A4 A5, A6, A7, A8, A9, A10, A12, A3A1, A3A2, A3A1-a,A3A2-a | $\begin{aligned} & 19,20,22,24 \\ & 25,27,30,32, \\ & 33,34,35,36 \\ & 37,38,39,40 \end{aligned}$ |  |
| $-10 \mathrm{~V}$ | -10 V regulated | A8, A2, A11 | 21, 33 |  |
|  | Note: All voltages generated in mainframe power supply. |  |  |  |
| 100 KCK | 100 kHz Clock to keyboard | A1*, A2 | $20 *, 21$ |  |
| 13GL-L | 1.3 GHz select for 86602 | A7*, A6 | 32*, 31 |  |
| 16LIM-L | 160 MHz limits (special only) | A7*, A6 | 32*, 31 |  |
| A0 | State flip-flop A0 output | A4*, A1, A5 | $26 *, 19,25,28$ |  |
| A2 | State flip-flop A2 output | A4*, A1, A5 | $26^{*}, 19,25,28$ |  |
| A2TR-H | A2 register to A bus | A5*, A9 | 27*, 34 | 3/1 |
| A3 | State flip-flop A3 output | A4*, A1, A5 | $26^{*}, 19,25,28$ |  |
| A3TR-H | A3 register to A bus | A5*, A9 | $28^{*}, 34$ | $\begin{aligned} & 2 / 13,2 / 12, \\ & 3 / 0 \end{aligned}$ |

Table 8-4. Mnemonics Information (2 of 13)

| Mnemonic | Description | Assy No. | Where Used SS. No. | ASM State |
| :---: | :---: | :---: | :---: | :---: |
| A4 | State flip-flop A4 output | A4*, A1, A5 | $26 *, 19,25,28$ |  |
| A5 | State flip-flop A5 output | A4*, A1, A5 | $26 *, 19,25,28$ |  |
| A6 | State flip-flop A6 output | A4*, A1, A5 | 26*, 19, 25, 28 |  |
| ADD-H | Add command to ALU | A5*, A7 | 28*, 32 | $\begin{aligned} & 2 / 12,3 / 10 \\ & 3 / 1,2 / 1,1 / 15 \\ & 3 / 4 \end{aligned}$ |
| ADD-L | Subtract command to ALU | A5*, A7 | 28*, 32 | $2,0,2 / 13,1 / 14,$ |
| ADDCK-H | ALU clock control | A6*, A3, A7 | 29*, 24,32 |  |
| ADOF-L | Add offset (special) | A5 | 28 | $\begin{aligned} & 3 / 2,2 / 6,1 / 10, \\ & 1 / 7 \end{aligned}$ |
| ALU1 | ALU1 Binary 1 | A7*, A6 | 32*, 29 |  |
| ALU2 | ALU Binary 2 | A7*, A6 | 32*, 29 |  |
| ALU4 | ALU Binary 4 | A7*, A6 | 32*, 29 |  |
| ALU8 | ALU Binary 8 | A7*, A6 | 32*, 29 |  |
| AREGCK-H | A register clock | A6*, 9 | 29*, 34 |  |
| ATR-H | A register to R bus | A5*, A9 | $28^{*}, 34$ | $\begin{aligned} & 3 / 2,2 / 15,2 / 6, \\ & 3 / 7,3 / 4,0 / 9 \end{aligned}$ |
| AT01. | A Register to output 1 | A9*, A10 | 34*, 35 |  |
| AT02 | A. Register to output 2 | A9*, A10 | 34*, 35 |  |
| AT04 | A Register to output 4 | A9*, A10 | $34 *, 35$ |  |
| AT08 | A Register to output 8 | A9*, A10 | $34^{*}, 35$ |  |
| B0-L | 9 clock gate signal | A5*, A3, A5 | 24*, 36 |  |
| BR-L | Brightness control of readout | A3*, A12 | $24^{*}, 26$ |  |
| CDN-L | [See (KIUP-CPN)-L] |  |  |  |
| CF-H | Center Frequency | A2 ${ }^{*}$, 44 | $21^{*}, 25$ | $\begin{aligned} & 6 / 8 Q, 4 / 3 Q \\ & 6 / 3 Q, 6 / 10 Q \end{aligned}$ |
| CFR-H | Center Frequency Readout | A1*, A4 | 19*, 25 | 6/6Q, $6 / 15 Q$ |

Table 8-4. Mnemonics Information (3 of 13)

| Mnemonic | Description | Assy No. | Where Used SS. No. | ASM State |
| :---: | :---: | :---: | :---: | :---: |
| CK | 1 MHz System Clock | $\begin{aligned} & \mathrm{A} 1 *, \mathrm{~A} 2, \mathrm{~A} 3, \\ & \mathrm{~A} 4, \mathrm{~A} 5, \mathrm{~A} 6, \\ & \mathrm{~A} 7, \mathrm{~A} 8, \mathrm{~A} 9 \\ & \mathrm{~A} 10, \mathrm{~A} 3 \mathrm{~A} 1 \end{aligned}$ | $\begin{aligned} & 20 *, 22,24 \\ & 26,27,29,32, \\ & 33,34,35,37, \\ & 39 \end{aligned}$ |  |
| CK10-L | Clock 10. Instruction for ten clock pulses. | A4*, A5, A6 | $26^{*}, 27,29$ | $\begin{aligned} & 2 / 13,3 / 2,2 / 12 \\ & 3 / 0,3 / 1,2 / 15 \\ & 2 / 9,2 / 1,1 / 15 \\ & 2 / 0,0 / 9,1 / 13 \\ & 1 / 14,2 / 7,1 / 12 \\ & 3 / 8,2 / 5,2 / 6 \\ & 0 / 3,1 / 11,3 / 7 \\ & 1 / 2,1 / 3,1 / 4 \\ & 3 / 4,1 / 8,0 / 1 \\ & 1 / 7,1 / 10 \end{aligned}$ |
| CK10CK-H | Gated control for chain of 10 clock pulses | A6*, A3 | $29^{*}, 23$ |  |
| CK10J-L | Decimal point justification clock | A3*, A5, A6 | 23*, 27, 29 | 1/6 |
| CK1213-L | Instruction for 12 or 13 clock pulse train | A5*, A6 | $27 *, 29$ | $\begin{aligned} & 2 / 13,2 / 12,3 / 0 \\ & 3 / 1 \end{aligned}$ |
| CKA-H | Clock A ANDED with CKB, signifies completion of 12 or 13 clock pulses | $\begin{aligned} & \mathrm{A} 5^{*}, \mathrm{~A} 4, \mathrm{~A} 6, \\ & \mathrm{~A} 8 \end{aligned}$ | $\begin{aligned} & 27 *, 25,29, \\ & 33 \end{aligned}$ | $\begin{aligned} & 2 / 13 Q, 2 / 12 Q \\ & 1 / 10 Q, 3 / 0 Q \\ & 3 / 1 Q \end{aligned}$ |
| CK12-L <br> CK13-L |  |  |  |  |
| CKB-H | Clock B, signifies completion of 10 clock pulses | $\begin{aligned} & \mathrm{A} 5 *, \mathrm{~A} 4, \mathrm{~A} 3 \\ & \mathrm{~A} 6, \mathrm{~A} 8 \end{aligned}$ | $\begin{aligned} & 27 *, 25,23, \\ & 29,33 \end{aligned}$ | $3 / 2 Q, 2 / 13 Q$, 2/12Q, 3/0Q, 3/1Q, 2/15Q, $1 / 15 Q, 2 / 1 Q$, 2/9Q, 2/0Q, $0 / 9 Q, 1 / 13 Q$, 1/14Q, 2/7Q, $0 / 1 Q, 1 / 4 Q$, 3/4Q, 1/3Q, $1 / 12 Q, 3 / 8 Q$, $2 / 5 Q, 0 / 3 Q$, 1/11Q, 2/6Q, 3/7Q, 1/2Q, $1 / 3 Q, 1 / 8 Q$, 1/10Q, 1/7Q |
| CMND P-L | Permanent command from external programming interface | A3A1*, A2 | $39 *, 21$ |  |

Table 8-4. Mnemonics Information (4 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS. No. | ASM State |
| CMND T-L | Temporary command from external programming interface | A3A1*, A2 | $39 *, 21$ |  |
| CNT1 | Parallel dump count, binary 1 | A5*, A10 | 27*, 35 |  |
| CNT2 | Parallel dump count, binary 2 | A5*, A10 | $27^{*}, 35$ |  |
| CNT4 | Parallel dump count, binary 4 | A5*, A10 | 27*, 35 |  |
| CNT8 | Parallel dump count, binary 8 | A5*, A10 | $27^{*}, 35$ |  |
| COAXCK | 2 MHz clock input from interface board | A1 | 20 |  |
| CODE 1 CODE 2 | These are bias levels that are used to aid in leveling the output of the RF Section. See RF Section Manual. | A6* | 31* |  |
| CTR-H | Center Frequency register to R bus | A5*, A6 | $28^{*}, 29$ | $\begin{aligned} & 2 / 1,2 / 0,1 / 7 \\ & 1 / 15,1 / 14 \end{aligned}$ |
| CTT-H | Center Frequency register to T bus | A5*, A6 | $28^{*}, 29$ | $\begin{aligned} & 2 / 9,2 / 7,3 / 8, \\ & 1 / 8 \end{aligned}$ |
| CUP-H | Count up instruction to sweep | A5*, A8 | $28^{*}, 33$ | 2/12, 3/0, 3/1 |
| D1-1 | Digit 1 BCD 1 | A10* | 35*, 37 |  |
| D1-2 | Digit 1 BCD 2 | A10* | 35*, 37 |  |
| D1-4 | Digit 1 BCD 4 | A10* | 35*, 37 |  |
| D1-8 | Digit 1 BCD 8 | A10* | $35 *, 37$ |  |
|  | Note <br> Repeat for digits 2 through 9. Note that digits proceed in numerical sequency from right to left. |  |  |  |
| D10-1 | Digit 10 BCD 1 | A10* | $35^{*}, 37$ |  |
|  | Note Digit 10 BCD 2, 4 and 8 are not used. |  |  |  |
| DAOUT | Digital to Analog output (sweep ramp) | A8*, J1 | $33 *$ |  |
| DBL-L | Double Frequency Output | $\begin{aligned} & \mathrm{A} 6^{*}, \mathrm{~A} 3, \mathrm{~A} 9, \\ & \mathrm{~A} 11 \end{aligned}$ |  |  |
| DP-L | Decimal point qualifier | A2*, A4 | $35^{*}, 37$ | 5/0Q |

Table 8-4. Mnemonics Information (5 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| DP1-L <br> thru <br> DP9-L | Readout decimal points. <br> Numbered from right to left. | A3*, A12 | $23^{*}, 36$ |  |
| ETKQ-L | Encoder to K $\emptyset$ register | A1*, A2 | 19*, 22 | 0/2 |
| F LIM-L | Frequency Limits. Out of range annunciator. | A1* | 19*, 37 |  |
| F1-H | Interrupt sweep for new entry, flip-flop. | A1*, A4 | 19*, 25 | 3/12Q, 1/1Q |
| F2-L | Keyboard initial entry, flip-flop. | A4*, A3 | 26*, 23 | 5/1Q, 6/1Q |
| F3-L | Prevents entry of information before justification, flip-flop. | A2* ${ }^{\text {a }}$ A 4 | $21^{*}, 25$ | 5/6Q, 6/9Q |
| F7-H | Sweep function flip-flop (also functions as plug-in remote flip-flop). | A4* | 26*, 25 | $\begin{aligned} & 2 / 8 \mathbf{Q}, 2 / 4 \mathbf{Q} \\ & 2 / 3 \mathbf{Q}, 4 / 0 \mathbf{Q} \end{aligned}$ |
| F8-H | Sweep ramp flip-flop | A4* | 26*, 25 | 6/11Q, 4/11Q |
| F10-H | Start flip-flop | A1*, A4 | 19*, 25 | 0/0Q |
| FM <br> MODE-L | Lights FM MODE lamp in annunciator | A1* | 19* |  |
| FM-H | Frequency modulation instruction | MOD* A1 | 19 |  |
| FPB-L | Causes sweep width register data to be displayed on center frequency readout | $\begin{aligned} & \mathrm{A} 1^{*}, \mathrm{~A} 3 \\ & \mathrm{~A} 4 \end{aligned}$ | 19*, 23 | 6/4Q |
| FTS-H | Sweep width register to S bus | A5*, A7 | 28*, 32 | $\begin{aligned} & 2 / 13,2 / 12,3 / 0, \\ & 3 / 1,2 / 15,1 / 3 \end{aligned}$ |
| G2 0 | Gate 2 to Code $\emptyset$ instruction selector | A5*, A1 | $27^{*}, 19$ |  |
| Hz-H | Hertz | A2*, A3 | 21*, 23 |  |
| IDN-H | Inhibit down | A4* |  | 4/12Q |
| INC-H | Incremental step | A2*, A4 | 21*, 25 | 5/9Q |
| IPB-L | Causes STEP register data to be displayed on center frequency readout | A1*, A3, A4 | 19*, 23, 25 | 5/4Q |
| ITS-H | Increment (step) register to S bus | A5*, A7 | 28*, 32 | 1/15, 1/14, 1/2 |

Table 8-4. Mnemonics Information (6 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| IUP-H | Inhibit up | A4* |  | 6/12Q |
| JCFR-L | See KPBR-JOFR-L |  |  |  |
| JF1-H | J input to FF1 | A1* |  | 0/10 |
| JF2-H | J input to flip-flop 2 | A1*, A4 | 19*, 26 | 0/7, 1/6 |
| JF3-L | J input to flip-flop 3 | A5*, A2 | 28*, 21 | $\begin{aligned} & 1 / 0,1 / 11,1 / 10 \\ & 1 / 13 \end{aligned}$ |
| $\begin{aligned} & \text { (JF7A, } \\ & \text { ILD)-L } \end{aligned}$ | Jinput to flip-flop 7, and Input Load (presets swp counter) | A1*, A4, A8 | 19*, 26, 33 | 0/13 |
| JF7B-L | J input to flip-flop 7 | A2*, A4 | 21*, 26 |  |
| $\begin{aligned} & \text { (JF8, } \\ & \text { IRS)-L } \end{aligned}$ | Jinput to flip-flop 8, and input reset to sweep increment counter | $\begin{aligned} & \mathrm{A} 5 *, \mathrm{~A} 8, \\ & \mathrm{~A} 4 \end{aligned}$ | 28*, 33, 26 | $\begin{aligned} & 0 / 13,2 / 15,2 / 9 \\ & 0 / 0 \end{aligned}$ |
| JF9-H |  |  |  | 0/14, 0/15 |
| JF10-L |  |  |  | 0/0 |
| JIDN-L | J input inhibit down flip-flop | A5*, A4 | 28*, 26 | 2/11 |
| JIUP-L | J input inhibit up flip-flop | A5*, A4 | 28*, 26 | 2/10 |
| (JUS, KF3, (JF2)-L | Justification (DP justify), K input to flip-flop 3 , J input to flip-flop 2 | $\begin{aligned} & \mathrm{A} 5 *, \mathrm{~A} 1, \mathrm{~A} 1 \\ & \mathrm{~A} 2, \mathrm{~A} 3 \end{aligned}$ | $\begin{aligned} & 28^{*}, 19,21, \\ & 23 \end{aligned}$ | 1/6 |
| JSW1-L | JF3-L (1/12) |  |  | 0/0, 0/8 |
| K甲- K9 | Keyboard key pairs | A12*, A2 | 21* |  |
| Kø TK-L | K0 to Keyboard Register | A2 | 22 | 0/3 |
| KA | Keyboard register output A BCD 1 | A2*, A6 | 22*, 29 |  |
| KB | Keyboard register output B BCD 2 | A2*, A6 | 22*, 29 |  |
| KC | Keyboard register output C BCD 4 | A2*, A6 | $22 *, 29$ |  |
| KD | Keyboard register output D BCD 8 | A2*, A6 | $22^{*}, 29$ |  |
| KCFR-L | K input to Center Frequency Readout flip-flop | A5*, A1 | 28*, 19 | 1/8 |
| KCK-L | Keyboard register clock | A3*, A2 | 23*, 22 |  |

Table 8-4. Mnemonics Information (7 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| KD2-L | Keydown 2 | A2*, A1 | $21^{*}, 19$ |  |
| KDN-H | Keydown | A2*, A4 | $21^{*}, 25$ | 4/10Q |
| KF2-H |  |  |  | 0/5 |
| KF3-L |  |  |  | 1/6 |
| KF7-H | K input to flip-flop 7 | A5*, A4 | 28*, 26 | 2/9, 1/0 |
| KF8-H |  |  |  | 2/9 |
| KF9-H |  |  |  | 0/0 |
| KF10-H |  |  |  | 1/1, 1/0, 3/6 |
| KHZ-H | Kilohertz | A2*, A3 | $21^{*}, 23$ |  |
| KIDN-H | K input to inhibit down flip-flop | A5*, A4 | $28^{*}, 26$ | 2/12 |
| $\begin{aligned} & \text { (KIUP, } \\ & \text { CDN)-L } \end{aligned}$ | K input of increment up flip-flop Count down instruction to sweep | A5*, A4, A8 | $28^{*}, 26$ | 2/13 |
| KPB-L | Causes keyboard register data to be displayed on center frequency readout | A1*, A3, A4 | 19*, 23, 25 | 6/14Q |
| $\begin{aligned} & (\mathrm{KPBR}, \\ & \text { JCFR)-L } \end{aligned}$ | K input to pushbutton readout flip-flop, J input to center frequency readout flip-flop | A5*, A1 | 29*, 19 | 3/6 |
| KSW1-H |  |  |  | 0/10 |
| $\begin{aligned} & \text { (KTR, } \\ & \text { CTS)-H } \end{aligned}$ |  |  |  | 1/10 |
| KTT-H | Keyboard register to T bus | A5*, A6 | $28^{*}, 29$ | $\begin{aligned} & 1 / 3,1 / 12,2 / 5 \\ & 1 / 11,1 / 4,1 / 13 \end{aligned}$ |
| KYBCK1 <br> KYBCK2 | These are separate keyboard strobe lines which join at a common point in the A2 assy. | A2* | $21 *$ |  |
| LCL-H | Local/remote input | $\begin{aligned} & \text { A3A1*, A1, } \\ & \text { A2, A3 } \end{aligned}$ | $\begin{aligned} & 39 *, 37,20 \\ & 21,23 \end{aligned}$ |  |
| LD-L | Load resets the A2 and A3 registers on the A9 assy. | A8* ${ }^{*}$ A9 | 33*, 34 |  |

Table 8-4. Mnemonics Information (8 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| MHZ-H | Megahertz | A2*, A3 | 21*, 23 |  |
| MNE-H | Manual entry | A1*, A4 | $20^{*}, 25$ | $\begin{aligned} & 3 / 13 Q, 6 / 13 Q \\ & 1 / 9 Q, 5 / 14 Q \end{aligned}$ |
| NTS-L | Manual tune increment n to S bus | A5*, A7 | $28^{*}, 21$ | 2/1, 2/0 |
| NUM-H | Numeral | A2*, A4 | $21^{*}, 25$ | 6/0Q, 1/5Q |
| OFS-L | Offset frequency (special) | A4 | 25,37 | $\begin{aligned} & 4 / 2 \mathrm{Q}, 3 / 10 \mathrm{Q} \\ & 5 / 5 \mathrm{Q}, 5 / 7 \mathrm{Q} \\ & 3 / 3 \mathrm{Q} \end{aligned}$ |
| OPID1 | Output plug-in digit 1 BCD 1 | $\begin{aligned} & \mathrm{J} 6 \text { pin } 33^{*}, \\ & \mathrm{~A} 6, \mathrm{~A} 7 \end{aligned}$ | 31, 32 |  |
| OPID2 | Output plug-in digit 2 BCD 2 | J6 pin 34*, A7 | 32 |  |
| OPID4 | Output plug-in digit 4 BCD 4 | J6 pin $35^{*}, \mathrm{~A} 7$ | 32 |  |
| OPR-L | Option reset. <br> Option $004-100 \mathrm{~Hz}$ resolution. | A5*, A3 | 27*, 24 |  |
| OPRO-L | Option readout. <br> Option $004 \cdot 100 \mathrm{~Hz}$ resolution | A1*, A3 | 19*, 24 |  |
| OTS-L | Offset frequency to S bus | A5*, A7 | 28*, 32 | $\begin{aligned} & 2 / 6,1 / 10,1 / 7, \\ & 3 / 2 \end{aligned}$ |
| OVEN-L | Oven signal (oven not at temperature when lamp is lit). (Annunciator) | A21* | 2*,19 |  |
| OVRNG-L |  |  |  |  |
| PBCOM-L | Pushbutton common | A1* | $28^{*}, 19$ |  |
| PBF-L | Sweep width readout pushbutton | A1* | 19* |  |
| PBI-L | Increment (step) readout pushbutton | A1* | 19* |  |
| PBK-L | Keyboard readout pushbutton | A1* | 19* |  |
| PD-H | Parallel dump | A5*, A10 | 28*, 35 | 2/9, 3/7 |
| PDN-L |  |  |  | 3/7, 2/9, 0/9 |
| PDS-L | Parallel dump sweep | A1*, A5, A9 | 19*, 28, 34 | 0/9 |
| PI1 | Data to plug-in section, binary 1 | A6*, A11 | 29*, 37 |  |

Table 8-4. Mnemonics Information (9 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| PI2 | Data to plug-in sections, binary 2 | A6*, A11 | $29 *, 37$ |  |
| PI4. | Data to plug-in sections, binary 4 | A6*, A11 | $28^{*}, 37$ |  |
| PI8 | Data to plug-in sections, binary 8 | A6*, A11 | $29^{*}, 37$ |  |
| PICK-L | Plug-in clock for remote data transfer | A6*, A11 | 29*, 37 | 0/1 |
| PILIM-L | 110 MHz limit select for 86601A | A7*, A6, A1 | 32*, 31, 20 |  |
| PLS-H | Plus (manual tune sense) | A1 ${ }^{*}$, A4 | $20 *, 25$ | 0/12Q, 5/15Q |
| PRDT-L | Power detect (DCU) | $\begin{aligned} & \mathrm{A} 2^{*}, \mathrm{~A} 1, \mathrm{~A} 4, \\ & \mathrm{~A} 6 \end{aligned}$ | $\begin{aligned} & 22 *, 37,20 \\ & 26,29 \end{aligned}$ |  |
| PWRDT-L | Power detect from mainframe | A3A1*, A2 | 39*, 37, 22 |  |
| Q100-H | Qualifier 100 (100 step sweep) | A1*, A4, A8 | $20^{*}, 25,33$ | 5/12Q |
| QA-H | Qualifier A. Frequency above limits. | A6*, A4 | $31 *, 25$ | $2 / 2 \mathrm{Q}$ |
| QAD-H | Qualifier add | A2*, A4 | 21*, 25 | 5/13Q |
| QB-H | Qualifier B. Frequency below limits. | A7*, A4, A6 | $32^{*}, 25,31$ | $\begin{aligned} & 4 / 13 Q, 6 / 7 Q \\ & 4 / 15 Q, 5 / 2 Q \\ & 5 / 7 Q \end{aligned}$ |
| QCTM-H | Qualifier count maximum. Sweep Count. | A8*, A4 | 33*, 25 | 4/14Q, $5 / 11 \mathrm{Q}$ |
| QCTZ-H | Qualifier count zero. Sweep count. | A8*, A4 | $33^{*}, 25$ | 4/7Q |
| QEI-H | Qualifier enter 1 (any entry key) | A2*, A4 | $21^{*}, 25$ | 4/9Q, 4/4Q |
| QJØ -H | Justification operation | A3*, A4 | 23*, 25 | 1/6Q |
| QMSW-H | Qualifier, manual sweep | A1*, A4 | $20^{*}, 25$ | $\begin{aligned} & 0 / 15 Q, 5 / 8 Q \\ & 0 / 11 Q, 0 / 14 Q \end{aligned}$ |
| QSP-H | Qualifier sweep pulse | A1*, A4 | 20*, 25 | 0/10Q |
| QSS-H | Qualifier single sweep | A1*, A4 | $20 *, 25$ | 3/15Q |
| QU1-H | Qualifier units 1 (any units key) | A2*, A4 | $21^{*}, 25$ | 0/4Q |
| RBUS A1 | A register to R bus BCD 1 | A9*, A7 | 34*, 32 |  |

Table 8-4. Mnemonics Information (10 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| RBUS A2 | A register to R bus BCD 2 | A9*, A7 | $34^{*}, 32$ |  |
| REBUS A4 | A register to R bus BCD 4 | A9*, A7 | $34^{*}, 32$ |  |
| REBUS A8 | A register to R bus BCD 8 | A9*, A7 | 34*, 32 |  |
| RBUS C1 | CF register to R bus BCD 1 | A6*, A7 | $29 *, 32$ |  |
| REBUS C2 | CF register to R bus BCD 2 | A6*, A7 | 29*, 32 |  |
| RBUS C4 | CF register to R bus BCD 4 | A6*, A7 | 29*, 32 |  |
| RBUS C8 | CF register to R bus BCD 8 | A6*, A7 | 29*, 32 |  |
| RBUS K1 | M register to R bus BCD 1 | A6*, A7 | $29^{*}, 32$ |  |
| RBUS K2 | M register to R bus BCD 2 | A6*, A7 | 29*, 32 |  |
| RBUS K4 | M register to R bus BCD 4 | A6*, A7 | $29^{*}, 32$ |  |
| RBUS K8 | M register to R bus BCD 8 | A6*, A7 | $29 *, 32$ |  |
| RENC-H | Reset encode counter | A5*, A7 | 28*,32 | $\begin{aligned} & 2 / 13,2 / 12,2 / 8, \\ & 3 / 4,2 / 4,2 / 3, \\ & 1 / 9,3 / 3 \end{aligned}$ |
| RERR-L |  |  |  | 0/4 |
| RF1-L |  |  |  | 0/8 |
| $\begin{aligned} & \text { (RF2, } \\ & \text { RJCT)-L } \end{aligned}$ | Reset flip-flop 2 and reset justification counter. | $\begin{aligned} & \mathrm{A} 2^{*}, \mathrm{~A} 3, \\ & \mathrm{~A} 4 \end{aligned}$ | $\begin{aligned} & 22 *, 23 \\ & 26 \end{aligned}$ | 1/5 |
| RF9-L |  |  |  | 0/9 |
| RKB-L | Reset keyboard register | A5*, A2 | 28*, 22 | 1/5, 1/0 |
| $\begin{aligned} & \text { (RKD2, } \\ & \text { KF10)-H } \end{aligned}$ | Reset keydown flip-flop 2, and K input to flip-flop 10. | A5*, A2, A1 | $28^{*}, 21,19$ | $3 / 6,1 / 1,1 / 0$ |
| RKO-L | Reset K0 register - | A3*, A2 | $23^{*}, 22$ | 0/4 |
| RMT STEP DN-L | Remote step down (increment) | A3A1*, A2 | 39*, 21 |  |
| RMT STEP UP-L | Remote step up (increment) | A3A1*, A2 | 39*, 21 |  |
| RMT-H | Remote Qualifier | A3*, A4 | 23*, 25 | 5/10Q |

Table 8-4. Mnemonics Information (11 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| RMT1-L | Remote data input binary 1 | A3A1*, A2 | $39 *, 37,22$ |  |
| RMT2-L | Remote data input binary 2 | A3A1*, A2 | 39*, 37, 22 |  |
| RMT4-L | Remote data input binary 4 | A3A1*, A2 | 39*, 37, 22 |  |
| RMT8-L | Remote data input binary 8 | A3A1*, A2 | 39*, 37, 22 |  |
| RMTCF-L | Remote center frequency command | A3A1*, A2 | 39*, 22 |  |
| RMTL-L | Readout remote lamp (annunciator) | A1*, lamp | 20* |  |
| ROCK | Readout clock ( 10 kHz ) | A1*, A12 | $20 *, 36$ |  |
| ROGHZ-L | Readout GHz | A3* ${ }^{*}$ A12 | $23^{*}, 36$ |  |
| ROMHZ-L | Readout MHz | A3*, A12 | $23^{*}, 36$ |  |
| ROKHZ-L | Readout kHz | A3* ${ }^{*}$ A12 | 23*, 36 |  |
| ROHZ-L | Readout Hertz | A3* ${ }^{*}$ A12 | $23^{*}, 36$ |  |
| ROI-L | Readout inhibit (option 004) | A1*, A3 | $19^{*}, 24$ |  |
| ROM A1 <br> ROM A2 <br> ROM A4 <br> ROM A8 | To read-only-memory A on A1A12. Controls readout digits 7, 8 and 9 . | A3* ${ }^{*}$ A12 | $24^{*}, 36$ |  |
| ROM B1 <br> ROM B2 <br> ROM B4 <br> ROM B8 | To read-only-memory B on A1A12. Controls readout digits 1 thru 6. Digit 1 is least significant digit. | A3* A12 | 24*, 36 |  |
| RQB-L | Reset qualifier B flip-flop in ALU | A5*, A7 | $28^{*}, 32$ | 2/8, 2/4, 2/2, |
| RQSP-L |  |  |  | 0/11, 0/9 |
| (RQSS, KF8, RSW1)-H | Reset QSS flip-flop, K input to flip-flop 8, reset SW1 flip-flop. | A5*, A4, A1 | $28^{*}, 26,20$ | 2/0, 0/7 |
| RSCAN-H | Reset readout scanner circuit | A3*, A12 | $24^{*}, 36$ |  |
| RSWON-L |  |  |  | 0/8 |
| RZER-L | Reset zero flip-flop | A5*, A7 | 28*, 32 | 2/2, 2/12 |
| S1, S2 | Sense lines from keyboard | A15*, A2 | 21 |  |

Table 8-4. Mnemonics Information (12 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| SBUS F1 | Sweep register to S bus BCD 1 | A6*, A7 | $30 *, 32$ |  |
| SBUS F2 | Sweep register to S bus BCD 2 | A6*, A7 | 30*, 32 |  |
| SBUS F4 | Sweep register to S bus BCD 4 | A6*, A7 | $30 *, 32$ |  |
| SBUS F8 | Sweep register to S bus BCD 8 | A6*, A7 | $30^{*}, 32$ |  |
| SBUS I1 | Step register to S bus BCD 1 | A6*, A7 | 30*, 32 |  |
| SBUS I2 | Step register to S bus BCD 2 | A6*, A7 | $30^{*}, 32$ |  |
| SBUS I4 | Step register to S bus BCD 4 | A6*, A7 | $30^{*}, 32$ |  |
| SBUS I8 | Step register to S bus BCD 8 | A6*, A7 | $30^{*}, 32$ |  |
| SCAN CK | 5 kHz clock to readout control | A1*, A3 | $20^{*}, 24$ |  |
| SCDP-L | Set center frequency decimal point (Stores DP) | A5*, A3 | $28^{*}, 23$ | 2/5 |
| $\begin{aligned} & \text { (SFDP, } \\ & \text { TTF)-L } \end{aligned}$ | Set sweep width decimal point (stores DP), T bus to sweep width register | A5*, A3, A6 | $28^{*}, 23,30$ | 1/11 |
| $\begin{aligned} & \text { (SIDP, } \\ & \text { TTI)-L } \end{aligned}$ | Set step decimal point (stores DP) T bus to step register | A5*, A3, A6 | $28^{*}, 23,30$ | 1/13 |
| SIND1, 4 | Set error lamp driver | A5*, A1, A2 | $28 *, 19,21$ | 2/8,2/3 |
| SIND2-L |  |  |  |  |
| SJCT-L | Set justification counter | A5*, A3 | $28^{*}, 23$ | 3/5 |
| SQB-H | Set qualifier B flip-flop | A5*, A7 | 28*, 32 | $\begin{aligned} & 2 / 13,3 / 2,2 / 15 \\ & 2 / 0,1 / 7,1 / 10 \\ & 1 / 14,2 / 6 \end{aligned}$ |
| ST01-L | Machine state 0/1 | A1*, A6 | 19*, 29 |  |
| ST04-L | Machine state 0/4 | A1*, A3 | 19*, 23 |  |
| STEP-L | Manual tune switch to A1A4 | A1* ${ }^{*}$ A4 | $20^{*}, 25$ | 5/3Q, 4/8Q |
| SW1-H | Sweep 1 qualifier flip-flop | A1*, A4 | 20*, 25 | $\begin{aligned} & 3 / 14 \mathrm{Q}, 4 / 1 \mathrm{Q}, \\ & 0 / 6 \mathrm{Q} \end{aligned}$ |
| SWL-L | Sweep lamp (annunciator) | A1*, A13 | $20^{*}$ |  |

Table 8-4. Mnemonics Information (13 of 13)

| Mnemonic | Description | Where Used |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Assy No. | SS No. | ASM State |
| SWON-H | Sweep on | A1 ${ }^{*}$, A4 | $20^{*}, 25$ | 3/9Q, 4/6Q |
| SZER-L | Set zero flip-flop | A5*, A7 | 28*, 32 | 2/14 |
| TBUS 1 | T bus BCD 1 | A6*, A9 | 29*, 30, 31, |  |
| TBUS 2 | T bus BCD 2 | A10, A3 | 34, 35, 24 |  |
| TBUS 4 | T bus BCD 4 |  |  |  |
| TBUS 8 | T bus BCD 8 |  |  |  |
| TRP-L | Tuning Range zero | $\begin{aligned} & \mathrm{A} 1^{*}, \mathrm{~A} 2, \mathrm{~A} 3 \\ & \mathrm{~A} 7 \end{aligned}$ | $\begin{aligned} & 20^{*}, 21,23, \\ & 32 \end{aligned}$ |  |
| TR1-L | Tuning range 1 coarse | A1*, A7 | 20*, 32 |  |
| TR2-L | Tuning range 2 medium | A1*, A7 | 20*, 32 |  |
| TR3-L | Tuning range 3 fine | A1*, ${ }^{\text {A }} 7$ | 20*, 32 |  |
| TTA-L | T bus to A register | A4*, A9 | 26*, 34 | $\begin{aligned} & 2 / 13,2 / 12,3 / 0 . \\ & 3 / 1,2 / 15,2 / 9 \\ & 2 / 7,2 / 5,2 / 6 \end{aligned}$ |
| TTC-H | $T$ bus to center frequency register | A5*, A6 | 28*, 29 | $\begin{aligned} & 2 / 15,1 / 14,2 / 0, \\ & 2 / 1,2 / 5,1 / 15 \end{aligned}$ |
| TTF.L |  |  |  | 1/11 |
| TTI-L |  |  |  | 1/13 |
| TTM-L | T bus to M register | A4*, A6 | 26*, 31 | $\begin{aligned} & 2 / 13,2 / 12,3 / 0, \\ & 1 / 15,3 / 1,2 / 1, \\ & 2 / 15,2 / 0,1 / 14, \\ & 1 / 12,3 / 8,1 / 10, \\ & 1 / 7,2 / 9 \end{aligned}$ |
| TTRO-L | T bus to readout register | A4*, A3 | 26*, 24 | $\begin{aligned} & 2 / 13,3 / 2,2 / 12, \\ & 2 / 9,2 / 7,2 / 5, \\ & 1 / 4,1 / 2,3 / 4, \\ & 1 / 8,1 / 3 \end{aligned}$ |
| UTT-H | ALU to T bus | A4*, A7 | 26*, 32 | $\begin{aligned} & 2 / 13,3 / 2,2 / 12, \\ & 1 / 10,3 / 0,3 / 1, \\ & 2 / 15,2 / 1,1 / 15, \\ & 2 / 0,0 / 9,1 / 14, \\ & 2 / 6,1 / 7,3 / 7, \\ & 1 / 3,3 / 4,1 / 2 \end{aligned}$ |
| XOR-H | Exclusive OR; ALU does not change data | A5*, A7 | 28*,32 | 1/2, 1/3 |
| ZER-H | Zero qualifier flip-flop | A7*, A4 | 32*, 25 | 6/5Q |


| 1 indicates true signal <br> 0 indicates false signal. |  | on symbol indicates logical inversion (not necessarily electrical) of the input or output signal(s). The logic indicated within the symbol remains the same. <br> $\rightarrow$ indicates direction of signal flow. |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Designation | Logic Symbol | Description | Truth Table | Typical Circuit |
| AND <br> Gate <br> (Positive <br> True) |  | Both input signals (A and B) must be true simultaneously to produce a true output at C. | A B C <br> 0 0 0 <br> 0 1 0 <br> 1 0 0 <br> 1 1 1 |  |
| OR <br> Gate <br> (Positive <br> True) |  | If either input signal (A or B) or both is true, the output at C is true | A B C <br> 0 0 0 <br> 0 1 1 <br> 1 0 1 <br> 1 1 1 |  |
| Time Delay | $A \rightarrow-15 \mathrm{MS} \longrightarrow B$ | Input signal delayed by the time indicated. True input at A produces a true output at B after a 15 ms delay |  | RC and FL Coupling |
| Trigger |  | The binary is a flip-flop which changes state with every true input pulse at $A$. Since $A$ is applied to the bases of both transistors, it is shown centered in the symbol. The negative pulse produces the same effect as a positive pulse applied to the opposite base. To preserve the positive logic, the reset pulse is shown inverted and applied to the opposite side. A reset pulse sets B true. |  |  |



OR
$\begin{array}{lllllll}V_{C C} & 4 B & 4 A & 4 Y & 3 B & 3 A & 3 Y\end{array}$


1820-0661

NAND


NOR
$\begin{array}{lllllll}V_{C C} & 4 Y & 4 B & 4 A & 3 Y & 3 B & 3 A\end{array}$


INVERTER


1820-0174 AND 1820-0577

Figure 8-6. Common Gates and Inverters Used in the Model 8660C

Table 8-6. Power Supply Troubleshooting (1 of 3)


Table 8-6. Power Supply Troubleshooting (2 of 3)


Table 8-6. Power Supply Troubleshooting (3 of 3)

| Symptom | Take the following action or proceed to step shown |
| :---: | :---: |
| +21 and -21 V supplies inoperative. <br> +21 V supply inoperative but -21 V supply OK. <br> -21 V supply inoperative but +21 V supply OK. | Check A20CR4, A20F4 and A20F3, T1, A 20 C 4 and A20C5. <br> Check A20C4 and A20F4. <br> Check A20C5 and A20F3. |

Table 8-7. Digital Control Unit Troubleshooting by Replacement (1 of 2)
Note: Where the procedure column lists several assemblies, replace them in the order shown.

|  | Test | Result | Procedure |
| :---: | :---: | :---: | :---: |
|  | Perform operator's checks 1 through 1-c. | Readout does not display 1.000000 MHz . | Check the 2 MHz and power supply inputs to the DCU. If present, proceed to step 1-a. |
|  | Ground the connector pin labeled PWR DET on the mother board. | Readout displays 1.000000 MHz . Readout display is not correct. | Trouble is in A3 interface assembly. A2, A1, A7, A4, A5, A6, A12. |
|  | Enter a center frequency (within the limits of the RF Section in use) in Hz . With the 86603A RF Section set to 1300 MHz the DCU output data is $1 / 2$ the RO. DBL-L on A1A6 pin 1c is also activated. | Readout correct. (It has been determined that the data out of the DCU is incorrect <br> or <br> Readout incorrect, but RF output is correct.) | $\mathrm{A} 9, \mathrm{~A} 10, \mathrm{~A} 1, \mathrm{~A} 5, \mathrm{~A} 4, \mathrm{~A} 7$. A3, A2, A1, A12. |
|  | Enter center frequencies in $\mathrm{GH}, \mathrm{MHz}, \mathrm{kHz}$ (stay within limits of the RF Section in use). | Readout is not positioned properly. | A3, A2, check wiring from the keyboard to the A1A11 mother board. |
|  | Perform operator's checks 2-a and 2-b. | Readout is not positioned properly. | A3, A2, check wiring from the keyboard to the A1A11 mother board. |
|  | Perform operator's check 2-c. | Readout incorrect. | A1, A4, A5. |
|  | Perform operator's checks 2-d and 2-e. | Readout isn't all zeroes when CLEAR KYBD is pressed. | A2, check wiring between keyboard and A1A11 mother board. |
| 7. | Perform operator's check 3-a with 86601 A ; 4-a with 86602A; 5 -a with the 86603A. | STEP $\uparrow$ operation does not function properly. | $\mathrm{A} 2, \mathrm{~A} 4, \mathrm{~A} 5, \mathrm{~A} 6, \mathrm{~A} 7$, check wiring between keyboard and A1A11 mother board. |

Table 8-7. Troubleshooting by Replacement (2 of 3)

|  | Test | Result | Procedure |
| :---: | :---: | :---: | :---: |
| 7-a. | Check STEP $\downarrow$ operation. | STEP $\downarrow$ operation does not function properly. | Same as step 7. |
| 8. | Perform operator's check 3-b with 86601 A ; 4-b with 86602A; 5-b with the 86603A. | STEP readout incorrect. | A1, A4, A5, A7, check STEP pushbutton switch and wiring. |
| 9. | Perform operator's checks $3-\mathrm{c}$ and 3 -d with the 86601 A , and $4-$ d with the 86602 A ; 5-d with 86603A. | OUT OF RNG light does not flash. | A6, A1, light bulb, A4, A5, A7. Check OPID lines as follows: Extend the A1A7 assembly and check the following lines on connector -1 . |
|  |  |  | RF Sec. 86601 $\mathbf{8 6 6 0 2}$ $\mathbf{8 6 6 0 3}$ <br> Pin 3 H L H <br> Pin C H H L <br> Pin B H H H <br> Pin 2 not used (open) line on A1A7.    |
|  |  |  | NOTE <br> If proper levels are present, trouble is in the A1A7 assembly or associated wiring. If proper levels are not present, trouble is in the cabling to the plug-in unit. |
|  | Perform operator's check <br> 3-e with the 86601A; <br> 4-e with the 86602A: <br> $5-\mathrm{e}$ with the 86603 A . | Readout does not decrease in 111111 Hz steps. | A1, A4, A5, A6, A7. Check MANUAL switch and wiring. Check TUNING control and wiring. Extend the A1A1 assy on two extender boards and use an oscilloscope to check for pulses at A1A1U12 pins 4 and 5. If pulses are present, the A1A1 assembly is probably defective. If the pulses are not present the TUNING control, A1A17, is probably defective. |
| 11. | Perform operator's check <br> 3-f with 86601 A ; 4 -f with <br> $5-\mathrm{f}$ with the 86603 A . | OUT OF RNG light doesn't stay on below lower frequency limit. | A6, A1 lightbulb, A4, A5, A7. Check OPID lines on the A1A7 assembly as shown in step 9. Results are the same. |
| 12 | Perform operator's checks 6-a through 6-d. | Manual tune mode not operating properly | A1, A4, A5, A6, A7. Check MANUAL switch A1A17 TUNING CONTROL. <br> Extend the A1A1 assembly on two extender boards and check as in step 10. Results are the same. |
| 13. | Perform operator's checks 7-a through 7-c for 86601 A . 8-a thru 8 -c with the 86602 A or 86603 A . | Does not perform as specified in Table 3-5. | $\mathrm{A} 4, \mathrm{~A} 5, \mathrm{~A} 6, \mathrm{~A} 7, \Lambda 8, \mathrm{~A} 1, \mathrm{~A} 9, \mathrm{~A} 10, \mathrm{~A} 12 .$ <br> Check lightbulbs, sweep switches and wiring. |

Table 8-7. Troubleshooting by Replacement (3 of 3)

| Test | Result | Procedure |
| :--- | :--- | :--- |
| 14.Perform operator's check <br> 9-a. | Readout and/or output is incorrect. | A1, A4, A5, A6, A7, A8, A9, A10, A12. <br> Check sweep switches and TUNING con- <br> trol. Extend the A1A1 Assembly on <br> two extender boards and check as in <br> step 10. Results are the same. |
| 15.Perform operator's check <br> 9b through 9f. | Incorrect output. | A4, A5, A6, A7, A8, A1, A9, A10, A12. <br> Check SINGLE switch and wiring. |

Table 8-8. DCU and Interface Troubleshooting Guide (1 of 3)

## NOTES

1. The steps referred to in the Prior Steps Required column must have been observed and found to be operating properly before proceeding to the table referred to in any step.
2. The following notes apply to all of the troubleshooting tables:
a. Always check qualifiers or instructions in the machine state with which they are listed.
b. Refer to Table 8-4 for descriptions of mnemonics and "where used" information.
c. When an instruction or qualifier which should be high is found to be low, the source is listed as a faulty assembly. However, it is possible that the load may be shorted to a low level. Circuit trace and isolate before ordering a replacement assembly.

| Step | Instruction or Fault | Prior Steps Req'd |
| :---: | :---: | :---: |
| 1 | When the power is turned on the CENTER FREQUENCY readout should display 1.000000 MHz . If the readout is correct proceed to step 2 . If the readout is not correct, refer to Table 8-9. |  |
| 2. | Enter a new frequency with the keyboard. The CENTER FREQUENCY readout should display the selected frequency; if it does, proceed to step 3 , if it does not, refer to Table 8-10. | 1 |
| 3 | If the CENTER FREQUENCY readout is correct, but BCD data to the mainframe is not, refer Table 8-11. If both are correct, proceed to step 4. If the selected frequency is above 1.3 GHz , the BCD output will be one-half that shown on the readout. | 1 |
| 3. | NOTE <br> The BCD data to the mainframe may be checked at several points. The most readily accessible is at the top of the DCU at connectors A1A11XA11-1 and A1A11XA11-2. See Service Sheet 42 for pin number identification. The logic at these pins is positive $\quad \mathrm{HIGH}=1$, LOW $=0$. |  |

Table 8-8. DCU and Interface Troubleshooting Guide (2 of 3)

| Steps | Instruction or Fault | Prior Steps Required |
| :---: | :---: | :---: |
| 4 | Enter a CENTER FREQUENCY in Hz. The CENTER FREQUENCY readout should display the selected frequency; if it does proceed to step 5 . If it does not, refer to Table 8-10. At frequencies above 1.3 GHz the least significant digit is always even. | 1 |
| 5 | If the CENTER FREQUENCY readout displays only one or two half-digits (other digits are blank) refer to Table 8-12. Otherwise, proceed to step 6. | 1 |
| 6 | If CENTER FREQUENCY readout is not properly positioned when units (decimal point not properly placed) of $\mathrm{GHz}, \mathrm{MHz}, \mathrm{kHz}$ or Hz are entered, and/or associated annunciator lamp does not light, refer to Table 7-14. If only one entry is not properly positioned, proceed to step 7. | 1-5 |
| 7 | If CENTER FREQUENCY readout does not position properly for only one units entry ( $\mathrm{GHz}, \mathrm{MHz}, \mathrm{kHz}$, or Hz ), refer to Table 8-15. Otherwise, proceed to step 8. | 1-5 |
| 8 | If STEP $\uparrow$ or STEP $\downarrow$ do not function properly, refer to Table 8-16. If both STEP $\uparrow$ and STEP $\downarrow$ do not function properly, proceed to step 9 . If both are functioning properly, proceed to step 10 . At frequencies above 1.3 GHz , the STEP is also divided by two. | 1-7 |
| 9 | STEP $\uparrow$ and STEP $\downarrow$ are both defective, refer to Table 8-17. If both function properly, proceed to step 10 . | 1-7 |
| 10 | Manual step does not function properly. If true, refer to Table 8-18. If manual step functions properly proceed to step 11 . At frequencies above 1.3 GHz the manual step is divided by two. | 1-9, 11, 12 |
| 11 | If all manual tune ranges do not function properly refer to Table 8-19. If only one range COARSE, MED or FINE does not function properly, proceed to step 12. | 1-9 |
| 12 | If only one RESOLUTION range (COARSE, MED, or FINE) is defective in the MANUAL MODE refer to Table 8-20. If the frequency can be set only in one direction (up or down) proceed to step 13. | 1-9 |
| 13 | Set the MANUAL MODE switch to COARSE, MED, FINE or STEP. Rotating the TUNING control clockwise should cause an increase in frequency; counterclockwise rotation should cause a decrease in frequency. If the frequency does now change in one direction refer to Table 8-21. If operation is normal proceed to step 14 . | 1-9 |
| 14 | Set the SWEEP MODE switch to AUTO. If all rates (SLO, MED and FAST) are defective refer to Table 8-22. If only one rate is defective proceed to step 15. | 1.7 |
| 15 | If only one sweep rate in the auto sweep mode is defective proceed to Table 8-23. If all sweep rates function properly, proceed to step 16. | 1-7 |

Table 8-8. DCU and Interface Troubleshooting Guide (3 of 3)

| Step | Instruction or Fault | Prior Steps Required |
| :---: | :---: | :---: |
| 16 | If only single sweep is defective in the sweep mode refer to Table 8-24. If single sweep is not defective proceed to step 17. | 1-7, 14, 15 |
| 17 | If only the manual sweep mode is defective refer to Table 8-25. At frequencies above 1.3 GHz manual sweep is divided by two. If manual sweep functions normally proceed to step 18 . | 1-7, 11, 12 |
| 18 | D/A sweep ramp output is defective. Repair or replace the A1A8 assembly. For repair information see Service Sheet 33. | 1-7, 14, 15 |
| 19 | If the out of range lamp does not function correctly refer to Table 8-26. If lamp does not function at all proceed to step 20. | 1-7 |
| 20 | If code 1 or Code 2 information to the RF section is not correct repair or replace the A1A6 assembly. For repair information see Service Sheet 31. | 1-7 |
| 21 | Press the KYBD pushbutton. The CENTER FREQUENCY readout should display the information stored in the keyboard register. If the display is correct, proceed to step 22. If the display is not correct refer to Table 8-27. Leading zeros should not be blanked. | $1-7$ |
| 22 | Press the STEP pushbutton. The CENTER FREQUENCY readout should display the information stored in the step register. If the display is correct, proceed to step 23. If the display is not correct refer to Table 8-28. Check the DBL-L line on SS31 when using the 86603 RF Section. | 1-10 |
| 23 | Press the SWP WIDTH pushbutton. The CENTER FREQUENCY readout display should display the information stored in the sweep register. If the display is correct proceed to step 24 . If the display is not correct refer to Table 8-29. | 1-7, 14, 15 |
| 24 | CENTER FREQUENCY readout visible but dim. Check the mainframe +4 V supply. |  |
| 25 | Some CENTER FREQUENCY readout digits not complete or a random display appears. Repair or replace A1A12 assembly. For repair information see Service Sheet 36. |  |
| 26 | Remote operation is defective. All local functions are correct. Refer to Table 8-30. | $1-25$ |
| 27 | Harmonics excessive below 1.3 GHz or output frequency is twice that programmed. If true, refer to Table 8-31. | 1 |
| 28 | Output frequency is half that programmed when operating above 1.3 GHz . If true, refer to Table 8-32. | 1 |

Table 8-9. Incorrect Initial Readout (1 of 2)


Table 8-9. Incorrect Initial Readout (2 of 2)


Table 8-10. Center Frequency Readout Faulty (1 of 5)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next state wrong - check | Test Point Location | Logic <br> Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Key in a valid center frequency. Check the RF Section output with a frequency counter. If the frequency is correct, but the readout is not, proceed to Table 8-12. |  |  |  |  |  |  |  |
| 2 | If the output frequency and the readout are both faulty, hold in the KYBD key while entering a few frequency. If the readout is correct, but the decimal point is not properly justified, proceed to Table 8-14. |  |  |  |  |  |  |  |

Table 8-10. Center Frequency Readout Faulty (2 of 5)



Table 8-10. Center Frequency Readout Faulty (4 of 5)


Table 8-10. Center Frequency Readout Faulty (5 of 5)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next state wrong - check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrang |
| 1 | (Cont'd) <br> Hold in any numbered key |  |  |  |  |  |  |  |
|  | Manually clock | 4/0 |  | F7 |  |  | A1 A4 | A1A4 |
|  | Manually clock | 5/0 |  | DP | A1A4XA4-1 2 | H | A1A4 | A1A2 |
|  | Manually clock | 6/0 |  | NUM | A1A4XA4-1 C | H | A1A4 | A1A2 |
|  | Manually clock | 6/1 |  |  |  |  |  |  |
| 2 | Extend A1 A1 on an extender board. Set to manual test mode by momentarily grounding the MAN TP Set to state | 0/0 | KD2 |  | A1A1XA1-1 12 | L | A1A1 | A1A2 |
|  | NOTE |  |  |  |  |  |  |  |
|  | Hold in a numbered key while checking KD2. |  |  |  |  |  |  |  |

Table 8-11. BCD Data to Mainframe Incorrect (1 of 2)

|  | Symptom or Instruction | State Succession | Check Instruction | If Next state wrong - check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrong |
|  | Center frequency DCU output data to mainframe loops is incorrect. Center frequency readout is correct. <br> NOTE: BCD data to the mainframe should be $\mathbf{1 / 2}$ of the CF readout. |  |  |  |  |  |  |  |
| 1 | Press STEP $\uparrow$ key repeatedly and observe PD. |  | PD |  | A1A5XA5-1 4 | Flash <br> L to H | con't | A1A5 |
| 2 | Enter CLEAR KYBD, Hz, \& CF (CF readout is blank). |  |  |  |  |  |  |  |
| 3 | Enter $11.111111 \mathrm{MHz} \mathrm{STEP} \uparrow$; |  |  |  |  |  |  |  |

Table 8-11. BCD Data to Mainframe Incorrect (2 of 2)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next state wrong check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 4 | Check mainframe output frequency with counter. If frequency is not the same as entered frequency, switch Sweep Mode from OFF to AUTO and back to OFF. Check output frequency again. |  |  |  |  |  | A1A9 | A1A10* |
|  | *Possibly one or two digits only are faulty. Continue with Step 5 to detect faulty digit. IC corresponding to faulty digit on A10 may be replaced. |  |  |  |  |  |  |  |
| 5 | Enter STEP $\uparrow$. Check for counter reading 22.222222 MHz . Repeat STEP $\uparrow$ and check with counter. Faulty digit will give incorrect reading. |  |  |  |  |  |  |  |

Table 8-12. Readout is Partially Displayed or Incorrect (1 of 2)

\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \& \multirow[b]{2}{*}{Symptom or Instruction} \& \multirow[b]{2}{*}{State Succession} \& \multirow[b]{2}{*}{Check Instruction} \& \multirow[t]{2}{*}{$$
\begin{aligned}
& \text { If Next } \\
& \text { state wrong } \\
& \text { - check }
\end{aligned}
$$} \& \multirow[b]{2}{*}{Test Point Location} \& \multirow[b]{2}{*}{Logic Level} \& \multicolumn{2}{|r|}{Repair or Replace} <br>
\hline Step \& \& \& \& \& \& \& If $\mathbf{O K}$ \& If Wrong <br>
\hline 1

2 \& | Check readout with the following entries: |
| :--- |
| $11111111 \mathrm{~Hz} \quad 44444444 \mathrm{~Hz}$ |
| $22222222 \mathrm{~Hz} \quad 88888888 \mathrm{~Hz}$ |
| If ALL digits show any other number, or an odd character, repair or replace A1A3. |
| If the readout if incorrect but not as defined in step 1 , connect a frequency counter to the RF Section output. Enter If the counter reading is not the same as the frequency entered, refer to Table 8-10. | \& \& \& . \& \& \& \& <br>

\hline
\end{tabular}

Table 8-12 . Readout is Partially Displayed or Incorrect (2 of 2)

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrong |
| 3 | When the counter reading in step 2 is the same as the keyboard entry: <br> a. If the readout right hand six digits is defective replace A1A12U2. <br> b. If the readout of the remaining digits is defective replace A1A12U1. <br> c. If both sides of the readout are faulty refer to Table 8-13. |  |  |  |  |  |  |  |

Table 8-13. Only 1 or 2 Half-Digits Displayed

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Use extender boards to extend A1A3 |  | RSCAN |  | A1A3XA3-2 5 | Square wave 1.2 ms | Step 2 | Step 4 |
| 2 | Use extender boards to extend A1A1 |  | ROCK |  | A1A1XA1-2 E | 10 kHz <br> Clock | A1A12 | A1A1 |
| 3 | Check cabling to A1A12 |  |  |  |  |  |  |  |
| 4 |  |  | SCANCK |  | A1A1XA1-2 5 | 5 kHz <br> Clock | A1A3 | A1A1 |

Table 8-14. Center Frequency Readout Does Not Justify Correctly

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If $\mathbf{O K}$ | If Wrong |
| 1 | Hold KYBD pushbutton and enter 10 MHz , then 10 kHz , then 10 Hz . If the readout justifies correctly refer to Table 8-14. |  |  |  |  |  |  |  |
| 2 | If justification was incorrect in step 1 Hold in the Hz key |  | QU1 |  | A1A4XA4-2 10 | H | cont. | A1A2 |
| 3 | Press Hz key several times |  | JUS |  | A1A5 XA5-2 H | $\mathrm{H} \rightarrow \mathrm{L}$ | A1A3 | cont. |
| 4. | Set to manual mode by momentarily grounding the MAN TP and hold the Hz key down. <br> Set to state Manually clock | $\begin{aligned} & 0 / 4 \\ & 1 / 6 \end{aligned}$ |  |  |  |  | A1A5 | A1A4 |

Table 8-15. Readout Does Not Justify with Only One Units Key (1 of 2)

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If 0K | If Wrong |
| 1 | Use extender boards to extend A1A2 and press the units key that does not respond |  | $\begin{aligned} & \mathrm{GHz} \\ & \mathrm{MHz} \\ & \mathrm{kHz} \\ & \mathrm{~Hz} \end{aligned}$ |  | A1A2U21 pin 8 <br> A1A2XA2-1 L <br> A1A2XA2-1 K <br> A1A2XA2-1 13 | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \\ & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \text { A1 A3 } \\ & \text { A1 A3 } \\ & \text { A1A3 } \\ & \text { A1A3 } \end{aligned}$ | cont. cont. cont. cont. |
| 2 | Use a Logic Probe (or an oscilloscope) to check for a clock while pressing the units key which does not respond |  | GHz <br> MHz <br> kHz <br> Hz |  | A1A2U26 pin 11 A1A2U26 pin 7 A1A2U26 pin 5 A1A2U26 pin 4 | $\begin{aligned} & \mathrm{L} \\ & \mathrm{~L} \\ & \mathrm{~L} \\ & \mathrm{~L} \end{aligned}$ | $\begin{aligned} & \text { A1 A2 } 2 \\ & \text { A1A } 2 \\ & \mathrm{~A} 1 \mathrm{~A} 2 \\ & \mathrm{~A} 1 \mathrm{~A} 2 \end{aligned}$ | cont. cont. cont. cont. |


| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 3 | Verify presence of dc voltages $\quad-10 \mathrm{~V}$ |  |  |  | A1A2XA2-2 L | -10V | cont. | Power <br> Supply |
|  | $+20 \mathrm{~V}$ |  |  |  | A1A2XA2-2 11 | $+20 \mathrm{~V}$ | cont. | Power Supply |
|  |  |  | 100 KCK |  | A1A2XA2-1 9 |  | A1A2 | A1A1 |
|  | NOTE <br> Check the interconnections between the keyboard and A1 A11. |  |  |  |  |  |  |  |

Table 8-16. Either STEP $\uparrow$ or STEP $\downarrow$ Operation Defective (1 of 2)


Table 8-16. Either STEP $\uparrow$ or STEP $\downarrow$ Operation Defective (2 of 2)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 2 | Set to manual test mode by momentarily grounding the MAN TP. Set to state | 5/13 |  |  |  |  |  |  |
|  | Hold STEP $\downarrow$ key in |  |  | QAD | A1A4XA4-1 7 | L | A1A4 | A1 A2 |
|  | Manually clock | 1/14 | ADD |  | A1A5XA5-1 6 | L | cont. | A1A5 |
|  |  |  |  | CKB | A1A5XA5-1 P | H | A1A4 | A1 A5 |
|  | Manually clock | 5/2 |  | QB | A1A4XA4-1 5 | L | A1A4 | A1A5 |
|  | Manually clock | 3/3 |  |  |  |  | $\begin{aligned} & \text { A1A5 } \\ & \text { NOTE } \end{aligned}$ |  |
|  | NOTE |  |  |  |  |  |  |  |
|  | If the manual tune down is also defective, repair or replace A1A7, not A1A5. |  |  |  |  |  |  |  |

Table 8-17. Both STEP $\uparrow$ and STEP $\downarrow$ Defective at the RF Output (1 of 2)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Enter 10 MHz CF and 1 kHz STEP $\uparrow$. Press STEP display pushbutton. Does the readout display show 9 digits with the same character for most; If yes, repair or replace A1A6. |  |  |  |  |  |  |  |
| 2 | Key in Hz on the keyboard and set to manual mode by momentarily grounding the MAN TP. Hold in STEP $\uparrow$ key. |  |  |  |  |  |  |  |
|  | Set to state | 5/9 |  | INC | A1A4XA4-1 F | H | A1A4 | A1A2 |
|  | Manually clock | 5/6 |  | F3 | A1A4XA4-1 A | L | A1A4 | A1A2 |
|  | Manually clock | 1/13 | KTT |  | A1A5XA5-2 P | H | cont. | A1A5 |
|  |  |  | TTI |  | A1A5XA5-2 9 | L | cont. | A1A5 |
|  |  |  | CK10 |  | A1A4XA4-2 17 | L | cont. | A1A4 |
|  |  |  |  | CKB | A1A5XA5-1 P | H | A1 A4 | A1A5 |
|  | Manually clock | 5/13 |  | QAD | A1A4XA4-1 7 | H | A1A4 | A1A2 |

Table 8-17. Both STEP $\uparrow$ and STEP $\downarrow$ Defective at the RF Output (2 of 2)

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong Check | Test Point Location | Logic <br> Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrong |
| $\begin{gathered} 2 \\ \text { (cont) } \end{gathered}$ | Manually clock | 1/15 | CTR <br> ITS | CKB | A1 A5XA5-1 K <br> A1A5XA5-1 D <br> A1A5XA5-1 P | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | cont. cont. A1A4 | $\begin{aligned} & \text { A1 A5 } \\ & \text { A1 A5 } \\ & \text { A1 A5 } \end{aligned}$ |
|  | Manually clock | 3/3 |  |  |  |  |  |  |
|  | Set to state | 0/0 |  |  |  |  |  |  |
|  | Set to state | 4/3 |  | CF | A1A4XA4-1 D |  | A1A4 | A1A2 |
|  | Manually clock |  | CTT |  | A1A5XA5-1 10 | H | cont. | A1A5 |
|  |  |  | TTA |  | A1A4XA4-1 14 | L | cont. | A1A5 |
|  |  |  | CK10 |  | A1A4XA4-2 17 | L | cont. | A1 A5 |
|  |  |  |  | CKB | A1 A5XA5-1 P | H | A1 A4 | A1A5 |
|  | Manually clock | 5/5 |  |  |  |  | A1 A6 |  |

Table 8-18. Manual STEP Defective

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Select manual step <br> NOTE <br> Check continuity between A1A1, mother board, cabling and the switch. |  | $\begin{aligned} & \text { STEP } \\ & \text { STEP } \end{aligned}$ |  | A1A4XA4-2 D <br> A1A1XA1-1 R | $\begin{aligned} & \mathrm{L} \\ & \mathrm{~L} \end{aligned}$ | A1A4 SEE NOTE | cont. |

Table 8-19. Manual Tune Mode Inoperative



Table 8-21. Either Up or Down Manual Tune Defective (1 of 2)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Select fine manual tune and turn the manual tune knob |  | PLS |  | A1A4XA4-1 K | Flash | Step <br> 2 or 3 | cont. |
|  | Extend A1A1 on the extender boards and rotate the manual tune knob |  | $\begin{aligned} & \mathrm{CCW} \\ & \mathrm{CW} \end{aligned}$ |  | A1A1J1 pin 10 A1A1J1 pin 11 | Flash <br> Flash | $\begin{aligned} & \mathrm{A} 1 \mathrm{~A} 1 \\ & \mathrm{~A} 1 \mathrm{~A} 1 \end{aligned}$ | $\begin{aligned} & \mathrm{A} 1 \mathrm{~A} 17 \\ & \mathrm{~A} 1 \mathrm{~A} 17 \end{aligned}$ |
|  | If up tune is defective proceed to step 2 If down tune is defective proceed to step 3 |  |  |  |  |  |  |  |

Table 8-21. Either Up or Down Manual Tune Defective (2 of 2)

Table 8-22. Auto Sweep Defective at All Sweep Rates (1 of 2)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 12 | Enter 10 MHz CF and 10 kHz SWP WIDTH. <br> Press sweep width display pushbutton. If the display is correct proceed to step 3 . If not, proceed to step 2. |  |  |  |  |  |  |  |
|  | Set to manual test mode by momentarily grounding the MAN TP Set to state | 6/10 |  | CF | A1A4XA4-1 D | L | A1A4 | A1A2 |
|  | Manually clock | 1/11 | KTT |  | A1A5XA5-2 P | H | cont. | A1A5 |
|  |  |  | TTF |  | A1A5XA5-2 N | L | cont. | A1A5 |
|  |  |  | JF3 |  | A1A5XA5-2 2 | L | cont. | A1A5 |
|  |  |  | CK10 |  | A1A4XA4-2 17 | L | cont. | A1A4 |
|  |  |  |  | CKB | A1A5XA5-1 P | H | A1A4 | A1A5 |
|  | Manually clock | 6/6 |  |  |  |  | A1A6 |  |
| 3 | Switch to Auto sweep and fast rate. Set to manual test mode by momentarily grounding the MAN TP. Set to state | 4/1 |  | SW1 | A1A4XA4-1 N | H | A1 A4 |  |
|  | grounding the MAN TP. Set to state | 4/1 $0 / 13$ | JF7A | SW1 | A1A4XA4-1 A1 A4XA4-2 | L L | cont. | $\begin{aligned} & \text { A1A1 } \\ & \text { A1A1 } \end{aligned}$ |
|  |  |  |  | No check |  |  | A1A4 |  |
|  | Manually clock | 3/14 |  | SW1 | A1A4XA4-1 N | H | A1 A4 | A1A1 |
|  | Manually clock | 3/12 |  | F1 | A1A4XA4-2 H | L | A1A4 | A1A1 |
|  | Manually clock | 0/10 |  | QSP | A1A4XA4-2 12 | H | A1A4 | A1A1 |
|  | Manually clock | 0/11 |  | QMSW | A1A4XA4-2 13 | L | A1A4 | A1A1 |
|  | Manually clock | 5/11 |  | QCTM | A1A4XA4-1 9 | L | A1A4 | A1A8 |
|  | Manually clock | $5 / 12$ |  | Q100 | A1A4XA4-1 H | H | A1A4 | A1A1 |
|  | Manually clock |  | FTS |  | A1A5XA5-15 | NOTE | cont. | A1A5 |
|  |  |  | A2TR |  | A1A5XA5-1 M | H | cont. | A1A5 |
|  | NOTE |  | ADD |  | A1A5XA5-1 6 | H | cont. | A1A5 |
|  | Flashes high when going from state $5 / 12$ |  | CUP |  | A1A5XA5-1 13 | ${ }^{\text {H }}$ | cont. | A1A5 |
|  | to state $3 / 1$ only. |  | CK1213 |  | A1 A5XA5-1 1 | L | cont. | A1A5 |
|  |  |  | CK10 |  | A1A4XA4-2 17 | L | cont. | A1A4 |
|  |  |  | UTT |  | A1A4XA4-2 16 | H | cont. | A1A4 |
|  |  |  | TTM |  | A1A4XA4-2 14 | L | cont. | A1A4 |
|  |  |  | TTA |  | A1A4XA4-1 14 | L | cont. | A1A4 |
|  |  |  |  |  | A1A5XA5-1 R | H | A4 if both | A1A5 |
|  |  |  |  | CKB | A1A5XA5-1 P | H | OK | A1A5 |

Table 8-22. Auto Sweep Defective at All Sweep Rates (2 of 2)

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrang |
| 3 | Cont'd |  |  |  |  |  |  |  |
|  | Manually clock | 6/5 |  | ZER | A1A4XA4-1 E | L | A1A4 | A1A7 |
|  | Manually clock | 2/2 |  | QA | A1A4XA4-13 | L | A1A4 | A1A6 |
|  | Manually clock | 2/4 |  | F7 |  |  | A1A4 | A1A4 |
|  | Manually clock | 4/11 |  | F8 |  |  | A1A4 | A1A4 |
|  | Manually clock | 0/9 | PDS |  | A1A5XA5-2 6 | L | cont. | A1A1 |
|  |  |  | ATR |  | A1A5XA5-1 L | H | cont. | A1A5 |
|  |  |  | UTT |  | A1A4XA4-2 16 | H | cont. | A1A4 |
|  |  |  | CK10 |  | A1A4XA4-2 17 | L | cont. | A1A4 |
|  |  |  |  | CKB | A1A5XA5-1 P | H | A1A4 | A1A5 |
|  | Manually clock | 3/14 |  |  |  |  |  |  |
|  | Set to auto mode. Enter 10 MHz CF and 10 kHz SWP WIDTH. Switch to manual sweep and tune manual sweep until the output frequency exactly equals 10.005 MHz . |  |  |  |  |  |  |  |
|  | Set to manual test mode by momentarily grounding the MAN TP. Set to state | 5/11 |  | QCTM | A1A4XA4-1 9 | H | A1A4 | A1A8 |
|  | Manually clock | 6/11 |  | F8 |  |  | A1A4 | A1A4 |
|  | Manually clock | 2/15 | ATR |  | A1A5XA5-1 L | H | cont. | A1A5 |
|  |  |  | FTS |  | A1A5XA5-1 5 | H | cont. | A1A5 |
|  |  |  | ADD |  | A1 A5 XA5-1 6 | L | cont. | A1A5 |
|  |  |  | SQB |  | A1 A5XA5-19 | H | cont. | A1A5 |
|  |  |  | JF8 |  | A1A5 XA5-2 K | L | cont. | A1A5 |
|  |  |  | CK10 |  | A1A4XA4-2 17 | L | cont. | A1A4 |
|  |  |  | UTT |  | A1A4XA4-2 16 | H | cont. | A1A4 |
|  |  |  | TTM |  | A1A4XA4-2 14 | L | cont. | A1A4 |
|  |  |  | TTA |  | A1A4XA4-1 14 | L | cont. | A1A4 |
|  |  |  |  | CKB | A1A5XA5-1 P | H | A1A4 | A1A5 |
|  | Manually clock | 4/15 |  | QB | A1A4XA4-1 5 | L | A1A4 | A1A7 |
|  | Manually clock | 2/2 |  |  |  |  |  |  |
|  | Set to state | $0 / 0$ |  |  |  |  |  |  |
|  | Set to state | $0 / 10$ |  | QSP | A1A4XA4-2 12 | L | $\mathrm{A} 1 \mathrm{~A} 4$ | A1 A1 |
|  | Manually clock | 3/14 |  |  |  |  | A1A9 |  |

Table 8-23. Auto Sweep Defective at One Sweep Rate (1 of 2)


Table 8-23. Auto Sweep Defective at One Rate (2 of 2)


Table 8-24. Single Sweep Defective

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point <br> - Check | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Enter 10 MHz CF and 5 MHz SWP WIDTH. Switch to single sweep and any sweep rate. Set to manual test mode by momentarily grounding the MAN TP. Press single sweep pushbutton once. <br> Set to state Manually clock <br> NOTE <br> Check cabling to switches before replacing A1A1. | $\begin{aligned} & 3 / 15 \\ & 2 / 9 \end{aligned}$ | RQSS | QSS | A1A4XA4-2 B <br> A1A5XA5-2 F | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \text { A1A4 } \\ & \text { A1A1 } \end{aligned}$ | $\begin{aligned} & \mathrm{A} 1 \mathrm{~A} 1 \\ & \mathrm{~A} 1 \mathrm{~A} 5 \end{aligned}$ |

Table 8-25. Manual Sweep Defective (1 of 4)


Table 8-25. Manual Sweep Defective (2 of 4)



Table 8-25. Manual Sweep Defective (4 of 4)

Table 8-26. Out of Range Indicator Inoperative (1 of 2)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Paint Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Use a frequency counter to count the output rf frequency. If the center frequency stops at the upper frequency limit, proceed to step 3. <br> Observe the dc level on the test point while tuning the center frequency above the upper limit. |  |  |  |  | Flash H | A1A4 | cont. |
| 2 | If 86601 A is being used: Extend A1A7 on the extender board |  | $\begin{aligned} & \text { PILIM } \\ & \text { 13GL } \\ & \text { 16LIM } \\ & \text { OPID1 } \\ & \text { OPID2 } \\ & \text { OPID4 } \end{aligned}$ |  | A1A7XA7-1 D A1A7XA7-1 4 A1A7XA7-2 K A1A7XA7-1 3 A1A7XA7-1 C A1A7XA7-1 B | L <br> H <br> H <br> H <br> H <br> H | A1A6 A1A6 A1A6 A1A7 A1A7 A1A7 | cont. cont. cont. cont. cont. cont. |
|  | If 86602 A is being used: Extend A1A7 on the extender board |  | PILIM <br> 13GL <br> 16LIM <br> OPID 1 <br> OPID 2 <br> OPID4 |  | A1A7XA7-1D <br> A1A7XA7-1 4 <br> A1A7XA7-2 K <br> A1A7XA7-1 3 <br> A1A7XA7-1 C <br> A1A7XA7-1 B | H <br> L <br> H <br> L <br> H <br> H | A1A6 A1A6 A1A6 A1A7 A1A7 A1A7 | cont. <br> cont. <br> cont. <br> cont. <br> cont. <br> cont. |

Table 8-26. Out of Range Indicator Inoperative (2 of 2)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| $\begin{aligned} & 2 \\ & \text { cont. } \end{aligned}$ | If 86603 A is being used Extend A1A7 on extender board |  |  |  |  |  |  |  |
|  |  |  | $\begin{aligned} & \text { PILIM } \\ & \text { 13GL } \\ & \text { 16LIM } \\ & \text { OPID1 } \\ & \text { OPID2 } \\ & \text { OPID4 } \end{aligned}$ |  | A1A7XA7-1 D A1A7XA7-1 4 A1A7XA7-2 K A1A7XA7-1 3 A1A7XA7-1 C A1A7XA7-1 B | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \\ & \mathrm{~L} \\ & \mathrm{H} \\ & \mathrm{~L} \\ & \mathrm{H} \end{aligned}$ | A1A6 A1A6 A1A6 A1A7 A1A7 A1A7 | cont. cont. cont. cont. cont. cont. |
|  | NOTE <br> If any of the above checks are wrong repair interconnections. |  |  |  |  |  |  |  |
| 3 | Check OUT OF RNG lamp at upper frequency limit |  |  |  |  | Blinks | A1A6 | cont. |
|  | At upper frequency limit check If lamp is on continuously |  | SIND2 |  | A1A1XA1-1 4 | Flash L | cont. <br> A1A1 | A1A6 cont. |
|  | Ground ERR pin at front of mother board. <br> If the out of range lamp lights <br> If the out of range lamp does not light, check the lamp and wiring. |  |  |  |  |  | A1A1 |  |

Table 8-27. KYBD Pushbutton Readout Defective

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If 0K | If Wrong |
| 1 | Set to manual test mode Set to state | 6/14 |  |  |  |  |  |  |
|  | Press KYBD pushbutton |  |  | KPB | A1A4XA4-1 8 | L | A1A4 | A1A1 |
|  | Manually clock | 1/4 | KTT |  | A1A5XA5-2 P | H | cont. | A1A5 |
|  |  |  | TTRO |  | A1A4XA4-2 15 | L | cont. | A1A4 |
|  |  |  | CK10 |  | A1A4XA4-2 17 | L | cont. | A1A4 |
|  |  |  |  | CKB | A1 A5XA5-1 P | H | A1A4 | A1A5 |
|  | Manually clock | 3/6 |  |  |  |  | A1A7 |  |
|  | NOTE |  |  |  |  |  |  |  |
|  | If KPB is wrong, check A1A11 and cabling. |  |  |  |  |  |  |  |

Table 8-28. STEP Pushbutton Readout Defective

| Step | Symptom or Instruction | State <br> Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 1 | Set to manual test mode by momentarily grounding the MAN TP. Set to state | 5/4 | ITS | IPB |  |  |  |  |
|  | Hold in STEP pushbutton <br> Manually clock | 1/2 |  |  | A1A4XA4-1 B A1A5XA5-1 D | $\begin{aligned} & \mathbf{L} \\ & \mathrm{H} \end{aligned}$ | A1A4 cont. | NOTE A1A5 |
|  | NOTE |  |  |  |  |  |  |  |
|  | If wrong, check A1 A1 and interconnections. | 3/6 | $\begin{aligned} & \text { XOR } \\ & \text { UTT } \\ & \text { TTRO } \\ & \text { CK10 } \end{aligned}$ | CKB | A1A4XA4-2 R | H | cont. | A1A5 |
|  |  |  |  |  | A1A4XA4-2 16 | H | cont. | A1A4 |
|  |  |  |  |  | A1A4XA4-2 15 | L | cont. | A1A4 |
|  |  |  |  |  | A1A4XA4-2 17 | L | cont. | A1A4 |
|  | Manually clock |  |  |  | A1A5XA5-1 P | H | $\mathrm{A} 1 \mathrm{~A} 4$ | A1A5 |
|  |  |  |  |  |  |  | A1A7 |  |

Table 8-29. Sweep Width Pushbutton Readout Defective

\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Step} \& \multirow[b]{2}{*}{Symptom or Instruction} \& \multirow[b]{2}{*}{State Succession} \& \multirow[b]{2}{*}{Check Instruction} \& \multirow[b]{2}{*}{If Next State Wrong - Check} \& \multirow[b]{2}{*}{Test Point Location} \& \multirow[b]{2}{*}{Logic Level} \& \multicolumn{2}{|r|}{Repair or Replace} <br>
\hline \& \& \& \& \& \& \& If 0K \& If Wrong <br>
\hline \multirow[t]{9}{*}{1} \& Set to manual test mode by momentarily grounding the MAN TP. Set to state \& 6/4 \& \multirow{3}{*}{FTS} \& \multirow{9}{*}{FPB

CKB} \& \multirow{3}{*}{| A1A4XA4-1 4 |
| :--- |
| A1A5XA5-1 5 |} \& \multirow{3}{*}{\[

$$
\begin{aligned}
& \mathrm{L} \\
& \mathrm{H}
\end{aligned}
$$

\]} \& \multirow{3}{*}{A1A4 cont.} \& \multirow{3}{*}{| NOTE |
| :--- |
| A1A5 |} <br>


\hline \& \multirow[t]{7}{*}{| Hold in the SWP WIDTH pushbutton Manually clock |
| :--- |
| NOTE |
| If FPB is wrong, check A 1 A 1 and wiring |} \& \multirow[t]{2}{*}{1/3} \& \& \& \& \& \& <br>

\hline \& \& \& \& \& \& \& \& <br>
\hline \& \& \& XOR \& \& A1 A5XA5-2 R \& H \& cont. \& A1 A5 <br>
\hline \& \& \& UTT \& \& A1A4XA4-2 16 \& H \& cont. \& A1A4 <br>
\hline \& \& \& TTRO \& \& A1A4XA4-2 15 \& L \& cont. \& A1A4 <br>
\hline \& \& \& CK10 \& \& A1A4XA4-2 17 \& L \& cont. \& A1 A4 <br>
\hline \& \& \& \& \& A1 A5XA5-1 P \& H \& A1A4 \& A1A5 <br>
\hline \& Manually clock \& $3 / 6$ \& \& \& \& \& A1A7 \& <br>
\hline
\end{tabular}

Table 8-30. Remote Control Problems (1 of 7)

Table 8-30. Remote Control Problems (2 of 7)

| $\infty$ |
| :--- |



Table 8-30. Remote Control Problems (3 of 7)

| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 3-a | Cont'd |  |  |  |  |  |  |  |
|  | ground) J3 pin $9 . \quad$ Check |  | D2-8 |  | A3A2U4 pin 1 | L | cont. | A3A2 |
|  |  |  | D2-4 |  | A3A2U4 pin 14 | L | cont. | A3A2 |
|  |  |  | D2-2 |  | A3A2U4 pin 11 | L | cont. | A3A2 |
|  |  |  | D2-1 |  | A3A2U4 pin 8 | H | cont. | A3A2 |
|  |  |  | CF |  | A1A11XA11-2 33 | H | cont. | A3A1 |
|  |  |  | STEP $\uparrow$ |  | A1A11XA11-2 34 | L | cont. | A3A1 |
|  |  |  | STEP $\downarrow$ |  | A1A11XA11-2 36 | H | cont. | A3A1 |
|  | Remove the ground from J3 pin 31. |  |  |  |  |  |  |  |
|  | Ground J3 pin 30 and pulse (or momentarily ground) J3 pin 9. <br> Check |  | D2-8 |  | A3A2U4 pin 1 | L | cont. | A3A2 |
|  |  |  | D2-4 |  | A3A2U4 pin 14 | L | cont. | A3A2 |
|  |  |  | D2-2 |  | A3A2U4 pin 11 | H | cont. | A3A2 |
|  |  |  | D2-1 |  | A3A2U4 pin 8 | L | cont. | A3A2 |
|  | Check | . | CF |  | A1A11XA11-2 33 | H | cont. | A3A1 |
|  |  |  | STEP $\uparrow$ |  | A1A11XA11-2 34 | H | cont. | A3A1 |
|  | If all check OK |  | STEP $\downarrow$ |  | A1A11XA11-2 36 | L | cont. <br> A1A2 | A3A1 |
| 3-b | See NOTE 2 |  |  |  |  |  |  |  |
|  | If any modulation or rf output plug-in functions can be correctly programmed, continue; if not, proceed to step 3-c. |  |  |  |  |  |  |  |
|  | Perform the following checks for the particular function which has failed. |  |  |  |  |  |  |  |
|  | Ground J3 pins 13, 14, 15 and 16. |  |  |  |  |  |  |  |
|  | ATTENUATION |  |  |  |  |  |  |  |
|  | Ground J3 pins 30 and 31. Check |  | D2-8 |  | A3A2U4 pin 1 | L | cont. | A3A2 |
|  |  |  | D2-4 |  | A3A2U4 pin 14 | L | cont. | A3A2 |
|  |  |  | D2-2 |  | A3A2U4 pin 11 | H | cont. | A3A2 |
|  |  |  | D2-1 |  | A3A2U4 pin 8 | H | cont. | A3A2 |

Table 8-30. Remote Control Problems (4 of 7)

|  | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Step |  |  |  |  |  |  | If OK | If Wrong |
| 3-b | Cont'd |  | Atten |  | J6 pin 24 | Pulses $\mathrm{L} \rightarrow \mathrm{H}$ | cont. | A3A1 |
|  | AM-FM FCTN |  |  |  |  |  |  |  |
|  | Ground J3 pin 29 and pulse (or momentarily ground) J3 pin 9 . <br> Check |  | D2-8 |  | A3A2U4 pin 1 | L | cont. | A3A2 |
|  |  |  | D2-4 |  | A3A2U4 pin 14 | H | cont. | A3A2 |
|  |  |  | D2-2 |  | A3A2U4 pin 11 | L | cont. | A3A2 |
|  | Check |  | D2-1 |  | A3A2U4 pin 8 | L | cont. | A3A2 |
|  | Pulse command |  | AM-FM |  | J5 pin V | $\begin{aligned} & \text { Pulses } \\ & \mathrm{L} \rightarrow \mathrm{H} \end{aligned}$ | cont. | A3A1 |
|  | AM-FM \% |  |  |  |  |  |  |  |
|  | Ground J3 pins 29 and 31 and pulse (or momentarily ground) J3 pin 9 . Check |  | D2-8 |  | A3A2U4 pin 1 | L | cont. | A3A2 |
|  |  |  | D2-4 |  | A3A2U4 pin 14 | H | cont. | A3A2 |
|  |  |  | D2-2 |  | A3A2U4 pin 11 | L | cont. | A3A2 |
|  |  |  | D2-1 |  | A3A2U4 pin 8 | H | cont. | A3A2 |
|  | Pulse command |  | AM-FM \% |  | J5 pin U | Pulses $\mathrm{L} \rightarrow \mathrm{H}$ | cont. | A3A2 |
|  | FM CAL |  |  |  |  |  |  |  |
|  | Ground J3 pins 29 and 30 and pulse (or momentarily ground) J3 pin 9 . Check |  | D2-8 |  | A3A2U4 pin 1 | L | cont. | A3A2 |
|  |  |  | D2-4 |  | A3A2U4 pin 14 | H | cont. | A3A2 |
|  |  |  | D2-2 |  | A3A2U4 pin 11 | H | cont. | A3A2 |
|  |  |  | D2-1 |  | A3A2U4 pin 8 | L | cont. | A3A2 |
|  | Pulse command |  | FM CAL |  | J5 pin Z | Pulses $\mathrm{L} \rightarrow \mathrm{H}$ | cont. | A3A1 |
|  | RF FCTN |  |  |  |  |  |  |  |
|  | Ground J3 pins 29, 30 and 31 and pulse (or momentarily ground) J3 pin 9 . <br> Check |  | $\begin{aligned} & \text { D2-8 } \\ & \text { D2-4 } \end{aligned}$ |  | $\begin{aligned} & \text { A3A2U4 pin } 1 \\ & \text { A3A2U4 pin } 14 \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | cont. cont. | $\begin{aligned} & \text { A3A2 } \\ & \text { A3A2 } \end{aligned}$ |

Table 8-30. Remote Control Problems (5 of 7)


| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong - Check | Test Point Location | Logic <br> Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
| 4 | Cont'd <br> If the front panel remote indicator is not on and panel controls are functional Pulse J3 pin 9 |  |  |  |  |  |  | A1A1 |
|  | Check |  | CMND T |  | A3A2U1 pin 13 | Pulses <br> $\mathrm{H} \rightarrow \mathrm{L}$ | cont. | A3A2 |
|  |  |  | CMND T |  | A3A11XA11-2 32 | $\begin{aligned} & \text { Pulses } \\ & \mathrm{H} \rightarrow \mathrm{~L} \end{aligned}$ | cont. | A3A1 |
|  | Remove the ground from J3 pin 5. Press STEP $\uparrow$ one time. Ground J3 pin 5 again |  |  |  |  |  |  |  |
|  | Check <br> Pulse J3 pin 9 |  | F3 |  | A1A4XA4-1 A | $\underset{\mathrm{H} \rightarrow \mathrm{~L}}{\mathrm{H}}$ | cont. | A1A2 |
|  | Ground J3 pins 13, 14, 15 and 16 and Pulse J3 pin 9. <br> Check |  | D1-8 |  | A3A1U2 $\operatorname{pin} 1$ | H | cont. |  |
|  |  |  | D1-4 |  | A3A1U2 pin 14 | H | cont. | A3A2 |
|  |  |  | D1-2 |  | A3A1U2 pin 11 | H | cont. | A3A2 |
|  |  |  | D1-1 <br> CMND $p$ |  | A3A1U2 pin 8 | $\mathrm{H}$ | cont. | A3A2 |
|  |  |  |  |  |  |  |  |  |
|  | Pulse J3 pin 9 |  |  |  |  | Pulses $\mathrm{H} \rightarrow \mathrm{~L}$ | cont. | A3A1 |
|  |  |  | F10 |  | A1A4XA4-2 M | L |  |  |
|  | Pulse J3 pin 9 |  |  |  |  | Pulses $\mathrm{L} \rightarrow \mathrm{H}$ | cont. | A1A2 |
|  | Ground J3 pins 28, 29, 30 and 31 and pulse J3 pin 9 |  | D2-8 |  | A3A1U4 pin 1 | H |  |  |
|  |  |  | D2-4 |  | A3A1U4 pin 14 | H | cont. | A3A1 |
|  |  |  | D2-2 |  | A3A1U4 pin 11 | H | cont. | A3A1 |
|  |  |  | D2-1 |  | A3A1U4 pin 8 | H | cont. | A3A1 |
|  | Pulse J3 pin 9 for each of the following checks |  | RMT 8 |  | A1A11XA11-2 24 |  |  | A3A1 |
|  |  |  | RMT 8 |  | A1A11XA11-2 24 | $\begin{aligned} & \text { Pulses } \\ & \mathrm{H} \rightarrow \mathrm{~L} \end{aligned}$ | cont. | A3A1 |
|  |  |  | RMT 4 |  | A1A11XA11-2 27 | Pulses $\mathrm{H} \rightarrow \mathrm{~L}$ | cont. | A3A1 |

Table 8-30. Remote Control Problems (7 of 7)


| Step | Symptom or Instruction | State Succession | Check Instruction | If Next State Wrong Check | Test Point Location | Logic Level | Repair or Replace |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  | If OK | If Wrong |
|  | Check Doubler line |  |  |  | A1A11XA11-1 26 | H | A1A6* | 86603A |
|  | *Check continuity of line to plug-in. |  |  |  |  |  |  |  |

Table 8-32. Output Frequency is Half Indicated Frequency Above 1300 MHz


Table 8-33. Troubleshooting Option 005 Interface Circuits (1 of 2)

| Step | Procedure | Take the following action or proceed to step shown |
| :---: | :---: | :---: |
| 1 | Check the instrument in the LOCAL mode as shown in Section III. | If the instrument does not operate properly proceed to Step 2. If the instrument operates properly proceed to Step 4. |
| 2 | Check LCL/RMT line on A3A2U9 pin 9. | If the level is high refer to the RF Section Troubleshooting. If level is low proceed to Step 3. |
| 3 | Check REN-H at A3XA5 pin 5. | If the level is high A3A2 is defective. If the level is low check the external controller or cabling. |
| 4 | Check +5 V at A3XA4 pin L. | If the voltage is not correct, refer to Table 8-6. If the voltage is correct proceed to Step 5. |
| 5 | Check the 2 MHz input clock on A 3 A 1 . | If the 2 MHz clock is not present refer to the reference section troubleshooting tables. If the clock is present proceed to Step 6. |
| 6 | Check Center Frequency programming for both the mainframe and Plug-in. | If just Plug-in programming is defective, proceed to Step 7. If all programming modes are defective, proceed to Step 8. |
| 7 | Check to see if only Plug-in programming is defective. | If just Plug-in programming is bad proceed to Step 7-a. Otherwise proceed to Step 7-b, then Step 7-c. |
| 7-a | Check PICK-L on A3A1U5 pin 8 for a burst of clock pulses when the Plug-in is addressed. | If the clock pulses are present proceed to Step 7-d. If the clock pulses are not present, trouble is in the DCU. |
| 7-b | If only CF is defective, program a CF and check RMT CF-L at A3A1U4 pin 10. | If RMT CF-L steps low, trouble is in the DCU. If RMT CF-L does not step low, A3A1 is defective. |
| 7-c | If only CF is defective program a CF Step $\uparrow$ and check level at A3A1U4 pin 3. | If Step $\uparrow$ goes low, continue with test. If Step 7-c does not go low, A3A1 is defective. |
|  | Program a CF Step $\downarrow$ and check level at A3A1U4 pin 2. | If Step $\downarrow$ goes low, trouble is in the DCU. If Step 7-c does not go low, trouble is in A3A1 assembly. |
| 7-d | Check the output clocks to the plug-ins. A burst of clock pulses should appear on A3A1U5 pins as listed below: <br> U5 pin 10 - FM CAL <br> U5 pin 13 - AM/FM\% <br> U5 pin $4-$ AM/FM Function <br> U5 pin $1-\mathrm{RF}$ Attenuator | If any of the clocks do not appear verify that programming is correct. <br> If the burst of address pulses does not appear for any function, A 3 A 1 is defective. |
| 8 | If all programming modes are defective, remove the A3A2 assy and check the jumper pins for the following configuration: | If jumper pins are not as shown repair and replace the A3A2 Assy. <br> If the jumper pins are correctly placed proceed to Step 9. |

Table 8-33. Troubleshooting Option 005 Interface Circuits (2 of 2)

| Step | Procedure | Take the following action or proceed to step shown |
| :---: | :---: | :---: |
| 9 | With an external controller enter a correct call-up address. Check A3A2U12 pin 8 MLA-L for correct action (Refer to SS 39). | If the circuit does not function properly, A3A2 is defective. If the circuit functions properly proceed to Step 10. |
| 10 | With an external controller program the 8660 to unlisten. Make the following checks on A3A2U9: $\begin{aligned} & \text { Address } \mathrm{F} / \mathrm{F} \text { pin } 9-\mathrm{H} \\ & \text { pin } 8-\mathrm{L} \\ & \text { Remote } \mathrm{F} / \mathrm{F} \text { pin } 5-\text { RMT-H } \\ & \text { pin } 6-\text { RMT-L } \end{aligned}$ | If the address flip-flop is not functioning properly check A3A2U9 pin 13-H. If A3A2U9 pin 13 is high proceed to Step 10-a, if low, proceed to step 10-b. <br> If checks are OK proceed to Step 11 |
| 10-a | Check A3A2U3 pins 4, 5-H. | If pin 5 is low, A3A1 is defective. |
| 10-b | Same as 10-a. | If the Remote $F / F$ is not functioning properly in Step 10, or if Step $10-\mathrm{a}$ pin 4 is not functioning properly, A3A2 or the EOP-L input from the controller is defective. |
| 11 | Same as Step 10 | If the tests in Step 10 are as shown, check A3A2 U2 pin $6-\mathrm{L}$ and pin 11-H. If either or both checks are bad, proceed to Step 11-a. If both checks are good proceed to Step 11-b. |
| 11-a | Check A3A2U3 pin 3 (ADR-H). It should go high after the Synthesizer address command. | If ADR-H does not go high, A3A2 is defective. |
| 11-b | If Step 11-a checks properly check A3A2U1 pin 3 (INSL-L). It should go high during Synthesizer address and data commands. | If INSL-L does not go high when it should, A3A2 is defective. <br> If INSL-L functions properly, proceed to Step 12. |
| 12 | Check A3A1U9 pin 6 CMDT-L. It should go low during the data transfer address command. | If this point does not switch low, A3A1 is defective. If it does switch low, proceed to Step 12-b. |
| 12-b | Check A3A1U4 pin 10 for the RMT CF-L when $C F$ is addressed and during the transfer command. | If this point does not switch low, A3A1 is defective. If it does switch low, trouble is in the DCU. |

Table 8-34. Troubleshooting the Reference Section (1 of 2)

## Test Equipment Required:

| Oscilloscope (with 10:1 divider probes) | . | . | HP180A/1801A/1821A |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| VLF Comparator | . | . | . | . | . | . | . | HP 117A

## PROCEDURE:

1. Internal Reference Accuracy Adjustment (see Figure 5-3), (allow adequate warmup time).
2. Use the Digital Voltmeter to verify the presence of dc operating voltages at all assemblies before beginning tests. Proceed to next step.
3. Disconnect the REF INPUT cable from A4A2. Use the Spectrum Analyzer and the counter to verify the presence of the reference signal at the cable output ( 10 MHz , at least +5 dBm ).
4. Set the rear panel REFERENCE switch to EXT and apply a 1 Vrms 10 MHz signal to the reference INPUT. Recheck the signal at the end of the cable to the A4A2 assembly.
5. Signal is present - A22 assembly is defective. Order replacement or refer to Service Sheet and repair as necessary.
6. Set the rear panel REFERENCE switch to INT and check the output of the A21 reference oscillator signal is present (check cable to A21) - signal is not present - A21 is defective. Order a replacement unit.
7. Use the Spectrum Analyzer and the Counter to verify the presence of the 100 MHz signal at the A4Q4 100 MHz output. Should be exactly 100 MHz , at least +10 dBm . Amplitude not as specified, A4A4 Assembly is defective. Order replacement assembly or refer to Service Sheet 3 and repair as required.

7-a. Frequency is not as specified. Remove the covers from A4A3 and A4A2. Use an oscilloscope and a Counter to verify the presence of the 20 MHz input to A 4 A 3 . Should be $20 \mathrm{MHz} \pm 1 \mathrm{MHz}$ and at least 300 mV p-p. A4A4 assembly is defective. Order replacement assembly or refer to Service Sheet 3 and repair as required.

7-b. Use an oscilloscope and a counter to verify the presence of the 20 MHz output from the A4A3 assembly. Should be $20 \mathrm{MHz} \pm 1 \mathrm{MHz}$ and at least 2 V p-p - frequency or level is not as specified. A4A3 assembly is defective. Order a replacement assembly or refer to Service Sheet 3 and repair as required.

7-c. Connect the oscilloscope to A4TP1. The oscilloscope should display a 20 nanosecond pulse at least 2V p-p. Pulse is present as specified.

7-d. Use the DVM to check the dc level at the A4A2 "VCO" lead. Voltage should be about +12 to +14 volts. Voltage is as specified.

7-e. Connect the counter to the 20 MHz OUTPUT from the A4A4 assembly. Verify that A4A4C2 can be adjusted to $20 \mathrm{MHz} \pm 5 \mathrm{kHz}$.

## NOTE

If the outputs from the A4A2 assemblies as specified in 7-c, 7-d and 7-e are not as specified, order replacement assemblies or refer to Service Sheet 3 and repair as required.

7-f. Adjustment called for in step 7-e cannot be made as per specifications called for in test 7-e:- A4A4 assembly is defective. Order replacement assembly or refer to Service Sheet 3 and repair as required.

Table 8-34. Troubleshooting the Reference Section (2 of 2)
8-a. If the amplitude and frequency are as specified in test 7 use the Spectrum Analyzer and the Counter to check the 500 MHz output from the A4A4 assembly. Should be exactly 500 MHz and at least +3 dBm .

- Frequency or level is not as specified. A4A4 assembly is defective. Order an A4A4 assembly or refer to Service Sheet 3 and repair as required.

8-b. If the signal is as specified in step 8-a, use the Spectrum Analyzer and the Counter to check the 20 MHz output from the A4A4 assembly. Should be exactly 20 MHz and at a level between -3 and -6 dBm .

8-c. Frequency or level is not as specified. A4A4 assembly is defective. Order a replacement assembly or refer to Service Sheet 3 and repair as required.

8-d. If the signal is as specified use the Oscilloscope to check the 10 MHz output from the A4A4 assembly. Level should be greater than 1.5 V p-p. Use the counter to check the frequency. Frequency should be exactly 10 MHz . If frequency or level is not as specified, A 4 A 3 assembly is defective. Order a replacement assembly or refer to Service Sheet 3 and repair as required.

8-e. If the signal is as specified in 8-d, use the oscilloscope and counter to check the reference outputs from the A4A1 assembly. The $2 \mathrm{MHz}, 400 \mathrm{kHz}$, and both 100 kHz signals should be greater than 2 V p-p.

8-f. Frequency or level is not as specified. Use an oscilloscope to check 10 MHz input to the A 4 A 1 assembly from the A 4 A 3 assembly. Level should be greater than 1.5 V p-p. Signal is not as specified - A4A3 assembly is defective. Order replacement assembly or refer to Service Sheet 4 and repair as required. Signal is defective order replacement assembly or refer to Service Sheet 2 and repair as required.

8-g. All signals from A4A1 assembly are correct. Reference loop is functioning properly.
NOTE
If a malfunction is found and corrected in the Reference Section, perform all of the alignment instructions for the Reference Section which appear in Section V.

Table 8-35. High Frequency Loop Troubleshooting (1 of 3)

Test Equipment Required:
Frequency Counter
Digital Voltmeter
Pulse Generator
Spectrum Analyzer
Signal Generator/Sweeper
Oscilloscope (with 10:1 divider probes)
Logic Analyzer

## NOTE

The HP Analyzer may not be readily available. If it is not, other instruments may be substituted from Table 1-2 at the expense of additional funds and "out-of-service" time.

Table 8-35. High Frequency Loop Troubleshooting (2 of 3)

## PROCEDURE:

1. Check that keyboard digit information is reaching the remote input and the HF Loop input. The MAN TP. should be grounded to enable using a single clock pulse until KDN-H is released. This enables the KDN-H to be held until adequate time has elapsed to complete the specified test.
Use the Spectrum Analyzer and a Counter to verify that the output at the rear (remote) connector of the A4A5 assembly is about +13 to +15 dBm at the frequencies shown.

Center Frequency
Settting in MHz
$\begin{array}{lll}0 & 0 & 0 \\ 0 & 1 & 0\end{array}$
010
020
030
040
050
060
070
080
090
100

## Center Output <br> MHz

450.000000
440.000000
430.000000
420.000000
410.000000
400.000000
390.000000
380.000000
370.000000 , 01000
$360.000000 \quad 01001$
*350.000000 10000

Input Logic Level EDCBA pins 00000 00001 00010 00011 00100 00101 00110 00111
*This frequency not used when RF Section with
$>_{110} \mathrm{MHz}$ maximum Center Frequency is used.

If the frequencies are not correct use the DVM to check the logic levels at the A4A6 "A", " $B$ ", " $C$ ", " $D$ " and " $E$ " inputs. For frequencies shown in this Table logic levels should be as shown in the level column. $1=$ high, about +3 V .
2. All frequencies and levels are as specified. HF Loop is functioning properly.
3. Output is low or there is no output. A4A5 is defective. Order replacement assembly or refer to Service Sheet 3 and repair as required.
4. Input logic levels are not as specified. Check interconnections to the interface circuit. If connections are good, trouble is in the interface circuits of the DCU. Refer to Table 8-8.
5. Levels are as specified in test 1 but frequencies are not. Use the Oscilloscope and Counter to check the 10 MHz input to the A4A7 assembly. Should be greater than $1-5 \mathrm{~V}$ p-p. If all frequencies and levels are as specified in Test 1 the HP Loop circuits are functioning properly. Proceed to Table 8-35.
6. If frequencies or levels are not as specified, trouble is in the Reference Section or cable A4W2. Check the cable, then return to the beginning of this test. If the cable is good, recheck the Reference Section.
7. If frequency and level is as specified, open the HF phase lock loop by removing the cable from the A4A5 $350-450 \mathrm{MHz}$ VCO OUTPUT. Use the Oscilloscope or the DVM to check the dc level on the lead marked $\emptyset$ between the A4A6 and A4A7 assemblies, the level should be $0 \mathrm{~V} \pm 0.1 \mathrm{~V}$. If the de level is not as specified, the A4A7 assembly is defective. Order a replacement assembly or refer to Service Sheet 5 and repair as required.
8. If dc level is as specified, refer to the first step in the HF Loop procedure and repeat the frequency portion of the test. Frequencies shown should be within $\pm 500 \mathrm{kHz}$. If the frequencies are not as specified, use the DVM to check the dc on the lead marked "freq" between the A4A5 and A4A6 assemblies. With

Table 8-35. High Frequency Loop Troubleshooting (3 of 3)
center frequencies at 0 MHz reading should be -34 Vdc . At 100 MHz it should be approximately -7 Vdc . If levels are not as specified, refer to Section $V$ and perform the adjustment procedure.

8-a. If the adjustment procedure does not correct the problem, use the DVM to measure the lead "comp" in the A4A6 assembly. Should be about -37 V to -38 V .

8-b. If the levels are correct from test 8 or the voltage is not as specified in $8-\mathrm{a}$, the A4A5 assembly is defective. Order a replacement assembly or refer to Service Sheet 6 and repair as required.

8-c. If the voltage is as specified in 8-a the A4A6 assembly is defective. Order a replacement assembly or refer to Service Sheet 4 and repair as required.
9. Frequencies are as specified in test 8. Close the HF Loop by reconnecting the cable between the A4A6 and A4A7 assemblies. Use the Oscilloscope to check 2 to 3 V p-p beat note at the lead labeled $\emptyset$ on the A4A7 assembly.

## NOTE

The beat frequency depends on how far the high frequency is out of lock.

9-a. The beat note is present. The A4A6 assembly is defective. Order a replacement assembly or refer to Service Sheet 5 and repair as required.

9-b. The beat note is present. The A4A7 assembly is defective. Order a replacement assembly or refer to Service Sheet 5 and repair as required.

## NOTE

If repairs are required in any portion of the HF Loop perform the adjustment procedures outlined in Section V of this manual.

## NOTES

1. The following five troubleshooting tables are arranged in the sequence of the output to the RF Section back to the inputs from the Reference Section. These Loops are commonly referred to as the LF (Low Frequency) Loops; all are physically mounted on the A2 Mother Board Assembly.
2. Since some of these notes are used in several places, they appear in Table 8-39 to avoid repetition.
3. Locations of the assemblies within these loops are shown in Figure 8-114.

Table 8-36. Summing Loop 1 Troubleshooting

| Reference: Service Sheets 15,16 and 17. <br> Test Equipment Required (from Table 1-2): <br> Digital Voltmeter <br> Oscilloscope (with 10:1 probes) <br> Frequency Counter |  |  |
| :---: | :---: | :---: |
| Step | Procedure | Take the following action or proceed to step shown |
| 1 | Use the Oscilloscope and the Frequency Counter to check the N1 output at A2XA17-1 pin 2. Level should be greater than 0.4 V p-p. For formula to calculate frequency see Note 5 of Table 8-39. | If the frequency is not as specified see Note 2 of Table 8-39 and proceed to Step 2. If the frequency and level are as specified, proceed to Step 3. |
| 2 | Proceed to Table 8-38 N1 Loop Troubleshooting. | Perform tests shown in Table 8-38. |
| 3 | Use the plug provided to ground A2TP14. Use the Frequency Counter to check the SL1 output at A2TP22. | See Note 6 of Table 8-39 to calculate frequency output. Frequency should be as calculated, $\pm 150 \mathrm{kHz}$. If frequency is not as calculated, proceed to Step 4 (also see Note 2 of Table 8-39). If frequency is as calculated, proceed to Step 5. |
| 4 | Use the DVM to check the dc levels at A2XA18-2 pin R. The level is controlled by digits 5,6 and 7 . With the digits set to 000 , the level should be -25.5 V (typical). With the digits set to 999 , the level should be about -5.4 V . Intermediate steps should be about .02 V . | If the level is not as specified the A18 assembly is defective. Order a replacement assembly or refer to Service Sheet 16 and repair as required. If the levels are as specified the A19 assembly is defective. Order a replacement or refer to Service Sheet 16 and repair as required. |
| 5 | Use the Frequency Counter to check the frequency at A2XA19-1 pin 2. The frequency should be as calculated for Step 3. | If frequency is not as calculated the A19 assembly is defective. Order a replacement or refer to Service Sheet 17 and repair as required. If the frequency is correct, proceed to Step 6. |
| 6 | Use the Frequency Counter to check the frequency at A2TP19. The frequency should be the difference frequency between the N1 and SL1 outputs. If the frequency is as specified, trouble is in the Frequency Extension Module or the RF Section. | If the frequency is not as specified the A18 assembly is defective. Order a replacement or refer to Service Sheet 16 and repair as required. If the frequency is as specified, the A15 assembly is defective. Order a replacement or refer to Service Sheet 15 and repair as required. |

Table 8-37. Summing Loop 2 Troubleshooting

| Reference: Service Sheets 13 and 14 <br> Test Equipment Required (from Table 1-2): <br> Oscilloscope (with 10:1 probes) <br> Frequency Counter |  |  |
| :---: | :---: | :---: |
| Step | Procedure | Take the following action or proceed to step shown |
| 1 | Use the Oscilloscope and the Frequency Counter to check the SL2 output at A2TP6. Level should be greater than 1 V p-p. For the formula to calculate frequency see Note 1 of Table 8-39. | If the frequency and level are as specified, recheck Summing Loop 1 (Table 8-34). If the frequency and level are correct proceed to Step 2. |
| 2 | Use the Oscilloscope and the Frequency Counter to check the N2 output at A2XA13-1 pin 4. Level should be greater than 275 mV p-p. Refer to Note 3 of Table 8-39 for formula to calculate frequency. | If the frequency and level are not as specified, proceed to the N2 Loop Troubleshooting, Table 8-37. If the frequency and level are as specified, proceed to Step 3. |
| 3 | Use the Oscilloscope and the Frequency Counter to check the N3 output at A2XA8-1 pin 4. Level should be greater than 2 V p-p. Refer to note 4 of Table 8-39 for formula to calculate frequency. | If the frequency and level are not as specified, proceed to the N3 Loop Troubleshooting, Table 8-38. If the frequency and level are as specified proceed to Step 4. |
| 4 | Use the plug provided to ground A2TP8. Use the Frequency Counter to check the SL2 output at A2XA11-1 pin 2. Refer to Note 1 of Table 8-39 for formula to calculate frequency. Should be $\pm 150 \mathrm{kHz}$. | If the frequency is as specified the A12 assembly is defective. Order a replacement assembly or refer to Service Sheet 13 and repair as required. If the frequency is not correct proceed to Step 5. |
| 5 | Use the Frequency Counter to check the output at A2TP6. | If the frequency is as specified in Step 4 the A11 assembly is defective. <br> If the frequency is not as specified in Step 4 proceed to Step 6. |
| 6 | Remove the A12 assembly and repeat the test. The frequency should be the same as that calculated for Step 4. | If the frequency is as specified the A12 assembly is defective. Order a replacement assembly or refer to Service Sheet 13 and repair as required. If the frequency is not as specified the A11 assembly is defective. Order a replacement assembly or refer to Service Sheet 14 and repair as required. |


| Reference: Service Sheets 11 and 12. <br> Test Equipment Required (from Table 1-2): <br> Oscilloscope (with $10: 1$ probes) <br> Frequency Counter |  |  |
| :---: | :---: | :---: |
| Step | Procedure | Take the following action or proceed to step shown |
| 1 | Use the Oscilloscope and the Frequency Counter to check the N3 output at A2XA8-1 pin 6 . The level should be greater than 0.5 V p-p. Frequency should be the same as that in Table 8-35 $\times 10$. | If the frequency and level are as specified, the A8 assembly is defective. Order a new assembly or refer to Service Sheet 12 and repair as required. If the frequency is not as specified, proceed to step 2. |
| 2 | Use the plug provided to ground A2TP4. Use Frequency Counter to check the frequency at A2XA8-1 pin 6 . The frequency should be the same as Step $1 \pm 250 \mathrm{kHz}$. Remove the ground plug. | If the frequency is not as specified the A8 assembly is defective. Order a replacement or refer to Service Sheet 12 and repair as required. If the frequency is as specified proceed to Step 3. |
| 3 | Use the Oscilloscope and the Frequency Counter to check the 100 kHz input at A2XA10-1 pin 2. The signal should be exactly 100 kHz at about 2.5 V p-p. | If the frequency is not as specified check the interconnection to the reference section. If the frequency is as specified the A10 assembly is defective. Order a replacement assembly or refer to Service Sheet 11 and repair as required. |

Table 8-39. N2 Loop Troubleshooting (1 of 2)

| Reference: Service Sheets 9 and 10. <br> Test Equipment Required (from Table 1-2): <br> Oscilloscope (with 10:1 probes) <br> Frequency Counter |  |  |
| :---: | :--- | :--- |
| Step | Procedure | Take the following action or proceed to step shown |
| 1 | If the frequency was not as specified in Step 2 <br> of Table 8-35 use the plug provided to ground <br> A2TP12 and use the Frequency Counter to <br> check the N2 output at A2XA13-1 pin 4. <br> The frequency should be as specified in the <br> step shown above $\pm 250$ kHz. | If the frequency is not as specified the A13 assembly is <br> defective. Order a replacement assembly or refer to <br> Service Sheet 10 and repair as required. If the frequency <br> is as specified proceed to Step 2. |
| 2 | Use the Oscilloscope and the Frequency Counter <br> to check the frequency and level at A2XA13-1 <br> pin 6. The frequency should be as shown for <br> step 1. The level should be about 0.4V p-p. | If the frequency is not as specified the A13 assembly is <br> defective. Order a replacement assembly or refer to <br> Service Sheet 10 and repair as required. If the frequency <br> is as specified proceed to Step 3. |

Table 8-39. N2 Loop Troubleshooting (2 of 2)

| Step | Procedure | Take the following action or proceed to step shown |
| :---: | :--- | :--- |
| 3 | Use the Oscilloscope and the Frequency <br> Counter to check the frequency and level <br> at A2XA14-1 pin 2. The frequency <br> should be exactly 100 kHz and the level <br> should be about 2 V p-p. | If the frequency is not as specified check the inter- <br> connection wiring to the reference section. If the <br> frequency and level are as specified the A14 assembly <br> is defective. Order a new assembly or refer to Service <br> Sheet 9 and repair as required. |

Table 8-40. N1 Loop Troubleshooting
Reference: Service Sheets 7 and 8.
Test Equipment Required (from Table 1-2):
Oscilloscope (with 10:1 probes)
Frequency Counter

| Step | Procedure | Take the following action or proceed to step shown |
| :---: | :---: | :---: |
| 1 | If the frequency was not as calculated in Step 1 of Table 8-34 use the Frequency Counter to check the output at A2XA17-1 pin 2. Frequency should be as calculated in Step 1 of Table 8-34 $\pm 250 \mathrm{kHz}$. | If the frequency is not as specified the A17 assembly is defective. Order a replacement assembly or refer to Service Sheet 8 and repair as required. If the frequency is correct proceed to Step 2. |
| 2 | Use the Frequency Counter to check the frequency at A2XA17-1 pin D. Should be the same as calculated for Step 1. | If frequency is not as specified the A17 assembly is defective. Order a replacement assembly or refer to Service Sheet 8 and repair as required. If the frequency is as specified proceed to Step 3. |
| 3 | Use the Oscilloscope and the Frequency Counter to check the input at A2XA16-1 pin 2 . The input should be exactly 400 kHz at about 2.5 V p-p. | If the frequency is not as specified check the interconnection wiring to the reference section. If the signal is as specified the A16 assembly is defective. Order a replacement assembly or refer to Service Sheet 7 and repair as required. |

Table 8-41. Low Frequency Loops Notes (1 of 2)

1. The output frequency of the SL2 loop may be determined by adding the N2 output frequency to the divider-by-ten output of the N3 loop assembly. EXAMPLE: Programmed frequency is $107.654321 \mathrm{MHz} .24 .36+$ $0.2079=24.5679$. Output frequency is 24.5679 MHz .
2. If there is no RF output, or if the RF level is low, the trouble is in the circuit board containing the voltage controlled oscillator and output circuits.
3. The output frequency of the N 2 loop is equal to 29.79 MHz less the setting of center frequency digits 5,4 , and 3. EXAMPLE: center frequency set to $107.654321 \mathrm{MHz}, 29.79-5.43=24.36$. Output frequency is 24.36 MHz .

Table 8-41. Low Frequency Loops Notes (2 of 2)
4. The output frequency of the N 3 loop is equal to 2.100 MHz less the setting of center frequency digits 2 and 1. EXAMPLE: center frequency set to $107.654321 \mathrm{MHz}(2.100-.021=2.079)$. Output frequency is 2.079 MHz .
5. The output frequency of the N 1 loop is equal to 29.7 MHz less the setting of center frequency digits 7 and 6. EXAMPLE: center frequency set to $107.654321 \mathrm{MHz}, 29.7-7.6=22.1$. Output frequency is 22.1 MHz .
6. The output frequency of the SL1 loop may be determined by subtracting the last seven digits of the programmed frequency from $30.000000-7.654321=22.345679$. Output frequency is 22.345679 MHz .

Table 8-42. Index to Assembly Illustrations (1 of 2)

| Assy No. | Description | SS No. | (Photo) Fig. 8- |
| :---: | :---: | :---: | :---: |
| A1 | Digital Control Unit | 18 thru 36 | 50, 114 |
| A1A1 | P/O Switch Control Assy (1 of 2) | 19 | 52 |
| A1A1 | P/O Switch Control Assy (2 of 2) | 20 | 54 |
| A1A2 | P/O Key Control Assy (1 of 2) | 21 | 58 |
| A1A2 | P/O Key Control Assy (2 of 2) | 22 | 60 |
| A1A3 | P/O Readout Control Assy (1 of 2) | 23 | 62 |
| A1 A3 | P/O Readout Control Assy (2 of 2) | 24 | 64 |
| A1A4 | P/O ROM Input Assy (1 of 2) | 25 | 66 |
| A1A4 | P/O ROM Input Assy (2 of 2) | 26 | 68 |
| A1A5 | P/O ROM Output Assy (1 of 2) | 27 | 70 |
| A1 A5 | P/O ROM Output Assy (2 of 2) | 28 | 72 |
| A1A6 | P/O Register Assy (1 of 3) | 29 | 74 |
| A1A6 | P/O Register Assy (2 of 3) | 30 | 76 |
| A1A6 | P/O Register Assy (3 of 3) | 31 | 78 |
| A1A7 | Arithmetic Logic Unit | 32 | 80 |
| A1A8 | Sweep Count Assy | 33 | 82 |
| A1 A9 | A Register Assy | 34 | 84 |
| A1 A10 | Output Register Assy | 35 | 86 |
| A1 A11 | DCU Mother Board |  | 110 |
| A1 A12 | Numeric Readout Assy | 36 | 80 |
| A1 A13 | Board Assy Annunciator Block | Various | 107 |
| A1A14 | Switch Assy Sweep | Various |  |
| A1A15 | Switch Assy Keyboard | 21 | 56,57 |
| A1A16 | Switch Assy Manual Mode | 20 |  |
| A1A17 | Tuner Assy Manual Mode | 20 |  |
| A2 | Board Assy Interconnection | - | 108,109 |

Table 8-42. Index to Assembly Illustrations (2 of 2)

| Assy No. | Description | SS No. | (Photo) Fig. 8- |
| :---: | :---: | :---: | :---: |
| A3 | Interface Assy | 41 | 114 |
| A3A1 | Front Interface Assy | 37, 41 | 92,98 |
| A3A2 | Read Interface Assy | 38, 41 | 94, 96 |
| A4 | Loop Assy RF | 2, 3, 4, 5, 6 | $2,3,4,5,6 \text {, }$ |
| A4A1 | Reference Divider Assy | 2 | 13 |
| A4A2 | Reference Phase Detector | 2 | 12 |
| A4A3 | Reference Divide-by-Two | 3 | 16 |
| A4A4 | Reference VCO Assy | 3 | 15 |
| A4A5 | VCO and Amplifiers | 6 | 22 |
| A4A6 | Pretuning Assy | 4 | 18 |
| A4A7 | Phase Detector Assy | 5 | 20 |
| A5 | Board Assy Rectifier | 41 | 103 |
| A6 | Fan Assy, 400 Hz (Opt. 003) | - | 100 |
| A6 | Fan Assy, 60 Hz STD | - | 100 |
| A6A1 | Pre-Regulator Assy | 41 | 101, 102 |
| A7 | Power Line Module/Filter | 41 | 114 |
| A8 | N3 Oscillator Assy (except Opt 004) | 12 | 38 |
| A9 | Cable Assy Loop Box | 42 | 114, 111 |
| A10 | N3 Phase Detector | 11 | 36 |
| A11 | SL2 Oscillator Assy | 14 | 42 |
| A12 | SL2 Detector | 13 | 40 |
| A13 | N2 Oscillator | 10 | 34 |
| A14 | N2 Phase Detector | 9, 9a | 30, 32 |
| A15 | SL1 Detector | 15 | 44 |
| A16 | N1 Phase Detector | 7 | 26 |
| A17 | N1 Oscillator | 8 | 28 |
| A18 | SL1 Mixer | 16 | 46 |
| A19 | SL1 Oscillator | 17 | 48 |
| A20 | Rectifier Assy | 41 | 104 |
| A21 | Crystal Oscillator | 2 | 10 |
| A22 | Switch Assy Reference | 2 | 11 |
| A23 | Wiring Harness | Various | 114 |

## 8-87. PRINCIPLES OF OPERATION

$8-88$. The following discussion illustrates the basic principles of operation of the Model 8660 System. More detailed information about principles of operation for the phase lock loops and the Digital Control Unit appears on Service Sheets 1 and 18 respectively. In addition, detailed information to the circuit level is provided on individual Service Sheets.

8-89. General. The Model 8660 was designed to provide precise digitally controlled output frequencies utilizing indirect synthesizer techniques. Unlike conventional signal generators, the output frequency is not $\pm$ some percentage factor: the output frequency of the Model 8660 is exactly that selected (the only factor which must be considered here is the accuracy and stability of the reference source). The output frequency range is determined by the RF Section plug-in being used.

8-90. All of the phase lock loops are phase locked, directly or indirectly, to a very stable temperature controlled internal 10 MHz source or to an external reference source. (The term "indirect synthesis" as used in paragraph 8-89 refers to a synthesizer that derives all frequencies from a single source, as opposed to a "direct synthesizer" which uses different crystal oscillators for each frequency generated.)

8-91. Reference Section. A 100 MHz voltage controlled óscillator which is phase locked to an internal reference, or to an external reference source, serves as a master oscillator. The internal reference is a 10 MHz standard temperature controlled crystal oscillator. The external reference source may be 4 or 10 MHz at 0.2 to 2 V rms. All of the outputs from the reference section are derived from the 100 MHz master oscillator.

8-92. The reference section provides the following outputs:
a. $\quad 500 \mathrm{MHz}$ to the RF Output Section.
b. 100 MHz to the RF Output Section. This 100 MHz is coupled out of the RF Section for use in other circuits.
c. 20 MHz to the Modulator Section. This 20 MHz is coupled out of the Modulator Section for use in the RF Section and the Frequency Extension Module.
d. 10 MHz to the High Frequency Loop phase detector for use as a reference signal.
e. 2 MHz to the Digital Control Unit to be used as a clock.
f. 400 kHz to the N 1 loop for a reference signal.
g. Separate 100 kHz signals to the N 2 and N3 loops for reference signals.

## NOTE

In the following discussion the terms digit 1, digit 2, through digit 10 are used to refer to the 10 digits of frequency selection. Digit 1 refers to the least significant digit ( 1 Hz increments). Digit numbers progress from right to left until digit 10 refers to the most significant digit ( 1 GHz increments).

8-93. High Frequency Loop. The HF loop contains a voltage controlled oscillator which provides eleven discrete outputs between 350 and 450 MHz in 10 MHz increments when the Model 86601A RF Section is used. When other RF Sections are used the output of the HF loop will still step in 10 MHz increments, but there will be more than, or less than, eleven steps.

8-94. Pretuning tunes the voltage controlled oscillator to a point within the capture range of the phase lock loop and the phase detector then causes the loop to be phase locked to the 10 MHz reference signal at the exact frequency selected.
$8-95$. When a 0.01 to 110 MHz RF Section such as the HP Model 86601A is used, the output of the HF loop is applied to the RF Section. When a higher frequency RF Section is used, the output of the HF loop is applied to the Frequency Extension Module.

8-96. N1 Phase Lock Loop. The N1 loop provides an output to Summing Loop 1 (SL1) that is between 19.8 and 29.7 MHz in 100 kHz steps. The N 1 voltage controlled oscillator is roughly pretuned by a digital to analog converter which is controlled by digits 6 and 7 .

8-97. The N 1 sampling phase detector is driven by pulses derived from the N1 voltage controlled oscillator through a programmable divider and a pulse shaper. The programmable divider is con-
trolled by digits 6 and 7. When the loop is phase locked the 400 kHz reference input is sampled at a 100 kHz rate. The error voltage from the phase detector is summed with the digital to analog converter output to precisely control the voltage controlled oscillator frequency.

## NOTE

In Option 004 instruments the N2A programmable divider is used. The N2 loop output is then between 20.01 and 30.00 MHz .

8-98. N2 Phase Lock Loop. The N2 loop provides an output to Summing Loop 2 (SL2) that is between 19.80 and 29.79 MHz in 10 kHz steps. The N2 voltage controlled oscillator is roughly pretuned by a digital to analog converter which is controlled by digits 4 and 5 .

8-99. The N2 sampling phase detector is driven by pulses derived from the N2 voltage controlled oscillator through a programmable divider and a pulse shaper. The programmable divider is controlled by digits 3,4 , and 5 . When the loop is phase locked the 100 kHz reference signal input is sampled at a 10 kHz rate. The error voltage from the phase detector is summed with the digital to analog converter output to precisely control the voltage controlled oscillator.

8-100. N3 Phase Lock Loop. The N3 loop provides an output to Summing Loop 2 (SL2) that is between 2.001 and 2.100 MHz in 1 kHz steps. The N3 voltage controlled oscillator is roughly pretuned by a digital to analog converter which is controlled by digit 2 .
$8-101$. The N3 sampling phase detector is driven by pulses derived from the N3 voltage controlled oscillator through a programmable divider and a pulse shaper. The programmable divider is controlled by digits 1 and 2 . When the loop is phase locked the 100 kHz reference signal is sampled at a 10 kHz rate. The error voltage from the phase detector is summed with the digital to analog converter output to precisely control the voltage controlled oscillator frequency.

## NOTE

In Option 004 instruments Summing Loop 2 (SL2) is not used.

8-102. Summing Loop 2. SL2 provides an output to SL1 that is between 20.0001 and 30.0000 MHz
in 100 Hz steps. The SL2 voltage controlled oscillator is roughly pretuned by a digital-to-analog converter which is controlled by digits 3,4 , and 5 .

8-103. The output from the SL2 voltage controlled oscillator is also applied to a mixer where it is mixed with the output of the N2 loop. The output of this mixer is applied to one input of a digital phase detector through a pulse shaper. The other input to the digital phase detector is the divided by ten output of the N3 loop assembly in pulse form. When SL2 is phase locked the frequency ratio of the two inputs to the phase detector is always $1: 1$; the mixer output frequency must exactly match the divided by ten output of the N2 loop assembly (the pulses are received altemately).

## NOTE

In Option 004 instruments the Summing Loop 1 output is from 20.0001 to 30 MHz .

8-104. Summing Loop 1. SL1 provides an output to the RF Section that is between 20.000001 and 30 MHz in 1 Hz steps. The SL1 voltage controlled oscillator is roughly pretuned by a digital to analog converter which is controlled by digits 5,6 , and 7 .

8-105. The output from the SL1 voltage controlled oscillator is also applied to a mixer where it is mixed with the output of the N1 loop. The output of this mixer is applied to one input of a digital phase detector through a pulse shaper. The other input to the digital phase detector is the divided-by-one hundred output of the SL2 voltage controlled oscillator in pulse form. When SL2 is phase locked the frequency ratio of the two inputs to the phase detector is $1: 1$; the mixer output frequency must exactly match the divided by one hundred output of the SL2 voltage controlled oscillator (the pulses are received alternately).

8-106. Digital Control Unit (DCU). In the local mode all functions of the Model 8660 are controlled by the DCU. These functions are itemized and described in Section III of this manual.

8-107. Interface Circuits. The interface circuits provide the capability of operating the Model 8660 with the front panel controls (local mode), or by a remote programming device via a rear panel connector (remote mode).

8-108. RF Section. An RF Section plug-in is required to produce a useable rf output. Figure $8-11$ shows a block diagram of the Model 8660 . All plug-in sections are covered by separate manuals.

8-109. Modulation Section. If a modulation section is not available, it will be necessary to have an auxiliary section in the modulator compartment to complete necessary connections.

## INTEGRATED CIRCUITS ( PLASTIC AND METAL CASE )

24 PIN


14 PIN
DUAL-IN-LINE


16 PIN
DUAL IN-LINE


OR TO-99

Figure 8-7. Integrated Circuit Packaging

Table 8-43. 8660 System

|  | Mainframes |
| :--- | :--- |
| 8660 A |  |
| $8660 \mathrm{~B} / \mathrm{C}$ |  |$\quad$| Thumbwheel Frequency Control - Fully Programmable |
| :--- |
| Keyboard Frequency Control - Fully Programmable |



## SERVICE SHEET 1

## BLOCK DIAGRAM

## General

The Hewlett-Packard Model 8660 C is a signal generator which tilizes synthesizer techniques to produce precise RF output signals. These signals may be selected in increments as small as one Hz .

Each step in the generation of the output frequency is controlled by phase lock loops. This ensures that the output frequency is exactly that selected by front panel (or remote) controls.

All of the seven phase lock loops (five loops in option 004) are referenced to a single source. This source may be the internal temperature controlled crystal oscillator or an external frequency standard of 5 or 10 MHz .

The Model 8660C mainframe does not provide a direct RF output, except for the reference signal which may be used as a time base for xed in plug-in modules which generated within the mainframe are the selected output RF signals.

## Reference Loop

The reference loop consists of four circuit boards mounted in the A4 assembly. Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided by Service Sheets 2 and 3

All of the signals generated within the Model 8660C mainframe are derived from the 100 MHz master oscillator in the reference loop. The master oscillator is a voltage controlled oscillator which is phase The 100 MHz oscillator is located in the A4A4 assembly

Also included in the A4A4 assembly are divide-by-five and multiply-by-five circuits. The outputs from the A4A4 assembly are $500 \mathrm{MHz}, 100 \mathrm{MHz}$, and 20 MHz . The 20 MHz output from the A4A4 assembly is sampled in the reference loop phase detector to provide a phase correction signal to the master oscillator. The 20 MHz signal is also applied to the A4A3 assembly where it is divided dividers and in the high frequency phase lock loop.

The reference loop input circuit (A4A2) converts the signal from the eference oscillator into sharp short-duration pulses to open a sampler gate which samples the 20 MHz signal from the A4A4 assembly. The sampled signal is used to generate anterror signal which biases the varactor in the 100 MHz voltage controlled oscillator in the A4A4 assembly to maintain the phase locked condition.

The A4A1 assembly divides the 10 MHz input from the A4A3 assembly by five to provide a 2 MHz clock for the digital control unit. The 2 MHz signal is divided by five to provide a 400 kHz signal to the phase detector in the N 1 loop. The 400 kHz is twice divided by two to provide 100 kHz signals to the phase detectors in the N2 and N3 loops.

## High Frequency Loop

The HF loop consists of three circuit boards mounted in the A4 assembly. Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided by Service Sheets 4, 5 and 6.

The HF loop provides digitally controlled RF signals between 350 and 450 MHz in precisely selected 10 MHz increments.

The sampling phase detector (A4A7) compares the voltage controlled oscillator (A4A5) output to a 10 MHz signal from the reference loop and provides an output to phase lock the voltage controlled oscillator to generator a sampler and a signal processing circuit.

The frequency of the voltage controlled oscillator (A4A5) is roughly pretuned by a digital to analog converter located in the A4A6 assembly. The error signal from the A4A7 assembly is summed with the output of the digital to analog converter to maintain the phase locked condition. The A4A5 assembly also contains two identical three-stage amplifiers. These amplifiers serve as buffers to isolate any extraneous signals at their outputs from the oscillator. One of the amplifiers provides an output to the RF plug-in; the other output goes to the HF loop sampling phase detector.

The A4A6 pretuning circuit consists of a digital to analog converter which roughly pretunes the voltage controlled oscillator to the 10 MHz increment between 350 and 450 MHz selected by CF digits 8 and 9 of the front panel (or remote) controls. The pretuning cannot, by itself, set the voltage controlled oscillator frequency accurately; it does set the frequency within the capture range of the loop.

The A4A6 assembly also contains a summing circuit which sums the negative dc level from the digital to analog converter with the current from a +20 volt source and the output of the phase detector. The the voltage controlled oscillator.

## Divide By N Loop N1

The purpose of the N 1 loop is to generate digitally controlled RF signals in the range of 19.8 to 29.7 MHz in selectable 100 kHz increments. The voltage controlled oscillator is phase locked to a 400
kHz reference signal which is derived from the master oscillator in the reference loop. The output of the N1 loop is applied to summing loop 1.

The N1 loop circuits are mounted on two circuit boards, A16 and A17. Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided by Service Sheets 7 and 8.

The A16 phase detector assembly contains a programmable divider, a sampling phase detector and a signal processing circuit

The programmable divider divides by a number determined by CF digits 6 and 7 of the front panel (or remote) controls. The terminal count of the programmable divider is always 297 . The actual number of cycles counted is determined by the count programmed into the
divider prior to the start of each count cycle. The output of the programmable divider is always 100 kHz when the loop is locked

The output frequency of the N1 loop may be determined by subtracting the CF digits 7 and 6 information from 29.7 MHz . As an example, if CF digits 7 and 6 are set for 3.4 MHz , the N1 output frequency will be 26.3 MHz (29.7-3.4).

The sampling phase detector uses the 100 kHz pulses from the programmable divider to sample the 400 kHz reference signal and provides an error output to the summing circuit in the A17 assembly.

The signal processing circuit consists of an operational amplifier with lead and lag compensation.

The A17 assembly contains a digital to analog converter, a voltage controlled oscillator and a summing circuit.
The digital to analog converter converts the digital inputs from CF digits 6 and 7 to a dc level which roughly pretunes the voltage controlled oscillator to a frequency within the capture range of the loop.

The summing circuit sums the current from the negative digital to analog converter source with current from a +20 volt source and the error signal from the phase detector to precisely control the voltage controlled oscillator frequency

## Divide By N Loop N2

The purpose of the N2 loop is to generate digitally controlled RF signals in the range of 19.80 to 29.79 MHz in selected 10 kHz increments.

## NOTE

In option 004 instruments the N2 loop output is from 20.01 to 30.00 MHz in 10 kHz increments.

The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section. The output of the N2 loop is applied to summing loop 2 (summing loop 1 in option 004 instrument)

## SERVICE SHEET 1 (Cont'd)

kHz reference signal which is derived from the master oscillator in the reference loop. The output of the N1 loop is applied to summing loop 1
The N1 loop circuits are mounted on two circuit boards, A16 and A17. Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided by Service Sheets 7 and 8.
The A16 phase detector assembly contains a programmable divider, a sampling phase detector and a signal processing circuit.

The programmable divider divides by a number determined by CF digits 6 and 7 of the front panel (or remote) controls. The terminal count of the programmable divider is always 297. The actual number of cycles counted is determined by the count programmed into the divider prior to the start of each count cycle. The output of the programmable divider is always 100 kHz when the loop is locked.
The output frequency of the N 1 loop may be determined by subtracting the CF digits 7 and 6 information from 29.7 MHz . As an example, if CF digits 7 and 6 are set for 3.4 MHz , the N1 output frequency will be 26.3 MHz (29.7-3.4).
The sampling phase detector uses the 100 kHz pulses from the programmable divider to sample the 400 kHz reference signal and provides an error output to the summing circuit in the A17 assembly.
The signal processing circuit consists of an operational amplifier with lead and lag compensation.
The A17 assembly contains a digital to analog converter, a voltage controlled oscillator and a summing circuit.

The digital to analog converter converts the digital inputs from CF digits 6 and 7 to a dc level which roughly pretunes the voltage controlled oscillator to a frequency within the capture range of the loop.

The summing circuit sums the current from the negative digital to analog converter source with current from a +20 volt source and the error signal from the phase detector to precisely control the voltage controlled oscillator frequency.

## Divide By N Loop N2

The purpose of the N 2 loop is to generate digitally controlled RF signals in the range of 19.80 to 29.79 MHz in selected 10 kHz increments.

## NOTE

In option 004 instruments the N2 loop output is from 20.01 to 30.00 MHz in 10 kHz increments.

The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section. The output of the N2 loop is applied to summing loop 2 (summing loop 1 in option 004 instrument).

## SERVICE SHEET 1 (Cont'd)

The N2 loop circuits are mounted on two circuit boards, A13 and A14. Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided by Service Sheets 9 (9A for option 004 instruments) and 10.
Operation of the N2 loop is virtually the same as operation of the N1 loop. The reference input is 100 kHz and the output of the programmable divider is always 10 kHz when the loop is locked. The digital inputs are from CF digits 3,4 and 5 (or remote controls) and range from 000 to 999 .

The programmable divider count always terminates in a count of 2979 ( 3000 in option 004 instruments). The output frequency in MHz of the oscillator may be calculated by subtracting the programmed digital input from CF digits 5, 4 and 3 from 2979 ( 3000 for option 004 instruments) and dividing the results by 100 . Example: with CF digits 5, 4 and 3 set to 222 the output frequency will be $27.57 \mathrm{MHz}\left(\frac{2979-222}{100}\right)$. (Option $004 \frac{3000-222}{100}=27.78 \mathrm{MHz}$.)

## Divide By N Loop N3

## NOTE

The N3 loop is not included in option 004 instruments.

The purpose of the N3 loop is to generate digitally controlled RF signals in the range of 20.01 to 21.00 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section. The output from the N 3 phase lock loop is divided by ten and the resulting 2.001 to 2.100 MHz ( 1 kHz steps) signal is applied to summing loop 2 .

The N3 loop circuit is mounted on 2 circuit boards, A8 and A10 Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided by Service Sheets 11 and 12.

Operation of the N3 loop is virtually identical to operation of the N1 and N2 loops. The reference signal is 100 kHz and the output of the programmable divider is always 10 kHz when the loop is phase locked. The digital inputs are from CF digits 1 and 2, and range from 00 to 99 .

The programmable divider count always terminates in a count of 2100. The output frequency in MHz of the voltage controlled oscillator may be calculated by subtracting the programmed digital input from CF digits 2 and 1 from 2100 and dividing the result by 100. Example; with CF digits 2 and 1 set to 34 , the output frequency of the voltage controlled oscillator will be 20.66 MHz $\left(\frac{2100-34}{100}\right)$. Since the voltage controlled oscillator output is divided by 10 , the output to summing loop 2 will be 2.066 MHz .

## SERVICE SHEET 1 (Cont'd)

## Summing Loop 2

## NOTE

Summing Loop 2 is not included in option 004 instruments.

The purpose of SL2 is to generate digitally controlled RF signals in the range of 20.0001 to 30.0000 MHz in selectable 100 Hz increments. The output frequency of the SL2 voltage controlled oscillator is equal to the sum of the N2 output and the divided-by-ten output of the N3 assembly. The inputs to the digital phase detector are the divided-by-ten output of the N3 assembly and the output from a mixer which detects the difference frequency of the N2 output and the SL2 voltage controlled oscillator. The output of SL2 is applied to SL1

The SL2 circuits are mounted on two circuit boards, A11 and A12. Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided by Service Sheets 13 and 14

The SL2 phase detector A12 is completely digital; it compares the relative positions (in time) of two sets of pulses and provides an error signal to correct phase errors or a dc level to correct frequency errors. One of the inputs to the phase detector is the divided by ten output of the N3 A8 assembly. The other input to the phase detector is the difer voltage controlled oscillator output. When the loop is locked, both phase detector input signals are at the same frequency ( $1: 1$ ratio). detected by a detected by a sense circuit which disables the phase detector. The phase detector output goes low if the SL2 voltage controlled oscillator frequency is low, the output goes high if the SL2 voltage controlled oscillator frequency is high. The pretuning circuit and

The pretuning circuit is a digital to analog converter controlled by CF digits 3,4 and 5 . The digital to analog converter for the CF digit three is physically located on the A12 assembly. The pretuning circuit roughly presets the voltage controlled oscillator to a frequency within the capture range of the loop. A summing circuit sums the negative current from the digital to analog converter circuit with a current from a +20 volt source and the output of the SL2 digital phase detector to precisely set the output frequency of the voltage controlled oscillator. The output from the voltage control oscillator is applied to SL1 and to a mixer in the A12 assembly.
The output frequency of SL2 is equal to the N2 frequency plus the divided by ten input from the N3 circuit.

## Summing Loop 1

The purpose of SL1 is to generate digitally controlled RF signals in the range of 20.000001 to 30.0 MHz in selectable increments as small as

## SERVICE SHEET 1 (Cont'd)

1 Hz . The output frequency of the SL1 voltage controlled oscillator is equal to the sum of the N1 output and the divided-by-one hundred output of SL2. The inputs to the digital phase detector are the divided-by-one hundred output of the SL2 assembly and the output from a mixer which detects the difference frequency of the N1 output and the SL1 voltage controlled oscillator. The output of SL1 is applied to the RF Section plug-in.

NOTE
In option 004 instruments the output is from 20.0001 to 30.0 MHz in selectable increments as low as 100 Hz . The voltage controlled oscillator is phase locked to the divided by one hundred output of the N2 loop.

The SL1 circuits are mounted on three circuit boards, A15, A18 and A19. Schematics, a more comprehensive circuit analysis, and troubleshooting information are provided on Service Sheets 15,16 and 17.

Operation of SL1 is the same as operation of SL2 except that the phase detector inputs are the divided by one hundred output of SL2 and the difference frequency between the output of N 1 and the SL1 oscillator. The output frequency is equal to $\mathrm{N} 1+\frac{\mathrm{SL} 2}{100}$ or $\mathrm{N} 1+\frac{\mathrm{N} 2}{100}+\frac{\mathrm{N} 3}{1000}$.

## NOTE

In option 004 instruments the phase detector inputs are the divided by one hundred output of N2 and the difference frequency between the N1 output and the frequency of the SL1 voltage controlled oscillator output. The output frequency is equal to $N 1+\frac{N 2}{100}$.

## RF Section

The RF Section plug-in processes the outputs from the mainframe to provide the desired output frequency.

Information relative to operation and service of the RF Section is provided in a separate manual.

## Digital Control Unit

Service Sheet 18 provides a logic diagram of the digital control unit.



## SERVICE SHEET 2

## PART OF REFERENCE LOOP CIRCUITS

Normally, causes of malfunctions in the Model 8660 C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.
When repairing the reference loop only one of the four covers should be removed at any given time. Operating the instrument with the erratic performance after required repairs have been completed.

## NOTE

After making repairs in any part of the reference loop circuits the adjustment procedures specified in Section $V$ paragraph 5-27 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

## Digital Voltmeter

Test Oscillator
10:1 Oscilloscope probes (2)
Oscilloscope
Frequency Counter

## REFERENCE LOOP GENERAL

The reference loop consists of four circuit boards located in the A4 assembly. This service sheet provides information about circuit operation and test procedures for the reference oscillator, reference
amplifier and relays, the phase detector and the divide-by-five and divide-by-two circuits. Schematic diagrams, text and troubleshooting information for the voltage controlled oscillator and divide-by-two circuits appear on Service Sheet 3.

The accuracy and stability of all the signals generated in the Model 8660C mainframe are traceable to the reference loop outputs.
The reference loop provides output frequencies of $500 \mathrm{MHz}, 100$ $\mathrm{MHz}, 20 \mathrm{MHz}, 10 \mathrm{MHz}, 2 \mathrm{MHz}, 400 \mathrm{kHz}$, and 100 kHz . These signals are used in other circuits in the mainframe and in the plug-in sections. All of the reference section outputs are derived from a 100 source. The reference signal may be supplied by the internal reference oscillator or by an external reference standard. The reference signal may be 5 or 10 MHz at a level of 0.2 to 2 volts rms.

## 1 REFERENCE OSCILLATOR, AMPLIFIER AND RELAYS

The Model 8660C (except for option 002 instruments) contains a 10 MHz temperature controlled crystal oscillator which is used as a

## SERVICE SHEET 2 (Cont'd)

reference source. Also included are switching relays and a buffer amplifier. The buffer amplifier serves to isolate the reference oscillator when its output is used as a reference source for external equipment.

## TEST PROCEDURE 1

Test 1-a. Connect the oscilloscope to the Model 8660C rear panel REFERENCE OUTPUT connector. If the internal reference is being used the oscilloscope should display a 10 MHz signal at about 4 volt peak to peak. If an external reference is used the oscilloscope should reference signal input.

If the signal is present proceed to test 1-b. If the signal is not present proceed to test 1-c.

Test 1-b. Disconnect the coaxial cable from A4J5 (REF INPUT) and connect the oscilloscope to the end of the cable. If the interna signal at about 5 volts peak to peak If an external reference is used the oscilloscope should display the input reference signal.

If the signal appeared in test 1-a, but does not appear in test 1-b, the cable between the A4A2 assembly and the reference relay/amplifier is probably defective.

If the correct signal is observed in test 1-b, proceed to TEST
PROCEDURE 2 .

Test 1-c. If the signal was not present in test 1-a, tilt the A4 assembly out of the frame, disconnect the coaxial cable from the reference oscillator assembly and connect the reference oscillato signal at about 7 volts peak to peak.

If the signal is not present, check for dc levels as follows: terminal 1 +20 volts, terminal $2,+35$ volts (oven voltage) and terminal $6,+5.2$ volts (when present indicates thermostat is open, temperatur stabilized). If the voltages are correct the reference oscillato assembly (A21) is defective.

## NOTE

The reference oscillator assembly is not considered a field repairable unit. Replacement is recommended.

If the signal is present at the reference oscillator output check the SELECTOR switch, the relay assembly (A22A1) and the reference amplifier (A22A2).

## SERVICE SHEET 2 (Cont'd)

## PHASE DETECTOR ASSEMBLY (A4A2) GENERAL

The phase detector consists of three basic circuits; a pulse generator, a sampler and a circuit to process the error signal.

The pulse generator converts the reference signal to very sharp, short duration pulses. These pulses are used to forward bias the sampler gate diodes.

The sampler gate provides a means of comparing the pulses generated from the reference signal to the 20 MHz signal from the A4A3 assembly. An error signal is developed to control the voltag controlled oscillator in the A4A4 assembly when a phase error exists.

## 2 PULSE GENERATOR

The pulse generator consists of Q1 through Q5, U1, T1 and associated components.

The reference input to Q1 may be 5 or 10 MHz . Q1 and Q2 act as an Tmplifier for low level signals and as a limiter for high level signals. Q3 acts as a limiter to ensure that the input to NAND gate U1A is always the same when the input reference signal is 0.2 to 2 volts rms. The output from Q3 is essentially a square wave with a slow rise time and a fast fall time; it is clipped, top and bottom, and it is approximately 5 volts peak to peak.
$\mathrm{U} 1, \mathrm{C} 11$ and R20 are used as a pulse shaper. The output of U1A is differentiated by C11 and R20 and inverted by U1B. The sharp pulses ( 20 to 25 nanoseconds) are inverted by U1D to provide positive-going pulses to drive Q4/Q5.

Q4/Q5 comprise a complementary emitter-follower pair; its purpose is to provide a low impedance drive to T1.

## TEST PROCEDURE

Test 2-a. Composite waveform SS2-1 and trace 2 of composit waveform SS2-2 illustrate the development of the 10 MHz pulse derived from the internal reference signal. These pulses are used to drive the sampling phase detector diode gates. Observing the ndividual waickly is to quickly isolate a malfunction in the circuit to an individual stage or to the reference oscillator/switching circuits.

There are no loops or feedback circuits in the pulse generator circuit It is safe to assume when a correct waveform is observed that all preceding portions of the circuit are operating properly.

## 3) SAMPLER

Sampler diodes CR4 and CR5 are normally reverse biased. When the sampling pulse appears across the secondary of T1 it is coupled through C18 and C19 to forward bias CR4 and CR5. Since the gate pulses are equal in amplitude but opposite in polarity, they will cancel at the junction of R32, R33, R34, and C20.

## 10 MHz reference input

 about 5 volts01-c about 5 volts
02-3 about 3 volts


3-c about 5 volts
1 pin 11 about 5 volts
Composite Waveform SS2-1


## Composite Waveform SS2-2

While CR4 and CR5 are forward biased the sampling gate is open and the 20 MHz signal from the A4A3 assembly is sampled. If the 20 MHz input from the A4A3 assembly is not phase locked to the pulses derived from the reference signal an ac signal will appear on the base of Q7. The polarity of the signal at any given time depends on the
polarity of the 20 MHz signal from the A4A3 assembly when the last sample was taken. The amplitude of the ac signal at any given time depends on what portion of the 20 MHz sine wave the last sample was taken from.

Each time CR4 and CR5 are forward biased the charge on C20 will change unless the phase relationship is the same as it was in the previous sample. The time constant of C20 and R34 is long and since the time between samples is never more than one microsecond, C20 cannot discharge appreciably between sampling pulses.

The reverse bias levels for CR4 and CR5 are maintained at the same levels (opposite polarities) by voltage divider networks.

## TEST PROCEDURE

Test 3-a. An oscilloscope loads the sampling circuit at TP3 and TP to a point where accurate analysis of the signal is not possible However, observing the waveforms and comparing them to the an adequate indication that the circuit is, or is not, functioning properly. The important points to observe are the two-to-one frequency ratio between the 20 MHz signal and the pulses, and the time coincidence of the positive-going and negative-going pulses at TP3 and TP4 with the pulses at TP1

## 4 ERROR SIGNAL AMPLIFIER

When a phase difference between the reference signal and the 20 MHz input exists, a signal appears on C20. This signal is amplified and used to correct the frequency of the voltage controlled oscillator in the A4A4 assembly.
Q7 and Q9 provide a high impedance input for the sampler output Q8 and Q10 comprise a differential amplifier. Emitter-follower Q11 provides the output to the A4A4 assembly.

## TEST PROCEDURE

Test 4-a. Connect an oscilloscope to the A4A2 output labeled VCO With the input 10 MHz reference disconnected from A4J5, (REF a test oscillator (output $0 \mathrm{dBm}, 3 \mathrm{kHz}$ ) to arbitrarily.)

Vary the output level of the test oscillator and note that the A4A2 output level displayed on the oscilloscope varies.

## NOTE

If the A4A2 output does not vary when the test oscillator output is varied, use the oscilloscope to check back through the stages for a point in the circuit where the level does change with a change in the output level of the test oscillator. The following stage is probably defective.

## 5 REFERENCE DIVIDE-BY-FIVE AND DIVIDE-BY-TWO ASSEMBLY A4A1

The A4A1 assembly divides the 10 MHz input from the A4A3 assembly four times; two times by five and two times by two. The assembly provides a 2 MHz clock signal to the digital control unit 100 kHz signals to the N 2 and N3 loops and 400 kHz to the N1 loop.

## SERVICE SHEET 2 (Cont'd)

Q3 and CR1 reduce the +20 volt input to +5 volts for operation of all circuits in the assembly. This method of providing power is used to minimize the effect of ac ripple on the power supply.

Q1 isolates the circuit from the 10 MHz source. Q2 amplifies the 10 MHz input and NAND gate U1A shapes it into pulses to drive U2. U2 provides a divided-by-five 2 MHz output at pin 8 which is used as a clock signal in the digital control unit. The 2 MHz output is also available at pin 11 of U 2 and is used to drive U3.
U3 divides the 2 MHz input from pin 11 of U 2 by five and provides outputs of 400 kHz at pins 8 and 11 . The 400 kHz output at U3 pin 8 is used as the phase detector reference in the N 1 loop. The 400 kHz at pin 11 of U3 is coupled to U3 pin 14 and divided by two. The 200 again divided by two. The 100 kHz output from U2 pin 12 is coupled through NAND gate U1B to the phase detector in the N3 loop. The 100 kHz signal is also coupled through NAND gate U1D to the phase detector in the N2 loop.

## TEST PROCEDURE 5

Composite waveform SS2-3 illustrates the development of pulses from the 10 MHz reference input and the 2 MHz clock output to the digital control unit.
Composite waveform SS2-4 illustrates the development of the 400 kHz and 100 kHz N loop reference signals from the 2 MHz clock signals.


Composite Waveform SS2-3


2 MHz clock about 5 volts
400 kHz to N 1 about 3 volts
200 kHz U 2 pin 14
00 kHz to N 2 about 4 volts
00 kHz to N 3 about 4 volts
Composite Waveform SS2-4
There are no loops or feed back paths in the circuit. It is safe to assume that when the proper waveform is observed at any point that preceding stages are functioning properly.
averving the waveforms at the test points specified should enable the technician to quickly solate the cause of a malfunction to a specific stage or component.


Figure 8-10. A21 Reference Oscillator Assembly


Figure 8-11. A22 Assembly Component Locations


Figure 8-12. A4A2 Reference Phase Dētector Component Locations


Figure 8-1 3. A4A1 Reference Divider Component Locations



## SERVICE SHEET 3

## PART OF REFERENCE LOOP CIRCUITS

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

When repairing the reference loop only one of the four covers should be removed at any given time. Operation of the instrument with the voltage controlled oscillator cover removed may cause faulty or erratic performance after required repairs have been completed.

## NOTE

After making repairs in any part of the reference loop circuits the adjustment procedures specified in Section $V$ paragraph 5-27 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

## Digital Voltmeter

Oscilloscope
Frequency Counter
10:1 Oscilloscope probes (2)

## REFERENCE LOOP GENERAL

The reference loop consists of four circuit boards located in the A4 assembly. Service Sheet 2 provides information about circuit operation and test procedures for the reference oscillator, reference amplifier and relays, the phase detector and the divide-by-five and divide-by-two circuits. Schematic diagrams, text and troubleshooting information for the voltage controlled oscillator and divide-by-two circuits appear on this service sheet.

The accuracy and stability of all the signals generated in the Model 8660C mainframe are traceable to the reference loop circuits.

The reference loop provides output frequencies of $500 \mathrm{MHz}, 100$ $\mathrm{MHz}, 20 \mathrm{MHz}, 10 \mathrm{MHz}, 2 \mathrm{MHz}, 400 \mathrm{kHz}$, and 100 kHz . These signals are used in other circuits in the mainframe and in the plug-in sections. All of the reference section outputs are derived from a 100 MHz master oscillator which is phase locked to a stable reference source. The reference signal may be supplied by the internal reference oscillator or by an external reference standard. The reference signal may be 5 or 10 MHz at a level of 0.2 to 2 volts rms.

1 OSCILLATOR, POWER SPLITTER, 500 MHz AMP and 100 MHz AMP

Q3 and associated components comprise a 100 MHz voltage controlled oscillator. Varactor CR1 is biased by the output of the

## SERVICE SHEET 3 (Cont'd)

A4A2 phase detector to assure that the oscillator is phase locked to the reference signal at 100 MHz .

The oscillator output is capacitively coupled to the base of Q4 which functions as a power splitter.

Q9 and associated components provide isolation from the +20 volt power supply for the oscillator and power splitter to minimize effects of ac power supply ripple or line variations.

The collector output of Q4 is capacitively coupled to A8, a 100 MHz tuned amplifier which functions as a buffer stage. The times five function is accomplished by Q7 which is tuned to 500 MHz . The 500 MHz output from the Q7 tank circuit is capacitively coupled to Q6, another 500 MHz tuned amplifier which also provides isolation.

The emitter output of Q4 is capacitively coupled to the base of Q5 which functions as a 100 MHz tuned amplifier buffer stage. This output is used in the Frequency Extension Module (accessory number 11661A).

TEST PROCEDURE 1

## NOTE

If the signal frequency is close to that specified in the following tests but is erratic, or not exact, the trouble is probably in the Phase Detector circuit. Refer to Service Sheet 2.

Test 1-a. With the A4A4 assembly cover removed use the counter and spectrum analyzer (separately) to check the 500 MHz output. The counter should indicate exactly 500 MHz and the oscilloscope should display a sine wave at about $>+3 \mathrm{dBm}$.

If the signal is present proceed to test 1-d. If the signal is not present proceed to test 1-b.

Test 1-b. Connect the oscilloscope and the counter (separately) to Q4-c. The counter should indicate exactly 100 MHz and the oscilloscope should display a sine wave at about 2.5 V p-p.

If the signal is present, but was not present in test 1-a, check Q6, Q7, Q8 and associated components. If the signal is not present, proceed to test 1-c.

Test 1-c. Connect the oscilloscope and the counter (separately) to Q4-b. The counter should indicate exactly 100 MHz and the scope should display a sine wave at about 0.4 volts.

## SERVICE SHEET 3 (Cont'd)

If the signal is present, but was not present in previous tests, Q4 is probably defective. If the signal is not present check Q3, Q9 and associated components.

Test 1-d. Use the oscilloscope and the counter (separately) to check the 100 MHz output. The counter should indicate exactly 100 MHz and the oscilloscope should display a sine wave at about 0.5 volts.

If the signal is not present, but was present in test 1-a, check Q5 and associated components. If the signal is present, proceed to Test Procedure 2.

## $2 \mathbf{2 0 M H z}$ OUTPUTS

A third 100 MHz signal is capacitively coupled from the oscillator tank circuit to the base of 100 MHz tuned amplifier Q2. The output of Q2 is used to drive a divide-by-five circuit (U1) whith provides the 20 MHz output. The 20 MHz output is used to drive the divide-by-two circuit in the A4A3 assembly. The 20 MHz signal is also coupled to 20 MHz tuned amplifier Q1 for use in circuits external to the reference loop.

## TEST PROCEDURE

Test 2-a. Connect the oscilloscope to the 20 MHz output from Q1. The display should be similar to that shown in the center.trace of composite waveform SS3-1. Proceed to test 2-b.

Test 2-b. Connect the oscilloscope to the 20 MHz output which goes to the A4A3 assembly. The display should be similar to that shown in the lower trace of composite waveform SS3-1.

If the correct signal is present, but was not present in test 2-a, check Q1 and associated components.

If the signal is not present proceed to test 2-c.

Test 2-c. Connect the oscilloscope to Q2-c. The oscilloscope display should be similar to the top trace in composite waveform SS3-1. If the signal is present, but was not present in test $2-\mathrm{b}, \mathrm{U} 1$ is probably defective.

If the signal is not present at Q2-c, Q2 is probably defective.

## SERVICE SHEET 3 (cont'd)



Composite Waveform SS3-1

## 3 DIVIDE-BY-TWO CIRCUIT A4A3

The A4A3 assembly provides 10 MHz outputs to the HF Loop (A4A7) phase detector, and to the divide-by-five and divide-by-two circuits (A4A1). It also provides a 20 MHz output for use in the reference loop phase detector A4A2.

Q1 and Q2 amplify the 20 MHz signal from the A4A4 assembly and applies it to U1 which divides by two. The +5 volts required for operation of U1 is derived from the +20 volt supply by R4 and CR1 to minimize effects of power supply ac ripple and line variations.

The output from U1 is capacitively coupled out to the HF loop as a reference signal. It is also coupled through Q3 to 10 MHz tuned amplifier Q5. The 10 MHz output from the Q5 is used in the divide-by-five and divide-by-two circuits (A4A1).

The 20 MHz output of Q2 is also coupled through tuned amplifier Q4 to the A4A2 phase detector assembly.

## TEST PROCEDURE 3

Test 3-a. Connect the oscilloscope to the 10 MHz output to the A4A1 assembly. The oscilloscope display should be about as shown in the bottom trace of composite waveform SS3-2. Verify that the frequency is exactly 10 MHz with the counter.

If the signal is not present proceed to test 3-b. If the signal is present, proceed to test 3-d.

Test 3-b. Connect the oscilloscope to the 10 MHz output which goes to the A4A4 assembly. The oscilloscope display should be about as shown in the next-to-the-bottom trace of composite waveform SS3-2. Verify that the frequency is exactly 10 MHz with the counter.

If the signal is present, but was not present in test $3-\mathrm{a}$, check Q3, Q5 and associated components. If the signal is not present proceed to test 3-c.

## SERVICE SHEET 3 (Cont'd)



Composite Waveform SS3-2
Test 3-c. Connect the oscilloscope to U1 pin 12. The oscilloscope display should be similar to the second from the top trace in composite waveform SS3-2.

## NOTE

The counter may be used to verify that the frequency is approximately 20 MHz . However, this point in the circuit is critical; the additional load on the circuit will probably disturb the phase lock loop balance.

If the display is correct, but was not correct in previous tests, U 1 is probably defective. If the display is not correct, check Q1, Q2 and associated components.

Test 3-d. Connect the oscilloscope and the counter (separately) to the 20 MHz output to the A4A2 assembly. The oscilloscope display should be similar to that shown in the top trace of composite waveform SS3-2. The counter readout should be exactly 20 MHz .

If the correct signal is not present check Q4 and associated components.

## A4A4



Figure 8-15. A4A4 Reference VCO Component Locations


Figure 8-16. A4A3 Reference Divide-by-Two Component Locations


## SERVICE SHEET 4

## PRETUNING ASSEMBLY (A4A6

Normally, causes of malfunctions in the Model 8660 C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees

The A4A6 assembly, a part of the three-assembly High Frequency Loop, is shown schematically and described on this service sheet. The other two assemblies, A4A5 and A4A7, are shown schematically and described on Service Sheets 5 and 6 .

## NOTE

After making repairs in any parts of the HF Loop circuits the adjustment procedure specified in Section $V$ paragraph 5-28 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Digital Voltmeter

## HIGH FREQUENCY LOOP GENERAL INFORMATION

The purpose of the HF loop is to provide a precise digitally controlled output frequency between 350 and 450 MHz in 10 MHz increments. This output is used in the internal extension module and in the plug-in RF Sections to provide the desired output signal.

## 1 PRETUNING CIRCUIT

Q1 through Q11, U1 and associated components comprise a digital to analog converter which pretunes the A4A5 voltage controlled oscillator. The pretuning circuit cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the loop.
Integrated circuit U1 is a decoder which converts the BCD input from CF digit 8 to individual select lines which turn on one of nine transistors connected in a resistive network. The transistor which is turned on effectively grounds one point in the resistive network. The voltage level output to the voltage controlled oscillator depends on which transistor is turned on. The voltage varies from about -7 volts ( 350 MHz ) to about -34 volts ( 450 MHz ).
A single input line, representative of BCD ' 1 ' from CF digit 9 drives Q1 to turn on Q11. Q11, the tenth transistor switch in the pretuning network, grounds the lowest resistance point in the network; it pretunes the voltage controlled oscillator to 350 MHz .

## TEST PROCEDURE 1

Test 1-a. With the digital voltmeter connected to the junction of R15, R18 and R19 set the CF as shown in table 8-28. The voltages shown in the table are typical; the actual voltage levels will depend on the characteristics of the varactor used in the voltage controlled oscillator.

If changing the setting of CF digit 8 through its range does not result in a change in the dc level at the junction of R15, R18 and R19, U1 may be defective.

Test 1-b. Use the digital voltmeter to check the A, B, C and D inputs to U1 from CF digit 8. These inputs are binary 1248 positive true logic. (Example: with CF digit 8 set to a 3 , U1 pins 15 and 14 should be high, about +4 volts, and pins 12

Reference Loop Vco
SERVICE SHEET 3

## SERVICE SHEET 4 (Cont'd)

and 13 should be low, about 0.3 volt). If the $A, B, C$ and $D$ inputs to $U 1$ are correct, use the digital voltmeter to check the U1 output. (Example: if thumbwheel digit 8 is set to a 3 Inputs A and B will be high and U1 pin 4 will go low.)

Operation of transistors Q2 through Q11 may be checked by checking the dc level at their collectors which are connected to the transistor shell. The numbers plated on the circuit board next to the potentiometers correspond to CF digits 8 and 9. CF digit 8 controls Q2 through Q10 and CF digit 9 drives Q1 to control Q11. The metallic shell (collector) of the transistor selected goes low ( 0.1 volt or less).

## 2 SUMMING CIRCUIT

Common base current source Q13 sums the output of the digital to analog converter, current from a +20 volt source (R13) and the error signal from the A4A7 sampling phase detector. The output of the digital to analog converter is partially controlled by common base current source Q14. Conduction of Q14 is controlled by a temperature sensitive stabistor diode on the voltage controlled oscillator circuit board. The current from Q14 is injected into the pretuning network to provide correct compensation for the voltage controlled oscillator drift characteristics. Q12 provides a means of coupling the error signal from the phase detector through C7 to the voltage controlled oscillator in the A4A5 assembly.

## TEST PROCEDURE 2

Test 2-a. Connect the digital voltmeter to the A4A6 output labeled FREQ on the circuit board. Set the CF digits as shown in Table 8-28. The voltages shown are typical; actual voltage levels depend on the characteristics of the varactor in the voltage controlled oscillator.

If the voltages were correct in test $1-\mathrm{a}$, but are not in test $2-\mathrm{a}$, check Q12, Q13 and associated components.

Table 8-44. Pretuning DC Levels

| Center Frequency | Test 1-a DC Level | Test 2-a DC Level |
| :---: | :---: | :---: |
| 0000.010000 MHz | -34.7 volts | -34.5 volts |
| 0010.010000 MHz | -28.3 volts | -29.3 volts |
| 0020.010000 MHz | -23.1 volts | -25.0 volts |
| 0030.010000 MHz | -18.7 volts | -21.4 volts |
| 0040.010000 MHz | -14.9 volts | -18.4 volts |
| 0050.010000 MHz | -11.6 volts | -15.7 volts |
| 0060.010000 MHz | -8.9 volts | -13.5 volts |
| 0070.010000 MHz | -6.5 volts | -11.6 volts |
| 0080.010000 MHz | -4.5 volts | -9.9 volts |
| 0090.010000 MHz | -2.6 volts | -8.4 volts |
| 0100.010000 MHz | -1.1 volts | -7.2 volts |



Figure 8-18. A4A6 HF Loop Pretuning Component Locations


## SERVICE SHEET 5

## SAMPLING PHASE DETECTOR (A4A7)

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A4A7 assembly, a part of the three-assembly High Frequency Loop, is shown schematically and described on this service sheet. The other two assemblies, A4A5 and A4A6, are shown schematically and described on Service Sheets 4 and 6.

## NOTE

After making repairs in any part of the HF Loop circuits the adjustment procedure specified in Section $V$ paragraph 5-28 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes)
Test Oscillator
Digital Voltmeter

## HIGH FREQUENCY LOOP GENERAL INFORMATION

The purpose of the HF loop is to provide a precise digitally controlled output frequency between 350 and 450 MHz in 10 MHz increments. This output is used in the internal extension module and in the plug-in RF Sections to provide the desired output signal.

The sampling phase detector compares the voltage controlled oscillator output to a 10 MHz signal from the reference section. The output of the phase detector circuit is a beat note or a varying dc level. The phase detector assembly contains a pulse generator, a sampler, and a signal processing circuit.

## 1 PULSE GENERATOR

Q1 and Q2 comprise a non-saturating, limiting amplifier. It provides a constant amplitude square wave (about 6 volts) derived from the 10 MHz reference signal. The circuit is designed to minimize the sensitivity of the output ac swing to power supply ripple.

The output of Q2 is applied to Q3 which converts the signal to a stable current waveform. A two-to-one stepdown transformer (T1) is used in conjunction with Q3 to provide the additional current required to drive the step-recovery diode CR1.

When Q3 conducts heavily CR1 is reverse biased by the signal which appears across the secondary winding of T 1 . When Q3 is turned off the collapsing

## SERVICE SHEET 5 (Cont'd)

inductive field of the T1 primary winding and the resonant circuit of L5 and C10 cause a flyback action which drives CR1 into conduction. L4 and C9 also enhance the flyback action.

## NOTE

One of the characteristics of a step-recovery diode, also called a charge-storage diode, is that the junction transition capacitance accumulates a charge while the diode is forward biased.

When the pulse which forward biased CR1 has ended, CR1 is again reverse biased; however, current will flow in the reverse direction until the charge stored in CR1 is depleted. When the charge stored in CR1 is depleted current flow stops abruptly; the sharp current transition causes L6 and L7 to develop large narrow voltages spikes of about 6 volts amplitude and one nanosecond in duration. The pulse is positive-going at L7 and negative-going at L6. These pulses are coupled through C10, C11 and balun T2 to forward bias the diodes in the sampler bridge. Balun T2 improves amplitude balance of the pulses.

## TEST PROCEDURE

Test 1-a. Composite waveform SS5-1 illustrates the correct waveforms for the three stages of the pulse generator.


## NOTE

Since an oscilloscope would load the remainder of the pulse generator circuit, and due to the short duration of the gate pulse, waveform analysis is not practicable. If the waveforms are as shown in SS5-1 and the loop does not phase lock, proceed to test procedure 2

## SAMPLER AND SIGNAL PROCESSOR

The sampler is a matched quad diode gate which is normally reverse biased. When the step-recovery diode generates the gate pulse all four of the sampler gate diodes are simultaneously forward biased. When the sampler gate diodes are forward

HF Loop Pretuning
SERVICE SHEET 4

## A4A7)

in the Model 8660 C will be isolated to a circuit of performing the tests specified in the
three-assembly High Frequency Loop, is shown service sheet. The other two assemblies, A4A5 and described on Service Sheets 4 and 6

## NOTE

yy part of the HF Loop circuits the ecified in Section $V$ paragraph $5-28$ $o$ ensure proper operation of the

See Table 1-2)

## RAL INFORMATION

provide a precise digitally controlled output 1 Hz in 10 MHz increments. This output is used and in the plug-in RF Sections to provide the
ares the voltage controlled oscillator output to ce section. The output of the phase detector c level. The phase detector assembly contains a §nal processing circuit.
ting, limiting amplifier. It provides a constant ,lts) derived from the 10 MHz reference signal. the sensitivity of the output ac swing to power

3 which converts the signal to a stable current transformer (T1) is used in conjunction with ent required to drive the step-recovery diode
is reverse biased by the signal which appears T1. When Q3 is turned off the collapsing

## SERVICE SHEET 5 (Cont'd)

inductive field of the T1 primary winding and the resonant circuit of L5 and C10 cause a flyback action which drives CR1 into conduction. L4 and C9 also enhance the flyback action.

## NOTE

One of the characteristics of a step-recovery diode, also called a charge-storage diode, is that the junction transition capacitance accumulates a charge while the diode is forward biased.

When the pulse which forward biased CR1 has ended, CR1 is again reverse biased; however, current will flow in the reverse direction until the charge stored in CR1 is depleted. When the charge stored in CR1 is depleted current flow stops abruptly; the sharp current transition causes L6 and L7 to develop large narrow pulse is positive-going at L7 and negative-going at L6. These pulses are coupled through C10, C11 and balun T2 to forward bias the diodes in the sampler bridge. Balun T2 improves amplitude balance of the pulses.

## TEST PROCEDURE

Test 1-a. Composite waveform SS5-1 illustrates the correct waveforms for the three stages of the pulse generator


10 MHz input 4 volts p -p

01-c 10 MHz 9 volts p-p
02-c 10 MHz 9 volts p -p 03-c 10 MHz 5 volts p-p

Composite Waveform SS5-1

## NOTE

Since an oscilloscope would load the remainder of the pulse senerator circuit, and due to the short duration of the gate pulse, waveform analysis is not practicable. If the waveforms are as shown in SS5-1 and the loop does not phase lock, proceed to test procedure

## 2 SAMPLER AND SIGNAL PROCESSOR

The sampler is, a matched quad diode gate which is normally reverse biased. When the step-recovery diode generates the gate pulse all four of the sampler gate diodes are simultaneously forward biased. When the sampler gate diodes are forward

## SERVICE SHEET 5 (Cont'd)

biased a sample of the signal from the A4A5 voltage controlled oscillator is taken and stored in C13.

Q4 and Q5 comprise a differential amplifier. The non-inverting input (G2) is derived from the sampling circuit. The output is applied to emitter-follower Q6 which provides a low impedance phase error output. The output of Q6 is also fed back to the differential amplifier inverting input (G1) to close the loop at unity gain. The holding capacitor, C13 is connected directly between the two inputs to Q4; this bootstraps C13 to extend the sampler's frequency response.

CR8 and CR9 provide reverse bias voltages for the sampling gate diodes. These bias voltages are balanced and centered on the output signal to improve sampler efficiency.

R18 controls the response of the sampler by varying the amount of back-bias for the bridge; R18 controls the response of the sampler by varying the amount of ba

R22 controls the quiescent output level to the summing circuit in A4A6; it should be adjusted for zero output with the input from the voltage controlled oscillator disconnected. If the voltage controlled oscillator output is harmonically related to the reference signal the
output of the phase detector is proportional to the sine of the difference in phase of the two signals. If the voltage controlled oscillator frequency is not harmonically related to the reference signal, the output of the phase detector is a beat note at the difference frequency.

## TEST PROCEDURE

Test 2-a. Disconnect the input to the sampler gate from the A4A5 voltage controlled oscillator and substitute a $1 \mathrm{MHz}, 10 \mathrm{dBm}$ signal from the test oscillator. Connect the oscilloscope to the phase error output (labeled on the circuit board) Varying the output level of the test oscillator should cause the oscilloscope display to follow the amplitude change

If the oscilloscope display is not as specified proceed to test 2-b
If the display is correct and the display for test 1-b was correct, check the step-recovery diode and associated components.

Test 2-b. With the oscilloscope connected as it was in test 2 -a, inject the 1 MHz signal at Q4-G2. If the signal is now displayed on the oscilloscope and varies as the output of the test oscillator is varied, check the step-recovery diode, the sampler gate diodes and associated components
If the signal is not displayed check Q4, Q5, Q6 and associated components. SERVICE SHEET 4


Figure 8-20. A4A 7 HF Loop Phase Detector Component Locations


SERVICE SHEET 6

## VCO AND AMPLIFIERS (A4A5)

Normally, causes of malfunctions in the Model 8660 C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A4A5 assembly, a part of the three-assembly HF Loop, is shown schematically and described on this service sheet. The other two assemblies, A4A6 and A4A7, are shown schematically and described on Service Sheets 4 and 5 .

## NOTE

After making repairs to any part of the HF Loop circuits the adjustment procedures specified in Section V paragraph 5-28 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Digital Voltmeter
Spectrum Analyzer
Frequency Counter

## 1 HIGH FREQUENCY LOOP GENERAL INFORMATION

The purpose of the HF Loop is to provide a precise digitally controlled output frequency between 350 and 450 MHz in 10 MHz increments. This output is used in the Frequency Extension Module and in the plug-in RF Section to provide the desired output signal.

## VCO AND AMPLIFIERS

Transistor A4 and associated components comprise a voltage controlled oscillator. The output frequency, when the loop is phase locked, is always a 10 MHz harmonic between 350 and 450 MHz . C3 is adjusted to set the high frequency end of the band. C1 is part of the loop filter in the control path and also provides an ac ground for the varactor at the bias point.
The oscillator output (about .5 volts rms ) is coupled through an isolation transformer to two identical three-stage buffer amplifiers. The isolation transformer splits the power equally to the two amplifiers and also eliminates feedthrough of extraneous signals from one amplifier to the other. The amplifiers provide outputs that are about 1 volt rms into 50 ohms.

Additional isolation from extraneous signals is provided by separate power supply inputs to the two amplifiers, extensive decoupling between stages, multiple grounding points for individual stages and separation of ground planes for individual stages.

CR2 is a stabistor used for temperature compensation for the voltage controlled oscillator. The forward voltage drop of the stabistor changes with the voltage controlled oscillator temperature and controls a current source (A4A6Q14) in the pretuning assembly.

A4A5




## SERVICE SHEET 7

## N1 PHASE DETECTOR ASSEMBLY A16

Normally, causes of malfunctions in the Model 8660 C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.
The A16 assembly, a part of the two-assembly N1 phase lock loop is shown schematically and described on Service Sheet 8 .
When trouble has been isolated to the A16 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

NOTE
After making repairs in any part of the N1 loop circuits the adjustment procedures specified in Section V paragraph 5-29 should be performed to ensure proper operation of the instrument

## TEST EQUIPMENT REQUIRED (see Table 1-2)

Oscilloscope (with 10:1 divider probes)
Drequency Counter
N1 LOOP GENERAL INFORMATION
The purpose of the N 1 loop is to generate digitally controlled RF signals in the range of 19.8 to 29.7 MHz in selectable 100 kHz increments. The voltage controlled oscillator is phase locked to a 400 kHz reference which is derived from the master oscillator in the reference section. The RF output from the N1 loop is applied to Summing Loop 1.

## 1 PROGRAMMABLE DIVIDER CIRCUIT

The integrated circuits in the A16 assembly, except for U1, are all used to count down the input from the N 1 voltage controlled oscillator. When there is no BCD input (all inputs low) and the loop is locked, the input from the voltage controlled oscillator will be 29.7 MHz ;
the programmable divider will divide by 297 and provide a 100 kHz output at TP3. U5 and the programmable divider will divide by 297 and provide a 100 kHz output at TP3. U5 and U6 are preset by CF digits 6 and 7 and programmed to vary between start counts of 00 to
99 . Operation of the circuit is as follows:

Assume that initially there are no BCD input to decade dividers $U 5$ and $U 6$ and they have been preset to zero. Assume also that U2A pin $6(\mathrm{Q})$ and U 2 B pin $8(\mathrm{Q})$ are both low. U 4 pin $6(\bar{Q})$, U3A pin $6(\bar{Q})$ and U3B pin $8(\bar{Q})$ are all high.
AND gate U7A functions as a Schmitt trigger to change the incoming positive half cycles of the sine wave from the voltage controlled oscillator to positive-going pulses. These pulse clock U5 when AND gate U7B is enabled. U5 pin 12 provides a divided-by-ten output to
clock U6 and also provides A and B (BCD 1 and 2) outputs. The A and B outputs of U5 clock U6 and also provides A and B (BCD 1 and 2) outputs. The A and B outputs of U5
have no effect on U4 until AND gate U7C pin 8 goes high (AND gate U7C will be discussed have no effect on

U6 pin 12 provides a divided-by-one hundred output to clock U2A and also provides A and D (BCD 1 and 8) outputs to AND gate U7C. The A and D outputs have no effect on AND gate U7C until after U2B pin $8(\bar{Q})$ goes high at the count of 200 .
The D output of U6 (pin 12) goes high on the count of 8 ( 80 input pulses to U5). This output has no effect on U2A because U2A is clocked on negative-going pulses only.
The D output of U6 (pin 12) goes low at the count of 10 ( 100 input pulses to U5) and clocks U2A. This causes U2A pin $6(\bar{Q})$ to go high. When the D output of U6 (pin 12) again output goes low to clock U2B. When U2B pin $8(\overline{\mathrm{Q}})$ goes high it provides a high input to AND gate U7C pin 11.

## SERVICE SHEET 7 (Cont'd)

Ninety input cycles after U2B pin $8(\overline{\mathrm{Q}})$ goes high ( 290 input cycles), U6 A and D outputs (BCD 1 and 8) go high and enable AND gate U7C and provide a high to J input 3 of U4, U4 still cannot be clocked because U4 J pins 4 and 5 are still low.

Three input cycles after U4 pin 3 goes high ( 293 input cycles), the A and $B$ outputs of U5 (BCD 1 and 2) go high and enable the $J$ input to $J$-K flip-flop U4.

The 294th input cycle will clock U 4 at pin 12 because all J and K inputs are high. When clocked, 44 Q goes low and AND gate U7B no longer enabled; the count, as far as U5, U6 and U2 are concerned is ended. When U4 $\bar{Q}$ goes low it also sets U3A and U3B; the $\bar{Q}$ outputs go low and the $Q$ outputs go high. When U3A pin $6(\bar{Q})$ goes low it is used to preset U5 and U6 to the start count programmed by CF digits 6 and 7 or by remote control; U2A and U2B Q outputs are no longer enabled since the count is no longer at the 'sense' count of 293.

When U3B pin $9(\mathrm{Q})$ goes high the leading edge is used to generate the sampling pulse. The first pulse to the sampling phase detector i initiated by the 294th input cycle. Since three more cycles are required to restart the count cycle, following sampler pulses are 297
cycles apart.

The 295th input cycle will clock U4 and since U 4 K is high, $\mathrm{U} 4 \overline{\mathrm{Q}}$ will go high. This $\bar{Q}$ high is applied to the $K$ input of U3A (pin 2) and to pin 4 of AND gate U7B. AND gate U7B will not be enabled because U3B pin $8(\bar{Q})$ is holding AND gate U7B pin 5 low.
The 296th input cycle will clock U3A because the $K$ input is now high. U3A pin $6(\bar{Q})$ will go high. This high $\bar{Q}$ output is applied to AND gate U7B pin 5 and the next count cycle is enabled through AND gate U7B.

When there is a preset input programmed into U5 and U6 pins 3, 4 10 and 11 the terminal count is still 297 . However, the count starts at the number programmed into the BCD inputs. As an example, if the BCD input into U5 and U6 is 99, the first cycle would cause the same digital circuit changes that the 100th cycle caused in the
discussion above (U2A would be clocked). The frequency division would be 297 - 99, equal to division by 198. The phase lock loop operation would result in an input frequency to the programmable divider of 19.8 MHz . When divided by 198 , the divider output at TP3 would again be 100 kHz .
The output from U3B at TP3 is always 100 kHz when the voltage controlled oscillator is phase locked to the reference signal.

Q6 and CR1 provide Vcc to U3 to minimize the effect of power supply ac ripple and line variations.

## TEST PROCEDURE

Composite waveform SS7-1 illustrates the proper timing relationship between the 400 kHz reference input, the pulse output from the

## SERVICE SHEET 7 (Cont'd)

pulse generator and the sampling point on the 400 kHz reference ignal when the loop is phase locked.


Composite Waveform SS7-1

## NOTE

In the following tests the $C F$ is set to 0 unless otherwise noted. Test
TP5. ine wave at TP5 is as shown in trace 2 of composite waveform SS7-1. If the signal is as shown proceed to test 1-b.

If the 400 kHz signal cannot be counted or does not appear as shown n the composite waveform for TP5, check the reference input at XA16-1-2. The reference input signal should be about 4 volts peak-to-peak and 400 kHz as shown in trace 1 of composite waveform SS7-1. If the correct waveform is observed, but was not observed at TP5, check Q1, Q2 and associated components. If the loop and, if necessary, the reference loop (See Service Sheet 3 ).

If trouble is found and corrected, perform the adjustment procedures specified in paragraph 5-16 to verify proper operation of the loop.
Test 1-b. Connect one oscilloscope channel and the counter to TP4 and the other oscilloscope channel to the junction of C20, R24 and nd 4 of composite waveform SS7-1 and the counter will display nd 4 of comp

Note that the waveform shown by trace 3 of the composite waveform may appear as shown even if the counter does not indicate 100.000 kHz . This is because the frequency sensitivity of the scilloscope is not as exacting as the frequency sensitivity of the counter

If the programmable divider and the pulse shaper are working properly but the loop is not locked, trace 4 as shown in composite

## SERVICE SHEET 7 (Cont'd)

waveform SS7-1 may still show the pulses, but the signal between the pulses will be erratic.

Test 1-c. If the pulses are not present at TP4 or the junction of C20, R24 and T1 and the counter counts randomly or not at all, connect the oscilloscope to TP3. The oscilloscope should display a waveform similar to that shown in trace 3 of the composite waveform SS7-1 at about half the amplitude.

If the pulses are not present at TP3 proceed to test 1-d.
If the pulses are present at TP3 but were not present at TP4, check Q4, Q5 and associated components. After repairs are made recheck test procedure 1-b.

If the pulses are now present at TP4 and the junction of C20, R24 and T1, but the four-cycle sine wave is not present as shown in trace 4 of composite waveform SS7-1, rotate R38 through its range to see if the proper waveform can be obtained. If the frequency displayed on the counter does change as R38 is rotated but phase lock cannot be achieved, check Q3, the sampling diodes and associated components.

Test 1-d. If the pulse is not present at TP3 in test 1-c connect the oscilloscope to AND gate U7B pin 6. The waveform should be as shown in the top trace of composite waveform SS7-2. If the correct signal is observed proceed to test 1-e.

If the correct signal is not observed connect the oscilloscope to TP1. The waveform should be as shown in the center trace of composite waveform SS7-2. If the signal is present, but was not present at AND gate U7B pin 6, use the digital voltmeter to check the voltage at pins 4 and 5 of AND gate U7B. The digital voltmeter should indicate about 4 volts. If the voltages are present AND gate U7B is defective.


Composite Waveform SS7-2
If the voltages are not present at AND gate U7B pins 4 and 5 , ground pin 2 of U4. If the signal now appears at AND gate U7B pin 6, U3 and U7B are functioning properly. The trouble is probably in the gating circuit to U4. Proceed to test 1-e.
If the signal is not present at TP1, use the oscilloscope to check the input from the voltage controlled oscillator at XA16-2-15. The signal should be as shown in the lower trace in composite waveform SS7-2.

## SERVICE SHEET 7 (Cont'd)

If the signal is present AND gate U7A is probably defective. If the signal is not present, the A17 assembly or interconnections are defective.

Test 1-e. It is assumed in this test that the signal from the N1 voltage controlled oscillator is present at U5 pin 8. Composite waveform SS7-3 illustrates the correct waveforms at the points shown. All signals are about 4.5 volts.


Composite Waveform SS7-3
If none of the waveforms are present, U 5 is probably defective.
Note that the reset pulse in trace 5 is in time coincidence with the 'missing' pulse in trace 1 and that the reset pulse resets traces 2 and 4.

Test 1-f. Composite waveform SS7-4 illustrates the correct waveforms at the points shown. All signals are about 4.5 volts in amplitude. Sync the oscilloscope to TP3 for this test.


Composite Waveform SS7-4
Note that U4 pin 8 goes high only when all of the J inputs (U4 pins 3,4 and 5) are high.
If the waveforms for traces 2 and/or 3 are not present, U5 is probably defective.
If the waveforms for traces 1,4 and 5 are not present, proceed to test $1-\mathrm{g}$.
Test 1-g. Composite waveform SS7-5 illustrates the correct waveforms at the points shown. All signals are about 4.5 volts in amplitude. Sync the oscilloscope to TP3 for this test.

## 7 (Cont'd)

nay still show the pulses, but the signal between the tic.
ulses are not present at TP4 or the junction of C20, the counter counts randomly or not at all, connect o TP3. The oscilloscope should display a waveform own in trace 3 of the composite waveform SS7-1 at plitude
ot present at TP3 proceed to test 1-d
oresent at TP3 but were not present at TP4, check oresent at TP3 but were not present at TP4, check
ciated components. After repairs are made recheck
now present at TP4 and the junction of C20, R24 our-cycle sine wave is not present as shown in trace our-cycle sine wave is not present as shown in trace
aveform SS7-1, rotate R38 through its range to see eform can be obtained. If the frequency displayed oes change as R38 is rotated but phase lock cannot leck Q3, the sampling diodes and associated
pulse is not present at TP3 in test 1-c connect the ND gate U7B pin 6 . The waveform should be as trace of composite waveform SS7-2. If the correct proceed to test 1-e.
ral is not observed connect the oscilloscope to TP1. ould be as shown in the center trace of composite If the signal is present, but was not present at AND use the digital voltmeter to check the voltage at pins gate U7B. The digital voltmeter should indicate the voltages are present AND gate U7B is defective.

## WWONOV 1 p ping spepox suols

$W_{W W}^{T P 1}$ approx $^{4.5}{ }^{\text {volts }}$
WWWM ${ }_{\text {xA16-2-15 approx }} 1.5$ volts
te Waveform SS7-2
not present at AND gate U7B pins 4 and 5 , ground he signal now appears at AND gate U7B pin 6, U3 he signal now appears at AND a is probably in the J4. Proceed to test 1-e.
ot present at TP1, use the oscilloscope to check the oltage controlled oscillator at XA16-2-15. The signal in in the lower trace in composite waveform SS7-2.

## SERVICE SHEET 7 (Cont'd)

If the signal is present AND gate U7A is probably defective. If the signal is not present, the A17 assembly or interconnections are defective.
Test 1-e. It is assumed in this test that the signal from the N 1 voltage controlled oscillator is present at U5 pin 8. Composite waveform signals are about 4.5 volts.


Composite Waveform SS7-3
If none of the waveforms are present, U 5 is probably defective.
Note that the reset pulse in trace 5 is in time coincidence with the 'missing' pulse in trace 1 and that the reset pulse resets traces 2 and 4.

Test 1-f. Composite waveform SS7-4 illustrates the correct waveforms at the points shown. All signals are about 4.5 volts in amplitude. Sync the oscilloscope to TP3 for this test.


## Composite Waveform SS7-4

Note that U4 pin 8 goes high only when all of the Jinputs (U4 pins 3,4 and 5) are high.
f the waveforms for traces 2 and/or 3 are not present, U5 is probably defective.
If the waveforms for traces 1,4 and 5 are not present, proceed to test $1-\mathrm{g}$.
Test 1-g. Composite waveform SS7-5 illustrates the correct waveforms at the points shown. All signals are about 4.5 volts in amplitude. Sync the oscilloscope to TP3 for this test.

HF Loop VCO
SERVICE SHEET 6

## SERVICE SHEET 7 (Cont'd)



## Composite Waveform SS7-5

If the inputs to AND gate U7C are not as shown, U6 or U2 may be defective.
If the inputs are as shown but there is no output at AND gate U7C pin 8, U7 is defective.

## 2 PULSE AMPLIFIER

The positive-going output from U3B pin 9 is used to generate the pulse required to open the sampler gate. Common base amplifier Q5 and emitter follower Q4 amplifies and couples the pulse to T1. CR2 and CR3 are used to minimize flyback action. CR3 also bypasses the negative-going pulse around the transformer primary to ensure that only the positive-going pulse is coupled to the transformer secondary.
A 400 kHz signal from the reference loop is applied to the secondary center tap of T1. L5 and C8 (along with C7 in the reference loop A4A1 assembly) comprise a low pass filter with a cut off frequency of about 500 MHz . The TTL input from the reference loop is reshaped into a sine wave by the low pass filter. L6 and C 13 comprise a tuned circuit which bypasses unwanted signals and further filters the sine wave.

Sampler diodes CR4 and CR5 are normally reverse biased. When the sampling pulse appears across the secondary of T1 it is coupled through C20 and C21 to forward bias CR4 and CR5. Since the gate pulses are equal in amplitude but opposite in polarity, they will cancel at TP6.

While CR4 and CR5 are forward biased the sampling gate is open and the 400 kHz reference signal is sampled.
This type of sampling phase detector may be phase locked at virtually any point on the sine wave curve. Ideally, the zero crossover point of the sine wave should be used to improve the lock and hold-in capability of the loop.

If the divided down output of the voltage controlled oscillator in the A17 assembly ( 100 kHz pulses) is not phase locked to the 400 kHz reference signal an ac signal is developed at TP6. The polarity of the signal at any given time depends on the polarity of the 400 kHz reference signal at the time the last sample wa taken. The amplitude of the signal at any given time depends on what portion of the sine wave the las sample was taken from. Each time CR4 and CR5 are forward biased the signal derived from the 400 kHz reference signal at T1 terminals 4 and 6 are coupled through the sampling gate to control the charge on C22.

When the sampling gate pulse ends, CR4 and CR5 are again reverse biased and the sampling gate is closed Since Q3 is a high impedance device, the charge will remain on C22 until the next sampling pulse. The error signal from Q3 is applied to the summing amplifier in the A17 assembly through operational amplifier U1

Test point 8 may be grounded to open the phase lock loop. Since the emitter of A17Q4 in the A17 assembly is also almost exactly at dc ground level, grounding this test point will not affect the pretuning circuit. With the loop open both the pretuning and the error signal may be checked.

## SERVICE SHEET 7 (Cont'd)

## TEST PROCEDURE 2

Test 2-a. Connect the oscilloscope to TP6. If the 400 kHz signal is present one of the sampling gate diodes (CR4 or CR5) is probably shorted. If the gate pulses are present one of the sampling gate diodes is probably open (negative-going pulses CR5, positive-going pulses, CR4). Proceed to test 2-b.

Test 2-b. With the oscilloscope connected to TP6, ground TP8. The signal displayed should be similar to that shown in waveform SS7-6, at about 3 volts. The frequency of the signal will be determined by the difference detected by the sampling gate (typically 200 to 400 Hz ).

If the signal is present at TP6, connect the oscilloscope to U1 pin 6 . The sine wave should be about the same as that shown for TP6 except that the sampling points will not be as obvious.

If the signal is present at $U 1$ pin 6 the error amplifier and the sampling circuits are functioning properly.
If the signal is not present at U1 pin 6, but was present at TP6, check U1 and associated components. After repairs are made repeat the test and remove the ground from TP8.


Waveform SS7-6


Figure 8-26. A16 N1 Phase Detector Component Locations


## SERVICE SHEET 8

## N1 PRETUNING AND OSCILLATOR ASSEMBLY A17

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A17 assembly, a part of the two-assembly N1 phase lock loop is shown schematically and described on this service sheet. The N1 Phase Detector Assembly, A16, is shown schematically and described on Service Sheet 7

When trouble has been isolated to the A17 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points reinstalled using
and components.

## NOTE

After making repairs in any part of the N1 loop circuits the adjustment procedures specified in Section V paragraph 5-29 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Digital Voltmeter
Frequency Counte
Oscilloscope (with 10:1 divider probes)

## N1 LOOP GENERAL'INFORMATION

The purpose of the N1 loop is to generate digitally controlled RF signals in the range of 19.8 to 29.7 MHz in selectable 100 kHz increments. The voltage the master oscillator in the reference section. The RF output from the N1 loop is applied to Summing Loop 1.

## 1 VOLTAGE CONTROLLED OSCILLATOR

Q3, Q5 and associated components comprise a voltage controlled oscillator. Two varactors (CR6 and CR7) are used in parallel to provide a high $Q$ as well as the wide capacitance range required

FET Q5 acts as a source follower in the feedback circuit; it provides high impedance at the gate and a low impedance at the source. The gain of the FET is
held at less than unity to minimize the Miller effect which might reflect held at less than unity to minimize the Miller effect which might reflect capacitance back into the oscillator tank circuit.
Q1 amplifies the signal from the FET and applies it to two separate amplifiers. Q10 and Q15 provide the output to drive the SL1 mixer and Q8 drives the programmable divider in the A16 assembly.

## SERVICE SHEET 8 (Cont'd)

## TEST PROCEDURE

Test 1-a. Connect the frequency counter to XA17-1-2 and set CF as shown in table 8-4. The counter readout should be as shown in the table. (Make allowances for counter accuracy).

If the counter does not display a frequency at, or close to, that specified, connect the oscilloscope to TP3. The oscilloscope should display a sine wave at about .3 voits peak-to-peak. If the sine wave is present at TP3
XA17-1-2, check Q10, Q15 and associated components.

If there is no signal at TP3 check the bias level at TP2. The bias level should be about as shown in Table $8-4$ for the front panel frequency setting. If the bias level is within the range of approximately -3.4 to -30 volts, and there is no signal at within the range shown, proceed to 2 -b If the counter displays the
panel settings, proceed to $2-\mathrm{a}$.

## 2 PRETUNING CIRCUIT

The frequency of the voltage controlled oscillator is roughly preset by the digital The frequency of the voltage controlled oscillator is roughly preset by the digital
to analog converter (U1, U2, Q11 through Q14 and Q16 through Q19). The digital to analog converter cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the phase lock loop, The inputs to U 1 and U 2 are BCD bits coded $8,4,2$ and 1 . When any of the BCD inputs are high they cause the output of the NAND gate to which they are connected to go low; the transistor connected to the NAND gate output is switched on.

When all of the BCD inputs are low Q9 is biased to provide approximately -25 volts at TP1 (Q7-e). With this de level at TP1 the oscillator is roughly preset to 29.7 MHz.

When any one or more of the BCD inputs go high the transistor associated with it saturates and the current through Q9 is reduced. The reduction in current flow through Q9 changes the bias on Q7 and causes the voltage at TP1 to go less negative (closer to do ground level). Finally, when preset to 19.8 MHz .

Q4 is a summing amplifier which combines the output of the digital to analog converter and the signal from the N 1 phase detector. The summing point (Q4-e) sums the current from three sources; a current source from the +20 volts supply hrough R31, R32 and R33, a negative source from the digital to analog converter TP1) and the error signal from the N1 phase detector. The voltage at the

When TP1 is at approximately -25 volts (all inputs low), most of the current from the +20 volts source flows through Q7; very little current flows through Q4. Under these conditions the voltage at Q4-c is about -30 volts. As the voltage at TP1 decreases (gets closer to dc ground level), less current flows through Q7, more current flows through Q4, and the Q4 collector voltage goes less negative.

## SERVICE SHEET 8 (Cont'd)

CR3 through CR5, CR8 through CR15 and associated resistors are used to the voltage applied to the voltage controlled oscillator so that the frequenc be linear with the applied voltage. When all BCD inputs are low, Q4-c is at a -30 volts, the junction of R43 R48 is about -27.5 volts and all of the dioc the resistive network are reverse biased. As the voltage at TP1 decreases
closer to -5.2 volts), current through Q4 increases and the Q4 collector vo goes less negative. As the Q4 collector voltage decreases first CR3, then CR are forward biased. As the diodes are forward biased resistors are added in pa with R38 and R39 to shape the rate at which the voltage decreases at Q4-c.

Q2 and Q5 are emitter followers which couple the output of Q4 to the vara Q2 provides a high impedance for the output of the summing amplifier colle $\mathrm{R46}$, L 7 and C14 comprise a 400 kHz trap to attenuate ( 15 to 20 dB ) any detector. R51, L8, C20 and C21 comprise a low pass filter with a frequency of about 200 kHz .

## TEST PROCEDURE

Table 8-29 represents typical voltage levels for test points 1 and 2 and fequencies at XA17-1-2 for given settings of CF digits six and seven whe loop is locked.

## NOTE

While the voltages shown for TP2 are typical (they will vary from instrument to instrument due to differences in varacto characteristics), they are representative of normal ratio of TP to TP1 voltages.
Test 2-a. With the digital voltmeter connected to TP1 select CF's shown in -8-4. The voltage level should approximately follow those shown in Table 8-4. If the voltage at TP1 does not vary at all, first verify the presence of input d
information to the NAND gates, then check Q7, Q9 and associated compon
If the voltage at TP1 does not vary as shown, or some CF (or CF's) do produce a change, first verify the presence of the input to the N transistor.

If the voltages at TP1 are approximately as shown in Table 8-29 proceed to 2 -b.

Test 2-b. Connect the digital voltmeter to TP2 and the counter to XA17-1 he voltage at TP2 does not change about as shown in Table 8-29 for spec CF's, or does not change at all, check Q2, Q4, Q6 and associated components
f the voltage at TP2 varies approximately as shown in Table 8-19, bu frequency at XA17-12 does not step (or there is no RF output), refer to Procedure 1 and check the oscillator circuits.

## SERVICE SHEET 8 (Cont'd)

CR3 through CR5, CR8 through CR15 and associated resistors are used to shape the voltage applied to the voltage controlled oscillator so that the frequency will be linear with the applied voltage. When all BCD inputs are low, Q4-c is at about -30 volts, the junction of R43 R48 is about -27.5 volts and all of the diodes in the resistive network are reverse biased. As the voltage at TP1 decreases (gets closer to -5.2 volts), current through Q4 increases and the Q4 collector voltage goes less negative. As the Q4 collector voltage decreases first CR3, then CR4 etc. are forward biased. As the diodes are forward biased resistors are added in parallel with R38 and R39 to shape the rate at which the voltage decreases at Q4-c.

Q2 and Q5 are emitter followers which couple the output of Q4 to the varactors. Q2 provides a high impedance for the output of the summing amplifier collector. R46, L7 and C14 comprise a 400 kHz trap to attenuate ( 15 to 20 dB ) any 400 kHz ripple which may be present from the reference signal used in the phase detector. R51, L8, C20 and C21 comprise a low pass filter with a cutoff frequency of about 200 kHz .

## TEST PROCEDURE 2

Table 8-29 represents typical voltage levels for test points 1 and 2 and exact frequencies at XA17-1-2 for given settings of CF digits six and seven when the loop is locked.

## NOTE

While the voltages shown for TP2 are typical (they will vary from instrument to instrument due to differences in varactor characteristics), they are representative of normal ratio of TP2 to TP1 voltages.

Test 2-a. With the digital voltmeter connected to TP1 select CF's shown in Table 8-4. The voltage level should approximately follow those shown in Table 8-4.

If the voltage at TP1 does not vary at all, first verify the presence of input digital information to the NAND gates, then check Q7, Q9 and associated components.

If the voltage at TP1 does not vary as shown, or some CF (or CF's) do not produce a change, first verify the presence of the input to the NAND gate/transistor combination affected, then check the NAND gate and the gate/transi

If the voltages at TP1 are approximately as shown in Table 8-29 proceed to Test 2-b.

Test 2-b. Connect the digital voltmeter to TP2 and the counter to XA17-1-2. If the voltage at TP2 does not change about as shown in Table 8-29 for specified CF's, or does not change at all, check Q2, Q4, Q6 and associated components.

If the voltage at TP2 varies approximately as shown in Table $8-19$, but the frequency at XA17-12 does not step (or there is no RF output), refer to Test Procedure 1 and check the oscillator circuits.

## SERVICE SHEET 8 (Cont'd)

If the voltage at TP2 varies approximately as shown in Table 8-29 and the frequency readout of the counter approximately follows the table ( $\pm 20-30 \mathrm{kHz}$ ) check Q8 and associated components.

Table 8-45. N1 Oscillator Test Point Measurements

| Center <br> Frequency MHz | Frequency <br> At TP3 kHz | Voltage at <br> TP1 | Voltage at <br> TP2 |
| :---: | :---: | :---: | :---: |
| 0000.100000 | 29600.000 | -25.2 v | -29.2 v |
| 0000.100000 | 29600.000 | -25.0 v | -28.7 v |
| 0000.200000 | 29500.000 | -24.8 v | -28.2 v |
| 0000.300000 | 29400.000 | -24.6 v | -27.7 v |
| 0000.400000 | 29300.000 | -24.4 v | -27.1 v |
| 0000.500000 | 29200.000 | -24.2 v | -26.6 v |
| 0000.600000 | 29100.000 | -24.0 v | -26.2 v |
| 0000.700000 | 29000.000 | -23.8 v | -25.7 v |
| 0000.800000 | 28900.000 | -23.6 v | -25.2 v |
| 0000.900000 | 28800.000 | -23.4 v | -24.7 v |
| 0001.000000 | 28700.000 | -23.2 v | -24.3 v |
| 0002.000000 | 27700.000 | -21.2 v | -20.2 v |
| 0003,000000 | 26700.000 | -19.2 v | -16.6 v |
| 0004,000000 | 25700.000 | -17.2 v | -13.6 v |
| 0005.000000 | 24700.000 | -15.2 v | -11.9 v |
| 0006.000000 | 23700.000 | -13.2 v | -8.9 v |
| 0007.000000 | 22700.000 | -11.2 v | -7.1 v |
| 0008.000000 | 21700.000 | -9.2 v | -5.6 v |
| 0009.000000 | 20700.000 | -7.1 v | -4.3 v |
| 0009.900000 | 19800.000 | -5.3 v | -3.4 v |

A17


Figure 8-28. A17 N1 VCO Component Locations


## SERVICE SHEET 9

## N2 PHASE DETECTOR ASSEMBLY A14

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A14 assembly, a part of the two-assembly N2 phase lock loop is shown schematically and described on this Service Sheet. The N2 Oscillator assembly, A13, is shown schematically and described on Service Sheet 10.
When trouble has been isolated to the A14 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

NOTE
After making repairs in any part of the N2 loop circuits the adjustment
After making repairs in any part of the N2 loop circuits the adjustment
procedures specified in Section V paragraph 5-30 should be performed
to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes) Digital Voltmeter
Frequency Counter

## N2 LOOP GENERAL INFORMATION

The purpose of the N2 loop is to generate digitally controlled RF signals in the range of 19.80 to 29.79 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the re ference section. The RF output from the N2 loop is applied to Summing Loop 2.

## 1 PROGRAMMABLE DIVIDER CIRCUIT

All of the integrated circuits in the A14 assembly are used to count down the input from the N 2 voltage controlled oscillator.
When there is no BCD input to U5, U6 and U7 (all inputs low) the input from the oscillator will be 29.79 MHz ; the programmable divider will divide by 2979 to provide a 10 kH output. U5, U6 and U7 may be preset by CF digits 3,4 and 5 and programmed to vary between counts of 1980 and 2979 . Operation of the circuit is as follows:
Assume that initially there are no BCD inputs to U5, U6 and U7 (divide-by-ten decades) and they have all been preset to zero.
At the start of every count cycle, regardless of the BCD input, U1A pin $6(\bar{Q})$ and U1B pin 8 $\overline{(\bar{Q}) \text { are both low; U3 pin } 6(\bar{Q}), \mathrm{U} 4 \mathrm{~A} \operatorname{pin} 6(\overline{\mathrm{Q}}) \text { and U4B pin } 8(\overline{\mathrm{Q}}) \text { are all high. }}$
NAND gate U8C functions as a Schmitt trigger and provides pulses derived from the N2 voltage controlled oscillator output to clock U7 when AND gate U2B is enabled. U7 provides a divide-by-ten output to clock U6 and also provides A and C (binary 1 and 4 outputs to J inputs of JK flip-flop U3. The A and C outputs have no effect on U3 until the count down reaches 2975.
U6 provides a divide-by-ten output to clock U5 and also provides A, B and C (binary 1,2 and 4) outputs to AND gates U2A and U2C. The A, B and C outputs have no effect on the and 4) outputs to AND gates 2970 is reached.

U5 provides a divide-by-ten output to clock U1A and also provides A and D outputs to NAND gate U8A. The A and D (binary 1 and 8 ) outputs have no effect on the circuit unti the count down has reached 2900.
The D output of U5 (pin 12) goes low on the 1000th pulse input to U7 pin 8 and clocks U 1 A. One thousand input cycles later U1A is again clocked and the negative-going $\bar{Q}$ output

## SERVICE SHEET 9 (Cont'd)

of U1A (pin 6) clocks U1B. When U1B $\bar{Q}$ goes high it provides a high to AND gate U2A. The count down has reached 2000.
When the count down reaches 2900 , U5 A and D outputs are high NAND gate U8A pin 3 goes low and NAND gate U8B pin 6 goes high.

When the count down reaches 2970, U6 A, B and C outputs are high The B and C outputs are applied to AND gate U2C pins 10 and 11 and since U2C pin 9 has been high since the count of 2900 , U2C pi 8 goes high. The U6A output is applied to AND gate U2A, and since the other two inputs to U2A are high, U2A pin 12 goes high and i

When the count down reaches 2975, U7 A and C high outputs are applied to U3 J input pins 4 and 5 . Since U3 J pin 3 is now held high, the next input pulse from U8C will clock U3. Coun coincidence at 2975 cycles has been achieved.
When the count down reaches 2976 , U3 is clocked and the U3 $\bar{Q}$ output goes low. When $\mathrm{U} 3 \overline{\mathrm{Q}}$ goes low, AND gate U2B is no longer enabled; the count, as far as U7, U6, U5 and U1 are concerned is ended. When $\mathrm{U} 3 \overline{\mathrm{Q}}$ goes low it also sets U 4 A and U 4 B ; the $\overline{\mathrm{Q}}$ outputs go low and the $Q$ outputs go high. When the $\bar{Q}$ output of U4B goe ow it presets U7, U6, U5 and U1. When U7, U6, U5 and U1 are preset the $J$ inputs to U3 are inhibited since the count is no longer at the coincident count of 2975 .
When the U4B Q output goes high the leading edge of the pulse is used to generate the sampler pulse. The first pulse to the sampling phase detector is initiated by the 2976th input cycle. Since three more cycles are required to restart the count cycle, following sample pulses will be 2979 cycles apart.

When the count down reaches 2977 , U3 is again clocked and since the $K$ input is high and the $J$ input is low, $Q$ will go high. This $Q$ high applied to the K input of U4A and to pin 4 of AND gate U 2 B . U2B will not be enabled because U4B $\bar{Q}$ is holding AND gate U2B pin 5 low.
When the count down reaches 2978 U4A is clocked because the K input is high. U4A $\bar{Q}$ goes high and is applied to the $K$ input of U4B. On the 2979 th input cycle, U4B is clocked and the $\bar{Q}$ output goes high. When U4B $\bar{Q}$ goes high the preset pulse is ended and AND gat U2B is enabled. The next input cycle will initiate the count cycle.

When there is a preset input programmed into U7, U6 and U5, the terminal count is still 2979. However, the count down starts at the umber programmed into the BCD inputs. As an wample, if the binary input to U7 U6 and U5 is 999 the first input cycle would cause the same digital circuit changes that the 1000th input cycle caused in the discussion above (U1A would be clocked for the first time). The frequency division would be 2979 minus 999 , equal to division by 1980. The phase lock loop operation would result in an nput frequency to the programmable divider of 19.80 MHz . When the 19.80 MHz is divided by 1980 the divider output would again be 10 kHz .

The output from U4B is always 10 kHz when the oscillator is phas ocked.

## SERVICE SHEET 9 (Cont'd)

## TEST PROCEDURE

Composite Waveform SS9-1 illustrates the proper timing relationship between the 100 kHz reference input, the pulse output from the pulse generator and the sampling point on the 100 kHz reference signal when the loop is phase locked.

## NOTE

Center frequency is initially set to zero.

Test 1-a. Use the counter and the oscilloscope to check for a 100.000 kHz sine wave at approximately 5 volts $\mathrm{p} / \mathrm{p}$ at TP5. The display should be similar to that shown in the second trace from the top in composite waveform SS9-1.

If the correct signal is present, proceed to test 1-b
If the counter readout is 100.000 kHz but the sine wave is distorted, check Q1, Q2 and associated components.

If the signal is not present, connect the counter and the oscilloscope to XA14-1-2. The counter readout should be 100.000 kHz and the oscilloscope display should be similar to that shown in the top trace of composite waveform SS9-1.

If the correct signal is observed but was not observed at TP5, check Q1, Q2 and associated components.

If the signal is not present at XA14-1-2 check interconnections to the reference loop and, if necessary, the reference loop.


Test 1-b. Connect the oscilloscope and the counter to TP4. The counter readout should be 10.000 kHz and the oscilloscope should display positive-going pulses as shown in composite waveform SS9-1 at about 7 volts amplitude.

If the signal is not present proceed to test 1-c. If the signal is present connect the oscilloscope to the junction of R19 and C21. The oscilloscope display shour of composite waveform SS9-1.

If the programmable divider and the pulse generator are working properly but the loop is not phase locked, the oscilloscope may stil show the signals, but the relationship between the pulses and the sine wave will not be the same as shown in composite waveform SS9-1. If the voltage controlled oscillator and the summing circuits in the A13 assembly

Test 1-c. If the pulses are not present at TP5, and the counter count randomly or not at all, connect the oscilloscope to TP3. The oscilloscope should display pulses at approximately 10 kHz and about $3.5 \mathrm{v} \mathrm{p} / \mathrm{p}$.

If the pulses are present at TP3, but were not present at TP4, check Q6, Q7 and associated components.

If the pulses are not present at TP3 proceed to test 1-d.
Test 1-d. If the pulse is not present at TP3 connect the oscilloscop to U2B pin 6. The waveform should be similar to that shown in the op trace of composite waveform SS9-2. If the signal is as show proceed to test $1-\mathrm{e}$.

If there is no signat present at AND gate U2B pin 6 connect the oscilloscope to TP1. The waveform should be similar to that shown in the center trace of composite waveform SS9-2. If the signal is now present, use the digital voltmeter to check the voltage at AND gate U2B pins 4 and 5 . The digital voltmeter should indicate about +3 . volts; if it does, U2B is defective.

If the voltages are not present at AND gate U2B pins 4 and 5 , ground U3B pin 2. If the voltages now appear at AND gate U2B pins 4 and and the signal appears at U2B pin 6, U2B is functioning properly; the trouble is probably in the gating circuits to U3.
If the voltage is present at AND gate U2B pin 4 with U3 pin 2 grounded, but is not present at U2B pin 5, U4 is probably defective. If the voltages are not present at AND gate U2B pins 4 or 5 with U3 pin 2 grounded, U3 is probably defective.

If the signal is not present at TP1, use the oscilloscope to check the voltage controlled oscillator input at XA14-2-15. The display should be similar to the lower trace in composite waveform SS9-2. If the signal is present NAND gate U8C is probably defective. If the signal is not present check interconnections to the A13 assembly and, if necessary, the A13 assembly


Composite Waveform SS9-2

Test 1 e. It is assumed in this test that the signal input is present at U7 pin 8 only because U3 pin 2 is grounded. Composite waveforms SS9-3 through SS9-7 illustrate the correct waveforms for the integrated circuits in the programmable divider loop. All waveform are about 4.5 volts in amplitude. Follow the numerical sequence of the waveforms; when an IC output is missing the trouble is found Replace the defective component, remove the ground from U3 pin 2
and repeat test 1-b.

Composite waveform SS9-8 illustrates the proper waveforms for U3 under normal operating conditions.

## NOTE

Composite waveforms SS9-7 and SS9-8 waveform pictures were taken with the oscilloscope being triggered from TP3 and the oscilloscope sweep magnified X10



Composite Waveform SS9-4


Composite Waveform SS9-5


A14


Figure 8-30. A14 N2 Phase Detector Component Locations

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## SERVICE SHEET 9 (Cont'd)



Composite Waveform SS9-7


Composite Waveform SS9-8

## SAMPLING PHASE DETECTOR

The positive-going output from U4B pin 9 is used to generate the pulse required to open the sampler gate. Common base amplifier Q6 and emitter follower Q7 amplifies and couples the pulse to T1. CR1 and CR2 are used to minimize transformer flyback action. CR2 also bypasses the negative-going pulse around the transformer primary to ensure that only the positive-going pulse is coupled to the transformer secondary.
A 100 kHz signal from the reference loop is applied to the secondary center tap of T1. L7 and C9 (along with C3 in the reference loop A4A1 assembly) comprise a low pass filter; it has an impedance of about 450 ohms and a cutoff frequency of about 150 kHz . The TTL input from the reference loop is reshaped into a sine wave by the low pass filter. L8 and C14 comprise a tuned circuit which bypasses unwanted high frequency signals and further filters the sine wave.
Sampler diodes CR3 and CR4 are normally reverse biased. When the sampling pulse appears across the secondary of T1 it is coupled through C20 and C21 to pulse appears across the secondary of T1 it is coupled through C20 and C21 to
forward bias CR3 and CR4. Since the gate pulses are equal in amplitude but opposite in polarity, they will cancel at TP6.

While CR3 and CR4 are forward biased the sampling gate is open and the 100 kHz reference signal is sampled.

## SERVICE SHEET 9 (Cont'd)

This type of sampling phase detector may be phase locked at virtually any point on the sine wave curve Ideally, the zero volt crossover point of the sine wave should be used to improve the lock and hold in capability of the loop.

If the divided down output of the voltage controlled oscillator in the A13 assembly ( 10 kHz pulses) is not phase locked to the 100 kHz reference signal an ac signal is developed at TP6. The polarity of the signal at any given time depends on the polarity of the 100 kHz sine wave at the time the last sample was taken. The amplitude of the signal at any given time depends on what portion of the sine wave the last sample was taken from. Each time CR3 and CR4 are forward biased the signal derived from the 100 kHz reference signal at T1 terminals 4 and 6 are coupled through the sampling gate to control the charge on C22.

When the sampling gate pulse ends, CR3 and CR4 are again reverse biased and the sampling gate is closed. Since Q4 is a high input impedance device, the charge will remain in C22 until the next sampling pulse. The error signal from Q4 is applied to the summing amplifier in the A13 assembly through emitter followers Q3 and Q5.

Test Point 8 may be grounded to open the phase lock loop. Since the emitter of A13Q12 in the A13 assembly is also exactly at dc ground level, grounding this test point will not affect the pretuning circuit. With the loop open both the pretuning and the error signal may be checked.

## TEST PROCEDURE 2

Test 2-a. Connect the oscilloscope to TP6. If the 100 kHz reference signal is present one of the sampling gate diodes (CR3 or CR4) is probably shorted. If the gate pulse are present one of the sampling gate diod is probably open (Negative-going pulses CR4 - positive going pulses CR3). Proceed to test 2-b

Test 2-b. With the oscilloscope connected to TP6, ground TP8. The signal displayed should be similar to that shown in Composite Waveform SS9-9, at about 4 volts. The frequency of the signal will be determined by the frequency difference detected by the sampling gate (typically 200 to 400 Hz ).

If the signal is present at TP6, connect the oscilloscope to Q5-e. The sine wave should be about the same as that shown for TP6 except that the sampling points will not be as obvious.

If the signal is present at Q5-e the error amplifier and the sampling circuits are functioning properly.
If the signal is not present at Q5-e and was present at TP6, check Q3, Q4, Q5 and associated components. After repairs are made repeat the test and remove the ground from TP8.

## NOTE

Operation of the circuit shown on Service Sheet 9-a is essentially the same as that shown on Service Sheet 9. Reference designations differ. The count down is always 3000.


Waveform SS9-9

A14a


Figure 8-32. A14a N2a Phase Detector Component Locations


## SERVICE SHEET 10

## N2 OSCILLATOR ASSEMBLY A13

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A13 assembly, a part of the two-assembly N2 phase lock loop is shown schematically and described on this service sheet. The N2 Phase Detector assembly, A14, is shown schematically and described on Service Sheet 9.

When trouble has been isolated to the A13 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the N2 loop circuits the adjustment procedures specified in Section V paragraph 5-30 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Digital Voltmeter
Frequency Counter

## N2 LOOP GENERAL INFORMATION

The purpose of the N 2 loop is to generate digitally controlled RF signals in the range of 19.80 to 29.79 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section. The RF output of the N2 loop is applied to Summing Loop 2.

## VOLTAGE CONTROLLED OSCILLATOR

Varactors CR8 and CR9, transistors Q2 and Q9 and associated components comprise a voltage controlled oscillator. Two varactors are used in parallel to provide high Q as well as the wide capacitance range required. C18 provides isolation for the dc levels required to bias the varactors. C17 provides the feedback required to sustain oscillation. The resonant tank circuit is coupled to Q9 by means of capacitive divider C22 and C23. The FET acts as a source follower in the feedback circuit; it provides a high impedance at the gate and a low impedance at the source. The gain of the FET amplifier for the output signal is less than one; this minimizes the Miller effect which might otherwise reflect capacitance back into the oscillator tank circuit

Q1 amplifies the signal and applies it to U1A which functions as a Schmitt trigger. U1D inverts the output from U1A and applies it to the programmable divider in the A14 assembly. U1C inverts the output from U1A and applies it to the divide-by-one hundred circuit in Summing Loop 2.

## TEST PROCEDURE

## NOTE

Do not use long coax leads from the counter to $T_{P}^{4} 3$. The capacitive loading may attenuate the signal below a useable level.

## SERVICE SHEET 10 (Cont'd)

Test 1-a. Connect the counter to TP3 and set Center Frequencies as shown in Table 8-5. The counter readout should be as shown in the table. (Make allowances for counter accuracy.)

## NOTE

If the frequency readouts listed in Table 8-30 are not approximately as shown check the voltage levels shown for TP2 in Table 8-30. If the voltage levels are incorrect proceed to test procedure

If the signal is present use the oscilloscope to check the outputs at XA13-1 pins 4 and 6 with center frequency set to zero. The signal at XA13-1-4 should be about 0.8 volt $\mathrm{p} / \mathrm{p}$ and the signal at XA13-1-6 should be about 0.3 volt.

If the signal is present at TP3 but is not present at XA13-1 pins 4 and 6 check U1.
Test 1-b. If the signal is not present at TP3 use the oscilloscope to check the signal at the collector of Q1. The signal should be about 1 volt in amplitude.
If the signal is not present at Q1-c use the oscilloscope to check the signal at the Q1 base. If the signal is now present (about 0.3 volt), Q1 is probably defective

If the signal is not present at Q1 base, check Q2, Q9 and associated components.

## PRETUNING CIRCUIT

The frequency of the voltage controlled oscillator is roughly preset by the digital to analog converter (U2, U3, transistors connected to the outputs of the NAND gates and associated components). The digital to analog converter cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the loop. The inputs to U2 and U3 are BCD bits coded 8, 4, 2 and 1 . When any of the BCD inputs are high they cause the output of the NAND gate with which they are associated to go low; the transistor associated with the NAND gate is switched on.

When all of the BCD inputs are low Q4 is biased to provide approximately - 25 volts at TP1 (Q3-e). With this dc level at TP1 the oscillator is roughly preset to 29.79 MHz .

When any one or more of the BCD inputs go high the transistor associated with it saturates and draws current through R34 and R35. The change in bias for Q4 causes the voltage at TP1 to go less negative (closer to ground level). Finally when the binary input is 99 , the voltage at TP1 is approximately -5.2 volts and the oscillator frequency is roughly preset to 19.80 MHz .
Q12 is a summing amplifier which combines the output of the digital to analog converter and the signal from the N2 phase detector. The summing point (Q12-e) sums the current from three sources; a current source from the +20 volt supply through R28, R30 and R37, a negative source from the digital to analog converter (TP1) and the signal from the N2 phase detector. The voltage at the summing point is always zero volts.

When TP1 is at approximately -25 volts (no BCD input), most of the current from the +20 volt supply flows through Q4 and Q3; very little flows through Q12. Under these conditions the voltage at Q12-c is about - 30 volts. As the voltage at TP1 decreases (gets closer to ground level) less current flows through Q4 and Q3, more current flows through Q12, and the Q12 collector voltage decreases.

N2a Phase Detector
SERVICE SHEET 9A

## SERVICE SHEET 10 (Cont'd)

Test 1-a. Connect the counter to TP3 and set Center Frequencies as shown in Table 8-5. The counter readout should be as shown in the table. (Make allowances for counter accuracy.)

## NOTE

If the frequency readouts listed in Table 8-30 are not approximately as shown check the voltage levels shown for TP2 in Table 8-30. If the voltage levels are incorrect proceed to test procedure

If the signal is present use the oscilloscope to check the outputs at XA13-1 pins 4 and 6 with center frequency set to zero. The signal at XA13-1-4 should be about 0.8 volt $\mathrm{p} / \mathrm{p}$ and the signal at XA13-1-6 should be about 0.3 volt.

If the signal is present at TP3 but is not present at XA13-1 pins 4 and 6 check U1.
Test 1-b. If the signal is not present at TP3 use the oscilloscope to check the signal at the collector of Q1. The signal should be about 1 volt in amplitude.
If the signal is not present at Q1-c use the oscilloscope to check the signal at the Q1 base. If the signal is now present (about 0.3 volt), Q1 is probably defective.

If the signal is not present at Q1 base, check Q2, Q9 and associated components.

## 2 PRETUNING CIRCUIT

The frequency of the voltage controlled oscillator is roughly preset by the digital to analog converter (U2, U3, transistors connected to the outputs of the NAND gates and associated components). The digital to analog converter cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the loop. The inputs to U 2 and U 3 are BCD bits coded $8,4,2$ and 1. When any of the BCD inputs are high they cause the output of the NAND gate with which they are associated to go low; the transistor associated with the NAND gate is switched on.

When all of the BCD inputs are low Q 4 is biased to provide approximately -25 volts at TP1 (Q3-e). With this dc level at TP1 the oscillator is roughly preset to 29.79 MHz .

When any one or more of the BCD inputs go high the transistor associated with it saturates and draws current through R34 and R35. The change in bias for Q4 causes the voltage at TP1 to go less negative (closer to ground level). Finally when the binary input is 99 , the voltage at TP1 is approximately -5.2 volts and the oscillator frequency is roughly preset to 19.80 MHz .
Q12 is a summing amplifier which combines the output of the digital to analog converter and the signal from the N 2 phase detector. The summing point (Q12-e) sums the current from three sources; a current source from the +20 volt supply through R28, R30 and R37, a negative source from the digital to analog converter (TP1) and the signal from the N2 phase detector. The voltage at the summing point is always zero volts.
When TP1 is at approximately -25 volts (no BCD input), most of the current from the +20 volt supply flows through Q4 and Q3; very little flows through Q12. Under these conditions the voltage at Q12-c is about -30 volts. As the voltage at TP1 decreases (gets closer to ground level) less current flows through Q4 and Q3, more current flows through Q12, and the Q12 collector voltage decreases.

## SERVICE SHEET 10 (Cont'd)

CR4 through CR7, CR11 through CR16 and associated resistors are used to shape the voltage applied to the varactors in the voltage controlled oscillator circuit so that the frequency will be linear with the voltage change. The voltage at the junction of R42 and R47 is about - 27.5 volts. When there is no BCD input (Q12-c is about - 30 volts) all of the diodes in the shaper are reverse biased. As the voltage at TP1 decreases (gets closer to -5.2 volts) current through Q12 increases and the Q12 collector voltage also decreases. As the Q12-c voltage decreases first CR4, then CR5, etc. are forward biased. As the diodes are forward biased resistors are added in parallel with R31 and R32 to shape the voltage curve to the varactors

Q11 and Q10 are emitter followers which couple the output of Q12 to the varactors. Q11 provides a high impedance for the output of the summing amplifier, Q12.

## TEST PROCEDURE 2

Test 2-a. Use the digital voltmeter to check the voltages at TP1 and TP2. These dc levels should be about as shown in Table 8-30 for the center frequencies shown.

If the voltages at TP1 are about right, but those at TP2 are not, check Q12, Q11, Q10 and associated components.

If the voltages at TP1 are not approximately as shown in Table 8-46, check the components in the digital to analog converter.

## NOTE

Also check the BCD input lines for the correct levels. With CF digits 4 and 5 set to a zero all eight input lines should be low. With CF digits 4 and 5 set to a 1 inputs at XA13-2 pins 11 and 9 should be high, etc.

Table 8-46. N2 Frequency Versus Voltage Chart

| Center Frequency | Counter Readout | TP1 Volts | TP2 Volts |
| :---: | :---: | :---: | :---: |
| 00000 Hz | 29.790000 MHz | -25 | -31 |
| 11100 Hz | 28.680000 MHz | -23 | -26 |
| 22200 Hz | 27.570000 MHz | -21 | -21 |
| 33300 Hz | 26.460000 MHz | -18.5 | -16.8 |
| 44400 Hz | 25.350000 MHz | -16.4 | -13.4 |
| 55500 Hz | 24.240000 MHz | -14.2 | -10.6 |
| 66600 Hz | 23.130000 MHz | -12 | -8.3 |
| 77700 Hz | 22.020000 MHz | -9.8 | -6.4 |
| 88800 Hz | 20.910000 MHz | -7.7 | -4.8 |
| 99900 Hz | 19.800000 MHz | -5.4 | -3.6 |

N2a Phase Detector
SERVICE SHEET 9A

## A13




## SERVICE SHEET 11

## N3 PHASE DETECTOR ASSEMBLY A10

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.
The A10 assembly, a part of the two-assembly N3 phase lock loop is shown schematically and described on this service sheet. The N3 oscillator assembly, A8, is shown schematically and described on Service Sheet 12.
When trouble has been isolated to the A10 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the N3 loop circuits the adjustment procedures specified in Section V paragraph 5-31 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes) Digital Voltmeter
Frequency Counter

## N3 LOOP GENERAL INFORMATION

The purpose of the N3 loop is to generate digitally controlled RF signals in the range of 20.01 to 21.00 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section.
The RF output of the N 3 voltage controlled oscillator is divided by ten before being applied to the SL2 assembly. The output to SL2 is 2.001 to 2.100 MHz in 1 kHz increments.

## 1 N3 PROGRAMMABLE DIVIDER CIRCUI

All of the integrated circuits in the A10 assembly are used to count down the input from the N3 voltage controlred oscillator.
When there are no BCD inputs to U 5 and U 6 (all inputs low), the input from the oscillator will be 21.00 MHz when the oscillator is phase locked; the programmable divider will divide by 2100 to provide a 10 kHz output at TP3. U5 and U6 are preset by CF digits 1 and 2 and programmed to vary between start counts of 00 and 99 . Operation of the circuit is as follows:

Assume that initially all BCD inputs are low and $\mathrm{U} 4, \mathrm{U} 5$ and U 6 have been preset to zero. Assume also that U2A pin $6(\overline{\mathrm{Q}})$ and U2B pin $8(\overline{\mathrm{Q}})$ are both low. U1B pin $8(\overline{\mathrm{Q}})$ and U1A pin $6(\bar{Q})$ are both high.
NAND gate U7C couples the input from the N3 oscillator to the clock input of U5. U5 provides a divided-by-ten output to clock U6 and also provides A, B and C (BCD 1, 2 and 4) outputs. The A, B and C outputs are not used until the count of 2097 has been reached.
U6 provides a divided-by-ten output to clock U4 and also provides A and D (BCD 1 and 8) outputs to AND gates U3A and U3C. The A and D outputs are not used until the count has reached 2090.

U4 provides a divided-by-ten output to clock U2A. At the count of 1000 U4 clocks U2A and the U2A Q output at pin 6 goes high. At the count of 2000 U4 again clocks U2A and the regative-going $\bar{Q}$ output at pin 6 clocks U2B. When U2B is clocked $\bar{Q}$ at pin 8 goes high and is applied to pins 2 and 13 of AND gate U3A.
At the count of 2090 the high A and D outputs of U6 are applied to AND gates U3A and U3C. Since U3A pins 2 and 13 are both high, U3A is enabled and it places a high on pin 11 of AND gate U3C.

## SERVICE SHEET 11 (Cont'd)

At the count of 2097 the high A, B and C outputs of U5 are applied to AND gates U3B and U3C to provide a high at the J input of U1B at pin 11 .
At the count of 2098 U1B is clocked, U1B $\bar{Q}$ (pin 8) goes low and sets U1A. U1A $\bar{Q}$ (pin 6) goes low and presets U2, U4, U5 and U6; they are held in preset until the count is completed.
When U1A is set Q (pin 5 ) goes high and initiates the sampling pulse. The first pulse to the sampling phase detector is initiated by the 2098 th input cycle. Since two more cycles are required to restart the pulses are 2100 cycles apart when there is no BCD input.
At the count of 2099 U1B is again clocked and $\bar{Q}$ (pin 8) goes high The high at pin 8 is applied to the $K$ input of U1A (pin 2).
At the count of 2100 U 1 A is clocked and pin $6 \overline{\mathrm{Q}}$ goes high to end the preset pulse. The next input to U5 initiates the next count cycle When there is a BCD input programmed into U5 and U6 pins $3,4,10$ and 11 the terminal count in the BCD inputs. As an count if the BCD input to U5 and U6 is 99 the first input cycle would cause the same digital circuit changes that the 100th input cycle caused in the discussion above (U4 would be clocked). The frequency division would be $2100-99$, equal to division by 2001 . The phase lock loop operation would result in an input frequency to the programmable divider of 20.01 MHz . When divided by 2001 , the divider output at TP3 would again be 10 kHz .
The output from U1A pin 5 is always 10 kHz when the oscillator is phase locked regardless of the oscillator frequency.

## TEST PROCEDURE 1

Composite Waveform SS11-1 illustrates the proper timing relationship between the 100 kHz reference input, the pulse output from the pulse generator and the sampling point on the 100 kHz reference signal when the loop is locked.

## NOTE

Center Frequency is initially set to zero.
Test 1-a. Use the counter and the oscilloscope to check for a 100.000 kHz sine wave at approximately $5 \mathrm{volts} \mathrm{p} / \mathrm{p}$ at TP5. The display should be similar to that shown in the second trace from the top of composite waveform SS11-1.


## SERVICE SHEET 11 (Cont'd)

If the counter readout is $100,000 \mathrm{kHz}$ but the sine wave is distorted check Q1, Q2 and associated components.
If the signal is not present, connect the counter and the oscilloscope to XA10-1-2. The counter readout should be 100.000 kHz and the oscilloscope display should be similar to that shown in the top trace of composite waveform SS11-1.
If the correct signal is present at XA10-1-2, but was not present at TP5, check Q1, Q2 and associated components.

If the signal is not present at XA10-1-2 check interconnections to the reference loop and, if necessary, the reference loop.
Test 1-b. Connect the oscilloscope and the counter to TP4. The counter readout should be 100.000 kHz and the oscilloscope should display positive-going pulses as shown in composite waveform SS11-1 test 1-c
If the signal is present, connect the oscilloscope to the junction of R19 and C20. The oscilloscope display should be similar to that shown in the lowest trace of composite waveform SS11-1.
If the programmable divider and the pulse generator are working properly but the loop is not phase locked, the oscilloscope may still display the signals at the junction of R19 and C20, but the same as shown in composite waveform SS11-1. If the voltage controlled oscillator and the summing circuit in the A8 assembly are known to be functioning properly, proceed to test procedure 2 .

Test 1-c. If the pulses are not present at TP4, and the counter count randomly or not at all, connect the oscilloscope to TP3. The oscilloscope display should be a series of pulses at approximately 10 kHz and about 4 volts in amplitude.
If the pulses are present at TP3, but were not present at TP4, check Q6, Q7 and associated components.
If the pulses are not present at TP3, proceed to test 1-d.
Test 1-d. If the pulse is not present at TP3 connect the oscilloscope to NAND gate U7C pin 8. The oscilloscope should display a slightly distorted sine wave at about 21 MHz and about 3 volts in amplitude.

If the signal is not present at U7C pin 8, connect the oscilloscope to XA10-2-15. The 21 MHz signal should be about 0.06 volt in amplitude. If the signal is present, U7 is probably defective. If the signal is not present check in
if necessary the A8 assembly.

Test 1 -e. It is assumed in this test that the signal input is present a U5 pin 8. Composite waveforms SS11-2 through SS11-6 illustrate the correct waveforms for the integrated circuit points shown.

## NOTE

These waveforms were taken with the oscilloscope triggered from TP3

## SERVICE SHEET 11 (Cont'd)

If the counter readout is $100,000 \mathrm{kHz}$ but the sine wave is distorted, check Q1, Q2 and associated components.

If the signal is not present, connect the counter and the oscilloscope to XA10-1-2. The counter readout should be 100.000 kHz and the oscilloscope display should be similar to that shown in the top trace of composite waveform SS11-1.

If the correct signal is present at XA10-1-2, but was not present at TP5, check Q1, Q2 and associated components
If the signal is not present at XA10-1-2 check interconnections to the reference loop and, if necessary, the reference loop.
Test 1-b. Connect the oscilloscope and the counter to TP4. The counter readout should be 100.000 kHz and the oscilloscope should display positive-going pulses as shown in composite waveform SS11-1 at about 7 volts amplitude. If the signal is not present, proceed to test 1-c.

If the signal is present, connect the oscilloscope to the junction of R19 and C20. The oscilloscope display should be similar to that shown in the lowest trace of composite waveform SS11-1.
If the programmable divider and the pulse generator are working properly but the loop is not phase locked, the oscilloscope may still display the signals at the junction of R19 and C20, but the elationship between the pulses and the sine wave will not be the relationship between the pusite waveform SS11-1. If the voltage controlled oscillator and the summing circuit in the A8 assembly are known to be functioning properly, proceed to test procedure 2

Test 1-c. If the pulses are not present at TP4, and the counter counts randomly or not at all, connect the oscilloscope to TP3. The oscilloscope display should be a series of pulses at approximately 10 kzz and about 4 volts in amplitude.
If the pulses are present at TP3, but were not present at TP4, check Q6, Q7 and associated components.

If the pulses are not present at TP3, proceed to test 1-d.
Test 1-d. If the pulse is not present at TP3 connect the oscilloscope to NAND gate U7C pin 8. The oscilloscope should display a slightly distorted sine wave at about 21 MHz and about 3 volts in amplitude.
f the signal is not present at U7C pin 8, connect the oscilloscope to A10-2-15. The 21 MHz signal should be about 0.06 volt in amplitude. If the signal is present, U7 is probably defective. If the signal is not present check interconnections to the A8 assembly and, if necessary the A8 assembly.

Test 1-e. It is assumed in this test that the signal input is present at U5 pin 8. Composite waveforms SS11-2 through SS11-6 illustrate the correct waveforms for the integrated circuit points shown.

## NOTE

These waveforms were taken with the oscilloscope triggered from TP3.

SERVICE SHEET 11 (Cont'd)
SERVICE SHEET 11 (Cont'd)

Follow the numerical sequence of the waveforms shown; when an IC output is missing the trouble is found. Replace the defective component and repeat test 1-b. center the pulses shown. probably defective.

U6 pin 12 about 4.5 V

## NOTE

If the output from U5 is not present proceed to test 1-f before replacing $U 5$.
Test 1-f. Composite waveform SS11-7 illustrates correct waveforms for a properly operating U1. In this test the oscilloscope was again triggered by TP3 and the sweep delay of the oscilloscope was used to

If the waveforms in composite waveform SS11-7 cannot be observed (because an adequate oscilloscope is not available or other reasons) measure the voltage at U 1 pin 6 , it should be about +3.7 volts; U 1 pin 5 should be at about +100 millivolts. If the voltages are not as specified, ground U1 pin 10 . The voltages should then be; U1 pin 6 about +130 millivolts and U 1 pin 5 about +3.8 volts. If the voltages are as specified in either case and there is no output from U5, U5 is

If there is no change in the dc levels at U 1 pins 5 and 6 with U 1 pin 10 grounded U1 is probably defective.


Composite Waveform SS11-5


Composite Waveform SS11-4



Composite Waveform SS11-2

Composite Waveform SS11-6


Composite Waveform SS11-3

## SERVICE SHEET 11 (Cont'd)



Composite Waveform SS11-4


Composite Waveform SS11-5


Composite Waveform SS11-6
4

## SERVICE SHEET 11 (Cont'd)



Composite Waveform SS11-7

## SAMPLING PHASE DETECTOR

The positive-going output from U1A Q (pin 5) is used to generate the pulse required to open the sampler gate. Common base amplifier Q6 and emitter follower Q7 amplifies and couples the pulse to T1. CR1 and CR2 are used to minimize transformer flyback action. CR2 also bypasses the negative-going pulse around the transformer primary to ensure that only the positive-going pulse is coupled to the transformer secondary.

A 100 kHz signal from the reference loop is applied through Q2 and Q1 to the secondary center tap of T1. L 5 and C8 (along with C4 in the reference loop A4A1 assembly) comprise a low pass filter; it has an impedance of about 450 ohms and a cutoff frequency of about 150 kHz . The TTL input from the reference loop is reshaped into a sine wave by the low pass filter. Q2 and Q1 amplify the signal to the level required in the sampling phase detector. L7 and C13 comprise a tuned circuit which bypasses unwanted high frequency signals and further filters the sine wave.

Sampler diodes CR3 and CR4 are normally reverse biased. When the sampling pulse appears across the secondary of T1 it is coupled through C20 and C21 to forward bias CR3 and CR4. Since the gate pulses are equal in amplitude but opposite in polarity, they will cancel at TP6.

While CR3 and CR4 are forward biased the sampling gate is open and the 100 kHz reference input signal is sampled.

This type of sampling phase detector may be phase locked to virtually any point on the sine wave slope. Ideally, the zero crossover point of the sine wave should be used to improve the lock and lock hold capabilities of the loop.

If the divided down output of the voltage controlled oscillator ( 10 kHz pulses) is not phase locked to the 100 kHz reference signal an ac error signal will be developed at TP6. The polarity of the error signal at any given point in time depends on the polarity of the 100 kHz reference signal at the time the last sample was taken. The amplitude of the error signal at any given time depends on what part of the sine wave the last sample was taken from. Each time CR3 and CR4 are forward biased the 100 kHz reference signal at T1 terminals 4 and 6 are coupled through the sampling gate to control the charge on C22.

When the sampling gate pulse ends CR3 and CR4 are again reverse biased and the sampling gate is closed. Since Q4 is a high impedance input device, the charge will remain on C22 until the next sampling pulse. The current through Q4 is controlled by the difference in Gate-source voltage of the lower FET. Operation of the dual FET sets the output level at the lower FET drain to exactly the level at the upper FET gate. The output is coupled through two emitter followers to the summing amplifier in the A8 assembly.

## SERVICE SHEET 11 (Cont'd)

## TEST PROCEDURE

Test 2-a. Connect the oscilloscope to TP6. If the 100 kHz reference signal is present one of the sampling gate diodes (CR3 or CR4) is probably shorted. If the gate pulses are present one of the sampling gate diodes is probably open (Negative-going pulses CR4 - positive-going pulses CR3). Proceed to test 2-b.

Test 2-b. With the oscilloscope connected to TP6, ground TP8. The oscilloscope should display a low frequncy sine wave (about 4 volts) that varies in frequency. The frequency of the signal will be the difference frequency detected by the sampling gate.

If the signal is present at TP6, connect the oscilloscope to Q5-e. The sine wave should be the same as seen at TP6.

If the signal is present at Q5-e the error amplifier and the sampler circuit are functioning properly.
If the signal is not present at Q5-e and was present at TP6, check Q3, Q4, Q5 and associated components.


Figure 8-36. A10 N3 Phase Detector Component Locations


## SERVICE SHEET 12

## N3 OSCILLATOR ASSEMBLY A8

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A8 assembly, a part of the two-assembly N3 phase lock loop is shown schematically and described on this service sheet. The N3 Phase Detector assembly, A10, is shown schematically and described on Service Sheet 11.

When trouble has been isolated to the A8 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the N3 loop circuits the adjustment procedures specified in Section V paragraph 5-31 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Digital Voltmeter
Frequency Counter

## N3 LOOP GENERAL INFORMATION

The purpose of the N3 loop is to generate digitally controlled RF signals in the range of 20.01 to 21.00 MHz in selectable 10 kHz increments. The voltage controlled oscillator is phase locked to a 100 kHz reference which is derived from the master oscillator in the reference section. The RF output of the N3 voltage controlled oscillator is divided by ten before it is applied to summing Loop 2. The output from the N3 assembly to SL2 is 2.001 to 2.100 MHz in selectable 1 kHz increments.

## VOLTAGE CONTROLLED OSCILLATOR

Q2, Q7 and associated components comprise a voltage controlled oscillator. C14 and C17 provide isolation for the dc levels required to bias the varactor. C13 provides the feedback required to sustain oscillation. The resonant tank is coupled to Q7 by capacitive divider C16 and C17. The FET acts as a source follower in the feedback circuit; it provides a high impedance at the gate and a low impedance at the source. The gain of the FET for the output signal at the drain is held at less than unity to minimize the Miller effect which might otherwise reflect capacitance back into the oscillator tank circuit.

Q1 amplifies the voltage controlled oscillator output and applies it to U1A which functions as a Schmitt trigger. U1D provides the output to the N3 programmable divider in the A10 assembly. U1B and U3 provide a divided by ten output to Summing Loop 2.

## SERVICE SHEET 12 (Cont'd)

## TEST PROCEDURE

## NOTE

Do not use long coax leads from the counter to N3 test points. The capacitive loading may attenuate the signal below a useable level.

Test 1-a. Connect the counter to TP2. With the center freuqency set to zero the counter readout should be 21.00 MHz . Set CF digits 1 and 2 to the settings specified in Table 8-31. Frequency readouts on the counter should follow those specified in the table. (Make allowances for counter accuracy).

## NOTE

If the frequency readouts listed in Table 8-31 are not approximately as shown, check the voltage levels shown for TP3 in the table. If the voltage levels are incorrect proceed to test procedure 2

If the signal is present use the oscilloscope to check the signal at points shown in composite waveform SS12-1. Signals shown are about 4 volts in amplitude.


Composite Waveform SS12-1

If the signal is present at TP2 but is not present at U 1 pin 11 , U 1 is probably defective; if the signal is not present at U3 pin 12 , U1 or U3 may be defective.

If the signal is not present at TP2 use the oscilloscope to check for the signal at Q1-b. If the signal is present at Q1-b check Q1 and NAND gate U1A. If the signal is not present check Q2, Q7 and associated components.

## 2 PRETUNING CIRCUIT

The frequency of the voltage controlled oscillator is roughly preset by the digital to analog converter (U2 and Q8 through Q11). The digital to analog converter

## SERVICE SHEET 12 (Cont'd)

cannot, by itself, set the oscillator frequency precisely; it does set the frequency within the capture range of the phase lock loop. The inputs to U2 are BCD bits coded $1,2,4$ and 8 . When any one of the BCD inputs are high they cause the output of the NAND gate to which they are connected to go low; the transistor connected to the NAND gate output is switched on.

When all of the BCD inputs are low Q6 is biased to provide approximately -8.5 volts at TP1 (Q5-e). With this dc level at TP1 the oscillator is roughly preset to 21 MHz (how close depends on adjustment of R24 and R26).

When any one or more BCD inputs go high the transistor associated with it saturates and the current through Q6 is reduced. The reduction of current through Q6 changes the bias on Q5 and causes the voltage at TP1 to go less negative (closer to dc ground level). Finally, when the BCD input is 9 , the voltage at TP1 is approximately -6.7 volts and the oscillator is roughly preset to 20.01 MHz (again depending on adjustment of R24 and R26).

Q3 is a summing amplifier which combines the output of the digital to analog converter and the error signal from the N3 Phase Detector. The summing point (Q3-e) sums the current from three sources; a current source from the +20 volt power supply through R19, R25 and R26, a negative source from the digital to analog converter (TP1), and the error signal from the phase detector. The voltage at the summing point is always zero volts when the loop is locked.

The output from Q3 is coupled through Q4 and Q12 to control the bias on varactor CR5 and the frequency of the voltage controlled oscillator.

## TEST PROCEDURE 2

Test 2-a. Use the digital voltmeter to check the voltages at TP1 and TP3. These dc levels should be about as shown in Table 8-31 for the center frequencies shown.

## NOTE

These voltages are typical. They will vary from instrument to instrument because of differences in individual varactor characteristics.

If the voltages at TP1 are about right, but those at TP3 are not, check Q3, Q4, Q12 and associated components.

If the voltages at TP1 are not approximately as shown in Table 8-31, check the components in the digital to analog converter.

## SERVICE SHEET 12 (Cont'd

Table 8-47. N3 Frequency Versus Voltage Chart

| Center Frequency | Counter Readout | TP1 Voltage | TP3 Voltage |
| :---: | :---: | :---: | :---: |
| 00 Hz | 21.000000 MHz | -8.5 V | -3.7 V |
| 11 Hz | 20.890000 MHz | -8.3 V | -3.6 V |
| 22 Hz | 20.780000 MHz | -8.1 V | -3.5 V |
| 33 Hz | 20.670000 MHz | -7.9 V | -3.4 V |
| 44 Hz | 20.560000 MHz | -7.7 V | -3.3 V |
| 55 Hz | 20.450000 MHz | -7.5 V | -3.2 V |
| 66 Hz | 20.340000 MHz | -7.3 V | -3.1 V |
| 77 Hz | 20.230000 MHz | -7.1 V | -3.0 V |
| 88 Hz | 20.120000 MHz | -6.9 V | -2.9 V |
| 99 Hz | 20.010000 MHz | -6.7 V | -2.8 V |

## NOTE

Also check the dc levels at the BCD input lines.


Figure 8-38. A8 N3 VCO Component Locations


## SERVICE SHEET 13

## SUMMING LOOP 2 PHASE DETECTOR A12

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A12 assembly, a part of the two-assembly SL2, is shown schematically and described on this Service Sheet. The SL2 Oscillator Assembly (A11) is shown schematically and described on Service Sheet 14

When trouble has been isolated to the A12 assembly it should be removed and reinstalled When trouble has been isolated to the A12 assembly it should be removed and reinst
using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the SL2 circuits the adjustment procedures in Section $V$ paragraph 5-32 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes)

## Digital Voltmeter

Frequency Counter

## SUMMING LOOP 2 GENERAL

The purpose of Summing Loop 2 (SL2) is to generate digitally controlled RF signals in the range of 20.0001 to 30.0000 MHz in selectable 100 Hz increments. The difference frequency between the SL2 voltage controlled oscillator and the input from the N2 loop is phase locked to the divided-by-ten output of the N3 assembly. The output of SL2 is applied to SL1.

The portion of the pretuning circuit that appears on service sheet 13 (U8 and Q8 through Q11) is explained in the text for service sheet 14.

## 1 PHASE DETECTOR

There are three signal inputs to the phase detector assembly. They are the output of the N2 voltage controlled oscillator, the divided by ten output of the N3 voltage controlled oscillator and the output of the SL2 voltage controlled oscillator.

The N2 and SL2 signals are mixed and the difference frequency is used as one input to the digital phase detector. The second input to the digital phase detector is the divided by ten input from the N3 assembly.

The output of the N3 voltage controlled oscillator is divided by ten in the N3 assembly and The output of the N voltage controlled oscillator is divided by ten in the N assembly and
again divided by ten by U9. Q12 and NAND gate U7A shape the resulting pulses which vary in frequency (depending on programming to the N3 loop) from 0.2001 to 0.2100 MHz . The pulses at TP2 are negative-going.

## SERVICE SHEET 13 (Cont'd)

The inputs from the N2 loop and the SL2 voltage controlled oscillator are applied to double balanced mixer E1 R and L ports. The difference signal from the X port is amplified by Q5 and Q4 and
shaped by Q3, Q7 and NAND gates U4B and U4C. When the loop is phase locked the negative-going pulses at TP3 are at the same frequency as those at TP2. The pulses do not appear in time coincidence; they are received alternately.

U7B, U7D, U4A and U4D comprise a coincidence gate which inhibits signals that appear simultaneously at TP2 and TP3. Normally, when signals are not present, TP2 and TP3 are both high. When a signal
appears at TP2, U7B pin 6 and U4D pin 13 go high If there is no signal at TP3 U5D pin 12 is also high; U4D pin 11 goes low, and U1B pin 6 goes high. The positive pulse at TP5 drives the clock generator pin 6 goes high. The positive pulse at TP5 drives the clock generator U4A pin 3 and U7D pin 12 go high. If there is no signal at TP2, U7D pin 13 is also high; U7D pin 11 goes low, and U7C pin 8 goes high. The positive pulse at TP9 drives the clock generator and the sense circuit or the phase detector. When signals appear at TP2 and TP3 at the same time U7D pin 13 and U4D pin 12 go low, U7D pin 11 and U4D pin 11 remain high, and the signals cannot reach TP5 or TP9.

U1A, U1C, U1D and U5C comprise a clock generator which clocks U2A and U2B each time a signal appears at TP5 or TP9. With no U2A and U2B each time a signal appears at TP5 or TP9. With no signals present TP5 and TP9 are low. When a positive pulse appears at pulse appears at TP6. When a positive pulse appears at TP5 operation of the circuit is the same except that U1C pin 8 goes low (rather than U1A pin 3). Since a clock pulse is generated for each input, the pulse frequency at TP6 is the sum of the frequencies at TP5 and TP9.

Since the sense circuit does not function when the loop is locked, operation of the phase detector will be discussed first.

When the loop is phase locked U2A $\bar{Q}$ is held high to enable U3A and U3D. Assume that initially U2B $\bar{Q}$ is high, U3B pin 6 is low and U3C pin 8 is high. When a positive-going signal from TP9 appears at U3A pin 1, U3A pin 3 goes low and causes a change in state of flip-flop U2B pin thB pin 12 sets the flip/flop and the positive-going trailing edge of the clock pulse causes U2B Q to go high. The following positive pulse
from TP5 is applied to U3D pin 12, U3D pin 11 goes low and changes the state of flip/flop U3B/U3C. U3B pin 6 goes low and the clock pulse causes U2B $/ \mathrm{Q}$ to again go high. This sequence continues as long as the signals at TP5 and TP9 are received alternately.

The signals at TP5 and TP9 are applied to the sense circuit even when the loop is phase locked. They have no effect on the circuit because of the relationship of the $Q$ and $\bar{Q}$ outputs of $U 2 B$ to the incoming signals.

## SERVICE SHEET 13 (Cont'd)

When U2B Q is high NAND gates U6A and U6C are enabled. When the signal from TP5 appears at U6C pin 9, U6C pin 8 goes low; flip/flop U5A/U5B does not change state because U5B pin 3 is low. The signal at U6B has no effect because U2B $\bar{Q}$ and U6B pin 4 are low.

When U2B $\bar{Q}$ is high NAND gates U6B and U6D are enabled. When the signal at TP9 appears at U6D pin 13, U6D pin 11 goes low; flip/flop U5A/U5B does not change state becuase U5B pin 3 is low. The signal at pin 1 of U6A has no effect on the circuit because U2B $Q$ and pin 2 of U6A are low.

When two or more consecutive pulses from either input (TP5 or TP9) occur between pulses from the other input the sense circuit functions to disable the phase detector until the frequency error is corrected.

As an example of circuit operation assume that two pulses from TP9 (SL2 signal) are received between two pulses from TP5 (N3 signal) indicating that the SL2 frequency is high. When the first pulse from TP9 is received U3A pin 3 goes low, U3B pin 6 goes high to set U2B and the clock pulse causes U2B $Q$ to go high. When the second consecutive pulse is received from TP9 U6A has been enabled by the
high $Q$ output of U2B. U6A pin 3 goes low and causes flip/flop high $Q$ output of U2B. U6A pin 3 goes low and causes flip/flop
U5A/U5B to change state. When the D input of U2A goes low the clock pulse causes U2A Q to go low and inhibit U3A and U3D. If a clock pulse causes U2A Q to go low and inhibit U3A and U3D. If a
third SL2 signal is received prior to receipt of an N3 signal U6A pin 3 will again go low but will have no effect on flip/flop U5A/U5B because U5A pin 13 is low.

When an N3 pulse is received U2B Q is still high and U6C pin 8 will go low to change the state of flip/flop U5A/U5B. When the D input of U2A goes low the clock pulse causes U2A $\bar{Q}$ to go high and enable U3A and U3D. The propagation time of the signal through the sense circuit is long enough for the puse fred flip (flop U3B/U3C does not change.

The next pulse from SL2 will again cause U6A pin 3 to go low and change the state of flip/flop U5A/U5B. With the D input to U2A high again, the clock pulse again causes U2A Q to go low and inhibit U3A and U3D. The signal applied to U3A has no effect on flip/flop U3B/U3C because U3B pin 5 is low.

The sense circuit continues operation in the manner described above until two consectutive N3 pulses are received between two SL2 signals. When this occurs the first pulse causes U6C pin 8 to go low
and change the state of flip/flop U5A/U5B. With the D input to U2A low the clock pulse will cause U2A $\bar{Q}$ to go high and enable U3A and U3D. Again, because of propagation time through the sense circuit

## SERVICE SHEET 13 (Cont'd)

the pulse will have ended before U3D in enabled. The second consecutive N3 pulse again causes U6C pin 8 to go low but, because
U5B pin 3 is low, no change in state occurs in flip/flop U5A/U5B. U5B pin 3 is low, no change in state occurs in flip/flop U5A/U5B. U3B/U3C to change state. With the D input to U2B low, the clock pulse causes U2B $\bar{Q}$ output to go high. Phase lock has been achieved and the loop will remain locked as long as pulses at the same frequency appear alternately at TP5 and TP9.

When the SL2 frequency is low U2B $Q$ is low. When the SL2 frequency is high U2B Q is high.

DC amplifier Q2, Q1, Q6 and associated components filter the Q output of U2B and applies it to a summing circuit in the A11 assembly to precisely control the voltage controlled oscillator.

## TEST PROCEDURE

Test 1-a. Connect the oscilloscope input to test points shown by composite waveform SS13-1. This composite waveform illustrates correct waveforms and timing relationships for the points tested. All signals are about 4 volts in amplitude.

## NOTE

The oscilloscope was triggered from TP1 for these tests.


Composite Waveform SS13-1

If the pulses are not present at TP2 proceed to test 1-b.
If the pulses are not present at TP3 proceed to test 1-c
If the pulses are present at TP2 and TP3, but opposite polarity pulses are not present at TP5 and/or TP9, check the NAND gates petween TP2 and TP5 or TP3 and TP9 as appropriate.

## SERVICE SHEET 13 (Cont'd)

If the positive-going pulses are present at TP5 and TP9, but negative-going pulses are not present at TP6 for each of the pulses,
check NAND gates U1A, U1C, U1D and U5C as appropriate.

If the pulses are approximately as shown in the top five traces of composite waveform SS13-1 but there is no square wave at TP7, use the oscilloscope to check the signal at NAND gate U3B pin 6. The display should be the same as that shown for TP7. If the signal is
present U2B is probably defective. present, U2B is probably defective.
If the signal is not present at U3B pin 6 use the oscilloscope to check the signals at NAND gates U3D pin 11 and U3A pin 3. The signals should appear as they did at TP5 and TP9 except that they are the signal is present at one of the NAND gate outputs but not at the other, replace U3.

If the signal is not present at U3D pin 11 or U3A pin 3, use the digital voltmeter to check the dc level at U2A pin 6. The dc level should be about +4 volts. If U2A pin 6 is at about +4 volts, U3 is defective.

If the +4 volts is not present at U2A pin 6, ground U2A pin 1 . If the voltage at U2A pin 6 does not go to about +4 volts, U 2 is defective.

If trouble still has not been found, connect the counter to TP3 and the digital voltmeter and the oscilloscope to NAND gate U5A pin 12 . The counter readout should be about 210 kHz and U5A pin 12 should be low (about +60 millivolts). If the counter readout is lower or higher than 210 kHz and U5A pin 12 is high, slowly rotate oscilloscope. As the counter readout passes through the 210 kHz point the oscilloscope display should show a change in dc level; if it does not, U5 or U6 is probably defective.

Test 1-b. If there is no signal at TP2, or the signal is not approximately as shown in the top trace of composite waveform SS13-2, connect the oscilloscope first to TP1, then to U9 pin 8. TP1 and U9 pin 8 signals should be as shown in composite waveform SS13-2. All signal levels are about 4 volts.


Composite Waveform SS13-2

## SERVICE SHEET 13 (Cont'd)

If the signal is as shown at TP1, U7A or Q12 may be defective.
If the signal is as shown at U9 pin 8 but does not appear at TP1, U9 is probably defective.
If the signal does not appear at U9 pin 8 check the interconnections to the N3 loop and, if necessary, the N3 loop.

Test 1-c. If there is no signal at TP3, or the signal is not approximately as shown in the top trace of composite waveform SS13-3, connect the oscilloscope, in turn, to the points shown in composite waveform SS13-3


Composite Waveform SS13-3

If the signal shown in the second trace from the top of composite waveform $\mathrm{SS} 13-3$ is not as shown check Q3, Q7, U4B, U4C and associated components.
If the signal does not appear at Q4-c but the signal at TP4 is present check Q5, Q4 and associated components.

If the signal is not present at TP4 check for signals shown at TP10 and TP11. If both signals are present mixer E1 is probably defective. If either TP10 or TP11 signals are not present, trouble is in the N2 Loop or the SL2 voltage controlled oscillator

Test 1-d. To check operation of the dc amplifier connect the digital voltmeter to TP8 and rotate A11R19 through its range. The digital voltmeter readout should vary from about Q1, Q6 and associated components.


Figure 8-40. A12 SL2 Phase Detector Component Locations


## SERVICE SHEET 14

## SUMMING LOOP 2 OSCILLATOR A11

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A11 assembly, a part of the two-assembly SL2, is shown schematically and described on this service sheet. The SL2 Phase Detector assembly (A12) is shown schematically and described on service sheet 13 .

When trouble has been isolated to the A11 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the SL2 circuits the adjustment procedures in Section V paragraph 5-32 should be perform to ensure proper operation of the instrument.

## TEST EQUIPMENT REOUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes)
Digital Voltmeter
Frequency Counter

## SUMMING LOOP 2 GENERAL

The purpose of Summing Loop 2 (SL2) is to generate digitally controiled RF signals in the range of 20.0001 to 30.0000 MHz in selectable 100 Hz increments. The difference frequency between the SL2 voltage controlled oscillator and the input from the N2 loop is phase locked to the divided-by-ten output of the N3 assembly. The output of SL2 is applied to SL1.

## PRETUNING AND OSCILLATOR

The A11 assembly contains a voltage controlled oscillator, a digital to analog converter and a circuit to combine the pretuning dc level with the output from the phase detector. The frequency of the voltage controlled oscillator is roughly preset by the pretuning signal from the digital to analog converter circuit. The pretuning signal cannot, by itself, set the oscillator precisely; it does set the frequency within the capture range of the phase lock loop.

U2 is a decoder which converts the BCD information from digit 5 to turn on one of nine transistors in a resistive network. Quad NAND gate U3 turns on one or more transistors (Q17 through Q20) when there is a BCD input from digit 4. Quad NAND gate U8 in the A12 assembly turns on one or more transistors (A12Q8 through A12Q11 also in the A12 assembly) when there is a BCD input from digit 3.

When there is no BCD input (all inputs low), the voltage at TP3 is approximately -25 volts and the oscillator is roughly preset to 30.0000 MHz . As the digital to

## SERVICE SHEET 14 (Cont'd)

analog transistors are switched on the voltage at TP3 decreases (becomes less negative). When the BCD inputs are at 999 the voltage at TP3 is about -5 volts and the oscillator is roughly preset to 20.0001 MHz .

Q4 is a summing amplifier which combines the output of the digital to analog converter and the signal from the SL2 phase detector. The summing point (Q4-e) sums the current from three sources; a current source from the +20 volt supply through R19, R20 and R21, a negative source from the digital to analog converter (TP3) and the signal from the SL2 phase detector. The voltage at the summing point is always zero volts.

When TP3 is at approximately -25 volts (all BCD inputs low), most of the current from the +20 volt source flows through Q5, very little flows through Q4. Under these conditions the voltage at Q4-c is about -30 volts. As the voltage at TP3 decreases (gets closer to dc ground level) less current flows through Q5, more flows through Q4 and the voltage at Q4-c decreases.

CR2 through CR11 and associated resistors are used to shape the voltage curve applied to the voltage controlled oscillator tuning varactors to ensure that the frequency change is linear with the applied voltage. The voltage at the junction of R52 and R53 is about -27.5 volts. When all BCD inputs are low (Q4-c is at about -30 volts) all of the diodes in the shaper are reverse biased. As the voltage at TP3 decreases (gets closer to -5 volts), current through Q4 increases and the Q4 collector voltage decreases. As the Q4-c voltage decreases first CR11, then CR10, etc are forward biased. As the diodes are forward biased resistors are added in parallel with R37 and R38 to shape the voltage curve to the varactors. Q15 provides a low impedance output to drive the varactors.

Q1 drives U1A which functions as a Schmitt trigger. U1B inverts the signal and applies it to the SL1 phase detector. U1D also inverts the signal and applies it to the SL2 phase detector.

## TEST PROCEDURE

Test 1-a. Connect the counter to TP4. With the center freuqency set to zero the counter readout should be 30.000000 MHz . Set CF to the settings specified in Table 8-32. Frequency readouts should follow those specified in the table. (Make allowances for counter accuracy).

## NOTE

If the frequency readouts listed in Table 8-32 are not as shown, check the voltage levels shown for TP5 in the table. If the voltages are incorrect proceed to test procedures 2.

If the signal is present use the oscilloscope to check the signals at points shown by composite waveform SS14-1.

## SERVICE SHEET 14 (Cont'd)



Composite Waveform SS14-1

If the signal is present at TP4 but is not present at XA11-1-2 or XA11-1-6, U1 is probably defective.

If the signal is not present at TP4, use the oscilloscope to check for the signal at Q1-b. If the signal in present at Q1-b, check Q1 and NAND gate U1A. If the signal is not present at Q1-b check Q2, Q3 and associated components.

## TEST PROCEDURE 2

Test 2-a. Use the digital voltmeter to check the voltages at TP3, TP2 and TP5 These dc levels should be about as shown in Table 8-32 for the center frequencies shown.

## NOTE

These voltages are typical. They will vary from instrument to instrument because of differences in individuat varactor characteristics.
f the voltage at TP3 does not change when CF digit 5 is changed to any position U2 is probably defective. (Verify presence of BCD inputs). If the voltage at TP3 reaches about -25 volts when any CF digit 5 position is set (other than 0 ) the transistor associated with that number is probably open.

When the voltage at TP3 does not change with a change of the setting of CF digit 4, U3 or the associated transistors may be defective.

When the voltage at TP3 does not change with a change in the setting of CF digit 3, A12U8 or associated transistors may be defective. (This portion of the digital to analog converter is located in the A12 assembly).

## SERVICE SHEET 14 (Cont'd)

If the voltages are approximately correct at TP3 but are not correct at either TP2 or TP5, check Q4, Q15 and associated components.

The counter is connected to TP4 for readouts specified in Table 8-48.

Table 8-48. SL2 Frequency Versus Voltage Chart

| Center Frequency | Counter Readout | TP3 | TP2 | TP5 |
| :---: | :---: | :---: | :---: | :---: |
| 00000 Hz | 30.000000 MHz | -25.1 V | -31.6 V | -30.9 V |
| 11100 Hz | 28.890000 MHz | -22.8 V | -25.5 V | -24.8 V |
| 22200 Hz | 27.780000 MHz | -20.5 V | -20.5 V | -19.9 V |
| 33300 Hz | 26.670000 MHz | -18.3 V | -16.4 V | -15.7 V |
| 44400 Hz | 25.560000 MHz | $-16 . \mathrm{V}$ | $-13 . \mathrm{V}$ | -12.4 V |
| 55500 Hz | 24.450000 MHz | -13.8 V | -10.3 V | -9.6 V |
| 66600 Hz | 23.340000 MHz | -11.7 V | $-8 . \mathrm{V}$ | -7.3 V |
| 77700 Hz | 22.230000 MHz | -9.5 V | -6.2 V | -5.5 V |
| 88800 Hz | $21.120000 . \mathrm{MHz}$ | -7.3 V | -4.6 V | $-4 . \mathrm{V}$ |
| 99900 Hz | 20.010000 MHz | -5.3 V | -3.4 V | -2.8 V |
|  |  |  |  |  |



Figure 8-42. A11 SL2 VCO Component Locations


## SERVICE SHEET 15

## SUMMING LOOP 1 PHASE DETECTOR A15

Normally, causes of malfunctions in the Model 8660 C will be isolated to a circuit board or Normally, causes of malfunctions in the Model 8660 C will be isolated to a circu
assembly as a result of performing the tests specified in the troubleshooting trees.

The A15 assembly, a part of the three-assembly SL1, is shown schematically and described n this Service Sheet. The SL1 Oscillator Assembly (A19) is shown schematically an described on Service Sheet 17. The SL1 Mixer and D/A Converter Assembly (A18) is shown

When trouble has been isolated to the A15 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the SL1 circuits the adjustment procedures in Section V paragraph 5-33 should be performed to ensure proper operation of the instrument.
TEST EQUIPMENT REQUIRED (See Table 1-2)
Oscilloscope (with 10:1 divider probes)
Digital Voltmeter
Frequency Counter

## SUMMING LOOP 1 GENERAL

The purpose of Summing Loop 1 (SL1) is to generate digitally controlled RF signals in the range of 20.000001 to 30.000000 MHz in selectable increments as low as 1 Hz . The SL1 voltage controlled oscillator is phase locked to the divided by one hundred output of the SL1 is applied to the RF Section plug-in. SL1 is applied to the RF Section plug-in

## 1 PHASE DETECTOR ASSEMBLY A15

There are two signal inputs to the phase detector assembly. One is the input from the SL2 loop which is shaped by U10D and divided by 100 by U6 and U5. The output of U5 is again shaped by Q5 and U4A to provide negative-going pulses at TP2. The other input to the
phase detector is from the SL1 mixer and is the difference frequency between the N1 phase detector is from the SL1 mixer and is the difference frequency between the N1
oscillator and the SL1 voltage controlled oscillator. Q6, U4B, Q4 and U4C shape the signal and provides negative-going pulses at TP3

The pulse frequency at TP2 and TP3 varies (depending on programming) from 0.200001 to 0.300000 MHz . When the phase lock loop is locked the pulse frequency is the same at TP2 and TP3. The sampling ratio is $1: 1$.
U9A, U3B, U4D and U9B comprise coincidence gates which inhibit signals which appear simultaneously at TP2 and TP3. Normally, when signals are not present, TP2 and TP3 are both high.
When a signal appears at TP2, U9A pin 3 and U3B pin 4 go high. If there is no signal at TP3, U3B pin 5 is also high; U3B pin 6 goes low and U3C pin 8 goes high. The positive pulse at TP4 drives the clock generator and the sense circuit or the phase detector
When a signal appears at TP3, U4D pin 11 and U9B pin 5 go high. If there is no signal at TP2, U9B pin 4 is also high; U9B pin 6 goes low and U9D pin 11 goes high. The positive pulse at TP8 drives the clock generator and the sense circuit or the phase detector.
When signals appear simultaneously at TP2 and TP3, U9B pin 4 and U3B pin 5 go low: U9B pin 6 and U3B pin 6 remain high and the signals cannot reach TP4 or TP8.
U7C, U9C, U3D and U3A comprise a clock generator which clocks U2A and U2B each time a signal appears at TP4 or TP8. With no signals present TP4 and TP8 are low. When a
positive pulse appears at TP8, U9C pin 8 goes low, U3D pin 11 goes high and a positive pulse appears at TP8, U9C pin 8 goes low, U3D pin 11 goes high and a circuit is the same except that U7C pin 8 (rather than U9C pin 8 goes low). Since a clock

## SERVICE SHEET 15 (Cont'd)

pulse is generated for each input, the clock pulse frequency at TP5 is the sum of the pulse frequencies at TP4 and TP8. U2A and U2B are clocked by the positive-going trailing edge of the negative clock pulses.
Since the sense circuit does not function when the loop is locked, operation of the phase detector will be described first.
When the loop is phase locked U2A $\bar{Q}$ is held high to enable U1A and U1B. Assume that initially U2B $\bar{Q}$ is high U1D pin 11 is low and U1C pin 8 is high. When a positive pulse from TP8 appears at U1A pin 1, U1A pin 3 goes low and 8 goes low. The high at U1D pin 11 sets the D input to U2B and the clock pulse causes U2B Q to go high. The following positive pulse at TP4 is applied to U1B pin 5, U1B pin 6 goes low and changes the state of flip/flop U1D/U1C. U1D pin 11 goes low and the clock pulse causes U2B $\bar{Q}$ to again go high. This sequence continues as long as the pulses at TP4 and TP8 alternate.
The signals at TP4 and TP8 are applied to the sense circuit even when the loop is phase locked. They have no effect on the circuit because of the relationship between the $Q$ and $\bar{Q}$ outputs of U2B to the incoming signals.
When U2B is high, NAND gates U8A and U8C are enabled. When the signal from TP4 appears at U8C pin 9, U8C pin 8 goes low; flip/flop U7A/U7B does from change state because U7B pin 3 is low. The signal at U8B pin 4 has no effect because U2B $\bar{Q}$ and U8B pin 5 are low.
When two or more consecutive pulses from either input (TP4 or TP8) occur between pulses from the other input, the sense circuits function to disable the phase detector until the frequency error has been corrected.
As an example of circuit operation, assume that two pulses from TP8 are received between two pulses from TP4, indicating that the SL1 frequency is too high. high to set the D input to U2B and the clock pulse causes U2B Q to go high high to set second consecutive pulse is received from TP8, U8A has been enabled by the high Q output of U2B. U8A pin 3 goes low and causes flip/flop U7A/U7B to change state. When the D input to U2A goes high, the clock pulse causes U2A Q to go low and inhibit NAND gates U1A and U1B. If a third pulse from TP8 is received prior to receipt of a signal from TP4, U8A pin 3 will again go low but will not affect flip/flop U7A/U7B because U7A pin 13 is low
When a pulse is received from TP4, U2B Q is still high and U8C pin 8 will go low and change the state of flip/flop U7A/U7B. When the D input to U2A goes low the clock pulse will cause U2A Q to go high and enable U1A and U1B. The
propagation time of the signal through the sense circuit is long enough for the propagation time of the signal through the sense circuit is long enough for the pulse from TP4 to have ended before U1B is enabled so the state of flip/flop
U1D/U1C does not change.

The next pulse from TP8 will again cause U8A pin 3 to go low and change the state of flip/flop U7A/U7B. With the D input of U2A high again, the clock pulse causes U2A $\bar{Q}$ to go low and inhibit U1A and U1B. The signal applied to U1A has no effect on flip/flop U1D/U1C because U1D pin 12 is low.
The sense circuit continues operation in the manner described above until two consecutive pulses are received at TP4 between two pulses at TP8. When this occurs the first pulse causes U8C pin 8 to go low and change the state of flip/flop U7A/U7B. With the D input to U2A low the clock pulse will cause U2A $\vec{Q}$ to go high and enable NAND gates U1A and U1B. Because of the propagation time through the sense circuit, the pulse will have ended before U1B is enabled. The U7B pin 3 is now low, no change in state occurs in flip/flop U7A/U7B. Since U1B is enabled, U1B pin 6 goes low and causes flip/flop U1D/U1C to change state. With the D input of U2B low, the clock pulse will cause U2B $\bar{Q}$ output to go high.

## SERVICE SHEET 15 (Cont'd)

Phase lock has been achieved and the loop will remain locked as long the same frequency are received alternately at TP4 and TP8.
When the SL1 frequency is too low, U2B Q is low. When the SL1 frequ high, U2B $Q$ is high.

DC amplifier Q1, Q2, Q3 and associated components filter the Q out and applies it to a summing circuit in the A19 assembly to precisely

## TEST PROCEDURE

Test 1-a. Connect the oscilloscope input to test points shown by waveform SS15-1. This composite waveform illustrates correct wa timing relationships for the points tested. All signals are about amplitude.

## NOTE

The oscilloscope was triggered from TP1 for all waveform
If the pulses are not present at TP2 proceed to test 1-b.
If the pulses are not present at TP3 proceed to test 1-c.
f the pulses are present at TP2 and TP3, but opposite polarity puls present at TP4 and/or TP8, check the NAND gates between TP2 and T and TP8 as appropriate.
If the positive-going pulses are present at TP4 and TP8, but negative-g re not present at TP5 for each of the pulses, check NAND gates U3A, and U9C as appropriate


Composite Waveform SS15-1
If the pulses are approximately as shown in the top five traces of waveform SS15-1 but there is no square wave at TP6, use the oscil check the signal at NAND gate U1D pin 11. The display should be $t$ hat shown for TP6. IA the signa is present, U2B is probably defective. If the signal is not present at U1D pin 11 use the oscilloscope to check at NAND gates U1A pin 3 and U1B pin 6 . The signals should appear as
TP4 and TP8 except that they are inverted. If the signals are present, $U$ TP4 and TP8 except that they are inverted. If the signals are present, $U$
may be defective. If the signal is present at one of the NAND gates but may be defective. If the signal is not present at U 1 A pin 3 or U 1 B pin 6 , use the digital vc
check the dc level at U 2 A pin 6 . If U2A pin 6 is about +4 volts, U 1 is dt
If the +4 volts is not present at U2A pin 6 , ground U2A pin 1. If the U2A pin 6 does not go to about +4 volts, U2 is defective.
alse frequency at TP5 is the sum of A and U2B are clocked by the x pulses.
on the loop is locked, operation of
ld high to enable U1A and U1B. 11 is low and U1C pin 8 is high A pin 1, U1A pin 3 goes low and U1D pin 11 goes high and U1C pir input to U2B and the clock pulse ve pulse at TP4 is applied to U1E te of flip/flop U1D/U1C. U1D pin Q to again go high. This sequenc alternate.
sense circuit even when the loop is oming signals.
are enabled. When the signal from low; flip/flop U7A/U7B does not signal at $U 8 B$ pin 4 has no effect
either input (TP4 or TP8) occu se circuits function to disable the en corrected.
t two pulses from TP8 are received the SL1 frequency is too high the SL1 frequency is too high. pin 3 goes low, k pulse causes U2B Q to go high from TP8, U8A has been enabled low and causes flip/flop U7A/U7B s high, the clock pulse causes U2A U1B. If a third pulse from TP8 U8A pin 3 will again go low but pin 13 is low.
till high and U8C pin 8 will go low hen the D input to U2A goes low nen the D input enable U1A and U1B. The nse circuit is long enough for the enabled so the state of flip/flop

A pin 3 to go low and change the of U2A high again, the clock pulse of U2A high again, the clock pulse
1B. The signal applied to U1A has n 12 is low.
nanner described above until two en two pulses at TP8. When this w and change the state of flip/flop lock pulse will cause U2A Q to go Because of the propagation tim nded before U1B is enabled. The in flip flop to go low, but because pflop U1D/U1C to change state ill cause U2B $\bar{Q}$ output to go high

## SERVICE SHEET 15 (Cont'd)

Phase lock has been achieved and the loop will remain locked as long as pulses at the same frequency are received alternately at TP4 and TP8.
When the SL1 frequency is too low, U2B $Q$ is low. When the SL1 frequency is too high, U2B Q is high.
DC amplifier Q1, Q2, Q3 and associated components filter the Q output of U2B and applies it to a summing circuit in the A19 assembly to precisely control the voltage controlled oscillator.

## TEST PROCEDURE

Test 1-a. Connect the oscilloscope input to test points shown by composite waveform SS15-1. This composite waveform illustrates correct waveforms and timing relationships for the points tested. All signals are about 4 volts in amplitude.

## NOTE

The oscilloscope was triggered from TP1 for all waveforms
If the pulses are not present at TP2 proceed to test 1-b.
If the pulses are not present at TP3 proceed to test 1-c
If the pulses are present at TP2 and TP3, but opposite polarity pulses are not present at TP4 and/or TP8, check the NAND gates between TP2 and TP4 or TP3 and TP8 as appropriate.
If the positive-going pulses are present at TP4 and TP8, but negative-going pulses are not present at TP5 for each of the pulses, check NAND gates U3A, U3D, U7C and U9C as appropriate.


Composite Waveform SS15-1
If the pulses are approximately as shown in the top five traces of composite waveform SS15-1 but there is no square wave at TP6, use the oscilloscope to check the signal at NAND gate U1D pin 11. The display should be the same as that shown for TP6. If the signal is present, U2B is probably defective.
If the signal is not present at U1D pin 11 use the oscilloscope to check the signals at NAND gates U1A pin 3 and U1B pin 6. The signals should appear as they did at TP4 and TP8 except that they are inverted. If the signals are present, U1C or U1D may be defective. If the signal is present at one of the NAND gates but not at the other, replace U1.

If the signal is not present at U1A pin 3 or U1B pin 6, use the digital voltmeter to check the dc level at U2A pin 6. If U2A pin 6 is about +4 volts, U 1 is defective.
If the +4 volts is not present at U2A pin 6 , ground U2A pin 1 . If the voltage at U2A pin 6 does not go to about +4 volts, U2 is defective.

SL 2 VCO

SERVICE SHEET 14

## SERVICE SHEET 15 (Cont'd)

If the cause of trouble still has not been found, connect the counter to TP3 and the digital voltmeter and oscilloscope to NAND gate U7A pin 12. The counter readout should be about 300.000 kHz (center frequency set to zero) and U7A pin 12 should be low (about +70 millivolts). If the counter readout is lower or higher than 300 kHz and U5A pin 12 is high, slowly rotate A15R14 through its range while observing the counter and the oscilloscope As the counter readout passes through the 300 kHz point the oscilloscope display should show a change in level; if it does not, U7 or U8 is probably defective

Test 1-b. If there is no signal at TP2 or the signal is not approximately as shown in the top trace of composite waveform SS15-2, connect the oscilloscope first to TP2, then U6 pin 12, which the correct signal is first observed is followed by the defective circuit. If the signal is not present at XA15-2-14, check the interconnections to the SL2 loop and, if necessary, the SL2 loop.


Test 1-c. If there is no signal at TP3 or the signal is not approximately as shown in the top trace of composite waveform SS15-3 connect the oscilloscope first to U4 pin 6, then to U4 pin 4 or 5 and finally to XA15-2-C.


Composite Waveform SS15-3
In making the checks in the order shown, the point at which the signal is first observed is followed by the defective circuit. If the signal is not present at XA15-2-C check the interconnections to the A18 assembly and, if necessary, the A18 assembly

Test 1-d. To check operation of the dc amplifier connect the digital voltmeter to Q3-e, ground TP7, and rotate A15R14 through its range. The digital voltmeter readout should vary from about -1.5 volts to about +1.5 volts. If the voltage does not vary as A15R14 is adjusted, check Q1, Q2, Q3 and associated components.

## A15



$$
\begin{array}{lll}
\mathrm{L} 3 & \mathrm{U7} & \mathrm{U1}
\end{array}
$$



Figure 8-44. A15 SL1 Phase Detector Component Locations


## SERVICE SHEET 16

## SUMMING LOOP 1 MIXER AND D TO A CONVERTER A18

Normally, causes of malfunctions in the Model 8660 C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A18 assembly, a part of the three-assembly SL1, is shown schematically and described on this Service Sheet. The SL1 Phase Detector Assembly (A15) is shown schematically and described on Service Sheet 15. The SL1 Oscillator Assembly (A19) is shown schematically and described on Service Sheet 17.

When trouble has been isolated to the A18 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the SL1 circuits the adjustment procedures in Section V paragraph 5-33 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes)
Digital Voltmeter
Frequency Counter

## SUMMING LOOP 1 GENERAL

The purpose of Summing Loop 1 (SL1) is to generate digitally controlled RF signals in the range of 20.000001 to 30.000000 MHz in selectable increments as low as 1 Hz . The SL1 voltage controlled oscillator is phase locked to the divided by one hundred output of the SL2 loop and the difference frequency of the N1 loop and the SL1 oscillator. The output of SL1 is applied to the RF Section output plug-in.

## MIXER AND AMPLIFIERS

E1 is a double balanced mixer which mixes the output of the SL1 voltage controlled oscillator with the output of the N1 loop and provides an output which is the difference frequency of the two inputs.

Q14 and Q1 amplify the input from the SL1 voltage controlled oscillator.
Q2, Q15, Q18 and associated components amplify the output from the mixer before applying it to the phase detector circuit in the A15 assembly.

## TEST PROCEDURE

Test 1-a. With the center frequency set to zero use the counter and the oscilloscope to check for the following (approximately sine wave) signals:

> TP5 300.000 kHz at about 4 volts p/p
> TP4 (oscilloscope only) 300 kHz at about 0.1 volt $\mathrm{p} / \mathrm{p}$
> TP3 29.700000 MHz at゙about 0.5 volt $\mathrm{p} / \mathrm{p}$
> Q1-e 30.000000 MHz at about 1.1 volt $\mathrm{p} / \mathrm{p}$
> TP2 30.000000 MHz at about 0.5 volts $\mathrm{p} / \mathrm{p}$

## SERVICE SHEET 16 (Cont'd

## 2 DIGITAL TO ANALOG CONVERTER

U3 is a decoder which converts the BCD inputs from digit 7 to an output that will turn on one of nine transistors in a resistive network. Quad NAND gates U2 and U1 turn on one or more transistors connected to their outputs in a resistive network. U2 and U1 are controlled by digits 6 and 5 respectively.

The current flow through Q4 and the bias for Q3 is determined by which of the transistors in the resistive network are saturated. The dc level at TP1 is determined by which transistors are on. This dc level is applied to a summing circuit in the A19 assembly and used to roughly pretune the voltage controlled oscillator. When the BCD input is 000 the dc level at TP1 is about -25 volts. When the BCD input is 999 the dc level is about -5 volts.

## TEST PROCEDURE 2

Test 2-a. Connect the digital voltmeter to TP1 and the counter to TP5. Refer to Table 8-33 for CF settings, counter readouts, and approximate voltage levels.

## NOTE

The voltage readings are typical and may vary greatly from that shown due to differences in varactor characteristics. The important point to note is the ratio of change as the center frequency is changed.

If the voltage ratio changes about as shown but the frequency requirements are not met, trouble is probably in the oscillator assembly or the phase detector assembly.

Table 8-49. SL1 Frequency Versus Voltage Chart

| Center Frequency | Frequency TP5 | Voltage TP1 |
| :---: | :---: | :---: |
| 0000000 Hz | 300.000 kHz | -25.5 V |
| 1110000 Hz | 290.000 kHz | -23.4 V |
| 2220000 Hz | 280.000 kHz | -21.0 V |
| 3330000 Hz | 270.000 kHz | -18.8 V |
| 4440000 Hz | 260.000 kHz | -16.6 V |
| 5550000 Hz | 250.000 kHz | -14.3 V |
| 6660000 Hz | 240.000 kHz | -12.1 V |
| 7770000 Hz | 230.000 kHz | -9.9 V |
| 8880000 Hz | 220.000 kHz | -7.7 V |
| 9990000 Hz | 210.000 kHz | -5.4 V |
| 9999999 Hz | 200.000 kHz | -5.4 V |



Figure 8-46. A18 SL1 Mixer and D/A Converter Component Locations


## SERVICE SHEET 17

## SUMMING LOOP 1 OSCILLATOR A19

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

The A19 assembly, a part of the three-assembly SL2, is shown schematically and described on this Service Sheet. The SL1 Mixer and D/A Converter Assembly (A18) is shown schematically and described on Service Sheet 16. The SL1 Phase Detector Assembly (A15) is shown schematically and described on Service Sheet 15.

When trouble has been isolated to the A19 assembly it should be removed and reinstalled using two extender boards. This will provide easy access to test points and components.

## NOTE

After making repairs to any part of the SL1 circuits the adjustment procedures in Section V paragraph 5-33 should be performed to ensure proper operation of the instrument.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes)
Digital Voltmeter
Frequency Counter

## SUMMING LOOP 1 GENERAL

The purpose of Summing Loop 1 (SL1) is to generate digitally controlled RF ignals in the range of 20.000001 to 30.000000 MHz in selectable increments as low as 1 Hz . The SL1 voltage controlled oscillator is phase locked to the divided by one hundred output of the SL2 loop and the difference frequency of the N1 loop and the SL1 oscillator. The output of SL1 is applied to the RF Section plug-in.

## 1 SUMMING AMPLIFIER

Q6 is a summing amplifier which combines the output of the digital to analog converter and the signal from the SL1 phase detector. The summing point (Q6-e) sums the current from three sources; a current source from the +20 volt supply through R9, R10 and R11, a negative source from the digital to analog converte through R3, R7 and R68, and the signal from the SL1 phase detector through R6 The dc level at the summing point is held at zero volts.

When the input at XA19-2-J is about -25 volts (all BCD inputs to A18 low) most of the current from the +20 volt source flows through A18Q3; very little flows through Q6. Under these conditions the voltage at Q6-c is about - 30 volts. As the voltage at XA19-2-J decreases (becomes less negative), less current flows through A18Q3, more flows through Q6, and the voltage at Q6-c decreases (becomes less negative).

## SERVICE SHEET 17 (Cont'd)

CR1 through CR10 and associated resistors are used to shape the voltage curve applied to the voltage controlled oscillator tuning varactors to ensure that frequency change is linear with voltage change. The voltage at the junction of R32 and R39 is about -27.5 volts. When all BCD input to the A18 assembly are low, Q6-c is about -30 volts and all of the diodes in the shaper are reverse biased. As Q6-c is about -30 volts and all of the diodes in the shaper are reverse biased. A
the voltage from the digital to analog converter decreases (gets closer to -5 volts) current through Q6 increases and the Q6 collector voltage decreases. As the Q6-c voltage decreases first CR10, then CR9, etc. are forward biased. As the diodes are forward biased resistors are added in parallel with R35 and R38 to shape the voltage curve to the varactors. Q7 provides a low impedance output to drive the varactors.

## TEST PROCEDURE

Test 1-a. Connect the digital voltmeter to TP1 and set the center frequency as shown in Table 8-34.

## NOTE

The voltage readings are typical and may vary greatly from that shown due to differences in varactor characteristics. The important point to note is the ratio of change as the center frequency is changed.

If the voltage at TP1 does not change as the CF are changed check the input from the digital to analog converter (A18) at XA19-2-J. If the voltage levels at this point do not change as the CF is changed, trouble is probably in the A18 assembly.

If the voltage level from the digital to analog converter does change, but the leve at TP1 does not, check Q6, Q7 and associated components.

## 2 VOLTAGE CONTROLLED OSCILLATOR AND AMPLIFIERS

Q5, Q4 and associated components comprise a voltage controlled oscillator. C17 C20 and C21 provide isolation for the dc levels required to bias the varactors. C19 provides the feedback necessary to sustain oscillation. The resonant tank circuit is coupled to Q4 by capacitive divider C20 and C21. The FET acts as a source follower in the feedback circuit; it provides a high impedance at the gate and a ow impedance at the source.

Q3 is a power splitter which drives two two-stage amplifiers. One amplifier output is applied to the RF Section plug-in and the other is applied to the mixer in the A18 assembly.

## TEST PROCEDURE

Test 2-a. Connect the oscilloscope to TP3 then to TP4. The sine wave at both test points should be about 0.3 volts $\mathrm{p} / \mathrm{p}$.

## SERVICE SHEET 17 (Cont'd)

CR1 through CR10 and associated resistors are used to shape the voltage curve applied to the voltage controlled oscillator tuning varactors to ensure that frequency change is linear with voltage change. The voltage at the junction of R32 and R39 is about -27.5 volts. When all BCD input to the A18 assembly are low Q6-c is about -30 volts and all of the diodes in the shaper are reverse biased. As the voltage from the digital to analog converter decreases (gets closer to -5 volts) current through Q6 increases and the Q6 collector voltage decreases. As the Q6-c voltage decreases first CR10, then CR9, etc. are forward biased. As the diodes are forward biased resistors are added in parallel with R35 and R38 to shape the voltage curve to the varactors. Q7 provides a low impedance output to drive the varactors.

## TEST PROCEDURE

Test 1-a. Connect the digital voltmeter to TP1 and set the center frequency as shown in Table 8-34.

## NOTE

The voltage readings are typical and may vary greatly from that shown due to differences in varactor characteristics. The important point to note is the ratio of change as the center frequency is changed.

If the voltage at TP1 does not change as the CF are changed check the input from the digital to analog converter (A18) at XA19-2-J. If the voltage levels at this point do not change as the CF is changed, trouble is probably in the A18 assembly.

If the voltage level from the digital to analog converter does change, but the level at TP1 does not, check Q6, Q7 and associated components.

2 VOLTAGE CONTROLLED OSCILLATOR AND AMPLIFIERS
Q5, Q4 and associated components comprise a voltage controlled oscillator. C17, C20 and C21 provide isolation for the dc levels required to bias the varactors. C19 provides the feedback necessary to sustain oscillation. The resonant tank circuit is coupled to Q4 by capacitive divider C20 and C21. The FET acts as a source follower in the feedback circuit; it provides a high impedance at the gate and a low impedance at the source.

Q3 is a power splitter which drives two two-stage amplifiers. One amplifier output is applied to the RF Section plug-in and the other is applied to the mixer in the A18 assembly.

## TEST PROCEDURE

Test 2-a. Connect the oscilloscope to TP3 then to TP4. The sine wave at both test points should be about 0.3 volts $\mathrm{p} / \mathrm{p}$.

## SERVICE SHEET 17 (Cont’d)

If the signal is not present at either TP3 or TP4 connect the oscilloscope to Q3-b. The signal level should be about 0.2 volts $p / p$. If the signal is present at Q3-b but was not present at TP3 or TP4, Q3 is probably defective. If the signal is not present at Q3-b, check Q5, Q4 and associated components.

Test 2-b. Connect the counter to TP3 or TP4 and check for correct frequencies at the CF shown in Table 8-47

Table 8-50. Varactor Bias Versus Frequency SL1

| Center Frequency | Frequency TP3 or TP4 | Voltage TP1 |
| :---: | :---: | :---: |
| 0000000 Hz | 30.000000 MHz | -30.7 V |
| 1110000 Hz | 28.890000 MHz | -25.3 V |
| 2220000 Hz | 27.780000 MHz | -21.2 V |
| 3330000 Hz | 26.670000 MHz | -17.2 V |
| 4440000 Hz | 25.560000 MHz | -13.4 V |
| 5550000 Hz | 24.450000 MHz | -10.6 V |
| 6660000 Hz | 23.340000 MHz | -8.2 V |
| 7770000 Hz | 22.230000 MHz | -6.3 V |
| 8880000 Hz | 21.120000 MHz | -4.7 V |
| 9990000 Hz | 20.010000 MHz | -3.3 V |
| 9999999 Hz | 20.000001 MHz | -3.2 V |



Figure 8-48. A19 SL1 VCO Component Locations


## SERVICE SHEET 18

## dCu block diagram

## GENERAL

The DCU (Digital Control Unit) controls all functions of the mainframe in the local mode of operation. In addition, in the remote mode of operation, the DCU displays the selected center frequency (CF) and processes the programming data to control all functions of the mainframe and the plug-in sections.

The DCU is a bus oriented system with three major buses.
All of the data from the keyboard shift register (KYBD SR), the Arithmetic Logic Unit (ALU) and the CF register is routed through the T bus to their destination(s).
The R bus couples the outputs of the CF and A registers to the ALU on command.
The S bus couples the outputs of the step and sweep width registers, and the output of a read-only-memory (ROM) to the ALU on command

The following information describes, in general terms, the overall operation of the various functions of the DCU. More detailed information to the circuit level appears on the foldout page opposing the schematic diagrams of the individual circuits.

## KEYBOARD

The keyboard (KYBD) assembly consists of 20 non-contacting keys and a circuit board containing 20 printed circuit transformers. The transformer secondaries are series connected and the primaries are connected in series pairs. The transformer windings in each pair are oppositely paired. Each pair of the transformers are controlled by one numeral ( $0-9$ ) key and one function (D.P., CF, MHz, etc.) key. A 100 kHz clock controls scanning of the transformer pairs.
When a key is pressed, a spring loaded, metal disc closely coupled to the transformer changes the mutual inductance between the primary and secondary of the corresponding transformer. The key detect and encode circuit in the A1A2 keyboard control assembly then determines which key of the pair has been pressed.
The keyboard is shown schematically on Service Sheet 21.

## KEYBOARD CONTROL ASSEMBLY

Key Detect and Encode. The keyboard control assembly provides a train of 100 kHz pulses to the ten key-pair transformers on the keyboard. The keyboard pairs are strobed successively in the scanning process. When a key is pressed the scanning is stopped until the key is released.
During the period of time that scanning is stopped, the key detect and encode circuit determines which key of the pair has

## SERVICE SHEET 18 (Cont'd)

been pressed and furnishes outputs to MPX I (multiplexer I) or to the qualifier select circuits on the A1A4 assembly. Numer ical information goes to MPX I and all other information goes to A1A4.

Keyboard Register and Multiplexers. In order to simplify the following discussion the multiplexers in the keyboard control assembly are referred to as MPX I, MPX II and MPX III. Each of the multiplexers has four-line inputs to points labeled $\mathrm{I}_{0}$ and $\mathrm{I}_{1}$. The input to be used is determined by the level at the IS selector line, i.e., a high level, logic 1, would select the I1 inputs.

In the local mode, $\mathrm{K} \emptyset$ register and the KYBD SR function as a four-bit, eleven digit, recirculating shift register. The purpose of recirculating the BCD information is to ensure that when al data is stored in the KYBD SR, the least significant digit is stored in a position to be the first digit shifted out of the register.
Operation of the circuit is as follows (example entry is 12.345678 MHz ); KYBD key 1 is pressed first and the BCD information (0001) is coupled through MPX I to be stored in K0. The KYBD SR is then clocked by a burst of ten clock pulses and the BCD information is shifted to the least significant digit position in the KYBD SR.
The second KYBD entry, a 2 (0010) is clocked into K $\emptyset$. A burst of ten clock pulses again transfers the K $\emptyset$ data to the leas significant digit of the KYBD SR. Now, however, there is an input to MPX I, $\mathrm{I}_{1}$, which is clocked into K 0 ; this entry, BCD 0001, follows the BCD 0010 information through to the KYBD SR. When the burst of ten clock pulses ends, the BCD 0010 data is stored in the KYBD SR least significant storage and the BCD 0001 data is stored in the next least significant digit storage.
The third keyboard entry, for the example used, is a decimal point (DP) which does not directly affect the KYBD SR. The DP information is applied to the qualifier select circuit in the A1A4 assembly.

The fourth keyboard entry, for the example used, a 3 (0011) is processed in the same manner as the first and second entries. A the end of the burst of ten clock pulses the information stored in the KYBD SR is 0000000123 .

## NOTE

If the KYBD pushbutton is now pressed the CF readout will display 12.3.

The remaining keyboard entries are processed in the same manner as entries 1,2 and 4 . When all information has been entered the KYBD SR data will be 0012345678 . If the KYBD pushbutton is pressed the CF readout will display 12.345678

## SERVICE SHEET 18 (Cont'd)

The last keyboard entry (in the example an 8, BCD1000), will be the first digit clocked out when the data is transferred to another shift register.
When information is clocked out of the KYBD SR it is also recirculated through MPX III and clocked back into the KYBD SR. In the local mode the information is retained in the KYBD SR until the keyboard is cleared or a new data entry is made.
In the remote mode, MPX III $\mathrm{I}_{0}$ inputs are enabled by the RMT CMND-L line which goes low on command. Information from the mainframe interface circuits is applied to MPX III IO inputs with the least significant digit first. Data is entered in the KYBD SR until all required data is entered.

It should be noted that when the information in the KYBD SR is clocked out in the remote mode, it is again coupled back to MPX I and MPX III. This feedback is coupled through MPX I to $\mathrm{K} \emptyset$ but cannot affect the KYBD SR because MPX II I 1 is selected. Since MPX III IS is low only when remote data is being programmed in from an external source, the feedback flows through MPX III and MPX II to recirculate the informa tion in the KYBD SR. When the data is stored in a final register the KYBD SR is cleared.

The output from the KYBD SR is applied to the A1A6 register assembly.

Refer to Service Sheets 19,20, and 32 for more detailed information regarding these circuits.

## REGISTER ASSEMBLY

The A1A6 assembly contains the CF, STEP, SWEEP WIDTH and $M$ registers.

The data inputs to the A1A6 assembly consist of inputs from the KYBD SR and the ALU. Most instructions are received from the A1A5 ROM output assembly.

The BCD inputs from the KYBD SR are applied to two sets of gates. If these BCD inputs are data inputs for the plug-in sections, the gates are enabled by the input ST01-H, and the data is transferred to the appropriate register in the addressed plug-in section.
If the information stored in the KYBD SR is not for the plug-in sections, gates may be enabled by KTT-H to couple the information to the $T$ bus. Simultaneously, the information on the T bus is clocked into one, or more, of the shift registers on the A1A3 or A1A9 assembly as well as the A1A6 assembly.
Most of the registers are preceeded by multiplexers. These multiplexers may be an integral part of the register integrated circuit or a separate integrated circuit.
When new information is present on the T bus, one set of multiplex gates is enabled to couple the information to the

## SERVICE SHEET 18 (Cont'd)

register. When information is being clocked out of a register, the other set of multiplexer gates are enabled to recirculate the information to the register. This ensures that register information is retained for future use without re-programming.

Center Frequency (CF) Register
The CF register is the only register that feeds its output back to the T bus. This output to the T bus, which is coupled through gates enabled by CTT-H occurs when:

1. Entry of an out-of-range frequency has been attempted (state 3/8).
2. A frequency increment (STEP) has been added to or subtracted from, the center frequency (state 2/7).
3. The instrument has been switched from the sweep mode to the fixed frequency mode (state $2 / 9$ ).
4. The readout is to display CF again after the readout has been used to display KYBD, STEP, or SWP WIDTH (state $1 / 8)$.
Refer to Service Sheet 29 for more detailed information about the CF register.

## Step Register

Any frequency (within the range of the RF Section in use) may be stored in the step register and added to, or subtracted from, the center frequency by the ALU. Since the step register is a recirculating register, the stored information may be used as many times as destred.

Refer to Service Sheet 30 for more detailed information about the step register.

## Sweep Width Register

Any sweep width within the range of the RF Section in use may be stored in the sweep width register. In the sweep mode the sweep width is centered on the center frequency. Example; CF 50 MHz , SWP WIDTH 50 MHz , RF output is swept from 25 to 75 MHz .

Refer to Service Sheet 30 for more detailed information about the sweep width register.

## M Register and Limits

When CF data from the KYBD SR is first clocked to the $T$ bus it is applied only to the M register. The M register and the frequency limits decoder then determined if the programmed frequency is within the limits of the RF Section in use.

The $M$ register is a six digit register. Only the six most significant digits are required for limit detection.

## SERVICE SHEET 18 (Cont'd)

The frequency limits decoder, in addition to the BCD inputs from the M register, has 16LIM and 13GL inputs. The 16LIM and 13GL inputs are decoded inputs from the RF Section plug-in which are used to select the frequency limits.
The frequency limits decoder controls operation of the OUT OF RNG lamp and also provides Code 1 and Code 2 dc levels to the RF Section power amplifiers to operate two transistor switches to change the response time for output leveling.

After the M register and the frequency limits decoder have determined that the CF data is valid, the KYBD SR data is again clocked via the T bus into the CF , readout (RO) and A registers. The data is then clocked from the A register through the ALU via the $R$ bus to the $T$ bus and to A1A10, the output register.

Refer to Service Sheet 31 for a more detailed description of the M register and frequency limits circuit.

## ARITHMETIC LOGIC UNIT (ALU)

The ALU, as the name implies, arithmetically manipulates the inputs from the other registers. The ALU may add, subtract, or allow the data to flow through without change. It also has a ROM (read-only-memory) which contains incrementing numbers used for the manual tune operation. The ROM may be used to cause the selected center frequency to be offset by any frequency within the range of the RF Section in use.

## NOTE

Offset is a special option. The frequency offset must be specified, and the ROM programmed at the factory.

Refer to Service Sheet 32 for a more complete description of the ALU circuits.

## OUTPUT REGISTER

The output register converts the serial BCD data from the T bus or the A register to parallel BCD data. This is referred to as parallel dump. The advantage of parallel dump over serial dump is that only those mainframe phase lock loops which are programmed for a different rf output lose phase lock. This improves switching time and avoids generation of unwanted frequencies.

Refer to Service Sheet 35 for a more detailed explanation of the output register circuit.

## SWEEP COUNT ASSEMBLY

Shown directly under the ALU block is the sweep count assembly. The major function of this assembly is to keep track of the number of steps which have been taken in the sweep

## SERVICE SHEET 18 (Cont'd)

operation. The three UP/DN counters have the capability of counting to 1000 steps. When the sweep is set to 100 steps the first UP/DN counter is bypassed and the count is 100 .

When the sweep mode is selected, the sweep always starts at the center frequency. In the AUTO mode the frequency steps are always to a higher frequency. When the upper limit of the sweep range is reached, the sweep starts at the lower limit of th range and is stepped up in frequency until the upper limit is again reached.

In the manual (MAN) sweep mode the sweep may be stepped either up or down by use of the manual tuning control.

The D/A (digital to analog) output ( 0 to +8 V ) may be used as an input to X-Y recorders, oscilloscopes, etc.

For more complete details about the sweep count assembly refer to Service Sheet 33 .

## SWITCH CONTROL ASSEMBLY

The switch control assembly is shown at the far left side of the block diagram. This assembly provides seven clocks for use in various parts of the DCU. It also generates and stores qualifiers for all of the front panel controls except the keyboard numbers.

For a more complete description of the switch control assembly refer to Service Sheets 19 and 20.

ROM INPUT AND ROM OUTPUT ASSEMBLIES
The outputs of the seven state flip-flops control the qualifier select and seven of the address bits of the ROMs. When the eighth address bit is provided to the ROMs, the seven state flip/flops are set to the next state by the outputs of ROMs 1 and 2 . ROM 2 also provides 1 output instruction and ROM 3 provides 4 output instructions.

Circuits are also provided to manually clock (single step) the DCU. When this feature is used, light emitting diodes verify the machine state.

## SERVICE SHEET 18 (Cont'd)

The frequency limits decoder, in addition to the BCD inputs from the M register, has 16LIM and 13GL inputs. The 16LIM and 13GL inputs are decoded inputs from the RF Section plug-in which are used to select the frequency limits.

The frequency limits decoder controls operation of the OUT OF RNG lamp and also provides Code 1 and Code 2 dc levels to the RF Section power amplifiers to operate two transistor switches to change the response time for output leveling.

After the M register and the frequency limits decoder have determined that the CF data is valid, the KYBD SR data is again clocked via the T bus into the CF, readout (RO) and A registers. The data is then clocked from the A register through the ALU via the $R$ bus to the $T$ bus and to A1A10, the output register.
Refer to Service Sheet 31 for a more detailed description of the M register and frequency limits circuit.

## ARITHMETIC LOGIC UNIT (ALU)

The ALU, as the name implies, arithmetically manipulates the inputs from the other registers. The ALU may add, subtract, or allow the data to flow through without change. It also has a ROM (read-only-memory) which contains incrementing numbers used for the manual tune operation. The ROM may be used to cause the selected center frequency to be offset by any frequency within the range of the RF Section in use.

## NOTE

Offset is a special option. The frequency offset must be specified, and the ROM programmed at the factory.

Refer to Service Sheet 32 for a more complete description of the ALU circuits.

## OUTPUT REGISTER

The output register converts the serial BCD data from the T bus or the A register to parallel BCD data. This is referred to as parallel dump. The advantage of parallel dump over serial dump is that only those mainframe phase lock loops which are programmed for a different rf output lose phase lock. This improves switching time and avoids generation of unwanted frequencies.

Refer to Service Sheet 35 for a more detailed explanation of the output register circuit.

## SWEEP COUNT ASSEMBLY

Shown directly under the ALU block is the sweep count assembly. The major function of this assembly is to keep track of the number of steps which have been taken in the sweep

## SERVICE SHEET 18 (Cont'd)

operation. The three UP/DN counters have the capability of counting to 1000 steps. When the sweep is set to 100 steps the first UP/DN counter is bypassed and the count is 100 .

When the sweep mode is selected, the sweep always starts at the center frequency. In the AUTO mode the frequency steps are always to a higher frequency. When the upper limit of the sweep range is reached, the sweep starts at the lower limit of the range and is stepped up in frequency until the upper limit is again reached.

In the manual (MAN) sweep mode the sweep may be stepped either up or down by use of the manual tuning control.

The $\mathrm{D} / \mathrm{A}$ (digital to analog) output ( 0 to +8 V ) may be used as an input to X-Y recorders, oscilloscopes, etc.

For more complete details about the sweep count assembly refer to Service Sheet 33 .

## SWITCH CONTROL ASSEMBLY

The switch control assembly is shown at the far left side of the block diagram. This assembly provides seven clocks for use in various parts of the DCU. It also generates and stores qualifiers for all of the front panel controls except the keyboard numbers.

For a more complete description of the switch control assembly refer to Service Sheets 19 and 20.

## ROM INPUT AND ROM OUTPUT ASSEMBLIES

The outputs of the seven state flip-flops control the qualifier select and seven of the address bits of the ROMs. When the eighth address bit is provided to the ROMs, the seven state flip/flops are set to the next state by the outputs of ROMs 1 and 2 . ROM 2 also provides 1 output instruction and ROM 3 provides 4 output instructions.

Circuits are also provided to manually clock (single step) the DCU. When this feature is used, light emitting diodes verify the machine state.

## NOTE

The term "machine state" refers to a given set of conditions at a given point in time. These states are shown in logical succession on the Algorithmic State Machine (ASM) Flow Chart on the last foldout sheet of this manual.

For a more complete description of circuit operation refer to Service Sheet 26.

The box labeled qualifier select in the ROM input assembly is shown schematically on Service Sheet 25. Multiple devices form a large selector circuit providing one output selected from 34 qualifier inputs. Seven inputs from the seven state flip-flops control the selection. The single output provides the eighth address bit to ROMs 1,2 and 3 .

For a more detailed description of circuit operation refer to Service Sheet 25.

The ROM output assembly contains a clock burst control which selects the number of pulses in the clock train, and a state decoder which converts the coded outputs of the seven state flip-flops to instructions.

For a more detailed description of the circuits refer to Service Sheets 27 and 28.

## READOUT CONTROL ASSEMBLY

The major function of the A1A3 readout control assembly is to justify (position) the decimal point in the readout. The assembly also contains a 10 digit readout register which controls the ROMs in the readout assembly. Blanking of the leading zeros, and scanning of the register for the readout assembly is also provided.

For a more detailed description of the cirucits in the readout control assembly refer to Service Sheets 23 and 24 .

## READOUT ASSEMBLY

The readout assembly contains two side by side solid state readouts. Both are 6 digit readouts.

For a more complete description of the readout assembly circuits refer to Service Sheet 36.


Figure 8-50. 8660B DCU (A1)



## SERVICE SHEET 19

## P/O SWITCH CONTROL ASSEMBLY A1A1

Service sheets 19 and 20 provide schematic diagrams for the circuits on the A1A1 assembly and some of the front panel operating controls.

The pushbutton switches shown in the upper left hand corner of Service Sheet 19 labeled KYBD, STEP and SWP WIDTH, when pressed, cause the information stored in the KYBD SR (keyboard shift register), STEP (step register), or the SWP WIDTH (sweep width register) to be displayed on the CENTER FREQUENCY readout.

The PBCOM (pushbutton common line) is low when the instrument is in the local mode and the power detect requirements have been met. When any one of the pushbuttons is pressed the D input of the associated D type flip-flop goes low. The $Q$ output of the associated flip-flop goes low and remains low until the pushbutton is released. On release the Q output goes high on the next clock pulse. The clock pulse to these flip-flops are operated by a 200 Hz clock.

The Q outputs of the pushbutton flip-flops U21B, U29B and U29A are used in the readout control assembly, A1A3 and the ROM Input assembly A1A4. These Q outputs also control the output of NAND gate U22B. When any one of the $Q$ outputs go low, the output of NAND gate U22B goes high.

Normally, the pushbutton readout (PBR) flip-flop, U11A and the center frequency (CFR) flip-flop, U11B, are in the reset state.

When one of the pushbuttons is pressed and the output of U22B goes high, both inputs to AND gate U20C are high, the J input to U11A is high and U11A Q will go high on the first clock pulse. The Q output of U11A goes high to enable U20B.
When U11A $\bar{Q}$ goes low, AND gates U19A and U13C are inhibited. The low level at U13C pin 8 enables NOR gate U24C. When the instrument is in state $0 / 0$ the output of U 24 is also low so the J input of flip-flop F10 goes high. The next clock pulse causes U16B Q to go high. When qualifier F10-H goes high the state machine is enabled to proceed from state $0 / 0$ to state $4 / 0$.

When state $3 / 6$ is reached, KPBR and JCFR go low, KF10 and RKD2 go high. The KPBR-JCFR input is inverted and applied to the K input of U11A and, through AND gate U20B to the J input of U11B. Simultaneously the KF10-H level is applied to the K input of the F 10 flip/flop U16B. The next clock pulse causes U11A $Q$ to go low, U11B $\bar{Q}$ to go high and U16B $Q$ to go low.

## SERVICE SHEET 19 (Cont'd)

The state progression then flows back to state $0 / 0$ where it remains until the pushbutton is released. On release of the pushbutton the $Q$ output of the associated pushbuttton flip-flop again goes high and the output of NAND gate U22B goes low.

Both inputs to NOR gate U24A are now low so the output goes high and is inverted to inhibit AND gates U19A and U13C. The next clock pulse causes the Q output of the F10 flip-flop, U16B, to go high. The state machine again proceeds from state $0 / 0$, state $4 / 0$ and on.

When machine state $1 / 8$ is reached the instructions cause the Center Frequency readout to again display the center frequency. Instruction KCFR-L occurs in state $1 / 8$. This input is inverted and applied to the $K$ input of U11B which is then clocked to drive the Q output terminating the CFR flip-flop function.

When any keyboard key is pressed, input KD2-L goes low. This inhibits NAND gates U19A and U13C and enables NOR gate U24C. The J input to the F10 flip-flop, U16B, goes high when in state $0 / 0$ and the next clock pulse causes the Q output to go high.

The F10 flip-flop $Q$ output also is caused to go high at state $0 / 0$ when a manual tune operation causes U19A pin 4 to go low or when a sweep operation causes U13C pins 10 and 11 to go low. In each case, the F10 flip-flop is set and this starts the state to state progression.

The F1 flip-flop, U16A, which is also called the interrupt flip-flop, is set in state $0 / 0$ when a keyboard entry, a manual entry, or a pushbutton entry is made during a sweep operation. When any of these entries are made, the output of NAND gate U19A goes low to enable NOR gate U24D.

When state $0 / 10$ is reached, the J input of U16A goes high, and the next clock pulse causes the $\mathbf{Q}$ output to go high.

When a keyboard entry is made while in the sweep mode, the sweep is interrupted while the entry is being executed. During execution U15A K input goes high in state $0 / 5$ enabling the reset of the F1 flip-flop. The sweep is resumed when the entry is completed.

U 26 is a 4 -line to 16 -line selector. The A, B, C and D inputs are in binary format. Inputs G1 and G2 are enabling inputs which must both be low to enable the selector. U26 is the code 0 selector; whenever it is active the state is $0 / 0,0 / 1,0 / 2$, etc. All outputs are high except the one selected. The outputs of the selector are instructions. Some of the instructions are qualified; they do not affect the circuits unless certain conditions are met. As an example, the F10 flip-flop, U16B will not be set in state $0 / 0$ unless a front panel control, switch or key has been manipulated. Some instructions such as JF9-H, are generated by more than one state.

Flip-flop U1 in the lower left corner of the schematic performs the sole function of operating the OUT OF RNG lamp. When the frequency selected is above the range of the RF Section in use, the data is rejected and the OUT OF RNG lamp flashes once (about 0.5 second). When the frequency selected is below the specified limits, the OUT OF RNG lamp light stays lit (frequencies below the specified limits are useable).

U28B, in conjunction with cross-connected NAND gates U18A and U18B serve to speed up detection of an out of range frequency to provide an FLIM-L (out of range) signal for programming equipment external to the 8660 C .

Flip-flop U28A controls the SWON-H (sweep on line.

## A1A1



Figure 8-52. P/O A1A1 Switch Control Assy Component Locations (Part 1)

P/O AIAI SWITCH CONTROL ASSY 08660-60200


## SERVICE SHEET 20

## P/O SWITCH CONTROL ASSEMBLY A1A1

Service Sheets 19 and 20 show the circuits of the A1A1 assembly schematically.

The circuits receive inputs from all front panel switches except the keyboard. These inputs serve to set (or reset) certain flip/flops or may simply flow through the assembly for use in other assemblies.
A principal output is qualifier F10-H from flip/flop U15 shown on SS19 When qualifier F10-H is set the state machine will go through the various states to set up the operation selected by the operator. Principal inputs to the F10 flip/flop are from the keyboard via input KD2-L, the readout pushbutton switches, the sweep control switches or the manual mode tuning dial.

A second principal circuit is the 4 -to- 16 selector U26 (shown on SS 19 ) which is one of four such selectors in the DCU. Selector U26, which is designated as CODE 0 , is a part of this assembly because many of the outputs are directly used in other circuits in the assembly. The other three select 28.

A third principal circuit is the clock dividers which provide seven different check outputs used in various DCU circuits.

The first divider, D type flip-flop U32B, divides the 2 MHz coax clock by two. The 1 MHz output of U32B drives divide-by-ten U9 and is also used as the system clock.

The second divider, U9, divides by ten. The 100 kHz output drives divide-by-ten U8 and is also used as the keyboard clock.

The third divider, U8, divides by ten. The 10 kHz output drives U 6 and is also used in the readout assembly.

The fourth divider, U6, provides two outputs. The first, a divide-by-two, 5 kHz clock is used in the readout control assembly. The second output is a divided-by-ten 1 kHz clock used in controlling the sweep. The 1 kHz output also drives U7. The fifth divider, U7, divides by 5 . The 200 Hz output is used in the sweep control circuits and to clock the pushbutton flip-flops (see SS19). This output also drives U7.

The sixth divider, U5, divides by ten. The 20 Hz output is used in the sweep control circuits.

In the upper left hand corner of the schematic is a block labeled ROTARY PULSE GENERATOR (abbreviated RPG). The RPG is enabled by the MANUAL MODE RESOLUTION switch in any position except OFF. The RPG is also enabled when the SWEEP MODE switch is placed in the MAN position. The SWEEP MODE switch takes precedence over the ${ }^{\text {d-MANUAL }}$
MODE RESOLUTION switch.

## SERVICE SHEET 20 (Cont'd)

The RPG contains a light source and two photocells which are used to generate two square waves. These two square waves have a quadrature relationship - they are 90 degrees out of phase.
The circuits following the RPG CW and CCW outputs must detect when a manual entry has been made and also whether the input is an increase or a decrease in frequency.

AND gate U33D is driven by the CW and CCW inputs from the RPG
Assume that the RPG is to be turned in the CW direction and that initially the CW output is low. The CCW output is low when the CW output goe high. When the CCW output goes high AND gate U33D is enabled and its output is high. When the CW output goes low, PLS-H goes high to cause an add operation and the low output of AND gate U33D clocks U32A through NAND gate U31D to cause the Q output (MNE-H) to go high.

When the RPG is turned CCW, the CCW output will go high at a time when the CW output is low. $90^{\circ}$ later CW goes high and AND gate U33D output goes high. When, $90^{\circ}$ later, CCW goes low, U33D output goes low and clock U32A through U31D. The CW output is still high so the output of NAND gate U21A, PLS-H, is low. A subtraction operation is directed rather than an addition operation.

The enabling input to NAND gate U28A is from a cross-connected pair flip-flop, U31B/C. TRD-L is low only during the power detect operation when the instrument is first turned on. TRD-L is also coupled back to NAND gate U25B and U3A to inhibit the front panel manual controls during power detect.
Divide-by-five counter U4 is used when the HF RF output unit is in use and the 1 MHz (COARSE) step increment is selected. This is done to provide a fine control over the 1 MHz COARSE operation. Only every fifth input from the RPG can clock the MNE-H flip-flop, and control is improved.

Option 004 instruments have a 100 Hz resolution rather than 1 Hz resolution. Part of the changes required for this change is to shift R18 from its location shown on the schematic to a point between U30D pin 13 to 004 instruments are $100 \mathrm{~Hz}, 10 \mathrm{kHz}$ and 1 MHz

## SWEEP ENABLE CIRCUITS

The SW1 flip-flop, U23A, Q output (SW1-H) and SWON-H go high for all sweep operations. Selection of AUTO or MAN sweep controls the J input fo U23A through AND gate U23A and U22B when enabled by state $0 / 0$ at 19 (H). Selection of SWEEP OFF controls the K inputs for reset of U23A through NAND gate U22A.
Flip-flop U23B, also referred to as the F9 flip-flop, is the sweep rate control. When the instrument is first turned on the K input to U23B is high due to the state of the TRD flip-flop (U31B/U32C), so the $\bar{Q}$ output is set high.
When state $0 / 13,0 / 14$ or $0 / 15$ is reached the J input to U23 goes high and the system clock causes the Q output to go high. When U23B Q output is
/O A1A1 Switch Control Assy (Part 1)
SERVICE SHEET 19

## SERVICE SHEET 20 (cont'd)

high, NAND gate U25D is enabled and the system clock is coupled through to NAND gate U14C. These three states enable the sweep to step at the maximum clock rate ( 1 MHz ) during certain parts of the sweep operation

The $\bar{Q}$ output of the single sweep flip-flop, U21A, is high in the quiescent state. Since both inputs to AND gate U20A are high the level at the $S$ input to U21A does not affect the flip-flop.

When the SWEEP MODE switch is placed in the SINGLE mode and the SINGLE pushbutton is pressed, the output of AND gate U20A goes low to set the Q output of U21A high. The Q output of U21A (QSS-H) stays high for the period of one sweep width. The inverted system clock at the pin 2 input of OR gate U30A cannot reset U21A because instructions RQSS-H is low during the single sweep operation.

When the single sweep operation is concluded, instruction RQSS-H goes high, is inverted by U2D and enables OR gate U21A. The next inverted system clock resets both U21A and U23A (Q goes low and $\bar{Q}$ goes high).
When the single sweep was initiated, U21A $\bar{Q}$ went low to cause the output of AND gate U13A to go low. The pin 6 input to NOR gate U24B is also low so the J input is high at U23A, the SW1 flip-flop. The next clock pulse will cause the $Q$ output of U23A (SW1-H) to go high. SWON-H is also high during the time the output of U21

While the $Q$ output of U23B is high the system clock is coupled through NAND gate U25D to pin 10 of NAND gate U14C. Pins 9 and 11 of U14C are high because U23B Q is low. The system clock is coupled through NAND gate U14C to $15 A$. Since the D input to U15A is held high the $Q$ output goes high on the clock pulse. The inverted QSP-H) to go high. When state $0 / 11$ is reached 9 f U30C goe low to permit the inverted system cock to reset U15A and U15B (Q outputs go low) make them ready for the next system clock.

When one of the three other clock sources is to be used to drive U15A, state $0 / 9$ is reached, pin 12 of OR gate U30D goes low, the inverted system clock at OR gate U30D pin 11 resets U23B and the output of AND gate U20D resets U15A and U15B.

When U23B is reset $t$ NAND gate U25D is system clock pulses fro output from U25D is
NAND gate U14C.

When the SWEEP MO and the SWEEP RATI output of NAND gate NAND gate U10D whic 1 kHz ) clock to U10B igh because the high and used to inhibit U1
Pins 2 and 13 of NAN clock path is complet J14C. Pins 9 and 10 U15A is clocked and it

The next inverted syste high. This signal instr another sweep step. clock to clock U15B er clock is synchronized millisecond clock is de However, the dividers the propagation delay m shift. Also, durng pulses are received thr must be synchronized. When the FAST sweel of the circuit is the xcept that the out Q100-H) is high. In steps at the 1 kHz rate. When the SLO sweep similar to the MED mo U 10 is low, U10C is second $(20 \mathrm{~Hz})$ clock is

When the SWEEP MOI RPG is enabled. Op associated circuits is e in the MANUAL TL MNE-H is applied to th U14B; U14B pin 3 is U14B pin 4 is held hig coupled through to N . two inputs to U14C a by MNE-H. U15B is inverted system cloc MNE-H input is syng clock and provides QSF

## Y A1A

the circuits of the A1A1 assembly
all front panel switches except the set (or reset) certain flip/flops or may r use in other assemblies.
-H from flip/flop U15 shown on SS19. ate machine will go through the various ted by the operator. Principal inputs to eyboard via input KD2-L, the readout trol switches or the manual mode tuning

4-to-16 selector U26 (shown on SS19) rs in the DCU. Selector U26, which is rs in the DCU. Selector
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The circuits following the RPG CW and CCW outputs must detect when a manual entry has been made and also whether the input is an increase or decrease in frequency.

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Assume that the RPG is to be turned in the CW direction and that initially the CW output is low. The CCW output is low when the CW output goes high. When the CCW output goes high AND gate U33D is enabled and its high. When the CCW output goes high AND gate is high. When the CW output goes low, PLS-H goes high to cause an add operation and the low output of AND gate U33D clocks U32A through NAND gate U31D to cause the Q output (MNE-H) to go high.

When the RPG is turned CCW, the CCW output will go high at a time when the CW output is low. $90^{\circ}$ later CW goes high and AND gate U33D output goes high. When, $90^{\circ}$ later, CCW goes low, U33D output goes low and clocks U32A through U31D. The CW output is still high so the output of NAND gate U21A, PLS-H, is low. A subtraction operation is directed rather than an addition operation.

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Divide-by-five counter U4 is used when the HF RF output unit is in use and the 1 MHz (COARSE) step increment is selected. This is done to provide fine control over the 1 MHz COARSE operation. Only every fifth input from the RPG can clock the MNE-H flip-flop, and control is improved.

Option 004 instruments have a 100 Hz resolution rather than 1 Hz resolution. Part of the changes required for this change is to shift R18 from its location shown on the schematic to a point between U30D pin 13 to ground. The step increments

## SWEEP ENABLE CIRCUITS

The SW1 flip-flop, U23A, Q output (SW1-H) and SWON-H go high for all sweep operations. Selection of AUTO or MAN sweep controls the J input fo U23A through AND gate U23A and U22B when enabled by state $0 / 0$ at 19 (H). Selection of SWEEP OFF controls the K inputs for reset of U23A through NAND gate U22A.
Flip-flop U23B, also referred to as the F9 flip-flop, is the sweep rate control. When the instrument is first turned on the K input to U23B is high due to the state of the $\mathrm{T}_{\mathrm{A}}$ (R flip-flop (U31B/U32C), so the $\bar{Q}$ output is set high.
When state $0 / 13,0 / 14$ or $0 / 15$ is reached the J input to U23 goes high and the system clock causes the Q output to go high. When U23B Q output is

P/O A1A1 Switch Control Assy (Part 1)
SERVICE SHEET 19

## SERVICE SHEET 20 (cont'd)

high, NAND gate U25D is enabled and the system clock is coupled through to NAND gate U14C These three states enable the sweep to step at the maximum clock rate ( 1 MHz ) during certain part of the sweep operation

The $\bar{Q}$ output of the single sweep flip-flop, U21A is high in the quiescent state. Since both inputs to AND gate U20A are high the level at the S input to U21A does not affect the flip-flop.

When the SWEEP MODE switch is placed in the SINGLE mode and the SINGLE pushbutton is pressed, the output of AND gate U20A goes low to set the $Q$ output of U21A high. The $Q$ output of U21A (QSS-H) stays high for the period of one sweep width. The inverted system clock at the pin because of OR gate U30A cannot reset ingle sweep operation.

When the single sweep operation is concluded instruction RQSS-H goes high, is inverted by U2 and enables OR gate U21A. The next inverted system clock resets both U21A and U23A (Q goe low and $\overline{\mathrm{Q}}$ goes high)
When the single sweep was initiated, U21A $\bar{Q}$ went low to cause the output of AND gate U13A to go low The pin 6 input to NOR gate U24B is also low so the J input is high at U23A the SW1 flip flop The next clock pulse will cause the $Q$ output of U23A (SW1-H) to go high. SWON-H is also high during the time the output of U21A is low controlled by the QSS flip-flop U21A
While the Q output of U23B is high the system clock is coupled through NAND gate U25D to pi 10 of NAND gate U14C. Pins 9 and 11 of U14C are high because U23B $\bar{Q}$ is low. The system clock is coupled through NAND gate U14C to U15A Since the D input to U15A is held high the Q output goes high on the clock pulse. The inverted system clock then causes the $Q$ output of U15B (QSP-H) to go high. When state $0 / 11$ is reached pin lock to rese U15A and U15B (Q outputs go low)有

When one of the three other clock sources is to used to drive U15A, state $0 / 9$ is reached, pin 12 o OR gate U30D goes low, the inverted system clock at OR gate U30D pin 11 resets U23B and the output of AND gate U20D resets U15A and U15B.

When U23B is reset the Q output goes high and NAND gate U25D is inhibited to prevent furthe system clock pulses from reaching U15A. The high output from U25D is also used to partially enable NAND gate U14C.

When the SWEEP MODE switch is set to AUTO and the SWEEP RATE swtich is set to MED, th output of NAND gate U10A goes high to enable NAND gate U10D which supplies the 1 millisecond $(1 \mathrm{kHz})$ clock to U10B. The pin 5 input to U10B is high because the high output of U10A is inverted and used to inhibit U10C.
Pins 2 and 13 of NAND gate U14A are high so the clock path is completed through to NAND gate 14C. Pins 9 and 10 of $U 14 \mathrm{C}$ are both high so 15 A is clocked and its $Q$ output goes high.

The next inverted system clock causes QSP-H to go high. This signal instructs the system to advance another sweep step. Using the inverted system clock to clock U15B ensures that the 1 millisecond clock is synchronized to the system clock. The millisecond clock is derived from the system clock However, the dividers are low power devices and he propagation delay may result in excessive phase hift. Also, during manual sweep, asynchronou pulses are received through U14B and U14C which must be synchronized.
When the FAST sweep rate is selected, operation of the circuit is the same as in the MED mode except that the output of AND gate U33B (Q100-H) is high. In this mode the sweep is 100 teps at the 1 kHz rate.

When the SLO sweep rate is selected, operation is similar to the MED mode except that the output of 10 is low, U10C is enabled, and the 10 milli second ( 20 Hz ) clock is used.

When the SWEEP MODE switch is set to MAN, the RPG is enabled. Operation of the RPG the associated circuits is essentially the same as it wa in the MANUAL TUNE RESOLUTION mode. MNE-H is applied to the pin 5 input of NAND gate U14B; U14B pin 3 is held high by U23B $\bar{Q}$ and U14B pin 4 is held high by QMSW-H so MNE-H is coupled through to NAND gate U14C. The other two inputs to U14C are high so U15A is clocked by MNE-H. U15B is then clocked by the next nverted system clock. This ensures that the MNE-H input is synchronized with the system clock and provides QSP-H.


Figure 8-54. P/O A1A1 Switch Control Assembly Component Locations (Part 2)


Figure 8-55. A1A1 Switch Control


## SERVICE SHEET 21

## P/O A1A2 KEY CONTROL ASSEMBLY AND KEYBOARD

The circuits in the A1A2 assembly are shown schematically on Service Sheets 21 and 22. The keyboard scan, encoding circuits and the keyboard shift register are all contained in this assembly. Also shown on Service Sheet 21 is the keyboard printed circuit board schematic.

The Model 8660C keyboard is unique in that there are no mechanical contacts. Basically the keyboard consists of ten pairs of printed circuit pulse transformers with metallic spring leafs suspended adjacent to them. When a key is pressed the associated pulse transformer is inductively shorted.

The pulse transformer primaries are connected in series pairs between the 100 kHz clock pulses and a 1 of 10 selector, U26. The pulse transformer secondaries are connected in series between the inputs of a dual comparator, U20. The pulse transformer pairs are connected so that secondary currents cancel until a key is pressed.

The keyboard clock (KYB CK) is connected to all of the transformer pairs. However, only one transformer pair is selected at any given time by U26. The keys are scanned sequentially, 10 times for numeric data, then 10 times time the $D$ output of divide-by-ten U25 is active The $Q$ and $\bar{Q}$ outputs of U17B determine which of the U20 comparators is being strobed. The lower comparators is being strobed. The lower comparator is the numeric key detector.

When the lower U20 comparator is being strobed, if a numeric key is pressed a positive going pulse appears at U20 $\mathrm{E}_{0}$ output. This causes the one-shot a positive going pulse appears at $\mathrm{U} 20 \mathrm{E}_{0}$ output. This causes the one-shot
U 19 to change states ( $\overline{\mathrm{Q}}$ goes low). The low output of $\mathrm{U} 19 \overline{\mathrm{Q}}$ inhibits the U19 to change states (Q goes low). The low output of U19 Q inhibits the
clock gate (U16C) to the divider (U25). U25A, B, C and D outputs retain the clock gate (U16C) to the divider (U25). U25A, B, C and D outputs retain the multiplexer U12 which is shown on Service Sheet 22 . Numeric data cannot affect the non-numeric data circuits because OR gates U24A, B, C and D outputs are held high by NAND gate U16B.

U19 is a monostable multivibrator which may be re-triggered during its period of about 15 microseconds. The period of U19 will be extended as long as the key is pressed since re-triggering pulses are received from U20 every 10 microseconds.

Operation when a non-numeric key is pressed is essentially the same as it is for a numeric key. The upper U20 comparator is enabled by U17B Q and both U16B inputs are high. The low level at the output of U16B enables U24A, B, C and D to couple the data through to one-of-ten selector, U23. The outputs of U23 correspond to the input binary weighted code.
U15 is a multiplexer which processes data from U23 in the local mode or from external programming circuits in the remote mode. The only data functions processed through U15 are the step up, step down and center frequency. In the local mode 15 pin 1 (select) selects inputs $1 \mathrm{~A}, 1 \mathrm{~B}$, and 1 C becaun 1) is low so inputs $0 \mathrm{~A}, \mathrm{~B}$ and 0 C are selected. In either case the $\mathrm{Z}_{\mathrm{A}}, \mathrm{Z}_{\mathrm{B}}$ and $\mathrm{Z}_{\mathrm{C}}$ outputs correspond to the $\mathrm{A}, \mathrm{B}$ and C inputs.

## SERVICE SHEET 21 (Cont'd)

The gating circuits to the right of U15 and U23 generate various qualifiers and instructions. As an example, if the CF key is pressed (code 8, 1000) the $0_{8}$ output of U23 is low, $\mathrm{U} 15 \mathrm{Z}_{\mathrm{C}}$ is low and the output of U22D is high. At all other times, when the CF function has not been initiated, qualifier CF-H is low.

Flip/flop U7B functions in the microprogram to prevent an entry operation from being made before a unit key is pressed. A unit key must be pressed to complete the justification process. The F3 flip/flop (U7B) K input goes high when qualifier QU1 (U21B pin 8) is high and instruction KF3-L is low which low. The F3 J input mue next clock pulse resets U7B and qualifier F3 goes complete the cycle. This is high in order to make the Q output go high to becomes active when the machine is active in any $1 / 12,1 / 13$ or $1 / 0$ and U7B is clocked The $Q$ any one of four states, $1 / 1$, CLEAR KYBD key is pressed generating $Q$ output will also go high if the (KD2-L) provides a signal to the F10 flip/flop on the A1A1 U23. U17A Q key has been pressed or when CMND-P-L goes low in the remote mode.

J -K flip/flop U7A is used in a synchronizing process; it is connected as a "D" type flip/flop. The "D" input from U19 is asynchronous since it is a response to manual press and release of a key. The synchronized KDN-H output ensures correct machine state action.


Figure 8-56. Keyboard Assembly Front View


Figure 8-57. Keyboard Assembly Rear View


Figure 8-58. P/O A1A2 Key Control Assy Component Locations (Part 1)


370

| 37 © |
| :--- |
| 28 |

$$
\begin{array}{lll}
\mathbf{3 7} \boldsymbol{N}^{-1}<{ }^{6} & \text { RMT CF-L } \\
\mathbf{2 0} \boldsymbol{G}^{-1} \ll^{-5} & \text { TR } \mathrm{L}-\mathrm{L}
\end{array}
$$

$$
\begin{array}{lll}
28 \mathrm{~J}^{-1}<\mathrm{C}^{11} & \text { JF3-L } \\
28<^{3} & {[J U S \text { KF3 JF2]-L }}
\end{array}
$$

$$
\begin{array}{lll}
28 \boldsymbol{A}^{-2} \ll \\
37 \boldsymbol{E}^{-1} \ll & \text { CMUS KF3 JF2] }
\end{array}
$$


$2108:$

$\sum_{5022}^{n 20}$



## SERVICE SHEET 22

## P/O A1A2 KEY CONTROL ASSEMBLY

The A1A2 key control assembly circuits are shown schematically on Service Sheets 21 and 22. The circuits shown on this Service Sheet consist of the recirculating keyboard register and the circuits which control it.

Multiplexer U12, when a keyboard numeral is being entered (ETK $\emptyset$-L is active), couples the data to U5 which is a one digit, 4 bit-register (referred to as the $\mathrm{K} \emptyset$ register).

After the data is stored in $\mathrm{K} \emptyset$ a train of 10 clock pulses transfer the data to the main keyboard shift register consisting of $\mathrm{U} 4, \mathrm{U} 6, \mathrm{U} 14$ and U 13 .

U6 and U4 are dual 8 bit registers. Data bits 1 and 2 for digits 3 through 10 are stored in U6 and data
bits 4 and 8 for digits 3 through 10 are stored in U4. U14 and U13 are one digit four bit registers. U14 stores digit 2 and U13 stores digit 1.

Note that the output of the main keyboard register is coupled back to U 5 thorugh U 12 while the train of 10 clock pulses is present. This is true because ETK $\emptyset$-L is now in the quiescent (high) state. The cycle continues until all of the required numeric entries are made. When the last digit has been entered (the least significant digit) it will be so positioned in the register that it will be the first digit clocked out. The first digit clocked in will be the last digit clocked out.

In the local mode when the keyboard data is clocked out, it is also clocked back into the main keyboard register, through multiplexer U11. U12 and U5 are bypassed.

The control gates for the keyboard register are conventional.


Figure 8-60. P/O A1A2 Key Control Assy Component Locations (Part 2)


## SERVICE SHEET 23

## P/o A1A3 READOUT CONTROL ASSEMBLY

Most of the circuitry shown on this service sheet is used to justify (properly locate) the decimal point in the readout. Following entry of a multidigit number, units are selected and the number is shifted left or right in the keyboard register as controlled by the following circuitry which determines position of the decimal point.

The $\mathrm{MHz}, \mathrm{kHz}$ and Hz inputs are applied to the B inputs of comparator U11 The A inputs to comparator U11 are from justification counter, U20. The purpose of U 11 is to detect when $\mathrm{A}=\mathrm{B}$.

The justification counter, U20, is a decade counter which operates only after a decimal point or a units entry has been made.

Referring to the Algorithmic State Machine, (flow graph), assume that the first keyboard entry is a numeral and follow the machine states from 0/0 first keyboard entry is a numeral and follow the machine states from instruction that directly affects the circuits shown on Service Sheet 23 .

The instructions in state $1 / 5$ are RF2-L which resets FF2, RKB-L which resets the keyboard and RJCT-L which resets the justification flip-flop, U14A. RJCT-L is also inverted by U31C to reset the counter, U20, to nine (1001).

The next state, $0 / 2$, contains the instruction ETK 0 -L. This causes the numeric data to be stored in the K 0 register.

The next state, $0 / 3$, contains instruction K 0 TK-L (KD to keyboard register and a train of 10 clock pulses. These clock pulses transfer the data from the single digit K 0 register to the least significant storage in the ten digit keyboard storage register.

## NOTE

See Service Sheets 21 and 22 for a more complete analysis of the keyboard register.

When a decimal point is entered after a numeric entry the machine state path is from state $0 / 0$ through states $4 / 0,5 / 0$ and $5 / 1$ to state $3 / 5$.

In state $3 / 5$ instruction SJCT-L (set justification counter) appears. This instruction, which has a low assertive state, is applied to NOR gate U13A pin 3. The second input to NOR gate U13A is the inverted system clock which is high when SJCT-L appears. When the inverted system clock at ${ }^{\text {E }} 13 \mathrm{~A}$ pin 2 goes low the clock input to U14A goes high and causes the Q output to go high.

## SERVICE SHEET 23 (Cont'd

When U14A Q goes high NAND gate U33A is enabled. Pin 4 of U33A is high because B9-L is not active at this time. The system clock at NAND gate because B9-L is not active at this time. The system clock at NAND gate
U35B pin 3 is applied to U33A pin 5 when CK10 CK is high and JUS or QJO are high. Pin 2 of U33A is high because KDTK is low.
The output of NAND gate U33B is high since QJO is low and NAND gate The output of NAND gate U33B is high since QJO is low and NAND gate
U30D is enabled for a period of nine clock pulses. The train of clock pulses ends when B9-L goes low and inhibits U33A.
The justification counter, U20, starts at a count of 9 in the local mode. The 9 clock pulses it receives cause it to stop one count lower than where it started. In other words, the first entry after a decimal point would cause the counter output to be an 8 , the next entry a 7 , etc.

The output of NAND gate U35B pin 6 is also used to clock the keyboard register via line KCK-L. The output burst of 10 clock pulses shifts the new entry to the correct sequential position as described in Service Sheets 21 and 22.

So far, justification has not taken place; the justification counter has merely deducted the number of entries after the decimal point from 9. Flip/flop U14B has not yet been clocked because the JUS-L high level has been inverted by U31E to inhibit AND gate U32B.

As an example of circuit operation assume that 12.34 has been entered and the output is to be 12.34 kHz . Referring to the Algorithmic State Machine it can be seen that the UNITS path is the same as the numeral path until state $6 / 0$ is reached. The qualifier following state $6 / 0$, NUM $-H$, is not active so the next state is $0 / 4$ which contains instruction $\mathrm{RK} \emptyset-\mathrm{L}$ (reset $\mathrm{K} \emptyset$ register).
RK $\emptyset-\mathrm{L}$ is the output of AND gate U32D. The inputs to U32D are from OR gate U21C which is high because JUS-L is not active and from AND gate U9A. ST04-L is active by virtue of being an output of state $0 / 4$ and the low level is inverted by U24E to enable U9A. The system clock is then coupled to AND gate U32D to produce RK $\emptyset$-L.

Qualifier QU1-H is active for state $0 / 4$ so the next state is $1 / 6$ which contains instructions JUS-L, KF3-L and CK10J-L.
When JUS-L goes low it is inverted by U31E and applied to AND gates U25A and U32B. The second input to U32B is from OR gate U21D. The output of OR gate U21D is high because input pin 13 is connected to B9-L which is high.

The low to high output transition of U32B clocks U14B. Since the B inputs to U11 are a $6(0110)$ and the A inputs are a $7(0111)$, both $\mathrm{A}=\mathrm{B}$ and $\mathrm{A}<\mathrm{B}$ are low. The D input to U14B is low and clocking U14B causes the Q output to go low.
The low Q output of U14B is applied to one input of NOR gate U13B. The The low Q output of U14B is applied to one input of NOR-H which is also low. The high input to OR gate U21A at pin 1 is coupled through to pin 10 of AND gate U32C. Pin 2 of OR gate U21A is also held high by the inverted low $A=B$ level.
The second input to AND gate U32C is from AND gate U25A. U25A pin 2 is held high by the inverted JUS-L level and pin 1 is held high by the local line. The high output of U25A enables AND gate U32C and QJ $\emptyset$ - H goes high.

## SERVICE SHEET 23 (Cont'd)

When QJQ-H goes high it holds the instrument in state $1 / 6$ until justification requirements are met. QJQ-H enables NAND gate U35B thro through U30D.

The clock train is again stopped after nine clock pulses by the action of B and the outputs of U20 and U2 are compared by U11. Since both of inputs to U11 are now 6 ( 0110 ), $A=B$ goes high to cause the $D$ input U14B to go high.

When U11 $\mathrm{A}=\mathrm{B}$ is a high the justification requirements are satisfi However, several things must happen before state $1 / 6$ may be left.

The $A=B$ high level is inverted by U31A and applied to pin 2 of OR $g$ U21A. This does not immediately affect the output of U21A because output of NOR gate U13B is held high by the low Q output of U14B and CKB-H level which is low.

U14B is clocked by AND gate U32B as follows: U32B pin 5 is still held $h$ by the inverted JUS-L low level. The second input to U32B is from OR g U21D. When B9-L goes low, pin 13 of U21D is also low. The inverted syst clock at pin 12 of U21D is high so the output of U32B remains high. On 1 next clock the inverted clock goes low and the output of U32B goes lo
This does not clock U14B because a D type flip/flop may be triggered or This does not clock U14B because a D type flip/flop may be triggered or
on a positive going pulse. The next time the inverted clock goes high is at on a positive going pulse. The next time the inverted clock goes high is at
beginning of the tenth clock; this clocks U14B and causes the Q output to heginn.

The high Q output of U14B inhibits NOR gate U13B. Since both inputs OR gate U21A are now low AND gate U32C is inhibited and QJ $\emptyset-\mathrm{H}$ g ow. The machine state progression is now through states $6 / 14,1 / 1,4 / 1,1$ $4 / 9,4 / 10$ and $5 / 10$ to $0 / 0$. The instrument is now ready for the next en
(function).

Now assume that 12.34 kHz was entered by accident, it should have be 12.34 MHz .12 .340 is still stored in the keyboard register so all that necessary to start the justification process over is to press the MHz key.

Operation of the justification circuit is the same as it was for kHz exce that now the input to 011 is a 3 (0011) and the output of U20 is a 6 ( 011 QJD-H goes high as it did in the previous example. QJD-H stays high u QJQ-H goes high as it did in the previous example. QJD-H stays high u
three trains of clock pulses cause the output of U20 to reach $3(0011)$ a once again U11 A=B is high. QJD-H is caused to go low in the same man as in the previous example

For a third example assume it is decided that 12.340 kHz was, after all, t desired output frequency.

Initiation of the justification cycle is the same as it was in the previous tr examples. How, however, the A inputs to U11 are a 3 (0011) and the inputs are a $6(0110)$ so $\mathrm{A}<\mathrm{B}$ is high. This high level at pin 10 of NOR gi U13C holds the D input of U14B high and U14B is clocked as it was befc but no output change results since the $Q$ output was already high.

## SERVICE SHEET 23 (Cont'd)

When QJ0-H goes high it holds the instrument in state $1 / 6$ until the justification requirements are met. QJQ-H enables NAND gate U35B through OR gate U23A. QJ $\emptyset$-H also enables NAND gate U33B which then clocks U20 through U30D.

The clock train is again stopped after nine clock pulses by the action of B9-L and the outputs of U20 and U2 are compared by U11. Since both of the inputs to U 11 are now 6 (0110), $\mathrm{A}=\mathrm{B}$ goes high to cause the D input to U14B to go high.

When U11 $\mathrm{A}=\mathrm{B}$ is a high the justification requirements are satisfied. However, several things must happen before state $1 / 6$ may be left.

The A=B high level is inverted by U31A and applied to pin 2 of OR gate U21A. This does not immediately affect the output of U21A because the output of NOR gate U13B is held high by the low Q output of U14B and the CKB-H level which is low.

U14B is clocked by AND gate U32B as follows: U32B pin 5 is still held high by the inverted JUS-L low level. The second input to U32B is from OR gate U21D. When B9-L goes low, pin 13 of U21D is also low. The inverted system clock at pin 12 of U21D is high so the output of U32B remains high. On the next clock the inverted clock goes low and the output of U32B goes low. This does not clock U14B because a D type flip/flop may be triggered only on a positive going pulse. The next time the inverted clock goes high is at the beginning of the tenth clock; this clocks U14B and causes the $Q$ output to go high.

The high Q output of U14B inhibits NOR gate U13B. Since both inputs to OR gate U21A are now low AND gate U32C is inhibited and QJ $\emptyset-\mathrm{H}$ goes low. The machine state progression is now through states $6 / 14,1 / 1,4 / 1,1 / 9$, $4 / 9,4 / 10$ and $5 / 10$ to $0 / 0$. The instrument is now ready for the next entry (function)

Now assume that 12.34 kHz was entered by accident, it should have been 12.34 MHz .12 .340 is still stored in the keyboard register so all that is necessary to start the justification process over is to press the MHz key.

Operation of the justification circuit is the same as it was for kHz except that now the input to 011 is a 3 (0011) and the output of U20 is a $6(0110)$. QJD-H goes high as it did in the previous example. QJD-H stays high until three trains of clock pulses cause the output of U20 to reach 3 (0011) and once again U11 A=B is high. QJD-H is caused to go low in the same manner as in the previous example.

For a third example assume it is decided that 12.340 kHz was, after all, the desired output frequency.

Initiation of the justification cycle is the same as it was in the previous two examples. How, however, the A inputs to U11 are a 3 (0011) and the B inputs are a $6(0110)$ so $A<B$ is high. This high level at pin 10 of NOR gate U13C holds the D input of U1" ${ }^{4}$ B high and U14B is clocked as it was before but no output change results since the $Q$ output was already high.

## SERVICE SHEET 23 (Cont'd)

The low $\mathrm{A}=\mathrm{B}$ output of U11 is again inverted and applied to OR gate U21A to enable AND gate U32C and again cause QJ $\emptyset$-H to go high (U32C pin 9 is caused to go high in the same manner as in the previous examples).

U11 is continually comparing the outputs from U20, U1B and U21B. The first clock to U20 causes the output to go to 4 ( 0100 ), the second to 5 (0101) and the third to 6 (0110). Justification has been accomplished, $\mathrm{A}=\mathrm{B}$ is high, U21A is inhibited and QJD-H immediately goes low. The state progression back to state $0 / 0$ is the same as it was in the previous examples.

During all of these justification counts, outputs from KCK-L to the keyboard register cause the entry to be shifted to positions consistent with units and decimal point.

It may be seen from the foregoing examples that left shifting (from kHz to MHz ) takes three trains of clock pulses, while right shifting (from MHz to kHz ) takes only three clock pulses.

The decimal point storage, U3, is a $4 \times 4$ file. It stores 4 four-bit words. These words are selected by the outputs of U22A and U22B as follows: word 1 , center frequency 00 ; word 2 , sweep width 01 ; word 3 , step (increment) 10 and word 4 , keyboard 11.

The inverted system clock is applied to pin 12 ( $G_{W}$ ) of U3 where it is used as the write clock. W ${ }_{A}$ and $W_{B}$ (write) inputs are controlled by AND gates U22A and U22B which are, in turn, controlled by the KYBD, STEP or SWP WIDTH pushbuttons in the local mode. When these pushbuttons are all inactive the center frequency is selected.

When operating in the remote mode only the center frequency is displayed. It is displayed in MHz only. In the remote mode the LOCAL-H line is low. This low level is inverted by U31F and used to reset the justification counter, U20, to zero. OR gates U1C and U1D provide the inputs to U3 in the remote mode. Pin 10 of U1C and Pin 12 of U1D are connected directly to the output of U22A AND gate. Normally, in the local mode, the output of U22A is low.

When the remote mode is selected and LOCAL-H goes low it is applied to INVERTER U6 and AND gate U30A. The output of AND gate U32A goes low, is inverted and applied to AND gate U25B The second input to AND gate U25B is QHF-H which is low.

Decoder U7 is one-of-ten selector. All outputs of the decoder are high except the one selected. The outputs of the decoder directly drive the decimal point LED's in the readout (the series resistors are for current limiting).

The gates shown to the right of decoder U7 are used to drive the $\mathrm{Hz}, \mathrm{kHz}, \mathrm{M}$ ( M and Hz are both used to display MHz ) and GHz lamps. NAND gates U26A, B, C and D are open collector lamp drivers. The common input to these gates is controlled by the combined functions of F2 and KPB. During the time when keyboard entries are being made, the KYBD pushbutton is pressed for readout of the entries, the units lamps are inhibited. When the entry is justified, F2-L goes low and the units lamps are then enabled.


Figure 8-62. P/O A1A3 Readout Control Assembly Component Locations (Part 1)


## SERVICE SHEET 24

## P/O READOUT CONTROL ASSEMBLY A1A3

The A1A3 assembly is shown schematically on Service Sheets 23 and 24.

The circuits shown on SS24 consist of the ten digit recirculating readout register, scan control for the readout and a blanking control for the readout.

When new information is to be clocked into the readout register from the T bus, TTRO-L goes low at pin 4 of NAND gate U5B and U5B output goes high. OPRO-L and ROI-L are normally high, so the output of AND gate U25B goes high to select the $\mathrm{I}_{1}$ inputs of multiplexer U17.
The outputs of multiplexer U17 are applied to U8, U27, U36, U37, U38 and U28. The last five IC's comprise the ten digit register which, in conjunction with other circuits shown on SS24 control operation of the readout.

While the output of AND gate U25 is high the preset enable (PE) to the sync register, U39, is also high. The register will function as a shift register, and, with the $J$ input high, the first four clock pulses will cause the Q outputs of U39 to go high. These outputs of U39, a 15 , ( 1111 ) is the scan synchronizing code.

The output of AND gate U25B also is used to partially control clock inputs to the readout and synch registers.

Many of the gates shown in the lower left of the schematic function to control the clocks. The output of NAND gate U15D clocks the recirculating register including U39, the synch register.

The inputs to NAND gate U15D are from three-input NAND gate U35C and U22C/U24F which function together as a three-input NAND gate. One or the other of these inputs to U15D will be high at any given time and the other input provides the clock pulses.
When new data is being clocked in NAND gate U35C drives NAND gate U15D to clock the recirculating readout register at the system clock rate, 1 MHz . NAND gate U35C is enabled by the output of U34D and the ADDCK-H input which remains high for the period of ten clock pulses required to clock in the information. The system clock pulses are coupled through AND gate U25C and inverted by U6D. C9 and R10 form a one-shot which effectively delays the clock while TTRO is going low. Inverter U24A again inverts the clock before it is applied to NAND gate U34B. Since NAND gate U5D output is high the output of NAND gate U34B goes low with the positive clock pulse to trigger flip/flop U34C/U34D. The output of U34D then goes high to complete the enabling process for NAND gate U35C.

## SERVICE SHEET 24 (Cont'd)

When the output of NAND gate U5D goes high the next system clock triggers one-shot U10 and the $\bar{Q}$ output at pin 6 goes low, typically for a period of 105 microseconds. The low level at $\mathrm{U} 10 \overline{\mathrm{Q}}$ sets the Q output of flip/flop U29 high and holds it high The low output from U20 $\overline{\mathrm{Q}}$ also inhibits U4C and blanks the readout through the brightness control.
When NAND gate U4C is inhibited the output goes high and enables one input to AND gate U22C. Since the Q output of flip/flop U29 is high, the inverted system clock is coupled through NAND gate U15B back to the pin 10 input of AND gate U22C.

The third input to AND gate U22C is enabled when TTRO-L goes high and causes the output of NAND gate U5D to go low. Flip/flop U34C/U34D changes state, AND gate U22C is enabled, and the system clock is coupled through inverter U24F and NAND gate U15D to clock the recirculating data. Note that the MSD register, U8, is not being clocked.

As long as the Q output of one-shot U 10 is low, (approximately 100 microseconds) AND gate U22C is enabled and the system clock drives the recirculating portion of the register including the sync register, U39. During this portion of the cycle insignificant leading zeros are blanked.
Whenever a leading zero reaches the sync register, U39, all of its outputs are low so the inputs to NOR gates U13D and U19D are low and their outputs are high. The low output of NAND gate U15A is applied to pin 5 of NOR gate U19B. Pin 6 of NOR gate U19B is also low since the QH outputs of U38 and U28 are high. The sync code (1111) has recirculated to the QH digit of the register. These two high levels are applied to NAND gate U9C which provides the low input to NOR gate U19B. The pin 10 input to AND gate U18C is high. Assume for the time being that the other two inputs to AND gate U18C and the output are all high (these inputs will be discussed later in this text). The high inputs to OR gates U23B, C and D cause the outputs to go high. The output of U18C is inverted by U6F to drive the output of AND gate U25D low. These outputs comprise the blanking code, $14\left(\begin{array}{llll}1 & 1 & 1 & 0\end{array}\right)$ which will recirculate in the position of a leading zero.

The information in the readout register continues to recircul ate until the $\bar{Q}$ output of U10 returns to a high state. Pin 13 ( $\overline{\mathrm{S}}$ ) of flip/flop U29 also goes high to allow U29 to function as a J-K flip/flop. U29 Q remains high and the data continues to recirculate until the sync code (15) reaches the sync register, U39.

When the sync code reaches U39 all of the outputs go high to enable the K input to flip/flop U29. The next system clock causes the $\bar{Q}$ output of U29 to go high. The scan cycle is not initiated.

## SERVICE SHEET 24 (Cont'd)

When the $\bar{Q}$ output of flip/flop U29 goes high, NAND gate U9B output goes low to enable the one-of-twelve selector, U5, on the readout assembly (SS36). The second input to NAND gate U9B at pin 4 is high because command TTRO-L is high.

The high level at the $\bar{Q}$ output of flip/flop U10 enables NAND gate U4C to allow the 5 kHz SCANCK to be applied to AND gate U22C. The input to pin 9 of U22C is held high by flip/flop U34C/U34D and the pin 10 input is held high by the output of NAND gate U15B. The clock output of AND gate U22C is inverted and applied to NAND gate U15D. The second input to U15D is held high because flip/flop U34C/U34D inhibits NAND gate U35C.

It takes only six clock pulses at the 5 kHz rate (SCANCK) to clock the information in the readout register to the ROM's in the readout assembly.

When the six clock, 5 kHz train has clocked the nine data digits to the readout assembly the sync code (15) has recirculated to the QE output of the eight-bit registers. These outputs all go high to enable the J input of flip/flop U29. The next clock pulse causes the Q output of U29 to go high and couple the system clock through NAND gate U15B back to input pin 10 of AND gate U22C. The input to pin 11 of AND gate U22C is high because the 5 kHz clock is low. The system clock continues the recirculating process for four system clock periods at which time the sync code (15) again reaches U39. The K input to flip/flop U29 causes the $\bar{Q}$ output of U29 to go high and restart the scan cycle.

The scan cycle continues without interruption until the readout register contents are changed by a new entry.

Blanking AND gate U18C is inhibited in several different ways in conjunction with selected frequency units.
When GHz is selected, input pin 9 of NOR gate U19C goes high, the output goes low and AND gate U18C is inhibited. Blanking of the MSD still occurs if the MSD is a zero because the low Q3 output of U8 turns off transistor switch Q1 in the readout assembly.
When MHz is selected all leading insignificant zeros are blanked until the sync code (15) reaches QE in the 8-bit registers. All inputs to AND gate U18A are high and the output also goes high. The high input to NOR gate U19A causes the output to go low and inhibit AND gate U18C. Blanking of zeros following the MHz decimal point is prevented.

When kHz is selected all leading zeros are blanked until a number is reached or the sync code reaches $Q_{B}$ of the 8 -bit registers. All inputs to AND gate U18B go high and the output goes high. The high input to NOR gate U19A causes the output

## SERVICE SHEET 24 (Cont'd)

to go low and inhibit AND gate U18C. Blanking of zeros following the kHz decimal point is prevented.

When Hz is selected all leading zeros are blanked.
nputs OPR-L and OPRO-L are used only in option $004,100 \mathrm{~Hz}$ resolution to 1.3 GHz resolution $(200 \mathrm{~Hz}$ to 2.6 GHz resolution)instruments. These inputs last for two clock pulses and they force the two least significant digits to zero.

Input ROI-L establishes priority for the readout during manual sweep.

When one of the pushbuttons is pressed to call up the contents f a given register it takes priority and is displayed regardless of any change in manual sweep. When the pushbutton is released the readout will again display the manual sweep frequency.
Whenever the selected output frequency of the RF Section is 1.3 GHz or higher the DBL-L line goes low. When the DBL-L line goes low it is inverted and applied to NAND gate U35A. This signal, in conjunction with other inputs to U35A cause flip-flop U5A/U5C to change states. The output of NAND gate U5A goes low and inhibits AND gate U25C. U25C the Pens BCD 1 fra be the mist the least significant digit from hange state. This act being an odd number.

In Option 004 instruments operating above 1.3 GHz , the lowes increment is 200 Hz . In this configuration, the output of U5A increment is 200 Hz . In this configuration, the output of USA remains high for the first three BC inputs to the readout control area and control-line the reset of flip-flop U5C/U5A by means of U39, U19D and the QH outputs of U36, U37, U38 and U28. When the Q2 and Q3 outputs of U39 go high, the output of U19D goes low to reset flip-flop U5C/U5D to enable AND gate U25C. The fourth input and all higher digits may be odd numbers.

Table 8-51. Readout Register Leading Zero Blanking

| MSD | ROM A |  |  |  |  | Romb |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{O}_{\mathrm{A}}$ | $\mathrm{O}_{\mathrm{B}}$ | ${ }^{0} \mathrm{C}$ | $\mathrm{O}_{\mathrm{D}}$ | $\mathrm{O}_{\mathrm{E}}$ | $0_{F}$ | $\mathrm{a}_{\mathrm{G}}$ |  | S |  |
| U8 | U27 | U36 | U37 | U38 | U28 | U36 | U37 | U38 | U28 | U39 |  |
| B | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | S | Initial state Hz |
| S | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 |  |
| 6 | s | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 |  |
| 5 | 6 | 5 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 |  |
| 4 | 5 | 6 | S | 0 | 0 | 0 | 0 | 1 | 2 | 3 |  |
| 3 | 4 | 5 | 6 | S | 0 | 0 | 0 | 0 | 1 | 2 |  |
| 2 | 3 | 4 | 5 | 6 | s | 0 | 0 | 0 | 0 | 1 |  |
| 1 | 2 | 3 | 4 | 5 | 6 | S | 0 | 0 | 0 | 0 |  |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | s | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | s | 0 | 0 |  |
| 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | S | B | Detect zero |
| B | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | S | Blank (code 14) |
| S | B | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 |  |
| 6 | S | B | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 |  |
| 5 | 6 | S | B | 0 | 0 | 0 | 1 | 2 | 3 | 4 |  |
| 4 | 5 | 6 | S | B | 0 | 0 | 0 | 1 | 2 | 3 |  |
| 3 | 4 | 5 | 6 | S | B | 0 | 0 | 0 | 1 | 2 |  |
| 2 | 3 | 4 | 5 | 6 | S | B | 0 | 0 | 0 | 1 |  |
| 1 | 2 | 3 | 4 | 5 | 6 | S | B | 0 | 0 | 0 |  |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | S | 0 | B | 0 |  |
| 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | s | B | B | Detect zero |
| Continue to final state. |  |  |  |  |  |  |  |  |  |  | Blank (code 14) |
|  | B | B | B | 1 | 2 | 3 | 4 | 5 | 6 | s | Final state. |

## SERVICE SHEET 24 (Cont'd)

Table 8-52. Readout Register Significant Zero Blanking Inhibit


> Table 8-53. Readout Register Recirculating Cycle

|  |  | $\mathrm{Q}_{\text {A }}$ | $\begin{gathered} \text { 20M A } \\ \stackrel{\uparrow}{Q_{B}} \end{gathered}$ | $\mathrm{a}_{\mathrm{C}}$ | $\mathrm{a}_{\mathrm{D}}$ | $\mathrm{O}_{\mathrm{E}}$ | $\mathrm{O}_{\mathrm{F}}$ | $0_{G}$ | $\begin{gathered} \mathrm{ROM} \\ \stackrel{\uparrow}{1} \\ \mathrm{O}_{\mathrm{H}} \end{gathered}$ | S |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| U8 | U27 | U36 | U37 | U38 | U28 | U36 | U37 | U38 | U28 | U39 |  |
| 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | s) | Initial State |
| s | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 |  |
| 6 | S | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 |  |
| 5 | 6 | s | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 \} | $5 \mathrm{kHz}$ |
| 4 | 5 | 6 | S | 0 | 0 | 0 | 0 | 1 | 2 | 3 |  |
| 3 | 4 | 5 | 6 | s | 0 | 0 | 0 | 0 | 1 | 2 |  |
| 2 | 3 | 4 | 5 | 6 | s | 0 | 0 | 0 | 0 | 15 | Detects code 15 |
| 1 | 2 | 3 | 4 | 5 | 6 | s | 0 | 0 | 0 | 0 |  |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | s | 0 | 0 | 0 | 1 MHz |
| 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | S | 0 | 0 | clock |
| 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | s | 0 | Return to initial state |

Model 8660C


Figure 8-64. P/O A1A3 Readout Control Assembly Component Locations (Part 2)


## SERVICE SHEET 25

## P/O ROM INPUT ASSEMBLY A1A4

The A1A4 (SS25 and 26) and the A1A5 (SS27 and 28) assemblies contain most of the microprogramming circuits that control the entire instrument.

The A1A4 assembly contains the qualifier select circuit shown on SS25 and the seven flip/flops, ROMs and qualifier flip/flops shown on SS26.

Because of the number of inputs from other assemblies to the circuit shown on SS25 the inputs are shown at the bottom of the page. The only output on SS25 is the output of U1 labeled A 26. This output provides the eighth address bit for the ROMs shown on SS26.

U18, U9, U19, U20, U21, U22 and U23 are four input one-of-sixteen selectors. The A, B, C and D inputs are positive logic binary 1248 format from the $A_{0}, A_{1}, A_{2}$ and $A_{3}$ outputs of the seven state flip/flops shown on SS26. These inputs are applied to all of the selectors in parallel. However, only one of the selectors is active at any given time.

One-of-ten selector U10 (only 7 outputs are used) is controlled by the $\mathrm{A}_{4}, \mathrm{~A}_{5}$ and $\mathrm{A}_{6}$ outputs of the seven state flip/flops shown on SS26. All of the U10 outputs are high except the one selected. The

D input to U10 is grounded because only three data bits are required to select the output (BCD 4, 2 and 1).

It is readily apparent from the circuit configuration that the state for any of the inputs to the code selectors is easily detected. As an example, assume that the inputs from the seven state flip/flops are all low. The U10 00 output is low and U23 (code 0 ) is selected. Since the A, B, C and D inputs to U23 are all low, input $\mathrm{E}_{0}$ is selected. The $\mathrm{E}_{0}$ input is qualifier F10-H. If an Entry has not been made, F10-H is low the $\overline{\mathrm{W}}$ output of U23 is high and the instrument is held in state $0 / 0$. If the F10-H input is high, the $\bar{W}$ output of U 23 goes low, the output of U1 goes high and the next state is selected.

In the foregoing example, assume that qualifier F10-H was high. Referring to the ASM chart it may be seen that the next state is $4 / 0(1000000)$. Since the input to U10 is now a 4 (100) U19 is selected. The A, B, C and D inputs to U19 are all low so once again $E_{0}$ input is selected. The input to $E_{0}$ is from the F7-H flip/flop shown on SS26. It may be seen on the algorithm that if F7 is high the next state is $0 / 1$, if low, $5 / 0$.

AND gate U2C combines CKA-H and CKB-H when they are both high to provide inputs to U20 and U21. These inputs are used in states $3 / 1,3 / 0,2 / 13$ and $2 / 12$.


Figure 8-66. P/O A1A4 ROM Input Assembly Component Locations (Part 1)



## SERVICE SHEET 26

## P/O ROM INPUT ASSEMBLY A1A4

The A1A4 (SS25 and 26) and the A1A5 (SS27 and 28) assemblies contain most of the micro-programming circuits that control the entire instrument.

The A1A4 assembly contains the qualifier select circuit shown on SS25. The seven-state flip/flops, ROM's, and qualifier flip/flops are shown on SS26.

Seven J-K flip/flops, U6A, U5A, U4A, U7B, U5B, U6B and U4B form the seven-state flip/flops. The outputs of these flip/flops provide seven of the eight address bits required to control the next state outputs of ROM's U11, U12 and U17 The outputs also control the qualifier selector circuits shown on SS25 and the output instruction selectors on SS28 and SS19.

The eighth address bit to the ROM's is supplied by the selector circuit shown on SS25. When the seven-state flip/flops are clocked all four of the outputs from ROM U11 and three of the outputs from ROM U12 determine the next machine state. The remaining output of ROM U12 and all four of the outputs from ROM U17 are used directly as output instructions.

The light emitting diodes (LED's) connected between the $\bar{Q}$ outputs of the seven-state flip/flops and +5 V indicate the machine state. These LED's light when the $\bar{Q}$ outputs of the flip/flops go low. Proper utilization of these LED's in the manual test mode will enable the technician to quickly isolate the cause of a problem to the assembly or even the circuit level In the automatic mode of operation the machine states change so rapidly that the LED's serve no useful purpose.

At the far left of the schematic, U7, a J-K flip/flop is used to set the manual test mode. When TP9 is momentarily grounded $\bar{Q}$ goes low to inhibit the clock gate, U8A. Momentarily grounding TP8 will reset the flip/flop causing the $\bar{Q}$ output to go high and enable the clock gate, U8A. This returns the instrument to the automatic mode. The PRDT-L (power detect) input, which is low when the instrument is first turned on ensures that the automatic mode of operation is selected.

In order to use the manual test mode facilities it is necessary to momentarily ground or pulse the manual test point, TP9. The machine state may be $0 / 0$ (all LED's out) or may be any state in an operation sequence. If state $0 / 0$ test point, is desired, momentarily ground or pulse the state $0 / 0$ test point, TP10 Any machine state may now be set by momentarily grounding or pulsing the appropriate seven-state flip/flop test points.

## SERVICE SHEET 26 (Cont'd)

If, for instance, TP7, TP4 and TP1 were momen tarily grounded or pulsed, the machine state would be $4 / 9$ ( 100 1001). The ASM chart shows the qualifier QEI (qualifier entry instruction) following state $4 / 9$. If an entry instruction (CF, STEP or SWP) is being made (key held down), pressing the MAN SW microswitch should cause the next state to be 5/9 (101 1001) as shown by the LED's. If the state $5 / 9$ is not present, the operation was incorrect. Refer to Table 8-2, Mnenmonics Information, locate qualifier QEI, read across the page to determine where the qualifier originates and refer to the applicable service sheet to effect necessary repairs.

When NAND gate U8A pin 1 goes low pin 3 goes high to enable AND gate U2B. The clock pulse source is now flip/flop U15B. Normally, the $\overline{\mathrm{R}}$ and CK inputs to U15B are held low by R2 and the $\bar{Q}$ output is high. As soon as SW1 NC contacts are opened the R input to U15B goes high. When the SW1 NO contacts are closed the U15B CK goes high but this does not affect the output since J-K flip/flops are triggered by a negative-going transition. When SW1 is released it is returned to the NC position. The negative-going transition at the CK input causes U15B $\bar{Q}$ to go low. The output of AND gate U2B goes low and the outputs of inverters U13C and U13F go high. When the NC contacts of SW1 are again closed, the $\overline{\mathrm{R}}$ input to U15B again goes low to cause the $\overline{\mathrm{Q}}$ output to go high, AND gate U2B output goes high and the outputs of inverters U13C and U13F go low to clock the seven-state flip/flops.

AND gates U2A and U2D are used to reset the seven-state flip/flops to state $0 / 0$ when PRDT-L is low or when TP10 is momentarily grounded or pulsed.

The J-K flip/flops shown in the lower part of the schematic provide qualifiers; most of which are used in the selector circuits shown on SS25. These flip/flops are all clocked by the system ( 1 MHz ) clock. They are also reset ( $\overline{\mathrm{Q}}$ goes high) when PRDT-L is active or TP10 is momentarily grounded or pulsed.

Flip/flop U16A generates the F7 qualifier. The K inputs is an instruction (KF7-H) which appears in states $2 / 9$ and $1 / 0$. The $J$ input goes high whenever JF7B-L or (JF7A, ILD)-L goes low. F7 is fundamentally the sweep flip/flop but it also functions in the remote mode

U15A is the sweep ramp qualifier flip/flop F8. It appears in states 6/11 and 4/11.

U14B (IUP) inhibits the sweep up operation when QCTM-H (qualifier count maximum) on the sweep count assembly A1A8 goes high.

U14A (IDN) inhibits the sweep down operation when QCTZ (qualifier count zero) on the sweep count assembly A1A8 goes high.

U16B (F2) is active ( $\bar{Q}$ low) only for the first keyboard entry


Figure 8-68. P/O A1A4 ROM Input Assembly Component Locations (Part 2)


## SERVICE SHEET 27

## P/O ROM OUTPUT ASSEMBLY A1A5

The A1A4 (SS25 and 26) and the A1A5 (SS27 and 28) assemblies contain most of the microprogramming circuits that control operation of the entire instrument.

U17, shown in the center of the schematic, is the major control element for most of the circuits shown on this service sheet. It is a preset counter but is used only as a binary counter. When U17 is not active the master reset, $\overline{\mathrm{MR}}$, input is low and all of the $Q$ outputs are held low.

Any of the clock inputs, except the system clock, will inhibit NAND gate U9B and enable binary counter U17 by removing the reset input.

As an example of circuit operation, assume that the CK12-L input goes low. The output of AND gate U11A goes low to cause the output of NAND gates U9A and U9B to go high. This inhibits the MR input to U17. Since the output of U20A is low at this time, the output of inverter U10C is high and the clock is coupled through NAND gate U9C to U17.

When CK12-L went low it was inverted by U4E and used to enable NAND gate U19A. U19A, U19B, U19C and U20A form a detect circuit which provides the CKA-H output for the binary number selected.

In the case of CK12-L, when the output of U17 reaches 12 (1100), the output of U19A goes low and causes the output of U20A to go high.

While U19 and U20A were detecting a specific binary number, U18 was also detecting counts of 10,11 , and 12 . When the count of $10(1010)$ is reached the output of NAND gate U18C goes low and causes the output of U18D to go high. When the count of 11 (1011) is reached the CKB-H output remains high because NAND gate U18C is still enabled. When the count of ' 12 is reached NAND gate U18A is enabled so CKB-H is still high. The outputs of U20A (CKA) and U18D (CKB) are ANDed together in the system, and when the 12 count is reached, the combined signal enables the state machine to go to the next state. In doing so, the CK12-L input goes high again, causing reset of U17 through U11A and U9B.

NAND gate U18B produces the B9-L output which goes low on the 9th clock pulse. It is used in the readout control assembly to limit a normal tenclock train to 9 clocks.

The output labeled OPR-L is used in the readout control assembly to set the two least significant readout digits to 0 in Option 004 instruments.

Output A2TR-H enables output gates for the 12 digit portion of the A register assembly.

The A4 and A5 inputs are from the seven-state flip/flops in the switch control assembly, A1A4. The 2 -bit code on these inputs is decoded by the gates shown in the lower right corner of the schematic to produce one of four outputs. Output G20 enables the code 0 instruction decoder on A1A1. The outputs labeled 28, E, F and G enable the code 1, 2 and 3 instruction decoders shown on SS28.


Figure 8-70. P/O A1A5 ROM Output Assembly Component Locations (Part 1)


## SERVICE SHEET 28

## P/O ROM OUTPUT ASSEMBLY A1A5

The A1A4 (SS25 and 26) and the A1A5 (SS27 and 28) assemblies contain most of the microprogramming circuits that control operation of the entire instrument.

All of the gates shown on SS28 are controlled by the 4 -line-to-16-line instruction decoders U25, U17 and U8. These decoders have six inputs, all of which are required to decode to the single output. All outputs are high except the one decoded.

Note that the decoders are labeled CODE 1, CODE 2 and CODE 3. These code numbers and the output numbers of the decoders quickly reveal the machine state code as shown on the algorithm, which is the state of the seven-state flip/flops in the ROM input assembly.

The gates shown combine the decoder outputs to provide the desired instruction.

As an example, assume that output 6 of U25 is low. Decoder U25 is labeled CODE 1 (001) and the decoded output is $6(0110)$. The state code is $1 / 6$ and the outputs of the seven-state flip/flops is 001 0110. Instructions (JUS, KF3, JF2)-L are low.

The example quoted for the instructions in state $1 / 6$ is very simple. Generation of many of the instructions is more complex when the instruction is decoded from several machine states.

Take, as an example, state $2 / 5$ (output 5 of U16). Following the line across the schematic leads to instruction SCDP-L, set center frequency decimal point - assertive state low. The state $2 / 5$ low output from U16 is applied to inverter U4C and its high output causes TTC-H, T bus to center frequency register - assertive state high, to go high. The state $2 / 5$ output from U17 is also applied to AND gate U13B, the pin 12 input to NAND gate U2D goes low and KTT-H keyboard to T bus assertive state high, goes high.

The instruction SCDP-L occurs only in state $2 / 5$. However, some of the other instructions generated in state $2 / 5$ are also generated in other states.

Instruction TTC-H is also made to go high when NAND gate U23B pin 8 CTR-H goes high. This occurs when any one of the inputs to U23B goes low in states $1 / 15,1 / 14,2 / 0$ or $2 / 1$.

Instruction KTT-H also goes high when the pin 5 input to U13B goes low in state $1 / 4$. KTT-H goes high and JF3-L goes low when any of the inputs to AND gate U6A go low in states $1 / 13,1 / 12$ or $1 / 11$. Input pin 5 of U21B also causes JF3-L to go low in state $1 / 0$, but does not affect KTT-H.

Any of the instruction paths may be quickly checked by setting the instrument to the manual test mode and to the state to be checked. The machine state block in the algorithm indicates all instructions required in the set state.


Figure 8-72. P/O A1A5 ROM Output Assembly Component Locations (Part 2)



## SERVICE SHEET 29

## P/O REGISTER ASSEMBLY A1A6

A1A6 register assembly circuits are shown schematically on Service Sheets 29, 30 and 31 .

Service Sheet 29 shows the center frequency register and some clock control gating circuits.

The center frequency register, consisting of U9, U18, U28 and U38, is a ten digit recirculating shift register. U9 and U18 are dual 8 -bit registers with built-in multiplexers. U28 and U38 are single-digit four-bit registers; they store the least significant digits (U38 digit 1 and U28 digit 2). U9 stores BCD 1 and 2 data and U18 stores BCD 4 and 8 data.

When the instrument is first turned on PRDT-L is low, the $\overline{\mathrm{MR}}$ inputs to the registers are low and the register is held in the reset state until the power supply is stabilized.

When a new center frequency is entered on the keyboard and transferred to the T bus, it is not immediately entered into the center frequency register. It is, instead, first entered in the M register (SS31). If the M register and associated gates determine that the center frequency selected is within the output range of the RF Section installed, KTT-H and TTC-H both go high and the contents of the keyboard shift register is transferred to the center frequency register. If the center frequency entered is out of range it is rejected and the center frequency register retains the last valid entry.

When CTR-H goes high, the U33 NAND gates are enabled and the data stored in the center frequency register is clocked out to the $R$ bus. The data is also clocked back into the center frequency register for future use. While the data is being clocked out TTC-H is low so the $\mathrm{D}_{\mathrm{OB}}$ and DOA inputs of U7 and U16 are selected and the data recirculates.

The data stored in the center frequency register may also be transferred back to the T bus when desired. This occurs when CTT-H goes high.

The input lines labeled $\mathrm{KA}, \mathrm{KB}, \mathrm{KC}$ and KD are the inputs from the keyboard register. When these inputs carry data to be used in the plug-in sections,

ST01-L is low and is inverted by U40B to enable the U39 AND gates. NAND gate U19A is also enabled to provide a burst of ten clock pulses (PICK-L) to the appropriate plug-in register. This operation occurs in the remote mode of operation.

The clock pulses for the center frequency, step and sweep registers are provided by AND gate U8B. A train of ten clock pulses is provided when the following conditions exist:

1. The low CKB-H level is inverted and applied to pin 5 of AND gate U10B.
2. The low CK10-L level is inverted by U40E and applied to pin 4 of AND gate U10B.

## 3. The system clock is present at U10B pin 3 .

Input CK10-L initiates the clock burst when it goes low. The input CKB-H from the clock generator portion of A1A5 (SS27) goes high on the 10th clock and inhibits further output from U8B.

AND gate U10C provides a train of 10,12 or 13 clock pulses to drive the M register (SS31), when TTM-L at 31 B goes low. The CK10-L and CKB-H will enable and inhibit respectively a clock burst of ten pulses by their drive through U20A and U10A to U10C. The clock pulses are then coupled through U10C to the M register.

Three other clocks originate in the gating circuits shown on SS29. They are:

1. CK10CK-H used in the A1A3 readout control assembly, $\mathbf{1 0}$ clock pulses long.
2. ADDCK-H used in the A1A7 ALU assembly
and A1A3 readout control assembly, may be 10,12 or 13 clock pulses long.
3. AREGCK-H used in the A1A9 A register assembly, may be 10,12 or 13 clock pulses long.
These are similarly generated when enabled by CK1213-L, or CK10-L, or CK10J-L and inhibited by combined sequential operation of CKB-H and CKA-H. The latter two limit clock bursts to 10, 12 or 13 pulses.

The U15 NAND gates permit passage of BCD data from the keyboard SR to the A6U.


Figure 8-74. P/O A1A6 Register Assembly Component Locations (Part 1)


## SERVICE SHEET 30

## P/O REGISTER ASSEMBLY A1A6

A1A6 register assembly circuits are shown schematically on Service Sheets 29, 30 and 31 .

The sweep and step registers, which operate identically, are shown schematically on Service Sheet 30. The configuration of these registers is the same as the center frequency register shown on Service Sheet 29. They each consist of two dual 8 bit registers with built in multiplexers and two 4 bit registers.

When new data is to be entered into the sweep register the input labeled (SFDP, TTF)-L goes low and this level at U8 and U17 pins 4 and 13 (DS) selects the $\mathrm{D}_{0 \mathrm{~A}}$ and $\mathrm{D}_{0 \mathrm{~B}}$ inputs. A train of ten
clock pulses clock the sweep width information off the T bus into the sweep register where it is stored until called for.

When the data in the sweep register is to be clocked to the S bus, the train of ten clock pulses again appears at the CPC and CP inputs. During this cycle (SFDP, TTF)-L are high and the data from the register output is recirculated back into the register through the $\mathrm{D}_{1} \mathrm{~A}$ and $\mathrm{D}_{1 \mathrm{~B}}$ inputs to U6 and U15.

Operation of the step register is the same as operation of the sweep register except that the inputs are selected by (SIDP, TTI)-L.

PRDT-L at 29 (E) holds the registers in the reset when the instrument is first turned on until the mainframe power supplies are stabilized.

A1A6


Figure 8-76. P/O A1A6 Register Assembly Component Locations (Part 1)


## SERVICE SHEET 31

## P/O REGISTER ASSEMBLY A1A6

A1A6 register assembly circuits are shown schematically on Service Sheets 29, 30 and 31.

Service Sheet 31 shows the M register and the frequency limits detect gates.

The M register differs considerably from the other registers in the A1A6 assembly. U10 (BCD 1), U11 (BCD 2), U1 (BCD 4) and U2 (BCD 8) are all eight bit shift registers. Only six of the 8 bit locations are used ( 6 most significant digits). Data is clocked into the M register by a train of ten clock pulses, and digits $1,2,3$ and 4 are discarded. They are not needed because 10 kHz is the lowest detected frequency limit for any of the plug in RF Sections available.

All of the gates, except U13, to the right of the M register are used to detect and provide frequency limit information.

Two inputs, PILIM and 13GL, shown in the lower left corner of the schematic enable selected gates
that correspond to the limits of the RF Section in use.

The output of U31C, qualifier QA-H, signifying an above range frequency, is processed through A1A4 (ROM input assembly) and A1A5 (ROM output assembly) to a one-shot on the A1A1 switch control assembly. When QA-H goes high the (SIND1, JNINC)-H input to A1A1 goes high and causes the OUT OF RNG light to flash for about 1 second. The entered frequency will not be transferred to the center frequency register.

The output of U30B, SIND2 (lower frequency limit), is applied directly to A1A1 U14; it causes the OUT OF RNG light to light and remain lit. The instrument is capable of producing frequencies considerably lower than those specified as the lower frequency limit. However, the output level may be degraded.

The Code 1 and Code 2 outputs are used to change time constants in the RF Section plug in power amplifier to aid in output leveling.


Figure 8-78. P/O A1A6 Register Assembly Component Locations (Part 3)

P/0 AIAG REG ITTER ASSY 08660-60198 (M REG ITER AND LIMITS) -


## SERVICE SHEET 32

## ARITHMETIC LOGIC UNIT (ALU) A1A7

The ALU processes input data from the A, Center Frequency, Sweep Width and Step registers as well as data from ROM \#4 (U9) and associated circuitry.

U5 and U6 are four-bit full adders; they can accept two four-bit inputs and produce an output which is the binary sum of the inputs.
In a sense, U5 is the focal point of the ALU. It is here that the ALU inputs are initially combined.
U12 and U14 are complementers which may be operated in four different modes. The mode is selected by the dc levels on control inputs $B$ and $C$ as follows:

1. B and C both low - the $Y$ outputs are the complements of the A inputs - subtract function.
2. B is low and C is high (ADD-H is active) - the Y outputs follow the A inputs - add function.
3. B and C both high (XOR-H is active) - all Y outputs are low the $B$ inputs to U5 are processed through U5 without change.
4. B is high and C is low - all Y outputs are high. This mode is not used in the 8660B.
At the top center of the schematic are four three-input NAND gates (U18A, B, C and U3C). The inputs to these NAND gates are from the A, M, or CF registers. The output lines of the NAND gates are the R bus. The Y outputs of U12 are applied to the A inputs of ADDER U5.

The second input to ADDER U5 is from the S bus. The inputs to the $S$ bus are from the sweep width register via NAND gates U10A, B, C and D, the increment register via NAND gates U17A, B, C and D and ROM U9

In the arithmetic process the A and B inputs to ADDER U5 are summed and appear at the $\Sigma$ summation outputs in binary format. Whenever the U5 $\Sigma$ outputs are greater than 9 (1001) U6 adds 6 (0110) to the output of U5 to convert the binary sum to a BCD sum.
When ADD-H is high NAND gates U4B and U4C are enabled. U4B detects an output of 10 or 11 ( 1010 or 1011) at the output of U5. U4C detects an output of $12,13,14$ or 15 at the output of U5. U16D detects a carry, C4 from U5. A low output from any of these NAND gates will drive the output of NAND gate U4A high. With U6 inputs $\mathrm{B}_{2}$ and $\mathrm{B}_{3}$ high, U6 will add 6 (0110) to the inputs from U5.

In the subtraction process, the subtrahend is 1 's complemented added to the minuend, and the sum is 1 's complemented to get the difference. The binary sum is converted to BCD by adding 6

## SERVICE SHEET 32 (Cont'd)

(0110) whenever a carry (borrow) is generated. The $\mathrm{C}_{4}$ output is the carry from the fourth bit. Whenever there is a carry from U5C4, U16D output goes low, U4A output goes high and U6 again adds 6 to the U5 output. Note that U4B and U4C are again adds 6 to the U5 output. Note that U4B and U4C are
inhibited during the subtraction process because input ADD-H inhibite

In the subtraction operation XOR-H and ADD-H are both low so the B and C inputs of U12 and U14 are also low. The Y outputs of U12 and U14 are the complements of the A inputs.

Following are a few examples of binary addition and subtraction which may be helpful to the technician who has had little experience in the techniques involved.

| Add $75+38$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| BCD | 5 | 0101 |  |  |
| BCD | 8 | 1000 |  |  |
|  |  | 1101 | $>9$ | (13) |
|  |  | $\underline{0110}$ | + 6 |  |
|  |  |  | $=3$ | + carry |
| BCD |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  | add carry |
| BCD | 3 | 1000 | $=8$ |  |
|  |  | $\underline{0011}$ |  |  |
|  |  | 1011 | $>9$ | (11) |
|  |  | 0110 | + 6 |  |
|  |  | 0001 | = 1 | + carry |
| $=\mathrm{BCD} 000100010011=$ |  |  |  | DECIMAL |
| Add 456+82 |  |  |  |  |
| BCD | 6 | 0110 |  |  |
| BCD |  | 0010 |  |  |
|  |  | 1000 | $=8$ |  |
| BCD | 5 | 0101 |  |  |
| BCD |  | 1000 |  |  |
|  |  | 1101 | > 9 | (13) |
|  |  | 0110 | + 6 |  |
|  |  |  | $=3$ | + carry |
| BCD |  |  |  | add carry |
|  |  |  |  |  |
|  |  | 0101 | $=5$ |  |

$=$ BCD $010100111000=$ DECIMAL 538

## SERVICE SHEET 32 (Cont'd)

The subtraction process is really an addition process with numbers which have been complemented, summed, manipulated and again complemented to convert the binary sum to BCD .

Subtract 86 from 275

| BCD | 5 | $C_{1010}^{0101}$ |  | complement |
| :---: | :---: | :---: | :---: | :---: |
| BCD | 6 | $\underline{0110}$ |  |  |
|  |  | $\left\{\begin{array}{l} 0000 \\ \underline{0110} \end{array}\right.$ |  |  |
|  |  | $\begin{array}{r} 0110 \\ 1001 \\ \hline \end{array}$ |  | complement |
| BCD | 7 | $\begin{aligned} & 0111 \\ & 1000 \\ & 0001 \end{aligned}$ |  | complement <br> add carry (borrow) |
| BCD | 8 | $\begin{aligned} & 1001 \\ & 1000 \\ & \hline \end{aligned}$ |  |  |
|  |  | $\left\{\begin{array}{l} 0001 \\ 0110 \\ \hline \end{array}\right.$ |  | carry |
|  |  | $\underbrace{0111}_{1000}$ |  | complement |
| BCD | 2 | $\begin{array}{r} 0010 \\ 1101 \\ -0001 \end{array}$ |  | complement <br> add carry (borrow) |
|  |  | $\underbrace{1110}_{0001}$ | $=1$ | complement |
| $=\mathrm{BCD} 000110001001=$ |  |  |  | DECIMAL 189 |
| Subtract 45 from 92 |  |  |  |  |
| BCD | 2 | $C_{1101}^{0010}$ |  | complement |
| BCD | 5 | $\underline{0101}$ |  |  |
|  |  | $\begin{aligned} & 0010 \\ & 0110 \\ & \hline \end{aligned}$ | + 6 | carry |
|  |  | $\underbrace{1000}_{0111}$ |  | complement |
| BCD | 9 | $\begin{aligned} & 1001 \\ & 0110 \\ & 0001 \\ & \hline \end{aligned}$ |  | complement <br> add carry (borrow) |
|  | 4 | $\begin{aligned} & 0111 \\ & 0100 \\ & \hline \end{aligned}$ |  |  |
| BCD |  | $\int_{0100}^{1011}$ | $=4$ | complement |

$=$ BCD $01000111=$ DECIMAL 47

## SERVICE SHEET 32 (Cont'd)

Subtract 40 from 00036

| BCD | 6 | $\left(\begin{array}{l} 0110 \\ 1001 \end{array}\right.$ |  | complement |
| :---: | :---: | :---: | :---: | :---: |
| BCD | 0 | 0000 |  |  |
|  |  | $C_{1001}^{10110}$ | $=6$ | complement |
| BCD | 3 | $\underbrace{1100}_{0011}$ |  | complement |
| BCD | 4 | 0100 |  |  |
|  |  | $\left(\begin{array}{r}0000 \\ \frac{0110}{0110} \\ 1001\end{array}\right.$ | +6 $=9$ | carry complement |
| BCD | 0 | 0000 1111 $\underline{0001}$ |  | complement <br> add carry (borrow) |
|  |  | $\left(\begin{array}{r}0000 \\ \begin{array}{l}0110 \\ 0110 \\ 1001\end{array}\end{array}\right.$ | +6 $=9$ | carry complement |
| BCD | 0 | $\left[\begin{array}{l}0000 \\ 1111 \\ 0001 \\ \hline 0000\end{array}\right.$ |  | complement <br> add carry (borrow) |
|  |  | $\begin{array}{r} 0000 \\ \frac{0110}{0110} \\ 1001 \end{array}$ | $\begin{aligned} & +6 \\ & =9 \end{aligned}$ | carry complement |
| BCD | 0 | $\left(\begin{array}{l}0000 \\ 1111 \\ \mathbf{0 0 0 1} \\ \hline\end{array}\right.$ |  | complement <br> add carry (borrow) |
|  |  | $\begin{aligned} & 0000 \\ & 0110 \\ & \hline \end{aligned}$ | + 6 | carry |
|  |  | $\left(\begin{array}{l} 0110 \\ 1001 \end{array}\right.$ | $=9$ | complement |

$=$ BCD $10011001100110010110=$
DECIMAL 99996 + carry (borrow)
This subtraction result indicates a number less than zero. In the synthesizer it implies a negative frequency, which is impossible. In a following paragraph on ZER - FF, U19B, the impossibility is explained.
Shown in the lower right corner of the schematic are two $D$ type flip/flops, U19A and U19B. These flip/flops provide two qualifier outputs, QB-H and ZER-H. The QB flip/flop also provides the carry bit storage during add and subtract operations. The U19A D input is connected to the $\mathrm{C}_{4}$ (carry) outputs of both adders through OR gate U13D. If a clock pulse appears

## SERVICE SHEET 32 (Cont'd)

at a time when either carry is high, U19A $Q$ will go high. The QB-H output may change state several times during an operation to store the carry bit. The QB-H output logic sense is important only for the last clock in the operation. The clock train may last for 10,12 or 13 pulses depending on the operation being performed. When the D input to U19A is high at the time the last clock pulse is received, $\mathrm{QB}-\mathrm{H}$ goes high. It will stay high until the reset input, RQB-L is generated.

Flip/flop U19B retains the information occasionally generated during subtraction, that the difference number is effectively less than zero (minus). The ZER-H output will go high if the U19B D input is high during the last clock. Following this event a sequence of additions take place until the sum is no longer minus, and input RZER-L will enable the reset of U19B.
The 13 clock pulse train is used in the sweep mode when the 1000 step sweep is selected. It is possible to set the sweep width wide enough to go below 0 Hz (minus frequency). When this happens the sweep increment is repeatedly added to the A register content until the A register is 0 or + .

As an example, assume that the center frequency is 1 MHz and a sweep width of 4 MHz is entered. The sweep range is arithmetically -1 MHz to +3 MHz . Since the sweep starts initially at the center frequency, the sweep output is accurate until the frequency reaches 3 MHz . Then, when the sweep step count is reset to zero, the arithmetic circuit is calling for an output frequency of -1 MHz . Since this is impossible, it is necessary to add, for the example quoted, 4.000 kHz to the A register content 250 times ( $250 \mathrm{X} 4 \mathrm{kHz}=1 \mathrm{MHz}$ ), before there is an rf output and sweep is resumed. During the process of returning the A register content to zero or a + frequency, the sweep step clock is replaced with system clock to decrease dead time.

For the example quoted, 1 MHz center frequency, 4 MHz sweep width and 1000 step sweep the input from the A register is 13 digits long. The input from the sweep register is 10 digits long The arithmetic process is as follows:

> A register input to ALU
> Sweep input to ALU
> Next A register content
0001.000000000
0000004.000000
0000004.000000

It may be seen from the foregoing that the sweep width is effectively divided by 1000 , for the example quoted, by adding a ten digit sweep width to an extended 13 digit A register number. Each step adds 4.000 kHz to the A register.

## NOTE

See SS34 for details on the A register.

## SERVICE SHEET 32 (Cont'd)

After the adding process the information in the ten digit portion of the A register is 1.004000 MHz . This information is then clocked back through the ALU, without change, and returned to the $T$ bus and the output register for use in the mainframe RF circuits.

When it is desired to display the contents of the increment or sweep width register on the center frequency readout the data is passed through the ALU without change. This is accomplished by causing the XOR-H input to go high. When XOR-H is high, both the B and C inputs to U 12 are high so the Y outputs are held low. UTT-H is high so the data is coupled thorugh NAND gates U20A, B, C and D to the T bus.
Manual tune operation. ROM \#4, U9, provides the $B$ inputs to ADDER U5 when a manual tune or offset operation has been initiated.
When a manual tune operation is initiated, multiplexer U8 IS is high, so the $I_{1}$ inputs are selected. The $Z$ outputs follow the $I_{1}$ inputs (note that $I_{1} A$ is held high and I1D is held low). NAND gates U3A and U16B control the I1B and I1C inputs to multiplexer U8. The inputs to NAND gates U3A and U16A are:

1. TR $\emptyset$ is a function of the power detect circuit and selects coarse resolution mode $(1 \mathrm{MHz}$ steps).
2. TR1 is the coarse resolution mode ( 1 MHz steps). When it is active the $\mathrm{I}_{1} \mathrm{~B}$ input to multiplexer U8 is high.
3. TR2 is the medium resolution mode ( 1 kHz steps). When it is active the $\mathrm{I}_{1} \mathrm{C}$ input to multiplexer U8 is high.
4. TR3 is the fine resolution mode ( 1 Hz steps) When it is active, both the $\mathrm{I}_{1 \mathrm{~B}}$ and $\mathrm{I}_{1 \mathrm{C}}$ inputs to multiplexer U8 are high.

When a manual entry is made NTS-L goes low and the output of NAND gate U16C goes high to enable counter U2. The high output of U 16 C is inverted by U1E to enable the ROM, U9.

## SERVICE SHEET 32 (Cont'd)

at a time when either carry is high, U19A Q will go high. The QB-H output may change state several times during an operation to store the carry bit. The QB-H output logic sense is important only for the last clock in the operation. The clock train may last for 10,12 or 13 pulses depending on the operation being performed. When the D input to U19A is high at the time the last clock pulse is received, QB-H goes high. It will stay high until the reset input, RQB-L is generated.

Flip/flop U19B retains the information occasionally generated during subtraction, that the difference number is effectively less than zero (minus). The ZER-H output will go high if the U19B D input is high during the last clock. Following this event a sequence of additions take place until the sum is no longer minus, and input RZER-L will enable the reset of U19B.
The 13 clock pulse train is used in the sweep mode when the 1000 step sweep is selected. It is possible to set the sweep width wide enough to go below 0 Hz (minus frequency). When this happens the sweep increment is repeatedly added to the A register content until the A register is 0 or + .
As an example, assume that the center frequency is 1 MHz and a sweep width of 4 MHz is entered. The sweep range is arithmetically -1 MHz to +3 MHz . Since the sweep starts initially at the center frequency, the sweep output is accurate until the frequency reaches 3 MHz . Then, when the sweep step count is reset to zero, the arithmetic circuit is calling for an output frequency of -1 MHz . Since this is impossible, it is necessary to add, for the example quoted, 4.000 kHz to the A register content 250 times ( $250 \mathrm{X} 4 \mathrm{kHz}=1 \mathrm{MHz}$ ), before there is an rf output and sweep is resumed. During the process of returning the A register content to zero or a + frequency, the sweep step clock is replaced with system clock to decrease dead time.
For the example quoted, 1 MHz center frequency, 4 MHz sweep width and 1000 step sweep the input from the A register is 13 digits long. The input from the sweep register is 10 digits long. The arithmetic process is as follows:

| A register input to ALU | 0001.000000000 |
| :--- | :--- |
| Sweep input to ALU | 0000004.000000 |
| Next A register content | 0001.004000000 |

It may be seen from the foregoing that the sweep width is effectively divided by 1000 , for the example quoted, by adding a ten digit sweep width to an extended 13 digit A register number. Each step adds 4.000 kHz to the A register.

NOTE
See SS34 Yor details on the A register.

## SERVICE SHEET 32 (Cont'd)

After the adding process the information in the ten digit portion of the A register is 1.004000 MHz . This information is then clocked back through the ALU, without change, and returned to the T bus and the output register for use in the mainframe RF circuits.

When it is desired to display the contents of the increment or sweep width register on the center frequency readout the data is passed through the ALU without change. This is accomplished by causing the XOR-H input to go high. When XOR-H is high, both the B and C inputs to U12 are high so the Y outputs are held low. UTT-H is high so the data is coupled thorugh NAND gates U20A, B, C and D to the T bus.
Manual tune operation. ROM \#4, U9, provides the B inputs to ADDER U5 when a manual tune or offset operation has been initiated.

When a manual tune operation is initiated, multiplexer U8 IS is high, so the $\mathrm{I}_{1}$ inputs are selected. The Z outputs follow the $\mathrm{I}_{1}$ inputs (note that $\mathrm{I}_{1} \mathrm{~A}$ is held high and $\mathrm{I}_{1}$ D is held low). NAND gates U3A and U16B control the I 1 B and I1C inputs to multiplexer U8. The inputs to NAND gates U3A and U16A are:

1. TR $\emptyset$ is a function of the power detect circuit and selects coarse resolution mode ( 1 MHz steps).
2. TR1 is the coarse resolution mode ( 1 MHz steps). When it is active the $\mathrm{I}_{1 \mathrm{~B}}$ input to multiplexer U8 is high.
3. TR2 is the medium resolution mode ( 1 kHz steps). When it is active the $\mathrm{I}_{1} \mathrm{C}$ input to multiplexer U 8 is high.
4. TR3 is the fine resolution mode ( 1 Hz steps). When it is active, both the $\mathrm{I}_{1 \mathrm{~B}}$ and $\mathrm{I}_{1} \mathrm{C}$ inputs to multiplexer U8 are high.
When a manual entry is made NTS-L goes low and the output of NAND gate U16C goes high to enable counter U2. The high output of U16C is inverted by U1E to enable the ROM, U9.

When ADDCK-H goes high it enables AND gate U7B which couples the clock to counter U2. The Z outputs of U 8 and the Q outputs of U 2 select sequentially, 10 ROM addresses as the counter is clocked from 0 to a count of 9 . The data in the ROM ripples through NAND gates U11A, B, C and U3B to the B inputs of ADDER U5. Simultaneously, complimenter U12 applies the contents of the center frequency register to the A inputs of ADDER U5. The sum of the two inputs to U5 is then processed as previously described to provide a new center frequency incremented, or decremented, by the selected fine, medium or coarse step.

Offset is a special feature which allows the center frequency to be offset by fixed amount. This is accomplished when OTS-L is active. The select input to multiplexer U8 is low and the inputs labeled OPID 8-L, OPID 4-L, OPID 2-L and OPID 1-L are selected. The fixed code from these inputs address that part of the ROM where the offset number is stored. The Z outputs of U 8 are applied to the most significant ROM address bits. When AND gate U7D pin 11 goes low, NAND gate U16C pin 8 goes high to enable counter U2. The high at U16C pin 8 is inverted by U1E to enable U9. When ADDCK-H is active the clock is coupled through AND gate U7B to the CP input of counter U2. The data stored in the 10 ROM addresses is then coupled through U11A, B, C and U3B to the B inputs of ADDER U5 as the counter is clocked from $\emptyset$ to a count of 9 . Simultaneously, complimenter U12 applies the contents of the center frequency register into the A inputs of ADDER U5. The sum of the two inputs is then processed as previously described to provide a frequency offset by a fixed amount.

## NOTE

ROM \#4 (U9) must be set up at the factory before offset can be used. The offset amount may be either plus or minus when referenced to the center frequency.


Figure 8-80. A1A7 Arithmetic Logic Unit Component Locations

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## SERVICE SHEET 33

## SWEEP COUNT ASSEMBLY A1A8

The sweep count assembly performs two major functions. It keeps trace of the number of sweep steps which have occurred and it also provides a $\mathrm{D} / \mathrm{A}$ voltage output ( 0 to +8 V ) which is proportional to the sweep ramp.

The principle elements of the circuits are the presettable up/down counters U8, U10 and U5. The reason up/down counters are required is that in manual sweep mode the output frequency may be set up or down to any point within the sweep width range.

Note that the center frequency and the sweep frequency have no effect on the sweep count circuit. The counter tracks and counts the number of steps that have taken place on the sweep ramp. In the AUTO sweep and SINGLE sweep modes the count is always up. In the MANUAL sweep mode the count may be either up or down.

Since U8, U10 and U5 comprise a three digit counter, it is capable of reaching a count of 999. Essentially, the final count is 1000 because the input following 999 creates a carry at U5 pin 12 which causes flip/flop U3C/U3D to change state and cause QCTM-H (qualifier count maximum) to go high.

The count may be 1000 or 100 . When the count is 1000 all three up/down counters are used. When the count is $100, \mathrm{U} 8$ is bypassed.

When the count of 100 is selected Q100-H goes high to clear U8. U8 is held cleared as long as Q100-H is high. The Q100-H level enables NAND gates U2C and U2D. The Q100-H level is inverted by U13F and is used to inhibit NAND gates U2A and U2B which then enable NAND gates U3A and U3B. With the CDN output of NAND gate U6A connected to pin 13 of NAND gate U2D and the CUP output of NAND gate U6B connected to pin 10 of U2C, U8 is effectively bypassed and the terminal count will be 100 .

The $\overline{\mathrm{LD}}$ inputs to $\mathrm{U} 8, \mathrm{U} 10$ and U5 are preset inputs. When ILD-L (input load) goes low it is inverted by U7D to enable NAND gate U6C. The system clock then presets U8, U10 and U5. Since the $\mathrm{A}, \mathrm{B}, \mathrm{C}$ and D inputs of U 8 and U 10 are grounded, the outputs will be preset to zero.

Since the sweep operation starts initially at the center frequency, U5 must be preset to the center
of its range, a 5 . Note that the $\mathrm{D}_{\mathrm{B}}$ and $\mathrm{D}_{\mathrm{D}}$ inputs are grounded but the $\mathrm{D}_{\mathrm{A}}$ and $\mathrm{D}_{\mathrm{C}}$ inputs are high; the preset output of U5 is a 5 (0101).

When the selected sweep is 1000 steps the up/down counter is effectively preset to 500 ; it will take 500 CUP inputs for the count to reach maximum. All sweep ramps following the first will start at 000 and require 1000 steps to reach maximum.

When the selected sweep is 100 steps, U5 is preset to 5 , U10 is preset to zero and U8 is bypassed.

The CUP and CDN inputs to U8 (or U10 when 100 step sweep is selected) are coupled through NAND gates U6A and U6B. Operation of the gates is essentially the same except that input CND-L must be inverted because its assertive state is low.

## NOTE

The CDN-L and CUP-H inputs are in their assertive states for a period of 12 or 13 clock pulses. During this period the output of U6A or U6B is low. When the period ends the output of U6A or U6B goes high. This positive going excursion is the input to trigger U10 or U8.

At the bottom right of the schematic is the output QCTZ-H (qualifier count zero). This qualifier performs no useful function in the AUTO mode. In the manual sweep mode when manual sweep control is rotated CCW and the lower end of the sweep width range is reached, all of the outputs from U8, U10 and U5 are low and QCTZ goes high. Further rotation of the manual sweep control will not change the output frequency.

The digital-to-analog (D/A) output is a voltage proportional to the number of steps which have occurred during the sweep operation. U1 functions as a summing circuit; it sums the currents from 12 inverters and one transistor switch, Q1. It is important to note that the inverters are open collector inverters. When their inputs are high, the outputs are low and they provide a current which is proportional to their load resistors, to a common point. When the inverter inputs go low their outputs do not go high; they seek the voltage level at their common point. When QCTM-H (qualifier count maximum) goes high, Q1 is supplying all of the current to the summing circuit and the D/A output is +8 V .


Figure 8-82. A1A8 Sweep Count Assy Component Locations


## SERVICE SHEET 34

## A REGISTER ASSEMBLY A1A9

The major difference between the A register and other registers in the instrument is that it may be 10,12 or 13 digits long.

The 12 and 13 digit data is used in sweep operation. The 12 digit register is used when the sweep is to be 100 steps. The 13 digit register is used when the sweep is to be 1000 steps.

When the instrument is operated in the CW mode the final output to the mainframe through the ALU and the output register is from the ten-digit A register (U1, U2, U3 and U4). U1 and U2 are dual 8 -bit shift registers. U3 and U4 are four-bit registers. U3 and U4 are four-bit registers. The ten-digit register is a recirculating shift register when not in the sweep mode. The information in the ten-digit register is clocked to the ALU when ATR-H goes high to enable NAND gates U11A, B, C and D.

When a sweep operation is initiated for 100 steps, the register is lengthened to 12 digits by use of four-bit registers U5 and U6. The 12 -digit data is clocked to the ALU when A2TR-H goes high to enable NAND gates U12A, B, C and D.

When a sweep operation is initiated for 1000 steps, the register is lengthened to 13 digits by use of
four-bit register U7. The 13 digit data is clocked to the ALU when A3TR-H goes high to enable NAND gates U13A, B, C and D.

When the 12 or 13 digit data is clocked into the ALU and manipulated, it is clocked back into the A register via the T bus. In the AU'TO sweep mode the ALU normally adds one hundredth or one thousandth of the sweep width until QCTM-H goes high in the sweep count assembly.

## NOTE

It may be necessary for the technician to review the text for the sweep count assembly and the ALU to understand this operation.

Two of the three inputs to AND gates U10A, B, C and U9B are always high. The outputs are controlled by the selected NAND gates which precede them.

The gates shown in the lower left corner of the schematic control the clock inputs to the registers.

The instruction TTA-L or ATR-H enable the clock gate, U9A. The period of instruction AREGCK-H, determines whether 10,12 or 13 clock pulses will drive the combined registers. The instructions PDS-L inhibits clocking the three add-on registers U5, U6 and U7 at times during sweep when stored information is to be preserved.


Figure 8-84. A1A9 A Register Assembly Component Locations


## SERVICE SHEET 35

## OUTPUT REGISTER ASSEMBLY A1A10

The output register assembly contains the final DCU register. From this register the data goes to the mainframe RF loops through the A9 Cable Loop Assembly or the A3 Interface Assembly.

U4 through U8 function to provide serial to parallel data storage. Each of them are dual four-bit latches. One of the characteristics of this type of latch is that the $Q$ outputs follow the $D$ inputs when the latch is enabled. These latches are not clocked directly by the system clock; they are enabled by a combination of the output of one-of-ten selector U1, the system clock and the PD-H input. This type of register is commonly termed a parallel dump register.

A parallel dump register has a distinct advantage over serial dump registers, in that only the BCD bits that require change, are changed. In serial dump registers, all of the RF phase lock loops lose lock each time the frequency is changed, even if the frequency change is as low as 1 Hz . The result of losing lock in all of the RF loops is longer
switching time and temporary generation of many undesired frequencies. These problems are particularly troublesome in the sweep mode of operation.

Assume that the RF output has been 1.000000 MHz and is changed to 1.100000 MHz . The Q0A output (binary 1 of digit 6) of U8 goes high and all other outputs remain unchanged.

U1, a one-of-ten selector, enables the gates in the dual four-bit latches sequentially. They are enabled at a point in time when the data of the $T$ bus applies only to their output digit number (D1 through D10). All outputs are high except the one selected. The sequential BCD inputs on CNT 1, 2 , 4 and 8 originates in a counter U17 on the A1A5 assembly (see Service Sheet 27).

All of the enable latch gates are connected to the output of NAND gate U3D. One of the inputs to U3D is PD-H which is high in the assertive state. The other input is derived from the system clock. This second input to U3D is delayed approximately 0.1 microsecond to ensure that the latches are not enabled while a change is taking place on the T bus.


Figure 8-86. A1A10 Output Register Component Locations


## SERVICE SHEET 36

## NUMERIC READOUT ASSEMBLY A1A2

The numeric readout assembly consists of two readout units, U3 and U4, and the circuits required to drive them. U4 displays the least significant digits, 1 through 6 . U3 displays the 4 most significant digits, $7,8,9$ and 10 . The most significant digit, digit 10 , is always a 1,2 or 0 . U3 is also a six-digit display, but only the four least significant digits are displayed.

The readout display creates the illusion that the LEDs (light emitting diodes) are lit continuously. They are actually scanned at a 10 kHz rate and therefore each half digit is illuminated for 100 microseconds for each scan cycle.

Referring to Figure $8-88$ it may be seen that each digit is made up of 20 LEDs that are divided into two 10 LED half digits. During the scanning cycle the half digits are scanned, first right half, then left half. The LEDs require approximately 50 milliamperes each so the transistor drivers are heavy duty types capable of delivering about 400 milliamperes each.

Referring back to the schematic it is readily seen that one-of-twelve selector U5, the transistor drivers and ROMs U1 and U2 jointly control the readout.

It is important to understand the relationship of the ROCK ( 10 kHz ), RSCAN-H and ROM (read only memory) inputs.

The 10 kHz ROCK input clocks U5 only during the time that RSCAN-H is low, i.e., when not in reset. RSCAN-H stays low for the period of six clock pulses at a 5 kHz rate. The 5 kHz clock drives the ten-digit register on the A1A3 assembly, Service Sheet 24, during the period of time that the readout is being displayed. The BCD inputs to ROMs A and B are BCD data which is clocked in at a 5 kHz rate.

It may be seen from the foregoing that U5 provides two outputs to the transistor drivers for each BCD input to the ROMs. U5 also provides an R/L (right/left) output which is used as the fifth address bit to the ROMs. This R/L output determines, in conjunction with the other ROM inputs, which LEDs of the half digit being displayed are illuminated.

As the scanning cycle starts U5 output OR (output 0, right half) turns on Q20 and Q8 to apply about +4 volts to the right hand half of digits 1 and 7. Simultaneously the R/L output of U5 provides the fifth address bit to ROMs A and B. ROMs A and B then provide ground returns for the LEDs which are to be illuminated in the right half of digits 1 and 7 . When U5 output OL goes high Q19 and Q7 drive the left half of digits 1 and 7 . The R/L output of U5 again provides the fifth address bit to ROMs A and B which then provide the ground returns to light the appropriate LEDs in the left half of digits 1 and 7. Next, digits 2 and 8 , then digits 3 and 9 , then digits 4 and 10 , and finally digits 5 and 6 are scanned in order.

It can be seen that the scanning cycle has effectively scanned 10 digits with 12 inputs clocks at a 10 kHz rate. At this point in time RSCAN-H goes high to reset U5.

## SERVICE SHEET 36 (Cont'd)

In the A1A3 assembly the ten digit recirculating register contains a sync register. At the end of the readout scan cycle, four more clock pulses are required to re-position the data in the register before the data can again be used in the readout scanning cycle. During the readout scanning cycle the recirculating register is clocked at a 5 kHz rate. If this rate were continued, it would be 800 microseconds before the next readout scanning could start. However, a detect circuit driven from the sync register detects the sync code at the sixth 5 kHz clock and switches to the system clock of 1 MHz for the next four clock pulses. Using this system assures that there are only four microseconds between readout scan cycles. See Service Sheet 24 for expanded details of this operation.

All controls for the numeric readout, except for the 10 kHz ROCK, originate in the A1A3 Readout Control Assembly.

The assembly also has the drive circuits for the four incandescent lamps, which display $\mathrm{GHz}, \mathrm{MHz}, \mathrm{kHz}$ and Hz units.

The pushbuttons select SWP WIDTH, STEP and KYBD readout instructions for the A1A1 Switch Control Assembly.

## SERVICE SHEET 36 (Cont'd)

In the A1A3 assembly the ten digit recirculating register contains a sync register. At the end of the readout scan cycle, four more clock pulses are required to re-position the data in the register before the data can again be used in the readout scanning cycle. During the readout scanning cycle the recirculating register is clocked at a 5 kHz rate. If this rate were continued, it would be 800 microseconds before the next readout scanning could start. However, a detect circuit driven from the sync register detects the sync code at the sixth 5 kHz clock and switches to the system clock of 1 MHz for the next four clock pulses. Using this system assures that there are only four microseconds between readout scan cycles. See Service Sheet 24 for expanded details of this operation.

All controls for the numeric readout, except for the 10 kHz ROCK, originate in the A1A3 Readout Control Assembly.

The assembly also has the drive circuits for the four incandescent lamps, which display $\mathrm{GHz}, \mathrm{MHz}, \mathrm{kHz}$ and Hz units.

The pushbuttons select SWP WIDTH, STEP and KYBD readout instructions for the A1A1 Switch Control Assembly.


A1A12
FRONT VIEW


A1LI

## REAR VIEW



A1L1

Figure 8-89. A1A12 Numeric Readout Assembly Component Locations


Figure 8-90. A1A12 Numeric Readout Assy

## SERVICE SHEET 37

## FRONT INTERFACE CIRCUIT BOARD

Normally, causes of malfunctions in the Model 8660C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.

When the defect has been traced to the front interface board, access to the component side of the circuit board may be improved by removing the four screws which hold the digital control unit in place and sliding it forward to the extent of the interconnecting cables

## TEST EQUIPMENT REQUIRED (See Table 1-3)

Oscilloscope (with 10:1 divider probes)
Digital Voltmeter

## GENERAL

The major purpose of the interface circuits is to assure compatability between the digital control unit, the phase lock loops, the plug-in section and the programming information from the remote programming device (vi J3).

## FRONT INTERFACE CIRCUIT - REMOTE MODE

## DATA INPUT

The multiplexer, U9 and U10, converts the eight-line two-digit parallel BCD input to four-line serial information. The serial BCD data is stored in the temporary storage register in the digital control unit

When a command pulse is received at A3XA1 pin 1 it is inverted by U1F and applied to the "D" input of flip/flop U2A. Pin 1 of U2A is held high by the inverted low AUTO-MAN input at A3XA1 pin B so U2A is enabled. (A low at U2A pin 1 would hold the Q output high regardless of other inputs).

The 2 MHz clock, which is always present is inverted and applied to the clock input of U2A. Since the inverted command pulse is high the first clock pulse to U2A will cause the $Q$ output to go high. The $Q$ output enables the upper AND gates in U10A, U10B, U9A and U9B. The outputs of the multiplexer follow the selected inputs (in this case, digit 1). Several other circuits function simultaneously with this change of state to determin where and how the input will be used.

If the BCD inputs are data (BCD 0-9), the output of NAND gate U3A is high because at least one of the inputs is low. U1D inverts the output of U3A to inhibit U4D which is the permanent command gate. The high output of U3A enables U4C which is the temporary command gate.

When U2A $\bar{Q}$ output goes low with the clock pulse it presets U2B; U2B Q goes high and $\bar{Q}$ goes low. The low at U2B $\bar{Q}$ resets the one-shot (U1A and U1B) on the rear interface board to end the command pulse. This assures that the command pulse will end and the "D" input to U2A will go low before the next clock pulse appears.

## SERVICE SHEET 37 (Cont'd)

When U2B $Q$ goes high it enables NAND gate U4A. NAND gate U4A provides a negative-going clock pulse to NOR gate U6A which provides, in turn, a positive pulse to NAND gate U4C. Since NAND gate U4C pin 9 is held high by the output of NAND gate U3A, the output of NAND gate U4C clocks the digit 1 BCD information into the temporary storage register

When the next clock pulse appears the "D" input to U2A is low. The Q output goes low and the $\bar{Q}$ output goes high. The lower AND gates in U10A, U10B, U9A and U9B are now enabled and the upper AND gates are inhibited. The multiplexer outputs are the same as the digit 2 inputs.

When U2A Q goes low the output of NOR gate U6B goes high to enable NAND gate U4B. Since the $Q$ output of U2B is still high when the second clock pulse appears this clock is coupled through U4A, U6A and U4C to clock digit 2 into the temporary storage unit in the digital control unit.

Since NAND gate U4B pin 5 is now held high by NOR gate U6B the clock pulse at U4B pin 4 causes the output of U4B to go low and clear flip/flop U2B. When U2B is cleared the $Q$ output goes low to inhibit U4A, the $\frac{P}{Q}$ output goes high to enable the command one-shot on the rear interface board, and the circuit is quiescent until the next command pulse is received.

## ADDRESS INPUT

When all four digit 1 lines are high (BCD 15), NAND gate U3A output is low. This low level inhibits the temporary command gate U4C; through inverter U1D it also enables the permanent (transfer) command gate U4D. When the input command pulse appears (U2A "D" input goes low), the first clock pulse will cause U2A $Q$ to go high and $\bar{Q}$ to go low. The high $Q$ output causes the output of NAND gate U4D to go low.

The digit 2 inputs have been simultaneously applied to BCD to decimal decoder U5. When the digit 2 address is 0000 (center frequency) pin 1 of U5 goes low to address the information stored in the temporary storage register to the center frequency register.

The outputs from U5 pins 2 and 3 are not used in the Model 8660A
When the digit 2 address data causes U5 to produce a low to the input of one of the NOR gates connected to the U5 outputs, a train of ten clock pulses transfer the data stored in the temporary storage register to the selected final register.

The outputs from the multiplexer are not used during the address function.
Operation of U2B is the same during the address function as it is during the data function

When the next clock pulse appears the state of U2A and U2B will change and the circuit is quiescent until the next command pulse appears.

SERVICE SHEET 37 (Cont'd) POWER DETECT CIRCUIT

Q3 and U7D comprise a power detect circuit. The pin 11 input to NOR gate U7D is low unless the reset input to Q 4 is grounded. When the +5 V power supply is below about +4.75 volts Q3 is turned off, the pin 12 input to NOR gate U7D is high, and the output from U7D is low. When the PWR DET output is low the center frequency register and the modulation register are cleared. This prevents incorrect programming when the instrument is first turned on before the power upplies have stabilized. When a ground is applied upplies have stabilized. When a ground is applied the remote reset line Q4 is turned off, pin 11 of NOR gate U7D goes high and the U7D output goes ow. The result is the same as when the +5 V power supply is low.

## FLAG CIRCUIT

The flag circuit provides a busy signal to the remote programming device. Whenever any one or more of the inputs to U3B are low the output is high. This output is inverted on the rear interface board and applied to rear panel connector J3 pin 17.

There are several factors which determine the duration of the flag signal.

When data is being programmed into the temporary storage register in the digital control unit the duration of the flag signal is a maximum of about 1.5 microseconds. It starts when the command pulse causes U3B pin 12 to go low. U2B $\bar{Q}$ almost immediately goes low to end the command pulse. The command line now goes high, but U2B $\overline{\mathrm{Q}}$ is now holding U3B pin 13 low so the flag pulse

## SERVICE SHEET 37 (Cont'd)

When U2B $Q$ goes high it enables NAND gate U4A. NAND gate U4A provides a negative-going clock pulse to NOR gate U6A which provides, in turn, a positive pulse to NAND gate U4C. Since NAND gate U4C pin 9 is held high by the output of NAND gate U3A, the output of NAND gate U4C clocks the digit 1 BCD information into the temporary storage register.

When the next clock pulse appears the " $D$ " input to U2A is low. The Q output goes low and the $\bar{Q}$ output goes high. The lower AND gates in U10A, U10B, U9A and U9B are now enabled and the upper AND gates are inhibited. The multiplexer outputs are the same as the digit 2 inputs.

When U2A Q goes low the output of NOR gate U6B goes high to enable NAND gate U4B. Since the Q output of U2B is still high when the second clock pulse appears this clock is coupled through U4A, U6A and U4C to clock digit 2 into the temporary storage unit in the digital control unit.

Since NAND gate U4B pin 5 is now held high by NOR gate U6B the clock pulse at U4B pin 4 causes the output of U4B to go low and clear flip/flop U2B. When U2B is cleared the Q output goes low to inhibit U4A, the Q output goes high to enable the command one-shot on the rear interface board, and the circuit is quiescent until the next command pulse is received.

## ADDRESS INPUT

When all four digit 1 lines are high (BCD 15), NAND gate U3A output is low. This low level inhibits the temporary command gate U4C; through inverter U1D it also enables the permanent (transfer) command gate U4D. When the input command pulse appears (U2A "D" input goes low), the first clock pulse will cause U2A $Q$ to go high and $Q$ to go low. The high $Q$ output causes the output of NAND gate U4D to go low.

The digit 2 inputs have been simultaneously applied to BCD to decimal decoder U5. When the digit 2 address is 0000 (center frequency) pin 1 of U5 goes low to address the information stored in the temporary storage register to the center frequency register.

The outputs from U5 pins 2 and 3 are not used in the Model 8660A.
When the digit 2 address data causes $U 5$ to produce a low to the input of one of the NOR gates connected to the U5 outputs, a train of ten clock pulses transfer the data stored in the temporary storage register to the selected final register.

The outputs from the multiplexer are not used during the address function.
Operation of U2B is the same during the address function as it is during the data function.

When the next clock pulse appears the state of U2A and U2B will change and the circuit is quiescent until the next command pulse appears.

## SERVICE SHEET 37 (Cont'd)

## POWER DETECT CIRCUIT

Q3 and U7D comprise a power detect circuit. The pin 11 input to NOR gate U7D is low unless the reset input to Q4 is grounded. When the +5 V power supply is below about +4.75 volts Q3 is turned off, the pin 12 input to NOR gate U7D is high, and the output from U7D is low. When the PWR DET output is low the center frequency register and the modulation register are cleared. This prevents incorrect programming when the instrument is first turned on before the power supplies have stabilized. When a ground is applied to the remote reset line Q4 is turned off, pin 11 of NOR gate U7D goes high and the U7D output goes low. The result is the same as when the +5 V power supply is low.

## FLAG CIRCUIT

The flag circuit provides a busy signal to the remote programming device. Whenever any one or more of the inputs to U3B are low the output is high. This output is inverted on the rear interface board and applied to rear panel connector J3 pin 17.

There are several factors which determine the duration of the flag signal.

When data is being programmed into the temporary storage register in the digital control unit the duration of the flag signal is a maximum of about 1.5 microseconds. It starts when the command pulse causes U3B pin 12 to go low. U2B Q almost immediately goes low to end the command pulse. The command line now goes high, but U2B $\overline{\mathrm{Q}}$ is now holding U3B pin 13 low so the flag pulse
continues. When the second clock pulse causes U2B to be cleared, U2B $\bar{Q}$ goes high and the flag pulse is ended. One/shot U8 cannot be triggered because the high output of U3A is inverted and applied to pins 3 and 4 of U8.

When the plug-in programmable attenuator in the RF Section plug-in is being addressed one-shot U8 is triggered when U2B $\bar{Q}$ goes low on the second clock pulse (U8 pins 3 and 4 are now held high by the inverted low at U3A pin 6). One-shot U8 pin 6 goes low and the flag signal is extended to about 50 milliseconds. The low output from U5 pin 4 turns off Q2 and the Q2 high output turns off Q1. The time constant of one-shot U8 is determined by R10, C5 and C6.

When any address other than the programmable attenuator is programmed, one-shot U8 extends the flag signal to about 3 or 4 milliseconds. Operation of the circuit is the same as when the attenuator is addressed except that Q1 and Q2 are on and the time constant of the one-shot is determined by R9 and C6.

When the FM modulator is being calibrated a 5 second pulse appears at A3XA3 pin 15 which is applied to U3B pin 9 to produce an output pulse that is 5 seconds in duration.

## LOCAL MODE

In the local mode the AUTO-MAN input is high. Inverter U1C inverts this level to hold the clear input to U2A low and the Q output high. This inhibits all of the circuits on the front interface board except U1C, U1A and U1B. U1A and U1B again invert the AUTO-MAN input to provide a LCL-RMT fan-out of ten to the plug-ins and the digital control unit.


Figure 8-91. Interface Mother Board


Figure 8-92. A3A1 Front Interface Board Component Locations


## SERVICE SHEET 38

## REAR INTERFACE CIRCUIT BOARD

Normally, causes of malfunctions in the Model 8660 C will be isolated to a circuit board or assembly as a result of performing the tests specified in the troubleshooting trees.
When trouble has been traced to the rear interface circuit board it will be necessary to swing the A4 assembly out of the frame to provide access to the wiring side of the circuit board.

## TEST EQUIPMENT REQUIRED (See Table 1-2)

Oscilloscope (with 10:1 divider probes)
Digital Voltmeter

## GENERAL

The major purpose of the interface circuits is to assure compatability between the digital control unit, the phase lock loops, the plug-in sections and the programming information from the remote programming device (via J3).

## REAR INTERFACE CIRCUIT

The BCD inputs from the remote input (J3) are applied to the "D" inputs of two quad latch flip/flops (U2 and U4). When a negative-going command pulse appears at the input to U3A the outputs of U1D and U1C clock U2 and U4.

Since the $\overline{\mathrm{Q}}$ outputs of U2 and U4 provide the front interface drive signals the negative-true input BCD data (low $=1$, high $=0$ ) is inverted. This data is stored in U2 and U4 until the next command pulse.
NAND gates U1A and U1B comprise a one-shot with a maximum time constant of 0.75 microsecond. Normally NAND gate U1B pin 6 is high because R21 is holding pin 4 of U1B low and pin 1 of NAND gate U1A is held high by the command line. Pin 5 of NAND gate U1B is normally held high by the $\bar{Q}$ output of the flip/flop U2B on the front interface board. When a negative-going command pulse appears the output of NAND gate U1A at pin 3 goes high and is coupled through C4 to cause the output (pin 6) of NAND gate U1B to go low. The time constant of C4/R21 limits the negative-going pulse to a maximum duration of 0.75 microseconds to allow adequate time for a flip/flop in the front interface circuit to be clocked once by the 2 MHz clock ( 0.5 microsecond time base). To assure that two or more clock pulses do not appear in the front interface circuit while the command pulse is present, the inputs to NAND gate U1B pin 5 is caused to go low (output, pin 6 goes high) when the first clock pulse is received in the front interface circuit.

Q1, Q2 and NAND gate U3D comprise an error detect circuit. The input to NAND gate U3D pin 12 is from the reference oscillator (A21) assembly. When the oven temperature has not stabilized this level will be low. When either input to U3D is low the output will be high, Q1 will be turned on, and an error signal (low) be applied to J3 pin 3 to inform the remote

## SERVICE SHEET 38 (Cont'd)

programming device that the Model 8660 C is not ready to receive data. The input to pin 12 of NAND gate U3D is also applied to the digital control unit to light a lamp on the annunciator block when the oven temperature has not stabilized.

The input to pin 13 of U3D is from one of two sources. The F LIM input from A3XA4 pin 11 originates in the digital control unit center frequency circuit and is a low when the selected output frequency is not within the range of the RF Section in use. The second input to control NAND gate U3D pin 13 is the "GHz" input at A3XA5 pin D. This input is a high when selected frequency is not within the range of the 1.3 GHz RF Section or the internal Frequency Extension Module. A high input to the base of Q2 will cause Q2 to turn on the output of NAND gate U3D will again go high to turn on Q1.

NAND gate U3C inverts the FLAG signal, which is generated in the front interface circuit, and applies it to J 3 pin 17 as a busy signal to the remote programming device.

R25 and R29 hold the AUTO line (A3XA5 pin 5) high when the instrument is operated in the local mode. When J3 pin 5 is grounded by the remote programming device, this line goes low and the instrument is in the remote mode.

R26 and R30 hold the RESET line (A3XA5 pin J) high when no error is present in the remote programming device. When an error is present J3 pin 24 goes low and causes the PWR DET circuit on the front interface board to clear the center frequency storage register and shut off the modulation.

## A3A2

To A3XA4 on A3 Mother Board


To A3XA5

Figure 8-94. A3A2 Rear Interface Board Component Locations


Figure 8-95. A3A 2 Rear Interface Board Schematic

## SERVICE SHEET 39

## HP-IB INPUT ASSEMBLY A3A2 (08660-60192)

## General

Basically the HP-IB input assembly accepts the data from the bus, detects the programming action taking place and provides outputs that determine the operational parameters for the Model 8660.

## Voltage Dividers (U8, U14) and Schmitt Triggers (U7, U13)

U8 and U14 are resistive arrays which contain eight two-resistor voltage dividers each. Each voltage divider consists of (typical values) 3000 ohms to +5 V and 6200 ohms to ground. These dividers bias the input lines to about +3 V when the lines are not being driven by data. These dividers are used to keep the load on the bus, which is wire ANDed to all instruments, constant. Note that the lines which are not used in the Model 8660 (DI 08, E01-L and SRQ-L) are also terminated in loads to preserve the constant loading of the HP-IB bus.

The HP-IB input lines are negative true logic. These lines are high in the quiescent state and are pulled low in the assertive state ( $0 \mathrm{~V}=\mathrm{H}$ ). One of the reasons for using negative true logic is that TTL "sees" an open circuit as a high. If positive true logic were used, a discontinuity or a disconnected connector would simulate a high and the inputs lines would see this as the assertive state.

U7 and U13 are Schmitt Triggers. These Schmitt Triggers improve the quality of the data inputs, provide buffering and invert the input logic levels. Buffering is required to limit the load on the controller to one standard load (approx. 1.6 milliamperes sink current) for each controlled instrument. Following the data lines it may be seen that they are again inverted to negative true logic. Again, the data bits cannot be directly used from the inputs lines because of excessive loading.

## Address Decoder U12

One of the characteristics of a NAND gate is that all of the inputs must be high in order for the output to be low. Therefore, all of the inputs to U12 must be high before the output MLA-L (My Local Address-Low) can be in the assertive state. As may be seen by evaluating the circuits which provide the inputs to U12, only one set of input data bits will cause the output of U12 (MLA-L) to go to the assertive state. For the Model 8660 this is an HP-IB characters 3 .

If more than one Model 8660 is used in the system, each additional 8660 's would require a different address. This involves a different set of address bits from the controller and changing the address jumpers to accept the new HP-IB character.

## SERVICE SHEET 39 (Cont'd)

## Remote Flip/Flop U9A

When the REN (Remote Enable) input line goes low the input is inverted by Schmitt Trigger U13A and applied to the "D" input of U9A.

U9A, however, cannot change state until it is clocked by a combination of MLA-L, DAC-H, DAV-L and MRE-L. This is because it is desired to keep the Model 8660 in the local mode until it is addressed by the bus. U9A is clocked as follows:

1. When MLA-L goes low it is inverted by U11F and applied to one input of AND gate U10D.
2. The second input to AND gate U10D is the inverted DAC-H output of NAND gate U2B which is low until the data is accepted.
3. The high output of AND gate U10D is applied to one input of AND gate U10B. The second input to U10B is from AND gate U10A.
4. The inputs to AND gate U10A are the inverted MRE-L (Multiple Response Enable) and the inverted DAV-L (Data Valid) inputs.
5. MRE is an address function so it goes low first.
6. Finally, DAV goes low, is inverted and applied to the clock input of U9A. It is the negative-going DAV signal which supplies the positive-going pulse to clock U9A.

When MLA-L is low and U9A is clocked the U9A Q output goes high and the $\overline{\mathrm{Q}}$ output goes low.

Note that the $\bar{Q}$ output of U9A is labeled LCL-H When the LCL line goes low the Model 8660 goes to the remote mode and the front panel controls (except for STBY/ON) are inhibited.

## Address Flip/Flop U9B

When MLA-L goes low it is also used to set the "D" input to U9B high. This is accomplished as follows: the pin 10 input of U3C is high, and until an "unlisten" command appears, so is the pin 9 input. The high output of U3C enables the "D" input of U9B.

U9B is clocked in the same manner as U9A, by a combination of MRE and DAV.

The $Q$ output of U9B is applied to one input of AND gate U3A. The second input to U3A is MRE, which is now in the quiescent state (high), so the output of U3A (ADR-H) is also high.

## Unlisten Gate U5

When all of the inputs to U 5 go high the address flip/flop is reset and the incoming data has no effect on the Model 8660.

## DCR-L Gate U4 (Device Clear)

When all of the inputs to U4 go high the output goes low. The low output has the same effect on the Model 8660 as the power detect circuit. The instrument is initialized with frequency (8660C) and attenuation set to predetermined values.

The remaining gates and inverters are conventional and should pose no problem to the average technician.

Model 8660C


Figure 8-96. A3A2 Component Locations

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## SERVICE SHEET 40

## HP-IB OUTPUT ASSEMBLY A3A1 (08660-60188)

## General

The HP-IB Output Board accepts inputs from the HP-IB Input Board, the DCU and the mainframe and converts these inputs to data which is used to program the mainframe, the plug-in sections and the HP-IB Input assembly.

## Four-State Macine U7A/B

Located at the lower left side of Service Sheet 2 is a schematic representation of the four-state machine designated as U7A and U7B. Located outside of the schematic image area is an algorithmic state machine graph (ASM or flow chart) which graphically illustrates the operation of flip/flops U7A and U7B.

Each of the four states of the ASM are labeled at the upper right hand corner with the machine state ( $11,10,00$ and 01 ). Each of the states refer to the state of the $Q$ outputs of the flip/flops with the 1 representing a high. For example, the top box, labeled state 11, indicates that the Q outputs of both U7A and U7B are high. Note that in each case the first digit is for U7B and the second digit is for U7A.

Initially, with U7A/B in the quiescent state (state 11), the flip/flops are ready for DAV (Data Valid) to go low signifying that there is a data input. When DAV goes low it is inverted by U10E and applied to AND gate U1A. The other input to U1A is held high at this time by U7B $Q$, so the $K$ input of U7A goes high.

The next clock pulse causes U7A to change state; Q goes low and $\overline{\mathrm{Q}}$ goes high and the ASM proceeds to state 10 . In state 10 the incoming data is stored in U2 and the RFD state remains active.

Since there is no qualifier following state 10 , the next clock pulse moves the ASM to state 00 . In state 00 the command pulse to transfer the data is generated.

Like state 10 , there is no qualifier following state 00 , so the next clock pulse moves the ASM to state 01, which is the DAC (Data Accepted) state.

Following state 01 is qualifier DAV-H and BUSY-L. When the output of qualifier DAV-H and BUSY-L is low, the ASM is held in state 01 . When the qualifier output goes high the ASM (and the flip/flops), return to state 11 and are ready for the next data input.

Flip/flops U7A/B control the three-wire handshake procedure within the instrument.

Jumper J1, when in place, is used to couple the internally generated BUSY signal to delay the RFD response. Without J1 the operator must make allowances in programmingafor the necessary settling time delays of the Model 8660.

## SERVICE SHEET 40 (Cont'd)

## Delay One Shot U6

U6, in conjunction with Q1 and associated components, comprise a delay circuit which inhibits the start of the RFD period when certain programming steps are initiated. This is required because the programming time required for different functions varies.

As an example of circuit operation assume that a change in frequency is programmed. Q1 is turned on and R1 and C2 determine the 5 millisecond operating time of the one-shot. One-shot output is from pin 4 to U1 and pin 12.

When an attenuation function is programmed, Q1 is turned off and R2, C1 and C2 determine the 50 millisecond operating time of the one-shot.

There is also a 5 second delay built into the Mode 8660 DCU for use in the FM CAL operation. The HP-IB interface utilizes this signal to delay RFD for 5 seconds when FM CAL is programmed. This delay input is the FLAG-L (BUSY) signal.

## Shift Register U2

U2 is a conventional 4-bit shift register which is operated in the preset mode. U2 functions as a temporary storage register.

When the inputs to U 2 are data the U 2 outputs are directly applied to the DCU.

When the inputs to U2 are an address, ENSL-H (Enable Select) goes high to enable the U3 NAND gates and the address data is coupled to one-of-ten selector U4. When the U2 register is processing an address, the clock input, CP , at pin 10 is inhibited for 100 microseconds by one-shot U6 pin 12 output. This prevents controller change of address until after sufficient time has passed for the Model 8660C state machine process. Jumper J2 may be installed to disable this operation for a Model 8660A.

## One-of-Ten Selector U4

U4 determines which programming function (address) has been selected, and, in conjunction with PICK-L (Plug-in Clock) couples the address data to the appropriate register.

## Power Detect Circuit

Q2 and associated components comprise a power detect circuit which inhibits circuit operation on initial turn-on until the power supply has reached a stable condition. Initialization follows removal of the low level pulse, setting frequency to 1 MHz ( 8660 C ) and attenuation to -140 dB .


Figure 8-98. Opt 005 A3A1 Component Locations


Figure 8-99. HP-IB Output Assembly, Schematic


Figure 8-100. A6 Assembly Open View


Figure 8.101. A6A1 Assy Component Locations Front View


Figure 8-102. A6A1 Assy Component Locations Rear View HP-IB Output Assembly, Schematic SERVICE SHEET 40


Figure 8-101. A6A1 Assy Component Locations Front View
A6A1 REAR VIEW


Figure 8-102. A6A1 Assy Component Locations Rear View HP-IB Output Assembly, Schematic
SERVICE SHEET 40


Figure 8-104. A20 Top and Bottom Component Locations



Model 8660C


Figure 8-106. A1A2 Annunciator Assembly and Schematic

Figure 8-107. DCU and Interface Wiring Diagram





Figure 8-112. Mainframe Mother Board Test Points (1 of 2)

| Test Points | Assemblies | Mother Board Inputs and Outputs |
| :---: | :---: | :---: |
| (27) TP1 N3 Oscillator <br> (30 TP2 N3 10 kHz <br> (29) TP3 N3 Phase Error <br> (28) TP4 N3 Phase Error Grounding <br> (24) TP5 SL2 Tuning <br> (25) TP6 SL2 Oscillator <br> (26) TP7 SL2 Pulse Phase Error <br> (20) TP8 SL2 Phase Error <br> (18) TP9 N2 Oscillator <br> (33) TP10 N2 Phase Error <br> (34) TP11 N2 10 kHz <br> (32 TP12 N2 Phase Error Grounding <br> (15) TP13 SL1 Pulse Phase Error <br> (14) TP14 SL1 Phase Error <br> (35) TP15 N1 100 kHz <br> (10) TP16 N1 Phase Error Grounding <br> (12) TP17 N1 Phase Error <br> (30) TP18 N1 Oscillator <br> (37) TP19 SL1 Mixer Output TP20 Not Connected <br> (5) TP21 SL1 Driver <br> (8) TP22 SL1 Oscillator | (9) N1 Oscillator (A17) <br> (11) N1 Phase Detector (A16) <br> 11 N2 Oscillator (A13) <br> (16) N2 Phase Detector (A14) <br> 23 N3 Oscillator (A5) <br> (22) N3 Phase Detector (A10) <br> (21) SL2 Oscillator (A11) <br> (19) SL2 Phase Detector (A12) <br> (6) SL1 Oscillator (A19) <br> (13) SL1 Phase Detector (A15) <br> (1) SL1 Mixer (A18) | (1) 100 kHz Reference Input to N 2 <br> (2) 100 kHz Reference Input to N3 <br> (3) 400 kHz Reference Input to N1 <br> (4) SL1 Output <br> (31) BCD Frequency Data Digits 1 through 7 |

Figure 8-112. Mainframe Mother Board Test Points (2 of 2)

TOP VIEW


BOTTOM VIEW


A4 INVERTED


REAR VIEW

LEFT VIEW





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Table 8-54. Low Frequency Adjustment Identification

| $\begin{aligned} & \text { A8 } \\ & \text { (N3) } \end{aligned}$ | R24, R26 $\longrightarrow$ | Frequency Range Adjustment Pots |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { A11 } \\ & \text { (SL2) } \\ & \text { Osc. } \end{aligned}$ | $\begin{aligned} & \begin{array}{l} \text { R15, R19 } \\ \text { R39, } 54,60,67,73,77,83,90 ~ \end{array} \\ & \mathrm{C} 17 \longrightarrow \end{aligned}$ | Frequency Range Adjustment Pots Oscillator Pretune Pots 30 MHz Oscillator Trimmer Adjustment |
| $\begin{aligned} & \text { A12 } \\ & \text { (SL2 Det) } \end{aligned}$ | R37 $\longrightarrow$ | Phase Error Adjustment Pot |
| $\begin{aligned} & \text { A13 } \\ & \text { (N2 Osc) } \end{aligned}$ | $\begin{aligned} & \mathrm{R} 37, \mathrm{R} 39 \longrightarrow \\ & \mathrm{C} 19 \end{aligned}$ | Frequency Range Adjustment Pots 29.79 MHz Oscillator Trimmer Adjustment |
| A15 <br> (SL1) <br> Phase <br> Det | $\mathrm{R} 14 \longrightarrow$ | Phase Error Adjustment Pot |
| A16 <br> (N1 Det) | R38 $\longrightarrow$ | Phase Error Adjustment Pot |
| A17 <br> (N1 Osc) | $\begin{aligned} & \mathrm{R} 24, \mathrm{R} 31 \longrightarrow \\ & \mathrm{C} 17 \\ & \longrightarrow \end{aligned}$ | Frequency Range Adjustment Pots 29.7 MHz Oscillator Trimmer Adjustment |
| A18 (SL1 Mixer) | R35, 40, 44, 51, 55, 62, 68, $74 \rightarrow$ | Oscillator Pretune Pots |
| A19 <br> (SL1 Osc) | $\begin{aligned} & \mathrm{R} 3, \mathrm{R} 9 \longrightarrow \\ & \mathrm{C} 18 \longrightarrow \end{aligned}$ | Frequency Range Adjustment Pots 30 MHz Oscillator Trimmer Adjustment |



Figure 8-115. LF Loops Adjustment Locations


Table 8-56. Reference Loop Adjustment Identification

## A4A4 <br> (Ref Loop

VCO)



Figure 8-116. HP-IB Adapter
Ble 8-55. High Frequency Loop Adjustment Identification

## Table 8-56. Reference Loop Adjustment Identification



A4 ASSEMBLY




Figure 8-118. Self Test Features


[^0]:    *When using 86603A RF section above 1300 MHz least significant digit becomes either 2 Hz (standard) or 200 Hz (Option 004).

