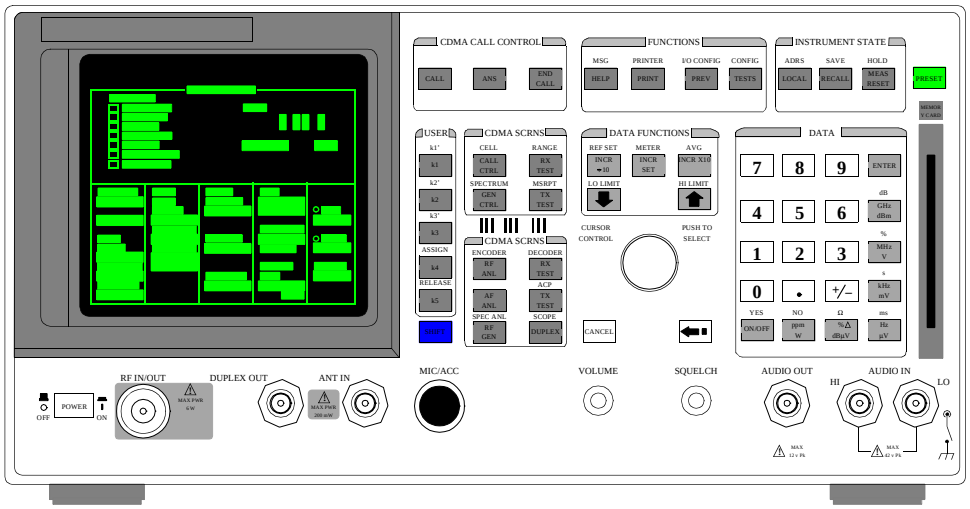
HP 8924C/E CDMA Mobile Station Test Set

Assembly Level Repair

HP 8924C: Firmware Version A.02.17 and above
HP 8924E: Firmware Version A.01.00 and above



HP P/N 08924-90061
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November 1998
Rev. A

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Hewlett-Packard Company
Learning Products Department
24001 E. Mission
Liberty Lake, WA 99019-9599
U.S.A.

Manufacturer’s Declaration

This statement is provided to comply with the requirements of the German Sound Emission Directive, from 18 January 1991.

This product has a sound pressure emission (at the operator position) < 70 dB(A).

- Sound Pressure Lp < 70 dB(A).
- At Operator Position.
- Normal Operation.
- According to ISO 7779:1988/EN 27779:1991 (Type Test).

Herstellerbescheinigung

Diese Information steht im Zusammenhang mit den Anforderungen der Maschinenlärminformationsverordnung vom 18 Januar 1991.

- Schalldruckpegel Lp < 70 dB(A).
- Am Arbeitsplatz.
- Normaler Betrieb.
- Nach ISO 7779:1988/EN 27779:1991 (Typprüfung).

Safety Considerations

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

This product has been designed and tested in accordance with *IEC Publication 1010*, "Safety Requirements for Electronic Measuring Apparatus," and has been supplied in a safe condition. This instruction documentation contains information and warnings which must be followed by the user to ensure safe operation and to maintain the product in a safe condition.

SAFETY EARTH GROUND

A uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set.

CHASSIS GROUND TERMINAL

To prevent a potential shock hazard, always connect the rear-panel chassis ground terminal to earth ground when operating this instrument from a dc power source.

SAFETY SYMBOLS

Indicates instrument damage can occur if indicated operating limits are exceeded. Refer to instruction in this guide.

Indicates hazardous voltages.

Indicates earth (ground) terminal

WARNING

A WARNING note denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

A CAUTION note denotes a hazard. It calls attention to an operation procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond an CAUTION note until the indicated conditions are fully understood and met.

Safety Considerations for this Instrument

WARNING

This product is a Safety Class I instrument (provided with a protective earthing ground incorporated in the power cord). The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. Any interruption of the protective conductor inside or outside of the product is likely to make the product dangerous. Intentional interruption is prohibited..

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.

If this product is not used as specified, the protection provided by the equipment could be impaired. This product must be used in a normal condition (in which all means for protection are intact) only.

No operator serviceable parts in this product. Refer servicing to qualified personnel. To prevent electrical shock, do not remove covers.

Servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.

The opening of covers or removal of parts is likely to expose dangerous voltages. Disconnect the product from all voltage sources while it is being opened.

Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

The power cord is connected to internal capacitors that my remain live for 5 seconds after disconnecting the plug from its power supply.

For Continued protection against fire hazard, replace the line fuse(s) only with 250 V fuse(s) or the same current rating and type (for example, normal blow or time delay). Do not use repaired fuses or short circuited fuseholders.

CAUTION: Always use the three-prong ac power cord supplied with this product. Failure to ensure adequate earth grounding by not using this cord may cause product damage.

This product is designed for use in Installation Category II and Pollution Degree 2 per *IEC 1010* and *IEC 664* respectively. For indoor use only.

This product has autoranging line voltage input, be sure the supply voltage is within the specified range.

Ventilation Requirements: When installing the product in a cabinet, the convection into and out of the product must not be restricted. The ambient temperature (outside the cabinet) must be less than the maximum operating temperature of the product by 4° C for every 100 watts dissipated in the cabinet. If the total power dissipated in the cabinet is greater than 800 watts, then forced convection must be used.

Product Markings

CE - the CE mark is a registered trademark of the European Community. A CE mark accompanied by a year indicated the year the design was proven.

CSA - the CSA mark is a registered trademark of the Canadian Standards Association.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASE ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products. For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name:	**Hewlett-Packard Co.**
Manufacturer's Address:	**Spokane Division** **24001 E. Mission Avenue** **Liberty Lake, Washington 99019-9599** **USA**

declares that the product

Product Name:	CDMA Mobile Station Test Set
Model Number:	HP 8924C
Product Options:	This declaration covers all options of the above product.

conforms to the following Product specifications:

Safety: IEC 1010-1:1990+A1 / EN 61010-1:1993
CAN/CSA-C22.2 No. 1010.1-92

EMC: CISPR 11:1990/EN 55011:1991 Group 1, Class A
IEC 801-2:1984/EN 50082-1:1992 4 kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1:1992 3V/m
IEC 801-4:1988/EN 50082-1:1992 0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:

This product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

Spokane, Washington USA November 20, 1995
Date

Vince Roland/Quality Manager

European Contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH Department ZQ/Standards Europe, Herrenberger Strasse 130, D-71034 Böblinger, Germany (FAX+49-7031-14-

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name:	**Hewlett-Packard Co.**
Manufacturer's Address:	**Spokane Division** **24001 E. Mission Avenue** **Liberty Lake, Washington 99019-9599** **USA**

declares that the product

Product Name:	CDMA Mobile Station Test Set
Model Number:	HP 8924E
Product Options:	This declaration covers all options of the above product.

conforms to the following Product specifications:

Safety: IEC 1010-1:1990+A1 / EN 61010-1:1993
CAN/CSA-C22.2 No. 1010.1-92

EMC: CISPR 11:1990/EN 55011:1991 Group 1, Class A
IEC 801-2:1984/EN 50082-1:1992 4 kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1:1992 3V/m
IEC 801-4:1988/EN 50082-1:1992 0.5 kV Sig. Lines, 1 kV Power Lines

Supplementary Information:

This product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

Spokane, Washington USA March 27, 1998
Date

Vince Roland/Quality Manager

European Contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH Department ZQ/Standards Europe, Herrenberger Strasse 130, D-71034 Böblinger, Germany (FAX+49-7031-14-

HP 8924C/E Support Contacts

The documentation supplied with your test set is an excellent source of reference, applications, and service information. Please use these manuals if you are experiencing technical problems:

Table 1Documentation P/Ns

Description	HP 8924C	HP 8924E
User's Guide	08924-90038	08924-90057
Application Guide	08924-90021	08924-90070
Reference Guide	08924-90053	08924-90060
Assembly Level Repair	08924-90061	
CD ROM	08924-90059	

If you have used the manuals and still have *application* questions, contact your local HP Sales Representative.

Repair assistance is available for the HP 8924C/E CDMA Mobile Test Set from the factory by phone and e-mail. Internal Hewlett-Packard users can contact the factory through HPDesk or cc:Mail© (Lotus Corporation). Parts information is also available from Hewlett-Packard.

When calling or writing for repair assistance, please have the following information ready:

- Instrument model number (HP 8924C/E)
- Instrument Serial Number (tag located on the rear panel).
- Installed options - if any (tag located on the rear panel).
- Instrument firmware revision (displayed at the top of the screen when the Test Set is powered up, and is also displayed on the CONFIGURE screen).

Support Telephone Numbers:

1 800 827 3848 (Spokane Division Service Assistance, U.S. only)
1 509 921 3848 (Spokane Division Service Assistance, International)
1 800 227 8164 (HP Direct Parts Ordering, U.S. only)
1 916 783 0804 (HP Service Parts Identification, U.S. & Intl.)

Electronic mail (Internet): Spokane_Service@spk.hp.com

cc:Mail: SERVICE, SPOKANE /HP-Spokane,desk1

Table 2 Regional Sales and Service Offices

United States of America U.S. Instrument Support Center For Test & Measurement Equipment Repair & Calibration. Hewlett-Packard Company Englewood, Colorado 80112 Telephone: (800) 403-0801 Fax: (888) 857-8161	United States of America Customer Information Center For Assistance On All HP Products. Hewlett-Packard Company Tel: (800) 752-0900 6:00 am to 5:00 pm Pacific Time Parts Direct: 1-800-227-8164	
South Eastern Europe Sales and Service Hewlett-Packard Ges. m.b.h. Liebigasse 1 P.O. Box 72 A-1222 Vienna, Austria Telephone: 43 222 2500 0 Telex: 13 4425	European Multicountry Region Sales and Service Hewlett-Packard S.A. P.O. Box 95 150, Route dv Nant_dl_AVRIL CH-1217 Meyrin 2 Geneva, Switzerland Telephone: (41/22) 780-8111 Fax: (41/22) 780-8542	Northern Europe Sales and Service Hewlett-Packard Nederland B.V. Startbaan 16 1187 XR Amstelveen, The Netherlands P.O. Box 667 Telephone: 31/20 5476911 X 6631 Fax: 31-20-6471825NL
Asia Sales and Service Hewlett-Packard Asia Ltd. 22-30/F Peregrine Tower Lippo Center 89 Queensway, Central Hong Kong G.P.O. Box 863 Hong Kong Telephone: 852-848-7777 Fax: 852-868-4997	Japan Sales and Service Yokogawa-Hewlett-Packard Ltd. 3-29-21, Takaido-Higashi Suginami-Ku, Tokyo 168 Telephone: 81 3 3331-6111 Fax: 81 3 3331-6631	International Sales Branch Headquarters Sales and Service Hewlett-Packard S.A. 39 Rue Veyrot P.O. Box 365 1217 Meyrin 1 Geneva, Switzerland Telephone: 41-22-780-4111 Fax: 41-22-780-4770
Australia, New Zealand Sales and Service Hewlett-Packard Ltd. P.O. Box 221 31-41 Joseph Street Blackburn, Victoria 3130 Telephone: (61/3) 895-2895 Fax: (61/3) 898-9257	Canada Sales and Service Hewlett-Packard (Canada) Ltd. 5150 Spectrum Way Mississauga, Ontario L4W 5G1 Canada Telephone: (416) 206-4725 Fax: (416) 206-4739	Canada Service Center Hewlett-Packard Company 17500 Transcanada Highway S. Serv Road Kirkland, Quebec H9J 2X8 Canada Telephone: (416) 206-3295

Table 2 Regional Sales and Service Offices (Continued)

Canada
Service Center
Hewlett-Packard Ltd.
11120 178 Street
Edmonton, Alberta T5S 1P2
Canada

Telephone: (403) 486-6666
Fax: (403) 489-8764

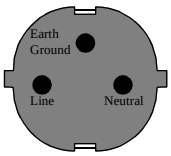
Latin America
Hewlett-Packard Company
LAHQ Mexico City
Col. Lomas de Virreyes
11000 Mexico D.F.
Mexico

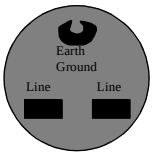
Telephone: (52/5) 326-4000
Fax: (52/5) 202 7718

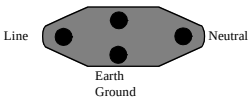
United Kingdom
Sales and Service
Hewlett-Packard Ltd.
Cain Road
Amen Corner
Bracknell, Berkshire
RG12 1HN
United Kingdom

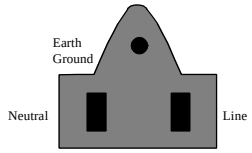
Telephone: 44 344 360000
Fax: 44 344 363344

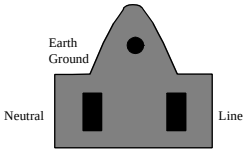
Power Cables

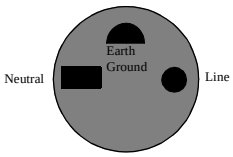
Plug Type	Plug Descriptions male/female	HP Part # (cable &plug)	Cable Descriptions
	Straight/Straight Straight/90°	8120-1689 8120-1692	79 inches, mint gray 79 inches, mint gray
Used in the following locations			
Afghanistan, Albania, Algeria, Angola, Armenia,Austria, Azerbaijan, Azores			
Bangladesh, Belgium, Benin, Bolivia,Boznia-Herzegovina, Bulgaria, Burkina Faso, Burma, Burundi,Byelarus			
Cameroon, Canary Islands, Central AfricanRepublic, Chad, Chile, Comoros, Congo, Croatia, Czech Republic,Czechoslovakia			
Denmark, Djibouti			
East Germany, Egypt, Estonia, Ethiopia			
Finland, France, French Guiana, French Indian Ocean Areas			
Gabon, Gaza Strip, Georgia, Germany, Gozo, Greece			
Hungary			
Iceland, Indonesia, Iran, Iraq, Israel, Italy, Ivory Coast			
Jordan			
Kazakhstan, Korea, Kyrgystan			
Latvia, Lebanon, Libya, Lithuania, Luxembourg			
Macedonia, Madeira Islands, Malagasy Republic, Mali, Malta, Mauritania, Miquelon, Moldova, Mongolia, Morocco, Mozambique			
Nepal, Netherlands, Netherlands Antilles, Niger, Norway			
Oman			
Pakistan, Paraguay, Poland, Portugal			
Rep. South Africa, Romania, Russia, Rwanda			
Saudi Arabia (220V), Senegal, Slovak Republic, Slovenia, Somalia, Spain, Spanish Africa, Sri Lanka, St.Pierce Islands			
Sweden, Syria			
Tajikistan, Thailand, Togo, Tunisia, Turkey, Turkmenistan			
USSR, Ukraine, Uzbekistan			
Western Africa, Western Sahara			
Yugoslavia			
Zaire			

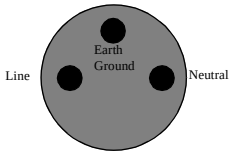
Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
	Straight/Straight	8120-0698	90 inches, black
Used in the following locations			
Peru			

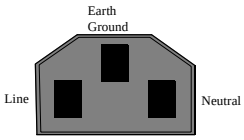
Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
	Straight/Straight Straight/90°	8120-2104 8120-2296	79 inches, gray 79 inches, gray
Used in the following locations			
Switzerland			

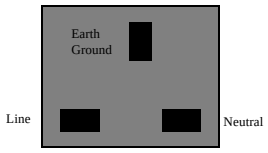
Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
125V  	Straight/Straight Straight/90° Straight/Straight	8120-1378 8120-1521 8120-1751	90 inches, jade gray 90 inches, jade gray 90 inches, jade gray
Used in the following locations			
American Samoa			
Bahamas, Barbados, Belize, Bermuda, Brazil,			
Caicos, Cambodia, Canada, Cayman Islands, Columbia, Costa Rica, Cuba			
Dominican Republic			
Ecuador, El Salvador			
French West Indies			
Guam, Guatemala, Guyana			
Haiti, Honduras			
Jamaica			
Korea			
Laos, Leeward and Windward Is., Liberia			
Mexico, Midway Islands			
Nicaragua			
Other Pacific Islands			
Panama, Philippines, Puerto Rico			
Saudi Arabia (115V,127V), Suriname			
Taiwan, Tobago, Trinidad, Trust Territories of Pacific Islands			
Turks Island			
United States			
Venezuela, Vietnam, Virgin Islands of the US			
Wake Island			

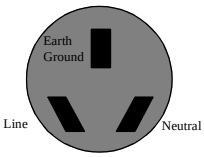
Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
JIS C 8303, 100 V 	Straight/Straight Straight/90°	8120-4753 8120-4754	90 inches, dark gray 90 inches, dark gray
Used in the following locations			
Japan			

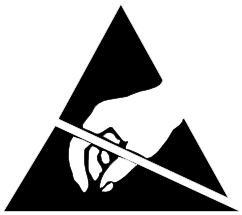
Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
	90°/Straight 90°/90° Straight/Straight	8120-2956 8120-2957 8120-3997	79 inches, gray 79 inches, gray 79 inches, gray
Used in the following locations			
Denmark			
Greenland			

Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
	Straight/Straight Straight/90°	8120-4211 8120-4600	79 inches, mint gray 79 inches, mint gray
Used in the following locations			
Botswana			
India			
Lesotho			
Malawi			
South-West Africa (Namibia), Swaziland			
Zambia, Zimbabwe			

Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
	Straight/Straight Straight/Straight Straight/90° Straight/90°	8120-1860 8120-1575 8120-2191 8120-4379	60 inches, jade gray 30 inches, jade gray 60 inches, jade gray 15.5 inches, jade gray
Used in the following locations			
System Cabinets			

Plug Type (Male)	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
	90°/Straight 90°/90°	8120-1351 8120-1703	90 inches, mint gray 90 inches, mint gray
Used in the following locations			
Bahrain, British Indian Ocean Terr., Brunei			
Canton, Cyprus			
Enderbury Island, Equatorial Guinea			
Falkland Islands, French Pacific Islands			
Gambia, Ghana, Gibraltar, Guinea			
Hong Kong			
Ireland			
Kenya, Kuwait			
Macao, Malaysia, Mauritius			
Nigeria			
Qatar			
Seychelles, Sierra Leone, Singapore, Southern Asia, Southern Pacific Islands, St. Helena, Sudan			
Tanzania			
Uganda, United Arab Emirates, United Kingdom			
Yeman (Aden & Sana)			

Plug Type	Plug Descriptions male/female	HP Part # (cable & plug)	Cable Descriptions
	Straight/Straight Straight/90°	8120-1369 8120-0696	79 inches, gray 80 inches, gray
Used in the following locations			
Argentina, Australia			
China (People's Republic)			
New Zealand			
Papua New Guinea			
Uruguay			
Western Samoa			



ATTENTION
Static Sensitive Devices

This instrument was constructed in an ESD (electro-static discharge) protected environment. This is because most of the semi conductor devices used in this instrument are susceptible to damage by static discharge.

Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity of a static charge. The result can cause degradation of device performance, early failure, or immediate destruction.

These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction.

Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service circuitry with these devices.

In all instances, measures must be taken to prevent static charge build-up on work surfaces and persons handling the devices.

In This Book

Chapter 1, Introduction

A general description of what the Test Set does is included. Theory of Operation, troubleshooting, repairing, calibrating, and verifying instrument performance are discussed. Additional HP support information is provided.

Chapter 2, Troubleshooting

The process for isolating a failure to the faulty assembly is discussed, including how to use the automated diagnostic routines.

Chapter 3, Repair

Illustrated disassembly/assembly drawings are provided to show the order of disassembly and to identify the component designators for most assemblies.

Chapter 4, Periodic Adjustment

Automated calibration procedures for various Test Set functions are discussed, including step-by-step procedures for using the automated calibration procedures.

Chapter 5, Performance Verification

Procedures are provided to verify the performance of each section of the Test Set. Included are the necessary test instruments are their settings, instruments connections, and the Test Set setup0 needed for each test.

Chapter 6, Specifications

The warranted specifications of the Test Set are listed.

Chapter 7, Service Screen

A description of the Service Screen and its operation is provided.

Chapter 8, Block Diagrams

Diagrams are provided illustrating the general operation of major sections of the Test Set. The diagrams also provide detailed illustrations of each assembly, including signal functions and connector pin numbers. This information is used to better understand the operation of the Test Set when manually troubleshooting (if the automated diagnostics cannot identify a faulty assembly with high confidence).

Chapter 9, Replaceable Parts

Part numbers for each replaceable part are provided.

Chapter 10, Diagnostic Descriptions

Test Set's automated diagnostics are described. The descriptions help you understand what has been checked by the diagnostics in case they cannot identify a probable failure and you must troubleshoot further.

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1

Introduction

This manual explains how to repair and calibrate the HP 8924C/E CDMA Mobile Station Test Set; called “the Test Set” throughout this manual.

Test Set Description

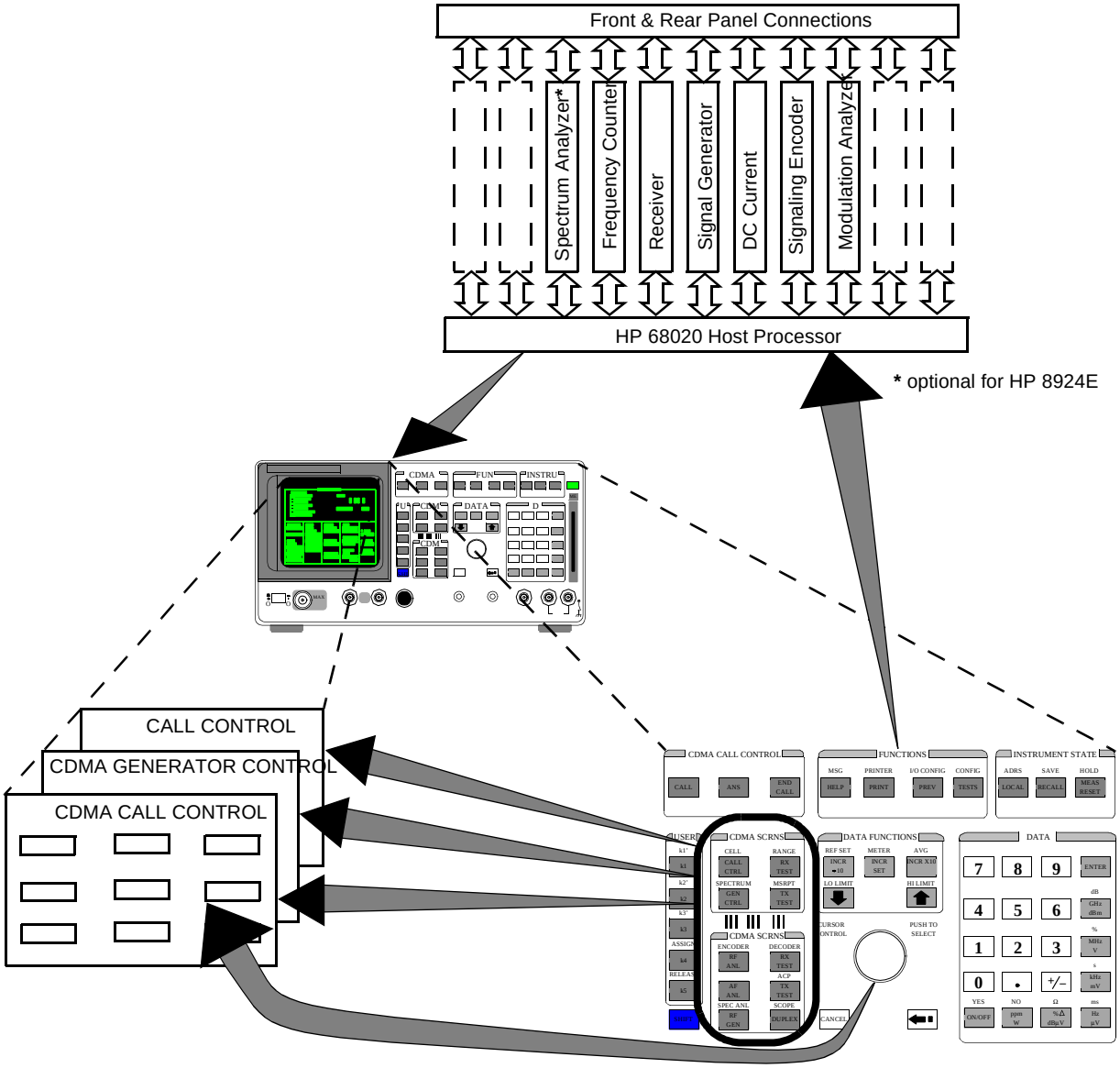
Several analog and digital test instruments are integrated into one package to test Code Division Multiple Access (CDMA) digital cellular telephones and several types of analog telephones (such as AMPS, NAMPS, and TACS). Some of the instrument functions in the Test Set include:

- Synthesized AM, FM, and IQ modulation signal generator
- AM, FM, and IQ modulation analyzer
- Duplex offset generator
- SSB demodulator
- RF and audio power meters
- Audio and RF frequency counter and RF frequency error meter
- AC and DC voltmeter
- Distortion, SINAD, and signal-to-noise-ratio meters
- Two variable audio sources
- Oscilloscope
- Spectrum analyzer and tracking generator (optional on HP 8924E)
- Signaling encoder and decoder
- DC current meter

Some of these functions are directly replaceable assemblies (such as the spectrum analyzer); some functions are digitally derived from other assemblies (such as the oscilloscope). There are about 40 replaceable assemblies - mostly plug-in printed circuit boards.

Most instrument functions can be controlled by front-panel (local) controls and by remote commands (using a connected controller). Power on/off, volume, and squelch controls cannot be accessed remotely. Controls are grouped together on display screens that are usually associated with a specific task (such as making a call to a CDMA mobile phone).

An HP Instrument BASIC (IBASIC) computer is also built into the Test Set to allow automated operation without using an external controller. This computer also has the ability to be a system controller to other test system instruments. Refer to the Test Set's *User's Guide* for information on using the IBASIC computer (also referred to as the IBASIC controller).


Front & Rear Panel Connections
Spectrum Analyzer*
Frequency Counter
Receiver
Signal Generator
DC Current
Signaling Encoder
Modulation Analyzer
HP 68020 Host Processor
* optional for HP 8924E
CALL CONTROL
CDMA GENERATOR CONTROL
CDMA CALL CONTROL

Theory of Operation

The Test Set is primarily an RF transceiver that operates in the 30 to 1000 MHz range, and a group of instruments that analyze received signals. Several modulation sources are available for testing a variety of cellular phones and other types of radios. A modulation analyzer is used to measure various parameters on the received signal from the radio-under-test. The oscilloscope and spectrum analyzer provide additional received signal analysis.

The following information is very general. Refer to Chapter 9, *Block Diagrams,* for detailed drawings for each assembly.

Internal Operating System

A 68020 microprocessor acts as the “host” processor of the Test Set. It receives commands from the front-panel controls and communicates directly with almost every assembly inside the Test Set. The host is also in constant communication with several other microprocessors located in assemblies throughout the Test Set.

Communications to the HP-IB, Serial, and Parallel ports are through the Control Interface (A33) assembly to the host processor.

This processor is also the core for the internal IBASIC computer. The IBASIC computer is used to load and run various software packages for automated radio tests. It is also responsible for executing the internal diagnostic routines used to troubleshoot a failing instrument.

Instrument Frequency References

Most of the Test Set's internal oscillators and counters are phase-locked to the signal input from the rear-panel REF INPUT port. This signal is usually the output of the 10 MHz Oven Oscillator (A38) assembly, also available on the rear-panel. The Reference Assembly (A27) is internally connected to the CDMA Reference (A29), which is connected to the external reference. The CDMA Reference provides the clocks for the CDMA assemblies, the AWGN (Additive White Gaussian Noise) source, and the reference for the Reference Assembly. The Reference Assembly provides the references for the analog assemblies.

If the message"**`Reference unlocked, check reference connection and frequency`**" is displayed on the top of the Test Set's screen, verify that a good BNC cable (or factory jumper) is connected between the REF INPUT and 10 MHz OVEN OUT ports. If the message is still displayed, make sure the **`External Reference`** control on the CONFIGURE screen is set to **`10.0000 MHz`**, and use a frequency counter to verify the presence and frequency of the 10 MHz Oven's Output signal. If an external reference is used, verify that the reference frequency matches the **`External Reference`** setting (±10 ppm), and that the level is at 0 dbm (±3 dB).

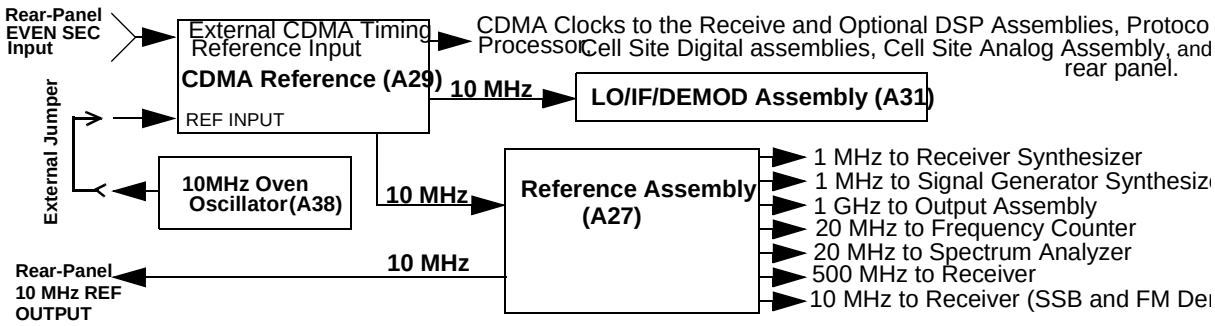


Figure 1 **Reference Signal Generation**

RF Analysis

RF signals connected to the front panel RF IN/OUT port or ANTENNA IN port go to the Input Assembly (A5) . The signal level and RF frequency are measured, and the level is adjusted using fixed step and variable attenuators.

OVER-POWER DAMAGE!

The ANTENNA IN connector is only used for very low level signals (200 mW or less), and cannot be used for Transmitter (TX) Power measurements. Exceeding this limit may destroy this assembly! The RF IN/OUT connector is used to measure direct mobile transmitter power up to 6.0 Watts.

The Receiver 1st Mixer Assembly (A19) then mixes the signal with a local oscillator signal from the Receiver Synthesizer Assembly (A28) to produce a 114.3 MHz or 614.3 MHz IF signal (depending on the frequency of the received signal). The signal goes through a bandpass filter and then to the Receiver Assembly (A30). .

If the IF is 614.3 MHz, the Receiver Assembly then mixes the signal with a 500 MHz LO signal from the Reference Assembly (A27) to get the 114.3 MHz IF. If the IF from A28 is already 114.3 MHz, the signal bypasses this downconversion.

The 114.3 MHz signal divides into two paths.

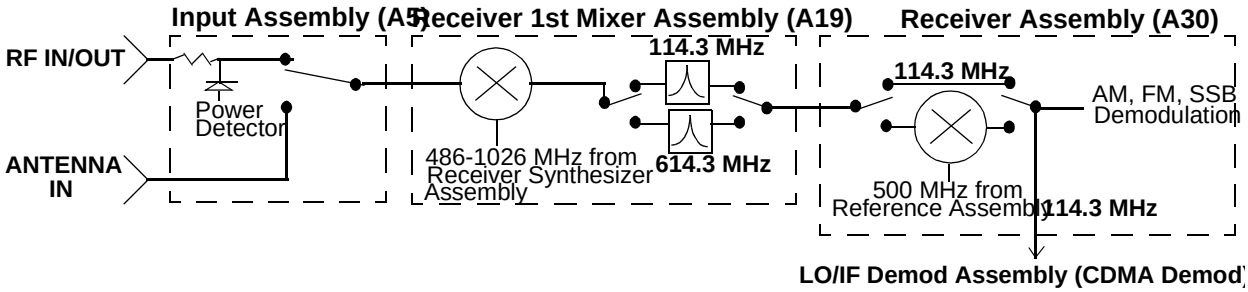


Figure 2 Received Signal Downconversion

AM, FM, or SSB Modulation Analysis

(HP 8924E: FM only)

For AM, FM, or SSB signals, the 114.3 MHz signal is downconverted to 10.7 MHz and routed through a user-selected IF bandpass filter (15 kHz or 230 kHz) that is centered around the 10.7 MHz IF. AM and SSB signals are demodulated at this point; FM signals are downconverted to a 700 kHz IF before demodulation. The demodulated signal is routed to the Audio Analyzer 1 (A35) assembly for audio frequency filtering. This assembly is also connected to the front-panel AUDIO IN connector for direct audio measurements. Several low-pass and high-pass filters can be selected, as well as a C-Message or optional CCITT filter. Frequency and voltage measurements are then made on this signal by the Measurement Assembly (A37) . The signal is then routed to the Audio Anlayzer 2 (A36) assembly.

The Audio Analyzer 2 assembly routes the signal through a user-selectable detector. A variable frequency notch filter may also be selected for SINAD and distortion measurements. The detector's signal is then sent to several other assemblies:

- The Measurement Assembly, to measure and display the modulation level (such as FM deviation) and provide the input to the oscilloscope.
- The Signaling Source and Analyzer (A15) assembly for signaling decoding.
- The rear-panel AUD MONITOR OUTPUT connector for external use of the demodulated signal.
- The front-panel **VOLUME** control and internal **Speaker** to listen to the demodulated signal.

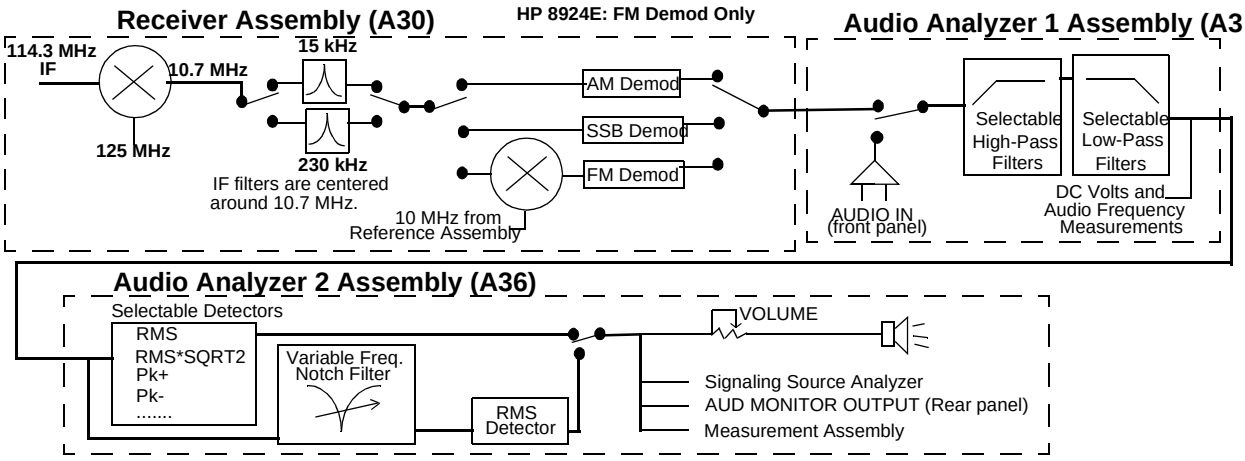


Figure 3 **AM, FM, and SSB Signal Demodulation and Filtering**

CDMA Signal Analysis

The 114.3 MHz IF also goes to the LO/IF Demod (A13) assembly. This assembly provides a path to the Spectrum Analyzer (A32) for all RF signals, and also provides down conversion for CDMA signals.

To downconvert the CDMA signal, the 114.3 MHz IF is mixed with a 117.9864 MHz LO to produce a 3.6864 MHz IF. (The LO signal is from an oscillator that is phase locked to a 10 MHz signal from the CDMA Reference module.)

The 3.6864 MHz signal goes to the Receiver DSP (A12) and Optional DSP (A11) assemblies, and also goes through a variable-gain IF Amplifier and an IQ Demodulator. The demodulator provides I and Q baseband signals to the Cell Site Digital (A7 & A9) assemblies.

Under control from the Protocol Processor (A6) assembly, the Cell Site Digital assemblies use the IQ information to set up and maintain calls to CDMA phones. The Cell Site Digital 1 assembly also furnishes feedback to the LO/IF/DEMOD assembly to control the level of the variable-gain IF Amplifier into the demodulator.

The Receive DSP assemblies analyze the 3.6864 MHz signal to make IQ modulation measurements, such as Rho, Timing Accuracy, Carrier Feedthrough, and Phase Error.

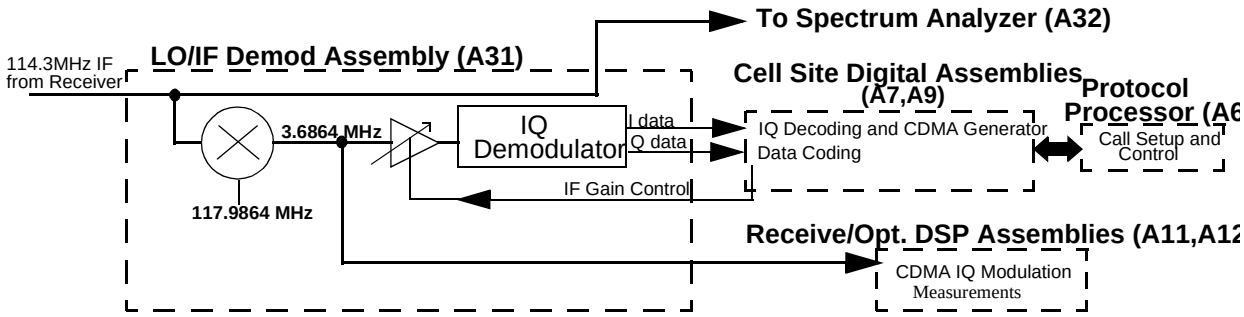


Figure 4 Analyzing CDMA Signals

RF Signal Generation

The Signal Generator Synthesizer (A24) assembly creates a 500-1000 MHz signal. The reference signal for the synthesizer is supplied by the Reference (A27) assembly. The synthesizer's frequency is varied using a divider network in the feedback circuit of the phase locked loop. Any FM modulation signal (from the Modulation Distribution (A34) assembly), and the frequency sweep signal for the Spectrum Analyzer and Tracking Generator, are integrated into this feedback loop. If a CDMA signal is not being generated, the 500-1000 MHz signal is passed through the I/Q Modulator (A25) assembly, bypassing the I/Q modulator.

IQ Modulation

If a CDMA signal is being generated, the signal is I/Q modulated in the I/Q Modulator assembly, using data from the Cell Site Analog (A8) assembly. The Cell Site Analog assembly gets its data from the two Cell Site Digital (A7 & A9) assemblies, which are controlled by the Protocol Processor (A6) assembly. Up to eight code channels of CDMA modulation data and noise may be summed into the IQ modulator at one time. These channels provide phone paging, synchronization, voice (traffic) transmission, and other CDMA system functions.

Final Frequency Conversion and Leveling

The Output (A26) assembly performs three tasks:

- Mixes or divides the 500-1000 MHz signal to produce signals below 500 MHz (down to 0.4 MHz). A 1 GHz LO from the Reference (A27) assembly is used for mixing.
- Provides AM modulation (when selected).

- Controls the signal level out of the assembly using an Automatic Level Control (ALC) loop.

The signal out of the Output assembly is now at the user-selected frequency, and contains any modulation that was selected (AM, FM, or CDMA), or is a continuous wave (CW) signal. The level has been adjusted to provide the required level (after going through the Input (A5) assembly).

RF and DUPLEX Outputs

The Input assembly receives the signal from the output assembly and routes it to the selected output port: RF IN/OUT or DUPLEX OUT. The signal first goes to a variable attenuator for level control. If the DUPLEX OUT port is selected, the signal then goes directly to that port without additional attenuation. If the RF IN/OUT port is used as an output, the signal passes through additional attenuation before reaching the port. This is why a greater signal level can be output through the DUPLEX OUT port than through the RF IN/OUT port.

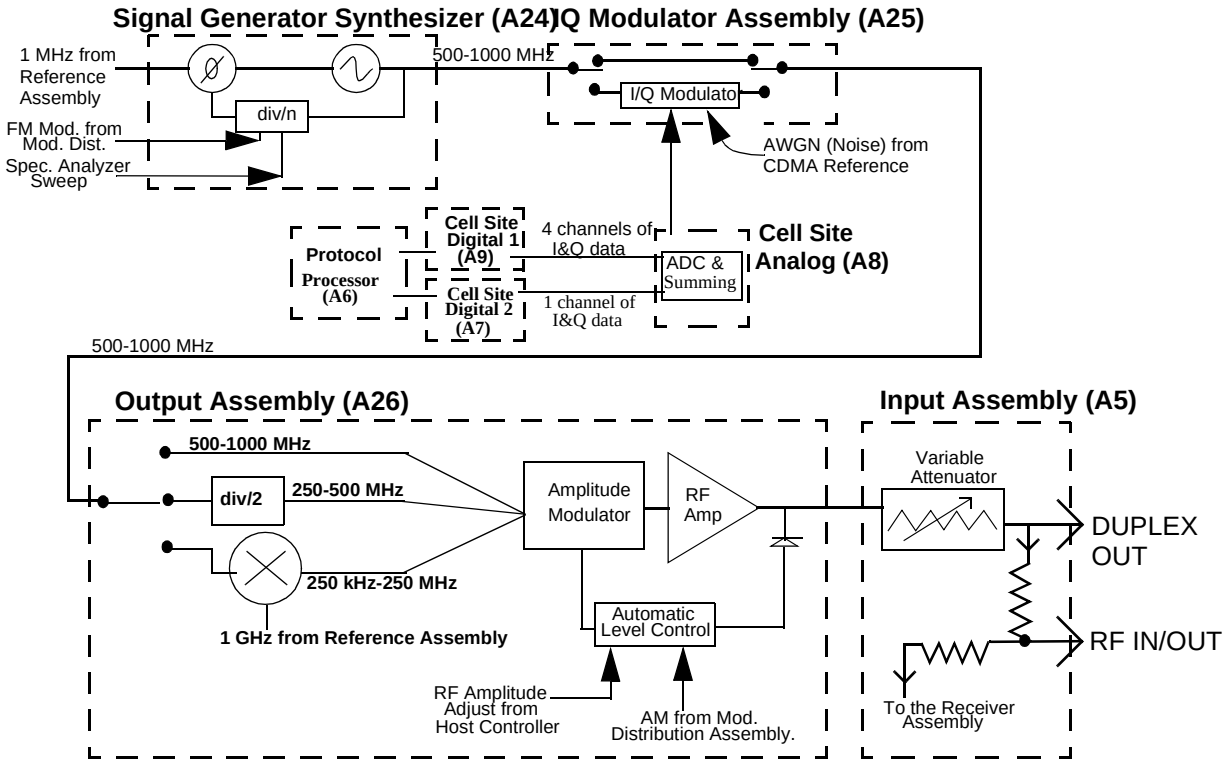


Figure 5 RF Generation Path Overview

Troubleshooting Strategy

You can repair the Test Set yourself or send it to your local Hewlett-Packard Customer Service Center. Before starting a repair, you should become familiar with basic Test Set operation using the *User's Guide*.

Troubleshooting relies on built-in diagnostics. Because some diagnostic results may be ambiguous, further interpretation and testing may be required. There are several diagnostic routines built into the Test Set:

- Power-up self-test diagnostics to test controller functioning. These are automatically run when the instrument is turned on, and can also be run after the instrument has been on.
- RF (Radio Frequency) assembly diagnostics.
- AF (Audio Frequency) assembly diagnostics.
- Digital assembly diagnostics for CDMA signals.

Troubleshooting hints in this manual include:

- Instructions on how to begin troubleshooting (see **chapter 2, "Troubleshooting"**).
- Block diagrams and theory of operation (see **chapter 11, "Block Diagrams"**).
- Detailed information about the built-in diagnostics (see **chapter 14, "Diagnostics Descriptions"**).
- Error message explanations (see *Appendix A: Error Messages*) .

Repair Process

Repairing the Test Set consists of:

- Identifying the faulty assembly (see **chapter 2, "Troubleshooting"**)
- Ordering a replacement assembly (see **chapter 12, "HP 8924C Replaceable Parts"** or **chapter 13, "HP 8924E Replaceable Parts"**)
- Replacing the faulty assembly (see **chapter 3, "Repair"**)
- Downloading calibration data (see**chapter 3, "Repair"**)
- Performing periodic calibration (see **chapter 4, "Periodic Adjustments"**)
- Verifying Test Set performance (see **chapter 5, "HP 8924C Performance Verification"** or **chapter 6, "HP 8924E Performance Verification"**)

Calibration and Performance Verification

The Test Set periodically requires some maintenance to verify that it meets its published specifications. Periodic Adjustments (calibration) consists of running several built-in calibration programs, and should be performed every year. An external frequency counter and dc voltmeter are required. (See **chapter 4, "Periodic Adjustments"**).

The Performance Verification tests in chapter 5 verify that the Test Set performs as indicated in the Specifications. These tests should be performed if the Test Set's operation is suspect, even though it passes all internal diagnostic checks. This identifies whether a problem actually exists in the Test Set, or if an application problem exists outside of the Test Set.

Several assemblies, when replaced, require running specific periodic calibration procedures to create calibration factors for that assembly. In other cases, the calibration data will be included with the replacement assembly on a memory card. Instructions that come with the replacement assembly explain how to download the calibration data. (This is not considered part of periodic calibration.)

NOTE: When troubleshooting the Test Set, it is sometimes desirable to swap a known-good assembly (perhaps from another Test Set) for a suspected-faulty assembly. If the swapped assembly requires calibration data, most assemblies will operate well enough with the original assembly's calibration data to troubleshoot and run the diagnostics. However, do not expect the Test Set to meet its specifications. Also, some assemblies may appear to fail because of the incorrect calibration data.

HP 8924C/E Support Contacts

The documentation supplied with your test set is an excellent source of reference, applications, and service information. Please use these manuals if you are experiencing technical problems:

Table 3Documentation P/Ns

Description	HP 8924C	HP 8924E
User's Guide	08924-90038	08924-90057
Application Guide	08924-90021	08924-90070
Reference Guide	08924-90053	08924-90060
Assembly Level Repair	08924-90061	
CD ROM	08924-90059	

If you have used the manuals and still have *application* questions, contact your local HP Sales Representative.

Repair assistance is available for the HP 8924C/E CDMA Mobile Test Set from the factory by phone and e-mail. Internal Hewlett-Packard users can contact the factory through HPDesk or cc:Mail© (Lotus Corporation). Parts information is also available from Hewlett-Packard.

When calling or writing for repair assistance, please have the following information ready:

- Instrument model number (8924C/E)
- Instrument Serial Number (tag located on the rear panel).
- Installed options - if any (tag located on the rear panel).
- Instrument firmware revision (displayed at the top of the screen when the Test Set is powered up, and is also displayed on the CONFIGURE screen).

Support Telephone Numbers:

1 800 827 3848 (Spokane Division Service Assistance, U.S. only)
1 509 921 3848 (Spokane Division Service Assistance, International)
1 800 227 8164 (HP Direct Parts Ordering, U.S. only)
1 916 783 0804 (HP Service Parts Identification, U.S. & Intl.)

Electronic mail (Internet): Spokane_Service@spk.hp.com

cc:Mail: SERVICE, SPOKANE /HP-Spokane,desk1

Hardware and Firmware Enhancements

The hardware and firmware of the Test Set are enhanced on a continuous basis. If an assembly is replaced, it is recommended that the firmware be upgraded at the same time. This is important if an assembly-level repair is performed because exchange assemblies, which may be of a later revision than the one being replaced, may require a later revision of the firmware to function correctly.

2

Troubleshooting

This chapter tells how to isolate a problem to the defective assembly. Troubleshooting is centered around the built-in diagnostics. If diagnostics can’t identify the faulty assembly, supplementary information in the form of detailed Block Diagrams (**chapter 11**), Diagnostics Descriptions (**chapter 14**), and descriptions of **"Error Messages" on page 613** are provided.

How to Troubleshoot the Test Set

This section explains the steps for troubleshooting the Test Set. Document the result of each step in case you need to contact Hewlett-Packard for service assistance.

ARE YOU SURE A PROBLEM EXISTS?

Before troubleshooting the Test Set, you should attempt to duplicate the problem by performing the application where the suspected failure occurred. This is especially important if the Test Set is being used in a new application where misapplication, or incorrect operation of the Test Set may be involved.

If the Test Set fails in an application where it has worked correctly before, and the unit-under-test is working correctly, a failure probably exists.

Step 1- Run the Power-up Diagnostic

On power-up, the Test Set runs a Self-Test Diagnostic. Most of the Test Set's digital control functions are tested. The outcome of the test appears on the CRT (if operating) and on four LEDs under the top cover.

Step 2- Run the Functional Diagnostic Routines

The RF, AF, Miscellaneous, and Digital diagnostic routines verify the proper operation of most assemblies in the Test Set. If a problem is found, the suspected faulty assembly is indicated, along with the level of confidence that replacing the indicated module will correct the problem.

Step 3- Run the Periodic Calibration Routines

Operating parameters may drift over extended periods. Built-in calibration routines adjust certain data latch settings to assure optimal Test Set operation. Applications requiring operation at the limits of Test Set's performance may fail if the Test Set is not calibrated.

Step 4- Manual Troubleshooting

Suggestions of things to try include: using Performance Tests to verify specified operation, and swapping assemblies.

These steps are illustrated on the next page. Instructions for performing these steps are given in this chapter.

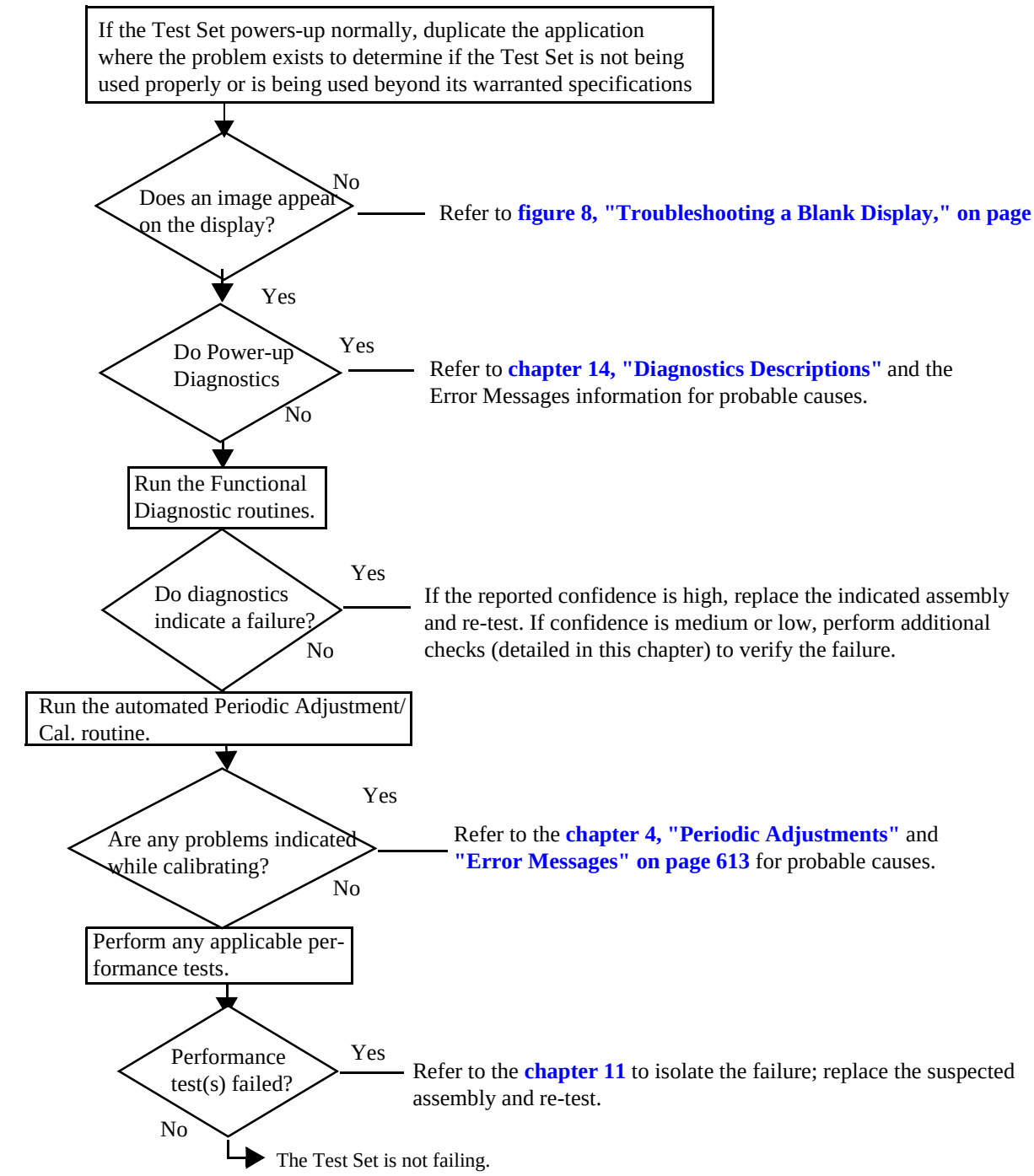


Figure 6 **Troubleshooting Flowchart**

Step 1- Run the Power-up Diagnostics

To start troubleshooting:

- Turn on the Test Set to automatically run the power-up diagnostics.
- After power-up, the top line of the Test Set's display should show copyright information and the firmware revision code. The second line should display **`All self tests passed`**.
- The CDMA CALL CONTROL screen should be displayed. Two conditions cause a different screen to be displayed on power-up:
  - r A SAVE/RECALL register named POWERON was saved to automatically power-up the box in a different state. Press the PRESET key before proceeding; this will restore the Test Set to the factory power-up condition.
  - r The **`Autostart Test Procedure on Power-Up:`** field is set to **`On`** to automatically run a loaded program. Press the SHIFT key, then press the CANCEL key to stop the program. Press the PRESET key to restore the Test Set to the factory power-up condition.

    To turn the autostart function off, press the TESTS key, then select Execution Cond function (under the **`SET UP TEST SET:`** heading). The autostart function is at the bottom of the screen; turn it **`Off`**.

If **`All self tests passed`** is displayed, run the Functional Diagnostics to try to locate the fault.

If the Test Set powers up with an error condition, or if the screen is blank: **See "More About Step 1- Run the Power-Up Diagnostic" on page 79**.

Step 2- Run the Functional Diagnostics

The Functional Diagnostics make measurements that test many of the circuits. There are four Functional Diagnostics. The first three (Audio, RF, and CDMA diagnostics) can be run in a loop mode after an initial setup. This is useful for trapping intermittent failures. The fourth diagnostic (Miscellaneous Diagnostics) requires a different setup for each test.

Functional Diagnostics should pinpoint faults in the AF, RF, and CDMA-related circuits to the faulty assembly. When a measurement is out-of-limits, the diagnostics post a message suggesting which assembly to replace and the certainty (low, medium, or high) of that suggestion. Before ordering replacement parts (especially when the certainty is medium or low) or if you have difficulty in understanding or running the Functional Diagnostics, **See "More About Step 2- Run the Functional Diagnostics" on page 81**.

NOTE: The measurement limits of the Functional Diagnostic tests are valid only at room temperature; that is, 20 to 25°C or 65 to 75°F.

Select the Test

1. Press the PRESET key.
2. Press the TESTS key.
3. Set the **`Select Procedure Location:`** field to **`ROM`**.
4. Set the **`Select Procedure Filename:`** field to load one of the diagnostic routines.
   - **`AFDIAGS3`** (to run the Audio Diagnostics)
   - **`RFDIAGS3`** (to run the RF Diagnostics)
   - **`MSDIAGS3`** (to run the Miscellaneous Diagnostics)
   - **`CDMADIAG`** (to run the CDMA Diagnostics)

Define Testing Conditions

5. Under the **`SET UP TEST SET:`** area, select Execution Cond to access the TESTS (Execution Conditions) screen.
6. Set **`Output Results To`**:
   - **`Crt`** to view measurements only on the display.
   - **`Printer`** to print the test results as well as display them on the CRT. The printer

is configured later in this procedure

7. Under **`Output Results For:`**
   - Select **`All`** to display (and print) all test information.
   - Select **`Failures`** to only display (and print) failed test points.
8. Under **`If Unit-Under-Test Fails:`**
   - Select **`Continue`** to continue to the next test point.
   - Select **`Stop`** to pause testing at that point.
9. Under **`Test Procedure Run Mode:`**
   - Select **`Continuous`** to run the tests continuously.
   - Select **`Single Step`** to pause after each measurement.
10. Under **`Autostart Test Procedure on Power-Up:,`** verify that the setting is **`Off`**.

CONFIGURE A PRINTER

Only perform this next step if you want to print test results to a printer, otherwise go to step 16.

11. Press the TESTS key to return to the TESTS (Main Menu) screen.
12. Under **`SET UP TEST SET:`**, select **`Printer Setup`** to access the TESTS (Printer Setup) screen.
13. Under **`PRINT SETUP:`**, select the **`Model:`** of printer to use.
14. Set the **`Printer Port:`** for the rear-panel connector your printer is connected to.

    If an HP-IB printer is used, you need to enter the printer's two-digit bus address when the **`Printer Adrs`** field appears (Example; enter **`01`** for bus address 701). Also, press the SHIFT key, then the PREV key to access the I\O CONFIGURE screen, and set the **`Mode`** field to **`Control`**.
15. Under **`PAGE CONTROL:`**, set the **`Lines/Page`**: and Form Feed (**`FF at Start:`**, and **`FF at End:`**) parameters if necessary.

Begin Testing

16. Select the **`Run Test`** field (or press K1) and wait for the "**`Loading program - Enter SHIFT-CANCEL to abort.`**" message to go away.
17. Choose the test or tests to run by selecting **`Up`** or **`Down`** to move the pointer and then choosing **`Select`**. When running the Audio, RF, or CDMA diagnostics for the first time, you should run "**`All xxx Tests`**" (xxx=Audio, RF, or CDMA).
18. Follow the instructions on the screen.
19. As the tests run, you can alter test execution conditions by selecting:
    - **`Loop`** to run the test continuously.
    - **`Pause`** to pause the tests.
    - **`Stp Fail`** (stop-on-failure) to pause the tests when a failure is detected.
    - **`Sgl Step`** (single-step) to pause the test after each measurement.

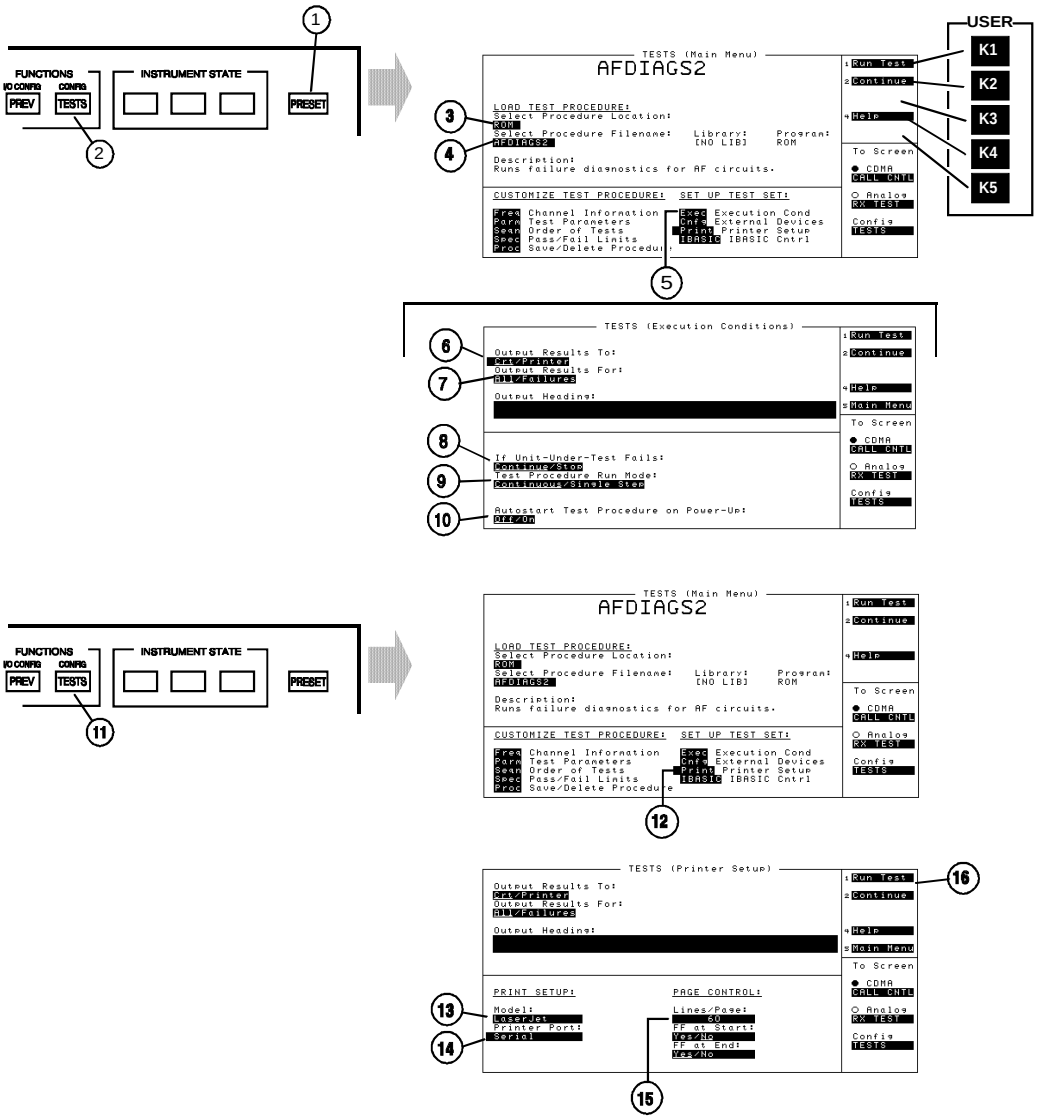


Figure 7 Running the Functional Diagnostics

If all Functional Diagnostics pass: Verify that the Test Set is functioning. Got to step 3 below.

If any Functional Diagnostic fails: **See "More About Step 2- Run the Functional Diagnostics" on page 81**.

Step 3 - Verify Test Set Functions

Suggestions:

- Run all or a selected group of the Performance Tests. See **chapter 5, "HP 8924C Performance Verification"** or .**chapter 6, "HP 8924E Performance Verification"**
- Run selected Periodic Calibration procedures. See **chapter 4, "Periodic Adjustments"**.
- Swap suspected assemblies with known-good ones. See **"Swapping Known-Good Assemblies" on page 94**.

More About Step 1- Run the Power-Up Diagnostic

If the Test Set powers up with the message:

`"All self tests passed."` it is still possible to have the following digital problems:

- Intermittent failure in any digital assembly.
- Input or output failure on any I/O port of the A14 Host Serial I/O assembly.
- Key failure (other than stuck keys) on the A1 Keyboard.

If all Self-Test Diagnostics pass, and the front-panel keys and knob work, you can assume that the digital control assemblies work.

If the Test Set powers up with the message:

`"One or more self-tests failed. Error code:<hexadecimal error code>"`:**See "Description Of Self-Test Diagnostic," in chapter 14, on page 541** for further details on troubleshooting with the Self-Test Diagnostic.

If the Test Set fails to power-up at all:

- If there is no image on the display, see **figure 8, "Troubleshooting a Blank Display," on page 80**.
- If an error message appears and remains in the *center* of the display, or if the Test Set does not respond to any keys or HP-IB commands, the Test Set may be configured to power-up to a custom procedure (rather than the default screen) and that procedure may have errors. This feature is initiated by setting **`Autostart`** to **`On`** from the TESTS (Execution Conditions) screen. To correct this fault, turn the power off, then the power on while holding down the MEAS RESET and Hz keys until an image appears on the screen. Note: *this will erase all existing programs and Save/Recall settings.*
- If the Test Set does not power-up properly, but the fan operates and the power supply voltages are correct on the Filter regulator (A20) outputs, the Host Controller (A16) may be failing. It may be possible to run the Self-Test Diagnostic and read the test results using the diagnostic LEDs on the Host Controller assembly. **See "Description Of Self-Test Diagnostic," in chapter 14, on page 541** for details.

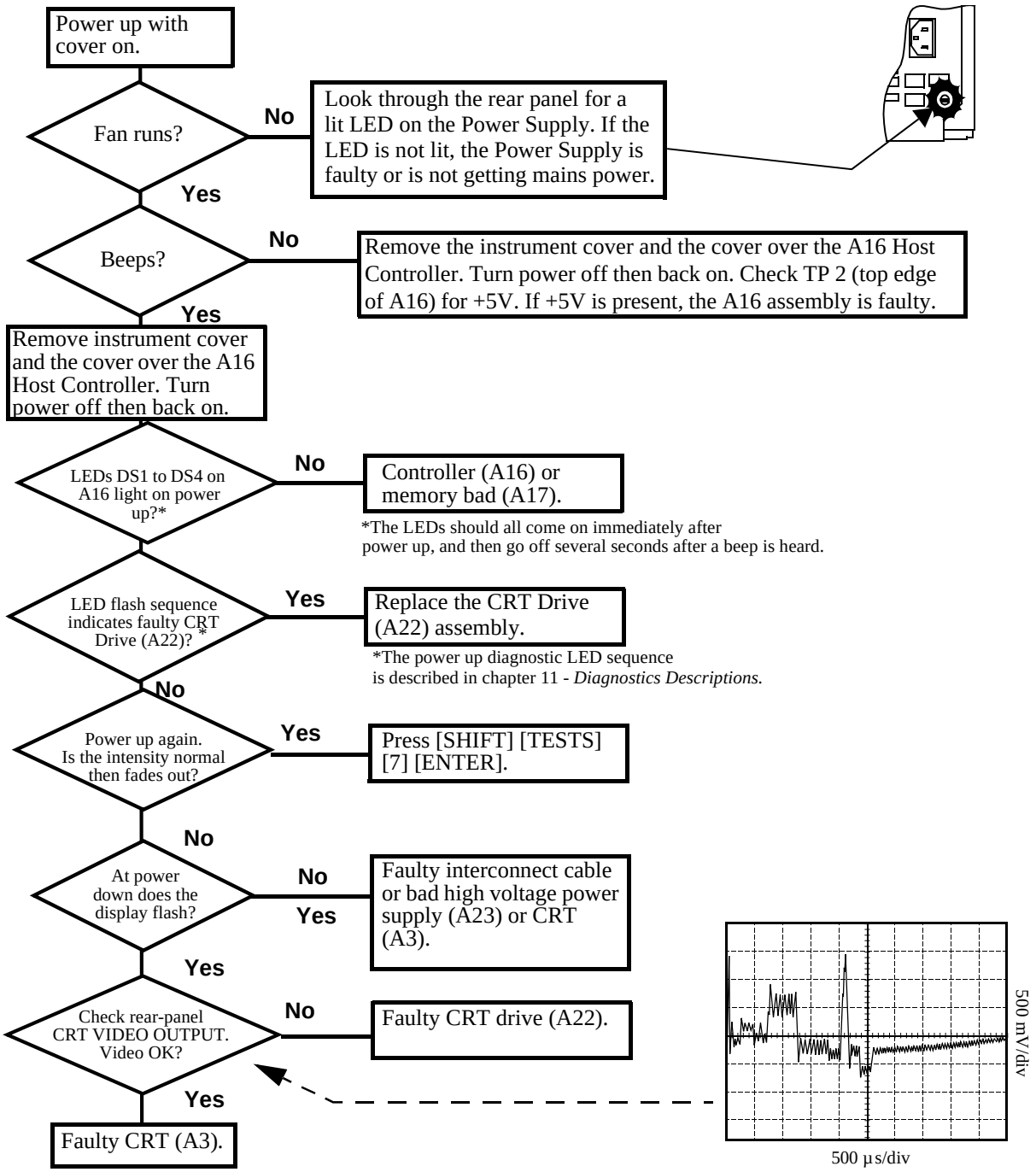


Figure 8 Troubleshooting a Blank Display

More About Step 2- Run the Functional Diagnostics

USER Keys

The numbered control fields in the upper-right corner of the TESTS screens correspond to the USER keys to the right of the screen.

Frequently Encountered Error Messages

Error messages that appear on the second line of the Test Set's display frequently occur while the Functional Diagnostics are running. The most complete and general list of error messages is in the *Error Messages* chapter of the Test Set's *User's Guide* . Some messages relating specifically to troubleshooting can be found in the *Error Messages* chapter of this manual. Some of the messages you can expect to occur while running the Functional Diagnostics are as follows:

Functional Diagnostics measurements commonly generate the message **"Direct latch write occurred. Cycle power when done servicing."** The message appears the first time the diagnostic program directly addresses a latch. The message should be ignored until you wish to make a normal (not a diagnostic) measurement with the Test Set. To clear this message the Test Set should be turned off and back on again.

The message **"Printer does not respond."** usually indicates that one or more settings on the TESTS (Printer Setup) screen are set wrong for your printer. Also, check that the printer's power is on and that it is correctly cabled. For HP-IB printers make sure the printer is correctly addressed. If a serial printer is used, you may have to change the serial communication settings on the I/O CONFIGURE screen (press SHIFT then PREV to get to this screen). The message times-out after a few seconds, and the output destination is changed to CRT by the program.

Some error messages you might encounter when running the Functional Diagnostics are the following:

"ERROR 173 IN XXXX Active/system controller req'd" (where **"XXXX"** represents a line number) indicates that the Test Set's internal IBASIC computer must be set as a system controller for some reason. This usually indicates that the **Printer Port** field of the TESTS (Printer Setup) screen was set to **HP-IB** but the **Mode** field on the I/O CONFIGURE screen is set to **Talk&Lstn** instead of **Control**. Change the mode setting to **Control** and run the diagnostic again.

Timeouts

Certain failures may cause a frequency or voltage reading to timeout, that is, the time required for the measurement will be unreasonably long. If a timeout occurs, measurement execution will stop and an error message will be displayed.

- If frequency or voltage readings have been successfully made before the timeout, the assembly currently being tested or a multiplexer on the A37 Measurement assembly may be at fault.
- If most measurements fail, the A27 Reference assembly may be faulty in supplying clock signals to the A37 Measurement assembly.
- Re-run the test to see if the timeout is intermittent.

The Four Functional Diagnostics

The Functional Diagnostics are contained in four independent program files. Before ordering a replacement assembly based on the diagnostics, you should read the descriptions of the diagnostic tests. **See chapter 14, "Diagnostics Descriptions"**. See also **chapter 11, "Block Diagrams"**.

Audio Diagnostics (AFDIAGS3)

This program tests the audio functions of the following assemblies:

- A36 Audio Analyzer 2
- A35 Audio Analyzer 1
- A34 Modulation Distribution
- A15 Signalling Source/Analyzer (AF Generators 1 and 2 only)
- A37 Measurement (only a few selected inputs)

After initial cabling, all tests can be run in a loop mode without further intervention. This makes it easier to catch intermittent failures.

NOTE: The measurement limits of the Functional Diagnostic tests are valid only at room temperature; that is, 20 to 25°C or 65 to 75°F.

When a test fails, a diagnosis is given in three parts:

- A diagnostic code.
- The name of the assembly or assemblies most likely to have failed.
- A rating (high, medium, or low) of the confidence of the diagnosis.

Before ordering an assembly based on the diagnosis, you should read the description of the diagnostic test and details of the diagnosis based on the diagnostic code. **See chapter 14, "Diagnostics Descriptions"**. See also **chapter 11, "Block Diagrams"**.

RF Diagnostics (RFDIAGS3)

This program tests the RF functions of the following assemblies:

- A19 Receiver 1st Mixer
- A26 Output
- A24 Signal Generator Synthesizer
- A27 Reference
- A30 Receiver
- A28 Receiver Synthesizer
- A32 Spectrum Analyzer
- A5 Input

Some tests require cabling before the RF Diagnostics can be run; but all tests can be run in a loop mode without further intervention. Running in loop mode makes it easier to catch intermittent failures.

NOTE: The measurement limits of the Functional Diagnostic tests are valid only at room temperature; that is, 20 to 25°C or 65 to 75°F.

When a test fails, a diagnosis is given in two parts:

- The name of the assembly or assemblies most likely to have failed.
- A rating (high, medium, or low) of the confidence of the diagnosis.

The diagnosis given by the RF Diagnostics should be verified by other means before ordering and replacing parts. This particularly applies to the Spectrum Analyzer, Receiver, and Receiver Mixer assemblies. Some suggestions for doing this are as follows:

- Become familiar with the block diagram and theory of operation of the assemblies in **chapter 11, "Block Diagrams"**.
- Read the description of the diagnostic test in **chapter 14, "Diagnostics Descriptions"**.
- Follow the suggestions in **"Further Isolating RF Failures" on page 96** later in this chapter.

Miscellaneous Diagnostics (MSDIAGS3)

This program verifies the following:

- The ability of the A27 Reference to detect the presence of the A29 CDMA Reference signal and its ability to lock to that signal.
- The integrity of the front-panel RF IN/OUT, DUPLEX OUT, and ANT IN connectors.
- The Self-Test Diagnostics, and power supply voltages. The Self-Test Diagnostics are described in detail in **"Description Of Self-Test Diagnostic" on page 541**.
- Serial bus communication

The Miscellaneous Diagnostics cannot be run in a loop mode.

CDMA Diagnostics (CDMADIAG)

This program tests the following parameters:

- CDMA Reference (A29): 20MHz VCXO tune voltage and phase-lock status, 19.6608MHz VCXO tune voltage and phase-lock status, and AWGN (noise) source's status.
- LO/IF Demod (A31): 117.9864MHz local oscillator (LO) bias and tune voltage, 3.686MHz IF sense, 114.3MHz IF sense, Spectrum Analyzer path sense, supply voltages references, and IQ Demodulator LO tune voltage and sense.
- IQ Modulator (A25): RF Input detection, IQ output detection, baseband I and Q detection, I signal gain, various modulator control levels.
- Cell Site Analog (A8): Cell Site 1&2 video DAC references, Cell Site 1 I and Q gain control DAC voltage, I and Q summing amplifier outputs.

Troubleshooting Aids

Refer to following table to determine which Diagnostic Tests, Performance Tests, and Periodic Self Calibration Adjustments apply to an assembly. Downloading calibration data is discussed in **chapter 3, "Repair," on page 101**.

Table 4 Relating Assemblies To Troubleshooting Aids

Ref. Des.	Assembly Name	Troubleshooting with Diagnostics (Chapter 2)		Performance Verification (Chapter 5)	Periodic Adjustments Cal (Chapter 4)	Cal-Data Needed After Repl ?
		Power-Up Self Tests [a]	ROM			
A1	Keyboard	X	MS DIAGS3: (Self Test)			No
A2	Keyboard Filters					No
A3	CRT					No
A4	Attenuator		MS DIAGS3: (RF In/Out)			Yes
A5	Input		RF DIAGS3: (Input)	RF Generator (Level Accuracy)	Receiver Mixer[b] Attenuator Generic Cable	Yes
A6	Protocol Processor	X	MS DIAGS3: (Self-Test)			No
A7	Cell Site Digital 2	X	MS DIAGS3: (Self_Test)		PCB_CAL	No
A8	Cell Site Analog		CDMADIAG (Cell Site)		Power Sensor Zero PCB_CAL	Yes
A9	Cell Site Digital 1	X	MS DIAGS3: (Self Test)		PCB_CAL	No
A10	Vocoder (Option)					
A11	DSP Receiver (Optional)					No
A12	DSP Receiver					No

Table 4 Relating Assemblies To Troubleshooting Aids (Continued)

Ref. Des.	Assembly Name	Troubleshooting with Diagnostics (Chapter 2)		Performance Verification (Chapter 5)	Periodic Adjustments Cal (Chapter 4)	Cal-Data Needed After Repl ?
		Power-Up Self Tests [a]	ROM			
A14	Host Serial I/O Interface	X	MS DIAGS3: (Self Test)			No
A15	Signaling Source/Analyzer	X	AF DIAGS3: (Audio Frequency Generators 1 and 2)			No
A16	Host Controller	X	MS DIAGS3: (Self Test)			No
A17	Memory	X	MS DIAGS3: (Self Test)			No
A19	Receiver 1st Mixer		RF DIAGS3: (Receiver)		Receiver Mixer	Yes
A20	Filter/ Regulator		MS DIAGS3: (Self-Test)			No
A21	Fan					No
A22	CRT Drive	X	MS DIAGS3: (Self Test)			No
A23	Power Supply Connections		MS DIAGS3: (Self Test)			No
A24	Signal Generator Synthesizer		RF DIAGS3: (Signal Generator Synthesizer)	RF Generator: (Harmonic and Spurious Spectral Purity)		Yes
A25	I/Q Modulator		CDMADIAG (I/Q Mod)		I/Q Mod PCB_CAL	Yes

Table 4 Relating Assemblies To Troubleshooting Aids (Continued)

Ref. Des.	Assembly Name	Troubleshooting with Diagnostics (Chapter 2)		Performance Verification (Chapter 5)	Periodic Adjustments Cal (Chapter 4)	Cal-Data Needed After Repl ?
		Power-Up Self Tests [a]	ROM			
A26	Output		RF DIAGS3: (Output)	AF Generator: (AM Accuracy)	Attenuator Generic Cable	Yes
A27	Reference		RF DIAGS3: (Reference)	RF Generator: (Residual FM)	Timebase Reference	Yes
A28	Receiver Synthesizer		RF DIAGS3: (Receiver Synthesizer)	RF Analyzer: (Residual FM)		Yes
A29	CDMA Reference		CDMADIAG (CDMA Ref.)		Power Sensor Zero PCB_CAL	Yes
A30	Receiver		RF DIAGS3: (Receiver)	RF Analyzer: (AM Accuracy and FM Accuracy)	Receiver Mixer	Yes
A31	LO/IF Demod		CDMADIAG (LO/IF Demod)		Receiver Mixer	No
A32	Spectrum Analyzer (8924E Option)		RF DIAGS3: (Spectrum Analyzer)	Spectrum Analyzer	Receiver Mixer	Yes
A33	Control Interface	X	MS DIAGS3: (Self Test)			Yes
A34	Modulation Distribution		AF DIAGS3: (Mod Distribution Internal Paths)	AF Generator: (AC Level Accuracy)	AF Gen Gain EXT Mod Path Gain Audio Analyzer Offset	No
A35	Audio Analyzer 1		AF DIAGS3: (Audio Ana-lyzer 1 Inter-nal Paths)		Audio Analyzer Offset	No

Table 4 Relating Assemblies To Troubleshooting Aids (Continued)

Ref. Des.	Assembly Name	Troubleshooting with Diagnostics (Chapter 2)		Performance Verification (Chapter 5)	Periodic Adjustments Cal (Chapter 4)	Cal-Data Needed After Repl ?
		Power-Up Self Tests [a]	ROM			
A36	Audio Analyzer 2		AF DIAGS3: (Audio Analyzer 2)	AF Analyzer: (AC Voltage Accuracy)	VFN (a must)	Yes
A37	Measurement [c]	X	MS DIAGS3: (Self Test)	Oscilloscope	Voltmeter Reference	Yes
A38	Oven Oscillator				Timebase Adjust	No
A39	37-Pin Filter					No
A40	Motherboard					No

a. Besides checking the assemblies marked X, the power-up self test checks the serial data lines which the controller uses to send control signals to and receive status signals from the RF and AF assemblies.
b. HP 8924E: Required if Spectrum Analyzer is installed.
c. Measurement checked indirectly by all diagnostics.

More about Step 4 - Verify Test Set Functioning

See "Locating the Out-Of-Lock (OOL) Indicators" on page 89

Out-of-lock (OOL) LEDs light when a phase-locked loop inside an assembly is failing. The Signal Generator Synthesizer (A24), Receiver Synthesizer (A28), CDMA Reference (A29), and LO/IF Demod (A31) assemblies have these LEDs mounted close to the top of the modules. The location of each LED is labeled on the assembly.

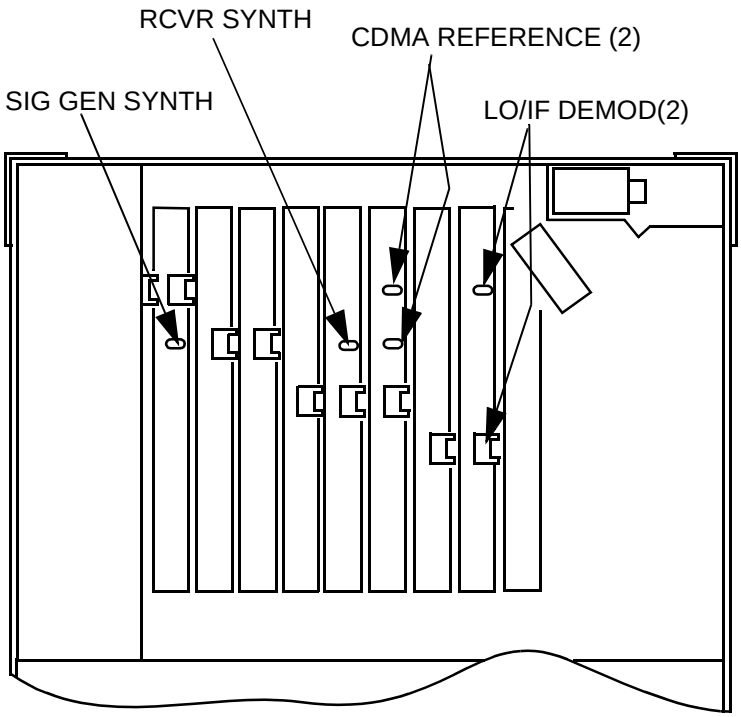


Figure 9 **Locating the Out-Of-Lock (OOL) Indicators**

Isolating Out-of-Lock Conditions

If more than one OOL indicator is lit.

CDMA Reference and LO/IF Demod: If the CDMA Reference is unlocked, the LO/IF Demod assembly will be unlocked, since its reference comes from the CDMA Reference. Verify that the CDMA Reference (A29) is working correctly before troubleshooting the LO/IF Demod assembly.

Receiver Synthesizer and Signal Generator Synthesizer: If both assemblies are unlocked, the Reference (A27) is the probable cause, since it provides the reference for both assemblies.

CDMA Reference (A29) Unlocked

1. Verify that the rear-panel 10 MHz Oven Out signal is at 10 MHz, and at a level of 0 dBm ±3 dB into 50 Ω.
2. Connect a BNC cable between the 10 MHz Oven Out and REF IN ports.
3. Press the SHIFT key, then press the TESTS key to access the CONFIGURE screen.
4. Set the **`External Reference`** field to **`10.0000 MHz`** (if not already set).
5. If the OOL indicator is lit on the CDMA Reference (A29) assembly, replace the assembly and re-test.

.

LO/IF Demod (A31) Unlocked

This assembly is phase-locked to a signal from the CDMA Reference. If the CDMA Reference is out-of-lock, troubleshoot that assembly first before proceeding.

1. Turn the Test Set off.
2. Remove the rear assemblies cover (two assembly pry tools are removed in the process).
3. Use the pry tools to remove the LO/IF Demod assembly.
4. Turn the Test Set on.
5. Verify that a 10 MHz signal of about 0 dBm is present on pin 19 of J72. This is the reference signal from the CDMA Reference assembly.
6. If the signal is present, replace the LO/IF Demod assembly.

   If the 10 MHz signal is not present, an open or shorted trace on the Motherboard assembly (A40) may be the cause. Check for continuity between J72 pin 19 (under the LO/IF Demod assembly) and J69 pin 19 (under the CDMA Reference assembly), and verify that the trace is not shorted to ground.

Receiver Synthesizer (A28) Unlocked

1. Turn the Test Set off.
2. Remove the rear assemblies cover (two assembly pry tools are removed in the process).
3. Use the pry tools to remove the Receiver Synthesizer assembly.
4. Turn the Test Set on.
5. Verify that a 1 MHz signal of about - 1 dBm is present on pin 3 of J40. This is the reference signal from the Reference assembly.
6. If the signal is present, replace the Receiver Synthesizer assembly.

   If the 1 MHz signal is not present, the Reference (A27) assembly is probably faulty. It is also possible that an open or shorted trace on the Motherboard assembly (A40) exists. Check for continuity between J40 pin 3 (under the Receiver Synthesizer) and J34 pin 2 (under the Reference assembly), and verify that the trace is not shorted to ground.

Signal Generator Synthesizer (A24) Unlocked

1. Turn the Test Set off.
2. Remove the rear assemblies cover (two assembly pry tools are removed in the process).
3. Use the pry tools to remove the Receiver Synthesizer assembly.
4. Turn the Test Set on.
5. Verify that a 1 MHz signal of ≥ –20 dBm is present on pin 3 of J31. This is the reference signal from the Reference assembly.
6. If the signal is present, replace the Signal Generator Synthesizer assembly.

   If the 1 MHz signal is not present, the Reference (A27) assembly is probably faulty. It is also possible that an open or shorted trace on the Motherboard assembly (A40) exists. Check for continuity between J31 pin 3 (under the Signal Generator Synthesizer) and J34 pin 1 (under the Reference assembly), and verify that the trace is not shorted to ground.

Swapping Known-Good Assemblies

Swapping a known-good assembly for a suspected faulty assembly performed Most swapped assemblies which use calibration data will operate well enough with the original assembly's calibration data to troubleshoot and to run the diagnostics; do not expect the Test Set to meet its specifications. Some assemblies may appear to fail because of incorrect calibration data. It is also important to keep track of the original assemblies in the Test Set. If calibration data is lost, the assembly will have to be sent back to the factory.

Calibration data is generally stored in a socketed EEPROM on the A16 Host Controller. If the controller is replaced or swapped, the original EEPROM must be put in the new Test Set's Controller. Should the EEPROM lose its data, the entire instrument will require a factory recalibration.

The assemblies that require down-loaded calibration data from a memory card are:

- A19 Receiver 1st Mixer
- A26 Output
- A24 Signal Generator Synthesizer
- A27 Reference
- A30 Receiver
- A28 Receiver Synthesizer
- A32 Spectrum Analyzer (optional in some Test Sets)
- A37 Measurement
- A33 HP-IB/RS-232/Current Sense
- A5 Input
- A4 Attenuator

Of these assemblies the A5 Input is the least likely candidate for a successful assembly swap.

The A32 Spectrum Analyzer may also pose difficulties. To verify operation, first set the Spectrum Analyzer's **`RF Gen`** controls to **`Track`**, and the **`Port/Sweep`** field to **`Dupl`**. This directs the Tracking Generator to the DUPLEX OUT port. Connect the DUPLEX port to the ANT IN port. Set the **`Main`** control to **`Ant`**. Set the **`Center Freq`** to 501 MHz, and the **`Span`** to 1 GHz. You should see a (roughly) flat line across the screen, varying about 4dB. "**`Generator sweep truncated`**" may appear - but does not indicate a problem.

Some assemblies require that a periodic calibration procedure be run. These are:

- A36 Audio Analyzer 2 (variable-frequency notch filter null if present)
- A35 Audio Analyzer 1 (DC offset)
- A34 Modulation Distribution (DC offset, external amplifier gain)
- A27 Reference (time base frequency)
- A37 Measurement (voltage references)
- A29 CDMA Reference
- A31 LO/IF Demod
- A25 IQ Modulator
- A8 Cell Site Analog

For general troubleshooting, these assemblies can generally be swapped without an immediate need of recalibration.

Further Isolating RF Failures

Isolating failures in the RF assemblies of the Test Set can be difficult. One problem is that the RF Diagnostics sometimes use the built-in RF analyzer to test the built-in RF source, and vice versa. This is necessary to make the diagnostics self-contained, that is, they run without external equipment.

Before using the helps in this section, run all of the RF Diagnostics (**see "More About Step 2- Run the Functional Diagnostics," in chapter 2, on page 81**) It will also be helpful to become familiar with:

- the RF source and analyzer block diagrams and theory of operation in **chapter 11, "Block Diagrams"**
- the description of the RF and Miscellaneous Diagnostic tests in **chapter 14, "Diagnostics Descriptions"**.

Some general-purpose, RF test equipment will be needed:

- RF signal generator
- RF modulation analyzer or spectrum analyzer.

Isolating Input and Output Failures

If all RF diagnostic tests pass, there could still be a problem with the input and output paths (including reverse-power and overpower protection). Run the Miscellaneous Diagnostics test titled RF Input Output Test. A failure indicates that the input section or front-panel connection is faulty.

Isolating the RF Analyzer

The RF Analyzer function uses the following assemblies. (Refer to block diagrams in **chapter 11, "Block Diagrams"**.)

- A5 Input
- A19 Receiver First Mixer
- A30 Receiver 1st
- A28 Receiver Synthesizer
- A32 Spectrum Analyzer
- A29 CDMA Reference and A27 Reference (for downconversion).

To isolate an RF Analyzer problem:

- On the Test Set:
  - Press PRESET.
  - Press the SHIFT key, then press the TESTS key to access the CONFIGURE screen.
    - r Set the **RF Display** field to **Freq**.
    - r Set the **RF Offset** field to **Off**.
  - Locate the ANLG SCRNS (Analog Screens) group of keys and press the TX TEST key (to go to the analog TX TEST screen).
    - r Set the **Tune Mode** to **Auto** . This enables the Test Set to automatically tune the receiver to a strong RF signal.
    - r Set the **Input Port** to **RF IN**.
- On the external RF signal generator:
  - Set the frequency to 100 MHz CW.
  - Set the amplitude to 0 dBm.
  - Connect the output to the Test Set's RF IN/OUT connector.
- Set the RF signal generator frequency to 100, 500, and 900 MHz. For each frequency, the Test Set's measurements should read as follows:
  - TX POWER should read approximately 0.001 W for each frequency.
  - TX FREQUENCY should read 100, 500, and 900 MHz respectively.
  - Press the SHIFT key, then press the RF GEN key to access the analog Spectrum Analyzer. Observe the level and frequency of the signal. Press PREV to return to the TX TEST screen.

Refer to the block diagrams in **chapter 11, "Block Diagrams"**. The down conversion frequencies for the three input frequencies are shown in the following table.

Table 5 Deriving Output Frequencies

Input Frequency (MHz)	First LO Frequency (MHz)	IF From First Mixer (MHz)
100	714.3	614.3
500	614.3	114.3
900	785.7	114.3

Isolating the RF Source

The RF Generator function uses the following assemblies. Refer to the block diagrams in **chapter 11, "Block Diagrams"**.

- A27 Reference and A29 CDMA Reference
- A24 Signal Generator Synthesizer
- A26 Output
- A5 Input

To isolate the RF Source:

- On the Test Set:
  - Press PRESET.
  - Press the SHIFT key, then press the TESTS key to access the CONFIGURE screen.
    - r Set the **RF Display** field to **Freq**.
    - r Set the **RF Offset** field to **Off**.
  - Locate the ANLG SCRNS group of keys and press the RX TEST key (to go to the analog RX TEST screen).
  - Set **RF Gen Freq** to **600 MHz**.
  - Set **Amplitude** to **0 dBm**.
  - Set **Output Port** to **Dupl**.
- On the external RF modulation analyzer or spectrum analyzer:
  - Set the tuning for a 600 MHz, 0 dBm input signal.
  - Connect the analyzer's input to the Test Set's DUPLEX OUT connector.
- Set the Test Set's **RF Gen Freq** to 600, 300, and 150 MHz. For each frequency, the external RF analyzer should read as follows:
  - Power should read approximately 0.001 W for each frequency.

`Frequency should read 600, 300, and 150 MHz respectively.`

3

Repair

This chapter contains information needed to remove and replace assemblies in the Test Set. Some assemblies require calibration data to be downloaded when replaced (**see "Downloading Calibration Data" on page 103**).

Before You Start

CAUTION: Perform the following procedures only at a static-safe work station. The printed circuit assemblies in this instrument are sensitive to STATIC ELECTRICITY DAMAGE. Wear an anti-static wrist strap that is connected to earth ground.

Recommended Torque

- Screws: Tighten until just snug. Do not to strip threads.
- RF connectors
  SMA: 9.0 lb-in. (102 N-cm)
  SMC: 6.0 lb-in. (68 N-cm)

Tools

One or more of the following tools may be required to access and remove Test Set's assemblies.

- TX-10 Torx screwdriver
- TX-15 Torx screwdriver
- Flat-blade screwdriver
- 7-mm socket wrench
- 1/16-inch allen wrench
- 3/16-inch socket wrench
- 1/4 -inch open-end wrench
- 5/16-inch open-end wrench

Ordering Replacement Parts

Lists of replaceable parts and part ordering information are provided in - **See chapter 12, "HP 8924C Replaceable Parts"** or **see chapter 13, "HP 8924E Replaceable Parts"**.

Downloading Calibration Data

Most assemblies in the Test Set require calibration data. To ensure that the Test Set remains calibrated after an assembly is replaced, new calibration data must be downloaded. When required, calibration data is provided on a PCMCIA memory card that is included with the replacement assembly. Refer to **table 4, "Relating Assemblies To Troubleshooting Aids" on page 85**, to see which modules require calibration data.

Calibration Data Download Procedure

1. Switch the Test Set's power off.
2. Remove the faulty assembly.
3. Install the replacement assembly.
4. Switch the Test Set's power on.
5. Insert the memory card.
6. Press the TESTS key.
7. Set the **`Select Procedure Location`**: field to **`Card`**.
8. Set the **`Select Procedure Filename`**: field to: **`DNLDCAL`**.
9. Press the K1 key to run the test.
10. Follow the instructions on the screen.

Locating Assemblies

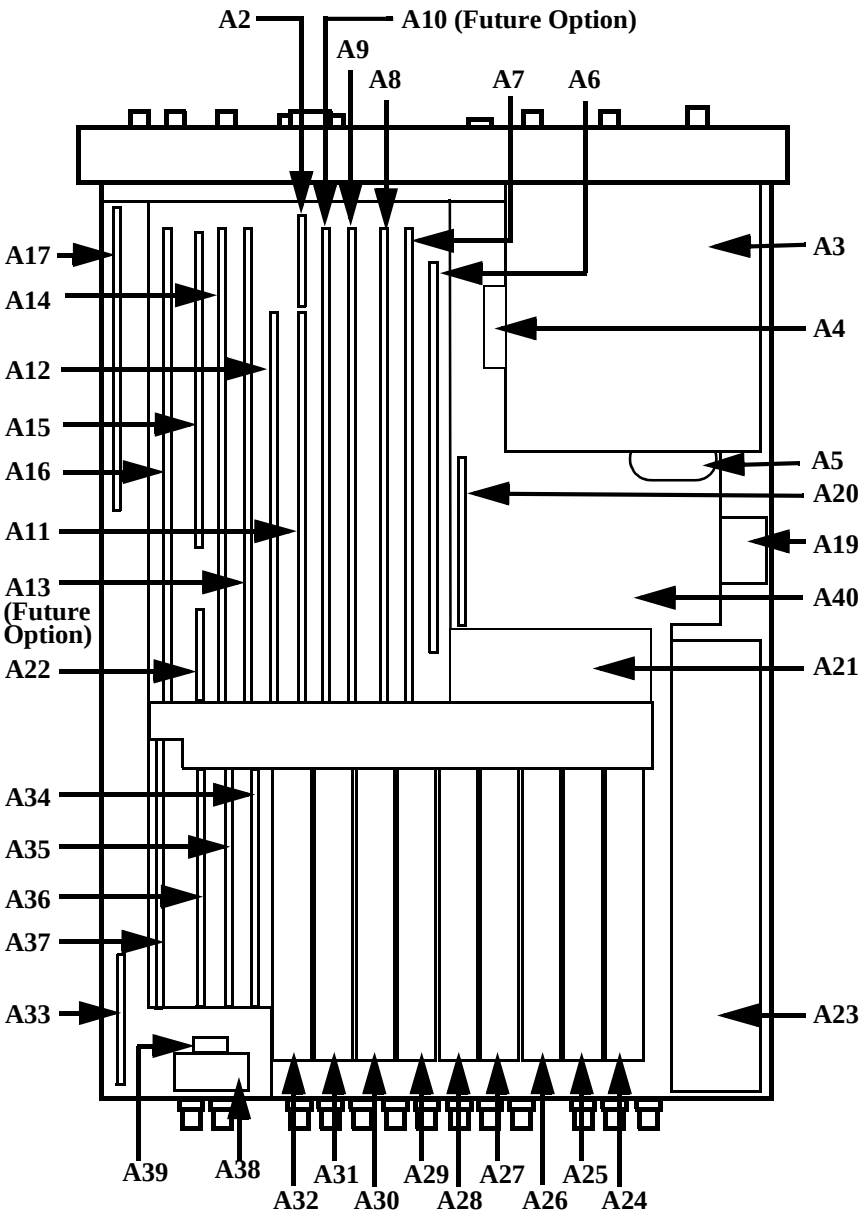
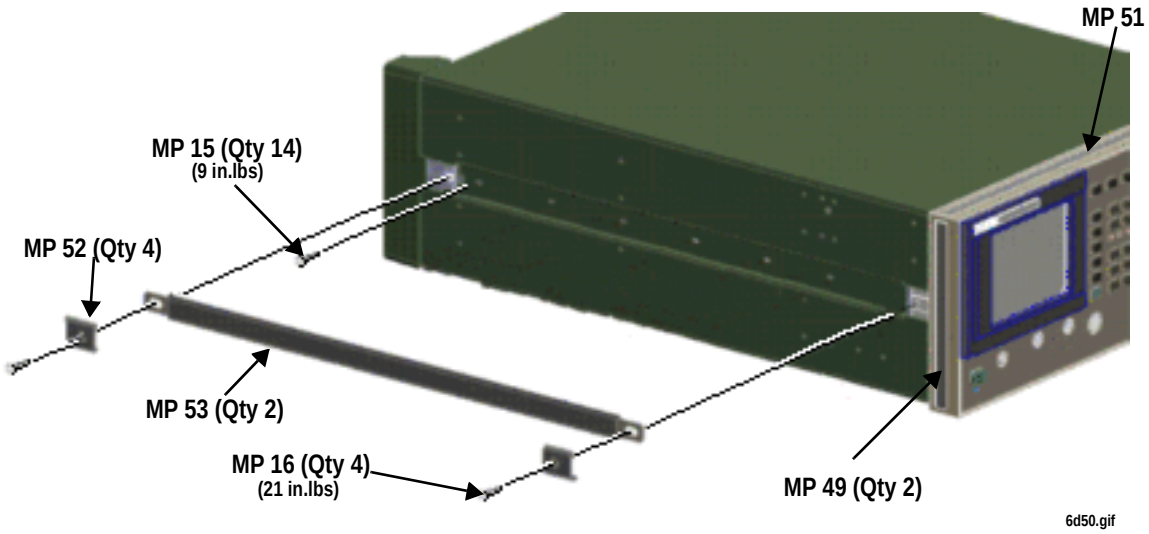


Figure 10 **Locating Assemblies**

Disassembly and Replacement Procedures

Removing the External Covers



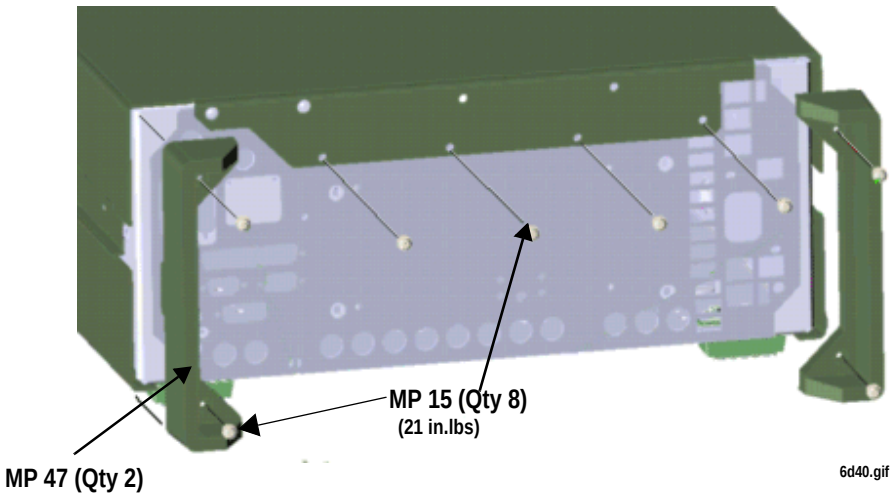


Figure 11 **Removing the External Cover**

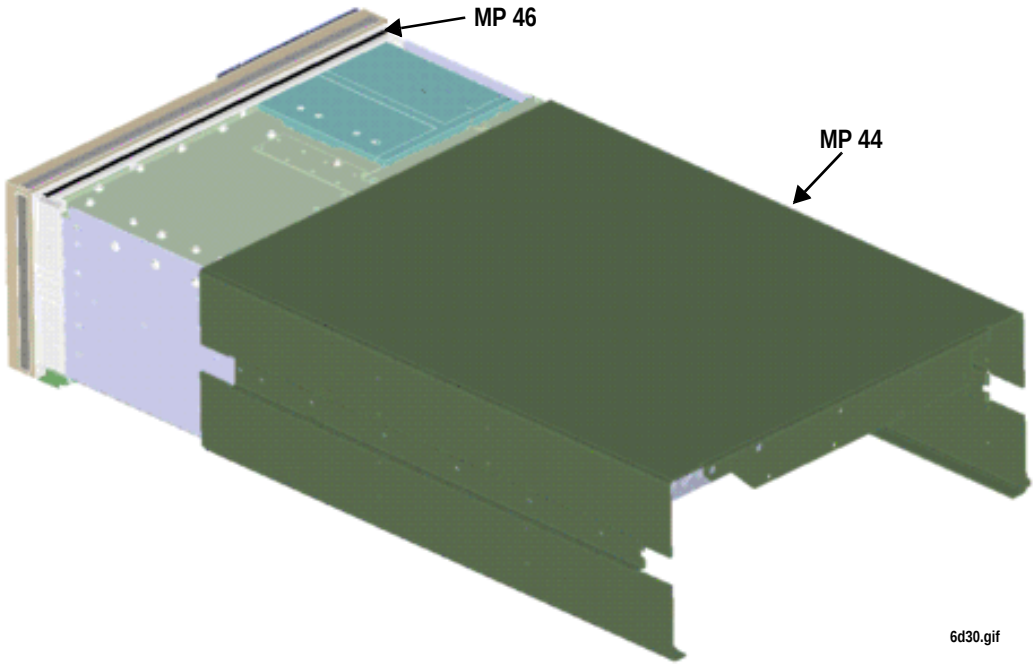


Figure 12 Removing the Instrument Cover

Removing the Front Panel Assembly: A1, A2, A3, A4, and A5

The front panel assembly consists of the Keyboard (A1), Keyboard Filters (A2), CRT (A3) Attenuator (A4), and the Input assembly (A5). The entire front-panel assembly must be removed before any of the sub-assemblies can be removed.

The general procedure is:

1. Remove the Power Supply Cover.
2. Disconnect cable W10 from the Output assembly (A26).
3. Disconnect W3 on the Receiver 1st Mixer (A19).
4. Disconnect W7 from the Front Panel Assembly (A41).
5. Remove the four screws attaching the front frame to the chassis, and move the frame slightly forward (to provide room to access Motherboard cables).
6. Disconnect W1, W5, W6, MP20, MP21, and MP22 from the Motherboard (A40).
7. Carefully slide the front frame assembly forward until the keyboard cable (W26) can be disconnected from the chassis bulkhead connector.

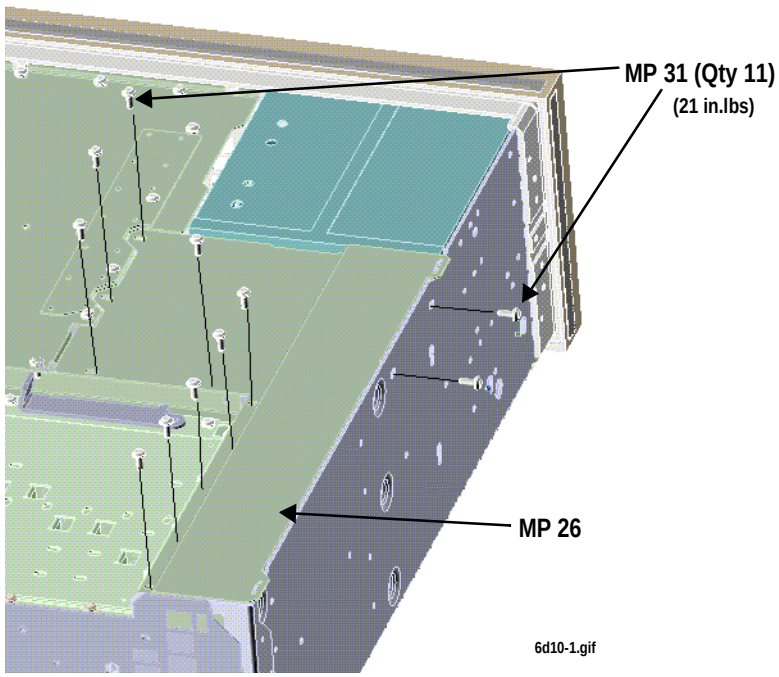


Figure 13 **Removing the Power Supply Cover**

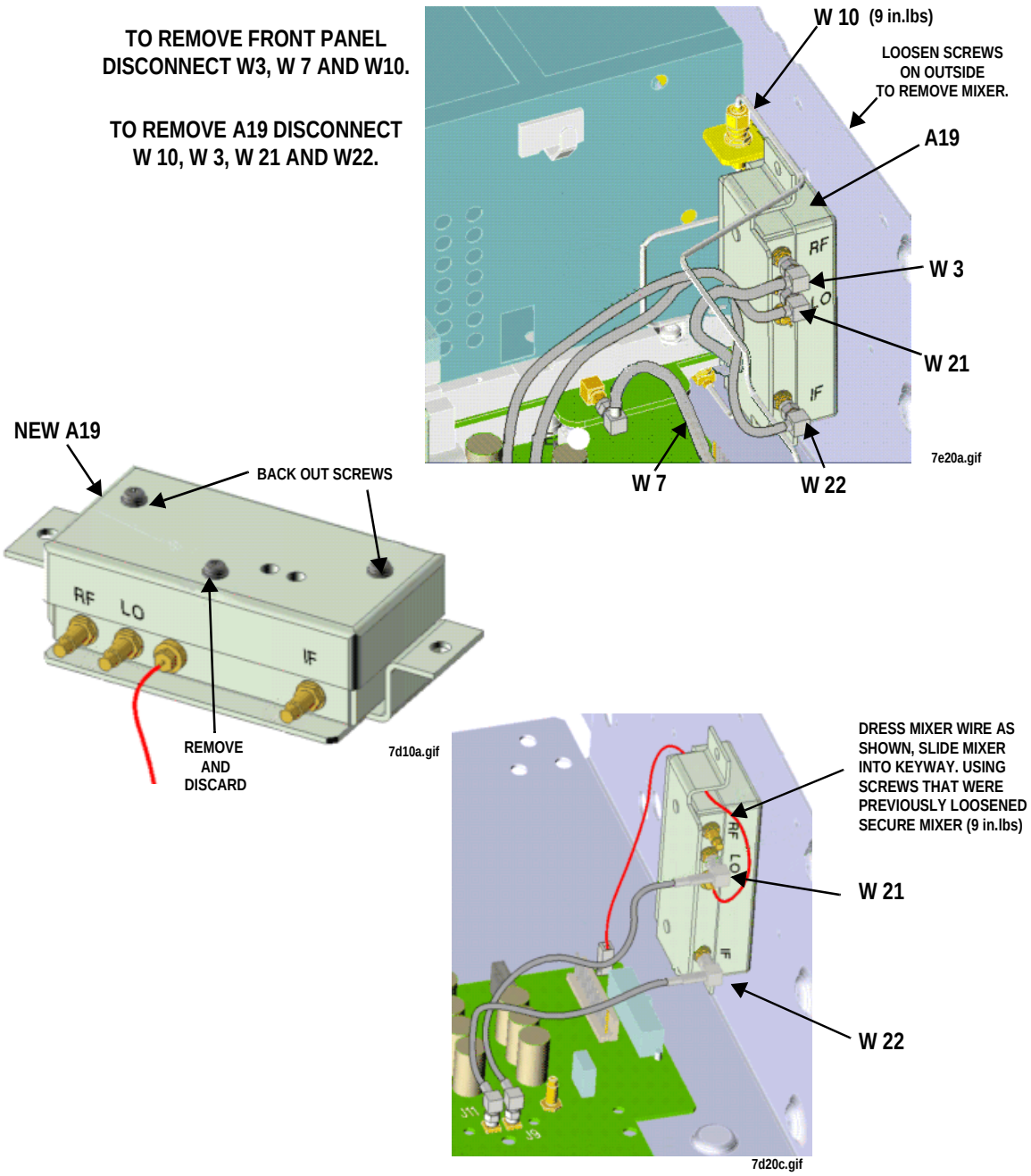
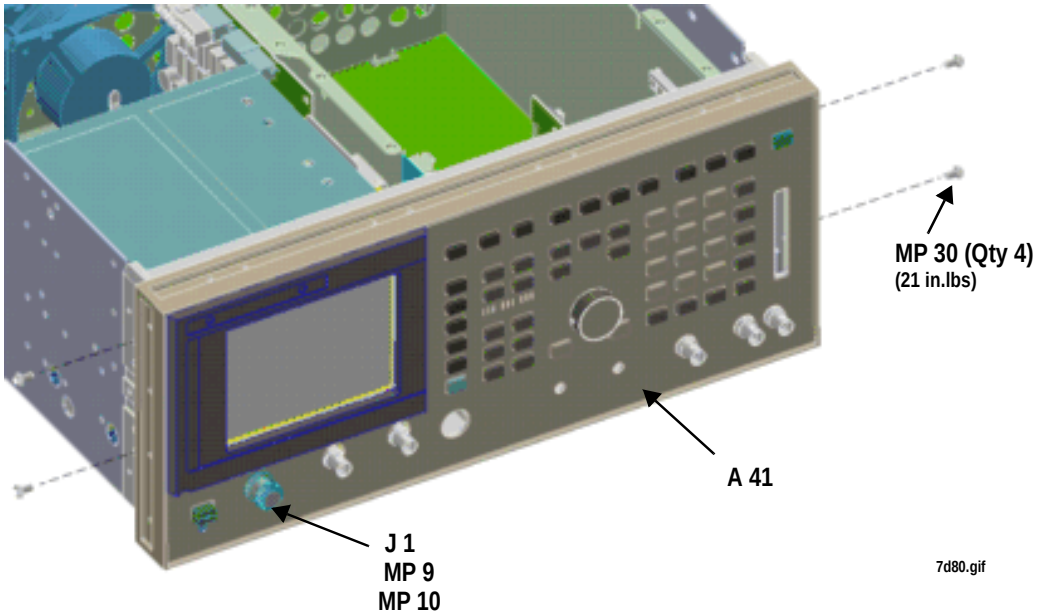


Figure 14 **Cable Connections to A19**



DISCONNECT MP20-22, W1, W5, AND W6 FROM MOTHERBOARD (W60).

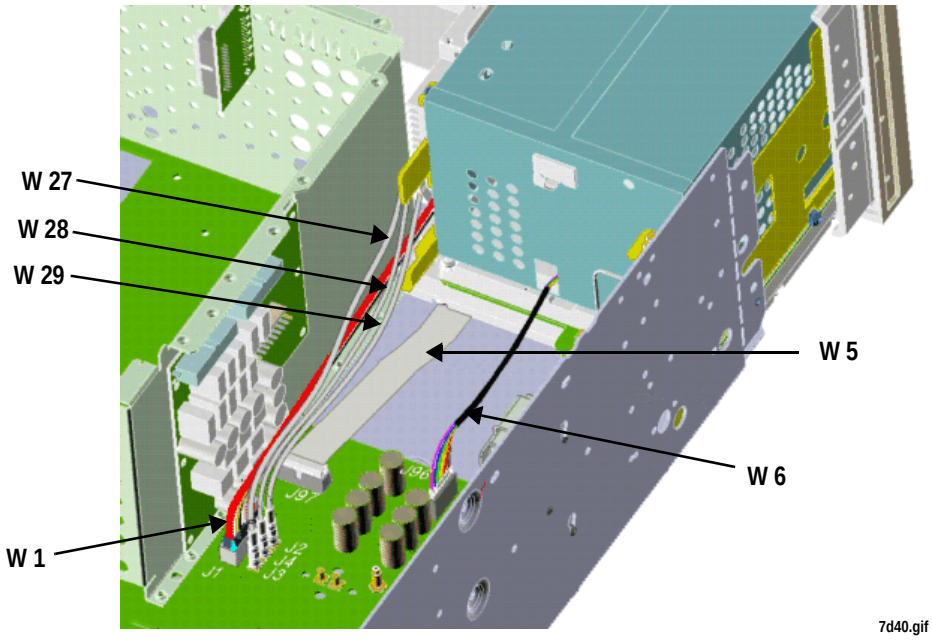


Figure 15 Front Panel Assembly Connections

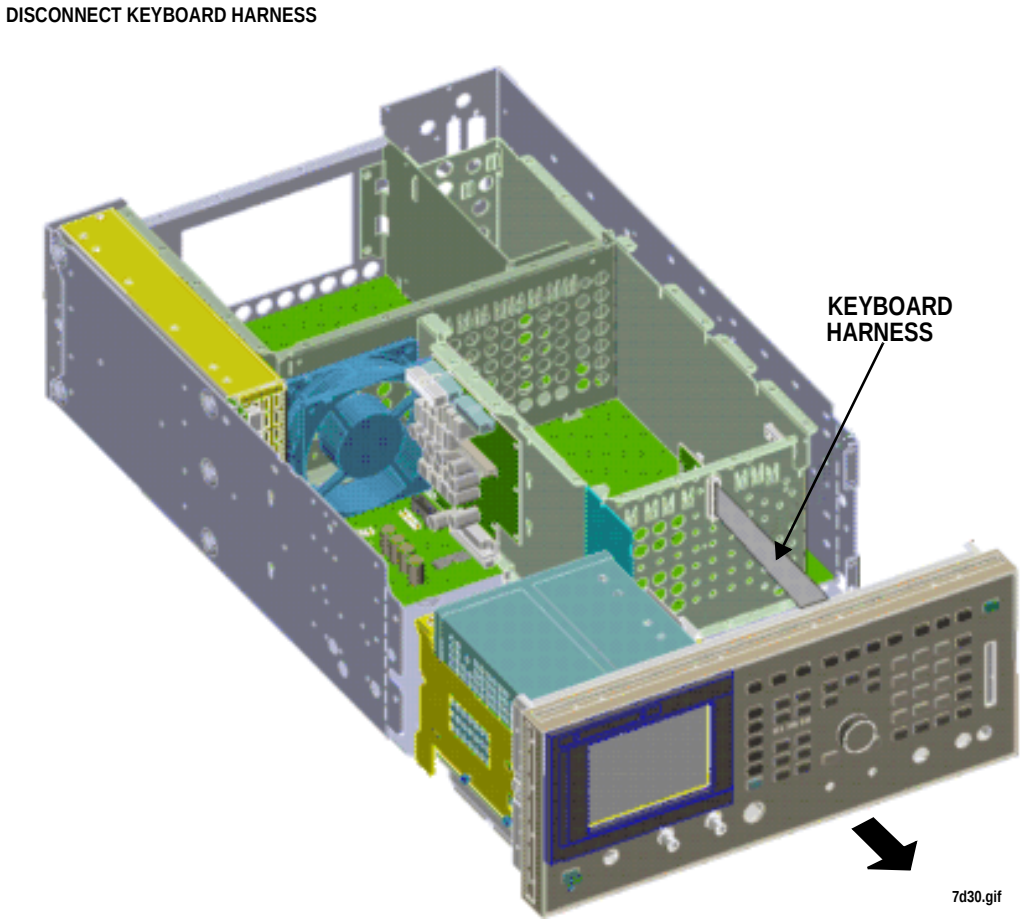


Figure 16 Keyboard

Replacing Keyboard Filter Assembly (A2)

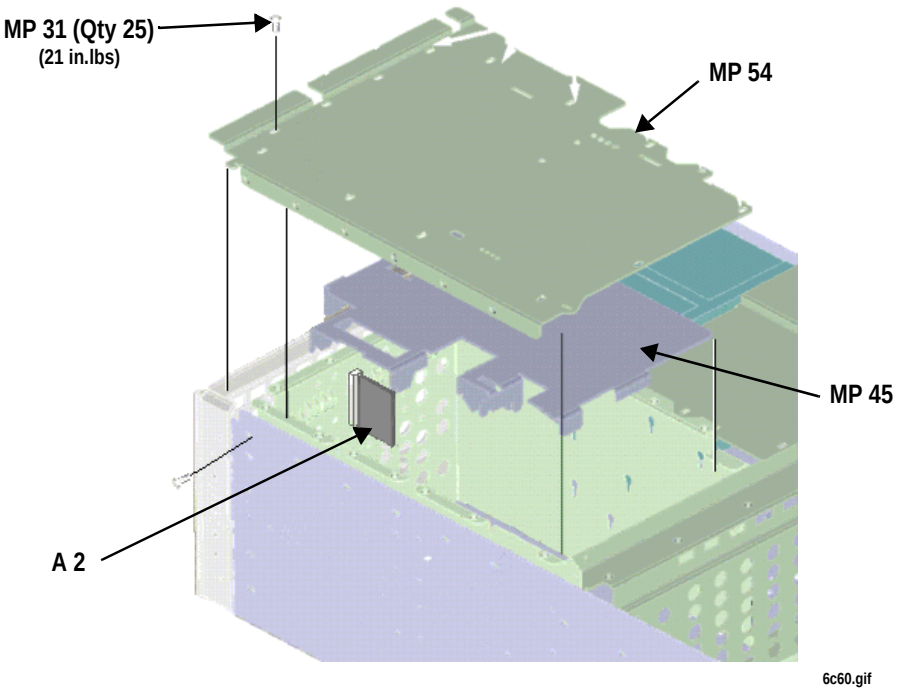
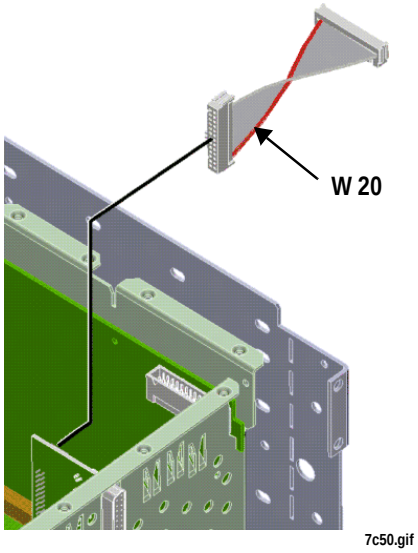


Figure 17 Keyboard Cable Connections



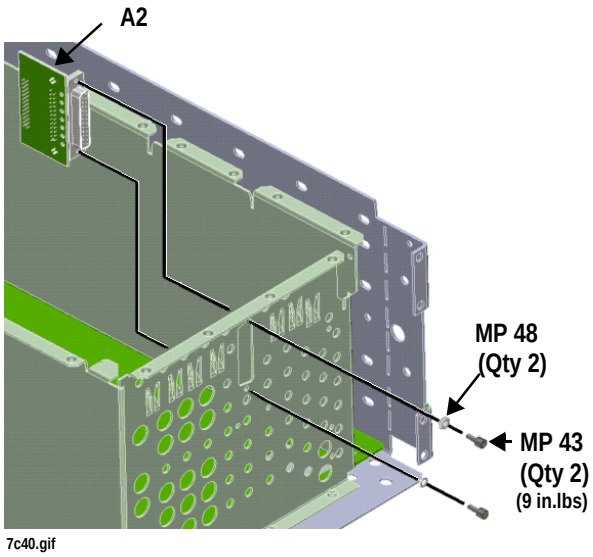


Figure 18 **Keyboard Filter Replacement (A2)**

Front Panel Disassembly

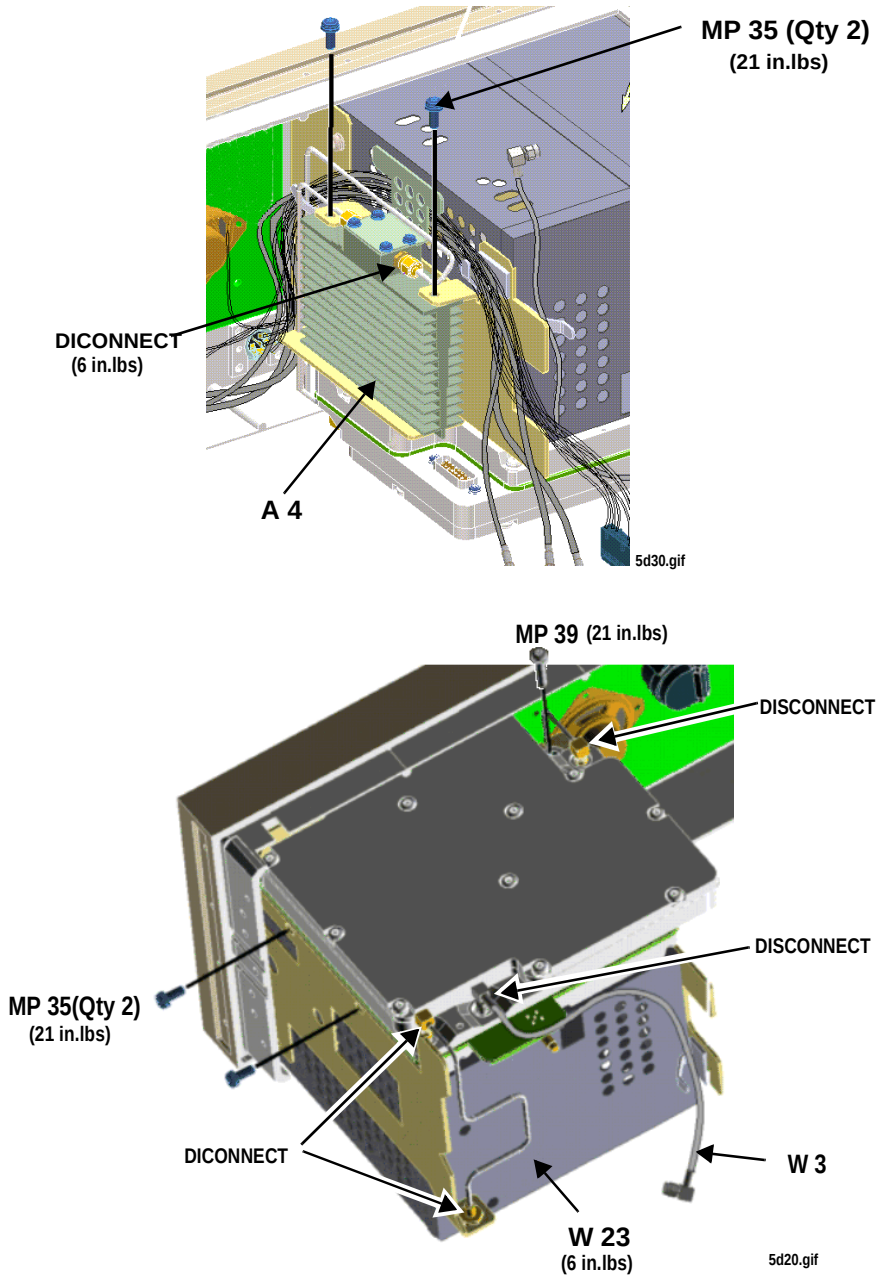


Figure 19 **Disconnecting A4 and A5 From the Front Frame**

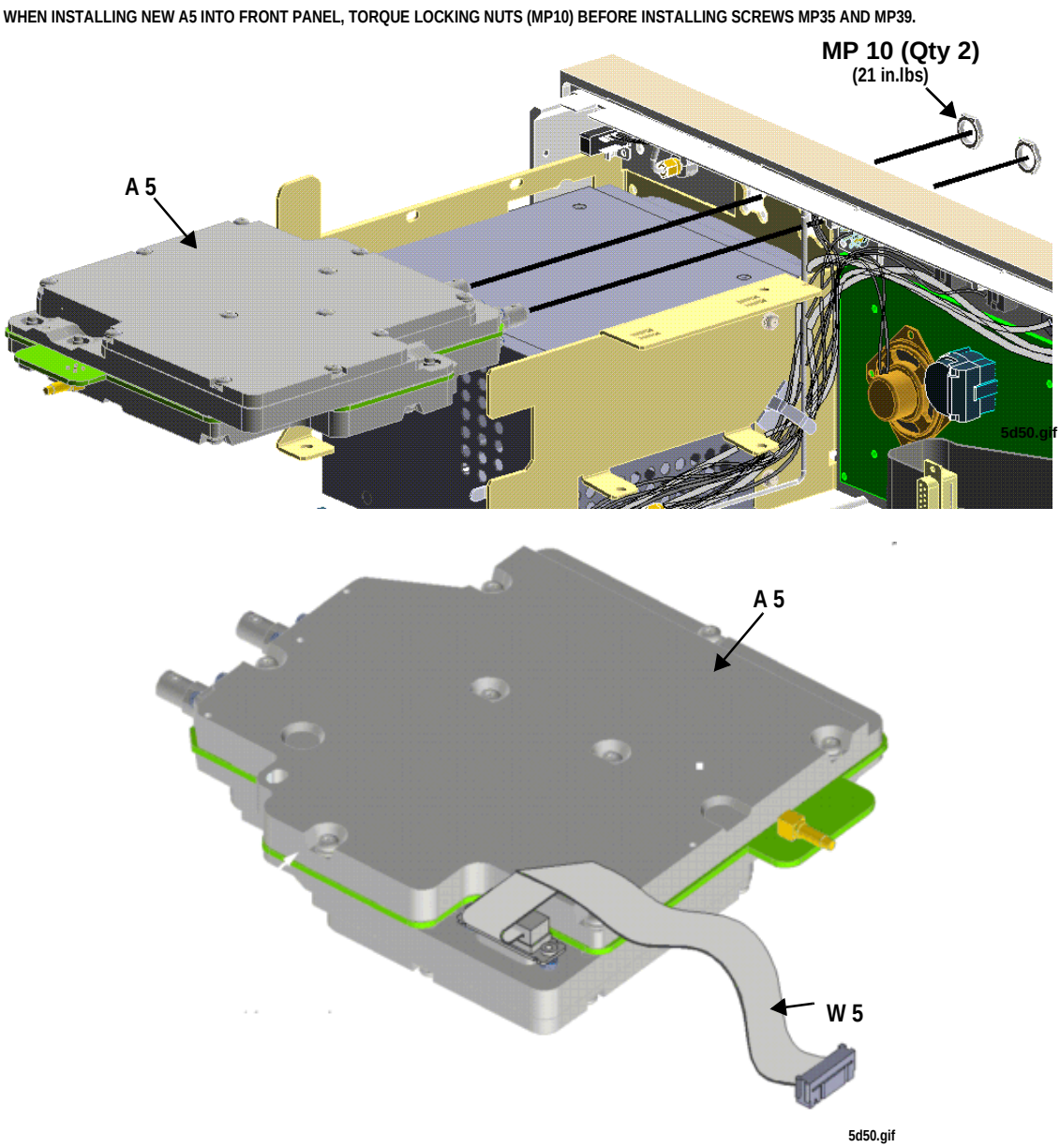


Figure 20 **Removing A5**

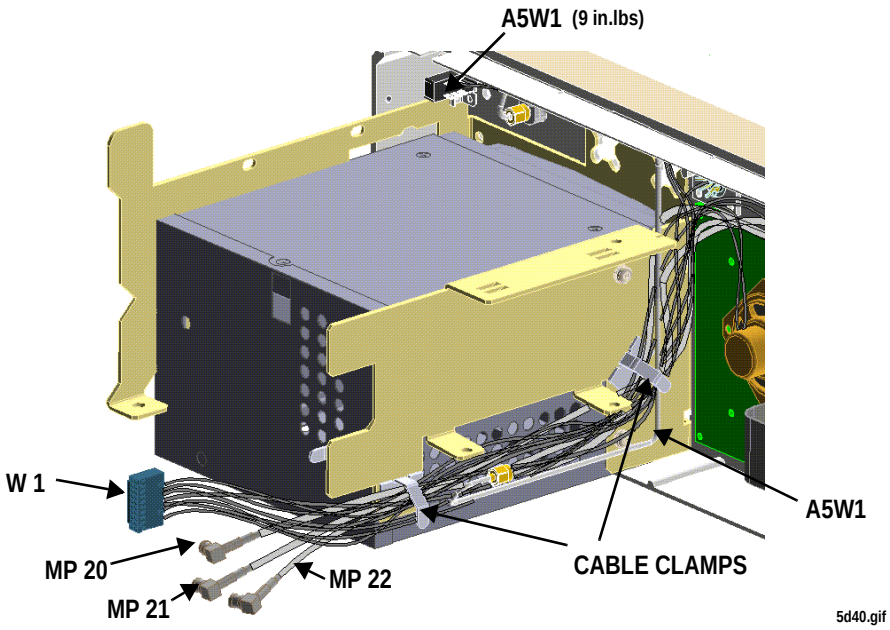


Figure 21 **Cable Routing to the Front Frame**

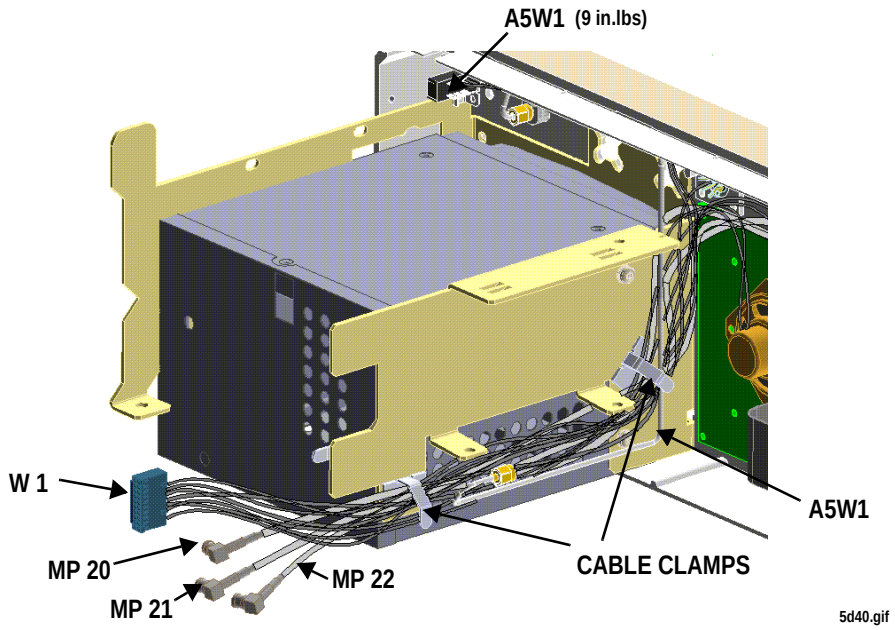


Figure 22 **Cable Routing to the Front Frame**

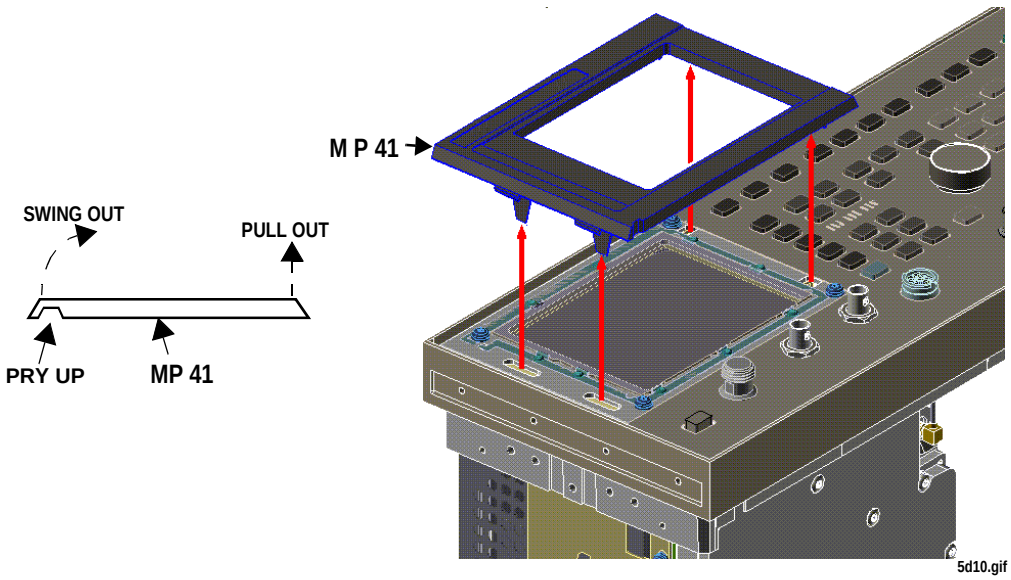


Figure 23 **Removing the Display Bezel**

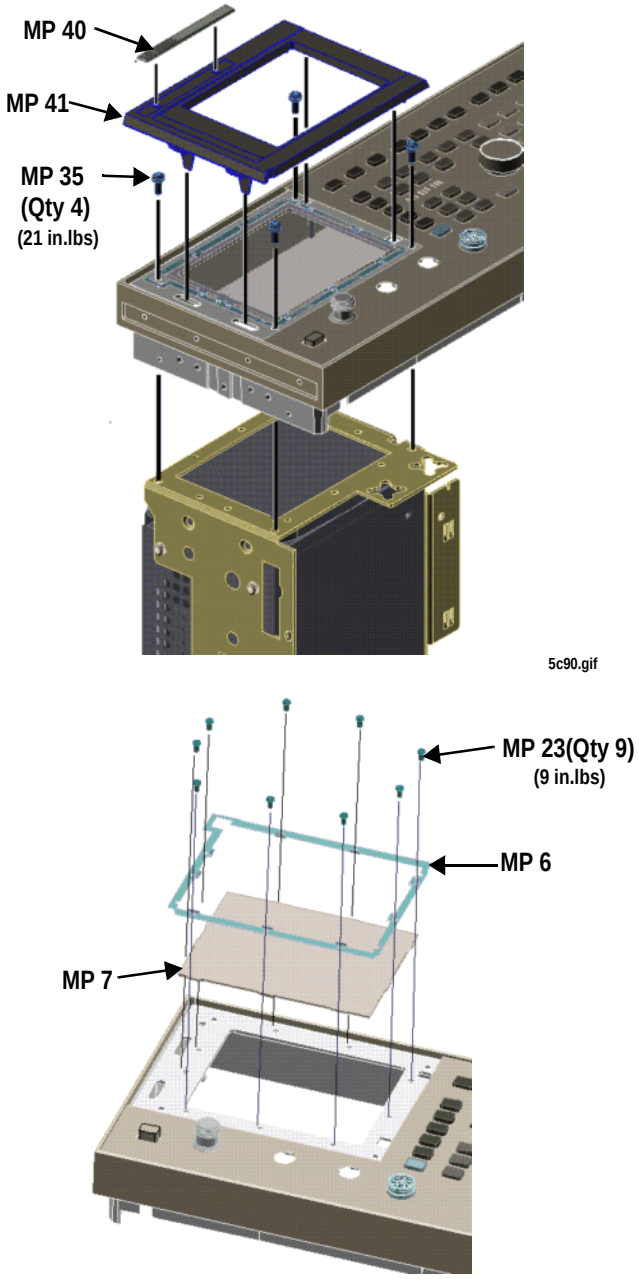
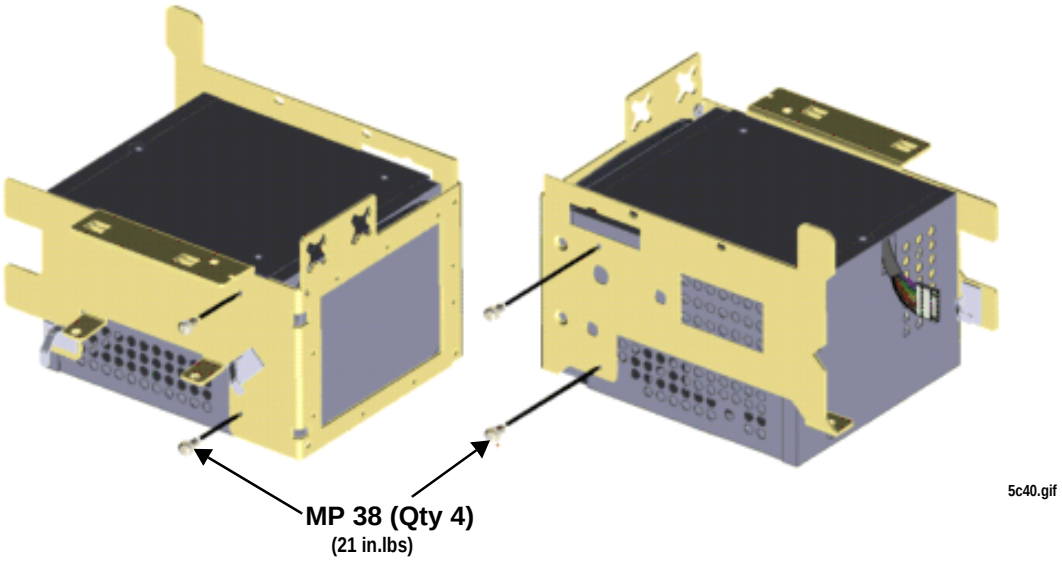


Figure 24 **Removing the Display from the Front Panel**



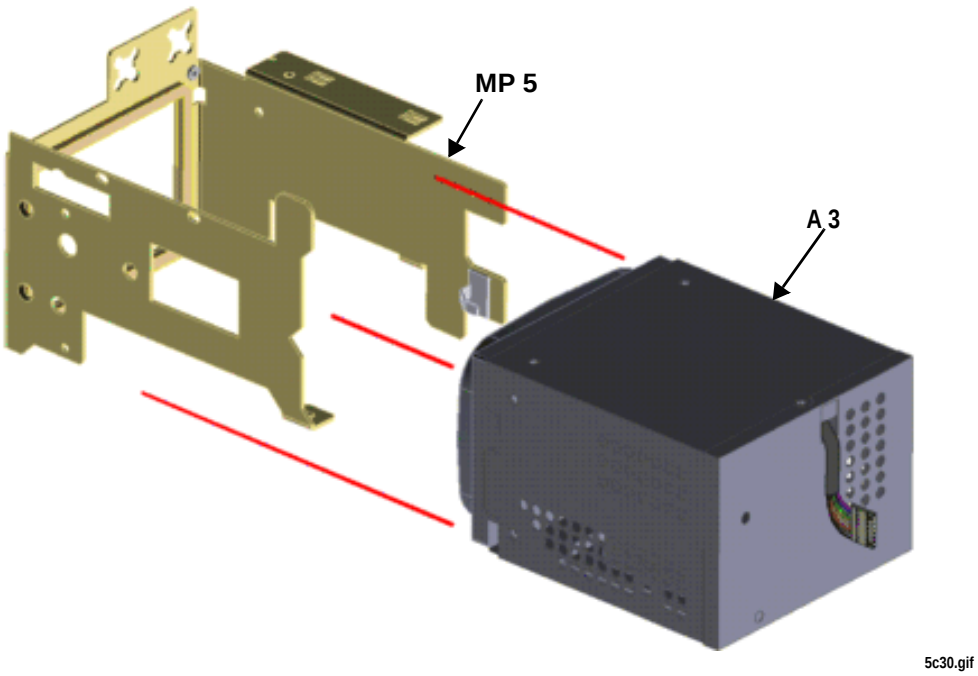
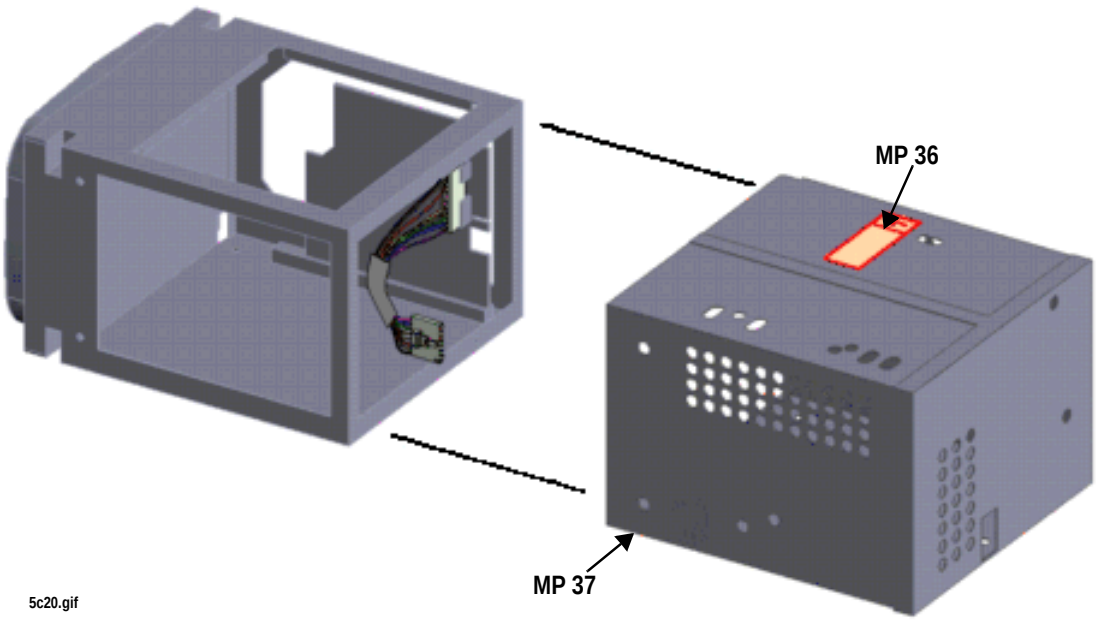


Figure 25 **Removing the Display Assembly from the Bracket**



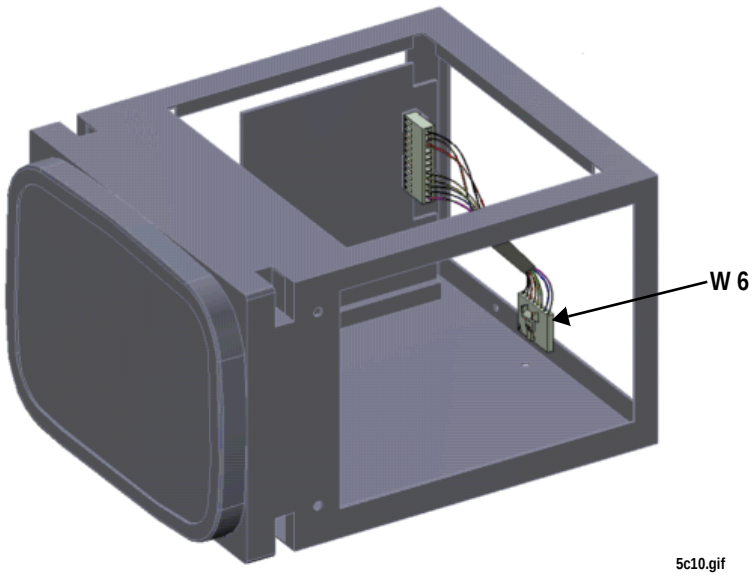


Figure 26 **Removing the CRT Assembly (A3) from its Shield**

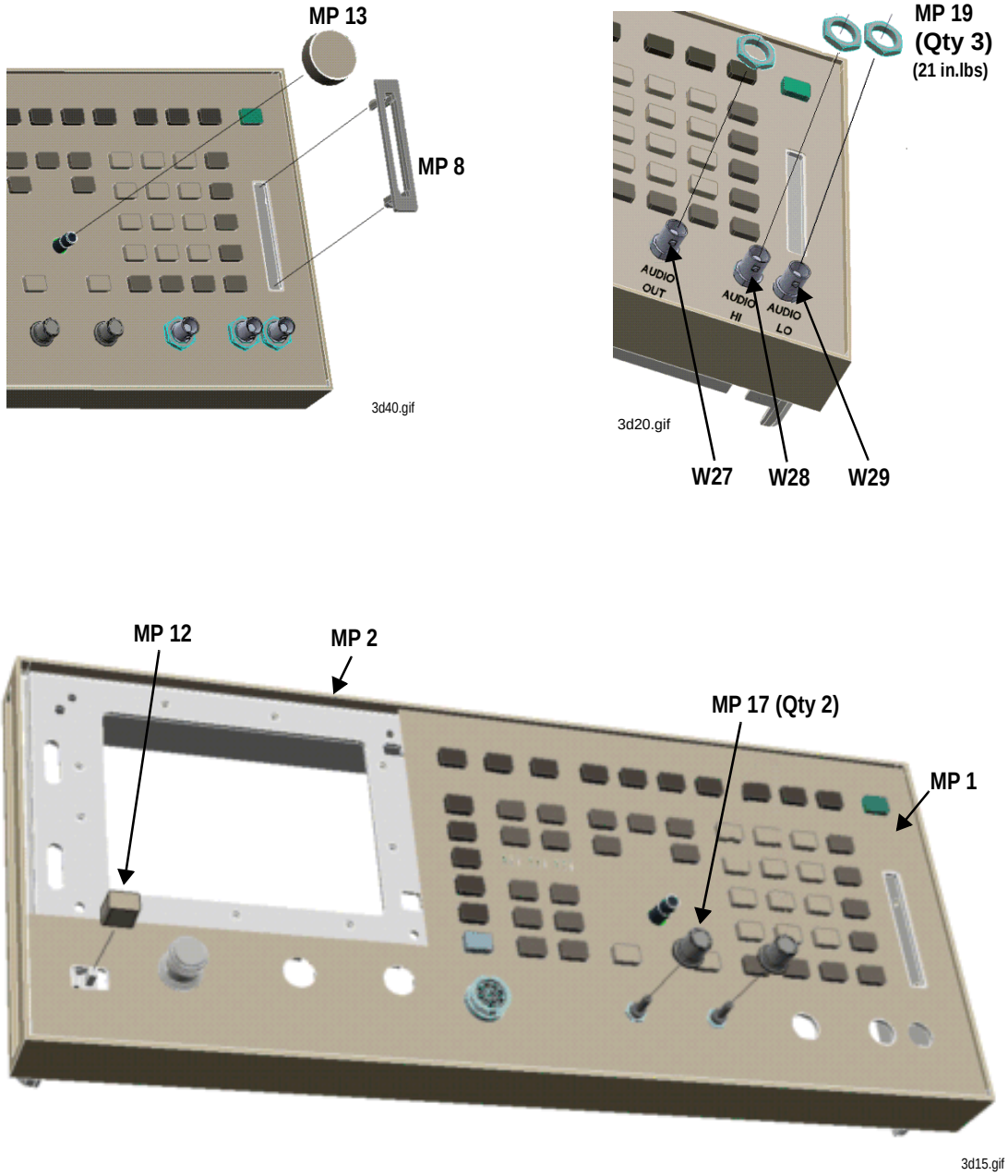


Figure 27 Identifying Replaceable Front Panel Parts

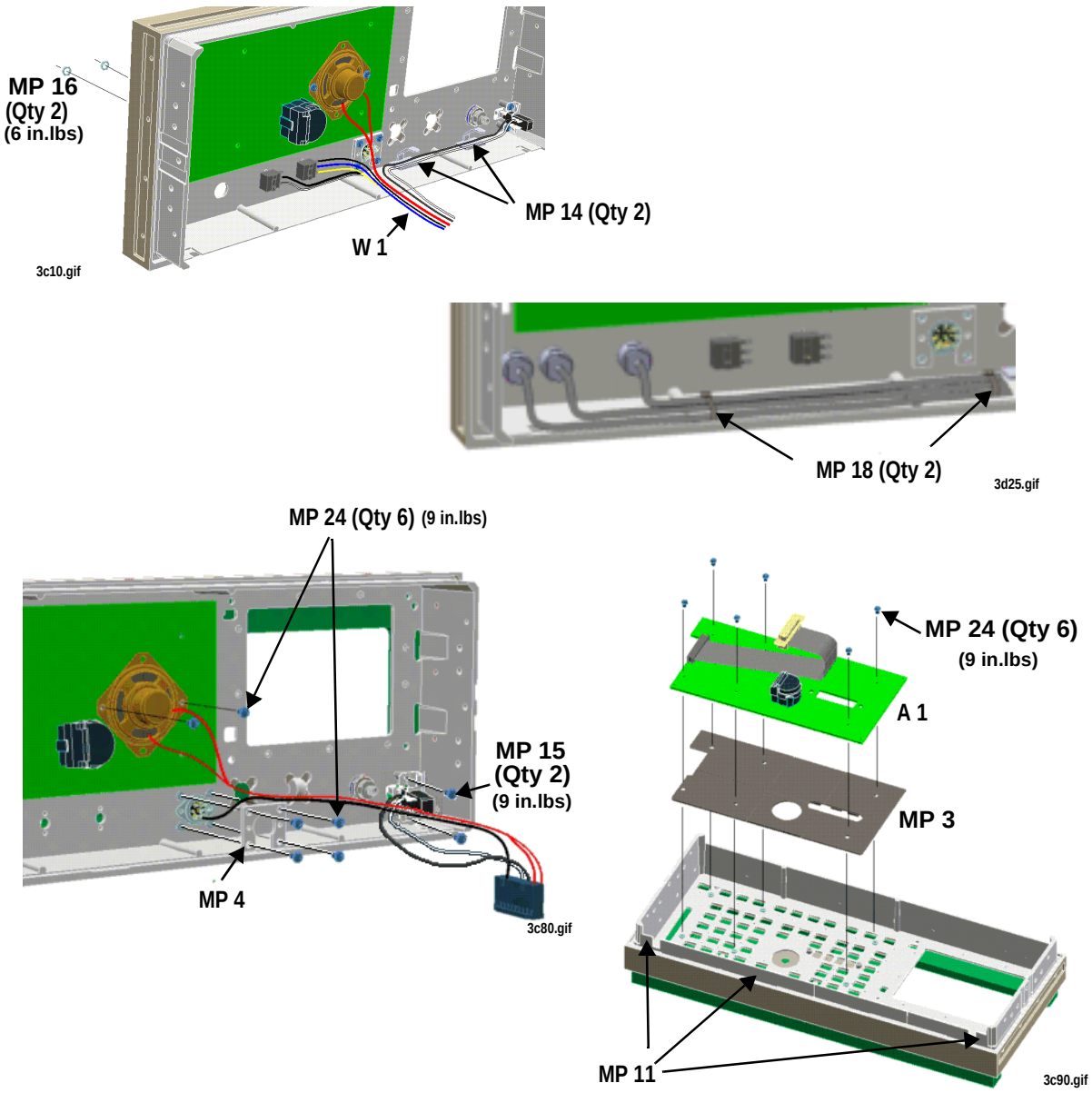


Figure 28 **Front Panel Wiring**

Removing Power Supply (A23)

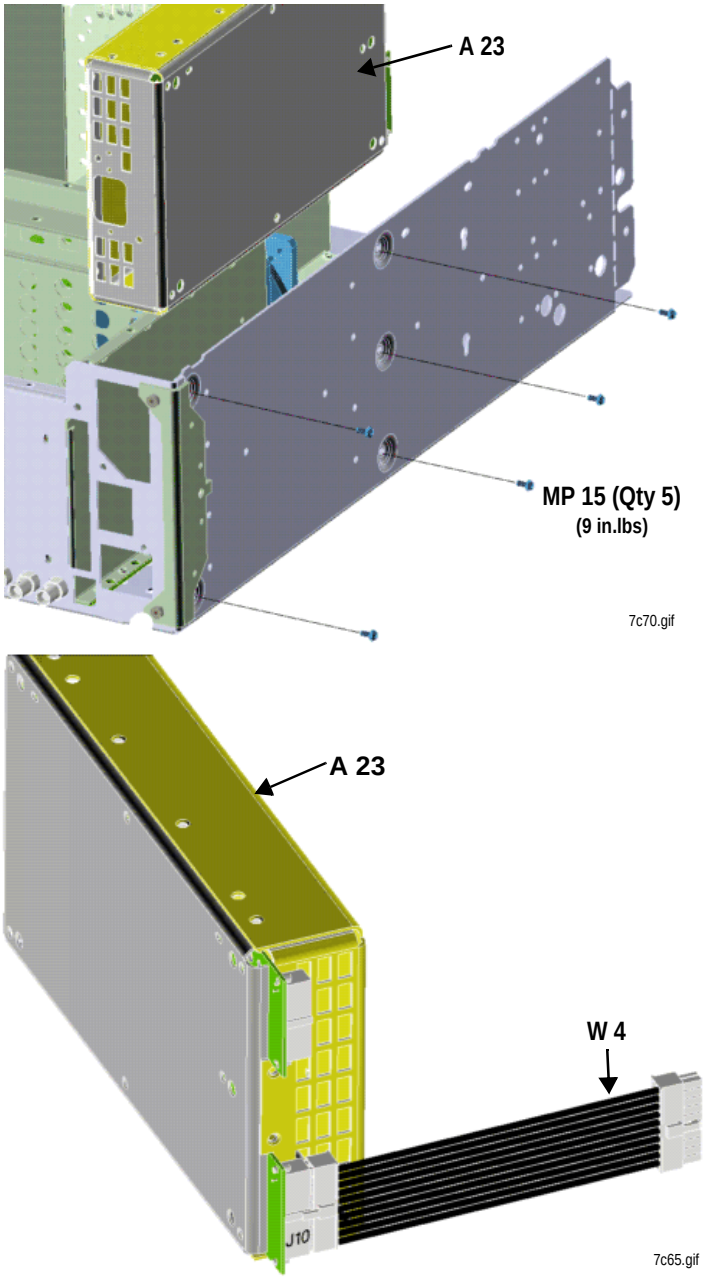
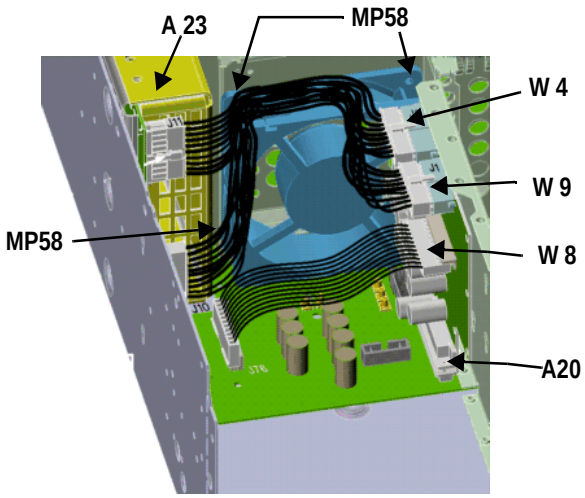


Figure 29 **Removing the Power Supply**

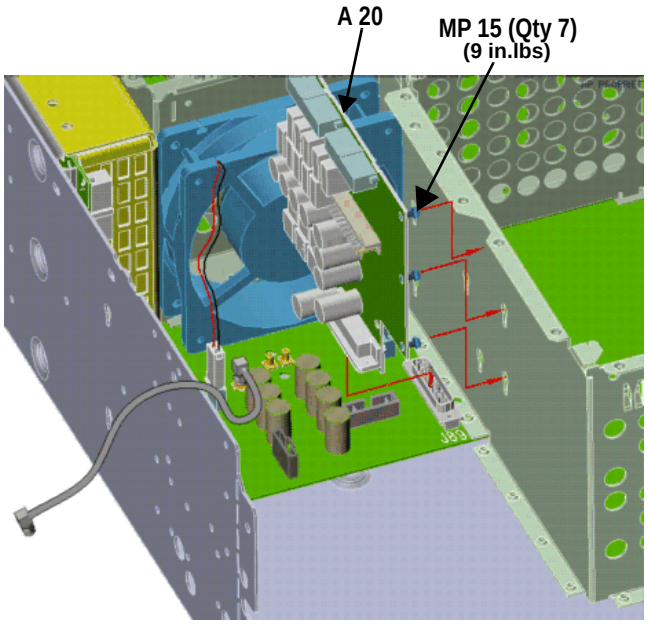
Removing the Voltage Regulator (A20) and Fan (A21)



7c60.gif

DISCONNECT W4, W9 AND W8
TO REMOVE FAN OR A20.

TO REPLACE FAN REMOVE A23 AND
DISCONNECT FAN WIRING FROM J10
ON MOTHERBOARD.
PULL OUT THREE (3)PLASTIC RIVETS (MP 58)



7c90.gif

WITH NEW REGULATOR BOARD
(A20) START SCREWS (MP15)IN BOARD
PLACE BOARD IN KEYWAYS AND SLIDE
DOWN PLUGING BOARD INTO J89 ON THE
MOTHERBOARD. TIGHTEN 9 SCREWS WITH
T-10 BIT AND POWER DRIVER SET AT 9in-l.bs

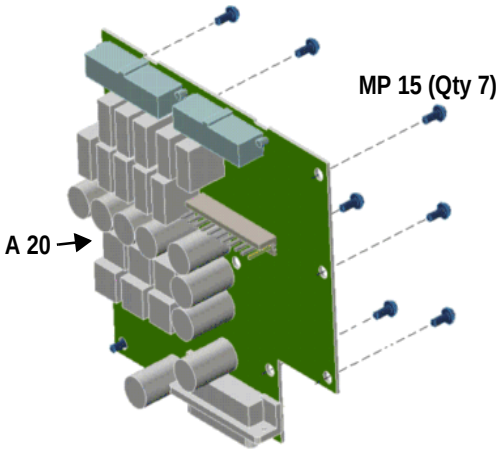
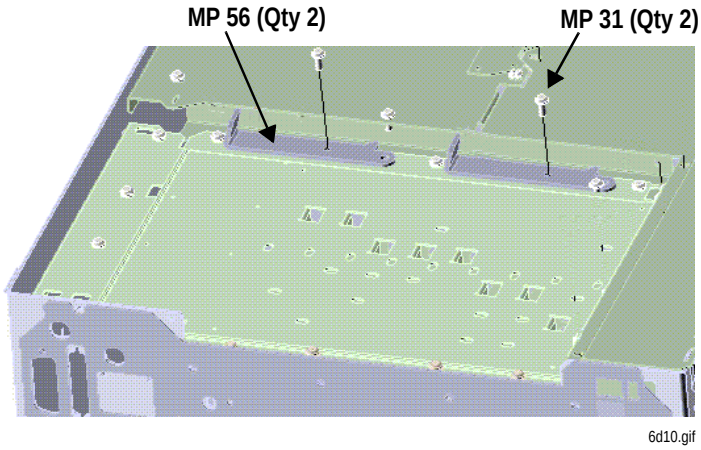
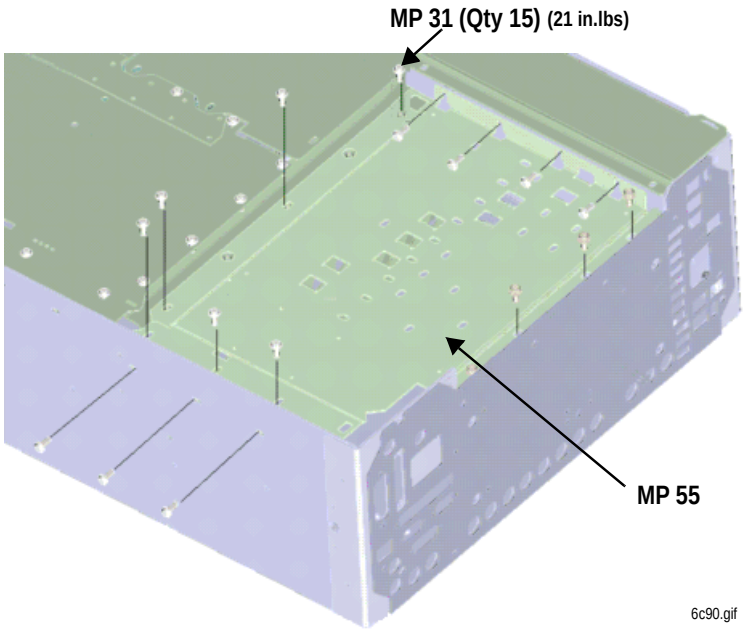


Figure 30 Removing the Voltage Regulator and Fan

Removing the RF and AF Assembly Covers





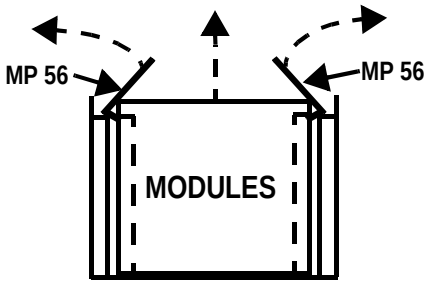


Figure 31 **Removing the RF and AF Assembly Covers**

Removing the Control Interface Assembly (A33)

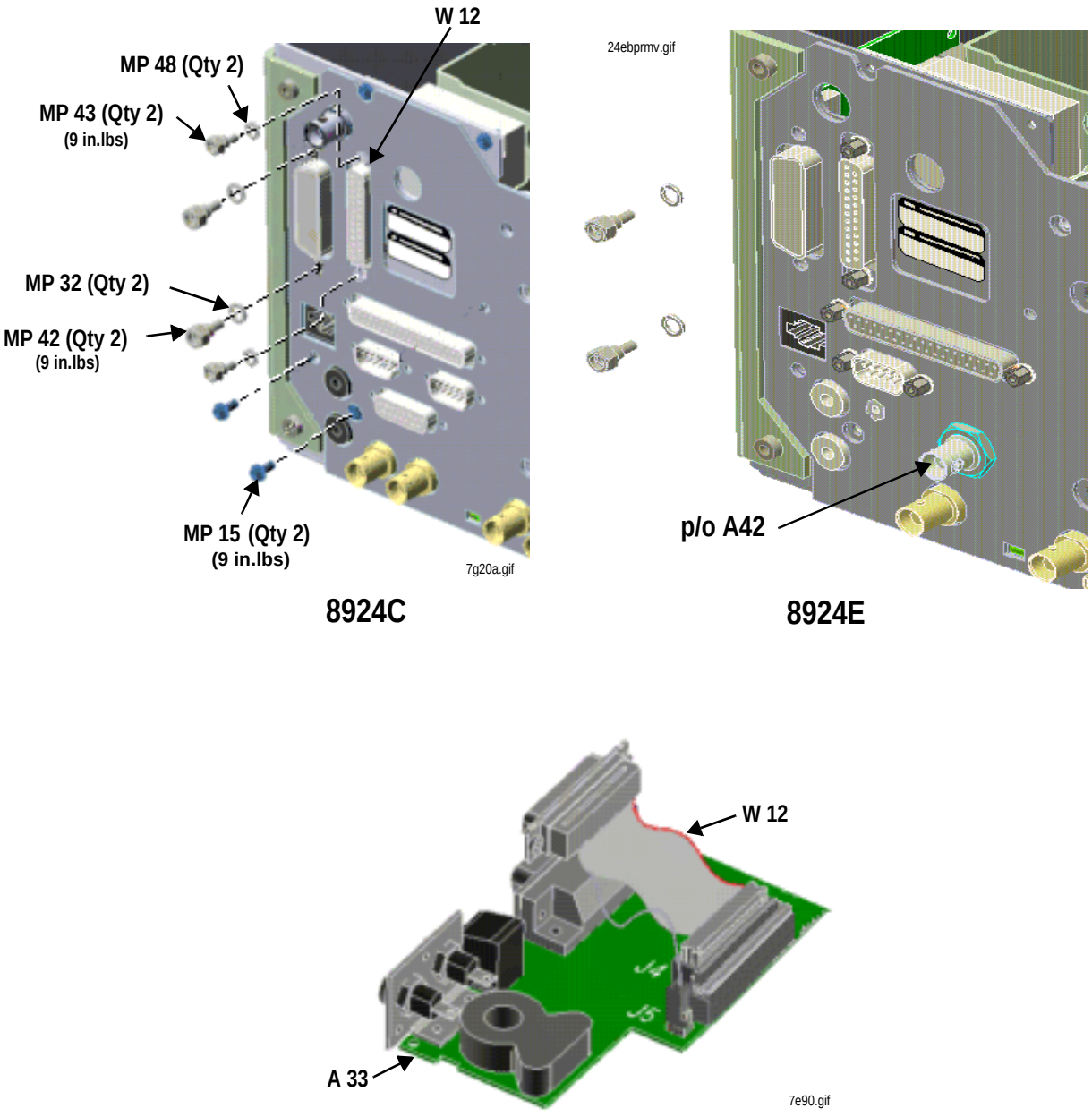


Figure 32 **Removing the Control Interface Assembly**

Removing the Rear Sub-Panel (MP27)

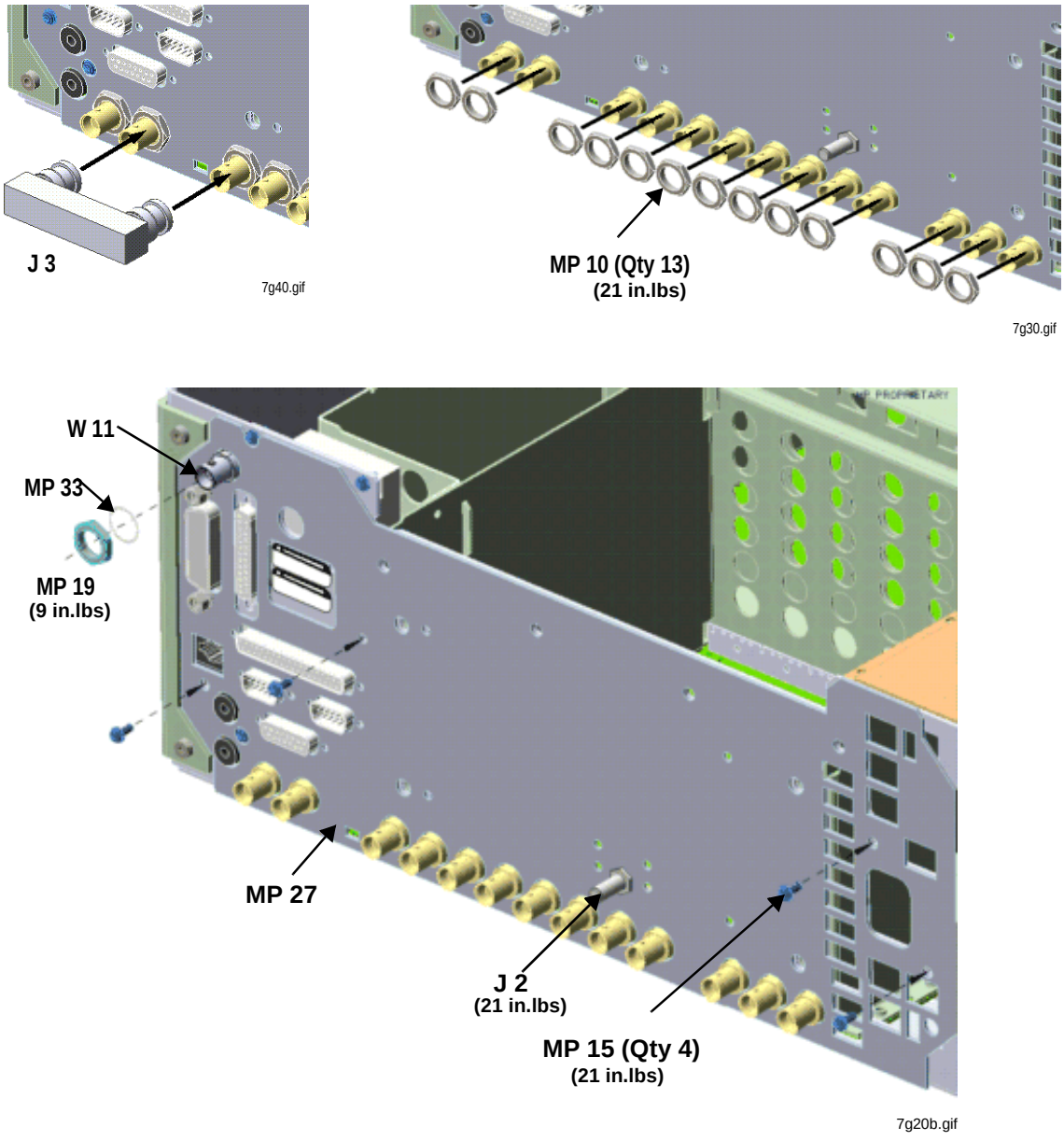
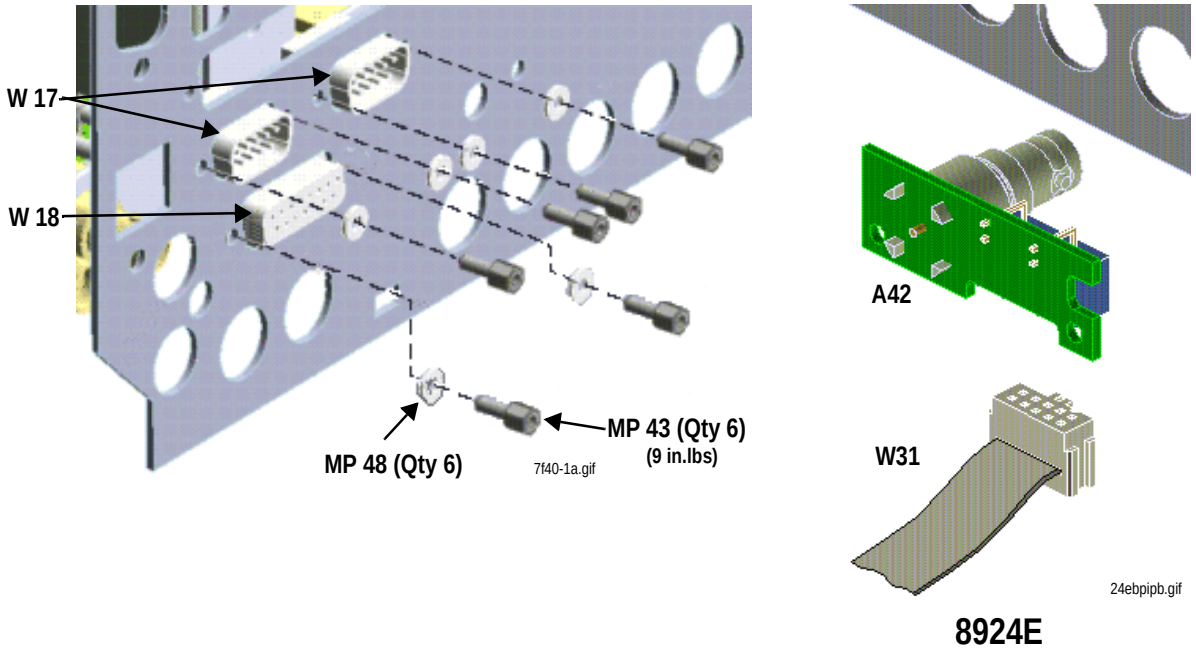


Figure 33 **Removing the Rear Sub-Panel**



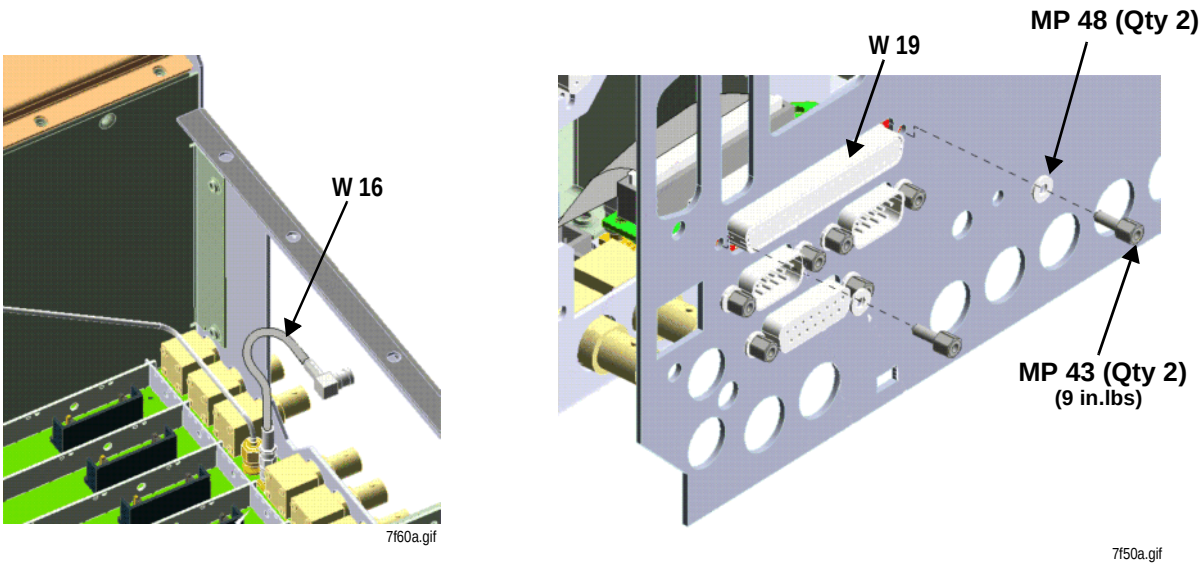


Figure 34 Removing the Rear Sub-Panel (continued)

Removing the Memory Assembly (A17)

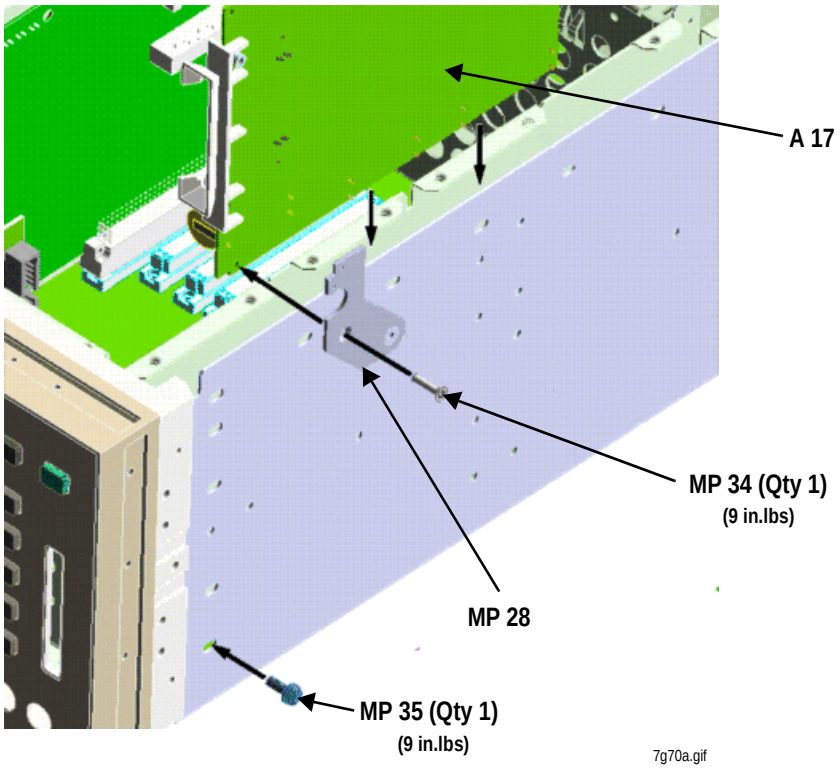


Figure 35 **Removing the Memory Board (A17) and Mounting Bracket (MP28)**

Remove the Oven Time Base (A38)

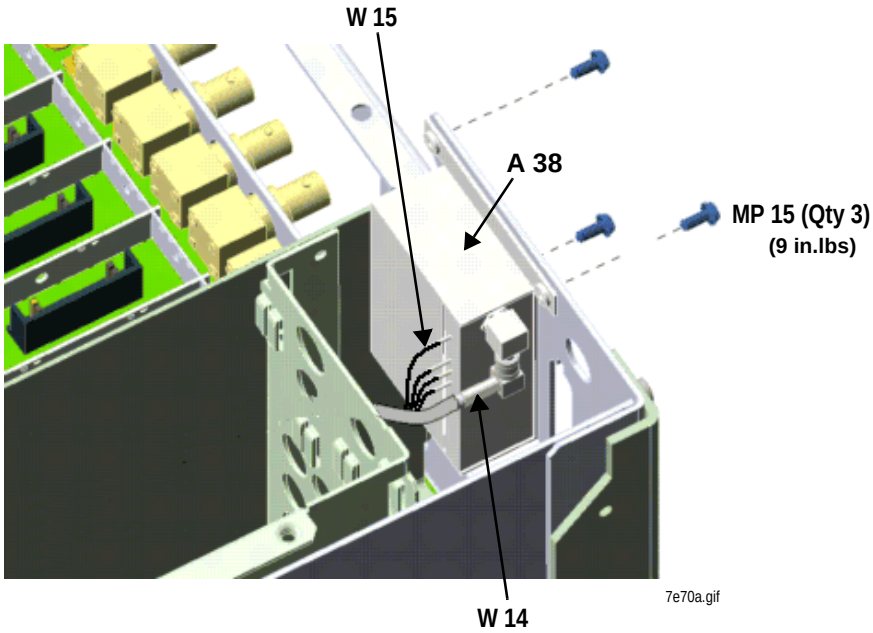


Figure 36 **Removing the Oven Time Base (A38)**

Remove the Audio Analyzer1 Sub-assemblies (A35)

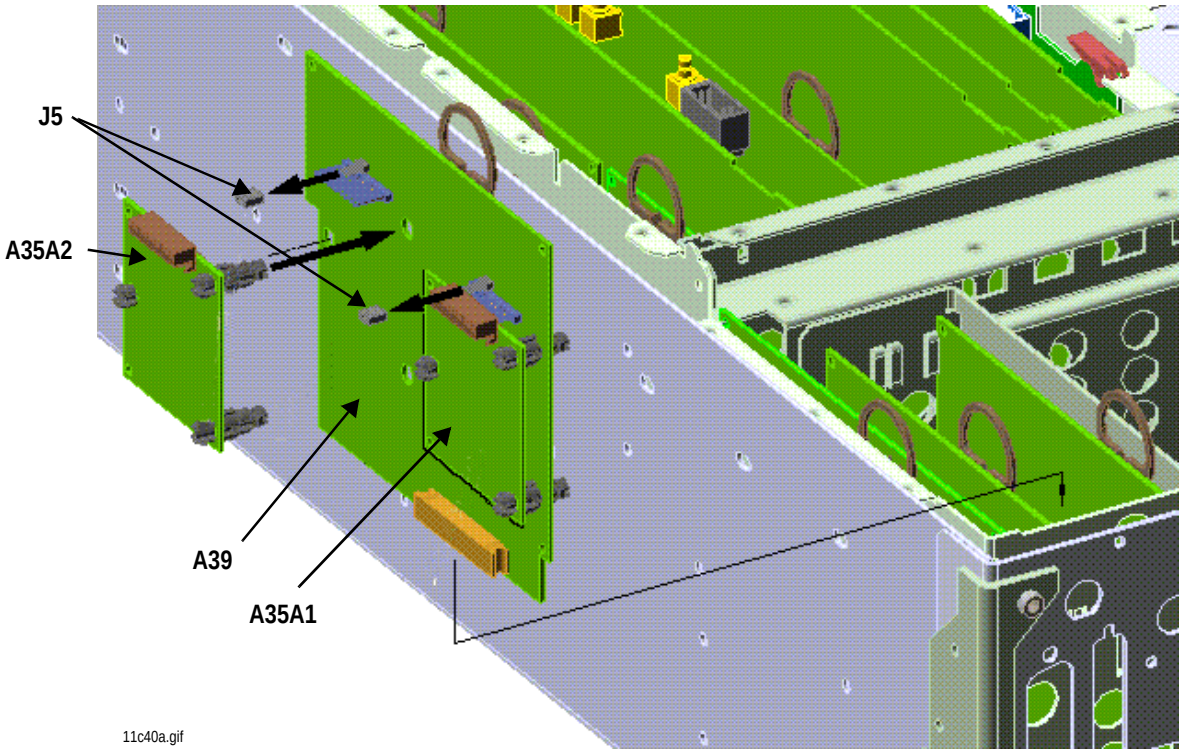


Figure 37 **Audio Analyzer (A35) Assembly Detail**

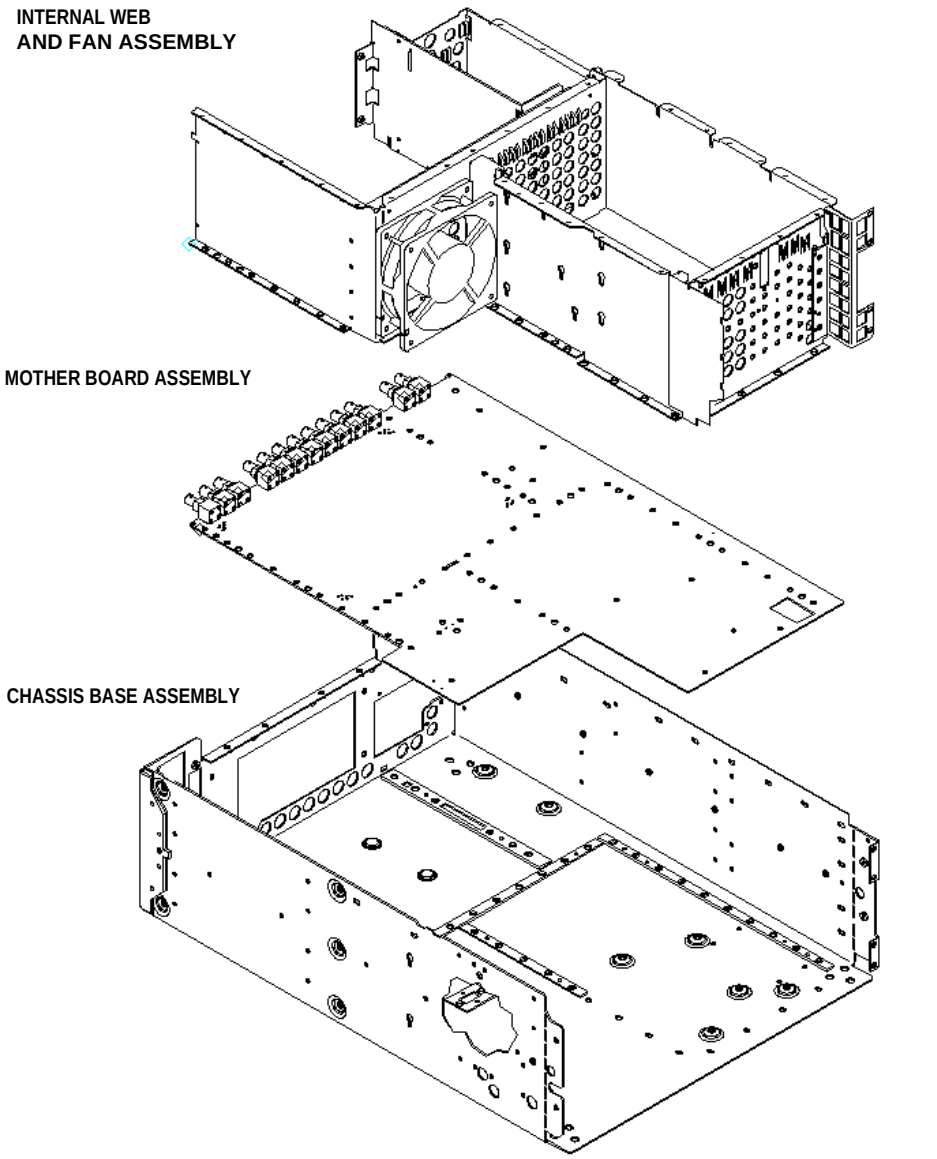


Figure 38 Motherboard-to-Chassis Detail

Fastening the Motherboard to the Chassis Base

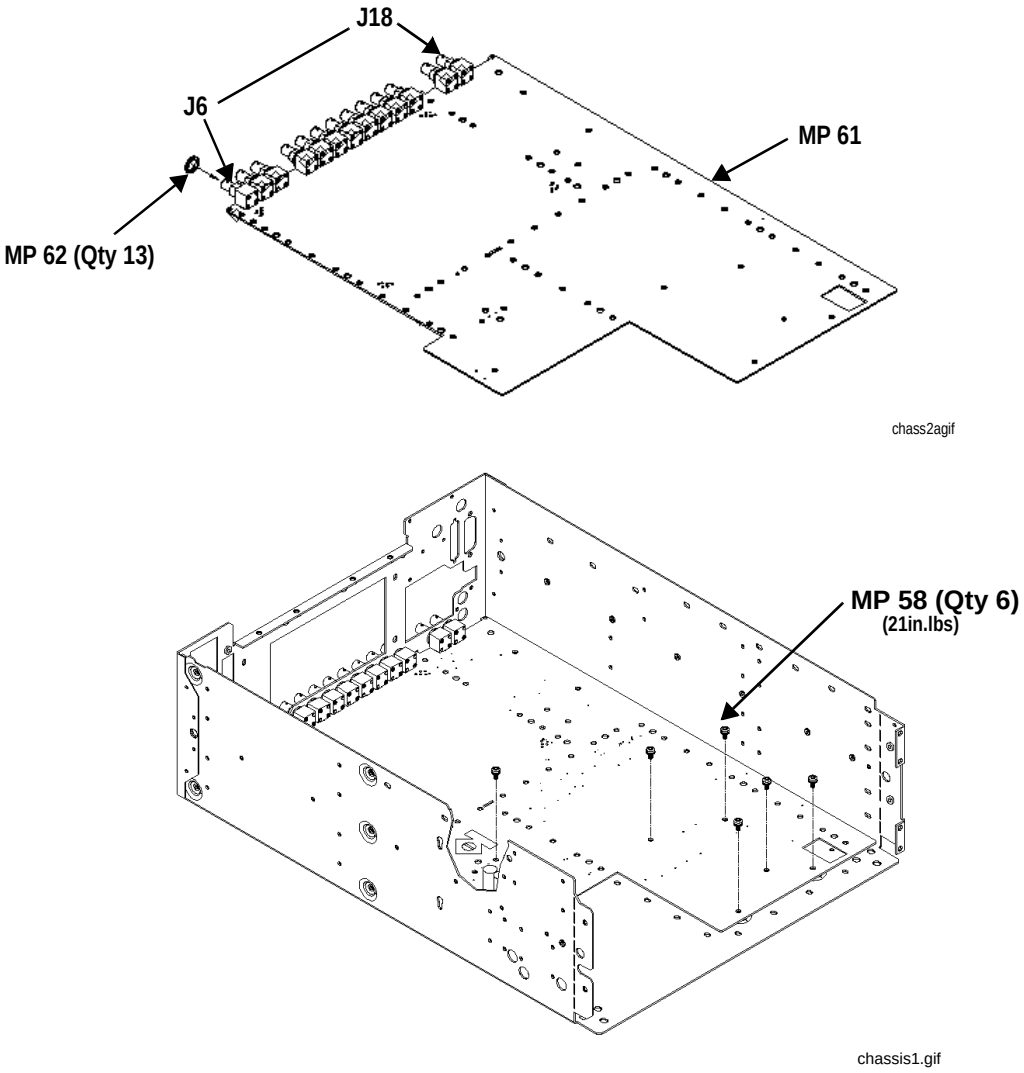
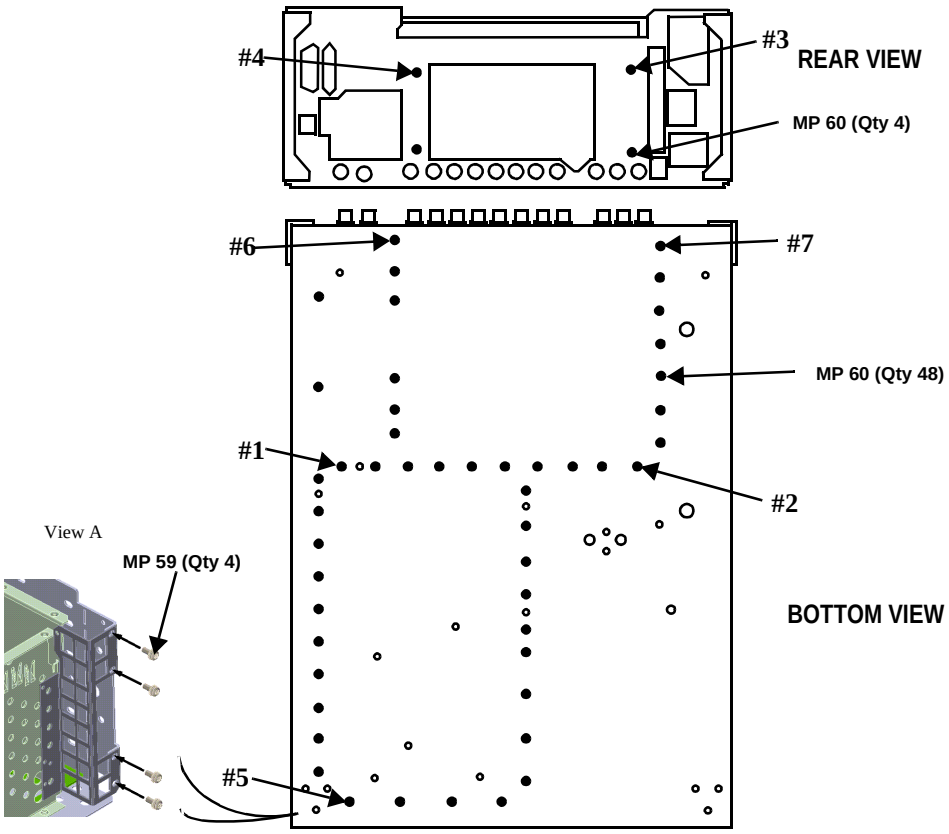


Figure 39 **Fastening the Motherboard to the Chassis Base**

Fastening the Internal Web to the Chassis



Secure Internal Web Assembly and Chassis Base/Motherboard Assembly as follows:

1. Install screws in location #1 and #2 in that order. Tighten to 16 in.lbs.

2. Start screws in locations #3 and #4 but do not tighten

3. Install screws in locations #5, #6 and #7. Tighten to 16 in.lbs

4. Install screws in other holes Tighten to 16 in.lbs.

5. Tighten screws #3 and #4 to16 in.lbs.

Figure 40 Fastening the Internal Web to the Main Chassis

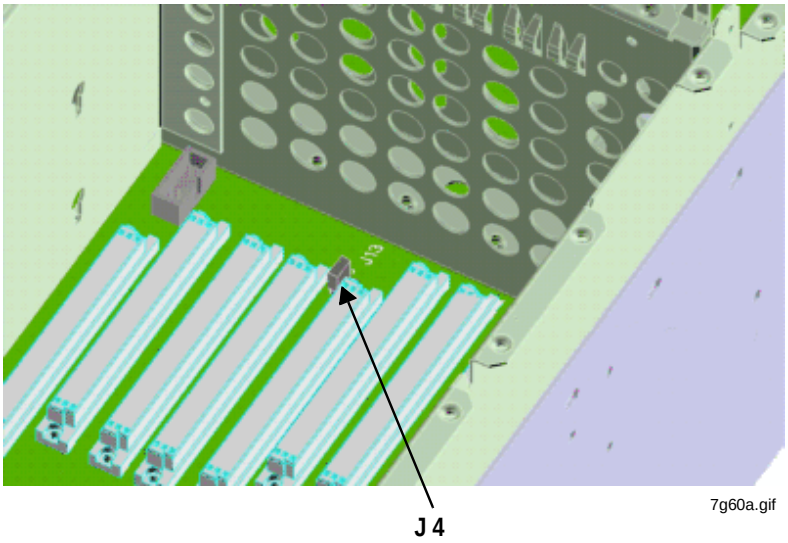


Figure 41 Locating Jumper J4 on the Motherboard

Replacing the A16 Host Controller

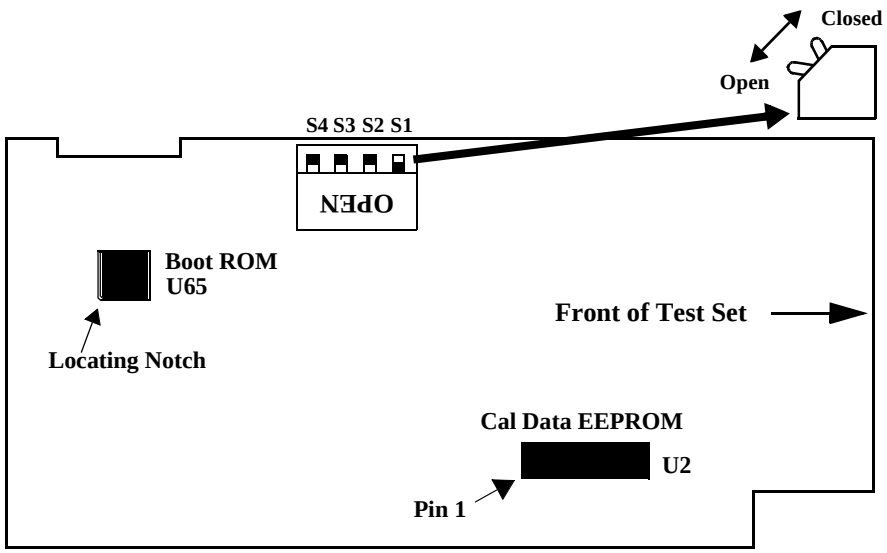
RESTORING CALIBRATION DATA IN NEW A16 ASSEMBLIES

Calibration data for the entire Test Set is stored in EEPROM U21 on the A16 Host Controller. When replacing the A16 Host Controller assembly, you must remove the Cal Data EEPROM from the old A16 assembly and insert it into the new assembly to preserve the calibration data for that instrument.

Replacing the "Boot Code "

"Boot Code" is the firmware that initializes the Test Set on power-up. It also looks at the PCMCIA card port at power-up to see if a firmware revision card has been inserted. This code is stored in EPROM U65 on the A16 Host Controller.

If a new version of boot code needs to be installed, carefully remove the old EPROM and insert the new part, being careful to orient the notch on the EPROM as indicated in the following drawing.



Switch S1 Settings

The following table lists the factory default settings for the four-position DIP switch, S1. Note that the Write Protect function is set to allow calibration data to be entered when the automated periodic adjustments are made. To safeguard calibration data between periodic adjustments, set Switch 1 to the OPEN position.

Table 6 Default Controller Switch Settings

Switch 1	Switch 2	Switch 3	Switch 4
Closed	Open	Open	Not Used

- Switch 1: Write Calibration EEPROM (Open=Disabled, Closed=Enabled)
- Switch 2: Smart Card (Open=PCMCIA, Closed=Epson)
- Switch 3: Run from Flash/OTP (Open=Flash, Closed=OTP) Switch 4: Not Used

4

Periodic Adjustments

Introduction

Some assemblies, or combination of assemblies, require adjustments to compensate for variations in circuit performance over time. Periodic Adjustments are used to optimize Test Set performance by creating and storing new calibration factors to compensate for these changes. This operation is also referred to as “periodic calibration.”

Manual and Automated Adjustments

The Oven Oscillator (A38) frequency is the only manual adjustment made; the remaining adjustments are made automatically when the internal Periodic Calibration routines (PER_CAL3, CDMA_CAL, and PCB_CAL) are run, or when certain “zeroing” fields are selected on various screens. *Any other manual adjustments must not be altered from their factory settings.*

Storing Calibration Data

There are two types of calibration data:

- Factory-supplied data on memory cards shipped with the new assembly or already programmed into the new assembly’s ROMs. (Instructions for downloading calibration data from the memory card are provided with the replacement assembly.)
- Data generated internally by running calibration programs. See **"Running the Periodic Calibration Programs" on page 142**.

In either case calibration data is loaded into non-volatile memory on the A16 Host Controller.

NOTE: Because calibration data resides on the A16 Host Controller assembly, it is important to transfer calibration data from the original failing Host Controller assembly to its replacement assembly. The calibration data resides in a socketed EEPROM which can be moved with little danger of losing its contents. Refer to the instructions accompanying the replacement assembly for details.

When to Make Adjustments

The internal calibration programs should be run whenever an assembly requiring calibration is replaced. It is also recommended that all the procedures in the periodic calibration programs be run at least once a year.

Calibration Equipment

The manual *10 MHz Oven Timebase Adjustment* requires a frequency counter that matches or exceeds the required accuracy for the tests performed by the Test Set.

The automated *Voltmeter References* adjustment requires a DC voltmeter with ±0.015% accuracy.

10 MHz Oven Timebase Adjustment

The timebase frequency is adjusted from the rear panel; it is not necessary to remove any instrument covers.

1. Turn the Test Set on and let it warm up for at least 15 minutes.
2. Remove the factory-supplied jumper between the rear-panel 10MHz OVEN OUT and REF INPUT connectors.
3. Connect the frequency counter to the 10 MHz OVEN OUT connector.
4. Use a screwdriver to turn the TIMEBASE ADJUST screw until a stable 10,000,000.0 Hz is measured by the frequency counter.
5. Replace the jumper between the 10MHz OVEN OUT and REF INPUT connectors.

Zeroing the DC_FM, DC Current, TX Power, and CDMA Power Functions

These functions generate calibration offsets when selected. They are located on various Test Set screens because they are meant to be performed as a routine optimization procedure during normal instrument operation.

DC FM Zero

This function nulls any DC offset on the MODULATION INPUT connector when DC coupling the modulating signal to the Signal Generator Synthesizer.

1. Disconnect any signals to the MODULATION INPUT connector.
2. Access the analog RF GENERATOR screen using the RF GEN key.
3. Select the **DC FM Zero** field (under **FM Coupling**).

DC Current Zero

This function zeroes the DC Current measurement.

1. Disconnect any connections to the rear-panel DC Current Meas connectors.
2. Access the analog AF ANALYZER screen using the AF ANL key.
3. Select **Zero** under the **DC Current** field.

TX Power Zero

This function zeroes the TX Power measurement.

1. Disconnect any cables to the ANTENNA IN or RF IN/OUT connectors.
2. Access the analog TX TEST screen using the TX TEST key located in the ANLG SCRNS group of keys.
3. Select **Zero** under the **TX Pwr Zero** field.

Power Meas Zero

This function zeroes the Avg Power measurement for measuring CDMA signals.

1. Disconnect any signals to the RF IN/OUT connector.
2. Access the CDMA CELLULAR MOBILE TRANSMITTER TEST screen by pressing the TX TEST key located the CDMA SCRNS group of keys.
3. Select **Zero** under the **Power Meas** field.

Running the Periodic Calibration Programs

1. Press the TESTS key to access the TESTS (Main Menu) screen.
2. Select the **Select Procedure Location:** field.
3. Select **ROM** from the **Choices**: menu.
4. Select the **Select Procedure Filename:** field.
5. Select **PER_CAL3** from the **Choices**: menu.
6. Select **Run Test** (USER key K1).
7. Follow the instructions on the screen.
8. Run the **CDMA_CAL** and **PCB_CAL** procedures by repeating steps 4 through 7 for each routine.

Write-Protected Calibration Data

A write-protect switch on the controller assembly protects calibration data from corruption. The calibration procedures check the setting of the write-protect switch. If the switch is set to write-protect, a message is displayed: **`HP-IB Error: Cal data is read only`**. Change the switch setting as shown in **figure 42** and re-run the procedure. Write-protect status is checked again before exiting the program.

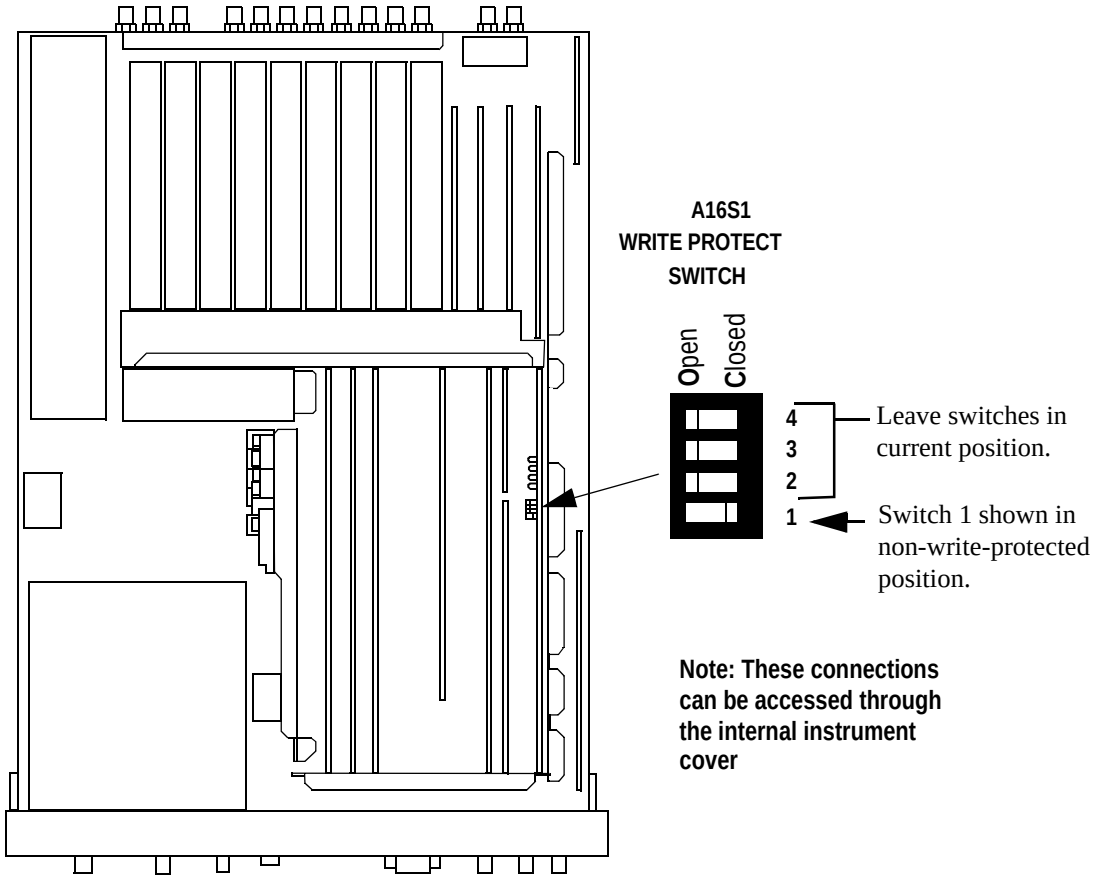


Figure 42 **Locating the Calibration Data Write-Protect Switch**

PER_CAL3 Routines

Voltmeter References

Instructions are displayed explaining how to measure the negative and positive references with an external voltmeter. The user is then required to key in the readings. If the readings are reasonable, the two values are downloaded.

For the Test Set to meet published specifications, the external DC voltmeter must be 0.015% accurate. The voltmeter is connected to the test points shown in **figure 43** .

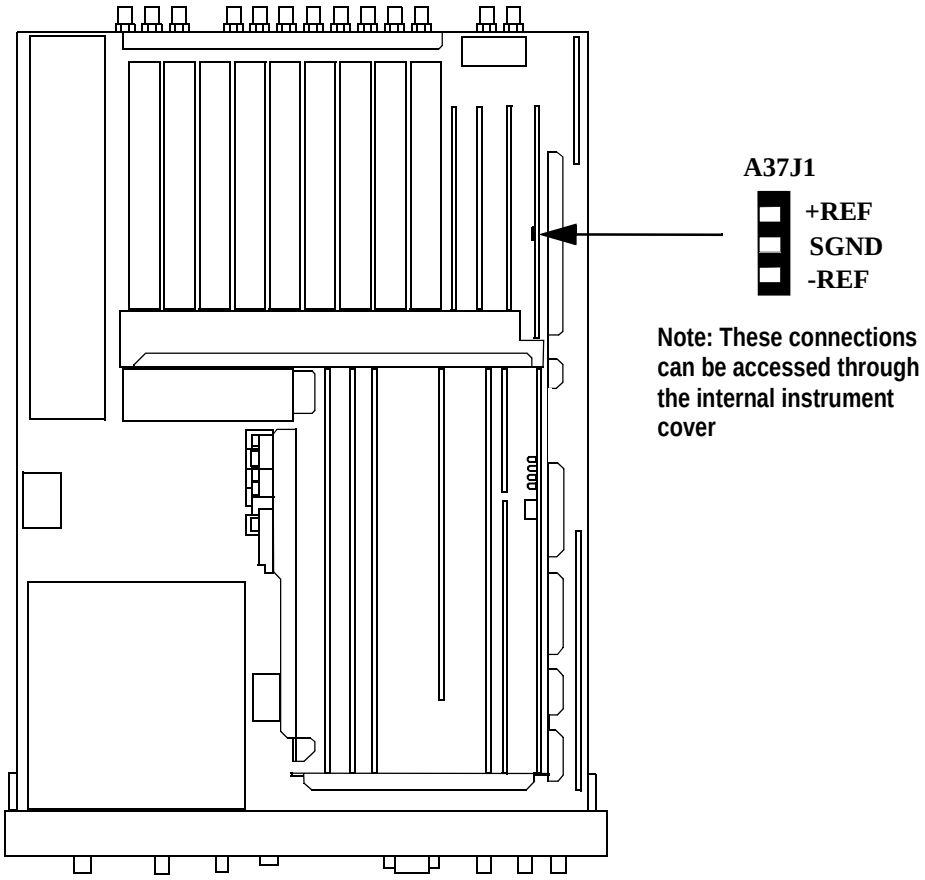


Figure 43 **Locating the Voltage Measurement Reference Points**

Audio Frequency Generator Gain

The gain of the following paths is calibrated:

1. The internal paths that run from Audio Frequency Generators 1 and 2 (individually) through the Modulation Distribution assembly, to the monitor select output, then onto Audio Analyzer 1 to the DVM
2. The paths that run from Audio Frequency Generators 1 and 2 (individually) through the Modulation Distribution assembly to the **AUDIO OUT** connector, externally to the rear-panel **MODULATION IN** connector, then again through the Modulation Distribution assembly to the monitor select output and to the DVM

The above-measured levels are used to adjust the output level of the audio generators so that they produce a calibrated level to the modulation inputs of the RF Generator. These measurements are made at DC. Both positive and negative levels are measured to produce an optimum calibration factor.

External Modulation Path Gain

The *Audio Frequency Generator Gain* program should be run first.

The path in this program runs from the external MODULATION IN connector through the Modulation Distribution assembly, through the Monitor Select Switch, then through Audio Analyzer 1 to the Test Set's internal DVM. The DC source is Audio Frequency Generator 1 through the AUDIO IN connector and an external cable.

The goal of this procedure is to set the External Level Amplifier gain DAC (on the Modulation Distribution assembly) to produce a gain of exactly 4 between the MODULATION IN connector and output of the Monitor Select Switch. This requires measuring the input and output levels, calculating the gain, changing the DAC setting, and then repeating the process until the calculated gain equals 4.

Audio Analyzer 1 Offset

Two DC offsets are measured and downloaded as calibration factors to the Audio Analyzer 1 assembly:

1. Input Select Switch grounded
2. Audio Input selected with return conductor grounded

Variable Frequency Notch Filter

The calibration factors for tuning the variable-frequency notch filter are determined: The input to the filter is set to 10 evenly-spaced frequencies between 300 and 10 000 Hz. The DAC that tunes the notch filter is adjusted for best null of the tune error voltage. From this data, three coefficients of a parabola which best fit the tuning data are calculated using a least-squares curve fit. The coefficients are then downloaded into the Test Set's non-volatile memory.

CDMA_CAL Routines

I/Q Modulator

The four DACs on the IQ Modulator assembly are adjusted to minimize the gain/quadrature spurs (GQS) and the origin offset spurs (OOS) that are present in IQ modulation. Twelve adjustments are made between 500 to 1000 MHz. At each frequency, the Phase Quadrature DAC and the I Gain DAC are adjusted to minimize the gain/quadrature spur first, and then the I Offset DAC and the Q Offset DAC are adjusted to minimize the origin offset spur. By reducing spurs, carrier feed-through (caused by OOS) and modulation distortion (caused by GQS) are reduced, increasing the Rho measurement quality.

Receiver Mixer

The mixer's loss is characterized at several points from 0.4 to 1010 MHz to improve the level accuracy of the Spectrum Analyzer by ≥ 20%. During the procedure, the Spectrum Analyzer's self-calibration signal is removed and the RF Analyzer's power meter is zeroed. Signal level at each frequency point is measured by the Spectrum Analyzer and RF Analyzer; calibration data is calculated using the difference in their measurements.

Attenuator

The attenuators loss is characterized from 0 to -35 dBm in 5 dB steps. Calibration factors are generated at 31 frequencies from.4 to 1010 MHz. The level at -40 dBm is used as the reference to calculate the calibration factors for the other attenuator settings. The -40 dBm setting uses 20 dB attenuators at the input and output of the attenuator section, affecting SWR from -40 dBm and below. Using -40 dBm as the reference helps stabilize SWR at these lower levels. A 6 inch BNC cable and a 3 dB pad are required for this routine.

Generic Cable

Cable losses between the Input and Output sections are measured to generate calibration factors to compensate. Calibration factors are generated at 31 frequencies from 0.4 to 1010 MHz, at a level of -40 dBm (for best SWR). See *Attenuator* above.

PCB_CAL Routine

The levels of each I and Q signal into the IQ Modulator (A25) are equalized. Sixteen signals are generated on the Cell Site Analog (A8) assembly (eight I and eight Q), and two I and Q noise signals come from the CDMA Reference (A29) assembly. The gain DAC for each signal is set to several states and the resulting signal level is measured on the IQ Modulator. Calibration offsets for each signal are stored to produce equal levels for each signal at a given setting.

5

HP 8924C
Performance Verification

This chapter contains step-by-step tests to verify the specified performance of the Test Set. Performance Test Records are included at the end of this chapter to document the measurement results for each test point (**see "HP 8924C Performance Test Records" on page 305**).

Verifying Performance

Test Set Operation

You need to know basic Test Set operation to perform these test procedures (refer to the User's Guide). You should be familiar with the front-panel controls and the use of the control screens. You need to be able to operate the Test Set's RF Generator, RF Analyzer, AF Generators, AF Analyzer, and Oscilloscope.

NOTE: Periodic adjustments should always be performed before verifying instrument performance. **See "Periodic Adjustments" on page 137**.

PRESET BEFORE EACH TEST

Press PRESET on the Test Set before beginning each test to return the controls to a known state.

Equipment

To perform all tests you will need the equipment described in **Table 7**. Equipment for individual tests is shown in the test setup drawings. Alternative test equipment can be used if specifications are equal to those listed in the Hewlett-Packard Test and Measurement Catalog for each HP model. If you just need to verify operation, rather than verify specified performance, you can use the test procedures with functionally equivalent equipment.

Test Equipment Operation

The test procedures give critical instrument settings and connections, but they do not tell how to operate the test instruments. Refer to each instrument's operating manual.

Table 7 Required Test Equipment

Equipment Model # (or equivalent)	Model Name	Performance Test #
HP 3458A	Digital Voltmeter	10, 11, 14, 17, 20
HP 8116A	Function Generator	21
HP 8562A	RF Spectrum Analyzer	8, 9, 29
HP 8902A	Measuring Receiver	1-3,4[a], 5-7, 19, 21-23, 27, 30, 31, 32
HP 8903B	Audio Analyzer	4[b], 12,14, 18, 22, 22 23, 25
HP 11715A	AM/FM Test Source	22-28
HP 11722A	Sensor Module	5-7, 21, 30, 31,32
HP 5316B	Universal Counter	13, 18
HP 778D	Dual Directional Coupler	21, 30
HP 8642A, 8657A/B	Synthesized Signal Generator	4, 19, 26, 29, 30, 31, 32
HP 11667A	Power Splitter	31, 32

a. For connections for an external LO, included as part of HP 8902A Option 003 or 030. For Option 030 it does not matter which filters are installed (only the switching of the LO is important).

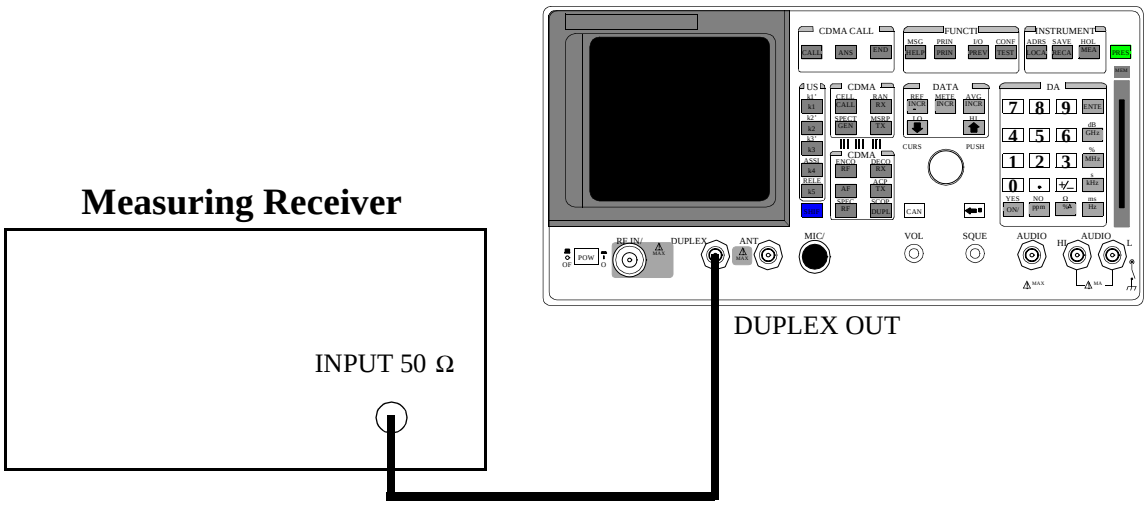
b. For Performance Test 4 the HP 8903B requires a CCITT filter (Option 011 or 051).

RF Gen FM Distortion Performance Test 1

Description

The FM distortion of the RF generator is measured directly by the measuring receiver. The Test Set's internal audio generator provides the modulation source.

Setup

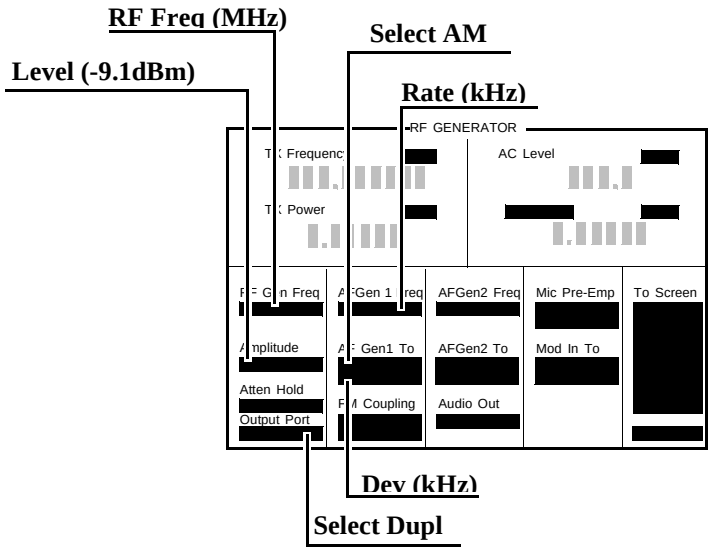


Make the following measuring receiver settings:

- Reset the measuring receiver
- 300 Hz High-Pass Filter
- 3 kHz Low-Pass Filter
- FM mode
- Distortion analyzer mode

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Access the RF GENERATOR screen.
4. Set the **`AFGen1 To`** field to **`FM`**.
5. Set the **`Output Port`** field to **`Dupl`**.



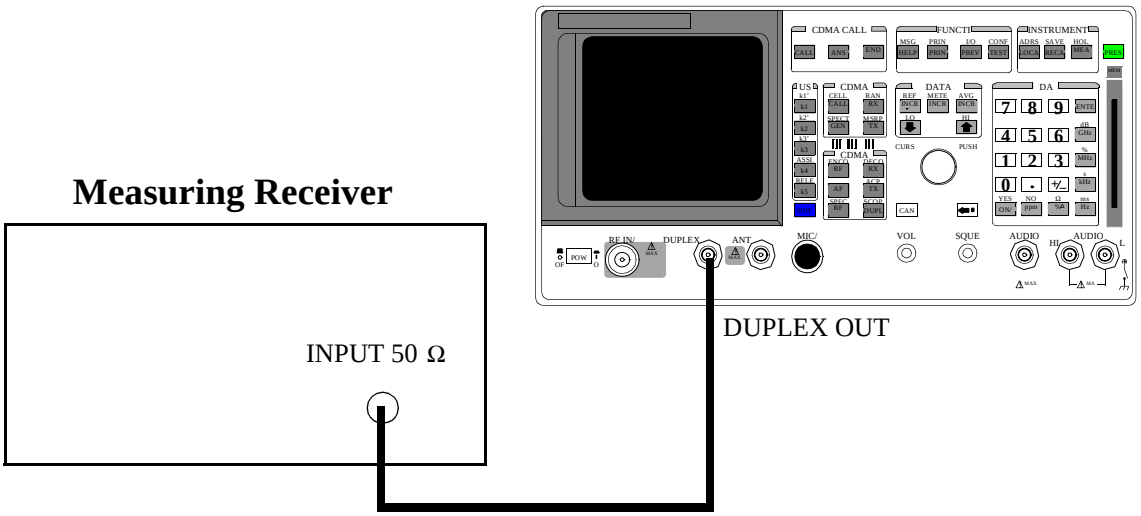
6. Measure the FM distortion at the RF level, frequencies, deviations, and rate shown in the PTR (**see "RF Gen FM Distortion Performance Test 1" on page 307**) and compare the measured distortion to the limits shown in the PTR.

RF Gen FM Accuracy Performance Test 2

Description

The FM distortion of the RF generator is measured directly by the measuring receiver. The Test Set's internal audio generator provides the modulation source.

Setup

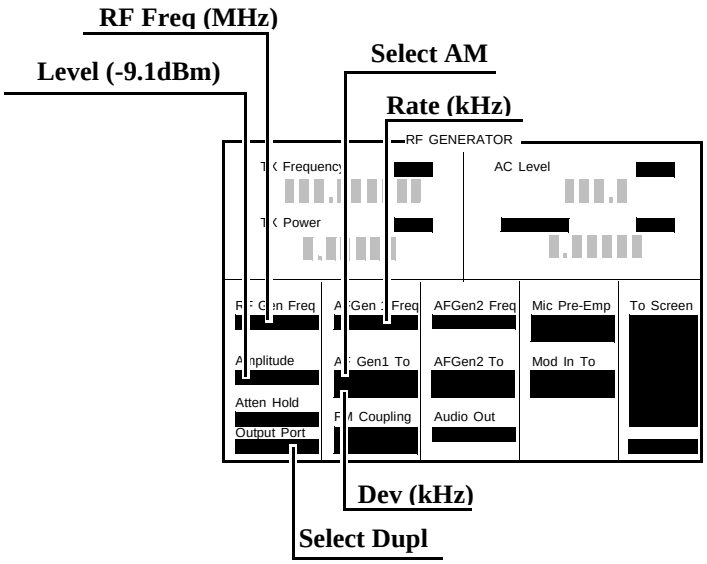


Make the following measuring receiver settings:

- Reset the measuring receiver
- 300 Hz High-Pass Filter
- 3 kHz Low-Pass Filter
- FM mode
- FM de-emphasis off

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Access the RF GENERATOR screen.
4. Set the **`AFGen1 To`** field to **`FM`**.
5. Set the **`Output Port`** field to **`Dupl`**.



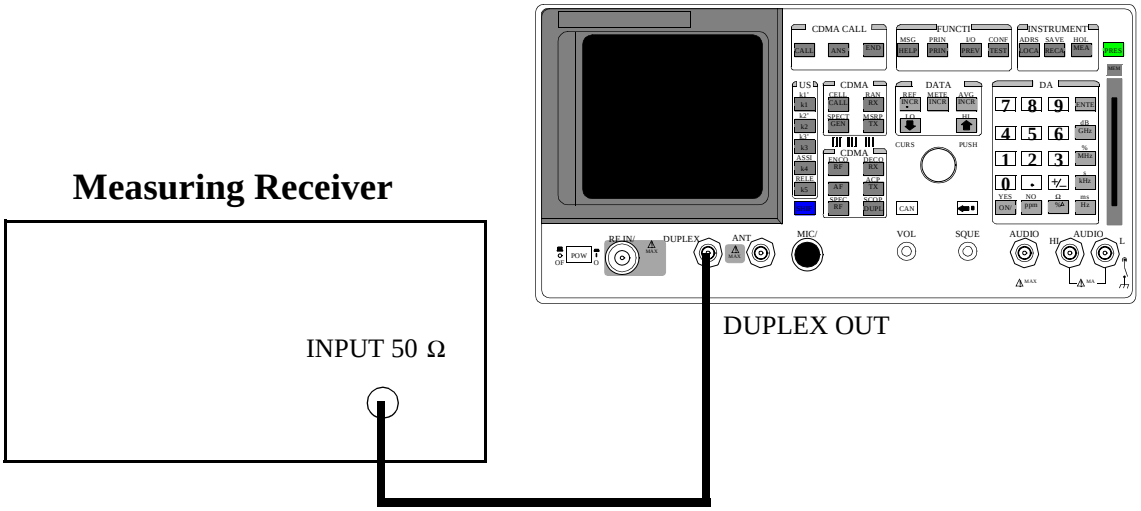
6. Measure the deviations at the RF level, frequencies, deviations, and rate shown in the PTR (**see "RF Gen FM Accuracy Performance Test 2" on page 309**) and compare the measured deviation to the limits shown in the PTR.

RF Gen FM Flatness Performance Test 3

Description

The FM flatness of the RF generator is measured directly by the measuring receiver. The Test Set's internal audio generator provides the modulation source.

Setup

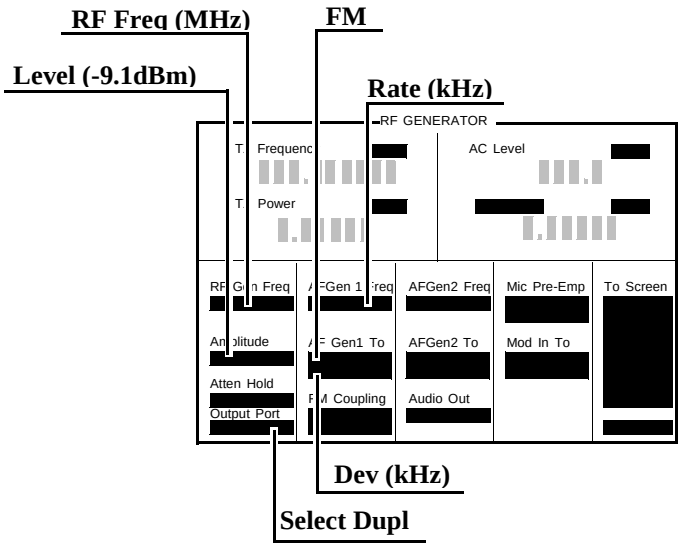


Make the following measuring receiver settings:

- Reset the measuring receiver
- FM mode

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Access the RF GENERATOR screen.
4. Set the **`AFGen1 To`** field to **`FM`**.
5. Set the **`Output Port`** field to **`Dupl`**.



6. Measure the FM deviation at the RF level, frequencies, deviations, and rates shown in the PTR (**see "RF Gen FM Flatness Performance Test 3" on page 311**).
7. Convert the measurement results to dB referenced to the deviation measured at 1 kHz as follows:

$$dB = 20 \log \frac{\text{Deviation}}{\text{Deviation at 1kHz}}$$

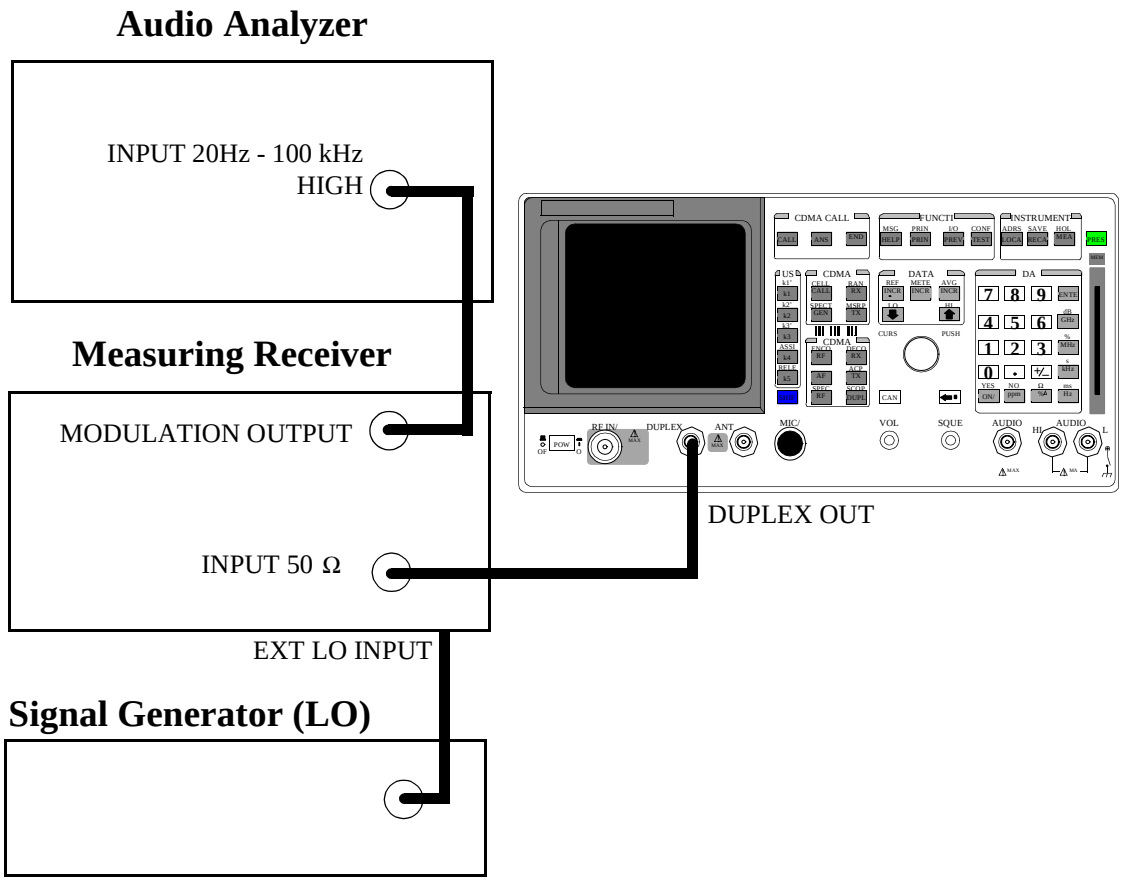
(The computed values must be 0, ±1 dB.)

RF Gen Residual FM Performance Test 4

Description

The residual FM of the RF generator is demodulated by the measuring receiver. An audio analyzer with a CCITT psophometric filter is required to measure the demodulated residual FM.

Setup



Make the following measuring receiver settings:

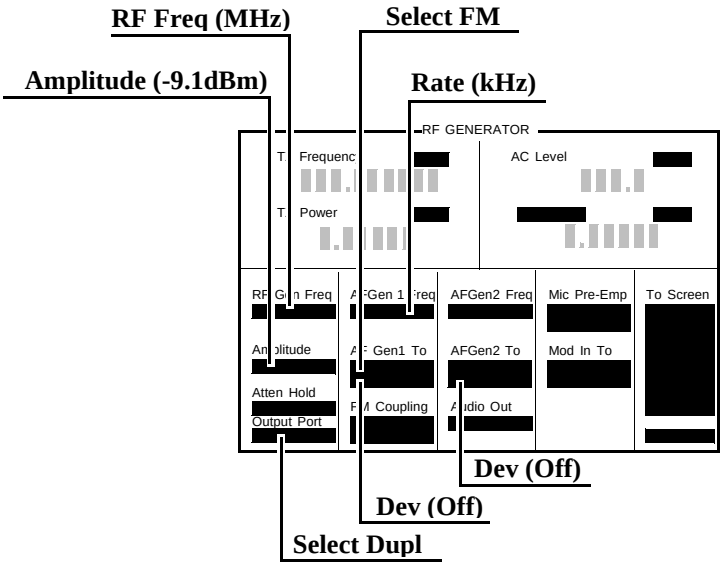
- Reset the measuring receiver
- 1.5 MHz IF
- FM mode
- RMS detector
- 50 Hz High-Pass Filter
- 15 kHz Low-Pass Filter
- Enable the external LO mode

Make the following audio analyzer settings:

- Reset the audio analyzer
- AC level
- CCITT weighting Filter
- 30 kHz Low-Pass Filter

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Access the RF GENERATOR screen.
4. Set the **`Output Port field`** to **`Dupl.`**
5. Set the **`Amplitude field`** to –9.1 dBm.
6. Set the **`AFGen1 To`** field to **`FM.`**
7. Set the **`AFGen1`** and **`AFGen2`** deviation to **`Off`** (using the ON/OFF key).



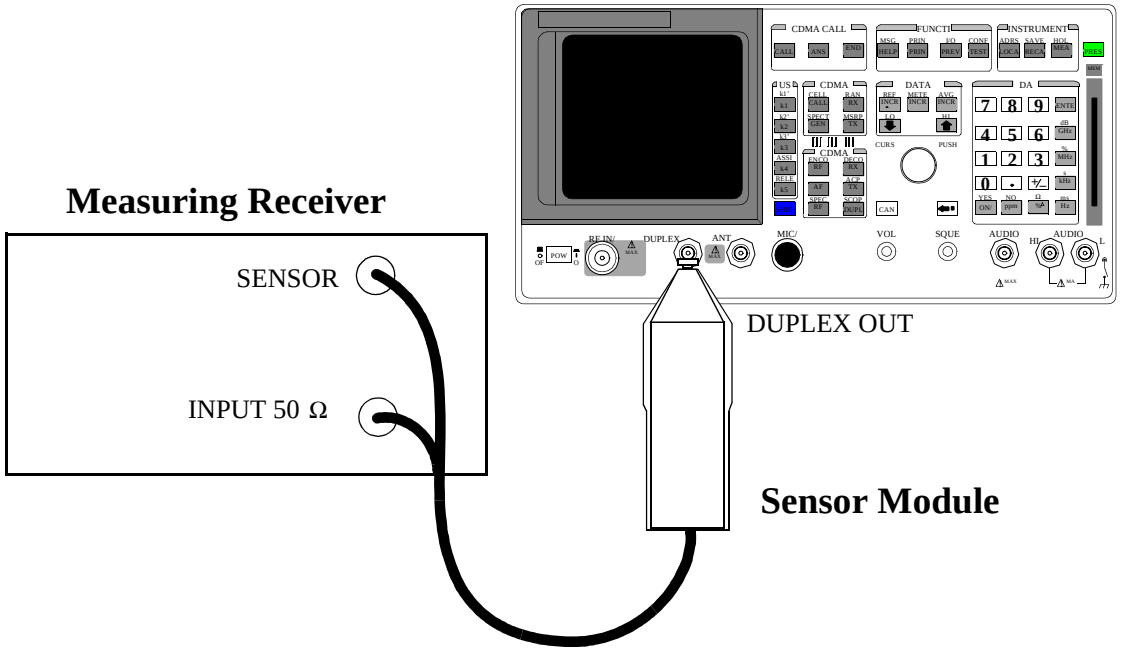
8. Set the signal generator (used as an external LO for the measuring receiver) to the LO frequencies shown in the PTR (**see "RF Gen Residual FM Performance Test 4" on page 312**).
9. Set the Test Set to the RF frequencies shown in the PTR and measure the ac level, in millivolts, on the audio analyzer.
10. Multiply the measured ac levels by 1000 to convert to FM deviation in Hz and compare the computed results to the limits shown in the PTR.

RF Gen Duplex Output High Level Accuracy Performance Test 5

Description

The level of the RF generator, set to 1 and 3.5 dBm, at the duplex output is measured at numerous frequencies by the sensor module of the measuring receiver.

Setup



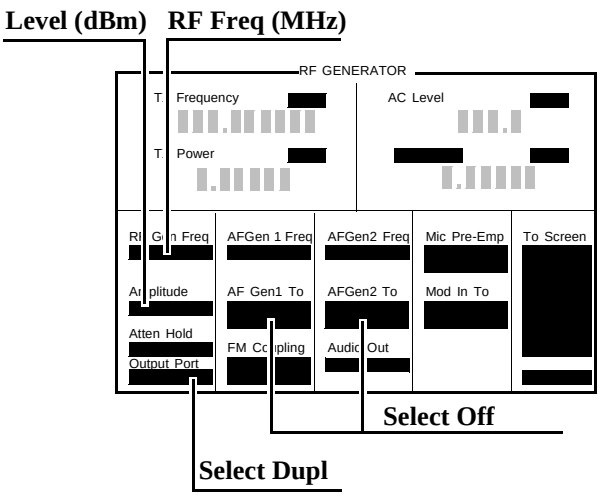
Make the following measuring receiver settings:

- Reset the measuring receiver
- RF power mode
- Log display

NOTE: Make sure to enter the power sensor's calibration data into the measuring receiver and zero the sensor module. Refer to the measuring receiver's and the sensor module's operating manuals.

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Access the RF GENERATOR screen.
4. Set the **`Output Port`** field to **`Dupl.`**
5. Set the **`AFGEN1 TO`** and **`AFGEN2 To`** fields to **`Off (using the ON/OFF key).`**



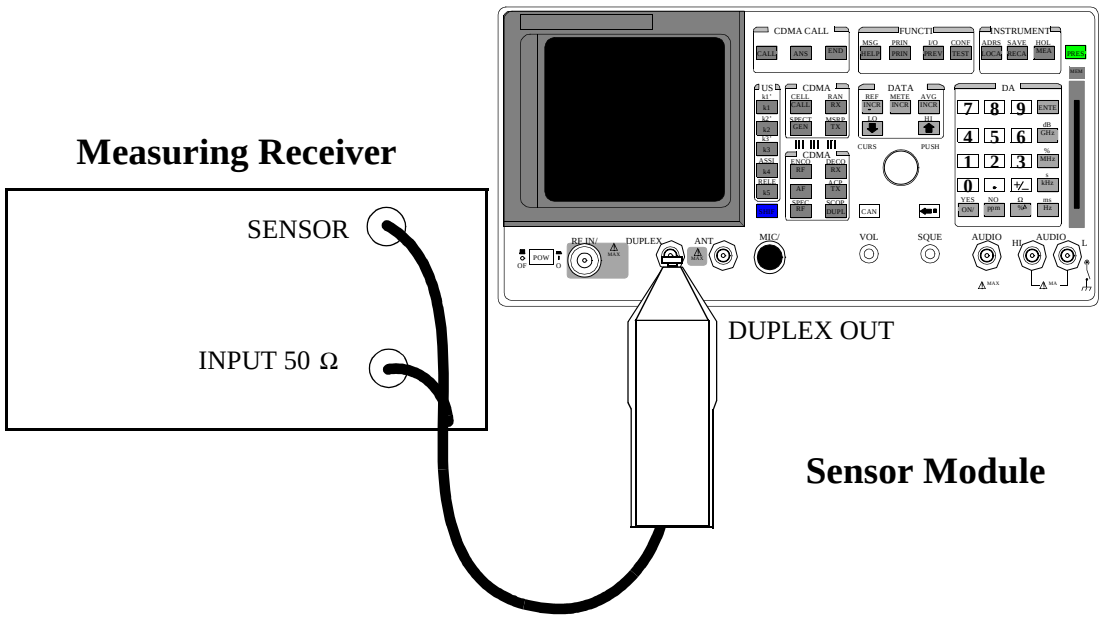
6. Measure the RF power at the frequencies and levels shown in the PTR (**see "RF Gen Duplex Output High Level Accuracy Performance Test 5" on page 314**) and compare the measured RF power to the limits shown in the PTR.

RF Gen Duplex Output Low Level Accuracy Performance Test 6

Description

The Duplex output is set to selected frequencies and to levels between 1 and –124 dBm (in 5 dB steps) and measured by the tuned RF level feature of the measuring receiver. As the test proceeds you may be required to recalibrate the measuring receiver.

Setup



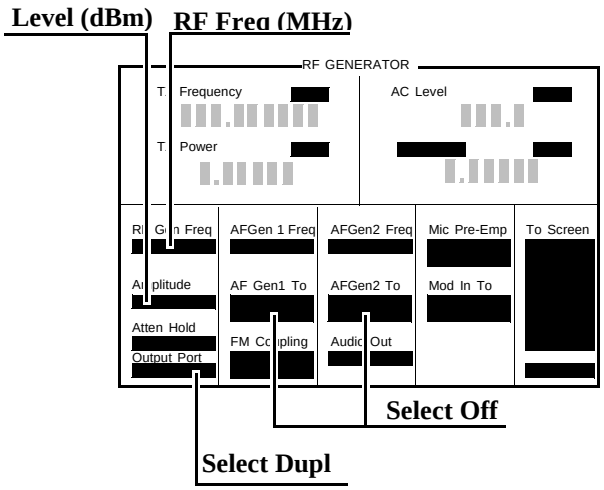
Make the following measuring receiver settings:

- Reset the measuring receiver
- Tuned RF Level power measurement
- Log display

NOTE: Make sure to enter the power sensor's calibration data into the measuring receiver and zero the power sensor. Refer to the measuring receiver's operating manual. The procedure for making tuned RF level measurements is also in the measuring receiver's manual.

Procedure

1. Access the CONFIGURE screen.
2. Change the **RF Display** field to **Freq**.
3. Select the RF GENERATOR screen.
4. Set the **Output Port** field to **Dupl**
5. Set the **AFGen1 To** and **AFGen2 To** fields to **Off**



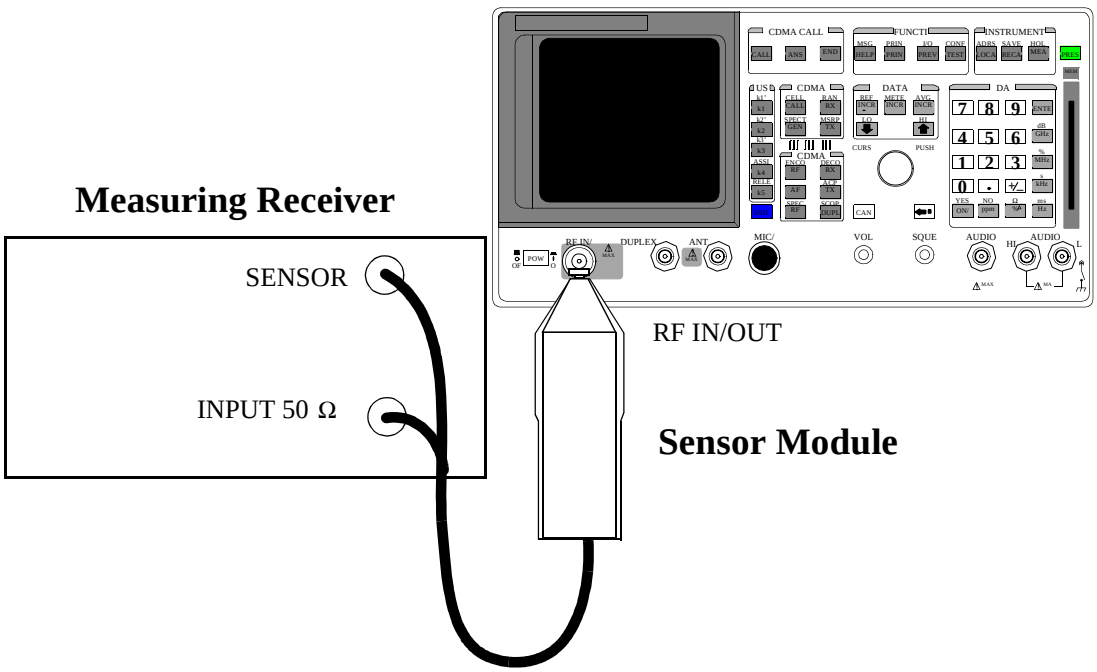
6. Measure the RF level at the frequencies and levels shown in the PTR (**see "RF Gen Duplex Output Low Level Accuracy Performance Test 6" on page 315**) and compare measured RF level to the limits shown in the PTR.

RF Gen RF IN/OUT Level Accuracy Performance Test 7

Description

The RF output is set to selected frequencies and to levels between –10.5 and –124 dBm (in 5 dB steps) and measured by the tuned RF level feature of the measuring receiver. As the test proceeds you may be required to recalibrate the measuring receiver.

Setup



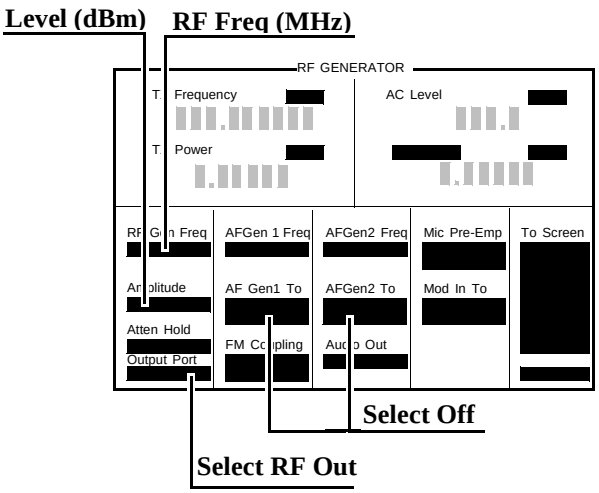
Make the following measuring receiver settings:

- Reset the measuring receiver
- Tuned RF Level power measurement
- Log display

NOTE: Make sure to enter the power sensor's calibration data into the measuring receiver, and zero the power sensor. Refer to the measuring receiver's operating manual. The procedure for making tuned RF Level measurements is also in the measuring receiver's manual.

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Select the RF GENERATOR screen.
4. Set the **`Output Port`** field to **`RF Out.`**
5. Set the **`AFGen1 To`** and **`AFGen2 To`** fields to **`Off.`**



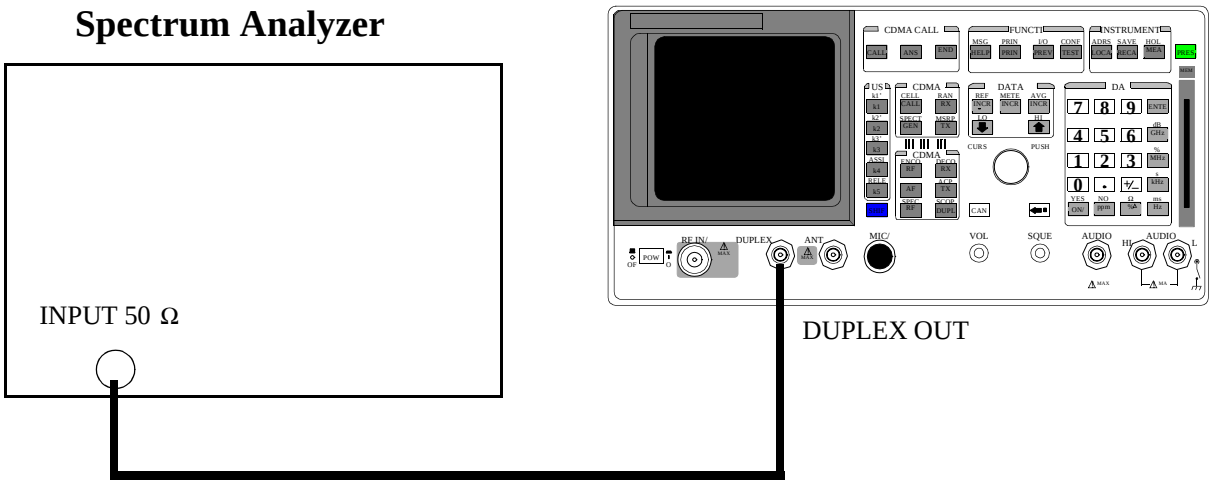
6. Measure the RF Level at the frequencies and levels shown in the PTR (**see "RF Gen RF IN/OUT Level Accuracy Performance Test 7" on page 319**) and compare the measured RF level to the limits shown in the PTR.

RF Gen Harmonics Spectral Purity Performance Test 8

Description

Harmonic signals with the carrier set to several frequencies and two different levels (maximum and minimum level vernier) are searched for by an RF spectrum analyzer.

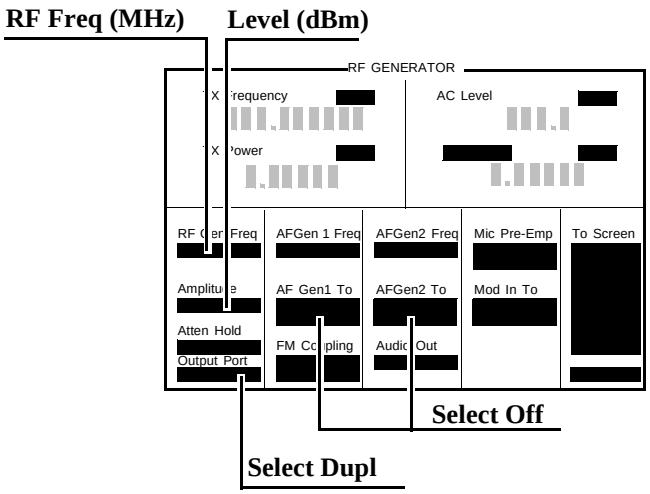
Setup



Refer to the spectrum analyzer's operating manual to set up the spectrum analyzer.

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Select the RF GENERATOR screen.
4. Set the **`Output Port`** field to **`Dupl`**.
5. Set the **`AFGen1`** and **`AFGen2`** levels to **`Off`**.



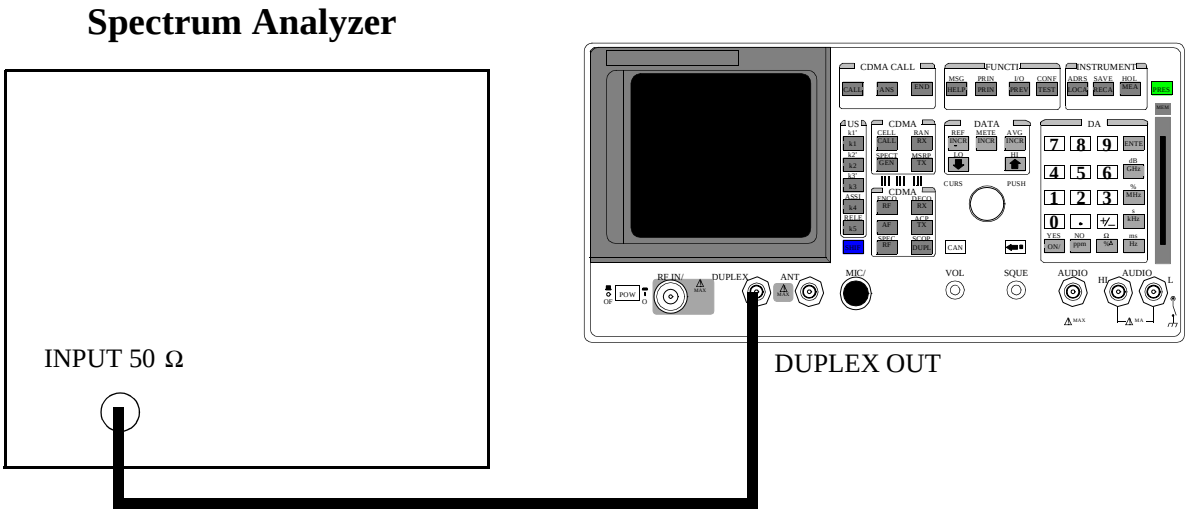
6. Set the Test Set to the RF Generator frequencies and level shown in the PTR (**see "RF Gen Harmonics Spectral Purity Performance Test 8" on page 323**), and measure the level of the second and third harmonics and the half-harmonics also shown in the PTR.
7. Convert the harmonic levels to decibels below the fundamental (dBc) and compare the computed levels to the limits shown in the PTR.

RF Gen Spurious Spectral Purity Performance Test 9

Description

Spurious signals with the carrier set to several frequencies and two different levels (maximum and minimum level vernier) are searched for by an RF spectrum analyzer.

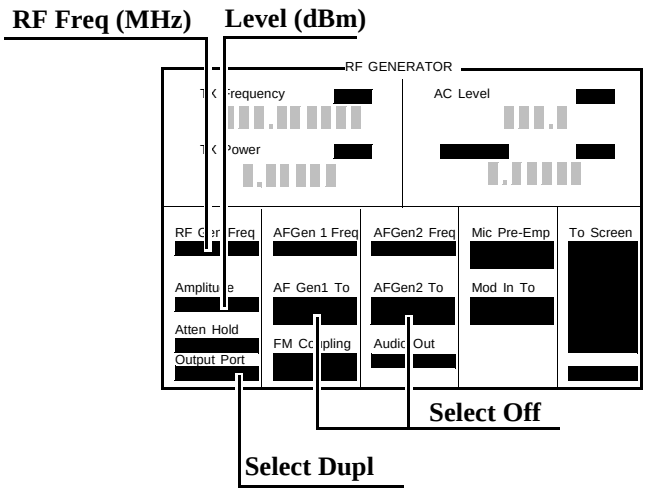
Setup



Refer to the spectrum analyzer's operating manual to set up the spectrum analyzer.

Procedure

1. Access the CONFIGURE screen.
2. Change the **`RF Display`** field to **`Freq`**.
3. Select the RF GENERATOR screen.
4. Set the **`Output Port`** field to **`Dupl`**.
5. Set the **`AFGen1`** and **`AFGen2`** levels to **`Off.`**



6. Set the Test Set to the RF Generator frequencies and levels (– 2.5 dBm or –4 dBm) shown in the PTR (**see "RF Gen Spurious Spectral Purity Performance Test 9" on page 327**), and measure the levels of the spurious signals at the frequencies shown in the PTR.
7. Convert the measured levels to decibels below the carrier (dBc), and compare the computed results to the limits shown in the PTR.

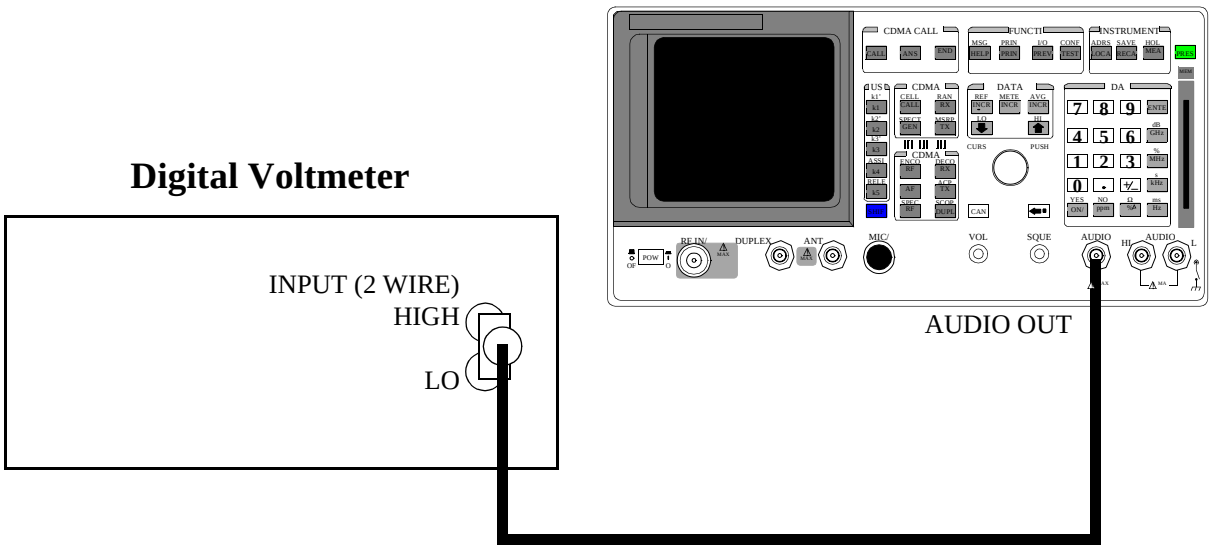
NOTE: Ignore the spur source column of the PTR. That information is for help in troubleshooting.

AF Gen AC Level Accuracy Performance Test 10

Description

There are two audio generators. AC level accuracy is measured directly by a digital voltmeter.

Setup

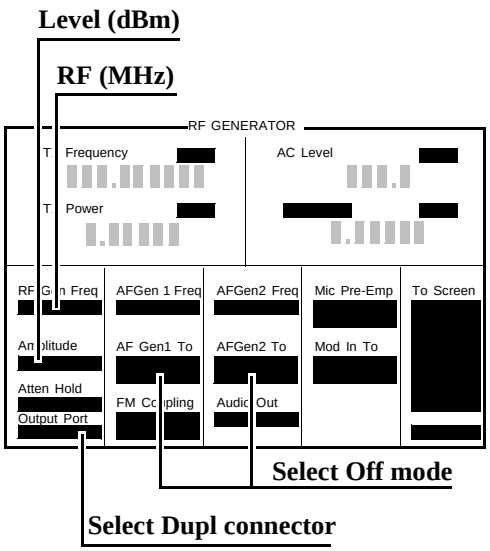


Make the following digital voltmeter setting:

- AC Volts

Procedure

1. Select the RF GENERATOR screen.
2. Set the Output Port field to RF Out.
3. Set the AFGen1 To and AFGen2 To fields to Off.



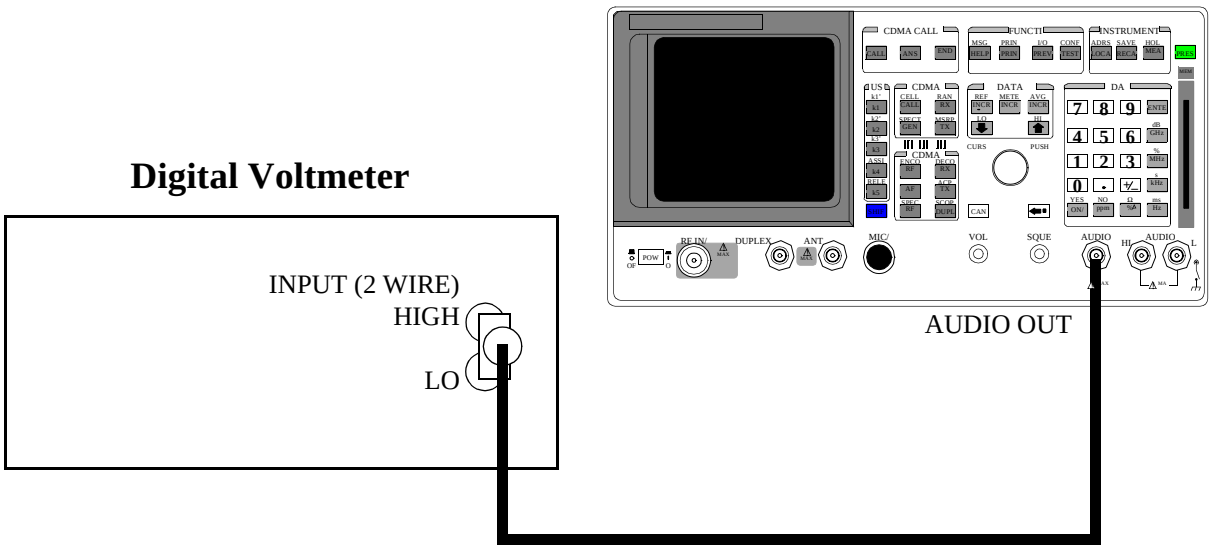
4. Measure the RF Level at the frequencies and levels shown in the PTR and compare the measured RF level to the limits shown in the PTR.

AF Gen DC Level Accuracy Performance Test 11

Description

There are two audio generators. DC level accuracy is measured directly by a digital voltmeter.

Setup

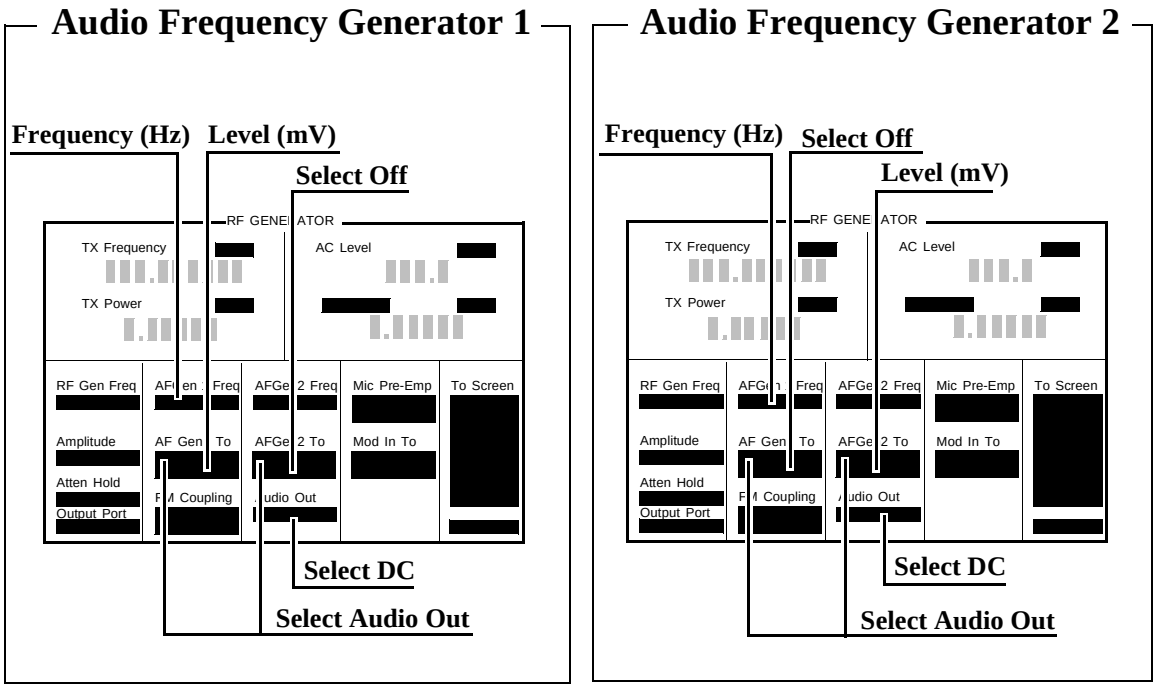


Make the following digital voltmeter setting:

- DC Volts

Procedure

1. Access the RF GENERATOR screen.
2. Set the **AFGen1 To** and **AFGen2 To** fields to **Audio Out.**
3. Set the **AFGEN1 Freq** and **AFGen2 Freq** fields to **0.0 Hz**.
4. Set the **Audio Out** field to **DC**.



5. Audio Frequency Generator 1: Set the AFGen2 level to **Off**. Measure the dc voltage at the levels shown in the PTR (**see "AF Gen DC Level Accuracy Performance Test 11" on page 331**) and compare the measured voltage to the limits shown in the PTR.

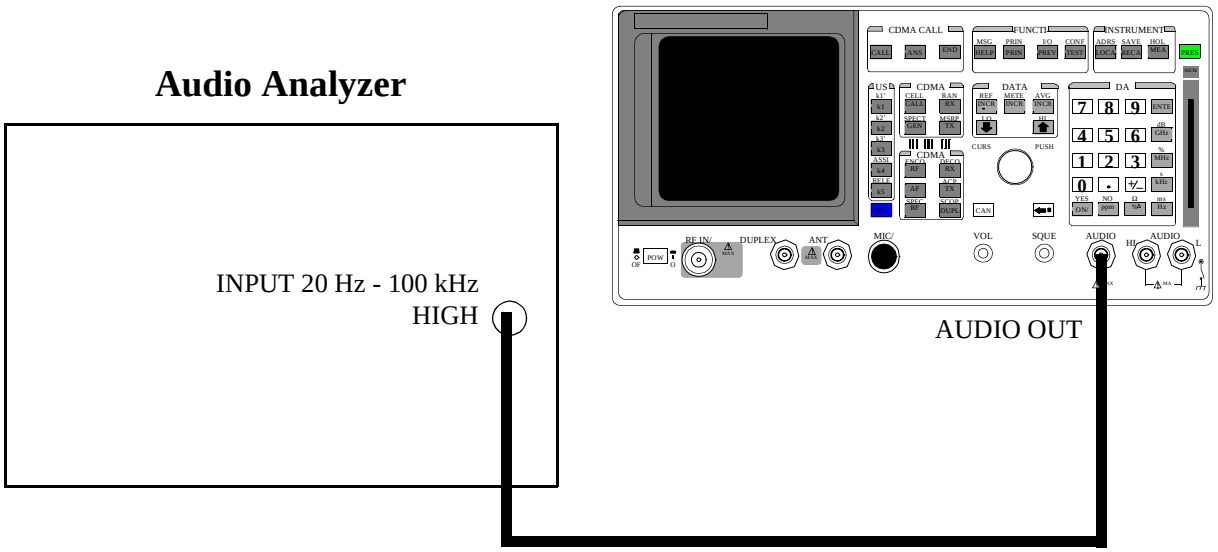
   Audio Frequency Generator 2: Set the AFGen1 level to **Off**. Measure the dc voltage at the levels shown in the PTR and compare the measured voltage to the limits shown in the PTR.

AF Gen Residual Distortion Performance Test 12

Description

Audio distortion is measured directly by an audio analyzer.

Setup

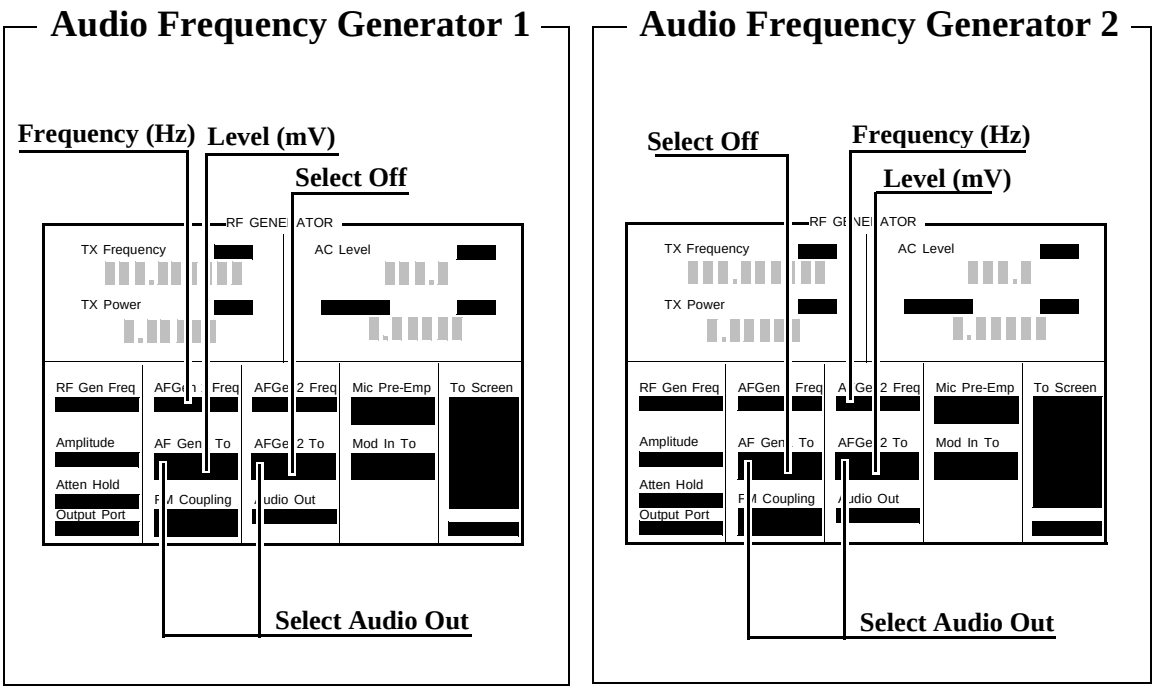


Make the following audio analyzer settings:

- Reset the audio analyzer
- 80 kHz Low-Pass Filter
- Distortion mode

Procedure

1. Access the RF GENERATOR screen.
2. Set the **`AFGen1 To`** and **`AFGen2 To`** fields to **`Audio Out`**.



3. Audio Frequency Generator 1: Set the AFGen2 level to **`Off`**. Measure the audio distortion at the frequencies and levels shown in the PTR (**see "AF Gen Residual Distortion Performance Test 12" on page 332**) and compare the measured distortion to the limits shown in the PTR.

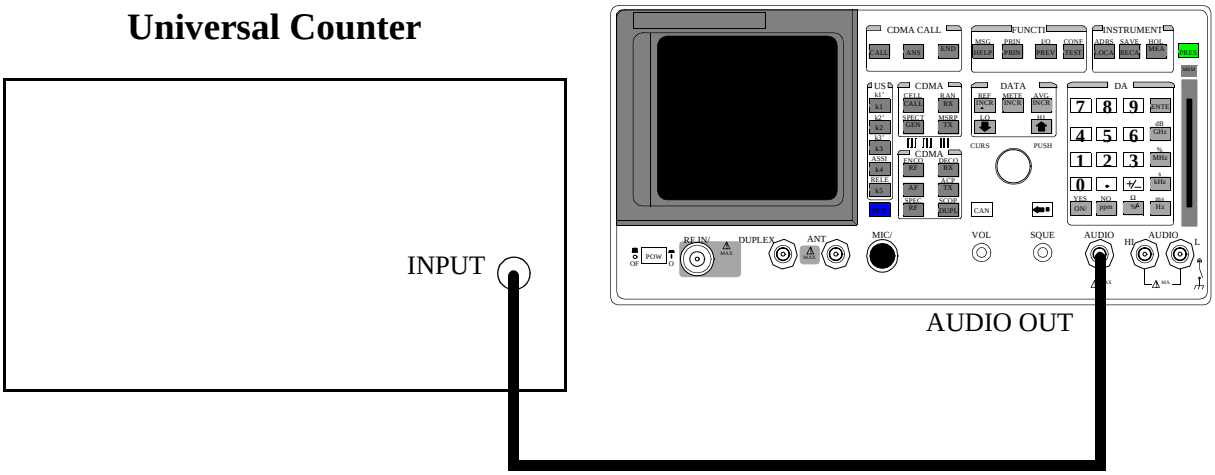
   Audio Frequency Generator 2: Set the AFGen1 level to **`Off`**. Measure the audio distortion at the frequencies and levels shown in the PTR and compare the measured distortion to the limits shown in the PTR.

AF Gen Frequency Accuracy Performance Test 13

Description

Frequency accuracy is measured directly by an audio frequency counter in the measuring receiver. The counter must be able to resolve 0.005% at 20 Hz. The counter in some audio analyzers lacks the resolution to do this.

Setup

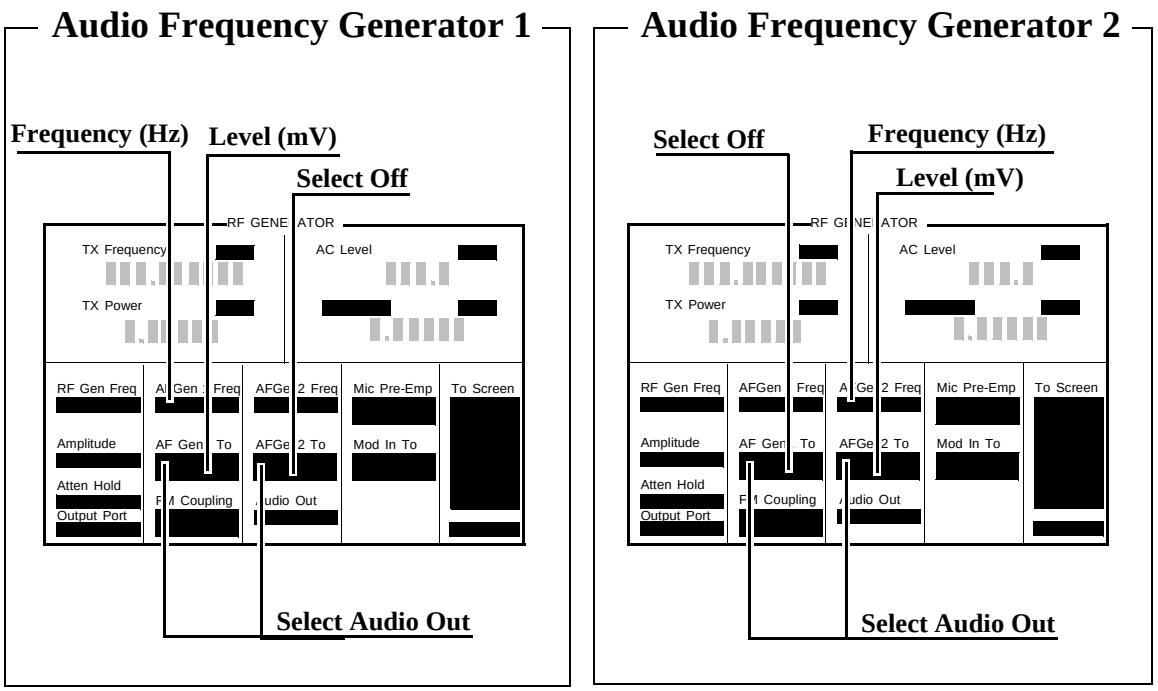


Make the following counter settings:

- Select frequency

Procedure

1. Access the RF GENERATOR screen.
2. Set the **`AFGen1 To`** and **`AFGen2 To`** fields to **`Audio Out.`**



3. Audio Frequency Generator 1: Set the AFGen2 to **`Off`**, and AFGen1 level to **`1 V`**. Measure the audio frequency at the frequencies shown in the PTR (**see "AF Gen Frequency Accuracy Performance Test 13" on page 334**) and compare the results to the PTR.

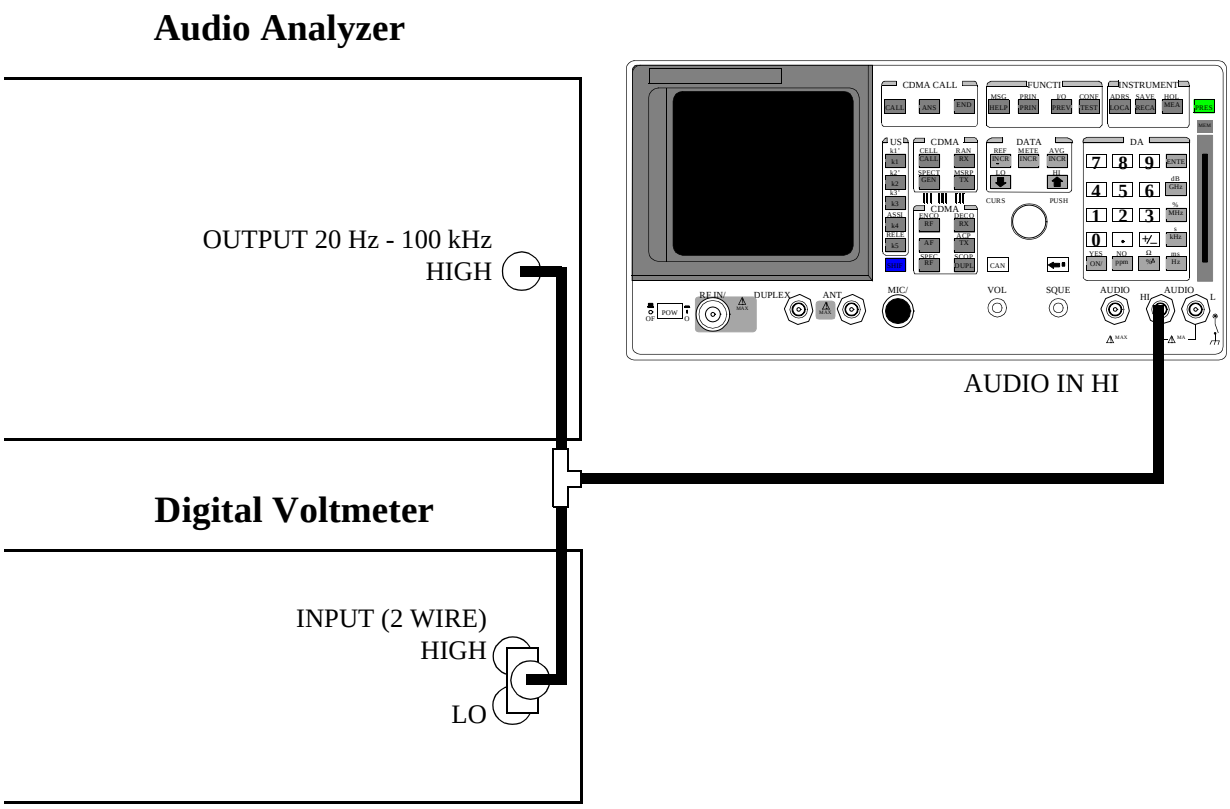
   Audio Frequency Generator 2: Set the AFGen1 to **`Off`**, and AFGen2 level to **`1 V`**. Measure the audio frequency at the frequencies shown in the PTR and compare the results to the PTR.

AF Analyzer AC Voltage Accuracy Performance Test 14

Description

To measure ac voltage accuracy, an ac signal is measured by an external multimeter and compared to the Test Set's internal ac voltmeter reading.

Setup

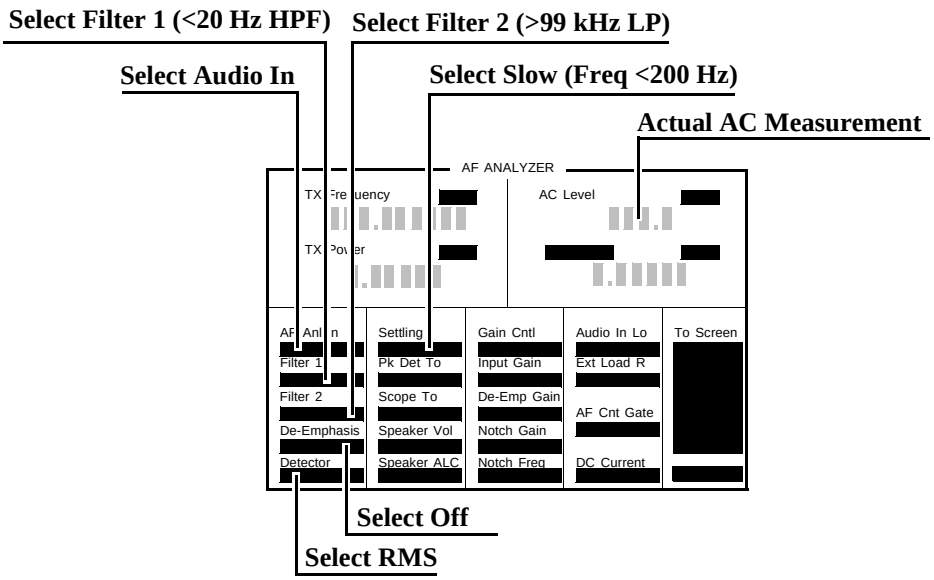


Make the following digital voltmeter setting:

- AC Volts

Procedure

1. Access the AF ANALYZER screen.
2. Set the **AF ANL In** field to **Audio In.**
3. Set **Filter 1** to **<20 Hz HPF**, and **set Filter 2** to **>99 kHz LP**.
4. Set the **De-Emphasis** field to **Off**.
5. Set the **Detector** field to **RMS**.
6. Set the **Settling** field to **SLOW** for frequencies < 200 Hz.



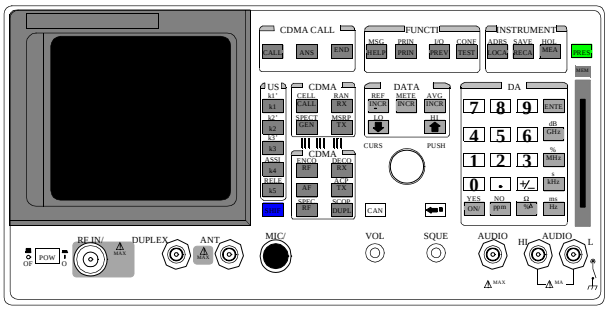
7. Set the audio analyzer's source to the frequencies and levels shown in the PTR (**see "AF Analyzer AC Voltage Accuracy Performance Test 14" on page 335**), adjust the level until the DVM reads the correct level.
8. Measure the ac level on the Test Set.
9. Compare the measured ac level to the limits shown in the PTR.

AF Analyzer Residual Noise Performance Test 15

Description

The ac level of the audio input is measured with no signal source connected.

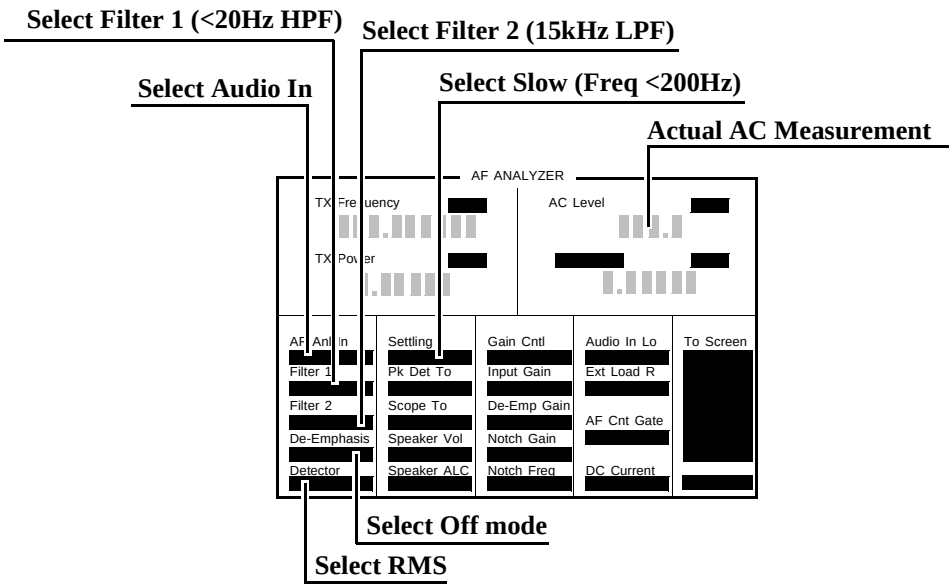
Setup



This test does not need external equipment or connections.

Procedure

1. Access the AF ANALYZER screen.
2. Set the **AF Anl In** field to **Audio In**.
3. Set the **AFGen1** and **AFGen2** deviation to **Off** (using the ON/OFF key).
4. Set **Filter 1** to **<20 Hz HPF** and **Filter 2** to **15 kHz LPF**.
5. Set the **De-Emphasis** field to **Off**.
6. Set the **Detector** field to **RMS**.



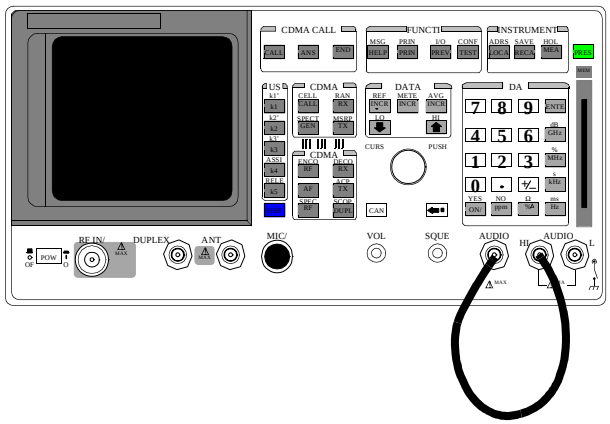
7. Measure ac level (Residual Noise). The upper limit is 150 µV. **See "AF Analyzer Residual Noise Performance Test 15" on page 336**.

AF Analyzer Distortion, SINAD, and SNR Accuracy Performance Test 16

Description

A calibrated distortion source is created by summing the two internal audio generators. Levels are measured separately by the internal ac voltmeter. One source is set to a harmonic two or three times the frequency of the other. The measured distortion is compared with the calculated value.

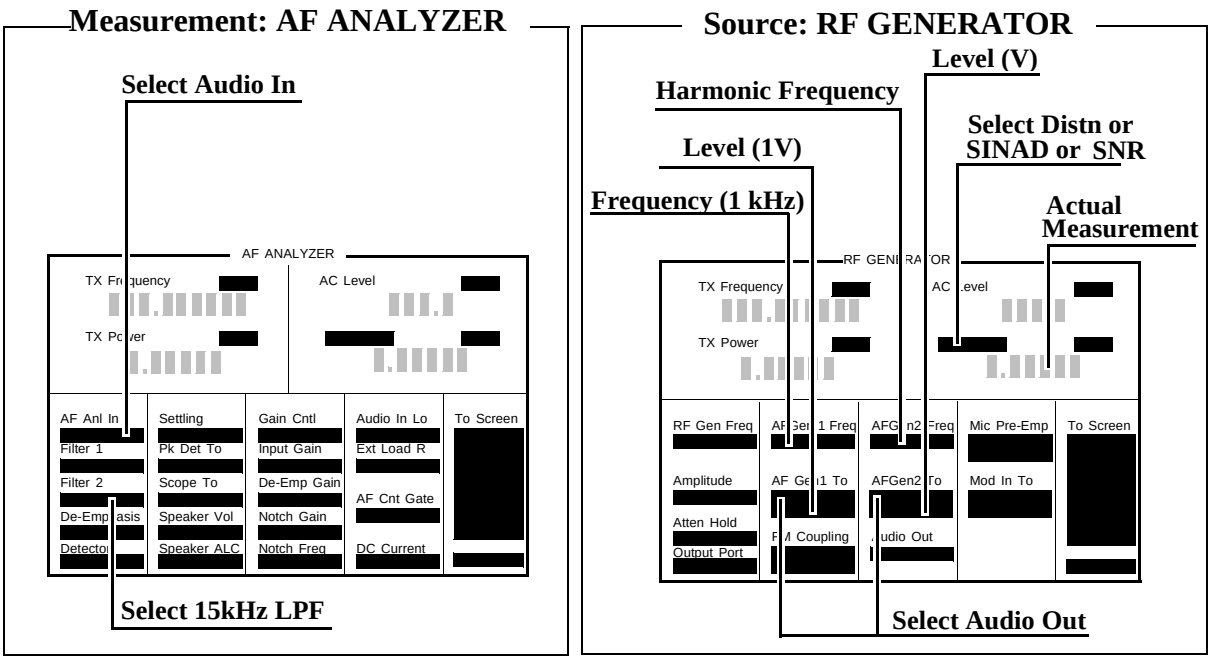
Setup



This test does not require external equipment.

Procedure

1. Access the AF ANALYZER screen and set **`Filter 2`** to **`15 kHz LPF`**.
2. Set the **`AF Anl In`** field to **`Audio In`**.
3. Access the RF GENERATOR screen and set the **`AF GEN 1 TO`** and **`AF GEN2`** to fields to **`Audio Out`**.



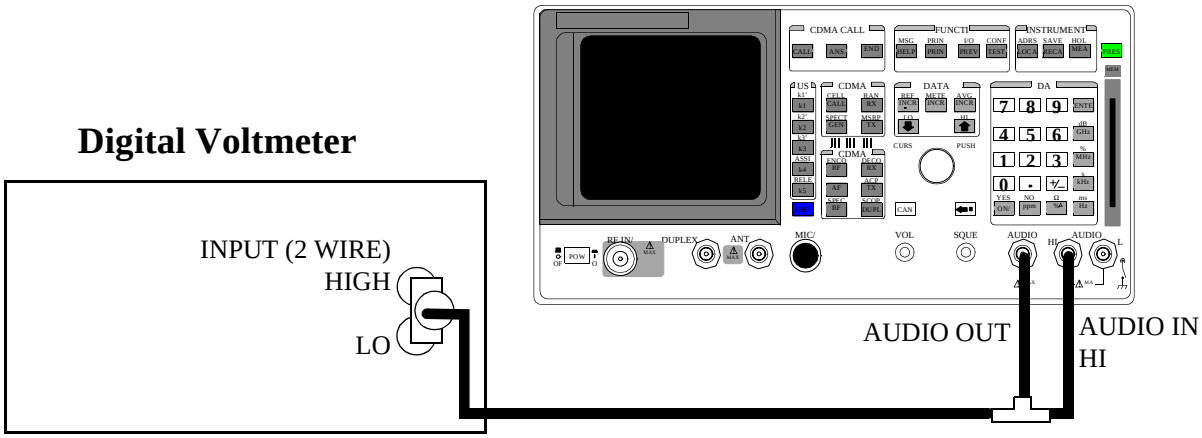
4. Set **`AFGen1 Freq`** to **`1 kHz`** and the **`AFGen1`** level to **`1 V`**.
5. Set **`AFGen2 Freq`** to the Harmonic frequencies shown in the PTR (**see "AF Analyzer Distortion, SINAD and SNR Accuracy Performance Test 16" on page 337**), and the **`AFGen2`** level to the distortion product levels shown in the PTR.
6. Measure the distortion and SINAD at each frequency and level, and compare the measured results with the limits shown in the PTR.
7. Measure the SNR (Signal to Noise Ratio) at each harmonic and level shown in the PTR. Compare the results to the limits shown in the PTR.

AF Analyzer DC Level Accuracy Performance Test 17

Description

To measure dc level accuracy, a dc signal is measured by an external digital voltmeter and compared to the Test Set's internal dc voltmeter reading.

Setup

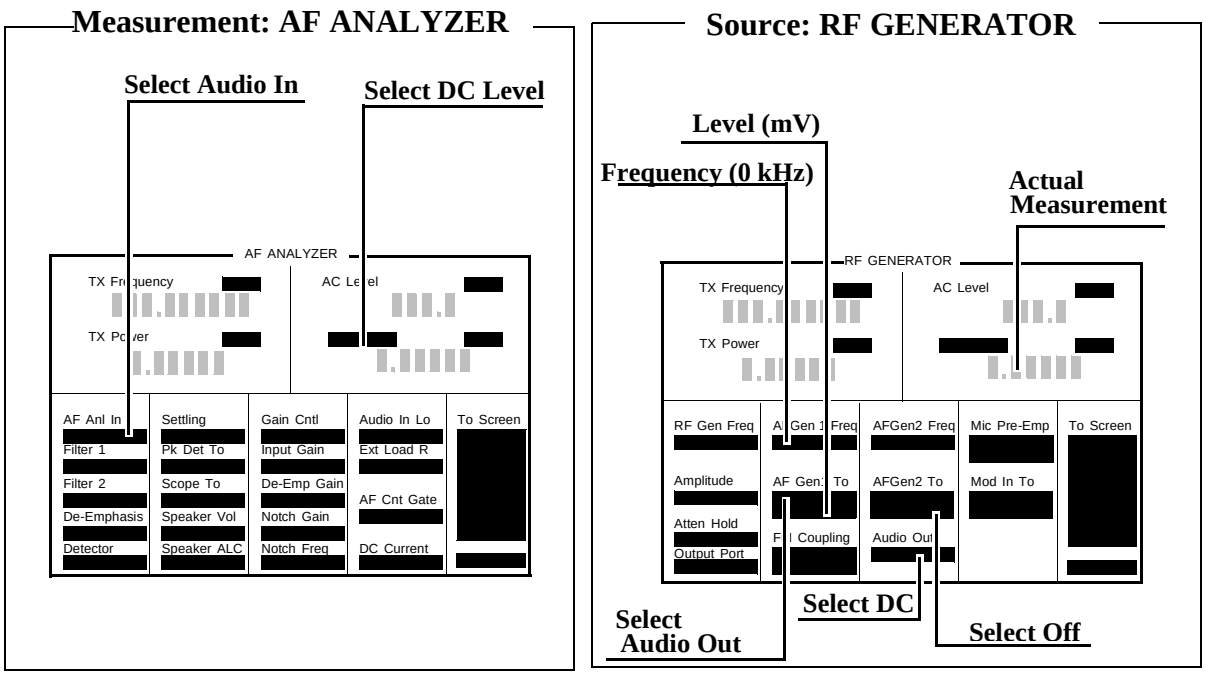


Make the following digital voltmeter setting:

- DC Volts

Procedure

1. Access the AF ANALYZER screen and set the **AF Anl In** field to **Audio In**.
2. Set the lower-right measurement to **DC Level**.
3. Access the RF GENERATOR screen and set the **AFGen1 Freq** field to **0 kHz.**



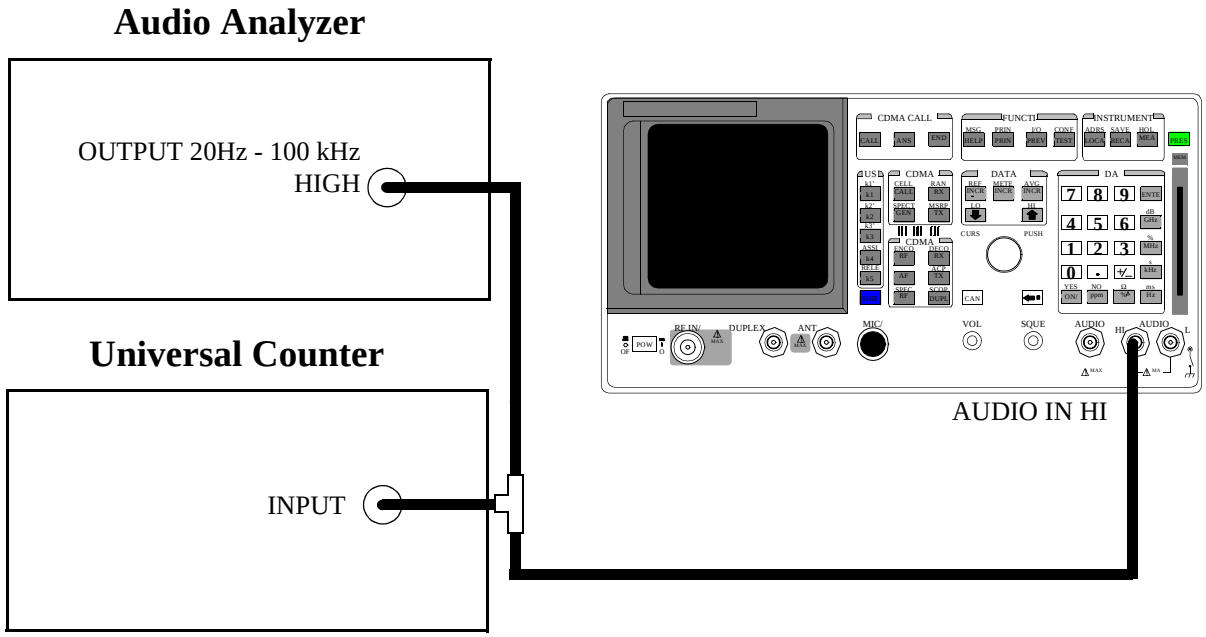
4. Set the **AFGen1 To** field to **Audio Out**, and set the **AFGen2 To** field to **Off.**
5. Set the **Audio Out** field to **DC**.
6. Set the **AFGen1** level to the levels shown in the PTR (**see "AF Analyzer DC Level Accuracy Performance Test 17" on page 339**), adjust until the voltmeter reads the correct level.
7. Read the DC Level and compare the reading to the limits shown in the PTR.

AF Analyzer Frequency Accuracy to 100 kHz Performance Test 18

Description

To measure frequency accuracy up to 100 kHz, an ac signal at the audio output is measured by the audio frequency counter in the measuring receiver and compared to the Test Set's internal audio frequency counter.

Setup

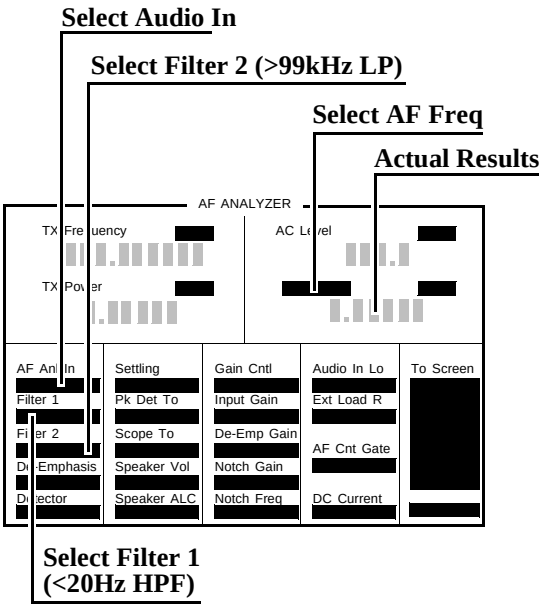


Make the following counter settings:

- Select Frequency

Procedure

1. Access the AF ANALYZER screen and set the **AF Anl In** field to **Audio In**.
2. Set the lower-right display to **AF Freq**.
3. Set **Filter 1** to **<20** and set **Filter 2** to **>99 Hz LP**.
4. Set the lower-right measurement display to **AF Freq**.



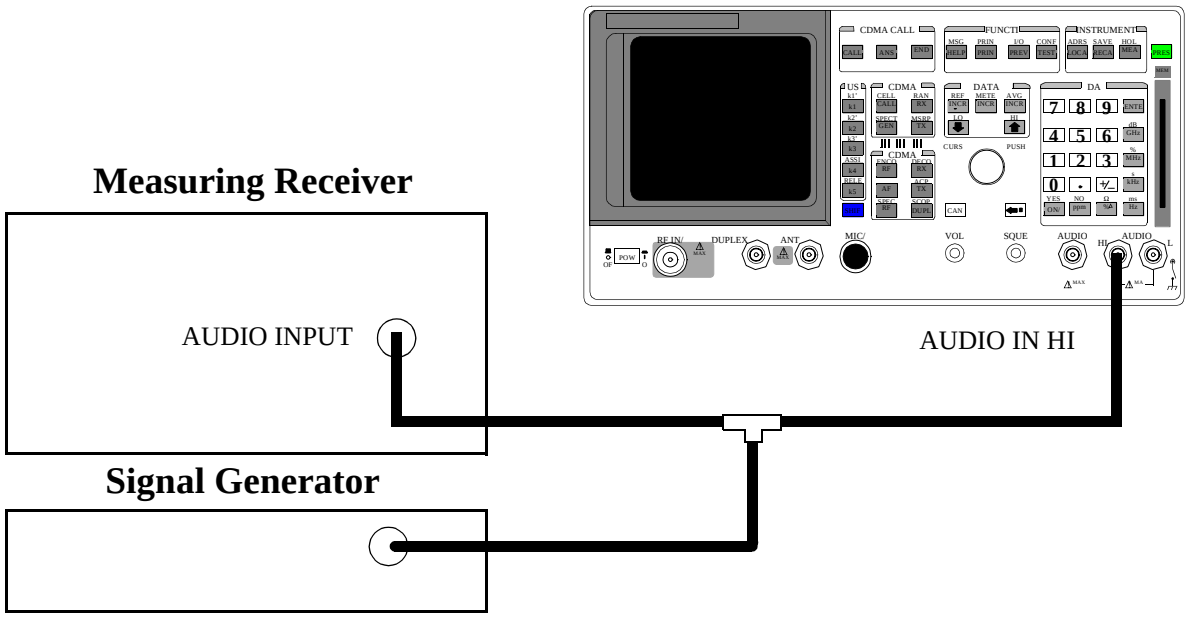
5. Set the audio analyzer's source amplitude to 1 V, and the frequency to the frequencies shown in the PTR (**see "AF Analyzer Frequency Accuracy to 100 kHz Performance Test 18" on page 340**), adjust until the audio frequency counter reads the correct frequencies.
6. Read the AF frequency on the measuring receiver and compare the reading to the limits shown in the PTR.

AF Analyzer Frequency Accuracy at 400 kHz Performance Test 19

Description

To measure the frequency accuracy at 400 kHz an ac signal from the Signal Generator is measured by the frequency counter in the measuring receiver and compared to the Test Set's internal RF counter.

Setup



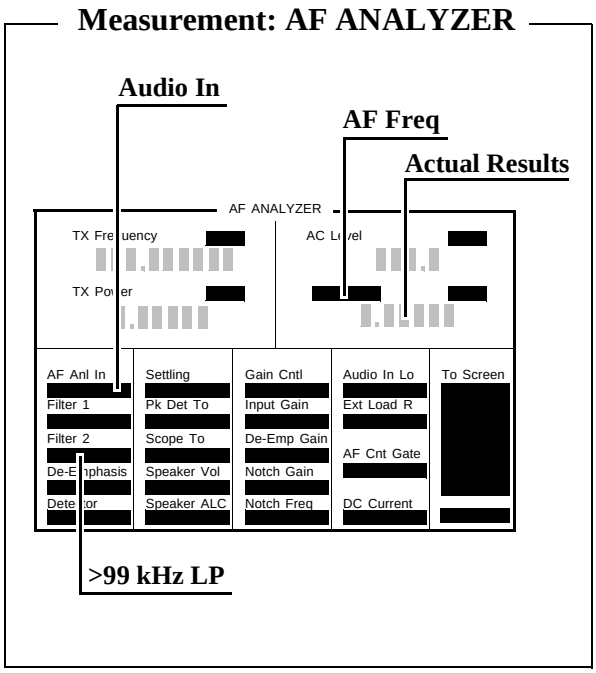
Make the following measuring receiver settings:

- Reset the measuring receiver
- Select Audio Freq
- Select Audio Input

Make the following Signal Generator settings:

- Amplitude 0 dBm
- Frequency 400 kHz

Procedure



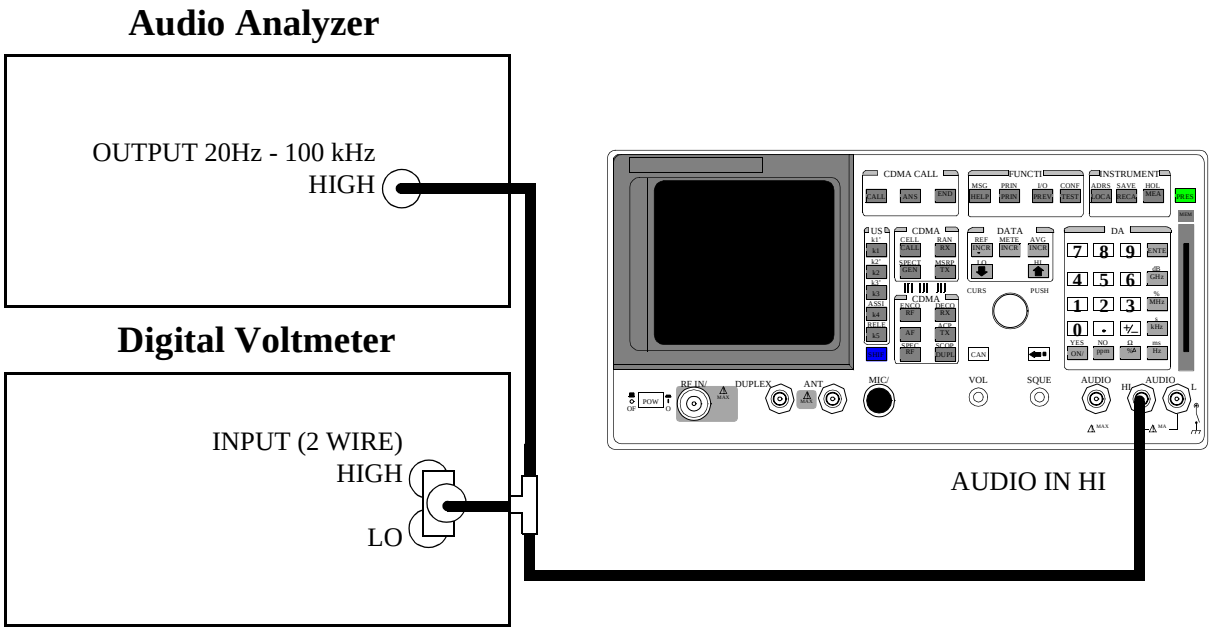
1. Access the AF ANALYZER screen, and set the **`AF Anl In`** field to **`Audio In`**.
2. Set the **`Filter 2`** field to **`>99 kHz LP`**, and the lower-right measurement field to **`AF Freq.`**
3. Read the **`AF Freq`** on the Test Set and compare the reading to the limits shown in the PTR (**see "AF Analyzer Frequency Accuracy at 400 kHz Performance Test 19" on page 341**).

Oscilloscope Performance Test 20

Description

A 5 V AC signal from the audio analyzer is measured by both an external AC voltmeter and the Test Set's internal AC voltmeter. The measurement results are compared. Since the external ac voltmeter measures the RMS level, its level is multiplied by the square root of two to obtain the peak value measured by the oscilloscope.

Setup

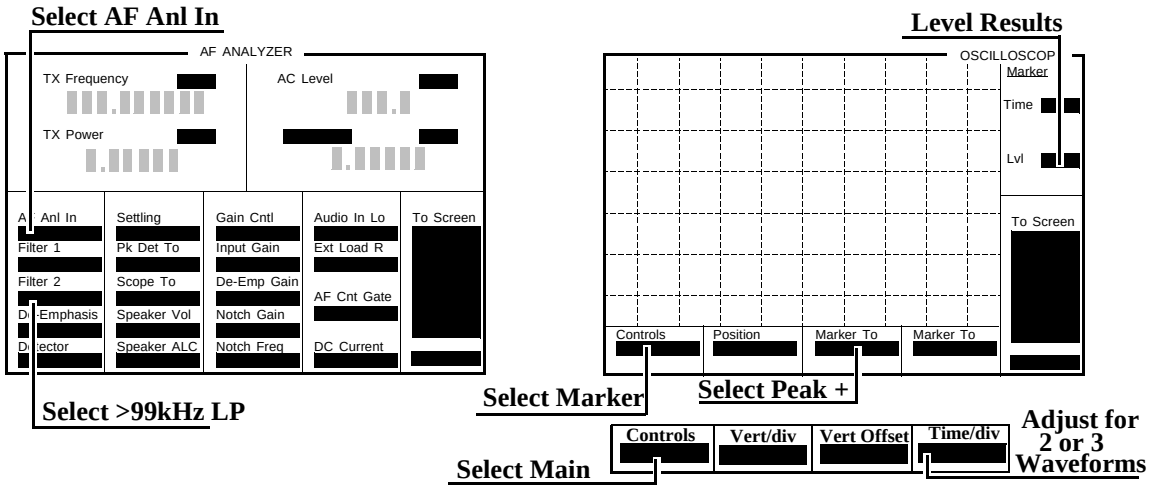


Make the following digital voltmeter setting:

- AC Volts

Procedure

1. Access the AF ANALYZER screen.
2. Set the **`Filter 2`** field to **`>99 kHz LP`**, and set the **`AF Anl In`** field to **`Audio In`**.
3. Access the OSCILLOSCOPE screen.



4. Adjust the audio analyzer's source until the digital voltmeter reads 5 V. Adjust the frequency to the frequencies shown in the PTR (**see "Oscilloscope Performance Test 20" on page 342**).
5. Adjust the **`Time/Div`** field to display 2 to 3 waveforms each time the frequency is changed. (The **`Time/Div`** field is displayed when the **`Controls`** field is set to **`Main`**.)
6. Set the **`Controls`** field to **`Marker`**. Select the **`Peak +`** field (located under **`Marker To`**) to move the marker to the peak of the waveform. Repeat this step each time the frequency is changed.
7. Read the **`Marker Lvl`** and compare the reading to the limits shown in the PTR.

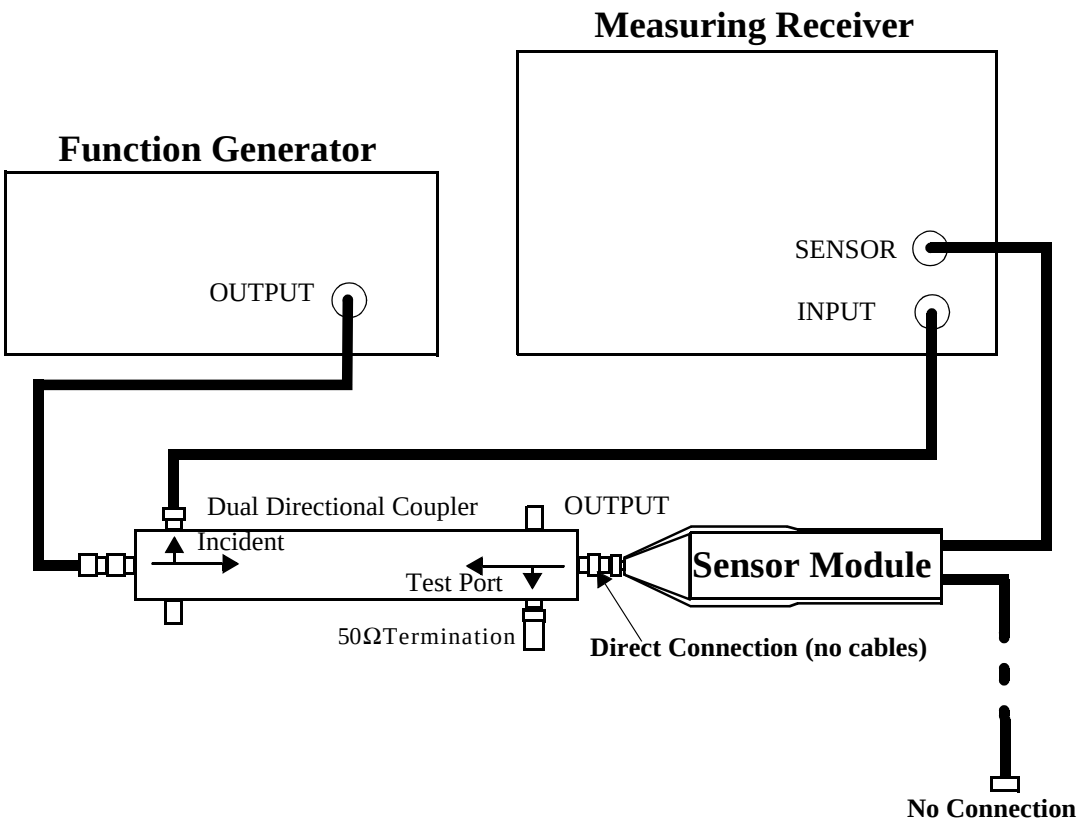
RF Analyzer Level Accuracy Performance Test 21

Description

A function generator's level is set to approximately 500 mW and measured with a power meter. Then, the power is measured with the unit-under-test, and the two measurements are compared.

A dual directional coupler is used to minimize mismatch uncertainty.

Calibration Setup



Make the following function generator settings:

- Frequency: 50 MHz
- Level: 14 V
- Waveform: Sine

NOTE: Make sure the function generator is warmed up so the frequency doesn't drift excessively during the measurement.

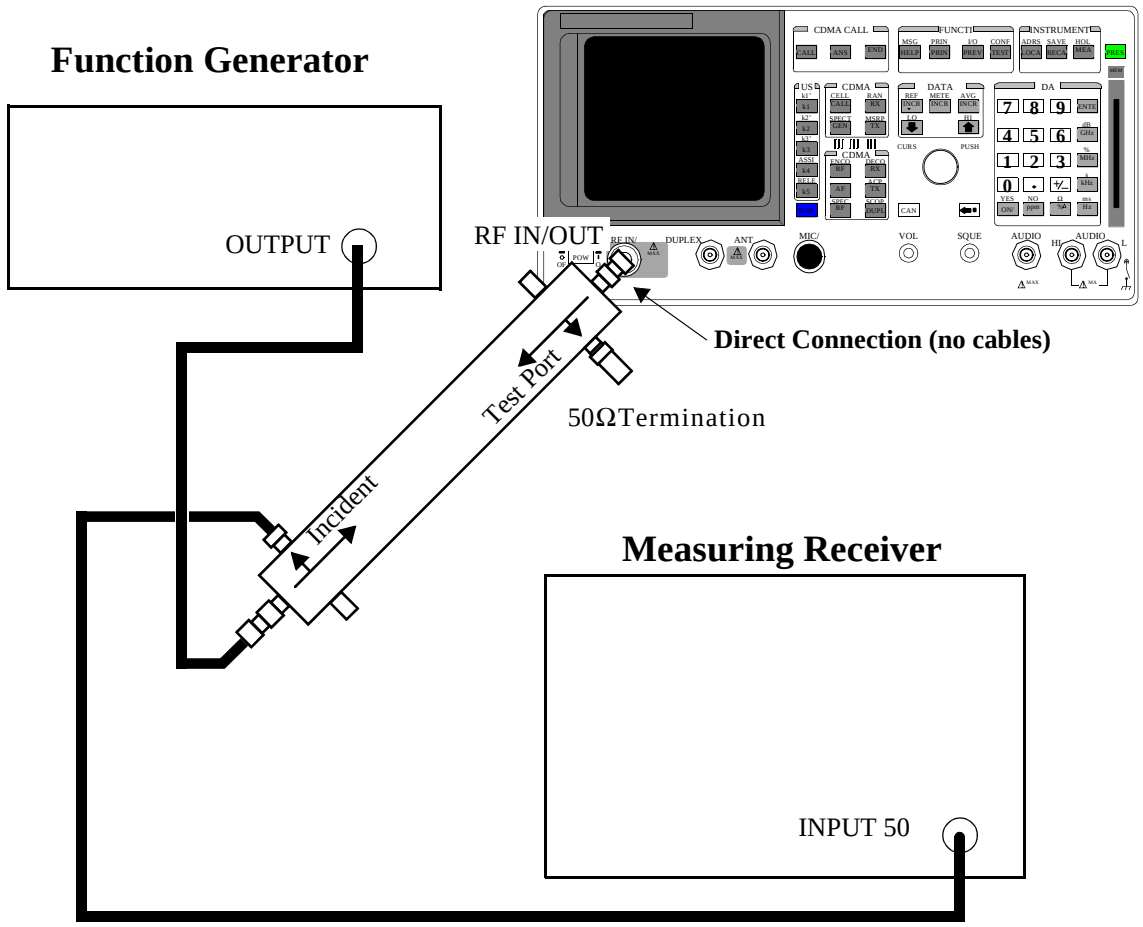
Make the following measuring receiver settings:

- Input frequency: 50 MHz
- Track mode
- RF Power measurement
- 4.4 SPCL
- 8.3 SPCL

Calibration Procedure

1. Make an RF POWER measurement, in watts, with the measuring receiver. Record the measured power as **`Reference power`** in step 10.
2. Disconnect the sensor cable at the measuring receiver (leave the sensor connected to the directional coupler so it will be terminated into 50 Ω).
3. Make a TUNED RF LEVEL measurement, in watts, with the measuring receiver. Record the measured level as **Tuned RF #1** in the *Measurement Procedure* in step 10.

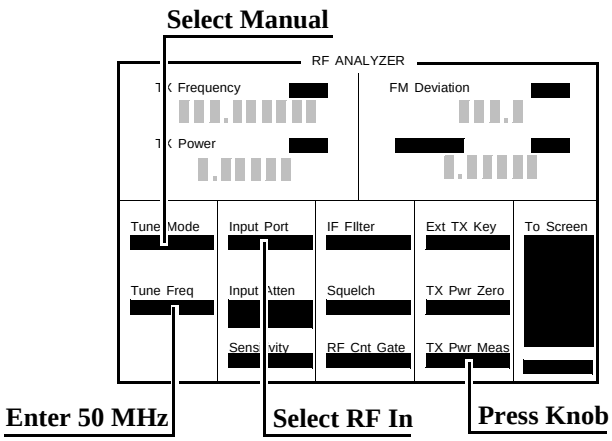
Measurement Setup



Measurement Procedure

1. After replacing the sensor module with the Test Set, make a TUNED RF LEVEL measurement, in watts, with the measuring receiver. Record the measured level as **Tuned RF #2** in step 10.
2. Access the CONFIGURE screen, and set the **`RF Display`** field to **`Freq`**.
3. Access the RF ANALYZER screen.
4. Set the **Tune Mode** field to **`Manual`**.

5. Set the **`Tune Freq`** field to **`50 MHz`**.
6. Set the **`Input Port`** field to **`RF In`**
7. Zero the power meter:
   - **a** Temporarily disconnect the Test Set from the coupler.
   - **b** Move the cursor to the **`TX Pwr Zero`** field and press the knob.



8. Re-connect the coupler directly to the Test Set's **RF IN/OUT** port (use no cables).
9. Read the **`TX Power`** field, in watts, and record it as **UUT Power** below.
10. Calculate the **Measured Power** as follows:

$$\text{Measured Power} = 500\text{mW}\left[\left(\frac{\text{UUT Power}}{\text{Reference Power}}\right)\left(\frac{\text{Tuned RF \#1}}{\text{Tuned RF \#2}}\right)\right]$$

The result is in mW. Record the results in the PTR (**see "RF Analyzer Level Accuracy Performance Test 21" on page 343**).

11. Set the Function Generator to 8.90 V.
12. Repeat the Calibration and Measurement procedures substituting 200 mW (in place of 500 mW) in the formula.

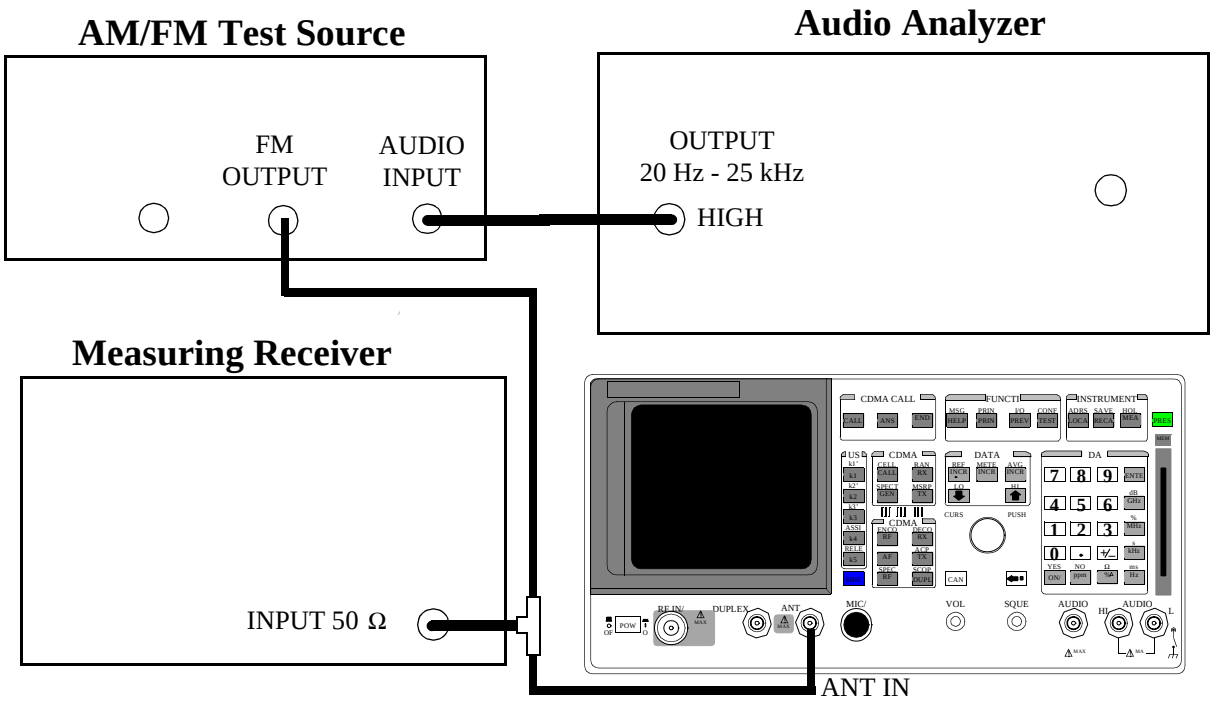
RF Analyzer FM Accuracy Performance Test 22

Description

A low noise/wide bandwidth AM/FM test source provides an RF carrier that is modulated by the audio analyzer's source. The signal is measured by the Test Set's internal RF analyzer and the measuring receiver's FM demodulator. The audio level is varied until the modulation is at the desired level as measured by the measuring receiver.

NOTE: Use the AM/FM test source output labeled **FM÷4** for 100 MHz and the output labeled **FM** for 400 MHz. You can measure the frequency with the measuring receiver and adjust it with the CARRIER FREQUENCY TUNE knob, but the exact frequency isn't critical.

Setup



Make the following AM/FM test source setting:

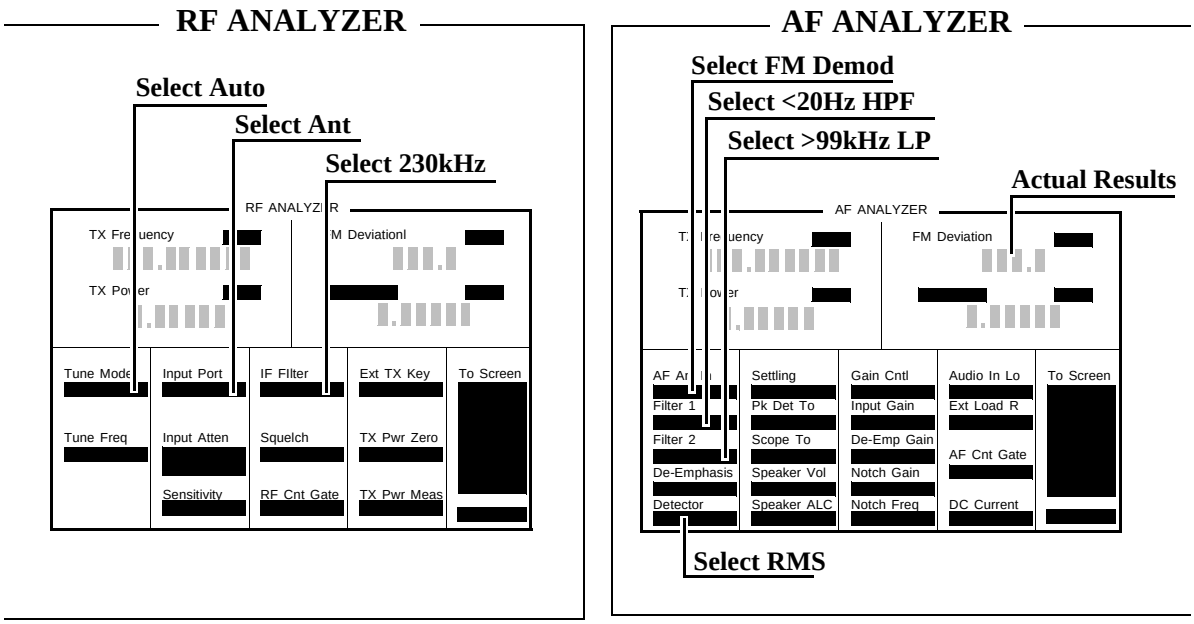
- Test Mode: FM

Make the following measuring receiver settings:

- Reset the measuring receiver
- FM Mode
- RMS Detector

Procedure

1. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
2. Access the RF ANALYZER screen, and set **Tune Mode** field to **Auto**.
3. Set the **Input Port** field to **Ant**, and the **IF Filter** field to **230kHz.**
4. Access the AF ANALYZER screen, and set the **AF Anl In** field to **FM Demod**.



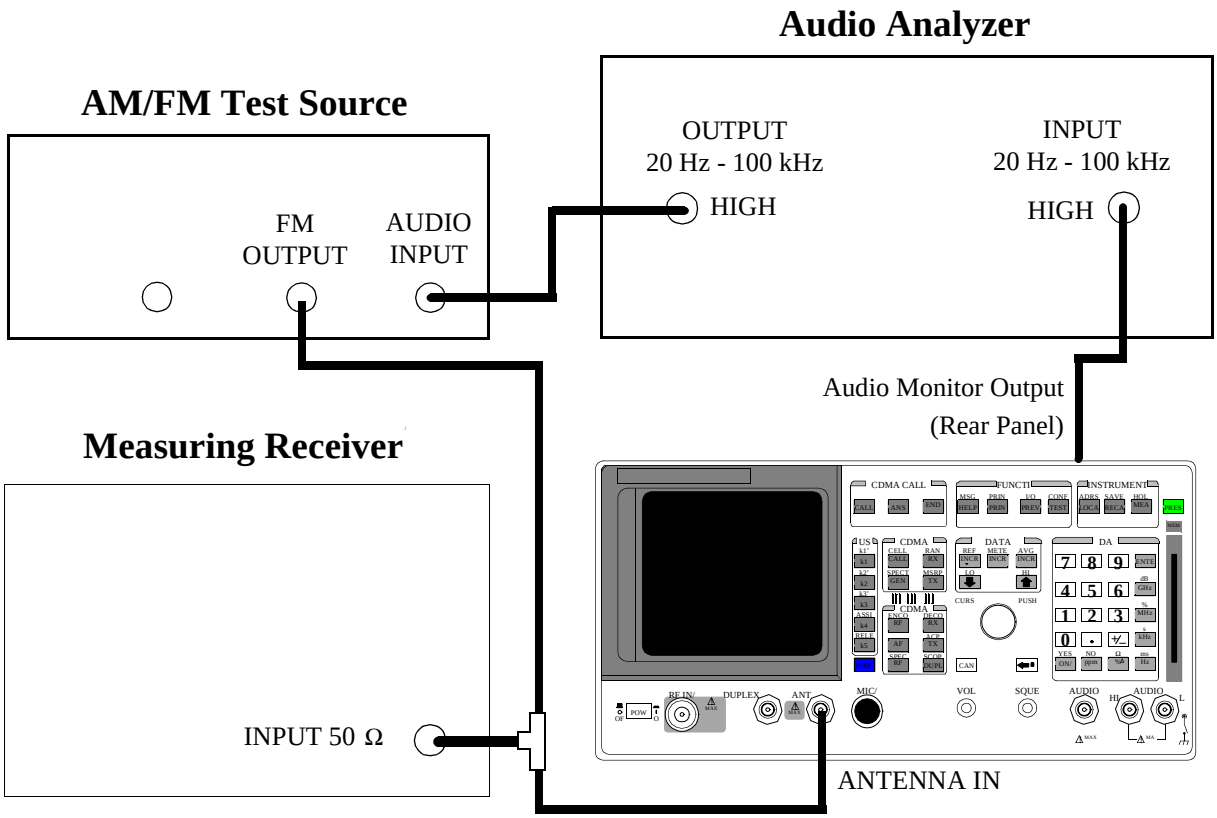
5. Set the **Filter 1** field to **<20 Hz HPF**, and set the **Filter 2** field to **>99 kHz LP**.
6. Set the **Detector** field to **RMS**.
7. Set the audio analyzer to the frequency (audio rate) shown in the PTR (**see "RF Analyzer FM Accuracy Performance Test 22" on page 344**). Adjust the audio analyzer's amplitude until the measuring receiver reads the correct deviation.
8. Read the FM Deviation on the Test Set, and compare it to the limits shown in the PTR.

RF Analyzer FM Distortion Performance Test 23

Description

A low-noise/wide-bandwidth AM/FM test source provides an RF carrier that is modulated by the audio analyzer's source. The signal is measured by the Test Set's internal RF analyzer and the measuring receiver. The audio level is varied until the modulation is at the desired FM deviation as measured by the measuring receiver. The distortion of the demodulated FM is measured by the external audio analyzer.

Setup



Make the following AM/FM test source setting:

- Test Mode: FM

Make the following measuring receiver settings:

- Reset the measuring receiver
- FM Mode
- 300 Hz High-Pass Filter
- 3 kHz Low-Pass Filter

Make the following audio source setting in the audio analyzer:

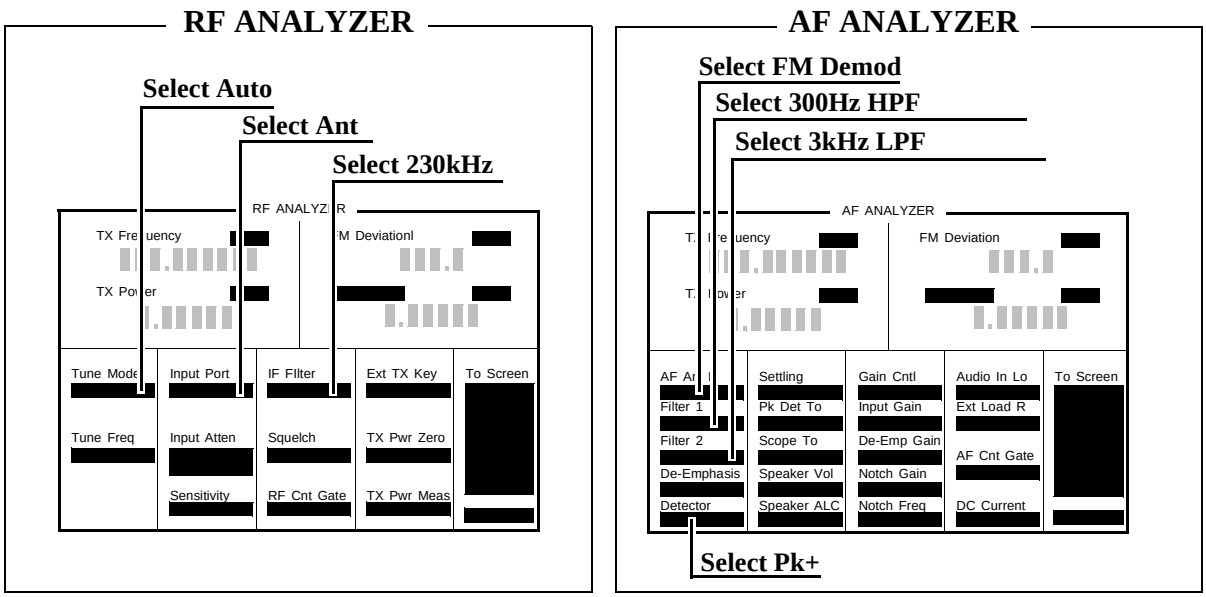
- Frequency: 1 kHz

Make the following audio analyzer setting:

- Distortion

Procedure

1. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
2. Access the RF ANALYZER screen, and set the **Tune Mode** field to **Auto**.
3. Set the **Input Por**t field to **Ant**, and set the **IF Filter** field to **230 kHz**.
4. Access the AF ANALYZER screen, and set the **AF Anl In** field to **FM Demod**..



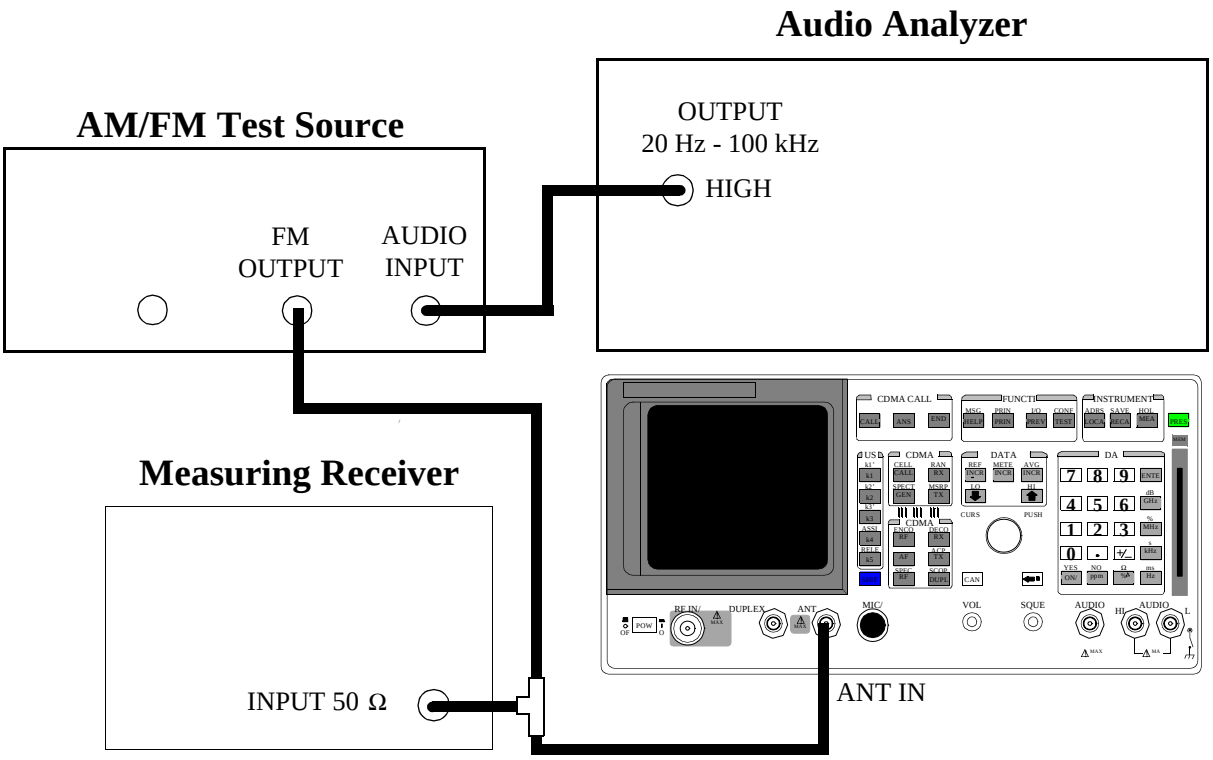
5. Set the **Filter 1** field to **300 Hz HPF**, and set the **Filter 2** field to **3 kHz LPF**.
6. Set the **Detector** field to **Pk+**.
7. Adjust the amplitude of the audio analyzer's source until the deviation displayed on the measuring receiver matches the deviation shown in the PTR (**see "RF Analyzer FM Distortion Performance Test 23" on page 345**).
8. Read the distortion on the audio analyzer and compare the reading to the limits shown in the PTR.

RF Analyzer FM Bandwidth Performance Test 24

Description

A low noise/wide bandwidth AM/FM test source provides an RF carrier that is modulated by the audio analyzer's source. The signal is measured by the Test Set's internal RF analyzer and the measuring receiver. The audio level is varied until the modulation is at the desired level as measured by the measuring receiver. The audio rate is varied in several steps from 20 Hz to 70 kHz. The difference between the maximum and minimum FM peak deviation is noted.

Setup



Make the following AM/FM test source setting:

- Test Mode: FM

Make the following measuring receiver settings:

- Reset the measuring receiver
- FM Mode
- Filters off

Make the following audio analyzer settings:

- Frequency: 1 kHz
- Impedance: 50 [ohm]
- Amplitude: 50 mV

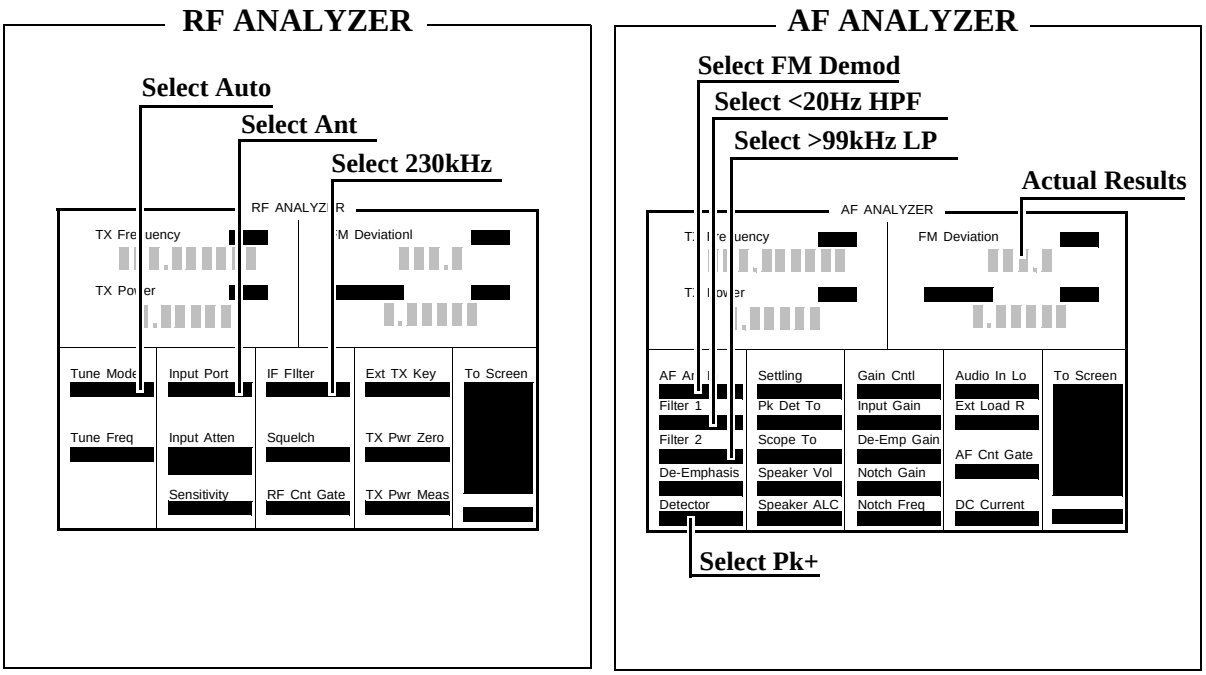
OR

- Frequency: 1 kHz
- Impedance: 600 [ohm]
- Amplitude: 300 mV

These settings should result in a deviation reading of about 25 kHz on the measuring receiver. Adjust the amplitude for 25 kHz deviation as read on the measuring receiver.

Procedure

1. Access the CONFIGURE screen, and set the **`RF Display`** field to **`Freq`**.
2. Access the RF ANALYZER screen, and set the **`Tune Mode`** field to **`Auto.`**
3. Set the **`Input Port`** field to **`Ant`**, and set the **`IF Filter`** field to **`230kHz`**.
4. Set the front-panel SQUELCH control full counter-clockwise (open).
5. Allow the Test Set to tune to the input signal, and then set the **`Tune Mode`** field to **`Manual`**.
6. Access the AF ANALYZER screen, and set the **`AF Anl In`** field to **`FM Demod`**. ,



7. Set the **Filter 1** field to **<20 Hz HPF**, and set the **Filter 2** field to **>99 kHz LPF.**
8. Set the **Detector** field to **Pk+**.
9. Set the audio analyzer to the following frequencies and record the FM deviation displayed on the measuring receiver for each frequency (check the deviation measured by the measuring receiver at each frequency and adjust the audio analyzer amplitude if needed to make sure it is 25 kHz): **20 Hz, 100 Hz, 1000 Hz, 10 000 Hz, 35 000 Hz, 70 000 Hz**.
10. The result of this test is the ratio of the maximum to the minimum measured deviation. Calculate the ratio in dB as follows:

$$\text{Result (dB)} = 20\log\frac{\text{max. deviation}}{\text{min. deviaiton}}$$

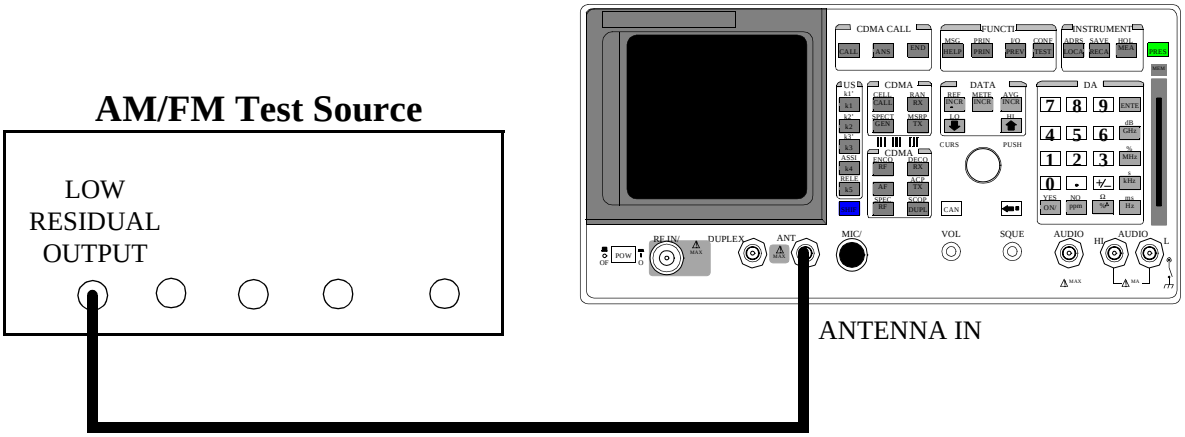
The test limit is max 3 dB. **See "RF Analyzer FM Bandwidth Performance Test 24" on page 346**.

RF Analyzer Residual FM Performance Test 25

Description

The AM/FM test source provides a CW signal with minimal residual FM. The FM is measured by the Test Set's internal RF analyzer.

Setup

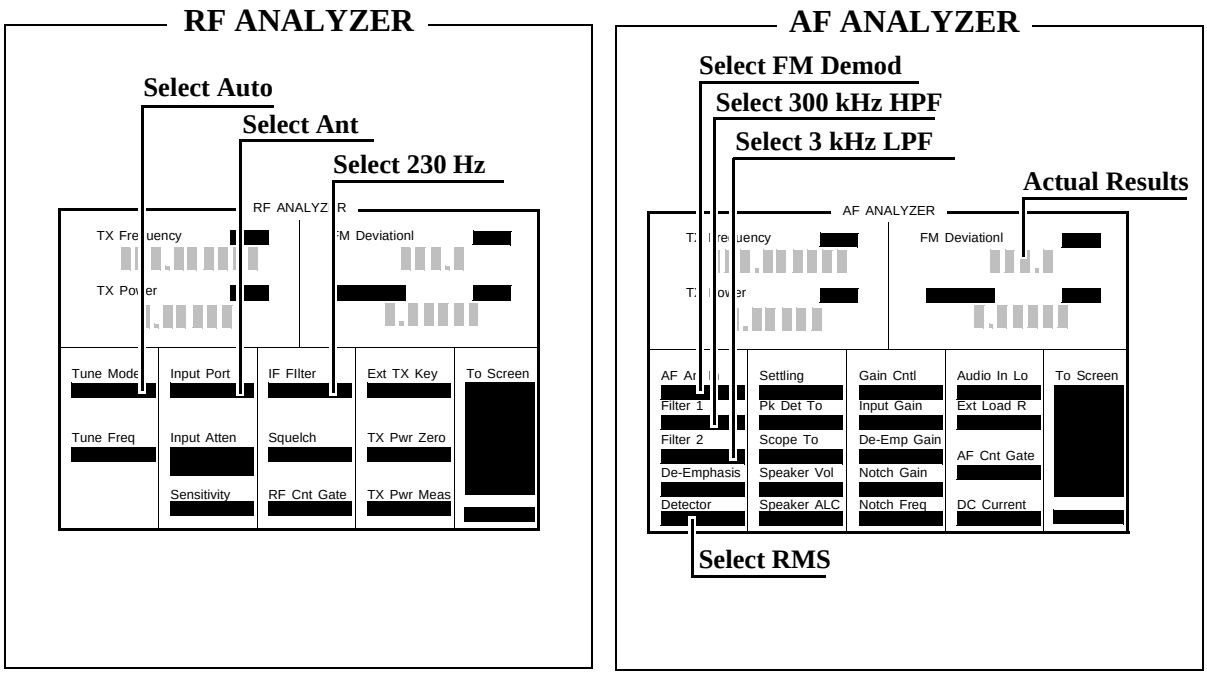


Make the following AM/FM test source setting:

- Test Mode: Residual FM

Procedure

1. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
2. Access the RF ANALYZER screen, and set the **Tune Mode** field to **Auto**.
3. Set the **Input Port** field to **Ant**, and the **IF Filter** field to **230 kHz**.
4. Access the AF ANALYZER screen, and set the **AF Anl In** field to **FM Demod**.
5. Set the **Filter 1** field to **300 Hz HPF**, and set the **Filter 2** field to **3 kHz LPF**.
6. Set the **Detector** field to **RMS**.



7. Read the FM Deviation (residual FM) and compare to the limits shown in the PTR (see "RF Analyzer Residual FM Performance Test 25" on page 347).

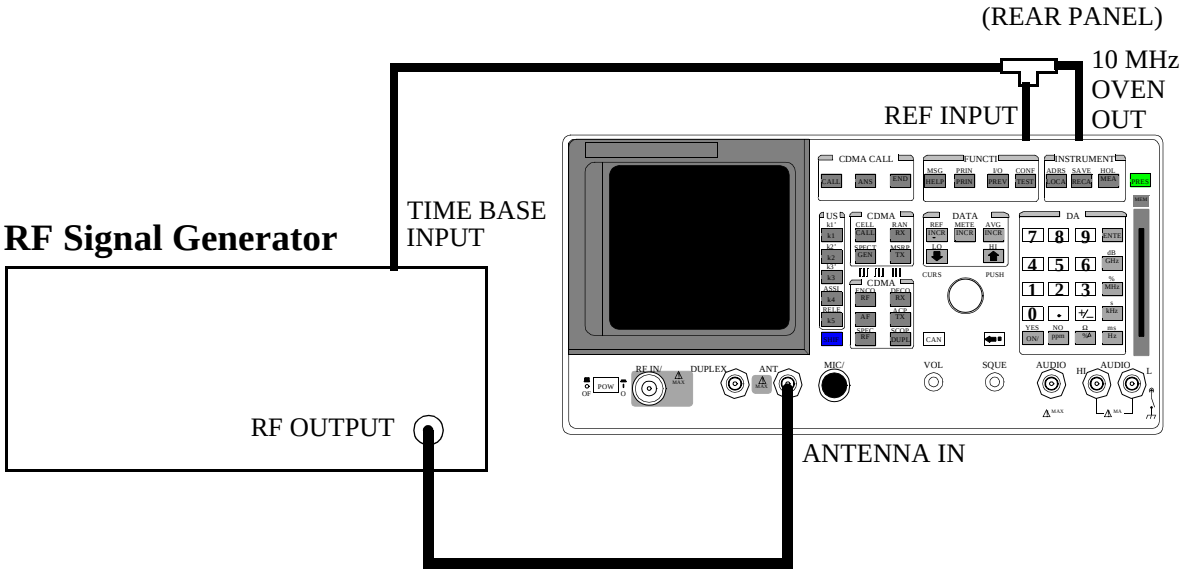
Spectrum Analyzer Image Rejection Performance Test 26

Description

This test has two parts. The first part measures the spectrum analyzer's ability to reject image frequencies. The spectrum analyzer is tuned to a signal frequency while an image signal is applied to the ANTENNA IN connector from a signal generator.

The second part measures the spectrum analyzer's residual response at several frequencies.

Setup

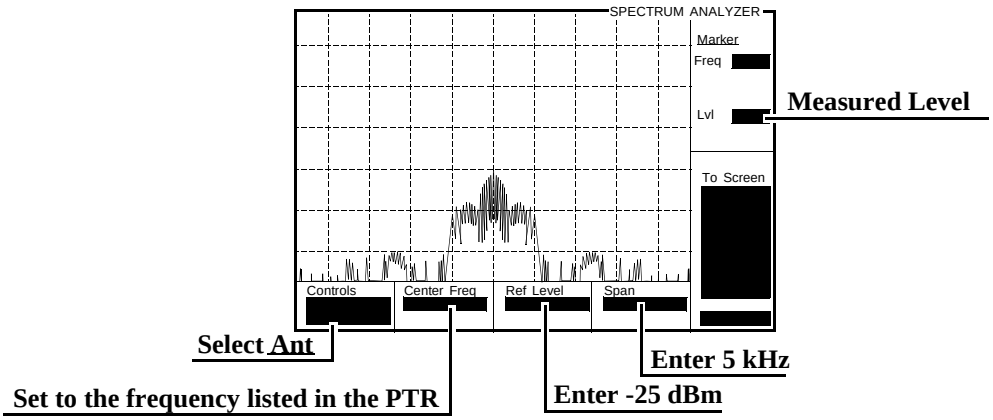


Make the following signal generator settings:

- Power: –20 dBm
- Modulation: OFF

Image Rejection Procedure

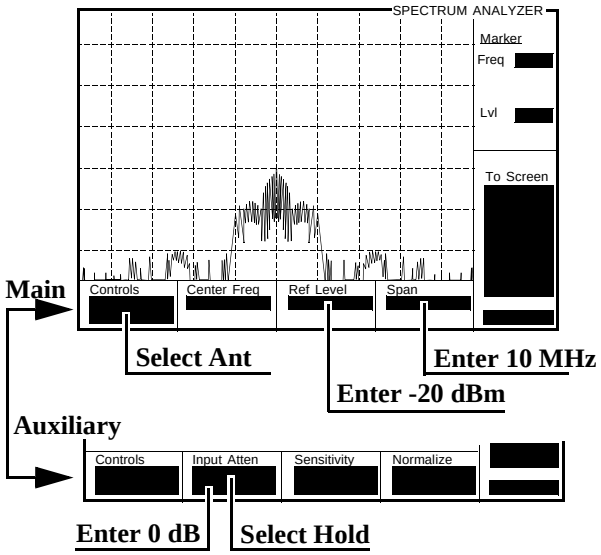
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen, and set the **`RF Display`** field to **`Freq`**.
3. Access the SPECTRUM ANALYZER screen.
4. Set the **`RF In/Ant`** field to **`Ant`**.
5. Set the **`Ref Level`** field to **`–25 dBm`**.
6. Set the **`Span`** field to **`5 kHz`**.



7. Set the signal generator's frequency, and the spectrum analyzer's **`Center Freq`** field, to the frequencies shown in the PTR (**see "Image Rejection" on page 348**). The image response is the spectrum analyzer's marker level plus the signal generator's output level (-20 dBm).

Residual Response Procedure

1. Disconnect the signal generator from the Test Set's ANTENNA IN connector.
2. Set the **Controls** field to **Auxiliary,** and set the **Input Atten** field to **Hold** and **0 dB**.
3. Set the **Controls** field to **Main.**
4. Set the **Span** field to **10 MHz**.
5. Set the **Ref Level** field to **-20 dBm**.



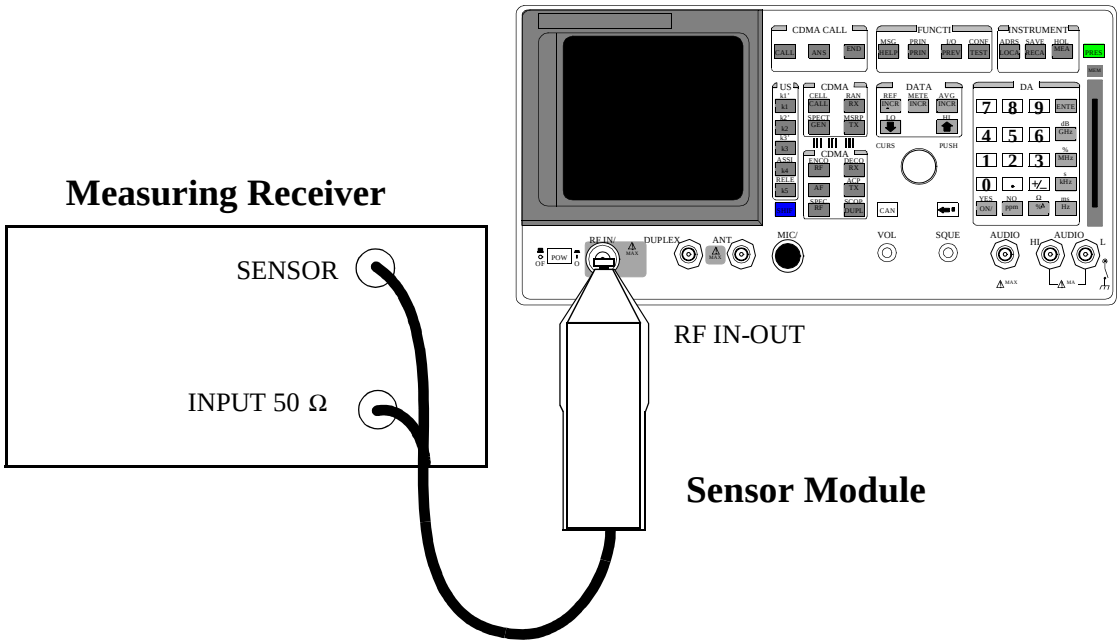
6. Set the **Center Freq** field to the frequencies shown in the PTR (**see "Residual Response" on page 348**) and measure the residual response on the spectrum analyzer's marker level field.

CDMA Generator RF In/Out Amplitude Level Accuracy Performance Test 27

Description

The amplitude level accuracy of the CDMA Generator at the RF IN/OUT port is measured directly with a power meter.

Calibration Setup



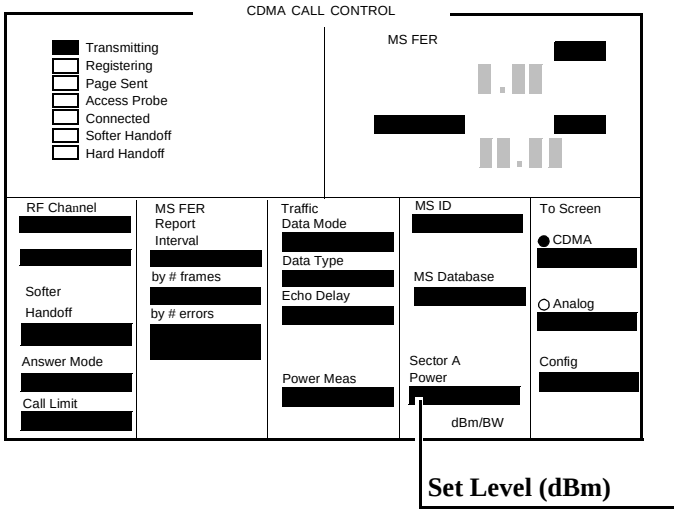
Make the following measuring receiver settings:

- Reset the measuring receiver
- RF power mode
- Log display

NOTE: The power sensor's calibration data must be entered into the measuring receiver and the sensor module must be zeroed. Refer to the measuring receiver's and the sensor module's operating manuals.

Procedure

1. Push PRESET.
2. Set the **`Sector A Power`** field to the values listed in the PTR (**see "CDMA Generator RF In/Out Amplitude Level Accuracy Performance Test 27" on page 350**).

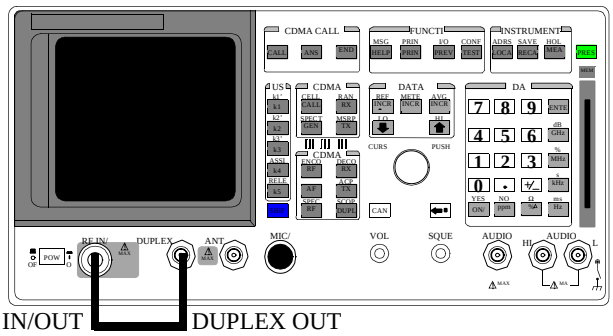


CDMA Generator Duplex Out Amplitude Level Accuracy Performance Test 28

Description

The amplitude level accuracy of the CDMA generator at the DUPLEX OUT port is measured using the CDMA analyzer.

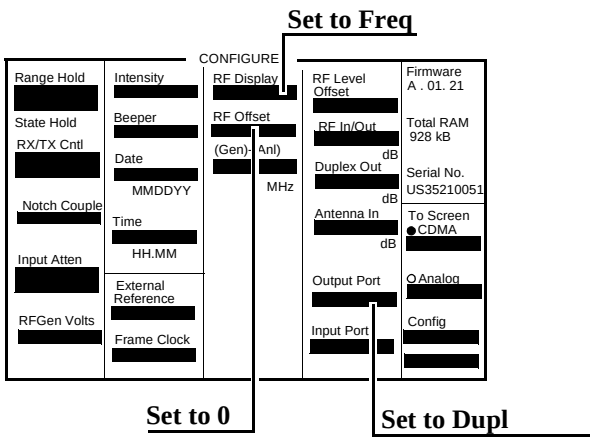
Setup



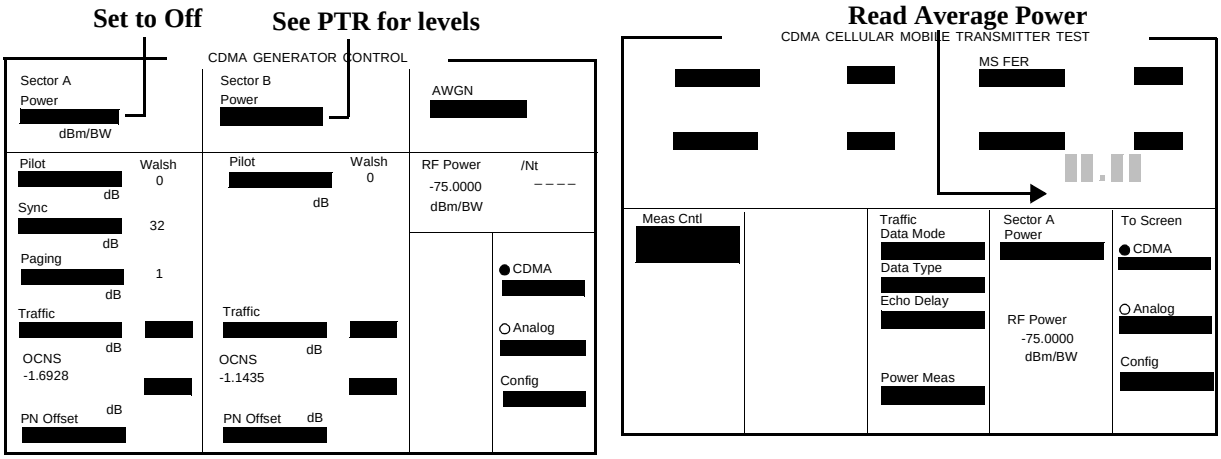
RF IN/OUT DUPLEX OUT

Procedure

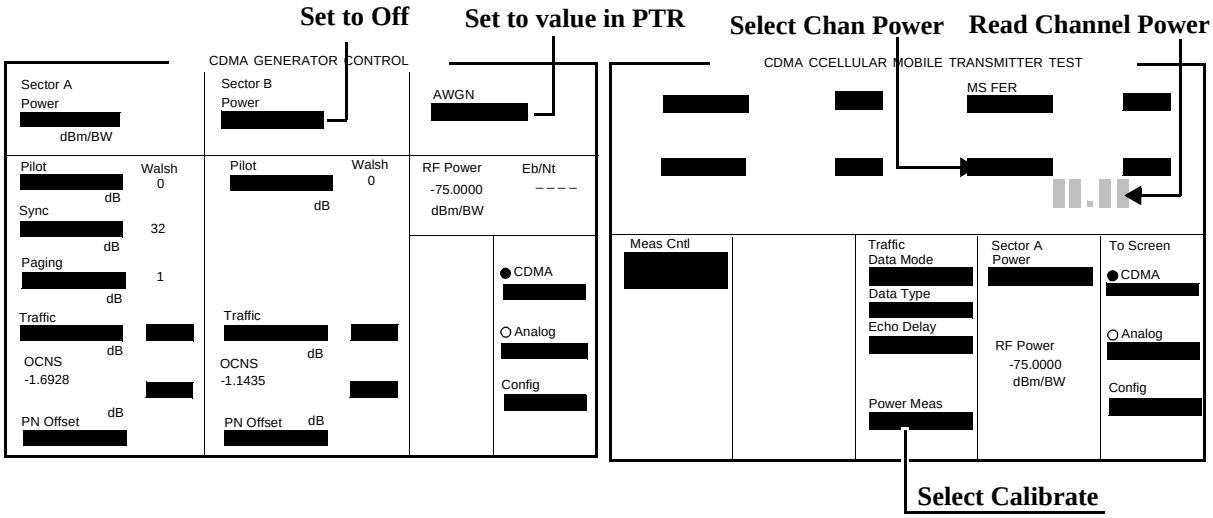
1. Push the PRESET key.
2. Access the CONFIGURE screen, and change the **`RF Display`** field to **`Freq`**.
3. Set the **`(Gen)-(Anl)`** field to **`0`**.
4. Set the **`Output Port`** to **`Dupl`**.



5. Access the RF GENERATOR screen and change the RF Gen Freq to 840 MHz.
6. Access the CDMA GENERATOR CONTROL screen.
7. Set the **`Sector A Power`** field to **`Off`**.
8. Set the **`Sector B Power`** field to the values listed in the PTR for Sector B Power. **See "CDMA Generator Duplex Out Amplitude Level Accuracy Performance Test 28" on page 351**.



9. Go to the CDMA CELLULAR MOBILE TRANSMITTER TEST screen.
10. Read the **Avg Power** (Average Power) and record it in the PTR.
11. Access the CDMA GENERATOR CONTROL screen.
12. Set the **Sector B Power** field to **Off**.
13. Access the CDMA CELLULAR MOBILE TRANSMITTER TEST screen.
14. Change the **Avg Power** measurement field to **Chan Power** (Channel Power).
15. Calibrate the Channel Power by selecting **Calibrate** in the **Power Meas** field.
16. Access the CDMA GENERATOR CONTROL screen.
17. Set the **AWGN Power** field to the values listed in the PTR for AWGN Power.
18. Read the Channel Power and record it in the PTR.

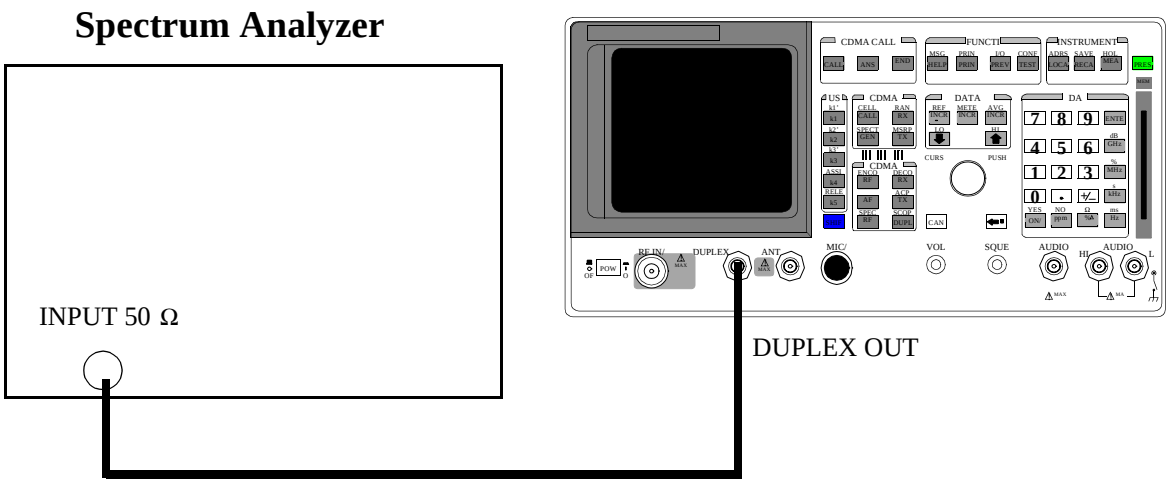


CDMA Generator Adjacent Channel Spectral Purity Performance Test 29

Description

The adjacent channel spectral purity of the CDMA generator is measured with a spectrum analyzer by comparing the RF power in the adjacent channel to the power at the center frequency of the CDMA signal. A 12 dB adder is used to convert the center frequency level to total carrier power.

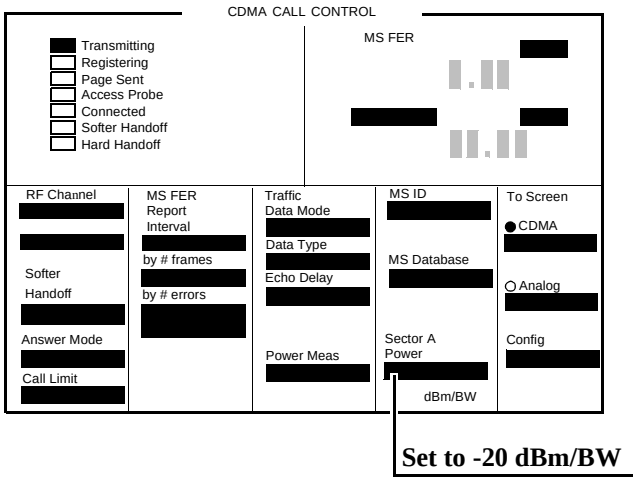
Setup



Procedure

On the Test Set:

1. Push PRESET
2. Change the **Sector A Power** field to **-20 dBm/BW**.



On the Spectrum Analyzer:

1. Set the span to 200 kHz.
2. Set the center frequency to 881.520 MHz. (This is the default center frequency of the CDMA Generator after preset.)
3. Measure the RF level: this is $\mathbf{P}_{center}$
4. Set the center frequency to the Adjacent Channel frequencies in the PTR table (**see "CDMA Generator Adjacent Channel Spectral Purity Performance Test 29" on page 352**). The measured values at these frequencies are $\mathbf{P}_{adj}$.

   Use the following equation to complete the PTR.

   $P_{relative} = P_{adj} - [P_{center} + 12]$

   $P_{relative}$ = Relative Adjacent Channel Power (dBc)

   P_{center} = Measured Center Frequency Power (dBm)

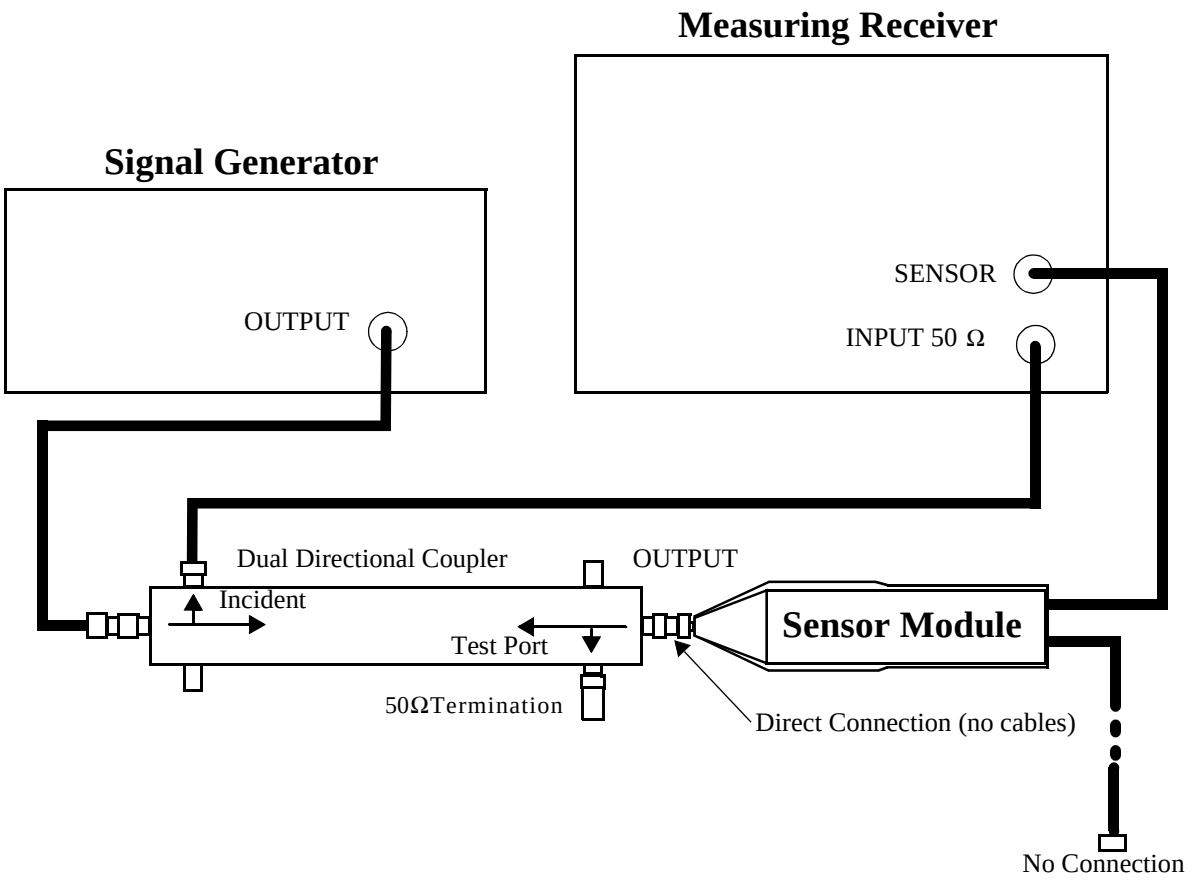
   P_{adj} = Adjacent Channel Power (dBm)

CDMA Analyzer Average Power Level Accuracy Performance Test 30

Description

The CDMA average power level accuracy is verified by comparing the measured power in a CDMA signal with the power level measured by a power meter. The signal is first measured by the power meter for a reference and then the same measurements are performed using the HP 8924C's analyzer. A dual directional coupler is used to minimize mismatch uncertainty.

Calibration Setup



Make the following signal generator setting:

- Amplitude 0 dB

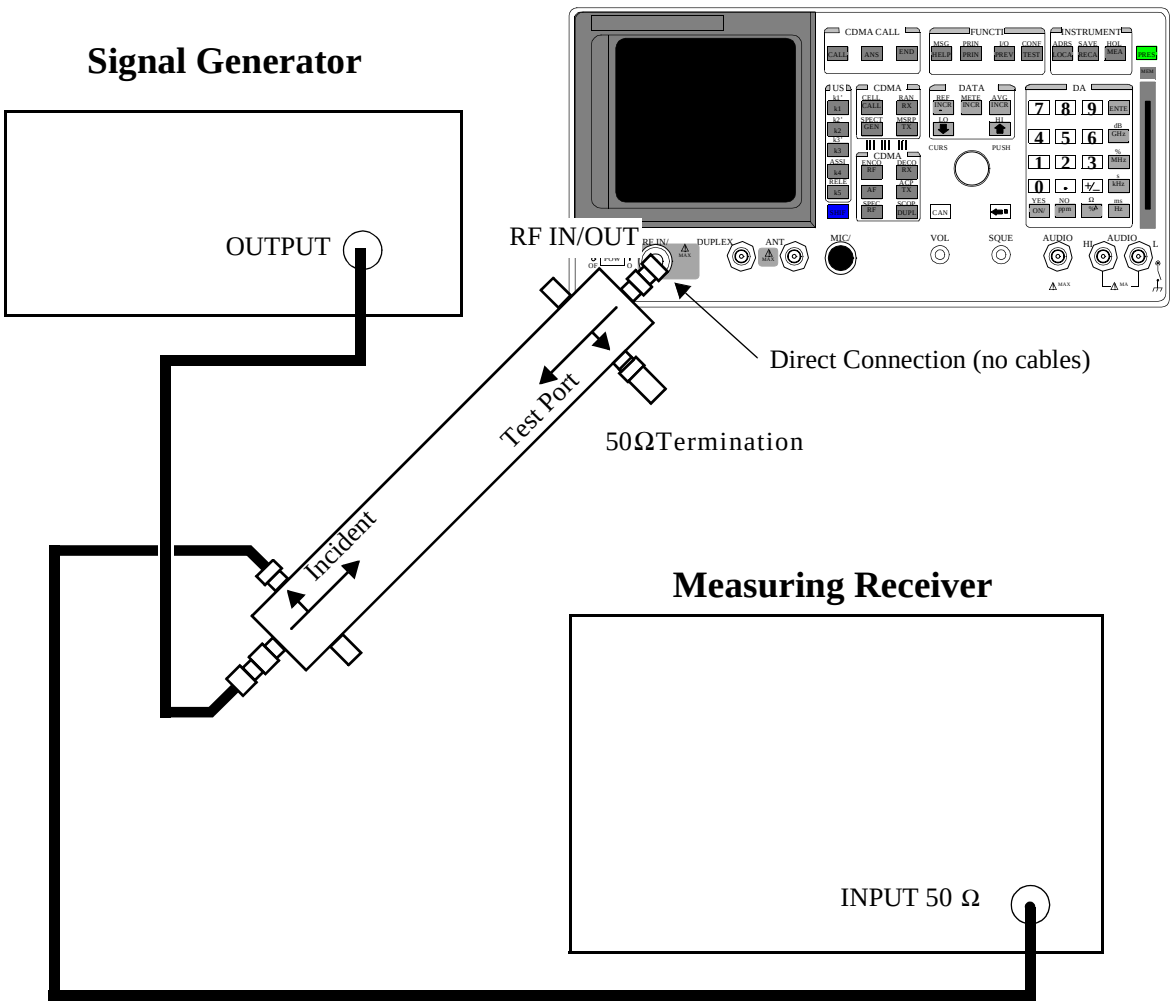
Make the following measuring receiver settings:

- Track mode
- RF Power measurement
- 4.4 SPCL
- 8.3 SPCL

Calibration Procedure

1. Set the signal generator and the measuring receiver to 40 MHz.
2. Make an RF POWER measurement, in mW, with the measuring receiver. Record the measured power as **Reference Power** in the *Measurement Procedure* in step 11.
3. Disconnect the sensor cable at the measuring receiver. (leave the sensor connected to the directional coupler so that it will be terminated into 50 Ω
4. Make a **TUNED RF LEVE**L measurement, in mW, with the measuring receiver. Record the measured level as **Tuned RF #1** in the *Measurement Procedure* in step 11.
5. Repeat this procedure for each of the frequencies listed in the PTR (**see "CDMA Analyzer Average Power Level Accuracy Performance Test 30" on page 353**).

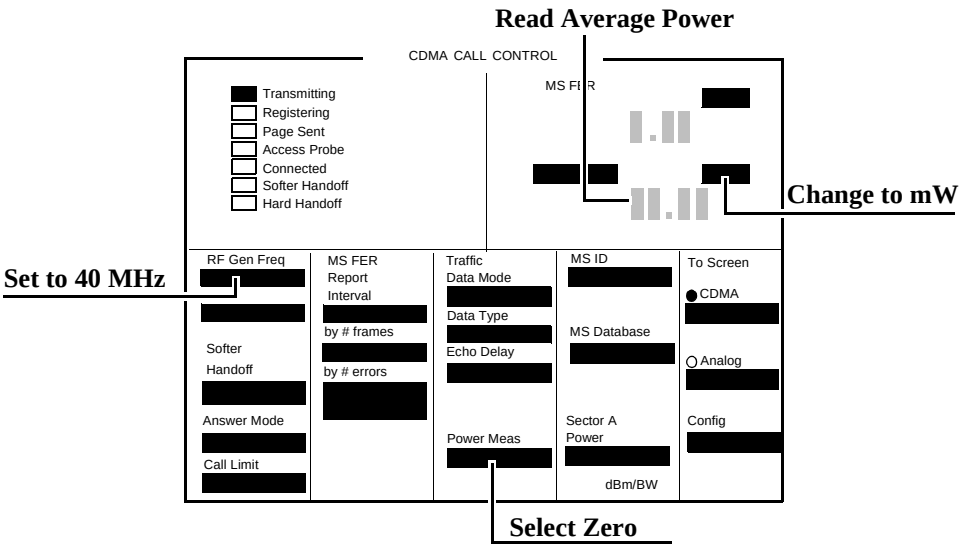
Measurement Setup



Measurement Procedure

On the Measuring Receiver:

1. After replacing the coupler with the Test Set, make a TUNED RF LEVEL measurement, in mW, with the measuring receiver. Record the measured level as **Tune RF #2** in step 11.
2. On the Test Set push PRESET.
3. Access the CONFIGURE screen.
4. Set the **RF Display** field to **Freq**.
5. Access the CDMA CALL CTRL screen.
6. Change the **Avg Power** measurement units to **mW**.
7. Set the **RF Gen Freq** field to **40 MHz**.
8. Zero the power meter: a: Temporarily disconnect all RF inputs to the HP 8924C.
   a Select **Zero** (under the **Power Meas** label).
9. Reconnect the output of the directional coupler to the 8924C's Test Set RF IN/OUT connector (connect directly - no cables).
10. Read the **Avg Power** field in mW, and record it as **UUT Power** in step 11.



11. Calculate the Measured Power as follows:

$$\text{Measured Power} = 1\text{mW} * \frac{\text{UUT Power}}{\text{ReferencePower}} * \frac{\text{Tuned RF\#1}}{\text{Tuned RF \#2}}$$

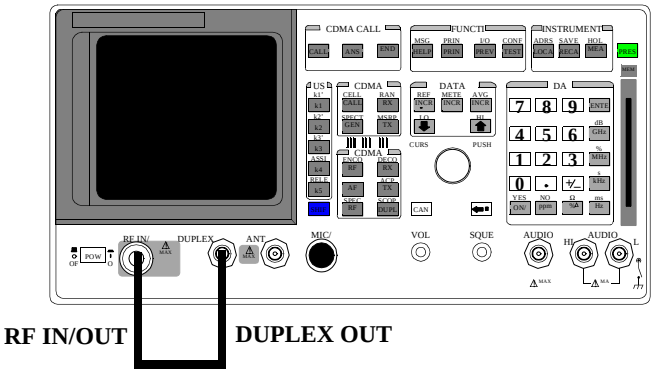
12. Repeat the Calibration and Measurement procedures for each of the frequencies listed in the PTR.

CDMA Analyzer Calibrated Tuned Channel Power Level Accuracy Performance Test 31

Description

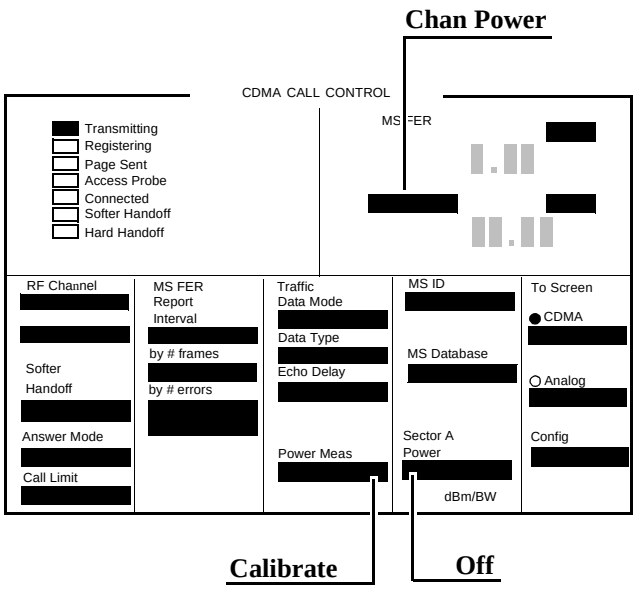
The tuned channel power level accuracy is verified by comparing the measured power in a CW signal with the power level measured by a measuring receiver.

Calibration Setup

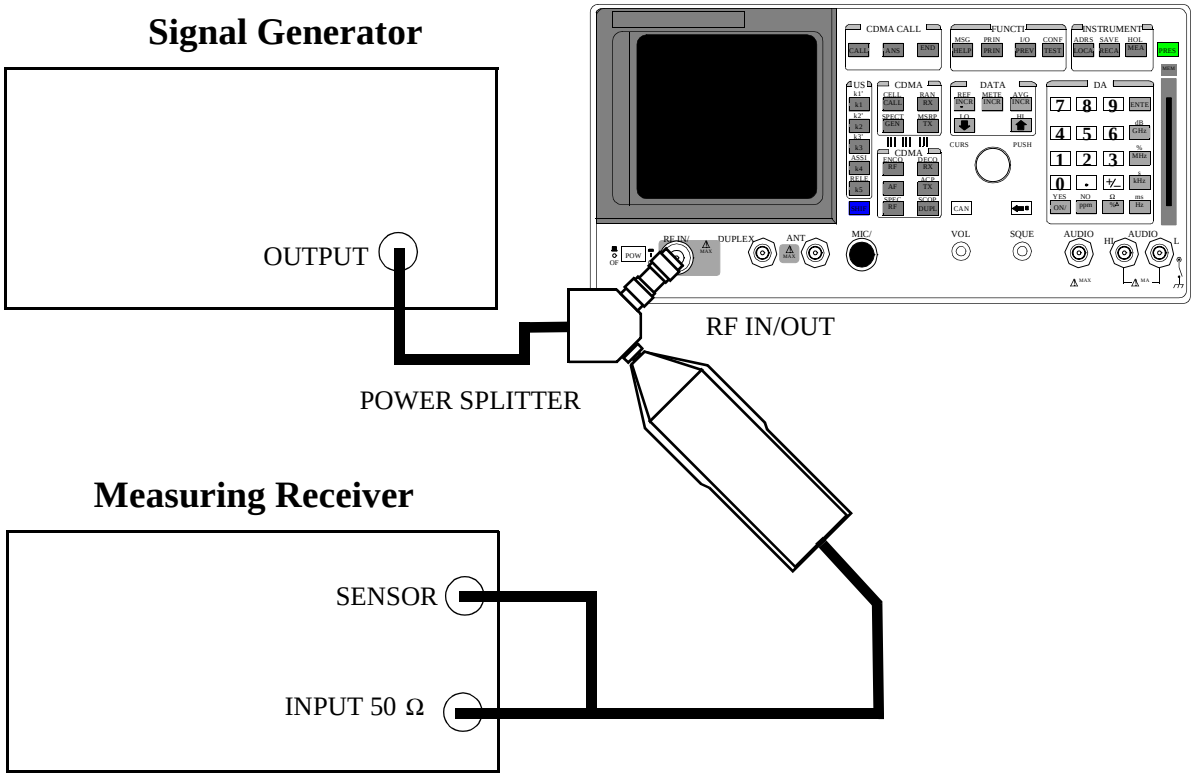


Calibration Procedure

1. Push PRESET.
2. Set the **`Sector A Power`** field to **`Off`**.
3. Change the **`Avg Power`** measurement to **`Chan Power`**.
4. Select **`Calibrate`** under the **`Power Meas`** field.



Measurement Setup



Signal Generator

Set the frequency to 840 MHz.

Set the output level to 1 dBm.

Measuring Receiver

Set the display mode to LOG.

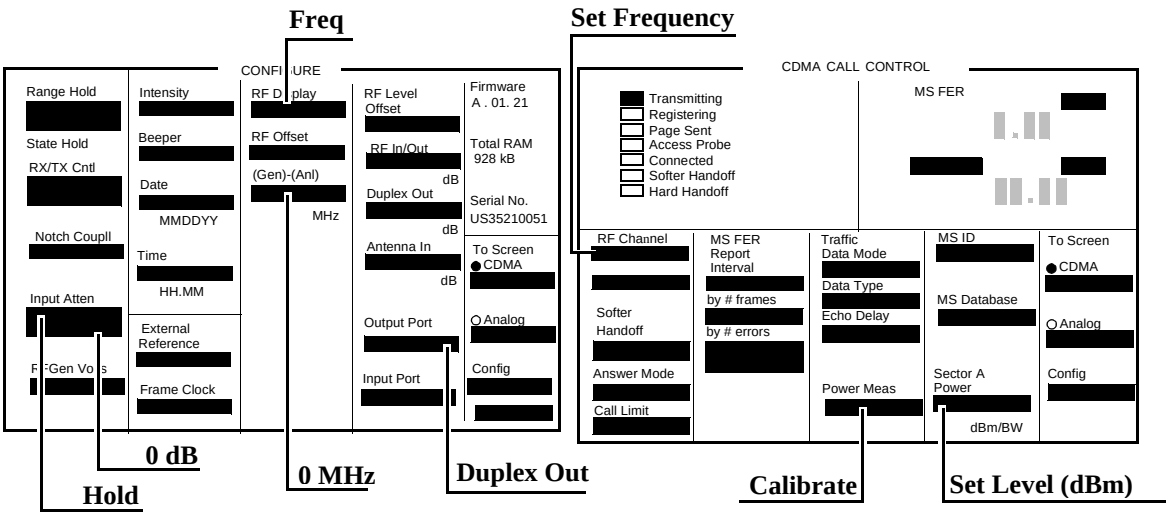
Set the measurement to Tuned RF Level.

Calibrate the power sensor.

NOTE: The power sensor's calibration data must be entered into the measuring receiver and the sensor module must be zeroed. Refer to the measuring receiver's and the sensor module's operating manual.

Measurement Procedure

1. Access the CONFIGURE screen.
2. Set the **RF Display** field to **Freq**.
3. Set the **(GEN)-(ANL)** field to **0 MHz**.
4. Change **Output Port** to **Duplex Out**.
5. Set the **Input Atten** field to **Hold** and **0 dB**.
6. Access CDMA Call Control Screen.
7. Set the **RF Gen Freq** field to **840 MHz**.



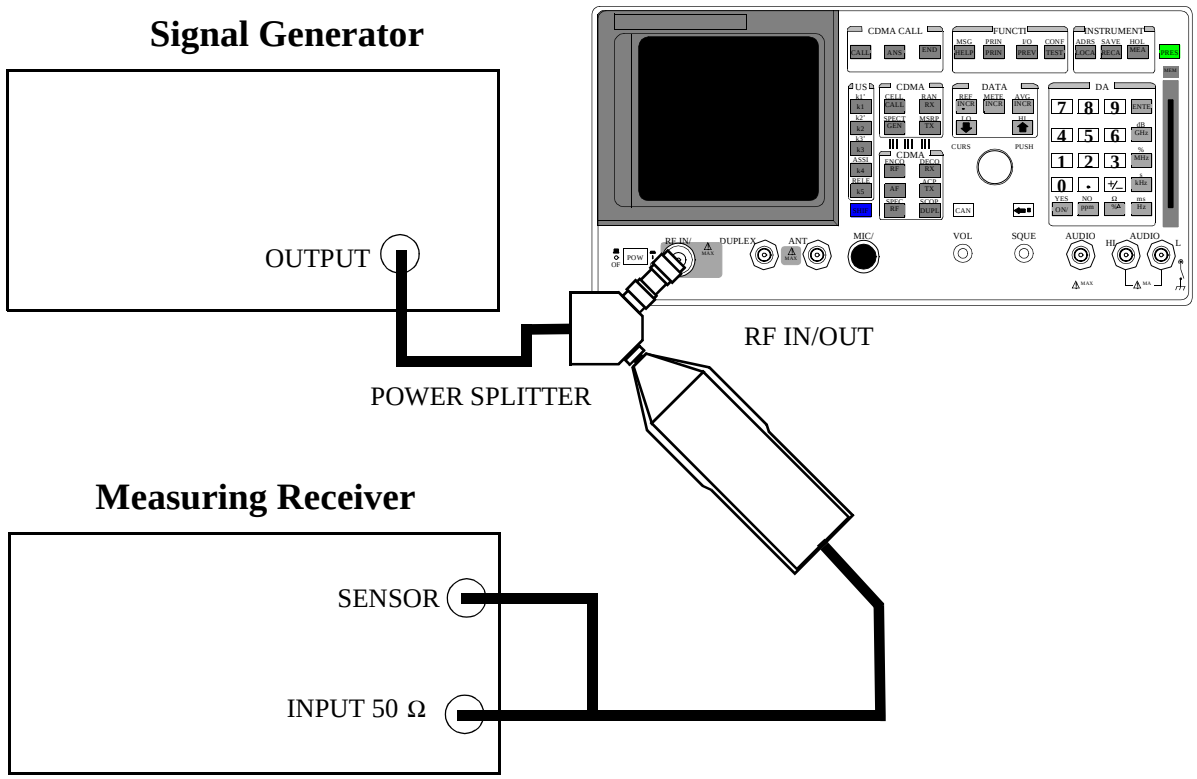
8. Measure each of the RF levels in the PTR with the Test Set and the measuring receiver (**see "CDMA Analyzer Calibrated Tuned Channel Power Level Accuracy Performance Test 31" on page 354**) and record the results.

CDMA Analyzer Relative Tuned Channel Power Level Accuracy Performance Test 32

Description

The signal generator is set to approximately -10 dBm for a reference level. Then the power level is reduced in approximately 5 dB steps. The relative tuned channel power level is verified on the measuring receiver.

Setup



Signal Generator

Set the frequency to 840 MHz.

Set the output level to 1 dBm.

Measuring Receiver

Set the display mode to LOG.

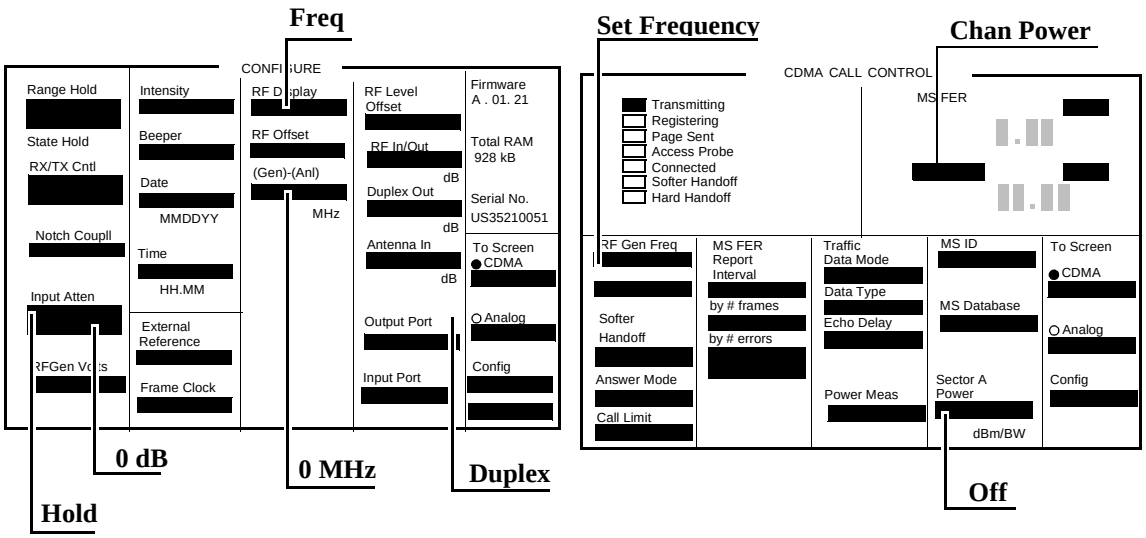
Set the measurement to Tuned RF Level.

Calibrate the power sensor.

NOTE: The power sensor's calibration data must be entered into the measuring receiver and the sensor module must be zeroed. Refer to the measuring receiver's and the sensor module's operating manuals.

Procedure

1. Push PRESET.
2. Access the CONFIGURE screen.
3. Set the **RF Display** field to **Freq**.
4. Set the **(GEN)-(ANL)** field to **0 MHz**.
5. Change the **Input Atten** field to **Hold** and **0 dB.**
6. Access the CDMA CALL CTRL screen.
7. Set the **Avg Power** field to **Chan Power.**
8. Turn **Sector A Power** to **Off**.
9. Set the **RF Gen Freq** to the values listed in PTR.



10. Measure each of the RF levels in the PTR with the HP 8924C and the Measuring Receiver (**see "CDMA Analyzer Relative Tuned Channel Power Level Accuracy Performance Test 32" on page 355**).

11. Use the following measurement equation and enter the result in the PTR.

$$A_{meas} = R_{8924c} - R_{8902A}$$

A_{meas} = Measured value
R_{8924C} = Power reading on HP 8924C
R_{8902A} = Power Reading on Measuring Receiver

12. Change the Frequency on the Signal Generator, Measuring Receiver, and the HP 8924C to each of the values in the PTR and repeat the above procedure.

6

HP 8924E
Performance Verification

This chapter contains step-by-step tests to verify the specified performance of the Test Set. Performance Test Records are included at the end of this chapter to document the measurement results for each test point (**see "HP 8924E Performance Test Records" on page 357**).

Verifying Performance

Test Set Operation

You need to know basic Test Set operation to perform these test procedures (refer to the User's Guide). You should be familiar with the front-panel controls and the use of the control screens. You need to be able to operate the Test Set's RF Generator, RF Analyzer, AF Generators, AF Analyzer, and Oscilloscope.

NOTE: Periodic adjustments should always be performed before verifying instrument performance. **See "Periodic Adjustments" on page 137**.

PRESET BEFORE EACH TEST

Press PRESET on the Test Set before beginning each test to return the controls to a known state.

Equipment

To perform all tests you will need the equipment described in **Table 8**. Equipment for individual tests is shown in the test setup drawings. Alternative test equipment can be used if specifications are equal to those listed in the Hewlett-Packard Test and Measurement Catalog for each HP model. If you just need to verify operation, rather than verify specified performance, you can use the test procedures with functionally equivalent equipment.

Test Equipment Operation

The test procedures give critical instrument settings and connections, but they do not tell how to operate the test instruments. Refer to each instrument's operating manual.

Table 8 Required Test Equipment

Equipment Model # (or equivalent)	Model Name	Performance Test #
HP 3458A	Digital Voltmeter	10, 11, 14, 17, 20
HP 8116A	Function Generator	21
HP 8562A	RF Spectrum Analyzer	8, 9, 29
HP 8902A	Measuring Receiver	1-3,4[a], 5-7, 19, 21-23, 27, 30, 31, 32
HP 8903B	Audio Analyzer	4[b], 12,14, 18, 22, 22 23, 25
HP 11715A	AM/FM Test Source	22-28
HP 11722A	Sensor Module	5-7, 21, 30, 31,32
HP 5316B	Universal Counter	13, 18
HP 778D	Dual Directional Coupler	21, 30
HP 8642A, 8657A/B	Synthesized Signal Generator	4, 19, 26, 29, 30, 31, 32
HP 11667A	Power Splitter	31, 32
HP 8904A Opt 001	Function Synthesizer	16

a. For connections for an external LO, included as part of HP 8902A Option 003 or 030. For Option 030 it does not matter which filters are installed (only the switching of the LO is important).

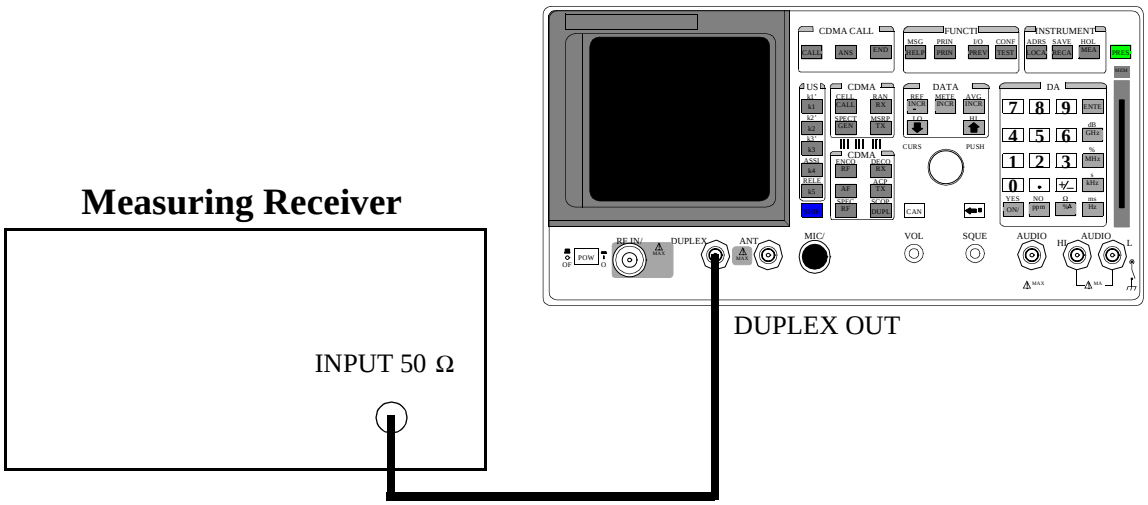
b. For Performance Test 4 the HP 8903B requires a CCITT filter (Option 011 or 051).

RF Gen FM Distortion Performance Test 1

Description

The FM distortion of the RF generator is measured directly by the measuring receiver. The Test Set's internal audio generator provides the modulation source.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- 300 Hz High-Pass Filter
- 3 kHz Low-Pass Filter
- FM mode
- Distortion analyzer mode

Procedure

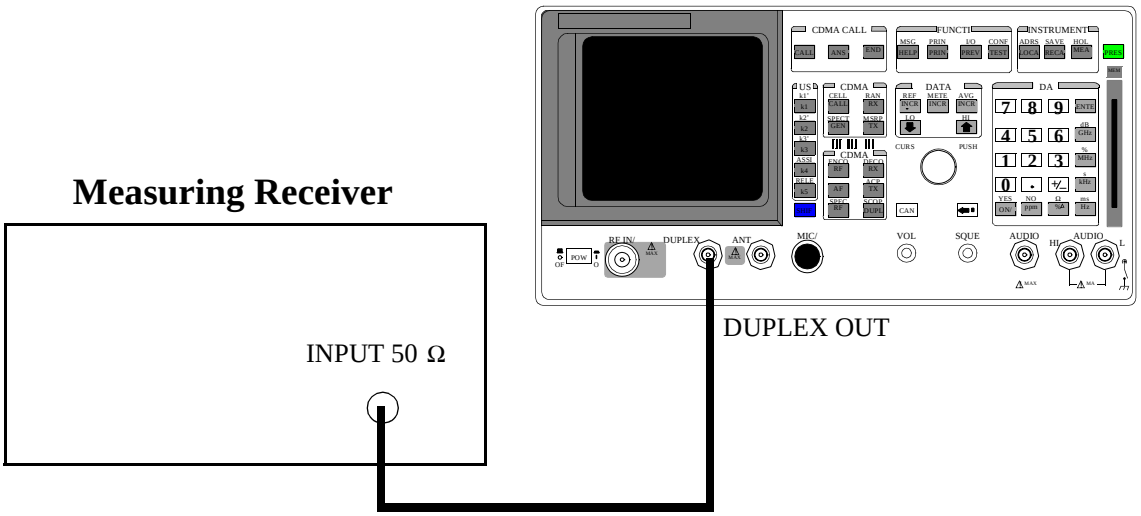
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **RF Display** field to **Freq**.
4. Set the **Output Port** field to **Dupl**.
5. Access the ANAGLOG MEAS screen.
6. Set the **AFGen1 To** field to **FM**.
7. Measure the FM distortion at the RF level, frequencies, deviations, and rate shown in the PTR (**see "RF Gen FM Distortion Performance Test 1" on page 359**) and compare the measured distortion to the limits shown in the PTR.

RF Gen FM Accuracy Performance Test 2

Description

The FM distortion of the RF generator is measured directly by the measuring receiver. The Test Set's internal audio generator provides the modulation source.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- 300 Hz High-Pass Filter
- 3 kHz Low-Pass Filter
- FM mode
- FM de-emphasis off

Procedure

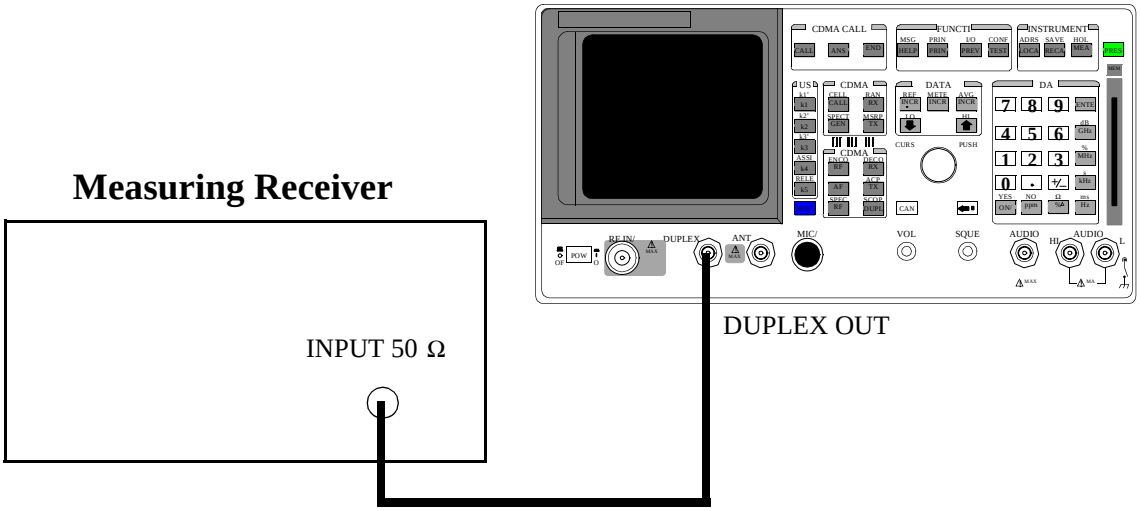
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **RF Display** field to **Freq**.
4. Set the **Output Port** field to **Dupl**.
5. Access the ANALOG MEAS screen.
6. Set the **AFGen1 To** field to **FM**.
7. Measure the deviations at the RF level, frequencies, deviations, and rate shown in the PTR (**see "RF Gen FM Accuracy Performance Test 2" on page 361**) and compare the measured deviation to the limits shown in the PTR.

RF Gen FM Flatness Performance Test 3

Description

The FM flatness of the RF generator is measured directly by the measuring receiver. The Test Set's internal audio generator provides the modulation source.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- FM mode

Procedure

1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **`RF Display`** field to **`Freq`**.
4. Set the **`Output Port`** field to **`Dupl`**.
5. Access the ANALOG MEAS screen.
6. Set the **`AFGen1 To`** field to **`FM`**.
7. Measure the FM deviation at the RF level, frequencies, deviations, and rates shown in the PTR (**see "RF Gen FM Flatness Performance Test 3" on page 363**).
8. Convert the measurement results to dB referenced to the deviation measured at 1 kHz as follows:

$$dB = 20 \log \frac{\text{Deviation}}{\text{Deviation at 1kHz}}$$

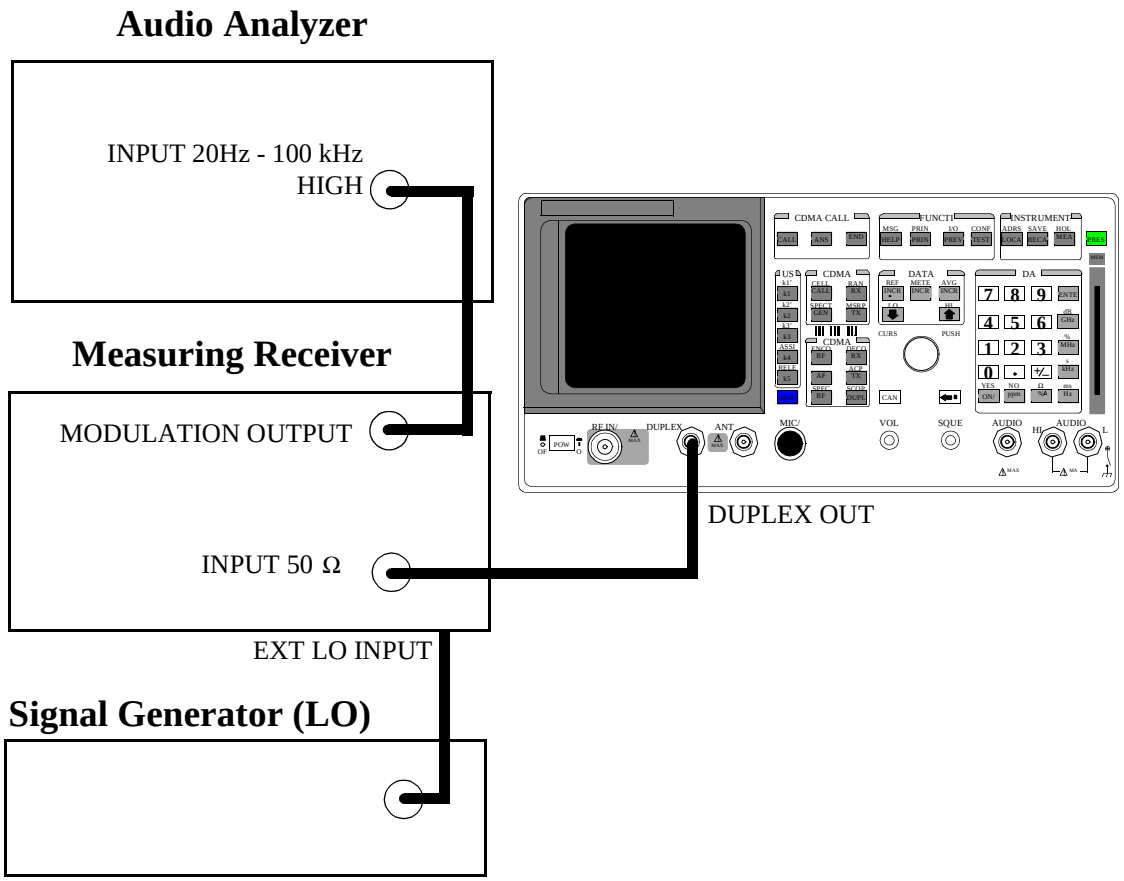
(The computed values must be 0, ±1 dB.)

RF Gen Residual FM Performance Test 4

Description

The residual FM of the RF generator is demodulated by the measuring receiver. An audio analyzer with a CCITT psophometric filter is required to measure the demodulated residual FM.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- 1.5 MHz IF
- FM mode
- RMS detector
- 50 Hz High-Pass Filter
- 15 kHz Low-Pass Filter
- Enable the external LO mode

Make the following audio analyzer settings:

- Reset the audio analyzer
- AC level
- CCITT weighting Filter
- 30 kHz Low-Pass Filter

Procedure

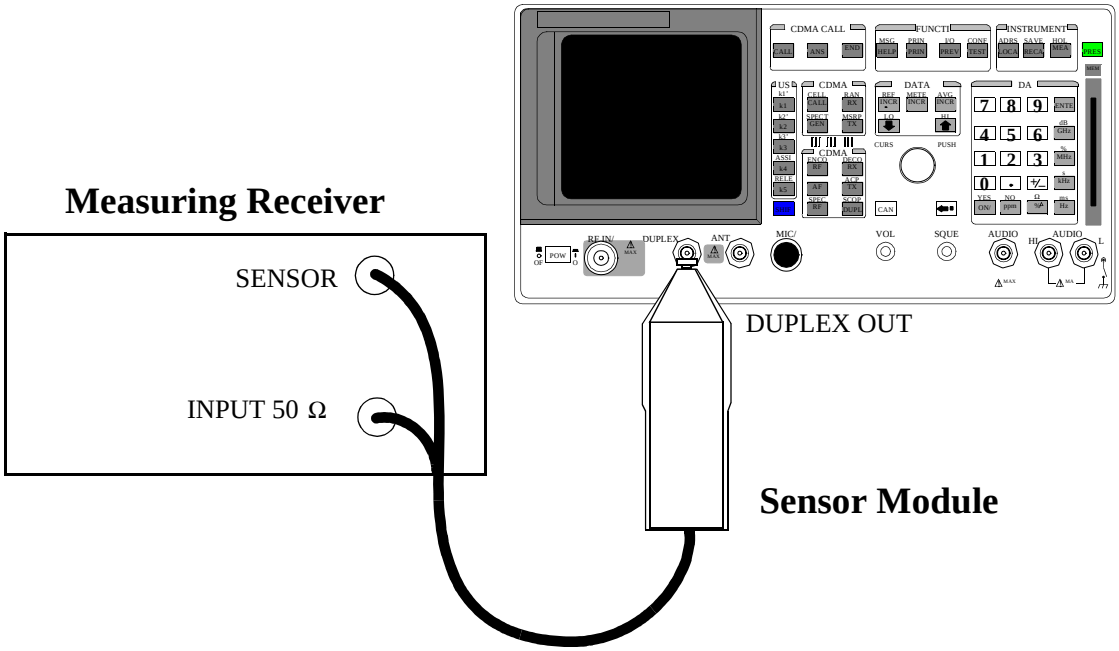
1. Access the CONFIGURE screen.
2. Change the **RF Display** field to **Freq**.
3. Set the **Output Port field** to **Dupl.**
4. **AFGen1**Set the **Amplitude field** to –9.1 dBm.
5. Set the **AFGen1 To** field to **FM.**
6. Set the **AFGen1** deviation to **Off** (using the ON/OFF key).
7. Set the signal generator (used as an external LO for the measuring receiver) to the LO frequencies shown in the PTR (**see "RF Gen Residual FM Performance Test 4" on page 364**).
8. Set the Test Set to the RF frequencies shown in the PTR and measure the ac level, in millivolts, on the audio analyzer.
9. Multiply the measured ac levels by 1000 to convert to FM deviation in Hz and compare the computed results to the limits shown in the PTR.

RF Gen Duplex Output High Level Accuracy Performance Test 5

Description

The level of the RF generator, set to 1 and 3.5 dBm, at the duplex output is measured at numerous frequencies by the sensor module of the measuring receiver.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- RF power mode
- Log display

NOTE: Make sure to enter the power sensor's calibration data into the measuring receiver and zero the sensor module. Refer to the measuring receiver's and the sensor module's operating manuals.

Procedure

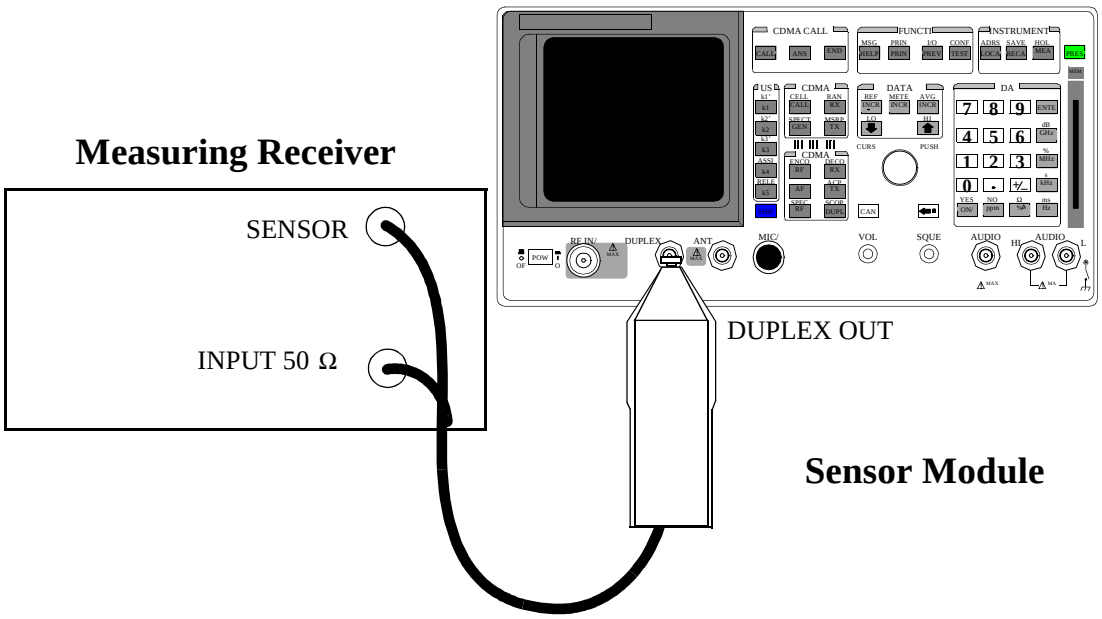
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **`RF Display`** field to **`Freq`**.
4. Set the **`Output Port`** field to **`Dupl.`**
5. Access the ANALOG MEAS screen.
6. Set the **`AFGEN1 TO`** field to **`Off (using the ON/OFF key).`**
7. Measure the RF power at the frequencies and levels shown in the PTR (**see "RF Gen Duplex Output High Level Accuracy Performance Test 5" on page 366**) and compare the measured RF power to the limits shown in the PTR.

RF Gen Duplex Output Low Level Accuracy Performance Test 6

Description

The Duplex output is set to selected frequencies and to levels between 1 and –124 dBm (in 5 dB steps) and measured by the tuned RF level feature of the measuring receiver. As the test proceeds you may be required to recalibrate the measuring receiver.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- Tuned RF Level power measurement
- Log display

NOTE: Make sure to enter the power sensor's calibration data into the measuring receiver and zero the power sensor. Refer to the measuring receiver's operating manual. The procedure for making tuned RF level measurements is also in the measuring receiver's manual.

Procedure

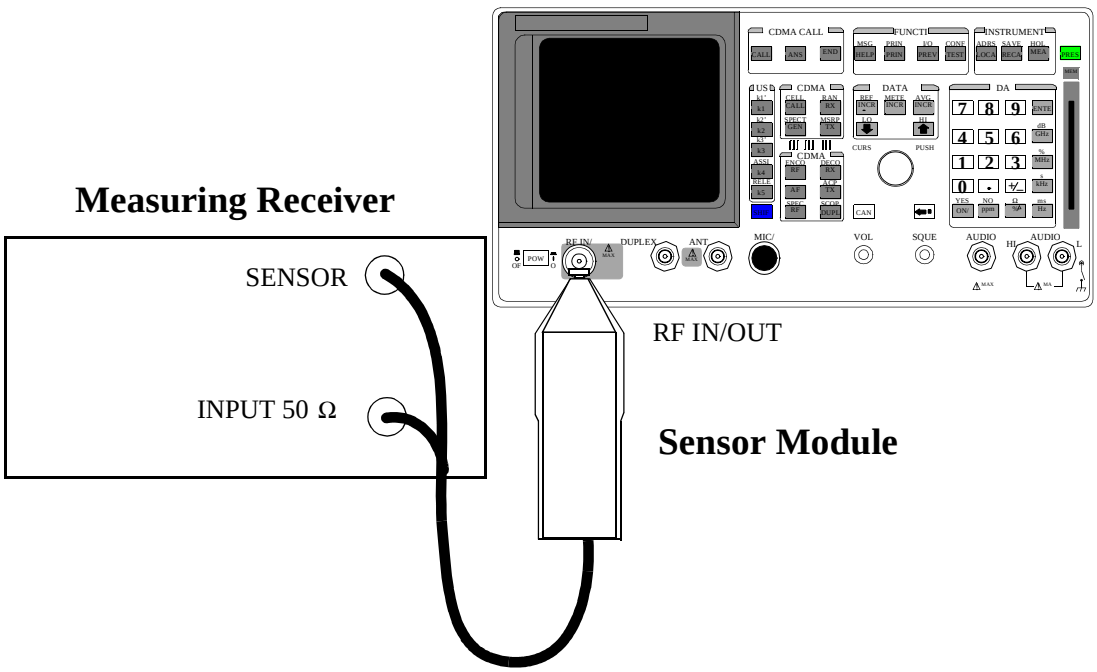
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **RF Display** field to **Freq**.
4. Set the **Output Port** field to **Dupl**.
5. Select the ANALOG MESAS screen.
6. Set the **AFGen1 To** and **f**ield to **Off**.
7. Measure the RF level at the frequencies and levels shown in the PTR (**see "RF Gen Duplex Output Low Level Accuracy Performance Test 6" on page 244**) and compare measured RF level to the limits shown in the PTR.

RF Gen RF IN/OUT Level Accuracy Performance Test 7

Description

The RF output is set to selected frequencies and to levels between –10.5 and –124 dBm (in 5 dB steps) and measured by the tuned RF level feature of the measuring receiver. As the test proceeds you may be required to recalibrate the measuring receiver.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- Tuned RF Level power measurement
- Log display

NOTE: Make sure to enter the power sensor's calibration data into the measuring receiver, and zero the power sensor. Refer to the measuring receiver's operating manual. The procedure for making tuned RF Level measurements is also in the measuring receiver's manual.

Procedure

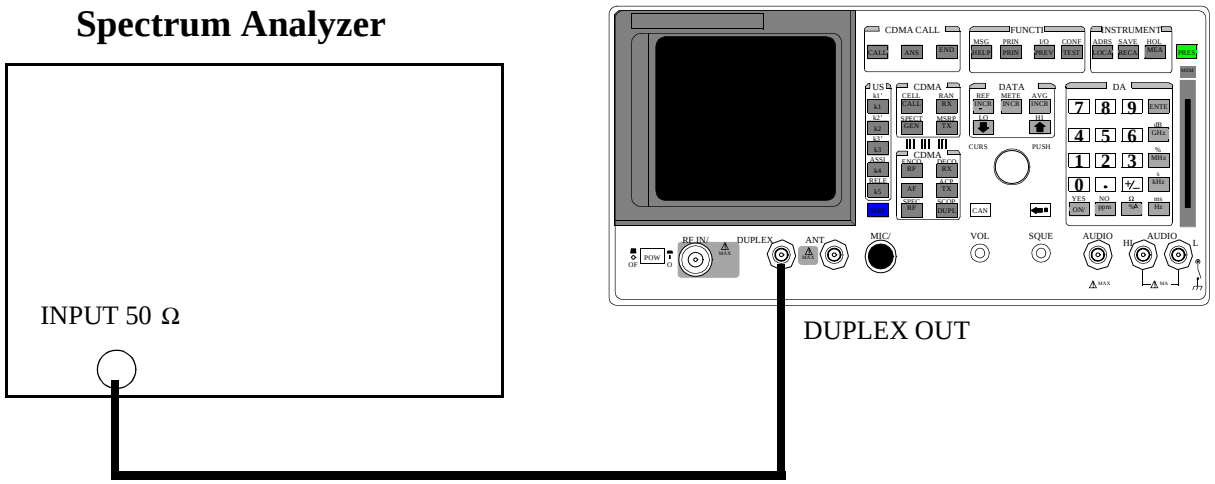
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **`RF Display`** field to **`Freq`**.
4. Set the **`Output Port`** field to **`RF Out.`**
5. Select the ANALOG MESAS screen.
6. Set the **`AFGen1 To`** field to **`Off.`**
7. Measure the RF Level at the frequencies and levels shown in the PTR (**see "RF Gen RF IN/OUT Level Accuracy Performance Test 7" on page 371**) and compare the measured RF level to the limits shown in the PTR.

RF Gen Harmonics Spectral Purity Performance Test 8

Description

Harmonic signals with the carrier set to several frequencies and two different levels (maximum and minimum level vernier) are searched for by an RF spectrum analyzer.

Setup



Refer to the spectrum analyzer's operating manual to set up the spectrum analyzer.

Procedure

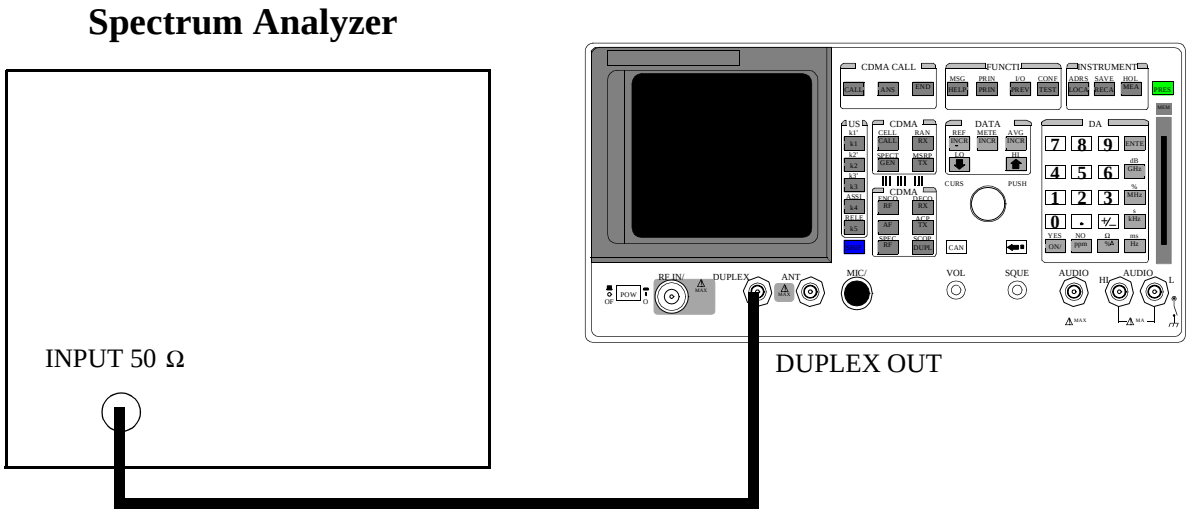
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **`RF Display`** field to **`Freq`**.
4. Set the **`Output Port`** field to **`Dupl`**.
5. Select the ANALOG MEAS screen.
6. Set the **`AFGen1`** level to **`Off`**.
7. Set the Test Set to the RF Generator frequencies and level shown in the PTR (**see "RF Gen Harmonics Spectral Purity Performance Test 8" on page 375**), and measure the level of the second and third harmonics and the half-harmonics also shown in the PTR.
8. Convert the harmonic levels to decibels below the fundamental (dBc) and compare the computed levels to the limits shown in the PTR.

RF Gen Spurious Spectral Purity Performance Test 9

Description

Spurious signals with the carrier set to several frequencies and two different levels (maximum and minimum level vernier) are searched for by an RF spectrum analyzer.

Setup



Refer to the spectrum analyzer's operating manual to set up the spectrum analyzer.

Procedure

1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Change the **`RF Display`** field to **`Freq`**.
4. Set the **`Output Port`** field to **`Dupl`**.
5. Select the ANALOG MEAS screen.
6. Set the **`AFGen1 To`** level to **`Off.`**
7. Set the Test Set to the RF Generator frequencies and levels (– 2.5 dBm or –4 dBm) shown in the PTR (**see "RF Gen Spurious Spectral Purity Performance Test 9" on page 379**), and measure the levels of the spurious signals at the frequencies shown in the PTR.
8. Convert the measured levels to decibels below the carrier (dBc), and compare the computed results to the limits shown in the PTR.

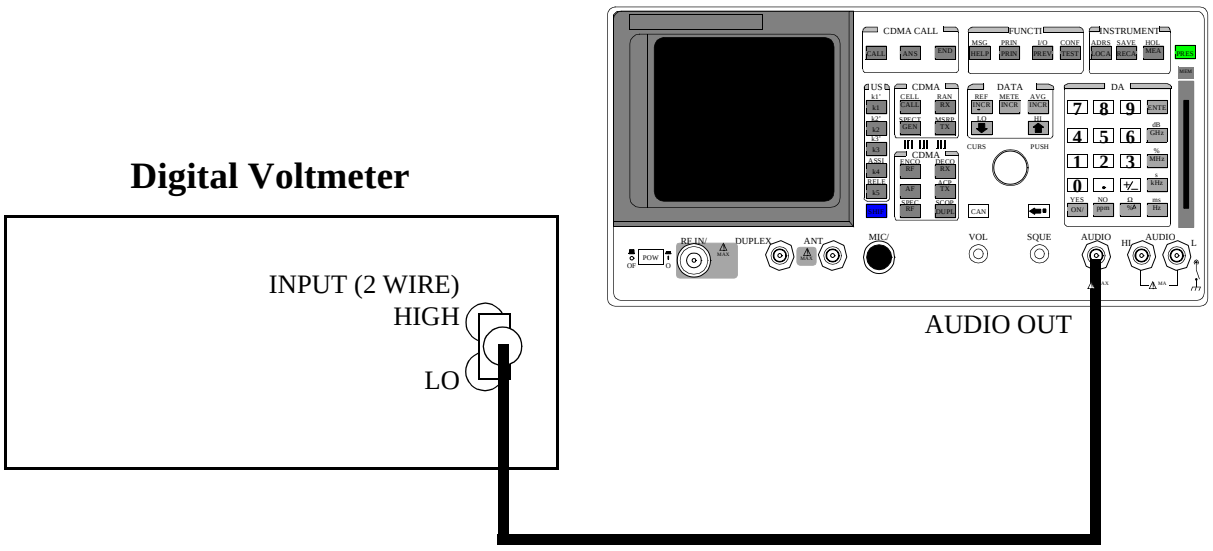
NOTE: Ignore the spur source column of the PTR. That information is for help in troubleshooting.

AF Gen AC Level Accuracy Performance Test 10

Description

There are two audio generators. AC level accuracy is measured directly by a digital voltmeter.

Setup



Make the following digital voltmeter setting:

- AC Volts

Procedure

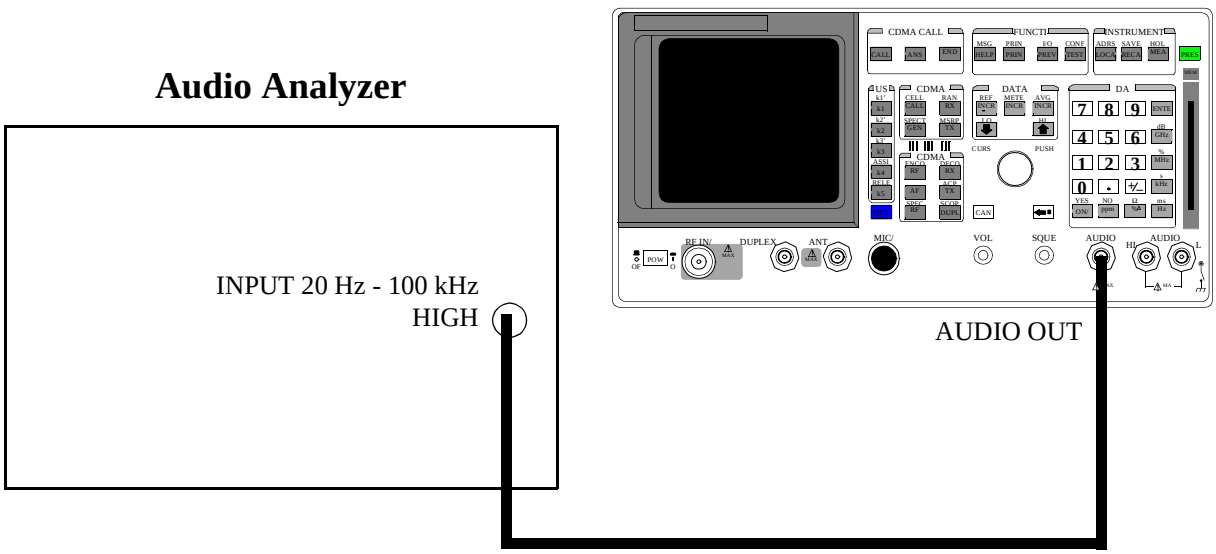
1. Press the PRESET key on the Test Set.
2. Select the RF GENERATOR screen.
3. Set the Output Port field to RF Out.
4. Set the AFGen1 To and AFGen2 To fields to Off.
5. Measure the RF Level at the frequencies and levels shown in the PTR and compare the measured RF level to the limits shown in the PTR.

AF Gen Residual Distortion Performance Test 12

Description

Audio distortion is measured directly by an audio analyzer.

Setup



Make the following audio analyzer settings:

- Reset the audio analyzer
- 80 kHz Low-Pass Filter
- Distortion mode

Procedure

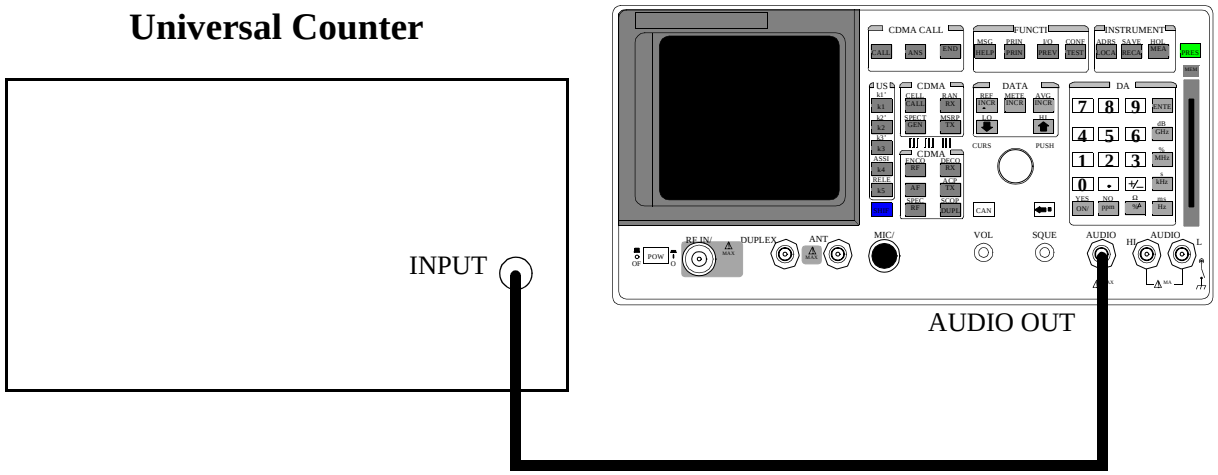
1. Press the PRESET key on the Test Set.
2. Access the ANALOG MEAS screen.
3. Set the **`AFGen1 To`** field to **`Audio Out`**.
4. Measure the audio distortion at the frequencies and levels shown in the PTR (**see "AF Gen Residual Distortion Performance Test 12" on page 382**) and compare the measured distortion to the limits shown in the PTR.

AF Gen Frequency Accuracy Performance Test 13

Description

Frequency accuracy is measured directly by an audio frequency counter in the measuring receiver. The counter must be able to resolve 0.005% at 20 Hz. The counter in some audio analyzers lacks the resolution to do this.

Setup



Make the following counter settings:

- Select frequency

Procedure

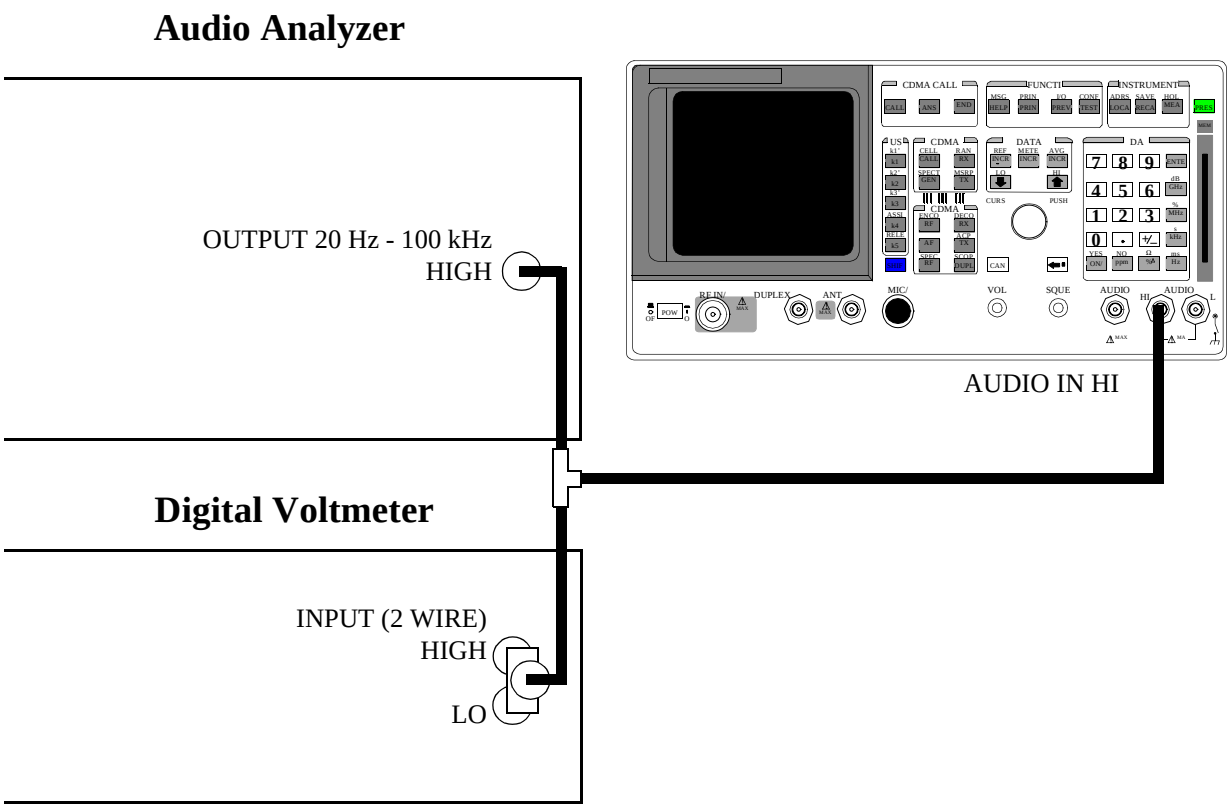
1. Press the PRESET key on the Test Set.
2. Access the ANALOG MEAS screen.
3. Set the **AFGen1 To** fields to **Audio Out.**
4. Set AFGen1 level to **1 V**.
5. Measure the audio frequency at the frequencies shown in the PTR (**see "AF Gen Frequency Accuracy Performance Test 13" on page 383**) and compare the results to the PTR.

AF Analyzer AC Voltage Accuracy Performance Test 14

Description

To measure ac voltage accuracy, an ac signal is measured by an external multimeter and compared to the Test Set's internal ac voltmeter reading.

Setup



Make the following digital voltmeter setting:

- AC Volts

Procedure

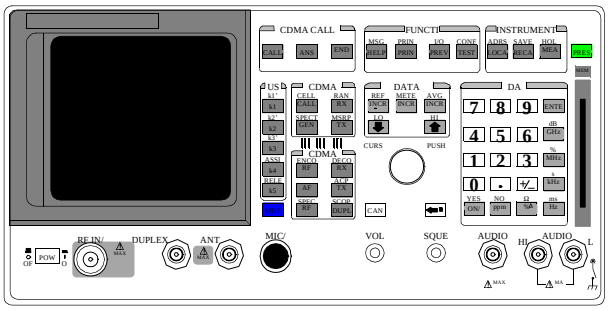
1. Press the PRESET key on the Test Set.
2. Access the ANALOG MEAS screen.
3. Set the **AF ANL In** field to **Audio In.**
4. Set **Filter 1** to **<20 Hz HPF**, and **set Filter 2** to **>99 kHz LP**.
5. Set the **De-Emphasis** field to **Off**.
6. Set the **Detector** field to **RMS**.
7. Set the audio analyzer's source to the frequencies and levels shown in the PTR (**see "AF Analyzer AC Voltage Accuracy Performance Test 14" on page 384**), adjust the level until the DVM reads the correct level.
8. Measure the ac level on the Test Set.
9. Compare the measured ac level to the limits shown in the PTR.

AF Analyzer Residual Noise Performance Test 15

Description

The AC level of the audio input is measured with no signal source connected.

Setup



This test does not need external equipment or connections.

Procedure

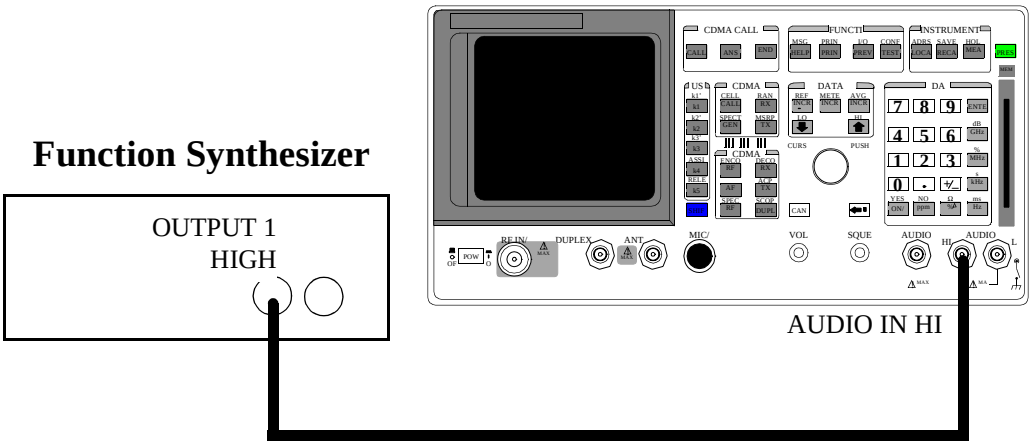
1. Press the PRESET key on the Test Set.
2. Access the ANALOG MEAS screen.
3. Set the **AFGen1** deviation to **Off** (using the ON/OFF key).
4. Set the **AF Anl In** field to **Audio In**.
5. Set **Filter 1** to **<20 Hz HPF** and **Filter 2** to **15 kHz LPF**.
6. Set the **De-Emphasis** field to **Off**.
7. Set the **Detector** field to **RMS**.
8. Measure ac level (Residual Noise). The upper limit is 150 µV. **See "AF Analyzer Residual Noise Performance Test 15" on page 385**.

AF Analyzer Distortion, SINAD, and SNR Accuracy Performance Test 16

Description

A calibrated distortion source is created by summing two audio generators. Levels are measured separately by the internal ac voltmeter. One source is set to a harmonic two or three times the frequency of the other. The measured distortion is compared with the calculated value.

Setup



Procedure

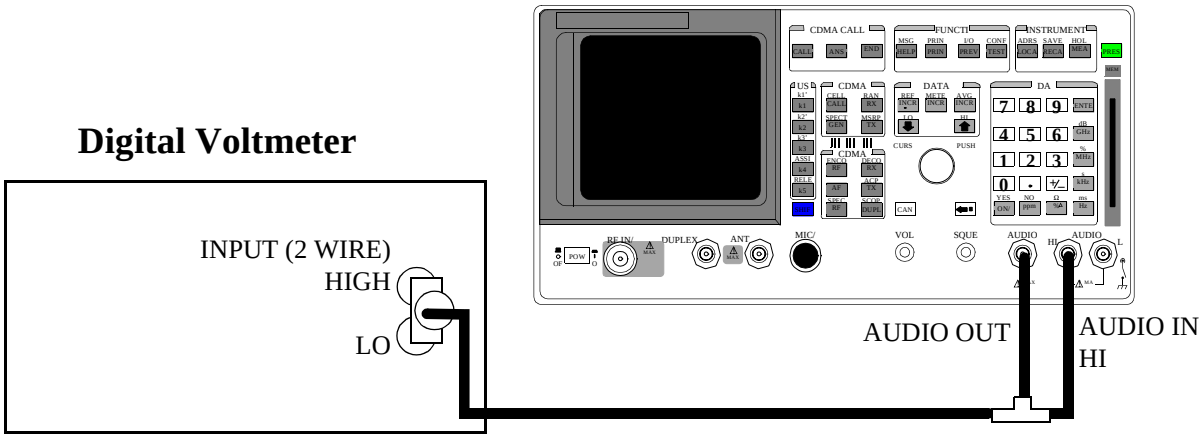
1. Press the PRESET key on the Test Set.
2. Access the AF ANALYZER screen and set **`Filter 2`** to **`15 kHz LPF`**.
3. Set the **`AF Anl In`** field to **`Audio In`**.
4. On the Function Synthesizer set **`ch A Freq`** to **`1 kHz`** and the level to **`1 V DESTN Out1`**.
5. Set **`ch B Freq`** to the Harmonic frequencies shown in the PTR **`DESTN Out1`** (**see "AF Analyzer Distortion, SINAD and SNR Accuracy Performance Test 16" on page 386**), and the **`AFGen2`** level to the distortion product levels shown in the PTR.
6. Measure the distortion and SINAD at each frequency and level, and compare the measured results with the limits shown in the PTR.
7. Measure the SNR (Signal to Noise Ratio) at each harmonic and level shown in the PTR. Compare the results to the limits shown in the PTR.

AF Analyzer DC Level Accuracy Performance Test 17

Description

To measure dc level accuracy, a dc signal is measured by an external digital voltmeter and compared to the Test Set's internal dc voltmeter reading.

Setup



Make the following digital voltmeter setting:

- DC Volts

Procedure

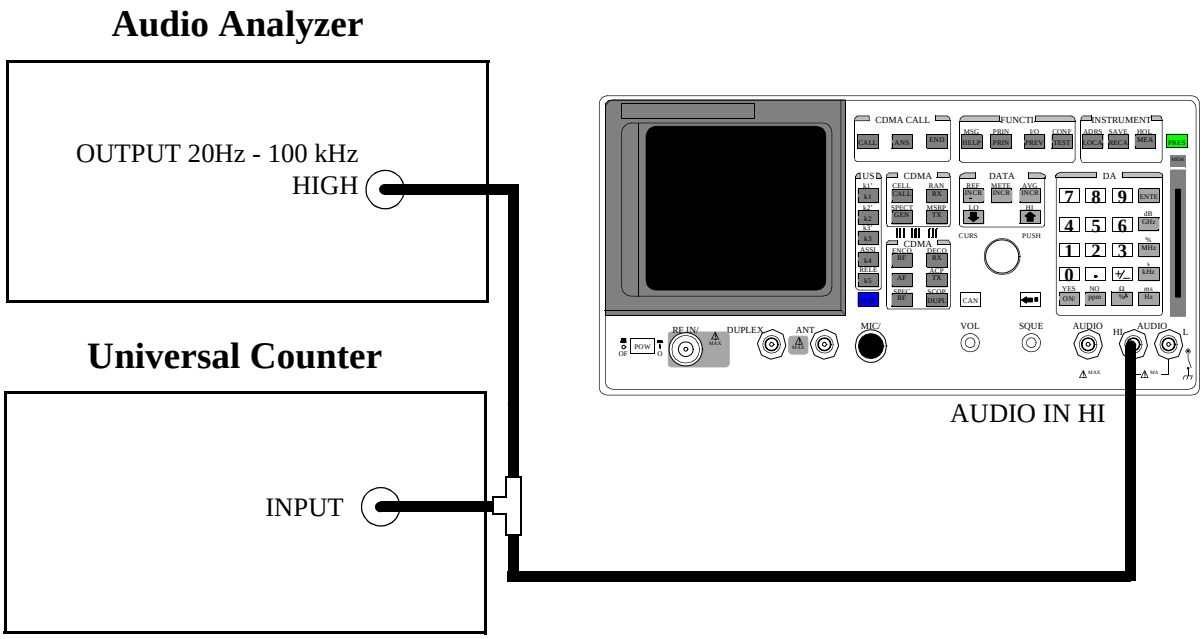
1. Press the PRESET key on the Test Set.
2. Access the ANALOG MEAS screen and set the **AF Anl In** field to **Audio In**.
3. Set the lower-right measurement to **DC Level**.
4. Set the **AFGen1 Freq** field to **0 kHz.**
5. Set the **AFGen1 To** field to **Audio Out**.
6. Set the **AFGen1** level to the levels shown in the PTR (**see "AF Analyzer DC Level Accuracy Performance Test 17" on page 388**), adjust until the voltmeter reads the correct level.
7. Read the DC Level and compare the reading to the limits shown in the PTR.

AF Analyzer Frequency Accuracy to 100 kHz Performance Test 18

Description

To measure frequency accuracy up to 100 kHz, an AC signal at the audio output is measured by the audio frequency counter in the measuring receiver and compared to the Test Set's internal audio frequency counter.

Setup



Make the following counter settings:

- Select Frequency

Procedure

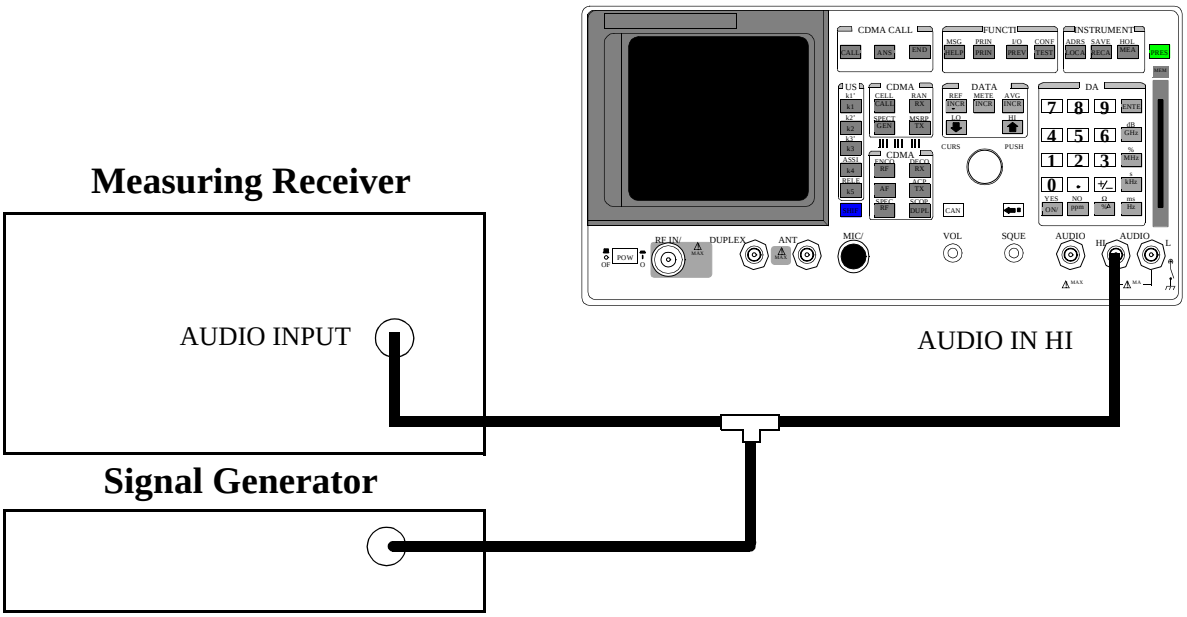
1. Press the PRESET key on the Test Set.
2. Access the ANALOG MEAS screen and set the **`AF Anl In`** field to **`Audio In`**.
3. Set **`Filter 1`** to **`<20`** and set **`Filter 2`** to **`>99 KHz LP`**.
4. Set the lower-right measurement display to **`AF Freq`**.
5. Set the audio analyzer's source amplitude to 1 V, and the frequency to the frequencies shown in the PTR (**see "AF Analyzer Frequency Accuracy to 100 kHz Performance Test 18" on page 389**), adjust until the audio frequency counter reads the correct frequencies.
6. Read the AF frequency on the measuring receiver and compare the reading to the limits shown in the PTR.

AF Analyzer Frequency Accuracy at 400 kHz Performance Test 19

Description

To measure the frequency accuracy at 400 kHz an AC signal from the Signal Generator is measured by the frequency counter in the measuring receiver and compared to the Test Set's internal RF counter.

Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- Select Audio Freq
- Select Audio Input

Make the following Signal Generator settings:

- Amplitude 0 dBm
- Frequency 400 kHz

Procedure

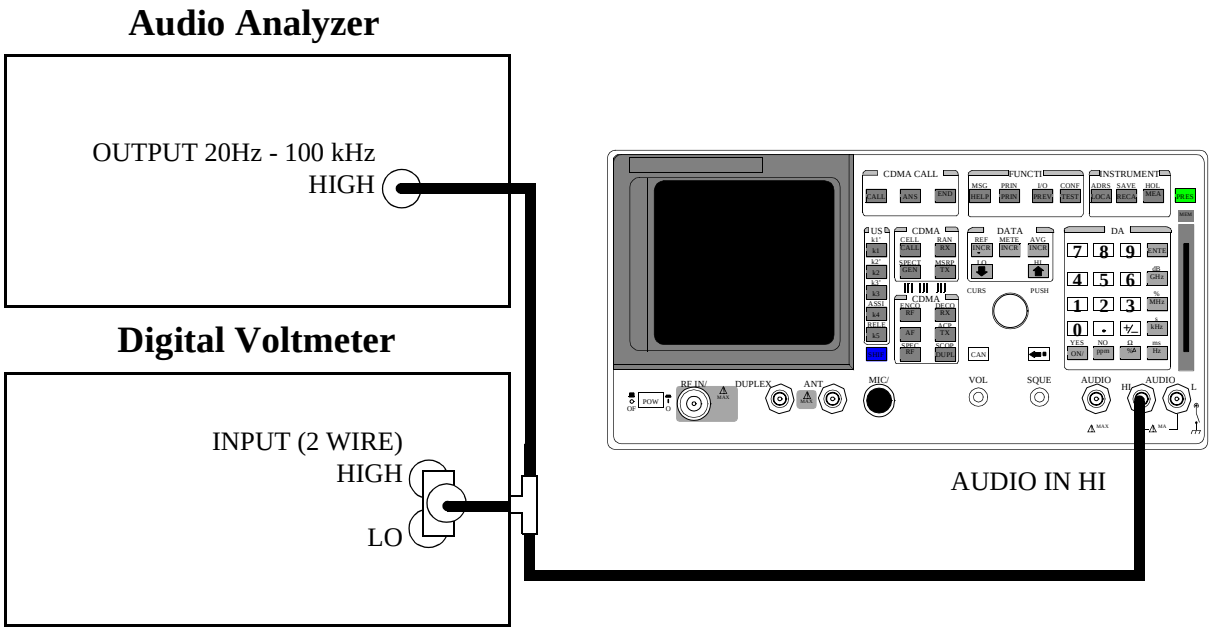
1. Press the PRESET key on the Test Set.
2. Access the ANALOG MES screen, and set the **`AF Anl In`** field to **`Audio In`**.
3. Set the **`Filter 2`** field to **`>99 kHz LP`**, and the lower-right measurement field to **`AF Freq.`**
4. Read the **`AF Freq`** on the Test Set and compare the reading to the limits shown in the PTR (**see "AF Analyzer Frequency Accuracy at 400 kHz Performance Test 19" on page 390**).

Oscilloscope Performance Test 20

Description

A 5 V AC signal from the audio analyzer is measured by both an external AC voltmeter and the Test Set's internal AC voltmeter. The measurement results are compared. Since the external AC voltmeter measures the RMS level, its level is multiplied by the square root of two to obtain the peak value measured by the oscilloscope.

Setup



Make the following digital voltmeter setting:

- AC Volts

Procedure

1. Press the PRESET key on the Test Set.
2. Access the ANALOG MEAS screen.
3. Set the **AF Anl In** field to **Audio In**.
4. Set the **Filter 2** field to **>99 kHz LP**.
5. Access the OSCILLOSCOPE screen.
6. Adjust the audio analyzer's source until the digital voltmeter reads 5 V. Adjust the frequency to the frequencies shown in the PTR (**see "Oscilloscope Performance Test 20" on page 391**).
7. Adjust the **Time/Div** field to display 2 to 3 waveforms each time the frequency is changed. (The **Time/Div** field is displayed when the **Controls** field is set to **Main**.)
8. Set the **Controls** field to **Marker**. Select the **Peak +** field (located under **Marker To**) to move the marker to the peak of the waveform. Repeat this step each time the frequency is changed.
9. Read the **Marker Lvl** and compare the reading to the limits shown in the PTR.

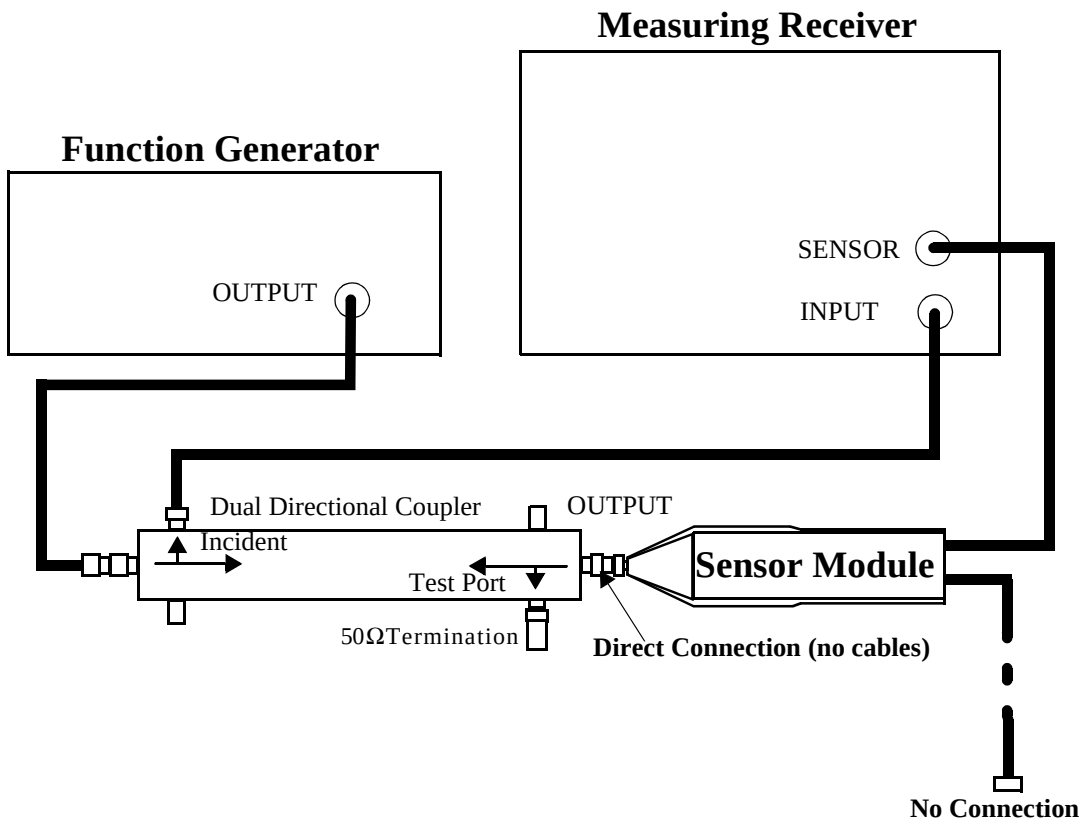
RF Analyzer Level Accuracy Performance Test 21

Description

A function generator's level is set to approximately 500 mW and measured with a power meter. Then, the power is measured with the unit-under-test, and the two measurements are compared.

A dual directional coupler is used to minimize mismatch uncertainty.

Calibration Setup



Make the following function generator settings:

- Frequency: 50 MHz
- Level: 14 V
- Waveform: Sine

NOTE: Make sure the function generator is warmed up so the frequency doesn't drift excessively during the measurement.

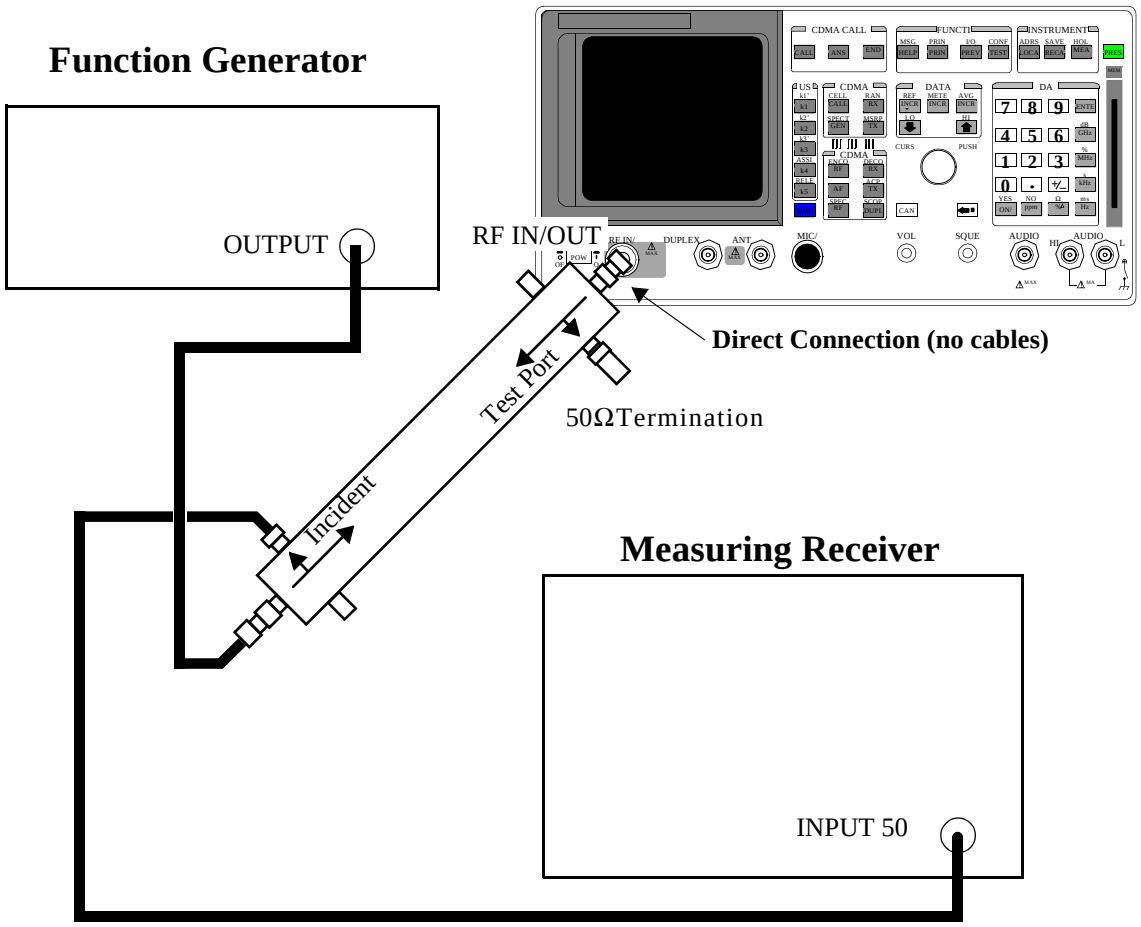
Make the following measuring receiver settings:

- Input frequency: 50 MHz
- Track mode
- RF Power measurement
- 4.4 SPCL
- 8.3 SPCL

Calibration Procedure

1. Press the PRESET key on the Test Set.
2. Make an RF POWER measurement, in watts, with the measuring receiver. Record the measured power as **`Reference power`** in step 10.
3. Disconnect the sensor cable at the measuring receiver (leave the sensor connected to the directional coupler so it will be terminated into 50 Ω).
4. Make a TUNED RF LEVEL measurement, in watts, with the measuring receiver. Record the measured level as **Tuned RF #1** in the *Measurement Procedure* in step 10.

Measurement Setup



Measurement Procedure

1. Press the PRESET key on the Test Set.
2. After replacing the sensor module with the Test Set, make a TUNED RF LEVEL measurement, in watts, with the measuring receiver. Record the measured level as **Tuned RF #2** in step 10.
3. Access the CONFIGURE screen, and set the **`RF Display`** field to **`Freq`**.
4. Set the **`Input Port`** field to **`RF In`** (on config screen).

5. Access the ANALOG MEAS screen.
6. Set the **Tune Mode** field to **`Manual`**.
7. Set the **`Tune Freq`** field to **`50 MHz`**.
8. Zero the power meter:
   a. Temporarily disconnect the Test Set from the coupler.
   b. Move the cursor to the **`TX Pwr Zero`** field and press the knob.
9. Re-connect the coupler directly to the Test Set's **RF IN/OUT** port (use no cables).
10. Read the **`TX Power`** field, in watts, and record it as **UUT Power** below.
11. Calculate the **Measured Power** as follows:

$$\text{Measured Power} = 500\text{mW}\left[\left(\frac{\text{UUT Power}}{\text{Reference Power}}\right)\left(\frac{\text{Tuned RF \#1}}{\text{Tuned RF \#2}}\right)\right]$$

The result is in mW. Record the results in the PTR (**see "RF Analyzer Level Accuracy Performance Test 21" on page 392**).

12. Set the Function Generator to 8.90 V.
13. Repeat the Calibration and Measurement procedures substituting 200 mW (in place of 500 mW) in the formula.

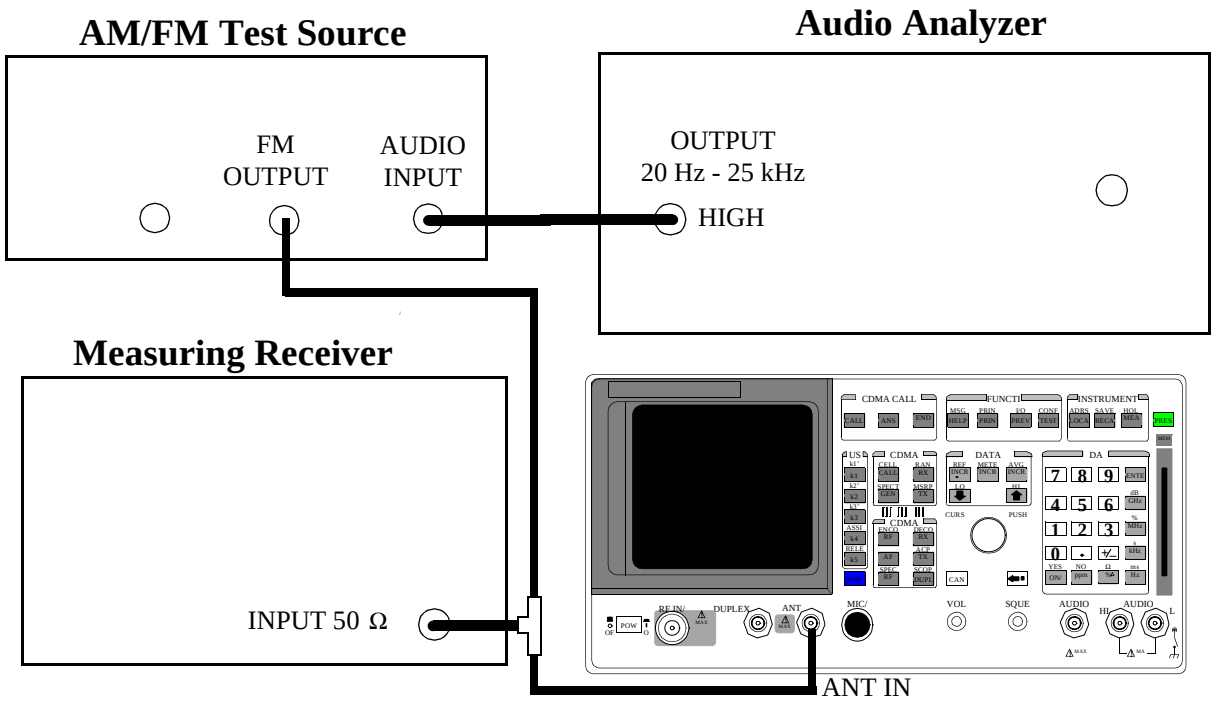
RF Analyzer FM Accuracy Performance Test 22

Description

A low noise/wide bandwidth AM/FM test source provides an RF carrier that is modulated by the audio analyzer's source. The signal is measured by the Test Set's internal RF analyzer and the measuring receiver's FM demodulator. The audio level is varied until the modulation is at the desired level as measured by the measuring receiver.

NOTE: Use the AM/FM test source output labeled **FM÷4** for 100 MHz and the output labeled **FM** for 400 MHz. You can measure the frequency with the measuring receiver and adjust it with the CARRIER FREQUENCY TUNE knob, but the exact frequency isn't critical.

Setup



Make the following AM/FM test source setting:

- Test Mode: FM

Make the following measuring receiver settings:

- Reset the measuring receiver
- FM Mode
- RMS Detector

Procedure

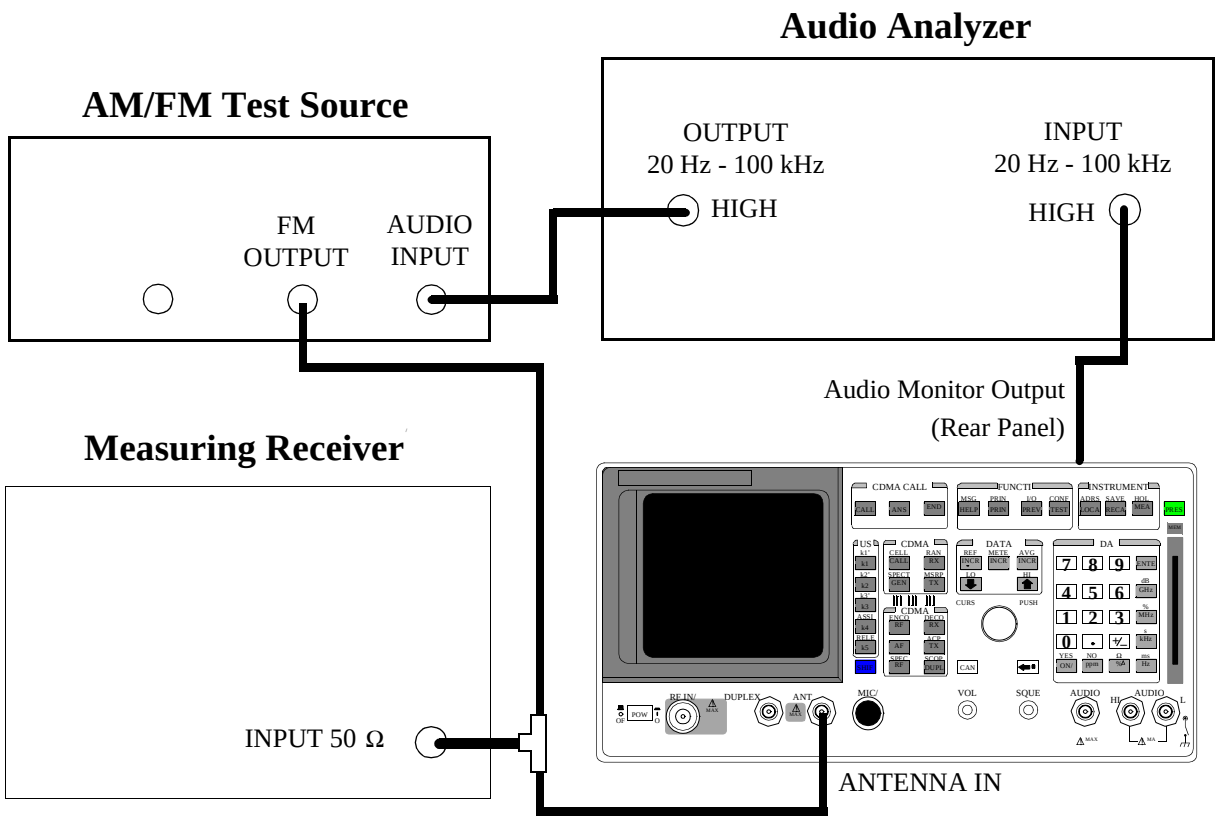
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
3. Set the **Input Port** field to **Ant**.
4. Access the ANALOG MEAS screen, and set **Tune Mode** field to **Auto**.
5. Set the **IF Filter** field to **230kHz.**
6. Set the **AF Anl In** field to **FM Demod**.
7. Set the **Filter 1** field to **<20 Hz HPF**, and set the **Filter 2** field to **>99 kHz LP**.
8. Set the **Detector** field to **RMS**.
9. Set the audio analyzer to the frequency (audio rate) shown in the PTR (**see "RF Analyzer FM Accuracy Performance Test 22" on page 393**). Adjust the audio analyzer's amplitude until the measuring receiver reads the correct deviation.
10. Read the FM Deviation on the Test Set, and compare it to the limits shown in the PTR.

RF Analyzer FM Distortion Performance Test 23

Description

A low-noise/wide-bandwidth AM/FM test source provides an RF carrier that is modulated by the audio analyzer's source. The signal is measured by the Test Set's internal RF analyzer and the measuring receiver. The audio level is varied until the modulation is at the desired FM deviation as measured by the measuring receiver. The distortion of the demodulated FM is measured by the external audio analyzer.

Setup



Make the following AM/FM test source setting:

- Test Mode: FM

Make the following measuring receiver settings:

- Reset the measuring receiver
- FM Mode
- 300 Hz High-Pass Filter
- 3 kHz Low-Pass Filter

Make the following audio source setting in the audio analyzer:

- Frequency: 1 kHz

Make the following audio analyzer setting:

- Distortion

Procedure

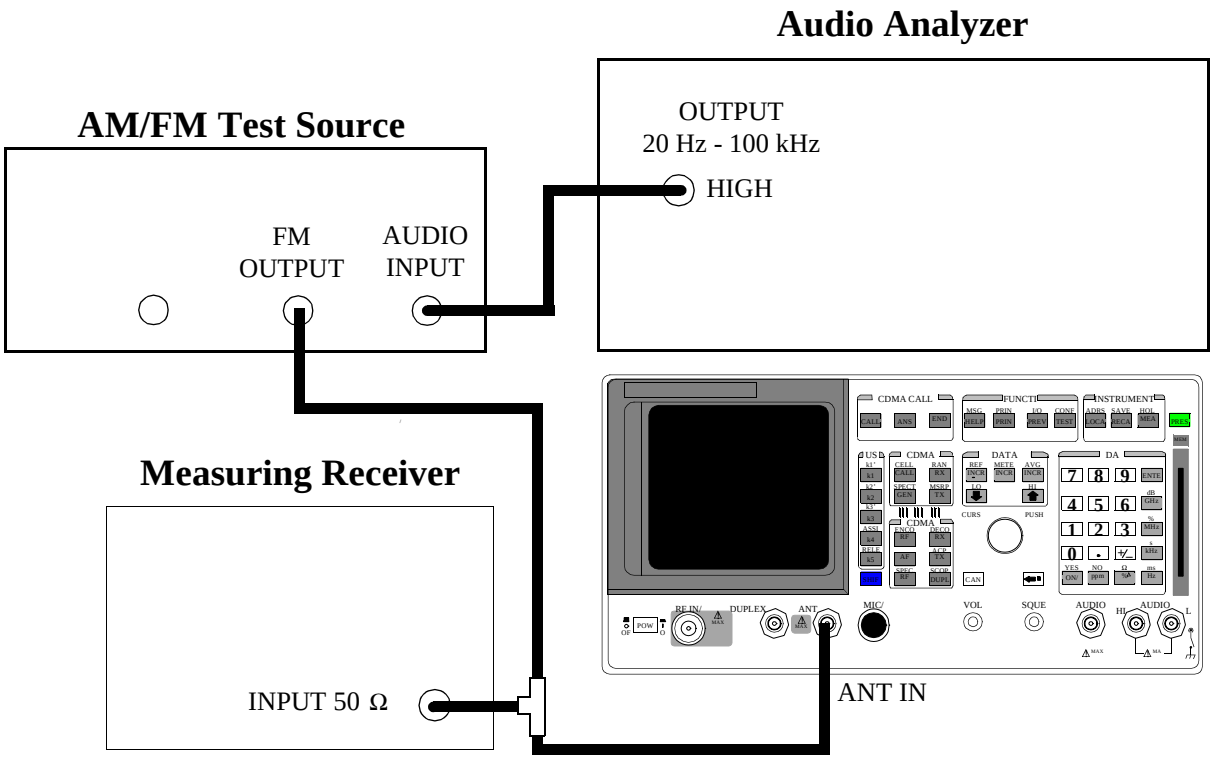
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
3. Set the **Input Por**t field to **Ant**.
4. Access the **ANALOG MEAS** screen, and set the **Tune Mode** field to **Auto**.
5. Set the **IF Filter** field to **230 kHz**.
6. Set the **AF Anl In** field to **FM Demod**..
7. Set the **Filter 1** field to **300 Hz HPF**, and set the **Filter 2** field to **3 kHz LPF**.
8. Set the **Detector** field to **Pk+**.
9. Adjust the amplitude of the audio analyzer's source until the deviation displayed on the measuring receiver matches the deviation shown in the PTR (**see "RF Analyzer FM Distortion Performance Test 23" on page 394**).
10. Read the distortion on the audio analyzer and compare the reading to the limits shown in the PTR.

RF Analyzer FM Bandwidth Performance Test 24

Description

A low noise/wide bandwidth AM/FM test source provides an RF carrier that is modulated by the audio analyzer's source. The signal is measured by the Test Set's internal RF analyzer and the measuring receiver. The audio level is varied until the modulation is at the desired level as measured by the measuring receiver. The audio rate is varied in several steps from 20 Hz to 70 kHz. The difference between the maximum and minimum FM peak deviation is noted.

Setup



Make the following AM/FM test source setting:

- Test Mode: FM

Make the following measuring receiver settings:

- Reset the measuring receiver
- FM Mode
- Filters off

Make the following audio analyzer settings:

- Frequency: 1 kHz
- Impedance: 50 [ohm]
- Amplitude: 50 mV

OR

- Frequency: 1 kHz
- Impedance: 600 [ohm]
- Amplitude: 300 mV

These settings should result in a deviation reading of about 25 kHz on the measuring receiver. Adjust the amplitude for 25 kHz deviation as read on the measuring receiver.

Procedure

1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
3. Set the **Input Port** field to **Ant**.
4. Access the ANALOG MEAS screen, and set the **Tune Mode** field to **Auto.**
5. Set the **IF Filter** field to **230kHz**.
6. Set the front-panel SQUELCH control full counter-clockwise (open).
7. Allow the Test Set to tune to the input signal, and then set the **Tune Mode** field to **Manual**.
8. Set the **AF Anl In** field to **FM Demod**. ,
9. Set the **Filter 1** field to **<20 Hz HPF**, and set the **Filter 2** field to **>99 kHz LPF.**
10. Set the **Detector** field to **Pk+**.
11. Set the audio analyzer to the following frequencies and record the FM deviation displayed on the measuring receiver for each frequency (check the deviation measured by the measuring receiver at each frequency and adjust the audio analyzer amplitude if needed to make sure it is 25 kHz): **20 Hz, 100 Hz, 1000 Hz, 10 000 Hz, 35 000 Hz, 70 000 Hz**.
12. The result of this test is the ratio of the maximum to the minimum measured deviation. Calculate the ratio in dB as follows:

$$\text{Result (dB)} = 20\log\frac{\text{max. deviation}}{\text{min. deviaiton}}$$

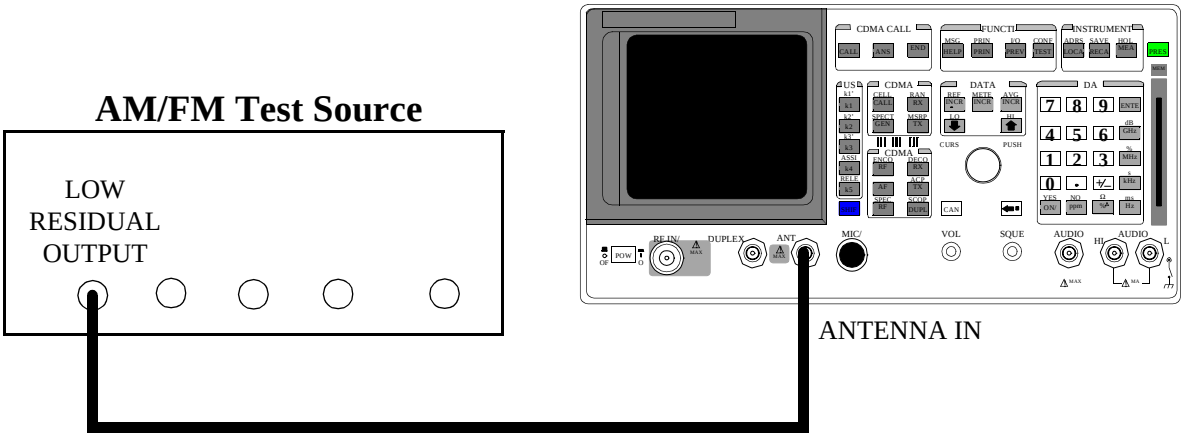
The test limit is max 3 dB. **See "RF Analyzer FM Bandwidth Performance Test 24" on page 395**.

RF Analyzer Residual FM Performance Test 25

Description

The AM/FM test source provides a CW signal with minimal residual FM. The FM is measured by the Test Set's internal RF analyzer.

Setup



Make the following AM/FM test source setting:

- Test Mode: Residual FM

Procedure

1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
3. Set the **Input Port** field to **Ant**.
4. Access the ANALOG MEAS screen, and set the **Tune Mode** field to **Auto**.
5. Set the **IF Filter** field to **230 kHz**.
6. Set the **AF Anl In** field to **FM Demod**.
7. Set the **Filter 1** field to **300 Hz HPF**, and set the **Filter 2** field to **3 kHz LPF**.
8. Set the **Detector** field to **RMS**.
9. Read the FM Deviation (residual FM) and compare to the limits shown in the PTR (**see "RF Analyzer Residual FM Performance Test 25" on page 396**).

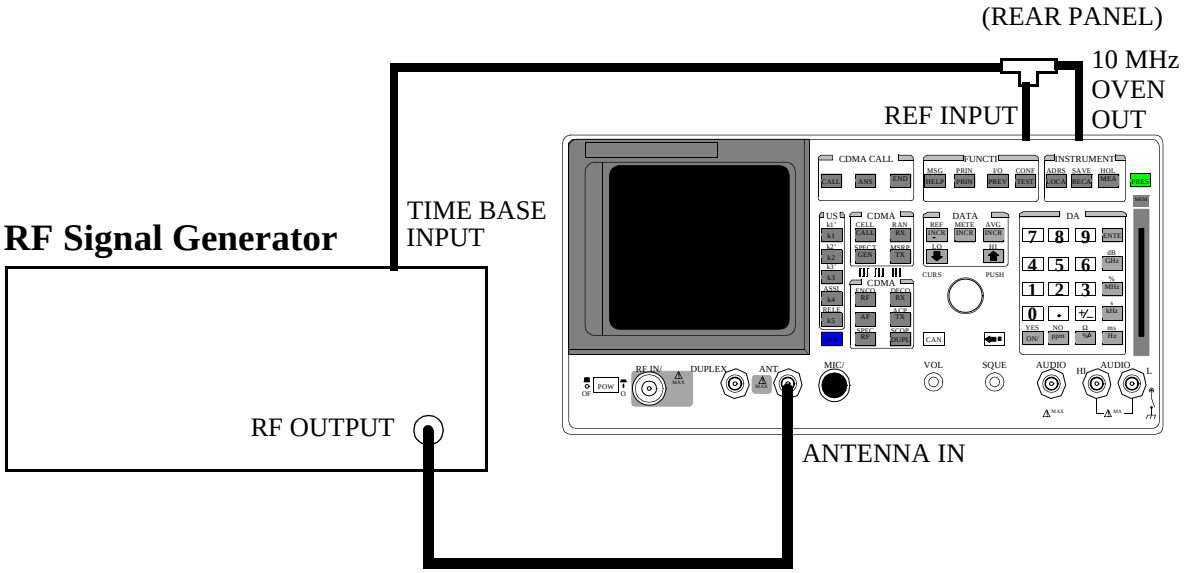
Spectrum Analyzer Image Rejection (Optional) Performance Test 26

Description

This test has two parts. The first part measures the spectrum analyzer's ability to reject image frequencies. The spectrum analyzer is tuned to a signal frequency while an image signal is applied to the ANTENNA IN connector from a signal generator.

The second part measures the spectrum analyzer's residual response at several frequencies.

Setup



Make the following signal generator settings:

- Power: –20 dBm
- Modulation: OFF

Image Rejection Procedure

1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen, and set the **RF Display** field to **Freq**.
3. Access the SPECTRUM ANALYZER screen.
4. Set the **RF In/Ant** field to **Ant.**
5. Set the **Ref Level** field to **–25 dBm**.
6. Set the **Span** field to **5 kHz**.
7. Set the signal generator's frequency, and the spectrum analyzer's **Center Freq** field, to the frequencies shown in the PTR (**see "Spectrum Analyzer Image Rejection (Option 102) Performance Test 26" on page 397**). The image response is the spectrum analyzer's marker level plus the signal generator's output level (-20 dBm).

Residual Response Procedure

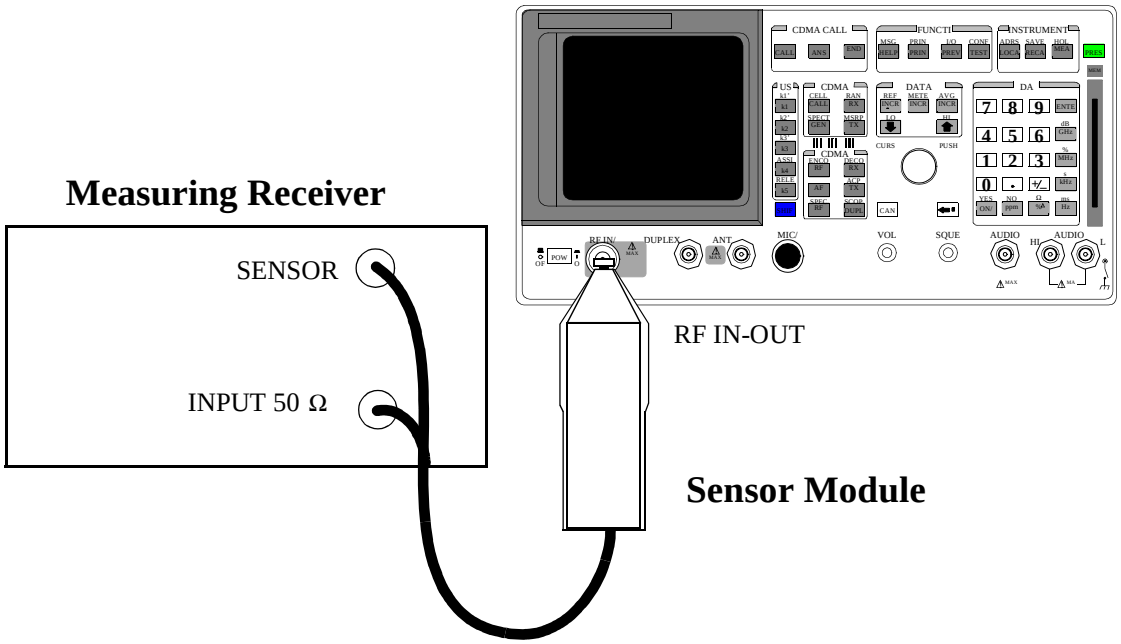
1. Press the PRESET key on the Test Set.
2. Disconnect the signal generator from the Test Set's ANTENNA IN connector.
3. Set the **Controls** field to **Auxiliary,** and set the **Input Atten** field to **Hold** and **0 dB**.
4. Set the **Controls** field to **Main.**
5. Set the **Span** field to **10 MHz**.
6. Set the **Ref Level** field to **-20 dBm**.
7. Set the **Center Freq** field to the frequencies shown in the PTR (**see "Spectrum Analyzer Image Rejection (Option 102) Performance Test 26" on page 397**) and measure the residual response on the spectrum analyzer's marker level field.

CDMA Generator RF In/Out Amplitude Level Accuracy Performance Test 27

Description

The amplitude level accuracy of the CDMA Generator at the RF IN/OUT port is measured directly with a power meter.

Calibration Setup



Make the following measuring receiver settings:

- Reset the measuring receiver
- RF power mode
- Log display

NOTE: The power sensor's calibration data must be entered into the measuring receiver and the sensor module must be zeroed. Refer to the measuring receiver's and the sensor module's operating manuals.

Procedure

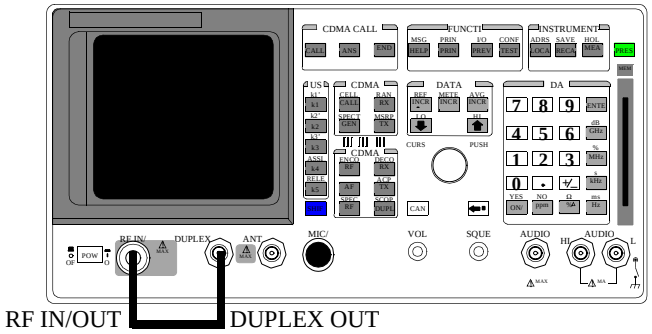
1. Press the PRESET key on the Test Set.
2. Set the **`Sector A Power`** field to the values listed in the PTR (**see "CDMA Generator RF In/Out Amplitude Level Accuracy Performance Test 27" on page 399**).

CDMA Generator Duplex Out Amplitude Level Accuracy Performance Test 28

Description

The amplitude level accuracy of the CDMA generator at the DUPLEX OUT port is measured using the CDMA analyzer.

Setup



Procedure

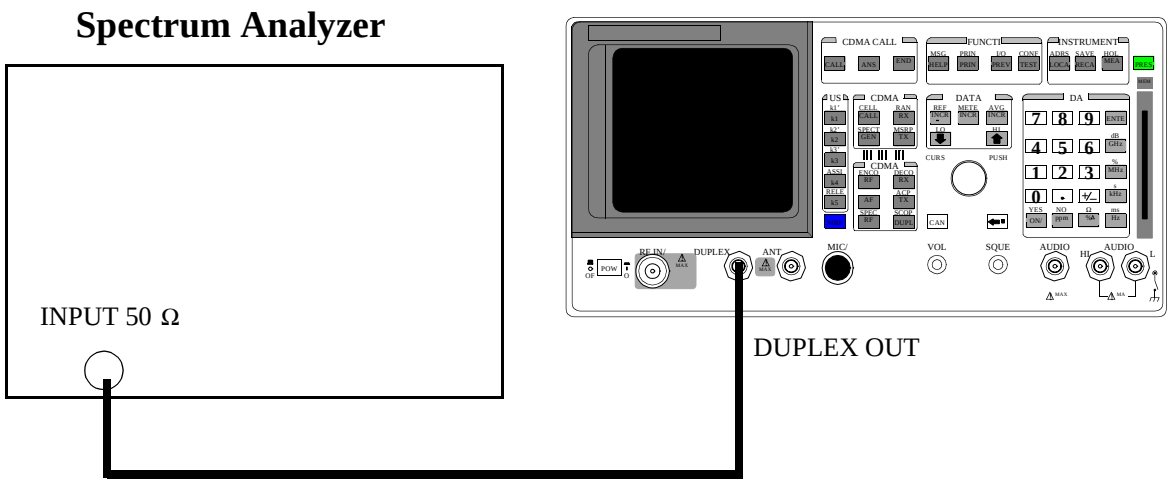
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen, and change the **`RF Display`** field to **`Freq`**.
3. Set the **`(Gen)-(Anl)`** field to **`0`**.
4. Set the **`Output Port`** to **`Dupl`**.
5. Access **`CDMA Call Control`** screen.
6. Set RF GEN Freq to 840 MHz.
7. Access the CDMA CELLULAR MOBILE TRANSMITTER TEST screen.
8. Set the **`Sector Power`** field to the values listed in the PTR for Sector Power. **See "CDMA Generator Duplex Out Amplitude Level Accuracy Performance Test 28" on page 400**.
9. Set the **`Sector Power`** field to **`Off`**.
10. Change the **`Avg Power`** measurement field to **`Chan Power`** (Channel Power).
11. Calibrate the Channel Power by selecting **`Calibrate`** in the **`Power Meas`** field.
12. Access the CDMA GENERATOR CONTROL screen.
13. Set the **`AWGN Power`** (Average Power) field to the values listed in the PTR for AWGN Power.
14. Access the CDMA CELLULAR MOBILE TRANSMITTER TEST screen and read **`Chan Power`** and record it in the PTR.

CDMA Generator Adjacent Channel Spectral Purity Performance Test 29

Description

The adjacent channel spectral purity of the CDMA generator is measured with a spectrum analyzer by comparing the RF power in the adjacent channel to the power at the center frequency of the CDMA signal. A 12 dB adder is used to convert the center frequency level to total carrier power.

Setup



Procedure

On the Test Set:

1. Press the PRESET key on the Test Set.
2. Access the CDMA CALL CTRL screen.
3. Change the **`Sector PWR`** field to **`-20 dBm/BW`**.

On the Spectrum Analyzer:

1. Set the span to 200 kHz.
2. Set the center frequency to 881.520 MHz. (This is the default center frequency of the CDMA Generator after preset.)
3. Measure the RF level: this is $\mathbf{P}_{center}$
4. Set the center frequency to the Adjacent Channel frequencies in the PTR table (**see "CDMA Generator Adjacent Channel Spectral Purity Performance Test 29" on page 401**). The measured values at these frequencies are $\mathbf{P}_{adj}$.

   Use the following equation to complete the PTR.

   $P_{relative} = P_{adj} - [P_{center} + 12]$

   $P_{relative}$ = Relative Adjacent Channel Power (dBc)

   P_{center} = Measured Center Frequency Power (dBm)

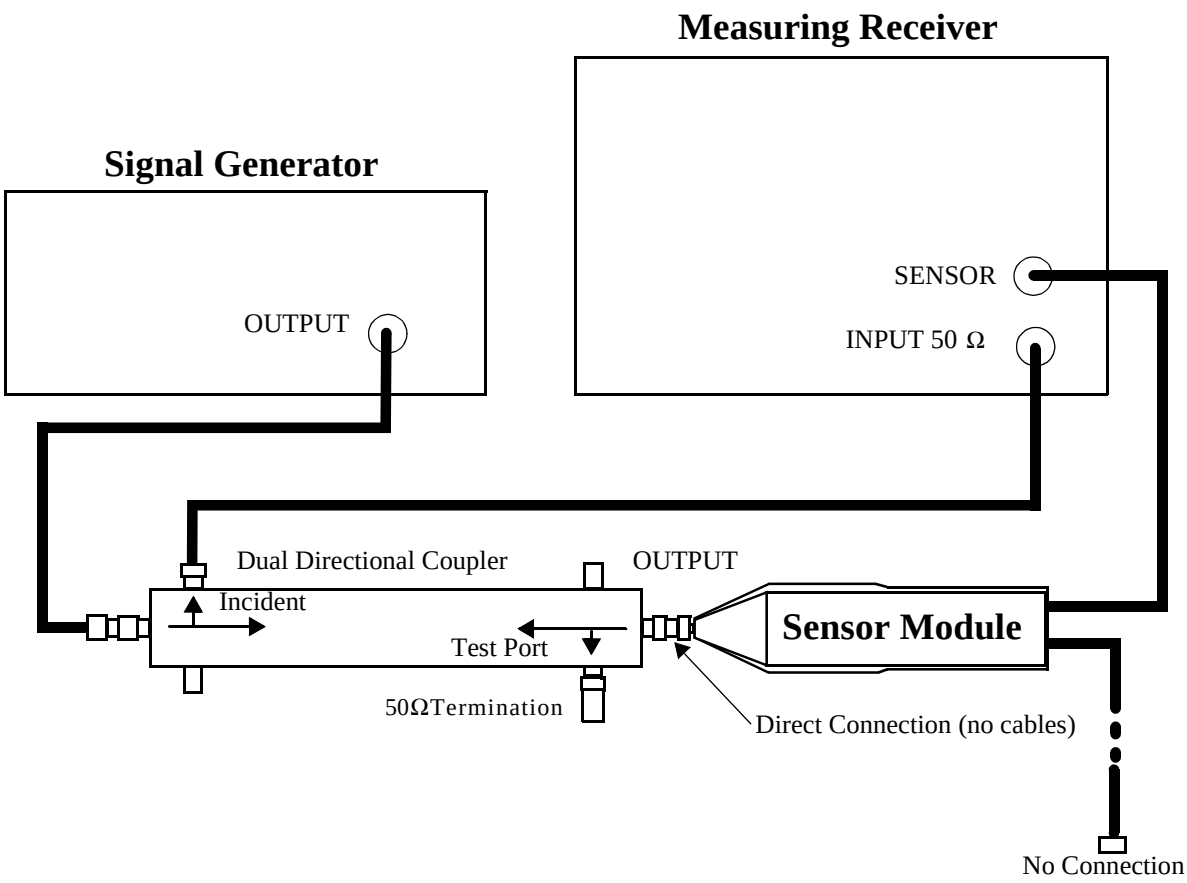
   P_{adj} = Adjacent Channel Power (dBm)

CDMA Analyzer Average Power Level Accuracy Performance Test 30

Description

The CDMA average power level accuracy is verified by comparing the measured power in a CDMA signal with the power level measured by a power meter. The signal is first measured by the power meter for a reference and then the same measurements are performed using the HP 8924E's analyzer. A dual directional coupler is used to minimize mismatch uncertainty.

Calibration Setup



Make the following signal generator setting:

- Amplitude 0 dB

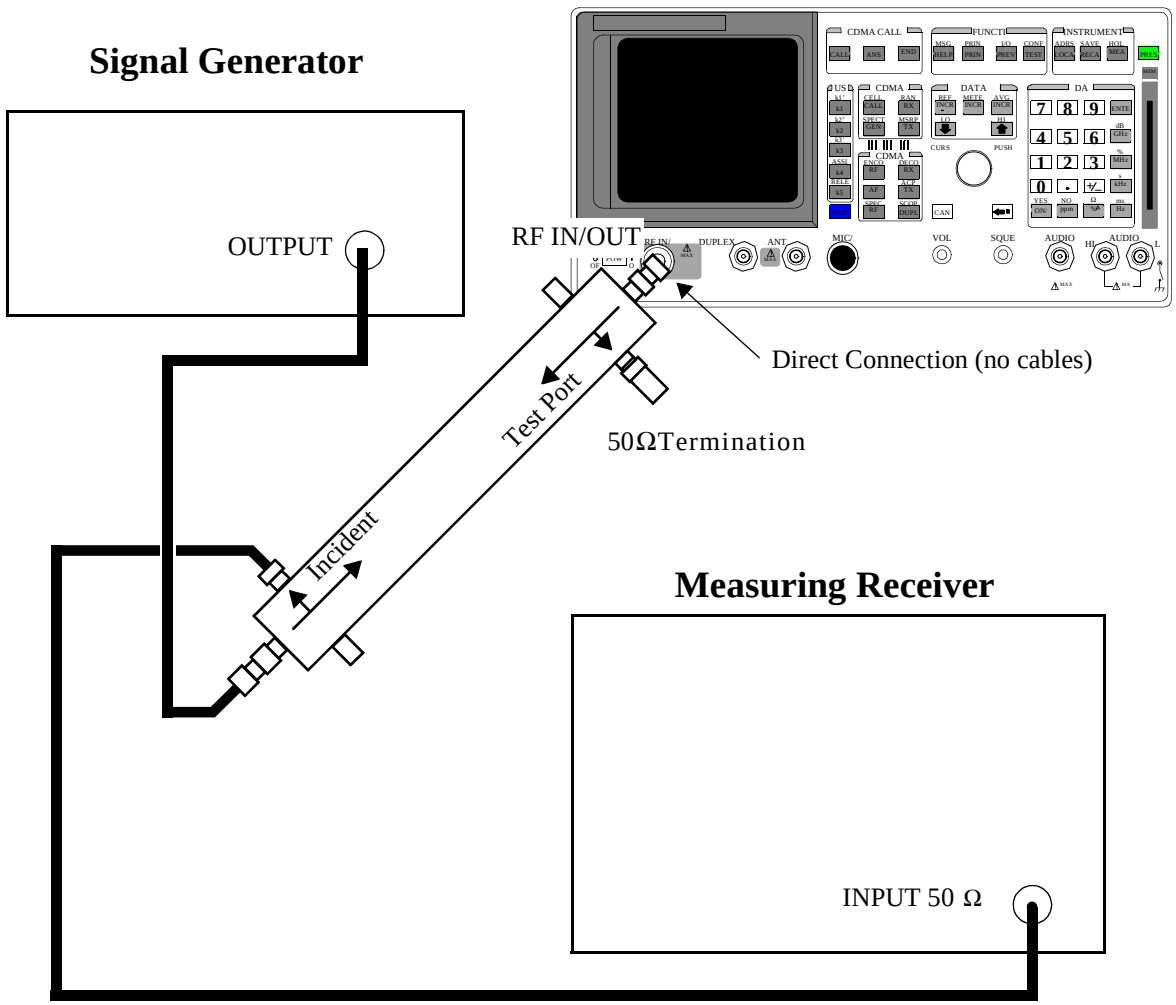
Make the following measuring receiver settings:

- Track mode
- RF Power measurement
- 4.4 SPCL
- 8.3 SPCL

Calibration Procedure

1. Press the PRESET key on the Test Set.
2. Set the signal generator and the measuring receiver to 840 MHz.
3. Make an RF POWER measurement, in mW, with the measuring receiver. Record the measured power as **Reference Power** in the *Measurement Procedure* in step 11.
4. Disconnect the sensor cable at the measuring receiver. (leave the sensor connected to the directional coupler so that it will be terminated into 50 Ω
5. Make a **TUNED RF LEVE**L measurement, in mW, with the measuring receiver. Record the measured level as **Tuned RF #1** in the *Measurement Procedure* in step 11.
6. Repeat this procedure for each of the frequencies listed in the PTR (**see "CDMA Analyzer Average Power Level Accuracy Performance Test 30" on page 402**).

Measurement Setup



Measurement Procedure

On the Measuring Receiver:

1. Press the PRESET key on the Test Set.
2. After replacing the coupler with the Test Set, make a TUNED RF LEVEL measurement, in mW, with the measuring receiver. Record the measured level as **Tune RF #2** in step 11.
3. On the Test Set push PRESET.
4. Access the CONFIGURE screen.
5. Set **(Gen) - (Anl)** to 0 MHz.
6. Set the **RF Display** field to **Freq**.
7. Access the CDMA CALL CTRL screen.
8. Change the **Avg Power** measurement units to **mW**.
9. Set the **RF Gen Freq** field to **840 MHz**.
10. Zero the power meter: a: Temporarily disconnect all RF inputs to the HP 8924E.
    a. Select **Zero** (under the **Power Meas** label).
    b. Set **Sector PWR to off.**
11. Reconnect the output of the directional coupler to the 8924E's Test Set RF IN/OUT connector (connect directly - no cables).
12. Read the **Avg Power** field in mW, and record it as **UUT Power** in step 11.
13. Calculate the Measured Power as follows:

$$\text{Measured Power} = 1\text{mW} * \frac{\text{UUT Power}}{\text{ReferencePower}} * \frac{\text{Tuned RF\#1}}{\text{Tuned RF \#2}}$$

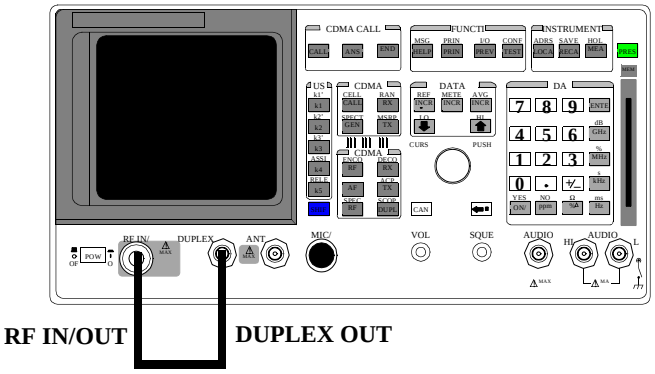
14. Repeat the Calibration and Measurement procedures for each of the frequencies listed in the PTR.

CDMA Analyzer Calibrated Tuned Channel Power Level Accuracy Performance Test 31

Description

The tuned channel power level accuracy is verified by comparing the measured power in a CW signal with the power level measured by a measuring receiver.

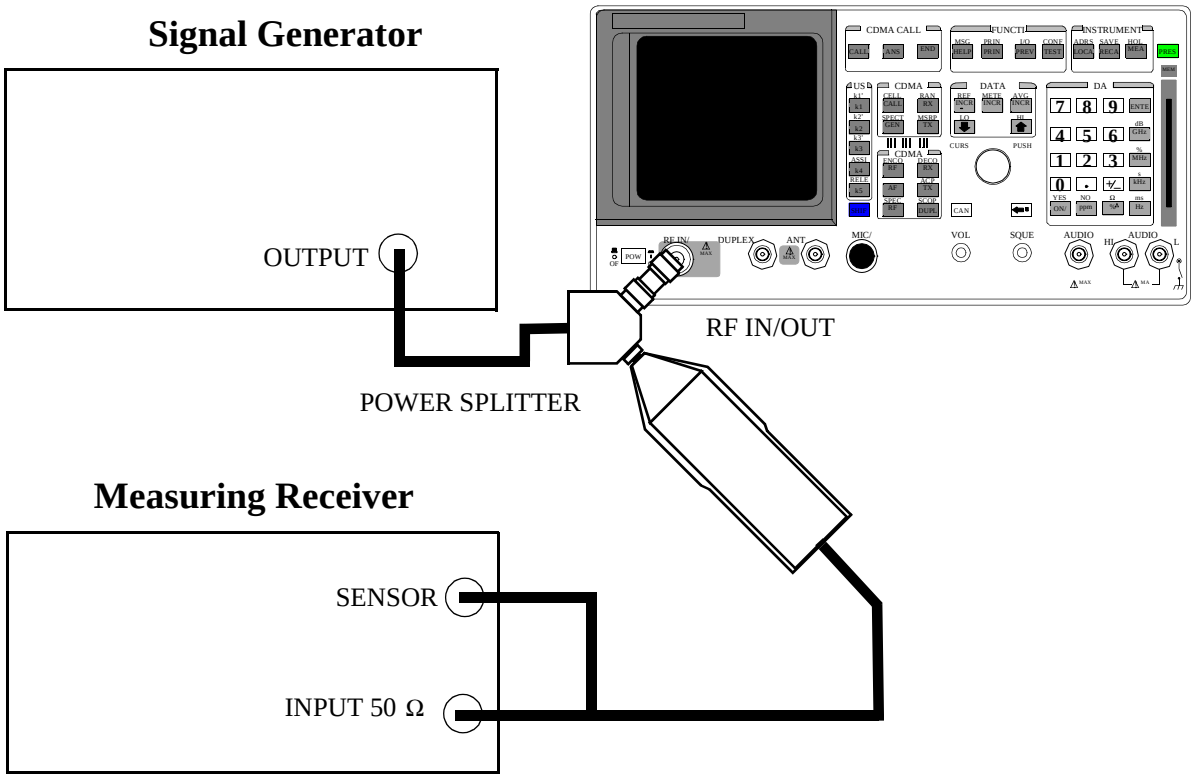
Calibration Setup



Calibration Procedure

1. Press the PRESET key on the Test Set.
2. Change the **`Avg Power`** measurement to **`Chan Power`**.
3. Select **`Calibrate`** under the **`Power Meas`** field.
4. Set the **`Sector A Power`** field to **`Off`**.

Measurement Setup



Signal Generator

Set the frequency to 840 MHz.

Set the output level to 1 dBm.

Measuring Receiver

Set the display mode to LOG.

Set the measurement to Tuned RF Level.

Calibrate the power sensor.

NOTE: The power sensor's calibration data must be entered into the measuring receiver and the sensor module must be zeroed. Refer to the measuring receiver's and the sensor module's operating manual.

Measurement Procedure

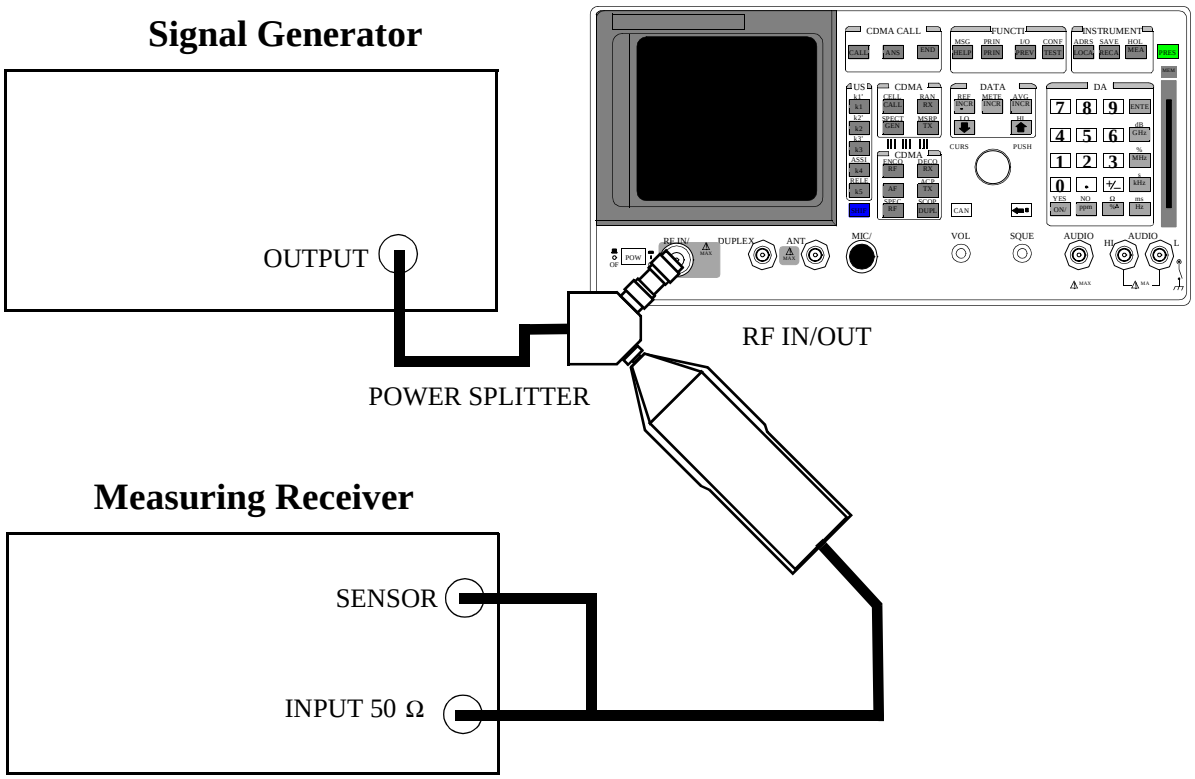
1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Set the **`RF Display`** field to **`Freq`**.
4. Set the **`(GEN)-(ANL)`** field to **`0 MHz`**.
5. Change **`Output Port`** to **`Duplex Out`**.
6. Set the **`Input Atten`** field to **`Hold`** and **`0 dB`**.
7. Access CDMA Call Control Screen.
8. Set the **`RF Gen Freq`** field to **`840 MHz`**.
9. Measure each of the RF levels in the PTR with the Test Set and the measuring receiver (**see "CDMA Analyzer Calibrated Tuned Channel Power Level Accuracy Performance Test 31" on page 403**) and record the results.

CDMA Analyzer Relative Tuned Channel Power Level Accuracy Performance Test 32

Description

The signal generator is set to approximately -10 dBm for a reference level. Then the power level is reduced in approximately 5 dB steps. The relative tuned channel power level is verified on the measuring receiver.

Setup



Signal Generator

Set the frequency to 840 MHz.

Set the output level to 1 dBm.

Measuring Receiver

Set the display mode to LOG.

Set the measurement to Tuned RF Level.

Calibrate the power sensor.

NOTE: The power sensor's calibration data must be entered into the measuring receiver and the sensor module must be zeroed. Refer to the measuring receiver's and the sensor module's operating manuals.

Procedure

1. Press the PRESET key on the Test Set.
2. Access the CONFIGURE screen.
3. Set the **`RF Display`** field to **`Freq`**.
4. Set the **`(GEN)-(ANL)`** field to **`0 MHz`**.
5. Change the **`Input Atten`** field to **`Hold`** and **`0 dB.`**
6. Access the CDMA CALL CTRL screen.
7. Set the **`Avg Power`** field to **`Chan Power.`**
8. Turn **`Sector A Power`** to **`Off`**.
9. Set the **`RF Gen Freq`** to the values listed in PTR.
10. Measure each of the RF levels in the PTR with the HP 8924E and the Measuring Receiver (**see "CDMA Analyzer Relative Tuned Channel Power Level Accuracy Performance Test 32" on page 404**).
11. Use the following measurement equation and enter the result in the PTR.

    $A_{meas} = R_{8924E} - R_{8902A}$

    A_{meas} = Measured value
    R_{8924E} = Power reading on HP 8924E
    R_{8902A} = Power Reading on Measuring Receiver
12. Change the Frequency on the Signal Generator, Measuring Receiver, and the HP 8924E to each of the values in the PTR and repeat the above procedure.

7

HP 8924C Performance Test Records

This section contains the instrument settings and measurement limits for each of the performance tests. Space is provided to record actual measurement results for future reference.

HP 8924C RF Communications Test Set

Tested By _____ Serial Number _____ Date _____

Temp _____ Humidity _____ Time _____

RF Gen FM Distortion Performance Test 1

Table 9 RF Gen FM Distortion

RF Freq (MHz)	Deviation (kHz)	Rate (kHz)	Measured FM Limits (%)		
			Lower	Upper	Actual
30	99	1	0.00	0.50	
30	5	1	0.00	0.50	
312.5	5	1	0.00	0.50	
425	50	1	0.00	0.50	
501	99	1	0.00	0.50	
501	50	1	0.00	0.50	
501	5	1	0.00	0.50	
568.75	50	1	0.00	0.50	
656.25	99	1	0.00	0.50	
656.25	50	1	0.00	0.50	
656.25	5	1	0.00	0.50	
750	99	1	0.00	0.50	
750	50	1	0.00	0.50	
750	5	1	0.00	0.50	
856.25	99	1	0.00	0.50	
856.25	50	1	0.00	0.50	
856.25	5	1	0.00	0.50	
956.25	50	1	0.00	0.50	
976.002	5	1	0.00	0.50	
1000	99	1	0.00	0.50	

Table 9 RF Gen FM Distortion (Continued)

RF Freq (MHz)	Deviation (kHz)	Rate (kHz)	Measured FM Limits (%)		
			Lower	Upper	Actual
1000	50	1	0.00	0.50	
1000	11	1	0.00	0.50	
1000	5	1	0.00	0.50	
1000	6	1	0.00	0.50	
1000	7	1	0.00	0.50	
1000	8	1	0.00	0.50	
1000	9	1	0.00	0.50	
998.401	8	1	0.00	0.50	
768.001	8	1	0.00	0.50	
512.001	8	1	0.00	0.50	
511.601	8	1	0.00	0.50	
511.201	8	1	0.00	0.50	

RF Gen FM Accuracy Performance Test 2

Table 10 RF Gen FM Accuracy

RF Freq (MHz)	Deviation (kHz)	Rate kHz)	Measured FM Deviation Limits (kHz)		
			Lower	Upper	Actual
30	99	1	95.035	102.965	
30	3	1	2.845	3.155	
312.5	3	1	2.845	3.155	
425	50	1	47.750	52.250	
501	99	1	95.035	102.965	
501	50	1	47.750	52.250	
501	3	1	2.845	3.155	
568.75	50	1	47.750	52.250	
656.25	99	1	95.035	102.965	
656.25	50	1	47.750	52.250	
656.25	3	1	2.845	3.155	
750	99	1	95.035	102.965	
750	50	1	47.750	52.250	
750	3	1	2.845	3.155	
856.25	99	1	95.035	102.965	
856.25	50	1	47.750	52.250	
856.25	3	1	2.845	3.155	
956.25	50	1	47.750	52.250	
976.002	3	1	2.845	3.155	
1000	99	1	95.035	102.965	

Table 10 RF Gen FM Accuracy (Continued)

RF Freq (MHz)	Deviation (kHz)	Rate kHz)	Measured FM Deviation Limits (kHz)		
			Lower	Upper	Actual
1000	50	1	47.750	52.250	
1000	11	1	10.115	11.885	
1000	3	1	2.845	3.155	

RF Gen FM Flatness Performance Test 3

Table 11 RF Gen FM Flatness

Level (dBm)	RF Freq (MHz)	Deviation (kHz)	Rate	Computed FM Flatness Limits (dB)		Measured Reading (kHz)	Computed Results (dB)
				Lower	Upper		
-9.1	521	50	1 kHz	-1	1		0 dB
-9.1	521	50	100 Hz	-1	1		
-9.1	521	50	200 Hz	-1	1		
-9.1	521	50	2 kHz	-1	1		
-9.1	521	50	10 kHz	-1	1		
-9.1	521	50	25 kHz	-1	1		
-9.1	975.5	50	1 kHz	-1	1		0 dB
-9.1	975.5	50	100 Hz	-1	1		
-9.1	975.5	50	200 Hz	-1	1		
-9.1	975.5	50	2 kHz	-1	1		
-9.1	975.5	50	10 kHz	-1	1		
-9.1	975.5	50	25 kHz	-1	1		

RF Gen Residual FM Performance Test 4

Table 12 RF Gen Residual FM

LO (MHz)	RF Freq (MHz)	Measured Residual FM Limits (Hz)	
		Upper	Actual
31.5	30	7	
101.5	100	7	
249.5	248	7	
251.5	250	4	
401.5	400	4	
501.5	500	4	
502.5	501	7	
512.701	511.201	7	
513.101	511.601	7	
513.501	512.001	7	
626.5	625	7	
736.5	735	7	
741.5	740	7	
746.5	745	7	
751.5	750	7	
769.501	768.001	7	
846.5	845	7	
851.5	850	7	
856.5	855	7	
866.5	865	7	

Table 12 RF Gen Residual FM (Continued)

LO (MHz)	RF Freq (MHz)	Measured Residual FM Limits (Hz)	
		Upper	Actual
901.5	900	7	
999.901	998.401	7	
1001.5	1000	7	

RF Gen Duplex Output High Level Accuracy Performance Test 5

Table 13 RF Gen High Level Accuracy at Duplex Output

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	3.5	2.500	4.500	
30	1	0.000	2.000	
100	3.5	2.500	4.500	
100	1	0.000	2.000	
300	3.5	2.500	4.500	
300	1	0.000	2.000	
687.5	3.5	2.500	4.500	
687.5	1	0.000	2.000	
800	3.5	2.500	4.500	
800	1	0.000	2.000	
900	3.5	2.500	4.500	
900	1	0.000	2.000	
1000	3.5	2.500	4.500	
1000	1	0.000	2.000	

RF Gen Duplex Output Low Level Accuracy Performance Test 6

Table 14 RF Gen Low Level Accuracy at Duplex Output

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	1	0.000	2.000	
30	-4	-5.000	-3.000	
30	-9	-10.000	-8.000	
30	-14	-15.000	-13.000	
30	-19	-20.000	-18.000	
30	-24	-25.000	-23.000	
30	-29	-30.000	-28.000	
30	-34	-35.000	-33.000	
30	-39	-40.000	-38.000	
30	-44	-45.000	-43.000	
30	-49	-50.000	-48.000	
30	-54	-55.000	-53.000	
30	-59	-60.000	-58.000	
30	-64	-65.000	-63.000	
30	-69	-70.000	-68.000	
30	-74	-75.000	-73.000	
30	-79	-80.000	-78.000	
30	-84	-85.000	-83.000	
30	-89	-90.000	-88.000	
30	-94	-95.000	-93.000	

Table 14 RF Gen Low Level Accuracy at Duplex Output (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	-99	-100.000	-98.000	
30	-104	-105.000	-103.000	
30	-109	-110.000	-108.000	
30	-114	-115.000	-113.000	
30	-119	-120.000	-118.000	
30	-124	-125.000	-123.000	
687.5	1	0.000	2.000	
687.5	-4	-5.000	-3.000	
687.5	-9	-10.000	-8.000	
687.5	-14	-15.000	-13.000	
687.5	-19	-20.000	-18.000	
687.5	-24	-25.000	-23.000	
687.5	-29	-30.000	-28.000	
687.5	-34	-35.000	-33.000	
687.5	-39	-40.000	-38.000	
687.5	-44	-45.000	-43.000	
687.5	-49	-50.000	-48.000	
687.5	-54	-55.000	-53.000	
687.5	-59	-60.000	-58.000	
687.5	-64	-65.000	-63.000	
687.5	-69	-70.000	-68.000	
687.5	-74	-75.000	-73.000	
687.5	-79	-80.000	-78.000	
687.5	-84	-85.000	-83.000	

Table 14 RF Gen Low Level Accuracy at Duplex Output (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
687.5	-89	-90.000	-88.000	
687.5	-94	-95.000	-93.000	
687.5	-99	-100.000	-98.000	
687.5	-104	-105.000	-103.000	
687.5	-109	-110.000	-108.000	
687.5	-114	-115.000	-113.000	
687.5	-119	-120.000	-118.000	
687.5	-124	-125.000	-123.000	
1000	1	0.000	2.000	
1000	-4	-5.000	-3.000	
1000	-9	-10.000	-8.000	
1000	-14	-15.000	-13.000	
1000	-19	-20.000	-18.000	
1000	-24	-25.000	-23.000	
1000	-29	-30.000	-28.000	
1000	-34	-35.000	-33.000	
1000	-39	-40.000	-38.000	
1000	-44	-45.000	-43.000	
1000	-49	-50.000	-48.000	
1000	-54	-55.000	-53.000	
1000	-59	-60.000	-58.000	
1000	-64	-65.000	-63.000	
1000	-69	-70.000	-68.000	
1000	-74	-75.000	-73.000	

Table 14 RF Gen Low Level Accuracy at Duplex Output (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
1000	-79	-80.000	-78.000	
1000	-84	-85.000	-83.000	
1000	-89	-90.000	-88.000	
1000	-94	-95.000	-93.000	
1000	-99	-100.000	-98.000	
1000	-104	-105.000	-103.000	
1000	-109	-110.000	-108.000	
1000	-114	-115.000	-113.000	
1000	-119	-120.000	-118.000	
1000	-124	-125.000	-123.000	

RF Gen RF IN/OUT Level Accuracy Performance Test 7

Table 15 RF Gen Level Accuracy at RF IN/OUT

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	-10.5	-11.7	-9.3	
30	-14	-15.2	-12.8	
30	-19	-20.200	-17.800	
30	-24	-25.200	-22.800	
30	-29	-30.200	-27.800	
30	-34	-35.200	-32.800	
30	-39	-40.200	-37.800	
30	-44	-45.200	-42.800	
30	-49	-50.200	-47.800	
30	-54	-55.200	-52.800	
30	-59	-60.200	-57.800	
30	-64	-65.200	-62.800	
30	-69	-70.200	-67.800	
30	-74	-75.200	-72.800	
30	-79	-80.200	-77.800	
30	-84	-85.200	-82.800	
30	-89	-90.200	-87.800	
30	-94	-95.200	-92.800	
30	-99	-100.200	-97.800	
30	-104	-105.200	-102.800	

Table 15 RF Gen Level Accuracy at RF IN/OUT (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	-109	-110.200	-107.800	
30	-114	-115.200	-112.800	
30	-119	-120.200	-117.800	
30	-124	-125.200	-122.800	
687.5	-10.5	-11.7	-9.3	
687.5	-14	-15.2	-12.8	
687.5	-19	-20.200	-17.800	
687.5	-24	-25.200	-22.800	
687.5	-29	-30.200	-27.800	
687.5	-34	-35.200	-32.800	
687.5	-39	-40.200	-37.800	
687.5	-44	-45.200	-42.800	
687.5	-49	-50.200	-47.800	
687.5	-54	-55.200	-52.800	
687.5	-59	-60.200	-57.800	
687.5	-64	-65.200	-62.800	
687.5	-69	-70.200	-67.800	
687.5	-74	-75.200	-72.800	
687.5	-79	-80.200	-77.800	
687.5	-84	-85.200	-82.800	
687.5	-89	-90.200	-87.800	
687.5	-94	-95.200	-92.800	
687.5	-99	-100.200	-97.800	
687.5	-104	-105.200	-102.800	

Table 15 RF Gen Level Accuracy at RF IN/OUT (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
687.5	-109	-110.200	-107.800	
687.5	-114	-115.200	-112.800	
687.5	-119	-120.200	-117.800	
687.5	-124	-125.200	-122.800	
1000	-10.5	-11.7	-9.3	
1000	-14	-15.2	-12.8	
1000	-19	-20.200	-17.800	
1000	-24	-25.200	-22.800	
1000	-29	-30.200	-27.800	
1000	-34	-35.200	-32.800	
1000	-39	-40.200	-37.800	
1000	-44	-45.200	-42.800	
1000	-49	-50.200	-47.800	
1000	-54	-55.200	-52.800	
1000	-59	-60.200	-57.800	
1000	-64	-65.200	-62.800	
1000	-69	-70.200	-67.800	
1000	-74	-75.200	-72.800	
1000	-79	-80.200	-77.800	
1000	-84	-85.200	-82.800	
1000	-89	-90.200	-87.800	
1000	-94	-95.200	-92.800	
1000	-99	-100.200	-97.800	
1000	-104	-105.200	-102.800	

Table 15 RF Gen Level Accuracy at RF IN/OUT (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
1000	-109	-110.200	-107.800	
1000	-114	-115.200	-112.800	
1000	-119	-120.200	-117.800	
1000	-124	-125.200	-122.800	

RF Gen Harmonics Spectral Purity Performance Test 8

Table 16 RF Gen Harmonics at +1 dBm

Level (dBm)	RF Freq (MHz)	Harmonic Number	Harmonic Limits (dBc)	
			Upper	Actual
+1	30	2nd	-30.000	
+1	30	3rd	-30.000	
+1	50	2nd	-30.000	
+1	50	3rd	-30.000	
+1	100	2nd	-30.000	
+1	100	3rd	-30.000	
+1	200	2nd	-30.000	
+1	200	3rd	-30.000	
+1	300	2nd	-30.000	
+1	300	3rd	-30.000	
+1	400	2nd	-30.000	
+1	400	3rd	-30.000	
+1	500	2nd	-30.000	
+1	500	3rd	-30.000	
+1	600	2nd	-30.000	
+1	600	3rd	-30.000	
+1	700	2nd	-30.000	
+1	700	3rd	-30.000	
+1	800	2nd	-30.000	
+1	800	3rd	-30.000	

Table 16 RF Gen Harmonics at +1 dBm (Continued)

Level (dBm)	RF Freq (MHz)	Harmonic Number	Harmonic Limits (dBc)	
			Upper	Actual
+1	900	2nd	-30.000	
+1	900	3rd	-30.000	
+1	1000	2nd	-30.000	
+1	1000	3rd	-30.000	

Table 17 RF Gen Harmonics at –4 dBm

Level (dBm)	RF Freq (MHz)	Harmonic Number	Harmonic Limits(dBc)	
			Upper	Actual
-4	30	2nd	-30.000	
-4	30	3rd	-30.000	
-4	50	2nd	-30.000	
-4	50	3rd	-30.000	
-4	100	2nd	-30.000	
-4	100	3rd	-30.000	
-4	200	2nd	-30.000	
-4	200	3rd	-30.000	
-4	300	2nd	-30.000	
-4	300	3rd	-30.000	
-4	400	2nd	-30.000	
-4	400	3rd	-30.000	
-4	500	2nd	-30.000	
-4	500	3rd	-30.000	
-4	600	2nd	-30.000	
-4	600	3rd	-30.000	
-4	700	2nd	-30.000	
-4	700	3rd	-30.000	
-4	800	2nd	-30.000	
-4	800	3rd	-30.000	
-4	900	2nd	-30.000	
-4	900	3rd	-30.000	
-4	1000	2nd	-30.000	

Table 17 RF Gen Harmonics at –4 dBm (Continued)

Level (dBm)	RF Freq (MHz)	Harmonic Number	Harmonic Limits(dBc)	
			Upper	Actual
-4	1000	3rd	-30.000	

Table 18 RF Gen Half-Harmonics at +1 dBm

Level (dBm)	RF Freq (MHz)	Half Frequency (MHz)	Half-Harmonic Limits (dBc)	
			Upper	Actual
+1	501	250.5	-60.000	
+1	850	425	-60.000	
+1	1000	500	-60.000	

Table 19 RF Gen Half-Harmonics at –4 dBm

Level (dBm)	RF Freq (MHz)	Half Frequency (MHz)	Half-Harmonic Limits (dBc)	
			Upper	Actual
-4	501	250.5	-60.000	
-4	850	425	-60.000	
-4	1000	500	-60.000	

RF Gen Spurious Spectral Purity Performance Test 9

Table 20 RF Gen Spurious Signal at -2.5 dBm

Spur Source	RF Freq (MHz)	Spur Freq (MHz)	Spurious Signal at +1 dBm Limits (dBc)	
			Upper	Actual
3/2 Mixer	242	274	-60.000	
3/2 Mixer	247	259	-60.000	

Table 21 RF Gen Spurious Signal at – 4 dBm

Spur Source	RF Freq (MHz)	Spur Freq (MHz)	Spurious Signal at –4 dBm Limits (dBc)	
			Upper	Actual
Supply	100	100.03	-60.000	
Supply	400	400.03	-60.000	
Supply	501	501.03	-60.000	
Supply	1000	999.97	-60.000	
Supply	100	.03	-60.000	
RF Feedthru	31	969	-60.000	
RF Feedthru	41	959	-60.000	
RF Feedthru	61	939	-60.000	
RF Feedthru	81	919	-60.000	
RF Feedthru	91	909	-60.000	
RF Feedthru	101	899	-60.000	
RF Feedthru	111	889	-60.000	
RF Feedthru	121	879	-60.000	

Table 21 RF Gen Spurious Signal at – 4 dBm (Continued)

Spur Source	RF Freq (MHz)	Spur Freq (MHz)	Spurious Signal at –4 dBm Limits (dBc)	
			Upper	Actual
3/2 Mixer	242	274	-60.000	
3/2 Mixer	247	259	-60.000	
4/3 Mixer	242	32	-60.000	
4/3 Mixer	247	12	-60.000	
5/4 Mixer	211	55	-60.000	
5/4 Mixer	217	85	-60.000	
5/4 Mixer	221	105	-60.000	
5/4 Mixer	227	135	-60.000	
5/4 Mixer	231	155	-60.000	
5/4 Mixer	237	185	-60.000	
Ref 10 MHz	165	175	-60.000	
Ref 200 kHz	150	150.2	-60.000	
Ref 200 kHz	150	149.8	-60.000	
Ref 200 kHz	150	150.4	-60.000	
Ref 200 kHz	150	149.6	-60.000	
Ref 200 kHz	150	150.6	-60.000	
Reference	150	149.4	-60.000	

AF Gen AC Level Accuracy Performance Test 10

Table 22 AF Gen AC Level Accuracy

AF Gen	Frequency (Hz)	Level (mV)	Measured AC Level Accuracy Limits (mV)		
			Lower	Upper	Actual
1	25000	4000	3885.000	4115.000	
1	25000	700	682.500	717.500	
1	25000	75	70.000	80.000	
1	10000	4000	3885.000	4115.000	
1	10000	700	682.500	717.500	
1	10000	75	70.000	80.000	
1	1000	4000	3885.000	4115.000	
1	1000	700	682.500	717.500	
1	1000	75	70.000	80.000	
1	100	4000	3885.000	4115.000	
1	100	700	682.500	717.500	
1	100	75	70.000	80.000	
2	25000	4000	3885.000	4115.000	
2	25000	700	682.500	717.500	
2	25000	75	70.000	80.000	
2	10000	4000	3885.000	4115.000	
2	10000	700	682.500	717.500	
2	10000	75	70.000	80.000	
2	1000	4000	3885.000	4115.000	
2	1000	700	682.500	717.500	

Table 22 AF Gen AC Level Accuracy (Continued)

AF Gen	Frequency (Hz)	Level (mV)	Measured AC Level Accuracy Limits (mV)		
			Lower	Upper	Actual
2	1000	75	70.000	80.000	
2	100	4000	3885.000	4115.000	
2	100	700	682.500	717.500	
2	100	75	70.000	80.000	

AF Gen DC Level Accuracy Performance Test 11

Table 23 AF Gen DC Level Accuracy

AFGen	Level (mV)	Measured DC Level Accuracy Limits (mV)		
		Lower	Upper	Actual
1	4000	3820.000	4180.000	
1	1000	925.000	1075.000	
2	4000	3820.000	4180.000	
2	1000	925.000	1075.000	

AF Gen Residual Distortion Performance Test 12

Table 24 AF Gen Residual Distortion

AFGen	Frequency (Hz)	Level (mV)	Measured Residual Distortion (%)		
			Lower	Upper	Actual
1	25000	4000	0.000	.125	
1	25000	2000	0.000	.125	
1	25000	200	0.000	.125	
1	10000	4000	0.000	.125	
1	10000	2000	0.000	.125	
1	10000	200	0.000	.125	
1	1000	4000	0.000	.125	
1	1000	2000	0.000	.125	
1	1000	200	0.000	.125	
1	100	4000	0.000	.125	
1	100	2000	0.000	.125	
1	100	200	0.000	.125	
2	25000	4000	0.000	.125	
2	25000	2000	0.000	.125	
2	25000	200	0.000	.125	
2	10000	4000	0.000	.125	
2	10000	2000	0.000	.125	
2	10000	200	0.000	.125	
2	1000	4000	0.000	.125	
2	1000	2000	0.000	.125	

Table 24 AF Gen Residual Distortion (Continued)

AFGen	Frequency (Hz)	Level (mV)	Measured Residual Distortion (%)		
			Lower	Upper	Actual
2	1000	200	0.000	.125	
2	100	4000	0.000	.125	
2	100	2000	0.000	.125	
2	100	200	0.000	.125	

AF Gen Frequency Accuracy Performance Test 13

Table 25 AF Gen Frequency Accuracy

AFGen	Frequency (Hz)	Measured Frequency (Hz)		
		Lower	Upper	Actual
1	25000	24993.750	25006.250	
1	10000	9997.500	10002.500	
1	5000	4998.750	5001.250	
1	2000	1999.500	2000.500	
1	1000	999.750	1000.250	
1	500	499.875	500.125	
1	200	199.950	200.050	
1	100	99.975	100.025	
1	50	49.988	50.012	
1	20	19.995	20.005	
2	25000	24993.750	25006.250	
2	10000	9997.500	10002.500	
2	5000	4998.750	5001.250	
2	2000	1999.500	2000.500	
2	1000	999.750	1000.250	
2	500	499.875	500.125	
2	200	199.950	200.050	
2	100	99.975	100.025	
2	50	49.988	50.012	
2	20	19.995	20.005	

AF Analyzer AC Voltage Accuracy Performance Test 14

Table 26 AF Analyzer AC Voltage Accuracy

Frequency (Hz)	Level (mV)	AC Voltage Accuracy Limits (mV)		
		Lower	Upper	Actual
15000	5000	4849.850	5150.150	
2000	5000	4849.850	5150.150	
200	5000	4849.850	5150.150	
20	5000	4849.850	5150.150	
15000	500	484.850	515.150	
2000	500	484.850	515.150	
200	500	484.850	515.150	
20	500	484.850	515.150	
15000	50	48.350	51.650	
2000	50	48.350	51.650	
200	50	48.350	51.650	
20	50	48.350	51.650	

AF Analyzer Residual Noise Performance Test 15

Table 27 AF Analyzer Residual Noise

Residual Noise μV	
Upper	**Actual**
150	

AF Analyzer Distortion, SINAD and SNR Accuracy Performance Test 16

Table 28 AF Analyzer Distortion and SINAD Accuracy

Harmonic Frequency (kHz)	Harmonic Level (V)	Measurement Type	Distortion (%) and SINAD (dB) Accuracy Limits		
			Lower	Upper	Actual
2	.1	Distortion	8.856	11.144	
2	.1	SINAD	19.043	21.043	
3	.1	Distortion	8.856	11.144	
3	.1	SINAD	19.043	21.043	
2	.01	Distortion	.890	1.120	
2	.01	SINAD	39.000	41.000	
3	.01	Distortion	.890	1.120	
3	.01	SINAD	39.000	41.000	
2	.005	Distortion	.445	.560	
2	.005	SINAD	45.021	47.021	
3	.005	Distortion	.445	.560	
3	.005	SINAD	45.021	47.021	

Table 29 SNR (Signal to Noise Ratio)

Harmonic Frequency (kHz)	Harmonic Level(V)	Measurement Type	SNR (dB) Accuracy Limits		
			Lower	Upper	Actual
2	.1	SNR	19.000	21.000	
2	.01	SNR	39.000	41.000	

AF Analyzer DC Level Accuracy Performance Test 17

Table 30 AF Analyzer DC Voltage Accuracy

Level (mV)	DC Voltage Limits (mV)		
	Lower	Upper	Actual
5000	4905.000	5095.000	
500	450.000	550.000	

AF Analyzer Frequency Accuracy to 100 kHz Performance Test 18

Table 31 AF Analyzer Frequency Accuracy to 100 kHz

Frequency (Hz)	HP 8902A Counter Limits (Hz)		
	Lower	Upper	Actual
20	19.986	20.014	
100	99.97	100.03	
1000	999.790	1000.21	
10000	9997.90	10002.1	
100000	99979	100021	

AF Analyzer Frequency Accuracy at 400 kHz Performance Test 19

Table 32 AF Analyzer Frequency Accuracy at 400 kHz

Frequency Accuracy at 400 kHz		
Lower	**Upper**	**Actual**
399.919	400.081	

Oscilloscope Performance Test 20

Table 33 Oscilloscope Amplitude Accuracy

Frequency (kHz)	Level (V)	Amplitude Limits (V)		
		Lower	Upper	Actual
1	5	6.765	7.377	
10	5	6.765	7.377	
50	5	5.000	10.000	

RF Analyzer Level Accuracy Performance Test 21

Table 34 RF Analyzer Level Accuracy

Power	Level Accuracy Limits (mW)		
	Lower	Upper	Actual
500 mW	475	525	
200 mW	190	210	

RF Analyzer FM Accuracy Performance Test 22

Table 35 RF Analyzer FM Accuracy

RF Freq (MHz)	Deviation (kHz)	Rate (Hz)	FM Accuracy Limits (kHz)		
			Lower	Upper	Actual
100	1	50	.953	1.047	
100	1	1000	.953	1.047	
100	1	25000	.953	1.047	
100	10	50	9.593	10.407	
100	10	1000	9.953	10.407	
100	10	25000	9.953	10.407	
400	10	50	9.953	10.407	
400	10	1000	9.953	10.407	
400	10	25000	9.953	10.407	
400	17	50	16.313	17.687	
400	17	1000	16.313	17.687	
400	17	25000	16.313	17.687	

RF Analyzer FM Distortion Performance Test 23

Table 36 RF Analyzer FM Distortion

Deviation (kHz)	FM Distortion Limits (%)	
	Upper	Actual
5	1.000	
25	1.000	
75	1.000	

RF Analyzer FM Bandwidth Performance Test 24

Table 37 RF Analyzer FM Bandwidth

FM Bandwidth (dB)	
Upper	**Actual**
3.0	

RF Analyzer Residual FM Performance Test 25

Table 38 RF Analyzer Residual FM

Residual FM (Hz)	
Upper	**Actual**
7	

Spectrum Analyzer Image Rejection Performance Test 26

Table 39 Image Rejection

Signal Generator Frequency(MHz) (image)	Test Set Spectrum Analyzer Center Frequency (MHz) (signal)	Measure Image Response (dB)	
		Upper Limits	Actual
613.6	385.0	–50	
873.6	645.0	–50	
883.6	655.0	–50	
1023.6	795.0	–50	
1000.0	771.4	–50	
576.4	805.0	–50	
771.0	1000.0	–50	
319.02	300.0	–50	

Table 40 Residual Response

Test Set Spectrum Analyzer Center Frequency (MHz)	Measured Residual Response (dBm)	
	Upper Limit	Actual
5.534	–70	
10.0	–70	
20.0	–70	
21.4	–70	
107.126	–70	
164.28	–70	
257.139	–70	
271.4	–70	

Table 40 Residual Response

Test Set Spectrum Analyzer Center Frequency (MHz)	Measured Residual Response (dBm)	
	Upper Limit	Actual
347.607	–70	
500.0	–70	

CDMA Generator RF In/Out Amplitude Level Accuracy Performance Test 27

Table 41 CDMA Generator RF In/Out Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
881.52	-20	-21.5	-18.5	
881.52	-25	-26.5	-23.5	

CDMA Generator Duplex Out Amplitude Level Accuracy Performance Test 28

Table 42 CDMA Generator Duplex Out Sector B Power Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual (Avg. Power)
840	-7.5	-9.0	-6.0	
840	-9	-10.5	-7.5	

Table 43 CDMA Generator Duplex Out AWGN Power Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual (Chan. Power)
840	-7.5	-9.5	-5.5	
840	-9	-11.0	-7.0	

CDMA Generator Adjacent Channel Spectral Purity Performance Test 29

Table 44 CDMA Generator Adjacent Channel Spectral Purity

Sector A RF Freq (MHz)	Adjacent Channel (MHz)	Relative Adjacent Channel Power (dBc)	
		Upper	Actual
881.52	882.415	-45	
881.52	880.625	-45	

CDMA Analyzer Average Power Level Accuracy Performance Test 30

Table 45 CDMA Analyzer Average Power Level Accuracy

RF Freq (MHz)	Level (mW)	Average Power Measurement Accuracy (mW)		
		Lower	Upper	Actual
840	1	.949	1.051	

CDMA Analyzer Calibrated Tuned Channel Power Level Accuracy Performance Test 31

Table 46 CDMA Analyzer Calibrated Tuned Chan. Power Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
840	-5	-6	-4	
840	-10	-11	-9	
840	-15	-16	-14	
840	-20	-21	-19	
840	-25	-26	-24	
840	-30	-31	-29	
840	-35	-36	-34	
840	-40	-41	-39	
840	-45	-46	-44	
840	-50	-51	-49	

CDMA Analyzer Relative Tuned Channel Power Level Accuracy Performance Test 32

Table 47 CDMA Analyzer Relative Tuned Channel Power Level Accuracy

RF Freq (MHz)	Absolute Level (dBm)	Relative Level (dB)	Relative Channel Power Measurement Accuracy (dB)		
			Lower	Upper	Actual
840	-10	0	Reference		
840	-14	-4	-0.1	0.1	
840	-19	-9	-0.1	0.1	
840	-24	-14	-0.2	0.2	
840	-29	-19	-0.2	0.2	
840	-34	-24	-0.5	0.5	
840	-39	-29	-0.5	0.5	
840	- 44	- 34	-0.5	0.5	

8

HP 8924E Performance Test Records

This section contains the instrument settings and measurement limits for each of the performance tests. Space is provided to record actual measurement results for future reference.

HP 8924E RF Communications Test Set

Tested By _____ Serial Number _____ Date _____

Temp _____ Humidity _____ Time _____

RF Gen FM Distortion Performance Test 1

Table 48 RF Gen FM Distortion

RF Freq (MHz)	Deviation (kHz)	Rate (kHz)	Measured FM Limits (%)	
			Upper	Actual
30	99	1	0.50	
30	5	1	0.50	
312.5	5	1	0.50	
425	50	1	0.50	
501	99	1	0.50	
501	50	1	0.50	
501	5	1	0.50	
568.75	50	1	0.50	
656.25	99	1	0.50	
656.25	50	1	0.50	
656.25	5	1	0.50	
750	99	1	0.50	
750	50	1	0.50	
750	5	1	0.50	
856.25	99	1	0.50	
856.25	50	1	0.50	
856.25	5	1	0.50	
956.25	50	1	0.50	
976.002	5	1	0.50	
1000	99	1	0.50	

Table 48 RF Gen FM Distortion (Continued)

RF Freq (MHz)	Deviation (kHz)	Rate (kHz)	Measured FM Limits (%)	
			Upper	Actual
1000	50	1	0.50	
1000	11	1	0.50	
1000	5	1	0.50	
1000	6	1	0.50	
1000	7	1	0.50	
1000	8	1	0.50	
1000	9	1	0.50	
998.401	8	1	0.50	
768.001	8	1	0.50	
512.001	8	1	0.50	
511.601	8	1	0.50	
511.201	8	1	0.50	

RF Gen FM Accuracy Performance Test 2

Table 49 RF Gen FM Accuracy

RF Freq (MHz)	Deviation (kHz)	Rate kHz)	Measured FM Deviation Limits (kHz)		
			Lower	Upper	Actual
30	99	1	95.035	102.965	
30	3	1	2.845	3.155	
312.5	3	1	2.845	3.155	
425	50	1	47.750	52.250	
501	99	1	95.035	102.965	
501	50	1	47.750	52.250	
501	3	1	2.845	3.155	
568.75	50	1	47.750	52.250	
656.25	99	1	95.035	102.965	
656.25	50	1	47.750	52.250	
656.25	3	1	2.845	3.155	
750	99	1	95.035	102.965	
750	50	1	47.750	52.250	
750	3	1	2.845	3.155	
856.25	99	1	95.035	102.965	
856.25	50	1	47.750	52.250	
856.25	3	1	2.845	3.155	
956.25	50	1	47.750	52.250	
976.002	3	1	2.845	3.155	
1000	99	1	95.035	102.965	

Table 49 RF Gen FM Accuracy (Continued)

RF Freq (MHz)	Deviation (kHz)	Rate kHz)	Measured FM Deviation Limits (kHz)		
			Lower	Upper	Actual
1000	50	1	47.750	52.250	
1000	11	1	10.115	11.885	
1000	3	1	2.845	3.155	

RF Gen FM Flatness Performance Test 3

Table 50 RF Gen FM Flatness

Level (dBm)	RF Freq (MHz)	Deviation (kHz)	Rate	Computed FM Flatness Limits (dB)		Measured Reading (kHz)	Computed Results (dB)
				Lower	Upper		
-9.1	521	50	1 kHz	-1	1		0 dB
-9.1	521	50	100 Hz	-1	1		
-9.1	521	50	200 Hz	-1	1		
-9.1	521	50	2 kHz	-1	1		
-9.1	521	50	10 kHz	-1	1		
-9.1	521	50	25 kHz	-1	1		
-9.1	975.5	50	1 kHz	-1	1		0 dB
-9.1	975.5	50	100 Hz	-1	1		
-9.1	975.5	50	200 Hz	-1	1		
-9.1	975.5	50	2 kHz	-1	1		
-9.1	975.5	50	10 kHz	-1	1		
-9.1	975.5	50	25 kHz	-1	1		

RF Gen Residual FM Performance Test 4

Table 51 RF Gen Residual FM

LO (MHz)	RF Freq (MHz)	Measured Residual FM Limits (Hz)	
		Upper	Actual
31.5	30	7	
101.5	100	7	
249.5	248	7	
251.5	250	4	
401.5	400	4	
501.5	500	4	
502.5	501	7	
512.701	511.201	7	
513.101	511.601	7	
513.501	512.001	7	
626.5	625	7	
736.5	735	7	
741.5	740	7	
746.5	745	7	
751.5	750	7	
769.501	768.001	7	
846.5	845	7	
851.5	850	7	
856.5	855	7	
866.5	865	7	

Table 51 RF Gen Residual FM (Continued)

LO (MHz)	RF Freq (MHz)	Measured Residual FM Limits (Hz)	
		Upper	Actual
901.5	900	7	
999.901	998.401	7	
1001.5	1000	7	

RF Gen Duplex Output High Level Accuracy Performance Test 5

Table 52 RF Gen High Level Accuracy at Duplex Output

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	3.5	2.500	4.500	
30	1	0.000	2.000	
100	3.5	2.500	4.500	
100	1	0.000	2.000	
300	3.5	2.500	4.500	
300	1	0.000	2.000	
687.5	3.5	2.500	4.500	
687.5	1	0.000	2.000	
800	3.5	2.500	4.500	
800	1	0.000	2.000	
900	3.5	2.500	4.500	
900	1	0.000	2.000	
1000	3.5	2.500	4.500	
1000	1	0.000	2.000	

RF Gen Duplex Output Low Level Accuracy Performance Test 6

Table 53 RF Gen Low Level Accuracy at Duplex Output

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	1	0.000	2.000	
30	-4	-5.000	-3.000	
30	-9	-10.000	-8.000	
30	-14	-15.000	-13.000	
30	-19	-20.000	-18.000	
30	-24	-25.000	-23.000	
30	-29	-30.000	-28.000	
30	-34	-35.000	-33.000	
30	-39	-40.000	-38.000	
30	-44	-45.000	-43.000	
30	-49	-50.000	-48.000	
30	-54	-55.000	-53.000	
30	-59	-60.000	-58.000	
30	-64	-65.000	-63.000	
30	-69	-70.000	-68.000	
30	-74	-75.000	-73.000	
30	-79	-80.000	-78.000	
30	-84	-85.000	-83.000	
30	-89	-90.000	-88.000	
30	-94	-95.000	-93.000	

Table 53 RF Gen Low Level Accuracy at Duplex Output (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	-99	-100.000	-98.000	
30	-104	-105.000	-103.000	
30	-109	-110.000	-108.000	
30	-114	-115.000	-113.000	
30	-119	-120.000	-118.000	
30	-124	-125.000	-123.000	
687.5	1	0.000	2.000	
687.5	-4	-5.000	-3.000	
687.5	-9	-10.000	-8.000	
687.5	-14	-15.000	-13.000	
687.5	-19	-20.000	-18.000	
687.5	-24	-25.000	-23.000	
687.5	-29	-30.000	-28.000	
687.5	-34	-35.000	-33.000	
687.5	-39	-40.000	-38.000	
687.5	-44	-45.000	-43.000	
687.5	-49	-50.000	-48.000	
687.5	-54	-55.000	-53.000	
687.5	-59	-60.000	-58.000	
687.5	-64	-65.000	-63.000	
687.5	-69	-70.000	-68.000	
687.5	-74	-75.000	-73.000	
687.5	-79	-80.000	-78.000	
687.5	-84	-85.000	-83.000	

Table 53 RF Gen Low Level Accuracy at Duplex Output (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
687.5	-89	-90.000	-88.000	
687.5	-94	-95.000	-93.000	
687.5	-99	-100.000	-98.000	
687.5	-104	-105.000	-103.000	
687.5	-109	-110.000	-108.000	
687.5	-114	-115.000	-113.000	
687.5	-119	-120.000	-118.000	
687.5	-124	-125.000	-123.000	
1000	1	0.000	2.000	
1000	-4	-5.000	-3.000	
1000	-9	-10.000	-8.000	
1000	-14	-15.000	-13.000	
1000	-19	-20.000	-18.000	
1000	-24	-25.000	-23.000	
1000	-29	-30.000	-28.000	
1000	-34	-35.000	-33.000	
1000	-39	-40.000	-38.000	
1000	-44	-45.000	-43.000	
1000	-49	-50.000	-48.000	
1000	-54	-55.000	-53.000	
1000	-59	-60.000	-58.000	
1000	-64	-65.000	-63.000	
1000	-69	-70.000	-68.000	
1000	-74	-75.000	-73.000	

Table 53 RF Gen Low Level Accuracy at Duplex Output (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
1000	-79	-80.000	-78.000	
1000	-84	-85.000	-83.000	
1000	-89	-90.000	-88.000	
1000	-94	-95.000	-93.000	
1000	-99	-100.000	-98.000	
1000	-104	-105.000	-103.000	
1000	-109	-110.000	-108.000	
1000	-114	-115.000	-113.000	
1000	-119	-120.000	-118.000	
1000	-124	-125.000	-123.000	

RF Gen RF IN/OUT Level Accuracy Performance Test 7

Table 54 RF Gen Level Accuracy at RF IN/OUT

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	-10.5	-11.7	-9.3	
30	-14	-15.2	-12.8	
30	-19	-20.200	-17.800	
30	-24	-25.200	-22.800	
30	-29	-30.200	-27.800	
30	-34	-35.200	-32.800	
30	-39	-40.200	-37.800	
30	-44	-45.200	-42.800	
30	-49	-50.200	-47.800	
30	-54	-55.200	-52.800	
30	-59	-60.200	-57.800	
30	-64	-65.200	-62.800	
30	-69	-70.200	-67.800	
30	-74	-75.200	-72.800	
30	-79	-80.200	-77.800	
30	-84	-85.200	-82.800	
30	-89	-90.200	-87.800	
30	-94	-95.200	-92.800	
30	-99	-100.200	-97.800	
30	-104	-105.200	-102.800	

Table 54 RF Gen Level Accuracy at RF IN/OUT (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
30	-109	-110.200	-107.800	
30	-114	-115.200	-112.800	
30	-119	-120.200	-117.800	
30	-124	-125.200	-122.800	
687.5	-10.5	-11.7	-9.3	
687.5	-14	-15.2	-12.8	
687.5	-19	-20.200	-17.800	
687.5	-24	-25.200	-22.800	
687.5	-29	-30.200	-27.800	
687.5	-34	-35.200	-32.800	
687.5	-39	-40.200	-37.800	
687.5	-44	-45.200	-42.800	
687.5	-49	-50.200	-47.800	
687.5	-54	-55.200	-52.800	
687.5	-59	-60.200	-57.800	
687.5	-64	-65.200	-62.800	
687.5	-69	-70.200	-67.800	
687.5	-74	-75.200	-72.800	
687.5	-79	-80.200	-77.800	
687.5	-84	-85.200	-82.800	
687.5	-89	-90.200	-87.800	
687.5	-94	-95.200	-92.800	
687.5	-99	-100.200	-97.800	
687.5	-104	-105.200	-102.800	

Table 54 RF Gen Level Accuracy at RF IN/OUT (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
687.5	-109	-110.200	-107.800	
687.5	-114	-115.200	-112.800	
687.5	-119	-120.200	-117.800	
687.5	-124	-125.200	-122.800	
1000	-10.5	-11.7	-9.3	
1000	-14	-15.2	-12.8	
1000	-19	-20.200	-17.800	
1000	-24	-25.200	-22.800	
1000	-29	-30.200	-27.800	
1000	-34	-35.200	-32.800	
1000	-39	-40.200	-37.800	
1000	-44	-45.200	-42.800	
1000	-49	-50.200	-47.800	
1000	-54	-55.200	-52.800	
1000	-59	-60.200	-57.800	
1000	-64	-65.200	-62.800	
1000	-69	-70.200	-67.800	
1000	-74	-75.200	-72.800	
1000	-79	-80.200	-77.800	
1000	-84	-85.200	-82.800	
1000	-89	-90.200	-87.800	
1000	-94	-95.200	-92.800	
1000	-99	-100.200	-97.800	
1000	-104	-105.200	-102.800	

Table 54 RF Gen Level Accuracy at RF IN/OUT (Continued)

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
1000	-109	-110.200	-107.800	
1000	-114	-115.200	-112.800	
1000	-119	-120.200	-117.800	
1000	-124	-125.200	-122.800	

RF Gen Harmonics Spectral Purity Performance Test 8

Table 55 RF Gen Harmonics at +1 dBm

Level (dBm)	RF Freq (MHz)	Harmonic Number	Harmonic Limits (dBc)	
			Upper	Actual
+1	30	2nd	-30.000	
+1	30	3rd	-30.000	
+1	50	2nd	-30.000	
+1	50	3rd	-30.000	
+1	100	2nd	-30.000	
+1	100	3rd	-30.000	
+1	200	2nd	-30.000	
+1	200	3rd	-30.000	
+1	300	2nd	-30.000	
+1	300	3rd	-30.000	
+1	400	2nd	-30.000	
+1	400	3rd	-30.000	
+1	500	2nd	-30.000	
+1	500	3rd	-30.000	
+1	600	2nd	-30.000	
+1	600	3rd	-30.000	
+1	700	2nd	-30.000	
+1	700	3rd	-30.000	
+1	800	2nd	-30.000	
+1	800	3rd	-30.000	

Table 55 RF Gen Harmonics at +1 dBm (Continued)

Level (dBm)	RF Freq (MHz)	Harmonic Number	Harmonic Limits (dBc)	
			Upper	Actual
+1	900	2nd	-30.000	
+1	900	3rd	-30.000	
+1	1000	2nd	-30.000	
+1	1000	3rd	-30.000	

Table 56 RF Gen Harmonics at –4 dBm

Level (dBm)	RF Freq (MHz)	Harmonic Number	Harmonic Limits(dBc)	
			Upper	Actual
-4	30	2nd	-30.000	
-4	30	3rd	-30.000	
-4	50	2nd	-30.000	
-4	50	3rd	-30.000	
-4	100	2nd	-30.000	
-4	100	3rd	-30.000	
-4	200	2nd	-30.000	
-4	200	3rd	-30.000	
-4	300	2nd	-30.000	
-4	300	3rd	-30.000	
-4	400	2nd	-30.000	
-4	400	3rd	-30.000	
-4	500	2nd	-30.000	
-4	500	3rd	-30.000	
-4	600	2nd	-30.000	
-4	600	3rd	-30.000	
-4	700	2nd	-30.000	
-4	700	3rd	-30.000	
-4	800	2nd	-30.000	
-4	800	3rd	-30.000	
-4	900	2nd	-30.000	
-4	900	3rd	-30.000	
-4	1000	2nd	-30.000	
-4	1000	3rd	-30.000	

Table 57 RF Gen Half-Harmonics at +1 dBm

Level (dBm)	RF Freq (MHz)	Half Frequency (MHz)	Half-Harmonic Limits (dBc)	
			Upper	Actual
+1	501	250.5	-60.000	
+1	850	425	-60.000	
+1	1000	500	-60.000	

Table 58 RF Gen Half-Harmonics at −4 dBm

Level (dBm)	RF Freq (MHz)	Half Frequency (MHz)	Half-Harmonic Limits (dBc)	
			Upper	Actual
-4	501	250.5	-60.000	
-4	850	425	-60.000	
-4	1000	500	-60.000	

RF Gen Spurious Spectral Purity Performance Test 9

Table 59 RF Gen Spurious Signal at -2.5 dBm

Spur Source	RF Freq (MHz)	Spur Freq (MHz)	Spurious Signal at +1 dBm Limits (dBc)	
			Upper	Actual
3/2 Mixer	242	274	-60.000	
3/2 Mixer	247	259	-60.000	

Table 60 RF Gen Spurious Signal at – 4 dBm

Spur Source	RF Freq (MHz)	Spur Freq (MHz)	Spurious Signal at –4 dBm Limits (dBc)	
			Upper	Actual
Supply	100	100.03	-60.000	
Supply	400	400.03	-60.000	
Supply	501	501.03	-60.000	
Supply	1000	999.97	-60.000	
Supply	100	.03	-60.000	
RF Feedthru	31	969	-60.000	
RF Feedthru	41	959	-60.000	
RF Feedthru	61	939	-60.000	
RF Feedthru	81	919	-60.000	
RF Feedthru	91	909	-60.000	
RF Feedthru	101	899	-60.000	
RF Feedthru	111	889	-60.000	
RF Feedthru	121	879	-60.000	

Table 60 RF Gen Spurious Signal at – 4 dBm (Continued)

Spur Source	RF Freq (MHz)	Spur Freq (MHz)	Spurious Signal at –4 dBm Limits (dBc)	
			Upper	Actual
3/2 Mixer	242	274	-60.000	
3/2 Mixer	247	259	-60.000	
4/3 Mixer	242	32	-60.000	
4/3 Mixer	247	12	-60.000	
5/4 Mixer	211	55	-60.000	
5/4 Mixer	217	85	-60.000	
5/4 Mixer	221	105	-60.000	
5/4 Mixer	227	135	-60.000	
5/4 Mixer	231	155	-60.000	
5/4 Mixer	237	185	-60.000	
Ref 10 MHz	165	175	-60.000	
Ref 200 kHz	150	150.2	-60.000	
Ref 200 kHz	150	149.8	-60.000	
Ref 200 kHz	150	150.4	-60.000	
Ref 200 kHz	150	149.6	-60.000	
Ref 200 kHz	150	150.6	-60.000	
Reference	150	149.4	-60.000	

AF Gen AC Level Accuracy Performance Test 10

Table 61 AF Gen AC Level Accuracy

AF Gen	Frequency (Hz)	Level (mV)	Measured AC Level Accuracy Limits (mV)		
			Lower	Upper	Actual
	10000	4000	3885.000	4115.000	
	10000	700	682.500	717.500	
	10000	75	70.000	80.000	
	1000	4000	3885.000	4115.000	
	1000	700	682.500	717.500	
	1000	75	70.000	80.000	
	300	4000	3885.000	4115.000	
	300	700	682.500	717.500	
	300	75	70.000	80.000	
			70.000	80.000	
			3885.000	4115.000	
			682.500	717.500	
			70.000	80.000	

AF Gen Residual Distortion Performance Test 12

Table 62 AF Gen Residual Distortion

AFGen	Frequency (Hz)	Level (mV)	Measured Residual Distortion (%)		
			Lower	Upper	Actual
	10000	4000	0.000	.125	
	10000	2000	0.000	.125	
	10000	200	0.000	.125	
	1000	4000	0.000	.125	
	1000	2000	0.000	.125	
	1000	200	0.000	.125	
	300	4000	0.000	.125	
	300	2000	0.000	.125	
	300	200	0.000	.125	

AF Gen Frequency Accuracy Performance Test 13

Table 63 AF Gen Frequency Accuracy

Frequency (Hz)	Measured Frequency (Hz)		
	Lower	Upper	Actual
10000	9997.500	10002.500	
5000	4998.750	5001.250	
2000	1999.500	2000.500	
1000	999.750	1000.250	
500	499.875	500.125	
300	199.950	200.050	

AF Analyzer AC Voltage Accuracy Performance Test 14

Table 64 AF Analyzer AC Voltage Accuracy

Frequency (Hz)	Level (mV)	AC Voltage Accuracy Limits (mV)		
		Lower	Upper	Actual
15000	5000	4849.850	5150.150	
2000	5000	4849.850	5150.150	
200	5000	4849.850	5150.150	
20	5000	4849.850	5150.150	
15000	500	484.850	515.150	
2000	500	484.850	515.150	
200	500	484.850	515.150	
20	500	484.850	515.150	
15000	50	48.350	51.650	
2000	50	48.350	51.650	
200	50	48.350	51.650	
20	50	48.350	51.650	

AF Analyzer Residual Noise Performance Test 15

Table 65 AF Analyzer Residual Noise

Residual Noise μV	
Upper	**Actual**
150	

AF Analyzer Distortion, SINAD and SNR Accuracy Performance Test 16

Table 66 AF Analyzer Distortion and SINAD Accuracy

Harmonic Frequency (kHz)	Harmonic Level (V)	Measurement Type	Distortion (%) and SINAD (dB) Accuracy Limits		
			Lower	Upper	Actual
2	.1	Distortion	8.856	11.144	
2	.1	SINAD	19.043	21.043	
3	.1	Distortion	8.856	11.144	
3	.1	SINAD	19.043	21.043	
2	.01	Distortion	.890	1.120	
2	.01	SINAD	39.000	41.000	
3	.01	Distortion	.890	1.120	
3	.01	SINAD	39.000	41.000	
2	.005	Distortion	.445	.560	
2	.005	SINAD	45.021	47.021	
3	.005	Distortion	.445	.560	
3	.005	SINAD	45.021	47.021	

Table 67 SNR (Signal to Noise Ratio)

Harmonic Frequency (kHz)	Harmonic Level(V)	Measurement Type	SNR (dB) Accuracy Limits		
			Lower	Upper	Actual
2	.1	SNR	19.000	21.000	
2	.01	SNR	39.000	41.000	

AF Analyzer DC Level Accuracy Performance Test 17

Table 68 AF Analyzer DC Voltage Accuracy

Level (mV)	DC Voltage Limits (mV)		
	Lower	Upper	Actual
5000	4905.000	5095.000	
500	450.000	550.000	

AF Analyzer Frequency Accuracy to 100 kHz Performance Test 18

Table 69 AF Analyzer Frequency Accuracy to 100 kHz

Frequency (Hz)	HP 8902A Counter Limits (Hz)		
	Lower	Upper	Actual
20	19.986	20.014	
100	99.97	100.03	
1000	999.790	1000.21	
10000	9997.90	10002.1	
100000	99979	100021	

AF Analyzer Frequency Accuracy at 400 kHz Performance Test 19

Table 70 AF Analyzer Frequency Accuracy at 400 kHz

Frequency Accuracy at 400 kHz		
Lower	**Upper**	**Actual**
399.919	400.081	

Oscilloscope Performance Test 20

Table 71 Oscilloscope Amplitude Accuracy

Frequency (kHz)	Level (V)	Amplitude Limits (V)		
		Lower	Upper	Actual
1	5	6.765	7.377	
10	5	6.765	7.377	
50	5	5.000	10.000	

RF Analyzer Level Accuracy Performance Test 21

Table 72 RF Analyzer Level Accuracy

Power	Level Accuracy Limits (mW)		
	Lower	Upper	Actual
500 mW	475	525	
200 mW	190	210	

RF Analyzer FM Accuracy Performance Test 22

Table 73 RF Analyzer FM Accuracy

RF Freq (MHz)	Deviation (kHz)	Rate (Hz)	FM Accuracy Limits (kHz)		
			Lower	Upper	Actual
100	1	50	.953	1.047	
100	1	1000	.953	1.047	
100	1	25000	.953	1.047	
100	10	50	9.593	10.407	
100	10	1000	9.953	10.407	
100	10	25000	9.953	10.407	
400	10	50	9.953	10.407	
400	10	1000	9.953	10.407	
400	10	25000	9.953	10.407	
400	17	50	16.313	17.687	
400	17	1000	16.313	17.687	
400	17	25000	16.313	17.687	

RF Analyzer FM Distortion Performance Test 23

Table 74 RF Analyzer FM Distortion

Deviation (kHz)	FM Distortion Limits (%)	
	Upper	Actual
5	1.000	
25	1.000	
75	1.000	

RF Analyzer FM Bandwidth Performance Test 24

Table 75 RF Analyzer FM Bandwidth

FM Bandwidth (dB)	
Upper	**Actual**
3.0	

RF Analyzer Residual FM Performance Test 25

Table 76 RF Analyzer Residual FM

Residual FM (Hz)	
Upper	**Actual**
7	

Spectrum Analyzer Image Rejection (Option 102) Performance Test 26

Table 77 Image Rejection

Signal Generator Frequency(MHz) (image)	Test Set Spectrum Analyzer Center Frequency (MHz) (signal)	Measure Image Response (dB)	
		Upper Limits	Actual
613.6	385.0	–50	
873.6	645.0	–50	
883.6	655.0	–50	
1023.6	795.0	–50	
1000.0	771.4	–50	
576.4	805.0	–50	
771.0	1000.0	–50	
319.02	300.0	–50	

Table 78 Residual Response

Test Set Spectrum Analyzer Center Frequency (MHz)	Measured Residual Response (dBm)	
	Upper Limit	Actual
5.534	–70	
10.0	–70	
20.0	–70	
21.4	–70	
107.126	–70	
164.28	–70	
257.139	–70	
271.4	–70	

Table 78 Residual Response

Test Set Spectrum Analyzer Center Frequency (MHz)	Measured Residual Response (dBm)	
	Upper Limit	Actual
347.607	–70	
500.0	–70	

CDMA Generator RF In/Out Amplitude Level Accuracy Performance Test 27

Table 79 CDMA Generator RF In/Out Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
881.52	-20	-21.5	-18.5	
881.52	-25	-26.5	-23.5	

CDMA Generator Duplex Out Amplitude Level Accuracy Performance Test 28

Table 80 CDMA Generator Duplex Out Sector Power Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual (Avg. Power)
840	-7.5	-9.0	-6.0	
840	-9	-10.5	-7.5	

Table 81 CDMA Generator Duplex Out AWGN Power Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual (Chan. Power)
840	-7.5	-9.5	-5.5	
840	-9	-11.0	-7.0	

CDMA Generator Adjacent Channel Spectral Purity Performance Test 29

Table 82 CDMA Generator Adjacent Channel Spectral Purity

Sector A RF Freq (MHz)	Adjacent Channel (MHz)	Relative Adjacent Channel Power (dBc)	
		Upper	Actual
881.52	882.415	-45	
881.52	880.625	-45	

CDMA Analyzer Average Power Level Accuracy Performance Test 30

Table 83 CDMA Analyzer Average Power Level Accuracy

RF Freq (MHz)	Level (mW)	Average Power Measurement Accuracy (mW)		
		Lower	Upper	Actual
840	1	.949	1.051	

CDMA Analyzer Calibrated Tuned Channel Power Level Accuracy Performance Test 31

Table 84 CDMA Analyzer Calibrated Tuned Chan. Power Level Accuracy

RF Freq (MHz)	Level (dBm)	Measured Level Limits (dBm)		
		Lower	Upper	Actual
840	-5	-6	-4	
840	-10	-11	-9	
840	-15	-16	-14	
840	-20	-21	-19	
840	-25	-26	-24	
840	-30	-31	-29	
840	-35	-36	-34	
840	-40	-41	-39	
840	-45	-46	-44	
840	-50	-51	-49	

CDMA Analyzer Relative Tuned Channel Power Level Accuracy Performance Test 32

Table 85 CDMA Analyzer Relative Tuned Channel Power Level Accuracy

RF Freq (MHz)	Absolute Level (dBm)	Relative Level (dB)	Relative Channel Power Measurement Accuracy (dB)		
			Lower	Upper	Actual
840	-10	0	Reference		
840	-14	-4	-0.1	0.1	
840	-19	-9	-0.1	0.1	
840	-24	-14	-0.2	0.2	
840	-29	-19	-0.2	0.2	
840	-34	-24	-0.5	0.5	
840	-39	-29	-0.5	0.5	
840	- 44	- 34	-0.5	0.5	

9

HP 8924C/E Specifications

Specifications describe the instrument's warranted performance and are valid over the entire operating and environmental range unless otherwise noted.

Supplemental Characteristics are intended to provide additional information useful in applying the instrument by giving typical, but non-warranted performance parameters. These are shown in *italics* or labeled as "typical," "usable to," or "nominal."

Signal Generator Specifications (Analog Mode)

RF Frequency

Range

- 30 MHz to 1000 MHz.

Accuracy and Stability

- Same as reference oscillator ± 0.015 Hz.

Switching Speed

- *< 150 ms to be within 100 Hz of carrier frequency.*

Resolution

- *1 Hz.*

Output

RF In/Out Connector

- **Level Range:** –127 to –10.5 dBm into 50 ohms.
- **Level Accuracy:** ± 1.2 dB,if RF analyzer is also connected add ± 0.1dB,*typically ± 1.0 dB.*
- **Reverse Power:** 3watts continuous.10 watts for 10 seconds/minute.
- **SWR:** < 1.5:1.

Duplex Out Connector

- **Level Range:** –127 to +3.5 dBm into 50 ohms.
- **Level Accuracy:** ± 1.0 dB.
- **Reverse Power:** 200 mW maximum.
- **SWR:** < 2.0:1 (level < –7.5 dBm).

Resolution

- *0.1 dB.*

Spectral Purity

Spurious Signals (for ≤ -2.5 dBm output level at DUPLEX OUT or ≤ –16.5 dBm output level at RF IN/OUT).

- **Harmonics:** < –30 dBc.
- **Non-Harmonic Spurious:** < –60 dBc (at >5 kHz offset from carrier).

Residual FM (CCITT, rms)

- < 7 Hz for 500 MHz < fc ≤ 1000 MHz.
- < 4 Hz for 250 MHz ≤ fc ≤ 500 MHz.
- < 7 Hz for 30 MHz ≤ fc < 250 MHz.

SSB Phase Noise

- *< –116 dBc/Hz (for > 20 kHz offsets at a 1000 MHz carrier frequency).*

FM

FM Deviation (rates >25 Hz)

- 100 kHz; 30 to < 249 MHz.
- 50 kHz; 249 to < 501 MHz.
- 100 kHz; 501 to 1000 MHz. FM not specified for $\{f_c$ – FM deviation$\}$ < 250 kHz.

FM Rate (1 kHz reference)

- Internal:
  - dc to 25 kHz (1 dB BW).
- *External:*
  - *AC Coupled: 20 Hz to 75 kHz (typical –3 dB BW).*
  - *DC Coupled: dc to 75 kHz (typical –3 dB BW).*

FM Accuracy (1 kHz rate)

- ≤ 10 kHz deviation: ± 3.5% of setting ± 50 Hz.
- > 10 kHz deviation: ± 3.5% of setting ± 500 Hz.

FM Distortion (THD+Noise, 0.3 to 3 kHz BW)

- < 0.5% at > 4 kHz deviation and 1 kHz rate.

Center Frequency Accuracy in DCFM Mode

- External source impedance < 1 k ohms: ± 500 Hz (after DCFM zero), *typically ±50 Hz.*

External Modulation Input Impedance

- *600 ohms nominal.*

Resolution

- *50 Hz for < 10 kHz deviation.*
- *500 Hz for ≥ 10 kHz deviation.*

Audio Source Specifications (Analog Mode)

The following specifications apply to both internal sources.

Frequency

Range

- dc to 25 kHz.

Accuracy

- 0.025% of setting.

Resolution

- 0.1 Hz.

Output Level

Range

- 0.1 mV to 4 Vrms.

Maximum Output Current

- 20 mA peak.

Output Impedance

- < 2.5 ohm (at 1 kHz).

Accuracy

- ± 2% of setting plus resolution.

Residual Distortion (THD + Noise, level ≥ 200 mV rms)

- < 0.125%; 20 Hz to 25 kHz in an 80 kHz BW.

Resolution

- *Level ≤ 0.01V: ± 50 µV.*
- *Level ≤ 0.1V: ± 0.5 mV.*
- *Level ≤ 1V: ± 5 mV.*
- *Level < 10V: ± 50 mV.*

Offset in dc-coupled Mode

- *< 50 mV.*

RF Analyzer Specifications (Analog Mode)

RF Frequency Measurement

Measurement Range

- 30 MHz to 1000 MHz.

Level Range

- RF IN/OUT
  - 0.1 mW to 3W continuous.
  - 10 W for 10 seconds per minute.
- ANT IN
  - –36 dBm to +20 dBm.

Accuracy

- ± 1 Hz + timebase accuracy.

Minimum Resolution

- *1 Hz*.

RF Power Measurement

Note: To achieve the specified accuracy when measuring power at the RF IN/OUT port, the internal signal generator's level must be 40 dB below the measured power or less than
–20 dBm at the DUPLEX OUT port.

Frequency Range

- 30 MHz to 1000 MHz.

Input Connector

- RF In/Out connector only.

Measurement Range

- 0.1 mW to 3 W continuous.
- 10 W for 10 seconds per minute.

Accuracy

- ± 5% of reading ±1 µW ± 1 count from 15° C to 35° C.
- ± 10% of reading ±1 µW ± 1 count from 0° C to 55° C.

SWR

- < 1.5:1.

Resolution

- *Power < 10 W: 1 mW.*
- *Power < 100 mW: 0.1 mW.*
- *Power < 10 mW: 0.01 mW.*

FM Measurement

Frequency Range

- 30 to 1000 MHz

Deviation Range

- 20 Hz to 75 kHz.

Sensitivity (15 kHz IF BW, High Sensitivity Mode, 0.3 to 3 kHz BW)

- 2 µV. *Typically < 1 µV (12 dB SINAD, fc ≥ 10 MHz).*

Accuracy (20 Hz to 25 kHz rates, deviation ≤ 25 kHz)

- ± 4% of reading plus residual FM and noise contribution.

Bandwidth (3 dB)

- 2 Hz to 70 kHz (DCFM measurements also available).

THD+Noise

- < 1% for ≥ 5 kHz deviation and 1 kHz rate in a 0.3 to 3 kHz BW.

Input Level Range for Specified Accuracy

- –28 to +35 dBm at RF IN/OUT (1.6 µW to 3W).
- –50 to +14 dBm at ANT IN.

Residual FM and Noise (0.3 to 3 kHz, rms)

- < 7 Hz.

Resolution

- *Deviation < 10 kHz: 1 Hz.*
- *Deviation. ≥ 10 kHz: 10 Hz.*

Spectrum Analyzer Specifications (HP 8924E: Option 102 required)

General

Frequency Range

- 30 MHz to 1000 MHz. Center frequency coupled to RF Analyzer setting.

Frequency Span, Resolution Bandwidth (coupled)

Table 86

Span	Bandwidth
< 50 kHz	300 Hz
< 200 kHz	1 kHz
< 1.5 MHz	3 kHz
< 18 MHz	30 kHz
≥ 18 MHz	300 kHz

Plus full span capability

Display

- Log with 10 dB/div, 2 dB/div, or 1 dB/div.

Display Range

- 80 dB.

Reference Level Range

- + 50 to –50 dBm.

Residual Responses

- < –70 dBm (antenna input, no input signal, 0 dB attenuation).

Image Rejection

- > 50 dB.

Non-harmonic Spurious Responses

- *> 70 dB (for input signals ≤ –30 dBm).*

Level Accuracy

- *± 2.5 dB.*

Log Scale Linearity

- *± 2 dB (for input levels ≤ –30 dBm and/or 60 dB range).*

Displayed Average Noise Level

- *< –114 dBm (≤ 50 kHz spans).*

Other Features

- *Peak hold.*
- *Marker with frequency and level readout.*
- *Marker to peak.*
- *Marker to next peak.*
- *Trace comparison A-B.*

Tracking Generator

Frequency Range

- 30 MHz to 1000 MHz.

Frequency Offset

- Frequency span endpoints ± frequency offset cannot be < 30 MHz or > 1000 MHz.

Output Level Range

- Same as signal generator.

Sweep Modes

- Normal and Inverted.

Adjacent Channel Power Specifications (HP 8924C ONLY)

Relative Measurements

Level Range

- RF IN/OUT
  - –10 dBm to +35 dBm continuous (3 W).
  - Up to +40 dBm (10 W) for 10 seconds/minute.
- ANT IN
  - –40 dBm to +20 dBm.

Dynamic Range (typical values for channel offsets)

Table 87

Offset	Resolution Bandwidth	Dynamic Range
12.5 kHz	8.5 kHz	–65 dBc
20 kHz	14 kHz	–68 dBc
25 kHz	16 kHz	–68 dBc
30 kHz	16 kHz	–68 dBc
60 kHz	30 kHz	–65 dBc

Relative Accuracy

- ±2.0 dB

Absolute Measurements (HP 8924C ONLY)

Level

- Results of absolute power in Watts or dBm are determined by adding the ACP ratio from the spectrum analyzer to the carrier power measurement obtained from the input section RF power detector.

Level Range

- RF IN/OUT
  - 0.1 mW to 3 W continuous.
  - Up to 10 W for 10 seconds/minute.
- ANT IN
  - Not available.

Dynamic Range (typical values for channel offsets)

Table 88

Offset	Resolution Bandwidth	Dynamic Range
12.5 kHz	8.5 kHz	–65 dBc
20 kHz	14 kHz	–68 dBc
25 kHz	16 kHz	–68 dBc
30 kHz	16 kHz	–68 dBc
60 kHz	30 kHz	–65 dBc

Absolute Accuracy

- Absolute accuracy is the sum of the RF Analyzer's RF Power Measurement **"Accuracy" on page 412** and the ACP Relative Accuracy of ±2.0 dB.

AF Analyzer Specifications

Frequency Measurement

Measurement Range

- 20 Hz to 400 kHz.

Accuracy

- ± 0.02% plus resolution plus reference oscillator accuracy.

External Input

- 20 mV to 30 Vrms.

Resolution

- *f < 10 kHz: 0.01 Hz.*
- *f < 100 kHz: 0.1 Hz.*
- *f ≥ 100 kHz: 1 Hz.*

AC Voltage Measurement

Measurement Range

- 0 to 30 Vrms.

Accuracy (20 Hz to 15 kHz, inputs ≥ 1 mV)

- ± 3% of reading.

Residual THD+Noise (15 kHz BW)

- 150 µV.

3 dB Bandwidth

- *Typically 2 Hz to 100 kHz.*

Nominal Input Impedance

- *Switchable between 1 M ohm in parallel with 95 pF or 600 ohms floating.*

Resolution

- *4 digits for inputs ≥ 100 mV.*
- *3 digits for inputs < 100 mV.*

DC Voltage Measurement

Voltage Range

- 100 mV to 42 V.

Accuracy

- ± 1.0% of reading plus DC Offset.

DC Offset

- ± 45 mV.

Resolution

- *1 mV.*

Distortion Measurement

Fundamental Frequency Range

- 300 Hz to 10 kHz ±5%.

Input Level Range

- 30 mV to 30 Vrms.

Display Range

- 0.1% to 100%.

Accuracy

- ± 1 dB for frequencies from 300 to 1500 Hz, measured with the 15 kHz LPF (0.5 to 100% distortion).
- ± 1.5 dB for frequencies from 300 Hz to 10 kHz, measured with the >99 kHz LPF (1.5 to 100% distortion).

Residual THD+Noise

- –60 dBc or 150 µV, whichever is greater for frequencies from 300 Hz to 1500 Hz measured with the 15 kHz LPF.
- –57 dBc or 450 µV, whichever is greater for frequencies from 300 Hz to 10 kHz measured with the > 99 kHz LPF.

Resolution

- *0.1% distortion*.

SINAD Measurement

Fundamental Frequency Range

- 300 Hz to 10 kHz ±5%.

Input Level Range

- 30 mV to 30 Vrms.

Display Range

- 0 to 60 dB.

Accuracy

- ± 1 dB for frequencies from 300 to 1500 Hz, measured with the 15 kHz LPF (0 to 46 dB SINAD).
- ± 1.5 dB for frequencies from 300 Hz to 10 kHz, measured with the >99 kHz LPF (0 to 36 dB SINAD).

Residual THD+Noise

- –60 dB or 150 µV, whichever is greater for frequencies from 300 Hz to 1500 Hz measured with the 15 kHz LPF.
- –57 dBc or 450 µV, whichever is greater for frequencies from 300 Hz to 10 kHz measured with the > 99 kHz LPF.

Resolution

- *0.01 dB.*

Audio Filters

High-Pass Filters

- < 20 Hz.
- 50 Hz.
- 300 Hz.

Low-Pass Filters

- 300 Hz.
- 3 kHz.
- 15 kHz.
- > 99 kHz.

Other Filters

- C-Message Weighting Filter.
- 6 kHz Bandpass Filter.

Optional Filters

- CCITT Weighting Filter (for TACS phones).
  Option 011 replaces the C-Message filter with the CCITT filter.

Variable Frequency Notch Filter

Frequency Tuning Range

- 300 Hz to 10 kHz.

Notch Depth

- > 60 dB.

Notch Width

- *Typically ±5% of the notch center frequency*.

Audio Detectors

- RMS.
- Pk+.
- Pk–.
- Pk+hold.
- Pk–hold.
- Pk±/2.
- Pk±/2 hold.
- Pk±max.
- Pk±max hold.

Oscilloscope Specifications (Analog Mode)

General

Frequency Range (–3 dB Bandwidth)

- 2 Hz to 50 kHz.

Scale/Division

- 10 mV to 10 V.

Amplitude Accuracy (20 Hz to 10 kHz)

- ± 1.5% of reading ± 0.1 division.

Time/Division

- 10 µs to 100 ms.

Trigger Delay

- 20 µs to 3.2 seconds.

3 dB Bandwidth

- *Typically > 100 kHz.*

Internal DC Offset

- *≤ 0.1 div (≥ 50 µV/division sensitivity).*

Signaling Specifications (Analog Mode)

General

Capability for generating and analyzing the following formats

- AMPS, EAMPS, NAMPS.
- TACS, JTACS, NTACS, ETACS.
- NMT-450S, NMT-900S.
- LTR.
- EDACS.
- MPT 1327.

Function Generator Waveforms

- Sine.
- Square.
- Triangle.
- Ramp.
- dc.
- White Gaussian noise.
- White uniform noise.

Function Generator Frequency Range and Level

- Same as audio source.

DC Current Meter Specifications (Analog Mode)

General

Measurement Range

- 0 to 10 A *(usable to 20 A).*

Accuracy

- The greater of ± 10% of reading after zeroing or 30 mA (levels > 100 mA).

CDMA Call Processing Functions

General

Base Station User Settable Parameters

- NID.
- SID.
- BASE_ID.
- SRCH_WIN_A.
- SRCH_WIN_N.
- SRCH_WIN_R.
- Pilot Inc.
- Register NID.
- Register SID.

Access Probe User Settable Parameters

- NOM_PWR.
- INIT_PWR.
- PWR_STEP.
- PAM_SZ.
- NUM_STEP.
- MAX_REQ_SEQ.
- MAX_RSP_SEQ.

Paging Channel User Settable Parameters

- Paging Data Rate (full or half rate).
- SLOT_CYCLE_INDEX.

Base Station Threshold User Settable Parameters

- T_ADD.
- T_DROP.
- T_COMP.
- T_TDROP.

Service Option Modes

- Service Option 001 (normal voice).
- Service Option 002.

Call Control

- BS call originate.
- BS call disconnect.
- MS call originate.
- MS call disconnect.

Handoff Support

- Hard (RF Frequency).
- Softer.
- CDMA to Analog.

Call Status Indicators

- Transmitting (cell active).
- Registering.
- Page Sent.
- Access Probe Received.
- Connected.
- Softer Handoff.
- Hard Handoff.
- Svc Opt 2.

Speech Encoding

- None.

Speech Echo Mode (user selectable fixed delays)

- 0 seconds.
- 2 seconds.
- 5 seconds.

CDMA Data Source

- Pseudo-random data (CCITT 2^{15}–1 pattern).
- Voice Echo.
- 1 kHz Tone.
- 400 Hz Tone.
- Audio Chirp (3 second sweep from 5 Hz to 3.75 kHz).

Closed Loop Power Control (supports the following)

- True Closed Loop Power Control Mode.
- Open Loop Mode (alternating 0's and 1's power control bit pattern).
- Always Up Mode.
- Always Down Mode.

Closed Loop Change Bits

- n Up.
- n Down.
- Ramp of 100 up followed by 100 down power control bits.

Open Loop Power Control

- Supported through varying the level of CDMA Generator. CDMA analyzer autoranges to the ideal RF power level for the nominally expected open-loop response.

Mobile Station FER Reporting

- User selectable number of frames (from predefined list). Report by number of frames or by user defined number of errors.

Adjacent Cell Mobile Reporting

- Displays status, PN offset, strength, and keep bit for all pilots found by the CDMA mobile, and reported via pilot strength messages.

Neighbor List Support

- Automatically generates a list of 8 neighbors based on user entry of Sector A PN offset, Sector B PN offset and Pilot Inc.

Mobile Station Identification

- 10-digit phone number).
- MIN (hex entry only).
- Auto (requests an automatic zone based registration)

Registration

- Zone based registration through HP-IB command or front panel keys.
- Mobile power-on registration.

Retrievable Mobile Parameters (Supports IS-95A message format only. Does not work properly with IS-95 phones.)

- MUX_REV_(1 to 14).
- MUX1_FOR_(1 to 14).
- PAG_(1 to 7).
- ACC_(1 to 8).
- LAYER2_RTC_(1 to 5).
- OTHER_SYS_TIME.

Mobile Database (upon registration)

- ESN.
- MIN1.
- MIN2.
- Phone number.
- Dual-mode status.
- Slot class.
- Slot index.
- Power class.
- Transmit mode.
- Called number.

CDMA Generator Specifications

CDMA Channels

Additive White Gaussian Noise (I_{oc})

Sector A with Selectable PN Offset

- Pilot Channel at Walsh Code 0.
- Sync Channel at Walsh Code 32.
- Paging Channel at Walsh Code 1.
- Traffic Channel with selectable Walsh Code.
- OCNS Channel with selectable Walsh Code.

Sector B with Selectable PN Offset (HP 8924C Only)

- Pilot Channel at Walsh Code 0.
- Traffic Channel with selectable Walsh Code.
- OCNS Channel with selectable Walsh Code.

Frequency

Frequency Range

- 501 MHz to 1000 MHz. *Also usable from 30 to 248.9 MHz with reduced accuracy.*

Frequency Resolution

- 1 Hz.

Frequency Accuracy

- Same as reference oscillator accuracy ± 0.015 Hz

AWGN Bandwidth

- *Nominal BW of 1.8 MHz.*

Amplitude

Composite Signal Output Level Range

- **RF In/Out:** –109 dBm/1.23 MHz to –21.5 dBm/1.23 MHz.
  Usable to –127 dBm/1.23 MHz with reduced level accuracy.
- **Duplex Out**: –109 dBm/1.23 MHz to –7.5 dBm/1.23 MHz.
  Usable to –127 dBm/1.23 MHz with reduced level accuracy.

Composite Signal Output Level Accuracy (using the IS-98 sensitivity setup)

- **RF In/Out:**
  AWGN Off: ±1.5 dB.
  AWGN On: ±2.0 dB.
- **Duplex Out:** .
  AWGN Off: ±1.5 dB.
  AWGN On: ±2.0 dB.

Composite Signal Output Power

- Equal to the sum of the individually settable power levels for AWGN, Sector A, and Sector B.

Maximum Individual Signal Dynamic Range

- The maximum dynamic range of any CDMA channel (AWGN, Sector A: Pilot, Sync, Paging, Traffic, or OCNS, Sector B: Pilot, Traffic, or OCNS) is from 0 dB to –30 dB relative to the total composite output power. The dynamic range of the Paging and Traffic channels will vary depending on the data rate in use.

AWGN Bandwidth

- *Typically > 1.8 MHz bandwidth. Because the reported total composite power and AWGN power is in terms of dBm in a 1.23 MHz bandwidth, the actual broadband output power as seen by a power meter on the front panel will be higher than reported on the front panel.*

Sector A OCNS Channel Relative Level Range

- Automatically calculated from other Sector A channel relative levels to provide the set Sector A total power.

Sector B OCNS Channel Relative Level Range (HP 8924C Only)

- Automatically calculated from other Sector B channel relative levels to provide the set Sector B total power.

Individual Channel Amplitude Resolution

- 0.01 dB.

Relative CDMA Channel Level Accuracy

- AWGN to Traffic Channel: < 0.2 dB ±5° C from last temperature at which PCB_CAL was run for values of E_b/N_t from 1 dB to 10 dB.
- Between any two CDMA Channels: < 0.2 dB ±5° C from last calibration temperature at which PCB_CAL was run.

CDMA Modulation

Modulation Type

- QPSK per TIA IS-95.

Residual ρ (rho)

- Better than 0.97, *typically > 0.98.*

Carrier Feedthrough

- Better than –30 dBc, *typically better then –34 dBc from +10° C to +40° C.*

Adjacent Channel Spectral Purity

- *< –45 dBc in a 30 kHz bandwidth at ±895 kHz offset from carrier frequency relative to the total carrier power in a 1.23 MHz bandwidth.*

Data Rate Transmission Modes

- IS-95 defined Base Station modes including full rate, half rate, quarter rate, one-eighth rate data transmission, and variable rate with equally weighted, randomly spaced occurrences of each rate.

Data Generator Patterns

- Pseudo-random data (CCITT 2^{15}–1 pattern).

CDMA Analyzer Specifications

CDMA Average Power Measurement

To achieve the specified accuracy when measuring power at the RF IN/OUT port, the internal signal generator's level must be 40 dB below the measured power or less than
–20 dBm at the DUPLEX output port.

Input Frequency Range

- 30 MHz to 1000 MHz.

Input Connector

- RF IN/OUT Connector Only.

Measurement Bandwidth

- Provides an accurate measure of the total power for all present signals within ±2 MHz of the specified operating frequency. If other signals are present outside of this frequency range, reduced measurement accuracy will result.

Maximum Input Level

- +35 dBm (3 Watts continuous, 10 Watts allowable for 10 seconds per minute).

Measurement Range

- –10 dBm to +35 dBm.

Measurement Method

- Reports the overall average power for all active power control groups captured.

Measurement Period

- Measures over one-half of a CDMA frame (8 power control groups) in full, half, quarter, or one-eighth rate modes.

Measurement Update Rate

- *Typically 1.5 readings-per-second.*

Measurement Accuracy

- ±5% ±1 µW at 25° C ±10° C.
- ±10% ±1 µW from 0° C to +55° C.

CDMA Tuned Channel Power Measurement

Input Frequency Range

- 30 MHz to 1000 MHz.

Input Connector

- RF IN/OUT *(usable on antenna input (ANT IN) with relative power measurement capability only)*.

Measurement Bandwidth

- Measures the total power in a 1.23 MHz bandwidth centered on the active reverse channel center frequency.

Maximum Input Level

- +35 dBm (3 Watts continuous, 10 Watts allowable for 10 seconds per minute).

Measurement Range

- –50 dBm to +10 dBm *(usable to +35 dBm with degraded accuracy).*

Measurement Update Rate

- *Typically 2 readings-per-second.*

Measurement Accuracy

- Relative Mode (uncalibrated against average power)
  - 0 to –10 dB relative level: ±0.1 dB.
  - –10 to –20 dB relative level: ±0.2 dB.
  - –20 to –40 dB relative level: ±0.5 dB.
- Calibrated Mode (calibrated against average power)
  - ±1.0 dB at ±5° C from the calibration temperature.

Measurement Method

- Reports the average channel power for all active power control groups captured.

Measurement Period

- Measures power in a 1.23 MHz bandwidth over one-half of a CDMA frame (8 power control groups) in full, half, quarter or one-eighth rate modes.

CDMA Modulation Measurement

Input Frequency Range

- 30 MHz to 1000 MHz.

Modulation Measurement Format

- OQPSK per TIA IS-95.

ρ (rho) Measurement Input Level Range

- –20 dBm to +35 dBm *(usable to –30 dBm with degraded accuracy)*.

Range of ρ (rho) Measurement for Specified Accuracy

- 0.45 to 1.00.

ρ (rho) Measurement Interval

- Traffic Channel ρ: 1.042 ms (5 walsh symbols).
- Test Mode ρ: 1.25 ms (6 walsh symbols).

Measurement Update Rate

- *Typically 1.5 readings-per-second*.

ρ (rho) Measurement Accuracy

- ρ ±0.003.

Frequency Error Measurement Range

- ± 1 kHz.

Frequency Error Measurement Accuracy

- ± 30 Hz.

Other Reported Parameter with ρ Measurement

- Static Timing Accuracy.
- Carrier Feedthrough.
- Amplitude Error.
- Phase Error.

CDMA Frame Error Rate Measurement

FER Measurement Method

- Data loopback per Service Option 2 supporting confidence limits as outlined in TIA IS-98.

Supported Data Rates for FER Measurement

- Full.
- Half.
- Quarter.
- Eighth.

Confidence Limit Range

- User definable from 80.0% to 99.9% and Off.

Confidence Limit Statistical Model

- Meets IS-98 statistical model parameters.

FER Reported Parameters

- Measured FER.
- Number of Errors.
- Number of Frames tested.
- One of the following
  - Passed Confidence limit.
  - Failed Confidence limit.
  - Max Frames (test indeterminate).

Conditions for Terminating FER Test (with confidence limits on)

- **Max Frames:** Maximum number of frames to test completed, indicative of an indeterminate test result.
- **Failed:** Measured FER failed the specified FER limit with specified confidence.
- **Passed:** Measured FER passed the specified FER limit with specified confidence.

CDMA Reverse Channel Spectrum Display (HP 8924E: Option 102 required)

Frequency Range

- Fixed to the active CDMA reverse channel setting. Not independently adjustable.

Frequency Span/Resolution Bandwidth (coupled, maximum span of 5 MHz)

Table 89

Span	Bandwidth
< 50 kHz	300 Hz
< 200 kHz	1 kHz
< 1.5 MHz	3 kHz
5 MHz	30 kHz

Display

- Log with 10 dB/div.

Display Range

- 80 dB.

Reference Level Range

- +50 to –50 dBm.

CDMA Triggers

Output Trigger Signals

- Power control bit send (some error is in this signal's timing).
- CDMA Flag.
- Protocol Flag.

Trigger Inputs

- DSP Trigger.

General Specifications

Remote Programming Specifications

HP-IB

- Hewlett-Packard's implementation of IEEE Standard 488.2.

Remote Front-Panel Lockout

- Allows remote user to disable the front panel display to improve HP-IB measurement speed.

Functions Implemented

- SH1.
- AH1.
- T6.
- L4.
- SR1.
- RL1.
- LE0.
- TE0.
- PP0.
- DC1.
- DT1.
- C4.
- C11.
- E2.

RS-232

- 3-wire RJ-11 connector used for serial data in and out (no hardware handshake capability, 2 available).

Baud Rates (selectable)

- 300.
- 600.
- 1200.
- 2400.
- 4800.
- 9600.
- 19200.

Centronics Port

- Industry standard parallel printer port for hard copies of test results or screen dumps.

Timebase Subsystem Specifications

For proper operation, this reference must be locked to either the Test Sets's high stability 10 MHz timebase output on the rear panel or to an external, high quality reference.

Locking Range

- ±10 ppm.

Input

- Rear-panel coaxial BNC.

Accepted Input Frequencies

- 19.6608 MHz.
- 15 MHz.
- 10 MHz.
- 9.8304 MHz.
- 5 MHz.
- 4.9152 MHz.
- 2.4576 MHz.
- 2 MHz.
- 1.2288 MHz.
- 1 MHz.

Outputs (all on rear panel)

- Coaxial BNCs
  - 19.6608 MHz.
  - 10 MHz.
  - 1.2288 MHz.
  - Frame Clock BNC Output (CDMA Mode Only)
    - User selectable output of one of the following clocks through this BNC
      - 1.25 ms.
      - 20 ms frame clock.
      - 26.67 ms short sequence clock.
      - 80 ms clock.
      - Every even second (PP2S).
- TTL Sub Min D Connector
  - Individual pins for the following
    - 1.25 ms.
    - 20 ms frame clock.
    - 26.67 ms short sequence clock.
    - 80 ms clock.
    - Every even second (PP2S).

Ovenized Reference Specifications

Aging Rate

- < 0.005 ppm peak-to-peak/day, < ±0.1 ppm per year (±85 Hz at 850 MHz in one year).

Warm-up

- ±0.1 ppm in 5 minutes, ±0.01 ppm in 15 minutes.

Temperature

- < 0.01 ppm.

Supply Voltage

- *2 x 10-9 (±1%)*.

Rear-Panel BNC Connectors

- *Output Frequency: 10 MHz.*
- *Output Level: 0 dBm ±3 dB into 50 Ω.*

Store/Recall Specifications

Available RAM

- *Approximately 928 KB of user available RAM. When running the HP 83217A Dual Mode CDMA Mobile Station Test Software, approximately 280 KB of RAM is available for store/recall use.*

Memory Card Specifications

Card Compatibility

- Single industry standard PCMCIA slot that accepts type I and type II SRAM and ROM cards.

Storage Capability

- Allows for the storage and retrieval of IBASIC programs, IBASIC program parameter and results data, input of new calibration data, and long term storage of Store/Recall information.

Firmware Upgrades

- Accepts PCMCIA memory cards to allow automatic loading of new firmware for the Host CPU, Protocol CPU, DSP, and Channel Card CPUs without opening the Test Set.

Physical Specifications

Dimensions (H×W×D

- 177× 426×574 mm (7×16.75×23 in).

Weight

- 27 kg (59 lbs).

CRT Size

- 7 × 10 cm.

Operating Temperature

- 0° C to +55° C.

Storage Temperature

- –55° C to +75° C.

Power

- 100 V to 240 V, 50/60 Hz, *nominally 400 VA.*

Calibration Interval

- One year.

EMI

- Conducted and Radiated interference meets CISPR-11, IEC 801-2, 801-3, and 801-4.

Leakage

- *At RF Generator output levels <–40 dBm, typical radiated leakage is < 1 µV induced in a resonant dipole antenna 25 mm (1 inch) away from any surface except the rear panel. Spurious leakage levels are typically < 5 µV in a resonant dipole antenna 25 mm (1 inch) away from any surface except the rear panel. Spurious leakage levels at the rear panel are typically < 5 µV in a resonant dipole antenna at a distance of 254mm (10 inches).*

Connector Summary

Front-Panel Inputs

- RF Input/Output: Type N
- Antenna Input: BNC
- Microphone/Accessory: 8-pin DIN
- Audio Input: Dual BNCs

Front-Panel Outputs

- RF Input/Output: Type N
- Duplex Output: BNC
- Audio Output: BNC

Rear-Panel Outputs

- CRT Video Output: BNC
- Audio Monitor Output: BNC
- 10 MHz Oven Output: BNC
- 10 MHz Reference Output: BNC
- CDMA Clocks & Triggers: 37-pin sub-min D
- CDMA Clock MUX Output: BNC **(HP 8924C Only)**
- 19.6608 MHz Clock Output: BNC **(HP 8924C Only)**
- 1.2288 MHz Clock Output: BNC **(HP 8924C Only)**
- 3.6869 MHz IF Output: BNC **(HP 8924C Only)**
- Spectrum Analyzer Trigger Out **(HP 8924E Only)**

Rear Panel Inputs

- Reference Input: BNC
- Modulation Input: BNC
- Translator Power Detector Input: SMC
- Current Sense Input: Dual Banana Jacks
- Auxiliary DSP Baseband Input: BNC **(HP 8924C Only)**
- External Scope Trigger Input: BNC **(HP 8924C Only)**
- Even Second Input: BNC **(HP 8924C Only)**
- DSP Trigger Input: BNC **(HP 8924C Only)**

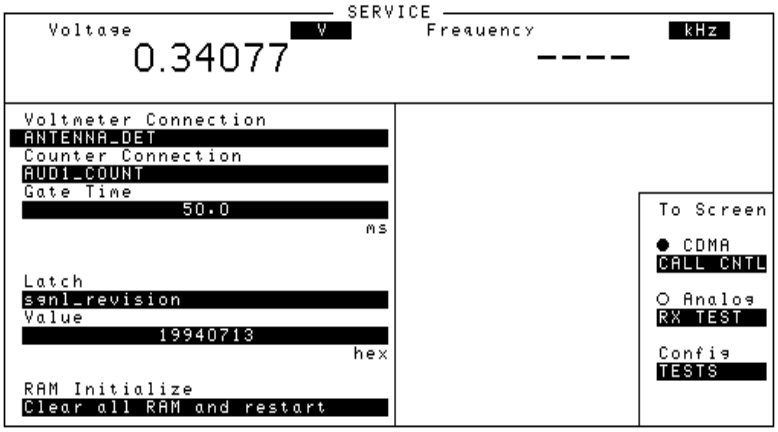
Rear-Panel Digital Ports

- HP-IB Port: 24-pin GP-IB
- Parallel Printer Port: 25-pin Centronics
- Host RS-232 Port: RJ-11
- Protocol Diagnostic RS-232 Port: 9-pin sub-min D
- Protocol Logging RS-232 Port: 9-pin sub-min D **(HP 8924C Only)**
- Translator Interface Port: 15-pin sub-min D **(HP 8924C Only)**

10

Service Screen

Troubleshooting with the Service Screen



The Service screen uses the internal voltmeter and frequency counter functions to monitor specific nodes in most assemblies. A large number of latch and DAC settings used throughout the Test Set can also be read and/or set to alter standard operation. These functions are primarily intended to allow the automated internal diagnostic routines to verify proper instrument operation, and to allow the periodic adjustment routines (PER_CAL3, CDMA_CAL, and PCB_CAL) to modify Test Set operation.

Access to these functions under manual control is provided to allow further troubleshooting when the diagnostics cannot isolate a failure to a specific assembly. To do this, you must understand how to operate the Test Set and, especially, understand how the assemblies in the Test Set work together.

Detailed manual Test Set operation is provided in the *User's Guide*. Refer to the Block Diagram chapter in this manual for information on how the overall instrument, and each module, works.

How to Access the Service Screen

1. Press PRESET to preset the Test Set.
2. Press the SHIFT key, then press the TESTS key to access the CONFIGURE screen.
3. Select the SERVICE field in bottom-right corner of the screen ("To Screen" menu).

Field Names and Descriptions

Voltmeter Connection

This field selects the desired circuit node for voltage measurements. To change the voltmeter connection, move the cursor in front of the **Voltmeter Connection** field and push the cursor control knob. A **Choices** menu will appear. Move the cursor to the desired circuit node in the list and push the cursor control knob. The reading is displayed in the **Voltage** measurement field at the top left of the display.

Because the diagnostic MUX points being measured must be in the range of 0 to ±5 volts, the measurement of some points are scaled to that measurement range. For example; the +12 Volt reference (**MEAS_12V_REF** should measure about +5volts. The -12 Volt reference (**MEAS_NEG_12V_REF** should measure about -5 volts. Many of the voltage measurements are only valid after a number of instrument settings are changed.

When run, the diagnostic routines make the necessary circuit changes and measurements automatically, comparing the measurements to known limits for each node.

Counter Connection

This field selects the desired circuit node to connect to the Test Set's internal frequency counter. The reading is displayed in the **Frequency** measurement field at the top right of the display.

To change the counter connection, move the cursor in front of the **Counter Connection** field and push the cursor control knob. A **Choices** menu will appear, then move the cursor to the desired circuit node and push the cursor control knob.

Gate Time

This field is used to adjust the Test Set's internal frequency counter's gate time. A shorter gate time may enable you to see frequency fluctuations that might not be seen using a longer gate time.

To change the gate time, move the cursor in front of the Gate Time field and push the cursor control knob. Rotate the cursor control knob until the desired gate time (10 to 1000µ in 10µ increments) is displayed, then press the cursor control knob.

Latch

This field is used to manually alter the circuit latches that control switch, DAC, and gain settings within the Test Set. The value of the selected latch is displayed and changed in the **`Value`** field. Some settings are read-only.

To set a switch, DAC, or gain setting:

1. Move the cursor in front of the **`Latch`** field and push the cursor control knob. A **`Choices`** menu will appear.
2. Move the cursor to the desired latch name and push the cursor control knob.
3. Move the cursor in front of the **`Value`** field and push the cursor control knob.
4. Rotate the cursor control knob to modify the value (hexadecimal).

NOTE: If any of the switches, DACs, or gain settings are changed with the **`Latch`** field, the Test Set will generate the message **`"Direct latch write occurred. Cycle power when done servicing."`** To clear this message, cycle the Test Set's power. Upon power-up, the internal controller will return the Test Set to its default settings and values.

The first part of the names in the **`Choices`** menu relates to the assembly where the switch, DAC, or gain setting is located. Some latch names are not listed here.

- dstr: A34 Modulation Distribution
- aud1: A35 Audio Analyzer 1
- aud2: A36 Audio Analyzer 2
- refs: A27 Reference
- inpt: A5 Input
- out: A26 Output
- rcvr: A30 Receiver
- gsyn: A24 Signal Generator Synthesizer
- rsyn: A28 Receiver Synthesizer
- spec: A32 Spectrum Analyzer
- meas: A37 Measurement
- metron: A37 Measurement
- afg1: A15 Signaling Source/Analyzer
- afg2: A15 Signaling Source/Analyzer
- sgnl: Displays version number of the Signaling Source/Analyzer firmware.
- cellSite1: A9 Cell Site 1 Digital board
- cellSite2: A7 Cell Site 2 Digital board
- cdmaRef: A29 CDMA Reference
- iq_mod: A25 I/Q Modulator
- loif: A31 LO/IF Demod
- main_dsp: A12 Main DSP Receiver
- aux_dsp: A11 Optional DSP Receiver
- protocol: A6 Protocol Processor

Value (hex)

This field displays and changes the value for the latch shown in the **`Latch`** field.

RAM Initialize

Selecting this field clears all SAVE registers and test programs, and any initialized RAM disk(s), that may be in RAM. It also resets all latches to their factory power-up configuration. If you have saved one or more instrument setups using the SAVE function, using this function will permanently remove them.

11

Block Diagrams

Introduction

This chapter includes detailed block diagrams and descriptions for each section of the Test Set. It also has I/O signal and pin number information that can be used to help isolate a problem to the assembly level if the diagnostics are unable to do so.

"Theory of Operation" on page 58 describes how the Test Set generates and analyzes audio and RF signals, and the generation of timing references. You should become familiar with that information before using the information in this section.

The chapter is organized into two areas:

- **Section details** - graphically describes how the primary RF and AF sections of the Test Set work together to generate and analyze signals.
- **Assembly details** - illustrates how each assembly works.

I/O Specifications and Switch Information

I/O and switch information is included for *some* assemblies to help you determine if voltages and signals are getting to the assemblies with the proper levels, shapes, and frequencies. Line names and connector pin numbers are given on the block diagrams.

Section Details

RF Input/Output Section

RF Frequency Measurement

The A5 Input assembly pre-scales the RF input frequency and sends it to the A37 Measurement assembly where it is counted. This measurement is used to automatically tune the local oscillator (LO) and to select the input RF filters. The IF is also counted by the A37 Measurement assembly via the A30 Receiver assembly. The A16 Host Controller calculates the RF frequency from the IF frequency measurement by taking into account the LO frequency. Accuracy is determined by the counter clock on the A27 Reference assembly (which is derived from the 10 MHz reference from the A29 CMDA Reference).

RF Power Measurement

The A5 Input assembly's power splitter has one port terminated by a 50 Ω load with a diode peak detector across it and a temperature sensor near it. The output of the diode detector is sent to the A37 Measurement assembly where it is measured. The A16 Host Controller converts the measured value to RF power and displays it.

A temperature sensor detects the presence of too much power at the RF IN/OUT connector. The output of the sensor is a DC voltage proportional to RF power. This voltage is measured by the A37 Measurement assembly, and the value is compared to a reference limit by the A16 Host Controller. The Controller displays an overpower message if the voltage goes above the limit. The temperature sensor is also used to temperature-compensate the RF power measurement.

Accuracy is ensured using factory-generated calibration data stored in EEPROM. Unlike the level-control calibration data for the RF Generator, the calibration data is mathematically applied to the measurement results by the A16 Host Controller. The following assemblies have calibration data which affects RF power measurement:

- A4 Attenuator
- A5 Input
- A37 Measurement

Input Gain Control

The A4 High Power Attenuator reduces the level through the RF IN/OUT port by 4 dB (but does not affect the level into the ANTENNA IN port). Step attenuators in the A5 Input section are switched in and out, manually or automatically. This keeps the input level within an optimum range for the mixers, IF amplifiers, and detectors.

Filters are automatically switched in to remove image and other interfering signals. The frequency ranges of the filters are as follows:

- 150 MHz low-pass
- 150 MHz - 386 MHz bandpass
- 350 MHz - 650 MHz tuneable bandpass
- 600 MHz - 1000 MHz tunable bandpass

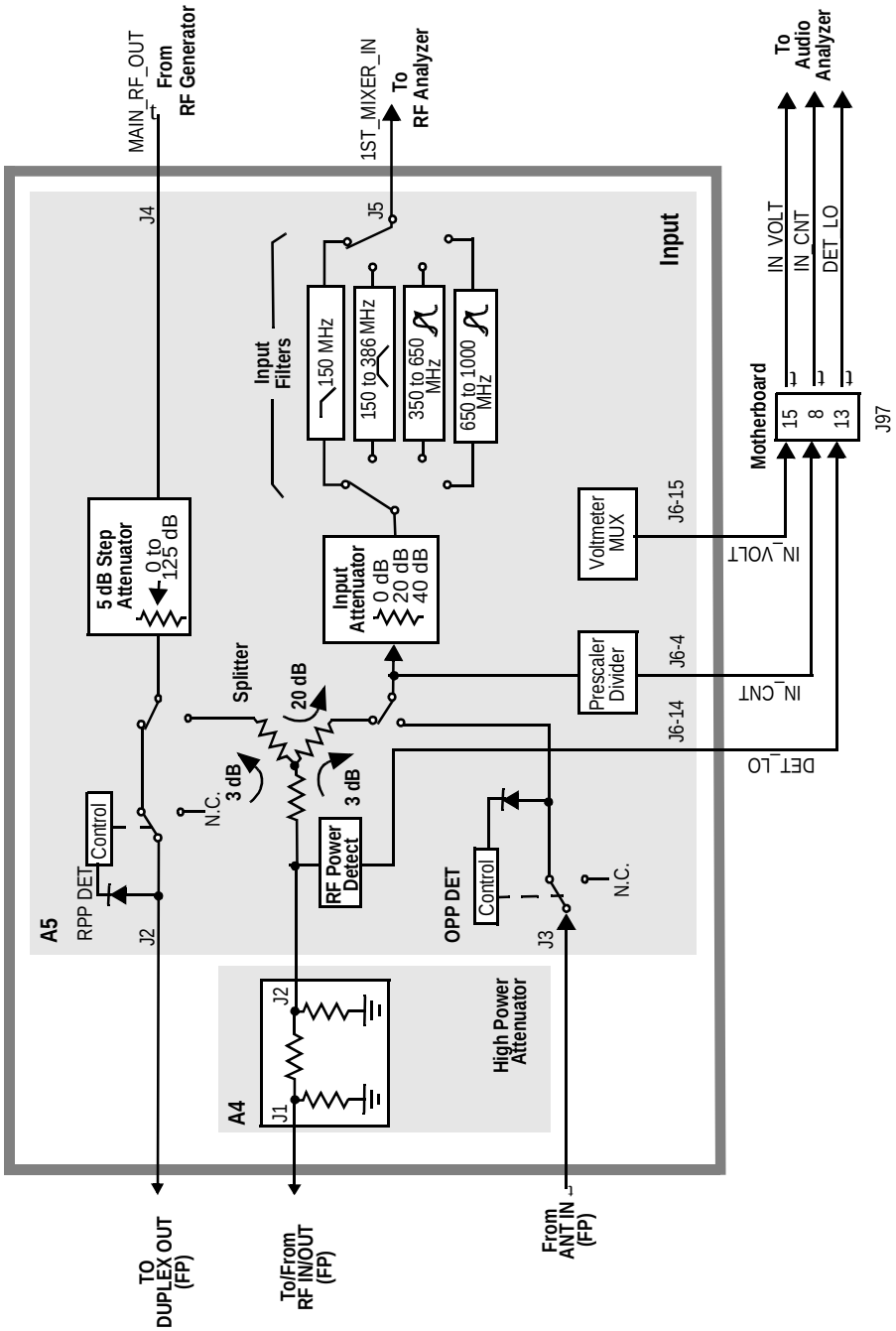


Figure 44 **RF Input/Output Overview**

Spectrum Analysis (Optional on 8924E)

The LO on the A32 Spectrum Analyzer assembly is swept across the span by the Controller. The LO starts sweeping when the oscilloscope circuits on the A37 Measurement assembly trigger the display sweep to start. As the LO sweeps, the spectrum analyzer filters and then amplifies the IF signal in a logarithmic detector so the signal voltage will be proportional to the log of power. The signal voltage is measured by a sampler on the A37 Measurement assembly and displayed.

Span Width and Bandwidth

Spectrum analyzer resolution bandwidth is determined by switchable bandwidth IF filters on the A32 Spectrum Analyzer assembly. These filters are set by the Controller as a function of the span selected from the front panel.

Markers

The Controller keeps track of the marker position set on the front panel and displays the frequency and level measured for that position. Frequency accuracy is the same as that of the A27 Reference assembly but it is limited by the resolution of the display.

Level accuracy can be affected by the logarithmic detector on the A32 Spectrum Analyzer assembly.

Tracking Generator

When the tracking generator function is selected, the Controller controls the spectrum analyzer and the RF generator together, causing them to track each other.

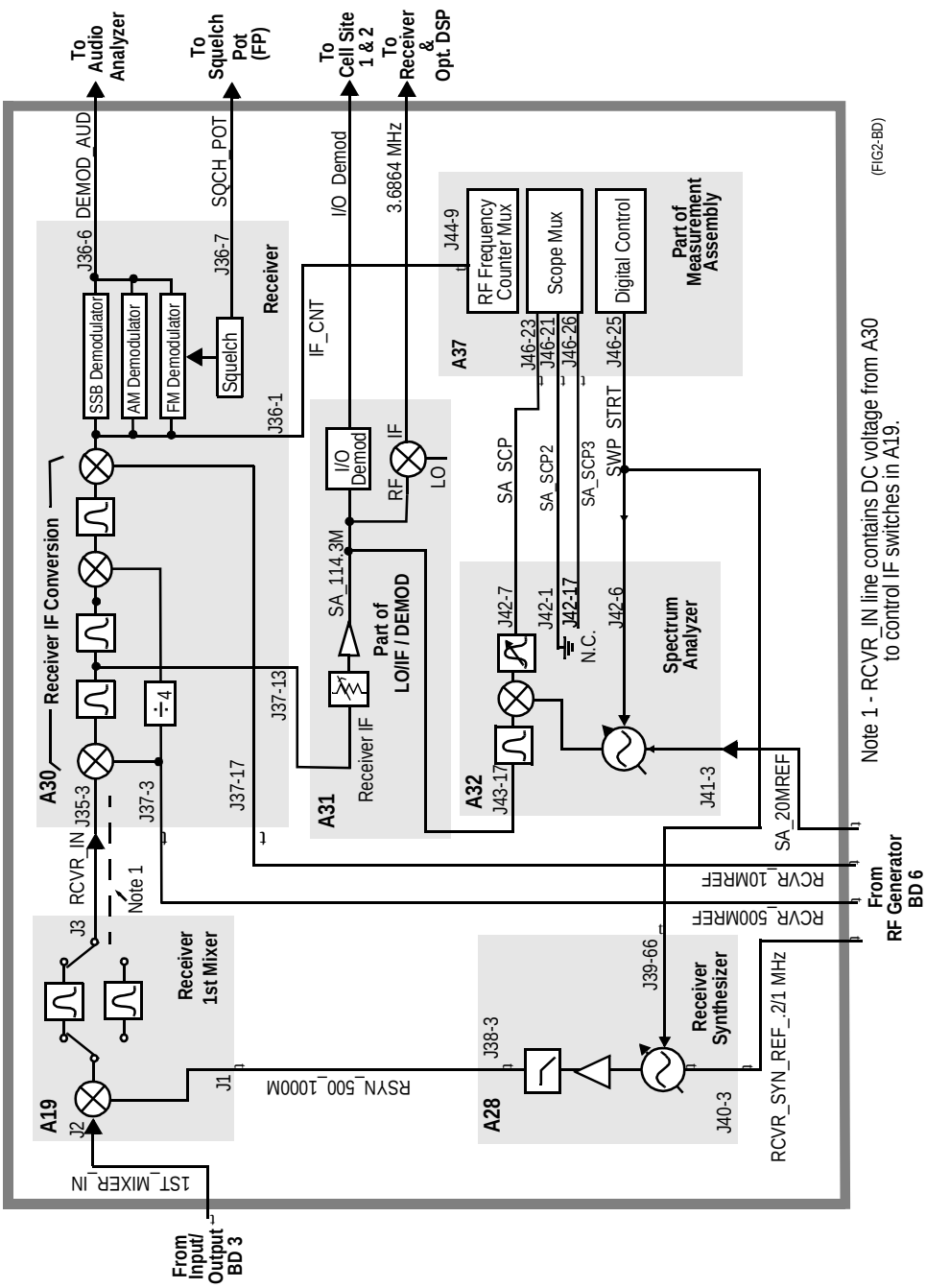


Figure 45 **RF Analysis Overview**

Audio Analyzer Section

Input Level Control

Switchable gain amplifiers on the A35 Audio Analyzer 1 and A36 Audio Analyzer 2 assemblies keep the audio input signal within a range suitable for the detectors.

AC and DC Level Measurements

Detected voltages from the Peak+, Peak –, and RMS detectors are measured on the A37 Measurement assembly. The A16 Host Controller calculates the displayed value; taking into account the detector selected from the front panel, the gain of the amplifiers, and the source of the input signal (demodulators, front panel).

Distortion and SINAD Measurements

Distortion and SINAD can be measured on 300 Hz to 10 kHz audio signals. The A16 Host Controller calculates Distortion and SINAD by comparing the ratio of the voltage after the variable notch filter to the ratio of the voltage before the notch filter.

Oscilloscope Functions

The Test Set has no specialized oscilloscope assemblies. The A35 and A36 Audio Analyzer assemblies, A37 Measurement assembly, and the A16 Host Controller work together to perform the oscilloscope functions.

Display

The audio or dc signal to be displayed goes from the A36 Audio Analyzer 2 assembly to a sampler on the A37 Measurement assembly (the same sampler used by the Spectrum Analyzer). The A16 Host Controller calculates the display level by taking into account the value of the measured signal at each point of the sweep, the gain of the signal path in the Audio Analyzer assemblies, and the volts-per-division setting.

Trigger

The scope trigger signals from the rear-panel MEAS TRIGGER connector, the A15 Signaling Source/Analyzer assembly, and the internal trigger signal are used by the A37 Measurement assembly and the A16 Host Controller to determine when to start the scope sweep. The Controller takes into account the pre-trigger time entered from the front panel.

Marker

The A16 Host Controller keeps track of the marker position set on the front panel and displays the time and level measured for that position.

Time accuracy is the same as the frequency counter's accuracy because the scope timing is derived from the A27 Reference assembly but it is limited by the resolution of the display.

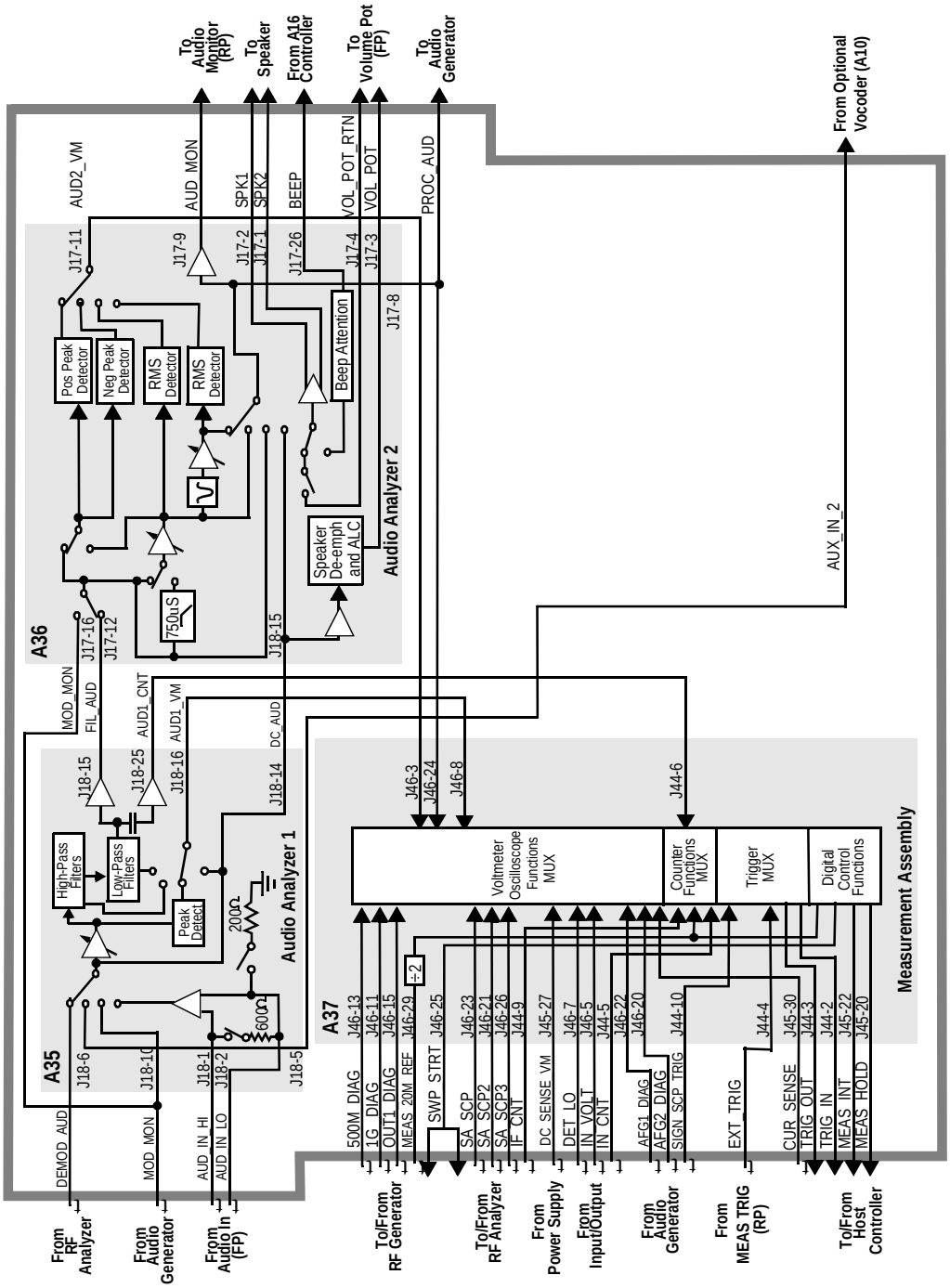


Figure 46 **Audio Analysis Overview**

RF Generator Section

Frequency Reference Generation

The A38 Oven Oscillator provides a 10 MHz reference that is connected by an external jumper to the rear panel REF INPUT connector. This signal goes to the A29 CDMA Reference to generate the CDMA clock signals and provide the 10 MHz reference for the A27 Reference. All generated frequencies are derived from the A27 Reference assembly. The A27 Reference assembly also has its own temperature compensated crystal oscillator (TCXO) that is switched in if the signal from the A29 CMDA Reference is not present (however, this condition would not permit CDMA operation). The A27 Reference assembly develops the local oscillator (LO) and reference signals needed by the assemblies that make up the RF Generator, RF Analyzer, Spectrum Analyzer, and the A37 Measurement assembly.

The A24 Signal Generator Synthesizer develops a 500 MHz to 1000 MHz signal which is phase-locked to the 200 kHz reference from the A27 Reference Assembly. When FM is needed, the modulating signal from the A34 Modulation Distribution assembly is summed into the tune voltage of the voltage controlled oscillator in the synthesizer. An out-of-lock indicator LED lights if the phase-lock-loop is out-of-lock. When you turn the Test Set's power on the LED lights for a few seconds then goes out. If it stays on or comes on again, the loop is out-of-lock.

The 500-1000 MHz signal then goes to the A25 I/Q Modulator assembly. The signal is I/Q modulated when creating a CDMA signal, or is routed past the I/Q modulators for non-CDMA signals. The signal is then sent to the A26 Output assembly.

The A26 Output assembly develops the RF Generator's full frequency range by mixing, dividing, or passing the 500 MHz to 1000 MHz from the A24 assembly. The frequencies are derived as follows:

Output Frequency	Derivation
250 kHz - 250 MHz	mix
250 MHz - 500 MHz	divide
500 MHz - 1 GHz	pass

Level Control

The A26 Output assembly has an automatic-level-control (ALC) loop that acts as a vernier control of RF level between –2 and +9 dBm. A step attenuator in the A5 Input assembly takes the level down to –127 dBm (–137 dBm at the RF IN/OUT connector) in 5 dB steps.

Assemblies that affect output level calibration have factory-generated calibration data stored in the Test Set's EEPROM. Calibration data is fed to digital-to-analog-converters that control level-adjustable devices in the RF path. These assemblies are:

- A4 Attenuator
- A5 Input
- A26 Output

Amplitude Modulation (AM)

Amplitude Modulation is done on the A26 Output assembly. The modulating signal from the A34 Modulation Distribution assembly is applied to the ALC loop's control voltage.

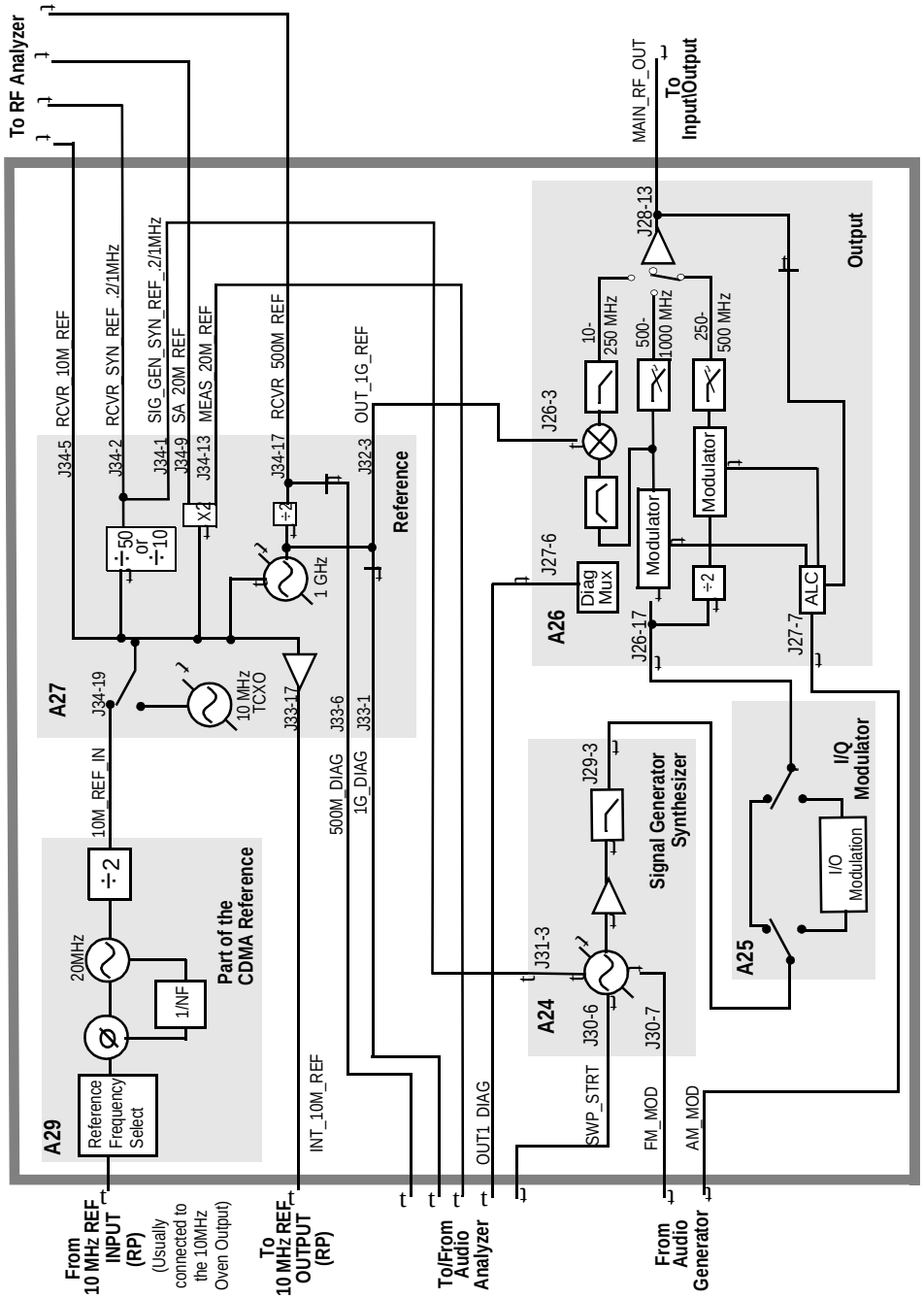


Figure 47 **RF Generation Overview Diagram**

Audio Generator Section

Waveform Generation

The A15 Signal Source and Analyzer gets frequency and waveshape information from the A16 Host Controller. Waveform values are calculated real-time by a digital waveform synthesis IC. The AFGen1 output is always a sine-wave. The AFGen2 output is a sine-wave unless one of the signaling encoder functions is selected from the front panel.

Signaling tones and sequences are generated by AFGen2. This consists of a read-only-memory (ROM) IC that contains the program code for enabling the digital waveform synthesis IC to generate signaling. This ROM is on the A15 assembly.

Level Control

Audio level is controlled by the A34 Modulation Distribution assembly by using a DAC and variable attenuators. The leveled audio signal is passed on to the RF Generator section.

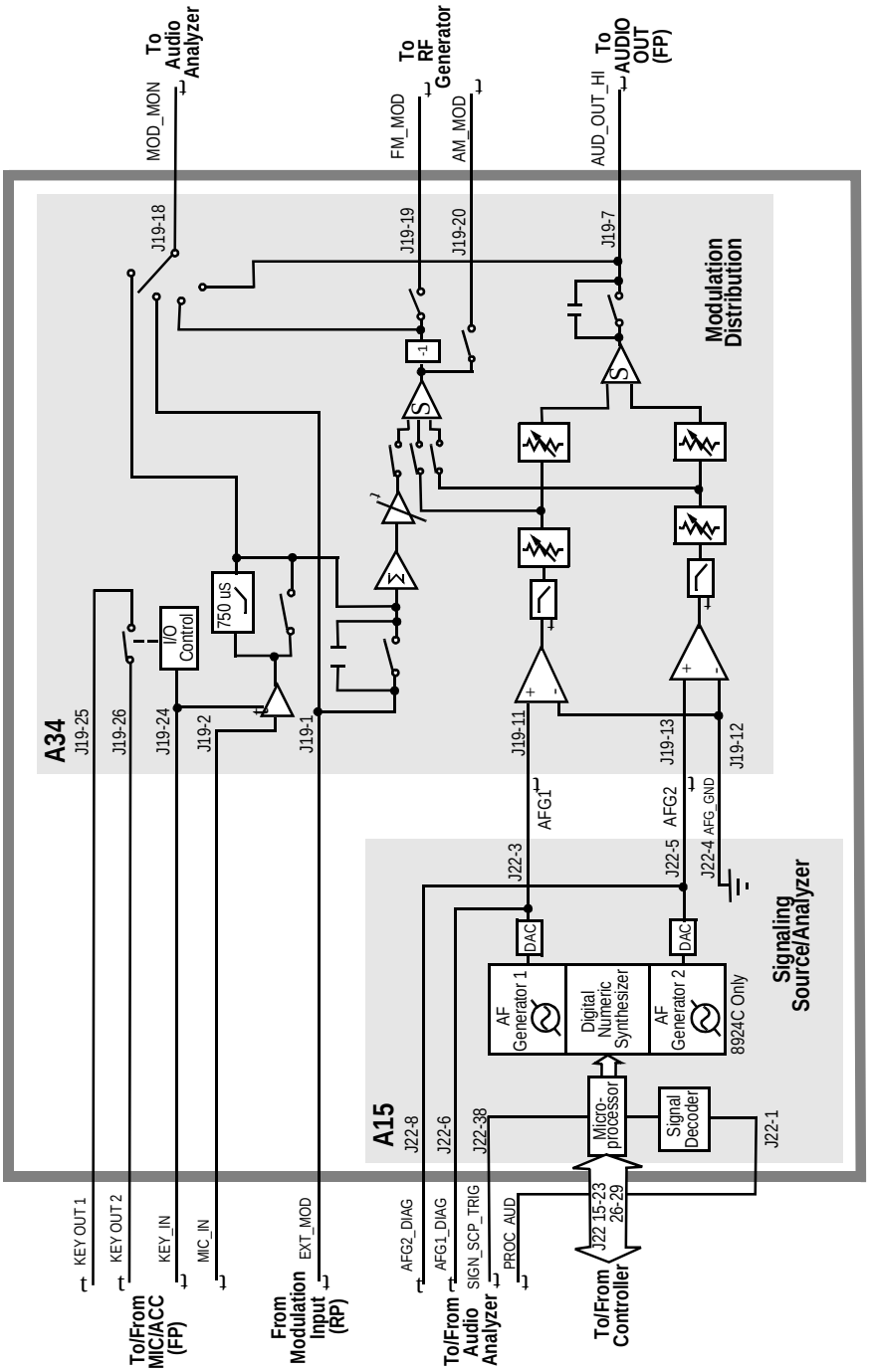


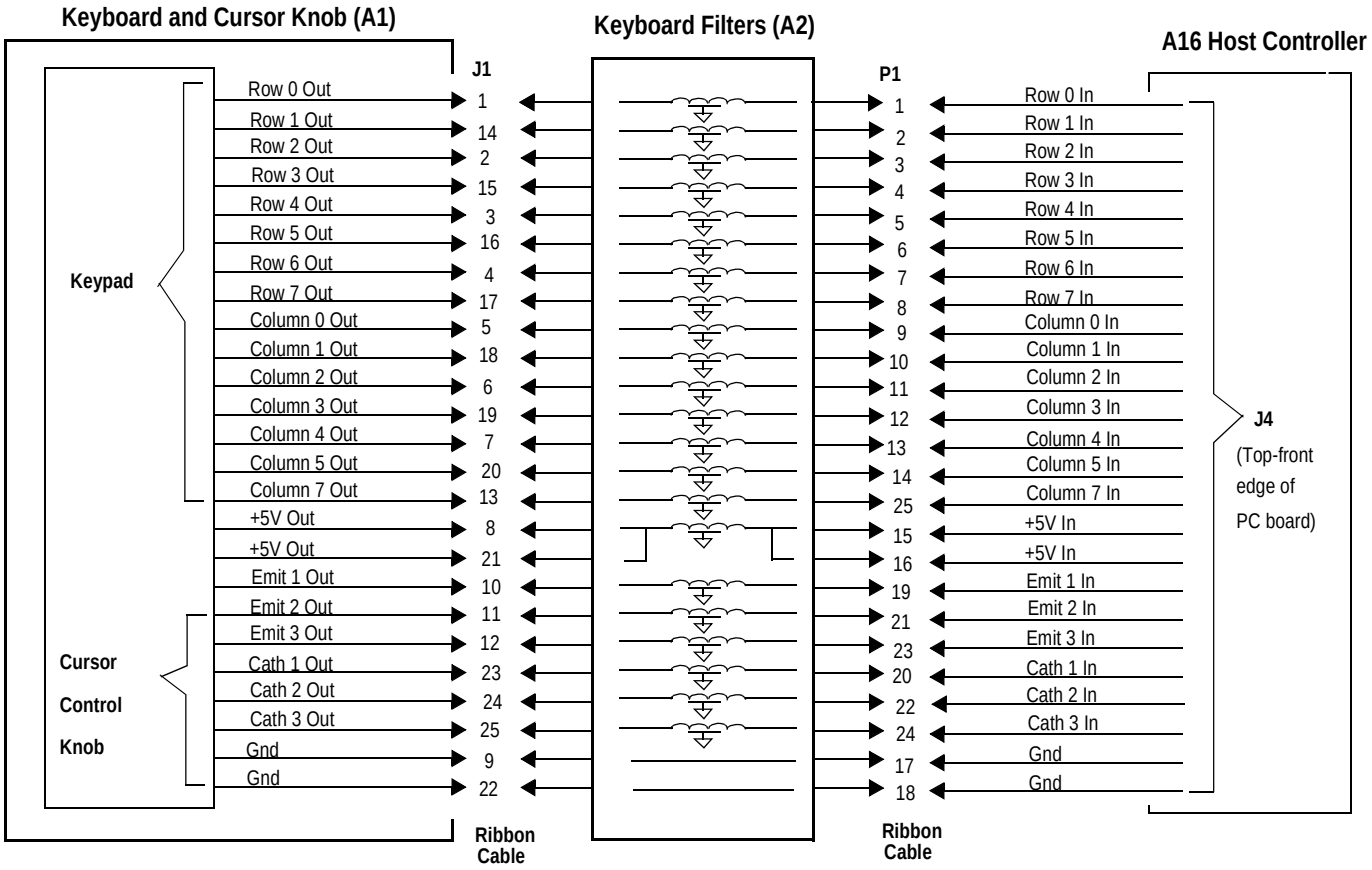
Figure 48 **Audio Signal Generation Overview**

Assembly Details

Assembly Level Block Diagrams

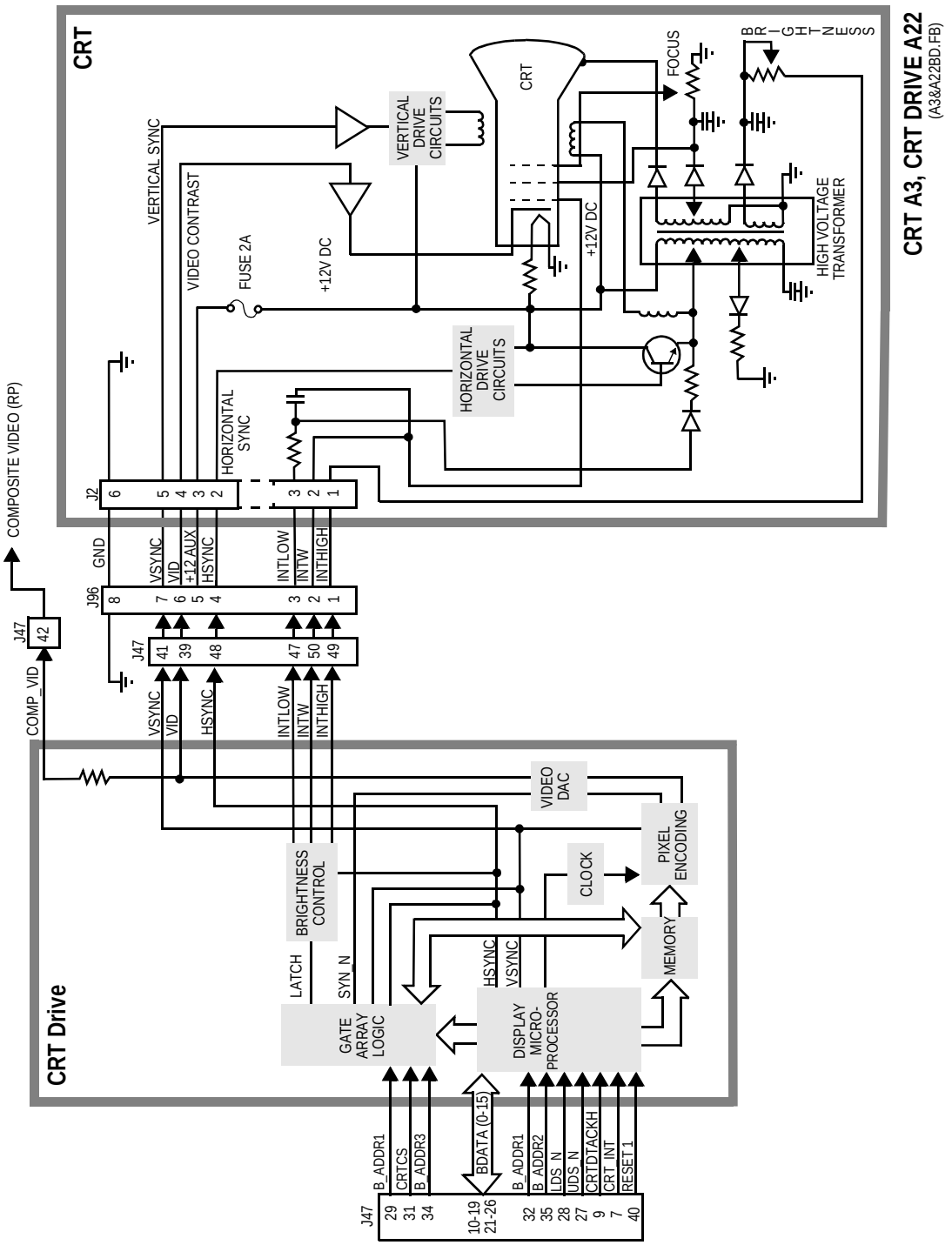
The remainder of this chapter contains individual block diagrams for each assembly in the Test Set. Unless otherwise stated, the connector and pin numbers shown refer to the A40 Motherboard connections.

The tables that accompany some the block diagrams provide switch and/or latch setting information, and module signal Input/Output specifications, for troubleshooting. The switch and latch names and settings are accessed through the SERVICE screen. **See "Service Screen" on page 449** for information on how to use these functions.



A1 Keyboard , A2 Keyboard Filters

(A1&2-BD.FB)


CRT A3, CRT DRIVE A22
(A3&A22BD.FB)
CRT
VERTICAL SYNC
VIDEO CONTRAST
FUSE 2A
+12V DC
VERTICAL DRIVE CIRCUITS
CRT
FOCUS
BRIGHTNESS
+12V DC
HIGH VOLTAGE TRANSFORMER
HORIZONTAL DRIVE CIRCUITS
HORIZONTAL SYNC
J2
GND
VSYNC
VID
+12 AUX
HSYNC
INTLOW
INTW
INTHIGH
J96
J47
COMPOSITE VIDEO (RP)
COMP_VID
CRT Drive
VIDEO DAC
PIXEL ENCODING
CLOCK
BRIGHTNESS CONTROL
MEMORY
LATCH
SYN_N
HSYNC
VSYNC
GATE ARRAY LOGIC
DISPLAY MICRO-PROCESSOR
BDATA (0-15)
B_ADDR1
CRTCS
B_ADDR3
B_ADDR1
B_ADDR2
LDS_N
UDS_N
CRTDTACKH
CRT_INT
RESET1

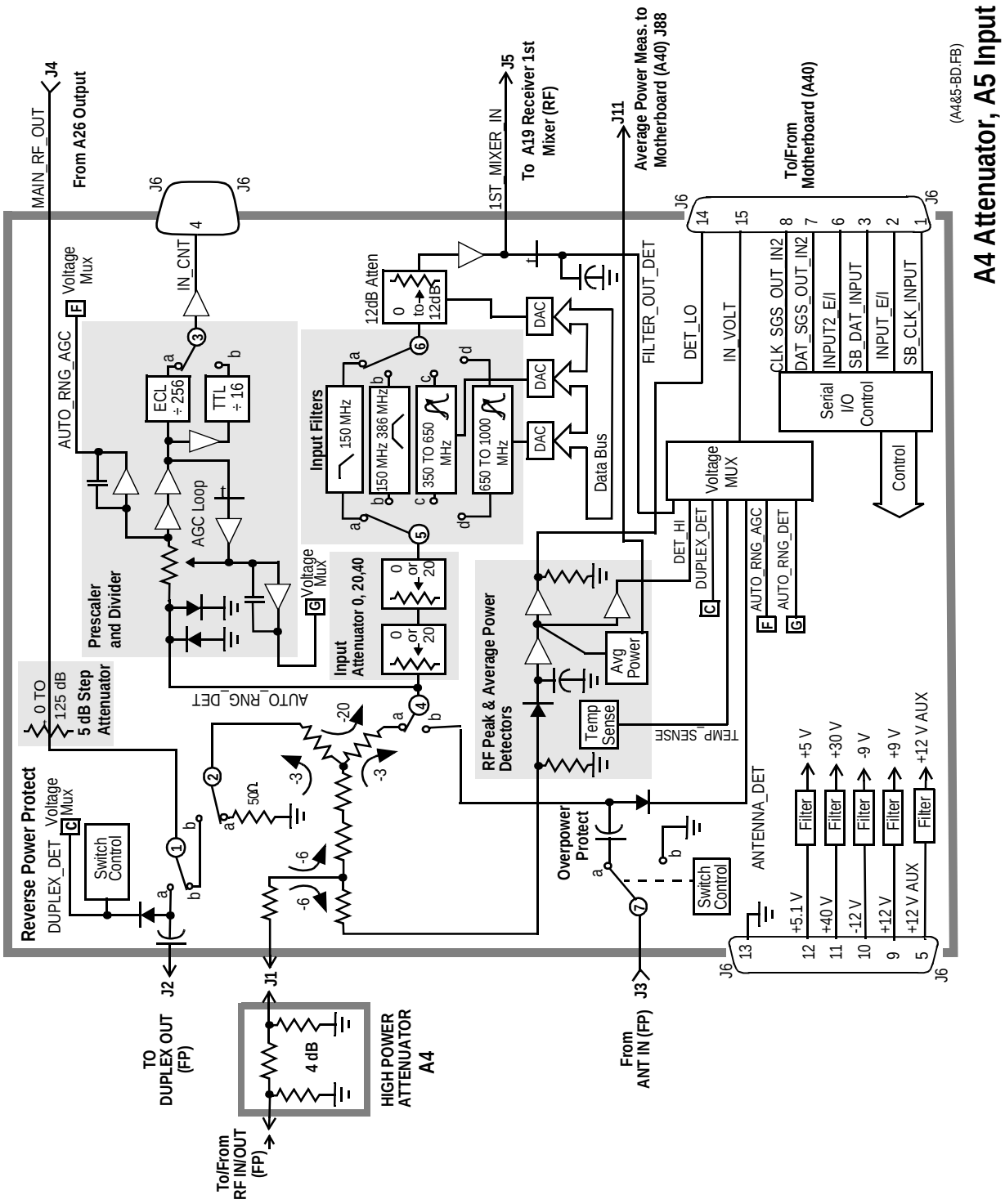
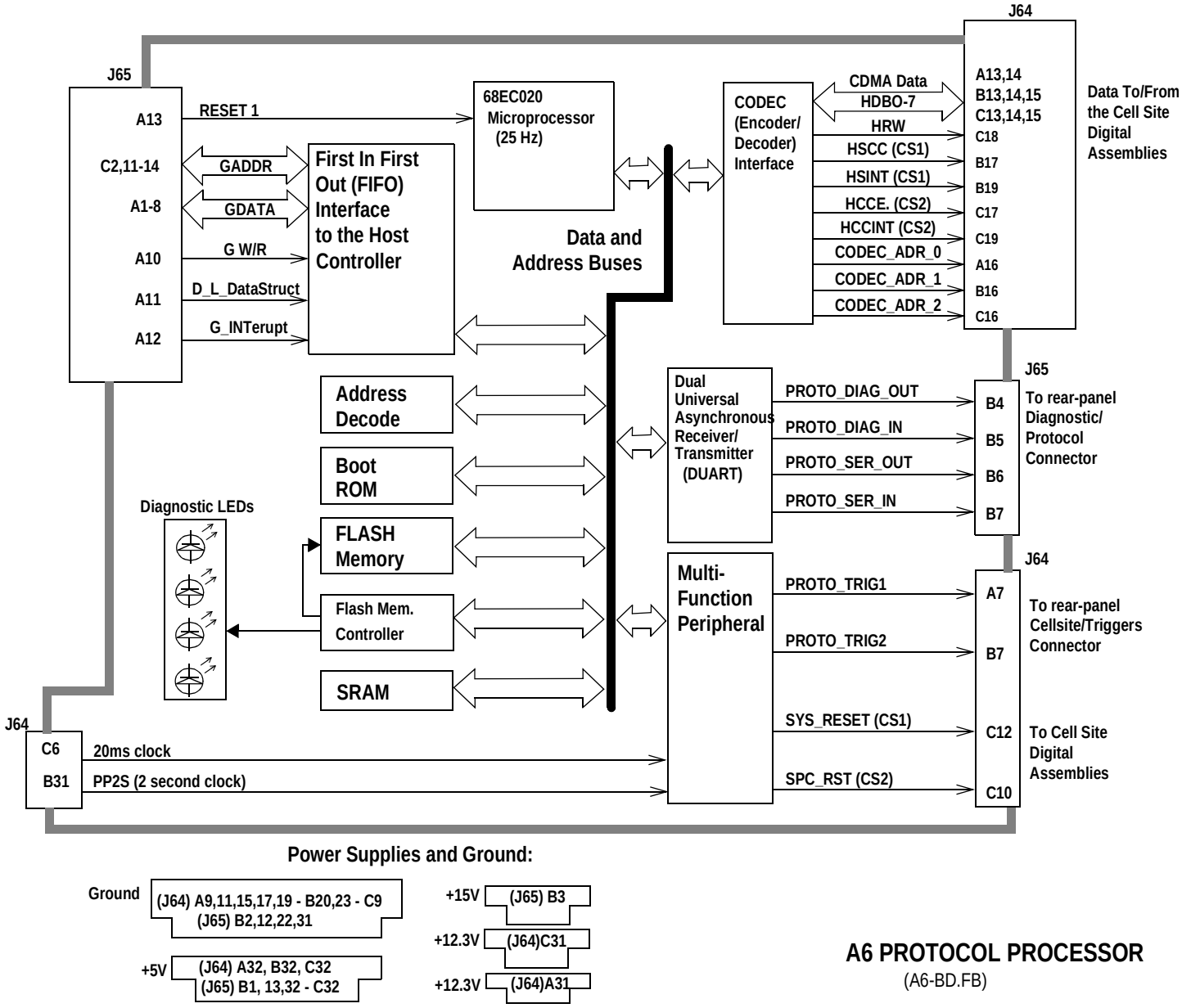

A4 Attenuator, A5 Input
(A4&5-BD.FB)
MAIN_RF_OUT
J4
From A26 Output
1ST_MIXER_IN
J5
To A19 Receiver 1st Mixer (RF)
J11
Average Power Meas. to Motherboard (A40) J88
To/From Motherboard (A40)
J6
IN_CNT
Voltage Mux
AUTO_RNG_AGC
ECL ÷ 256
TTL ÷ 16
AGC Loop
Prescaler and Divider
12dB Atten
0 to 12dB
Input Filters
150 MHz
150 MHz 386 MHz
350 TO 650 MHz
650 TO 1000 MHz
DAC
Data Bus
FILTER_OUT_DET
DET_LO
IN_VOLT
CLK_SGS_OUT_IN2
DAT_SGS_OUT_IN2
INPUT2_E/I
SB_DAT_INPUT
INPUT_E/I
SB_CLK_INPUT
Serial I/O Control
Control
Voltage MUX
DET_HI
DUPLEX_DET
AUTO_RNG_AGC
AUTO_RNG_DET
Input Attenuator 0, 20,40
0 or 20
AUTO_RNG_DET
0 TO 125 dB
5 dB Step Attenuator
RF Peak & Average Power Detectors
Avg Power
Temp Sense
TEMP_SENSE
Reverse Power Protect
DUPLEX_DET
Switch Control
50Ω
-3
-6
-20
Overpower Protect
ANTENNA_DET
Filter
+5 V
+30 V
-9 V
+9 V
+12 V AUX
+5.1 V
+40 V
-12 V
+12 V
+12 V AUX
J2
J1
J3
TO DUPLEX OUT (FP)
4 dB
HIGH POWER ATTENUATOR A4
From ANT IN (FP)
To/From RF IN/OUT (FP)

Table 90 Switch Control A5 Input

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	inpt_dup_op_reset	a	1	Instrument MEAS RESET
		b	0	When Reverse Power Is Applied
2	inpt_duplex_switch	a	1	RF Generator Output Port to Duplex
		b	0	RF Generator Output Port to RF Out
3	Counter Connection	a		Service Screen Counter Connection to INPUT_ECL_COUNT
		b		Service Screen Counter Connection to INPUT_TTL_COUNT
4	inpt_antenna_switch	a	0	RF Analyzer Input Port to RF IN
		b	1	RF Analyzer Input Port to Antenna
5	inpt_filter_select	a	1D	RF Analyzer Tune Freq <150 MHz
		b	1B	RF Analyzer Tune Freq >150 MHz <380 MHz
		c	16	RF Analyzer Tune Freq >380 MHz <650 MHz
		d	E	RF Analyzer Tune Freq >650 MHz
6	inpt_filter_select	a	1D	RF Analyzer Tune Freq <150 MHz
		b	1B	RF Analyzer Tune Freq >150 MHz <380 MHz
		c	16	RF Analyzer Tune Freq >380 MHz <650 MHz
		d	E	RF Analyzer Tune Freq >650 MHz
7	inpt_ant_op_reset	a	1	Instrument MEAS RESET
		b	0	When Overpower is Applied

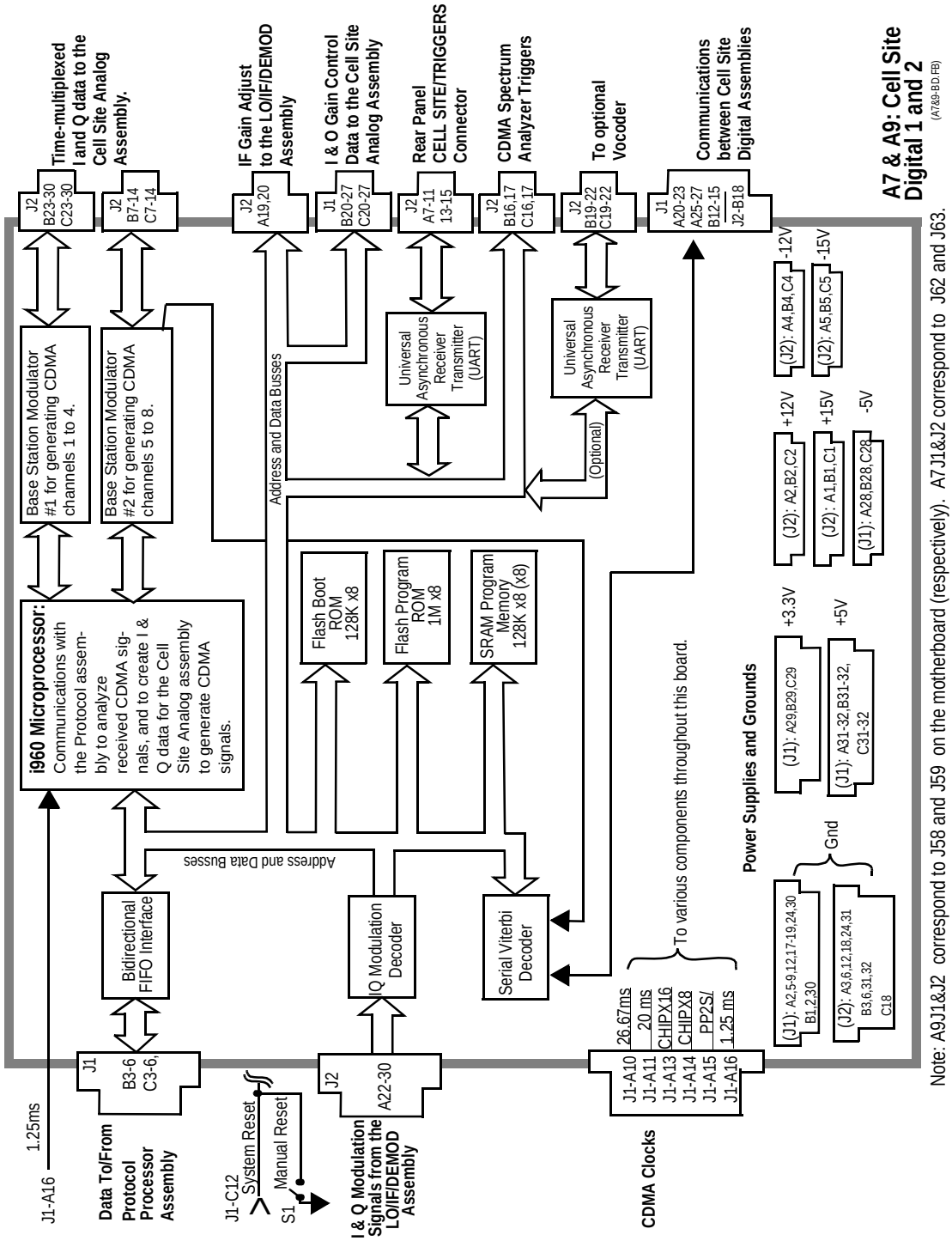
Table 91 I/O Specs A5 Input

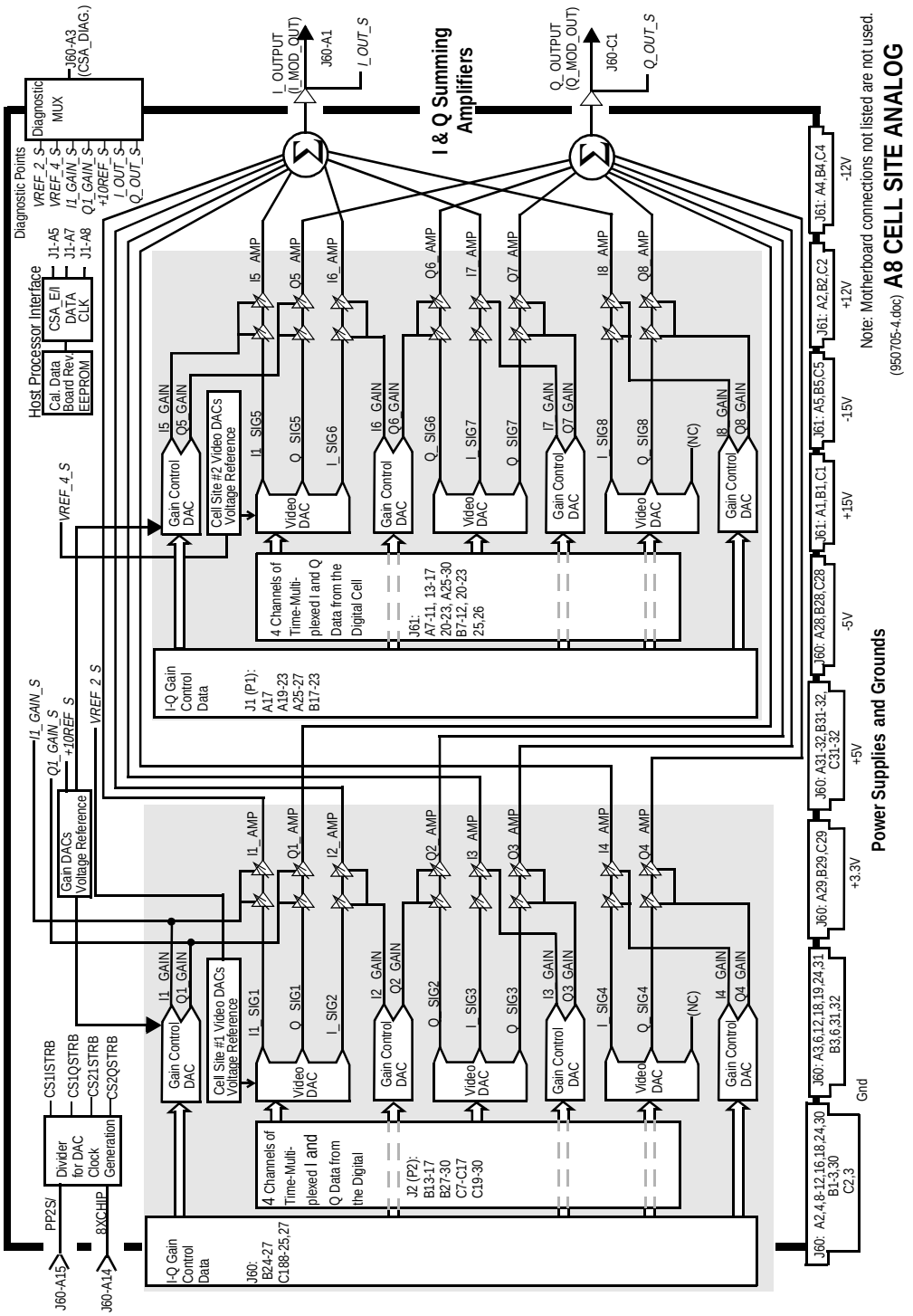
Connector	Name	Type	Range	Max
			Min	
J1	RF IN/OUT	Input	30 MHz	1000 MHz
				1.2 Watts
J2	DUPLEX OUT	Output	30 MHz	1000 MHz
J3	ANTENNA IN	Input	30 MHz	1000 MHz
				0.10 Watts
J4	MAIN_RF_OUT	Input	30 MHz	1000 MHz
				<1 dBm
J5	1ST_MIXER_IN	Output	30 MHz	1000 MHz
			–22 dBm	–12 dBm

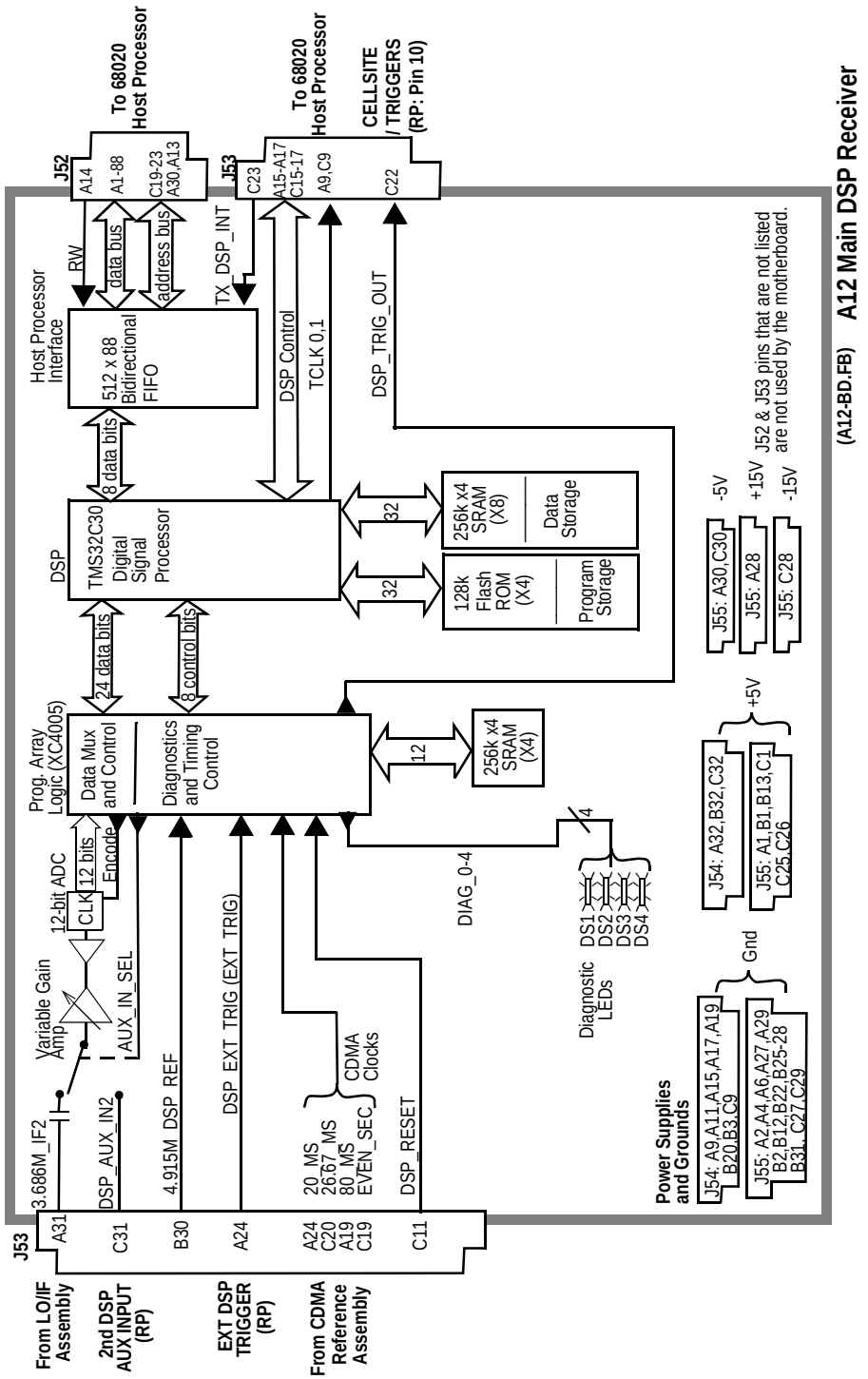


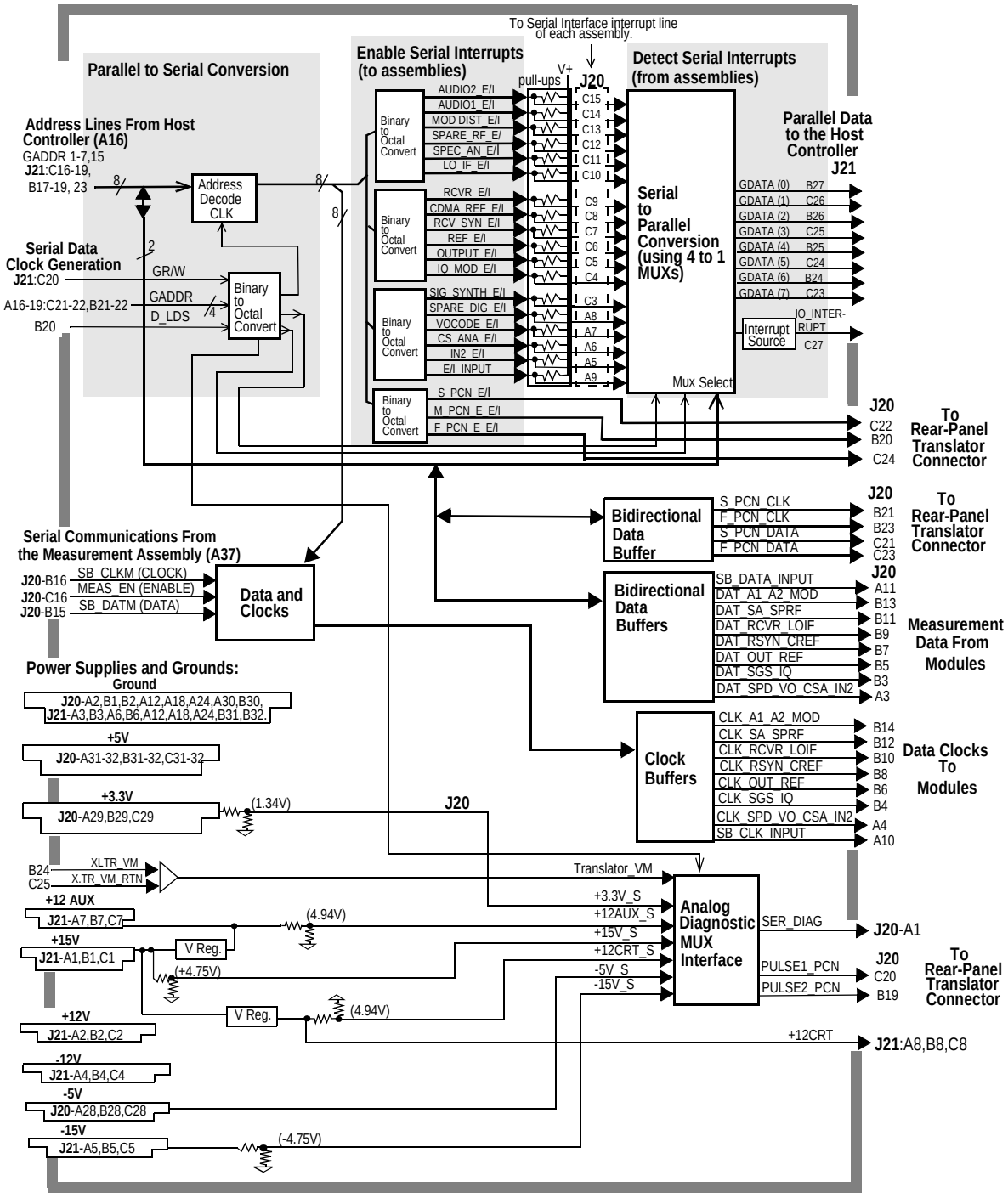
A6 PROTOCOL PROCESSOR

(A6-BD.FB)


A7 & A9: Cell Site
Digital 1 and 2
(A7&9-BD.FB)
Time-multiplexed I and Q data to the Cell Site Analog Assembly.
IF Gain Adjust to the LO/IF/DEMOD Assembly
I & Q Gain Control Data to the Cell Site Analog Assembly
Rear Panel CELL SITE/TRIGGERS Connector
CDMA Spectrum Analyzer Triggers
To optional Vocoder
Communications between Cell Site Digital Assemblies
J2 B23-30 C23-30
J2 B7-14 C7-14
J2 A19,20
J1 B20-27 C20-27
J2 A7-11 13-15
J2 B16,17 C16,17
J2 B19-22 C19-22
J1 A20-23 A25-27 B12-15 J2-B18
Base Station Modulator #1 for generating CDMA channels 1 to 4.
Base Station Modulator #2 for generating CDMA channels 5 to 8.
Address and Data Busses
Universal Asynchronous Receiver Transmitter (UART)
Universal Asynchronous Receiver Transmitter (UART)
(Optional)
i960 Microprocessor: Communications with the Protocol assembly to analyze received CDMA signals, and to create I & Q data for the Cell Site Analog assembly to generate CDMA signals.
Flash Boot ROM 128K x8
Flash Program ROM 1M x8
SRAM Program Memory 128K x8 (x8)
(J2): A4,B4,C4 -12V
(J2): A5,B5,C5 -15V
(J2): A2,B2,C2 +12V
(J2): A1,B1,C1 +15V
(J1): A28,B28,C28 -5V
Power Supplies and Grounds
(J1): A29,B29,C29 +3.3V
(J1): A31-32,B31-32, C31-32 +5V
Gnd
(J1): A2,5-9,12,17-19,24,30 B1,2,30
(J2): A3,6,12,18,24,31 B3,6,31,32 C18
Address and Data Busses
Bidirectional FIFO Interface
IQ Modulation Decoder
Serial Viterbi Decoder
To various components throughout this board.
J1 B3-6 C3-6,
J2 A22-30
J1-A10 26.67ms
J1-A11 20 ms
J1-A13 CHIPX16
J1-A14 CHIPX8
J1-A15 PP2S/
J1-A16 1.25 ms
1.25ms
J1-A16
Data To/From Protocol Processor Assembly
J1-C12 System Reset
S1 Manual Reset
I & Q Modulation Signals from the LO/IF/DEMOD Assembly
CDMA Clocks
Note: A9J1&J2 correspond to J58 and J59 on the motherboard (respectively). A7J1&J2 correspond to J62 and J63.

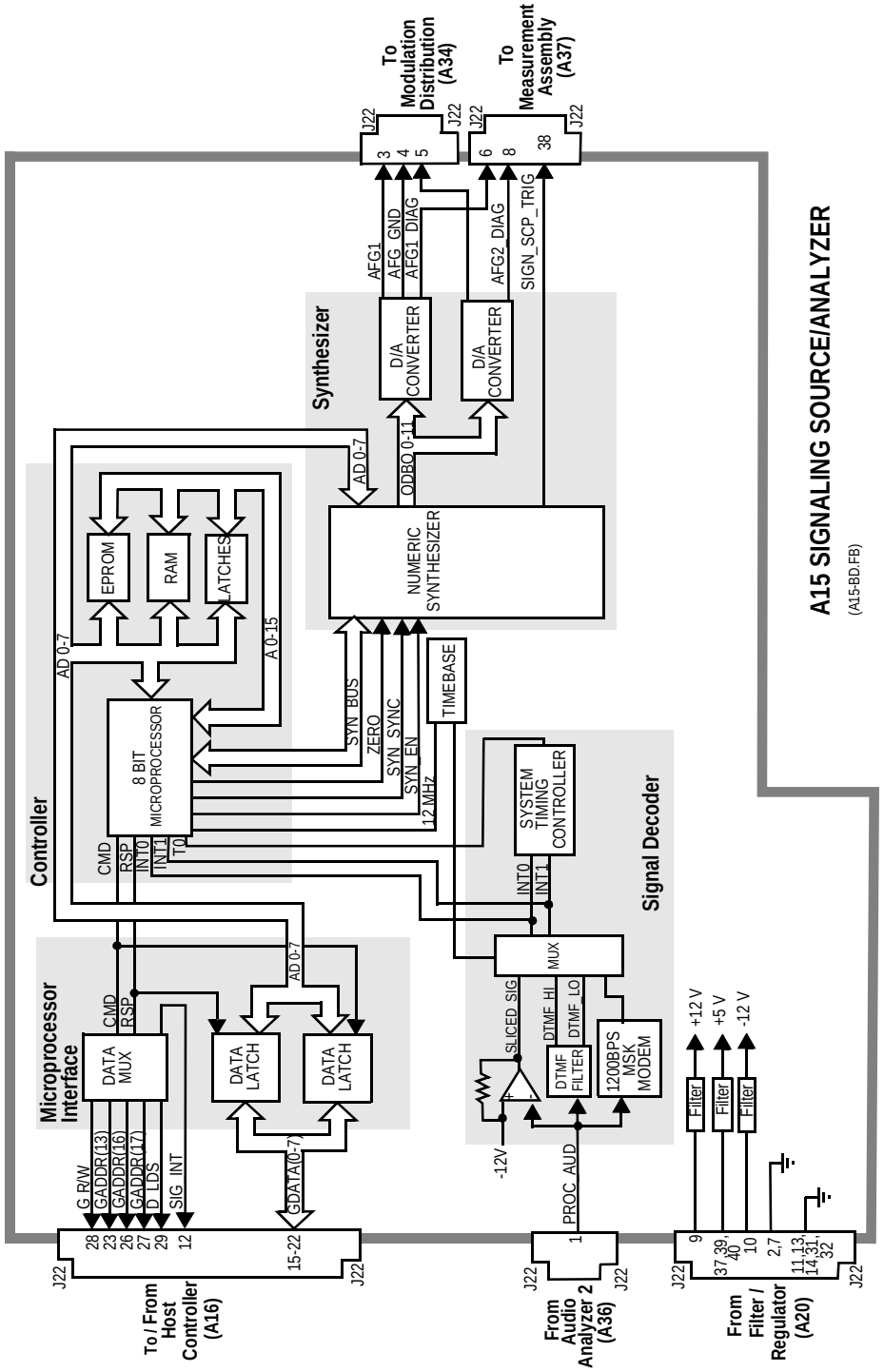

A8 CELL SITE ANALOG
(950705-4.doc)
Note: Motherboard connections not listed are not used.
I & Q Summing Amplifiers
I_ OUTPUT (I_MOD_OUT)
Q_ OUTPUT (Q_MOD_OUT)
J60-A1
J60-C1
I_OUT_S
Q_OUT_S
Diagnostic MUX
J60-A3 (CSA_DIAG.)
Diagnostic Points
VREF_2_S
VREF_4_S
I1_GAIN_S
Q1_GAIN_S
+10REF_S
I_OUT_S
Q_OUT_S
J1-A5
J1-A7
J1-A8
Host Processor Interface
CSA_E/I
DATA
CLK
Cal. Data Board Rev EEPROM
Gain DACs Voltage Reference
Cell Site #2 Video DACs Voltage Reference
Cell Site #1 Video DACs Voltage Reference
Gain Control DAC
Video DAC
I-Q Gain Control Data
J1 (P1): A17 A19-23 A25-27 B17-23
J60: B24-27 C18B-25,27
J2 (P2): B13-17 B27-30 C7-C17 C19-30
J61: A7-11, 13-17 20-23, A25-30 B7-12, 20-23 25,26
4 Channels of Time-Multi-plexed I and Q Data from the Digital Cell
Divider for DAC Clock Generation
CS11STRB
CS1QSTRB
CS21STRB
CS2QSTRB
PP2S/
8XCHIP
J60-A15
J60-A14
Power Supplies and Grounds
+3.3V
+5V
-5V
+15V
-15V
+12V
-12V
Gnd
J60: A29,B29,C29
J60: A31-32,B31-32 C31-32
J60: A28,B28,C28
J61: A1,B1,C1
J61: A5,B5,C5
J61: A2,B2,C2
J61: A4,B4,C4
J60: A3,6,12,18,19,24,31 B3,6,31,32
J60: A2,4,8-12,16,18,24,30 B1-3,30 C2,3
(NC)


A12 Main DSP Receiver
(A12-BD.FB)
J53
From LO/IF Assembly
2nd DSP AUX INPUT (RP)
EXT DSP TRIGGER (RP)
From CDMA Reference Assembly
A31
C31
B30
A24
A24 C20 A19 C19
C11
3.686M_IF2
DSP_AUX_IN2
4.915M_DSP_REF
DSP_EXT_TRIG (EXT_TRIG)
20_MS 26.67_MS 80_MS EVEN_SEC
CDMA Clocks
DSP_RESET
Variable Gain Amp
AUX_IN_SEL
12-bit ADC
CLK
12 bits
Encode
Prog. Array Logic (XC4005)
Data Mux and Control
Diagnostics and Timing Control
24 data bits
8 control bits
DIAG_0-4
12
256k x4 SRAM (X4)
4
Diagnostic LEDs
DS1
DS2
DS3
DS4
DSP
TMS32C30 Digital Signal Processor
8 data bits
32
256k x4 SRAM (X8)
Data Storage
32
128k Flash ROM (X4)
Program Storage
Host Processor Interface
512 x 88 Bidirectional FIFO
RW
data bus
address bus
J52
A14
A1-88
C19-23 A30,A13
To 68020 Host Processor
TX_DSP_INT
J53
C23
A15-A17 C15-17
A9,C9
To 68020 Host Processor
DSP Control
TCLK 0,1
DSP_TRIG_OUT
CELLSITE / TRIGGERS (RP: Pin 10)
C22
J52 & J53 pins that are not listed are not used by the motherboard.
-5V
+15V
-15V
J55: A30,C30
J55: A28
J55: C28
+5V
J54: A32,B32,C32
J55: A1,B1,B13,C1 C25,C26
Gnd
Power Supplies and Grounds
J54: A9,A11,A15,A17,A19 B20,B3,C9
J55: A2,A4,A6,A27,A29 B2,B12,B22,B25-28 B31, C27,C29



(A14-BD.FB)

A14 HOST SERIAL I/O INTERFACE


A15 SIGNALING SOURCE/ANALYZER
(A15-BD.FB)
To Modulation Distribution (A34)
To Measurement Assembly (A37)
J22
3
4
5
6
8
38
AFG1
AFG_GND
AFG1_DIAG
AFG2_DIAG
SIGN_SCP_TRIG
Synthesizer
D/A CONVERTER
D/A CONVERTER
ODBO 0-11
AD 0-7
NUMERIC SYNTHESIZER
TIMEBASE
SYN_BUS
ZERO
SYN_SYNC
SYN_EN
12 MHz
Controller
EPROM
RAM
LATCHES
A 0-15
AD 0-7
8 BIT MICROPROCESSOR
CMD
RSP
INT0
INT1
T0
SYSTEM TIMING CONTROLLER
INT0
INT1
Signal Decoder
MUX
SLICED_SIG
DTMF_HI
DTMF_LO
DTMF FILTER
1200BPS MSK MODEM
-12V
PROC_AUD
+12 V
+5 V
-12 V
Filter
Filter
Filter
Microprocessor Interface
CMD
RSP
AD 0-7
DATA MUX
DATA LATCH
DATA LATCH
G R/W
GADDR(13)
GADDR(16)
GADDR(17)
D_LDS
SIG_INT
GDATA(0-7)
28
23
26
27
29
12
15-22
1
9
37,39,
40
10
2,7
11,13,
14,31,
32
To / From Host Controller (A16)
From Audio Analyzer 2 (A36)
From Filter / Regulator (A20)

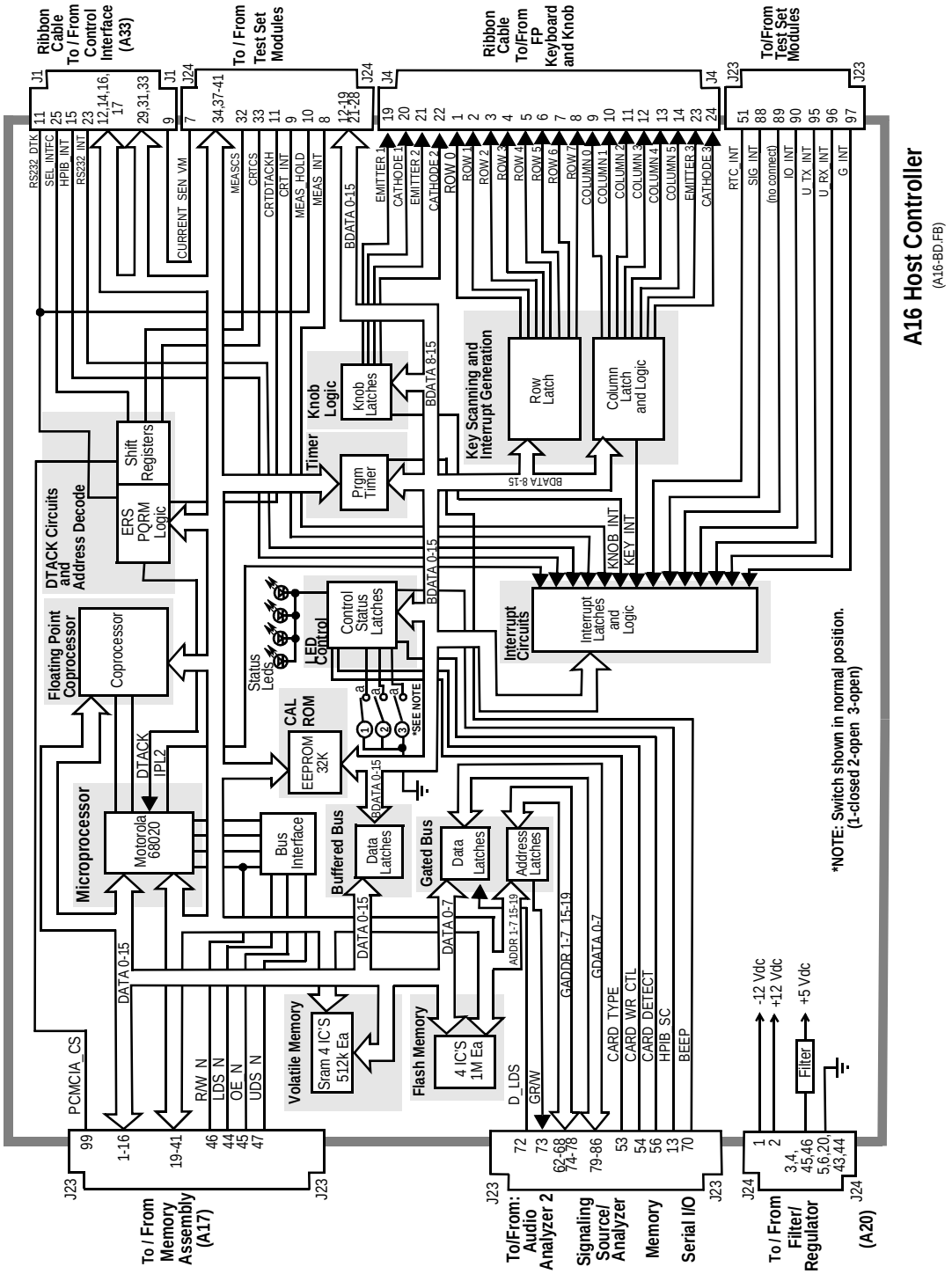
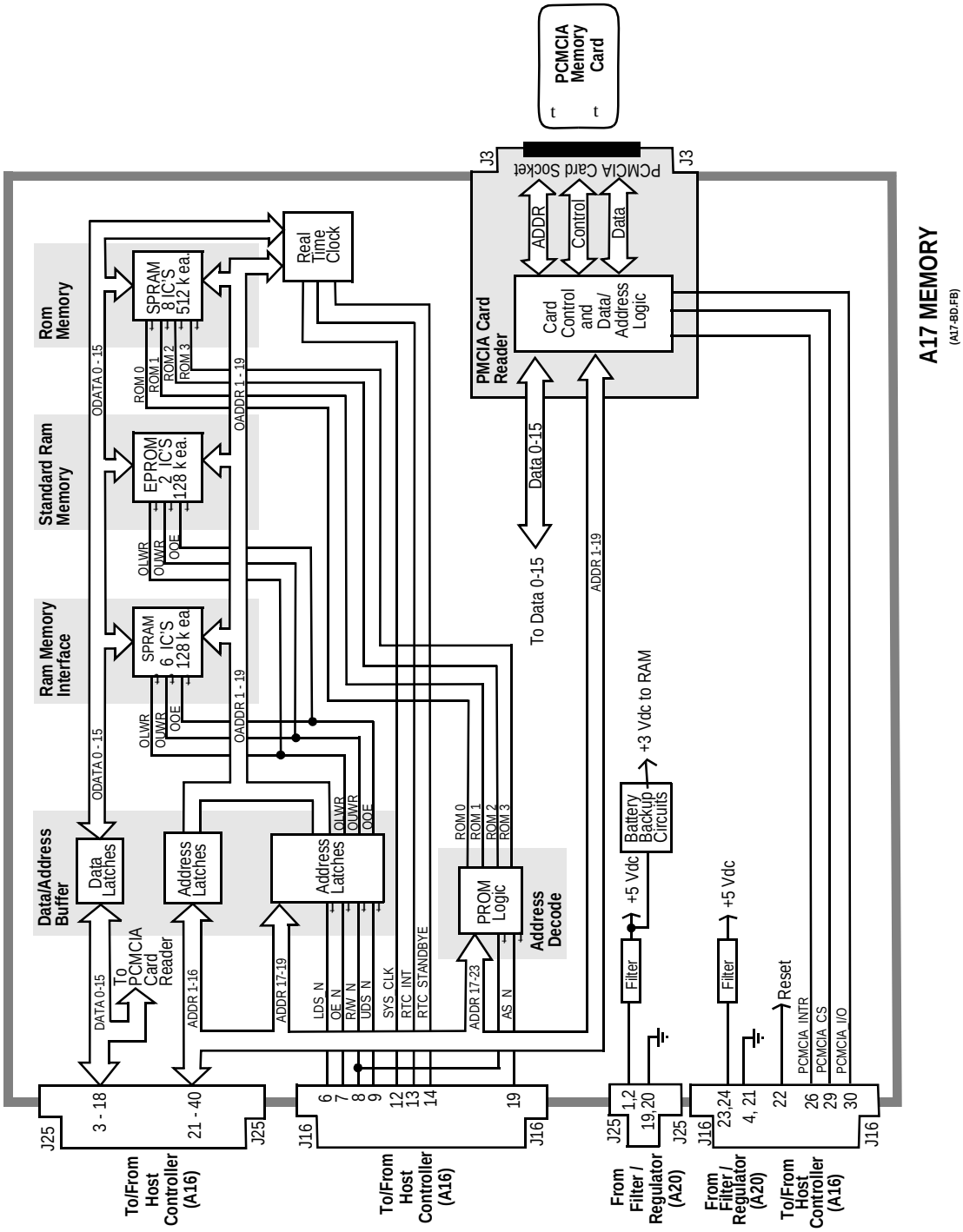

A16 Host Controller
(A16-BD.FB)
*NOTE: Switch shown in normal position.
(1-closed 2-open 3-open)
Ribbon Cable To / From Control Interface (A33)
To / From Test Set Modules
Ribbon Cable To/From FP Keyboard and Knob
To/From Test Set Modules
DTACK Circuits and Address Decode
Shift Registers
ERS PORM Logic
Floating Point Coprocessor
Coprocessor
Microprocessor
Motorola 68020
DTACK
IPL2
Bus Interface
Buffered Bus
Data Latches
CAL ROM
EEPROM 32K
Status Leds
LED Control
Control Status Latches
*SEE NOTE
Timer
Prgm Timer
Knob Logic
Knob Latches
Key Scanning and Interrupt Generation
Row Latch
Column Latch and Logic
Interrupt Circuits
Interrupt Latches and Logic
Gated Bus
Data Latches
Address Latches
Volatile Memory
Sram 4 IC'S 512k Ea
Flash Memory
4 IC'S 1M Ea
Filter
To / From Memory Assembly (A17)
To/From: Audio Analyzer 2
Signaling Source/ Analyzer
Memory
Serial I/O
To / From Filter/ Regulator
(A20)

Table 92 Switch Control A16 Host Controller

Switch No.	Switch Name	Position	Hex Value	Instrument Setting
1	Write Protect/ Unprotect	a		Manually Switched to Unprotected
		open		Manually Switch to Protected
2	Smart Card Type	a		Manually Switched to Epson TypeReader
		open		Manually Switched to PCMCIA Type Reader
3	Memory Type	a		Manually Switched to One Time Programma-ble ROM
		open		Manually Switched to Flash ROM


A17 MEMORY
(A17-BD.FB)
PCMCIA Memory Card
PCMCIA Card Socket
J3
ADDR
Control
Data
PMCIA Card Reader
Card Control and Data/ Address Logic
Data 0-15
To Data 0-15
ADDR 1-19
Real Time Clock
Rom Memory
SPRAM 8 IC'S 512 k ea.
ROM 0
ROM 1
ROM 2
ROM 3
ODATA 0 - 15
OADDR 1 - 19
Standard Ram Memory
EPROM 2 IC'S 128 k ea.
OLWR
OUWR
OOE
Ram Memory Interface
SPRAM 6 IC'S 128 k ea.
Data/Address Buffer
Data Latches
Address Latches
Address Latches
PROM Logic
Address Decode
DATA 0-15
To PCMCIA Card Reader
ADDR 1-16
ADDR 17-19
ADDR 17-23
LDS_N
OE_N
R/W_N
UDS_N
SYS CLK
RTC_INT
RTC_STANDBYE
AS_N
Battery Backup Circuits
+3 Vdc to RAM
+5 Vdc
+5 Vdc
Filter
Filter
Reset
PCMCIA_INTR
PCMCIA_CS
PCMCIA_I/O
J25
3 - 18
21 - 40
J25
To/From Host Controller (A16)
J16
6
7
8
9
12
13
14
19
J16
To/From Host Controller (A16)
J25
1,2
19,20
J25
From Filter / Regulator (A20)
J16
23,24
4, 21
22
26
29
30
J16
From Filter / Regulator (A20)
To/From Host Controller (A16)

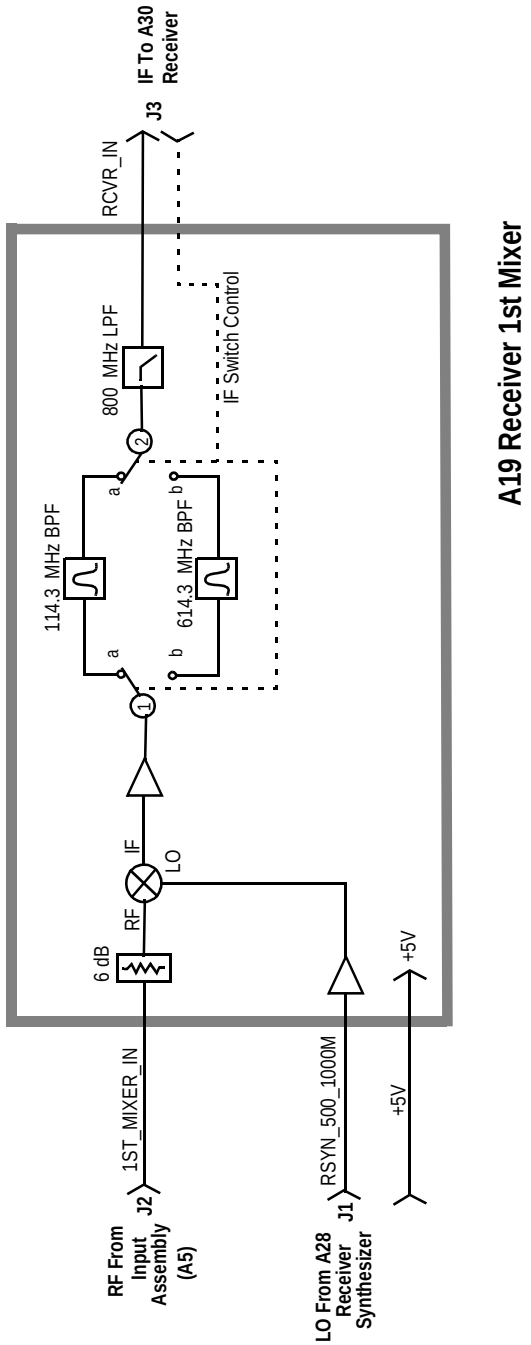
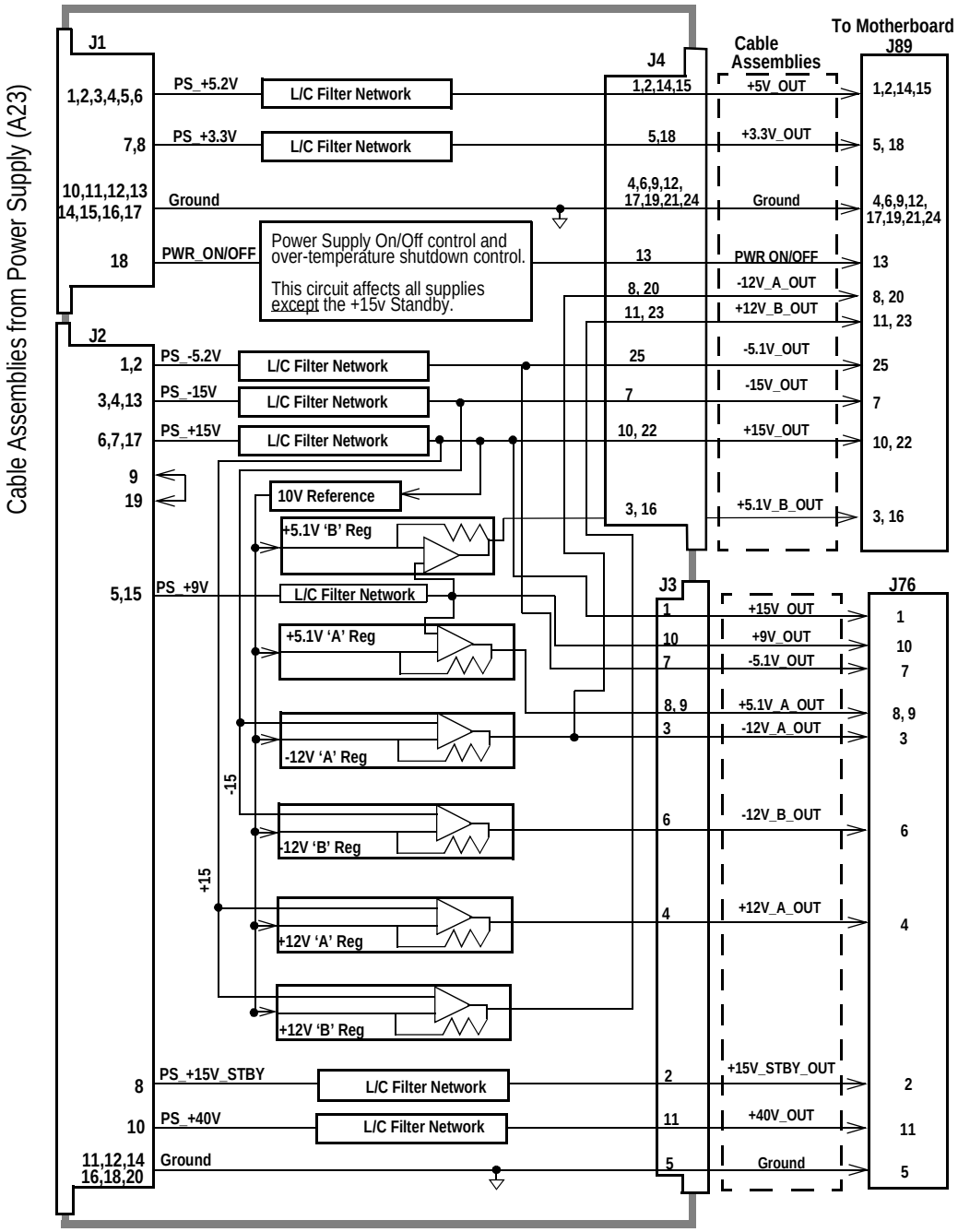

A19 Receiver 1st Mixer
(A19-BD.FB)
IF To A30 Receiver
J3
RCVR_IN
800 MHz LPF
IF Switch Control
114.3 MHz BPF
614.3 MHz BPF
a
b
1
2
IF
LO
RF
6 dB
+5V
1ST_MIXER_IN
RSYN_500_1000M
J2
J1
RF From Input Assembly (A5)
LO From A28 Receiver Synthesizer

Table 93 Switch Control A19 Receiver Mixer

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	rcvr_if_path_select	a	2	RF Analyzer Tune Frequency ≥380.7 MHz
		b	1	RF Analyzer Tune Frequency <380.7 MHz
2	rcvr_if_path_select	a	2	RF Analyzer Tune Frequency ≥380.7 MHz
		b	1	RF Analyzer Tune Frequency <380.7MHz

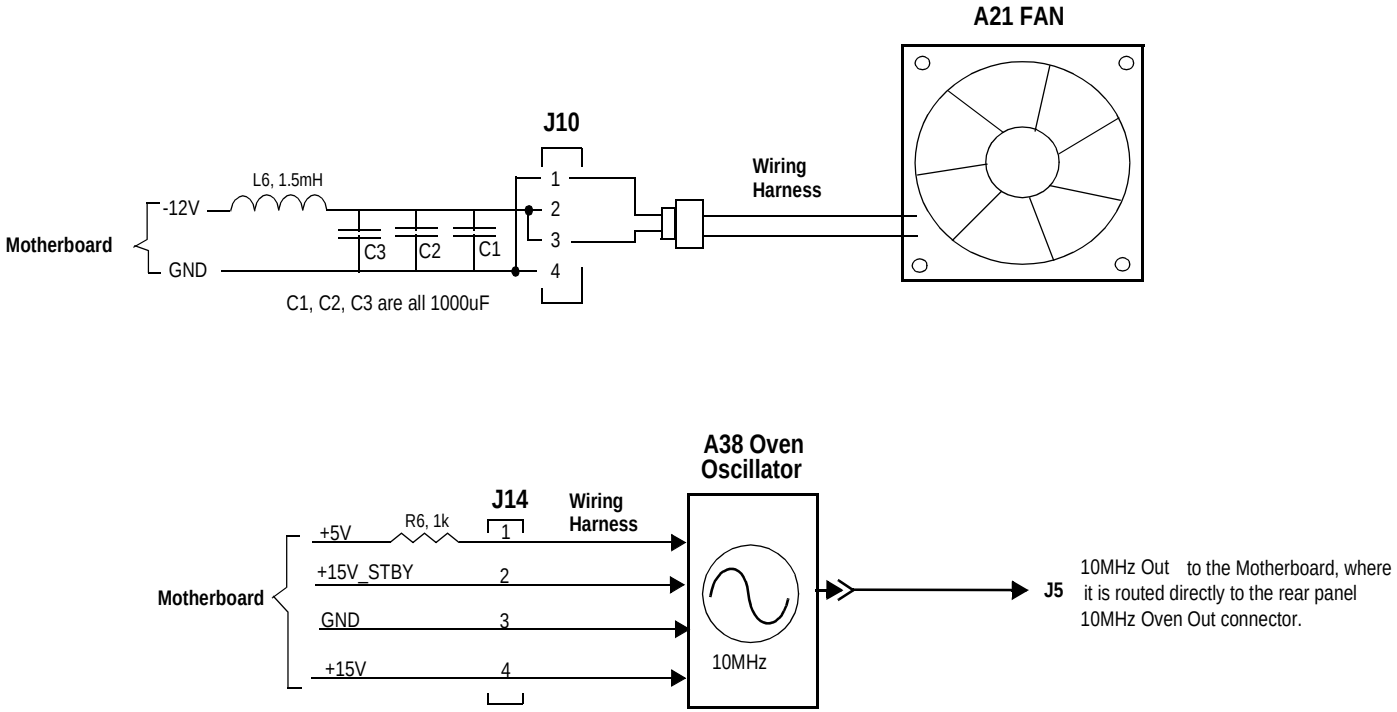
Table 94 I/O Specs A19 Receiver Mixer

Connector	Name	Type	Range	
			Min	Max
J1	RSYN_500_1000M	Input	500 MHz	1000 MHz
			0 dBm	+6 dBm
J2	1ST_MIXER_IN	Input	0.4 MHz	10000 MHz
J3	RCVR_IN	Output	– 37 dBm	–14 dBm



(A20&23BD.FB)

A20 Filter/Regulator, A23 Power Supply Connections



A21 Fan, A38 Oven Oscillator

(A21&38BD.FB)

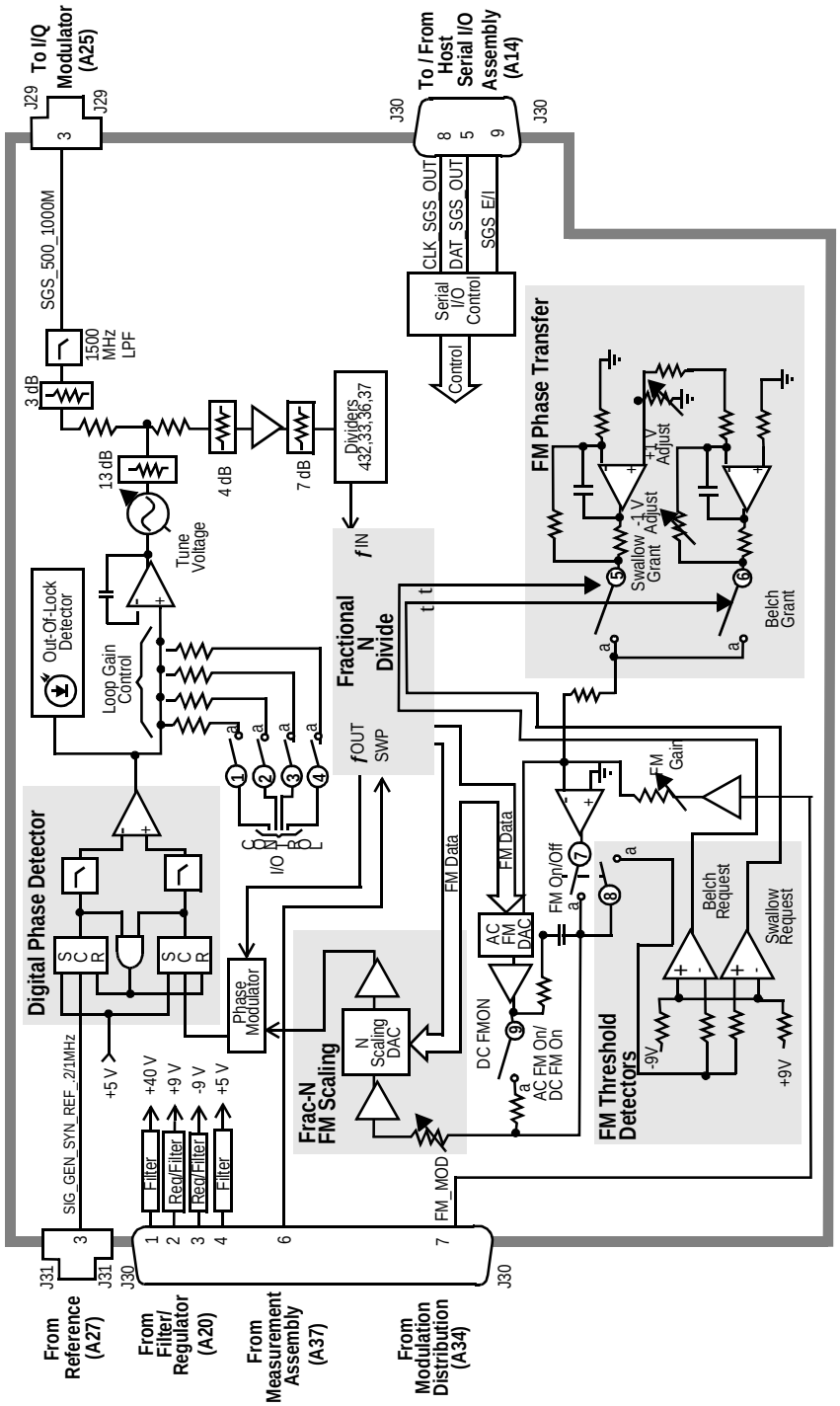
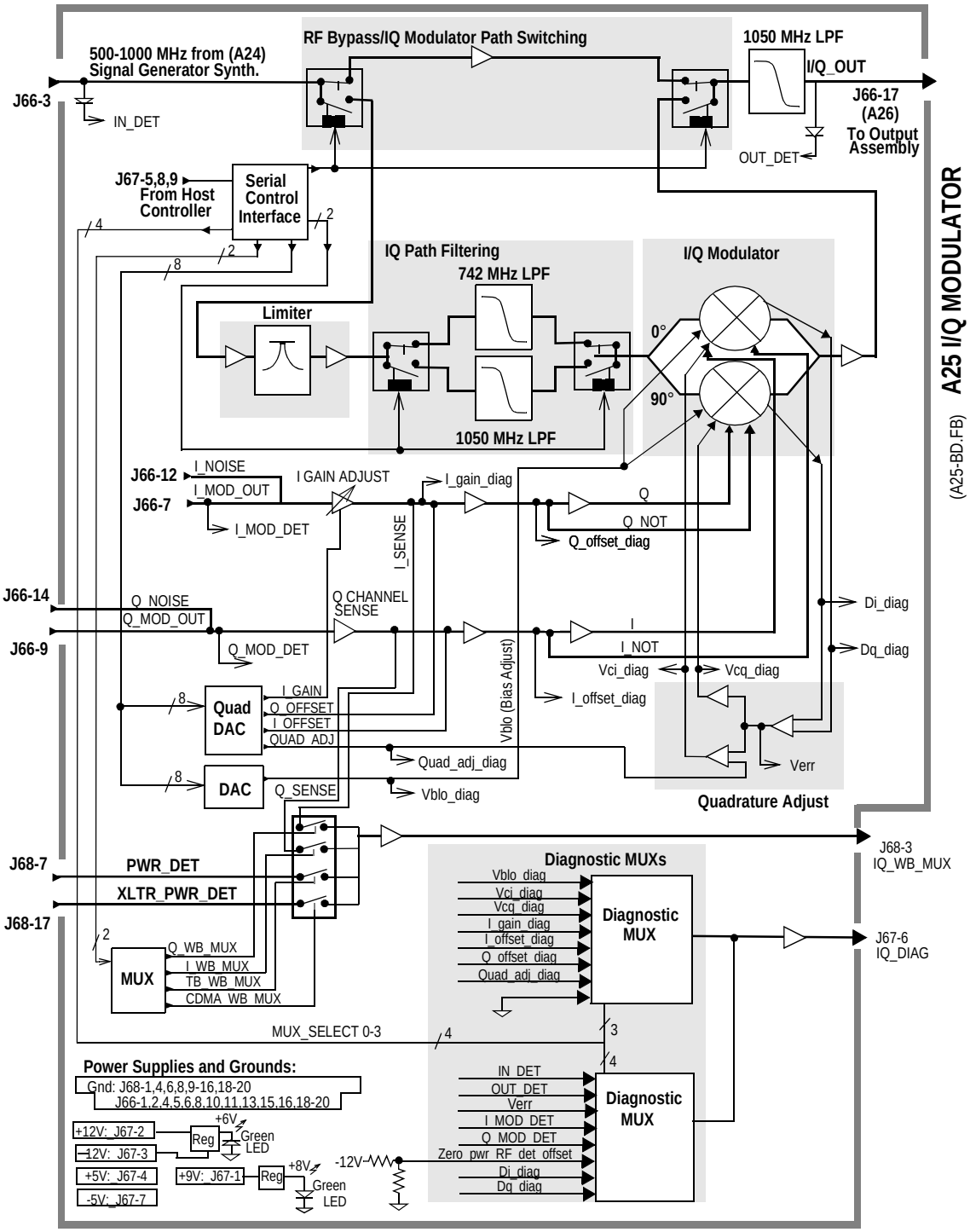

A24 SIGNAL GENERATOR SYNTHESIZER
(A24-BD.FB)
To I/Q Modulator (A25)
To / From Host Serial I/O Assembly (A14)
SGS_500_1000M
1500 MHz LPF
3 dB
13 dB
4 dB
7 dB
Dividers 432,33,36,37
Tune Voltage
Out-Of-Lock Detector
Loop Gain Control
Fractional N Divide
fIN
fOUT
SWP
Serial I/O Control
CLK_SGS_OUT
DAT_SGS_OUT
SGS_E/I
Control
FM Phase Transfer
+1 V Adjust
Swallow Grant
-1 V Adjust
Belch Grant
FM Gain
FM Data
FM Qn/Off
AC FM DAC
DC FMON
AC FM On/ DC FM On
FM Threshold Detectors
Belch Request
Swallow Request
-9V
+9V
Digital Phase Detector
S C R
Phase Modulator
Frac-N FM Scaling
N Scaling DAC
I/O BUS
SIG_GEN_SYN_REF_2/1MHz
+5 V
+40 V
+9 V
-9 V
+5 V
Filter
Reg/Filter
Reg/Filter
Filter
FM_MOD
From Reference (A27)
From Filter/ Regulator (A20)
From Measurement Assembly (A37)
From Modulation Distribution (A34)

Table 95 Switch Control A24 Signal Generator Synthesizer

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	gsyn_gain_control	a		Note: Gain Control switches are set in either single positions or combinations according to receiver tuning frequency. Independent hexadecimal values are not applicable.
		open		
2	gsyn_gain_control	a		
		open		
3	gsyn_gain_control	a		
		open		
4	gsyn_gain_control	a		
		open		
5	Swallow Grant	open	1	Part of FM Loop - No User Control
		a	0	Part of FM Loop - No User Control
6	Belch Grant	a	1	Part of FM Loop - No User Control
		open	0	Part of FM Loop - No User Control
7	gsyn_fm	a	1	RF Generator AF Gen1 to FM On
		open	0	RF Generator AF Gen1 to FM Off
8	gsyn_fm	a	1	RF Generator AF Gen1 to FM On
		open	0	RF Generator AF Gen1 to FM Off
9	gsyn_dc_fm_state	a	1	RF Generator FM Coupling AC
		open	0	RF Generator FM Coupling DC

Table 96 I/O Specs A24 Signal Generator Synthesizer

Connector	Name	Type	Range	
			Min	Max
J31-3	SIG_GEN_SYN_REF_ 0.2/1 MHz	Input	CMOS	CMOS
J30-6	SWP_STRT	Input	TTL	TTL
J30-7	FM_MOD	Input	O Vp	4 Vp
J29-3	SGS_500_1000M	Output	–2 dBm	+2 dBm


A25 I/Q MODULATOR
(A25-BD.FB)
RF Bypass/IQ Modulator Path Switching
500-1000 MHz from (A24)
Signal Generator Synth.
J66-3
IN_DET
1050 MHz LPF
I/Q_OUT
J66-17
(A26)
To Output
Assembly
OUT_DET
J67-5,8,9
From Host
Controller
Serial
Control
Interface
IQ Path Filtering
742 MHz LPF
Limiter
I/Q Modulator
0°
90°
1050 MHz LPF
J66-12
I_NOISE
I_MOD_OUT
J66-7
I_MOD_DET
I GAIN ADJUST
I_gain_diag
I_SENSE
Q
Q_NOT
Q_offset_diag
J66-14
Q_NOISE
Q_MOD_OUT
J66-9
Q_MOD_DET
Q CHANNEL
SENSE
I
I_NOT
Vci_diag
Vcq_diag
I_offset_diag
Di_diag
Dq_diag
Vblo (Bias Adjust)
Quad
DAC
I_GAIN
Q_OFFSET
I_OFFSET
QUAD_ADJ
Quad_adj_diag
DAC
Q_SENSE
Vblo_diag
Verr
Quadrature Adjust
J68-7
PWR_DET
XLTR_PWR_DET
J68-17
J68-3
IQ_WB_MUX
Diagnostic MUXs
Vblo_diag
Vci_diag
Vcq_diag
I_gain_diag
I_offset_diag
Q_offset_diag
Quad_adj_diag
Diagnostic
MUX
J67-6
IQ_DIAG
MUX
Q_WB_MUX
I_WB_MUX
TB_WB_MUX
CDMA_WB_MUX
MUX_SELECT 0-3
Power Supplies and Grounds:
Gnd: J68-1,4,6,8,9-16,18-20
J66-1,2,4,5,6,8,10,11,13,15,16,18-20
+12V: J67-2
-12V: J67-3
+5V: J67-4
-5V: J67-7
+9V: J67-1
Reg
+6V
+8V
Green
LED
-12V
IN_DET
OUT_DET
Verr
I_MOD_DET
Q_MOD_DET
Zero_pwr_RF_det_offset
Di_diag
Dq_diag
Diagnostic
MUX

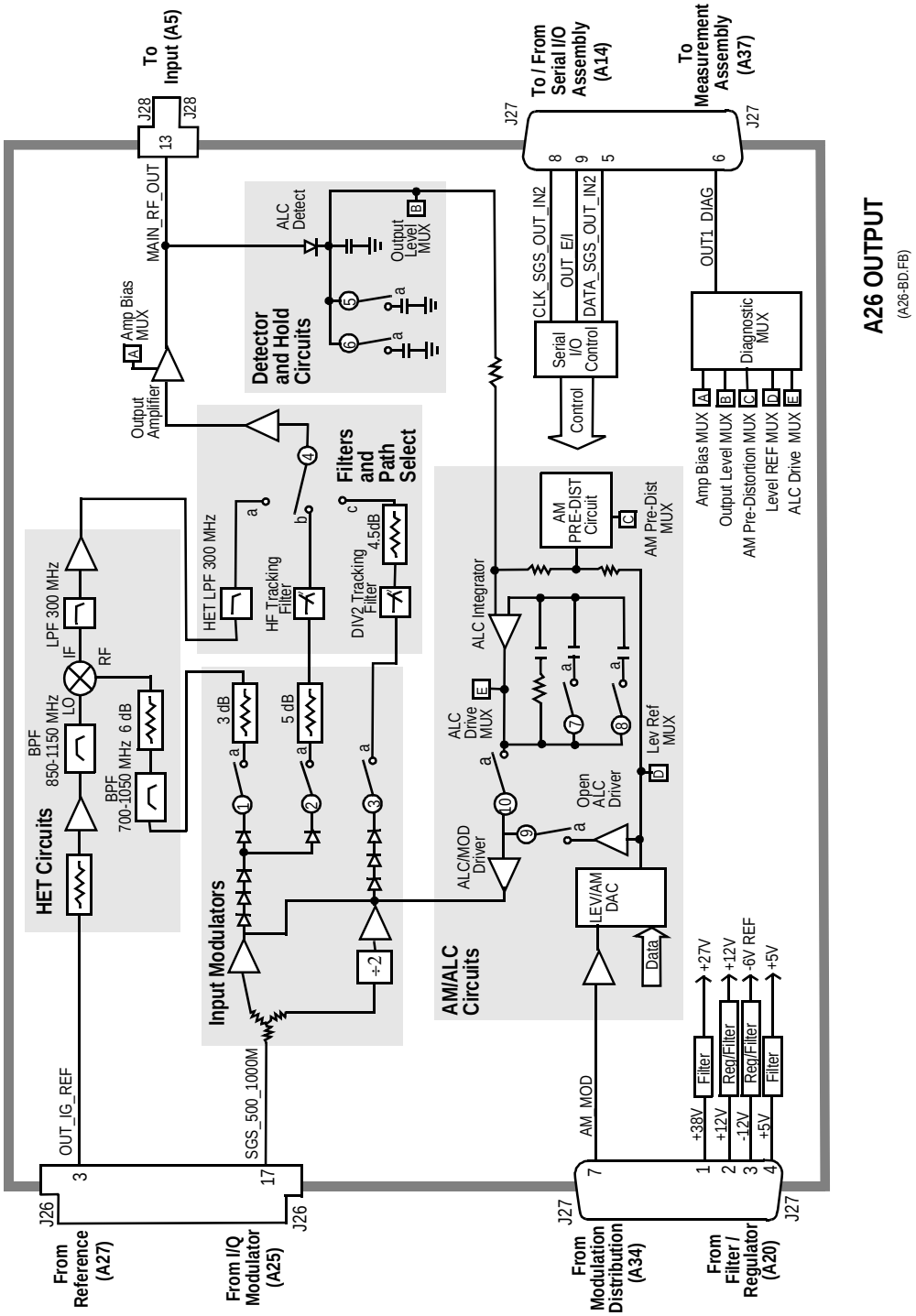

A26 OUTPUT
(A26-BD.FB)
To Input (A5)
J28
13
MAIN_RF_OUT
Amp Bias MUX
Output Amplifier
Detector and Hold Circuits
ALC Detect
Output Level MUX
Filters and Path Select
HET LPF 300 MHz
HF Tracking Filter
DIV2 Tracking Filter
4.5dB
HET Circuits
LPF 300 MHz
IF
RF
LO
BPF 850-1150 MHz
BPF 700-1050 MHz
6 dB
Input Modulators
3 dB
5 dB
÷2
SGS_500_1000M
OUT_IG_REF
J26
From Reference (A27)
From I/Q Modulator (A25)
AM/ALC Circuits
ALC Integrator
AM PRE-DIST Circuit
AM Pre-Dist MUX
ALC Drive MUX
Lev Ref MUX
Open ALC Driver
ALC/MOD Driver
LEV/AM DAC
Data
AM_MOD
J27
From Modulation Distribution (A34)
To / From Serial I/O Assembly (A14)
CLK_SGS_OUT_IN2
OUT E/I
DATA_SGS_OUT_IN2
Serial I/O Control
Control
To Measurement Assembly (A37)
OUT1 DIAG
Diagnostic MUX
Amp Bias MUX
Output Level MUX
AM Pre-Distortion MUX
Level REF MUX
ALC Drive MUX
+38V
+12V
-12V
+5V
+27V
+12V
-6V REF
+5V
Filter
Reg/Filter
Reg/Filter
Filter
From Filter / Regulator (A20)

Table 97 Switch Control A26 Output

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	out_band_select	a	4	RF Generator RF Gen Freq to <250 MHz
		open	Not 4	RF Generator RF Gen Freq to ≥250 MHz
2	out_band_select	a	1	RF Generator RF Gen Freq to ≥500 MHz
		open	Not 1	RF Generator RF Gen Freq to <500 MHz
3	out_band_select	a	2	RF Generator RF Gen Freq to ≥250 MHz <500 MHz
		open	Not 2	RF Generator RF Gen Freq to <250 MHz ≥500 MHz
4	out_band_select	a	4	RF Generator RF Gen Freq to <250 MHz
		b	1	RF Generator RF Gen Freq to ≥500 MHz
		c	2	RF Generator RF Gen Freq to ≥250 MHz <500 MHz
5	out_det_time_cntl	a	1	Condition not used in 8924C operation.
		open	2 or 3	RF Generator RF Gen Freq ≥ 30 MHz
6	out_det_time_cntl	a	2	Condition not used in 8924C operation.
		open	1 or 3	RF Generator RF Gen Freq ≥ 30 MHz

Table 97 Switch Control A26 Output (Continued)

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
7	out_ALC_bw_cntl	a	2	RF Generator RF Gen Freq ≤ 30 MHz
		open	1	RF Generator AF Gen1 to AM Off
8	out_ALC_bw_cntl	a	0	RF Generator AFGen1 to AM RF Gen Freq ≥30 MHz
		open	1	RF Generator AFGen1 to AM Off
9	out_ALC_state	a	1	Condition Not Used in 8924C Operation
		open	0	Normal Operation
10	out_ALC_state	a	0	Normal Operation
		open	1	Condition Not Used in 8924C Operation

Table 98 I/O Specs A26 Output

Connector	Name	Type	Range	
			Min	Max
J26-3	OUT_1G_REF	Input	–1 dBm	+3 dBm
J26-17	SGS_500_1000M	Input	–2 dBm	+2 dBm
J27-7	AM_MOD	Input	0 Vp	4 Vp
J28-13	MAIN_RF_OUT	Output	–6 dBm	+16 dBm

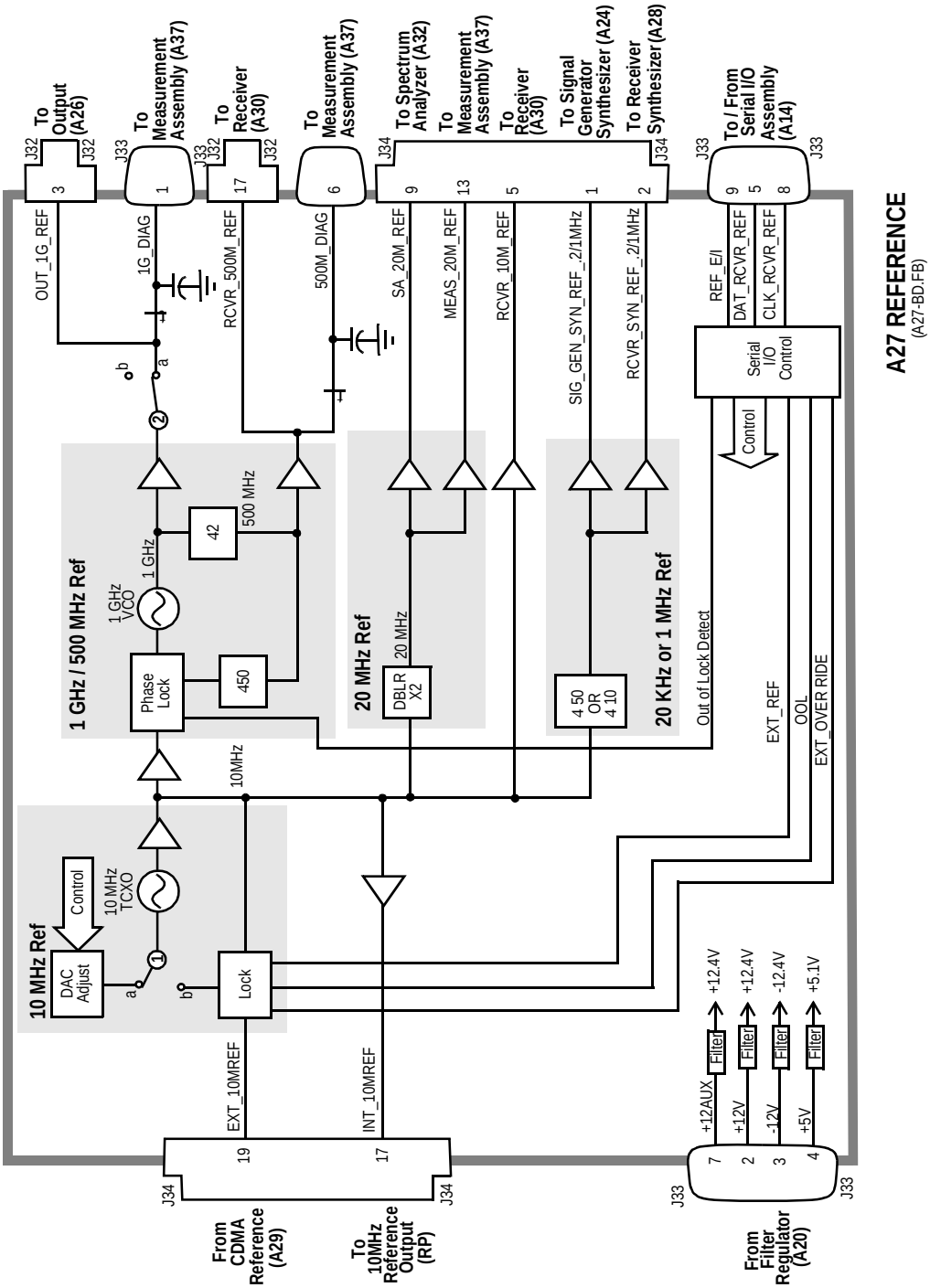

A27 REFERENCE
(A27-BD.FB)
To Output (A26)
To Measurement Assembly (A37)
To Receiver (A30)
To Measurement Assembly (A37)
To Spectrum Analyzer (A32)
To Measurement Assembly (A37)
To Receiver (A30)
To Signal Generator Synthesizer (A24)
To Receiver Synthesizer (A28)
To / From Serial I/O Assembly (A14)
OUT_1G_REF
1G_DIAG
RCVR_500M_REF
500M_DIAG
SA_20M_REF
MEAS_20M_REF
RCVR_10M_REF
SIG_GEN_SYN_REF_.2/1MHz
RCVR_SYN_REF_.2/1MHz
REF_E/I
DAT_RCVR_REF
CLK_RCVR_REF
Serial I/O Control
Control
1 GHz / 500 MHz Ref
1 GHz VCO
Phase Lock
42
500 MHz
450
20 MHz Ref
DBLR X2
20 MHz
20 KHz or 1 MHz Ref
4 50 OR 4 10
Out of Lock Detect
10MHz
EXT_REF
OOL
EXT_OVER RIDE
10 MHz Ref
Control
10 MHz TCXO
DAC Adjust
Lock
EXT_10MREF
INT_10MREF
+12AUX
+12V
-12V
+5V
Filter
+12.4V
+12.4V
-12.4V
+5.1V
From CDMA Reference (A29)
To 10MHz Reference Output (RP)
From Filter Regulator (A20)

Table 99 Switch Control A27 Reference

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	refs_tbase_select	a	1	Normal Operation
		b	0	Automatic Selection if External lT Base Applied
2	refs_1GHz_switch	a	1	RF Generator RF Gen Freq <249 MHz
		open	0	RF Generator RF Gen Freq ≥ 249 MHz

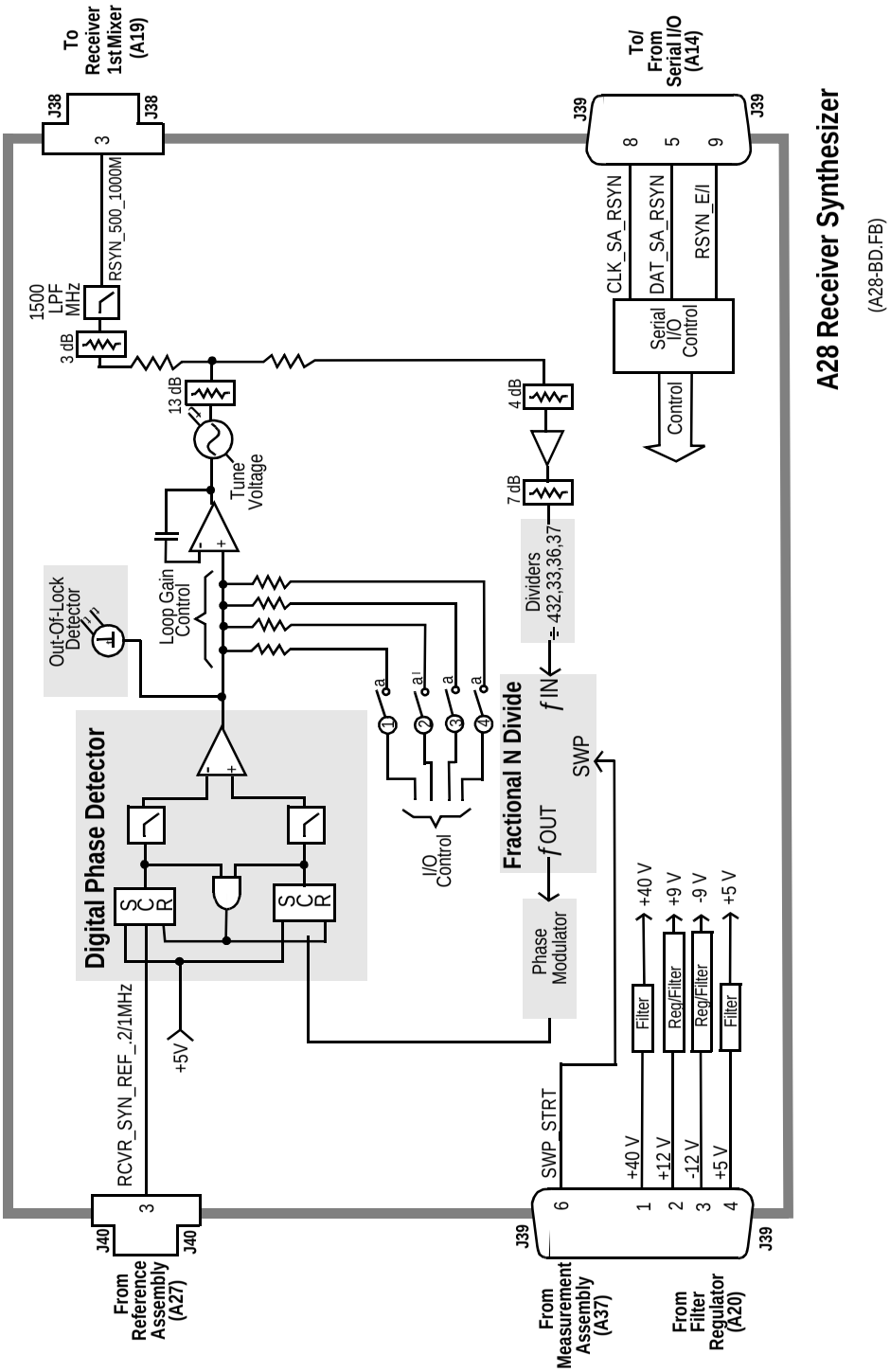
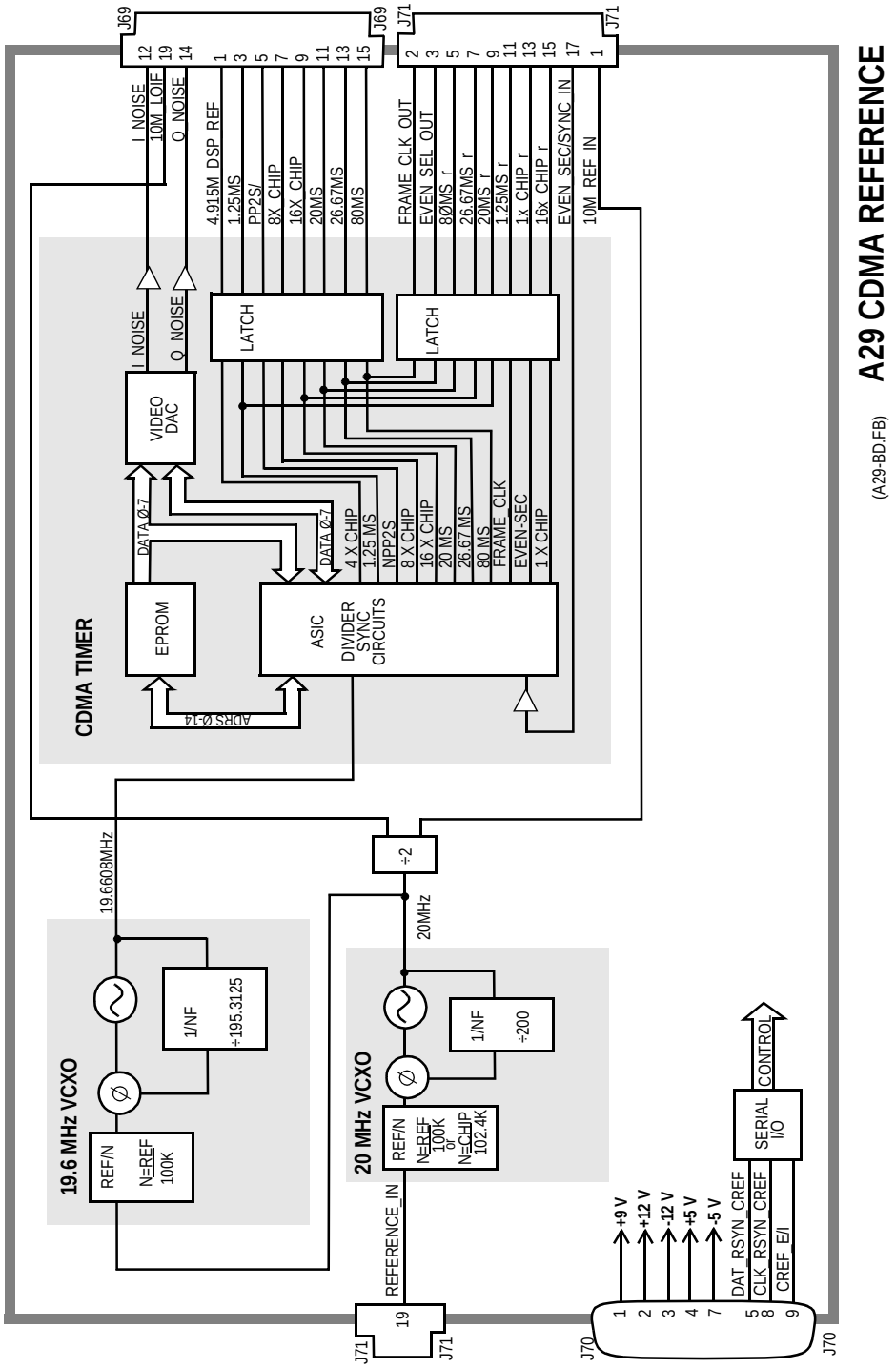

A28 Receiver Synthesizer
(A28-BD.FB)
To Receiver 1st Mixer (A19)
To/ From Serial I/O (A14)
J38
J39
RSYN_500_1000M
1500 MHz LPF
3 dB
13 dB
4 dB
7 dB
Tune Voltage
CLK_SA_RSYN
DAT_SA_RSYN
RSYN_E/I
Serial I/O Control
Control
Out-Of-Lock Detector
Loop Gain Control
Dividers ÷ 432,33,36,37
Digital Phase Detector
S C R
I/O Control
Fractional N Divide
fIN
fOUT
SWP
Phase Modulator
+40 V
+9 V
-9 V
+5 V
Filter
Reg/Filter
Reg/Filter
Filter
RCVR_SYN_REF_.2/1MHz
+5V
SWP_STRT
+40 V
+12 V
-12 V
+5 V
J40
J39
From Reference Assembly (A27)
From Measurement Assembly (A37)
From Filter Regulator (A20)

Table 100 Switch Control A28 Receiver Synthesizer

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	rsyn_gain _control	a		Note: Gain Control switches are set in either single position combinations according to receiver tuning frequency. Independent hexadecimal values are not applicable.
		open		
2	rsyn_gain _control	a		
		open		
3	rysn_gain _control	a		
		open		
4	rysn_gain _control	a		
		open		

Table 101 I/O Specs A28 Receiver Synthesizer

Connector	Name	Type	Range	
			Min	Max
J40-3	RCVR_SYN_REF_.2/1 MHz	Input	CMOS	CMOS
J39-6	SWP_STRT	Input	TTL	TTL
J38-3	RSYN_500_1000M	Output	–2 dBm	+2 dBm


A29 CDMA REFERENCE
(A29-BD.FB)
CDMA TIMER
EPROM
ASIC
DIVIDER
SYNC
CIRCUITS
VIDEO
DAC
LATCH
LATCH
I NOISE
Q NOISE
10M LOIF
4.915M DSP REF
1.25MS
PP2S/
8X CHIP
16X CHIP
20MS
26.67MS
80MS
FRAME CLK OUT
EVEN SEL OUT
80MS r
26.67MS r
20MS r
1.25MS r
1x CHIP r
16x CHIP r
EVEN SEC/SYNC IN
10M REF IN
DATA Ø-7
ADRS Ø-14
4 X CHIP
1.25 MS
NPP2S
8 X CHIP
16 X CHIP
20 MS
26.67 MS
80 MS
FRAME CLK
EVEN-SEC
1 X CHIP
÷2
19.6608MHz
20MHz
19.6 MHz VCXO
REF/N
N=REF 100K
1/NF
÷195.3125
20 MHz VCXO
REF/N
N=REF 100K or N=CHIP 102.4K
1/NF
÷200
REFERENCE_IN
SERIAL I/O
CONTROL
+9 V
+12 V
-12 V
+5 V
-5 V
DAT_RSYN_CREF
CLK_RSYN_CREF
CREF E/I
J69
J71
J70

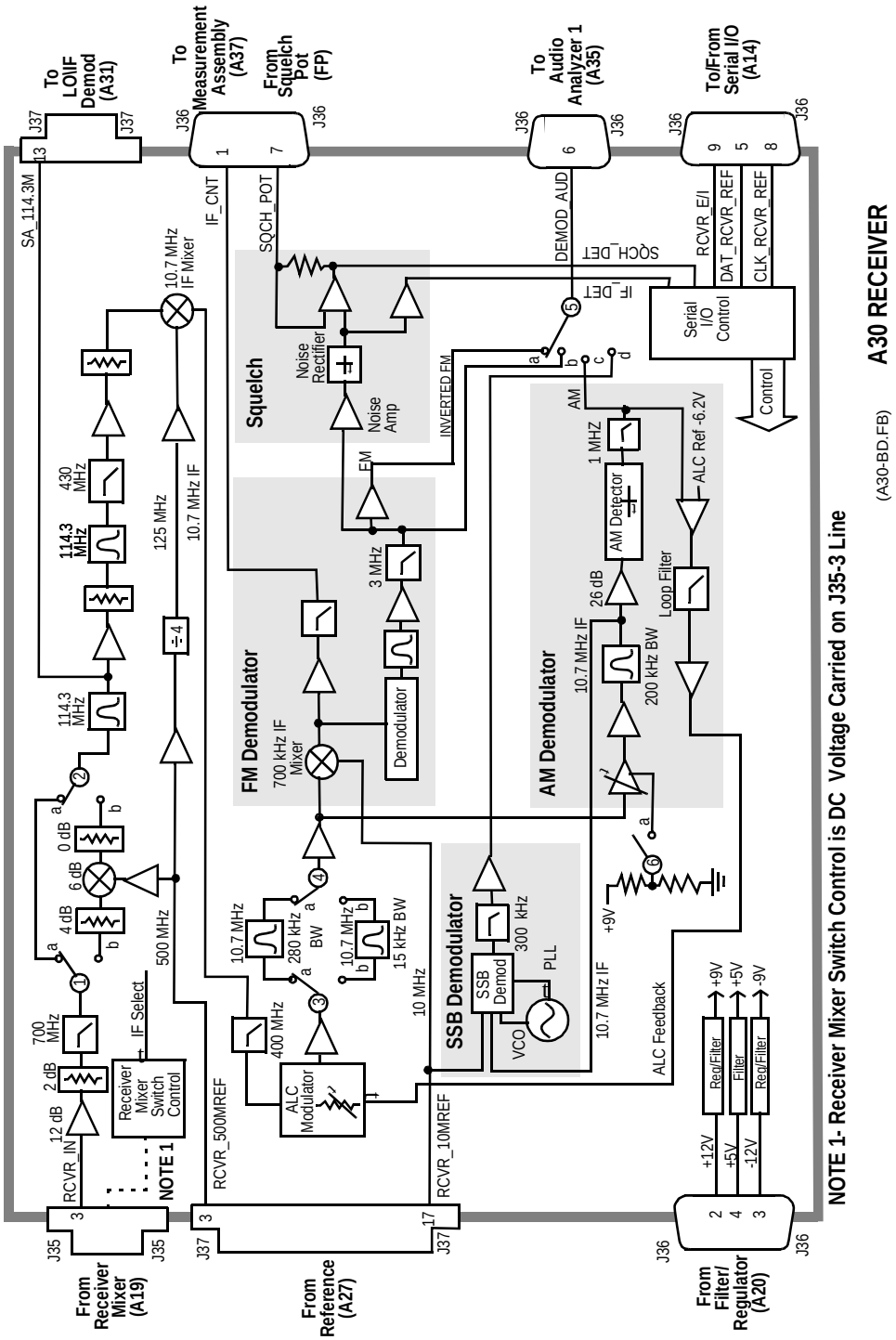
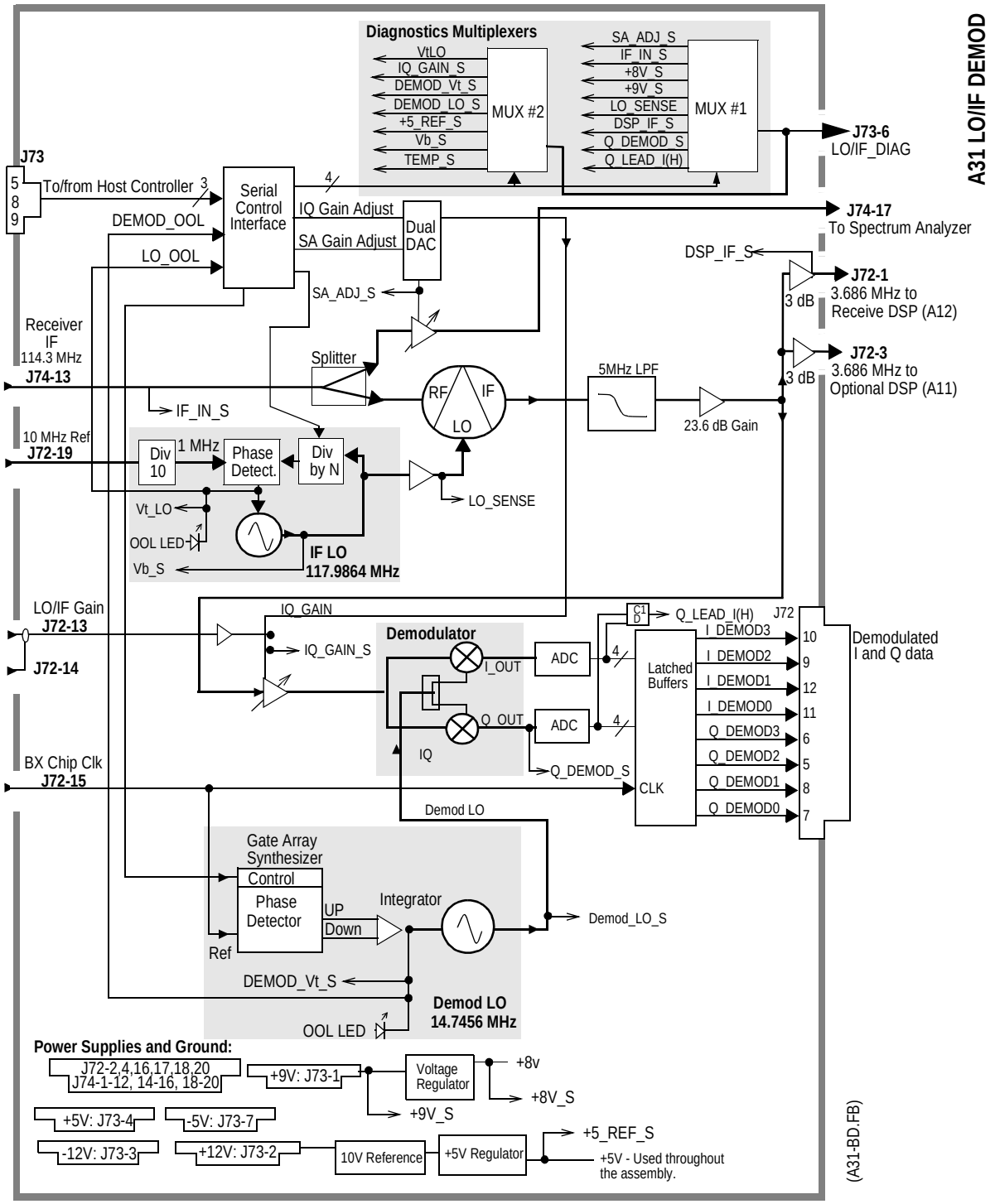

To LO/IF Demod (A31)
To Measurement Assembly (A37)
From Squelch Pot (FP)
To Audio Analyzer 1 (A35)
To/From Serial I/O (A14)
SA_114.3M
IF_CNT
SQCH_POT
DEMOD_AUD
SQCH_DET
IF_DET
RCVR_E/I
DAT_RCVR_REF
CLK_RCVR_REF
10.7 MHz IF Mixer
Squelch
Noise Rectifier
Noise Amp
INVERTED FM
FM
AM
Serial I/O Control
Control
ALC Ref -6.2V
1 MHZ
AM Detector
26 dB
Loop Filter
200 kHz BW
AM Demodulator
10.7 MHz IF
FM Demodulator
700 kHz IF Mixer
3 MHz
Demodulator
430 MHz
114.3 MHz
125 MHz
10.7 MHz IF
÷4
0 dB
6 dB
4 dB
2 dB
12 dB
RCVR_IN
700 MHz
IF Select
Receiver Mixer Switch Control
500 MHz
NOTE 1
10.7 MHz
280 kHz BW
15 kHz BW
400 MHz
ALC Modulator
10 MHz
SSB Demodulator
SSB Demod
300 kHz
PLL
VCO
+9V
ALC Feedback
Reg/Filter
Filter
Reg/Filter
+12V
+5V
-12V
+9V
+5V
-9V
RCVR_500MREF
RCVR_10MREF
From Receiver Mixer (A19)
From Reference (A27)
From Filter/ Regulator (A20)
NOTE 1- Receiver Mixer Switch Control is DC Voltage Carried on J35-3 Line
(A30-BD.FB)
A30 RECEIVER

Table 102 Switch Control A30 Receiver

Switch No.	Switch Name	Position	Hex Value	Instrument Setting
1	rcvr_if_path_select	a	2	RF Analyzer Tune Frequency 380.7 MHz
		b	1	RF Analyzer Tune Frequency <380.7 MHz
2	rcvr-if_path_select	a	2	RF Analyzer Tune Frequency ≥380.7 MHz
		b	1	RF Analyzer Tune Frequency <380.7 MHz
3	rcvr_if_filter_select	a	2	RF Analyzer IF Filter To 15 kHz
		b	1	RF Analyzer IF Filter to 230 kHz
4	rcvr_if_filter_select	a	2	RF Analyzer IF Filter to 15 kHz
		b	1	RF Analyzer IF Filter to 230 kHz
5	rcvr_demod_select	a	0	AF Analyzer AF Anl IN to FMD Demod, Tune Frequency >710 MHz
		b	1	AF Analyzer AF Anl IN to FM Deod, Tune Frequency <710 MHz
		c	2	AF Analyzer AF Anl IN to AM Demod
		d	3	AF Analyzer AF Anl IN to SSB Demod
6	rcvr_alc_select	a	1	AF Analyzer AF Anl IN to AM Demod
		open	0	AF Analyzer AF Anl IN to FM Demod

Table 103 I/O Specs A30 Receiver

Connector	Name	Type	Range	
			Min	Max
J35-3	RCVR_IN	Input	–37 dBm	–14 dBm
J37-3	RCVR_500MREF	Input	–2 dBm	+2 dBm
J37-17	RCVR_10MREF	Input	–12 dBm	– 8 dBm
J37-13	SA_114.3M	Output	109.3 MHz	119.3 MHz
				–12 dBm
J37-9	J-114.3M	Output	109.3 MHz	119.3 MHz
J36-6	DEMOD_AUD	Output		12 Vp


A31 LO/IF DEMOD
Diagnostics Multiplexers
VtLO
IQ_GAIN_S
DEMOD_Vt_S
DEMOD_LO_S
+5_REF_S
Vb_S
TEMP_S
MUX #2
SA_ADJ_S
IF_IN_S
+8V_S
+9V_S
LO_SENSE
DSP_IF_S
Q_DEMOD_S
Q_LEAD_I(H)
MUX #1
J73-6
LO/IF_DIAG
J73
5
8
9
To/from Host Controller
3
Serial Control Interface
4
IQ Gain Adjust
SA Gain Adjust
Dual DAC
J74-17
To Spectrum Analyzer
DEMOD_OOL
LO_OOL
SA_ADJ_S
DSP_IF_S
J72-1
3.686 MHz to Receive DSP (A12)
3 dB
Receiver IF
114.3 MHz
J74-13
Splitter
RF
IF
LO
5MHz LPF
3 dB
J72-3
3.686 MHz to Optional DSP (A11)
IF_IN_S
23.6 dB Gain
10 MHz Ref
J72-19
Div 10
1 MHz
Phase Detect.
Div by N
LO_SENSE
Vt_LO
OOL LED
IF LO
117.9864 MHz
Vb_S
LO/IF Gain
J72-13
J72-14
IQ_GAIN
IQ_GAIN_S
Demodulator
I_OUT
Q_OUT
IQ
ADC
ADC
4
4
C1
D
Q_LEAD_I(H)
J72
Latched Buffers
I_DEMOD3
I_DEMOD2
I_DEMOD1
I_DEMOD0
Q_DEMOD3
Q_DEMOD2
Q_DEMOD1
Q_DEMOD0
10
9
12
11
6
5
8
7
Demodulated I and Q data
BX Chip Clk
J72-15
Q_DEMOD_S
CLK
Demod LO
Gate Array Synthesizer
Control
Phase Detector
UP
Down
Integrator
Demod_LO_S
Ref
DEMOD_Vt_S
OOL LED
Demod LO
14.7456 MHz
Power Supplies and Ground:
J72-2,4,16,17,18,20
J74-1-12, 14-16, 18-20
+9V: J73-1
Voltage Regulator
+8v
+8V_S
+9V_S
+5V: J73-4
-5V: J73-7
-12V: J73-3
+12V: J73-2
10V Reference
+5V Regulator
+5_REF_S
+5V - Used throughout the assembly.
(A31-BD.FB)

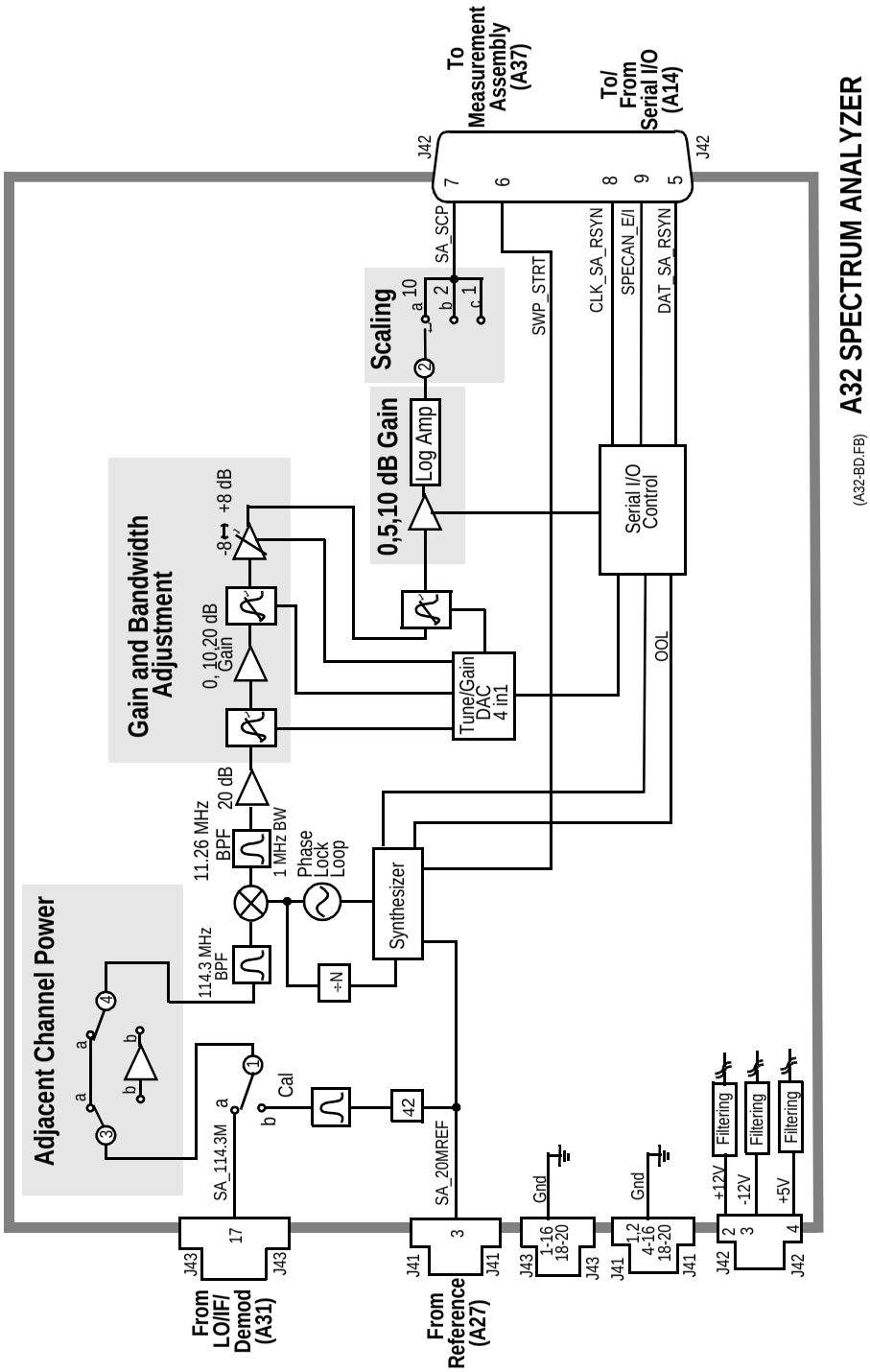
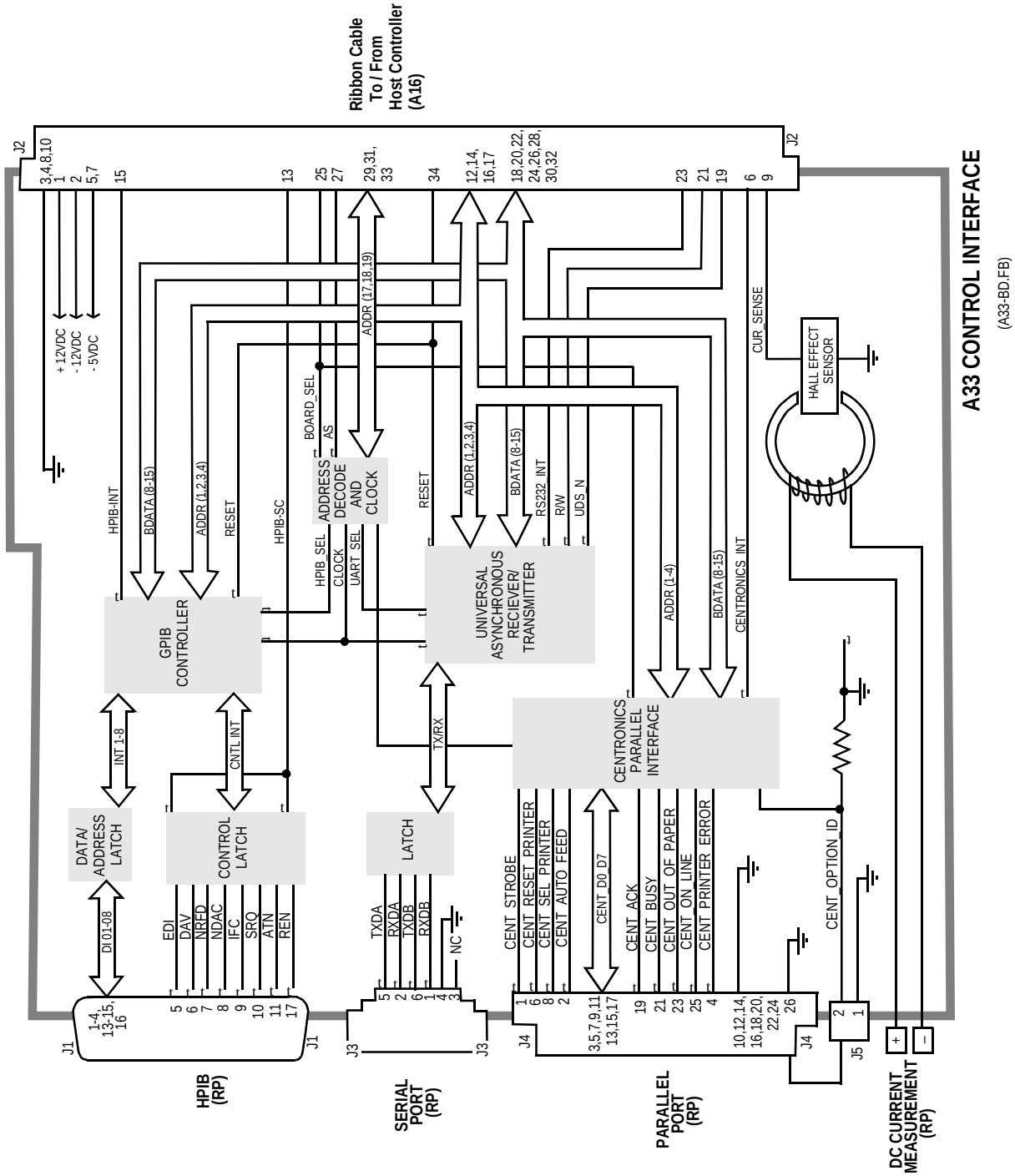

A32 SPECTRUM ANALYZER
(A32-BD.FB)
To Measurement Assembly (A37)
To/ From Serial I/O (A14)
J42
7
6
8
9
5
SA_SCP
SWP_STRT
CLK_SA_RSYN
SPECAN_E/I
DAT_SA_RSYN
Scaling
10
2
1
0,5,10 dB Gain
Log Amp
Serial I/O Control
Gain and Bandwidth Adjustment
+8 dB
-8
0, 10,20 dB Gain
Tune/Gain DAC 4 in1
OOL
20 dB
11.26 MHz BPF
1 MHz BW
Phase Lock Loop
Synthesizer
Adjacent Channel Power
114.3 MHz BPF
÷N
Cal
42
SA_114.3M
SA_20MREF
Gnd
Gnd
Filtering
Filtering
Filtering
+12V
-12V
+5V
From LO/IF/ Demod (A31)
From Reference (A27)
J43
17
J41
3
1-16
18-20
4-16
18-20
2
3
4

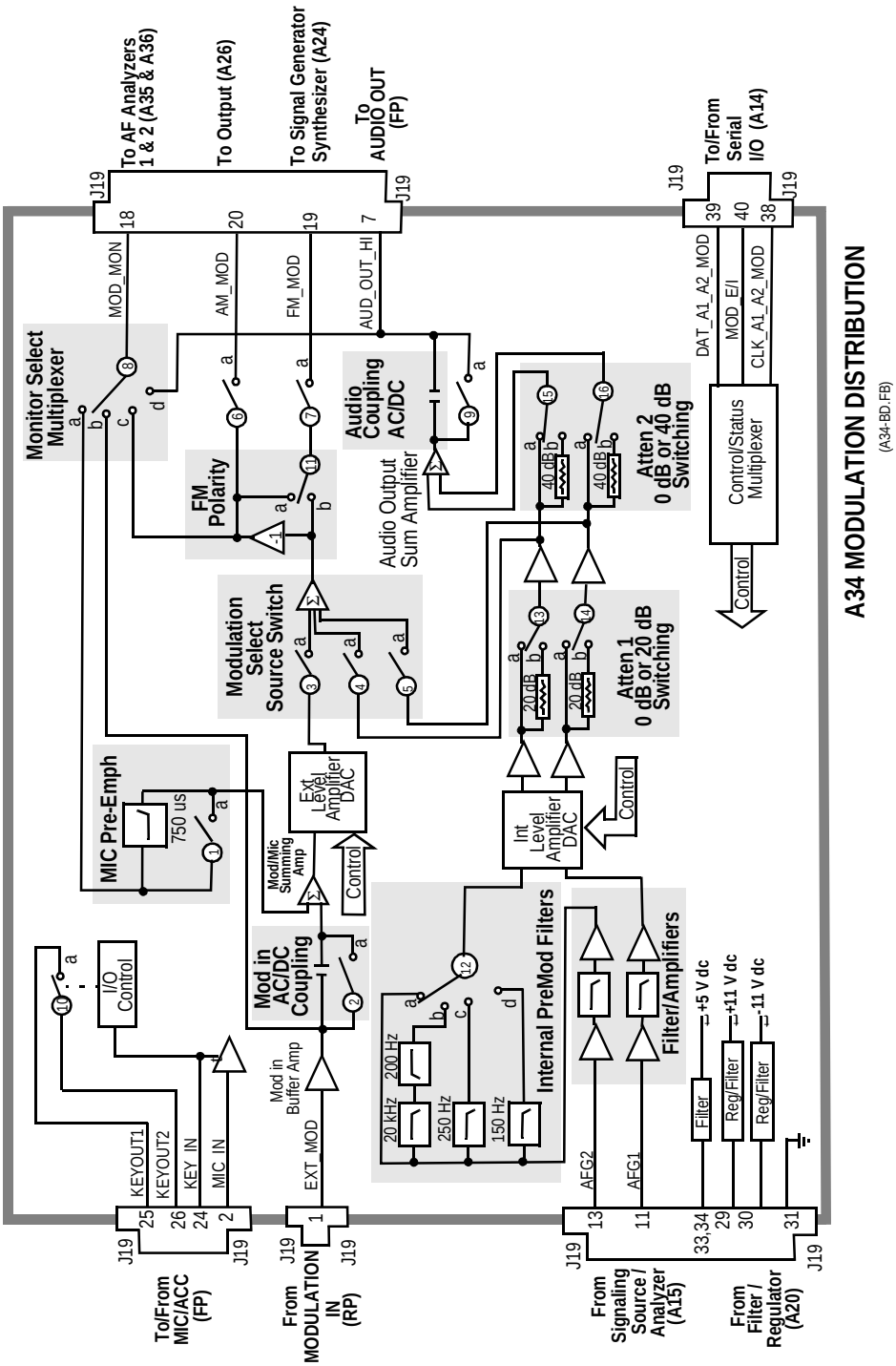
Table 104 Switch Control A32 Spectrum Analyzer

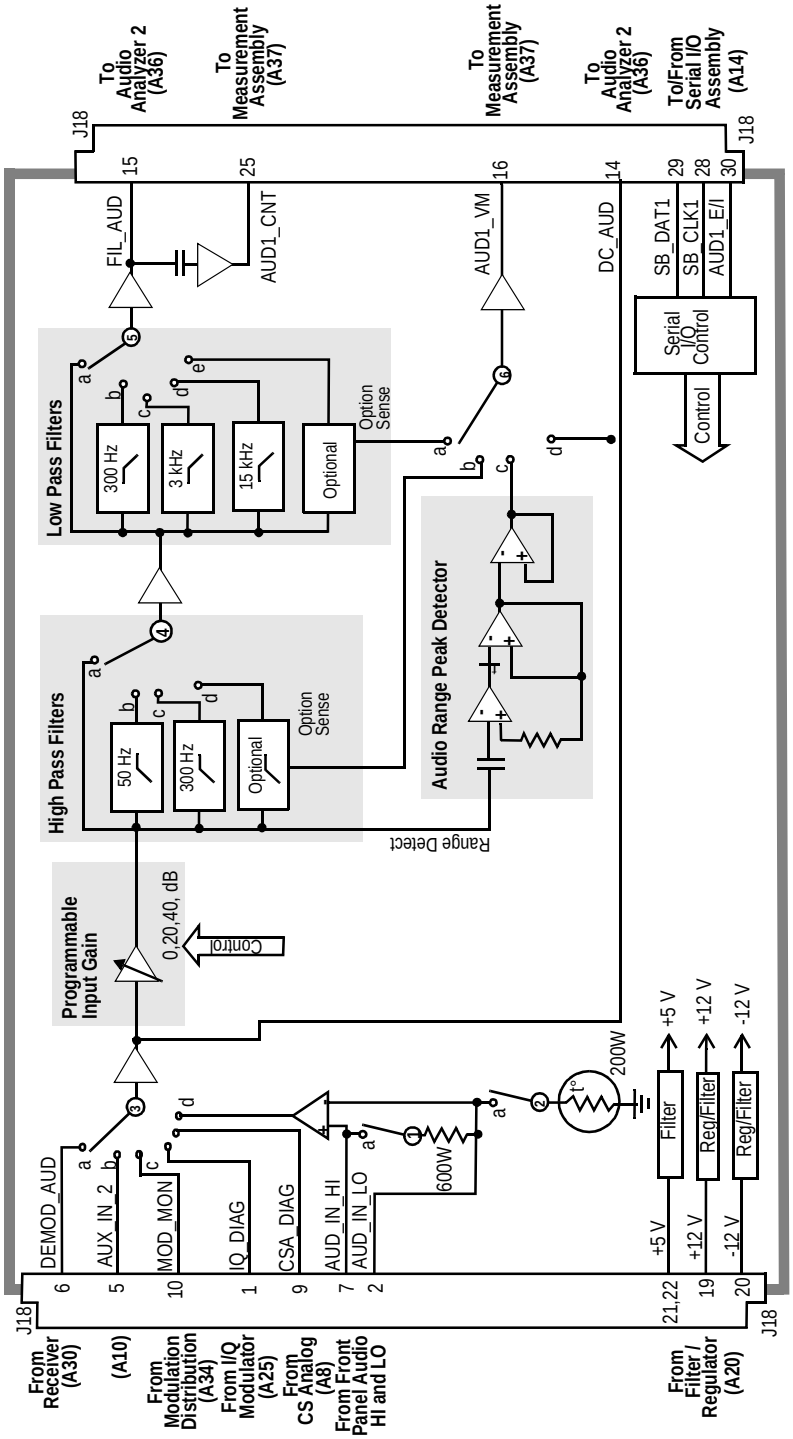
Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	spec_cal_switch	a	0	Normal Operation
		b	1	Position Active During-Calibration Cycle
2	spec_log_amp_path	a	6	Spectrum Analyzer Sensitivity 10 dB div
		b	5	Spectrum Analyzer Sensitivity 2 dB div
		c	3	Spectrum Analyzer Sensitivity 1 dB div

Table 105 I/O Secs A32 Spectrum Analyzer

Connector	Name	Type	Range	
			Min	Max
J43-17	SA_114.3M	Input		–12 dBm
J41-6	SA_20M REF	Input	>+3 dBm	


A33 CONTROL INTERFACE
(A33-BD.FB)
Ribbon Cable To / From Host Controller (A16)
J2
3,4,8,10
1
2
5,7
15
13
25
27
29,31, 33
34
12,14, 16,17
18,20,22, 24,26,28, 30,32
23
21
19
6
9
+ 12VDC
- 12VDC
- 5VDC
HPIB-INT
BDATA (8-15)
ADDR (1,2,3,4)
RESET
HPIB-SC
BOARD_SEL
AS
ADDR (17,18,19)
ADDRESS DECODE AND CLOCK
HPIB_SEL
CLOCK
UART SEL
RESET
ADDR (1,2,3,4)
BDATA (8-15)
RS232_INT
R/W
UDS_N
CUR_SENSE
HALL EFFECT SENSOR
GPIB CONTROLLER
UNIVERSAL ASYNCHRONOUS RECIEVER/ TRANSMITTER
CENTRONICS_INT
ADDR (1-4)
BDATA (8-15)
INT 1-8
CNTL INT
TX/RX
CENTRONICS PARALLEL INTERFACE
DATA/ ADDRESS LATCH
CONTROL LATCH
LATCH
DI 01-08
EDI
DAV
NRFD
NDAC
IFC
SRQ
ATN
REN
TXDA
RXDA
TXDB
RXDB
NC
CENT_STROBE
CENT_RESET PRINTER
CENT_SEL_PRINTER
CENT_AUTO FEED
CENT_D0..D7
CENT_ACK
CENT_BUSY
CENT_OUT_OF_PAPER
CENT_ON_LINE
CENT_PRINTER_ERROR
CENT_OPTION_ID
1-4, 13-15, 16
5
6
7
8
9
10
11
17
2
5
6
1
4
3
1
6
8
2
3,5,7,9,11 13,15,17
19
21
23
25
4
10,12,14, 16,18,20, 22,24
26
2
1
+
–
J1
J3
J4
J5
HPIB (RP)
SERIAL PORT (RP)
PARALLEL PORT (RP)
DC CURRENT MEASUREMENT (RP)


A34 MODULATION DISTRIBUTION
(A34-BD.FB)
To AF Analyzers 1 & 2 (A35 & A36)
To Output (A26)
To Signal Generator Synthesizer (A24)
To AUDIO OUT (FP)
To/From Serial I/O (A14)
MOD_MON
AM_MOD
FM_MOD
AUD_OUT_HI
DAT_A1_A2_MOD
MOD_E/I
CLK_A1_A2_MOD
Monitor Select Multiplexer
FM Polarity
Audio Coupling AC/DC
Audio Output Sum Amplifier
Atten 2 0 dB or 40 dB Switching
Control/Status Multiplexer
Control
Modulation Select Source Switch
Atten 1 0 dB or 20 dB Switching
MIC Pre-Emph
750 us
Ext Level Amplifier DAC
Mod/Mic Summing Amp
Int Level Amplifier DAC
Mod in AC/DC Coupling
Mod in Buffer Amp
Internal PreMod Filters
Filter/Amplifiers
I/O Control
KEYOUT1
KEYOUT2
KEY_IN
MIC_IN
EXT_MOD
AFG2
AFG1
20 kHz
200 Hz
250 Hz
150 Hz
Filter
Reg/Filter
Reg/Filter
+5 V dc
+11 V dc
-11 V dc
To/From MIC/ACC (FP)
From MODULATION IN (RP)
From Signaling Source / Analyzer (A15)
From Filter / Regulator (A20)



(A35-BD.FB) **A35 AUDIO ANALYZER 1**

Table 106 Switch Control A34 Modulation Distribution

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
1	dstr_pre_emphasis	a	1	RF Generator Mic Pre-Emp Off
		Open	0	RF Generator Mic Pre-Emp On
2	dstr_ext_mod_coupling	a	1	RF Generator FM Coupling DC
		open	0	RF Generator FM Coupling AC
3	dstr_ext_mod_to_mod	a	1	RF Generator Mod In to FM or AM
		open	0	RF Generator Mod In to Off
4	dstr_afg2_to_mod	a	0	RF Generator AFGen2 to On
		open	1	RF Generator AFGen2 to Off
5	dstr_afg1_to_mod	a	0	RF Generator AFGen1 to On
		open	1	RF Generator AFGen1 to Off
6	dstr_mod _destination	a	3	RF Generator AFGen1 to AM
		open	0	RF Generator AFGen1 to FM or Off
7	dstr_mod_destination	a	0	RF Generator AFGen2 to FM
		open	0	RF Generator AFGen2 to AM or Off
8	dstr_monitor_select	a	1	AF Analyzer AF Anl In to Mic Mod
		b	2	AF Analyzer AF Anl In to Ext
		c	3	AF Analyzer AF Anl In to FM Mod or AM Mod
		d	0	AF Analyzer AF Anl In to Audio Out
9	dstr_mod_coupling	a	1	RF Generator Audio Out to DC
		open	0	RF Generator Audio Out to AC
		open	0	TX Test Ext TX Key Off
10	dstr_xmtr_key	a	1	TX Test Ext TX Key On
		open	0	TX Test Ext TX Key Off

Table 106 Switch Control A34 Modulation Distribution (Continued)

Switch No.	Switch Name	Position	Hexadecimal Value	Instrument Setting
11	dstr_mod_polarity	a	1	RF Generator RF Gen Freq < 249 MHz
		0	0	RF Generator RF Gen Freq ≥ 249 MHz
12	dstr_premod_filter	a	0	Encoder Mode to Amps-Tacs, Channel to Voice
		b	1	Encoder Mode to Amps-Tacs, Channel to Cntl
		c	2	Encoder Mode to NAmps-NTacs, Channel to Voice
		d	3	Encoder Mode to LTR
13	dstr_afg2_1_atten	a	0	RF Generator AFGen2 to AM >10 or FM > 10 kHz
		b	1	RF Generator AFGen2 to AM≤10 or FM≤10 kHz
14	dstr_afg1_1_atten	a	0	RF Generator AFGen1 to AM >10 or FM > 10 Hz
		b	1	RF Generator AFGen1 to AM ≤10 or FM ≤10 kHz
15	dstr_afg2_2_atten	a	1	RF Generator AFGen2 to Audio Out >72 mV
		b	2	RF Generator AFGen2 to Audio Out≤72 mV
16	dstr_afg1_2_atten	a	1	RF Generator AFGen1 to Audio Out > 72 mV
		b	2	RF Generator AFGen2 to Audio Out ≤72 mV

Table 107 I/O Specs A34 Modulation Distribution

Connector	Name	Type	Range			Connector	Name	Type	Range	
			Min	Max					Min	Max
J19-2	MIC_IN	Input	0 Vp	10 Vp		J19-20	AM_MOD	Output	0 Vp	4 Vp
J19-1	EXT_MOD	Input	0 Vp	12 Vp		J19-19	FM_MOD	Output	0 Vp	4 Vp
J19-11	AFG1	Input	0 Vp	2.5 Vp		J19-7	AUD_OUT_HI	Output	0 Vrms	5 Vrms
J19-13	AFG2	Input	0 Vp	2.5 Vp		J19-38	AUD_OUT2	Output	0 Vrms	5 Vrms
J19-18	MOD_MON	Output	0 Vp	12 Vp						

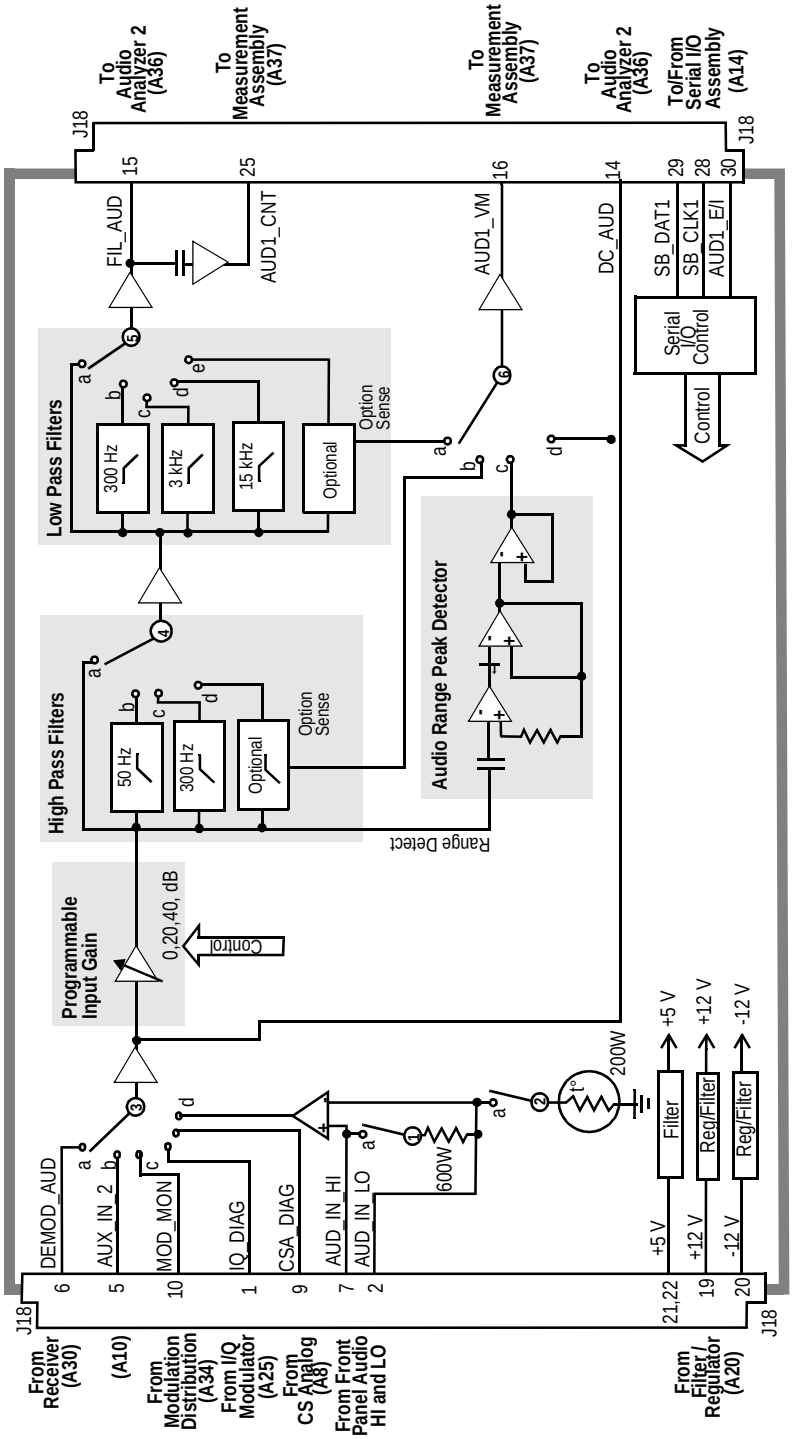

A35 AUDIO ANALYZER 1
(A35-BD.FB)
From Receiver (A30)
From Modulation Distribution (A34)
From I/Q Modulator (A25)
From CS Analog (A8)
From Front Panel Audio HI and LO
From Filter/ Regulator (A20)
To Audio Analyzer 2 (A36)
To Measurement Assembly (A37)
To Measurement Assembly (A37)
To Audio Analyzer 2 (A36)
To/From Serial I/O Assembly (A14)
J18
DEMOD_AUD
AUX_IN_2
MOD_MON
IQ_DIAG
CSA_DIAG
AUD_IN_HI
AUD_IN_LO
FIL_AUD
AUD1_CNT
AUD1_VM
DC_AUD
SB_DAT1
SB_CLK1
AUD1_E/I
Serial I/O Control
Control
Programmable Input Gain
0,20,40, dB
High Pass Filters
50 Hz
300 Hz
Optional
Option Sense
Low Pass Filters
300 Hz
3 kHz
15 kHz
Optional
Option Sense
Audio Range Peak Detector
Range Detect
600W
200W
Filter
Reg/Filter
Reg/Filter
+5 V
+12 V
-12 V

Table 108 Switch Control A35 Audio Analyzer 1

Switch No.	Switch Name	Position	Hex Value	Instrument Setting
1	aud1_input_impedance_switch	a	1	AF Analyzer Audio In Lo to 600 To Hi
		open	0	AF Analyzer Audio In Lo to GND or Float
2	aud1_input_float_gnd	a	1	AF Analyzer Audio In Lo to GND
		open	0	AF Analyzer Audio In Lo to Float or 600 To HI
3	aud1_input_select	a	0	AF Analyzer AF Anl In to FM Demod
		b	4	AF Analyzer AF Anl to Radio INT
		c	1	AF Analyzer AF Anl to EXT MOD
		d	2	AF Analyzer AF Anl to AUDIO IN
4	aud1_filter_1	a	0	AF Analyzer Filter 1 to <20 Hz HPF
		b	3	AF Analyzer Filter 1 to 50 Hz HPF
		c	1	AF Analyzer Filter 1 to 300 Hz HPF
		d	2	AF Analyzer Filter 1 to C-Message BPF
5	aud1_filter_2	a	1	AF Analyzer Filter 2 to >99 kHz LP
		b	0	AF Analyzer Filter 2 to 300 Hz LPF
		c	2	AF Analyzer Filter 2 to 3 kHz LPF
		d	3	AF Analyzer Filter 2 to 15 kHz LPF
		e	4	AF Analyzer Filter 2 to 6 kHz LPF
6	Voltmeter Connection	a		Service Screen Voltmeter to OPTION FILTER 2

Table 108 Switch Control A35 Audio Analyzer 1 (Continued)

Switch No.	Switch Name	Position	Hex Value	Instrument Setting
		b		Service Screen Voltmeter to OPTION FILTER1
		c		Service Screen Voltmeter to RANGE DETECT
		d		Service Screen Voltmeter to DC AUDIO

Table 109 I/O Specs A35 Audio Analyzer 1

Connector	Name	Type	Range	
			Min	Max
J18-6	DEMOD_AUD	Input	.02 kHz	75 kHz
				12 Vp
J18-5	AUX_IN_2	Input	.02 kHz	0.75 kHz
				12 Vp
J18-10	MOD_MON	Input	.02 kHz	75 kHz
				12 Vp
J18-1	AUD_IN_HI	Input	.02 kHz	75 kHz
				42 Vp
J18-2	AUD_IN_LO	Input	.02 kHz	75 kHz
J18-15	FIL_AUD	Output	–5 Vp	+5 Vp
J8-14	DC_AUD	Output	– 5 Vp	+5 Vp

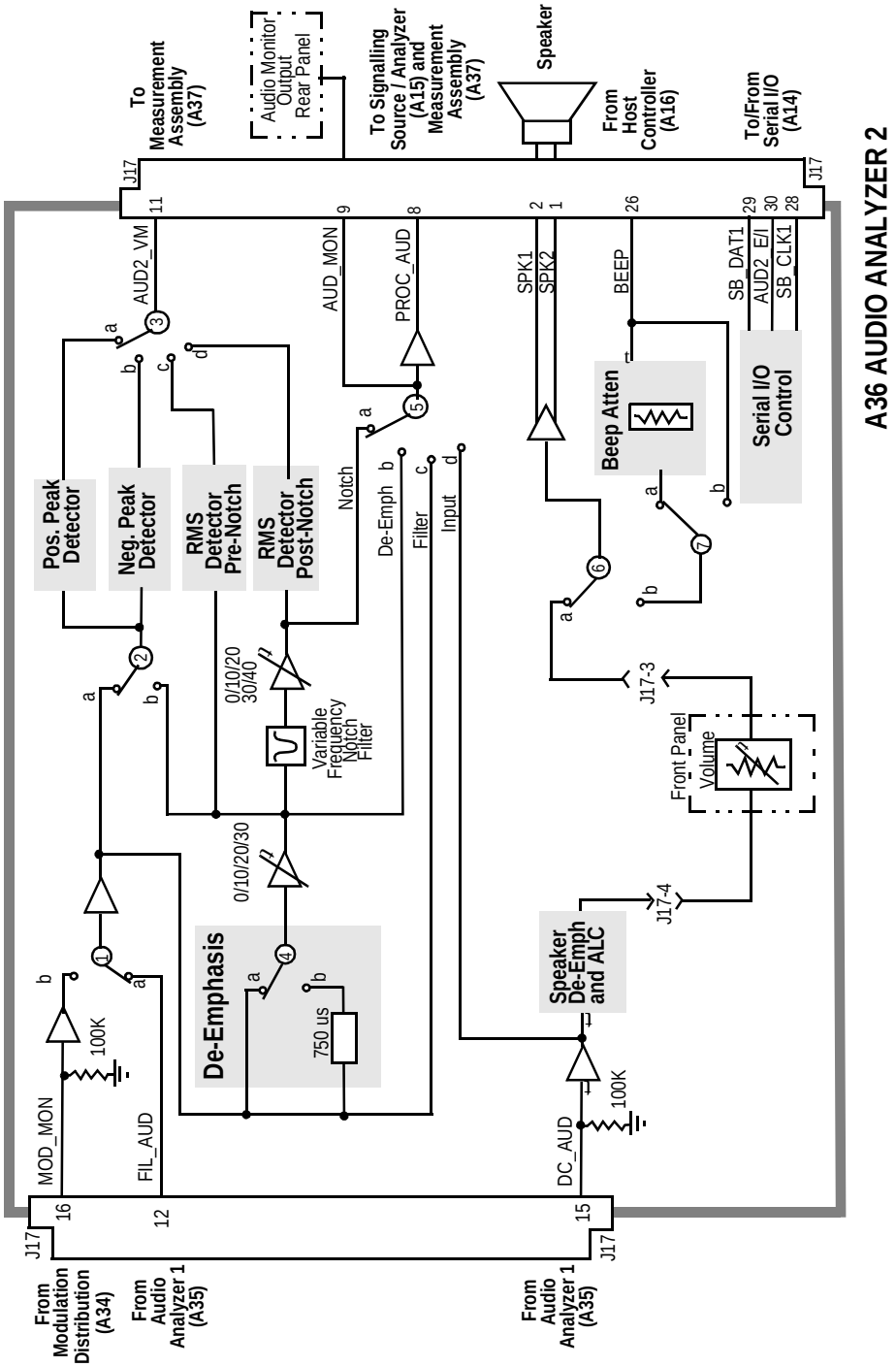
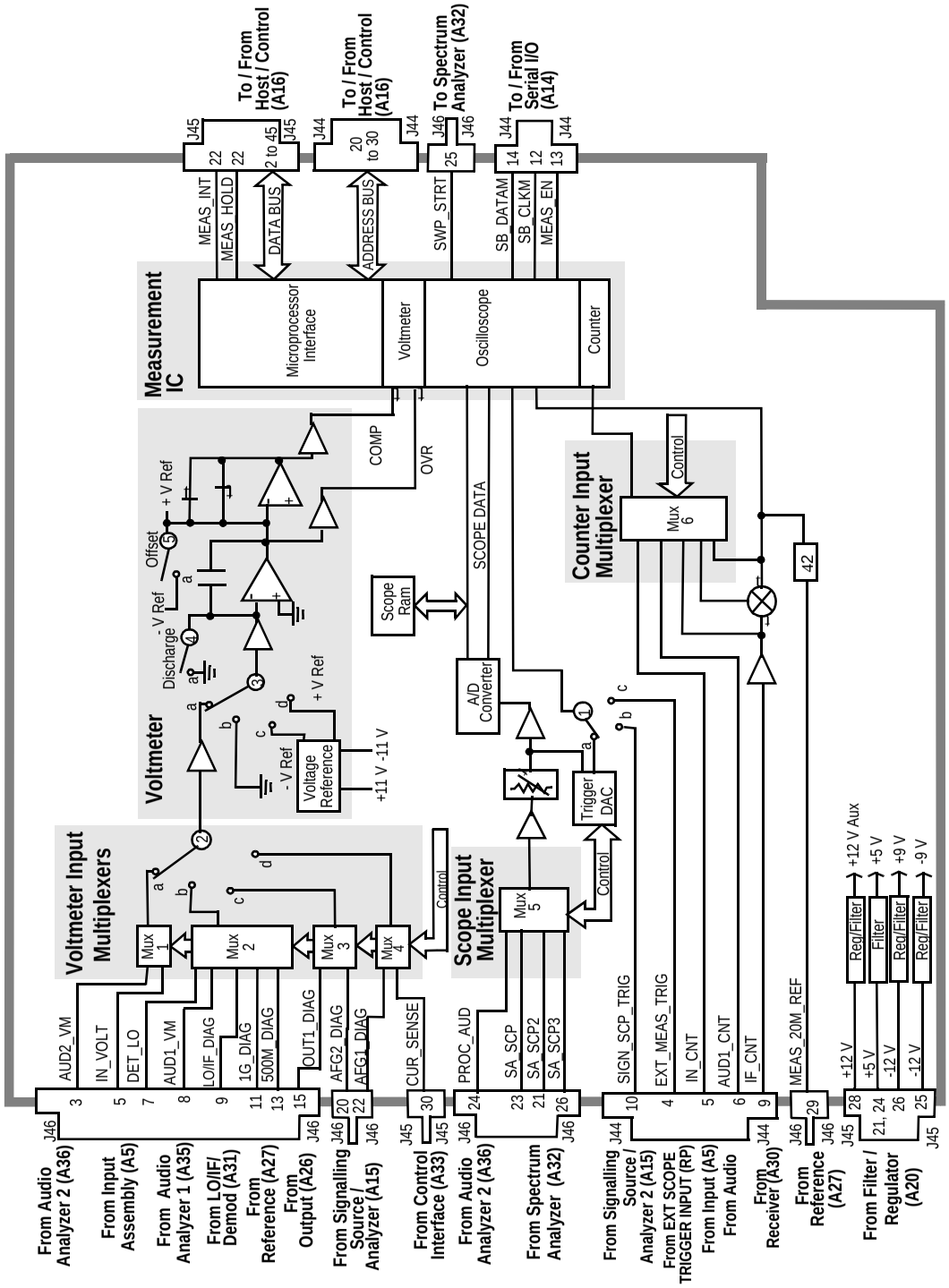

A36 AUDIO ANALYZER 2
To Measurement Assembly (A37)
Audio Monitor Output Rear Panel
To Signalling Source / Analyzer (A15) and Measurement Assembly (A37)
Speaker
From Host Controller (A16)
To/From Serial I/O (A14)
J17
AUD2_VM
AUD_MON
PROC_AUD
SPK1
SPK2
BEEP
SB_DAT1
AUD2 E/I
SB_CLK1
Pos. Peak Detector
Neg. Peak Detector
RMS Detector Pre-Notch
RMS Detector Post-Notch
Notch
De-Emph
Filter
Input
Beep Atten
Serial I/O Control
0/10/20 30/40
Variable Frequency Notch Filter
0/10/20/30
J17-3
J17-4
Front Panel Volume
De-Emphasis
750 us
Speaker De-Emph and ALC
100K
MOD_MON
FIL_AUD
DC_AUD
From Modulation Distribution (A34)
From Audio Analyzer 1 (A35)
From Audio Analyzer 1 (A35)

Table 110 Switch Control A36 Audio Analyzer 2

Switch No.	Switch Name	Position	Hex Value	Instrument Setting
1	aud2_input_select	a	0	Switched to under Normal Conditions
		b	1	Switched to under Diagnostic Test
2	aud2_pk_det_input	a	0	AF Analyzer PK Det to Filters
		b	1	AF Analyzers PK Det to De-Emp
3	aud2_vm_mux	a		Service Screen Voltmeter Connections to POS_PK_DET
		b		Service Screen Voltmeter Connection to NEG_PK_DET
		c		Service Screen Voltmeter Connection to PRE_NOTCH_RMS
		d		Service Screen Voltmeter Connection to POST_NOTCH_RMS
4	aud2_de_emphasis	a	0	AF Analyzer De-Emphasis to Off
		b	1	AF Analyzer De-Emphasis to 750 us
5	aud2_monitor_select	a	3	AF Analyzer Scope to Notch
		b	2	AF Analyzer Scope to De-Emph
		c	1	AF Analyzer Scope to Filter
		d	0	AF Analyzer Scope to Input
6	aud2_speaker_source	a	1	AF Analyzer Speaker Vol to Off
		b	0	AF Analyzer Speaker Vol to Pot
7	aud2_beep_volume	a	1	Configure Beeper to Quiet
		b	0	Configure Beeper to Loud

Table 111 I/O Specs A36 Audio Analyzer 2

Connector	Name	Type	Range	
			Min	Max
J17-16	MOD_MON	Input		100 kΩ
J17-12	FIL_AUD	Input	–5 Vp	+5 Vp
				1mΩ
J17-15	DC_AUD	Input	–5 Vp	+5 Vp
				100 k Ω
J17-11	AUD2_VM	Output	–5 V	+5 V
J17-1,2	SPK1, SPK2	Output		.25 Vp
J17-8	AUD_MON	Output	–5 V	+5 V
J17-9	PROC_AUD	Output	–5 V	+5 V


A37 MEASUREMENT
(A37-BD.FB)
To / From Host / Control (A16)
To / From Host / Control (A16)
To Spectrum Analyzer (A32)
To / From Serial I/O (A14)
MEAS_INT
MEAS_HOLD
DATA BUS
ADDRESS BUS
SWP_STRT
SB_DATAM
SB_CLKM
MEAS_EN
Measurement IC
Microprocessor Interface
Voltmeter
Oscilloscope
Counter
COMP
OVR
SCOPE DATA
Scope Ram
A/D Converter
Voltmeter
Offset
+ V Ref
- V Ref
Discharge
Voltage Reference
+11 V -11 V
Voltmeter Input Multiplexers
Mux 1
Mux 2
Mux 3
Mux 4
Control
Scope Input Multiplexer
Mux 5
Trigger DAC
Counter Input Multiplexer
Mux 6
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From Audio Analyzer 2 (A36)
From Input Assembly (A5)
From Audio Analyzer 1 (A35)
From LO/IF/ Demod (A31)
From Reference (A27)
From Output (A26)
From Signalling Source / Analyzer (A15)
From Control Interface (A33)
From Audio Analyzer 2 (A36)
From Spectrum Analyzer (A32)
From Signalling Source / Analyzer 2 (A15)
From EXT SCOPE TRIGGER INPUT (RP)
From Input (A5)
From Audio
From Receiver (A30)
From Reference (A27)
From Filter / Regulator (A20)
AUD2_VM
IN_VOLT
DET_LO
AUD1_VM
LO/IF_DIAG
1G_DIAG
500M_DIAG
OUT1_DIAG
AFG2_DIAG
AFG1_DIAG
CUR_SENSE
PROC_AUD
SA_SCP
SA_SCP2
SA_SCP3
SIGN_SCP_TRIG
EXT_MEAS_TRIG
IN_CNT
AUD1_CNT
IF_CNT
MEAS_20M_REF
+12 V
+5 V
-12 V
-12 V
Reg/Filter
Filter
Reg/Filter
Reg/Filter
+12 V Aux
+5 V
+9 V
-9 V

Table 112 Switch Control A37 Measurement

Switch No.	Switch Name	Position	Hex Value	Instrument Setting
1	meas_scope _trigger_sel	a	0	Oscilloscope Controls Trigger Internal
		b	1	Oscilloscope Controls to Trigger Encoder
		c	3	Oscilloscope Controls to Trigger EXT (TTL)
2	Voltmeter Connection	a		Service Screen Voltmeter Connection to POS_PK_DET
		b		Service Screen Voltmeter-Connection to REF_1GHz_DIAG
		c		Service Screen Voltmeter-Connection to AFG2_DIAG
		d		Service Screen Voltmeter-Connection to AFG1_DIAG
3	Voltmeter Connection	a		Service Screen Voltmeter Connection to Any Switch 2 Connect
		b		Service Screen Voltmeter-Connection to MEAS_SGND
		c		Done During Self Cal Every 3 Minutes
		d		Done During Self Cal Every 3 Minutes
4	Voltmeter Discharge Switch	a		Done After Every Measurement
		open		Normal Position

Table 112 Switch Control A37 Measurement (Continued)

Switch No.	Switch Name	Position	Hex Value	Instrument Setting
5	Voltmeter Offset Switch	a		Done during Self Cal Every 3Minutes
		open		Normal Position

Table 113 I/O Specs A37 Measurement

Connector	Name	Type	Range	
			Min	Max
J46-3,5,7	All Voltmeter	Input	–5 V	+5 V
J46-8,9,11	Inputs			
J46-13,15,20				
J46-22				
J45-27,30	All Voltmeter	Input	–5 V	+5 V
	Inputs			
J46-21,23	All Scope	Input	None	10V
J46-24,26	Inputs			
J44-5	IN_CNT	Input	100 mVp	
J44-6	AUD1_CNT	Input	100 mVp	
J44-9	IF_CNT	Input	100 mVp	
J46-29	MEAS_20m_REF	Input	>+5 dBm	
J44-10	SIGN_SCP_TRIG	Input	100 mVp	
J44-4	EXT_TRIG	Input	2.5 Vp	20 Vp

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HP 8924C Replaceable Parts

In the U.S. you can order replacement parts by phone. There are two ways to do this. If your Test Set is under warranty you can use the Self-Support program to obtain replacement parts. The other method is to order the part directly. Outside the U.S. contact your local Hewlett-Packard Sales and Service office.

General Information about Replaceable Parts

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For U.S. customers that wish to repair their own Test Sets, a special toll-free number (1 800 827 3848) is now available for hardware troubleshooting assistance. This is a special service specifically designed for Hewlett-Packard customers that repair their own Test Sets. For a Test Set under warranty, there is no charge for troubleshooting assistance, and repair parts covered under warranty will be sent directly to the customer. If the Test Set is out of warranty, there will be a charge for parts.

Direct Parts Ordering

Call Hewlett-Packard parts specialists at 1 800 227 8164. They can help you identify parts and can also take your order.

Assembly Replacements

With some assemblies you will receive a Memory Card that contains factory-generated calibration data for that assembly. There will also be an instruction sheet for loading the calibration data into your Test Set after you've replaced the assembly.

A table, *Relating Assemblies To Troubleshooting Aids*, at the beginning of chapter 3 - *Repair* shows which assemblies need calibration data as well as which performance tests and periodic self-calibration adjustments are recommended after replacing an assembly.

NOTE: Refer to illustrations in Chapter 3, Repair for part identification.

Replaceable Parts Listing

Item	Description	Part Number
A1	BD AY KEY	08924-60110
A2	BD AY FRNT PNL FLTR	08924-60115
A3	CRT DISPLAY AY	08920-61005
A5	INPUT W/ATTEN KIT	08924-61813
A6	PROTOCOL PROC KIT	08924-61809
A7	C-SITE DIGITAL KIT	08924-61802
A8	C-SITE ANALOG KIT	08924-61807
A12	AUX/MAIN DSP REC KIT	08924-61812
A14	SERIAL I/O KIT	08924-61808
A15	NEW SIG/SCE #004 KIT	08920-61850
A16	KIT-CONTROLLER	08920-61872
A17	KIT-MEM W/PCMCIA	08920-61871
A19	RECEIVER MIXER KIT	08920-61832
A20	N REG/FLTR	08924-61814
A21	FAN ASSY	08924-61038
A22	NEW DISPLAY PROC KIT	08920-61824
A23	POWER SUPPLY	0950-2952
A24	NEW SIGGEN SYNTH	08921-61819
A25	I/Q MOD KIT	08924-61806
A26	NEW RF OUT KIT	08924-61815
A27	NEW REFERENCE KIT	08920-61829
A28	NEW RCVR SYNTH	08921-61820
A29	CDMA REF KIT	08924-61804

A30	NEW RECEIVER KIT	08920-61828
A31	CDMA LO/IF DEMOD KIT	08924-61805
A32	SPECTRUM ANAL #002/102	08920-61852
A33	HPIB CENT/SENSE KIT	08920-61818
A34	NEW MOD DIST KIT	08920-61809
A35	NEW AUDIO ANALYZER #1 KIT	08920-61811
A35A1	6KHZ BP FLT #014	08920-61063
A35A2	CCITT FLTR #011	08920-61055
A35A2	C-MESS FLTR #013	08920-61056
A36	NEW AUDIO 2 KIT	08920-61853
A37	MEASUREMENT KIT	08920-61836
A38	OSC XTAL	1813-0644
A39	37 PIN FILTER KIT	08924-61811
A40	MTHR BD KIT	08924-61801
A41	FRONT PANEL ASSY	08924-61002
ACC-1	FW REPLMT KIT	08924-61810
ACC-2	USERS GUIDE	08924-90008
ACC-3	BD AY RF EXTDR	08924-60109
J1	ADPT F N F SMA	1250-1811
J2	ADPT F SMA F SMA	1250-1666
J3	ADPT M BNC F BNC	1250-1499
J4,J5	JMPR CONN 1 PR	1258-0209
J6-18	CONN RF F BNC RA	1250-1842
MP1	PANEL DRESS	08924-00050
MP2	FRAME-FRONT MACH	08924-21001
MP3	KEYPAD	08924-40001
MP4	BRKT CONN MOUNT	08920-00005

MP5	BRACKET-CRT	08924-00003
MP6	CLIP-WINDOW	08922-00056
MP7	CRT WINDOW	08920-21023
MP8	BEZEL-CARD	08920-40028
MP9	WASH LOCK .50ID	2190-0068
MP10	NUT HEX 1/2-28	2950-0054
MP11	RFI GASKET	5001-5527
MP12	KEY CAP	5041-3621
MP13	KNOB BASE.250 JG	0370-2110
MP14	CLAMP-CABLE	1400-1391
MP15	SMM3.0 8SEMPNTX	0515-0372
MP16	NUT HEX 1/4-36	2950-0196
MP17	KNOB CONC BASE	0370-3079
MP18	CABLE TIE	1400-0249
MP19	NUT-HEX 15/32-32	2950-0035
MP23	SMM2.5 6PCHPNTX	0515-1940
MP24	SMM3.0 6SEMPNTX	0515-2126
MP25	CHASSIS ASSY	08924-61001
MP26	COVER PWR SPLY	08924-00023
MP27	REAR PANEL	08924-00008
MP28	BRKT MEM BOARD	08924-00043
MP29	LBL BLK SERIAL	5180-1871
MP30	SMM4.0 8 PN TX	0515-1142
MP31	M4X.7 10MM PN-HD	0515-1993
MP32	WSHR LK .1941D	2190-0577
MP33	WSHR LK .472ID	2190-0102
MP34	SMM3.0 14 FL TX	0515-1032

MP35	SMM4.0 6MML PNTX	0515-2143
MP36	LBL WARNING	08590-80007
MP37	SHIELD - CRT	08922-00096
MP38	SMM4.0 10SEMPNTX	0515-0380
MP39	SMM4.0 20MML	0515-0456
MP40	NAMEPLATE	08924-00002
MP41	BEZEL-CRT	08922-40001
MP42	STDF .327L 6-32	0380-0644
MP43	CONN SCREWLOCK F	0380-2079
MP44	CVR INSTRMT	08924-00046
MP45	HOLDDOWN PCB	08924-00026
MP46	RFI STRP-FINGER	8160-0857
MP47	BUMPER RR LEFT	08924-21002
MP48	WSHR-LK HLCL #4	2190-0003
MP49	TRIM,SIDE, 177H	5001-0540
MP50	FOOT FULL MOD	5041-8801
MP51	TRIM,TOP,FM	5041-8802
MP52	CAP,HDL RTR,FRNT	5041-8819
MP53	STRAP HDL AY574D	5062-3705
MP54	COVER AIR, DGTL	08924-00004
MP55	COVER - ANALOG	08924-00007
MP56	TOOL - REMOVAL	08924-00021
MP57	RFI ROUND STRIP	8160-0551
MP58	RIVET-PLASTIC SNAPIN	0361-1620
MP59	SMM4.0 8 PN TX	0515-0433
MP60	SMM4.0 10SEMPNTX	0515-0380
MP61	BD AY MOTHER	08924-60101

MP62	NUT-KNURL 1/2-28	0590-1611
W1	HARN SPEAKER AY	08924-61007
W3,W7	CA CX A23A23 275	8120-5731
W4	HARNESS- PWR SUP	08924-61008
W5	RBN-CBL ASSY	08924-61018
W6	CBL AY CRT	08920-61020
W8	CA ASSY 11-COND	08924-61009
W9	HARN PWR SPLY 18	08924-61019
W10	SR-2.18 SMA-SMA	08924-61015
W11	CA CX A04A06 400	8120-5845
W12	RBN 26CNDCT28AWG	08920-61146
W13	RIB CBL 34 COND	08924-61010
W14	CA F SMB-SMB 205	08924-61033
W15	CBL AY TIMEBASE	08924-61011
W16	CA-COAX SMB-SMC	08924-61026
W17	CA - RBN 20 COND	08924-61013
W18	CA MCNDCT RJ11SP	08924-61031
W19	RBN 26CNDCT28AWG	08924-61034
W20	RBN 26CNDCT28AWG	08924-61035
W21-22	CA CX A06A23 250	8120-6263
W23	SR 2.18 RF, LUFF	08924-61016
W24	CBL ADAPTER	08924-61044
W27,W28,W29	CBL COAX	8120-5805
----	RACK MOUNT KIT	5062-3978

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HP 8924E Replaceable Parts

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NOTE: Refer to illustrations in Chapter 3, Repair for part identification.

Replaceable Parts Listing

Item	Description	Part Number
A1	BD AY KEY	08924-60110
A2	BD AY FRNT PNL FLTR	08924-60115
A3	DISPLAY AY A22	08920-61005
A5,A4	INPUT W/ATTEN KIT	08924-61813
A5J1,A5J2	CONN-RF BNC INST	1250-2659
A6	PROTOCOL PROC 24E KIT	08924-61827
A7	C-SITE DIG #2 24E KIT	08924-61822
A8	C-SITE ANLG 24E KIT	08924-61821
A9	C-SITE DIG #1 24E KIT	08924-61823
A12	AUX/MAIN DSP REC KIT	08924-61812
A14	SERIAL I/O KIT	08924-61808
A15	SIGNAL SOURCE KIT	08920-61850
A16	CPU 24E KIT	08924-61826
A17	KIT-MEM W/PCMCIA	08920-61871
A19	RECEIVER MIXER KIT	08920-61832
A20	REG/FLTR	08924-61814
A21	FAN ASSY	08924-61038
A22	NEW DISPLAY PROC KIT	08920-61824
A23	POWER SUPPLY	0950-2952
A24	SIGGEN SYNTH KIT	08921-61819
A25	I/Q MOD KIT	08924-61806
A26	RF OUT KIT	08924-61815
A27	REFERENCE KIT	08920-61829

A28	RCVR SYNTH KIT	08921-61820
A29	CDMA REF KIT	08924-61804
A30	RECEIVER KIT	08920-61828
A31	CDMA LO/IF DEMOD KIT	08924-61805
A32	MOD AY TERM	08920-61040
A32	SPECTRUM ANALYZER KIT	08920-61852
A33	HPIB CENT/SENSE KIT	08920-61818
A34	MOD DISTRIBUTION KIT	08920-61809
A35	AUDIO ANALYZER #1 KIT	08920-61811
A35A1	6KHZ BP FLT	08920-61063
A35A2	CCITT FLTR #011	08920-61055
A35A2	C-MESS FLTR	08920-61056
A36	AUDIO ANALYZER 2 KIT	08920-61853
A37	MEASUREMENT KIT	08920-61836
A38	OSC XTAL	1813-0644
A39	37 PIN FILTER KIT	08924-61811
A40	MTHR BD 24E KIT	08924-61820
A41	FRNT PNL 24E KIT	08924-61825
A42	BNC ADPT 24E KIT	08924-61824
ACC-1	FW REPL 24E KIT	08924-61858
ACC-2	USERS GUIDE	08924-90057
ACC-3	BD AY RF EXTDR	08924-60109
ACC-4	QUICK REF GUIDE	08924-90058
ACC-8	RACKMOUNT KIT	5062-3978
J1	ADPTR-COAX SMA-N	1250-2621
J2	ADPT F SMA F SMA	1250-1666
J3	ADPT M BNC F BNC	1250-1499

J4,J5	JMPR CONN 1 PR	1258-0209
J6,J10,J14,J15,J16,J17	CONN RF F BNC RA	1250-1842
MP5	BRACKET-CRT	08924-00003
MP6	CLIP-WINDOW	08924-00048
MP7	CRT WINDOW	08920-21023
MP8	BEZEL-CARD	08920-40028
MP9	WASH LOCK .50ID	2190-0068
MP3	KEYPAD-24E	08924-40003
MP4	BRKT CONN MOUNT	08920-00005
MP10	NUT HEX 1/2-28	2950-0054
MP11	RFI GASKET	5001-5527
MP12	KEY CAP	5041-3621
MP13	KNOB BASE.250 JG	0370-2110
MP14	CLAMP-CABLE	1400-1391
MP15	SMM3.0 8SEMPNTX	0515-0372
MP16	NUT HEX 1/4-36	2950-0196
MP17	KNOB CONC BASE	0370-3079
MP18	CABLE TIE	1400-0249
MP19	NUT-HEX 15/32-32	2950-0035
MP24	SMM3.0 6SEMPNTX	0515-2126
MP25	CHASSIS AY 24E	08924-61052
MP26	COVER PWR SPLY	08924-00023
MP27	REAR PANEL-24E	08924-00055
MP28	BRKT MEM BOARD	08924-00043
MP30	SMM4.0 8 PN TX	0515-1142
MP31	SMM4.0 10 ST PN	0515-1993
MP32	WSHR LK .1941D	2190-0577

MP33	WSHR LK .472ID	2190-0102
MP34	SMM3.0 14 FL TX	0515-1032
MP35	SMM4.0 6MML PNTX	0515-2143
MP36	LBL WARNING	08590-80007
MP37	SHIELD - CRT	08922-00096
MP38	SMM4.0 10SEMPNTX	0515-0380
MP39	SMM4.0 20MML	0515-0456
MP40	NAMEPLATE -24E	08924-00058
MP41	BEZEL-CRT	08922-40001
MP42	STDF .327L 6-32	0380-0644
MP43	CONN SCREWLOCK F	0380-2079
MP44	COVER INSTRUMENT	08924-00046
MP45	HOLDDOWN PCB	08924-00026
MP46	RFI STRP-FINGER	8160-0857
MP47	BUMPER REAR	08924-40002
MP48	WSHR-LK HLCL #4	2190-0003
MP49	TRIM,SIDE, 177H	5001-0540
MP50	FOOT FULL MOD	5041-8801
MP51	TRIM,TOP,FM	5041-8802
MP52	CAP,HDL RTR,FRNT	5041-8819
MP53	STRAP HDL AY574D	5062-3705
MP54	COVER AIR, DGTL	08924-00004
MP55	COVER - ANALOG	08924-00007
MP56	TOOL - REMOVAL	08924-00021
MP57	RFI ROUND STRIP	8160-0551
MP58	RIVET-PLASTIC SNAPIN	0361-1620
MP59	SMM4.0 8 PN TX	0515-0433

MP60	SCREW M4 THD FORM	0515-2787
W1	HARN SPEAKER AY	08924-61007
W3,W7	CA CX A23A23 275	8120-5731
W4	HARNESS- PWR SUP	08924-61008
W5	RBN-CBL ASSY	08924-61018
W6	CBL AY CRT	08920-61020
W8	CA ASSY 11-COND	08924-61009
W9	HARN PWR SPLY 18	08924-61019
W10	SR-2.18 SMA-SMA	08924-61015
W11	CA CX A04A06 400	8120-5845
W12	RBN 26CNDCT28AWG	08920-61146
W13	RIB CBL 34 COND	08924-61010
W14	CA F SMB-SMB 205	08924-61033
W15	CBL AY TIMEBASE	08924-61011
W16	CA-COAX SMB-SMC	08924-61026
W17	CA - RBN 20 COND	08924-61013
W18	CA MCNDCT RJ11SP	08924-61031
W19	RBN 26CNDCT28AWG	08924-61034
W20	RBN 26CNDCT28AWG	08924-61035
W21,W22	CA CX A06A23 250	8120-6263
W23	SR 2.18 RF, LUFF	08924-61016
W24	CBL ADAPTER	08924-61044
W27,W28,W29	CBL COAX	8120-5805
W30	CBL RBN 20COND	08924-61050
W31	CBL RBN 28AWG	08924-61051

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Diagnostics Descriptions

This chapter explains what the each of the diagnostic routines do. These include:

- Power-up Self-Test Diagnostic
- Audio Frequency Diagnostics (AFDIAGS3)
- RF Functional Diagnostics (RFDIAGS3)
- Miscellaneous Functional Diagnostics (MSDIAGS3)
- CDMA Digital Functional Diagnostics (CDMADIAG)

Use this information when your diagnosis is ambiguous, or when you want further confirmation of your diagnosis before ordering replacement assemblies.

To run the Diagnostics follow the procedures in **chapter 2, "Troubleshooting"**.

For more information, read the block-diagram theory of operation that applies to the Functional Diagnostic you are running. Additional theory of operation is in **chapter 11, "Block Diagrams"**.

Description Of Self-Test Diagnostic

Introduction

The Self-Test Diagnostic can be run three ways:

1. The test runs automatically when the Test Set is turned on. After the Test Set powers up, a message appears at the top of the display. If one or more tests fail, the message reports the failure with a hexadecimal code.

   During the test, coded failure information is displayed on four LEDs on the top of the Host Controller (A16) assembly. The Test Set's cover must be removed to view these LEDs. See **chapter 3, "Repair"** for instructions on removing the Test Set's cover.

2. The test runs when the Test Set receives the query **`*TST?`** over HP-IB. The resultant decimal code can be read over the bus.

3. The test runs when Miscellaneous Diagnostics (MSDIAGS3) are run and the **`Self Test`** is selected.

Reading Self-Test Diagnostic Failure Codes From the Front Panel or HP-IB

The failure codes are listed in **table 114 on page 542**. If more than one failure occurs, the failure code will be the sum of the individual failure codes. The nature of the failure and the assembly most-likely at fault is also listed.

Table 114 Returned Values for Self-Test Diagnostic Failures

Detected Failure Failed Assembly		Returned Error code	
		Hexadecimal (displayed)	Decimal (HP-IB)
Microprocessor	A16 Controller	0002	2
ROM	A16 Controller	0004	4
RAM	A17 Memory	0008	8
RAM	A17 Memory	0010	16
Timer	A16 Controller	0020	32
Real-Time Clock	A17 Memory	0040	64
Keyboard (stuck key)	A1 Keyboard [a]	0080	128
RS-232 I/O	A33 HP-IB/RS-232/Current Sense	0100	256
Serial Bus Communication	Any Non-Optional assembly [b]	0200	512
Signaling Board Self-Test	A15 Signaling Source/Analyzer	0400	1024
CRT Controller Self-Test	A22 CRT Drive	0800	2048
Miscellaneous Hardware	Several Possible Assemblies [c]	1000	4096

a. Could also be the A16 Controller with a faulty key-down detector.
b. This checks the ability of the Controller to communicate with any hardware on the bus.
c. This message occurs if expected hardware is absent or non-responding to the Controller.

Reading LED Codes

When the Self-Test Diagnostic reports a failure, more information about the failure may be available inside the Test Set. This additional information is output to the four LEDs on the top of the A16 Host Controller assembly. The failure codes are layered, that is, sent out as code sequences. **Figure 49, "Reading the Self-Test Diagnostic Using the Internal LEDs," on page 544** and the tables following it document some of the more useful code sequences. You may need to run the Self-Test Diagnostic several times to figure out a particular LED sequence.

NOTE: The LEDs output Self-Test Diagnostic codes only when the Test Set is powering up. The LEDs remain off when the Self-Test Diagnostic is initiated through programming or by running the Miscellaneous Diagnostics. To read the LED codes, the Test Set's cover must be removed.

If the Test Set has no faults that can be detected by the Self-Test Diagnostic, the four LEDs on the Controller assembly will light and remain on for about ten seconds. During that period, a short beep will be heard. Then the LEDs will extinguish and remain off.

If a fault is detected during the test:

1. The four LEDs will go on for about four seconds.
2. The LEDs will blink a failure code which corresponds to the error listed in **Table 114, "Returned Values for Self-Test Diagnostic Failures" on page 542 Figure 50, "First LED Patterns," on page 545** shows the blinking LED codes.
3. Two non-blinking LED codes will follow. The interpretation of these codes depends on the preceding blinking code. Two sets of the non-blinking codes are listed in **figure 51, "Non-blinking LED Codes For Serial Bus Communication Failure," on page 546** and **figure 52, "Non-Blinking LED Codes For Miscellaneous Hardware Failure," on page 547**.
4. If there is more than one failure, the test will loop back to step 2 and repeat until the last failure is reported.

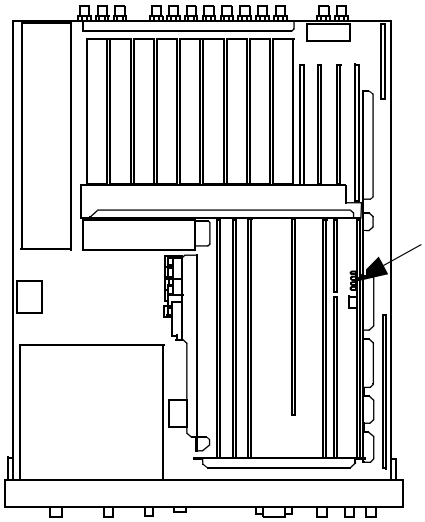
The pattern generated by the LEDs can be interpreted as a binary-weighting code. The LED closest to the rear of the instrument (labeled "0") is the least-significant bit. For example if the LEDs output the blinking pattern: Off, On, On, On (reading front-to-back or LEDs "4 3 2 1"), the binary number is 0111 or decimal 7. The error codes shown in **table 114 on page 542** are weighted by the binary value. The weighted value for this example is decimal $2^7 = 128$ or hexadecimal 80. (This example is easy to emulate; simply power-up the Test Set while holding a key down.)

1

Remove Test Set cover.

2

Turn power on.



3

Read LED sequence.

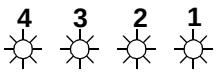
NOTE

For multiple failures, the failure patterns described below will repeat for all failures detected.

LED Sequences

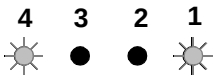
No Failures ...

- The LEDs will light for about 10 seconds, then all will turn off.



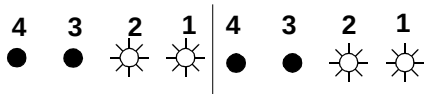
Failures ...

- Three patterns are displayed. The first blinks rapidly and indicates the type of failure.



See the following tables. (The example indicates a Serial Bus Communication fault.)

- The second and third patterns blink slowly and indicate failure details.



This manual covers only Serial Bus Communication and Miscellaneous Hardware failures. (The example indicates a faulty A35 Audio Analyzer 1.)

LED Legend

- ● = off
- ☼ = rapid blink
- ☼ = steady on or slow blink

Figure 49 **Reading the Self-Test Diagnostic Using the Internal LEDs**

If the first LED pattern displayed is ... (4 3 2 1)	Then the failure is ...
● ● ● ☼	Microprocessor
● ● ☼ ●	ROM Checksum (See note 1.)
● ● ☼ ☼	RAM (See note 2.)
● ☼ ● ●	RAM (See note 3.)
● ☼ ● ☼	Timer
● ☼ ☼ ●	Real-Time Clock
● ☼ ☼ ☼	Keyboard (stuck key or faulty key-down detector)
☼ ● ● ●	RS-232 I/O
☼ ● ● ☼	Serial Bus Communication (see **figure 51**)
☼ ● ☼ ●	Signaling Board Self Test
☼ ● ☼ ☼	CRT Controller Self Test
☼ ☼ ● ●	Miscellaneous Hardware (see figure 51.)

LED Legend
● = off
☼ = rapid blink
☼ = steady on or slow blink

NOTES

1. Second and third LED failure patterns:
   0001 and 0001 for any main ROM failure
   0001 and 0002 for boot ROM failure

2. Second and third LED failure patterns:
   0001 and 0001 for A17 Memory board RAM failure
   0001 and 0002 for A16 Host Controller board RAM failure

3. Second and third LED failure patterns:
   0001 and 0001 for A17 Memory board RAM failure
   0001 and 0010 for A17 Memory board RAM failure

Figure 50 First LED Patterns

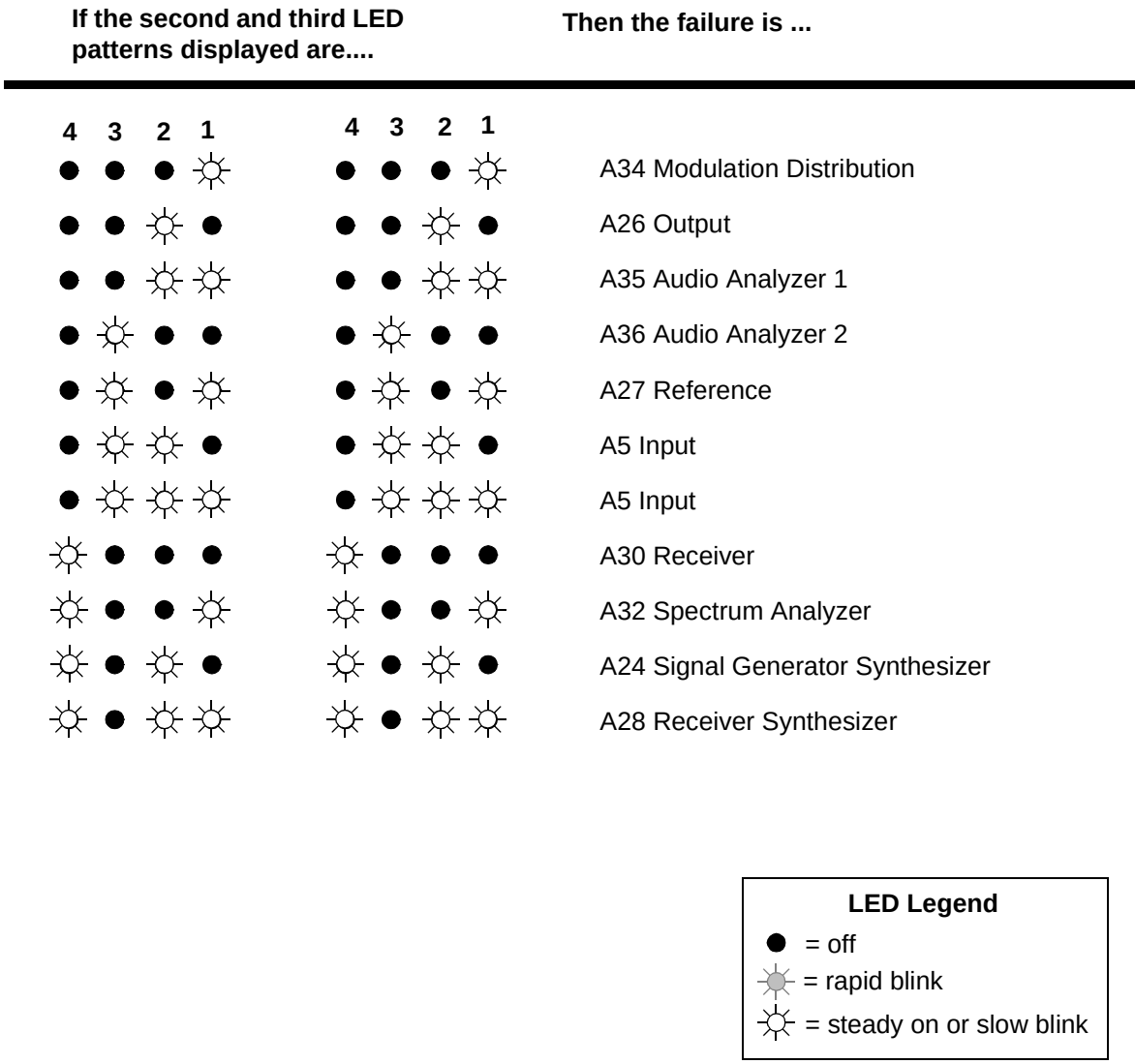


Figure 51 **Non-blinking LED Codes For Serial Bus Communication Failure**

If the second and third LED patterns displayed are....								Then the failure is ...
3	2	1	0	3	2	1	0	
●	●	●	☼	●	●	●	☼	A27 Reference
●	●	●	☼	●	●	☼	●	A35 Audio Filter 1 - C-Message
●	●	●	☼	●	●	☼	☼	A35 Audio Filter 2 - 6 kHz BPF
●	●	●	☼	●	☼	●	●	A36 Audio Analyzer 2 - Var Freq Notch Filter
●	●	●	☼	●	☼	●	☼	A33 Control Interface (HP-IB, Serial, Centronics.)

LED Legend

● = off

☼ = rapid blink

☼ = steady on or slow blink

Figure 52 **Non-Blinking LED Codes For Miscellaneous Hardware Failure**

Description Of Audio Diagnostics (AFDIAGS3)

Introduction

The Audio Diagnostics are divided into seven tests. In each test, a diagnosis of the failures is made at the end of all the measurements in that test. Even though each test is independent from the others, it is recommended that all tests be run in the order presented on the menu screen.

The failure codes are keyed to the circuit names in the block diagrams accompanying the test explanations. If an explanation is ranked **(high)**, there is a high probability that the assembly named is faulty. A rank of **(medium)** is shown when more than one assembly is listed and it is unclear which assembly is most likely at fault. A rank of **(low)** indicates that the assembly named is not the only suspect assembly.

Audio circuits not tested by the Audio Diagnostics are:

- A15 Signaling Source/Analyzer - audio analyzer portion
- A34 Modulation Distribution -circuits associated with the MIC/ACC jack, AM and FM outputs
- A35 Audio Analyzer 1 - some of the inputs
- A36 Audio Analyzer 2 - speaker drive, volume control, ALC
- General - digital control

Audio Frequency Generators 1 and 2

This test checks the ability of Audio Frequency Generators 1 and 2 on the A15 Signaling Source/Analyzer assembly to generate the DC levels programmed into them.

The Audio Frequency Generators are located on the Signaling/Source Analyzer assembly.

In this test, a “walking 1” (that is, 0, 1, 2, 4,…, 1024) is input to the DAC. The DC output level is measured by the Test Set’s internal DVM through a dedicated multiplexer line. The output level should be proportional to the programmed input.

The following values are also input to the DAC:

- 2047 (which gives the highest positive output)
- 2048 (which outputs 0 V)
- 2049 (which produces the negative of the value for 2047 and is sufficient to verify that the output can accurately output a negative voltage)
- 4095

Note that the measurements are static (DC); an AC waveform should be accurate if the DC values are correct. (Other tests will implicitly confirm this.)

The measurement limits are ±10% of nominal ±16 mV offset. To keep the test simple, no attempt is made to check incremental stepping to improve accuracy at low settings. Failure information is simple enough so that it is possible to pinpoint the faulty assembly without elaborate diagnosis. The failure codes are as follows:

Table 115 Audio Generators 1 and 2 Failure Codes

Failure Codes	Probable Cause(s)
Code 1	Suspect Signaling Source/Analyzer assembly (medium). (AFG1 Level Setting DAC faulty.) Or Measurement assembly (medium) (Voltmeter multiplexer problem.)
Code 2	Suspect Signaling Source/Analyzer assembly (medium) (AFG2 Level Setting DAC faulty.) Or Measurement assembly (medium) (Voltmeter multiplexer problem.)
Code 3	Suspect Measurement assembly (high) (Voltmeter problem.)

Preliminary Audio Paths

This test checks the ability of the A4 Modulation Distribution assembly to route an audio signal from Audio Frequency Generators, to the monitor select switch, and to the AM and FM modulators. It checks that the audio leaves the A4 assembly, but does not check whether it actually gets to the AM and FM modulators. The test that follows this one (*Modulation Distribution Internal Paths*) does the fine-resolution testing of the circuits.

This is a test of the integrity of the Modulation Distribution assembly. It verifies the functioning of the signal-routing switches. The nine paths in this test are shown as heavy lines in **figure 51** through **figure 56** .

NOTE: In these figures, three circuits on the Modulation Distribution assembly (AFG1 Amplifier, AFG1 Level Amplifier, and AFG1 Attenuator 1) are combined into one circuit block labeled AFG1 Circuits. This also applies to AFG2. Refer to **figure 58** which explicitly shows these circuits.

Measurement limits are ±10% of nominal when a signal is expected at the output (Paths 1, 3, 5, 6, 7, and 9). The limits are ±20 mV when the signal should be absent (Paths 2, 4, and 8). It is also as important to check paths which are intended to block signals (that is, that expect no output) as it is to check paths that should pass signals.

Paths which block signals are open switches (in Paths 2 and 4) or blocking capacitors with DC applied (in Path 8).

All paths are stimulated with DC except Path 9. Path 9 checks the DC blocking capacitor that couples signal to the front-panel AUDIO OUT port. Path 9 is the only path that uses a Peak Detector.

All measurements in this test are made with fixed level and gain parameters. Only signal-routing switch settings and the waveform of Audio Frequency Generator 2 are changed. The fixed settings are as follows:

- Level of Audio Frequency Generators 1 and 2 (AFG1 and AFG2) set to 1 V.
- Frequency of Audio Frequency Generator 2 set to 1 kHz in AC.
- Gain of AFG 1 and 2 Level Amplifiers set to 0.784 (DAC set to 200 out of a maximum of 255).
- Attenuation of AFG1 and AFG2 Attenuator 1 set to 0 dB.
- Attenuation of AFG1 and AFG2 Attenuator 2 set to 0 dB.

These fixed final settings result in nominal DVM readings of:

- 1.725 V for Paths 1.
- 3.45 V for Path 5.
- 2.16 V for Paths 6, 7, and 9.
- 0 V for Paths 2, 4, and 8.

These settings are near optimum for the devices tested. The DAC setting of 200 (which sets the gain of the two AFG level amplifiers) is the nominal maximum. (Values between 201 and 215 are not normally used.)

The following example illustrates how the levels are determined. For Path 1:

- AFG1 input is 1 V.
- AFG1 Amplifier gain is 2.2 (6.85 dB).
- AFG1 Level Amplifier gain is set to 0.784 (-2.11 dB).
- AFG1 Attenuator 1 gain is set to 1 (0 dB).
- Modulation Select Sum Amplifier gain is 1 (0 dB).
- Other gains (switches and buffers) are 1 (0 dB).

Multiplying the these settings gives 1.725 V (4.74 dBV) at the input to the DVM.

The failure codes for the preliminary audio paths are as follows:

Table 116 Preliminary Audio Paths Failure Codes

Failure Codes	Probable Cause(s)
Code 2	Suspect Modulation Distribution assembly (high) (AFG1 Modulation Select Source Switch stays closed.)
Code 8	Suspect Modulation Distribution assembly (high) (AFG2 Modulation Select Source Switch stays closed.)
Code 17	Suspect Modulation Distribution assembly (high) (AFG1 Modulation Select Source Switch open.)
Code 20	Suspect Modulation Distribution assembly (high) (AFG2 Modulation Select Source Switch open.)
Code 21	Suspect Modulation Distribution assembly (high)\ (Modulation select output problem. Check Modulation Select Source Switch (including FM Polarity amplifier, not shown in figure).)
Code 31	Suspect Modulation Distribution assembly (high) (Monitor Select Multiplexer Switch stays in audio output position.)
Code 32	Suspect Modulation Distribution assembly (high) (AFG1 Atten 2 or Audio Output Sum Amplifier open.)
Code 49	Suspect Modulation Distribution assembly (high) (AFG1 path problem. Check AFG1 circuits Filter Amplifier, Int Level Amplifier DAC, and Atten 1.)
Code 96	Suspect Modulation Distribution assembly (high) (Audio AC/DC Coupling switch open.)
Code 117	Suspect Audio Analyzer 2 assembly (medium) (Problem with path from the Monitor Select Input to DVM OUT.) Or Measurement assembly (low) (Voltmeter multiplexer problem.)
Code 128	Suspect Modulation Distribution assembly (high) (Shorted Audio AC/DC Coupling switch or capacitor.)
Code 256	Suspect Modulation Distribution assembly (high) (Audio AC/DC Coupling capacitor open.) Or Audio Analyzer 2 assembly (low)(Problem with path from Monitor Select input to Pos Peak Detector.) Or Measurement assembly (low) (Voltmeter multiplexer problem.)
Code 320	Suspect Modulation Distribution assembly (high) (AFG2 Atten 2 or Audio Output Sum Amplifier open.)
Code 340	Suspect Modulation Distribution assembly (high) (AFG2 path problem. Check AFG2 circuits Filter Amplifiers, Internal Level Amplifier DAC, and Atten 1.)

Table 116 Preliminary Audio Paths Failure Codes (Continued)

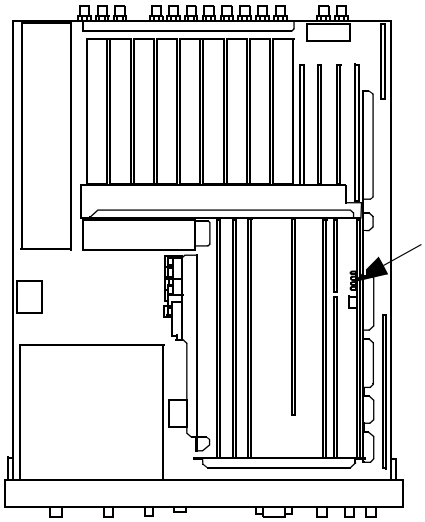
Failure Codes	Probable Cause(s)
Code 352	Suspect Modulation Distribution assembly (high) (Audio output problem. Check Audio Output Sum Amplifier, and Monitor Select Multiplexer switch.)
Code 373	Suspect Modulation Distribution assembly (high) (Monitor Select Multiplexer switch open or stays in modulation input or Microphone input position (not shown in figure).) Or Measurement assembly (low) (Voltmeter multiplexer problem.)

1

Remove Test Set cover.

2

Turn power on.



3

Read LED sequence.

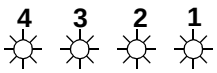
NOTE

For multiple failures, the failure patterns described below will repeat for all failures detected.

LED Sequences

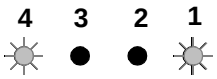
No Failures ...

- The LEDs will light for about 10 seconds, then all will turn off.



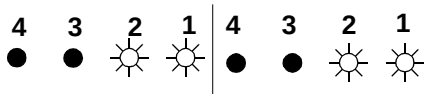
Failures ...

- Three patterns are displayed. The first blinks rapidly and indicates the type of failure.



See the following tables. (The example indicates a Serial Bus Communication fault.)

- The second and third patterns blink slowly and indicate failure details.

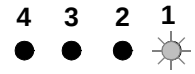
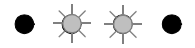
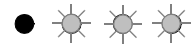


This manual covers only Serial Bus Communication and Miscellaneous Hardware failures. (The example indicates a faulty A35 Audio Analyzer 1.)

LED Legend

- ● = off
- ☼ = rapid blink
- ☼ = steady on or slow blink

Figure 53 **Reading the Self-Test Diagnostic Using the Internal LEDs**

If the first LED pattern displayed is ...	Then the failure is ...
	Microprocessor
	ROM Checksum (See note 1.)
	RAM (See note 2.)
	RAM (See note 3.)
	Timer
	Real-Time Clock
	Keyboard (stuck key or faulty key-down detector)
	RS-232 I/O
	Serial Bus Communication (see **figure 51**)
	Signaling Board Self Test
	CRT Controller Self Test
	Miscellaneous Hardware (see figure 51.)

NOTES

1. Second and third LED failure patterns:
   0001 and 0001 for any main ROM failure
   0001 and 0002 for boot ROM failure

2. Second and third LED failure patterns:
   0001 and 0001 for A17 Memory board RAM failure
   0001 and 0002 for A16 Host Controller board RAM failure

3. Second and third LED failure patterns:
   0001 and 0001 for A17 Memory board RAM failure
   0001 and 0010 for A17 Memory board RAM failure

Figure 54 First LED Patterns

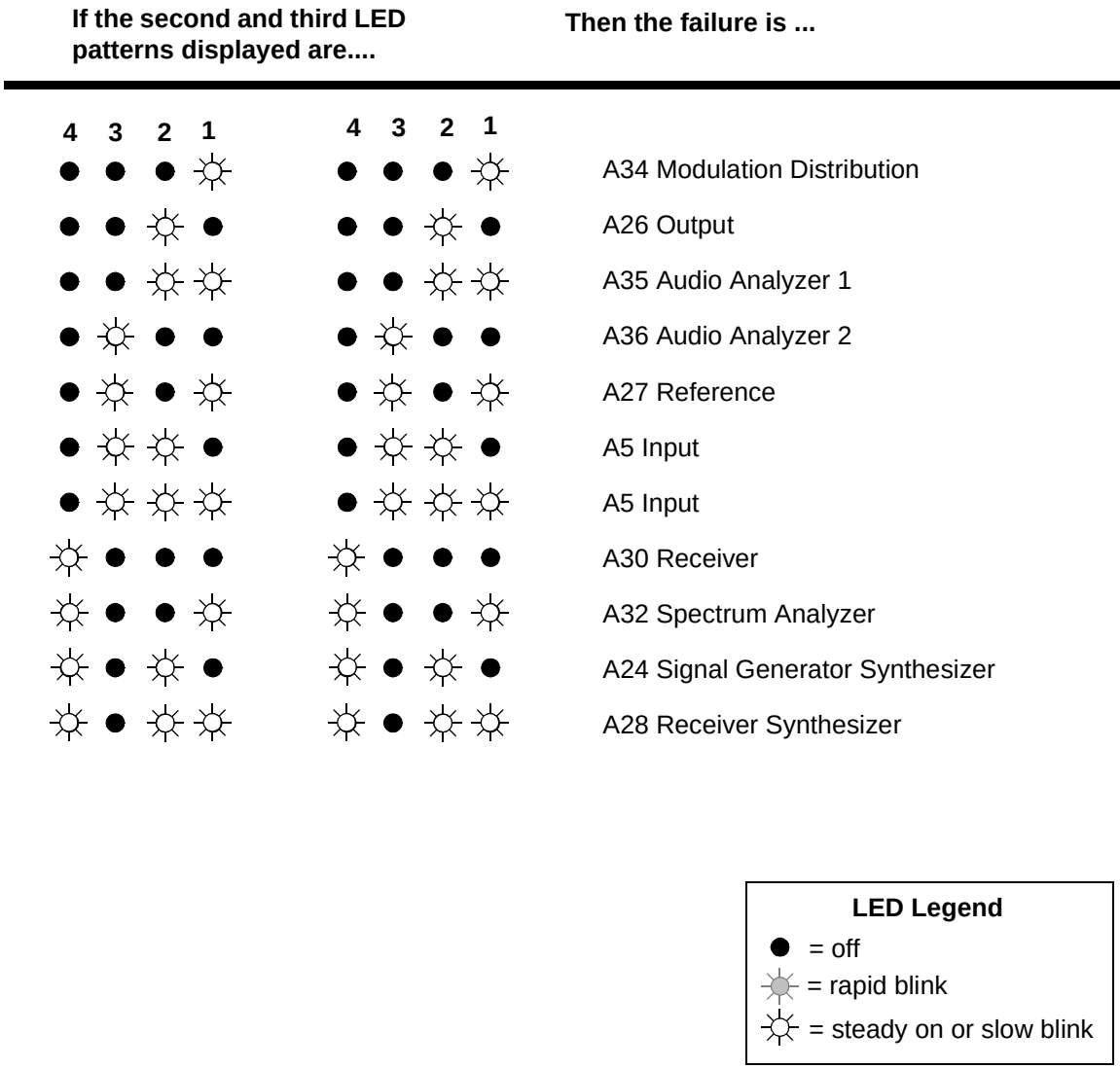


Figure 55 **Non-blinking LED Codes For Serial Bus Communication Failure**

If the second and third LED patterns displayed are....								Then the failure is ...
3	2	1	0	3	2	1	0	
●	●	●	☼	●	●	●	☼	A27 Reference
●	●	●	☼	●	●	☼	●	A35 Audio Filter 1 - C-Message
●	●	●	☼	●	●	☼	☼	A35 Audio Filter 2 - 6 kHz BPF
●	●	●	☼	●	☼	●	●	A36 Audio Analyzer 2 - Var Freq Notch Filter
●	●	●	☼	●	☼	●	☼	A33 Control Interface (HP-IB, Serial, Centronics.)

LED Legend

● = off

☼ = rapid blink

☼ = steady on or slow blink

Figure 56 **Non-Blinking LED Codes For Miscellaneous Hardware Failure**

Modulation Distribution Internal Paths

The Modulation Distribution assembly paths that relate to inputs from the two Audio Frequency Generators are tested. The paths are the same as in the *Preliminary Audio Paths* test; however, the circuits are tested more thoroughly by varying settable parameters (gain and attenuation). The paths are illustrated in **figure 57, "Modulation Distribution Internal Paths 1 to 4," on page 560** and **figure 58, "Mod Distribution Internal Paths 5-8 (Paths 9-11 check Internal Pre Mod Filters)," on page 561**.

The audio sources are set to AC. The measurements at the DVM are always DC since the signal is routed to the Peak Detector in Audio Analyzer 2 (this is not shown in **figure 57** and **figure 58**). Measurement limits are ±10% of nominal ±10 mV offset when a signal is expected at the output, and ±10 mV when the signal is absent (when Attenuator 2 is set to open).

In this test, a “walking 1” (that is, 0, 1, 2, 4,…, 128, 255) is programmed into the gain-control DAC of the Level Amplifiers. In normal use the highest DAC setting is 200. The system gain was discussed in the *Preliminary Audio Paths* test. Attenuator 1s are set to attenuation’s of 1 and 0.1. Attenuator 2s are set to attenuation’s of 1, 0.01, and open. Do not confuse Attenuators 1 and 2. There are two Attenuator 1s, AFG1 Attenuator 1 and AFG2 Attenuator 1; there are two Attenuator 2s, AFG1 Attenuator 2 and AFG2 Attenuator 2.

There are three low-pass filters (150 Hz, 250 Hz, and 20 kHz) in the path for AFG2. The three filters are tested in measurement paths 9, 10, and 11 (not shown in **figure 58**).

The failure codes for the Modulation Distribution assembly's internal paths are as follows:

Table 117 Modulation Distribution Internal Paths Failure Codes

Failure Codes	Probable Cause(s)
Code 2	Suspect Modulation Distribution assembly (high) (AFG1 Atten 1 stays at gain=1.)
Code 5	Suspect Modulation Distribution assembly (high) (AFG1 Atten 1 stays at gain=0.1.)
Code 7	Suspect Modulation Distribution assembly (high) AFG1 path problem. Check AFG1 Filter/Amplifiers, Int Level Amplifier DAC, and Atten 1 and 2.)
Code 11	Suspect Modulation Distribution assembly (high) (AFG1 Atten 2 stays at gain=0.01.)
Code 12	Suspect Modulation Distribution assembly (high) (AFG1 Atten 2 stays at gain=1.)
Code 32	Suspect Modulation Distribution assembly (high) (AFG2 Atten 1 stays at gain=1.)
Code 80	Suspect Modulation Distribution assembly (high) (AFG2 Atten 1 stays at gain=0.1.)
Code 112	Suspect Modulation Distribution assembly (high) (AFG2 path problem. Check AFG2 Filter/Amplifiers, Int Level Amplifier DAC, and Atten 1 and 2.)
Code 119	Suspect Modulation Distribution assembly (high) (Path from Audio Output Sum Amplifier through Monitor Select Multiplexer open.) OR Audio Analyzer 2 assembly (low) (Path from the Monitor Select Input to DVM OUT faulty.)
Code 176	Suspect Modulation Distribution assembly (high) (AFG2 Atten 2 stays at gain=0.01.)
Code 192	Suspect Modulation Distribution assembly (high) (AFG2 Atten 2 stays at gain=1.)

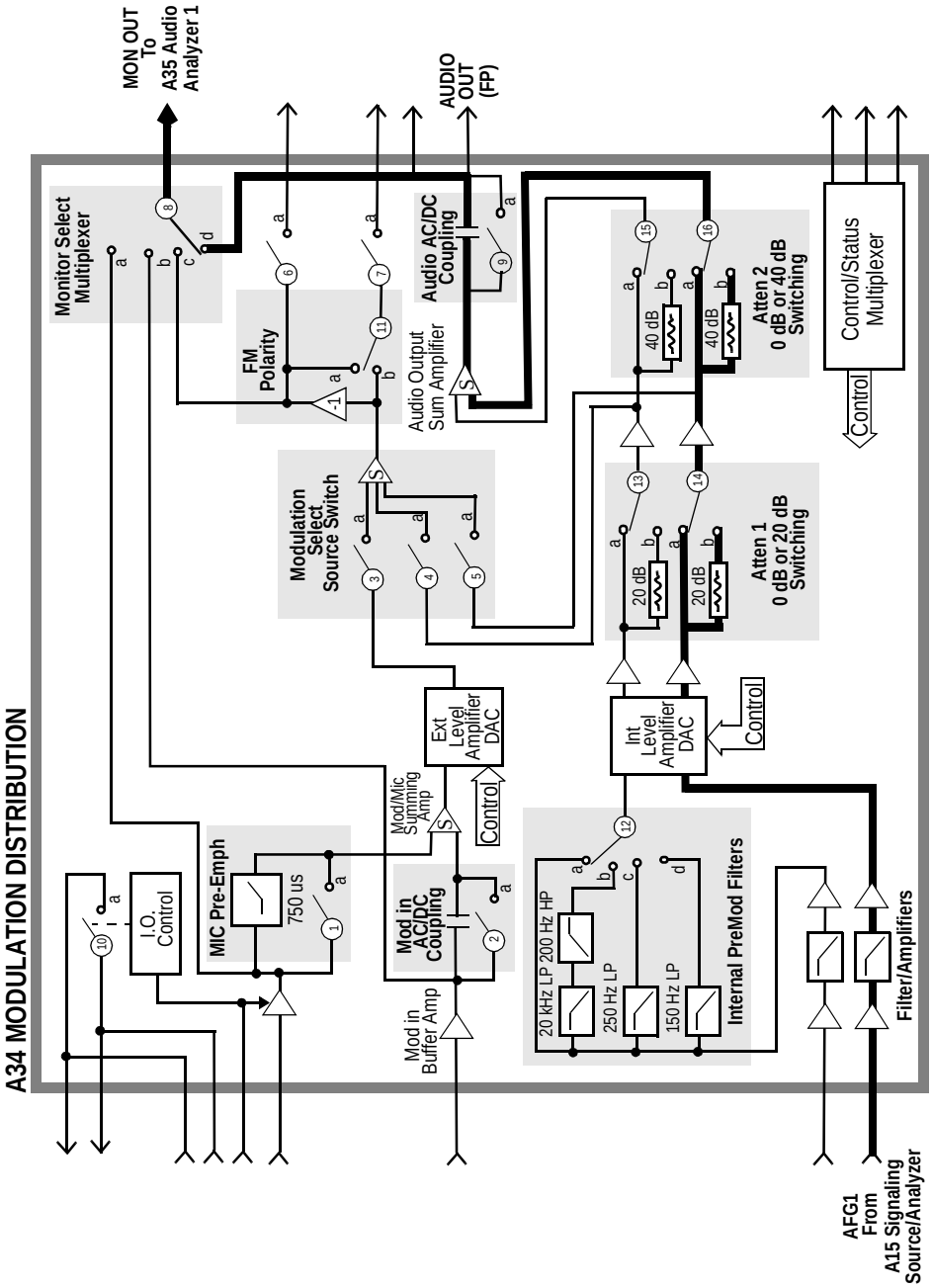


Figure 57 **Modulation Distribution Internal Paths 1 to 4**

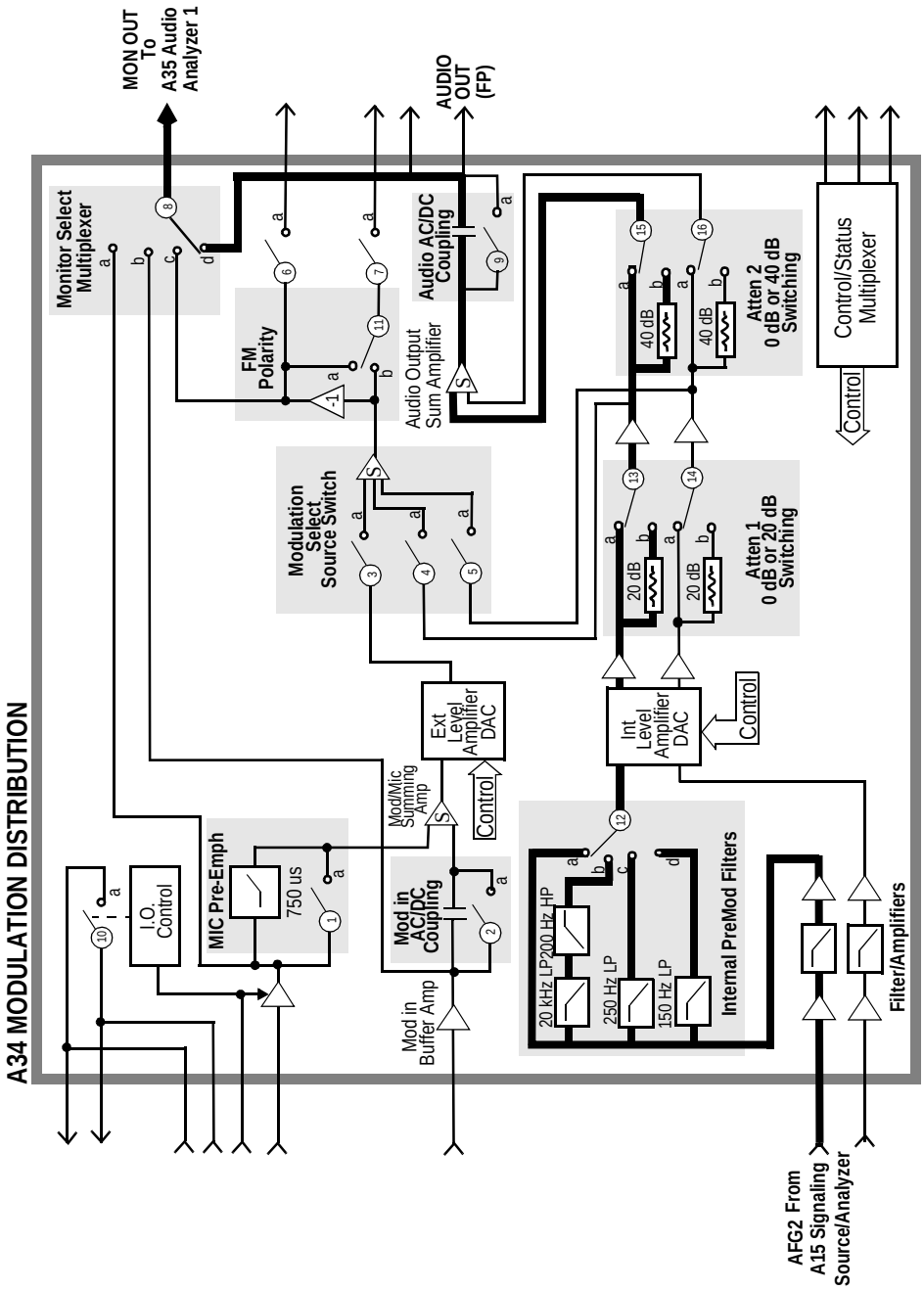


Figure 58 **Mod Distribution Internal Paths 5-8 (Paths 9-11 check Internal Pre Mod Filters)**

Modulation Distribution External Paths

This test checks the ability of the A34 Modulation Distribution assembly to route an external modulation signal to the monitor output of the A34 assembly. It also checks the ability of the A34 assembly to adjust the level of an external modulation signal. The paths which relate to internal inputs are checked in the previous test.

This test checks the Modulation Distribution assembly's path from the rear-panel MODULATION INPUT to the Monitor Select output. Before doing this, the path from Audio Frequency Generator 1 to the Monitor Select is checked to assure that the audio source can be used as an external test signal via the front-panel AUDIO OUT connector. The paths are illustrated in **figure 59** through **figure 61** .

Audio Generator 1 is the signal source for all measurements (internal or external). The signal is DC except where AC coupling is checked (Path 7). Measurement limits are ±10% of nominal when a signal is expected at the output, and ±40 mV when the signal is absent (this occurs when the Modulation Select Source Switch is set to open and when DC is applied to blocking capacitor of Mod In AC/DC coupling). However, the limit on DAC-gain controlled amplifiers is ±10% of nominal ±40 mV.

In Path 1 the integrity of the internal signal at the AUDIO OUT connector is tested. In Path 2 the signal is routed externally to the MODULATION INPUT connector where it is measured through the shortest path (which goes from the output of the Modulation Input Buffer Amplifier to the Monitor Multiplexer Select Source switch).

The strategy for checking the DAC-controlled external level amplifier is similar to the strategy for the previous test. This amplifier has two variable-gain stages: (1) a stage which sets the level based on user input and (2) a fine-adjustment stage which is factory- or user-calibrated to correct for variations in overall path gain. Stage 1 is tested with a "walking 1"; stage 2 is tested at one point (DAC set to 255).

The external attenuator is checked for gains of 1 and 0.1.

The failure codes for the Modulation Distribution assembly's external paths are as follows:

Table 118 Modulation Distribution External Paths Failure Codes

Failure Codes	Probable Cause(s)
Code 1	Suspect Modulation Distribution assembly (high) (Audio output path problem from AUDIO OUT junction to Monitor Select Multiplexer output.)
Code 3	Suspect Modulation Distribution assembly (high) (Monitor Select Multiplexer switch stays in Mod Select position.)
Code 4	Suspect Modulation Distribution assembly (high) (The calibration portion of Ext Level Amplifier DAC stays at a low setting or has low gain.)
Code 8	Suspect Modulation Distribution assembly (high) (Ext Level Amplifier Attenuation stays at gain=1 or Ext Level Amplifier DAC stays at high gain.)
Code 12	Suspect Modulation Distribution assembly (high) (Mod In AC/DC Coupling switch is always open.)
Code 16	Suspect Modulation Distribution assembly (high) External switch 3 of Modulation Select Source stays closed.)
Code 32	Suspect Modulation Distribution assembly (high) (Mod In AC/DC Coupling switch or capacitor is shorted.)
Code 64	Suspect Modulation Distribution assembly (high) (The Mod In AC/DC Coupling capacitor is open.)
Code 68	Suspect Modulation Distribution assembly (high) (Ext Level Amplifier Attenuation stays at gain=0.1.)
Code 76	Suspect Modulation Distribution assembly (high) (The Modulation Input path is faulty. Check Modulation/Mic Summing Amp, Ext Level Amplifier DAC, Ext Level Amplifier Attenuation, and Modulation Select Source Switch summing amplifier or switches.)
Code 78	Suspect Modulation Distribution assembly (high) (The path from AUDIO OUT to MODULATION INPUT or Mod In Buffer Amp is faulty.)
Code 79	Suspect Modulation Distribution assembly (high) (AFG1 path problem. Check AFG1 Filter/Amplifiers, Int Level Amplifier DAC, and Atten 1 and 2.) Or path from Audio Output Sum Amplifier to Monitor Select Multiplexer output is faulty.) Or Measurement assembly (low) (Voltmeter multiplexer problem.)
Code 125	Suspect Modulation Distribution assembly (high) (Monitor Select Multiplexer switch stays in modulation input position **c**.)
Code 126	Suspect Modulation Distribution assembly (high) (Monitor Select Multiplexer switch stays in audio output position **d**.)

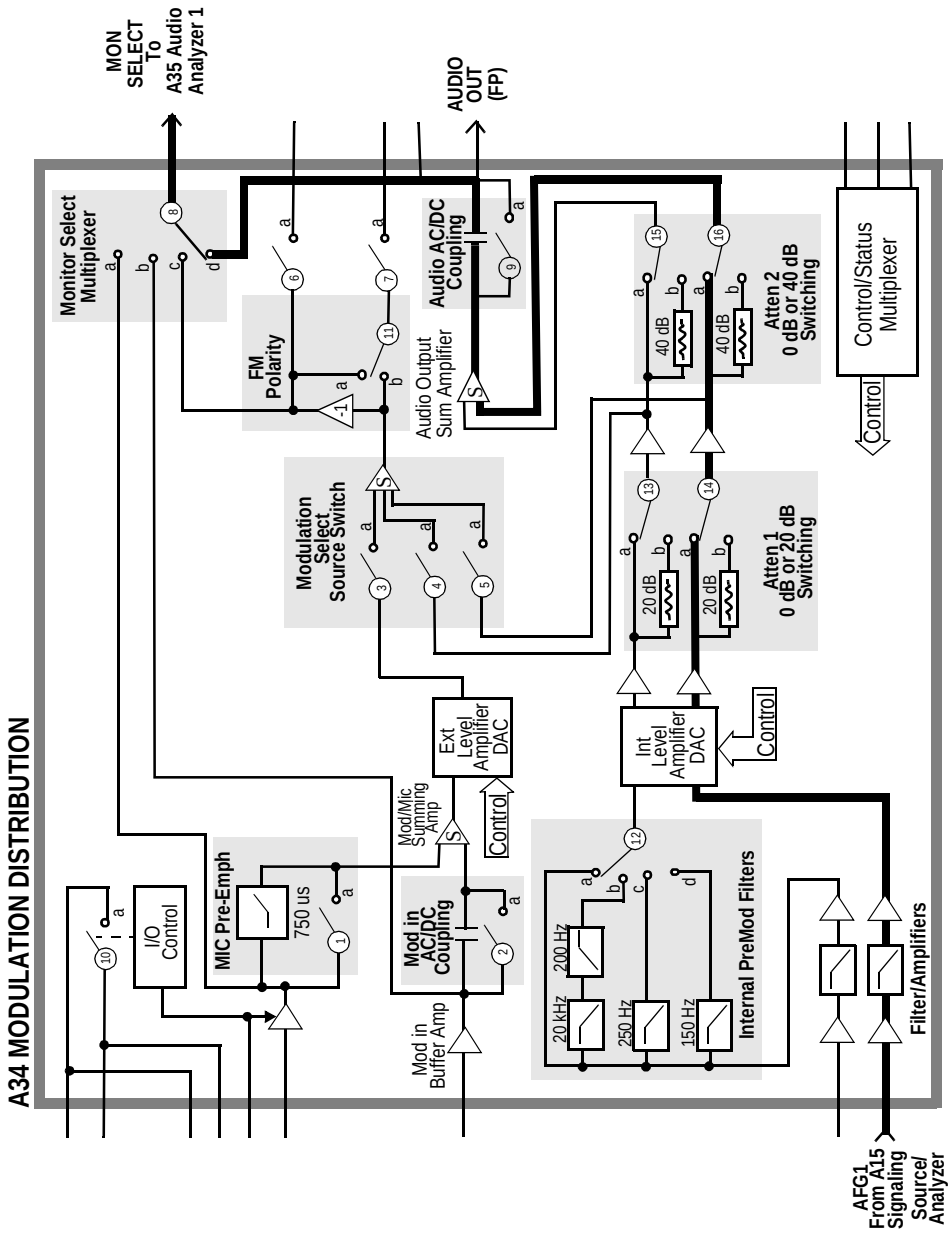


Figure 59 **Modulation Distribution External Path 1**

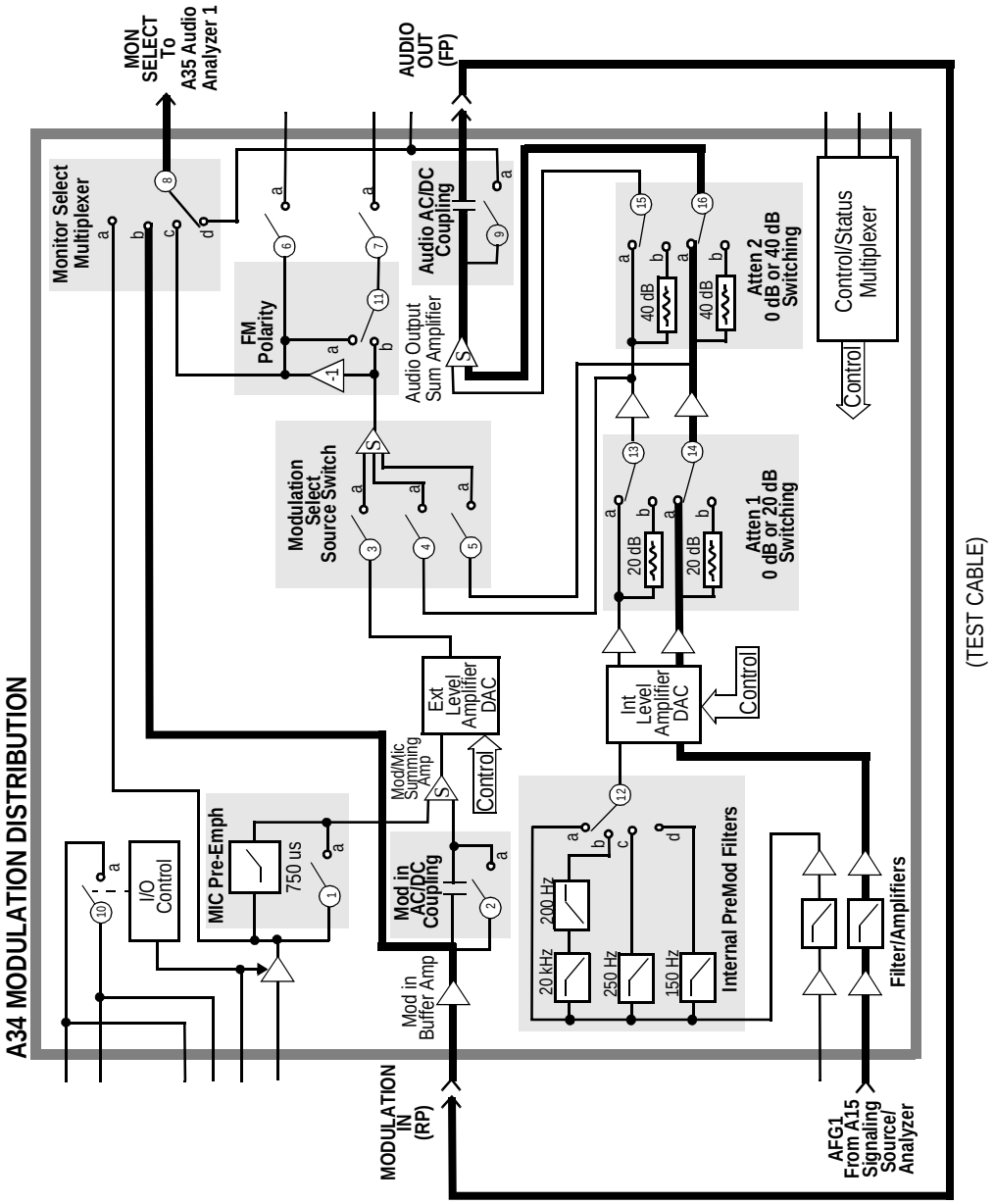


Figure 60 **Modulation Distribution External Path 2**

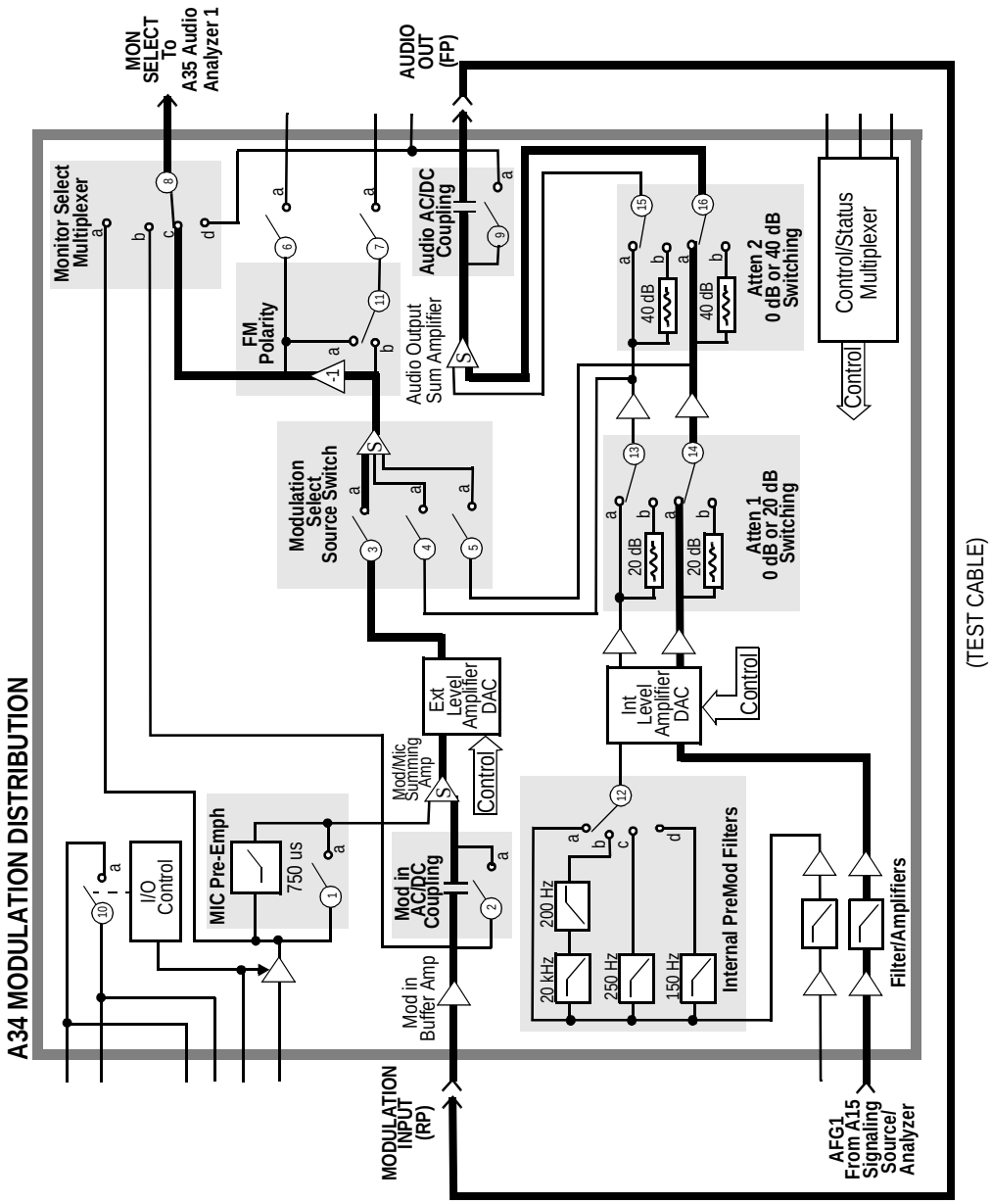


Figure 61 **Modulation Distribution External Paths 3 to 7**

Audio Analyzer 1 Internal Paths

This test checks Audio Analyzer 1's paths which receives the input from the Modulation Distribution assembly. The paths are illustrated in **figure 62** , **figure 63** , and **figure 64** .

In Path 1, the audio source is set to DC. The simplest path through the Modulation Distribution assembly is chosen. The signal passes through Audio Analyzer 1 by this path to the DVM. In Path 2, the source is set to AC and the signal is peak detected before being measured by the DVM. In Paths 2 to 4, the gain of the Programmable Input Gain amplifier is tested for gains of 1, 10, and 100 (0, 20, 40 dB). The input signal is adjusted to keep the signal level in the range of the circuits that follow. In Paths 5 to 12, the frequency response of the filters are tested.

Paths 8 and 12 specifically test the optional filters. The presence and identification of the filters is determined by measuring a DC voltage from a resistive divider on the filter daughter-board. 0 V corresponds to no filter present; 0.95 to 1.1 V indicates the 6 kHz high-pass filter; and so forth. Measurement limits are based on the specified frequency response.

The measurement limits are ±10% of nominal ±10 mV offset for levels not involved with frequency responses (Paths 1 to 5). Through the filters, the measurement limits vary: ±20% in the passband and much wider in the stopband (Paths 6 to 12).

The failure codes for Audio Analyzer 1's internal paths are as follows:

Table 119 Audio Analyzer 1 Internal Paths Failure Codes

Failure Codes	Probable Cause(s)
Code 1	Suspect Audio Analyzer 1 assembly (high) (Failure in path from Input Buffer Amplifier to DVM Select Switch Out.)
Code 12	Suspect Audio Analyzer 1 assembly (high) (Progammable Input Gain stays at gain=1.)
Code 14	Suspect Audio Analyzer 1 assembly (high) (Audio Range Peak Detector faulty.)
Code 15	Suspect Audio Analyzer 1 assembly (high) (DVM Select Switch faulty.)
Code 32	Suspect Audio Analyzer 1 assembly (high) (50 Hz HPF faulty.)
Code 64	Suspect Audio Analyzer 1 assembly (high) (300 Hz HPF faulty or HPF select switch stays at 50 Hz HPF.)
Code 96	Suspect Audio Analyzer 1 assembly (high) (HPF select switch stays in bypass.)
Code 256	Suspect Audio Analyzer 1 assembly (high) (300 Hz HPF faulty.)
Code 288	Suspect Audio Analyzer 1 assembly (high) (HPF select switch stays in 300 Hz HPF position.)
Code 512	Suspect Audio Analyzer 1 assembly (high) (3 kHz HPF faulty.)
Code 768	Suspect Audio Analyzer 1 assembly (high) (LPF select switch stays in 15 kHz LPF position.)
Code 1024	Suspect Audio Analyzer 1 assembly (high) (15 kHz HPF faulty.)
Code 1280	Suspect Audio Analyzer 1 assembly (high) (LPF select switch stays in 3 kHz LPF position.)
Code 1648	Suspect Audio Analyzer 1 assembly (high) (LPF select switch stays in 300 Hz LPF position.)
Code 1792	Suspect Audio Analyzer 1 assembly (high) (LPF select switch stays in bypass position.)
Code 1904	Suspect Audio Analyzer 1 assembly (high) (HPF select switch open, LPF select switch open, or DVM Select Switch stays in Audio Range Peak Det position.) Or Audio Analyzer 2 assembly (low) (Path from Filtered Audio Input to DVM Select Output faulty.)
Code 1910	Suspect Audio Analyzer 1 assembly (high) (Programmable Input Gain stays at gain=100.)

Table 119 Audio Analyzer 1 Internal Paths Failure Codes (Continued)

Failure Codes	Probable Cause(s)
Code 1914	Suspect Audio Analyzer 1 assembly (high) (Programmable Input Gain stays at gain=10.)
Code 1916	Suspect Audio Analyzer 1 assembly (high) (DVM Select Switch stays in Input Buffer Amplifier position **d**.)
Code 1918	Suspect Audio Analyzer 1 assembly (high) (Programmable Input Gain faulty.)
Code 1919	Suspect Audio Analyzer 1 assembly (high) (Input Select Switch, Input Buffer Amplifier, HPF select switch, filter buffer amplifier, LPF select switch, filtered output amplifier, or DVM Select Switch failed; or Optional High Pass or Low Pass filters missing.) Or Modulation Distribution assembly (low) (Faulty signal from Monitor Select Multiplexer output.)

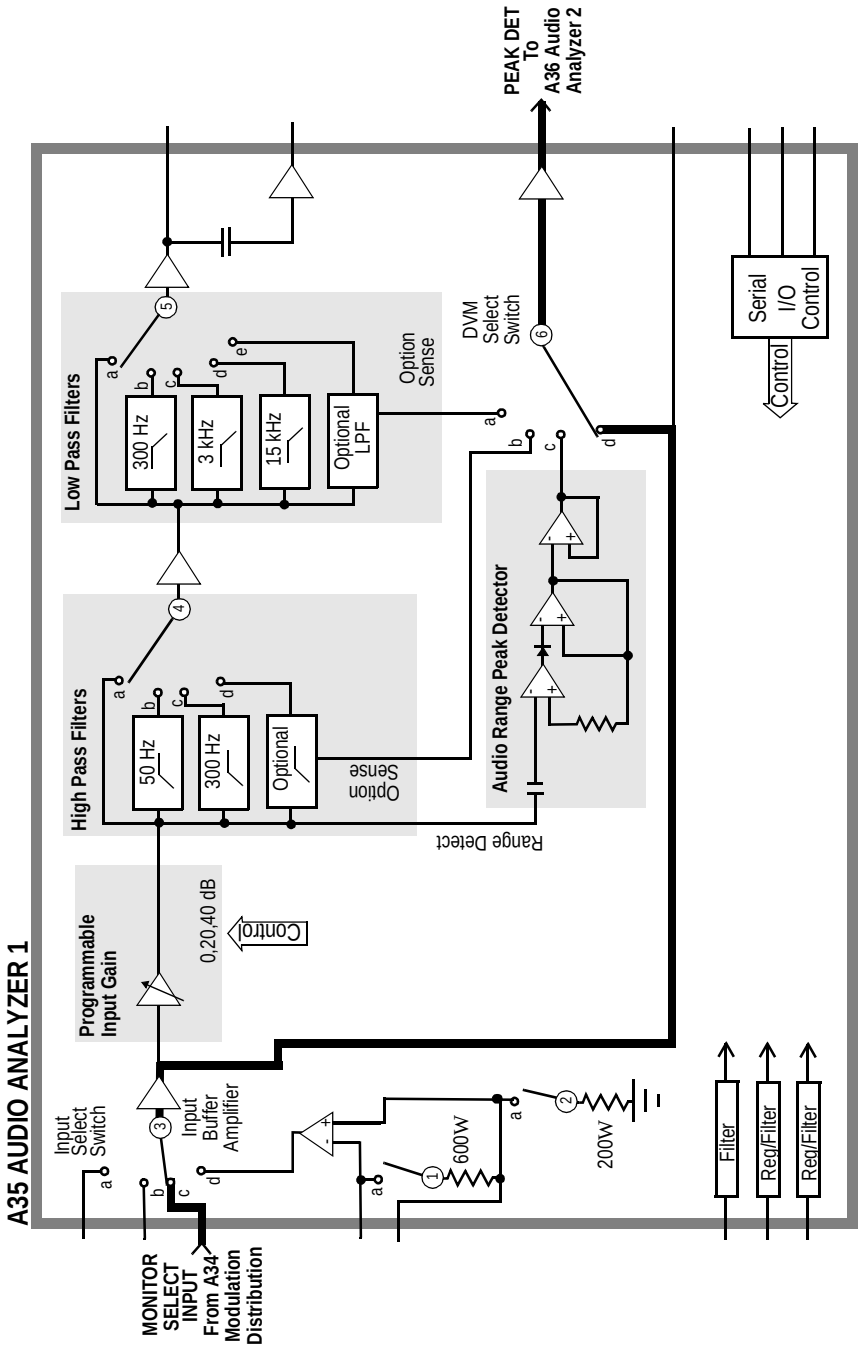


Figure 62 **Audio Analyzer 1 Internal Path 1**

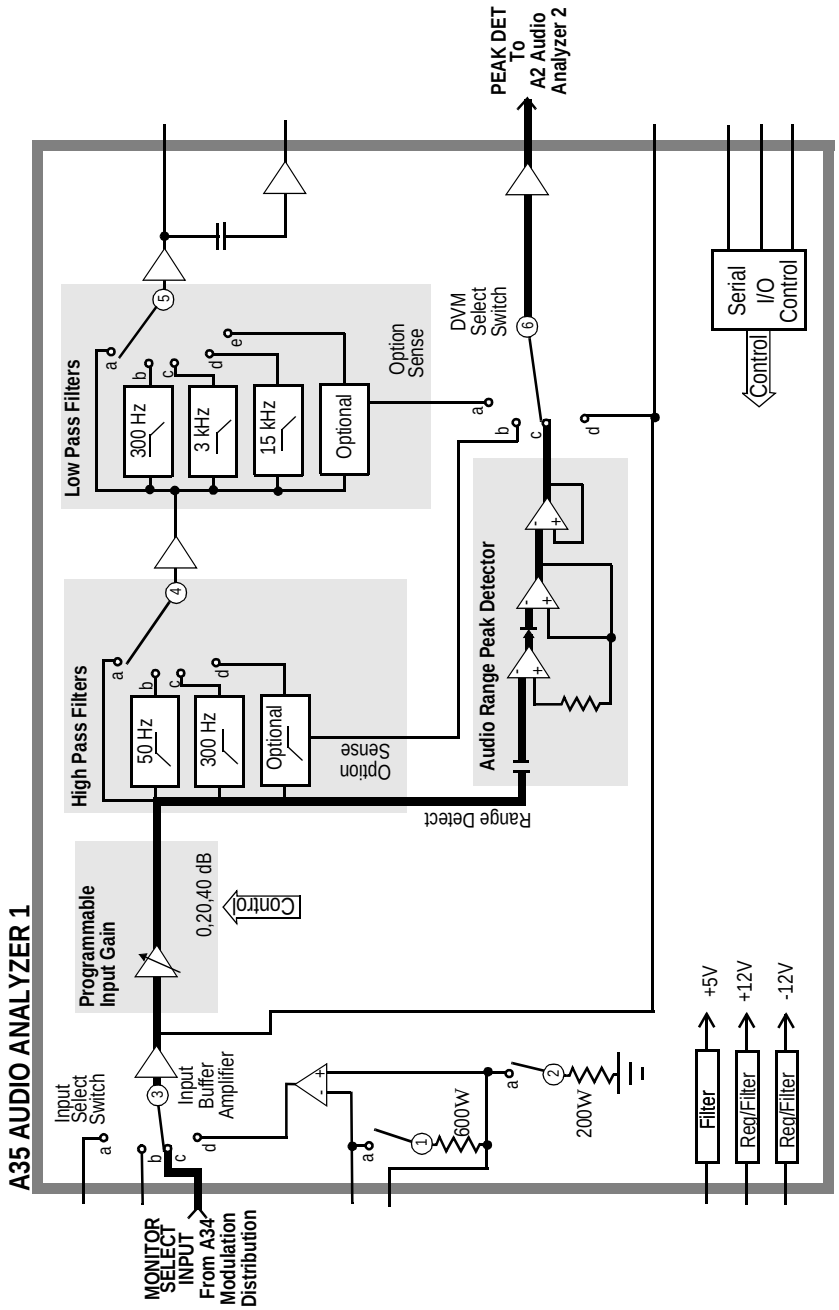


Figure 63 **Audio Analyzer 1 Internal Paths 2 to 4**

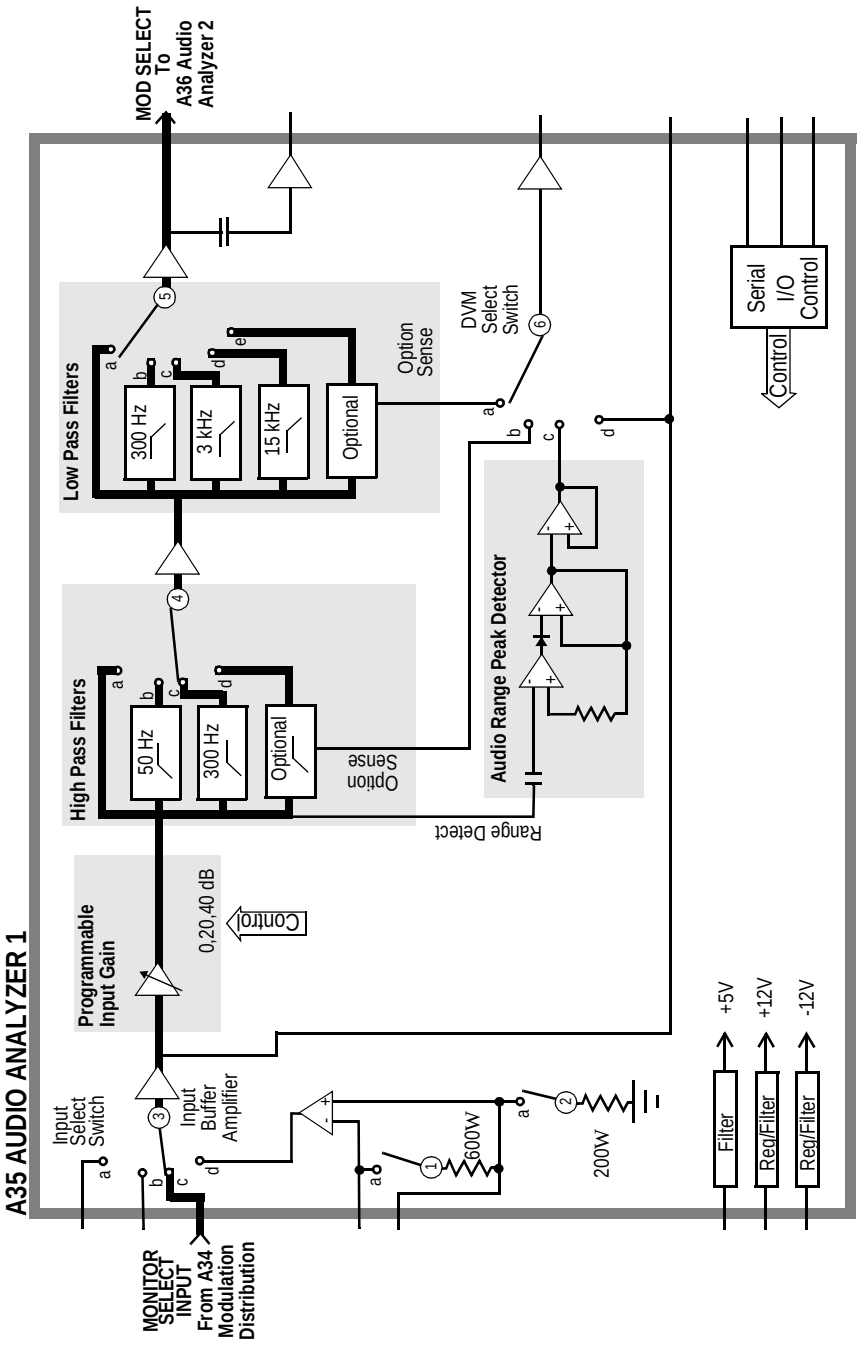


Figure 64 **Audio Analyzer 1 Internal Paths 5 to 12**

Audio Analyzer 1 External Paths

This test checks Audio Analyzer 1's path which receives its input from the front-panel AUDIO IN connector. The path which receives the internal inputs is checked in the previous test. The source for this test is the Audio Frequency Generator 1 which routes through the Modulation Distribution assembly and an external cable from the front-panel AUDIO OUT connector. The external path is illustrated in **figure 65, "Audio Analyzer 1 External Path 1," on page 574**. A check to verify that the input switch can switch out of the audio input position is performed. The check of the input switch is the same as depicted in **figure 63, "Audio Analyzer 1 Internal Paths 2 to 4," on page 571**.

The test limits for the audio input is ±10% of nominal. The limits for the decoupled audio input is ±20 mV. The Peak Detector converts the AC signal to DC.

The failure codes for the Audio Analyzer's external paths are as follows:

Table 120 Audio Analyzer 1 External Paths Failure Codes

Failure Codes	Probable Cause(s)
Code 1	Suspect Audio Analyzer assembly (high) (Input Select Switch stays in Audio Input position **d**.)
Code 2	Suspect Audio Analyzer 1 (medium) or cable (medium)

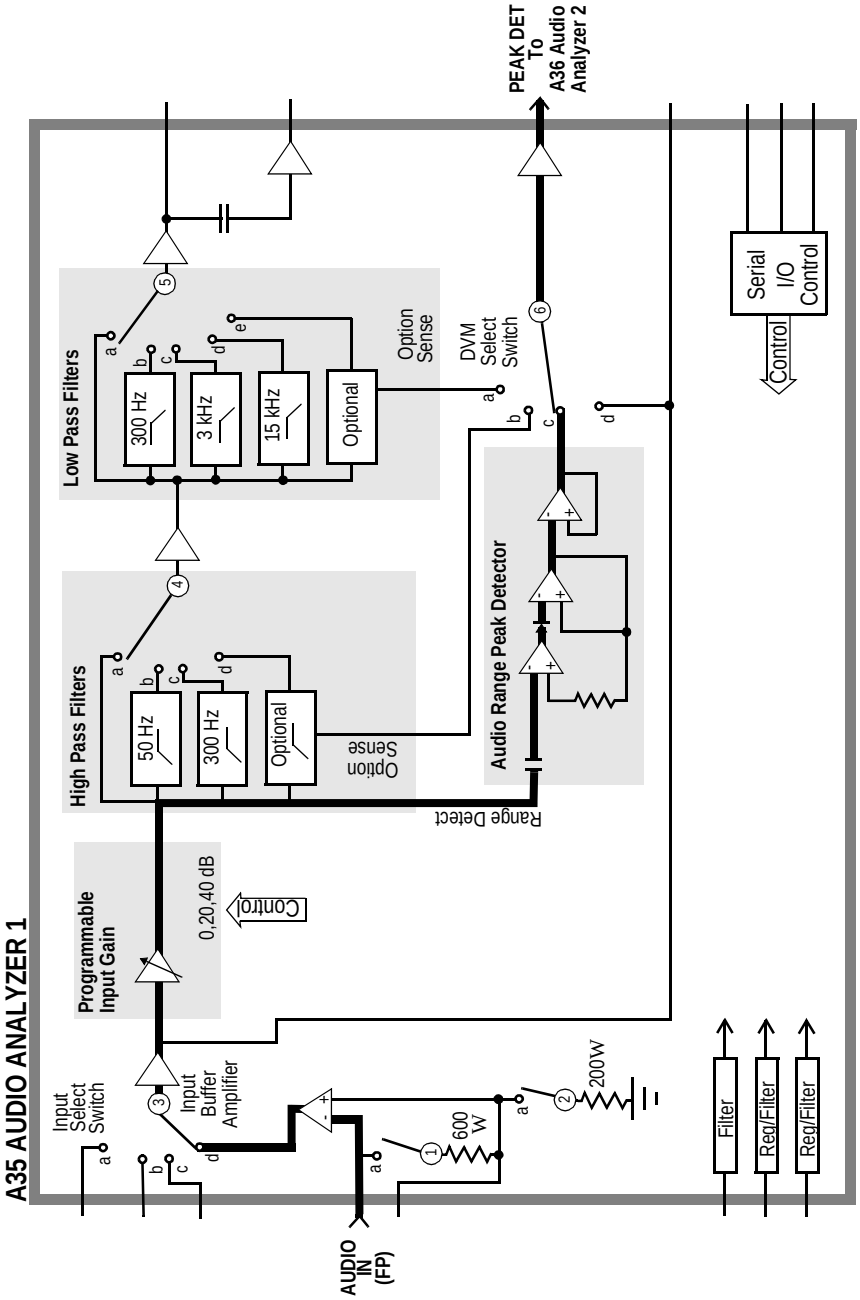


Figure 65 **Audio Analyzer 1 External Path 1**

Audio Analyzer 2 Paths

This test checks Audio Analyzer 2 (A36). The source for this test is Audio Frequency Generator 1 which is always set to AC. The signal from Audio Frequency Generator 1 passes through the Modulation Distribution assembly, through the Modulation Select Source Switch, and the Monitor Select Multiplexer. It bypasses Audio Analyzer 1. The test paths are illustrated in **figure 66** to **figure 69** .

The gain of the Detector Range Amplifier (Paths 5 to 7) is 3.16, 10, and 31.6 corresponding to gains of 10 dB, 20 dB, and 30 dB. The gain of the Post-Notch Amplifier (Paths 11 to 14 in **figure 68, "Audio Analyzer 2 Path 8," on page 579**) is similar.

The variable-frequency Notch Filter is tested at the beginning of this test. The input is set to 1 kHz and the notch output is nulled using a notch-error detector in conjunction with a DAC-setting routine. The notch-error detector is not shown in **figure 68, "Audio Analyzer 2 Path 8," on page 579**, but it is multiplexed with the pre-notch RMS detector.

The test then proceeds as if the filter were fixed at 1 kHz and measurements are made at the output of the filter for input frequencies of 500, 1000, and 2000 Hz.

The failure codes for Audio Analyzer 2's paths are as follows:

Table 121 Audio Analyzer 2 Paths Failure Codes

Failure Codes	Probable Cause(s)
Code 1	Suspect Audio Analyzer 2 assembly (high) (Peak Detector Select Switch stays in position **b**.)
Code 2	Suspect Audio Analyzer 2 assembly (high) (Neg Peak Detector faulty or DVM Select Switch stays in position **b**.)
Code 3	Suspect Audio Analyzer 2 assembly (high) (Coupling capacitor following Peak Detector Buffer Amplifier faulty, not shown in figure.)
Code 8	Suspect Audio Analyzer 2 assembly (high) (De-Emphasis LPF faulty or De-Emphasis select switch stays in position **a**.)
Code 112	Suspect Audio Analyzer 2 assembly (high) (Detector Range Amplifier stays at gain=1.)
Code 120	Suspect Audio Analyzer 2 assembly (high) (Peak Detector Select Switch stays in position **a**.)

Table 121 Audio Analyzer 2 Paths Failure Codes (Continued)

Failure Codes	Probable Cause(s)
Code 125	Suspect Audio Analyzer 2 assembly (high) (Pos Peak Detector faulty or DVM Select Switch stays in position **a**.)
Code 127	Suspect Audio Analyzer 2 assembly (high) (Peak Detector Select Switch open.)
Code 128	Suspect Audio Analyzer 2 assembly (high) (Pre-notch RMS Detector faulty or DVM Select Switch stays in position **c**.)
Code 756	Suspect Audio Analyzer 2 assembly (high) (De-emphasis select switch stays in position **b**.)
Code 6912	Suspect Audio Analyzer 2 assembly (high) (Post-Notch Amplifier stays at gain=3.)
Code 12032	Suspect Audio Analyzer 2 assembly (high) (Post-Notch Amplifier stays at gain=30.)
Code 14080	Suspect Audio Analyzer 2 assembly (high) (Post-Notch Amplifier stays at gain=10.)
Code 15360	Suspect Audio Analyzer 2 assembly (high) (Post-Notch amplifier stays at gain=1.)
Code 16128	Suspect Audio Analyzer 2 assembly (high) (Notch Filter, Post-Notch Amplifier, or post-notch RMS Detector faulty or DVM Select Switch stays in position **d**.)
Code 16316	Suspect Audio Analyzer 2 assembly (high) (Detector Range Amplifier stays at gain=30.)
Code 16348	Suspect Audio Analyzer 2 assembly (high) (Detector Range Amplifier stays at gain=10.)
Code 16364	Suspect Audio Analyzer 2 assembly (high) (Detector Range Amplifier stays at gain=3.)
Code 16380	Suspect Audio Analyzer 2 assembly (high) (De-emphasis select switch open or Detector Range Amplifier faulty.)
Code 16382	Suspect Audio Analyzer 2 assembly (high) (Monitor Select Output Amplifier, Monitor Select output LPF, or input select switch faulty.) Or Modulation Distribution assembly (low) (Faulty signal from Monitor Select Multiplexer output.)

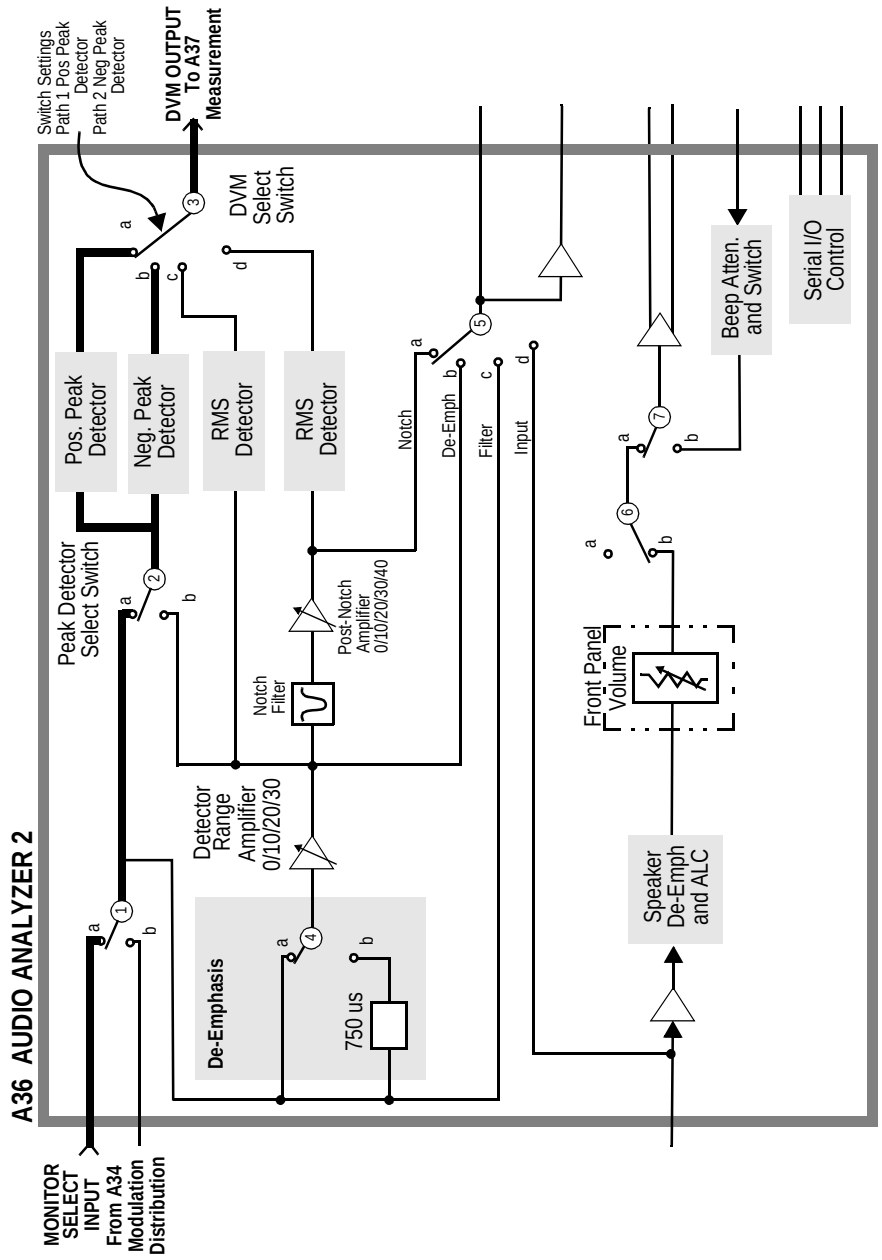


Figure 66 **Audio Analyzer 2 Paths 1 and 2**

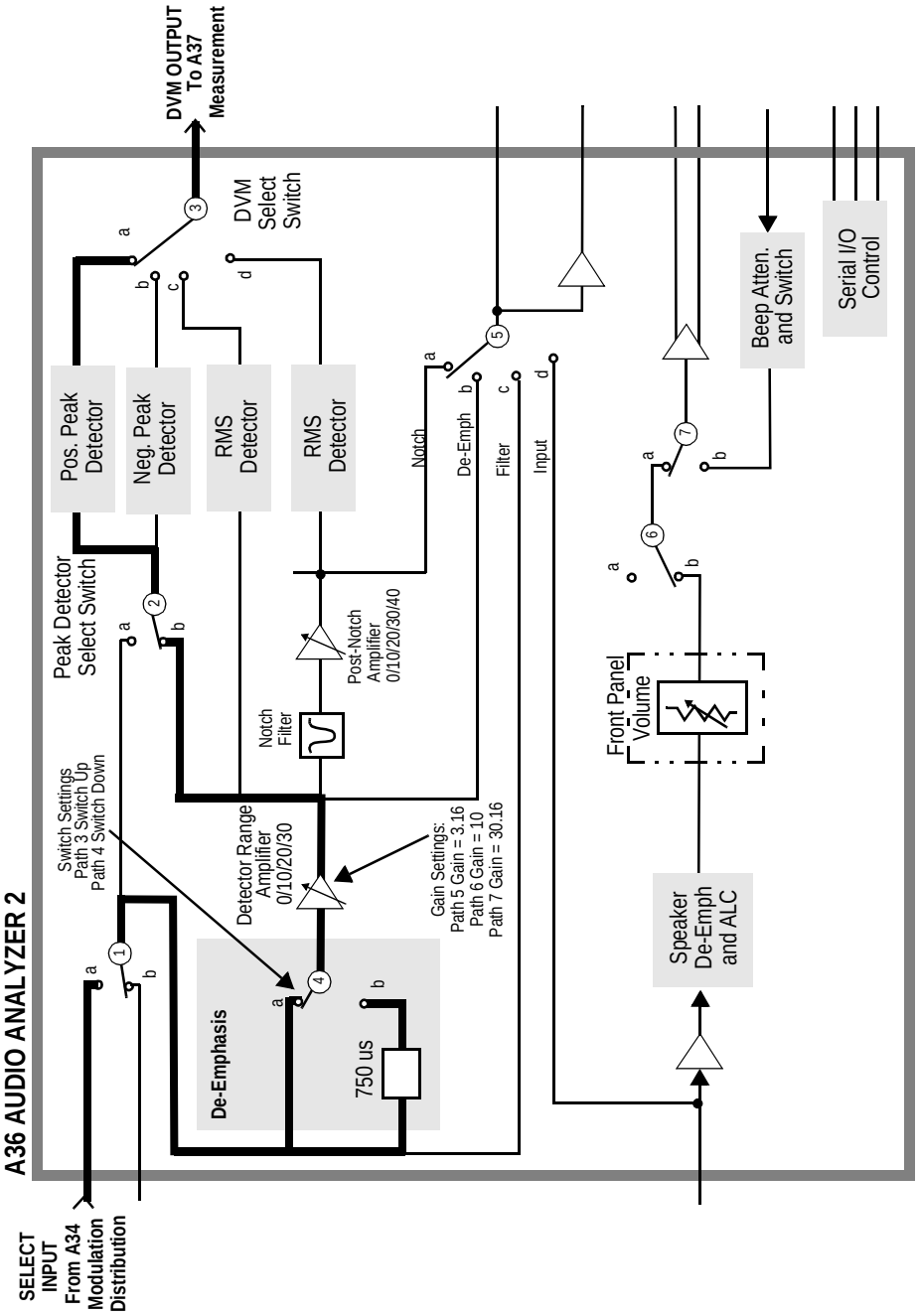


Figure 67 **Audio Analyzer 2 Paths 3 to 7**

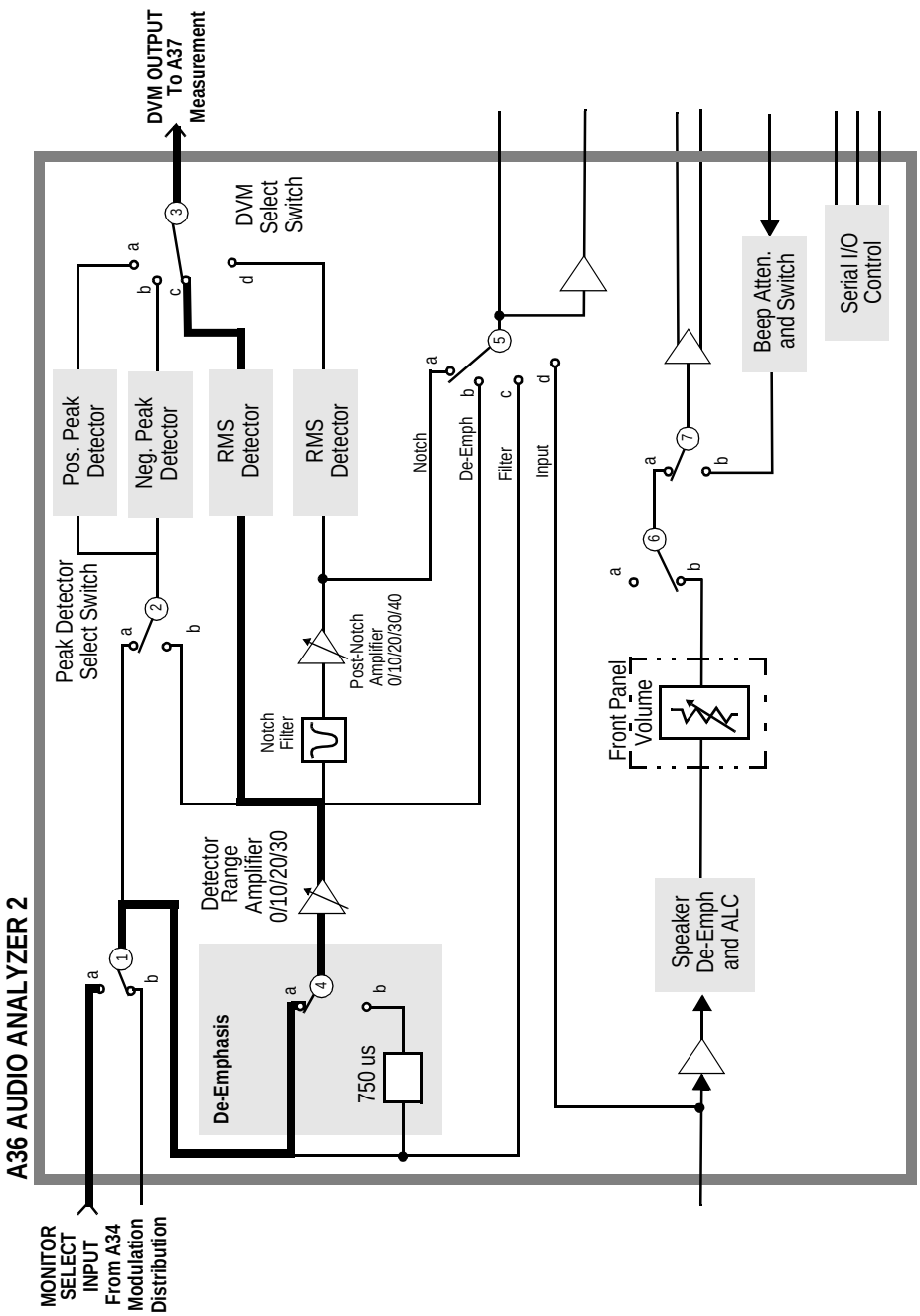


Figure 68 **Audio Analyzer 2 Path 8**

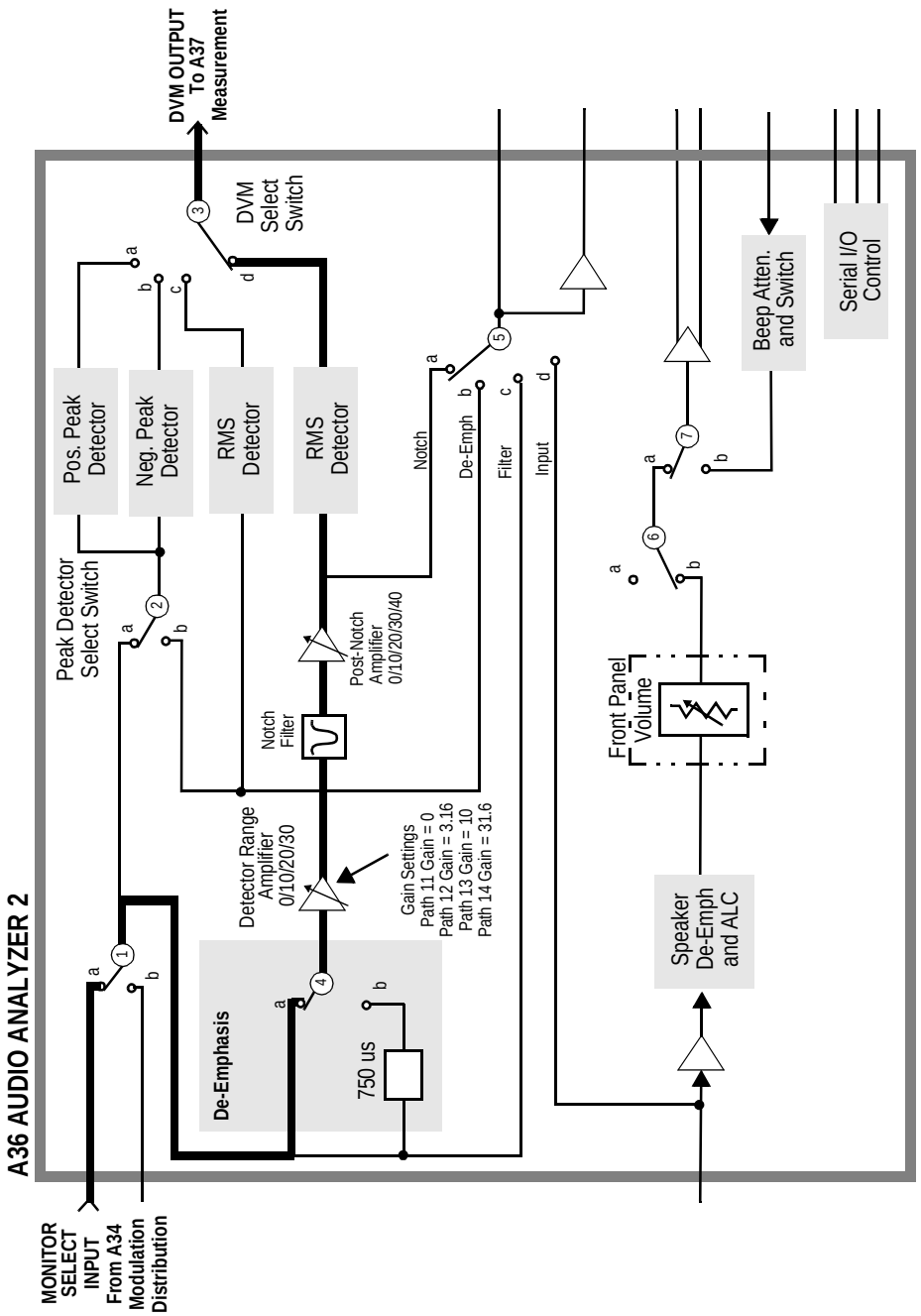


Figure 69 **Audio analyzer 2 Paths 9 to 14**

Description of RF Diagnostics (RFDIAGS3)

Introduction

Unlike the Audio Diagnostics, the RF Diagnostics attempt to determine the faulty assembly when the first failure is noted. For this reason, the tests should be run in order. In the following tables of tests, the measurement point refers to **`Voltmeter Connection`** (DVM), **`Counter Connection`** (Counter), or **`Latch`** (Latch) readings on the SERVICE screen.

Reference Assembly A27

Table 122 A27 Reference Tests

Measurement	Explanation and Suggestions	Measurement Point
10 MHz Lock Detector	The lock detector on the internal 10 MHz reference oscillator is read.	Latch:refs_10MHz_sense
10 MHz Time Base Count	The frequency of the 10 MHz reference is measured by the counter. Since the reference being measured is also the reference for the counter, a valid counter reading indicates only that the counter is functioning but is meaningless as to accuracy. If the counter loses its reference, this measurement will timeout and the diagnostic test will stop. If this happens, trace the 20 MHz signal from P3-13 of the A27 Reference to P3-29 of the A37 Measurement.	Counter:REF_10MHZ
1 GHz Oscillator Lock Detector	The lock detector on the 1 GHz Loop is read.	Latch:refs_1GHz_sense
1 GHz Enabled Output Level	The RF detector on the 1 GHz output with the 1 GHz switch closed is read.	DVM:REF_1GHZ_DIAG
1 GHz Disabled Output Level	Open the switch that routes the 1 GHz signal to the output of the board. The detector is after the switch so it should detect that the signal is no longer there. A long wait is needed before measuring the detector.	DVM:REF_1GHZ_DIAG
500 MHz Output Level	The RF detector on the 500 MHz output is read.	DVM:REF_500MHZ_ DIAG
200 kHz or 1 MHz Output	The Test Set is queried as to whether the reference output is set to 200 kHz or 1 MHz. The 200 kHz or 1 MHz outputs can be turned off by holding the output flip-flops in reset. The output detector is read with the output in the reset condition and in the normal operating condition. (Note: The Latch name is correct despite the “250_kHz” indication.)	Latch:refs_250_kHz_sense
10 MHz Fine and Coarse DACs	It is not possible to actually measure the 10 MHz frequency change caused by changing the DAC setting. Each DAC is set to a low value (0) and a high value (2000), and checked to make sure that the loop stays locked.	Latch:refs_10MHz_sense

Signal Generator Synthesizer A24

Table 123 A24 Signal Generator Synthesizer Tests

Measurement	Explanation and Suggestions	Measurement Point
Reference Detector (Ref present)	The reference present detector is read with the 200 kHz reference signal enabled. If this measurement fails, trace the 200 kHz signal from P3-1 of the A27 Reference to P3-3 of the A24 Signal Generator Synthesizer.	Latch:gsyn_ref_not_present_sense
Out-of-Lock Detector (Locked)	The Out-of-Lock Detector is read with the loop set to be locked.	Latch:gsyn_out_of_lock_int_sense
Reference Detector (Reference NOT present)	The reference-present detector is read with the 200 kHz the Reference signal disabled at the Reference assembly.	Latch:gsyn_ref_not_present_sense
Out-of-Lock Detector (NOT locked)	The out-of-lock detector at the Reference assembly. This should cause the loop to be out of lock.	Latch:gsyn_out_of_lock_int_sense
Frequency Range	The 200 kHz Reference is enabled at the Reference assembly. Then the frequency of this loop is incriminated from 500 to 1000 MHz in 50 MHz steps. The out-of-lock detector is read at each step.	Latch:gsyn_out_of_lock_int_sense

Receiver Synthesizer A28

Table 124 A28 Receiver Synthesizer Tests

Measurement	Explanation and Suggestions	Measurement Point
Reference Detector (Ref present)	The reference-present detector is read with the 200 kHz reference signal enabled. If this measurement fails, trace the 200 kHz signal from P3-2 of the A27 Reference to P3-3 of the A28 Receiver Synthesizer.	Latch:rsyn_ref_not_present_sense
Out-of-Lock Detector (Locked)	The out-of-lock detector is read with the loop set to be locked.	Latch:rsyn_out_of_lock_int_sense
Reference Detector (Reference NOT present)	The reference-present detector is read with the 200 kHz Reference signal disable data the Reference assembly.	Latch:rsyn_ref_not_present_sense
Out-of-Lock Detector (NOT locked)	The out-of-lock detector is read with the 200 kHz Reference disabled at the Reference assembly. This should cause the loop to be out of lock.	Latch:rsyn_out_of_lock_int_sense
Frequency Range	The 200 kHz reference is enabled at the Reference assembly. Then the frequency of this loop is incremented from 500 to 1000 MHz in 50 MHz steps. The out-of-lock detector is read at each step.	Latch:rsyn_out_of_lock_int_sense

Output A26

Table 125 A26 Output Tests

Measurement	Explanation and Suggestions	Measurement Point
+8 V Power Supply	The +8 Vdc supply generated on the Output assembly is measured. The voltage measured by the DVM is the actual voltage divided-by-2.	DVM:OUT_POS_8V
– 6 V Power Supply	The –6 Vdc supply generated on the Output assembly is measured. The voltage measured by the DVM is the actual voltage divided-by-2.	DVM:OUT_NEG_6V
Amplifier Bias Voltage	The bias voltage is measured on the output amplifier.	DVM:OUT_AMP_BIAS
Carrier Level DAC	The carrier level DAC is checked by turning on each bit, one at a time, and measuring the voltage output with each bit turned on. It is also checked with all bits on. The limits are calculated based on the actual voltage measured for the –6 V supply in a previous test. The bit value (B) is calculated as (–6 V actual) × 4 ÷ 6 ÷ 4096.	DVM:OUT_LEVEL_REF
Filter Tune DAC	The Filter Tune DAC is checked by turning on each bit one at a time and measuring the voltage output with each bit turned on. It is also checked with all bits on. The limits are calculated based on the actual voltage measured for the –6V supply in a previous test. The bit value (B) is calculated as -1 × (–6 V actual) × 2 × 422 ÷ 984 ÷ 4096.	DVM:OUT_TUNE_FILTER
Open Loop ALC Drive	This test opens the ALC Loop and checks that the voltage from the Level DAC appears at the modulator, input. The carrier level DAC is set to 4095 (full scale). The nominal output of the DAC (Ref) is calculated based on the actual voltage measured for the –6 V supply in a previous test. Ref = –1 × (–6 V actual) × 4 ÷6 × 100 ÷ 75 × 4095 ÷ 4096.	DVM:OUT_ALC_DRIVE

Table 125 A26 Output Tests (Continued)

Measurement	Explanation and Suggestions	Measurement Point
Output Detector, Detector Caps	The detector is checked with the carrier level DAC at a high level (4000). Then the detector caps are switched in separately and together. The detector's voltage should not change as the caps are switched in and out. If the jumper coax between the output of the signal generator's Synthesizer and the input to the output section fails, the detector capacitors test will fail. This is a rather common failure.	DVM:OUT_OUTPUT_ LEVEL
Output Detector, Low Level	The carrier-level DAC is set to a low level (0) so there should be no RF signal reaching the RF detector.	DVM:OUT_OUTPUT_ LEVEL
Output Frequency Range, Loop Closed	The ALC loop is closed and the signal generator Synthesizer's frequency is set to all values from 1 to 1001 MHz in 100 MHz steps. The detector voltage is measured at each frequency.	DVM:OUT_OUTPUT_ LEVEL
Bandwidth Control	The bandwidth control bits are set to all combinations. This should not change the output level.	DVM:OUT_OUTPUT_ LEVEL
Tracking Filter Rejection	The ALC loop is opened and the tracking filters are checked by setting the RF frequency to the center of the 2 bands (375 and 750 MHz) that use these filters. Then the filter DAC is changed to tune the filters below the RF frequency. The RF level as measured by the output detector should be close to zero.	DVM:OUT_OUTPUT_ LEVEL

Input A5

Refer to **figure 70, "Input Tests: Duplex Detector, RF Detector, and Step Attenuator," on page 590** and **figure 71, "Input Tests: Ant, O/P Filter & Atten, Autorange Atten, Counter, Temp Sensor," on page 591** for signal flow and measurement points for the various measurement described in **table 126**.

Table 126 A5 Input Tests

Measurement	Explanation and Suggestions	Measurement Point
Duplex Detector (No Signal)	See Path 1, Node 1 in **figure 70 on page 590**. The signal from the signal generator synthesizer is set to 750 MHz at >+10 dBm. The step attenuator is set to zero attenuation. The duplex switch is set so this internal signal does NOT go to the detector on the duplex input so the detector should read close to zero. If this test fails, it could be that a signal is being applied to the front-panel BNC connector. A cable hanging from the DUPLEX IN connector can cause a failure.	DVM:DUPLEX_DET
Duplex Detector (Signal Present)	See Path 2, Node 1 in **figure 70 on page 590**.The duplex switch is changed so the internal signal is applied to the duplex detector. The detector should read the signal level.	DVM:DUPLEX_DET
RF Detector (Low Power), No Signal	See Path 2, Node 2 in **figure 70 on page 590**. The low power RF detector is checked with no signal present. The duplex switch from the previous test is not letting the signal reach the RF detector.	DVM:RF_PK_DET_LOW
RF Detector (Low Power), Signal Present	See Path 1, Node 2 in **figure 70 on page 590**. The duplex switch is changed to route the signal to the RF detector.	DVM:RF_PK_DET_LOW
RF Detector (High Power), No Signal	See Path 2, Node 3 in**figure 70 on page 590**. The high power RF detector is checked with no signal present. The duplex switch is set so it does not let the signal reach the RF detector.	DVM:RF_PK_DET_HIGH
RF Detector (High Power), Signal Present	See Path 1, Node 3 in **figure 70 on page 590**. The duplex switch is changed to route the signal to the RF detector.	DVM:RF_PK_DET_HIGH

Table 126 A5 Input Tests (Continued)

Measurement	Explanation and Suggestions	Measurement Point
Step Attenuator	See Path 1, Node 2 in **figure 70 on page 590**. The step attenuator is checked by switching-in one pad at a time. The limits are set in terms of the no signal (RF Detector (Low Power), No Signal) reading obtained in the test and the difference between the readings obtained in the previous RF Detector (Low Power) Signal Present and No Signal tests.	DVM:RF_PK_DET_LOW
Antenna Input Detector	See Path 3, Node 4 in **figure 71 on page 591**. The antenna input detector cannot read the internal signal level in the Input module. It is read anyway to be sure it is zero. If the test fails it could be because there is a signal being applied to the front-panel **ANT IN** connector.	DVM:ANTENNA_DET
Filter Output Detector, No Signal	See Path 3, Node 5 in**figure 71 on page 591**. All the switches that connect the signal to the Receiver's output EXCEPT the antenna switch are set. Thus, there is NO signal yet on the filter output detector. The detector should read zero.	DVM:FILTER_OUT_DET
Filter Output Detector, Signal Present	See Path 4, Node 5 in **figure 71 on page 591**. The filters are checked by setting the RF Analyzer and RF source to the same frequencies (1, 100,300, 600, 800, 1000 MHz). The frequencies are selected so each filter is checked. Setting the analyzer frequency's sets the right filter.	DVM:FILTER_OUT_DET
Output Filter Rejection	See Path 4, Node 5 in **figure 71 on page 591**. Each filter is checked to see that it rejects signals outside of its passband. The filter is selected using the analyzer's frequency command.	DVM:FILTER_OUT_DET
Output Variable Attenuator	See Path 4, Node 5 in **figure 71 on page 591**.The variable attenuator is checked by programming the DAC to full scale and reading the voltage on the output detector. Then the DAC is programmed to values which turn on the 5 most significant bits, 1 bit at a time, starting with the MSB. In each case the output detector is measured and checked to see if the voltage is less than the previous reading (last).	DVM:FILTER_OUT_DET

Table 126 A5 Input Tests (Continued)

Measurement	Explanation and Suggestions	Measurement Point
Auto Range Attenuator	See Path 4, Node 5 in**figure 71 on page 591**. The Auto Range Attenuator is programmed to its 3 possible values (+20 dB, 0 dB and -20 dB). At each setting the output detector is read.	DVM:FILTER_OUT_DET
Counter with TTL Divider	See Path 4, Node 6 in **figure 71 on page 591**. The signal from the signal generator's synthesizer is routed to the counter TTL prescaler. The frequency of the signal is set to all values between 1 and 51 MHz in 5 MHz steps. The count returned is the actual frequency in kHz, divided-by-16.	Counter:INPUT_TTL_COUNT
Counter with ECL Divider	See Path 4, Node 7 in **figure 71 on page 591**. The signal from the signal generator's synthesizer is routed to the counter's ECL prescaler. The frequency of the signal is set to all values between 50 and 1000 MHz in 50 MHz steps. The count returned is the actual frequency in kHz, divided-by-256.	Counter:INPUT_ECL_COUNT
Temperature Sensor	See Node 8 in **figure 71 on page 591**. The Temperature Sensor produces a DC voltage proportional to the internal temperature. The scale factor is 10 mV/°C	DVM:TEMP_SENSE

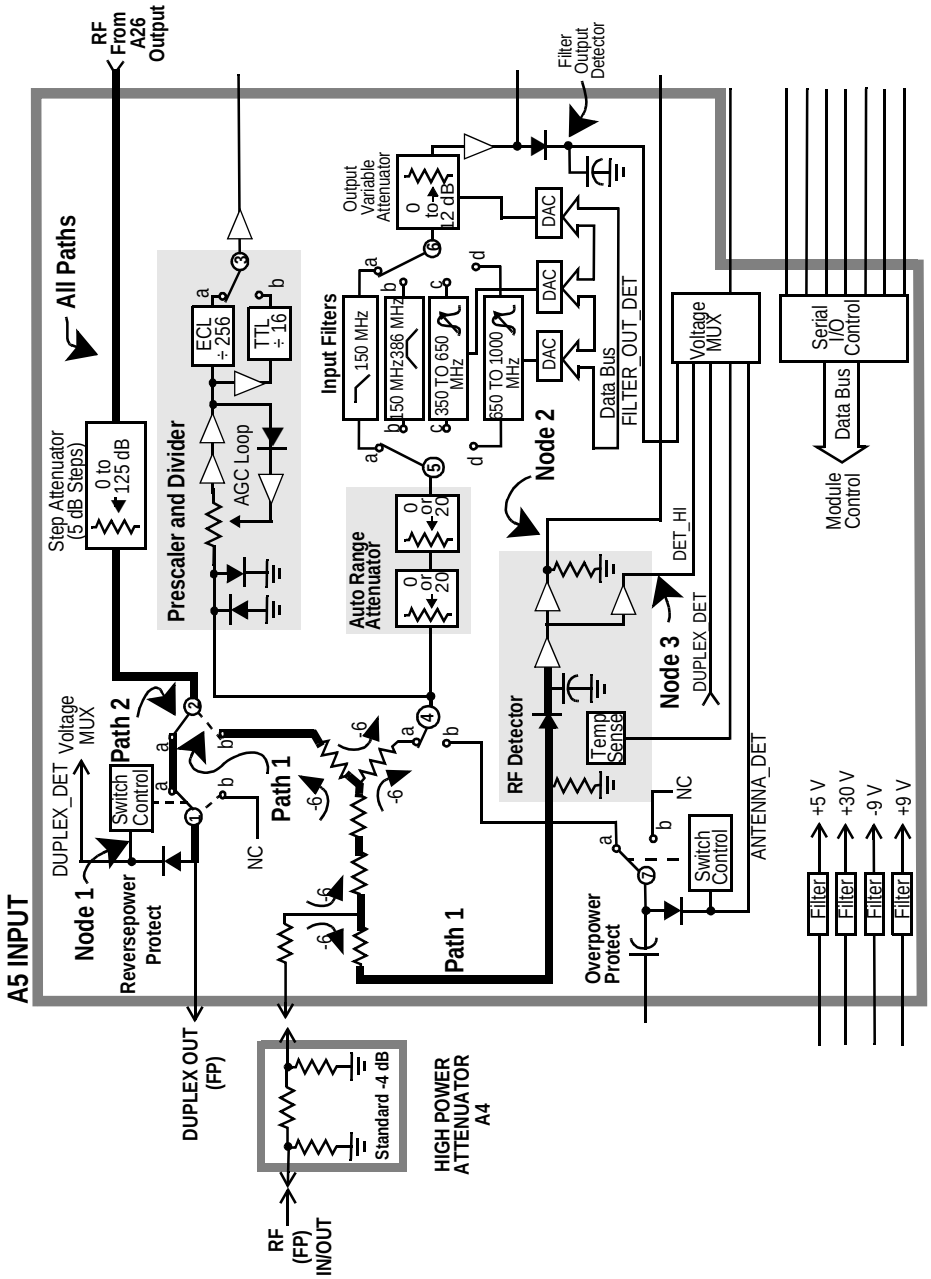


Figure 70 **Input Tests: Duplex Detector, RF Detector, and Step Attenuator**

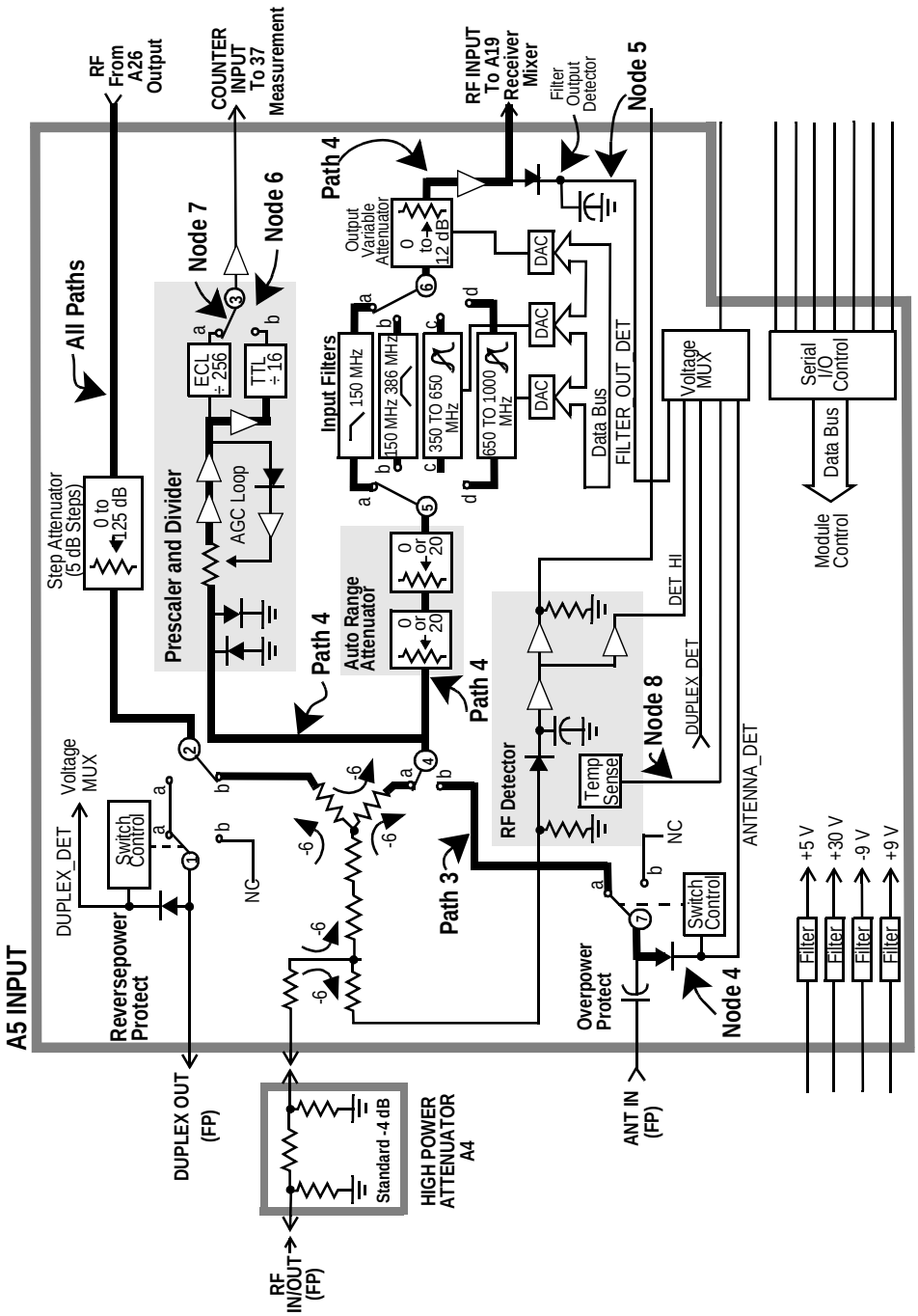


Figure 71 **Input Tests: Ant, O/P Filter & Atten, Autorange Atten, Counter, Temp Sensor**

Spectrum Analyzer Tests A32

Table 127 A32 Spectrum Analyzer Tests

Measurement	Explanation and Suggestions	Measurement Point
Detector Output, No Signal	The signal generator's signal is routed to the spectrum analyzer, but the level is set to −100 dBm at the **RF IN/OUT** connector which produces a very small signal at the spectrum analyzer. The spectrum analyzer's detector should produce just an off-set voltage.	DVM:SCOPE2
Stepped Gain	Using the spectrum analyzer's internal calibration signal (110 MHz), the stepped-gain amplifiers are checked. Each gain step is turned on one step at a time. The sensitivity of the detector varies from 24 mV/dB to 6 mV/dB at the levels where the internal calibration signal could be. 3 dB of gain error is allowed for the steps. If this measurement fails, trace the 20 MHz signal from P3-9 of the A27 Reference to P1-3 of the A32 Spectrum Analyzer.	DVM:SCOPE2
IF Band Width	The IF bandwidth is set to all possible values. The spectrum analyzer LO is moved in increments of 10% of the bandwidth of the filter being tested to find a signal within each filter. The voltage read by the detector should be basically the same as the full scale reading (0 dB) in the stepped gain test above.	DVM:SCOPE2
Filter Rejection	The LO's frequency is set 10 × BW away from the normal center of each filter. Then the detector is read. The level at the detector should be low. A 0.55 V change is equivalent to a 27.5 dB change in signal level.	DVM:SCOPE2
Variable Gain IF Amplifier	The variable-gain IF amplifier is checked by turning on one bit at a time, the DAC which controls it. The least-significant bit is turned on first.	DVM:SCOPE2

Table 127 A32 Spectrum Analyzer Tests (Continued)

Measurement	Explanation and Suggestions	Measurement Point
RF Input Signal	The internal calibration signal is disabled and the input signal path from the Receiver is enabled. The signal generator's synthesizer and the RF analyzer are set to 100 MHz. This provides an IF of 114.3 MHz at the input to the spectrum analyzer. The level is set so that the level at the RF IN/OUT connector is equivalent to – 120 dB at the **ANT IN** connector. This should produce a DVM reading of 1.892 Vdc from the spectrum analyzer's detector. Limits of ± 0.200 V are used which is equivalent to approximately a 10 dB variation in signal level. For newer Test Sets, additional measurements are made by setting a reference level then dropping the level 10, 2, and 1 dB with the vertical sensitivity set to 10, 2, and 1 dB/division respectively.	DVM:SCOPE2

Receiver A30

Refer to **table 72 on page 596** for signal flow of the measurements described in **table 128**.

Table 128 A30 Receiver Tests

Measurement	Explanation and Suggestions	Measurement Point
Down Converter	See **figure 72 on page 596**. The internal RF generator frequency, set to 100 MHz and –46 dBm CW, is fed into the first mixer (where it is downconverted to the 614.3 MHz IF) and the receiver (where it is downconverted to the 114.3 MHz IF). The IF is then fed into the LO/IF/Demod and then to the spectrum analyzer. The test is repeated for 500 MHz and 900 MHz. Failures occurring in this test are inconclusive. Failures may be due to the receiver's first mixer, the receiver, the LO/IF/Demod, or the spectrum analyzer.	Spectrum Analyzercenter frequency
IF Counter	See **figure 73 on page 597**. The internal RF generator is set to 100 MHz CW and fed into the receiver's input. The IF frequency is measured by the IF counter. The IF chain must operate properly through the FM demodulator for this test to pass. (If the spectrum analyzer option is not installed, this becomes the first test.)	Counter:REC_IF_COUNT
FM	See **figure 74 on page 598**. The internal RF generator is set for FM at 10 kHz peak deviation and a 1 kHz rate. The peak deviation is measured by the receiver. This is the first test in which the internal audio source is applied to the signal generator synthesizer's FM modulator. If all the Audio Diagnostics run with no failures but this and/or the next test fails, check the path of the audio source from the output of the Modulation Select Multiplexer switch on the A34 Modulation Distribution assembly to the A24 Signal Generator Synthesizer's input.	DVM:POS_PK_DET
FM Inverted	See **figure 74 on page 598**. Same as previous test except the demodulated FM is inverted.	DVM:POS_PK_DET

Table 128 A30 Receiver Tests (Continued)

Measurement	Explanation and Suggestions	Measurement Point
Squelch	See**figure 75 on page 599** . The internal RF generator is set for FM at 10 kHz peak deviation and 1 kHz rate. The RMS deviation is measured under the following four conditions. (High level is –80 dBm; lowlevel is –127 dBm.) Condition 1 - RF generator level high, squelch fixed. Condition 2 - RF generator level low, squelch fixed. Condition 3 - RF generator level high, squelch open. Condition 4 - RF generator level low, squelch open.	DVM:PRE_NOTCH_RMS
ALC On	See **figure 76 on page 600**. The internal RF generator is set to CW. The receiver is set to measure AM. The ALC level is measured.	DVM:DC_AUDIO
ALC Off	See **figure 76 on page 600**. Same as previous test except ALC is set to off.	DVM:DC_AUDIO
AM	See **figure 77 on page 601**. The internal RF generator is set for AM at 50% and a 1 kHz rate. The AM depth is measured by the receiver. This is the first test in which the internal audio source is applied to the Output section's AM modulator. If all the Audio Diagnostics run with no failures but this test does fail, check the path of the audio source from the output of the Modulation Select Multiplexer switch on the A4 Modulation Distribution assembly to the A13 Output section's AM input.	DVM:POS_PK_DET
SSB Level	See **figure 78 on page 602**. The internal RF generator is set to 100.001 MHz CW. The receiver is tuned to 100 MHz. The output of the SSB demodulator is the difference frequency, 1 kHz.	DVM:PRE_NOTCH_RMS
SSB Frequency	See **figure 78 on page 602**. Same as previous test except the frequency (1 kHz) is measured.	Counter:AUD1_COUNT

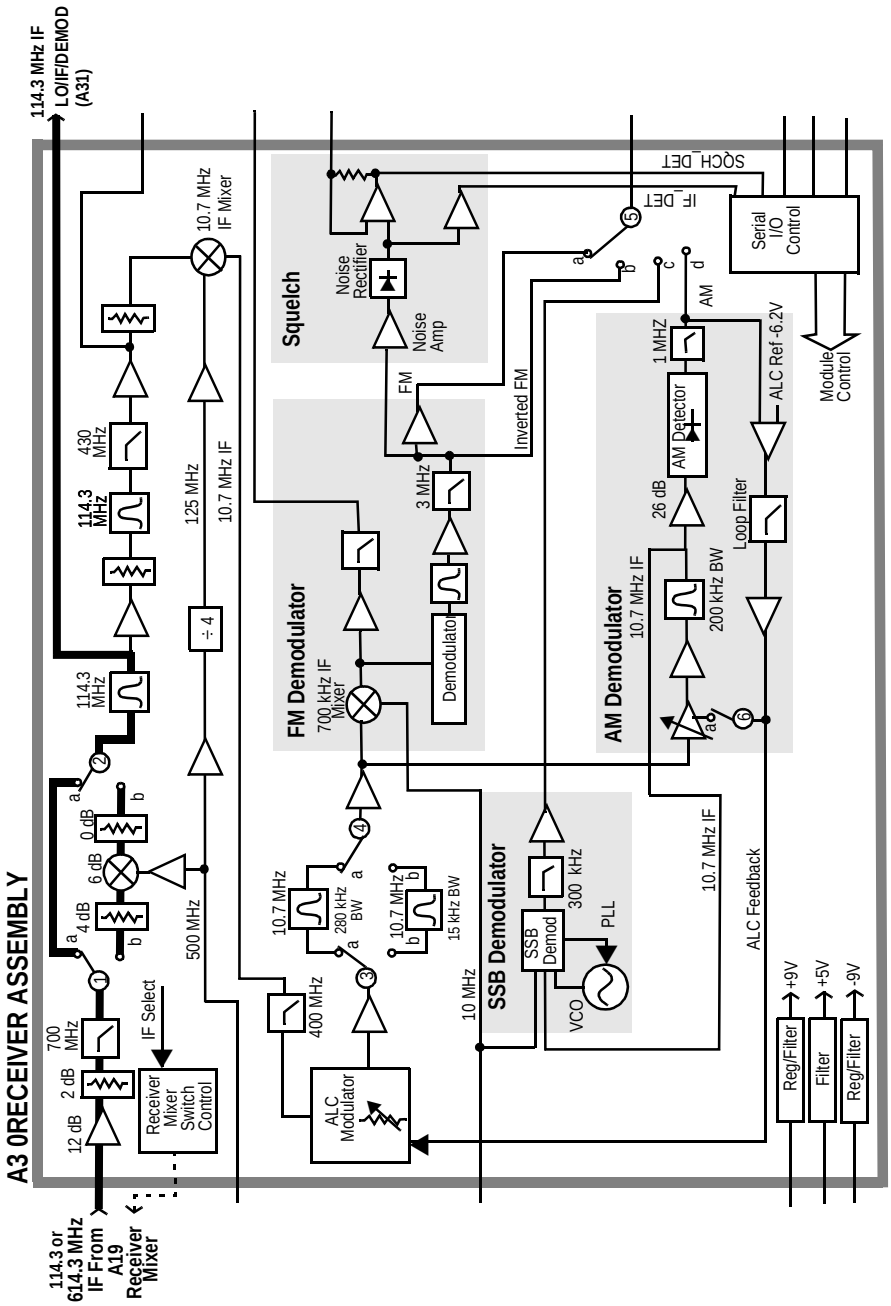


Figure 72 Receiver Tests_Down Converter

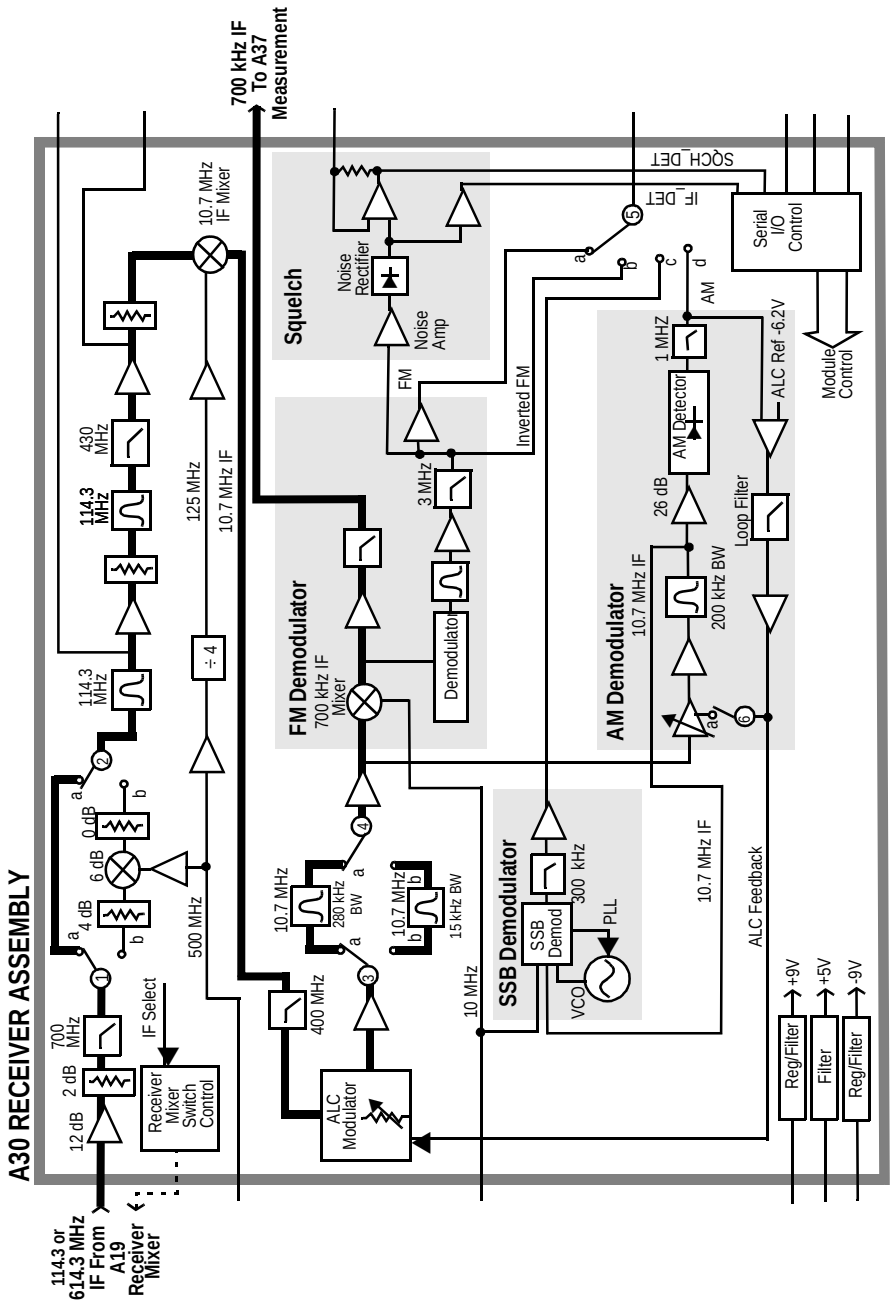


Figure 73 **Receiver Tests_IF Counter**

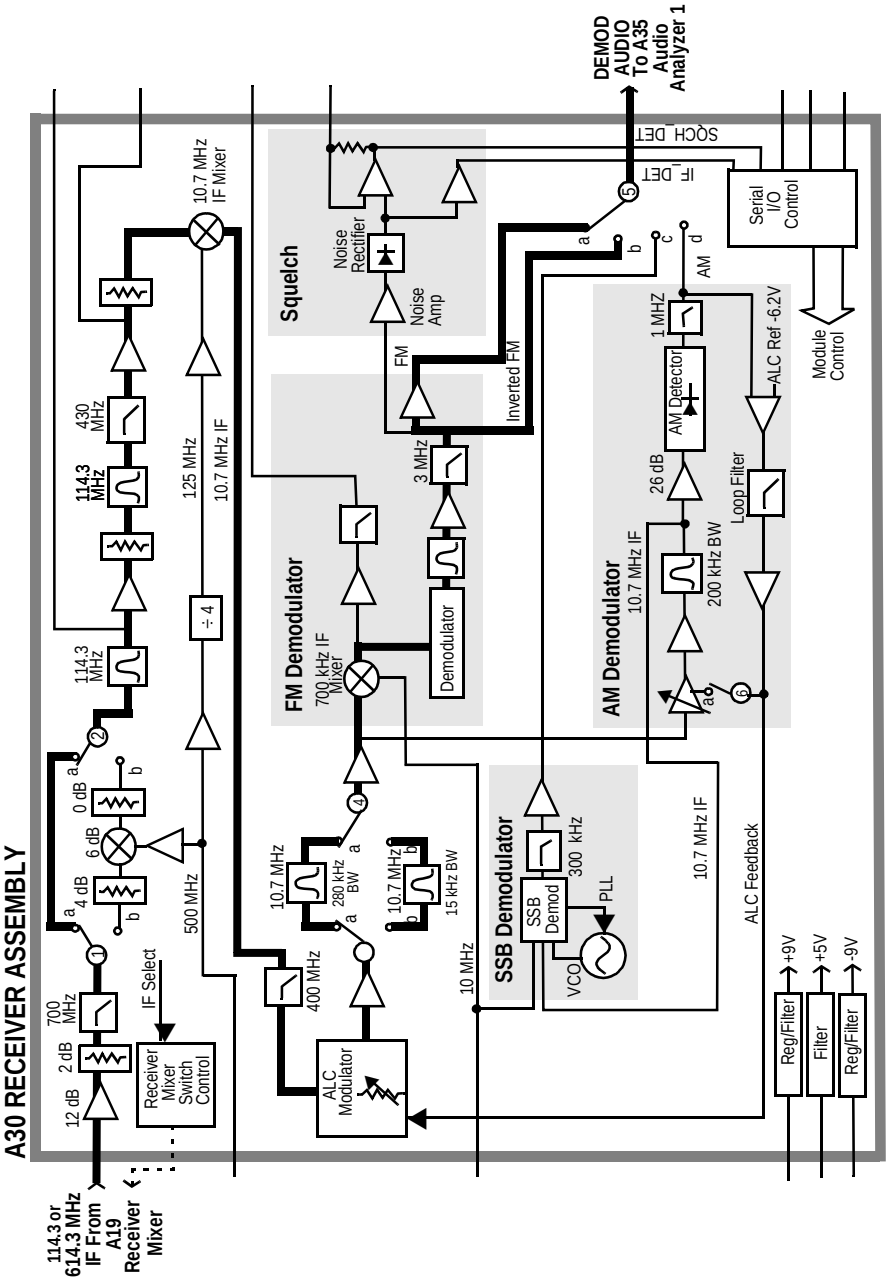


Figure 74 **Receiver Tests_FM**

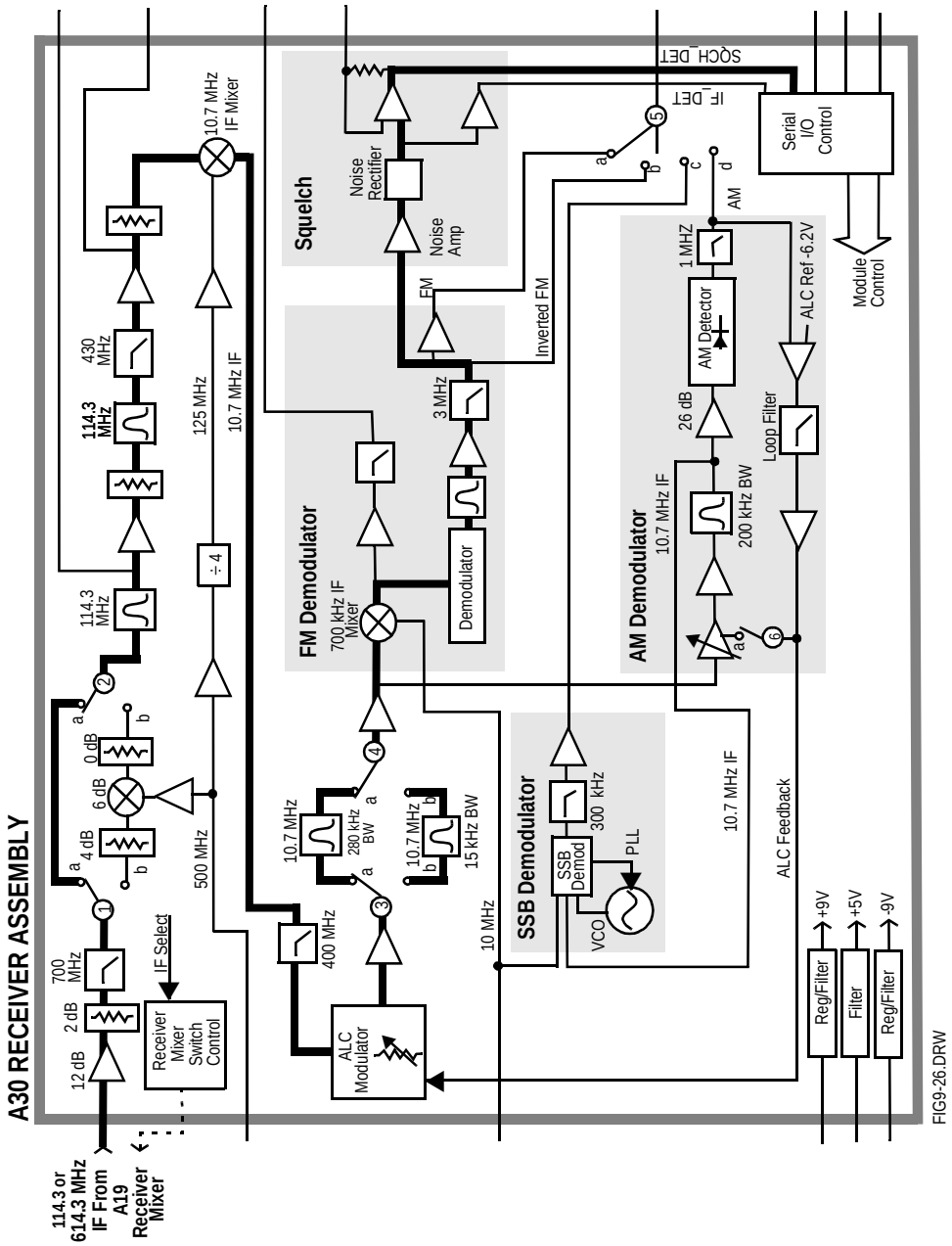


Figure 75 **Receiver Tests_Squelch**

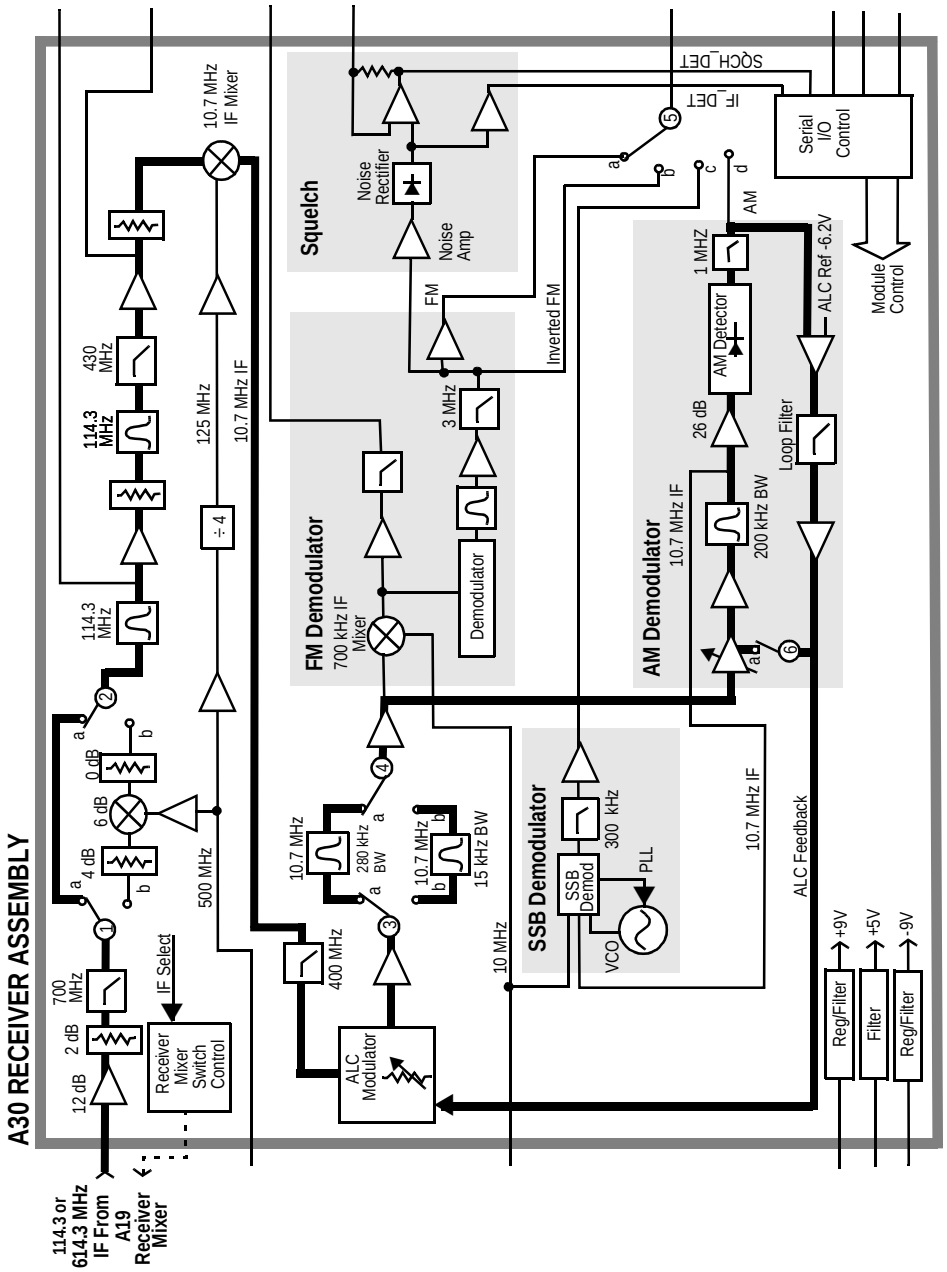


Figure 76 **Receiver Tests_ALC**

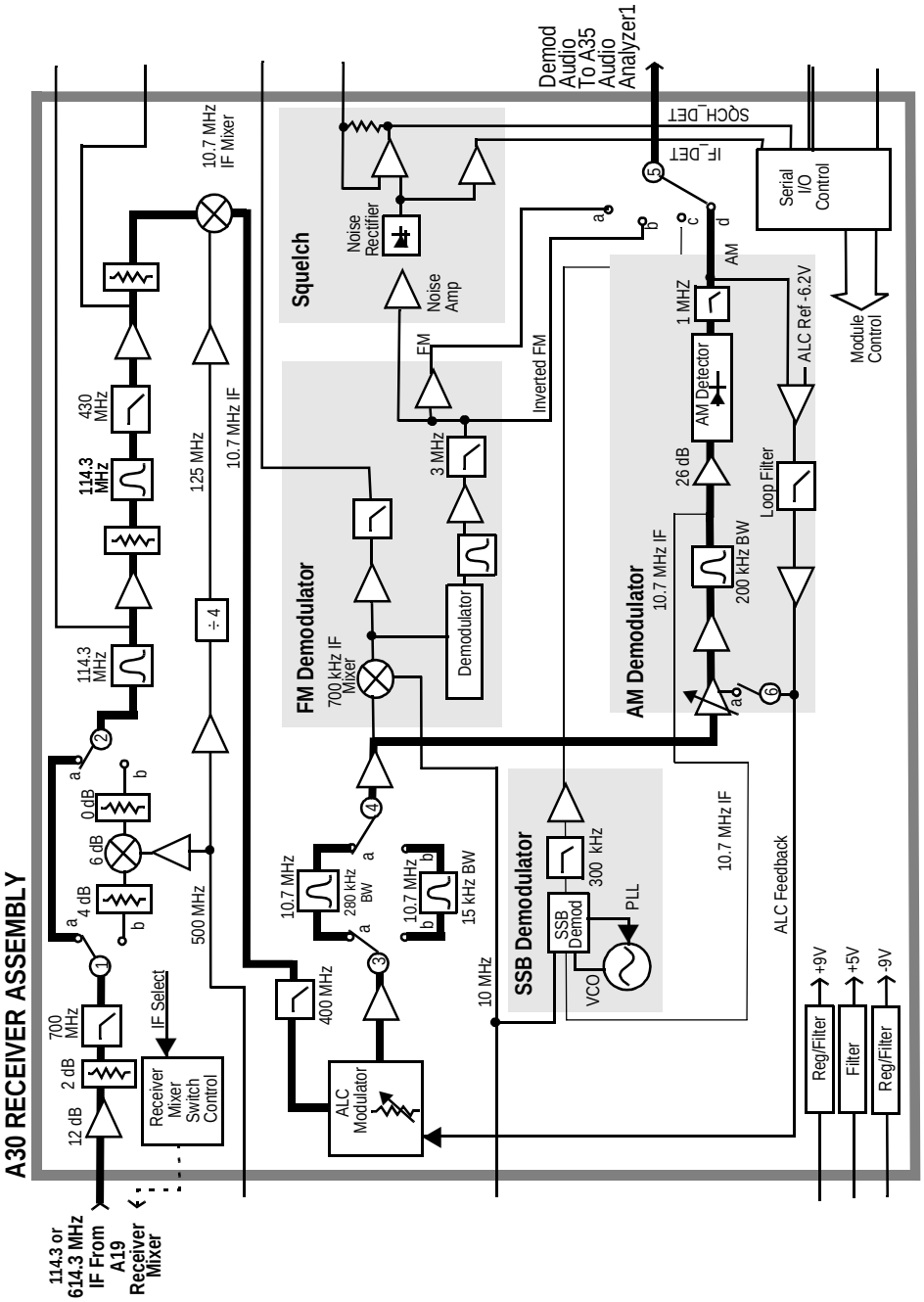


Figure 77 Receiver Tests_AM

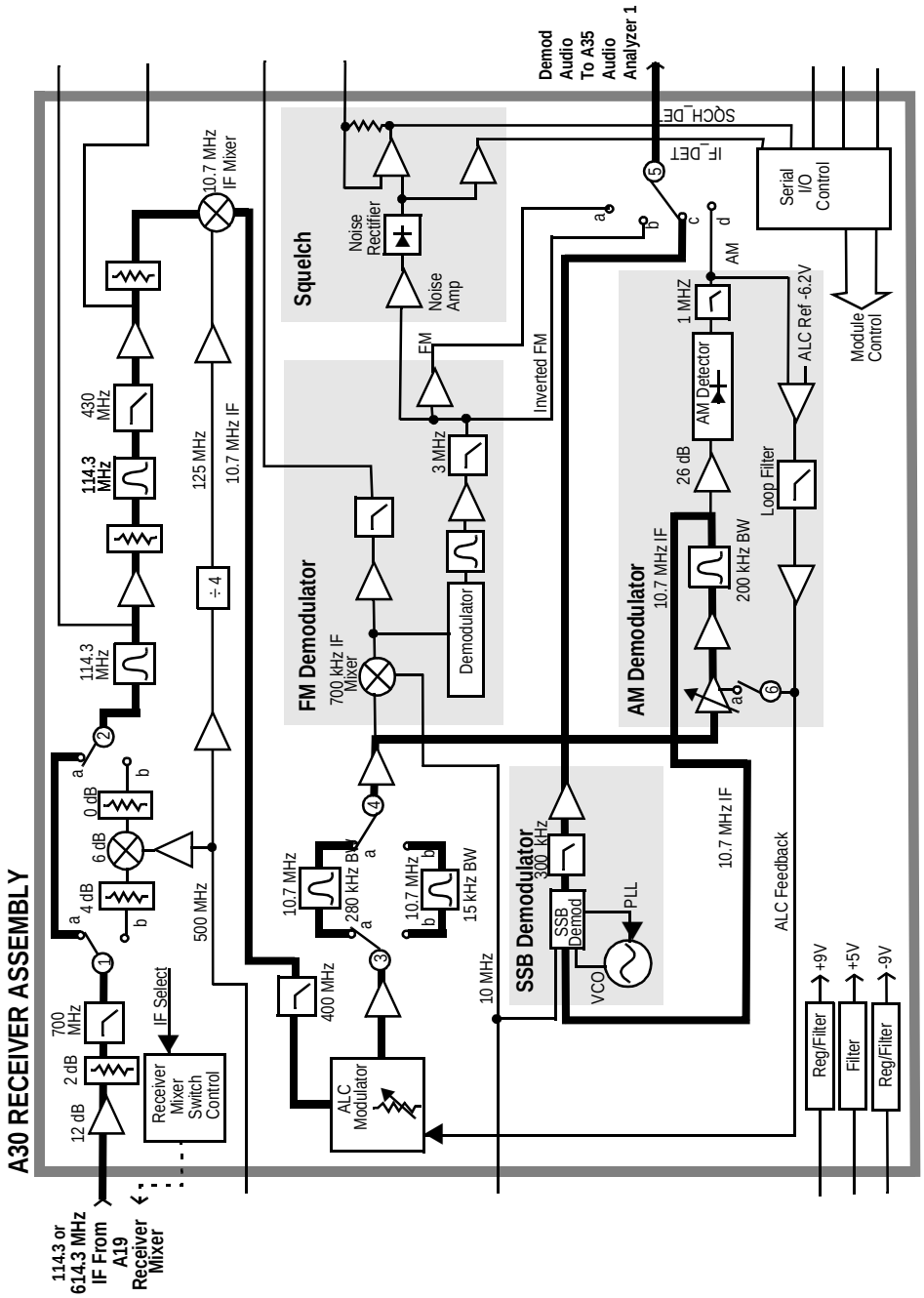


Figure 78 Receiver Tests_SSB

Description Of Miscellaneous Diagnostics (MSDIAGS3)

Introduction

The Miscellaneous Diagnostics are varied and cannot be run in a loop. In the following tables of tests, the measurement point refers to **`Voltmeter Connection (DVM)`** or **`Latch`** (Latch) readings on the SERVICE screen.

CYCLE POWER AFTER THE SELF-TEST!

The Self-Test diagnostic turns off the CDMA timing clocks *when run as part of the MSDIAGS3 diagnostics*. This prevents ALL CDMA-related modules from operating properly until the clocks are restored. After running the Self-Test, cycle Test Set power to restore the CDMA clocks.

External Reference Test

Table 129 External Reference Test

Measurement	Explanation and Suggestions	Measurement Point
Ext Reference Present Detector	This test requires that an external reference signal be connected to the **10 MHz REF INPUT** (rear panel). The external reference sensor is checked.	Latch:refs_ext_ref_sense
Ext Reference Lock Detector	This test requires that an external reference signal be connected to the **10 MHz REF INPUT** (rear panel). The 10 MHz loop lock sensor is checked.	Latch:refs_10MHz_sense
Ext Reference Lock-out	The external reference can be locked out. The external reference sensor should not detect a signal if the lock-out works.	Latch:refs_ext_ref_sense

RF Input/Output Test

Table 130 RF Input/Output Test

Measurement	Explanation and Suggestions	Measurement Point
Duplex Out to RF In/Out	The RF Generator is set to 100 MHz at –100 dBm to the **DUPLEX OUT**. The user must connect a cable from the **DUPLEX OUT** to the **RF IN/OUT** connector. The power meter is zeroed. Then the RF generator's amplitude is set to +10 dBm and the power meter is read.	HP-IB "MEAS:RFR:POWER?" statement
Duplex Out to Ant In	The RF generator is set to 100 MHz at +10 dBm to the **DUPLEX OUT**. The user must connect a cable from the DUPLEX OUT to the ANT IN connector. The signal is routed to the filter out detector in the input section.	DVM:FILTER_OUT_DET

Self-Test

Table 131 Self-Test

Measurement	Explanation and Suggestions	Measurement Point
Instrument Self-Test	The HP-IB command, *TST?, is sent to the instrument. The instrument responds with a result in the range, 0 to 4094. If the result is not zero, then one or more instrument self tests failed. Individual bits in the result are set to 1 to indicate that certain tests failed. The program decodes the bits that are set and prints a message for each bit that is set to 1. The messages are listed below. See Description of *Self-Test Diagnostic* earlier in this chapter. 1: Microprocessor Failure 2: ROM Failure 3: Standard RAM Failure 4: Option RAM Failure 5: Timer Failure 6: Real Time Clock Failure 7: Keyboard (stuck Key) Failure 8: RS-232 Failure 9: Serial Comm Failure 10: Signaling Failure 11: CRT Controller Failure 12: Misc Hardware Failure	
Power Supplies On :Power Supply, +5.1 V	Reads the actual +5.1 V power supply voltage on the Measurement Board.	DVM:MEAS_5V_REF
Power Supplies On :Power Supply, +12.37 V	Reads the divided +12.37 V power supply voltage on the Measurement Board.	DVM:MEAS_12V_REF
Power Supplies On :Power Supply, +41.5 V	Reads the divided +41.5 V power supply voltage on the Measurement Board.	DVM:MEAS_38V_REF
Power Supplies On :Power Supply, –12.37 V	Reads the divided – 2.37 V power supply voltage on the Measurement Board.	DVM:MEAS_NEG_12V _REF
Power Supplies On :Power Supply, +12.00 V	Reads the divided +12.00 V power supply voltage on the Measurement Board.	DVM:PS_12V_AUX

Description of the Digital Assembly Diagnostics (CDMADIAG)

Introduction

The Digital Diagnostics test the assemblies required for CDMA-formatted IQ modulation.

These assemblies include:

- CDMA Reference (A29)
- LO/IF Demod (A31)
- I/Q Modulator (A25)
- Cell Site Analog (A8)

The CDMA Reference, LO/IF Demod, and I/Q Modulator are also used when generating or analyzing analog signals. Refer to , to see how these modules are used.

Table 132 CDMA Reference

Measurement	Explanation and Suggestions	Measurement Point
20.00 MHz VCXO Tune Voltage	The 20.00 MHz Voltage Controlled Crystal Oscillator (VCXO) provides the 10 MHz reference for the Reference and LO/IF/Demod assemblies.	CREF_SYNTH_TB_TUNE
20.00 VCXO Reference Lock	The phase-locked loop detector voltage comes from the cathode of the out-of-lock LED. With the VCXO locked, this point should measure about 4.9 V. When unlocked, this line is pulled low, lighting the LED.	CREF_REF_LOCK
19.6608 MHz VCXO Tune Voltage	The 19.6608 MHz VCXO furnishes clock signals to several CDMA assemblies.	CREF_CDMA_TB_TUNE
19.6608 MHz VCXO Reference Lock	The phase-locked loop detector voltage comes from the cathode of the out-of-lock LED. With the VCXO locked, this point should measure about 4.9 V. When unlocked, this line is pulled low, lighting the LED.	CREF_CDMA_LOCK
AWGN I & Q Out Sense	The outputs of the Additive White Gaussian Noise source for the I and Q signals are measured at off, low, medium, and high levels.	CREF_I_NOISE_S CREF_Q_NOISE_S
AWGN Source Sense	The Gain High pins of the two AWGN amplifiers are monitored at off, low, medium, and high levels.	CREF_I_GAIN_S
CDMA Reference Ground	The ground potential of the CDMA Reference Assembly is measured.	CREF_GND

Table 133 LO/IF/Demodulator

Measurement	Explanation and Suggestions	Measurement Point
LO VCO/ Integrator Bias Voltage	This point measures the bias voltage to the 117.9864 MHz Voltage Controlled Oscillator used to downconvert the 114.3 MHz IF to 3.6864 MHz.	LOIF_VB_S
LO VCO Tune Voltage	This point measures the integrated tune voltage out of the LO phase detector.	LOIF_VT_LO
LO Output Sense	This point measures the filtered output of the LO's RF amplifier immediately before being mixed with the 114.3 MHz IF.	LOIF_LO_SENSE
DSP IF Sense	This point monitors the level of the 3.686 MHz IF signal just before it goes to the Receive DSP (A12) assembly.	LOIF_DSP_IF_S
114.3 MHz IF Input Sense	The 114.3 MHz IF from the Receiver (A30) is measured at the input of the LO/IF/Demod assembly.	LOIF_IF_IN_S
Spectrum Analyzer Path Sense	The signal into the LO/IF/Demod assembly is either I/Q demodulated (for CDMA signals) or bypassed through multiple buffers to the Spectrum Analyzer. This point measures the bypassing signal part way through the buffer chain.	LOIF_SA_ADJ_S
+5 Volt Reference Supply	The +5 volt supply for the 1 MHz Reference is measured. This point should measure very close to +5 V.	LOIF_5V_REF
IQ IF Gain Sense	This point monitors the operation of the wide band amplifier that boosts the 3.686 MHz IF level immediately before I/Q demodulation.	LOIF_IQ_GAIN_S
IQ Demodulator LO Tune Voltage	This point monitors the tune voltage for the 14.7456 MHz VCO that is used as an LO for IQ demodulation.	LOIF_DEMOD_VT_S
IQ Demodulator LO Sense	This point monitors the output of the 14.7456 MHz VCO used for IQ demodulation.	LOIF_DEMOD_LO_S
+8 Volt Supply Sense	This point monitors the +8 V power supply through a 1-to-2 voltage divider; this point should measure +4 V.	LOIF_PLUS_8V_S
+9 Volt Supply Sense	This point monitors the +9 V power supply through a voltage divider; this point should measure + 0.50 V.	LOIF_PLUS_9V_S
LO/IF/Demodulator Ground	This point measures the ground potential of the LO/IF/Demod Assembly.	LOIF_GND

Table 133 LO/IF/Demodulator (Continued)

Measurement	Explanation and Suggestions	Measurement Point
IQ Demodulator Q Out Sense	This point measures the Q Out of the IQ Demodulator IC.	LOIF_Q_DEMOD_S
Q Offset Reset	This point verifies that the demodulation has corrected for the 1/2 period clock in the reverse Q Channel.	Q_LEAD_I
LO/IF/Demodulator Temperature Sense	This point measures the ambient air temperature of the LO/IF/Demodulator assembly.	LOIF_TEMP_SENSE

Table 134 I/Q Modulator

Measurement	Explanation and Suggestions	Measurement Point
RF Input Detection	The RF input to the I/Q Modulator assembly is monitored using a detector. (The RF signal comes from the Signal Generator Synthesizer.)	IQMOD_IN_DET
I/Q Modulation Output Detection	The RF output of the I/Q Modulator assembly (to the Output Assembly) is monitored using a detector.	IQMOD_OUT_DET
Baseband I Detection	This point monitors the combined level of the I Noise and I Data baseband signals. (The signal is then buffered and fed to the I/Q modulator IC.)	IQMOD_I_MOD_DET
Baseband Q Detection	This point monitors the combined level of the QNoise and QData baseband signals. (The signal is then buffered and fed to the I/Q modulator IC.)	IQMOD_Q_MOD_DET
I Gain Control	This point monitors the level of the I baseband modulation signal immediately after buffering by an adjustable amp.	IQMOD_I_GAIN
Baseband I and Q Offset	The I and Q modulation signal offsets are measured	IQMOD_I_OFFSET IQMOD_Q_OFFSET
Quadrature Adjust Voltage Error	This point measures the summed output of the DI and DQ signals from the IQ Modulator IC.	IQMOD_VERR
I/Q Modulator I Control Voltage	This is the I quadrature adjust signal that is derived from the quadrature Adjust Error Voltage.	IQMOD_VCI

Table 134 I/Q Modulator (Continued)

Measurement	Explanation and Suggestions	Measurement Point
I/Q Modulator Q Control Voltage	This is the Qquadrature adjust signal that is derived from the quadrature Adjust Error Voltage.	IQMOD_VCQ
I/Q Modulator LO Bias Voltage	This point monitors the output of a DAC that tunes a VCO inside the I/Q Modulator IC.	IQMOD_VBLO
DAC Quadrature Adjust Output	This point monitors the output of a DAC that adjusts the phase of the I/Q Modulator IC to achieve quadrature.	IQMOD_QUAD_ADJ
I/Q Modulator IC DI and DQ pins	These points monitor the quadrature adjust lines out of the I/Q Modulator IC before reaching the Quadrature Adjust circuitry.	IQMOD_Di_diag IQMOD_Dq_diag
I/Q Modulator Ground	This point measures the ground potential of the I/Q Modulator Assembly.	IQMOD_GND
Zero Power RF Detector Offset	This point measures the offset of the RF Power Detector at the zero power state.	IQMOD_RF_DET_OFFSET

Table 135 Cell Site Analog

Measurement	Explanation and Suggestions	Measurement Point
Cell Site 1 Video DACs Reference Voltage Supply	This point measures the level of the reference supply for the three Cell Site #1 video DACs.	CSAN_VREF_2_S
Cell Site 2 Video DACs Reference Voltage Supply	This point measures the level of the reference supply for the three Cell Site #2 video DACs.	CSAN_VREF_4_S
Control DACs Reference Voltage Supply Sense	The +15V supply is regulated to +10V and used as a reference for the Gain DACs. This voltage is sampled through a 1-to-2 voltage divider; so this voltage should measure very close to +5 V.	CSAN_PLUS10_REF_S
Cell Site 1 Amp 1 Gain Control	These points monitor the output of the Cell Site #1 Gain Control DAC Q and I gain control lines.	CSAN_I1_GAIN_S CSAN_Q1_GAIN_S

Table 135 Cell Site Analog (Continued)

Measurement	Explanation and Suggestions	Measurement Point
Baseband I and Q Summing Amp Outputs Sense	The eight channels are summed, and the eight Q channels are summed, to provide the I and Q drive signals to the I/Q Modulator assembly. These points monitor the I and Q signals (through detectors) just prior to going to the I/Q Modulator.	CSAN_I_OUT_S CSAN_Q_OUT_S
Cell Site Analog Ground	This point measures the ground potential of the Cell Site Analog assembly.	CSAN_GND

8924C Settings for CDMA Diagnostics

On the CONFIGURE screen the **RF Display** is set to **Freq,** for all assemblies. The **RF Offset** is turned **Off**, for the LO/IF/Demod assembly, and for all others its turned **On** , AT **0** MHz.

On the CDMA GENERATOR CONTROL screen **Sector A Power, Sector B** and **AWGN** are all set to **-60** dBm/Bw. During the measurement of I and Q Noise on the CDMA Reference assembly (CREF_I_NOISE_S and CREF_Q_NOISE_S), **Sector A Power** and **Sector B Power** are turned **Off.**

For all measurements on the LO/IF Demod assembly only, the RF ANALYZER and RF GENERTOR screens are used. On the RF ANALYZER screen the **Tune Mode** is set to **800** MHz, the **Input Port** is set to **RF In**, the **IF Filter** is set to **230 kHz** and the **Input Atten** is set to **Hold** and **0 dB.** On the RF GENERATOR screen the RF GEN FREQ is set to **800** MHz, the Output Port is set to **RF Out**, the **Amplitude** is set to **-10** dBm and the **AF GEN 1 To** is turned **Off.**

For all measurements on the IQ Modulator assembly, four latches are set according to directions in the Internal Maintenance Specification so diagnostic limits can match those as determined by the R&D designer. The settings are on the SERVICE screen and are as follows:

Select **Latch** cdmaRef_noise_mode_cntl and set **Value** to **1.**

Select **Latch** cdmaRef_noise_src_cnon and set **Value** to **1.**

Select **Latch** cdmaRef_I_Noise_Gain_DACand set **Value** to **3DE**

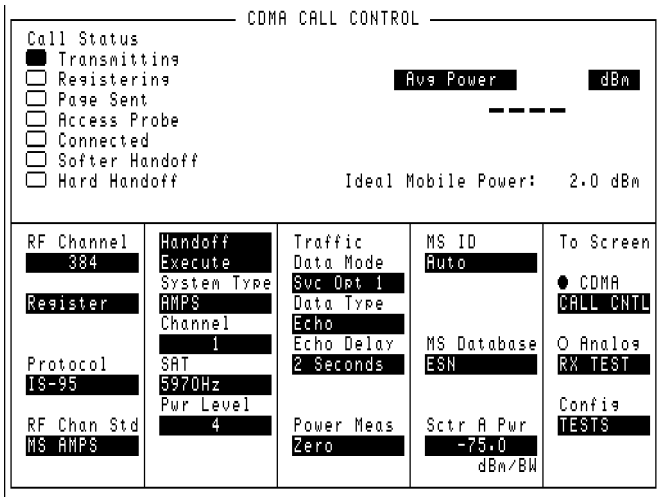
Select **Latch** cdmaRef_Q_Noise_Gain__DACand set **Value** to **3DE.**

A

Error Messages

Error Messages are Located at the Top of the Display

One or more self tests failed. Error code: 0080



General Information About Error Messages

Several types of messages may be displayed at the top of the Test Set's screen. Descriptions of the Error messages displayed by the Test Set may be found in the following manuals:

- *HP 8924C User's Guide*
- *HP 8924C Assembly Level Repair Manual* (this manual)
- *HP Instrument BASIC User's Handbook*: (HP P/N E2083-90005).

The type of message determines which manual to refer to for more information. There are four types of messages:

- Positive numbered error messages
- IBASIC error messages
- HP-IB error messages
- Text only messages

The following paragraphs give a brief description of each message format and direct you to the manual to look in for information about error messages displayed in that format.

BEEPER OPERATION

Messages are always accompanied by a BEEP from the internal speaker, unless the **Beeper** field on the CONFIGURE screen is set to **Off**.

CAUTION! IF YOU HEAR A LOUD SIREN OR "WARBLING" SOUND

TURN THE INSTRUMENT OFF! This warns of a situation that will eventually damage the Test Set. Remove any connections to the front panel RF IN/OUT, DUPLEX OUT, and ANTENNA IN connections. Turn the Test Set back on; the instrument should power up in its factory preset state (unless a POWERON Save/Recall register was saved). The siren should not come back on.

The MESSAGE Screen

During instrument operation, various messages may appear on the Test Set's display. Prompt-type messages generally appear on the first line of the Test Set's display. General operating and error messages usually appear on the second line of the display. Some messages are persistent; they remain displayed until the error condition no longer exists, or until another persistent message with greater priority occurs. Other messages are only displayed when the error first occurs; they are removed when a key is pressed or the knob is turned, or when an HP-IB command is received. Many of the messages are displayed on the MESSAGE screen until the instrument is turned off (press the SHIFT key, and then the HELP key to access this screen).

Messages about error conditions may tell you what to do to correct the error (turn something off, reduce a field's value, press a certain key, and so forth).

Powerup Self-Test Error Messages

One or more self tests failed. Error code: 0080

A Test Set failure was detected when the Test Set was turned on. (For example, having a stuck front-panel key during turn-on.) The (hexadecimal) error code corresponds to the failure message (or messages); see **table 114, "Returned Values for Self-Test Diagnostic Failures" on page 542**. For example, error code 0080 corresponds to the message “Keyboard Failure (stuck key)”; **see chapter 14, "Diagnostics Descriptions"** for more information.

Functional Diagnostics Messages

Direct latch write occurred. Cycle power when done servicing.

This message will occur when initiating and running the Functional Diagnostics. For information on this and other diagnostic messages **see "Frequently Encountered Error Messages" on page 81**, .

Audio Diagnostics Messages

When a measurement is out of limits, a message is displayed at the end of the test which indicates the following:

- Suspected faulty assembly.
- Confidence level of the assertion (low, medium, high).
- Failure Code

For a detailed description of the test, including an interpretation of the failure codes and relevant block diagrams, **see chapter 14, "Diagnostics Descriptions"**.

RF and Miscellaneous Diagnostics Messages

When a measurement is out of limits, a message is displayed at the end of the test which indicates the following:

- Suspected faulty assembly.
- Confidence level of the assertion (low, medium, high).

For a detailed description of the test, including an interpretation of the failure codes and relevant block diagrams, **See chapter 14, "Diagnostics Descriptions"**.

CDMA Diagnostics Messages

The RF, AF, and MS Diagnostics should always be run prior to running the CDMA Diagnostics to help isolate analog assembly failures.

The CDMA Diagnostics compare measured MUX point values to upper and lower limits for several CDMA assemblies. Any failed data points are reported at the bottom of the test. When used with the individual block diagrams for each assembly, the pass/fail data helps to identify failing assemblies.

You can select an individual CDMA assembly to test, or test all of the assemblies in sequence.

Calibration Download Failure Error Message

Cal file checksum incorrect. File reset to default values.

This message occurs at powerup when downloading of calibration data is unsuccessful. It indicates that the calibration data is corrupt, and although the Test Set will function, measurements will be inaccurate. Calibration data is downloaded from a memory card when certain assemblies are replaced, or it is generated when the Periodic Calibration program is run. This message will not occur again at powerup unless another unsuccessful downloading occurs.

Flash ROM Firmware Upgrade Error Messages

Test Set firmware is stored in flash ROMs. With flash ROMs, the firmware can be quickly upgraded with new firmware from a memory card. It is not necessary to open the Test Set and replace individual ICs. Should problems arise in the process of uploading the new firmware, the user is notified by messages on the display which state the situation and suggest any actions to be taken.

The firmware upgrade process begins when the user inserts the firmware upgrade memory card into the front-panel memory card socket and turns the Test Set on. The Test Set notes the presence of a valid firmware upgrade card and proceeds to upload the firmware on the memory card into the flash ROMs on the A16 Host Controller assembly. Any failures that occur during the upload process are immediately reported and the upload is aborted.

The error messages that may be displayed during a firmware upgrade are listed below in alphabetical order. Supplemental fault information is included.

Memory Card Checksum Error

The memory card may be at fault. The card reader on the A17 Memory board could also be faulty.

Memory Card Read Error

This error will always appear if the user removes the memory card during the upload process. The memory card itself could be faulty or, less likely, the card reader on the A17 Memory board.

Memory Erase Error

This fault is most likely caused by either the flash ROMs themselves or the controller circuits. In either case replace the A16 Host Controller assembly.

Memory Write Error

This fault is most likely caused by either the flash ROMs themselves or the controller circuits. In either case replace the A16 Host Controller assembly.

Programming Voltage Error

The programming voltage is supplied to the flash ROMs from the power supply via the A16 Host Controller assembly. The fault is most likely on the A16 Host Controller but can be caused by the A20 Filter/Regulator assembly.

ROM Checksum Error

With the new firmware loaded into the Test Set's flash ROMs, the checksum on the ROM is tested. A faulty checksum is most likely caused by the flash ROMs themselves or possibly the controller circuits. In either case replace the A16 Controller assembly.

Self-Calibration Error Messages

Voltmeter Self Calibration Failed. Error = 223, 0x0000ffff (EXAMPLE)

The example noted above is one of many messages that may occur during self-calibration. When the Test Set is powered up and at timed intervals for certain measurements, the Test Set calibrates itself internally. Calibration usually takes 20 to 30 ms. The following measurements are calibrated at these timed intervals:

- Voltmeter: approximately every 3 minutes
- Counter: approximately every 3 minutes
- Oscilloscope: approximately every 3 minutes
- Spectrum Analyzer: approximately every 4 minutes

Should a self-calibration fail, an error message is displayed. The error code (223, 0x0000ffff in the example above) will vary depending on the particular failure. Failures of this type are generally caused by hardware. Since a general self-calibration occurs immediately after power-up, these failures often appear as though they are power-up self-test errors.

When a self-calibration failure occurs, check the A37 Measurement assembly first since most of the measurement circuitry described above is located on it. However, in the case of the spectrum analyzer calibration, check the A32 Spectrum Analyzer assembly first. The A27 Reference assembly may also cause its own self-calibration failure or a Spectrum Analyzer error message. (The error message in the example above can be generated by unplugging the A27 Reference before powering up the Test Set.)

After displaying a self-calibration error message, the Test Set will proceed with the measurement using default calibration factors. Depending on the nature of the failure, subsequent measurements may look normal. The error message will persist.

Text Only Error Messages

Text only error messages are generally associated with manual operation of the Test Set. Refer to the *HP 8924C User's Guide* for information on text only error messages.

Text only error messages can also be displayed while running the Test Set's built-in diagnostic or calibration utility programs. Diagnostic messages are described in **see chapter 14, "Diagnostics Descriptions"**.

Text only error messages take the form: **`This is an error message.`**

For example:

- **`Input value out of range`** occurs when trying to set a value above or below it capability (such as attempting to set the **`RF Gen Freq`** field to 2 GHz).
- **`Turn off either AM or FM setting`** occurs when trying to perform simultaneous AM and FM modulation.

Positive Numbered Error Messages

Positive numbered error messages usually occur when trying to save or retrieve an IBASIC file, or when trying to run a faulty IBASIC program. Refer to the *HP Instrument BASIC User's Handbook* for information on IBASIC error messages.

Positive numbered error messages take the form: **`ERROR XX 'error message'`**

For example:

- **`Error 54 Duplicate file name`** occurs when trying to save a file to a device where a file with the same name already exists.
  - or
- **`Error 5 Improper Context Terminator`** occurs when an END, SUBEND, or FNEND statement is not present in the program when required.

IBASIC Error Messages

IBASIC Error Messages are associated with IBASIC language operation. IBASIC error messages can have both positive and negative numbers (but always start with "**`IBASIC Error:`**") . Refer to the *HP Instrument BASIC User's Handbook* for information on positive numbered error messages. Refer to the HP-IB Error Messages section of the *HP 8924C User's Guide* for information on negative numbered error messages (the error message associated with a negative number is the same for HP-IB errors and IBASIC errors).

IBASIC error messages take the form: **`IBASIC Error: -XX error message`**

For example:

- **`IBASIC Error: -286 Program runtime error`**

HP-IB Error Messages

HP-IB Error Messages are associated with HP-IB operation. Refer to the *HP 8924C User's Guide* for information on HP-IB error messages.

HP-IB error messages take the form: **`HP-IB Error: -XX error message`** or **`HP-IB Error error message`**

For example:

`HP-IB Error: -410 Query INTERRUPTED.`

or

`HP-IB Error: Input value out of range.`

Non-Recoverable Firmware Error

This error occurs when the Test Set encounters a condition that the firmware doesn't understand - causing the Test Set to halt operation until power is cycled. The message appears in the center of the Test Set's display and (except for the two lines in the second paragraph) has the form:

```
Non-recoverable firmware error.  Please record the 2 lines of
text below and contact Hewlett Packard through your local
service center. In the U.S., you may call the factory at
(800) 827-3848.

  'Address error exception'
   at line number 0

To continue operation, turn POWER off and back on.
```

Follow the instructions in the message.

Unfortunately, you may not be able to recover from this condition without turning the Test Set off. The error may not reoccur when you turn the Test Set back on and rerun the test where the Error Message first occurred. If the failure reoccurs, you should record exactly what the configuration of the instrument was when the error appeared, and contact HP. This information will help us determine the proper course of action for your repair.

If This Error Occurs at Power-up

If the Test Set displays this error when first powered up, disabling Test Set operation, it could be related to the **Autostart** field on the main TESTS screen. This field causes the Test Set to automatically run the last program loaded in memory when the Test Set is powered up. If the program is corrupted, the Test Set will automatically "lock up".

The only way to recover from this condition is to clear the Test Set's operating RAM. This will clear any IBASIC program, Save/Recall registers, and RAM disks that have been saved, as well as three calibration factors. The calibration factors are easily re-entered; the IBASIC programs, Save/Recall registers, and RAM disks must be re-loaded or re-initialized after clearing memory.

To clear the Test Set's RAM;

1. Turn the Test Set off.
2. Hold the PRESET and HZ/µV keys down.
3. Turn the power on (with the buttons still held down) and wait until the CDMA CALL CONTROL screen is displayed.

Use this procedure to re-enter the three calibration factors that were erased when RAM is cleared. Use the ANLG SCRNS keys (to the left of the cursor control knob) to access the required screens.

1. Access the RF GENERATOR screen and select the **DC FM Zero** field (under **FM Coupling**).
2. Disconnect any cables to the ANTENNA IN or RF IN/OUT connectors.
3. Access the TX TEST screen and select **Zero** under the **TX Pwr Zero** field.
4. Access the AF ANALYZER screen and select **Zero** under the **DC Current** field.

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