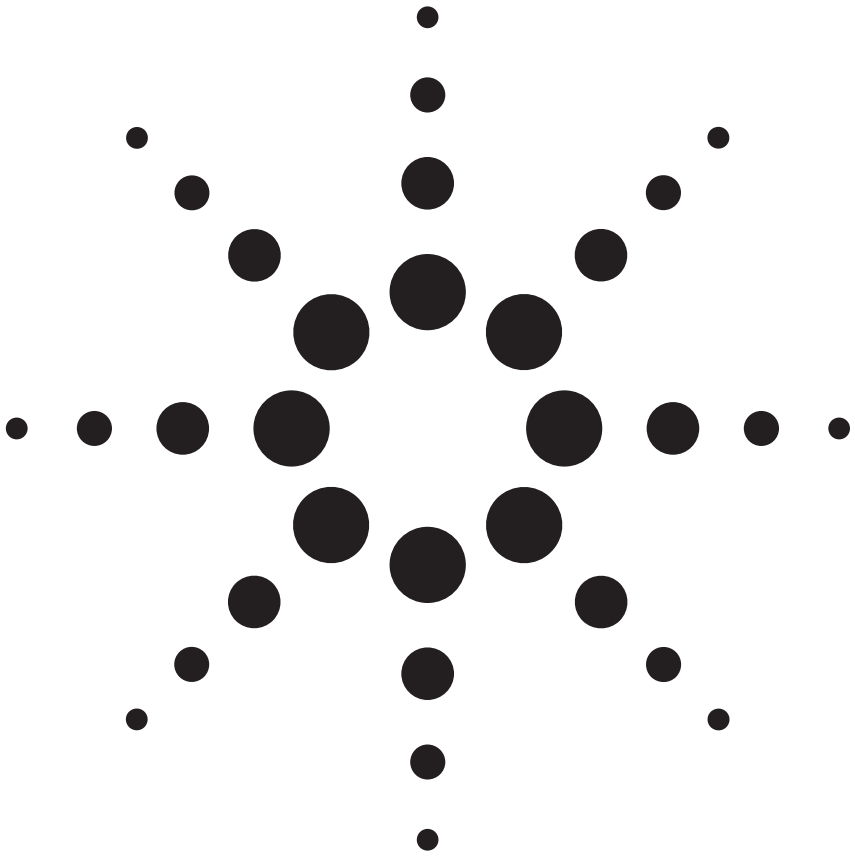
Agilent
Investigating Microvia Technology for 10 Gbps and Higher Telecommunications Systems

White Paper



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Introduction

Today's telecommunication platforms depend upon high-speed serial data transmission. Leading edge digital designers push the performance limit of what is possible to achieve on copper. The proliferation of serial links beyond 10 Gbps has exposed signal integrity issues not typically encountered in the standard digital design laboratory. Optimization of signal integrity by focusing on the physical layer structures within these high-speed channels can produce astonishing results. The fundamental insight of how signals propagate can be clearly understood with the proper design tools and methodologies.

Network switches and routers have recently employed advanced backplane technology to break the terabit barrier. This accomplishment is in part due to sophisticated design techniques within the physical layer components. A major portion of this design cycle is geared toward modeling, simulation, and measurement validation. Reflections, crosstalk, impedance mismatch, and loss can be visualized. These complex phenomenon become intuitive through the use of design tools that allow both time and frequency domain analysis.

Real estate constraints of high-speed digital systems necessitate the use of microvia technology to allow more components to be placed on a single circuit board. With more companies using microvia technology, the process has been able to advance rapidly from controlled depth drilling to more advanced laser ablation techniques. Printed circuit board manufactures are tasked with developing processes for microvias that meet the aspect ratio requirements of today's multilayer backplanes. Implementing microvias opens the door for SMT board to backplane connectors and the overall system performance improvements inherent in these connector systems.

Telecom System Physical Layer Overview

Typical 10 Gbps Telecom System

During the late 1990s and early 2000s the focus of network OEMs was the delivery of high-performance technology-leading communication systems to meet the demands for ever greater telecom bandwidths. Chassis and backplane design were key differentiators for market-leading manufacturers. The communications industry today is evolving towards modularity in a manner very similar to the server world transition in the early 90s.

Telecommunication systems such as that shown in Figure 1 typically achieve high-speed data transport through a switch fabric interface that can be used as a secondary communications channel in parallel with the base interface. In most high-speed networking applications, the base interface will be used to carry communications between the control-plane processors on each line card. This physical layer copper interface creates many challenges for signal integrity engineers designing, developing, and testing network elements. One of the most challenging and interesting areas for high-speed design is in backplane applications. Performance of routers and switches is fundamentally limited by the bottleneck created by the backplane components. Therefore, this is an area rich for technology breakthroughs and innovation.

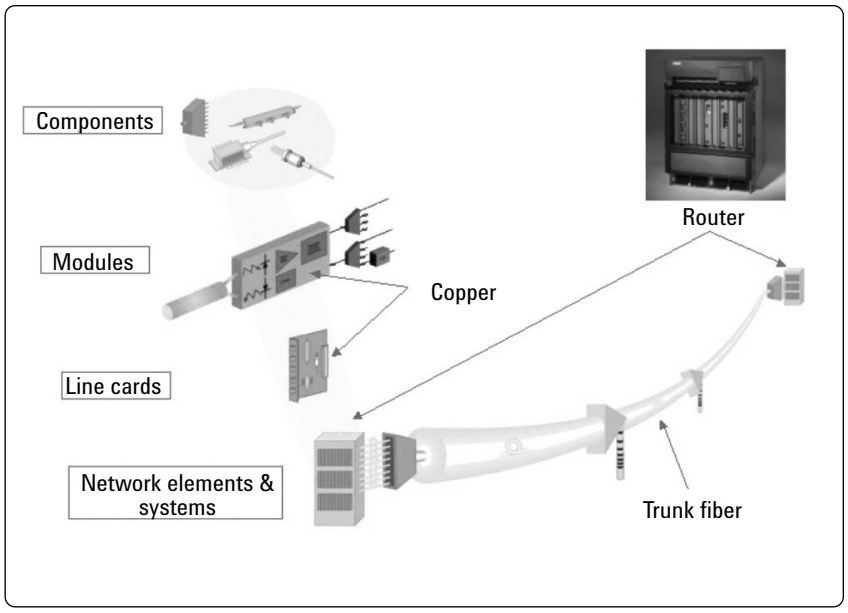


Figure 1. Typical telecommunication system

Backplanes are a critical link

Today's standards efforts for a 10 Gbps Ethernet backplane are under development within the IEEE 802.3ap task force. The goal is to use an ordinary copper backplane as shown in Figure 2 to send 10 Gbps Ethernet signals between line cards using no optics. A standard would give systems designers a head start, allowing them to choose among several physical-layer chips that would be pre-wired for the standard. Exciting work is being done with 10-Gbps serial and novel signaling schemes such as binary signaling or PAM4 that can help achieve this high-speed data transmission. However, the ultimate limit of serial rates will be most likely dictated by the signal integrity of the physical layer backplane. Achieving a controlled impedance environment throughout the complete backplane channel from chip-to-chip will demand careful and meticulous design methodologies. The backplane connector plays a critical part of this channel.

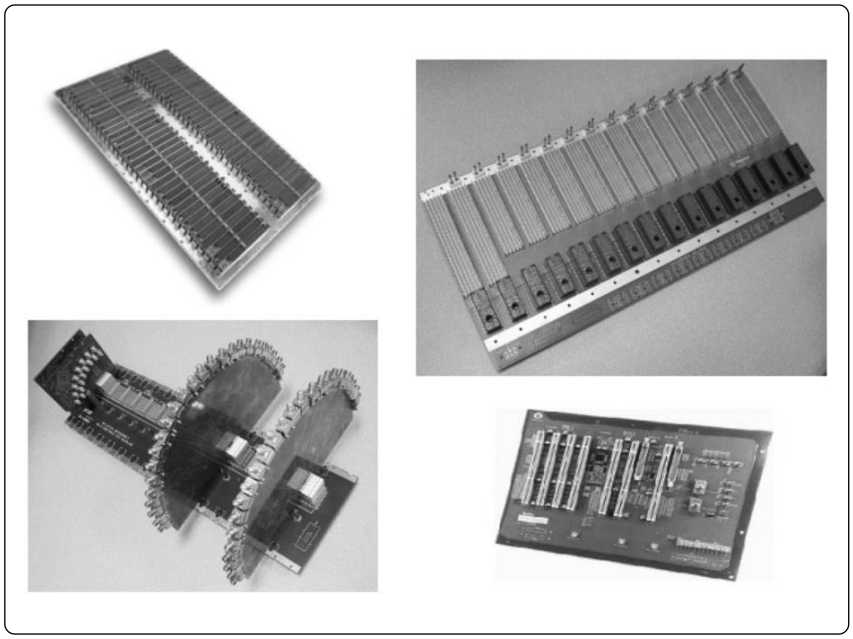


Figure 2. Examples of ordinary copper backplanes

Backplane connectors are advanced

Designing a surface mount board to backplane connector has numerous requirements. First, the interface must withstand the mechanical conditions faced by standard board applications and be very rugged. Secondly, the connector must be able to transmit data at speeds exceeding 10 Gbps. Recent designs of Surface Mount (SMT) backplane connectors have evolved from press fit connector technology, including many of the same mechanical features such as the 1.5 mm x 2.5 mm pin grid. The two main differences in the connector designs revolve around the use of SMT signal leads and the 'C-shaped' pin-in-paste ground shield pin. The exploded view shown in Figure 3 shows the details of construction of a 10 Gbps connector.

A well-designed high-speed board to backplane connector integrates the mechanical, chemical, and electrical properties of the device seamlessly. Orientation of differential pairs, spacing of contacts, and selection of component materials all play key roles in the overall performance. It is a challenge to find the proper combination of these design criterions without impacting the signal integrity of the connector. A great deal of time and effort goes into the design and modeling of these types of connectors before the first piece of steel is cut.

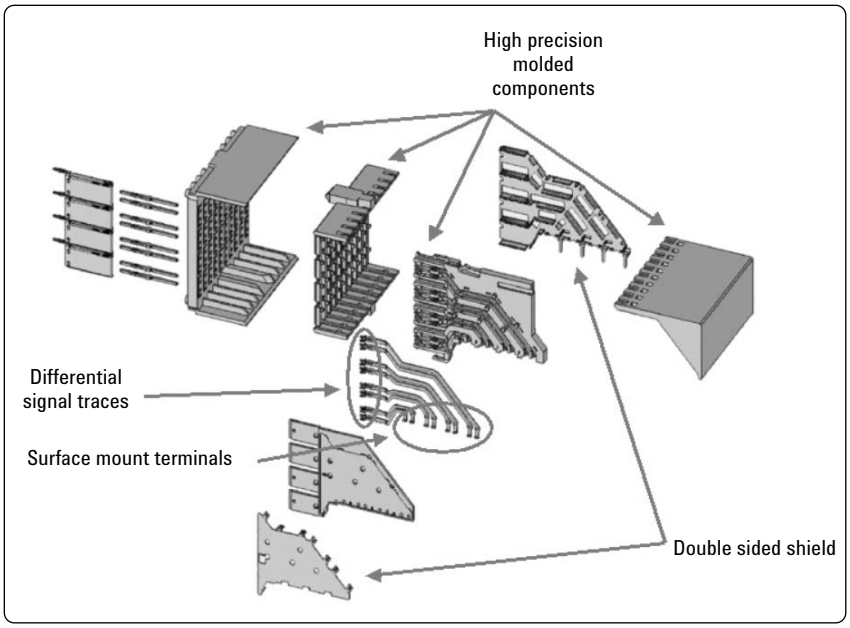


Figure 3. Construction of a 10 Gbps connector

Via stubs create capacitive loads

It is essential to reduce the amount of via stub to successfully transmit data at 10 Gbps. Connectors that require interfaces to Plated Thru Holes (PTHs) are susceptible to capacitive loading that is inherent to the geometry of these commonly used board attachments. To overcome this challenge, the most critical lines would need to be routed closest to the bottom surface of the PCB as shown in Figure 4 or the via barrels back drilled to reduce the via stub. This may lead to longer design times and more layers to achieve the desired signal integrity performance.

Many board designers implementing press-fit connectors try to reduce the resonant behavior of a PTH by routing signals near the bottom layer of the PCB, or back-drilling critical lines to reduce the via stub. With surface mount connectors, there is no need for back-drilling since the connector is mounted on the top surface of the PCB and the signals are attached with blind or buried vias. This type of connection scheme allows the system bottleneck to move from the connector to the PCB material.

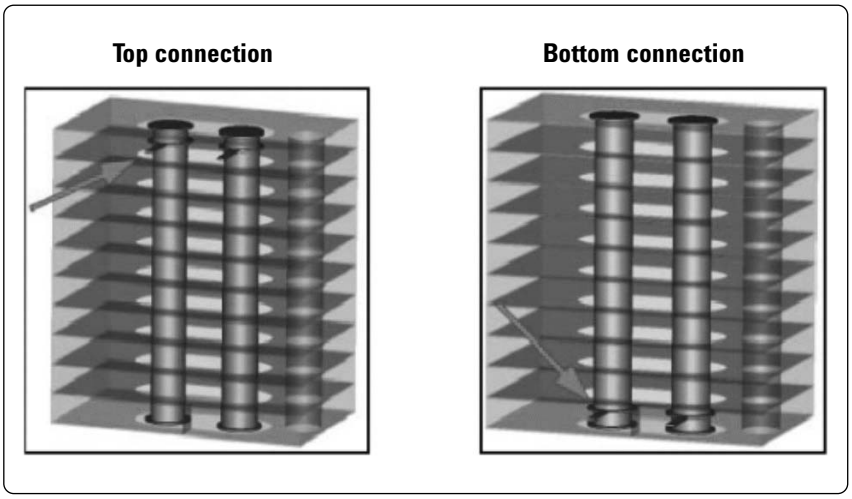


Figure 4. Top and bottom routed lines

Connector to board interface

With an SMT termination the reflective behavior associated with a PTH is reduced or even eliminated since there is very little dangling stub. The interface to surface mount devices, whether it is resistors, silicon IC's, or connectors, must be made on the outer surfaces of the PCB. It would be impossible to route all of the signal lines of a high density, high-speed, differential connector on the outer surface alone, therefore an alternate approach must be taken. Additionally, these high-speed lines will need to interact and connect with inner routing layers to achieve all of the desired functionality of the system. Different via structures can be used in conjunction with the backplane connector to interface the connector to the inner board traces. Graphical examples of both PTH and SMT are shown in Figure 5.

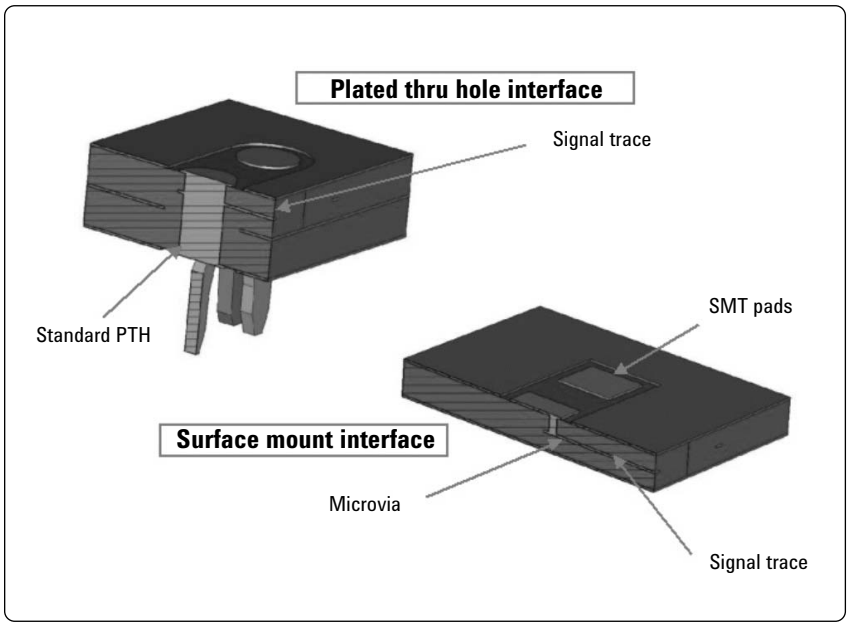


Figure 5. PTH and SMT technology

Microvia with surface mount (SMT) improves signal

Figure 6 shows a typical PTH and microvia structure within a mixed board stack-up. The same type of SMT lead from the connector is attached to the PCB but we can use two different techniques to bring the signals from the connector to the PCB traces. With the illustration on the left, a PTH connects the SMT pad to the trace near the bottom surface of the PCB. Since there is no pin inserted into this PTH, the via diameter can be shrunk to a size that reduces the capacitive effect while still meeting the aspect ratio requirements of the board vendor. Using this smaller via allows for added signal performance with respect to a standard PTH, while creating a cost savings over more expensive via alternatives. Additionally, using a full plated thru barrel allows signals to be accessed at any layer within the PCB stack, although accessing signal traces that are close to the surface will introduce stubbing effects into the signal path.

In the example on the right, a small microvia is used to connect the SMT pad to an inner board trace. This via can be made even smaller in diameter, in relation to the PTH, as it is often formed by more precise methods then the mechanical drilling process used to create PTHs. Selectively stacking microvias to reach a desired layer allows the board designer to achieve optimal signal performance by eliminating the electrical stub.

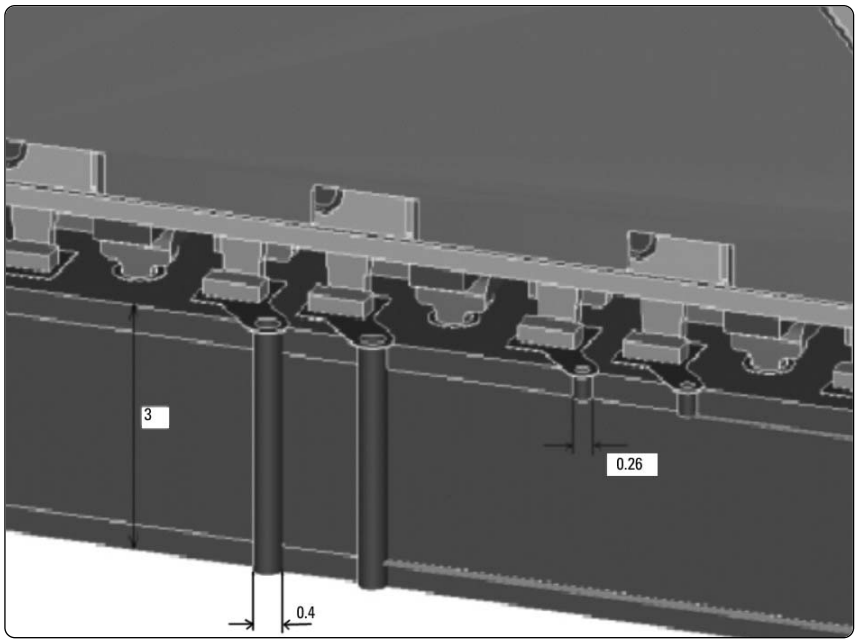


Figure 6. PTH to SMT pad vs. microvia to SMT pad

Signal Integrity and Differential Signaling

Backplane data rates are increasing

The proliferation of many new high-speed digital standards depicted in Figure 7 push the envelope of what's possible on copper. The data must be transmitted with very few bit errors to maintain system reliability. Unfortunately, the signal integrity suffers when the risetime of the data transition from a one to a zero becomes faster. This faster risetime emphasizes poor design technique of any physical layer component in the system, including every stripline, microstrip, cable, and connector. Frequency dependent effects are now commonplace across most high-speed digital designs and knowledge of transmission line theory is now a requirement for leading edge design. To complicate matters further, the majority of these standards utilize differential circuit topology. A paradigm shift in measurement technology is under way to achieve the goals of the advanced differential interconnect.

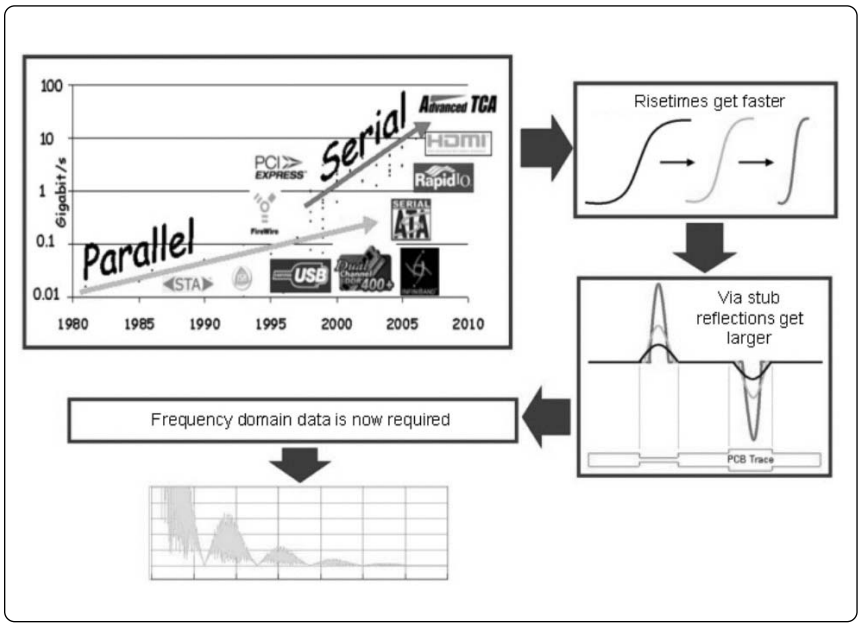


Figure 7. Proliferation of standards

Transmission lines are differential

Using Figure 8 as a guide for understanding current flow, imagine two transmission lines that are driven by single ended signals that are exactly out of phase (we call this differential driving). As the signal propagates down the differential pair, there is a voltage pattern between each signal line and the reference plane below. In addition, there is a signal between the two signal lines. This is called the difference signal or differential signal.

Differential impedance is simply the impedance the difference signal sees that is driven between the two signal lines in the differential pair. The impedance the difference signal sees is the ratio of the signal voltage (difference voltage) to the current in the line. The difference voltage is twice the voltage of the edges driven into each line. The current into each line is related to the impedance of each individual line in the pair. There is an additional current between the signal lines that is due to the coupling between the traces themselves. This is in general a small amount, but cannot be neglected. If there were no coupling between transmission lines, the impedance of a line, as defined by the ratio of the voltage across the paths and the current through them, would be dependent on just the line parameters of the one line. However, as soon as coupling is introduced, the voltage on one line may be dependent on the current in an adjacent line. To include these effects, the concept of impedance or characteristic impedance must be expanded to allow for one trace interacting with another. This is handled by expanding the impedance into an impedance matrix. Matrix math is very useful when quantifying the performance of differential transmission lines, as will be evident in the next discussion that describes another type of matrix called the mixed mode s-parameter matrix.

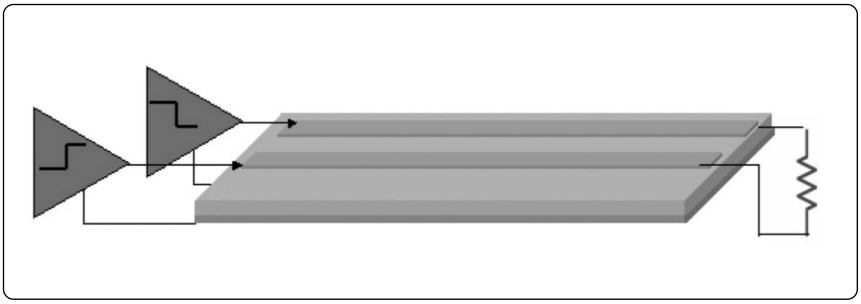


Figure 8. Differential driving

Single ended parameters

To lay a foundation for understanding how to characterize a physical layer device within a 10 Gbps telecom system, a brief discussion of multiport measurements is in order. The four port device shown in Figure 9 is an example of what a real world structure might look like if we had two adjacent PCB traces that are operating in a single-ended fashion. Let's assume that these two traces are located within relatively close proximity to each other on a backplane and some small amount of coupling might be present. Since these are two separate single-ended lines in this example, this coupling is an undesirable effect and we call it crosstalk.

The matrix on the left in Figure 9 shows the 16 single-ended s-parameters that are associated with these two lines. The matrix on the right in Figure 9 shows the 16 single-ended time domain parameters associated with these two lines. Each parameter on the left can be mapped directly into its corresponding parameter on the right through an Inverse Fast Fourier Transform (IFFT). Likewise, the parameters on the right can be mapped to the parameters on the left by a Fast Fourier Transform (FFT).

If these two traces were routed very close together as a differential pair, then the coupling would be a desirable effect and it would enable good common mode rejection that provides EMI benefits.

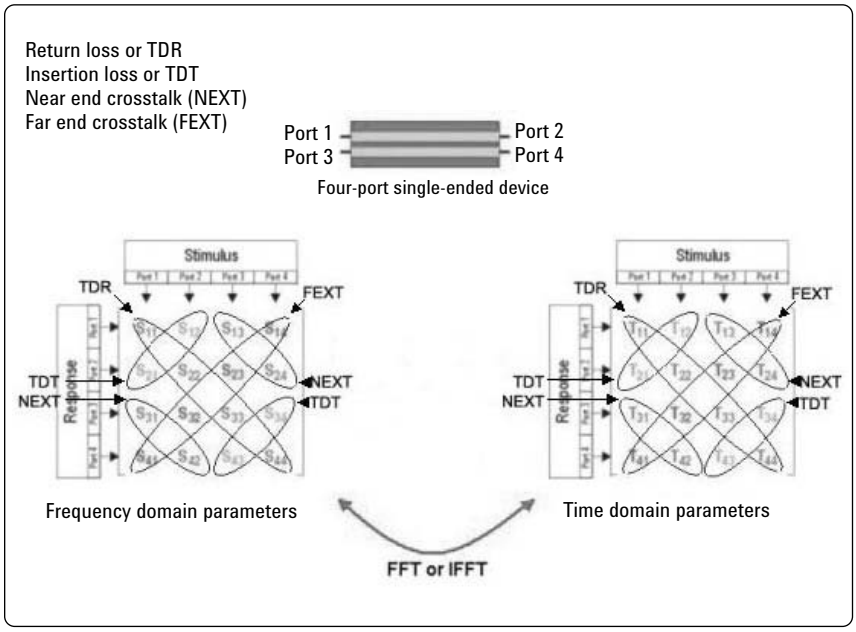


Figure 9. Effects of undesirable coupling on two single-ended lines

Single-ended to differential s-parameter

Once the single-ended s-parameters have been measured, it is desirable to transform these to balanced s-parameters to characterize differential devices. This mathematical transformation is possible because a special condition exists when the device under test is a linear and passive structure. Linear passive structures include PCB traces, backplanes, cables, connectors, IC packages and other interconnects. Utilizing linear superposition theory, all of the elements in the single-ended s-parameter matrix on the left of Figure 10 are processed and mapped into the differential s-parameter matrix on the right. Much insight into the performance of the differential device can be achieved through the study of this differential s-parameter matrix, including EMI susceptibility and EMI emissions.

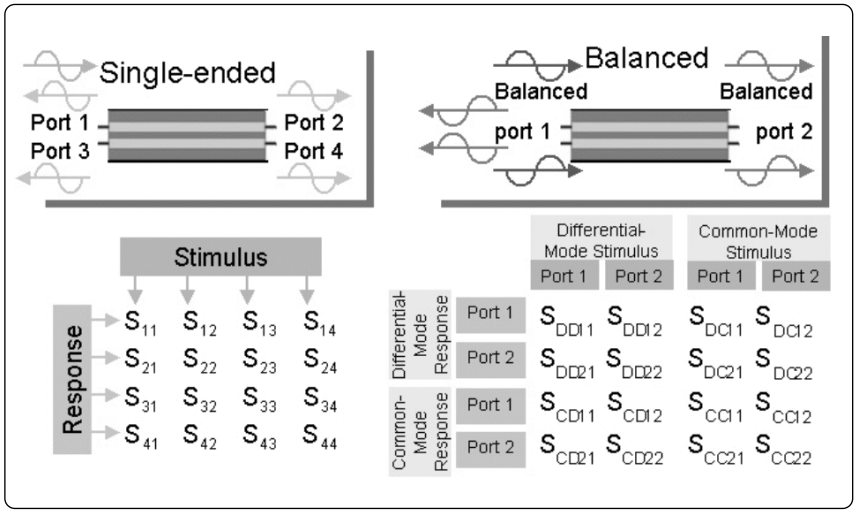


Figure 10. Balanced s-parameters of a differential device

Differential s-parameters

Interpreting the large amount of data in the 16-element differential s-parameter matrix is not trivial, so it is helpful to analyze one quadrant at a time. The first quadrant in the upper left of Figure 11 is defined as the 4 parameters describing the differential stimulus and differential response characteristics of the device under test. This is the actual mode of operation for most high-speed differential interconnects, so it is typically the most useful quadrant that is analyzed first. It includes input differential return loss (SDD11), forward differential insertion loss (SDD21), output differential return loss (SDD22) and reverse differential insertion loss (SDD12). Note the format of the parameter notation SXYab, where S stands for Scattering Parameter or S-Parameter, X is the response mode (differential or common), Y is the stimulus mode (differential or common), a is the output port and b is the input port. This is typical nomenclature for frequency domain scattering parameters. The matrix representing the 16 time domain parameters will have similar notation, except the "S" will be replaced by a "T" (i.e. TDD11). The fourth quadrant is located in the lower right and describes the performance characteristics of the common signal propagating through the device under test. If the device is design properly, there should be minimal mode conversion and the fourth quadrant data is of little concern. However, if any mode conversion is present due to design flaws, then the fourth quadrant will describe how this common signal behaves. The second and third quadrants are located in the upper right and lower left of Figure 11. These are also referred to as the mixed mode quadrants. This is because they fully characterize any mode conversion occurring in the device under test, whether it is common-to-differential conversion (EMI susceptibility) or differential-to-common conversion (EMI radiation). Understanding the magnitude and location of mode conversion is very helpful when trying to optimize the design of interconnects for gigabit data throughput.

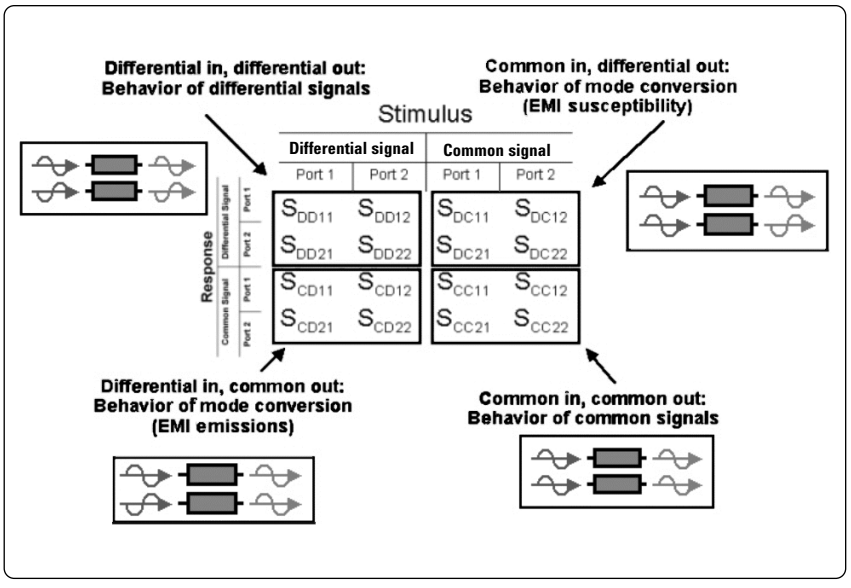


Figure 11. 16-element differential s-parameter matrix

Four Port Microvia Measurements

Measurement set up

The test equipment used in this experiment consists of a 4 port performance network analyzer (PNA) and 4 channel time domain reflectometer (TDR) running Physical Layer Test System software. Both instruments are simultaneously on the GPIB bus and are used to validate measurements between each other. See Figure 12 for set up picture.

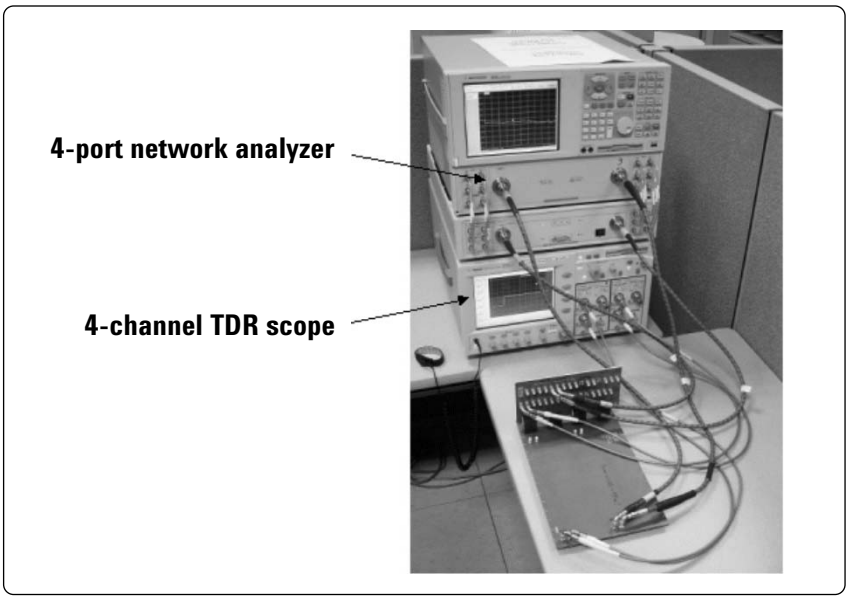


Figure 12. Test equipment set up

Frequency domain analysis

Now that we have a good understanding about 4-port s-parameters, let's interpret the actual data in Figure 13. The more intuitive parameter to review first is typically differential insertion loss or SDD21. This is the frequency response seen by the differential signal as it propagates through the device. At lower frequencies (DC to 10 GHz), both vias perform nearly identical. However, the microvia structure clearly shows less attenuation of higher frequencies when compared to the standard via. This indicates a channel structure that allows higher frequencies to pass without significant degradation. This will inevitably result in an eye diagram that is more open, as will be shown shortly. The standard via, on the other hand, shows higher frequencies being attenuated more than the microvia.

The second set of curves is perhaps less intuitive, but equally important to analyze. The differential return loss (SDD11) indicates the magnitude of reflections occurring at various frequencies within each structure. Again, the low frequency response is very similar for both vias. However, the magnitude of reflections in the standard via is higher than the microvia from 12 to 20 GHz. Reflections are due to a poorly controlled impedance environment and the spacing between the nulls is related to the spacing of the resonant cavity within the structure. In the case of the standard via, this is related to the length of the via stub.

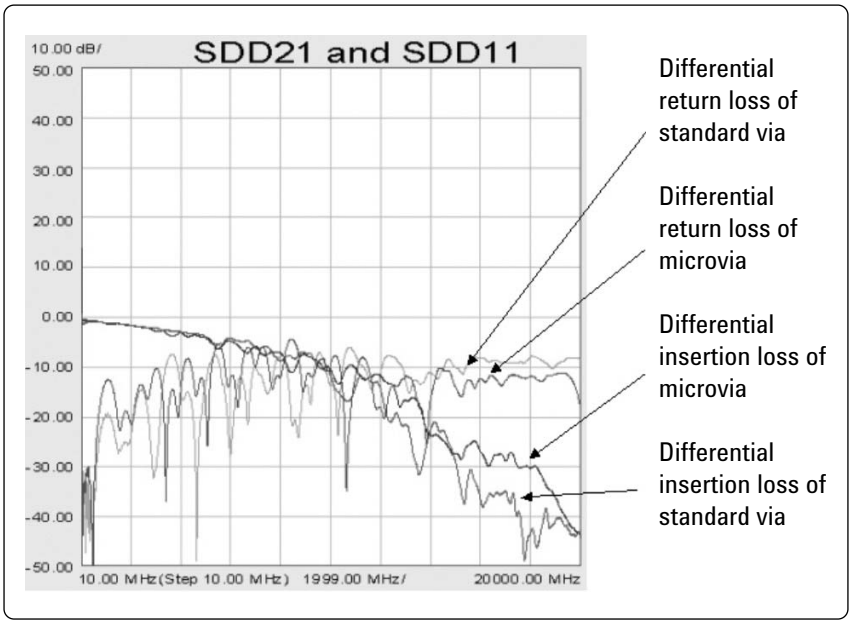


Figure 13. Affects of frequency on standard via and microvia

Differential eye diagram analysis

The eye diagrams in Figure 14 are synthesized from the 4-port s-parameters. This method of creating eye diagrams correlates well with the standard method of compliance testing with a pattern generator and a sampling scope with standard masks. As can be seen, the eye diagrams for the microvia are clearly more open than the standard via, even at 20 Gbps.

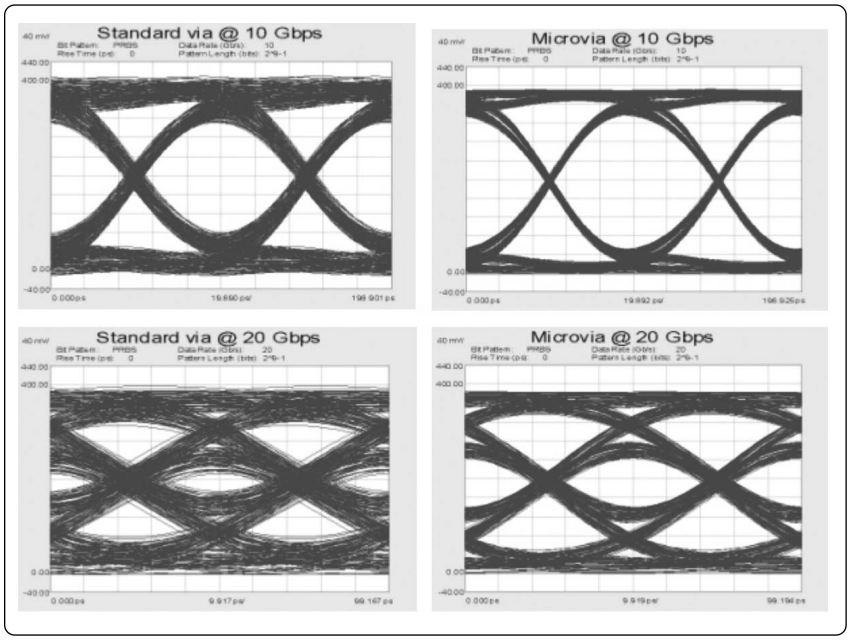


Figure 14. Eye diagrams for standard via and microvia

Microvia Construction

Laser drilling for microvia forming

With Laser drilling a similar process to mechanical drilling is used except the holes are formed by the ablation of material by the laser. When accessing layers beyond layer 1, a number of techniques can be used. Different laser technologies are often used to ensure that the correct features are formed. UV-YAG lasers will cut thru metal layers, but will not damage the organic material of the PCB. CO2 lasers will only cut thru the organic material and stop when they reach a metal layer. Using these types of lasers allows precise forming of the via down to the desired layer in the PCB. Again, this physical forming requires additional real estate.

CO2 lasers operate using wavelengths in the 9 to 11 µm range, which limits their ability primarily to cutting dielectrics. As a result of using CO2 lasers, a hole in the outer copper foil is needed and larger inner layer pads are used to compensate for any image registration issues. UV lasers have a distinct advantage in the creation of microvias, as they operate at wavelengths less then 400 nm. At these wavelengths, the laser can be used to ablate a wide range of materials from metals and organic materials to glasses and inorganic materials. UV-YAG lasers are particularly advantageous given their ability to rapidly and precisely cut thru multiple copper layers as shown in Figure 15. The more precise the laser, the smaller the inner pad dimensions are required, which will further reduce routing density. As a rule of thumb, aspect ratios less than 1:1 should be maintained due to plating limitations. The sidewalls of the microvia are tapered slightly to help in the plating process and the thermal characteristics of the microvia. The ease of implementation of laser drilling into standard PCB manufacturing lines has made this methodology the most widely accepted microvia formation technique. Of boards using microvia technology, more than 90% of them were processed using laser drilling.

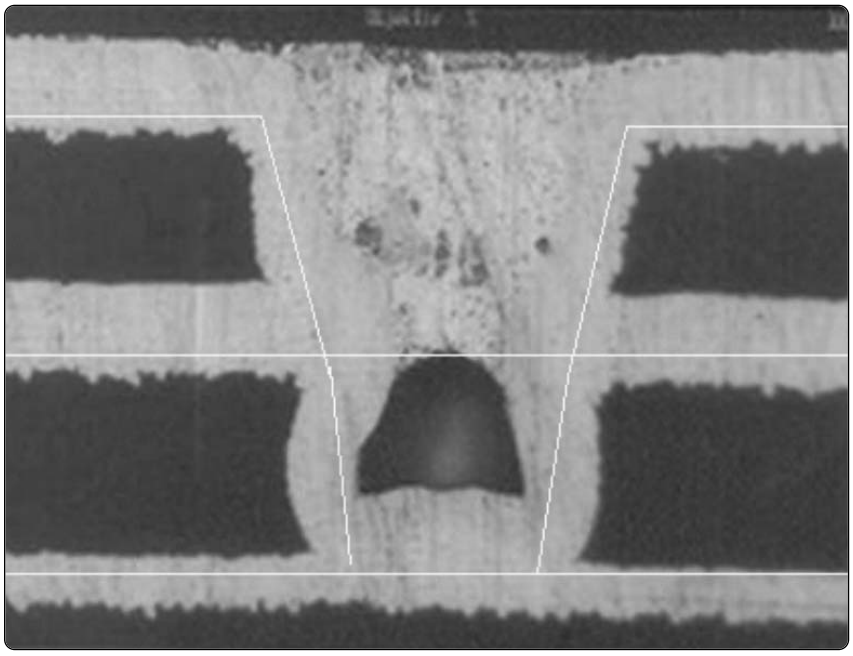


Figure 15. Multiple copper layers cut by UV-YAG laser

Sequential stack up

Since the introduction of microvia technology there has been a rapid evolution in complexity from the single layer laser drilled, to stacked 'inline' vias, to even more complex structures. In some cases more than one via technology has been used to create a multi layer PCB that combines superior signal integrity and efficient use of board space. Two examples are shown in Figure 16. The applications will dictate which configuration is best, as in the case of mobile devices. These devices are leading edge, so they require using the most advanced silicon, which may be packaged in BGA configuration. Mobile devices also have to be small and cost effective, as they tend to become outdated very quickly and must adjust rapidly to changes in the market. For these types of applications, the simple laser drilled PCB will often provide the needed board space and desired signal performance in the smallest real estate.

For higher density applications that require more interconnection to inner routing layers, the stacked (or inline) via approach may fit the bill. Any of these approaches can be used in conjunction with standard PTH technologies to link older legacy devices (press-fit or PTH solder devices) to newer high-density components.

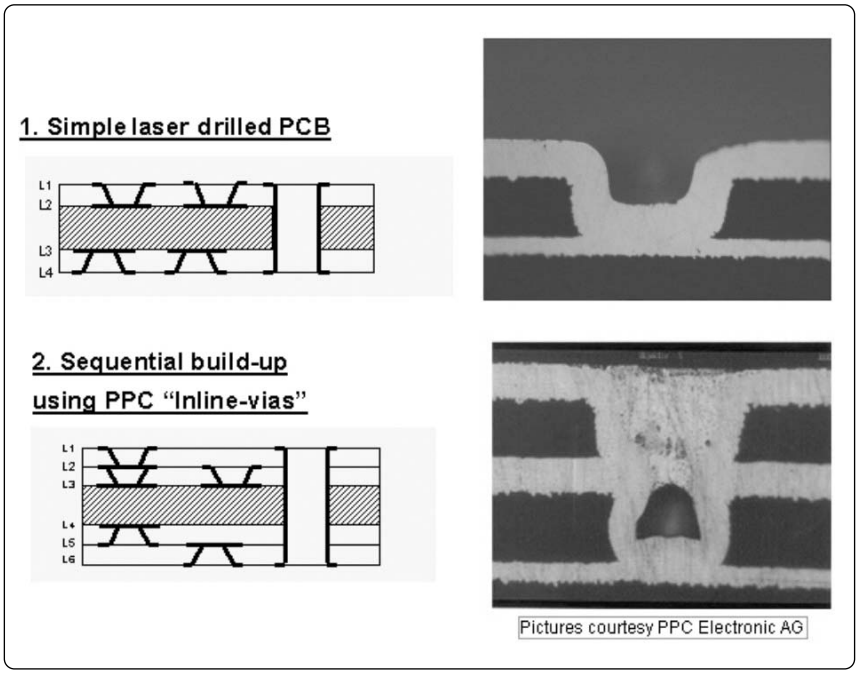


Figure 16. Single layer and stacked inline vias

High density microvia applications for telecom

The most complex of microvia applications is reserved for the ultra high-density telecom and datacom switches and routers. An example of one of these structures is shown in Figure 17. These systems require PCBs that have laser-drilled vias, stacked vias, PTHs and even buried vias. Sophisticated BGA ICs and FPGAs are often used to perform the advanced functions of these networking devices and must have circuits routed in the most efficient manner. A sequential build-up approach to the fabrication of the PCB can reduce the via congestion by routing signals to various inner layers while still using the minimal board footprint. The benefit is seen in the reduced layer count for a microvia board in comparison to a PCB designed with standard thru vias. The use of microvias will also reduce the amount of time that is needed to route these complex devices. This is because the auto-routing functions of the CAD layout software can easily determine efficient routing schemes for microvias.

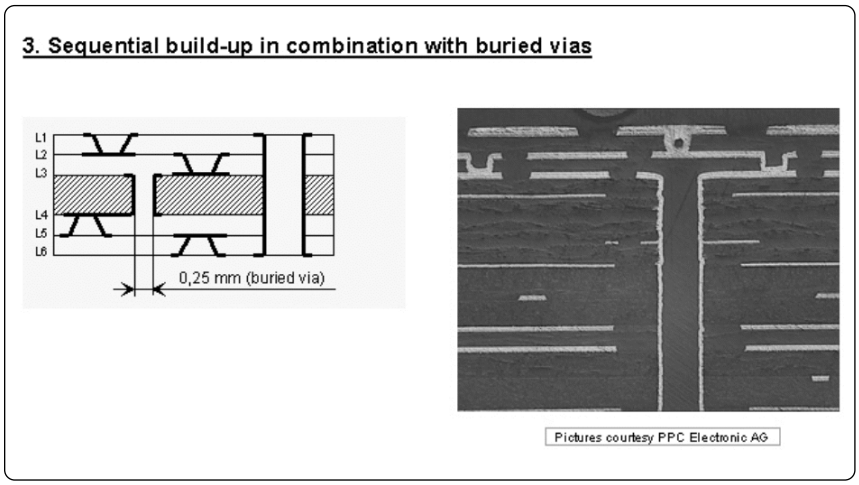


Figure 17. Ultra-high density board

Microvia manufacturing process comparison

Today's microvias can be created using a variety of processes, but these processes can be divided into two main categories, physical forming and chemical forming. With physical forming the two most common approaches are mechanical and laser drilling. Chemical processes exist that allow board manufacturer's to reduce the via size to it's smallest size and also use very little board space. Two common forms of chemical via forming are photo forming and plasma etching. A tabularized summary of these processes is shown in Figure 18.

Mechanical drilling requires very little investment by the PCB suppliers since the equipment that is used to process standard PTHs can be used to create controlled depth vias. The limitations of this approach are in the microvia's diameter and depth control accuracy of the drill press. Additionally, mechanical drilling requires drilling thru multiple layers of the PCB, so additional real estate is needed. The mechanical drilling approach is like inverting the back-drilling approach for standard PTHs.

Factor	*YAG - Laser*	*CO2 - Laser*	*Mechanical drilling*	*Plasma*
Via min. diameter	1-2 mil	12 mil	8 mil	3 mil
Via max. diameter	7 mils	14 mils	none	none
Via aspect ratio	<= 1:1	<= 1:1	<= 1 :1	<= 0.5 :1
Consistant dielectric thickness	Not so important	important	Not so important	Very important
Ablation rate (5 mil vias 1.5 mil dielectric)	4500 vias/min.	8500 vias/min.	Limited by sequential drilling	All vias etched simultaniously
Via clean after ablation	No	Yes	No	Yes
Special preparation prior to plating	No	No	No	Cu overhang removal
Proprietary process	No	No	No	Dyconex, APS
Type of Equipment	UV Laser	Pulsed CO2 Laser	Standard drilling machine	Plasma gas in Vacuum

Figure 18. Comparison of different manufacturing processes

Different microvia routing patterns

As circuit densities push higher and higher it is essential to find alternative methods for interconnecting devices and alleviating via congestion. With microvia technology, the designer is capable of utilizing via in pad technology to reduce the physical space requirements of routing high-density components. This via in pad approach shown in Figure 19 does not use any more additional space to route the signals than the mechanical outline of the SMT pad. This is a huge space savings on high-density components like BGA devices, but is limited to via diameters less then 4-5 mils. Larger diameter vias placed in the SMT pad could show voiding the component is soldered.

Microvias also open up the opposite side of the PCB for additional components and circuitry, since the vias do not extend thru the PCB. This extra space can be used to reduce the overall number of PCB layers, or add functionality that would not be possible with conventional via approaches.

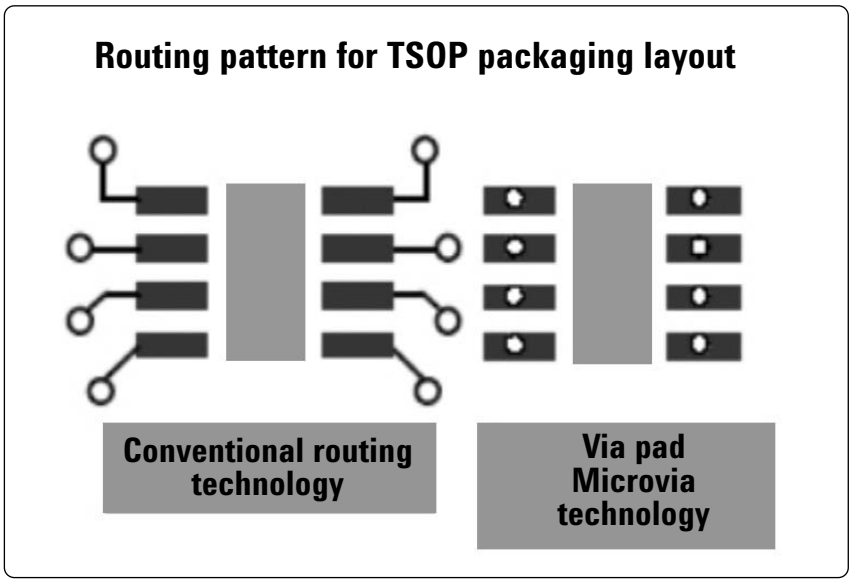


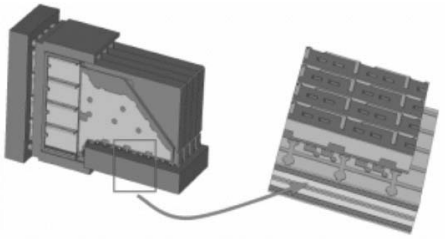
Figure 19. Via in pad methodology

Modeling and Simulation Case Study

Three configurations modeled with advanced design software

This section discusses the particular advantages of microvias in conjunction with SMT connectors with respect to the electrical behavior. The connector to board interface of the ERNI ERmet 0XT connector is taken as an experimental vehicle for this investigation. The following sketch in Figure 20 shows the connector-to-board interface of the connector receptacle that is soldered to a typical board with 16 layers and an overall thickness of 4mm. Using this realistic assumption, the following three typical configurations will be compared.

Looking at the entries in Figure 20, one can identify that the selected signal layer is different for setup three. The reason is, that a connection to a signal layer very close to the bottom of a PCB is typically a non-critical case because the remaining stub is very small and the diameter of the via and the antipad can be optimized to achieve good matching behavior. The critical case is the wiring from a connector to one of the upper signal layers in the PCB. Using conventional pressfit or SMT technology would lead to a via stub with a very large length. The very high capacitive load of this stub would result in a significant impedance mismatch which reduces the overall signal quality. This is the reason why this “worst” case is not taken into account and the two solutions are compared that are currently used to overcome this limitation. One of these options is to apply back drilling to these critical vias while the second one is the implementation of microvia technology.



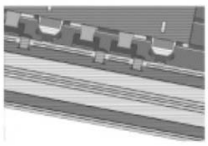
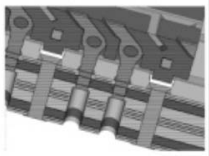
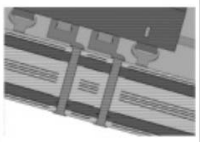
	Setup 1	Setup 2	Setup 3
Zoomed cross section			
Connector pad	SMT	Pressfit	SMT
Via type	Microvia	Throughole with backdrill	Through hole
Via diameter	0.35	0.5	0.3

Figure 20. Connector-to-board interface of connector receptacle

Characteristic impedance and crosstalk

The comparison is done by a simulation in the time domain using a full 3D high frequency field solver, where a step signal with a rise time of 50 ps (20 to 80%) is applied to the device under test. The differential signal is fed into the remaining part of the connector. Such a waveform is typical for a 10 Gbps serial transmission. As an outcome of the simulation experiment, the characteristic impedance Z0 of the system can be evaluated together with near end crosstalk (NEXT) and far end crosstalk (FEXT). Looking at the impedance mismatch in Figure 21, it is evident that the microvia approach showed the smallest impact on the impedance profile compared to the other two setups. It can be seen that the crosstalk in the relatively short vias of the setups with microvias and backdrilled pressfit connections is much lower compared to the long through hole vias. In both cases (far end crosstalk, near end crosstalk), the microvia approach showed a better crosstalk behavior.

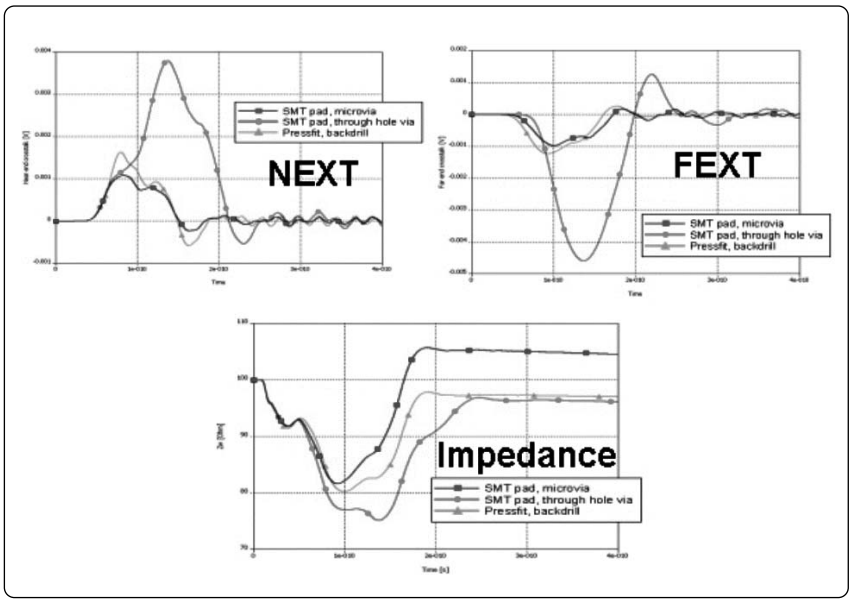


Figure 21. Connector system impedance mismatch

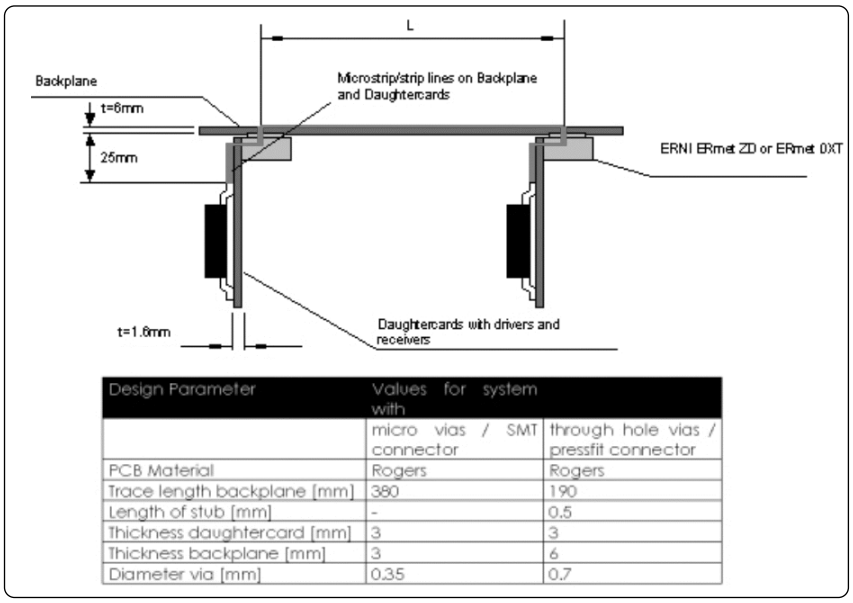
System simulation set up

This section discusses a comparison of the electrical performance of a serial link in two different backplane systems using either microvias in conjunction with a SMT connector or through hole vias with a pressfit connector. In a first step, both alternative scenarios are evaluated in a circuit simulator. The original goal of this investigation is to demonstrate the influence of several design parameters:

- between daughter cards
- connector to board interface
- width of transmission lines
- PCB material
- metalization layer in the PCB
- termination of the transmission lines
- type of transmission lines
- statistical variations

For this special application, two typical cases will be highlighted which demonstrate the superior behavior of microvia technology and SMT connectors compared to traditional pressfit connectors and through hole vias. The following general system scenario in Figure 22 and Figure 23 is used for this simulation study.

The signal path is a point-to-point connection between two integrated circuits on two different daughter cards. The daughter cards are plugged into a backplane printed circuit board. The connections are done using the ERNI ERmet ZD connector (pressfit pins) or the ERNI ERmet 0XT connector with SMT interface. The characteristic impedance of differential striplines is $Z0_{diff}$ = 100 W and the data rate applied is 10 Gbps using a Non-Return Zero (NRZ) 8B10B code. The table in Figure 22 also lists the different design parameters of the two experimental test vehicles.



Design Parameter	Values for system with	
	micro vias / SMT connector	through hole vias / pressfit connector
PCB Material	Rogers	Rogers
Trace length backplane [mm]	380	190
Length of stub [mm]	-	0.5
Thickness daughtercard [mm]	3	3
Thickness backplane [mm]	3	6
Diameter via [mm]	0.35	0.7

Figure 22. System scenario and design parameters

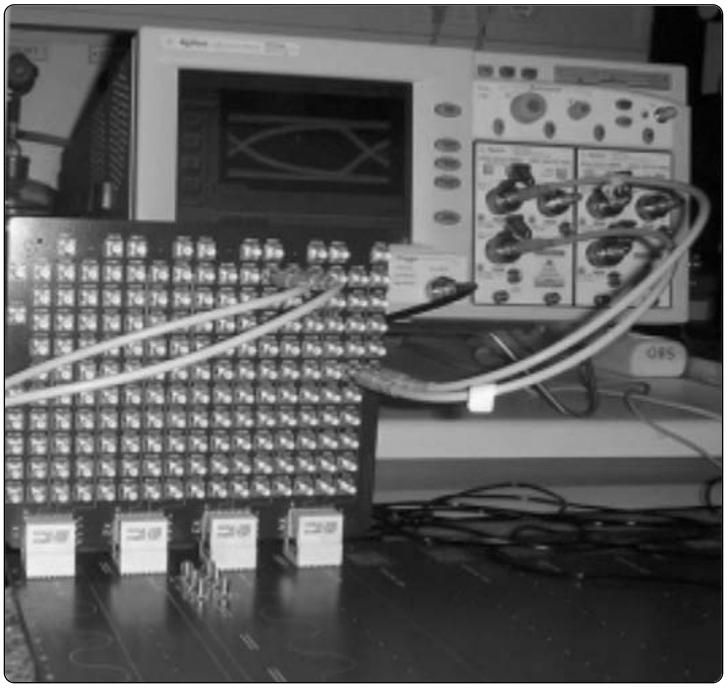


Figure 23. Simulation and measurement set up

Time domain results – simulation vs. measured

The diagrams in Figure 24 show both results from the two system setups from the measurements and the circuit simulations. The left column shows a very smooth eye diagram in both simulation and measurement of the system with microvia connections. In contrast, the right column contains the corresponding diagrams of the system with pressfit connectors and through hole vias. Here, we can see a heavily distorted eye with a reduced eye height compared to the results of the microvia system. The overall system behavior in the case of microvia interfaces is much smoother compared to the strong reflections in the case of plated through hole connections (PTH). The eye diagrams for the microvia are more open, indicating better performance at higher data rates. In both cases, a very good agreement between the simulated and measured behavior of the overall system behavior can be seen in these diagrams.

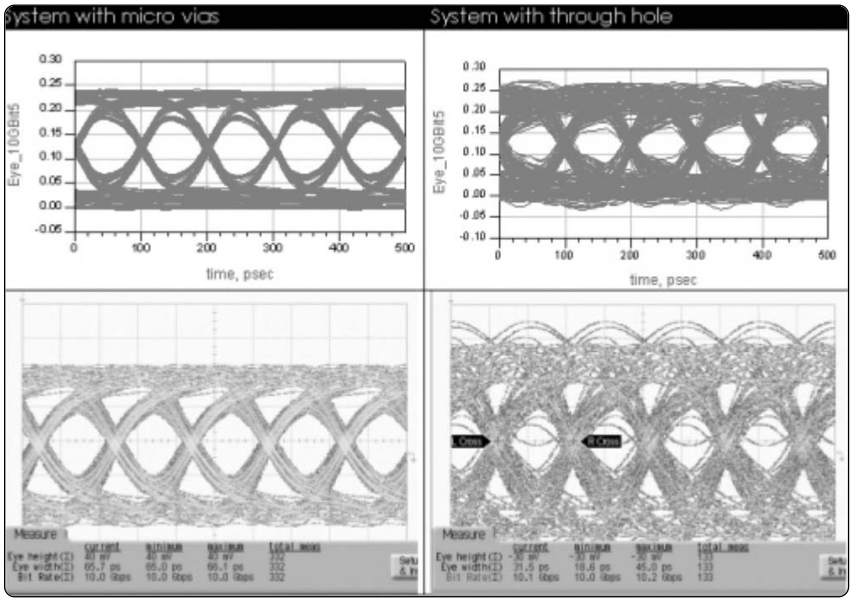


Figure 24. Eye diagrams from measured and simulated setups

Summary and conclusions

With data rates approaching 10 Gbps small geometry changes inside components and attachment features will become more evident. If care is taken in both the design of the surface mount connector and the board to connector interface, very high-speed serial links can be achieved. Understanding, testing and designing these features to be as quiet as possible is essential for optimizing the complete signal path. This paper has examined the frequency domain effects that limit the performance of backplane structures, as well as used intuitive time domain analysis such as the eye diagram and differential impedance profile. A design case study utilizing 3D field solver simulations of various microvia technologies and implementations allowed for a thorough investigation of attachment performance prior to board layout. A complete signal path has been created in a simulation environment by using models exported from the 3D field solver in conjunction with other known models of connectors and traces. A 4-port measurement tool environment has been utilized to characterize differential insertion loss, differential return loss, and differential eye diagrams in order to optimize the signal integrity of the microvia structures.

Web Resources

Learn more about Physical Layer Test Systems:
www.agilent.com/find/PLTS

For more information about PNA Series network analyzers go to:
www.agilent.com/find/PNA

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