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PLL's using a Charge Pump, High Divide-by-N Factors, and Decimation before Plotting

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Phase Locked Loops (PLL) using a Charge Pump, PLL's with High Divide-by-N Factors, and Decimation Before Plotting

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Introduction

A spreadsheet approach will be shown for designing a phase locked loop (PLL) that uses a charge pump. Although the spreadsheet is specific to SystemView by ELANIX, it may be used for other PLL systems using a charge pump. In SystemView, PLL's with a high divide-by-N factor (greater than ~1000) will result in very long plotting times. In these cases, decimation of the sink data can dramatically speed up the plotting times.

PLL Example 1 -- The Charge Pump

The 1st example is taken directly from a National Semiconductor application note (**Ref. 1**). **Figure 1** shows what the PLL looks like in SystemView. To simulate the 5.0 ma current sources in the charge pump, two step source tokens are used at the input to the charge pump: +5000 volts and -5000 volts Inside the charge pump, there is a resistor in series with each of the 5000 volt inputs. Each of the series resistors is set to 1.0 e6 ohms.

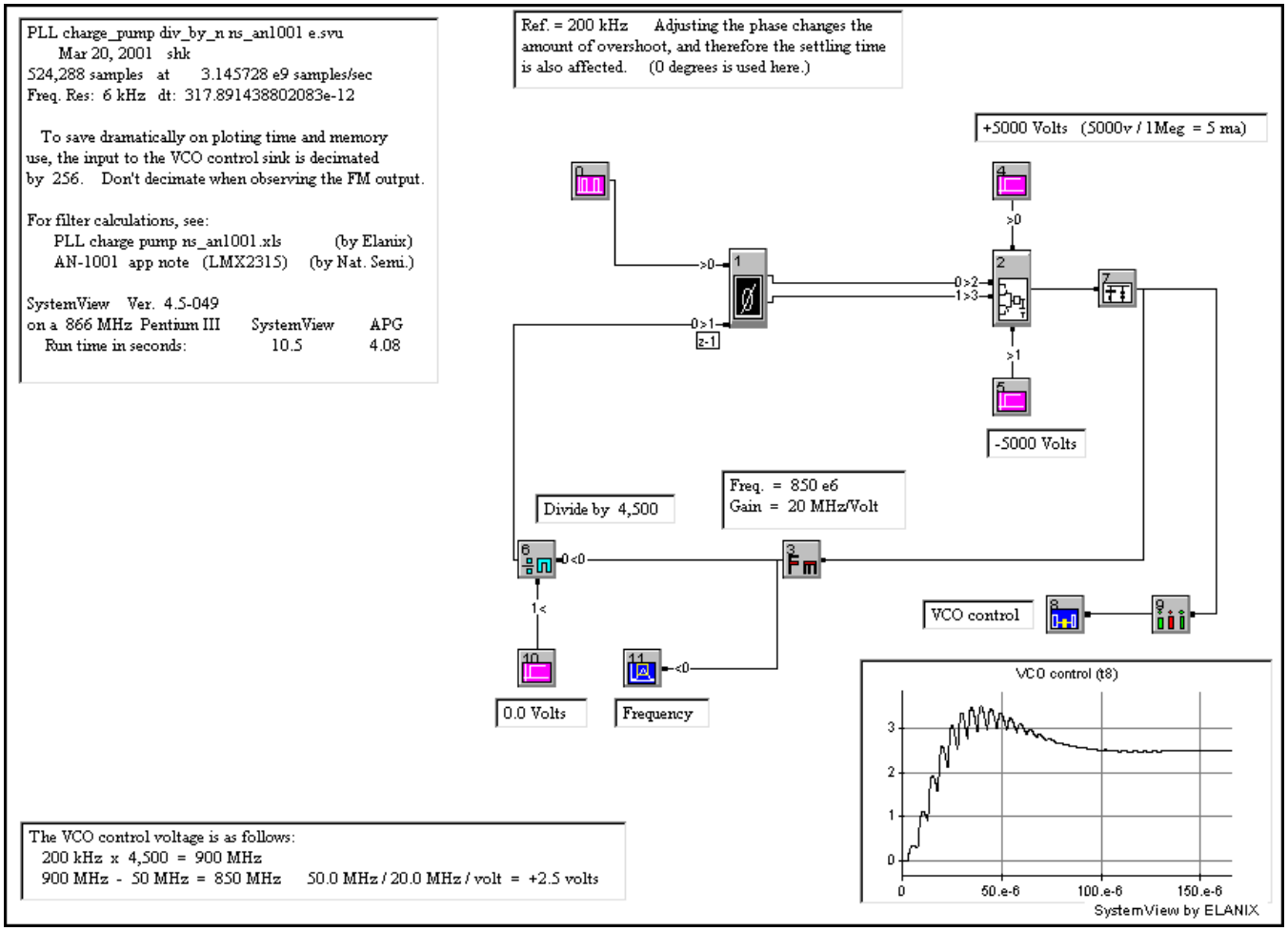

Figure 1. A divide by 4,500 PLL with a charge pump, followed by a low pass RC filter.

Other parameter values can be used for the current source that have almost no effect on the VCO control waveform. A 50.0 volt source with a 10.0 k resistor and a 5.0 volt source with a 1.0 k resistor each worked fine. However, there is a difference in each of the Bode plots for the various voltage/resistor combinations. The -3dB point for the lowpass cutoff frequency tracks the resistor value. When 5000 volts and a 1.0 Meg resistor are used, the lowpass -3dB point is moved far away from the point of inflection in the gain plot.

Charge Pump Filter

The filter in the charge pump token in (**Figure 2**) is simplified by setting some of the component values to near zero or infinity. The SystemView charge-pump circuit consists of an external voltage applied to an input resistor, followed by an R/C filter.

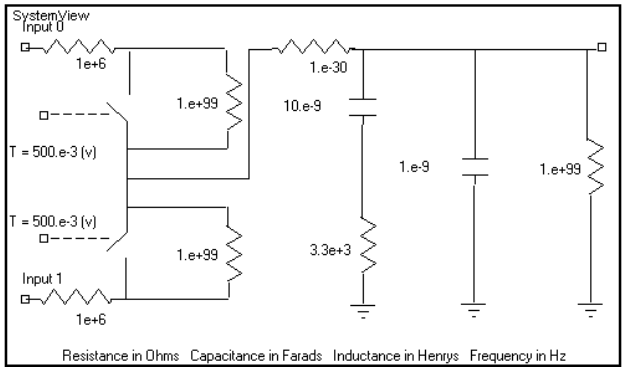

Figure 2. The RC_Cpump parameter window.
(divide by 4,500 Charge pump)

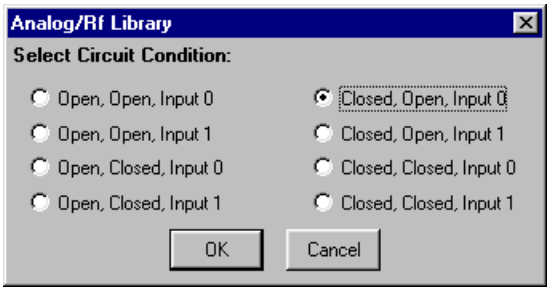

Figure 3. The select circuit condition window.

Again, the combination of an external voltage applied to the input resistor, is the current source for the SystemView model. To see the Bode plot of this token, select the "Closed (top switch), Open (bottom switch), Input 0 (top input)" circuit condition (**Figure 3**). The resulting Bode plot in **Figure 4** shows a local peak in the phase plot at 15.9 kHz (the gain plots' point of inflection).

With a real-world part, the voltage excursion inside of the RC_Cpump would be limited to values between the two limits of the power supply to the chip. This lack of voltage limiting in the SystemView model does not seem to cause any problems because within the PLL, the relatively slowly changing capacitor voltage is inside the control loop. If some sort of voltage limiting is desired, a partial solution is to use a limit token from the Function library at the output of the RC_Cpump token. Although the limit token is not used here, its parameters could be set as follows:

Input Max (+/- v):	5
Output Max (+/- v):	5

Reference Sideband Spur Filter

Additional filtering, is done by a RC-PLL token (**Figure 6**) to help in the rejection of the reference sidebands, or spurs. The circuit in **Figure 6** is also simplified by setting some component values to near zero or infinity.

In SystemView, these two filters (charge-pump and spur-filter) are represented by two separate tokens. This means that the two filters are buffered or isolated from each other, and that the RC components don't interact with each other as they do in the circuit in National Semiconductor's app note AN-1001 about the LMX2315. This is not a problem because the cutoff frequencies in the two filters are widely separated. AN-1001 indicates that the pole of the spur filter should be at least 5 times the loop bandwidth. In this example the point of inflection of the gain plot of the charge pump is 15.9 kHz, and the -3 dB cutoff point of the spur filter is 73 kHz (**Figure 5**).

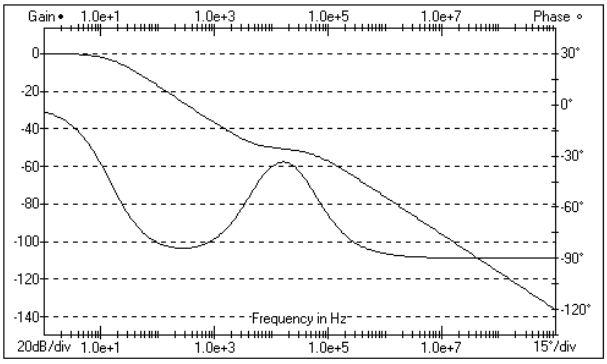

Figure 4. The Bode plot of the charge pump filter.
(divide by 4,500)

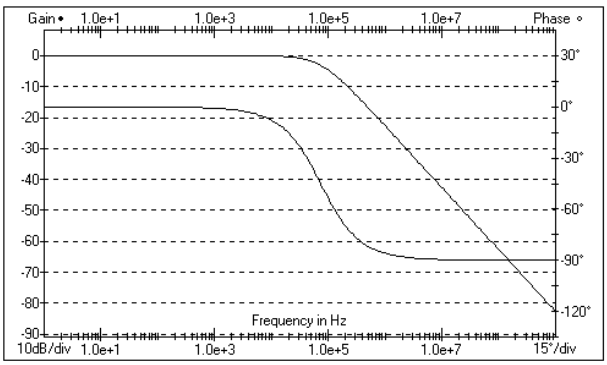

Figure 5. Bode plot of the sideband spur filter.
(divide by 4,500)

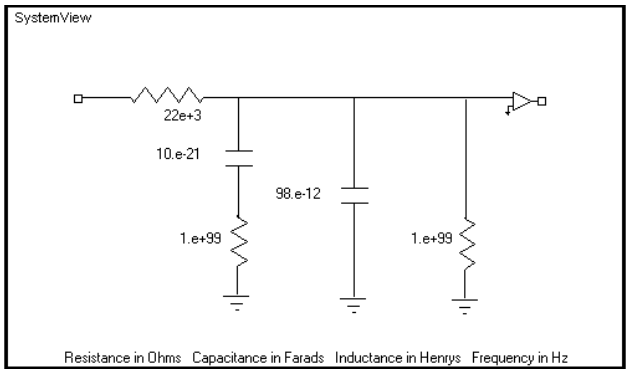

Figure 6. The RC_PLL parameter window. The 98 pF includes the VCO's 30 pF input cap. (divide by 4,500)

VCO or FM token

The loop reference is 200 kHz. A division ratio of 4,500 gives a locked in frequency of 900 MHz (**Figure 7**). The 900 MHz FM token (or VCO) has been set 50 MHz low to 850 MHz. The VCO has a gain of 20 MHz/Volt. Therefore, when locked in the control voltage to the VCO will be 2.5 volts (**Figure 1**).

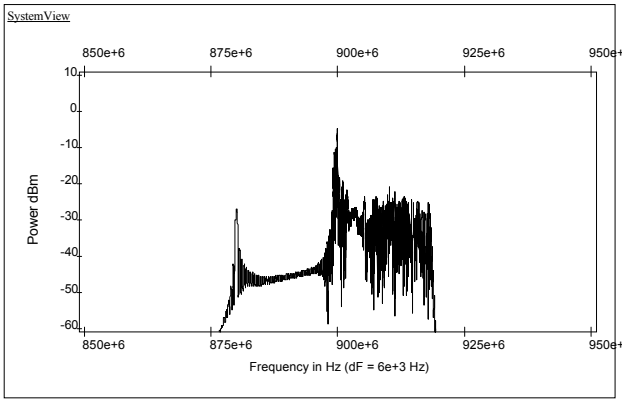

Figure 7. The 900 MHz frequency out of the FM token in the 1st example.
(Scale: 849 e6 to 951 e6, 11 dBm to -61 dBm)

Comm Library Divide by N Token

In March 1999, the Comm library divide-by-N token was given a 2nd input that is a control that selects one of the following modes of operation:

divide-by-N divide-by-N+1

In these examples, the control threshold is set above the fixed value of the control input (Step source) to cause the token to always divide-by-N.

In May 1999, the Comm library divide-by-N token was given an additional output signal. The original token always had a 50% duty cycle output with either an even or odd divide number. The additional output connection now provides a logic signal that is not 50% duty cycle for an odd divide factor. The output changes state only on a LOW-to-HIGH transition of the input frequency. Either output may be used in this PLL example.

Application note AN127A describes a dual modulus divider that may be used in place of the Comm library divider.

Each particular divider will produce its own unique initial lock-in waveform when used in a PLL circuit. To minimize the simulation time, the phase of the reference frequency may be adjusted to reduce the initial overshoot, or undershoot of the simulation.

PLL Calculations using a Spreadsheet

National Semiconductor's application note AN1001 (**Ref. 1**) shows the calculations for the charge pump. A Microsoft Excel™ spreadsheet was created to perform similar calculations. (There is a small, disagreement between the Application Information in the data sheet and the spreadsheet, but it is far less than the variation of 5% component values. The difference is apparently due to the spreadsheet carrying the full numerical precision through all the calculations, verses the application note that starts each calculation with a rounded-off number.) The spreadsheet is located at the end of this application note. The SystemView file and spreadsheet are saved as follows:

The 1st example with N = 4,500 is saved as:

PLL charge_pump div_by_n ns_an1001 e.svu
PLL charge pump ns_an1001.xls

The magnified view in **Figure 8** (using twice as many samples) shows the PLL settling time as about 150 uSec. This is close to the settling time shown in the National Semiconductor app note AN1001, Figure 10. (The SystemView plot seems to have a larger overshoot and smaller undershoot preceding the lock-in.)

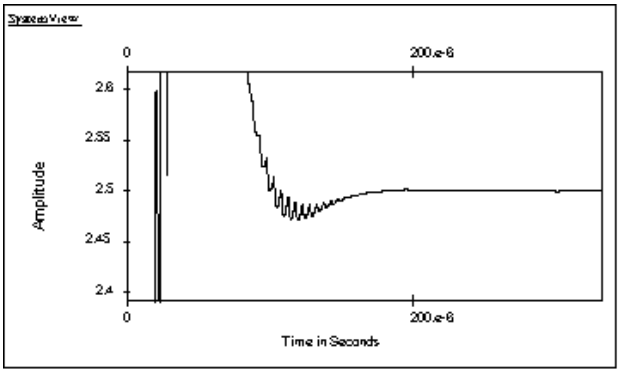

Figure 8. A magnified view of the VCO control voltage.

The SystemView Voltage Driven Charge-Pump verses a Current-driven Charge-Pump

The SystemView charge-pump circuit (**Figure 2**) consists of an external voltage applied to an input resistor, followed by two capacitors and a resistor to ground.

1.0 e6 ohms, 10 e-9 F with 3.3e3 ohms in series, 1.0e-9 F

The external voltage applied to the input resistor, is the current source for the SystemView model.

In National Semiconductor's application note (Page 2, Figure 3) the charge-pump circuit has the same two capacitors and a resistor to ground, but there is no input resistor or voltage source. This is because National Semiconductor's 2nd order filter is driven by a current source, "D_O". The two different circuits give almost exactly the same answer. However, the Bode plots for the two circuits will be different because of the extra input resistor in the SystemView model, (or the missing input resistor in the current mode model.)

Decimating Sink Data

Notice that the system in **Figure 1** has the output of the filter decimated by 256 before it is applied too the sink for viewing. This allows the full plot to appear in the *Real Time* sink. Without the decimation the plotting time would take many minutes as the computer software prepares hard disk space for the 524,288 samples. Also, with the 256 decimation the system run time is about 6% faster and the plotting time is very rapid.

Decimation can't always be used. In each system, the signal at the FM token is about 900 MHz. Since the system sample rate is 3,145,728,000 samples/sec, even a decimation by 2 will violate the Nyquist rule for sampled systems. (The system sample rate should be at least twice the signals rate.)

PLL Example 2

The 2nd PLL example with a divide factor of 35,440 is shown in **Figure 9**. National Semiconductor's data sheet for the LMX1511 (**Ref. 2**) shows the calculations for the charge pump. A 2nd Microsoft Excel™ spreadsheet was created to perform similar calculations. (Again, there is a small, disagreement between the Application Information in the data sheet and the spreadsheet.)

The 2nd example with N = 35,440 is saved as:

PLL charge_pump div_by_n ns_ds1995 e.svu
PLL charge pump ns_ds1995.xls

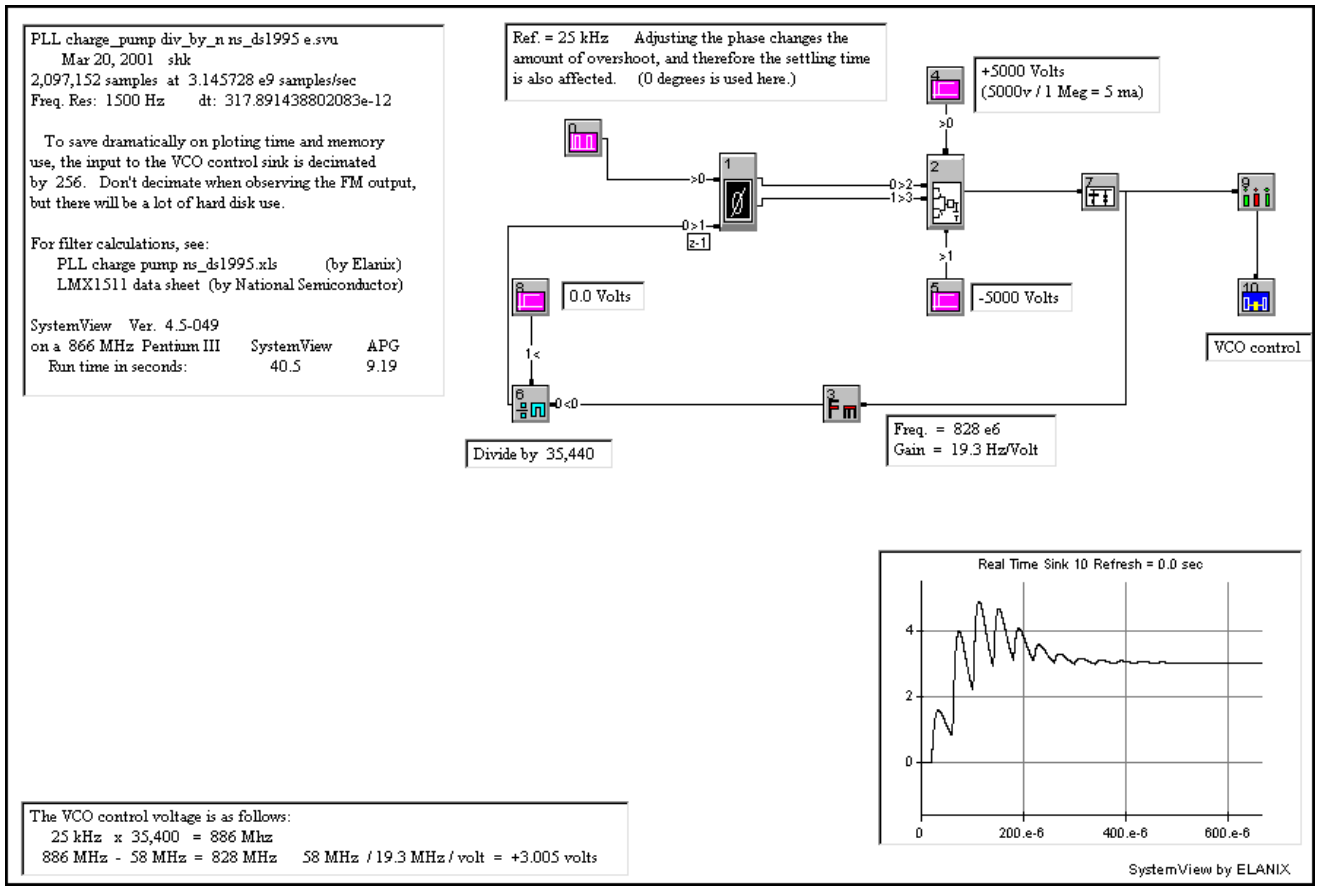

Figure 9. The divide by 35,440 PLL example with a charge pump, followed by a low pass RC filter.

The circuit values for the 2nd PLL example with a divide factor of 35,440 are shown in **Figures 10** and **11**. The Bode plots for the charge pump and the sideband filter are shown in **Figures 12** and **13**.

The magnified view in **Figure 14** (using twice as many samples) shows the PLL settling time as about 1.0 mSec. This is close to the settling time shown in the National Semiconductor data sheet, page 18.

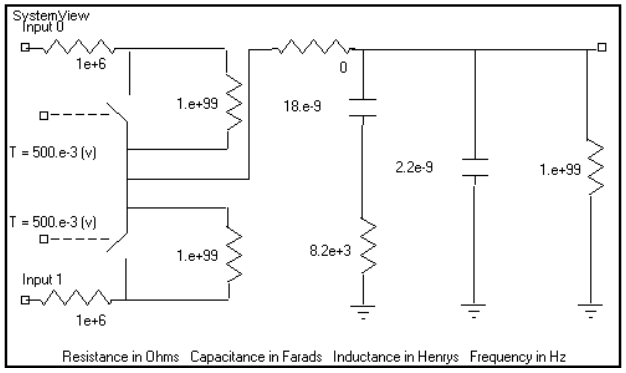

Figure 10. The divide by 35,400 charge pump filter.

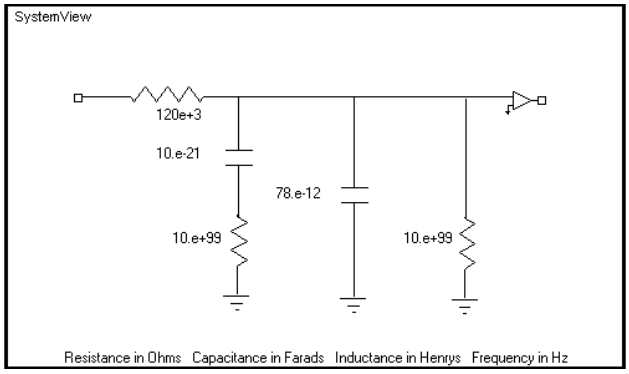

Figure 11. The divide by 35,400 sideband filter.

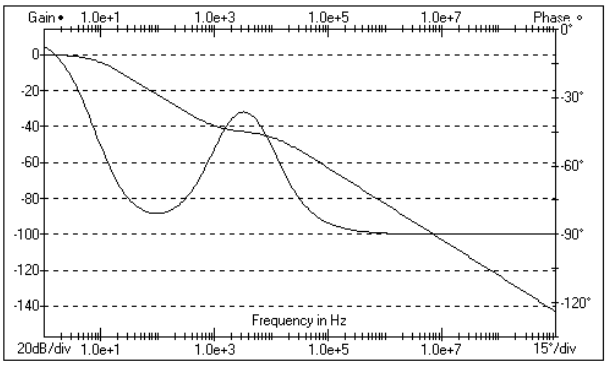

Figure 12. The divide by 35,400 Bode plot.

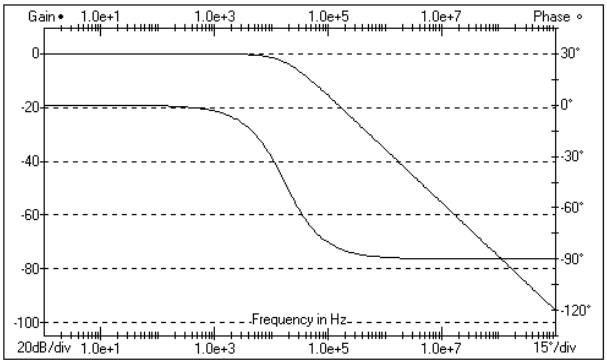

Figure 13. The divide by 35,400 sideband filter.

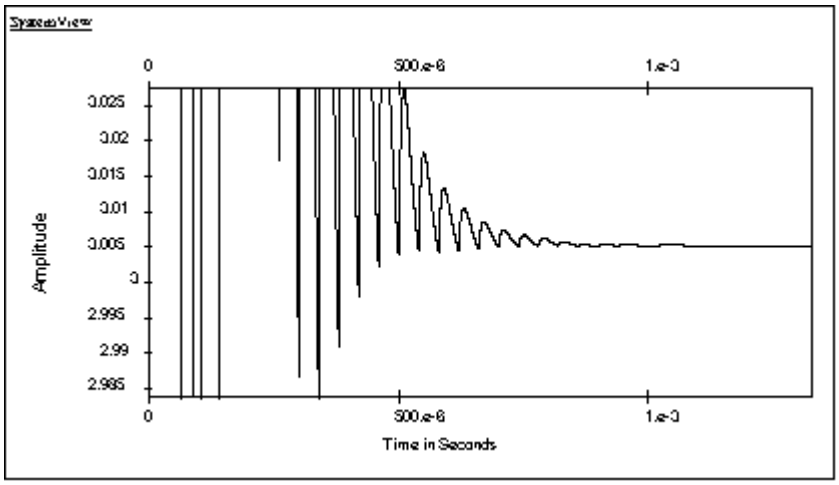

Figure 14. A magnified view of the divide by 35,400 VCO control voltage.

Adding Noise to the model

It is not the intent of this application note to cover the topic of PLL phase noise. However, **Figure 15** shows a PLL with noise added to various points in the system. The PLL is the same one used in **Figure 1**, but with eight noise sources which are documented in **Table 1**.

If token 13 or 19 is raised to 110.0 e-3 v, every once in awhile, the loop will jump out of it's locked state, and then re-lock. For more information on this model with its noise sources, please see to **Ref. 3**.

Noise Sources Used in Figure 13		
Type of Noise	Token Number	Amplitude (volts)
Reference	13	50.0 e-3
Divider	19	50.0 e-3
Phase detector	21 and 23	50.0 e-3
Loop filter	25 and 27	1.0 e-3
FM	15	1.0 e-3
VCO	17	1.0 e-3

Table 1.

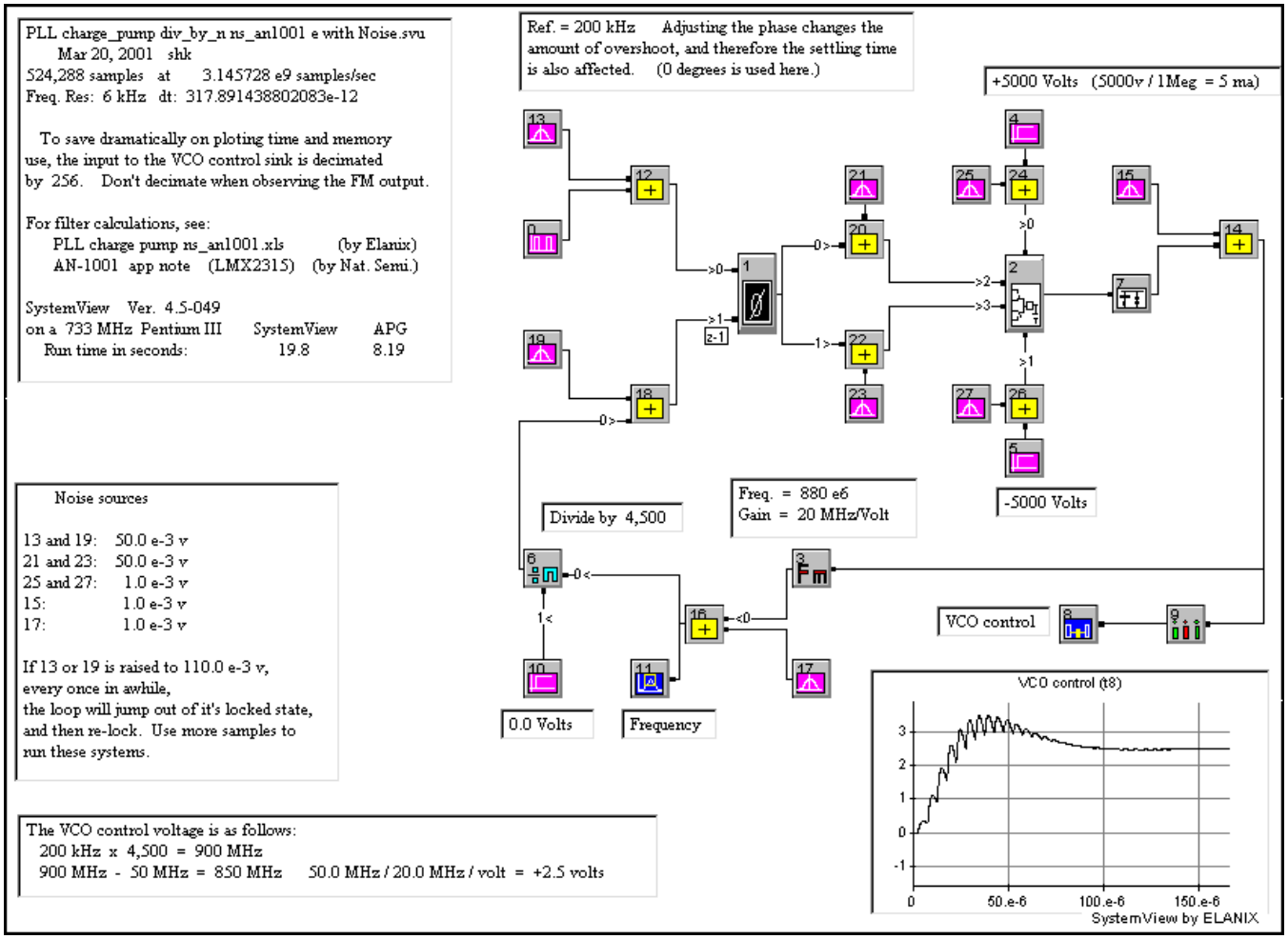

Figure 15. The PLL in **Figure 1** with eight noise sources added to the system.

Adding Reference Frequency Leakage to the model

Figure 17 shows a PLL with some reference frequency leakage. The PLL is the same one used in **Figure 1**, but an attenuator reduces the reference frequency by 30 dB, and then adds the signal to the input of the second loop filter. This leakage would normally find its way into the loop through various ways, such as:

1. The power supply for the charge pump.
2. The power supply for the VCO.
3. The printed circuit board layout.

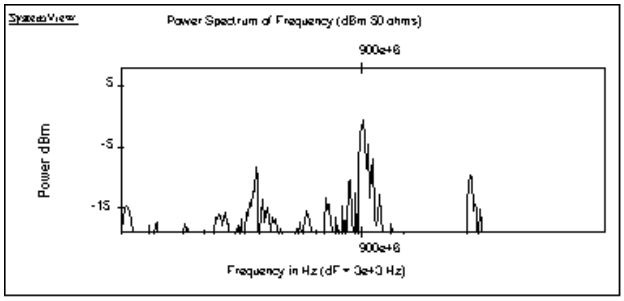

Figure 16. Plus and minus 200 kHz spurs on either side of the 900 MHz PLL frequency.

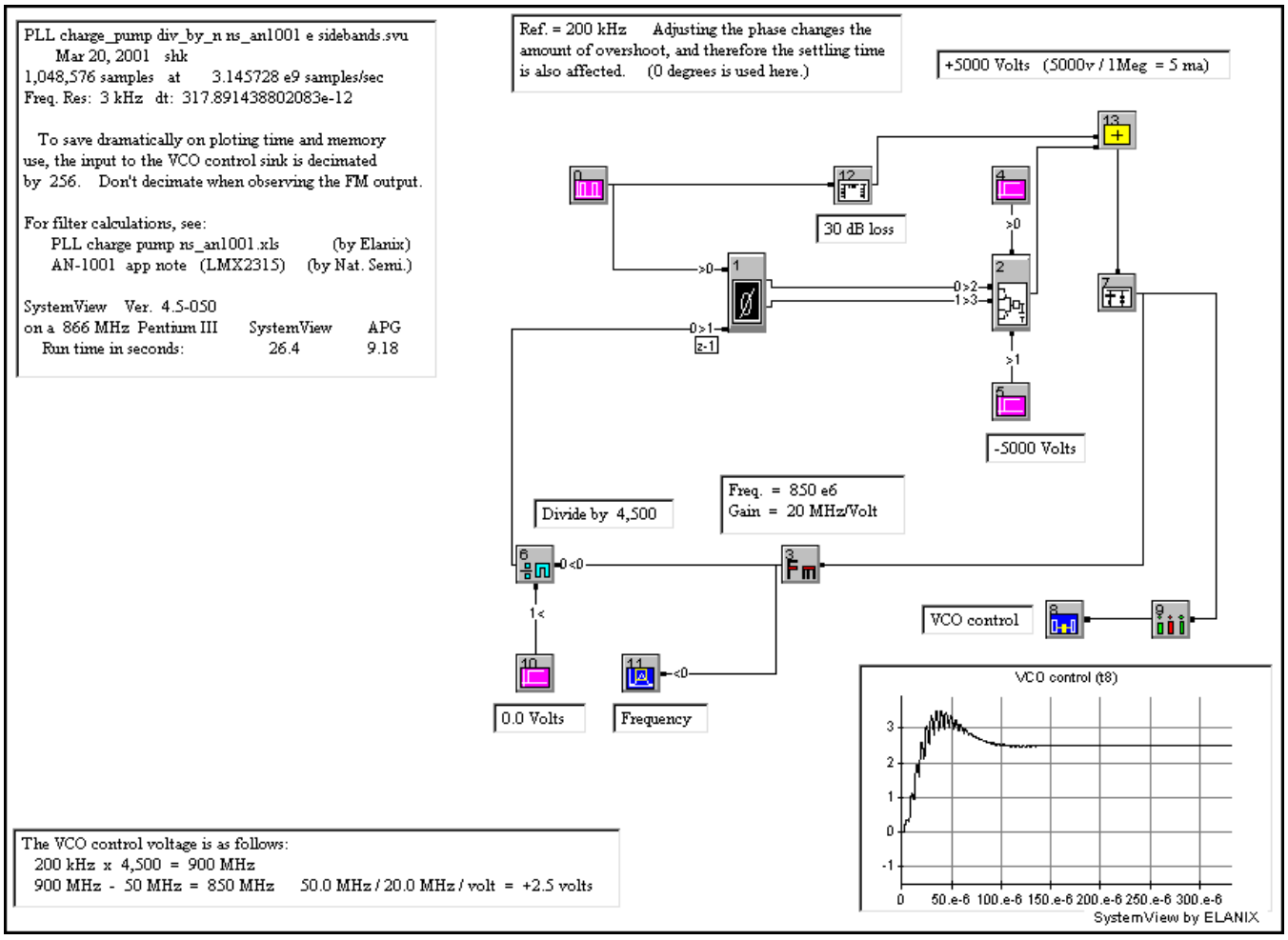

Figure 17. The PLL in **Figure 1** with some reference frequency leakage added to the system.

References

Ref. 1 An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops, National Semiconductor, AN1001, May 1996, Available on their Web site: http://www.national.com/search/corp_search_tools.html

Ref. 2 National Semiconductor data sheet for the LMX1501A/LMX1511 PLLatinum™ IC. Feb 1995, pages 15, 16, and 17

Ref. 3 Philip J. Rezin, Microwaves & RF, Mar 2000, pages 63 - 72 (specifically, pages 66 and 71).

For more information on SystemView simulation software please contact:

ELANIX, Inc.
5655 Lindero Canyon Road, Suite 721
Westlake Village CA 91362
Tel: (818) 597-1414
Fax: (818) 597-1427

Visit our web home page (www.elanix.com) to download an evaluation version of the software that can run this simulation as well as other user entered designs.

Calculation of Parts Values for a Charge Pump style PLL

Values Entered from the Keyboard

Kvco	20.00E+6	Hz/Volt	VCO gain (FM Mod gain).
Kcp	5.00E-3	Amp	Phase-detector/Charge-pump gain.
RFopt	900.00E+6	Hz/Volt	VCO frequency when optimized.
Fref	200.00E+3	Hz/Volt	Reference frequency.
BWhz	20.00E+3	Hz/Volt	Loop bandwidth in Hertz.
PhMar	45.0	degrees	Phase margin in degrees.
ATTEN	20.0	dB	Attenuation of reference spurs by the additional RC filter.
Lpf_R3	22,000	Ohms	RC-PLL filter series resistor (R3)

Calculated Charge Pump Filter and Low Pass Filter Circuit Values

N	4,500		Divide ratio = (RFopt / Fref)	
Ctog	1.076E-9	Farads	Capacitor only to ground.	(Charge pump)
Cwsr	10.50E-9	Farads	Capacitor with series resistor.	(Charge pump)
Rwsc	3.38E+3	Ohms	Resistor with series capacitor.	(Charge pump)
Lpf_C3	108.51E-12	Farads	RC-PLL filter capacitor to ground (C3).	(RC-PLL filter)

Calculated Charge Pump Current Source Parameters

To keep the current source relitively linear, use +500.0 and -500.0 voltage sources (Step Source) at the input to the charge pump token. Then calculate the current source series resistor as follows:

Rcp	100,000	ohms	Charge pump resistor (2 places). (Rcp = 500 / Kcp) The resistor after the switches (feeding the charge pump filter) is set to zero ohms.

Intermediate Calculations

BWrad	125,664	Radians	Loop bandwidth in Radians = (2 pi x BWhz)
T1calc	3.296E-06	Seconds	T1 = secPhMar - tanPhMar / BWrad = (1/cosPhMar) - tanPhMar / BWrad
T3calc	2.387E-06	Seconds	T3 = sqrt((10 exp((ATTEN / 20) - 1) / (2 x PI() x Fref) x 2)

Calculated loop bandwidth

BWcalcLT	5.6835E-06		BWcalcLT = tanPhMar x (T1calc + T3calc)
BWcalcLB	4.0172E-11		BWcalcLB = ((T1calc + T3calc) ^ 2) + (T1calc x T3calc)
BWcalcRT	4.0172E-11		BWcalcRT = BWcalcLB
BWcalcRB	3.2303E-11		BWcalcRB = BWcalcLT ^ 2
BWcalc	7.0439E+04	Hz	BWcalc = (BWcalcLT / BWcalcLB) x [(sqrt(1 + (BWcalcRT / BWcalcRB)) - 1]
T2calc	3.5461E-05	Seconds	T2calc = 1 / [(BWcalc ^ 2) x (T1calc + T3calc)]

C1 (Ctog -- Cap to ground in charge pump) Calculations

CtogLT	1.0000E+05		CtogLT = Kcp x Kvco
CtogLB	2.2327E+13		CtogLB = (BWcalc ^ 2) x N
CtogRT	7.2393E+00		CtogRT = (1 + (BWcalc ^ 2) x (T2calc ^ 2))
CtogRB	1.0837E+00		CtogRB = (1 + (BWcalc ^ 2) x (T1calc ^ 2)) x (1 + (BWcalc ^ 2) x (T3calc ^ 2))
Ctog	1.08E-9	Farads	Ctog = (T1calc / T2calc) x (CtogLT / CtogLB) x sqrt[CtogRT / CtogRB]

C2 (Cwsr -- Cap with series resistor in charge pump) Calculations

Cwsr	10.50E-9	Farads	Cwsr = Ctog x ((T2calc / T1calc) - 1)

R2 (Rwsc -- Resistor with series cap in charge pump) Calculations

Rwsc	3,377.3	Ohms	Rwsc = T2calc / Cwsr

C3 (LPF_C3 RC-PLL filter) Calculations

Lpf_C3	108.51E-12	Farads	Lpf_C3 = T3calc / Lpf_R3

The equations above are from National Semiconductor's application note AN1001 (May 1996)

Calculation of Parts Values for a Charge Pump style PLL

Values Entered from the Keyboard

Kvco	19.30E+6	Hz/Volt	VCO gain (FM Mod gain).
Kcp	5.00E-3	Amp	Phase-detector/Charge-pump gain.
RFopt	886.00E+6	Hz/Volt	VCO frequency when optimized.
Fref	25.00E+3	Hz/Volt	Reference frequency.
BWhz	5.00E+3	Hz/Volt	Loop bandwidth in Hertz.
PhMar	43.0	degrees	Phase margin in degrees.
ATTEN	10.0	dB	Attenuation of reference spurs by the additional RC filter.
Lpf_R3	120,000	Ohms	RC-PLL filter series resistor (R3)

Calculated Charge Pump Filter and Low Pass Filter Circuit Values

N	35,440		Divide ratio = (RFopt / Fref)	
Ctog	2.163E-9	Farads	Capacitor only to ground.	(Charge pump)
Cwsr	18.47E-9	Farads	Capacitor with series resistor.	(Charge pump)
Rwsc	7.15E+3	Ohms	Resistor with series capacitor.	(Charge pump)
Lpf_C3	78.0E-12	Farads	RC-PLL filter capacitor to ground (C3).	(RC-PLL filter)

Calculated Charge Pump Current Source Parameters

To keep the current source relitively linear, use +500.0 and -500.0 voltage sources (Step Source) at the input to the charge pump token. Then calculate the current source series resistor as follows:

Rcp	100,000	ohms	Charge pump resistor (2 places). (Rcp = 500 / Kcp) The resistor after the switches (feeding the charge pump filter) is set to zero ohms.

Intermediate Calculations

BWrad	31,416	Radians	Loop bandwidth in Radians = (2 pi x BWhz)
T1calc	1.384E-05	Seconds	T1 = secPhMar - tanPhMar / BWrad = (1/cosPhMar) - tanPhMar / BWrad
T3calc	9.361E-06	Seconds	T3 = sqrt((10 exp((ATTEN / 20) - 1) / (2 x PI() x Fref) x 2)

Calculated loop bandwidth

BWcalcLT	2.1636E-05		BWcalcLT = tanPhMar x (T1calc + T3calc)
BWcalcLB	6.6789E-10		BWcalcLB = ((T1calc + T3calc) ^ 2) + (T1calc x T3calc)
BWcalcRT	6.6789E-10		BWcalcRT = BWcalcLB
BWcalcRB	4.6812E-10		BWcalcRB = BWcalcLT ^ 2
BWcalc	1.8070E+04	Hz	BWcalc = (BWcalcLT / BWcalcLB) x [(sqrt(1 + (BWcalcRT / BWcalcRB)) - 1]
T2calc	1.3200E-04	Seconds	T2calc = 1 / [(BWcalc ^ 2) x (T1calc + T3calc)]

C1 (Ctog -- Cap to ground in charge pump) Calculations

CtogLT	9.6500E+04		CtogLT = Kcp x Kvco
CtogLB	1.1572E+13		CtogLB = (BWcalc ^ 2) x N
CtogRT	6.6891E+00		CtogRT = (1 + (BWcalc ^ 2) x (T2calc ^ 2))
CtogRB	1.0930E+00		CtogRB = (1 + (BWcalc ^ 2) x (T1calc ^ 2)) x (1 + (BWcalc ^ 2) x (T3calc ^ 2))
Ctog	2.16E-9	Farads	Ctog = (T1calc / T2calc) x (CtogLT / CtogLB) x sqrt[CtogRT / CtogRB]

C2 (Cwsr -- Cap with series resistor in charge pump) Calculations

Cwsr	18.47E-9	Farads	Cwsr = Ctog x ((T2calc / T1calc) - 1)

R2 (Rwsc -- Resistor with series cap in charge pump) Calculations

Rwsc	7,147.7	Ohms	Rwsc = T2calc / Cwsr

C3 (LPF_C3 RC-PLL filter) Calculations

Lpf_C3	78.01E-12	Farads	Lpf_C3 = T3calc / Lpf_R3

The equations above are from National Semiconductor's data sheet for the LMX1501A PLLatinnumTM (Feb 1995)

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